IBM

ZZ22-6953-0

SALES and SYSTEMS GUIDE

IBM BASIC COUNTER UNIT
COMPONENT DESCRIPTION AND USER'S GUIDE

This guide describes the organization and use of the IBM Basic Counter Unit. The IBM Basic Counter Unit monitors the various activities of a system and provides data for analyzing a system's performance. Among the systems that can be monitored are:

- IBM System/360
- IBM 1800 Data Acquisition and Control System
- IBM 1130 Computing System

Preface

The IBM Basic Counter Unit is referenced by Field Engineering Publications as the IBM 2989 Model 11 Basic Counter Unit. The type number, 2989 Model 11 is used by the Field Engineering Division for installation and maintenance information recording.

IBM Basic Counter Unit Related Publications:

IBM Basic Counter Unit Probe Assignment Planning Form, ZX22-6946

IBM Basic Counter Unit Patch Panel Planning Form, ZX22-6952

IBM 2989 Model 11 Basic Counter Unit, FETOM, ZY27-2236

IBM Systems Journal, Volume Eight, Number Four, 1969, G321-0019

IBM System/360 I/O Interface, Channel to Control Unit, OEMI, GA22-6843

Introduction to IBM System/360 Direct Access Storage Devices and Organization Methods, GC20-1649

IBM System/360 Principles of Operation, GA22-6821

First Edition (February, 1970)
This edition contains information formerly in, and obsoletes, Form Y22-6934-0. Changes are periodically made to the specifications herein; any such changes will be reported in subsequent revisions.

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This manual has been prepared by the IBM Systems Development Division, Product Publications, Dept. B98, PO Box 390, Poughkeepsie, N.Y. 12602. A form for readers' comments is provided at the back of this publication. If the form has been removed, comments may be sent to the above address.

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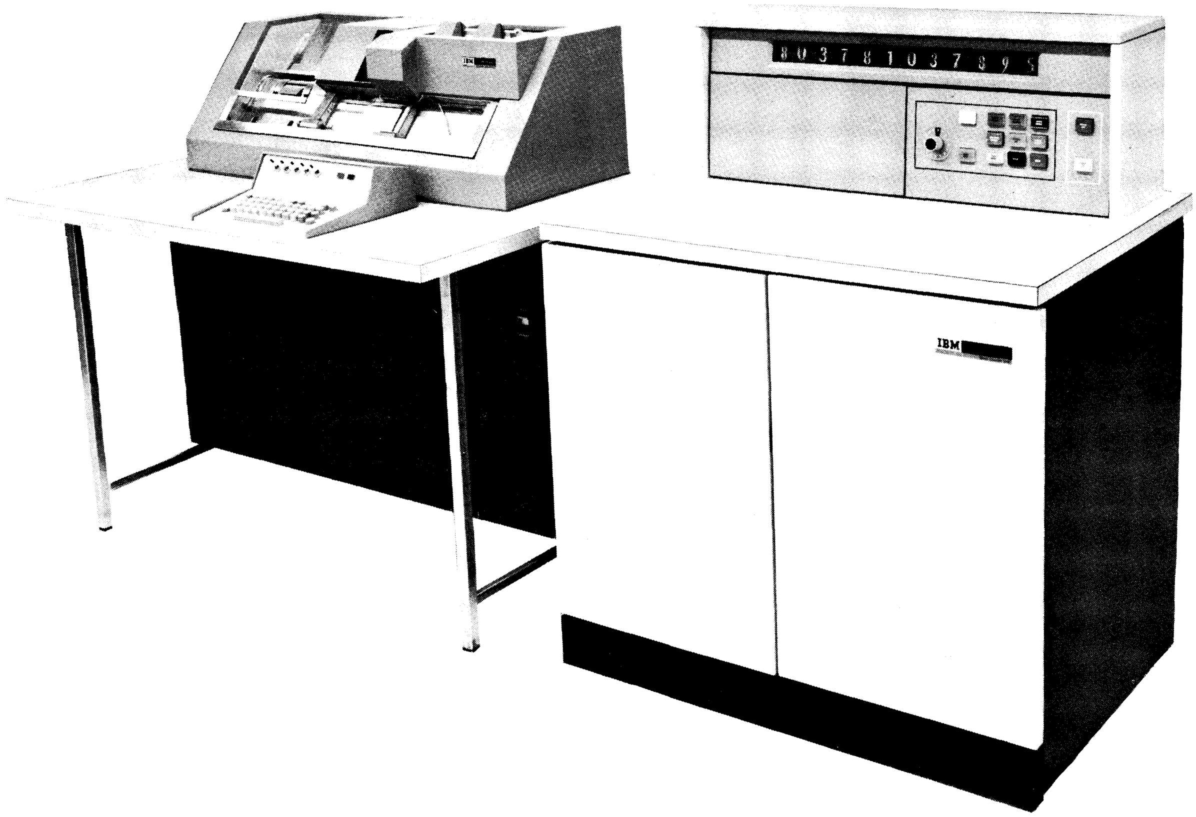


IBM 1058 Printing Card Punch Model 2 Attached to IBM Basic Counter Unit

PURPOSE AND FUNCTION

Data Processing Management is concerned with optimizing the use of a computing center installation. Their need for the system is to:

Improve performance.

Evaluate requirements for expansion.

Determine the effects of upgrading the system to a larger and faster system.

Evaluate programming improvements.

The IBM Basic Counter Unit (Frontispiece) measures the various activities of a system and provides data for analyzing a system's performance.

The Basic Counter Unit consists of 16 counters. Each counter is 11 decimal digits wide and counts or times events at the maximum rate of 1 MHz. Counter output is obtained by visual display or by punched card.

To meet the wide range of measurement applications, the Basic Counter Unit incorporates a patch panel of combinatorial logic. The user selects time inputs, incident counts, logic functions, or combinations of these by wiring the patch panel. Input signals to the Basic Counter Unit are obtained from monitor probes attached to the desired function points in the system being measured. Among the systems that can be monitored by the Basic Counter Unit are:

IBM System/360
IBM 1800 Data Acquisition and Control System
IBM 1130 Computing System

Figure 1 illustrates general applications of the Basic Counter Unit; Figure 2 is an example of a measured system profile.

DESCRIPTION

Monitoring is done by attaching probes at specified points on the equipment to be monitored, by setting up on the patch panel the logic that specifies the functions to be measured on specific counters, and by collecting information in counters and analyzing it.

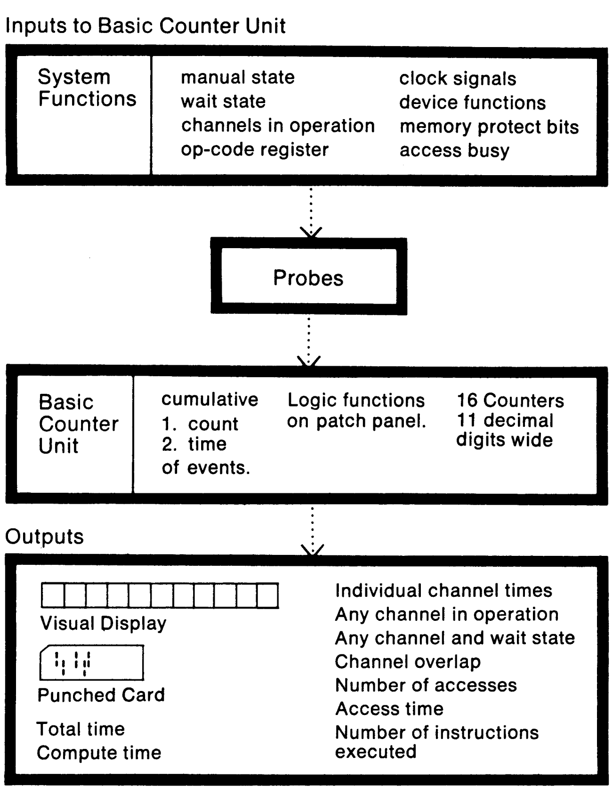


Figure 1. General Applications of the Basic Counter Unit

Counter Number	Measured Function
0	Total Time (not manual)
1	Compute Time — The time CPU is actually executing instructions.
2	Multiplexer Channel Time — The time multiplexer channel is in operation. Note 1
3	Selector Channel 1 Time — The time Selector Channel 1 is in operation. Note 1
4	Selector Channel 2 Time — The time Selector Channel 2 is in operation. Note 1
5	Any Channel in Operation — The logical OR of the above 3 channels in operation.
6	Any Channel AND Wait State — The logical AND of any Channel in operation and not compute.
7	Selector Channel 1 — Selector Channel 2 Overlap — The logical AND of selector channels 1 and 2.

Note 1. Devices on a channel may be in operation for a greater time than the channel.

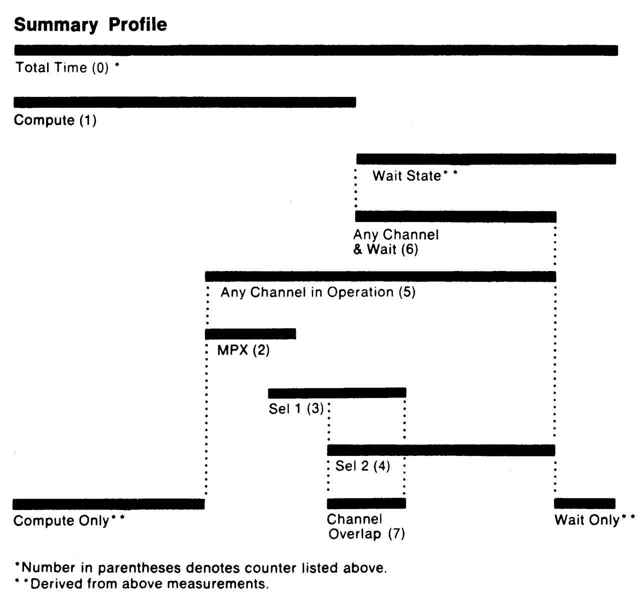


Figure 2. Example of a Measured System Profile

The connection of the IBM Basic Counter Unit to the equipment to be monitored is illustrated in Figure 3. The monitor probe cables, 15 feet each, terminate at a centrally located junction box, close to the units to be monitored. The monitor probe cable may be extended from 15 feet to 35 feet by connecting a 20-foot monitor probe extension cable. The junction box has 10 connectors for receiving the 10 monitor probe cables. From the box, the signals are routed via a signal cable to the Basic Counter Unit. The signal cable is 50 feet long.

The Basic Counter Unit (Figure 4) operator's panel contains: the pushbuttons and lights for operating the Basic Counter Unit, a decimal-digit display for displaying counter contents, a switch for selecting the counter to be displayed, a patch panel, and a desk surface for the operator. The operator wires the patch panel, using the combinatorial logic, for the functions to be measured and the counters to be used in the measurement.

The Basic Counter Unit has 16 counters. A single display on the operator's panel contains 12 windows for displaying the contents of the 16 counters. The leftmost window, backlighted in red, identifies the counter being displayed. Counters 0-15 are identified by the digits 0-15, respectively. The other 11 windows display the data for a particular selected counter.

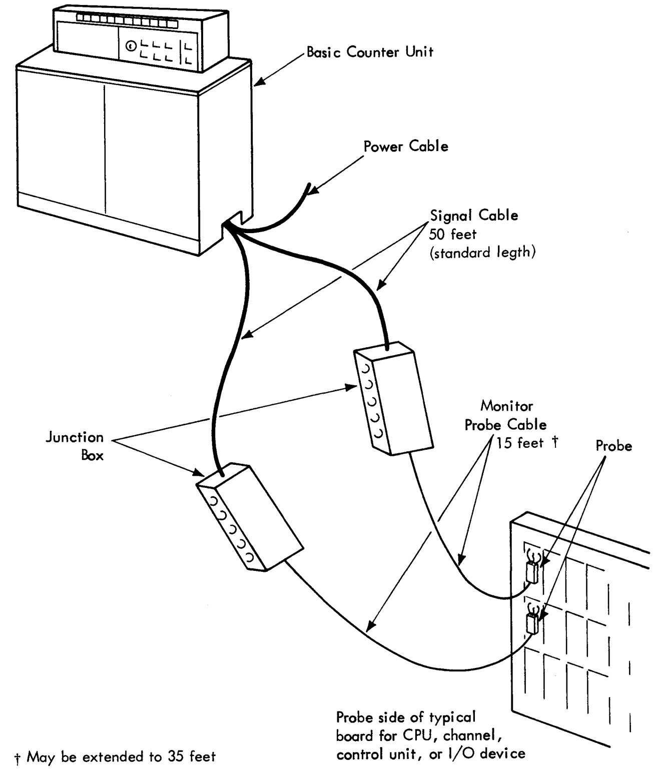


Figure 3. Basic Counter Unit Configuration

Power and Portability: The Basic Counter Unit weighs 225 pounds and is mounted on locking casters. The standard Basic Counter Unit uses 115-volts, 60-Hz power. A 50-Hz power version is available for export. The power source for the Basic Counter Unit must be a primary outlet. To avoid electrical interference, do not connect the Basic Counter Unit to convenience outlets on the CPU or I/O devices.

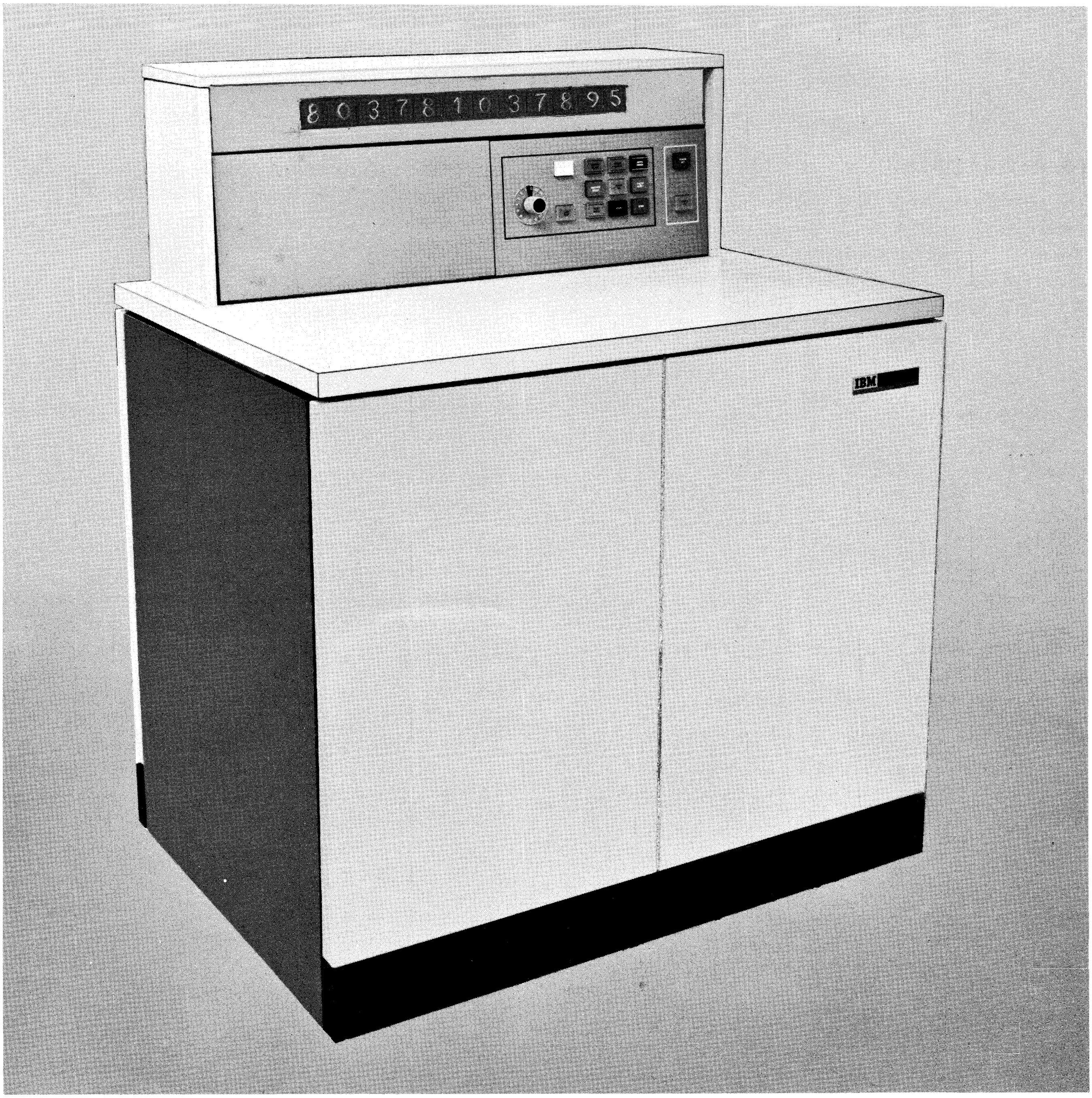


Figure 4. IBM Basic Counter Unit

Operating the IBM Basic Counter Unit

OPERATING CONTROLS

The operating controls on the operator's panel of the IBM Basic Counter Unit (Figure 5) consist of: eight pushbutton switches, four indicator lights, a counter select rotary switch, and a decimal digit display. These controls, when selected in their proper sequence, control the operation and test functions of the Basic Counter Unit.

Pushbutton Switches

Power-On (backlighted)
Power-Off
Start
Stop
Machine Reset
Check Reset
Punch Go (backlighted)
Lamp Test (backlighted)

Power-On activates the voltages within the Basic Counter Unit. The pushbutton is backlighted to indicate when normal power is on.

Power-Off turns off all dc and ac voltages in the Basic Counter Unit beyond the main power control compartment. Note that the backlighted power-on pushbutton is also turned off.

Start enables all counters, allowing monitoring to begin. Note that the count-enable light turns on. If the start hub of the patch panel is wired, it overrides the start and stop pushbuttons. See "Appendix F."

Stop disables all counters, stopping the monitoring. Note that the count-enable light turns off. If the stop hub of the patch panel is wired, it overrides the stop and start pushbuttons. See "Appendix F."

Machine Reset resets the contents of all counters and patch panel latches to zero.

Check Reset resets (turns off) the interface check indicator light. A new punch cycle can now be initiated.

Punch Go initiates a card punch operation. The pushbutton is backlighted and remains on until the completion of the punch operation. The operation punches the contents of 16 counters on four IBM cards. If the punch go pushbutton is inoperative, check the intfc check indicator light.

Lamp Test is pressed to test if the decimal digit display lamps are operating. The lamp-test pushbutton is backlighted and remains on until it is pressed again. Once this switch is set, it is used with the counter select rotary switch to test proper indication of digits 0-9 on each of the 12 decimal digit display lamps.

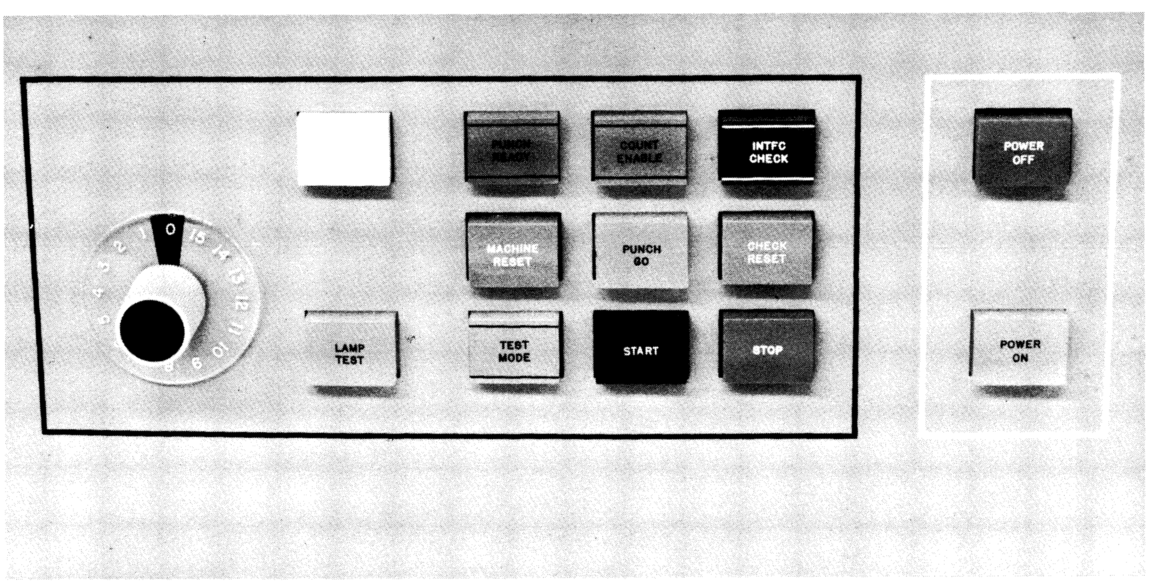


Figure 5. Operating Controls

Indicator Lights

Punch Ready
Count Enable
Intfc Check
Test Mode

Punch Ready indicates that the IBM 1057/1058 Card Punch is ready to accept data from the Basic Counter Unit.

Count Enable signifies that timing and counting signals are being accepted by the Basic Counter Unit. This indicator light is activated by the start switch. The light is turned off when either the stop hub is activated or the stop switch or machine reset switch is pressed.

Intfc Check (Interface Check) denotes that an error has occurred during a counter select sequence of a card punch operation or during a data transfer between the Basic Counter Unit and the Punch. The light remains on until check reset or machine reset switch is pressed.

Test Mode is on when the Basic Counter Unit is in test mode. In this state, the Basic Counter Unit is disabled from accepting input pulses from any external sources. See "Appendix F."

Counter Display Rotary Switch

This 16-point (0-15) rotary switch selects the counter to be displayed on the decimal digit display.

Decimal Digit Display

The decimal digit display (Figure 6), a row of 12 decimal digit display indicators, shows the static or dynamic accumulation of any selected counter. The leftmost digit, backlighted in red, indicates which of the 16 counters has been selected for display by the counter display rotary switch. The remaining 11 digits display the decimal value of the selected counter.

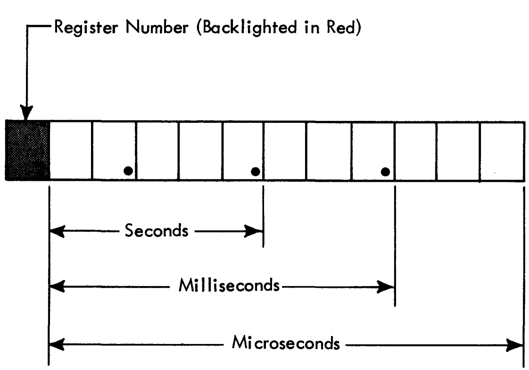


Figure 6. Decimal Digit Display

CONNECTING THE MONITOR PROBES

The following standard accessories are supplied with each Basic Counter Unit to monitor signals from systems and I/O devices for measurement:

20 monitor probes with connected monitor probe cables (15 feet each).
10 monitor probe extension cables (20 feet each).
2 junction boxes.
2 signal cables (50 feet each).

Monitor Probe Description

The Basic Counter Unit connects to a system by using a specially designed non-interfering monitor probe. Monitor probes are connected to pin locations on the back panel of the equipment being monitored. The monitor probe connection procedure is similar to the oscilloscope connection procedure used by a customer engineer. See *IBM 2989 Model 11 Basic Counter Unit,* FETOM,ZY27-2236, for the approved probe attachment points for IBM System/360, IBM 1800 Data Acquisition and Control System, and IBM 1130 Computing System.

In measuring a system, the Basic Counter Unit requires data from primary sources or generated sources or both.

A primary source is when the Basic Counter Unit records data directly from the system to which the monitor probes are attached. Primary sources are listed in "Appendix A" under *ALD.*

A generated source is when the Basic Counter Unit uses a combination of primary sources through its combinatorial (Boolean) logic on the patch panel. Generated sources are listed in "Appendix B" under *Combinatorial Logic.*

The monitor probe is a high-impedance differential input device that is suitable for monitoring signal lines in most IBM circuit families without disturbing the normal operation of the circuit.

The probe contains a miniature differential amplifier, which is capable of detecting a voltage change from a reference voltage. A voltage at one level during one state (CPU active) will change when the state changes (CPU wait). The differential amplifier in the probe detects this voltage change and drives a signal to the Basic Counter Unit. The operating power for the monitor probe is obtained from the Basic Counter Unit.

Each probe consists of a module with six protruding wires (Figure 7). Supplied with the probes are adapters that slip on to allow attachment to the pins on the systems or I/O devices being monitored. An example of the *IBM Basic Counter Unit Probe Assignment Planning Form,* ZX22-6946, appears in "Appendix C."

Monitor Probe Cable

The length between the monitor probe and the junction box is called the monitor probe cable. Each Basic Counter

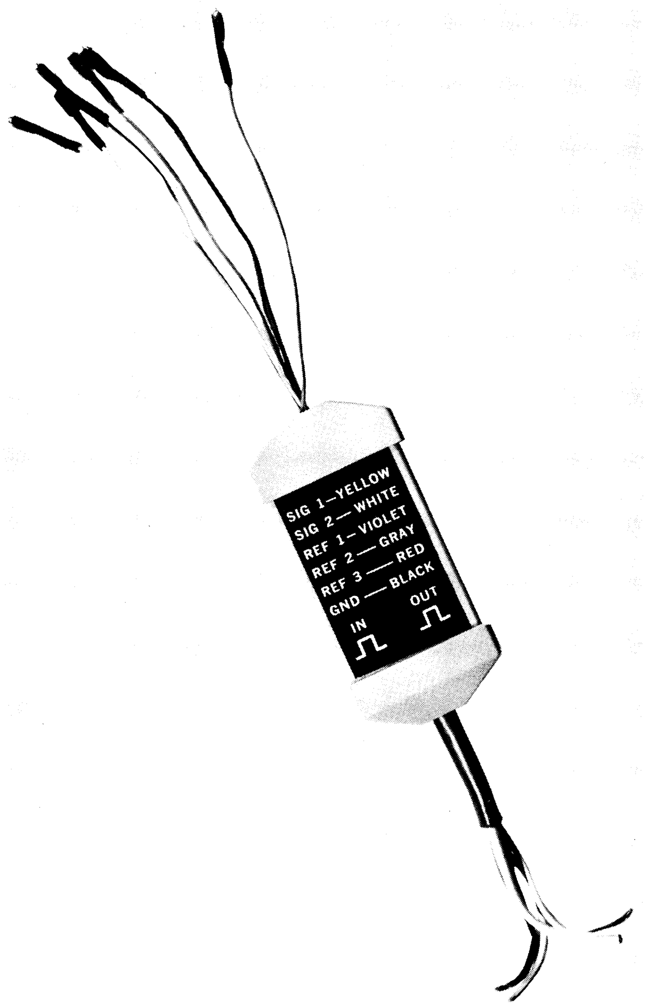


Figure 7. Monitor Probe Module

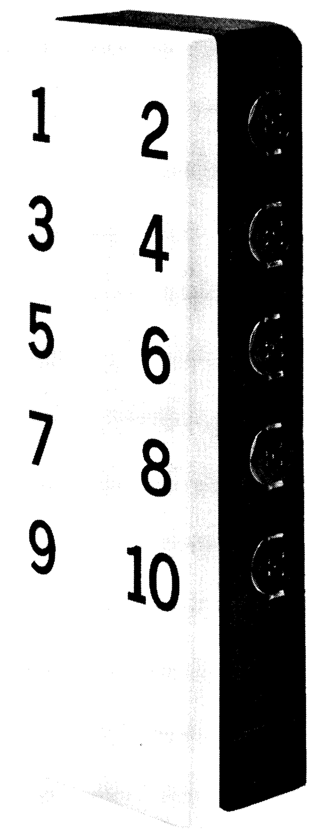


Figure 8. Junction Box

Unit is supplied with 20 monitor probes with connected monitor probe cables; each monitor probe cable is 15 feet long.

Monitor Probe Extension Cable

Any 10 of the 20 monitor probe cables may be extended from 15 feet to 35 feet by connecting a monitor probe extension cable to a monitor probe cable. Each Basic Counter Unit is supplied with 10 monitor probe extension cables; each monitor probe extension cable is 20 feet long.

Only one monitor probe extension cable may be connected to any monitor probe cable because an inconsistent result may occur due to signal loss.

Junction Box

Each Basic Counter Unit is supplied with two junction boxes. Each junction box (Figure 8) receives signals from up to ten monitor probes for transfer to the Basic Counter Unit and receives power from the Basic Counter Unit for transfer to the monitor probes.

Each junction box connects a maximum of ten monitor probe cables to one signal cable.

Signal Cable

The length between the junction box and the Basic Counter Unit is called the signal cable; each signal cable is 50 feet long. Each Basic Counter Unit is supplied with two signal cables.

Each signal cable receives signals from up to ten monitor probes through the junction box and transfers the signals to the Basic Counter Unit. Also, each signal cable receives power from the Basic Counter Unit and transfers the power through the junction box to the monitor probes.

WIRING THE PATCH PANEL

The patch panel (Figure 9) is a three-section panel to the left of the operating controls under a cover plate. Monitored signals from the probes are present in the two

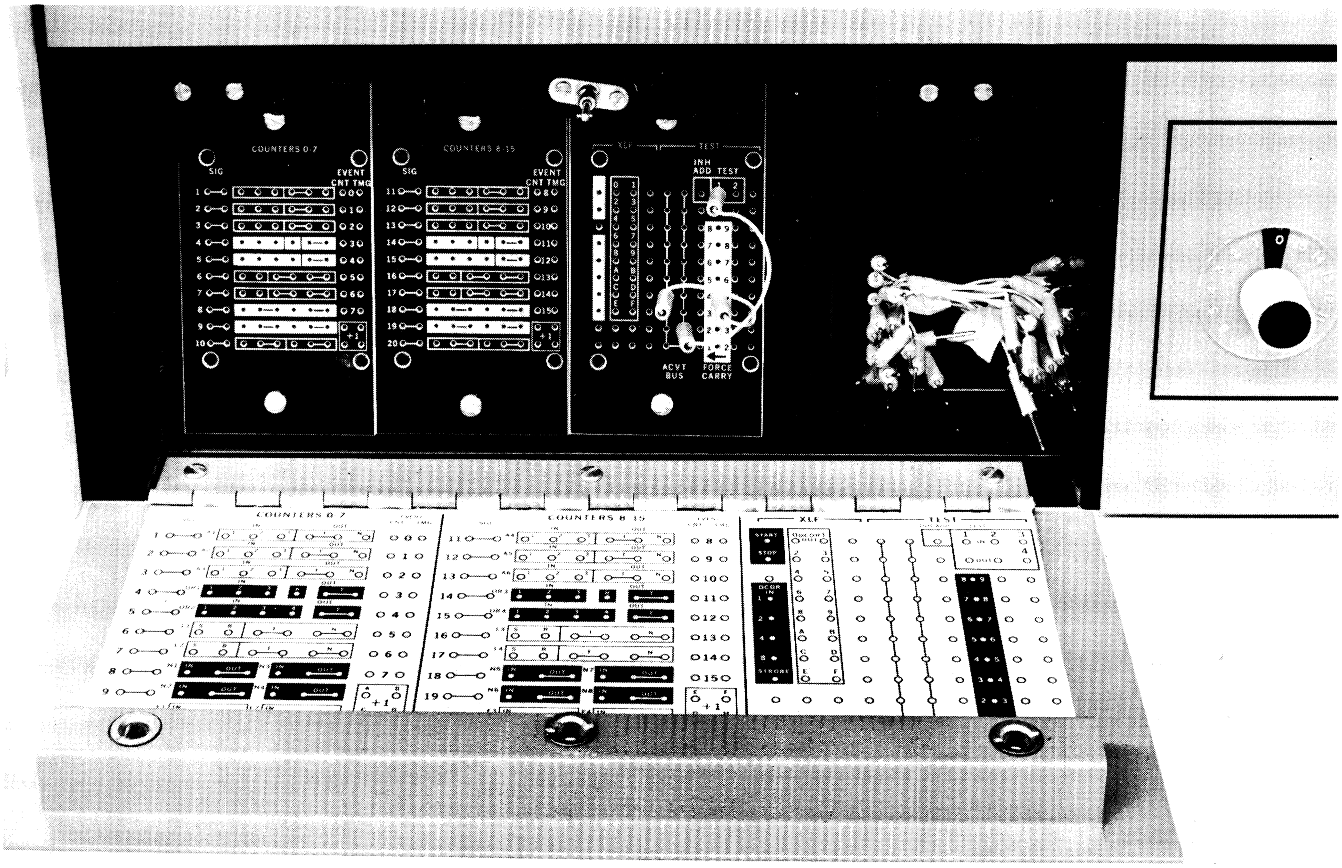


Figure 9. Open Cover Plate

leftmost panels (called operational patch panels). Operational patch panel 1 is associated with counters 0-7; operational patch panel 2 is associated with counters 8-15. Both operational patch panels are functionally identical. Signals from operational patch panel 1 can be interconnected to operational patch panel 2. See "Appendix D" and "Appendix E" for a detailed description of operational patch panel 1, and operational patch panel 2.

The rightmost section of the patch panel contains additional logic and test functions used to check and perform reliability test on the Basic Counter Unit. The panel is divided into two sections: XLF (expanded logic functions) and TEST. See "Appendix F" for a detailed description of the XLF and TEST patch panel.

To the right of the test panel is a storage compartment for patch panel wires. Wiring the patch panel is accomplished by connecting selected hub positions with patch panel wires. For this purpose, fifty 4-inch patch panel wires and twenty-five 8-inch patch panel wires are provided with the Basic Counter Unit as standard accessories.

A patch panel image card is provided inside the cover plate to be used by the operator as a reference wiring diagram (Figure 26). Before wiring the patch panel, the user should plan his work on the *IBM Basic Counter Unit Patch Panel Planning Form,* ZX22-6952 (see "Appendix G").

Patch Panel Signal Hubs

On the patch panel are 20 pairs of signal hubs designated SGL 1-20 (Figure 26); each pair supplies a two-way distribution of the same signal from each of 20 connected monitor probes. The signals from the signal hubs provide the basic input to other logic areas of the patch panel by connecting the signal hubs to other logic hubs with patch panel wires.

Patch Panel Signal Definition

Signals on the patch panel are either *true* or *not true* (false) by following the Boolean algebra rules of *true, false* logic.

True is the functionally active state of an event; *not true* is the functionally inactive state of an event.

CPU or I/O Device Signal Definitions

Signals to be measured in a CPU or I/O device exist as either a minus (-) signal level or a plus (+) signal level. That is, the electrical state of a signal in the CPU or I/O device may be negative or positive when active.

Patch Panel Signal Hub Evolution

The evolution of a signal at a signal hub on the patch panels begins when the monitor probe is connected to a pin location (probe point) on the back panel of the equipment being monitored. A probe point location may be minus (-) or plus (+) as specified by the line name in the ALD pages. A monitor probe connected to a minus (-) probe point location detects either a minus (-) signal level or a plus (+) signal level. Similarly, a monitor probe connected to a (+) probe point detects either a minus (-) signal level or a plus (+) signal level. Circuit conventions used within the Basic Counter Unit define a signal to be *true* (active) at the patch panel signal hub when the monitor probe detects a minus (-) signal level at either a minus (-) or plus (+) probe point location. A signal is *not true* (inactive, false) at the patch panel signal hub when the monitor probe detects a plus (+) signal level at either a minus (-) or plus (+) probe point location.

Signal Polarity at Probe Point Location	*Monitor Probe Signal Level Detection*	*Patch Panel Logic at Signal Hub*
minus (-) probe point location	minus (-) signal level	true (active)
	plus (+) signal level	not true (inactive, false)
plus (+) probe point location	minus (-) signal level	true (active)
	plus (+) signal level	not true (inactive, false)

When connecting a monitor probe to a plus (+) probe point location it may be necessary to invert the signal at the signal hub on the patch panel to yield a *true* state. Inversions of a signal at the signal hub is accomplished by connecting the signal hub with a patch panel wire to the input hub of any NOT function on the patch panel.

Logic Sections

Operational patch panel 1 and operational patch panel 2 provide the following logical functions:

Six AND functions
Four OR functions
Eight NOT functions
Four LATCH functions
Two OR LATCH functions
Four FANOUT functions
Eight Self-Generated True Sources

Operational patch panel 1 and operational patch panel 2 also provide additional logical functions that are derivatives from some of the previously named logical functions:

Using the LATCH as a FANOUT
DOT OR functions
Using Inverted Logic

The XLF (expanded logic function) patch panel provides the following logical functions:

One START/STOP function
One 4 x 16 Decoder function

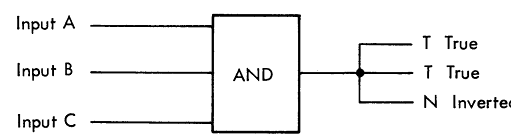
The test patch panel provides 20 additional TRUE functions. Other functions on the test patch panel are for maintenance and test use only and are fully described in "Appendix F."

Connections for the AND Functions

The six AND functions are designated A1, A2, A3, A4, A5, and A6 on the patch panel (Figure 26); each has three inputs numbered horizontally 1-3 under the heading IN. Under the heading OUT, each has three outputs: two are *true* (noninverted) outputs, and the other one (labeled N) is an inverted output.

The AND condition is satisfied when all three input signals are *true* (Figure 10). The *true* outputs are then active, and the inverted output is *not true*. When the AND condition is not satisfied, the output states are the reverse.

When fewer than three conditioning inputs are needed, the unused hubs of the three IN hubs must be connected to a source of a *true* signal; any of the hubs labeled +1 (A, B, C, D) or +1 (E, F, G, H) are used as this source (Figure 11).



A	B	C	T	T	N
1	1	1	1	1	0
1	1	0	0	0	1
1	0	1	0	0	1
1	0	0	0	0	1
0	1	1	0	0	1
0	1	0	0	0	1
0	0	1	0	0	1
0	0	0	0	0	1

Figure 10. AND Function

If All Inputs True → Output True

If Any Input Not True → Output Not True

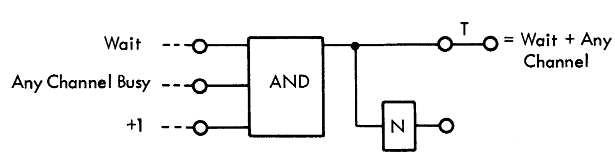


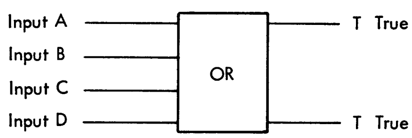
Figure 11. Example of AND Function

Connections for the OR Functions

The four OR functions are designated OR1, OR2, OR3, and OR4 on the patch panel (Figure 26). OR1 and OR3 have three inputs, numbered horizontally 1-3 under the heading

IN. Under the heading OUT, each has two *true* outputs. OR1 and OR3 can serve as either an OR function or as a LATCH function. See "Connections for the OR LATCH Functions."

OR2 and OR4 have four inputs, numbered horizontally 1-4 under the heading IN. Under the heading OUT, each has two *true* outputs. When one or more input signals are *true,* the OR condition is satisfied and the *true* outputs are active. See Figures 12 and 13.



A	B	C	D	T	T
1	1	1	1	1	1
1	1	1	0	1	1
1	1	0	1	1	1
1	1	0	0	1	1
1	0	1	1	1	1
1	0	1	0	1	1
1	0	0	1	1	1
1	0	0	0	1	1
0	1	1	1	1	1
0	1	1	0	1	1
0	1	0	1	1	1
0	1	0	0	1	1
0	0	1	1	1	1
0	0	1	0	1	1
0	0	0	1	1	1
0	0	0	0	0	0

Figure 12. OR Function

Any Input True = Output True

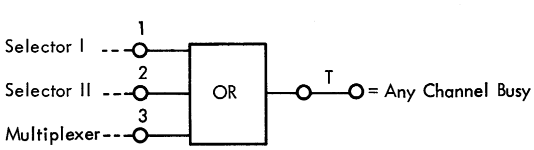


Figure 13. Example of OR Function

Connections for the NOT Functions

The eight NOT functions are designated N1, N2, N3, N4, N5, N6, N7, and N8 on the patch panel (Figure 26). Under IN, each has one input; under OUT, each has two outputs. *True in equals not true out, not true in equals true out.* See Figures 14 and 15.

Input	Output	
1	0	0
0	1	1

Figure 14. NOT Function

True Input = Not True Output

Not True Input = True Output

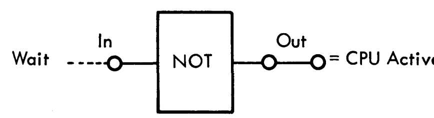


Figure 15. Example of NOT Function

Connections for the LATCH Functions

The four LATCH functions are designated L1, L2, L3, and L4 on the patch panel (Figure 26). Each LATCH has two inputs; one input labeled S (set) and one input labeled R (reset). Each LATCH also has four outputs; two outputs labeled T (*true*) and two outputs labeled N *(not true).* A latch is set during the time interval between two events; for example, seek start and seek complete (Figures 16 and 17). A *true* applied to the S (set) hub produces two *true* outputs. At this time, the LATCH function is set and remains set until a *true* is applied to the R (reset) hub. When a *true* is applied to the reset hub, the LATCH is reset and remains reset until a *true* is applied to the set hub.

Input		Output			
S (Set)	R (Reset)	T (True)		N (Not True)	
1 True	0 Not True	1 True	1 True	0 Not True	0 Not True
0 Not True	1 True	0 Not True	0 Not True	1 True	1 True
0 Not True	0 Not True	0 Not True	0 Not True	1 True	1 True
1 True	1 True	1 True	1 True	0 Not True	0 Not True

Figure 16. LATCH Function

Connections for the OR LATCH Functions

OR1 and OR3 each contain three OR input hubs and one H (hold) hub (Figure 26). OR1 and OR3 serve as OR functions when any of the three OR input hubs are used exclusively. OR1 and OR3 serve as LATCH functions when the H hub is used with any of the three OR input hubs. If a

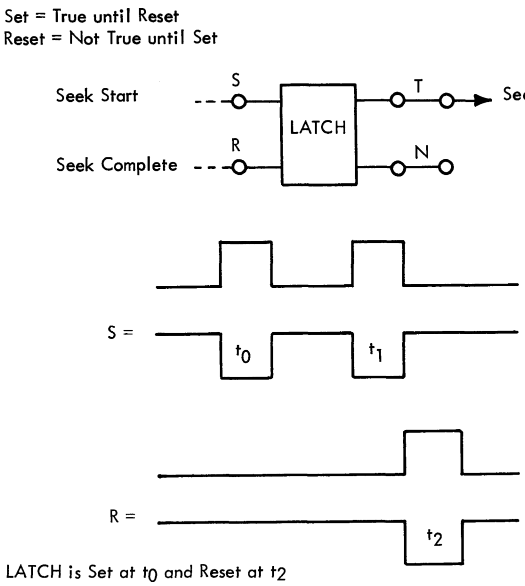


Figure 17. Example of LATCH Function

true is first applied to an H hub and if a *true* is applied to any of the three OR input hubs, a LATCH is set and remains set until reset by a *not true* at the H hub. Think of the H hub as a hold hub, holding a *true* signal; the hold is removed when the signal changes from *true* to *not true* (Figure 18).

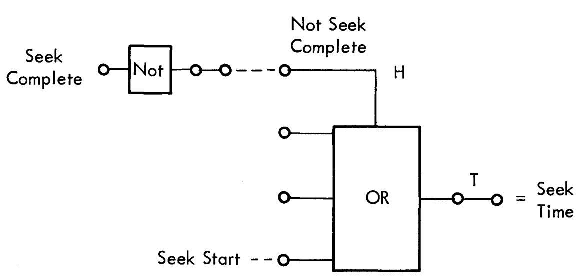


Figure 18. Example of OR LATCH Function

Connections for the FANOUT Functions

The four FANOUT functions are designated F1, F2, F3, and F4 on the patch panel (Figure 26). Each FANOUT has one input labeled IN and two outputs labeled OUT. Think of the FANOUT function as a duplicating function: any *true* input is duplicated twice as *true* output and any *not true* input is duplicated twice as *not true* output (Figure 19).

Self-Generated True Signals

Four sources of self-generated *true* signals are designated +1 (A, B, C, D) on operational patch panel 1, and four sources of self-generated *true* signals are designated +1 (E, F, G, H) on operational patch panel 2 (Figure 26). These eight

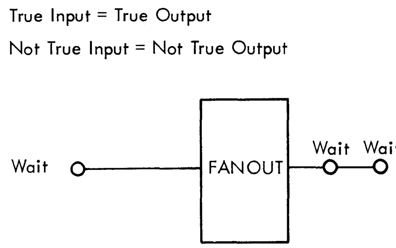


Figure 19. Example of FANOUT Function

sources of self-generated *true* signals are available to satisfy the input requirement of any logical function on the patch panel when a *true* input is required. For example, if another *true* input is needed to satisfy an *AND* function, any of the hubs labeled +1 (A, B, C, D) or +1 (E, F, G, H) may be used as this source.

Do not confuse +1 (A, B, C, D) or +1 (E, F, G, H) with plus (+) signal levels in a CPU or I/O device. See "Patch Panel Signal Definition."

Using the LATCH as a FANOUT

If additional FANOUTS are required, a LATCH function can serve as a FANOUT function. If both the set and reset hubs of a LATCH are *true*, set overrides reset.

If a wait is the input to the set hub and a plus-one (+1) is the input to the reset hub (Figure 20), the *true* output is active when the wait input is active. The *not true* outputs are inactive because wait active in the set hub overrides the plus-one (+1) in the reset hub. When the wait input becomes inactive, the plus-one (+1) input in the reset hub causes the *not true* hub to become active (equal to not-wait).

Note: To use a LATCH in this manner, the Basic Counter Unit must have an EC258994 installed.

DOT OR Function

The logic on the patch panel may be expanded by using the rules of logic to obtain functions from other functions on the patch panel. The DOT OR function is created from two AND functions (Figure 21).

Using Inverted Logic

An AND function can serve as an OR function by inverting the inputs to an AND function through a NOT function

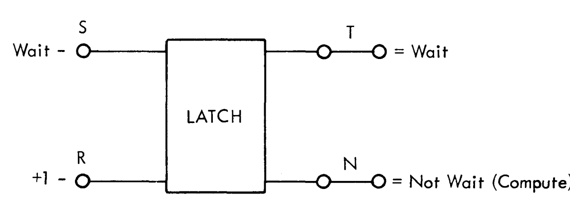


Figure 20. Example of LATCH used as a FANOUT Function

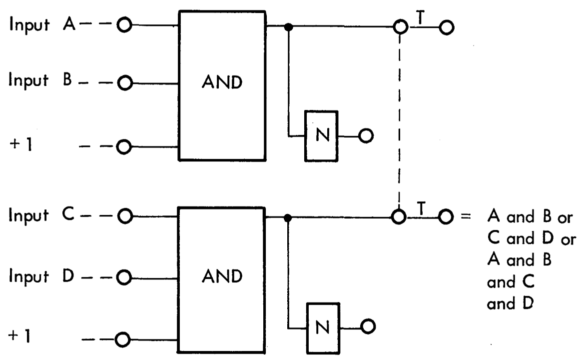


Figure 21. Example of DOT OR Function

and by using the *not true* output from the AND function as being logically true (Figure 22).

Also, an OR function can serve as an AND function by inverting the inputs to an OR function through a NOT function and by inverting the output from an OR function through a NOT function.

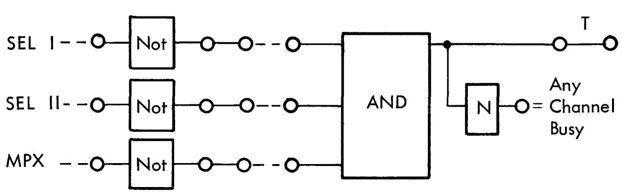


Figure 22. Using Inverted Logic

START/STOP Function

The START and STOP hubs are on the XLF patch panel (Figure 26).

The START hub, when activated, starts the Basic Counter Unit counters from an external source. The source may be an input pulse or patch panel logic. A *true* signal activates the START function and turns on the count-enable light. The START hub is interlocked with PUNCH GO to prevent data skew while punching out counter contents. If a *true* is wired to the START hub, the STOP pushbutton becomes inoperative.

The STOP hub, when activated, stops the Basic Counter Unit counters from an external source. The source may be an input pulse or patch panel logic. A *true* signal activates the STOP function and turns off the count-enable light. If a *true* is wired to the STOP hub, the START pushbutton becomes inoperative.

4 x 16 Decoder

A 4 x 16 decoder, on the XLF patch panel, is provided to decode up to any combination of four *true* binary inputs into one of 16 *true* hexadecimal outputs (Figure 26).

The 4 x 16 decoder (Figure 23) is designated on the XLF patch panel as:

DCDR IN 8, 4, 2, 1 (four positions)
STROBE (one position)
DCDR OUT 0, 1, 2, 3, 4, 5, 6, 7, 8, 9,
A, B, C, D, E, F (16 positions)

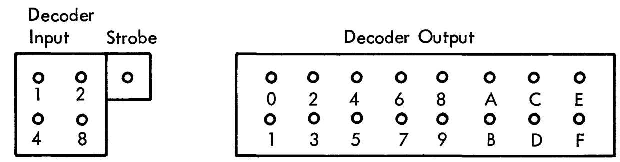


Figure 23. 4 x 16 Decoder

DCDR IN, four hub positions, is wired from a *true* or *not true* source from any of the logical functions on the patch panel. A *true* wired to DCDR IN 8, 4, 2, or 1 hub defines the presence of a particular bit; a *not true* wired to DCDR IN 8, 4, 2, or 1 hub defines the absence of a particular bit. If DCDR IN 8, 4, 2, or 1 hub is not wired, it is treated by the decoder as *not true*.

The STROBE, one hub position, provides a pulse that controls the decoder's output. The STROBE must be wired from a *true* signal source. Any combination of four *true* inputs to DCDR IN plus a *true* input to STROBE produces a true decoder output.

DCDR OUT, 16 hub positions, provides the decoder output functions. Each position is designated by the hexadecimal value 0-F. Only one of the DCDR OUT hubs may be *true* at any one time. The decoder output remains *true* for the duration of the strobe *true* pulse.

If DCDR IN hubs 2 and 1 are wired from *true* sources and if the pulse to the STROBE hub is wired from a *true* source, DCDR OUT hub 3 (and only hub 3) is *true* (active). See Figure 24.

The decoder can be used to simplify the wiring on the patch panel to measure CPU active time and CPU wait time and to apportion these timings to I/O channels.

The four signal sources and inputs to DCDR IN are:

Signal Sources	*DCDR IN*
Selector Channel 2	8
Selector Channel 1	4
Multiplexer Channel	2
Wait	1

True is wired to STROBE
Manual is wired to STOP
Not Manual is wired to START

The decoder provides all possible combinations of CPU, wait, channel, and CPU/channel overlap. The Karnaugh map (Figure 25) illustrates the available combinations of CPU, wait, and channel(s) for a three-channel system. The desired DCDR OUT hubs may be wired to counter timing or counting hubs depending on the user's specific application.

Strobe

Pulse to Strobe = True

DCDR IN | DCDR OUT (10)(11)(12)(13)(14)(15)

8	4	2	1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
				T															
			T		T														
		T				T													
		T	T				T												
	T							T											
	T		T						T										
	T	T								T									
	T	T	T								T								
T												T							
T			T										T						
T		T												T					
T		T	T												T				
T	T															T			
T	T		T														T		
T	T	T																T	
T	T	T	T																T

Figure 24. Possible Decoder Input and Output Values

Decoder Input
1 Wait
2 Mpx
4 Channel 1
8 Channel 2
Strobe -- True

Decoder Out Hub "1"
Wired to Ctr "1" Hub

	Wait		CPU		
Mpx Operating	(15) F	(11) B	(14) E	(10) A	Chan 2
Mpx Operating	7	3	6	2	Not Chan 2
Mpx not Operating	(13) D	9	(12) C	8	Chan 2
Mpx not Operating	5	1	4	0	Not Chan 2
	Chan 1	Not Chan 1	Chan 1	Not Chan 1	

Decoder Out

Figure 25. Karnaugh Map Showing Use of 4 x 16 Decoder

Additional Self-Generated True Signals

Twenty hubs, designated ACVT BUS, on the test patch panel may be used as a source of self-generated *true* signals when the supply of +1 (A, B, C, D) and +1 (E, F, G, H) hubs has been exhausted (Figure 26). The use of ACVT BUS hubs as maintenance functions is described in "Appendix F."

Counters Section

Two counter sections are on the patch panel (Figure 26). One counter section is to the far right of operational control panel 1 and is associated with counters 0-7. The other counter section is to the far right of operational control panel 2 and is associated with counters 8-15. For each counter, two hubs are available for input connection: the CNT hub for counting; the TMG hub for timing.

A counter is activated to count or time when an active signal is wired to the respective CNT or TMG hub.

Counting Rate: A maximum of 1 MHz on all counters. Increments once for each occurrence of an event up to a maximum of one million events per second.

Timing Rate: Records the duration of an event(s) at a rate of 1 MHz with a 1-microsecond resolution. With counters counting at a 1-MHz timing rate, the counter overflows in 27.8 hours.

Counter Accuracy: A slight arithmetic error may occur in the low-order positions of the Decimal Digit Display while measuring a system function. This slight arithmetic error is caused by signal delays through the logic blocks. For example, total elapsed time should equal total compute plus total wait. However, if both total compute and total wait are monitored, the sum of the two will not, in many instances, equal total elapsed time (to eleven digits precision) although both values are derived from the same signal source, the wait latch. The necessity of routing total wait through a NOT function (not total wait=total compute) causes a slight delay. The delay may cause a discrepancy and in some measurements may not occur at all. (This slight discrepancy is mathematically referred to as lack of closure.) The nominal delay time for each logic function is given in Appendixes D and E. Each nominal delay time is listed in nanoseconds (ns) beside each OUT hub under the heading "Hub Title."

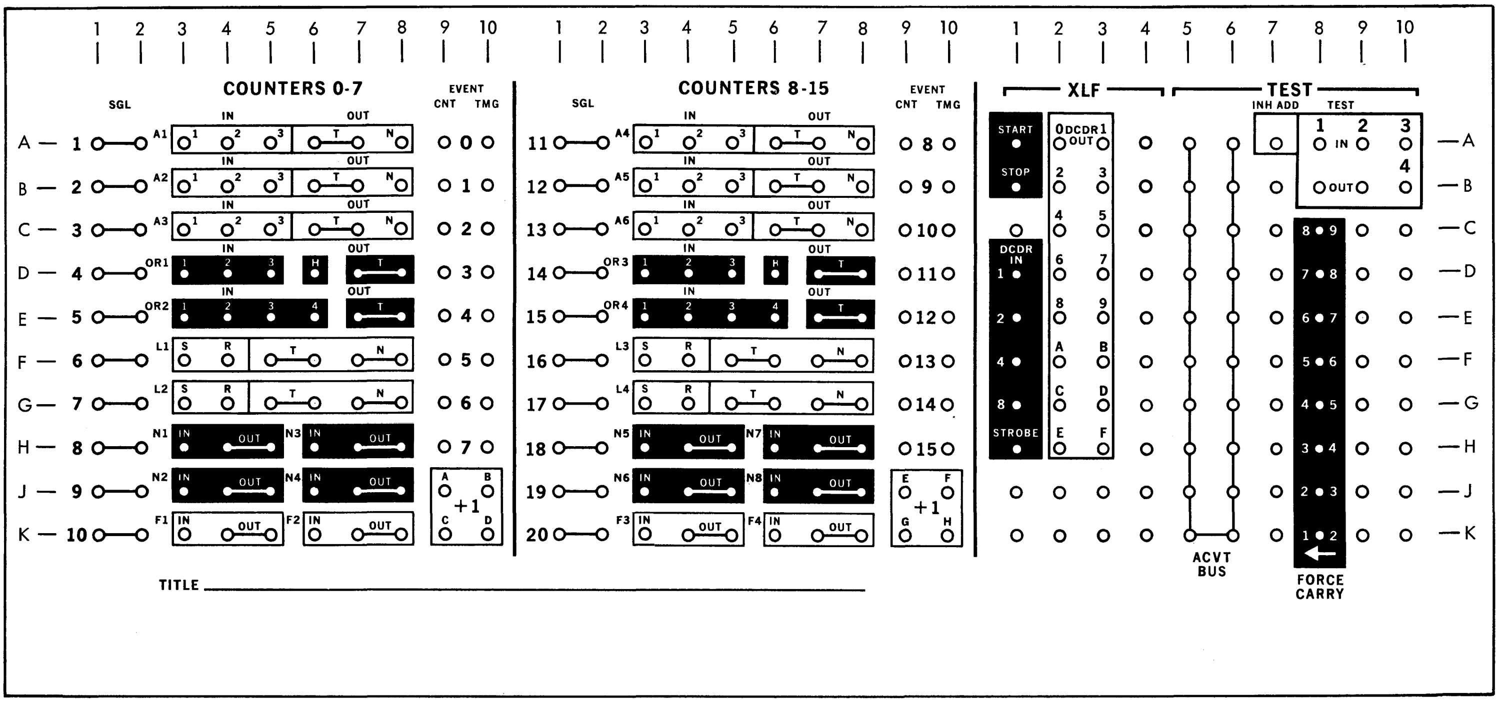


Figure 26. Patch Panel Image Card

Optional Accessory – IBM 1057/1058 Card Punch

This section briefly describes the 1057/1058 Card Punch; for further details see *IBM 1050 Data Communication System, Principles of Operation,* GA24-3474 and *IBM 1050 Operator's Guide,* GA24-3125.

The IBM 1057/1058 (minimum EC level must be 206345) records the contents of the 16 counters in the Basic Counter Unit on four punched cards that are used as permanent records for future study and analysis.

OPERATING PROCEDURES

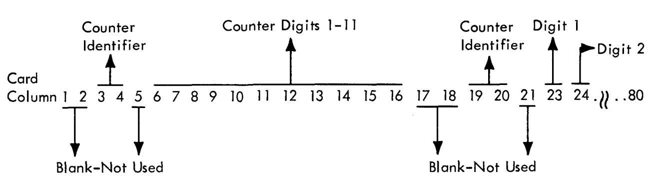
To start a punch operation on the 1057/1058, follow the housekeeping procedures for the Basic Counter Unit and the 1057/1058 and refer to the punch operation procedures illustrated in Figure 27.

IBM Basic Counter Unit Housekeeping Procedures
- Basic Counter Unit and 1057/1058 are connected
- Power is on
- Probes are connected
- Patch panel is wired
- Count-enable light is on
- Basic Counter Unit is monitoring

IBM 1057/1058 Housekeeping Procedures
- Install program card
- Place program card starwheels in read position
- Load card hopper
- Card stacker must not be full
- Position card in both read and punch station
- Switch card punch from KEY to AUTO

PUNCH CARD FORMAT

The contents of four counters are punched on one card. Because 16 counters are used in the Basic Counter Unit, a total of four cards are required to record the contents of the 16 counters (Figure 28). All cards are formatted in an identical manner. (Only 64 columns are used on each card.) Considering one card only, 16 columns are required to reflect the contents of one counter. The punching format is as follows:



Counter identifier digits (2 positions) reflect the counter number (00-15) recorded. The following column position is not used and digit data is then punched in the next 11 columns. Formatting of the other three counters in the same card is effected in the same manner.

PUNCH PROGRAM CARD

The program card used in the 1057/1058 Card Punch permits the execution of particular control functions, such as space advance, auto dup, end-of-card detect, etc. These control functions are dependent on the punched format of the program card. An example of a typical punched program card is shown in Figure 29. A punch in a column and row location is indicated by a rectangular bar, a non-punched position is denoted by the absence of the bar. The function of each punch position is:

Punch	*Function*
Row 1	Allows alpha shift, which permits Basic Counter Unit punch controls to punch a blank, thus performing a column space function.
Row 2	Punch preceding zero's in a counter value. For example, if a counter value is equal to 00000670019, the zero values preceding the numeral 6 are punched under control of the program card.
Row 12	Determines field definition. A single field, columns 2-64, required for Basic Counter Unit operations.
Column 64, Row 8	Activates control line to indicate that the next column operation is an internal 1057/1058 function.
Column 65, Row 0	Initiates punching in auto dup mode.
Columns 66-80, Row 12	Defines auto dup field to punch date, job identity, etc., predetermined by preceding card.
Column 80, Row 8	Control line to signify end of card.

POWER SUPPLY

Interface power is supplied to the 1057/1058 by the Basic Counter Unit through a standard cable that connects both units. The standard cable is furnished by the 1057/1058. Power must be off in the Basic Counter Unit and the 1057/1058 prior to connecting or disconnecting the standard cable.

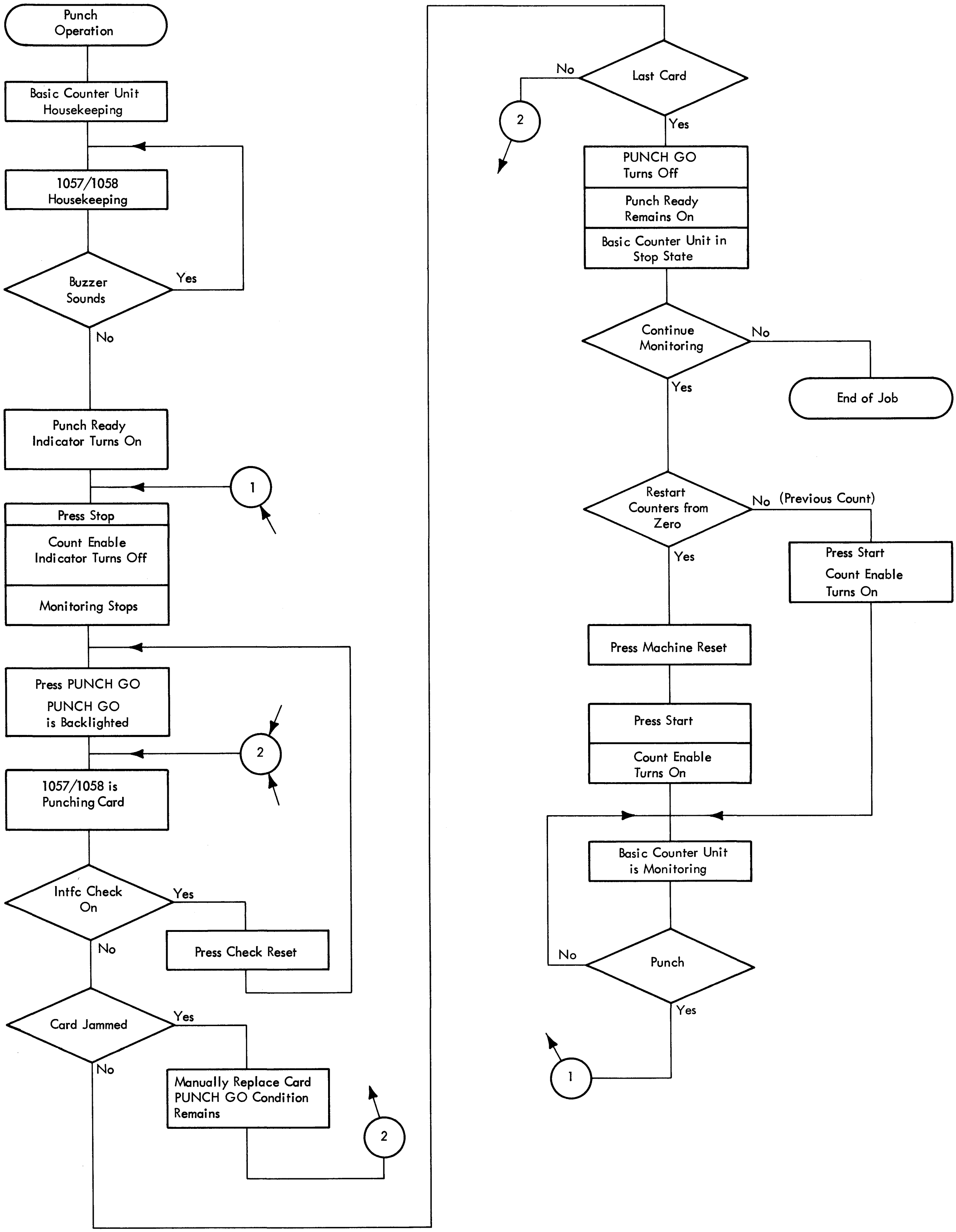


Figure 27. IBM 1057/1058 Card Punch Operating Procedures

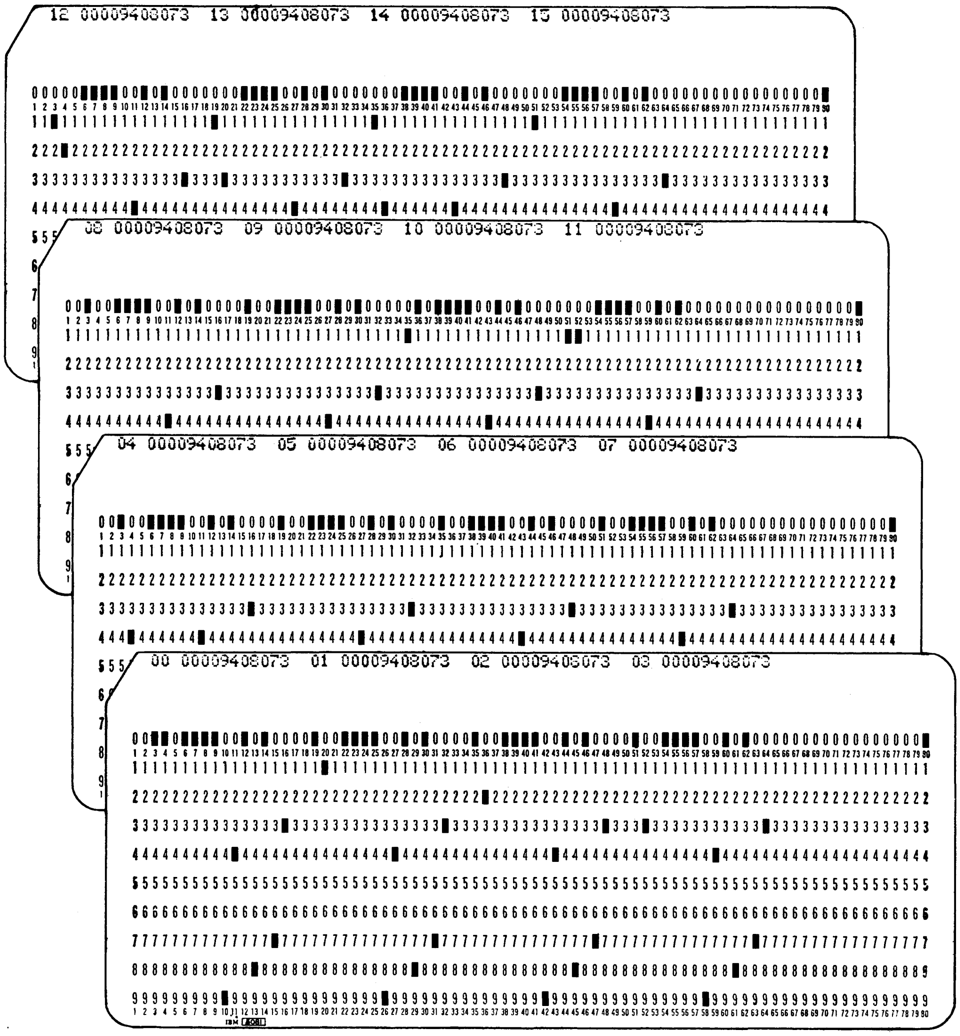


Figure 28. Punched Card Output

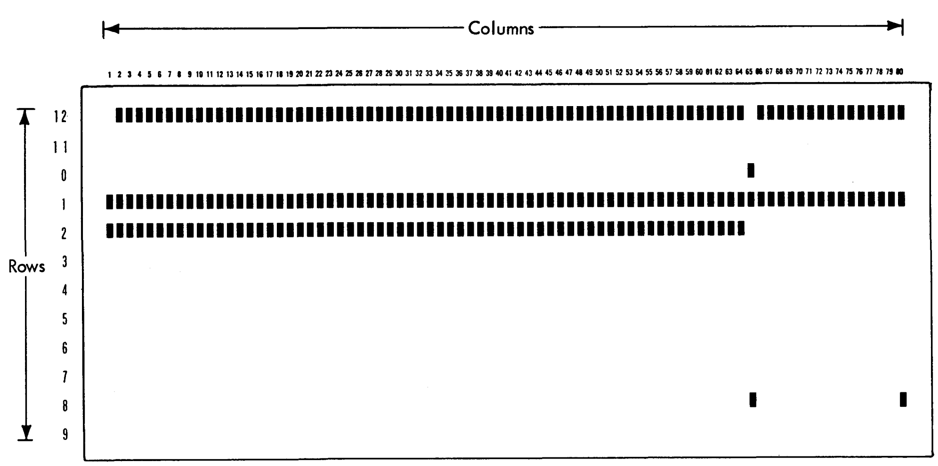


Figure 29. Example of Program Card

Testing Procedures

This section contains testing procedures for the IBM Basic Counter Unit and the IBM 1057/1058 Card Punch.

BASIC COUNTER UNIT TESTING PROCEDURES

Testing procedures for the Basic Counter Unit consist of:
- Installation Tests
- Performance Tests
- Operational Control Patch Panel Test
- Lamp Test

Installation Tests

After the Basic Counter Unit has been placed in position and before it is attached to a unit to be monitored, perform the following tests to ensure that the unit is functioning correctly.

Ones Retention Test

1. Activate the following hubs: TEST 2, FORCE CARRY 9-8, 8-7, 7-6, 6-5, 5-4, 4-3, 3-2, and 2-1.
2. Press MACHINE RESET.
3. Press START nine times. Visual display should read 99.999.999.900 for all 16 counters.
4. Activate INH ADD and move wire from TEST 2 to TEST 1.
5. Press START; allow the Basic Counter Unit to run for 30 minutes.
6. Press STOP; check the visual display for a reading of 99.999.999.9xx on all 16 counters. (The value xx is indeterminate but should be equal for all 16 counters.)

Zeros Retention Test

1. Activate TEST 1 and INH ADD hubs.
2. Press MACHINE RESET and START; allow the Basic Counter Unit to run for 30 minutes.
3. Stop the Basic Counter Unit; check visual display for 00.000.000.0xx in all counters. (The value xx is indeterminate but should be equal for all 16 counters.)

High Speed Count 1 Test

1. Activate TEST 1 and FORCE CARRY 6-5 hubs.
2. Press MACHINE RESET.
3. Press START; allow the Basic Counter Unit to run for 30 minutes.
4. Press STOP; note that digits 2, 3, 4, 5, and 6, 7, 8, 9 are equal.
5. Check that all 16 counters are equal.

High Speed Count 2 Test

1. Activate TEST 1 and FORCE CARRY 5-4 hubs.
2. Press MACHINE RESET.
3. Press START; allow the Basic Counter Unit to run for 15 minutes.
4. Press STOP; note that digits 1, 2, 3, 4, and 6, 7, 8, 9 are equal.
5. Check that all 16 counters are equal.

Performance Tests

Broadside Count to All Counters

This test checks that all counters run automatically at a rate of 1 MHz.

1. Connect patch wire from TEST 1 hub on the operational control maintenance panel to one of the ACVT BUS hubs.
2. Press POWER ON, MACHINE RESET and START.
3. Allow the Basic Counter Unit to operate for 2 minutes; then press STOP.
4. Rotate the counter select switch; note that all counters contain the same value.
5. Press MACHINE RESET.
6. Rotate the counter select switch; note that all counters equal zero.

Force Carry to All Counters

1. Connect patch wires from FORCE CARRY hubs 7-6 and 4-3 and TEST 1 hub to ACVT BUS hubs.
2. Press MACHINE RESET, then START; allow counters to run for 2 minutes.
3. Press STOP; check that all counters contain the same value.

Force Carry to All Counters by Single Stepping

This test is similar to the preceding test except that the counters are stepped manually each time START is pressed. Because the change in the displayed counter value may be easily seen, this test also checks that the digital display lamps are functioning.

1. Connect patch wires from all eight FORCE CARRY hubs to ACVT BUS positions.
2. Connect patch wires from TEST 2 hub to an ACVT BUS hub.
3. Press MACHINE RESET, then START.
4. Rotate the counter select switch; note that all counters contain the same value.

5. Single step the counters by repeatedly pressing START. Check that all counters contain the same value after each impression.

Operational Patch Panel Test

The logical functions available at the operational patch panels may be checked by using the plus one (+1) hubs, the TEST 1 OUT and TEST 2 OUT hubs on the test patch panel, and any available counter.

Lamp Test

1. Press POWER ON, MACHINE RESET and LAMP TEST.
2. Refer to Figure 30 and rotate the counter select switch through each position. Note that the lamps displayed correspond with those specified in the figure.

Counter Select Switch	Display Position 0*	Display Position 1-10	Display Position 11
0	0	0,1	0
1	1	1,0	1 & 0
2	2	2,5,0	2 & 0
3	3	3,4,0	3 & 0
4	4	4,3,0	4 & 0
5	5	5,2,0	5 & 0
6	6	6,9,0	6 & 0
7	7	7,8,0	7 & 0
8	8	8,7,0	8 & 0
9	9	9,6,0	9 & 0
10	10	0	0
11	11	0	0
12	12	0	0
13	13	0	0
14	14	0	0
15	15	0	0

* Displayed with red background

Figure 30. Lamp Test Data

1057/1058 TESTING PROCEDURES

Testing procedures for the 1057/1058 consist of:

Punch Test 1

Punch Test 2

These tests are performed with the punch connected. Under manual control, the contents of the 16 counters are punched into a set of four cards. The 16 counters are identified as 0-15.

A program card must be installed in the card punch. The card must allow the punch interface to control 64 columns of the card. In auto dup mode, the card controls the remaining 16 columns. These 16 columns can be used for job identity, dates, etc., at the discretion of the operator. The program card must be formatted to punch four counter values in 16 character groups.

If a data error occurs during punching, the affected byte is punched as two negative zoned digits. If the program card is improperly punched, a control check occurs. In either case, the interface check indicator is activated on the Basic Counter Unit console.

Note: The punch controls are interlocked with the start and stop pushbuttons on the Basic Counter Unit. Punch go will not activate a punch cycle unless the Basic Counter Unit has been stopped. Start is disabled as long as the punch go latch is active. This interlock will prevent the possibility of data skew during the punch cycle.

Punch Test 1

1. Attach 1058 punch and activate the following hubs: TEST 2, FORCE CARRY 9-8, 8-7, 7-6, 6-5, 5-4, 4-3, 3-2, and 2-1.
2. Press MACHINE RESET.
3. Press PUNCH GO.
4. After punch go light turns off, check the cards for all zeros in the data fields and also check for proper format. The intfc check light must be off.
5. Press START.
6. Press PUNCH GO.
7. After punch go light turns off, check that the cards are equal to the value in the counters.
8. Return to step 5 and continue to check all cards punched through a value of 99.999.999.900.

Punch Test 2

1. Activate the TEST 1 hub.
2. Press MACHINE RESET and START.
3. Allow the Basic Counter Unit to run for approximately 2 minutes, then press STOP and PUNCH GO.
4. Check cards against values in the counters.
5. Remove all wires from test panel and establish different values in all counters by pressing START and wiring each counter's timing hub to a +1 signal for random amounts of time (it is not necessary to exceed 15 seconds for any counter).
6. Press STOP and PUNCH GO.
7. Check cards against values in all counters.

Measuring Techniques

TERMINOLOGY

System functions, measured or derived, are referred to throughout this manual, especially in the examples on measurement techniques. Measured system functions are measured directly by the counters in the Basic Counter Unit. Derived system functions are derived from previously measured system functions by using mathematical formulas. Derived system functions can also be measured directly by the counters in the Basic Counter Unit; however, to achieve maximum efficiency of the Basic Counter Unit, measuring system functions that can be derived should be kept at a minimum.

Measured System Functions

Total Elapsed Time is measured by monitoring the time that a system is not in the stopped state. The stopped state is indicated by the manual light and caused by pressing STOP or SYSTEM RESET on the system control panel. *Total elapsed time* provides a base of reference against which other comparisons can be computed.

Total Compute is the signal present when bit number 14 of the program status word (PSW) is off, indicating that the processor is executing instructions.

Processor Not Active (Wait State) is the signal present when bit number 14 of the PSW is on, indicating that the processor is not executing instructions.

Channel Busy is a signal made available to the Basic Counter Unit, once for the multiplexer channel, and once for each selector channel on the system.

Any Channel Busy is created by using the combinatorial logic on the Basic Counter Unit patch panel. It is the logical OR of any *channel busy*.

Wait and Any Channel Busy is created by using the combinatorial logic on the Basic Counter Unit patch panel. It is the logical OR of *any channel busy*, and the resultant output of the OR ANDed with *processor not active*.

Channel Overlap is a measurement of the time the input/output channels are operating simultaneously. The logical AND of selector channel-one busy and selector-two busy provides this measurement.

Derived System Functions

Total Wait is the *total elapsed time* minus *total compute*.

Wait Only (System Idle) is the *total wait* minus *wait and any channel busy*.

Compute and Any Channel Overlap is *any channel busy* minus *wait and any channel busy*.

Compute Only is the *total compute* minus *compute and any channel overlap*.

EXAMPLES

The user must decide on and develop his own techniques and define his own system functions, but certain examples may prove helpful to him in formulating plans. Several examples are presented in this section that illustrate basic measurement techniques. The numbers shown in the examples are for illustration only and are not to be considered as standard cases.

Each example given consists of three parts:

Objectives
Patch Panel Wiring Diagram
Summary

Example 1

During the processing of a job or jobs on System/360, the CPU either overlaps or non-overlaps the I/O channels. Overlap and non-overlap are interrelated and influence the efficiency of a system. Overlap exists when one or more I/O channels perform I/O operations while the CPU simultaneously executes instructions. Non-overlap exists when I/O channels perform I/O operations at one time and the CPU executes instructions at another time.

Objectives

Measure *total elapsed time, any channel busy, compute and any channel overlap* and *total compute.* Derive *compute only, total wait, wait and any channel busy,* and *wait only.*

Wiring

The wiring for this example is shown in Figure 31.

The stop state on a System/360 (indicated by a manual light and caused by pressing STOP or SYSTEM RESET on the system control panel) is being monitored. One stop state signal is wired to the STOP hub, another stop state signal is wired as input to a NOT function, the NOT function output is then wired to the START hub and causes total counter stoppage if either STOP or SYSTEM RESET on the system control panel is pressed.

Any +1 hub is wired to a TMG hub and results in *total elapsed time.*

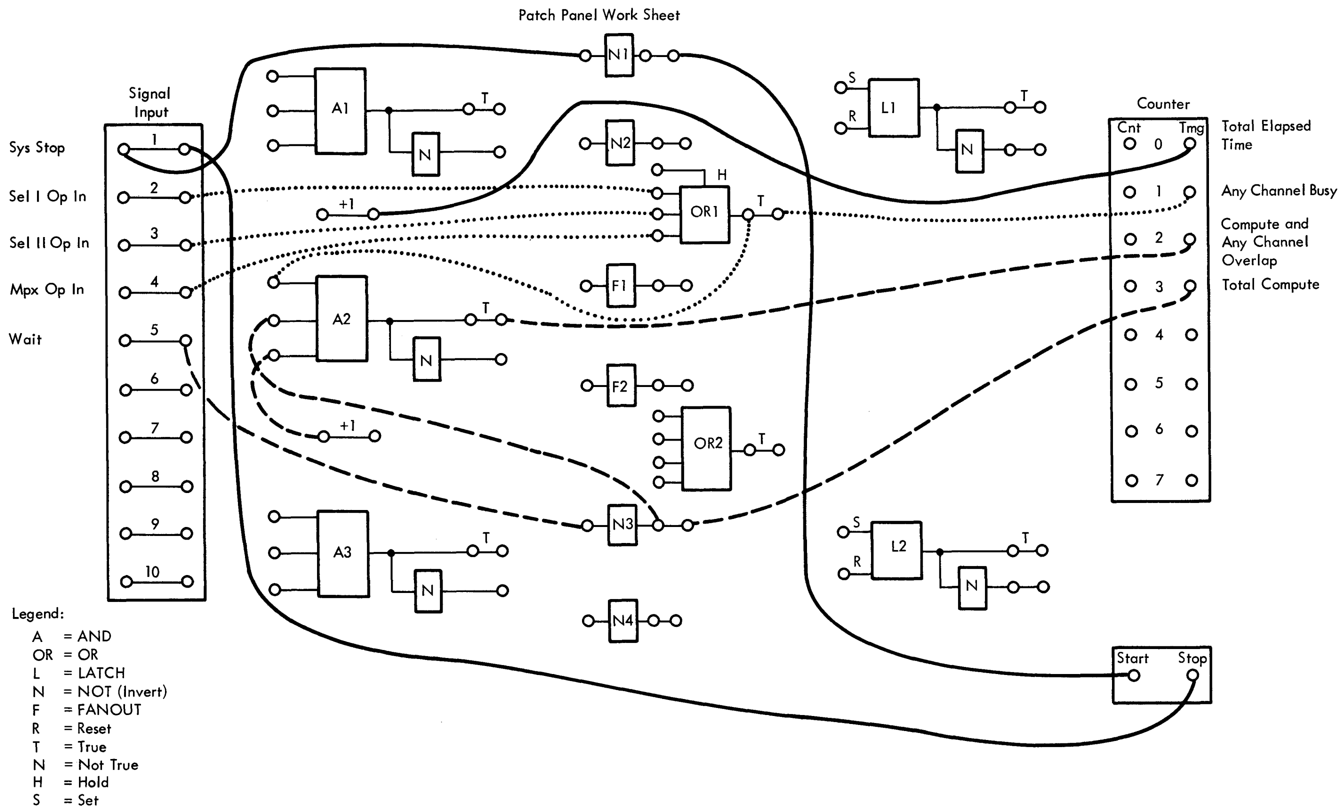


Figure 31. Wiring for Example 1

The signals from selector channel 1, selector channel 2, and the multiplexer channel are wired as inputs to the OR function. One OR output is wired to a TMG hub and results in *any channel busy*. Another OR output is wired as input to an AND function.

The wait signal is wired as input to a NOT function. One NOT output is wired to a TMG hub and results in *total compute*.

Another NOT output is wired as another input to the AND function. The AND output is wired to a TMG hub and results in *compute and any channel overlap*.

Summary

The counter results are:

Counter 0:	154,011,000	Total elapsed time
Counter 1:	32,417,300	Any channel busy
Counter 2:	19,450,100	Compute and any channel overlap
Counter 3:	81,800,500	Total compute

At the timing rate of 1 MHz (1 microsecond) provided by the Basic Counter Unit, the readings can be converted to:

Counter 0:	154.0 seconds	Total elapsed time
Counter 1:	32.4 seconds	Any channel busy
Counter 2:	19.5 seconds	Compute and any channel overlap
Counter 3:	81.8 seconds	Total compute

Additional functions were derived from the counter results by use of formulas:

Compute only = (Total compute) – (Compute and any channel overlap)
= (Counter 3) – (Counter 2)
= (81.8 seconds) – (19.5 seconds)
= 62.3 seconds

Total wait = (Total elapsed time) – (Total compute)
= (Counter 0) – (Counter 3)
= (154 seconds) – (81.8 seconds)
= 72.2 seconds

Wait and any channel busy = (Any channel busy) – (Compute and any channel overlap)
= (Counter 1) – (Counter 2)
= (32.4 seconds) – (19.5 seconds)
= 12.9 seconds

Wait only = (Total wait) – (Wait and any channel busy)
= (72.2 seconds) – (12.9 seconds)
= 59.3 seconds

The measured and derived functions can also be expressed in percentages:

Compute only:	62.3 seconds	40.5%
Compute and any channel overlap:	19.5 seconds	12.6%
Wait and any channel busy:	12.9 seconds	8.4%
Wait only:	59.3 seconds	38.5%
Total elapsed time:	154.0 seconds	100.0%

Each function should be pictured as a series of many short events. For example, the compute time is a series of short compute times, separated by short wait times. Each compute time is then followed by a short channel time, sometimes partially overlapped with the compute time. Figure 32 gives the relationship between the total-compute and total-channel times, which is a valid way of measuring systems performance. The numeric values shown in this example are for illustration only and are not to be interpreted as standard cases.

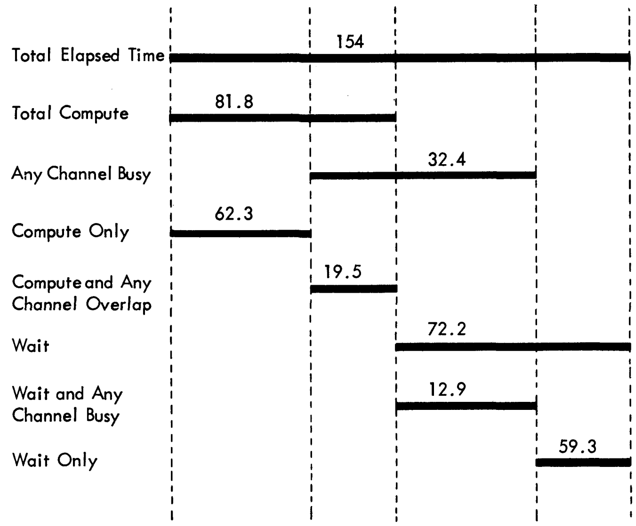


Figure 32. Summary Profile for Example 1

Example 2

IBM System/360 has one or more selector channels and a multiplexer channel. These channels can operate at different times or channel operations can overlap each other. Channels overlapping each other can also overlap the operation of the central processing unit.

Objectives

To measure *total elapsed time, total compute, any channel busy, selector channel 1 busy, selector channel 2 busy, multiplexer channel busy,* and *selector channel 1/selector channel 2 overlap.*

Wiring

The wiring for this example is shown in Figure 33.

Summary

The counter results are:

Counter 0:	25,368,941,208	Total elapsed time
Counter 1:	14,297,542,167	Total compute
Counter 2:	7,254,382,997	Selector channel 1 busy
Counter 3:	2,101,837,595	Selector channel 2 busy
Counter 4:	981,021,355	Multiplexer channel busy
Counter 5:	9,962,951,012	Any channel busy
Counter 6:	505,942,833	Selector channel 1/selector channel 2 overlap

At the timing rate of 1 MHz (1 microsecond) provided by the Basic Counter Unit, the readings can be converted to:

Counter 0:	25,369 seconds	Total elapsed time
Counter 1:	14,298 seconds	Total compute
Counter 2:	7,254 seconds	Selector channel 1 busy
Counter 3:	2,102 seconds	Selector channel 2 busy
Counter 4:	981 seconds	Multiplexer channel busy
Counter 5:	9,963 seconds	Any channel busy
Counter 6:	506 seconds	Selector channel 1/selector channel 2 overlap

The measured functions can also be expressed in percentages:

Total elapsed time	25,369 seconds	100.0%
Total compute	14,298 seconds	56.3%
Selector channel 1 busy	7,254 seconds	28.5%
Selector channel 2 busy	2,102 seconds	7.9%
Multiplexer channel busy	981 seconds	3.8%
Any channel busy	9,963 seconds	39.2%
Selector channel 1/selector channel 2 overlap	506 seconds	1.9%

Example 3

As many as 15 programs may reside in a system simultaneously and share the same processor by using the multiprogramming facilities of System/360 Operating System on an IBM System/360 Model 65. Actually, each program resides in a separately protected memory partition and shares the processor at different time intervals.

Objectives

To measure the *total compute time* and the amount of compute time used by each of three protected memory partitions and the amount of compute time used by the system's supervisory program.

Wiring

The wiring for this example is shown in Figure 34.

Summary

The counter results are:

Counter 8:	9,925,541,174	Total compute
Counter 9:	1,432,154,273	Supervisor
Counter 10:	2,418,010,710	Partition 1
Counter 11:	2,943,892,715	Partition 2
Counter 12:	3,131,483,476	Partition 3

Additional functions may be derived by using the formulas in Example 1. The numeric values shown in this example are for illustration only and are not to be interpreted as standard cases.

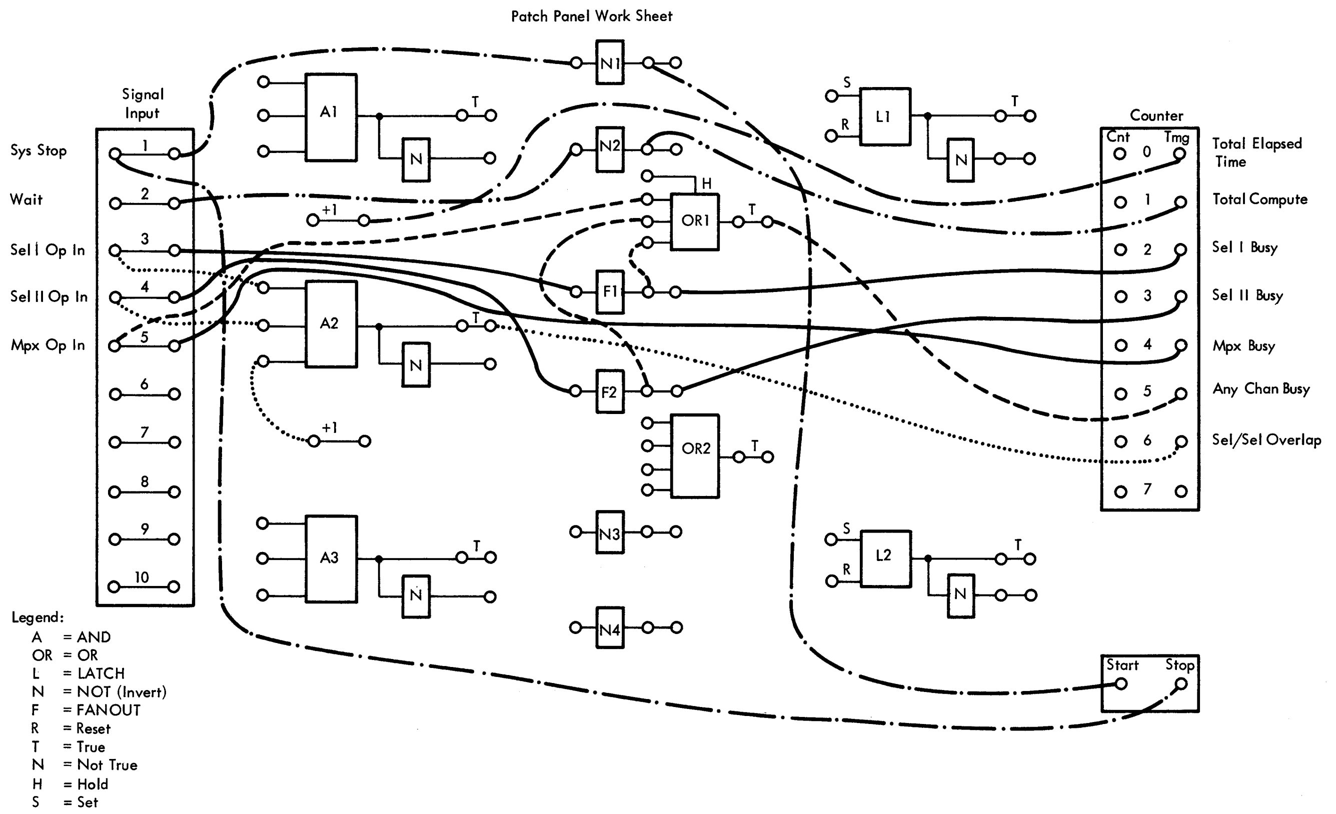


Figure 33. Wiring for Example 2

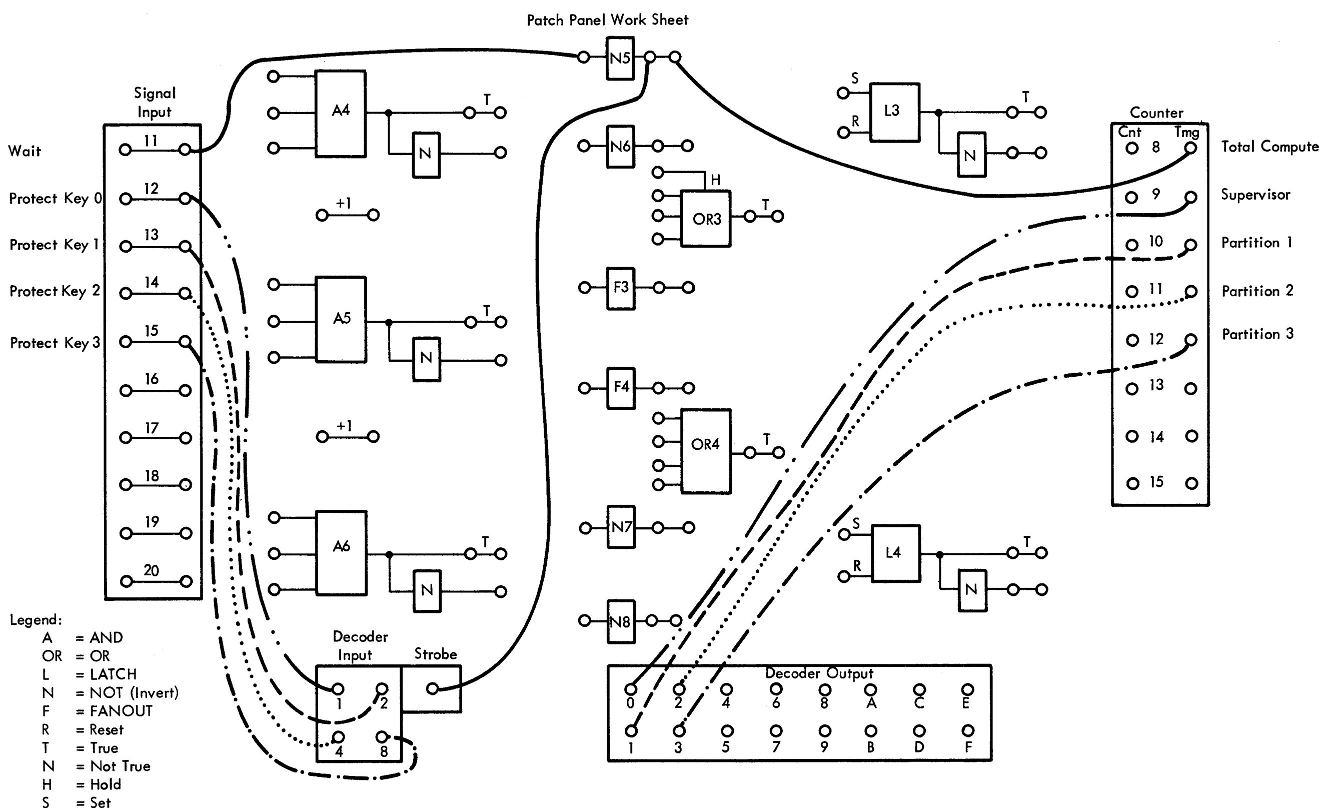


Figure 34. Wiring for Example 3

At the timing rate of 1 MHz (1 microsecond) provided by the Basic Counter Unit, the readings can be converted to:

Counter 8:	9,926 seconds	Total compute
Counter 9:	1,432 seconds	Supervisor
Counter 10:	2,418 seconds	Partition 1
Counter 11:	2,944 seconds	Partition 2
Counter 12:	3,132 seconds	Partition 3

The measured function can also be expressed in percentages:

Total compute	9,926 seconds	100.00%
Supervisor	1,432 seconds	14.34%
Partition 1	2,418 seconds	24.19%
Partition 2	2,944 seconds	29.45%
Partition 3	3,132 seconds	31.32%

Additional functions may be derived by using the formulas in Example 1. The numeric values shown in this example are for illustration only and are not to be interpreted as standard cases.

Example 4

The IBM 2314 Direct Storage Facility Model A1 or 1 contains eight separate modules. In a case study, the IBM System/360 Operating System for an IBM System/360 Model 50 was resident on two 2314 modules.

Objective

Measure the percentage of time that the two system residence modules of the 2314 are used and the percentage of time that the CPU is waiting for the system residence modules. For comparative purposes, measurements are made of the following other functions: *total wait, any channel busy, selector channel 1 time* (2314 residence), and *total elapsed time.*

Wiring

The wiring for this example is shown in Figure 35.

Summary

The counter results are as follows:

Counter 8:	395,044,983	Total elapsed time
Counter 9:	161,597,391	Total wait
Counter 10:	92,214,125	Total any channel
Counter 11:	47,014,497	Total system residence
Counter 12:	41,501,691	System residence and wait
Counter 13:	73,941,095	Selector channel 1 busy

At a timing rate of 1 MHz (1 microsecond) provided by the Basic Counter Unit, the readings can be converted to:

Counter 8:	395.0 seconds	Total elapsed time
Counter 9:	161.6 seconds	Total wait
Counter 10:	92.2 seconds	Total any channel
Counter 11:	47.0 seconds	Total system residence
Counter 12:	41.5 seconds	System residence and wait
Counter 13:	73.9 seconds	Selector channel 1 busy

The measured system function can also be expressed in percentages:

Total elapsed time	395.0 seconds	100.0%
Total wait	161.6 seconds	40.8%
Total any channel	92.2 seconds	23.3%
Total system residence	47.0 seconds	11.9%
System residence and wait	41.5 seconds	10.5%
Selector channel 1 busy	73.9 seconds	18.7%

Because this example measures only a portion of the total operation (channel time), the individual times do not add up to the total elapsed time. Other desired functions, such as *compute only,* must be calculated by using the formulas in Example 1. The numeric values shown in the examples are for illustration only and are not to be interpreted as standard cases.

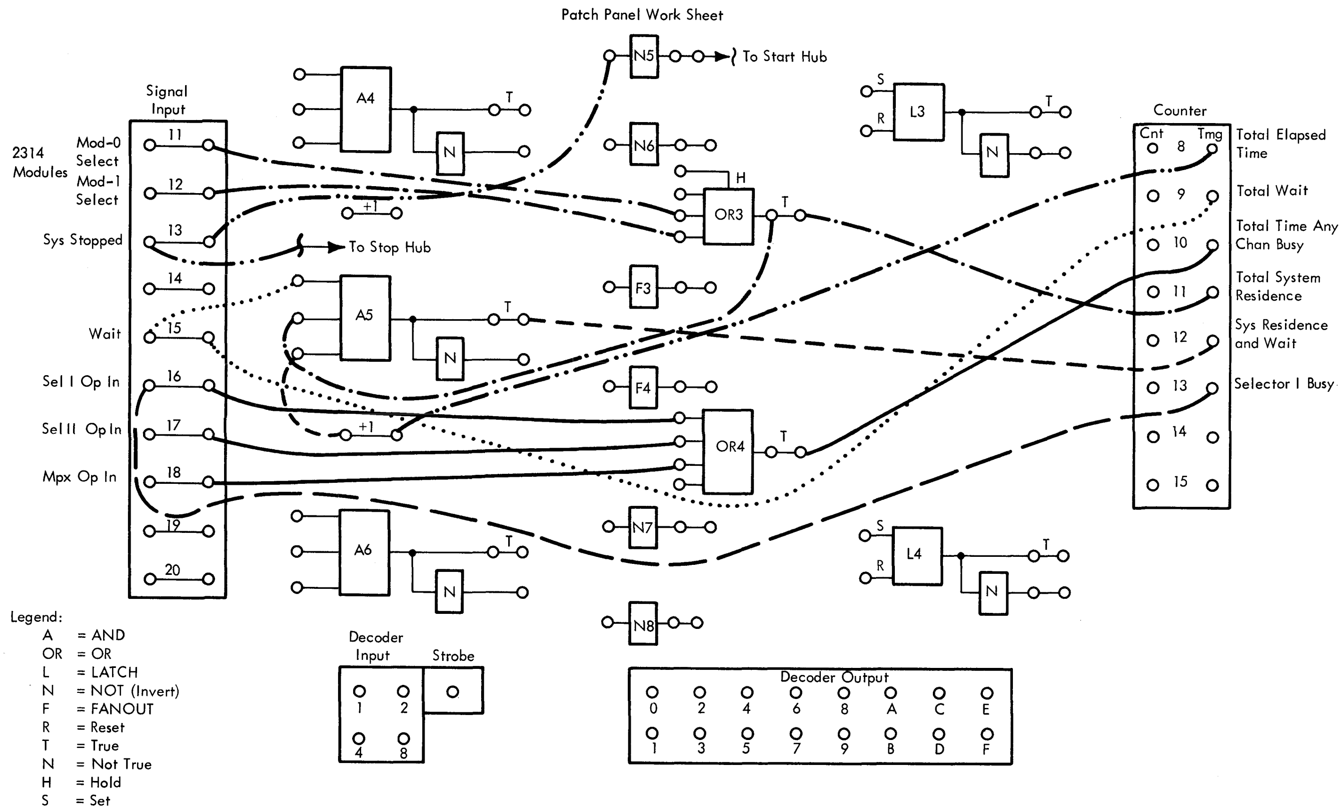


Figure 35. Wiring for Example 4

Appendix A. Primary Sources

True Function	*Line Name*	*ALD*
2040 Processing Unit		
Manual	HOLD CONDITION	KH142
Wait State	(No line name available)	KH171
Not Memory Protect Key 1, Current PSW Bit 11 Off	+CPU TAG REG BIT 3	KU011
Not Memory Protect Key 2, Current PSW Bit 10 Off	+CPU TAG REG BIT 2	KU011
Not Memory Protect Key 4, Current PSW Bit 9 Off	+CPU TAG REG BIT 1	KU012
Not Memory Protect Key 8, Current PSW Bit 8 Off	+CPU TAG REG BIT 0	KU013
Selector Channel 1 Busy	- OPERATIONAL IN LATCH SC1	GG513
Selector Channel 2 Busy	- OPERATIONAL IN LATCH SC2	HG513
Mpx Channel Busy	- IF OPERATIONAL IN MX	FA031
2044 Processing Unit		
Manual	- MANUAL STOPPED STATE	PK032
Not Wait	(No line name available)	KK081
Current PSW Bit 8	- SPLS OUTPUT BUSED BIT 0	KZ341
Current PSW Bit 9	- SPLS OUTPUT BUSED BIT 1	KZ341
Current PSW Bit 10	- SPLS OUTPUT BUSED BIT 2	KZ341
Current PSW Bit 11	- SPLS OUTPUT BUSED BIT 3	KZ351
Selector Channel 1 Not Busy	+OPL IN CH 1	GA011
Selector Channel 2 Not Busy	+OPL IN CH 2	HA011
Mpx Channel Busy	- OPERATIONAL IN	FX191
2050 Processing Unit		
Manual State	- MANUAL TRIGGER B	KS721
Run State	+MANUAL TRIGGER	KS721
Wait State	- WAIT BIT PSW 14	KS261
Compute State	+WAIT BIT PSW 14	KS261
Not Memory Protect Key 1, Current PSW Bit 11 Off	+CPU STOR PROT BIT 3	RP201
Not Memory Protect Key 2, Current PSW Bit 10 Off	+CPU STOR PROT BIT 2	RP201
Not Memory Protect Key 4, Current PSW Bit 9 Off	+CPU STOR PROT BIT 1	RP201
Not Memory Protect Key 8, Current PSW Bit 8 Off	+CPU STOR PROT BIT 0	RP201
Problem State	- MONITOR BIT PSW 15	KS261

True Function	*Line Name*	*ALD*
Supervisor State	+MONITOR BIT PSW 15	KS261
Processor Cycles to Support I/O Data Transfer	- I/O RTNE MODE	KE311
Main Storage Not Cycling	+ALLOW WRITE	MA031
Selector Channels 1, 2, 3 Interface Lines:	(Indicate channel)	
Service In Active	-SERVICE-IN	GS111
Selector Chan Busy	-OPER-IN A	GS121
Command Out Active	+COM OUT NOT ACTIVE	GS131
Address Out Active	+ADDR OUT NOT ACTIVE	GS131
Service Out Active	+SRV OUT NOT ACTIVE	GS131
Address In Active	- ADDRESS-IN	GS111
Status In Active	-STATUS-IN A	GS111
Run Meter	- CPU CLOCK RUNNING	PK061
Selector Channels 1, 2, 3 Bus Out Interface Lines:	(Indicate channel)	
Bus Out Bit 0 Active	(No line name available)	GN101
Bus Out Bit 1 Active	(No line name available)	GN111
Bus Out Bit 2 Active	(No line name available)	GN121
Bus Out Bit 3 Active	(No line name available)	GN131
Bus Out Bit 4 Active	(No line name available)	GN141
Bus Out Bit 5 Active	(No line name available)	GN151
Bus Out Bit 6 Active	(No line name available)	GN161
Bus Out Bit 7 Active	(No line name available)	GN171
Bus Out Bit P Active	(No line name available)	GN181
Selector Channels Bus In Interface Lines:	(Indicate channel)	
Bus In Bit 0 Not Active	+BUS IN POS 0	GN101
Bus In Bit 1 Not Active	+BUS IN POS 1	GN111
Bus In Bit 2 Not Active	+BUS IN POS 2	GN121
Bus In Bit 3 Not Active	+BUS IN POS 3	GN131
Bus In Bit 4 Not Active	+BUS IN POS 4	GN141
Bus In Bit 5 Not Active	+BUS IN POS 5	GN151
Bus In Bit 6 Not Active	+BUS IN POS 6	GN161
Bus In Bit 7 Not Active	+BUS IN POS 7	GN171
Mpx Channel Interface Tag Lines:		
Mpx Channel Busy with a Control Unit	- OP IN A	FA361
Request In Active	- REG IN	FA371
Select In Active	- SEL IN	FA361

True Function	*Line Name*	*ALD*
Address In Active	- ADDR IN	FA351
Status In Active	- STATUS IN	FA351
Service In Active	- SVC IN	FA351
Metering In Not Active	+CHO ME-I	FA471
Command Out Active	-COM OUT	FA141
Service Out Active	-SVC OUT	FA141
Address Out Active	-IF ADDR OUT	FA131
Mpx Channel Interface Bus In Lines:		
Bus In Bit P Not Active	+BUS IN BIT P	FA002
Bus In Bit 0 Not Active	+BUS IN BIT 0	FA002
Bus In Bit 1 Not Active	+BUS IN BIT 1	FA002
Bus In Bit 2 Not Active	+BUS IN BIT 2	FA002
Bus In Bit 3 Not Active	+BUS IN BIT 3	FA002
Bus In Bit 4 Not Active	+BUS IN BIT 4	FA002
Bus In Bit 5 Not Active	+BUS IN BIT 5	FA002
Bus In Bit 6 Not Active	+BUS IN BIT 6	FA002
Bus In Bit 7 Not Active	+BUS IN BIT 7	FA002
Mpx Channel Interface Bus Out Lines:		
Bus Out Bit P Not Active	+BUS OUT LTH P	FA051
Bus Out Bit 0 Not Active	+BUS OUT LTH 0	FA051
Bus Out Bit 1 Not Active	+BUS OUT LTH 1	FA051
Bus Out Bit 2 Not Active	+BUS OUT LTH 2	FA051
Bus Out Bit 3 Not Active	+BUS OUT LTH 3	FA051
Bus Out Bit 4 Not Active	+BUS OUT LTH 4	FA051
Bus Out Bit 5 Not Active	+BUS OUT LTH 5	FA051
Bus Out Bit 6 Not Active	+BUS OUT LTH 6	FA051
Bus Out Bit 7 Not Active	+BUS OUT LTH 7	FA051
2065 Processing Unit		
Manual	- MANUAL TGR	KW031
Wait	-PSW BIT 14	RW121
Not Memory Protect Key 1, Current PSW Bit 11 Off	+STORAGE KEY BIT 11	RW081
Not Memory Protect Key 2, Current PSW Bit 10 Off	+STORAGE KEY BIT 10	RW081
Not Memory Protect Key 4, Current PSW Bit 9 Off	+STORAGE KEY BIT 9	RW081
Not Memory Protect Key 8, Current PSW Bit 8 Off	+STORAGE KEY BIT 8	RW081

True Function	*Line Name*	*ALD*
2075 Processing Unit		
Not Manual	+MANUAL MODE	PY061
Wait	-PSW BIT 14 TO INTRPT	RE231
Current PSW Bit 8	- LHPSW 8 TO STG PROT	RG211
Current PSW Bit 9	- LHPSW 9 TO STG PROT	RG211
Current PSW Bit 10	- LHPSW 10 TO STG PROT	RG211
Current PSW Bit 11	- LHPSW 11 TO STG PROT	RG221
2860 Selector Channel		
Selector Channel 1 Busy	-OP-I	CC111
Selector Channel 2 Busy	-OP-I	CC111
Selector Channel 3 Busy	-OP-I	CC111
Service In	-SR-I	CC111
Service Out	-SR-O	CC117
I/O Command	-CMD-O	CC117
Bus Out Bit 0	-DATA OUT BUS BIT 0	UB121
Bus Out Bit 1	-DATA OUT BUS BIT 1	UB123
Bus Out Bit 2	-DATA OUT BUS BIT 2	UB125
Bus Out Bit 3	-DATA OUT BUS BIT 3	UB127
Bus Out Bit 4	-DATA OUT BUS BIT 4	UB131
Bus Out Bit 5	-DATA OUT BUS BIT 5	UB133
Bus Out Bit 6	-DATA OUT BUS BIT 6	UB135
Bus Out Bit 7	-DATA OUT BUS BIT 7	UB137
2870 Multiplexer Channel		
Mpx Chan Busy	-SSC OR MPLX OP IN	MX127
2311 Disk Storage Drive		
Seeks (Total)	+ACCESS READY	FD020
Seeks (Arm Movements)	+DETENT-IN	FD056
Not Module Busy	+MOD SELECT LINE 1	FD060
2314 Direct Access Storage Facility		
Seeks (Total)	- FILE BUSY	FL/FU053
Seeks (Arm Movements)	+DETENT-IN LATCH	FL/FU053
Upper Module Busy	-MOD SEL (Does not include seek time)	FU021
Lower Module Busy	-MOD SEL (Does not include seek time)	FL021

Appendix B. Generated Sources

Problem	*True Function*	*Combinatorial Logic*
2030-2075 Processing Units		
CPU Active	Wait, Manual	Not Wait and Not Manual
Any Channel Busy	Mpx Busy, Selectors 1, 2, . . . N, Busy	Mpx, *or* Selector 1, *or* Selector 2, *or* Selector "N" Busy
Wait and Any Channel Busy	Any Channel Busy Wait	Any Channel Busy *and* Wait
Selector/Selector Overlap	Selector 1 Busy, Selector 2 Busy	Selector 1 Busy *and* Selector 2 Busy (*and* Selector 3 Busy)
2030-2065 Processing Units		
CPU-Channel Overlap	Channel "N" Busy, Wait	Any Channel Busy *and* Not Wait
Partition "N" Compute	PSW Bits 8-11	Storage Protect Key "N" *and* Not Wait
2311 Disk Storage Drive *2314 Direct Access Storage Facility*		
Total Seeks	Access Ready	Not Access Ready
Seek (Arm Movements)	Detent-In	Not Detent-In

Appendix C. Probe Assignment Planning Form

The *IBM Basic Counter Unit Probe Assignment Planning Form,* ZX22-6946, is available in units of 25 sheets per pad. Users are advised to plan their work on this form before connecting the monitor probes to the assigned probe points on a CPU, channel, control unit, or I/O device.

IBM BASIC COUNTER UNIT PROBE ASSIGNMENT PLANNING FORM

Account ____________________ Prepared by ____________________

System Type ____________________ Date ____________________

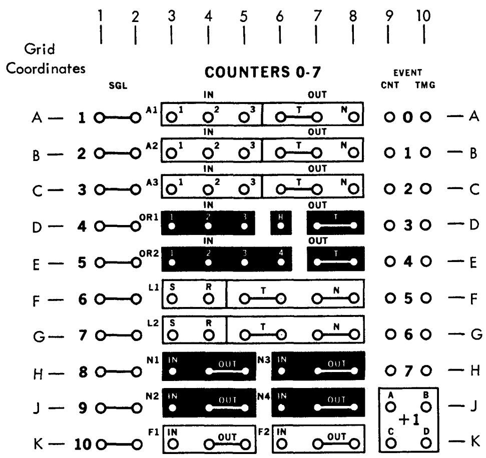
Basic Counter Unit Input	Junct Box	Pos	Line Name (Polarity)	Logic Page/Mach		Signal(s) Logic Pin	Ref 1	Ref 2	Ref 3	Ground
1	1	1			1 2					Ground
2	1	2			1 2					Ground
3	1	3			1 2					Ground
4	1	4			1 2					Ground
5	1	5			1 2					Ground
6	1	6			1 2					Ground
7	1	7			1 2					Ground
8	1	8			1 2					Ground
9	1	9			1 2					Ground
10	1	10			1 2					Ground
11	2	1			1 2					Ground
12	2	2			1 2					Ground
13	2	3			1 2					Ground
14	2	4			1 2					Ground
15	2	5			1 2					Ground
16	2	6			1 2					Ground
17	2	7			1 2					Ground
18	2	8			1 2					Ground
19	2	9			1 2					Ground
20	2	10			1 2					Ground

Monitor Probe Wire Legend

sig 1 = yellow sig 2 = white ref 1 = violet ref 2 = gray ref 3 = red ground = black

Appendix D. Operational Patch Panel 1

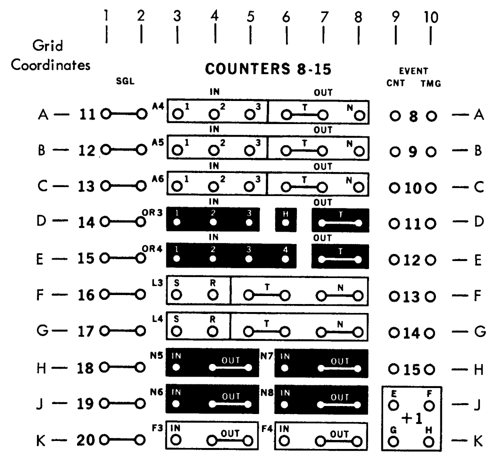
The 100 position operational patch panel 1 contains the Basic Counter Unit input and logical functions for counters 0-7. (An overall view of the patch panel is shown in Figure 26.)



Grid Position	Hub Title (Nominal delay in nanoseconds)	Description
A-K (1, 2)	SIGNAL	20 positions -- provide the Basic Counter Unit input signals from an external source. Grid positions 1 and 2 furnish a two-way distribution of the same signal to provide flexibility.
A (3, 4, 5)	AND1 In	3 positions -- provide the logical input to AND1. To perform combinatorial logic, all inputs must be wired.
A (6, 7)	AND1 Out True (60 ns)	2 positions -- provide the True function of AND1.
A (8)	AND1 Out Not True (85 ns)	1 position -- provides the Not True function of AND1.
B (3, 4, 5)	AND2 In	3 positions -- provide the logical input to AND2. All positions must be wired.
B (6, 7)	AND2 Out True (60 ns)	2 positions -- provide the True function of AND2.
B (8)	AND2 Out Not True (85 ns)	1 position -- provides the Not True function of AND2.
C (3, 4, 5)	AND3 In	3 positions -- provide the logical input to AND3. All positions must be wired.
C (6, 7)	AND3 Out True (60 ns)	2 positions -- provide the True function of AND3.
C (8)	AND3 Out Not True (85 ns)	1 position -- provides the Not True function of AND3.
D (3, 4, 5)	OR1 In	3 positions -- provide the logical input to OR1. Any True input position satisfies the function.
D (7, 8)	OR1 Out True (60 ns OR Latch Set) (110 ns OR Latch Reset)	2 positions -- provide the True function of OR1.
D (6)	OR1 Hold	1 position -- when wired, causes OR 1 to operate as a latch and provides the reset function to OR1. A True input allows the latch to remain set, and a Not True input resets the latch.
E (3, 4, 5, 6)	OR2 In	4 positions -- provide the logical inputs to OR2. Any True input position satisfies the function.
E (7, 8)	OR2 Out True (60 ns)	2 positions -- provide the True function of OR2.
F (3)	LATCH1 Set	1 position -- provides the logical set to LATCH1. A True input sets the latch.
F (4)	LATCH1 Reset	1 position -- provides a reset function to LATCH1. A Not True input allows the latch to remain set and a True input resets the latch.
F (5, 6)	LATCH1 Out True (60 ns Set) (85 ns Reset)	2 positions -- provide the True function of LATCH1.
F (7, 8)	LATCH1 Out Not True (85 ns Set) (110 ns Reset)	2 positions -- provide the Not True function of LATCH1.
G (3)	LATCH2 Set	1 position -- provides the logical set to LATCH2. A True input sets the latch.
G (4)	LATCH2 Reset	1 position -- provides a reset function to LATCH2. A Not True input allows the latch to remain set and a True input resets the latch.
G (5, 6)	LATCH2 Out True (60 ns Set) (85 ns Reset)	2 positions -- provide the True function of LATCH2.
G (7, 8)	LATCH2 Out Not True (85 ns Set) (110 ns Reset)	2 positions -- provide the Not True function of LATCH2.
H (3) J (3) H (6) J (6)	NOT1 In NOT2 In NOT3 In NOT4 In	4 positions -- provide invert functions for incoming or patch panel generated signals. Each NOT block is a single-legged function.
H (4, 5) J (4, 5) H (7, 8) J (7, 8)	NOT1 Out (35 ns) NOT2 Out (35 ns) NOT3 Out (35 ns) NOT4 Out (35 ns)	8 positions -- provide the output functions for the four NOT blocks. Each NOT block has two output hubs.
K (3) K (6)	FANOUT1 In FANOUT2 In	2 positions -- provide a means of distributing incoming or patch panel generated signals. The logical definition of the signal remains unchanged.
K (4, 5) K (7, 8)	FANOUT1 Out (60 ns) FANOUT2 Out (60 ns)	4 positions -- provide the output functions for the FANOUT hubs.
A-H (9)	EVENT COUNT	8 positions -- provide the input signals to each of the eight counters to count the number of occurrences of an event.
A-H (10)	EVENT TIME	8 positions -- provide the input signals to each of the eight counters to time the duration of an event.
J (9, 10) K (9, 10)	+1 A B C D	4 positions -- provide a True level for AND1, 2, and 3 if all inputs are not wired to logical functions. In this way unused AND inputs are wired to satisfy the logical function.

Appendix E. Operational Patch Panel 2

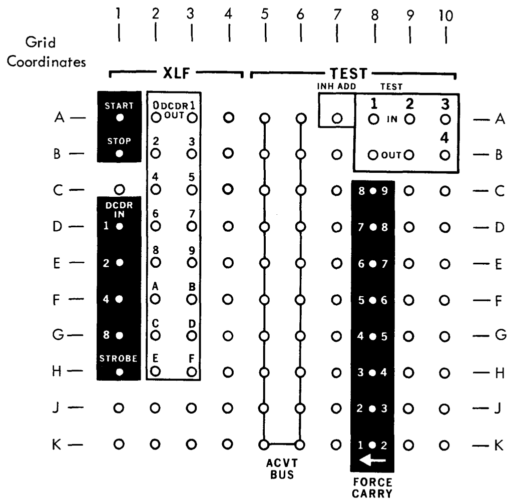
The 100 position operational patch panel 2 contains the Basic Counter Unit input and logical functions for counters 8-15. (An overall view of the patch panel is shown in Figure 26.)



Grid Position	Hub Title (Nominal delay in nanoseconds)	Description
A-K (1, 2)	SIGNAL	20 positions -- provide the Basic Counter Unit input signals from an external source. Grid positions 1 and 2 furnish a two-way distribution of the same signal to provide flexibility.
A (3, 4, 5)	AND4 In	3 positions -- provide the logical input to AND4. To perform combinatorial logic, all inputs must be wired.
A (6, 7)	AND4 Out True (60 ns)	2 positions -- provide the True function of AND4.
A (8)	AND4 Out Not True (85 ns)	1 position -- provides the Not True function of AND4.
B (3, 4, 5)	AND5 In	3 positions -- provide the logical input to AND5. All positions must be wired.
B (6, 7)	AND5 Out True (60 ns)	2 positions -- provide the True function of AND5.
B (8)	AND5 Out Not True (85 ns)	1 position -- provides the Not True function of AND5.
C (3, 4, 5)	AND6 In	3 positions -- provide the logical input to AND6. All positions must be wired.
C (6, 7)	AND6 Out True (60 ns)	2 positions -- provide the True function of AND6.
C (8)	AND6 Out Not True (85 ns)	1 position -- provides the Not True function of AND6.
D (3, 4, 5)	OR3 In	3 positions -- provide the logical input to OR3. Any True input position satisfies the function.
D (7, 8)	OR3 Out True (60 ns OR Latch Set) (110 ns OR Latch Reset)	2 positions -- provide the True function of OR3.
D (6)	OR3 Hold	1 position -- when wired, causes OR3 to operate as a latch and provides the reset function to OR3. A True input allows the latch to remain set and a Not True input resets the latch.
E (3, 4, 5, 6)	OR4 In	4 positions -- provide the logical inputs to OR4. Any True input position satisfies the function.
E (7, 8)	OR4 Out True (60 ns)	2 positions -- provide the True function of OR4.
F (3)	LATCH3 Set	1 position -- provides the logical set to LATCH3. A True input sets the latch.
F (4)	LATCH3 Reset	1 position -- provides a reset function to LATCH3. A Not True input allows the latch to remain set and a True input resets the latch.
F (5, 6)	LATCH3 Out True (60 ns Set) (85 ns Reset)	2 positions -- provide the True function of LATCH3.
F (7, 8)	LATCH3 Out Not True (85 ns Set) (110 ns Reset)	2 positions -- provide the Not True function of LATCH3.
G (3)	LATCH4 Set	1 position -- provides the logical set to LATCH4. A True input sets the latch.
G (4)	LATCH4 Reset	1 position -- provides a reset function to LATCH4. A Not True input allows the latch to remain set and a True input resets the latch.
G (5, 6)	LATCH4 Out True (60 ns Set) (85 ns Reset)	2 positions -- provide the True function of LATCH4.
G (7, 8)	LATCH4 Out Not True (85 ns Set) (110 ns Reset)	2 positions -- provide the Not True function of LATCH4.
H (3) J (3) H (6) J (6)	NOT5 In NOT6 In NOT7 In NOT8 In	4 positions -- provide input functions for incoming or patch panel generated signals. Each NOT block is a single-legged function.
H (4, 5) J (4, 5) H (7, 8) J (7, 8)	NOT5 Out (35 ns) NOT6 Out (35 ns) NOT7 Out (35 ns) NOT8 Out (35 ns)	8 positions -- provide the output functions for the four NOT blocks. Each NOT block has two output hubs.
K (3) K (6)	FANOUT3 In FANOUT4 In	2 positions -- provide a means of distributing incoming or patch panel generated signals. The logical definition of the signal remains unchanged.
K (4, 5) K (7, 8)	FANOUT3 Out (60 ns) FANOUT4 Out (60 ns)	4 positions -- provide the output functions for the FANOUT hubs.
A-H (9)	EVENT COUNT	8 positions -- provide the input signals to each of the eight counters to count the number of occurrences of an event.
A-H (10)	EVENT TIME	8 positions -- provide the input signals to each of the eight counters to time the duration of an event.
J (9, 10) K (9, 10)	+1 E F G H	4 positions -- provide a True level for AND4, 5, 6 if all inputs are not wired to logical functions. In this way unused AND inputs are wired to satisfy the logical function.

Appendix F. XLF and Test Patch Panel

The 100 position XLF (Expanded Logic Functions) and test patch panel contains all of the Basic Counter Unit maintenance functions. (An overall view of the patch panel is shown in Figure 26.)

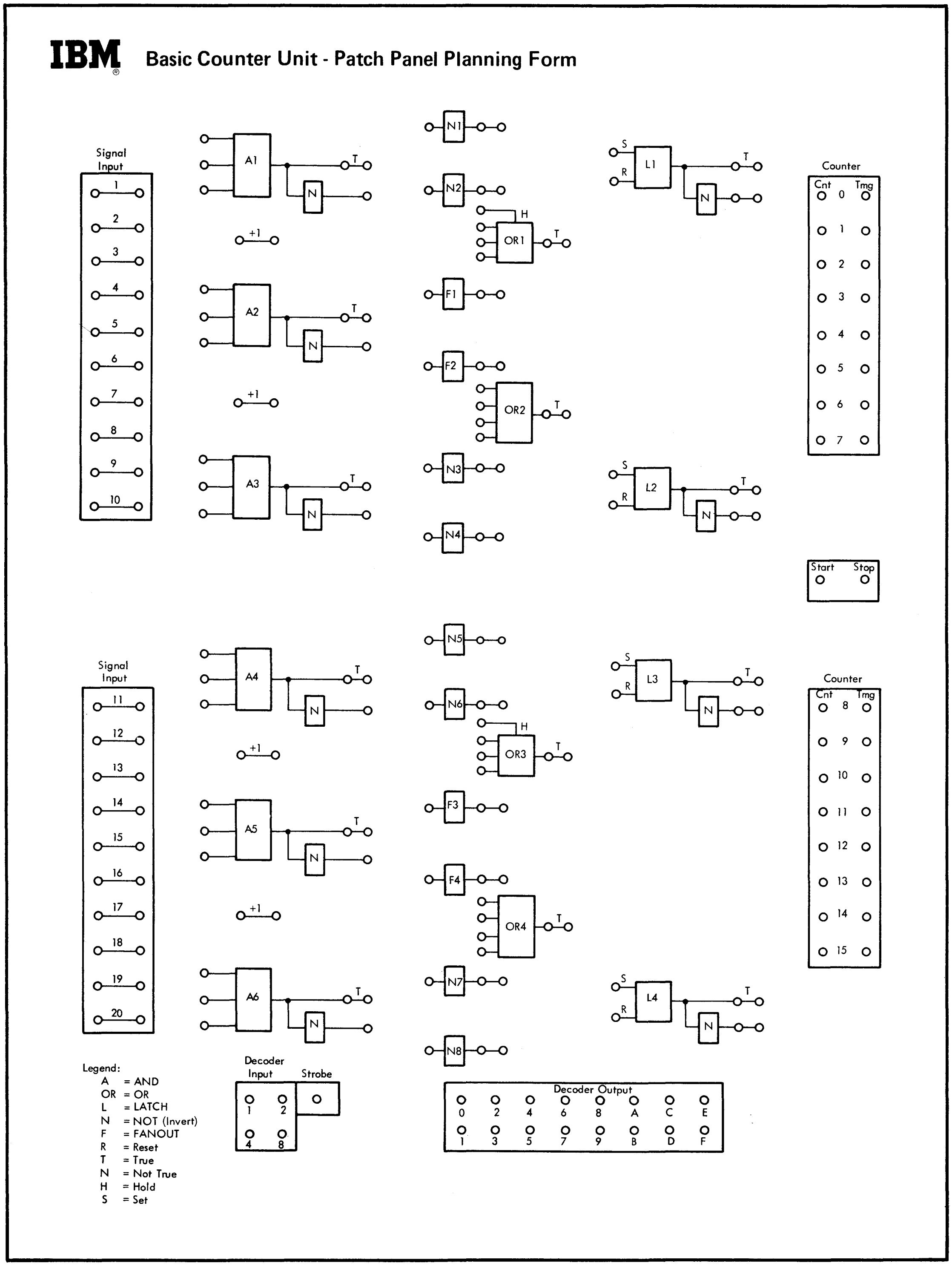


Grid Position	Hub Title	Description
A (1)	START	1 position -- enables the Basic Counter Unit counters from an external source. The source may be an input pulse or patch panel logic. A True signal activates the function and turns on the count enable indicator. This hub is interlocked with PUNCH GO to prevent data skew while punching out counter contents. If a True level is used at this hub position, the stop pushbutton becomes inoperative.
B (1)	STOP	1 position -- provides for stopping the Basic Counter Unit counters from an external source, which may be an input pulse or patch panel logic. A True signal activates this function and turns off the count enable indicator. If a True level is used at this hub position, the start pushbutton becomes inoperative.
D, E, F, G (1)	DECODER In 1, 2, 4, 8	4 positions -- provide the decoder input. A position that is wired as a True function defines the presence of the particular bit. If a bit position is not wired, it is treated by the decoder as a Not True function.
H (1)	STROBE	1 position -- when wired, provides the sample pulse for the decoder output. The strobe must be a True function. Any combination of four True inputs to the decoder plus a True input to the strobe produces a True decoder output.
A-H (2, 3)	DECODER Out	16 positions -- provide the decoder output function. Only one of these hubs may be active at one time. The decoded output is True for the duration of the strobe pulse.
A-K (5, 6)*	ACVT BUS	20 positions -- provide the activate positions for the several maintenance functions. No function is active unless it is wired to one of these positions.
A (8)	TEST1	1 position -- when wired to the activate bus, enables all Basic Counter Unit counters to be cycled at a fixed rate of 1 MHz. TEST1, when wired to an activate bus position, inhibits all external signals from being counted or timed within the Basic Counter Unit.
A (9)	TEST2	1 position -- when wired to the activate bus, enables all Basic Counter Unit counters to be cycled on each depression of the start pushbutton. The TEST2 step pulse is injected into stage 9 of the counter (low-order position of adder). This test checks for proper adder operation. This position, when wired, inhibits all external signals from being counted or timed within the Basic Counter Unit.
C (8) D (8) E (8) F (8) G (8) H (8) J (8) K (8)	FORCE CARRY 9-8 8-7 7-6 6-5 5-4 4-3 3-2 2-1	8 positions -- when wired, inject the test signal directly into each relative stage of the adder to enable checking for proper adder operation without waiting for a large count to be accumulated. A single stage or combinations of stages may be wired. These positions are enabled only if TEST1 or TEST2 are activated.
A (7)	INH ADD	1 position -- when activated, inhibits the ADD1 signal from being generated within the adder. This position is used to check the data path through the adder and the counter positions in a regenerative mode. This position is enabled only if TEST1 or TEST2 is activated.
A (10)	TEST3	1 position -- when activated, causes the punch controls to cycle at a rate of 1 MHz. This hub also causes PUNCH READY to turn on to allow scoping the punch controls when a punch is not present. (TEST3 is for CE use only.)
B (10)	TEST4	1 position -- when activated, causes the punch controls to step once for each depression of the start switch if PUNCH GO has been depressed. COUNT ENABLE does not turn on and this test can be used to single cycle through a punch sequence. (TEST hub 4 is for CE use only.)
B (8)	TEST1 Out	1 position -- provides a 100- nanosecond pulse at a rate of 1 MHz for testing the combinatorial logic.
B (9)	TEST2 Out	1 position -- provides a single pulse for each depression of the start switch. This can be used for checking the logic latches.

* ACVT BUS may be used as additional +1 lines if functions required use more +1's than are furnished by the operational patch panel.

Appendix G. Patch Panel Planning Form

The *IBM Basic Counter Unit Patch Panel Planning Form,* ZX22-6952, is available in units of 25 sheets per pad. Users are advised to plan their work on this form before wiring the various functions on the patch panel. By using the patch panel planning form, the user increases his understanding of the logical functions on the patch panel and diminishes the possibility of error when wiring the patch panel.



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