IBM®

Field Engineering

Maintenance Diagrams

Restricted Distribution

2030

Processing Unit

System/360 Model 30

PREFACE

This manual contains Condensed Logic Flow charts to be used for recall or instructional purposes.

The EC Level of the CAS Logic Diagrams (CLD) for the basic machine is 128062. The Level for the 1400 Compatibility section is 128122.

The charts in this manual were drawn to show the general logic and flow of the microprogram used by the 2030. The charts contain the CAS logic diagram page numbers where the exact process can be located and followed.

Fifth Edition (June 1967)

This edition, Y24-3466-2, is a major revision of and obsoletes the previous edition, Y24-3466-1, and the Supplement Y24-3490. Principal changes include the addition of the diagnostic techniques charts and information pertaining to ROAR stop.

This manual has been prepared by the IBM Systems Development Division, Product Publications, Dept. 171, P. O. Box 6, Endicott, N. Y. 13760. Send comments concerning the manual to this address.

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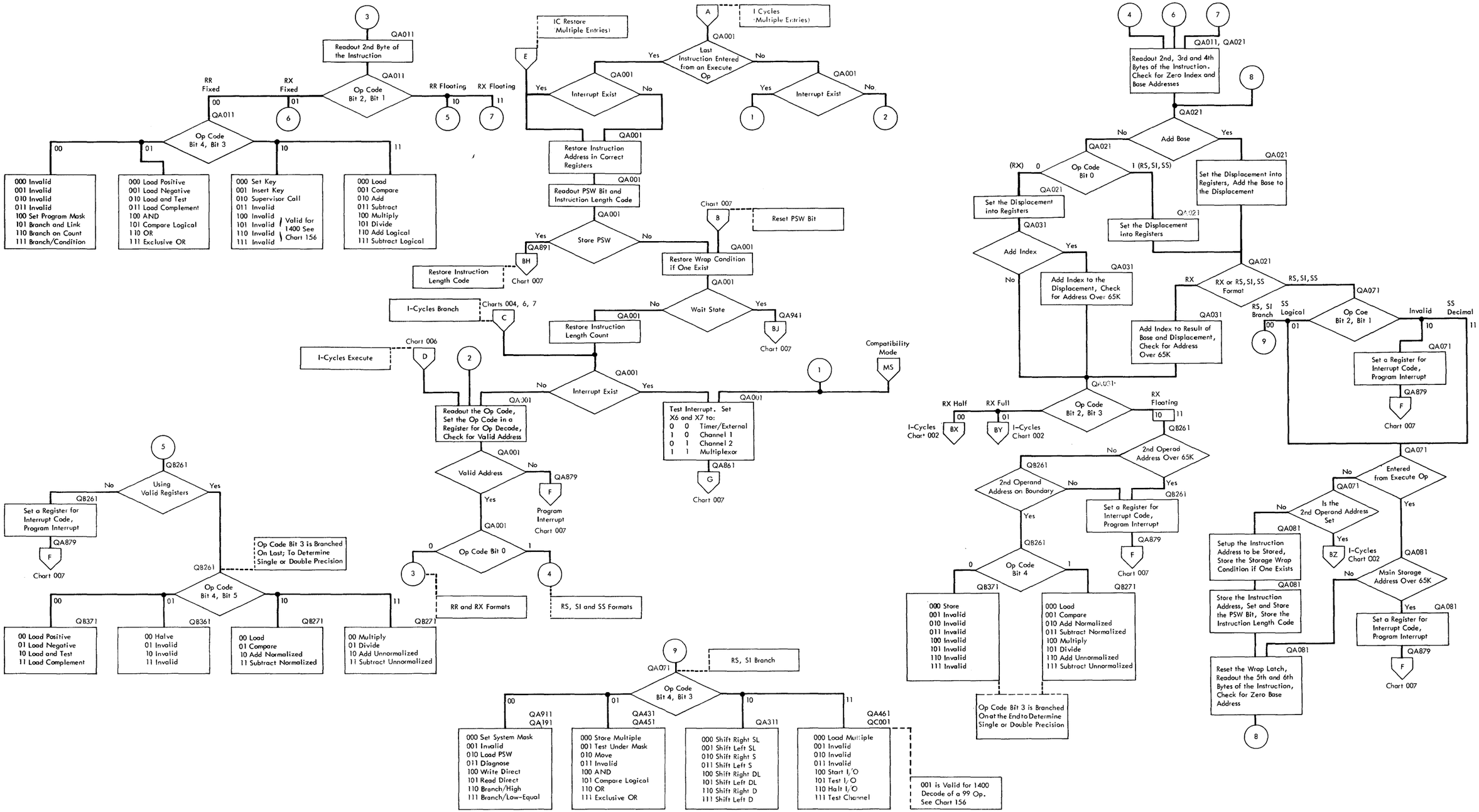
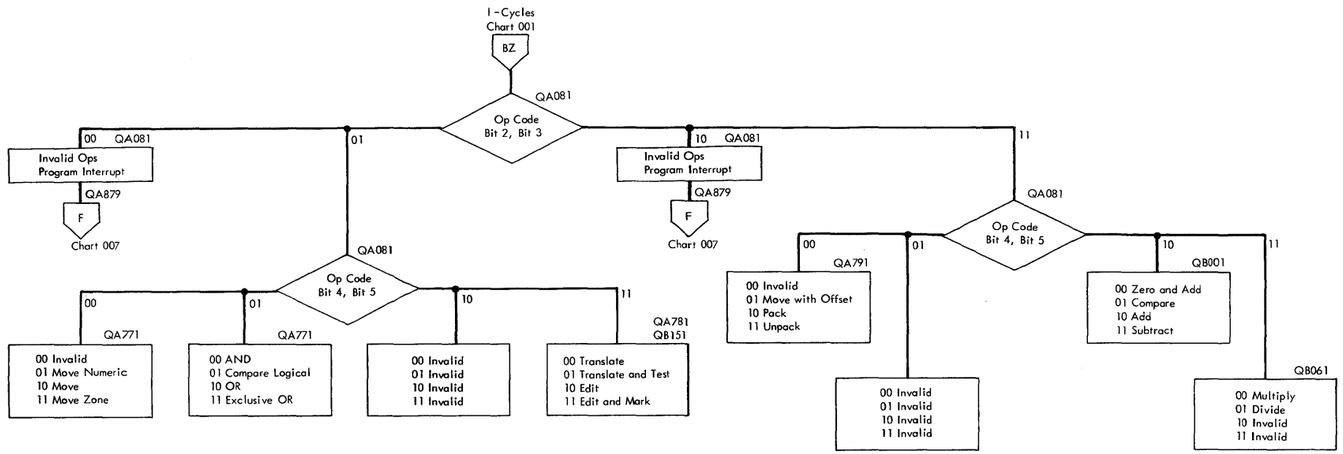
Contents

CONDENSED LOGIC FLOW CHARTS

DIAGNOSTIC TECHNIQUES CHARTS

ROAR STOP CHARTS


3
QA011
Readout 2nd Byte of the Instruction
QA011
Op Code Bit 2, Bit 1
RR Fixed
RX Fixed
RR Floating
RX Floating
00
01
10
11
6
5
7
QA011
Op Code Bit 4, Bit 3
00 Invalid
001 Invalid
010 Invalid
011 Invalid
100 Set Program Mask
101 Branch and Link
110 Branch on Count
111 Branch/Condition
000 Load Positive
001 Load Negative
010 Load and Test
011 Load Complement
100 AND
101 Compare Logical
110 OR
111 Exclusive OR
000 Set Key
001 Insert Key
010 Supervisor Call
011 Invalid
100 Invalid
101 Invalid
110 Invalid
111 Invalid
Valid for 1400 See Chart 156
000 Load
001 Compare
010 Add
011 Subtract
100 Multiply
101 Divide
110 Add Logical
111 Subtract Logical
E
IC Restore Multiple Entries
A
I Cycles (Multiple Entries)
QA001
Last Instruction Entered from an Execute Op
Yes
No
QA001
Interrupt Exist
Yes
No
1
2
QA001
Restore Instruction Address in Correct Registers
QA001
Readout PSW Bit and Instruction Length Code
QA001
Store PSW
Yes
No
QA891
BH
Chart 007
Restore Instruction Length Code
Chart 007
B
Reset PSW Bit
QA001
Restore Wrap Condition if One Exist
QA001
Wait State
No
Yes
QA941
BJ
Chart 007
I-Cycles Branch
Charts 004, 6, 7
C
QA001
Restore Instruction Length Count
I-Cycles Execute
Chart 006
D
2
QA001
Interrupt Exist
No
Yes
1
Compatibility Mode
MS
QA001
Readout the Op Code, Set the Op Code in a Register for Op Decode, Check for Valid Address
QA001
Valid Address
No
Yes
QA879
F
Program Interrupt
Chart 007
QA001
Op Code Bit 0
0
1
3
4
RR and RX Formats
RS, SI and SS Formats
QA001
Test Interrupt. Set X6 and X7 to:
0 0 Timer/External
1 0 Channel 1
0 1 Channel 2
1 1 Multiplexor
QA861
G
Chart 007
5
QB261
Using Valid Registers
No
Yes
QB261
Set a Register for Interrupt Code, Program Interrupt
QA879
F
Chart 007
Op Code Bit 3 is Branched On Last; To Determine Single or Double Precision
QB261
Op Code Bit 4, Bit 5
00
01
10
11
QB371
00 Load Positive
01 Load Negative
10 Load and Test
11 Load Complement
QB361
00 Halve
01 Invalid
10 Invalid
11 Invalid
QB271
00 Load
01 Compare
10 Add Normalized
11 Subtract Normalized
QB271
00 Multiply
01 Divide
10 Add Unnormalized
11 Subtract Unnormalized
9
QA071
RS, SI Branch
Op Code Bit 4, Bit 3
00
01
10
11
QA911
QA191
000 Set System Mask
001 Invalid
010 Load PSW
011 Diagnose
100 Write Direct
101 Read Direct
110 Branch/High
111 Branch/Low-Equal
QA431
QA451
000 Store Multiple
001 Test Under Mask
010 Move
011 Invalid
100 AND
101 Compare Logical
110 OR
111 Exclusive OR
QA311
000 Shift Right SL
001 Shift Left SL
010 Shift Right S
011 Shift Left S
100 Shift Right DL
101 Shift Left DL
110 Shift Right D
111 Shift Left D
QA461
QC001
000 Load Multiple
001 Invalid
010 Invalid
011 Invalid
100 Start I/O
101 Test I/O
110 Halt I/O
111 Test Channel
001 is Valid for 1400 Decode of a 99 Op. See Chart 156
4
6
7
QA011, QA021
Readout 2nd, 3rd and 4th Bytes of the Instruction. Check for Zero Index and Base Addresses
8
QA021
Add Base
No
Yes
QA021
Op Code Bit 0
(RX) 0
1 (RS, SI, SS)
QA021
Set the Displacement into Registers
QA031
Add Index
Yes
No
QA031
Add Index to the Displacement, Check for Address Over 65K
QA021
Set the Displacement into Registers, Add the Base to the Displacement
QA021
Set the Displacement into Registers
QA021
RX or RS, SI, SS Format
RX
RS, SI, SS
QA031
Add Index to Result of Base and Displacement, Check for Address Over 65K
RS, SI Branch
SS Logical
QA071
Op Coe Bit 2, Bit 1
Invalid
SS Decimal
00
01
10
11
9
QA071
Set a Register for Interrupt Code, Program Interrupt
QA879
F
Chart 007
QA031
Op Code Bit 2, Bit 3
RX Half
RX Full
RX Floating
00
01
10
11
I-Cycles Chart 002
BX
BY
I-Cycles Chart 002
QB261
2nd Operad Address Over 65K
No
Yes
QB261
2nd Operand Address on Boundary
No
Yes
QB261
Set a Register for Interrupt Code, Program Interrupt
QA879
F
Chart 007
QB261
Op Code Bit 4
0
1
QB371
000 Store
001 Invalid
010 Invalid
011 Invalid
100 Invalid
101 Invalid
110 Invalid
111 Invalid
QB271
000 Load
001 Compare
010 Add Normalized
011 Subtract Normalized
100 Multiply
101 Divide
110 Add Unnormalized
111 Subtract Unnormalized
Op Code Bit 3 is Branched On at the End to Determine Single or Double Precision
QA071
Entered from Execute Op
No
Yes
QA071
Is the 2nd Operand Address Set
No
Yes
BZ
I-Cycles Chart 002
QA081
Setup the Instruction Address to be Stored, Store the Storage Wrap Condition if One Exists
QA081
Store the Instruction Address, Set and Store the PSW Bit, Store the Instruction Length Code
QA081
Reset the Wrap Latch, Readout the 5th and 6th Bytes of the Instruction, Check for Zero Base Address
8
QA081
Main Storage Address Over 65K
No
Yes
QA081
Set a Register for Interrupt Code, Program Interrupt
QA879
F
Chart 007



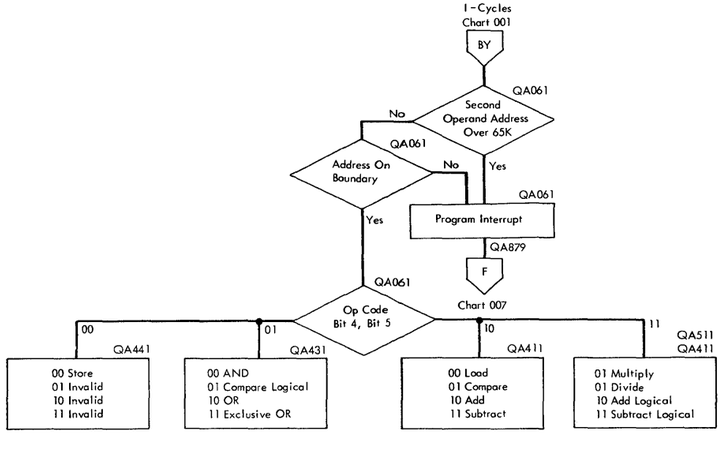
OP	Name	Chart
04	Set Program Mask	007
05	Branch and Link	006
06	Branch on Count	004
07	Branch on Condition	004
08	Set Key	003
09	Insert Key	003
0A	Supervisor Call	007
10	Load Positive	003
11	Load Negative	003
12	Load and Test	003
13	Load Complement	027
14	AND	004
15	Compare Logical	004
16	OR	004
17	Exclusive OR	004
18	Load	003
19	Compare	005
1A	Add	005
1B	Subtract	005
1C	Multiply	008
1D	Divide	009
1E	Add Logical	005
1F	Subtract Logical	005
20	Load Positive	003
21	Load Negative	003
22	Load and Test	003
23	Load Complement	027
24	Halve	026
28	Load	027
29	Compare	028
2A	Add N	028
2B	Subtract N	028
2C	Multiply	030
2D	Divide	032
2E	Add U	028
2F	Subtract U	028
30	Load Positive	003
31	Load Negative	003
32	Load and Test	003
33	Load Complement	027
34	Halve	026
38	Load	027
39	Compare	028
3A	Add N	028
3B	Subtract N	028

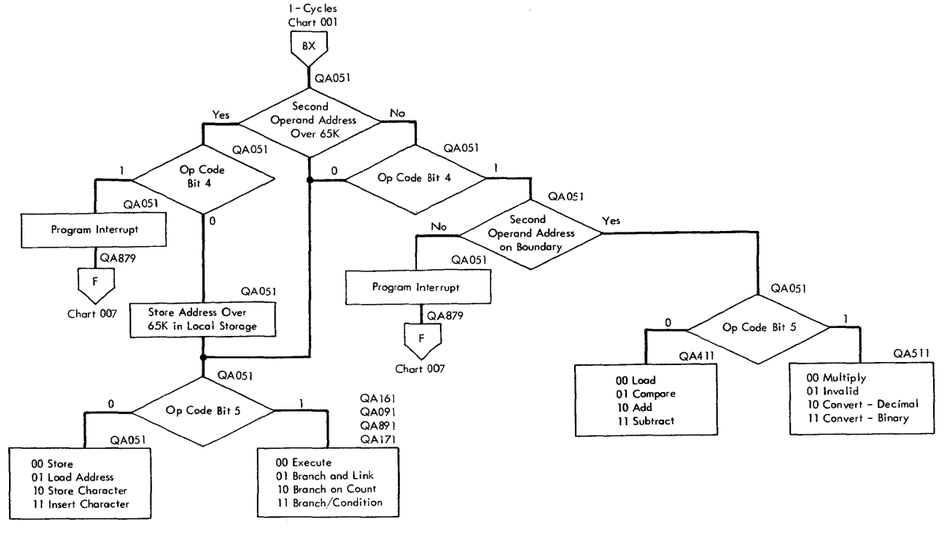
Op	Name	Chart
3C	Multiply	030
3D	Divide	032
3E	Add U	028
3F	Subtract U	028
40	Store	003
41	Load Address	003
42	Store Character	003
43	Insert Character	003
44	Execute	006
45	Branch and Link	006
46	Branch on Count	004
47	Branch on Condition	004
48	Load	003
49	Compare	005
4A	Add	005
4B	Subtract	005
4C	Multiply	008
4E	Convert - Decimal	012
4F	Convert - Binary	011
50	Store	003
54	AND	004
55	Compare Logical	004
56	OR	004
57	Exclusive OR	004
58	Load	003
59	Compare	005
5A	Add	005
5B	Subtract	005
5C	Multiply	008
5D	Divide	009
5E	Add Logical	005
5F	Subtract Logical	005
60	Store	026
68	Load	027
69	Compare	028
6A	Add N	028
6B	Subtract N	028
6C	Multiply	030
6D	Divide	032
6E	Add U	028
6F	Subtract U	028
70	Store	026
78	Load	027
79	Compare	028
7A	Add N	028

Op	Name	Chart
7B	Subtract N	028
7C	Multiply	030
7D	Divide	032
7E	Add U	028
7F	Subtract U	028
80	Set System Mask	007
82	Load PSW	007
83	No Chart	---
84	No Chart	---
85	No Chart	---
86	Branch/High	006
87	Branch/Low Equal	006
88	Shift Right SL	013
89	Shift Left SL	013
8A	Shift Right S	013
8B	Shift Left S	013
8C	Shift Right DL	013
8D	Shift Left DL	013
8E	Shift Right D	013
8F	Shift Left D	013
90	Store Multiple	014
91	Test Under Mask	014
92	Move	014
93	Test and Set	014
94	AND	004
95	Compare Logical	004
96	OR	004
97	Exclusive OR	004
98	Load Multiple	014
9C	Start I/O	034
9D	Test I/O	034
9E	Halt I/O	034
9F	Test Channel	034
D1	Move Numeric	015
D2	Move	015
D3	Move Zone	015
D4	AND	015
D5	Compare Logical	015
D6	OR	015
D7	Exclusive OR	015
DC	Translate	016
DD	Translate and Test	016
DE	Edit	017
DF	Edit and Mark	017
F1	Move with Offset	019

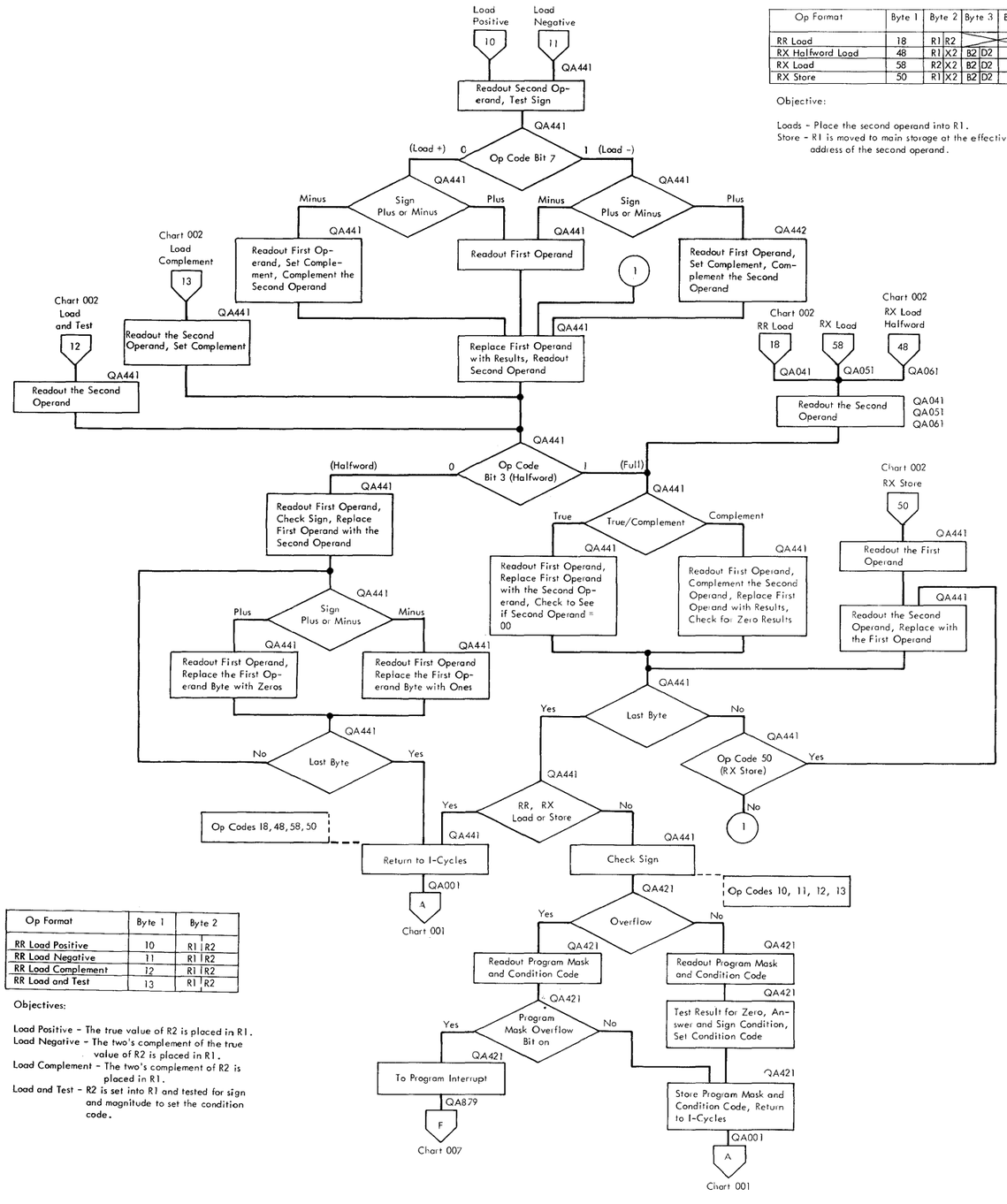
Op	Name	Chart
F2	Pack	019
F3	Unpack	019
F8	Zero and Add	020
F9	Compare	020
FA	Add	020
FB	Subtract	020
FC	Multiply	022
FD	Divide	024

Notes: Codes Not Shown Are Invalid and Cause a Program Interrupt.





CLF 002 I-Cycles, Sheet 2



Op Format	Byte 1	Byte 2	Byte 3	Byte 4
RR Load	18	R1 R2		
RX Halfword Load	48	R1 X2	B2 D2	D2
RX Load	58	R2 X2	B2 D2	D2
RX Store	50	R1 X2	B2 D2	D2

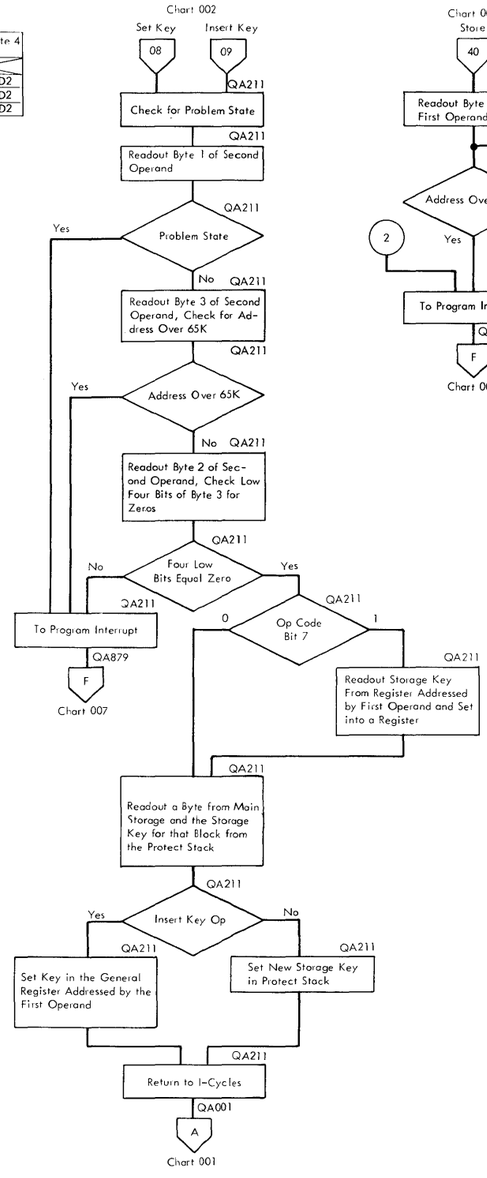
Objective:

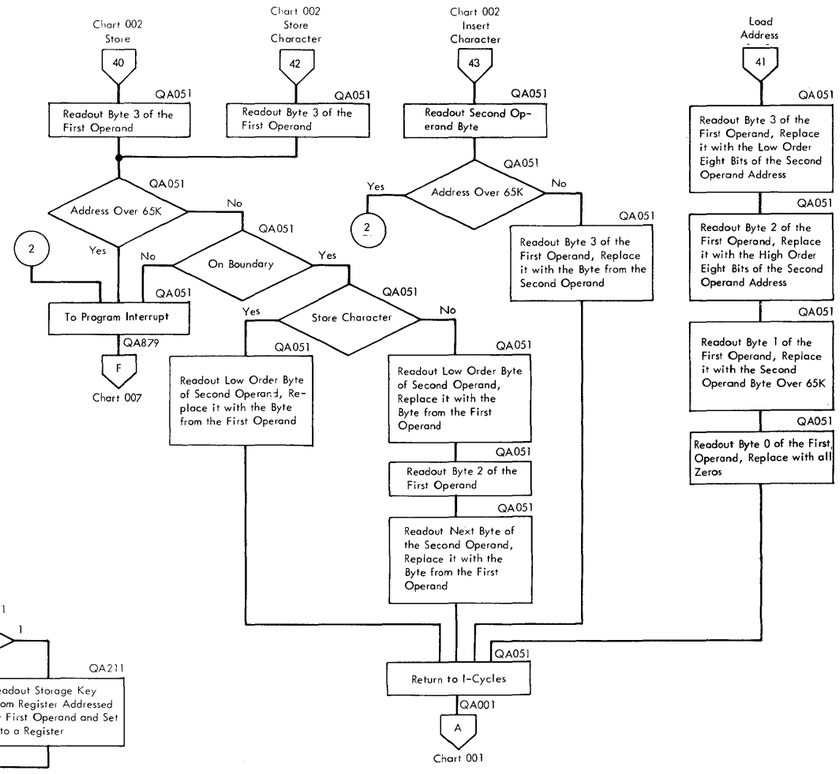
Loads - Place the second operand into R1.
Store - R1 is moved to main storage at the effective address of the second operand.

Op Format	Byte 1	Byte 2
RR Load Positive	10	R1 R2
RR Load Negative	11	R1 R2
RR Load Complement	12	R1 R2
RR Load and Test	13	R1 R2

Objectives:

Load Positive - The true value of R2 is placed in R1.
Load Negative - The two's complement of the true value of R2 is placed in R1.
Load Complement - The two's complement of R2 is placed in R1.
Load and Test - R2 is set into R1 and tested for sign and magnitude to set the condition code.





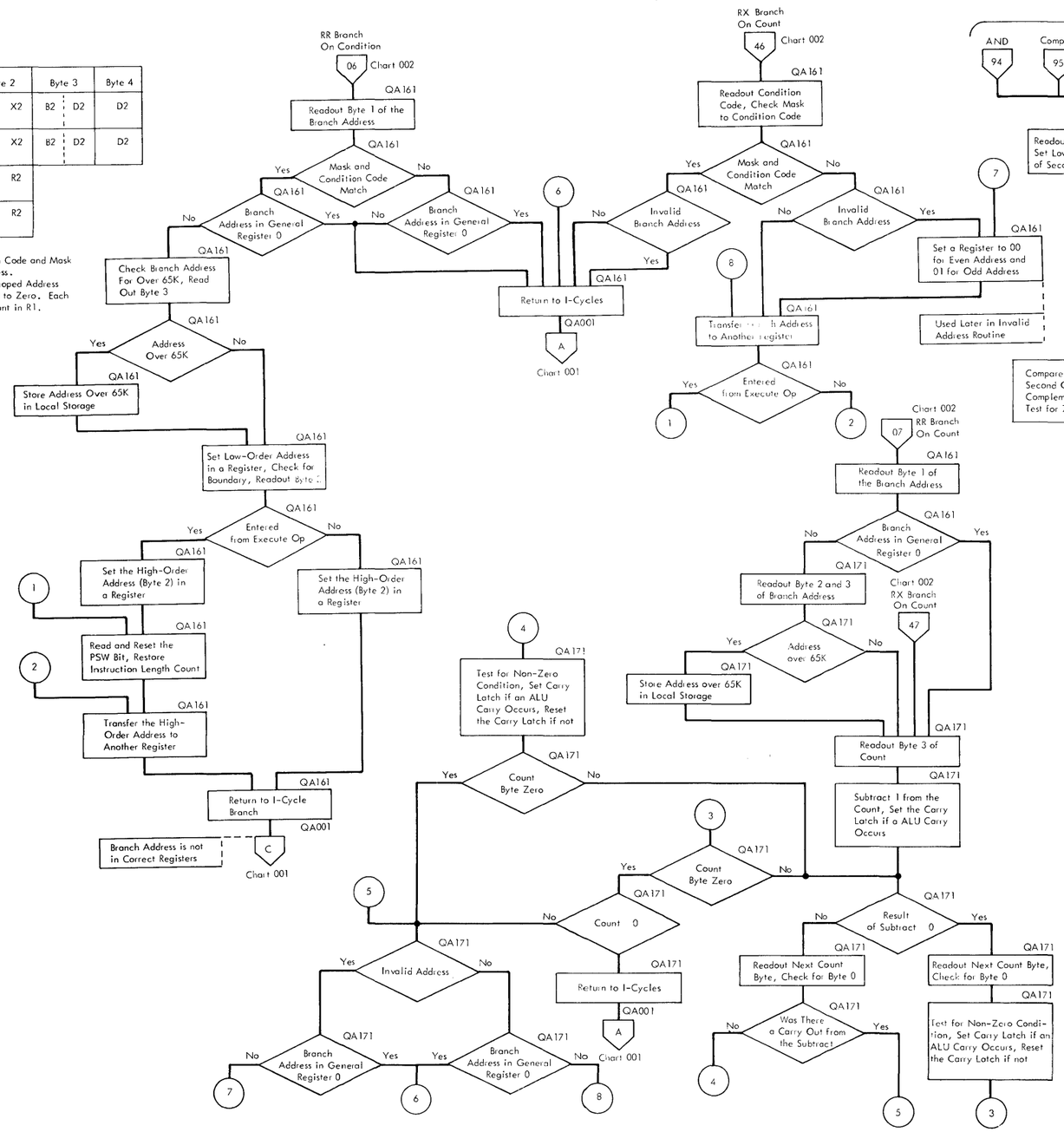
Op Format	Byte 1	Byte 2	Byte 3	Byte 4
RR Set Key	08	R1 R2		
RR Insert Key	09	R1 R2		
RX Store Half.	40	R1 X2	B2 D2	D2
RX Load Address	41	R1 X2	B2 D2	D2
RX Store Char.	42	R1 X2	B2 D2	D2
RX Insert Char.	43	R1 X2	B2 D2	

Objective:

Set Key - Set the Storage Protect Key for main storage block addressed by R2 into the stack.
Insert Key - Read the Storage Protect Key for main storage block addressed by R2 and set into R1.
Store Halfword - To move the 16 low order bits of R1 to main storage addressed by the second operand.
Load Address - Set the effective address of the second operand into the low 24 bits of R1.
Store Character - Move byte 3 of R1 to main storage addressed by second operand.
Insert Character - The byte in main storage addressed by the second operand is set into byte 3 of R1.

OP Format	Byte 1	Byte 2	Byte 3	Byte 4
RX Branch On Condition	46	M1 X2	B2 | D2	D2
RX Branch On Count	47	R1 X2	B2 | D2	D2
RR Branch On Condition	06	M1 R2		
RR Branch On Count	07	R1 R2		

Objective:
Branch On Condition: If Condition Code and Mask Match, Branch to Developed Address.
Branch On Count: Branch to Developed Address Each Time Until Sum In R1 Is Equal to Zero. Each Time Through Subtract 1 from Amount in R1.



OP Format	Byte 1	Byte 2	Byte 3	Byte 4
RR AND	14	R1 R2		
RR OR	15	R1 R2		
RR Compare	16	R1 R2		
RR Exclusive OR	17	R1 R2		
RX, AND	54	R1 X2	B2 — D2	
RX OR	55	R1 X2	B2 — D2	
RX Compare	56	R1 X2	B2 — D2	
RX Exclusive OR	57	R1 X2	B2 — D2	
SI AND	94	I2	B1 — D1	
SI OR	95	I2	B1 — D1	
SI Compare	96	I2	B1 — D1	
SI Exclusive OR	97	I2	B1 — D1	

Objectives:

AND - To AND the Bytes of the First Operand with the Bytes of the Second Operand. The Results of the AND Replace the First Operand.

OR - To OR the Bytes of the First Operand with the Bytes of the Second Operand. The Results of the OR Replace the First Operand.

Compare - Compare the First Operand to the Second Operand. Comparison is Left to Right, Ends on an Unequal.

Exclusive OR - The First Operand is Exclusively ORED with the Second Operand. The Results of the Exclusive OR Replace the First Operand.

Note: In the SI Format, I2 is the Second Operand and is One Byte Long. The Address of the First Operand is for the Leftmost Byte in the Field.

The Condition of the Result for AND, OR, Compare, and Exclusive OR is Stored in the Condition Code Register in Local Storage.

Example: (Only Two Bytes Shown)

	AND	OR
First	0001 1100 1010 0001	0001 1100 1010 0001
Second	0001 0011 1001 1110	0001 0011 1001 1110
Result	0001 0000 1000 0000	0001 1111 1011 1111

	Compare	Exclusive OR
First	0001 1100 1010 0001	0001 1100 1010 0001
Second	0001 0011 1001 1110	0001 0011 1001 1110
		0000 1111 0011 1111
First	0001 1100 1010 0001	
Complement Second	1110 1100	
Unequal	0000 1000	
	Ends	

Op Format	Byte 1	Byte 2	Byte 3	Byte 4
RR Compare	19	R1 R2		
RR Add	1A	R1 R2		
RR Subtract	1B	R1 R2		
RR Add Logical	1E	R1 R2		
RR Subtract Log.	1F	R1 R2		
RX Half Compare	49	R1 X2	B2 D2	D2
RX Half Add	4A	R1 X2	B2 D2	D2
RX Half Subtract	4B	R1 X2	B2 D2	D2
RX Compare	59	R1 X2	B2 D2	D2
RX Add	5A	R1 X2	B2 D2	D2
RX Subtract	5B	R1 X2	B2 D2	D2
RX Add Logical	5E	R1 X2	B2 D2	D2
RX Subtract Log.	5F	R1 X2	B2 D2	D2

Objective:

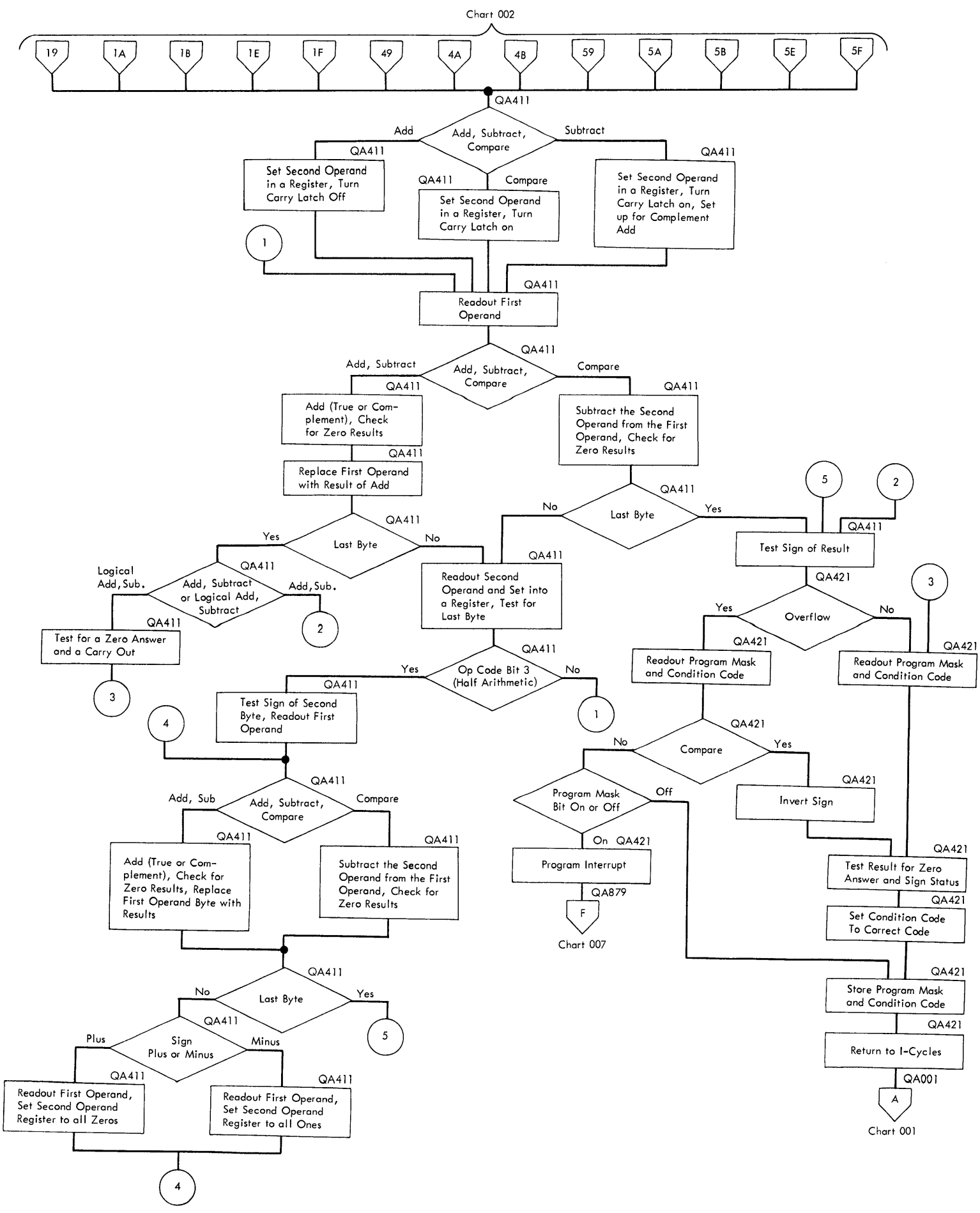
Add - The second operand is added to the first operand, and the sum is placed in the first operand location.

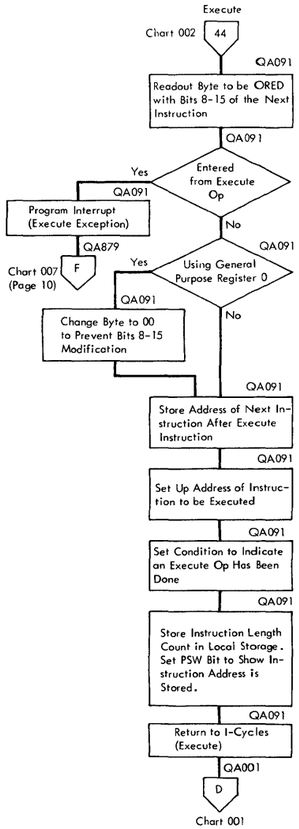
Add Logical - Same as Add. The difference is in the setting of the condition code.

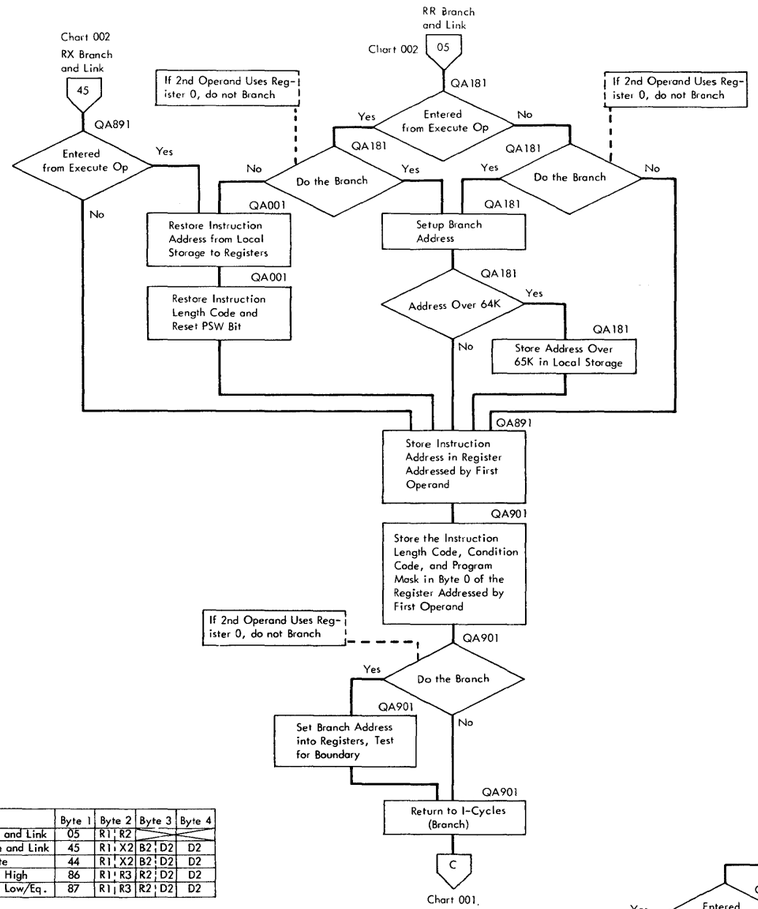
Subtract - The second operand is subtracted from the first operand, and the difference is placed in the first operand location.

Subtract Log. - Same as Subtract. The difference is in the setting of the condition code.

Compare - The first operand is compared with the second operand, and the result determines the setting of the condition code.







Op Format	Byte 1	Byte 2	Byte 3	Byte 4
RR - Branch and Link	05	R1 ; R2		
RX - Branch and Link	45	R1 ; X2	B2 ; D2	D2
RX - Execute	44	R1 ; X2	B2 ; D2	D2
RS - Branch High	86	R1 ; R3	R2 ; D2	D2
RS - Branch Low/Eq.	87	R1 ; R3	R2 ; D2	D2

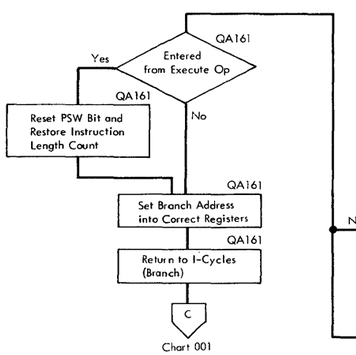
Objective:

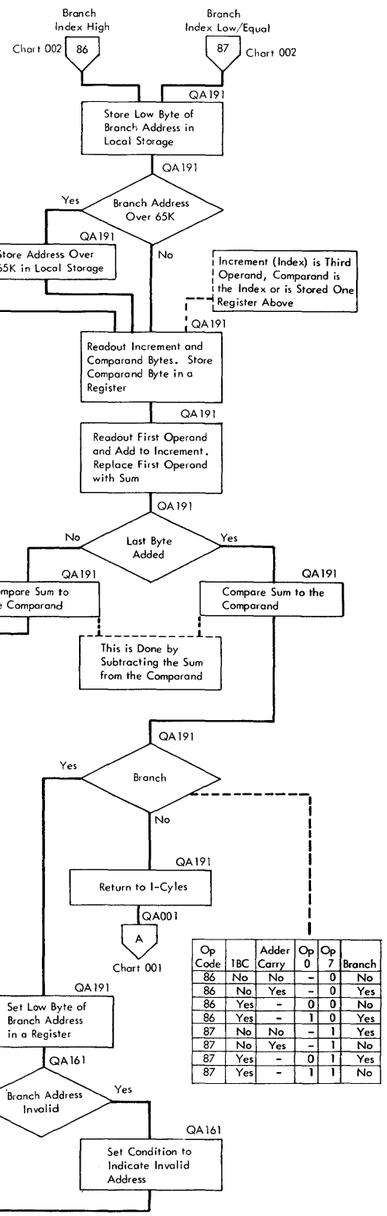
Branch and Link - Store the Updated Rightmost 32 Bits of the Current PSW and Set the Branch Address into the Instruction Counter.

Execute - Bits 8-15 of the Instruction at the Branch Address, Second Operand Effective Address, is Modified by ORING Byte 3 of R1 with Bits 8-15. The Instruction as Modified Will Now be Processed.

Branch High - Add the Contents of R3 to R1 and is Compared to the Contents of R3 or R3+1. If the Compare is High, a Branch is Taken to the Effective Address of the Second Operand.

Branch Low/Equal - Same as Branch High only Branch on Equal or Low Compare.





Op Code	IBC	Adder Carry	Op 0	Op 7	Branch
86	No	No	-	0	No
86	No	Yes	-	0	Yes
86	Yes	-	0	0	No
86	Yes	-	1	0	Yes
87	No	No	-	1	Yes
87	No	Yes	-	1	No
87	Yes	-	0	1	Yes
87	Yes	-	1	1	No

	1st Operand	Increment	Comparand
Start	00 00 02 04	00 00 00 60	00 00 02 12
Finish	00 00 02 64	00 00 00 60	00 00 02 12

Low Order Byte Address: 23, 43, 53

Readout Low-Order Bytes, Add A to C, Subtract Sum of A+C from B. Replace 1st Operand Byte with Sum of A + C.

1st Operand Address	Increment Address	Comparand Address	Register A	Register B	Register C	1st Operand
2 3	4 3	5 3	-	-	-	00 00 02 04
	Readout 4 3		6 0			
		Readout 5 3		1 2		
Readout 2 3				No Carry A E	0 4	00 00 02 64
2 2	4 2	5 2				

Readout Next Byte, Repeat Routine

	Readout 4 2		0 0		
		Readout 5 2		0 2	
Readout 2 2				No Carry F F	0 2 00 00 02 64
2 1	4 1	5 1			

Readout Next Byte, Repeat Routine

	Readout 4 1		0 0		
		Readout 5 1		0 0	
Readout 2 1				No Carry F F	0 0 00 00 02 64
2 0	4 0	5 0			

Readout Next (Last) Byte, Repeat Routine

	Readout 4 0		0 0		
		Readout 5 0		0 0	
Readout 2 0				No Carry F F	0 0 00 00 02 64

Check for a Carry from Bit 1 (in Example, Bit 1 Carry did not Occur)
Now Add High 4 Bits of the Last Compare, B-(A+C), to Op Code.

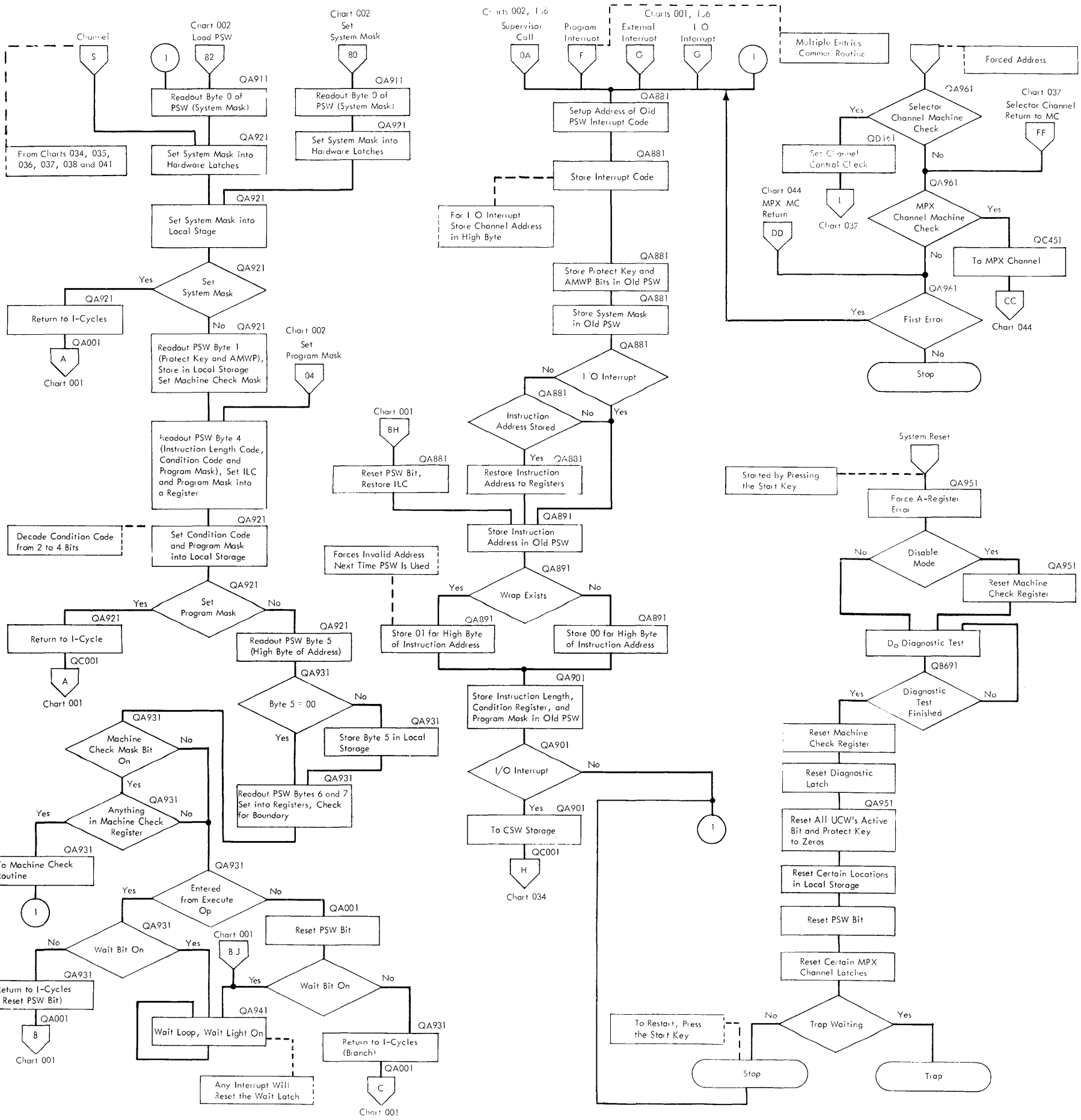
Branch High
86 = 1000 0110
1111 0110 No Carry ry

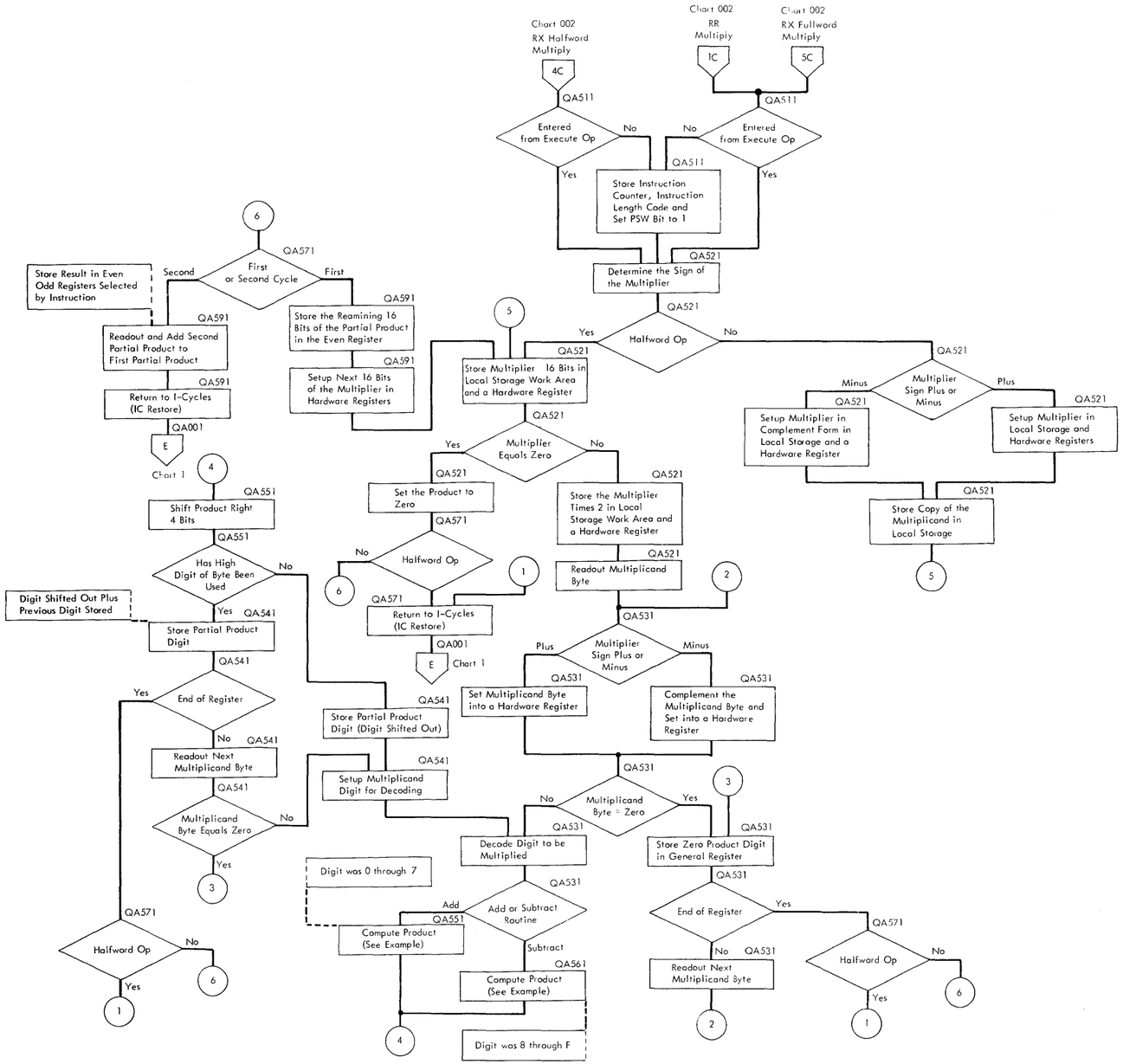
Adder Carry 0111 0110

Branch Low/Equal
87 = 1000 0111
1111 0000 No Carry

Adder Carry 0111 0111

Branches are Now Taken on Result of this Add, Adder Carry and Op Bit 7, to Determine if the Branch is to be Taken. If a Carry from Bit 1 had Occurred then the Branch is Determined by Op Bit 0 and Op Bit 7 after the Add.


Channel
S
From Charts 034, 035, 036, 037, 038 and 041
Chart 002 Load PSW
1
82
QA911
Readout Byte 0 of PSW (System Mask)
QA921
Set System Mask into Hardware Latches
Chart 002 Set System Mask
80
QA911
Readout Byte 0 of PSW (System Mask)
QA921
Set System Mask into Hardware Latches
QA921
Set System Mask into Local Stage
QA921
Set System Mask
Yes
QA921
Return to I-Cycles
QA001
A
Chart 001
No
QA921
Readout PSW Byte 1 (Protect Key and AMWP), Store in Local Storage Set Machine Check Mask
Chart 002 Set Program Mask
04
Readout PSW Byte 4 (Instruction Length Code, Condition Code and Program Mask), Set ILC and Program Mask into a Register
QA921
Decode Condition Code from 2 to 4 Bits
Set Condition Code and Program Mask into Local Storage
QA921
Set Program Mask
Yes
QA921
Return to I-Cycle
QC001
A
Chart 001
No
QA921
Readout PSW Byte 5 (High Byte of Address)
QA931
Byte 5 = 00
No
QA931
Store Byte 5 in Local Storage
Yes
QA931
Readout PSW Bytes 6 and 7 Set into Registers, Check for Boundary
QA931
Machine Check Mask Bit On
No
Yes
QA931
Anything in Machine Check Register
Yes
No
QA931
To Machine Check Routine
1
QA931
Entered from Execute Op
Yes
No
QA001
Reset PSW Bit
Chart 001
B J
QA931
Wait Bit On
No
Yes
QA931
Return to I-Cycles (Reset PSW Bit)
QA001
B
Chart 001
Yes
Wait Bit On
No
QA941
Wait Loop, Wait Light On
Any Interrupt Will Reset the Wait Latch
QA931
Return to I-Cycles (Branch)
QA001
C
Chart 001
Charts 002, 156
Supervisor Call
0A
Program Interrupt
F
Charts 001, 156
External Interrupt
C
I O Interrupt
G
1
Multiple Entries Common Routine
QA881
Setup Address of Old PSW Interrupt Code
QA881
Store Interrupt Code
For I O Interrupt Store Channel Address in High Byte
QA881
Store Protect Key and AMWP Bits in Old PSW
QA881
Store System Mask in Old PSW
QA881
I O Interrupt
No
Yes
QA881
Instruction Address Stored
No
Yes
QA881
Restore Instruction Address to Registers
Chart 001
BH
QA881
Reset PSW Bit, Restore ILC
QA891
Store Instruction Address in Old PSW
Forces Invalid Address Next Time PSW Is Used
QA891
Wrap Exists
Yes
No
QA891
Store 01 for High Byte of Instruction Address
QA891
Store 00 for High Byte of Instruction Address
QA901
Store Instruction Length, Condition Register, and Program Mask in Old PSW
QA901
I/O Interrupt
No
Yes
QA901
To CSW Storage
QC001
H
Chart 034
1
Forced Address
QA961
Selector Channel Machine Check
Yes
QD161
Set Channel Control Check
1
Chart 037
No
Chart 037 Selector Channel Return to MC
FF
QA961
MPX Channel Machine Check
Yes
Chart 044 MPX MC Return
DD
QC451
To MPX Channel
CC
Chart 044
No
QA961
First Error
Yes
No
Stop
System Reset
Started by Pressing the Start Key
QA951
Force A-Register Error
No
Disable Mode
Yes
QA951
Reset Machine Check Register
Do Diagnostic Test
QB691
Diagnostic Test Finished
Yes
No
Reset Machine Check Register
Reset Diagnostic Latch
QA951
Reset All UCW's Active Bit and Protect Key to Zeros
Reset Certain Locations in Local Storage
Reset PSW Bit
Reset Certain MPX Channel Latches
No
Trap Waiting
Yes
To Restart, Press the Start Key
Stop
Trap



Multiply Examples:

Multiply Table

Multiplicand Digit	Multiplier Value
0	+0
1	+1X
2	+2X
3	+2X +1X
4	+2X +2X
5	+2X +2X +1X
6	+2X +2X +2X
7	+2X +2X +2X +1X
8	-2X -2X -2X -2X
9	-2X -2X -2X -1X
A	-2X -2X -2X
B	-2X -2X -1X
C	-2X -2X
D	-2X -1X
E	-2X
F	-1X

This Same Table is Used for Add or Subtract. If the Last Cycle was a Subtract, Add One to the Multiplicand Digit.

RX Halfword Multiply

4C	R1	X2	B2	D2

Multiplier is 16 Bits
Multiplicand is 32 Bits
Product is 32 Bits

Operation is the Same as Fullword Except Only One Partial Product is Formed. The Low 32 Bits of This Product are Set into a Register as the Product.
R1 can be an Even or Odd Numbered Register.

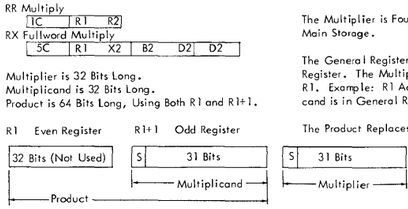
RR Multiply

1C	R1	R2

RX Fullword Multiply

5C	R1	X2	B2	D2	D2

Multiplier is 32 Bits Long.
Multiplicand is 32 Bits Long.
Product is 64 Bits Long, Using Both R1 and R1+1.



The Multiplier is Found in R2 or at the Effective Address in Main Storage.

The General Register Addressed by R1 must be an Even Number Register. The Multiplicand is Found in the Odd Register After R1. Example: R1 Addresses General Register 6, the Multiplicand is in General Register 7.

The Product Replaces the Multiplicand.

To do a Full Word Multiply, Two Partial Products are Developed, then Added together to Form the Product.
Example of Full Word Multiply. Multiplier = 00100024 Multiplicand = 00300904

1. Readout Multiplier, Complement if Minus. Put the High-Order 16 Bits into the 16 High-Order Bits of General Register Addressed by R1. Put Low-Order 16 Bits into Hardware Registers. Set a Copy of the Multiplicand into Local Storage.

R1	R1 + 1	Hardware Registers	Local Storage
00 10 XX XX	00 30 09 04	00 24	00 30 09 04
High 16 Bits of Multiplier	Multiplicand	Low 16 Bits of Multiplier	Copy of Multiplicand

2. Setup in Local Storage and Hardware Register 1 Times and 2 Times the Low 16 Bits of the Multiplier
   1X = 0024
   2X = 0048

3. Develop the First Partial Product by Reading Out the Multiplicand, Decoding each Digit and Adding or Subtracting the 1X or 2X of the Low Multiplier. The Product Digits Replace the Multiplicand and the Low-Order 16 Bits of the Even Register. Put High 16 Bits of the Multiplier in the Hardward Registers.

R1	R1 + 1	Hardware Registers
00 10 00 00	06 C1 44 96	0 0 | 1 0
High 16 Bits of Multiplier	First Partial Product	High 16 Bits of Multiplier

4. Setup in Local Storage and Hardware Registers 1 Times and 2 Times the Hihg 16 Bits of the Multiplier
   1X = 0010
   2X = 0020

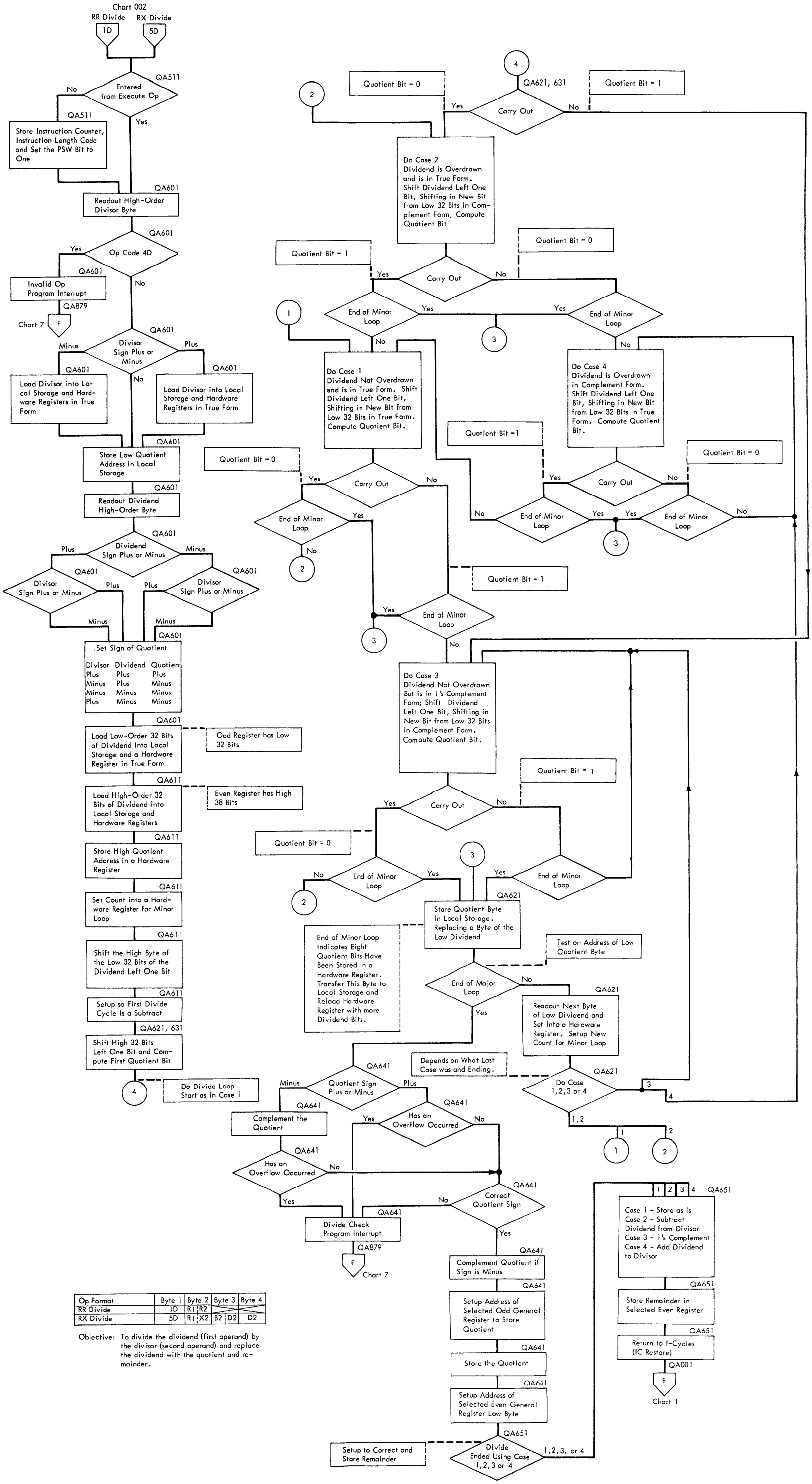
5. Develop the Second Partial Product by Reading Out the Copy of the Multiplicand, Decoding Each Digit and Adding or Subtracting the 1X or 2X of the High Multiplier. The Second Product Digits Replaces the Multiplicand Copy and the High 16 Bits are Stored in Hardware Registers.

Hardware Register	Local Storage
0 0 | 0 0	03 00 90 40
High 16 Bits of Second Partial Product.	Low 32 Bits of Second Partial Product.

6. Add the Second Partial Product to the First Partial Product. The Second Partial Product is Shifted the Correct Amount. Result is Set into the Even and Odd Registers Selected by R1.

```
  00 00 06 C1 44 96  First Partial Product
+ 00 00 03 00 90 40  Second Partial Product
```

R1	R1+1
00 00 03 00	97 01 44 96



Op Format	Byte 1	Byte 2	Byte 3	Byte 4
RR Divide	1D	R1 R2		
RX Divide	5D	R1 X2	B2 D2	D2

Objective: To divide the dividend (first operand) by the divisor (second operand) and replace the dividend with the quotient and remainder.

Note: For this example, assume a divisor of 16 bits and a dividend of 32 bits. This is done to shorten the example but still show how the quotient is developed.

1. Divisor = 10 52 — The divisor is readout of its General Register or Main Storage location and copied into Local Storage and a hardware register.

2. Signs. Check sign of divisor and dividend and set quotient sing. In example, both signs are plus, so the quotient sign is plus.

3. Dividend = 07 35 FB 0A (Even: 07 35; Odd: FB 0A) — The dividend is located in two General Registers. The high dividend in the even-numbered register and the low dividend in the odd-numbered register. The dividend is readout and the two parts, high and low, are copied into Local Storage and hardware registers.

4. Quotient. The quotient is developed 1 bit at a time and set into a hardware register until the end of a minor loop. Then it is placed in local storage.

Note: Shifting of the dividend uses the copy in local storage work area. The 4 low bits of a hardware register are set to F to be used in the minor loop count. When the 4 low bits equal 7, the minor loop is ended.

Note: Setup to start as in case 1.

5. Set high byte of low dividend into a hardware register.
6. Shift byte left 1 bit.

7. Add carry in high dividend, shift left 1 bit and do 1's complement.

8. Add complemented high dividend to divisor to compute quotient bit and new high dividend.
   Case 1, Carry out = Quotient bit 0 and do case 2.
9. Shift byte left 1 bit and set quotient bit in low-order position, subtract 1 from count.

10. Add carry in high dividend, shift left 1 bit.

11. Subtract dividend from divisor.

    Case 2, Carry out = Quotient bit 1 and do case 1.
12. Shift byte left 1 bit and set quotient bit in. Subtract 1 from count.

13. Add carry in high dividend, shift left 1 bit.

14. Subtract dividend from divisor.

    Case 1, No Carry = Quotient bit 1 and do case 3.
15. Shift byte left 1 bit and set quotient bit in. Subtract 1 from count.

16. Add carry in high dividend, Shift left 1 bit.

17. Add dividend to divisor.

    Case 3, No carry = Quotient bit 1 and do case 3.
18. Shift byte left 1 bit and set quotient bit in. Subtract 1 from count.

19. Add carry in high dividend, Shift left 1 bit.

20. Add dividend to divisor.

    Case 3, Carry out = Quotient bit 0 and do case 2.

21. Shift byte left 1 bit and set quotient bit in. Subtract 1 from count.

22. Shift high dividend left 1 bit.

23. Subtract dividend from divisor.

    Case 2, No Carry = Quotient bit 0 and do case 4.
24. Shift byte left 1 bit and set quotient bit in. Subtract 1 from count.

25. Add carry in high dividend, Shift left 1 bit.

26. Add dividend to divisor.

    Case 4, No Carry = Quotient bit 0 and do case 4.
27. Shift byte left 1 bit and set quotient bit in. Subtract 1 from count.

28. Add carry in high dividend, Shift left 1 bit.

29. Add dividend to divisor.

    Case 4, Carry out = Quotient bit 1 and do case 1.
30. Shift byte left 1 bit and set quotient bit in. Subtract 1 from count.

31. Count has gone to 7. End of minor loop. A quotient byte is in the hardware register. The quotient byte is set into local storage replacing the high byte of the low dividend copy. The low byte of the low dividend is placed in the hardware register for shifting and the count is set to F for the next minor loop.

32. Shift high dividend left 1 bit.

33. Subtract dividend from divisor.

    Case 1, Carry out = Quotient bit 0 and do case 2
34. Shift byte left 1 bit and set quotient bit in. Subtract 1 from count.

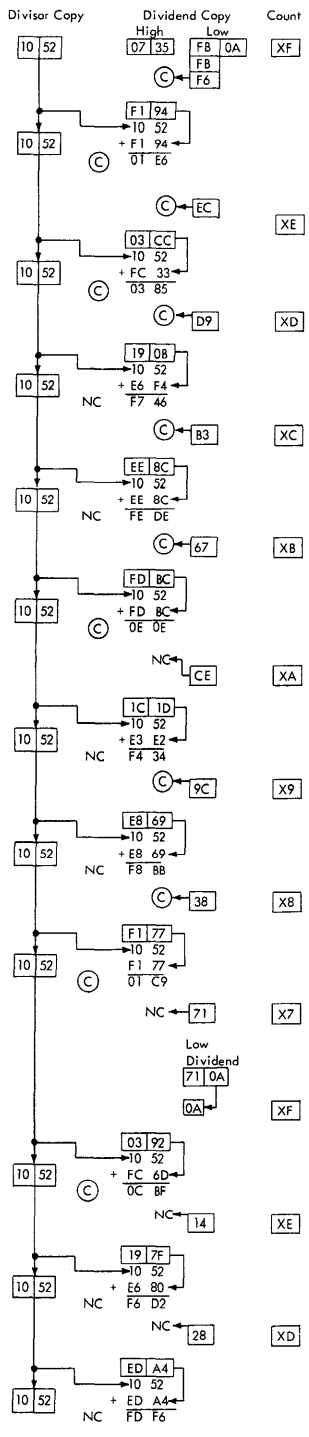
35. Shift high dividend left 1 bit.

36. Subtract dividend from divisor.

    Case 2, No Carry = Quotient bit 0 and do case 4.
37. Shift byte left 1 bit and set quotient bit in. Subtract 1 from count.

38. Shift high dividend left 1 bit.

    Case 4, No Carry = Quotient bit 0 and do case 4.



Do case 4.

40. Shift byte left 1 bit. Set quotient bit in and subtract 1 from count.

41. Shift high dividend left 1 bit.

42. Add dividend to divisor.

    Case 4, Carry out = Quotient bit 1 and do case 1.

43. Shift byte left 1 bit. Set quotient bit in and subtract 1 from count.

44. Shift highdivided left 1 bit.

45. Subtract dividend from divisor.

    Case 1, No Carry = Quotient bit 1 and do case 3.

46. Shift byte left 1 bit. Set quotient bit in and subtract 1 from count.

47. Shift high dividend left 1 bit.

48. Add dividend to divisor.

    Case 3, No Carry = Quotient bit 1 and do case 3,
49. Shift byte left 1 bit. Set quotient bit in and subtract 1 from count.

50. Shift high dividend left 1 bit

51. Add dividend to divisor.

    Case 3, Carry out = Quotient bit 0 and do case 2.
52. Shift byte left 1 bit, Set quotient bit in and subtract 1 from count.

53. Shift high dividend left 1 bit.

54. Subtract dividend from divisor

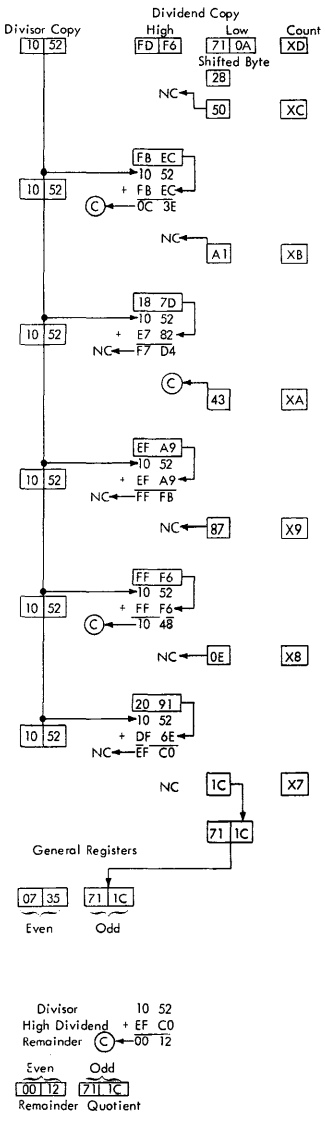
    Case 2, No Carry = Quotient bit 0 and do case 4.
55. Shift byte left 1 bit. Set quotient bit in and subtract 1 from count.
56. Count has gone to 7. End of minor loop. Set quotient byte into low byte of low dividend.
57. Address of low quotient byte has been reached indicating end of major loop. Check signs and set the quotient into the odd numbered general register.

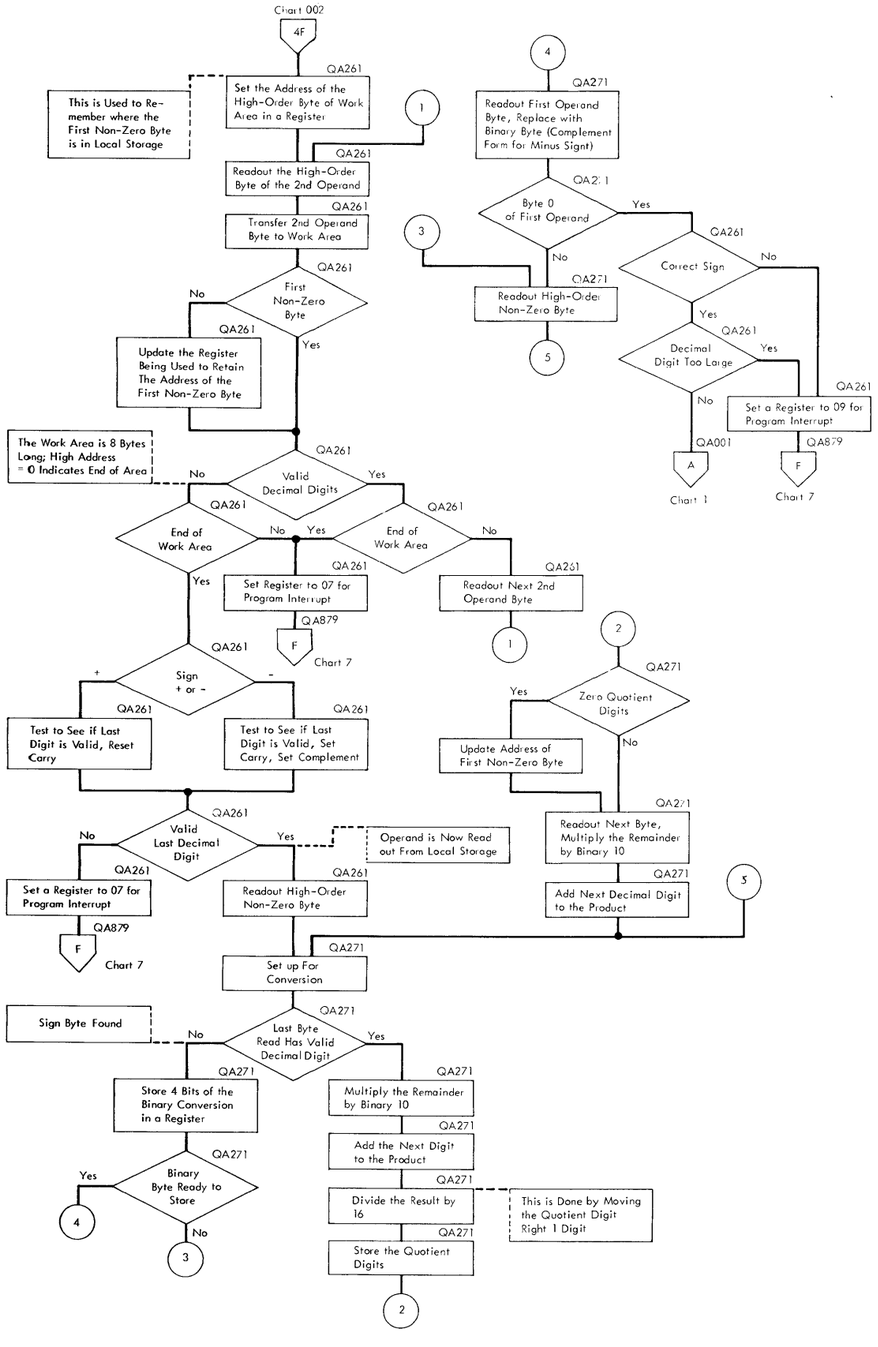
58. The remainder is developed and set into the even numbered general register. The correct sign is set for the reaminder. In the example, we ended in case 4. Case 4 causes the high dividend that has been developed to be added to the divisor. The result is the remainder.

The even/odd general registers have been set with the remainder and quotient with proper sign and divide is ended.

Note: The divisor and dividend in actual form would be:

Divisor	00	00	10	52					
Dividend	00	00	00	00	07	35	F8	0A	
The Quotient would be:					Even			Odd	
Quotient	00	00	00	12	00	00	71	1C	





Instruction

Format	Byte 0	Byte 1	Byte 2	Byte 3
RX	4F	R1 X2	B2	D 2

First Operand

Start	XX	XX	XX	XX
Finish	00	00	11	61

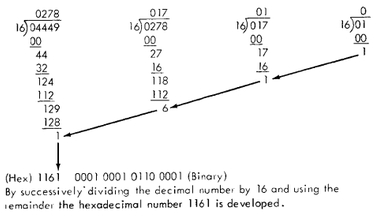
Second Operand - Main Storage

Byte	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Digits	00	00	00	00	00	04	44	9C

Work Area - Local Storage

Load	00	00	00	00	00	04	44	9C
Finish	00	00	00	00	00	00	00	0C

The convert to binary routine works something like a manual conversion of decimal to binary (hexadecimal). Example:



(Hex) 1161 0001 0001 0110 0001 (Binary)
By successively dividing the decimal number by 16 and using the remainder the hexadecimal number 1161 is developed.

The 2030 converts a decimal number to a binary number by multiplying each digit by binary 10 and then adding the next digit to the product. Then this result is divided by 16. The Quotient is stored and the Remainder is multiplied by 10. This continues until the number has been converted.

In the example to the right, the register numbers are for example only. The work area has been loaded and R4 has the location of the first high-order non-zero byte.

To multiply a digit by binary 10, shift the number left 3 times (by adding). Then add the result of the first shift to the third shift----
Examples:

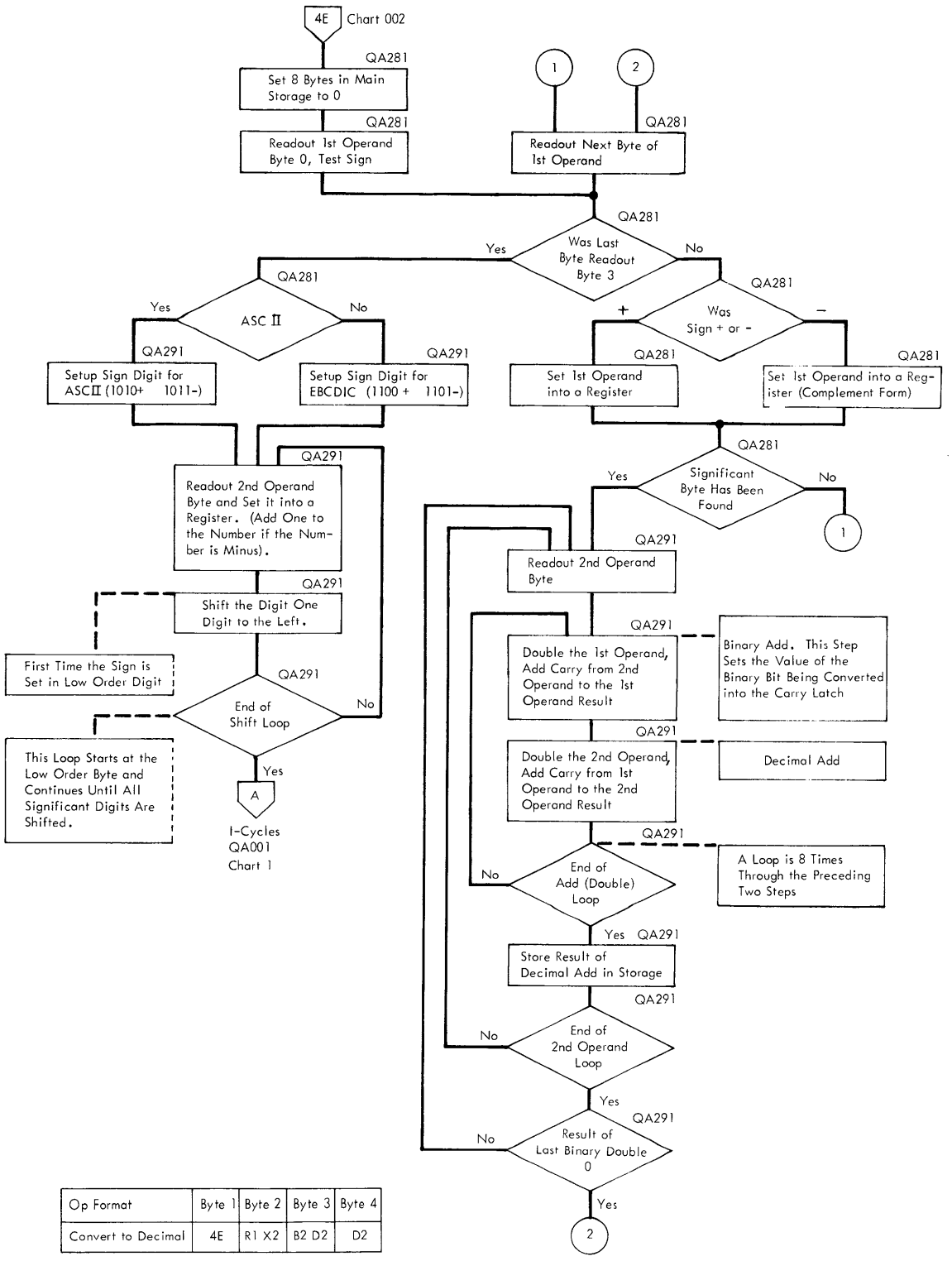
```
04  0000 0100
04 +0000 0100                1
08  0000 1000 ]
08  0000 1000 ]  2
16  0001 0000 ]
16  0002 0000 ]  3
32  0010 0000 ]
 8  0000 1000 ]
40  0010 1000
```

To divide a digit by 16, the digit is shifted 1 digit to the right.
Example:

```
 2        64 48 32 16  8 4 2 1
16)33      0  0  1  0  0 0 0 1 -- Remainder
32
 1                  0 0 1 0 -- Quotient
```

In Example R1, 2, and 3 are used to convert the number. R4 retains the work area byte with the first significant digit. R5 hold the low four bits of each convert byte for storing complete byte.

Comments	R1	R2	R3	Work Area Byte 5	Work Area Byte 6	Work Area Byte 7	R4	R5	First Operand Byte 1	First Operand Byte 2	First Operand Byte 3
Set R1 to 00 and set byte 5 in R2. Note: The R1 high digit is called Quotient (Q1) and the R1 low digit is called the Remainder.	00	04		04	44	9C	5		00	00	00
	Quotient / Remainder	1st / Next									
	00										
The R2 1st digit is added to the Remainder. Q1 2nd R2 next digit are set into R3. A test for sign digit is made. Multiply by 10 if the byte does not contain a sign digit.	-0										
	00		04								
	xA										
	00										
Add next digit to the product.	-4										
	04										
Divide by 16. This is done by shifting the high digit right 1 digit. Store Q1 and the Quotient (Q2) of this divide in the work area. If bytes stored equal zero, change R4.	0			00	44	9C	6				
Readout next byte. Multiply the Remainder by 10.	04	44									
	xA										
	28										
The Product and 1st digit are added. Q1 and next digit are set into R3. Test for sign.	+4										
	2C		24								
	0C										
Multiply remainder by 10.	xA										
	78										
Add next digit.	+4										
	7C										
Divide by 16, store Q1 and Q2, test for Zero.	7			00	27		6				
Readout next byte.	0C	9C									
Multiply Remainder by 10.	xA										
	78										
Add 1st digit.	+9										
Set the Quotient and next digit in R3, test for sign. Sign is found, set remainder in R5 and set R3 into low byte of work area.	81		8C								
				00	27	8C	6	1			
Set R1 to 00 and set byte 6 in R2	00	27		00	27	8C					
Add 1st digit to Remainder.	-2										
Set Q1 and next digit in R3, test for sign.	02		07								
Multiply Remainder by 10.	xA										
	14										
Add next digit.	+7										
Divide by 16, store Q1 and Q2, test for zero quotients.	1										
	0B	8C									
Readout next byte.	xA										
Multiply Remainder by 10.	67										
Add 1st digit.	x8										
Set the Quotient and next digit in R3, test for sign. Sign is found. Store the remainder and low digit in R5 in the First Operand byte 3, store R3 in the low byte of the work area.	76		7C						00	00	61
				00	01	8C	6				
Set R1 to 00 and set byte 6 in R2.	00	01									
Add 1st digit.	+0										
Set Q1 and next digit in R3, test for sign. multiply Remainder by 10.	00		01								
	xA										
	00										
Divide by 16, store Q1 and Q2, test for zero quotient.	+1										
Zeros found. Change R4.	01			00	00	7C	7				
Readout next byte.	0	7C									
Multiple Remainder by 10.	xA										
	0A										
Add 1st digit.	+7										
Set the Quotient and next digit in R3, test for sign. Sign is found. Set the Remainder in R5 and set R3 in low byte of the work area.	11		1C								
				00	00	1C		1			
Set R1 to 00 and set byte 7 in R2.	00	1C									
	+1										
Set Q1 and next digit in R3, test for sign. Sign is found. Store remainder and low digit in R5 in the First Operand byte 2, store R3 in low byte of the work area.	01		0C							00	11	61
				00	00	0C					
The number has been converted, but the loop continues until the first operand remaining bytes have been set to 00.											



Op Format	Byte 1	Byte 2	Byte 3	Byte 4
Convert to Decimal	4E	R1 X2	B2 D2	D2

First Operand

Byte 0	Byte 1	Byte 2	Byte 3
00	00	11	61

Second Operand

	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Zeroed	00	00	00	00	00	00	00	00
Added	00	00	00	00	00	00	44	49
Shifted	00	00	00	00	00	04	44	9C

To Manually Convert the Hexadecimal Number 1161 to Decimal, multiply each Digit by 16, then Add the Next Digit to the Product. The Sum is Multiplied by 16 and the Next Digit Added, etc.

Example:

```
01    1  6  1
x16
06
10
16
+1
17
x16
102
17
272
+ 6
278
x16
1668
278
4448
+  1
4449
```

The Operation in the 2030 is Similar to the Manual Operation. Each Byte is Doubled Eight Times. Whenever a Carry Occurs from the ALU During the Binary Add, it is Set into a Register and is Decimally Added to Itself. Any Carry during a Decimal Add is Added to the Result of the Next Binary Add. This Continues until the Binary Number is Converted to a Decimal Number. The Decimal Number is then Shifted Left One Digit so the Correct Sign can be Stored in the Low Order Digit of the Low Order Byte.

In the Example at the Right, the Register Numbers are for this Example Only. The 2nd Operand has been Set to all Zeros and the 1st Significant Byte of the 1st Operand is in R1. Note: RX is shown in Binary Form while RY and the 2nd Operand are shown in Decimal.

Carry	Binary Add Register X	Carry	Decimal Add Register Y	Storage - 8 Bytes 2nd Operand
	0001 0001		0 0	0000000000000000
	0001 0001			
	0010 0010		0 0	
			0 0	
	0010 0010			
	0100 0100		0 0	
			0 0	
	0100 0100			
	1000 1000		0 0	
			0 0	
	1000 1000			
1	0001 0000		0 0	
			1	
	0001 0000		0 1	
	0010 0000		0 1	
	0010 0000		0 2	
	0100 0000		0 2	
	0100 0000		0 4	
	1000 0000		0 4	
	1000 0000		0 8	
1	0000 0000		0 8	
			1	
			1 7	0000000000000017
	0000 0000			
	0000 0000			

End of Add Loop, End of 2nd Operand Loop, and Result of Binary Add 0
Readout Byte 3

	0110 0001		1 7
	0110 0001		
	1100 0010		1 7
			3 4
	1100 0010		
1	1000 0100		3 4
			1
	1000 0100		6 9
1	0000 1000		6 9
			1
	0000 1000	1	3 9
	1		
	0001 0001		3 9
			7 8
	0001 0001		
	0010 0010		7 8
	0010 0010	1	5 6
	1		
	0100 0101		5 6
	0100 0101	1	1 2
	1		
	1000 1011		1 2
	1000 1011		2 4
1	0001 0110		2 4
			1
			4 9	0000000000000049
	0001 0110			
	0010 1100			

End of Add Loop, Not the End of 2nd Operand Loop

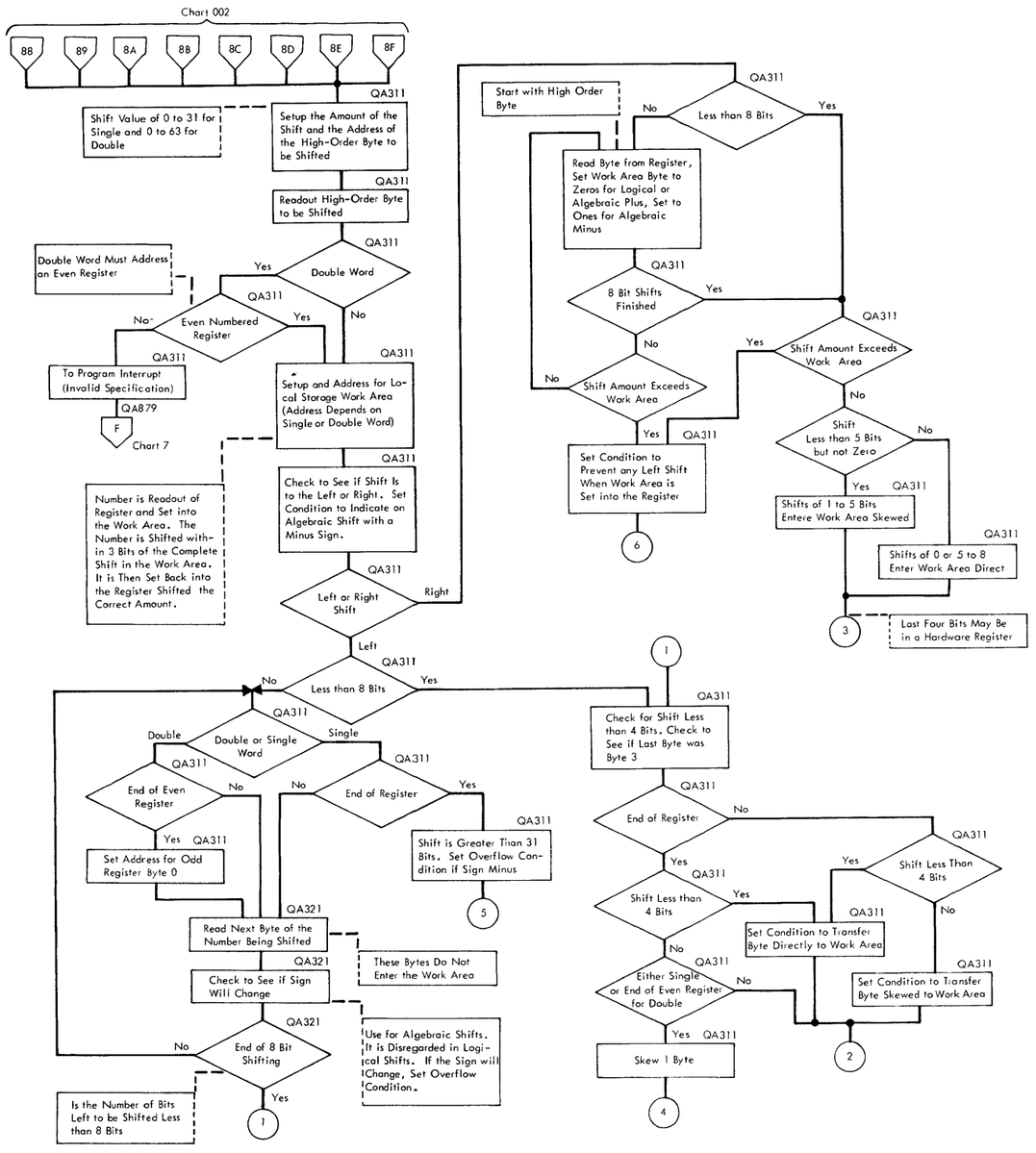
	0010 1100		0 0
	0010 1100		
	0101 1000		0 0
			0 0
	0101 1000		
	1011 0000		0 0
			0 0
	1011 0000		
1	0110 0000		0 0
			1
	0110 0000		0 1
	1100 0000		0 1
	1100 0000		0 2
1	1000 0000		0 2
			1
	1000 0000		0 5
1	0000 0000		0 5
			1
	0000 0000		1 1
	0000 0000		1 1
	0000 0000		2 2
	0000 0000		2 2
			4 4	0000000000004449
	0000 0000			
	0000 0000			

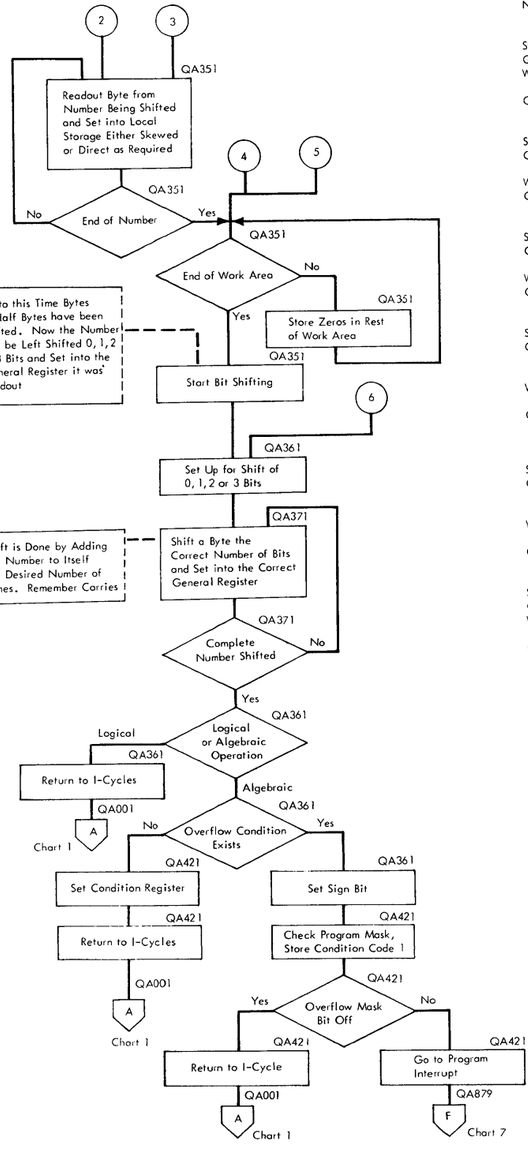
End of Add Loop, End of 2nd Operand Loop, and Result of Binary Add 0
Last Byte Read Out was Byte 3
Sign was Plus, not in ASCII Mode - Set Sign in R1
Note: Contents in the Register for the Rest of the Example are in Hexadecimal.

Register X	Register Y	Register Z	Storage
F C	4 9	4 9	0000000000004449
	9 C		000000000000449C
0 4			
	4 4	4 4	
0 4	4 4		000000000000449C
	0 0	0 0	
0 0	0 4		000000000004449C

End of Shift Loop

Set Sign in RX, RY to RZ;
RX Low to RY Low; RZ Low to RY High;
RZ High to RX Low;
RY to RZ, etc. until the Shift of the Decimal Number is Completed.





Note: All Examples Show a Single Word Shift.

Shift Left 3 Logical Single
General Register Start
Work Area
General Register Finished

0000 0000 0000 0000 0101 0110 0001 0010
0000 0000 0000 0000 0101 0110 0001 0010
0000 0000 0000 0010 1011 0000 1001 0000

Transfer to Work Area Direct.
Shift of 3 is Accomplished by Adding the Byte to Itself.
Three Times and Remembering Carries.

Shift Left 10 Algebraic +
General Register Start
Work Area
General Register Finished

0000 0000 0000 0001 0110 1000 0111 0001
0000 0001 0110 1000 0111 0001 0000 0000
0000 0101 1010 0001 1100 0100 0000 0000

Transfer to Work Area Direct but Shift 8 Bits.
Add on 1 Byte of Zeros.
Transfer Back to General Register, Shifted 2 Bits.

Shift Left 12 Algebraic -
General Register Start
Work Area
General Register Finished

1111 1111 1111 1111 1001 0010 1101 1011
1111 1001 0010 1101 1011 0000 0000 0000
1111 1001 0010 1101 1011 0000 0000 0000

Transfer to Work Area Skewed Shifted 12 Bits.
Add Low-Order Zeros.
Register Direct.

Shift Right 3 Logical Single
General Register Start
Work Area
General Register Finished

0000 0000 0000 0000 0101 0110 0001 0010
0000 0000 0000 0000 0000 0101 0110 0001
0000 0000 0000 0000 0000 1010 1100 0010

These Four Bits are held in a Hardware Register after First Shift.
Transfer to Work Area Skewed.
Low 4 Bits Shifted Out.
Add High-Order Zeros.
Transfer Back to General Register, Shifted 1 Bit.

Shift Right 12 Algebraic -
General Register Start
Work Area
General Register Finished

1111 1111 1111 1111 1001 0010 1101 1011
1111 1111 1111 1111 1111 1111 1111 1001
1111 1111 1111 1111 1111 1111 1111 1001

These Four Bits are held in a Hardware Register.
Transfer to Work Area Skiewed.
Shift 12 Bits.
Add High-Order Ones.

Shift Right 5 Logical Single
General Register Start
Work Area
General Register Finished

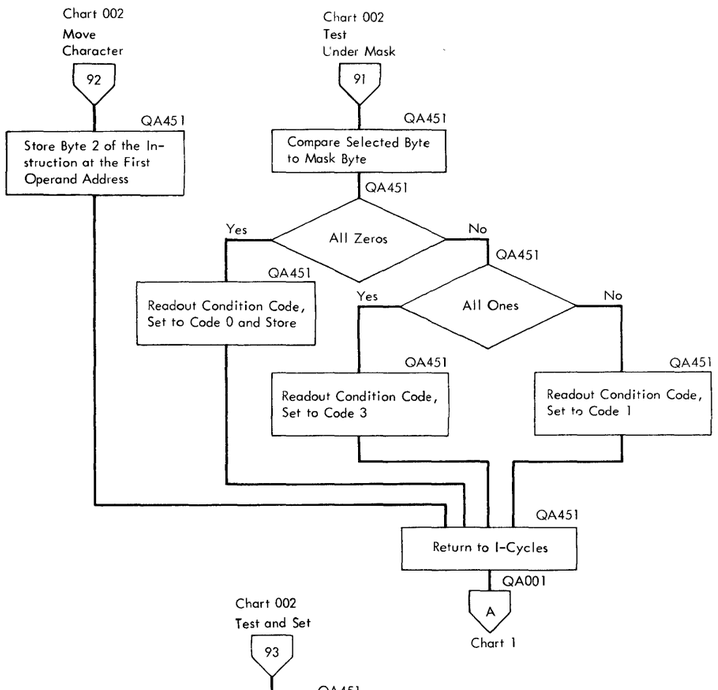
0000 0000 0000 1001 1110 0001 1010 1001
0000 0000 0000 0000 0000 1001 1110 0001
0000 0000 0000 0000 0100 1111 0000 1101

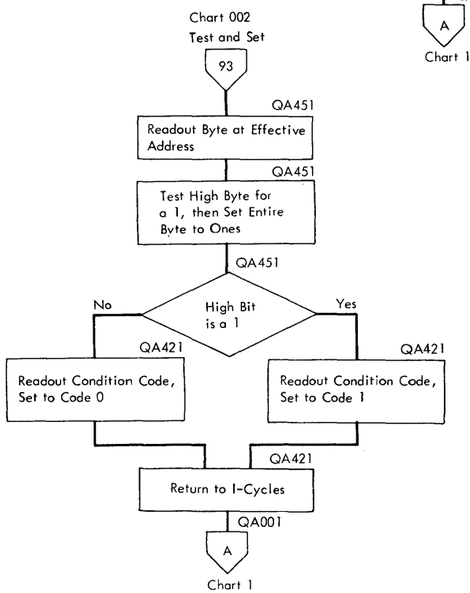
This Byte held in a Hardware Register.
Transfer to Work Area Direct but Shifted 8 Bits. Add High-Order Zeros.
Transfer Back to General Register. Shift Left 3 Bits. Three Low-Order Bits are Determined by Byte in Hardware Register.

Op Format	Byte 1	Byte 2	Byte 3	Byte 4
Right Single Log.	8 8	R1	B2 D2	D2
Left Single Log.	8 9	R1	B2 D2	D2
Right Single Alg.	8 A	R1	B2 D2	D2
Left Single Alg.	8 B	R1	B2 D2	D2
Right Double Log.	8 C	R1	B2 D2	D2
Left Double Log	8 D	R1	B2 D2	D2
Right Double Alg	8 E	R1	B2 D2	D2
Left Double Alg	8 F	R1	B2 D2	D2

Objective:

Shifts - To Obtain a Binary Value of the Second Operand Effective Address Low Order Six Bits. Example - 001011 - 11. Then shift the First Operand Either Left or Right that Amount. If the Shift is Algebraic, the Condition Code is Set.





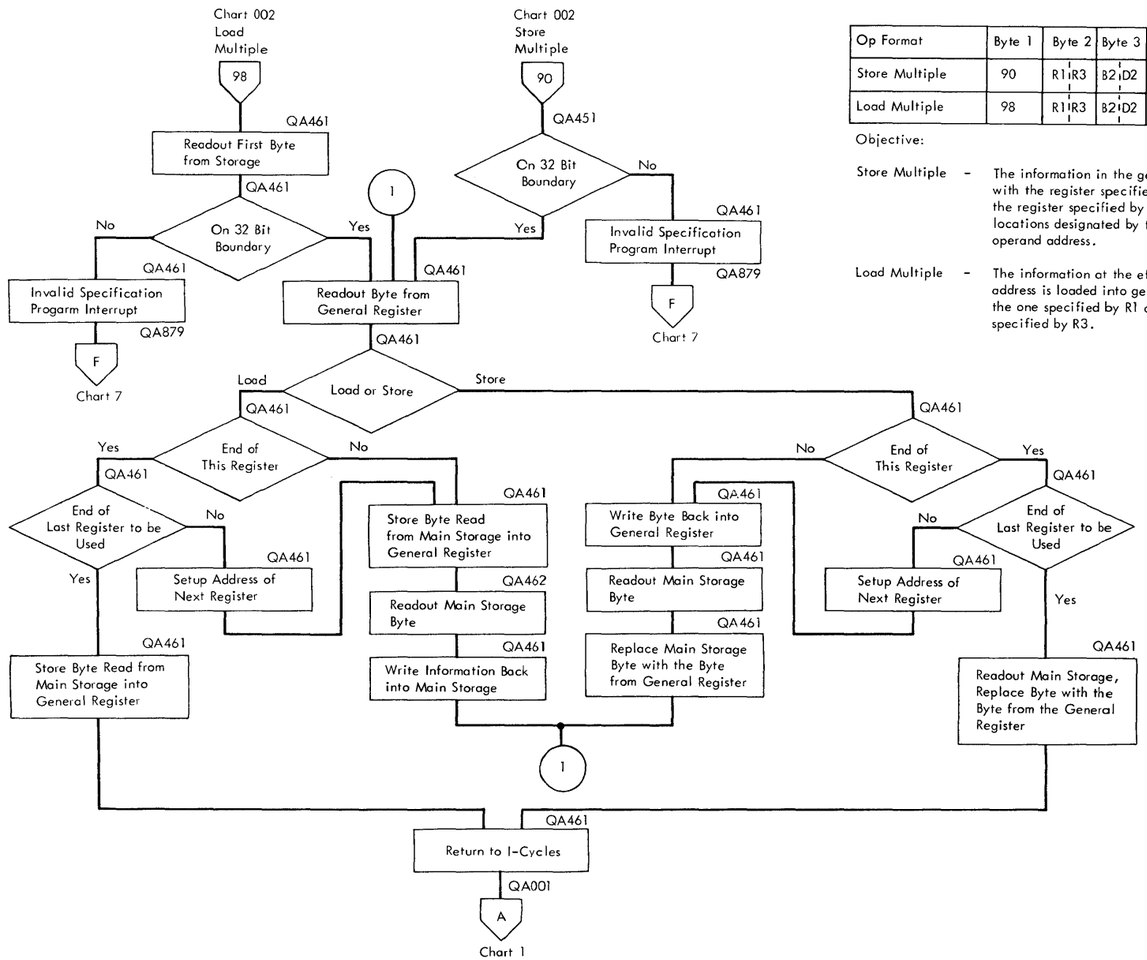
Op Format	Byte 1	Byte 2	Byte 3	Byte 4
SI Test and Set	91	I2	B1 D1	D1
SI Test Under Mask	92	I2	B1 D1	D1
SI Move Character	93	I2	B1 D1	D1

Objective:

Test and Set – Test the high-order bit of the byte at the effective address and set condition code.

Test Under Mask – The byte of immediate data, I2, is used as a eight-bit mask. The bits of the mask are made to correspond one for one with the bits of the byte in storage specified by the first operand effective address.

Move Character – The second operand, one eight-bit byte, is placed at the effective address of the first operand.



Op Format	Byte 1	Byte 2	Byte 3	Byte 4
Store Multiple	90	R1 R3	B2 D2	D2
Load Multiple	98	R1 R3	B2 D2	D2

Objective:

Store Multiple – The information in the general register starting with the register specified by R1 and ending with the register specified by R3 is stored at the locations designated by the effective second operand address.

Load Multiple – The information at the effective second operand address is loaded into general register starting with the one specified by R1 and ending with the one specified by R3.

Op Format	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
SS AND	D4	L	B1 D1	D1	B2 D2	D2
SS Compare	D5	L	B1 D1	D1	B2 D2	D2
SS OR	D6	L	B1 D1	D1	B2 D2	D2
SS Exclusive OR	D7	L	B1 D1	D1	B2 D2	D2

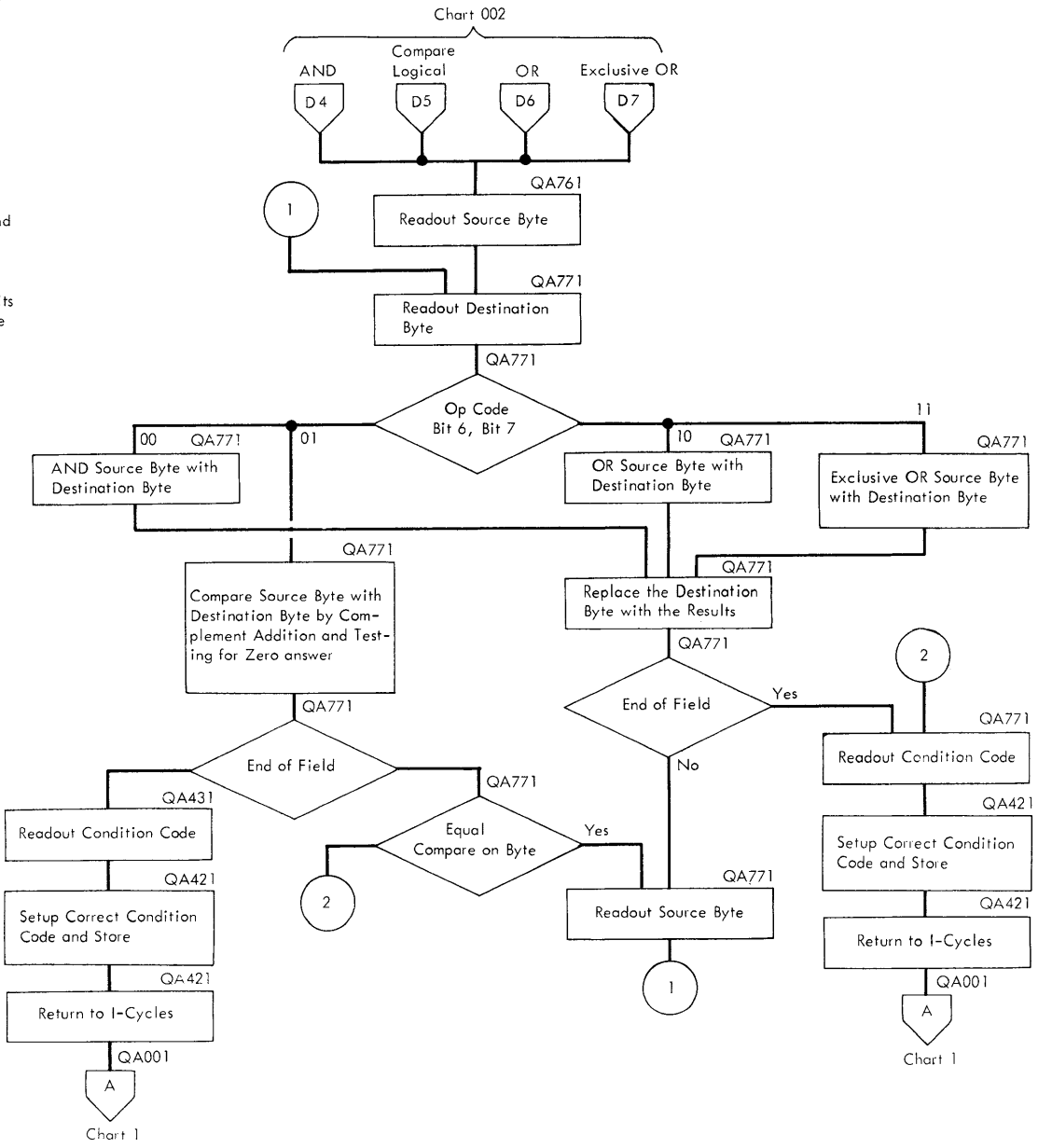
Objective:

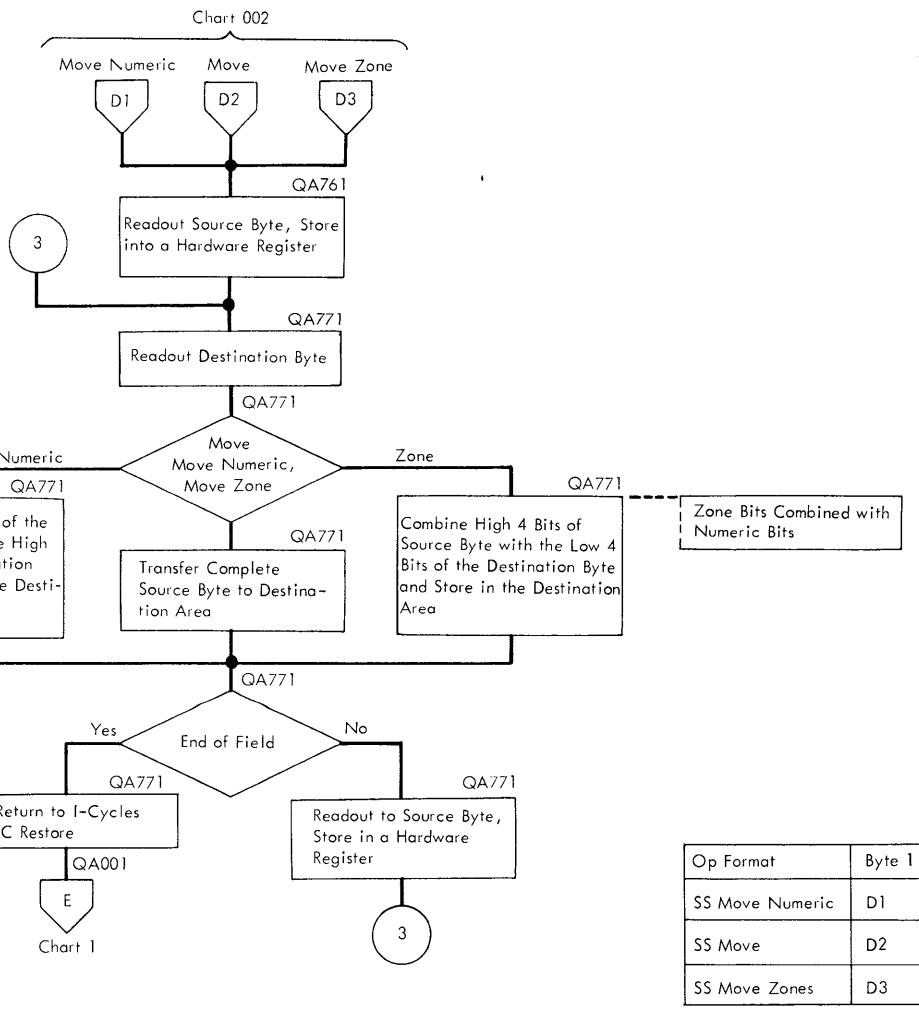
And - The logical answer (AND) of the bits of the first and second operand is placed in the first operand location.

Compare Logical - The first operand is compared with the second operand, and the result is indicated in the condition code.

OR - The logical sum (OR) of the bits of the first and second operand is placed in the first operand location.

Exclusive OR - The modulo - two sum (exclusive OR) of the bits of the first and second operand is placed in the first operand location.





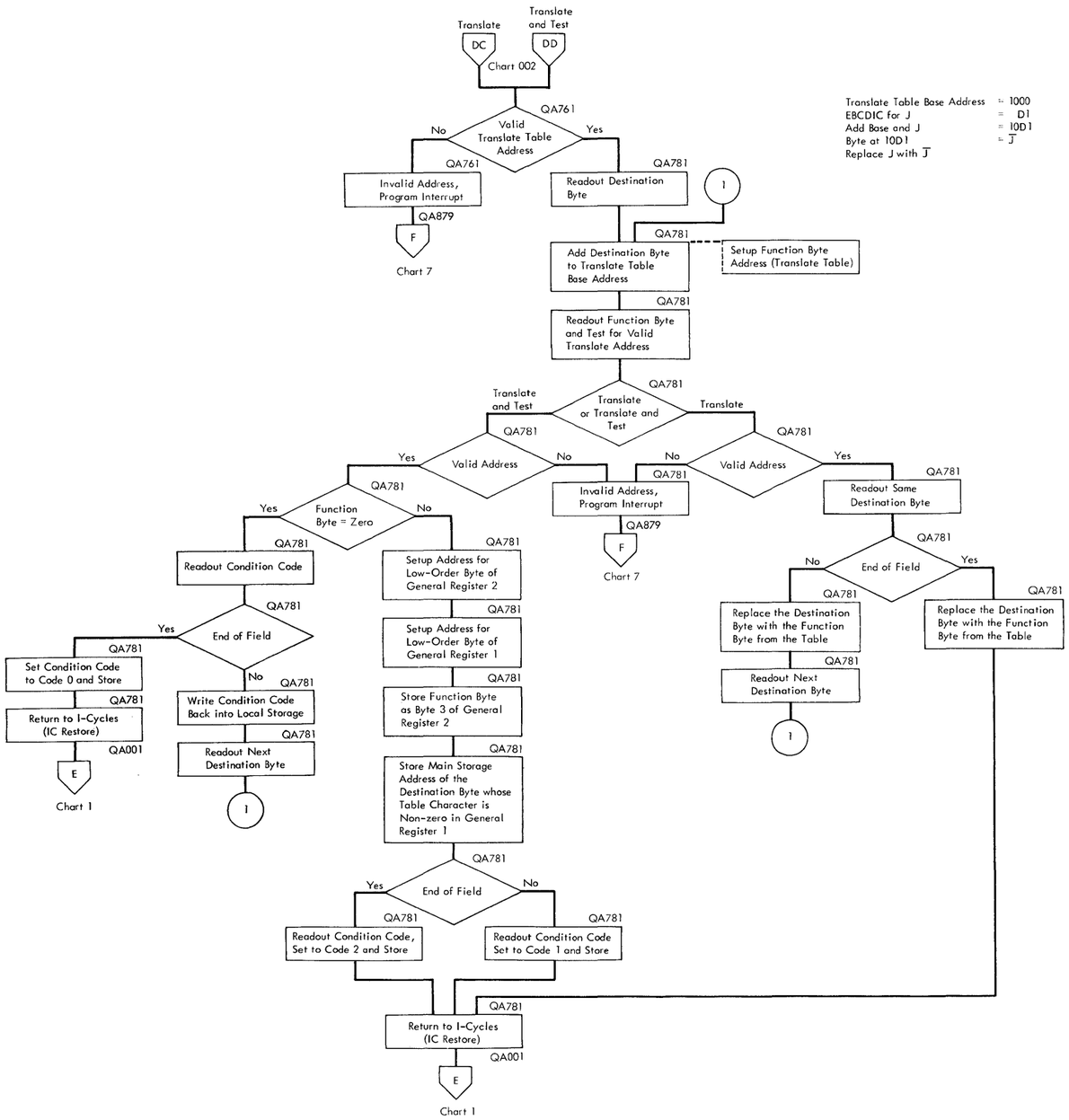
Op Format	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
SS Move Numeric	D1	L	B1 D1	D1	B2 D2	D2
SS Move	D2	L	B1 D1	D1	B2 D2	D2
SS Move Zones	D3	L	B1 D1	D1	B2 D2	D2

Objectives:

Move Numeric - The low-order four bits of each byte in the second operand field are placed in the low-order bit positions of the corresponding bytes in the first operand field. Movement is storage to storage, left to right.

Move - The second operand is placed in the first operand location. Movement is storage to storage, left to right.

Move Zones - The high-order four bits of each byte in the second opeand field are placed in the high-order four bit postions of the corresponding bytes in the first operand field. Movement is storage to storage, left to right.



Translate Table Base Address = 1000
EBCDIC for J = D1
Add Base and J = 10D1
Byte at 10D1 = J
Replace J with J

Translate

Assume a stream of 20 characters comes into location 2100 in EBCDIC. Translate to ASCII.

Assume:

Reg 12	00 00 20 00
Reg 15	00 00 10 00
Loc 2100 - 2113 (before)	JOHN JONES 257 W. 95

The instruction is:

Op Code	L	B_1	D_1	B_2	D_2
TR	13	C	100	F	0

Loc 2100 - 2113 (after) JOHN JONES 257 W. 95
where the overbar means the same graphic in ASCII
Condition code: unchanged

Translate Table

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
100X																
101X																
102X																
103X																
104X	BI											.	<	(	+	
105X	&											$	*	)		
106X		/										,	%			
107X												#	@			
108X		a	b	c	d	e	f	g	h	i						
109X		j	k	l	m	n	o	p	q	r						
10AX			s	t	u	v	w	x	y	z						
10BX																
10CX		A	B	C	D	E	F	G	H	I						
10DX		J	K	L	M	N	O	P	Q	R						
10EX			S	T	U	V	W	X	Y	Z						
10FX	0	1	2	3	4	5	6	7	8	9						

Op Format	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
SS Translate	DC	L	B1 D1	D1	B2 D2	D2
SS Translate and Test	DD	L	B1 D1	D1	B2 D2	D2

Objective:

Translate - The eight-bit bytes of the first operand are used as arguments to reference the list designated by the second operand address. Each eight-bit function byte selected from the list replaces the corresponding argument in the first operand.

Translate and Test - The eight-bit bytes of the first operand are used as arguments to reference the list designated by the second operand address. Each eight-bit function byte thus selected from the list is used to determine the continuation of the operation. When the function byte is a zero, the operation proceeds by fetching and translating the next argument byte. When the function byte is nonzero, the operation is completed by inserting the related argument address in general register 1, and by inserting the function byte in general register 2. The first operand is not changed.

Translate and Test

Assume that an assembly-language statement, located at 3000 - 3016, is to be scanned for various punctuation marks. A translate and test table is constructed with zeros in all positions except where punctuation marks are assigned.

Assume:

Reg 1 (before)	00 00 00 00
Reg 2 (before)	00 00 00 00
Reg 12	00 00 30 00
Reg 15	00 00 20 00
Loc 3000-3016	UNPK PROUT (9), WORD(5)

EBCDIC for (is 4D.

The instruction is:

Op Code	L	B_1	D_1	B_2	D_2
TRT	16	C	0	F	0

Reg 1 (after)	00 00 30 0B
Reg 2 (after)	00 00 00 20

Condition code = 1; scan not completed.

Translate and Test Table

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
200X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
201X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
202X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
203X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
204X	0	0	0	0	0	0	0	0	0	0	0	10	15	20	25	0
205X	0	0	0	0	0	0	0	0	0	0	0	30	35	40	45	0
206X	0	0	0	0	0	0	0	0	0	0	0	50	55	0	0	0
207X	0	0	0	0	0	0	0	0	0	0	0	60	65	70	75	0
208X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
209X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20AX	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20BX	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20CX	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20DX	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20EX	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20FX	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

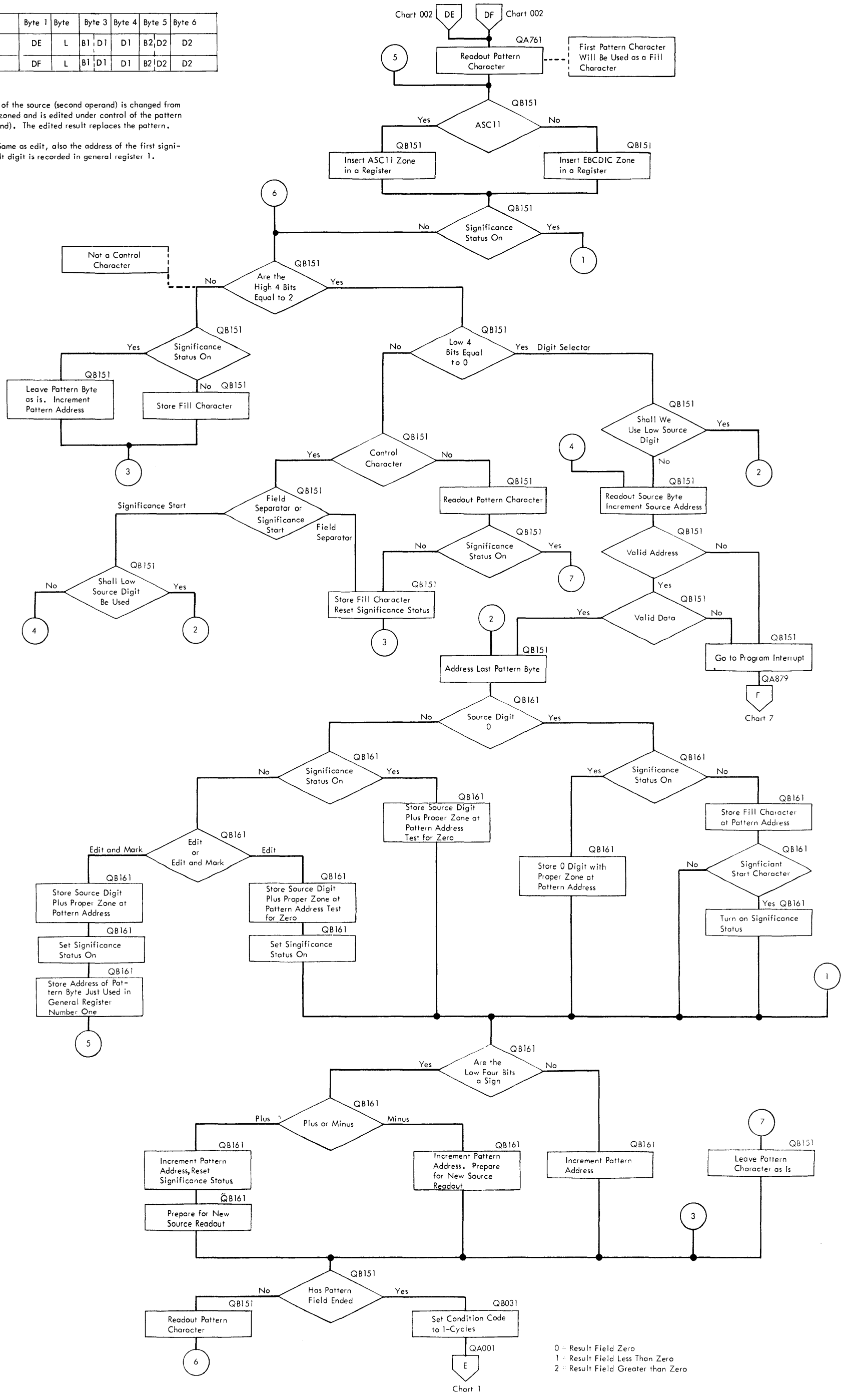
Note:
If all possible combinations of eight bits (i.e., 256 combinations) cannot appear in the statement being scanned, then a table less than 256 bytes can be used.

Op Format	Byte 1	Byte	Byte 3	Byte 4	Byte 5	Byte 6
SS Edit	DE	L	B1 D1	D1	B2 D2	D2
SS Edit and Mark	DF	L	B1 D1	D1	B2 D2	D2

Objective:

Edit - The format of the source (second operand) is changed from packed to zoned and is edited under control of the pattern (first operand). The edited result replaces the pattern.

Edit and Mark - Same as edit, also the address of the first significant result digit is recorded in general register 1.



Edit, and Edit and Mark

The format of the source (second operand) is changed from packed to zoned and is edited under control of the pattern (first operand). The edited result replaces the pattern.

The Edit and Mark also performs the operation of storing the byte address of the first significant digit. The address is not inserted when significance is forced by the significance start character of the pattern.

pattern field	b	d	d	,	d	d	(	.	d	d	b	C	R
source field	0 2	5 7	4 2	6 +									

1. Read out pattern character. Retain as fill character and store back into pattern field.

   Pattern Character b

b

2. Read out next pattern character. Decoded as digit select. Read out source byte. High digit 0 significance status is still off, store fill character in pattern field.

   Pattern Character d
   Source Byte 0 2

b	b

3. Read out next pattern character. Decoded as digit select. Low source digit significant, insert proper zone and store at pattern digit location.
   Turn on significance status.

   Pattern Character d

   Edit and Mark operation would store the address of this significant digit into General register number one.

b	b	Zone 2

4. Read out next pattern character. Decoded as non control character, leave as is because significance status on.

   Pattern character,

b	b	Zone 2	,

5. Read out next pattern character. Decoded as digit select. Read out source byte, store high source digit with proper zone at pattern digit location.

   Pattern character d
   Source Byte 5 7

b	b	Zone 2	,	Zone 5

6. Read out next pattern character. Decoded as digit select. Use low source digit of last source byte, insert proper zone and store at pattern digit location.

   Pattern Character d

b	d	Zone 2	,	Zone 5	Zone 7

7. Read out next pattern character. Decoded as significance start. Significance start status is on already, this character performs like the digit select. Read out next source byte. Store high source digit with proper zone, at pattern digit location.

   Pattern Character (
   Source Byte 4 2

b	b	Zone 2	,	Zone 5	Zone 7	Zone 4

8. Read out next pattern character. Decode as non control type. Leave as is. Read out next pattern character, digit select, store low source digit with zone at pattern digit location.

b	b	Zone 2,	,	Zone 5	Zone 7	Zone 4	.	Zone 2

9. Read out next pattern character, digit select. Read out source byte. This byte contains plus sign, turn off significance status. If sign had been minus, significance status would have been left on. Store high source digit with proper zone at pattern digit location. Store fill characters for remainder of field.

   source byte 6 +

   Edited field replacing pattern field

b	b	Zone 2	,	Zone 5	Zone 7	Zone 4	.	Zone 2	Zone 6	b	b	b

Set condition register

0 = Result field is source
1 = Result field is less than zero
2 = Result field is greater than zero

Pack, Unpack, and Move with Offset.
None of These Instructions Check for
Valid Digits or Signs.

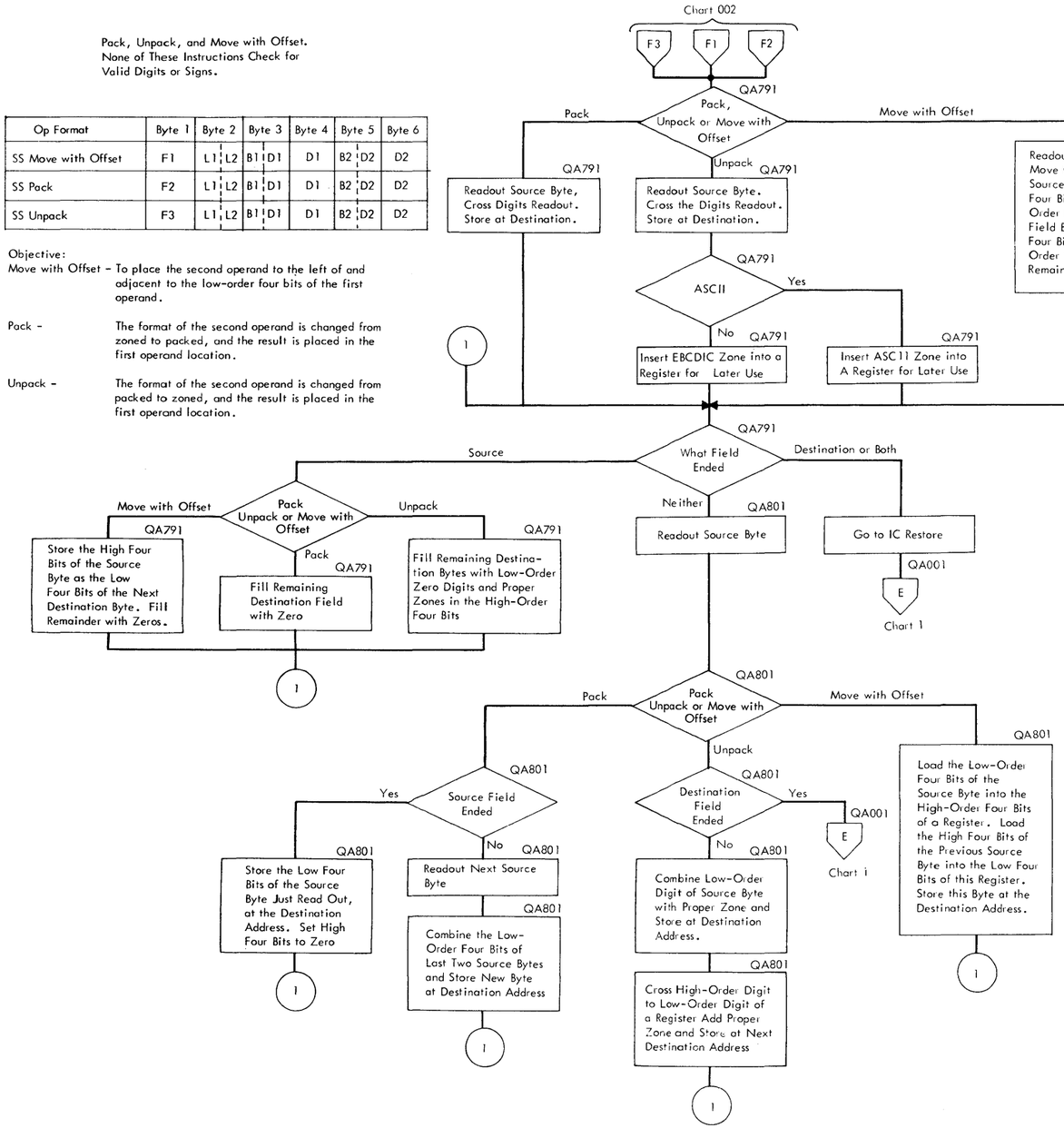
Op Format	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
SS Move with Offset	F1	L1 L2	B1 D1	D1	B2 D2	D2
SS Pack	F2	L1 L2	B1 D1	D1	B2 D2	D2
SS Unpack	F3	L1 L2	B1 D1	D1	B2 D2	D2

Objective:

Move with Offset - To place the second operand to the left of and adjacent to the low-order four bits of the first operand.

Pack - The format of the second operand is changed from zoned to packed, and the result is placed in the first operand location.

Unpack - The format of the second operand is changed from packed to zoned, and the result is placed in the first operand location.



Pack Instruction

	Zone 7	Zone 8	Zone 2	Zone 6	Sign 3
Source Field					
Destination Field		0 0	0 0	0 0	0 0

(1) Readout Low Source Byte. Cross Digits. Store at Destination Low Address. (Sign 3 → 3 Sign)					3 Sign
(2) Readout Next Two Source Bytes. Combine Low Order Digits. Store at Next Higher Destination Address. (Zone 2 → 2, Zone 6 → 6)				2 6	3 Sign
(3) Readout Next Two Source Bytes. Combine Low Order Digits. Store at Next Higher Destination Address. (Zone 7 → 7, Zone 8 → 8)			7 8	2 6	3 Sign
(4) Source Field Has Ended. Supply Zero's for Destination Field Until it Ends.	0 0		7 8	2 6	3 Sign

Unpack Instruction

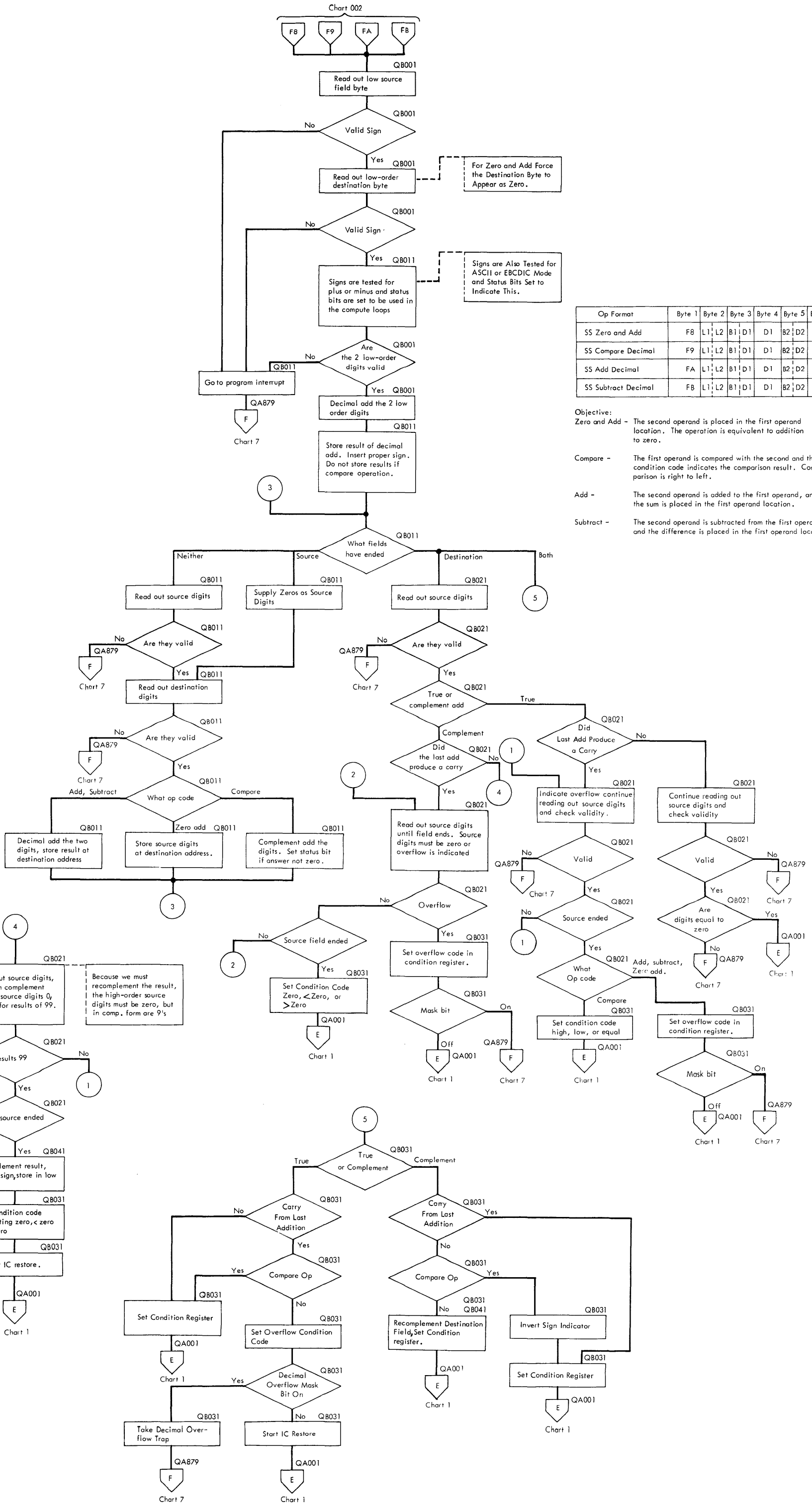
Source Field						6 4	9 2	5 Sign	
Destination Field	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	

(1) Readout Low-Order Source Byte. Cross and Store at Low Order Destination Address. (5 Sign → Sign 5)	0 0	0 0	0 0	0 0	0 0	0 0	0 0	Sign 5	
(2) Readout Next Source Byte. Combine Low-Order Digit with Proper Zone. Store at Destination. Cross High-Order Digit into Low Order of a Register. Read Register Out. Insert Proper Zone Store at Destination. (9 2 → Zone 2, 9)	0 0	0 0	0 0	0 0	0 0	0 0	Zone 2	Sign 5	
	0 0	0 0	0 0	0 0	0 0	Zone 9	Zone 2	Sign 5	
(3) Repeat Step 2. (6 4 → Zone 4, 6)	0 0	0 0	0 0	0 0	Zone 4	Zone 9	Zone 2	Sign 5	
	0 0	0 0	0 0	Zone 6	Zone 4	Zone 9	Zone 2	Sign 5	
(4) Source Ended, Supply Zero Digits with Proper Zones until Destination Ends. (Zone 0)	Zone 0	Zone 6	Zone 4	Zone 9	Zone 2	Sign 5			

Move with Offset

The Source Field is Moved to the Destination Field to the Left of the Low-Order Four Bits of the Destination. If the Destination Field Ends Before the Source Field, the Remaining Source Digits are Ignored.

Source Field	7 2	4 8	3 2	3 4	5 7			
Destination Field		9 2	8 7	5 4	6 Sign			
Destination Field		8 3	2 3	4 5	7 Sign			



Op Format	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
SS Zero and Add	F8	L1 L2	B1 D1	D1	B2 D2	D2
SS Compare Decimal	F9	L1 L2	B1 D1	D1	B2 D2	D2
SS Add Decimal	FA	L1 L2	B1 D1	D1	B2 D2	D2
SS Subtract Decimal	FB	L1 L2	B1 D1	D1	B2 D2	D2

Objective:

Zero and Add - The second operand is placed in the first operand location. The operation is equivalent to addition to zero.

Compare - The first operand is compared with the second and the condition code indicates the comparison result. Comparison is right to left.

Add - The second operand is added to the first operand, and the sum is placed in the first operand location.

Subtract - The second operand is subtracted from the first operand, and the difference is placed in the first operand location.

DECIMAL ADD, SUBTRACT EXAMPLE

Sign analysis is done first and will indicate if the operands will be true or complement added.

Eight conditions may occur as shown in the following table:

Operation	First Operand Sign	Second Operand Sign	True or Complement
Add	Plus	Plus	True
Add	Minus	Plus	Complement
Add	Minus	Minus	True
Add	Plus	Minus	Complement
Subtract	Plus	Plus	Complement
Subtract	Minus	Plus	True
Subtract	Minus	Minus	Complement
Subtract	Plus	Minus	True

After sign analysis, the operation for both add and subtract are the same.

Decimal Add

1st Operand = Destination field 0 4 6 +
2nd Operand = Source field 0 0 1 3 4 -

1. Read out low source byte. 4 -
2. Read out low destination byte. 6 +

3. Decimal add the digits.
   Complement add indicated.

```
        6
      @5   9's complement of 4
        1   Insert carry
Carry (c)←2  Converts 9's complement to 10's complement
```

   Insert Destination Sign. Intermediate sum = 2 +
   1 Carry from previous cycle

4. Read out source digits. 04
   Read out destination digits. @86 9's complement of destination byte.
   Complement add. NC 91

5. Destination field ended. Intermediate sum 9 1 2 +
   There was no carry from high-order significant addition, indicating recomplementing will be necessary.

6. Read out source digits. 00
   Complement add to zero. @99
   9's must result or overflow will be indicated. 99

7. Source field ended, recomplement answer and change sign. Intermediate sum 9 9 9 1 2 +
   Result stored in destination field 0 8 8 -

Cases when the source field is longer than the destination and a complement addition is being performed.

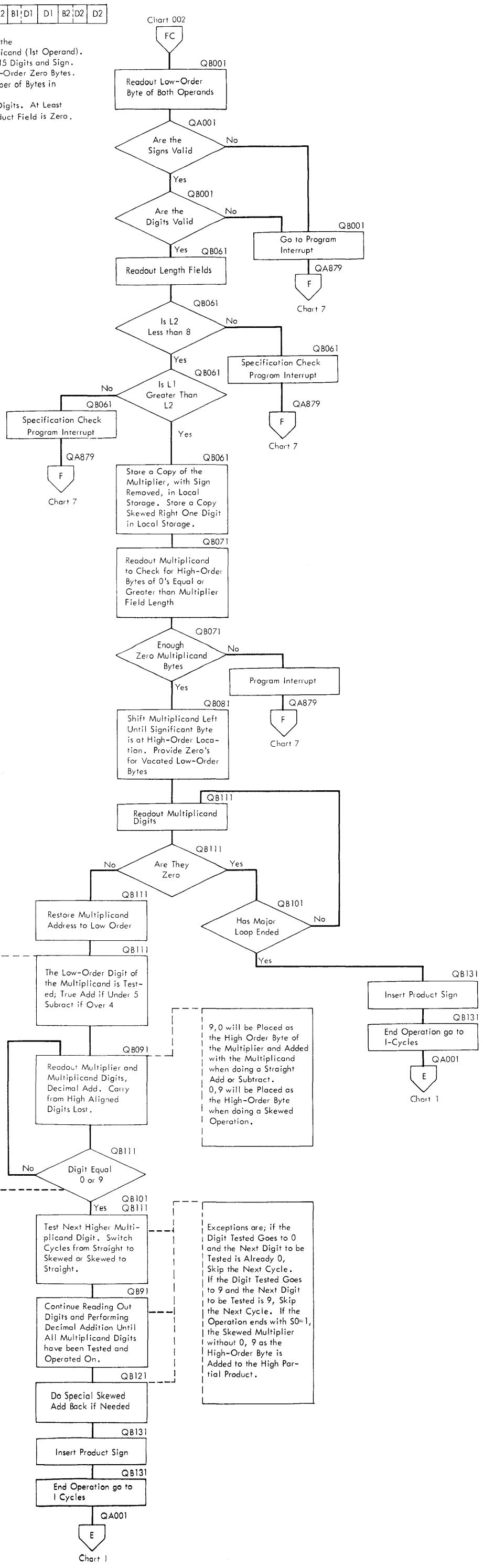
1. Destination ends and no carry results from last addition; all further adds must produce 9's or an overflow results.
2. Destination ends, with a carry resulting from last addition:
   The answer produced so far is zero and all further adds must produce zeros.
   The answer produced so far is not zero; examine carry from the addition following the one in which the destination ended. If there was a carry, the result just produced must be zero; if there was no carry, the result just produced must be 9's. In either case, all further cycles must produce the same result as the first.

When doing a true add, all cycles after the destination field ends must produce zeros.
Overflow when doing a complement add causes a recomplement, then a branch to overflow case when setting condition register.
Overflow when doing a true add forces overflow when setting condition register.

Condition Code
0 = Result is zero
1 = Result less than zero
2 = Result greater than zero
3 = Overflow

SS Multiply Decimal	FC	L1	L2	B1	D1	D1	B2	D2	D2

The Product of the Multiplier and the Multiplicand Replaces the Multiplicand (1st Operand).
The Multiplier Size is Limited to 15 Digits and Sign.
The Multiplicand Must Have High-Order Zero Bytes Equal to or Greater than the Number of Bytes in the Multiplier Field.
The Maximum Product Size is 31 Digits. At Least One High-Order Digit of the Product Field is Zero.



Refer to multiply example for multiply loop.

Decimal Multiply

The product of the multiplier (second operand) and the multiplicand (first operand) replaces the multiplicand.
The multiplicand must have high-order zero digits for at least a field size equal to the multiplier field.

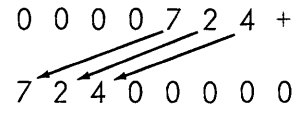
multiplicand	0 0 0 0 7 2 4 +
multiplier	3 4 6 +

1. Make 2 copies of the multiplier, with sign stripped out, into local storage. One copy straight and one copy skewed right.

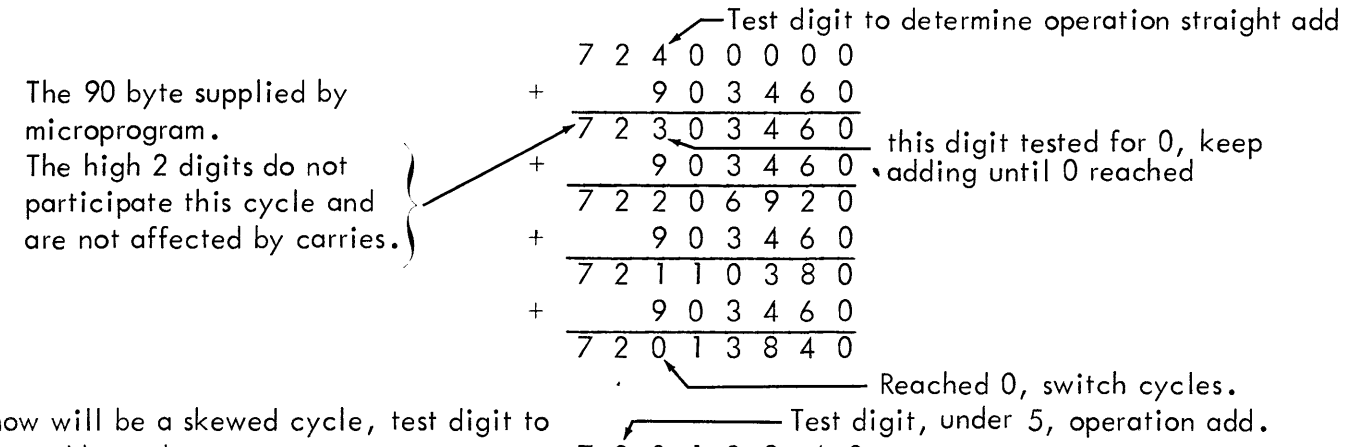
straight copy of multiplier	3 4 6 0
skewed copy of multiplier	0 3 4 6

2. Test for enought zeros in multiplicand field.

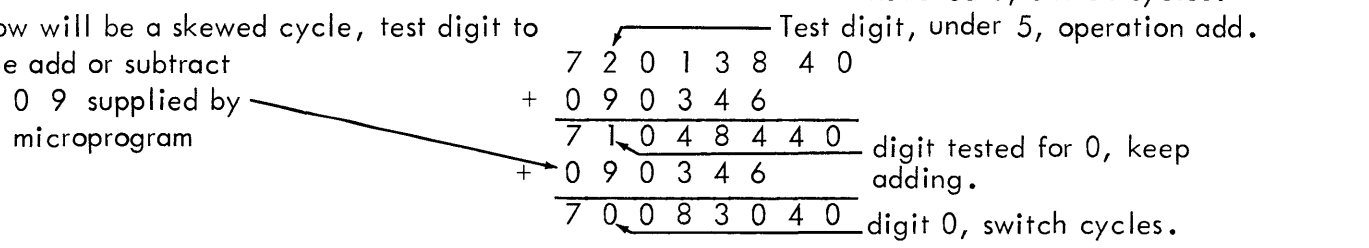
3. Move the most significant byte and following byes of the multiplicand to the high-order byte of the multiplicand. Supply zeros for vacated bytes, sign is stripped out.



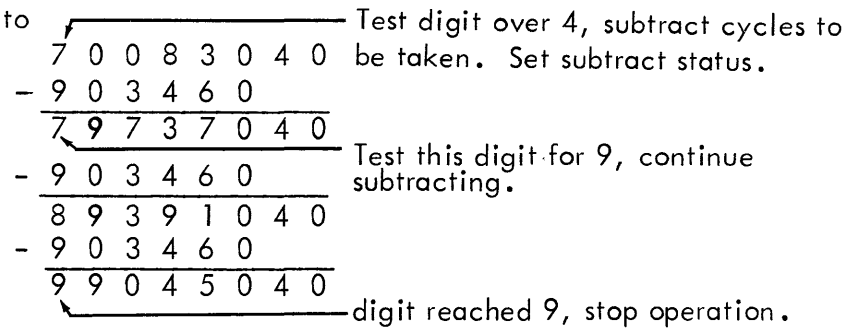
4. Start compute loop. First cycle will be a straight cycle. The first low significant digit of the multiplicand is tested. If over 4, a straight subtract will be done. If under 5, a straight true add will be done.



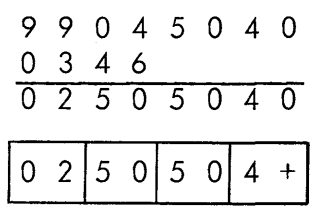
5. Cycle now will be a skewed cycle, test digit to determine add or subtract



6. Cycle now will be a straight cycle, test digit to determine add or subtract



7. Operation stopped with subtract status on; the skewed multiplier must be added to partial product to obtain correct product.



8. Insert sign and end operation
Product located in first operand location.

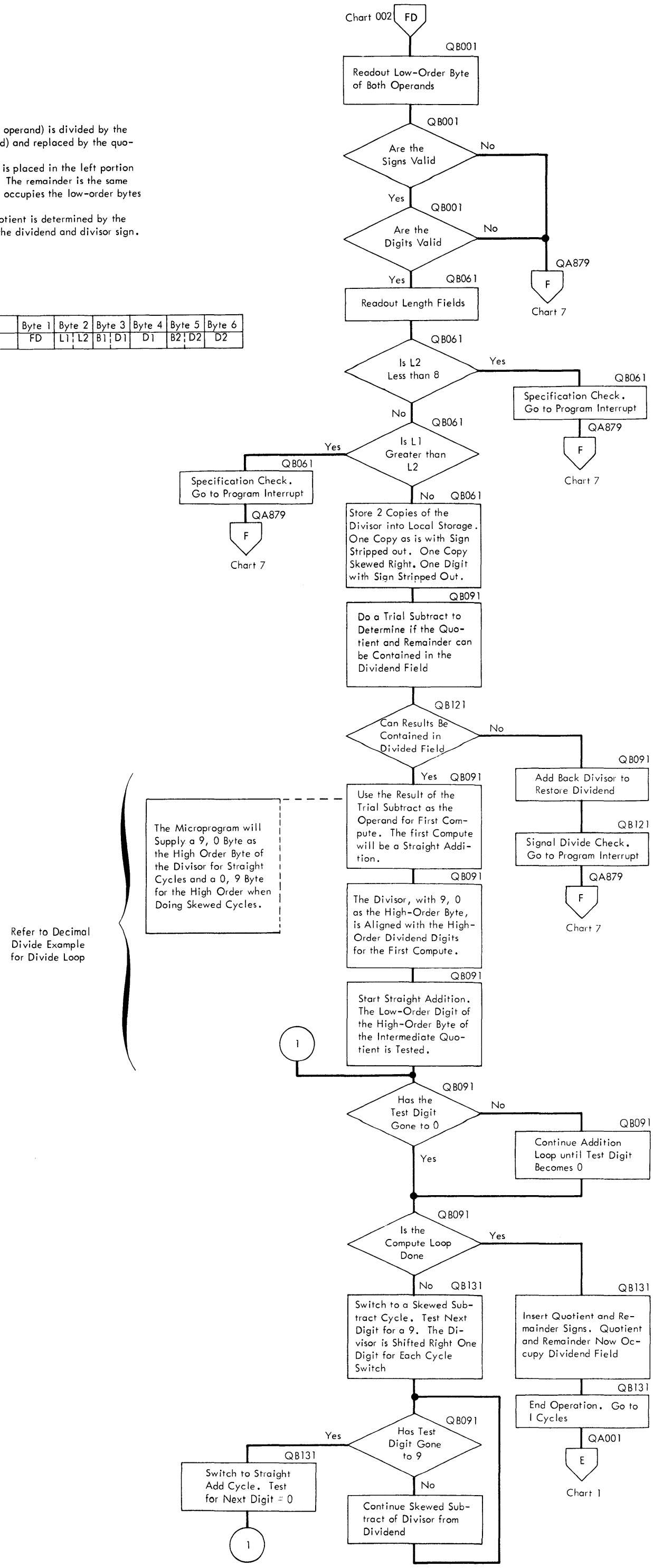
Decimal Divide

The dividend (first operand) is divided by the divisor (second operand) and replaced by the quotient and remainder.

The quotient field is placed in the left portion of the dividend field. The remainder is the same size as the divisor and occupies the low-order bytes of the dividend field.

The sign of the quotient is determined by the rules of algebra from the dividend and divisor sign.

Op Format	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
SS Divide Decimal	FD	L1 ¦ L2	B1 ¦ D1	D1	B2 ¦ D2	D2



Decimal Divide

The dividend (first operand) is divded by the divisor (second operand) and replaced by the quotient and remainder.

Dividend equal 0 1 2 3 5 6 8 +
Divisor equals 8 5 2 +

1. Copy divisor into local storage, with sign stripped out, in straight form and skewed right one digit.

8 5 2 0 straight
0 8 5 2 skewed

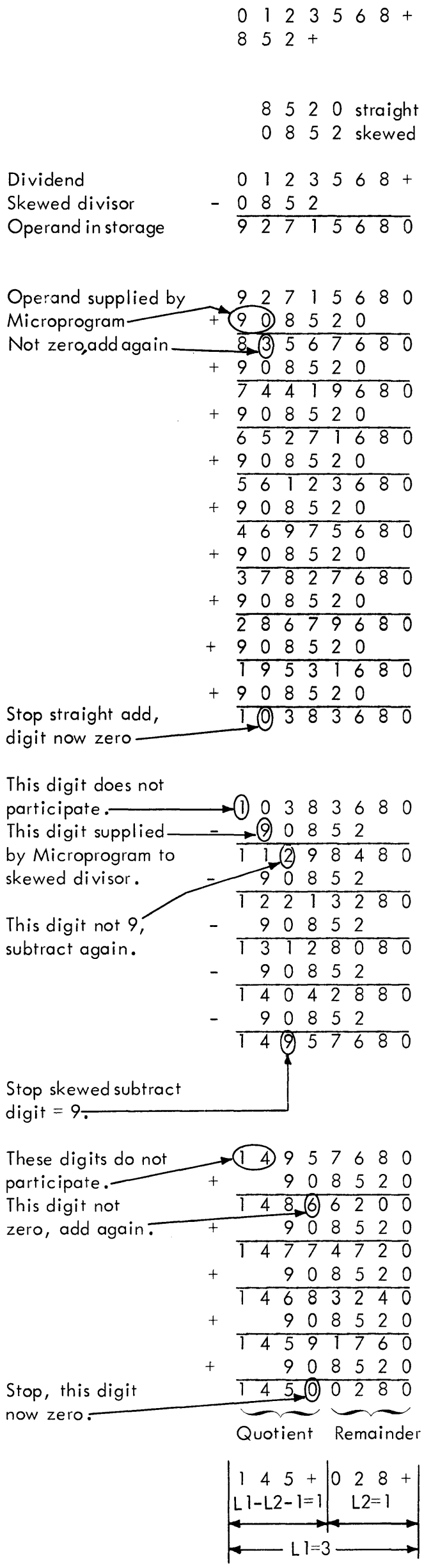
2. Setup data for trial subtract using skewed divisor. A carry out of the high-order position on the trial subtract would indicate a divide check. If divide check occurred, the skewed divisor is added back to restore dividend and a divide check taken.

3. Add straight divisor to operand in working storage until indicated digit goes to zero.

4. Subtract skewed divisor from result until indicated digit goes to nine.

5. Add straight divisor to result will indicated digit goes to zero.

6. Insert dividend sign into low-order 4 bits.
Insert quotient sign into low-order quotient 4 bits.
Quotient and remainder have now replaced dividend.

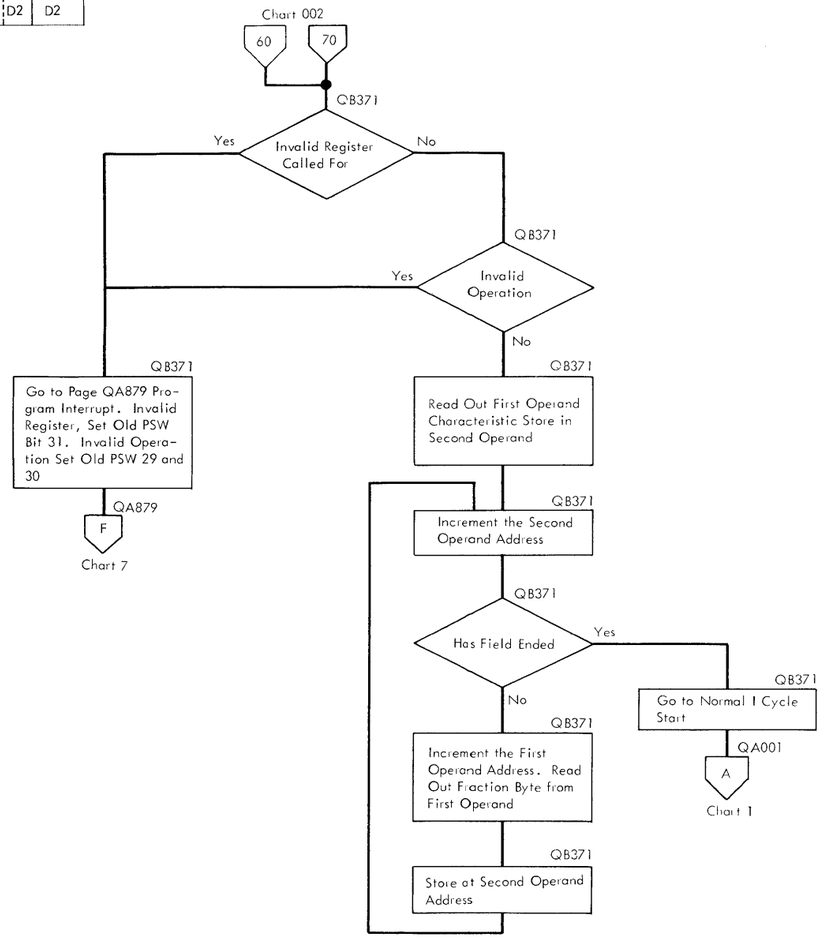


OP Format	Byte 1	Byte 2	Byte 3	Byte 4
RX FP Store Double	60	R1 X2	B2 D2	D2
RX FP Store Single	70	R1 X2	B2 D2	D2

Floating Point Store RX Format
Single and Double Precision.

Single Precision; the Low Order
Half of the First Operand
Register is Ignored.

Mnemoics
STD
STE

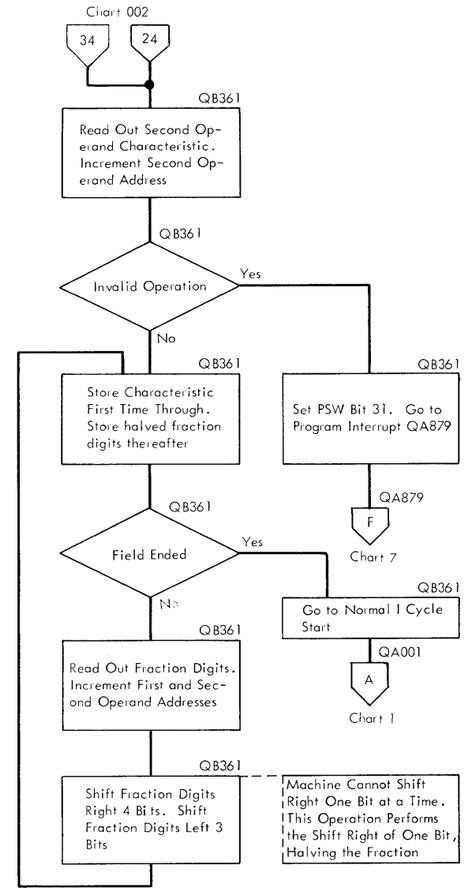


Op Format	Byte 1	Byte 2
RR FP Halve, Double	24	R1 R2
RR FP Halve, Single	34	R1 R2

Floating Point Halve RR Format
Single and Double Precision.
Single Precision, the Low Order
Half of the Result Register
Remains Unchanged.

The Second Operand is Divided
by 2 and the Quotient is
Placed in the First Operand
Location. Second Operand Sign
and Characteristic is Stored
without Change.

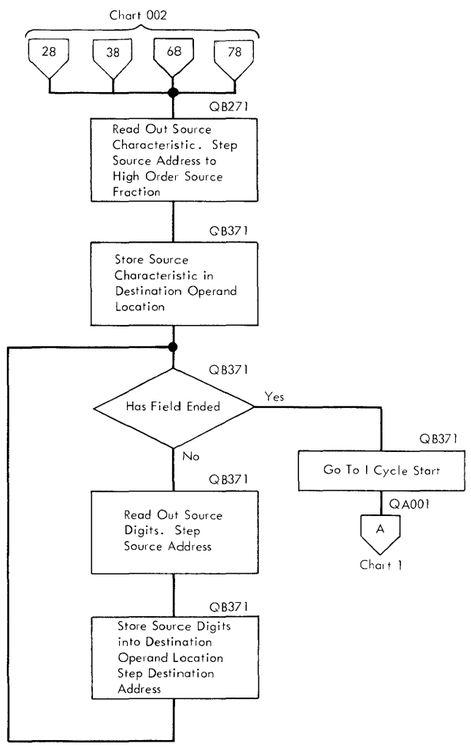
Mnemonics
HDR
HER



Op Format	Byte 1	Byte 2	Byte 3	Byte 4
RR FP Load, Double	28	R1 R2		
RR FP Load, Single	38	R1 R2		
RX FP Load, Double	68	R1 X2	B2 D2	D2
RX FP Load, Single	78	R1 X2	B2 D2	D2

Load RR and RX Formats
Single or Double Precision

Second Operand is Placed in
First Operand Location.
In Single Precision the
Low Half of the Destination
Operand Remains Unchanged.



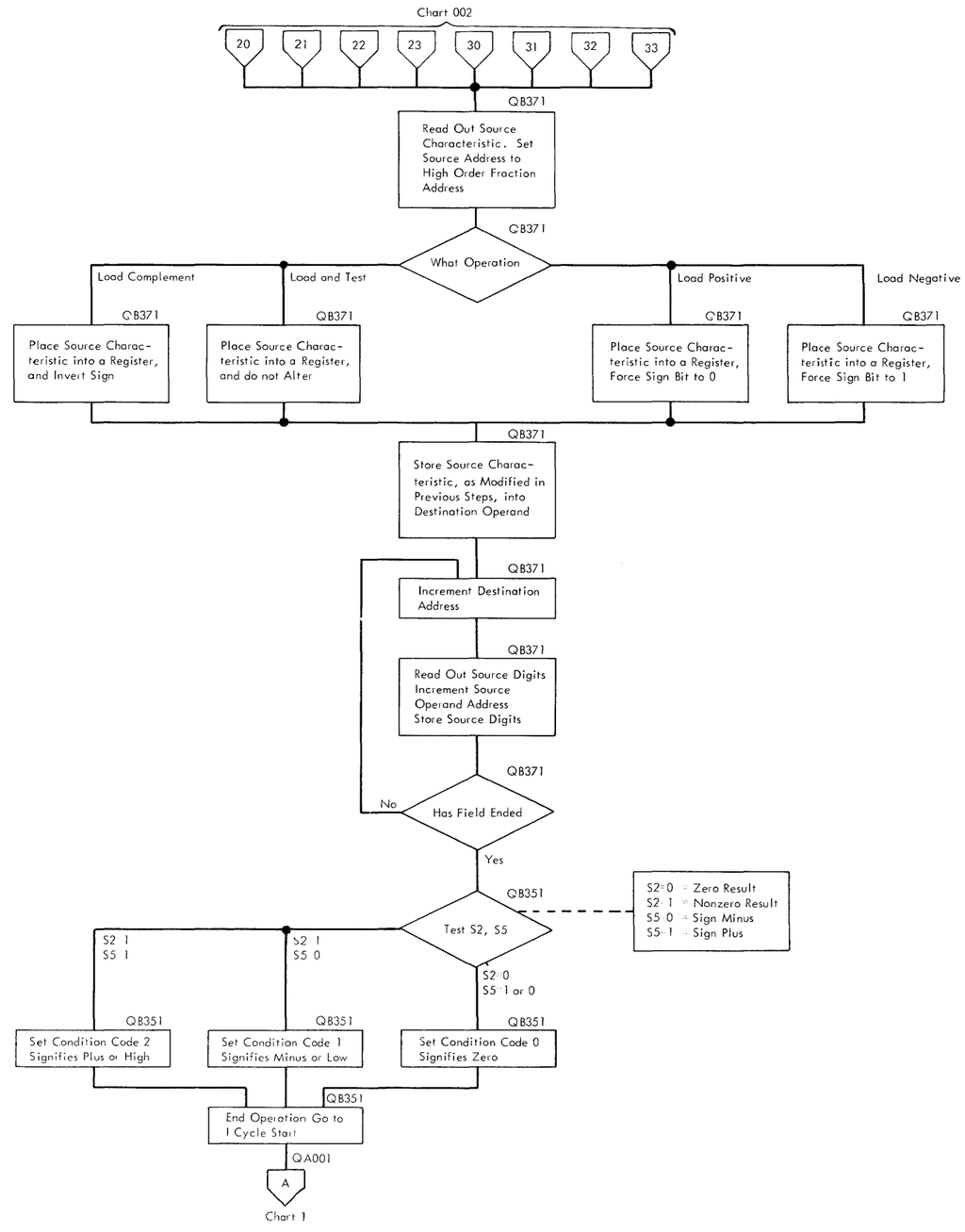
Load and Test; the Second Operand is Placed in the First Operand Location. Condition Codes are Set.

Load Complement; the Second Operand is Placed in the First Operand Location with the Sign Changed.

Load Positive; the Second Operand is Placed in the First Operand Location with the Sign Forced Positive.

Load Negative; the Second Operand is Placed in the First Operand Location with the Sign Forced Minus.

Op Format	Byte 1	Byte 2
RR FP Load Positive	20	R1 R2
RR FP Load Positive	30	R1 R2
RR FP Load Negative	21	R1 R2
RR FP Load Negative	31	R1 R2
RR FP Load and Test	22	R1 R2
RR FP Load and Test	32	R1 R2
RR FP Load Complement	23	R1 R2
RR FP Load Complement	33	R1 R2



Floating Point.

Op Format	Byte 1	Byte 2	Byte 3	Byte 4
RR Compare - Double	29	R1 ¦ R2		
RR Add N - Double	2A	R1 ¦ R2		
RR Subtract N - Double	2B	R1 ¦ R2		
RR Add U - Double	2E	R1 ¦ R2		
RR Subtract U - Double	2F	R1 ¦ R2		
RR Compare - Single	39	R1 ¦ R2		
RR Add N - Single	3A	R1 ¦ R2		
RR Subtract N - Single	3B	R1 ¦ R2		
RR Add U - Single	3E	R1 ¦ R2		
RR Subtract U - Single	3F	R1 ¦ R2		
RX Compare - Double	69	R1 ¦ X2	B2 ¦ D2	D2
RX Add N - Double	6A	R1 ¦ X2	B2 ¦ D2	D2
RX Subtract N - Double	6B	R1 ¦ X2	B2 ¦ Dz	D2
RX Add U - Double	6E	R1 ¦ X2	B2 ¦ Dz	D2
RX Subtract U - Double	6F	R1 ¦ X2	B2 ¦ D2	D2
RX Compare - Single	79	R1 ¦ X2	B2 ¦ D2	D2
RX Add N - Single	7A	R2 ¦ X2	B2 ¦ D2	D2
RX Subtract N - Single	7B	R2 ¦ X2	B2 ¦ D2	D2
RX Add U - Single	7E	R1 ¦ X2	B2 ¦ D2	D2
RX Subtract U - Single	7F	R1 ¦ X2	B2 ¦ D2	D2

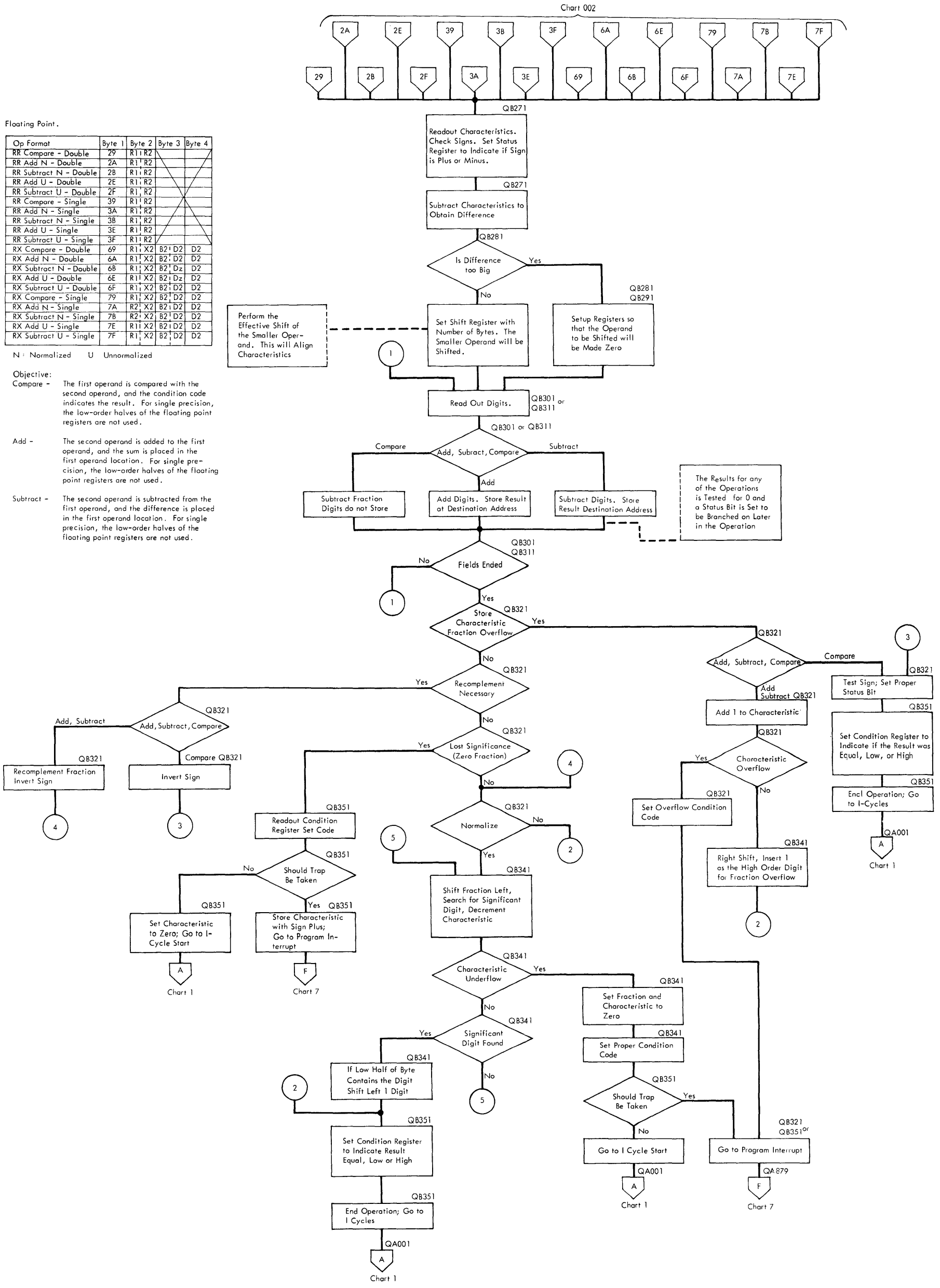
N : Normalized U Unnormalized

Objective:

Compare - The first operand is compared with the second operand, and the condition code indicates the result. For single precision, the low-order halves of the floating point registers are not used.

Add - The second operand is added to the first operand, and the sum is placed in the first operand location. For single precision, the low-order halves of the floating point registers are not used.

Subtract - The second operand is subtracted from the first operand, and the difference is placed in the first operand location. For single precision, the low-order halves of the floating point registers are not used.



Floating Point Normalized Add

The second operand is added to the first operand, and the normalized sum is placed in the first operand location.

Addition consists of characteristic comparison and fraction addition.

QB271 Read out characteristics, shift them left one bit to determine signs. Sign bit is the high-order bit of the characteristic.

Subtract characteristics to determine charactertic difference.

The difference represents double the number of hexadecimal digits that the smaller operand
QB281 will effectively be shifted right. Shifting is actually accomplished by changing the address of the first fraction byte to be read out. This aligns the low-order fraction bytes for addition.

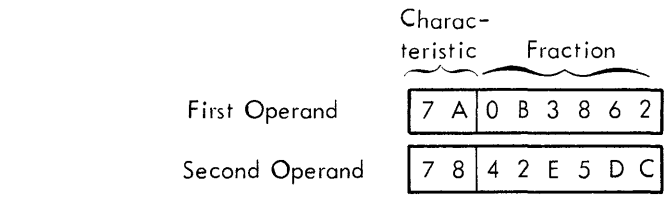
QB291 Determine the new address of the effective low-order byte, store the high-order digit of the next lower byte to be used as a guard digit.

QB301 Read out low-order fraction bytes and add.
or Store result in low-order 1st operand location.
QB311 Continue addition until fields end. When smaller operand field ends, 0's are supplied until larger ends.

Partial result characteristic will be characteristic of the larger operand.

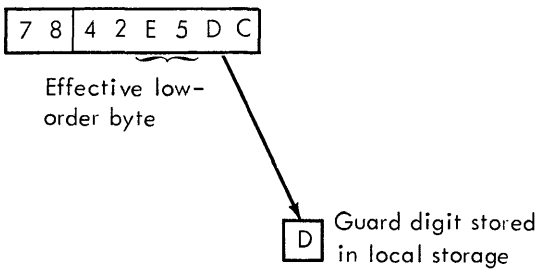
QB341 High-order partial result digit = 0, normalization required. Shift left until high-order digit is significant, add in guard digit as low-order result digit.

QB351 Condition register is set to indicate:
Code
0 = Result fraction is zero
1 = Result fraction less than zero
2 = Result fraction greater than zero
3 = Result exponent overflows



First Operand 7 A shift left F 4
Second Operand 7 8 shift left F 0
Signs Plus

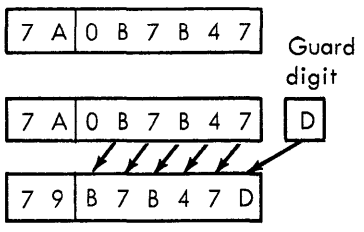
F 4
F 0
Characteristic difference 4



First Operand 6 2
Second Operand E 5
Carry 4 7

First Operand 3 8
Second Operand 4 2
7 B

First Operand 0 B
Zeros Supplied 0 0
0 B

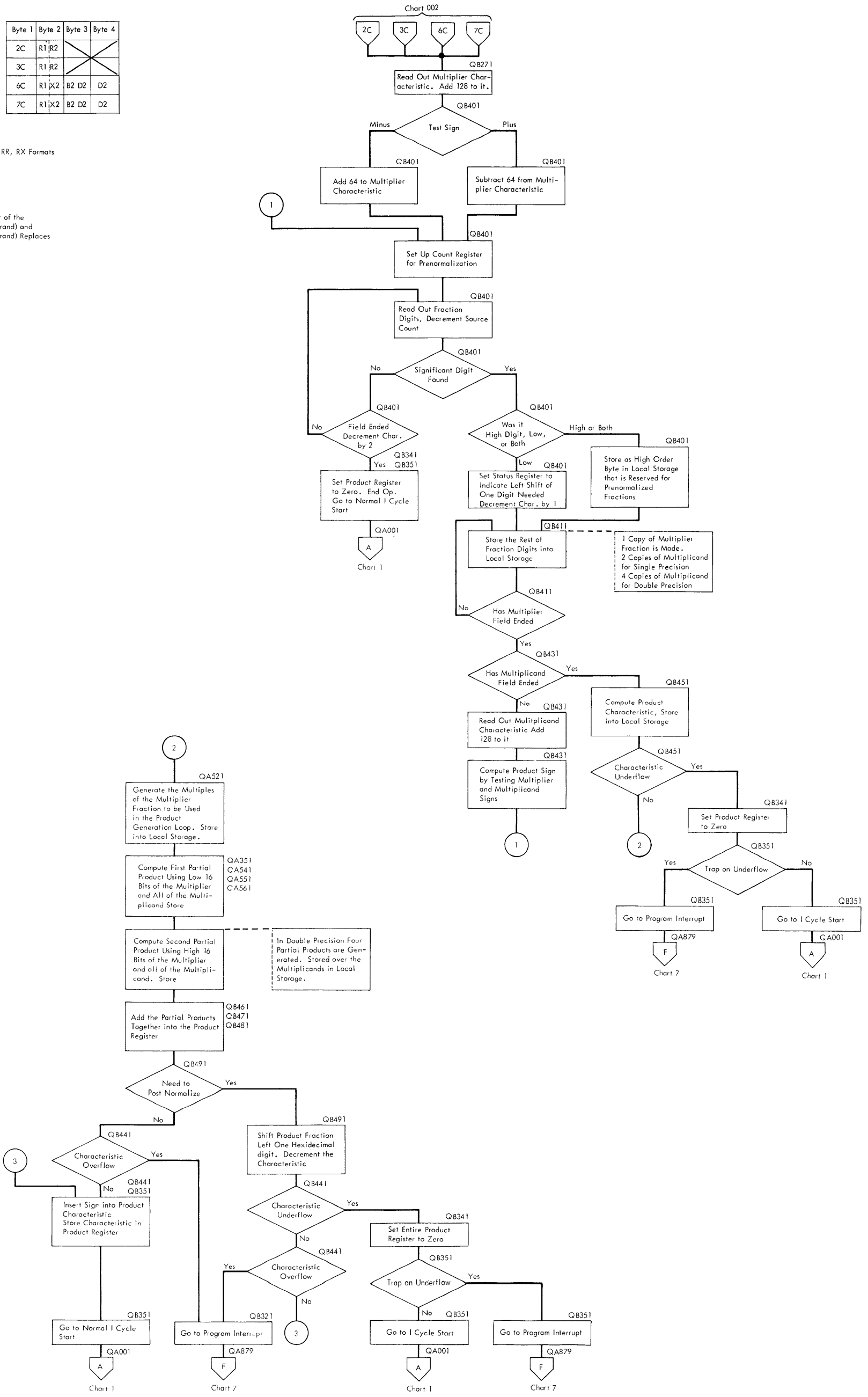


Characteristic is decremented 1 for every hexadecimal digit shifted left.

Op Format	Byte 1	Byte 2	Byte 3	Byte 4
RR Double	2C	R1 R2		
RR Single	3C	R1 R2		
RX Double	6C	R1 X2	B2 D2	D2
RX Single	7C	R1 X2	B2 D2	D2

Floating Point Multiply RR, RX Formats
Mnemonics
MER
ME
MDR
MD

The Normalized Product of the Multiplier (Second Operand) and Multiplicand (First Operand) Replaces the Multiplicand



Floating Point Multiply, Single Precision

The two 24-bit fractions are multiplied together and form a 56-bit product. The product replaces the first operand (multiplicand).

The product characteristic is the sum of the two characteristics minus 64.

QB401 QB411 1. Prenormalized the multiplier fraction into the work area of storage.

2. Make two prenormalized copies of the multiplicand into the work area of storage.

QB431 3. Compute product sign, store it until product is computed.

QB451 4. Compute product characteristic, test for underflow. Store into local storage until product is computed.

QB451 5. Load 16 bits of the multiplier into hardware registers. The first time through this preparation step, only 8 multiplier bits are loaded. Zeros are loaded into the other hardware register. Second time through, the next 16 multiplier bits are loaded into hardware registers.

QA521 6. Generate multiples of the multiplier to be used in the compute loop. Store multiples into working storage and hardware registers.

Two separate multiply loops will be done, each using 16 bits of the multiplier and all bits of the multiplicand.

Each multiply loop will produce a 40-bit partial product, the partial products are stored over the copies of the multiplicand.

7. Decode and operate on the multiplicand, one digit at a time. Decoding the multiplicand digits sets up branching conditions in the microprogram, which will cause the correct combinations of multiples to be added or subtracted to form a partial product.

8. After a digit is decoded and operated on, the low digit in the product accumulator is stored as a digit in the partial product location. Each multiplicand digit decoded, and operated on, produces one partial product digit.

9. Multiply loop continues until two partial products are produced.
Align the two partial products and add to produce a 56-bit product. Normalize if needed. Insert characteristic and sign.

	Characteristic	Fraction
R1 (multiplicand)	2 4	7 2 A 9 B 6
R2 (multiplier)	3 7	2 4 1 3 1 2

```
  2 4 = multiplicand characteristic
+ 3 7 = multiplier characteristic
  5 B
Minus binary 64 equals  1 B = product characteristic
```

Low 8 bits of multiplier into hardware register. 1 2
Zeros loaded into another register. 0 0
1st 16 bits of multiplier 1 2 0 0

For 1st multiply
1X = 1 2 0 0
2X = 2 4 0 0

For 2nd multiply
1X = 2 4 1 3
2X = 4 8 2 6

Example: 1st multiplicand digit = 6

6 decodes as 2X, 2X, 2X
this means, the multiplier times 2 is added 3 times into the product accumulator.

```
  2X = 2 4 0 0
+ 2X = 2 4 0 0
       4 8 0 0
+ 2X = 2 4 0 0
       6 C 0 0
```

Store low digit at low-digit location of 1st partial product. Shift digits right one digit in product accumulator and await next decode

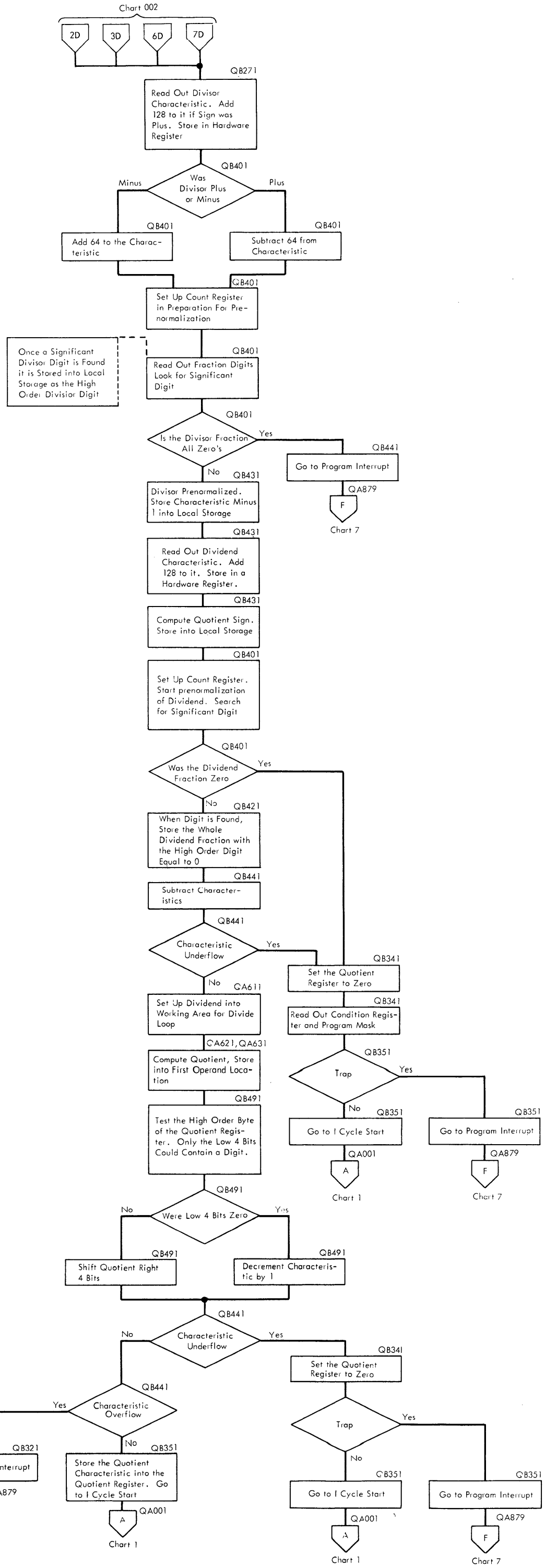
product accumulator
0 6 C 0

```
1st partial product          0 8 0 F E E C C 0 0
2nd partial product  1 0 2 8 6 0 3 0 8 2
product              1 0 2 8 6 8 4 0 7 0 C C 0 0
Insert characteristic  1 B   1 0 2 8 6 8 4 0 7 0 C C 0 0
Insert sign           +1 B   1 0 2 8 6 8 4 0 7 0 C C 0 0
```

Op Format	Byte 1	Byte 2	Byte 3	Byte 4
RR Divide, Double	2D	R1 | R2		
RR Divide, Single	3D	R1 | R2		
RX Divide, Double	6D	R1 | X2	B2 | D2	D2
RX Divide, Single	7D	R1 | X2	B2 | D2	D2

Floating Point Divide RR, RX Formats
Single and Double Precision
Mnemonics
DER
DE
DDR
DD

The First Operand is Divided by the Second Operand, the Quotient Replaces the First Operand



Floating Point Divide

All numbers shown are in hexadecimal

		Characteristic	Fraction
First Operand is the	Dividend	2 5	9 6 7 2 E A
Second Operand is the	Divisor	1 9	7 1 3 4 B 5

The characteristics are carried in excess 64 notation at all times.

The divisor in this example is a normalized number and will not be prenormalized. The dividend is prenormalized with the high-order digit equal to zero. In this example, the dividend will be shifted right one digit to accomplish this. The low-order digit will be shifted out into the hardware register in which the quotient will be formed. The first time through the divide loop, only 4 quotient digits will be computed and stored. The next divide loops will produce 8 quotient digits until the operation is completed.

Page No.

QB271 Divisor characteristic is read out, a bit is added to the high-order position (sign). The characteristic will now be without sign if it was minus, or effectively have a value of 128 higher if it was plus.

Divisor Characteristic

```
  1 9
+8 0
-----
  9 9
```

Sign was plus, characteristic is now expressed in excess 192. If sign were minus it would still be expressed in excess 64.

QB401 Divisor characteristic has 64 added to it or subtracted from it, depending on the sign position. If the sign had been plus, 64 will be subtracted from it; if it was minus, 64 is added. The characteristic now represents the numeric value of the exponent +128 instead of +64 as it usually does.

Divisor Characteristic

```
  9 9
+C 0
-----
  5 9
```

Subtracting 64 is done by adding C to high order.

```
  5 9
+F F
-----
  5 8
```

Subtract 1 from the characteristic leaving it expressed in excess 127. This is done to compensate for the fact that the dividend is shifted right one digit as it is loaded.

QB431 Dividend characteristic is read out and sign is tested. 128 is added to characteristic; it now represents the dividend exponent +192.

Dividend Characteristic

```
  2 5
+8 0
-----
  A 5
```

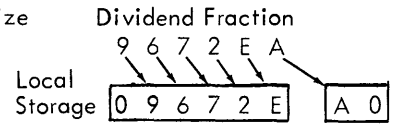
Sign was plus; characteristic is now expressed in excess 192.

Compute quotient sign and store. If signs are alike, quotient sign will be plus. If signs are unlike, quotient sign will be minus.

QB421 Do the skewed dividend prenormalize into local storage and hardware

Divisor fraction is loaded into hardware, or hardware and local storage.

Dividend Fraction



QB441 Compute the Quotient characteristic. The divisor characteristic is complement added to the dividend characteristic

```
    A 5    dividend characteristic ←→ excess 192
    A 7    divisor characteristic complemented ←→ excess 127
+     1    plus one
-----
c←4 D      quotient characteristic
```

The result is now excess 65; however, when the final quotient is produced (shifted left 4 bits), it will be excess 64.

If the computation of the quotient characteristic failed to produce a carry, an underflow would be sensed. The quotient register would be set to zero and the program would return to I-cycles or to program interrupt, depending on the mask bit.

QA621
QA631 The divide function is performed on these 2 pages. The quotient is produced one bit at a time into a hardware register. The first time through the divide loop, 4 quotient bits are produced and stored in the high-order address of the quotient register. In each of the following loops, 8 quotient bits are produced and stored until the entire quotient has been computed.

	Characteristic	Fraction
Final Result	4D	1 5 4 3 8 5

The quotient has been produced and is located in all bytes of the quotient register. The high-order byte must be checked to see if the quotient characteristic may be stored there. If the high-order byte is zero, the characteristic is stored there decremented by 1 to indicate high-order zero. If the high-order byte contains a low-order digit, (can never contain high-order digit) the quotient is right shifted one digit, the low quotient digit is lost, and the characteristic is stored unchanged. The characteristic is always checked, before storing, for overflow and underflow. If overflow, go to program interrupt. If underflow, set the quotient register to zero, test for trap, and go to normal I-cycles or program interrupt.

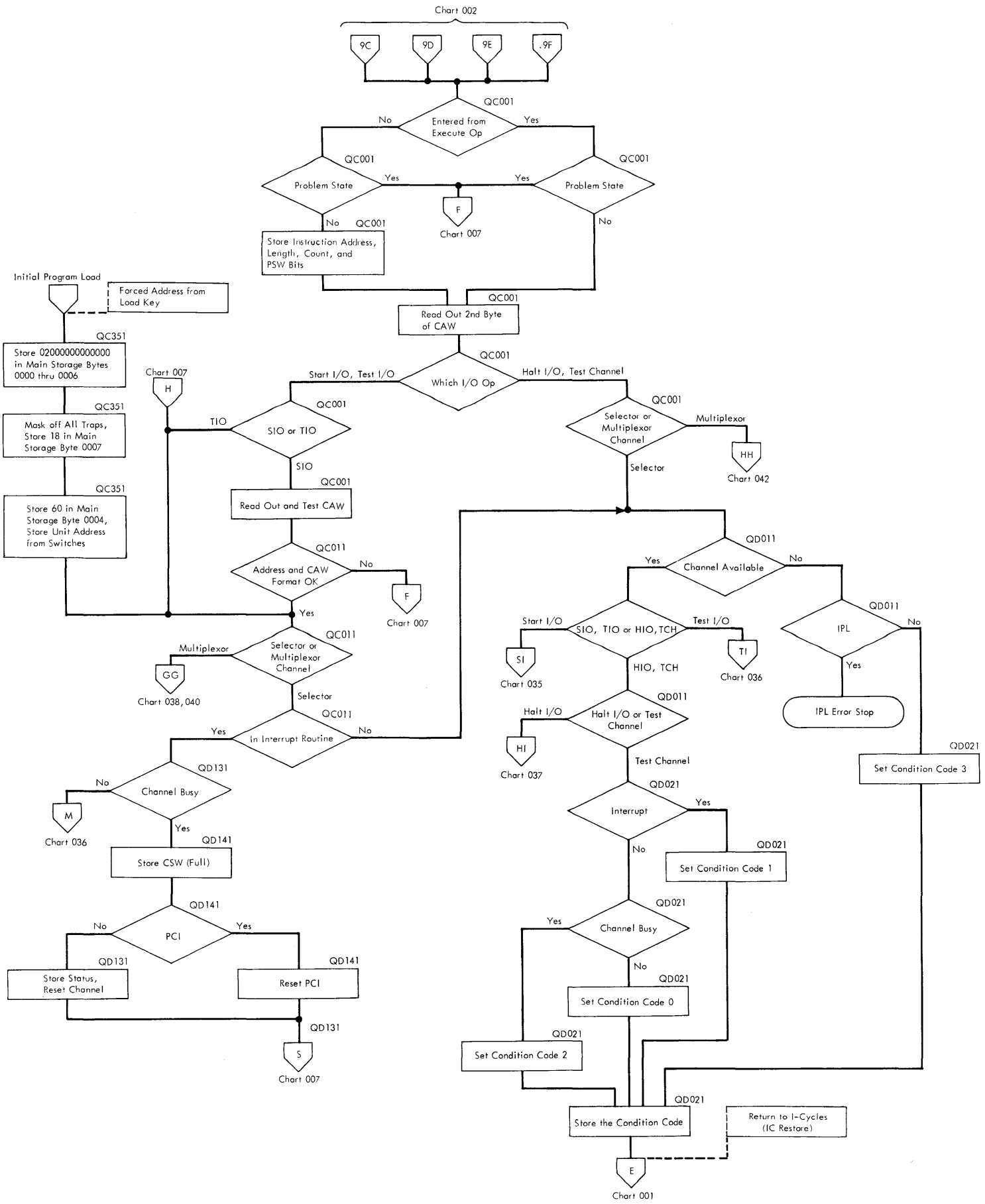


Chart 002
9C
9D
9E
.9F
QC001
Entered from Execute Op
No
Yes
QC001
Problem State
Yes
F
Chart 007
No
QC001
Store Instruction Address, Length, Count, and PSW Bits
QC001
Problem State
Yes
No
Initial Program Load
Forced Address from Load Key
QC001
Read Out 2nd Byte of CAW
QC001
Which I/O Op
Start I/O, Test I/O
Halt I/O, Test Channel
QC351
Store 02000000000000 in Main Storage Bytes 0000 thru 0006
QC351
Mask off All Traps, Store 18 in Main Storage Byte 0007
QC351
Store 60 in Main Storage Byte 0004, Store Unit Address from Switches
Chart 007
H
TIO
QC001
SIO or TIO
SIO
QC001
Read Out and Test CAW
QC011
Address and CAW Format OK
No
F
Chart 007
Yes
QC001
Selector or Multiplexor Channel
Multiplexor
HH
Chart 042
Selector
QD011
Channel Available
Yes
No
Start I/O
SIO, TIO or HIO, TCH
Test I/O
SI
Chart 035
TI
Chart 036
HIO, TCH
QD011
IPL
No
Yes
IPL Error Stop
QD021
Set Condition Code 3
QD011
Halt I/O or Test Channel
Halt I/O
HI
Chart 037
Test Channel
QD021
Interrupt
Yes
No
QD021
Set Condition Code 1
QD021
Channel Busy
Yes
No
QD021
Set Condition Code 0
QD021
Set Condition Code 2
QD021
Store the Condition Code
Return to I-Cycles (IC Restore)
E
Chart 001
QC011
Selector or Multiplexor Channel
Multiplexor
GG
Chart 038, 040
Selector
QC011
In Interrupt Routine
Yes
No
QD131
Channel Busy
No
M
Chart 036
Yes
QD141
Store CSW (Full)
QD141
PCI
No
Yes
QD131
Store Status, Reset Channel
QD141
Reset PCI
QD131
S
Chart 007

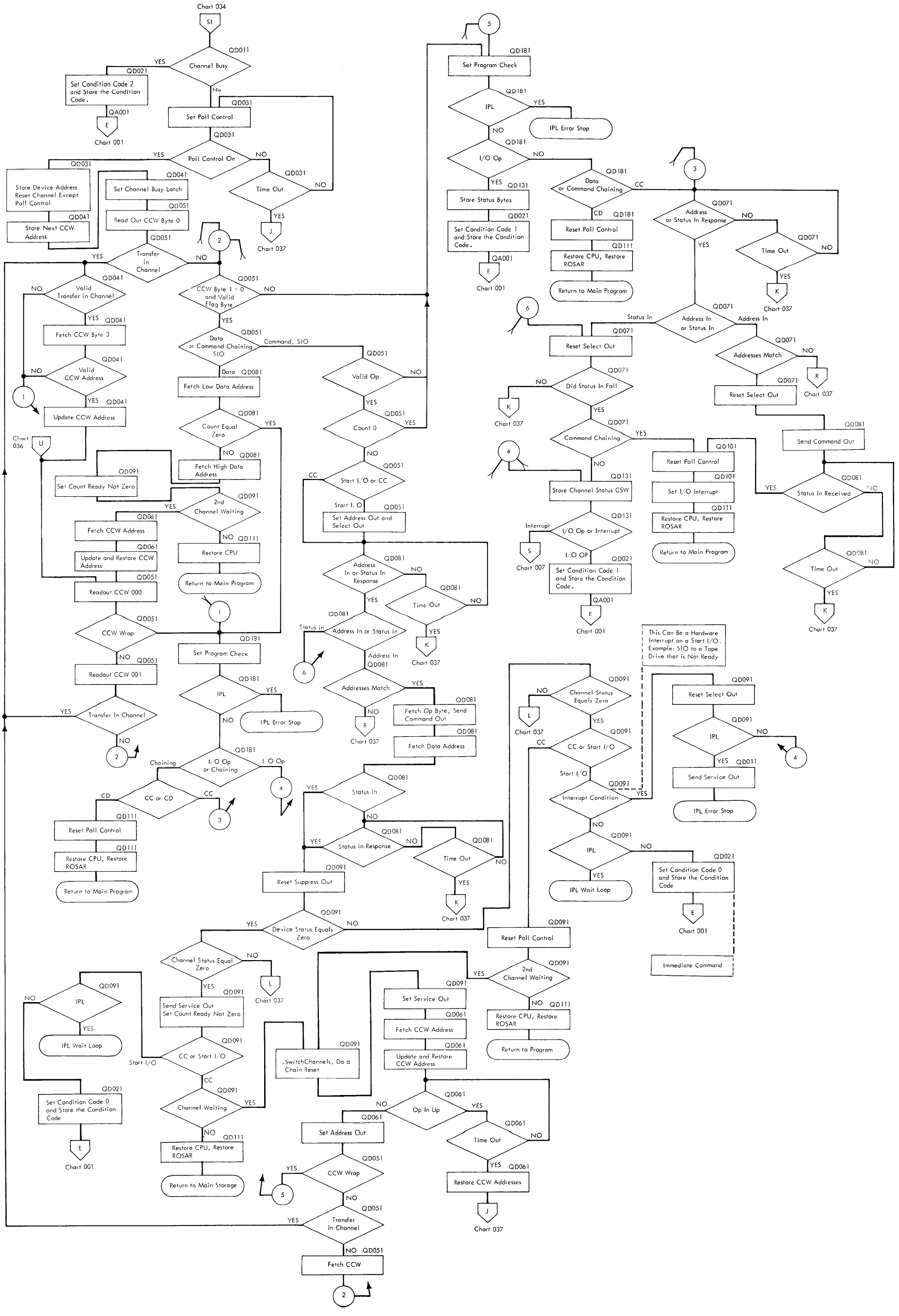
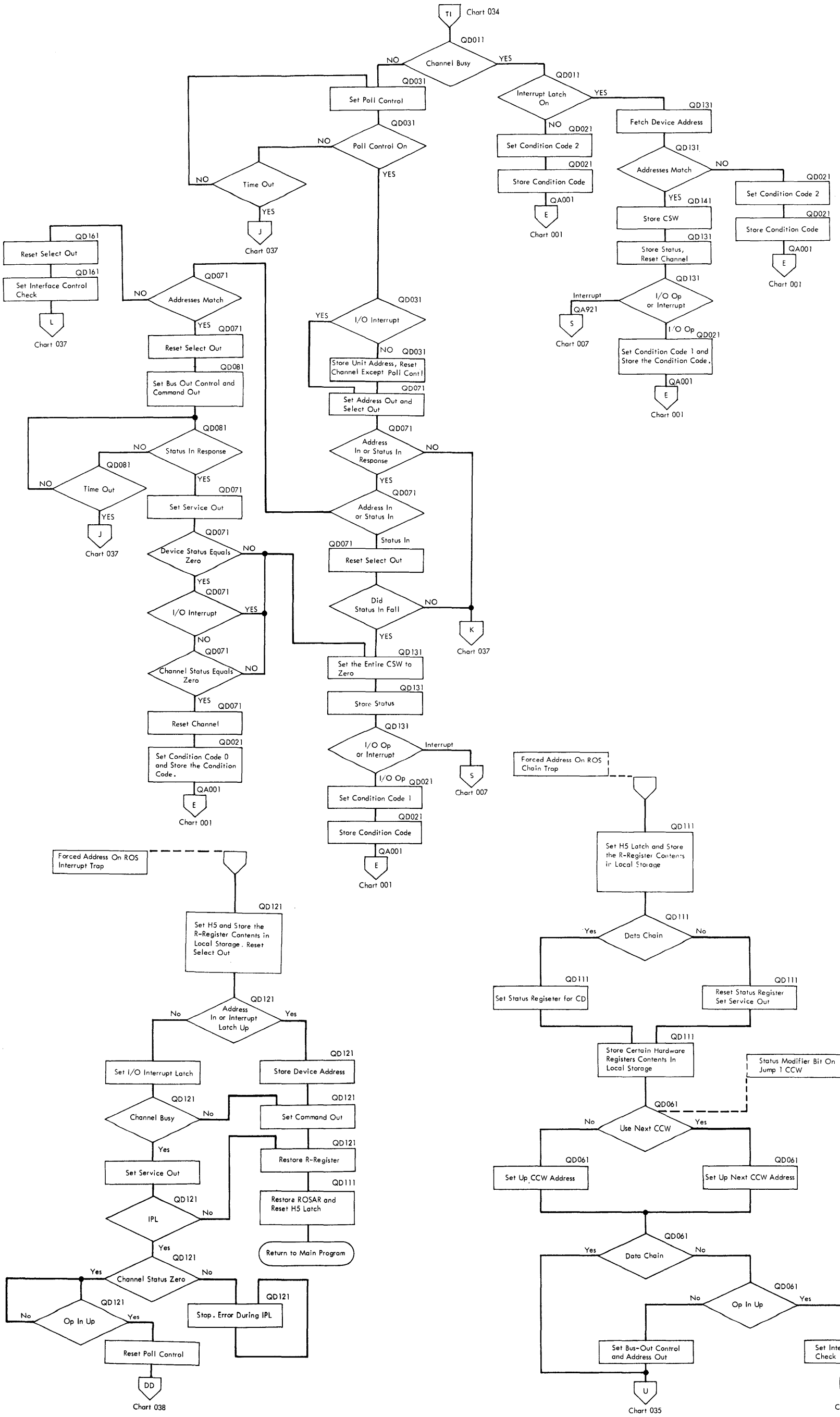


Chart 034
SI
QD011
Channel Busy
YES
QD021
Set Condition Code 2 and Store the Condition Code.
QA001
E
Chart 001
No
QD031
Set Poll Control
QD031
Poll Control On
YES
NO
QD031
Store Device Address Reset Channel Except Poll Control
QD041
Store Next CCW Address
QD041
Set Channel Busy Latch
QD051
Read Out CCW Byte 0
QD031
Time Out
NO
YES
J
Chart 037
2
QD051
Transfer in Channel
YES
NO
QD041
Valid Transfer in Channel
NO
YES
QD041
Fetch CCW Byte 3
QD041
Valid CCW Address
NO
YES
QD041
Update CCW Address
1
Chart 036
U
QD091
Set Count Ready Not Zero
QD091
2nd Channel Waiting
YES
NO
QD061
Fetch CCW Address
QD061
Update and Restore CCW Address
QD051
Readout CCW 000
QD051
CCW Wrap
NO
QD051
Readout CCW 001
YES
Transfer In Channel
NO
2
QD051
CCW Byte 1 = 0 and Valid Flag Byte
NO
YES
QD051
Data or Command Chaining SIO
Command, SIO
Data
QD081
Fetch Low Data Address
QD081
Count Equal Zero
YES
NO
QD081
Fetch High Data Address
QD111
Restore CPU
Return to Main Program
1
QD181
Set Program Check
QD181
IPL
YES
NO
IPL Error Stop
QD181
I/O Op or Chaining
Chaining
I/O Op
CD
CC or CD
CC
3
4
QD111
Reset Poll Control
QD111
Restore CPU, Restore ROSAR
Return to Main Program
QD051
Valid Op
NO
YES
QD051
Count 0
YES
NO
QD051
Start I/O or CC
CC
Start I/O
QD051
Set Address Out and Select Out
QD081
Address In or Status In Response
NO
YES
QD081
Time Out
NO
YES
K
Chart 037
QD081
Address In or Status In
Status In
Address In
6
QD081
Addresses Match
YES
NO
R
Chart 037
QD081
Fetch Op Byte, Send Command Out
QD081
Fetch Data Address
QD081
Status In
YES
NO
QD081
Status in Response
NO
YES
QD081
Time Out
NO
YES
K
Chart 037
QD091
Reset Suppress Out
QD091
Device Status Equals Zero
YES
NO
Channel Status Equal Zero
NO
YES
L
Chart 037
QD091
IPL
NO
YES
IPL Wait Loop
QD091
Send Service Out
Set Count Ready Not Zero
QD091
CC or Start I/O
Start I/O
CC
QD091
Channel Waiting
YES
NO
QD111
Restore CPU, Restore ROSAR
Return to Main Storage
QD021
Set Condition Code 0 and Store the Condition Code
E
Chart 001
QD091
.SwitchChannels, Do a Chain Reset
5
QD051
CCW Wrap
YES
NO
QD051
Transfer In Channel
YES
NO QD051
Fetch CCW
2
5
QD181
Set Program Check
QD181
IPL
YES
NO
IPL Error Stop
QD181
I/O Op
NO
YES
QD131
Store Status Bytes
QD021
Set Condition Code 1 and Store the Condition Code.
QA001
E
Chart 001
QD181
Data or Command Chaining
CC
CD
QD181
Reset Poll Control
QD111
Restore CPU, Restore ROSAR
Return to Main Program
3
QD071
Address or Status In Response
NO
YES
QD071
Time Out
NO
YES
K
Chart 037
6
Status In
QD071
Address In or Status In
Address In
QD071
Reset Select Out
QD071
Did Status In Fail
NO
YES
K
Chart 037
4
QD071
Command Chaining
YES
NO
QD101
Reset Poll Control
QD101
Set I/O Interrupt
QD111
Restore CPU, Restore ROSAR
Return to Main Program
QD131
Store Channel Status CSW
QD131
I/O Op or Interrupt
Interrupt
I/O OP
S
Chart 007
QD021
Set Condition Code 1 and Store the Condition Code.
QA001
E
Chart 001
QD071
Addresses Match
NO
R
Chart 037
QD071
Reset Select Out
QD081
Send Command Out
QD081
Status In Received
NO
YES
QD081
Time Out
NO
YES
K
Chart 037
This Can Be a Hardware Interrupt on a Start I/O. Example: SIO to a Tape Drive that is Not Ready
QD091
Channel Status Equals Zero
NO
YES
L
Chart 037
QD091
CC or Start I/O
CC
Start I/O
QD091
Interrupt Condition
YES
NO
QD091
IPL
NO
YES
IPL Wait Loop
QD091
Reset Poll Control
QD091
2nd Channel Waiting
YES
NO
QD111
Restore CPU, Restore ROSAR
Return to Program
QD091
Reset Select Out
QD091
IPL
NO
YES
QD011
Send Service Out
IPL Error Stop
4
QD021
Set Condition Code 0 and Store the Condition Code
E
Chart 001
Immediate Command
QD091
Set Service Out
QD061
Fetch CCW Address
QD061
Update and Restore CCW Address
QD061
Op In Up
NO
YES
QD061
Set Address Out
QD061
Time Out
NO
YES
QD061
Restore CCW Addresses
J
Chart 037


TI
Chart 034
QD011
Channel Busy
NO
YES
QD031
Set Poll Control
QD031
Poll Control On
NO
YES
NO
Time Out
YES
J
Chart 037
QD011
Interrupt Latch On
YES
NO
QD021
Set Condition Code 2
QD021
Store Condition Code
QA001
E
Chart 001
QD131
Fetch Device Address
QD131
Addresses Match
NO
YES
QD141
Store CSW
QD131
Store Status, Reset Channel
QD131
I/O Op or Interrupt
Interrupt
QA921
S
Chart 007
I/O Op
QD021
Set Condition Code 1 and Store the Condition Code.
QA001
E
Chart 001
QD021
Set Condition Code 2
QD021
Store Condition Code
QA001
E
Chart 001
QD161
Reset Select Out
QD161
Set Interface Control Check
L
Chart 037
NO
QD071
Addresses Match
YES
QD071
Reset Select Out
QD081
Set Bus Out Control and Command Out
QD081
Status In Response
NO
YES
QD081
Time Out
NO
YES
J
Chart 037
QD071
Set Service Out
QD071
Device Status Equals Zero
NO
YES
QD071
I/O Interrupt
YES
NO
QD071
Channel Status Equals Zero
NO
YES
QD071
Reset Channel
QD021
Set Condition Code 0 and Store the Condition Code.
QA001
E
Chart 001
QD031
I/O Interrupt
YES
NO
QD031
Store Unit Address, Reset Channel Except Poll Cont'l
QD071
Set Address Out and Select Out
QD071
Address In or Status In Response
NO
YES
QD071
Address In or Status In
Status In
QD071
Reset Select Out
Did Status In Fall
NO
YES
K
Chart 037
QD131
Set the Entire CSW to Zero
QD131
Store Status
QD131
I/O Op or Interrupt
Interrupt
S
Chart 007
I/O Op
QD021
Set Condition Code 1
QD021
Store Condition Code
QA001
E
Chart 001
Forced Address On ROS Interrupt Trap
QD121
Set H5 and Store the R-Register Contents in Local Storage. Reset Select Out
QD121
Address In or Interrupt Latch Up
No
Yes
QD121
Set I/O Interrupt Latch
QD121
Store Device Address
QD121
Channel Busy
No
Yes
QD121
Set Command Out
QD121
Restore R-Register
QD111
Restore ROSAR and Reset H5 Latch
Return to Main Program
Set Service Out
QD121
IPL
No
Yes
QD121
Channel Status Zero
Yes
No
QD121
Op In Up
No
Yes
QD121
Stop. Error During IPL
Reset Poll Control
DD
Chart 038
Forced Address On ROS Chain Trap
QD111
Set H5 Latch and Store the R-Register Contents in Local Storage
QD111
Data Chain
Yes
No
QD111
Set Status Regiseter for CD
QD111
Reset Status Register Set Service Out
QD111
Store Certain Hardware Registers Contents In Local Storage
Status Modifier Bit On Jump 1 CCW
QD061
Use Next CCW
No
Yes
QD061
Set Up CCW Address
QD061
Set Up Next CCW Address
QD061
Data Chain
Yes
No
QD061
Op In Up
No
Yes
QD161
Set Bus-Out Control and Address Out
Set Interface Control Check
U
Chart 035
L
Chart 037

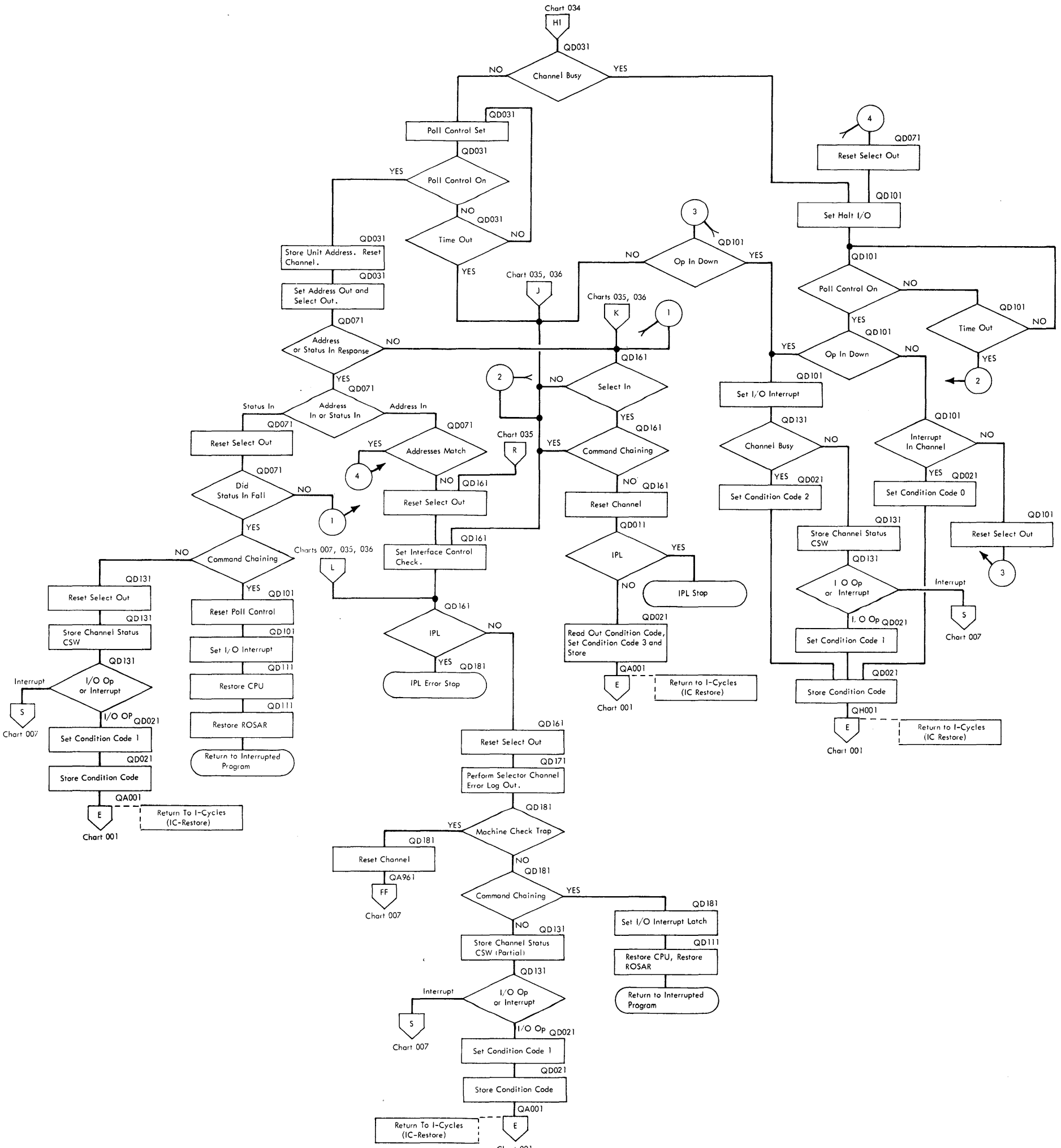
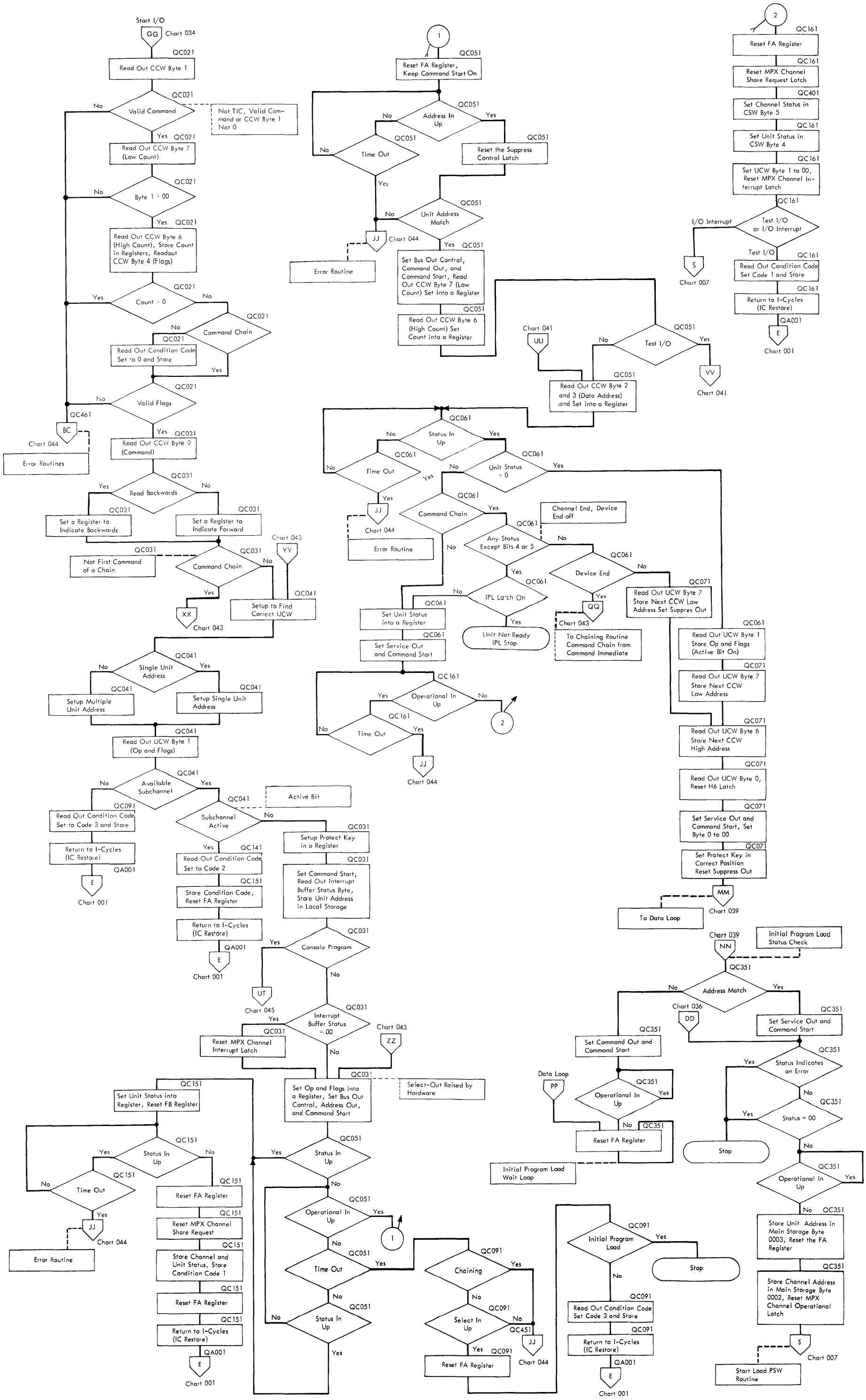


Chart 034
HI
QD031
Channel Busy
NO
YES
QD031
Poll Control Set
QD031
Poll Control On
YES
NO
QD031
Time Out
NO
YES
QD031
Store Unit Address. Reset Channel.
QD031
Set Address Out and Select Out.
QD071
Address or Status In Response
NO
YES
QD071
Address In or Status In
Status In
Address In
QD071
Reset Select Out
QD071
Did Status In Fall
NO
YES
Command Chaining
NO
YES
QD131
Reset Select Out
QD131
Store Channel Status CSW
QD131
I/O Op or Interrupt
Interrupt
I/O OP
S
Chart 007
QD021
Set Condition Code 1
QD021
Store Condition Code
QA001
E
Chart 001
Return To I-Cycles (IC-Restore)
Charts 007, 035, 036
L
QD101
Reset Poll Control
QD101
Set I/O Interrupt
QD111
Restore CPU
QD111
Restore ROSAR
Return to Interrupted Program
Chart 035, 036
J
Charts 035, 036
K
1
2
3
4
QD071
Addresses Match
YES
NO
Chart 035
R
QD161
Select In
NO
YES
QD161
Command Chaining
YES
NO
QD161
Reset Channel
QD011
IPL
YES
NO
IPL Stop
QD021
Read Out Condition Code, Set Condition Code 3 and Store
QA001
E
Chart 001
Return to I-Cycles (IC Restore)
QD161
Reset Select Out
QD161
Set Interface Control Check.
QD161
IPL
NO
YES
QD181
IPL Error Stop
QD161
Reset Select Out
QD171
Perform Selector Channel Error Log Out.
QD181
Machine Check Trap
YES
NO
QD181
Reset Channel
QA961
FF
Chart 007
QD181
Command Chaining
YES
NO
QD181
Set I/O Interrupt Latch
QD111
Restore CPU, Restore ROSAR
Return to Interrupted Program
QD131
Store Channel Status CSW (Partial)
QD131
I/O Op or Interrupt
Interrupt
I/O Op
S
Chart 007
QD021
Set Condition Code 1
QD021
Store Condition Code
QA001
E
Return To I-Cycles (IC-Restore)
Chart 001
QD071
Reset Select Out
QD101
Set Halt I/O
QD101
Poll Control On
NO
YES
QD101
Op In Down
YES
NO
QD101
Set I/O Interrupt
QD131
Channel Busy
NO
YES
QD021
Set Condition Code 2
QD131
Store Channel Status CSW
QD131
I O Op or Interrupt
Interrupt
I. O Op
S
Chart 007
QD021
Set Condition Code 1
QD021
Store Condition Code
QH001
E
Chart 001
Return to I-Cycles (IC Restore)
QD101
Time Out
NO
YES
QD101
Interrupt In Channel
NO
YES
QD021
Set Condition Code 0
QD101
Reset Select Out
3



CLF 038 MPX Start I/O 1

Chart 038
Data Loop
MM
QC231

Direct Branch
11 - Operational In Down
10 - Status In, Op In Up
01 - Service In, Op In Up
00 - Operational In Up and Neither or Both Status In and Service In Up or Command Out or Service Out Up

Status In, Service In
00, 01
10, 11

2
00
QC081
Status In, Service In
00
01
10, 11
1
QC081
Time Out
No
Yes
JJ
Chart 044
Error Routine

01
QC081
Decrement Low Count By 1, Readout Data
QC081
Skip Flag On
No
Yes
QC081
Input or Output
In
Out
QC081
Set Service Out and Command Start
QC081
Write New Data into Storage, Decrement High Count if Low Count Went from 00-FF
QC081
Set Bus Out Control, Service Out, and Command Start
QC081
Decrement High Count if Low Count Went from 00-FF
QC081
Count = 0
No
Yes
QC081
Increase or Decrease High Data Address
QC081
Chain Data Address
No
Yes
QC101
RR
Chart 043
Data Chain Routines
QC081
Set Condition to Indicate the End Data Cycle
Force Skip Flag and Output Flag On
Direct Branch
QC081
Status In, Service In
00,01
10, 11
2
1

QC081
Input or Output
In
Out
QC081
Restore Data, Decrement High Count
QC081
Command Out Response to Last Service In
Yes
No
QC081
Set Service Out and Command Start
QC081
Reset Output Indicating Bit, Set Command Out
QC081
Restore Count to Original Value
QC081
If Count is 0 Set a Condition to Indicate Status In Next
QC081
Status In, Service In
00, 01
10, 11
2
1
JJ
Chart 044
Error Routines

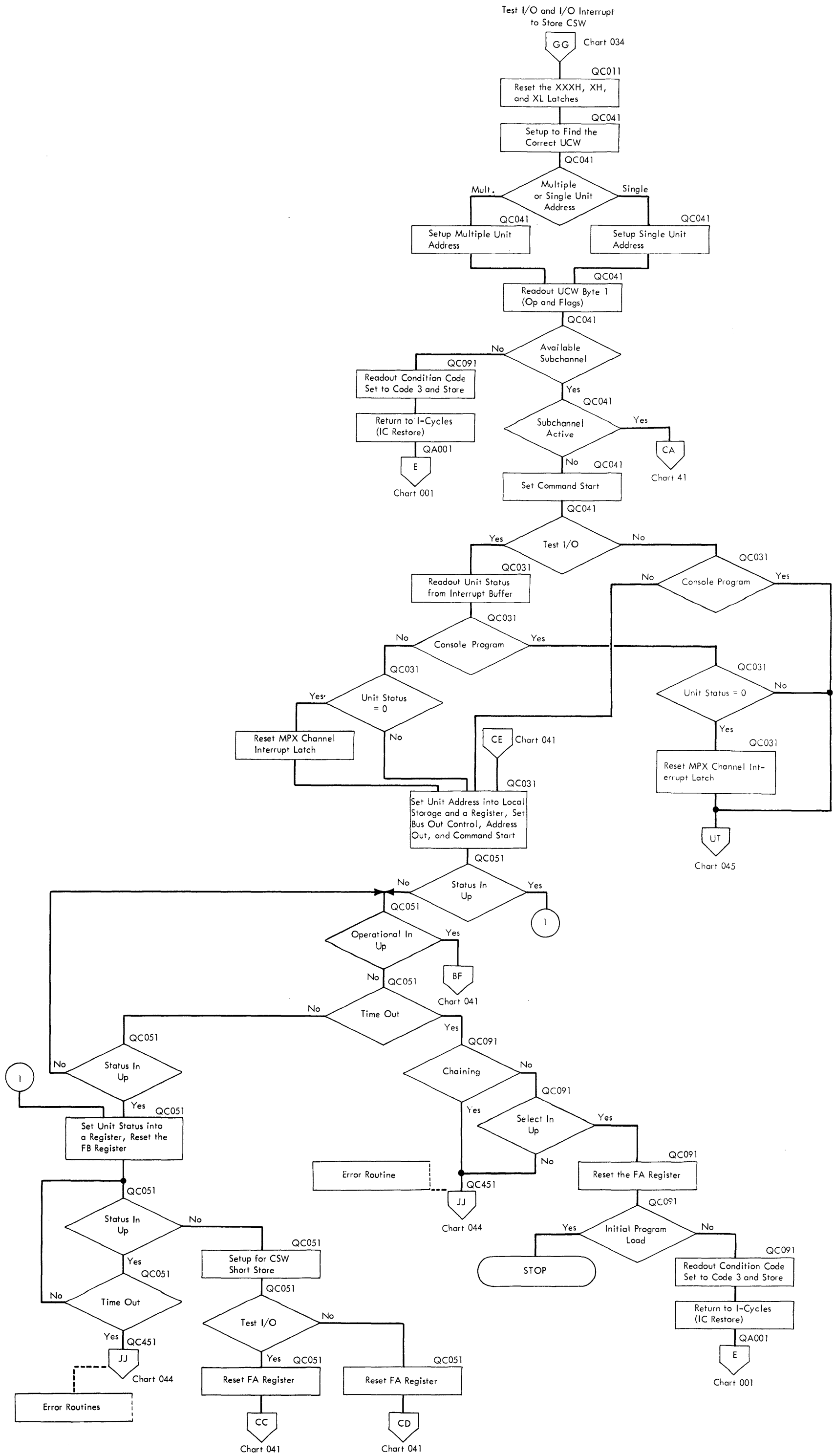
1
10
QC091
Correct Length Record
Yes
No
QC111
Readout UCW Byte 0 and Set into a Register
QC111
Command Chaining
No
3
Yes
QC111
Unit Status Ok
Yes
No
QC111
Readout Unit Address From Storage
QC111
Attention Bit On
Yes
No
QC111
Device End Bit On
Yes
No
SS
Chart 043
Command Chain Routine
QC111
Channel End Bit On
Yes
No
QC111
Set Suppress Control Latch
QC111
Set Service Out and Command Start

QC111
Readout UCW Byte 0 and Set into a Register
QC111
Chain Data Address
Yes
No
QC111
Set WLR in UCW
QC111
Suppress Length Indication
Yes
No
QC111
Command Chaining
Yes
No
3
QC111
Command Chaining
No
Yes
QC111
Readout UCW Byte 1
Set Status of Active Bit
QC111
Readout UCW Byte 1
QC121
Readout Unit Address
QC121
Initial Program Load
Yes
No
QC121
Readout and Set UCW Byte 1 to 00. Set Unit Status in a Register
NN
Chart 038
Initial Program Load Routine
QC121
MPX Channel Interrupt Latch On
Yes
No
QC121
Active Bit On
Yes
No
QC121
Store Unit Address in the Interrupt Buffer, Set MPX Channel Interrupt Latch on
QC121
Active Bit On
Yes
No QC121
Set Interrupt Buffer Unit Status to 00
QC121
Unit Status = 00
Yes
No
QC121
Set False Unit Status
QC121
Store Unit Status in Interrupt Buffer
QC121
Set Service Out and Command Start
QC121
Set Command Out and Command Start

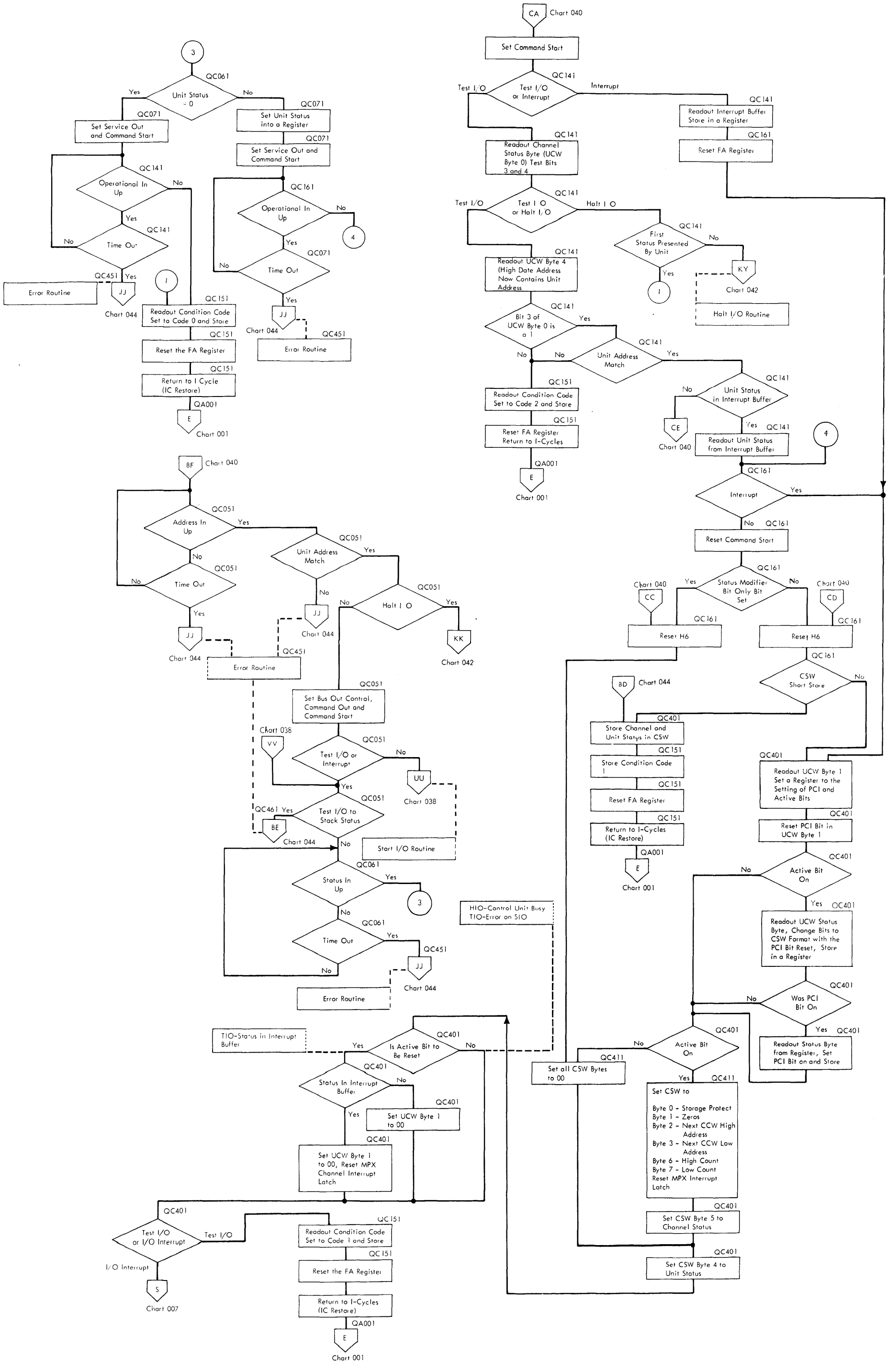
Interrupt Buffer Full
11
QC091
Program Controlled Interrupt Flag On
Yes
No
QC091
MPX Channel Interrupt Latch On
Yes
No QC091
Readout Interrupt Buffer Unit Address Byte and Replace it with New Unit Address, Set MPX Interrupt Latch On
QC091
Set the Interrupt Buffer Status Byte to 00
4
QC301
Setup UCW Bytes 0, 1, 2, 3, 4 and 5
5
Chart 044
BT
QC301
Initial Program Load
Yes
No
QC301
Reset MPX Operational Latch
PP
Chart 038
Initial Program Load Routine
QC301
Reset MPX Channel Operational Latch
QC311
Restore Protect Key (Interrupted Program)
QC311
MPX Channel Share Request
Yes
No
QC311
Return to I-Cycles
Yes
No
QC311
Restore CPU
QC311
Turn On Command Start
QC311
Select Out or Op In On
No
Yes
QC311
Reset Command Start
QC311
Set Up for Re-entry Path
QC311
Share Re-entry
QC211
TT
Chart 043
Share Routine
QC311
Set ROS Address from Backup ROAR Reset H6
QC311
Reset Command Start
Continue Interrupted Program
QC311
Reset the MPX Chan. Operational Latch Reset H6
QC311
Return to I-Cycles (IC Restore)
QA001
E
Chart 001

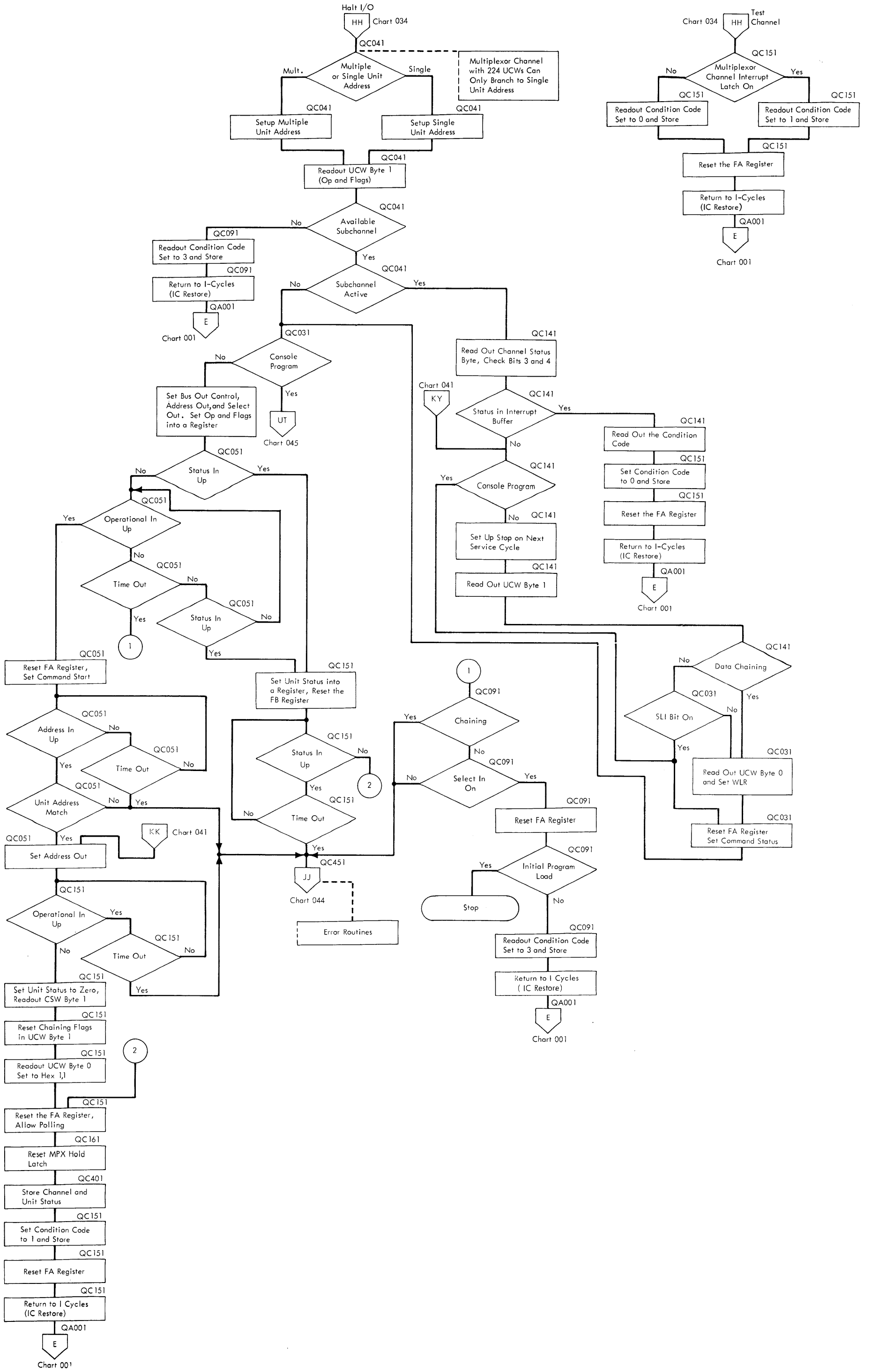
QC161
Operational In Up
No
Yes
QC161
Time Out
No
YES
JJ
Chart 044
Error Routines
QC161
Reset Suppress Control Latch
QC161
Secondary Status
No
Yes QC161
Reset FA Register
4
QC161
Set Updated Status Byte into UCW Byte 0, Reset FA Register
QC301
Set Updated UCW Bytes 1, 2, 3, 4 and 5
5
QC121
Channel End In Buffer for This Unit
Yes
No
QC121
Setup for Secondary Status
QC121
Setup for First Status

CLF 039 MPX Data Loop

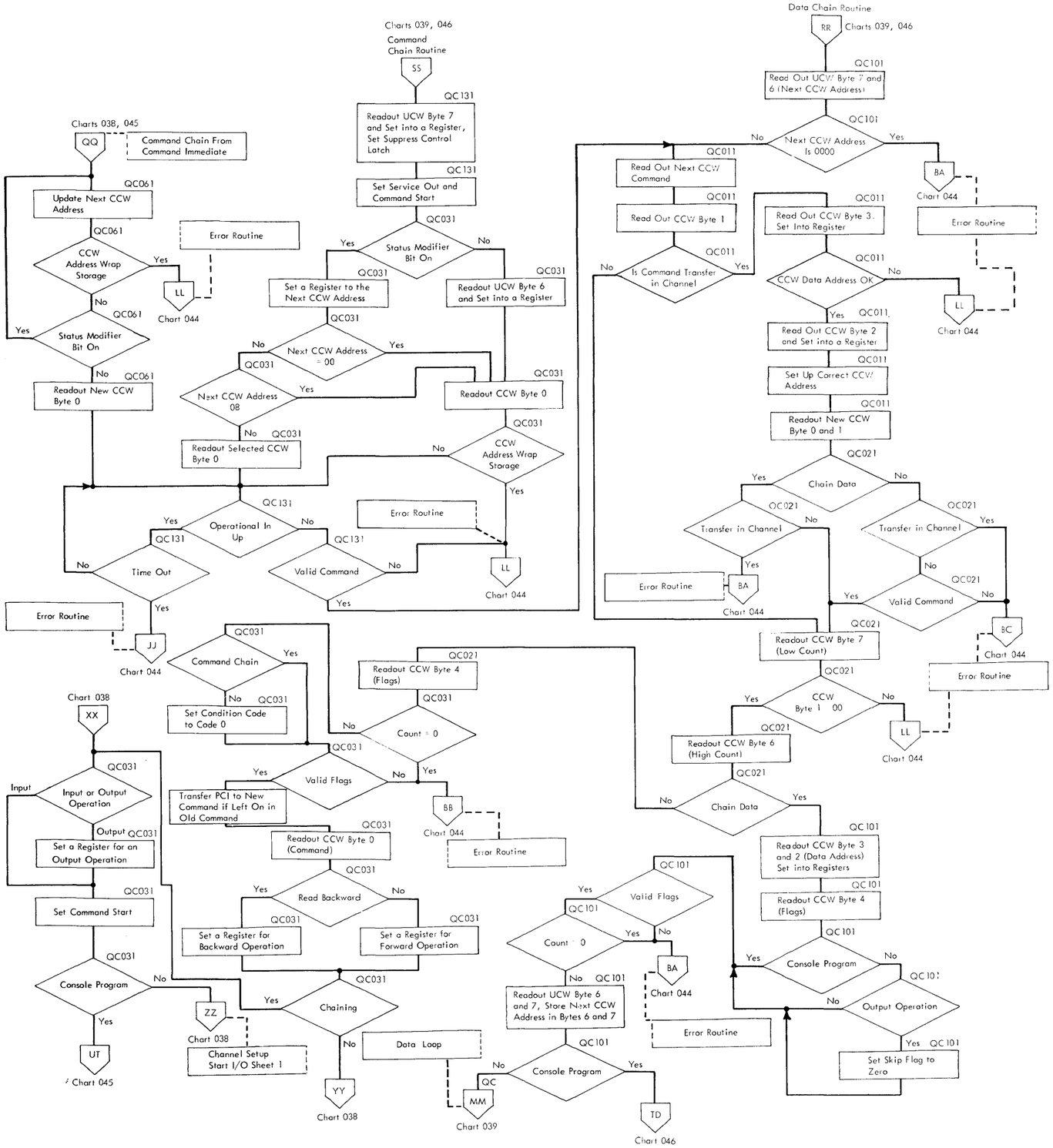


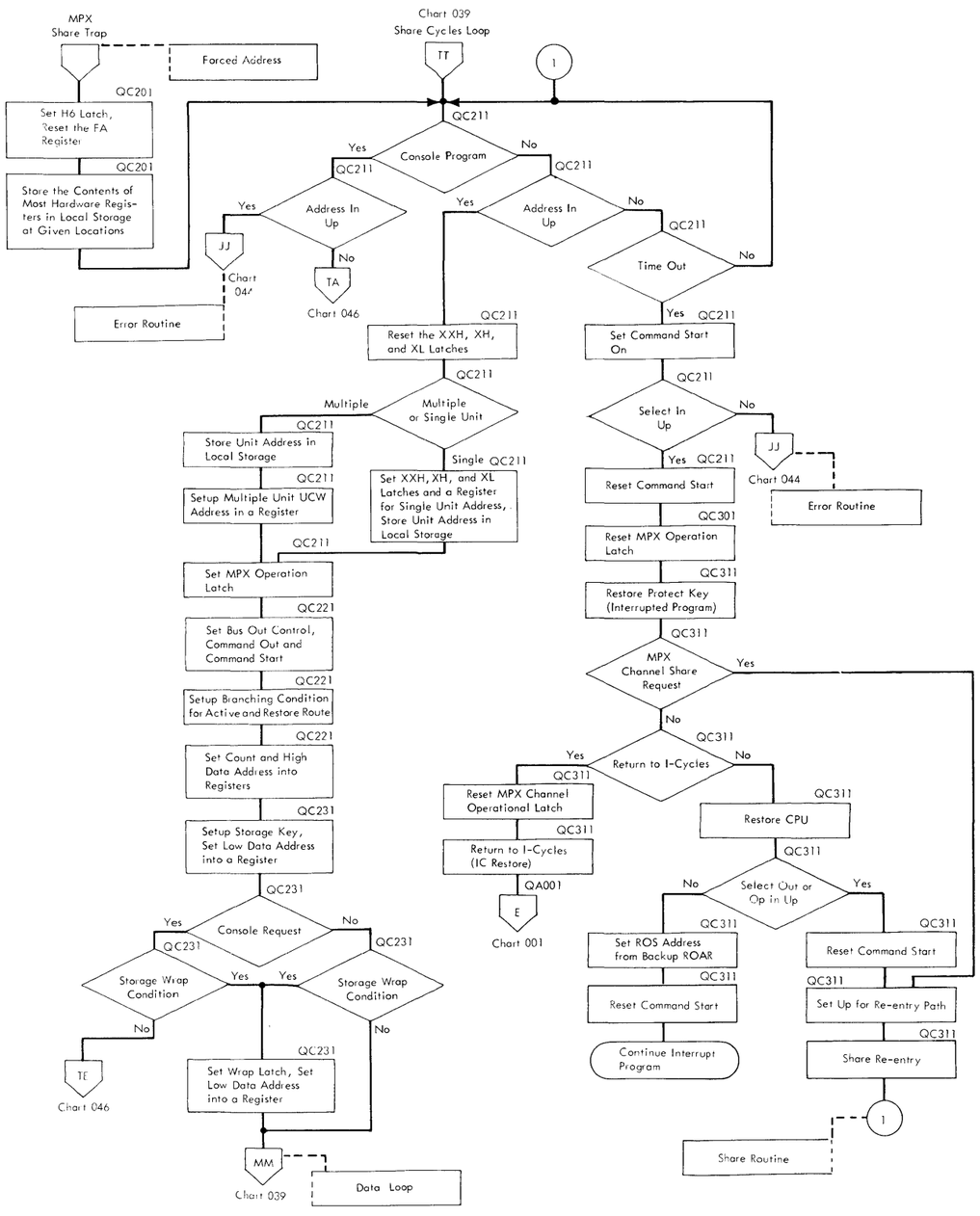
CLF 040 Test I/O - Interrupt to Store CSW


3
QC061
Unit Status = 0
Yes
No
QC071
Set Service Out and Command Start
QC141
Operational In Up
No
Yes
QC141
Time Out
No
QC451
Yes
Error Routine
JJ
Chart 044
1
QC151
Readout Condition Code Set to Code 0 and Store
QC151
Reset the FA Register
QC151
Return to I Cycle (IC Restore)
QA001
E
Chart 001
QC071
Set Unit Status into a Register
QC071
Set Service Out and Command Start
QC161
Operational In Up
No
4
Yes
QC071
Time Out
No
Yes
JJ
Chart 044
QC451
Error Routine
CA
Chart 040
Set Command Start
QC141
Test I/O or Interrupt
Test I/O
Interrupt
QC141
Readout Channel Status Byte (UCW Byte 0) Test Bits 3 and 4
QC141
Test I O or Halt I/O
Test I/O
Halt I O
QC141
Readout UCW Byte 4 (High Date Address Now Contains Unit Address
QC141
Bit 3 of UCW Byte 0 is a 1
Yes
No
QC141
Unit Address Match
No
Yes
QC151
Readout Condition Code Set to Code 2 and Store
QC151
Reset FA Register Return to I-Cycles
QA001
E
Chart 001
QC141
First Status Presented By Unit
No
Yes
1
KY
Chart 042
Halt I/O Routine
QC141
Readout Interrupt Buffer Store in a Register
QC161
Reset FA Register
QC141
Unit Status in Interrupt Buffer
No
Yes
CE
Chart 040
QC141
Readout Unit Status from Interrupt Buffer
4
QC161
Interrupt
Yes
No
QC161
Reset Command Start
QC161
Status Modifier Bit Only Bit Set
Yes
No
Chart 040
CC
Chart 040
CD
QC161
Reset H6
QC161
Reset H6
QC161
CSW Short Store
No
BD
Chart 044
QC401
Store Channel and Unit Status in CSW
QC151
Store Condition Code 1
QC151
Reset FA Register
QC151
Return to I-Cycles (IC Restore)
QA001
E
Chart 001
QC401
Readout UCW Byte 1 Set a Register to the Setting of PCI and Active Bits
QC401
Reset PCI Bit in UCW Byte 1
QC401
Active Bit On
No
Yes
QC401
Readout UCW Status Byte, Change Bits to CSW Format with the PCI Bit Reset, Store in a Register
QC401
Was PCI Bit On
No
Yes
QC401
Readout Status Byte from Register, Set PCI Bit on and Store
QC401
Active Bit On
No
Yes
QC411
Set all CSW Bytes to 00
QC411
Set CSW to
Byte 0 - Storage Protect
Byte 1 - Zeros
Byte 2 - Next CCW High Address
Byte 3 - Next CCW Low Address
Byte 6 - High Count
Byte 7 - Low Count
Reset MPX Interrupt Latch
QC401
Set CSW Byte 5 to Channel Status
QC401
Set CSW Byte 4 to Unit Status
BF
Chart 040
QC051
Address In Up
Yes
No
QC051
Unit Address Match
Yes
No
QC051
Time Out
No
Yes
JJ
Chart 044
QC451
Error Routine
JJ
Chart 044
QC051
Halt I O
No
Yes
KK
Chart 042
QC051
Set Bus Out Control, Command Out and Command Start
Chart 038
VV
QC051
Test I/O or Interrupt
No
Yes
UU
Chart 038
QC051
Test I/O to Stack Status
QC461 Yes
BE
Chart 044
No
Start I/O Routine
QC061
Status In Up
Yes
3
No
QC061
Time Out
Yes
QC451
JJ
Chart 044
No
Error Routine
HIO-Control Unit Busy
TIO-Error on SIO
TIO-Status in Interrupt Buffer
Yes
QC401
Is Active Bit to Be Reset
No
QC401
Status In Interrupt Buffer
No
Yes
QC401
Set UCW Byte 1 to 00
QC401
Set UCW Byte 1 to 00, Reset MPX Channel Interrupt Latch
QC401
Test I/O or I/O Interrupt
Test I/O
I/O Interrupt
S
Chart 007
QC151
Readout Condition Code Set to Code 1 and Store
QC151
Reset the FA Register
Return to I-Cycles (IC Restore)
QA001
E
Chart 001



CLF 042 MPX Halt I/O, Test Channel


Charts 038, 045
QQ
Command Chain From Command Immediate
QC061
Update Next CCW Address
QC061
CCW Address Wrap Storage
Yes
Error Routine
LL
Chart 044
No
QC061
Status Modifier Bit On
Yes
No
QC061
Readout New CCW Byte 0
Charts 039, 046
Command Chain Routine
SS
QC131
Readout UCW Byte 7 and Set into a Register, Set Suppress Control Latch
QC131
Set Service Out and Command Start
QC031
Status Modifier Bit On
Yes
No
QC031
Set a Register to the Next CCW Address
QC031
Readout UCW Byte 6 and Set into a Register
QC031
Next CCW Address = 00
No
Yes
QC031
Next CCW Address 08
Yes
No
QC031
Readout Selected CCW Byte 0
QC031
Readout CCW Byte 0
QC031
CCW Address Wrap Storage
No
Yes
QC131
Operational In Up
Yes
No
QC131
Time Out
No
Yes
QC131
Valid Command
No
Yes
Error Routine
LL
Chart 044
Error Routine
JJ
Chart 044
QC031
Command Chain
Yes
No
QC031
Set Condition Code to Code 0
Chart 038
XX
QC031
Input or Output Operation
Input
Output
QC031
Set a Register for an Output Operation
QC031
Set Command Start
QC031
Console Program
No
Yes
UT
Chart 045
ZZ
Chart 038
Channel Setup Start I/O Sheet 1
QC031
Chaining
Yes
No
YY
Chart 038
Data Chain Routine
RR
Charts 039, 046
QC101
Read Out UCW Byte 7 and 6 (Next CCW Address)
QC101
Next CCW Address Is 0000
No
Yes
BA
Chart 044
QC011
Read Out Next CCW Command
QC011
Read Out CCW Byte 1
QC011
Is Command Transfer in Channel
No
Yes
QC011
Read Out CCW Byte 3. Set Into Register
QC011
CCW Data Address OK
No
Yes
LL
Chart 044
Error Routine
QC011
Read Out CCW Byte 2 and Set into a Register
QC011
Set Up Correct CCW Address
QC011
Readout New CCW Byte 0 and 1
QC021
Chain Data
Yes
No
QC021
Transfer in Channel
No
Yes
Error Routine
BA
Chart 044
QC021
Transfer in Channel
Yes
No
QC021
Valid Command
Yes
No
BC
Chart 044
Error Routine
QC021
Readout CCW Byte 7 (Low Count)
QC021
CCW Byte 1 00
Yes
No
LL
Chart 044
QC021
Readout CCW Byte 6 (High Count)
QC021
Chain Data
No
Yes
QC021
Readout CCW Byte 4 (Flags)
QC031
Count = 0
No
Yes
QC031
Valid Flags
Yes
No
BB
Chart 044
Transfer PCI to New Command if Left On in Old Command
Error Routine
QC031
Readout CCW Byte 0 (Command)
QC031
Read Backward
Yes
No
QC031
Set a Register for Backward Operation
QC031
Set a Register for Forward Operation
QC101
Valid Flags
Yes
No
QC101
Count = 0
Yes
No
BA
Chart 044
Error Routine
QC101
Readout UCW Byte 6 and 7, Store Next CCW Address in Bytes 6 and 7
QC101
Console Program
No
Yes
QC
MM
Chart 039
TD
Chart 046
QC101
Readout CCW Byte 3 and 2 (Data Address) Set into Registers
QC101
Readout CCW Byte 4 (Flags)
QC101
Console Program
Yes
No
QC101
Output Operation
No
Yes
QC101
Set Skip Flag to Zero
Data Loop


MPX Share Trap
Forced Address
QC201
Set H6 Latch, Reset the FA Register
QC201
Store the Contents of Most Hardware Registers in Local Storage at Given Locations
Error Routine
Chart 039 Share Cycles Loop
TT
1
QC211
Console Program
Yes
No
QC211
Address In Up
Yes
No
JJ
Chart 044
TA
Chart 046
QC211
Address In Up
Yes
No
QC211
Time Out
No
Yes
QC211
Reset the XXH, XH, and XL Latches
QC211
Multiple or Single Unit
Multiple
Single QC211
QC211
Store Unit Address in Local Storage
QC211
Setup Multiple Unit UCW Address in a Register
QC211
Set XXH, XH, and XL Latches and a Register for Single Unit Address, Store Unit Address in Local Storage
QC211
Set MPX Operation Latch
QC221
Set Bus Out Control, Command Out and Command Start
QC221
Setup Branching Condition for Active and Restore Route
QC221
Set Count and High Data Address into Registers
QC231
Setup Storage Key, Set Low Data Address into a Register
QC231
Console Request
Yes
No
QC231
Storage Wrap Condition
Yes
No
TE
Chart 046
QC231
Storage Wrap Condition
Yes
No
QC231
Set Wrap Latch, Set Low Data Address into a Register
MM
Chart 039
Data Loop
QC211
Set Command Start On
QC211
Select In Up
Yes
No
JJ
Chart 044
Error Routine
QC211
Reset Command Start
QC301
Reset MPX Operation Latch
QC311
Restore Protect Key (Interrupted Program)
QC311
MPX Channel Share Request
Yes
No
QC311
Return to 1-Cycles
Yes
No
QC311
Reset MPX Channel Operational Latch
QC311
Return to 1-Cycles (IC Restore)
QA001
E
Chart 001
QC311
Restore CPU
QC311
Select Out or Op in Up
No
Yes
QC311
Set ROS Address from Backup ROAR
QC311
Reset Command Start
Continue Interrupt Program
QC311
Reset Command Start
QC311
Set Up for Re-entry Path
QC311
Share Re-entry
1
Share Routine

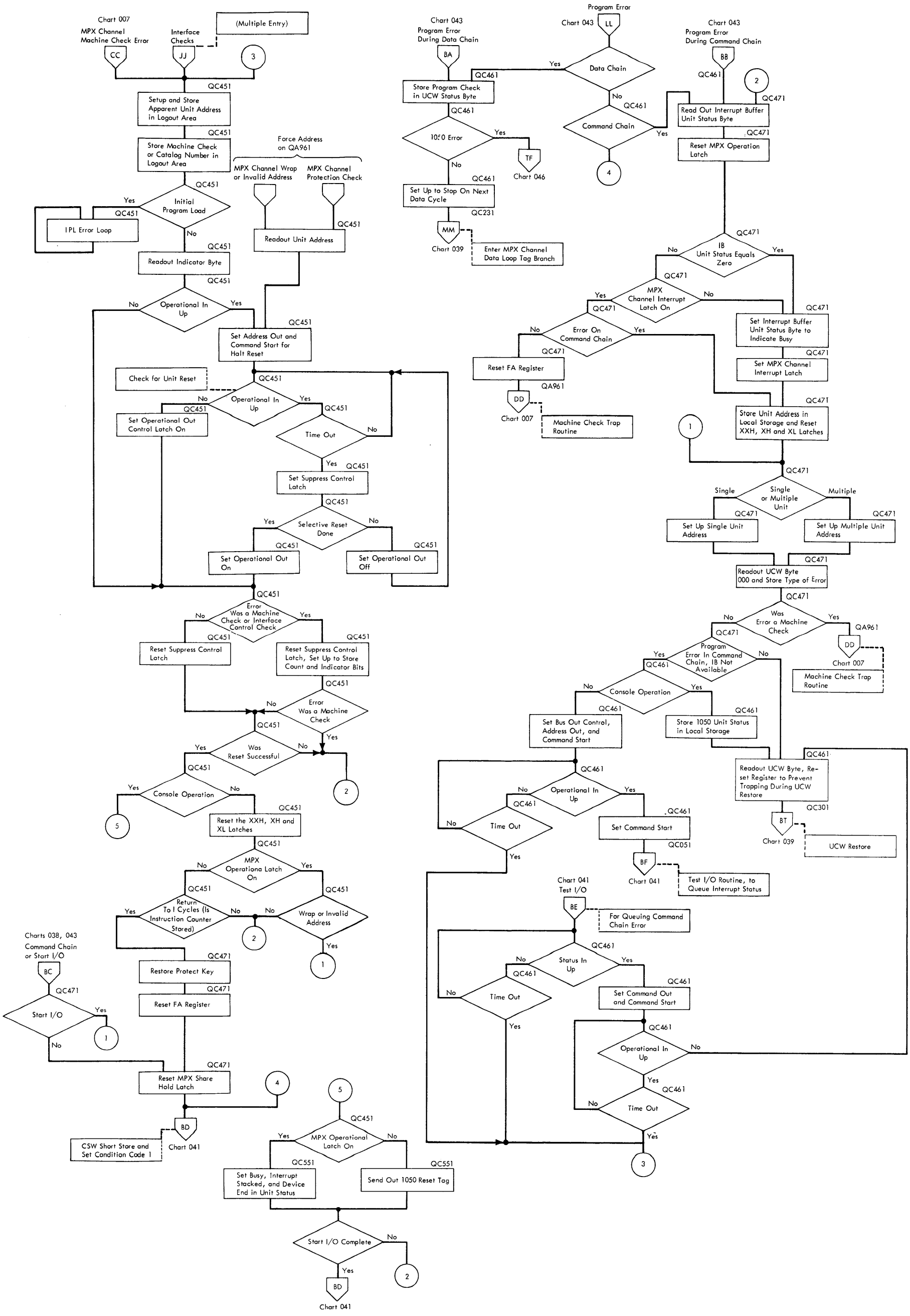
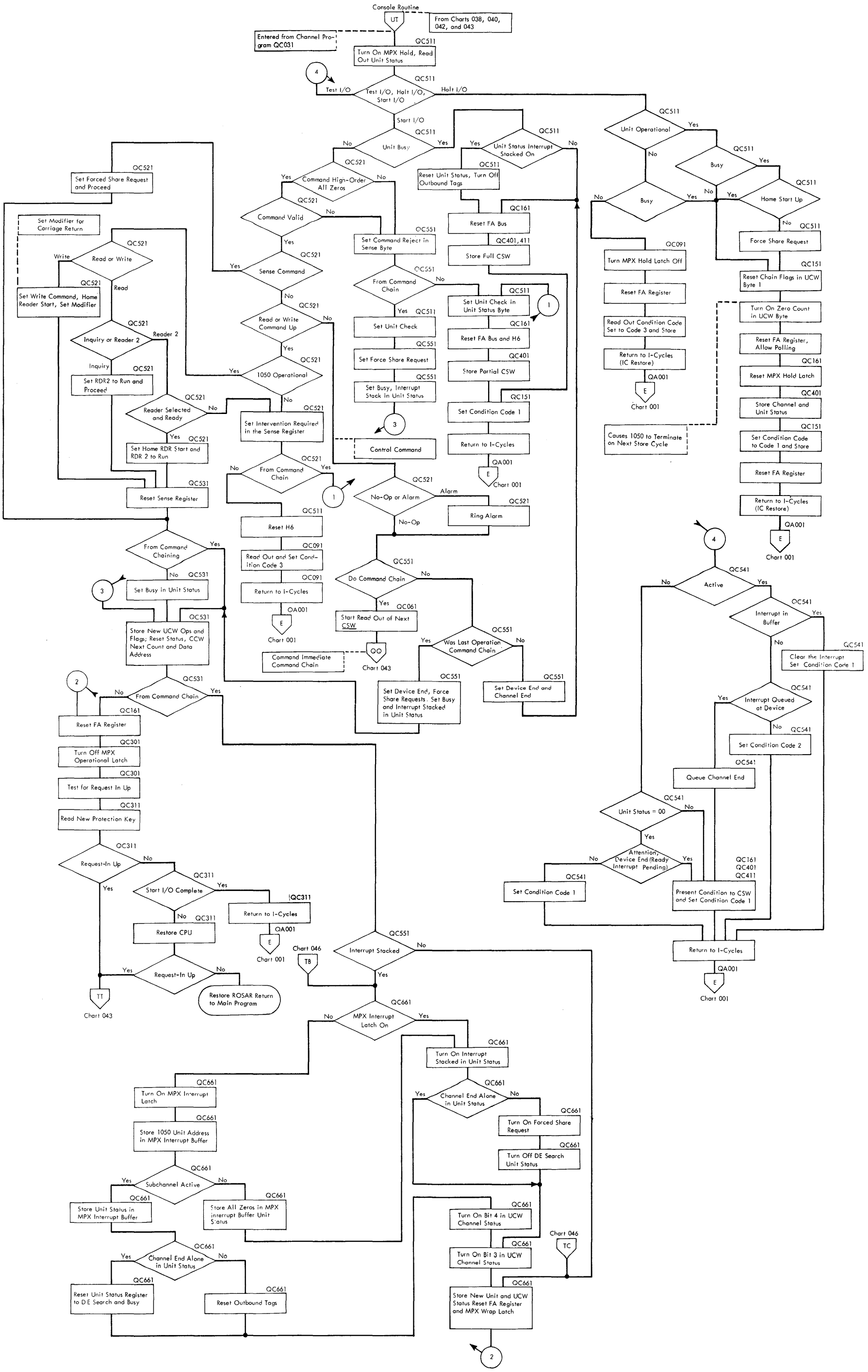


Chart 007
MPX Channel Machine Check Error
CC
Interface Checks
JJ
(Multiple Entry)
3
QC451
Setup and Store Apparent Unit Address in Logout Area
Store Machine Check or Catalog Number in Logout Area
Force Address on QA961
MPX Channel Wrap or Invalid Address
MPX Channel Protection Check
Initial Program Load
Yes
IPL Error Loop
No
Readout Unit Address
Readout Indicator Byte
Operational In Up
Set Address Out and Command Start for Halt Reset
Check for Unit Reset
Set Operational Out Control Latch On
Time Out
Set Suppress Control Latch
Selective Reset Done
Set Operational Out On
Set Operational Out Off
Error Was a Machine Check or Interface Control Check
Reset Suppress Control Latch
Reset Suppress Control Latch, Set Up to Store Count and Indicator Bits
Error Was a Machine Check
Was Reset Successful
Console Operation
5
2
Reset the XXH, XH and XL Latches
MPX Operationa Latch On
Return To I Cycles (Is Instruction Counter Stored)
Wrap or Invalid Address
1
Restore Protect Key
Reset FA Register
Charts 038, 043
Command Chain or Start I/O
BC
Start I/O
Reset MPX Share Hold Latch
4
BD
CSW Short Store and Set Condition Code 1
Chart 041
MPX Operational Latch On
Set Busy, Interrupt Stacked, and Device End in Unit Status
Send Out 1050 Reset Tag
Start I/O Complete
Chart 043
Program Error During Data Chain
BA
Store Program Check in UCW Status Byte
1050 Error
TF
Chart 046
Set Up to Stop On Next Data Cycle
QC231
MM
Chart 039
Enter MPX Channel Data Loop Tag Branch
Program Error
Chart 043
LL
Data Chain
Command Chain
4
Chart 043
Program Error During Command Chain
BB
Read Out Interrupt Buffer Unit Status Byte
Reset MPX Operation Latch
IB Unit Status Equals Zero
MPX Channel Interrupt Latch On
Error On Command Chain
Reset FA Register
DD
Chart 007
Machine Check Trap Routine
Set Interrupt Buffer Unit Status Byte to Indicate Busy
Set MPX Channel Interrupt Latch
Store Unit Address in Local Storage and Reset XXH, XH and XL Latches
Single or Multiple Unit
Set Up Single Unit Address
Set Up Multiple Unit Address
Readout UCW Byte 000 and Store Type of Error
Was Error a Machine Check
Program Error In Command Chain, IB Not Available
Console Operation
Set Bus Out Control, Address Out, and Command Start
Store 1050 Unit Status in Local Storage
Readout UCW Byte, Reset Register to Prevent Trapping During UCW Restore
BT
Chart 039
UCW Restore
Operational In Up
Time Out
Set Command Start
BF
Chart 041
Test I/O Routine, to Queue Interrupt Status
Chart 041
Test I/O
BE
For Queuing Command Chain Error
Status In Up
Set Command Out and Command Start
Operational In Up
Time Out
3


Console Routine
UT
From Charts 038, 040, 042, and 043
Entered from Channel Program QC031
QC511
Turn On MPX Hold, Read Out Unit Status
4
QC511
Test I/O, Halt I/O, Start I/O
Test I/O
Halt I/O
Start I/O
QC511
Unit Busy
No
Yes
QC511
Unit Status Interrupt Stacked On
Yes
No
QC511
Reset Unit Status, Turn Off Outbound Tags
QC511
Unit Operational
Yes
No
QC511
Busy
Yes
No
QC511
Busy
No
Yes
QC511
Home Start Up
No
QC521
Command High-Order All Zeros
Yes
No
QC521
Command Valid
No
Yes
QC521
Sense Command
Yes
No
QC521
Read or Write Command Up
No
Yes
QC521
1050 Operational
Yes
No
QC521
Set Forced Share Request and Proceed
QC521
Read or Write
Write
Read
QC521
Set Write Command, Home Reader Start, Set Modifier
Set Modifier for Carriage Return
QC521
Inquiry or Reader 2
Reader 2
Inquiry
QC521
Set RDR2 to Run and Proceed
QC521
Reader Selected and Ready
No
Yes
QC521
Set Home RDR Start and RDR 2 to Run
QC521
Set Intervention Required in the Sense Register
QC551
Set Command Reject in Sense Byte
QC551
From Command Chain
No
Yes
QC511
Set Unit Check
QC551
Set Force Share Request
QC551
Set Busy, Interrupt Stack in Unit Status
3
Control Command
QC521
From Command Chain
No
Yes
1
QC511
Reset H6
QC091
Read Out and Set Condition Code 3
QC091
Return to I-Cycles
QA001
E
Chart 001
QC521
No-Op or Alarm
Alarm
No-Op
QC521
Ring Alarm
QC551
Do Command Chain
No
Yes
QC061
Start Read Out of Next CSW
QQ
Chart 043
Command Immediate Command Chain
QC551
Was Last Operation Command Chain
Yes
No
QC551
Set Device End, Force Share Requests. Set Busy and Interrupt Stacked in Unit Status
QC551
Set Device End and Channel End
QC161
Reset FA Bus
QC401,411
Store Full CSW
QC511
Set Unit Check in Unit Status Byte
1
QC161
Reset FA Bus and H6
QC401
Store Partial CSW
QC151
Set Condition Code 1
Return to I-Cycles
QA001
E
Chart 001
QC091
Turn MPX Hold Latch Off
Reset FA Register
Read Out Condition Code Set to Code 3 and Store
Return to I-Cycles (IC Restore)
QA001
E
Chart 001
Causes 1050 to Terminate on Next Store Cycle
QC511
Force Share Request
QC151
Reset Chain Flags in UCW Byte 1
Turn On Zero Count in UCW Byte
Reset FA Register, Allow Polling
QC161
Reset MPX Hold Latch
QC401
Store Channel and Unit Status
QC151
Set Condition Code to Code 1 and Store
Reset FA Register
Return to I-Cycles (IC Restore)
QA001
E
Chart 001
QC531
Reset Sense Register
QC531
From Command Chaining
Yes
No
3
QC531
Set Busy in Unit Status
QC531
Store New UCW Ops and Flags; Reset Status, CCW Next Count and Data Address
2
QC531
From Command Chain
No
Yes
QC161
Reset FA Register
QC301
Turn Off MPX Operational Latch
QC301
Test for Request In Up
QC311
Read New Protection Key
QC311
Request-In Up
No
Yes
QC311
Start I/O Complete
Yes
No
QC311
Return to I-Cycles
QA001
E
Chart 001
QC311
Restore CPU
Yes
No
Request-In Up
TT
Chart 043
Restore ROSAR Return to Main Program
4
QC541
Active
No
Yes
QC541
Interrupt in Buffer
Yes
No
QC541
Clear the Interrupt Set Condition Code 1
QC541
Interrupt Queued at Device
Yes
No
QC541
Set Condition Code 2
QC541
Queue Channel End
QC541
Unit Status = 00
No
Yes
Attention, Device End (Ready Interrupt Pending)
No
Yes
QC541
Set Condition Code 1
QC161
QC401
QC411
Present Condition to CSW and Set Condition Code 1
Return to I-Cycles
QA001
E
Chart 001
QC551
Interrupt Stacked
No
Yes
Chart 046
TB
QC661
MPX Interrupt Latch On
No
Yes
QC661
Turn On Interrupt Stacked in Unit Status
QC661
Channel End Alone in Unit Status
Yes
No
QC661
Turn On Forced Share Request
QC661
Turn Off DE Search Unit Status
QC661
Turn On MPX Interrupt Latch
QC661
Store 1050 Unit Address in MPX Interrupt Buffer
QC661
Subchannel Active
Yes
No
QC661
Store Unit Status in MPX Interrupt Buffer
QC661
Store All Zeros in MPX interrupt Buffer Unit Status
QC661
Channel End Alone in Unit Status
Yes
No
QC661
Reset Unit Status Register to DE Search and Busy
QC661
Reset Outbound Tags
QC661
Turn On Bit 4 in UCW Channel Status
QC661
Turn On Bit 3 in UCW Channel Status
Chart 046
TC
QC661
Store New Unit and UCW Status Reset FA Register and MPX Wrap Latch
2

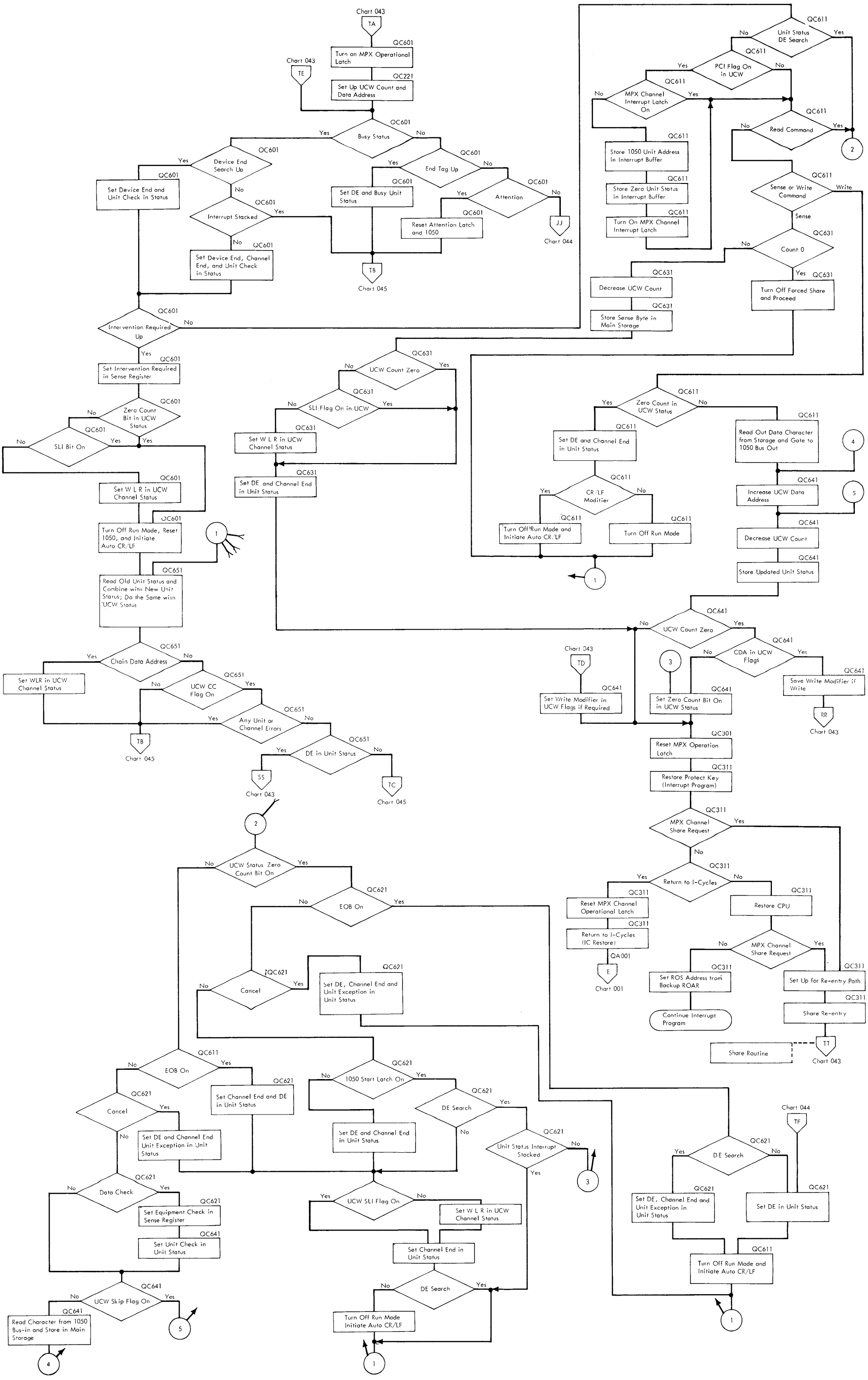
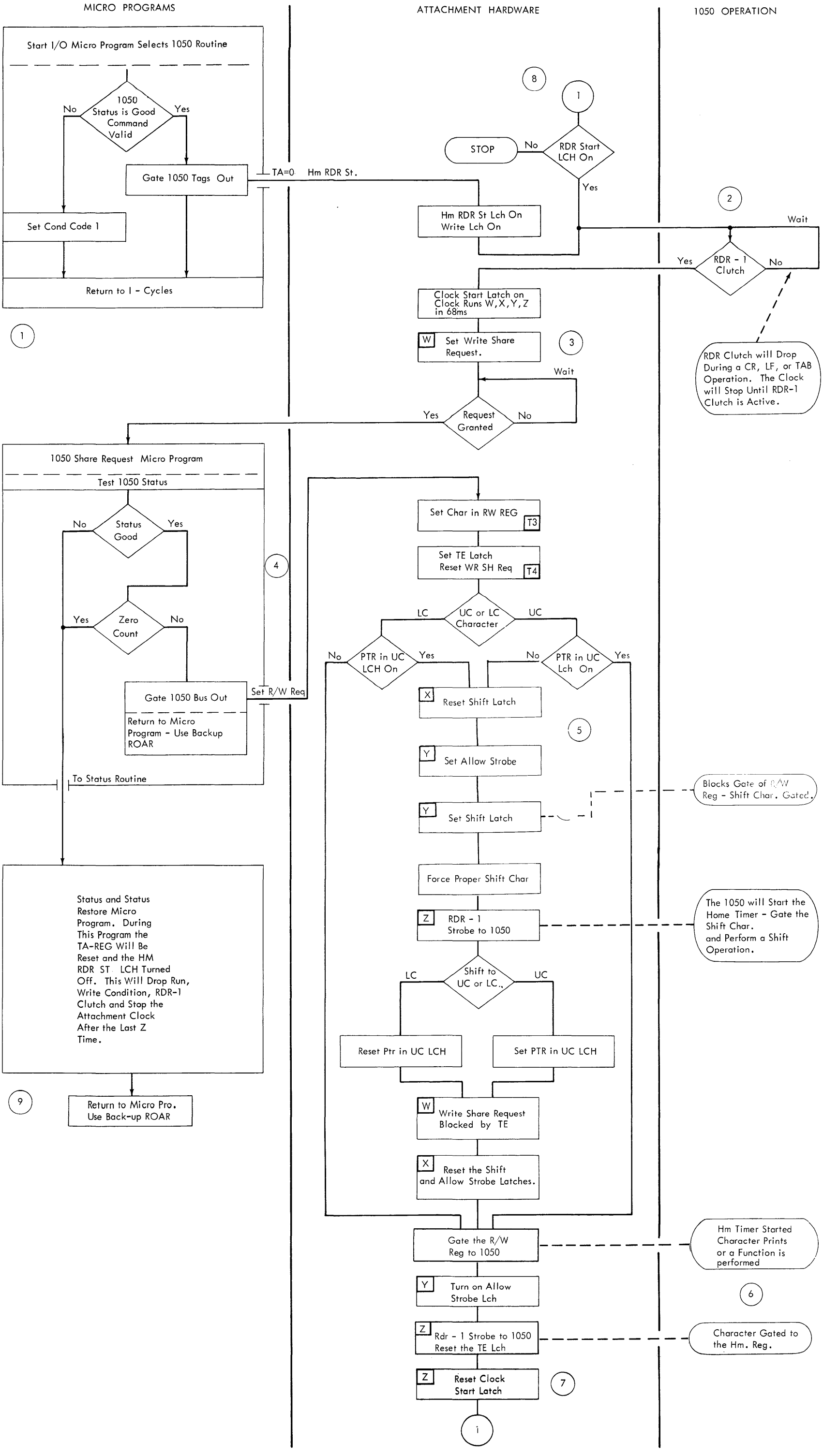
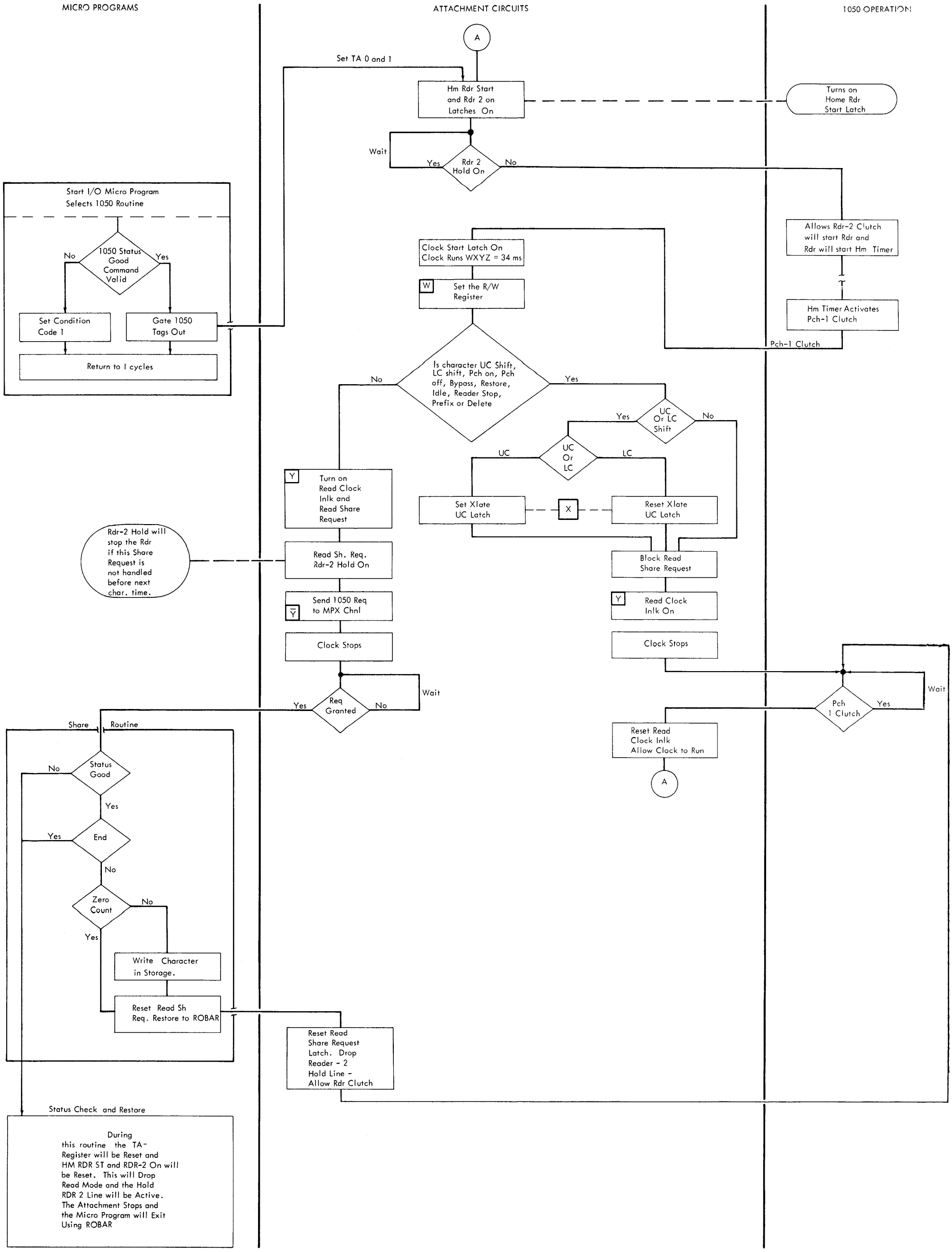


Chart 043
TA
QC601
Turn on MPX Operational Latch
Chart 043
TE
QC221
Set Up UCW Count and Data Address
QC601
Busy Status
Yes
No
QC601
Device End Search Up
Yes
QC601
Set Device End and Unit Check in Status
No
QC601
Interrupt Stacked
Yes
No
QC601
Set Device End, Channel End, and Unit Check in Status
QC601
End Tag Up
Yes
No
QC601
Set DE and Busy Unit Status
QC601
Attention
Yes
No
QC601
Reset Attention Latch and 1050
JJ
Chart 044
TB
Chart 045
QC601
Intervention Required Up
No
Yes
QC601
Set Intervention Required in Sense Register
QC601
Zero Count Bit in UCW Status
No
Yes
QC601
SLI Bit On
No
Yes
QC601
Set W L R in UCW Channel Status
QC601
Turn Off Run Mode, Reset 1050, and Initiate Auto CR/LF
1
QC651
Read Old Unit Status and Combine with New Unit Status; Do the Same with UCW Status
QC651
Chain Data Address
Yes
No
Set WLR in UCW Channel Status
QC651
UCW CC Flag On
No
Yes
QC651
Any Unit or Channel Errors
Yes
No
TB
Chart 045
QC651
DE in Unit Status
Yes
No
SS
Chart 043
TC
Chart 045
2
QC631
UCW Count Zero
No
Yes
QC631
SLI Flag On in UCW
No
Yes
QC631
Set W L R in UCW Channel Status
QC631
Set DE and Channel End in Unit Status
QC621
EOB On
No
Yes
QC621
Cancel
No
Yes
QC621
Set DE, Channel End and Unit Exception in Unit Status
QC611
EOB On
No
Yes
QC621
Set Channel End and DE in Unit Status
QC621
Cancel
Yes
No
QC621
Set DE and Channel End Unit Exception in Unit Status
QC621
Data Check
No
Yes
QC621
Set Equipment Check in Sense Register
QC641
Set Unit Check in Unit Status
QC641
UCW Skip Flag On
No
Yes
QC641
Read Character from 1050 Bus-in and Store in Main Storage
4
5
QC621
1050 Start Latch On
No
Yes
QC621
Set DE and Channel End in Unit Status
QC621
DE Search
Yes
No
QC621
Unit Status Interrupt Stacked
No
Yes
3
QC621
UCW SLI Flag On
Yes
No
Set W L R in UCW Channel Status
Set Channel End in Unit Status
DE Search
No
Yes
Turn Off Run Mode Initiate Auto CR/LF
1
QC611
Unit Status DE Search
No
Yes
QC611
PCI Flag On in UCW
Yes
No
QC611
MPX Channel Interrupt Latch On
No
Yes
QC611
Store 1050 Unit Address in Interrupt Buffer
QC611
Store Zero Unit Status in Interrupt Buffer
QC611
Turn On MPX Channel Interrupt Latch
QC611
Read Command
No
Yes
2
QC611
Sense or Write Command
Write
Sense
QC631
Count 0
No
Yes
QC631
Turn Off Forced Share and Proceed
QC631
Decrease UCW Count
QC631
Store Sense Byte in Main Storage
QC611
Zero Count in UCW Status
Yes
No
QC611
Set DE and Channel End in Unit Status
QC611
CR/LF Modifier
Yes
No
QC611
Turn Off Run Mode and Initiate Auto CR/LF
QC611
Turn Off Run Mode
1
QC611
Read Out Data Character from Storage and Gate to 1050 Bus Out
4
QC641
Increase UCW Data Address
5
QC641
Decrease UCW Count
QC641
Store Updated Unit Status
QC641
UCW Count Zero
No
Yes
Chart 043
TD
QC641
Set Write Modifier in UCW Flags if Required
3
QC641
CDA in UCW Flags
No
Yes
QC641
Save Write Modifier if Write
RR
Chart 043
QC641
Set Zero Count Bit On in UCW Status
QC301
Reset MPX Operation Latch
QC311
Restore Protect Key (Interrupt Program)
QC311
MPX Channel Share Request
Yes
No
QC311
Return to I-Cycles
Yes
No
QC311
Reset MPX Channel Operational Latch
QC311
Return to I-Cycles (IC Restore)
QA001
E
Chart 001
QC311
Restore CPU
QC311
MPX Channel Share Request
No
Yes
QC311
Set ROS Address from Backup ROAR
Continue Interrupt Program
QC311
Set Up for Re-entry Path
QC311
Share Re-entry
TT
Share Routine
Chart 043
Chart 044
TF
QC621
DE Search
Yes
No
QC621
Set DE, Channel End and Unit Exception in Unit Status
QC621
Set DE in Unit Status
QC611
Turn Off Run Mode and Initiate Auto CR/LF
1


MICRO PROGRAMS
ATTACHMENT HARDWARE
1050 OPERATION
Start I/O Micro Program Selects 1050 Routine
1050 Status is Good Command Valid
No
Yes
Gate 1050 Tags Out
TA=0 Hm RDR St.
Set Cond Code 1
Return to I - Cycles
1
8
1
STOP
No
RDR Start LCH On
Yes
2
Wait
Hm RDR St Lch On
Write Lch On
Yes
RDR - 1 Clutch
No
Clock Start Latch on Clock Runs W,X,Y,Z in 68ms
W
Set Write Share Request.
3
Wait
Yes
Request Granted
No
RDR Clutch will Drop During a CR, LF, or TAB Operation. The Clock will Stop Until RDR-1 Clutch is Active.
1050 Share Request Micro Program
Test 1050 Status
No
Status Good
Yes
4
Yes
Zero Count
No
Gate 1050 Bus Out
Set R/W Req
Return to Micro Program - Use Backup ROAR
To Status Routine
Set Char in RW REG
T3
Set TE Latch Reset WR SH Req
T4
LC
UC or LC Character
UC
No
PTR in UC LCH On
Yes
No
PTR in UC Lch On
Yes
X
Reset Shift Latch
5
Y
Set Allow Strobe
Blocks Gate of R/W Reg - Shift Char. Gated.
Y
Set Shift Latch
Force Proper Shift Char
Z
RDR - 1 Strobe to 1050
The 1050 will Start the Home Timer - Gate the Shift Char. and Perform a Shift Operation.
LC
Shift to UC or LC.,
UC
Reset Ptr in UC LCH
Set PTR in UC LCH
W
Write Share Request Blocked by TE
X
Reset the Shift and Allow Strobe Latches.
Status and Status Restore Micro Program. During This Program the TA-REG Will Be Reset and the HM RDR ST LCH Turned Off. This Will Drop Run, Write Condition, RDR-1 Clutch and Stop the Attachment Clock After the Last Z Time.
9
Return to Micro Pro. Use Back-up ROAR
Gate the R/W Reg to 1050
Hm Timer Started Character Prints or a Function is performed
Y
Turn on Allow Strobe Lch
6
Z
Rdr - 1 Strobe to 1050 Reset the TE Lch
Character Gated to the Hm. Reg.
Z
Reset Clock Start Latch
7
i


MICRO PROGRAMS
ATTACHMENT CIRCUITS
1050 OPERATION
A
Set TA 0 and 1
Hm Rdr Start and Rdr 2 on Latches On
Turns on Home Rdr Start Latch
Wait
Yes
Rdr 2 Hold On
No
Start I/O Micro Program Selects 1050 Routine
No
1050 Status Good Command Valid
Yes
Set Condition Code 1
Gate 1050 Tags Out
Return to I cycles
Allows Rdr-2 Clutch will start Rdr and Rdr will start Hm Timer
Clock Start Latch On Clock Runs WXYZ = 34 ms
W
Set the R/W Register
Hm Timer Activates Pch-1 Clutch
Pch-1 Clutch
Is character UC Shift, LC shift, Pch on, Pch off, Bypass, Restore, Idle, Reader Stop, Prefix or Delete
No
Yes
Yes
UC Or LC Shift
No
UC
UC Or LC
LC
Y
Turn on Read Clock Inlk and Read Share Request
Set Xlate UC Latch
X
Reset Xlate UC Latch
Rdr-2 Hold will stop the Rdr if this Share Request is not handled before next char. time.
Read Sh. Req. Rdr-2 Hold On
Block Read Share Request
Y
Send 1050 Req to MPX Chnl
Y
Read Clock Inlk On
Clock Stops
Clock Stops
Wait
Yes
Req Granted
No
Pch 1 Clutch
Yes
Wait
Share
Routine
Reset Read Clock Inlk Allow Clock to Run
A
No
Status Good
Yes
Yes
End
No
No
Zero Count
Yes
Write Character in Storage.
Reset Read Sh Req. Restore to ROBAR
Reset Read Share Request Latch. Drop Reader - 2 Hold Line - Allow Rdr Clutch
Status Check and Restore
During this routine the TA-Register will be Reset and HM RDR ST and RDR-2 On will be Reset. This will Drop Read Mode and the Hold RDR 2 Line will be Active. The Attachment Stops and the Micro Program will Exit Using ROBAR

MICRO PROGRAMS

ATTACHMENT CIRCUITS

1050 OPERATION

Operator wishes to send Information To CPU Presses Request Key

Sets Attention Latch
Turns On 1050 SH Req.

Request Granted — Yes / No — Wait

Share Request Program and Status Restore. Set Up I/O. Interrupt with Attention Bit On in CSW. This will Cause a Check of the CSW and Attention will Cause a Start I/O.

Will Reset Attention Lch & 1050

Start I/O U Program
Selects 1050 Routine

1050 Status Good Command Valid — No / Yes

Set Condition Code

Gate 1050 Tags Out

Set TA-1 and TA-3

Return to 1 Cycles

Turn On RDR - 2 On Lch
Turn On Proceed Lch
Set Read Inq Mode

Proceed

1

Light Proceed Light
Unlock Keyboard

Operator Depresses a Key to Send a Character

Home Timer Develops Pch - 1 Clutch.

Pch-1 Clutch

Clock Start Latch on Clock
Runs W,X,Y,Z, = 34 ms

W Read/Write Reg Set

Is Character UC Shift, LC Shift, Pch On, Pch Off, Bypass, Restore, Idle, Reader Stop Prefix or Delete — No / Yes

UC or LC Shift — Yes / No

UC or LC — UC / LC

Set X late UC Latch — X — Reset Xlate UC Latch

The Translate UC Latch is used with the Read Translator for Proper EBCDI Code

Block Read Sh Request

Y Read Clock Intlk On

Clock Stops

Pch 1 Clutch — No / Yes — Wait

Reset Read Clock Intlk - will Allow Clk to Run

1

1050 RD Share Request

Status Good — No / Yes

EOB EOT or Cancel — Yes / No

Zero Cnt — No / Yes

Write Character in Core

Reset Rd Sh Request Restore to CPU Backup ROAR

To Status Restore

Y Turn On Read Clock Intlk and Read Share Request

Read Share Request Drops Proceed Locks KBD

$\overline{Y}$ Send 1050 Req to MPX Ch.

Clock Stops

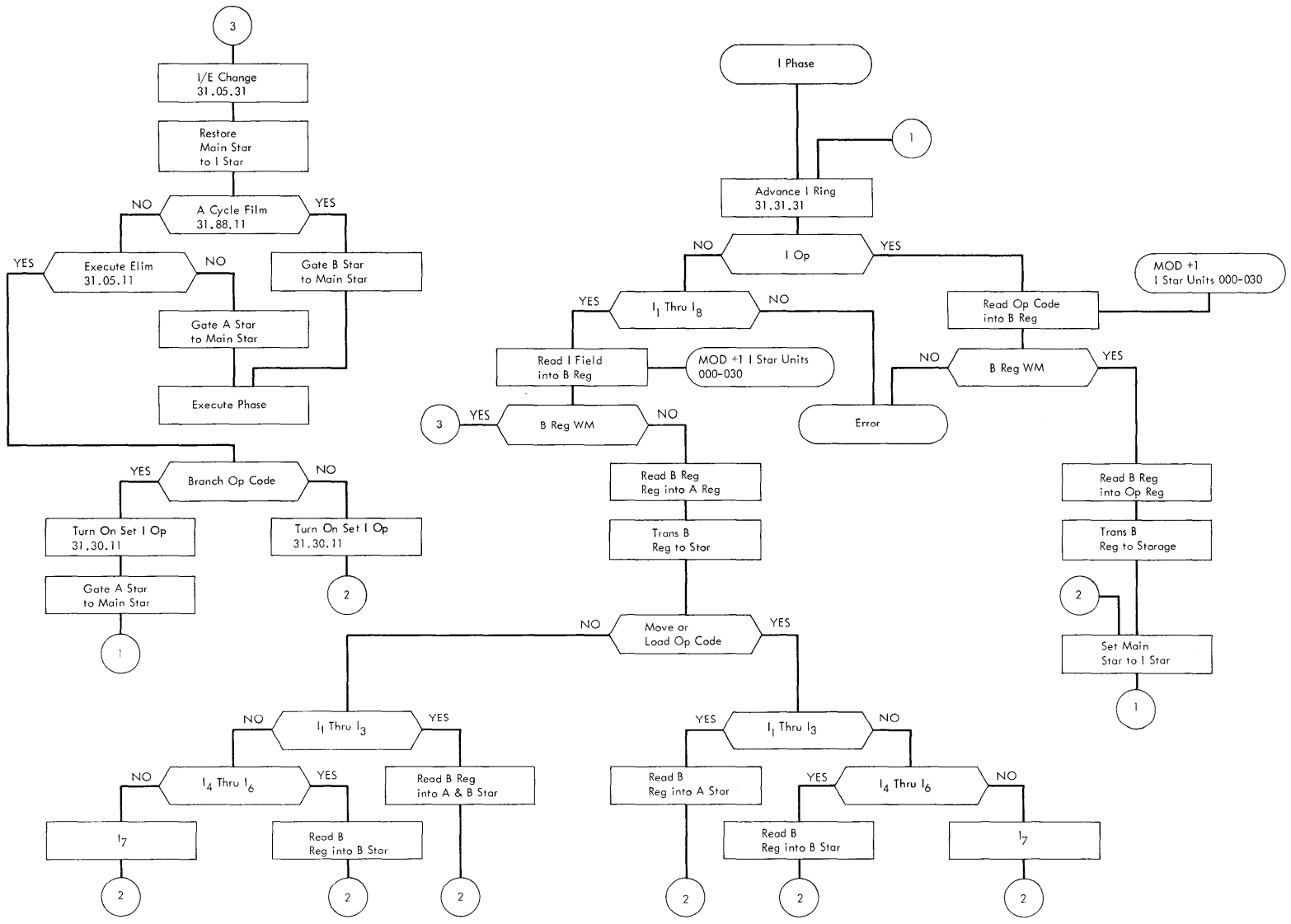
Req Granted — Yes / No — Wait

Reset Read Sh Request
Latch Activate Proceed to 1051 - Light Proceed and Unlock KBD.

Status Restore

During this Routine the TA Register will be Reset and the Proceed Lch will be Turned Off. This will Drop Proceed in the 1051 and Stop the Attachment.

Return to Micro Program - Use Backup ROAR

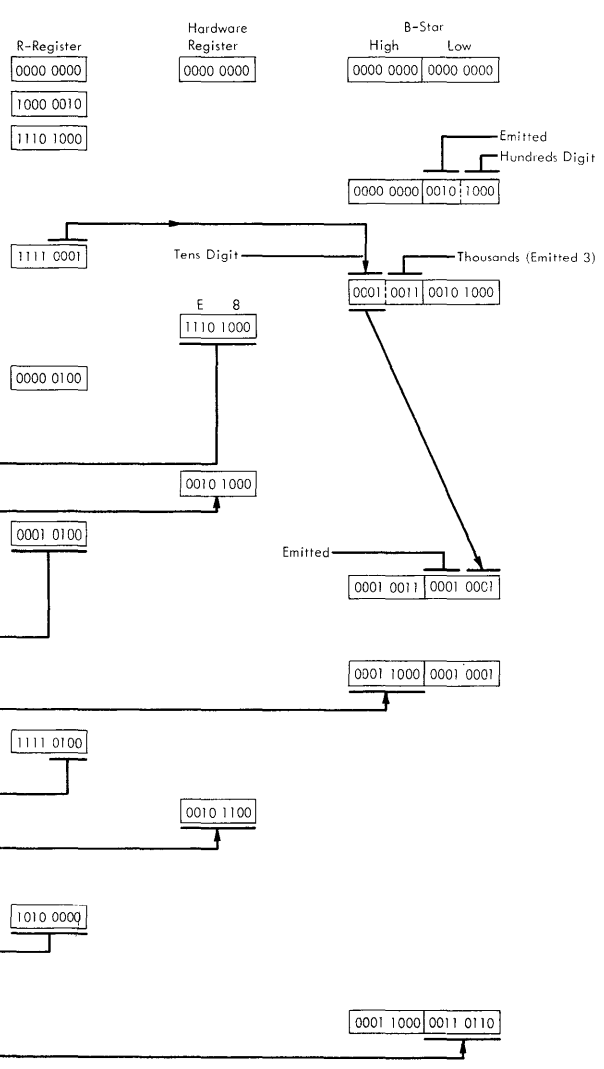


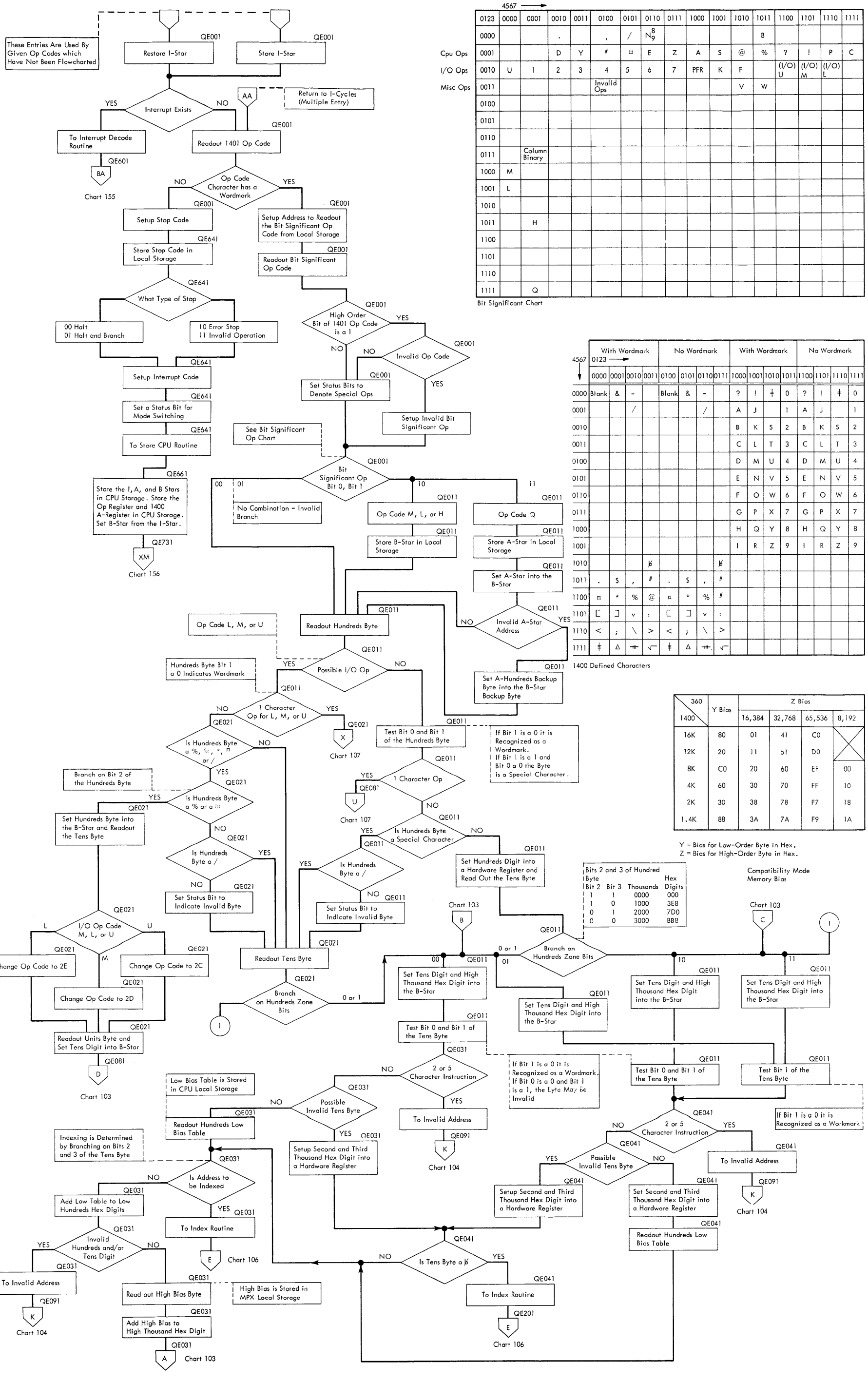
Example for A-Star or B-Star Address Development During I-Phase of 1401 Compatibility Feature on the 2030.

Assume the 2030 has 16,384 Positions of Storage and the 1401 Program is for a 12,000 Positions of Storage 1401. The Bias is 1120

Instruction is B Y14 E A

1. Read Op Code
2. Readout Hundreds Byte
3. Setup Address for Table Lookup by Emitting a Digit and Using the Hundreds Digit. Set Address into Low B-Star.
4. Readout Tens Byte and Test Hundreds Zone to Determine Thousands Digit. This Example has Zone of 10 for 1 Thousand (Hex Equivalent is 3E8). Set Tens Digit and Thousands High Hex Digit into the High B-Star.
5. Set Remaining Two Hex Digits (Emitted) into a Hardware Register.
6. Readout Low Bias Plus Hundreds Digit Hex Equivalent Byte from Table in CPU Storage. Low B-Star has Address of Position in Table. For this Example Table Readout is 04.
7. A Test is made on the Tens Byte for Zones. If Tens Byte is Zoned, Indexing is Required. For Example Tens Digit is not Zoned. Add Low Bias Plus Hundreds Digit Hex Equivalent Byte (Remember this Byte is Crossed in the Storage Table) to Digits in the Hardware Register. Retain any Carry in the Carry Latch.
8. Readout the High Bias Plus Hundreds Digit Hex Equivalent Byte from Table in MPX Storage. Use Same Address as Used for Low Bias. For this Example Table Readout is 14.
9. Setup Table Address for Tens Digit Hex Equivalent by Setting the Tens Digit from the High B-Star to the Low B-Star and Emitting a Digit to the Low B-Star.
10. Add High Hex Thousands Digit in High B-Star and High Bias Plus Hundreds Digit Hex. Equivalent Byte and any Carry from Low Bias Addition to Thousand Digit. Set Sum into B-Star.
11. Readout Units Byte.
12. Add Units Digit to Amount in the Hardware Register.
13. Test Zone Bits of Units Byte to Determine Remaining Thousands Address. For this Example Units Zone is 11 (No Zone) for 0 Thousands.
14. Readout the Hex Equivalent Byte of the Tens Digit from the Table in CPU Storage Using The Address Developed in the Low B-Star. The Digits in the Byte are Crossed in the Storage Table. For this Example Table Readout is A0.
15. Add the Hex Equivalent Byte (Uncrossed) to the Amount in the Hardware Register and Set the Sum into the Low B-Star. Any Carry is Added to the High B-Star.
16. The B-Star Now Contains the Required Hex Equivalent Address for the Address Y14 for the Condition in the Example. The B-Star is Transferred to the A-Star and I-Phase Continues. If Instruction has a B-Address the B-Star is Developed in Same Manner.





4567 →

0123	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000			.		,	/	N_9^8					B				
0001			D	Y	#	¤	E	Z	A	S	@	%	?	!	P	C
0010	U	1	2	3	4	5	6	7	PFR	K	F		(I/O) U	(I/O) M	(I/O) L	
0011					Invalid Ops						V	W				
0100																
0101																
0110																
0111		Column Binary														
1000	M															
1001	L															
1010																
1011		H														
1100																
1101																
1110																
1111		Q														

Cpu Ops
I/O Ops
Misc Ops

Bit Significant Chart

4567 ↓ 0123 →	With Wordmark				No Wordmark				With Wordmark				No Wordmark			
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	Blank	&	-		Blank	&	-		?	!	ǂ	0	?	!	ǂ	0
0001			/				/		A	J		1	A	J		1
0010									B	K	S	2	B	K	S	2
0011									C	L	T	3	C	L	T	3
0100									D	M	U	4	D	M	U	4
0101									E	N	V	5	E	N	V	5
0110									F	O	W	6	F	O	W	6
0111									G	P	X	7	G	P	X	7
1000									H	Q	Y	8	H	Q	Y	8
1001									I	R	Z	9	I	R	Z	9
1010				⅛				⅛								
1011	.	$	,	#	.	$	,	#								
1100	¤	*	%	@	¤	*	%	#								
1101	[	]	v	:	[	]	v	:								
1110	<	;	\	>	<	;	\	>								
1111	ǂ	Δ	⊣⊢	⌐	ǂ	Δ	⊣⊢	⌐								

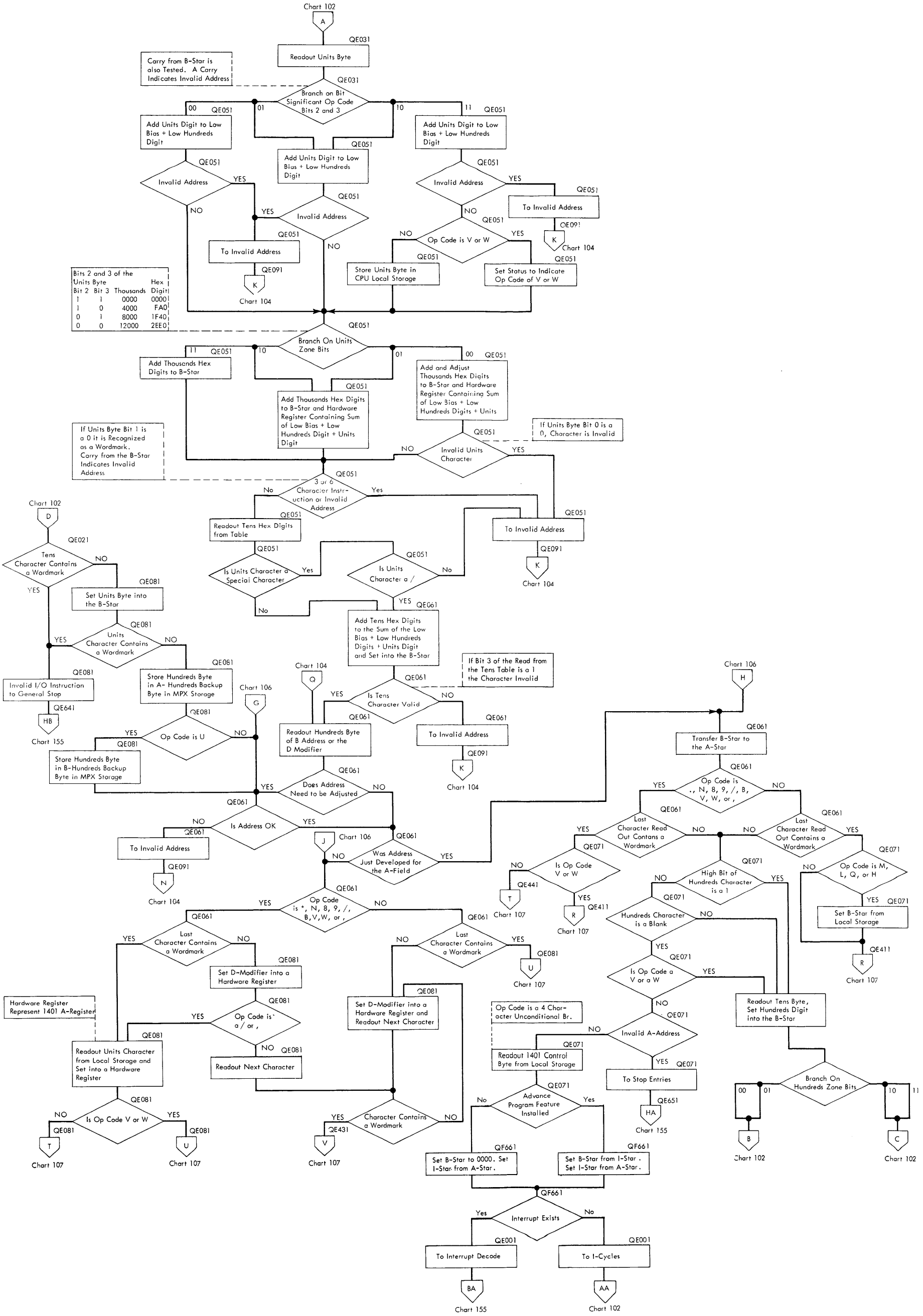
1400 Defined Characters

360 / 1400	Y Bias	Z Bias			
		16,384	32,768	65,536	8,192
16K	80	01	41	C0	
12K	20	11	51	D0	
8K	C0	20	60	EF	00
4K	60	30	70	FF	10
2K	30	38	78	F7	18
1.4K	88	3A	7A	F9	1A

Y = Bias for Low-Order Byte in Hex.
Z = Bias for High-Order Byte in Hex.

Bits 2 and 3 of Hundred Byte			Hex Digits
Bit 2	Bit 3	Thousands	
1	1	0000	000
1	0	1000	3E8
0	1	2000	7D0
0	0	3000	BB8

Compatibility Mode Memory Bias



CLF 103 1400 I-Cycles A and B Address Setup

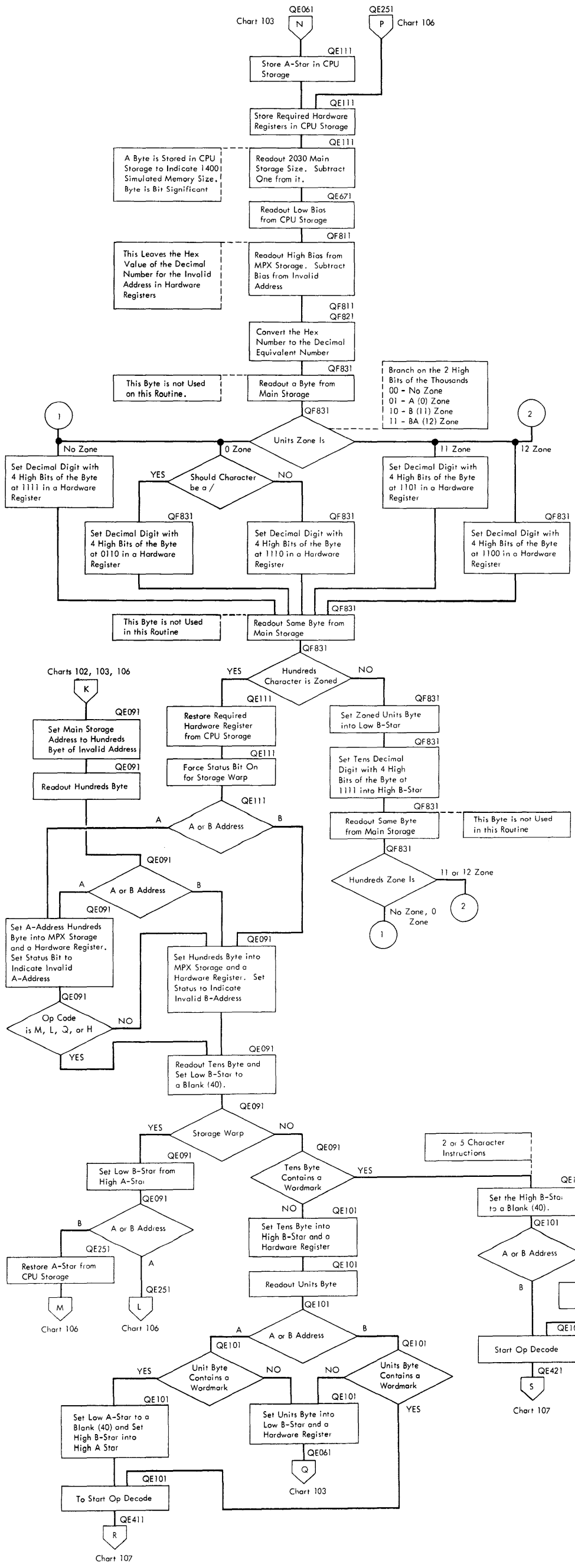
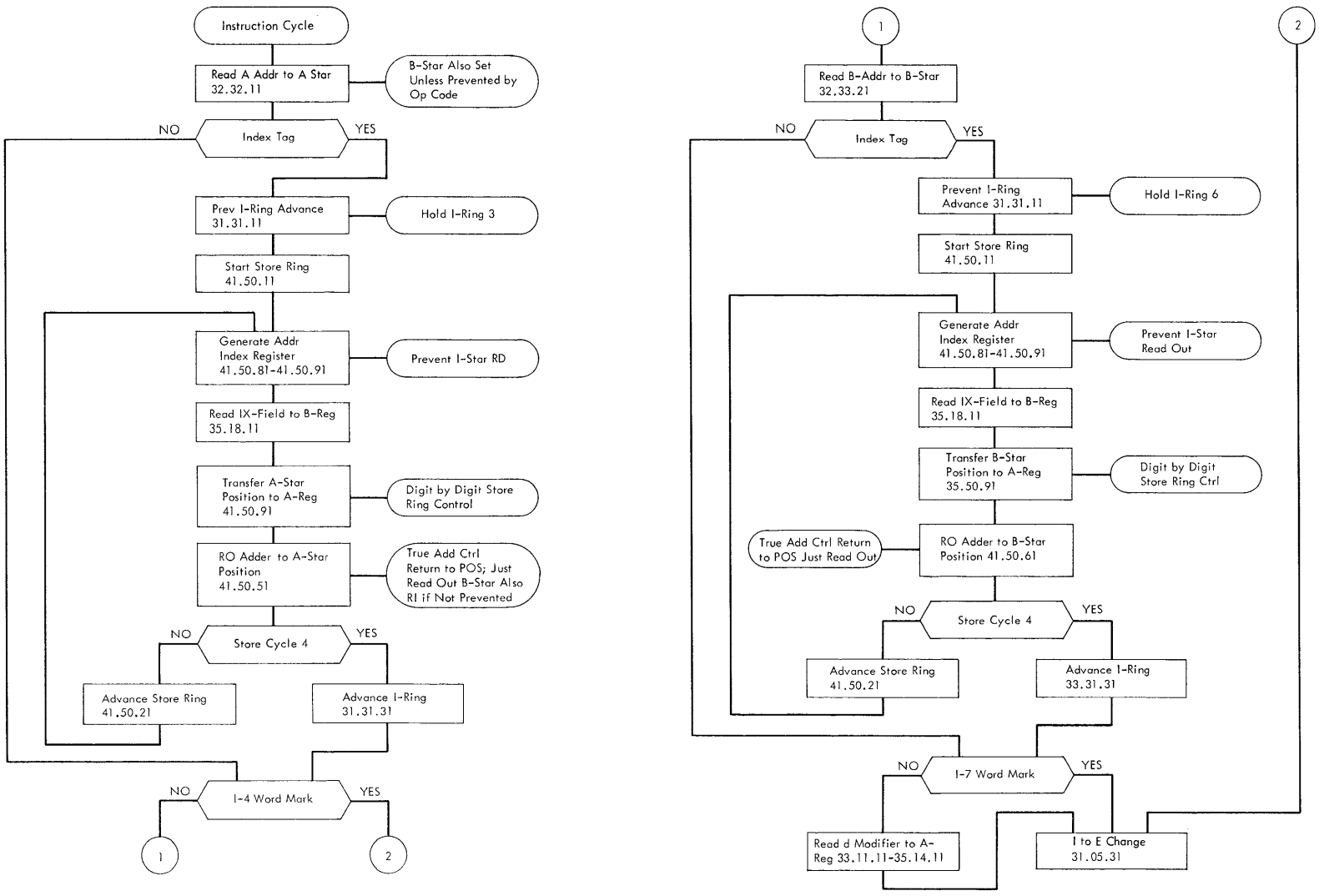


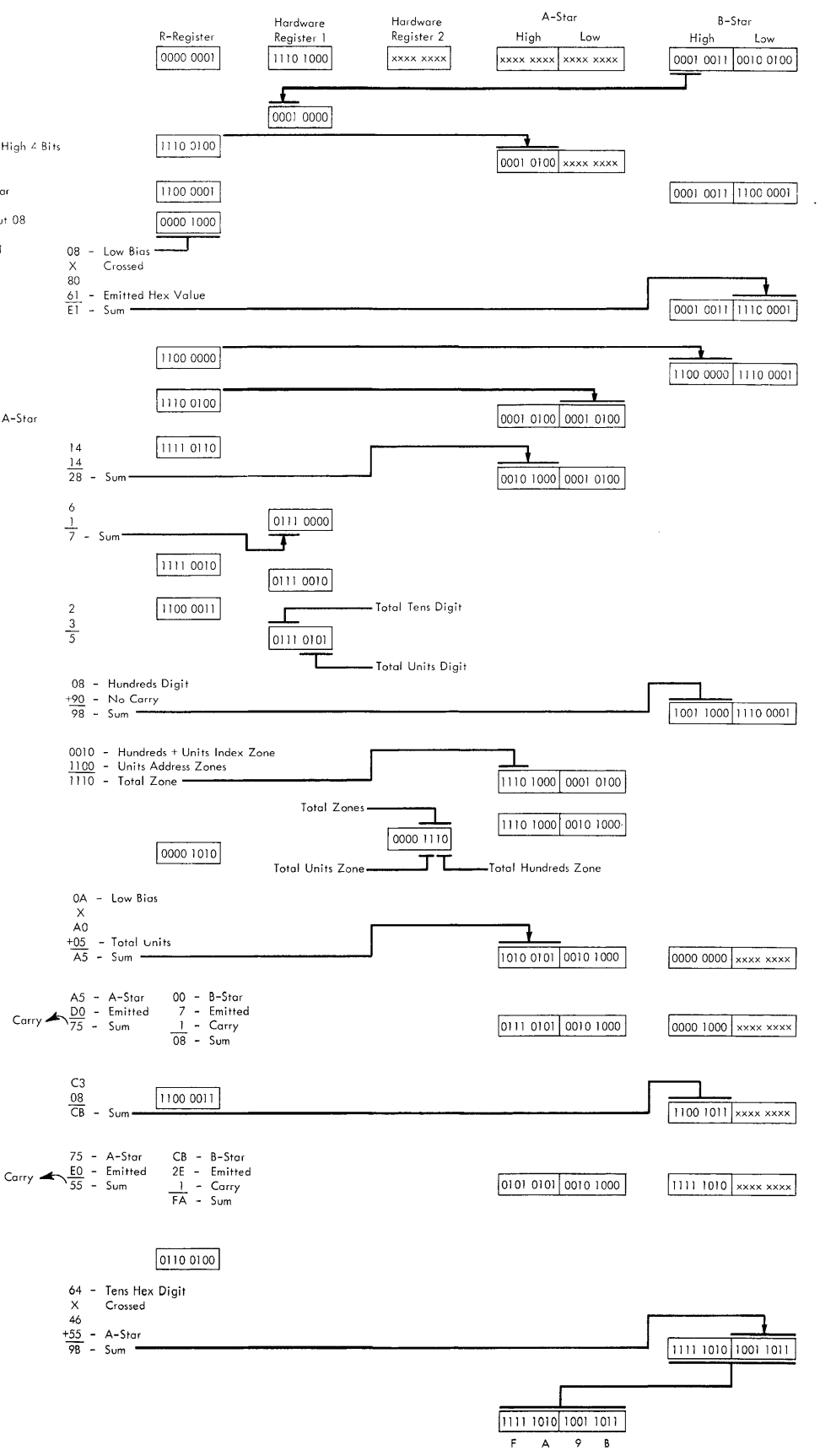
Chart 103
QE061
N
QE251
P
Chart 106
QE111
Store A-Star in CPU Storage
QE111
Store Required Hardware Registers in CPU Storage
QE111
A Byte is Stored in CPU Storage to Indicate 1400 Simulated Memory Size. Byte is Bit Significant
Readout 2030 Main Storage Size. Subtract One from it.
QE671
Readout Low Bias from CPU Storage
QF811
This Leaves the Hex Value of the Decimal Number for the Invalid Address in Hardware Registers
Readout High Bias from MPX Storage. Subtract Bias from Invalid Address
QF811
QF821
Convert the Hex Number to the Decimal Equivalent Number
QF831
This Byte is not Used on this Routine.
Readout a Byte from Main Storage
Branch on the 2 High Bits of the Thousands
00 - No Zone
01 - A (0) Zone
10 - B (11) Zone
11 - BA (12) Zone
QF831
1
2
Units Zone Is
No Zone
0 Zone
11 Zone
12 Zone
Set Decimal Digit with 4 High Bits of the Byte at 1111 in a Hardware Register
YES
Should Character be a /
NO
Set Decimal Digit with 4 High Bits of the Byte at 1101 in a Hardware Register
QF831
Set Decimal Digit with 4 High Bits of the Byte at 0110 in a Hardware Register
QF831
Set Decimal Digit with 4 High Bits of the Byte at 1110 in a Hardware Register
QF831
Set Decimal Digit with 4 High Bits of the Byte at 1100 in a Hardware Register
QF831
This Byte is not Used in this Routine
Readout Same Byte from Main Storage
QF831
Charts 102, 103, 106
K
YES
Hundreds Character is Zoned
NO
QE091
Set Main Storage Address to Hundreds Byet of Invalid Address
QE111
Restore Required Hardware Register from CPU Storage
QF831
Set Zoned Units Byte into Low B-Star
QE091
Readout Hundreds Byte
QE111
Force Status Bit On for Storage Warp
QF831
Set Tens Decimal Digit with 4 High Bits of the Byte at 1111 into High B-Star
QE111
A
A or B Address
B
QF831
Readout Same Byte from Main Storage
This Byte is not Used in this Routine
QF831
QE091
Hundreds Zone Is
11 or 12 Zone
2
A
A or B Address
B
No Zone, 0 Zone
1
QE091
Set A-Address Hundreds Byte into MPX Storage and a Hardware Register. Set Status Bit to Indicate Invalid A-Address
QE091
Set Hundreds Byte into MPX Storage and a Hardware Register. Set Status to Indicate Invalid B-Address
QE091
Op Code is M, L, Q, or H
NO
YES
QE091
Readout Tens Byte and Set Low B-Star to a Blank (40).
QE091
YES
Storage Warp
NO
QE091
Set Low B-Star from High A-Star
QE091
Tens Byte Contains a Wordmark
YES
2 or 5 Character Instructions
QE101
Set the High B-Star to a Blank (40).
QE101
A or B Address
A
B
QE101
Set A-Star from B-Star
QE101
Start Op Decode
QE421
S
Chart 107
NO
QE101
Set Tens Byte into High B-Star and a Hardware Register
QE101
Readout Units Byte
QE101
A
A or B Address
B
QE101
QE101
YES
Unit Byte Contains a Wordmark
NO
NO
Units Byte Contains a Wordmark
YES
QE101
Set Low A-Star to a Blank (40) and Set High B-Star into High A Star
QE101
Set Units Byte into Low B-Star and a Hardware Register
QE061
Q
Chart 103
QE101
To Start Op Decode
QE411
R
Chart 107
B
A or B Address
A
QE251
Restore A-Star from CPU Storage
QE251
M
Chart 106
L
Chart 106

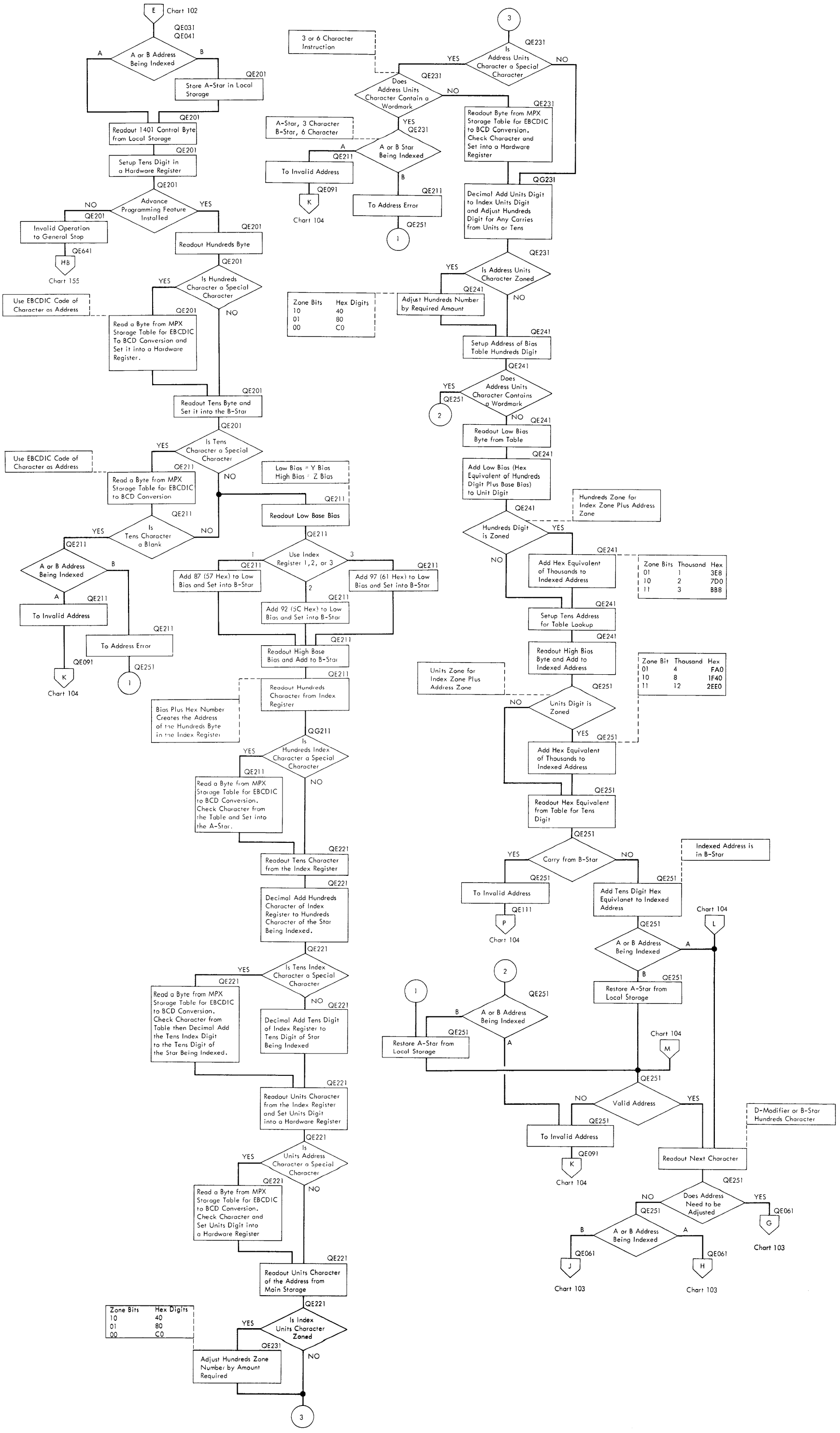


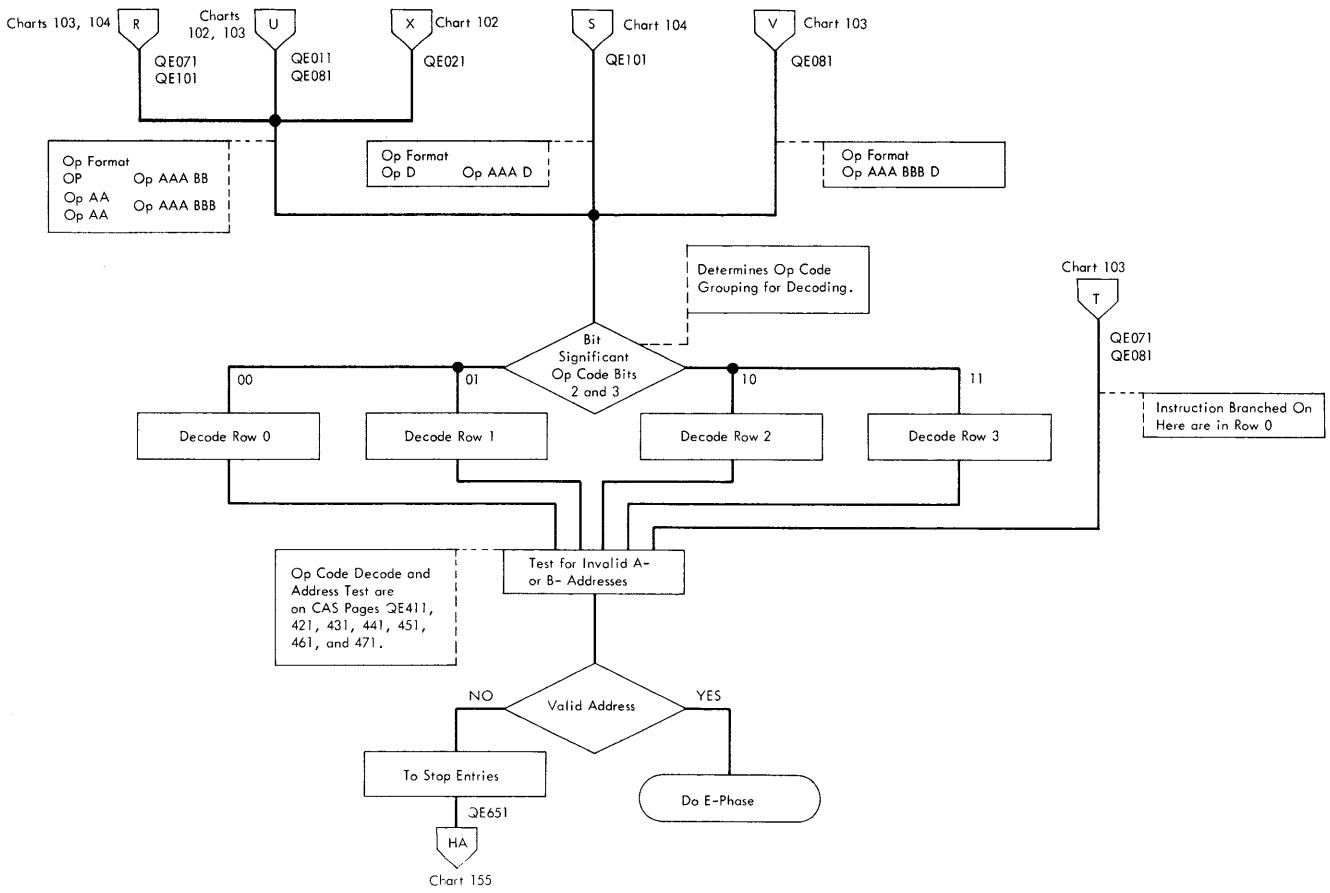
Example for A-Star or B-Star Development with Indexing During I-Phase of 1401 Compatibility Feature on the 2030. Program is for a 16,000 Positions of Storage 1401 and the 2030 Has 65,536 Positions of Storage.

Instruction is A UAC 456 B. Index Register 3 has U62 Stored.

1. Recognize Indexing Required (Tens Byte Zoned).
2. Set Tens Digit from High B-Star to the High 4-Bits of Hardware Register 1.
3. Readout Hundreds Byte Again. If Special Character, Do Table Lookup of BCD Equivalent. For this Example Invert High 4 Bits and Set Byte into High A-Star
4. Readout Tens Byte Again. If Special Character, Do Table Lookup of BCD Equivalent. Set Character into Low B-Star
5. Readout Low Bias from CPU Storage (Address is Emitted). Bias is Crossed in Storage Table. For this Example Readout 08
6. Test Zone Bits of Tens Character to Determine Index Register. For this Example Zone is 00 (Index Register 3). 1401 Index Register 3 Address is 0097 (Hex Equivalent is 61). Add the Hex Value to Low Bias and Set into Low B-Star.
7. Readout High Bias from MPX Storage (Same Address as Low Bias). For this Example Readout C0. Set High Bias into High B-Star
8. Address of Index Register Hundreds Byte in B-Star. Readout Hundreds Byte from Index Register. If Special Character, Do BCD Table Lookup. For this Example Character is U, Invert High 4 Bits and Set into Low A-Star
9. Read Tens Byte from Index Register. Decimal Add Index Hundreds and Address Hundreds Bytes and Set Sum into High A-Star
10. If Tens Byte is Special Character, Do Table Lookup for BCD Equivalent. Decimal Add Index Tens Digit (6) and Address Tens Digit (1) and Set Sum into High 4 Bits of Hardware Register 1.
11. Readout Units Byte from Index Register. If Special Character, Do BCD Table Lookup. For this Example Units Character is 2. Set Index Register Units Digit in the Low 4 Bits of Hardware Register 1.
12. Readout Units Byte for Address. If Special Character, Do BCD Table Lookup. Check Index Units Byte for Zone Bits; For Example Bits are 11 (No Zone) for 0 Thousands. Decimal Add Index Units Digit and Address Units Digit. Set Sum into Low 4 Bits of Hardware Register 1.
13. Decimal Add Any Carry (from Units or Tens Addition) to Combined Hundreds Digit and Set into High B-Star. For this Example No Carry. Emitt a 9 to Force a High Carry Should Low Digits Give a Carry.
14. Check Units Address Zone Bits. For Example Zone Bits are 00 (12,000). This Adds a C (Hex) to Accumulated Zones in High A-Star. Accumulated Zones are in High 4 Bits of the High A Star.
15. Setup Address for Table Lookup of Low Bias + Hundreds Digit Hex Equivalent Digit in Low A-Star. Set Total Zone Digit into Low 4 Bits of Hardware Register 2. Readout Low Bias + Hundreds Byte from CPU Storage. For this Example 0A is Readout Because 3yte is Crossed in Storage Table.
16. Add Low Bias Plus Hundreds Digit Hex Equivalent to Total Units Digit and Set into High A-Star. Set a Carry into High B-Star. For this Example No Carry.
17. Test Total Hundreds Zone to Determine Correct Hex Digits to Add to High A-Star and High B-Star. For this Example Bits are 10 (Hex Digits are 7D0). Add D0 to High A-Star, Any Carry from A-Star is Added to High B-Star. Add the 7 to High B-Star.
18. Readout High Bias Plus Hundreds Digit Hex Equivalent from MPX Storage. Setup Total Tens Digit Hex Equivalent Byte Address. Add High Bias Byte to High B-Star.
19. Test Total Units Zone to Determine Correct Hex Digits to Add to High A-Star and High B-Star. For this Example Bits are 11 (Hex Digits are 2EE0). Add E0 to High A-Star, Any Carry from A-Star is Added to High B-Star. Add 2E to High B-Star
20. Readout Total Tens Hex Equivalent Digit from CPI Storage. For this Example Readout 64. Remember Byte is Crossed in Storage Table.
21. Add Tens Hex Byte (Uncrossed) to High A-Star and Set Sum in Low B-Star. Any Carry is Added to High B-Star.
22. End of Indexing this Address Continue I-Phase. If Address Being Indexed was the A-Star, Transfer A-Star to B-Star. If Address Being Indexed was B-Star, Restore the A-Star from Local Storage. For Example Set B-Star into A Star.

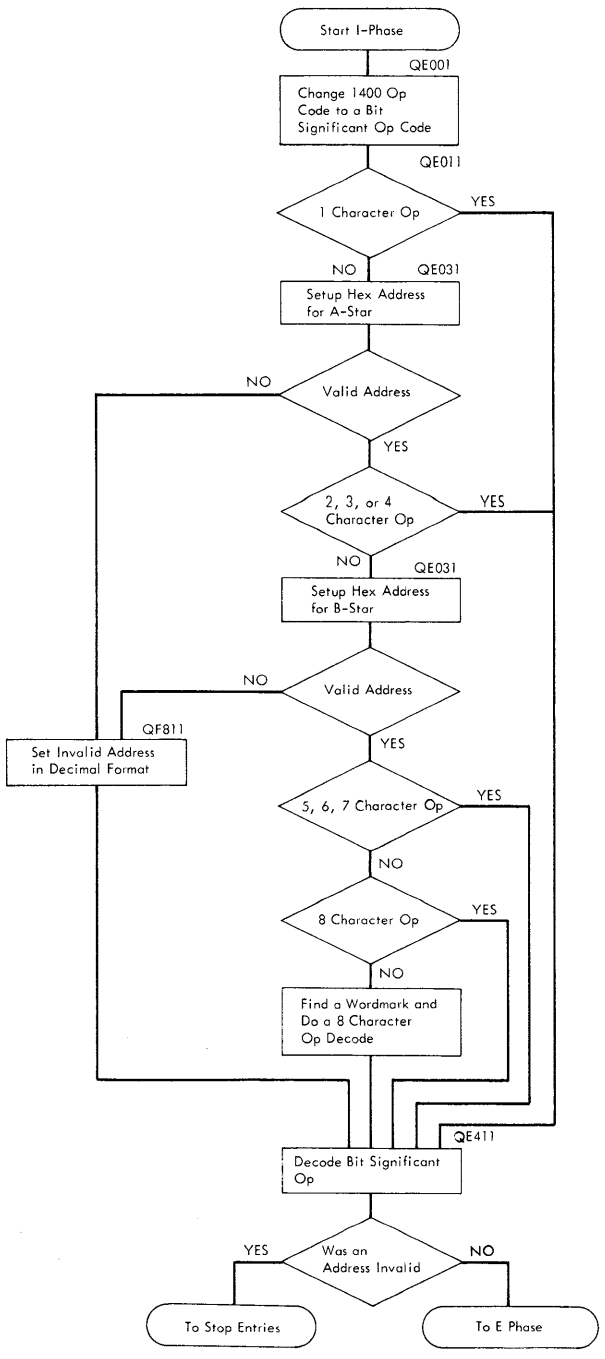


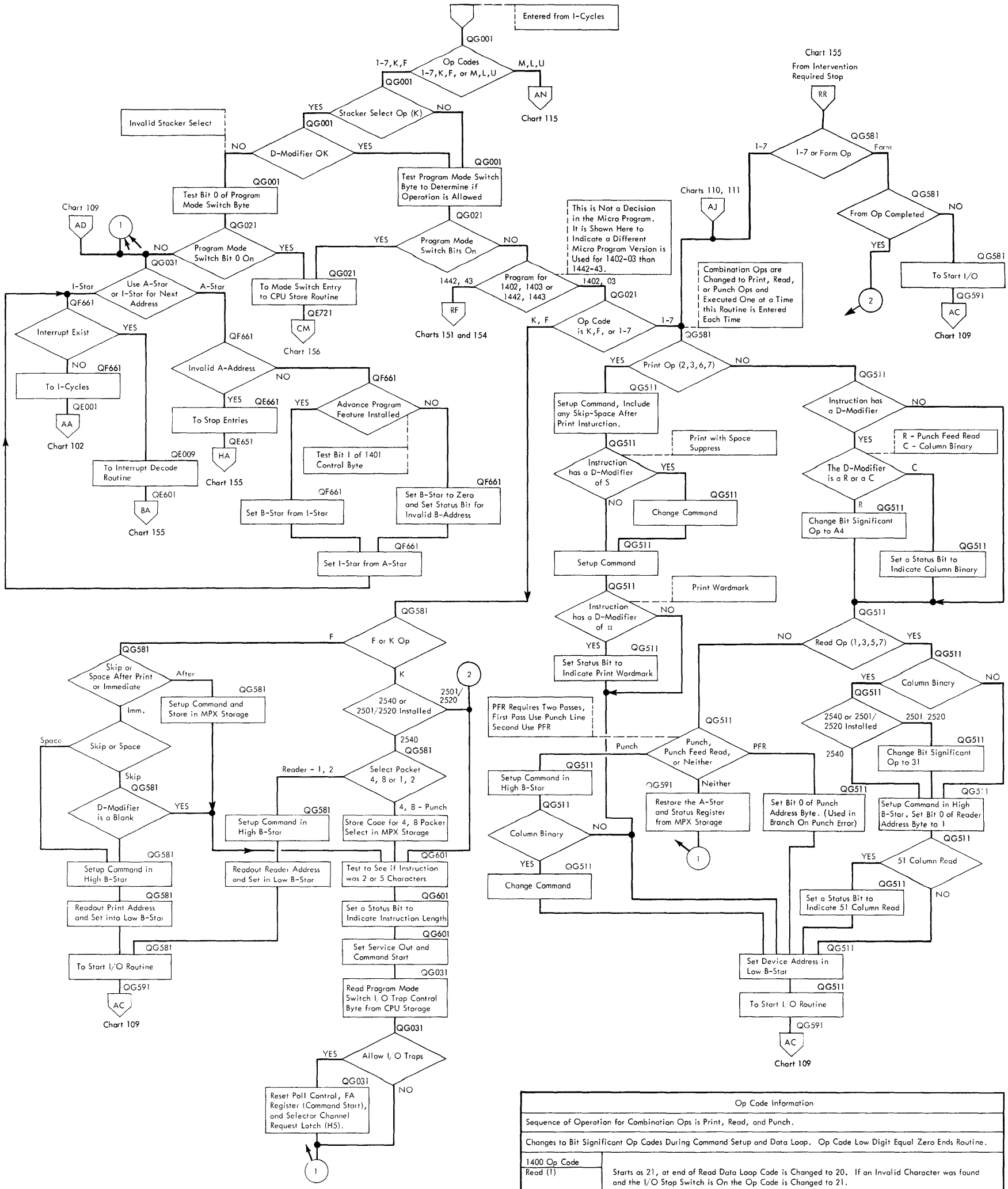

E
Chart 102
QE031
QE041
A or B Address Being Indexed
A
B
QE201
Store A-Star in Local Storage
QE201
Readout 1401 Control Byte from Local Storage
QE201
Setup Tens Digit in a Hardware Register
QE201
Advance Programming Feature Installed
NO
YES
QE201
Invalid Operation to General Stop
QE641
HB
Chart 155
QE201
Readout Hundreds Byte
QE201
Is Hundreds Character a Special Character
YES
NO
Use EBCDIC Code of Character as Address
QE201
Read a Byte from MPX Storage Table for EBCDIC To BCD Conversion and Set it into a Hardware Register.
QE201
Readout Tens Byte and Set it into the B-Star
QE201
Is Tens Character a Special Character
YES
NO
Use EBCDIC Code of Character as Address
QE211
Read a Byte from MPX Storage Table for EBCDIC to BCD Conversion
QE211
Is Tens Character a Blank
YES
NO
QE211
A or B Address Being Indexed
B
A
QE211
To Invalid Address
QE211
To Address Error
QE091
QE251
K
1
Chart 104
Low Bias = Y Bias
High Bias = Z Bias
QE211
Readout Low Base Bias
QE211
Use Index Register 1, 2, or 3
1
2
3
QE211
Add 87 (57 Hex) to Low Bias and Set into B-Star
QE211
Add 92 (5C Hex) to Low Bias and Set into B-Star
QE211
Add 97 (61 Hex) to Low Bias and Set into B-Star
QE211
Readout High Base Bias and Add to B-Star
QE211
Readout Hundreds Character from Index Register
Bias Plus Hex Number Creates the Address of the Hundreds Byte in the Index Register
QG211
Is Hundreds Index Character a Special Character
YES
NO
QE211
Read a Byte from MPX Storage Table for EBCDIC to BCD Conversion. Check Character from the Table and Set into the A-Star.
QE221
Readout Tens Character from the Index Register
QE221
Decimal Add Hundreds Character of Index Register to Hundreds Character of the Star Being Indexed.
QE221
Is Tens Index Character a Special Character
YES
NO
QE221
Read a Byte from MPX Storage Table for EBCDIC to BCD Conversion. Check Character from Table then Decimal Add the Tens Index Digit to the Tens Digit of the Star Being Indexed.
QE221
Decimal Add Tens Digit of Index Register to Tens Digit of Star Being Indexed
QE221
Readout Units Character from the Index Register and Set Units Digit into a Hardware Register
QE221
Is Units Address Character a Special Character
YES
NO
QE221
Read a Byte from MPX Storage Table for EBCDIC to BCD Conversion. Check Character and Set Units Digit into a Hardware Register
QE221
Readout Units Character of the Address from Main Storage
QE221
Is Index Units Character Zoned
YES
NO
QE231
Adjust Hundreds Zone Number by Amount Required
3
Zone Bits Hex Digits
10 40
01 80
00 C0
3 or 6 Character Instruction
QE231
Is Address Units Character a Special Character
YES
NO
QE231
Does Address Units Character Contain a Wordmark
NO
YES
QE231
A-Star, 3 Character
B-Star, 6 Character
A or B Star Being Indexed
A
B
QE211
To Invalid Address
QE091
K
Chart 104
QE211
To Address Error
QE251
1
QE231
Readout Byte from MPX Storage Table for EBCDIC to BCD Conversion. Check Character and Set into a Hardware Register
QG231
Decimal Add Units Digit to Index Units Digit and Adjust Hundreds Digit for Any Carries from Units or Tens
QE231
Is Address Units Character Zoned
YES
NO
QE241
Adjust Hundreds Number by Required Amount
Zone Bits Hex Digits
10 40
01 80
00 C0
QE241
Setup Address of Bias Table Hundreds Digit
QE241
Does Address Units Character Contains a Wordmark
YES
NO
QE251
2
QE241
Readout Low Bias Byte from Table
QE241
Add Low Bias (Hex Equivalent of Hundreds Digit Plus Base Bias) to Unit Digit
QE241
Hundreds Digit is Zoned
Hundreds Zone for Index Zone Plus Address Zone
YES
NO
QE241
Add Hex Equivalent of Thousands to Indexed Address
Zone Bits Thousand Hex
01 1 3E8
10 2 7D0
11 3 BB8
QE241
Setup Tens Address for Table Lookup
QE241
Readout High Bias Byte and Add to Indexed Address
Zone Bit Thousand Hex
01 4 FA0
10 8 1F40
11 12 2EE0
Units Zone for Index Zone Plus Address Zone
QE251
Units Digit is Zoned
NO
YES
QE251
Add Hex Equivalent of Thousands to Indexed Address
QE251
Readout Hex Equivalent from Table for Tens Digit
QE251
Carry from B-Star
YES
NO
Indexed Address is in B-Star
QE251
To Invalid Address
QE111
P
Chart 104
QE251
Add Tens Digit Hex Equivlanet to Indexed Address
Chart 104
L
QE251
A or B Address Being Indexed
A
B
QE251
Restore A-Star from Local Storage
1
2
QE251
A or B Address Being Indexed
B
A
QE251
Restore A-Star from Local Storage
Chart 104
M
QE251
Valid Address
NO
YES
D-Modifier or B-Star Hundreds Character
QE251
To Invalid Address
QE091
K
Chart 104
Readout Next Character
QE251
Does Address Need to be Adjusted
NO
YES
QE061
G
Chart 103
QE251
A or B Address Being Indexed
B
A
QE061
J
Chart 103
QE061
H
Chart 103



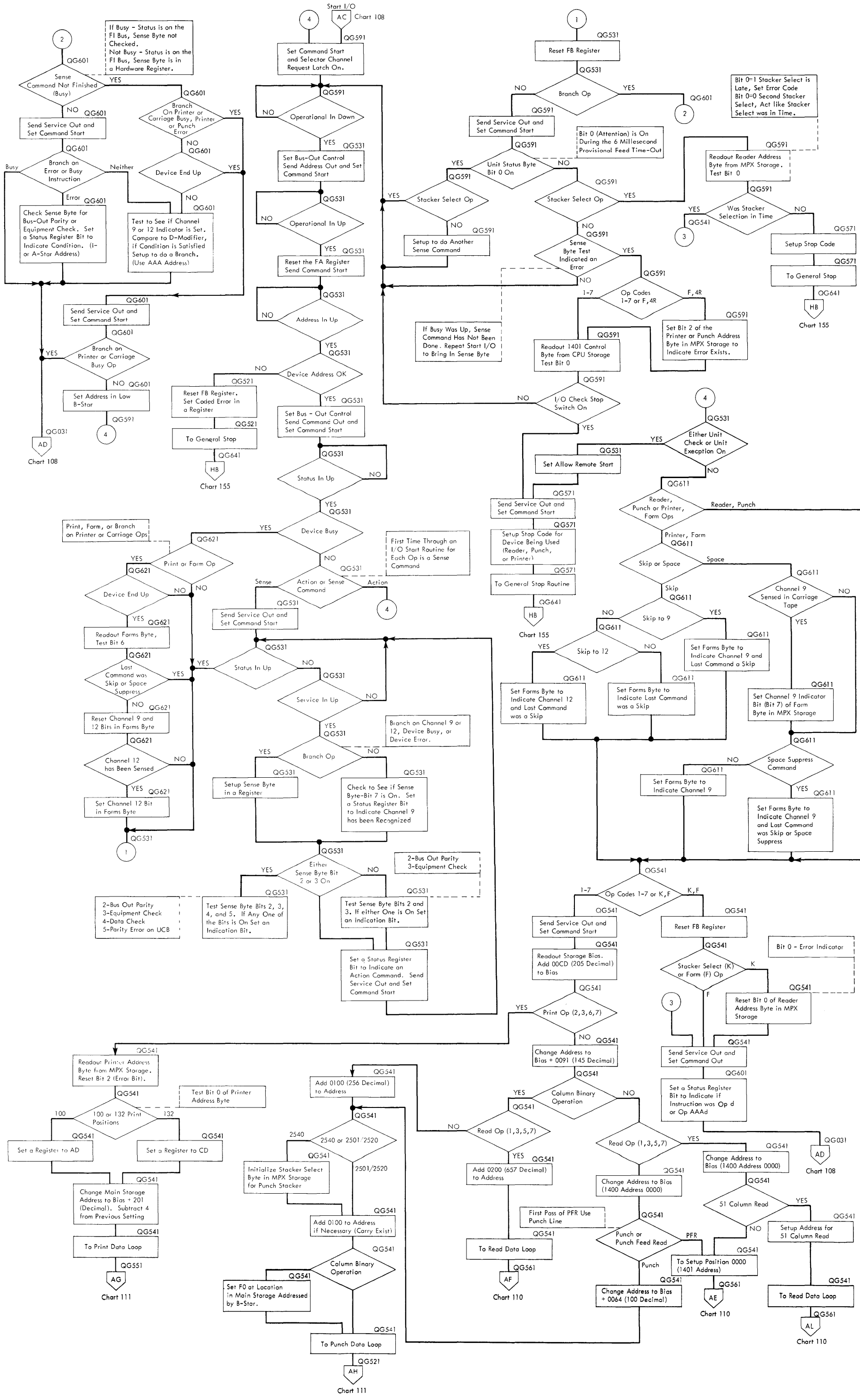
Row	Significant Op Byte	Instruction Name	1401 Sym.	CLF Ch.	Row	Significant Op Byte	Instruction Name	1401 Sym.	CLF Ch.	Row	Significant Op Byte	Instruction Name	1401 Sym.	CLF Ch.	Row	Significant Op Byte	Instruction Name	1401 Sym.	CLF Ch.
0	0000 0010	Halt	·		1	0001 0010	Move Digit	D		2	0010 0000	Control (Note 1)	U	108	3	0011 0100	Invalid		155
0	0000 0100	Set Wordmark	,		1	0001 0011	Move Zone	Y		2	0010 0001	*Read	1	108	3	0011 1010	Branch on WM/Zone	V	
0	0000 0101	Clear			1	0001 0100	Address Modify	#		2	0010 0010	*Print	2	108	3	0011 1011	Bit Test	W	
0	0000 0110	No Op	N		1	0001 0101	Clear Wordmark	¤		2	0010 0011	*Read-Print	3	108	3	1011 0001	Store A-Star	H	
0	0000 0110	Early Read (Note 2)	8		1	0001 0110	Edit	E		2	0010 0100	*Punch	4	108	3	1111 0001	Store B-Star	Q	
0	0000 0110	Early Punch (Note 2)	9		1	0001 0111	Move Zero Suppress	Z		2	0010 0101	*Read-Punch	5	108					
0	0000 0110	Branch	B		1	0001 1000	Add	A		2	0010 0110	*Print-Punch	6	108					
0	1000 0000	Move (Note 1)	M		1	0001 1001	Subtract	S		2	0010 0111	*Read-Punch-Print	7	108					
0	1000 0000	Move, Column Bin.	M		1	0001 1010	Multiply			2	0010 0100	*Punch Feed Read	4R	108					
0	1000 0000	Move, Sterling	M		1	0001 1011	Divide	%		2	0010 1001	Stacker Select	K	108					
					1	0001 1100	Reset Add	?		2	0010 1010	Form	F	108					
					1	0001 1101	Reset Subtract	!		2	0010 1100	Control	U	115					
					1	0001 1110	Move Record	P		2	0010 1101	Move	M	115					
					1	0001 1111	Compare	C		2	0010 1110	Load	L	115					
					1	1001 0000	Load (Note 1)	L											
												*Note 3							

Note 1. If I O Operation Change Op Code L to 0010 1110, M to 0010,1101, and U to 0010 1100
Note 2. These Op Codes are Handled as No Ops.
Note 3. This Op Codes Start with Bit Significant Byte as Shown. As the Op is Performed the Op Code is Changed to Indicate the First Pass or the Op Code has a D-Modifier, Also to Indicate when a Combination Op is Finished.





Op Code Information	
Sequence of Operation for Combination Ops is Print, Read, and Punch.	
Changes to Bit Significant Op Codes During Command Setup and Data Loop. Op Code Low Digit Equal Zero Ends Routine.	
1400 Op Code Read (1)	Starts as 21, at end of Read Data Loop Code is Changed to 20. If an Invalid Character was found and the I/O Stop Switch is On the Op Code is Changed to 21.
Print (2)	Starts as 22, at End of Print Data Loop Code is Changed to 20. If Operational In Drops During the Data Loop Code Stays 22 and a Stop Occurs.
Print, Read (3)	Starts as 23, at End of Print Data Loop Changes to 21 unless Operational In Drops During Loop. The 21 Causes a Read Routine to Start. End of Read Data Loop Change to 20 Unless Error Exists.
Punch (4) Punch Col Bin (4C)	Starts as 24, at End of Punch Data Loop Code Changes to 20 Unless Operational In Dropped During Data Loop or Last Card Punch had an Error Then Op Code Stays 24.
Read, Punch (5)	Starts as 25, End of Read Data Loop Code Changes to 24. If an Error has Occurred and I/O Stop Switch is On Op Code is Changed to 25 Again and Stops. No Error the 24 Cause a Punch Operation. If Operational End Drops During Data Loop or Last Card Punched had an Error Code Stays 24, Otherwise Changes to 20.
Print, Punch (6)	Starts as 26, End of Print Data Loop Unless an Error Occurs the Op Code Changes to 24 and a Punch Operation is Performed. The 24 Changes to 20 Unless Operational In Drops During the Data Loop or Last Card Punch was in Error.
Print, Read, Punch (7)	Starts as 27, End of Print Data Loop the Op Code Changes to 25 Unless an Error has Occurred. The 25 Starts a Read Operation; at the End of the Read Data Loop the Op Code is Changed to 24 Unless an Error has Occurred and the I/O Stop Switch is On. The 24 Causes a Punch Operation to Start, at the End of the Punch Data Loop the Op Code Changes to 20 Unless an Error has Occurred
Punch Feed Read (4R)	Starts as 24, the d-Modifier Causes the Op Code to Change to A4 then a Normal Punch Routine is Started. At the End of the Punch Data Loop if an Error Situation has Occurred the Op Code Stays as A4 and a Stop Occurs. No Error, the A4 Changes to 28 which Cause a Read Operation to be Performed. If no Errors Occur During Read Operation the Op Code Changes to 20. If Error Occurred and I/O Switch On, Stop with Op Code 20.
Read Col Binary (1C-2540)	Starts as 21. Note: Column Binary Read on a 2540 Requires Two Passes through the Read Data Loop: At the End of the First Pass (Information Entered into 401-480 and 501-580) the Op Code is Changed to 71, if an Error Occurred on the First Pass and the I/O Stop Switch is On the Op Code is Changed to 61 and then F1. No Error or I/O Stop Switch Off Op Code Stays 71. The Second Pass is Made Entering Some Information or Blanks into 0001-0080. Now if the Op Code had Changed to F1 it will be Changed to 61 and a Stop Occurs, but if the Op Code was 71 Entering the Second Pass the Op Code Changes to 00.
Read Col Binary (1C-2501/2520)	Starts as 21 and is Changed to 31 to Indicate 2501/2520 which Only take One Pass to Enter Information (Only Enters 401-480 and 501 to 580). At End of Read Data Loop for Column Binary First Pass the Op Code is Changed to 30. If an Error Occurred During the First Pass the and the I/O Stop Switch is On the Op Code is Changed to 21 and a Stop Occurs.


Start I/O
AC
Chart 108
4
QG591
Set Command Start and Selector Channel Request Latch On.
QG591
Operational In Down
NO
YES
QG531
Set Bus-Out Control Send Address Out and Set Command Start
QG531
Operational In Up
NO
YES
QG531
Reset the FA Register Send Command Start
QG531
Address In Up
NO
YES
QG531
Device Address OK
NO
YES
QG521
Reset FB Register. Set Coded Error in a Register
QG521
To General Stop
QG641
HB
Chart 155
QG531
Set Bus - Out Control Send Command Out and Set Command Start
QG531
Status In Up
NO
YES
QG531
Device Busy
YES
NO
QG531
Action or Sense Command
Sense
Action
First Time Through an I/O Start Routine for Each Op is a Sense Command
4
QG531
Send Service Out and Set Command Start
QG531
Status In Up
NO
YES
QG531
Service In Up
NO
YES
QG531
Branch Op
YES
NO
Branch on Channel 9 or 12, Device Busy, or Device Error.
QG531
Setup Sense Byte in a Register
QG531
Check to See if Sense Byte-Bit 7 is On. Set a Status Register Bit to Indicate Channel 9 has been Recognized
QG531
Either Sense Byte Bit 2 or 3 On
YES
NO
2-Bus Out Parity
3-Equipment Check
QG531
Test Sense Byte Bits 2 and 3. If either One is On Set an Indication Bit.
QG531
Set a Status Register Bit to Indicate an Action Command. Send Service Out and Set Command Start
2-Bus Out Parity
3-Equipment Check
4-Data Check
5-Parity Error on UCB
QG531
Test Sense Byte Bits 2, 3, 4, and 5. If Any One of the Bits is On Set an Indication Bit.
Print, Form, or Branch on Printer or Carriage Ops
QG621
Print or Form Op
YES
QG621
Device End Up
NO
YES
QG621
Readout Forms Byte, Test Bit 6
QG621
Last Command was Skip or Space Suppress
YES
NO
QG621
Reset Channel 9 and 12 Bits in Forms Byte
QG621
Channel 12 has Been Sensed
NO
YES
QG621
Set Channel 12 Bit in Forms Byte
QG531
1
2
QG601
Sense Command Not Finished (Busy)
YES
NO
If Busy - Status is on the FI Bus, Sense Byte not Checked.
Not Busy - Status is on the FI Bus, Sense Byte is in a Hardware Register.
QG601
Send Service Out and Set Command Start
QG601
Branch on Error or Busy Instruction
Busy
Neither
Error
QG601
Check Sense Byte for Bus-Out Parity or Equipment Check. Set a Status Register Bit to Indicate Condition. (I- or A-Star Address)
QG601
Branch On Printer or Carriage Busy, Printer or Punch Error
YES
NO
QG601
Device End Up
YES
NO
QG601
Test to See if Channel 9 or 12 Indicator is Set. Compare to D-Modifier, if Condition is Satisfied Setup to do a Branch. (Use AAA Address)
QG601
Send Service Out and Set Command Start
QG601
Branch on Printer or Carriage Busy Op
YES
NO
QG601
Set Address in Low B-Star
QG591
4
QG031
AD
Chart 108
1
QG531
Reset FB Register
QG531
Branch Op
NO
YES
QG601
2
QG591
Send Service Out and Set Command Start
Bit 0 (Attention) is On During the 6 Millesecond Provisional Feed Time-Out
QG591
Unit Status Byte Bit 0 On
YES
NO
QG591
Stacker Select Op
YES
NO
QG591
Setup to do Another Sense Command
QG591
Stacker Select Op
YES
NO
QG591
Sense Byte Test Indicated an Error
YES
NO
If Busy Was Up, Sense Command Has Not Been Done. Repeat Start I/O to Bring In Sense Byte
QG591
Op Codes 1-7 or F,4R
1-7
F,4R
QG591
Readout 1401 Control Byte from CPU Storage Test Bit 0
QG591
Set Bit 2 of the Printer or Punch Address Byte in MPX Storage to Indicate Error Exists.
QG591
I/O Check Stop Switch On
NO
YES
Bit 0=1 Stacker Select is Late, Set Error Code
Bit 0=0 Second Stacker Select, Act like Stacker Select was in Time.
QG591
Readout Reader Address Byte from MPX Storage. Test Bit 0
QG591
Was Stacker Selection in Time
YES
NO
QG541
3
QG571
Setup Stop Code
QG571
To General Stop
QG641
HB
Chart 155
4
QG531
Either Unit Check or Unit Execption On
YES
NO
QG531
Set Allow Remote Start
QG571
Send Service Out and Set Command Start
QG571
Setup Stop Code for Device Being Used (Reader, Punch, or Printer)
QG571
To General Stop Routine
QG641
HB
Chart 155
QG611
Reader, Punch or Printer, Form Ops
Reader, Punch
Printer, Form
QG611
Skip or Space
Skip
Space
QG611
Skip to 9
NO
YES
QG611
Skip to 12
YES
NO
QG611
Set Forms Byte to Indicate Channel 12 and Last Command was a Skip
QG611
Set Forms Byte to Indicate Last Command was a Skip
QG611
Set Forms Byte to Indicate Channel 9 and Last Command a Skip
QG611
Channel 9 Sensed in Carriage Tape
NO
YES
QG611
Set Channel 9 Indicator Bit (Bit 7) of Form Byte in MPX Storage
QG611
Space Suppress Command
NO
YES
QG611
Set Forms Byte to Indicate Channel 9
QG611
Set Forms Byte to Indicate Channel 9 and Last Command was Skip or Space Suppress
QG541
Op Codes 1-7 or K,F
1-7
K,F
QG541
Send Service Out and Set Command Start
QG541
Readout Storage Bias. Add 00CD (205 Decimal) to Bias
QG541
Print Op (2,3,6,7)
YES
NO
QG541
Change Address to Bias + 0091 (145 Decimal)
QG541
Column Binary Operation
YES
NO
QG541
Read Op (1,3,5,7)
NO
YES
QG541
Add 0200 (657 Decimal) to Address
First Pass of PFR Use Punch Line
QG541
To Read Data Loop
QG561
AF
Chart 110
QG541
Read Op (1,3,5,7)
YES
QG541
Change Address to Bias (1400 Address 0000)
QG541
Change Address to Bias (1400 Address 0000)
QG541
Punch or Punch Feed Read
PFR
Punch
QG541
To Setup Position 0000 (1401 Address)
QG561
AE
Chart 110
QG541
Change Address to Bias + 0064 (100 Decimal)
QG541
51 Column Read
YES
NO
QG541
Setup Address for 51 Column Read
QG541
To Read Data Loop
QG561
AL
Chart 110
QG601
Set a Status Register Bit to Indicate if Instruction was Op d or Op AAAd
QG031
AD
Chart 108
Bit 0 - Error Indicator
QG541
Stacker Select (K) or Form (F) Op
K
F
QG541
Reset Bit 0 of Reader Address Byte in MPX Storage
3
QG541
Send Service Out and Set Command Out
QG541
Readout Printer Address Byte from MPX Storage. Reset Bit 2 (Error Bit).
Test Bit 0 of Printer Address Byte
QG541
100 or 132 Print Positions
100
132
QG541
Set a Register to AD
QG541
Set a Register to CD
QG541
Change Main Storage Address to Bias + 201 (Decimal). Subtract 4 from Previous Setting
QG541
To Print Data Loop
QG551
AG
Chart 111
QG541
Add 0100 (256 Decimal) to Address
QG541
2540 or 2501/2520
2540
2501/2520
QG541
Initialize Stacker Select Byte in MPX Storage for Punch Stacker
QG541
Add 0100 to Address if Necessary (Carry Exist)
QG541
Column Binary Operation
QG541
Set F0 at Location in Main Storage Addressed by B-Star.
QG541
To Punch Data Loop
QG521
AH
Chart 111

0000
Chart 109 AE
Chart 109 Column Binary AF
51 Column AL
Note: This Routine Receives the Data from the Readers Control Unit Buffer, Check it for Valid Information and Store the Data in Main Storage.
QG561 Setup 1400 Position 0000
QG561 On Column Binary Change Address to Equal (1400) 401
QG561 Add 1 to Address
1
QG561 Status In Up
YES
NO
QG561 Service In Up
QG571 Reset FB Register (Select Out)
QG571 Op Code is 28
QG571 Last Card has been Read
QG571 Readout Sense Switch Byte from CPU Storage and Set Bit 0 On
QG571 Readout Sense Switch Byte from CPU Storage and Reset Bit 0
QG571 Column Binary or Read, 2nd PFR Pass
Column Binary
Read, 2nd PFR
QG571 Using a 2540 or 2501/2520
2540
2501/2520
QG571 First or Second Pass
Second
First
QG571 Change Op Code 71 to 00 F1 to 00
QG571 Change Op Code 21 to 71
QG571 Change Op Code 31 to 30 Finished
QG571 Change Op Code 21 to 20 Finished 25 to 24 Punch 28 to 20 Finished
QG571 Invalid Characters Existed
QG571 Error Existed on First Pass
QG571 Change Op Code 00 to 61 Second 71 to 61 First 30 to 21 First Send Service Out and Set Command Start
QG571 Do Second Column Binary Pass
QG571 Change Op Code 61 to F1
QG581 AJ
Chart 108
QG571 Setup Error Code
QG571 To General Stop
QE641 HB
Chart 155
QG571 Unit Check Exists
QG571 Readout I/O Error Byte from MPX Storage and Reset Bit 5
QG571 Send Service Out and Set Command Start
QG581 AJ
Chart 108
QG571 Readout I/O Error Byte from MPX Storage and Set Bit 5 On (Reader Error)
QG571 Readout 1400 Control Byte from CPU Storage. Test Bit 0 (I/O Check Stop Switch).
QG571 I/O Check Stop Switch On
QG571 Send Service Out and Set Command Start
QG581 AJ
Chart 108
QG561 Setup Error Code
QG571 To General Stop
QE641 HB
Chart 155
QG561 Force Bit 1 of Character Being Read-In On (No Wordmark) and into a Hardware Register. (Used for Address on Table Lookup).
Characters Entering are in EBCDIC Except for Column Binary.
QG561 Readout Position of Main Storage Character will Enter
QG561 Ending Address Found
QG561 Reset Ending Indicators. Send Command Out
1
If Using a 2540 Column Binary Requires Two Passes. First Pass Set Data in Column Binary Read-In Area in NPL. Second Pass Set BCD in Codes or Blank in Normal Read-In Area
QG561 First Pass of a Column Binary Operation
51 Column Read; Use Normal Read After Column 14 Normal
QG561 Send Service Out and Set Command Start
QG561 Do a Table Lookup to Change BCD Character To EBCDIC Character
QG561 Setup to Change Main Storage Address for Next Column Binary Character Position.
QG561 If Character Readout from Main Storage had a Wordmark, Add a Wordmark to the EBCDIC Character and Enter Character into Main Storage
QG561 Change Main Storage Address
Address Change from 400 Read In Area to 500 Read In Area and Back Again for Each Card Column
51 Column Read or Normal Read
Normal
QG561 Send Service Out and Set Command Start
QG561 Position 14 Readout
QG561 Enter a & (0101 0000) into Position 14 (Decimal) and Setup Ending Address in a Hardware Register
QG561 Change Main Storage Address
QG561 Position in Main Storage has a Wordmark
QG561 Ending Address Readout
QG561 Send Service Out and Set Command Start. Set Indicator Bits to Indicate Ending Address Has Been Read Out
QG561 Invalid/MLP Character
QG561 Send Service Out and Set Command Start
QG561 Invalid/MLP Character
QG561 Table Lookup Character is a Valid Character
Used on Second Pass of Column Binary and Some MLP Characters on Normal Read
QG561 MLP Character
QG561 Setup a Blank Character
QG561 Do Table Lookup or Create a NPL Character.
Punched NPL
8, 9, 1 F1
8, 9, 2 F2
8, 9, 3 F3
QG561 Position in Main Storage has a Wordmark
QG561 Setup Character for NPL Character with Wordmark
QG561 Store Character in Normal Read-In Position and Update Address to Next Position

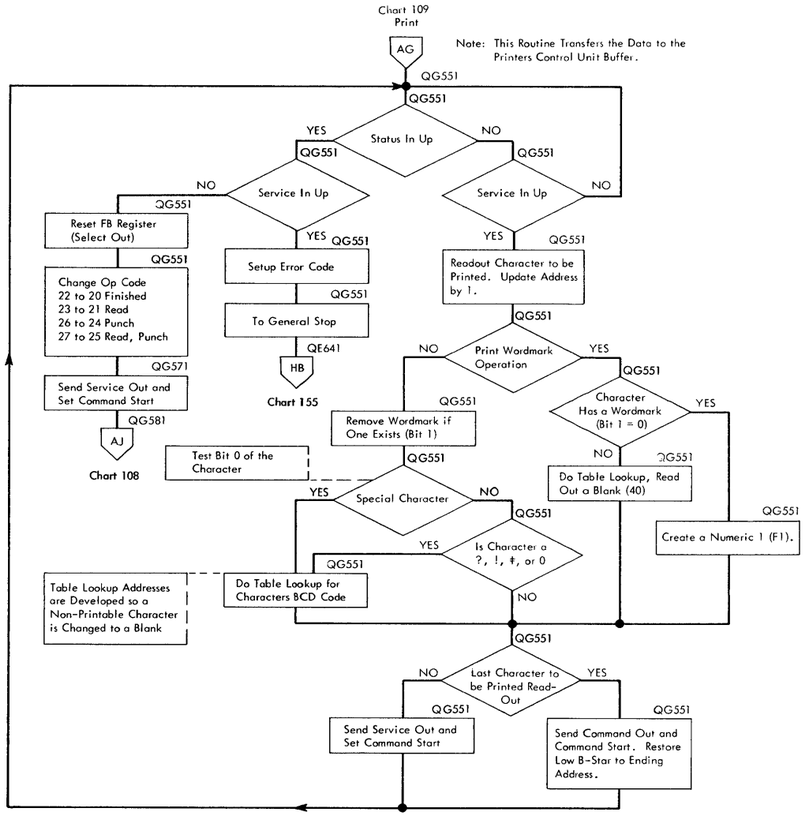


Chart 109
Print
AG
Note: This Routine Transfers the Data to the Printers Control Unit Buffer.
QG551
Status In Up
YES
NO
Service In Up
Reset FB Register (Select Out)
Change Op Code 22 to 20 Finished 23 to 21 Read 26 to 24 Punch 27 to 25 Read, Punch
Send Service Out and Set Command Start
QG581
AJ
Chart 108
Setup Error Code
To General Stop
QE641
HB
Chart 155
Readout Character to be Printed. Update Address by 1.
Print Wordmark Operation
Remove Wordmark if One Exists (Bit 1)
Test Bit 0 of the Character
Special Character
Table Lookup Addresses are Developed so a Non-Printable Character is Changed to a Blank
Do Table Lookup for Characters BCD Code
Is Character a ?, !, #, or 0
Character Has a Wordmark (Bit 1 = 0)
Do Table Lookup, Read Out a Blank (40)
Create a Numeric 1 (F1).
Last Character to be Printed Read-Out
Send Service Out and Set Command Start
Send Command Out and Command Start. Restore Low B-Star to Ending Address.

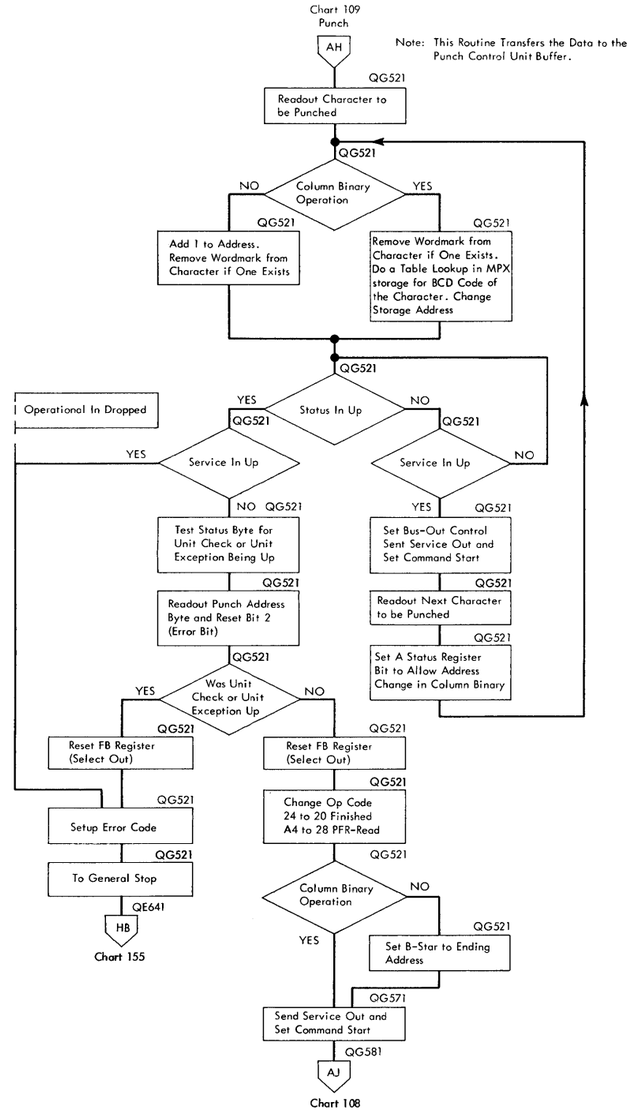
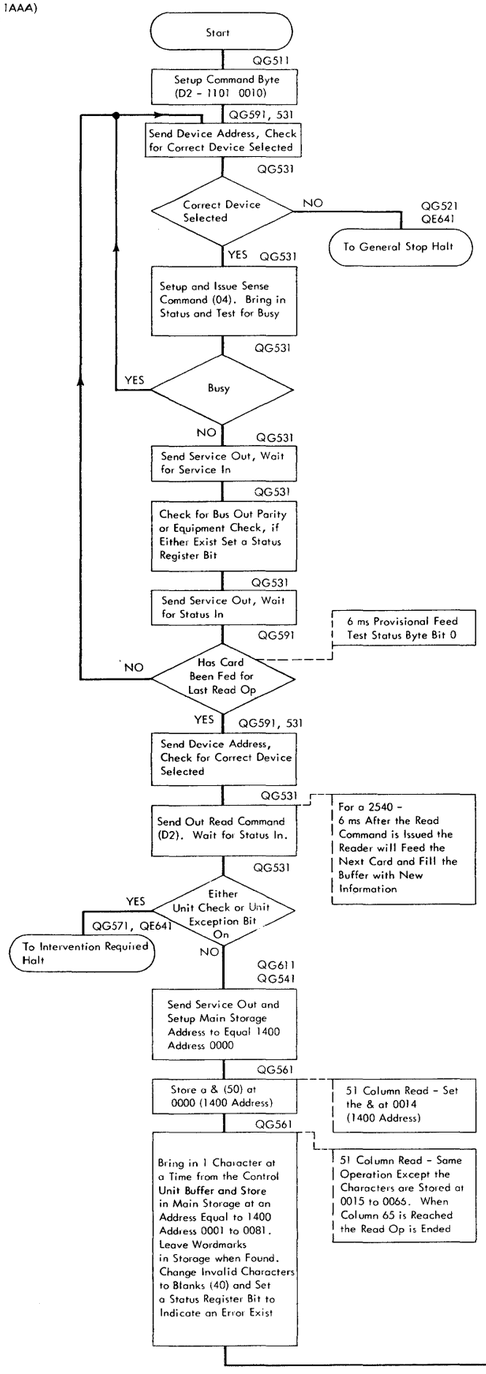
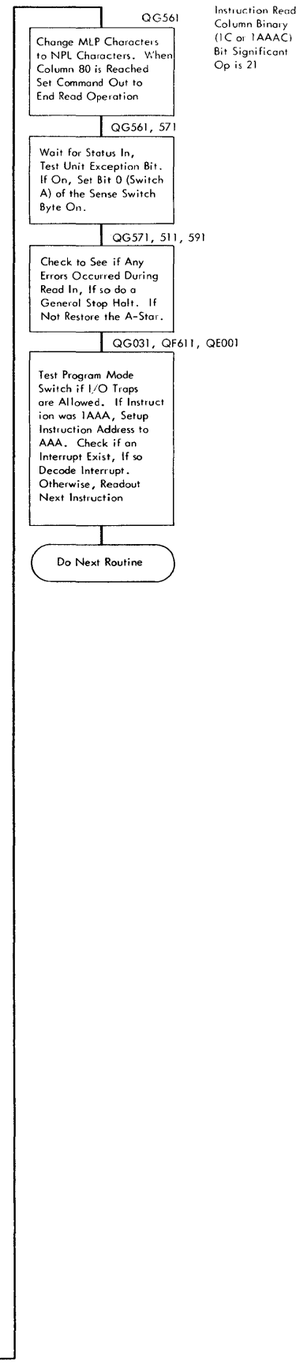


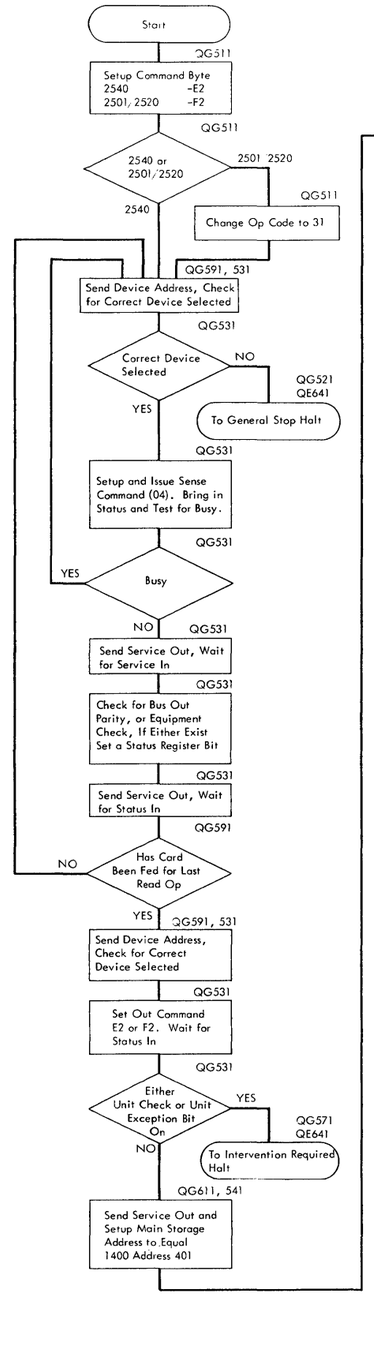
Chart 109
Punch
AH
Note: This Routine Transfers the Data to the Punch Control Unit Buffer.
QG521
Readout Character to be Punched
Column Binary Operation
Add 1 to Address. Remove Wordmark from Character if One Exists
Remove Wordmark from Character if One Exists. Do a Table Lookup in MPX storage for BCD Code of the Character. Change Storage Address
Operational In Dropped
Status In Up
Service In Up
Test Status Byte for Unit Check or Unit Exception Being Up
Readout Punch Address Byte and Reset Bit 2 (Error Bit)
Was Unit Check or Unit Exception Up
Reset FB Register (Select Out)
Setup Error Code
To General Stop
QE641
HB
Chart 155
Set Bus-Out Control Sent Service Out and Set Command Start
Readout Next Character to be Punched
Set A Status Register Bit to Allow Address Change in Column Binary
Change Op Code 24 to 20 Finished A4 to 28 PFR-Read
Column Binary Operation
Set B-Star to Ending Address
QG571
Send Service Out and Set Command Start
QG581
AJ
Chart 108

Instruction - Read (1 or 1AAA)
Bit Significant Op is 21

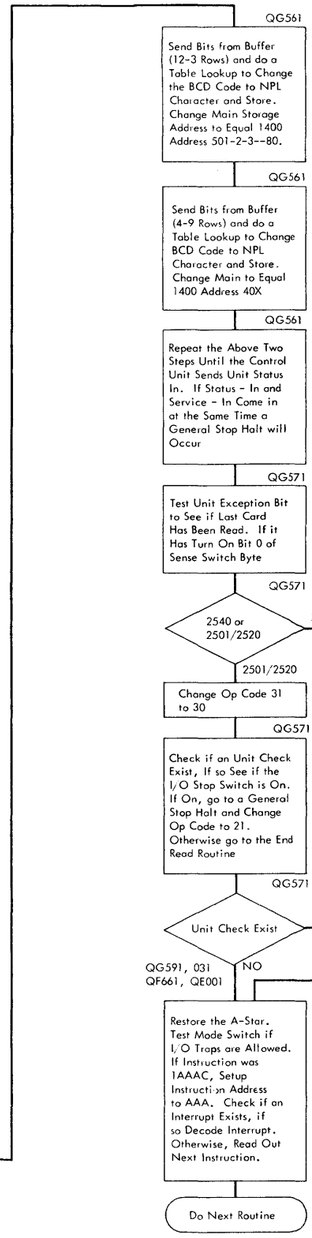


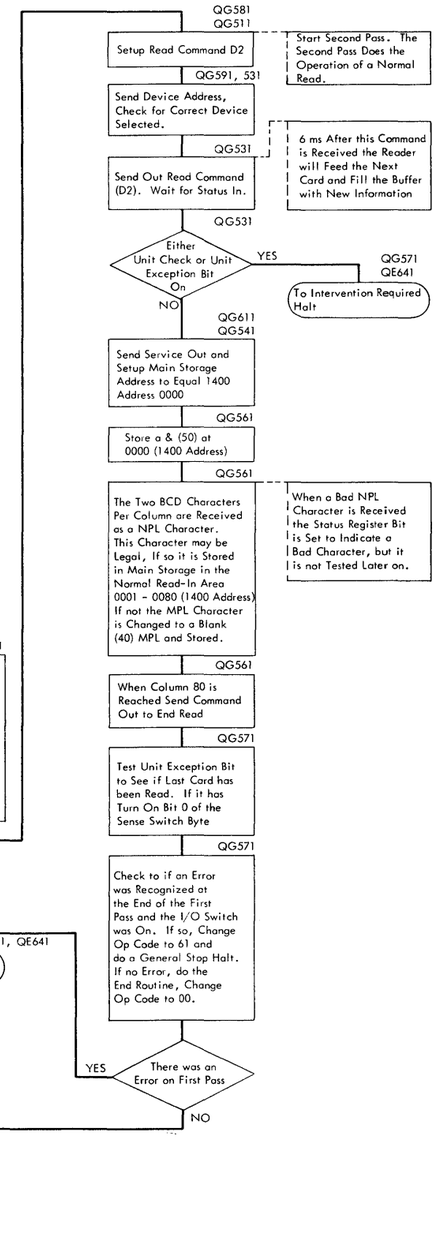
Instruction Read Column Binary (1C or 1AAAC) Bit Significant Op is 21



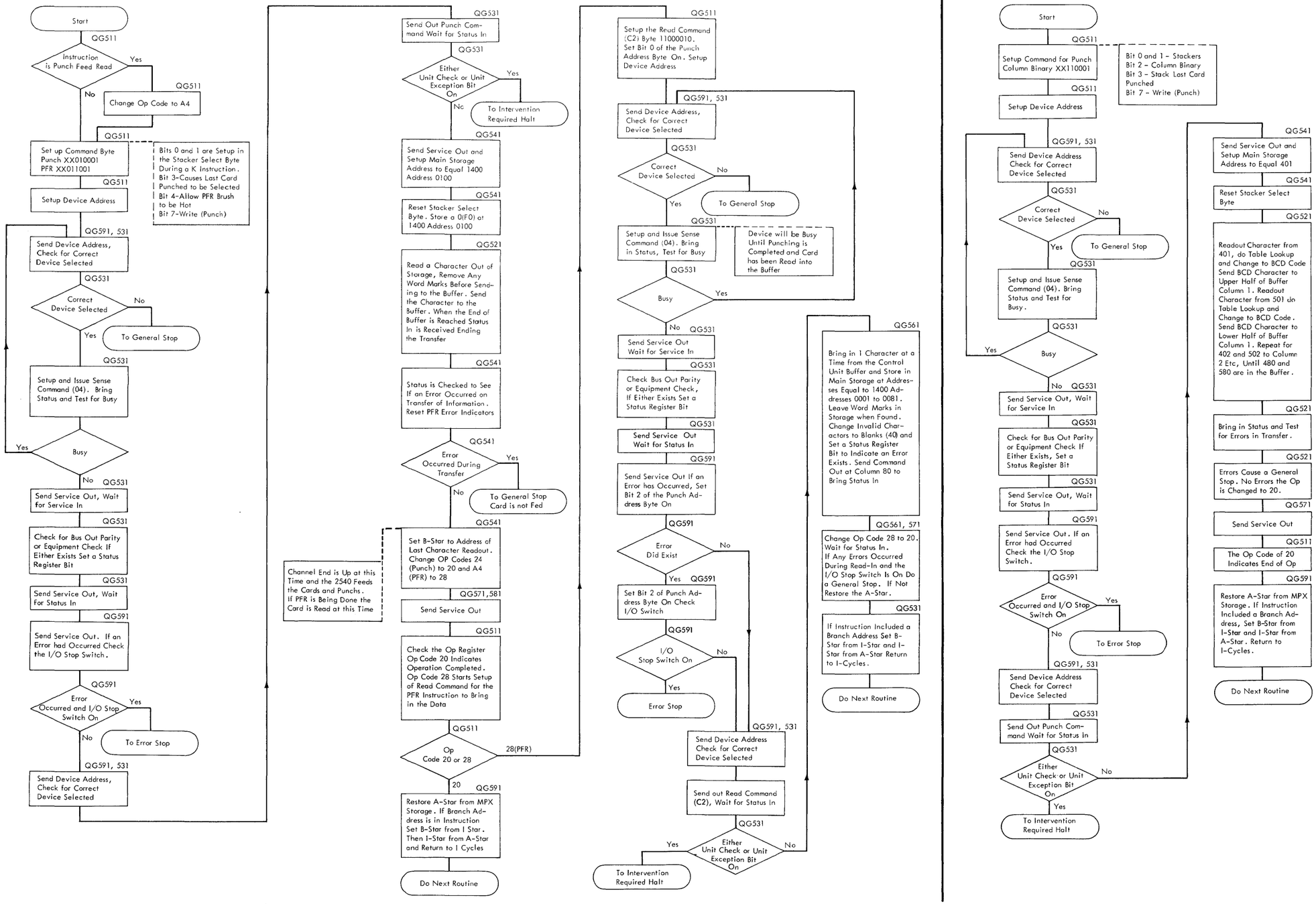


Note: Read Column Binary Operation Using a 2540 Requires Reading Out the Buffer Twice, So Two Passes are Made through the Routine.



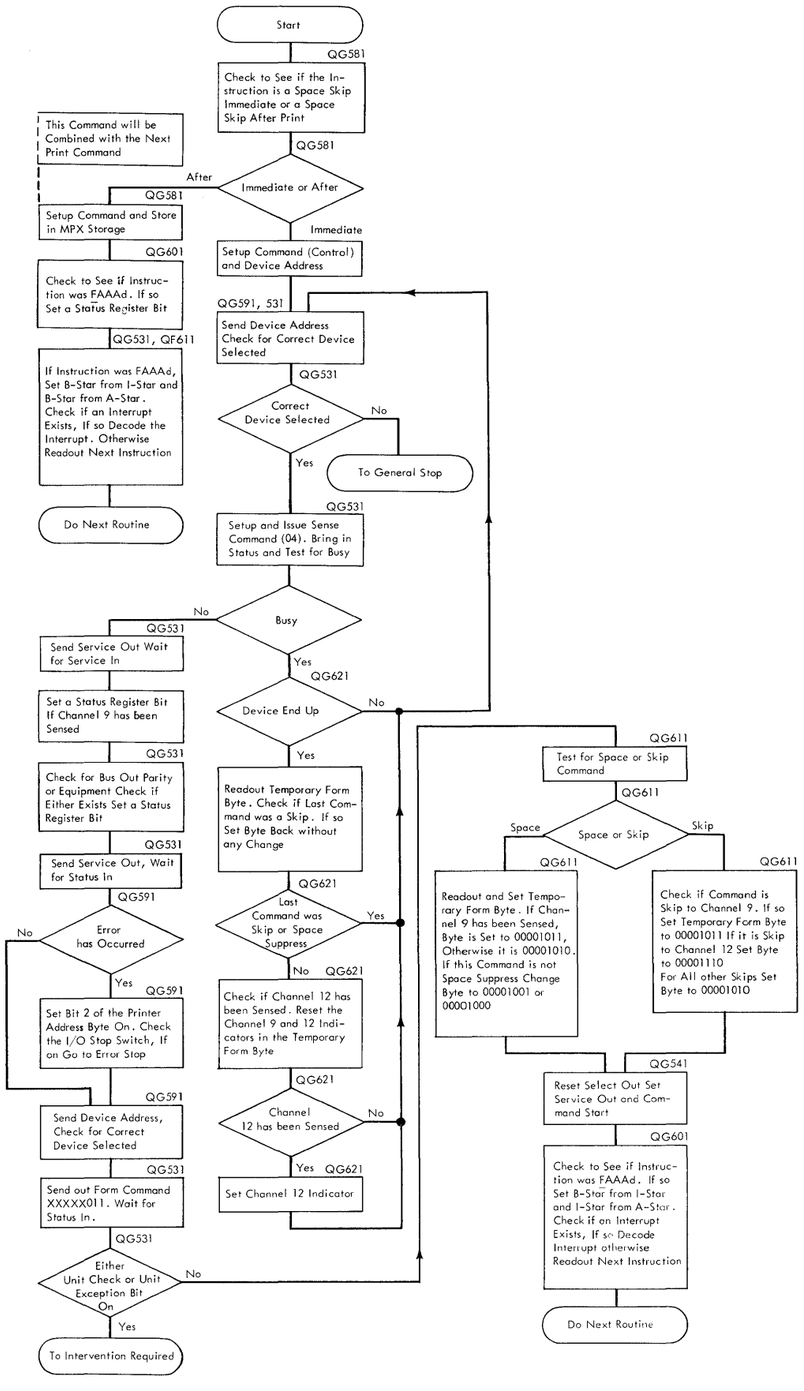


Instruction - 4, 4AAA_, 4R, or 4AAAR. .
Device - 2540

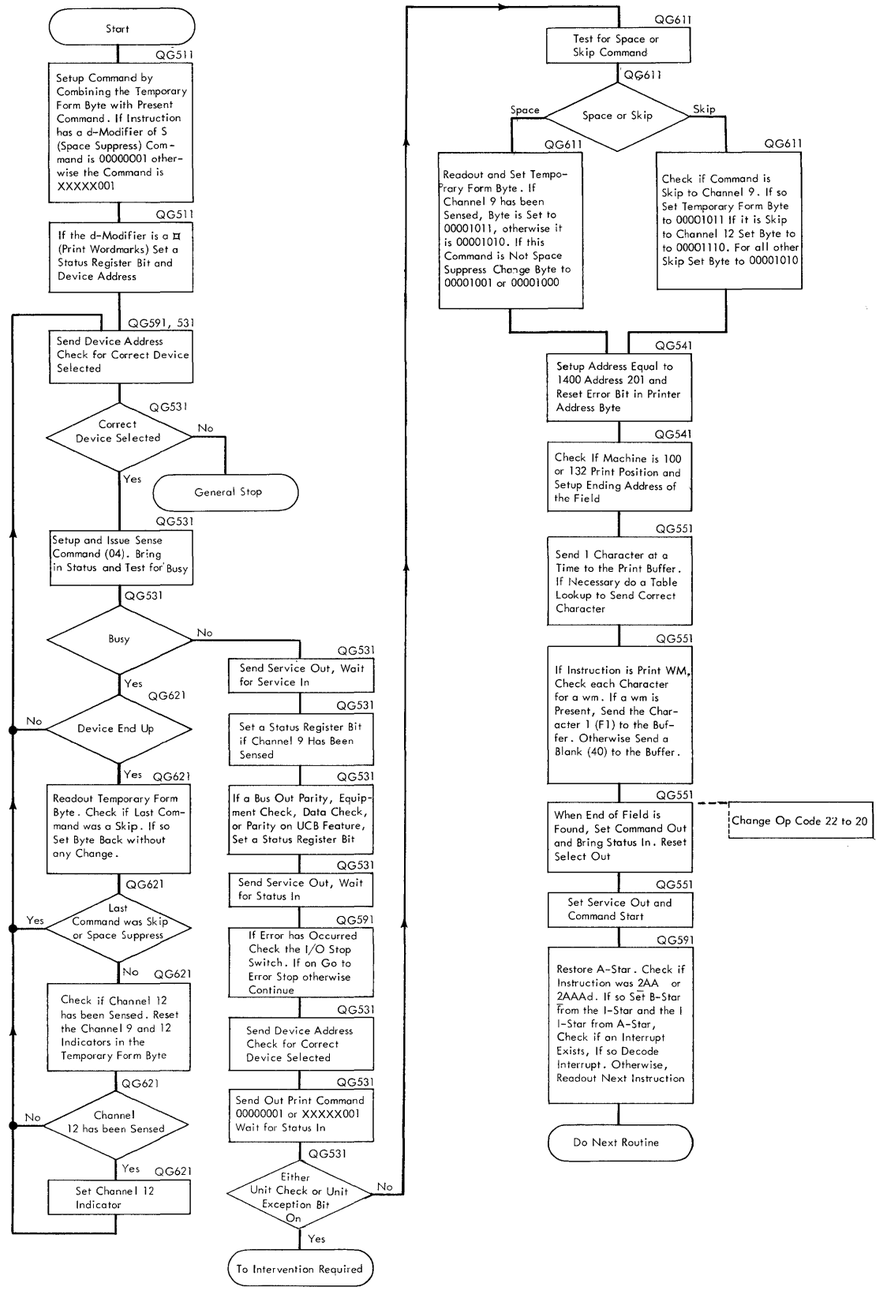


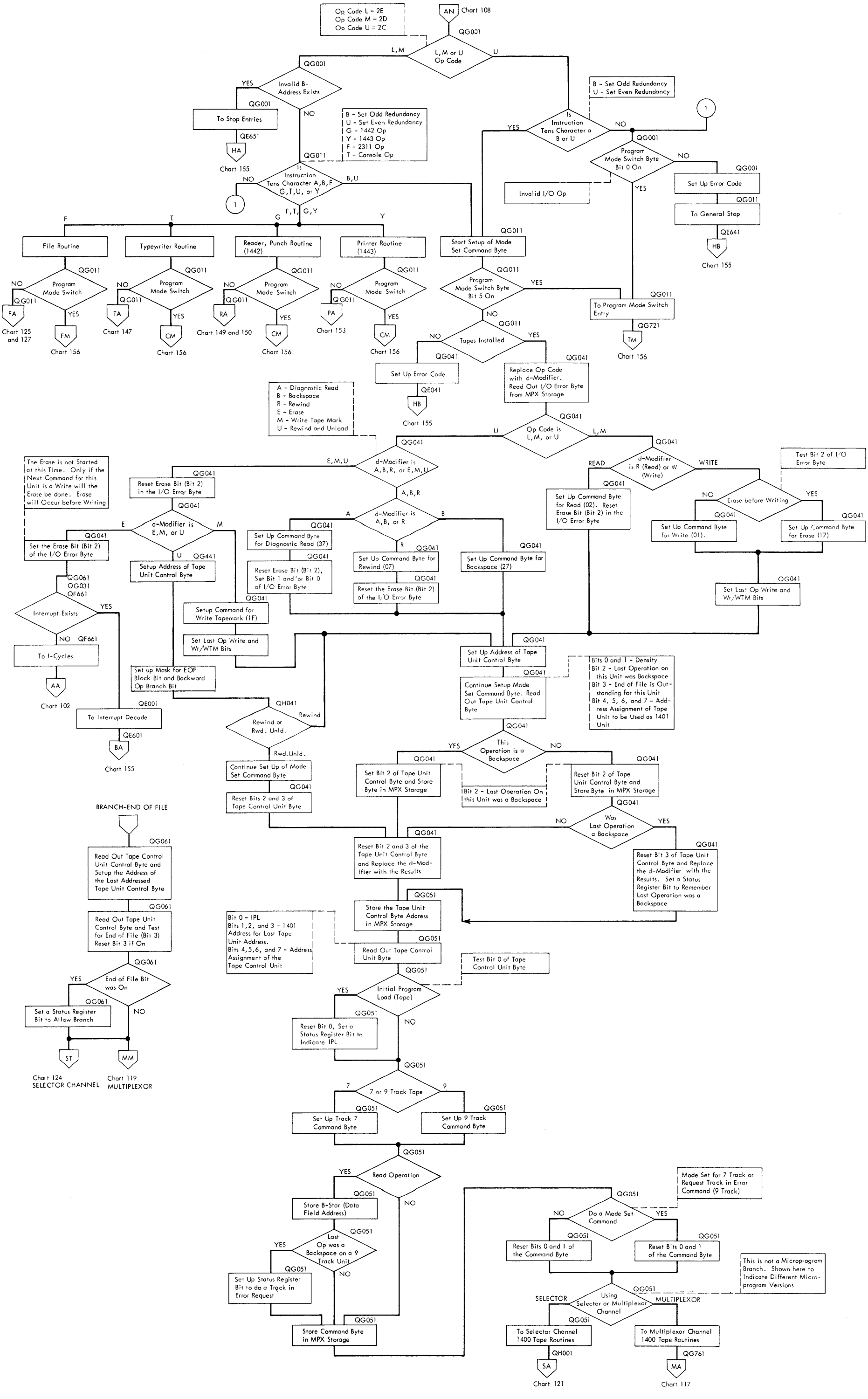
Instruction - 4C_ or 4AAAC_
Device - 2540

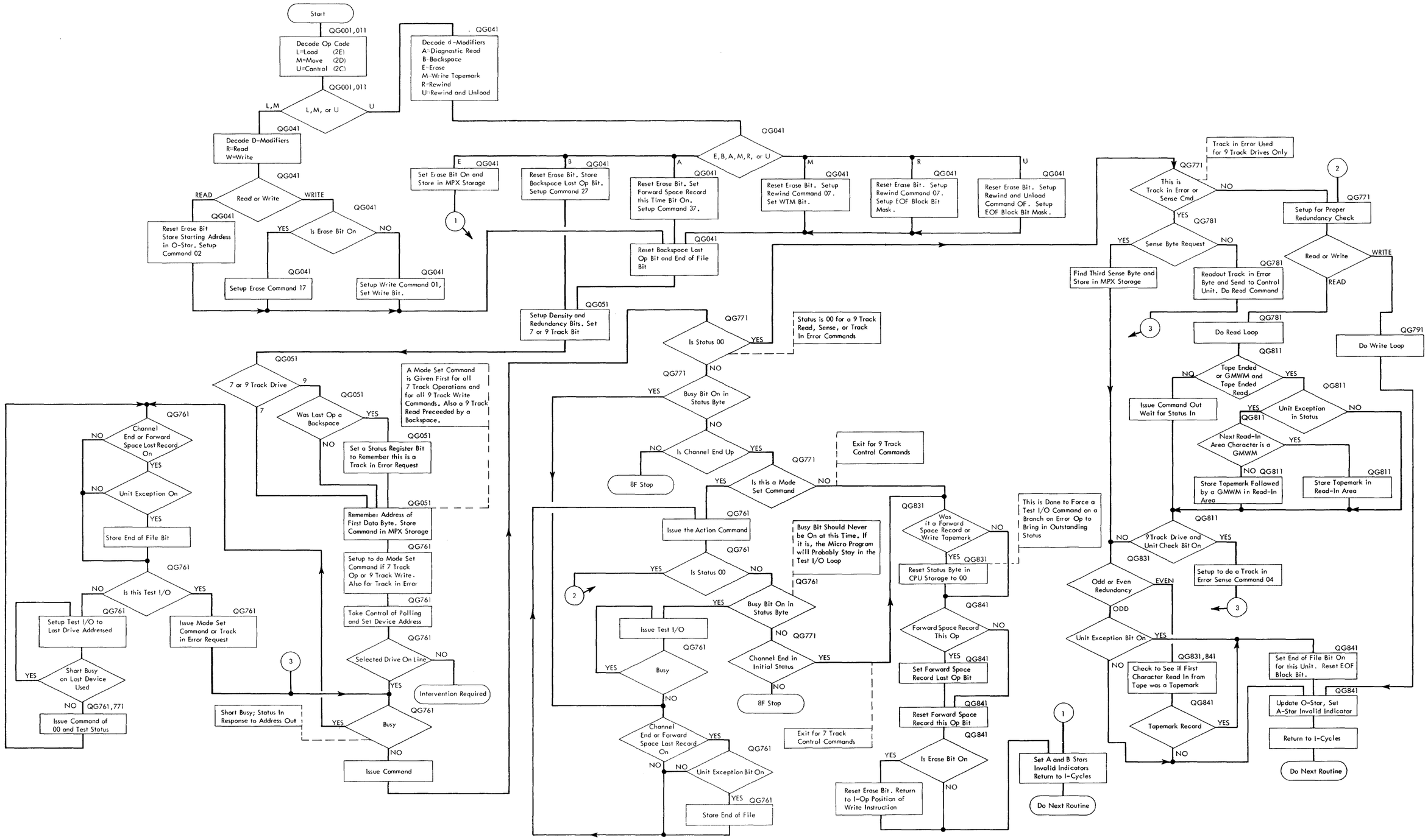
Forms Instruction Fd or FAAAd
Device 1403

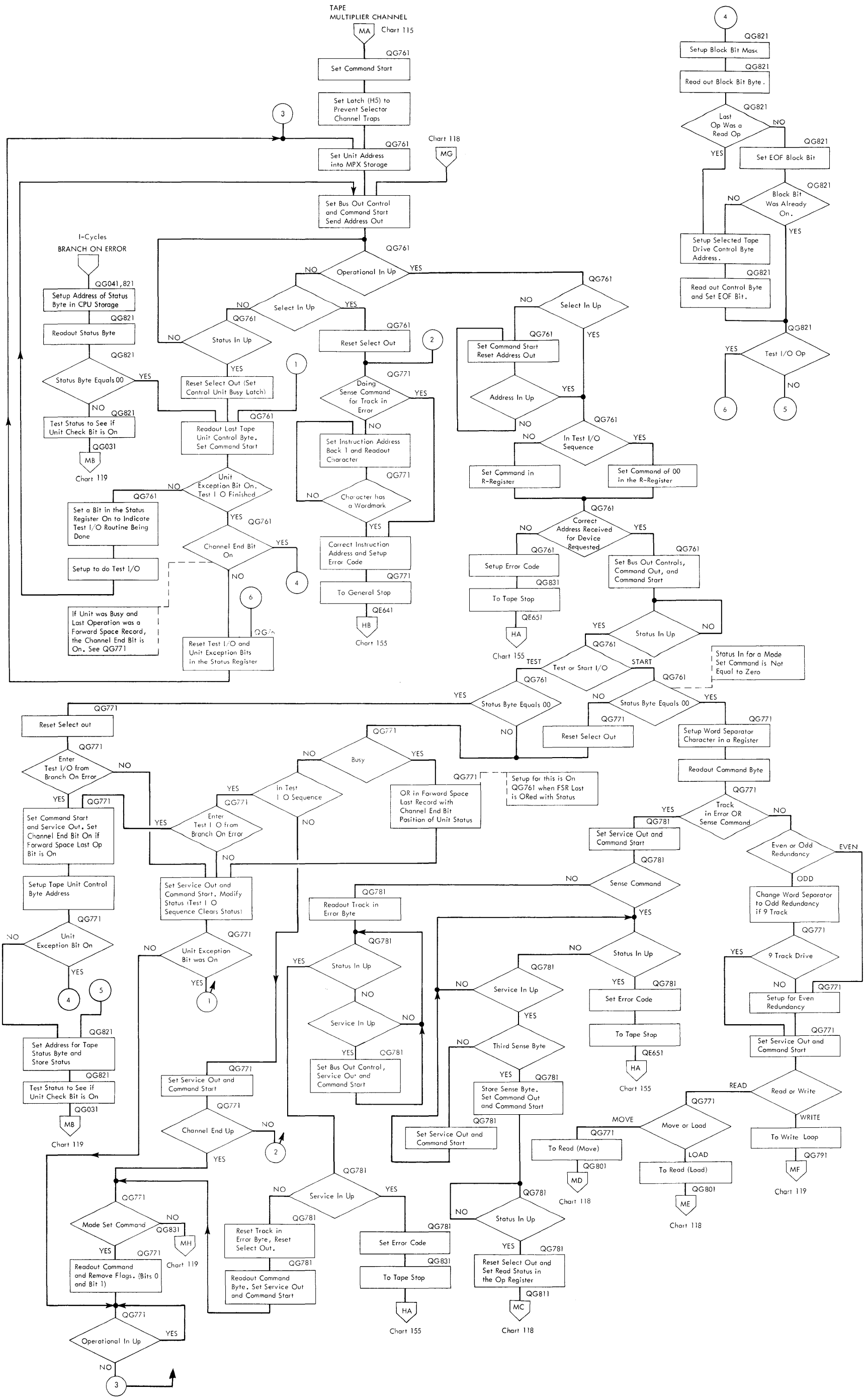


Print Instruction - 2, 2d, 2AAA, or 2AAAd
Device 1403

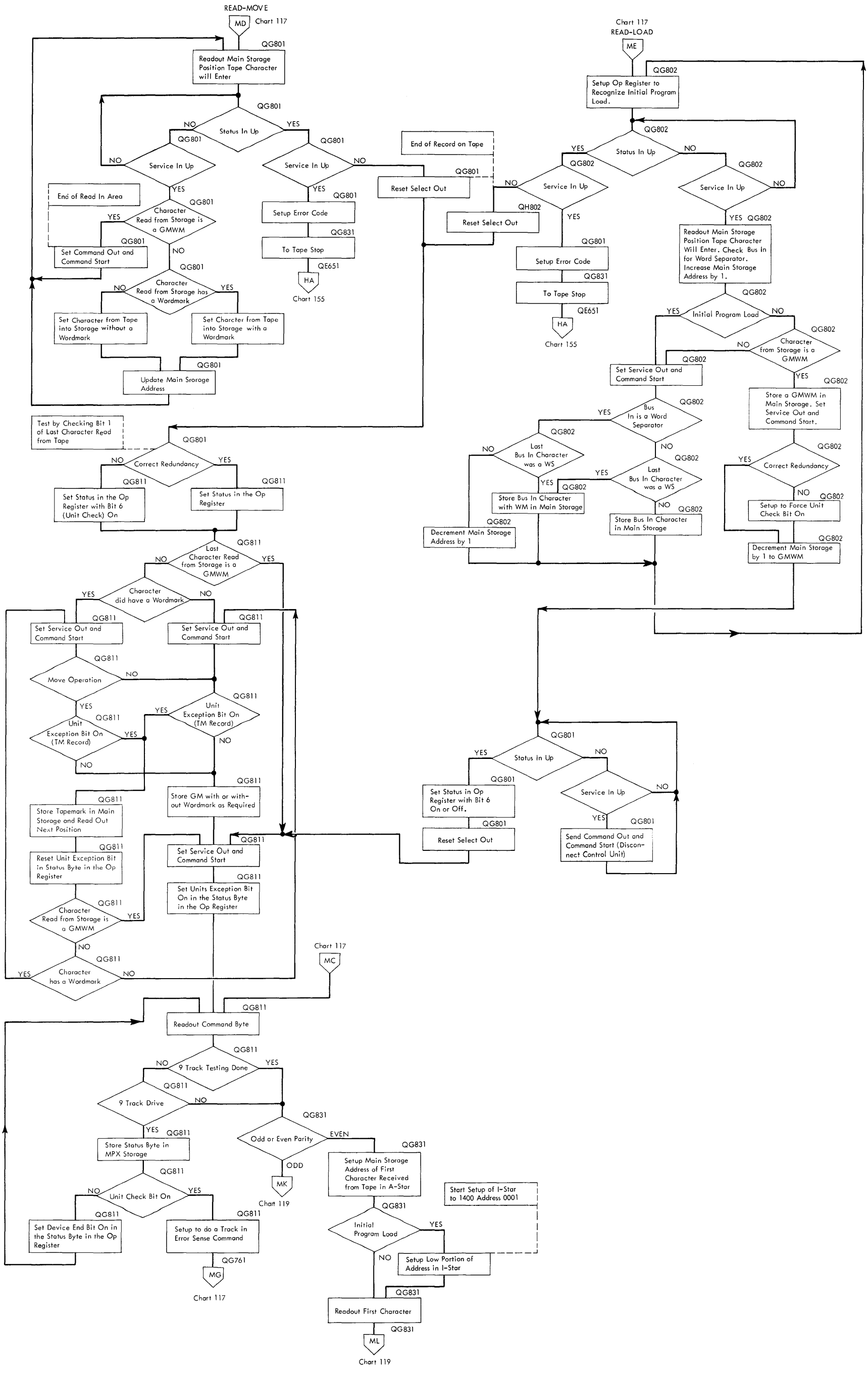


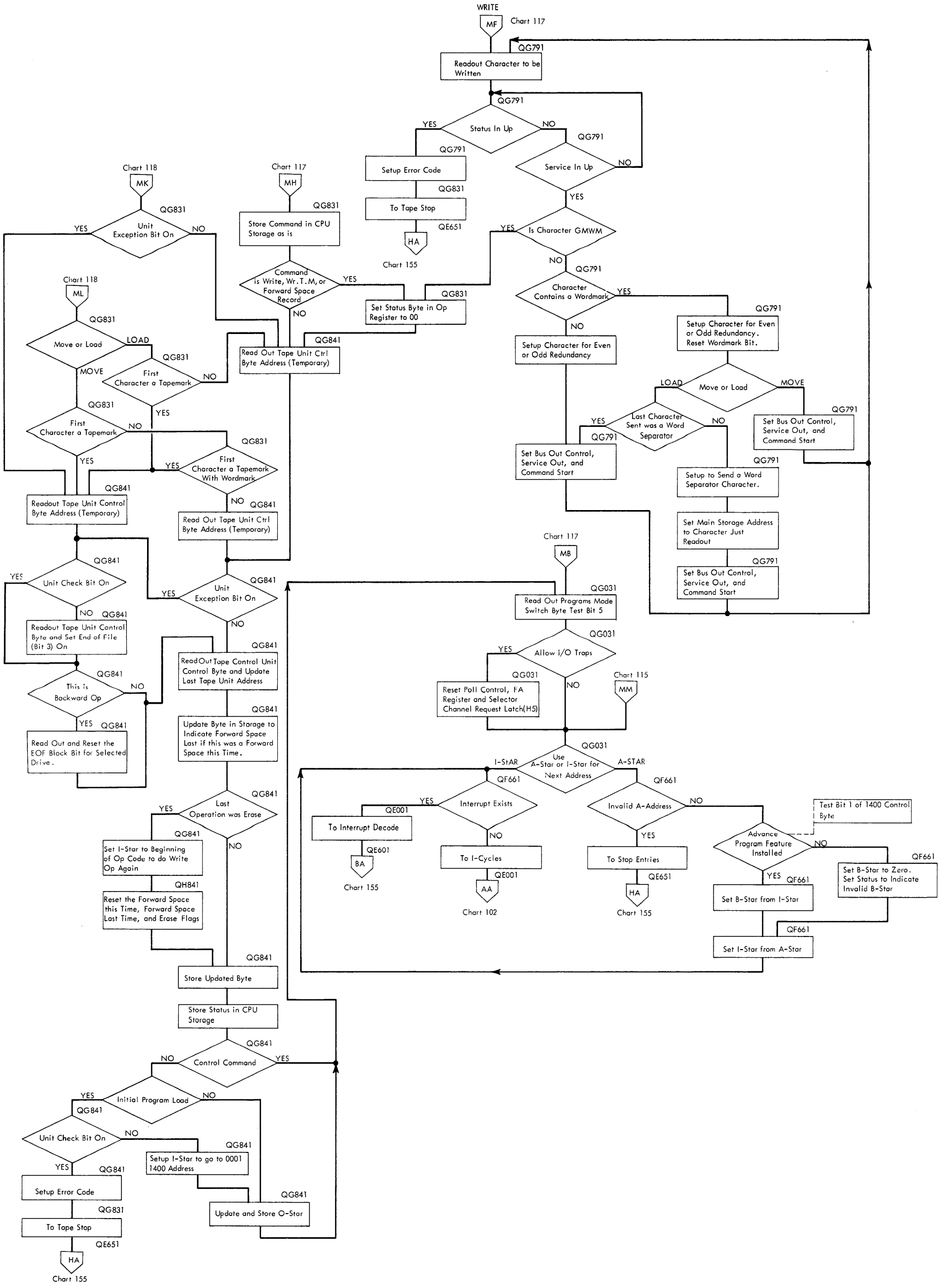

Op Code L = 2E
Op Code M = 2D
Op Code U = 2C
AN
Chart 108
QG001
L, M or U Op Code
L, M
U
QG001
Invalid B-Address Exists
YES
NO
QG001
To Stop Entries
QE651
HA
Chart 155
B - Set Odd Redundancy
U - Set Even Redundancy
G - 1442 Op
Y - 1443 Op
F - 2311 Op
T - Console Op
QG011
Is Instruction Tens Character A,B,F G,T,U, or Y
NO
B,U
1
F,T, G,Y
F
T
G
Y
File Routine
Typewriter Routine
Reader, Punch Routine (1442)
Printer Routine (1443)
QG011
Program Mode Switch
NO
YES
QG011
FA
Chart 125 and 127
FM
Chart 156
TA
Chart 147
CM
Chart 156
RA
Chart 149 and 150
CM
Chart 156
PA
Chart 153
CM
Chart 156
B - Set Odd Redundancy
U - Set Even Redundancy
Is Instruction Tens Character a B or U
YES
NO
1
QG001
Program Mode Switch Byte Bit 0 On
NO
YES
QG001
Set Up Error Code
QG011
To General Stop
QE641
HB
Chart 155
Invalid I/O Op
QG011
Start Setup of Mode Set Command Byte
QG011
Program Mode Switch Byte Bit 5 On
YES
NO
QG011
To Program Mode Switch Entry
QG721
TM
Chart 156
QG011
Tapes Installed
NO
YES
QG041
Set Up Error Code
QE041
HB
Chart 155
QG041
Replace Op Code with d-Modifier. Read Out I/O Error Byte from MPX Storage
A - Diagnostic Read
B - Backspace
R - Rewind
E - Erase
M - Write Tape Mark
U - Rewind and Unload
QG041
Op Code is L,M, or U
U
L,M
QG041
d-Modifier is A,B,R, or E,M,U
E,M,U
A,B,R
QG041
d-Modifier is R (Read) or W (Write)
READ
WRITE
Test Bit 2 of I/O Error Byte
The Erase is not Started at this Time. Only if the Next Command for this Unit is a Write will the Erase be done. Erase will Occur before Writing
QG041
Reset Erase Bit (Bit 2) in the I/O Error Byte
QG041
d-Modifier is E,M, or U
E
M
U
QG441
Setup Address of Tape Unit Control Byte
QG041
Set the Erase Bit (Bit 2) of the I/O Error Byte
QG061
QG031
QF661
Interrupt Exists
YES
NO
QF661
To I-Cycles
AA
Chart 102
QE001
To Interrupt Decode
QE601
BA
Chart 155
QG041
Setup Command for Write Tapemark (1F)
Set Last Op Write and Wr/WTM Bits
Set up Mask for EOF Block Bit and Backward Op Branch Bit
QH041
Rewind or Rwd. Unld.
Rewind
Rwd.Unld.
Continue Set Up of Mode Set Command Byte
QG041
Reset Bits 2 and 3 of Tape Control Unit Byte
A
B
R
QG041
d-Modifier is A,B, or R
QG041
Set Up Command Byte for Diagnostic Read (37)
QG041
Reset Erase Bit (Bit 2), Set Bit 1 and/or Bit 0 of I/O Error Byte
QG041
Set Up Command Byte for Rewind (07)
QG041
Reset the Erase Bit (Bit 2) of the I/O Error Byte
QG041
Set Up Command Byte for Backspace (27)
QG041
Set Up Command Byte for Read (02). Reset Erase Bit (Bit 2) in the I/O Error Byte
NO
YES
Erase before Writing
QG041
Set Up Command Byte for Write (01).
QG041
Set Up Command Byte for Erase (17)
QG041
Set Last Op Write and Wr/WTM Bits
QG041
Set Up Address of Tape Unit Control Byte
QG041
Continue Setup Mode Set Command Byte. Read Out Tape Unit Control Byte
Bits 0 and 1 - Density
Bit 2 - Last Operation on this Unit was Backspace
Bit 3 - End of File is Outstanding for this Unit
Bit 4, 5, 6, and 7 - Address Assignment of Tape Unit to be Used as 1401 Unit
QG041
This Operation is a Backspace
YES
NO
QG041
Set Bit 2 of Tape Unit Control Byte and Store Byte in MPX Storage
Bit 2 - Last Operation On this Unit was a Backspace
QG041
Reset Bit 2 of Tape Unit Control Byte and Store Byte in MPX Storage
QG041
Was Last Operation a Backspace
NO
YES
QG041
Reset Bit 2 and 3 of the Tape Unit Control Byte and Replace the d-Modifier with the Results
QG041
Reset Bit 3 of Tape Control Unit Byte and Replace the d-Modifier with the Results. Set a Status Register Bit to Remember Last Operation was a Backspace
QG051
Store the Tape Unit Control Byte Address in MPX Storage
Bit 0 - IPL
Bits 1, 2, and 3 - 1401 Address for Last Tape Unit Address.
Bits 4, 5, 6, and 7 - Address Assignment of the Tape Control Unit
QG051
Read Out Tape Control Unit Byte
Test Bit 0 of Tape Control Unit Byte
QG051
Initial Program Load (Tape)
YES
NO
QG051
Reset Bit 0, Set a Status Register Bit to Indicate IPL
QG051
7 or 9 Track Tape
7
9
QG051
Set Up Track 7 Command Byte
QG051
Set Up 9 Track Command Byte
QG051
Read Operation
YES
NO
QG051
Store B-Star (Data Field Address)
QG051
Last Op was a Backspace on a 9 Track Unit
YES
NO
QG051
Set Up Status Register Bit to do a Track in Error Request
QG051
Store Command Byte in MPX Storage
Mode Set for 7 Track or Request Track in Error Command (9 Track)
QG051
Do a Mode Set Command
NO
YES
QG051
Reset Bits 0 and 1 of the Command Byte
QG051
Reset Bits 0 and 1 of the Command Byte
This is not a Microprogram Branch. Shown here to Indicate Different Microprogram Versions
QG051
Using Selector or Multiplexor Channel
SELECTOR
MULTIPLEXOR
QG051
To Selector Channel 1400 Tape Routines
QH001
SA
Chart 121
To Multiplexor Channel 1400 Tape Routines
QG761
MA
Chart 117
BRANCH-END OF FILE
QG061
Read Out Tape Control Unit Control Byte and Setup the Address of the Last Addressed Tape Unit Control Byte
QG061
Read Out Tape Unit Control Byte and Test for End of File (Bit 3) Reset Bit 3 if On
QG061
End of File Bit was On
YES
NO
QG061
Set a Status Register Bit to Allow Branch
ST
Chart 124 SELECTOR CHANNEL
MM
Chart 119 MULTIPLEXOR

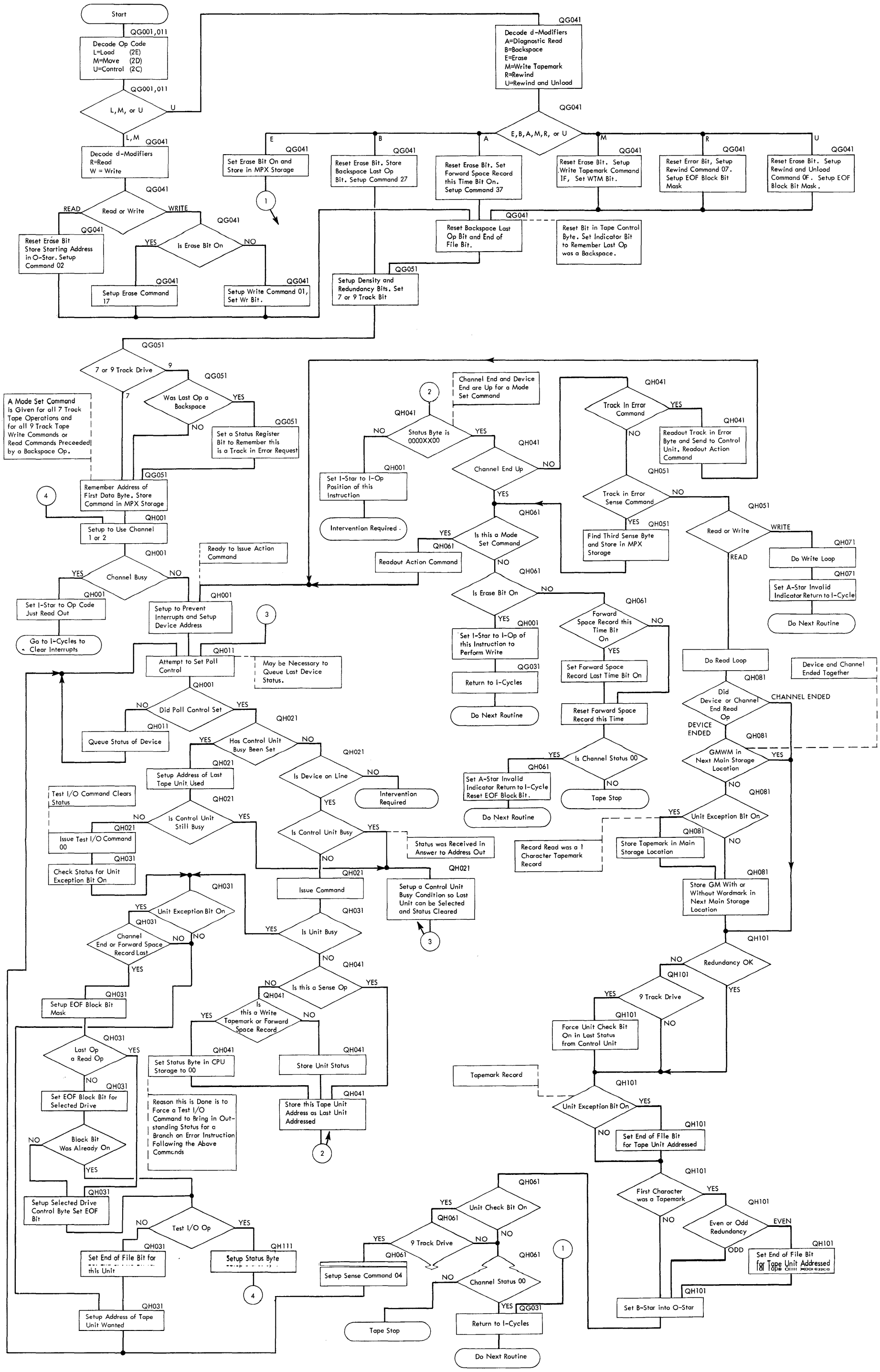

Start
QG001,011
Decode Op Code
L=Load (2E)
M=Move (2D)
U=Control (2C)
QG001,011
L, M, or U
L,M
U
QG041
Decode D-Modifiers
R=Read
W=Write
QG041
Read or Write
READ
WRITE
QG041
Reset Erase Bit
Store Starting Adrdess in O-Star. Setup Command 02
QG041
Is Erase Bit On
YES
NO
QG041
Setup Erase Command 17
QG041
Setup Write Command 01, Set Write Bit.
QG041
Decode d-Modifiers
A-Diagnostic Read
B-Backspace
E-Erase
M-Write Tapemark
R-Rewind
U-Rewind and Unload
QG041
E, B, A, M, R, or U
E
QG041
Set Erase Bit On and Store in MPX Storage
B
QG041
Reset Erase Bit. Store Backspace Last Op Bit. Setup Command 27
A
QG041
Reset Erase Bit. Set Forward Space Record this Time Bit On. Setup Command 37.
M
QG041
Reset Erase Bit. Setup Rewind Command 07. Set WTM Bit.
R
QG041
Reset Erase Bit. Setup Rewind Command 07. Setup EOF Block Bit Mask.
U
QG041
Reset Erase Bit. Setup Rewind and Unload Command OF. Setup EOF Block Bit Mask.
1
QG041
Reset Backspace Last Op Bit and End of File Bit
QG051
Setup Density and Redundancy Bits. Set 7 or 9 Track Bit
QG051
7 or 9 Track Drive
9
7
QG051
Was Last Op a Backspace
YES
NO
A Mode Set Command is Given First for all 7 Track Operations and for all 9 Track Write Commands. Also a 9 Track Read Preceeded by a Backspace.
QG051
Set a Status Register Bit to Remember this is a Track in Error Request
QG051
Remember Address of First Data Byte. Store Command in MPX Storage
QG761
Setup to do Mode Set Command if 7 Track Op or 9 Track Write. Also for Track in Error
QG761
Take Control of Polling and Set Device Address
QG761
Selected Drive On Line
NO
YES
Intervention Required
QG761
Busy
YES
NO
Issue Command
Short Busy; Status In Response to Address Out
3
QG761
Channel End or Forward Space Last Record On
NO
YES
QG761
Unit Exception On
NO
YES
Store End of File Bit
QG761
Is this Test I/O
NO
YES
QG761
Setup Test I/O to Last Drive Addressed
QG761
Issue Mode Set Command or Track in Error Request
Short Busy on Last Device Used
YES
NO
QG761,771
Issue Command of 00 and Test Status
QG771
Is Status 00
YES
NO
Status is 00 for a 9 Track Read, Sense, or Track In Error Commands
QG771
Busy Bit On in Status Byte
YES
NO
QG771
Is Channel End Up
NO
YES
8F Stop
QG771
Is this a Mode Set Command
YES
NO
Exit for 9 Track Control Commands
QG761
Issue the Action Command
QG761
Is Status 00
YES
NO
Busy Bit Should Never be On at this Time. If it is, the Micro Program will Probably Stay in the Test I/O Loop
2
QG761
Busy Bit On in Status Byte
YES
NO
Issue Test I/O
QG761
Busy
YES
NO
QG771
Channel End in Initial Status
YES
NO
8F Stop
Exit for 7 Track Control Commands
Channel End or Forward Space Last Record On
YES
NO
QG761
Unit Exception Bit On
NO
YES
QG761
Store End of File
QG831
Was it a Forward Space Record or Write Tapemark
NO
YES
QG831
Reset Status Byte in CPU Storage to 00
This is Done to Force a Test I/O Command on a Branch on Error Op to Bring in Outstanding Status
QG841
Forward Space Record This Op
NO
YES
QG841
Set Forward Space Record Last Op Bit
QG841
Reset Forward Space Record this Op Bit
QG841
Is Erase Bit On
YES
NO
Reset Erase Bit. Return to I-Op Position of Write Instruction
1
Set A and B Stars Invalid Indicators Return to I-Cycles
Do Next Routine
Track in Error Used for 9 Track Drives Only
QG771
This is Track in Error or Sense Cmd
NO
YES
QG781
Sense Byte Request
YES
NO
Find Third Sense Byte and Store in MPX Storage
QG781
Readout Track in Error Byte and Send to Control Unit. Do Read Command
3
QG781
Do Read Loop
QG811
Tape Ended or GMWM and Tape Ended Read
NO
YES
Issue Command Out Wait for Status In
QG811
Unit Exception in Status
YES
NO
QG811
Next Read-In Area Character is a GMWM
YES
NO
QG811
Store Tapemark Followed by a GMWM in Read-In Area
QG811
Store Tapemark in Read-In Area
QG811
9 Track Drive and Unit Check Bit On
NO
YES
QG831
Odd or Even Redundancy
EVEN
ODD
Setup to do a Track in Error Sense Command 04
3
Unit Exception Bit On
YES
NO
QG831,841
Check to See if First Character Read In from Tape was a Tapemark
QG841
Tapemark Record
YES
NO
2
QG771
Setup for Proper Redundancy Check
QG771
Read or Write
READ
WRITE
QG791
Do Write Loop
QG841
Set End of File Bit On for this Unit. Reset EOF Block Bit.
QG841
Update O-Star, Set A-Star Invalid Indicator
Return to I-Cycles
Do Next Routine

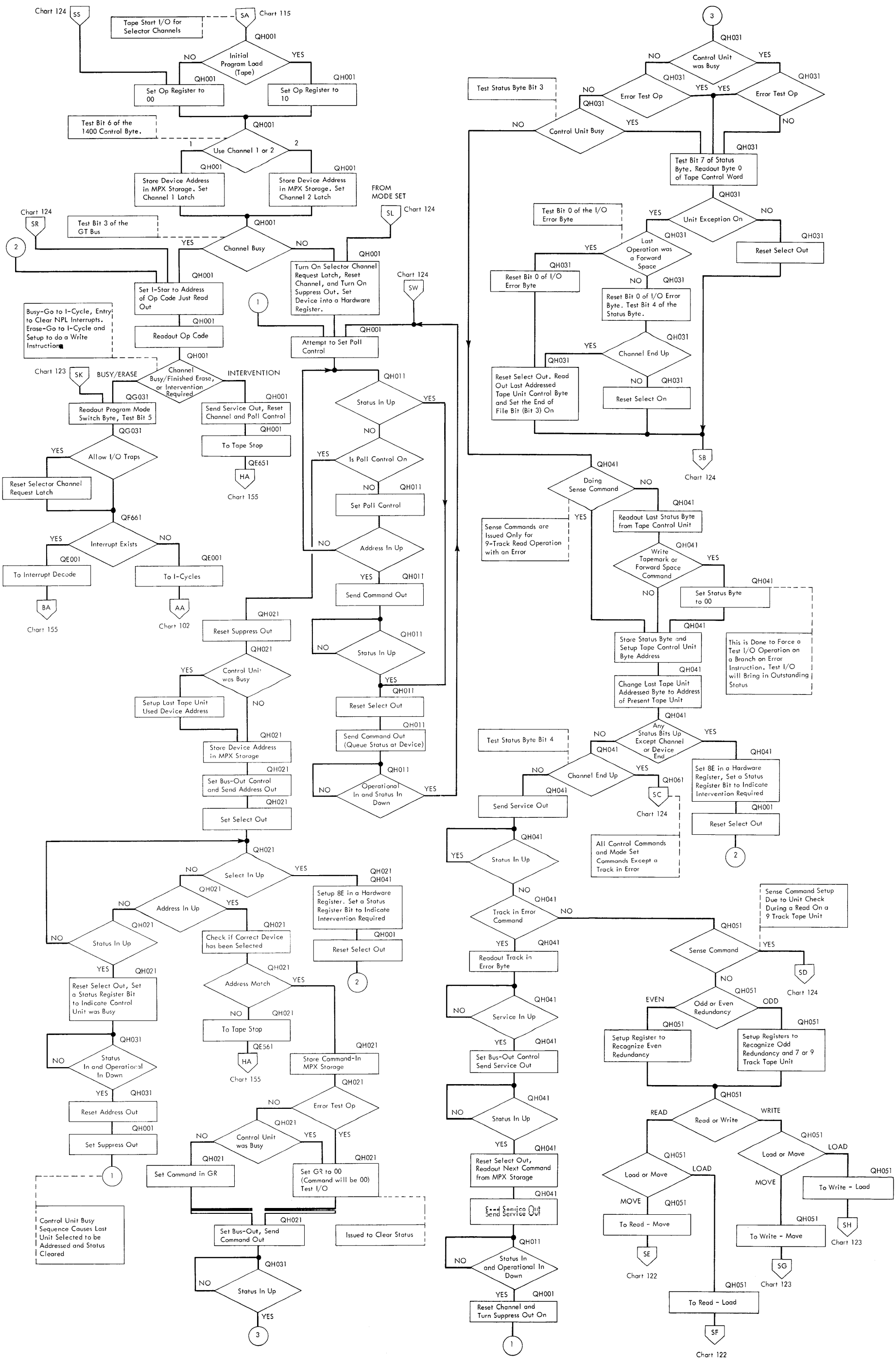


CLF 117 1400 Multiplexor Setup, Branch on Error

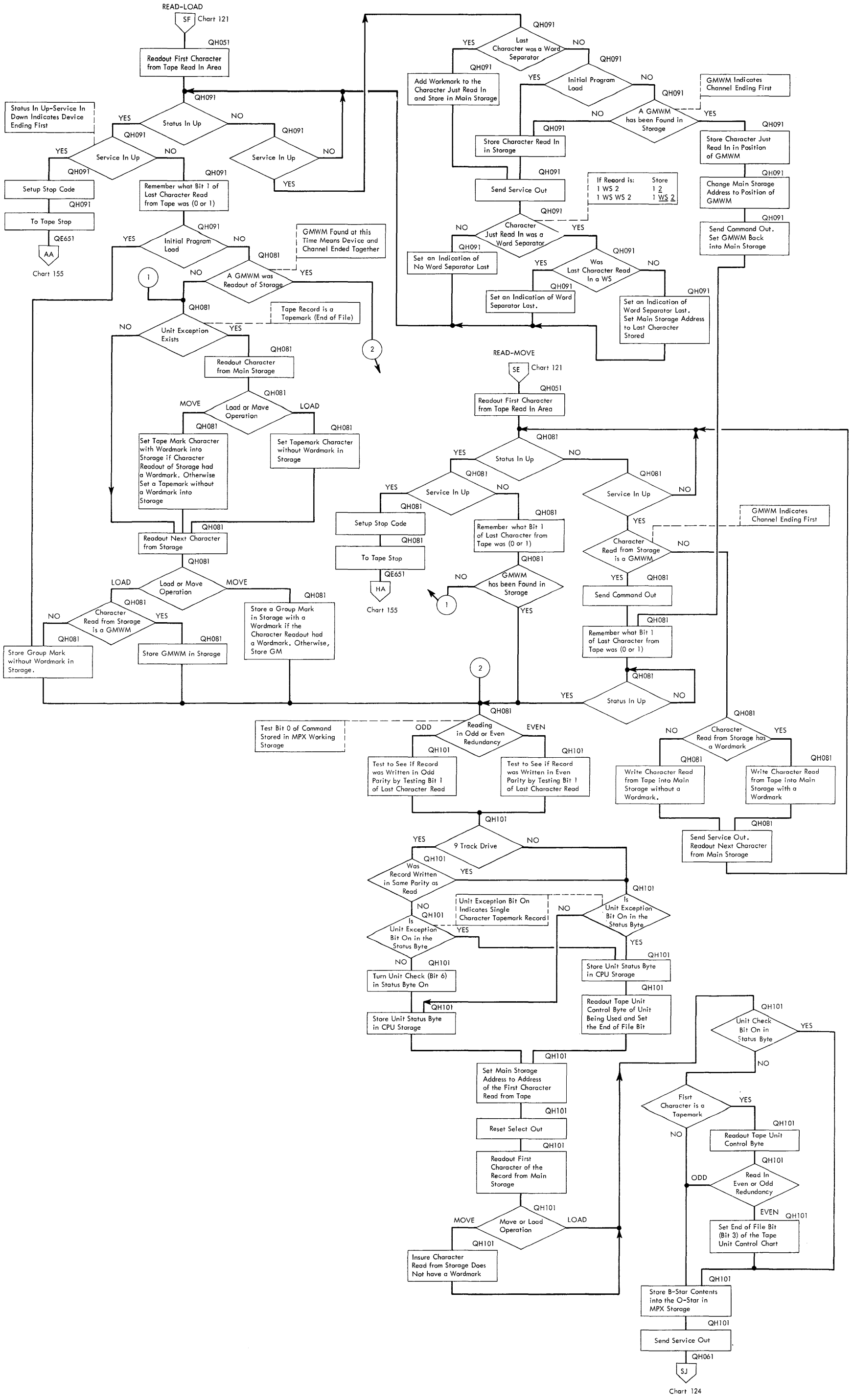

READ-MOVE
MD
Chart 117
QG801
Readout Main Storage Position Tape Character will Enter
Status In Up
Service In Up
End of Read In Area
Character Read from Storage is a GMWM
Set Command Out and Command Start
Character Read from Storage has a Wordmark
Set Character from Tape into Storage without a Wordmark
Set Charcter from Tape into Storage with a Wordmark
Update Main Srorage Address
Test by Checking Bit 1 of Last Character Read from Tape
Correct Redundancy
Set Status in the Op Register with Bit 6 (Unit Check) On
Set Status in the Op Register
QG811
Last Character Read from Storage is a GMWM
Character did have a Wordmark
Set Service Out and Command Start
Move Operation
Unit Exception Bit On (TM Record)
Store Tapemark in Main Storage and Read Out Next Position
Reset Unit Exception Bit in Status Byte in the Op Register
Character Read from Storage is a GMWM
Character has a Wordmark
Store GM with or without Wordmark as Required
Set Units Exception Bit On in the Status Byte in the Op Register
Chart 117
MC
Readout Command Byte
9 Track Testing Done
9 Track Drive
Store Status Byte in MPX Storage
Unit Check Bit On
Set Device End Bit On in the Status Byte in the Op Register
Setup to do a Track in Error Sense Command
QG761
MG
Chart 117
Odd or Even Parity
ODD
MK
Chart 119
EVEN
QG831
Setup Main Storage Address of First Character Received from Tape in A-Star
Initial Program Load
Start Setup of I-Star to 1400 Address 0001
Setup Low Portion of Address in I-Star
Readout First Character
ML
Chart 119
End of Record on Tape
Reset Select Out
QH802
Setup Error Code
To Tape Stop
QE651
HA
Chart 155
Chart 117
READ-LOAD
ME
Setup Op Register to Recognize Initial Program Load.
Readout Main Storage Position Tape Character Will Enter. Check Bus In for Word Separator. Increase Main Storage Address by 1.
Character from Storage is a GMWM
Set Service Out and Command Start
Store a GMWM in Main Storage. Set Service Out and Command Start.
Bus In is a Word Separator
Last Bus In Character was a WS
Store Bus In Character with WM in Main Storage
Decrement Main Storage Address by 1
Store Bus In Character in Main Storage
Correct Redundancy
Setup to Force Unit Check Bit On
Decrement Main Storage by 1 to GMWM
Set Status in Op Register with Bit 6 On or Off.
Send Command Out and Command Start (Disconnect Control Unit)

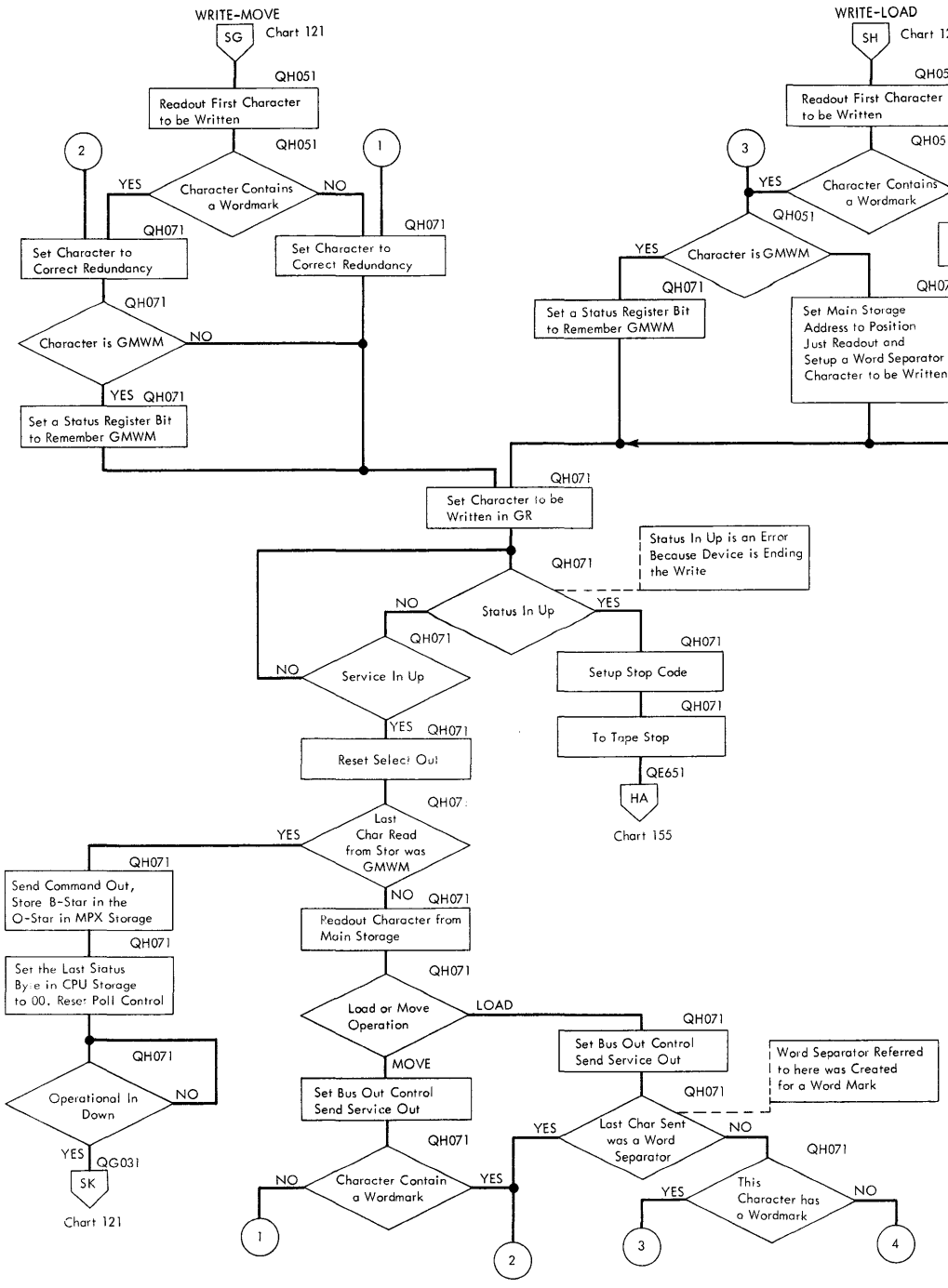

WRITE
MF
Chart 117
QG791
Readout Character to be Written
QG791
Status In Up
YES
NO
QG791
Service In Up
NO
YES
QG791
Setup Error Code
QG831
To Tape Stop
QE651
HA
Chart 155
YES
Is Character GMWM
NO
QG791
Character Contains a Wordmark
YES
NO
QG791
Setup Character for Even or Odd Redundancy. Reset Wordmark Bit.
Setup Character for Even or Odd Redundancy
LOAD
Move or Load
MOVE
QG791
Last Character Sent was a Word Separator
YES
NO
QG791
Set Bus Out Control, Service Out, and Command Start
QG791
Set Bus Out Control, Service Out, and Command Start
QG791
Setup to Send a Word Separator Character.
Set Main Storage Address to Character Just Readout
QG791
Set Bus Out Control, Service Out, and Command Start
Chart 118
MK
QG831
Unit Exception Bit On
YES
NO
Chart 118
ML
QG831
Move or Load
LOAD
MOVE
QG831
First Character a Tapemark
NO
YES
QG831
First Character a Tapemark
NO
YES
QG831
First Character a Tapemark With Wordmark
YES
NO
QG841
Readout Tape Unit Control Byte Address (Temporary)
QG841
Unit Check Bit On
YES
NO
QG841
Readout Tape Unit Control Byte and Set End of File (Bit 3) On
QG841
This is Backward Op
NO
YES
QG841
Read Out and Reset the EOF Block Bit for Selected Drive.
Chart 117
MH
QG831
Store Command in CPU Storage as is
Command is Write, Wr.T.M, or Forward Space Record
YES
NO
QG831
Set Status Byte in Op Register to 00
QG841
Read Out Tape Unit Ctrl Byte Address (Temporary)
QG841
Unit Exception Bit On
YES
NO
QG841
Read Out Tape Control Unit Control Byte and Update Last Tape Unit Address
QG841
Update Byte in Storage to Indicate Forward Space Last if this was a Forward Space this Time.
QG841
Last Operation was Erase
YES
NO
QG841
Set I-Star to Beginning of Op Code to do Write Op Again
QH841
Reset the Forward Space this Time, Forward Space Last Time, and Erase Flags
QG841
Store Updated Byte
Store Status in CPU Storage
QG841
Control Command
NO
YES
YES
Initial Program Load
NO
QG841
Unit Check Bit On
NO
YES
QG841
Setup Error Code
QG831
To Tape Stop
QE651
HA
Chart 155
QG841
Setup I-Star to go to 0001 1400 Address
QG841
Update and Store O-Star
Chart 117
MB
QG031
Read Out Programs Mode Switch Byte Test Bit 5
QG031
Allow I/O Traps
YES
NO
QG031
Reset Poll Control, FA Register and Selector Channel Request Latch(H5)
Chart 115
MM
QG031
Use A-Star or I-Star for Next Address
I-StAR
A-STAR
QF661
Interrupt Exists
YES
NO
QE001
To Interrupt Decode
QE601
BA
Chart 155
To I-Cycles
QE001
AA
Chart 102
QF661
Invalid A-Address
NO
YES
To Stop Entries
QE651
HA
Chart 155
Test Bit 1 of 1400 Control Byte
Advance Program Feature Installed
NO
YES
QF661
Set B-Star to Zero. Set Status to Indicate Invalid B-Star
QF661
Set B-Star from I-Star
QF661
Set I-Star from A-Star


Start
QG001,011
Decode Op Code
L=Load (2E)
M=Move (2D)
U=Control (2C)
QG001,011
L, M, or U
U
L, M
QG041
Decode d-Modifiers
R=Read
W = Write
QG041
Read or Write
READ
WRITE
QG041
Reset Erase Bit
Store Starting Address in O-Star. Setup Command 02
QG041
Is Erase Bit On
YES
NO
QG041
Setup Erase Command 17
QG041
Setup Write Command 01, Set Wr Bit.
QG041
Decode d-Modifiers
A=Diagnostic Read
B=Backspace
E=Erase
M=Write Tapemark
R=Rewind
U=Rewind and Unload
QG041
E, B, A, M, R, or U
E
QG041
Set Erase Bit On and Store in MPX Storage
B
QG041
Reset Erase Bit. Store Backspace Last Op Bit. Setup Command 27
A
Reset Erase Bit. Set Forward Space Record this Time Bit On. Setup Command 37
M
QG041
Reset Erase Bit. Setup Write Tapemark Command IF, Set WTM Bit.
R
QG041
Reset Error Bit, Setup Rewind Command 07. Setup EOF Block Bit Mask
U
QG041
Reset Erase Bit. Setup Rewind and Unload Command 0F. Setup EOF Block Bit Mask.
1
QG041
Reset Backspace Last Op Bit and End of File Bit.
QG041
Reset Bit in Tape Control Byte. Set Indicator Bit to Remember Last Op was a Backspace.
QG051
Setup Density and Redundancy Bits. Set 7 or 9 Track Bit
QG051
7 or 9 Track Drive
9
7
QG051
Was Last Op a Backspace
YES
NO
A Mode Set Command is Given for all 7 Track Tape Operations and for all 9 Track Tape Write Commands or Read Commands Preceeded by a Backspace Op.
QG051
Set a Status Register Bit to Remember this is a Track in Error Request
4
QG051
Remember Address of First Data Byte. Store Command in MPX Storage
QH001
Setup to Use Channel 1 or 2
QH001
Channel Busy
YES
NO
QH001
Set I-Star to Op Code Just Read Out
Go to I-Cycles to Clear Interrupts
Ready to Issue Action Command
QH001
Setup to Prevent Interrupts and Setup Device Address
3
QH011
Attempt to Set Poll Control
May be Necessary to Queue Last Device Status.
QH001
Did Poll Control Set
NO
YES
QH011
Queue Status of Device
QH021
Has Control Unit Busy Been Set
YES
NO
QH021
Setup Address of Last Tape Unit Used
Test I/O Command Clears Status
QH021
Is Control Unit Still Busy
NO
YES
QH021
Issue Test I/O Command 00
QH031
Check Status for Unit Exception Bit On
QH031
Unit Exception Bit On
YES
NO
QH031
Channel End or Forward Space Record Last
NO
YES
QH031
Setup EOF Block Bit Mask
QH031
Last Op a Read Op
YES
NO
QH031
Set EOF Block Bit for Selected Drive
NO
Block Bit Was Already On
YES
YES
QH031
Setup Selected Drive Control Byte Set EOF Bit
NO
Test I/O Op
YES
QH031
Set End of File Bit for this Unit
QH111
Setup Status Byte
4
QH031
Setup Address of Tape Unit Wanted
2
Channel End and Device End are Up for a Mode Set Command
QH041
Status Byte is 0000XX00
NO
YES
QH001
Set I-Star to I-Op Position of this Instruction
Intervention Required.
QH041
Channel End Up
NO
YES
QH061
Is this a Mode Set Command
YES
NO
QH061
Readout Action Command
QH061
Is Erase Bit On
NO
YES
QH001
Set I-Star to I-Op of this Instruction to Perform Write
QG031
Return to I-Cycles
Do Next Routine
QH061
Forward Space Record this Time Bit On
NO
YES
Set Forward Space Record Last Time Bit On
Reset Forward Space Record this Time
QH061
Is Channel Status 00
YES
NO
Tape Stop
QH061
Set A-Star Invalid Indicator Return to I-Cycle Reset EOF Block Bit.
Do Next Routine
QH021
Is Device on Line
NO
YES
Intervention Required
QH021
Is Control Unit Busy
YES
NO
Status was Received in Answer to Address Out
QH021
Issue Command
QH021
Setup a Control Unit Busy Condition so Last Unit can be Selected and Status Cleared
3
QH031
Is Unit Busy
YES
NO
QH041
Is this a Sense Op
NO
YES
QH041
Is this a Write Tapemark or Forward Space Record
YES
NO
QH041
Set Status Byte in CPU Storage to 00
QH041
Store Unit Status
QH041
Store this Tape Unit Address as Last Unit Addressed
Reason this is Done is to Force a Test I/O Command to Bring in Outstanding Status for a Branch on Error Instruction Following the Above Commands
2
QH061
Unit Check Bit On
YES
NO
QH061
9 Track Drive
YES
NO
QH061
Setup Sense Command 04
QH061
Channel Status 00
NO
YES
QG031
Return to I-Cycles
Do Next Routine
Tape Stop
1
Record Read was a 1 Character Tapemark Record
QH041
Track In Error Command
YES
NO
QH041
Readout Track in Error Byte and Send to Control Unit. Readout Action Command
QH051
Track in Error Sense Command
NO
YES
QH051
Find Third Sense Byte and Store in MPX Storage
QH051
Read or Write
WRITE
READ
QH071
Do Write Loop
QH071
Set A-Star Invalid Indicator Return to I-Cycle
Do Next Routine
Do Read Loop
Device and Channel Ended Together
QH081
Did Device or Channel End Read Op
CHANNEL ENDED
DEVICE ENDED
QH081
GMWM in Next Main Storage Location
YES
NO
QH081
Unit Exception Bit On
YES
NO
QH081
Store Tapemark in Main Storage Location
QH081
Store GM With or Without Wordmark in Next Main Storage Location
QH101
Redundancy OK
NO
YES
QH101
9 Track Drive
YES
NO
QH101
Force Unit Check Bit On in Last Status from Control Unit
Tapemark Record
QH101
Unit Exception Bit On
YES
NO
QH101
Set End of File Bit for Tape Unit Addressed
QH101
First Character was a Tapemark
YES
NO
QH101
Even or Odd Redundancy
EVEN
ODD
QH101
Set End of File Bit for Tape Unit Addressed
QH101
Set B-Star into O-Star



CLF 121 1400 Tape - Selector Setup


READ-LOAD
SF
Chart 121
QH051
Readout First Character from Tape Read In Area
QH091
Status In Up
YES
NO
Status In Up-Service In Down Indicates Device Ending First
Service In Up
Setup Stop Code
To Tape Stop
QE651
AA
Chart 155
Remember what Bit 1 of Last Character Read from Tape was (0 or 1)
Initial Program Load
GMWM Found at this Time Means Device and Channel Ended Together
A GMWM was Readout of Storage
QH081
Tape Record is a Tapemark (End of File)
Unit Exception Exists
Readout Character from Main Storage
Load or Move Operation
MOVE
LOAD
Set Tape Mark Character with Wordmark into Storage if Character Readout of Storage had a Wordmark. Otherwise Set a Tapemark without a Wordmark into Storage
Set Tapemark Character without Wordmark in Storage
Readout Next Character from Storage
Character Read from Storage is a GMWM
Store Group Mark without Wordmark in Storage.
Store GMWM in Storage
Store a Group Mark in Storage with a Wordmark if the Character Readout had a Wordmark. Otherwise, Store GM
Add Workmark to the Character Just Read In and Store in Main Storage
Last Character was a Word Separator
Store Character Read In in Storage
Send Service Out
If Reaord is: 1 WS 2 / 1 WS WS 2
Store 1 2 / 1 WS 2
Character Just Read In was a Word Separator
Set an Indication of No Word Separator Last
Was Last Character Read In a WS
Set an Indication of Word Separator Last.
Set an Indication of Word Separator Last. Set Main Storage Address to Last Character Stored
GMWM Indicates Channel Ending First
A GMWM has been Found in Storage
Store Character Just Read In in Position of GMWM
Change Main Storage Address to Position of GMWM
Send Command Out. Set GMWM Back into Main Storage
READ-MOVE
SE
Chart 121
Readout First Character from Tape Read In Area
Setup Stop Code
To Tape Stop
HA
Chart 155
Remember what Bit 1 of Last Character from Tape was (0 or 1)
GMWM has been Found in Storage
Send Command Out
Remember what Bit 1 of Last Character from Tape was (0 or 1)
Test Bit 0 of Command Stored in MPX Working Storage
Reading in Odd or Even Redundancy
ODD
EVEN
Test to See if Record was Written in Odd Parity by Testing Bit 1 of Last Character Read
Test to See if Record was Written in Even Parity by Testing Bit 1 of Last Character Read
Character Read from Storage has a Wordmark
Write Character Read from Tape into Main Storage without a Wordmark.
Write Character Read from Tape into Main Storage with a Wordmark
Send Service Out. Readout Next Character from Main Storage
9 Track Drive
Was Record Written in Same Parity as Read
Unit Exception Bit On Indicates Single Character Tapemark Record
Is Unit Exception Bit On in the Status Byte
Turn Unit Check (Bit 6) in Status Byte On
Store Unit Status Byte in CPU Storage
Readout Tape Unit Control Byte of Unit Being Used and Set the End of File Bit
Unit Check Bit On in Status Byte
Fisrt Character is a Tapemark
Readout Tape Unit Control Byte
Read In Even or Odd Redundancy
Set End of File Bit (Bit 3) of the Tape Unit Control Chart
Set Main Storage Address to Address of the First Character Read from Tape
Reset Select Out
Readout First Character of the Record from Main Storage
Move or Load Operation
Insure Character Read from Storage Does Not have a Wordmark
Store B-Star Contents into the O-Star in MPX Storage
Send Service Out
QH061
SJ
Chart 124


WRITE-MOVE
SG
Chart 121
QH051
Readout First Character to be Written
QH051
Character Contains a Wordmark
YES
NO
2
1
QH071
Set Character to Correct Redundancy
QH071
Set Character to Correct Redundancy
QH071
Character is GMWM
NO
YES QH071
Set a Status Register Bit to Remember GMWM
WRITE-LOAD
SH
Chart 121
QH051
Readout First Character to be Written
QH051
Character Contains a Wordmark
YES
NO
3
4
QH071
Set Character to Correct Parity
QH051
Character is GMWM
YES
QH071
Set a Status Register Bit to Remember GMWM
QH071
Set Main Storage Address to Position Just Readout and Setup a Word Separator Character to be Written
QH071
Set Character to be Written in GR
Status In Up is an Error Because Device is Ending the Write
QH071
Status In Up
NO
YES
QH071
Service In Up
NO
YES QH071
Reset Select Out
QH071
Setup Stop Code
QH071
To Tape Stop
QE651
HA
Chart 155
QH07:
Last Char Read from Stor was GMWM
YES
NO QH071
Peadout Character from Main Storage
QH071
Load or Move Operation
LOAD
MOVE
QH071
Set Bus Out Control Send Service Out
QH071
Set Bus Out Control Send Service Out
Word Separator Referred to here was Created for a Word Mark
QH071
Last Char Sent was a Word Separator
YES
NO
QH071
This Character has a Wordmark
YES
NO
QH071
Character Contain a Wordmark
NO
YES
QH071
Send Command Out, Store B-Star in the O-Star in MPX Storage
QH071
Set the Last Status Byte in CPU Storage to 00. Reset Poll Control
QH071
Operational In Down
NO
YES QG031
SK
Chart 121
1
2
3
4

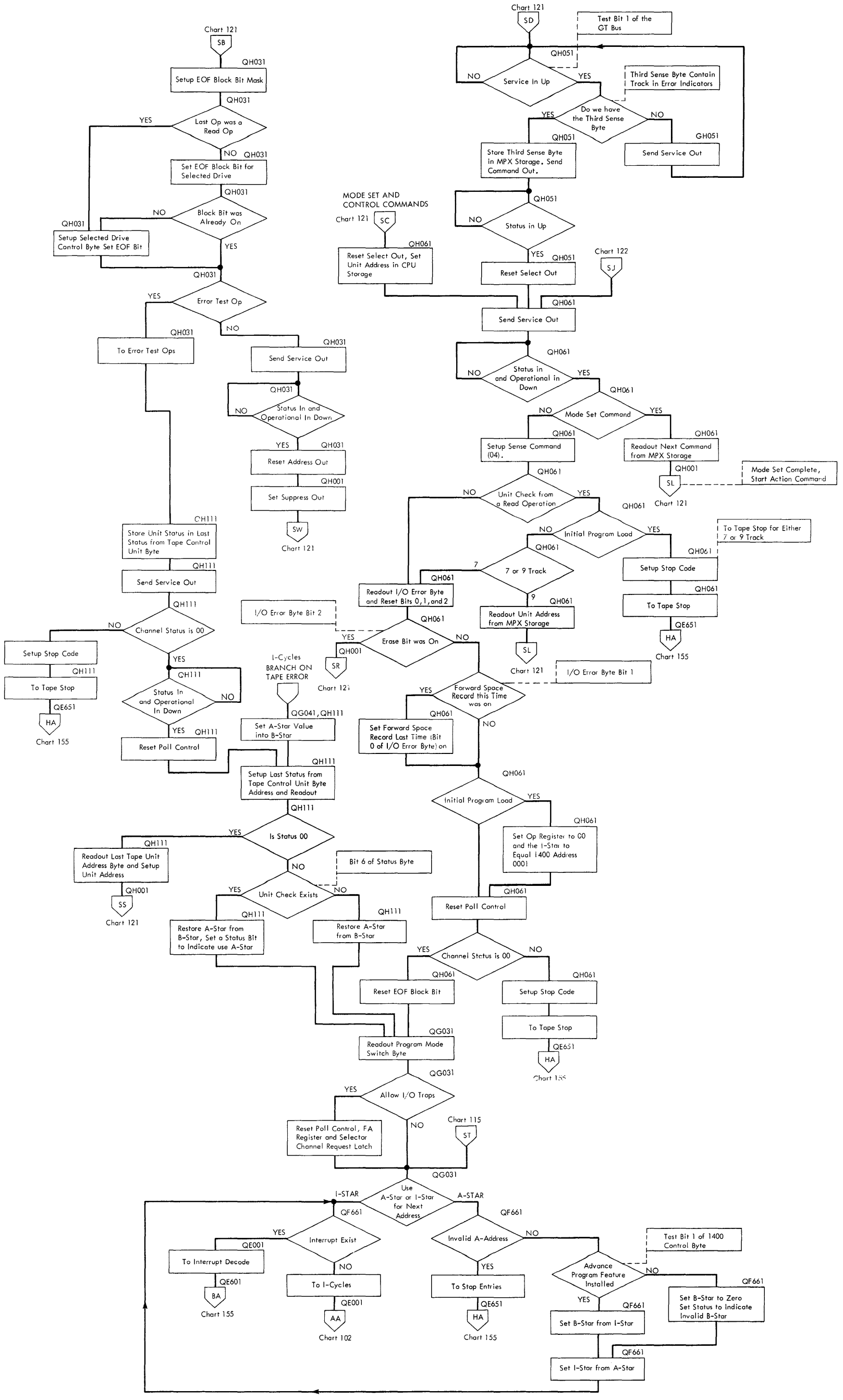
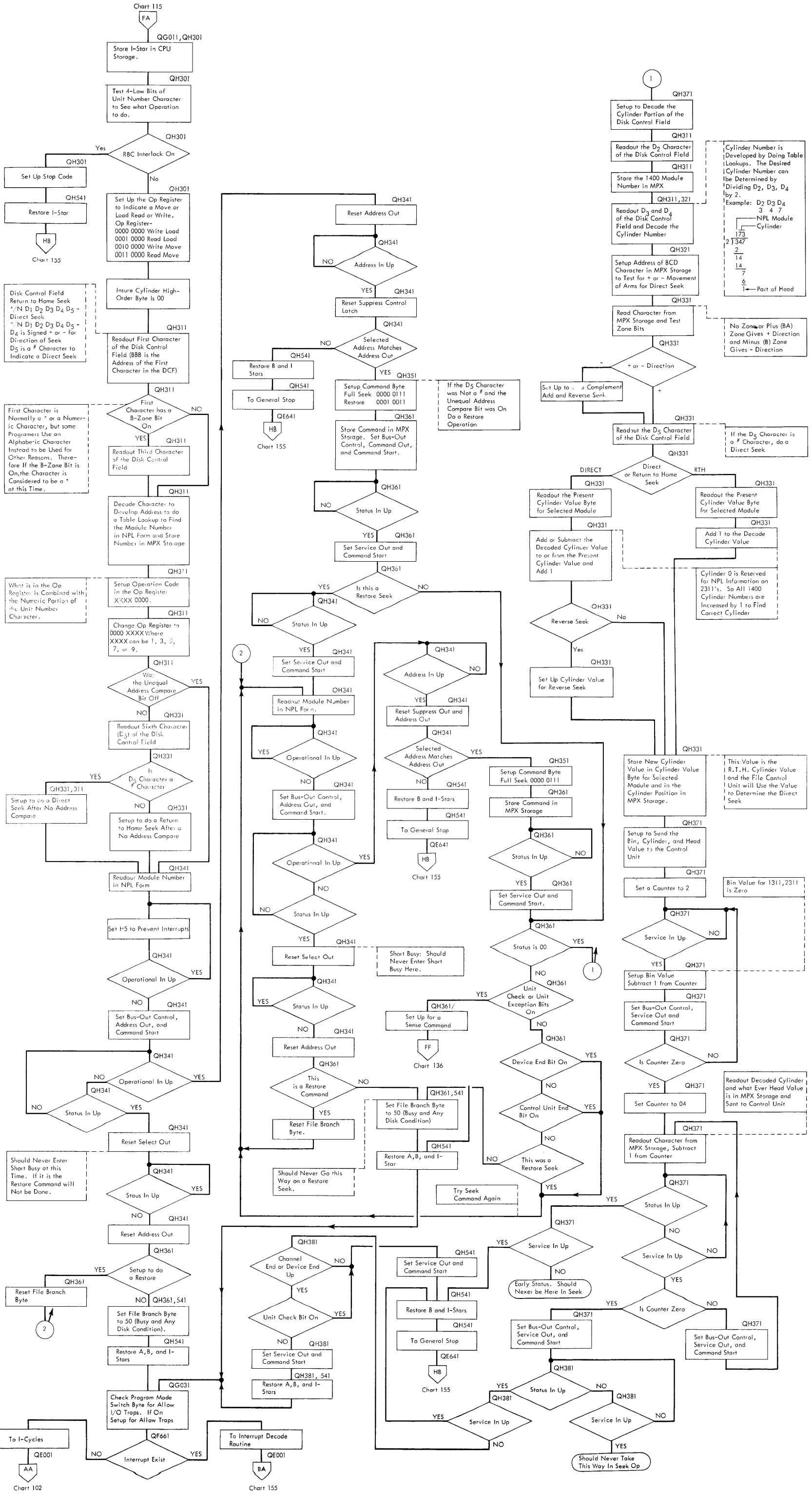


Chart 121
SB
QH031
Setup EOF Block Bit Mask
QH031
Last Op was a Read Op
YES
NO
QH031
Set EOF Block Bit for Selected Drive
QH031
Block Bit was Already On
NO
YES
QH031
Setup Selected Drive Control Byte Set EOF Bit
QH031
Error Test Op
YES
NO
QH031
To Error Test Ops
QH031
Send Service Out
QH031
Status In and Operational In Down
NO
YES
QH031
Reset Address Out
QH001
Set Suppress Out
SW
Chart 121
QH111
Store Unit Status in Last Status from Tape Control Unit Byte
QH111
Send Service Out
QH111
Channel Status is 00
NO
YES
Setup Stop Code
QH111
To Tape Stop
QE651
HA
Chart 155
QH111
Status In and Operational In Down
NO
YES
QH111
Reset Poll Control
I/O Error Byte Bit 2
I-Cycles
BRANCH ON TAPE ERROR
Chart 121
SR
QH001
QG041, QH111
Set A-Star Value into B-Star
QH111
Setup Last Status from Tape Control Unit Byte Address and Readout
QH111
Is Status 00
YES
NO
QH111
Readout Last Tape Unit Address Byte and Setup Unit Address
QH001
SS
Chart 121
Bit 6 of Status Byte
Unit Check Exists
YES
NO
QH111
Restore A-Star from B-Star, Set a Status Bit to Indicate use A-Star
QH111
Restore A-Star from B-Star
MODE SET AND CONTROL COMMANDS
Chart 121
SC
QH061
Reset Select Out, Set Unit Address in CPU Storage
Chart 121
SD
Test Bit 1 of the GT Bus
QH051
Service In Up
NO
YES
Third Sense Byte Contain Track in Error Indicators
Do we have the Third Sense Byte
YES
NO
QH051
Store Third Sense Byte in MPX Storage. Send Command Out.
GH051
Send Service Out
QH051
Status in Up
NO
YES
QH051
Reset Select Out
Chart 122
SJ
QH061
Send Service Out
QH061
Status in and Operational in Down
NO
YES
QH061
Mode Set Command
NO
YES
QH061
Setup Sense Command (04).
QH061
Readout Next Command from MPX Storage
QH001
SL
Chart 121
Mode Set Complete, Start Action Command
QH061
Unit Check from a Read Operation
NO
YES
QH061
Initial Program Load
NO
YES
To Tape Stop for Either 7 or 9 Track
QH061
7 or 9 Track
7
9
QH061
Setup Stop Code
QH061
To Tape Stop
QE651
HA
Chart 155
QH061
Readout I/O Error Byte and Reset Bits 0, 1, and 2
QH061
Readout Unit Address from MPX Storage
SL
Chart 121
QH061
Erase Bit was On
YES
NO
I/O Error Byte Bit 1
QH061
Forward Space Record this Time was on
YES
NO
QH061
Set Forward Space Record Last Time (Bit 0 of I/O Error Byte) on
QH061
Initial Program Load
YES
QH061
Set Op Register to 00 and the I-Star to Equal 1400 Address 0001
QH061
Reset Poll Control
QH061
Channel Status is 00
YES
NO
QH061
Reset EOF Block Bit
QH061
Setup Stop Code
QH061
To Tape Stop
QE651
HA
Chart 155
QG031
Readout Program Mode Switch Byte
QG031
Allow I/O Traps
YES
NO
Reset Poll Control, FA Register and Selector Channel Request Latch
Chart 115
ST
QG031
Use A-Star or I-Star for Next Address
I-STAR
A-STAR
QF661
Interrupt Exist
YES
NO
QE001
To Interrupt Decode
QE601
BA
Chart 155
To I-Cycles
QE001
AA
Chart 102
QF661
Invalid A-Address
NO
YES
To Stop Entries
QE651
HA
Chart 155
Test Bit 1 of 1400 Control Byte
Advance Program Feature Installed
NO
YES
QF661
Set B-Star to Zero
Set Status to Indicate Invalid B-Star
QF661
Set B-Star from I-Star
QF661
Set I-Star from A-Star

Operation: M/L%F0 BBB R/W
Full Seek (Not Alternate Track)



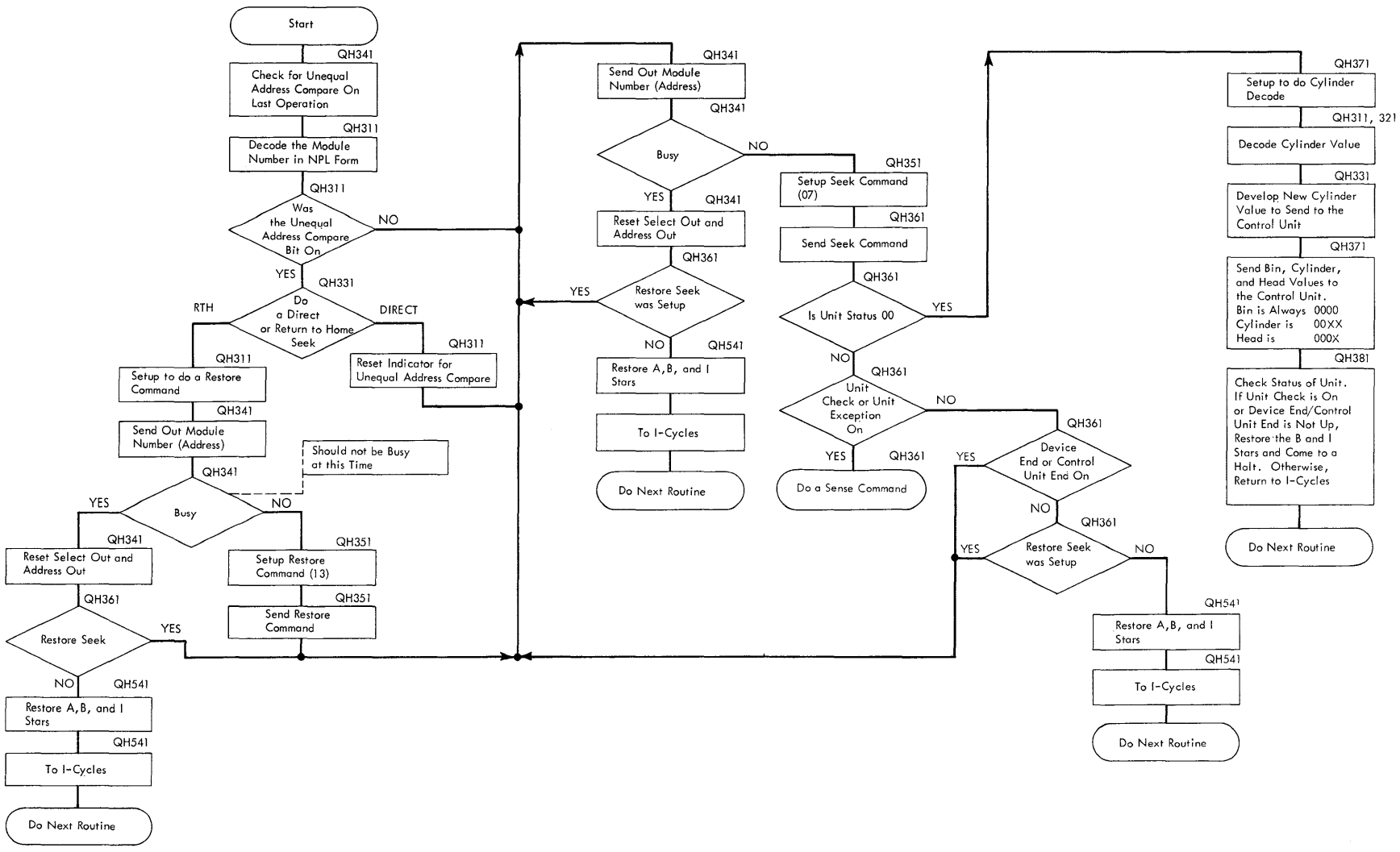
Seek Objectives:

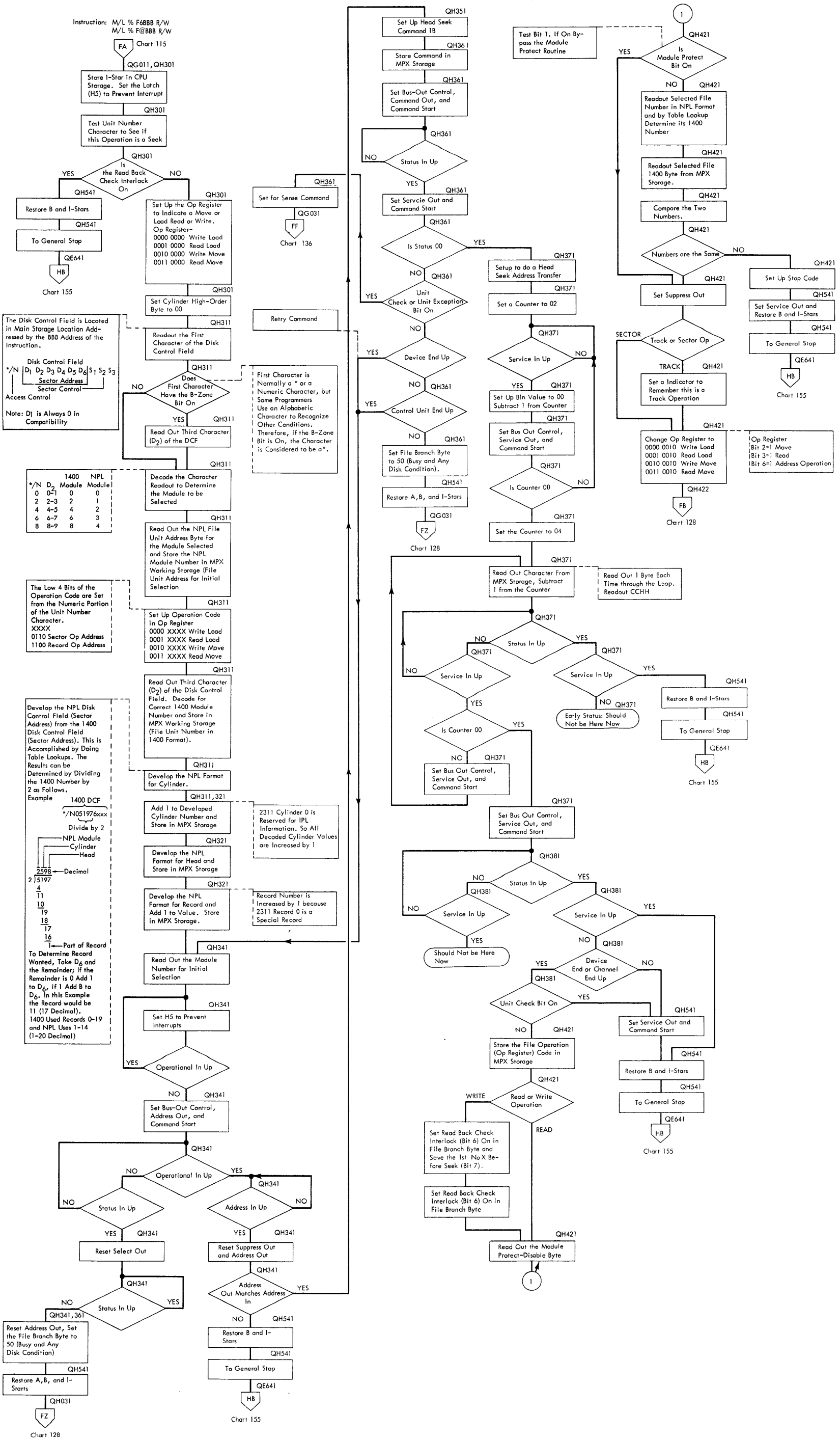
Direct Seek; Decode the Disk Control Field for Module and Cylinder Values. Select the Module, Issue Seek Command (07), and Develop the Return to Home Seek Value to Send to the Control Unit. Send the Return to Home Value to the Control Unit and Check Unit Status.

Return to Home; Decode the Disk Control Field for Module and Cylinder Values. Select the Module, Issue Seek Command (07), and Develop the Return to Home Seek Value to Send to the Control Unit. Send the Return to Home Value to the Control Unit and Check Unit Status.

Return to Home After a Unequal Address Compare; Decode the Disk Control Field for Module and Cylinder Values. Issue a Restore Command (13), when Device End is Found Issue a Seek Command, and Develop the Return to Home Seek Value to Send to the Control Unit. Send Return to Home Value to the Control Unit and Check Unit Status.

Note: The Cylinder Value is Increased by One Because Cylinder 0 is Reserved for IPL on 2311's. The format to Send Cylinder Value to the Control Unit is: Bin Bin Cylinder Cylinder Head Head
00 00 00 XX 00 0X
The Cylinder Value is Developed, the Head Value is whatever is in Head Location in MPX Storage. A Head Seek is Given on all Read or Write Operation so the Head Selected at this Time is not Important.





CLF 127 1400 File - R/W With Addresses

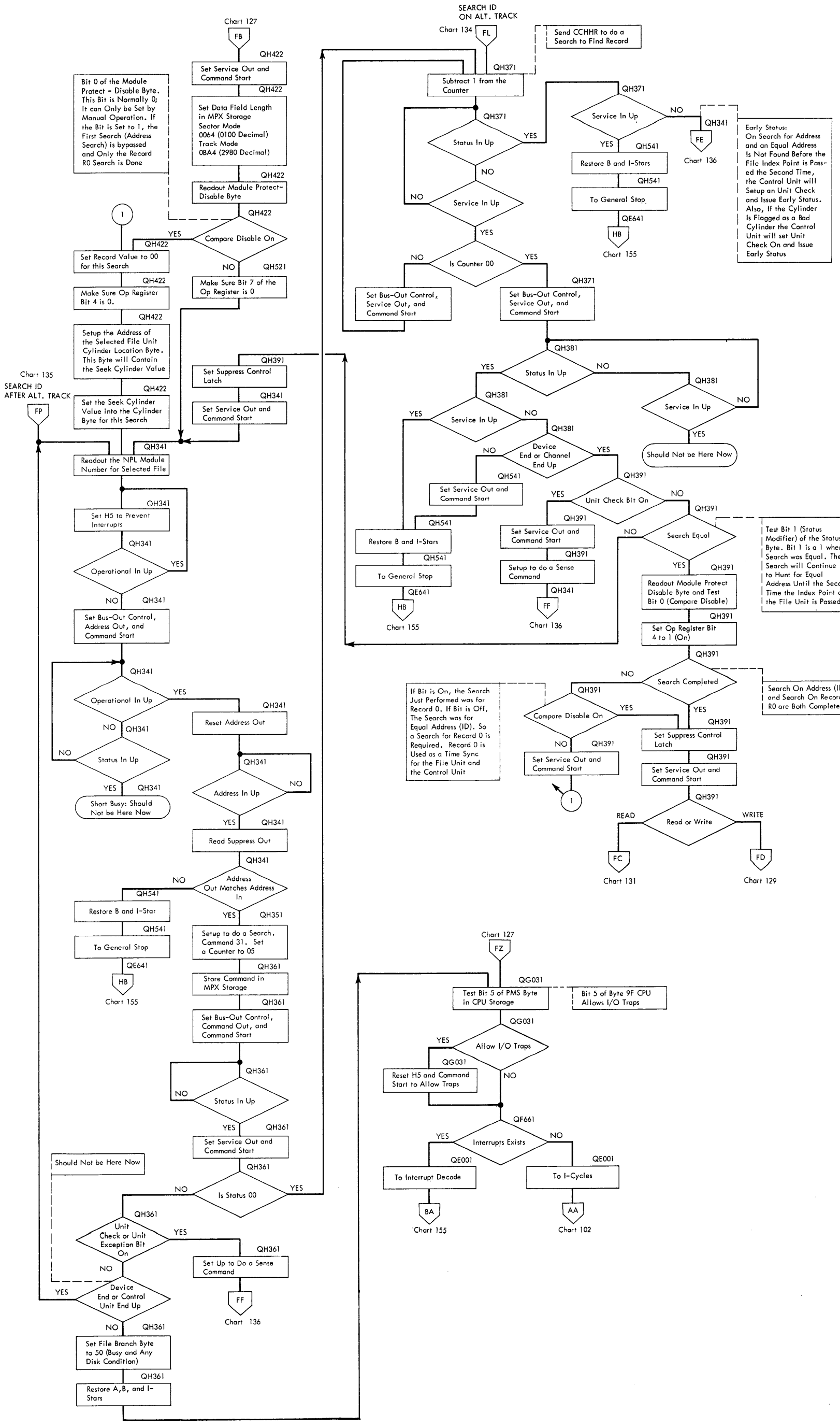
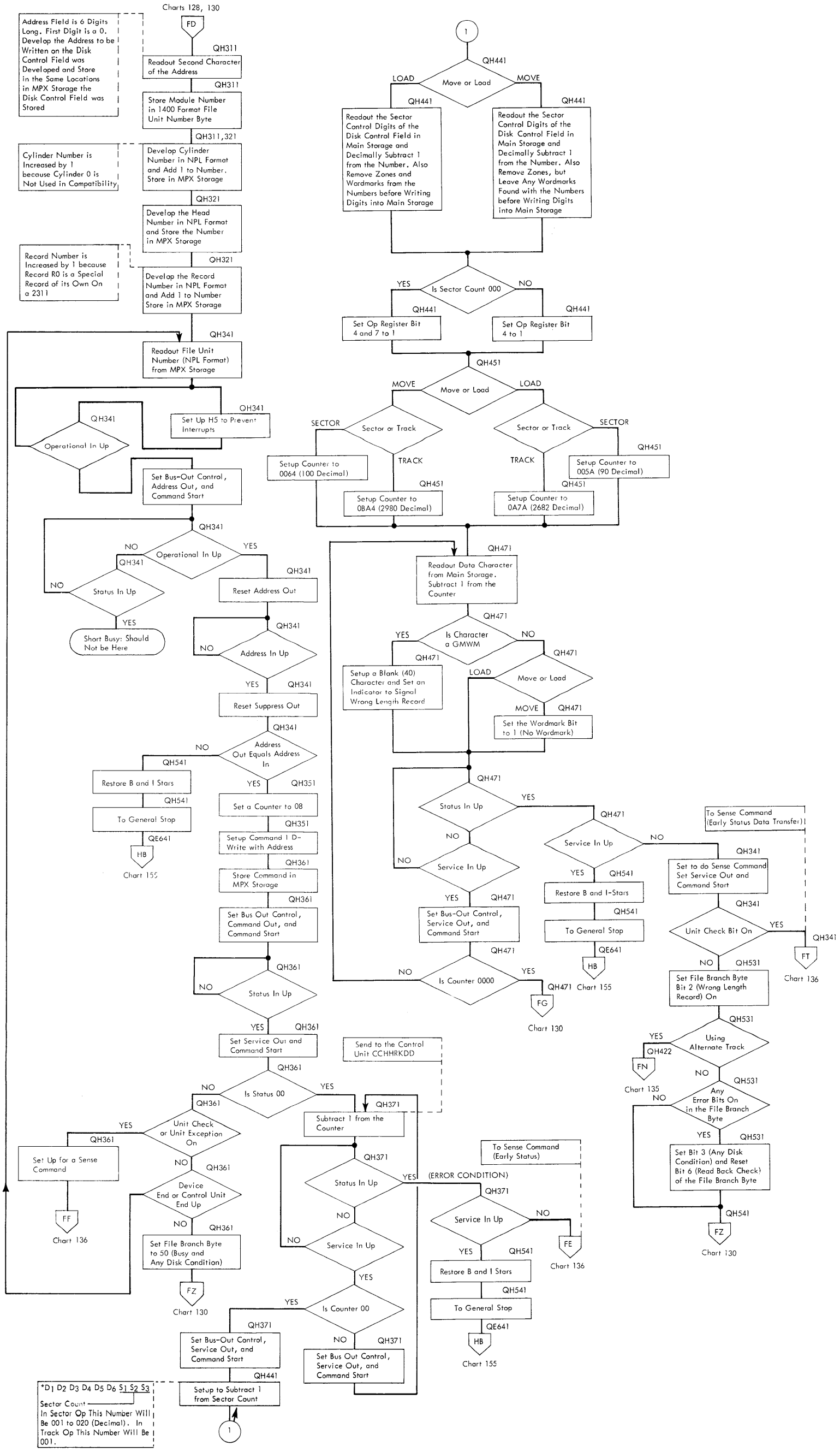


Chart 127
FB
QH422
Set Service Out and Command Start
QH422
Set Data Field Length in MPX Storage Sector Mode 0064 (0100 Decimal) Track Mode 0BA4 (2980 Decimal)
QH422
Readout Module Protect-Disable Byte
QH422
Compare Disable On
YES
NO
QH521
Make Sure Bit 7 of the Op Register is 0
Bit 0 of the Module Protect - Disable Byte. This Bit is Normally 0; It can Only be Set by Manual Operation. If the Bit is Set to 1, the First Search (Address Search) is bypassed and Only the Record R0 Search is Done
1
QH422
Set Record Value to 00 for this Search
QH422
Make Sure Op Register Bit 4 is 0.
QH422
Setup the Address of the Selected File Unit Cylinder Location Byte. This Byte will Contain the Seek Cylinder Value
QH422
Set the Seek Cylinder Value into the Cylinder Byte for this Search
Chart 135
SEARCH ID AFTER ALT. TRACK
FP
QH341
Readout the NPL Module Number for Selected File
QH341
Set H5 to Prevent Interrupts
QH341
Operational In Up
YES
NO
QH341
Set Bus-Out Control, Address Out, and Command Start
QH341
Operational In Up
YES
NO
QH341
Status In Up
NO
YES
QH341
Short Busy: Should Not be Here Now
QH341
Reset Address Out
QH341
Address In Up
NO
YES
QH341
Read Suppress Out
QH341
Address Out Matches Address In
NO
YES
QH541
Restore B and I-Star
QH541
To General Stop
QE641
HB
Chart 155
QH351
Setup to do a Search. Command 31. Set a Counter to 05
QH361
Store Command in MPX Storage
QH361
Set Bus-Out Control, Command Out, and Command Start
QH361
Status In Up
NO
YES
QH361
Set Service Out and Command Start
QH361
Is Status 00
NO
YES
Should Not be Here Now
QH361
Unit Check or Unit Exception Bit On
YES
NO
QH361
Set Up to Do a Sense Command
FF
Chart 136
Device End or Control Unit End Up
YES
NO
QH361
Set File Branch Byte to 50 (Busy and Any Disk Condition)
QH361
Restore A,B, and I-Stars
QH391
Set Suppress Control Latch
QH341
Set Service Out and Command Start
SEARCH ID ON ALT. TRACK
Chart 134
FL
Send CCHHR to do a Search to Find Record
QH371
Subtract 1 from the Counter
QH371
Status In Up
YES
NO
QH371
Service In Up
NO
YES
QH341
FE
Chart 136
QH541
Restore B and I-Stars
QH541
To General Stop
QE641
HB
Chart 155
Early Status: On Search for Address and an Equal Address Is Not Found Before the File Index Point is Passed the Second Time, the Control Unit will Setup an Unit Check and Issue Early Status. Also, If the Cylinder Is Flagged as a Bad Cylinder the Control Unit will set Unit Check On and Issue Early Status
NO
Service In Up
YES
NO
Is Counter 00
YES
NO
Set Bus-Out Control, Service Out, and Command Start
QH371
Set Bus-Out Control, Service Out, and Command Start
QH381
Status In Up
YES
NO
QH381
Service In Up
YES
NO
QH381
Service In Up
NO
YES
Should Not be Here Now
QH381
Device End or Channel End Up
NO
YES
QH541
Set Service Out and Command Start
QH391
Unit Check Bit On
YES
NO
QH391
Set Service Out and Command Start
QH391
Setup to do a Sense Command
QH341
FF
Chart 136
QH391
Search Equal
NO
YES
Test Bit 1 (Status Modifier) of the Status Byte. Bit 1 is a 1 when Search was Equal. The Search will Continue to Hunt for Equal Address Until the Second Time the Index Point of the File Unit is Passed.
QH391
Readout Module Protect Disable Byte and Test Bit 0 (Compare Disable)
QH391
Set Op Register Bit 4 to 1 (On)
QH391
Search Completed
NO
YES
Search On Address (ID) and Search On Record R0 are Both Completed.
If Bit is On, the Search Just Performed was for Record 0. If Bit is Off, The Search was for Equal Address (ID). So a Search for Record 0 is Required. Record 0 is Used as a Time Sync for the File Unit and the Control Unit
QH391
Compare Disable On
YES
NO
QH391
Set Service Out and Command Start
1
QH391
Set Suppress Control Latch
QH391
Set Service Out and Command Start
QH391
Read or Write
READ
WRITE
FC
Chart 131
FD
Chart 129
Chart 127
FZ
QG031
Test Bit 5 of PMS Byte in CPU Storage
Bit 5 of Byte 9F CPU Allows I/O Traps
QG031
Allow I/O Traps
YES
NO
QG031
Reset H5 and Command Start to Allow Traps
QF661
Interrupts Exists
YES
NO
QE001
To Interrupt Decode
BA
Chart 155
QE001
To I-Cycles
AA
Chart 102



CLF 129 1400 File - Write With Addresses Data Loop

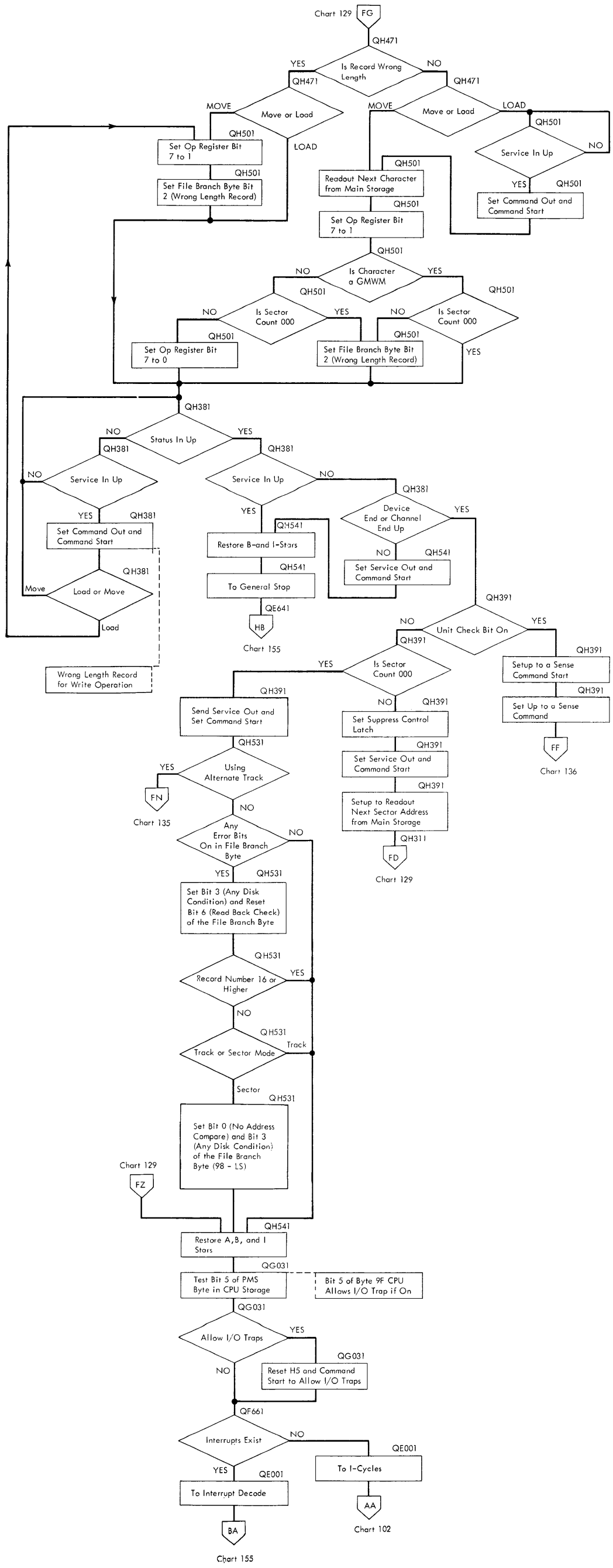
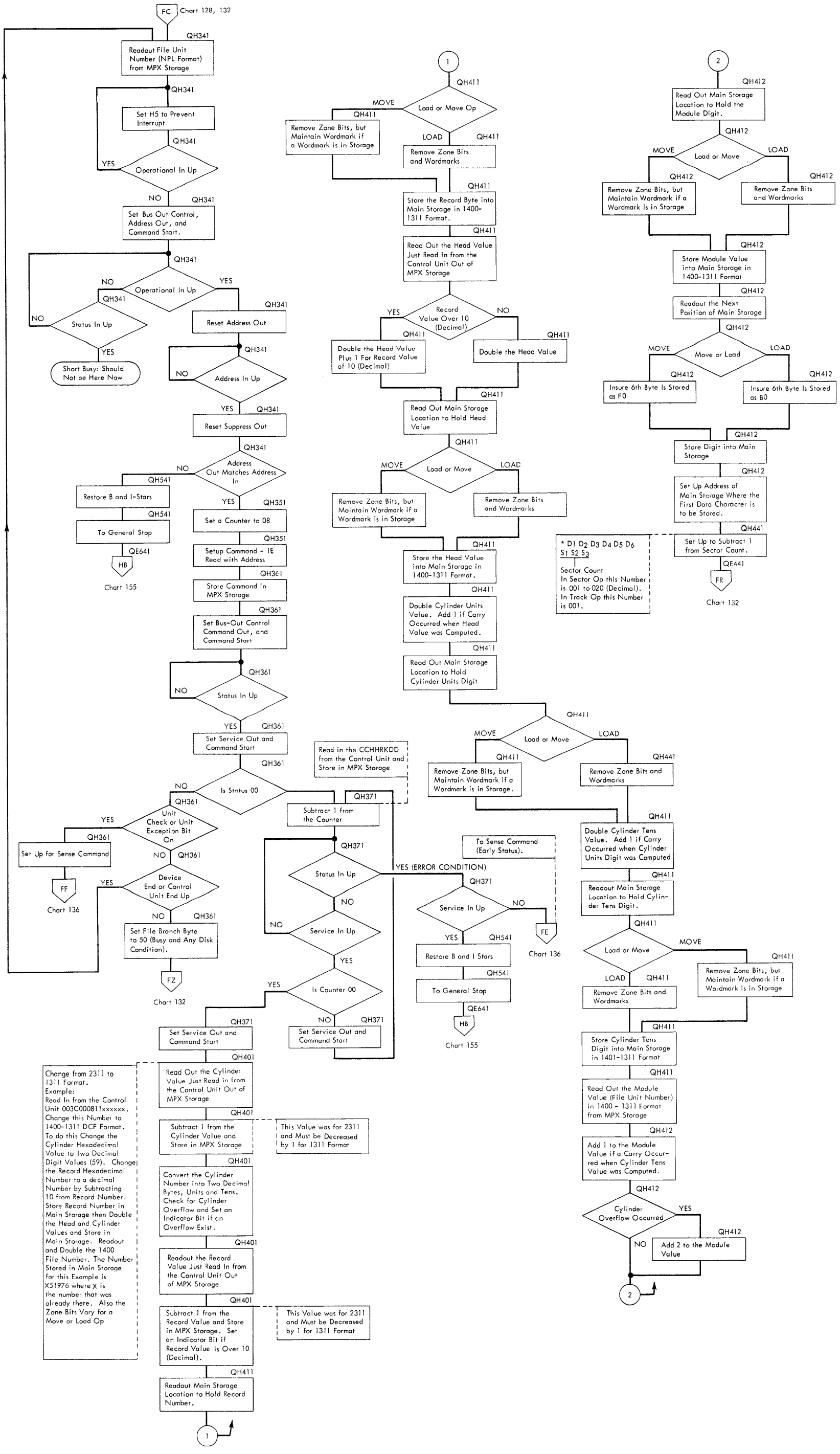
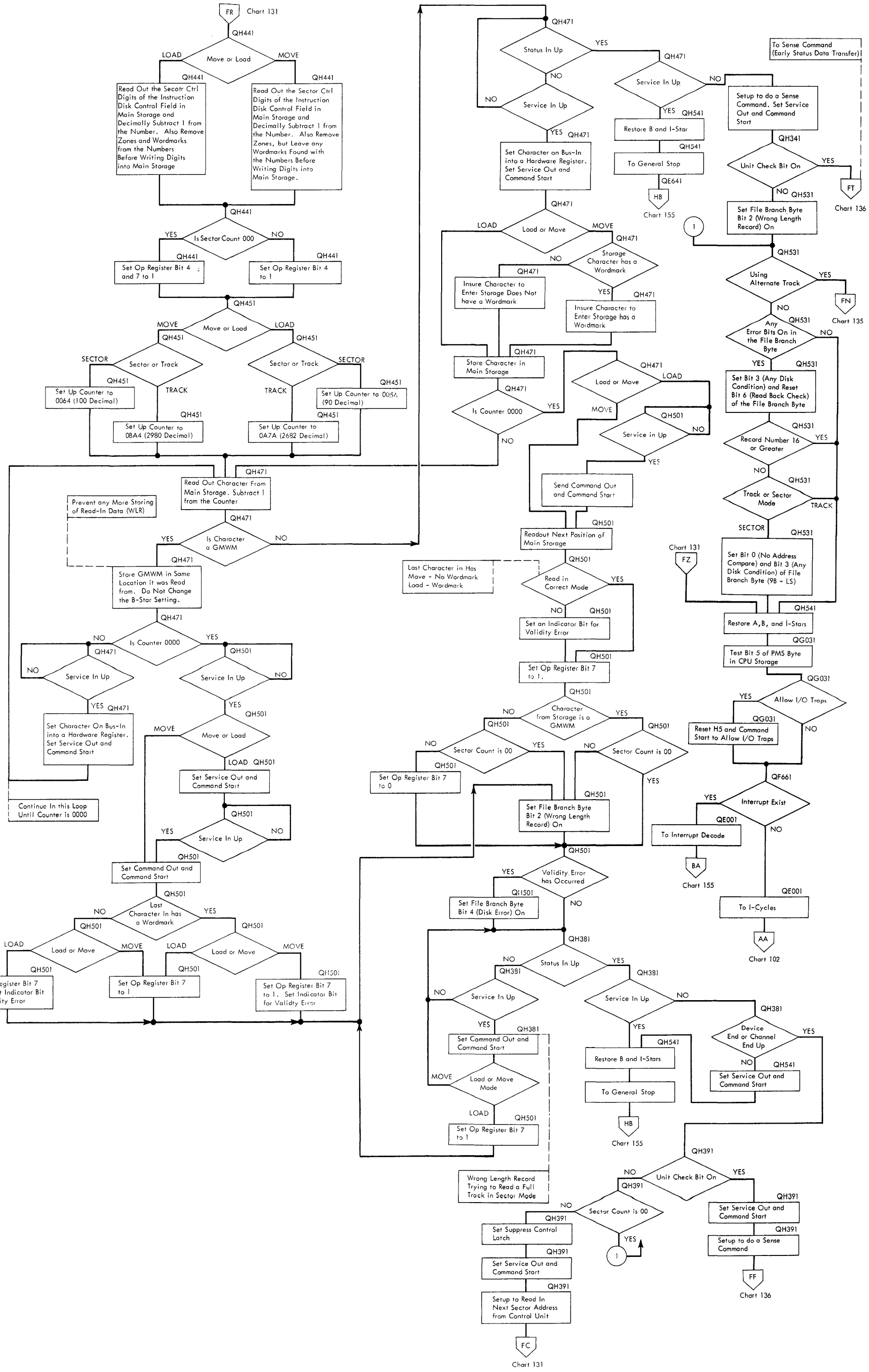
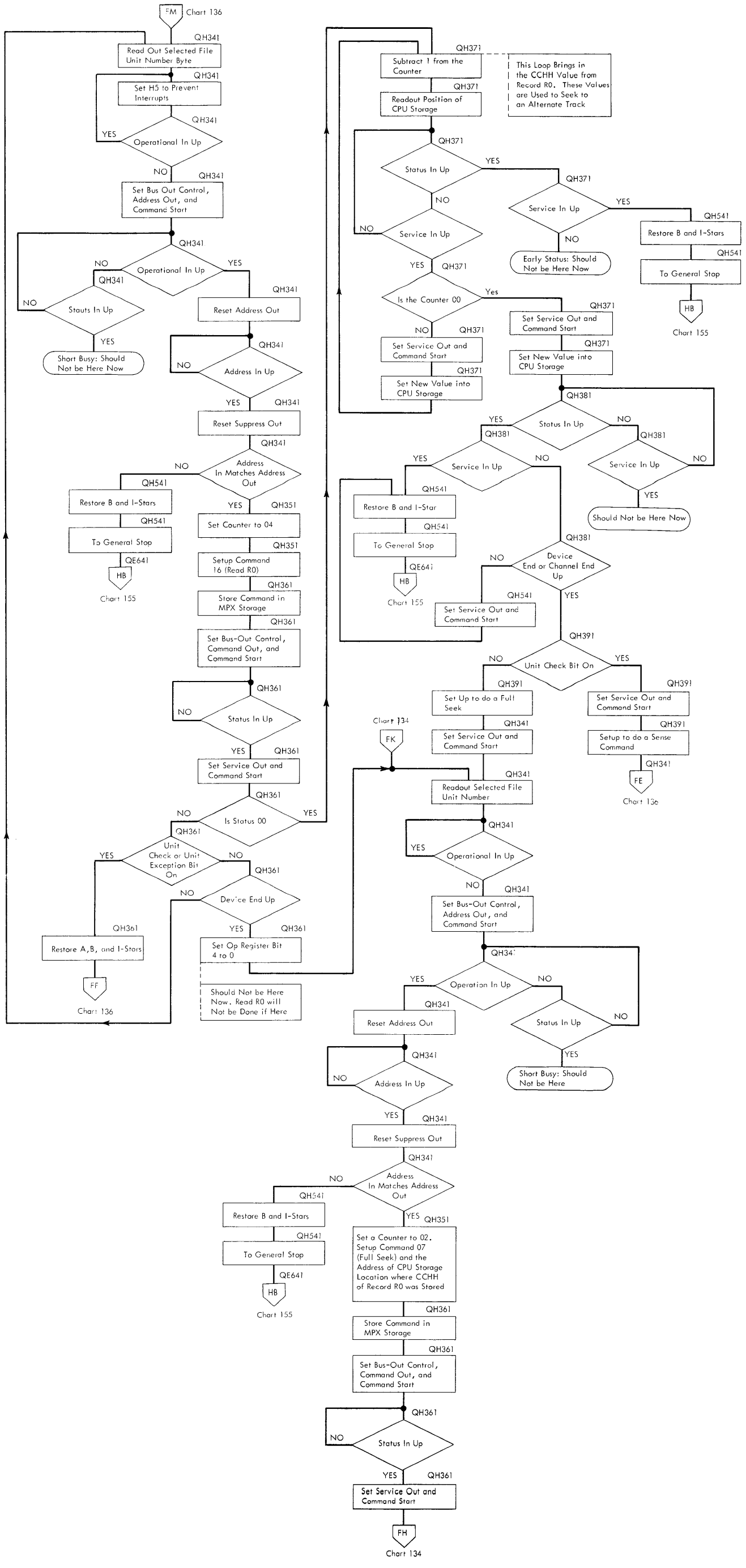


Chart 129 FG
QH471
Is Record Wrong Length
YES
NO
QH471
QH471
MOVE
Move or Load
LOAD
MOVE
Move or Load
LOAD
QH501
Service In Up
NO
YES
QH501
Set Command Out and Command Start
QH501
Set Op Register Bit 7 to 1
LOAD
QH501
Set File Branch Byte Bit 2 (Wrong Length Record)
QH501
Readout Next Character from Main Storage
QH501
Set Op Register Bit 7 to 1
QH501
Is Character a GMWM
NO
YES
QH501
Is Sector Count 000
NO
YES
QH501
Set Op Register Bit 7 to 0
Is Sector Count 000
NO
YES
QH501
Set File Branch Byte Bit 2 (Wrong Length Record)
YES
QH381
Status In Up
NO
YES
QH381
QH381
Service In Up
NO
Service In Up
NO
YES
QH381
Set Command Out and Command Start
YES
QH381
Load or Move
Move
Load
Wrong Length Record for Write Operation
QH541
Restore B-and I-Stars
QH541
To General Stop
QE641
HB
Chart 155
QH381
Device End or Channel End Up
YES
NO
QH541
Set Service Out and Command Start
QH391
Unit Check Bit On
NO
YES
QH391
Is Sector Count 000
YES
NO
QH391
Setup to a Sense Command Start
QH391
Set Up to a Sense Command
FF
Chart 136
QH391
Send Service Out and Set Command Start
QH391
Set Suppress Control Latch
QH391
Set Service Out and Command Start
QH391
Setup to Readout Next Sector Address from Main Storage
QH311
FD
Chart 129
QH531
Using Alternate Track
YES
FN
Chart 135
NO
Any Error Bits On in File Branch Byte
NO
YES
QH531
Set Bit 3 (Any Disk Condition) and Reset Bit 6 (Read Back Check) of the File Branch Byte
QH531
Record Number 16 or Higher
YES
NO
QH531
Track or Sector Mode
Track
Sector
QH531
Set Bit 0 (No Address Compare) and Bit 3 (Any Disk Condition) of the File Branch Byte (98 - LS)
Chart 129
FZ
QH541
Restore A,B, and I Stars
QG031
Test Bit 5 of PMS Byte in CPU Storage
Bit 5 of Byte 9F CPU Allows I/O Trap if On
QG031
Allow I/O Traps
YES
NO
QG031
Reset H5 and Command Start to Allow I/O Traps
QF661
Interrupts Exist
NO
YES
QE001
To Interrupt Decode
BA
Chart 155
QE001
To I-Cycles
AA
Chart 102


FC
Chart 128, 132
QH341
Readout File Unit Number (NPL Format) from MPX Storage
QH341
Set H5 to Prevent Interrupt
QH341
YES
Operational In Up
NO
QH341
Set Bus Out Control, Address Out, and Command Start.
QH341
NO
Operational In Up
YES
QH341
NO
Status In Up
YES
Short Busy: Should Not be Here Now
QH341
Reset Address Out
QH341
NO
Address In Up
YES
QH341
Reset Suppress Out
QH341
NO
Address Out Matches Address In
QH541
Restore B and I-Stars
QH541
To General Stop
QE641
HB
Chart 155
YES
QH351
Set a Counter to 08
QH351
Setup Command - 1E Read with Address
QH361
Store Command in MPX Storage
QH361
Set Bus-Out Control Command Out, and Command Start
QH361
NO
Status In Up
YES
QH361
Set Service Out and Command Start
QH361
NO
Is Status 00
QH361
YES
Unit Check or Unit Exception Bit On
QH361
Set Up for Sense Command
FF
Chart 136
NO
QH361
YES
Device End or Control Unit End Up
NO
QH361
Set File Branch Byte to 50 (Busy and Any Disk Condition).
FZ
Chart 132
Change from 2311 to 1311 Format.
Example:
Read In from the Control Unit 003C000811xxxxxx.
Change this Number to 1400-1311 DCF Format.
To do this Change the Cylinder Hexadecimal Value to Two Decimal Digit Values (59). Change the Record Hexadecimal Number to a decimal Number by Subtracting 10 from Record Number. Store Record Number in Main Storage then Double the Head and Cylinder Values and Store in Main Storage. Readout and Double the 1400 File Number. The Number Stored in Main Storage for this Example is X51976 where X is the number that was already there. Also the Zone Bits Vary for a Move or Load Op
QH401
Read Out the Cylinder Value Just Read in from the Control Unit Out of MPX Storage
QH401
Subtract 1 from the Cylinder Value and Store in MPX Storage
This Value was for 2311 and Must be Decreased by 1 for 1311 Format
QH401
Convert the Cylinder Number into Two Decimal Bytes, Units and Tens. Check for Cylinder Overflow and Set an Indicator Bit if an Overflow Exist.
QH401
Readout the Record Value Just Read In from the Control Unit Out of MPX Storage
QH401
Subtract 1 from the Record Value and Store in MPX Storage. Set an Indicator Bit if Record Value is Over 10 (Decimal).
This Value was for 2311 and Must be Decreased by 1 for 1311 Format
QH411
Readout Main Storage Location to Hold Record Number.
1
Read in the CCHHRKDD from the Control Unit and Store in MPX Storage
QH371
Subtract 1 from the Counter
QH371
Status In Up
YES (ERROR CONDITION)
NO
NO
Service In Up
YES
YES
Is Counter 00
NO
QH371
Set Service Out and Command Start
QH371
Set Service Out and Command Start
To Sense Command (Early Status).
QH371
Service In Up
NO
FE
Chart 136
YES
QH541
Restore B and I Stars
QH541
To General Stop
QE641
HB
Chart 155
1
QH411
Load or Move Op
MOVE
QH411
Remove Zone Bits, but Maintain Wordmark if a Wordmark is in Storage
LOAD
QH411
Remove Zone Bits and Wordmarks
QH411
Store the Record Byte into Main Storage in 1400-1311 Format.
QH411
Read Out the Head Value Just Read In from the Control Unit Out of MPX Storage
QH411
YES
Record Value Over 10 (Decimal)
NO
QH411
Double the Head Value Plus 1 For Record Value of 10 (Decimal)
QH411
Double the Head Value
QH411
Read Out Main Storage Location to Hold Head Value
QH411
MOVE
Load or Move
LOAD
Remove Zone Bits, but Maintain Wordmark if a Wordmark is in Storage
Remove Zone Bits and Wordmarks
QH411
Store the Head Value into Main Storage in 1400-1311 Format.
QH411
Double Cylinder Units Value. Add 1 if Carry Occurred when Head Value was Computed.
QH411
Read Out Main Storage Location to Hold Cylinder Units Digit
QH411
MOVE
Load or Move
LOAD
QH411
Remove Zone Bits, but Maintain Wordmark if a Wordmark is in Storage.
QH441
Remove Zone Bits and Wordmarks
QH411
Double Cylinder Tens Value. Add 1 if Carry Occurred when Cylinder Units Digit was Computed
QH411
Readout Main Storage Location to Hold Cylinder Tens Digit.
QH411
Load or Move
MOVE
QH411
Remove Zone Bits, but Maintain Wordmark if a Wordmark is in Storage
LOAD
QH411
Remove Zone Bits and Wordmarks
QH411
Store Cylinder Tens Digit into Main Storage in 1401-1311 Format
QH411
Read Out the Module Value (File Unit Number) in 1400 - 1311 Format from MPX Storage
QH412
Add 1 to the Module Value if a Carry Occurred when Cylinder Tens Value was Computed.
QH412
Cylinder Overflow Occurred
YES
QH412
Add 2 to the Module Value
NO
2
2
QH412
Read Out Main Storage Location to Hold the Module Digit.
QH412
MOVE
Load or Move
LOAD
QH412
Remove Zone Bits, but Maintain Wordmark if a Wordmark is in Storage
QH412
Remove Zone Bits and Wordmarks
QH412
Store Module Value into Main Storage in 1400-1311 Format
QH412
Readout the Next Position of Main Storage
QH412
MOVE
Move or Load
LOAD
QH412
Insure 6th Byte Is Stored as F0
QH412
Insure 6th Byte Is Stored as B0
QH412
Store Digit into Main Storage
QH412
Set Up Address of Main Storage Where the First Data Character is to be Stored.
QH441
Set Up to Subtract 1 from Sector Count.
QE441
FR
Chart 132
* D1 D2 D3 D4 D5 D6 S1 S2 S3
Sector Count
In Sector Op this Number is 001 to 020 (Decimal).
In Track Op this Number is 001.



CLF 132 1400 File - Read With Addresses Data Loop - Sheet 2



CLF 133 1400 File - Alternate Track Seek

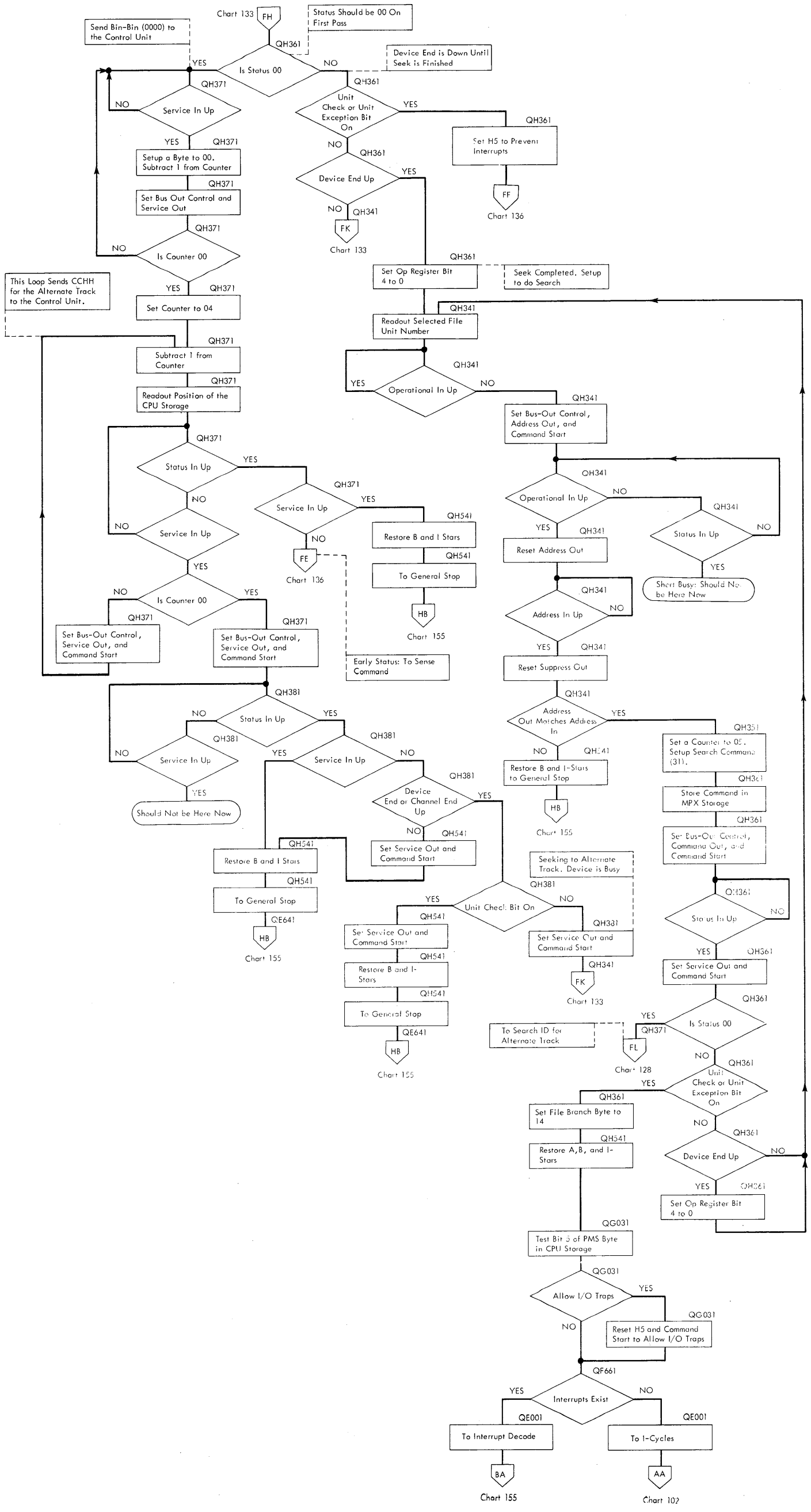
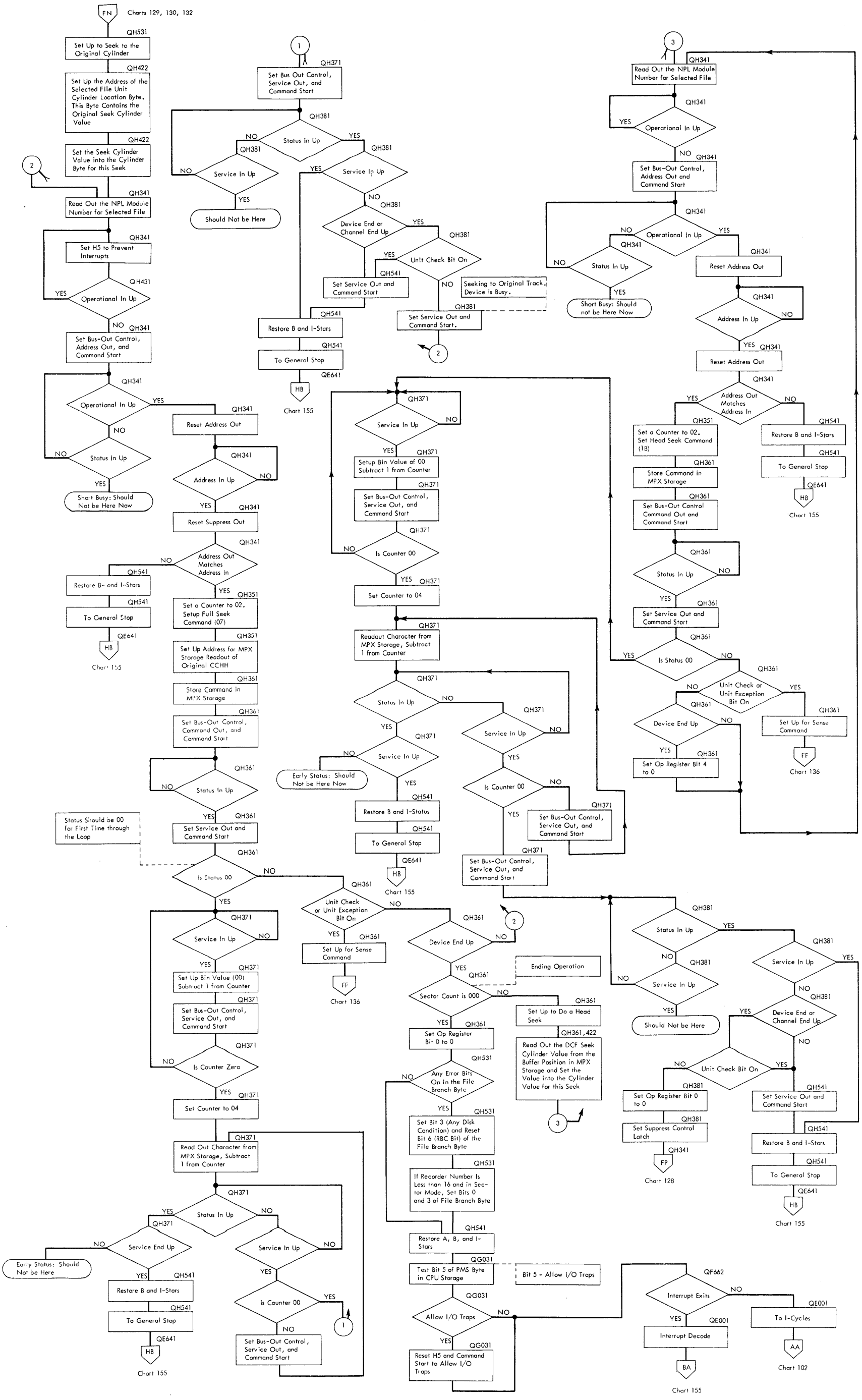
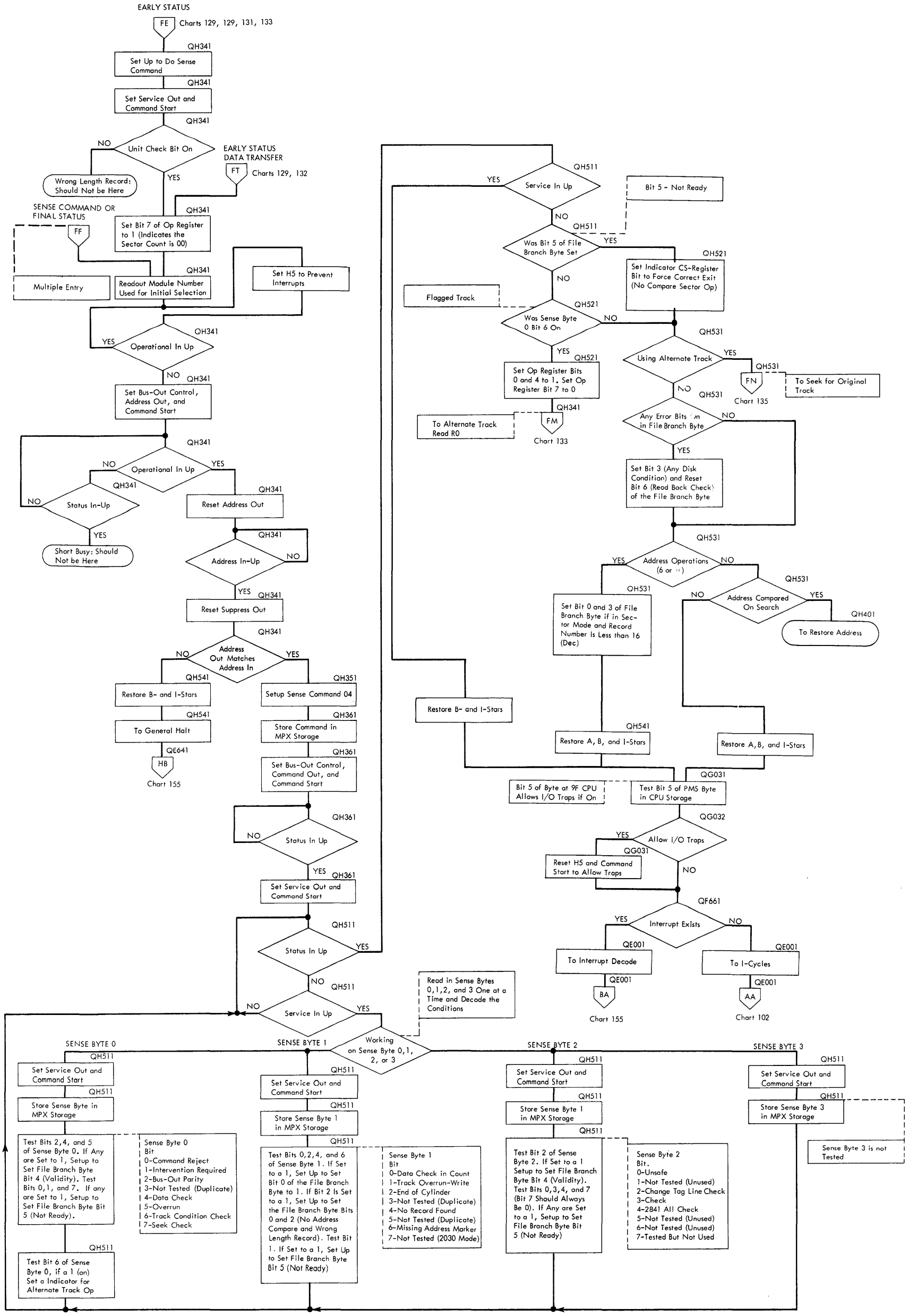
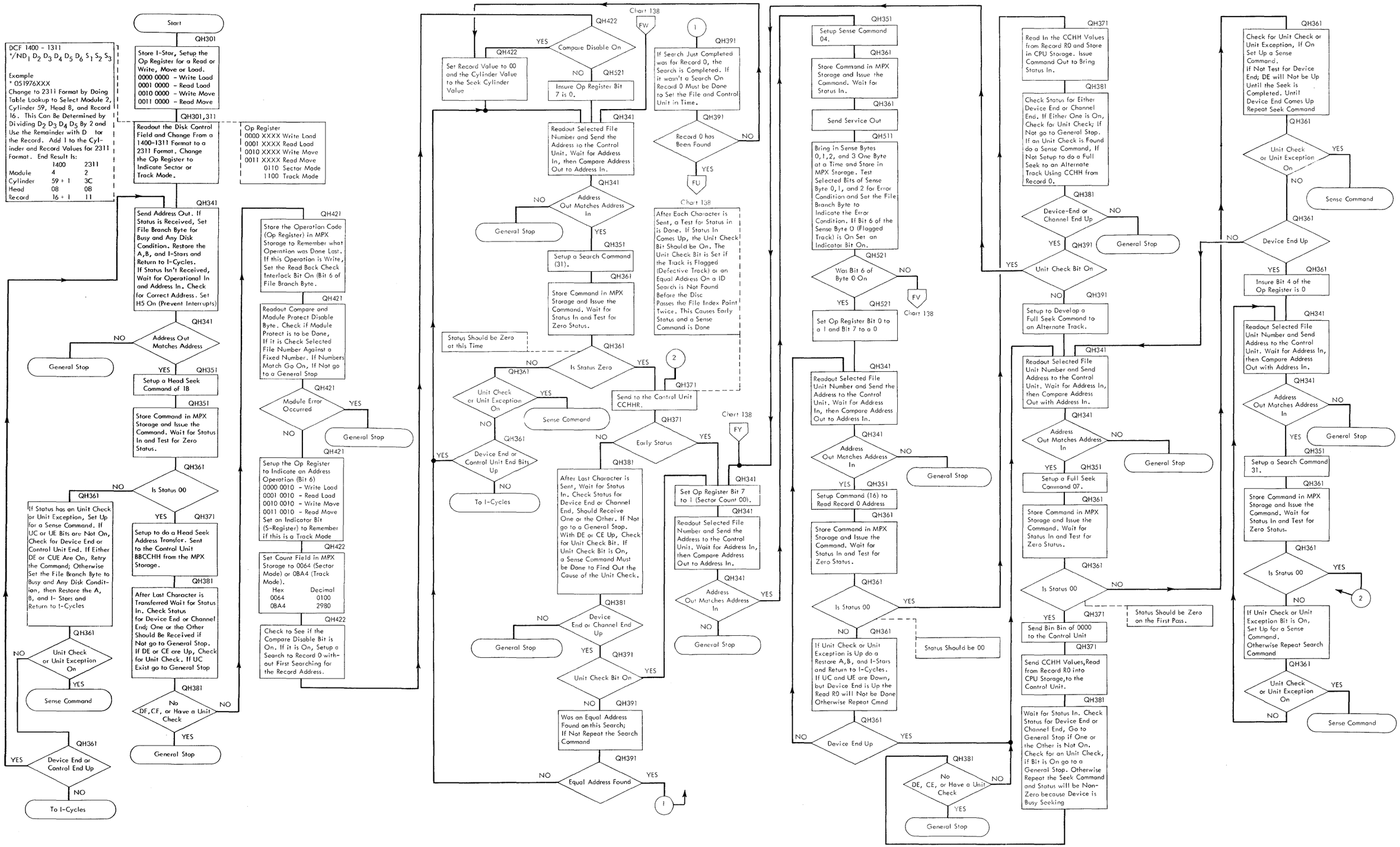
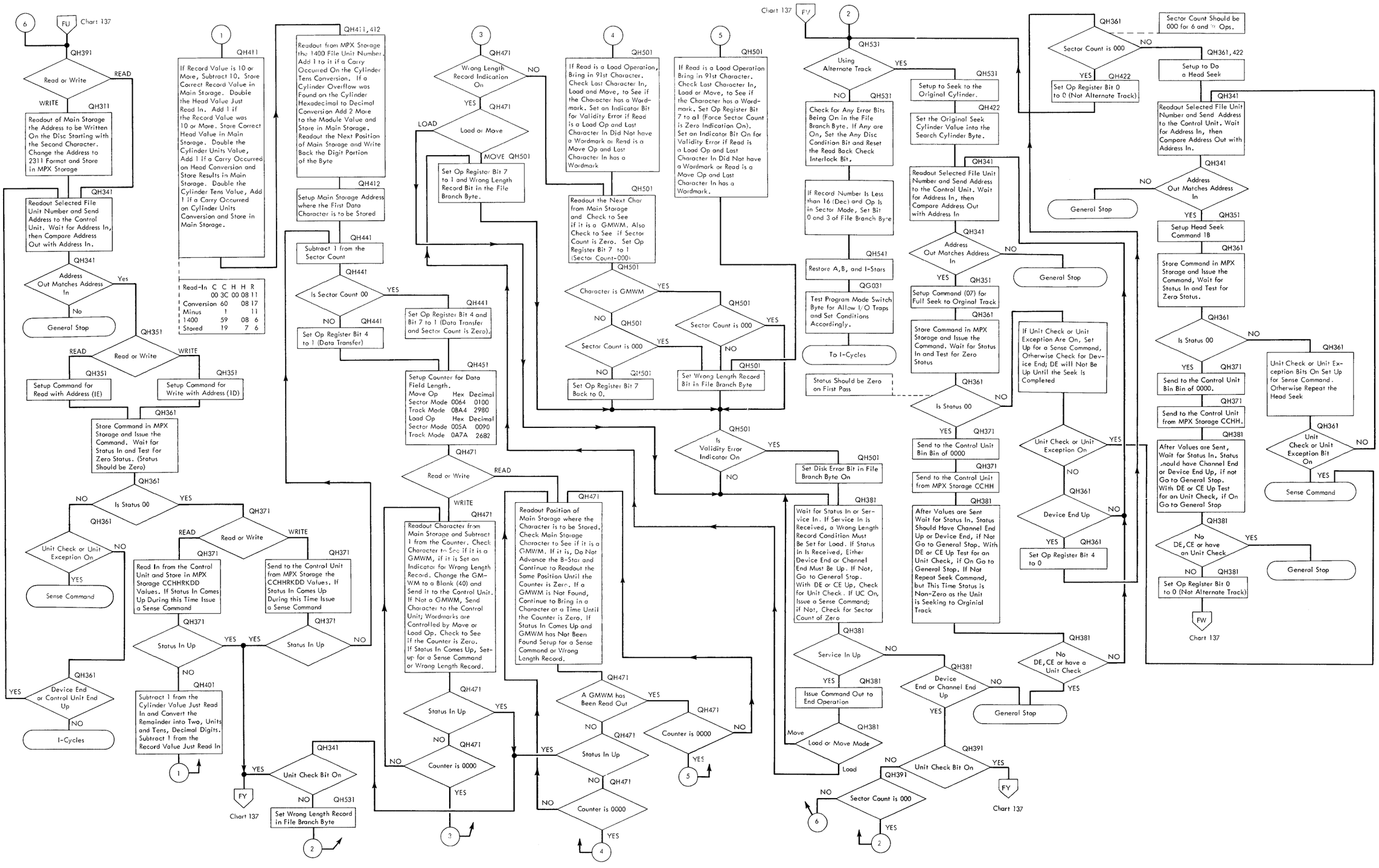


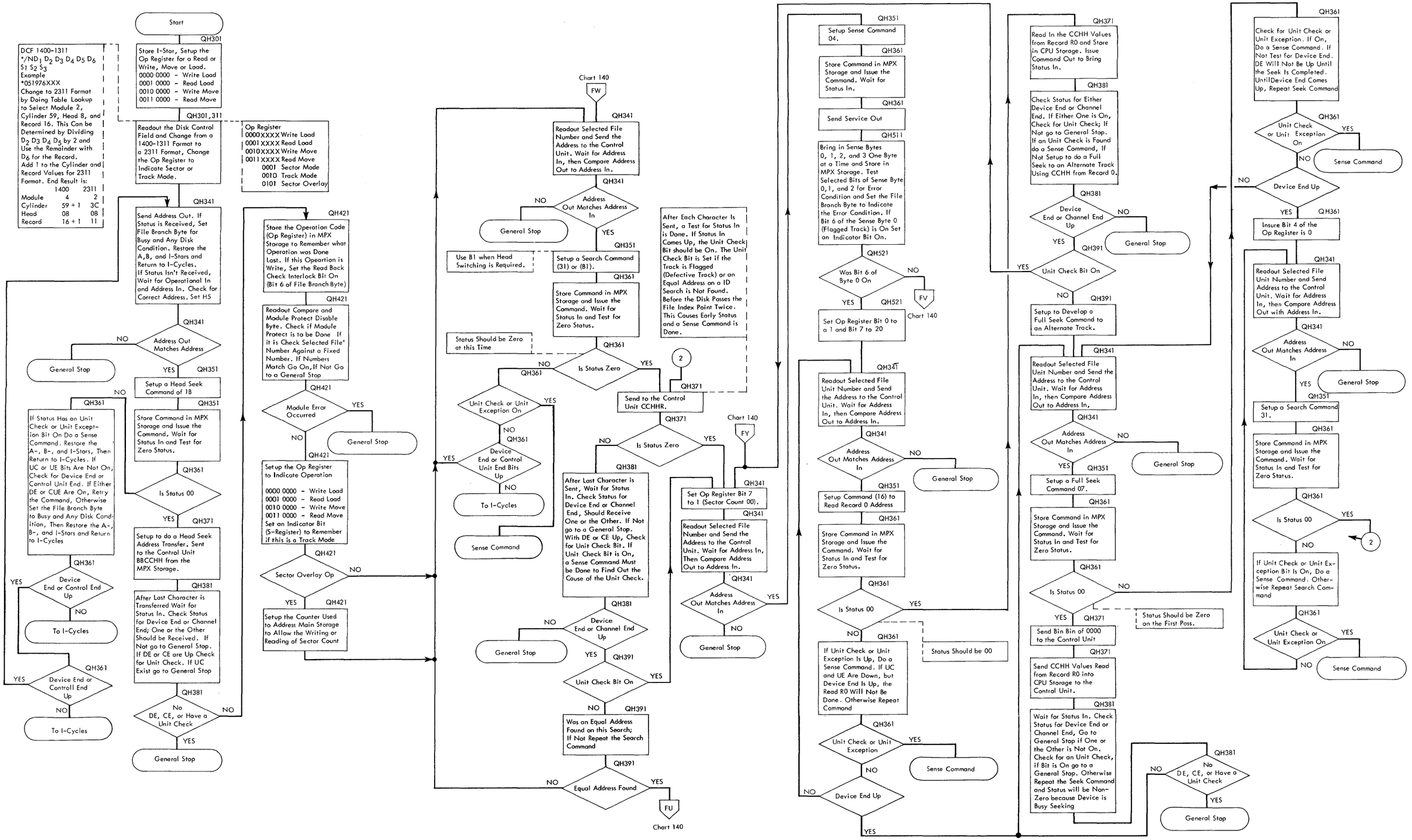
Chart 133 FH
Status Should be 00 On First Pass
Send Bin-Bin (0000) to the Control Unit
QH361
Is Status 00
YES
NO
Device End is Down Until Seek is Finished
QH371
Service In Up
NO
YES
QH371
Setup a Byte to 00. Subtract 1 from Counter
QH371
Set Bus Out Control and Service Out
QH371
Is Counter 00
NO
YES
This Loop Sends CCHH for the Alternate Track to the Control Unit.
QH371
Set Counter to 04
QH371
Subtract 1 from Counter
QH371
Readout Position of the CPU Storage
QH371
Status In Up
YES
NO
QH371
Service In Up
NO
YES
Is Counter 00
YES
NO
QH371
Set Bus-Out Control, Service Out, and Command Start
QH371
Set Bus-Out Control, Service Out, and Command Start
QH381
Status In Up
NO
YES
QH381
Service In Up
NO
YES
Should Not be Here Now
QH381
Service In Up
YES
NO
QH541
Restore B and I Stars
QH541
To General Stop
QE641
HB
Chart 155
QH381
Device End or Channel End Up
YES
NO
QH541
Set Service Out and Command Start
QH381
Unit Check Bit On
YES
NO
QH541
Set Service Out and Command Start
QH541
Restore B and I-Stars
QH541
To General Stop
QE641
HB
Chart 155
QH371
Service In Up
YES
NO
FE
Chart 136
Early Status: To Sense Command
QH541
Restore B and I Stars
QH541
To General Stop
HB
Chart 155
QH361
Unit Check or Unit Exception Bit On
YES
NO
QH361
Set H5 to Prevent Interrupts
FF
Chart 136
QH361
Device End Up
YES
NO
QH341
FK
Chart 133
QH361
Set Op Register Bit 4 to 0
Seek Completed. Setup to do Search
QH341
Readout Selected File Unit Number
QH341
Operational In Up
YES
NO
QH341
Set Bus-Out Control, Address Out, and Command Start
QH341
Operational In Up
NO
YES
QH341
Reset Address Out
QH341
Address In Up
NO
YES
QH341
Reset Suppress Out
QH341
Address Out Matches Address In
YES
NO
QH341
Restore B and I-Stars to General Stop
HB
Chart 155
Seeking to Alternate Track. Device is Busy
QH341
Set Service Out and Command Start
FK
Chart 133
To Search ID for Alternate Track
YES
QH371
FL
Chart 128
QH341
Status In Up
NO
YES
Short Busy: Should Not be Here Now
QH361
Set a Counter to 05. Setup Search Command (31).
QH361
Store Command in MPX Storage
QH361
Set Bus-Out Control, Command Out, and Command Start
QH361
Status In Up
NO
YES
QH361
Set Service Out and Command Start
QH361
Is Status 00
YES
NO
QH361
Unit Check or Unit Exception Bit On
YES
NO
QH361
Set File Branch Byte to 14
QH541
Restore A,B, and I-Stars
QG031
Test Bit 5 of PMS Byte in CPU Storage
QG031
Allow I/O Traps
YES
NO
QG031
Reset H5 and Command Start to Allow I/O Traps
QF661
Interrupts Exist
YES
NO
QE001
To Interrupt Decode
BA
Chart 155
QE001
To I-Cycles
AA
Chart 102
QH361
Device End Up
NO
YES
QH361
Set Op Register Bit 4 to 0

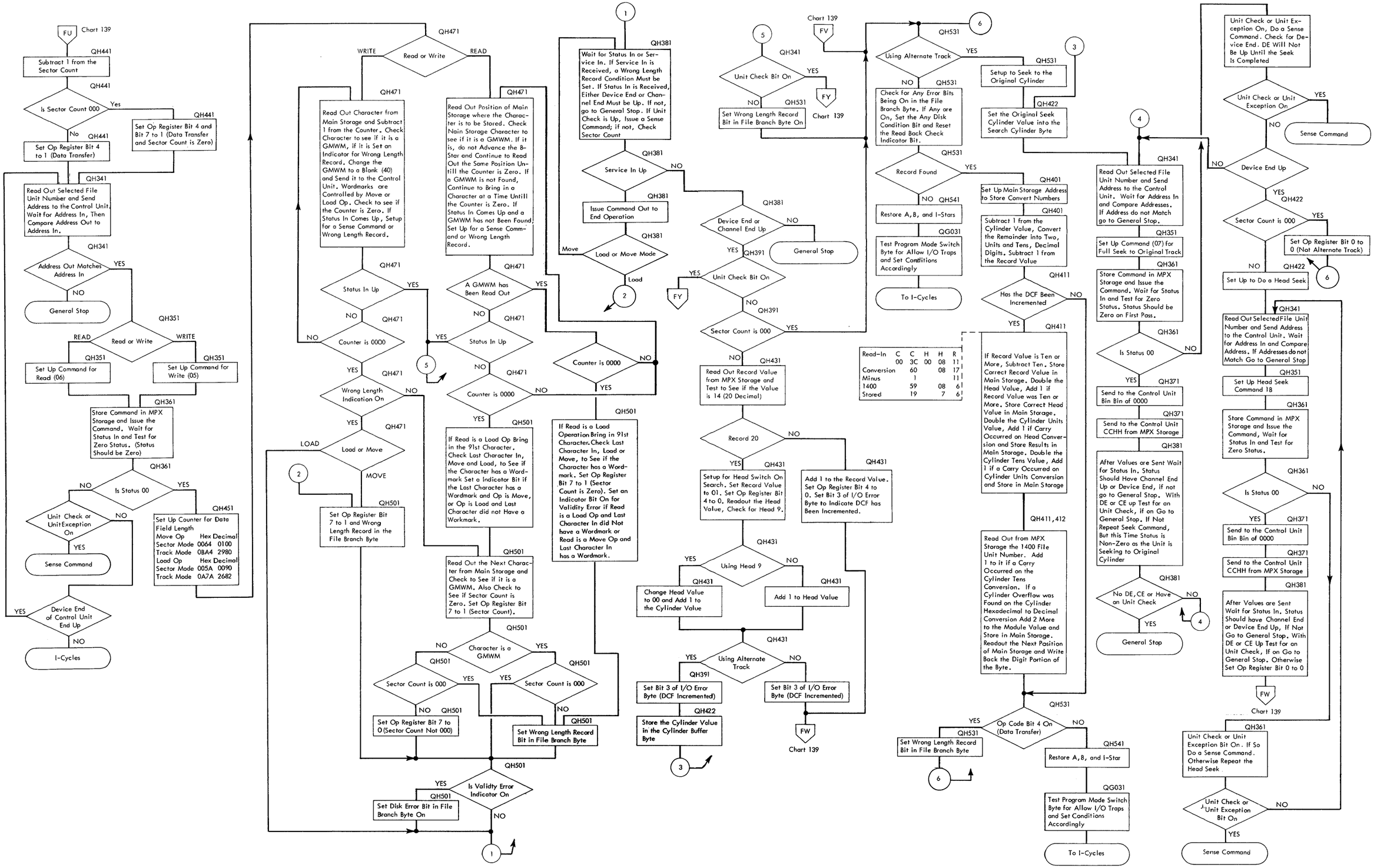

FN
Charts 129, 130, 132
QH531
Set Up to Seek to the Original Cylinder
QH422
Set Up the Address of the Selected File Unit Cylinder Location Byte. This Byte Contains the Original Seek Cylinder Value
QH422
Set the Seek Cylinder Value into the Cylinder Byte for this Seek
2
QH341
Read Out the NPL Module Number for Selected File
QH341
Set H5 to Prevent Interrupts
QH431
Operational In Up
YES
NO
QH341
Set Bus-Out Control, Address Out, and Command Start
QH341
Operational In Up
YES
NO
Status In Up
NO
YES
Short Busy: Should Not be Here Now
QH341
Reset Address Out
QH341
Address In Up
NO
YES
QH341
Reset Suppress Out
QH341
Address Out Matches Address In
NO
YES
QH541
Restore B- and I-Stars
QH541
To General Stop
QE641
HB
Chart 155
QH351
Set a Counter to 02. Setup Full Seek Command (07)
QH351
Set Up Address for MPX Storage Readout of Original CCHH
QH361
Store Command in MPX Storage
QH361
Set Bus-Out Control, Command Out, and Command Start
QH361
Status In Up
NO
YES
QH361
Set Service Out and Command Start
Status Should be 00 for First Time through the Loop
QH361
Is Status 00
NO
YES
QH371
Service In Up
NO
YES
QH371
Set Up Bin Value (00) Subtract 1 from Counter
QH371
Set Bus-Out Control, Service Out, and Command Start
QH371
Is Counter Zero
NO
YES
QH371
Set Counter to 04
QH371
Read Out Character from MPX Storage, Subtract 1 from Counter
QH371
Status In Up
YES
NO
QH371
Service End Up
NO
YES
Early Status: Should Not be Here
QH541
Restore B and I-Stars
QH541
To General Stop
QE641
HB
Chart 155
QH371
Service In Up
NO
YES
QH541
Restore B and I-Status
QH541
To General Stop
QE641
HB
Chart 155
QH371
Service In Up
NO
YES
Early Status: Should Not be Here Now
QH371
Service In Up
NO
YES
QH381
Should Not be Here
1
QH371
Set Bus Out Control, Service Out, and Command Start
QH381
Status In Up
NO
YES
QH381
Service In Up
NO
YES
QH381
Device End or Channel End Up
YES
NO
QH381
Unit Check Bit On
YES
NO
QH541
Set Service Out and Command Start
Seeking to Original Track, Device is Busy.
QH381
Set Service Out and Command Start.
2
QH541
Restore B and I-Stars
QH541
To General Stop
QE641
HB
Chart 155
QH361
Unit Check or Unit Exception Bit On
YES
NO
QH361
Set Up for Sense Command
FF
Chart 136
QH361
Device End Up
NO
YES
QH361
Sector Count is 000
NO
YES
QH361
Set Op Register Bit 0 to 0
QH531
Any Error Bits On in the File Branch Byte
NO
YES
QH531
Set Bit 3 (Any Disk Condition) and Reset Bit 6 (RBC Bit) of the File Branch Byte
QH531
If Recorder Number Is Less than 16 and in Sector Mode, Set Bits 0 and 3 of File Branch Byte
QH541
Restore A, B, and I-Stars
QG031
Test Bit 5 of PMS Byte in CPU Storage
Bit 5 - Allow I/O Traps
QG031
Allow I/O Traps
NO
YES
QG031
Reset H5 and Command Start to Allow I/O Traps
Ending Operation
QH361
Set Up to Do a Head Seek
QH361,422
Read Out the DCF Seek Cylinder Value from the Buffer Position in MPX Storage and Set the Value into the Cylinder Value for this Seek
3
QH371
Set Bus-Out Control, Service Out, and Command Start
QH371
Set Bus-Out Control, Service Out, and Command Start
2
3
QH341
Read Out the NPL Module Number for Selected File
QH341
Operational In Up
YES
NO
QH341
Set Bus-Out Control, Address Out and Command Start
QH341
Operational In Up
NO
YES
QH341
Status In Up
NO
YES
Short Busy: Should not be Here Now
QH341
Reset Address Out
QH341
Address In Up
NO
YES
QH341
Reset Address Out
QH341
Address Out Matches Address In
YES
NO
QH351
Set a Counter to 02. Set Head Seek Command (1B)
QH361
Store Command in MPX Storage
QH361
Set Bus-Out Control Command Out and Command Start
QH361
Status In Up
NO
YES
QH361
Set Service Out and Command Start
QH361
Is Status 00
YES
NO
QH361
Unit Check or Unit Exception Bit On
NO
YES
QH361
Device End Up
NO
YES
QH361
Set Op Register Bit 4 to 0
QH541
Restore B and I-Stars
QH541
To General Stop
QE641
HB
Chart 155
QH361
Set Up for Sense Command
FF
Chart 136
QH381
Status In Up
YES
NO
QH381
Service In Up
NO
YES
Should Not be Here
QH381
Service In Up
YES
NO
QH381
Device End or Channel End Up
NO
QH381
Unit Check Bit On
NO
YES
QH381
Set Op Register Bit 0 to 0
QH381
Set Suppress Control Latch
QH341
FP
Chart 128
QH541
Set Service Out and Command Start
QH541
Restore B and I-Stars
QH541
To General Stop
QE641
HB
Chart 155
QF662
Interrupt Exits
NO
YES
QE001
To I-Cycles
AA
Chart 102
QE001
Interrupt Decode
BA
Chart 155

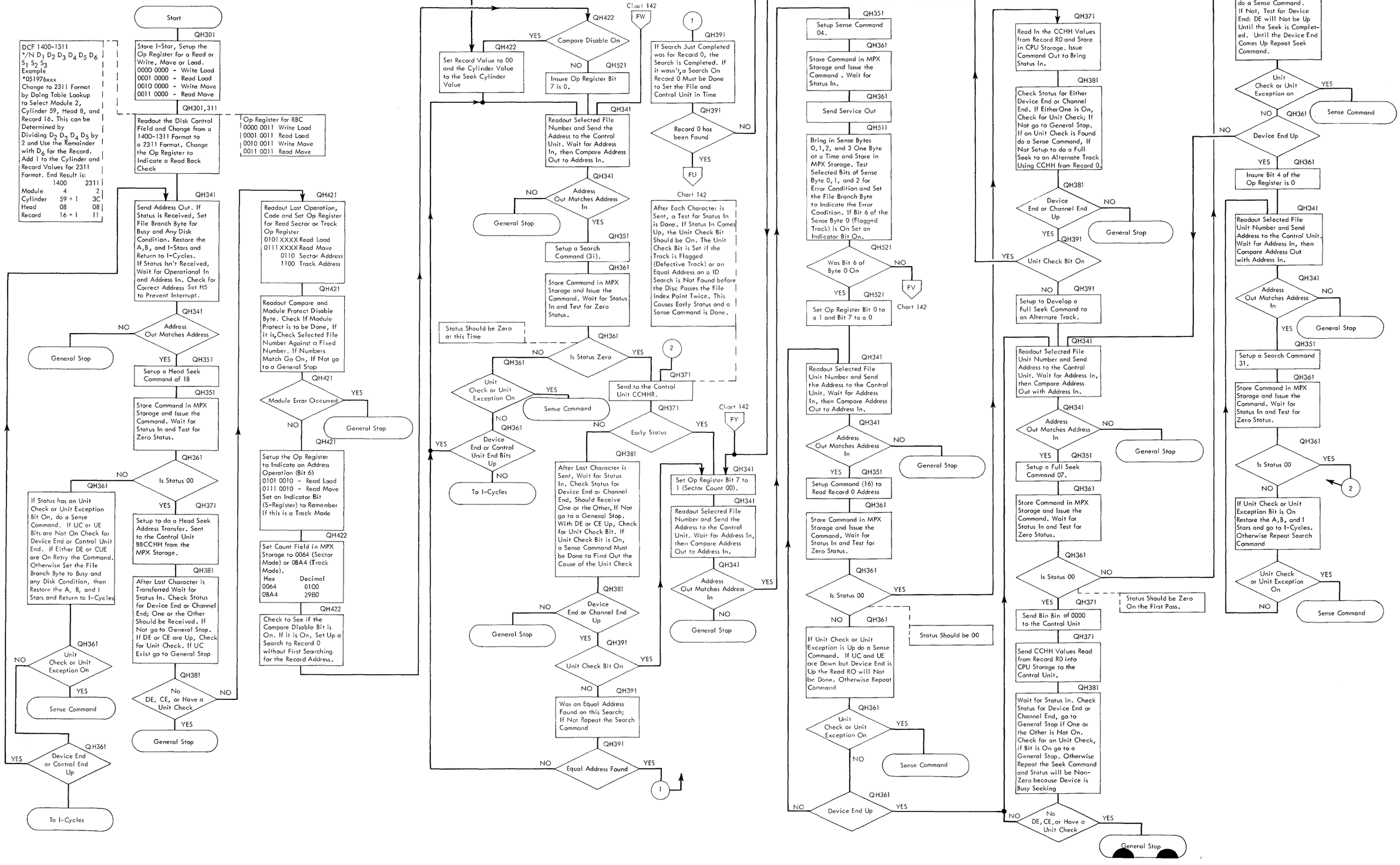

EARLY STATUS
FE
Charts 129, 129, 131, 133
QH341
Set Up to Do Sense Command
QH341
Set Service Out and Command Start
QH341
Unit Check Bit On
NO
YES
EARLY STATUS DATA TRANSFER
FT
Charts 129, 132
Wrong Length Record: Should Not be Here
SENSE COMMAND OR FINAL STATUS
FF
QH341
Set Bit 7 of Op Register to 1 (Indicates the Sector Count is 00)
Multiple Entry
QH341
Readout Module Number Used for Initial Selection
Set H5 to Prevent Interrupts
QH341
Operational In Up
YES
NO
QH341
Set Bus-Out Control, Address Out, and Command Start
QH341
Operational In Up
NO
YES
QH341
Status In-Up
NO
YES
Short Busy: Should Not be Here
QH341
Reset Address Out
QH341
Address In-Up
NO
YES
QH341
Reset Suppress Out
QH341
Address Out Matches Address In
NO
YES
QH541
Restore B- and I-Stars
QH541
To General Halt
QE641
HB
Chart 155
QH351
Setup Sense Command 04
QH361
Store Command in MPX Storage
QH361
Set Bus-Out Control, Command Out, and Command Start
QH361
Status In Up
NO
YES
QH361
Set Service Out and Command Start
QH511
Status In Up
YES
NO
QH511
Service In Up
NO
YES
Read in Sense Bytes 0,1,2, and 3 One at a Time and Decode the Conditions
Working on Sense Byte 0,1, 2, or 3
SENSE BYTE 0
QH511
Set Service Out and Command Start
QH511
Store Sense Byte in MPX Storage
Test Bits 2,4, and 5 of Sense Byte 0. If Any are Set to 1, Setup to Set File Branch Byte Bit 4 (Validity). Test Bits 0,1, and 7. If any are Set to 1, Setup to Set File Branch Byte Bit 5 (Not Ready).
Sense Byte 0 Bit
0-Command Reject
1-Intervention Required
2-Bus-Out Parity
3-Not Tested (Duplicate)
4-Data Check
5-Overrun
6-Track Condition Check
7-Seek Check
QH511
Test Bit 6 of Sense Byte 0, if a 1 (on) Set a Indicator for Alternate Track Op
SENSE BYTE 1
QH511
Set Service Out and Command Start
QH511
Store Sense Byte 1 in MPX Storage
QH511
Test Bits 0,2,4, and 6 of Sense Byte 1. If Set to a 1, Set Up to Set Bit 0 of the File Branch Byte to 1. If Bit 2 Is Set to a 1, Set Up to Set the File Branch Byte Bits 0 and 2 (No Address Compare and Wrong Length Record). Test Bit 1. If Set to a 1, Set Up to Set File Branch Byte Bit 5 (Not Ready)
Sense Byte 1 Bit
0-Data Check in Count
1-Track Overrun-Write
2-End of Cylinder
3-Not Tested (Duplicate)
4-No Record Found
5-Not Tested (Duplicate)
6-Missing Address Marker
7-Not Tested (2030 Mode)
SENSE BYTE 2
QH511
Set Service Out and Command Start
QH511
Store Sense Byte 1 in MPX Storage
QH511
Test Bit 2 of Sense Byte 2. If Set to a 1 Setup to Set File Branch Byte Bit 4 (Validity). Test Bits 0,3,4, and 7 (Bit 7 Should Always Be 0). If Any are Set to a 1, Setup to Set File Branch Byte Bit 5 (Not Ready)
Sense Byte 2 Bit.
0-Unsafe
1-Not Tested (Unused)
2-Change Tag Line Check
3-Check
4-2841 All Check
5-Not Tested (Unused)
6-Not Tested (Unused)
7-Tested But Not Used
SENSE BYTE 3
QH511
Set Service Out and Command Start
QH511
Store Sense Byte 3 in MPX Storage
Sense Byte 3 is not Tested
QH511
Service In Up
YES
NO
Bit 5 - Not Ready
QH511
Was Bit 5 of File Branch Byte Set
YES
NO
QH521
Set Indicator CS-Register Bit to Force Correct Exit (No Compare Sector Op)
Flagged Track
QH521
Was Sense Byte 0 Bit 6 On
NO
YES
QH521
Set Op Register Bits 0 and 4 to 1. Set Op Register Bit 7 to 0
QH341
FM
Chart 133
To Alternate Track Read R0
QH531
Using Alternate Track
YES
NO
QH531
FN
Chart 135
To Seek for Original Track
QH531
Any Error Bits On in File Branch Byte
NO
YES
Set Bit 3 (Any Disk Condition) and Reset Bit 6 (Read Back Check) of the File Branch Byte
QH531
Address Operations (6 or 7)
YES
NO
QH531
Set Bit 0 and 3 of File Branch Byte if in Sector Mode and Record Number Is Less than 16 (Dec)
QH531
Address Compared On Search
NO
YES
QH401
To Restore Address
Restore B- and I-Stars
QH541
Restore A, B, and I-Stars
Restore A,B, and I-Stars
Bit 5 of Byte at 9F CPU Allows I/O Traps if On
QG031
Test Bit 5 of PMS Byte in CPU Storage
QG032
Allow I/O Traps
YES
QG031
Reset H5 and Command Start to Allow Traps
NO
QF661
Interrupt Exists
YES
NO
QE001
To Interrupt Decode
QE001
BA
Chart 155
QE001
To I-Cycles
QE001
AA
Chart 102


Start
QH301
Store I-Star, Setup the Op Register for a Read or Write, Move or Load.
0000 0000 - Write Load
0001 0000 - Read Load
0010 0000 - Write Move
0011 0000 - Read Move
DCF 1400 - 1311
*/ND1 D2 D3 D4 D5 D6 S1 S2 S3
Example
* 051976XXX
Change to 2311 Format by Doing Table Lookup to Select Module 2, Cylinder 59, Head 8, and Record 16. This Can Be Determined by Dividing D2 D3 D4 D5 By 2 and Use the Remainder with D tor the Record. Add 1 to the Cylinder and Record Values for 2311 Format. End Result Is:
1400 2311
Module 4 2
Cylinder 59 + 1 3C
Head 08 08
Record 16 + 1 11
QH301,311
Readout the Disk Control Field and Change From a 1400-1311 Format to a 2311 Format. Change the Op Register to Indicate Sector or Track Mode.
Op Register
0000 XXXX Write Load
0001 XXXX Read Load
0010 XXXX Write Move
0011 XXXX Read Move
0110 Sector Mode
1100 Track Mode
QH341
Send Address Out. If Status is Received, Set File Branch Byte for Busy and Any Disk Condition. Restore the A,B, and I-Stars and Return to I-Cycles. If Status Isn't Received, Wait for Operational In and Address In. Check for Correct Address. Set H5 On (Prevent Interrupts)
QH341
Address Out Matches Address
NO
General Stop
YES
QH351
Setup a Head Seek Command of 1B
QH351
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
QH361
Is Status 00
NO
QH361
If Status has an Unit Check or Unit Exception, Set Up for a Sense Command. If UC or UE Bits are Not On, Check for Device End or Control Unit End. If Either DE or CUE Are On, Retry the Command; Otherwise Set the File Branch Byte to Busy and Any Disk Condition, then Restore the A, B, and I- Stars and Return to I-Cycles
QH361
Unit Check or Unit Exception On
NO
YES
Sense Command
QH361
Device End or Control End Up
YES
NO
To I-Cycles
YES
QH371
Setup to do a Head Seek Address Transfer. Sent to the Control Unit BBCCHH from the MPX Storage.
QH381
After Last Character is Transferred Wait for Status In. Check Status for Device End or Channel End; One or the Other Should Be Received if Not go to General Stop. If DE or CE are Up, Check for Unit Check. If UC Exist go to General Stop
QH381
No DF,CE, or Have a Unit Check
NO
YES
General Stop
QH421
Store the Operation Code (Op Register) in MPX Storage to Remember what Operation was Done Last. If this Operation is Write, Set the Read Back Check Interlock Bit On (Bit 6 of File Branch Byte.
QH421
Readout Compare and Module Protect Disable Byte. Check if Module Protect is to be Done, If it is Check Selected File Number Against a Fixed Number. If Numbers Match Go On, If Not go to a General Stop
QH421
Module Error Occurred
YES
General Stop
NO
QH421
Setup the Op Register to Indicate an Address Operation (Bit 6)
0000 0010 - Write Load
0001 0010 - Read Load
0010 0010 - Write Move
0011 0010 - Read Move
Set an Indicator Bit (S-Register) to Remember if this is a Track Mode
QH422
Set Count Field in MPX Storage to 0064 (Sector Mode) or 0BA4 (Track Mode).
Hex Decimal
0064 0100
0BA4 2980
QH422
Check to See if the Compare Disable Bit is On. If it is On, Setup a Search to Record 0 without First Searching for the Record Address.
Chart 138
QH422
Compare Disable On
YES
NO
QH521
Set Record Value to 00 and the Cylinder Value to the Seek Cylinder Value
Insure Op Register Bit 7 is 0.
QH341
Readout Selected File Number and Send the Address to the Control Unit. Wait for Address In, then Compare Address Out to Address In.
QH341
Address Out Matches Address In
NO
General Stop
YES
QH351
Setup a Search Command (31).
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
Status Should be Zero at this Time
QH361
Is Status Zero
NO
YES
QH361
Unit Check or Unit Exception On
YES
Sense Command
NO
QH361
Device End or Control Unit End Bits Up
YES
NO
To I-Cycles
2
QH371
Send to the Control Unit CCHHR.
QH371
Early Status
NO
YES
QH381
After Last Character is Sent, Wait for Status In. Check Status for Device End or Channel End, Should Receive One or the Other. If Not go to a General Stop. With DE or CE Up, Check for Unit Check Bit. If Unit Check Bit is On, a Sense Command Must be Done to Find Out the Cause of the Unit Check.
QH381
Device End or Channel End Up
NO
General Stop
YES
QH391
Unit Check Bit On
YES
NO
QH391
Was an Equal Address Found on this Search; If Not Repeat the Search Command
QH391
Equal Address Found
NO
YES
1
Chart 138
FW
1
QH391
If Search Just Completed was for Record 0, the Search is Completed. If it wasn't a Search On Record 0 Must be Done to Set the File and Control Unit in Time.
QH391
Record 0 has Been Found
NO
YES
FU
Chart 138
After Each Character is Sent, a Test for Status in is Done. If Status In Comes Up, the Unit Check Bit Should be On. The Unit Check Bit is Set if the Track is Flagged (Defective Track) or an Equal Address On a ID Search is Not Found Before the Disc Passes the File Index Point Twice. This Causes Early Status and a Sense Command is Done
Chart 138
FY
QH341
Set Op Register Bit 7 to 1 (Sector Count 00).
QH341
Readout Selected File Number and Send the Address to the Control Unit. Wait for Address In, then Compare Address Out to Address In.
QH341
Address Out Matches Address In
YES
NO
General Stop
QH351
Setup Sense Command 04.
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In.
QH361
Send Service Out
QH511
Bring in Sense Bytes 0,1,2, and 3 One Byte at a Time and Store in MPX Storage. Test Selected Bits of Sense Byte 0,1, and 2 for Error Condition and Set the File Branch Byte to Indicate the Error Condition. If Bit 6 of the Sense Byte 0 (Flagged Track) is On Set an Indicator Bit On.
QH521
Was Bit 6 of Byte 0 On
NO
FV
Chart 138
YES
QH521
Set Op Register Bit 0 to a 1 and Bit 7 to a 0
QH341
Readout Selected File Unit Number and Send the Address to the Control Unit. Wait for Address In, then Compare Address Out to Address In.
QH341
Address Out Matches Address In
NO
General Stop
YES
QH351
Setup Command (16) to Read Record 0 Address
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
QH361
Is Status 00
YES
NO
QH361
If Unit Check or Unit Exception is Up do a Restore A,B, and I-Stars and Return to I-Cycles. If UC and UE are Down, but Device End is Up the Read R0 will Not be Done Otherwise Repeat Cmnd
Status Should be 00
QH361
Device End Up
NO
YES
QH381
No DE, CE, or Have a Unit Check
NO
YES
General Stop
QH371
Read In the CCHH Values from Record R0 and Store in CPU Storage. Issue Command Out to Bring Status In.
QH381
Check Status for Either Device End or Channel End. If Either One is On, Check for Unit Check; If Not go to General Stop. If an Unit Check is Found do a Sense Command, If Not Setup to do a Full Seek to an Alternate Track Using CCHH from Record 0.
QH381
Device-End or Channel End Up
NO
General Stop
YES
QH391
Unit Check Bit On
YES
NO
QH391
Setup to Develop a Full Seek Command to an Alternate Track.
QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In.
QH341
Address Out Matches Address In
NO
General Stop
YES
QH351
Setup a Full Seek Command 07.
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
QH361
Is Status 00
NO
YES
QH371
Status Should be Zero on the First Pass.
Send Bin Bin of 0000 to the Control Unit
QH371
Send CCHH Values,Read from Record R0 into CPU Storage,to the Control Unit.
QH381
Wait for Status In. Check Status for Device End or Channel End, Go to General Stop if One or the Other is Not On. Check for an Unit Check, if Bit is On go to a General Stop. Otherwise Repeat the Seek Command and Status will be Non-Zero because Device is Busy Seeking
QH361
Check for Unit Check or Unit Exception, If On Set Up a Sense Command.
If Not Test for Device End; DE will Not be Up Until the Seek is Completed. Until Device End Comes Up Repeat Seek Command
QH361
Unit Check or Unit Exception On
YES
NO
Sense Command
QH361
Device End Up
NO
YES
QH361
Insure Bit 4 of the Op Register is 0
QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In.
QH341
Address Out Matches Address In
NO
General Stop
YES
QH351
Setup a Search Command 31.
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
QH361
Is Status 00
YES
NO
2
QH361
If Unit Check or Unit Exception Bit is On, Set Up for a Sense Command., Otherwise Repeat Search Command
QH361
Unit Check or Unit Exception On
YES
NO
Sense Command


6
FU
Chart 137
QH391
Read or Write
READ
WRITE
QH311
Readout of Main Storage the Address to be Written On the Disc Starting with the Second Character. Change the Address to 2311 Format and Store in MPX Storage
QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In.
QH341
Address Out Matches Address In
Yes
No
General Stop
QH351
Read or Write
READ
WRITE
QH351
Setup Command for Read with Address (IE)
QH351
Setup Command for Write with Address (ID)
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test For Zero Status. (Status Should be Zero)
QH361
Is Status 00
NO
YES
QH361
Unit Check or Unit Exception On
NO
YES
Sense Command
QH361
Device End or Control Unit End Up
YES
NO
1-Cycles
QH371
Read or Write
READ
WRITE
QH371
Read In from the Control Unit and Store in MPX Storage CCHHRKDD Values. If Status In Comes Up During this Time Issue a Sense Command
QH371
Send to the Control Unit from MPX Storage the CCHHRKDD Values. If Status In Comes Up During this Time Issue a Sense Command
QH371
Status In Up
YES
NO
QH371
Status In Up
YES
NO
QH401
Subtract 1 from the Cylinder Value Just Read In and Convert the Remainder into Two, Units and Tens, Decimal Digits. Subtract 1 from the Record Value Just Read In
1
1
QH411
If Record Value is 10 or More, Subtract 10. Store Correct Record Value in Main Storage. Double the Head Value Just Read In. Add 1 if the Record Value was 10 or More. Store Correct Head Value in Main Storage. Double the Cylinder Units Value, Add 1 if a Carry Occurred on Head Conversion and Store Results in Main Storage. Double the Cylinder Tens Value, Add 1 if a Carry Occurred on Cylinder Units Conversion and Store in Main Storage.
Read-In C C H H R
00 3C 00 08 11
Conversion 60 08 17
Minus 1 11
1400 59 08 6
Stored 19 7 6
QH411,412
Readout from MPX Storage the 1400 File Unit Number. Add 1 to it if a Carry Occurred On the Cylinder Tens Conversion. If a Cylinder Overflow was Found on the Cylinder Hexadecimal to Decimal Conversion Add 2 More to the Module Value and Store in Main Storage. Readout the Next Position of Main Storage and Write Back the Digit Portion of the Byte
QH412
Setup Main Storage Address where the First Data Character is to be Stored
QH441
Subtract 1 from the Sector Count
QH441
Is Sector Count 00
YES
NO
QH441
Set Op Register Bit 4 and Bit 7 to 1 (Data Transfer and Sector Count is Zero).
QH441
Set Op Register Bit 4 to 1 (Data Transfer)
QH451
Setup Counter for Data Field Length.
Move Op Hex Decimal
Sector Mode 0064 0100
Track Mode 08A4 2980
Load Op Hex Decimal
Sector Mode 005A 0090
Track Mode 0A7A 2682
QH471
Read or Write
READ
WRITE
QH471
Readout Character from Main Storage and Subtract 1 from the Counter. Check Character to See if it is a GMWM, if it is Set an Indicator for Wrong Length Record. Change the GM-WM to a Blank (40) and Send it to the Control Unit. If Not a GMWM, Send Character to the Control Unit; Wordmarks are Controlled by Move or Load Op. Check to See if the Counter is Zero. If Status In Comes Up, Set-up for a Sense Command or Wrong Length Record.
QH471
Status In Up
YES
NO
QH471
Counter is 0000
NO
YES
3
3
QH471
Readout Position of Main Storage where the Character is to be Stored. Check Main Storage Character to See if it is a GMWM. If it is, Do Not Advance the B-Star and Continue to Readout the Same Position Until the Counter is Zero. If a GMWM is Not Found, Continue to Bring in a Character at a Time Until the Counter is Zero. If Status In Comes Up and GMWM has Not Been Found Setup for a Sense Command or Wrong Length Record.
QH471
A GMWM has Been Read Out
YES
NO
QH471
Status In Up
YES
NO
QH471
Counter is 0000
NO
YES
4
4
QH471
Counter is 0000
YES
NO
5
5
QH501
If Read is a Load Operation, Bring in 91st Character. Check Last Character In, Load and Move, to See if the Character has a Word-mark. Set an Indicator Bit for Validity Error if Read is a Load Op and Last Character In Did Not have a Wordmark or Read is a Move Op and Last Character In has a Wordmark
QH501
Readout the Next Char from Main Storage and Check to See if it is a GMWM. Also Check to See if Sector Count is Zero. Set Op Register Bit 7 to 1 (Sector Count-000)
QH501
Character is GMWM
YES
NO
QH501
Sector Count is 000
YES
NO
QH501
Set Op Register Bit 7 Back to 0.
QH501
Set Wrong Length Record Bit in File Branch Byte
QH501
Is Validity Error Indicator On
YES
NO
QH501
Set Disk Error Bit in File Branch Byte On
QH501
If Read is a Load Operation Bring in 91st Character. Check Last Character In, Load or Move, to See if the Character has a Word-mark. Set Op Register Bit 7 to a1 (Force Sector Count is Zero Indication On). Set an Indicator Bit On for Validity Error if Read is a Load Op and Last Character In Did Not have a Wordmark or Read is a Move Op and Last Character In has a Wordmark.
QH471
Wrong Length Record Indication On
NO
YES
QH471
Load or Move
LOAD
MOVE QH501
Set Op Register Bit 7 to 1 and Wrong Length Record Bit in the File Branch Byte.
QH341
Unit Check Bit On
YES
NO
QH531
Set Wrong Length Record in File Branch Byte
2
2
FY
Chart 137
Chart 137 FY
2
QH531
Using Alternate Track
YES
NO
QH531
Check for Any Error Bits Being On in the File Branch Byte. If Any are On, Set the Any Disc Condition Bit and Reset the Read Back Check Interlock Bit.
QH531
Setup to Seek to the Original Cylinder.
QH422
Set the Original Seek Cylinder Value into the Search Cylinder Byte.
QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In
QH341
Address Out Matches Address In
YES
NO
QH351
Setup Command (07) for Full Seek to Orginal Track
General Stop
If Record Number Is Less than 16 (Dec) and Op Is in Sector Mode, Set Bit 0 and 3 of File Branch Byte
QH541
Restore A,B, and I-Stars
QG031
Test Program Mode Switch Byte for Allow I/O Traps and Set Conditions Accordingly.
To 1-Cycles
Status Should be Zero on First Pass
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status
QH361
Is Status 00
NO
YES
QH371
Send to the Control Unit Bin Bin of 0000
QH371
Send to the Control Unit from MPX Storage CCHH
QH381
After Values are Sent Wait for Status In. Status Should Have Channel End Up or Device End, if Not Go to General Stop. With DE or CE Up Test for an Unit Check, if On Go to General Stop. If Not Repeat Seek Command, but This Time Status is Non-Zero as the Unit is Seeking to Orginial Track
If Unit Check or Unit Exception Are On, Set Up for a Sense Command, Otherwise Check for Device End; DE will Not Be Up Until the Seek Is Completed
QH361
Unit Check or Unit Exception On
YES
NO
QH361
Device End Up
NO
YES
QH361
Set Op Register Bit 4 to 0
QH381
Wait for Status In or Service In. If Service In Is Received, a Wrong Length Record Condition Must Be Set for Load. If Status In Is Received, Either Device End or Channel End Must Be Up. If Not, Go to General Stop. With DE or CE Up, Check for Unit Check. If UC On, Issue a Sense Command; if Not, Check for Sector Count of Zero
QH381
Service In Up
NO
YES
QH381
Issue Command Out to End Operation
QH381
Load or Move Mode
Move
Load
QH381
Device End or Channel End Up
NO
YES
QH381
No DE, CE or have a Unit Check
NO
YES
General Stop
QH391
Unit Check Bit On
YES
NO
QH391
Sector Count is 000
NO
YES
6
2
FY
Chart 137
QH361
Sector Count is 000
YES
NO
QH422
Set Op Register Bit 0 to 0 (Not Alternate Track)
Sector Count Should be 000 for 6 and 7 Ops.
QH361,422
Setup to Do a Head Seek
QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In.
QH341
Address Out Matches Address In
NO
YES
General Stop
QH351
Setup Head Seek Command 1B
QH361
Store Command in MPX Storage and Issue the Command, Wait for Status In and Test for Zero Status.
QH361
Is Status 00
NO
YES
QH371
Send to the Control Unit Bin Bin of 0000.
QH371
Send to the Control Unit from MPX Storage CCHH.
QH381
After Values are Sent, Wait for Status In. Status should have Channel End or Device End Up, if not Go to General Stop. With DE or CE Up Test for an Unit Check, if On Go to General Stop
QH381
No DE,CE or have an Unit Check
YES
NO
General Stop
QH381
Set Op Register Bit 0 to 0 (Not Alternate Track)
FW
Chart 137
QH361
Unit Check or Unit Exception Bits On Set Up for Sense Command. Otherwise Repeat the Head Seek
QH361
Unit Check or Unit Exception Bit On
YES
NO
Sense Command


Start
QH301
Store I-Star, Setup the Op Register for a Read or Write, Move or Load.
0000 0000 - Write Load
0001 0000 - Read Load
0010 0000 - Write Move
0011 0000 - Read Move
DCF 1400-1311
*/ND1 D2 D3 D4 D5 D6 S1 S2 S3
Example
*051976XXX
Change to 2311 Format by Doing Table Lookup to Select Module 2, Cylinder 59, Head 8, and Record 16. This Can be Determined by Dividing D2 D3 D4 D5 by 2 and Use the Remainder with D6 for the Record.
Add 1 to the Cylinder and Record Values for 2311 Format. End Result is:
1400 2311
Module 4 2
Cylinder 59 + 1 3C
Head 08 08
Record 16 + 1 11
QH301,311
Readout the Disk Control Field and Change from a 1400-1311 Format to a 2311 Format, Change the Op Register to Indicate Sector or Track Mode.
Op Register
0000 XXXX Write Load
0001 XXXX Read Load
0010 XXXX Write Move
0011 XXXX Read Move
0001 Sector Mode
0010 Track Mode
0101 Sector Overlay
QH341
Send Address Out. If Status is Received, Set File Branch Byte for Busy and Any Disk Condition. Restore the A,B, and I-Stars and Return to I-Cycles. If Status Isn't Received, Wait for Operational In and Address In. Check for Correct Address. Set H5
QH341
Address Out Matches Address
NO
General Stop
YES
QH351
Setup a Head Seek Command of 1B
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
QH361
Is Status 00
NO
QH361
If Status Has an Unit Check or Unit Exception Bit On Do a Sense Command. Restore the A-, B-, and I-Stars, Then Return to I-Cycles. If UC or UE Bits Are Not On, Check for Device End or Control Unit End. If Either DE or CUE Are On, Retry the Command, Otherwise Set the File Branch Byte to Busy and Any Disk Condition, Then Restore the A-, B-, and I-Stars and Return to I-Cycles
YES
QH371
Setup to do a Head Seek Address Transfer. Sent to the Control Unit BBCCHH from the MPX Storage.
QH381
After Last Character is Transferred Wait for Status In. Check Status for Device End or Channel End; One or the Other Should be Received. If Not go to General Stop. If DE or CE are Up Check for Unit Check. If UC Exist go to General Stop
QH381
No DE, CE, or Have a Unit Check
NO
YES
General Stop
QH361
Device End or Controll End Up
YES
NO
To I-Cycles
QH361
Device End or Controll End Up
YES
NO
To I-Cycles
QH421
Store the Operation Code (Op Register) in MPX Storage to Remember what Operation was Done Last. If this Opeartion is Write, Set the Read Back Check Interlock Bit On (Bit 6 of File Branch Byte)
QH421
Readout Compare and Module Protect Disable Byte. Check if Module Protect is to be Done If it is Check Selected File' Number Against a Fixed Number. If Numbers Match Go On, If Not Go to a General Stop
QH421
Module Error Occurred
YES
General Stop
NO
QH421
Setup the Op Register to Indicate Operation
0000 0000 - Write Load
0001 0000 - Read Load
0010 0000 - Write Move
0011 0000 - Read Move
Set an Indicator Bit (S-Register) to Remember if this is a Track Mode
QH421
Sector Overlay Op
NO
YES
QH421
Setup the Counter Used to Address Main Storage to Allow the Writing or Reading of Sector Count
Chart 140
FW
QH341
Readout Selected File Number and Send the Address to the Control Unit. Wait for Address In, then Compare Address Out to Address In.
QH341
Address Out Matches Address In
NO
General Stop
YES
QH351
Setup a Search Command (31) or (B1).
Use B1 when Head Switching is Required.
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
Status Should be Zero at this Time
QH361
Is Status Zero
NO
YES
2
After Each Character Is Sent, a Test for Status In is Done. If Status In Comes Up, the Unit Check Bit should be On. The Unit Check Bit is Set if the Track is Flagged (Defective Track) or an Equal Address on a ID Search is Not Found. Before the Disk Passes the File Index Point Twice. This Causes Early Status and a Sense Command is Done.
QH361
Unit Check or Unit Exception On
YES
NO
QH361
Device End or Control Unit End Bits Up
YES
NO
To I-Cycles
Sense Command
QH371
Send to the Control Unit CCHHR.
QH371
Is Status Zero
NO
YES
Chart 140
FY
QH381
After Last Character is Sent, Wait for Status In. Check Status for Device End or Channel End, Should Receive One or the Other. If Not go to a General Stop. With DE or CE Up, Check for Unit Check Bit. If Unit Check Bit is On, a Sense Command Must be Done to Find Out the Cause of the Unit Check.
QH341
Set Op Register Bit 7 to 1 (Sector Count 00).
QH341
Readout Selected File Number and Send the Address to the Control Unit. Wait for Address In, Then Compare Address Out to Address In.
QH341
Address Out Matches Address In
YES
NO
General Stop
QH381
Device End or Channel End Up
NO
General Stop
YES
QH391
Unit Check Bit On
YES
NO
QH391
Was an Equal Address Found on this Search; If Not Repeat the Search Command
QH391
Equal Address Found
NO
YES
FU
Chart 140
QH351
Setup Sense Command 04.
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In.
QH361
Send Service Out
QH511
Bring in Sense Bytes 0, 1, 2, and 3 One Byte at a Time and Store in MPX Storage. Test Selected Bits of Sense Byte 0, 1, and 2 for Error Condition and Set the File Branch Byte to Indicate the Error Condition. If Bit 6 of the Sense Byte 0 (Flagged Track) is On Set an Indicator Bit On.
QH521
Was Bit 6 of Byte 0 On
NO
FV
Chart 140
YES
QH521
Set Op Register Bit 0 to a 1 and Bit 7 to 20
QH341
Readout Selected File Unit Number and Send the Address to the Control Unit. Wait for Address In, then Compare Address Out to Address In.
QH341
Address Out Matches Address In
NO
General Stop
QH351
Setup Command (16) to Read Record 0 Address
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
QH361
Is Status 00
YES
Status Should be 00
NO
QH361
If Unit Check or Unit Exception Is Up, Do a Sense Command. If UC and UE Are Down, but Device End Is Up, the Read R0 Will Not Be Done. Otherwise Repeat Command
QH361
Unit Check or Unit Exception
YES
Sense Command
NO
Device End Up
NO
YES
QH371
Read In the CCHH Values from Record R0 and Store in CPU Storage. Issue Command Out to Bring Status In.
QH381
Check Status for Either Device End or Channel End. If Either One is On, Check for Unit Check; If Not go to General Stop. If an Unit Check is Found do a Sense Command, If Not Setup to do a Full Seek to an Alternate Track Using CCHH from Record 0.
QH381
Device End or Channel End Up
NO
General Stop
YES
QH391
Unit Check Bit On
YES
NO
QH391
Setup to Develop a Full Seek Command to an Alternate Track.
QH341
Readout Selected File Unit Number and Send the Address to the Control Unit. Wait for Address In, then Compare Address Out to Address In,
QH341
Address Out Matches Address In
NO
General Stop
YES
QH351
Setup a Full Seek Command 07.
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
QH361
Is Status 00
NO
YES
Status Should be Zero on the First Pass.
QH371
Send Bin Bin of 0000 to the Control Unit
QH371
Send CCHH Values Read from Record R0 into CPU Storage to the Control Unit.
QH381
Wait for Status In. Check Status for Device End or Channel End, Go to General Stop if One or the Other is Not On. Check for an Unit Check, if Bit is On go to a General Stop. Otherwise Repeat the Seek Command and Status will be Non-Zero because Device is Busy Seeking
QH381
No DE, CE, or Have a Unit Check
NO
YES
General Stop
QH361
Check for Unit Check or Unit Exception. If On, Do a Sense Command. If Not Test for Device End. DE Will Not Be Up Until the Seek Is Completed. Until Device End Comes Up, Repeat Seek Command
QH361
Unit Check or Unit Exception On
YES
Sense Command
NO
Device End Up
NO
YES
QH361
Insure Bit 4 of the Op Register is 0
QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In.
QH341
Address Out Matches Address In
NO
General Stop
YES
QH351
Setup a Search Command 31.
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
QH361
Is Status 00
YES
2
NO
If Unit Check or Unit Exception Bit Is On, Do a Sense Command. Otherwise Repeat Search Command
QH361
Unit Check or Unit Exception On
YES
Sense Command
NO


FU
Chart 139
QH441
Subtract 1 from the Sector Count
QH441
Is Sector Count 000
Yes
No
QH441
Set Op Register Bit 4 and Bit 7 to 1 (Data Transfer and Sector Count is Zero)
QH441
Set Op Register Bit 4 to 1 (Data Transfer)
QH341
Read Out Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, Then Compare Address Out to Address In.
QH341
Address Out Matches Address In
YES
NO
General Stop
QH351
Read or Write
READ
WRITE
QH351
Set Up Command for Read (06)
QH351
Set Up Command for Write (05)
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status. (Status Should be Zero)
QH361
Is Status 00
NO
YES
Unit Check or UnitException On
YES
NO
Sense Command
QH451
Set Up Counter for Data Field Length
Move Op Hex Decimal
Sector Mode 0064 0100
Track Mode 0BA4 2980
Load Op Hex Decimal
Sector Mode 005A 0090
Track Mode 0A7A 2682
YES
Device End of Control Unit End Up
NO
I-Cycles
QH471
Read or Write
WRITE
READ
QH471
Read Out Character from Main Storage and Subtract 1 from the Counter. Check Character to see if it is a GMWM, if it is Set an Indicator for Wrong Length Record. Change the GMWM to a Blank (40) and Send it to the Control Unit. Wordmarks are Controlled by Move or Load Op. Check to see if the Counter is Zero. If Status In Comes Up, Setup for a Sense Command or Wrong Length Record.
QH471
Read Out Position of Main Storage where the Character is to be Stored. Check Main Storage Character to see if it is a GMWM. If it is, do not Advance the B-Star and Continue to Read Out the Same Position Untill the Counter is Zero. If Status In Comes Up and a GMWM has not Been Found, Set Up for a Sense Command or Wrong Length Record.
QH471
Status In Up
YES
NO
QH471
Counter is 0000
NO
YES
QH471
Wrong Length Indication On
YES
NO
QH471
Load or Move
LOAD
MOVE
2
QH501
Set Op Register Bit 7 to 1 and Wrong Length Record in the File Branch Byte
5
QH471
A GMWM has Been Read Out
YES
NO
QH471
Status In Up
YES
NO
QH471
Counter is 0000
YES
NO
QH501
If Read is a Load Op Bring in the 91st Character. Check Last Character In, Move and Load, to See if the Character has a Wordmark Set a Indicator Bit if the Last Character has a Wordmark and Op is Move, or Op is Load and Last Character did not Have a Workmark.
QH501
Read Out the Next Character from Main Storage and Check to See if it is a GMWM. Also Check to See if Sector Count is Zero. Set Op Register Bit 7 to 1 (Sector Count).
QH501
Character is a GMWM
YES
NO
QH501
Sector Count is 000
YES
NO
QH501
Set Op Register Bit 7 to 0 (Sector Count Not 000)
QH501
Sector Count is 000
YES
NO
QH501
Set Wrong Length Record Bit in File Branch Byte
QH501
Is Validty Error Indicator On
YES
NO
QH501
Set Disk Error Bit in File Branch Byte On
1
1
QH381
Wait for Status In or Service In. If Service In is Received, a Wrong Length Record Condition Must be Set. If Status In is Received, Either Device End or Channel End Must be Up. If not, go to General Stop. If Unit Check is Up, Issue a Sense Command; if not, Check Sector Count
QH381
Service In Up
NO
QH381
Issue Command Out to End Operation
QH381
Load or Move Mode
Move
Load
2
QH381
Device End or Channel End Up
NO
YES
General Stop
QH391
Unit Check Bit On
YES
NO
FY
QH391
Sector Count is 000
YES
NO
QH431
Read Out Record Value from MPX Storage and Test to See if the Value is 14 (20 Decimal)
Record 20
NO
YES
QH431
Setup for Head Switch On Search. Set Record Value to 01. Set Op Register Bit 4 to 0. Readout the Head Value, Check for Head 9.
QH431
Add 1 to the Record Value. Set Op Register Bit 4 to 0. Set Bit 3 of I/O Error Byte to Indicate DCF has Been Incremented.
QH431
Using Head 9
YES
NO
QH431
Change Head Value to 00 and Add 1 to the Cylinder Value
QH431
Add 1 to Head Value
QH431
Using Alternate Track
YES
NO
QH391
Set Bit 3 of I/O Error Byte (DCF Incremented)
QH422
Store the Cylinder Value in the Cylinder Buffer Byte
3
Set Bit 3 of I/O Error Byte (DCF Incremented)
FW
Chart 139
QH501
If Read is a Load Operation Bring in 91st Character. Check Last Character In, Load or Move, to See if the Character has a Wordmark. Set Op Register Bit 7 to 1 (Sector Count is Zero). Set an Indicator Bit On for Validity Error if Read is a Load Op and Last Character In did Not have a Wordmark or Read is a Move Op and Last Character In has a Wordmark.
Counter is 0000
NO
YES
5
Chart 139
FV
5
QH341
Unit Check Bit On
YES
NO
FY
QH531
Set Wrong Length Record Bit in File Branch Byte On
Chart 139
6
QH531
Using Alternate Track
YES
NO
QH531
Check for Any Error Bits Being On in the File Branch Byte. If Any are On, Set the Any Disk Condition Bit and Reset the Read Back Check Indicator Bit.
QH531
Record Found
YES
NO
QH541
Restore A, B, and I-Stars
QG031
Test Program Mode Switch Byte for Allow I/O Traps and Set Conditions Accordingly
To I-Cycles
Read-In C C H H R
00 3C 00 08 11
Conversion 60 08 17
Minus 1 11
1400 59 08 6
Stored 19 7 6
3
QH531
Setup to Seek to the Original Cylinder
QH422
Set the Original Seek Cylinder Value into the Search Cylinder Byte
QH401
Set Up Main Storage Address to Store Convert Numbers
QH401
Subtract 1 from the Cylinder Value, Convert the Remainder into Two, Units and Tens, Decimal Digits. Subtract 1 from the Record Value
QH411
Has the DCF Been Incremented
YES
NO
QH411
If Record Value is Ten or More, Subtract Ten. Store Correct Record Value in Main Storage. Double the Head Value, Add 1 if Record Value was Ten or More. Store Correct Head Value in Main Storage. Double the Cylinder Units Value, Add 1 if Carry Occurred on Head Conversion and Store Results in Main Storage. Double the Cylinder Tens Value, Add 1 if a Carry Occurred on Cylinder Units Conversion and Store in Main Storage
QH411,412
Read Out from MPX Storage the 1400 File Unit Number. Add 1 to it if a Carry Occurred on the Cylinder Tens Conversion. If a Cylinder Overflow was Found on the Cylinder Hexadecimal to Decimal Conversion Add 2 More to the Module Value and Store in Main Storage. Readout the Next Position of Main Storage and Write Back the Digit Portion of the Byte.
QH531
Op Code Bit 4 On (Data Transfer)
YES
NO
QH531
Set Wrong Length Record Bit in File Branch Byte
6
QH541
Restore A, B, and I-Star
QG031
Test Program Mode Switch Byte for Allow I/O Traps and Set Conditions Accordingly
To I-Cycles
4
QH341
Read Out Selected File Unit Number and Send Address to the Control Unit. Wait for Address In and Compare Addresses. If Address do not Match go to General Stop.
QH351
Set Up Command (07) for Full Seek to Original Track
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status. Status Should be Zero on First Pass.
QH361
Is Status 00
NO
YES
QH371
Send to the Control Unit Bin Bin of 0000
QH371
Send to the Control Unit CCHH from MPX Storage
QH381
After Values are Sent Wait for Status In. Status Should Have Channel End Up or Device End, if not go to General Stop. With DE or CE up Test for an Unit Check, if on Go to General Stop. If Not Repeat Seek Command, But this Time Status is Non-Zero as the Unit is Seeking to Original Cylinder
QH381
No DE, CE or Have an Unit Check
NO
YES
4
General Stop
Unit Check or Unit Exception On, Do a Sense Command. Check for Device End. DE Will Not Be Up Until the Seek Is Completed
Unit Check or Unit Exception On
YES
NO
Sense Command
Device End Up
NO
YES
QH422
Sector Count is 000
YES
NO
Set Op Register Bit 0 to 0 (Not Alternate Track)
6
QH422
Set Up to Do a Head Seek
QH341
Read Out SelectedFile Unit Number and Send Address to the Control Unit. Wait for Address In and Compare Address. If Addresses do not Match Go to General Stop
QH351
Set Up Head Seek Command 18
QH361
Store Command in MPX Storage and Issue the Command, Wait for Status In and Test for Zero Status.
QH361
Is Status 00
NO
YES
QH371
Send to the Control Unit Bin Bin of 0000
QH371
Send to the Control Unit CCHH from MPX Storage
QH381
After Values are Sent Wait for Status In. Status Should have Channel End or Device End Up, If Not Go to General Stop. With DE or CE Up Test for an Unit Check, If on Go to General Stop. Otherwise Set Op Register Bit 0 to 0
FW
Chart 139
QH361
Unit Check or Unit Exception Bit On. If So Do a Sense Command. Otherwise Repeat the Head Seek
Unit Check or Unit Exception Bit On
NO
YES
Sense Command


Start
QH301
Store I-Star, Setup the Op Register for a Read or Write, Move or Load.
0000 0000 - Write Load
0001 0000 - Read Load
0010 0000 - Write Move
0011 0000 - Read Move
DCF 1400-1311
*/N D1 D2 D3 D4 D5 D6 S1 S2 S3
Example
*051976xxx
Change to 2311 Format by Doing Table Lookup to Select Module 2, Cylinder 59, Head 8, and Record 16. This can be Determined by Dividing D2 D3 D4 D5 by 2 and Use the Remainder with D6 for the Record. Add 1 to the Cylinder and Record Values for 2311 Format. End Result is:
1400 2311
Module 4 2
Cylinder 59 + 1 3C
Head 08 08
Record 16 ÷ 1 11
QH301,311
Readout the Disk Control Field and Change from a 1400-1311 Format to a 2311 Format. Change the Op Register to Indicate a Read Back Check
Op Register for RBC
0000 0011 Write Load
0001 0011 Read Load
0010 0011 Write Move
0011 0011 Read Move
QH341
Send Address Out. If Status is Received, Set File Branch Byte for Busy and Any Disk Condition. Restore the A,B, and I-Stars and Return to I-Cycles. If Status Isn't Received, Wait for Operational In and Address In. Check for Correct Address Set H5 to Prevent Interrupt.
QH341
Address Out Matches Address
NO
General Stop
YES
QH351
Setup a Head Seek Command of 1B
QH351
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
QH361
Is Status 00
NO
QH361
If Status has an Unit Check or Unit Exception Bit On, do a Sense Command. If UC or UE Bits are Not On Check for Device End or Control Unit End. If Either DE or CUE are On Retry the Command. Otherwise Set the File Branch Byte to Busy and any Disk Condition, then Restore the A, B, and I Stars and Return to I-Cycles
QH361
Unit Check or Unit Exception On
YES
Sense Command
QH361
Device End or Control End Up
YES
To I-Cycles
YES
QH371
Setup to do a Head Seek Address Transfer. Sent to the Control Unit BBCCHH from the MPX Storage.
QH381
After Last Character is Transferred Wait for Status In. Check Status for Device End or Channel End; One or the Other Should be Received. If Not go to General Stop. If DE or CE are Up, Check for Unit Check. If UC Exist go to General Stop
QH381
No DE, CE, or Have a Unit Check
NO
YES
General Stop
QH421
Readout Last Operation, Code and Set Op Register for Read Sector or Track Op Register
0101 XXXX Read Load
0111 XXXX Read Move
0110 Sector Address
1100 Track Address
QH421
Readout Compare and Module Protect Disable Byte. Check If Module Protect is to be Done, If it is, Check Selected File Number Against a Fixed Number. If Numbers Match Go On, If Not go to a General Stop
QH421
Module Error Occurred
YES
NO
General Stop
QH421
Setup the Op Register to Indicate an Address Operation (Bit 6)
0101 0010 - Read Load
0111 0010 - Read Move
Set an Indicator Bit (S-Register) to Remember if this is a Track Mode
QH422
Set Count Field in MPX Storage to 0064 (Sector Mode) or 0BA4 (Track Mode).
Hex Decimal
0064 0100
0BA4 2980
QH422
Check to See if the Compare Disable Bit is On. If it is On, Set Up a Search to Record 0 without First Searching for the Record Address.
Chart 142
FW
QH422
Compare Disable On
YES
NO
QH422
Set Record Value to 00 and the Cylinder Value to the Seek Cylinder Value
QH521
Insure Op Register Bit 7 is 0.
QH341
Readout Selected File Number and Send the Address to the Control Unit. Wait for Address In, then Compare Address Out to Address In.
QH341
Address Out Matches Address In
NO
General Stop
YES
QH351
Setup a Search Command (31).
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
Status Should be Zero at this Time
QH361
Is Status Zero
NO
YES
QH361
Unit Check or Unit Exception On
YES
Sense Command
NO
QH361
Device End or Control Unit End Bits Up
YES
NO
To I-Cycles
1
QH391
If Search Just Completed was for Record 0, the Search is Completed. If it wasn't, a Search On Record 0 Must be Done to Set the File and Control Unit in Time
QH391
Record 0 has been Found
NO
YES
FU
Chart 142
After Each Character is Sent, a Test for Status In is Done. If Status In Comes Up, the Unit Check Bit Should be On. The Unit Check Bit is Set if the Track is Flagged (Defective Track) or an Equal Address on a ID Search is Not Found before the Disc Passes the File Index Point Twice. This Causes Early Status and a Sense Command is Done.
2
QH371
Send to the Control Unit CCHHR.
QH371
Early Status
NO
YES
Chart 142
FY
QH381
After Last Character is Sent, Wait for Status In. Check Status for Device End or Channel End, Should Receive One or the Other. If Not go to a General Stop. With DE or CE Up, Check for Unit Check Bit. If Unit Check Bit is On, a Sense Command Must be Done to Find Out the Cause of the Unit Check
QH341
Set Op Register Bit 7 to 1 (Sector Count 00).
QH341
Readout Selected File Number and Send the Address to the Control Unit. Wait for Address In, then Compare Address Out to Address In.
QH341
Address Out Matches Address In
YES
NO
General Stop
QH381
Device End or Channel End Up
NO
General Stop
YES
QH391
Unit Check Bit On
YES
NO
QH391
Was an Equal Address Found on this Search; If Not Repeat the Search Command
QH391
Equal Address Found
NO
YES
1
QH351
Setup Sense Command 04.
QH361
Store Command in MPX Storage and Issue the Command . Wait for Status In.
QH361
Send Service Out
QH511
Bring in Sense Bytes 0,1,2, and 3 One Byte at a Time and Store in MPX Storage. Test Selected Bits of Sense Byte 0, 1, and 2 for Error Condition and Set the File Branch Byte to Indicate the Error Condition. If Bit 6 of the Sense Byte 0 (Flagged Track) is On Set an Indicator Bit On.
QH521
Was Bit 6 of Byte 0 On
NO
FV
YES
QH521
Set Op Register Bit 0 to a 1 and Bit 7 to a 0
Chart 142
QH341
Readout Selected File Unit Number and Send the Address to the Control Unit. Wait for Address In, then Compare Address Out to Address In.
QH341
Address Out Matches Address In
NO
General Stop
YES
QH351
Setup Command (16) to Read Record 0 Address
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
QH361
Is Status 00
YES
NO
QH361
If Unit Check or Unit Exception is Up do a Sense Command. If UC and UE are Down but Device End is Up the Read RO will Not be Done. Otherwise Repeat Command
Status Should be 00
QH361
Unit Check or Unit Exception On
YES
Sense Command
NO
QH361
Device End Up
NO
YES
QH371
Read In the CCHH Values from Record R0 and Store in CPU Storage. Issue Command Out to Bring Status In.
QH381
Check Status for Either Device End or Channel End. If Either One is On, Check for Unit Check; If Not go to General Stop. If an Unit Check is Found do a Sense Command, If Not Setup to do a Full Seek to an Alternate Track Using CCHH from Record 0.
QH381
Device End or Channel End Up
NO
General Stop
YES
QH391
Unit Check Bit On
YES
NO
QH391
Setup to Develop a Full Seek Command to an Alternate Track.
QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In.
QH341
Address Out Matches Address In
NO
General Stop
YES
QH351
Setup a Full Seek Command 07.
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
QH361
Is Status 00
NO
YES
QH371
Status Should be Zero On the First Pass.
Send Bin Bin of 0000 to the Control Unit
QH371
Send CCHH Values Read from Record R0 into CPU Storage to the Control Unit.
QH381
Wait for Status In. Check Status for Device End or Channel End, go to General Stop if One or the Other is Not On. Check for an Unit Check, if Bit is On go to a General Stop. Otherwise Repeat the Seek Command and Status will be Non-Zero because Device is Busy Seeking
No DE, CE, or Have a Unit Check
NO
YES
General Stop
Check for Unit Check or Unit Exception. If On, do a Sense Command. If Not, Test for Device End: DE will Not be Up Until the Seek is Completed. Until the Device End Comes Up Repeat Seek Command.
Unit Check or Unit Exception on
YES
NO
QH361
Sense Command
Device End Up
NO
YES
QH361
Insure Bit 4 of the Op Register is 0
QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In.
QH341
Address Out Matches Address In
NO
General Stop
YES
QH351
Setup a Search Command 31.
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
QH361
Is Status 00
YES
NO
2
If Unit Check or Unit Exception Bit is On Restore the A,B, and I Stars and go to I-Cycles. Otherwise Repeat Search Command
Unit Check or Unit Exception On
YES
NO
Sense Command

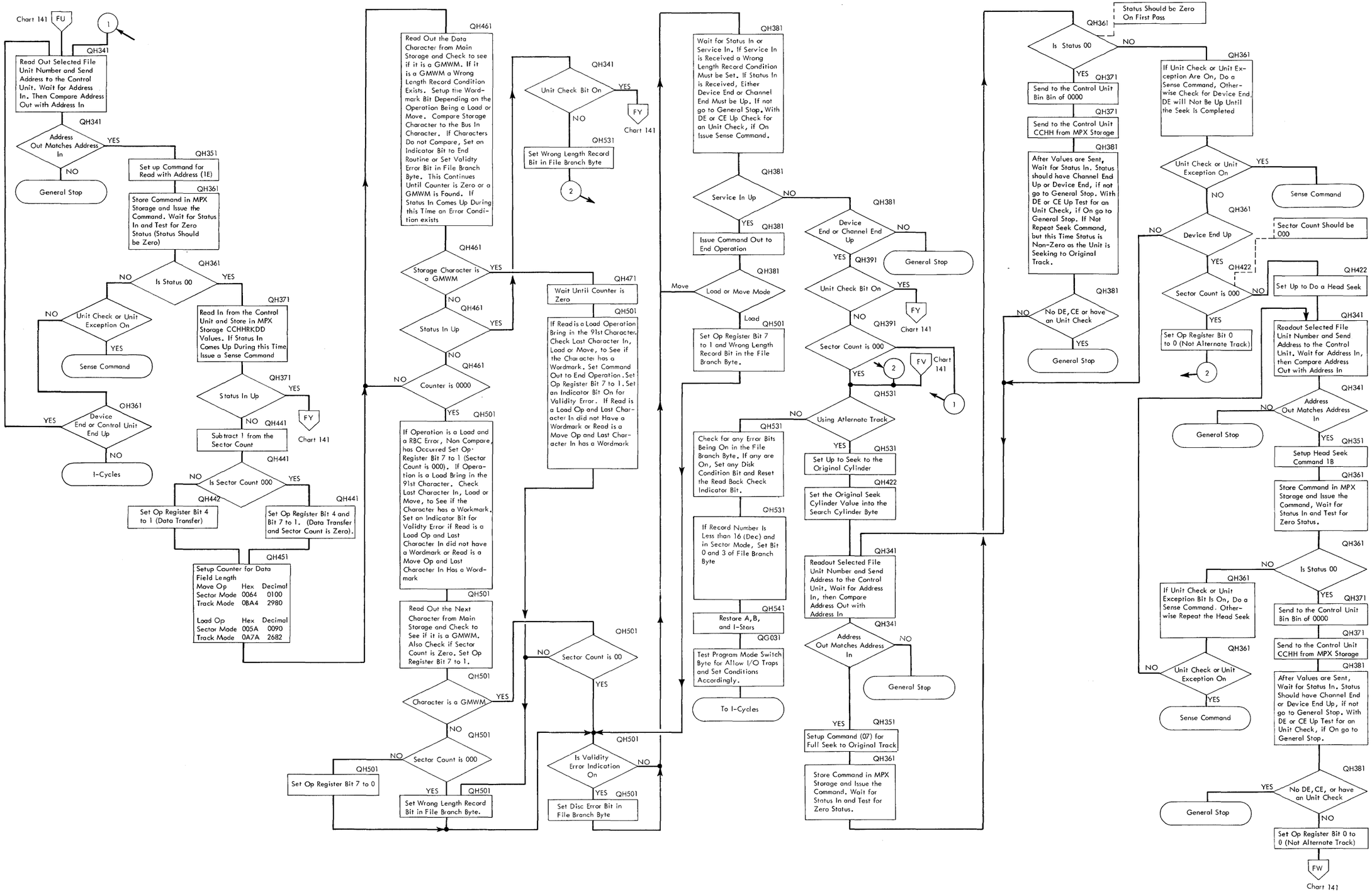


Chart 141 FU
1
QH341
Read Out Selected File Unit Number and Send Address to the Control Unit. Wait for Address In. Then Compare Address Out with Address In
QH341
Address Out Matches Address In
YES
NO
General Stop
QH351
Set up Command for Read with Address (1E)
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status (Status Should be Zero)
QH361
Is Status 00
NO
YES
QH371
Read In from the Control Unit and Store in MPX Storage CCHHRKDD Values. If Status In Comes Up During this Time Issue a Sense Command
NO
Unit Check or Unit Exception On
YES
Sense Command
QH371
Status In Up
YES
NO
FY
Chart 141
QH441
Subtract 1 from the Sector Count
QH441
Is Sector Count 000
NO
YES
QH442
Set Op Register Bit 4 to 1 (Data Transfer)
QH441
Set Op Register Bit 4 and Bit 7 to 1. (Data Transfer and Sector Count is Zero).
QH451
Setup Counter for Data Field Length
Move Op Hex 0064 Decimal 0100
Sector Mode Hex 0BA4 Decimal 2980
Track Mode
Load Op Hex 005A Decimal 0090
Sector Mode Hex 0A7A Decimal 2682
Track Mode
QH361
Device End or Control Unit End Up
YES
NO
1-Cycles
QH461
Read Out the Data Character from Main Storage and Check to see if it is a GMWM. If it is a GMWM a Wrong Length Record Condition Exists. Setup the Wordmark Bit Depending on the Operation Being a Load or Move. Compare Storage Character to the Bus In Character. If Characters Do not Compare, Set an Indicator Bit to End Routine or Set Validty Error Bit in File Branch Byte. This Continues Until Counter is Zero or a GMWM is Found. If Status In Comes Up During this Time an Error Condition exists
QH461
Storage Character is a GMWM
YES
NO
QH461
Status In Up
YES
NO
QH461
Counter is 0000
YES
QH501
If Operation is a Load and a RBC Error, Non Compare, has Occurred Set Op Register Bit 7 to 1 (Sector Count is 000). If Operation is a Load Bring in the 91st Character. Check Last Character In, Load or Move, to See if the Character has a Workmark. Set an Indicator Bit for Validty Error if Read is a Load Op and Last Character In did not have a Wordmark or Read is a Move Op and Last Character In Has a Wordmark
QH501
Read Out the Next Character from Main Storage and Check to See if it is a GMWM. Also Check if Sector Count is Zero. Set Op Register Bit 7 to 1.
QH501
Character is a GMWM
YES
NO
QH501
Sector Count is 000
NO
YES
QH501
Set Op Register Bit 7 to 0
QH501
Set Wrong Length Record Bit in File Branch Byte.
QH341
Unit Check Bit On
YES
NO
FY
Chart 141
QH531
Set Wrong Length Record Bit in File Branch Byte
2
QH471
Wait Until Counter is Zero
QH501
If Read is a Load Operation Bring in the 91st Character. Check Last Character In, Load or Move, to See if the Character has a Wordmark. Set Command Out to End Operation. Set Op Register Bit 7 to 1. Set an Indicator Bit On for Validity Error. If Read is a Load Op and Last Character In did not Have a Wordmark or Read is a Move Op and Last Character In has a Wordmark
QH501
Sector Count is 00
NO
YES
QH501
Is Validity Error Indication On
NO
YES
QH501
Set Disc Error Bit in File Branch Byte
QH381
Wait for Status In or Service In. If Service In is Received a Wrong Length Record Condition Must be Set. If Status In is Received, Either Device End or Channel End Must be Up. If not go to General Stop. With DE or CE Up Check for an Unit Check, if On Issue Sense Command.
QH381
Service In Up
NO
YES
QH381
Issue Command Out to End Operation
QH381
Load or Move Mode
Move
Load
QH501
Set Op Register Bit 7 to 1 and Wrong Length Record Bit in the File Branch Byte.
QH531
Check for any Error Bits Being On in the File Branch Byte. If any are On, Set any Disk Condition Bit and Reset the Read Back Check Indicator Bit.
QH531
If Record Number Is Less than 16 (Dec) and in Sector Mode, Set Bit 0 and 3 of File Branch Byte
QH541
Restore A,B, and I-Stars
QG031
Test Program Mode Switch Byte for Allow I/O Traps and Set Conditions Accordingly.
To I-Cycles
QH381
Device End or Channel End Up
NO
YES
General Stop
QH391
Unit Check Bit On
YES
NO
FY
Chart 141
QH391
Sector Count is 000
YES
NO
2
FV
Chart 141
QH531
Using Alternate Track
NO
YES
QH531
Set Up to Seek to the Original Cylinder
QH422
Set the Original Seek Cylinder Value into the Search Cylinder Byte
QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In
QH341
Address Out Matches Address In
NO
YES
General Stop
QH351
Setup Command (07) for Full Seek to Original Track
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
1
Status Should be Zero On First Pass
QH361
Is Status 00
NO
YES
QH371
Send to the Control Unit Bin Bin of 0000
QH371
Send to the Control Unit CCHH from MPX Storage
QH381
After Values are Sent, Wait for Status In. Status should have Channel End Up or Device End, if not go to General Stop. With DE or CE Up Test for an Unit Check, if On go to General Stop. If Not Repeat Seek Command, but this Time Status is Non-Zero as the Unit is Seeking to Original Track.
QH381
No DE, CE or have an Unit Check
YES
General Stop
QH361
If Unit Check or Unit Exception Are On, Do a Sense Command, Otherwise Check for Device End. DE will Not Be Up Until the Seek Is Completed
Unit Check or Unit Exception On
YES
NO
Sense Command
QH361
Device End Up
NO
YES
Sector Count Should be 000
QH422
Sector Count is 000
NO
YES
QH422
Set Up to Do a Head Seek
Set Op Register Bit 0 to 0 (Not Alternate Track)
2
QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In
QH341
Address Out Matches Address In
NO
YES
General Stop
QH351
Setup Head Seek Command 1B
QH361
Store Command in MPX Storage and Issue the Command, Wait for Status In and Test for Zero Status.
QH361
Is Status 00
NO
YES
QH361
If Unit Check or Unit Exception Bit Is On, Do a Sense Command. Otherwise Repeat the Head Seek
QH371
Send to the Control Unit Bin Bin of 0000
QH371
Send to the Control Unit CCHH from MPX Storage
QH381
After Values are Sent, Wait for Status In. Status Should have Channel End or Device End Up, if not go to General Stop. With DE or CE Up Test for an Unit Check, if On go to General Stop.
QH361
Unit Check or Unit Exception On
NO
YES
Sense Command
QH381
No DE, CE, or have an Unit Check
YES
NO
General Stop
Set Op Register Bit 0 to 0 (Not Alternate Track)
FW
Chart 141

Start

QH301

Store I-Star, Setup the Op Register for a Read or Write, Move or Load.
0000 0000 - Write Load
0001 0000 - Read Load
0010 0000 - Write Move
0011 0000 - Read Move

DCF 1400-1311
*/ND1 D2 D3 D4 D5 D6 S1 S2 S3
Example
*051976XXX
Change to 2311 Format by Doing Table Lookup to Select Module 2, Cylinder 59, Head 8, and Record 16. This can be Determined by Dividing D2 D3 D4 D5 by 2 and Use the Remainder with D6 for the Record. Add 1 to the Cylinder and Record Values for 2311 Format. End Result is:

	1400	2311
Module	4	2
Cylineer	59+1	3C
Head	08	08
Record	16+1	11

QH301,311

Read out the Disk Control Field and Change from a 1400-1311 Format to a 2311 Format. Change the Op Register to Indicate a Read Back Check

Op Register
0000 0011 Write Load
0001 0011 Read Load
0010 0011 Write Move
0011 0011 Read Move

QH341

Send Address Out. If Status is Received, Set File Branch Byte for Busy and Any Disk Condition. Restore the A,B, and I-Stars and Return to I-Cycles. If Status isn't Received Wait for Operational In and Address In. Check for Correct Address.

QH341

Address Out Matches Address In

NO → General Stop

YES

QH351

Setup a Head Seek Command of 1B

QH351

Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status

QH361

Is Status 00

NO

QH361

If Status Has an Unit Check or Unit Exception Bit On, Do a Sense Command. If UC or UE Bits Are Not On, Check for Device End or Control Unit End. If Either DE or CUE Are On, Retry the Command. Otherwise Set the File Branch Byte to Busy and any Disk Condition; Then Restore the A-, B-, and I-Stars and Return to I-Cycles

QH361

Unit Check or Unit Exception On

NO

YES → Sense Command

QH361

Device End or Control End Up

YES

NO → To I-Cycles

YES

QH371

Setup to do a Head Seek Address Transfer. Sent to the Control Unit BBCCHH from the MPX Storage.

QH381

After Last Character is Transferred Wait for Status In. Check Status for Device End or Channel End; One or the Other Should be Received. If not go to General Stop. If DE or CE are up, Check for Unit Check. If UC Exist go to General Stop

QH381

DE, CE, or Have a Unit Check

NO

YES → General Stop

QH421

Readout Last Operation Code and Set Op Register Read
Op Register
0101 xxxx Read Load
0111 xxxx Read Move
0001 Sector
0010 Track
0101 Sector Overlay

QH421

Readout Compare and Module Protect Disable Byte. Check if Module Protect is to be Done. If it is Check Selected File Number Against a Fixed Number. If Numbers Match go on. If not go to a General Stop

QH421

Module Error Occured

YES → General Stop

NO

QH421

Setup the Op Register to Indicate Operation
0101 0000 - Read Load
0111 0000 - Read Move
Set an Indicator Bit (S-Register) to Remember if this is a Track Mode

QH421

Sector Overlay Op

NO

YES

QH241

Setup the Counter Used to Address Main Storage to Allow the Reading of the Sector Count

Chart 144 FW

QH341

Readout Selected File Number and Send the Address to the Control Unit. Wait for Address In, then Compare Address Out to Address In

QH341

Address Out Matches Address In

NO → General Stop

YES

Use B1 when Head Switching is Required

QH351

Setup a Search Command (31 or B1)

QH361

Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status

Status Should be Zero at this Time

QH361

Is Status Zero

NO

YES → 2

After Each Character is Sent, a Test for Status In is Done. If Status In Comes Up, the Unit Check Bit Should be On. The Unit Check Bit is Set if the Track is Flagged (Defective Track) or an Equal Address on a ID Search is not Found Before the Disc Passes the File Index Point Twice. This Causes Early Status and a Sense Command is Done.

QH361

Unit Check or Unit Exception On

YES → Sense Command

NO

QH361

Device End or Control Unit End Bits Up

YES → To I-Cycles

NO

QH371

Early Status

NO

YES

QH381

After Last Character is Sent, Wait for Status In. Check Status for Device End or Channel End, should Receive One or the Other. If not go to a General Stop. With DE or CE Up, Check for Unit Check Bit. If Unit Check Bit is On, a Sense Command must be Done to Find Out the Cause of the Unit Check.

QH381

Device End or Channel End Up

NO → General Stop

YES

QH391

Unit Check Bit On

YES

NO

QH391

Was an Equal Address Found on this Search; If not Repeat the Search Command

QH391

Equal Address Found

NO

YES → FU Chart 144

Send to the Control Unit CCHHR.

Chart 144 FY

QH341

Set Op Register Bit 7 to 1 (Sector Count 00)

QH341

Readout Selected File Number and Send the Address to the Control Unit. Wait for Address In, then Compare Address Out to Address In.

QH341

Address Out Matches Address In

YES

NO → General Stop

QH351

Setup Sense Command 04.

QH361

Store Command in MPX Storage and Issue the Command. Wait for Status In.

QH361

Send Service Out

QH511

Bring in Sense Bytes 0, 1, 2, and 3 One Byte at a Time and Store in MPX Storage. Test Selected Bits of Sense Byte 0, 1, and 2 for Error Condition and Set the File Branch Byte to Indicate the Error Condition. If Bit 6 of the Sense Byte 0 (Flagged Track) is On Set an Indicator Bit On.

QH521

Was Bit 6 of Byte 0 On

NO → FV Chart 144

YES

QH521

Set Op Register Bit 0 to a 1 and Bit 7 to a 0

QH341

Readout Selected File Unit Number and Send the Address to the Control Unit. Wait for Address In, then Compare Address Out to Address In.

QH341

Address Out Matches Address In

NO → General Stop

YES

QH351

Setup Command (16) to Read Record 0 Address

QH361

Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.

QH361

Is Status 00

YES

NO

QH361

It Unit Check or Unit Exception Is Up, Do a Sense Command. If UC and UE Are Down but Device End Is Up, the Read R0 Will Not Be Done. Otherwise Repeat Command

Status Should be 00

QH361

Unit Check or Unit Exception On

YES → Sense Command

NO

QH361

Device End Up

NO

YES

QH371

Read In the CCHH Values from Record R0 and Store in CPU Storage. Issue Command Out to Bring Status In.

QH381

Check Status for Either Device End or Channel End. If Either One is On, Check for Unit Check. If Not go to General Stop. If an Unit Check is Found do a Sense Command, If Not Setup to do a Full Seek to an Alternate Track Using CCHH from Record 0.

QH381

Device End or Channel End Up

NO → General Stop

YES

QH391

Unit Check Bit On

YES

NO

QH391

Setup to Develop a Full Seek Command to an Alternate Track.

QH341

Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In.

QH341

Address Out Matches Address In

NO → General Stop

YES

QH351

Setup a Full Seek Command 07.

QH361

Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.

QH361

Is Status 00

NO

YES

Status Should be Zero on the First Pass.

QH371

Send Bin Bin of 0000 to the Control Unit.

QH371

Send CCHH Values Read from Record R0 into CPU Storage to the Control Unit.

QH381

Wait for Status In. Check Status for Device End or Channel End, Go to General Stop if One or the Other is Not On. Check for an Unit Check, if Bit is On go to a General Stop. Otherwise Repeat the Seek Command and Status will be Non-Zero Because Device is Busy Seeking

QH381

No DE, CE, or Have a Unit Check

NO

YES → General Stop

Check for Unit Check or Unit Exception. If On Do a Sense Command. If Not, Test for Device End. DE Will Not Be Up Until the Seek Is Completed. Until the Device End Comes Up, Repeat the Seek Command

QH361

Unit Check or Unit Exception On

YES → Sense Command

NO

QH361

Device End Up

NO

YES

QH361

Insure Bit 4 of the Op Register is 0

QH341

Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In

QH341

Address Out Matches Address In

NO → General Stop

YES

QH351

Setup a Search Comaand 31.

QH361

Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.

QH361

Is Status 00

YES → 2

NO

If Unit Check or Unit Exception Bit Is On Do a Sense Command. Otherwise Repeat Search Command

Unit Check or Unit Exception On

YES → Sense Command

NO

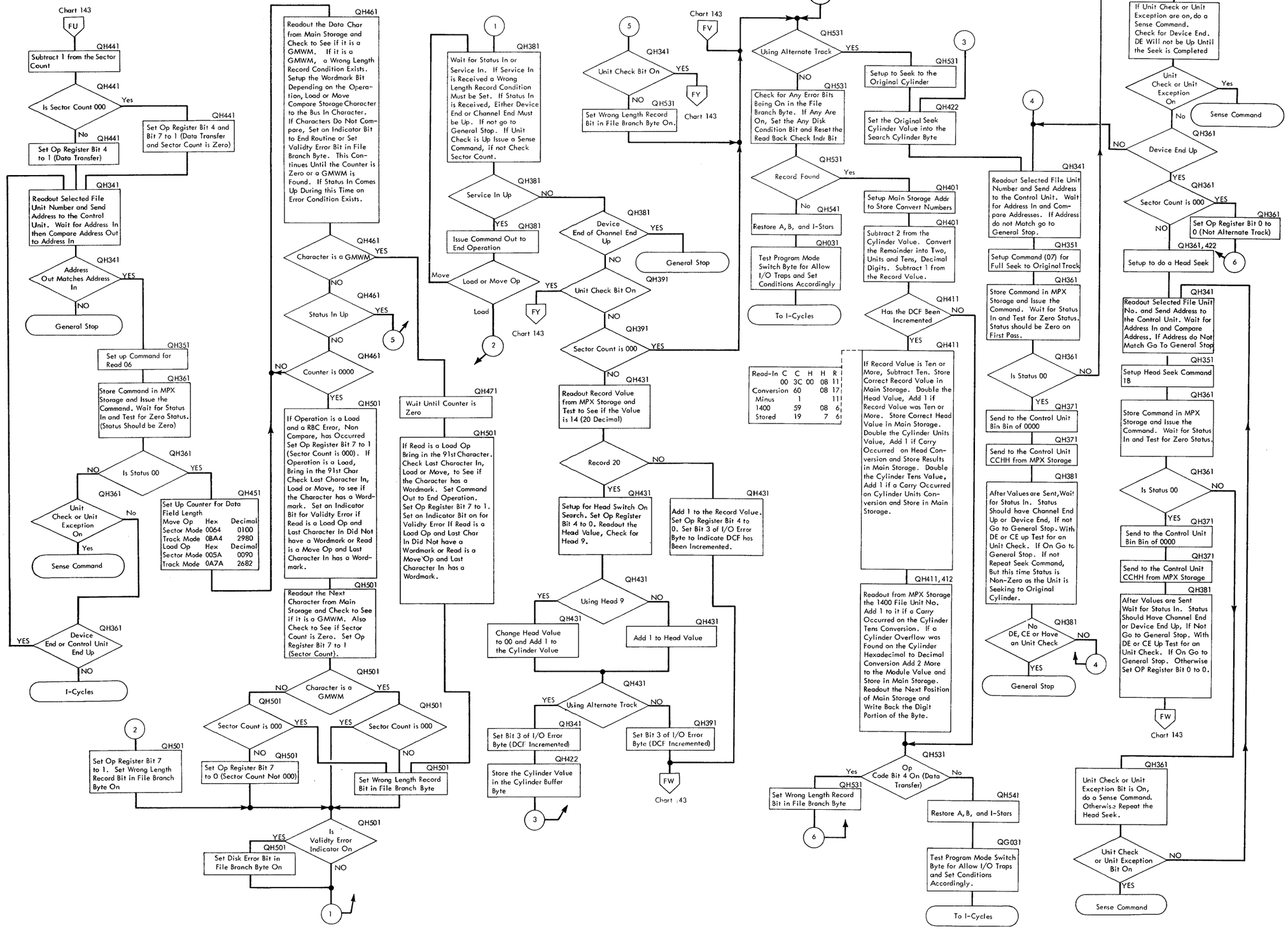


Chart 143
FU
QH441
Subtract 1 from the Sector Count
QH441
Is Sector Count 000
Yes
No
QH441
Set Op Register Bit 4 and Bit 7 to 1 (Data Transfer and Sector Count is Zero)
QH441
Set Op Register Bit 4 to 1 (Data Transfer)
QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In then Compare Address Out to Address In
QH341
Address Out Matches Address In
YES
NO
General Stop
QH351
Set up Command for Read 06
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status. (Status Should be Zero)
QH361
Is Status 00
NO
YES
QH361
Unit Check or Unit Exception On
No
Yes
Sense Command
QH361
Device End or Control Unit End Up
YES
NO
I-Cycles
QH451
Set Up Counter for Data Field Length
Move Op Hex 0064 Decimal 0100
Sector Mode 0064 0100
Track Mode 08A4 2980
Load Op Hex 005A Decimal 0090
Sector Mode 005A 0090
Track Mode 0A7A 2682
QH461
Readout the Data Char from Main Storage and Check to See if it is a GMWM. If it is a GMWM, a Wrong Length Record Condition Exists. Setup the Wordmark Bit Depending on the Operation, Load or Move Compare Storage Character to the Bus In Character. If Characters Do Not Compare, Set an Indicator Bit to End Routine or Set Validty Error Bit in File Branch Byte. This Continues Until the Counter is Zero or a GMWM is Found. If Status In Comes Up During this Time on Error Condition Exists.
QH461
Character is a GMWM
YES
NO
QH461
Status In Up
YES
NO
5
QH461
Counter is 0000
NO
YES
QH501
If Operation is a Load and a RBC Error, Non Compare, has Occurred Set Op Register Bit 7 to 1 (Sector Count is 000). If Operation is a Load, Bring in the 91st Char Check Last Character In, Load or Move, to see if the Character has a Wordmark. Set an Indicator Bit for Validity Error if Read is a Load Op and Last Character In Did Not have a Wordmark or Read is a Move Op and Last Character In has a Wordmark.
QH501
Readout the Next Character from Main Storage and Check to See if it is a GMWM. Also Check to See if Sector Count is Zero. Set Op Register Bit 7 to 1 (Sector Count).
QH501
Character is a GMWM
NO
YES
QH501
Sector Count is 000
YES
NO
QH501
Sector Count is 000
YES
NO
2
QH501
Set Op Register Bit 7 to 1. Set Wrong Length Record Bit in File Branch Byte On
QH501
Set Op Register Bit 7 to 0 (Sector Count Not 000)
QH501
Set Wrong Length Record Bit in File Branch Byte
QH501
Is Validty Error Indicator On
YES
NO
QH501
Set Disk Error Bit in File Branch Byte On
1
1
QH381
Wait for Status In or Service In. If Service In is Received a Wrong Length Record Condition Must be Set. If Status In is Received, Either Device End or Channel End Must be Up. If not go to General Stop. If Unit Check is Up Issue a Sense Command, if not Check Sector Count.
QH381
Service In Up
NO
YES
QH381
Issue Command Out to End Operation
Move
Load or Move Op
Load
YES
2
QH471
Wait Until Counter is Zero
QH501
If Read is a Load Op Bring in the 91st Character. Check Last Character In, Load or Move, to See if the Character has a Wordmark. Set Command Out to End Operation. Set Op Register Bit 7 to 1. Set an Indicator Bit on for Validty Error If Read is a Load Op and Last Char In Did Not have a Wordmark or Read is a Move Op and Last Character In has a Wordmark.
5
QH341
Unit Check Bit On
YES
NO
FY
Chart 143
QH531
Set Wrong Length Record Bit in File Branch Byte On.
Chart 143
FV
QH381
Device End of Channel End Up
YES
NO
General Stop
QH391
Unit Check Bit On
YES
NO
FY
Chart 143
QH391
Sector Count is 000
YES
NO
QH431
Readout Record Value from MPX Storage and Test to See if the Value is 14 (20 Decimal)
Record 20
NO
YES
QH431
Setup for Head Switch On Search. Set Op Register Bit 4 to 0. Readout the Head Value, Check for Head 9.
QH431
Add 1 to the Record Value. Set Op Register Bit 4 to 0. Set Bit 3 of I/O Error Byte to Indicate DCF has Been Incremented.
QH431
Using Head 9
YES
NO
QH431
Change Head Value to 00 and Add 1 to the Cylinder Value
QH431
Add 1 to Head Value
QH431
Using Alternate Track
YES
NO
QH341
Set Bit 3 of I/O Error Byte (DCF Incremented)
QH391
Set Bit 3 of I/O Error Byte (DCF Incremented)
QH422
Store the Cylinder Value in the Cylinder Buffer Byte
FW
Chart 143
3
6
QH531
Using Alternate Track
YES
NO
QH531
Check for Any Error Bits Being On in the File Branch Byte. If Any Are On, Set the Any Disk Condition Bit and Reset the Read Back Check Indr Bit
QH531
Record Found
Yes
No
QH541
Restore A, B, and I-Stars
QH031
Test Program Mode Switch Byte for Allow I/O Traps and Set Conditions Accordingly
To I-Cycles
Read-In C C H H R
00 3C 00 08 11
Conversion 60 08 17
Minus 1 11
1400 59 08 6
Stored 19 7 6
3
QH531
Setup to Seek to the Original Cylinder
QH422
Set the Original Seek Cylinder Value into the Search Cylinder Byte
QH401
Setup Main Storage Addr to Store Convert Numbers
QH401
Subtract 2 from the Cylinder Value. Convert the Remainder into Two, Units and Tens, Decimal Digits. Subtract 1 from the Record Value.
QH411
Has the DCF Been Incremented
NO
YES
QH411
If Record Value is Ten or More, Subtract Ten. Store Correct Record Value in Main Storage. Double the Head Value, Add 1 if Record Value was Ten or More. Store Correct Head Value in Main Storage. Double the Cylinder Units Value, Add 1 if Carry Occurred on Head Conversion and Store Results in Main Storage. Double the Cylinder Tens Value, Add 1 if a Carry Occurred on Cylinder Units Conversion and Store in Main Storage.
QH411,412
Readout from MPX Storage the 1400 File Unit No. Add 1 to it if a Carry Occurred on the Cylinder Tens Conversion. If a Cylinder Overflow was Found on the Cylinder Hexadecimal to Decimal Conversion Add 2 More to the Module Value and Store in Main Storage. Readout the Next Position of Main Storage and Write Back the Digit Portion of the Byte.
QH531
Op Code Bit 4 On (Data Transfer)
Yes
No
QH531
Set Wrong Length Record Bit in File Branch Byte
6
QH541
Restore A, B, and I-Stars
QG031
Test Program Mode Switch Byte for Allow I/O Traps and Set Conditions Accordingly.
To I-Cycles
4
QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In and Compare Addresses. If Address do not Match go to General Stop.
QH351
Setup Command (07) for Full Seek to Original Track
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status. Status should be Zero on First Pass.
QH361
Is Status 00
NO
YES
QH371
Send to the Control Unit Bin Bin of 0000
QH371
Send to the Control Unit CCHH from MPX Storage
QH381
After Values are Sent, Wait for Status In. Status Should have Channel End Up or Device End, If not Go to General Stop. With DE or CE up Test for an Unit Check. If On Go to General Stop. If not Repeat Seek Command, But this time Status is Non-Zero as the Unit is Seeking to Original Cylinder.
No
QH381
DE, CE or Have an Unit Check
NO
YES
4
General Stop
QH361
If Unit Check or Unit Exception are on, do a Sense Command. Check for Device End. DE Will not be Up Until the Seek is Completed
Unit Check or Unit Exception On
Yes
No
Sense Command
QH361
Device End Up
NO
YES
QH361
Sector Count is 000
YES
NO
QH361
Set Op Register Bit 0 to 0 (Not Alternate Track)
QH361, 422
Setup to do a Head Seek
6
QH341
Readout Selected File Unit No. and Send Address to the Control Unit. Wait for Address In and Compare Address. If Address do Not Match Go To General Stop
QH351
Setup Head Seek Command 1B
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.
QH361
Is Status 00
NO
YES
QH371
Send to the Control Unit Bin Bin of 0000
QH371
Send to the Control Unit CCHH from MPX Storage
QH381
After Values are Sent Wait for Status In. Status Should Have Channel End or Device End Up, If Not Go to General Stop. With DE or CE Up Test for an Unit Check. If On Go to General Stop. Otherwise Set OP Register Bit 0 to 0.
FW
Chart 143
QH361
Unit Check or Unit Exception Bit is On, do a Sense Command. Otherwise Repeat the Head Seek.
Unit Check or Unit Exception Bit On
NO
YES
Sense Command

DCF 1400-1311
*/N $D_2 D_3 D_4 D_5 D_6$
$S_1 S_2 S_3$
Example
*051976 XXXX
Changed to 2311 Format by Using Table Look Up to Select Module 2, Cylinder 59, Head 8, and Record 16. This can be Determined by Dividing $D_2 D_3 D_4 D_5$ by 2 and Using the Remainder with D_6 for the Record. Add 1 to the Cylinder and Record Values for 2311 Format.
End Result Is:

	1400	2311
Module	4	2
Cylinder	59+1	3C
Head	08	08
Record	16+1	11

Start

QH301
Store I-Star, Setup the Op Register for Write In Move or Load Mode.
0000 0000 Load
0010 0000 Move

Op Register
0000 XXXX Write Load
0010 XXXX Write Move
0111 Low
1000 Equal
1001 High

QH301, 311
Readout the Disk Control Field and Change from a 1400-1311 Format to a 2311 Format. Change the Op Register to Indicate High, Equal, or Low Scan

QH341
Send Address Out. If Status is Received, Set the File Branch Byte for Busy and Any Disk Condition. Restore the A, B, and I-Stars and Return to I-Cycles. If Status isn't Received, Wait for Operational In and Address In, Check for Correct Address

QH341
Address Out Matches Address In
No → General Stop
YES QH351
Setup a Head Seek (18) Command

QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.

QH361
Is Status 00
Yes QH371
Setup to do a Head Seek Address Transfer. Sent to the Control Unit Bin. Bin of 0000 and CCHH from MPX Storage.

QH381
After Last Character is Transferred Wait for S Status In, Check Status for Device End or Channel End. One or the Other Should be Received If Not go to a General Stop. If DE or CE are Up, Check for a Unit Check. If UC Exists go to a General Stop.

QH381
No Device End, Channel End or Have a Unit Check NO
Yes → General Stop

QH361
If Status Has a Unit Check or Unit Exception Bit On, Do a Sense Command. If UC or UE Bits are not On, Check for Device End or Control Unit End. If Either DE or CUE are Up, Retry the Command. Otherwise Set the File Branch Byte to Busy and Any Disk Condition, then Restore the A, B, and I-Stars and Return to I-Cycles

QH361
Unit Check or Unit Exception On
No → Yes → Sense Command

QH361
Device End or Control Unit End
Yes → No → I-Cycles

QH421
Store the Operation Code (Op Register) in MPX Storage to Remember what was Done Last. Since this is a Write Op Set the Read Back Check Interlock On.

QH421
Readout Compare and Module Protect Disable Byte. Check if Module Protect is to be Done. If it is, Check Selected File Number Against a Fixed Number. If Numbers Match Go On, If not Go to a General Stop.

QH421
Module Error Occurred
Yes → General Stop
NO

QH421
Setup the Op Register to Indicate a Scan Operation (Bit 5) and to do a Read (Bit 3).
0001 0100 Read Load
0011 0100 Read Move
Set a Byte in Storage to Remember What Type of Scan.
Low - 0000 0000
Equal - 0001 0000
High - 0010 0000

QH421
The Operation has Changed to a Read so it Resets the Read Back Check Indicator

QH521
Insure the Op Register Bit 7 is 0

FW Chart 146

QH341
Readout Selected File Number and Send the Address to the Control Unit. Wait for Address In, then Compare Address Out to Address In

QH341
Address Out Matches Address In
No → General Stop
Yes QH351
Setup a Search Command (31)

QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status

After Each Character is Sent, a Test for Status In is Done. If Status In Comes Up, the Unit Check Bit Should be On. The Unit Check Bit is Set if the Track is Flagged (Defective Track) or an Equal Address on an ID Search is not Found Before the Disc Passes the File Index Point Twice. This Causes Early Status and a Sense Command is Done.

Status Should be Zero at This Time

QH361
Is Status Zero
No → Yes

2

QH361
Unit Check or Unit Exception On
Yes → Sense Command
No

QH361
Device End or Control Unit End Bits Up
Yes
No → To I-Cycles

QH371
Send to the Control Unit CCHHR.

QH371
Early Status
No
Yes FY

QH381
After Last Character is Sent, Wait for Status In. Check Status for Device End or Channel End, Should Receive One or the Other. If Not go to a General Stop. With Device End or Channel End Up Check for Unit Check, If on a Sense Command must be Done to Find Out the Cause of the Unit Check

QH381
Device End or Channel End Up
No → General Stop
Yes

QH391
Unit Check Bit On
Yes
No QH391
Was an Equal Address Found on this Search. If not Repeat the Search Command.

QH391
Equal Address Found
No
Yes FU

Chart 146

FY Chart 146

QH341
Set Op Register Bit 7 to 1 (Sector Count 00)

QH341
Readout Selected File Number and Send the Address to the Control Unit. Wait for Address In, Then Compare Address Out to Address In

QH341
Address Out Matches Address In
Yes
No → General Stop

QH351
Setup a Sense Command 04

QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In.

QH361
Send Service Out

QH511
Bring in Sense Bytes 0, 1, 2, and 3 One Byte at a Time and Store in MPX Storage. Test Selected Bits of Sense Byte 0, 1, and 2 for Error Condition and Set the File Branch Byte to Indicate the Error Condition. If Bit 6 of the Sense Byte 0 (Flagged Track) is On Set an Indicator Bit On.

QH521
Was Bit 6 of Byte 0 on
No → FV Chart 146
Yes QH521
Set Op Register Bit 0 to a 1 and Bit 7 to a 0

QH341
Readout Selected File Unit Number and Send the Address to the Control Unit. Wait for Address In, then Compare Address Out to Address In.

QH341
Address Out Matches Address In
No → General Stop
Yes QH351
Setup Command (16) to Read Record 0 Address

QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status

QH361
Is Status 00
Yes
No QH361
If Unit Check or Unit Exception Is Up, Do a Sense Command. If UC and UE Are Down but Device End Is Up, the Read R0 Will Not Be Done. Otherwise Repeat Command

Status should be 00

QH361
Unit Check or Unit Exception On
Yes → Sense Command
No

QH361
Device End Up
Yes
No

QH371
Read In the CCHH Values from Record R0 and Store in CPU Storage. Issue Command Out to Bring Status In.

QH381
Check Status for Either Device End or Channel End. If Either One is On, Check for Unit Check. If not Go to General Stop. If an Unit Check is Found do a Sense Command, If not Set up to do a Full Seek to an Alternate Track Using CCHH from Record 0.

QH381
Device End or Channel End Up
No → General Stop
Yes QH391

QH391
Unit Check Bit On
Yes
No QH391
Setup to Develop a Full Seek Command to an Alternate Track.

QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In.

QH341
Address Out Matches Address In
No → General Stop
Yes QH351
Setup a Full Seek Command 07.

QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status.

QH361
Is Status 00
No
Yes QH371
Status should be Zero on the First Pass.

Send Bin Bin of 0000 to the Control Unit.

QH371
Send CCHH Values Read from Record R0 into CPU Storage to the Control Unit.

QH381
Wait for Status In. Check Status for Device End or Channel End. Go to General Stop if One or the Other is Not on. Check for an Unit Check, if Bit is On go to a General Stop. Otherwise Repeat the Seek Command and Status will be Non-Zero Because Device is Busy Seeking.

QH381
No Device End, Channel End, or Have an Unit Check
Yes → General Stop

QH361
Check for Unit Check or Unit Exception. If On Do a Sense Command. If Not Test for Device End. DE Will Not Be Up until the Seek Is Completed. Until the Device End Comes Up Repeat Seek Command

QH361
Unit Check or Unit Exception On
Yes → Sense Command
No

QH361
Device End Up
No
Yes
Insure Bit 4 of the Op Register is 0.

QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In.

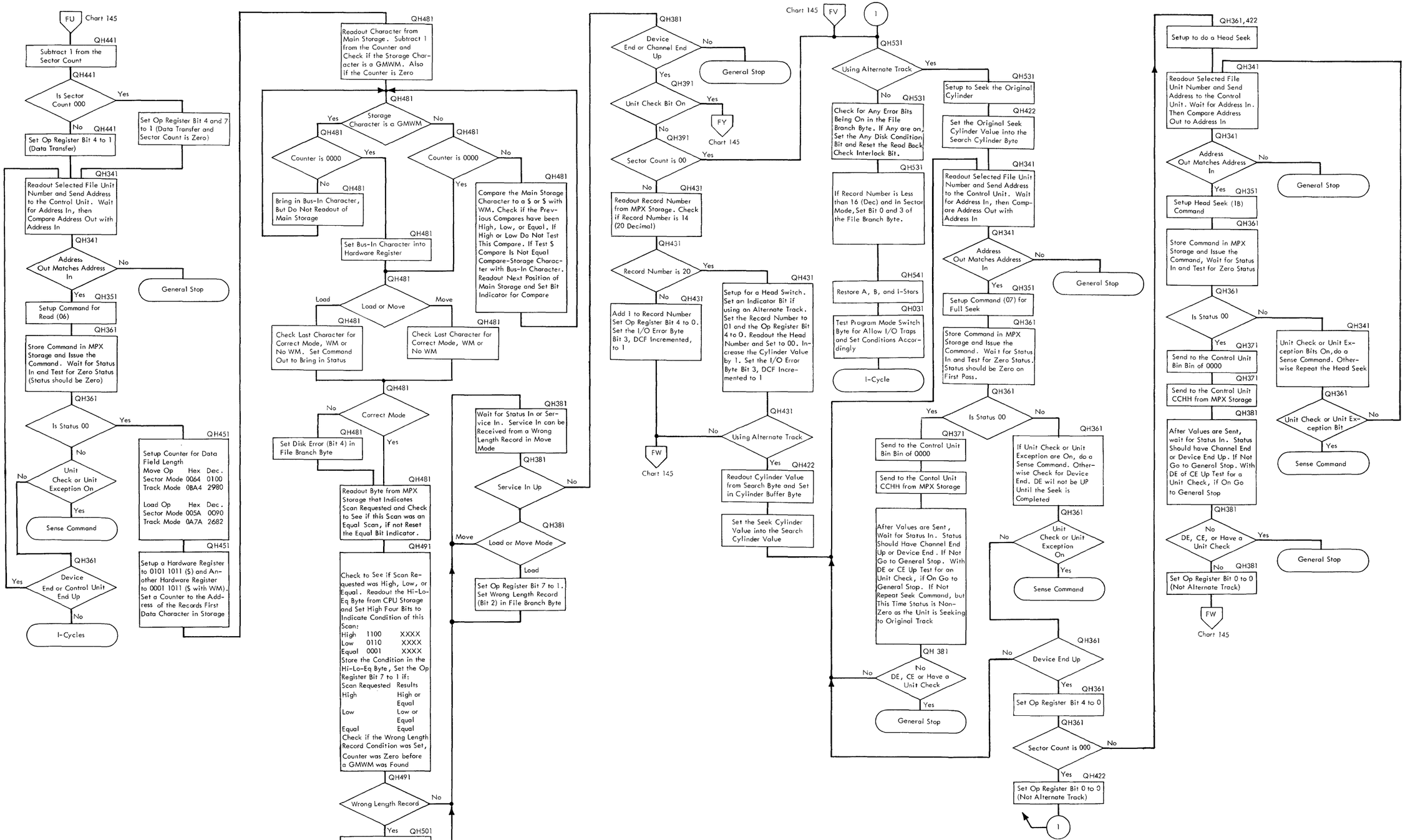
QH341
Address Out Matches Address In
No → General Stop
Yes QH351
Setup a Search Command 31

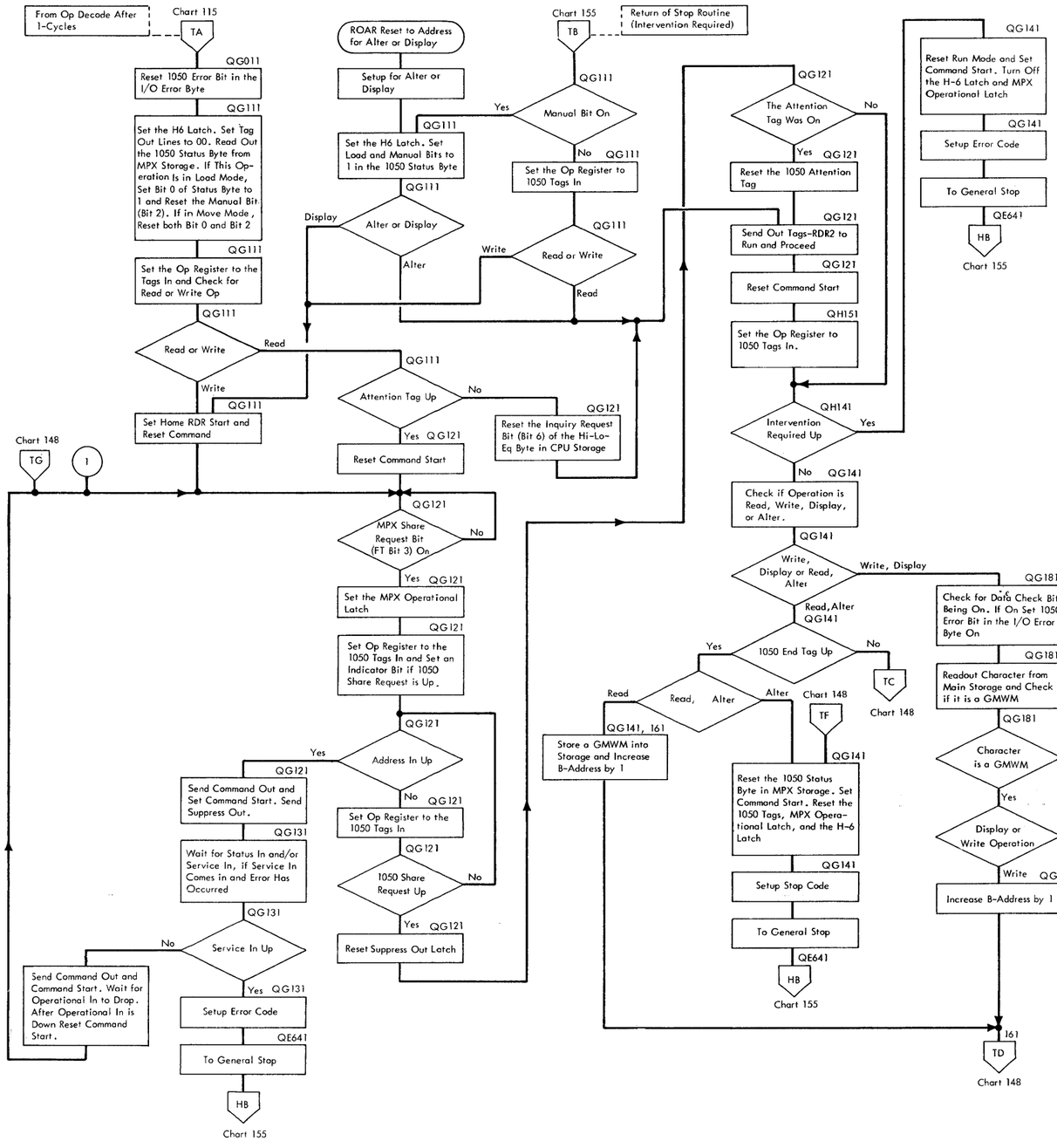
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status

QH361
Is Status 00
Yes → 2
No

If Unit Check or Unit Exception Bit is On Restore the A, B, and I-Stars and go to I-Cycles. Othewise Repeat Search Command.

Unit Check or Unit Exception On
Yes → Sense Command
No


FU Chart 145
QH441
Subtract 1 from the Sector Count
QH441
Is Sector Count 000
Yes
No
Set Op Register Bit 4 and 7 to 1 (Data Transfer and Sector Count is Zero)
QH441
Set Op Register Bit 4 to 1 (Data Transfer)
QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In
QH341
Address Out Matches Address In
No
General Stop
Yes
QH351
Setup Command for Read (06)
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status (Status should be Zero)
QH361
Is Status 00
Yes
No
QH451
Setup Counter for Data Field Length
Move Op Hex Dec.
Sector Mode 0064 0100
Track Mode 0BA4 2980
Load Op Hex Dec.
Sector Mode 005A 0090
Track Mode 0A7A 2682
QH451
Setup a Hardware Register to 0101 1011 ($) and Another Hardware Register to 0001 1011 ($ with WM). Set a Counter to the Address of the Records First Data Character in Storage
Unit Check or Unit Exception On
No
Yes
Sense Command
QH361
Device End or Control Unit End Up
Yes
No
I-Cycles
QH481
Readout Character from Main Storage. Subtract 1 from the Counter and Check if the Storage Character is a GMWM. Also if the Counter is Zero
QH481
Storage Character is a GMWM
Yes
No
QH481
Counter is 0000
Yes
No
QH481
Bring in Bus-In Character, But Do Not Readout of Main Storage
QH481
Counter is 0000
No
Yes
QH481
Compare the Main Storage Character to a $ or $ with WM. Check if the Previous Compares have been High, Low, or Equal. If High or Low Do Not Test This Compare. If Test $ Compare Is Not Equal Compare-Storage Character with Bus-In Character. Readout Next Position of Main Storage and Set Bit Indicator for Compare
QH481
Set Bus-In Character into Hardware Register
QH481
Load or Move
Load
Move
QH481
Check Last Character for Correct Mode, WM or No WM. Set Command Out to Bring in Status
QH481
Check Last Character for Correct Mode, WM or No WM
QH481
Correct Mode
No
Yes
QH481
Set Disk Error (Bit 4) in File Branch Byte
QH481
Readout Byte from MPX Storage that Indicates Scan Requested and Check to See if this Scan was an Equal Scan, if not Reset the Equal Bit Indicator.
QH491
Check to See if Scan Requested was High, Low, or Equal. Readout the Hi-Lo-Eq Byte from CPU Storage and Set High Four Bits to Indicate Condition of this Scan:
High 1100 XXXX
Low 0110 XXXX
Equal 0001 XXXX
Store the Condition in the Hi-Lo-Eq Byte, Set the Op Register Bit 7 to 1 if:
Scan Requested Results
High High or Equal
Low Low or Equal
Equal Equal
Check if the Wrong Length Record Condition was Set, Counter was Zero before a GMWM was Found
QH491
Wrong Length Record
No
Yes
QH501
Set Op Register Bit 7 to 1. Set Wrong Length Record (Bit 2) in File Branch Byte
QH381
Wait for Status In or Service In. Service In can be Received from a Wrong Length Record in Move Mode
QH381
Service In Up
No
QH381
Load or Move Mode
Move
Load
Set Op Register Bit 7 to 1. Set Wrong Length Record (Bit 2) in File Branch Byte
QH381
Device End or Channel End Up
No
General Stop
Yes
QH391
Unit Check Bit On
Yes
FY
Chart 145
No
QH391
Sector Count is 00
Yes
No
QH431
Readout Record Number from MPX Storage. Check if Record Number is 14 (20 Decimal)
QH431
Record Number is 20
Yes
No
QH431
Add 1 to Record Number Set Op Register Bit 4 to 0. Set the I/O Error Byte Bit 3, DCF Incremented, to 1
QH431
Setup for a Head Switch. Set an Indicator Bit if using an Alternate Track. Set the Record Number to 01 and the Op Register Bit 4 to 0. Readout the Head Number and Set to 00. Increase the Cylinder Value by 1. Set the I/O Error Byte Bit 3, DCF Incremented to 1
QH431
Using Alternate Track
No
Yes
FW
Chart 145
QH422
Readout Cylinder Value from Search Byte and Set in Cylinder Buffer Byte
Set the Seek Cylinder Value into the Search Cylinder Value
Chart 145 FV
1
QH531
Using Alternate Track
Yes
No
QH531
Setup to Seek the Original Cylinder
QH422
Set the Original Seek Cylinder Value into the Search Cylinder Byte
QH531
Check for Any Error Bits Being On in the File Branch Byte. If Any are on, Set the Any Disk Condition Bit and Reset the Read Back Check Interlock Bit.
QH531
If Record Number is Less than 16 (Dec) and in Sector Mode, Set Bit 0 and 3 of the File Branch Byte.
QH541
Restore A, B, and I-Stars
QH031
Test Program Mode Switch Byte for Allow I/O Traps and Set Conditions Accordingly
I-Cycle
QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In, then Compare Address Out with Address In
QH341
Address Out Matches Address In
No
General Stop
Yes
QH351
Setup Command (07) for Full Seek
QH361
Store Command in MPX Storage and Issue the Command. Wait for Status In and Test for Zero Status. Status should be Zero on First Pass.
QH361
Is Status 00
Yes
No
QH371
Send to the Control Unit Bin Bin of 0000
Send to the Contol Unit CCHH from MPX Storage
After Values are Sent, Wait for Status In. Status Should Have Channel End Up or Device End. If Not Go to General Stop. With DE or CE Up Test for an Unit Check, if On Go to General Stop. If Not Repeat Seek Command, but This Time Status is Non-Zero as the Unit is Seeking to Original Track
QH 381
No DE, CE or Have a Unit Check
No
Yes
General Stop
QH361
If Unit Check or Unit Exception are On, do a Sense Command. Otherwise Check for Device End. DE wil not be UP Until the Seek is Completed
QH361
Unit Check or Unit Exception On
No
Yes
Sense Command
QH361
Device End Up
No
Yes
QH361
Set Op Register Bit 4 to 0
QH361
Sector Count is 000
No
Yes
QH422
Set Op Register Bit 0 to 0 (Not Alternate Track)
1
QH361,422
Setup to do a Head Seek
QH341
Readout Selected File Unit Number and Send Address to the Control Unit. Wait for Address In. Then Compare Address Out to Address In
QH341
Address Out Matches Address In
No
General Stop
Yes
QH351
Setup Head Seek (18) Command
QH361
Store Command in MPX Storage and Issue the Command, Wait for Status In and Test for Zero Status
QH361
Is Status 00
No
Yes
QH341
Unit Check or Unit Exception Bits On, do a Sense Command. Otherwise Repeat the Head Seek
QH361
Unit Check or Unit Exception Bit
No
Yes
Sense Command
QH371
Send to the Control Unit Bin Bin of 0000
QH371
Send to the Control Unit CCHH from MPX Storage
QH381
After Values are Sent, wait for Status In. Status Should have Channel End or Device End Up. If Not Go to General Stop. With DE of CE Up Test for a Unit Check, if On Go to General Stop
QH381
No DE, CE, or Have a Unit Check
Yes
General Stop
No
QH381
Set Op Register Bit 0 to 0 (Not Alternate Track)
FW
Chart 145



	00				01				10				11			
	00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
0000					SP	&	—						?	!	‡	0
0001							/						A	J	'	1
0010													B	K	S	2
0011													C	L	T	3
0100													D	M	U	4
0101													E	N	V	5
0110													F	O	W	6
0111													G	P	X	7
1000													H	Q	Y	8
1001													I	R	Z	9
1010								ъ								
1011					•	$	,	#								
1100					¤	*	%	@								
1101					[	]	⁓	:								
1110					<	;	\	>								
1111					‡	△	╪	⌐								

Chart 1. 2030 Bit Format

	00				10				01				11			
	00	01	10	11	00	01	10	11	00	01	10	11	10	01	10	11
0000					SP	&	—									0
0001							/		A	J						1
0010									B	K	S					2
0011									C	L	T					3
0100									D	M	U					4
0101	HT	NL							E	N	V		(	▼	)	5
0110									F	O	W		b	=	∨	6
0111									G	P	X		?	!	‡	7
1000									H	Q	Y					8
1001									I	R	Z					9
1010								ъ								
1011					•	$	,	#								
1100					¤	*	%	@								
1101					[	]	⁓	:								
1110					<	;	\	>								
1111					‡	△	╪	⌐								

Chart 2. Bit Format form and to 1050

TC Chart 147

QG141

Check to See if the Cancel or Data Check Bits are On. If Data Check is On Set Bus-In Character into the Op Register. If Either Bit is on Set Bit 4 (1050 Error) an in the I/O Error Byte.

QG141

Cancel Bit On — No / Yes

QG141

Check Bits 0 and 1 of Bus-In Character to determine what Quadrant the Character is In. See Chart 2.

QG141

Quadrant 0, 1 or 2, 3 — 0, 1 / 2, 3

QG141

Quadrant 0 or 1 — 1 / 0

If Bus In Character is
05 Setup 4D - E
15 Setup 5D - J

QG151

Check to see if the Low 4 Bits of the Bus-In are Other than 0101, also if Bit 2 of the Character is a 1. If Either Condition Exists, Set the 1050 Error Bit (Bit 4) of the I/O Error Byte.

QG151

Alter or Read — Alter / Read

QG151

Set Op Register to 1050 Tags

QG151

Display Routine — Yes / No

QG151

Is the Attention Tag Up — No / Yes

QG151

Reset MPX Operational Latch

TG Chart 147

Chart 147 TE

1

Quadrant 2 or 3 — 2 / 3

QG141

Set Bit 1 of Character to 1 (Quadrant 3 Chart 1)

TF Chart 147

QG141

Alter or Read — Read / Alter

QG141

Change Character to a Blank (40)

QG141

Numeric Character — Yes / No

QG151

Low 4 Bits of Character are 0111 — Yes / No

Set 4 Low Bits of Character to 0000. See Chart 1.

See Chart 2 Quadrant 3

1

QG151

Low 4 Bits of Character are 0101 — Yes / No

QG171

Low 4 Bits of Character are 0110 — Yes / No

Set 1050 Error Bit (Bit 4) of the I/O Error Byte in MPX Storage.

QG171

Check Bits 2 and 3 of Character In, Change Character to be Stored to--

Chart 2	Chart 1
&-C6 to	00
=-D6 to	#-7B

If Bits 2 and 3 are 10 (Chart 2, Quadrant 3) Set an Indication if Last Character was a Wordmark.

QG171

Bits 2 and 3 are 00, 01 or 10 — 00,01 / 10

Character is a Wordmark Do Not Increase B-Address

Check Bits 2 and 3 of Character In. Change Character to be stored to:

Chart 2	Chart 1
Quadrant 3	Quandrant 2
Bits 2 and 3	
00 -)	to ¤ - 4C
01 - ▼	to @ - 7C
10 - (	to % - 6C

2

2

QG151

Readout Position of Main Storage Character is to Enter

QG161

Storage Character is a GMWM — Yes / No

QG161

Alter or Read — Alter / Read

QG161

Check to See if the Character in Storage Has a Word Mark. If in Move Mode and Character Has a WM, add a WM to the Character to be Stored. If no WM Insure Bit 1 is Set to 1 (No WM). If in Load Mode and Character Has a WM, Check if Last Character In Was a WM Indication. If Last Character In was a WM Set a WM into this character. If not Insure Bit 1 is a 1.

QG161

Set 1050 Error Bit in I/O Error Byte in MPX Storage.

Chart 147 TD

QG161

Restore the 1050 Status Byte in MPX Storage, Set Command Start, Send Out Carrier Return and Line Feed and Reset 1050. Reset the MPX Operational Latch and Set the Invalid A-Address Indication.

QG031

Check Mode Switch Byte to see if I/O Traps Are Allowed. Set up H5, H6 and Command Start as Required.

QG161

Reset Last-Character-In-Was-a-WM Indication and Store the Converted Character into Main Storage. Increase B-Address by 1.

QG161

Was the Cancel Tag On — No / Yes

1

I-Cycles
Branch on Inquiry
* Q

QE421, QF681,701

Decode the d-Modifier

QF702

d-modifier is * or Q — * / Q

QF701

Readout the I/O Error Byte in MPX Storage and Test Bit 4 (1050 Error)

QF681

Bit 4 is a 1 — No / Yes

QF661

Invalid A-Address Indication On — Yes / No

QF651

To Stop

HA Chart 155

QF701

Set the Op Register to 1050 Tag In and Check if the Attention Bit is On.

QF661

Attention Bit On — NO / Yes

QF661

Check to See if Advance Program Feature is Installed Set 1 and B-Star Accordingly

Interrupt Exist — Yes / No

QE001

To Interrupt Decode

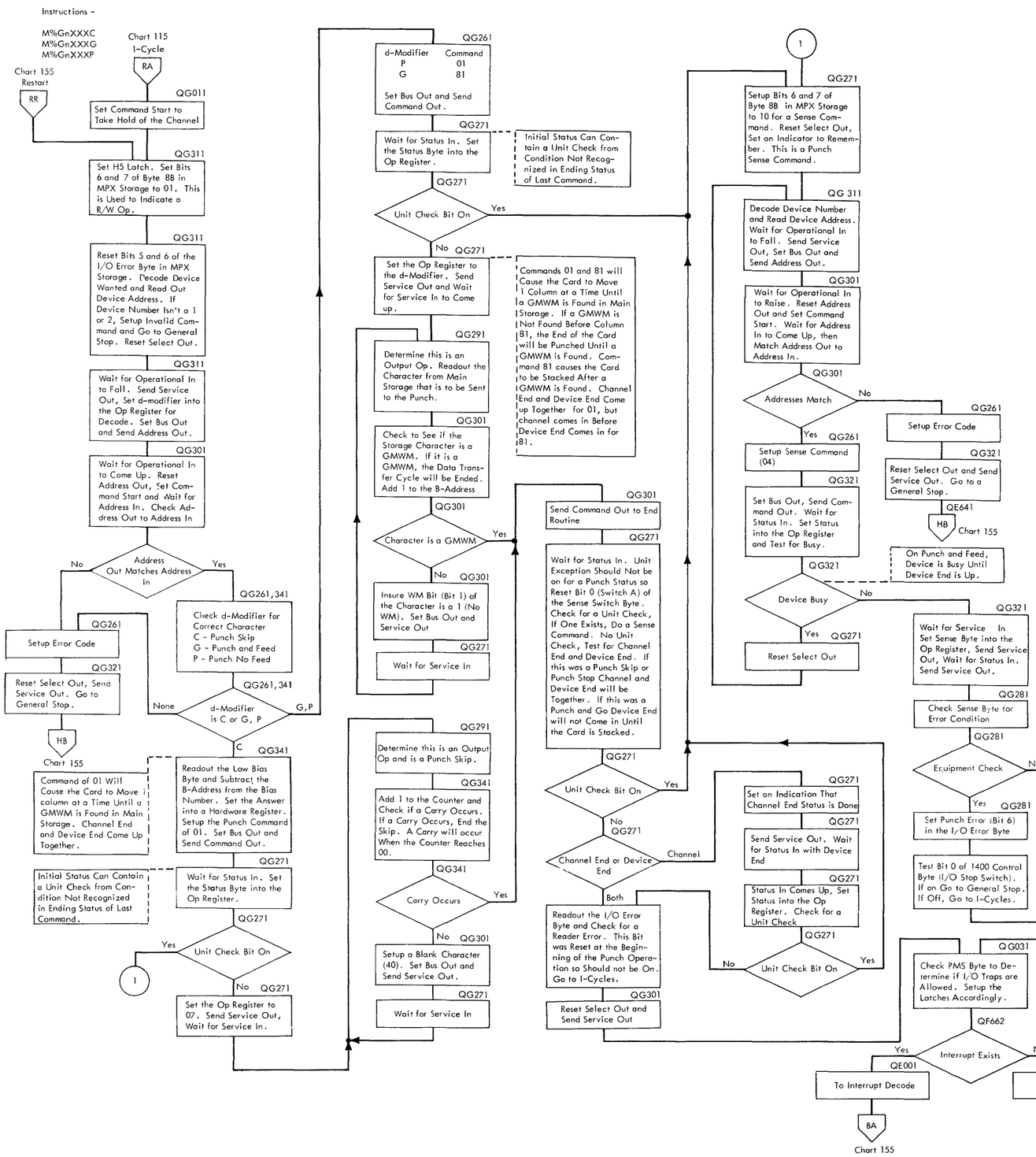
BA Chart 155

QE001

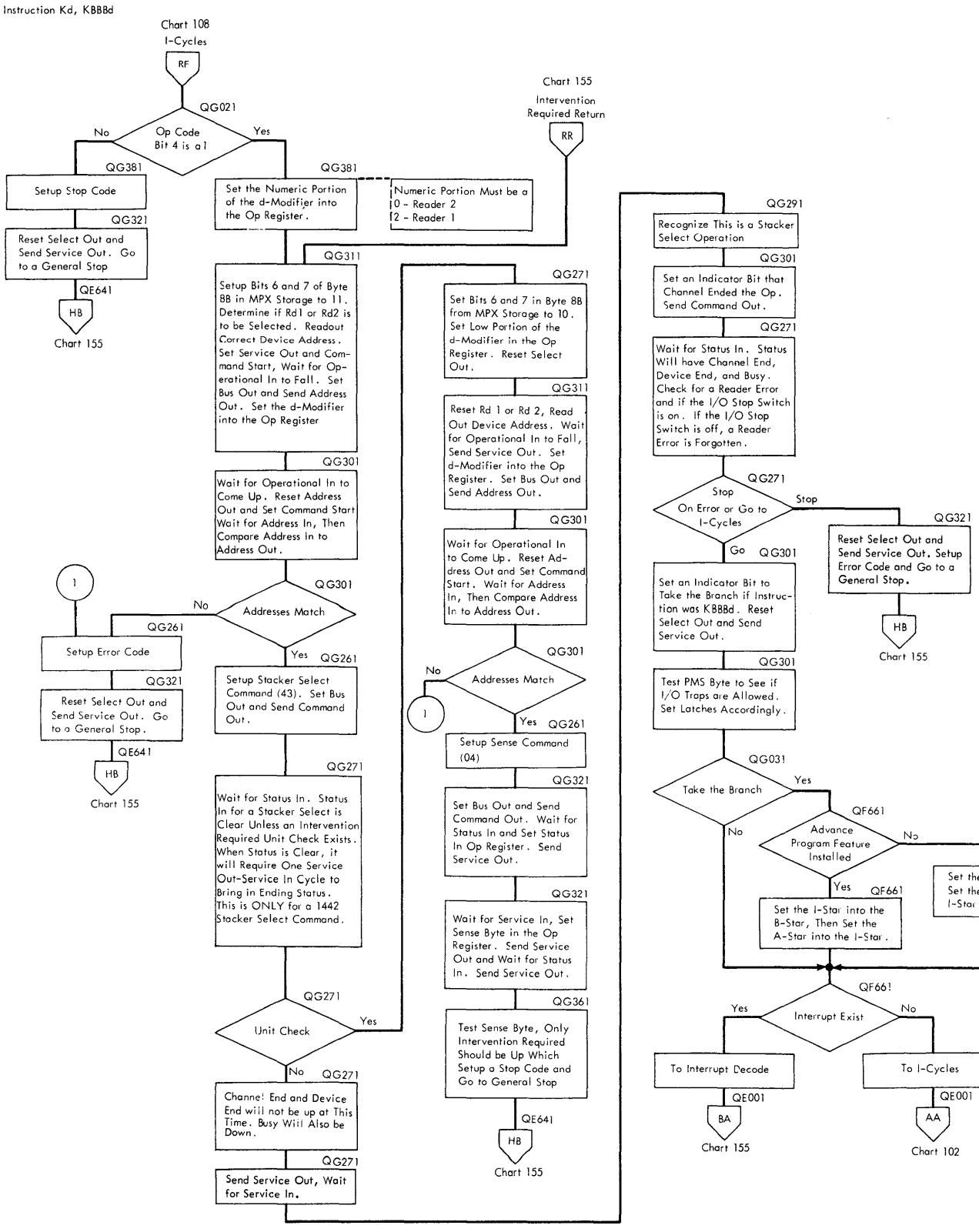
To I-Cycle

AA Chart 102

I-Cycles
Restart
RR
Chart 155
RA
Chart 115
QG011
Set Command Start to Take Hold of the Channel
QG311
Set H-5 Latch. Set Bits 6 and 7 of Byte 8B in MPX Storage to 01. This is Used to Indicate a R/W Op
QG311
Reset Bits 5 and 6 of the I/O Error Byte in MPX Storage. Decode Device Wanted and Read Out Device Address. If Device Number isn't 1 or 2 Setup Invalid Command and Go to General Stop. Reset Select Out.
QG311
Wait for Operational In to Fall. Send Service Out, Set d-Modifier into the Op Register for Decode. Set Bus Out and Send Address Out
QG301
Wait for Operational In to Come Up, Reset Address Out and Wait for Address In. Check Address Out to Address In.
QG301
Address Out Matches Address In
No
Yes
QG261
Check the d-Modifier to Insure it is an R. If Not Go to General Stop
QG261
d-Modifier OK
No
Yes
QG261
Set Up Read Command (12) and Issue Command. Reset Last Card Indication (Bit 0 of Sense Switch Byte).
QG261
Setup Error Code
QG321
Reset Select Out, Send Service Out. Go to General Stop
HB
Chart 155
QG271
Wait for Status In. Set the Status Byte into the Op Register
Intial Status Can Contain Unit Check from Condition Not Recognized in Ending Status of Last Command. Also Device End Can Be Up if this Is the First Command After the Device is Made Ready
QG271
Unit Check Bit On
Yes
No
2
QG271
Device End Up
No
Yes
QG271
Reset Select Out. Setup to Reselect the Device. This Clears Status
QG271
Send Service Out and Set the Op Register to the d-Modifier
QG271
Wait for Service In
QG291
Readout the Position In Main Storage that the Character from the Reader will Enter. Check the Character to See if it is a GMWM or if it Contains a Wordmark. If it is a GMWM the Read In of Data is Finished. If the Character from Storage Does Not Contain a WM Set an Indicator Bit
QG291
Character is a GMWM
Yes
No
QG301
Increase B-Address by 1. Set an Indicator Bit for Channel-Ended-the-Read and Send Command Out. Channel End Will Come Up Before Device End
1
QG291
Send Service Out and Check which Quadrant the Bus-In Character is In. Do a Table Lookup of Character to Determine if it is a Valid 1400 Character
QG291
Quadrant 0,2 or 1,3
1,3
0,2
QG291
Check if Character from Table has Bit 1 On. If Bit 1 Is On, a Further Test Is Made to Determine if the Bus In Character is a MLP Character
QG291
Table Character Has Bit 1 On
Yes
No
QG291
Test if the Bus In Character is a MLP Character
QG291
MLP Character
Yes
No
QG291
Change Bus In Character to a Character with the 9,8 Bits Removed.
Example:
Bus In Store
00111001 11110001
00111010 11110010
00111011 11110011
QG291
Readout I/O Error Byte and Set Bit 5 (Reader Error) On
If Bus-In Character was an Invalid 1400 Character, Leave the Character that was in Main Storage There
QG301
If Storage Character Had a Wordmark, Store the Bus In or Converted MLP Character with a WM in Main Storage
Increase the B-Address By 1
1
1
QG271
Wait for Status In or Service In. Service -In wil Come Up Until the Last Column Has been Read. After the Card Has been Read Status In will Come In with Channel End and Device End Both Up
QG271
Service In or Status In
Service In
Status In
QG271
Check for Unit Exception Bit being On..If On, Set Bit 0 (Switch A) of the Sense Switch Byte for Last Card Condition.
QG271
Check for a Unit Check, if On Setup for a Sense Command
QG271
Unit Check Bit On
No
Yes
2
QG271
Check for Channel End and Device End being Up. Both will be Up for a 80 Column Read. For a Read Less than 80 Columns Only Channel End will be Up
QG271
Channel End or Device End
Channel
Both
QG271
Set an Indicator Bit that Channel End Status is Done
QG271
Send Service Out. Set Op Register to the d-Modifier. Wait for Status In with Device End
QG271
Status In Comes Up; Set Status in the Op Register. Do Not Check for Unit Exception or the Last Card Indication will be Reset. Check for an Unit Check
3
QG271,281
Readout the 81st Position of the Read In Area and Check for a GMWM. If It Isn't a GMWM go to a Error Stop.
QG281
Character is a GMWM
Yes
No
QG281
Setup Error Code
QG321
Reset Select Out and Send Service Out. Go to a General Stop
QE641
HB
Chart 155
3
QG271
Unit Check Bit On
Yes
No
QG271
Check for Channel End and Device End. Device End is Up and an Indicator Bit for Channel Ended is On
QG271
Check the I/O Error Byte for a Reader Error, If On Check the I/O Stop Switch Bit. If Stop Switch is On and an Error is Indicated Setup an Error Code, Otherwise Return to 1-Cycles
QG271
Reader Error and I/O Stop Switch On
Yes
No
QG271
Setup Error Code
QG281,321
Reset Select Out and Send Service Out. Go to a General Stop
QE641
HB
Chart 155
QG301
Reset Select Out and Send Service Out
QG031
Check PMS Byte to Determine if I/O Traps are Allowed. Setup Latch Accordingly.
QF661
Interrupt Exist
Yes
No
To Interrupt Decode
BA
Chart 155
To I-Cycles
AA
Chart 102
2
QG271
Setup Bits 6 and 7 of Byte 8B in MPX Storage to 10 for a Sense Command. Reset Select Out. Set an Indicator Bit to Remember This Is a Read Sense Command
QG311
Decode Device Number and Read Device Address. Wait for Operational to Fall. Send Service Out, Set Bus Out and Send Address Out
QG301
Wait for Operational In to Raise. Reset Address Out and Set Command Start. Wait for Address In to Come Up, then Match Address Out to Address In.
QG301
Addresses Match
No
Yes
QG261
Setup Error Code
QG321
Reset Select Out and Send Service Out. Go to a General Stop.
HB
Chart 155
QG261
Setup Sense Command (04)
QG321
Set Bus Out, Send Command Out. Wait for Status In. Set Status into the Op Register and Test for Busy
QG321
Device Busy
No
Yes QG271
Reset Select Out
If Channel Ended the Read Device is Busy Until Device End Time
QG321
Wait for Service In. Set Sense Byte into the Op Register. Send Service Out, Wait for Status In. Send Service Out
QG281
Check Sense Byte for Error Conditions
QG281
Equipment Check
No
Yes QG281
Set Reader Error (Bit 5) in the I/O Error Byte
QG281
Test Bit 0 of 1400 Control Byte (I/O Stop Switch). If On Go to General Stop. If Off Go to I-Cycles
QG281
I/O Stop Switch On
Yes
No QG301
Reset Select Out and Send Service Out
QG281
Intervention Required On
No
Yes
QG281
If Either Data Check or Overrun Condition Exists Set Reader Error (Bit 5) in I/O Error Byte.
QG281
Setup Conditions for Intervention Required Stop.
QG321
Reset Select Out and Send Service Out. Go to a General Stop.
HB
Chart 155


Instructions -
M%GnXXXC
M%GnXXXG
M%GnXXXP
Chart 115
1-Cycle
RA
Chart 155
Restart
RR
QG011
Set Command Start to Take Hold of the Channel
QG311
Set H5 Latch. Set Bits 6 and 7 of Byte 8B in MPX Storage to 01. This is Used to Indicate a R/W Op.
QG311
Reset Bits 5 and 6 of the I/O Error Byte in MPX Storage. Decode Device Wanted and Read Out Device Address. If Device Number Isn't a 1 or 2, Setup Invalid Command and Go to General Stop. Reset Select Out.
QG311
Wait for Operational In to Fall. Send Service Out, Set d-modifier into the Op Register for Decode. Set Bus Out and Send Address Out.
QG301
Wait for Operational In to Come Up. Reset Address Out, Set Command Start and Wait for Address In. Check Address Out to Address In
Address Out Matches Address In
No
Yes
QG261
Setup Error Code
QG321
Reset Select Out, Send Service Out. Go to General Stop.
HB
Chart 155
Command of 01 Will Cause the Card to Move 1 column at a Time Until a GMWM is Found in Main Storage. Channel End and Device End Come Up Together.
Initial Status Can Contain a Unit Check from Condition Not Recognized in Ending Status of Last Command.
QG261,341
Check d-Modifier for Correct Character
C - Punch Skip
G - Punch and Feed
P - Punch No Feed
QG261,341
d-Modifier is C or G, P
None
G,P
C
QG341
Readout the Low Bias Byte and Subtract the B-Address from the Bias Number. Set the Answer into a Hardware Register. Setup the Punch Command of 01. Set Bus Out and Send Command Out.
QG271
Wait for Status In. Set the Status Byte into the Op Register.
QG271
Unit Check Bit On
Yes
No
1
QG271
Set the Op Register to 07. Send Service Out, Wait for Service In.
QG261
d-Modifier P G
Command 01 81
Set Bus Out and Send Command Out.
QG271
Wait for Status In. Set the Status Byte into the Op Register.
Initial Status Can Contain a Unit Check from Condition Not Recognized in Ending Status of Last Command.
QG271
Unit Check Bit On
Yes
No
QG271
Set the Op Register to the d-Modifier. Send Service Out and Wait for Service In to Come up.
Commands 01 and 81 will Cause the Card to Move 1 Column at a Time Until a GMWM is Found in Main Storage. If a GMWM is Not Found Before Column 81, the End of the Card will be Punched Until a GMWM is Found. Command 81 causes the Card to be Stacked After a GMWM is Found. Channel End and Device End Come up Together for 01, but channel comes in Before Device End Comes in for 81.
QG291
Determine this is an Output Op. Readout the Character from Main Storage that is to be Sent to the Punch.
QG301
Check to See if the Storage Character is a GMWM. If it is a GMWM, the Data Transfer Cycle will be Ended. Add 1 to the B-Address
QG301
Character is a GMWM
Yes
No
QG301
Insure WM Bit (Bit 1) of the Character is a 1 (No WM). Set Bus Out and Service Out
QG271
Wait for Service In
QG291
Determine this is an Output Op and is a Punch Skip.
QG341
Add 1 to the Counter and Check if a Carry Occurs. If a Carry Occurs, End the Skip. A Carry will occur When the Counter Reaches 00.
QG341
Carry Occurs
Yes
No
QG301
Setup a Blank Character (40). Set Bus Out and Send Service Out.
QG271
Wait for Service In
QG301
Send Command Out to End Routine
QG271
Wait for Status In. Unit Exception Should Not be on for a Punch Status so Reset Bit 0 (Switch A) of the Sense Switch Byte. Check for a Unit Check, If One Exists, Do a Sense Command. No Unit Check, Test for Channel End and Device End. If this was a Punch Skip or Punch Stop Channel and Device End will be Together. If this was a Punch and Go Device End will not Come in Until the Card is Stacked.
QG271
Unit Check Bit On
Yes
No
QG271
Channel End or Device End
Channel
Both
Readout the I/O Error Byte and Check for a Reader Error. This Bit was Reset at the Beginning of the Punch Operation so Should not be On. Go to 1-Cycles.
QG301
Reset Select Out and Send Service Out
1
QG271
Setup Bits 6 and 7 of Byte 8B in MPX Storage to 10 for a Sense Command. Reset Select Out, Set an Indicator to Remember. This is a Punch Sense Command.
QG 311
Decode Device Number and Read Device Address. Wait for Operational In to Fall. Send Service Out, Set Bus Out and Send Address Out.
QG301
Wait for Operational In to Raise. Reset Address Out and Set Command Start. Wait for Address In to Come Up, then Match Address Out to Address In.
QG301
Addresses Match
No
Yes
QG261
Setup Error Code
QG321
Reset Select Out and Send Service Out. Go to a General Stop.
QE641
HB
Chart 155
QG261
Setup Sense Command (04)
QG321
Set Bus Out, Send Command Out. Wait for Status In. Set Status into the Op Register and Test for Busy.
On Punch and Feed, Device is Busy Until Device End is Up.
QG321
Device Busy
No
Yes
QG271
Reset Select Out
QG321
Wait for Service In Set Sense Byte into the Op Register, Send Service Out, Wait for Status In. Send Service Out.
QG281
Check Sense Byte for Error Condition
QG281
Equipment Check
No
Yes
QG281
Set Punch Error (Bit 6) in the I/O Error Byte
Test Bit 0 of 1400 Control Byte (I/O Stop Switch). If on Go to General Stop. If Off, Go to 1-Cycles.
QG281
Intervention Required On
Yes
No
QG281
Setup Conditions for Intervention Required Stop
QG321
Reset Select Out and Send Service Out. Go to a General Stop
HB
Chart 155
QG281
I/O Stop Switch On
Yes
No
QG301
Reset Select Out and Send Service Out.
QG271
Set an Indication That Channel End Status is Done
QG271
Send Service Out. Wait for Status In with Device End
QG271
Status In Comes Up, Set Status into the Op Register. Check for a Unit Check
QG271
Unit Check Bit On
No
Yes
QG031
Check PMS Byte to Determine if I/O Traps are Allowed. Setup the Latches Accordingly.
QF662
Interrupt Exists
Yes
No
QE001
To Interrupt Decode
BA
Chart 155
QE001
To 1-Cycles
AA
Chart 102

Instruction Kd, KBBBd



Instruction
BXXX9 - Channel 9
BXXX12 - Channel 12
BXXX* - Punch Error
BXXX! - Printer Error
BXXXP - Printer Busy
I-Cycles
QG021
Program Mode Switch On
NO
YES
To Program Mode Switching
CM
Chart 156
QG021
Printer or Punch
Printer
Punch
QG331
Branch or Error Op
NO
YES
QG331
Branch On Printer Busy
YES
NO
QG331
Set d-Modifier into the Op Register
QG331
Testing for Print or Punch Error
Printer
Punch
QG331
Branch on Channel 9 or 12
12
9
QG331
Check if Printer Error (Bit 7) of I/O Error Byte is on . Set Op Register to Indicate the Condition. Reset Bit 7 of the I/O Error Byte.
QG331
Check if Punch Error (Bit 6) of I/O Error Byte. Set Op Register to Indicate Condition. Reset Bit 6 of the I/O Error Byte.
QG331
Readout Byte 8B from MPX Storage. Check Bit 0 to See if Channel 9 Has Been Sensed. Set Op Register to Indicate Condition. Reset Bit 0 of Byte 8B.
QG331
Readout Byte 8B from MPX Storage. Check Bit 2 to See if Channel 12 Has Been Sensed. Set Op Register to Indicate Condition. Reset Bit 2 of Byte 8B.
QG331
Set an Indicator Bit if the Branch is to be Taken
QG031
Check PMS Byte to See If I/O Traps Are Allowed, Set Latches Accordingly.
QG031
Take the Branch
NO
NO
YES
YES
QF661
Advance Program Feature Installed
NO
YES
QF661
Set B-Star to 0000
QF661
Set the Contents of I-Star into the B-Star
QF661
Set the Contents of A-Star into the I-Star
QF661
Interrupt Exists
YES
NO
QE001
To Interrupt Decode
QE001
To I-Cycle
BA
Chart 155
AA
Chart 102
Instruction-
BXXXA Last Card
BXXX? Reader Error
I-Cycles
QF681
Readout Sense Switch Byte from CPU Storage
QF681
Branch On Last Card or Reader Error
Reader Error
Last Card
QF681
Test Bit 0 of Sense Switch Byte, If on Take the Branch
QF681
Readout the I/O Error Byte from MPX Storage and Check Bit 5 (Reader Error). If on Take the Branch
QF681
Take the Branch
NO
YES
QG311
Set Bits 4, 5, 6 and 7 of Byte 8B in MPX Storage to 0000.
Bit 6 and 7 at 00 Indicate a Test I/O Command
QG311
Readout Printer Address. Wait Until Operational In is Down, Send Service Out. Set the d-Modifier into the Op Register. Set Bus Out and Send Address Out.
QG301
Wait for Operational In to Come Up. Reset Addr. Out and Set Command Start. Wait for Address In, Then Compare Address Out to Address In
QG301
Addresses Match
No
Yes
QG261
Setup Error Code
QG321
Reset Select Out and Send Service Out. Go to General Stop
QE641
HB
Chart 155
QG261
Set up a Test I/O Command (00).
QG321
Set Bus Out and Send Command Out. Wait for Status In. Check if Unit Check or Unit Exception Bits are On in Status, Reset Select Out.
QG321
Unit Check or Unit Exception Bit On
NO
YES
QG321
Send Service Out and Set Command Start
QG331
Check to See if the Busy Bit (Bit 3) of the Status Byte is On. If it is Set an Indicator So the Branch Will Be Taken
QG351
Bit 7 (Unit Exception) On
NO
YES
QG351
Set Channel 12 Indicator (Bit 2) of Byte 8B in MPX Storage
QG351
Bit 6 (Unit Check) On
NO
YES
QG351
Set Bit 6 and 7 of Byte 8B in MPX Storage to 10 (Sense Command).
QG351
Reset Select Out.
QG311
Readout Printer Address, Wait for Operational In to Fail, Send Service Out. Set the d-Modifier into the Op Register. Set Bus Out and Send Address Out
QG301
Wait for Operational In to come up. Reset Address Out and Set Command Start. Wait for Address In, Compare Address Out to Address In.
QG301
Addresses Match
NO
YES
QG261
Do Test I/O or Sense Command
Test I/O
Sense
QG261
Setup the Sense Command (04).
QG321
Set Bus Out and Send Command Out. Wait for Status In and Set Status into the Op Register. Send Service Out.
QG321
Wait for Service In, Set Sense Byte in the Op Register. Send Service Out and Wait for Status In. Send Service Out.
QG361
Equipment Check Bit On
NO
YES
QG361
Set Printer Error (Bit 7) in the I/O Error Byte
QG331
Channel 9 Was Sensed During Last Op
NO
YES
QG331
Set Bit 0 of Byte 8B in MPX Storage
QG331
Set Indicator Bit so the Branch Will Not Be Taken

Instruction - M%Y1BBBW
M%Y1BBBS.

Chart 155 RR

Chart 115 PA

QG011 Set Command Start to Take Control of Channel

QG311 Set the H5 Latch. Read-out Byte 8B from MPX Storage and Test Bit 3 to See if the Printer Has a NPL Bar Installed. Set an Indicator Bit to 1 if it is an NPL Bar. Set Bits 6 and 7 to 01 to Indicate an R/W Operation

QG311 Readout the I/O Error Byte and Reset Bit 7 (Printer Error).

QG311 Readout Printer Address. Wait Until Operational In is Down, Send Service Out Set the d-Modifier into the Op Register, Set Bus Out and Send Address Out.

QG301 Wait for Operational In to Come Up. Reset Address Out and Set Command Start. Wait for Address In, Then Compare Address Out to Address In.

QG301 Addresses Match

No → QG261 Setup Error Code → QG321 Reset Select Out and Send Service Out. Go to General Stop → QE641 → HB Chart 155

Yes → QG261 Decode the d-Modifier for a W or S (W-Print and Space and S-Print and No Space). If Not a W or S, Set an Error Code and Go to a General Stop. Check Byte 8B of MPX Storage to See if a Forms After Command Has Been Stored. Set up the Command.

d-Modifier	Command
S	01
W	09

If Form After Bit was Set, the Command will be XXXXX001 Depending on the Form Movement Required. Set Bus Out and Send Command Out. Check to See if the Form Portion of the Command is a Skip (Bit 0 of Command will be a 1).

QG261 Command Contains a Skip

Yes → QG361 Check to See if the Skip is to Channel 1, 9, or 12. Reset or Set Bits 0 and 2 of Byte 8B in MPX Storage According to the Skip.

Skip	Reset	Set
1	0 and 2	--
9	--	0
12	--	2

No → QG351 Wait for Status In

This Status will Be from the Last Printer Command

Device Is Busy Until Device End Comes Up at End of Carriage Motion

QG351 Wait for Status In

QG351 Set Status into the Op Register

QG351 Busy

Yes → QG351 Either Bit 6 or 7 On

Yes → QG351 Bit 7 (Unit Exception On)

Yes → QG351 Set Channel 12 Indicator (Bit 2) of Byte 8B in MPX Storage.

QG351 Bit 6 (Unit Check) On

Yes → QG351 Set Bit 6 and 7 of Byte 8B in MPX Storage to 10 (Sense Command)

QG351 Reset Select Out

QG311 Readout Printer Address, Wait for Operational In to Fall, Send Service Out. Set the d-Modifier into the Op Register. Set Bus Out and Send Address Out

QG301 Wait for Operational In to Come Up. Reset Address Out and Set Command Start. Wait for Address In, Then Compare Address Out to Address In

QG301 Addresses Match

Yes → QG261 Do R/W or Sense Command

R/W → Setup the Sense Command (04)

QG321 Set Bus Out and Send Command Out. Wait for Status In and Set Status into the Op Register. Send Service Out and Test for Busy Condition.

QG321 Busy

Yes → QG321 Reset Select Out

No → Device is Busy if Sense Command Was Entered from Channel End Status Until Device End Time

Sense → QG261 Setup Error Code → QG321 Reset Select Out and Send Service Out. Go to General Stop. → QG641 → HB Chart 155

No → QG361 Setup Stop Code → QG321 Reset Select Out and Send Service Out. Go to General Stop. → HB Chart 155

No → QG351 Either Bit 6 or 7 On

Yes → 2

No → 1

No → QG351 Channel End Up

Yes → QG351 Either Bit 6 or 7 On

No → 2

No → QG351 Either Bit 6 or 7 On

Yes → Set Remote Start Bit in PMS Byte (9F - LS)

QG321 Wait for Service In, Set Sense Byte in the Op Register. Send Service Out and Wait for Status In. Send Service Out.

QG361 Channel 9 Was Sensed During Last Op

Yes → QG361 Set Bit 0 of Byte 8B in MPX Storage

No → QG361 Equipment Check Bit On

Yes → QG361 Set Printer Error (Bit 7) in the I/O Error Byte

QG361 Intervention Required Bit On

Yes → 2

No → QG361 I/O Stop Switch On

Yes → 1

No → QG361 Set Bit 6 and 7 of Byte 8B in MPX Storage to 01. Reset Select Out.

QG361,311 Check Bit 3 of Byte 8B to see if a NPL Bar is in the Printer, if it is Set an Indicator Bit

QG311 Readout Printer Address. Wait for Operational In to Fall, Send Service Out. Set the d-Modifier into the Op Register, Set Bus Out and Send Address Out.

QG301 Wait for Operational In to Come Up. Reset Address Out and Set Command Start. Wait for Address In, then Compare Address Out to Address In.

QG301 Addresses Match

No → QG261 Setup Error Code → QG321 Reset Select Out and Send Service Out. Go to General Stop. → QE641 → HB Chart 155

Yes → QG261 Decode the d-Modifier for a W or S. If Not a W or S, Setup an Error Code and Go to a General Stop. Check Byte 8B of MPX Storage to See if a Forms After Command Has Been Stored. Setup the Command.

d-Modifier	Command
S	01
W	09

If Form After Bit was Set, the Command will be XXXXX001 Depending On the Form Movement Required. Set Bus Out and Send Command Out. Check to see if the Form Portion of the Command is a Skip (Bit 0 of the Command will be a 1).

QG261 Command Contains a Skip

Yes → QG361 Check to See if the Skip is to Channel 1, 9, or 12. Reset or Set Bits 0 and 2 of Byte 8B in MPX Storage According to the Skip

Skip	Reset	Set
1	0 and 2	--
9	--	0
12	--	2

No → QG351 Wait for Status In

QG351 Reset Byte 8B of MPX Storage Leaving Bits 0, 2, and 3 as is. Send Service Out, Wait for Service In.

QG371 Readout Character From Main Storage and Check if it is a GMWM

QG371 Character Is a GMWM

No → QG371 Increase B-Address By 1

QG371 NPL Bar Installed

No → Modify Character Bit Format for Table Lookup

QG371 Test to See if the Character is in Quadrant 1 or 3. Do a Table Lookup on the Characters in Quadrant 1, Also in Row 0 of Quadrant 3. Set Bus Out and Send Service Out

QG351 Wait for Status In or Service In. Status will Come In when the Print Buffer is Full. Status will Contain Channel End and Possibly Unit Check

QG351 Status in Up

No → 2

Yes → QG351 Unit Check Bit On

Yes → 1

No → QG301 Reset Select Out and Send Service Out

QG031 Readout PMS Byte From MPX Storage and Check if I/O Traps are Allowed. Set Latches Accordingly

QF661 Interrupt Exists

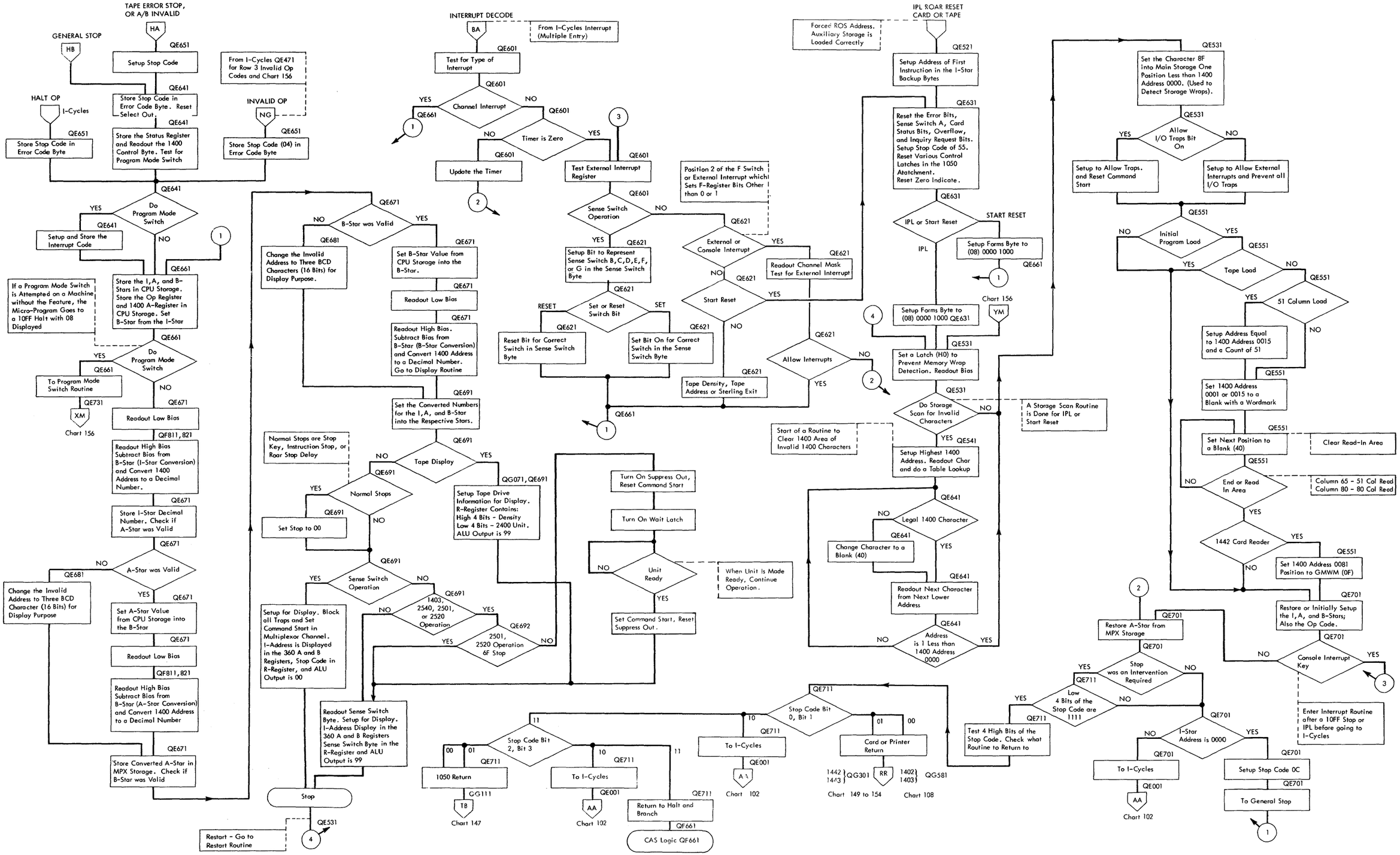
Yes → QE001 To Decode Interrupt → BA Chart 155

No → QE001 To I-Cycles → AA Chart 102

Yes → QG371 Increase B-Address by 1. Send Command Out.

QG351 Wait for Status In, Status will Contain Channel End and Possibly Unit Check.

Instruction - Fd
RF Chart 108
RR Chart 155
QG301
Read Out Byte 8B of MPX Storage
QG021
Op Code Bit 4 is a 1
No
Yes
QG381
Setup Stop Code
QG321
Reset Select Out and Send Service Out. Go to a General Stop
QE641
HB
Chart 155
QG381
Set the d-Modifier into the Op Register. Change the d-Modifier to a BCD Character and Test Zone Bits.
Zone Bits Form Op
No Zone Skip Immed.
A Zone Space After
B Zone Space Immed.
BA Zone Skip After
QG381
If d-Modifier is a Blank (00) Return to I-Cycles
QG381
d-Modifier is a Blank
Yes
No
QG381
Setup the Correct Forms Command Depending on the Operation and Form Movement.
Operation Command
Immediate XXXXX011
After XXXXX001
Store the Command in the Temporary Forms Byte in MPX Storage. Set the H5 Latch to 1. Set Bits 6 and 7 of Byte 8B in MPX Storage to 11. Reset Bit 1
QG381
Skip/Space Immediate or After
After
Immediate
QG381
Set Bit 1 of Byte 8B in MPX Storage to a 1 (Indicate a Forms After Command).
QG301
Reset Select Out and Send Service Out.
4
QG311
Readout Printer Address Wait for Operational In to Come Down, Send Service Out. Set Bus Out and Send Address Out. Set the d-Modifier into the Op Register.
QG301
Wait for Operational In to Come Up. Reset Address Out and Set Command Start. Wait for Address In, Then Compare Address Out to Address In.
QG301
Addresses Match
No
Yes
QG261
Setup Stop Code
QG321
Reset Select Out and Send Service Out. Go to a General Stop
QE641
HB
Chart 155
QG761
Readout the Temporary Form Byte. Set Bus Out and Send Command Out. Check if This is a Skip Command (Bit 0 of the Command is a 1 for a Skip)
QG261
Command is a Skip
No
Yes
QG361
Check to See if the Skip is to Channel 1, 9, or 12. Reset or Set Bits 0 and 2 of Byte 8B in MPX Storage According to the Skip.
Skip Reset Set
1 0 and 2 -
9 - 0
12 - 2
QG351
Wait for Status In. This Status Will Be from the Last Printer Command. Check Bits 6 and 7 to See If Either One is On. Set Status in the Op Register.
QG351
Either Bit 6 or 7 on
Yes
No
3
QG351
Bit 7 (Unit Exception) On
No
Yes
QG351
Set Channel 12 Indicator Bit 2 of Byte 8B in MPX Storage
QG351
Bit 6 (Unit Check On)
No
Yes
2
QG351
Set Bit 6 and 7 of Byte 8B in MPX Storage to 10 (Sense Command).
QG351
Reset Select Out
QG311
Readout Printer Address Wait for Operational In to Fall, Send Service Out. Set the d-Modifier into the Op Register. Set Bus Out and Send Address Out.
QG301
Wait for Operational In to Come Up. Reset Address Out and Set Command Start. Wait for Address In, then Compare Address Out to Address In.
QG301
Addresses Match.
No
Yes
1
QG351
Check if Device is Busy. Device Is Busy Until Device End Comes Up at End of Carriage Motion.
QG351
Device Busy
Yes
No
QG351
Reset Byte 8B of MPX Storage Leaving Bits 0, 2, and 3 as is, Send Service Out, Wait for Status In.
QG351
Unit Check Bit On
Yes
No
QG301
Reset Select Out, Send Service Out.
QG031
Check PMS Byte to See if I/O Traps are Allowed. Set the Latches Accordingly.
QF661
Interrupt Exist
No
Yes
QE001
To Interrupt Decode
BA
Chart 155
QE001
To I-Cycles
AA
Chart 102
1
QG261
Do Control or Sense Command
Control
Sense
QG261
Setup the Sense Command (04).
QG321
Set Bus Out and Send Command Out. Wait for Status In and Set Status into the Op Register. Send Service Out and Test for Busy Condition.
Device Should Not be Busy at This Time
QG321
Device Busy
Yes
No
QG321
Reset Select Out.
2
QG321
Wait for Service In, Set Sense Byte in the Op Register. Send Service Out and Wait for Status In. Send Service Out.
QG361
Channel 9 Was Sensed During Last Comand
Yes
No
QG361
Set Bit 0 of Byte 8B in MPX Storage.
Equipment Check Bit On
No
Yes
QG361
Set Printer Error (Bit 7) in the I/O Error Byte.
QG361
Intervention Required Bit On
Yes
No
QG361
I/O Stop Switch On
No
Yes
QG361
Setup Stop Code
QG321
Reset Select Out and Send Service Out. Go to General Stop.
QE641
HB
Chart 155
QG361
Set Bit 6 and 7 of Byte 8B in MPX Storage to 11. Reset Select Out.
QG361, 311
Check Bit 3 of Byte 8B to See if a NPL Bar is in the Printer. If it is,Set an Indicator Bit.
QG311
Readout Printer Address. Wait for Operational In to Come Down, Send Service Out. Set Bus Out and Send Address Out. Set the d-Modifier into the Op Register.
QG301
Wait for Operational In to Come Up. Reset Address Out and Set Command Start. Wait for Address In, then Compare Address Out to Address In.
QG301
Addresses Match
No
Yes
QG261
Setup Stop Code
Reset Select Out and Send Service Out. Go to General Stop.
HB
Chart 155
QG261
Readout the Temporary Form Byte. Set Bus Out and Send Command Out. Check if this is a Skip Command (Bit 0 of the Command is a 1 for a Skip).
QG261
Command is a Skip
No
Yes
QG361
Check to See If the Skip is to Channel 1, 9, or 12. Reset and Set Bits 0 and 2 of Byte 8B in MPX Storage According to the Skip.
Skip Reset Set
1 0 and 2 -
9 - 0
12 - 2
QG351
Wait for Status In. This Status Should Contain Channel End, Device End, and Busy. Unit Check Could be on for an Intervention Required.
Unit Check Bit On
Yes
No
3
QG301
Reset Select Out, Send Service Out.
4
QG031
Check PMS Byte to See if I/O Traps Are Allowed . Set the Latches Accordingly.
QF661
Interrupt Exists
No
Yes
QE001
To Interrupt Decode
BA
Chart 155
QE001
To I-Cycles
AA
Chart 102


TAPE ERROR STOP, OR A/B INVALID
HA
QE651
Setup Stop Code
GENERAL STOP
HB
HALT OP
I-Cycles
QE641
Store Stop Code in Error Code Byte. Reset Select Out.
QE641
Store the Status Register and Readout the 1400 Control Byte. Test for Program Mode Switch
QE651
Store Stop Code in Error Code Byte
From I-Cycles QE471 for Row 3 Invalid Op Codes and Chart 156
INVALID OP
NG
QE651
Store Stop Code (04) in Error Code Byte
QE641
Do Program Mode Switch
YES
QE641
Setup and Store the Interrupt Code
NO
1
If a Program Mode Switch is Attempted on a Machine without the Feature, the Micro-Program Goes to a 10FF Halt with 08 Displayed
QE661
Store the I, A, and B-Stars in CPU Storage. Store the Op Register and 1400 A-Register in CPU Storage. Set B-Star from the I-Star
QE661
Do Program Mode Switch
YES
QE661
To Program Mode Switch Routine
QE731
XM
Chart 156
NO
QE671
Readout Low Bias
QF811,821
Readout High Bias Subtract Bias from B-Star (I-Star Conversion) and Convert 1400 Address to a Decimal Number.
QE671
Store I-Star Decimal Number. Check if A-Star was Valid
QE671
A-Star was Valid
NO
QE681
Change the Invalid Address to Three BCD Character (16 Bits) for Display Purpose
YES
QE671
Set A-Star Value from CPU Storage into the B-Star
QE671
Readout Low Bias
QF811,821
Readout High Bias Subtract Bias from B-Star (A-Star Conversion) and Convert 1400 Address to a Decimal Number
QE671
Store Converted A-Star in MPX Storage. Check if B-Star was Valid
INTERRUPT DECODE
BA
From I-Cycles Interrupt (Multiple Entry)
QE601
Test for Type of Interrupt
QE601
Channel Interrupt
YES
QE661
1
NO
QE601
Timer is Zero
NO
QE601
Update the Timer
2
YES
3
QE601
Test External Interrupt Register
QE601
Sense Switch Operation
YES
QE621
Setup Bit to Represent Sense Switch B, C, D, E, F, or G in the Sense Switch Byte
QE621
Set or Reset Switch Bit
RESET
QE621
Reset Bit for Correct Switch in Sense Switch Byte
SET
QE621
Set Bit On for Correct Switch in the Sense Switch Byte
NO
QE621
External or Console Interrupt
YES
QE621
Readout Channel Mask Test for External Interrupt
Position 2 of the F Switch or External Interrupt which Sets F-Register Bits Other than 0 or 1
NO
QE621
Start Reset
YES
NO
QE621
Allow Interrupts
NO
2
YES
QE621
Tape Density, Tape Address or Sterling Exit
QE661
1
QE671
B-Star was Valid
NO
QE681
Change the Invalid Address to Three BCD Characters (16 Bits) for Display Purpose.
YES
QE671
Set B-Star Value from CPU Storage into the B-Star.
QE671
Readout Low Bias
QE671
Readout High Bias. Subtract Bias from B-Star (B-Star Conversion) and Convert 1400 Address to a Decimal Number. Go to Display Routine
QE691
Set the Converted Numbers for the I, A, and B-Star into the Respective Stars.
QE691
Tape Display
NO
QE691
Normal Stops
YES
QE691
Set Stop to 00
NO
QE691
Sense Switch Operation
YES
Setup for Display. Block all Traps and Set Command Start in Multiplexor Channel. I-Address is Displayed in the 360 A and B Registers, Stop Code in R-Register, and ALU Output is 00
NO
QE691
1403, 2540, 2501, or 2520 Operation
YES
QE692
2501, 2520 Operation 6F Stop
NO
YES
QG071,QE691
Setup Tape Drive Information for Display. R-Register Contains: High 4 Bits - Density Low 4 Bits - 2400 Unit. ALU Output is 99
Normal Stops are Stop Key, Instruction Stop, or Roar Stop Delay
Readout Sense Switch Byte. Setup for Display. I-Address Display in the 360 A and B Registers Sense Switch Byte in the R-Register and ALU Output is 99
Stop
Restart - Go to Restart Routine
4
QE531
Turn On Suppress Out, Reset Command Start
Turn On Wait Latch
NO
Unit Ready
YES
When Unit is Made Ready, Continue Operation.
Set Command Start, Reset Suppress Out.
QE711
Stop Code Bit 2, Bit 3
11
00
01
10
11
QE711
1050 Return
QG111
TB
Chart 147
QE711
To I-Cycles
QE001
AA
Chart 102
QE711
Return to Halt and Branch
QF661
CAS Logic QF661
QE711
Stop Code Bit 0, Bit 1
10
01
00
QE711
To I-Cycles
QE001
AA
Chart 102
Card or Printer Return
1442 1443 QG301
RR
1402 1403 QG581
Chart 149 to 154
Chart 108
Test 4 High Bits of the Stop Code. Check what Routine to Return to
IPL ROAR RESET CARD OR TAPE
Forced ROS Address. Auxiliary Storage is Loaded Correctly
QE521
Setup Address of First Instruction in the I-Star Backup Bytes
QE631
Reset the Error Bits, Sense Switch A, Card Status Bits, Overflow, and Inquiry Request Bits. Setup Stop Code of 55. Reset Various Control Latches in the 1050 Attachment. Reset Zero Indicate.
QE631
IPL or Start Reset
START RESET
Setup Forms Byte to (08) 0000 1000
QE661
1
IPL
Chart 156
YM
4
Setup Forms Byte to (08) 0000 1000 QE631
QE531
Set a Latch (H0) to Prevent Memory Wrap Detection. Readout Bias
QE531
Do Storage Scan for Invalid Characters
NO
A Storage Scan Routine is Done for IPL or Start Reset
YES QE541
Setup Highest 1400 Address. Readout Char and do a Table Lookup
Start of a Routine to Clear 1400 Area of Invalid 1400 Characters
QE641
Legal 1400 Character
NO
QE641
Change Character to a Blank (40)
YES
QE641
Readout Next Character from Next Lower Address
QE641
Address is 1 Less than 1400 Address 0000
NO
YES
QE531
Set the Character 8F into Main Storage One Position Less than 1400 Address 0000. (Used to Detect Storage Wraps).
QE531
Allow I/O Traps Bit On
YES
Setup to Allow Traps. and Reset Command Start
NO
Setup to Allow External Interrupts and Prevent all I/O Traps
QE551
Initial Program Load
NO
YES
QE551
Tape Load
YES
NO
QE551
51 Column Load
YES
Setup Address Equal to 1400 Address 0015 and a Count of 51
NO
QE551
Set 1400 Address 0001 or 0015 to a Blank with a Wordmark
QE551
Set Next Position to a Blank (40)
Clear Read-In Area
QE551
End or Read In Area
NO
Column 65 - 51 Col Read
Column 80 - 80 Col Read
YES
1442 Card Reader
YES
QE551
Set 1400 Address 0081 Position to GMWM (0F)
NO
QE701
Restore or Initially Setup the I, A, and B-Stars; Also the Op Code.
QE701
Console Interrupt Key
NO
YES
3
Enter Interrupt Routine after a 10FF Stop or IPL before going to I-Cycles
2
QE701
Restore A-Star from MPX Storage
QE701
Stop was an Intervention Required
YES
QE711
Low 4 Bits of the Stop Code are 1111
YES
QE711
NO
QE701
I-Star Address is 0000
NO
QE701
To I-Cycles
QE001
AA
Chart 102
YES
QE701
Setup Stop Code 0C
QE701
To General Stop
1

Op Code 99 Objectives

Bytes Defined	W2 LS'A'	W2 LS'B'
80 through 83	0	8
84 through 87	1	9
88 through 8B	2	A
8C through 8F	3	B
90 through 93	4	C
94 through 97	5	D
98 through 9B	6	E
9C through 9F	7	F

Chart 1

SI

99	W1	W2	B1	D1
CFIM	0	*	Main Storage Address	
CFMS	1	*		
CFSV	3	*1		
CFLV	2	*2		
CFSC	9	*3		
CFSC	D	*4		
CFLC	8	*5		
CFLC	C	*6		

* If W2 is a 0 - No Initialization Required
1 - Initialize for 1402 Card Load
2 - Initialize for 1400 Tape Load
9 - Initialize for 1442 Card Load

*1 If W2 Is 0 Through F, Store Four Bytes from Main Storage at Location Shown in Chart 1

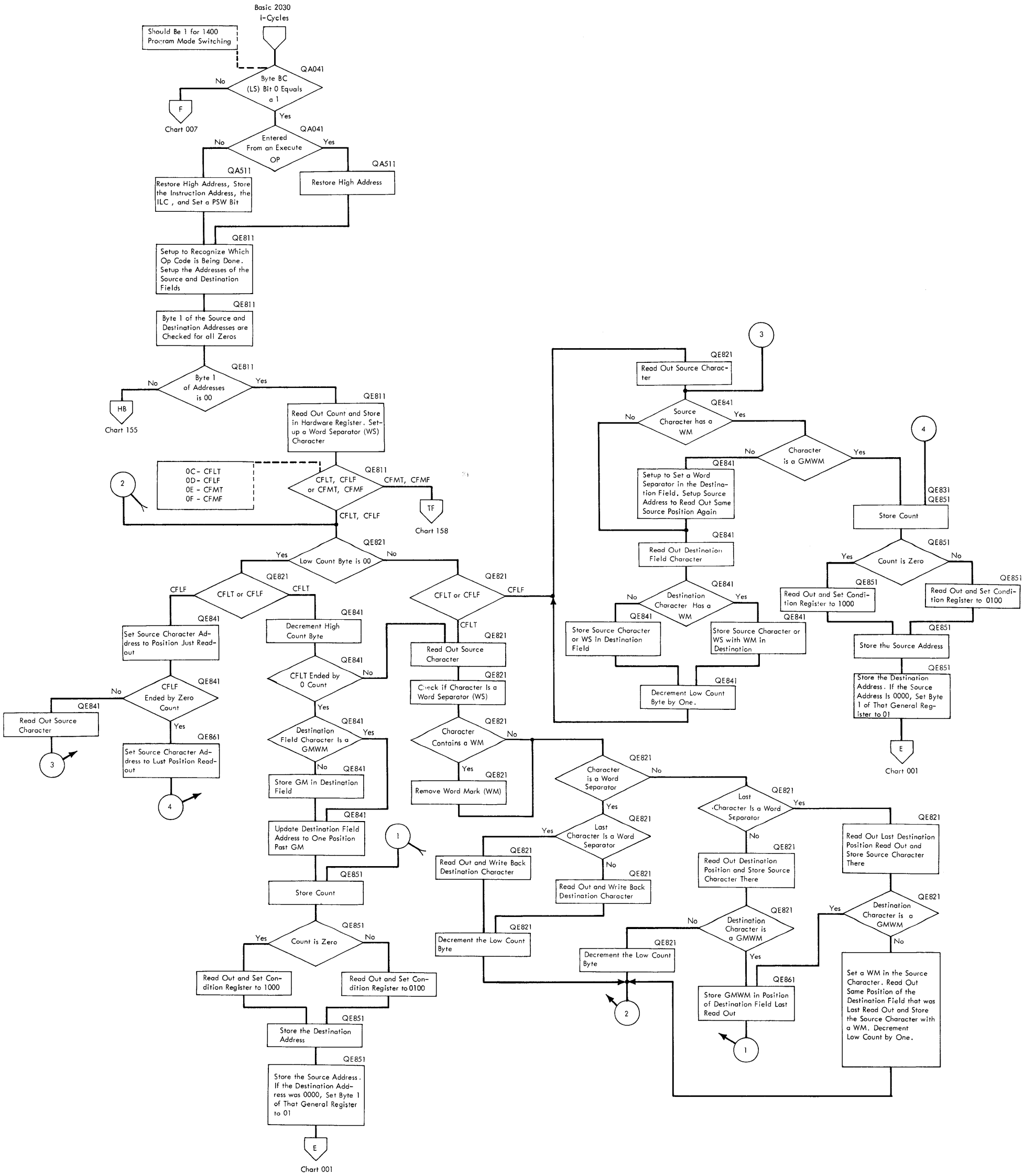
*2 If W2 Is 0 Through F, Load Four Bytes from Local Storage per Chart 1 into Main Storage

*3 If W2 Is 0 Through F, Store Sixteen Bytes from Main Storage into Local Storage 'A'. Local Storage Locations are Determined by W2; if a 0, Location 00 Through 0F are Stored etc.

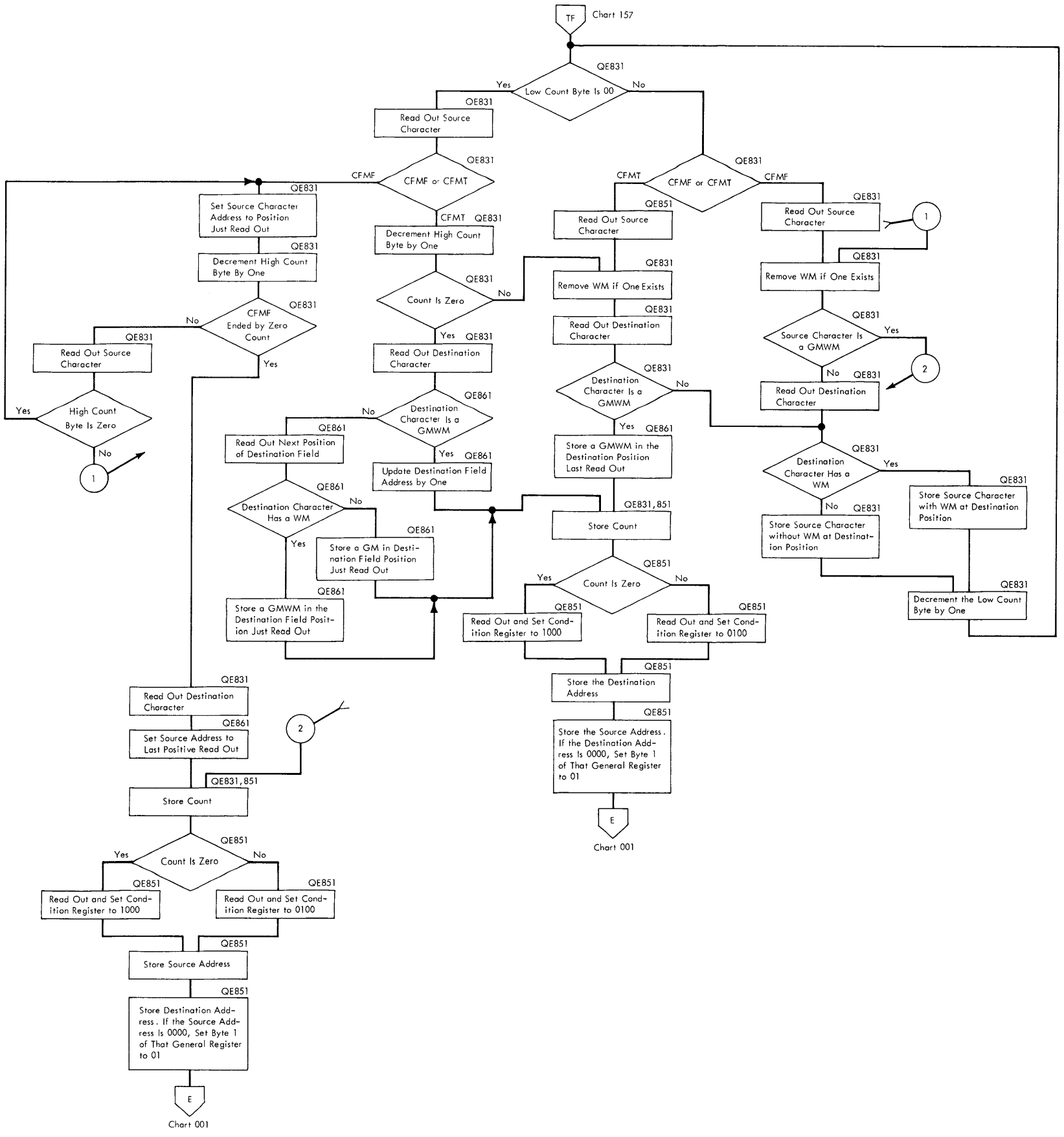
*4 Same as *3 Only Use Local Storage 'B'

*5 If W2 Is 0 Through F, Load Sixteen Bytes from Local Storage 'A' into Main Storage. Locations (LS) Are Determined the Same as *3

*6 Same as *5 Only Use Local Storage 'B'

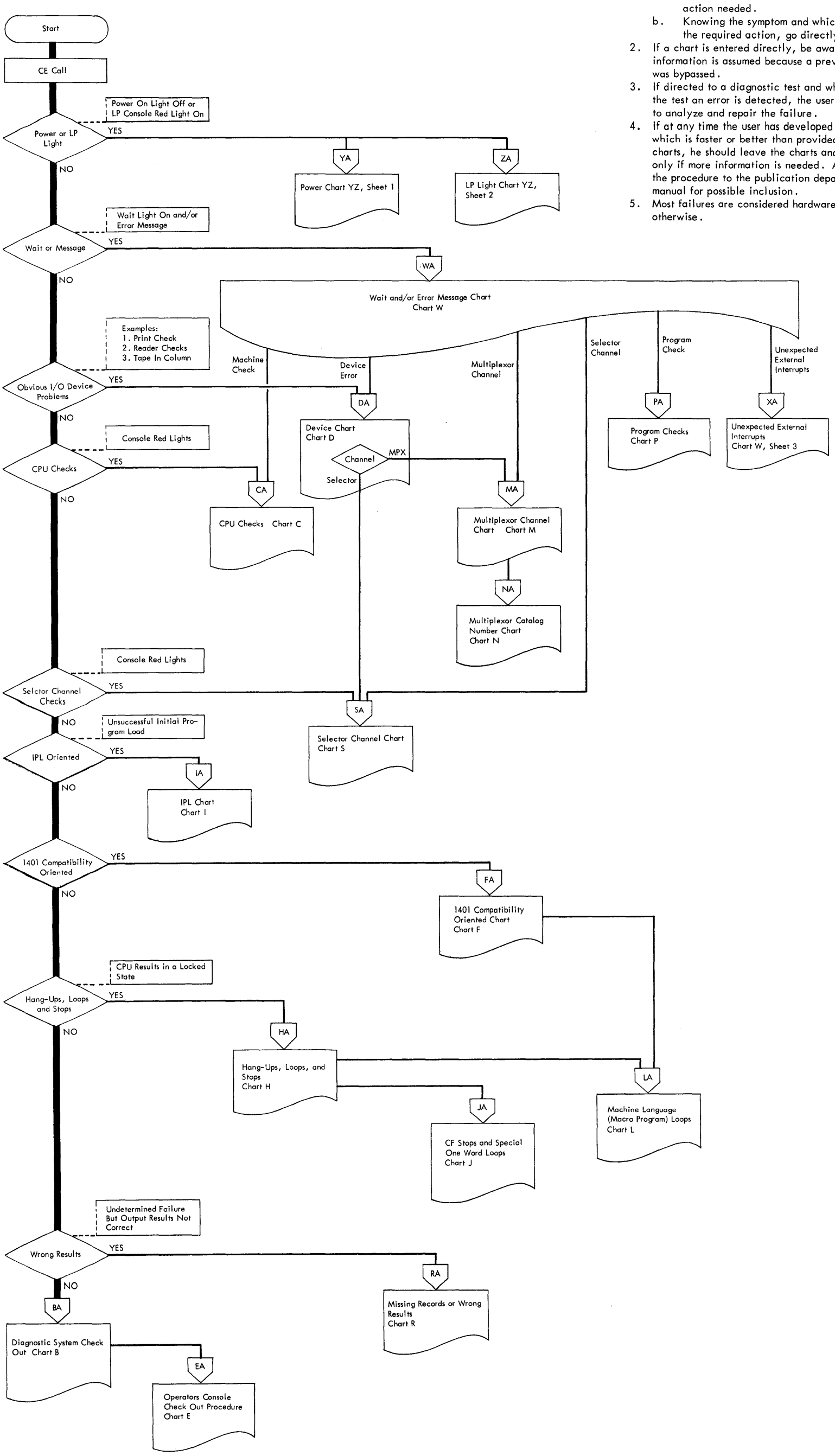


CLF 157 CFMT, CFMF, CFLT, and CFLF Instructions, Sheet 1

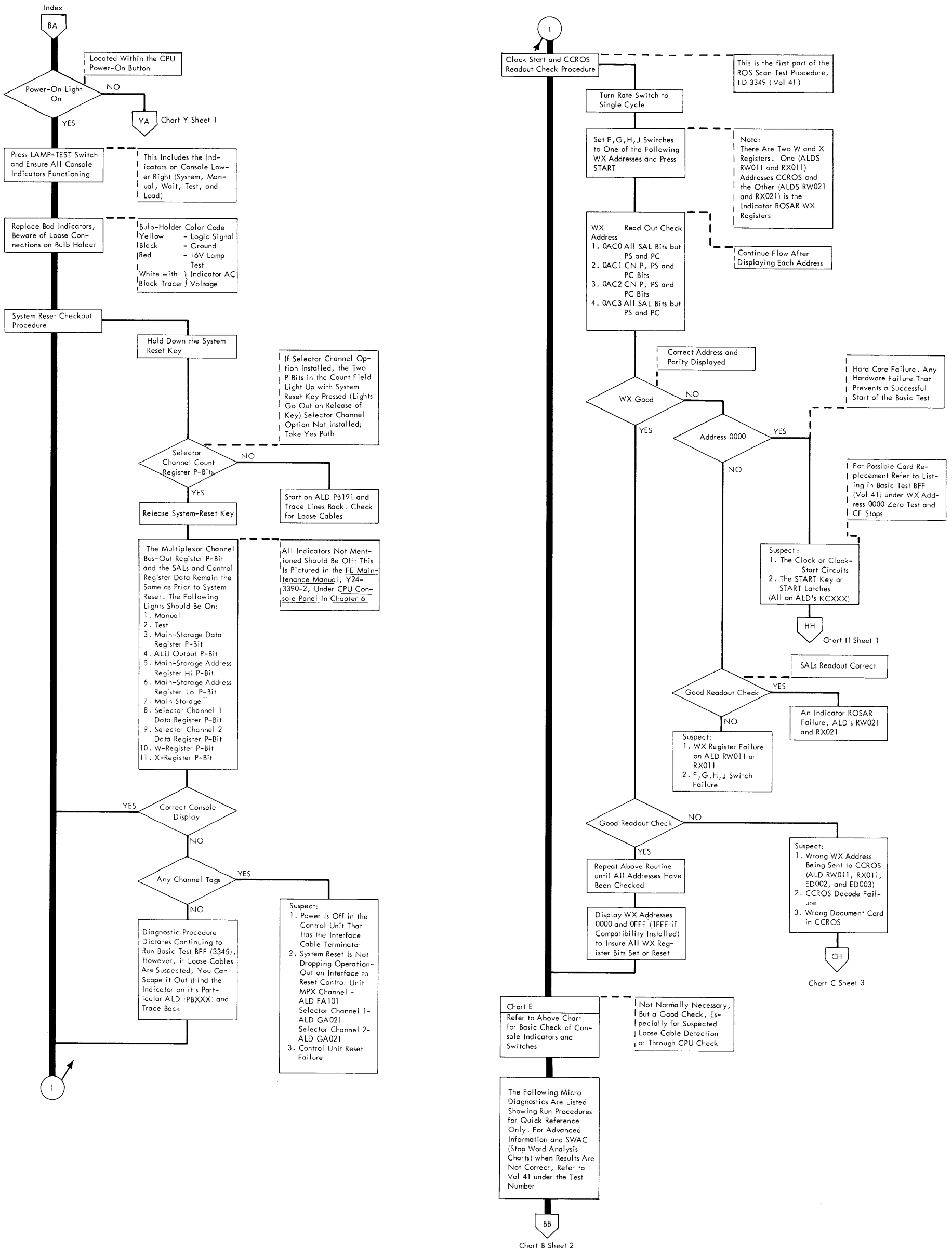

TF
Chart 157
QE831
Low Count Byte Is 00
Yes
No
QE831
Read Out Source Character
QE831
CFMF or CFMT
CFMF
CFMT
QE831
Set Source Character Address to Position Just Read Out
QE831
Decrement High Count Byte By One
QE831
CFMF Ended by Zero Count
No
Yes
QE831
Read Out Source Character
Yes
High Count Byte Is Zero
No
1
CFMT QE831
Decrement High Count Byte by One
QE831
Count Is Zero
No
Yes
QE831
Read Out Destination Character
QE861
Destination Character Is a GMWM
No
Yes
QE861
Read Out Next Position of Destination Field
QE861
Destination Character Has a WM
No
Yes
QE861
Store a GM in Destination Field Position Just Read Out
QE861
Store a GMWM in the Destination Field Position Just Read Out
QE861
Update Destination Field Address by One
QE831
Read Out Destination Character
QE831
Read Out Source Character
QE831,851
Store Count
QE851
Count Is Zero
Yes
No
QE851
Read Out and Set Condition Register to 1000
QE851
Read Out and Set Condition Register to 0100
QE851
Store Source Address
QE851
Store Destination Address. If the Source Address Is 0000, Set Byte 1 of That General Register to 01
E
Chart 001
2
QE831
Read Out Destination Character
QE861
Set Source Address to Last Positive Read Out
QE831,851
Store Count
QE851
Count Is Zero
Yes
No
QE851
Read Out and Set Condition Register to 1000
QE851
Read Out and Set Condition Register to 0100
QE851
Store Source Address
QE851
Store Destination Address. If the Source Address Is 0000, Set Byte 1 of That General Register to 01
E
Chart 001
QE831
CFMF or CFMT
CFMT
CFMF
QE851
Read Out Source Character
QE831
Remove WM if One Exists
QE831
Read Out Destination Character
QE831
Destination Character Is a GMWM
No
Yes
QE861
Store a GMWM in the Destination Position Last Read Out
QE831,851
Store Count
QE851
Count Is Zero
Yes
No
QE851
Read Out and Set Condition Register to 1000
QE851
Read Out and Set Condition Register to 0100
QE851
Store the Destination Address
QE851
Store the Source Address. If the Destination Address Is 0000, Set Byte 1 of That General Register to 01
E
Chart 001
QE831
Read Out Source Character
1
QE831
Remove WM if One Exists
QE831
Source Character Is a GMWM
Yes
No
2
QE831
Read Out Destination Character
QE831
Destination Character Has a WM
Yes
No
QE831
Store Source Character with WM at Destination Position
QE831
Store Source Character without WM at Destination Position
QE831
Decrement the Low Count Byte by One

Diagnostic Techniques Charts.
How to Use.

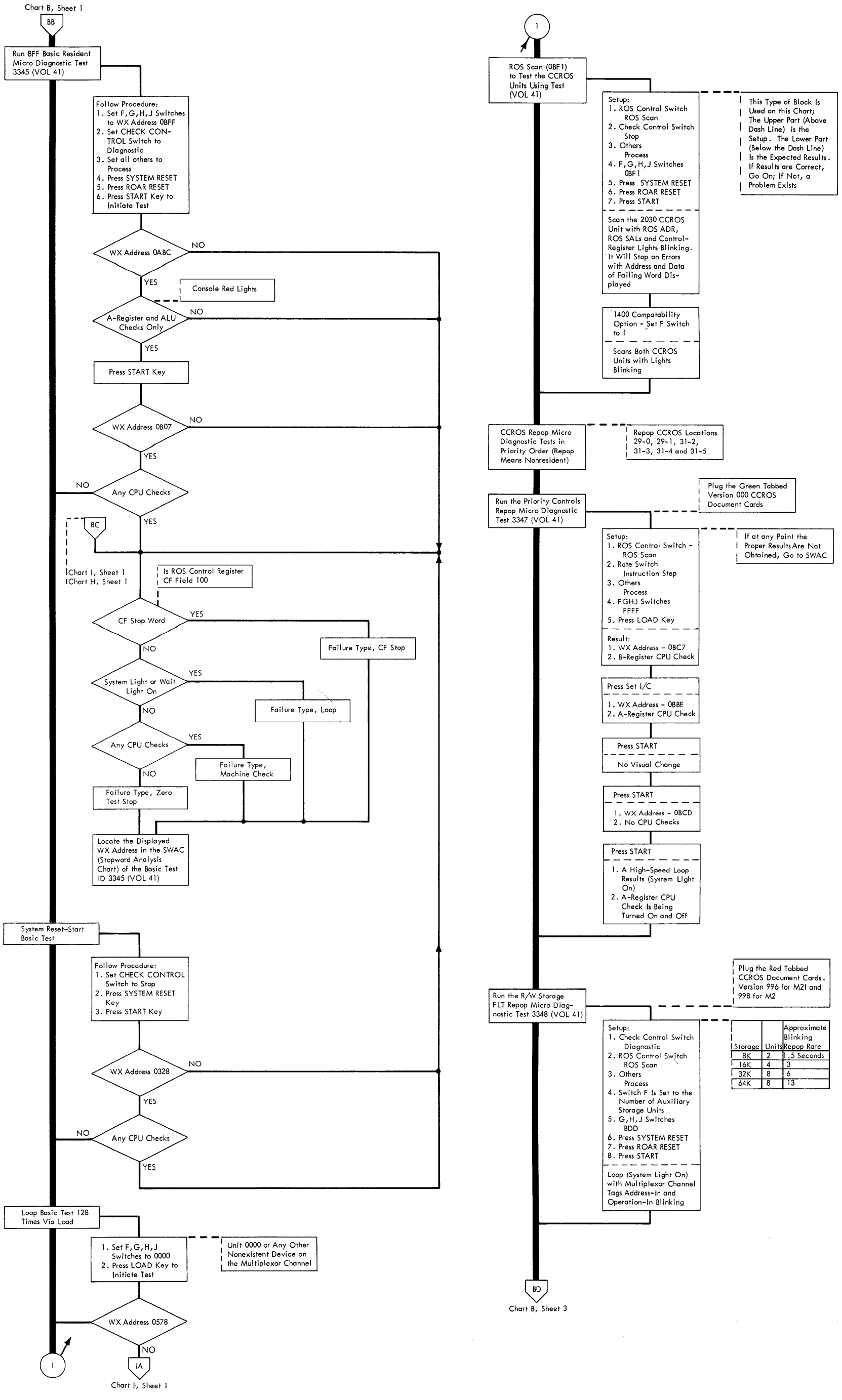
1. Initial entry can be by:
   a. Starting on this chart (chart A) find a symptom and find which chart shows the required action needed.
   b. Knowing the symptom and which chart shows the required action, go directly to that chart.
2. If a chart is entered directly, be aware that some information is assumed because a previous chart was bypassed.
3. If directed to a diagnostic test and while running the test an error is detected, the user is expected to analyze and repair the failure.
4. If at any time the user has developed an approach which is faster or better than provided in the charts, he should leave the charts and link back only if more information is needed. Also, send the procedure to the publication department of this manual for possible inclusion.
5. Most failures are considered hardware until proven otherwise.



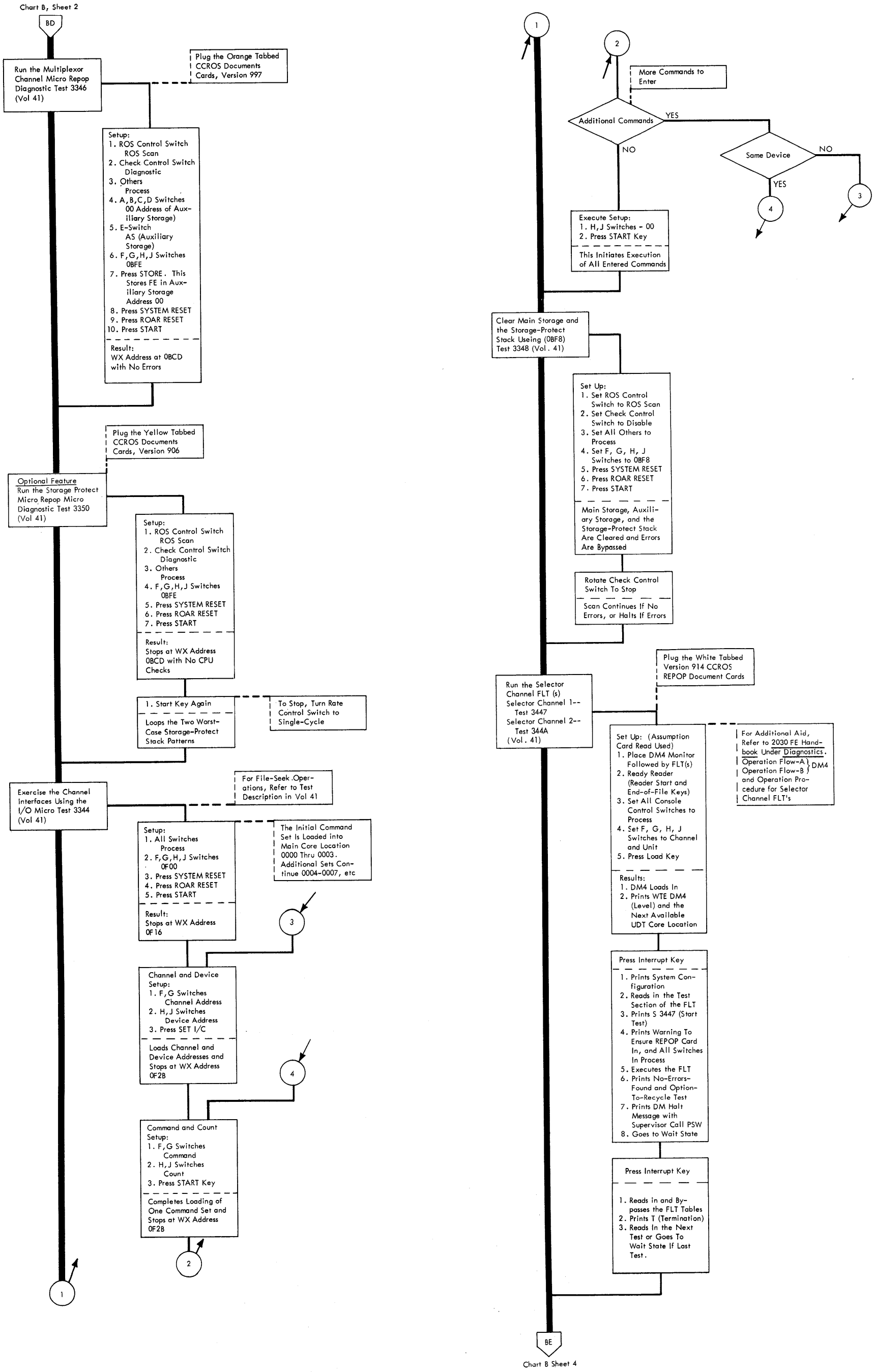
DT Chart A Action Index



DT Chart B Diagnostic Check Out (Sheet 1



DT Chart B Diagnostic Check Out (Sheet 2)



DT Chart B Diagnostic Check Out (Sheet 3)

Chart B Sheet 3

BE

The Selector Channel FLT's Are the Only 2030 Machine Language (Macro) Diagnostics That Cause CPU Red Light Checks. Thus the User Can Run the Remaining Tests in Stop Mode, if Desired

Stop Mode Stops the Machine for Unexpected CPU Failures Before Monitor Logs Them Out. Press Start if Logout Is Desired or Go Directly to Chart C Sheet 1 At CA

Run All Associated Machine Language (Macro) Diagnostics. This Should Include

1. CPU Standard Set
2. CPU Optional Features
3. Standard I/O
4. Optional I/O
5. Meter Test
6. Compatibility CPU and I/O
7. System Test

For Test ID Numbers Refer to The 2030 FE Handbook Under System/360 Diagnostics For An Excellent Listing and Suggested Running Order Refer to the 2030 Installation Instructions Part Number 824400 Appendix A Sections 3 and 4

Chart R, Sheet 2

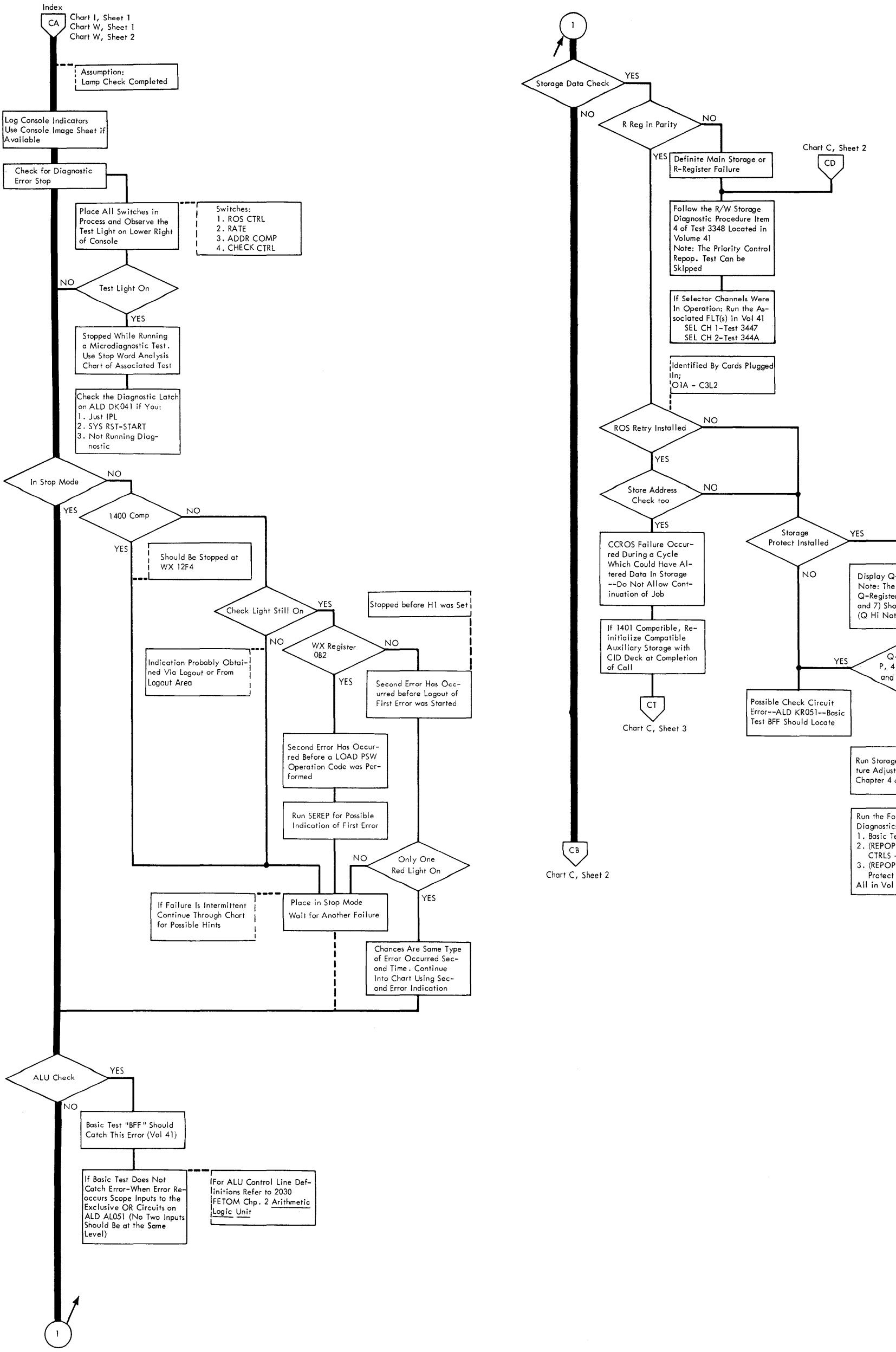
BF

The Remainder of This Chart Is Intended to Introduce the User to Methods, Procedures, and Areas of the System That Are Not Normally Checked. This Information May Be of Value on Intermittent Problems or When All Other Methods Have Been Exhausted, But Extreme Caution Is Recommended in Most Areas

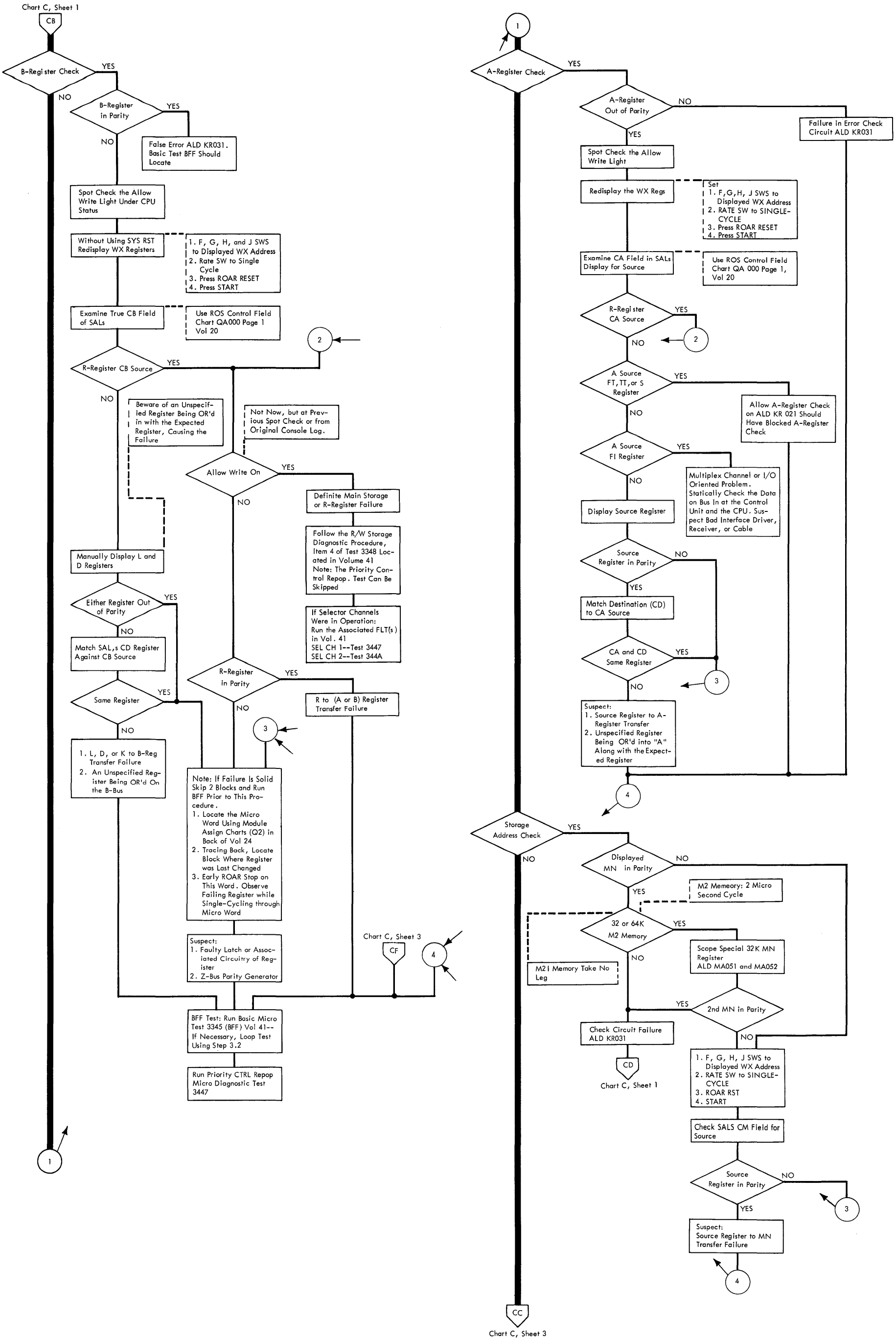
Review of CEM's, Retain, etc. Should Be Checked For Similar Problems Before Even Considering These Hints

1. An Excellent CPU Checkout Is Listed Under CCROS Service Hints in Chapter 1 of the 2030 FEMM
2. Do The CPU Switch and Indicator Check Procedure, Chart E, Sheet 1 at EA
3. Run the CCROS Voltage Check in Chapter 4 of the FE Maintenance Manual
4. Disable the Retry Circuits and Have Customer Run His Jobs in Stop Mode
5. Run Main Storage Worst-Case Pattern Tests and Check Memory SCHM00
6. Disconnect Blower Motors on CCROS and Storage Units, Raise Room Temperature in Attempt to Bring Out Intermittents
7. Cool Suspected Areas Using ICE or Dry Ice and a Blower or Fan (It May Help to Find a Broken Land Pattern.)
8. Vibrate Entire Units
9. Ensure That All Cards and Edge Connectors Are Seated; Use a Pencil with an Eraser to Reach the Small Crossover Cables in the CPU
10. Tap Cards and Edge Connectors
11. Use Marginal Voltages in SMS Control Units (Such As 2821)
12. Varying Voltages in the CPU Has Not Seemed to Be of Much Value, But Can Be Tried with Extreme Caution
13. Use Anti-Static Spray and Solutions when Static Electricity Is Suspected
    Note: Beware of Furniture with Casters Being Moved Past The System
14. Run or Prevent Operation of Communications and Other External Electronic and Electrical Devices to Decrease or Increase Failures
15. Beware of Room Temperatures Above 98° and Humidity Below 20%.
16. Is It Always the Same Shift or Operator When Failure Occurs
17. Check the Last Control Unit on Every Channel for the Interface Terminator
18. Spot-Check Voltage Levels on CPU Boards, CCROS, Storage, and the 1/2 Board 01F.
    For the 1050 Interface
    +6v--Pin B11
    +3v--Pin D03
    Ground--Pin D08
    -3--Pin B06
    Note: For 1/2 Board Voltages, Refer to ALD PF571
19. Check All Single-Shot Settings. The Following Is A List of the Single-Shots in the CPU

Single-Shots in CPU	
ALD	Function
DM051	Metering
FA101	MPX Channel Operation-Out Reset
GA021	Selector Channel 1 Operation-Out Reset
GA021	Selector Channel 1 Hold-Out Interlock
HA021	Selector Channel 2 Operation-Out Reset
HA021	Selector Channel 2 Hold-Out Interlock
PF042	1052 Carrier Return Line Feed
PF043	1050 Restore (Reset)
PF071	1050 Attention (Request)
PF251	Audible Alarm (Optional)



DT Chart C CPU Checks (Sheet 1)



DT Chart C CPU Checks (Sheet 2)

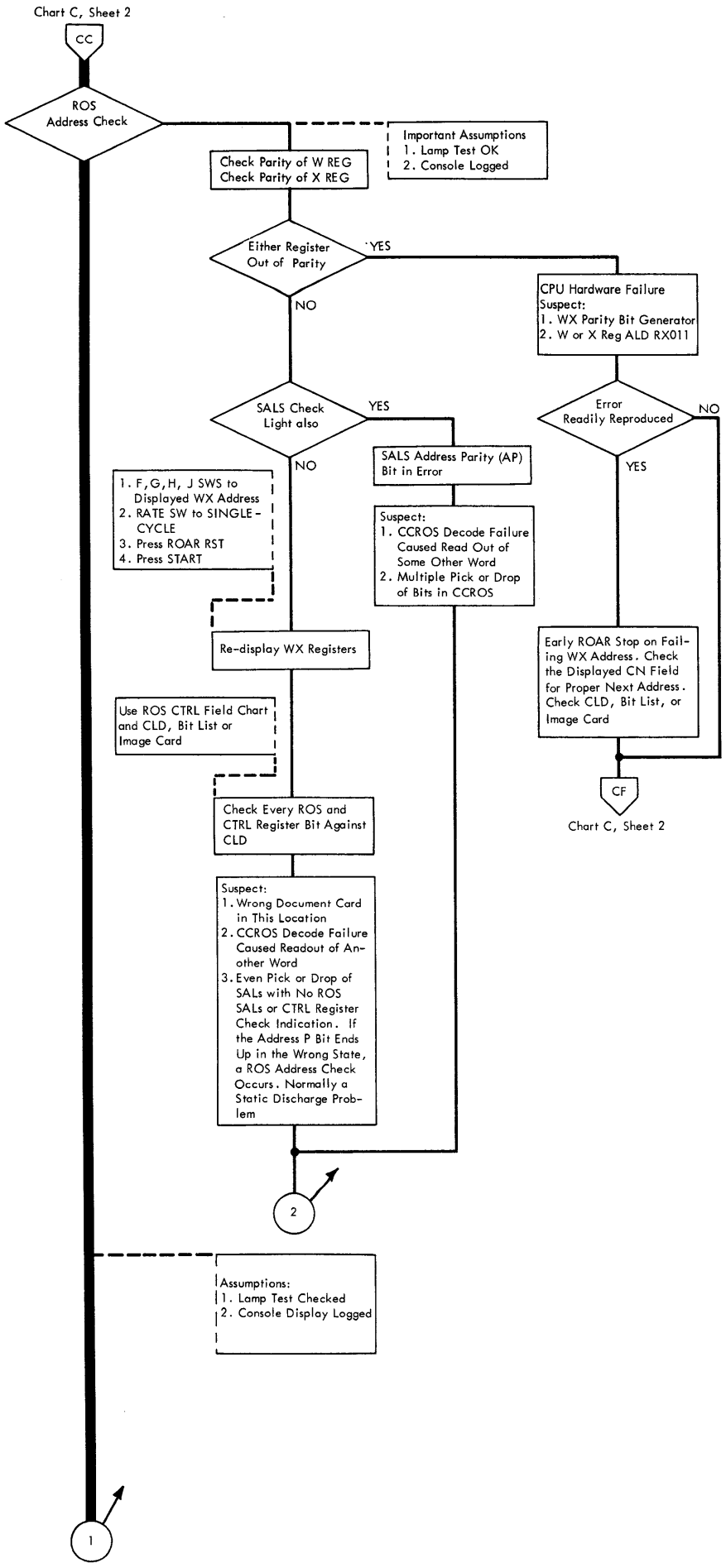
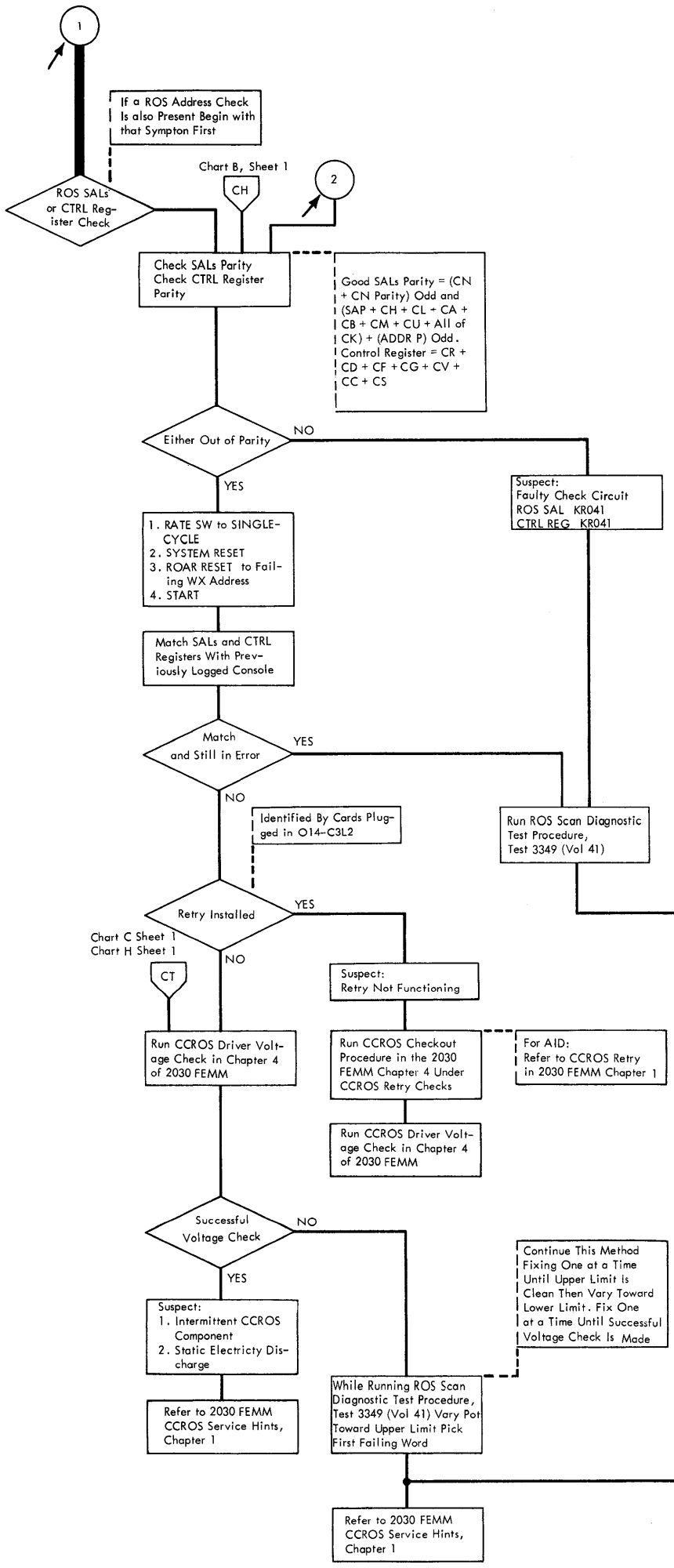
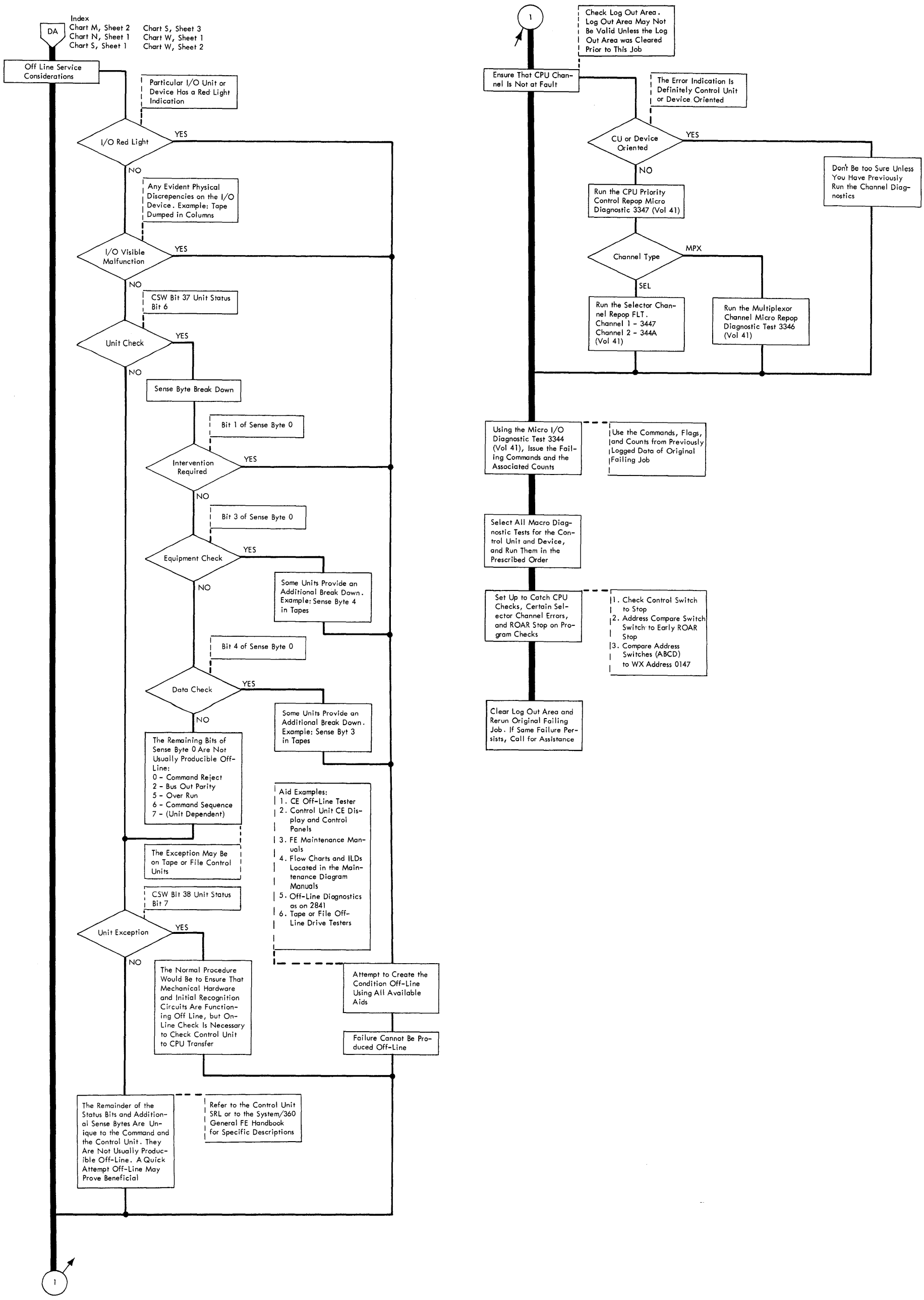
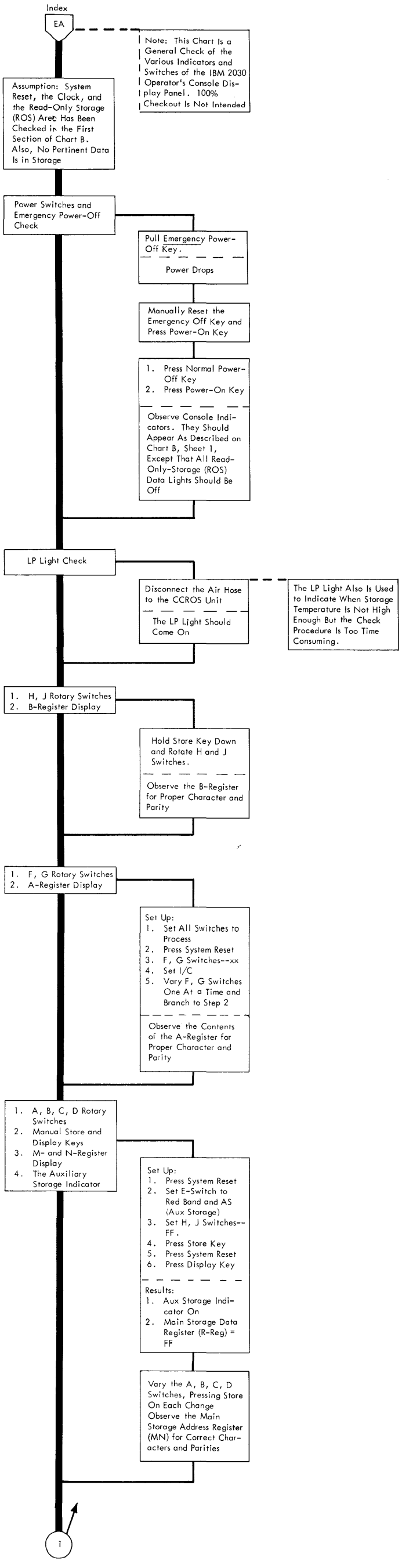


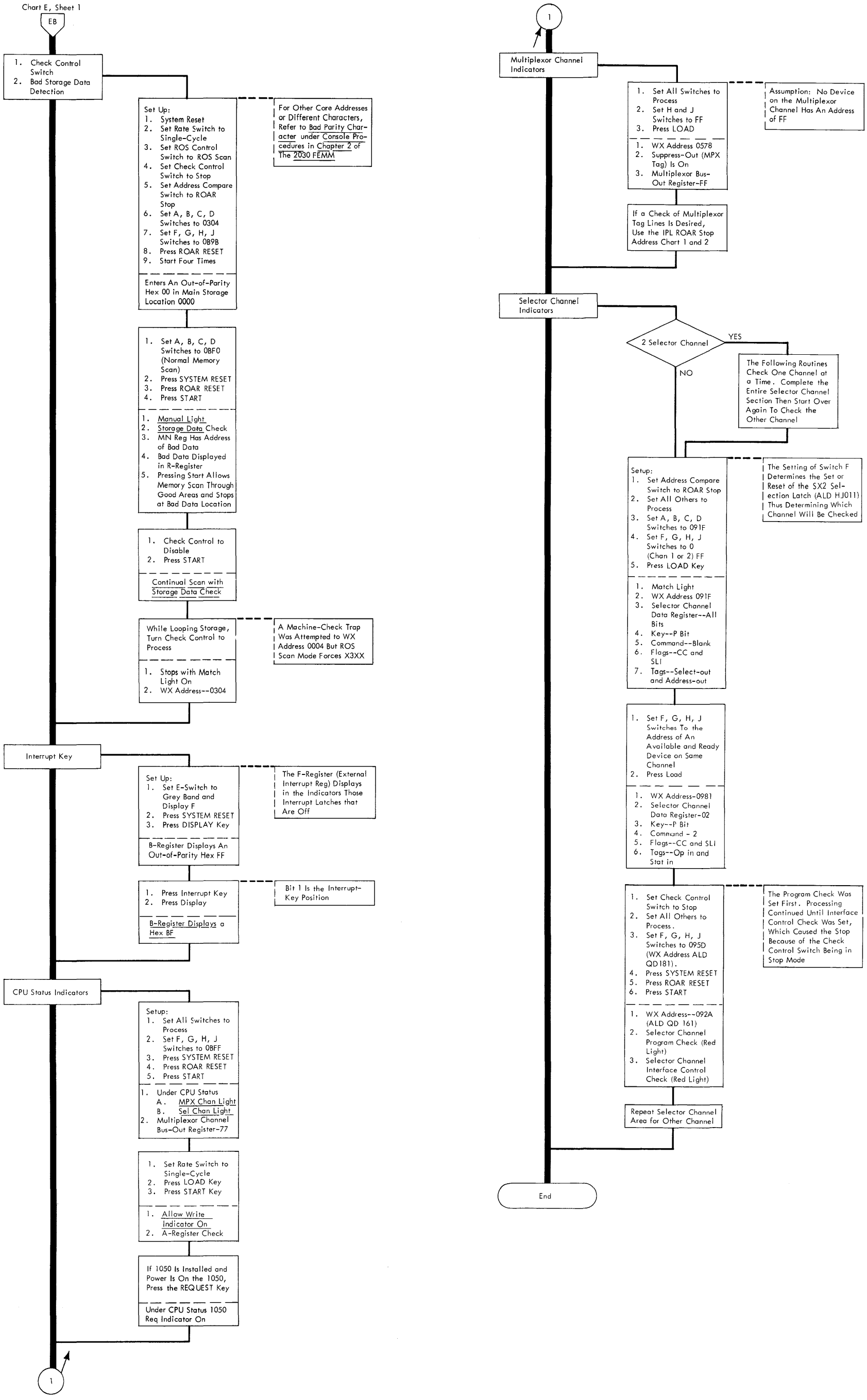
Chart C, Sheet 2
CC
ROS Address Check
Important Assumptions
1. Lamp Test OK
2. Console Logged
Check Parity of W REG
Check Parity of X REG
Either Register Out of Parity
YES
NO
CPU Hardware Failure Suspect:
1. WX Parity Bit Generator
2. W or X Reg ALD RX011
SALS Check Light also
YES
NO
Error Readily Reproduced
NO
YES
SALS Address Parity (AP) Bit in Error
1. F,G,H, J SWS to Displayed WX Address
2. RATE SW to SINGLE-CYCLE
3. Press ROAR RST
4. Press START
Suspect:
1. CCROS Decode Failure Caused Read Out of Some Other Word
2. Multiple Pick or Drop of Bits in CCROS
Re-display WX Registers
Early ROAR Stop on Failing WX Address. Check the Displayed CN Field for Proper Next Address. Check CLD, Bit List, or Image Card
CF
Chart C, Sheet 2
Use ROS CTRL Field Chart and CLD, Bit List or Image Card
Check Every ROS and CTRL Register Bit Against CLD
Suspect:
1. Wrong Document Card in This Location
2. CCROS Decode Failure Caused Readout of Another Word
3. Even Pick or Drop of SALs with No ROS SALs or CTRL Register Check Indication. If the Address P Bit Ends Up in the Wrong State, a ROS Address Check Occurs. Normally a Static Discharge Problem
2
Assumptions:
1. Lamp Test Checked
2. Console Display Logged
1


1
If a ROS Address Check Is also Present Begin with that Sympton First
ROS SALs or CTRL Register Check
Chart B, Sheet 1
CH
2
Check SALs Parity Check CTRL Register Parity
Good SALs Parity = (CN + CN Parity) Odd and (SAP + CH + CL + CA + CB + CM + CU + All of CK) + (ADDR P) Odd. Control Register = CR + CD + CF + CG + CV + CC + CS
Either Out of Parity
NO
YES
Suspect:
Faulty Check Circuit
ROS SAL KR041
CTRL REG KR041
1. RATE SW to SINGLE-CYCLE
2. SYSTEM RESET
3. ROAR RESET to Failing WX Address
4. START
Match SALs and CTRL Registers With Previously Logged Console
Match and Still in Error
YES
NO
Identified By Cards Plugged in O14-C3L2
Run ROS Scan Diagnostic Test Procedure, Test 3349 (Vol 41)
Retry Installed
YES
NO
Chart C Sheet 1
Chart H Sheet 1
CT
Suspect:
Retry Not Functioning
Run CCROS Driver Voltage Check in Chapter 4 of 2030 FEMM
Run CCROS Checkout Procedure in the 2030 FEMM Chapter 4 Under CCROS Retry Checks
For AID:
Refer to CCROS Retry in 2030 FEMM Chapter 1
Run CCROS Driver Voltage Check in Chapter 4 of 2030 FEMM
Successful Voltage Check
NO
YES
Continue This Method Fixing One at a Time Until Upper Limit is Clean Then Vary Toward Lower Limit. Fix One at a Time Until Successful Voltage Check Is Made
Suspect:
1. Intermittent CCROS Component
2. Static Electricty Discharge
Refer to 2030 FEMM CCROS Service Hints, Chapter 1
While Running ROS Scan Diagnostic Test Procedure, Test 3349 (Vol 41) Vary Pot Toward Upper Limit Pick First Failing Word
Refer to 2030 FEMM CCROS Service Hints, Chapter 1

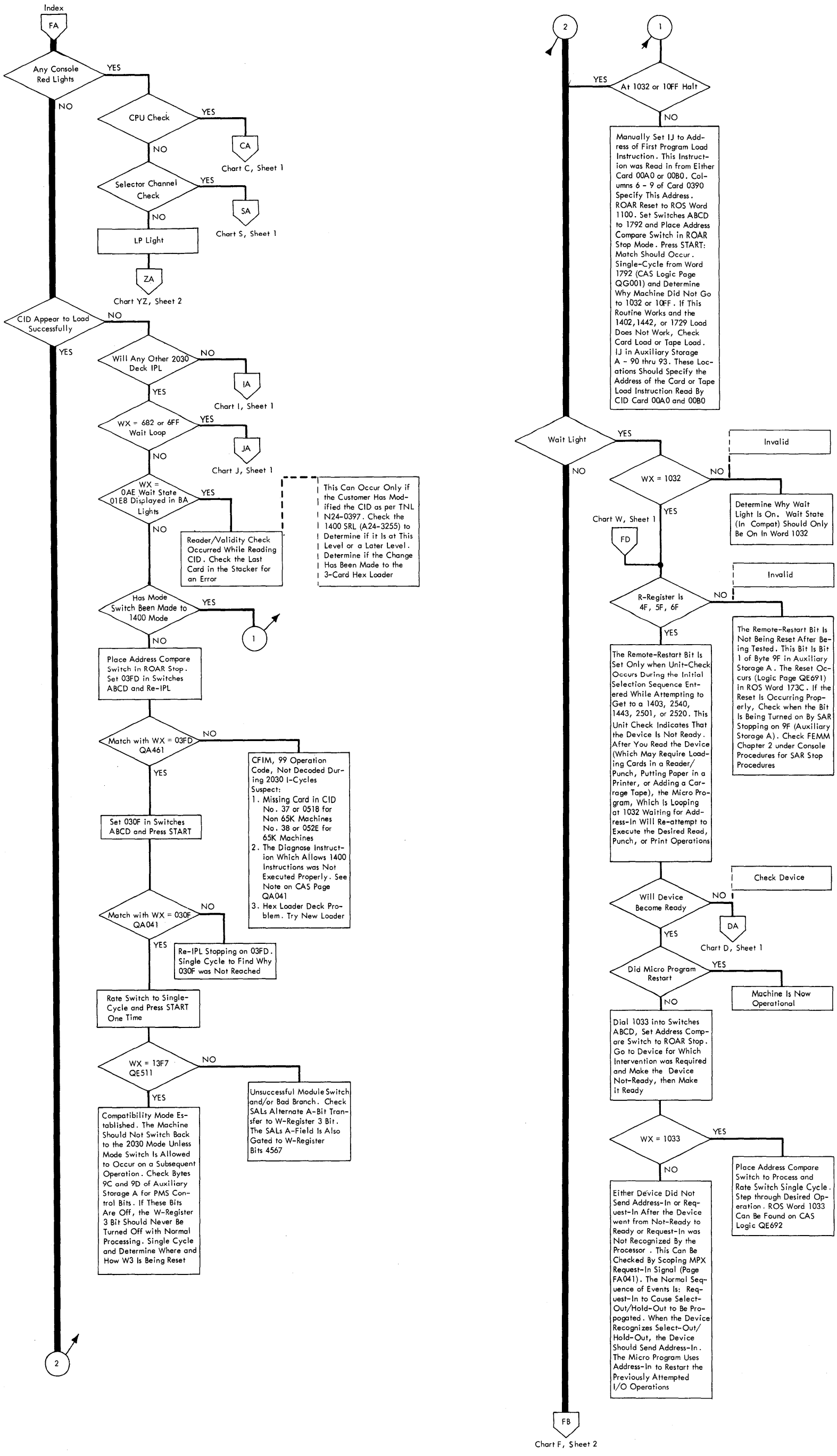

DA
Index
Chart M, Sheet 2
Chart N, Sheet 1
Chart S, Sheet 1
Chart S, Sheet 3
Chart W, Sheet 1
Chart W, Sheet 2
Off Line Service Considerations
Particular I/O Unit or Device Has a Red Light Indication
I/O Red Light
YES
NO
Any Evident Physical Discrepencies on the I/O Device. Example: Tape Dumped in Columns
I/O Visible Malfunction
YES
NO
CSW Bit 37 Unit Status Bit 6
Unit Check
YES
NO
Sense Byte Break Down
Bit 1 of Sense Byte 0
Intervention Required
YES
NO
Bit 3 of Sense Byte 0
Equipment Check
YES
NO
Some Units Provide an Additional Break Down. Example: Sense Byte 4 in Tapes
Bit 4 of Sense Byte 0
Data Check
YES
NO
Some Units Provide an Additional Break Down. Example: Sense Byt 3 in Tapes
The Remaining Bits of Sense Byte 0 Are Not Usually Producible Off-Line:
0 - Command Reject
2 - Bus Out Parity
5 - Over Run
6 - Command Sequence
7 - (Unit Dependent)
The Exception May Be on Tape or File Control Units
CSW Bit 38 Unit Status Bit 7
Unit Exception
YES
NO
The Normal Procedure Would Be to Ensure That Mechanical Hardware and Initial Recognition Circuits Are Functioning Off Line, but On-Line Check Is Necessary to Check Control Unit to CPU Transfer
Aid Examples:
1. CE Off-Line Tester
2. Control Unit CE Display and Control Panels
3. FE Maintenance Manuals
4. Flow Charts and ILDs Located in the Maintenance Diagram Manuals
5. Off-Line Diagnostics as on 2841
6. Tape or File Off-Line Drive Testers
Attempt to Create the Condition Off-Line Using All Available Aids
Failure Cannot Be Produced Off-Line
The Remainder of the Status Bits and Additional Sense Bytes Are Unique to the Command and the Control Unit. They Are Not Usually Producible Off-Line. A Quick Attempt Off-Line May Prove Beneficial
Refer to the Control Unit SRL or to the System/360 General FE Handbook for Specific Descriptions
1
1
Check Log Out Area. Log Out Area May Not Be Valid Unless the Log Out Area was Cleared Prior to This Job
Ensure That CPU Channel Is Not at Fault
The Error Indication Is Definitely Control Unit or Device Oriented
CU or Device Oriented
YES
NO
Don't Be too Sure Unless You Have Previously Run the Channel Diagnostics
Run the CPU Priority Control Repop Micro Diagnostic 3347 (Vol 41)
Channel Type
MPX
SEL
Run the Selector Channel Repop FLT.
Channel 1 - 3447
Channel 2 - 344A
(Vol 41)
Run the Multiplexor Channel Micro Repop Diagnostic Test 3346 (Vol 41)
Using the Micro I/O Diagnostic Test 3344 (Vol 41), Issue the Failing Commands and the Associated Counts
Use the Commands, Flags, and Counts from Previously Logged Data of Original Failing Job
Select All Macro Diagnostic Tests for the Control Unit and Device, and Run Them in the Prescribed Order
Set Up to Catch CPU Checks, Certain Selector Channel Errors, and ROAR Stop on Program Checks
1. Check Control Switch to Stop
2. Address Compare Switch Switch to Early ROAR Stop
3. Compare Address Switches (ABCD) to WX Address 0147
Clear Log Out Area and Rerun Original Failing Job. If Same Failure Persists, Call for Assistance



DT Chart E Operators Console Check Out (Sheet 1)



DT Chart E Operators Console Check Out (Sheet 2)



DT Chart F 1400 Compatibility Oriented (Sheet 1)

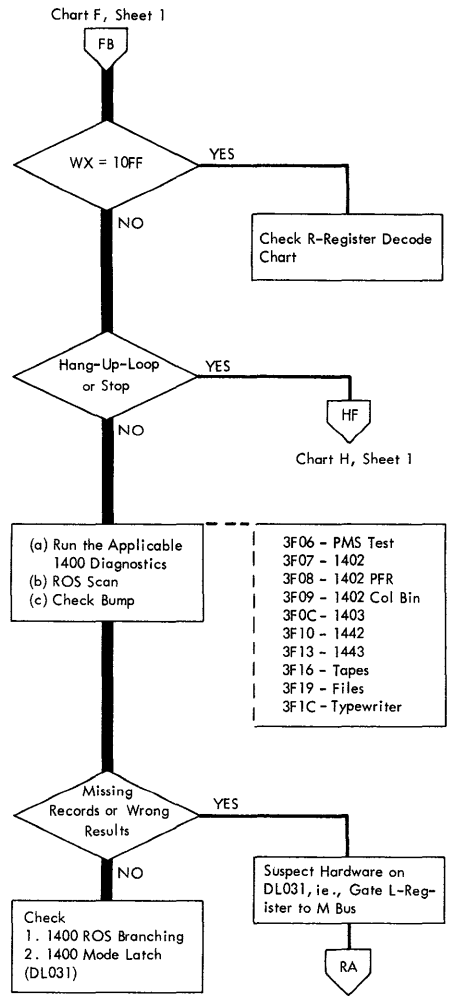


Chart F, Sheet 1
FB
WX = 10FF
YES
NO
Check R-Register Decode Chart
Hang-Up-Loop or Stop
YES
NO
HF
Chart H, Sheet 1
(a) Run the Applicable 1400 Diagnostics
(b) ROS Scan
(c) Check Bump
3F06 - PMS Test
3F07 - 1402
3F08 - 1402 PFR
3F09 - 1402 Col Bin
3F0C - 1403
3F10 - 1442
3F13 - 1443
3F16 - Tapes
3F19 - Files
3F1C - Typewriter
Missing Records or Wrong Results
YES
NO
Suspect Hardware on DL031, ie., Gate L-Register to M Bus
RA
Check
1. 1400 ROS Branching
2. 1400 Mode Latch (DL031)
Chart R, Sheet 1

On all stops at ROS address 10FF, a coded digit is displayed in the Main Storage Data Register. In the case of a set IC operation, the contents of the main storage location to which the instruction counter has been set are displayed. In the case of a sense switch operation, the resulting sense switch byte (98 of Aux. Stor. A) is displayed. In all other cases, the displayed digit has the significance shown in the R-Register Decode chart.

In addition to the coded digits which are detailed below, the following 1400 addresses are available on a 10FF halt.

(1) The decimal instruction address is displayed in the BA-registers.

(2) The decimal A-storage-address register is displayed by the MSDR lights.

(3) The decimal B-storage-address register is contained in the U-and V- registers and must be displayed manually.

The hexadecimal equivalents of these storage-address registers are also available and can be obtained by displaying the following Aux. Stor. A locations:

(1) The hexadecimal 1400 instruction address in locations 88 and 89.

(2) The hexadecimal 1400 A-storage-address register in locations 8A and 8B.

(3) The hexadecimal 1400 B-storage-address register in locations 8C and 8D.

The S-register is stored in byte 8F of Aux. Stor. A. If either S6 or S7 or both S6 and S7 equal 1, the respective 1400 storage-address register, A or B or both A and B, is displayed in hexadecimal rather than decimal form. A 1 for S6 or S7 denotes an invalid address for addressing storage. No hexadecimal-decimal conversion is attempted on an invalid address. For example: M%U1500R; - the contents of the A-storage-address register (%U1) is considered an invalid A-address.

FC Chart H, Sheet 1

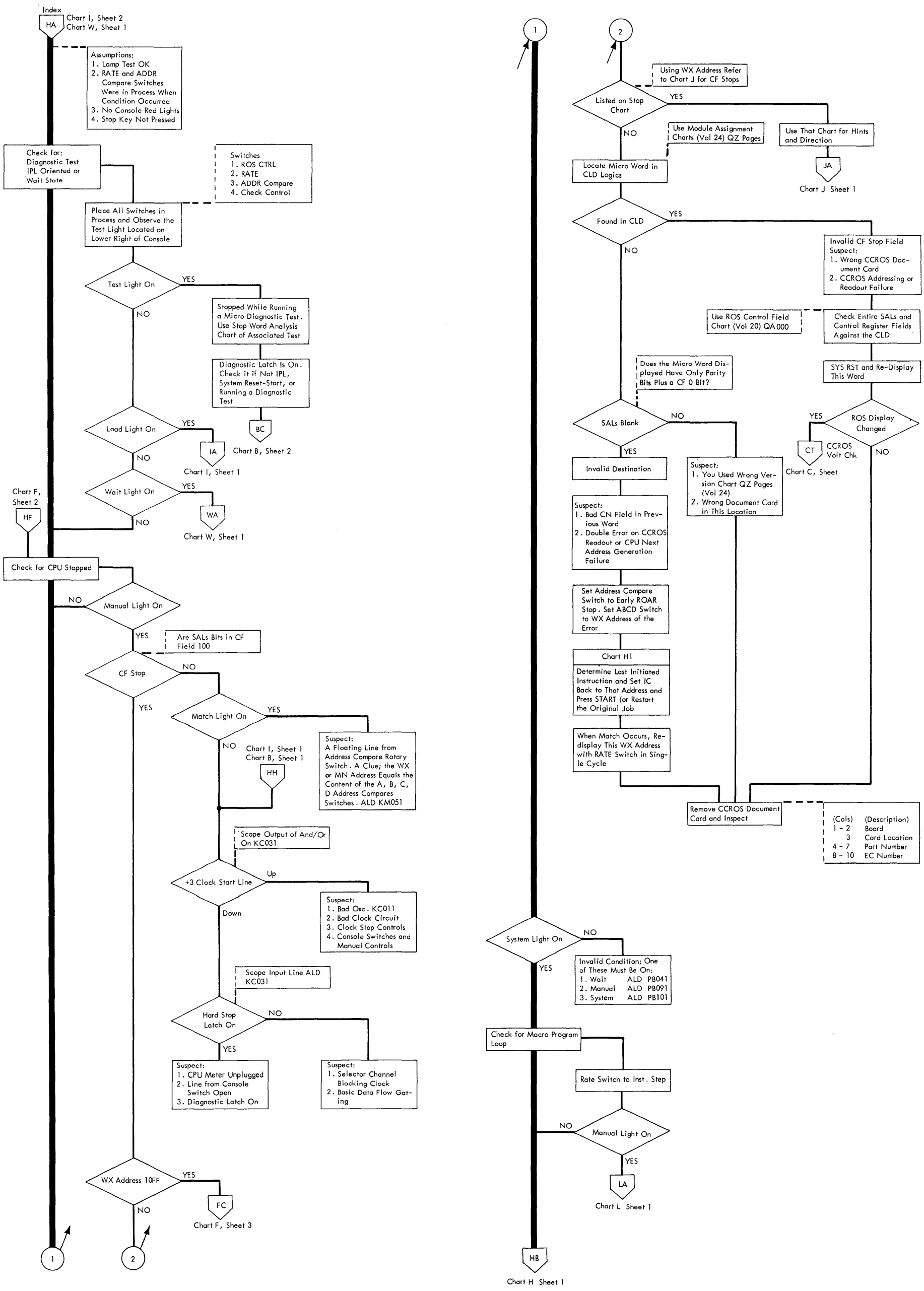
R-REGISTER DECODE CHART

Digit Displayed In MSDR	Reason For Halt	Comments
00	Normal stop. Appears when the stop is caused by pressing the stop key, ending an instruction executed in instruction-step mode, or a match occurs in SAR Delayed-Stop mode.	
01	The program attempts to use an invalid 1400 B-address.	The address displayed in the BA-register lights is the address of the next instruction character which has a word mark. Working back from this next instruction, assemble the failing instruction and attempt to determine why the B-address was invalid. Use a program listing if one is available. Was the instruction read into storage improperly?
02	The program attempted to use an invalid 1400 A-address.	Same comments apply as for character 01 halt.
04	The program attempted to use an invalid 1400 operation code.	The decimal address displayed in the BA-register lights is the address of the next character with a word mark. Working back from this address, determine the failing op-code. From a program listing, attempt to determine what the op code should be. Also investigate for a misplaced word mark.
05	An invalid I/O operation was attempted; either the unit selection or the unit number was invalid.	Check the A-field of the previous op-code. The address of the previous op-code should be 7 less than the address displayed in the BA-lights. This halt identifies a problem with the hundreds and/or units position of the A-field. In the case of M%U1500R, the difficulty would be with the U or the 1.
06	A storage-wrap condition occurred when an address outside of the system capacity was used to address core storage.	Check the op-code to ensure that valid addresses are being used. If these addresses are valid, check the storage size as defined in the CID. Cards 0320, 0390, 0420, 0500, and the last card of the IBM Standard CID contain references to storage size. If these addresses are invalid, attempt to determine what the address should be from a program listing.
07	Storage protection occurred in 1400 mode.	Check the Q-register. Bits 0 through 3 should be either 0000 or equal to bits 4 thru 7. If these bits do not compare as indicated above, check the protection key in the last loaded PSW. This key must be equal to Q-register bits 4 thru 7. If these two differ, call for programming assistance. Check that the conditions specified by the last loaded PSW exist while the machine is operating in 1400 mode. If the key in the PSW is 0000 or equal to bits 4 thru 7 of the Q-register and this halt occurs, a hardware malfunction has probably occurred. See Chart P-PE (Storage Protection).
08	An attempt was made to switch to 2030 mode without the PMS feature. May also be caused by erroneous interrupts.	Check the PMS control bytes for proper definition. Bytes 9C and 9D of Aux. Storage A contain bits that define the program-mode-switch subfeature. If the feature is not installed on the machine, these definition bits must be zero. The bytes are 9C / 9D 0. / Mode Sw On Inv I/O Ops 1. / Mode Sw On Console Ops 2. / Mode Sw On Printer Ops 3. Mode Sw On Inv Ops / Mode Sw On Rdr/Pch Ops 4. / 5. Mode Sw On Halts / Mode Sw On Tape Ops 6. / Mode Sw On File Ops 7. Mode Sw On Error Stops Also check if an erroneous interrupt is forcing a branch to word 1102 (CAS logic page QE601). ROAR stopping on this word and displaying the F-register indicates what type of interrupt has occurred. Note: All bits of the F-reg are normally on. Bit 0 being off indicates a timer interrupt has occurred. Bit 1 off indicates a console interrupt. Bits 2-7 indicate that an external interrupt has occurred.
09	An invalid source or destination address was specified on one of the following special 2030 PMS instructions: CFMT - 0E R1,R2 - COMPAT FEAT MOVE TO CFMF - 0F R1,R2 - COMPAT FEAT MOVE FROM CFLT - 0C R1,R2 - COMPAT FEAT LOAD TO CFLF - 0D R1,R2 - COMPAT FEAT LOAD FROM	The third byte of the source and or destination address is non-zero. The next Basic 2030 instruction should be stored in Basic 2030 LS A9 and AA. Working back from that address, check the specified registers to determine why the addresses are invalid.
0A	The microprogram attempted to convert to BCD an address that was less than the bias address. This occurred during execution of a clear-storage or store-address-register operation.	This situation usually appears when the execution of an operation is attempted where the A- and/or B-fields are obtained from the backup locations; for example, M H aaa. When execution of the Move operation is attempted, the A- and B-addresses are fetched from LT and UV backup locations. These addresses are in hexadecimal format. When the clear-or store-star operation is attempted, these addresses are converted to BCD. If the address is less than the bias, the 0A-halt occurs. When the PMS feature is installed, the programmer can alter these locations. Therefore, checking the 2030 op-code which can access these locations may point to the error. These op-codes are of the SI format: 99 | W1 | W2 | B1 | D1
0B	Storage wrap low; the 2030 storage location 1 less than 1400 000 was addressed.	The BA-register may be invalid at this halt, ie., it may not contain the decimal address of the next instruction. If this is the case, repeat the job and ROAR stop on word 1002. When a match occurs, the next instruction address may be obtained by displaying bytes 83 and 84 of Aux. Storage A. Working back from this instruction, determine the failing operation. Suspect misplaced wordmarks.
0E	The program attempted to index without advanced programming being defined by CID.	Check bit 1 of byte 9C in Aux. Storage A. This bit should equal 1. Card 0390 of the standard CID contains this definition.
11	Some device other than the 1050 attempted to take a multiplexor-channel data-cycle while preparing to enter the 1050 data loop.	While waiting for TREQ to come up, another device sent its address in an attempt to take a data cycle. CAS logic page QG121, ROS word 1944 detects the Address-In signal. This routine is normally used to stack any outstanding status so that the channel is free to operate with the 1050. Check to ensure that this data-transfer request is not from a device which was initiated in Basic 2030 mode prior to a mode switch to 1400 mode. This is defined as an invalid operation in the PMS portion of the IBM System/360 Model 30 1401/1440/1460 Compatibility Feature Systems Reference Libary. If the operation was initiated in 1400 mode, a hardware problem probably exists with the device whose address was sent in. Also check that the proper signals are received by the device which was forced to stack its status.
21	A word mark was missing from the 1400 op-code during I-Cycles.	Usually occurs when a branch is made to a location not containing a word mark. The decimal BA-address points 1 beyond this location. There is no easy method to determine the branch from address. Several steps which may be taken in order to further define the problem include: (1) SAR stopping on the location to which the branch has occurred to determine how it is changed during program initialization and execution. (2) Determine the operation when the failure occurs (perhaps through observing an I/O operation prior to the failure) and then operating in instruction mode to pinpoint the failing instruction.
22	A wrong address was sent back from the channel during initial selection of a tape operation.	Restart the operation. If tapes are on the multiplexor channel, ROAR stop on address 1AA0 (CAS logic page QG761). The desired unit address can be found in the D-register. Execute the next micro word 1AA4; this sends Address-Out. Check the TCU to determine that the proper address was received. Place rate switch to process mode and early ROAR stop on word 1A93. If entry to 1A93 is via 1A92, Address-In came up. This address may be determined by displaying F1. If this address is different than the contents of the D-Register, a TCU problem probably exists. If entry to 1A93 is via 1A41, an invalid channel condition exists; for example: Op-in and Select-In up simultaneously. If an address-mismatch condition does not exist at this time, single-cycle through the next several words to ensure that the proper address-compare branch takes place in word 1A98 or 1A99. If tapes are on a selector channel. ROAR stop on word 1A94 (CAS logic page QH021). The desired unit address can be found in the MSDR. This address is sent out to the TCU with the execution of ROS word 1A97. In word 1AA0 the address sent from the channel is compared to the address sent out. The address-compare branch takes place in word 1AA2.
23	GMWM in first position of tape write field.	A tape write command was issued. The first character to be written was a GMWM, which terminated the operation. Check the first data location to determine if there actually was a GMWM in this position. The decimal address in UV at this halt points 1 beyond the GMWM location. The B-field of the previous op-code points at the first data location. Determine how this GMWM was inserted in this field. Suspect tape drive failure or invalid programming. If the same situation were to occur on a 1400 system, the tape drive would have 'run away'. Check that this is not a delibertate operation by the customer.
31	A word mark was detected in the A-address of an I/O instruction, for example: M%U1500R	SAR stops on the main storage location containing the erroneous word mark. Determine when and why it is being set. Remember when SAR-stopping in compatibility mode, the hexadecimal Basic 2030 main storage address must be used rather than the 1400 decimal address. This can be obtained by performing a set IC operation to the decimal address and reading the hexadecimal address in the MN-register lights.
3F	A 2540 or 2501 reader error, a 2520 PFR error, or an invalid character has occurred.	Check the read-in area (001-080); any invalid characters have been replaced by a blank. Check the last card in the stacker for an error. If no invalid character has occurred, then unit check has been sent with the channel-end status from the reader; this means that an equipment-check condition, such as a hole-count error, has been detected.
41	An 8F character was detected at an address other than the bias address while in 1400 mode. For a 65K machine, this may indicate a 1400 high-wrap condition because 256 8F characters are placed between the upper limits of 1400 storage and the highest core address.	Detecting this character while in 1400 mode forces a microprogram trap to ROS word 1002. The displays at WX = 10FF cannot be guaranteed with this halt. In order to determine the location of the 8F character, check the BA-address and determine if it contains a valid address. Is there a word mark in the BA-address location? If BA contains a valid instruction address, determine what the failing op-code was; this may define the storage areas where the 8F was detected. Also check the A and B stars; these may point directly at the BF character or 1 position on either side of it. If these methods fail, ROAR stop on word 1002. When a match occurs, the failing location is displayed in the MN lights in hexadecimal form and the previous instruction address is in bytes 88 and 89 of Aux. Storage A (in hexadecimal). Once the failing address is known, SAR stopping on this should point out how the 8F was generated. It may occur as a result of a disk-out-of-sync condition or it may be read in via a Basic 2030 prepared tape where 8F is a valid character.
42	Invalid channel status was detected following a tape-read operation (Selector Channel only).	ROS word 1A30 gates the GJ-assembler containing the channel status on to the Z-bus. The following word branches on Z = 0; if Z is non-zero, this halt occurs. The bit configuration of GJ at word 1A30 is: 0 - Program controlled interruption 1 - Incorrect length 2 - Program check 3 - Protection check 4 - Channel data check 5 - Channel control check 6 - Interface control check 7 - Chaining check If this halt occurs while operating in 1400 mode, a channel hardware problem probably exists. Check the selector channel chart. Chart S at SA.
4F	1442 Reader or Punch intervention required.	This stop indicates that a Not Ready condition exists at the 1442. This condition usually results from: (1) an empty hopper (2) a full stacker, or (3) an open cover.

Digit Displayed In MSDR	Reason For Halt	Comments
51	The program attempted to perform an I/O operation on a device for which the compatibility feature is not installed.	Working back from the BA-address, determine what the invalid operation is, for example, M%Y1201W for a machine with 1402/1403 subfeature. If this occurs while running a diagnostic test, check the TAD(s) to determine that the proper types of I/O devices are described. If this occurs while loading CID, the IJ backup locations that point to the first 1400 instruction may be erroneously set. Columns 28 and 29 of card 0380 specify the Basic 2030 main storage locations from which the first 1400 instruction is read. This instruction is contained on card 00A0 or 00B0 of the CID and is loaded into the 2030 main storage. If the halt occurs while attempting a 1729, 1402, or 1442 load, the card-load or tape-load IJ address specified in bytes 90 through 93 of Aux. Storage A may be erroneously set. These locations are used to set IJ when 1729, 1402, or 1442 load is attempted. These locations should contain the addresses of a card-read or tape-read instruction located in Basic 2030 storage. These addresses are loaded from card 0390 and are contained in columns 6, 7, 8, and 9 for card load and 11, 12, 13, and 14 for tape load.
52	A device-end signal was received before a GMWM was encountered on a tape-write operation. This halt can occur on both selector and multiplexor channels.	This is probably a tape-drive or control-unit problem. If tapes are on a selector channel, refer to CAS logic page QH071. Word 1763 branches on Status-In and Service-In. If Status-In occurs before the group-mark word-mark, which normally terminates the operation, this error halt occurs. If tapes are on the multiplexor channel, refer to CAS logic page QG791. Word 1A40 or 19C4 branches on Status-In and Service-In. Do not attempt to ROAR stop on a word containing the Status-In, Service-In branch; these are part of the data loop and cause overrun conditions, etc., when the match occurs.
55	A 1400 start reset function was performed.	
62	For tapes on the selector channel, this stop means that Status-In and Service-In came up at the same time during a tape-write operation.	This is probably a TCU problem. CAS logic page QH071 contains the word where the branch is made.
62	For tapes on the multiplexor channel, this stop means that the TCU disconnected during a tape-write operation.	This is probably a hardware problem. ROS word 1A40 or 19C4 (CAS logic page QG791) contains the branching conditions which detects this failure. Taking the 1,1 branch does not mean that Status-In and Service-In came up simultaneously, but rather that Op-In dropped. Check the applicable hardware on ALD pages FA092 and FA041. Also refer to Chart D at DA.
7F	The program has issued a stacker-select command to a 2540 more than 6 ms after the previous card-read instruction was issued.	Check the program to determine if a lengthy I/O op was issued between the Read command and the stacker select. Also check the 2821 to ensure that the attention bit is sent to the processor during the 6 ms provisional feed time.
80	If this halt is used in conjunction with the 1403/2540 or 2501/2520/1403, it means either that there was no address compare (Address-In was not the same as Address-Out) or that a punch-transfer error occurred.	Early ROAR stop on word 1892. If the previous address displayed is 181B, a punch-transfer error has occurred; that is, an error occurred while filling the punch buffer. It can either be a Bus-Out check or an error internal to the punch which would result in bad parity data being transferred into the buffer. If the previous address was either 1896 or 1897, a no-compare condition exists between Address-Out and Address-In. This is probably a hardware problem in either the channel or the device. Check that the proper address was sent out and received by the device. Address-Out is sent during the execution of word 1801 (CAS logic page QG531). Also check the address sent in to verify the comparison and branch executed by the microprogram. The address compare is made in ROS word 1898 (CAS logic page QG531) and the branch is made in the following word.
80	When this halt occurs on a machine that has the 1442/1443 compatibility subfeature installed, one of the following situations has occurred: (1) A no-compare condition exists between Address-Out and Address-In. (2) A data-transfer error has occurred during a printer operation. (3) The print field was not terminated by a GMWM.	Repeat the operation and ROAR stop on ROS address 188A (CAS logic page QG261). If a match occurs, Address-In does not match Address-Out. The address sent out is contained in R-Register in its crossed form at this point. The address sent in can be displayed in FI. This is probably an I/O hardware problem. Check that Address-Out is properly received and decoded by the device; Address-Out is sent in word 1821 (CAS logic page QG311) and the address comparison is made in ROS word 1887 (CAS logic page QG301). If a match does not occur, there has been an error during data transmission, a unit check has occurred at channel end. This is probably either a Bus-Out error or a device error associated with receiving the data. This stop is set up on CAS logic page QG351 word 1842. Also, check if a GMWM (0F Hex) is in the print field; the absence of this character can also result in a unit check at channel end.
82	For tapes on the selector channel, this stop means that Status-In and Service-In came up simultaneously on a read-move operation.	This is probably a TCU problem. CAS logic page QH081 contains the word where the branch takes place.
8F	Tape-unit intervention is required for tapes on the multiplexor channel or on the selector channel. At this halt, IJ has been decremented to the op just attempted. BA points to this decimal address. Pressing START allows the operation to be tried again.	Unit check is in the status response to Command-Out during initial selection. Check that the TCU is on-line, that the desired tape drive is ready, that Aux. Storage properly defines the drives and control unit. (See the description for the 92 halt for proper definition), that a write operation is not being attempted on a file-protected drive.
90	The program has attempted to use an invalid d-modifier on a 1442/1443 operation.	Check the program residing in core storage to determine if the d-modifier is actually valid. If it is invalid, attempt to determine how it was introduced into the instruction stream. If it is valid, check the microprogram decode. The stop code is set in ROS words 1816, 188B and 1893 (CAS logic page QG261).
90	Operational-In disconnect on 2540 or 2501 reader.	Op-in dropped during a read operation. This is probably a hardware problem. ROS word 18CD (CAS logic page QG561) contains the branching conditions which detects this failure. Taking the 1,1 branch does not mean that Status-In and Service-In came up simultaneously, but rather that Op-In dropped. Check the applicable hardware on ALD pages FA092 and FA041. Also refer to Chart D at DA.
92	A tape error occurred on a tape initial program load.	A unit check is contained in the read ending-status of a 1729 tape load. This end status can be located by displaying FI after executing word 1A46 (CAS logic page QG802) when the tapes are on the multiplexor channel. When the tapes are on the selector channel, this ending status is displayed in GR following the execution of word 19D5 (CAS logic page QH081). When performing a tape IPL (1729 in switches FGHJ--Press SYSTEM RESET - ROAR RESET - START), the machine is forced to ROS word 1729 (CAS logic page QE521). This routine loads IJ-backup with the contents of tape-load-IJ (bytes 92 and 93 of Aux. Stor A). The instruction located at the address specified by tape-load-IJ is L%U1001R__ and is read into the machine from card 00A0 of the CID. After performing a start-reset function, the microprogram IJ-backup is loaded into IJ, and I-cycles are entered. After completing the read, IJ is forced to 1400 storage location 001 and processing of the data just read begins. Check that this is done correctly if the 92 halt occurs. Also check that the proper drive assignments have been made. Byte 81 of Aux. Stor. A must properly define the Basic 2030 drive containing the initial program: Bits 0 and 1 00 - 7-track @ 200 bpi 01 - 7-track @ 556 bpi 10 - 7-track @ 800 bpi 11 - 9-track Bits 2 and 3 should be zeros. Bits 4 - 7 contain the Basic 2030 drive number which is to be assigned as 1400 drive #1. Bits 4 - 7 of Byte 80 of Aux. Stor. A contains the TCU address. In addition, bytes 97 and BB of Aux. Stor. A contain 7- or 9-track status information and must be initialized as follows: Bit 0 of each byte has 7- or 9-track status for tape unit 0; bit 1 of both bytes is used for this status for tape unit 1, etc. If a bit of the first byte (position 97) is set to 1, the associated tape unit is equipped with 9-track read/write facilities. The unit is a 7-track drive if the associated bit in position 97 is set to 0. If the corresponding bit of the second byte (position BB) is set to 1, the associated tape unit is a 9-track phase-encoded drive with density set at 1600 bpi. If this bit is set to 0, the associated tape unit has a density setting of 800 bpi and is either a 7-track or 9-track unit.
A0	An Operational-In disconnect occurred during a 1403 print operation.	Op-in dropped during the data-transfer portion of a print operation. This is probably a hardware problem. ROS word 18BC (CAS logic page QG551) contains the branching conditions which detects this failure. Taking the 1,1 branch does not mean that Status-In and Service-In came up simultaneously, but rather that Op-In dropped. Check the applicable hardware on ALD pages FA092 and FA041. Also refer to Chart D at DA.
A0	There was no GMWM in storage to terminate a 1442 read operation.	On a 1442 read operation, a GMWM (0F hex) is required to terminate the operation. Manually check the read-in area for this character; if there is a GMWM in read-in area, this is probably a hardware problem with the GMWM detection latch (ALD page MB031). If this halt occurs after mode switching from Basic 2030 mode to 1400 mode during initialization, check CID card 0384, columns 28 and 29 and card 0390, columns 8 and 9. These columns should each contain AD. Also check card 37. For non-65K mach, columns 18 and 19 should be 09. For 65K machines, check card 38, columns 18 and 19. These should also contain 09. These cards cause a GMWM to be inserted in storage location 0082 of 1400 storage when compatibility mode is initialized via the 99 op code.
A2	Invalid selector-channel status was received on a 1400 branch-if-tape-error instruction.	Non-zero channel status was sent back from the channel on a TIO; Word 1A12 gates channel status on to the Z-bus (QH111). This is probably a channel hardware problem. Also check that the proper command was sent to the channel. Command-Out is sent during the execution of word 1AA4 (CAS logic page QH021). The command byte sent should be 00. Word 1AA9 (CAS logic page QH021) should reset GR prior to issuing Command-Out in word 1AA4. Check the selector channel chart (Chart S at SA) for additional assistance.
B0	An Operational-In disconnect occurred during a 2520 or 2540 punch command.	Op-in dropped during the data-transfer portion of a punch operation. This is probably a hardware problem. ROS word 1820 (CAS logic page QG521) contains the branching conditions which detects this failure. Taking the 1,1 branch does not mean that Status-In and Service-In came up simultaneously, but rather that Op-In dropped. Check the applicable hardware on ALD pages FA092 and FA041. Also refer to Chart D at DA.
B0	A printer error on a print operation or a 1442 error on a read or punch operation has been detected.	If on a read command, this signifies either an equipment check or an invalid card code. For the punch command, this halt identifies an equipment-check condition. ROAR stopping on word 1877 (CAS logic page QG281) allows displaying the sense byte in the G-register. The sense byte makeup is: 0 - Command reject 1 - Not ready 2 - Bus-Out check 3 - Equip check (a) reader check (b) punch check (c) invalid card code punched (d) data error at channel end 4 - Data Check - invalid card code on read 5 - Overrun check If performing a print operation, the sense byte may be displayed in the G-register by ROAR stopping on word 1876 (CAS logic page QG361). The sense byte content is: 0 - Command reject 1 - Intervention required--printer not ready because forms check, stop key, or carriage-stop key pressed , or cover interlock open. 2 - Bus-Out parity check 3 - Equipment check 4 and 5 - Typebar selection 6 - Channel 9 7 - Channel 12 If a 1403 is operated with the 1443 microprograms, the sense byte is: 0 - Command Reject 1 - Intervention Required--Not Ready 2 - Bus-out Parity Check 3 - Equipment Check--Parity Error in CU or device 4 - Data Check 5 - Not Used 6 - Channel 9 7 - Channel 12

Digit Displayed In MSDR	Reason For Halt	Comments
B2	Status-In and Service-In occurred simultaneously on a 1400 read-load operation, for example: L%UXBBBR This halt is valid only when tapes are on the selector channel.	ROS word 1A63 (CAS logic page QH091) has this branch. Both Status-In and Service-In up at the same time probably indicates a channel or device hardware problem. Also check the set and reset of S4 and S5. These are the status indicators on which the branch is made. Use the selector channel chart (Chart S at SA) for checking the channel.
C2	Operational-In disconnect on a multiplexor channel tape-read operation.	Op-in dropped on a tape-read operation. For a read-move operation, the branch is found on CAS logic page QG801; for a read-load operation (page QG802). This is probably a channel or device hardware problem. Also check the Status-In and Service-In branches. Taking the 1,1 branch does not mean that Status-In and Service-In came up simultaneously, but rather that Op-In dropped. Check the applicable hardware on ALD pages FA092 and FA041. Also refer to Chart D at DA.
CE	This halt indicates that a premature data disconnect occurred on a read operation. Pressing the start key causes processing at the next sequential instruction but loses the record just read. To re-read, the operator must set the instruction counter to the address of a backspace-re-read routine.	The following conditions have occurred when this halt is reached: (1) Unit check in read end-status. (2) 12 or fewer characters have been transferred into storage. (3) The noise bit has been set in the TCU and has been recognized as bit 0 of the 2nd sense byte sent from the TCU. The noise bit being turned on implies that after the data-disconnect additional bits were found before the IRG was detected. Tape movement was continued until an IRG was recognized. Therefore, the data encountered after data transfer was halted has been skipped over. This halt generally indicates a problem with the tape drives. Check the following: (1) IRG (2) Start/Stop adjustment (3) Dirty idlers/prolays (4) Ungrounded or improperly grounded drives.
CF	1050 intervention is required.	Check for an out-of-paper, power-off, or off-line condition. Bit 5 of the 1050 tags indicates this intervention-required condition. These tags are gated to the G-register in ROS word 1946 (CAS logic page QG121). Branch on G5 to check for the intervention-required condition (CAS logic page QG141 word 197A).
D2	A microprogram initiated sense operation was prematurely ended. This halt can only occur if tapes are on the multiplexor channel.	This is probably a hardware problem. ROS word 1A8D (CAS logic page QG781) contains the branching conditions which detects this failure. Taking the 1,1 branch does not mean that Status-In and Service-In came up simultaneously, but rather that Op-In dropped. Check the applicable hardware on ALD pages FA092 and FA041. Also refer to Chart D at DA.
E2	Operational-In disconnected on a microprogram-initiated mode-set operation with tapes on the multiplexor channel. This mode-set command is issued in order to send the track-in-error byte previously stored to the TCU.	ROS word 1A6C (CAS page QG781) contains the Status-In and Service-In branches for the track in-error mode-set command. If Op-In drops, this error halt occurs. This is probably a channel or device hardware problem. Taking the 1,1 branch does not mean that Status-In and Service-In came up simultaneously, but rather that Op-In dropped. Check the applicable hardware on ALD pages FA092 and FA041. Also refer to Chart D at DA.
F0	A 1400 halt instruction has been properly executed.	Not an error halt.
F1	A 1400 halt instruction with an invalid B-address has been successfully executed.	Not an error halt.
F2	A 1400 halt instruction with an invalid A-address has been successfully executed.	Not an error halt.
F3	A 1400 halt instruction with an invalid A- and B-address has been successfully executed.	Not an error halt.
FF	A 1400 halt-and-branch instruction has been properly executed.	Not an error halt.

Digit Displayed In MSDR	Reason For Halt	Comments
10	Read-back check stop. A disk write instruction was followed by a disk instruction other than a read-back check.	If the I/O stop was caused by operator intervention, press SYSTEM RESET to clear the read-back check interlock, set IC to the beginning of the write operation, and press START to continue processing. If the I/O stop is caused by programming--a write disk without a subsequent read-back check--the program is invalid and should be corrected.
20	Channel-end or device-end not received during ending status.	This condition is tested for on QH381, location J3. At this time, a 2030 disk command should have been completed, and ending status posted by the file control unit. Ending status was detected at location J1 on QH381. The last 2030 disk command issued can be read from the B Aux. Storage XXBE. To recreate the 1400 disk operation that led to this coded stop, find the address of the next sequential instruction displayed in the B-star and A-star registers. The beginning of the disk instruction is this address minus 8. It is necessary to set up the disk control field correctly each time before executing the 1400 disk operation. To set up the disk control field prior to executing the operation, a disk control field can be moved into its working location with a move data or load data op-code. Note: If the disk operation is a multi-sector operation, a microprogram stop at the J3 location (QH381) causes time disorientation. It is necessary to reset and restart at the beginning of the disk operation.
30	Wrong address sent back from the channel during initial selection.	This stop is probably caused by a hardware malfunction in the multiplexor channel bus cabling or associated hardware. A test I/O instruction to the 2311 in question can be used to determine if the problem exists in Basic 2030 mode. The 2841 file control unit hardware that receives the Address-Out from the processor is located on page GA071 (2841 ALD Page). The 2841 FCU initial selection microprogram is on QB010. During initial selection, the microprogram moves from location E2 to A6, where Address-In is raised. It is possible to single-step both the processor and the 2841 microprograms through the initial selection sequence. The disk compatibility initial selection microprogram is on page QH341 (2030 CLD Page), locations G5 through L8.
40	Unit-check status response to seek command, following address transfer.	This stop happens if the seek address sent to the file control unit is outside the range of addresses acceptable to the FCU. The address-transfer portion of a full seek is decoded to binary and stored in the B-auxiliary storage in addresses XXAD, E, F, and XXB0. The bytes stored in these locations for a seek operation are the CCHH values. The highest legitimate value that can be stored, is hex 00 CB 00 09, which represents cylinder 203, head 9. If for any reason, a previous read operation placed non-zero values in addresses XXAD or XXAF, which were not removed by a built-in microprogram housekeeping program, the seek check can be removed, as an interim measure, by manually performing the following steps: (1) Note the B-and A-reg display of the 1400 program next address. (2) Press SYSTEM RESET to clear 2841 microprogram notation. (3) Set the processor to 1400 mode. (4) Set IC to I-next minus 8. (5) Press START to retry the seek operation. This type of stop has been eliminated for all known cases used by customer programs.
50	Operational interlock	This stop occurs when the control unit is disconnected from the processor, and the processor microprogram is at a microaddress, where it should be only when the two boxes are logically connected. The processor disk-compatibility microprogram can exit to the 50 stop from several places. This exit is taken whenever the processor microprogram is at a 4-way branch, waiting for service-in or status-in. If the control unit is disconnected, the 11 branch is taken to the 50-coded stop. During the execution of disk operations, the file control unit should stay connected until the operation is completed. The most probable time at which this stop can occur is when the disk compatibility feature is updated and a wrong EC level or incorrect CCROSS card is inserted. A wrong next-address in a microprogram block can put the microprogram into one of the 4-way branch blocks that leads to a 50-coded stop. It might be possible to correct this condition rapidly by checking the EC level and version of CCROSS cards installed during change activity. Another approach is to use EARLY ROAR STOP on the processor, and work back to the wrong CCROSS card. This approach is based on the assumption that 2030 disk diagnostics had run successfully, and that the file control unit is working correctly. Disk compatibility CCROSS cards are from location 79-0 to 84-7.
60	Module overflow detected. The disk module value in Aux. Storage B B011, 2, 3, 4, or 5 is different from the module value specified by the disk control field of the disk instruction.	(Limited Usage). Change disk packs, if program depends upon module overflow to indicate pack replacement. All others: Set B010 Aux. Storage B to 40 hex. Set IC to 1400 displayed address -8, press console START to continue. In the IBM System/360, Mod 30 1401/1440/1460, Compatibility Feature Manual, Form No. A24-3255, see Appendix F card 410 - Disk File Functions, to determine whether this stop can be disabled for customer application. See Appendix D, Storage B Byte 10 Bit 1 on Module-Overflow Detection usage. Most users can disable this stop, and must disable this stop if they use labels on drives other than drive 0.



DT Chart H Hang Ups, Loops, and Stops (Sheet 1)

Chart H, Sheet 1

HB

Single Word Micro Program Loop

Rate Switch to Single -Cycle

Log in Console - Use Image Sheet if Available

Press START

YES — New Address in WX — NO

Locate WX Word in CLD Logics

Use Module Assignment Charts (Vol 24) QZ Pages

Does CLD Show That This Word Can Loop On Itself?

Valid Loop — NO

Suspect:
1. Wrong Document Card in CCROS, Check Version
2. CH, CL, or CN Fields Punched Wrong or Decoded Wrong in CPU

YES

Read All General Comments at Top and Bottom of CLD, Under the Looping Word, and Each Preceding Block

Waiting for an Interface Tag in Compatibility Mode

1401 Interface Tag — NO

Suspect:
1. CPU Status Set or Reset Failure
2. Wrong CCROS Document Card, Match SALs and Control Register Fields Against CLD

YES

Suspect:
1. Interface (RCVRS and Terminators)
2. Channel or Control Unit
3. I/O Cable

Chart H1

Determine What Instruction Code Is Being Performed when Failure Occurred

Chart H1

Determine What Instruction Code Is Being Performed when Failure Occurred

Run in This Order
Resident
Basic Test(BFF) 3345 Vol 41
Repop
Priority Controls 3347 Vol 41

Try Any or All:
1. Statically Scope Interface Line from CPU to Control Unit
2. Repop Micro I/O Test 3344 (Vol 41) to I/O Unit
3. BFF Basic Test 3345
4. Multiplexor Micro Diagnostic or Selector Channel FLT
5. 2030 Macro Diagnostics to I/O Unit

1

1

Assumptions:
1. Console Logged
2. Manual Light On

Multiple Word Micro Program Loop

Locate the Last Logged WX Address in the CLD Logics

Use Module Assign Charts QZ Pages (Vol 24)

Read All General Comments at the Top and Bottom of the CLD as Well as Under the Micro Word

1. Press START
2. Log in WX
3. Read and Analyze Micro Word Comments and Functions
4. Look for Possible Exits from This Loop

For Aid in Diagnosis Use the CLF Flow Charts in the 2030 FEMDM (Vol 32)

Continue the above 4 Steps until a Significant Portion or the Complete Loop Is Logged

Check to See if You Are Taking a Continual Trap or Interrupt By ROAR Stopping on Each Trap WX Address

Refer to Traps in Priority Order in the 2030 CE Hand Book. If Passing Through ROS ADDR 0147 This Is a Program Interrupt Probably Caused By IPL to a Non-Ready Device, to a Device Which Does Not Send Any Data, or Sends Bad Data in First Card

I/O Oriented Loop — NO

Suspect:
1. CPU Status Set or Reset Failure
2. Wrong Next ROS Address Decode
3. Wrong Document in CCROS

YES

Suspect:
1. 1401 Compatibility, Control Unit Continually Answering Busy to Initial Selection
2. Suppress Out Not Functioning or Control Unit Not Stacking Status
3. Continual Multiplexor Selector Channel Trap
4. Wrong ROS Next Address Due to Bad CN Decode or Wrong Document in CCROS
5. CPU Status Set or Reset Failure

Chart H1

Determine What Instruction Code Is Being Performed when Failure Occurred

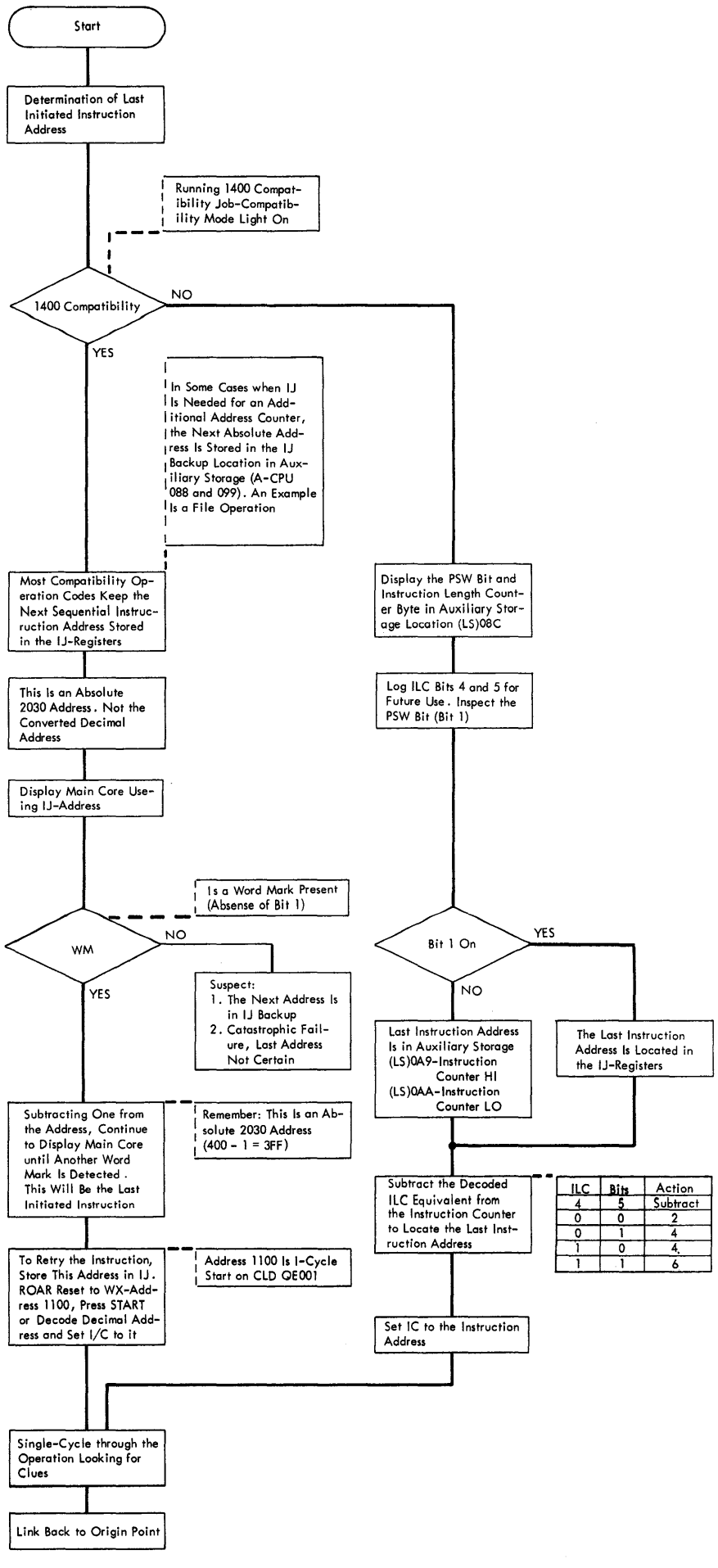
Chart H1

Determine What Instruction Code Is Being Performed when Failure Occurred

Run:
Resident
Basic Test(BFF) 3345 Vol 41
Repop
Priority Ctrls 3347 Vol 41

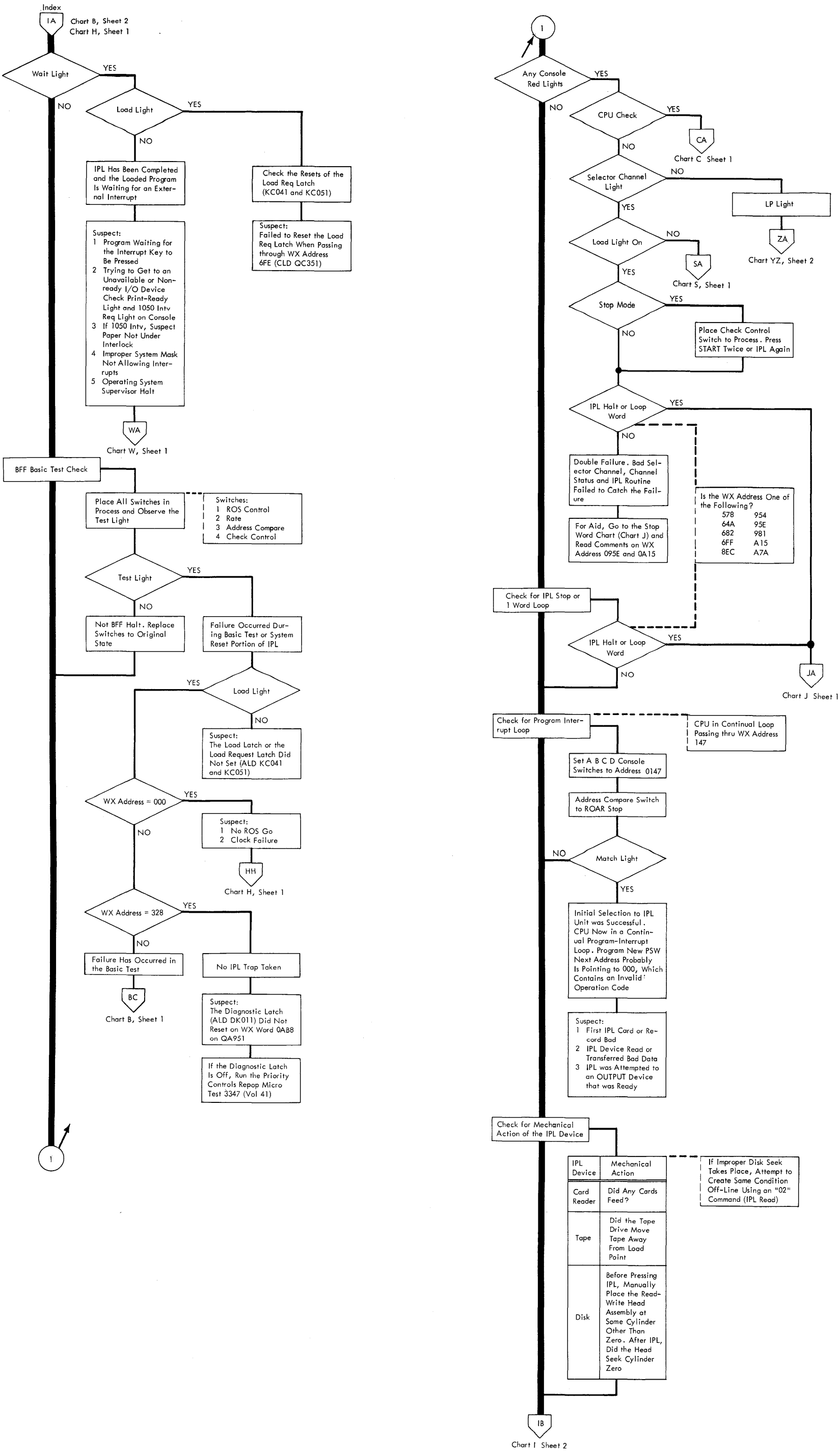
Run:
Resident
Basic Test(BFF) 3345 Vol 41
Repop
Priority Controls 3347 Vol 41
Multiplexor -
Repop or 3346 Vol 41
Selector Chan.
FLT Ch 1 3447 Vol 41
Ch 2 344A Vol 41

Try Any or All:
1. Repop Micro Test to I/O Unit
2. Macro Program Diagnostics to the I/O Unit
3. Hand Program to I/O Unit



ILC	Bits	Action
4	5	Subtract
0	0	2
0	1	4
1	0	4
1	1	6

DT Chart H1 Last Initiated Address



DT Chart I IPL (Sheet 1)

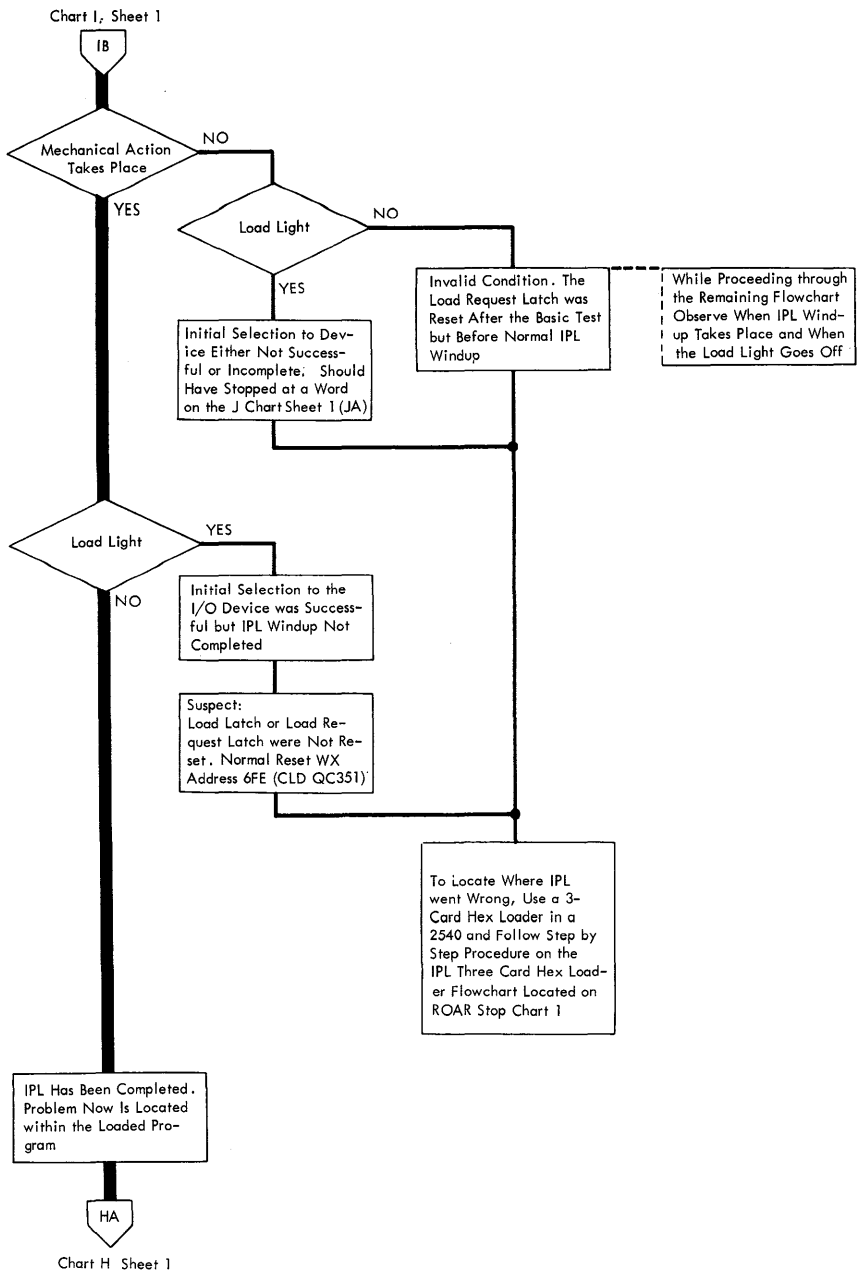


Chart I, Sheet 1
IB
Mechanical Action Takes Place
NO
YES
Load Light
NO
YES
Invalid Condition. The Load Request Latch was Reset After the Basic Test but Before Normal IPL Windup
While Proceeding through the Remaining Flowchart Observe When IPL Wind-up Takes Place and When the Load Light Goes Off
Initial Selection to Device Either Not Successful or Incomplete; Should Have Stopped at a Word on the J Chart Sheet 1 (JA)
Load Light
YES
NO
Initial Selection to the I/O Device was Successful but IPL Windup Not Completed
Suspect:
Load Latch or Load Request Latch were Not Reset. Normal Reset WX Address 6FE (CLD QC351)
To Locate Where IPL went Wrong, Use a 3-Card Hex Loader in a 2540 and Follow Step by Step Procedure on the IPL Three Card Hex Loader Flowchart Located on ROAR Stop Chart 1
IPL Has Been Completed. Problem Now Is Located within the Loaded Program
HA
Chart H Sheet 1

JA Index
Chart I, Sheet 1
Chart H, Sheet 1

Note 1: All CPU CF stops are listed except diagnostic test stops and 1620 feature stops.
* For additional aid in locating IPL failures, use a three-card hex loader in a 2540 and follow the step-by-step ROAR-STOP procedure on the IPL three-card hex loader flowchart located on ROAR stop Chart 1

WX ADDR	Type	CLD Page No	Normal Cause	Hints and Aids
00B2	Stop	QA961	A second machine check occurred with check control switch not in stop, before the first machine check could be logged.	Check control switch to stop; try again or go directly to CPU check. Chart C, Sheet 1 at CA
00FF	Stop	QA941	Soft stop occurred because STOP key was pressed. Rate switch was in instruction step, or match occurred using SAR delayed stop mode.	Check process stop latch on ALD KC081
0328	Stop	QA951	System reset followed by pressing the START key once -- basic test BFF has run successfully 128 times.	If IPL initiated, suspect the multiplexor channel. Trap was not taken at previous WX 00EA, best action run priority controls repop micro test 3447
0578	IPL Stop	QC091	Attempted to IPL to an unavailable or non-existent device on the multiplexor channel, Select-In received in response to Select-Out.	Suspect: * 1. Desired unit is off line 2. Desired unit does not recognize its address 3. Wrong address being sent out on channel Do: ROAR stop on ROS address 05A0 - QC051 Check Bus-Out and control unit statically
0649	IPL Stop	QC061	IPL was attempted to a non-ready device on the multiplexor channel.	Suspect: * Control unit answers busy to initial selection Do: ROAR stop on address 05AC, rate switch to single cycle, press START, A-Register now contains status from device.
0682	IPL Loop	QC351	1. During IPL on the multiplexor channel, the control unit failed to send Request-In or the CPU did not recognize Request-In, which is necessary to cause a multiplexor channel share request trap 2. First card read did not have proper IPL data or data read in was blank. This is one way of causing a program check that causes this loop	Suspect: * 1. If only one card fed into the stacker, suspect that it is not the proper IPL card 2. Request-In from control unit not getting to CPU. Check Request-In on ALD FA082 3. CPU failure to take multiplexor channel trap to WX 0010. 4. Operational-In appeared dropped to CPU 5. Reader clutch failed to energize Do: Run priority controls micro repop diagnostic test 3447 and multiplexor channel repop test 3346 (Vol 41)
06FF	IPL Stop	QC351	Bad final status received from source unit during IPL on the multiplexor or selector channel	Do: * Go to Chart J, Sheet 2 at JB
08EC	IPL Stop	QC511	IPL attempted using address assigned to the 1052 console KB-Printer	* 1. ROAR stop on WX Address 00EA - QA951 and IPL again - If no match, place rate switch to single cycle and IPL again, scope diagnostic latch on DK011. This latch is not on while executing basic test causing a premature IPL trap to 0002 2. If a match occurred in 1, ROAR stop on 053A - QC041 and single-cycle through address formation for clues
0954	IPL Loop	QD091	Selector channel wait loop, waiting for selector channel chaining trap or share cycles.	Suspect: * 1. CPU failed to take selector channel trap 2. Control unit failed to bring up Status-In or Service-In 3. Selector channel poll control problem Do: Run priority controls micro repop diagnostic test 3447 and selector FLT 3447 - 344A (Vol 41)
095E	IPL Stop	QD181	1. Initial internal channel status not equal to zero on selector channel IPL; or 2. Program check occurred during IPL on selector channel.	Do: * Go to Chart J, Sheet 2 at JC
0981	IPL Stop	QD011	1. Initial status from source unit during IPL on selector channel is non zero, or 2. IPL attempted to non existent or unavailable selector channel	Do: * Go to Chart J, Sheet 2 at JD
0A15	IPL Stop	QD121	Non-zero channel status detected at completion of IPL on the selector channel	ROAR stop on WX Address 0A01 - QD121, rate switch to single-cycle press START. R-Register now contains ending channel status *
0A7A	IPL Loop	QC451	1. A machine check occurred during IPL while check control switch was in process 2. A multiplexor channel control check occurred during IPL 3. Interface time-out occurred during IPL	Do: * Go to Chart J, Sheet 2 at JE
10FF	Stop	QE691	1401 Compatibility coded stop, R-Register hexadecimal character determines cause	Do: Go to Chart F, Sheet 3
12F4	Stop	QE561	1. Machine check occurred in Compatibility mode with check control switch in process; or 2. Second machine check occurred in Compatibility mode using mode switch on machine checks	Place in stop mode and catch error when it occurs, or go to Chart C, Sheet 1 at CA
1E4F	Stop	QG532	An RPQ operation (branch on next card column binary) was attempted but reader was not ready	Ready reader or ROAR stop on WX Address 1E4E - CLD QG532 and observe Status-In in multiplexor channel and control unit

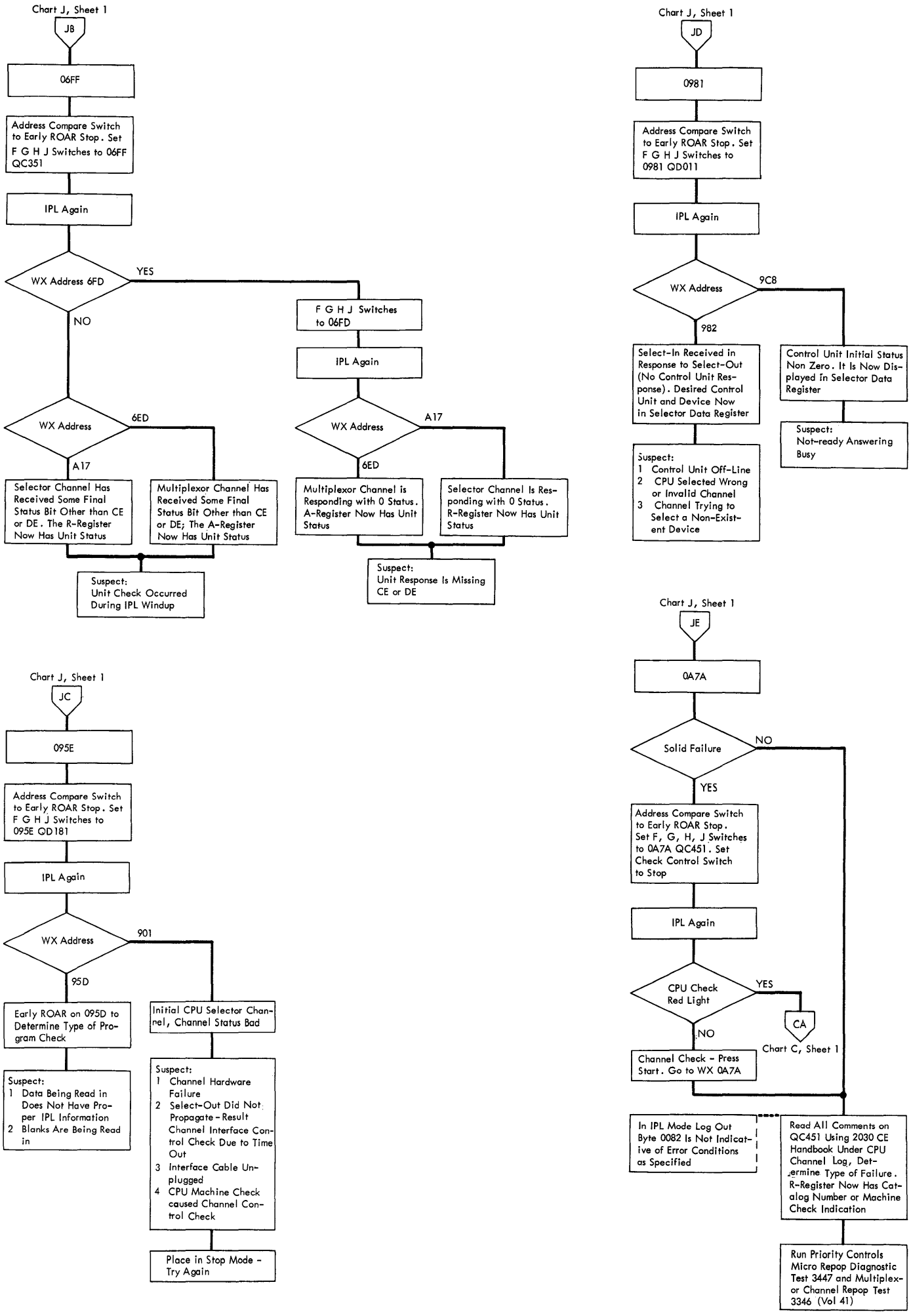
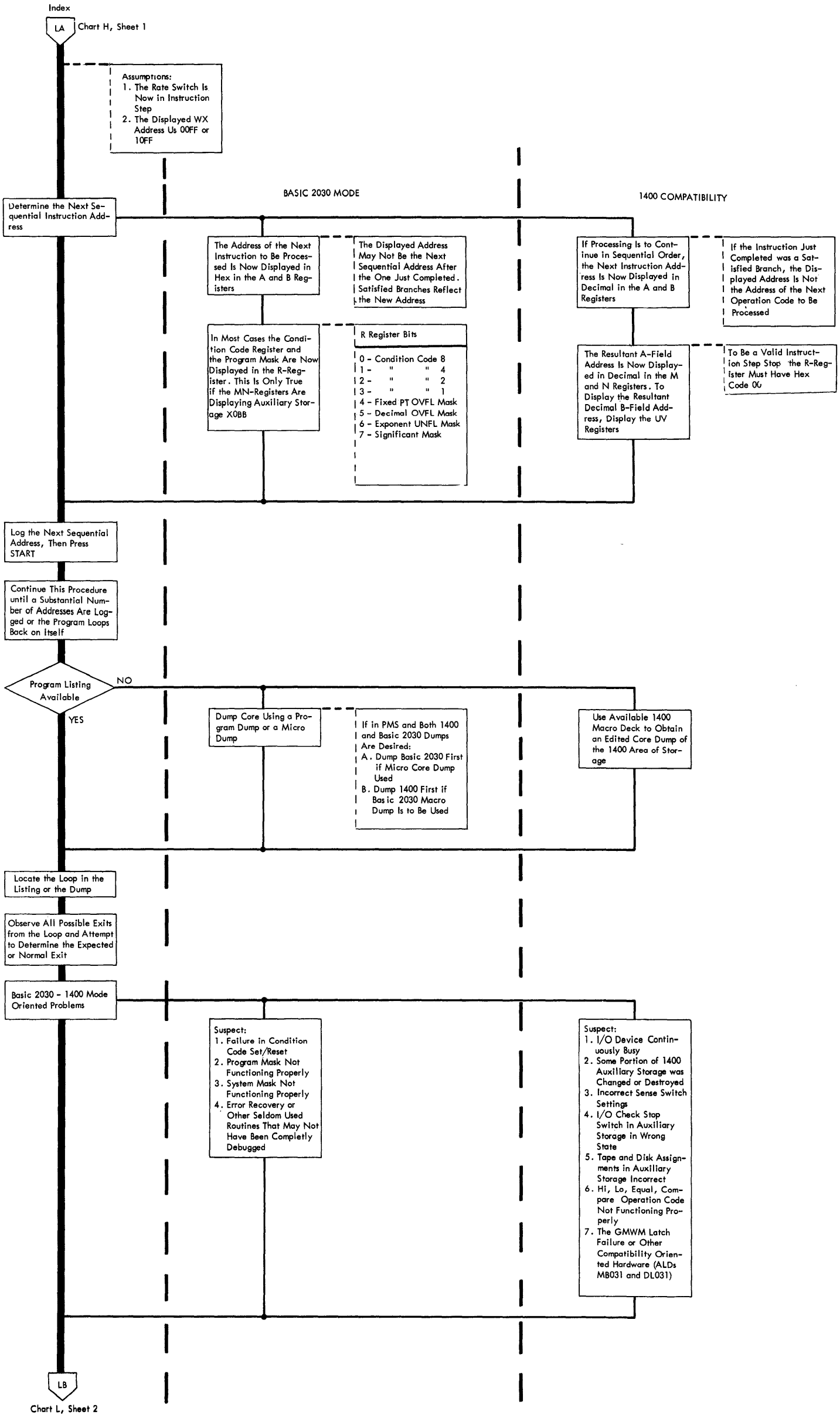


Chart J, Sheet 1
JB
06FF
Address Compare Switch to Early ROAR Stop. Set F G H J Switches to 06FF QC351
IPL Again
WX Address 6FD
YES
NO
F G H J Switches to 06FD
IPL Again
WX Address
A17
6ED
WX Address
6ED
A17
Selector Channel Has Received Some Final Status Bit Other than CE or DE. The R-Register Now Has Unit Status
Multiplexor Channel Has Received Some Final Status Bit Other than CE or DE; The A-Register Now Has Unit Status
Multiplexor Channel is Responding with 0 Status. A-Register Now Has Unit Status
Selector Channel Is Responding with 0 Status. R-Register Now Has Unit Status
Suspect: Unit Check Occurred During IPL Windup
Suspect: Unit Response Is Missing CE or DE
Chart J, Sheet 1
JD
0981
Address Compare Switch to Early ROAR Stop. Set F G H J Switches to 0981 QD011
IPL Again
WX Address
9C8
982
Select-In Received in Response to Select-Out (No Control Unit Response). Desired Control Unit and Device Now in Selector Data Register
Control Unit Initial Status Non Zero. It Is Now Displayed in Selector Data Register
Suspect: 1 Control Unit Off-Line 2 CPU Selected Wrong or Invalid Channel 3 Channel Trying to Select a Non-Existent Device
Suspect: Not-ready Answering Busy
Chart J, Sheet 1
JC
095E
Address Compare Switch to Early ROAR Stop. Set F G H J Switches to 095E QD181
IPL Again
WX Address
901
95D
Early ROAR on 095D to Determine Type of Program Check
Initial CPU Selector Channel, Channel Status Bad
Suspect: 1 Data Being Read in Does Not Have Proper IPL Information 2 Blanks Are Being Read in
Suspect: 1 Channel Hardware Failure 2 Select-Out Did Not Propagate - Result Channel Interface Control Check Due to Time Out 3 Interface Cable Unplugged 4 CPU Machine Check caused Channel Control Check
Place in Stop Mode - Try Again
Chart J, Sheet 1
JE
0A7A
Solid Failure
NO
YES
Address Compare Switch to Early ROAR Stop. Set F, G, H, J Switches to 0A7A QC451. Set Check Control Switch to Stop
IPL Again
CPU Check Red Light
YES
NO
CA
Chart C, Sheet 1
Channel Check - Press Start. Go to WX 0A7A
In IPL Mode Log Out Byte 0082 Is Not Indicative of Error Conditions as Specified
Read All Comments on QC451 Using 2030 CE Handbook Under CPU Channel Log, Determine Type of Failure. R-Register Now Has Catalog Number or Machine Check Indication
Run Priority Controls Micro Repop Diagnostic Test 3447 and Multiplexor Channel Repop Test 3346 (Vol 41)

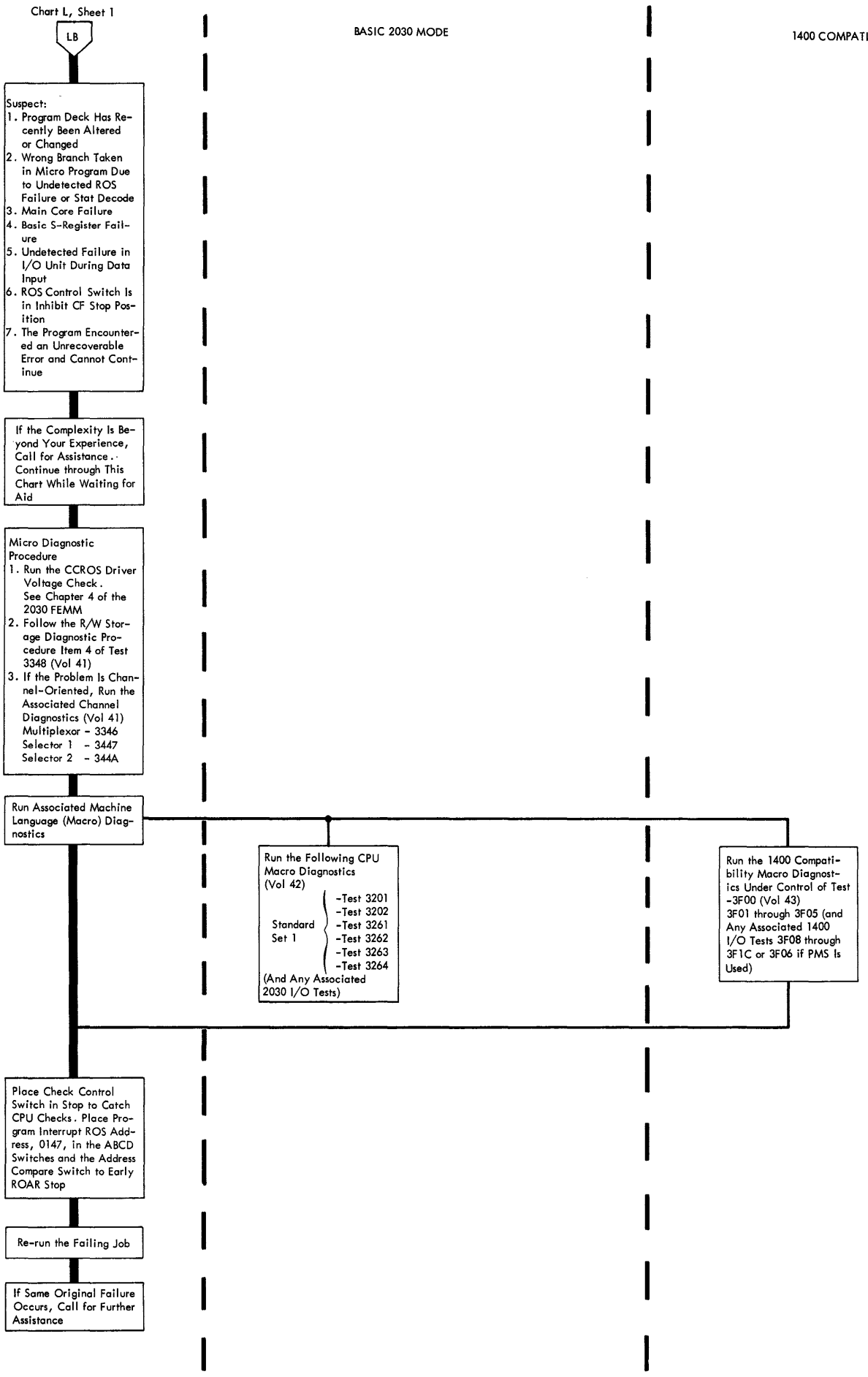


DT Chart L Machine Language (Macro Program) Loops (Sheet 1)

Chart L, Sheet 1

BASIC 2030 MODE

1400 COMPATIBILITY



Index
MA Chart W, Sheet 1
Chart W, Sheet 2

Reference Material
1. SRL--System/360 Principles of Operation.
2. System/360 I/O Interface Channel-to-Channel Manual
3. Field Engineering Maintenance Manual
4. FE Handbook

Save All Logged Data that Is Pertinent to the Existing Failure and Run Micro Diagnostics

Run Priority Controls Micro Repop. Test 3347 (Vol. 41) Followed by the Multiplexor Micro Repop. Test 3346 (Vol .41)

Continue Using Data Derived from Failing Job

Error Conditions--More Than One Bit in The Status Bytes May Be on. Use SRL for Reference

Check Channel Status (Byte 45) Byte 5 of CSW

This Is an Indication of A Channel Error. Bit Combinations Are Possible. Use System Reference Library Manual and Units Reference Manual with These Flow Charts for Trouble

CDC & CC Bit 44 & 47

Conditions Do Not Exist on MPX Channel

Program Check Bit 42

Error Due To CCW or CAW in Error

Run Macro Diagnostic 3430

1. Set Check Control Switch to Stop
2. Set Address Compare Switch to Roar Stop
3. Set Switches ABCD to 0A8E

Rerun Job--Match Light on Indicates Program Check Has Occurred

Unless Error Occurred During Command Chaining, Catalog No. will be in the High Data Field of the CSW

When Stop Occurs ALU Output will be Displaying Catalog # See CAS Page QC461

Go to Suspect Chart M Sheet 3

Channel Control Check Bit 45

Check Control Switch Was in Process Mode

Inspect Logout Area Bytes 81, 82, 83

Reference CLDs QC451 & CE Handbook Logout Area

Put System in Check Stop Mode. Run Channel Macro Test 3430

Refer to Red Light Chart (Chart C) when Stop Occurs.

1

PCI Bit 40

Inspect CCWs Previously Logged

Does One of The CCWs Have Bit 36 on

YES

This is not an Error. Refer to System/360 Principles of Operation for PCI Function

NO

This Condition Should Not Exist. To Do A CSW Store, A CCW Must Contain A PCI Bit

Rerun Job and Set Up to Stop When PCI Is Detected

1. Set Address Compare Switch to Roar Stop.
2. Set Switches A-B-C-D to 067E. CLD Page QC091

When Match Occurs A PCI Has Been Detected

Inspect UCW for CCW That Was Working when PCI Was Detected

Use CE Handbook to Inspect UCW. Subtract 8 from CCW Address to Find Working CCW Address. Inspect This String for A PCI Bit 36

2

2

Protect Check Bit 43

Analyze Log Data to Insure Not Programming Problem

Protect Keys Have Mismatched Somewhere

Run Storage Project Micro Diagram 3350

Run S.P. Macro Diagnostic 33C9

Do Storage Project Stack Adjustment Procedure

Use the Procedure as Outlined in the Field Engineering Maintenance Manual, Chapter 4

Set Up System to Stop on Error and Rerun Job

1. Set Address Compare Switch to Roar Stop.
2. Set Switches A-B-C-D to Address 0040. This Address Is Forced when Error Occurs
3. Rerun Job
4. Match Light on Indicates a Protection Error Occurred
5. Main Storage Now Contains Address of Protected Area
6. Set This Address into Switches A.B.C.D. Set Switch E to M.S. Press Display Key
7. Step Six Has Now Read into Q-Register Low, the Key from The Protect Stack
8. Display Q-Register
9. Normal Operation Would Have Q-High and Q-Low Match. the Occurrence of A Mismatch Is Flagged As A Program Error

MC Chart M Sheet 2

WLR Bit 41

Find Last Working CCW from Log Data. SLI Bit 34 Should not be On

Count In CCW Is the Amount Of Bytes To Be Transferred. Use This Count And Command And Run I/O Micro Test

Run Units Macro Diagnostic

Rerun Job to See if Error Reoccurs

MB Chart M Sheet 2

DT Chart M Multiplexor Channel (Sheet 1)

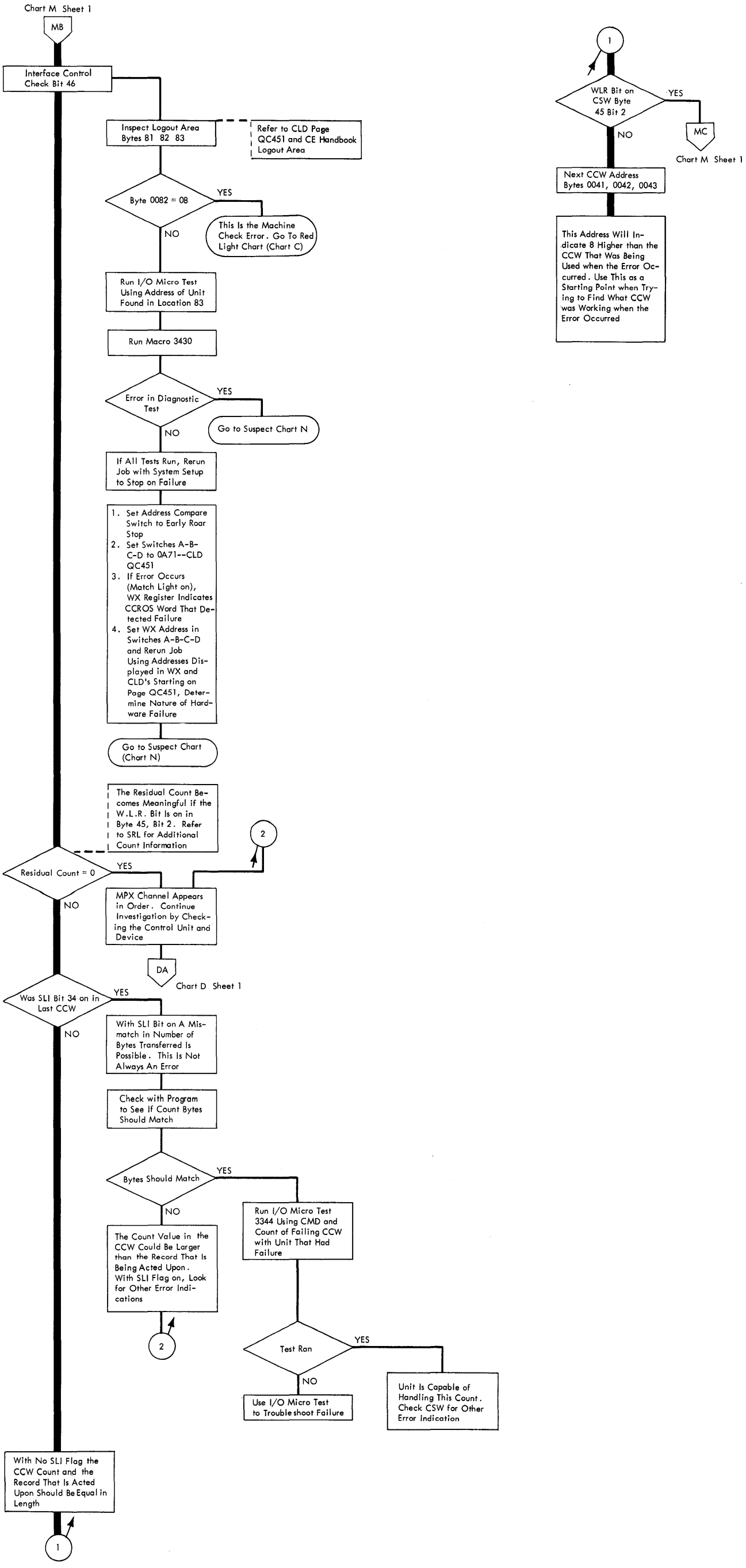
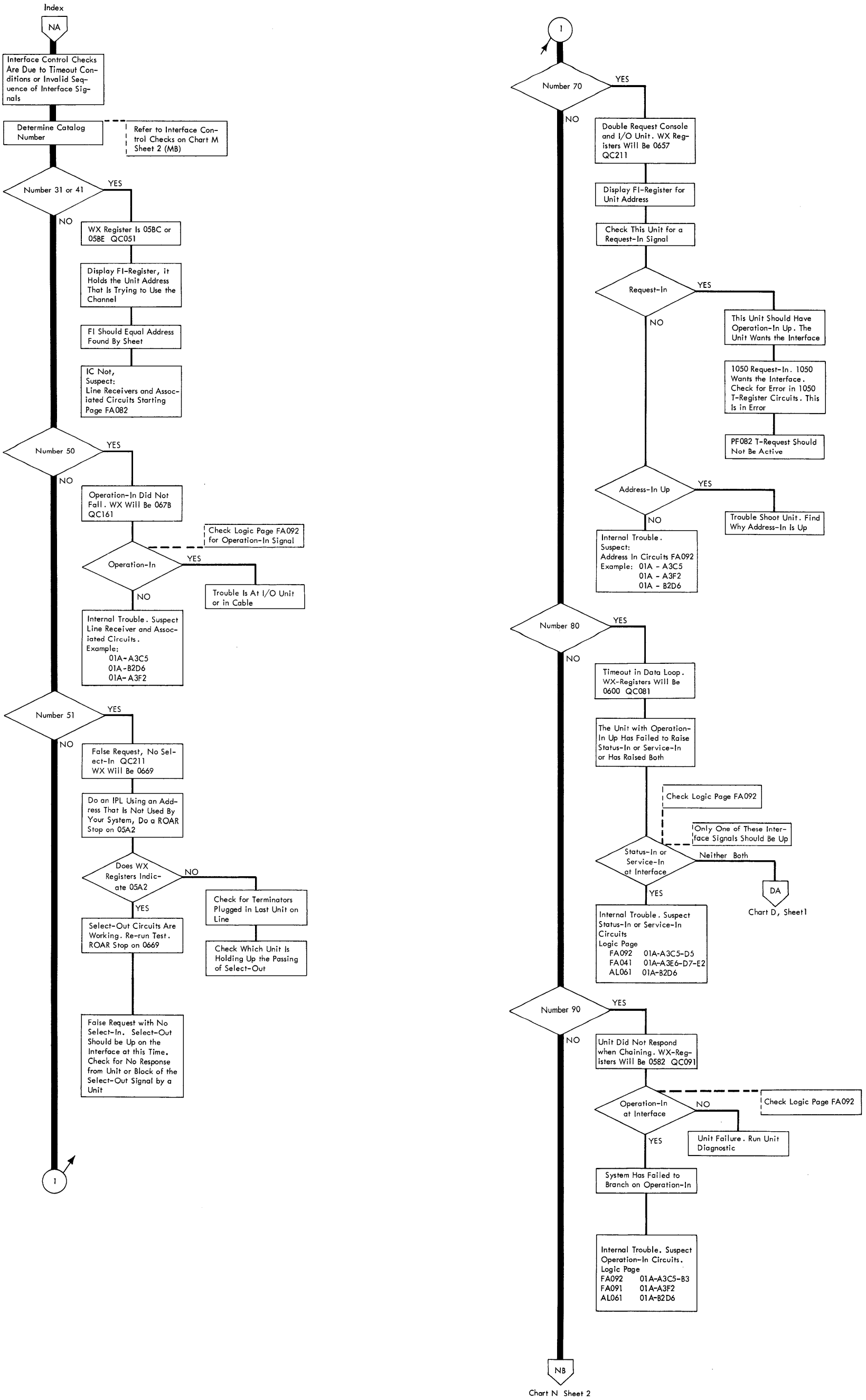


Chart M Sheet 1
MB
Interface Control Check Bit 46
Inspect Logout Area Bytes 81 82 83
Refer to CLD Page QC451 and CE Handbook Logout Area
Byte 0082 = 08
YES
NO
This Is the Machine Check Error. Go To Red Light Chart (Chart C)
Run I/O Micro Test Using Address of Unit Found in Location 83
Run Macro 3430
Error in Diagnostic Test
YES
NO
Go to Suspect Chart N
If All Tests Run, Rerun Job with System Setup to Stop on Failure
1. Set Address Compare Switch to Early Roar Stop
2. Set Switches A-B-C-D to 0A71--CLD QC451
3. If Error Occurs (Match Light on), WX Register Indicates CCROS Word That Detected Failure
4. Set WX Address in Switches A-B-C-D and Rerun Job Using Addresses Displayed in WX and CLD's Starting on Page QC451, Determine Nature of Hardware Failure
Go to Suspect Chart (Chart N)
The Residual Count Becomes Meaningful if the W.L.R. Bit Is on in Byte 45, Bit 2. Refer to SRL for Additional Count Information
2
Residual Count = 0
YES
NO
MPX Channel Appears in Order. Continue Investigation by Checking the Control Unit and Device
DA
Chart D Sheet 1
Was SLI Bit 34 on in Last CCW
YES
NO
With SLI Bit on A Mismatch in Number of Bytes Transferred Is Possible. This Is Not Always An Error
Check with Program to See If Count Bytes Should Match
Bytes Should Match
YES
NO
Run I/O Micro Test 3344 Using CMD and Count of Failing CCW with Unit That Had Failure
The Count Value in the CCW Could Be Larger than the Record That Is Being Acted Upon. With SLI Flag on, Look for Other Error Indications
2
Test Ran
YES
NO
Use I/O Micro Test to Troubleshoot Failure
Unit Is Capable of Handling This Count. Check CSW for Other Error Indication
With No SLI Flag the CCW Count and the Record That Is Acted Upon Should Be Equal in Length
1
1
WLR Bit on CSW Byte 45 Bit 2
YES
NO
MC
Chart M Sheet 1
Next CCW Address Bytes 0041, 0042, 0043
This Address Will Indicate 8 Higher than the CCW That Was Being Used when the Error Occurred. Use This as a Starting Point when Trying to Find What CCW was Working when the Error Occurred

L-Register	CLD Page	Early ROAR Stop at	Do WX Registers Read at	Hints
01	QC021	0A89	052C	1. Zero count in CCW Byte 6 and 7 Check CCW display DL-Registers now holding the count.
02	QC021	0A89	0590	1. Invalid flags in Byte 4 of CCW. Display L-Register. Low-order three bits must be zero.
04	QC021	0A89	0515	1. Initial operation has a TIC or 2. Two TICs in a row. 3. Inspect CCW string for this condition.
05	QC021	0A89	051D	1. Invalid command Byte, check Byte 0 of CCW.
06	QX021	051E	051B	1. Byte 1 of CCW is not zero. Check CCW for this Condition.
07	QC011	058A	0572	1. Protection error in CCW. 2. CCW address too big for memory size. 3. Byte 0049 must be zero for 2030. 4. Check CAW format using CE Handbook or SRL Manual.
08	QC021	0A8B	0517	1. Two successive TICs. I- and J-Registers now have address of CCW that had the second TIC as its command. Inspect CCW string for this condition.
09	QC011	0526	0522	1. The new CCW address designated by a TIC command was not located on a doubleword boundary.
0A	QC061	0A8F	0611/ 0613	1. Memory wrap when CCW was being updated during a chaining operation
0B	QC101	0A8B	069C	1. Zero count detected while data chaining or invalid flag Byte. 2. Check L- and D-Registers for count. 3. Check S-Register for 5 bit being on. If 5 bit is off, an invalid flag Byte was detected. 4. Check CCW for these conditions.
0C	QC101	058B	053C	1. Memory wrap on next CCW address while CDA. 2. I- and J-Registers now should indicate zero.
0D	QC021	0A8F	052D	1. Zero count detected during a command chain. Check L- and D-Registers for count. 2. Check CCW string for these conditions.
0E	QC031	0A8F	052A	1. Invalid flag Byte while command chining. 2. L-Register contains flag Byte. 3. Check CCW string for this condition
1F	QC131	0A8F	06BC	1. Memory wrap detected while command chaining. Next CCW was located outside of memory. I- and J-Registers are 0000. 2. Check CCW string for a CCW located in the last 8 locations in memory. This one is chaining out of memory.
2F	QC131	0A8F		1. Command Byte all zeros detected while command chaining. U-Register now holds the command. 2. I- and J-Registers now contain the failing CCW address plus 1. 3. Check CCW string for this address and the indicated error condition.



DT Chart N Multiplexor Catalog Numbers (Sheet 1)

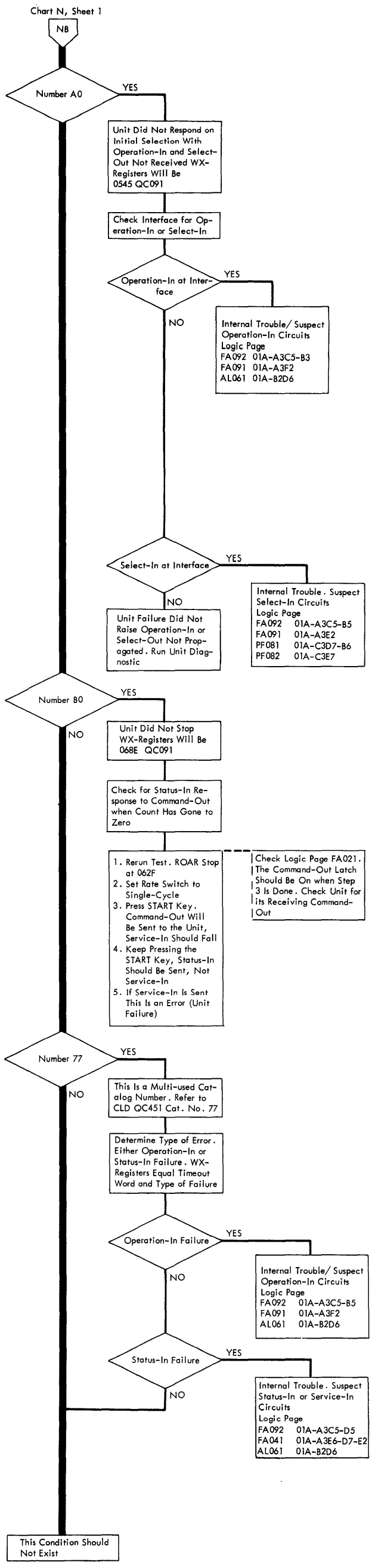
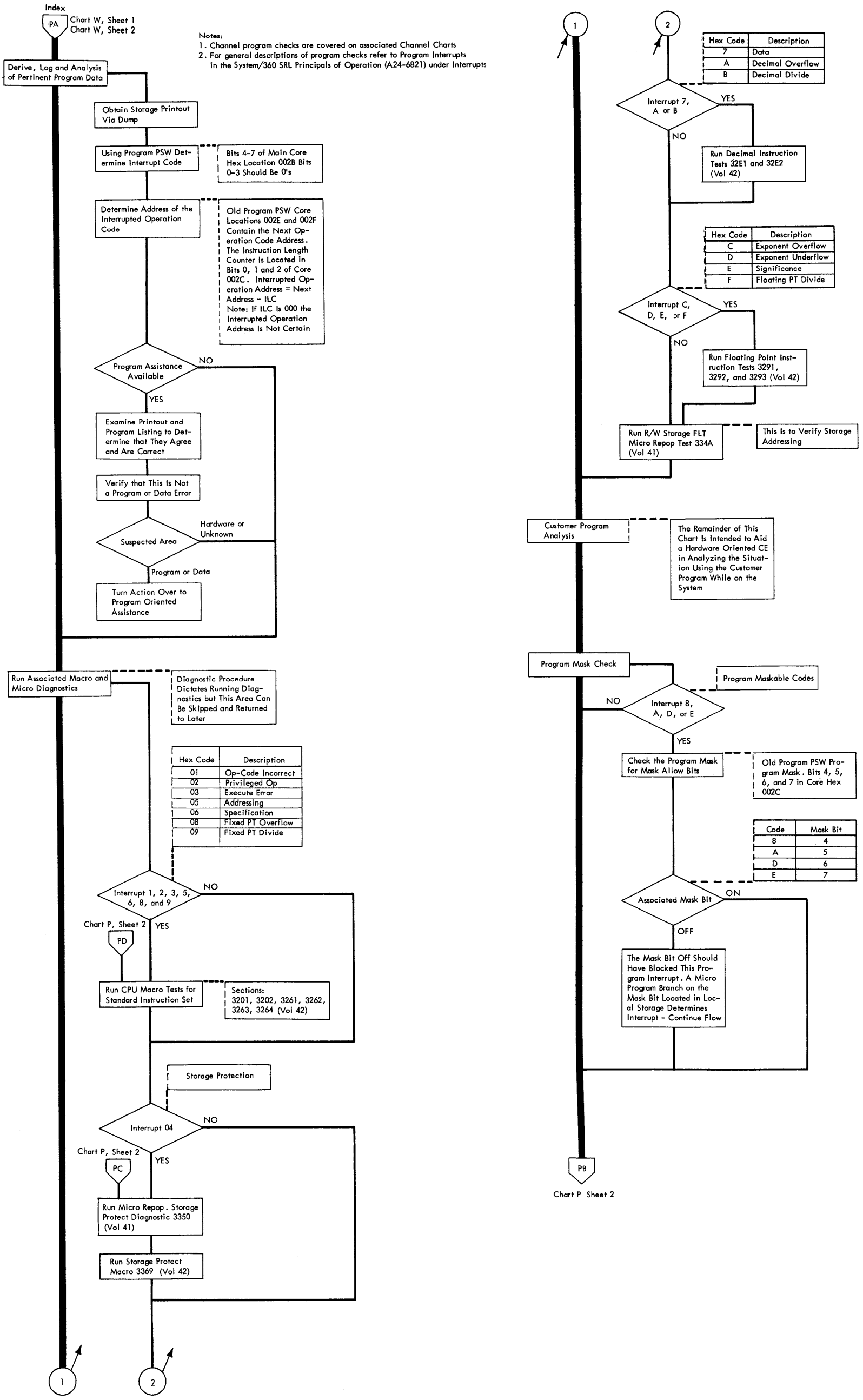


Chart N, Sheet 1
NB
Number A0
YES
Unit Did Not Respond on Initial Selection With Operation-In and Select-Out Not Received WX-Registers Will Be 0545 QC091
Check Interface for Operation-In or Select-In
Operation-In at Interface
YES
Internal Trouble/ Suspect Operation-In Circuits Logic Page
FA092 01A-A3C5-B3
FA091 01A-A3F2
AL061 01A-B2D6
NO
Select-In at Interface
YES
Internal Trouble. Suspect Select-In Circuits Logic Page
FA092 01A-A3C5-B5
FA091 01A-A3E2
PF081 01A-C3D7-B6
PF082 01A-C3E7
NO
Unit Failure Did Not Raise Operation-In or Select-Out Not Propagated. Run Unit Diagnostic
Number B0
YES
Unit Did Not Stop WX-Registers Will Be 068E QC091
NO
Check for Status-In Response to Command-Out when Count Has Gone to Zero
1. Rerun Test. ROAR Stop at 062F
2. Set Rate Switch to Single-Cycle
3. Press START Key. Command-Out Will Be Sent to the Unit, Service-In Should Fall
4. Keep Pressing the START Key, Status-In Should Be Sent, Not Service-In
5. If Service-In Is Sent This Is an Error (Unit Failure)
Check Logic Page FA021. The Command-Out Latch Should Be On when Step 3 Is Done. Check Unit for its Receiving Command-Out
Number 77
YES
This Is a Multi-used Catalog Number. Refer to CLD QC451 Cat. No. 77
NO
Determine Type of Error. Either Operation-In or Status-In Failure. WX-Registers Equal Timeout Word and Type of Failure
Operation-In Failure
YES
Internal Trouble/ Suspect Operation-In Circuits Logic Page
FA092 01A-A3C5-B5
FA091 01A-A3F2
AL061 01A-B2D6
NO
Status-In Failure
YES
Internal Trouble. Suspect Status-In or Service-In Circuits Logic Page
FA092 01A-A3C5-D5
FA041 01A-A3E6-D7-E2
AL061 01A-B2D6
NO
This Condition Should Not Exist



DT Chart P Program Checks (Sheet 1)

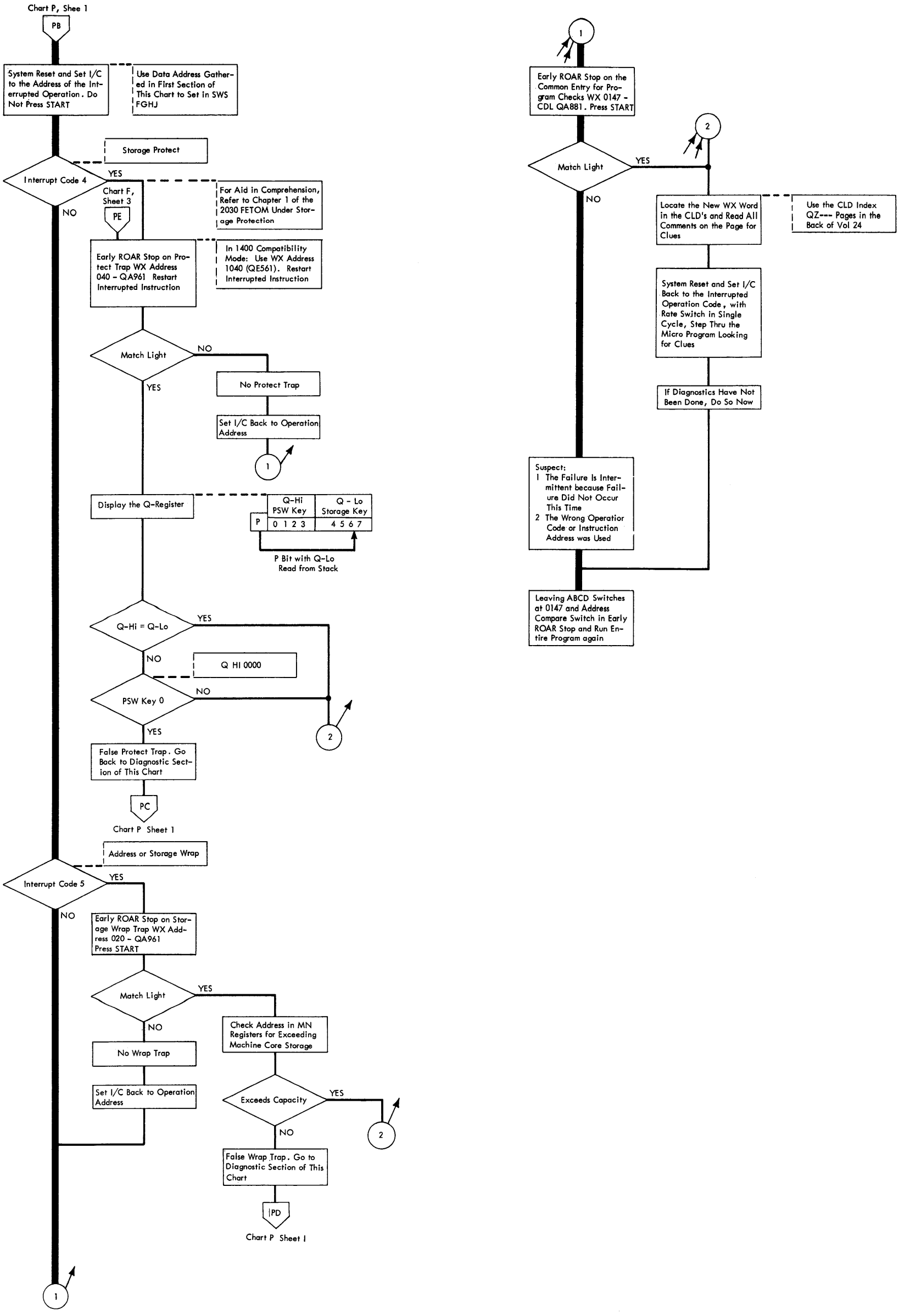
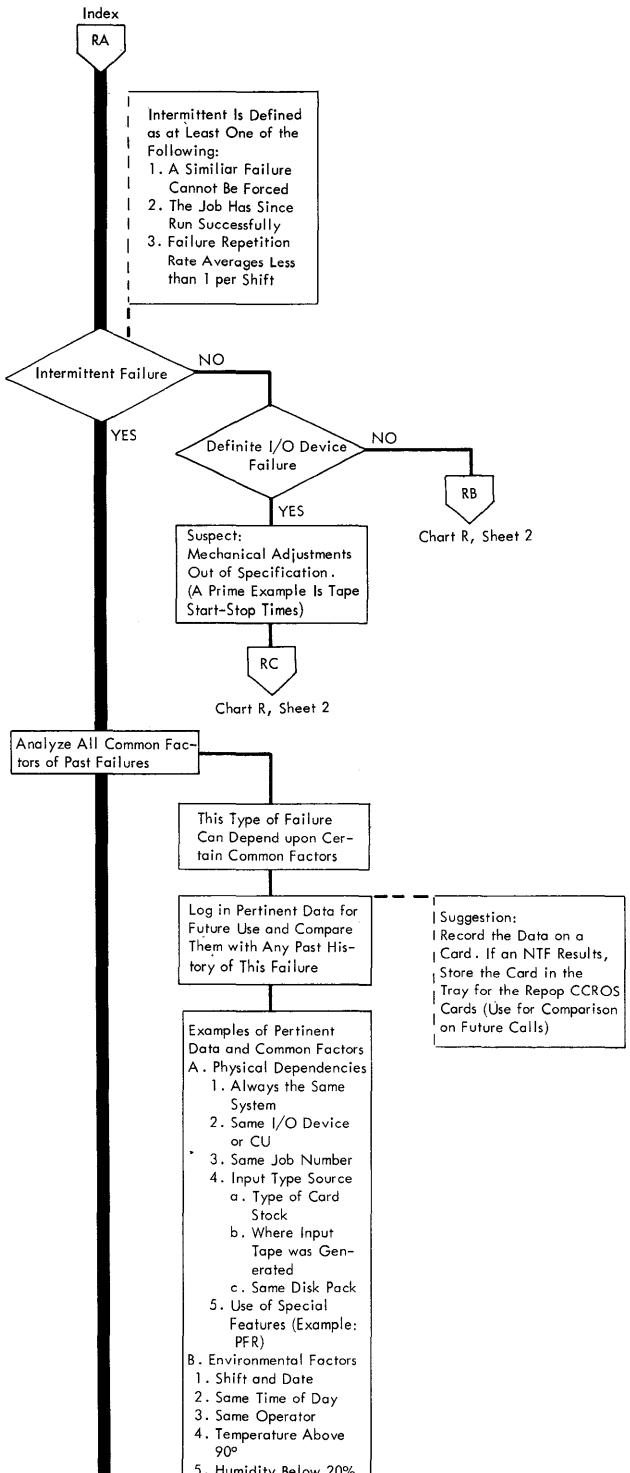
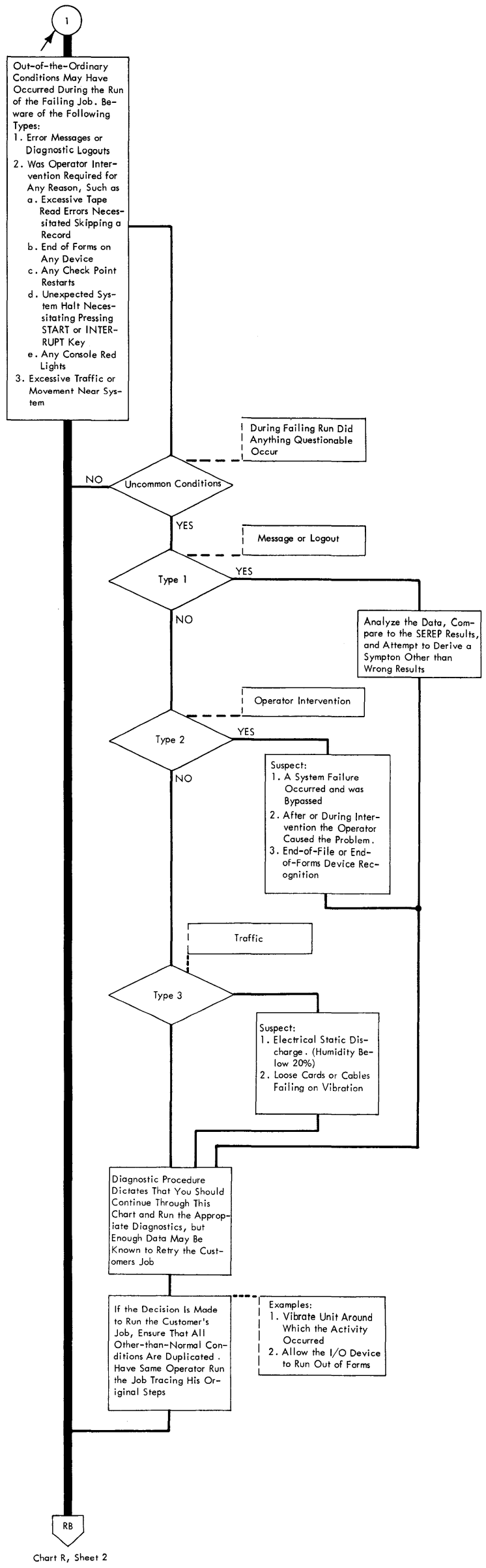


Chart P, Shee 1
PB
System Reset and Set I/C to the Address of the Interrupted Operation. Do Not Press START
Use Data Address Gathered in First Section of This Chart to Set in SWS FGHJ
Storage Protect
Interrupt Code 4
YES
NO
Chart F, Sheet 3
PE
For Aid in Comprehension, Refer to Chapter 1 of the 2030 FETOM Under Storage Protection
Early ROAR Stop on Protect Trap WX Address 040 - QA961 Restart Interrupted Instruction
In 1400 Compatibility Mode: Use WX Address 1040 (QE561). Restart Interrupted Instruction
Match Light
NO
YES
No Protect Trap
Set I/C Back to Operation Address
1
Display the Q-Register
Q-Hi PSW Key
Q - Lo Storage Key
P
0 1 2 3
4 5 6 7
P Bit with Q-Lo Read from Stack
Q-Hi = Q-Lo
YES
NO
Q HI 0000
PSW Key 0
NO
YES
2
False Protect Trap. Go Back to Diagnostic Section of This Chart
PC
Chart P Sheet 1
Address or Storage Wrap
Interrupt Code 5
YES
NO
Early ROAR Stop on Storage Wrap Trap WX Address 020 - QA961 Press START
Match Light
YES
NO
No Wrap Trap
Set I/C Back to Operation Address
Check Address in MN Registers for Exceeding Machine Core Storage
Exceeds Capacity
YES
NO
2
False Wrap Trap. Go to Diagnostic Section of This Chart
PD
Chart P Sheet 1
1
Early ROAR Stop on the Common Entry for Program Checks WX 0147 - CDL QA881. Press START
2
Match Light
YES
NO
Locate the New WX Word in the CLD's and Read All Comments on the Page for Clues
Use the CLD Index QZ--- Pages in the Back of Vol 24
System Reset and Set I/C Back to the Interrupted Operation Code, with Rate Switch in Single Cycle, Step Thru the Micro Program Looking for Clues
If Diagnostics Have Not Been Done, Do So Now
Suspect:
1 The Failure Is Intermittent because Failure Did Not Occur This Time
2 The Wrong Operatior Code or Instruction Address was Used
Leaving ABCD Switches at 0147 and Address Compare Switch in Early ROAR Stop and Run Entire Program again





DT Chart R Missing Records or Wrong Results (Sheet 1)

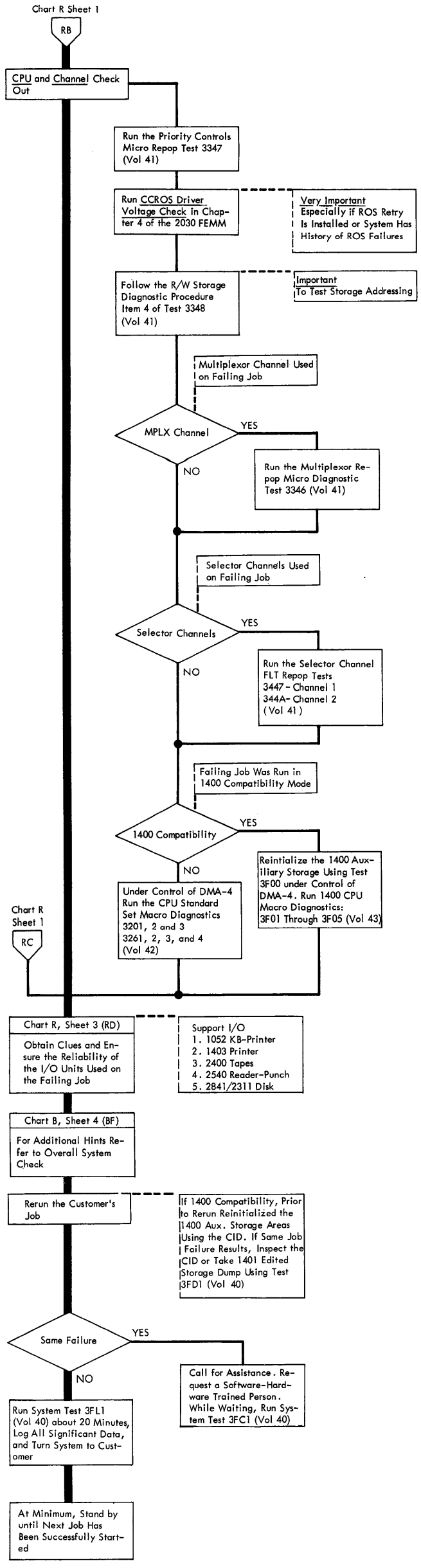


Chart R Sheet 1
RB
CPU and Channel Check Out
Run the Priority Controls Micro Repop Test 3347 (Vol 41)
Run CCROS Driver Voltage Check in Chapter 4 of the 2030 FEMM
Very Important Especially if ROS Retry Is Installed or System Has History of ROS Failures
Follow the R/W Storage Diagnostic Procedure Item 4 of Test 3348 (Vol 41)
Important To Test Storage Addressing
Multiplexor Channel Used on Failing Job
MPLX Channel
YES
NO
Run the Multiplexor Repop Micro Diagnostic Test 3346 (Vol 41)
Selector Channels Used on Failing Job
Selector Channels
YES
NO
Run the Selector Channel FLT Repop Tests 3447 - Channel 1 344A- Channel 2 (Vol 41)
Failing Job Was Run in 1400 Compatibility Mode
1400 Compatibility
YES
NO
Reintialize the 1400 Auxiliary Storage Using Test 3F00 under Control of DMA-4. Run 1400 CPU Macro Diagnostics: 3F01 Through 3F05 (Vol 43)
Under Control of DMA-4 Run the CPU Standard Set Macro Diagnostics 3201, 2 and 3 3261, 2, 3, and 4 (Vol 42)
Chart R Sheet 1
RC
Chart R, Sheet 3 (RD)
Obtain Clues and Ensure the Reliability of the I/O Units Used on the Failing Job
Support I/O
1. 1052 KB-Printer
2. 1403 Printer
3. 2400 Tapes
4. 2540 Reader-Punch
5. 2841/2311 Disk
Chart B, Sheet 4 (BF)
For Additional Hints Refer to Overall System Check
Rerun the Customer's Job
If 1400 Compatibility, Prior to Rerun Reinitialized the 1400 Aux. Storage Areas Using the CID. If Same Job Failure Results, Inspect the CID or Take 1401 Edited Storage Dump Using Test 3FD1 (Vol 40)
Same Failure
YES
NO
Call for Assistance. Request a Software-Hardware Trained Person. While Waiting, Run System Test 3FC1 (Vol 40)
Run System Test 3FL1 (Vol 40) about 20 Minutes, Log All Significant Data, and Turn System to Customer
At Minimum, Stand by until Next Job Has Been Successfully Started

RD

Unit Description	Symptom or Cause	Notes and Hints	Suggested Minimum Quick Check
1052 Key Board	1. Missing characters caused by console attachment failing to read punch-1-clutch signal	Check interface cables in the 1051, the half board 01F-A1, and in the CPU on boards 01A-C2 and C3 (ALD PF 521)	Run the read inquiry macro diagnostic 902 Vol 43
	2. Extra character in storage	Console request-in line may not be resetting properly (ALD PF021)	
	3. Wrong data in storage; good data on 1052 printer	Check PT & T to EBDIC Translate starting at PF 291 through PF 331	
	4. Wrong data on printer; good data in storage	Definite 1051 or 1052 printer failure	
1052 Printer	1. Missing characters--caused by 1051 home loop timer running slower than the console attachment clock--or console attachment clock faster than 1051 timer	1. Check attachment clock timing; refer to note on ALD PF011 2. Check 1051 home loop single shots in 1051 manual page 131TM	Run the basic write function macro diagnostic 900 Vol 43
	2. Only one character of a message prints. This may also be the wrong first character	Posssible that 1050-Request-in line not being reset (ALD PF071)	
	3. 1050 intervention required would cause no message to be accepted by 1052 printer (indicator on lower right of console under CPU status)	1. Is printer paper under interlock 2. Is CPU switch off 3. Check EPO switch inside back cover of 1051	
	4. Incorrect data	1. Turn the 1052 CPU switch off. Type A through Z. If incorrect character prints, 1051 or 1052 is at fault. 2. On-line check the EBCDIC to PT & T Translate on ALD PF 191 through 222	
1403 Printer	1. Wrong chain on 1403 or wrong UCB image	Check job for proper chain and UCB deck	Run printer macro diagnostics 1. F 832 (UCS printers) (2821 Vol 8) 2. F 836 ripple print (2821 Vol 8)
	2. Hammer check circuit malfunction not catching extra or missing hammer fire, or failure to receive data check on unprintable UCS character	Diagnostic F832 will check this	
	3. Interface or 2821 failure causing data record to be cut short		
	4. Multiple pick or drop of bits in UCB	Reinitialize UCB	
	5. Multiple pick or drop of bits in print buffer		
	6. UCB parity-check circuit failure		
	7. Print buffer parity-check circuit failure		
	8. Sync-check error circuit failure	To ensure back in sync, open and close T-casting or initialize the UCB.	
	9. End-of-forms indication malfunction	Test off-line	
	10. Failure to recognize data checks could be caused by the BLOCK DATA CHECK LATCH or the FOLDING LATCH in 2821 (in UCB only)	Diagnostic F832 will check this	
	11. Missing slug on chain or broken hammer	One character or one print position	
	12. 1401 compatibility missing last 32 positions of print line	Missing bit 0 in COMP AUX storage-B of byte 8C. This bit is reset on 8K machines if operator presses the load key with 1402 in the F, G, H, and J switches; then does system reset, ROAR reset, and start	
2400 Tapes	1. Drive start-stop time maladjustment	Most probable cause	Run the following macro diagnostics to check tape start-stop times: 16K systems --F521 and F522 8K Systems--3523 and 3524 only All systems--for Diagnostic Check F510 All tests are in MDP Tape/TCU (Vol 3)
	2. Check to see if the forward stop delay noise trigger ever comes on. Records can be skipped if it does	This is usually a result of maladjusted drive start-stop times	
	3. Tape being used was generated bad at a previous date, possibly on another system	Check tape source, and the age and condition of the tape	
	4. Detected hard errors not being handled	Run job with error hold plugged on TAU	
	5. Failures in special recognition circuits and command codes such as single tape mark records, noise bits, EOF, erase, backspace and forward space commands		
	6. 1400-compatibility mode: check the operation of the GMWM latch on CPU ALD MB 022		
	7. Failures with data convert, translate, and densities, either hardware or program failure		

Unit Description	Symptom or Cause	Notes and Hints	Suggested Minimum Quick Check
2540 Reader	1. Two cards feeding piggy-back through reader	Check reader throat adjustment; if near .020", this is a possibility	Run macro diagnostics 1. F821 routine 1-- (punch 27 cards) 2821 Vol 8 2. F811 routine 1-- (read same 27 cards) 2821 Vol 8
	2. Interface or 2821 failure causing data record to be cut short		
	3. Any error check circuit not functioning would fail to catch input errors	Running cards with one set of brushes removed will check one possibility	
	4. Multiple pick or drop in reader buffer		
	5. Cards way off registration	Very remote	
2540 Punch	1. Failure to give dummy write to punch at end of job allows one card to be left in punch. This card is not checked when nonprocess runout key is pressed	Check program for proper punch end procedure	Same as 2540 Reader
	2. Using EOF key on other than PFR can cause a missing record when cards are allowed to run out, new ones placed in hopper, and job continued	Use EOF on PFR operations only	
	3. Punch check circuit failure in conjunction with valid punch check	1. Lift punch brushes, check for errors when punched cards are fed 2. Check the PCH BRUSH CL DELAY INT signal	
	4. See No. 2 on reader		
	5. Punch buffer pick or drop of even bits		
2841/2311 Files	1. Intermittently missing data or receiving no-record-found	Head alignment problems can cause this. But if adjustment is made beware of causing new problems while trying to read packs written before adjustment	1. Run the 2841 nonresident micro test--read/write 100 address marks. 2. Run the 2841 macro test 602 (MDP Vol A02) 3. Run the 2841 interchangability macro test 613 (MDP Vol A01)
	2. Missing records resulting in no-record-found	1. Have customer temporarily add a patch to his program to do a read-back check after every file-write command 2. Suggested programming procedure after no-record-found a. Read home address to ensure correct cylinder b. If not correct cylinder, a recalibrate command should be issued c. If correct cylinder, retry the original record at least 10 times Note: STEP C may have to be patched in some operating systems 3. Address marker detection circuit failure	
	3. Missing or short-length records with no indications	1. Run 2841 in check-stop mode to ensure that all detected errors are caught and handled 2. Address marker detection circuit failure and the program is not checking record identification 3. 2841 metering-in line is not forcing CPU metering-out when the CPU is stopped and the file command is still being executed. Check -0 channel to meter line on ALD KU011	
	4. 1400-compatibility count fields and data fields located on the wrong cylinder.	The compare-disable bit 1400 AUX storage B UCW (XX10) bit 0 was possibly on when data records were written. This bit should be on only during the original 1400 formatting of the disk	

SELECTOR CHANNEL	
* SELECTOR LOG DATA	** SELECTOR CHANNEL FLT
1. GUV - Data Address 2. GCD - Count 3. GS - Status, Control, Error Conditions 4. GT - Inbound Tags, Control Information 5. Next CCW Address from Local Storage. Channel 1 - 8E - 8F Channel 2 - AE - AF	Channel 1 - 3447 Vol. 41 Channel 2 - 344A Vol. 41

Index SA → Chart I, Sheet 1; Chart W, Sheet 1; Chart W, Sheet 2

ASSUMPTIONS

Assumptions:
1. Lamp Test OK
2. Console Logged
3. Channel 1 Failure (If Channel 2, Replace G with H)

Channel Control Interface Control Program Check

Channel Data IL Protect Check

Set During Share or Micro Cycles

Set During Share Cycles Only

008 Interface Trap

Channel Control Interface Control Channel Data

Type

IL (Instruction Length) Program Check Protect Check

YES

Was CPU Check Switch in Stop

Stop Mode

NO

Interface Control Check

YES

NO

Run Selector FLT

Run Priority Controls Micro Diagnostic Repop Test 3347 (Vol 41)

CPU Check Switch to Stop, Try Original Program Again

Almost Always a Channel Failure

Channel Control Check

YES

NO

Is This Your Initial Attempt at This Failure

First Error Call

YES

NO

Run- Selector FLT **

Try Original Program Again

Selector Log *

Run- Selector FLT **

Run Storage Protect Micro Repop. Diagnostic Test 3350 (Vol 41)

Subtract 8 from Logged CCW Address to Get Address of Failing CCW

Generate a Macro Loop Using the Same CCWs as Failing Program

Suspect:
1. Selector Channel Clock Failure
2. Selector Priority
3. Hardware Failure of Channel Control Check Latch

1

1

Interface Control Check

YES

Generally a Cable, Interface, or Control Unit Failure

NO

Selector Log *

Check ROS Address

92A Turns on Interface Control Check Latch

WX Address 92A

YES

NO

Locate CLD Word

GR → GI Statement

NO

YES

Run- Selector FLT **

Suspect:
1. Error Check Circuits
2. Bad GR GI Decode
3. Bad GB Decode

GR Parity Error

NO

YES

Check Bus-In with Scope

Bus-In Good

NO

YES

Control Unit Problem or Cable

DA

Chart D, Sheet 1

Suspect:
1. GR-Registers
2. GR Assembler
3. Data Path to GR Assembler
4. Parity Check
5. SALs Timing
6. Skew on Bus-In

Compare R-Register to Selector Channel Catalog

Hex No	Meaning or Condition
10	Poll Control Timeout SIO, TIO, HIO
20	Queue Status Timeout SIO, TIO, HIO
30	No Address-In, Status-In, or Select-In. (CC or Initial Select SIO, TIO, HIO)
40	Address Mismatch (SIO, TIO, HIO, or Command Chain)
50	No Status-In or Initial Select (SIO, TIO, HIO, or Command Chaining)
60	Bad Address or Status Byte on Initial Select (SIO, TIO, HIO, or Command Chaining
70	Status-In Timeout on Initial Select (TIO)
80	Status-In Timeout on Command Chaining
90	Select-In on Command Chaining Reselection
A0	Control Unit Busy on Command Chaining
B0	Address Mismatch on TIO or Halt IO
C0	Status-In or Operation-In Cannot Be Reset on CSW Store
E0	Poll Control Cannot Be Set on HIO
F0	Operation-In Cannot Be Reset on HIO

Generally Main Storage Failure on Output Operation and Control Unit or Device on Input

Channel Data Check

YES

NO

GR-Register in Parity

YES

NO

Suspect:
1. Error Check Circuits

Run- Selector FLT **

Suspect:
1. Hardware Failure of Channel Data Check Latch

Inspect Displayed Selector Channel Command Register

Bit 7 On

YES

NO

Output Operation

Suspect:
1. Main Storage
2. Selector Channel Data Path

Run Selector FLT

Run Selector FLT *

Suspect:
Hardware Failure of GR-Registers

Input Operation

Suspect:
1. I/O Device Bus Lines
2. Interface and Cables
3. Selector Channel Line Receiver
4. Path from Receivers to GR-Registers

DA

Chart D, Sheet 1

SB

Chart S, Sheet 2

DT Chart S Selector Channel (Sheet 1)

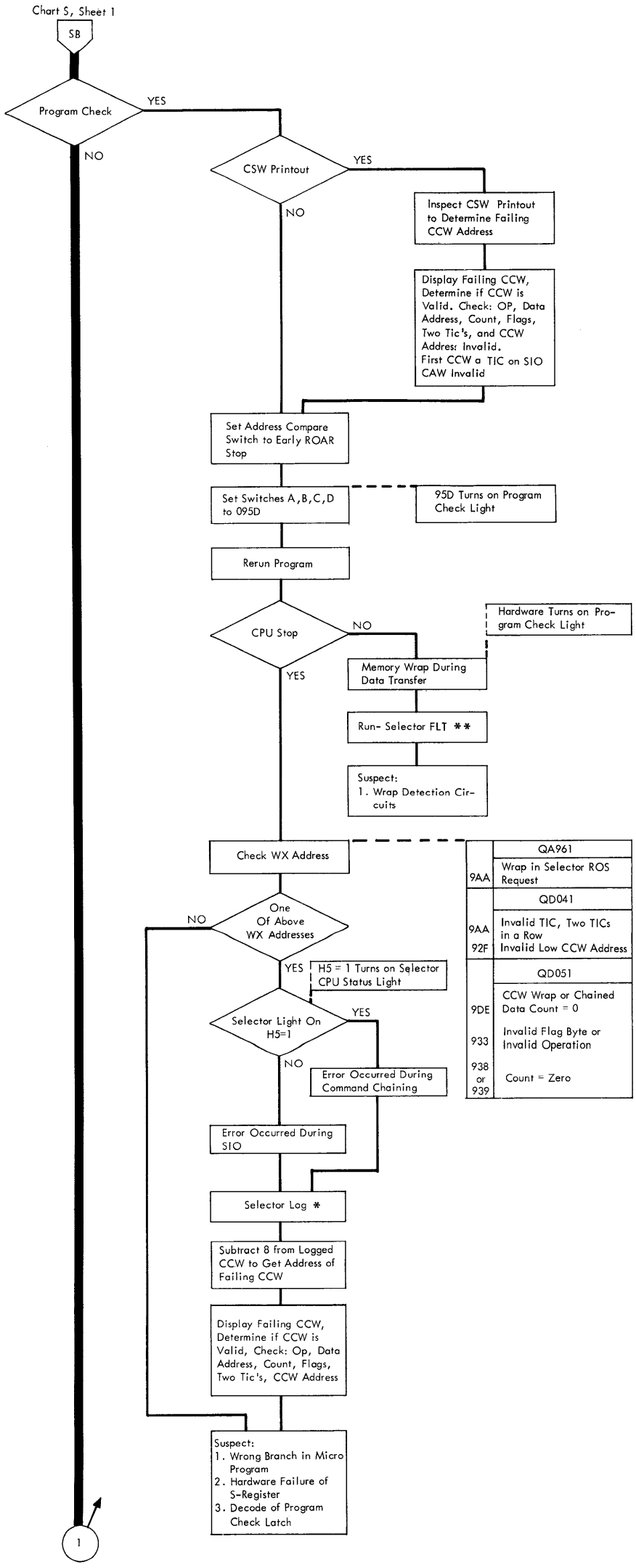


Chart S, Sheet 1
SB
Program Check
YES
NO
CSW Printout
YES
NO
Inspect CSW Printout to Determine Failing CCW Address
Display Failing CCW, Determine if CCW is Valid. Check: OP, Data Address, Count, Flags, Two Tic's, and CCW Address: Invalid. First CCW a TIC on SIO CAW Invalid
Set Address Compare Switch to Early ROAR Stop
Set Switches A,B,C,D to 095D
95D Turns on Program Check Light
Rerun Program
CPU Stop
NO
YES
Hardware Turns on Program Check Light
Memory Wrap During Data Transfer
Run- Selector FLT **
Suspect:
1. Wrap Detection Circuits
Check WX Address
One Of Above WX Addresses
NO
YES
H5 = 1 Turns on Selector CPU Status Light
Selector Light On H5=1
YES
NO
Error Occurred During Command Chaining
Error Occurred During SIO
Selector Log *
Subtract 8 from Logged CCW to Get Address of Failing CCW
Display Failing CCW, Determine if CCW is Valid, Check: Op, Data Address, Count, Flags, Two Tic's, CCW Address
Suspect:
1. Wrong Branch in Micro Program
2. Hardware Failure of S-Register
3. Decode of Program Check Latch
QA961
9AA Wrap in Selector ROS Request
QD041
9AA 92F Invalid TIC, Two TICs in a Row Invalid Low CCW Address
QD051
9DE CCW Wrap or Chained Data Count = 0
933 Invalid Flag Byte or Invalid Operation
938 or 939 Count = Zero
1
1
Instruction Length Check
YES
NO
Selector Log *
CSW Printout
NO
YES
Subtract 8 From Logged CCW to get Address of Failing CCW
Inspect Printouts; Check as Follows
Display Failing CCW, Check As Follows
Data Chaining
NO
YES
Residual Count in GCD and/or CSW
YES
NO
Device Not Sending or Accepting Enough Bytes to Channel
Inspect Displayed Selector Channel Command Register
Bit 7 On
YES
NO
Input Operation
Output Operation
Condition Should Not Exist
Device Not Accepting Last Byte from Channel
YES
SLI Bit On
NO
ILC Should Not Be Set
CCW Count Match Record Size
NO
YES
IL Check Should Be Set. Must Adjust Count in CCW
If Output Operation and GS0 =1 (GR Full), Then Residual Count is GCD+1
YES
Residual Count in GCD and/or CSW = Zero
NO
Device Trying to Send or Accept Too Many Bytes to Channel
Device Not Sending or Accepting Enough Bytes to Channel
Run- Selector FLT **
Suspect:
1. Circuit on GB
2. ILC Latch
SC
Chart S, Sheet 3

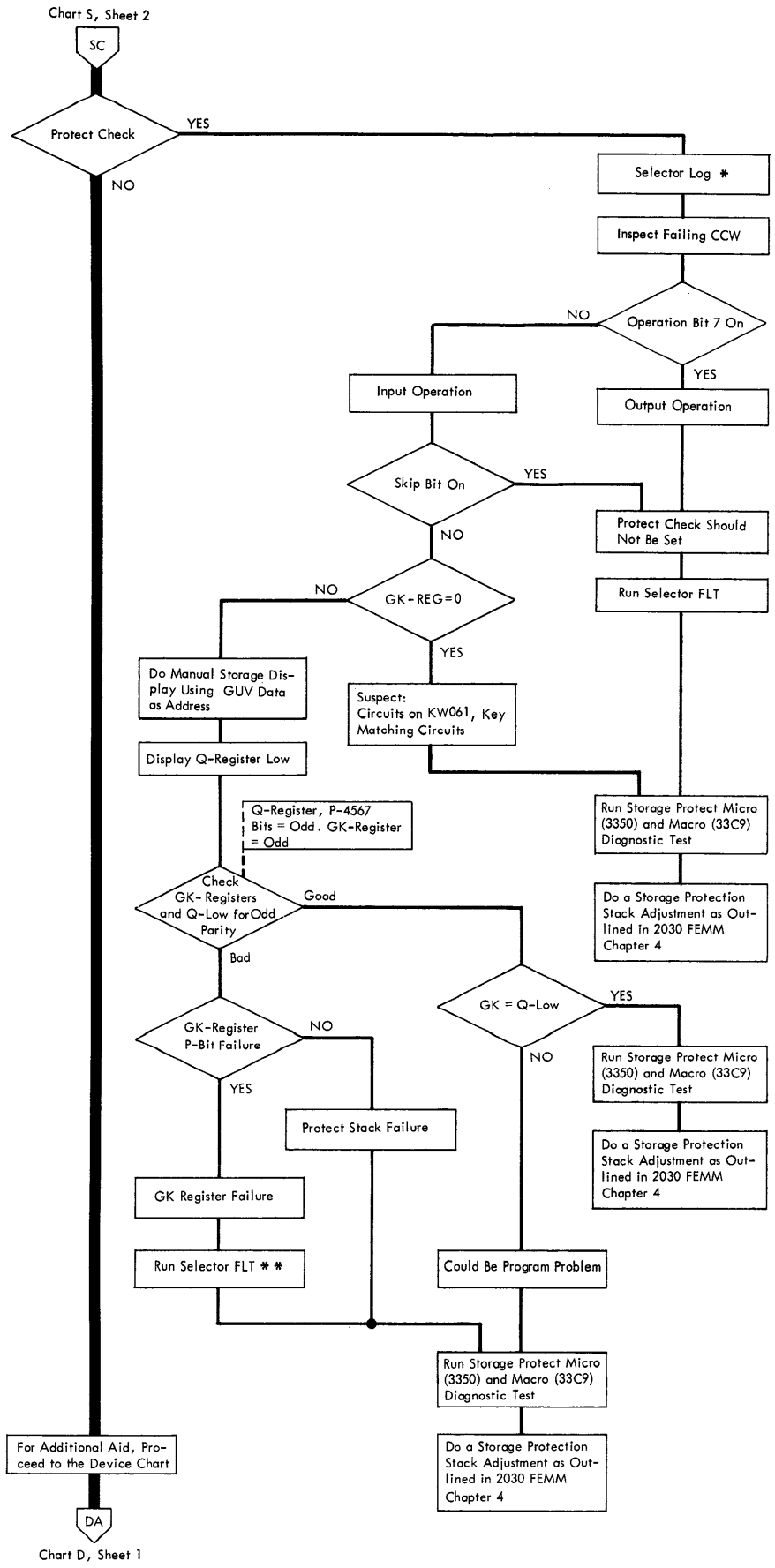
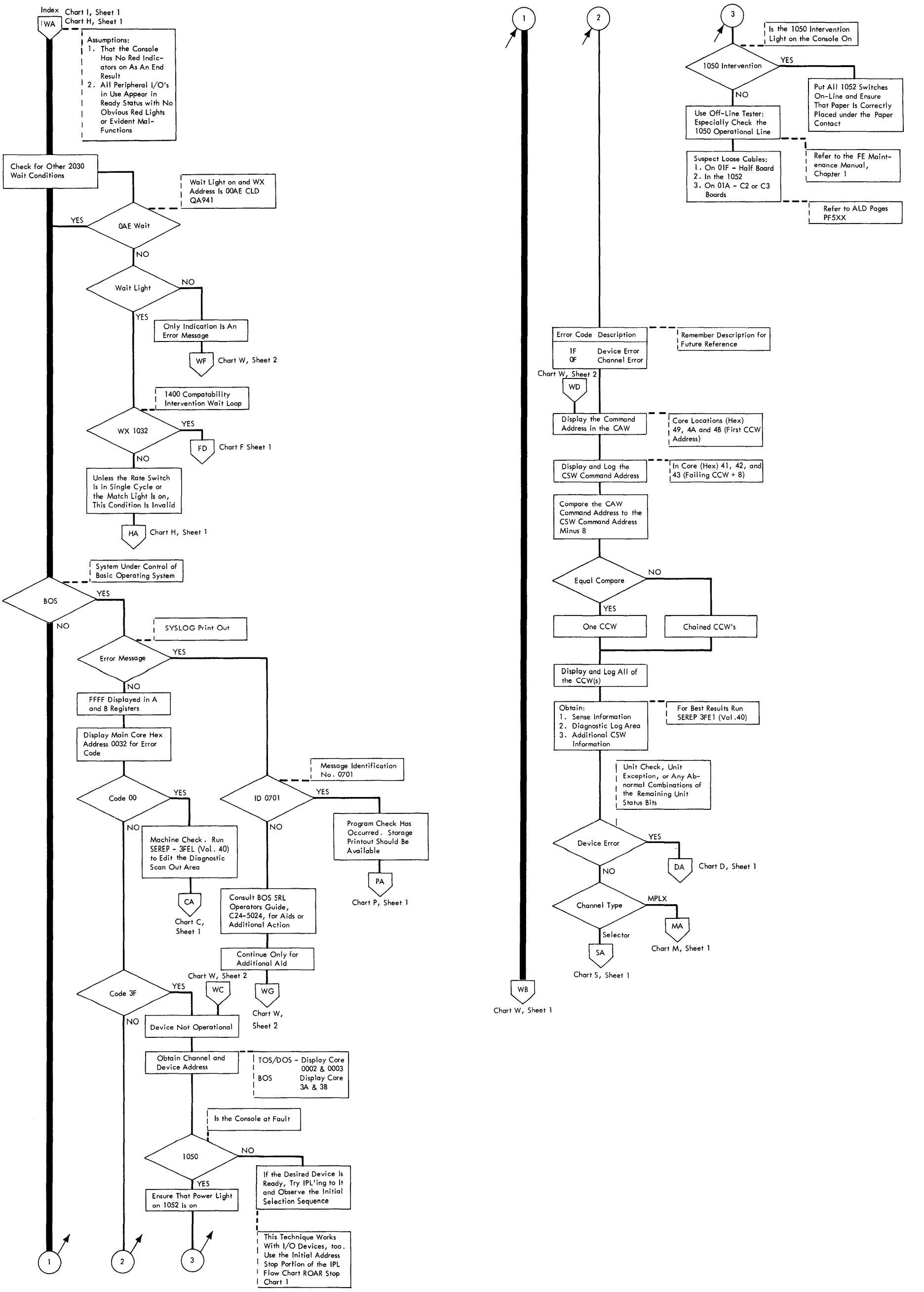
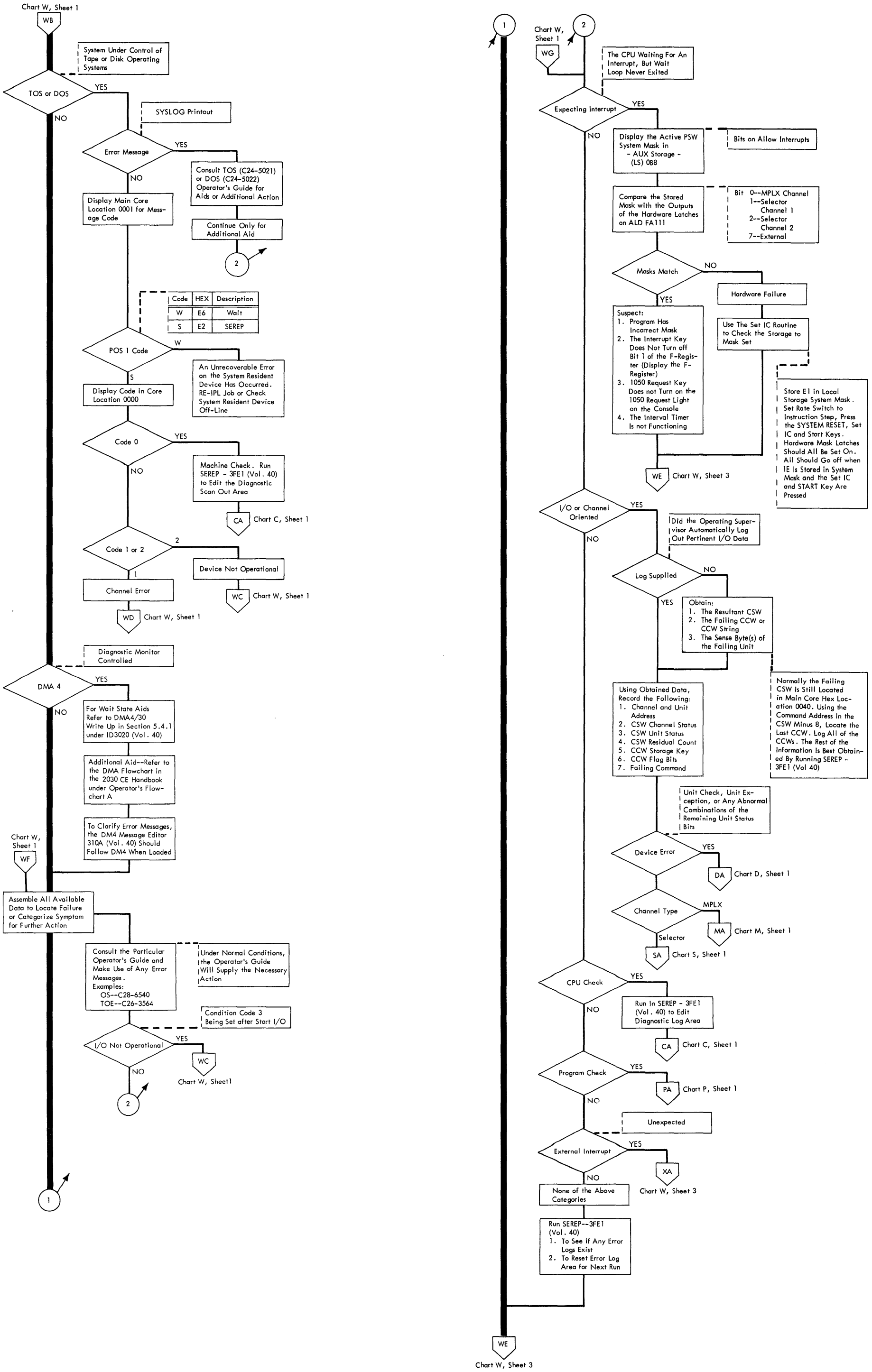


Chart S, Sheet 2
SC
Protect Check
YES
NO
Selector Log *
Inspect Failing CCW
Operation Bit 7 On
NO
YES
Input Operation
Output Operation
Skip Bit On
YES
NO
Protect Check Should Not Be Set
Run Selector FLT
GK-REG=0
NO
YES
Do Manual Storage Display Using GUV Data as Address
Suspect: Circuits on KW061, Key Matching Circuits
Display Q-Register Low
Q-Register, P-4567 Bits = Odd. GK-Register = Odd
Run Storage Protect Micro (3350) and Macro (33C9) Diagnostic Test
Check GK-Registers and Q-Low for Odd Parity
Good
Bad
Do a Storage Protection Stack Adjustment as Outlined in 2030 FEMM Chapter 4
GK = Q-Low
YES
NO
GK-Register P-Bit Failure
NO
YES
Run Storage Protect Micro (3350) and Macro (33C9) Diagnostic Test
Protect Stack Failure
Do a Storage Protection Stack Adjustment as Outlined in 2030 FEMM Chapter 4
GK Register Failure
Run Selector FLT * *
Could Be Program Problem
Run Storage Protect Micro (3350) and Macro (33C9) Diagnostic Test
For Additional Aid, Proceed to the Device Chart
Do a Storage Protection Stack Adjustment as Outlined in 2030 FEMM Chapter 4
DA
Chart D, Sheet 1



DT Chart WX Wait and/or Error Messages, Unexpected External Interrupt (Sheet 1)



DT Chart WX Wait and/or Error Messages, Unexpected External Interrupt (Sheet 2)

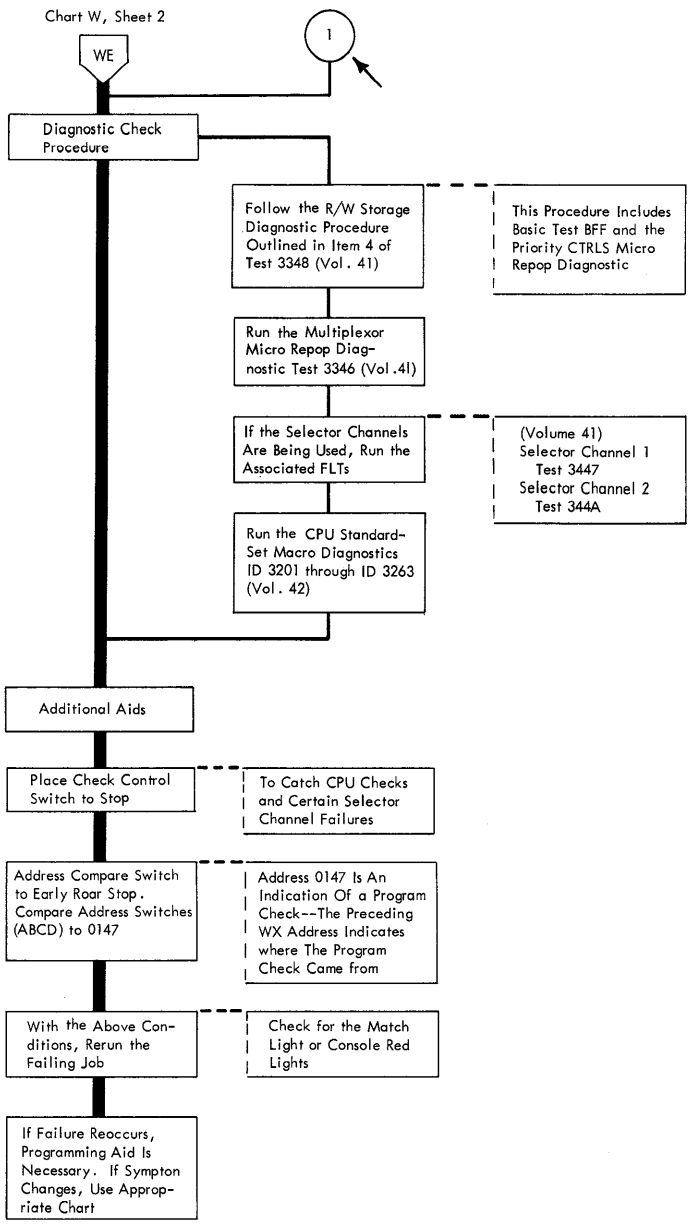
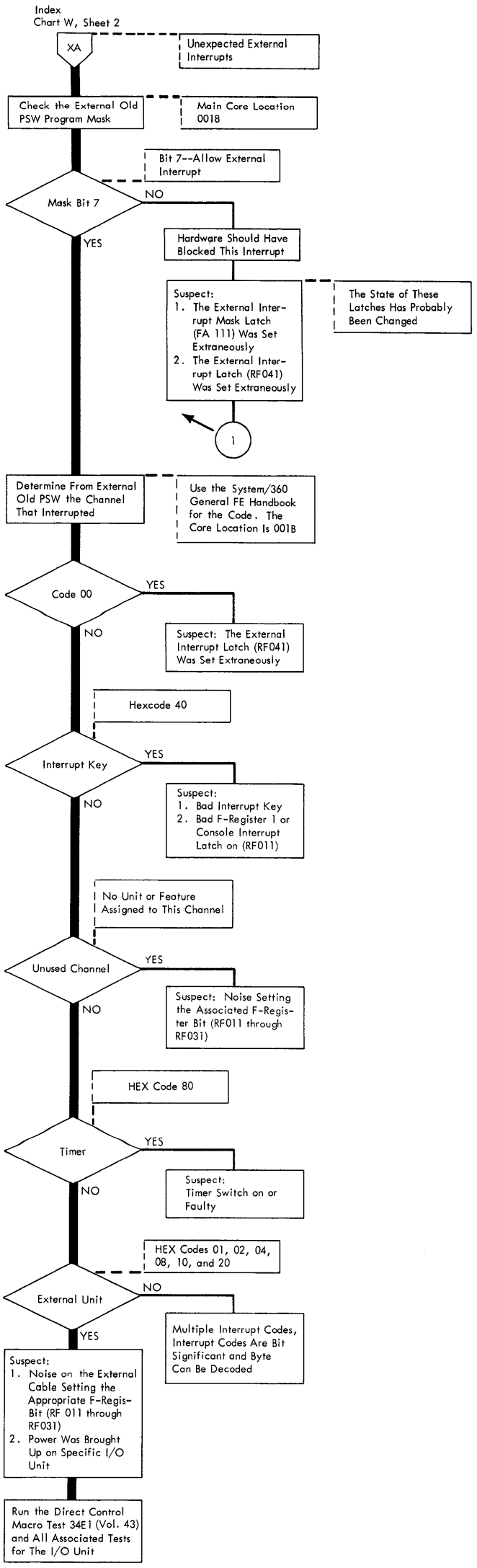
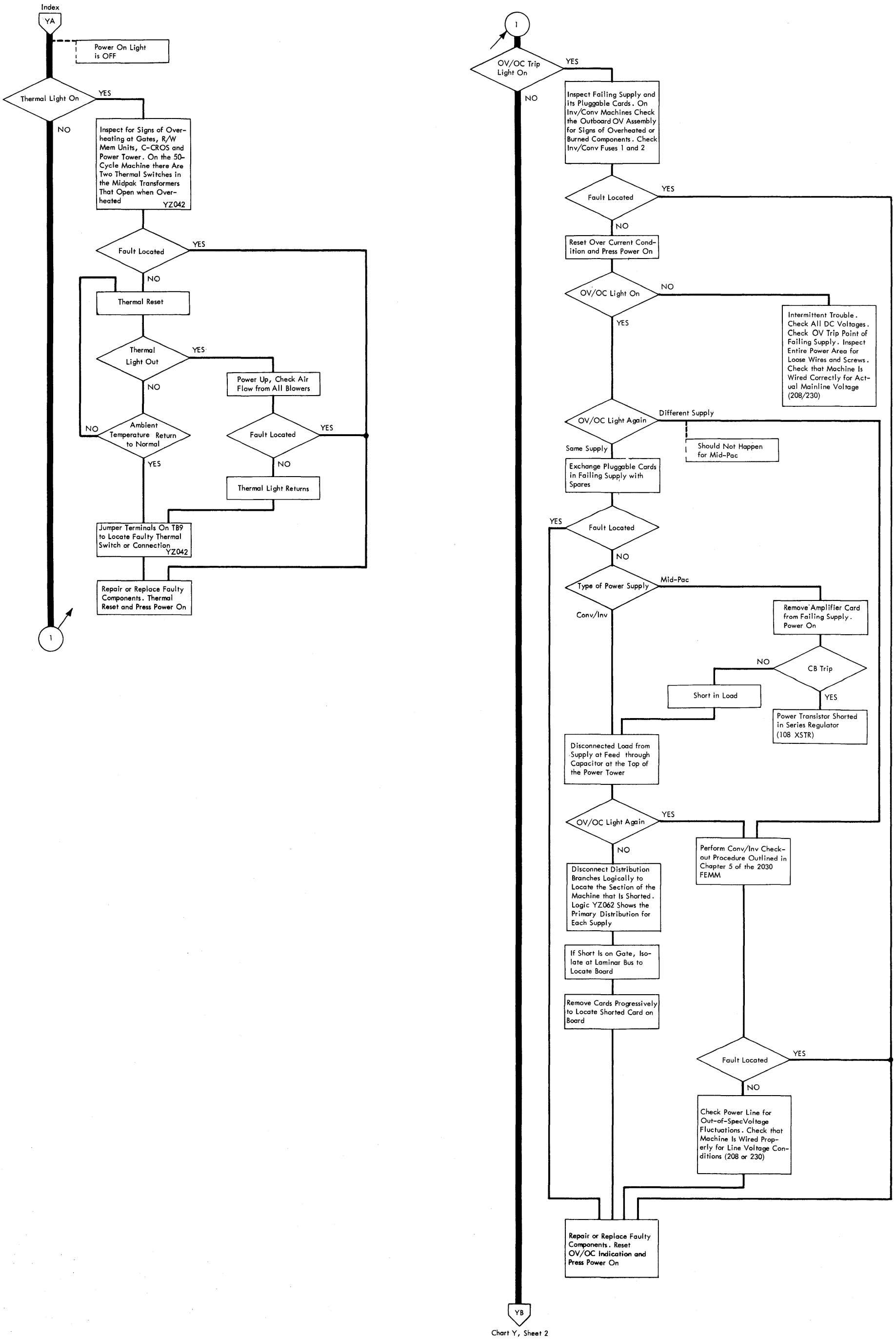


Chart W, Sheet 2
WE
1
Diagnostic Check Procedure
Follow the R/W Storage Diagnostic Procedure Outlined in Item 4 of Test 3348 (Vol. 41)
This Procedure Includes Basic Test BFF and the Priority CTRLS Micro Repop Diagnostic
Run the Multiplexor Micro Repop Diagnostic Test 3346 (Vol.41)
If the Selector Channels Are Being Used, Run the Associated FLTs
(Volume 41)
Selector Channel 1
Test 3447
Selector Channel 2
Test 344A
Run the CPU Standard-Set Macro Diagnostics ID 3201 through ID 3263 (Vol. 42)
Additional Aids
Place Check Control Switch to Stop
To Catch CPU Checks and Certain Selector Channel Failures
Address Compare Switch to Early Roar Stop. Compare Address Switches (ABCD) to 0147
Address 0147 Is An Indication Of a Program Check--The Preceding WX Address Indicates where The Program Check Came from
With the Above Conditions, Rerun the Failing Job
Check for the Match Light or Console Red Lights
If Failure Reoccurs, Programming Aid Is Necessary. If Sympton Changes, Use Appropriate Chart


Index
Chart W, Sheet 2
XA
Unexpected External Interrupts
Check the External Old PSW Program Mask
Main Core Location 0018
Bit 7--Allow External Interrupt
Mask Bit 7
NO
YES
Hardware Should Have Blocked This Interrupt
Suspect:
1. The External Interrupt Mask Latch (FA 111) Was Set Extraneously
2. The External Interrupt Latch (RF041) Was Set Extraneously
The State of These Latches Has Probably Been Changed
1
Determine From External Old PSW the Channel That Interrupted
Use the System/360 General FE Handbook for the Code. The Core Location Is 0018
Code 00
YES
NO
Suspect: The External Interrupt Latch (RF041) Was Set Extraneously
Hexcode 40
Interrupt Key
YES
NO
Suspect:
1. Bad Interrupt Key
2. Bad F-Register 1 or Console Interrupt Latch on (RF011)
No Unit or Feature Assigned to This Channel
Unused Channel
YES
NO
Suspect: Noise Setting the Associated F-Register Bit (RF011 through RF031)
HEX Code 80
Timer
YES
NO
Suspect: Timer Switch on or Faulty
HEX Codes 01, 02, 04, 08, 10, and 20
External Unit
NO
YES
Multiple Interrupt Codes, Interrupt Codes Are Bit Significant and Byte Can Be Decoded
Suspect:
1. Noise on the External Cable Setting the Appropriate F-Register Bit (RF 011 through RF031)
2. Power Was Brought Up on Specific I/O Unit
Run the Direct Control Macro Test 34E1 (Vol. 43) and All Associated Tests for The I/O Unit



DT Chart YZ Power and LP Light (Sheet 1)

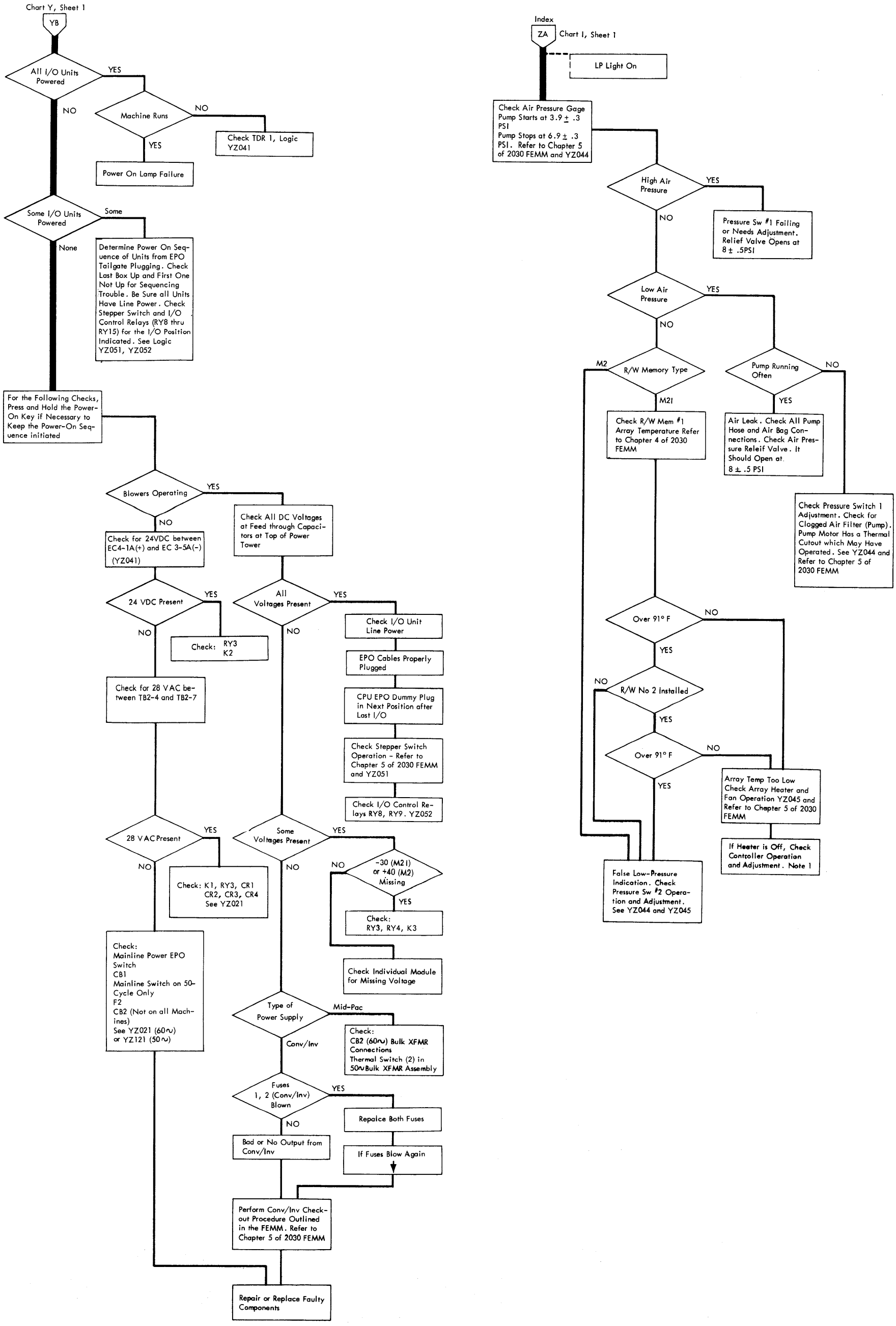


Chart Y, Sheet 1
YB
All I/O Units Powered
YES
NO
Machine Runs
NO
YES
Check TDR 1, Logic YZ041
Power On Lamp Failure
Some I/O Units Powered
Some
None
Determine Power On Sequence of Units from EPO Tailgate Plugging. Check Last Box Up and First One Not Up for Sequencing Trouble. Be Sure all Units Have Line Power. Check Stepper Switch and I/O Control Relays (RY8 thru RY15) for the I/O Position Indicated. See Logic YZ051, YZ052
For the Following Checks, Press and Hold the Power-On Key if Necessary to Keep the Power-On Sequence initiated
Blowers Operating
YES
NO
Check for 24VDC between EC4-1A(+) and EC 3-5A(-) (YZ041)
Check All DC Voltages at Feed through Capacitors at Top of Power Tower
24 VDC Present
YES
NO
Check: RY3 K2
All Voltages Present
YES
NO
Check I/O Unit Line Power
EPO Cables Properly Plugged
CPU EPO Dummy Plug in Next Position after Last I/O
Check Stepper Switch Operation - Refer to Chapter 5 of 2030 FEMM and YZ051
Check I/O Control Relays RY8, RY9. YZ052
Check for 28 VAC between TB2-4 and TB2-7
28 VAC Present
YES
NO
Check: K1, RY3, CR1 CR2, CR3, CR4 See YZ021
Some Voltages Present
YES
NO
-30 (M21) or +40 (M2) Missing
NO
YES
Check: RY3, RY4, K3
Check Individual Module for Missing Voltage
Check: Mainline Power EPO Switch CB1 Mainline Switch on 50-Cycle Only F2 CB2 (Not on all Machines) See YZ021 (60∿) or YZ121 (50∿)
Type of Power Supply
Mid-Pac
Conv/Inv
Check: CB2 (60∿) Bulk XFMR Connections Thermal Switch (2) in 50∿Bulk XFMR Assembly
Fuses 1, 2 (Conv/Inv) Blown
YES
NO
Repalce Both Fuses
If Fuses Blow Again
Bad or No Output from Conv/Inv
Perform Conv/Inv Checkout Procedure Outlined in the FEMM. Refer to Chapter 5 of 2030 FEMM
Repair or Replace Faulty Components
Index
ZA
Chart I, Sheet 1
LP Light On
Check Air Pressure Gage Pump Starts at 3.9 ± .3 PSI Pump Stops at 6.9 ± .3 PSI. Refer to Chapter 5 of 2030 FEMM and YZ044
High Air Pressure
YES
NO
Pressure Sw #1 Failing or Needs Adjustment. Relief Valve Opens at 8 ± .5PSI
Low Air Pressure
YES
NO
M2
R/W Memory Type
M21
Check R/W Mem #1 Array Temperature Refer to Chapter 4 of 2030 FEMM
Pump Running Often
NO
YES
Air Leak. Check All Pump Hose and Air Bag Connections. Check Air Pressure Releif Valve. It Should Open at 8 ± .5 PSI
Check Pressure Switch 1 Adjustment. Check for Clogged Air Filter (Pump). Pump Motor Has a Thermal Cutout which May Have Operated. See YZ044 and Refer to Chapter 5 of 2030 FEMM
Over 91° F
NO
YES
NO
R/W No 2 Installed
YES
Over 91° F
NO
YES
Array Temp Too Low Check Array Heater and Fan Operation YZ045 and Refer to Chapter 5 of 2030 FEMM
If Heater is Off, Check Controller Operation and Adjustment. Note 1
False Low-Pressure Indication. Check Pressure Sw #2 Operation and Adjustment. See YZ044 and YZ045

OVERALL SEQUENCE FOR 1st CARD

- Set F G H J Switches to Device Address
- Depress IPL Key
- BFF Runs 128 Times
- IPL Routine Forces 1st CCW in Core 00, Format 020000-0060000018 Command Chaining On
- Force SIO, Execute 1st CCW
- Determine if Using Sel Chan or Mpx Chan
  S2=1=Sel
  S2=0=Mpx
- Init Sel Seq Start
- Start Data Handling Seq
- Stop Data Handling Seq When CT=0
- CE, Check CE Status for Error, Issue Serv Out Do Not Put CE in IB Feed a Card
- Trap to 010
- DE Status, Check, Service Out Issued
- 1st Card Loaded
  1. PSW in 00
  2. CCW in 08
  3. CCW in 10

DETAILED SEQUENCE FOR 1st CARD

INFORMATION	ROS ADDRESS	LOGIC PAGE
MPX or SEL Channel S2=1=Sel S2=0=Mpx	588	QC011
Addr Out-Supp Out	5AO	QC051
Addr Out-Sel Out Op In	59D	QC051
Op In-Addr In	5A8	QC051
Stat In-Op In	5B0	QC051
Enter Data Loop	6C1	QC231
Op In-Serv In Count=0	62F	QC081
Op In-Stat In FI=CE 00001000 Feed Card	61D	QC081
Supp Out-Stat In-Op In FI=CE Issue Serv Out	638	QC121
Supp Out	67A	QC161
Trap to 010 Caused by DE Int	010	QC201
Check for Stat In	6C1	QC231
Serv Out Issued to Stat In	6B1	QC131
Start Getting Next CCW	6B9	QC131
Finish with CCW Ready to Execute	5E9	QC031

OVERALL SEQUENCE FOR DATA FLOW 2nd CARD

- Force Start I/O To Execute 2nd CCW
- Initial Sel Seq
- Data Handling Start
- Control Unit Initiates The CE Sequence
- CE Status Checked for Error, CE Not Put In IB, Feed Card
- DE Causes MPX Channel Trap to 010
- DE Status Checked, OK, Serv Out Issued
- 2nd Card Loads Data Starting at Addr 288

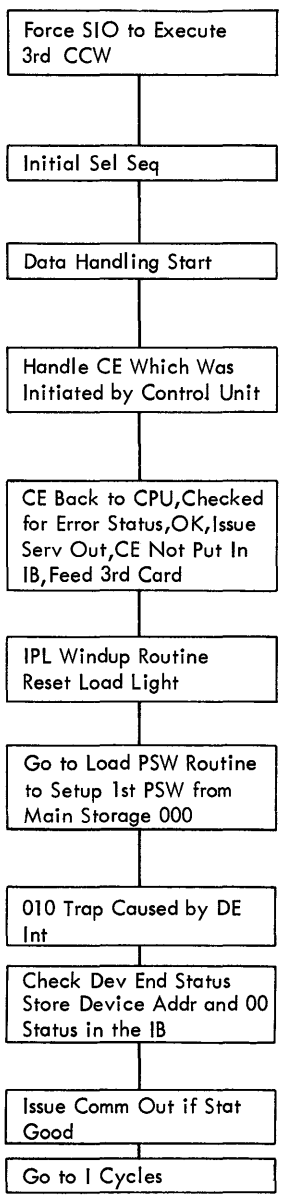
DETAILED SEQUENCE FOR 2nd CARD

INFORMATION	ROS ADDRESS	LOGIC PAGE
Addr Out-Supp Out	5AO	QC051
Addr Out-Sel Out Op In	59D	QC051
Op In-Addr In	5A8	QC051
Stat In-Op In End of Initial Sel Seq	5B0	QC051
Enter Data Loop	6C1	QC231
Cont Unit Ends Data Handling	6A7	QC111
Supp Out-Stat In Op In FI=CE Issue Serv Out	638	QC121
Supp Out	67A	QC161
Trap to 010 Caused by DE Int	010	QC201
Check for Stat In	6C1	QC231
Serv Out Issued	6B1	QC131
Start Getting Next CCW	6B9	QC131
Finish with CCW Ready to Execute	5E9	QC031

IPL Three Card Hex Loader--MPX Channel Burst Mode RS Chart 1 (Sheet 1)

IPL THREE CARD HEX LOADER - MPX CHANNEL BURST MODE

OVERALL SEQUENCE FOR 3rd CARD

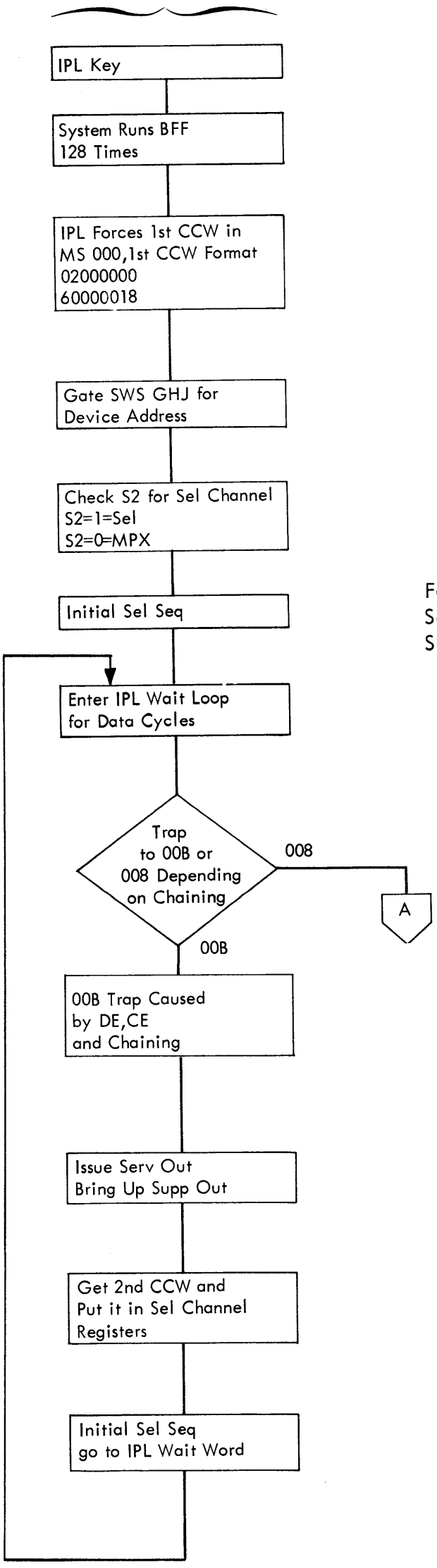


DETAILED SEQUENCE FOR 3rd CARD

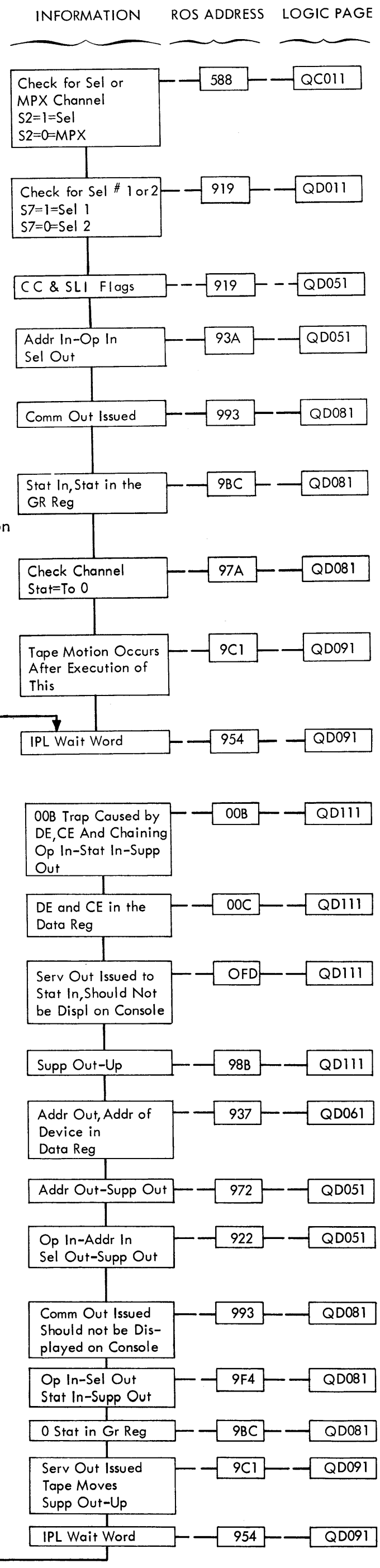
INFORMATION	ROS ADDRESS	LOGIC PAGE
Addr Out-Supp Out	5AO	QC051
Addr Out-Sel Out Op In	59D	QC051
Op In-Addr In	5A8	QC051
Stat In-Op In, End of Initial Sel Seq	5B0	QC051
Enter Data Loop	6C1	QC231
Control Unit End Initiates CE Status Prepare for IPL Windup	647	QC121
Reset Load Light	6FE	QC351
Enter LPSW Rtne	0377	QA921
I Cycle Start	109	QA001
DE Stat Causes Trap to 010	010	QC201
Load IB with Dev Addr	63D	QC121
Load IB with 00 Stat	640	QC121
Issue Comm Out to Stat In	64D	QC121
Restore CPU	6D9	QC311
Restore WX Reg	67F	QC311

SELECTOR CHANNEL - TAPE & FILE IPL

OVER-ALL SEQUENCE



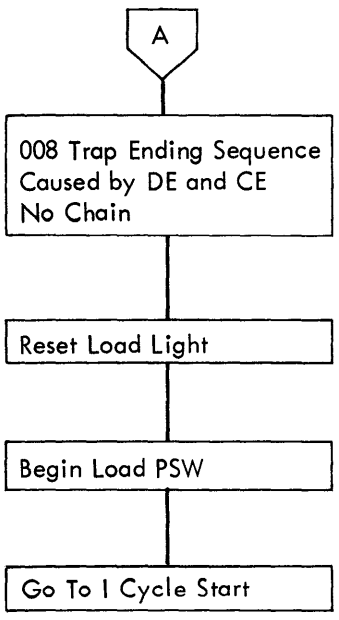
DETAILED SEQUENCE



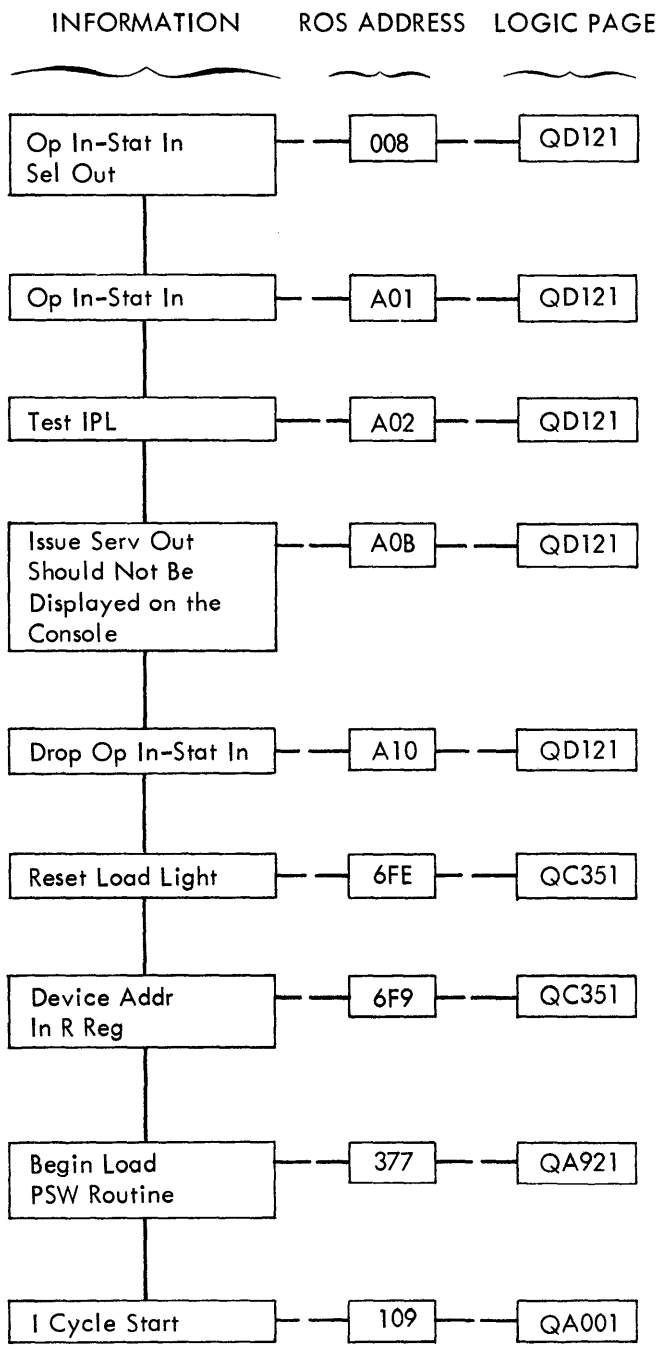
Selector Channel--Tape and File IPL RS Chart 2 (Sheet 1)

SELECTOR CHANNEL - TAPE & FILE IPL

OVER-ALL SEQUENCE



DETAILED SEQUENCE



NOTE:

1. File Control Unit Decodes the 02 as a Read IPL
2. Control Unit Causes a Seek to Cylinder Zero
3. Selects Head Zero
4. Search Address Mark on Record One
5. Reads Record One Data Field (24 Byte Loader)
6. Present Ending Status
7. Channel takes an 00B Trap if Chaining is designated in the Selector Channel GF Register

I OBJECTIVE APPROACH TO CHANNELS

A. Enter the following program using the illustrated variables desired to simulate your failure. Enter the program by using either manual store or BF6.

NOTE: Clear Memory using BF8 prior to entering program.

Review of BF6 procedure:

1. System Reset
2. Set IC to 1st Address to be Altered
3. Roar Reset to BF6
4. Start
5. Set Switches HJ to Desired Character
6. Start
7. Repeat Step 5 & 6 until Data Entry is Complete
8. Set IC to 500; Depress Start

By insertion of the following instructions in front of the I/O program, we can simulate customer operation. This is accomplished by introducing a time constant prior to execution of the I/O program.

MAIN STORAGE ADDRESS

Load Reg	04F8	41	10	01	00
Branch on Count	04FC	46	10	04	FC

0500 - Beginning of I/O Program

In the above example, we load register 1 with a value of Hex 100 which in turn causes the Branch on Count instruction to cycle 256 times prior to entering the I/O program. It should be noted that by changing the address in the Load Reg instruction varies the cycle time on the Branch on Count instruction.

MAIN STORAGE ADDRESS

Test I/O	0500	9D	00	0X	XX				
	0504	47	70	05	00				
Start I/O	0508	9C	00	0X	XX				
	050C	47	70	05	08				
	0510	47	F0	05	00				
CAW	0048	00	00	06	00				
CCW	0600	XX	00	07	01	20	00	00	XX

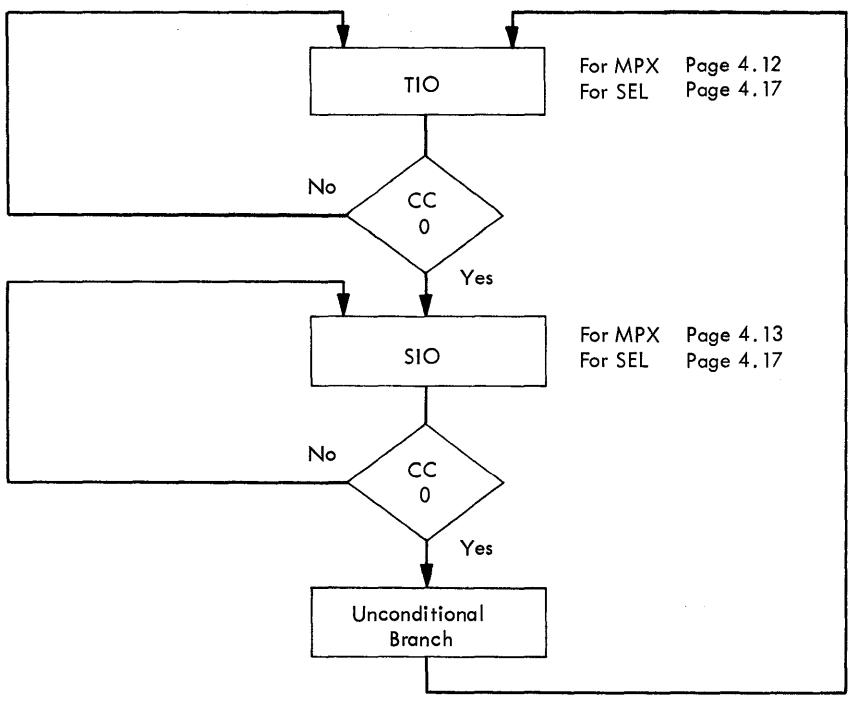
Channel And Device Address

Command Code

Count

Write	01	30	Less Than Buffer Size
Read	02	50	Buffer Size
Write/Space	09	30	Less Than Buffer Size
		50	Buffer Size
		30	Less Than Buffer Size
		84	Buffer Size

PROGRAM FLOW IN INSTRUCTION STEP FOR SELECTOR/MPX CHANNELS



Address of Next Instruction Displayed in A & B Reg in Instruction Step.

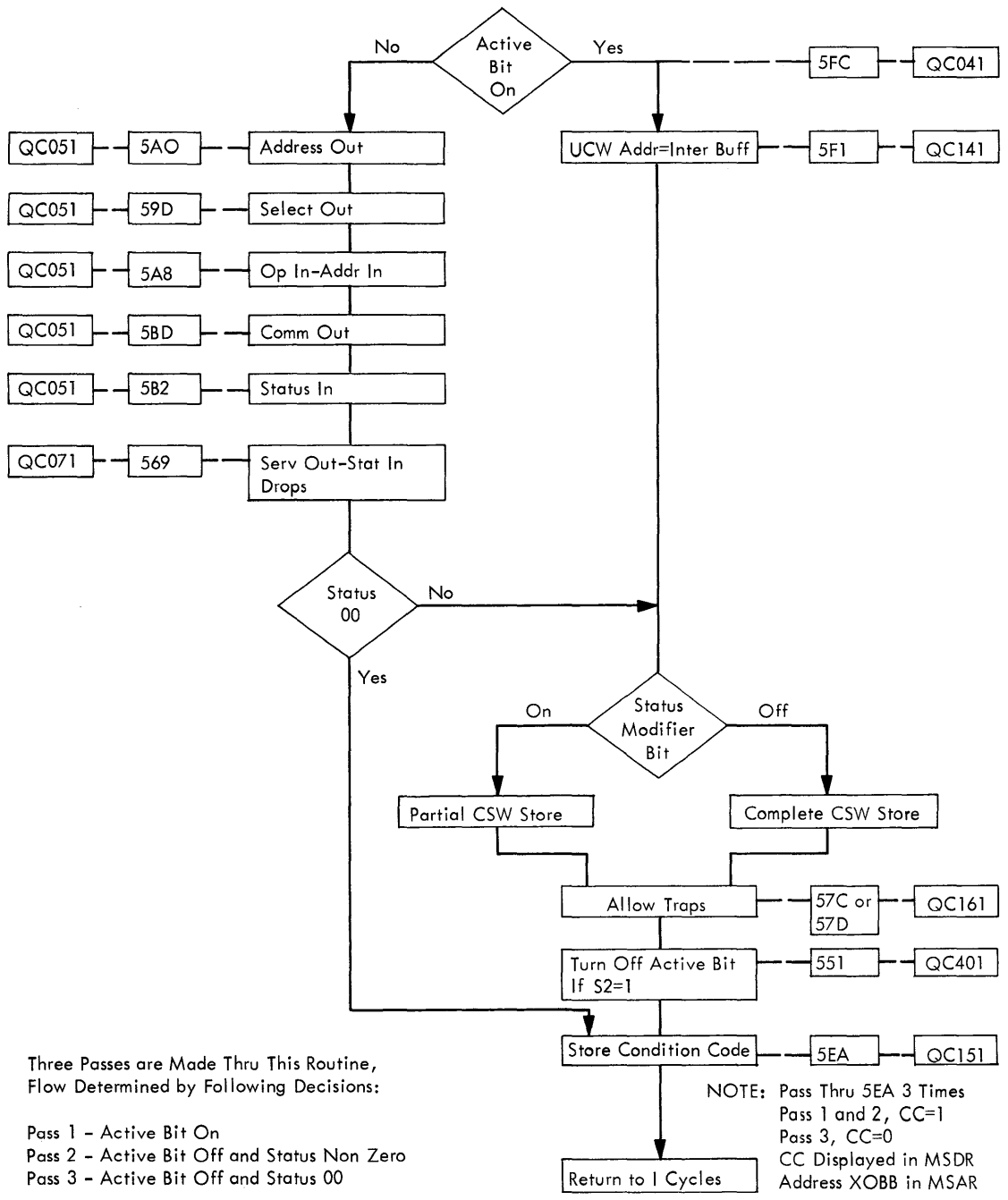
NOTE: Initial Test I/O after System Reset has:
CC = 0,
IB = 00
CSW = 00

Condition Code settings shown in charts are after execution of instruction.

MPX - Channel Address Trace	500	504	500	504	500	504	508	50C	510
Condition Code	1		1		0		0		
Interrupt - Buffer	00		00		00		08		
CSW - Byte 44	08	08	04	04	04	04	04	04	04
CSW - Byte 45	00	00	00	00	00	00	00	00	00

SEL- Channel Address Trace	500	504	500	504	508	50C	510
Condition Code	1		1	0	0	0	0
CSW - Byte 44	0C	0C	0C	0C	0C	0C	0C
CSW - Byte 45	00	00	00	00	00	00	00

TEST I/O - MPX - PRINTER - READER - PUNCH

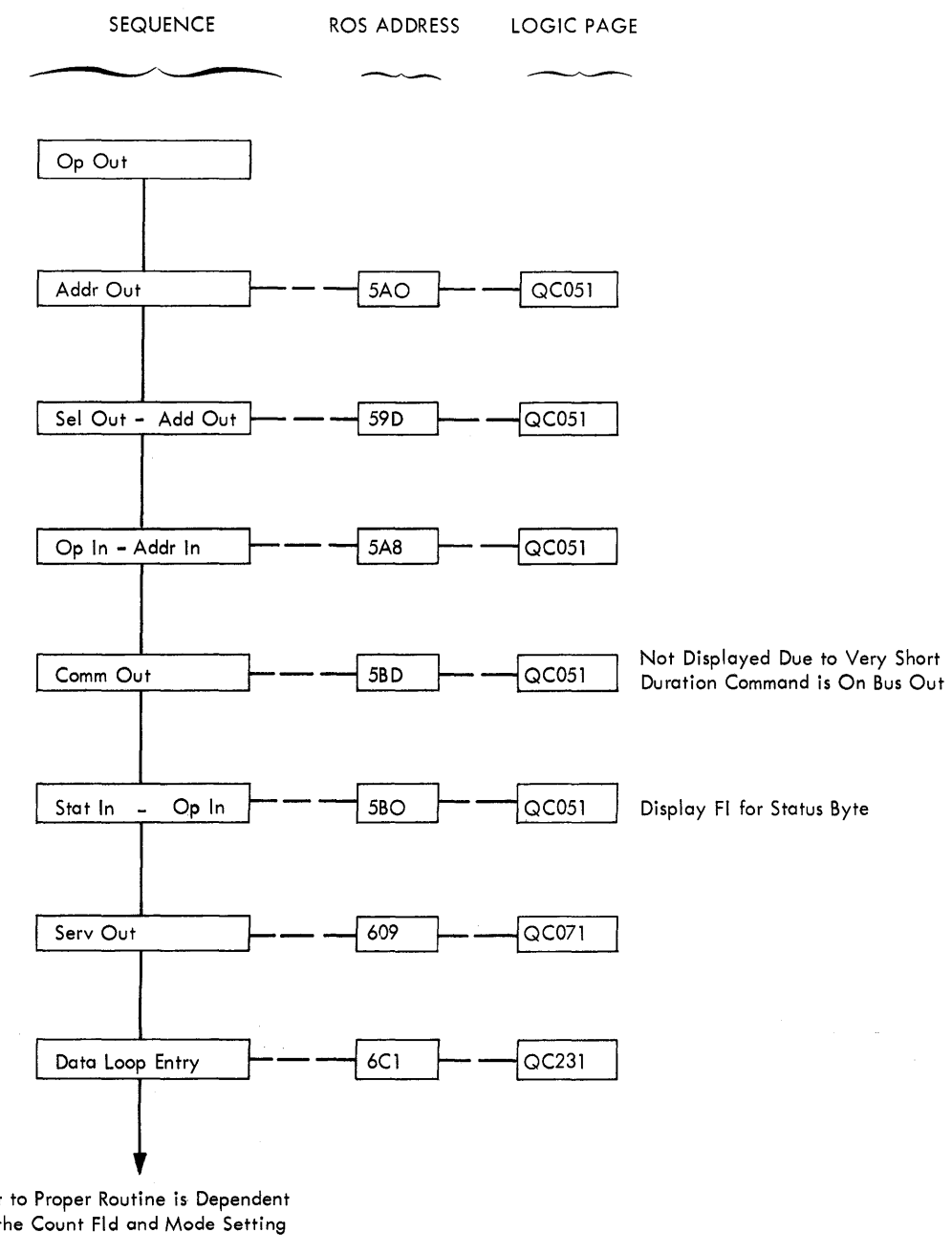


Three Passes are Made Thru This Routine,
Flow Determined by Following Decisions:

Pass 1 - Active Bit On
Pass 2 - Active Bit Off and Status Non Zero
Pass 3 - Active Bit Off and Status 00

NOTE: Pass Thru 5EA 3 Times
Pass 1 and 2, CC=1
Pass 3, CC=0
CC Displayed in MSDR
Address XOBB in MSAR

MPX - SIO INITIAL SELECTION

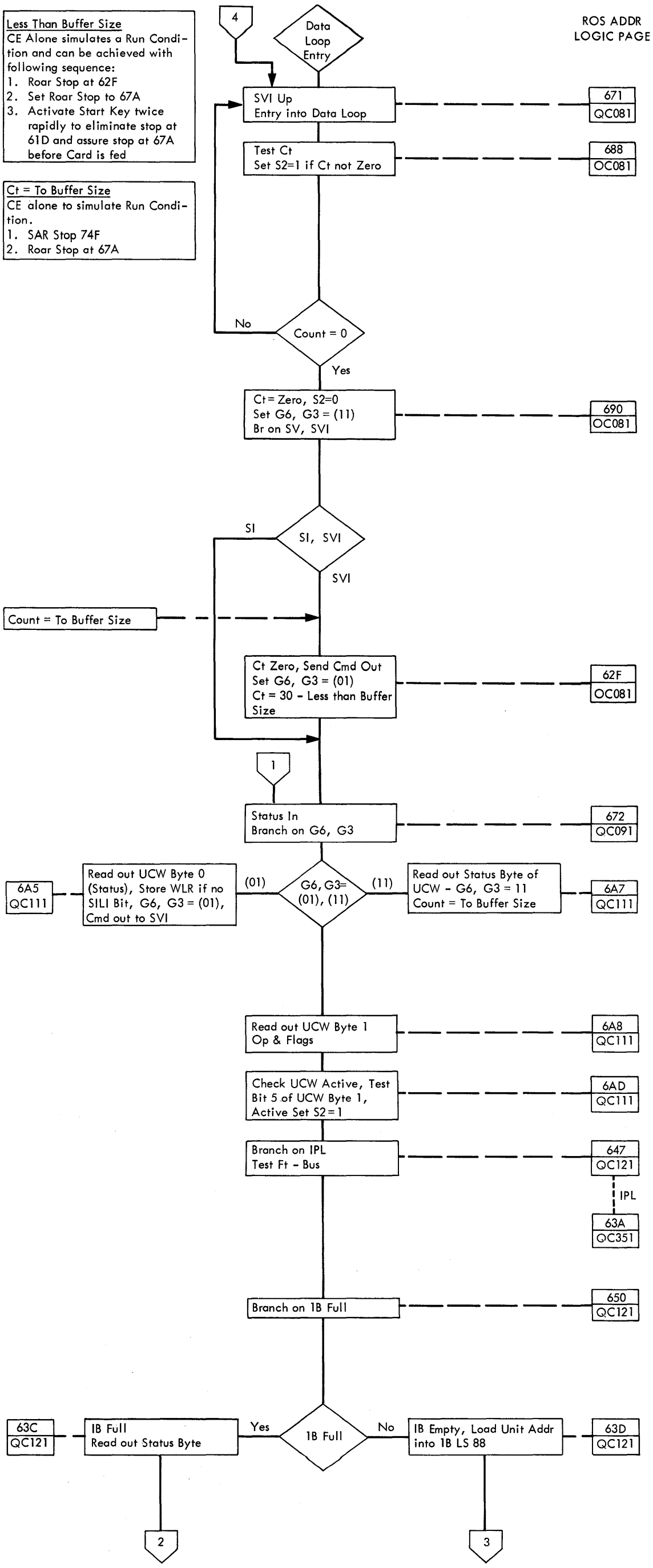


Not Displayed Due to Very Short Duration Command is On Bus Out

Display FI for Status Byte

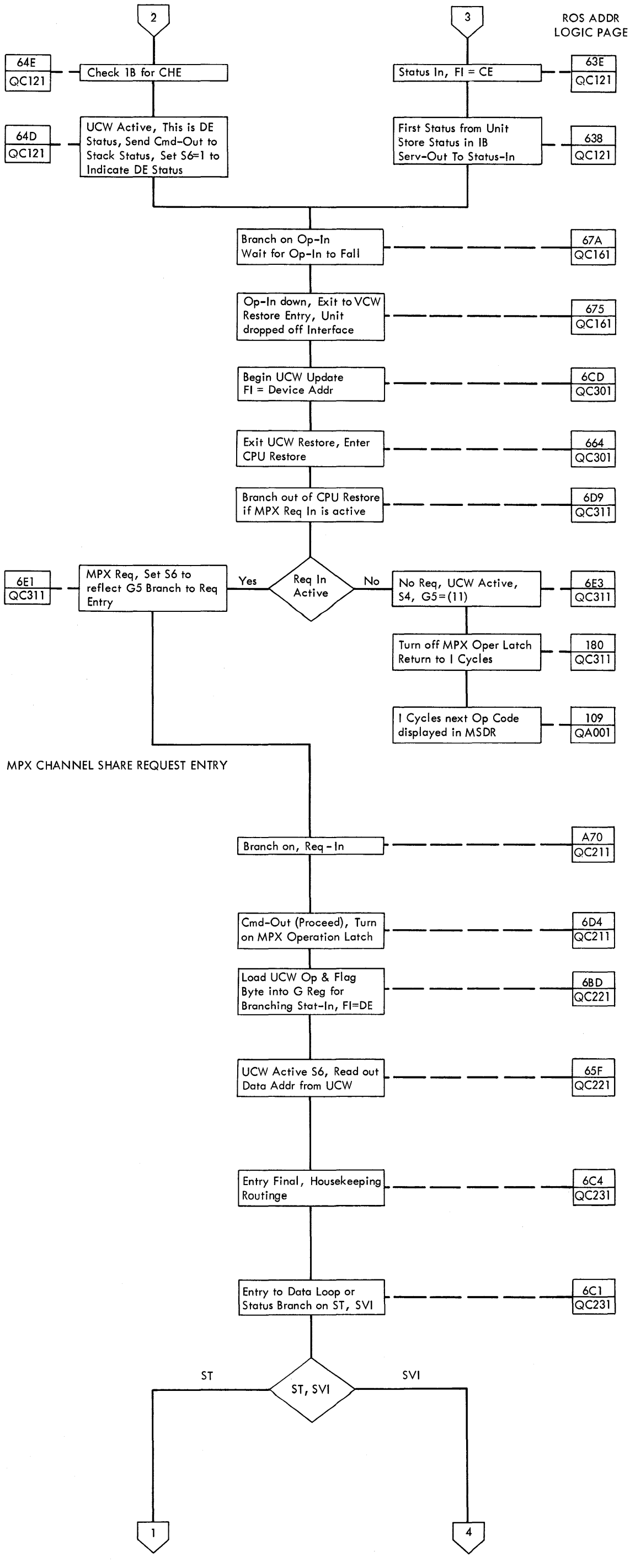
Exit to Proper Routine is Dependent on the Count Fld and Mode Setting

MPX - SIO INPUT/OUTPUT BURST OR BYTE MODE CHART REPRESENTS = TO AND LESS THAN BUFFER SIZE

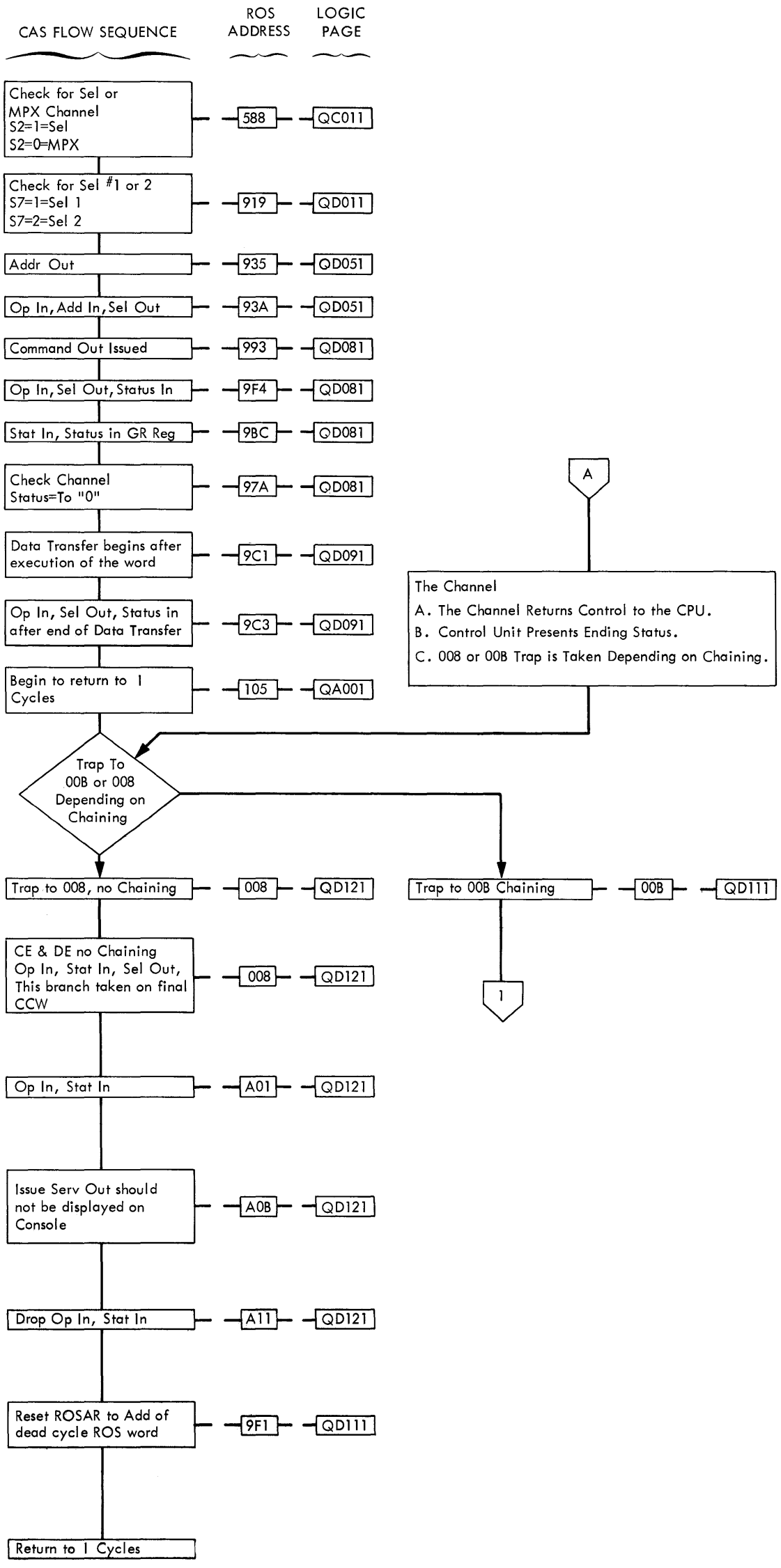


MPX--SIO Input/Output Burst or Byte Mode RS Chart 4 (Sheet 1)

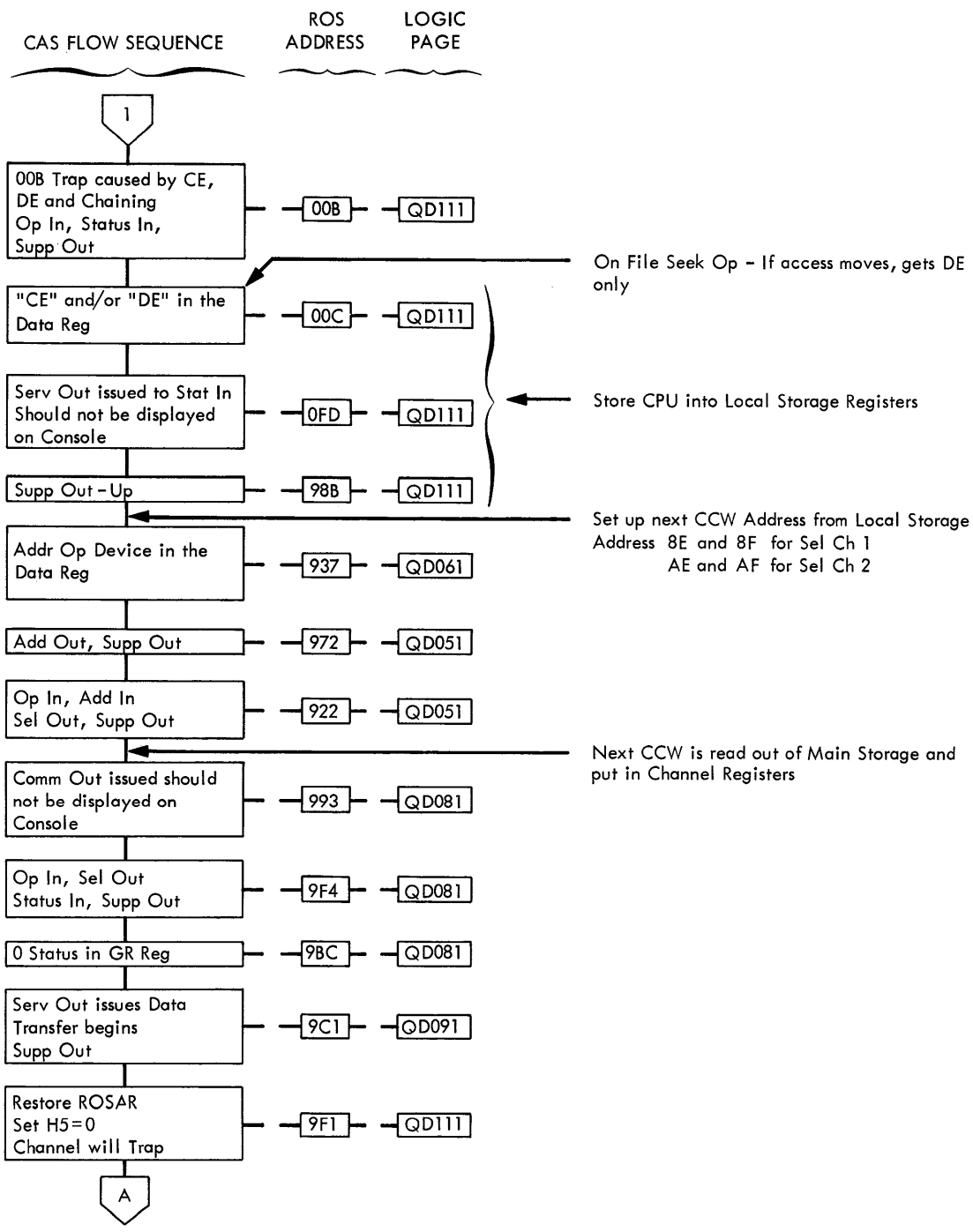
MPX - SIO INPUT/OUTPUT OR BYTE MODE CHART REPRESENTS = TO AND LESS THAN BUFFER SIZE

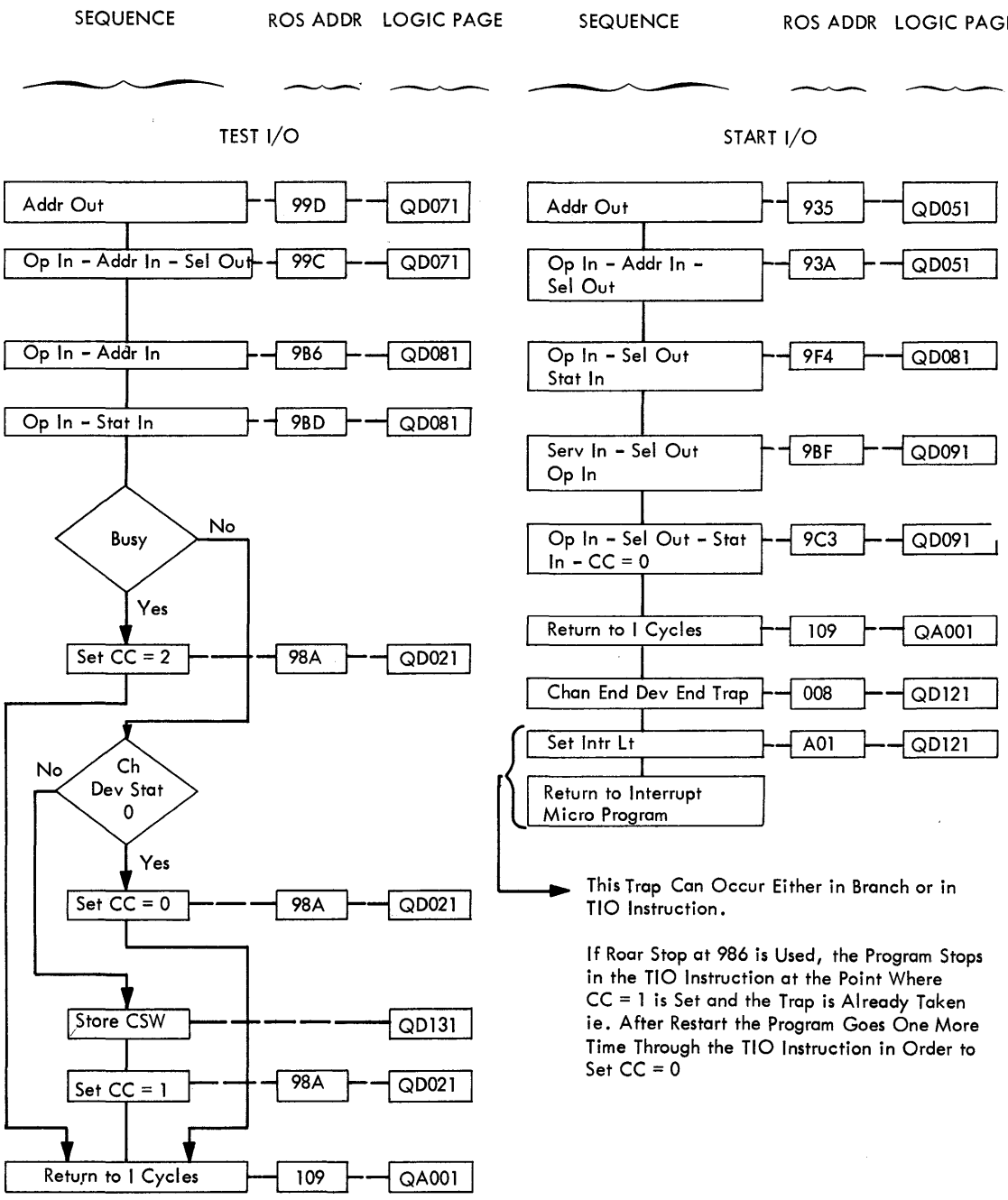


MPX--SIO Input/Output Burst or Byte Mode RS Chart 4 (Sheet 2)

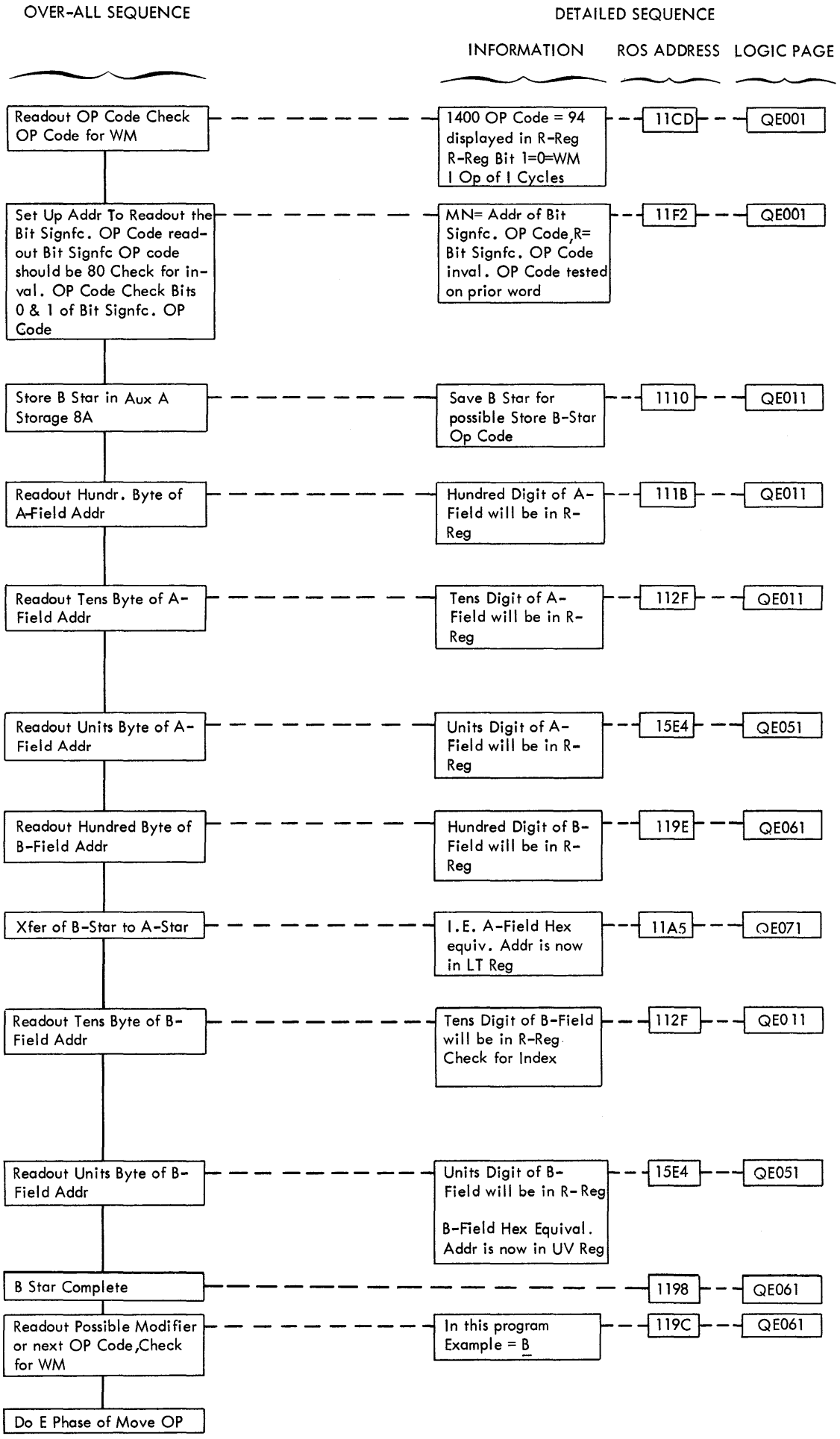

CAS FLOW SEQUENCE
ROS ADDRESS
LOGIC PAGE
Check for Sel or MPX Channel S2=1=Sel S2=0=MPX
588
QC011
Check for Sel #1 or 2 S7=1=Sel 1 S7=2=Sel 2
919
QD011
Addr Out
935
QD051
Op In, Add In, Sel Out
93A
QD051
Command Out Issued
993
QD081
Op In, Sel Out, Status In
9F4
QD081
Stat In, Status in GR Reg
9BC
QD081
Check Channel Status=To "0"
97A
QD081
Data Transfer begins after execution of the word
9C1
QD091
Op In, Sel Out, Status in after end of Data Transfer
9C3
QD091
Begin to return to I Cycles
105
QA001
A
The Channel
A. The Channel Returns Control to the CPU.
B. Control Unit Presents Ending Status.
C. 008 or 00B Trap is Taken Depending on Chaining.
Trap To 00B or 008 Depending on Chaining
Trap to 008, no Chaining
008
QD121
Trap to 00B Chaining
00B
QD111
1
CE & DE no Chaining Op In, Stat In, Sel Out, This branch taken on final CCW
008
QD121
Op In, Stat In
A01
QD121
Issue Serv Out should not be displayed on Console
A0B
QD121
Drop Op In, Stat In
A11
QD121
Reset ROSAR to Add of dead cycle ROS word
9F1
QD111
Return to I Cycles

TRAP, CHAINING ON SELECTOR CHANNEL



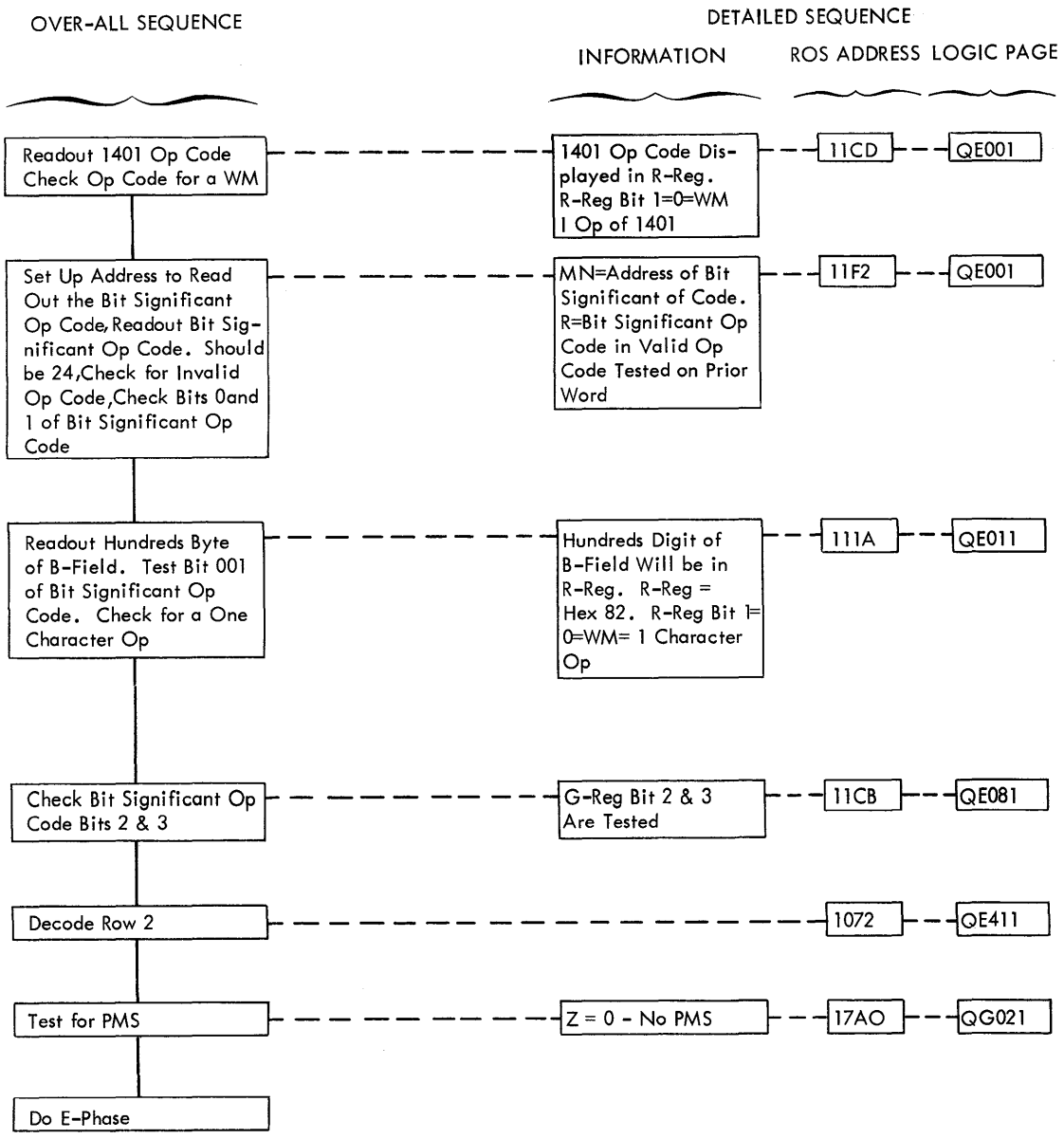

SEQUENCE
ROS ADDR
LOGIC PAGE
TEST I/O
Addr Out
99D
QD071
Op In - Addr In - Sel Out
99C
QD071
Op In - Addr In
9B6
QD081
Op In - Stat In
9BD
QD081
Busy
No
Yes
Set CC = 2
98A
QD021
No
Ch Dev Stat 0
Yes
Set CC = 0
98A
QD021
Store CSW
QD131
Set CC = 1
98A
QD021
Return to I Cycles
109
QA001
SEQUENCE
ROS ADDR
LOGIC PAGE
START I/O
Addr Out
935
QD051
Op In - Addr In - Sel Out
93A
QD051
Op In - Sel Out Stat In
9F4
QD081
Serv In - Sel Out Op In
9BF
QD091
Op In - Sel Out - Stat In - CC = 0
9C3
QD091
Return to I Cycles
109
QA001
Chan End Dev End Trap
008
QD121
Set Intr Lt
A01
QD121
Return to Interrupt Micro Program
This Trap Can Occur Either in Branch or in TIO Instruction.
If Roar Stop at 986 is Used, the Program Stops in the TIO Instruction at the Point Where CC = 1 is Set and the Trap is Already Taken ie. After Restart the Program Goes One More Time Through the TIO Instruction in Order to Set CC = 0

1400 COMPATIBILITY I CYCLE
500 M 555 666
507 B
555
666 I



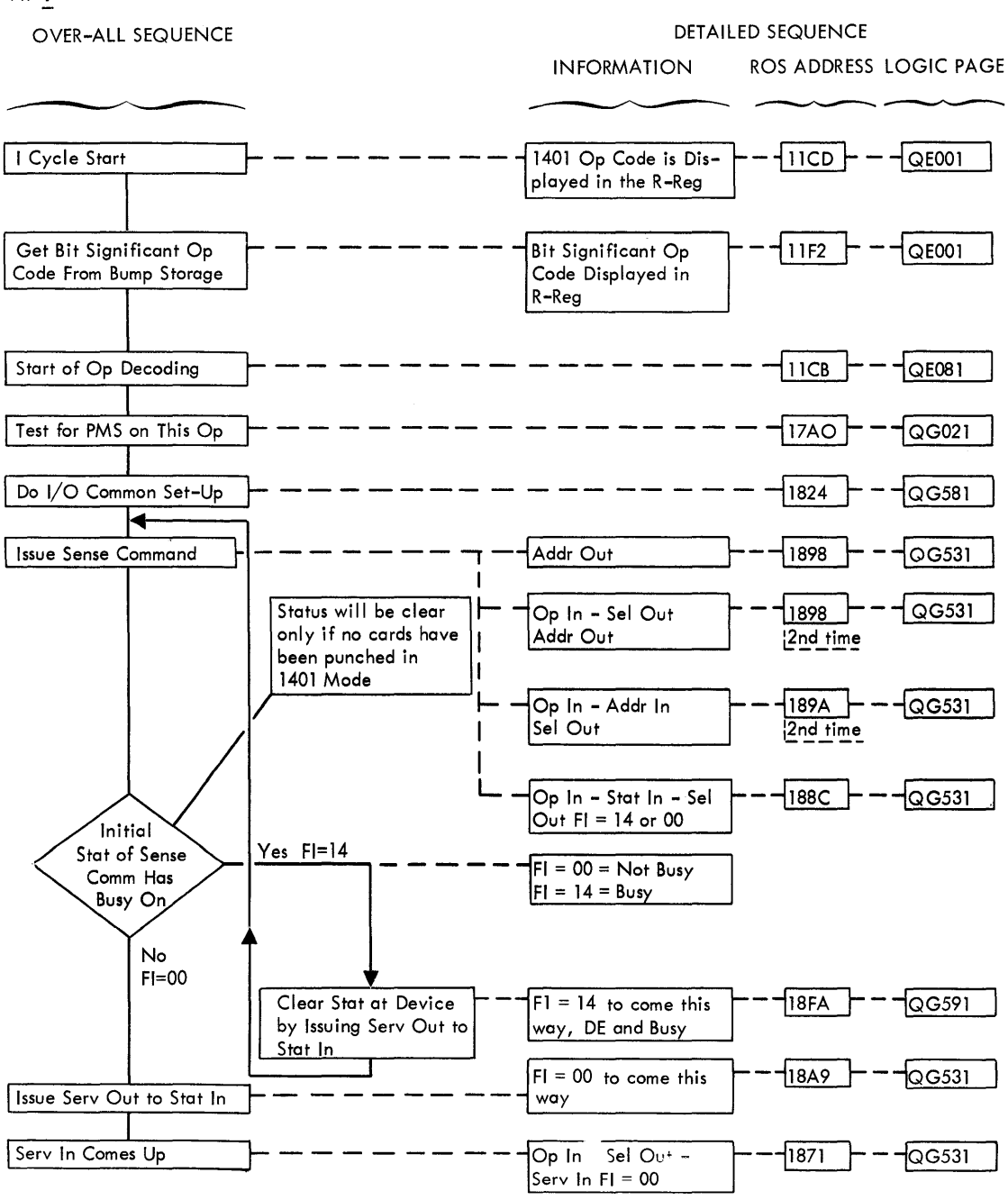
1401 COMPATIBILITY PUNCH OPERATION - I-CYCLES FOR 4 OP

444 4
445 B 444
449 .



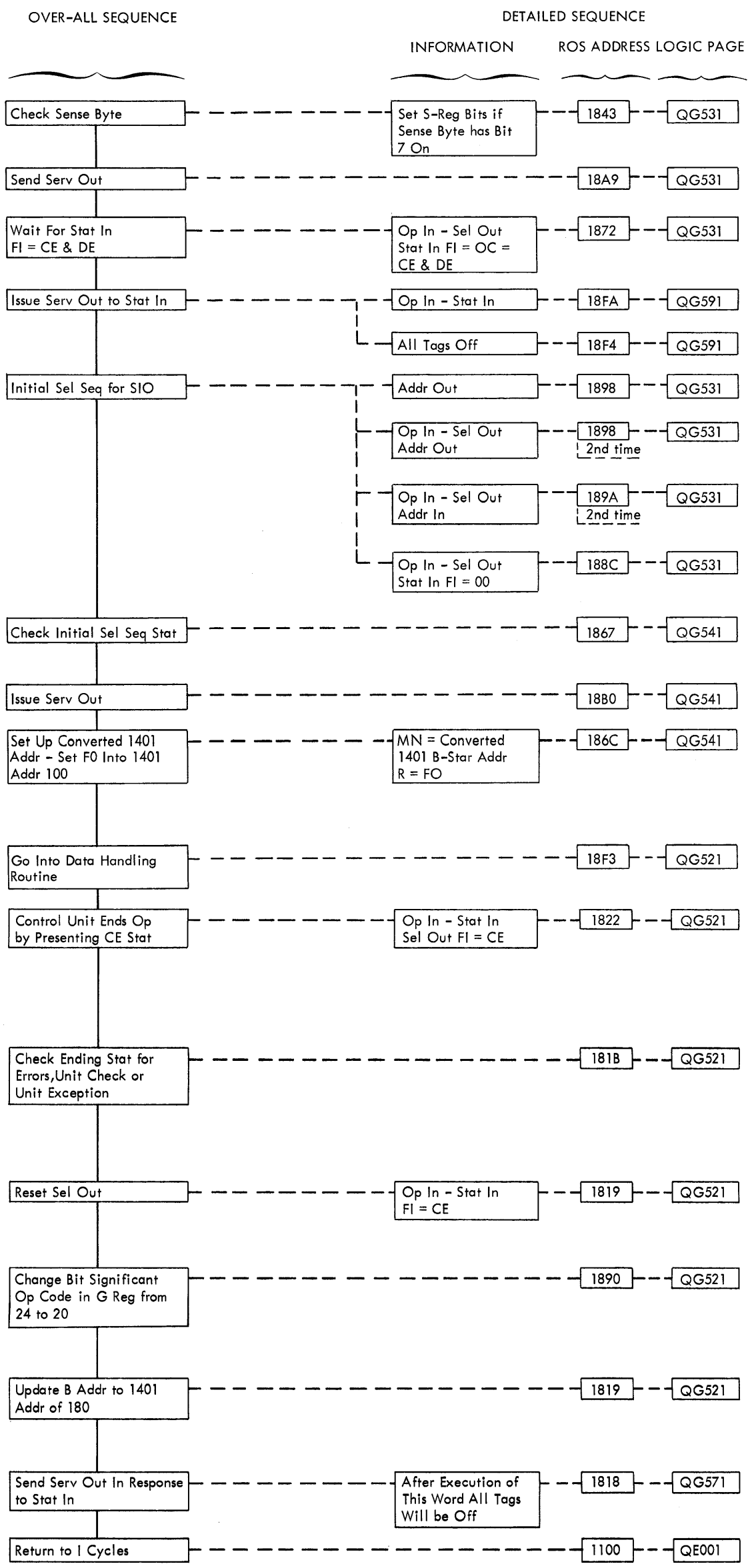
1401 COMPATIBILITY PUNCH OPERATION - EXECUTE

444 4
445 B 444
449 .



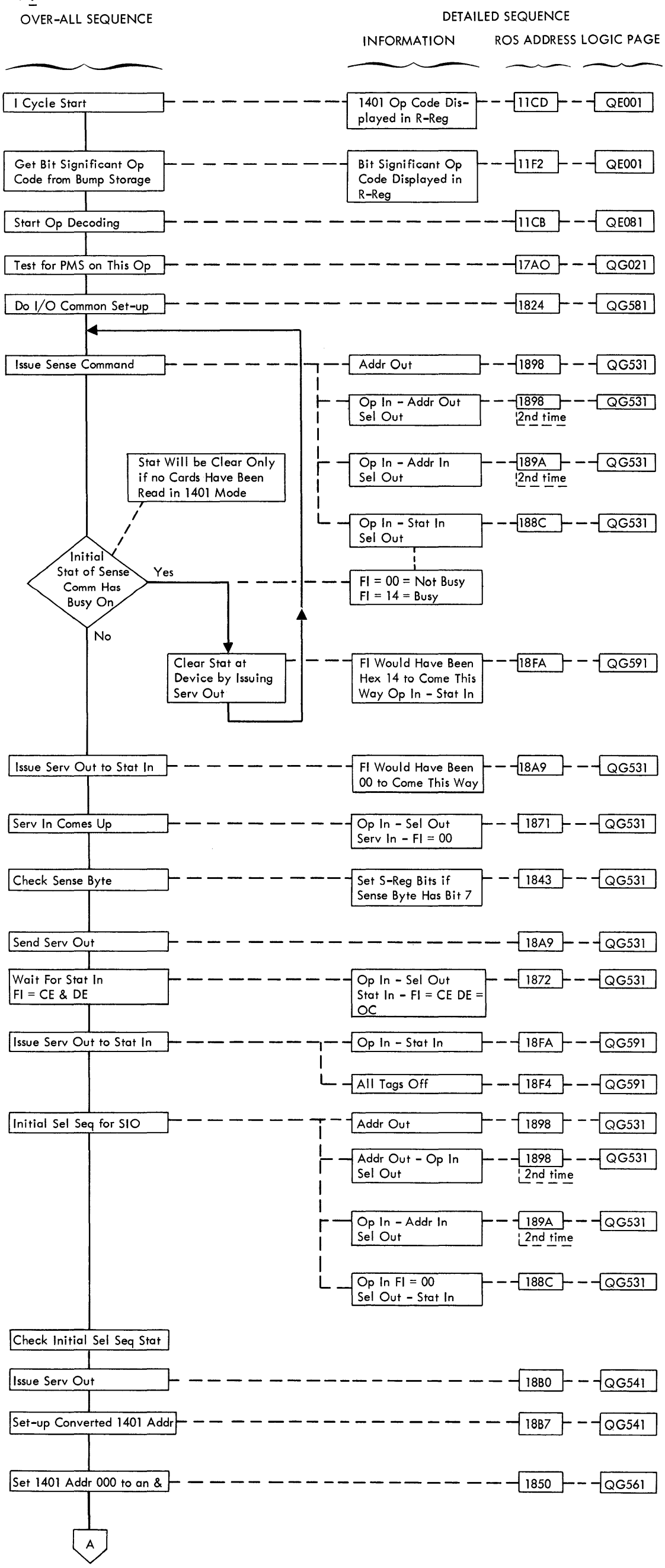
1401 Compatibility Punch Operation RS Chart 8 (Sheet 1)

1401 COMPATIBILITY PUNCH OPERATION - EXECUTE

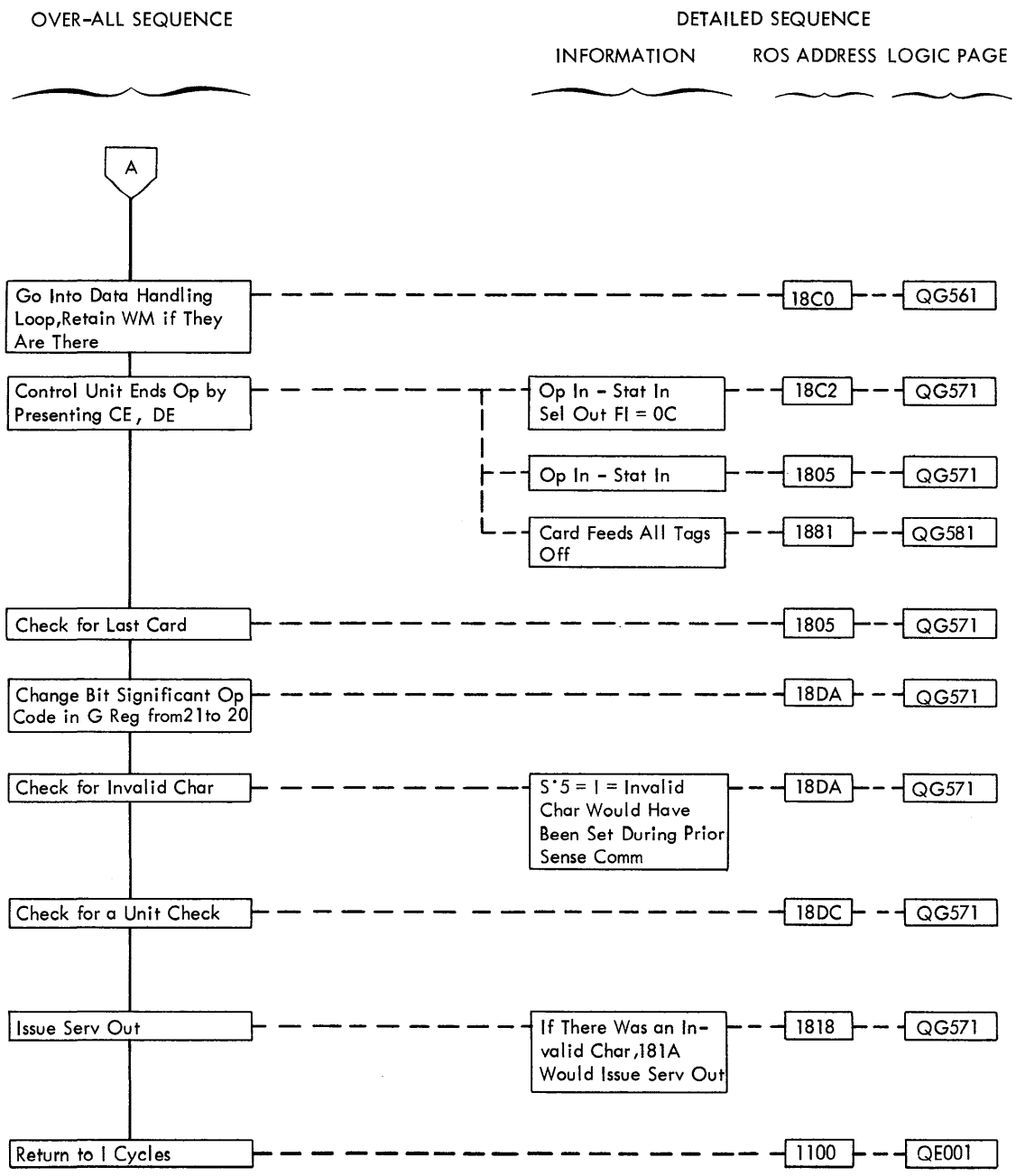


1401 COMPATIBILITY READ OPERATION

444 1
445 B 444
449 •

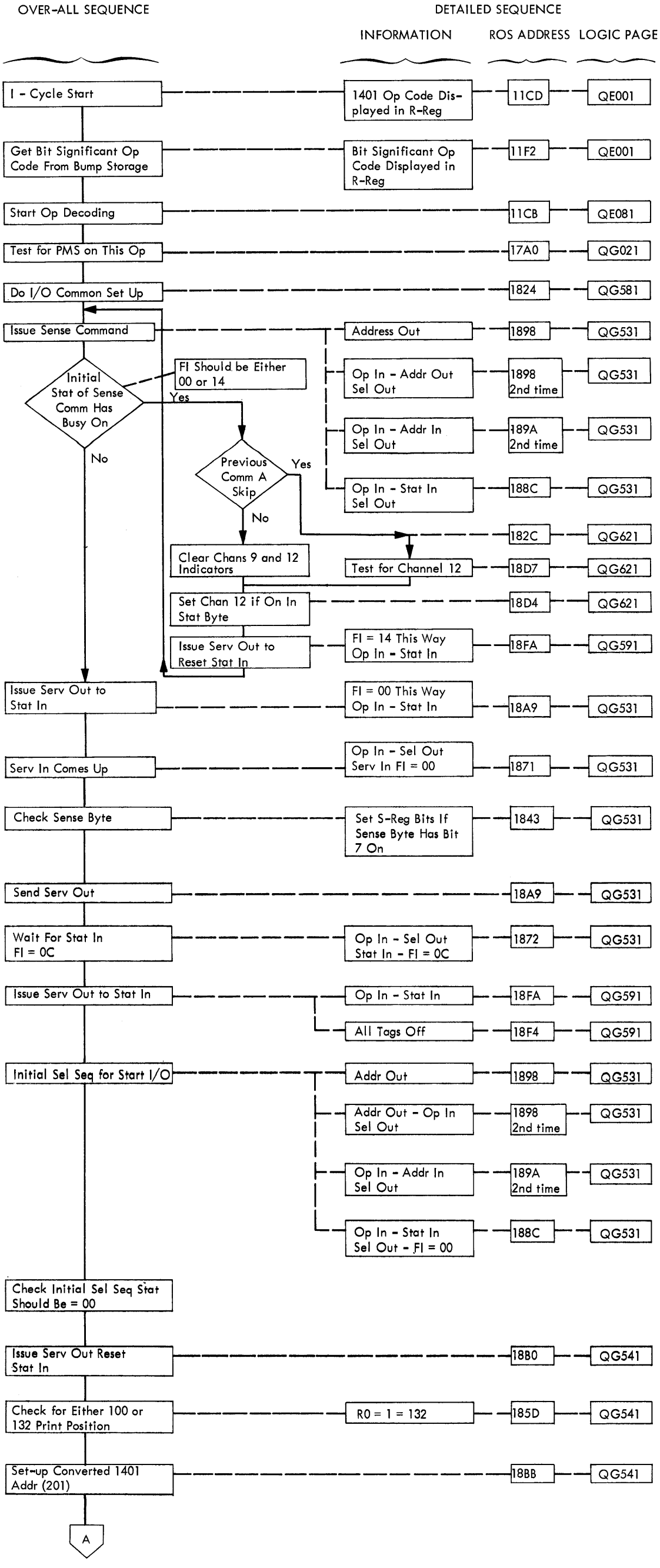


1401 Compatibility Read Operation RS Chart 9 (Sheet 1)


OVER-ALL SEQUENCE
DETAILED SEQUENCE
INFORMATION
ROS ADDRESS
LOGIC PAGE
A
Go Into Data Handling Loop,Retain WM if They Are There
18C0
QG561
Control Unit Ends Op by Presenting CE, DE
Op In - Stat In Sel Out FI = 0C
18C2
QG571
Op In - Stat In
1805
QG571
Card Feeds All Tags Off
1881
QG581
Check for Last Card
1805
QG571
Change Bit Significant Op Code in G Reg from21to 20
18DA
QG571
Check for Invalid Char
S'5 = 1 = Invalid Char Would Have Been Set During Prior Sense Comm
18DA
QG571
Check for a Unit Check
18DC
QG571
Issue Serv Out
If There Was an In-valid Char,181A Would Issue Serv Out
1818
QG571
Return to I Cycles
1100
QE001

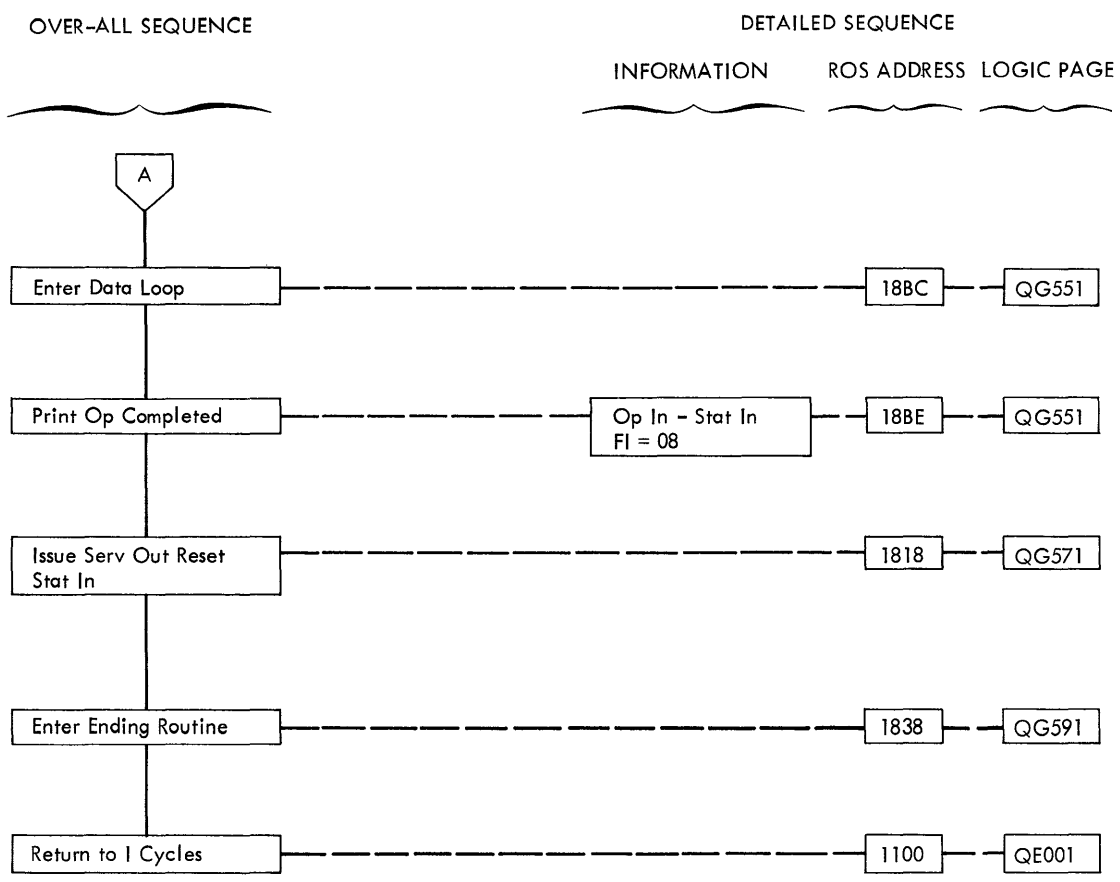
1401 COMPATIBILITY PRINT OPERATION

444 2
445 B 444
449 .



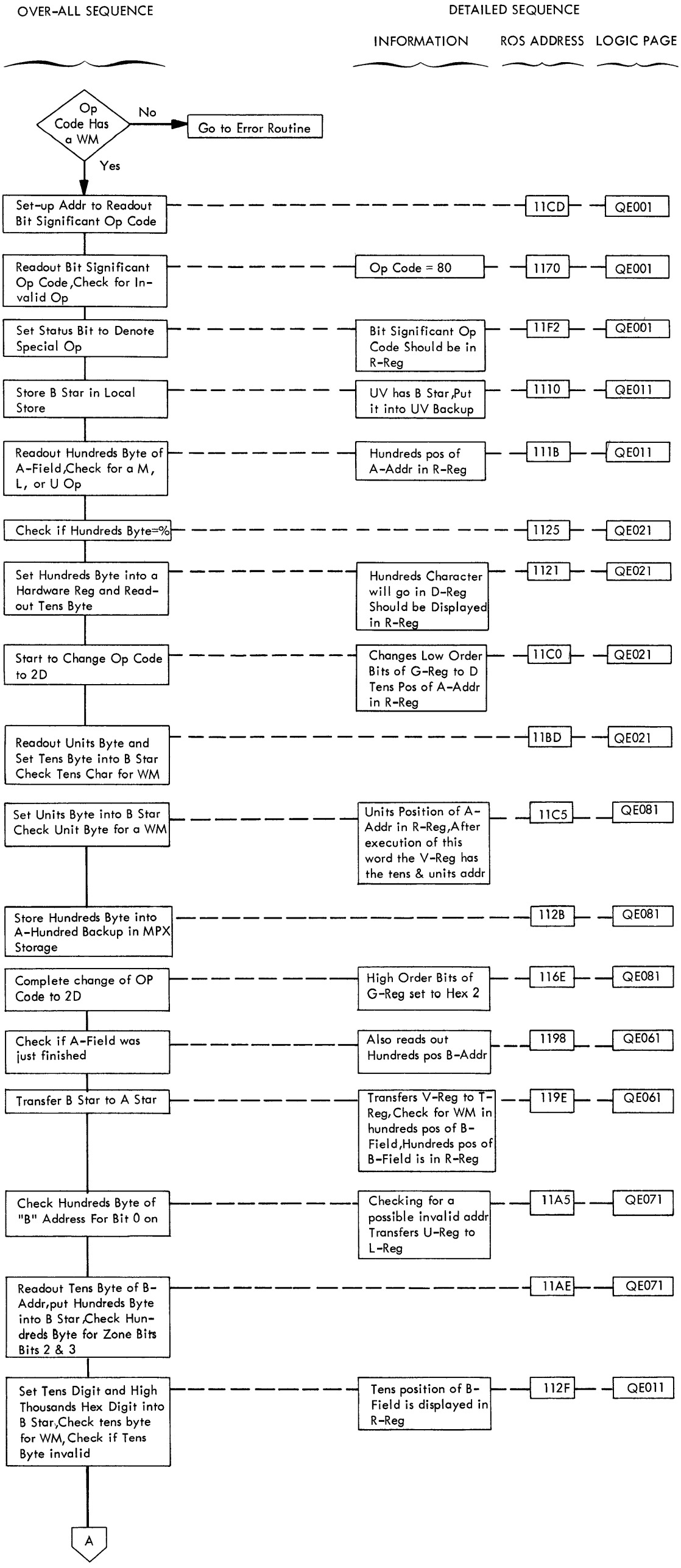
1401 Compatibility Print Operation RS Chart 10 (Sheet 1)

1401 COMPATIBILITY PRINT OPERATION

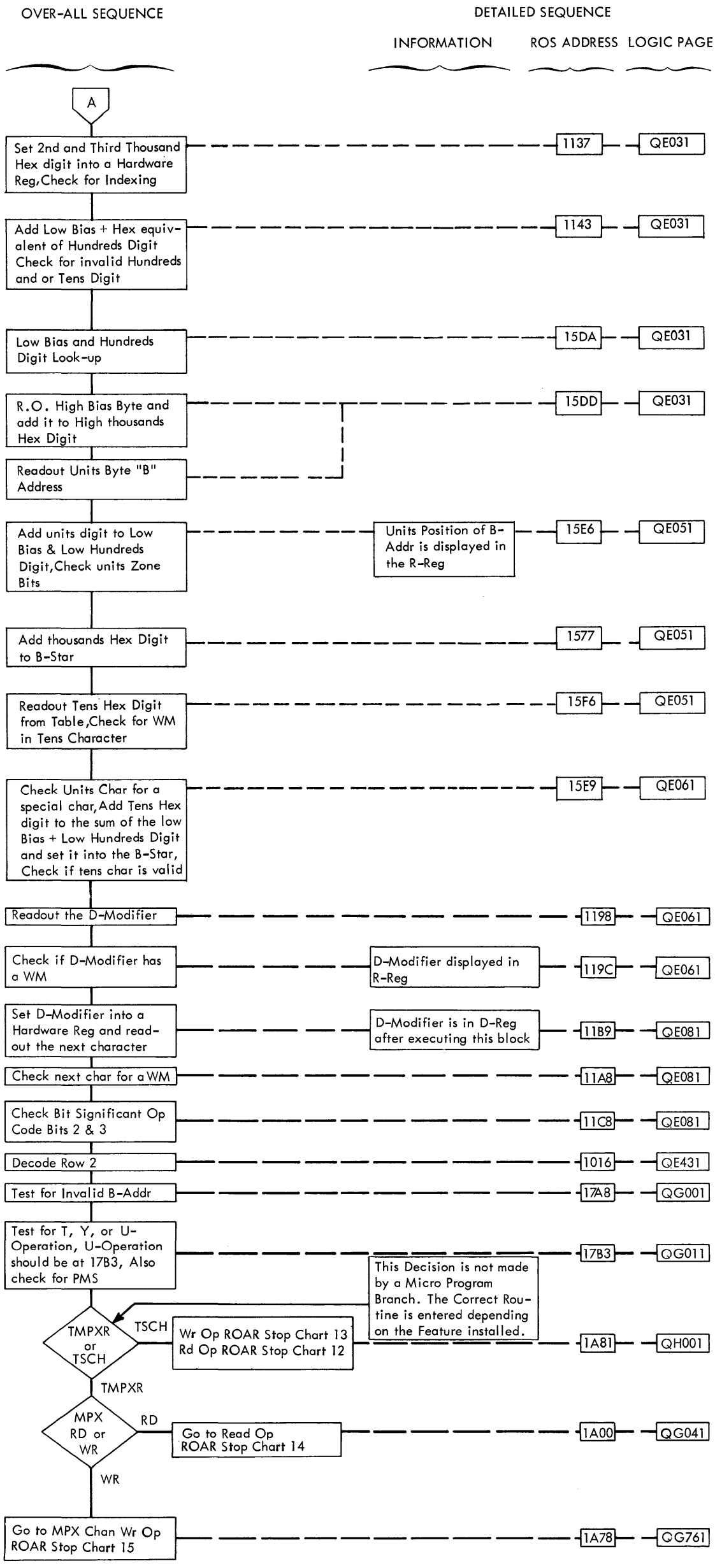


1400 TAPE OPERATION - TAPES ON MPX CHANNEL OR SELECTOR CHANNEL - I CYCLES

444 M %U 1 500W
452 B̄ 444
456 .̄



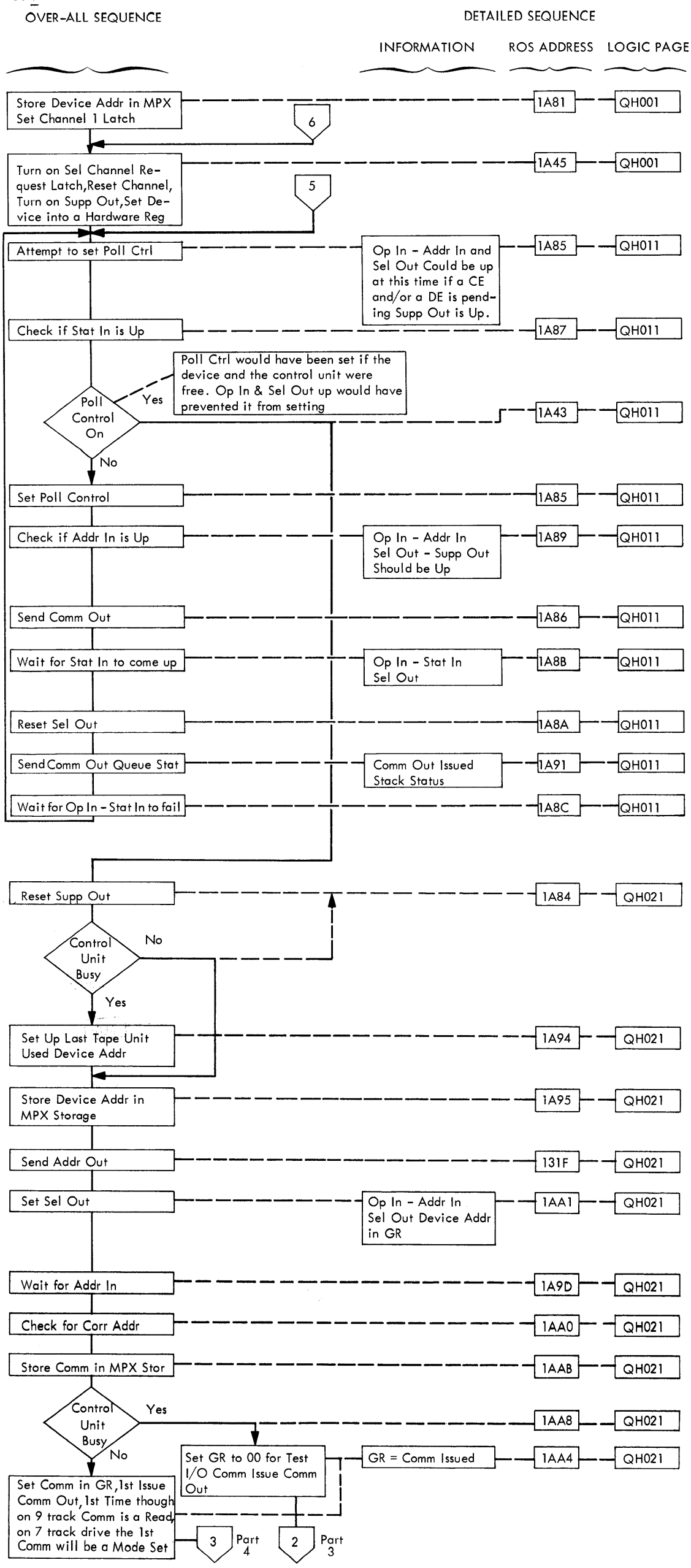
1400 Tape Operation-Tapes on MPX Channel or Selector Channel--I Cycles RS Chart 11 (Sheet 1)



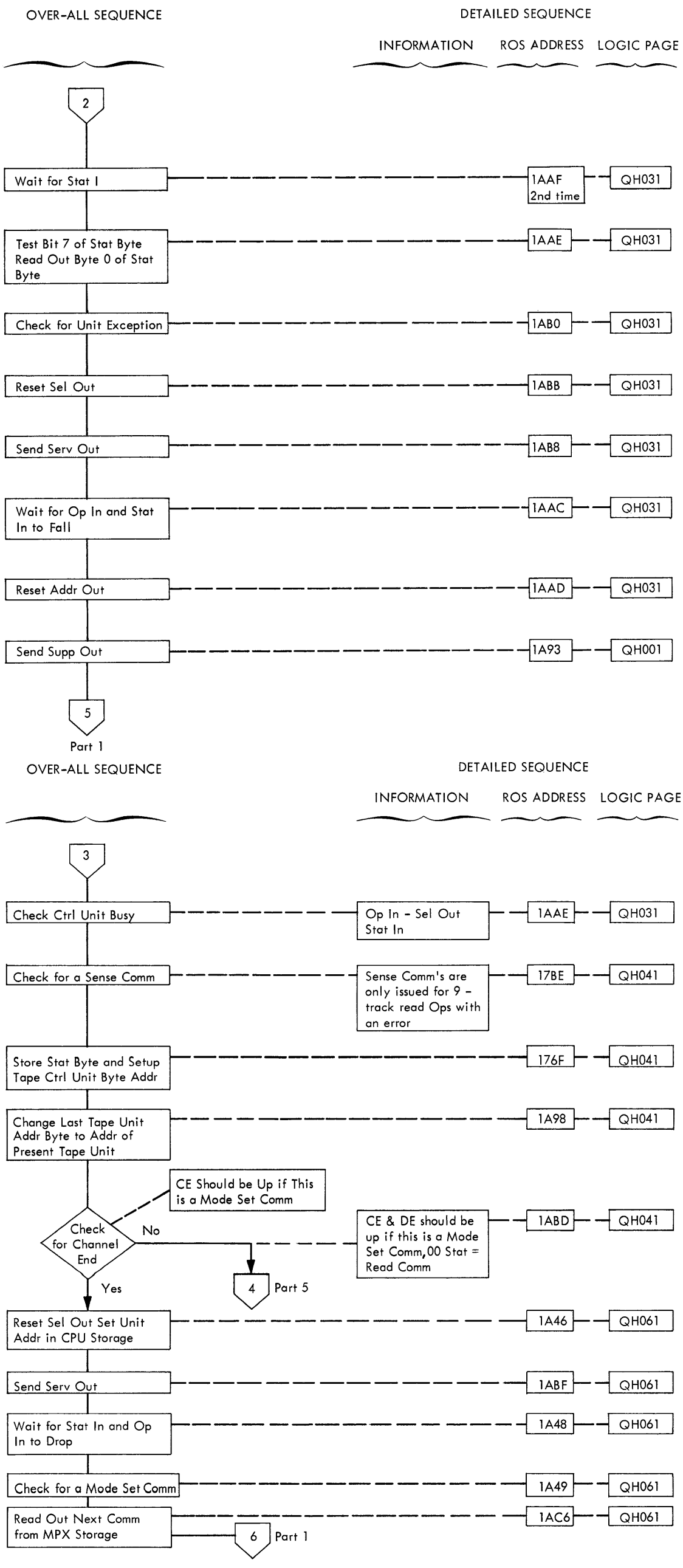
1400 Tape Operation-Tapes on MPX Channel or Selector Channel--I Cycles RS Chart 11 (Sheet 2)

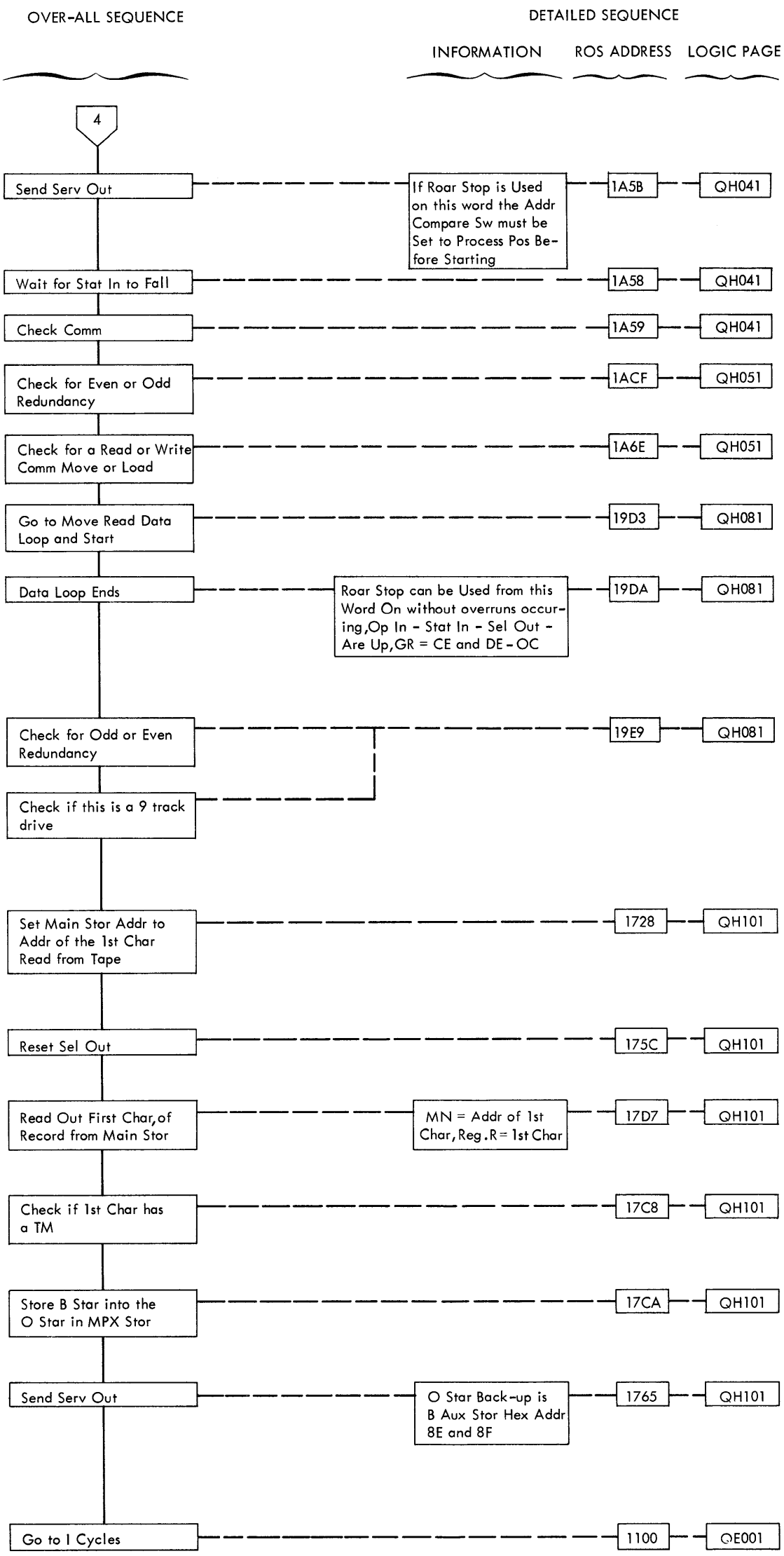
1400 COMPATIBILITY TAPE READ OPERATION - SELECTOR CHANNEL

444 M %U1 500R
452 B 444
456 -



1400 Compatibility Tape Read Operation--Selector Channel RS Chart 12 (Sheet 1)

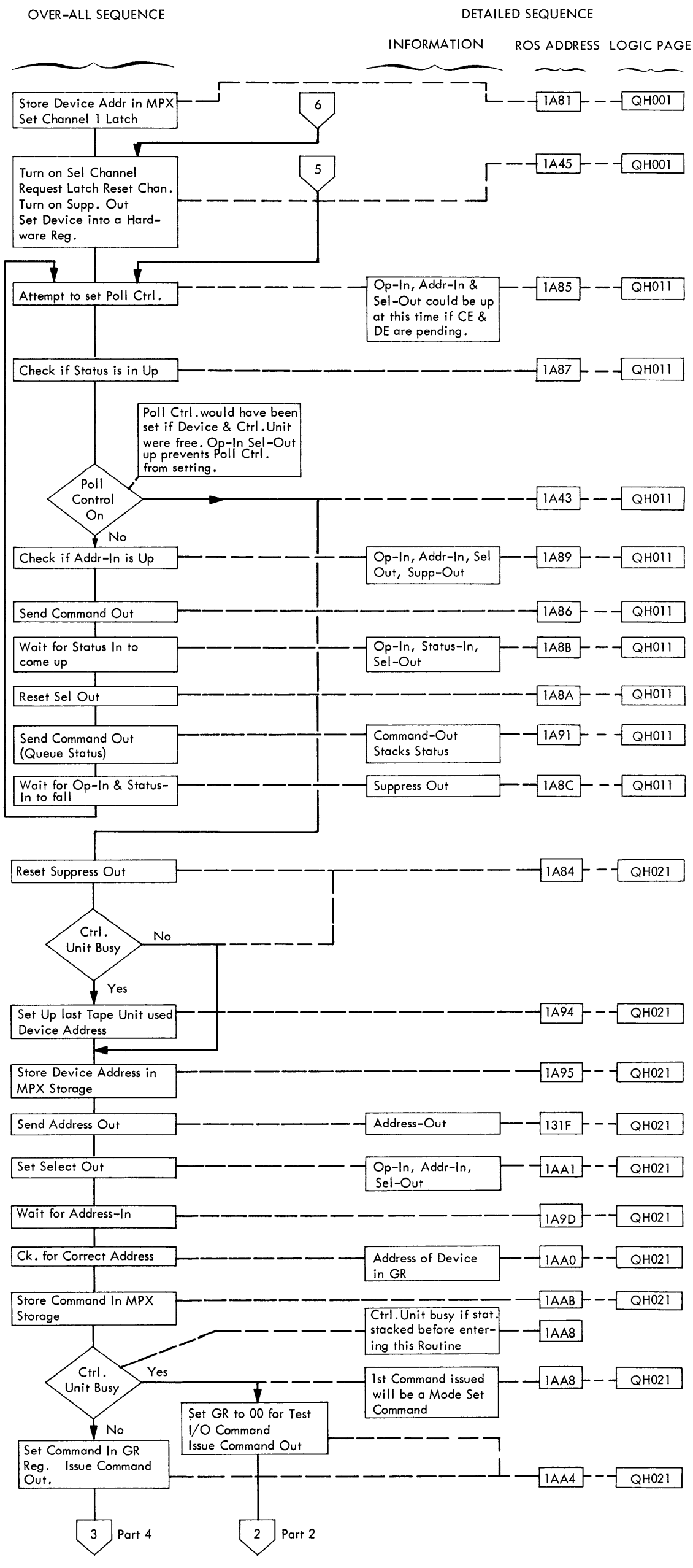

OVER-ALL SEQUENCE
DETAILED SEQUENCE
INFORMATION
ROS ADDRESS
LOGIC PAGE
2
Wait for Stat I
1AAF 2nd time
QH031
Test Bit 7 of Stat Byte Read Out Byte 0 of Stat Byte
1AAE
QH031
Check for Unit Exception
1AB0
QH031
Reset Sel Out
1ABB
QH031
Send Serv Out
1AB8
QH031
Wait for Op In and Stat In to Fall
1AAC
QH031
Reset Addr Out
1AAD
QH031
Send Supp Out
1A93
QH001
5
Part 1
OVER-ALL SEQUENCE
DETAILED SEQUENCE
INFORMATION
ROS ADDRESS
LOGIC PAGE
3
Check Ctrl Unit Busy
Op In - Sel Out Stat In
1AAE
QH031
Check for a Sense Comm
Sense Comm's are only issued for 9 - track read Ops with an error
17BE
QH041
Store Stat Byte and Setup Tape Ctrl Unit Byte Addr
176F
QH041
Change Last Tape Unit Addr Byte to Addr of Present Tape Unit
1A98
QH041
CE Should be Up if This is a Mode Set Comm
Check for Channel End
No
CE & DE should be up if this is a Mode Set Comm,00 Stat = Read Comm
1ABD
QH041
4
Part 5
Yes
Reset Sel Out Set Unit Addr in CPU Storage
1A46
QH061
Send Serv Out
1ABF
QH061
Wait for Stat In and Op In to Drop
1A48
QH061
Check for a Mode Set Comm
1A49
QH061
Read Out Next Comm from MPX Storage
1AC6
QH061
6
Part 1

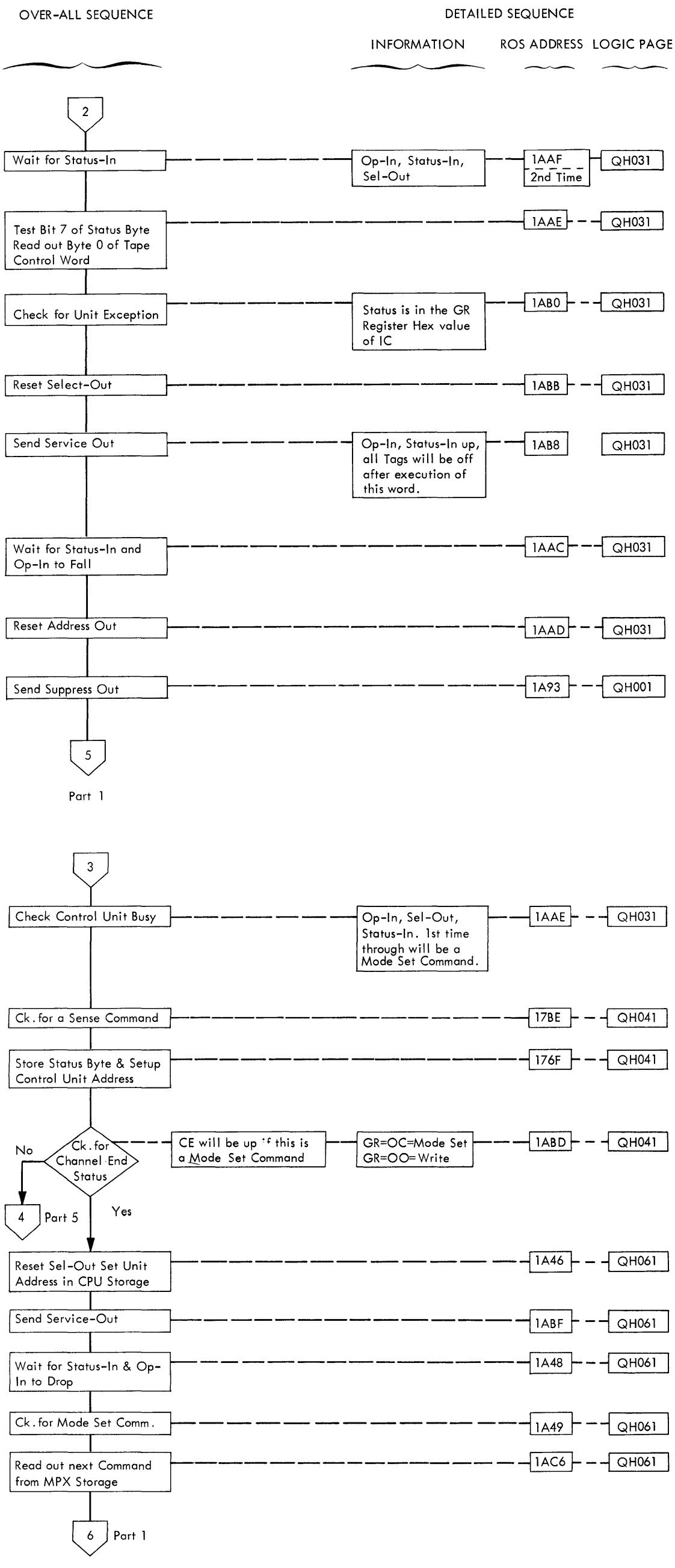


1400 Compatibility Tape Read Operation - Selector Channel RS 12 (Sheet 3)

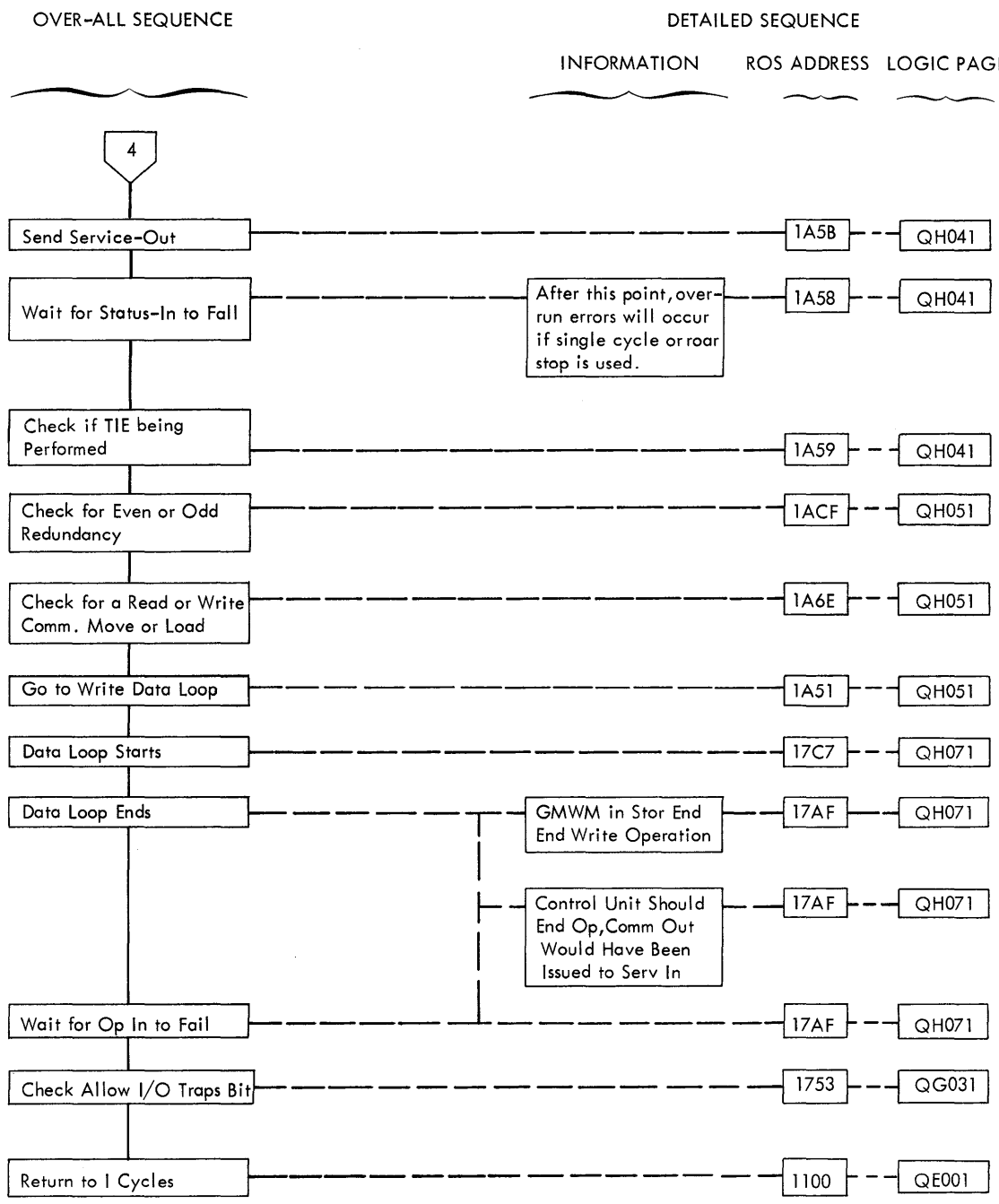
1400 COMPATIBILITY - TAPE SELECTOR SETUP - TAPE WRITE OP 9 TRACK DRIVE

444 M % U 1 500 W
452 B 444
456 .



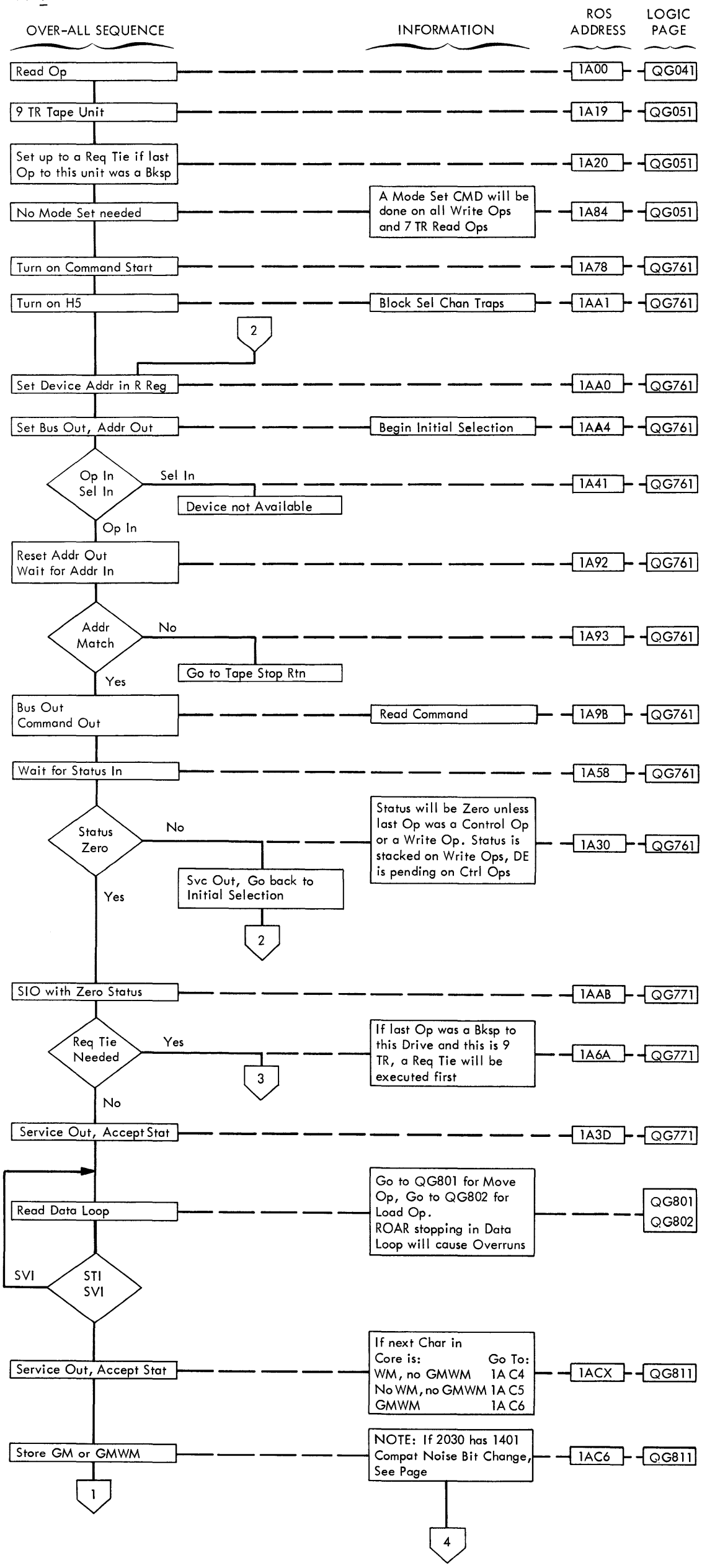


1400 Compatibility Tape Selector Setup-Tape Write Op 9 Track Drive RS Chart 13 (Sheet 2)


OVER-ALL SEQUENCE
DETAILED SEQUENCE
INFORMATION
ROS ADDRESS
LOGIC PAGE
4
Send Service-Out
1A5B
QH041
Wait for Status-In to Fall
After this point, over-run errors will occur if single cycle or roar stop is used.
1A58
QH041
Check if TIE being Performed
1A59
QH041
Check for Even or Odd Redundancy
1ACF
QH051
Check for a Read or Write Comm. Move or Load
1A6E
QH051
Go to Write Data Loop
1A51
QH051
Data Loop Starts
17C7
QH071
Data Loop Ends
GMWM in Stor End End Write Operation
17AF
QH071
Control Unit Should End Op, Comm Out Would Have Been Issued to Serv In
17AF
QH071
Wait for Op In to Fail
17AF
QH071
Check Allow I/O Traps Bit
1753
QG031
Return to I Cycles
1100
QE001

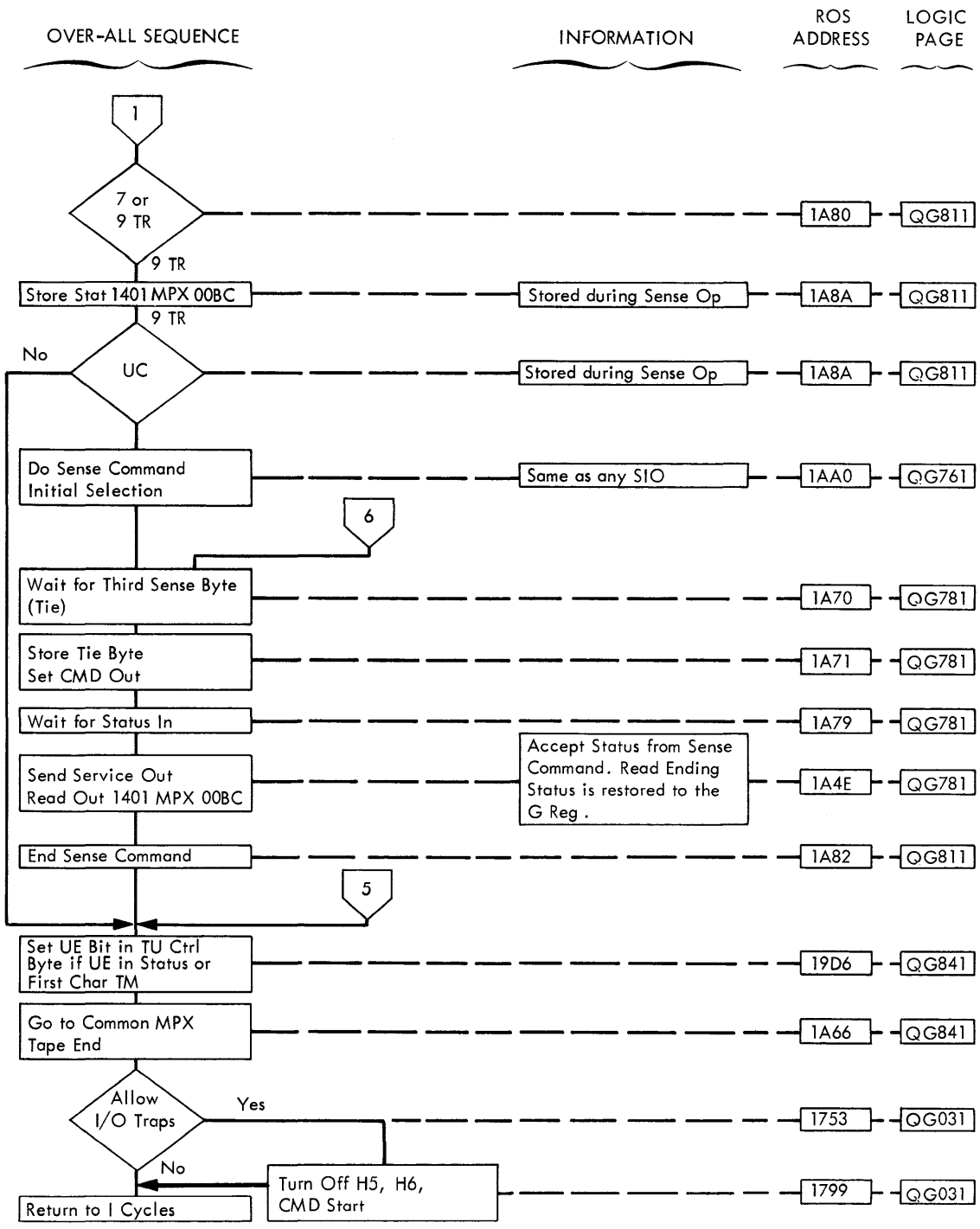
1400 COMPATIBILITY TAPE READ OPERATION TMPXR

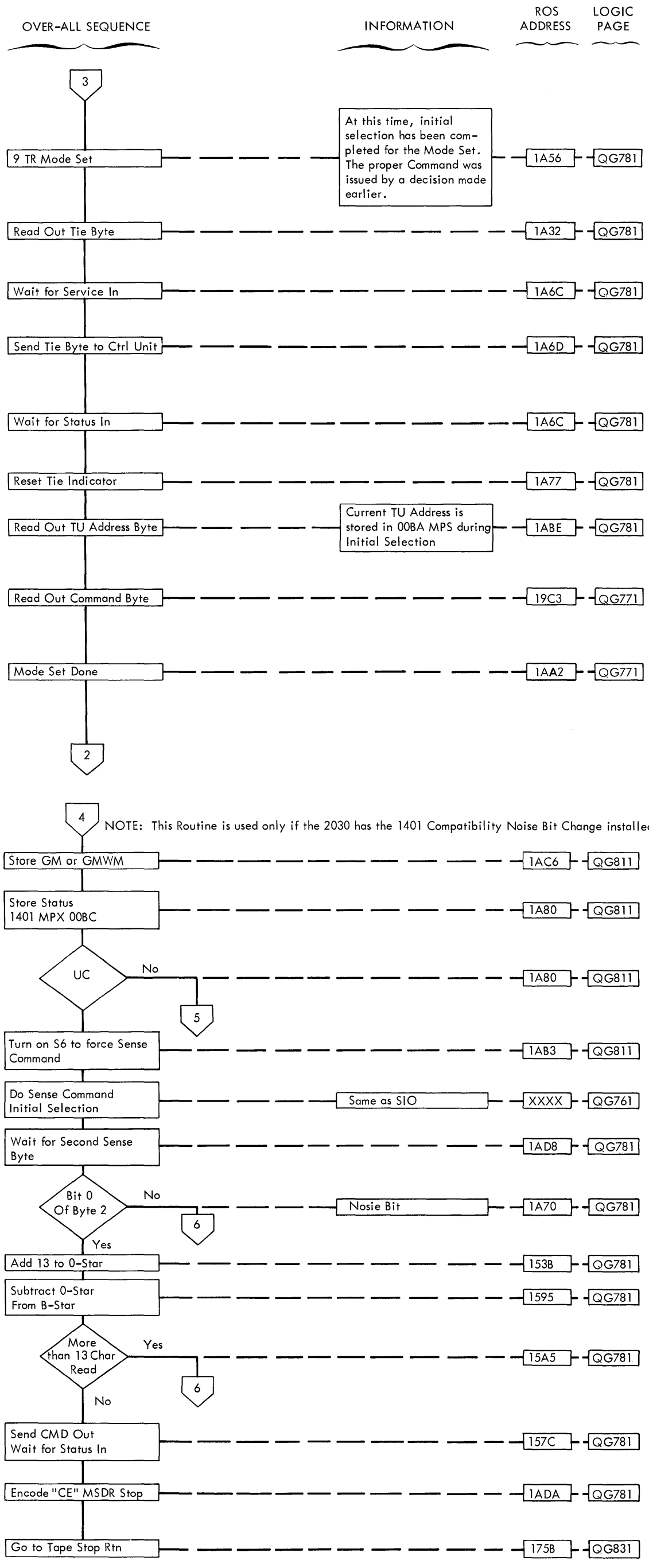
```
444  M % U I 500R
452  B  417 L
457  B̄  400
461  Ū  % U I B
466  B̄  400
470  .
```



1400 Compatibility Tape Read Operation TMPXR RS Chart 14 (Sheet 1)

1400 COMPATIBILITY TAPE READ OPERATION TMPXR

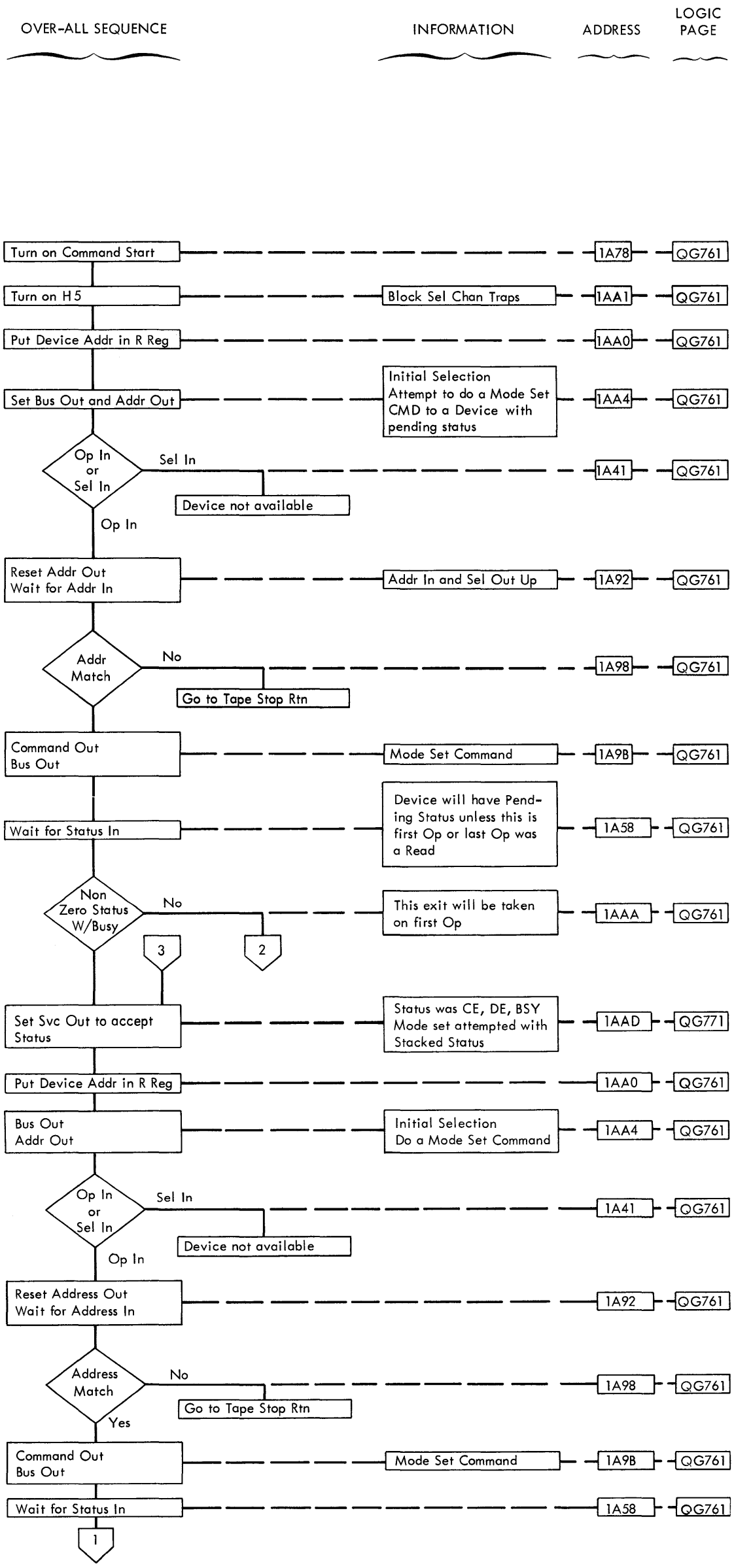




1400 Compatibility Tape Read Operation TMPXR RS Chart 14 (Sheet 3)

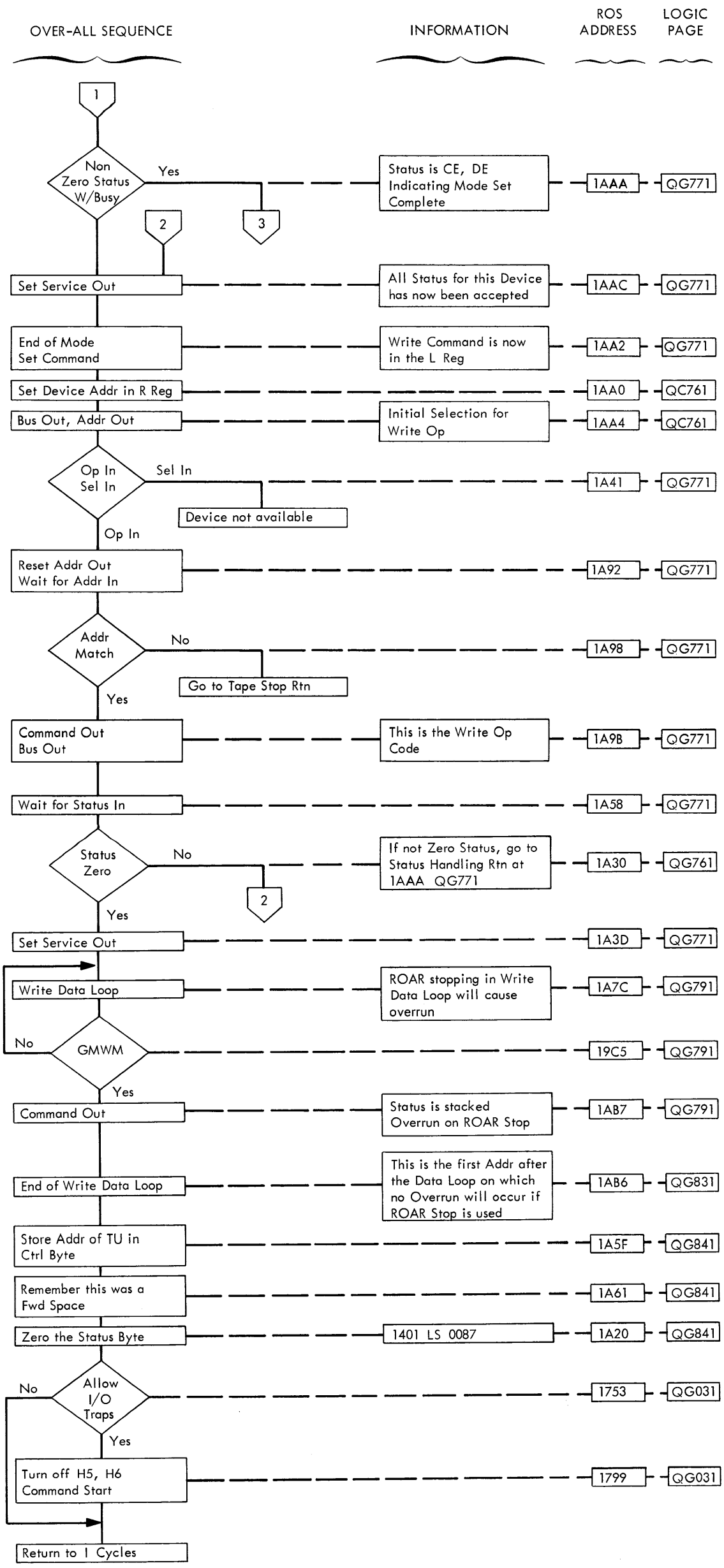
1400 COMPATIBILITY - TAPES ON MPX SET UP - TAPE WRITE OP 9 TRACK DRIVE

444 M % U 1 500W
452 B 400
456 .



1400 Compatibility-Tapes on MPX Set Up--Tape Write Op 9 Track Drive RS Chart 15 (Sheet 1)

1400 COMPATIBILITY TAPES ON MPX SET UP - TAPE WRITE OP 9 TRACK DRIVE



I 1400 FILE COMPATIBILITY

A. To allow proper operation of the included programs and stop words, the following initial preparation is necessary.

   1. Initialize Disc Pack in 360 Mode writing Home addresses and record zero on all tracks using UT069.

      Surface analysis should also be done to flag defective tracks.

   2. Load Auxiliary Storage using either CID or 3F00.

   3. Write 1400 addresses with Clear Disc Program.

      Item 3 can be bypassed if 1400 Write Address Operation is to be performed first with Compare Disable Bit on. This will write addresses on a given track and allow other tests to be run on that track.

B. When restarting any of the example programs, a second error may occur if the following is not performed.

   1. Do 1400 Start Reset

   2. Start program at an instruction that will restore the DCF.

C. A Validity Check during Read or Write will break chaining. This will force a Sector Count 000 Indicator (Bit .7 of Operation Register). The number of sectors not processed will be indicated in the 1400 DCF.

D. Sector Read and Write with addresses will post a No Address Compare (X) if the last Record Address is not 16 or greater. This test is made to check for missing 2311 address marks. (QH531, Word 1D1D).

   This may cause confusion if a Validity Check breaks chaining before 16 records are processed. Result is that X and V are posted when V is the actual cause.

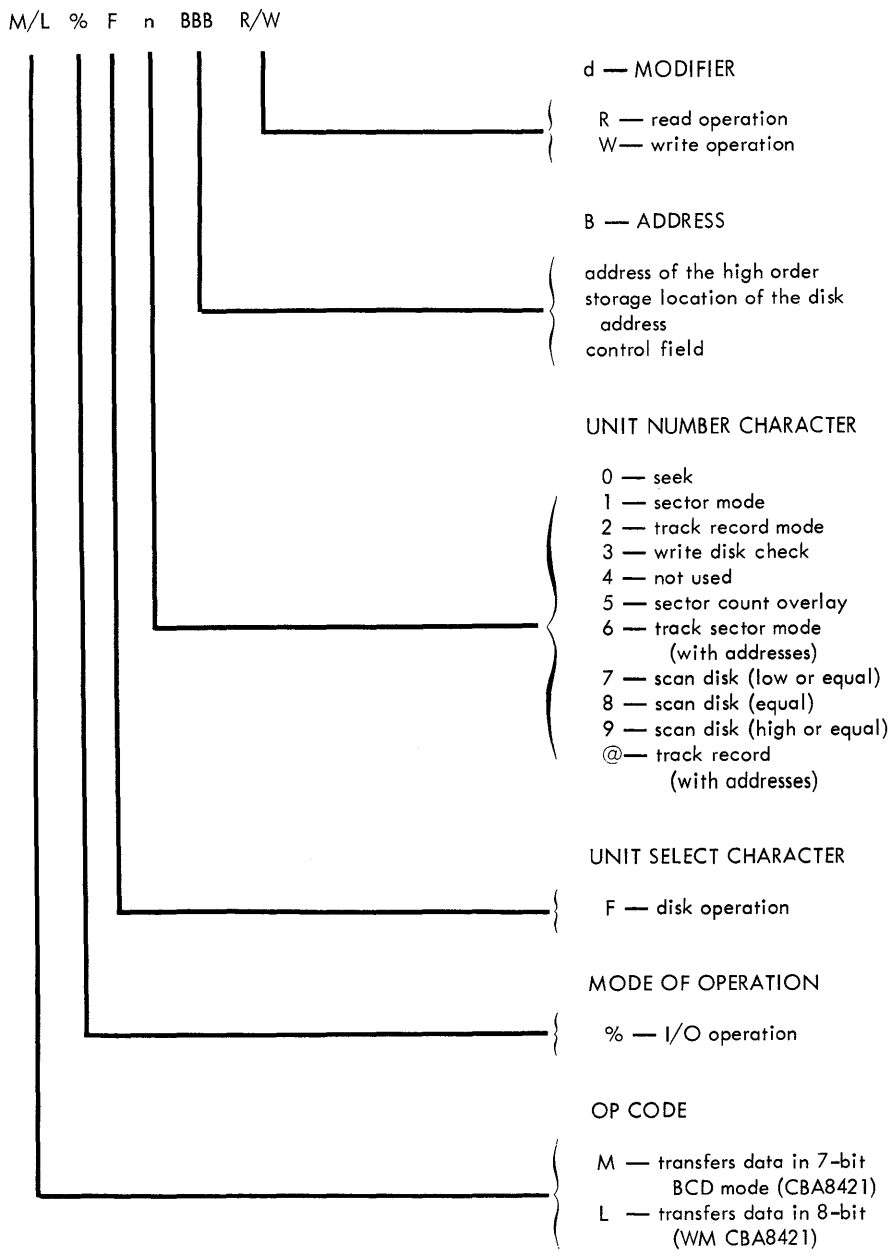
E. If an Alternate Track is assigned, the 2311 Carriage will be restored at the end of each completed 1400 Operation or 20 Sectors. This means that a RBC following a Write Operation will have to seek to the Alternate Track and return as did the Write Operation. Also, if a number of tracks are to be processed (sector count greater than 020) and more than one is flagged, the 2311 Carriage will be restored after each Alternate Track Read or Write is completed. Therefore, an Alternate Track Seek can occur more than once during a single 1400 Operation.

F. Auxiliary Storage B - 90,92,94,96 and 98 (File Unit Addresses) must be in sequence when doing Address Operations or Alternate Track Operations or a No Address Compare will occur. The data in these addresses is always stored in K29 MPX on Initial Selection. When the above two operations are performed, a table look-up is done using the value in K29 MPX to determine the Auxiliary Storage Address that the actual cylinder value is stored in 91,93,95,97 or 99. An Out of Sequence Unit Address will result in looking up cylinder value for the wrong file. This procedure is necessary because some program applications use other than normal addresses on certain cylinders, such as labels. If addresses are abnormal, it becomes impossible to read 360 Record 0 or return to the proper track.

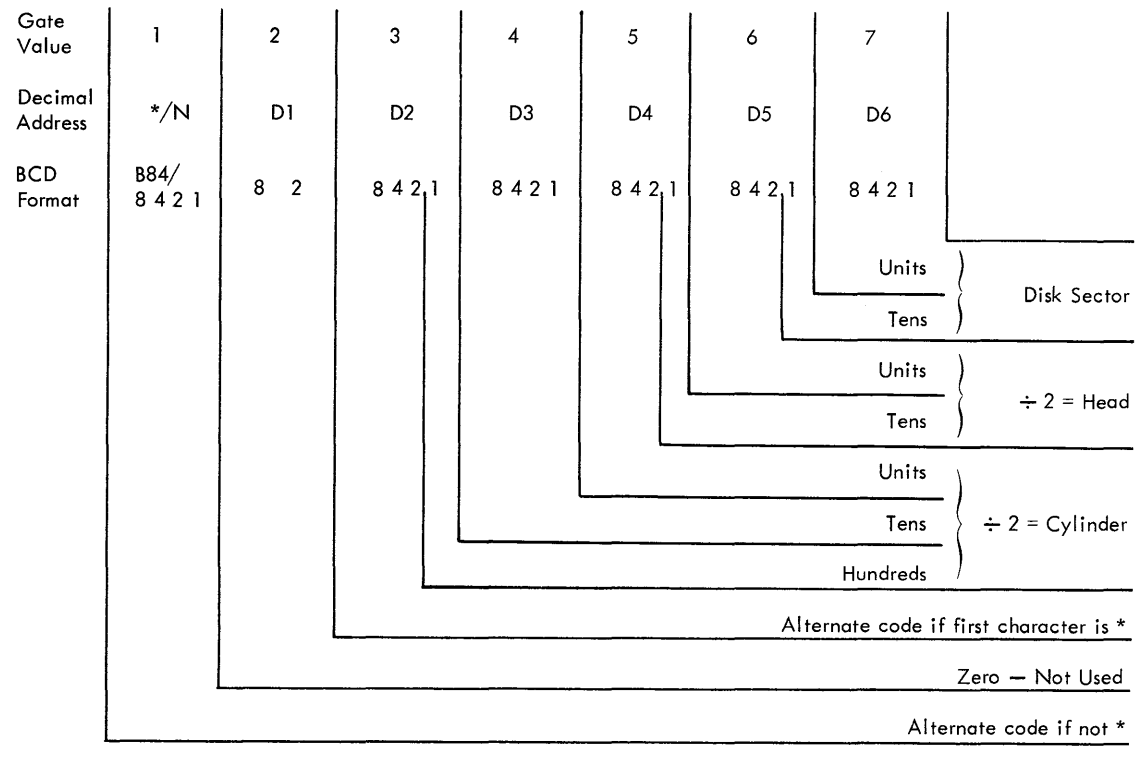
G. Module Protect Check is defined on Head Seek flow chart.

H. STOP CHECK is indicated on several flow charts. This is the first stop point since 1BB0 of the search command that will allow continuation of the operation without an overrun. Check FI = CE·DE, Op In and Stat In up, command code in Aux B - BE, updated CCHHR stored in Aux B - AD thru B1.

1311 DISK INSTRUCTION FORMAT



1311 ADDRESS CONTROL FIELD



PERMANENT FILE AUXILIARY STORAGE LOCATIONS

AUXILIARY STORAGE B

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	TLU for Head and Cylinder 10's Decode															
	00	05	01	06	02	07	03	08	04	09						
1	Note 1	File Mod 00	File Mod 02	File Mod 04	File Mod 06	File Mod 08										
8	0	Sense 1	Bytes 2	3												
9	File Unit 0 Addr 00	Cyl Loc	File Unit 1 Addr 01	Cyl Loc	File Unit 2 Addr 02	Cyl Loc	File Unit 3 Addr 03	3 Cyl Loc	File Unit 4 Addr 04	Cyl Loc	Note 2					
A	TLU for Cylinder 100's Decode Numeric										Previous File Op			Always 00		
	00	50	10	60	20	70	30	80	40	90				Cyl 00	Cyl	Head 00
	Hex															
	00	32	0A	3C	14	46	1E	50	28	5A						
B	Head	Record	K	D	D				Note 5	1400 File Mod No.				File Unit Addr Init Sel	Last File Command	Scan Cond Note 3

AUXILIARY STORAGE A

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
9										Scan Result Note 3		Note 4				
A	Alternate Track Addr Read From R0 of Flagged Track															
	Cyl	Cyl	Head	Head												

NOTE 1
BIT 0 - COMP DISABLE
1 - MOD PROTECT

NOTE 2
BIT 3 = 1 = DCF HAS INCREMENTED

NOTE 3

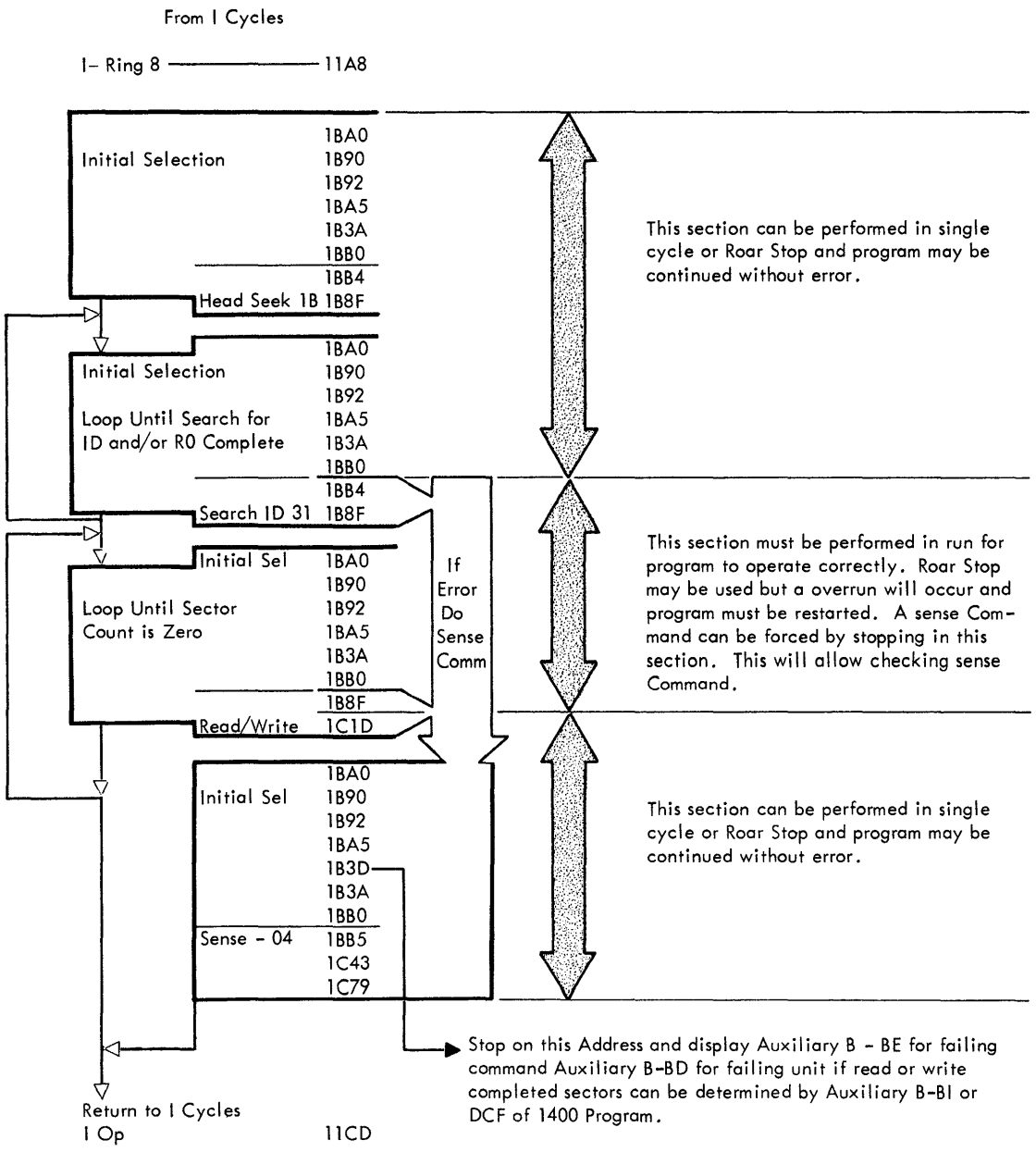
	K3I UCW SCAN OP	WT		K9H CPU SCAN RESULT	WT
SCAN LO	7	0	HI		12
		0	LO		6
		0	EQ		1
SCAN EQ	8	1	HI		12
		1	LO		6
		1	EQ		1
SCAN HI	9	2	HI		12
		2	LO		6
		2	EQ		1

NOTE 4
1400 BR BYTE
0 - NO ADDR COMP
1 - BUSY
2 - WLR
3 - ANY
4 - PARITY
5 - NOT RDY
6 - RBC
7 - ON-Checked for Recalibrate Seek Necessary

NOTE 5
On alternate track operation, original cylinder value in AE(K22) is stored here for return seek

FILE READ/WRITE GENERAL ADDRESS FLOW

Details on the following address are on the individual charts for each operation.



II SECTOR OPERATIONS IN COMPATIBILITY MODE

Note the following characteristics of Sector OPs in compatibility mode:

1. Sector address is incremented in 360 CCHHR not 1400 DCF.
2. Updated CCHHR is not converted and stored in DCF until sector count 000 is detected.
3. Sector count is decremented in 1400 DCF.
4. In event of error sector count could appear decreased and sector address may not be increased in the DCF. CCHHR in aux. B - AD thru B1 should be checked for actual sector address value.
5. DCF incremented bit - aux. B-9 A-Bit 3
   Bit 3 = 1 indicates CCHHR has been incremented (sector count more than one) therefore CCHHR must be converted 1400 format and zone bits stripped.
6. Zone bits will remain in DCF only if initial sector count is 001.

III SECTOR OPERATIONS - READ/WRITE/RBC

The following programs should be used when possible as they are tested and provide predictable results:

Read Op

500 M % F 0 800 R	Seek
508 M % F 1 800 R	Read
516 M 709 809	Restore DCF
523 B 532 Y	Branch on any condition
528 B 508	Loop
532 . 500	
536 .	

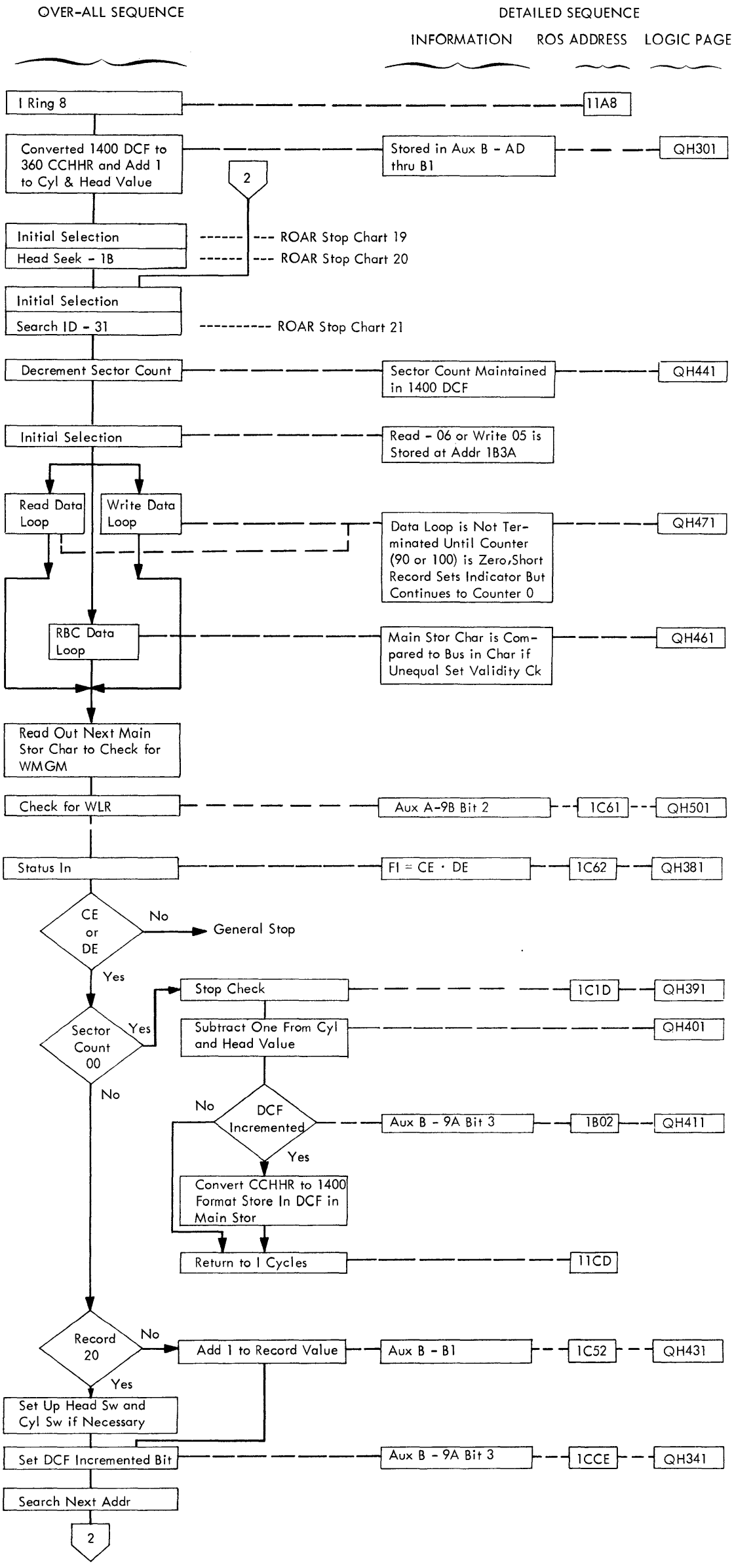
Write Op

500 M % F 0 800 R	Seek
508 M % F 1 800 W	Write
516 M 709 809	Restore DCF
523 M % F 3 800 R	RBC
531 M 709 809	Restore DCF
538 B 557 Y	Branch on any condition
543 B 508	Loop
547 . 500	
551 .	

700 - * 010000 001
800 - * 010000 001
910 - ‡

Can be increased from 1 thru 20 depending on the number of sector operations desired.

Add 100 addresses for each sector over one (1) to be processed.


OVER-ALL SEQUENCE
DETAILED SEQUENCE
INFORMATION
ROS ADDRESS
LOGIC PAGE
I Ring 8
11A8
Converted 1400 DCF to 360 CCHHR and Add 1 to Cyl & Head Value
Stored in Aux B - AD thru B1
QH301
2
Initial Selection
ROAR Stop Chart 19
Head Seek - 1B
ROAR Stop Chart 20
Initial Selection
Search ID - 31
ROAR Stop Chart 21
Decrement Sector Count
Sector Count Maintained in 1400 DCF
QH441
Initial Selection
Read - 06 or Write 05 is Stored at Addr 1B3A
Read Data Loop
Write Data Loop
Data Loop is Not Terminated Until Counter (90 or 100) is Zero, Short Record Sets Indicator But Continues to Counter 0
QH471
RBC Data Loop
Main Stor Char is Compared to Bus in Char if Unequal Set Validity Ck
QH461
Read Out Next Main Stor Char to Check for WMGM
Check for WLR
Aux A-9B Bit 2
1C61
QH501
Status In
FI = CE · DE
1C62
QH381
CE or DE
No
General Stop
Yes
Stop Check
1C1D
QH391
Sector Count 00
Yes
Subtract One From Cyl and Head Value
QH401
No
No
DCF Incremented
Aux B - 9A Bit 3
1B02
QH411
Yes
Convert CCHHR to 1400 Format Store In DCF in Main Stor
Return to I Cycles
11CD
Record 20
No
Add 1 to Record Value
Aux B - B1
1C52
QH431
Yes
Set Up Head Sw and Cyl Sw if Necessary
Set DCF Incremented Bit
Aux B - 9A Bit 3
1CCE
QH341
Search Next Addr
2

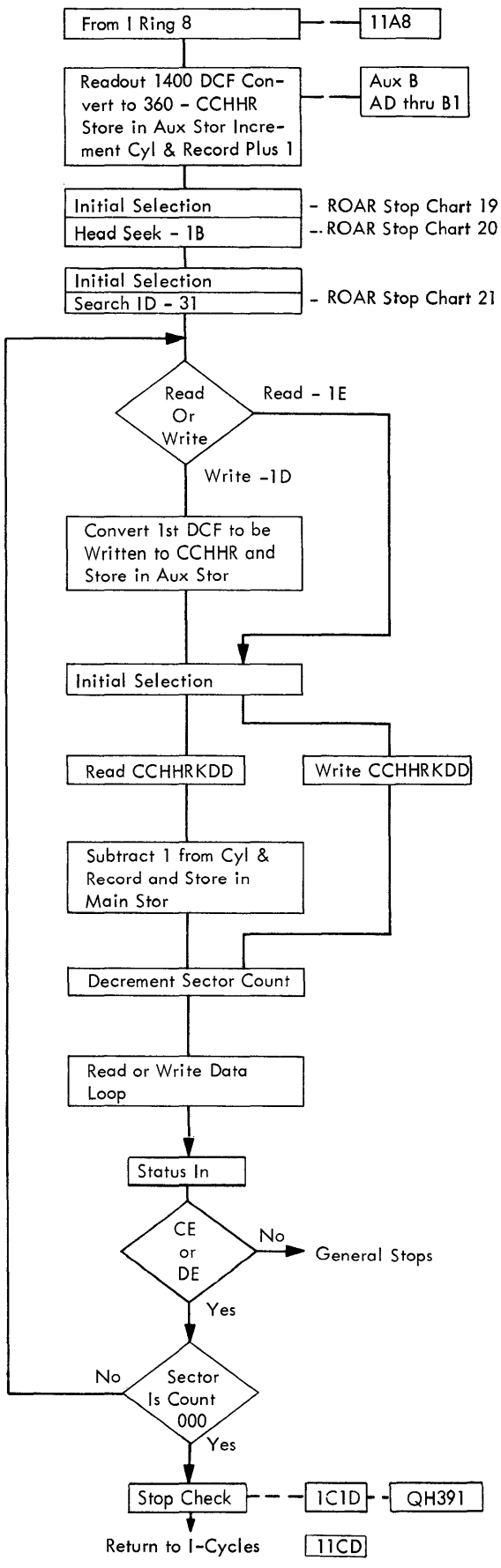
PROGRAM EXAMPLE FOR SECTOR WRITE WITH ADDRESSES (Write 20 Sectors with Addresses)

```
500 M % F 0 800 R        Seek to Cyl 050 (1400)
508 M % F 6 800 W        Write
516 M 709 809            Restore DCF
523 M % F 3 800 R        RBC
531 M 709 809            Restore DCF
538 B 547 Y              Branch on any Condition
543 B 508                Loop
547 - 500                Stop/Seek Restore after
                          Error

551 -
700 * 01 0000 020
800 * 01 0000 020 01 0000
2824 0 10 019
2930 ±
```

PROGRAM EXAMPLE FOR SECTOR READ WITH ADDRESSES

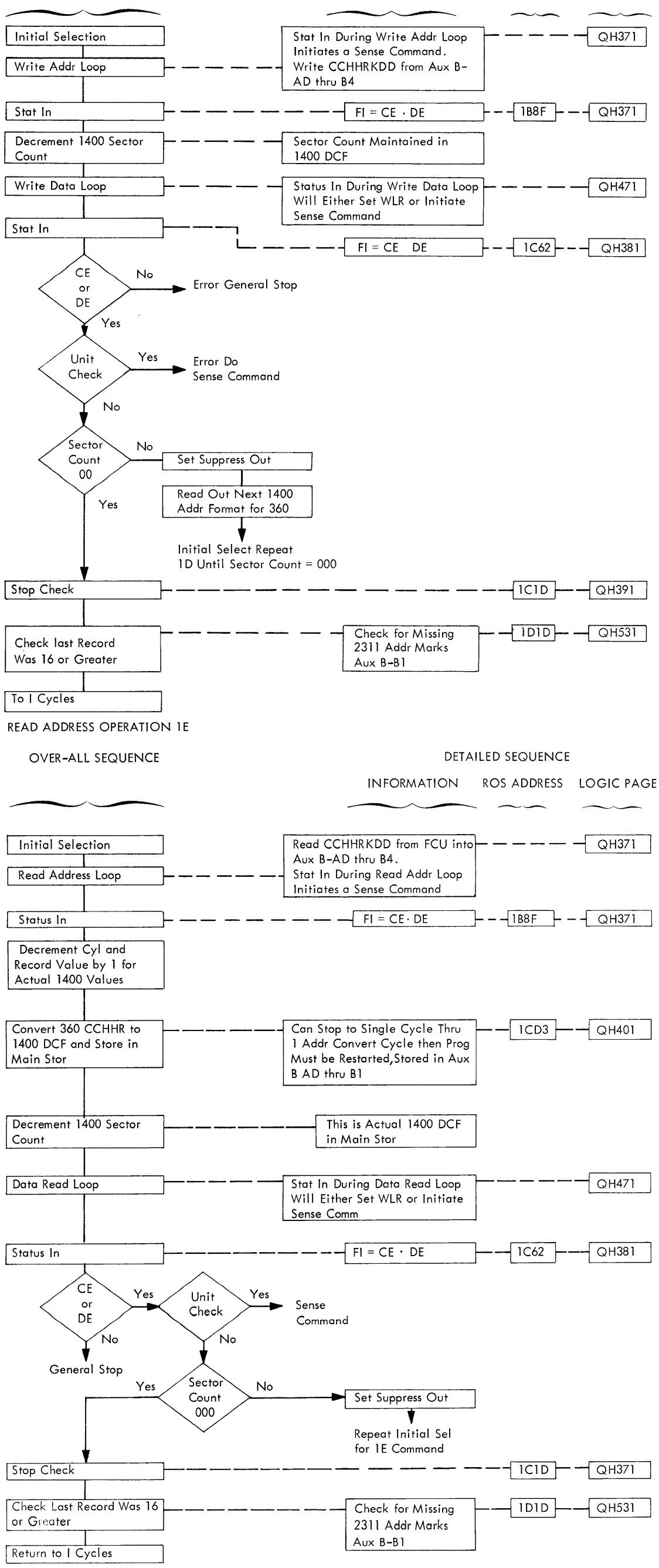
```
500 M % F 0 800 R        Seek
508 M % F 6 800 R        Read
516 M 709 809            Restore DCF
523 B 532 Y              Branch on any Condition
528 B 508                Loop
532 - 500                Stop/Seek Restore after
                          Error

536 -
700 * 01 0000 020
800 * 01 0000 020
2930 ±
```

SECTOR READ WRITE WITH ADDRESSES - OBJECTIVES



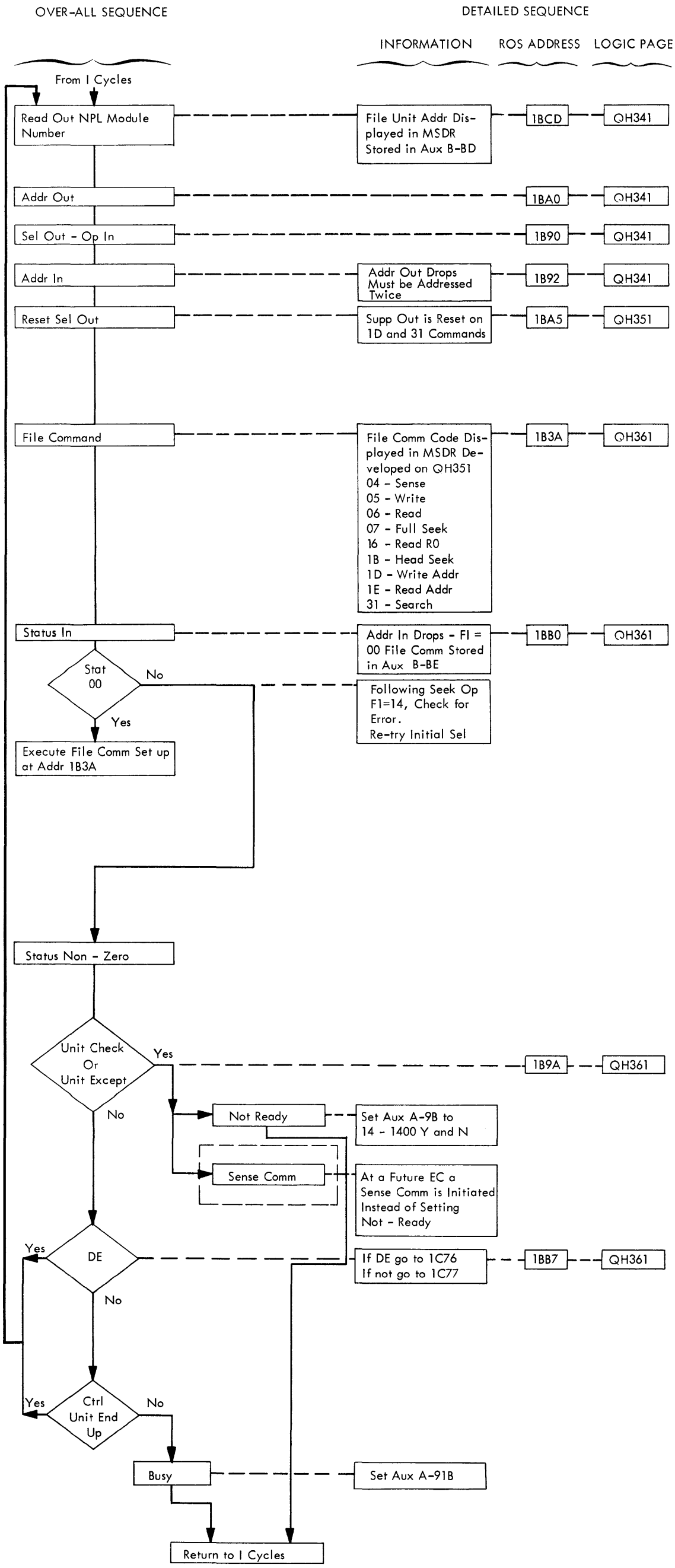
WRITE ADDRESS OPERATION 1D

Initial File Address to be Written Has Been Developed with the Cylinder and Record Count Incremented Plus 1 to Conform to 360 Format and Stored as CCHHRKDD in Aux B AD thru B4.



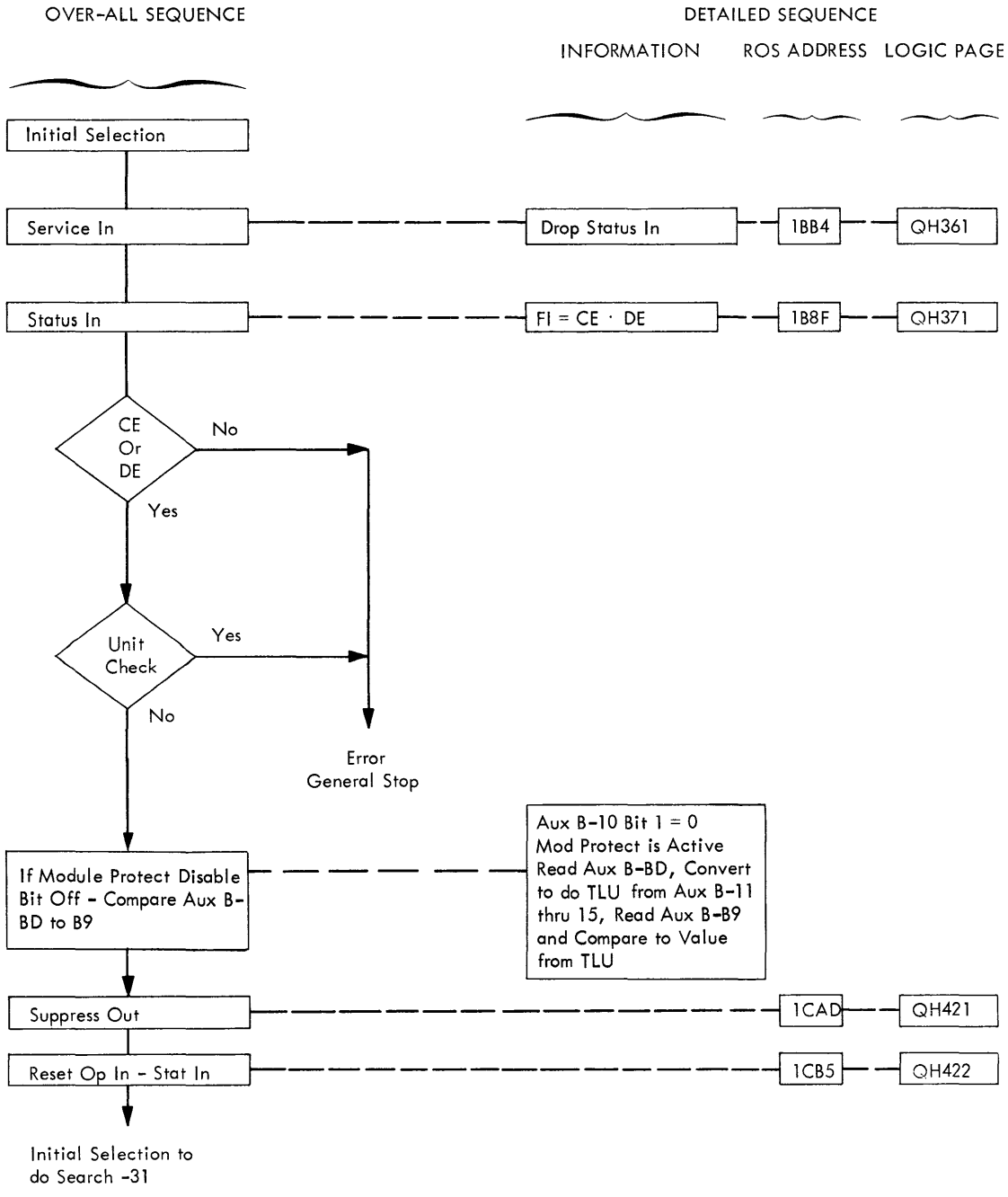
READ ADDRESS OPERATION 1E

INITIAL SELECTION FILE COMMANDS

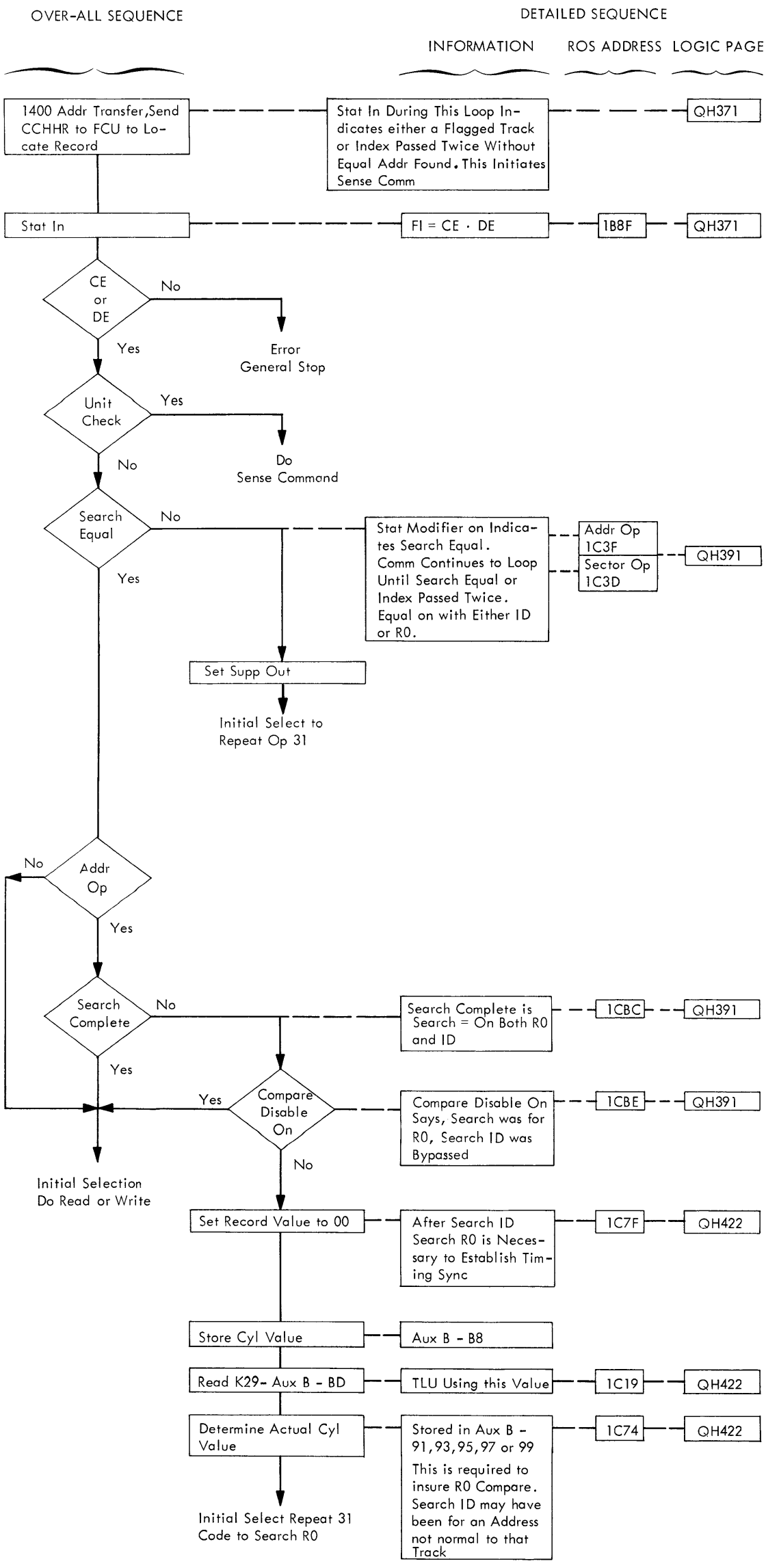


Initial Selection File Commands RS Chart 19 (Sheet 1)

HEAD SEEK 1B

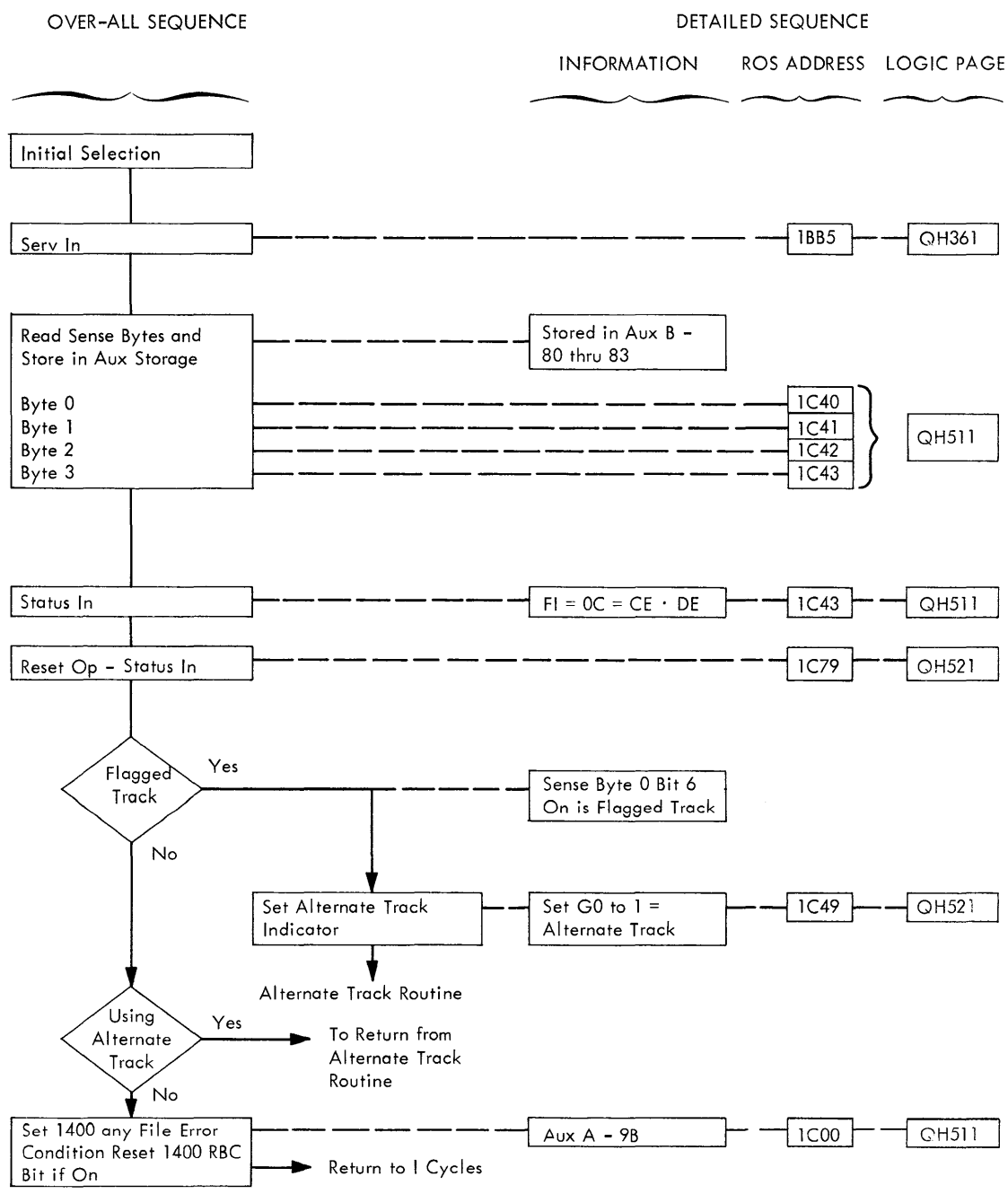


Head Seek 1B RS Chart 20 (Sheet 1)



Search ID--31 Command RS Chart 21 (Sheet 1)

SENSE COMMAND - 04



IV SEEK OPERATION

A. Initialize Auxiliary Storage

B. Enter following program

C Ready the 1st File

D. 1400 Start Reset

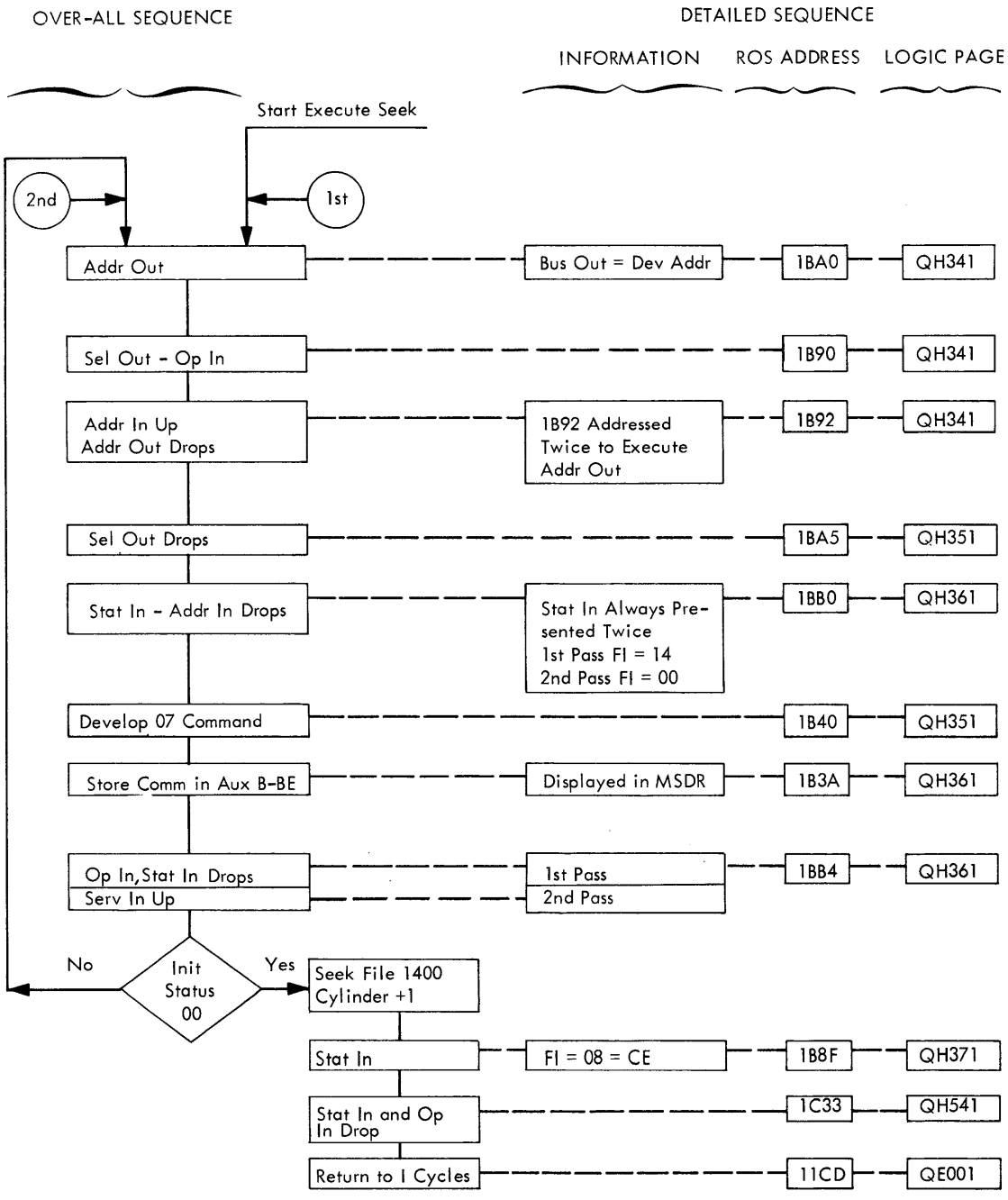
E. Start Program (Set 1C to 500)

F. Execute program in single cycle or Roar Stop on address provided in flow chart for Seek Operation.

This program should do repetitive seeks between 1400 cylinders 000 and 050. The actual physical location on the Disc Pack are cylinders 001 and 051. The compatibility feature increments all 1400 cylinders plus one because cylinder 000 is reserved for 360 use.

```
500  M ' F 0 600 R    Seek to Cylinder 00
508  B 5 0 0 \        Branch on Busy
513  M ' F 0 700 R    Seek to Cylinder 50
521  B 5 1 3 \        Branch on Busy
526  B 5 0 0 .        Return to Seek
600  * 0 0 0 0 0 0
700  * 0 1 0 0 0 0
```

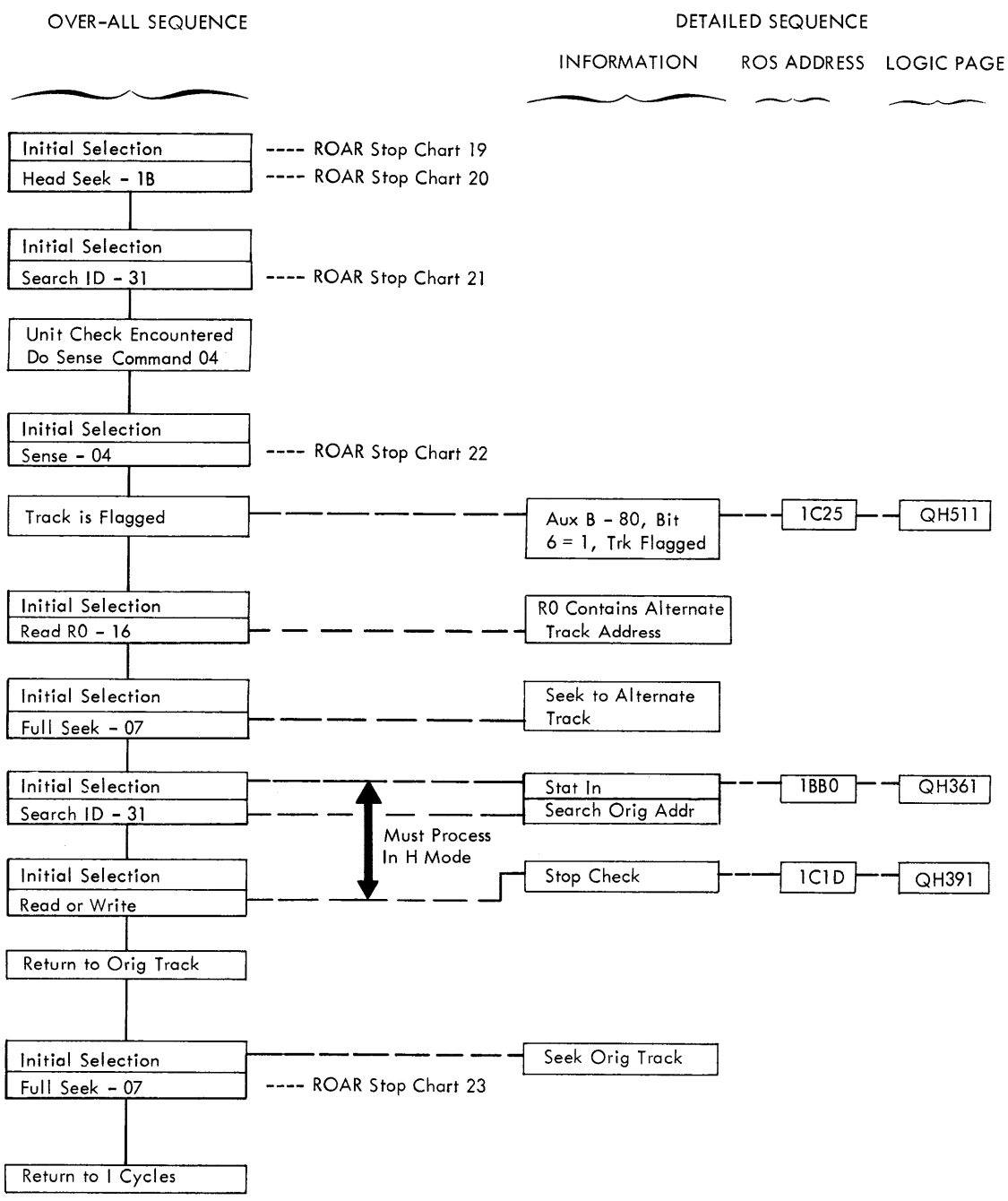
SEEK OPERATION -07



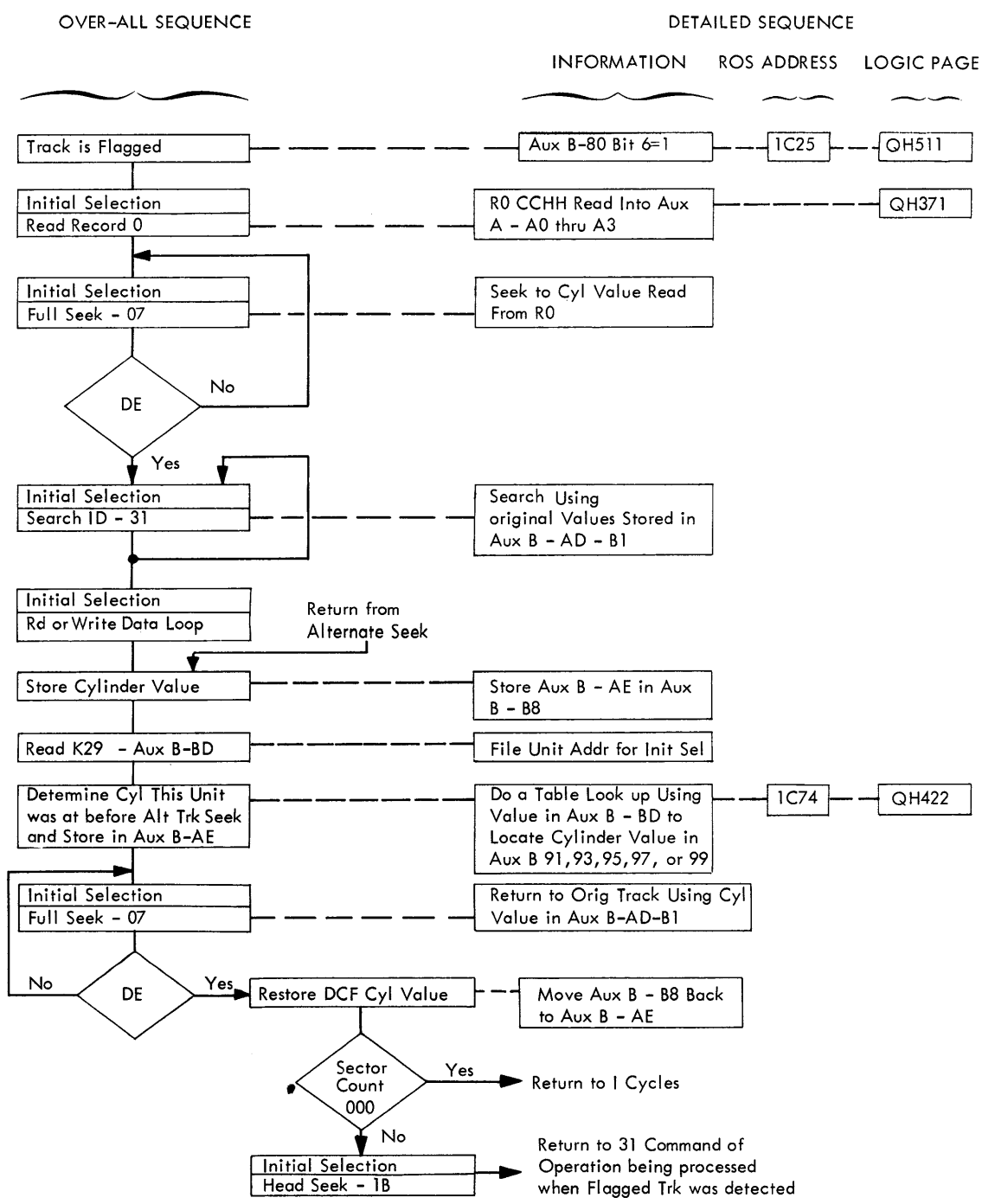
Seek Operation RS Chart 23 (Sheet 1)

ALTERNATE TRACK ENTRY AND EXIT OBJECTIVE

Refer to Individual Flow Charts for Details on the Following Command Codes.



ALTERNATE TRACK ROUTINE



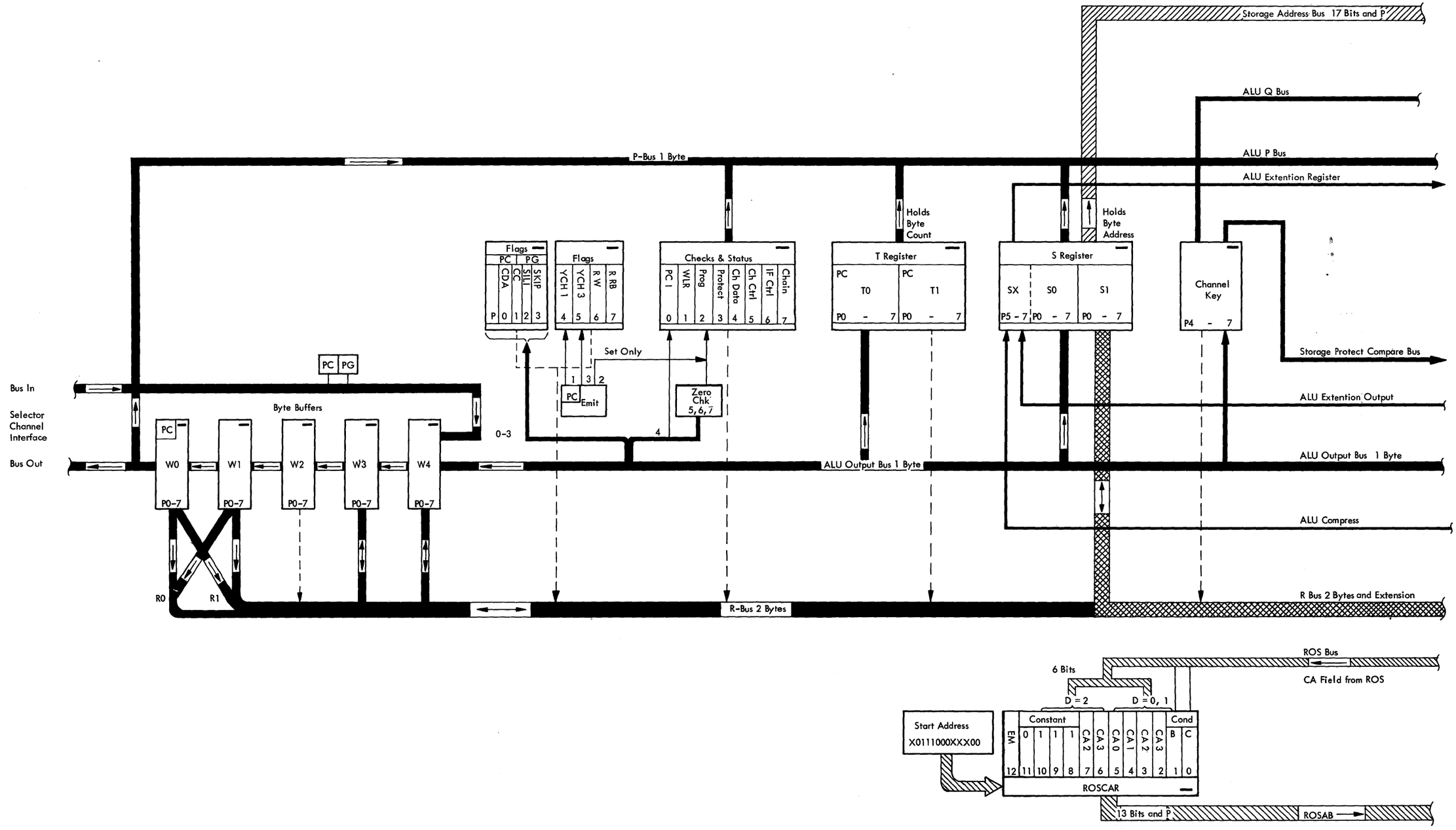


FIGURE 011. SELECTOR CHANNEL DATA FLOW

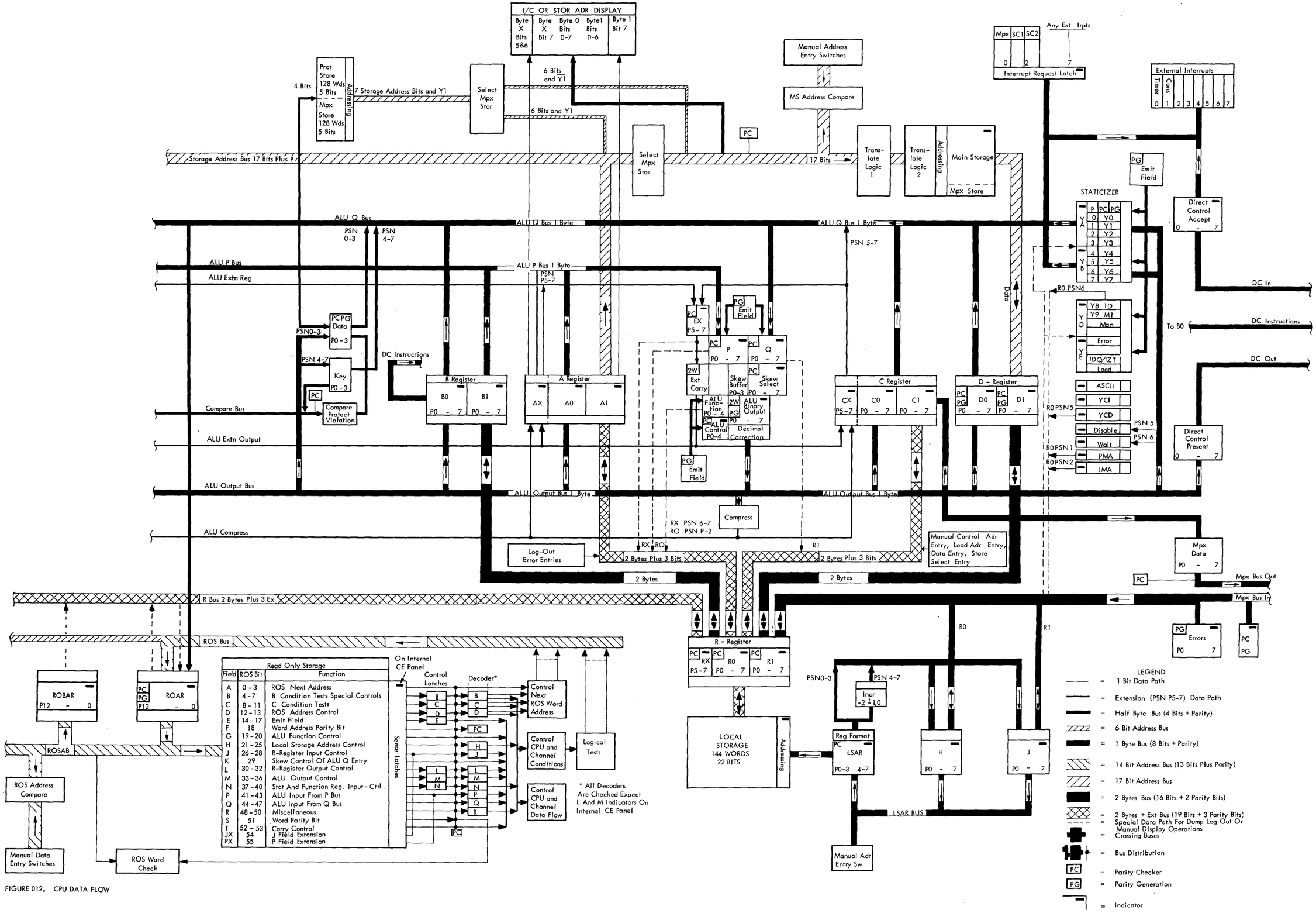


FIGURE 012. CPU DATA FLOW

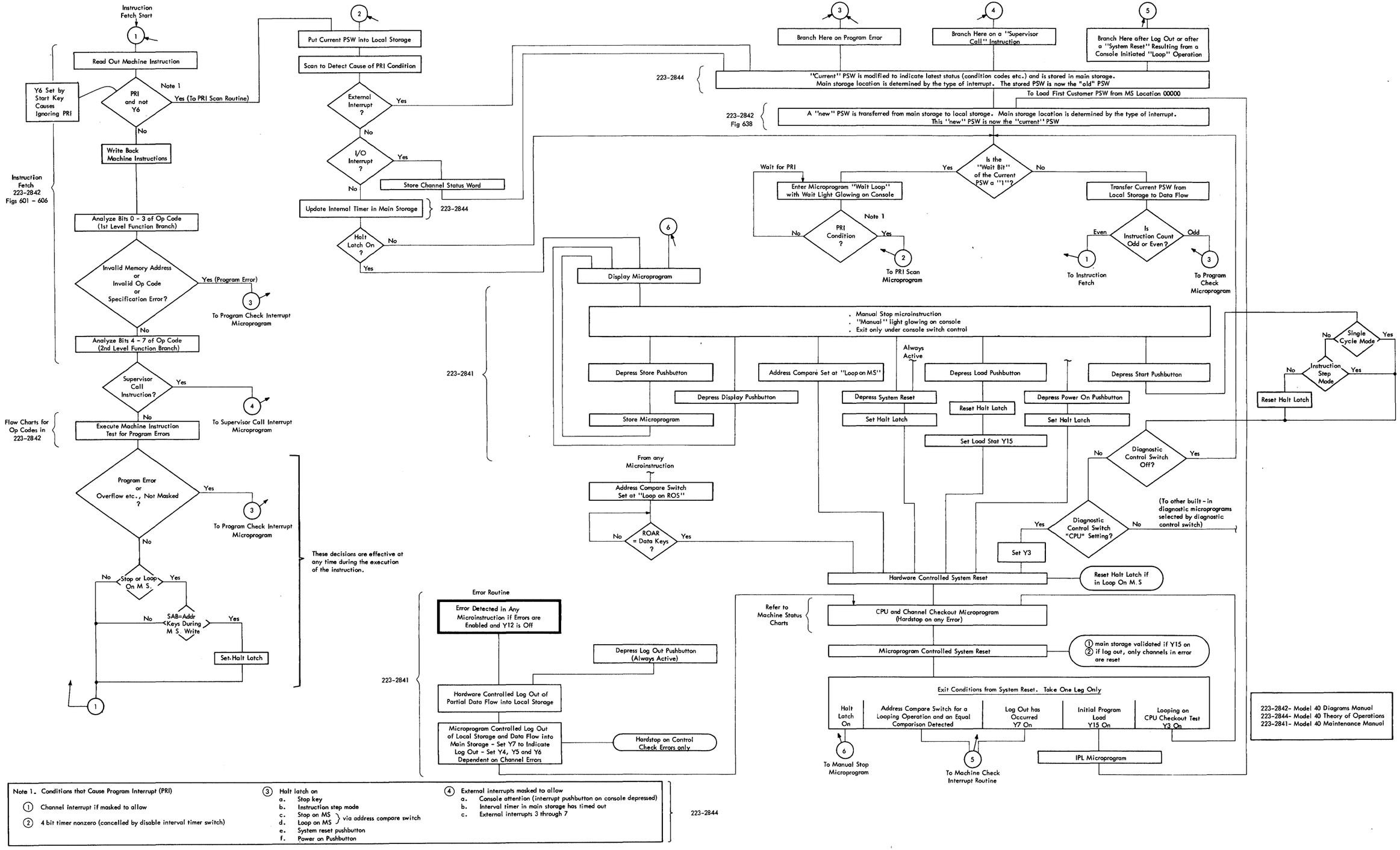


FIGURE 014. CPU MICROPROGRAM FLOW CHART (CHANNEL DATA SERVICE NOT SHOWN)

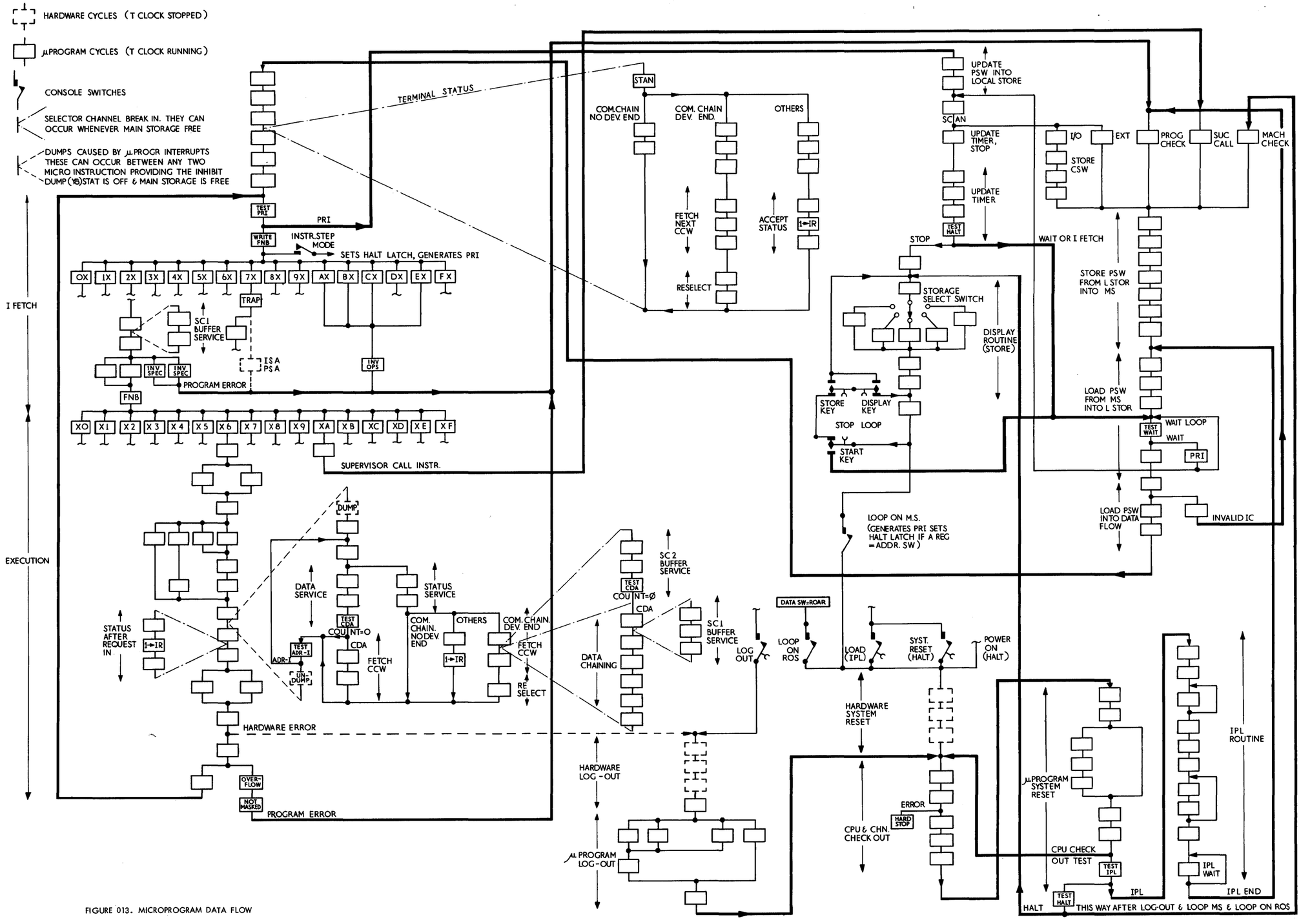


FIGURE 013. MICROPROGRAM DATA FLOW

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