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IBM System/360 Model 40
Operating Techniques

This manual describes operator procedures for an IBM 2040 Processing Unit. It is intended to be a handy reference manual for the user to take to an IBM Test Center for preparation of testing materials.

For information pertaining to operation of the units attachable to System/360 Model 40, refer to the appropriate SRL publication. SRL publications that pertain to IBM System/360 and attachable units are abstracted and referenced by form number in IBM System/360 Bibliography (A22-6822).

CONTENTS

Major Revision

This edition, C20-1635-2, is a major revision and completely obsoletes C20-1635-1. It removes a programming example no longer applicable, and updates the reference tables in Appendix A.

Copies of this and other IBM publications can be obtained through IBM branch offices. Address comments concerning the contents of this publication to IBM, Technical Publications Department, 112 East Post Road, White Plains, N.Y. 10601

SYSTEM/360 MODEL 40 CONFIGURATION EXAMPLE

SYSTEM CONFIGURATION

CPU Features

128K Storage Capacity
Storage Protection Feature
Mode Set Commands (TAU Modifier Bits)
Universal Instruction Set
One Multiplexor Channel
Two Selector Channels
Interval Timer

I/O Units and Addresses

DEVICE	ADDRESS
Tapes (2400), Selector Channel 1	180, 181 -- 7 track, 182, 183 -- 9 track
Tapes (2400), Selector Channel 2	280, 281 -- 7 track, 282, 283 -- 9 track
Card Reader-Punch (1442)	00A
Printer (1443)	00B
Card Reader (2540)	00C
Card Punch (2540)	00D
Printer (1403)	00E
Typewriter-Keyboard (1052)	009
Disk Storage (2311)	190

NOTE: LOAD/SYSTEM RESET forces Mode Set on all channels to 800 bpi, odd parity, data converter on, translator off, unless otherwise requested. Mode set applies only to 7-track tapes, with the exception of track-in-error sense information, which applies to 9-track tapes (1600 bpi).

I/O ADDRESS ASSIGNMENTS EXAMPLE

The three position device address XYZ indicates:

X -- Channel
- 0 = multiplexor
- 1 = selector channel 1
- 2 = selector channel 2

Y -- Control Unit
- 0 = peripheral or unit record
- 8 = magnetic tapes
- 9 = disk files

Z -- Device
- A = 1442 Card Reader-Punch
- B = 1443 Printer
- C = 2540 Reader
- D = 2540 Punch
- E = 1403 Printer
- 9 = 1052 Typewriter-Keyboard
- 0 to 9 = Tape or Disk Address

For example: I/O address 00A would be interpreted as being on the multiplexor channel whose subchannel is 0. The particular device selected is A, the 1442; I/O address 189 would be the tape drive number 9 on selector channel 1.

FUNCTIONS OF THE IBM 2040 SYSTEM CONTROL PANEL

The System Control Panel contains the switches, keys, and lights necessary to operate and control the system. The controls are divided into three sections: operator control, operator intervention, and field engineering control. In the following discussion, the operator's console refers to the former two sections, which constitute the lower half of the System Control Panel. The engineering control is the upper half.

All the keys, lights, and switches necessary for operator control and intervention are subsequently discussed; refer to Appendix D for the IBM 2040 Console diagram.

KEYS

LOAD -- loads from the I/O unit specified in the three LOAD UNIT SWITCHES on the console. Depressing the LOAD key causes execution of the system reset internal diagnostic sequence, then loads the first 24 bytes of information from the load unit into the first 24 bytes of main storage. This procedure is called initial program load (IPL).

START -- starts instruction execution in the manner defined by the RATE switch. This key is effective only when the CPU is in the stopped or manual state.

STOP -- causes the CPU to enter the stopped state as indicated by the MANUAL light on the console.

SYSTEM RESET -- stops all instruction processing; resets all indicators and lights on the console; resets channels, online nonshared control units, and I/O devices. It also restores the tape modes on all channels to their original setting (usually 800 bpi odd parity, data converter on, translator off). It does not reset any of the registers, or alter main storage.

CHECK RESET -- resets the three main error triggers. Specifically, it resets the EARLY, LATE and C'NTRL lights in the upper left portion of the System Control Panel. It does not reset any of the registers or channels.

PSW RESTART -- causes the IPL PSW to be fetched from core storage location zero (provided the CPU is in the manual state). The CPU then continues to process starting at the location indicated by the Instruction Address portion of the IPL PSW.

INTERRUPT -- requests an external interrupt, provided the PSW is masked to allow external interrupts.

STORE -- causes the information specified by the INSTRUCTION COUNTER OR STORAGE ADDRESS and STORAGE DATA keys to be entered in the area specified by the STORAGE SELECT switch. When the STORE key is being used, storage protection is ignored.

DISPLAY -- displays information in the location specified by the STORAGE SELECT and STORAGE ADDRESS switches.

POWER ON, POWER OFF -- initiates the power on or power off sequence for the entire system. Before initiating the power off sequence each I/O device must be at its not ready or unloaded state.

SWITCHES

ADDRESS COMPARE (a rotary switch) -- provides the means of stopping the CPU at a predetermined address (indicated by the INSTRUCTION COUNTER OR STORAGE ADDRESS keys) when in the MS position. An equal address comparison causes the CPU to enter the manual state.

LOAD UNIT (three rotary switches) -- provides the "XYZ" (eleven-bit) address of the input device to be used for initial program loading. The left-most switch, corresponding to the "X" position of the device address, has eight positions labeled 0 - 7. The other two switches, "Y" and "Z", have 16 positions each, and are labeled with the hexadecimal characters 0 - F. (Refer to the I/O address assignments example given earlier.)

RATE (a rotary switch) -- indicates the manner in which instructions are to be performed. The position of the switch should be changed only while the CPU is in the manual state. The RATE switch has the following settings:

PROCESS. In this position, the system operates at normal speed.

INSTRUCTION STEP. When the START key is pressed with the RATE switch in this position, one complete instruction is performed, and the CPU then returns to the manual state. The Interval Timer is not updated when the switch is in this position.

SINGLE-CYCLE (ordinarily for customer engineering use only). In this position single-cycling of each phase of an instruction is allowed.

STORAGE SELECT (a rotary switch) -- selects the storage area to be addressed by the ADDRESS switches. It can be manipulated without disrupting CPU operations, and has the following settings:

FP -- Floating Point Registers
GP -- General Purpose Registers
PSW -- Current Program Status Word
MS -- Main Storage
IC -- Instruction Counter
SP -- Storage Protect

LIGHTS

LOAD -- is turned on when the LOAD key is pressed for initial program loading (IPL), and remains on until the loading process has been terminated (that is, until the CCWs have been successfully executed).

WAIT -- is on when the CPU is in the wait state.

MANUAL -- is on when the CPU is in the stopped state or manual mode (caused by pressing the STOP key or the SYSTEM RESET key). In this state, the CPU is not actually stopped, but rather is cycling through the microprogram. To exit from this state (that is, to resume instruction processing), press the START key.

TEST -- is on when the ADDRESS COMPARE, INTERFACE CONTROL, CPU, and RATE switches are in other than their normal positions.

SYSTEM -- is on when the CPU is in the running state.

DATA AND ADDRESS -- LIGHTS AND SWITCHES

Directly above the System Control Panel keys are two individual sets of lights and switches. They each have a length of two bytes (one halfword).

STORAGE DATA -- specify the data to be stored in the location indicated by the INSTRUCTION COUNTER OR STORAGE ADDRESS keys, and the STORAGE SELECT switch. The lights directly above the STORAGE DATA keys indicate the information being displayed or stored.

INSTRUCTION COUNTER OR STORAGE ADDRESS -- specify the address of the halfword of storage to be altered or displayed; these keys may also be used to indicate the number of the register (general purpose or floating point) to be altered or displayed. They can be manipulated without disrupting CPU operations only when the ADDRESS COMPARE switch is in the PROCESS position.

INITIAL PROGRAM LOADING (IPL)

Initial program loading is started manually by selecting the desired input device with the three LOAD UNIT (XYZ) switches, and then pressing the LOAD key. The first 24 bytes (six words) of information are loaded from the device selected into positions 0-23 of storage. These positions contain the initial program load program status word (IPL PSW), and the two channel command words (CCW) after initial loading. The IPL PSW will be in positions 0-7, and the CCWs in 8-23. If loading was not successful, the CPU idles (SYSTEM light is on) and the LOAD light remains on.

If, at the beginning of a job, any individual unit cannot be readied, press the SYSTEM RESET key on the console. This should reset all unusual conditions. (Note, however, that if this key is depressed while running a job, information already on the channels or interface units will be lost.)

Since this IPL procedure executes the same internal diagnostic sequence and reset functions that the SYSTEM RESET key performs, the SYSTEM RESET key need not be pressed before IPL.

CLEAR STORAGE -- MANUALLY

The following procedure for clearing storage manually does not clear the general purpose or floating point registers:

1. Press the DSAB INTVL TIMER (disable interval timer) switch down.
2. Press the SYSTEM RESET key
3. Set the RATE switch to SINGLE CYCLE
4. Set the DIAGNOSTIC CONTROL switch to MS ADDRESS
5. Set bit 3 of byte 0 of the STORAGE DATA keys in the down position to address the clear storage microprogram.
6. Flip up the STORAGE STATS switch
7. RESET the RATE switch to PROCESS
8. Press START. This causes the microprogram that sets all of main storage to zeros to be executed. None of the STORAGE DATA lights should be on, but the microprogram light (μ P light in the upper left-hand portion of the field engineering console) should be on, to indicate successful completion. If this light does not come on, or if any other lights on the field engineering console are on, the clear storage procedure was not successful.

DISPLAYING -- STORAGE SELECT SWITCH

All console displaying on the System/360 Model 40 is done a halfword at a time only when the system is in the manual state. The STORAGE SELECT switch and the STORAGE ADDRESS keys are used for the register select, etc. All the data is displayed in the STORAGE DATA registers, bytes 0 and 1, except as indicated.

Floating Point Registers

1. Press the STOP or SYSTEM RESET key.
2. Set the STORAGE SELECT switch to FP.
3. Set the following bits in byte 1 of the STORAGE ADDRESS keys:
   Bits 0-3 (REGISTER SELECT switches), for the desired register to be displayed.
   Bits 4-5, ignore.
   Bits 6-7 (HALFWORD SELECT switches), to indicate which halfword is to be displayed, as follows:
   First halfword -- 00
   Second halfword -- 01
   Third halfword -- 10
   Last halfword -- 11
4. Press the DISPLAY button.

General Purpose Registers

1. Press the STOP or SYSTEM RESET key.
2. Set the STORAGE SELECT switch to GP.
3. Set the following bits of byte 1 of the STORAGE ADDRESS bit switches:
   Bits 0-3 (REGISTER SELECT switches), for the desired register to be displayed.
   Bits 4-5, ignore.
   Bits 6-7 (HALFWORD SELECT switches), to indicate which halfword is to be displayed, as follows:
   First halfword -- 00
   Second halfword -- 01
4. Press the DISPLAY button.

Current Program Status Word

1. Press the STOP or SYSTEM RESET key.
2. Set the STORAGE SELECT switch to PSW.
3. Set the following bits in byte 1 of the STORAGE ADDRESS keys:
   Bits 0-3 (REGISTER SELECT switches), ignore
   Bits 4-5, ignore.
   Bits 6-7 (HALFWORD SELECT switches), to indicate which halfword is to be displayed, as follows:
   First halfword -- 00
   Second halfword -- 01
   Third halfword -- 10
   Last halfword -- 11
4. Press the DISPLAY button.

Main Storage

1. Press the STOP or SYSTEM RESET key.
2. Set the STORAGE SELECT switch to MS.
3. Set the STORAGE ADDRESS keys for the desired storage address.
4. Press the DISPLAY button.

(Note that two bytes are always displayed in the STORAGE DATA lights at one time; byte 0 always displays the contents of an even numbered address, and byte 1 of the next higher odd numbered address. If an even numbered address is set into the STORAGE ADDRESS keys, byte 0 of the STORAGE DATA lights displays the contents of that address, and byte 1 displays the contents of the next higher odd numbered address. If an odd numbered address is set into the STORAGE ADDRESS keys, byte 1 of the STORAGE DATA lights displays the contents of the odd numbered address, and byte 0 displays the contents of the next lower even numbered address.)

Instruction Counter (Instruction Address Portion of PSW)

1. Press the STOP or SYSTEM RESET key.
2. Set the STORAGE SELECT switch to IC.
3. Press the DISPLAY key. The entire 3 bytes of the IC are displayed; the first byte is in byte 1 of the STORAGE DATA lights; the second byte is in byte 0 of the INSTRUCTION COUNTER lights; and the third byte is in byte 1 of the INSTRUCTION COUNTER lights.

Storage Protection

1. Press the STOP or SYSTEM RESET key.
2. Set the STORAGE SELECT switch to SP.
3. Set in the STORAGE ADDRESS bit switches the storage address for which the protection information is desired.
4. Press the DISPLAY button; the following information will be displayed in bytes 0 and 1 of the STORAGE DATA lights:
   a. Byte 0 will be cleared.
   b. Bits 0-3 (SP DATA) of byte 1 contain the protection key for the block of core in which the desired storage address is located; this is called the "protection data"
   c. Bits 4-7 (SP KEY) contain the protection key in the current PSW (bits 8-11 in the (PSW); this is called the "protection tag".

ALTERING -- STORAGE SELECT SWITCH

Main Storage

The altering or changing of the contents of main storage (done only when the system is in the manual state) always involves two bytes at a time, even though only one of the bytes may be actually changed. The procedure is as follows:

1. Press the STOP or SYSTEM RESET key.
2. Set the STORAGE SELECT switch to MS.
3. Set the STORAGE ADDRESS keys to the address of the data to be changed.
4. Set the STORAGE DATA keys as follows:

If the content of an even numbered address is to be changed, set the new data in the byte 0 STORAGE DATA keys. Also, since two bytes are always stored at the same time, the data already stored in the odd numbered address (next above the even address being changed) must be repeated in byte 1 of the STORAGE DATA keys, so that it may be "restored" at the same time the contents of the even numbered address are changed.

If the content of an odd numbered address is to be changed, set the new data in the byte 1 DATA STORAGE keys, and "repeat" the data already stored in the next lower even numbered address in byte 0 of the STORAGE DATA keys.

5. Press the STORE key; the data stored will be displayed in the STORAGE DATA lights.

Current PSW, FP, and GP Registers

The procedure for changing data in any of these registers (done only when the system is in the manual state) which is similar to the procedure for displaying the respective registers is as follows:

1. Press the STOP or SYSTEM RESET key.
2. Set the STORAGE SELECT switch to select the desired type of register.
3. Set bits 0-3 of byte 1 of the STORAGE ADDRESS keys to select the desired number of the register.
4. Set bits 4-7 of byte 1 of the STORAGE ADDRESS keys to select the halfword to be changed.
5. Set the STORAGE DATA keys for the halfword of data to be stored.
6. Press the STORE key; the data stored will be displayed in the STORAGE DATA lights.
7. Repeat steps 3 through 5 for all halfwords of data to be changed.

Instruction Counter

To manually transfer to another location in main storage (that is, to set the IC to a new starting point) when the CPU is in any state other than the wait state:

1. Press the STOP key to place the CPU in the manual state.
2. Set the STORAGE SELECT switch to IC.
3. Set the STORAGE ADDRESS keys to the transfer location.

4. Press the STORE button.

5. Press the START button to resume processing at the new location.

NOTE: The transfer to another location can also be accomplished by altering the Instruction Address (last three bytes) of the current PSW.

To alter the IC in wait state, the wait state bit in the current PSW (bit 14) must first be cleared. This returns the system to the operating state as indicated by the SYSTEM light on the console.

1. Press the STOP or SYSTEM RESET key.

2. Display the first halfword of the current PSW in the STORAGE DATA lights.

3. Restore the contents of the first halfword with the exception of the wait state bit (byte 1, bit 6 in the Storage Data lights). This turns the wait state off.

4. Follow the above steps for transferring to another location of storage

Storage Protect Key

To change the protection information associated with a given block of core (in blocks of 2048 bytes):

1. Press the STOP button.

2. Set the STORAGE SELECT switch to SP.

3. Set the STORAGE ADDRESS keys to the storage address that is to be changed.

4. In the SP DATA keys, bits 0-3 of byte 1, key in the new "Protection Data"; in bits 4-7 (SP KEY) of byte 1, key in the new "Protection Tag" (byte 0 is ignored for this operation).

5. Press the STORE button.

6. Press the START button to resume processing.

CONTINUOUS LOOPING

When a program is continuously looping in execution (indicated by console lights steadily flashing, and no indication of correct processing) and it is desired to trace the loop:

1. Press the STOP button.

2. Record the current PSW.

3. Record the CAW, if the loop involves some I/O function.

4. Set the STORAGE SELECT switch to IC.

5. Set the RATE switch to INSTRUCTION STEP.

6. Press the START key; one instruction is executed, and the address of the next sequential instruction is displayed in the STORAGE ADDRESS lights. Record the displayed address, and keep pressing the START key until this recorded address is again displayed in the STORAGE ADDRESS lights, that is, until one loop is completed.

7. Reset the RATE switch to PROCESS.

8. Take a core dump.

ADDRESS STOP

To stop the CPU at a specified address:

1. Press the STOP key.

2. Set the ADDRESS COMPARE switch to MS STOP.

3. Place the desired address in the STORAGE ADDRESS keys.

4. Press the START button.

The system will resume processing until an equal address comparison is made. The CPU then switches itself to the manual state. This condition will occur when an equal comparison is made on an instruction or a data address.

ANALYZING AN UNEXPECTED WAIT STATE CONDITION

If the CPU unexpectedly switches to the wait state as indicated by the WAIT light on the console, the contents of the current PSW should be examined, and then a core dump should be taken. Note that PSW is an internal register that will be destroyed by any core dump program.

If any of the System/360 BPS Utility programs are being used, bits 40 to 63 of the current PSW, which normally contain the instruction address, will contain a three-byte BCD message indicating the type of error. For example, if the instruction address field of the current PSW contains D3D7C1, decoded LPA, this signifies that a program check has occurred; a core dump helps to investigate further the cause. In this example, the old program PSW should be examined starting in location 28 hexadecimal. This action helps to isolate the cause of the program check and where it occurred. The instruction address (which caused the wait state) minus the instruction length code is found at location hexadecimal 2E.

Under the BPS packages, an I/O interrupt will also switch the CPU to the wait state. In this case, the above procedure should be followed, except that the old I/O PSW (starting in hexadecimal location 38) should be examined instead of the old program PSW.

Refer to Operating Guide for Basic Assembler and Utilities (C28-6557) for the list of codes (and corresponding descriptions) that replace the instruction address in the current program PSW following an unexpected switch by the CPU to the wait state. Appendix C contains a reference list.

ANALYZING INPUT/OUTPUT COMMANDS

For analyzing I/O commands for any reason whatever, the procedure for using either the console or a core dump to determine the last I/O command

issued, the device associated with that command, and the status or result of the execution of that command, is as follows:

1. Examine the Channel Address Word (CAW -- fullword at location 48 hexadecimal), which contains the address of the Channel Command Word (CCW). (Refer to Appendix C for formats.)

(NOTE: If I/O command chaining was employed, the CAW will contain the address of the first CCW.)

2. Analyze the Channel Status Word (CSW -- doubleword starting at location 40 hexadecimal). The CSW has three significant parts: (a) the command address of the CCW, (b) the status of the channel, etc., and (c) the residual byte count (which may be zero).

a. The command address portion of the CSW always contains the address of the last CCW executed plus eight bytes.

b. The status portion (bits 32 through 47) of the CSW halfword at location 44 hexadecimal contains the status of the channel control unit or subchannel, and the status of the device to which the I/O command was issued. Each I/O device that can be attached to the system has its own characteristics as far as status bits are concerned. Refer to the individual SRL for each I/O device status bit meaning, as they vary. The address of the particular device to which the I/O command was directed can normally be found in the Interruption Code portion (bits 16 through 31) of the old I/O PSW at location 3A hexadecimal.

c. The residual byte count should be zero at the completion of the I/O command. Otherwise, one of three things is indicated: (a) a wrong-length record was encountered; (b) a command reject was issued from the channel for the last I/O command received — in either of these two cases, something may be wrong with the user's channel program; (c) a data check occurs during a read or write operation causing data transfer to stop at the point where the error occurred, and causing device motion to stop at the end of the affected record. Channel end, device end, unit check and incorrect length indications are posted in the CSW, and the residual byte count may indicate the amount of data not stored.

When working with variable-length records, the wrong-length record indication in the CCW bit 34 should be on; otherwise, every time a record with a count different from that specified in the CCW is encountered, bit 41 in the CSW (incorrect length) will be turned on, causing an I/O interrupt (if the Basic I/O subroutines are used, the CPU will enter the wait state).

3. Check the Channel Command Word (CCW-- doubleword location on any doubleword boundary in storage). The CCW contains the data address, a byte count indicating the number of bytes involved in the operation, the command code defining the actual I/O operation, and the flag bits (if any) for command and data chaining, etc. Note that, initially, there must be a byte count of one or more for any I/O operation, except Transfer in Channel (TIC). (For the definitions of I/O device command codes, refer to the individual SRLs; Appendix B contains a reference list.)

APPENDIX A: REFERENCE TABLES FOR THE SYSTEM/360 UNITS

OPERATION CODES FOR:

RR FORMAT INSTRUCTIONS

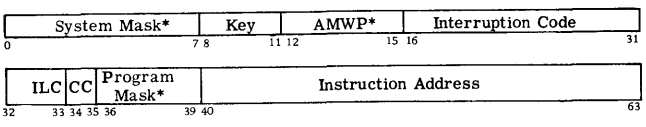
	Decimal	Hexadecimal	Mnemonic	Graphic & Control Symbols BCDIC	EBCDIC	(2) 7-Track Tape BCDIC	Punched Card Code	System/360 8-bit Code	(3)
Standard Instruction Set	0	00					12-0-9-8-1	0000 0000	CCW
	1	01					12-9-1	0000 0001	
	2	02					12-9-2	0000 0010	
	3	03					12-9-3	0000 0011	
	4	04	SPM		PF		12-9-4	0000 0100	
	5	05	BALR		HT		12-9-5	0000 0101	
	6	06	BCTR		LC		12-9-6	0000 0110	
	7	07	BCR		DEL		12-9-7	0000 0111	
	8	08	SSK				12-9-8	0000 1000	CCW
	9	09	ISK				12-9-8-1	0000 1001	
	10	0A	SVC				12-9-8-2	0000 1010	
	11	0B					12-9-8-3	0000 1011	
	12	0C	(EBCDIC +)				12-9-8-4	0000 1100	
	13	0D	(EBCDIC −)				12-9-8-5	0000 1101	
	14	0E					12-9-8-6	0000 1110	
	15	0F			CU1		12-9-8-7	0000 1111	
	16	10	LPR				12-11-9-8-1	0001 0000	CCW
	17	11	LNR				11-9-1	0001 0001	
	18	12	LTR				11-9-2	0001 0010	
	19	13	LCR				11-9-3	0001 0011	
	20	14	NR		RES		11-9-4	0001 0100	
	21	15	CLR		NL		11-9-5	0001 0101	
	22	16	OR		BS		11-9-6	0001 0110	
	23	17	XR		IL		11-9-7	0001 0111	
	24	18	LR				11-9-8	0001 1000	CCW
	25	19	CR				11-9-8-1	0001 1001	
	26	1A	AR		CC		11-9-8-2	0001 1010	
	27	1B	SR				11-9-8-3	0001 1011	
	28	1C	MR				11-9-8-4	0001 1100	
	29	1D	DR				11-9-8-5	0001 1101	
	30	1E	ALR				11-9-8-6	0001 1110	
	31	1F	SLR		CU2		11-9-8-7	0001 1111	
Floating-Point Feature Instructions	32	20	LPDR				11-0-9-8-1	0010 0000	CCW
	33	21	LNDR				0-9-1	0010 0001	
	34	22	LTDR				0-9-2	0010 0010	
	35	23	LCDR				0-9-3	0010 0011	
	36	24	HDR		BYP		0-9-4	0010 0100	
	37	25			LF		0-9-5	0010 0101	
	38	26			EOB		0-9-6	0010 0110	
	39	27			PRE		0-9-7	0010 0111	
	40	28	LDR				0-9-8	0010 1000	CCW
	41	29	CDR				0-9-8-1	0010 1001	
	42	2A	N ADR		SM		0-9-8-2	0010 1010	
	43	2B	N SDR				0-9-8-3	0010 1011	
	44	2C	N MDR				0-9-8-4	0010 1100	
	45	2D	N DDR				0-9-8-5	0010 1101	
	46	2E	AWR				0-9-8-6	0010 1110	
	47	2F	SWR		CU3		0-9-8-7	0010 1111	
	48	30	LPER				12-11-0-9-8-1	0011 0000	CCW
	49	31	LNER				9-1	0011 0001	
	50	32	LTER				9-2	0011 0010	
	51	33	LCER				9-3	0011 0011	
	52	34	HER		PN		9-4	0011 0100	
	53	35			RS		9-5	0011 0101	
	54	36			UC		9-6	0011 0110	
	55	37			EOT		9-7	0011 0111	
	56	38	LER				9-8	0011 1000	CCW
	57	39	CER				9-8-1	0011 1001	
	58	3A	N AER				9-8-2	0011 1010	
	59	3B	N SER				9-8-3	0011 1011	
	60	3C	N MER				9-8-4	0011 1100	
	61	3D	N DER				9-8-5	0011 1101	
	62	3E	AUR				9-8-6	0011 1110	
	63	3F	SUR				9-8-7	0011 1111	

(2) Note that check bit (C) is not shown; add C bit for odd or even parity as needed except for even parity, decimal 64 is CA, the same as decimal 122
(3) CCW flag bit assignments
(4) Decimal feature instructions
(5) System/360 assembler programs require these codes

RX FORMAT INSTRUCTIONS

	Decimal	Hexadecimal	Mnemonic	Graphic & Control Symbols BCDIC	EBCDIC	(2) 7-Track Tape BCDIC	Punched Card Code	System/360 8-bit Code	(3)	(5)
Standard Instruction Set	64	40	STH		SP	(2)	no punches	0100 0000	CCW	
	65	41	LA				12-0-9-1	0100 0001		
	66	42	STC				12-0-9-2	0100 0010		
	67	43	IC				12-0-9-3	0100 0011		
	68	44	EX				12-0-9-4	0100 0100		
	69	45	BAL				12-0-9-5	0100 0101		
	70	46	BCT				12-0-9-6	0100 0110		
	71	47	BC				12-0-9-7	0100 0111		
	72	48	LH				12-0-9-8	0100 1000	CCW	
	73	49	CH				12-8-1	0100 1001		
	74	4A	AH		¢		12-8-2	0100 1010		
	75	4B	SH	.	.	B A 8 2 1	12-8-3	0100 1011		
	76	4C	MH	¤)	<	B A 8 4	12-8-4	0100 1100		
	77	4D		[	(	B A 8 4 1	12-8-5	0100 1101		(
	78	4E	CVD	<	+	B A 8 4 2	12-8-6	0100 1110		+
	79	4F	CVB	¥	!	B A 8 4 2 1	12-8-7	0100 1111		
	80	50	ST	& +	&	B A	12	0101 0000	CCW	
	81	51					12-11-9-1	0101 0001		
	82	52					12-11-9-2	0101 0010		
	83	53					12-11-9-3	0101 0011		
	84	54	N				12-11-9-4	0101 0100		
	85	55	CL				12-11-9-5	0101 0101		
	86	56	O				12-11-9-6	0101 0110		
	87	57	X				12-11-9-7	0101 0111		
	88	58	L				12-11-9-8	0101 1000	CCW	
	89	59	C				11-8-1	0101 1001		
	90	5A	A		!		11-8-2	0101 1010		
	91	5B	S	$	$	B 8 2 1	11-8-3	0101 1011		
	92	5C	M	*	*	B 8 4	11-8-4	0101 1100		
	93	5D	D	]	)	B 8 4 1	11-8-5	0101 1101		)
	94	5E	AL	;	;	B 8 4 2	11-8-6	0101 1110		
	95	5F	SL	¬	¬	B 8 4 2 1	11-8-7	0101 1111		
	96	60	STD	-	-	B	11	0110 0000	CCW	
	97	61		/	/	A 1	0-1	0110 0001		
	98	62					11-0-9-2	0110 0010		
	99	63					11-0-9-3	0110 0011		
	100	64					11-0-9-4	0110 0100		
	101	65					11-0-9-5	0110 0101		
	102	66					11-0-9-6	0110 0110		
	103	67					11-0-9-7	0110 0111		
Floating-Point Feature Instructions	104	68	LD				11-0-9-8	0110 1000	CCW	
	105	69	CD				0-8-1	0110 1001		
	106	6A	N AD				12-11	0110 1010		
	107	6B	N SD	,	,	A 8 2 1	0-8-3	0110 1011		
	108	6C	N MD	% (	%	A 8 4	0-8-4	0110 1100		
	109	6D	N DD	∨	—	A 8 4 1	0-8-5	0110 1101		
	110	6E	AW	\	>	A 8 4 2	0-8-6	0110 1110		
	111	6F	SW	⊣	?	A 8 4 2 1	0-8-7	0110 1111		
	112	70	STE				12-11-0	0111 0000	CCW	
	113	71					12-11-0-9-1	0111 0001		
	114	72					12-11-0-9-2	0111 0010		
	115	73					12-11-0-9-3	0111 0011		
	116	74					12-11-0-9-4	0111 0100		
	117	75					12-11-0-9-5	0111 0101		
	118	76					12-11-0-9-6	0111 0110		
	119	77					12-11-0-9-7	0111 0111		
	120	78	LE				12-11-0-9-8	0111 1000	CCW	
	121	79	CE				8-1	0111 1001		
	122	7A	N AE	¢	:	A	8-2	0111 1010		
	123	7B	N SE	# =	#	8 2 1	8-3	0111 1011		
	124	7C	N ME	@	@	8 4	8-4	0111 1100		
	125	7D	N DE	:	'	8 4 1	8-5	0111 1101		'
	126	7E	AU	>	=	8 4 2	8-6	0111 1110		=
	127	7F	SU	∨	"	8 4 2 1	8-7	0111 1111		

PROGRAM STATUS WORD



0-7 System mask
- 0 Multiplexer channel mask
- 1 Selector channel 1 mask
- 2 Selector channel 2 mask
- 3 Selector channel 3 mask
- 4 Selector channel 4 mask
- 5 Selector channel 5 mask
- 6 Selector channel 6 mask
- 7 External mask

8-11 Protection key
- 12 ASCII mode (A)
- 13 Machine check mask (M)
- 14 Wait state (W)
- 15 Problem state (P)

16-31 Interruption code
32-33 Instruction Length code (ILC)
34-35 Condition code (CC)
36-39 Program mask
- 36 Fixed-point overflow mask
- 37 Decimal overflow mask
- 38 Exponent underflow mask
- 39 Significance mask

40-63 Instruction address

*A one-bit equals on, and permits an interrupt.

PERMANENT STORAGE ASSIGNMENT

ADDRESS DEC	ADDRESS HEX	ADDRESS BINARY	LENGTH	PURPOSE
0	0	0000 0000	double-word	Initial program loading PSW
8	8	0000 1000	double-word	Initial program loading CCW1
16	10	0001 0000	double-word	Initial program loading CCW2
24	18	0001 1000	double-word	External old PSW
32	20	0010 0000	double-word	Supervisor call old PSW
40	28	0010 1000	double-word	Program old PSW
48	30	0011 0000	double-word	Machine-check old PSW
56	38	0011 1000	double-word	Input/output old PSW
64	40	0100 0000	double-word	Channel status word
72	48	0100 1000	word	Channel address word
76	4C	0100 1100	word	Unused
80	50	0101 0000	word	Timer (uses bytes 50,51 & 52)
84	54	0101 0100	word	Unused
88	58	0101 1000	double-word	External new PSW
96	60	0110 0000	double-word	Supervisor call new PSW
104	68	0110 1000	double-word	Program new PSW
112	70	0111 0000	double-word	Machine-check new PSW
120	78	0111 1000	double-word	Input/output new PSW
128	80	1000 0000	(1)	Diagnostic scan-out area

(1) The size of the diagnostic scan-out area depends on the particular model and I/O channels; for models 30 through 75, maximum size is 256 bytes.

RS, SI FORMAT INSTRUCTIONS

Decimal	Hexadecimal	Mnemonic	Graphic & Control Symbols BCDIC	Graphic & Control Symbols EBCDIC	(2) 7-Track Tape BCDIC	Punched Card Code	System/360 8-bit Code	(3)
128	80	SSM				12-0-8-1	1000 0000	CCW
129	81			a		12-0-1	1000 0001	
130	82	LPSW		b		12-0-2	1000 0010	
131	83	(Diagnose)		c		12-0-3	1000 0011	
132	84	WRD		d		12-0-4	1000 0100	
133	85	RDD		e		12-0-5	1000 0101	
134	86	BXH		f		12-0-6	1000 0110	
135	87	BXLE		g		12-0-7	1000 0111	
136	88	SRL		h		12-0-8	1000 1000	CCW
137	89	SLL		i		12-0-9	1000 1001	
138	8A	SRA				12-0-8-2	1000 1010	
139	8B	SLA				12-0-8-3	1000 1011	
140	8C	SRDL				12-0-8-4	1000 1100	
141	8D	SLDL				12-0-8-5	1000 1101	
142	8E	SRDA				12-0-8-6	1000 1110	
143	8F	SLDA				12-0-8-7	1000 1111	
144	90	STM				12-11-8-1	1001 0000	CCW
145	91	TM		j		12-11-1	1001 0001	
146	92	MVI		k		12-11-2	1001 0010	
147	93	TS		l		12-11-3	1001 0011	
148	94	NI		m		12-11-4	1001 0100	
149	95	CLI		n		12-11-5	1001 0101	
150	96	OI		o		12-11-6	1001 0110	
151	97	XI		p		12-11-7	1001 0111	
152	98	LM		q		12-11-8	1001 1000	CCW
153	99			r		12-11-9	1001 1001	
154	9A					12-11-8-2	1001 1010	
155	9B					12-11-8-3	1001 1011	
156	9C	SIO				12-11-8-4	1001 1100	
157	9D	TIO				12-11-8-5	1001 1101	
158	9E	HIO				12-11-8-6	1001 1110	
159	9F	TCH				12-11-8-7	1001 1111	
160	A0					11-0-8-1	1010 0000	CCW
161	A1					11-0-1	1010 0001	
162	A2			s		11-0-2	1010 0010	
163	A3			t		11-0-3	1010 0011	
164	A4			u		11-0-4	1010 0100	
165	A5			v		11-0-5	1010 0101	
166	A6			w		11-0-6	1010 0110	
167	A7			x		11-0-7	1010 0111	
168	A8			y		11-0-8	1010 1000	CCW
169	A9			z		11-0-9	1010 1001	
170	AA					11-0-8-2	1010 1010	
171	AB					11-0-8-3	1010 1011	
172	AC					11-0-8-4	1010 1100	
173	AD					11-0-8-5	1010 1101	
174	AE					11-0-8-6	1010 1110	
175	AF					11-0-8-7	1010 1111	
176	B0					12-11-0-8-1	1011 0000	CCW
177	B1					12-11-0-1	1011 0001	
178	B2					12-11-0-2	1011 0010	
179	B3					12-11-0-3	1011 0011	
180	B4					12-11-0-4	1011 0100	
181	B5					12-11-0-5	1011 0101	
182	B6					12-11-0-6	1011 0110	
183	B7					12-11-0-7	1011 0111	
184	B8					12-11-0-8	1011 1000	CCW
185	B9					12-11-0-9	1011 1001	
186	BA					12-11-0-8-2	1011 1010	
187	BB					12-11-0-8-3	1011 1011	
188	BC					12-11-0-8-4	1011 1100	
189	BD					12-11-0-8-5	1011 1101	
190	BE					12-11-0-8-6	1011 1110	
191	BF					12-11-0-8-7	1011 1111	

SS FORMAT INSTRUCTIONS

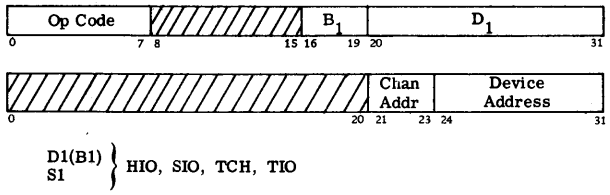
Decimal	Hexadecimal	Mnemonic	Graphic & Control Symbols BCDIC	Graphic & Control Symbols EBCDIC	(2) 7-Track Tape BCDIC	Punched Card Code	System/360 8-bit Code	(3)
192	C0		?		B A 8 2	12-0	1100 0000	CCW
193	C1		A	A	B A 1	12-1	1100 0001	
194	C2		B	B	B A 2	12-2	1100 0010	
195	C3		C	C	B A 2 1	12-3	1100 0011	
196	C4		D	D	B A 4	12-4	1100 0100	
197	C5		E	E	B A 4 1	12-5	1100 0101	
198	C6		F	F	B A 4 2	12-6	1100 0110	
199	C7		G	G	B A 4 2 1	12-7	1100 0111	
200	C8		H	H	B A 8	12-8	1100 1000	CCW
201	C9		I	I	B A 8 1	12-9	1100 1001	
202	CA					12-0-9-8-2	1100 1010	
203	CB					12-0-9-8-3	1100 1011	
204	CC					12-0-9-8-4	1100 1100	
205	CD					12-0-9-8-5	1100 1101	
206	CE					12-0-9-8-6	1100 1110	
207	CF					12-0-9-8-7	1100 1111	
208	D0		!		B 8 2	11-0	1101 0000	CCW
209	D1	MVN	J	J	B 1	11-1	1101 0001	
210	D2	MVC	K	K	B 2	11-2	1101 0010	
211	D3	MVZ	L	L	B 2 1	11-3	1101 0011	
212	D4	NC	M	M	B 4	11-4	1101 0100	
213	D5	CLC	N	N	B 4 1	11-5	1101 0101	
214	D6	OC	O	O	B 4 2	11-6	1101 0110	
215	D7	XC	P	P	B 4 2 1	11-7	1101 0111	
216	D8		Q	Q	B 8	11-8	1101 1000	CCW
217	D9		R	R	B 8 1	11-9	1101 1001	
218	DA					12-11-9-8-2	1101 1010	
219	DB					12-11-9-8-3	1101 1011	
220	DC	TR				12-11-9-8-4	1101 1100	
221	DD	TRT				12-11-9-8-5	1101 1101	
222	DE	ED (4)				12-11-9-8-6	1101 1110	
223	DF	EDMK (4)				12-11-9-8-7	1101 1111	
224	E0		✦		A 8 2	0-8-2	1110 0000	CCW
225	E1					11-0-9-1	1110 0001	
226	E2		S	S	A 2	0-2	1110 0010	
227	E3		T	T	A 2 1	0-3	1110 0011	
228	E4		U	U	A 4	0-4	1110 0100	
229	E5		V	V	A 4 1	0-5	1110 0101	
230	E6		W	W	A 4 2	0-6	1110 0110	
231	E7		X	X	A 4 2 1	0-7	1110 0111	
232	E8		Y	Y	A 8	0-8	1110 1000	CCW
233	E9		Z	Z	A 8 1	0-9	1110 1001	
234	EA					11-0-9-8-2	1110 1010	
235	EB					11-0-9-8-3	1110 1011	
236	EC					11-0-9-8-4	1110 1100	
237	ED					11-0-9-8-5	1110 1101	
238	EE					11-0-9-8-6	1110 1110	
239	EF					11-0-9-8-7	1110 1111	
240	F0		0	0	8 2	0	1111 0000	CCW
241	F1	MVO	1	1	1	1	1111 0001	
242	F2	PACK	2	2	2	2	1111 0010	
243	F3	UNPK	3	3	2 1	3	1111 0011	
244	F4		4	4	4	4	1111 0100	
245	F5		5	5	4 1	5	1111 0101	
246	F6		6	6	4 2	6	1111 0110	
247	F7		7	7	4 2 1	7	1111 0111	
248	F8	ZAP (4)	8	8	8	8	1111 1000	CCW
249	F9	CP (4)	9	9	8 1	9	1111 1001	
250	FA	AP (4)				12-11-0-9-8-2	1111 1010	
251	FB	SP (4)				12-11-0-9-8-3	1111 1011	
252	FC	MP (4)				12-11-0-9-8-4	1111 1100	
253	FD	DP (4)				12-11-0-9-8-5	1111 1101	
254	FE					12-11-0-9-8-6	1111 1110	
255	FF					12-11-0-9-8-7	1111 1111	

CODE FOR PROGRAM INTERRUPTION

Interruption Code			Program Interruption Cause
DEC	HEX	BINARY	
1	01	0000 0001	Operation
2	02	0000 0010	Privileged operation
3	03	0000 0011	Execute
4	04	0000 0100	Protection
5	05	0000 0101	Addressing
6	06	0000 0110	Specification
7	07	0000 0111	Data
8	08	0000 1000	Fixed-point overflow
9	09	0000 1001	Fixed-point divide
10	0A	0000 1010	Decimal overflow
11	0B	0000 1011	Decimal divide
12	0C	0000 1100	Exponent overflow
13	0D	0000 1101	Exponent underflow
14	0E	0000 1110	Significance
15	0F	0000 1111	Floating-point divide

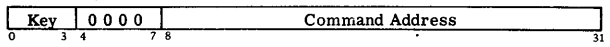
INPUT/OUTPUT OPERATIONS

SI Format

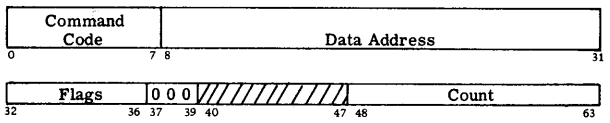


D1(B1)
S1
} HIO, SIO, TCH, TIO

CHANNEL ADDRESS WORD



CHANNEL COMMAND WORD



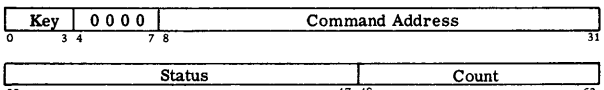
Command Code assignments are listed in the following table. The symbol X indicates that the bit position is ignored; M identifies a modifier bit.

CODE	COMMAND
MMMM 0 1 0 0	Sense
XXX X 1 0 0 0	Transfer in channel
MMMM 1 1 0 0	Read backward
MMMM MM0 1	Write
MMMM MM1 0	Read
MMMM MM1 1	Control

Bits 0-7 specify the command code.
Bits 8-31 specify the location of a byte in main storage.
Bits 32-36 are flag bits; refer to OPERATION CODE tables for flag bit assignments.
- Bit 32 causes the address portion of the next CCW to be used.
- Bit 33 causes the command code and data address in the next CCW to be used.
- Bit 34 causes a possible incorrect length indication to be suppressed.
- Bit 35 suppresses the transfer of information to main storage.
- Bit 36 causes an interruption as Program Control Interrupt

Bits 37-39 must contain zeros.
Bits 40-47 are ignored.
Bits 48-63 specify the number of bytes in the operation.

CHANNEL STATUS WORD



32	Attention	40	Program-controlled interruption
33	Status modifier	41	Incorrect length
34	Control unit end	42	Program check
35	Busy	43	Protection check
36	Channel end	44	Channel data check
37	Device end	45	Channel control check
38	Unit check	46	Interface control check
39	Unit exception	47	Chaining check

Count: Bits 48-63 form the residual count for the last CCW used.

CHANNEL COMMAND CODES

Device	Command for CCW	8-Bit Code 0	1	2	3	4	5	6	7	Hex	Dec
1052	Read Inquiry BCD	0	0	0	0	1	0	1	0	0A	10
	Read Reader 2 BCD	0	0	0	0	0	0	1	0	02	02
	Write BCD, Auto Carriage Return	0	0	0	0	1	0	0	1	09	09
	Write BCD, No Auto Carriage Return	0	0	0	0	0	0	0	1	01	01
	No Op	0	0	0	0	0	0	1	1	03	03
	Sense	0	0	0	0	0	1	0	0	04	04
	Alarm	0	0	0	0	1	0	1	1	0B	11
2540	Read, Feed, Select Stacker SS — Type AA	S	S	D	0	0	0	1	0		
	Read — Type AB	1	1	D	0	0	0	1	0		
	Read, Feed (1400 compatability mode only)	1	1	D	1	0	0	1	0		
	Feed, Select Stacker SS — Type BA	S	S	1	0	0	0	1	1		
	PFR Punch, Feed, Select Stacker SS — Type BA	S	S	D	0	1	0	0	1		
	Punch, Feed, Select Stacker SS — Type BB	S	S	D	0	0	0	0	1		
1442 N1	Read — MMM 0 0 X Eject and SS1	M	M	M	0	0	0	1	0		
	Write — MMM 0 0 0 1	M	M	M	0	0	0	0	1		
	Control — MM0 0 0 0 1 1	M	M	0	0	0	0	1	1		
	Read — 0 1 X Eject and SS2	0	0	0	0	0	0	1	1		
	Read — 1 1 X Eject and SS2	0	0	M	M	0	1	0	0		
	Write — 0 0 X SS1										
	Write — 1 0 X Eject and SS1										
	Write — 0 1 X SS2										
	Write — 1 1 X Eject and SS2										
	Control — 1 0 Eject and SS1										
	Control — 0 1 SS2										
	Control — 1 1 Eject and SS2										
	Sense — 1 1 Punch diagnostic										
	Sense — 0 1 Read diagnostic										
1403 or 1443	Write, No Space	0	0	0	0	0	0	0	1	01	01
	Write, Space 1 After Print	0	0	0	0	1	0	0	1	09	09
	Write, Space 2 After Print	0	0	0	1	0	0	0	1	11	17
	Write, Space 3 After Print	0	0	0	1	1	0	0	1	19	25
	Write, Skip To Channel N After Print	1	C	H	A	N	0	0	1		
	Diagnostic Read (1403)	0	0	0	0	0	0	1	0	02	02
	Diagnostic Read (1443)	0	0	0	0	0	1	1	0	06	06
	Test I/O	0	0	0	0	0	0	0	0	00	00
	Sense	0	0	0	0	0	1	0	0	04	04
Carriage Control	Space 1 Line Immediately	0	0	0	0	1	0	1	1	0B	11
	Space 2 Line Immediately	0	0	0	1	0	0	1	1	13	19
	Space 3 Line Immediately	0	0	0	1	1	0	1	1	1B	27
	Skip To Channel N Immediately	1	C	H	A	N	0	1	1		
	No Op	0	0	0	0	0	0	1	1	03	03
2400 Tape*	Transfer in Channel	0	0	0	0	1	0	0	0	08	08
	Sense	0	0	0	0	0	1	0	0	04	04
	Read Backward**	0	0	0	0	1	1	0	0	0C	12
	Write	0	0	0	0	0	0	0	1	01	01
	Read	0	0	0	0	0	0	1	0	02	02
	Control	0	0	C	C	C	1	1	1		
	Mode Set	D	D	M	M	M	0	1	1		

* 9 track op. forces 800 BPI and odd parity; also, it overrides 7 track but does not reset 7 track. Load/Sys Reset forces 7 track to 800 BPI, odd parity, data converter on, translator off.

C	C	C	Control Codes	Hex	Dec
0	0	0	REW	7	7
0	0	1	RUN	0F	15
0	1	0	ERG	17	23
0	1	1	WTM	1F	31
1	0	0	BSR	27	39
1	0	1	BSF	2F	47
1	1	0	FSR	37	55
1	1	1	FSF	3F	63

C	H	A	N	Channel
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6

C	H	A	N	Channel
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12

D	D	7 Track Density
0	0	200
0	1	556
1	0	800
1	1	800

M M M (Mode Modifiers)	Set Density	Set Odd Parity	Set Even Parity	Data Converter On	Data Converter Off	Translator On	Translator Off	Request T/E (Track in Error)
0 0 0 No Op								
0 0 1 Not Used								
0 1 0 Reset Condition	X	X		X			X	
0 1 1 Nine-track only								X
1 0 0	X		X		X		X	
1 0 1	X		X		X	X		
1 1 0 Reset Condition	X	X			X		X	
1 1 1	X	X			X	X		

**Overrides Data Converter On

HEXADECIMAL AND DECIMAL INTEGER CONVERSION TABLE

HALF WORD								HALF WORD							
BYTE				BYTE				BYTE				BYTE			
0123		4567		0123		4567		0123		4567		0123		4567	
Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	268,435,456	1	16,777,216	1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	536,870,912	2	33,554,432	2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	805,306,368	3	50,331,648	3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	1,073,741,824	4	67,108,864	4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	1,342,177,280	5	83,886,080	5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	1,610,612,736	6	100,663,296	6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	1,879,048,192	7	117,440,512	7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	2,147,483,648	8	134,217,728	8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	2,415,919,104	9	150,994,944	9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	2,684,354,560	A	167,772,160	A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	2,952,790,016	B	184,549,376	B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	3,221,225,472	C	201,326,592	C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	3,489,660,928	D	218,103,808	D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	3,758,096,384	E	234,881,024	E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	4,026,531,840	F	251,658,240	F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
8		7		6		5		4		3		2		1	

TO CONVERT HEXADECIMAL TO DECIMAL

1. Locate the column of decimal numbers corresponding to the left-most digit or letter of the hexadecimal; select from this column and record on a scratch sheet the number that corresponds to the position of the hexadecimal digit or letter.
2. Repeat step 1 for the next (second from the left) position.
3. Repeat step 1 for the units (third from the left) position.
4. Add the numbers selected from the table to form the decimal number.

SAMPLE	
Conversion of Hexadecimal	D34
1. D	3328
2. 3	48
3. 4	4
4. Decimal	3380

TO CONVERT DECIMAL TO HEXADECIMAL

1. (a) Select from the table the highest decimal number that is equal to or less than the number to be converted.
   (b) Record the hexadecimal of the column containing the selected number.
   (c) Subtract the selected decimal from the number to be converted.
2. Using the remainder from step 1 (c) repeat all of step 1 to develop the second position of the hexadecimal (and a remainder).
3. Using the remainder from step 2 repeat all of step 1 to develop the units position of the hexadecimal.
4. Combine terms to form the hexadecimal number.

SAMPLE	
Conversion of Decimal	3380
1. D	-3328
	52
2. 3	-48
	4
3. 4	-4
4. Hexadecimal	D34

To convert integer numbers greater than the capacity of the table, use the techniques below:

- HEXADECIMAL TO DECIMAL

Successive cumulative multiplication from left to right, adding units position.

Example: $D34_{16} = 3380_{10}$

$$D = 13$$
$$\times\ 16$$
$$208$$
$$3 = +\ 3$$
$$211$$
$$\times\ 16$$
$$3376$$
$$4 = +\ 4$$
$$3380$$

- DECIMAL TO HEXADECIMAL

Divide and collect the remainder in reverse order.

Example: $3380_{10} = X_{16}$

16 | 3380	→ remainder	
16 | 211	→ 4	
16 | 13	→ 3	
	→ D	$3380_{10} = D34_{16}$

HEXADECIMAL AND DECIMAL FRACTION CONVERSION TABLE

HALF WORD															
BYTE					BYTE										
	0123		4567			0123					4567				
Hex	Decimal	Hex	Decimal		Hex	Decimal			Hex	Decimal Equivalent					
.0	.0000	.00	.0000	0000	.000	.0000	0000	0000	.0000	.0000	0000	0000	0000		
.1	.0625	.01	.0039	0625	.001	.0002	4414	0625	.0001	.0000	1525	8789	0625		
.2	.1250	.02	.0078	1250	.002	.0004	8828	1250	.0002	.0000	3051	7578	1250		
.3	.1875	.03	.0117	1875	.003	.0007	3242	1875	.0003	.0000	4577	6367	1875		
.4	.2500	.04	.0156	2500	.004	.0009	7656	2500	.0004	.0000	6103	5156	2500		
.5	.3125	.05	.0195	3125	.005	.0012	2070	3125	.0005	.0000	7629	3945	3125		
.6	.3750	.06	.0234	3750	.006	.0014	6484	3750	.0006	.0000	9155	2734	3750		
.7	.4375	.07	.0273	4375	.007	.0017	0898	4375	.0007	.0001	0681	1523	4375		
.8	.5000	.08	.0312	5000	.008	.0019	5312	5000	.0008	.0001	2207	0312	5000		
.9	.5625	.09	.0351	5625	.009	.0021	9726	5625	.0009	.0001	3732	9101	5625		
.A	.6250	.0A	.0390	6250	.00A	.0024	4140	6250	.000A	.0001	5258	7890	6250		
.B	.6875	.0B	.0429	6875	.00B	.0026	8554	6875	.000B	.0001	6784	6679	6875		
.C	.7500	.0C	.0468	7500	.00C	.0029	2968	7500	.000C	.0001	8310	5468	7500		
.D	.8125	.0D	.0507	8125	.00D	.0031	7382	8125	.000D	.0001	9836	4257	8125		
.E	.8750	.0E	.0546	8750	.00E	.0034	1796	8750	.000E	.0002	1362	3046	8750		
.F	.9375	.0F	.0585	9375	.00F	.0036	6210	9375	.000F	.0002	2888	1835	9375		
1		2			3				4						

POWERS OF 16 TABLE

16^n	n
1	0
16	1
256	2
4 096	3
65 536	4
1 048 576	5
16 777 216	6
268 435 456	7
4 294 967 296	8
68 719 476 736	9
1 099 511 627 776	10
17 592 186 044 416	11
281 474 976 710 656	12
4 503 599 627 370 496	13
72 057 594 037 927 936	14
1 152 921 504 606 846 976	15

TO CONVERT .ABC HEXADECIMAL TO DECIMAL

Find .A in position 1 .6250

Find .0B in position 2 .0429 6875

Find .00C in position 3 .0029 2968 7500

.ABC Hex is equal to .6708 9843 7500

TO CONVERT .13 DECIMAL TO HEXADECIMAL

1. Find .1250 next lowest to subtract
   .1300
   - .1250 = .2 Hex
2. Find .0039 0625 next lowest to
   .0050 0000
   - .0039 0625 = .01
3. Find .0009 7656 2500
   .0010 9375 0000
   - .0009 7656 2500 = .004
4. Find .0001 0681 1523 4375
   .0001 1718 7500 0000
   - .0001 0681 1523 4375 = .0007

   .0000 1037 5976 5625 = .2147 Hex
5. .13 Decimal is approximately equal to ↑

To convert fractions beyond the capacity of the table, use techniques below:

● HEXADECIMAL FRACTION TO DECIMAL

Convert the hexadecimal fraction to its decimal equivalent using the same technique as for integer numbers. Divide the results by 16^n (n is the number of fraction positions).

Example: $.8A7 = .540771_{10}$

$8A7_{16} = 2215_{10}$

$16^3 = 4096$

$$4096 \overline{)2215.000000}\quad .540771$$

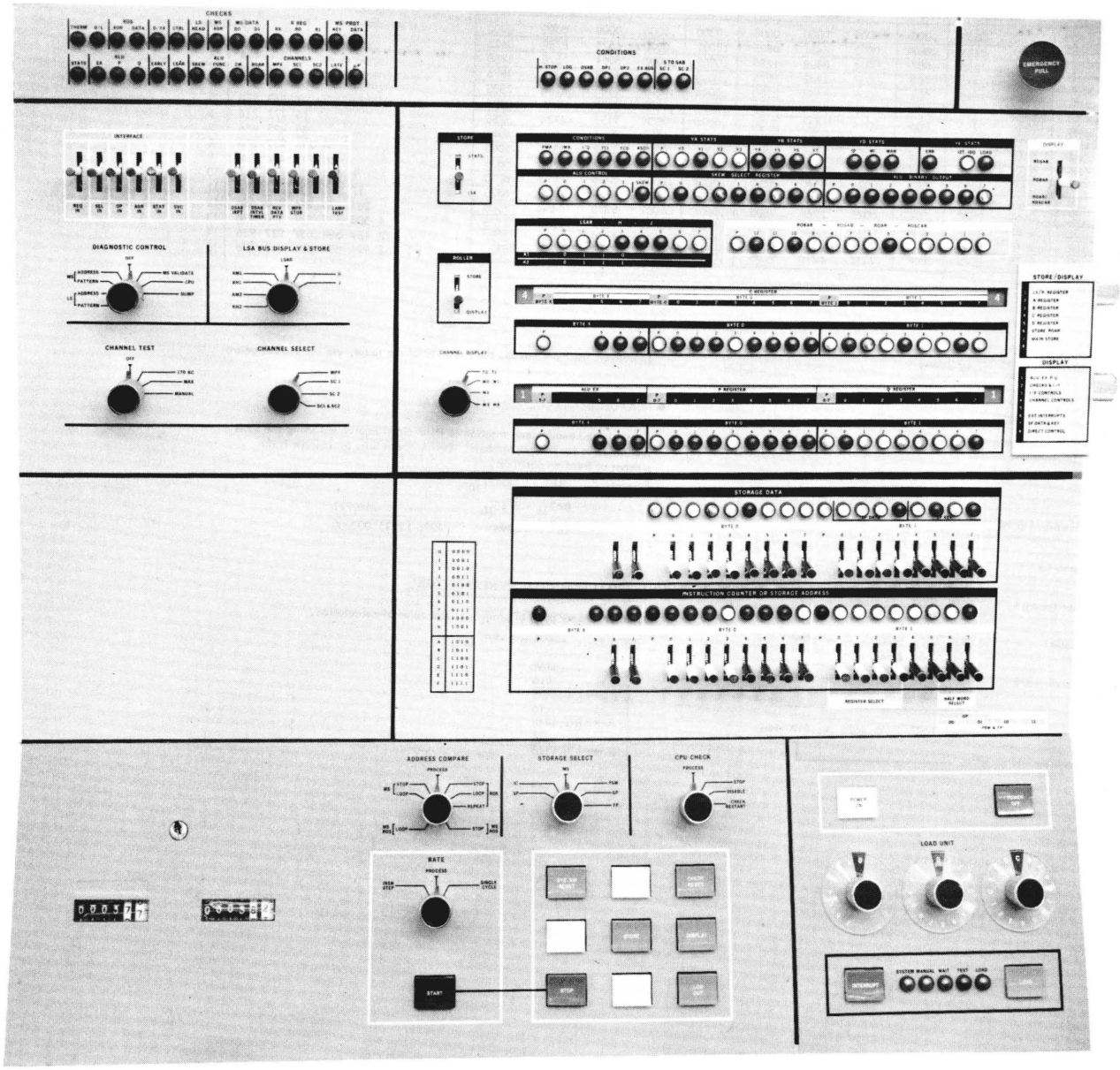
● DECIMAL FRACTION TO HEXADECIMAL

Collect integer parts of product in the order of calculation.

Example: $.5408_{10} = .8A7_{16}$

.5408
x16
8 ← [8].6528
x16
A ← [10].4448
x16
7 ← [7].1168

APPENDIX B: IBM 2040 SYSTEM CONTROL PANELS



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