IBM Maintenance Library

3830 Storage Control, Model 2

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SAFETY

Be constantly aware of hazardous situations when working on the 3830-2 Storage Control. Take time to review the CE safety practices listed below which have been reprinted from the pocket-size card available from Mechanicsburg (Order No. S229-1264).

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power, ac and dc, when removing or assembling major components, working in immediate areas of power supplies, performing mechanical inspection of power supplies, or installing changes in machine circuitry.
3. After turning off wall box power switch, lock it in the Off position or tag it with a "Do Not Operate" tag, Form 229-1266. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, observe the following precautions:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Do not wear rings, wrist watches, chains, bracelets, or metal cuff links.
   c. Use only insulated pliers and screwdrivers.
   d. Keep one hand in pocket.
   e. When using test instruments, be certain that controls are set correctly and that insulated probes of proper capacity are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc.). Use suitable rubber mats, purchased locally if necessary.
5. Wear safety glasses when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power or hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Cleaning parts with solvents, sprays, cleaners, chemicals, etc.
   f. Performing any other work that may be hazardous to your eyes. REMEMBER – THEY ARE YOUR EYES.
6. Follow special safety instructions when performing specialized tasks, such as handling cathode ray tubes and extremely high voltages. These instructions are outlined in CEMs and the safety portion of the maintenance manuals.
7. Do not use solvents, chemicals, greases, or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles – this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. After maintenance, restore all safety devices, such as guards, shields, signs, and grounding wires.
12. Each Customer Engineer is responsible to be certain that no action on his part renders products unsafe or exposes customer personnel to hazards.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. Ensure that all machine covers are in place before returning machine to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it; for example, under desk or table.
16. Avoid touching moving mechanical parts when lubricating, checking for play, etc.
17. When using stroboscope, do not touch ANYTHING – it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CEs and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machine while performing and after completing maintenance.

Knowing safety rules is not enough.
An unsafe act will inevitably lead to an accident.
Use good judgment - eliminate unsafe acts.

ARTIFICIAL RESPIRATION

General Considerations

1. Start Immediately – Seconds Count
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim, or apply stimulants.
2. Check Mouth for Obstructions
   Remove foreign objects. Pull tongue forward.
3. Loosen Clothing – Keep Victim Warm
   Take care of these items after victim is breathing by himself or when help is available.
4. Remain in Position
   After victim revives, be ready to resume respiration if necessary.
5. Call a Doctor
   Have someone summon medical aid.
6. Don't Give Up
   Continue without interruption until victim is breathing without help or is certainly dead.

Rescue Breathing for Adults

1. Place victim on his back immediately.
2. Clear throat of water, food, or foreign matter.
3. Tilt head back to open air passage.
4. Lift jaw up to keep tongue out of air passage.
5. Pinch nostrils to prevent air leakage when you blow.
6. Blow until you see chest rise.
7. Remove your lips and allow lungs to empty.
8. Listen for snoring and gurglings – signs of throat obstruction.
9. Repeat mouth to mouth breathing 10-20 times a minute. Continue rescue breathing until victim breathes for himself.

Thumb and finger positions

Final mouth-to-mouth position

CE-MLM Feedback forms are provided at the front of Volume R01 for reader comments. If the forms have been removed, send your comments to the address below.

This manual was prepared by the IBM General Products Division, Product Publications, Department G24, San Jose, California 95193.

CONTENTS

OLT

ONLINE TESTS -- RUNNING REFRESHER (Part 1 of 2)

Refer to OLT 25 for detailed running procedure.

OLTSEP

Preparation

Mount OLTSEP pack or tape and IPL.

Starting OLTSEP

OLTSEP will print:

```
04 SEP188D ENTER DATE (AND TIME)
   'MM/DD/YY,HH/MM/SS'
```

Your reply is:

```
r 04,'xx/xx/xx,hh/mm/ss'
```

OLTSEP will print:

```
04 SEP102I OLTS RUNNING
04 SEP107I OPTIONS ARE NTL,      X
   NEL,EP,CP,NPP,PR,FE,NMI,SI
01 SEP105D ENTER DEV/TEST/OPT
```

To run OLTS from card decks, the RDR (reader) device must be varied from its default of disk or tape to card. To do this, reply:

```
r 01,'VARY RDR=00C'
```

'00C' is the address of the card reader. Modify the address to conform to your system. OLTSEP will print:

```
01 SEP219I VARY COMPLETE
01 SEP105D ENTER DEV/TEST/OPT
```

If the RDR device is to remain on the disk or tape, do not reply with the Vary command.

Making a Run Request

Make a run request to select the test you want to run.

Note: OLTs 3830 AAA and AAB must be selected. You cannot enter /3830//.

Your reply is:

```
r 01,'160/3830AAA//'
```

This reply will begin testing on device 160. Run OLT test AAA and use the default options. To select some other sequence of testing, enter a reply of:

```
r 01,'160/3830AAA,7/MI,NFE'/'
```

This will run only routine 7 of the control unit online tests, and will cause all the default options to be selected except the option FE (first error communications), which will be altered to NFE and NMI (no manual intervention), which will be altered to MI.

Note: See OS-OLTEP paragraph "Make a Run Request" for additional examples.

OLTSEP *(Continued)*

Options

Option	Yes	No	Default
Test Loop	TL (Value)	NTL	NTL
Error Loop	EL		
	EL (I)		
	EL (Value)	NEL	NEL
Error Print	EP	NEP	EP
Control Print	CP	NCP	CP
Parallel Print	PP (Value)	NPP	NPP
Print	PR	NPR	PR
First Error Comm.	FE	NFE	FE
Manual Intervention	MI	NMI	NMI
Spurious Interrupt	SI	NSI	SI
Data Entry Field	EXT=(Data)	—	—
Remote FE Control	RE	NRE	NRE

The RE option is only recognized if the RETAIN interface has been activated. ('REI' was entered in response to the SEP105D message.)

Halting OLTSEP

To halt OLTSEP at any time, press Request key on the console. OLTSEP will print:

```
04 SEP 107I OPTIONS ARE --------
01 SEP105D ENTER DEV/TEST/OPT
```

Your reply is:

```
r 01,'(new device)/(new test)/
      (new options)/'
```
New instructions to OLTSEP

or:

(EOB) To continue

or:

```
r 01,'///'
```
To continue or restart the section under test.

or:

```
r 01,'cancel'
```
To terminate the section under test.

Note: See OLTSEP Guide (D99-SEPDT) for detail.

OS–OLTEP

Preparation

Units to be tested must be varied offline. This is accomplished through the console by using the Vary command. Examples:

```
V 160,OFFLINE
```
(will vary unit 160 offline)

```
V (160,161,162),OFFLINE
```
(will vary units 160, 161, and 162 offline. The system will reply `160 OFFLINE` when the vary is completed.)

Note: SYSRES cannot be varied offline.

It is important that you vary the units to be used offline prior to starting OS–OLTEP. If you decide to test another unit after OS–OLTEP has started, type in the Vary Offline command; then:

1. If running under MVT, type in `S INIT`, and after the initiator is started, type in `P INIT`. This causes an initiator to start and stop and varies the unit offline.

2. If running under MFT, type in `C OLTEP`. After OS–OLTEP is cancelled, type in `S OLTEP.PX`. This cancels and restarts OS–OLTEP and varies the unit offline.

Starting OS–OLTEP

S – causes a job to be started if a reader procedure is incorporated in your system. Examples:

`S OLTEP`	(for an MVT system)
`S OLTEP.PX`	(for an MFT system – where X is the partition number OLTEP is to run in. If in doubt, ask an operator which partition to use.) OR - (Use JCL on cards to execute program IFDOLT.)

Once OS–OLTEP is running, it generates various messages. These can be found in the Messages and Completion Codes SRL. Here are a few examples:

```
IFD102I  OLTS RUNNING
```
(To inform you that OS–OLTEP is running.)

```
00  IFD104E  TO FORCE COMMUNICATION
             WITH OLTEP EXECUTIVE,
             ENTER ANY CHARACTER
```
(A reply of any character will cause the test to stop at this point. Message IFD105D will then be presented.

OS–OLTEP *(Continued)*

Making a Run Request

OS–OLTEP will wait for a reply after issuing this message:

```
01 IFD105D ENTER-DEV/TEST/
   OPT/
```

Example of DEV/TEST/OPT/reply:

```
r 01,'160/3830AAA//'
```

Options

Use the Options chart from OLTSEP paragraph.

Halting OS–OLTEP

Reply to message '00' with any character to force communications. OS–OLTEP will print:

```
01 IFD105D ENTER -- DEV/
   TEST/OPT/
```

You will reply:

```
r 01,'cancel'
```
(This will cancel OS–OLTEP.)

Or press Request on the console, then enter:

```
C OLTEP
```
This will also cancel OLTEP.

Note: See OS/OLTEP SRL (Order No. GC28-6650) for details and procedures.

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437402A	437403	437404	437405	437408	437413	437414
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ONLINE TESTS – RUNNING REFRESHER (Part 2 of 2)

DOS–OLTEP

Preparation

Units to be tested must not be assigned to either of the foreground programs. The background program must be available for CE use.

Starting DOS–OLTEP

You may put job control cards in the reader or you may enter JCL commands from the system console. The example shown is for the console. Underlined characters are entered by the CE.

```
AR START BG
BG // JOB TEST 3830 MOD2
BG // ASSGN SYS014,X'160'
BG // EXEC IJZADOLT
BG E102I OLTS RUNNING
BG E107I OPTIONS ARE-NTL,NEL,NPP,     X
   FE,NMI,EP,CP,PR,NRE,NTR
BG 01E105D ENTER--DEV/TEST/OPT/
```

Note: This will be printed after the first error, after pressing the interrupt key, or at job completion.

Making a Run Request (Reply to E005D)

```
BG r 01,'160/3830AAA//'
```
(Test 160 with 3830AAA)

```
BG E158I S T3830AAA $ UNIT 0160
```
(Testing has begun)

Option Field Entries

Use the Options chart from OLTSEP paragraph on OLT 10.

Halting DOS–OLTEP

To halt DOS–OLTEP at any time, press the CPU/INTERRUPT button. DOS–OLTEP will print:

```
BG 01E105D ENTER--DEV/TEST/OPT/
BG r 01,'cancel'
```

DOS–OLTEP will be cancelled and the background program will again be available to the customer.

Note: See DOS/OLTEP SRL (Order No. GC24-5086) for details.

OLT PREREQUISITES

The 3830-2 online tests verify that:

- CPU can communicate with the control unit (CU).
- All tag and bus lines between the CU and channel are operational.
- Channel interface logic in the CU is operational.
- Identity of 23FD disk is correct.

Complete test descriptions are found on OLT 25, 30.

PROGRAM REQUIREMENTS

All documentation in this OLT section applies only to OLTs 3830AAA and 3830AAB at Version 2, Level 0 (PID release 5.0). These OLTs require a 3830-2 CU diagnostic disk at EC 437418 or higher. The control program used must be at the level specified below:

OLTSEP 8.0 or higher
OS/OLTEP 21.7 or higher
DOS/OLTEP 29.0 or higher
VS1/OLTEP 2.6 or higher
VS2/OLTEP 2.0 or higher

OLTEP requires a system or private library containing:
Configuration data set (CDS)
OLT sections T3830AAA and AAB

OLTSEP requires a load tape or disk load file containing:
IPL loader
OLTSEP nucleus
OLTSEP transient modules
SOSP
Configuration data set
OLT sections T3830AAA and AAB

EQUIPMENT REQUIREMENTS

3830-2 Storage Control
or
Integrated Storage Control (ISC) for 3145, 3158, or 3168
3830 Diagnostic 23FD disk

DEVICE CONFIGURATION DATA SET ENTRY

Configuration data must be correctly supplied for the unit addresses to be entered at dev/test/opt time as follows (one card per unit address plus one card per 3830 control unit).

Card Column	Enter
1	Blank
2–4	CDS
5–9	Blank
10–17	Device address (example: 00000160)
18–19	Model code (02)
20–21	Feature code (02)
22–23	Class (20)
24–25	Type 09 – 3333/3330 Mod 1, 2* Type 0A – 3340/3344 Type 0B – 3350* Type 0D – 3333 Mod 11/3330 Mod 11*
26–29	Blank
30–31	04 = Two Channel Switch or Two Channel Switch, Additional
flags	40 = Shared (either by string or channel) 44 = Both of above
32–35	Blank
36–37	Suffix to identify control unit CDS. This field must match card columns 42 and 43 in the CU 3830 CDS card that defines the control unit through which this unit address is accessed.
38	Enter a slash (/) to indicate end of CDS entry

*If in compatability mode, punch card for compatability type. For example, for 3330-11 compatability, punch 0D.

CDS must include entries for each device on your system. (See *CDS Guide,* D99-CDSGA.) Devices accessible via Two-Channel Switch, Two Channel Switch Additional, or String Switch will have more than one CDS entry per device.

3830 CU CONFIGURATION DATA SET ENTRY

When T3830AAA is running, control unit CDS information is used to:

1. Tell the CE which unit addresses must be made unusable to the system; *e.g.,* vary offline (OS), unassign (DOS).
2. Test the CU device address register.

Card Column	Enter
5–29	Unused – leave blank
30	Flags code – 4 if control unit is shared with another system, otherwise leave blank.
31	Flags code ('8') – indicates symbolic CDS name in card columns 36–43
32–35	Blank
36–41	Symbolic CDS name prefix – CU3830
42–43	Symbolic CDS name prefix – this field must match card columns 36–37 in all device CDS cards that define unit addresses that are accessible through the control unit described by this card.
44–71	Unit address extent blocks. These describe unit addresses accessible through this control unit. Unit addresses for each channel interface on this system must be provided. Use device addresses accessible by only one system. DO NOT use device addresses of systems sharing this CU or controller. Format (repeated for each set of contiguous unit addresses): a. An even number of blank card columns (*e.g.,* 2, 4, 6) may be used to separate blocks. b. Two card columns that indicate, in hexadecimal, the number of contiguous unit addresses (01 through 20) defined by this block. c. Four card columns containing the lowest unit address defined by this block (right-justified). *Examples:* 040130 (defines 130, 131, 132 and 133) 020120 020130 (defines 120, 121, 130 and 131) 020120 020320 (defines 120, 121, 320 and 321)
72	Continuation character when continuation card is required. Refer to Section 3 of *CDS Guide,* D99-CDSGA, for continuation card layout. Slash (/) must appear after all unit address extent blocks have been defined.

STANDALONE/ONLINE SUPPORT PROGRAM

The standalone/online support program (SOSP) is used to build CDS, add or update OLTs, *etc.* See *SOSP Operators Guide* (D99-SOSPB).

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See EC History	437416 11 Jan 74	447460 19 Dec 75	447461 12 Mar 76			

ONLINE TEST DESCRIPTION (Part 2 of 2)

SECTION ID T3830AAA *(Continued)*

Running *(Continued)*

7. Place the Operation Mode switch in Forced Logging position. Other positions will result in false check-1 errors.
8. Place the Enter/Display switch in Program Data Entry position.
9. Select OLT T3830AAA – 'xxx/3830AA/ /', where xxx can be any unit normally addressable by the channel/CU path under test. With 32 Drive Expansion feature, use only base (even) CU path.

   Note: ***The OLTSEP Device Address cannot be used in the device field (xxx).***
10. When OLT(S)EP indicates "DEVICE NOT OPERATIONAL CC=3," enable the CU/channel interface to be tested and reply "p" to cause the OLT to proceed.
11. If an error occurs, the error code should be displayed in the CU CE panel Address/Check/Program Display lamps. See OLT 50 for error display codes and related control storage locations.
12. Upon successful completion, perform IMPL of the functional microprogram disk and restore the 3830(s) and the drives to normal operation.

SECTION ID T3830AAB

Routine

Allows identification of any 23FD disk by:

Date	Device controlled
Part number	Feature
E/C number	

Running

1. Insert 23FD disk to be verified into 23FD file for the control unit.
2. Select OLT 3830AAB, 'xxx/3830AAB/NFE/', where xxx can be any device address. No reading or writing will be performed on this device.
3. When OLT terminates, see identification information on output device.

SECTION ID T3830AAC (Tracer Dumper Formatter)

Note: *Before running this OLT, the Tracer Dumper micro (routine 90) must be run.*

Run Instructions

1. Vary a device on the controller that is running the trace offline.
2. Select OLT T3830AAC:
   R01,'XXX/3830AAC/NFE/'
   (Where XXX is the device varied offline.) See OLT 10 for additional run instructions.
3. If any console error messages are printed, see OLT 250 for the message description.
4. The formatted trace is printed on the printer.

Formatted Output

FORMATTED TRACE

See OLT 42 for a description and example of the formatted trace.

DISPLACEMENT TABLE

Use the reference pages in Figure 1 to correlate the displacement to the microcode storage dump area for all functional microcode disks except for disks with P/Ns 4168811 and 4168816. For disk P/N 4168811, see microfiche page QA032, P/N 4168831; and for disk P/N 4168816, see microfiche page QA032, P/N 4168836.

ZERO BOUNDARY WORDS

Use the reference pages in Figure 1 for all functional microcode disks except for disks with P/Ns 4168811 and 4168816. For disk P/N 4168811, see microfiche page QA032, P/N 4168831; and for disk P/N 4168816, see microfiche page QA032, P/N 4168836.

Figure 1. Dump Data Storage Area

Displacement (Hex)	Number of Bytes	Control Storage Addresses	Contents	Page Reference
0000	256	0200-02FF	Usage/error records	CTLR 650
0100	256	0300-03FF		
0200	256	0400-04FF	CHL-I Trace	OLT 42
0300	256	0500-05FF	CTL-I Trace	
0400	256	0600-06FF	Working Storage	CTLR 650
0500	256	0000...xx00...3F0C	Zero Boundary words	CTLR 652

Upon entering the dumper (3C3C), the contents of the storage control unit registers are saved in control storage as follows:

Displacement (Hex)	Register	Displacement (Hex)	Register	Displacement (Hex)	Register
04E0	ND	04E9	TA	04F3	TG
04E1	NC	04EA	TD	05F0	SA
04E2	NB	04EB	MA	05F1	SB
04E3	TC	04EC	MD	05F2	SC
04E4	GB	04ED	GC	05F3	SD
04E5	GA	04EE	BR	05F4	GE
04E6	TB	04EF	MC	05F5	NE
04E7	NA	04F1	ST	05F6	TE
04E8	MB	04F2	GD	05F7	ME

ONLINE TEST DESCRIPTION

FORMATTED TRACE OUTPUT

1 Channel Interface Tracer

The channel interface tracer stores a word in the channel trace table every time the storage control unit attempts to present status to the channel, except for zero initial status.

Each entry contains:

2 Channel the trace is being run on.

3 Address of the controller and device.
- Bits 3–4 Logical controller address
- Bits 5–7 Logical device address

4 Channel Command is the last channel command before status is presented to the channel. Test I/O commands do not update this byte.

5 Unit Status presented to the channel. This does not indicate that the status was accepted by the channel.

6 ST–Register is a microcode register.

7 Controller Interface Tracer

The controller interface tracer stores a word in the controller trace table every time the storage control unit issues a tag to a controller or drive, except for the poll tag (82) in the idle wait loop.

8 Normally many control interface tags are expected for each channel interface trace entry. Due to the greater number of tag responses on the controller interface trace , in respect to the channel interface trace and the trace storage limitations to 64 lines for each trace, the earlier tag entrys from the controller interface are overlayed.

Each entry contains:

9 TD Register contents, CTL–I Bus Out

10 TA Register contents, CTL–I Tag Bus

11 Return address for the DCI Tag

12 13 The operations on the channel interface, such as in line 61 of the trace, correspond to the operations on the controller interface lines 61.01, 61.02, etc.

First Trace Entry

OLTSEP DATE=00/00/00 PAGE 0011 REL=9A

	1						7		
LINE #	CHANNEL 2	ADDR 3	CMD 4	STATUS 5	ST-REG 6	LINE # 8	TAG(TD) 9	BUS(TA) 10	RETURN 11
01.00	A	00	00	00	47				
02.00	A	00	00	00	47				
03.00	A	00	00	00	47				
60.00	A	00	04	0C	05				
						60.01	84	01	2A84
						60.02	8F	00	2ABC
						60.03	84	01	2A80
						60.13	04	10	2518
12 61.00	A	00	44	0C	05				
						61.01	84	01	2A84
						13 61.02	8F	00	2ABC
						61.03	84	01	2A80

Last Trace Entry

64.00	A	00	04	0C	05				
						64.01	84	01	2A84
						64.02	8F	00	2ABC
						64.03	84	01	2A80
						64.04	06	40	252C
						64.05	07	50	2AE0

ONLINE TESTS – ERROR MESSAGES

CU CHANNEL INTERFACE TEST (T3830AAA)

Note: CE panel Enter/Display switch must be in Program Data Entry/Display position. Read error message code in Address/Check/Program Display (A/C/PD) lamps.

Format for Error Codes Listed

A/C/PD Bits 0-7	
with A/C/PD bit 8 off	with A/C/PD bit 8 on
Bit 0 Command decode enabled 1 Not used 2 and 3 (00 channel A; 01 channel B; 10 channel C; 11 channel D) 4-7 Device address	**Bit** 0 Channel buffer parity check 1 Interface check channel A or C 2 Interface check channel B or D 3 Channel transfer check 4 CTL-I check 5 CTL-I load S register check 6 Compare assist check 7 Not used
A/C/PD Bits 8-15	If bit 8 is on, a check 2 was encountered with the error, and A/C/PD bits 0-7 contain the channel error byte (NA register), and storage position '1000' byte 3 contains the CTL-I error byte (ND register).
A/C/PD Lamps Ripple	If A/C/PD lamps ripple, turn off Multitag switch. If lamps continue to ripple, the Multitag switch is failing to disconnect.
A/C/PD Lamps Fail to Ripple	If the command decode is enabled, the A/C/PD lamps should ripple as long as the Multitag switch is on. If the Multitag switch is off, the lamps should stop rippling.

Error Codes Displayed in A/C/PD Lamps

A/C/PD Bits 8-15	Meaning
x000 0000	Address Out placed bad parity on bus out. CU storage location '1201' contains the address byte received.
x000 0100	SELTD was detected, then ADDRO was tested and found down. It should be up.
x000 0110	COMMO or HLTIO failed to come up.
x000 1000	Command Out placed bad parity on bus out (BOPAR). CU storage location '1203' contains the command byte received.
x000 1010	COMMO failed to drop after address in was dropped.
x000 1110	A command, other than the special OLT command set, has been issued.
x000 1111	Neither SERVO nor COMMO was received in response to Status In.
x001 0000	Received both SERVO and COMMO responses to Status In.
x001 0010	Request In was raised. This should raise SELTD. SELTD failed to raise.
x001 0100	Request In was raised. The CU selected and raised Op In and Address In with its CU address on bus in. The channel should have responded with Command Out but Command Out was not received.
x001 0110	XFER was checked and found up when it should be down. The channel transfer hardware is in neither Read nor Write mode.
x001 1000	BFRDY was checked and found up when it should be down. The channel transfer hardware is in neither Read nor Write mode.
x001 1010	During a Write data transfer, XFER failed to come up.
x001 1100	During a Write data transfer, BFRDY failed to come up.
x001 1110	During a Write data transfer, a bus out parity error (BOPAR) was detected. CU storage locations '1400' and '1401' contain the received data bytes. ('1400' = first byte of 2-byte XFER; '1401' = second or single byte.)
x010 0000	At the start of a Read operation, XFER should be up. When tested, it was found to be down.
x010 0010	At the start of a Read operation, BFRDY should be up. When tested, it was found to be down.
x010 0100	During a 2-byte Read data transfer, XFER failed to come up after the first byte was transferred.
x010 0110	During a Read operation, BFRDY failed to come up after all read data was transferred.
x010 1000	During a 256-byte Write data transfer, an unexpected Command Out was detected.
x010 1010	During a 256-byte transfer Read or Write, XFER failed to come up.
x010 1100	During a 256-byte Write, a bus out parity error (BOPAR) was detected. CU storage location '1400' contains the data byte expected and location '1401' contains the data byte received.
x010 1110	During a 256-byte Write data transfer, the data expected did not compare to the data received. CU storage location '1400' contains the byte expected, and location '1401' contains the byte received.
x011 0000	During a 256-byte Read operation, BFRDY should come up. When checked, it was found down.
x011 0010	During a Sense command, BFRDY failed to come up after the data was transferred.
x011 1011	Busy was not detected during the test for busy.

Control Storage Location

CONTROL STORAGE LOCATION '1000' CONTAINS:

Byte 0
Bit
0 Diagnostic command decoded
1 Not used
2-3 00 channel A; 01 channel B; 10 channel C; 11 channel D
4-7 Device address

Byte 1 Error code

Byte 2
Bit
0 Channel buffer parity check
1 Interface check channel A/C
2 Interface check channel B/D
3 Channel transfer check
4 CTL-I check
5 CTL-I load S register check
6 Compare assist check
7 Interface check C/D or multiconnect error

Byte 3
Bit
0 Controller check
1 Select active or select check
2 CTL-I buffer (CTL-I bus in) parity check
3 Unexpected end check
4 CTL-I tag bus parity check
5 CTL-I bus out parity check
6 CTL-I transfer error
7 Unused

CONTROL STORAGE LOCATION '1200' CONTAINS:

Byte 0 Error code at Address Out time
Byte 1 Received address
Byte 2 Error code at Command Out time
Byte 3 Received command

CONTROL STORAGE LOCATION '1400' CONTAINS:

Byte 0 The first byte from a 2-byte write transfer or the expected data during a 256-byte write operation
Byte 1 The second byte from a 2-byte write transfer, the received data from a single byte write, or the last received data byte from a 256-byte write operation
Byte 2 Used to store:
1. The data byte ('D9' or 'DA') for use in routine 0B (Mark In test). 'DA' indicates CU retry successful.
2. The data byte ('00' or 'D5') for use in routine 7 (CU busy). 'D5' indicates CU (short) busy occurred.

Byte 3 Not used

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
OLTSEP	SEP125I SEP137I SEP137I SEP139D	UNREADABLE LABEL ON xxxx CSW xxxxxxxxxxxxxxxx SNS xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx REPLY B TO BYPASS, R TO RETRY, P TO PROCEED	These messages are presented by OLT(S)EP when IMPL of the CU diagnostic disk is successfully completed prior to starting 3830AAA. This message will occur because the commands used by OLT(S)EP are not recognized by the microdiagnostic. OLTSEP may wait for approximately 30 seconds before presenting this message.	Reply p to start 3830AAA.
OS OLTEP	IFD125I IFD125I IFD125I IFD139D	UNREADABLE LABEL ON xxxxxxxx CSW xxxxxxxxxxxxxxxx SNS xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx REPLY B TO BYPASS, R TO RETRY, P TO PROCEED		
OLTSEP	SEP138I SEP139D	DEV xxxx NOT OPERATIONAL, CC=3 REPLY B TO BYPASS, R TO RETRY, P TO PROCEED	If the CU channel interface switch is disabled when starting 3830AAA, this message will be presented.	Enable the CU channel interface switch and reply p.
OS OLTEP	IFD138I IFD139D	DEVICE xxx NOT OPERATIONAL CC=3 REPLY B TO BYPASS, R TO RETRY, P TO PROCEED (MAY DESTROY DATA)		

T3830AAA ERROR MESSAGES (Part 1 of 14)

CU CHANNEL INTERFACE TEST

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAA	Any	ERROR CODE IS-xx	An unexpected error occurred, resulting in a Unit Check. A Sense ('C4') command successfully read the error code.	Refer to OLT 50 for definition of the error code.
3830AAA	Any Any Any Any	* ATTEMPT TO SENSE ERROR CODE FAILED XPTD CC-0 XPTD STATUS-0C00 RCVD CC-x • • • CHECK CU CE PANEL FOR ERROR CODE	An unexpected Unit Check previously occurred. When the OLT tried to sense the error code, the Sense command failed.	Refer to OLT 50 for information on obtaining the error code (for the sense error) from the CU CE panel.
3830AAA	Any	CHECK CU CE PANEL FOR ERROR CODE	An unexpected error occurred, resulting in a Unit Check. No attempt was made to sense the error code because data transfer had not yet been tested.	Refer to OLT 50 for information on obtaining the error code from the CU CE panel.
3830AAA	Any	RUN THE CHANNEL WRAP DIAGNOSTIC	This message is presented to direct the user to run the channel wrap diagnostic from the CU CE panel. This message is presented only if an error occurs.	Refer to MICRO 200 and perform the indicated task.
3830AAA	000	T3830AAA CANNOT RUN ON UNIT-xxxx. UNSUPPORTED DEV TYPE-tt	Unit address xxxx, entered at the OLT(S)EP "ENTER–DEV/TEST/OPT/" communications interval, is assigned to type code tt. Supported device types include the following: **Type** **Device** 09 3330 or 3333 0A 3340/3344 0B 3350 0D 3330 Mod 11/3333 Mod 11	1. Ensure that the specified unit address is correct. 2. If the right unit address was used, correct the CDS entry for that unit xxxx. Refer to OLT 20.

CU CHANNEL INTERFACE TEST

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAA	001 001 001	* WAIT TIMEOUT CONTROL UNIT=aacd ROUTINE-rr PASS-pp XPTD CC-x • • • • • • aacd = Unit address entered at OLT(S)EP DEV/TEST/OPT/ communications interval. aa = channel c = control unit d = device (not addressed) rr = OLT routine number. 00 = OLT initialization FF = OLT termination or cleanup See routine description on OLT 25. pp = Routines 01-0C are each exercised 255 times unless the EXT=option is used. This count is intended to indicate if a failure may be solid (PASS-01) or if it is intermittent. The pass count is not presented if the error did not occur in routines 01-0C, or if the EXT=I or N options were used.	Ending status was not received within 1 second from the time an I/O operation was started.	1. Check subsequent messages for additional details. For information about these messages, refer to OLT 100. 2. Run the channel wrap diagnostic. Refer to MICRO 200. 3. If channel wrap runs error free, run all channel diagnostics.
3830AAA	002	* CU CDS SUFFIX NOT IN CDS ENTRY FOR UNIT-xxxx	The CDS (configuration data set) entry for unit xxxx does not contain any information in card columns 36-37.	Correct the CDS entry for unit xxx. Refer to OLT 20.
3830AAA	003	* UNIT ADDRESSES NOT IN CDS ENTRY CU3830xx	The 3830 CDS (configuraiton data set) entry does not contain required unit address information.	Correct the CU3830xx CDS entry. Refer to OLT 20.
3830AAA	004	* TOO MANY UNIT ADDRESSES IN CDS ENTRY CU3830xx	One of the following conditions has been detected: 1. More than 32 unit addresses were specified in a unit address block. 2. More than 128 unit addresses were specified in the CDS entry.	

T3830AAA ERROR MESSAGES (Part 3 of 14)

CU CHANNEL INTERFACE TEST

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAA	005 005 005 005 005 005 005 005	WARNING - SYSTEM REQUIRED VOLUMES MUST BE ACCESSIBLE THROUGH ANOTHER CONTROL UNIT NOT BEING TESTED UNIT ADDRESSES ACCESSIBLE BY THIS SYSTEM AND CU- xxxx xxxx • • • • • • ENTER P TO PROCEED, C TO CANCEL	**FORMAT 1 (OLTSEP/Unshared CU)** The OLTSEP pack must not be mounted on a drive accessible only through the CU to be tested. Subsequent actions block access to all indicated units (xxxx).	1. If the OLTSEP pack is mounted on one of the indicated units (xxxx), reply c; then do one of the following: a. If another 3830-2 or ISC is available, move the OLTSEP pack to a unit attached to it and re-IPL OLTSEP. b. Perform IPL of OLTSEP from another device type. Refer to the SOSP Operator's Guide, D99-SOSPB, for information about building OLTSEP tape and disk systems. 2. If the OLTSEP pack is accessible through another control unit, reply p.
3830AAA	005 005 005 005 005 005 005 005 005 005	WARNING - SYSTEM REQUIRED VOLUMES MUST BE ACCESSIBLE THROUGH ANOTHER CONTROL UNIT NOT BEING TESTED THIS CONTROL UNIT (aacd) MUST BE VARIED OFF-LINE (OS) OR PHYSICALLY UNASSIGNED (DOS DVCDN) IN ALL SYSTEMS SHARING THIS CU UNIT ADDRESSES ACCESSIBLE BY THIS SYSTEM AND CU- xxxx xxxx • • • ENTER P TO PROCEED, C TO CANCEL *See REFNUM 001 for explanation of control unit address (aacd).*	**FORMAT 2 (OLTSEP/Shared CU)** If packs required for the operation of a sharing system are accessible only through the control unit under test, either those packs will have to be moved to another subsystem, or that system will have to be brought down in order to test.	1. If a sharing system is using OS, use the Vary command to place the indicated units in an offline status on that system. 2. If a sharing system is using DOS, use the DVCDN command to unassign the indicated physical units from that system. 3. If actions 1 and/or 2 are successfully completed, reply p. If unsuccessful, reply c. *Note: Sharing systems may use different unit addresses for these devices.*
3830AAA	005 005 005 005 005 005 005 005 005	WARNING - SYSTEM REQUIRED VOLUMES MUST BE ACCESSIBLE THROUGH ANOTHER CONTROL UNIT NOT BEING TESTED THIS CONTROL UNIT (aacd) MUST BE VARIED OFF-LINE UNIT ADDRESSES ACCESSIBLE BY THIS SYSTEM AND CU- xxxx xxxx • • • ENTER P TO PROCEED, C TO CANCEL *See REFNUM 001 for explanation of control unit address (aacd).*	**FORMAT 3 (OS-OLTEP/Unshared CU)** Packs required for the operation of OS must not be mounted on a drive accessible only through the CU to be tested. Subsequent actions block OS access to all indicated units.	1. Use the Vary command to place the indicated units in an offline status. Example: V (160,161) offline. 2. If action 1 is successful, reply p. 3. If action 1 is unsuccessful, reply c. To run this test, bring down OS and perform IPL of OLTSEP through another control unit.
3830AAA	005 005 005 005 005 005 005 005 005 005	WARNING - SYSTEM REQUIRED VOLUMES MUST BE ACCESSIBLE THROUGH ANOTHER CONTROL UNIT NOT BEING TESTED THIS CONTROL UNIT (aacd) MUST BE VARIED OFF-LINE AND BE EITHER VARIED OFF-LINE (OS) OR PHYSICALLY UNASSIGNED (DOS DVCDN) IN ALL SYSTEMS SHARING THIS CU UNIT ADDRESSES ACCESSIBLE BY THIS SYSTEM AND CU- xxxx xxxx • • • ENTER P TO PROCEED, C TO CANCEL *See REFNUM 001 for explanation of control unit address (aacd).*	**FORMAT 4 (OS-OLTEP/Shared CU)** Refer to Formats 3 and 2.	Refer to Formats 3 and 2.

CU CHANNEL INTERFACE TEST

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAA	005 005 005 005 005 005 005	WARNING - SYSTEM REQUIRED VOLUMES MUST BE ACCESSIBLE THROUGH ANOTHER CONTROL UNIT NOT BEING TESTED THIS CONTROL UNIT (aacd) MUST BE ASSGN'ED TO THE OLTEP PARTITION UNIT ADDRESSES ACCESSIBLE BY THIS SYSTEM AND CU- xxxx xxxx • • • ENTER P TO PROCEED, C TO CANCEL *See REFNUM 001 for explanation of control unit address (aacd).*	**FORMAT 5 (DOS-OLTEP/Unshared CU)** Packs required for the operation of DOS must not be mounted on a drive attached to the CU to be tested. Subsequent actions block DOS access to all indicated units.	1. Except for the ASSGN-designated unit used at OLTEP "ENTER–DEV/TEST/OPT/" time, the units listed must be unassigned using the DVCDN command. 2. If action 1 is successful, reply p. 3. If action 1 is unsuccessful, reply c. To run this test, bring down DOS and perform IPL of OLTSEP through another control unit.
3830AAA	005 005 005 005 005 005 005 005 005 005	WARNING - SYSTEM REQUIRED VOLUMES MUST BE ACCESSIBLE THROUGH ANOTHER CONTROL UNIT NOT BEING TESTED THIS CONTROL UNIT (aacd) MUST BE ASSGN'ED TO THE OLTEP PARTITION AND BE EITHER VARIED OFF-LINE (OS) OR PHYSICALLY UNASSIGNED (DOS DVCDN) IN ALL SYSTEMS SHARING THIS CU UNIT ADDRESSES ACCESSIBLE BY THIS SYSTEM AND CU- xxxx xxxx • • • ENTER P TO PROCEED, C TO CANCEL *See REFNUM 001 for explanation of control unit address (aacd).*	**FORMAT 6 (DOS-OLTEP/Shared CU)** Refer to Formats 5 and2	Refer to Formats 5 and 2.
3830AAA	006 006 006 006 006	DISABLE THE CU aacd MULTITAG SWITCH DO IMPL PROCEDURE WITH CU DIAGNOSTIC DISK PLACE CU OPERATION MODE SWITCH INTO FORCED LOGGING ENABLE THE CU aacd CHANNEL INTERFACE ENTER P TO PROCEED, C TO CANCEL *See REFNUM 001 for explanation of control unit address (aacd).*	At the completion of these actions: 1. Most of the CU not checked by the OLT will have been tested by microdiagnostic. 2. The Enter/Display switch on the CU CE panel should be in the Program Data Entry/Display position. 3. CU/channel interfaces not being tested should be disabled at the CU operator control panel.	1. If the CU has Two Channel Switch feature, turn off the Multitag switch. If no Two Channel Switch feature, this message will not be presented. 2. Go to START 25, entry A, and follow the IMPL procedure until it completes normally. (The CE panel displays C484). 3. Set the Operation Mode switch (CU CE panel) to the Forced Logging position. False check-1 errors may occur in other positions. 4. Enable the CU aacd channel interface to be rested (CU operator control panel).

T3830AAA ERROR MESSAGES (Part 5 of 14)

CU CHANNEL INTERFACE TEST

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAA	007 007 007 007	* ERROR DURING STEP TO VERIFY CU 23FD IMPL CONTROL UNIT-aacd ROUTINE-00 XPTD CC-1 XPTD STATUS-2C00 RCVD CC-x • • • • • • *See REFNUM 001 for explanation of control unit address (aacd).*	While attempting to determine if IMPL of the CU diagnostic disk had been accomplished, an immediate control command received unexpected results. The CU diagnostic presents CE, DE, UC status to all commands unless a Diagnostic command is received. Refer to REFNUM 008 for additional information.	1. Check subsequent REFNUM 007 messages for additional details of this error. For information about these messages, refer to OLT 100. 2. Ensure that all actions required by REFNUM 006 messages were completed. 3. If all REFNUM 006 requirements were met, run the channel wrap diagnostic. Refer to MICRO 200. 4. If channel wrap runs error free, run channel tests.
3830AAA	008 008 008 008	* ERROR DURING INITIAL SELECTION TEST CONTROL UNIT-aacd ROUTINE-01 PASS-pp XPTD CC-1 XPTD STATUS-2C00 RCVD CC-x • • • • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	The following channel/CU interface circuitry is checked: **Tags Out:** Hold | Op | Sel | Addr | Cmd **Tags In:** | Op | | Addr | Stat **Bus Out:** Unit address | Command 'C3' (Channel buffer A) **Bus In:** Unit address | Xptd stat '2C' (Channel buffer B)	Perform REFNUM 001 CE action.
3830AAA	009 009 009 009	* ERROR DURING POLLING SEQUENCE TEST CONTROL UNIT-aacd ROUTINE-02 PASS-pp XPTD CC-1 XPTD STATUS-0800 XPTD STATUS-0400 RCVD CC-x • • • • • • *See REFNUM 001 for explantion of control unit address, routine number, and pass count.*	The following channel/CU interface circuitry is checked: **Tags Out:** Hold | Op | Sel | Addr | Cmd **Tags In:** Req* | Op | | Addr | Stat *Some channels ignore Request In – they poll the units. **Bus Out:** Unit address | Command 'D3' **Bus In:** Unit address | Xptd stat* *Immediate CE status ('08') is posted. The CU polls to post DE status ('04').	1. Suspect polling sequence hardware in the control unit. 2. Perform REFNUM 001 CE action.

T3830AAA ERROR MESSAGES (Part 6 of 14)

CU CHANNEL INTERFACE TEST

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAA	010 010 010 010	* ERROR DURING ONE BYTE BUS-OUT DATA TEST CONTROL UNIT-aacd ROUTINE-03 PASS-pp XPTD CC-0 XPTD STATUS-0C00 RCVD CC-x • • • • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 1** The following channel/CU interface circuitry is checked: **Tags Out**: Hold | Op | Sel | Addr | Cmd | Serv **Tags In**: | Op | | Addr | Stat | **Bus Out**: Unit address | Command 'DF' | Service* **Bus In**: Unit address | Xptd stat '0C' | *'00', '4A', '7E', 'A1', or 'FF' Expected condition code (initial status) or ending status was not received in response to a 'DF' command.	1. Suspect Service Out circuitry. 2. Perform REFNUM 001 CE action.
3830AAA	010 010 010 010	* ERROR DURING ONE BYTE BUS-OUT DATA TEST CONTROL UNIT-aacd ROUTINE-03 PASS-pp XPTD DATA-xx RCVD DATA-rr • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 2 (Bus Out Data Error)** In addition to the channel/CU interface circuitry checked in Format 1, bus in data (data in tag) has also been transferred (command 'D6'). Channel buffer B is under control of Service In/ Service Out.	1. If RCVD data does not match XPTD data, suspect hot bits. 2. Run the channel wrap diagnostic. Refer to MICRO 200.
3830AAA	011 011 011 011	* ERROR DURING ONE BYTE BUS-IN DATA TEST CONTROL UNIT-aacd ROUTINE-03 PASS-pp XPTD CC-0 XPTD STATUS-0C00 RCVD CC-x • • • • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 1** The same channel/CU interface circuitry is checked as in REFNUM 010, Format 2.	Perform REFNUM 001 CE action.

T3830AAA ERROR MESSAGES (Part 7 of 14)

CU CHANNEL INTERFACE TEST

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAA	011 011 011 011	* ERROR DURING ONE BYTE BUS-IN DATA TEST CONTROL UNIT-aacd ROUTINE-03 PASS-pp XPTD DATA-xx RCVD DATA-xx • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 2 (Bus In Data Error)** The microprogram received the data it expected, but that same data was not read back by the OLT. Channel buffer A is under control of Data In/Data Out.	1. Suspect Data In circuitry. 2. Run the channel wrap diagnostic. Refer to MICRO 200.
3830AAA	012 012 012 012	* ERROR DURING TWO BYTE DATA TRANSFER (BUFFER) TEST CONTROL UNIT-aacd ROUTINE-04 PASS-pp XPTD CC-0 XPTD STATUS-0C00 RCVD CC-x • • • • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 1** The following channel/CU interface circuitry is checked: **Tags Out**: Hold | Op | Sel | Addr | Cmd | Serv 1 | Data 3 **Tags In**: | Op | | Addr | Stat | Serv 4 | Data 2 **Bus Out**: Unit address | Command 'C7' | Service* | Data* **Bus In**: Unit address | Xptd stat '0C' | | | **Bus Out**: Unit address | Command 'CE' | | | **Bus In**: Unit address | Xptd stat '0C' | Service* | Data* *'004A', '7EA1', 'FF00', '4A7E', 'A1FF' Expected condition code (initial status) or ending status was not received in response to either the C7 command or the CE command.	1. Suspect Data Out/Service In circuitry. 2. Perform REFNUM 001 CE action.
3830AAA	012 012 012 012	*ERROR DURING TWO BYTE DATA TRANSFER TEST CONTROL UNIT-aacd ROUTINE-04 PASS-pp XPTD DATA-xxxx RCVD DATA-xxxx • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 2** Channel buffer A is under control of Data In/Data Out. Channel buffer B is under control of Service In/Service Out.	1. Suspect Service In circuitry. 2. Run the channel wrap diagnostic. Refer to MICRO 200.

CU CHANNEL INTERFACE TEST

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAA	013 013 013 013	* ERROR DURING BUS-OUT 256 BIT COMB TEST. RESID-cccc CONTROL UNIT-aacd ROUTINE-05 PASS-pp XPTD CC-0 XPTD STATUS-0C00 RCVD CC-x • • • • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 1** Expected condition code (initial status) or ending status was not received in response to a 'D7' command. This command attempts to write 256 bytes to the CU. The data pattern consists of all hexadecimal codes 00-FF in ascending order. The CU microprogram will force an error if bus out does not contain expected data. cccc = the residual count received from the 'D7' command data transfer. If cccc is '0100', no data was written. If cccc is '0000', all 256 bytes were written unless channel error occurred. If cccc is not '0100', then '00FF' minus cccc will equal the bit pattern written when the failure occurred.	This format always precedes either a Format 2 REFNUM 013 message or a REFNUM 014 message. 1. If Format 2 follows this message, perform that CE Action. 2. If the indicated residual count is not '0100', calculate the failing bit pattern. Suspect bus out. 3. Perform REFNUM 001 CE Action.
3830AAA	013 013 013 013	* ERROR DURING BUS-OUT 256 BIT COMB TEST. RESID-cccc CONTROL UNIT-aacd ROUTINE-05 PASS-pp XPTD DATA-xx RCVD DATA-xx • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 2** Refer to Format 1 Diagnostic Information. When the value of the XPTD DATA is even (bit 7 is 0), channel buffer B was under control of Service Out/Data In. When the value of the XPTD DATA is odd (bit 7 is 1), channel buffer A was under control of Data Out/Service In. XPTD DATA = what CU expected RCVD DATA = what CU received	When this format appears, it is always preceded by Format 1. Run the channel wrap diagnostic. Refer to MICRO 200.
3830AAA	014 014 014 014	* ERROR READING BACK FAILING BUS-OUT DATA CONTROL UNIT-aacd ROUTINE-05 PASS-pp XPTD CC-0 XPTD STATUS-0C00 RCVD CC-x • • • • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	Expected condition code (initial status) or ending status was not received in response to a 'CE' command. This command was issued to read back the data the CU expected and received from the channel interface on a 'D7' command.	When this message appears, it is always preceded by a Format 1 REFNUM 013 message. Perform the CE Action indicated for that message.

T3830AAA ERROR MESSAGES (Part 9 of 14)

CU CHANNEL INTERFACE TEST

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAA	015 015 015 015	* ERROR DURING BUS-IN 256 BIT COMB TEST. RESID-cccc CONTROL UNIT-aacd ROUTINE-06 PASS-pp XPTD CC-0 XPTD STATUS-0C00 RCVD CC-x • • • • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 1** Expected condition code (initial status) or ending status was not received in response to a 'D2' command. This command attempts to read 256 bytes from the CU. The data pattern consists of all hexadecimal codes, 00-FF, in ascending order. cccc = The residual count received from the data transfer. If cccc is 0100, no data was read. If cccc is 0000, all 256 bytes were read unless a channel error occurred. If cccc is not 0100, then 00FF minus cccc will equal the bit pattern read when the failure occurred.	1. If the indicated residual count is not '0100', calculate the failing bit pattern. 2. Perform REFNUM 001 CE Action.
3830AAA	015 015 015 015	* ERROR DURING BUS-IN 256 BIT COMB TEST. CONTROL UNIT-aacd ROUTINE-06 PASS-pp XPTD DATA-xx RCVD DATA-xx • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 2** Refer to Format 1 Diagnostic Information. XPTD DATA = what OLT expected RCVD DATA = what OLT received	1. Suspect the failing data bits. 2. Run the channel wrap diagnostic. Refer to MICRO 200.
3830AAA	016 016 016 016	* ERROR DURING CONTROL UNIT BUSY TEST CONTROL UNIT-aacd ROUTINE-07 PASS-pp XPTD CC-x • • • RCVD CC-x • • • • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 1** Expected condition code (initial status) or ending status was not received in response to a 'DE' command.	1. Suspect Status Modifier and Busy status bit circuitry. 2. Perform REFNUM 001 CE Action.

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAA	016 016 016 016	* ERROR DURING CONTROL UNIT BUSY TEST CONTROL UNIT-aacd ROUTINE-07 PASS-pp XPTD DATA-D5 RCVD DATA-xx • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 2** Although expected results were received by the OLT, the CU diagnostic indicates the CU busy test failed. Under operating systems (OS and DOS), system retry of a CU busy is transparent to the OLT. To determine if this action successfully occurred, the CU diagnostic signals the OLT on every third 'DE' command, with 'D5' data, whenever the preceding command correctly responded to CU busy.	1. Suspect Status Modifier and Busy status bit circuitry. 2. Run the channel wrap diagnostic. Refer to MICRO 200.
3830AAA	017	RTN-xx BYPASSED. OLTSEP CNTRL MODE REQD	Either the OLT is running under an operation system OLTEP (OS or DOS), or the OLT is running under a standalone OLTEP (OLTSEP), but control mode is not available. Routine (xx) is skipped. The OLT proceeds to the next routine. **xx** **Test** 08 Halt device 09 Disconnect In tag 0A Device address register 0C Channel unshared UCW	If this routine must be run, bring down the operating system and perform IPL of OLTSEP through another control unit. Otherwise, no action is required.
3830AAA	018 018 018 018	* ERROR DURING HALT DEVICE TEST CONTROL UNIT-aacd ROUTINE-08 PASS-pp XPTD CC-1 XPTD STATUS-0000 RCVD CC-x • • • • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	Expected condition code or initial status was not received in response to the Halt Device instruction. The following channel/CU interface circuitry is checked: **Tags Out** Sup Hold Op Sel Addr **Tags In** Op Addr	1. Suspect Suppress Out tag circuitry. 2. Perform REFNUM 001 CE Action.
3830AAA	019 019 019 019	* ERROR READING HALT DEVICE COUNT CONTROL UNIT-aacd ROUTINE-08 PASS-pp XPTD CC-0 XPTD STATUS-0C00 RCVD CC-x • • • • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	Expected condition code (initial status) or ending status was not received in response to a 'D6' command. This command is issued once at the start of this routine and again after each Halt Device instruction. The purpose of the command is to read a value (provided by the CU diagnostic) indicating whether or not the Halt I/O latch set (CL bit 12).	Perform REFNUM 001 CE Action.

T3830AAA ERROR MESSAGES (Part 11 of 14)

CU CHANNEL INTERFACE TEST

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAA	020 020 020 020	* RECEIVED UNEXPECTED HALT DEVICE COUNT CONTROL UNIT-aacd ROUTINE-08 PASS-pp XPTD DATA-xx RCVD DATA-xx • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	Refer to REFNUM 019 Diagnostic Information.	1. Suspect Halt I/O latch and Suppress Out circuitry. 2. Run the channel wrap diagnostic. Refer to MICRO 200.
3830AAA	021 021 021 021	* ERROR DURING DISCONNECT-IN TAG TEST CONTROL UNIT-aacd ROUTINE-09 PASS-pp XPTD CC-1 XPTD STATUS-0C00 RCVD CC-x • • • • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count*	Expected condition code or initial status was not received in response to a 'CF' command. CU must be in forced logging mode. The following channel/CU interface circuitry is checked by forcing a check 1: **Tags Out**: Sup | Hold | Op | Sel | Addr | Cmd **Tags In**: Disc | | Op | | Addr | Stat	1. Suspect Disconnect In tag circuitry. 2. Suspect Selective Reset circuitry. 3. Perform REFNUM 001 CE Action.
3830AAA	022 022 022 022	* ERROR DURING DEVICE ADDRESS REG TEST CONTROL UNIT-aacd ROUTINE-0A PASS-pp XPTD CC-1 XPTD STATUS-xxxx XPTD STATUS-0002 RCVD CC-x • • • • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	The microprogram forces a check-1 error while Op In is down, causing Disconnect In to occur. As indicated in message REFNUM 006, the CU must be in Forced Logging mode. xxxx: 0C00 = diagnostic command C6 issued to force check-1 0002 = diagnostic command C6 issued to retrieve interface control check	1. Ensure that no other units on the channel under test were made ready or otherwise caused interrupts during this routine. 2. If the Disconnect In tag routine was successfully completed, suspect the device address register. 3. If the Disconnect In tag routine was not run successfully, perform REFNUM 021 CE Action. 4. Perform REFNUM 001 CE Action.
3830AAA	023	* PSW RECEIVED INCORRECT DEVICE ADDRESS REG VALUE-xxxx CONTROL UNIT-aacd ROUTINE-0A PASS-pp *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	The indicated VALUE-xxxx was received in the I/O OLD PSW. CONTROL UNIT-aacd was expected.	

CU CHANNEL INTERFACE TEST

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAA	024 024 024 024	* ERROR DURING MARK-IN TAG TEST CONTROL UNIT-aacd ROUTINE-0B PASS-pp XPTD CC-0 XPTD STATUS-0C00 RCVD CC-x • • • • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 1** Expected condition code (initial status) or ending status was not received in response to a 'C2' command, The following channel/CU interface circuitry is checked: **Tags Out** | | Hold | Op | Sel | Addr | Cmd | Serv **Tags In** | Mark | | Op | | Addr | Stat | Serv Status Modifier, Channel End, Device End and Unit Check ending status are presented with Mark 0 In. The channel should have retried the 'C2' command. Every other time, the CU presents CE, DE status.	1. Suspect Mark 0 In tag circuitry. 2. Suspect ending status presented with Mark 0 In. 3. Perform REFNUM 001 CE Action.
3830AAA	024 024 024 024	* ERROR DURING MARK-IN TAG TEST CONTROL UNIT-aacd ROUTINE-0B PASS-pp XPTD DATA-DA RCVD DATA-xx • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 2** CU retry is transparent to the CPU. The CU diagnostic signals the OLT on every other 'C2' command with 'DA' data, when CU retry was successfully performed.	1. Suspect Mark 0 In tag circuitry. 2. Run the channel wrap diagnostic. Refer to MICRO 200.
3830AAA	025 025 025 025	* ERROR DURING CHANNEL UNSHARED UCW TEST CONTROL UNIT-aacd ROUTINE-0C PASS-pp XPTD CC-1 XPTD STATUS-0800 RCVD CC-x. • • • • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 1** Command 'CB' was issued to cause posting of Channel End status. This test verifies unshared (block multiplex) channel operation.	1. This is a normal error message if channel UCW for device under test is plugged for shared (not block multiplex) operation, and should be ignored. 2. If unshared (block multiplex) operation is failing, check channel UCWs for correct unshared plugging for each device on this control unit. 3. Run channel wraparound diagnostic to verify correct CU operation. If no failures occur, refer to system/channel mailtenance procedures.
3830AAA	025 025 025 025	* ERROR DURING CHANNEL UNSHARED UCW TEST CONTROL UNIT-aacd ROUTINE-0C PASS-pp XPTD CC-1 XPTD STATUS-0C00 XPTD STATUS-0400 RCVD CC-x *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	**FORMAT 2** Command 'DB' was issued while Device End status was still outstanding for the previous 'CB' command.	

T3830AAA ERROR MESSAGES (Part 13 of 14)

CU CHANNEL INTERFACE TEST

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAA	026 026	DISABLE THE CU aacd CHANNEL INTERFACE SW ENTER P TO PROCEED, C TO CANCEL *See REFNUM 001 for explanation of control unit address (aacd).*	**FORMAT 1** Routine '0D' tests Select In tag circuitry and tests Metering Out, Clock Out, and Metering In circuitry.	1. If this test is to be bypassed, enter c to cancel. 2. If this test is to be run, disable the channel interface (CU aacd operator control panel). Enter p to run this test.
3830AAA	026 026 026 026	DISABLE THE CU aacd CHANNEL INTERFACE SW TURN ON CU MULTITAG SW. CU CE PANEL LIGHTS SHOULD RIPPLE. TURN OFF CU MULTITAG SW, THEN ENTER P TO PROCEED, C TO CANCEL *See REFNUM 001 for explanation of control unit address (aacd).*	**FORMAT 2** Refer to Format 1 Diagnostic Information. In addition, test the CU Multitag switch and associated circuitry. The CU CE panel lights should ripple whenever the Multitag switch is on.	1. If this test is to be bypassed, enter c to cancel. 2. If this test is to be run, disable the CU aacd channel interface. 3. If the Multitag circuitry is functioning properly, enter p to continue the test. 4. If the Multitag circuitry fails to function properly, make the necessary repairs; then rerun this test.
3830AAA	027 027 027 027	* ERROR WHILE TESTING CU METERING CONTROL UNIT-aacd ROUTINE-0D PASS-pp XPTD CC-x • • • RCVD CC-x • • • • • • *See REFNUM 001 for explanation of control unit address, routine number, and pass count.*	The following channel/CU interface circuitry is checked: **Tags Out**: Clock | Meter | Hold | Op | Sel | Addr | Cmd | Serv **Tags In**: | Meter | | Op | Sel | Addr | Stat | Serv The clock and meter tag circuitry is checked by issuing a 'C3', then a 'D4', command between the time the CU aacd Channel Enable/Disable switch is disabled and the time Clock Out is dropped. The 'D4' command causes the microprogram to allow interface disable.	1. If XPTD CC is 3 and RCVD CC is 1, ensure that the CU diagnostic disk matches the channel interface configuration (basic, Two Channel, etc.). 2. Ensure that the CU Channel Interface switch was disabled as instructed by REFNUM 026. 3. Suspect the following circuitry: a. Clock Out. b. Meter Out. c. Meter In. 4. Perform REFNUM 001 CE Action.
3830AAA	028	CLOCK-OUT TAG MOMENTARILY DROPPED TO ALLOW CU TO DISABLE	The CU/channel interface cannot disable until the Clock Out tag is dropped. This occurs whenever the system is either in a wait state or stopped. The CU Channel Interface switch has previously been disabled as instructed by message REFNUM 026. The OLT has previously issued command code 'D4' to tell the micro-diagnostic to allow the interface to disable when Clock Out drops.	None

CU CHANNEL INTERFACE TEST

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAA	029 029	ENABLE THE CU aacd CHANNEL INTERFACE SW, THEN ENTER P TO PROCEED, C TO CANCEL *See REFNUM 001 for explanation of control unit address (aacd).*	This message will appear only if message REFNUM 026 received a p reply.	Enable the CU aacd Channel Interface switch and reply p.
3830AAA	032	IMPL THE FUNCTIONAL MICROPROGRAM DISK IN CU-aacd *See REFNUM 001 for explanation of control unit address (aacd).*	The test has completed without detecting any errors.	Perform the indicated task.

READ FUNCTIONAL DISK

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAB	**CECOM**	READ 23FD DISK ***IBM CONFIDENTIAL COPYRIGHTED*** MOUNT DISK TO BE READ - DO NOT IMPL CE DISK - REPLY G/GO, T/TERM (EOB)		The CE may reply either G to continue and read the 23FD label, or T to terminate the test without reading the label.
3830AAB	**None**	DISK PART NUMBER xxxxxxx EC NUMBER eeeeeee DATE WRITTEN mm/dd/yy VERSION FEATURE CODE DEVICE TYPE dddd-d FEATURE ff----------ff	xxxxxxx — The disk part number. mm/dd/yy — Month, day, and year the disk was written. dddd-d — Can be any device type, or unknown device type code. ff--ff — The feature can be basic single-channel, Two Channel Switch feature, Two Channel Switch Additional feature, or feature unknown. *Note: Although some disks may operate with more than one feature, the disk indicates only one.*	
3830AAB	**None**	CASMIT TAPE FILE STATUS ss----------ss CASMIT TAPE DATE yy/ddd COMATS FORMAT DATE yy/ddd	ss--ss — The CASMIT file status can be current – no REAs, history-W/WO REAs, REA-current, – or status not readable. yy/ddd — This refers to the year and day for CASMIT tape date and COMATS format date.	
3830AAB	**00005**	ERROR ON DIAGNOSTIC LOAD CHAIN	Some status error occurred while trying to load the ID sector (x'80') from 23FD. See accompanying status and sense.	Go to FSI pages in MLM for fault symptom code defined in sense bytes.

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
3830AAC	A	Command reject received on both command 82 and command 44.	Tracer micro running (not in dump mode).	Put the tracer in dump mode (see MICRO 23), rerun OLT.
3830AAC	B	Condition Code 3 received on a SIO.	No path to the addressed controller/device.	Get a path to device and rerun OLT.
3830AAC	C	Busy was received as initial status to SIO 80 times.	Device is very busy.	Rerun OLT.
3830AAC	D	Unusual status received.	See printer output. Reference number can be 01 (failed on command 82) or 02 (failed on command 44).	1. Reference number = 01 Status = 0200 Sense = 40XX,XX,XX,XX,XX, ... Device not ready. Make device ready and rerun OLT. 2. Reference number = 02 Status = 0C40, residual count = 03F0. Tracer dumper micro not started. Run tracer dumper micro and rerun OLT. 3. Conditions other than 1 or 2 above. Check status and sense information for the cause of the problem and correct the problem. Rerun the OLT.

STANDARD ERROR NUMBERS (Part 1 of 2)

Nine (9) standard error numbers (reference numbers – REFNUM) have been reserved for errors encountered by the Start I/O routine used by the OLT sections. These error numbers are XX091 thru XX099, where XX is the routine number.

Sect. ID	REFNUM	Error Messages and Console Communications	Diagnostic Information	CE Action
TXXXXX	**XX091**	ENVIRONMENTAL ERROR	Some error occurred on a test CCW chain which established error logging mode or CU was in forced logging mode.	1. If the CU is in normal mode and this message appears intermittently, set the CU to CE Normal mode. 2. If the CU is in CE Normal and the error locks solid, analyze errors using fault symptom code from sense bytes (FSI 5).
TXXXXX	**XX092**	CHANNEL CHECK	This error message is printed out in the Start I/O subroutine when any channel checks are found in the CSW status. The test is terminated when channel checks are found.	Channel checks are probably not due to subsystem failure. Run CPU channel tests.
TXXXXX	**XX093**	WAIT TIMED OUT	This error message is printed out in the Start I/O subroutine when the test has timed out while waiting for ending status. The test is terminated when it times out.	Ending status not received from CCW chain printed with this message. Subsystem may have gone busy or not operational, which invalidates further testing. Look for messages to this effect following REFNUM 00093. If it is determined that the control unit is hung, the control unit must be reset prior to continuing the test.
TXXXXX	**XX094**	ERR ON SENSE	This error message is printed out in the Start I/O subroutine. When the sense is not posted, another Start I/O is tried.	1. If this failure persists 32 times, see REFNUM xx095. Continue running tests to determine if Sense I/O failure is intermittent or solid. 2. Run CU tests. 3. Run CPU channel test for Sense I/O.
TXXXXX	**XX095**	32 RETRIES	This message is printed prior to terminating a section if any of the following were received on Start I/O and retried 32 times: *CU Busy *Invalid Sense	1. Continue running tests to determine if Sense I/O failure is confined to this OLT. 2. Run CU tests. 3. Run CPU channel test for Sense I/O.
EXAMPLE		*T3830AABV/L 10 RTN 001 DEV 0160 REFNUM 00005 ERROR ON DIAGNOSTIC LOAD CHAIN CCW01 53 00B683 40 00 0001 CAW 0000B880 *CCW02 44 00B6AD 40 00 0200 XPTD CC 0 RCVD CC 0 XPTD CSW1 00 00B890 0C00 0001 *RCVD CSW1 00 00B890 0200 0001	This is an example of the error message output whenever a status error occurs. This message includes: An * Error message T3830AAB OLT ID V/L 10 OLT Version/Level RTN001 Routine in OLT DEV Device address against which OLT was run REFNUM Provides index into error dictionary (OLT section) First Line Name of test An * on CCW0Z Failing CCW An * on RCVD CSW Failing status	1. See REFNUM defined by going to OLT error dictionary (begins on OLT 100) and proceed, using diagnostic information and CE action. 2. Analyze errors, using Fault Symptom Code from sense bytes (FSI 5).

STANDARD ERROR NUMBERS (Part 2 of 2)

<table>
<tr><th>Sect. ID</th><th>REFNUM</th><th>Error Messages and Console Communications</th><th>Diagnostic Information</th><th>CE Action</th></tr>
<tr><td>TXXXXX</td><td>XX096</td><td>UNABLE TO ALLOCATE SPACE ON PACK</td><td>Status errors terminated Read Home Address chain (used to determine if track is OK for Write).</td><td></td></tr>
<tr><td>TXXXXX</td><td>XX099</td><td>ABTERM, RET CODE - xx RCVD FROM yyyyyyyy

Termination Code Table
<table><tr><th>Macro</th><th>Hex Code</th><th>Termination Reason</th><th>Macro</th><th>Hex Code</th><th>Termination Reason</th></tr><tr><td>ALLOCATE</td><td>04
08
0C
10</td><td>Module not available (D)
Device not in device entry list
Space allocated
Space not available (D)</td><td>GRAB</td><td>04
08

0C</td><td>Device not in device entry list
Entry list contains only one device
Device descriptors not available (C)</td></tr><tr><td>CECOM</td><td>04
08</td><td>Module not available (C, D)
Error executing module (C, D)</td><td></td><td></td><td></td></tr><tr><td>CONVERT</td><td>04
08</td><td>Module not available (D)
Error from EH conversion (O,D)</td><td>PLINK</td><td>04</td><td>Module not available (D)</td></tr><tr><td>DPRINT</td><td>04
08

0C</td><td>Module not available (D)
Error while putting out line of data (H)
Incomplete parameter list (O)</td><td>WAITIO</td><td>04
08
0C</td><td>Module not available (D)
Timed out (T)
Error – device not valid (O,C)</td></tr><tr><td>EXIO</td><td>04
08

0C</td><td>Module not available (D)
Device not available (C, D, T)
Device not primary or data protected (O, D)
Device busy (T)
File Protect Violate – try running OLT vs CE pack</td><td>$CUTEST</td><td>04
08</td><td>Module not available (C, H)
OS: Unit address not varied offline
DOS: Unit address not in OLTEP partition
OLTSEP: Unit address is OLTSEP device</td></tr></table></td><td>The OLT(s) error print module named yyyyyyyy returned to the OLT in use with an error (return code = xx, should be = 00).</td><td>1. Usually due to a failure in OLT(s) error print (unless EXIO or WAITIO is involved). Restart OLTEP or repeat IPL of OLTSEP.
2. Check the configuration data set (CDS) to ensure that it is correct for your system. Use SOSP list function to obtain configuration data.
3. Module not available (return code '04') from any request for a module means that:
a. OLT and OLT(s) error print are not at compatible levels. This is not an error, but probably a downlevel OLT(s) error print.
b. Module has been removed from OLT library.
c. Device may be shared. DIO will exhibit this. This is not an error.
4. Termination may be due to:
a. OLT (O).
b. OLT(s) error print driver (D).
c. Device under test (T) including channel and/or control unit.
d. Configuration data set not correct (C).
e. Hardware in use (H), including console, printer, etc.</td></tr>
<tr><td>TXXXXX</td><td>None</td><td>COND CODE = x, REPLY ANY CHAR TO RETRY</td><td>This message is output to the console to warn of catastrophic failure condition (code = 2 or 3). Usually, when the control unit goes Busy or Not Operational, further testing will be invalid. Determine if the subsystem is hung before continuing. A Halt I/O failed to clear the condition. After replying, the Start I/O will be retried once. A second failure causes the section to terminate. (See REFNUM xx099.)</td><td>1. Determine if the subsystem is hung before continuing.
2. See if CU is in normal idle loop. If not, go to FSIs. If normal, enter any character.</td></tr>
<tr><td>TXXXXX</td><td>None</td><td>INTERVENTION REQUIRED, REPLY ANY CHAR TO RETRY</td><td>After replying, the Start I/O will be retried once. A second failure will cause the section to terminate. (See REFNUM xx099.)</td><td>1. Determine cause of status then reply any character to retry.
2. Remove and reinsert logical address plug (LAP) on the selected file. This may clear the cause of the incorrect status.</td></tr>
</table>

CONTENTS

SENSE

*Exit 3830-2 14 Device MLX Chart

SENSE DATA SUMMARY – BYTES 0–7

BYTE	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	CONTROL STORE ADDRESS (hex)
0	Command Reject	Intervention Required	Chl Bus Out Parity	Equipment Check	Data Check	Overrun	See Device MLM*	See Device MLM*	0640
1	See Device MLM*	Invalid Trk Format	End of Cylinder	Unused	No Record Found	File Protected	Write Inhibited	Operation Incomplete	0641
2	See Device MLM*	Correctable	Unused	Environmental Data Present	See Device MLM*	See Device MLM*	See Device MLM*	See Device MLM*	0642
3	RESTART COMMAND (Provided only when byte 1 bit 7, Operation Incomplete, is active)								0643
4	PHYSICAL DRIVE IDENTIFICATION – See Device MLM*								0644
5	CYLINDER ADDRESS (low order) 128	64	32	16	8	4	2	1	0645
6	See Device MLM*								0646
7	FORMAT (bits 0-3 hex)				MESSAGE CODE (bits 4-7 hex)				0647

*Exit → 3830-2 (14) Device MLX Chart

Note: See Device MLM for sense data and/or messages for formats 1, 4, and 5*

SENSE BYTES 8-23 → To formats 2, 3, 6

MESSAGES →

MESSAGES, determined by format and message code (byte 7)

	FORMAT 0	FORMAT 2	FORMAT 3
0	No message	No message	No message
1	Invalid command		
2	Invalid sequence		
3	CCW count less than required	S-register load check	
4	Data value not as required	CTL-I registers valid	
5	Diagnostic Write command not permitted by file mask		
6	Channel discontinued retry operation		
7	Channel returned with incorrect retry CCW		
8	23FD not ready		
9	23FD permanent seek check		
A	23FD permanent read check		
B	↑		
C			
D	Device dependent (see descriptions on SENSE 40)		
E	↓		
F			
	FORMAT 0	FORMAT 2	FORMAT 3

SENSE DATA SUMMARY – FORMAT 2 (SCU ERROR) SENSE 15

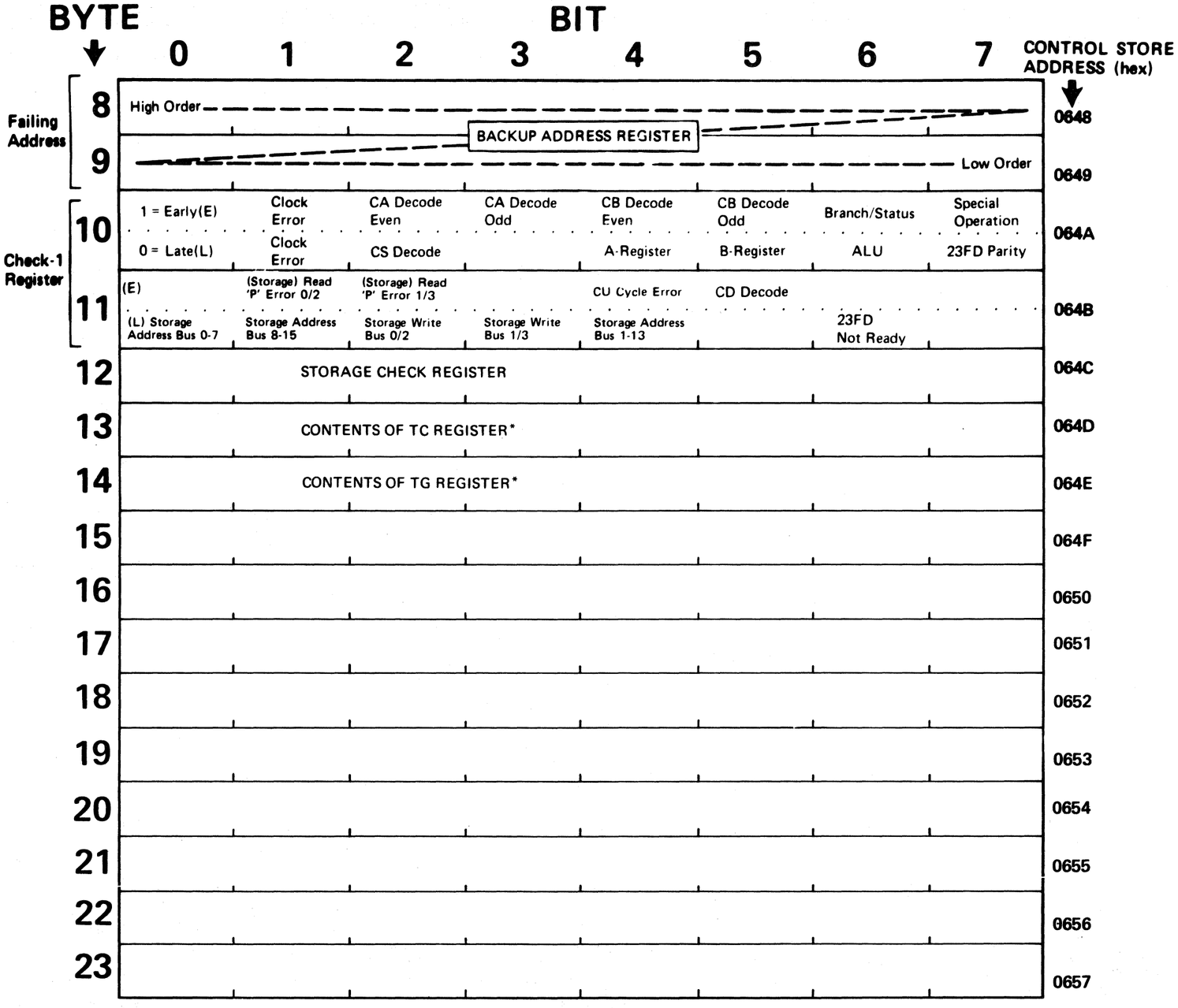
FORMAT 2

BYTE	BIT 0	1	2	3	4	5	6	7	CONTROL STORE ADDRESS (Hex)
8									0648
9									0649
10									064A
Control Check 11	Channel Buffer Parity Check	Interface Check- Channel A or C	Interface Check- Channel B or D	Data Transfer Check	CTL-I Check (defined by byte 20)	Load S-Registers	Compare Assist	Channel C/D or Multiconnect	064B
12									064C
CTL-I Bus Out 13	CONTENTS OF TA REGISTER (Valid only if sense byte 7 = '24')								064D
CTL-I Bus In 14	CONTENTS OF MA REGISTER (Valid only if sense byte 7 = '24')								064E
CTL-I Tag Bus 15	CONTENTS OF TD REGISTER (Valid only if sense byte 7 = '24')								064F
16									0650
17									0651
18									0652
19									0653
Control Interface Check 20	Controller Check*	Select Active Check*	CTL-I Buffer Check*	Unexpected End Check	Tag Bus Parity Check	Bus Out Parity Check	CTL-I Transfer Error		0654
21									0655
22									0656
23									0657

*These bits are secondary indications in format 2 and are shown for reference only.

SENSE DATA SUMMARY – FORMAT 3 (SELECTIVE RESET)

FORMAT 3



*T-registers are reset if selective reset is in response to Disconnect In from SCU.

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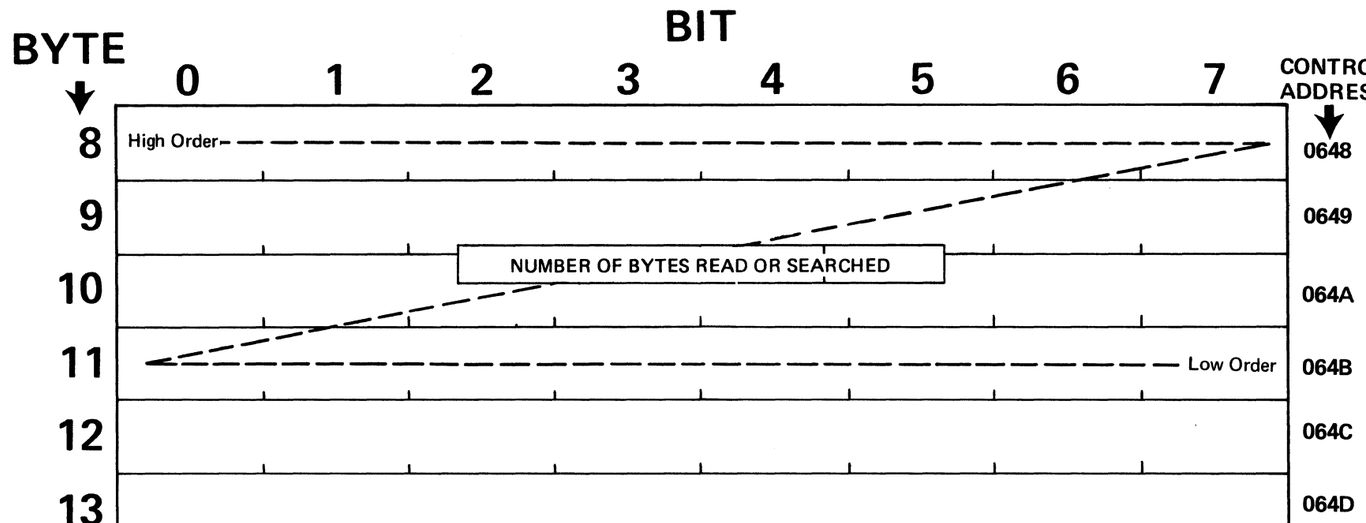
SENSE DATA SUMMARY – FORMAT 3 (SELECTIVE RESET)

SENSE 20

SENSE DATA SUMMARY – FORMAT 6 (USAGE/ERROR STATISTICS)

FORMAT 6



Device dependent information.
See device maintenance documentation.

3830-2
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Device
MLX Chart

AY0400	2347357
Seq 1 of 2	Part No. ( )

437403	437404	437405	437408	437414		
21 Apr 72	23 Jun 72	15 Aug 72	16 Oct 72	4 Jun 73		

SENSE DATA DESCRIPTION (Part 1 of 4)

Note: Sense byte formats 1, 4, and 5 are device dependent and are not described here. See device MLM.

SENSE BYTE 0

Sense bytes 0, 1, and 2 are generated when a Unit Check is presented. These bytes describe the error condition and identify which specific action should be invoked to effect subsystem error recovery.

Bit 0 — Command Reject (Format 0)

Sense Byte 7 identifies the error condition in more specific terms. Any of the following conditions causes this bit to be set:

- Invalid command code, or a command associated with an uninstalled feature has been issued.
- Invalid command sequence.
- Invalid or incomplete argument has been transferred by a control command.
- Write portion of file mask violated.
- Write command issued, but Write Inhibit (Write Protect) switch is on. Byte 1, bit 6 (Write Inhibited) is also set.

Refer to device MLM* for other conditions that can set this bit.

Bit 1 — Intervention Required (Format 1)

This bit indicates that the addressed device is:

- Not physically attached to the system.
- Not ready.
- A Diagnostic Write or Load CCW is issued while an inline microdiagnostic is resident in the control storage.

Bit 2 — Channel Bus Out Parity (Format 0)

The storage control has detected bad parity in data transferred from the channel. A parity error detected during command transfer is a Bus Out check and not a Command Reject. Go to START 25, entry A, and perform complete checkout procedure.

*Exit → 3830-2 / 14 Device MLX Chart

Bit 3 — Equipment Check (Formats 1, 2, 3)

An unusual hardware condition originated in the channel, storage control, controller, or drive. The conditions of this bit are defined in sense bytes 7 through 23. If sense byte 7 contains '00', perform checkout procedure on START 25, entry A. If byte 7 does not contain '00', decode using FSI 5.

Bit 4 — Data Check (Formats 4, 5)

Either of the following conditions causes this bit to be set:

- A correctable data error has been detected in information received from the drive. If byte 2, bit 1 is on; correction information is provided in sense bytes 15 through 22).
- An uncorrectable data error has been detected in information received from the drive. Condition is further defined in sense byte 7. See "Data Check" on MSG 20.

Bit 5 — Overrun (Format 0)

Data transfer was not accomplished within time allowed. This bit is posted only if:

- Overrun occurs more than ten times in a CCW chain.
- Overrun occurs in second or subsequent segment of an overflow record.
- Overrun occurs during a format Write operation.

Permanent Error (byte 1, bit 0) is also set if control unit retry is exhausted. Command overrun is retried, without Overrun being set. Overrun detection stops all data transmission. During writing, the remaining portion of the record is padded out with 0s. Go to START 25, entry A, and perform checkout procedure. If no failure, see FSI 10.

Bits 6, 7 — Refer to Device MLM*

SENSE BYTE 1

Bit 0 — Refer to Device MLM*

Bit 1 — Invalid Track Format (Format 0)

An attempt was made to write data exceeding track capacity. This bit normally indicates that a programming error or expected programming condition has been is detected. If a hardware malfunction suspected, go to device MLM* for checkout.

Bit 2 — End of Cylinder (Format 0)

One of the following conditions has occurred:

- A multitrack Read or Search operation has attempted to continue beyond the addressable cylinder boundary.
- An overflow operation has attempted to continue beyond the addressable cylinder boundary. Operation Incomplete (byte 1, bit 7) is also set.

End of Cylinder normally indicates that a programming error or expected programming condition has been detected. If a hardware malfunction is suspected, go to device MLM* for checkout.

Bit 3 — Unused

Bit 4 — No Record Found (Format 0)

One of the following has occurred:

- Two index points were sensed in the same command chain without an intervening Read operation in the home address or data area.
- Two index points were sensed in the same command chain without an intervening Write, Sense, or Control command.

The storage control always verifies that the access mechanism is positioned properly before posting this bit. This bit normally indicates a programming error or expected programming condition has occurred. If a hardware malfunction is suspected, go to device MLM* for checkout.

Bit 5 — File Protected (Format 0)

One of the following has occurred:

- A Seek command has violated the file mask.
- A multitrack Read or Search operation has violated the file mask.
- An overflow operation has violated the seek portion of the file mask. Operation Incomplete (byte 1, bit 7) is also set.

File Protected normally indicates a programming error or expected programming condition has been detected. If a hardware malfunction is suspected, go to device MLM* for checkout.

Bit 6 — Write Inhibited (Format 0)

A Write command was received for a drive that had its Write Inhibit (Write Protect) switch on.

Command Reject (byte 0, bit 0) is also set.

Check drive switch position; if found to be correct, go to device MLM*.

Bit 7 — Operation Incomplete (Format 0)

One of the following has occurred during the processing of an overflow record operation:

- Overflow to a file protected area. File Protected (byte 1, bit 5) is also set.
- Overflow past the cylinder boundary. End of Cylinder (byte 1, bit 2) is also set.
- A correctable Data Check was detected in the data field other than the last segment. Data Check (byte 1, bit 4) and Correctable (byte 2, bit 1) are also set.

Refer to device MLM* for other conditions that can set this bit.

Sense byte 3 provides the Restart command.

SENSE DATA DESCRIPTION (Part 1 of 4) SENSE 30

SENSE DATA DESCRIPTION (Part 2 of 4)

SENSE BYTE 2

Bit 0 — Refer to device MLM*

Bit 1 — Correctable (Format 5)

Indicates the data field Data Check posted in byte 0, bit 4 is correctable. Sense bytes 18 through 22 identify the error pattern and error pattern displacement.

Bit 2 — Unused

Bit 3 — Environmental Data Present (Format 6)

Usage or error counter statistics, or error log information, appears in sense bytes 8 through 23.

Bit 4 — Refer to Device MLM*

Bits 5-7 — Refer to device MLM*

SENSE BYTE 3

Bits 0-7 — Restart Command (Format 0)

This byte is provided when Operation Incomplete (byte 1, bit 7) is set. This byte identifies which operation was in progress when the interrupt occurred. The system recovery program uses this command, along with CSW information, to construct a new CCW. The new CCW is issued to the storage control, after correcting the unusual condition, to continue the operation following the point of interruption.

When Operation Incomplete is set, the Restart command is set to '06' to indicate a Read operation was in progress, or '05' to indicate a Write operation was in progress. Sense byte 3 is zero when Operation Incomplete is zero.

SENSE BYTE 4

Bits 0-7 — Physical Drive Identification (All Formats)

This byte identifies the physical drive that was selected when Unit Check was generated. Refer to device MLM* for bit interpretation.

SENSE BYTE 5

Bits 0-7 — Low Logical Cylinder (All Formats)

This byte identifies the low order cylinder address of the most current seek argument.

SENSE BYTE 6

Bits 0-7 — High Logical Cylinder, etc. (All Formats)

Refer to device MLM*.

SENSE BYTE 7

Bits 0-3 — Format

Bits 0-3 of sense byte 7 identify the format of the remaining sense bytes (8-23).

Format	General Category of Condition
0	Program or system checks (messages only; bytes 8-23 are unused)
1	Device equipment checks
2	Control unit equipment checks
3	Control unit control checks
4	Data checks not providing displacement information (uncorrectable data checks)
5	Data checks providing displacement information (correctable data checks)
6	Usage/error statistics

Formats 0, 2, and 3 pertain to storage control errors and are described in this MLM. Formats 1, 4, and 5 pertain to device errors and are described in the device MLM*. Format 6 contains usage/error information that is divided between this MLM and the device MLM.

Bits 4-7 — Message Code

Bits 4-7 of sense byte 7 provide an encoded message that describes the specific nature of the error condition.

*Exit
3830-2
14 Device MLX Chart

MESSAGE DESCRIPTIONS — FORMAT 0

Message 0 — No Message

No additional information is required.

Message 1 — Invalid Command

Issued command is not in the device's command set, or it belongs to a feature that is not installed.

Message 2 — Invalid Sequence

An invalid sequence of commands has occurred. Included are the following:

- A Read IPL command was preceded by a Set File Mask command in the same chain.
- A Write command has violated the write portion of a preceding Set File Mask command.
- A Write command has not satisfied the stipulated prerequisites.

Message 3 — CCW Count Less Than Required

The CCW count of a command is less than required. Included are the following:

- Any Seek command with a CCW count less than six.
- A Diagnostic Write command with a CCW count less than 512.
- 3340 series only — a Write HA command with a CCW count less than three.
- 3350 series only — a Write HA command with a CCW count less than seven.

Message 4 — Data Value Not As Required

The data argument is invalid. Included are the following:

- A Seek command argument that is not a valid seek address.
- A Set Sector command argument that is greater than 127 (3330 series) or 63 (3340 series), exluding 255.
- A Set File Mask command argument that does not have bits 2 and 6 set to zero.

Message 5 — Diagnostic Write Command Not Permitted By File Mask

A Diagnostic Write command is issued that violates bit 5 of the file mask.

FORMAT 0

Message 6 – Channel Discontinued Retry Operation

Channel did not indicate chaining after retry status was presented. Perform checkout procedure on START 25, entry A. Suspect disconnect sequence.

Message 7 – Channel Returned With Incorrect Retry CCW

Channel retry commands out of sequence. Perform checkout procedure on START 25, entry A.

Message 8 – MPL File Not Ready

Set on a Diagnostic Load command if the MPL file does not come to ready. See FSI 10, symptom code '0908'.

Message 9 – MPL File Permanent Seek Check

Set on a Diagnostic Load command if the operation cannot be completed because of an MPL file permanent seek check. See FSI 10, symptom code '0909'.

Message A – MPL File Permanent Read Check

Set on a Diagnostic Load command if the operation cannot be completed because of an MPL file permanent read check. See FSI 10, symptom code '090A'.

Message B (3330/3350 Series) – Improper Alternate Track Pointer

The record 0 count field of a defective track contains the track address of the defective track.

Message B (3340 Series) – Command Overrun

A command was received from the channel too late to be executed properly by the subsystem.

Message C (3330 Series) – Unconditional Reserve

String switch hardware is not modified for Unconditional Reserve Command or hardware failed to function.

Message C (3340/3344 Series) – Data Overrun

The response to a data request signal was not received by the storage control within the specified time or the command was a Unconditional Reserve and the string switch hardware has not been modified for this command.

Message C (3350 Series) – Unconditional Reserve

The microcode was unable to get access to the string switch with the use of the Unconditional Reserve Command.

FORMAT 0

Message D (3330 Series) – Index Detected In Gap Of Record

The index point was detected in the gap that precedes the key field or the data field. See FSI 10, symptom code '090D'.

Message D (3340/3344 Series) – Defective Track

- Track Condition Check (byte 0, bit 6) on:
  1. A single track command other than Search HA, Read HA, or Read R0 is executed on a defective track.
  2. A multitrack command (including Search HA, Read HA, or Read R0) or overflow record operation attempts to switch from a defective track.
  3. A multitrack command or overflow operation other than Search HA, Read HA, or Read R0 switches to a defective track.
- Operation Incomplete (byte 1, bit 7) on:

  During processing of an overflow record, a defective track condition is detected after initiation of data transfer.

Message D (3350 Series) – Unused

Message E (3330/3350 Series) – Unused

Message E (3340/3344 Series) – Alternate Track

This message is used in conjunction with Track Condition Check (byte 0, bit 6). It is generated when any multitrack command (including Search HA, Read HA, or Read R0) or overflow record operation attempts to switch from an alternate track.

Message F – Unused

FORMAT 2

MESSAGE DESCRIPTIONS – FORMAT 2

Message 0 – No Message

No additional information is required.

Messages 1, 2 – Unused

Message 3 – S-Register Load Check

S-register load circuit failed to operate properly. See FSI 25, symptom code '2923'.

Message 4 – CTL-I Registers Valid (Bytes 13-15)

Check-2 error while doing a CTL-I operation. Bytes 13-14, and 15 contain the contents of TA, MA, and TD registers. See FSI 25, symptom code '2924'.

Messages 5-F – Unused

FORMAT 2

SENSE BYTE 11 – FORMAT 2 (CONTROL CHECK)

Bit 0	Channel Buffer Parity Check
1	Interface Check, Channel A or C
2	Interface Check, Channel B or D
3	Data Transfer Check
4	CTL-I Check (see byte 20)
5	Load S-Registers Check
6	Compare Assist Check
7	Interface Check, Channel C/D or Multiconnect

SENSE BYTE 13 – FORMAT 2 (CTL-I BUS OUT)

This byte is cued for message 4 only. Identifies the contents of the TA register (CTL-I bus out).

SENSE BYTE 14 – FORMAT 2 (CTL-I BUS IN)

This byte is cued for message 4 only. Identifies the contents of the MA register (CTL-I bus in).

SENSE BYTE 15 – FORMAT 2 (CTL-I TAG BUS)

This byte is cued for message 4 only. Identifies the contents of the TD register (CTL-I tag bus).

SENSE BYTE 20 – FORMAT 2 (CTL-I CHECK)

Bit 0	Controller Check
1	Select Active or Select Check
2	CTL-I Buffer Parity Error
3	Unexpected End
4	Tag Bus Parity Check
5	Bus Out Parity Check
6	CTL-I Transfer Error
7	Unused

SENSE DATA DESCRIPTION (Part 3 of 4) SENSE 40

SENSE DATA DESCRIPTION (Part 4 of 4)

FORMAT 3

MESSAGE DESCRIPTIONS – FORMAT 3

Message 0 – No Message

No additional information is required.

Messages 1-F – Unused

SENSE BYTES 8, 9 – FORMAT 3 (FAILING ADDRESS)

Identifies the contents of the backup address register (CU storage address bus) at the moment the error was detected.

SENSE BYTES 10, 11 – FORMAT 3 (CHECK-1 REGISTER)

Bit assignment is dependent upon the state of byte 10, bit 0, as follows:

		On = Early Errors	Off = Late Errors
Byte 10, Bit 0			
	1	Clock Error	Clock Error
	2	CA Decode Even	CS Field or Stat Set
	3	CA Decode Odd	Zero
	4	CB Decode Even	A-Register Parity
	5	CB Decode Odd	B-Register Parity
	6	Branch/Status	ALU Check
	7	Special Operation	23FD Parity
Byte 11, Bit 0		Zero	Storage Addr Bus 0-7
	1	(Storage) Read 'P' Error 0/2	Storage Addr Bus Bus 8-15
	2	(Storage) Read 'P' Error 1/3	Storage Write Bus 0/2
	3	Zero	Storage Write Bus 1/3
	4	CU Cycle Error	Storage Address Bus 1-13
	5	DC Decode	
	6	Zero	23FD Not Ready
	7	Zero	Zero

SENSE BYTE 12 – FORMAT 3 (STORAGE CHECK REGISTER)

Identifies the contents of the storage error pattern register, which provides a binary code for diagnosing array card failures. See FSI 32.

SENSE BYTES 13, 14 – FORMAT 3

Identifies the contents of the TC and TG registers after an unsolicited selective reset has occurred. The TC and TG registers are reset by selective reset if the reset was invoked by the CU via the disconnect-in interface sequence.

FORMAT 6

SENSE BYTES 8-17 – FORMAT 6

Device-dependent information. See the device MLM* for details.

SENSE BYTE 18 – FORMAT 6

Bit 0 – Channel select for bytes 20-23. If bit 0 is off, the information applies to interfaces A and B. If bit 0 is on, the information applies to interfaces C and D.

Bits 1-7 – Unused

SENSE BYTE 19 – FORMAT 6 (SEEK ERRORS)

Identifies the total number of seek errors which were retried by the storage control. Seek errors detected on retry are excluded.

SENSE BYTE 20 – FORMAT 6 (COMMAND OVERRUN A/C)

Count of channel A or C command overruns retried by the storage control. (Overrun counts are frozen at 255 if the number of overruns exceeds 255.)

SENSE BYTE 21 – FORMAT 6 (DATA OVERRUN A/C)

Count of channel A or C data overruns retried by the storage control. (Overrun counts are frozen at 255 if the number of overruns exceeds 255.)

SENSE BYTE 22 – FORMAT 6 (COMMAND OVERRUN B/D)

Count of channel B or D command overruns retired by the storage control. (Overrun counts are frozen at 255 if the number of overruns exceeds 255.)

SENSE BYTE 23 – FORMAT 6 (DATA OVERRUN B/D)

Count of channel B or D data overruns retried by the storage control. (Overrun counts are frozen at 255 if the number of overruns exceeds 255.)

*Exit
3830-2
14 Device MLX Chart

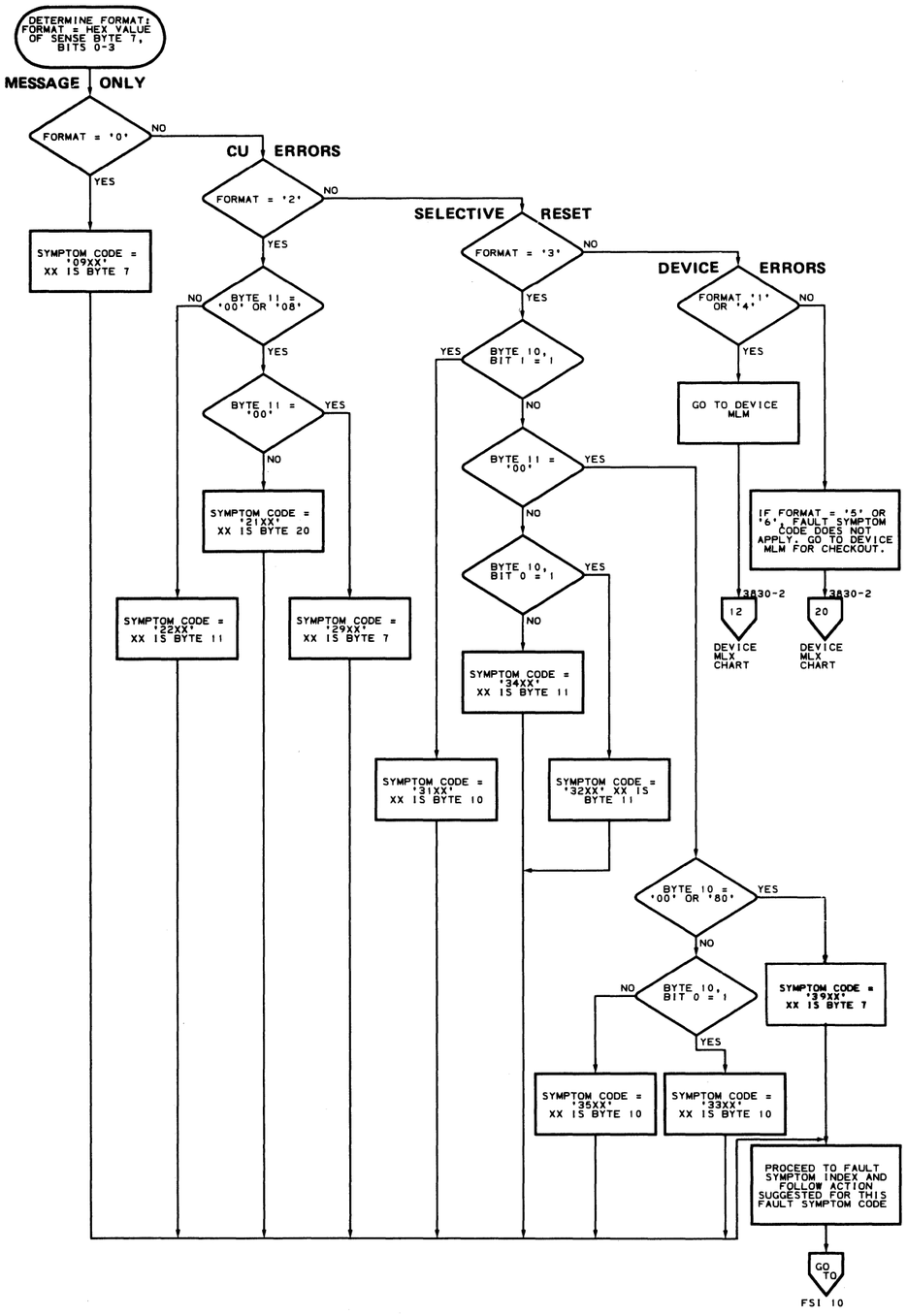
CONTENTS

FSI

DETERMINING FAULT SYMPTOM CODE

- The Fault Symptom Code (four hex digits) is used to enter the Fault Symptom Index.
- The Fault Symptom Code is constructed from sense data with the aid of the chart on this page.
- If sense data is not available from the CPU, it can be displayed on the CE panel from the Sense Control Block in control storage.

BIT	Sense Control Block '0684' SENSE CODE	'0685' FORMAT/MESSAGE	'0686' SENSE POINTER	'0687' MISC
0	Unused	Bits 0-3 are decoded into Formats 0-6 0 Message Only 1 Device Errors 2 CU Errors 3 Selective Reset 4 ECC Uncorrectable 5 ECC Correctable 6 Usage/Error Count	Points to location of stored sense data.	
1	Operation Incomplete			
2	Correctable			
3	Byte Number 01 Byte 0 10 Byte 1 11 Byte 2 00 Byte 0 and permanent error			
4		Bits 4-7 are decoded into messages 0-F. Meaning of messages depends on format decoded. (See SENSE 10)		
5				
6	Bit Position in Byte			
7				



1. Determine Fault Symptom Code from chart on FSI 5.
2. Using the Fault Symptom Code, find the corresponding line in the Fault Symptom Index. Take action indicated.
3. Refer to START 900-911 for data flow by card and common card information.
4. Refer to LGND section for logic symbology, voltage levels, etc.

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

CU CE PANEL REGISTERS	FORMAT	MESSAGE	DEVICE ERRORS							
SENSE BYTE	7	0	1							

FAULT SYMPTOM CODE	ERROR DESCRIPTION	ACTION REQUIRED FIELD REPLACEABLE UNITS in order of probability of failure			MAP ENTRY	SUGGESTED MICRODIAGNOSTIC	FORMAT 0 1 2 3 4 5 6 7	MESSAGE 0 1 2 3 4 5 6 7	COMMAND REJECT 0 1 2 3 4 5 6 7	BUS OUT PARITY / EQUIPMENT CHECK 0 1 2 3 4 5 6 7	OVERRUN 0 1 2 3 4 5 6 7	PERMANENT ERROR 0 1 2 3 4 5 6 7	FAULT SYMPTOM CODE
0000	Symptom code not generated by microprogram. Go to FSI 5 to develop code.												
0900	Channel bus out parity error detected (Also possible Permanent Data Overrun See below.)	A1M2	A1L2	B2L2	CHL-I 30		0 0 0 0 0 0 0 0	0 0 1 0 0 0				0	
		A1S2		A1U2									
	CHANNEL A	A1Q2	B-A1E2	B-A1F2		Rtn 60–6E (See MICRO 200 for procedures)							
	CHANNEL B	A1P2	B-A1E4	B-A1F4									
	CHANNEL C	A1K2	A1F2	A1E2									
	CHANNEL D	A1J2	A1F4	A1E4									
0900	Permanent Data Overrun detected (not set for Command Overrun)	A1S2	A1U2	B2L2	CHL-I 35		0 0 0 0 0 0 0 0	0 0 0 0 0 0 1				1	
0901	Invalid Command						0 0 0 0 0 0 0 1	1 0 0 0 0 0				0	
0902	Invalid Sequence (CCW)						0 0 0 0 0 0 1 0	1 0 0 0 0 0				0	
0903	CCW count less than required						0 0 0 0 0 0 1 1	0 0 0 1 0 0				0	
0904	Data Value not as required				SENSE 40		0 0 0 0 0 1 0 0	0 0 0 1 0 0				0	
0905	Diag Write Command not permitted by file mask.						0 0 0 0 0 1 0 1	1 0 0 0 0 0				0	
0906	Channel discontinued retry operation						0 0 0 0 0 1 1 0	0 0 0 1 0 0				0	
0907	Channel returned with incorrect retry CCW						0 0 0 0 0 1 1 1	0 0 0 1 0 0				0	
0908	MPL File Not Ready	B2S2	B1L2	B1T4	MPL 30		0 0 0 0 1 0 0 0	0 0 0 1 0 0				0	
0909	MPL File Permanent Seek Check	B1T4	B1S2 B2N2	B2S2 B2F2	MPL 45		0 0 0 0 1 0 0 1	0 0 0 1 0 0				0	
090A	MPL File Permanent Read Check	B1S2	B2S2 B2N2	B1T4 B2F2	MPL 15		0 0 0 0 1 0 1 0	0 0 0 1 0 0				0	
090B	Improper alternate track pointer				SENSE 40		0 0 0 0 1 0 1 1	1 0 0 0 0 0				0	
090C	Unconditional Reserve failed or controller hardware not installed					Note 1	0 0 0 0 1 1 0 0	0 0 0 1 0 0				0	
090D	Index detected in gap of record					Note 1	0 0 0 0 1 1 0 1	0 0 0 1 0 0				0	
						Note 1: Exit to Device MLX (entry 10 from 3830-2).							

FAULT SYMPTOM INDEX – FORMAT 2

1. Determine Fault Symptom Code from chart on FSI 5.
2. Using the Fault Symptom Code, find the corresponding line in the Fault Symptom Index. Take action indicated.
3. Refer to START 900-911 for data flow by card and common card information.
4. Refer to LGND section for logic symbology, voltage levels, etc.

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

FAULT SYMPTOM CODE	ERROR DESCRIPTION	ACTION REQUIRED: FIELD REPLACEABLE UNITS in order of probability of failure			MAP ENTRY	SUGGESTED MICRODIAGNOSTIC
2100	CTL-I Check with No CTL-I Check bit. See Note 1.	B1R2	B1F2		PANEL 50	CTL-I Wraparound Routines 8C-94 (See MICRO 500 for Running Procedure)
2102	CTL-I Transfer Check. See Note 1.	B1D2	B1R2			
2104	CTL-I Bus Out Parity Check. See Note 1.	B1D2	B1E2	B1R2		
2108	CTL-I Tag Bus Parity Check. See Note 1.	B1F2	B1R2	B1M2		
2110	Unexpected End. See Notes 1 and 2.	B1Q2 B1C4	B1M2	B1L2 B1D2		
2120	Buffer Bus In Parity Check. See Notes 1 and 2.	B1D2	B1C2	B1B2 B1E2		
2140	Select Active without Select Hold. See Notes 1 and 2.	B1B2	B1M2	B1R2		
2180	Controller Check. See Notes 1 and 2.	B1C4	B1R2			
2186	Controller Check and Transfer Check. See Note 2.					
21XX	If bit 0, 1, 2, or 3 of sense byte 20 is on, suspect device. See Note 2.					

CU CE PANEL REGISTERS	FORMAT	CONTROL	CI CHECK	TA	MA	TD	
SENSE BYTE	7	11	20	13	14	15	

FAULT SYMPTOM CODE	BITS 0-3 ARE DECODED TO FORM FORMATS 0-F	BITS 4-7 ARE DECODED TO FORM MESSAGES 0-F	BUFFER PARITY CHECK	INTERFACE CHK-CH A OR C	INTERFACE CHK-CH B OR D	CTL-I XFER CHECK	LOAD S REG CHECK	COMPARE ASSIST CHK	CH C/D OR MULTI-CONN	CONTROLLER CHECK	SELECT ACTIVE CHECK	CTL-I BUS IN PAR. CHK	UNEXPECTED END	TAG BUS CHECK	CTL-I BUS OUT PAR CHK	CTL-I XFER ERROR	UNUSED	FAULT SYMPTOM CODE
	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	
2100	0 0 1 0 0	0 0	0 0 0 0 1 0 0 0	0 0 0 0 0 0 0 0														
2102	0 0 1 0 0	0 0	0 0 0 0 1 0 0 0	0 0 0 0 0 0 0 1														
2104	0 0 1 0 0	0 0	0 0 0 0 1 0 0 0	0 0 0 0 0 0 1 0														
2108	0 0 1 0 0	0 0	0 0 0 0 1 0 0 0	0 0 0 0 0 0 1 0 0														
2110	0 0 1 0 0	0 0	0 0 0 0 1 0 0 0	0 0 0 0 1 0 0 0														
2120	0 0 1 0 0	0 0	0 0 0 0 1 0 0 0	0 0 0 1 0 0 0 0														
2140	0 0 1 0 0	0 0	0 0 0 0 1 0 0 0	0 1 0 0 0 0														
2180	0 0 1 0 0	0 0	0 0 0 0 1 0 0 0	1 0 0 0 0 0														
2186	0 0 1 0 0	0 0	0 0 0 0 1 0 0 0	1 0 0 0 1 1														

Note 1: If sense byte 7, bit 5 (Message 4) is on, then sense bytes 13, 14, 15 are valid, otherwise they are not valid.

Note 2: If no errors are detected by Wraparound Routine, suspect device problem. Exit to Device MLX, entry 15 from 3830-2.

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1. Determine Fault Symptom Code from chart on FSI 5.
2. Using the Fault Symptom Code, find the corresponding line in the Fault Symptom Index. Take action indicated.
3. Refer to START 900-911 for data flow by card and common card information.
4. Refer to LGND section for logic symbology, voltage levels, etc.

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

FAULT SYMPTOM CODE	ERROR DESCRIPTION	ACTION REQUIRED FIELD REPLACEABLE UNITS in order of probability of failure			MAP ENTRY	SUGGESTED MICRODIAGNOSTIC
2202	Compare Assist Check. See Note 1.	B1Q2	B1N2		PANEL 50	CTL-I Wraparound Routines 8C-94 (See MICRO 500 for Running Procedure)
2204	Even number of MA to S register gates detected active at the same time. See Note 1.	B1Q2	B1L2	B1D2		
2210	A failure is detected with the control lines that cause data to move from the channel interface to the NA Register on write operations and from the MD Register to the channel interface on read operations. Single Channel and Two Channel Switch.	A1U2	A1S2	A1L2 A1T2	PANEL 50 ALD GK702	
	Two Channel Switch, Additional	A1U2	A1S2 A1L2	A1M2 A1T2	PANEL 50	
2220	An invalid combination of control lines is active in the channel interface logic Channel B on Two Channel Switch machine.	A1P2	A1U2 A1T2	B1L2 A1L2	CHL-I 185 PANEL 50	Channel Wrap-around Routines 60 thru 6E (See MICRO 200 for Running Procedure.)
	Channel B on Two Channel Switch Additional machine.	A1P2	A1N2 B1L2	A1T2 A1L2		
2221	Channel D on Two Channel Switch Additional machine.	A1J2	A1N2 B1L2	A1T2 A1L2		
2240	An invalid combination of control lines is active in the channel interface logic. Single Channel or Channel A on Two Channel Switch machine.	A1Q2	A1U2 A1T2	B1L2 A1L2	CHL-I 185 PANEL 50	
	Channel A on Two Channel Switch Additional machine.	A1Q2	A1N2 B1L2	A1T2 A1L2		
2241	Channel C on Two Channel Switch Additional machine.	A1K2	A1N2 B1L2	A1T2 A1L2		
2280	Parity error detected on output of the channel buffer. Single Channel.	A1T2	B1F2		CHL-I 155 PANEL 50 ALD GK604	
	Two Channel Switch machine	A1T2	B1F2	A1L2		
	Two Channel Switch Additional machine	A1T2	B1F2	A1L2 A1M2		
2290	Refer to Symptom Code 2210				PANEL 50	

CU CE PANEL REGISTERS	FORMAT	CONTROL	CI CHECK	TA	MA	TD	
SENSE BYTE	7	11	20	13	14	15	

FAULT SYMPTOM CODE	BITS 0-3 ARE DECODED TO FORM FORMATS 0-F	BITS 4-7 ARE DECODED TO FORM MESSAGES 0-F	BUFFER PARITY CHECK	INTERFACE CHK-CH A OR C	INTERFACE CHK-CH B OR D	DATA XFER CHECK	CTL-I CHECK	LOAD S REG CHECK	COMPARE ASSIST CHK	CH C/D OR MULTI CONN	CONTROL LER CHECK	SELECT ACTIVE CHECK	CTL-I BUS IN PAR CHK	UNEXPECTED END	TAG BUS CHECK	CTL-I BUS OUT PAR CHK	CTL-I XFER ERROR	UNUSED	FAULT SYMPTOM CODE
	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	
2202	0 0 1 0 0 0 0 0	0 0 0 0 0 0 1																	2202
2204	0 0 1 0 0 0 0 0	0 0 0 0 0 0 1																	2204
2210	0 0 1 0 0 0 0 0	0 0 1 0																	2210
2220	0 0 1 0 0 0 0 0	0 1 0 0																	2220
2221	0 0 1 0 0 0 0 0	0 1 0 1																	2221
2240	0 0 1 0 0 0 0 0	1 0 0 0																	2240
2241	0 0 1 0 0 0 0 0	1 0 0 1																	2241
2280	0 0 1 0 0 0 0 0	1 0 0 0 0																	2280
2290	0 0 1 0 0 0 0 0	1 0 0 1 0																	2290

Note 1: If sense byte 7, bit 5 (Message 4) is on, then sense bytes 13, 14, 15 are valid, otherwise they are not valid.

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1. Determine Fault Symptom Code from chart on FSI 5.
2. Using the Fault Symptom Code, find the corresponding line in the Fault Symptom Index. Take action indicated.
3. Refer to START 900-911 for data flow by card and common card information.
4. Refer to LGND section for logic symbology, voltage levels, etc.

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

CU CE PANEL REGISTERS	FORMAT	CONTROL	CTL-I CHECK	TA	MA	TD	
SENSE BYTE	7	11	20	13	14	15	

FAULT SYMPTOM CODE	ERROR DESCRIPTION	ACTION REQUIRED: FIELD REPLACEABLE UNITS in order of probability of failure			MAP ENTRY	SUGGESTED MICRODIAGNOSTIC	BITS 0-3 ARE DECODED TO FORM FORMATS 0-F	BITS 4-7 ARE DECODED TO FORM MESSAGES 0-F	BUFFER PARITY CHECK	INTERFACE CHK-CH A ORC	INTERFACE CHK-CH B ORD	DATA XFER CHK-CH A ORC	CTL-I CHECK	LOAD S REG CHECK	COMPARE ASSIST CHK	CH C/D OR MULTI-CONN	CONTROLLER CHECK	SELECT ACTIVE CHECK	CTL-I BUS IN PAR CHK	UNEXPECTED END	TAG BUS CHECK	CTL-I BUS OUT PAR CHK	CTL-I XFER ERROR	UNUSED	FAULT SYMPTOM CODE
							0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	
2923	S Register Load Error Message.	B1Q2	B1L2		CTL-I 190	8C-94	**0 0 1 0 0 0 1 1**																		
2920	Check 2 with no bit in byte 11 or 20. See Note 1.	A1T2	B2Q2		PANEL 50	Hardcore and 8C-94 60-6E	**0 0 1 0 0 0 0 0**																		
2924	CTL-I Registers Valid Message. A Check 2 detected during a selection sequence with no bit in sense byte 11 or 20. Refer to Symptom Code 2920.						**0 0 1 0 0 1 0 0**																		

Note 1: If sense byte 7, bit 5 (Message 4) is on, then sense bytes 13, 14, 15 are valid, otherwise they are not valid.

FAULT SYMPTOM INDEX–FORMAT 3

1. Determine Fault Symptom Code from chart on FSI 5.
2. Using the Fault Symptom Code, find the corresponding line in the Fault Symptom Index. Take action indicated.
3. Refer to START 900-911 for data flow by card and common card information.
4. Refer to LGND section for logic symbology, voltage levels, etc.

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

CU CE PANEL REGISTERS	FORMAT	CHECK 1 REGISTER BITS 0–7	CHECK 1 REGISTER BITS 8–15							
SENSE BYTE	7	10	11							

FAULT SYMPTOM CODE	ERROR DESCRIPTION	ACTION REQUIRED FIELD REPLACEABLE UNITS in order of probability of failure			MAP ENTRY	SUGGESTED MICRODIAGNOSTIC	0 FORMAT	1 FORMAT	2 FORMAT	3 MESSAGE	4 MESSAGE	5 MESSAGE	6 MESSAGE	7 MESSAGE	0 ON=EARLY/OFF=LATE CLOCK	1 CA DECODE EVEN	2 CA DECODE ODD	3 CB DECODE EVEN	4 CB DECODE ODD	5 BRANCH/STATUS ERROR	6 SPECIAL OPER. ERROR	7 (Storage) READ 'P' ER. 0/2	8 (Storage) READ 'P' ER. 1/3	9 CU CYCLE ERROR	10 CD DECODE ERROR	11	12	13	14	15	FAULT SYMPTOM CODE
3XXX	A failure in the Check 1 register can cause any format 3 symptom. If problem is not resolved by action under appropriate symptom code below, replace Check 1 register card (B2Q2).	B2Q2	B2N2		PANEL 40	HC00-0A	0	0	1	1	0	0	0	0																	
31XX	Error detected in CU clock	B2N2	B2M2	B2P2	PANEL 40	84	0	0	1	1	0	0	0	0	1																
3204	Error detected in CD decode circuitry	B1P2	B2J2	B1D2	PANEL 40	82	0	0	1	1	0	0	0	0	1	0							0	0			1				
		B1F2	B2K2	A1T2																											
		B1M2	B2P2	B1Q2																											
		B1G2	B2N2	B1U4																											
		B2G2	B2S2	B2Q2																											
3208	Error detected in cycle control circuitry	B2P2	B2N2		PANEL 40	82	0	0	1	1	0	0	0	0	1	0							0	0			1	0			
3220	Generated Parity and Parity bytes 1 and 3 miscompared.				FSI 31, Entry A	88	0	0	1	1	0	0	0	0	1	0							0	1							
3240	Generated Parity and Parity bytes 0 and 2 miscompared.				FSI 31, Entry A	88	0	0	1	1	0	0	0	0	1	0							1	0							
3260	Generated Parity and Parity bytes 0 and 2, and 1 and 3 miscompared.				FSI 31, Entry A	88	0	0	1	1	0	0	0	0	1	0							1	1							

CONTROL STORAGE FAILURE ANALYSIS (Part 1 of 5)

SNIPE STORAGE FAILURE ANALYSIS

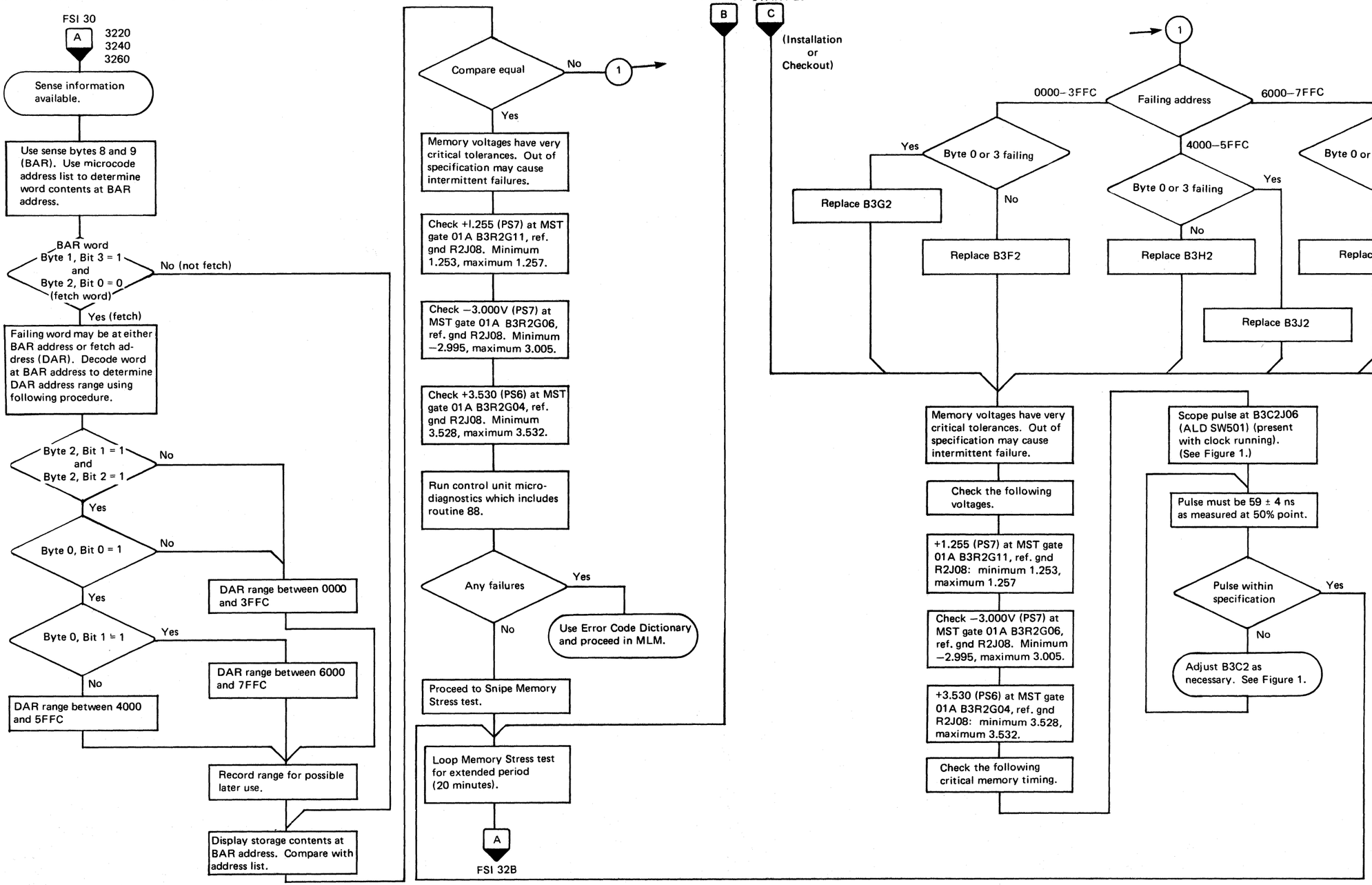
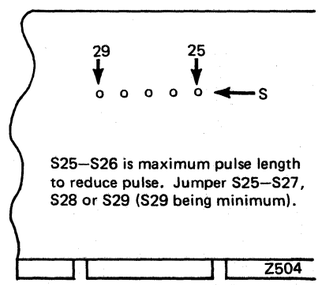


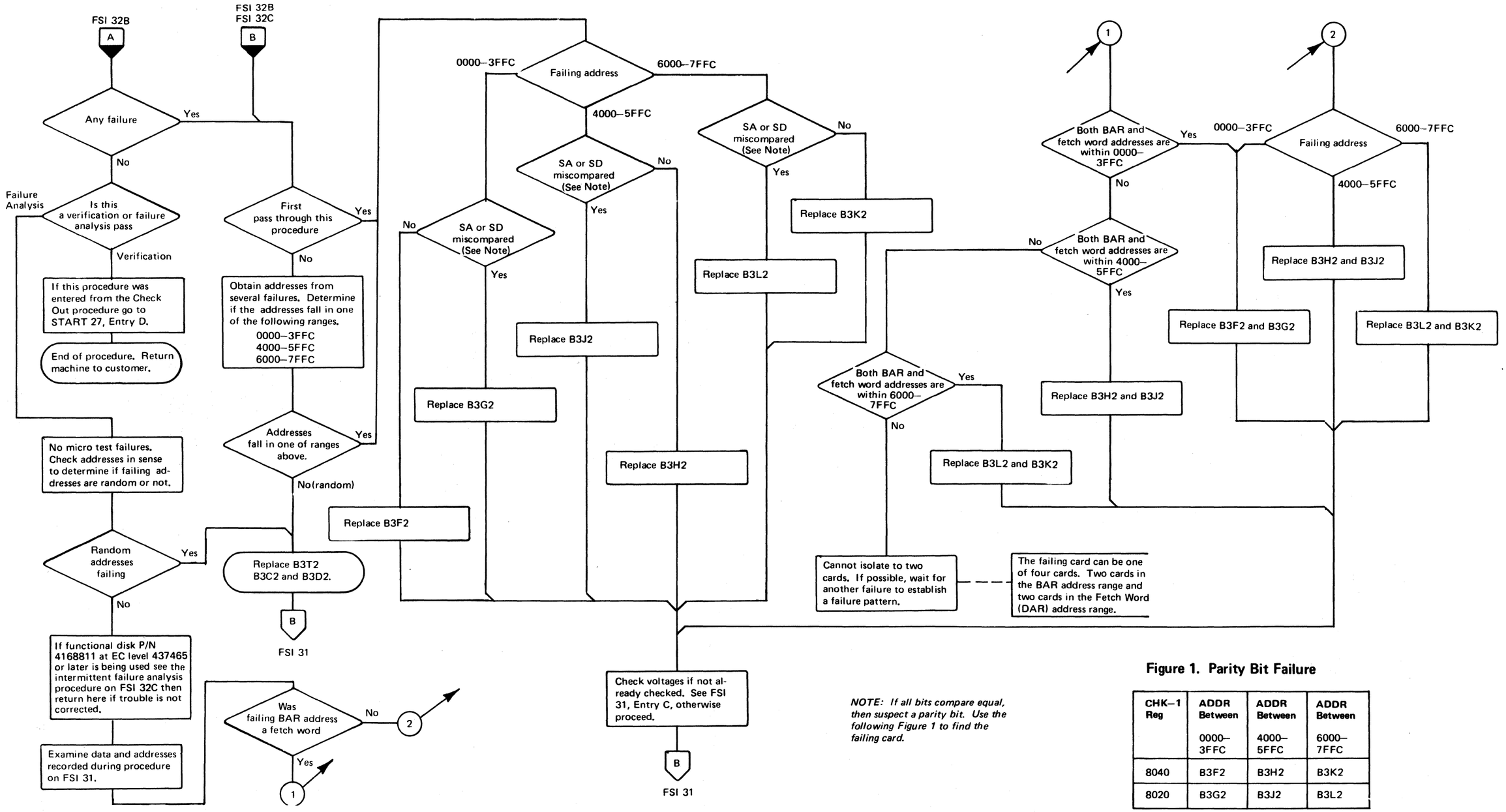
Figure 1. B3C2 Pulse Length Adjustment



3830-2	BA0600 Seq. 2 of 2	4290917 Part No. (2)	447460 19 Dec 75	447461 12 Mar 76	447464 15 Nov 77	447465 15 Dec 78	

CONTROL STORAGE FAILURE ANALYSIS (Part 2 of 5)

SNIPE STORAGE FAILURE ANALYSIS (Cont.)



NOTE: If all bits compare equal, then suspect a parity bit. Use the following Figure 1 to find the failing card.

Figure 1. Parity Bit Failure

CHK–1 Reg	ADDR Between 0000–3FFC	ADDR Between 4000–5FFC	ADDR Between 6000–7FFC
8040	B3F2	B3H2	B3K2
8020	B3G2	B3J2	B3L2

CONTROL STORAGE FAILURE ANALYSIS (Part 3 of 5)

- This procedure uses the control storage microdiagnostic (routine 88). Refer to MICRO 15 for loading of microdiagnostics.

ROUTINE 88 OPERATING DETAILS

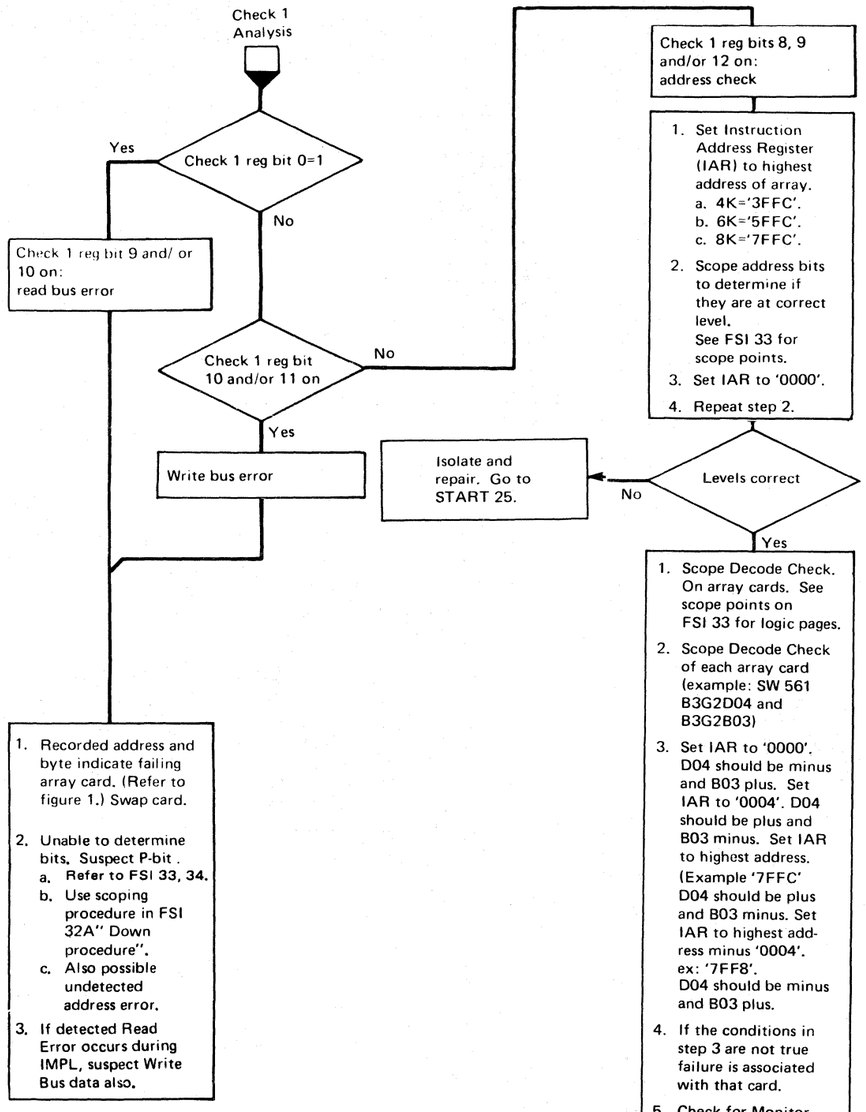
1. Mode switch to CE Check Bypass.
2. Entry/Display switch to Program Data Entry.
3. Data Entry switches to '88'.
4. Operate Execute switch.
5. Address/Check/Program Display lights indicate 'C088' when routine loaded.
6. Use option to inhibit linking. See MICRO 16.
7. For 6 or 8K enter parameters shown on MICRO 15, Step 11, and MICRO 402. Or, for default parameters, set Data switches to '38' and operate the Execute switch.
8. Program halts when error is detected:
   a. 81xx is displayed, where xx is failing bit.
   b. To get failing address and byte, execute '20' CE command for each byte:

      82xx (xx is address high byte)
      83xx (xx is address low byte)
      840x (x is the failing byte No. 0, 1, 2, or 3)

9. Use failing address and byte to determine possible failing array card (see figure 1.)
   Example: '8242' = Address high byte = '42'
   '8324' = Address low byte = '24'
   Address = '4224' (4K–6K range)
   '8401' = failing byte = byte 1
   Possible failing array card is B3H2 from figure 1.

10. If the array card does not correct the problem use error byte and bit to isolate.
    Example: error byte = 8400 = byte 0
    error bit = 8108 = bit position
    Lit bit indicates failing bit.
    00 indicates probable 'P' bit.
    See chart 1 (parity) and
    Trilead chart (Read Bus) on FSI 33

Microdiagnostic routine 88 normally halts on an error.
If the program cannot be loaded, go to the down procedure on FSI 32A.



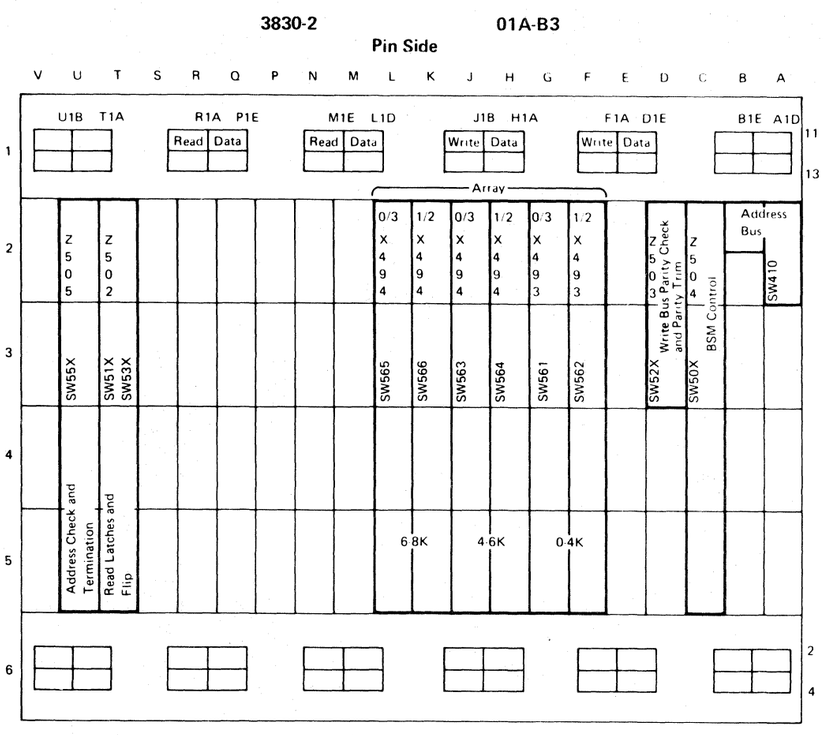


Figure 1.

Array Card	Byte 0	Byte 1	Byte 2	Byte 3
B3F2		0–4K	0–4K	
B3G2	0–4K			0–4K
B3H2		4–6K	4–6K	
B3J2	4–6K			4–6K
B3K2		6–8K	6–8K	
B3L2	6–8K			6–8K

CONTROL STORAGE FAILURE ANALYSIS (Part 4 of 5)

DOWN PROCEDURE

If the microdiagnostic will not run or cannot be loaded, consider the following:

1. Store - Display
   a. Store and display a pattern of all 1s and 0s in a known failing address. If address is unknown, start at '0000' with store and display operation. Increase IAR by '1000' until highest address is reached. Refer to PANEL 15 for CE panel operations.
   b. If a bit(s) is dropped or picked, decode array card by byte and bit and replace using chart on FSI 33.
      (1) If check 1 register bits 0 & 9 (read byte 1/3) or check 1 register bits 0 & 10 (read byte 0/2) are on, swap cards (one pair at a time)
          Lower 4K-B3F2 with B3G2
          Upper 4K-B3H2 with B3J2 and B3K2 with B3L2
      (2) If check 1 bits change, replace defective card.
   c. If same failure still exists go to step 2. Otherwise, see Note 1.
2. To check for picked or dropped bits, recycle the control unit in the following manner (See also Note 2.):
   a. If bits are picked, store a word of all 0s. Set ACR, IAR and Address Entry switches to same address as word just entered. Set ACR toggle switch to recycle, Mode switch to Check Bypass; operate Start switch. This one address should be recycling. Scope array card (see Note 3) output for bit in question. Refer to diagrams on FSI 33, 34 for scope points and trileads. Parity bits for byte 0/2, 1/3 equal logical 1.
   b. If bits are dropped, follow same procedure as (a) except: Store word of FF EF FFFF. (Byte 1, bit 3 must be 0 to prevent data cycles.) Parity bits for 0/2 = 1, for 1/3 = 0.
   c. Read, write and address bus may be scoped in the static condition. See trilead chart on FSI 33 for scoping points.

      Enter sotrage with known data (refer to PANEL 15) at failing address (or random address if failing address is unknown). After storage is entered, the write bus and address bus may be scoped in the static condition. The read bus may be scoped statically by displaying storage. (See PANEL 15.) The read bus will then be active.
3. If failures are highly intermittent or not determined, suspect:
   B3C2 - array control card
   Voltages - see PWR 50 (MLM)
   B3T2 - Read Parity Check Card
   B3D2 - Write Bus Parity Check
   B3U2 - address check card and terminators
   B2P2, B2N2, B3T2, B3D2, B2K2, B2T2, B2S2, B1Q2, B1P2, B1D2.
4. Refer to CTRL 600 for read/write timings and details of control store operation.

CAUTION
Power-down before removing or replacing any card in control storage.

NOTE 1: If failure is random or highly intermittent, suspect control card B3C2, address check card B3U2, and terminator cards. Also dump EREP and check for format 3, check 1 register = '8020', or '8040', or '8060'. Failing address will be in bytes 8 and 9.

NOTE 2: On this recycle operation there is no write cycle of the array. Writing in the array is done only when the Execute switch is operated in a manual store operation.

NOTE 3: Input can be scoped but will be in a static condition. (See down procedure on this page.) Write Gate will not be recycling.

CONTROL STORAGE FAILURE ANALYSIS (Part 5 of 5)

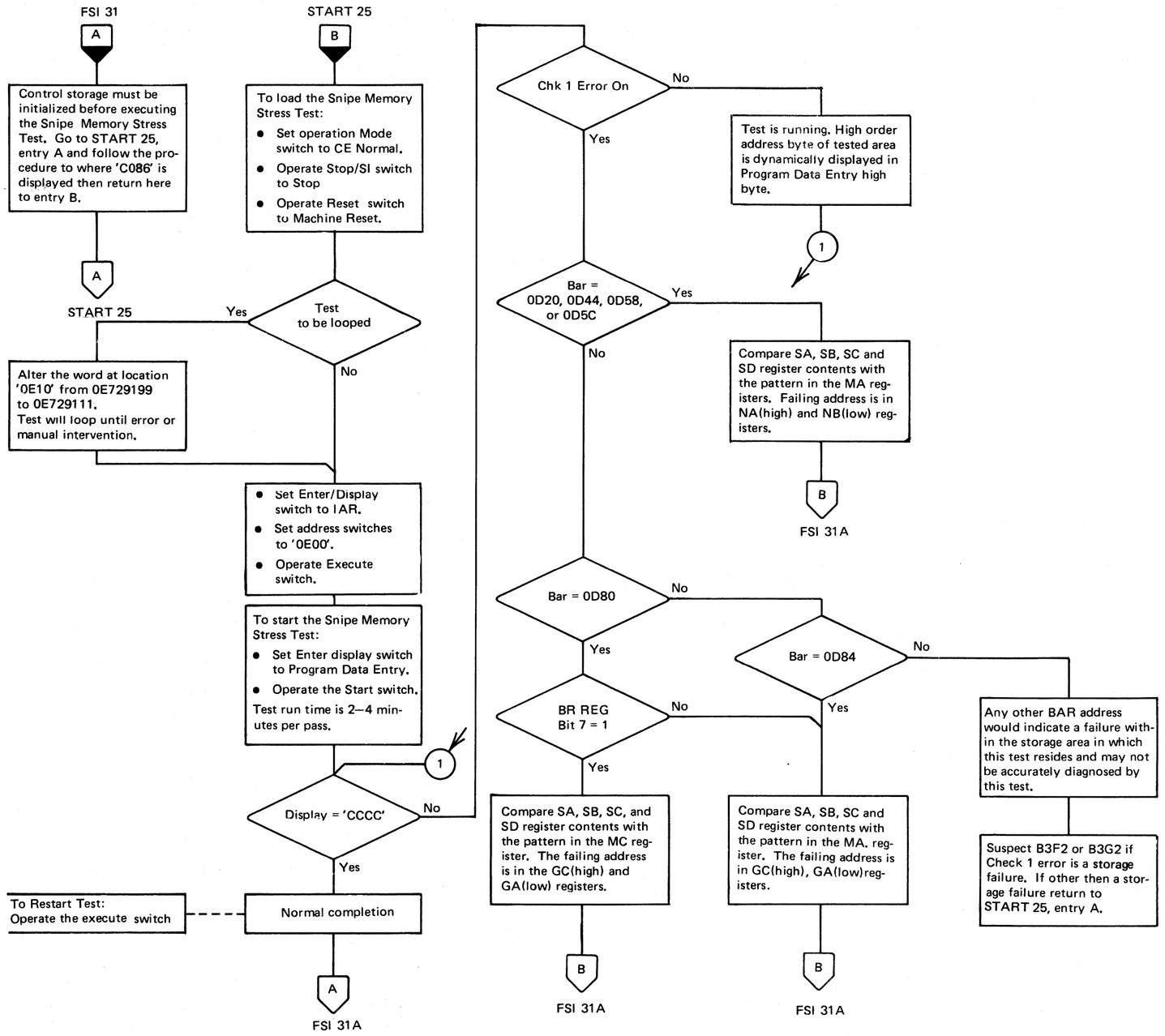
SNIPE MEMORY STRESS TEST

Test Description

Control storage is tested in 4K increments called test areas (with the exception of 0D00 through 0EFC which is where this test resides).

Four test patterns are used to scan storage, '00', 'AB' and their inverse 'FF' and '54'. The test begins by writing a test pattern throughout the test area. Upon completion of the write operation the test sets up to exercise the test area one word at a time. This word is referred to as the test position. The test position starts at the lowest address in the test area. The test position is written eight consecutive times alternating between the test pattern and inverted test pattern and ending with the inverted test pattern. At this time the test area is scanned twice. If no errors are detected in the read scans the test position is restored to the original pattern and the test position address is incremented to the next consecutive address. The process is repeated in this manner until all the test area has been tested, at which time the next test pattern is written into the test area and the above procedure is repeated until all the patterns have been used.

Upon the completion of one test area the address of the test area is incremented to the next 2K block of storage for 6K machines or 4K block for 8K machines. Upon successful completion 'CCCC' is displayed, any failure will be indicated by a Check 1 error.



SNIPE STORAGE REWRITE

Purpose

The functional microcode disk P/N 4168811 at EC level 437465 or later has a routine which will attempt to rewrite a failing control store word when a storage failure occurs. Busy will be presented to the channel while the rewrite from the 23FD is taking place. A successful rewrite of a bad word in control store will allow continued customer operation without repetitive storage failures (Check 1 errors).

Normal Operation

The functional microcode disk must be loaded in the 23FD reader. The rewrite routine is activated by Selective Reset following a storage failure (Check 1 register '8040' or '8020'). The rewrite routine will access and read the 23FD disk sector containing the failing word. The failing word is rewritten into control store if it is in a restorable location (locations in working storage containing dynamically updated instructions are not restorable. For example 04XX, 05XX where microdiagnostic routines reside are not restorable). Storage Rewrite is inoperative when routine '90' (Tracer Dumper Micro) is involked. After the rewrite is complete, all control storage is scanned for proper parity. An error detected during this scan or the inability to reload the original failing word successfully will result in a hard stop with BAR equal to '7250', Check 1 lamp On, and Interface Disable lamp On. DAR will contain the address of the failing word. The S-Registers will contain the failing word.

START 25

A

Failure Analysis

BAR must equal 7250 to use this procedure. If BAR is not 7250, analyze the failure as any other Check 1 error.

If BAR is equal to 7250, use the address in DAR to find the failing word in the microcode address list (address list is on microfiche P/N 4168831). Compare the address list failing word with the contents of the S-Registers to determine which bit is failing. If all bits compare equal, then suspect a parity bit. Use figure 1 on FSI 31A to locate the failing card. Record the contents of the S-Register containing the failing bit. Go to FSI 31A, entry B.

Intermittent Failure Analysis

A technique for analyzing intermittent failures is to prevent the rewrite operation from successfully completing by either removing the functional disk from the 23FD or leaving the 23FD cover open during customer operation. *Consider the impact on customer operations if the error is recoverable and this technique is used.* All indications described under **Normal Operation** will be present when a single failure occurs if BAR = 7250. Use the address in DAR to find the failing word in the microcode address list (address list is on microfiche P/N 4168831). Compare the address list failing word with the contents of S-Registers to determine which byte is failing. If all bytes compare equal, suspect a parity bit failure. Failing card isolation can then be accomplished using the MAP on FSI 31A, entry B.

Chart 1

Array Card	Byte 0	Byte 1	Byte 2	Byte 3
B3F2		0-4K	0-4K	
B3G2	0-4K			0-4K
B3H2		4-6K	4-6K	
B3J2	4-6K			4-6K
B3K2		6-8K	6-8K	
B3L2	6-8K			6-8K

Write Bus Parity Check and Trim B3D2.

Read Latches, Parity Check and Generate B3T2

+Read Bus

To CU. See also FSI 34.

INTERBOARD CONNECTOR

+Write Bus

RL 301-306
RL 401-406

SCOPE POINTS

BSM Control Bits 0, 1 and 2 SW50x B3C2

Array Address check Bits 0, 1, 3 and 4 P-0-7, P 8-13 SW553, CTRL 620 B3U2

D06 +Address Check

Array Cards
SW 561-B3G2 0-4K
SW 562-B3F2 0-4K
SW 563-B3J2 4-6K
SW 564-B3H2 4-6K
SW 565-B3L2 6-8K
SW 566 B3K2 6-8K

-Address Bus

RL 103
RL 104
RL 205
RL 206

-STORAGE ADDRESS BITS

SW410

-Address Bits	
13	B2B6D04
12	B2B6C04
11	B2B6B04
10	B2B6A04
9	B2A6E04
8	B2A6D04
7	B2B6D02
6	B2B6C02
5	B2B6B02
4	B2B6A02
3	B2N6A04
2	B2A6E02
1	B2A6D02
P1-7	B2Q6B04
P8-13	B2Q6C04

SW410

-Address Bits	
13	B3A2B13
12	B3A2B12
11	B3A2B11
10	B3A2B10
9	B3A2B09
8	B3A2B08
7	B3A2B07
6	B3A2B06
5	B3A2B05
4	B3A2B04
3	B3A2D03
2	B3A2B03
1	B3A2B02
P1-7	B3R1C11
P8-13	B3R1D11

Trilead SW400/410/420

Storage Bits	Test Points	Write Bus	
0	B2B6E02		0
1	B2C6A02	B	1
2	B02	Y	2
3	C02	T	3
4	D02	E	4
5	B2C6E02		5
6	B2B6E04	0	6
7	B2C6A04		7
P	B2C6B04	SA	P
0	B2D6E02		0
1	B2E6A02	B	1
2	B02	Y	2
3	C02	T	3
4	D02	E	4
5	B2E6E02		5
6	B2F6A02	1	6
7	B2F6B02		7
P	B2F6C02	SB	P
0	B2C6C04		0
1	D04	B	1
2	E04	Y	2
3	B2D6E04	T	3
4	B2E6A04	E	4
5	B04		5
6	C04	2	6
7	B2E6D04		7
P	B2E6E04	SC	P
0	B2F6D02		0
1	E02	B	1
2	B2G6A02	Y	2
3	B2F6A04	T	3
4	B04	E	4
5	C04		5
6	D04	3	6
7	B2F6E04		7
P	B2G6A04	SD	P

Trilead SW 400/410/420

Storage Bits	Test Points	Write Bus	
0	B3F1A13		0
1	B13	B	1
2	C13	Y	2
3	D13	T	3
4	B3F1E13	E	4
5	B3G1A13		5
6	B3F1A11	0	6
7	B11		7
P	B3F1C11	SA	P
0	B3H1A13		0
1	B13	B	1
2	C13	Y	2
3	D13	T	3
4	E13	E	4
5	B3J1A13		5
6	B13	1	6
7	C13		7
P	B3J1D13	SB	P
0	B3F1D11		0
1	E11	B	1
2	B3G1A11	Y	2
3	B3H1A11	T	3
4	B11	E	4
5	C11		5
6	D11	2	6
7	B3H1E11		7
P	B3J1A11	SC	P
0	B3J1E13		0
1	K1A13	B	1
2	K1B13	Y	2
3	J1B11	T	3
4	J1C11	E	4
5	J1D11		5
6	J1E11	3	6
7	B3K1A11		7
P	B3K1B11	SD	P

Trilead SW470

Bit	Test Points	Read Bus	
0	B3M1E11		0
1	B3N1A11	B	1
2	B11	Y	2
3	C11	T	3
4	D11	E	4
5	B3N1E11		5
6	B3P1E11	0	6
7	B3Q1A11		7
P	B3Q1B11	SA	P
0	B3M1E13		0
1	B3N1A13	B	1
2	B13	Y	2
3	C13	T	3
4	D13	E	4
5	B3N1E13		5
6	B3M1B11	1	6
7	C11		7
P	B3M1D11	SB	P
0	B3L1D13		0
1	E13	B	1
2	B3M1A13	Y	2
3	B13	T	3
4	C13	E	4
5	D13		5
6	B3L1D11	1	6
7	E11		7
P	B3M1A11	SC	P
0	B3P1E13		0
1	B3Q1A13	B	1
2	B13	Y	2
3	C13	T	3
4	D13	E	4
5	B3Q1E13		5
6	Q1C11	2	6
7	D11		7
P	B3Q1E11	SD	P

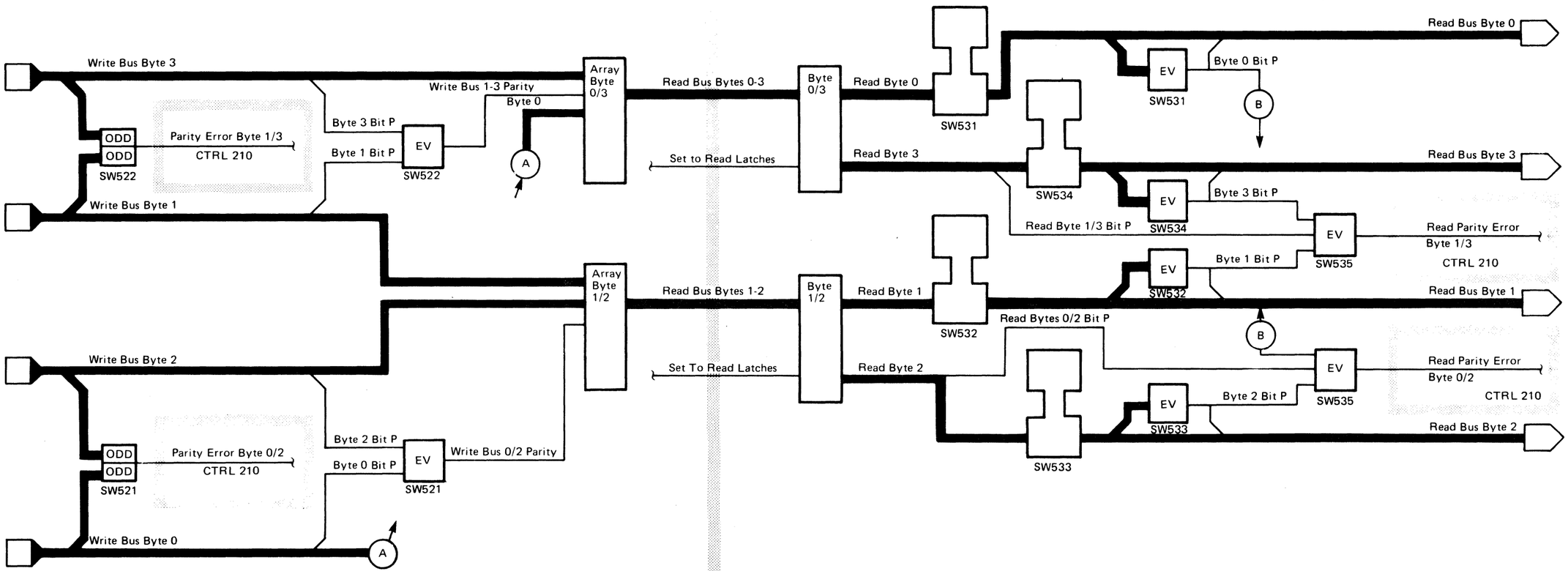
Trilead SW470

Bit	Test Points	Read Bus	
0	B2J6B04		0
1	C04	B	1
2	D04	Y	2
3	B2J6E04	T	3
4	B2K6A04	E	4
5	B2K6B04		5
6	B2L6D04	0	6
7	B2L6E04		7
P	B2M6A04	SA	P
0	B2J6B02		0
1	C02	B	1
2	D02	Y	2
3	B2J6E02	T	3
4	B2K6A02	E	4
5	B2K6B02		5
6	B2H6D04	1	6
7	B2H6E04		7
P	B2J6A04	SB	P
0	B2H6A02		0
1	B02	B	1
2	C02	Y	2
3	D02	T	3
4	B2H6E02	E	4
5	B2J6A02		5
6	B2H6A04	2	6
7	B04		7
P	B2H6C04	SC	P
0	B2L6D02		0
1	B2L6E02	B	1
2	B2M6A02	Y	2
3	B02	T	3
4	C02	E	4
5	D02		5
6	B04	3	6
7	C04		7
P	B2M6D04	SD	P

CONTROL STORAGE ECD

- Shows flow of data into and out of the control storage array.
- See CTRL 620 for details of array check circuits.

WRITE BUS PARITY **READ**



1. Determine Fault Symptom Code from chart on FSI 5.
2. Using the Fault Symptom Code, find the corresponding line in the Fault Symptom Index. Take action indicated.
3. Refer to START 900-911 for data flow by card and common card information.
4. Refer to LGND section for logic symbology, voltage levels, etc.

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

FAULT SYMPTOM CODE	ERROR DESCRIPTION	ACTION REQUIRED: FIELD REPLACEABLE UNITS in order of probability of failure			MAP ENTRY	SUGGESTED MICRODIAGNOSTIC
3381	Error detected in Special Operation decode circuitry.	B1U4	B2H2	B2L2 B2F2	PANEL 40	84
3382	Error detected in status register or CH/CL branch circuitry.	B2L2	B2F2	B1Q2	PANEL 40	86
				B2M4		
3384	Error detected in CB Odd decode circuitry.	B2J2 B2P2	B1E2 B1L2	B2E2 B2F2	PANEL 40	82
		B2H2 B2M4	B1F2 B1M2	B2G2 B2D2		
3388	Error detected in CB Even decode circuitry.	B2J2 B1G2 B2T2	B1M2 B1F2	B2D2 B2F2	PANEL 40	82
			B1E2 B1L2	B2G2 B2E2		
338C	Error detected in CB Even/Odd decode circuitry.	B2J2	B2G2 B2N2		PANEL 40	
3390	Error detected in CA Odd decode circuitry.	B2K2	B1L2	B1E2	PANEL 40	82
				B1M2		
33A0	Error detected in CA Even decode circuitry.	B2K2	B1F2	B1M2	PANEL 40	82
33B0	Error detected in CA Even/Odd decode circuitry.	B2K2	B2N2		PANEL 40	82

CU CE PANEL REGISTERS / SENSE BYTE: FORMAT = 7; CHECK 1 REGISTER BITS 0-7 = 10; CHECK 1 REGISTER BITS 8-15 = 11

Byte 7: bits 0–3 FORMAT, bits 4–7 MESSAGE.
Byte 10: 0 ON=EARLY/OFF=LATE CLOCK; 1 CA DECODE EVEN; 2 CA DECODE ODD; 3 CB DECODE EVEN; 4 CB DECODE ODD; 5 BRANCH/STATUS ERR; 6 SPECIAL OPERATION ERR.
Byte 11: 9 (Stor.) READ 'P' ERROR 0/2; 10 (Stor.) READ 'P' ERROR 1/3; 12 CU CYCLE ERROR; 13 CD DECODE ERROR.

FAULT SYMPTOM CODE	7:0	7:1	7:2	7:3	7:4	7:5	7:6	7:7	10:0	10:1	10:2	10:3	10:4	10:5	10:6	10:7	11:8	11:9	11:10	11:11	11:12	11:13	11:14	11:15
3381	0	0	1	1	0	0	0	0	1	0	0	0	0	0		1		0	0		0	0		
3382	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	0		0	0		0	0		
3384	0	0	1	1	0	0	0	0	1	0	0	0	0	1	0	0		0	0		0	0		
3388	0	0	1	1	0	0	0	0	1	0	0	0	1	0	0	0		0	0		0	0		
338C	0	0	1	1	0	0	0	0	1	0	0	0	1	1	0	0		0	0		0	0		
3390	0	0	1	1	0	0	0	0	1	0	0	1	0	0	0	0		0	0		0	0		
33A0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	0	0		0	0		0	0		
33B0	0	0	1	1	0	0	0	0	1	0	1	1	0	0	0	0		0	0		0	0		

FAULT SYMPTOM INDEX – FORMAT 3

1. Determine Fault Symptom Code from chart on FSI 5.
2. Using the Fault Symptom Code, find the corresponding line in the Fault Symptom Index. Take action indicated.
3. Refer to START 900-911 for data flow by card and common card information.
4. Refer to LGND section for logic symbology, voltage levels, etc.

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

FAULT SYMPTOM CODE	ERROR DESCRIPTION	ACTION REQUIRED: FIELD REPLACEABLE UNITS in order of probability of failure			MAP ENTRY	SUGGESTED MICRODIAGNOSTIC
3402	MPL File Not Ready. Can be caused by: 1. DC Ready. 2. IMPL switch. 3. Failure to receive or count sector pulses during IMPL operation.	B2S2	B1S2	B1T4	MPL 30	
			B2P2			
3408	Control storage address bus failure detected in the control storage board.	B3U2	B3C2 B2C2	B2H2 B2K2	FSI 32	88
3410	Error detected on control storage write bus bytes 1 or 3				PANEL 40	88
	1. If SCU stopped with error, display SB and SD Registers and use table below:					
	SB Register Parity / SD Register Parity					
	Odd / Even	B2E2	B2L2	B1E2 B1N2		
	Odd / Odd	B2E2	B2C2	B3D2		
	Even / Odd	B2E2	B2J2	B1N2		
	Even / Even	B1N2	B1E2			
	2. If not stopped with error replace cards listed.	B2E2 B1N2	B2C2 B2J2	B1E2 B2K2		
		B1P2 A1G2	B3D2 B2L2	B2S2 B2G2		
3420	Error detected on control storage write bus bytes 0 or 2				PANEL 40	88
	1. If SCU stopped with error, display SA and SC registers and use table below:					
	SA Register Parity / SC Register Parity					
	Even / Odd	B2D2 B2G2	B2L2 B2H2	B2J2 B1N2		
	Odd / Odd	B2D2	B2B2	B3D2		
	Odd / Even	B2D2	B2H2	B1N2		
	Even / Even	B1N2	B1E2			
	2. If not stopped with error replace cards listed	B2D2 B2B2	B2G2 B1N2	B1E2 B3D2		
		B2J2 B1P2	B2K2 B2J2	B2L2, B2H2 B2S2		

CU CE PANEL REGISTERS / SENSE BYTE

FAULT SYMPTOM CODE	FORMAT (Sense byte 7) bit 0	1	2	3	4	5	6	7	CHECK 1 REGISTER BITS 0-7 (Sense byte 10) bit 0 ON=EARLY/OFF=LATE	1 CLOCK	2 CS FIELD OR STAT SET	3	4 A REGISTER PARITY	5 B REGISTER PARITY	6 ALU CHECK	7 MPL PARITY ERROR	CHECK 1 REGISTER BITS 8-15 (Sense byte 11) bit 8 STOR. ADD. BUS 0-7 ERR	9 STOR. ADD. BUS 8-15 ERR	10 STOR. WRT. BUS BYTES 0/2	11 STOR. WRT. BUS BYTES 1/3	12 STOR. ADDRESS BUS 1-13	13	14 MPL NOT READY	15
3402									0	0	0		0	0	0	0	0	0	0	0	0	0	1	
3408	0	0	1	1	0	0	0	0	0	0							0	0			1	0	0	
3410	0	0	1	1	0	0	0	0	0	0							0	0	0	1	0	0	0	
3420	0	0	1	1	0	0	0	0	0	0							0	0	1	0	0		0	

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1. Determine Fault Symptom Code from chart on FSI 5.
2. Using the Fault Symptom Code, find the corresponding line in the Fault Symptom Index. Take action indicated.
3. Refer to START 900-911 for data flow by card and common card information.
4. Refer to LGND section for logic symbology, voltage levels, etc.

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

CU CE PANEL REGISTERS	FORMAT	CHECK 1 REGISTER BITS 0-7	CHECK 1 REGISTER BITS 8-15				
SENSE BYTE	7	10	11				

Sense byte bit names: Byte 7 bits 0-3 FORMAT, bits 4-7 MESSAGE; Byte 10 bit 0 ON=EARLY/OFF=LATE, bit 1 CLOCK, bit 2 CS FIELD OR STAT SET, bit 4 A REGISTER PARITY, bit 5 B REGISTER PARITY, bit 6 ALU CHECK, bit 7 MPL PARITY ERROR; Byte 11 bit 8 STOR.ADD.BUS 0-7 ERR, bit 9 STOR.ADD.BUS 8-15ERR, bit 10 STOR.WRT BUS BYTES 0/2, bit 11 STOR.WRT BUS BYTES 1/3, bit 12 STOR. ADDRESS BUS 1-13, bit 14 MPL NOT READY.

FAULT SYMPTOM CODE	ERROR DESCRIPTION	ACTION REQUIRED – FIELD REPLACEABLE UNITS in order of probability of failure			MAP ENTRY	SUGGESTED MICRODIAGNOSTIC	7:0	7:1	7:2	7:3	7:4	7:5	7:6	7:7	10:0	10:1	10:2	10:3	10:4	10:5	10:6	10:7	11:8	11:9	11:10	11:11	11:12	11:13	11:14	11:15	FAULT SYMPTOM CODE
3430	Write bus 0/2 and 1/3 error	B2Q2	B3D2	B1N2	PANEL 40	88	0	0	1	1	0	0	0	0	0	0							0	0	1	1	0		0		
			B1P2 B2B2	B2S2 B2C2																											
3440 3448	If Sense Byte 10, bit 5 on, refer to Symptom 3504.				PANEL 40	88	0	0	1	1	0	0	0	0	0	0				0			0	1					0		
	1. If error occurs only when loading IAR from CE panel, do following; Load ACR with all zeros and then all ones. If all bits correct replace cards. Otherwise, suspect low order Address Entry rotary Switches.	B2H2	B2T2	B1F2																											
	2. If failure occurs during IMPL replace cards listed.	B2S2	B2H2	B2T2 B1F2																											
	3. None of above symptoms: replace cards listed.	B2H2	B2T2 B2N2	B2K2 B2J2																											
		B2P2 B1S2	B2L2 B1F2	B2C2 B2S2																											

FAULT SYMPTOM INDEX – FORMAT 3

1. Determine Fault Symptom Code from chart on FSI 5.
2. Using the Fault Symptom Code, find the corresponding line in the Fault Symptom Index. Take action indicated.
3. Refer to START 900-911 for data flow by card and common card information.
4. Refer to LGND section for logic symbology, voltage levels, etc.

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

FAULT SYMPTOM CODE	ERROR DESCRIPTION	ACTION REQUIRED: FIELD REPLACEABLE UNITS in order of probability of failure			MAP ENTRY	SUGGESTED MICRODIAGNOSTIC
3480 3488	1. If error occurs only when loading IAR from CE Panel, Load ACR with all zeros and then all ones. If all bits correct replace cards. Otherwise, suspect high order Address Entry rotary switches.	B2T2	B2K2		PANEL 40	98
	2. If failure occurs during IMPL replace cards listed.	B2K2	B2T2			
	3. None of above symptoms replace cards listed.	B2K2	B2J2 B2T2	B2N2 B2B2		
			B2S2	B2H2		
34C0 34C8	Error detected on control storage address bus 0-7 and 8-15.	B2T2	B2N2	B2H2 B2S2	PANEL 40	98
				B2J2 B2L2		
3501	MPL parity error detected. 1. If this is only MPL disk failing with this symptom, try reseating disk. If failure persists, suspect bad disk. 2. If more than one MPL disk fails and card replace doesn't fix: a. Suspect cables to and from 23FD. b. Suspect 23FD motor speed (belt). c. Check 23FD adjustments; see 23FD section.	B1S2	B2S2 B2N2	B1T4 B2F2	MPL 15,45	
				B1M2		
3502	ALU failure	B1N2	B1H2	B1J2 B1S2	PANEL 40	86
		B2Q2	B2N2	B2T2 B2S2		

CU CE PANEL REGISTERS / SENSE BYTE: FORMAT = sense byte 7; CHECK 1 REGISTER BITS 0-7 = sense byte 10; CHECK 1 REGISTER BITS 8-15 = sense byte 11.

Bit names: Format bits 0-3 FORMAT; bits 4-7 MESSAGE. Check 1 register: 0 ON=EARLY/OFF=LATE; 1 CLOCK; 2 CS FIELD OR STAT SET; 4 A REGISTER PARITY; 5 B REGISTER PARITY; 6 ALU CHECK; 7 MPL PARITY ERROR; 8 STOR ADD BUS 0-7 ERR; 9 STOR ADD BUS 8-15 ERR; 10 STOR WRT BUS BYTES 0/2; 11 STOR WRT BUS BYTES 1/3; 12 STOR. ADDRESS BUS 1-13; 14 MPL NOT READY.

FAULT SYMPTOM CODE	Format 0	1	2	3	4	5	6	7	Check 1 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
3480 3488	0	0	1	1	0	0	0	0	0	0							1	0					0	
34C0 34C8	0	0	1	1	0	0	0	0	0	0							1	1						
3501									0	0	0		0	0	0	1	0	0	0	0	0	0	0	
3502	0	0	1	1	0	0	0	0	0	0	0		0	0	1	0	0	0	0	0	0			

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1. Determine Fault Symptom Code from chart on FSI 5.
2. Using the Fault Symptom Code, find the corresponding line in the Fault Symptom Index. Take action indicated.
3. Refer to START 900-911 for data flow by card and common card information.
4. Refer to LGND Section for logic symbology, voltage levels, etc.

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

CU CE PANEL REGISTERS	FORMAT	CHECK 1 REGISTER BITS 0-7	CHECK 1 REGISTER BITS 8-15			
SENSE BYTE	7	10	11			

FAULT SYMPTOM CODE	ERROR DESCRIPTION	ACTION REQUIRED: FIELD REPLACEABLE UNITS in order of probability of failure	MAP ENTRY	SUGGESTED MICRODIAGNOSTIC	0 FORMAT	1	2	3	4	5	6	7 MESSAGE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	FAULT SYMPTOM CODE
													ON=EARLY/OFF=LATE	CLOCK	CS FIELD OR STAT SET		A REGISTER PARITY	B REGISTER PARITY	ALU CHECK	MPL PARITY PARITY	STOR.ADR.BUS PARITY ERROR	STOR.ADR.BUS 0/7 ERR.	STOR.WRT BUS 8-15 ERR.	STOR.WRT BUS BYTES 0/2	STOR.WRT BUS BYTES 1/3	STOR. ADDRESS BUS 1-13	MPL NOT READY	
	A parity error is detected at the B-register. 1. Determine the address of the instruction that failed. If the CU is stopped with a Check 1 error the failing address is in BAR. 2. Refer to the address list (on microfiche) to determine the format of each failing instruction. If the address is between '0400' and '05FC' (diagnostic overlay area), control storage must be displayed to determine the instruction if a diagnostic routine has been run. 3. Determine the value of the CB field (byte 1) in the address list (bits 3, 4, 5, 6 and 7 for formats A,B, or C and bits 4, 5, 6 and 7 for other formats). If more than one address failing, look for CB values that are common to a register card. If commonality is found, swap or replace the CU register card, then the external input card. (See chart.) If commonality is not found, go to step 4.		PANEL 40	82	0	0	1	1	0	0	0	0	0	0	0		0	1		0	0	0	0	0	0					
3504	4. Display several registers from the chart at right. Look for a common bit being on in each register. If a common bit is found, pull the register cards until the bit is eliminated. *Note: Register cards may be pulled with dc power on.* If the common bit is still on with all register cards pulled, swap B-register cards. Bits 0, 1, 2, 3 = B1J2 Bits 4, 5, 6, 7 = B1H2 Bit P = B1N2 5. If a common card or continuously active bit is not found, suspect the following CU cards: (Remember that swapping a faulty card with any other card in following list will produce the same Fault Symptom Code). B1H2, B1J2 – Same P/N; B1N2 B1F2, B1L2, B1M2, B1E2 – Same P/N B2D2, B2E2 – Same P/N B2F2 B1K2 B1G2 B2P2 A1M2 B1P2 B2K2 B1Q2 B1D2 B2L2 B1R2 B2U2 A1T2 B2H2 B2N2 B2J2 B2G2																											
3506	B Register and ALU failure. Refer to Symptom 3504.		PANEL 40	82	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0							

CB Field Byte 1 Bits 3 4 5 6 7		POSSIBLE FAILING UNITS 1st Choice	2nd Choice
		Register	External Input
0 0 0 0 0	SA	B2D2	B2G2, J2, H2, L2, B1E2
0 0 0 1 0	SC		B2H2, B1E2
0 0 0 0 1	SB	B2E2	B2J2, B1E2
0 0 0 1 1	SD		B2L2, B1E2
0 0 1 0 1	GA	B1E2	
0 0 1 1 1	NA		A1T2, A1U2
0 1 0 0 1	TA		B1D2
0 1 0 1 1	MA		
0 1 0 1 0	TD	B1F2	
1 0 1 0 0	ND		B1B2, Q2, D2
1 0 0 1 0	GD		
0 1 1 0 0	MD		
0 1 1 1 1	MC	B1L2	
0 1 1 0 1	GC		
1 0 1 0 1	NC		
1 0 1 1 1	TC		
0 0 1 0 0	GB	B1M2	
0 0 1 1 0	TB		
0 1 0 0 0	MB		B1Q2
1 0 1 1 0	NB		B3L2, B2H2
0 1 1 1 0	BR	B2F2	
1 0 0 0 1	ST		
1 0 0 1 1	TG		
1 1 0 0 1	GE	B1K2	
1 1 0 1 1	NE		Optional
1 1 1 0 1	TE		
1 1 1 1 1	ME		
1 1 0 0 0	GF	B1G2	
1 1 0 1 0	NF		
1 1 1 0 0	TF		
1 1 1 1 0	MF		

FAULT SYMPTOM INDEX – FORMAT 3

1. Determine Fault Symptom Code from chart on FSI 5.
2. Using the Fault Symptom Code, find the corresponding line in the Fault Symptom Index. Take action indicated.
3. Refer to START 900-911 for data flow by card and common card information.
4. Refer to LGND Section for logic symbology, voltage levels, etc.

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

CU CE PANEL REGISTERS	FORMAT	CHECK 1 REGISTER BITS 0-7	CHECK 1 REGISTER BITS 8-15				
SENSE BYTE	7	10	11				

Byte 7 bits 0-3: FORMAT; bits 4-7: MESSAGE.
Byte 10: 0 ON=EARLY/OFF=LATE, 1 CLOCK, 2 CS FIELD OR STAT SET, 4 A REGISTER PARITY, 5 B REGISTER PARITY, 6 ALU CHECK, 7 MPL PARITY ERROR.
Byte 11: 8 STOR.ADD.BUS 0-7 ERR, 9 STOR.ADD.BUS 8-15 ERR, 10 STOR.WRT BUS BYTES 0/2, 11 STOR.WRT BUS BYTES 1/3, 12 STOR. ADDRESS BUS 1-13, 14 MPL NOT READY.

FAULT SYMPTOM CODE	ERROR DESCRIPTION	ACTION REQUIRED: FIELD REPLACEABLE UNITS in order of probability of failure	MAP ENTRY	SUGGESTED MICRODIAGNOSTIC	7:0	7:1	7:2	7:3	7:4	7:5	7:6	7:7	10:0	10:1	10:2	10:3	10:4	10:5	10:6	10:7	11:8	11:9	11:10	11:11	11:12	11:13	11:14	11:15	FAULT SYMPTOM CODE
3508	1. Determine the address of the instruction that failed. If the CU is stopped with a Check 1 error, the failing address is in BAR. 2. Refer to the address list (on microfiche) to determine the format of each failing instruction. If the address is between '0400' and '05FC' (diagnostic overlay area), control storage must be displayed to determine the instruction. 3. If all failing instructions are format A,D, or E with the KK bit equal to zero, go to step 4. Otherwise, go to step 5. 4. Determine the value of the CA field (byte 0) in the address list (bits 0-3). If more than one address failing, look for CA values that are common to a register card. If commonality is found, swap or replace the suspected register card, then the external input card. 5. For all other instruction formats, or if a common card cannot be found, suspect the following CU cards. (Remember that swapping a faulty card with any other card in the following list will produce the same Fault Symptom Code). B1H2, B1J2 } Same P/N B1E2, B1M2, B1L2, B1F2 } Same P/N B1N2, B2H2, B2K2, B2L2 B1P2, B2N2, B1D2, B1R2 B1Q2, A1T2		PANEL 40	82	0	0	1	1	0	0	0	0	0	0	0		1	0		0	0	0	0	0	0				
350A	A Register and ALU failure. Refer to Symptom 3508		PANEL 40	82	0	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0									

CA Field Byte 0 (0 1 2 3)	Register Name	POSSIBLE FAILURES: 1st Choice Register	2nd Choice External Input
0 0 0 1	GC	B1L2	
0 0 1 1	NC	B1L2	
0 1 0 1	TC	B1L2	
0 1 1 1	MC	B1L2	
0 1 1 0	MD	B1F2	
0 1 0 0	TD	B1F2	
0 0 1 0	ND	B1F2	B1D2, Q2, R2
1 0 0 0	GB	B1M2	
1 0 1 0	NB	B1M2	
1 1 0 0	TB	B1M2	
1 1 1 0	MB	B1M2	B1Q2
1 0 0 1	GA	B1E2	
1 0 1 1	NA	B1E2	A1T2
1 1 0 1	TA	B1E2	
1 1 1 1	MA	B1E2	B1D2

1. Determine Fault Symptom Code from chart on FSI 5.
2. Using the Fault Symptom Code, find the corresponding line in the Fault Symptom Index. Take action indicated.
3. Refer to START 900-911 for data flow by card and common card information.
4. Refer to LGND section for logic symbology, voltage levels, etc.

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

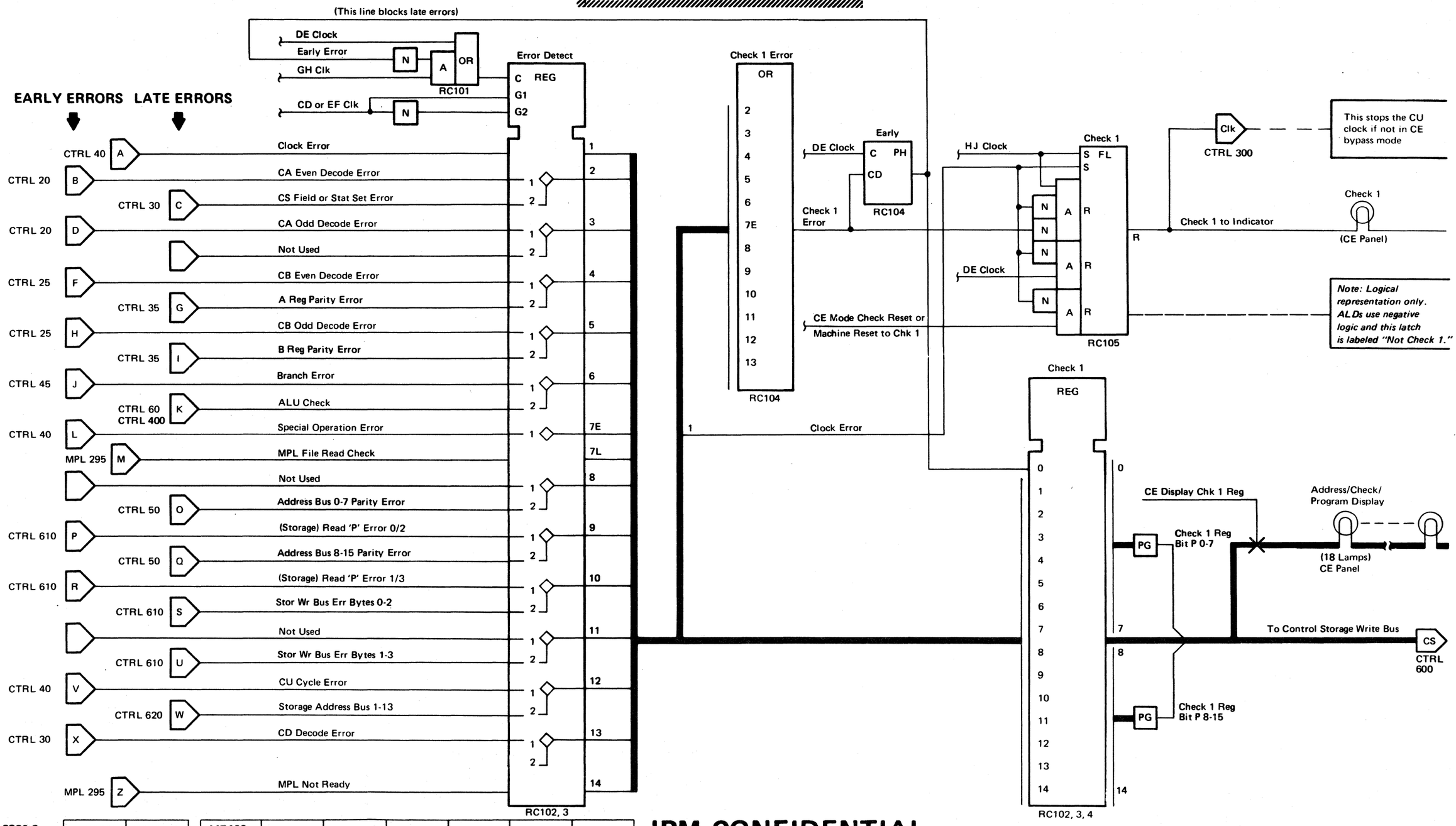
FAULT SYMPTOM CODE	ERROR DESCRIPTION	ACTION REQUIRED – FIELD REPLACEABLE UNITS in order of probability of failure			MAP ENTRY	SUGGESTED MICRODIAGNOSTIC
3520	Error detected CS field or CS decode circuitry.	B2M4	B2K2	B2N2	PANEL 40	Hardcore
3528 352A	Error detected loading A-register from CK field (byte 0).	B2K2			PANEL 40	Hardcore
3930	Check 1 Error detected, but no bits on in sense bytes 10 and 11.	B2Q2	B2C2 B2N2	B2B2 B2T2 B2M2	PANEL 40	84

CU CE PANEL REGISTERS / SENSE BYTE	FORMAT (7)								CHECK 1 REGISTER BITS 0-7 (10)								CHECK 1 REGISTER BITS 8-15 (11)							
	FORMAT				MESSAGE				ON=EARLY/OFF=LATE	CLOCK	CS FIELD OR STAT SET		A REGISTER PARITY	B REGISTER PARITY	ALU CHECK	MPL PARITY ERROR	STOR.ADD.BUS 0-7 ERR.	STOR.ADD.BUS 8-15 ERR.	STOR.WRT BUS BYTES 0/2	STOR.WRT BUS BYTES 1/3	STOR. ADDRESS BUS 1-13		MPL NOT READY	
FAULT SYMPTOM CODE	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
3520	0	0	1	1	0	0	0	0	0	0	1		0	0	0	0	0	0	0	0	0			
3528 352A	0	0	1	1	0	0	0	0	0	0	1		1	0		0	0	0	0	0	0			
3930	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CONTENTS

CTRL

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.



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CHECK 1 ERROR CONDITION DIAGRAMS (Part 1 of 8)

CA EVEN DECODE ERROR

Check 1 Register Bit 2 — Early (Bit 0 = 1)

The CA decode field (byte 0, bits 0-3) selects one or none of 15 registers to be gated onto the A-bus. The even decodes are those in which the low order bit position of the decode field (bit 3) is off.

Where the decimal value of the field is zero ('0000'), no register is selected for entry onto the A-bus.

The registers selected for even values are: 2 = ND, 4 = TD, 6 = MD, 8 = GB, 10 = NB, 12 = TB, and 14 = MB.

The decoder can select only one register, or the zero condition (no register selected), at any one time. This is an odd number of selections.

The CA even decoder checking circuitry uses an even circuit to check for an odd number of decoder outputs when the low order position of the field is a 0.

The CA even decode error is caused by either:

1. Two registers selected.
2. Register selected and the no-register-select condition present.
3. No register selected and the no-register-select condition missing.

CA ODD DECODE ERROR

Check 1 Register Bit 3 — Early (Bit 0 = 1)

The CA decode field (byte 0, bits 0-3) selects one or none of 15 registers to be gated onto the A bus. The odd decodes are those in which the low order bit position of the decode field (bit 3) is on.

Where the decimal value of the field is zero ('0000') no register is selected for entry onto the A bus.

The registers selected for odd values are: 1 = GC, 3 = NC, 5 = TC, 7 = MC, 9 = GA, 11 = NA, 13 = TA, and 15 = MA.

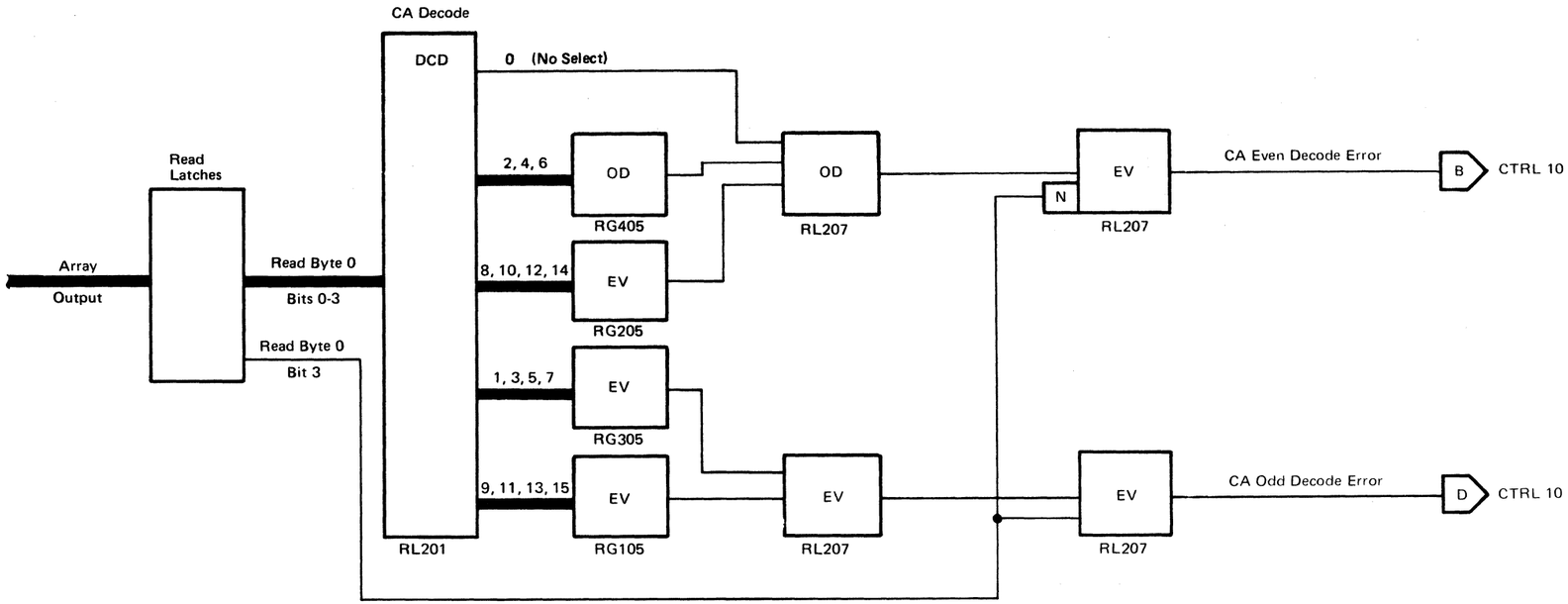
The decoder can select only one register, or the zero condition (no register selected), at any one time. This is an odd number of selections.

The CA odd decoder checking circuitry uses an even circuit to check for an odd number of decoder outputs when the low order position of the field is a 1.

The CA odd decode error is caused by either:

1. Two registers selected.
2. Register selected and the no-register-select condition present.
3. No register selected and the no-register-select condition missing.

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.



CHECK 1 ERROR CONDITION DIAGRAMS (Part 2 of 8)

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

CB EVEN DECODE ERROR

Check 1 Register Bit 4 — Early (Bit 0 = 1)

The CB decode field (byte 1, bits 3-7) selects one register, or else no register, to be gated onto the B-bus. The even decodes are those in which the low order bit position of the decode field (bit 7) is off.

Where the decimal value of the field is 16 ('10000'), no register is selected for entry onto the B-bus.

The decoder can select only one register, or the 16 decode (no register selected), at any one time.

The CB even decoder checking circuitry uses an even circuit to check for an odd number of decoder outputs when the low order position of the field is a 0.

The CB even decode error is caused by either:

1. Two registers selected.
2. A register selected and the no-register-select condition present.
3. No register selected and the no-register-select condition missing.

CB ODD DECODE ERROR

Check 1 Register Bit 5 — Early (Bit 0 = 1)

The CB decode field (byte 1, bits 3-7) selects one register, or else no register, to be gated onto the B-bus. The odd decodes are those in which the low order bit position of the decode field (bit 7) is on.

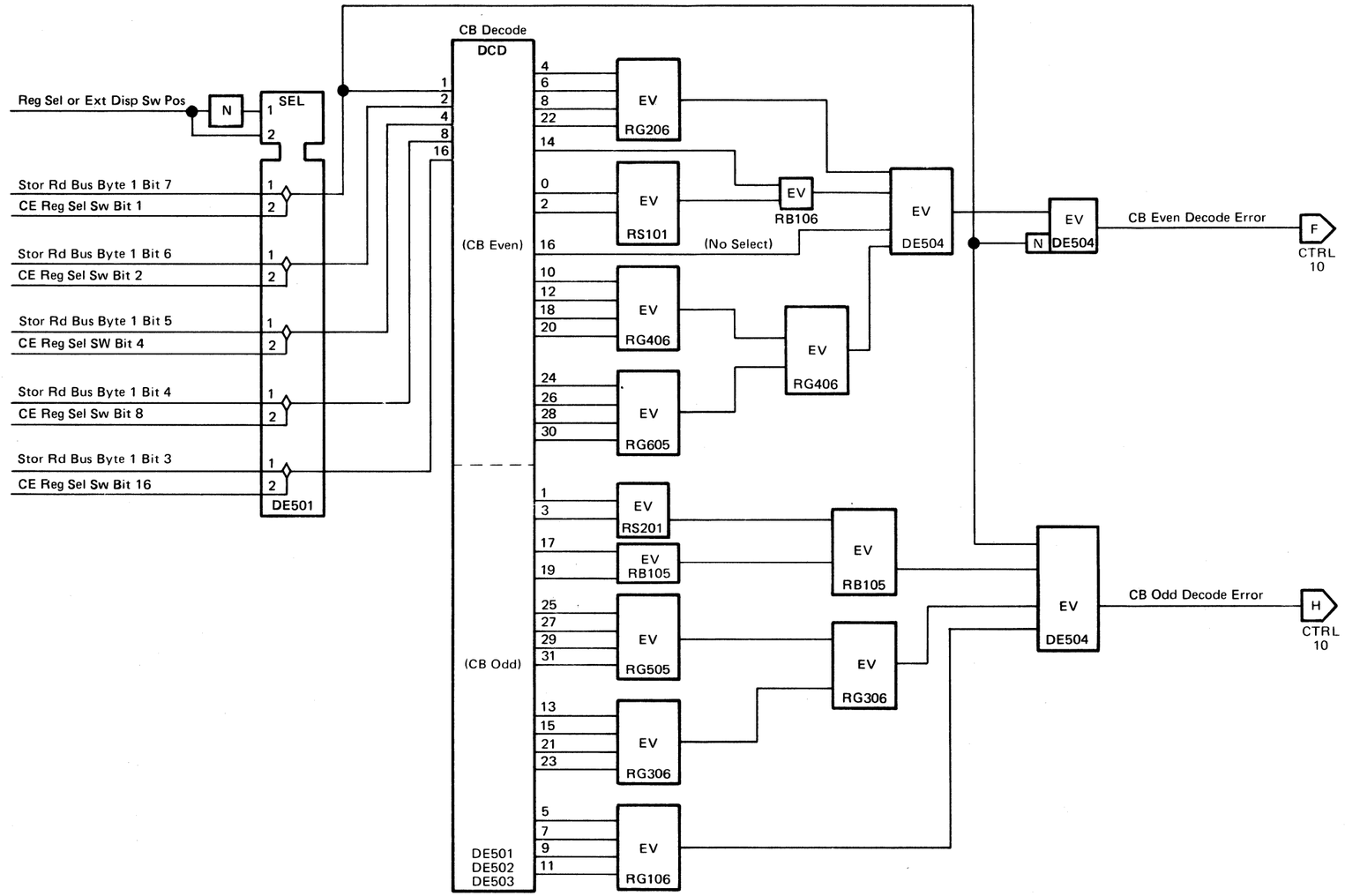
Where the decimal value of the field is 16 ('10000') no register is selected for entry onto the B-bus.

The decoder can select only one register, or the 16 decode (no register selected), at any one time.

The CB odd decoder checking circuitry uses an even circuit to check for an odd number of decoder outputs when the low order position of the field is a 1.

The CB odd decode error is caused by either:

1. Two registers selected.
2. A register selected and the no-register-select condition present.
3. No register selected and the no-register-select condition missing.



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CHECK 1 ERROR CONDITION DIAGRAMS (Part 3 of 8)

CD DECODE ERROR LATCHED

Check 1 Register Bit 13 — Early (Bit 0 = 1)

The CD Error latch is set in one of two ways.

READ BYTE 0 or 1 PARITY

The CD decoder decodes one of two 5-bit fields to select a GP register as a destination for the D bus. The field may be byte 0 bits 0-4 (format B) or byte 1 bits 3-7 (formats A, D, E, 1) according to the format of the instruction. An exclusive OR tree is used to check the parity of the selected field.

MULTIPLE CD SETS

The second part of the check uses an exclusive OR tree to count the number of GP set pulses which occur in a cycle (determines whether this is an odd or even number).

In the simplest case one set pulse should occur as a result of the block CD decode line being in its not condition. The presence of these two events, being an even number, prevents the error signal.

It may be that in a cycle one or more Gate External Data to GP Register lines are active. These lines are also counted in an exclusive OR tree and combined with the count of set pulses and the Not Block CD Decode line. For every external gate line found to be active, a corresponding set pulse should occur. These events should always total an even number.

If a data fetch cycle occurs, the data fetch cycle line is counted and matched against the resultant SA, SB, SC, SD set pulse. In a four byte fetch, another line, the data fetch 4 byte cycle, is entered into the exclusive OR tree to balance the resultant even number of set pulses (rather than the single pulse, which is an odd count).

Note that any attempt to read into the same GP register from both external gates and internal CD decodes causes an error signal because only three events are counted (only one set pulse occurs).

This checking circuit detects all single errors in the CD decoder and the set pulse selection gates.

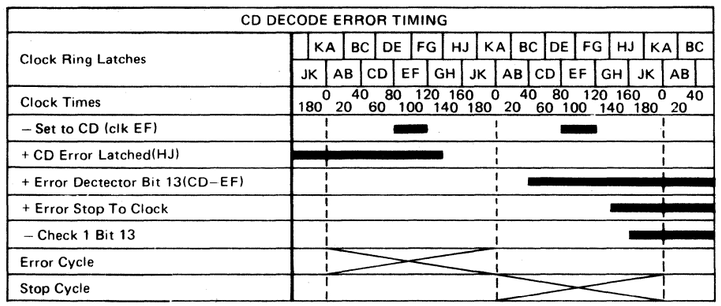
CD decode error sets the Check 1 indication one cycle after the error occurs.

CD References

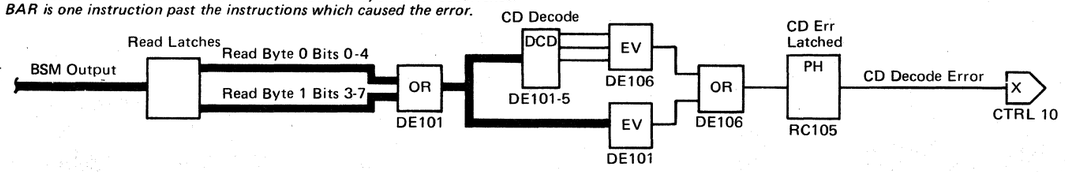
INTR 110	General
PANEL 40	Check 1
CTRL 225	CD Decode
CTRL 235	CD Decode
MIC 11	(Format B)

CS References

INTR 110	General
PANEL 40	Check 1
CTRL 225	CS Decode
CTRL 240	CS Decode



CD Decode Error sets Check 1 error indication one cycle after occurrence.
BAR is one instruction past the instructions which caused the error.



CS FIELD OR STATUS SET ERROR

Check 1 Register Bit 2 — Late (Bit 0 = 0)

The conditions which set this error indicator are divided into two main categories.

1. The four bits which form the CS decode field (byte 0 bits 4-7) are checked against an odd parity bit by an exclusive OR tree.

2. The set-reset lines to the status register (which also go to the duplicated status register) are checked by an exclusive OR tree against the condition which produced them. For each set-reset line active, a balancing entry into the exclusive OR tree must occur. If during a cycle the number of events being counted by the exclusive OR tree is odd, the error indication is given. The following are some permissible status register set-reset situations. (Where a line is noted as being inhibited this refers to its effect in the exclusive OR tree).

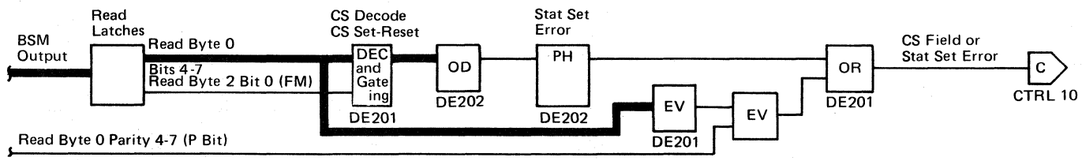
instruction cycle and not FM (CS decode active)	count 1
any one stat set-reset line active	count 1
	EVEN
store carryout and instruction cycle	count 1
stat 3 set-reset line active	count 1
	EVEN
instruction cycle and not FM (CS decode active)	count 1
any one stat set-reset line active (except 3)	count 1
store carryout and instruction cycle	count 1
stat 3 set-reset line active	count 1
	EVEN
instruction cycle and not FM (CS decode active)	count 1
CS decode equals 0 (no set-reset line produced)	count 1
	EVEN
external stat 4 set line active	count 1
stat 4 set-reset line active	count 1
	EVEN
instruction cycle and not FM (CS decode active)	count 1
stat 4 set-reset line active (produced by CS dec 8)	count 1
external stat 4 set line active (inhibited by CS dec 8)	
	EVEN
gate to stat reg CD dec 17 (read CD bus into stat reg)	
stats 0-7 set-reset lines active	count 8
	EVEN
gate to stat reg CD dec 17	
stats 0-7 set-reset lines active	count 8
external stat 4 set line active (inhibited by CD dec 17)	
	EVEN
instruction cycle and not FM (CS decode active)	count 1
stat 2 already set and CS decode 2	count 1
(stat 2 set-reset line is prevented from becoming active under these circumstances)	
	EVEN

Other information concerning the status register which may assist in the resolving of trouble in that area is the following:

Given a CS decode of 2 and stat 2 in the reset state, the stat 2 set-reset pulse occurs, but the stat is set only if the D-bus is not equal to zero.

Given a CS decode of 2 and stat 2 in the set state, no set-reset pulse occurs. The stat remains in its set state.

CD decode 17 and CS decode must not occur together. Stat 4 may be set from the external stat 4 line or set or reset from a CS dec 8. If a CD dec 17 takes place simultaneously with an external stat 4 signal, the D-bus bit 4 takes priority over the external stat 4 signal. If a CS dec 8 takes place simultaneously with an external stat 4 signal, the stat will be set (external stat 4 has priority).



CHECK 1 ERROR CONDITION DIAGRAMS (Part 4 of 8)

A-REGISTER PARITY ERROR

Check 1 Register Bit 4 — Late (Bit 0 = 0)

Any data entering the A-register must have odd parity. The A-register parity check is accomplished by an even circuit which checks for an odd number of bit positions on in the A-register (eight plus parity).

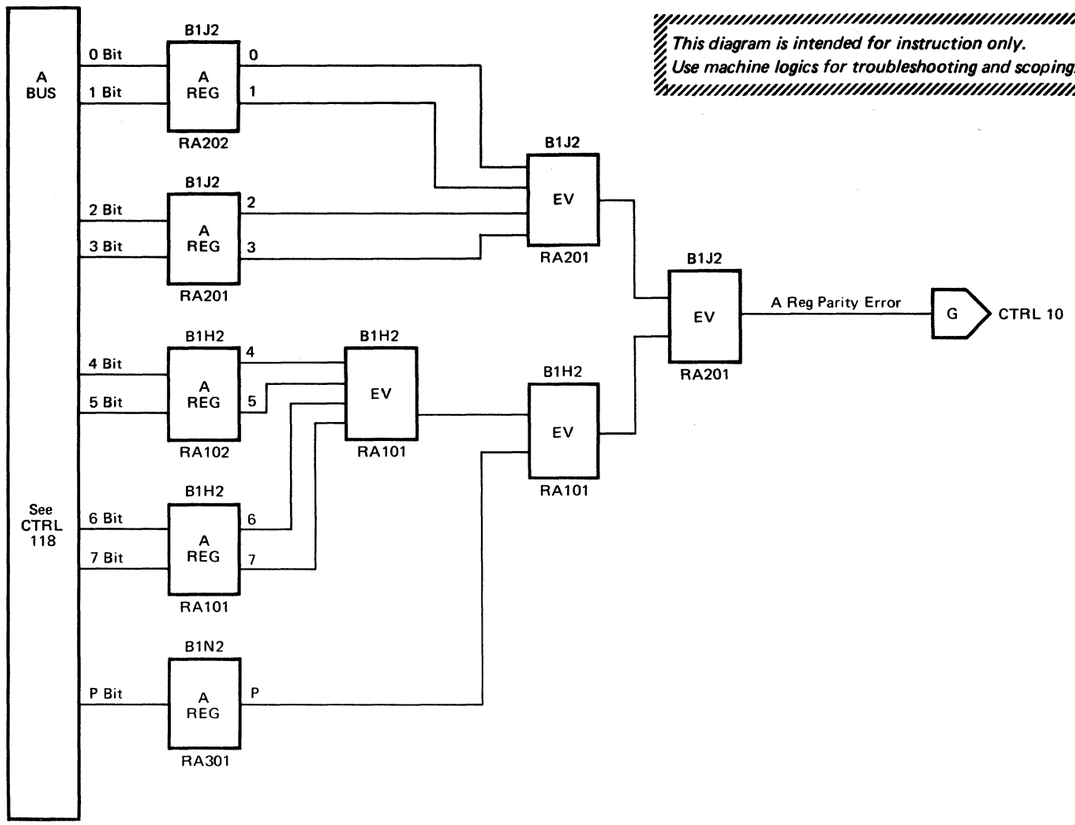
Entries to the A-register come from any of 15 general purpose registers as selected by the CA decode field, or from one of two different positions in the CK field (byte 0 from the read bus) depending on the format of the instruction.

In the case of entry from one of the general purpose registers the parity bit of the register is entered into the A-register parity bit position. Where a CA decode of zero is used, no register is selected but the A-register parity bit is automatically turned on (page RA301).

If the entire CK field is entered into the A-register (format A), the byte 0 parity bit is entered into the A-register parity bit position.

If only the high order four bits of the CK field (byte 0 bits 0-3, formats D, 1, 2) are entered into either the low or high order four bits of the A-register, the parity of these four bits is entered into the A-register parity bit position. Generation of this partial byte parity is shown on page RL105.

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.



B-REGISTER PARITY ERROR

Check 1 Register Bit 5 — Late (Bit 0 = 0)

Any data entering the B register must have odd parity. The B-register parity check is accomplished by an even circuit which checks for an odd number of bit positions on in the B-register (eight plus parity).

Entries to the B-register come from any one of 31 general purpose registers as selected by the CB decode field.

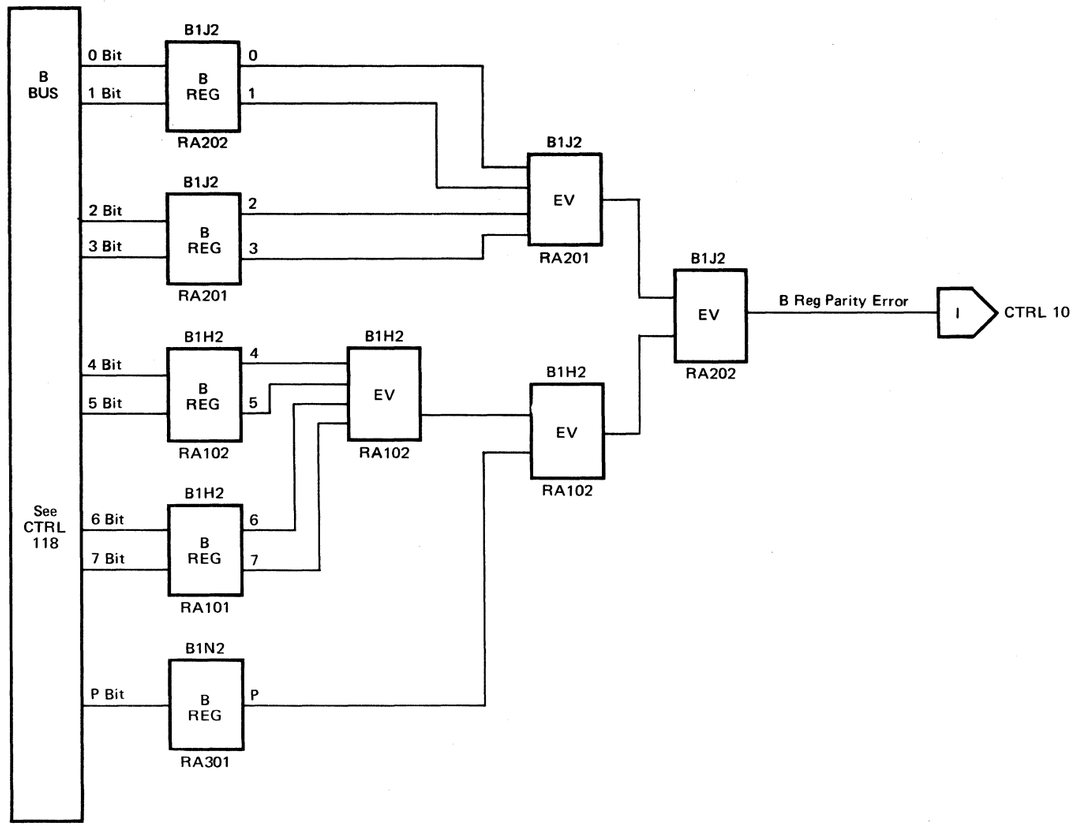
In the case of entry from one of the general purpose registers, the parity bit of the register is entered into the B-register parity bit position.

Where a CB decode of 16 is used, no register is selected but the B-register parity bit is automatically set to 1 (page RA301).

Entries into the B-register are inverted to produce a complement entry for the subtract operation. The parity bit is not inverted. The parity of an even number of bits (eight in this case) remains the same when inverted.

References

INTR 115	General
PANEL 40	Check 1
CTRL 225	Data Flow
CTRL 235	ALU Operation
CTRL 400	ALU Operation
CTRL 118	B bus Assm.



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CHECK 1 ERROR CONDITION DIAGRAMS (Part 5 of 8)

CHECK 1 ERROR CONDITION DIAGRAMS (Part 5 of 8)

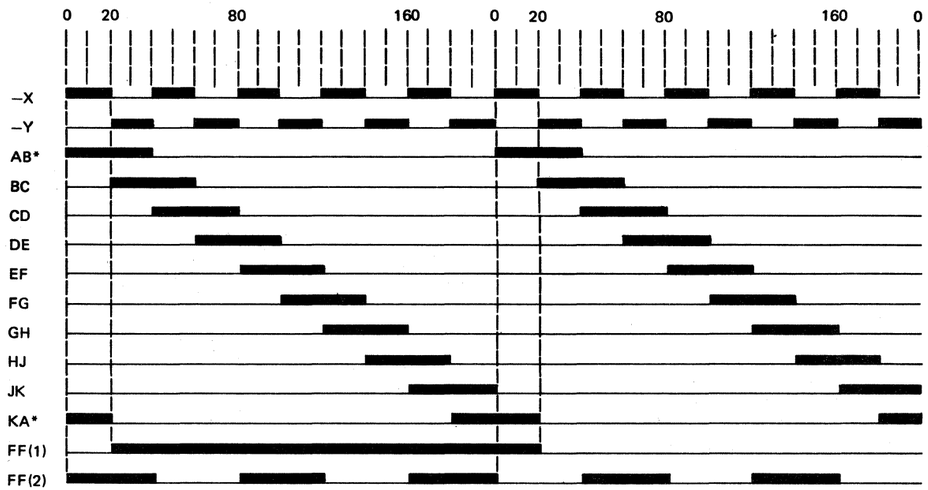
CLOCK ERROR

Check 1 Register Bit 1

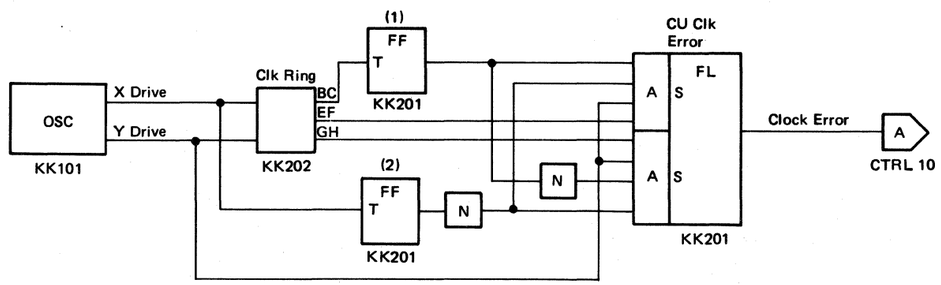
Two binary complementing flip-flops are used to detect erratic operation of the clock in a short period of time. One runs at oscillator X drive speed (complementing once every 40 ns); the other runs at cycle speed (complementing once every 200 ns). The flip-flops are arranged in a circuit sampled by oscillator Y drive, clock GH, and Clock EF.

This diagram is intended for instruction only. Use machine logics for troubleshooting and scoping.

The card containing the clock and its check is in location B2N2.



* = 'ON' when clock is stopped



CU CYCLE ERROR

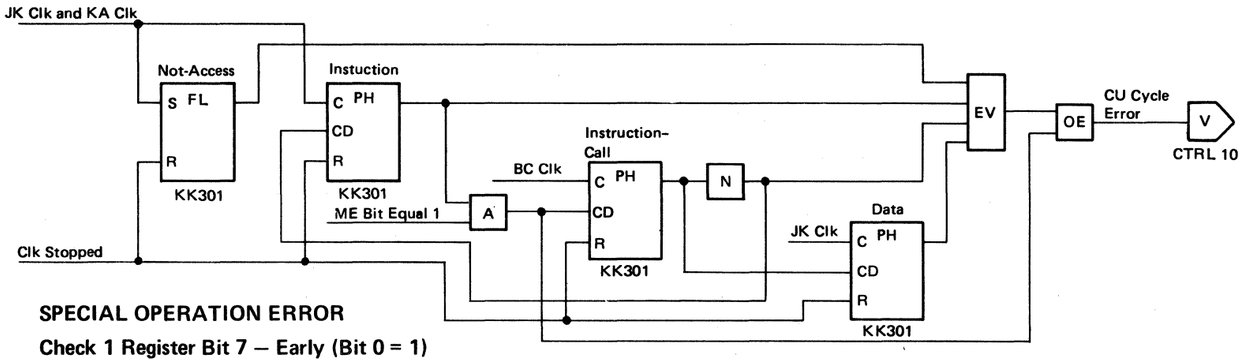
Check 1 Register Bit 12 – Early (Bit 0 = 1)

Machine cycles may be classified into one of four categories. These are access cycle, instruction cycle, instruction/call cycle, and data cycle. Four latches titled Not-Access, Instruction, Instr-Call, and Data perform the cycle control function.

The following table shows the correct condition of these latches and the ME Bit Equal 1 (fetch/store) line for each of the four cycle types.

	ME Bit=1	Not Access latch	Instruction latch	Instr-Call latch	Data latch
Access cycle (clock must be on)	0	reset	reset	reset	reset
Instruction cycle	0	set	set	reset	reset
Instruction–Call cycle	1	set	set	set	reset
Data cycle	0	set	reset	reset	set

The checking of the cycle control latches is accomplished by an exclusive OR tree which checks that the number of latches, set, plus the ME = 1 condition is an even number.



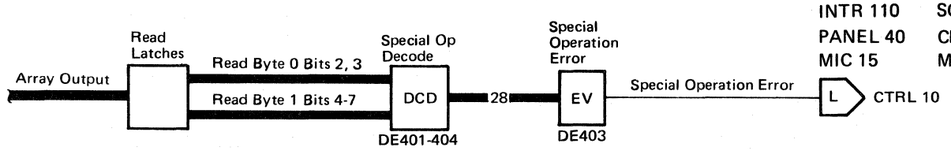
SPECIAL OPERATION ERROR

Check 1 Register Bit 7 – Early (Bit 0 = 1)

The special operation field consists of byte 0, bits 2, 3; and byte 1, bits 4-7. Of the possible 64 decoded outputs from this six-bit field, only outputs 0-24 and 26, 28, 30 are decoded. Of these outputs, 2, 11, and 12 are not used but are included in the error check circuit.

The special op decodes are active only in format F (ME, FM, KK, ND, NB = 00111). Furthermore, all decodes and checking are inhibited if byte 0, bit 2 stands at 1.

The check consists of a parity tree which checks for an odd number of decoder outputs (should be only one). The construction of the decoder is such that failure is most likely to produce no decodes or two decodes. Either of these conditions represents an even number, which the parity circuit will interpret as an error.



References

INTR 110	General
PANEL 40	Check 1
CTRL 320	Definition
CTRL 325	Timing

References

INTR 110	SCU Data Flow
PANEL 40	Check 1 Error Collection
MIC 15	Microword Format F

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CHECK 1 ERROR CONDITION DIAGRAMS (Part 6 of 8)

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

BRANCH/STATUS ERROR

Check 1 Register Bit 6 — Early (Bit 0 = 1)

The branch error indication is set by four separate checking circuits.

1. Read bus byte 3 serves as the input to two decoders. Bits 0-3 drive the CH decoder and bits 4-7 drive the CL decoder. The entire byte 3 from the read bus is checked for odd parity by even circuits.

2. The CH decoder, driven by byte 3 bits 0-3, samples any one of 14 different conditions. If the condition being sampled is true (or 1), a 1 is set into bit 12 of the instruction address register (which selects the next address). Two outputs from the decoder are not used for sampling conditions. These are the decode 1 and decode 0 outputs. The decode of 1 is placed directly in bit 12 of the IAR. The decode of 0 is tied down.

   The CH decoder is completely duplicated, with the outputs of the two decoders compared by even circuits.

   Note that although the decoders are well checked by duplication there does exist circuitry common to both in the areas being sampled.

3. The CL decoder is driven by byte 3 bits 4-7 and samples 14 different conditions. The operation of the CL decoder is is similar to that described for the CH decoder except that the result of the sample is used to set bit 13 of the IAR.

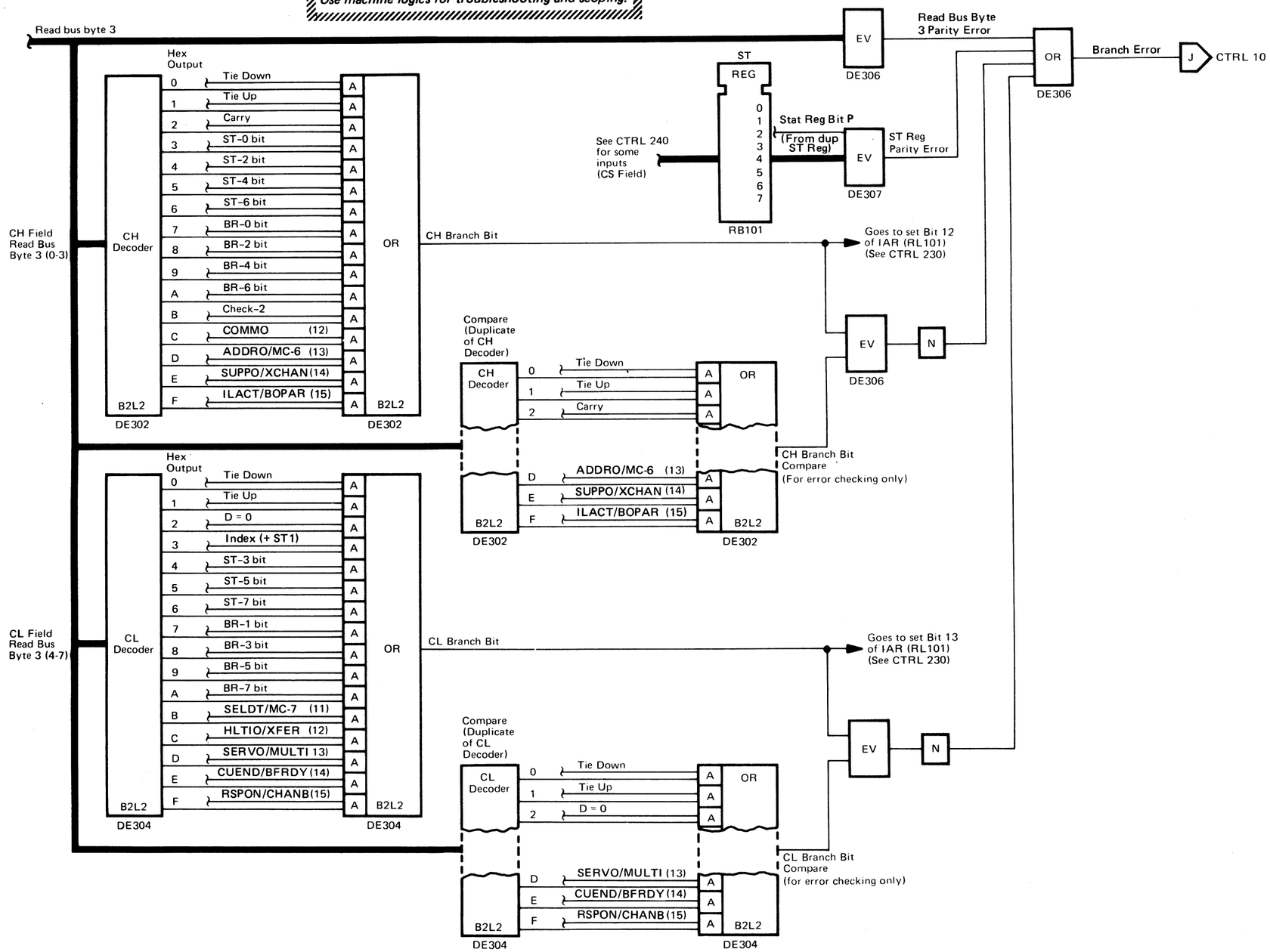
   The CL decoder is completely duplicated, with the outputs of the two decoders compared by even circuits.

   Note that although the decoders are well checked by duplication there does exist circuitry common to both in the areas being sampled.

4. Individual bits of the status register are capable of being sampled by the CH and CL decoders to establish branch conditions. The status register itself is duplicated and a parity bit is developed from it. This parity is checked against the output of the status register by even circuits.

   All single errors in the status registers will be detected but some input circuitry to the registers is common to both.

   Note that the BR register, also sampled by the CH and CL decodes, does not possess its own unique parity checking circuitry as in the case of the status register. The BR register is checked for parity only at such time that it is read onto the B-bus.



CHECK 1 ERROR CONDITION DIAGRAMS (Part 7 of 8)

ADDRESS BUS 0-7 PARITY ERROR

Check 1 Register Bit 8 — Late

The storage address bus high order byte is checked for odd parity by an even circuit.

The address being checked may originate from the DAR (Data Address Register), IAR (Instruction Address Register), CE, or IMPL circuitry.

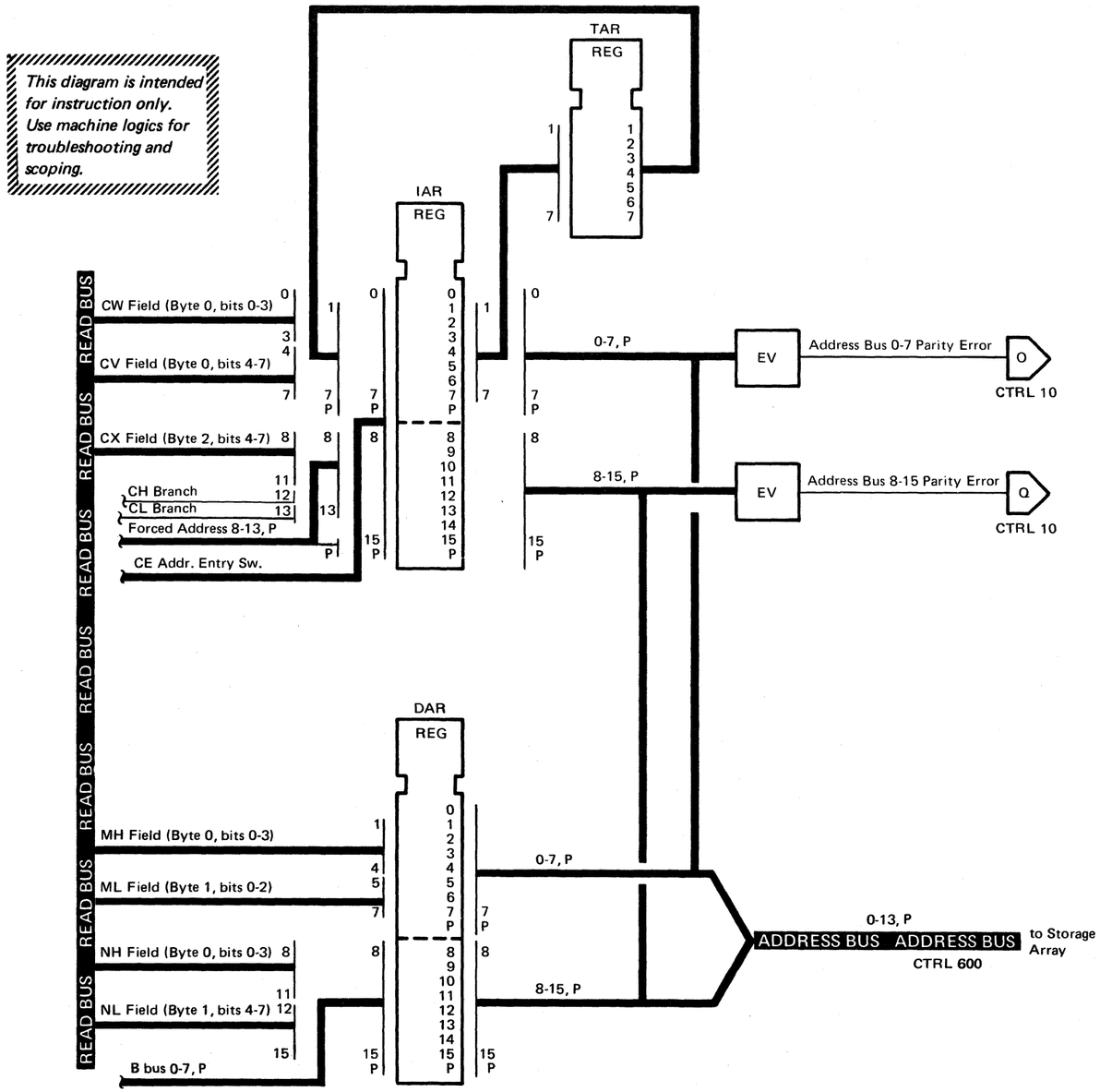
ADDRESS BUS 8-15 PARITY ERROR

Check 1 Register Bit 9 — Late

The storage address bus low order byte is checked for odd parity by an even circuit.

Note that bits 14 and 15 are checked but not sent to the storage element. These bits are used on single byte fetch operations to select one of the four bytes to place in the SA register.

The address being checked may originate from the DAR (data address register), IAR (instruction address register), CE, or IMPL circuitry.



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CHECK 1 ERROR CONDITION DIAGRAMS (Part 8 of 8)

ALU CHECK

Check 1 Register Bit 6 — Late (Bit 0 = 0)

Three different error checking circuits are ORed together to produce the ALU Check indication.

1 D Equal to Zero

At the conclusion of each arithmetic operation the result is gated onto the D-bus and a test is made for D equal to zero. The lines (0-7) are double checked by duplication of the 8-way ANDs and polarity-holds which detect and store the zero condition. If the results do not agree, the D Equal Zero Check line is raised. The duplicated circuits are located on card B1N2 and are shown on page RA302.

2 Operation Decode Check

The operation decoder provides control lines to the ALU which enable the ALU to perform eight different operations. The operation decode field is three bits wide: read bus byte 1, bits 0-2. Other entries to the operation decoder are the ME bit, which controls the decoder during store-fetch operations, and the output from ST3, which provides control for carry in on two of the arithmetic operations. No parity check occurs on the transfer of data from the read bus to the operation decoder. The decode check consists of a test for an odd number of decodes supplemented by a partial duplication of the more irregular parts of the decoder. An interconnected group of even circuits provides the necessary comparison. Any single error in the decode circuitry itself will be detected. The decoder is located on card B1N2 and is shown on page RA303.

3 D-Bus Parity Check

The output of the ALU is gated onto the D-bus, which at other times may receive data from CE switches or MPL. The D-bus is checked for correct (odd) parity by an even circuit (located on card B1N2 and shown on page RA303.) Checking the D-bus for odd parity also accomplishes the final check of all ALU arithmetic operations, which are of the parity predicting type.

The input to the ALU consists of eight bits plus parity from the A-register and the B-register, a carry-in line to the low-order position, and control lines from the operation decoder. For each of the eight operations, the parity of the result is predicted by circuitry independent of that which produced the result. Parity prediction in the ALU is accomplished as follows:

a) For the Exclusive-OR operation, the two input operand parity bits are exclusive-ORed to obtain the predicted parity.

   Par Op A exclusive-ORed with Par Op B equals the parity of the exclusive-OR sum.

b) For the Add or Subtract operation, the two input operand parity bits must be combined with a parity count of the number of individual carries which occur in the course of the addition.

   Par Op A, exclusive-ORed with Par Op B, exclusive-ORed with a parity count of all carries (including any carry in to the low-order position) equals the parity of the sum. A carry out from the high-order position sets the carry flip-flop and is not included in the count of carries.

c) For the OR operation, the two input operand parity bits must be combined with a parity count of the number of corresponding bit positions in the two operands. (Both of these corresponding bit positions contain 1s.) Positions which both contain 1s are those which would generate carries if the operation were addition. This fact allows use of the same circuitry which counts carries in the Add operation to be used in predicting parity for an OR operation. All that is required for this different operation is to suppress the entry of transmitted carries into the carry count circuitry. Transmitted carries are those produced by a carry into a position in the operand in which one, but not both, of the bit positions is on (1).

   Par Op A, exclusive-ORed with Par Op B, exclusive-ORed with the parity count of the generated (not the transmitted) carries, equals the parity of the result. A carry out from the high-order position is included in the count of carries.

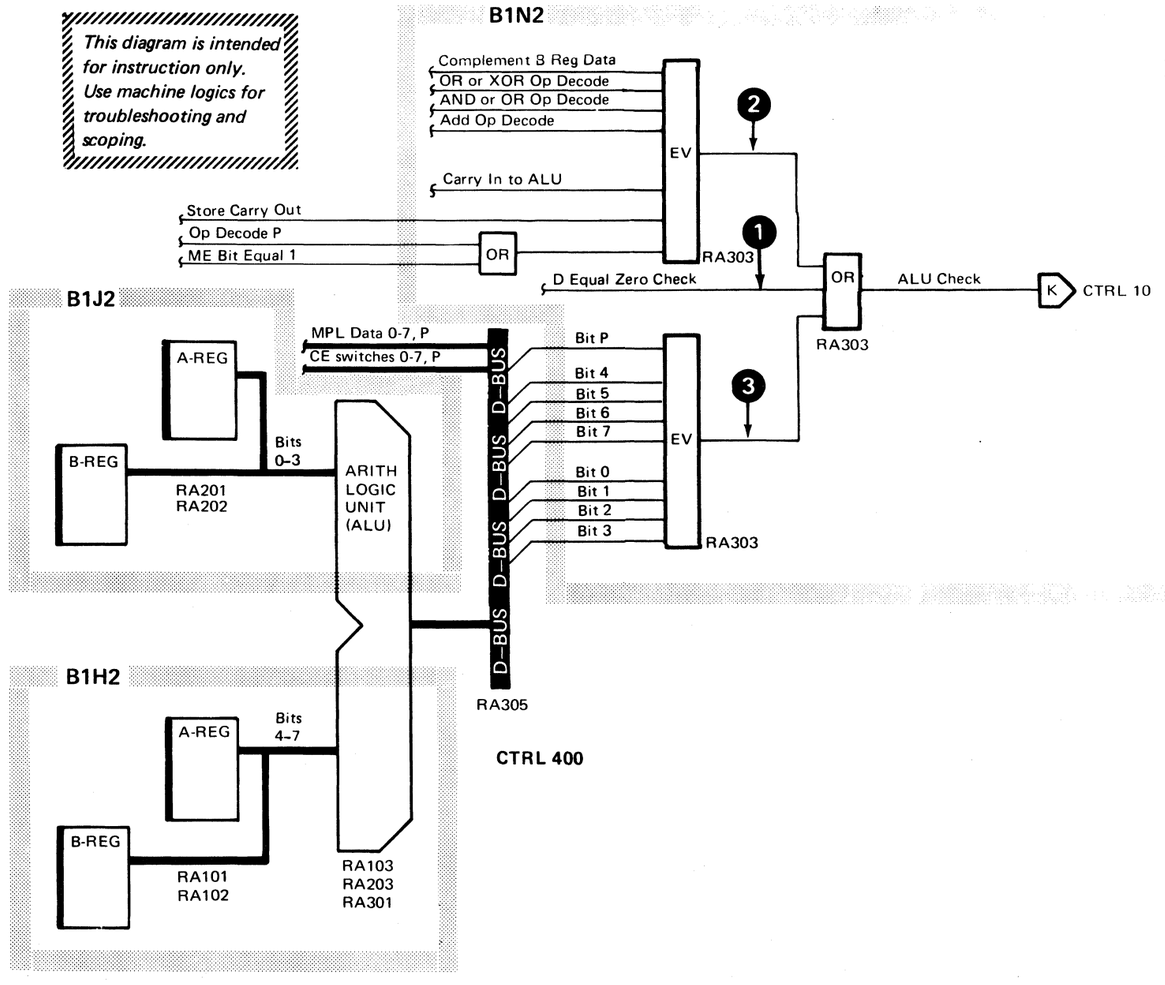
d) For the AND operation, the two operand parity bits are not used in predicting the parity of the result. (They are used, however, in checking data transfer into A- and B-registers from the sending registers.) The prediction of parity in the AND operation makes use of the same circuitry as that used in predicting the parity for OR. The parity count of the generated carries alone predicts the parity of the result. This is easily understood by noting that a 1 in the result of an AND operation stems from a 1 opposite a 1 in the two input operands. This is also the condition which produces a generated carry in addition. A carry out from the high-order position is included in the count of carries.

A feature of the adder is the self-checking of the Carry latch. This storage element is reset prior to arithmetic operations in the ALU. It is set by any carry out from the high order position of the adder on Add-Subtract operations only. The output of the carry latch is fed back into the carry count circuitry where it cancels the effect of the same carry coming directly from the last stage of the adder. Proper parity prediction in Add-Subtract requires that this end carry not be counted. Any failure of the Carry latch will interfere with the correct count and will be detected as an ALU check.

The parity predict circuitry for arithmetic operations is located primarily on card B1N2 but the actual addition and a partial count of carries occurs on cards B1J2 and B1H2. FEALD pages are RA301, RA302, and RA303 for most of the checking. The ALU check line occurs on page RA303.

Notice that incorrect transfer of information into the A- or B-registers will result in both an A or B register parity check and an ALU check for all arithmetic operations except AND.

This diagram is intended for instruction only. Use machine logics for troubleshooting and scoping.



CTRL 400

A-AND B-BUS ASSEMBLERS BLOCK DIAGRAM

- A- and B-registers are the inputs to the ALU.
- Four GP register (one card) outputs are gated and ORed to the A- or B-registers (A- and B-bus assemblers).
- A-bus is the input to A-register.
- B-bus is the input to B-register.
- A-group registers (GA, MA, TA, NA) and bus 1 (both A-bus and B-bus) are on one card, B-group registers (GB, MB, TB, NB) and bus 2 (both A-bus and B-bus) are on one card, etc.
- Example shows gating for MA register.
- Parity checking takes place on the outputs of the A- and B-registers.
- The CA decodes gate the A-bus to the A-register – (CTRL 235).
- The CB decodes gate the B-bus to the B-register – (CTRL 235).
- The CD decodes gate the D-bus to the receiving register – (CTRL 235).

SCOPE POINT REFERENCES

Registers

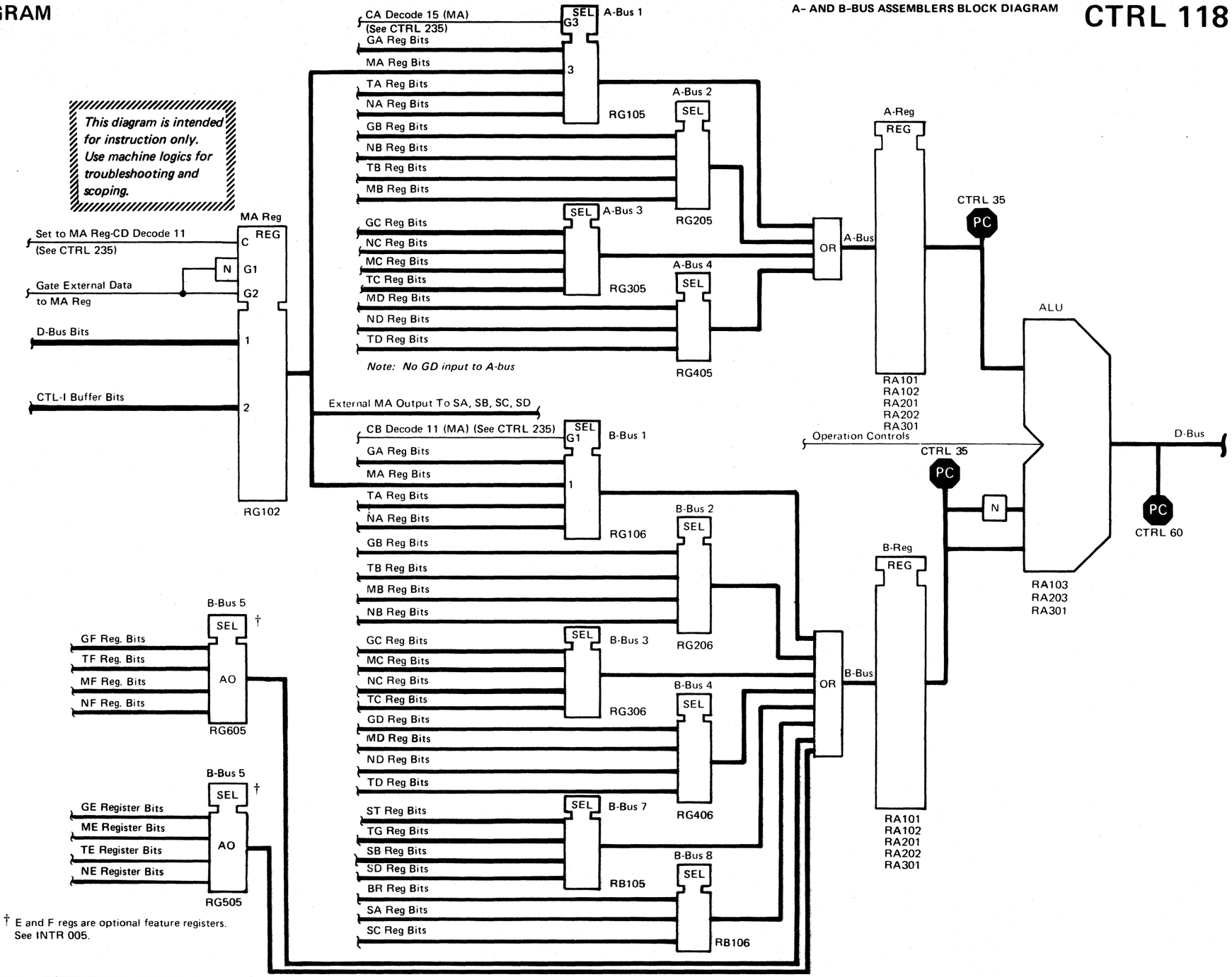
SA=RS101	TC=RG301	TE=RG501
SB=RS203	MC=RG302	ME=RG502
SC=RS103	NC=RG303	NE=RG503
SD=RS201	GC=RG304	GE=RG504
TA=RG101	TD=RG401	TF=RG601
MA=RG102	MD=RG402	MF=RG602
NA=RG103	ND=RG403	NF=RG603
GA=RG104	GD=RG404	GF=RG604
TB=RG201	ST=RB101	
MB=RG202	BR=RB103	
NB=RG203	TG=RB104	
GB=RG204		

A-Bus Assemblers

1=RG105
2=RG205
3=RG305
4=RG405

B-Bus Assemblers

1=RG106	7=RB105
2=RG206	8=RB106
3=RG306	
4=RG406	
5=RG505	
6=RG605	



† E and F regs are optional feature registers. See INTR 005.

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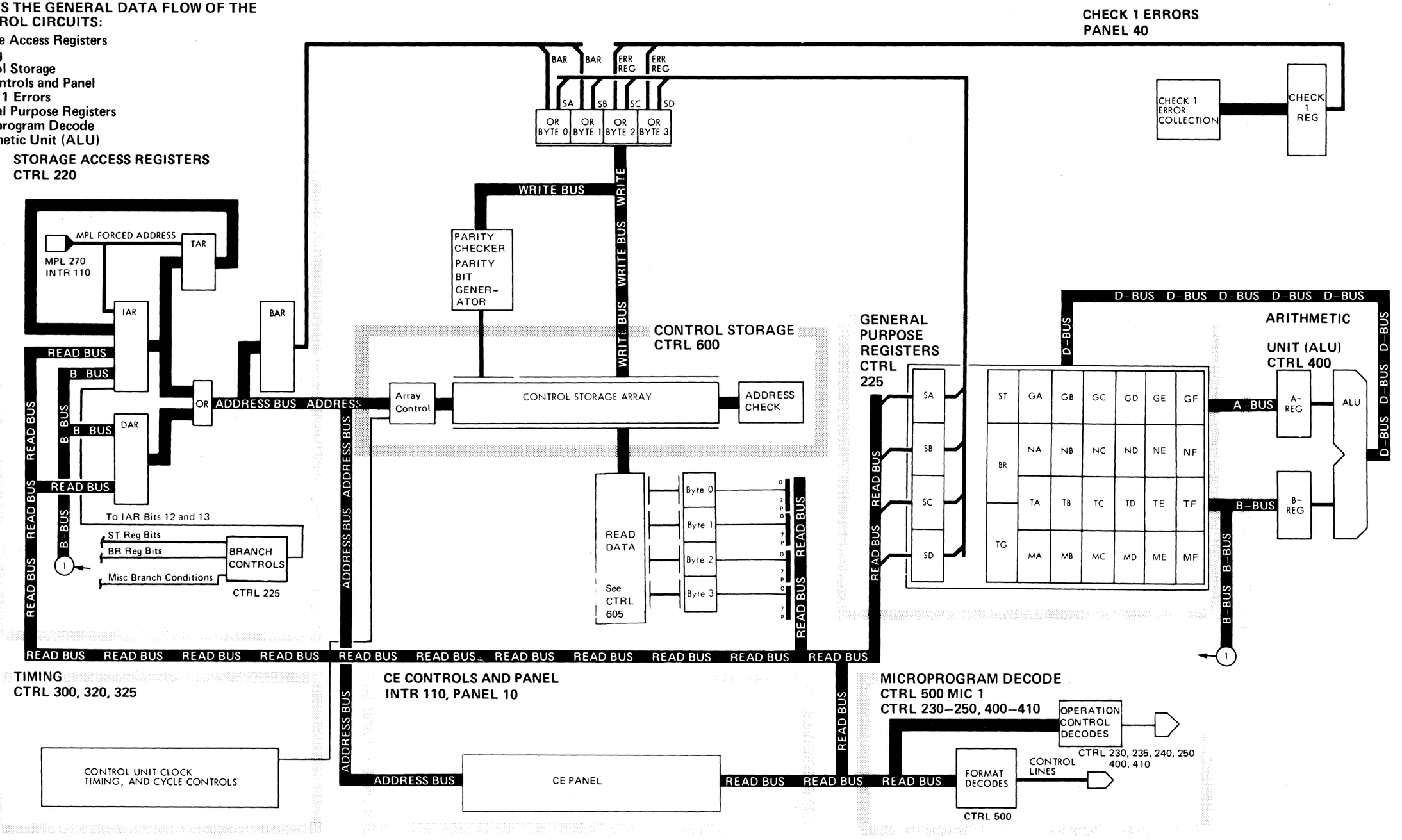
CONTROL DATA FLOW

THIS IS THE GENERAL DATA FLOW OF THE CONTROL CIRCUITS:

Storage Access Registers
Timing
Control Storage
CE Controls and Panel
Check 1 Errors
General Purpose Registers
Microprogram Decode
Arithmetic Unit (ALU)



CONTROL HARDWARE DESCRIPTION (Part 1 of 2)

- Data flow shown on CTRL 200.
- Detailed data flow diagram on INTR 100 through INTR 140.
- Control hardware – microprogram operation explained on CTRL 230 through CTRL 250.
- Control storage detailed description on CTRL 600 to 605.

STORAGE ACCESS (ADDRESSING) REGISTERS

INSTRUCTION ADDRESS REGISTER (IAR)

The IAR is effectively a 13-bit register that contains the address of the next microprogram instruction. The low-order bits are bits 8-13; the high-order bits are 1-7. Bits 14-15 are ignored since the word always contains four bytes. Therefore, the two low-order address bus bits are effectively set to 0. Bit 0 is always considered to be 0. The following table shows the various sources from which the IAR is set.

Source	IAR Bits												
	1	2	3	4	5	6	7	8	9	10	11	12	13
TAR 1-7	X	X	X	X	X	X	X						
TAR 1-4	X	X	X	X									
TAR 1-3	X	X	X										
CW Field (Byte 0, 0-3)	X	X	X										
CV Field (Byte 0, 4-7)				X	X	X	X						
CV Field (Byte 0, 5-7)					X	X	X						
CX Field (Byte 2, 4-7)								X	X	X	X		
CH Branch												X	
CL Branch													X
B Bus 0-5								X	X	X	X	X	X
Selective Reset Addr.	0	0	0	0	0	0	0	0	X	0	0	0	0
CE Addr. Entry Sw.	X	X	X	X	X	X	X	X	X	X	X	X	X

TEMPORARY ADDRESS REGISTER (TAR)

The TAR preserves the high-order part of the IAR when this part of the address does not change. The TAR also serves as a gate to the IAR when the IAR is set to an address forced by the CE panel switches or a reset.

DATA ADDRESS REGISTER (DAR)

The DAR is a 15-bit register that contains the address of a four-byte data word, which is to be fetched or stored. During one-byte fetches, bits 14-15 determine which one of the four bytes is placed in the SA register. The DAR is set during instruction-call cycles and is gated to the address bus during data cycles. The following table shows the sources that set the DAR:

Source	DAR Bits														
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MH Field (Byte 0, 0-3)	X	X	X	X											
ML Field (Byte 1, 0-2)					X	X	X								
NH Field (Byte 0, 0-3)								X	X	X	X				
NL Field (Byte 1, 4-7)												X	X	X	X
B Bus 0-7								X	X	X	X	X	X	X	X

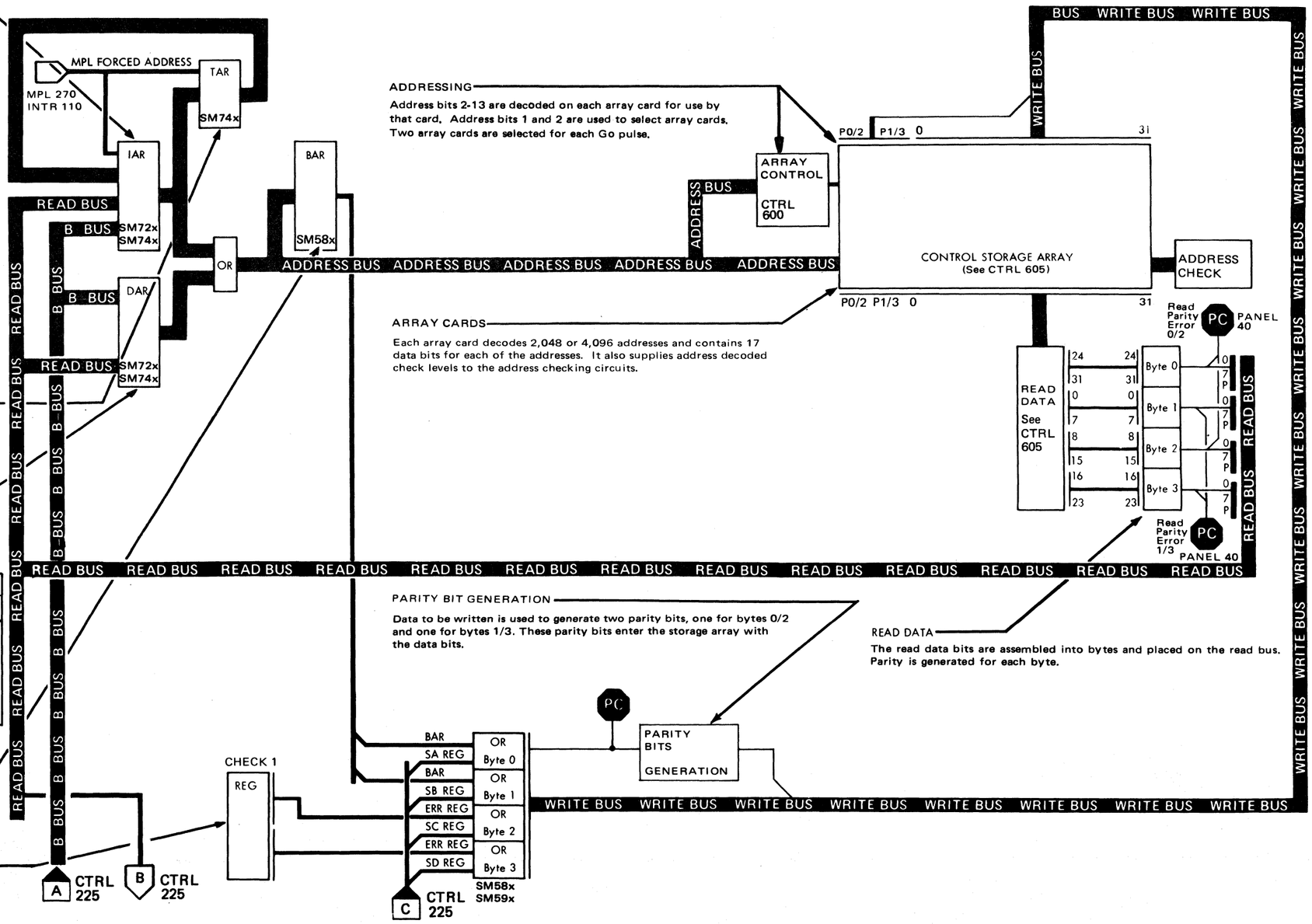
BACK UP ADDRESS REGISTER (BAR)

BAR is provided to save the contents of the IAR for the previous instruction cycle addresses.

BAR is not set during instruction-call cycles but is set during the following data cycle. BAR output is gated to the CE panel indicators and to the write data bus, bytes 0-1. Following selective reset, BAR contains the last IAR address prior to reset. BAR changes at the first data cycle.

CHECK 1 REGISTER

Check 1 errors, errors that prevent the microprogram from running correctly, are assembled in the Check 1 register. See PANEL 40 for details.



CONTROL STORAGE

ADDRESSING

Address bits 2-13 are decoded on each array card for use by that card. Address bits 1 and 2 are used to select array cards. Two array cards are selected for each Go pulse.

ARRAY CARDS

Each array card decodes 2,048 or 4,096 addresses and contains 17 data bits for each of the addresses. It also supplies address decoded check levels to the address checking circuits.

PARITY BIT GENERATION

Data to be written is used to generate two parity bits, one for bytes 0/2 and one for bytes 1/3. These parity bits enter the storage array with the data bits.

READ DATA

The read data bits are assembled into bytes and placed on the read bus. Parity is generated for each byte.

CONTROL HARDWARE DESCRIPTION (Part 2 of 2)

GENERAL PURPOSE REGISTERS

- Used by microprogram to control facility operation.
- Include branching and storage registers.

REGISTER SELECTION

The registers to be gated to the A- and B-bus and to be set by the contents of the D-bus, are selected by decodes of the CA, CB, and CD fields of the microprogram word.

- The D-bus is gated to the register selected by the CD decode.
- The A-bus is gated from the register selected by the CA decode.
- The B-bus is gated from the register selected by the CB decode.

BRANCH CONTROLS

Two microprogram fields, CH and CL, are decoded to sense the content of a particular bit of the BR and ST registers, or of 10 external CH or CL branch condition lines. IAR bits 12 and 13 are then set according to the condition sensed. Thus the microprogram can branch to the proper routines when performing operations. See CTRL 230, MIC 10-18.

ST REGISTER

The ST register is provided to record various events or conditions in the machine upon which the microprogram may branch.

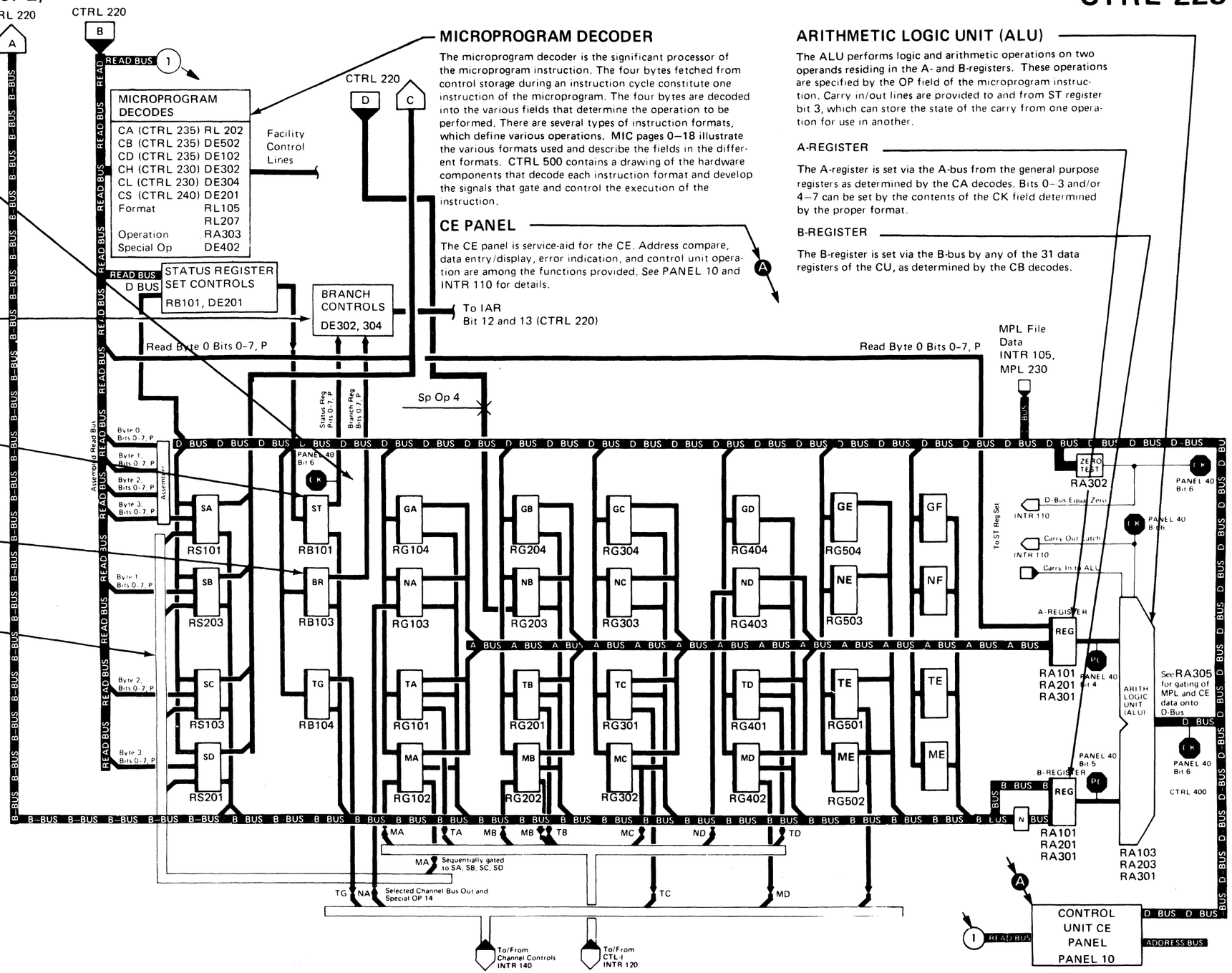
The ST register can be set by the contents of the D bus (or set individually by the microprogram or certain hardware signals). Its output is available to the B bus and to the branch controls.

BR REGISTER

The BR register is provided to enable a microprogrammed branch. This register is set by the contents of the D-bus. The odd bits are gated to the CL decoder/control, the even bits to the CH decoder/control. The output of the BR register is available to the B-bus.

STORAGE REGISTERS

SA, SB, SC, SD contain the data transferred into or out of the control storage. These registers are set by the contents of the control storage read bus, the D-bus, or by an external source. Their output is gated to the B-bus, and the control storage write bus.



MICROPROGRAM DECODER

The microprogram decoder is the significant processor of the microprogram instruction. The four bytes fetched from control storage during an instruction cycle constitute one instruction of the microprogram. The four bytes are decoded into the various fields that determine the operation to be performed. There are several types of instruction formats, which define various operations. MIC pages 0–18 illustrate the various formats used and describe the fields in the different formats. CTRL 500 contains a drawing of the hardware components that decode each instruction format and develop the signals that gate and control the execution of the instruction.

CE PANEL

The CE panel is service-aid for the CE. Address compare, data entry/display, error indication, and control unit operation are among the functions provided. See PANEL 10 and INTR 110 for details.

ARITHMETIC LOGIC UNIT (ALU)

The ALU performs logic and arithmetic operations on two operands residing in the A- and B-registers. These operations are specified by the OP field of the microprogram instruction. Carry in/out lines are provided to and from ST register bit 3, which can store the state of the carry from one operation for use in another.

A-REGISTER

The A-register is set via the A-bus from the general purpose registers as determined by the CA decodes. Bits 0–3 and/or 4–7 can be set by the contents of the CK field determined by the proper format.

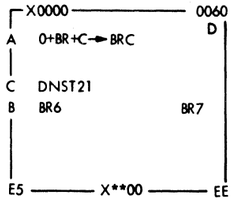
B-REGISTER

The B-register is set via the B-bus by any of the 31 data registers of the CU, as determined by the CB decodes.

INSTRUCTION DATA FLOW (Part 1 of 3)

Addressing

1 INSTRUCTION



Note: Refer to MIC 2 for detailed interpretations of microblock.

This example is Format D.

*See MIC 6 for page that shows field assignment for all the different formats. Also see CTRL 500 for format decode circuits.

MICROPROGRAM INSTRUCTION WORD

READ BUS	READ BUS	READ BUS	READ BUS	READ BUS	READ BUS	READ BUS	READ BUS
		Byte 0		Byte 1		Byte 2	Byte 3
0		7 0 3	4 7	0		7 0	7

FIELD*	CA	CS	OP	ME	CB/CD	FM	KK	ND	NB	CX	CH	CL
CONTROLS	A-Source	ST Register	ALU		B-Source and Destination					IAR Bits 8-11	Branch High Field	Branch Low Field
HEX VALUES	0	2	8		E	0				3	A	A
STATEMENT FROM INSTRUCTION BLOCK	No Register Selected	DNST21	0+BR+C→BRC		BR Register						BR 6	BR 7

CONDITIONS UPON ENTRY TO BLOCK

- BR register set to FF.
- ST register bit 3 set to 1.
- ST register bit 2 set to 0.
- This example microprogram word containing ('02', '8E', '03', 'AA') was fetched from control storage address '0060' during the later portion of the previous cycle.

EXECUTION SEQUENCE

Part 1 (This page)
1. Test branch conditions BR 6 and BR 7 and set the address of the next microprogram word to be executed into the IAR register.

Part 2
2. Execute the ALU statement specified.
3. Store carry out in ST register 3 bit.

Part 3
4. Test the D-bus for not zero and set ST register bit 2 if D-bus is not zero. Do not turn off if D = 0.
5. Fetch the next microprogram word from control storage.

2 SET BRANCH CONDITIONS

The CH and CL fields are decoded to determine the Branch Conditions.

CH DECODE

HEX CODE	CH FIELD
0	0
1	1
2	CARRY
3	ST0
4	ST2
5	ST4
6	ST6
7	BR0
8	BR2
9	BR4
A	BR6
B	CHECK-2
C	COMMO
D	ADDRO/MC6
E	SUPPO/XCHAN
F	ILACT/BOPAR

BR6 on gates the CH decode 1010

CL DECODE

HEX CODE	CL FIELD
0	0
1	1
2	D = 0
3	INDEX
4	ST3
5	ST5
6	ST7
7	BR1
8	BR3
9	BR5
A	BR7
B	SELTD/MC7
C	HLTIO/XFER
D	SERVO/MULTI
E	CUEND/BFRDY
F	RSPON/CHANB

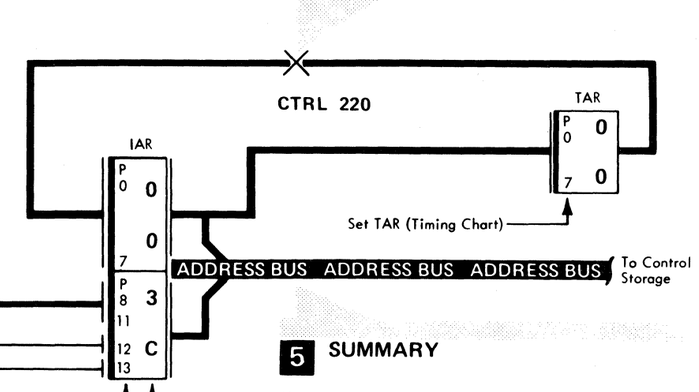
BR7 on gates the CL decode 1010

3 GATE CX TO IAR

The CX field is gated to IAR bits 8-11 for all formats except E.

4 GATE TAR TO IAR

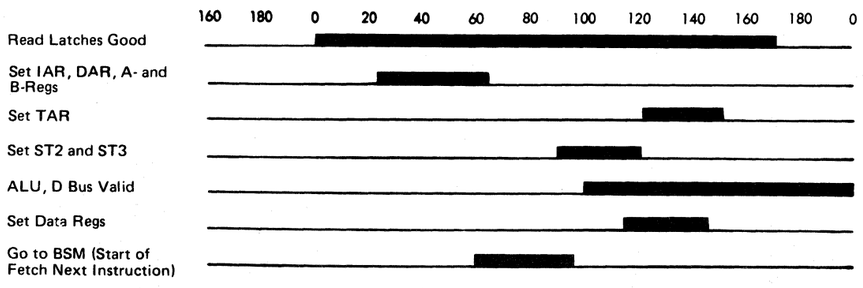
The temporary address register (TAR) is gated to the high-order positions of IAR in formats D, E, F, 1, 2, and 3. In formats A and B, partially gated. In format C, ungated.



5 SUMMARY

- When addressing the microprogram from the IAR, Control Storage is addressed on a word boundary. Address bits 14-15 are set to 0 by the address assembler.
- This instruction performs a four way branch to one of the following addresses:
  - '0030'
  - '0034'
  - '0038'
  - '003C'
- With the conditions given the next microprogram word is fetched from address '003C'.

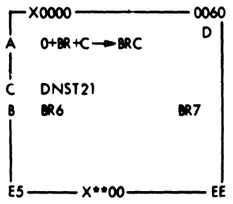
Timing Chart



INSTRUCTION DATA FLOW (Part 2of 3)

ALU Operation

1 INSTRUCTION



Note: Refer to MIC 2 for detailed interpretations of microblock.

MICROPROGRAM INSTRUCTION WORD

This example is Format D.

*See MIC 6 for page that shows field assignment for all the different formats. Also see CTRL 500 for format decode circuits.

CONDITIONS UPON ENTRY TO BLOCK

- BR register set to FF.
- ST register bit 3 set to 1.
- ST register bit 2 set to 0.
- This example microprogram word containing ('02', '8E', '03', 'AA') was fetched from control storage address '0060' during the later portion of the previous cycle.

EXECUTION SEQUENCE

Part 1
1. Test branch conditions BR 6 and BR 7 and set the address of the next microprogram word to be executed into the IAR register.

Part 2 (This page)
2. Execute the ALU statement specified.
3. Store carry out in ST register 3 bit.

Part 3
4. Test the D-bus for not zero and set ST register bit 2 if D-bus is not zero. Do not turn off if D = 0.
5. Fetch the next microprogram word from control storage.

READ BUS	READ BUS	READ BUS	READ BUS	READ BUS	READ BUS	READ BUS	READ BUS
		Byte 0		Byte 1		Byte 2	Byte 3
0		7 0 3		4 7 0		7 0	7
FIELD*	CA	CS	OP	ME	CB/CD	FM KK ND NB	CX	CH	CL
CONTROLS	A-Source	ST Register	ALU		B-Source and Destination		IAR Bits 8-11	Branch High Field	Branch Low Field
HEX VALUES	0	2	8		E	0	3	A	A
STATEMENT FROM INSTRUCTION BLOCK	No Register Selected	DNST21	0+BR+C→		BR Register			BR 6	BR 7

4 2 1 Operation Decode Bits

2 SELECT A–REG ENTRY

The CA field decode selects one of 16 gates. The selected register is gated to the A-bus.

HEX CODE		CA FIELD
0	0	0
1	1	GC
2	2	ND
3	3	NC
4	4	TD
5	5	TC
6	6	MD
7	7	MC
8	8	GB
9	9	GA
A	10	NB
B	11	NA
C	12	TB
D	13	TA
E	14	MB
F	15	MA

No Register Selected Set A-Reg to 00.

BR Register Selected

3 SELECT B–REG ENTRY

Also SELECT DESTINATION REGISTER (D Bus)
(CD field same as CB field for this format)
The CB/CD field decode selects one of 16 gates. The selected register is gated to the B bus. (32 gates and registers possible for other than D or E formats.)

HEX CODE	CB/CD FIELD	HEX CODE	CB/CD FIELD
00-0	SA	10-16	0 (None)
01-1	SB	11-17	ST
02-2	SC	12-18	GD
03-3	SD	13-19	TG
04-4	GB	14-20	ND
05-5	GA	15-21	NC
06-6	TB	16-22	NB
07-7	NA	17-23	TC
08-8	MB	18-24	
09-9	TA	19-25	
0A-10	TD	1A-26	
0B-11	NA	1B-27	
0C-12	MD	1C-28	TF
0D-13	GC	1D-29	TE
0E-14	BR	1E-30	
0F-15	MC	1F-31	

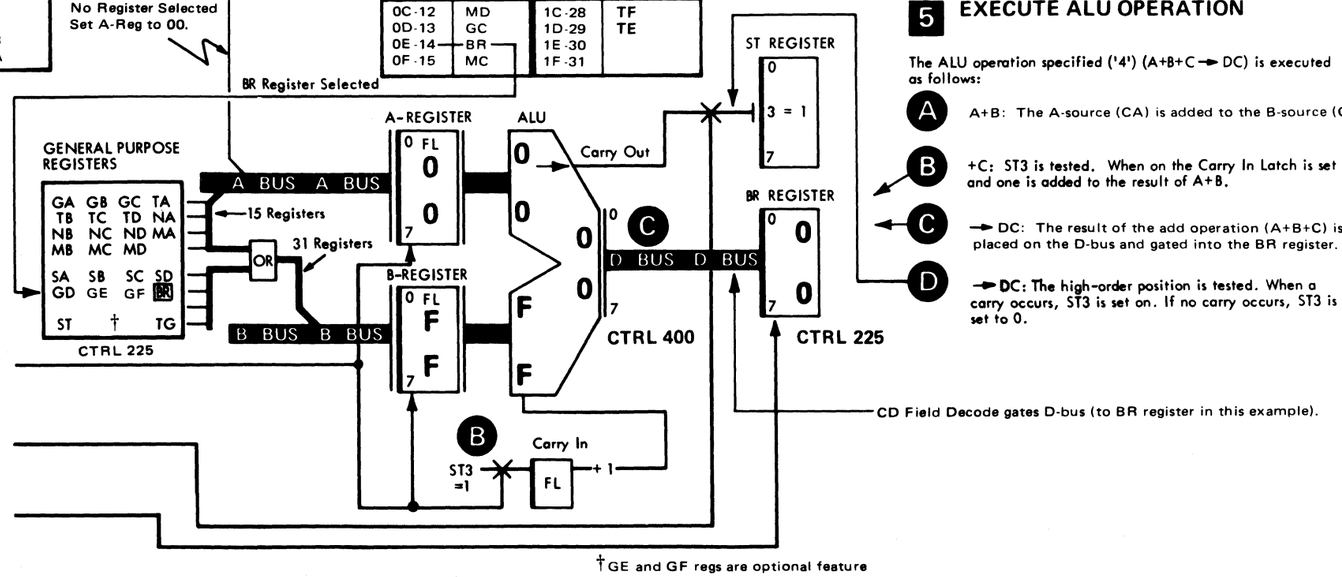
Note:
For microinstruction used in this example (Format D, ME = 0), only the first 16 registers are decoded.

4 SELECT ALU OPERATION

The OP field decode selects one of 8 ALU operations.

HEX CODE	OP * FIELD
0	AΩB → D
1	A●B → D
2	A∀B → D
3	A+B → D
4	A+B+C → DC
5	A–B+C → DC
6	A+B → DC
7	A–B+1 → D

*Refer to CTRL 410 for explanation of other ALU operations.



5 EXECUTE ALU OPERATION

The ALU operation specified ('4') (A+B+C → DC) is executed as follows:

A — A+B: The A-source (CA) is added to the B-source (CB).

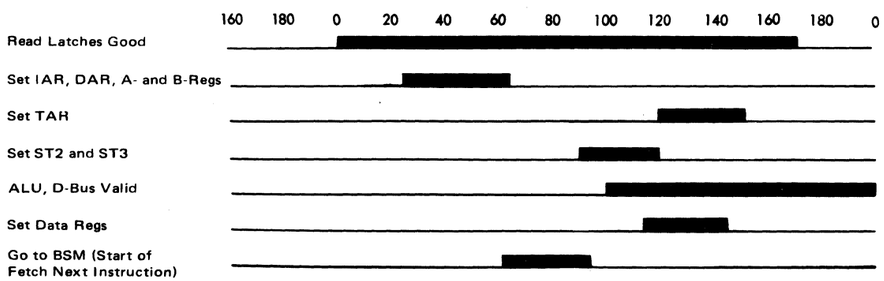
B — +C: ST3 is tested. When on the Carry In Latch is set and one is added to the result of A+B.

C — → DC: The result of the add operation (A+B+C) is placed on the D-bus and gated into the BR register.

D — → DC: The high-order position is tested. When a carry occurs, ST3 is set on. If no carry occurs, ST3 is set to 0.

†GE and GF regs are optional feature registers. See INTR 005.

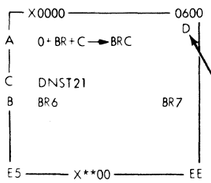
Timing Chart



INSTRUCTION DATA FLOW (Part 3 of 3)

Set Up Next Address

1 INSTRUCTION



Note: Refer to MIC 2 for detailed interpretation of microblock.

This example is format D.

*See MIC 6 for page that shows field assignment for all the different formats. Also see CTRL 500 for format decode circuits.

MICROPROGRAM INSTRUCTION WORD

	READ BUS	READ BUS	READ BUS	READ BUS	READ BUS	READ BUS	READ BUS	READ BUS
		Byte 0		Byte 1		Byte 2		Byte 3
	0	7	0 3	4 7	0	7	0	7
FIELD*	CA	CS	OP	ME	CB/CD	FM KK ND NB	CX	CH	CL
CONTROLS	A-Source	ST Register	ALU		B-Source and Destination		IAR Bits 8-11	Branch High Field	Branch Low Field
HEX VALUES	0	2	8		E	0	3	A	A
STATEMENT FROM INSTRUCTION BLOCK	No Register Selected	DNST21	0+BR+C→BRC		BR Register			BR 6	BR 7

CONDITIONS UPON ENTRY TO BLOCK

- BR register set to FF.
- ST register bit 3 set to 1.
- ST register bit 2 set to 0.
- This example microprogram word containing ('02', '8E', '03', 'AA') was fetched from control storage address '0060' during the later portion of the previous cycle.

EXECUTION SEQUENCE

Part 1
1. Test branch conditions BR 6 and BR 7 and set the address of the next microprogram word to be executed into the IAR register.

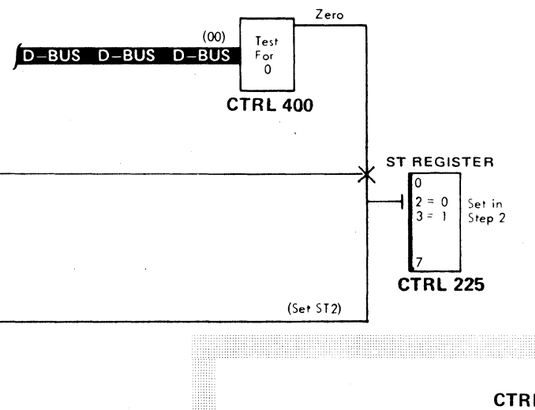
Part 2
2. Execute the ALU statement specified.
3. Store carry out in ST register 3 bit.

Part 3 (This page)
4. Test the D-bus for not zero and set ST register bit 2 if D-bus is not zero. Do not turn off if D = 0.
5. Fetch the next microprogram word from control storage.

2 TEST STATUS

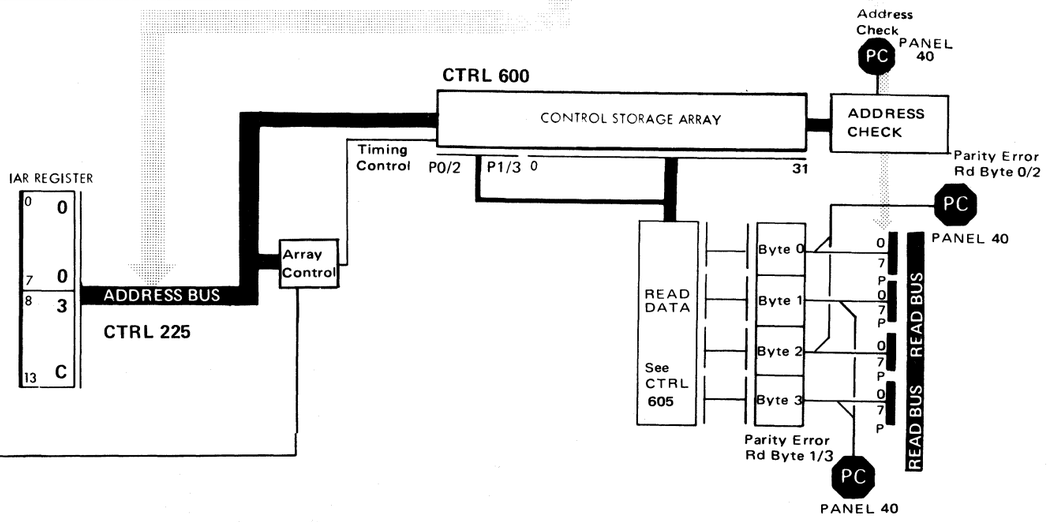
The CS field decode selects one of sixteen gates. If the D bus is not zero, ST2 is turned on. In this case the D bus is ZERO so ST2 remains unchanged.

HEX CODE	CS FIELD
0	
1	1→ST1
2	DNST21
3	1→ST3C
4	1→ST0
5	1→ST5
6	1→ST6
7	1→ST7
8	0→ST4
9	0→ST1
A	0→ST2
B	0→ST3C
C	0→ST0
D	0→ST5
E	0→ST6
F	0→ST7

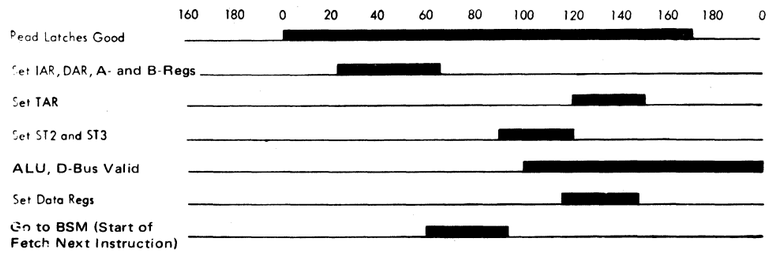


3 READ OUT NEXT INSTRUCTION FROM CONTROL STORAGE

- IAR is gated to the address bus. Control storage is addressed to read out the next instruction.
- The next microprogram word to be executed is set into the read bus latches.



Timing Chart



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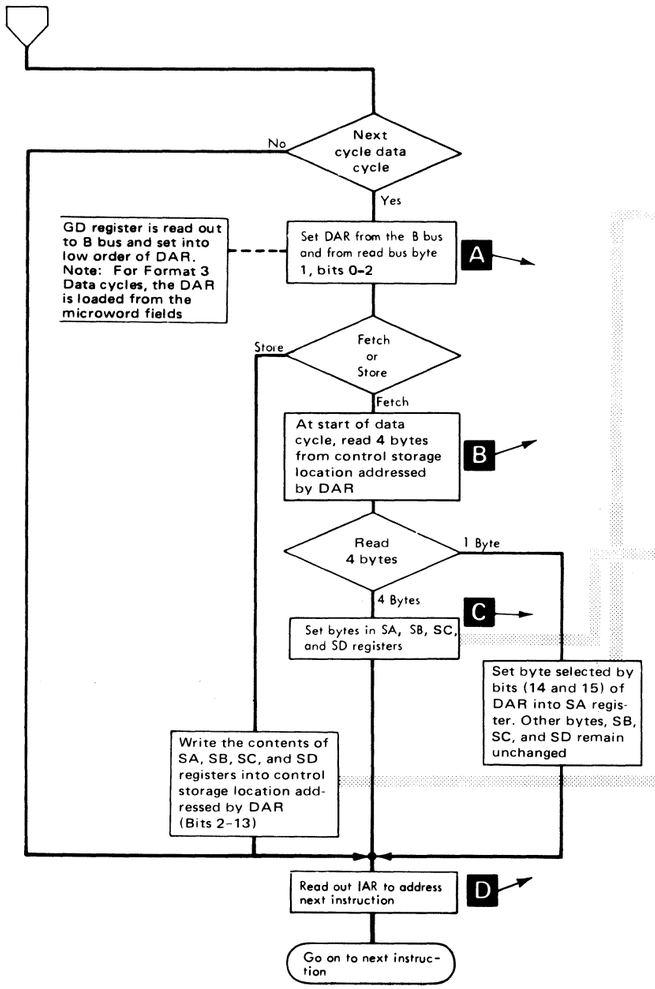
CONTROL STORAGE DATA CYCLES

Note: For example purposes, the GD register is used. In practice, any register can be used.

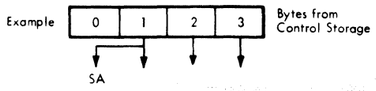
- Read data from control storage and store the data in the (SA, SB, SC, and SD) registers.
- Write data from the (SA, SB, SC, and SD) registers into the control storage.

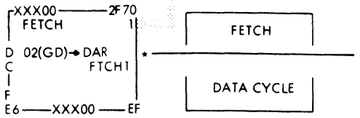
DESCRIPTION OF OPERATION



FETCH SINGLE BYTE

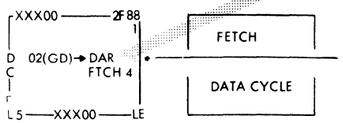
Read out four bytes from control storage, but place the byte selected by the two low order bits of DAR into the SA register.





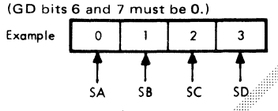
FETCH FOUR BYTES

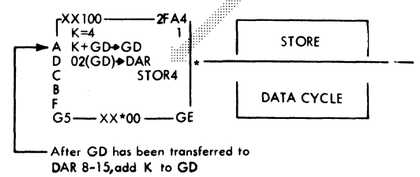
Read out four bytes from control storage and place the bytes in SA, SB, SC, and SD registers. (GD bits 6 and 7 must be 0.)



STORE FOUR BYTES

Write four bytes from SA, SB, SC, and SD into control storage.
(GD bits 6 and 7 must be 0.)





Format 1 causes a data cycle to occur. Control storage is addressed from DAR. The next instruction address is maintained in IAR.

Address control storage from DAR. Address is '02'(GD) where GD is the contents of the GD register read out on the B bus. In the example, GD = '01' so byte 1 goes into SA, and SB. Note: Formats 2 and 3 have a different address structure.

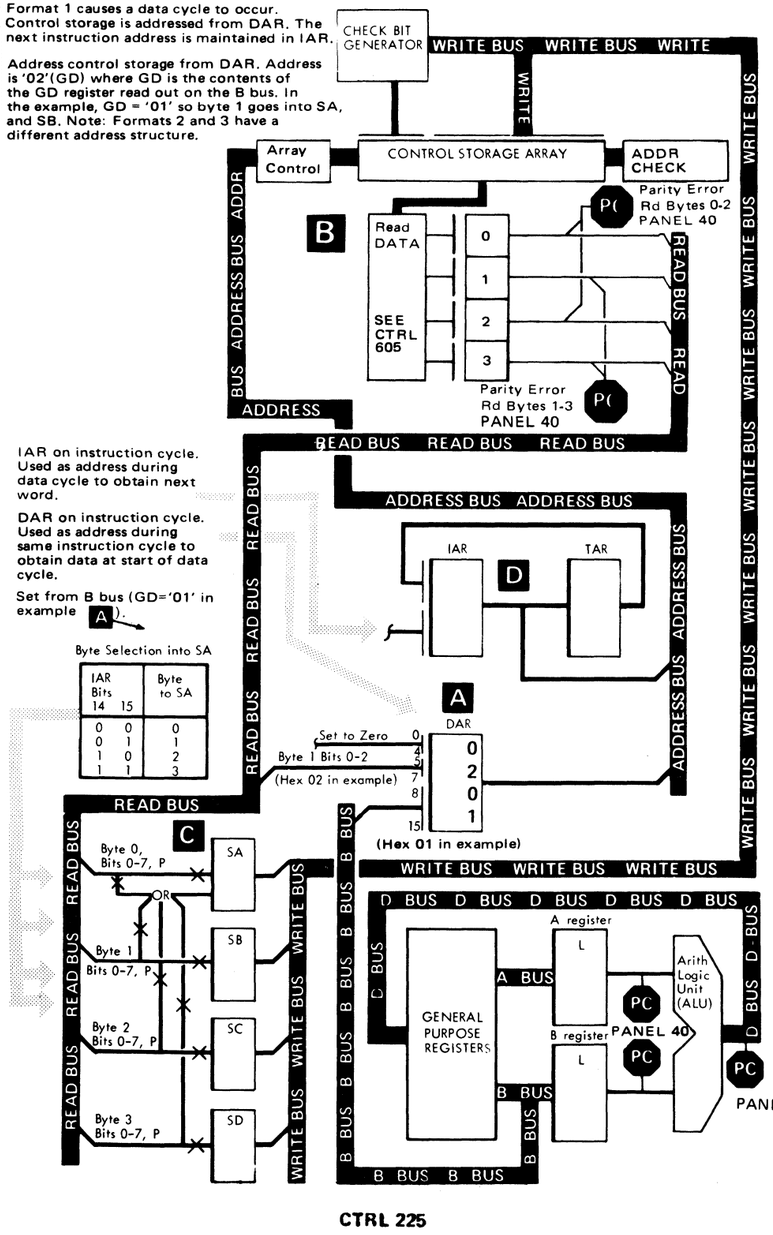
IAR on instruction cycle. Used as address during data cycle to obtain next word.

DAR on instruction cycle. Used as address during same instruction cycle to obtain data at start of data cycle.

Set from B bus (GD='01' in example A).

Byte Selection into SA

IAR Bits 14 15	Byte to SA
0 0	0
0 1	1
1 0	2
1 1	3



CTRL 605

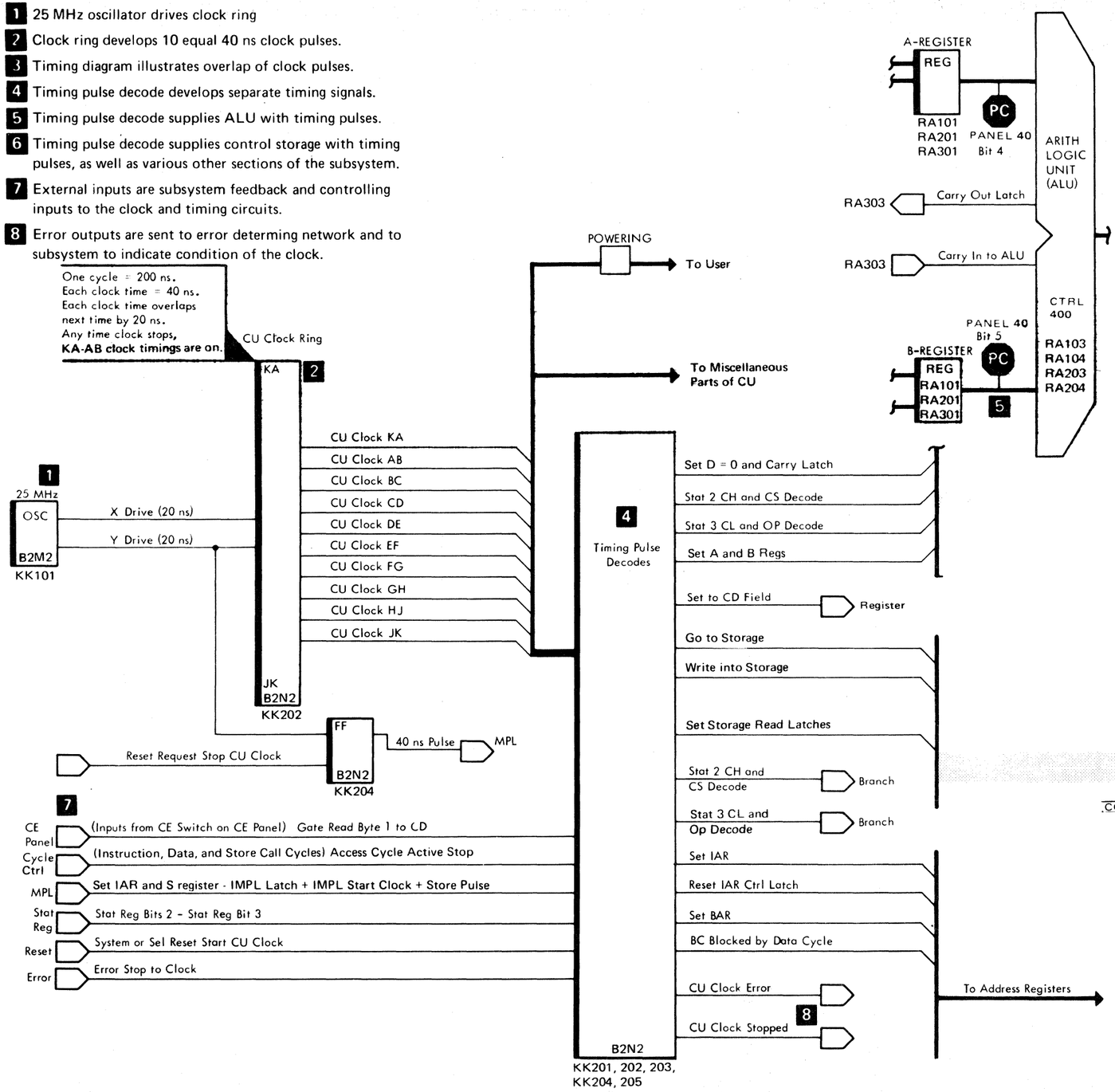
CTRL 220

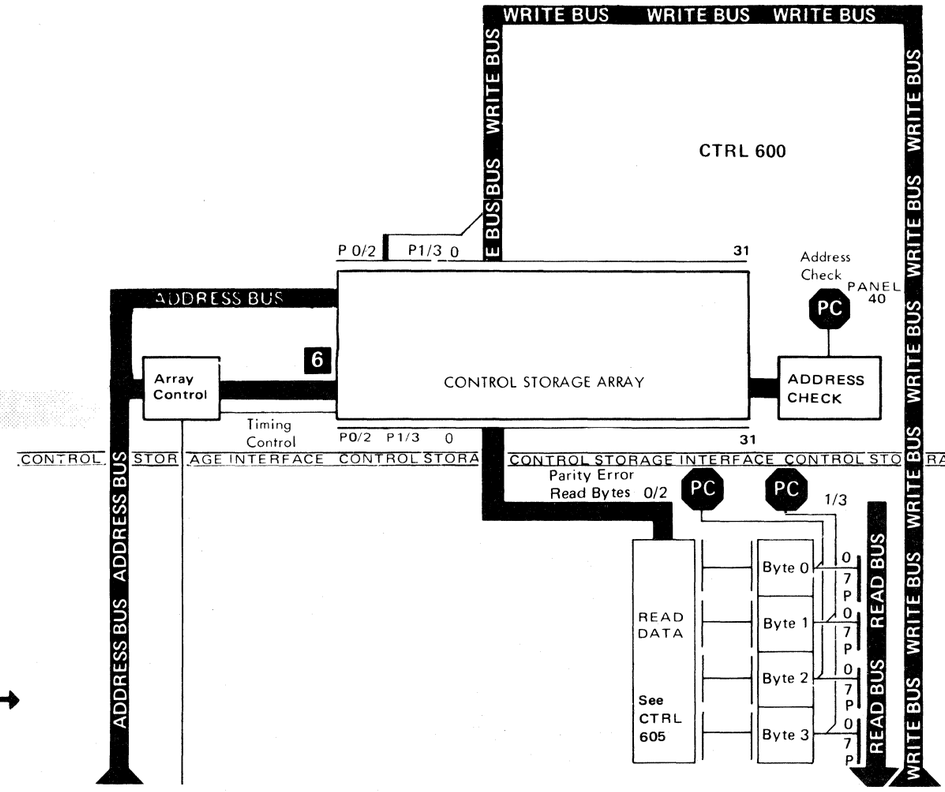
CTRL 400

CTRL 225

CONTROL UNIT CLOCK AND TIMING

1. 25 MHz oscillator drives clock ring
2. Clock ring develops 10 equal 40 ns clock pulses.
3. Timing diagram illustrates overlap of clock pulses.
4. Timing pulse decode develops separate timing signals.
5. Timing pulse decode supplies ALU with timing pulses.
6. Timing pulse decode supplies control storage with timing pulses, as well as various other sections of the subsystem.
7. External inputs are subsystem feedback and controlling inputs to the clock and timing circuits.
8. Error outputs are sent to error determing network and to subsystem to indicate condition of the clock.





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CONTROL UNIT CYCLE CONTROLS

- A machine cycle is 200 ns.
- Three major machine cycles exist:
  Access cycle, instruction/instruction call cycle, and data cycle.
- A typical sequence of machine cycles is shown on CTRL 325.
- ECD for cycle control error is on CTRL 40.

This diagram is intended for instruction only. Use machine logics for troubleshooting and scoping.

ACCESS CYCLE

This cycle occurs during each single-instruction (SI), a start from any stopped or reset state, a reset in normal mode, or a compare branch. During this cycle, control storage is addressed by the previously set instruction address register (IAR). The access cycle includes the time when the machine is stopped.

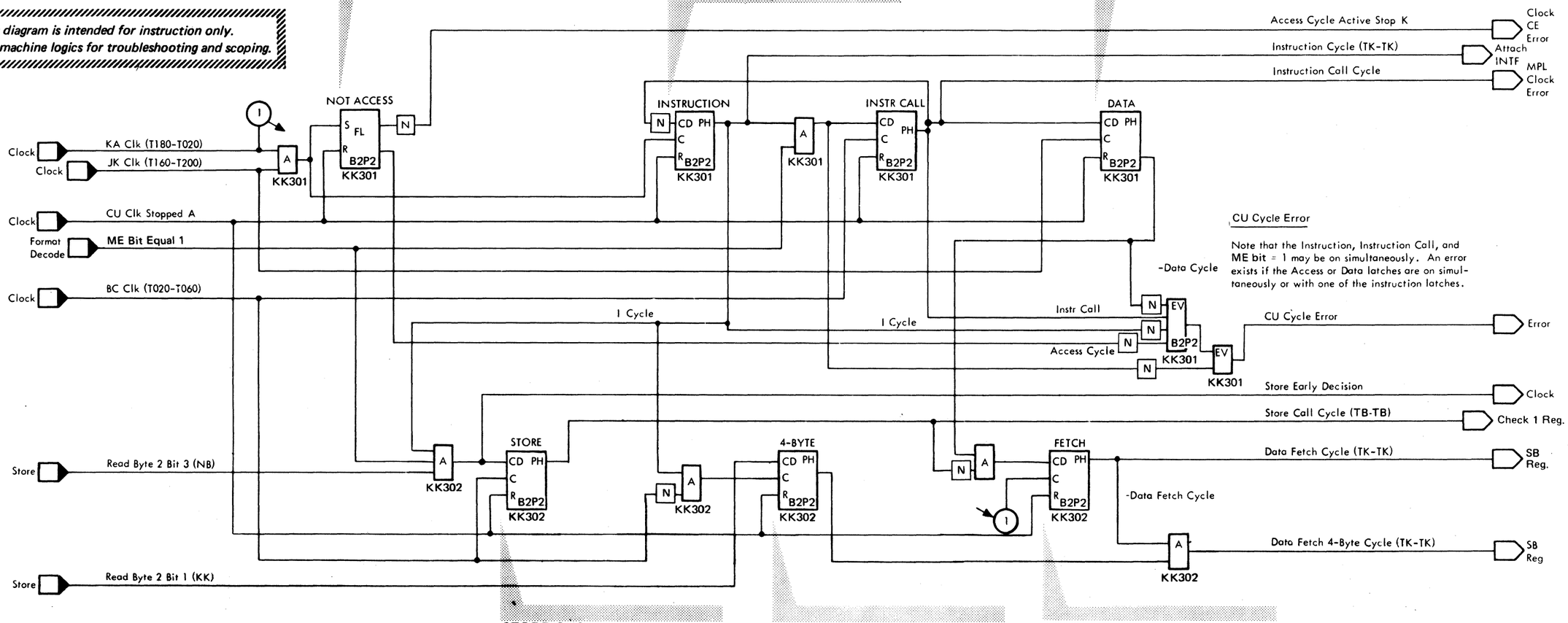
INSTRUCTION/INSTRUCTION CALL CYCLE

Data fetched from control storage during the previous cycle is interpreted as an instruction or instruction call cycle. If the next immediate cycle fetches an instruction word, this cycle is an instruction cycle. If the next immediate cycle fetches/stores data, this cycle is an instruction call cycle.

If this cycle is an instruction cycle, the IAR is set and a new instruction is fetched from control storage. If this cycle is an instruction call cycle, both the IAR and DAR are set to prepare for the following data cycle.

DATA CYCLE

This cycle immediately follows the previous instruction call cycle. Using the SA, SB, SC, and SD registers, data is either stored into or fetched from control storage at an address provided by the data address register (DAR). The fetch/store operation actually starts in the previous instruction call cycle. The IAR specifies the address of the next instruction, which is fetched in this cycle to be ready for the next cycle.



STORE CYCLE

Store cycle is set when the format decode, of the instruction fetched in the instruction call cycle, has a one in the NB (byte 2, bit 3) position.

Data store is started in the instruction call cycle and is finished at start of data cycle.

4-BYTE CYCLE

The 4 byte cycle is set when the format decode of the instruction fetched in the instruction call cycle has a one in the KK (byte 2, bit 1) position.

If 4-byte cycle is on during a fetch cycle, four bytes are set into SA, SB, SC, and SD registers. If 4-byte cycle is off only 1 out of 4 bytes is set into SA register.

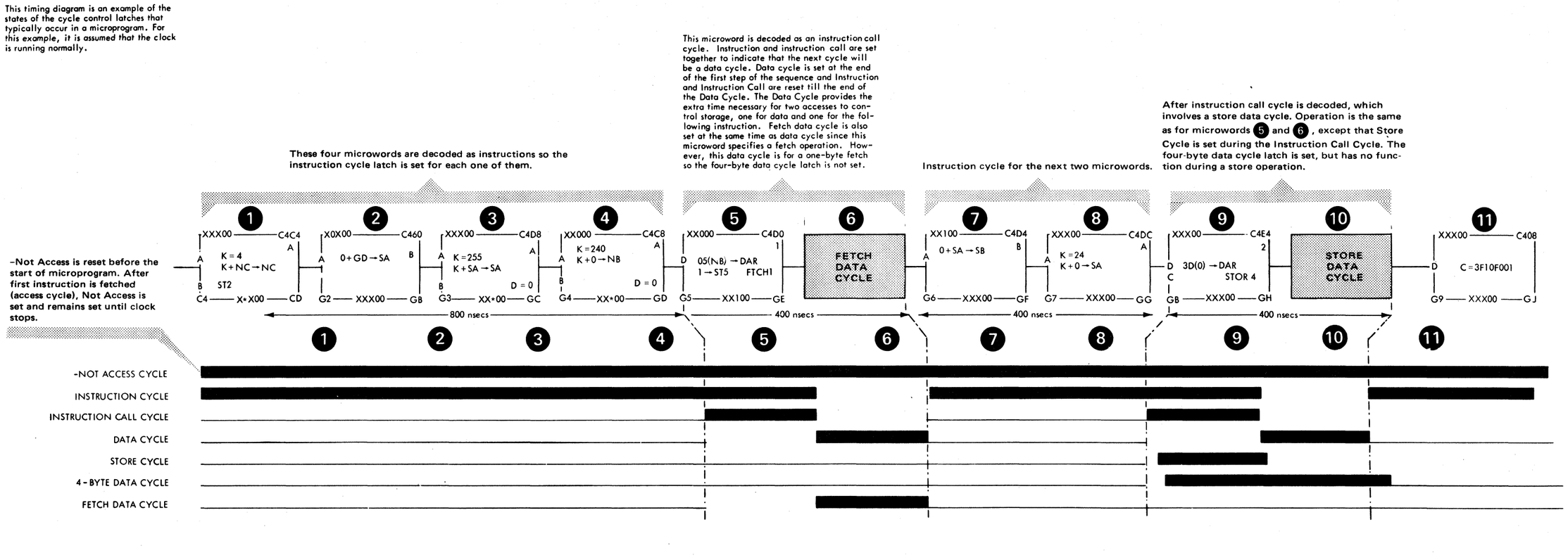
FETCH CYCLE

Data fetch cycle is set when the format decode of the instruction fetched in the instruction call cycle has a zero in the NB (byte 2, bit 3) position.

Data fetch is started in the instruction call cycle and is completed in the data cycle.

CONTROL UNIT CYCLE CONTROLS TIMING

This timing diagram is an example of the states of the cycle control latches that typically occur in a microprogram. For this example, it is assumed that the clock is running normally.



ARITHMETIC LOGIC UNIT (ALU) AND RELATED COMPONENTS

- ALU performs eight operations which are encoded in the Op field.
- ALU results always gated to D bus.
- ALU generates correct (odd) parity on any operation performed.
- ALU inputs come from A and B register and carry.
- ALU check ECD on CTRL 60.

ARITHMETIC LOGIC UNIT (ALU)

The ALU performes logic and arithmetic operations on two operands residing in the A and B registers. These operations are specified by the Op field of the microprogram instruction. Carry in/out lines are provided to and from ST register bit 3. The B register can be set to contain the 1's complement of its source. Look ahead carry and parity prediction make it possible to complete the ALU operation during the same machine cycle in which the microprogram instruction word was fetched. Error detection is provided by parity checking the A and B registers and also checking the ALU carry and parity outputs.

A REGISTER

The A register is set through the A bus from the general purpose registers as determined by the CA decodes. Bits 0-3 and/or 4-7 can also be set with contents of CK field.

OP FIELD

The Op field specifies the arithmetic function that is to be performed by ALU. The data source for ALU operations is the A register and the B register.

Hex Code	OP Field
0	A Ω B → D
1	A • B → D
2	A ∇ B → D
3	A + B → D
4	A + B + C → DC
5	A - B + C → DC
6	A + B → DC
7	A - B + 1 → D

This diagram is intended for instruction only. Use machine logics for troubleshooting and scoping.

B REGISTER

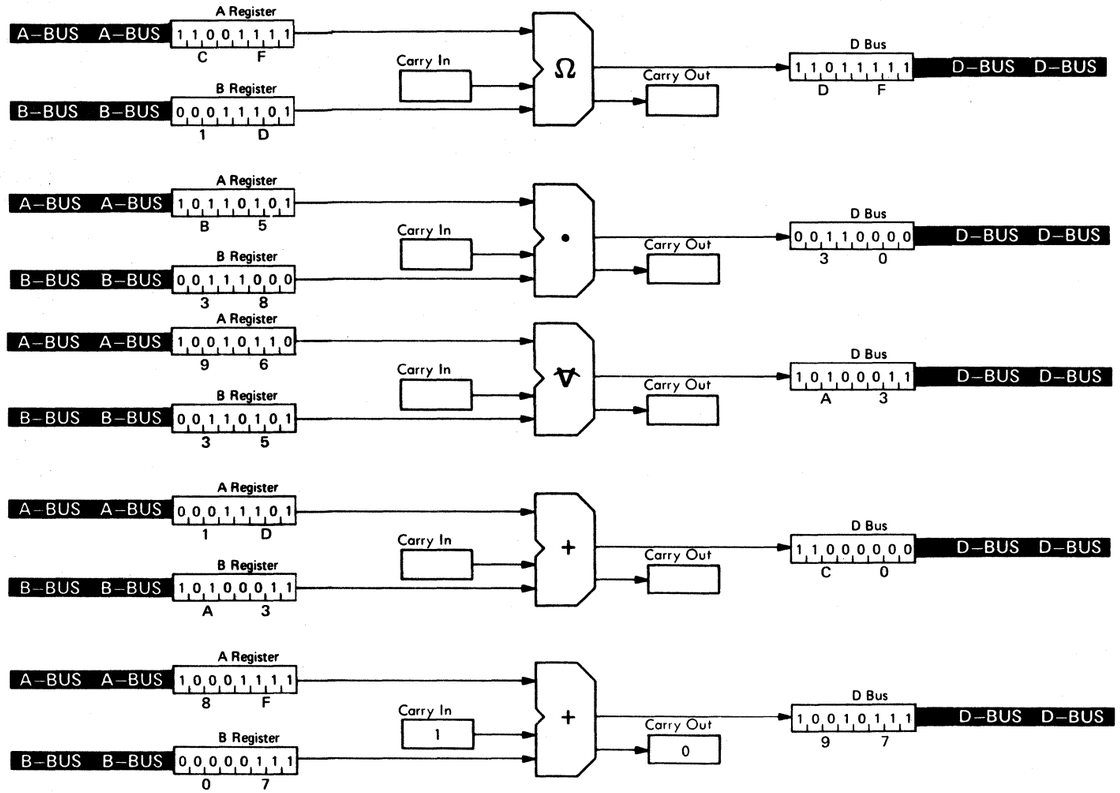
The B register is set through the B bus by any of 31 registers as determined by the CB decodes. ALU Op decodes 5, 7 force complementary inputs into the B register. On CB decode 16, the B register is set to all 0's.

ALU Check:

a. A noncomparision between predicted parity and actual parity of the ALU occured.
b. An Op decode parity error was gated to ALU.
c. A noncomparision between the two D bus equals zero checks occured

ALU OPERATIONS–EXAMPLES

OP Decode	Name	Symbolic
0	OR	A Ω B → D
1	AND	A • B → D
2	Exculusive OR	A ∀ B → D
3	Add	A + B → D
4	Add, Carry	A + B + C → D C
5	Add Complement, Carry	A - B + C → D C
6	Add and Carry	A + B → D C
7	Subtract	A - B + 1 → D



A Ω B → D (OR)

The contents of the A-register are ORed with the contents of the B-register.

A • B → D (AND)

The contents of the A-register are ANDed with the contents of the B-register.

A ∀ B → B (Exclusive OR)

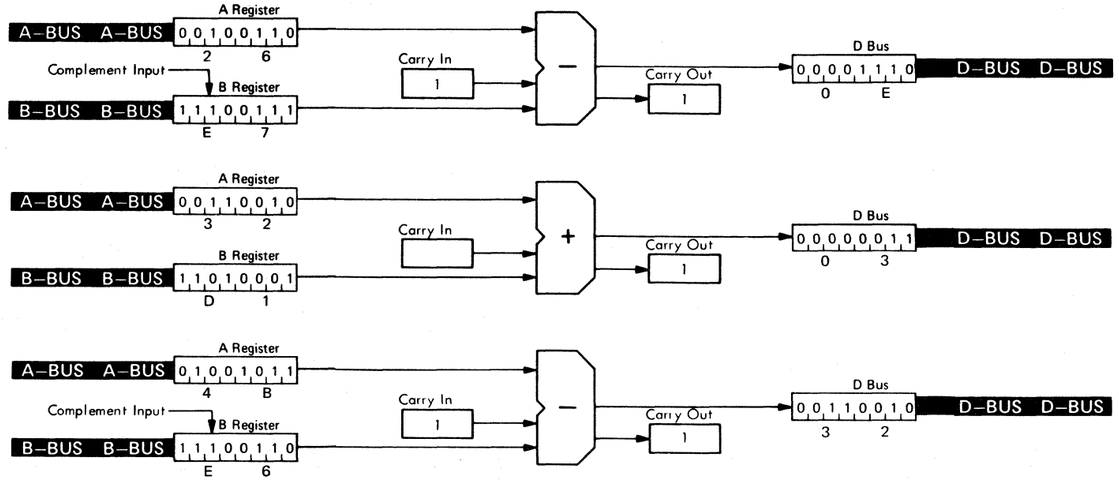
The contents of the A-register are exclusive ORed with the contents of the B-register.

A + B → D (Add)

The contents of the A-register are added to the contents of the B-register.

A + B + C → DC (Add, Carry)

The ALU adds the contents of the A- and B-registers with the present condition of status register Bit 3 (carry in). The carry out (if any) from the high order ALU position is stored back in status register bit 3.



A - B + C → DC (Add 1's Complement, Carry)

The ALU adds the contents of the A- and B-registers with the present condition of status register Bit 3. The B-register is a 1's complement of the B-bus. If no register is specified, the B-register is set to all 1s (1's complement of 0).
The carry out (if any) is stored back in status register bit 3.

A + B → DC (Add and Carry)

The ALU adds the contents of the A- and B-registers. A carry out (if any) is stored in status register bit 3.

A - B + 1 → D (Add 2's Complement - Subtract)

The ALU adds the contents of the A- and B-registers with a forced 1 in the low order ALU position. Since the B-register is set with a 1's complement of the B-bus, ALU effectively performs a subtraction. If no register is specified, the B-register is set to all 1s (1's complement of 0).

INSTRUCTION FORMAT DECODE

Formats are organized into three groups: A-C, D-F, 1-3. Formats 1 and 2 are further subdivided by a letter suffix, which differentiates between a four-byte fetch (suffix a), Four-byte store (suffix b), or one-byte fetch (suffix c) within the format. The following table lists the differences:

Format Groups Differentiation

Formats	Code	Status Setting	Fetch/Store
A-C	FM = 1	No	No
D-F	FM = 0 ME = 0	Yes	No
1-3	FM = 0 ME = 1	Yes	Yes

Formats 1-3 imply that the instruction cycle during which the microword is decoded is an instruction/call cycle. The next machine cycle following a format 1-3 readout is a data cycle during which data is fetched from or stored into control storage. Formats 1b and 2b store data (NB = 1) and the other formats in this group fetch data (NB = 0). A four-byte fetch is made between control storage and the SA, SB, SC, and SD registers when KK = 1. All store operations are four bytes wide. Formats 1c and 3 with KK = 0 specify one-byte operations. One byte out of four fetched is inserted into the SA register. The purpose of the formats is listed in the following table. For a detailed analysis see the MIC pages.

This diagram is intended for instruction only. Use machine logics for troubleshooting and scoping.

Format	Use
A and D	General Purpose
B	Independent Register Selection
C	Long Addressing
E	Indirect Addressing
F	Special Operations
1a	Four-byte Fetch, Register Update
1b	Four-byte Store, Register Update
1c	One-byte Fetch, Register Update
2a	Four-byte Fetch
2b	Four-byte Store
3	One-byte Fetch, address provided by microword.

This chart lists the lines that are active for each format decode.

ACTIVE LINES

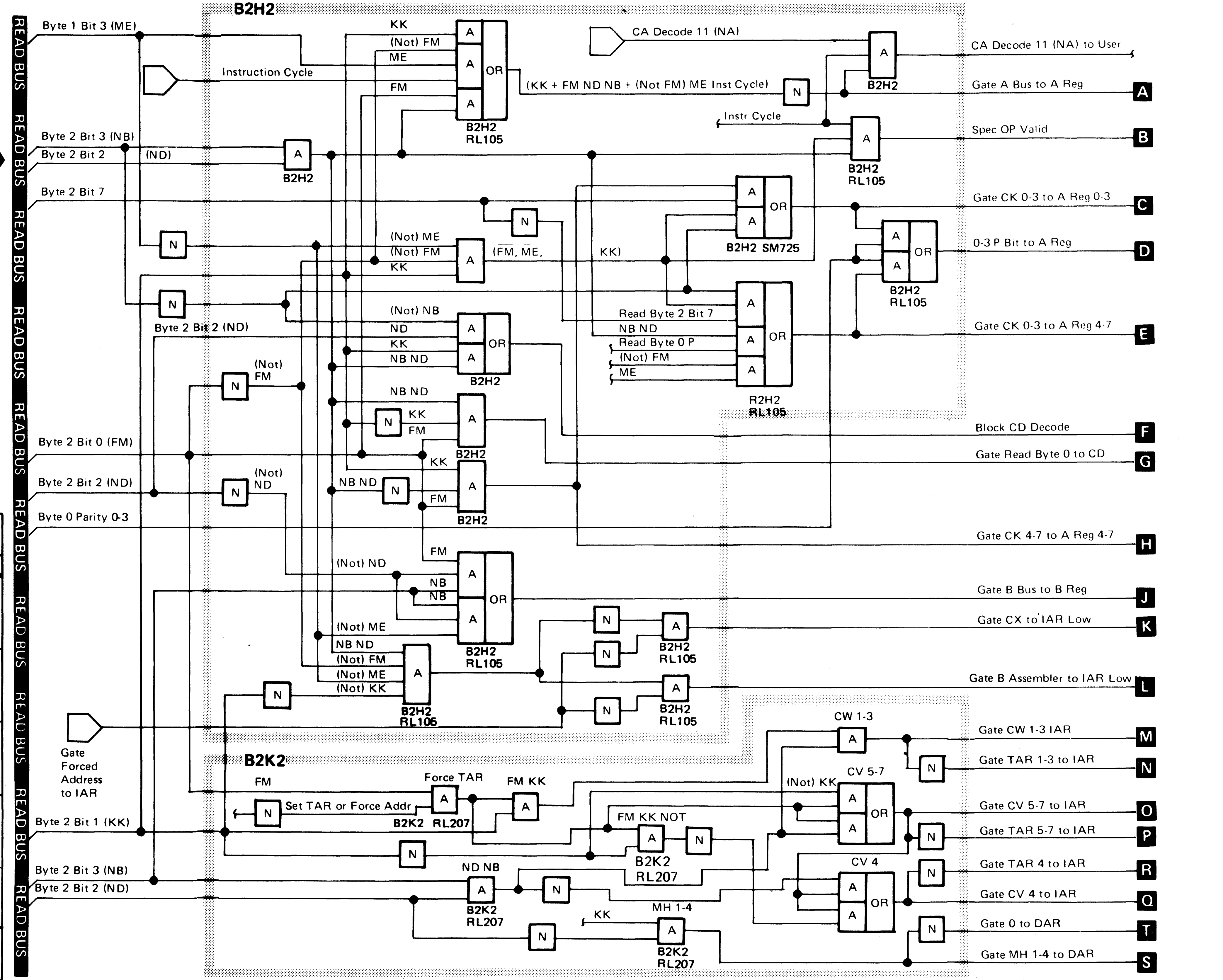
(Letters in table refer to lettered lines in the logic portion of this diagram.)

ME	FM	KK	ND	NB	FORMAT	A	B	C	D	E	F	G	H	J	K	L	M	N	O	P	Q	R	S	T
0	0	0	0	0	D	A								J	K			N		P		R		T
0	0	0	0	1	D	A									K			N		P		R		T
0	0	0	1	0	D	A					F			J	K			N		P		R		T
0	0	0	1	1	E	A								J		L		N		P		R		T
0	0	1	0	0	D			C*	D	E**				J	K			N		P		R		T
0	0	1	0	1	D			C*	D	E**					K			N		P		R		T
0	0	1	1	0	D			C*	D	E**	F			J	K			N		P		R	S	
0	0	1	1	1	F		B		D	E	F			J	K			N		P		R	S	
X	1	0	0	0	A	A								J	K			N	O		Q			T
X	1	0	0	1	A	A									K			N	O		Q			T
X	1	0	1	0	A	A					F			J	K			N	O		Q			T
X	1	0	1	1	B							G		J	K			N	O					T
X	1	1	0	0	A			C	D				H	J	K			N		P		R		T
X	1	1	0	1	A			C					H		K			N		P		R		T
X	1	1	1	0	A			C			F		H	J	K			N		P		R	S	
X	1	1	1	1	C				D	E	F			J	K		M		O		Q		S	
1	0	0	0	0	1c				D	E				J	K			N		P		R		T
1	0	0	0	1	3				D	E				J	K			N		P		R		T
1	0	0	1	0	3				D	E	F			J	K			N		P		R		T
1	0	0	1	1	3				D	E				J	K			N		P		R		T
1	0	1	0	0	1a				D	E				J	K			N		P		R		T
1	0	1	0	1	1b				D	E				J	K			N		P		R		T
1	0	1	1	0	2a				D	E	F			J	K			N		P		R	S	
1	0	1	1	1	2b				D	E	F			J	K			N		P		R	S	

*If byte 2, bit 7 = 1

**If byte 2, bit 7 = 0

Depends on state of Byte 0, Bits 0-3 Parity



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CONTROL STORAGE (Part 1 of 2)

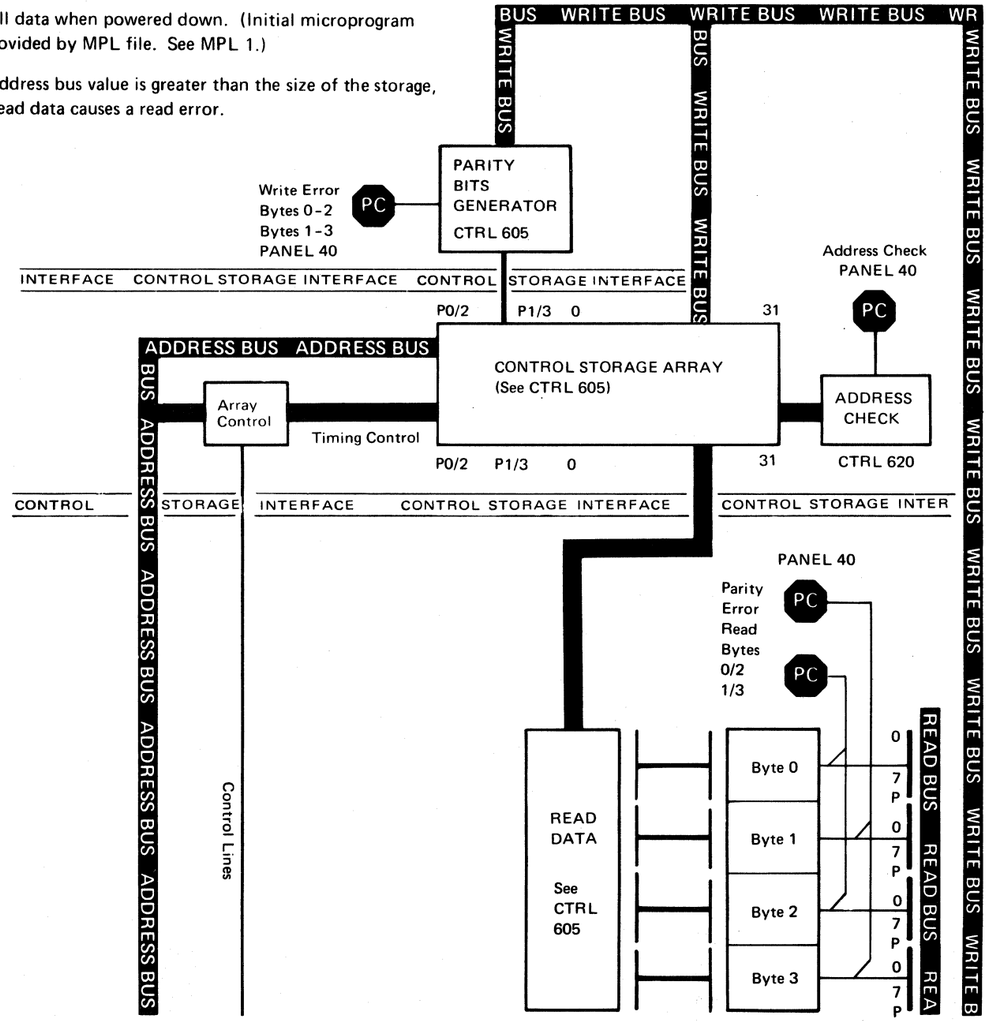
PURPOSE

- Stores microprograms used to control and test the facility.
- Stores error/usage log information and miscellaneous control data.

DESCRIPTION

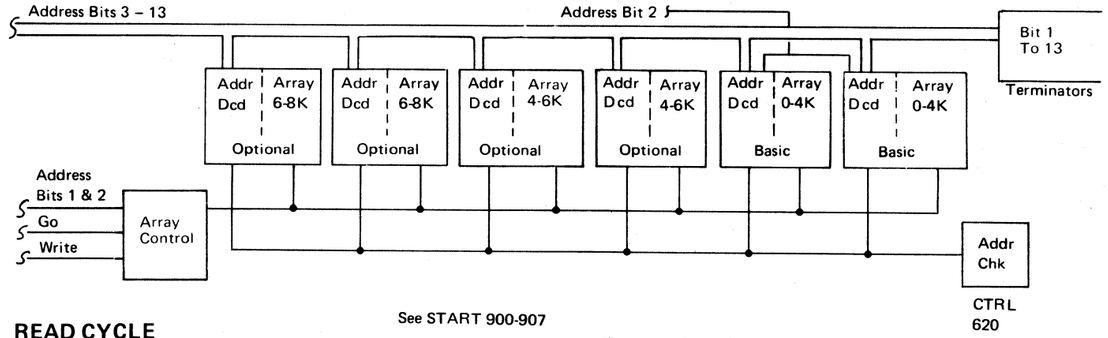
- Designed for use in many machines and sizes (4K, 6K, 8K)
- Each word contains 32 data bits and 2 parity bits.
- Loses all data when powered down. (Initial microprogram load provided by MPL file. See MPL 1.)
- If the address bus value is greater than the size of the storage, blank read data causes a read error.

Note: If timing card is replaced, the width of the TP Timing pulse must be checked. The width of the pulse is measured at the ground level and should be 55 ns, +8 -0 ns. Change jumpers as required. Recycle at address '0000' during measurement. See PANEL 16 for Recycle procedure.



ADDRESSING

Address bits 2 through 13 are fed to each array card directly from the address bus. Each array card decodes 2,048 or 4096 addresses to select (read or write) 17 data bits. Each array card also supplies decoded address check levels to the address checking circuitry. Address bits 1 and 2, Go, and Write Lines combine within the array control card to generate timing, Set, Reset, and Write Gate pulses. Timing pulses (see note) are sent only to the selected pair of array cards (bit 1=0 for 0 to 4K, bit 1=1 and bit 2=0 for 4 to 6K, bit 1=1 and bit 2=1 for 6 to 8K), whereas Set, Reset and Write Gate pulses go to all array cards.



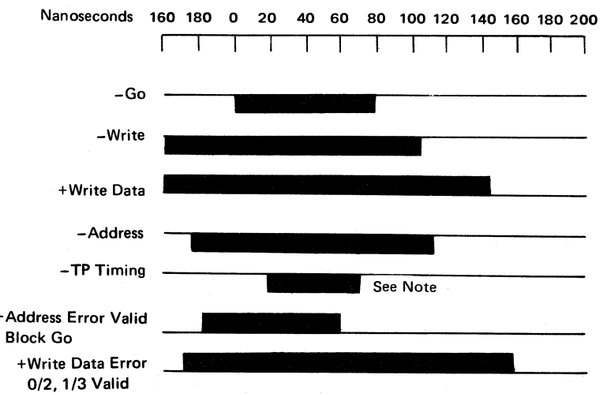
See START 900-907

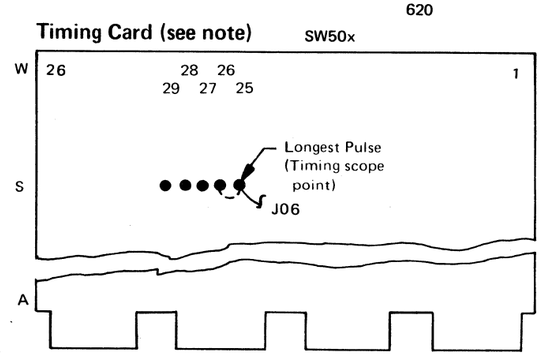
READ CYCLE

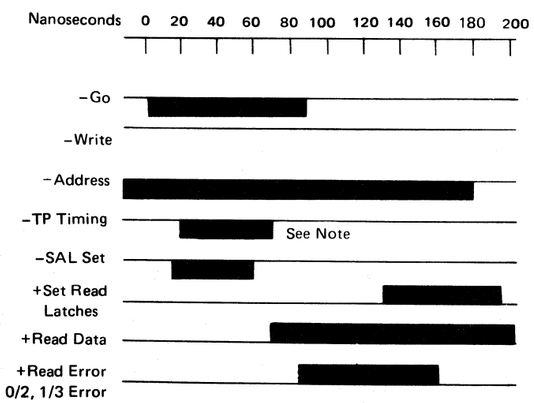
The bits are read from the array cards and checked. Bit failure (either read or write error) generates an error. Blank data (from cards not installed being addressed) causes a read error.

WRITE CYCLE

The 32 data bits supplied by the write bus are checked by byte (in groups of 16) by the write bus parity circuits. Parity bits are generated and stored with 32 data bits. The bits are stored in the monolithic array, 17 bits to a card.







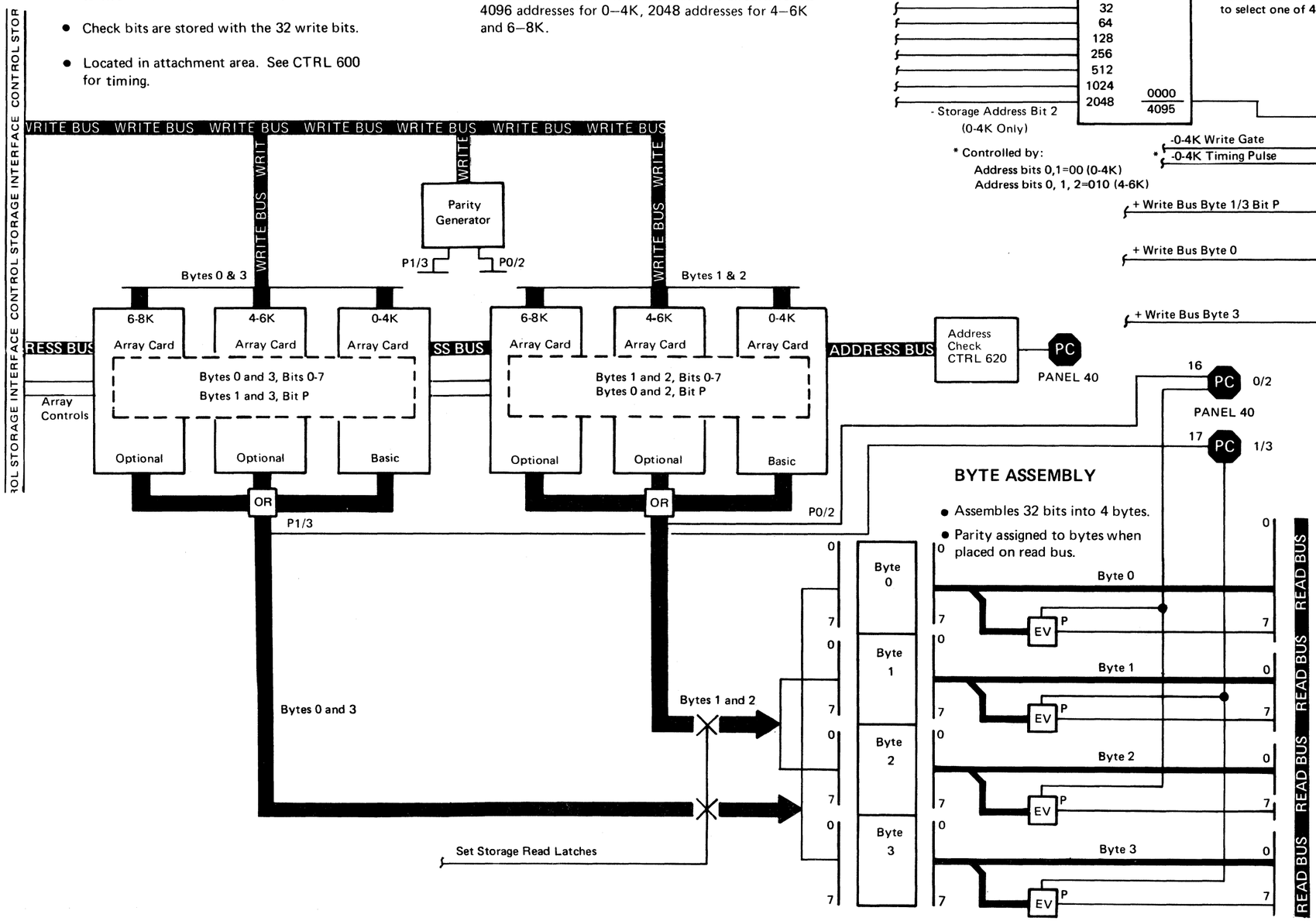
CONTROL STORAGE (Part 2 of 2)

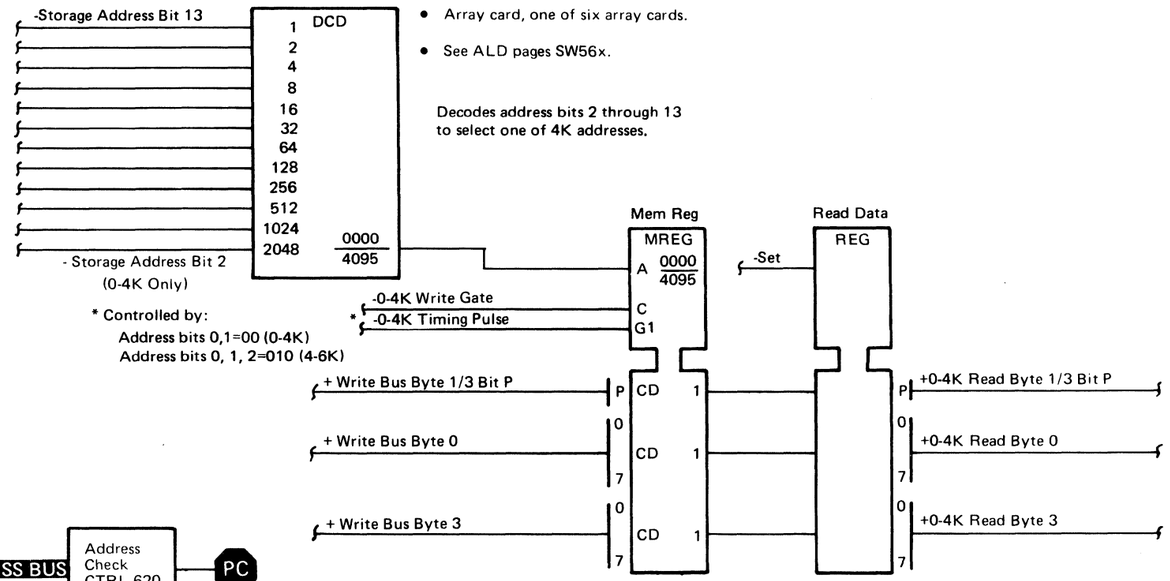
WRITE BUS PARITY

- Parity generator checks four parity bits from the write data and corrects them to two check bits.
- Check bits are stored with the 32 write bits.
- Located in attachment area. See CTRL 600 for timing.

ARRAY CARDS

- Each card stores 17 bits each of 4,096 addresses.
- Each card contains the address decode circuits for its' 4096 addresses for 0–4K, 2048 addresses for 4–6K and 6–8K.





STORAGE READ BYTES 1 AND 3, 0 AND 2

Check 1 Register Bit 9, 10 -- Early (Bit 0 = 1)

The storage read bytes are checked for odd parity through a series of even blocks (exclusive OR trees). The Check 1 lamp turns on when an error (even bits read from control storage) is detected.

The Check 1 register bit 10 is turned on by an error detected in bytes 1 or 3. Each byte is gated to an even block to generate a parity bit. These bits are sent to the parity error 1 and 3 even block with the output of the combined bytes 1 and 3 parity bit read from storage.

Any combination of two minus inputs and a plus or three plus inputs causes a parity error, and the Check 1 register 10 bit will be set by the error detect register bit 10.

The check 1 register 9 bit is set by a parity error in read bytes 0 or 2 in the same way as the 10 bit.

STORAGE WRITE BYTES 0 AND 2 ERROR

Check 1 Register Bit 10 — Late (Bit 0 = 0)

Storage write bytes 0 and 2 are checked for odd parity. They turn on bit 10 in the check 1 register if an error is detected.

All bits of each byte, including the parity bit, are gated through an even block to generate the error line. If an error is detected (even number of bits in either byte), the check 1 register bit 10 is turned on and the Check 1 lamp lit.

The two parity bits are also used to generate a single parity bit to be written in storage with the two bytes (SW521).

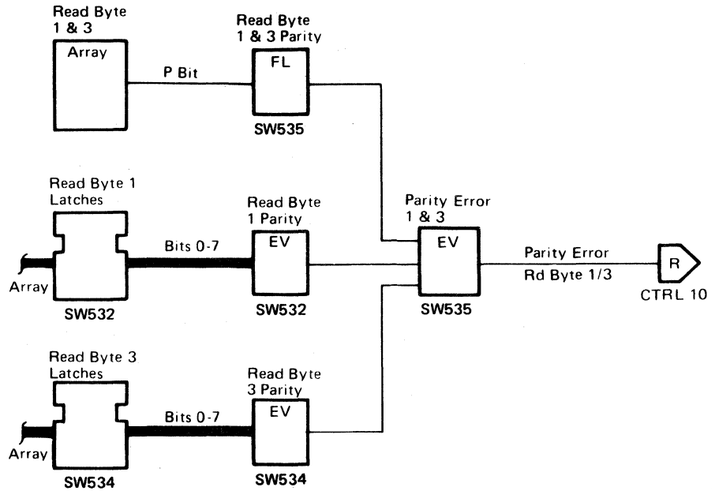
STORAGE WRITE BYTES 1 AND 3 ERROR

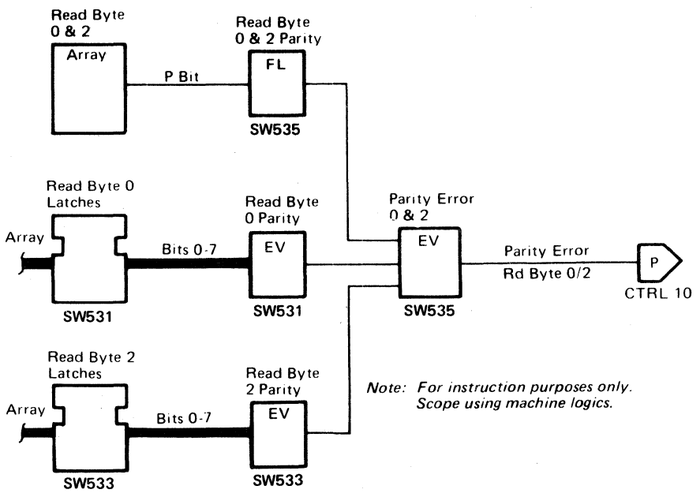
Check 1 Register Bit 11 — Late (Bit 0 = 0)

Storage write bytes 1 and 3 are checked for odd parity. They turn on bit 11 in the Check 1 register if an error is detected.

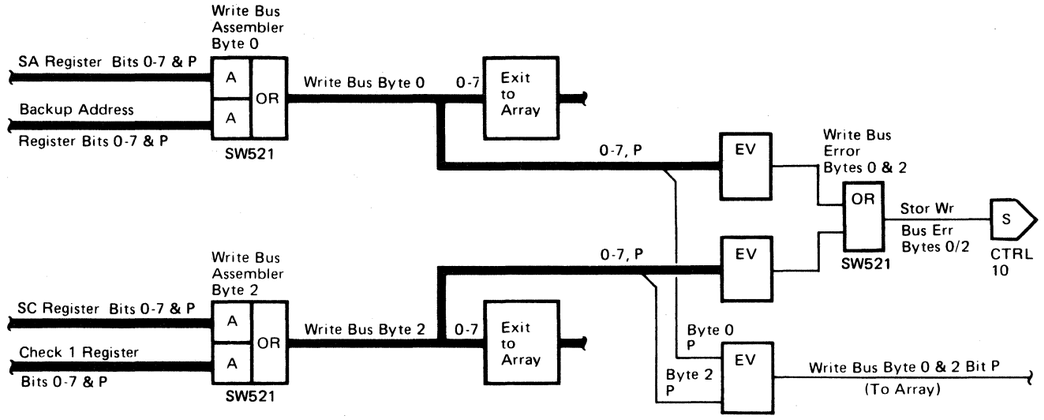
All bits of each byte, including the parity bit, are gated through an even block to generate the error line. If an error is detected (even number of bits in either byte), the Check 1 register bit 11 is turned on and the Check 1 lamp is lit.

The two parity bits are also used to generate a single parity bit to be written in storage with the two bytes (SW522).



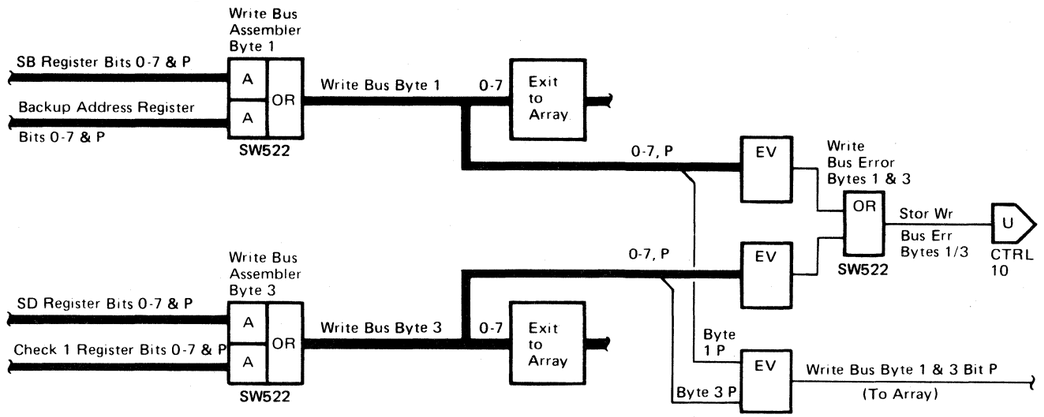


Note: For instruction purposes only. Scope using machine logics.



References

INTR 110 General
PANEL 40 Check 1
CTRL 600 Timing



Note: For instruction purposes only. Scope using machine logics.

CONTROL STORAGE ADDRESS CHECK LOGIC

ADDRESS ERROR

An address error indicates (1) incorrect addressing of array cards, or (2) malfunctions of internal addressing on the array cards. The address error circuits are checked (1) after cycling control storage on Read operations, and (2) before cycling control storage on Write operations. Three checks are made:

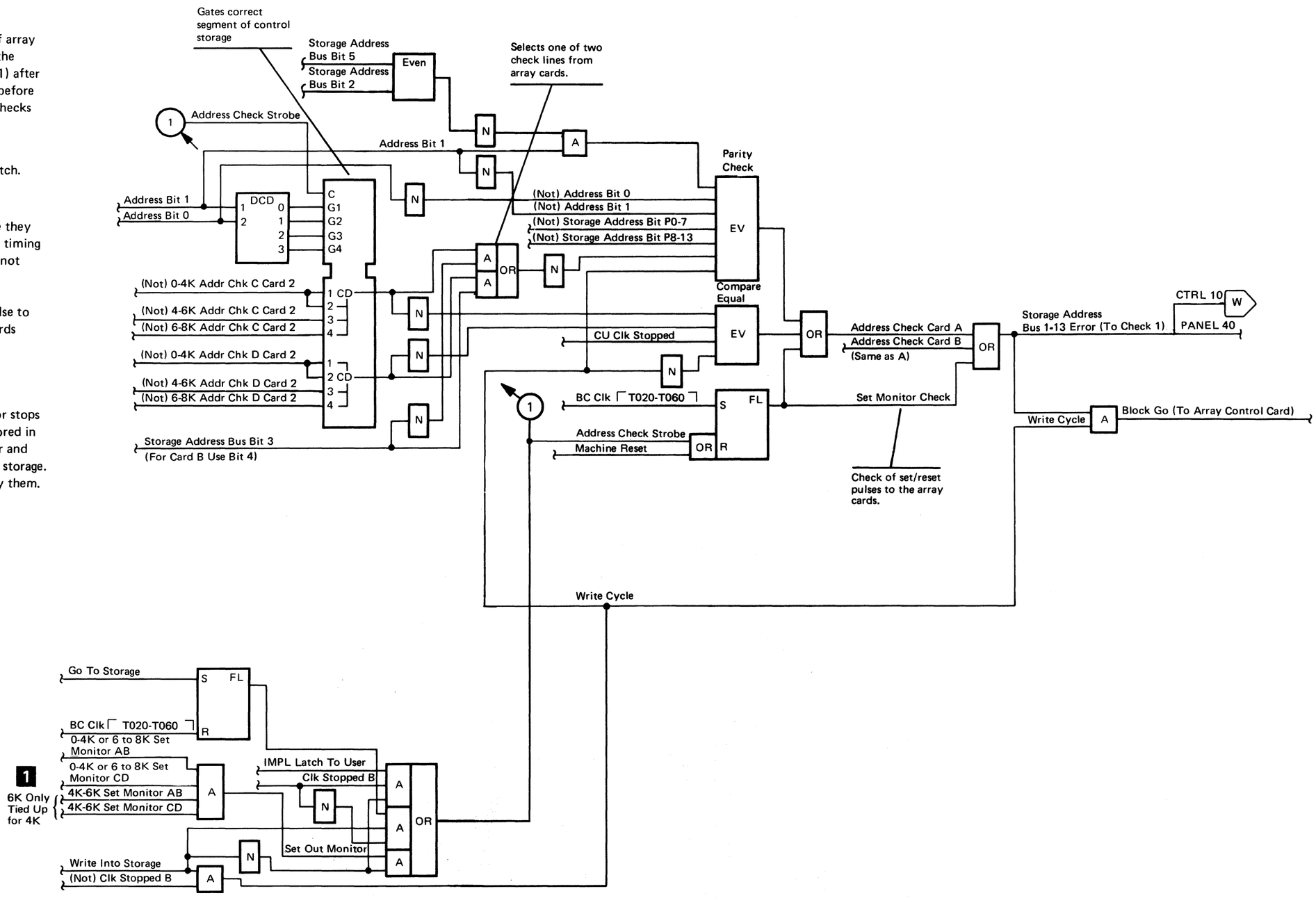
1. That all cards are set or reset.
2. That upper/lower addressing of all array cards match.
3. That address parity is odd.

Address bits 3 and 4 control the equal check because they control the timing pulse (PT) on the array card. The timing pulse is used when checking on Read operations but not Write operations.

The addressing on the array cards, and the timing pulse to the array cards, are partially checked on the array cards (two outputs per card).

ERROR DESTINATION

The address error is a Check 1 error. An address error stops the CU clock at the end of the cycle. The error is stored in the Check 1 register. After a selective reset, the error and the intended address from BAR are stored in control storage. See PANEL 40 for Check 1 errors and how to display them. See CTRL 650 for control storage contents.

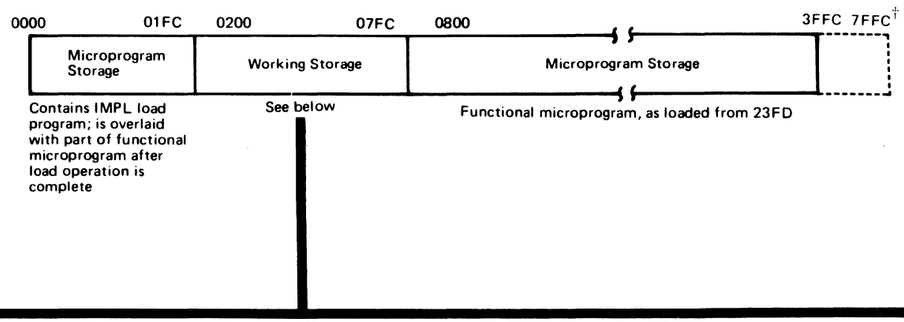


3830-2	BD2100 Seq 1 of 1	4290932 Part No. (2)	447460 19 Dec 75	447461 12 Mar 76	447465 15 Dec 78			

CONTROL STORAGE CONTENTS (Part 1 of 2)

The Control Storage Map for functional microcode P/N 4168811 can be found on CAS microfiche P/N 4168831.

- Read/write storage of data.
- Up to 8,192 four byte words (32,768 bytes).
- Contains the functional microprogram and working storage used by the microprogram.
- For microprogram use, each word (four bytes) equals one microprogram instruction.
- For data storage, can be read or written four bytes at a time or read one byte at a time.
- Input and output to control storage is to/from SA, SB, SC, and SD registers.



TERMINOLOGY

Add	Address	DCC	Disconnected Command Chain	Perm	Permanent
Bin	Binary			PCH	Pack Change
BSDA	Bit Significant Device Address	ECC	Error Correction Code	R	Record
				Res	Reserved
C, Cyl	Cylinder	EDI	Expected Device Interrupt	SCB	Sense Control Block
CEB	Command Execution Byte	EL	Error Log	SD	Skip Displacement
CM	Control Module	FM	File Mask	SIP	Seek In Progress
Cont Conn Const	Contingent Connection Constant	H, Hd	Head	SK	Seek
		ISCB	Initial Selection Control Block	Stkd	Stacked
CTLR	Controller			Stat	Status
CU	Control Unit	K	Key	TCS	Two Channel Switch
CI	Control Interface	MCI	Miscellaneous Control Information		
Corr	Correctable			Uncorr	Uncorrectable
Curr	Current	ODE	Outstanding Device End	'XX'	Hex Number
Def/Alt	Defective/Alternate			3/6	Three-of-six code
Drv	Drive	Ovrn	Overrun		

0200 to 03FC

8 bytes

Ctrl 0	Ctrl 1	Ctrl 2	Ctrl 3
0300	0380	0200	0280
0308	0388	0208	0288
0310	0390	0210	0290
0318	0398	0218	0298
0320	03A0	0220	02A0
0328	03A8	0228	02A8
0330	03B0	0230	02B0
0338	03B8	0238	02B8
0340	03C0	0240	02C0
0348	03C8	0248	02C8
0350	03D0	0250	02D0
0358	03D8	0258	02D8
0360	03E0	0260	02E0
0368	03E8	0268	02E8
0370	03F0	0270	02F0
0378	03F8	0278	02F8

FM	Cyl	Hd	3/6	Bytes Read			
Corr Data Checks		Uncorr Data Check		Seek Usage		Def/ Alt Head	Seek Errs

Usage/Error Records

Device 0
Device 1
Device 2
Device 3
Device 4
Device 5
Device 6
Device 7

0400 to 04FC 0500 to 05FC

0400	0500
DIAGNOSTIC OVERLAY BUFFER	DIAGNOSTIC OVERLAY BUFFER
04FC	05FC

0600 to 06FC

8 bytes

0600	C	C	H	H	R	K_L	D_H	D_L
0608	Dev. Type Pointer					3340 Only		
	'04'	'08'	'0C'	'10'		SD_2	SD_1	SD_2
0610	'80'	'40'	'20'	'10'	'08'	'04'	'02'	'01'
0618	'00'	'10'	'20'	'30'	'40'	'50'	'60'	'70'
0620	FM	Cyl	Hd	3/6	Number of Bytes Read			
0628	Corr Data Checks		Uncorr Data Checks		Num of Seeks			Seek Errs
0630	SA = Search results for first half of split key (3340)				ECC			
0638	ECC				ECC			
0640	0 Sense Bytes 3				4 Sense Bytes 7			
0648	8 Sense Bytes 11				12 Sense Bytes 15			
0650	16 Sense Bytes 19				20 Sense Bytes 23			
0658	Device Type Pointer (3340)							
	'04'	'08'	'02'	'0C'	'10'	'14'	'18'	'1C'
0660	Log				Log			
0668	Log				Log			
0670	Log				Log			
0678								

Service-plugged Device

† See INTR 005 for feature information.

0600 to 06FC

8 bytes

Selective System Reset

0680	Contingent Connection					Sense Control Block		
	'F0'		Last Stat Pres	CU/ Dev Addr				
0688	DCC Device Address (BSDA)				Hot Bit Constants			
	CTLR 0	CTLR 1	CTLR 2 †	CTLR 3 †	'FF	'FF'	'FF'	'FF'
0690	Chan A		CTLR 0		Chan B		CTLR 0	
	Res	EDI	ODE	PCH	Res	EDI	ODE	PCH
0698	Chan A		CTLR 1		Chan B		CTLR 1	
	Res	EDI	ODE	PCH	Res	EDI	ODE	PCH
06A0	Chan A		CTLR 2 †		Chan B		CTLR 2 †	
	Res	EDI	ODE	PCH	Res	EDI	ODE	PCH
06A8	Chan A		CTLR 3 †		Chan B		CTLR 3 †	
	Res	EDI	ODE	PCH	Res	EDI	ODE	PCH
06B0¤	Chan C		CTLR 0		Chan D		CTLR 0	
	Res	EDI	ODE	PCH	Res	EDI	ODE	PCH
06B8¤	Chan C		CTLR 1		Chan D		CTLR 1	
	Res	EDI	ODE	PCH	Res	EDI	ODE	PCH
06C0¤	Chan C		CTLR 2 †		Chan D		CTLR 2 †	
	Res	EDI	ODE	PCH	Res	EDI	ODE	PCH
06C8¤	Chan C		CTLR 3 †		Chan D		CTLR 3 †	
	Res	EDI	ODE	PCH	Res	EDI	ODE	PCH
06D0¤	Available to Channel A				Available to Channel B			
	CTLR 0	CTLR 1	CTLR 2 †	CTLR 3 †	CTLR 0	CTLR 1	CTLR 2 †	CTLR 3 †
06D8¤	Available to Channel C				Available to Channel D			
	CTLR 0	CTLR 1	CTLR 2 †	CTLR 3 †	CTLR 0	CTLR 1	CTLR 2 †	CTLR 3 †
06E0	Inline Sense				Inline Sense			
06E8	Inline Sense				Inline Sense			
06F0	Inline Sense				Inline Sense			
06F8								

¤ With Two Channel Switch Additional. For machines without Two Channel Switch Additional, contents of 06D0-06D7 are located at 06B0-06B7, and locations 06B8-06DF are not used.

0700 to 07FC

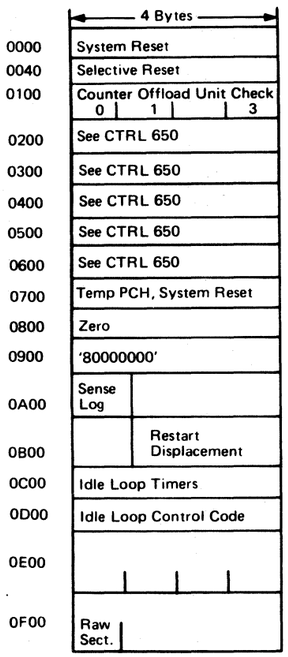
0700
BUFFER (READ/SEARCH COUNT AND KEY FIELDS)
07FC

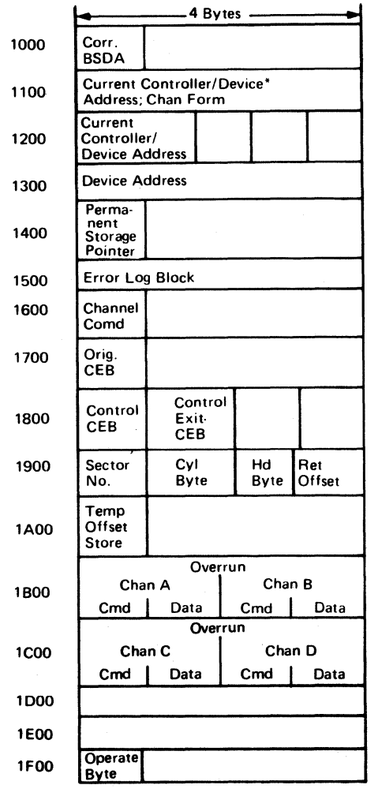
CONTROL STORAGE CONTENTS (Part 2 of 2)

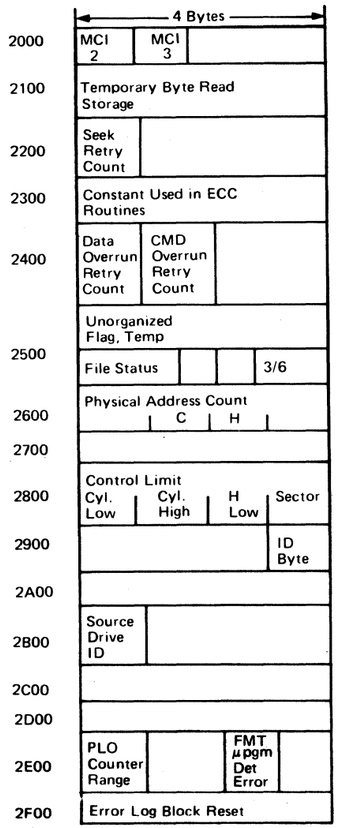
WORKING STORAGE (CONTINUED)

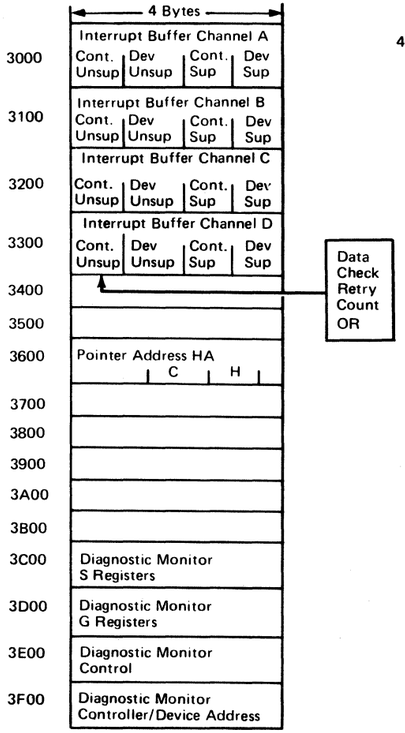
Zero Boundary Storage

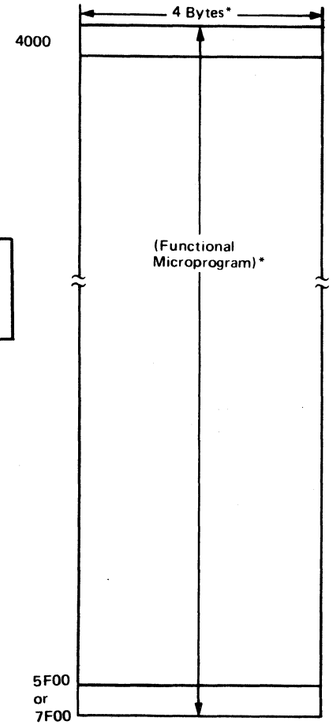
- The four bytes at the start of each even hundred block (0000, 0100, 0200-0800, 0900, to 3F00, 5F00†, or 7F00†) not covered on CTRL 650 are used for working storage.











†See INTR 005 for feature information.

CONTENTS

MPL (23FD)

PREFACE

READING ORDER

To become familiar with the theory and maintenance of the 23FD Disk Drive, read diagrams in the following order:

MPL5
MPL 10
MPL 45
MPL 25
MPL 2

In the maintenance situation, refer to the appropriate section as referenced from the START section or error dictionary. However, certain maintenance procedures are relatively critical, hence are recommended reading:

MPL 15
MPL 30

Notes:

1. *In this manual, the terms MPL and 23FD refer to one and the same file.*
2. *Stage I files have metal base plates. Stage II files have plastic baseplates. An identifying name plate is located next to the drive motor on Stage II models.*

CAUTIONS

The 23FD can be damaged by improper operation or improper servicing techniques. These are described under the appropriate servicing procedure. The most significant are listed below.

Heads and Head/Arm Assemblies

Handle assemblies with care:

- Avoid damage to head or arm.
- Avoid deformation of assembly flexure spring.
- Avoid loss of precise head setting within the arm.

SLT Card Removal/Insertion

Turn off dc power before removing or inserting SLT cards. Be sure that cards are properly seated in their sockets before turning power back on.

Cartridge Handling (See MPL 2)

SAFETY

Be aware of the following hazards:

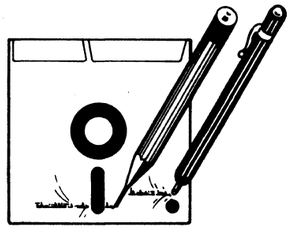
- AC and dc power are turned on under control of the control unit.
- AC power is present on connector terminals in the machine while the drive motor is energized.
- Objects can contact 208/230 volt connections despite safety shields.

CARTRIDGE HANDLING

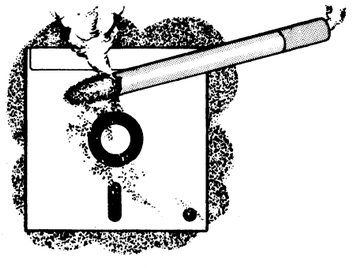
The 23FD disk cartridge contains information vital to system operation which may not be easily duplicated. HANDLE THE CARTRIDGE WITH CARE!

CAUTIONS

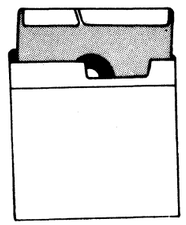
- NO PENS OR PENCILS Never write on disk cartridge. Writing pressure damages disk.



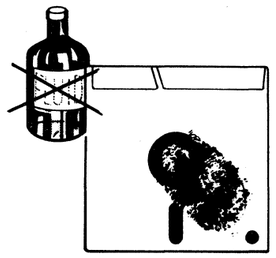
- NO SMOKING while handling cartridges.



- RETURN CARTRIDGE TO ENVELOPE whenever it is removed from the 23FD.

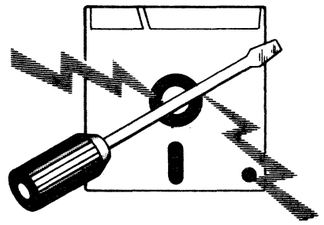


- DO NOT TOUCH OR CLEAN the disk surface.

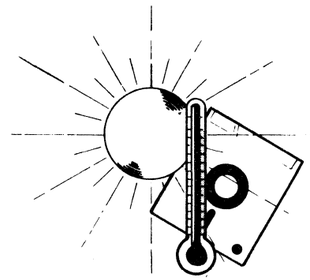


- REPLACE CARTRIDGE ENVELOPES when they become worn, cracked, or distorted.

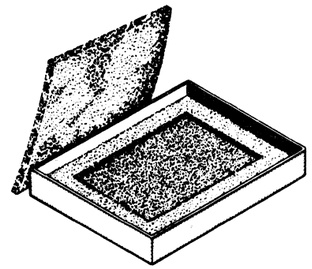
- KEEP CARTRIDGE AWAY FROM MAGNETIC FIELDS and ferromagnetic materials which may have become magnetized.



- DO NOT EXPOSE CARTRIDGES TO HEAT OR SUNLIGHT.

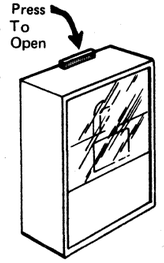


- STORE CARTRIDGES in the 23FD rack or in their original shipping cartons.



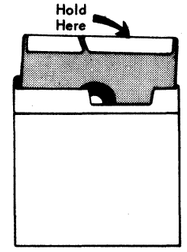
CARTRIDGE INSERTION

1 ACCLIMATE CARTRIDGES to the computer room before using:
If in mailing carton---------- wait 24 hours.
If not in mailing carton----- wait 1 hour.
If mounted on a non-powered file---------- wait 1/2 hour.



2 OPEN COVER. Do not open cover too wide as hinges may become damaged.

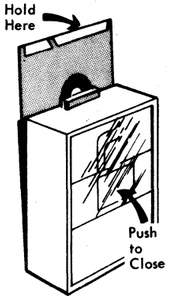
3 REMOVE CARTRIDGE. Grasp the cartridge by its white handling area and remove it from its envelope.



4 INSERT CARTRIDGE. Lower the cartridge squarely until it is stopped by the locating surfaces.

5 CLOSE COVER carefully. The 23FD centering cone must slide freely into the center of the disk. If not, check that the cartridge is seated against the 23FD locating surfaces and that the cartridge is not damaged.

6 Return the empty cartridge envelope to the 23FD disk storage rack.



CARTRIDGE REMOVAL

1 OPEN COVER.

2 LIFT CARTRIDGE. Grasp the cartridge by its white handling area and lift it straight up.

3 Slide the cartridge into its envelope and return it to the 23FD disk storage rack or to the storage area.

STORING CARTRIDGES

Place cartridges in their envelopes and store them either in the 23FD storage rack or in their original mailing cartons. A storage environment must be free of magnetic fields and must meet the following environmental criteria:

Temperature---------- 40°to 100°F (5° to 38° C)
Relative Humidity-------- 8% to 80%
Maximum Wet Bulb Temperature---------- 80°F(27°C)

SHIPPING AND RECEIVING

SHIP CARTRIDGES inside the original shipping carton. Additional shipping cartons are available at IBM Branch Offices. With the cartridge in place, the package weighs 10 ounces. Be sure to lable the package "DO NOT EXPOSE TO HEAT OR SUNLIGHT."

WHEN RECEIVING CARTRIDGES, check for carton and cartridge damage. Save the carton for storing a cartridge and for possible cartridge shipment at some future date.

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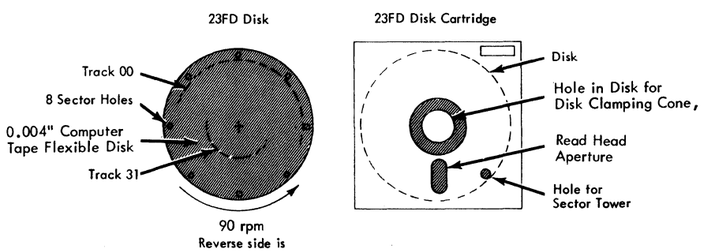
FUNCTIONAL PRINCIPLES, OPERATING SEQUENCE (STAGE I ONLY)

FUNCTIONAL PRINCIPLES

- The 23FD Disk Drive is a direct-access, read-only file used with computers and storage control systems for:
  1. Initial control program load.
  2. Microprogram storage backup.
  3. Diagnostic microprogram storage.
- The disk is prerecorded, interchangeable on any file, mailable, and "throw away".
- Data areas on the disk may be reached in random sequence.
- Data format, prewritten on the disk, is determined by the requirements of the Control Unit (CU).

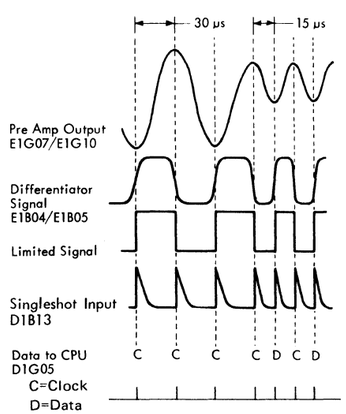


OPERATING SEQUENCE

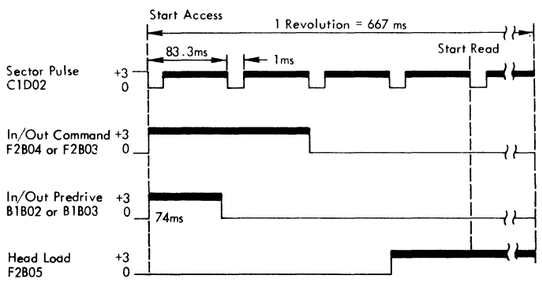
1. Operator installs disk cartridge and closes cover. Cover pushes positioning cone into the drive hub, clamping the disk in place.
2. DC power comes on under control of CU. AC power to motor comes on under control of CU. Disk turns.
3. Sector pulses are read. CU provides 4-second delay after motor comes on before sector pulses are recognized by the adapter.
4. Head engage signal is developed in CU upon completion of 4-second delay. Pressure pad pushes flexible disk against read head. One sector time (83.3 ms) after head engage signal comes up, data can be gated to the system.
5. Read data from the read head is in the form of a sine-wave signal that varies from 16.7 kHz (all 0's) to 33.3 kHz (all 1's). The signal is amplified and shaped to provide both clock and data pulses via the file data line to the data separator in the CU.
6. In or Out command causes the access stepping motor to rotate a lead screw 30° clockwise or counterclockwise each time a command is received from the CU. A lead screw rotation of 30° moves the read head one track position. The pressure pad is not unloaded during accessing operations.

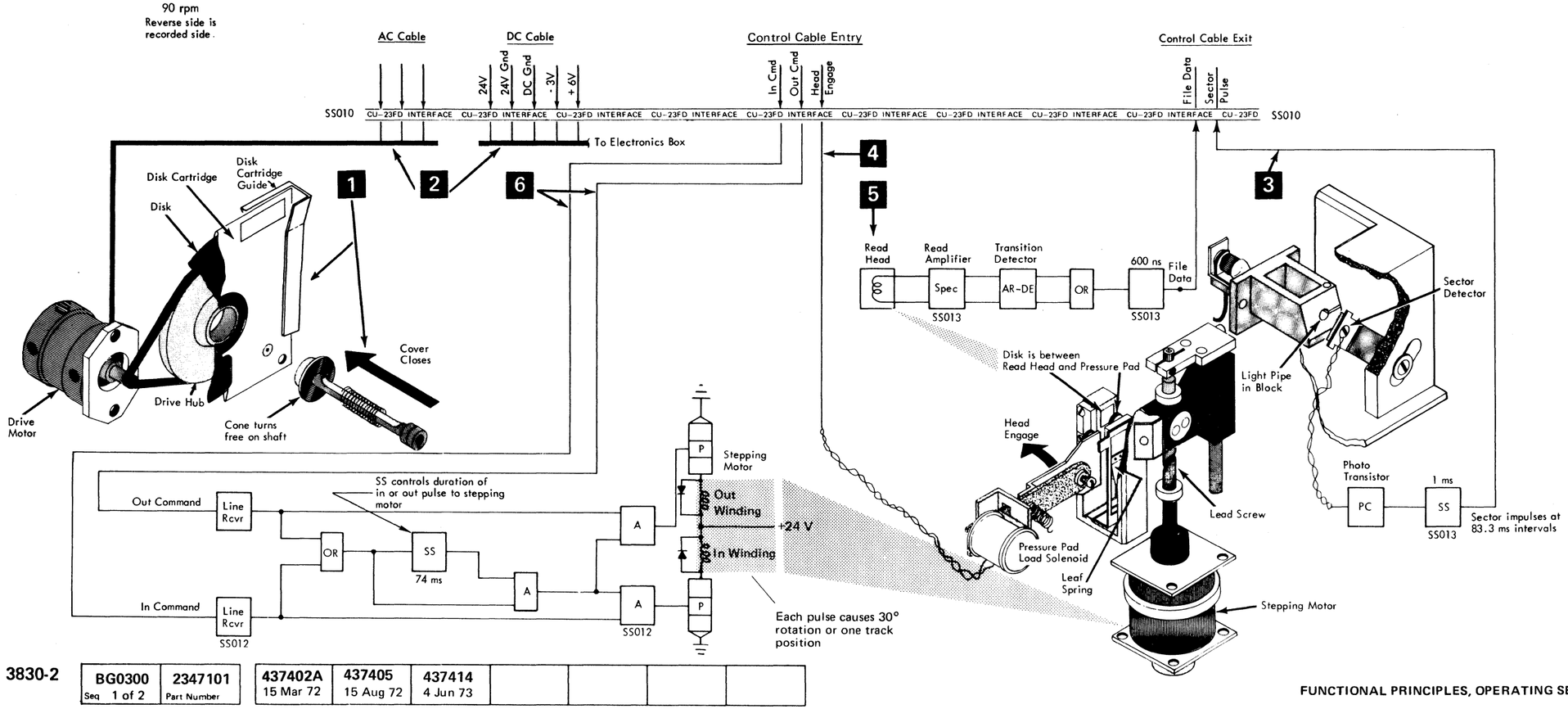
   Head disengages. If a read or access operation is not signaled within any 8-sector time period, the head engage line line is dropped by the CU.

READ CHANNEL TIMING



23FD TIMING





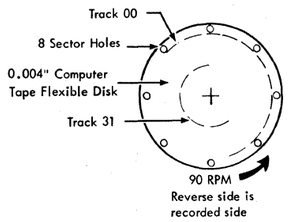
FUNCTIONAL PRINCIPLES, OPERATING SEQUENCE (STAGE II ONLY)

FUNCTIONAL PRINCIPLES, OPERATING SEQUENCE (STAGE II ONLY)

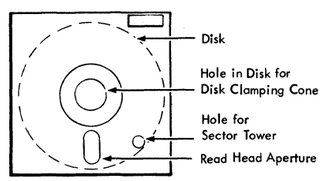
FUNCTIONAL PRINCIPLES

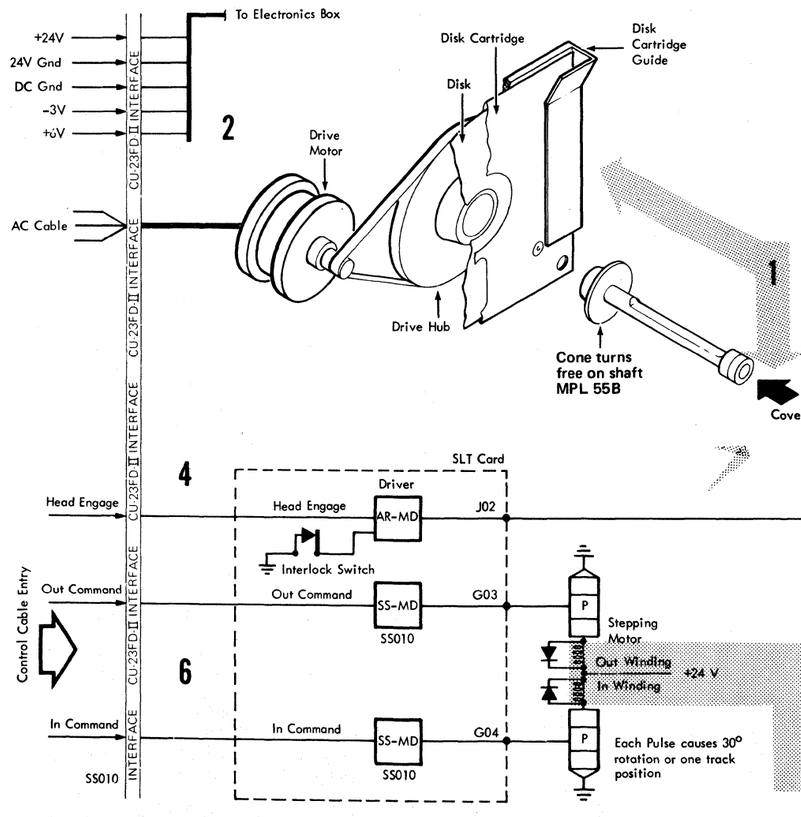
- The 23FD-II Disk Drive is a direct-access, read-only file used with computers and storage control systems for:
  1. Initial control program load
  2. Microprogram storage backup
  3. Diagnostic microprogram storage
- The disk is prerecorded, interchangeable on any file, mailable, and "throw away".
- Data areas on the disk may be reached in random sequence.
- Data format, prewritten on the disk, is determined by the requirements of the Control Unit (CU).

23FD-II Disk



23FD-II Disk Cartridge





OPERATING SEQUENCE

1. Operator installs disk cartridge and closes cover. Cover pushes positioning cone into the drive hub thus clamping the disk in place.
2. DC power comes on under control of CU. AC power to motor comes on under control of CU. Disk turns.
3. Sector pulses are read. CU provides 4-second delay after motor comes on before sector pulses are recognized by the adapter.
4. Head engage signal is developed in CU upon completion of 4-second delay. Pressure pad pushes flexible disk against read head. One sector time (83.3 ms) after Head Engage signal comes up, data can be gated to the system.
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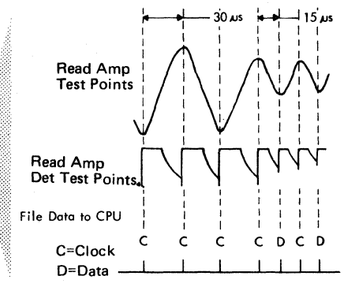
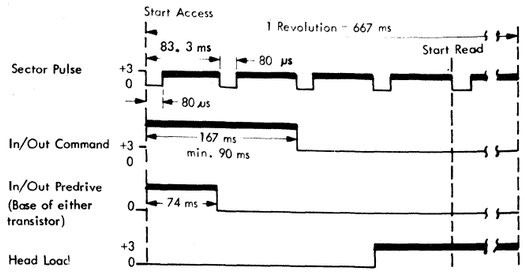
6. In or Out command causes the access stepping motor to rotate a lead screw 30° clockwise or counterclockwise each time a command is received from the CU. A lead screw rotation of 30° moves the read head one track position. The pressure pad is not unloaded during accessing operations.

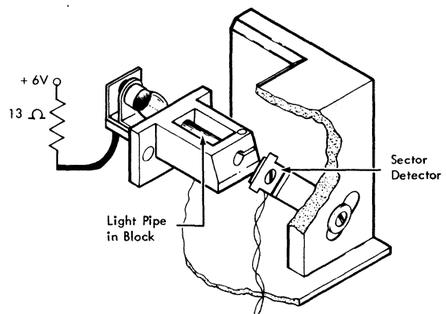
   Head disengages. If a read or access operation is not signaled within any 8-sector time period, the head engage line is dropped by the CU.

Read Channel Timing

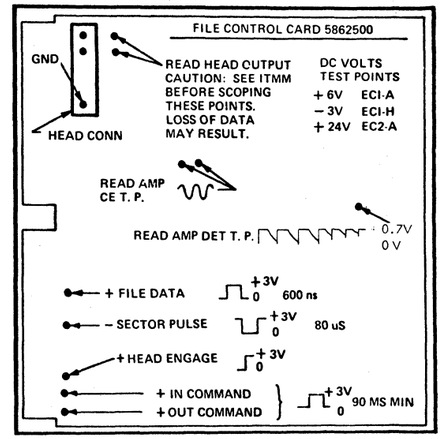


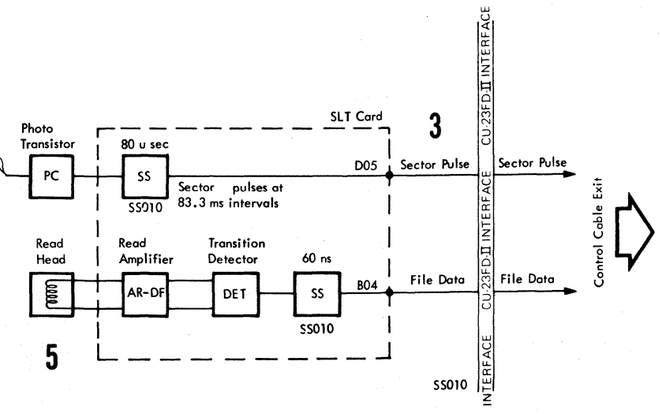
23FD-II Timing

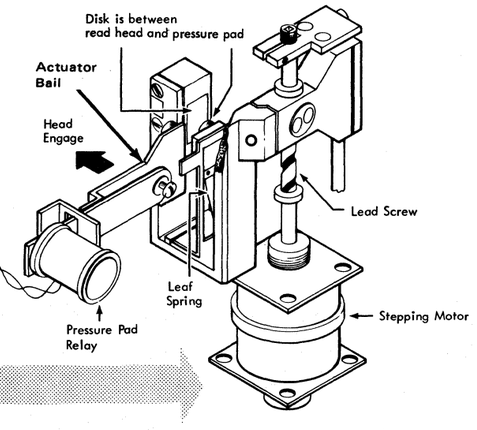




File Control Card Label







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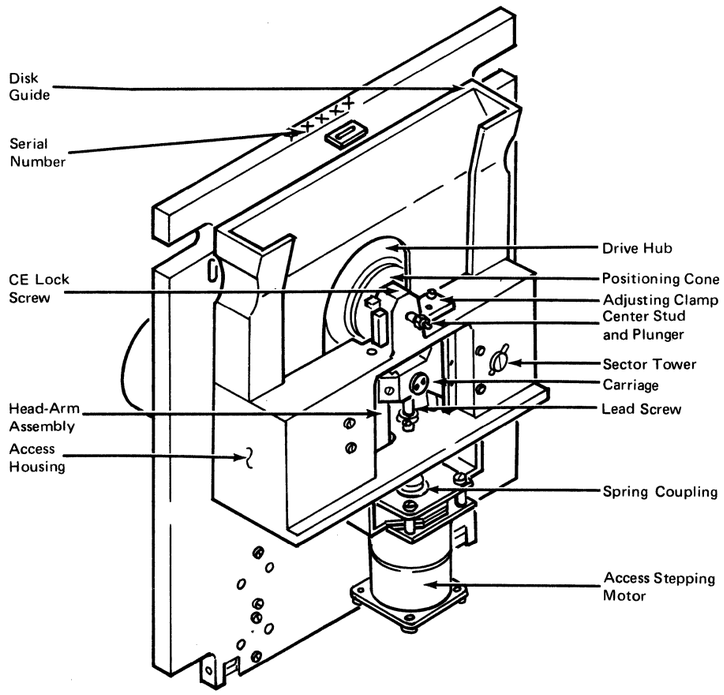
MACHINE CHARACTERISTICS, LOCATIONS (STAGE I ONLY)

CHARACTERISTICS

Disk rotational speed	90 revolutions per minute (RPM) counterclockwise viewed from the front.
Sectors per track	8
Capacity	Track: 20,416 bits Disk: 653,312 bits
Recording technology	Track density: 32 Tracks/In (32 tracks per 25.4 mm) Disk diameter: 7.5 in. (190.5 mm)
Access mechanism	Actuator: Stepping Motor Access motion time, single step: 333.3 ms Rotational period: 666.7 ms

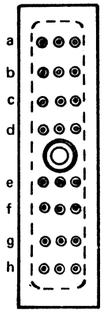
LOCATIONS

Front View, Cover Removed

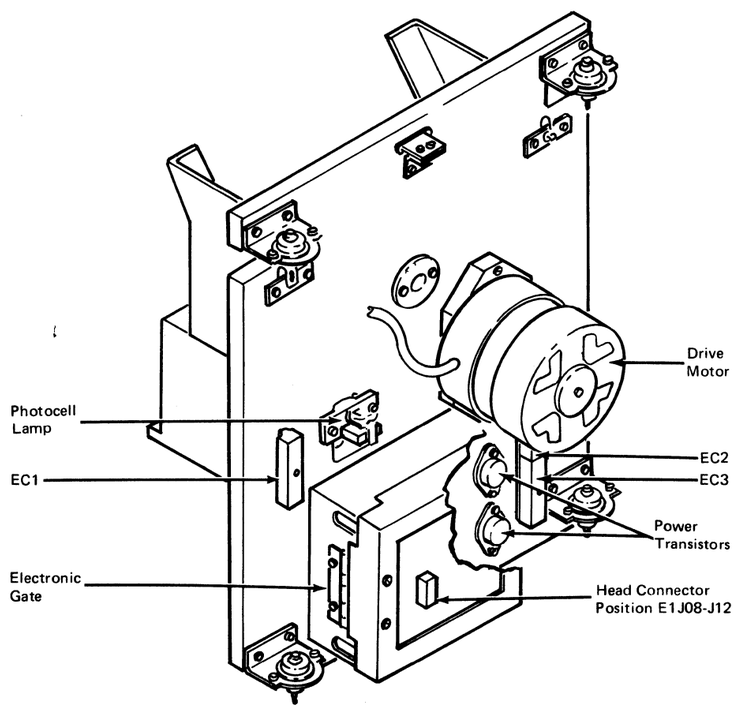


Edge Connector

Pin Identification for EC-1, EC-2, EC-3.



Rear View



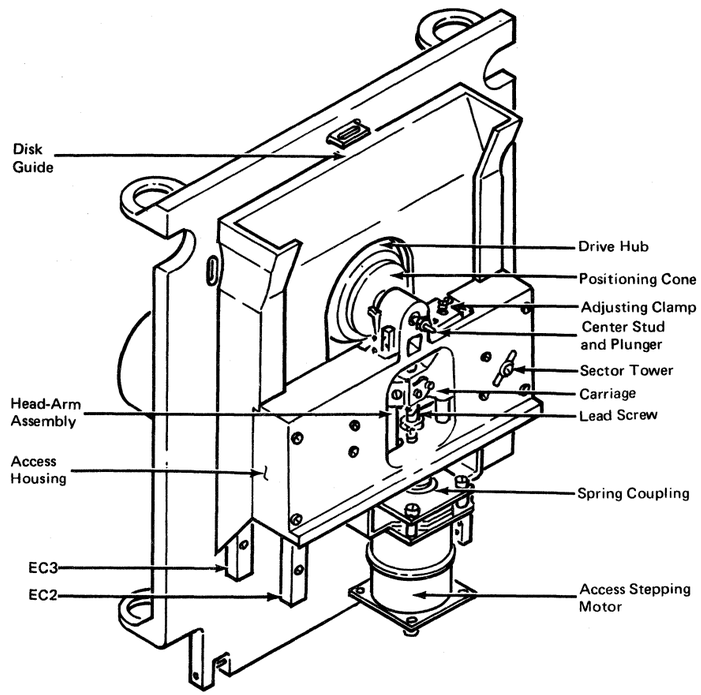
MACHINE CHARACTERISTICS, LOCATIONS (STAGE II ONLY)

CHARACTERISTICS

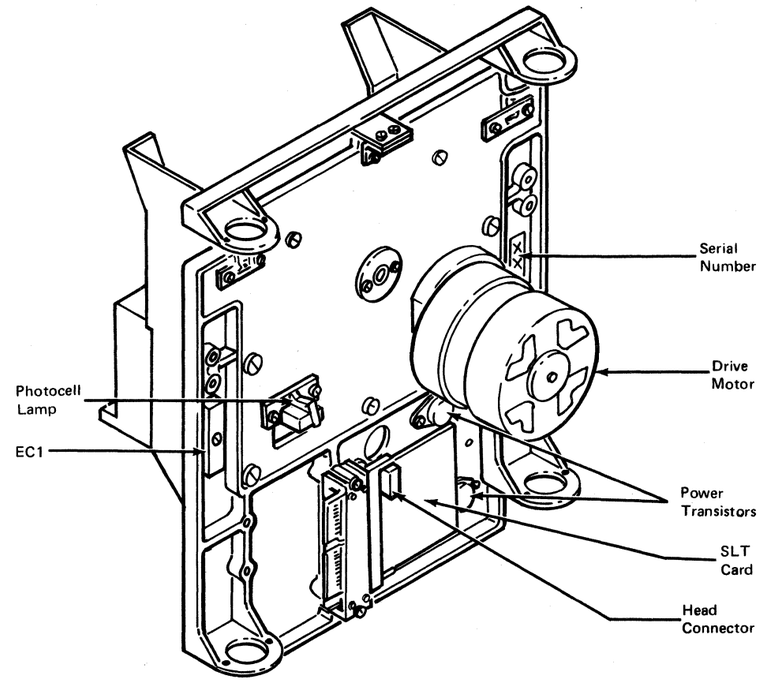
Disk rotational speed	90 revolutions per minute (RPM) counterclockwise viewed from the front.
Sectors per track	8
Capacity	Track: 20,416 bits Disk: 653,312 bits
Recording technology	Track density: 32 Tracks/In (32 tracks per 25.4 mm) Disk diameter: 7.5 in. (190.5 mm)
Access mechanism	Actuator: Stepping Motor Access motion time, single step: 333.3 ms Rotational Period: 666.7 ms

LOCATIONS

Front View, Cover Removed

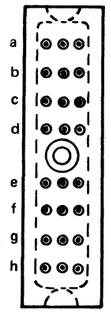


Rear View



Edge Connector

Pin Identification for EC-1, EC-2, or EC-3



MPL FILE READ CHECK (STAGE I ONLY)

MICRO 16 START 65

Byte of data received with bad parity or a checksum error was detected

MPL 20A

Remove disk and visually check for scratches down to the substrate. If disk is scratched, replace the head/arm assembly. If not, proceed below.

Replace disk and execute IMPL

Machine still fails — No → READ CIRCUIT DIAGNOSTIC

Yes

ACCESS DRIVE MECHANICAL DIAGNOSTIC

MPL 50A

Check for excessive motion in the head, carriage, and lead screw

OK — Yes → READ CIRCUIT DIAGNOSTIC

No

Spring coupling setscrew loose — Yes → MPL 20A, 50A: Repair and adjust alignment

No

Motion continues into stepping motor — Yes → MPL 50A: Replace stepping motor and adjust alignment

No

Stylus screws and condition of stylus — Loose/Defective → Repair and adjust alignment

OK

MPL 50A: Replace lead screw or head carriage

READ CIRCUIT DIAGNOSTIC

Five cards can cause this failure. If spare cards are available, replace them one at a time and check if the machine still fails.

1. 23FD card A1E1
2. 23FD card A1D1
3. CU card B1T4
4. CU card B1S2
5. CU card B2S2

Machine still fails — Yes → READ CIRCUIT DIAGNOSTIC

No

Re-IMPL to test and return unit to customer

MPL 25A

Scope head output and head alignment. Align if needed

Machine still fails — No → READ CIRCUIT DIAGNOSTIC

Yes

Head output good — No → **Check the following in MPL drive: pressure pad loading and force (MPL 20A) coax cable for noise, grounding, continuity, resistance, etc. (MPL 25A). Flex coax and cables while checking.**

Yes — Probably a card failure

MPL 25A: Scope file data at drives A1D1G05

OK — Yes → MPL 25A: Scope file data in CU, B1T4D12.

No

MPL 25A: Scope read amplifier output. Drive card A1E1G07 and G10.

OK — No → Replace A1D1 / Replace A1E1

Yes

OK — Yes → **Replace CU card B1T4**

No

Machine still fails — Yes → READ CIRCUIT DIAGNOSTIC

No

Replace CU cards B1S2 and B2S2

Machine still fails — Yes → READ CIRCUIT DIAGNOSTIC

No

B → MPL30A

PROCEDURES FOR SCOPING MPL FILE DATA

NORMAL PROCEDURE

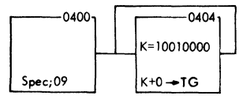
1. **Set Mode switch to CE Normal mode**
2. **Reset**
3. **Press IMPL**
4. Operate Seek/Head Load switch to Load Head
5. Sync on Sector Pulse, B1T4J04
6. Scope data

ALTERNATE PROCEDURE

If the normal procedure fails to start the motor, or load the head, perform the following:

1. Set Mode switch to CE Normal mode .
2. Enter this microprogram manually

   0400= 00 09 70 01
   0404= 90 73 D0 01



Start MPL File — Load Head and Raise Read Gate

3. Set IAR to 0400
4. Start
5. Sync on Sector Pulse, B1T4J04
6. **Scope data.**
7. Reset to stop program and unload head
8. To restart, repeat steps 3 and 4

MPL FILE READ CHECK (STAGE II ONLY)

MPL 15B

ACCESS DRIVE MECHANICAL DIAGNOSTIC

MICRO 16
START 65

Byte of data was received with bad parity or a check sum error was detected

MPL 20B

Remove disk and visually check for scratches down to substrate. If scratched, replace head. If not, proceed below

Replace disk and execute IMPL

Machine still fails — No

Yes

MPL 50B

Check for excessive motion in the head carriage and lead screw

OK — No

Yes

Five cards can cause this failure. If spares are available, replace them one at a time and check whether machine still fails:
1. Drive SLT card.
2. CU card B1T4.
3. CU card B1S2.
4. CU card B2S2.
5. CU card B2N2

Machine still fails — No

Yes

(1)

Spring coupling setscrew loose — Yes — MPL 20B MPL 50B — Repair and adjust

No

Motion continues into stepping motor — Yes — MPL 20B MPL 50B — Replace stepping motor perform alignment

No

Check stylus screws and condition of stylus — Loose/Defective — MPL 20B MPL 50B — Repair and adjust

OK

MPL 50B

Replace lead screw or head carriage

Test by re-IMPL and return unit to customer

READ CIRCUIT DIAGNOSTIC

(1)

MPL 25B

Scope head output and head alignment. Adjust if needed.

Machine still fails — No — (2)

Yes

Head output good — No

Yes — Probably a card failure

MPL 25B

Scope file data at drive

OK — Yes

No

MPL 25B — LA101

Scope file data in CU, B1T4D12

SS010

Replace MPL drive SLT card

OK — Yes

No

Replace CU cards: B1S2, B2S2

Replace CU card: B1T4

(2)

Machine still fails — Yes

No

MPL 20B MPL 25B

Check the following in the MPL drive; pressure pad loading and force; coax for noise grounding, continuity, resistance. Flex coax and cables while checking.

Machine still fails — Yes

No

(2)

B

MPL 30B

Machine still fails — No — Yes

Test by re-executing IMPL and return unit to customer

B

MPL 30B

Procedures for Scoping MPL File Data

NORMAL PROCEDURE

1. Place in CE Normal Mode.
2. Reset.
3. Press IMPL.
4. Operate Seek/Head Load switch to Load Head.
5. Sync on Sector Pulse, B1T4J04.
6. Scope Data.

ALTERNATE PROCEDURE

If the normal procedure fails to start the motor, or load the head, perform the following:

1. Place in CE Normal Mode.
2. Enter this microprogram manually:

```
0400  00 09 70 01
0404  90 73D0 01
```


Start MPL File — Load Head and Raise Read Gate

3. Set IAR to 0400.
4. Start.
5. Sync on Sector Pulse, B1T4J04 (LA101).
6. Scope data.
7. Reset to stop program and unload head.
8. To restart, repeat steps 2 and 3.

BG0500	2347103
Seq 2 of 2	Part Number

437402A	437405	437408	437414			
15 Mar 72	15 Aug 72	16 Oct 72	4 Jun 73			

READ HEAD (STAGE I ONLY)

READ HEAD RADIAL POSITION ALIGNMENT

Radial alignment for the read head is accomplished by adjusting the read head to the center of two eccentrically written tracks on the CE disk. When properly aligned, the read head is positioned on track 15.

Before adjusting, entire assembly should be exposed to ambient conditions for at least two hours.

Check Alignment may be checked by performing steps 1, 2, 3, 4, and 11 below.

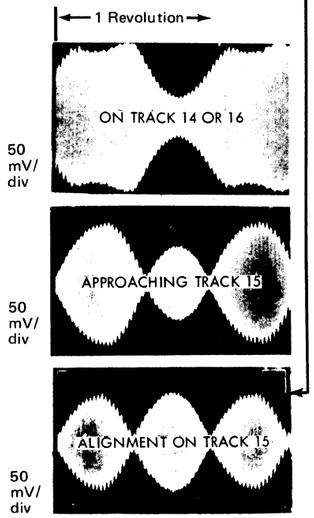
Adjustment

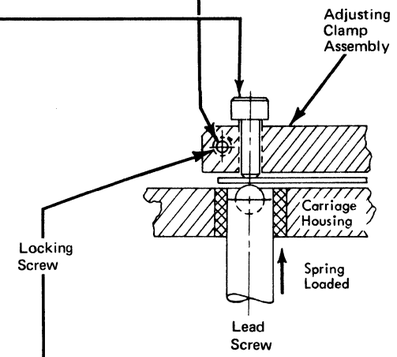
1. Remove cover. Clamp CE disk to drive hub, using CE lock screw (MPL 10A).
2. Power-up MPL file by setting mode switch to CE Normal, pressing Reset, and pressing IMPL. Be sure that rotation of disk is maintained with cone shaft locked in position by CE lock screw.
3. Access head to track 15; use Seek/Load switch and leave head in loaded state.
4. Connect scope to observe read amplifier output at E1G07 and E1G10 differentially. Use direct probes. Set trigger mode to Auto, input controls to AC Add, one input inverted, 50 mV/div, sweep speed at 0.1 sec/div.

   Note: Avoid direct light on scope face. Use hood (P/N 453201).
5. Loosen locking screw.
6. Turn adjusting screw so amplitude of adjacent lobes is equal within 10%.

E1G07
E1G10
Differentially

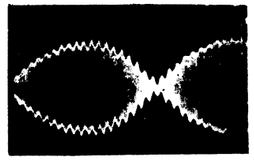
(Actual trace may not be the same as these representations)





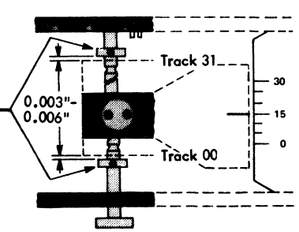
7. Tighten locking screw slightly. This completes rough adjustment.
8. Change time base to 50ms/div, uncalibrated. Adjust time base between 50 and 100 ms until 1-1/2 lobes are seen and lobes are stationary on screen. Scope sync is now on a specific sector pulse.
9. Make fine adjustment by turning adjusting screw so amplitude of adjacent lobes is equal within 25%.

E1G07
E1G10
Differentially



10. Tighten locking screw firmly.
11. Check by accessing off track 15 several steps, return to track 15 and check null amplitude. Repeat from opposite direction. Amplitude of adjacent lobes must be equal within 25%. Readjust if necessary.
12. With head at track 15, set track indicator scale at track 15.
13. Check top and bottom limit clamps for tracks 31 and 00. Adjust if necessary.

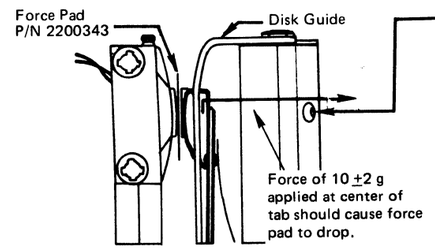
Limit Clamps



HEAD/ARM ASSEMBLY

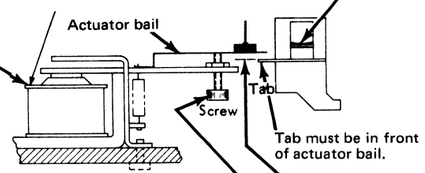
Pressure Pad Load Force Check

Make check with head/arm assembly removed from carriage. Replace head/arm assembly if check fails.

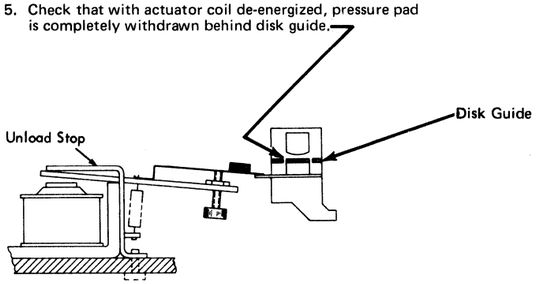


Pressure Pad Load - Unload Actuator Adjustment

1. Energize actuator coil (24V).
2. Check that pressue pad is contacting head.



3. Turn so actuator bail just touches tab.
4. Advance screw 1/4 to 3/4 turn to get clearance at all track positions.
5. Check that with actuator coil de-energized, pressure pad is completely withdrawn behind disk guide.



Removal

1. Turn off all power. Remove disk.
2. Unplug head connector at E1J08-J12. Note routing of head cable. Cable must be replaced in same position.
3. Remove screw.

Replacement

1. Check pressure pad load force (this page). Replace head/arm assembly if force is outside specification.
2. Place head/arm assembly in position against stop. Be sure that tab is not behind actuator bail.
3. Tighten screw.
4. Route head cable as noted during removal. (Loop must be large enough to allow accessing to all tracks.)
5. Perform:
   - Pressue pad load-unload actuator adjustment (this page).
   - Read head radial position alignment (this page).
   - Sector tower adjustment (MPL 35A).

BG0600 Seq 1 of 2	2347104 Part Number	437402A 15 Mar 72	437405 15 Aug 72	437414 4 Jun 73				

READ HEAD (STAGE II ONLY)

READ HEAD RADIAL POSITION ALIGNMENT

Radial alignment for the read head is accomplished by adjusting the read head to the center of two eccentrically written tracks on the CE disk. When properly aligned, the read head is positioned on track 15. Before adjusting, entire assembly should be exposed to ambient conditions for at least two hours.

Check Alignment may be checked as follows: Insert CE disk, access to track 15 (leave head in loaded state), and perform steps 2, 3, 8, and 14.

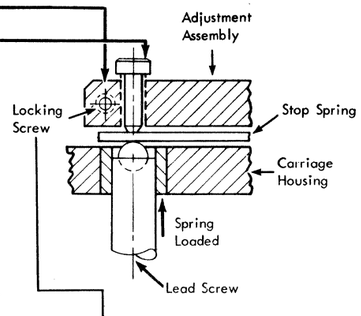
Adjustment

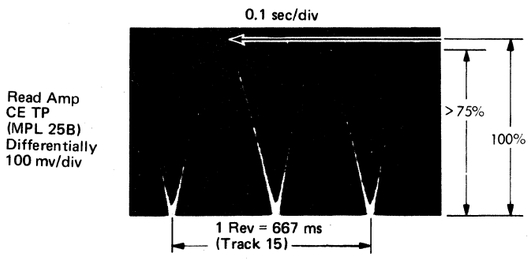
1. Remove disk and cover (MPL 55B).
2. Connect scope to read-amp CE test points (MPL 25B). Use X10 probes. Ground probes, using black wire connection on photocell light bulb.
3. Set trigger mode to Auto, input controls to AC Add, one input inverted (differential), 10 mV/div, sweep speed at 0.1 sec/div, and set baseline at bottom line of graticule.

   Note: Avoid direct light on scope face. Use hood (P/N 453201).

4. Using the Seek/Load switch, manually step head anywhere above track 20.
5. Loosen locking screw.
6. Turn adjusting screw CCW until stop spring is against the adjustment assembly.
7. Insert CE disk.
8. Set Mode switch to CE Normal, press Reset and IMPL.
9. Operate the Seek/Load switch (either direction), and leave head loaded.
10. Using a 1/4-inch socket, push center stud with sufficient force to rotate the disk. Hold in this position to keep disk rotating while making adjustment. (Do not grasp access housing as plastic may distort and cause inaccurate head alignment.)
11. Manually step the head assembly (seek out) until a signal appears on the scope. Step (seek out) one more track and turn adjusting screw clockwise until three lobes appear. Attempt to get picture shown below. If unobtainable, repeat step 6 and this step.
12. Snug-up locking screw. This is track 15.
13. Replace cover, but do not put cover guides through baseplate.
14. With cover closed, check scope trace. Amplitude of adjacent lobes should be equal within 25%. To readjust, open cover just enough to allow insertion of a hand to turn adjusting screw, then recheck scope trace with cover held closed.

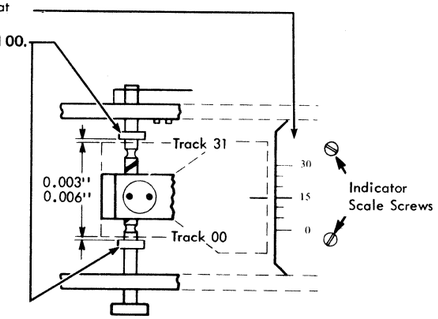
CAUTION
Opening the cover too wide will damage the hinges. Do not allow cover to drop.





Actual trace may not be the same as this representation.

15. Tighten locking screw firmly.
16. Check by accessing off track 15 several steps. Return to track 15 and check null amplitude. Repeat from opposite direction. Amplitude of adjacent lobes must be equal within 25%. Readjust if necessary.
17. With head at track 15, set track indicator scale at track 15.
18. Set top and bottom limit clamps for tracks 31 and 00.



PRESSURE PAD LOAD–UNLOAD ACTUATOR

Removal

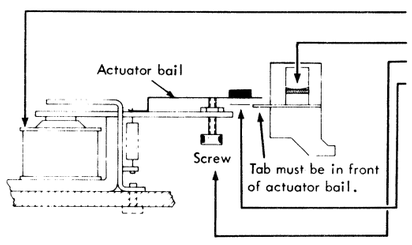
1. Turn off all power. Remove disk and cover (MPL 55B).
2. Remove access housing assembly (MPL 55B).
3. Remove two screws to remove solenoid assembly.

Replacement

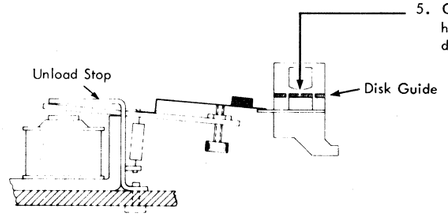
1. Reverse removal procedure to replace parts.
2. Adjust bail.

Adjustment

1. Energize actuator, reset, IMPL, and operate Seek/Head Load switch.
2. Check that pressure pad is contacting head.
3. Turn so actuator bail just touches tab.
4. Tighten screw 1/4 to 3/4 turn to get clearance at all track positions.



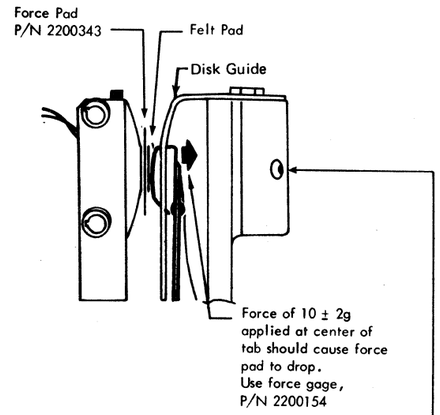
5. Check that with actuator coil de-energized, head pressure pad is completely withdrawn behind disk guide.



HEAD/ARM ASSEMBLY

Pressure Pad Load Force Check

Make check with head/arm assembly removed from carriage. Replace head/arm assembly if check fails.



Removal

1. Turn off all power. Remove disk and cover (MPL 55B).
2. Unplug head connector on SLT card. Note routing of head cable. Cable must be replaced in same position.
3. Remove screw.

Replacement

1. Check pressure pad load force (this page). Replace head/arm assembly if force is outside specification.
2. Place head/arm assembly in position against stop.

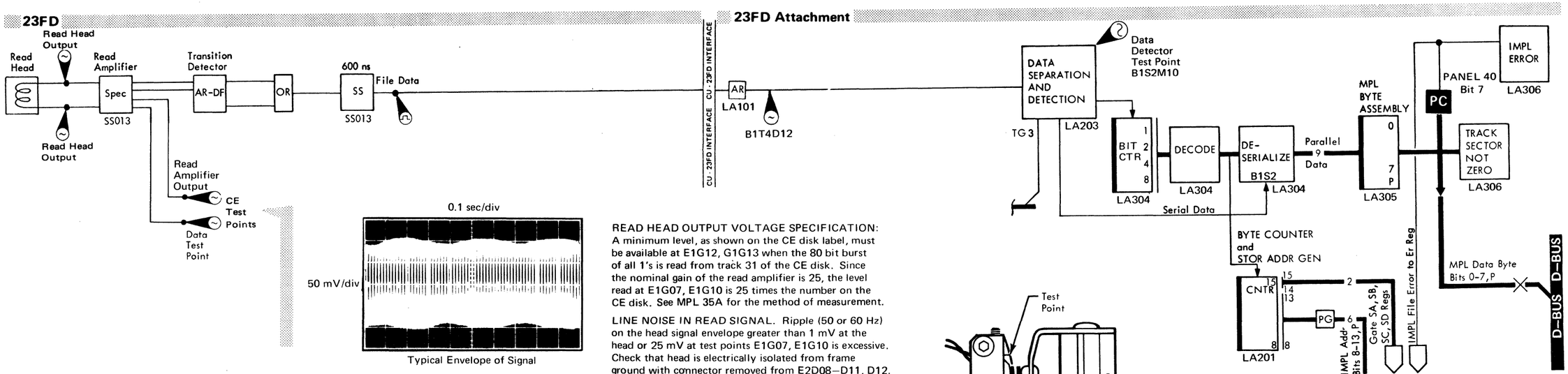
CAUTION
Be sure that tab is not behind cover bail

3. Tighten screw.
4. Route head cable as noted during removal. (Loop must be large enough to allow accessing to all tracks.)
5. Perform:
   - Pressure pad load-unload actuator adjustment (this page).
   - Read head radial position alignment (this page).
   - Sector tower adjustment (MPL 35B).

BG0600 Seq 2 of 2	2347104 Part Number	437402A 15 Mar 72	437405 15 Aug 72	437414 4 Jun 73				

READ CIRCUIT (STAGE I ONLY)

WAVEFORMS AND TEST POINTS



Typical Envelope of Signal

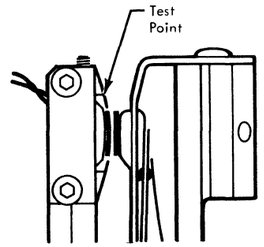
READ HEAD OUTPUT VOLTAGE SPECIFICATION: A minimum level, as shown on the CE disk label, must be available at E1G12, G1G13 when the 80 bit burst of all 1's is read from track 31 of the CE disk. Since the nominal gain of the read amplifier is 25, the level read at E1G07, E1G10 is 25 times the number on the CE disk. See MPL 35A for the method of measurement.

LINE NOISE IN READ SIGNAL. Ripple (50 or 60 Hz) on the head signal envelope greater than 1 mV at the head or 25 mV at test points E1G07, E1G10 is excessive. Check that head is electrically isolated from frame ground with connector removed from E2D08–D11, D12. Replace connector after measurement.

CAUTION
Don't measure head resistance with power on or with disk in machine. Erasure of data may result.

Don't touch face of head. Take measurement at test point.

The electrical resistance between the head, the base plate and the dc common must not exceed 1.0 ohms. Check for shorts between coil and arm assembly. The dc resistance of coil should be 70 ohms ±10%. The dc resistance between coil and arm assembly should be greater than 1 megohm. Check head alignment (MPL 20A).



This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

PRINCIPLES

Raw Read Data

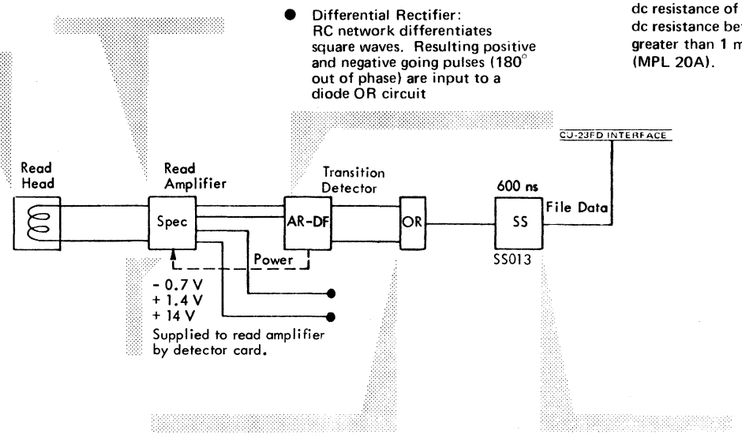
- Sine Wave Signal:
  16.7 kHz (All 0's)
  33.3 kHz (All 1's)
- Higher voltage at outer track because of higher disk speed and lower bit density.
- All 0's pattern gives higher voltage amplitude than all 1's.

Read Amplifier

- Input:
  1.5 to 30 mV (All 0's)
  0.75 to 20 mV (All 1's)
- Output:
  Minimum 1.86V P-P
  Maximum 5V P-P

Transition Detector Consists Of

- Limiter:
  High gain differential amplifier amplifies signal so one of amplifier transistors is cut off. Outputs of limiter are two out-of-phase square waves.
- Differential Rectifier:
  RC network differentiates square waves. Resulting positive and negative going pulses (180° out of phase) are input to a diode OR circuit



Diode OR Circuit

- Output is train of positive pulses
- Peaks of output pulses correspond to peaks in read signal.

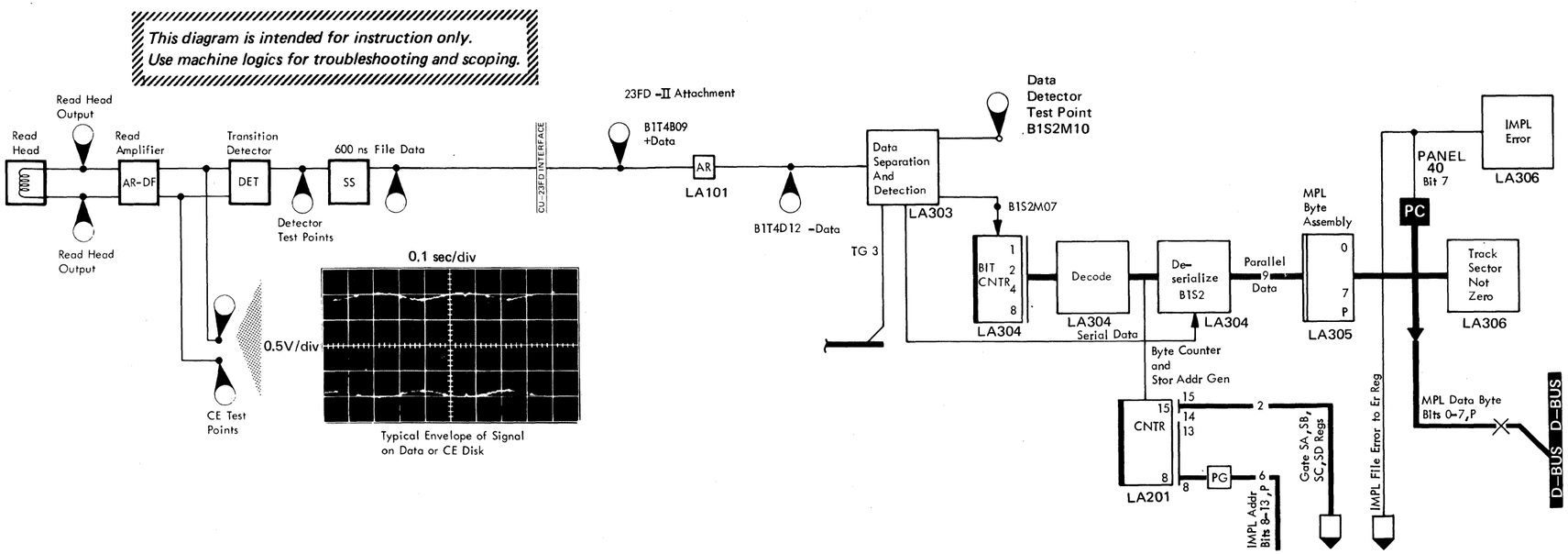
Single Shot

- OR circuit output pulses fed to SS cause 600 ns file data pulses.

READ CIRCUIT (STAGE II ONLY)

WAVEFORMS AND TEST POINTS

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.



PRINCIPLES

Raw Read Data

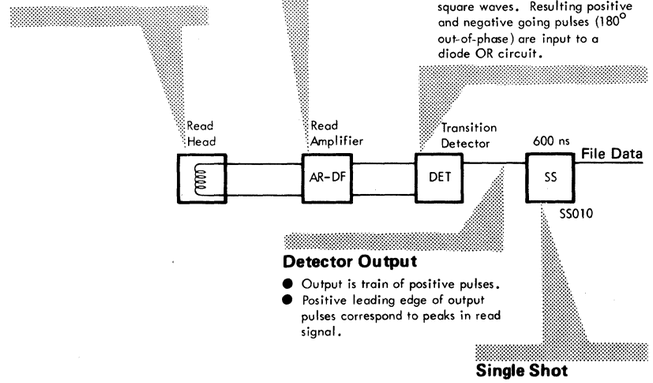
- Sine Wave Signal
  16.7 kHz (All 0's)
  33.3 kHz (All 1's)
- Higher voltage at outer track because of higher disk speed and lower bit density.
- All 0's pattern gives higher voltage amplitude than all 1's.

Read Amplifier

- Input
  1.5 to 30 mV (All 0's).
  .75 to 20 mV (All 1's).

Transition Detector Consists Of:

- Limiter:
  High gain differential amplifier amplifies signal so one of amplifier transistors is cut off. Outputs of limiter are two out-of-phase square waves.
- Differential Rectifier:
  RC network differentiates square waves. Resulting positive and negative going pulses (180° out-of-phase) are input to a diode OR circuit.



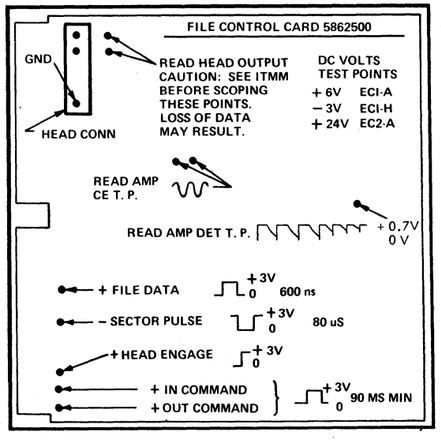
Detector Output

- Output is train of positive pulses.
- Positive leading edge of output pulses correspond to peaks in read signal.

Single Shot

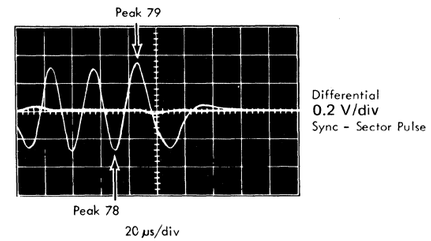
- Detector output pulses fed to SS cause 600 ns file data pulses.

FILE CONTROL CARD LABEL



READ HEAD OUTPUT CHECK

1. Insert CE Disk.
2. **Set Mode switch to CE Normal: operate reset switch.**
3. IMPL, then operate Seek/Load switch to access to track 31. Leave head loaded.
4. **Sync negative on leading edge of sector pulse (C1D02).** Set time base to 10 ms/div.
5. Scope read amplifier data differentially at CE test points, **and ensure waveform meets the following specification:**

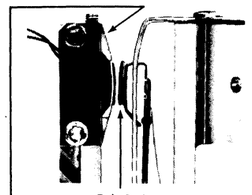


READ HEAD OUTPUT VOLTAGE SPECIFICATION: The voltage amplitude, measured between peaks 78 and 79 of the 80 bit burst on track 31 of a CE disk (figure above) must not be less than the number printed on the CE disk label as measured at the read head output or X100 at the read amp CE test points. If specification is not met, clean head with a rigid head cleaning tool, P/N 2200574, moistened (not soaked) with isopropyl alcohol. Do not allow alcohol to contact felt pad. Recheck amplitude. If unacceptable, replace head.

LINE NOISE IN READ SIGNAL: Ripple (50 or 60 hertz) on the head signal envelope greater than 1 mV at the head or 100 mV at read amp test points is excessive. This should be checked with scope probes grounded. Ground probes by using black wire connection on light bulb.

CAUTION:

- *Do not connect or disconnect scope probes to head test points with disk in machine. Loss of data by erasure may result.*
- *Do not measure head resistance with power on or with disk in machine. Erasure of data may result.*
- *Do not touch face of head.*
  Take measurement at card test points.



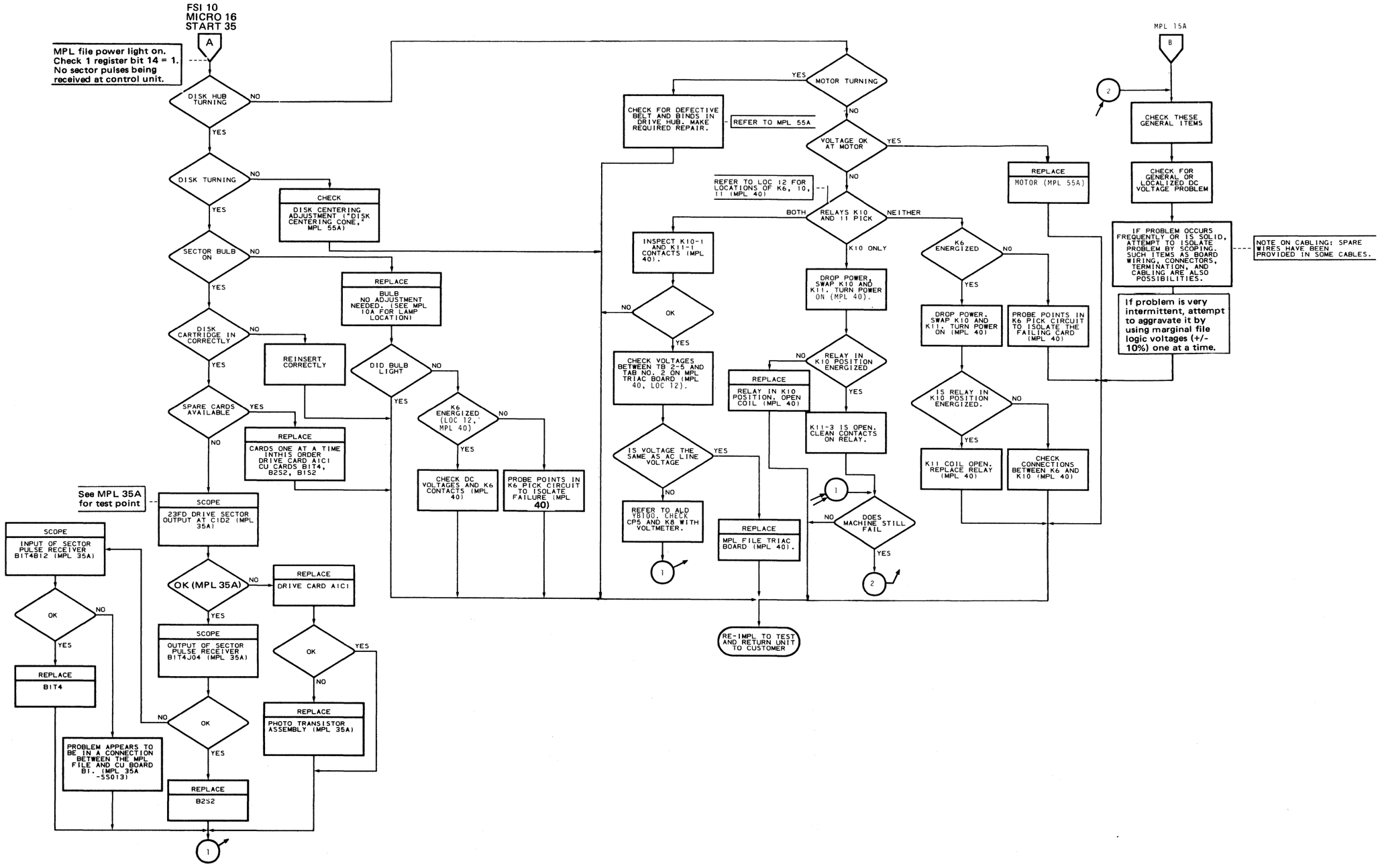
Check that head is electrically isolated from frame ground with connector removed from SLT card. Replace connector after measurement.

The electrical resistance between the head, plate, and the lightbulb ground must not exceed 1.0 ohms. Check for shorts between coil and arm assembly. The dc resistance of coil should be 70 ohms ± 10%. The dc resistance between coil and arm assembly should be greater than 1 megohm. Check head alignment (MPL 20B)

BG0700 Seq 2 of 2	2347105 Part Number

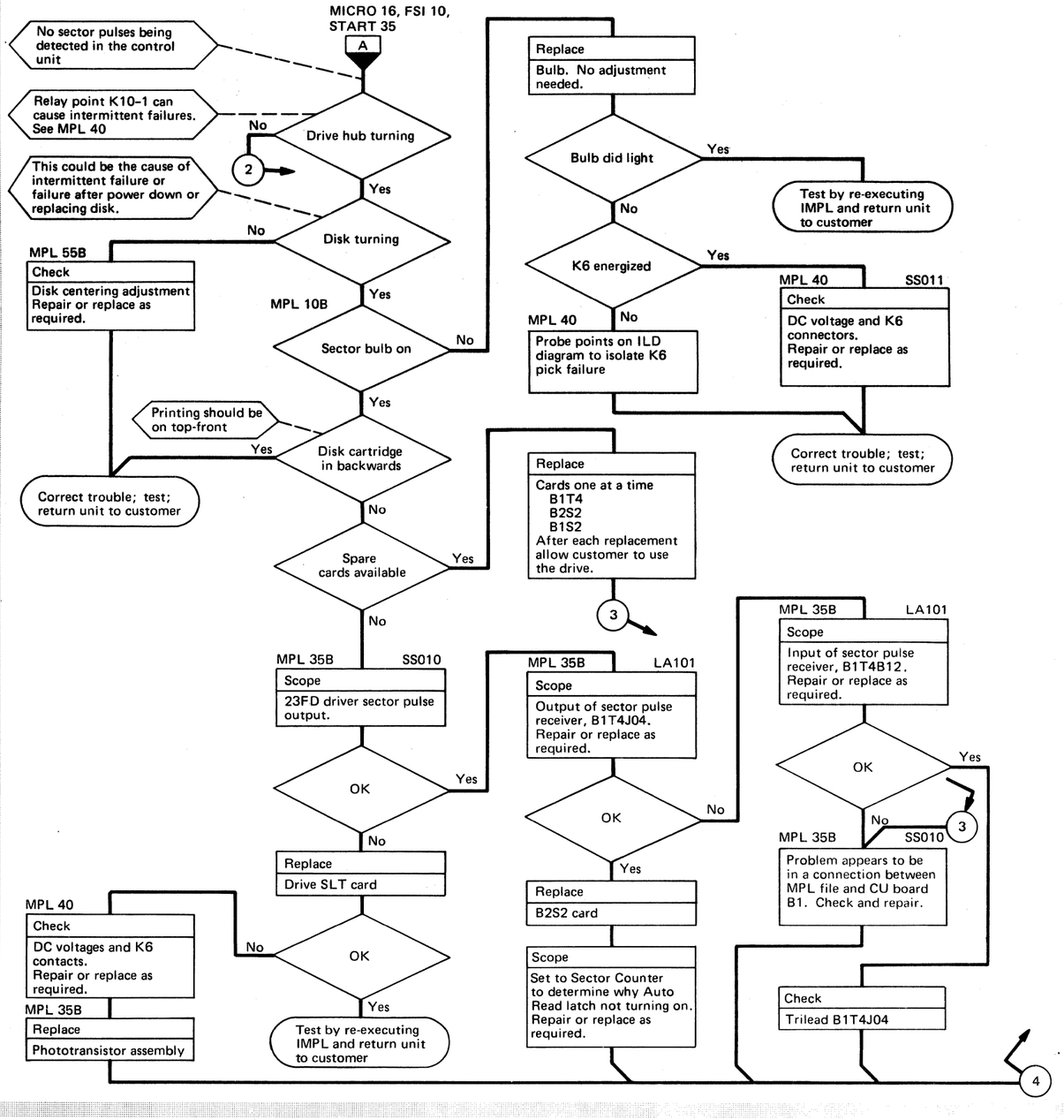
437402A	437405	437408	437414			
15 Mar 72	15 Aug 72	16 Oct 72	4 Jun 73			

MPL FILE NOT READY (Stage I only)

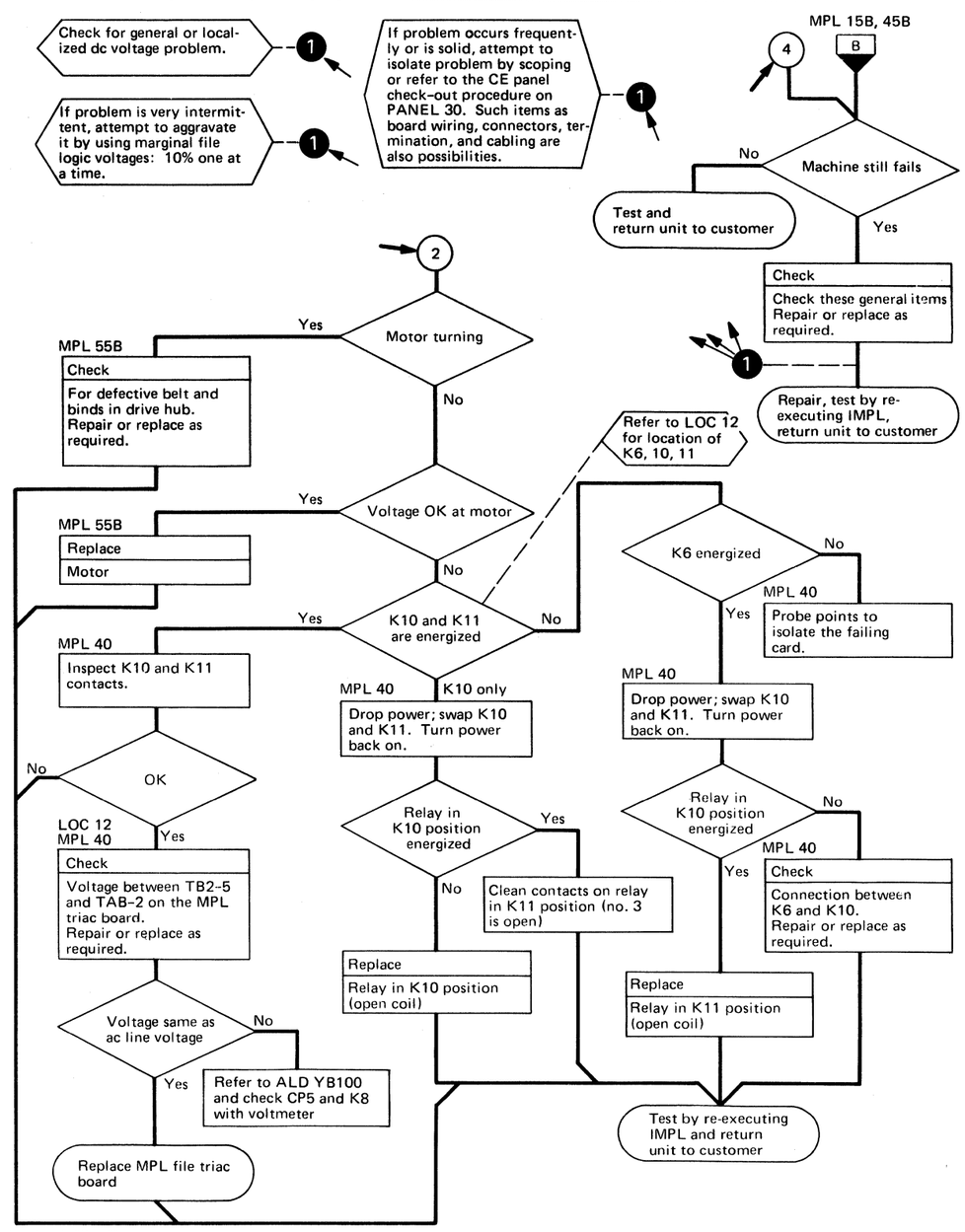


MPL FILE NOT READY (Stage II only)

SECTOR TOWER, SECTOR CIRCUITS



MOTOR AND MOTOR CONTROLS

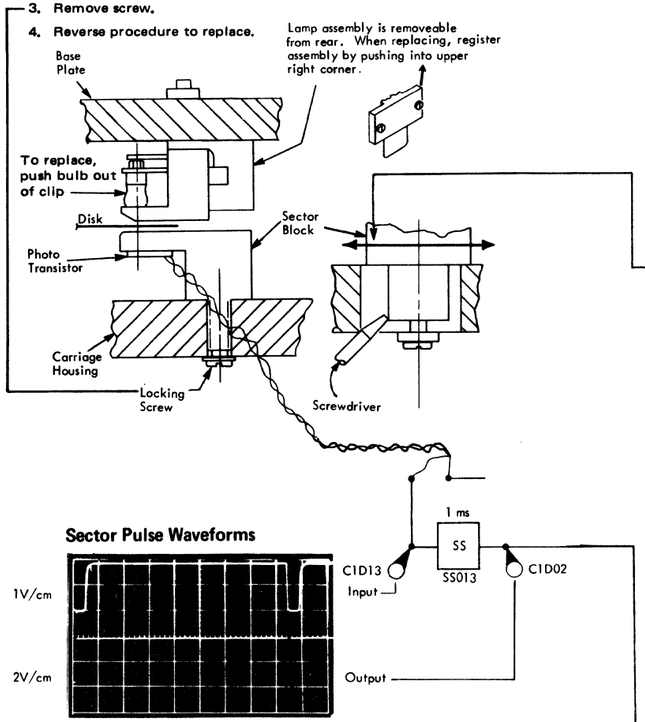


BG0800 Seq 2 of 2	2347106 Part Number	437402A 15 Mar 72	437403 21 Apr 72	437405 15 Aug 72	437408 16 Oct 72	437414 4 Jun 73		

SECTOR TOWER (STAGE I ONLY)

SECTOR TOWER ASSEMBLY
Removal/Replacement

1. Remove wires from EC1 a and b. Note color code so that wire can be replaced in the same position.
2. Remove housing (MPL 55A).
3. Remove screw.
4. Reverse procedure to replace.



Sector Pulse Waveforms

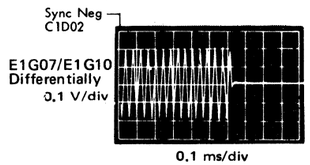
Check

Using CE disk, perform steps 2, 3, 4 and 11 of sector tower assembly adjustment procedure.

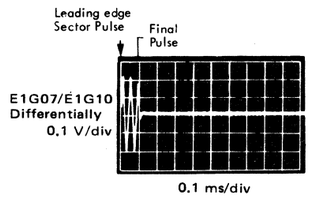
Adjustment

Adjustment of the sector block is done by circumferential alignment using prerecorded signal bursts of 1.2 ms duration on tracks 00 and 31.

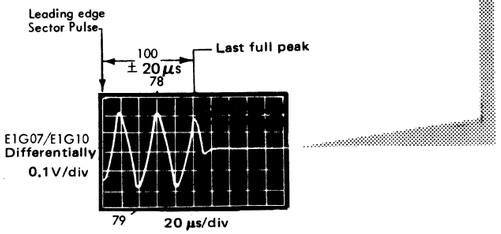
1. Remove cover. Clamp CE disk to drive hub.
2. Power up MPL file by setting Mode switch to CE Normal, pressing Reset, and pressing IMPL. Be sure that rotation of disk is maintained with cone shaft locked in position by CE lock screw (MPL 10A).
3. Access to track 00; use Seek/Load switch and leave head in loaded state.
4. Sync negative on leading edge of sector pulse (C1D02). Set time base to 10 ms/div.
5. Scope read amplifier data differentially (E1G07 and E1G10).
6. Adjust sector block assembly so 1.2-ms burst is in first division on scope screen. (Keep locking screw fairly tight and pry sector block with screwdriver.) Expand the trace to get:



7. Adjust sector block so final pulse of burst appears 100 ± 20 µs after leading edge of sector pulse.



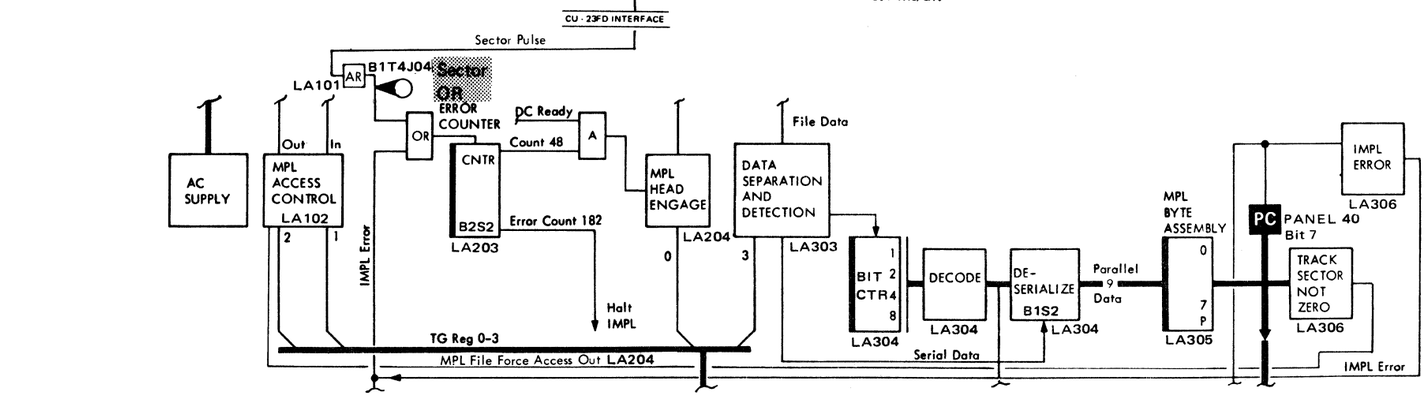
8. Expand time scale to 20 µs/div and make final adjustment:



9. Tighten sector block locking screw.
10. Check track 31 as in steps 5, 6, 7. If peak of last pulse is not within 100 ± 100 µs of the corresponding time on track 00, head alignment is incorrect.
11. Loosen CE lock screw 1 to 2 turns. Check that cone shaft moves freely in and out. Tighten locknut. Install cover.
12. Check track 0 for 100 ± 100 µs between leading edge of sector pulse and peak of last pulse.

READ HEAD OUTPUT CHECK

The voltage amplitude measured between peaks 78 and 79 must not be less than the number printed on the CE disk label. Replace head if specification is not met.



This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

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SECTOR TOWER ASSEMBLY

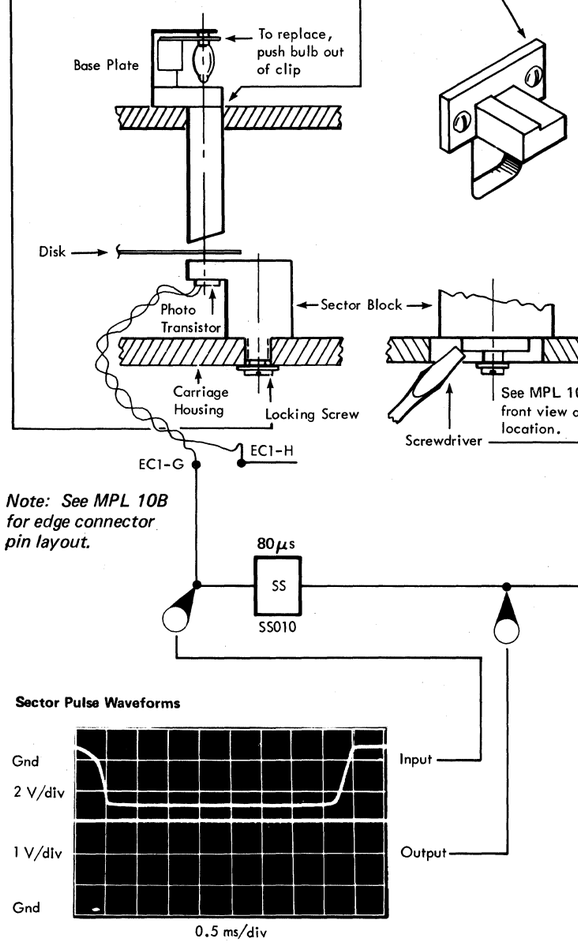
Removal

1. Turn off power. Remove disk and cover (MPL 55B).
2. Remove access housing assembly (MPL 55B).
3. Remove screw.

Replacement

1. Reverse removal procedure to replace parts.
2. Perform sector tower adjustments, (this page).

Lamp assembly is removable from rear. When replacing, register assembly by pushing into upper right corner.



Note: See MPL 10B for edge connector pin layout.

Sector Pulse Waveforms

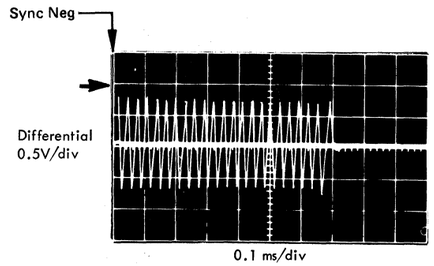
Check

Sector timing may be checked by performing steps 2, 3, 4, 5, and 13.

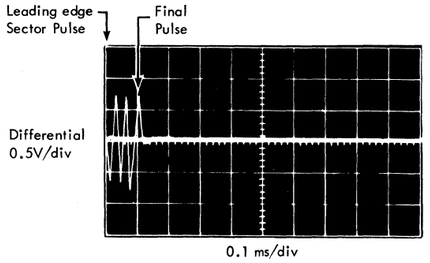
Adjustment

Adjustment of sector block is done by circumferential alignment using prerecorded signal bursts of 1.2 ms duration on tracks 00 and 31.

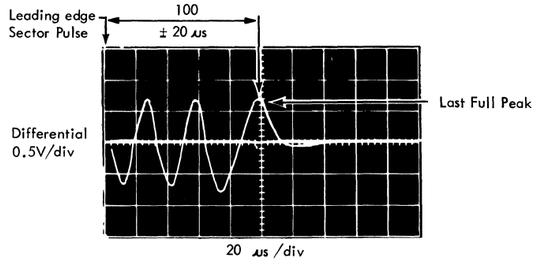
1. Remove disk and cover (MPL 55B).
2. Connect scope to read amp test points (MPL 25B), using X10 probes. Ground probes at black wire connection on light bulb.
3. Trigger Ext on sector pulse and set time base initially to 5 ms/div and to AC Add, one input inverted (differential), 50 mV/div.
4. Turn on power and access to track 00.
5. Insert CE disk.
6. Set Mode Switch to CE normal, press reset and IMPL, operate the Seek/Load switch to access head to track 0, leave head loaded.
7. Using a 1/4" socket, push center stud with sufficient force to rotate disk. Do not grasp access housing. (Have sector block assembly just loose enough to permit coarse adjustment.)
8. Adjust assembly so 1.2 ms burst is in first division on scope. (Keep locking screw fairly tight and pry sector block with screwdriver.) Expand the trace to get the following:



9. Adjust sector block so final pulse of burst appears 100 ± 20 μs after leading edge of sector pulse.

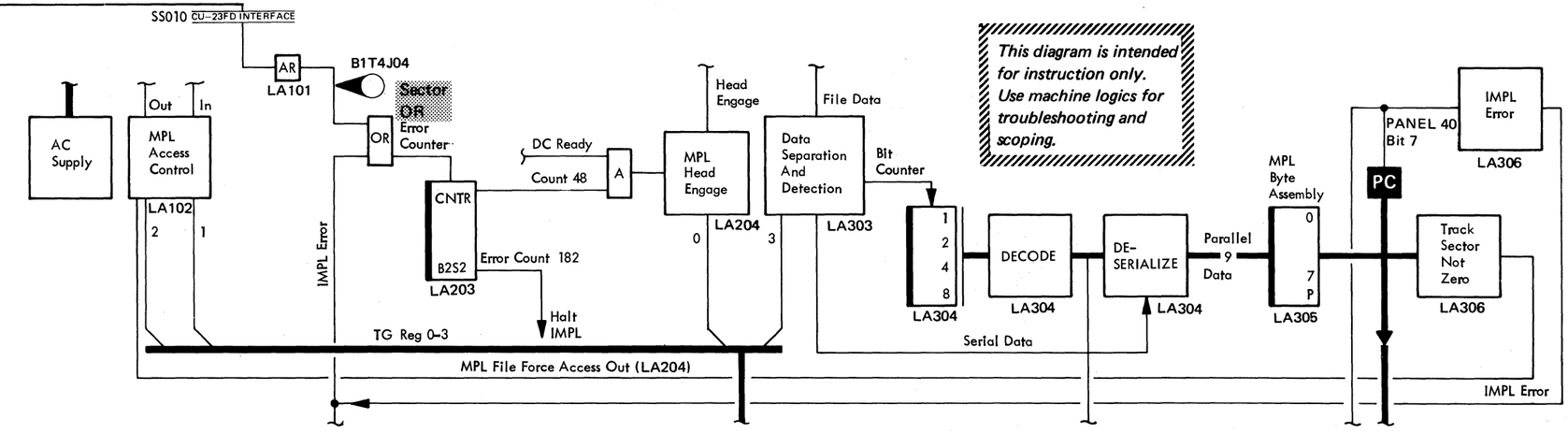


10. Final adjustments:



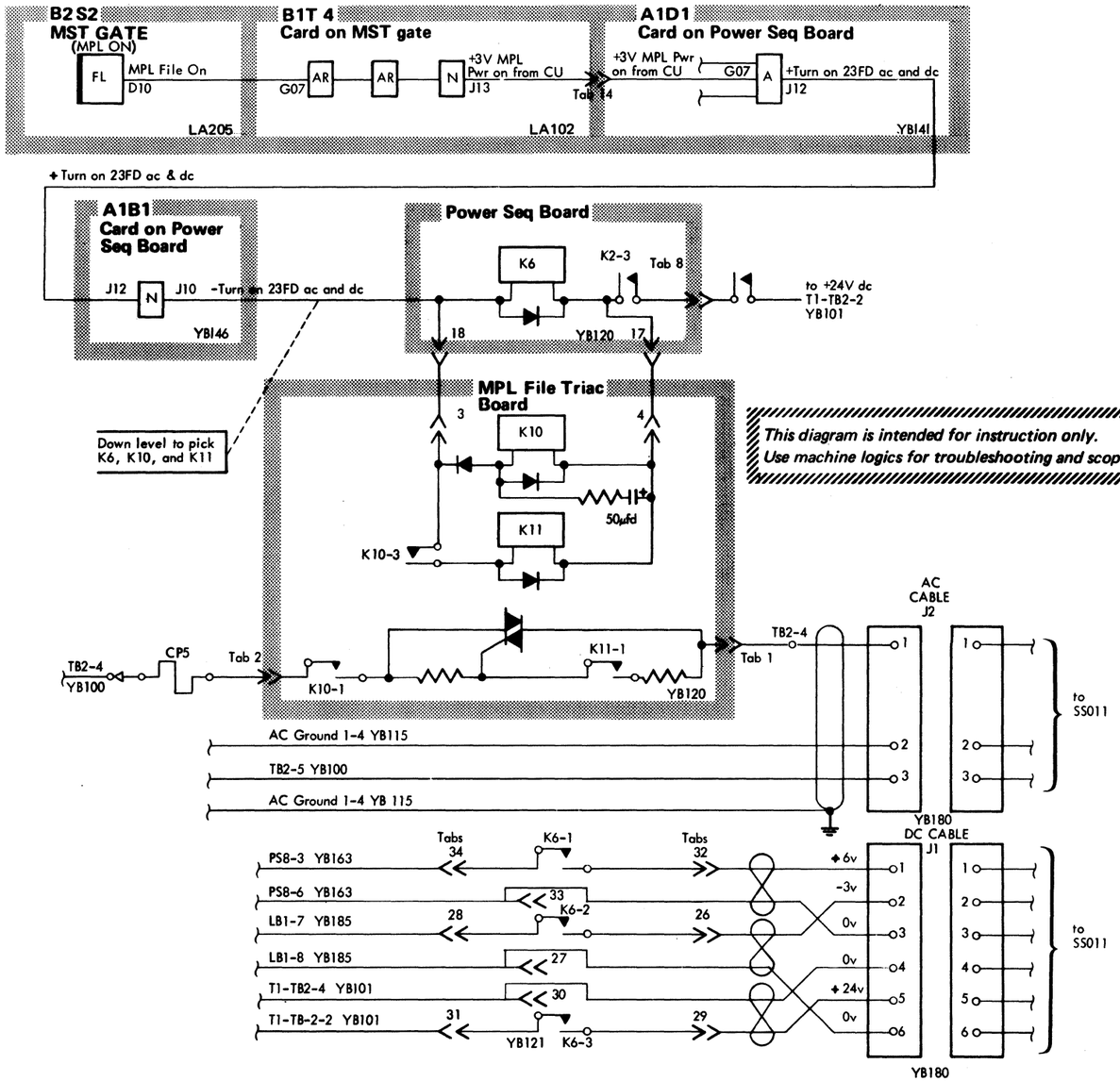
11. Tighten sector block locking screw. Force sector block into final adjustment.
12. Check track 31 as in steps 8 and 9. If peak of last pulse is not within 100 (+100, -80) μs of the corresponding time on track 00, head alignment is incorrect.
13. Install cover.
14. Check track 00 for 100 (+100, -80) μs between leading edge of sector pulse and peak of last pulse.

To move last peak to right, move sector block down.
To move last peak to left, move sector block up.



BG0900 Seq 2 of 2	2347107 Part Number	437402A 15 Mar 72	437405 15 Aug 72	437414 4 Jun 73				

MPL FILE AC–DC CONTROL CIRCUITS (STAGES I AND II)



MPL FILE SEEK CHECK (STAGE I ONLY)

FSI 10
MICRO 16
START 25
START 65
A

Did not read desired address or read an invalid address ('FF') after seek.

Put CU in CE Check Stop. Operate Seek/ Load Head switch.

SEEK CIRCUITS STEPPING CONTROL

Does access fail in both directions
Yes
No

Manually rotate stepping motor. Check for binds in stepping motor and lead screw

Bind in mechanism
Stepping Motor
Lead Screw

MPL 50A
Replace stepping motor

No Bind SS012
Check +24V between EC-2D and EC-3E

OK
No
MPL 40 SS010
Check connectors and K6

MPL 50A
Yes
Replace CU card B1T4

MPL 50A
Replace or repair lead screw

Normally, no voltage should be across the "in" or "out" stepping motor coils. If any voltage is present, suspect the power transistor and the diode across the coil.

Access moves both directions
Yes
No

Swap leads to stepping motor at EC2-B and EC2-A

Replace
B2F2
B1T4

Does access fail in same direction
Yes
No SS012

Restore wires at EC-2. Swap leads to transistors at EC3-A and EC3-C

MPL 50A
Restore wires at EC2. Replace stepping motor

Does access fail in same direction
Yes
No SS012

Restore wires at EC-3. Scope out/in commands at A1B1G03/J13

MPL 50A
Restore wires at EC3. Replace defective driver transistor
Out = T2
In = T1

OK
Yes
No

MPL 50A
Replace drive card A1B1

MPL 50A SS010
Replace CU card B1T4. Check cable connections

START 95
B

PRESSURE PAD LOADING

Inspect pressure pad load mechanism

OK
Yes
No

SS013
Scope head engage signal. Press reset, then IMPL. Drive A1B1G09

MPL 20A
Pressure pad load force check and actuator bail adjustment. Repair or replace head/arm assembly

+3V after 4 sec
No
Yes

LA102
Replace CU card B1T4 and check cables

SS013
Scope +24V at EC2-D. Press Reset then IMPL

OK
No
Yes

MPL 40 YB180
Check K6-3 and dc cables

SS013
Scope solenoid driver output. Should read +24V for 4 sec, then go to ground. Drive A1B1J12

+24V
No
Yes but did not go to ground
Yes then went to ground

MPL 20A
Open coil. Replace head/arm assembly

MPL 20A
Defective head/arm assembly. Replace assembly

SS013
Remove cone switch wire from EC3-G. Press Reset, then IMPL

Did head load
Yes
No

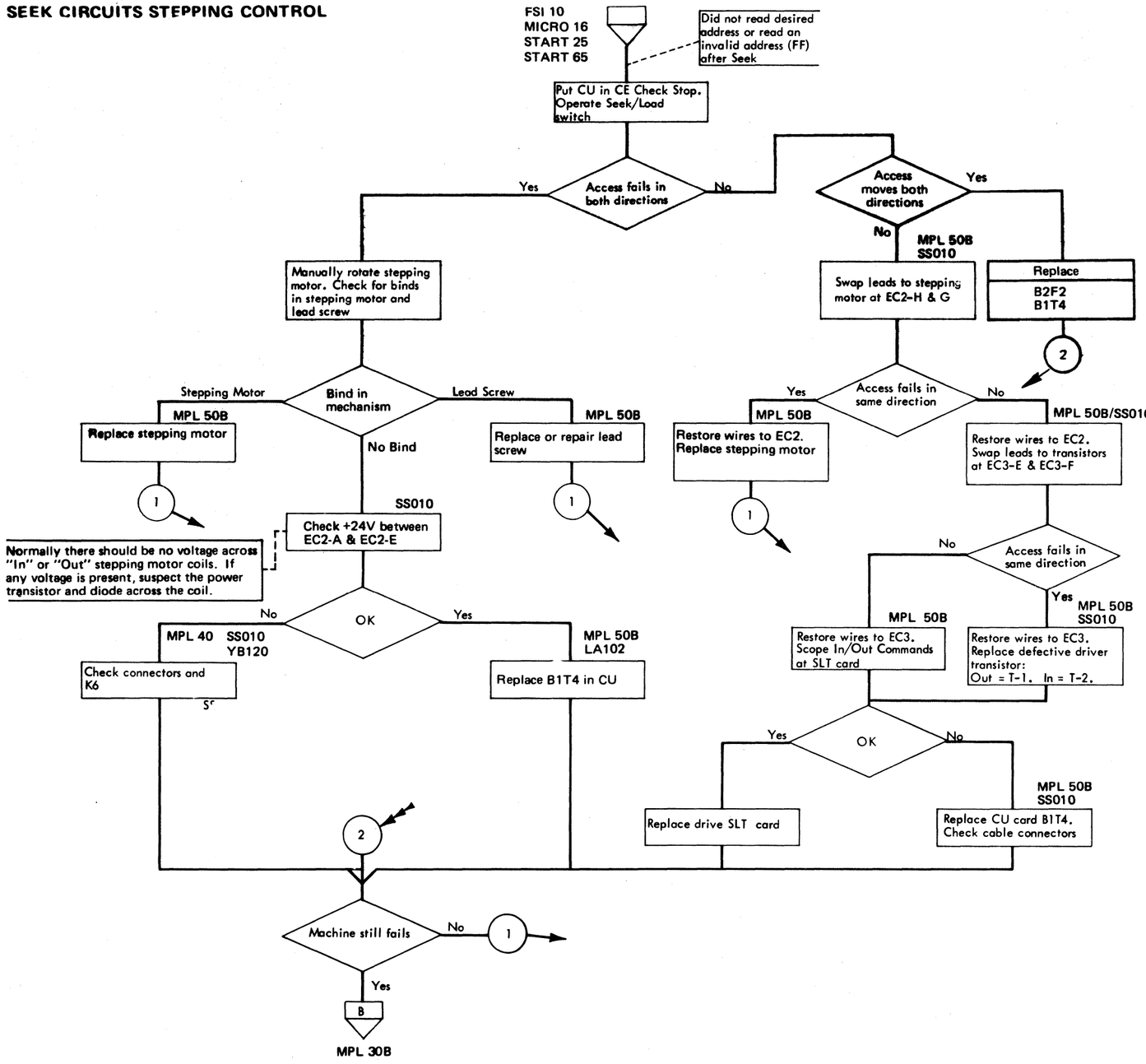
SS013
Adjust or replace cone switch

SS013
Replace SLT card A1B1

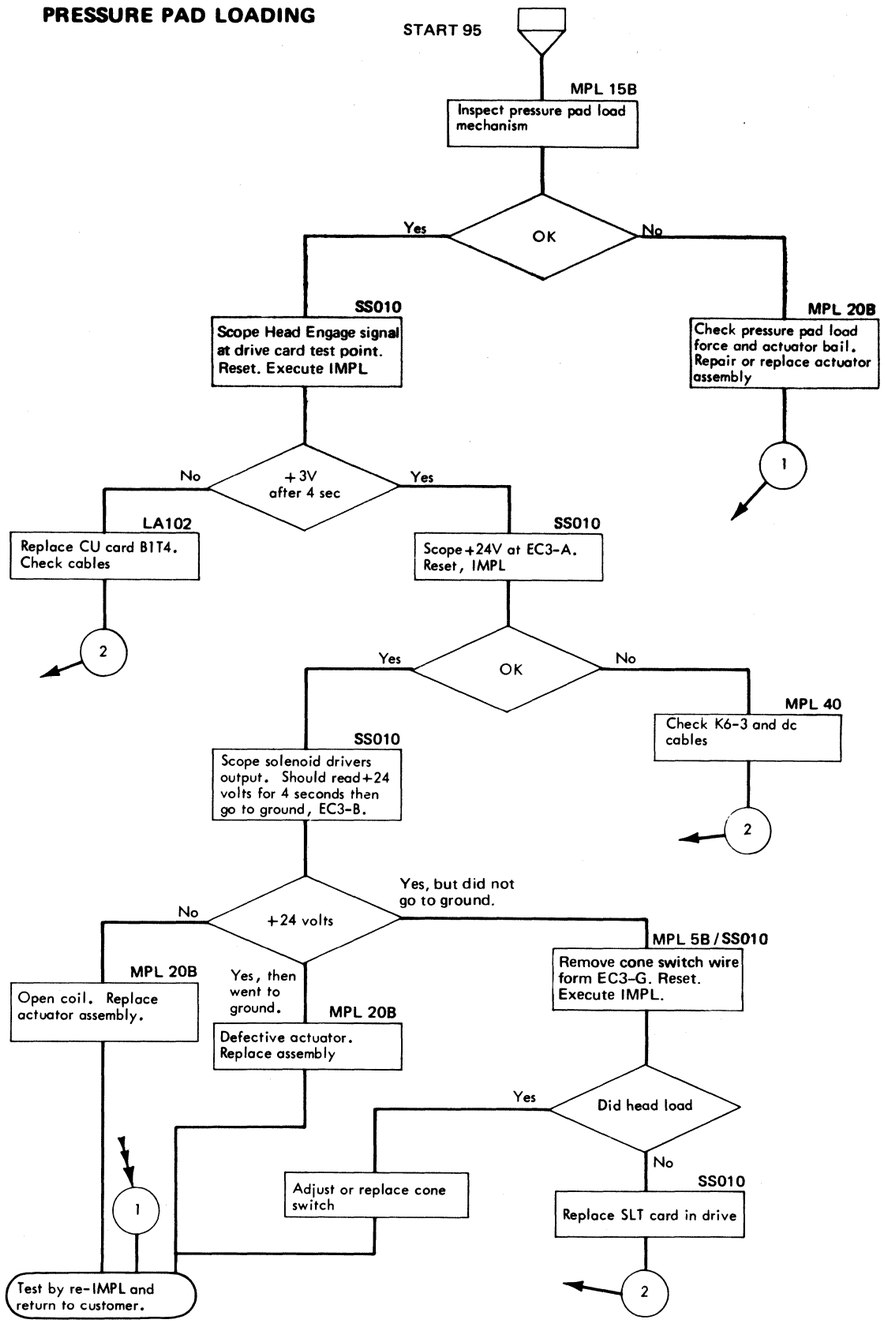
Test and return unit to customer

MPL FILE SEEK CHECK (STAGE II ONLY)

SEEK CIRCUITS STEPPING CONTROL



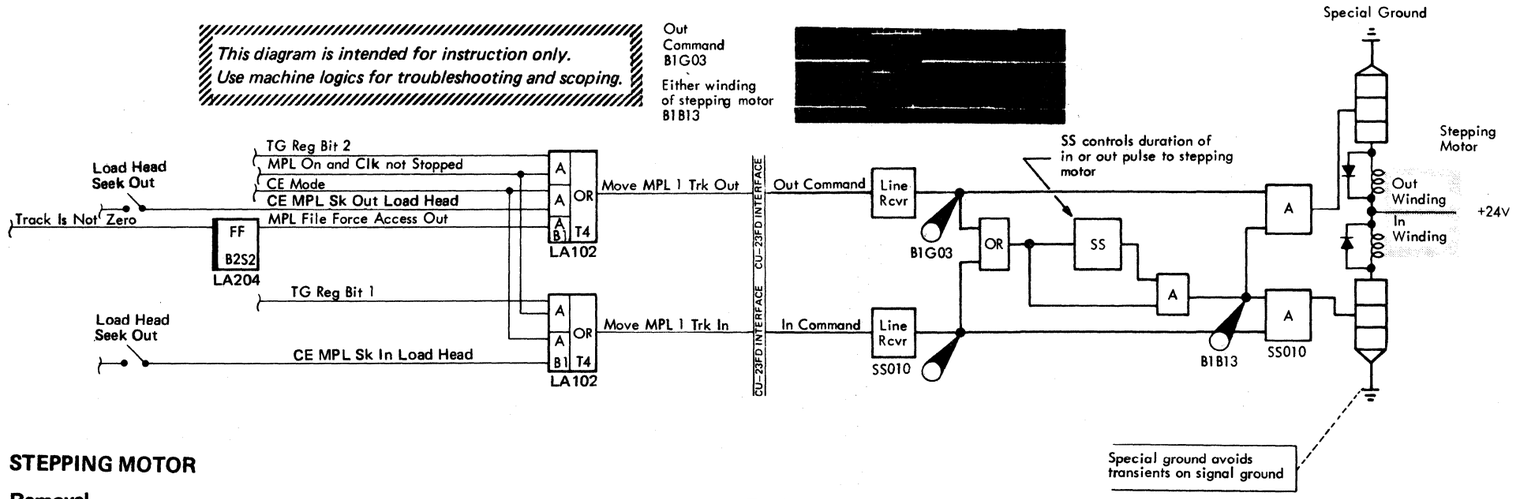
PRESSURE PAD LOADING



BG1100 Seq 2 of 2	2347109 Part No. (8)	437402A 15 Mar 72	437404 23 Jun 72	437405 15 Aug 72	437408 16 Oct 72	437414 4 Jun 73	447461 12 Mar 76	

STEPPING MOTOR, LEAD SCREW (STAGE I ONLY)

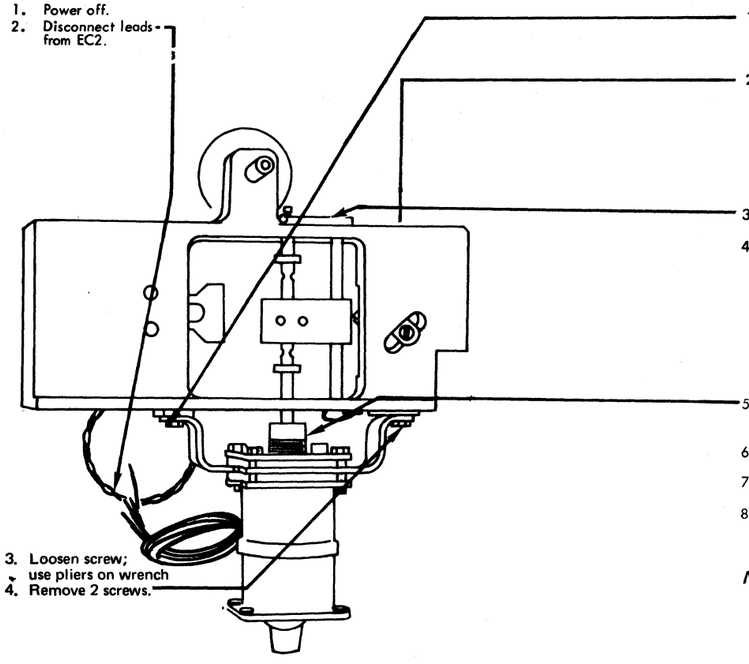
CONTROL CIRCUIT



STEPPING MOTOR

Removal

1. Power off.
2. Disconnect leads from EC2.
3. Loosen screw; use pliers on wrench
4. Remove 2 screws.

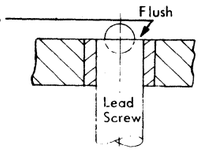


Replacement

1. Replace 2 screws; don't tighten. (Motor wires should be toward baseplate.)
2. Allow motor to hang free so that lead screw slides freely into coupling. Tighten 2 screws.

CAUTION:
Check that tab is in front of actuator bail. See Figure on MPL 20A.

3. Remove clamping assembly.
4. Move Lead screw to flush position.



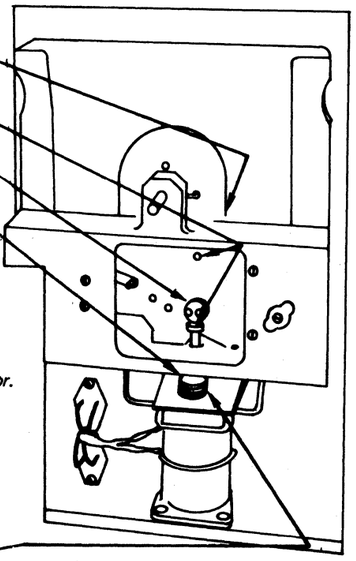
5. Firmly tighten set screws. Use pliers on wrench.
6. Replace clamping assembly.
7. Connect leads, power on.
8. Perform adjustments:
   - Read head radial position (MPL 20A).
   - Sector tower alignment (MPL 35A).

Note: If adjustment can't be made, return to step 4.

LEAD SCREW

Removal

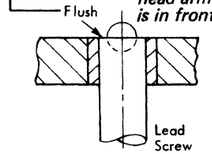
1. Power off.
2. Remove clamping assembly (2 screws).
3. Loosen screws.
4. Remove stylus (2 screws).
5. Loosen setscrew.
6. Remove lead screw from top.



Replacement

1. Hold lead screw as shown.

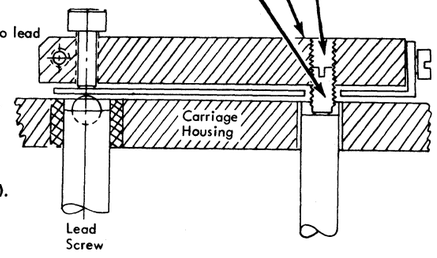
CAUTION:
Check that tab on head arm assembly is in front of actuator.



2. Firmly tighten setscrew. Use pliers on wrench.
3. Back out set screw a few turns.
4. Replace assembly.
5. Tighten setscrew.
6. Apply thin, uniform coat of Molykote G* (P/N357830) to lead screw and carriage stylus.
7. Replace stylus

CAUTION:
Stylus must be in lead screw helix groove.

8. Perform read head alignment (MPL 20A).
9. Check sector tower (MPL 35A).



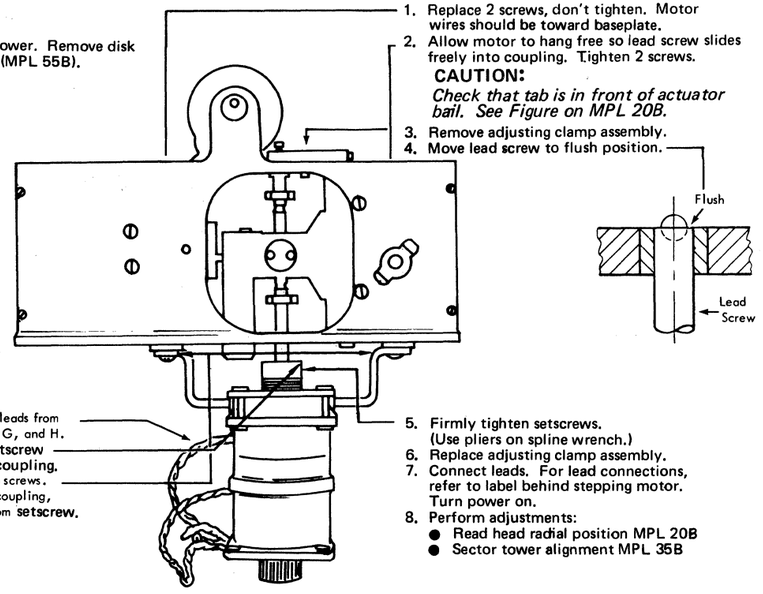
*Trademark of Dow-Corning Corp.

STEPPING MOTOR, LEAD SCREW (STAGE II ONLY)

STEPPING MOTOR

Removal

1. Turn off power. Remove disk and cover (MPL 55B).



Replacement

1. Replace 2 screws, don't tighten. Motor wires should be toward baseplate.
2. Allow motor to hang free so lead screw slides freely into coupling. Tighten 2 screws.

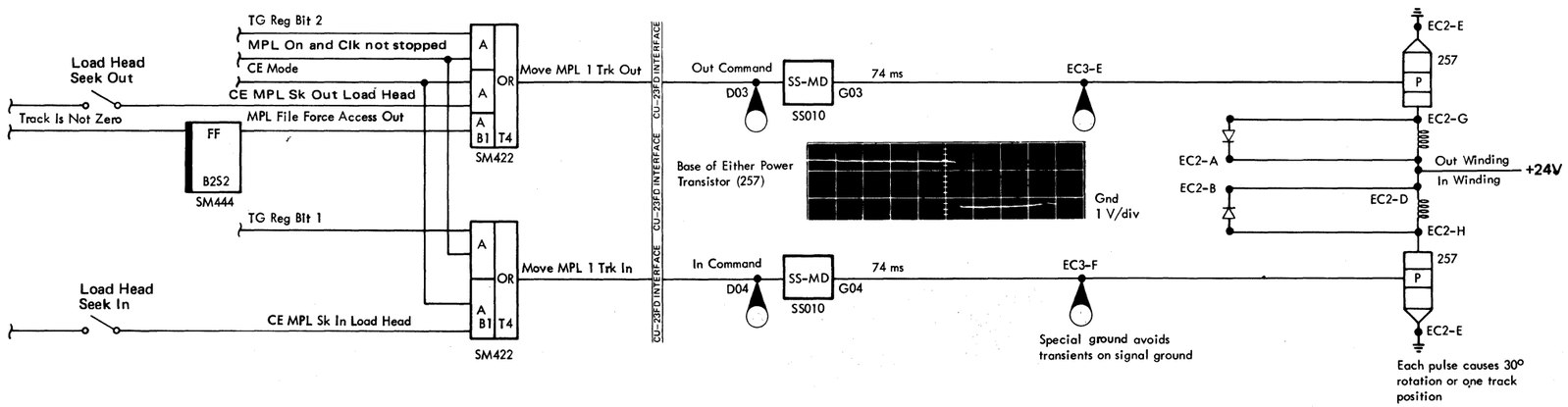
CAUTION:
Check that tab is in front of actuator bail. See Figure on MPL 20B.

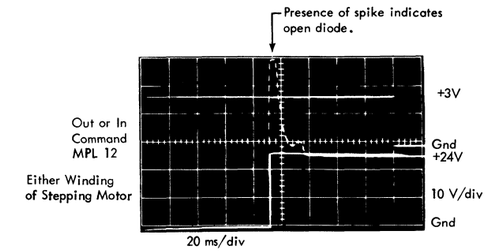
3. Remove adjusting clamp assembly.
4. Move lead screw to flush position.

5. Firmly tighten setscrews. (Use pliers on spline wrench.)
6. Replace adjusting clamp assembly.
7. Connect leads. For lead connections, refer to label behind stepping motor. Turn power on.
8. Perform adjustments:
   - Read head radial position MPL 20B
   - Sector tower alignment MPL 35B

CONTROL CIRCUIT

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.





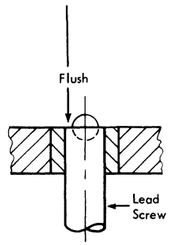
LEAD SCREW

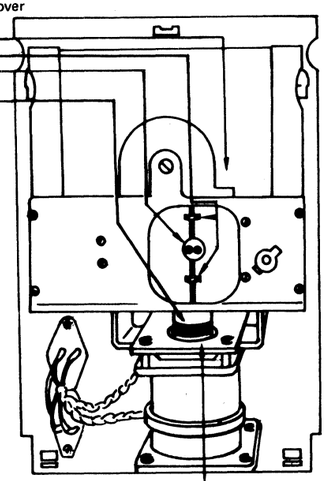
Removal

1. Turn off power. Remove disk and cover (MPL 55B).
2. Remove adjustment assembly (2 screws).
3. Loosen screws.
4. Remove stylus (2 screws).
5. Loosen screw.
6. Remove lead screw from top.

Replacement

1. Hold lead screw as shown.



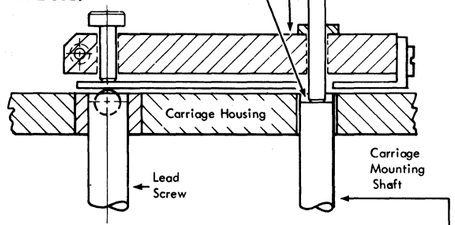


2. Firmly tighten set screw.
3. Loosen lock nut.
4. Back out screw a few turns.
5. Replace adjustment assembly.
6. Turn screw until it just contacts the carriage mounting shaft and tighten lock nut.
7. Apply thin uniform coat of Molykote G * (P/N 357830) to lead screw and carriage stylus.
8. Replace stylus. Check that tab on head arm assembly is in front of actuator.

CAUTION:
Stylus must be in lead screw helix groove. Stylus preload prevents full seating until screws are tight.

9. Perform read head alignment MPL 20B.
10. Check sector tower MPL 35B.

* Trademark of Dow-Corning Corp.



HEAD CARRIAGE

Removal

1. Power off. Remove disk and cover, MPL 55B.
2. Remove head assembly, MPL 20B.
3. Remove lead screw (this page).
4. Remove carriage mounting shaft through the top of the housing.

Replacement

1. Reverse removal procedure to replace parts. Perform all necessary adjustments.

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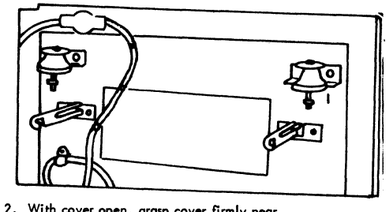
FRAME, DISK DRIVE (STAGE I ONLY)

FRAME AND ACCESS HOUSING

Cover Removal

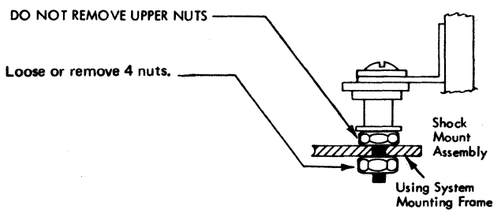
1. Loosen 4 screws and slide clips to release cover.



2. With cover open, grasp cover firmly near bottom, press in,and pull outward.

CAUTION:
Opening cover too wide will damage hinges. Do not allow cover to drop open.

Removal of 23FD From System Frame



Access Housing Assembly Removal/Replacement

1. Disconnect wires from connecting blocks leading to sector tower, head load solenoid, microswitch, and stepping motor.
2. Remove connector from SLT board E1 J08, J11, and J12 (read head wires).
3. Remove 2 screws holding access housing assembly to base plate. Note the two locating pins. If the housing or the drive hub spindle must be replaced, follow the procedures given on this page.

DISK DRIVE

Drive Motor and Pulley Removal/Replacement

1. Turn off all power to machine.
2. Unplug connector of cable leading to drive motor.
3. Remove belt (next paragraph).
4. Remove two screws holding the drive motor to the base plate.
5. To remove pulley loosen clamp screw.
6. To install pulley, place on motor shaft so that outer end of pulley is 63/64" (24,76 mm) from motor plate. To adjust belt tracking, pulley can be moved in or out one-half of 1/64".
7. Tighten clamping screw.

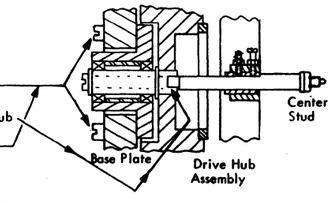
Drive Belt Removal/Replacement

1. Turn off all power to machine.
2. Remove disk from machine.
3. Remove disk guide.
4. Slip belt off the drive hub. Don't snag the sector tower assembly, or the head/arm assembly.

Reverse procedure to replace belt. Check that belt is around shaft of motor.

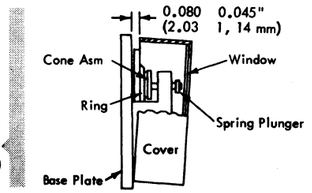
Alignment of Drive Hub Spindle Housing With Clamping Cone Shaft

1. Remove access housing assembly (this page).
2. Remove cone assembly from access housing.
3. Remove drive belt (this page).
4. Replace access housing.
5. Loosen two screws.
6. Insert center stub through the housing into drive hub center shaft. This aligns drive hub center to the center shaft. Tighten two screws. Check that alignment is correct by removing shaft and reinserting.
7. Remove access housing, replace cone assembly and drive belt.
8. Replace access housing.



Disk Centering Cone Adjustment

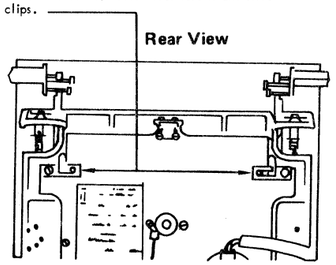
1. Remove cover (this page).
2. Position the center cone assembly so that the flange lightly contacts the rubber ring on the drive hub. Tighten CE lock screw.
3. Install the cover.
4. Adjust the spring plunger to contact the inside surface of the window when the upper rear surface of the cover is 0.080 0.045" (2,03 1, 14 mm) from the base plate.



FRAME, DISK DRIVE (STAGE II ONLY)

COVER REMOVAL/REPLACEMENT

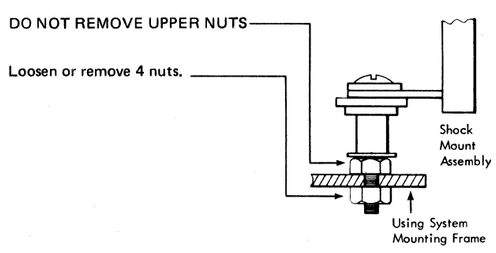
1. To release cover, loosen four screws and slide clips.



CAUTION
Opening the cover too wide will damage the hinges. Do not allow cover to drop open.

2. With cover open, remove by placing pencil near hinge and closing cover.
3. To replace cover, snap hinges at the bottom.

REMOVAL OF 23FD FROM SYSTEM FRAME



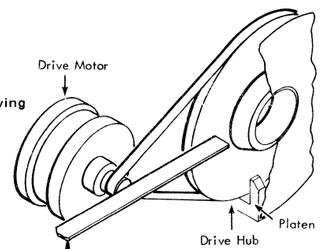
ACCESS HOUSING ASSEMBLY REMOVAL/REPLACEMENT

1. All power off. Remove disk and cover (this page).
2. Disconnect and mark wires from:
   Sector tower - EC1-G and H
   Pressure pad relay coil - EC3- A and B
   Pressure pad interlock Switch - EC3-G and H
   Stepping motor: Out coil - EC2-A and G
   In coil - EC2-D and H
   Frame ground - Ring terminal on motor
3. Remove head connector from SLT file control card (MPL 25B). Free it from cable clamp.
4. Remove four outside screws, holding access housing assembly to baseplate. Work access housing assembly off two locating pins. If the housing or the drive hub spindle must be replaced, follow the procedure given on this page.
5. Reverse procedure to replace parts.

DRIVE MOTOR AND PULLEY

Removal

1. Turn power off. Remove disk and cover (this page).
2. Unplug drive motor cable connector.
3. Remove wires from EC1-E and F (light bulb), and EC1-E (drive Hub ground). Note location of black and yellow wires.
4. Remove motor mounting plate assembly (MPL 10B) by removing seven screws on outer perimeter. Grasp motor firmly and work assembly off two locating pins.
5. Remove platen and slip belt off the drive hub.
6. Remove four nuts (50 Hz motors have four screws) and the washers that hold the drive motor to the mounting plate.
7. To remove pulley, loosen clamp screw.



Replacement

1. Place pulley on motor shaft so that outer end of pulley is flush with the drive hub. Use straightedge to align pulley with drive hub. Tighten clamping screw.
2. Reverse removal procedure to replace belt, motor and motor mounting plate assembly. See MPL 10B for ac cable orientation of drive motor.

DRIVE BELT REMOVAL/REPLACEMENT

To remove belt, perform steps 1 through 5 of Drive Motor and Pulley Removal. Reverse procedure to replace belt and motor mounting assembly plate.

DRIVE HUB

Removal

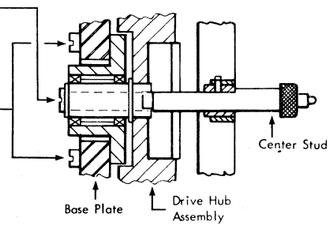
1. Perform steps 1 through 5 of Drive Motor and Pulley Removal.
2. Remove screws.

Replacement

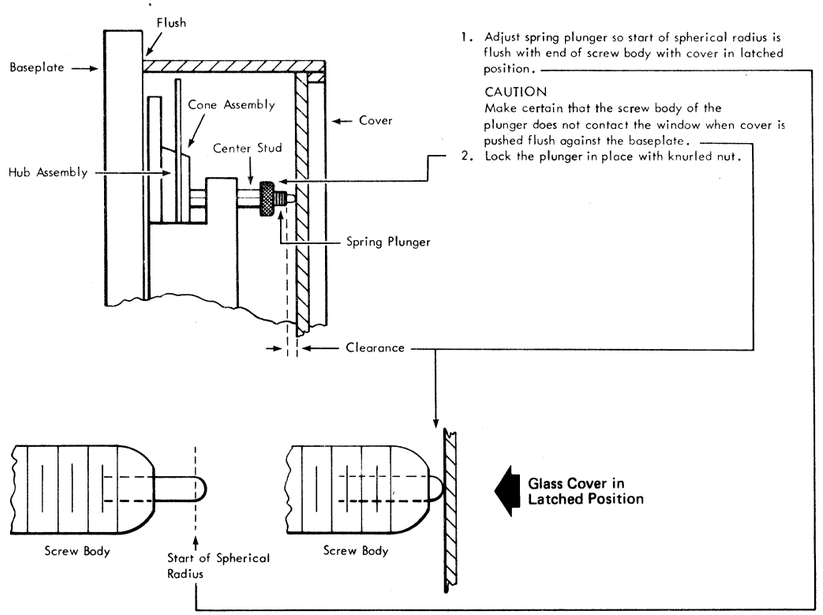
1. Reverse removal procedure to replace drive hub and motor mounting plate assembly.
2. Perform drive hub alignment.

Alignment

1. Turn power off. Remove disk and cover (this page).
2. Remove belt and drive hub.
3. Remove screw.
4. Insert bristol wrench through the hole opened in step 3 and remove screw from cone assembly.
   CAUTION
   Do not drop screw
5. Remove center stud and cone.
6. Loosen two screws.
7. Remove spring from center stud and insert center stud through the housing into the drive hub center shaft. This aligns drive hub center to the center shaft. Tighten two screws. Alignment is correct when center stud slides freely in and out of the drive hub center.
8. Replace spring on center stud and replace cone and screws.
9. Check head alignment (MPL 20B).



CENTER STUD TO COVER ADJUSTMENT



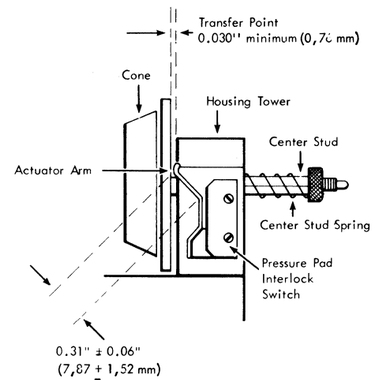
1. Adjust spring plunger so start of spherical radius is flush with end of screw body with cover in latched position.

CAUTION
Make certain that the screw body of the plunger does not contact the window when cover is pushed flush against the baseplate.

2. Lock the plunger in place with knurled nut.

PRESSURE PAD INTERLOCK SWITCH REMOVAL/REPLACEMENT

1. Turn power off. Remove disk and cover (this page).
2. Remove cable clamp under access housing and disconnect the two wires from EC3-G and H.
3. Remove two screws holding the microswitch to the housing assembly.
4. Replace microswitch with new one.
5. After replacing microswitch, form actuator arm as shown so that:
   a. Switch transfer occurs when the cone is a minimum of 0.030" (0,76 mm) from the housing tower.
   b. Cone is free to contact the housing tower when actuated only by the center stud spring.
6. Replace wiring and reconnect to EC3-G and H.
7. With power on and head engage input line up, operate center stud manually. Pressure pad actuator should operate.



CONTENTS

MPL ATTACHMENT

MICROPROGRAM LOAD (MPL) OPERATION

- MPL file serves as microprogram residence file.
- MPL operation transfers microprogram from file to control storage.
- Initial loading is hardware controlled. After initial loading, control is switched to the microprogram.

The functional microprogram must be loaded into control storage before the control unit (CU) can operate the facility. The MPL operation is initiated automatically by the Power-On reset; and is performed each time power is restored to the control unit. The MPL file serves as the microprogram residence file to store the functional microprogram and a variety of diagnostic routines. The MPL operation requires hardware controlled loading of 64 microprogram words containing a loader program. After the 64 words are loaded, control of the loading operation is switched to the microprogram, which continues loading the rest of the functional microprogram.

SYSTEM

- System is reset.
- Starts power up sequence.

POWER SEQUENCE INTERFACE

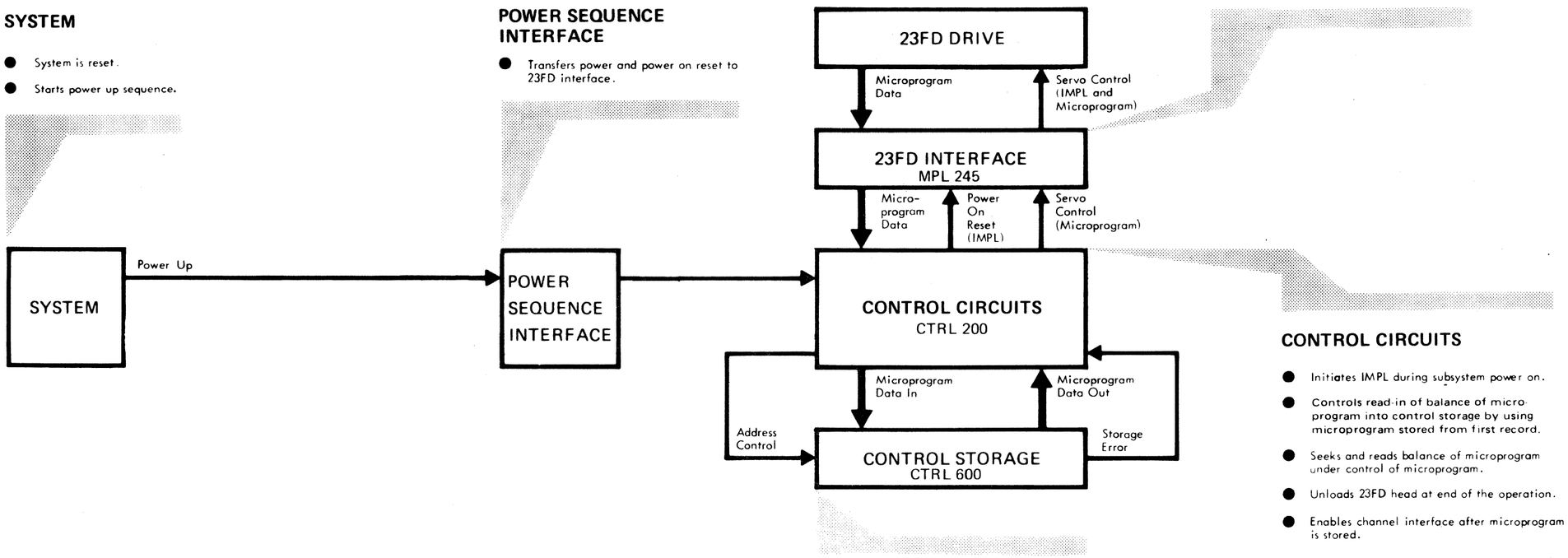
- Transfers power and power on reset to 23FD interface.

23FD DRIVE (MPL FILE)

- The microprogram is stored on disk.
- Provides drive to the disk.
- Provides method of positioning head over one of 32 tracks.
- Reads data to the interface.

23FD INTERFACE

- Power on reset starts intial microprogram load (IMPL) operation.
- Starts 23FD drive.
- Controls movement of 23FD head to track zero.
- Reads first sector into the control storage.
- Forces start of microprogram operation at beginning of record read in.
- Changes serial - by - bit 23FD data to serial - by - byte data.



CONTROL CIRCUITS

- Initiates IMPL during subsystem power on.
- Controls read-in of balance of micro-program into control storage by using microprogram stored from first record.
- Seeks and reads balance of microprogram under control of microprogram.
- Unloads 23FD head at end of the operation.
- Enables channel interface after microprogram is stored.

CONTROL STORAGE

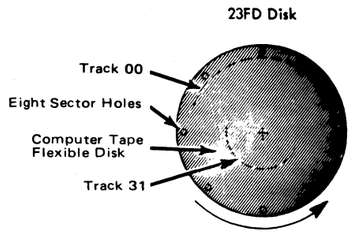
- Checks all data transferred for errors.

23FD ATTACHMENT INTRODUCTION

The 23FD Disk Drive is used on the Facility to store the Functional microprogram and microdiagnostics.

DISK FORMAT

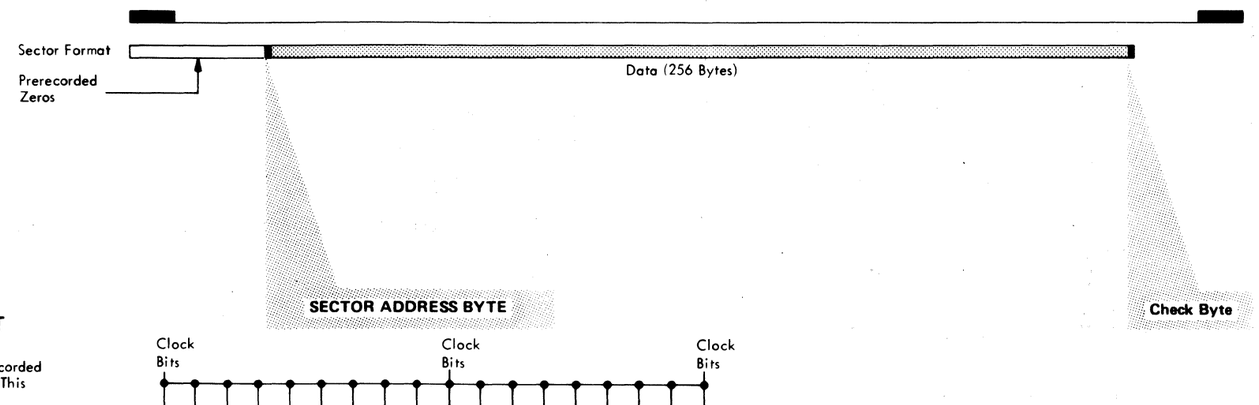
32 eight-sector tracks.



SECTOR FORMAT

Each Sector contains:

- One sector address byte
- 256 data bytes
- One check byte

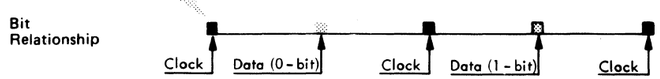


SECTOR ADDRESS BYTE FORMAT

Each byte has nine bits, 0-7 and parity. Data is recorded so that the first non-clock bit read is the sync bit. This bit signals that the sector address byte follows.

DATA SEPARATION

MPL information consists of a double frequency signal containing both clock and data pulses. The data separation counter strobes between clock pulses; the presence of a data pulse indicates a 1; the absence of a data pulse indicates a 0. As the data bits are read, the bit counter gates the data pulses into the byte assembler.



23FD/CONTROL STORAGE ADDRESS RELATIONSHIP

The microprogram on the 23FD is moved to the control storage each time power is sequenced on. The following table shows the 23FD to control storage address relationship.

Track	Sector							
	0	1	2	3	4	5	6	7
0	0000	0100	0200	0300	0400	0500	0600	0700
1	0800	0900	0A00	0B00	0C00	0D00	0E00	0F00
2	1000	1100	1200	1300	1400	1500	1600	1700
3	1800	1900	1A00	1B00	1C00	1D00	1E00	1F00
4	2000	2100	2200	2300	2400	2500	2600	2700
5	2800	2900	2A00	2B00	2C00	2D00	2E00	2F00
6	3000	3100	3200	3300	3400	3500	3600	3700
7	3800	3900	3A00	3B00	3C00	3D00	3E00	3F00
8-11	Reserved for expansion							

0000 *= the initial microprogram load program location in the control storage. The microprogram loading is completed by overlaying the load program in address '0000' with data residing at track 16 sector 0 so that a subsequent system reset will not cause another microprogram load.*

INITIAL PROGRAM LOAD

The CU microprogram is loaded into the control storage from the 23FD each time power is sequenced on because information stored in the control storage is lost when power is turned off. This microprogram load is both hardware controlled and microprogram controlled. The microinstructions on sector 0, track 0 of the 23FD are read into the control storage under hardware control. These microinstructions are than used to control the loading of the rest of the control storage from the 23FD.

MICRODIAGNOSTICS

CU microdiagnostics reside on the 23FD from track 12 through track 31, with the exception of track 16, sectors 0 and 1. These sectors are loaded in pairs into control storage locations 0400-05FF.

23FD ATTACHMENT CONCEPTS

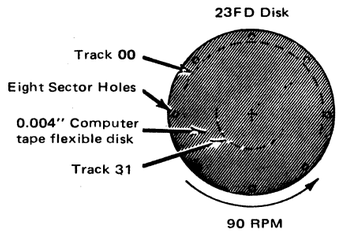
Concepts

- Locate the beginning of data on a 23FD sector and read the serially recorded data.
- Place the data into a register, bit by bit, until the register is full (deserialize).
- Group the assembled bytes into words and gate each assembled word into the proper storage location.

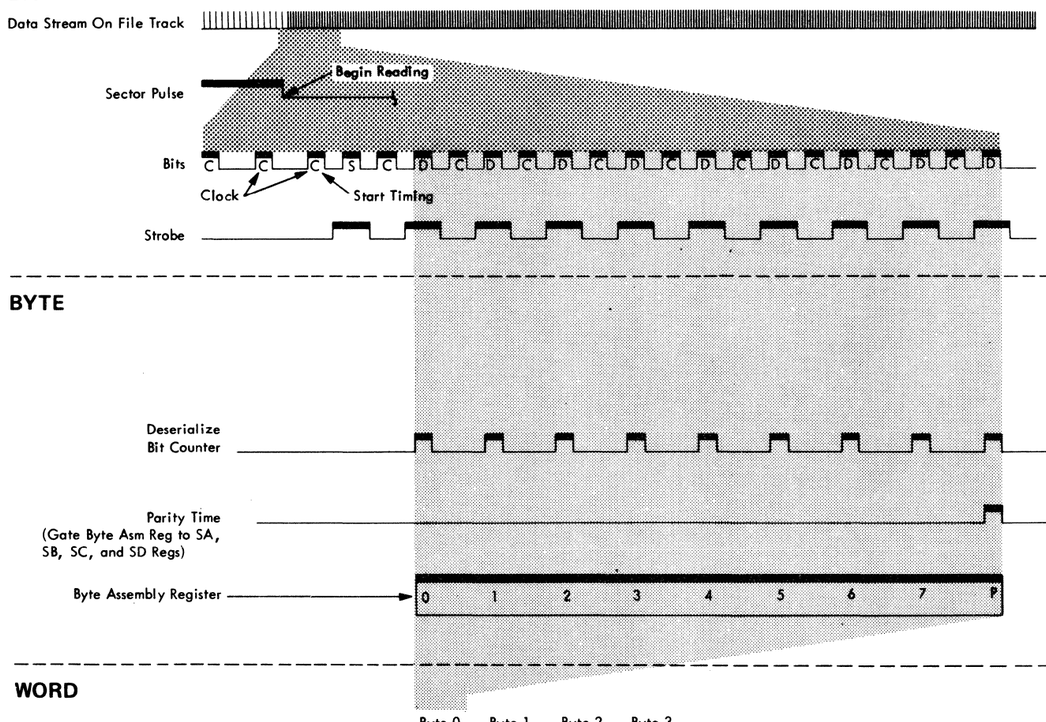
Note: Timing charts are for reference only.

TRACK DATA ORIENTATION

The 23FD begins reading at the end of sector pulse time. The first pulse read from the disk is a clock pulse which starts a timing sequence. The first data pulse available at strobe time is a sync pulse.



BIT



BYTE ASSEMBLY

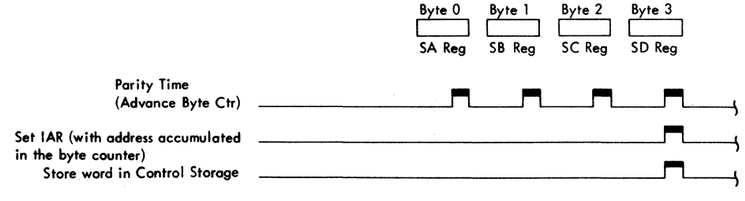
At each strobe time after the sync pulse, the presence or absence of a data pulse is gated into the byte assembly register as a one or zero. The bit counter controls the gating.

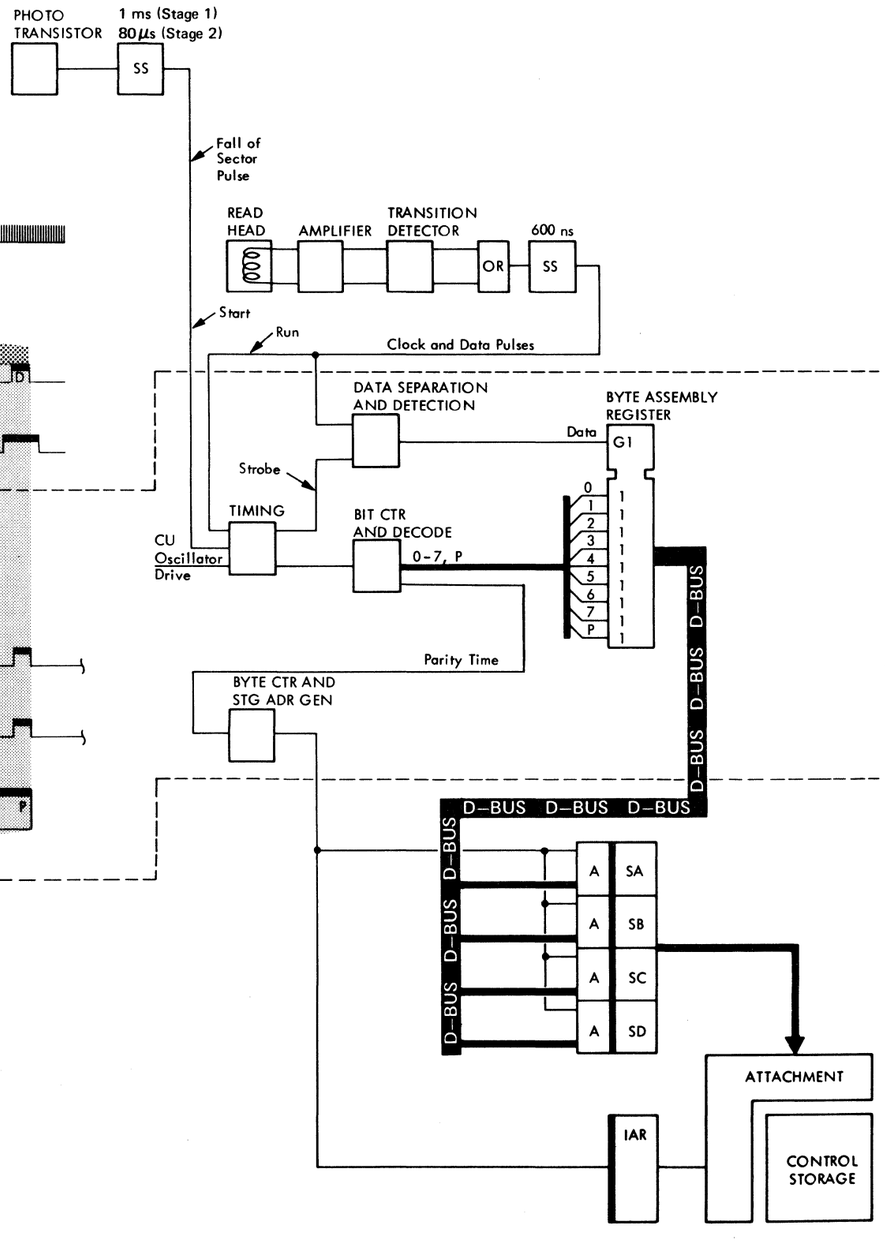
BYTE

WORD AND PARITY ASSEMBLY

At parity time, the byte assembly register is full. The byte is transferred to the proper register (SA, SB, SC, or SD register). When a full word is deserialized, it is gated into the control storage.

WORD

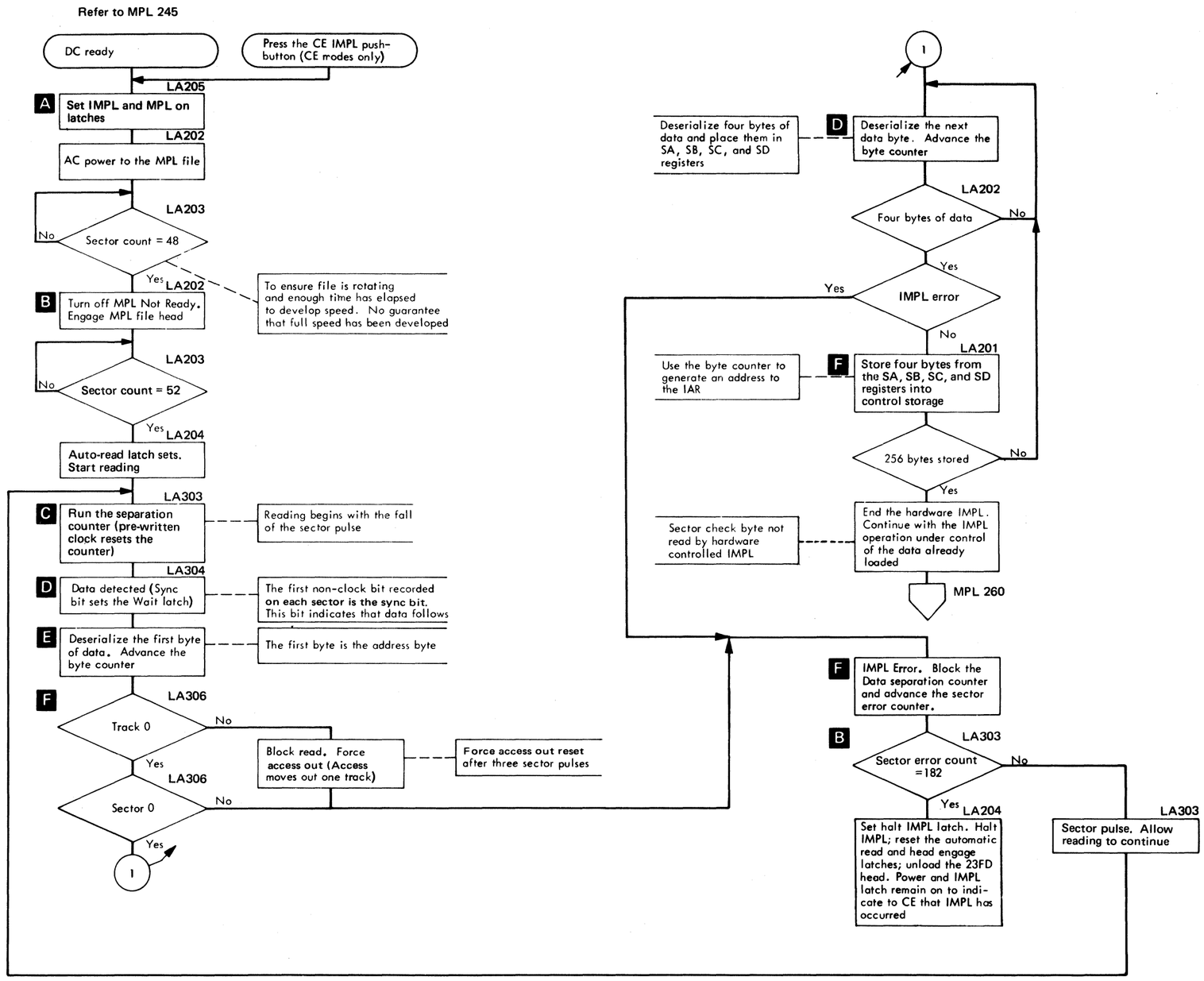




HARDWARE CONTROLLED IMPL (Part 1 of 2)

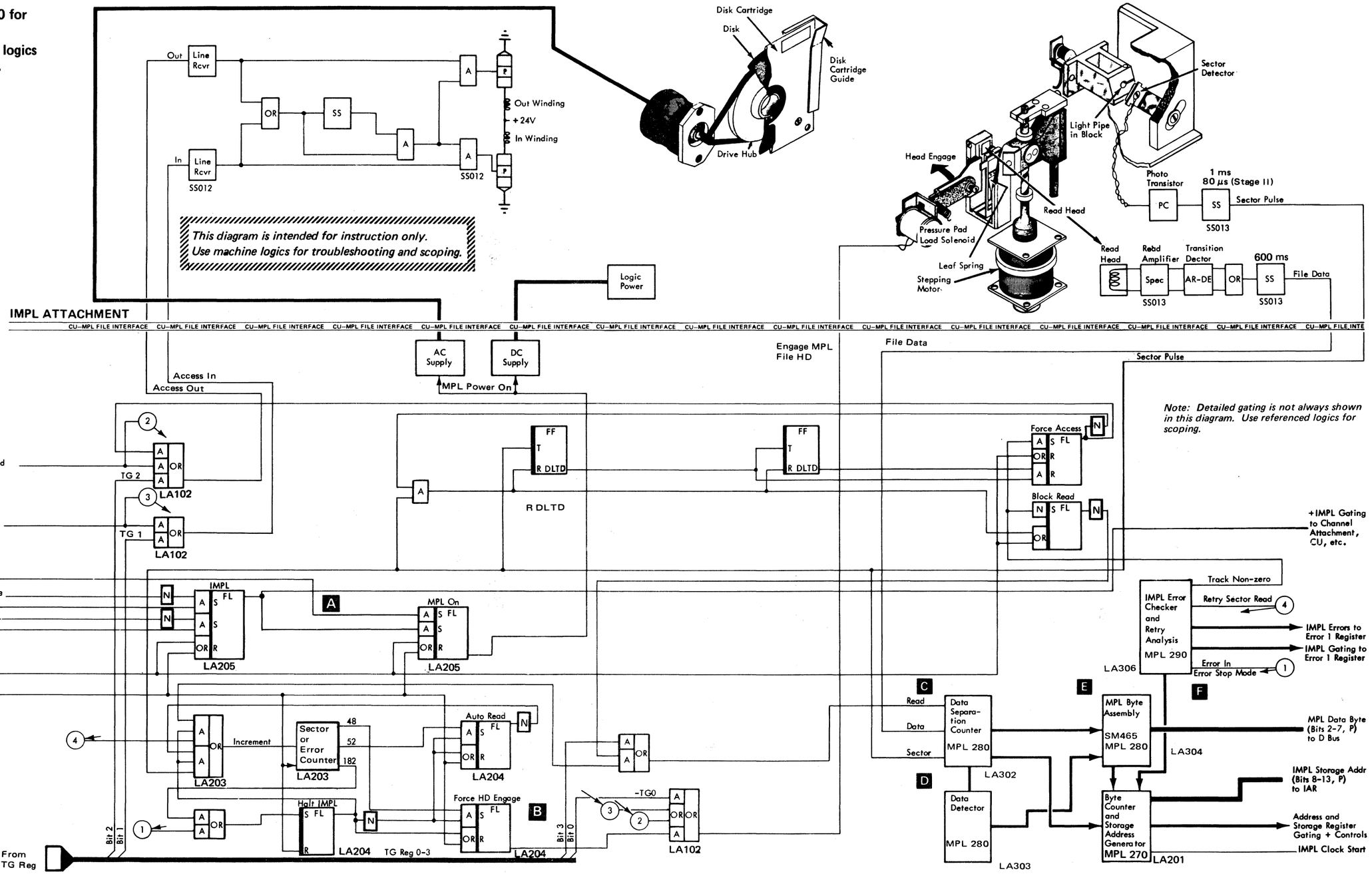
The first 64 words of the microprogram are loaded from the 23FD under hardware control each time power is sequenced on if the control unit is in Normal, Forced Logging, or CE Normal mode. The microprogram load can also be initiated manually by pressing the IMPL pushbutton if the CU is reset and in any CE mode.

Note: Blocks on this diagram are keyed to the positive logic diagram on MPL 245.



HARDWARE CONTROLLED IMPL (PART 2 OF 2)

- Refer to MPL 240 for operation.
- Refer to machine logics for circuit details.



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MICROPROGRAM CONTROLLED IMPL AND DIAGNOSTIC LOAD

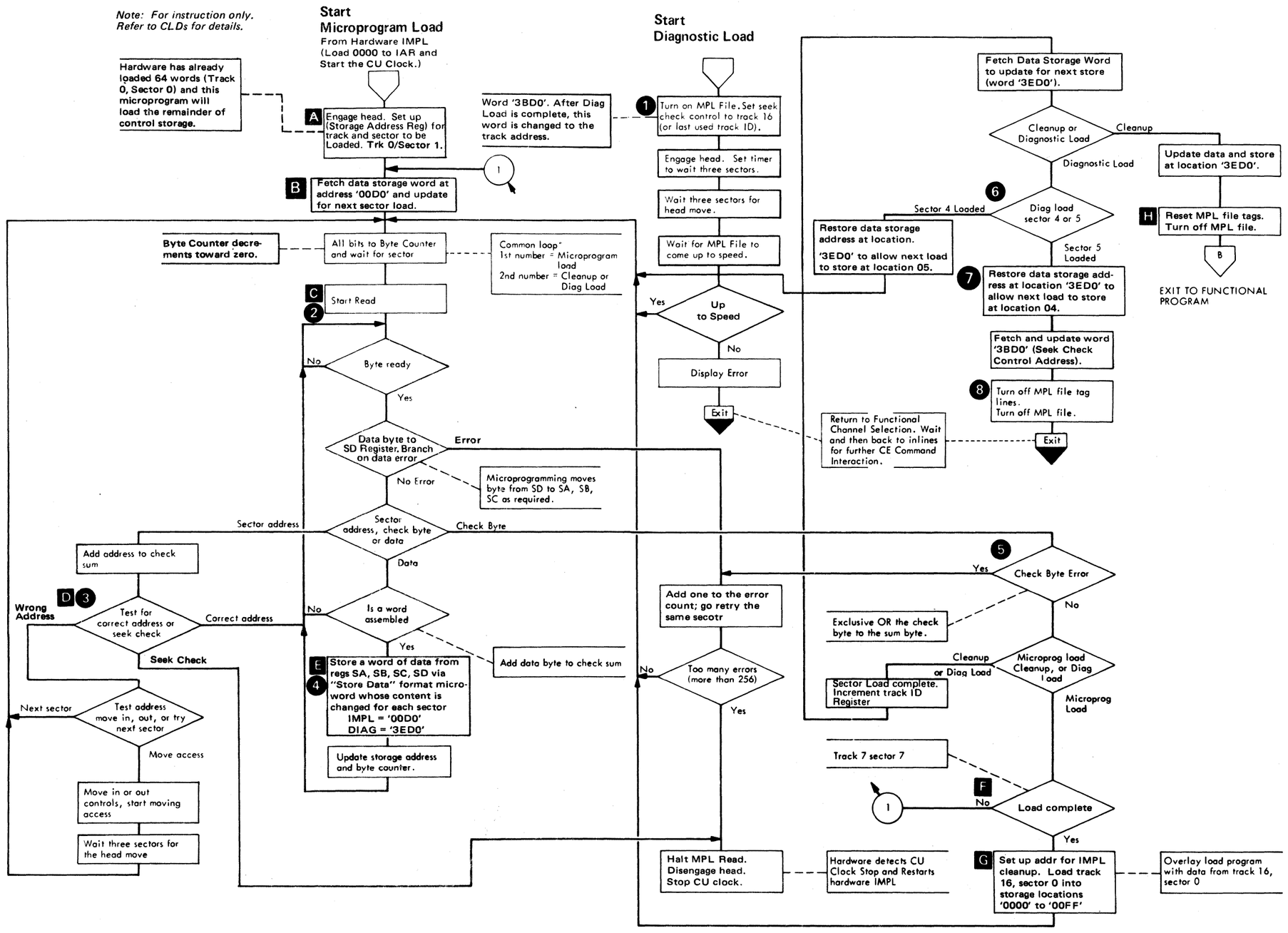
REFER TO MPL245

MICROPROGRAM LOAD OBJECTIVES

- A Engage read head.
- B Update the storage address (data storage location).
- C Read data.
- D Test address byte for correct address.
- E Load 256 bytes per sector.
- F Test for load complete.
- G Overlay the load program. (cleanup).
- H Turn off the MPL file.

DIAGNOSTIC LOAD OBJECTIVES

1. Turn on the MPL File.
2. Read data.
3. Test address byte for correct address.
4. Load 256 bytes per sector.
5. Test the check sum byte.
6. Load two sectors.
7. Get ready for next load.
8. Turn off the MPL File.



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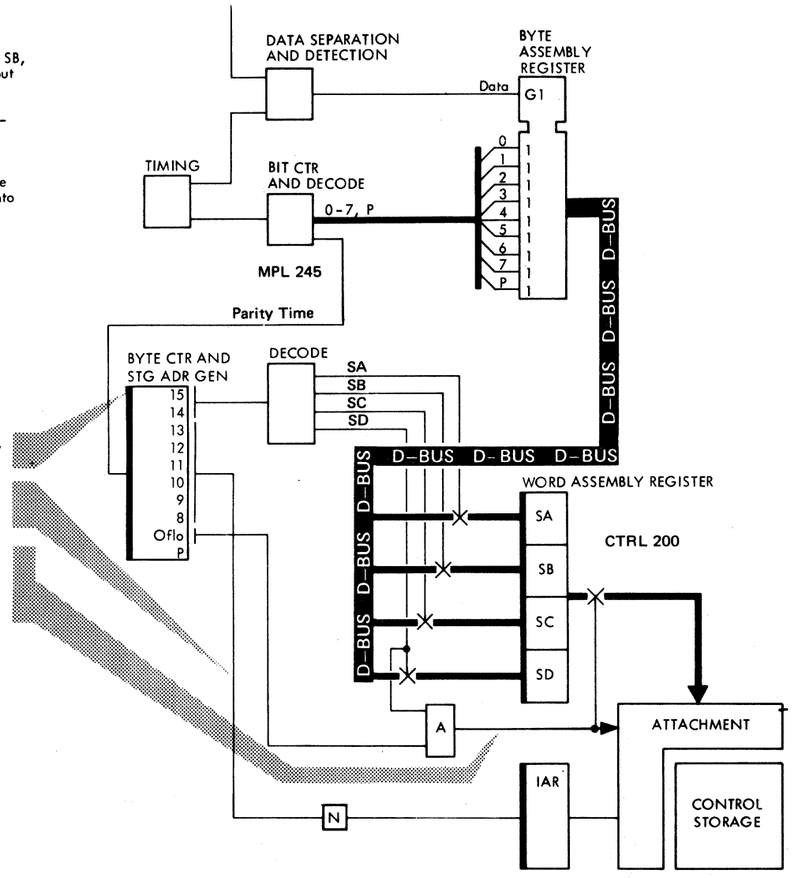
23FD/CONTROL STORAGE ADDRESSING

HARDWARE IMPL

- Word assembly register (SA, SB, SC, or SD) requires byte input control.
- Control storage needs an address for each 4-byte word stored.
- Control storage needs a write signal to place each word into storage.



BYTE COUNTER

1. Controls byte transfer to SA, SB, SC, or SD register.
2. Provides a control storage address to IAR for each word assembled.
3. Provides a pulse to the control storage that causes the control storage to write the assembled word into the address specified by IAR.

BYTE COUNTER STATUS FOR IMPL

1. The sector address (first byte) is not transferred because the store pulse is blocked by the overflow latch being off.
2. All bits are set on at the end of sector address byte parity time and the counter is then decremented every subsequent parity time.
3. Bits 8-13 (inverted) are gated to IAR at SD register time and used for the storage address.
4. Bits 14-15 control the data transfer (by byte) to the SA, SB, SC, and SD registers
5. The byte counter maintains parity and forces an IMPL error if the counter fails. See MPL 290.
6. When the byte counter contents indicate that the entire first sector has been loaded into control storage, the control unit clock is started so that the IMPL can continue under control of the microprogram just loaded.

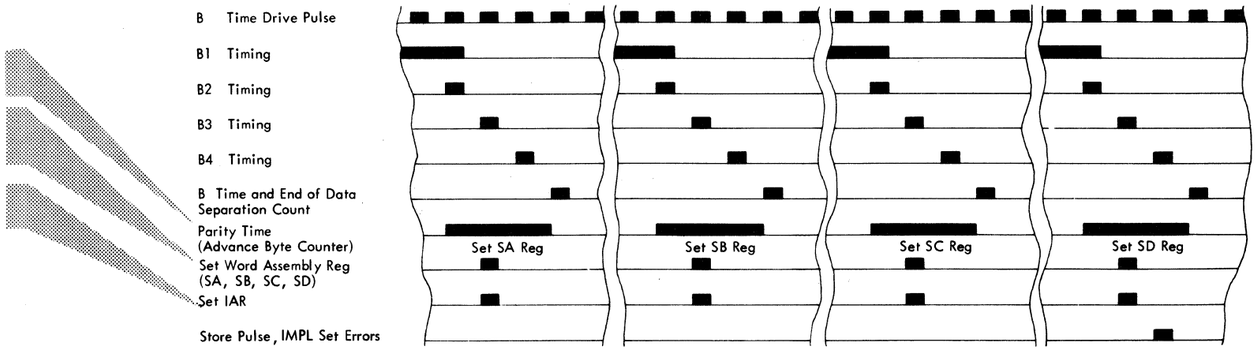
	BYTE COUNTER BITS										
	Over-flow	8	9	10	11	12	13	14	15	Store Pulse	Data To
Sector Address Byte	0	0	0	0	0	0	0	0	0		
0	1	1	1	1	1	1	1	1	1		SA Reg
1	1	1	1	1	1	1	1	1	0		SB Reg
2	1	1	1	1	1	1	1	0	1		SC Reg
3	1	1	1	1	1	1	1	0	0	X	SD Reg
4	1	1	1	1	1	1	0	1	1		SA Reg
5	1	1	1	1	1	1	0	1	0		SB Reg
6	1	1	1	1	1	1	0	0	1		SC Reg
7	1	1	1	1	1	1	0	0	0	X	SD Reg
Byte 255	1	0	0	0	0	0	0	0	0	X	SD Reg
Check Byte★	0	1	1	1	1	1	1	1	1		

★= Not transferred to the control unit under hardware IMPL.

BYTE COUNTER TIMING

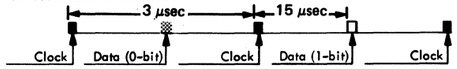
1. When the byte assembly register is filled, the parity time latch advances the byte counter.
2. Byte counter bits 14-15 cause the proper word assembly register to be set and the IAR to be set. Note that while the IAR is set 4 times, only the final state of each word is used as a control storage address.
3. When the SD register is filled, the IAR is set with the contents of bits 8-13 of the byte counter at B3 time and a store pulse is sent to the control storage at B4 time.

Timings for reference only.



READ DATA TIMING CONTROLS

This page is intended for instruction only.
Use machine logics for troubleshooting and scoping.



The objectives of the 23FD attachment timing pulses are to:

- **Locate the beginning of data on a sector.**
- **Place the data in a register, bit by bit, until the register is full (deserialize).**
- **Transfer the data into the control storage.**

A BEGINNING OF DATA

The beginning of each sector is defined by the sector pulse derived from a sector hole in the disk.

The first pulse on the disk after the sector pulse falls is a clock pulse which starts the 23FD attachment timing sequence.

B TIMING PULSES

Timing pulses for the 23FD attachment logic are generated from an oscillator (**KK101**). The oscillator pulses operate a frequency - dividing counter (data separation counter) that provides additional timing for the logic.

C DATA STROBE

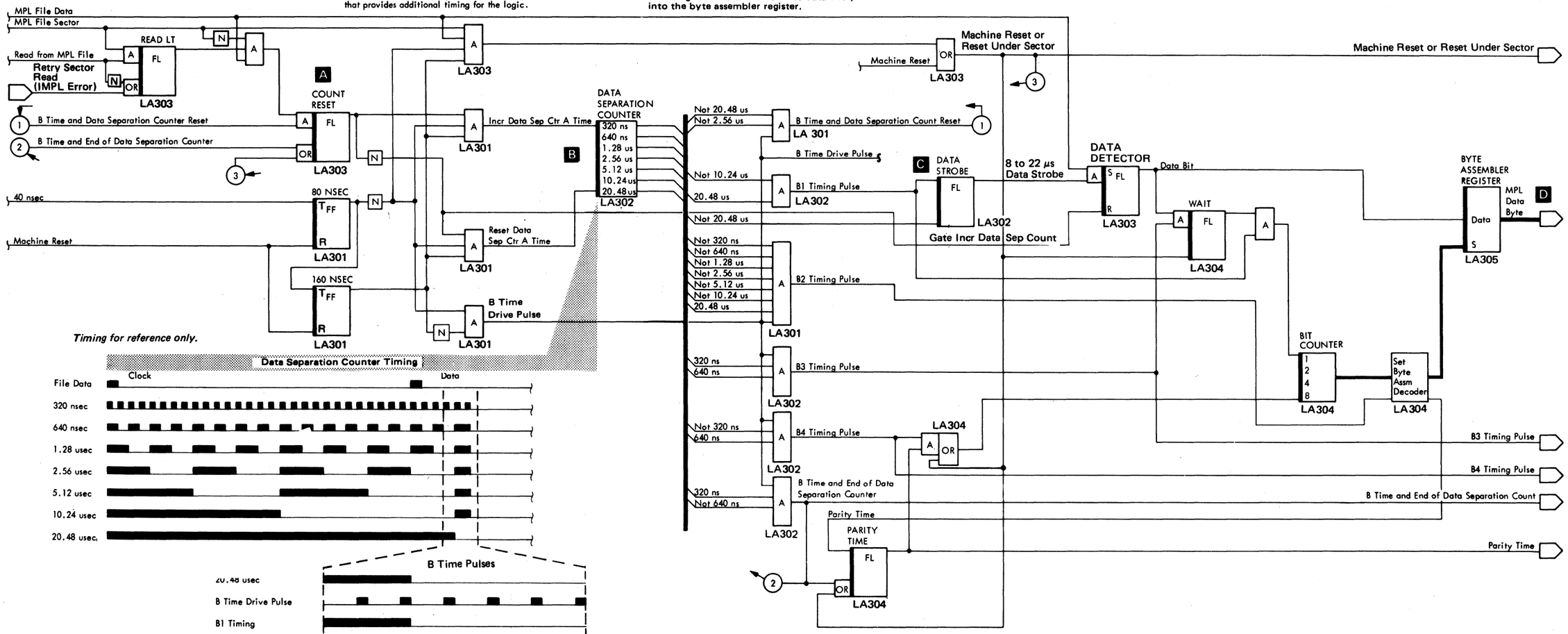
With the count reset latch set and the data separation counter running, data strobe conditions the data detect latch.

If a data bit is present, it sets the data detect latch. The first data bit in each sector is a sync bit which sets the wait latch too late for the bit counter to advance. Each prewritten clock pulse starts the data separation counter again, provided the data separation counter has run to completion. Outputs from the data separation counter are ANDed to provide the B-timing pulses that control the data flow and bit counting from data detection to data entry into the byte assembler register.

D DATA TRANSFER

When the byte assembler register is full, the parity time latch signals the byte counter to advance. The status of the byte counter :

1. Causes the assembled byte to transfer to the proper register (SA, SB, SC, or SD).
2. Provides a storage address for each word transferred to control storage.
3. Generates a store pulse every fourth byte to cause the assembled word to transfer into control storage.



Timing for reference only.

Data Separation Counter Timing

23FD ATTACHMENT ERRORS

Refer to MPL 245 Overall Diagram
Refer to MPL 295 for ECD's

A MPL FILE PARITY ERROR

During an IMPL Read operation, all data bytes are parity checked. A parity error blocks the Read operation and increments the error counter. The machine then searches for track 0, sector 0, and restarts the operation. During the search for track 0, sector 0, the error counter may be incremented up to eight times (one time for parity and seven times for sector not 0). A sector is retried 15 or 16 times before the error counter indicates IMPL is impossible and terminates the operation.

B TRACK NOT ZERO, SECTOR NOT ZERO

These signals are used to find track 0, sector 0 on an IMPL.
If the sector address byte indicates that the track is not 0, read is blocked, the head is moved outward one track, and the error counter is incremented.
If the address is track 0 but not sector 0, read is blocked, the error counter is incremented, and read is restarted at each succeeding sector until sector 0 is found or the error count indicates that IMPL is impossible.

C ERROR OR SECTOR COUNTER

This counter has two functions:

1. To count sector pulses in the IMPL sequence. At count **48** the head loads and at count 52 the **Auto Read** latch is turned on so reading can begin.
2. An error counter. Any IMPL retry increments this counter. If the counter exceeds **182, the operation** is terminated.

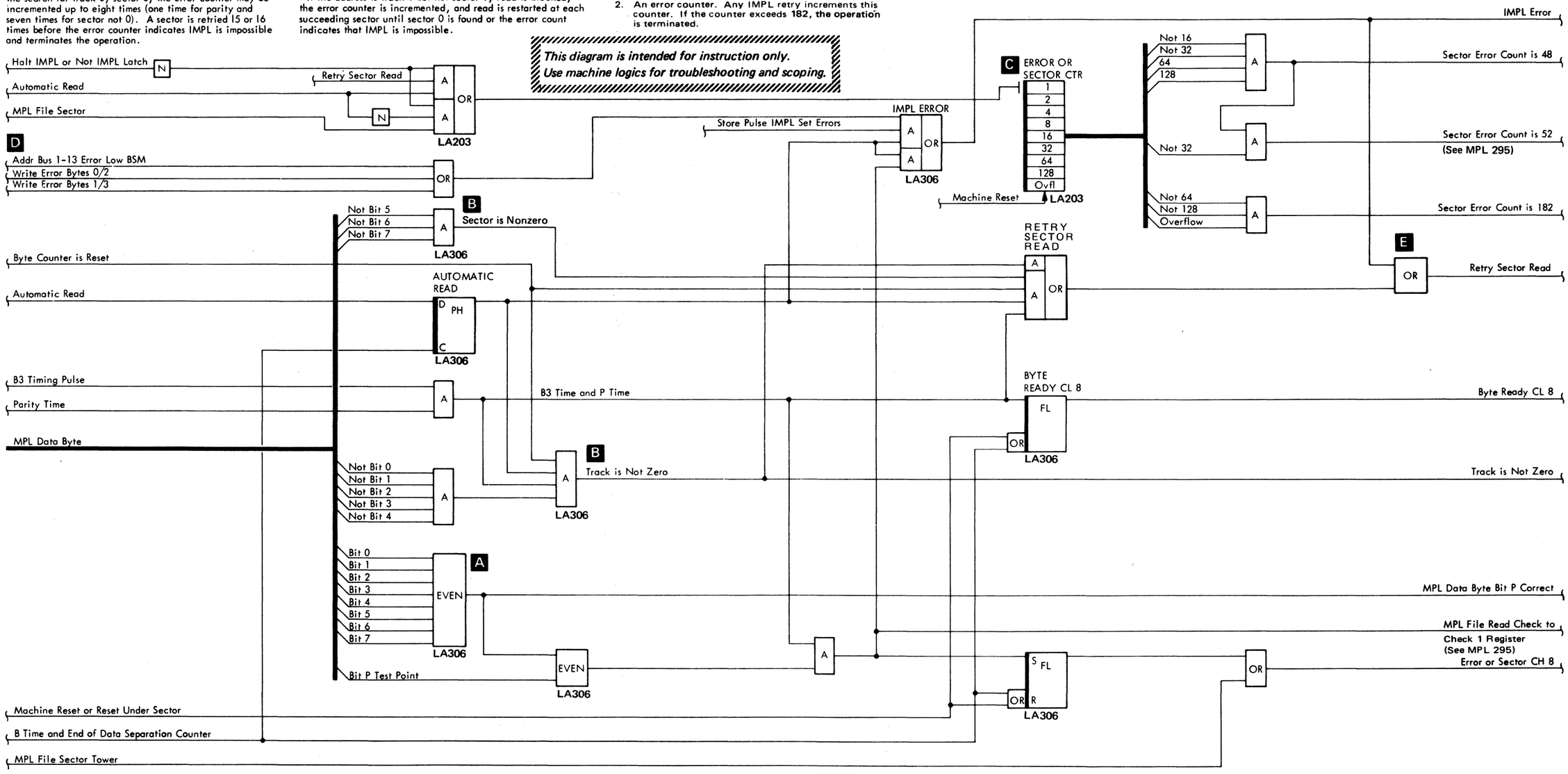
D ADDRESS BUS ERROR AND WRITE ERRORS

Address Bus 1-13 Error low indicates an error in the address generated for the control storage.
Write Error, Bytes 0/2 or 1/3 indicate an error in the data being stored in the control storage.

E IMPL ERROR

In CE Error Stop Mode, any hardware IMPL error will stop the IMPL process. A retry of a sector read will not.

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.



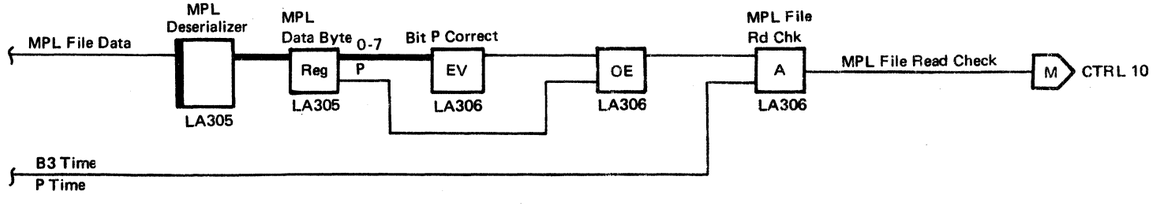
MPL FILE READ CHECK

Check 1 Register Bit 7 — Late (Bit 0=0)

MPL File Data enteres from the file in serial form. It is deserialized (LA305) and stored in the MPL Data Byte Register (LA305).

The parity bit is sent to an Exclusive OR block where it is matched against a P bit generated by the Even MPL Data Byte Bit P Correct Latch (LA305). The output of this latch is checked at B3 and P time and if the parity bits are different the Check 1 Bit 7 line is activated and the error is displayed in the Check 1 Register although the Check 1 lamp is not lit.

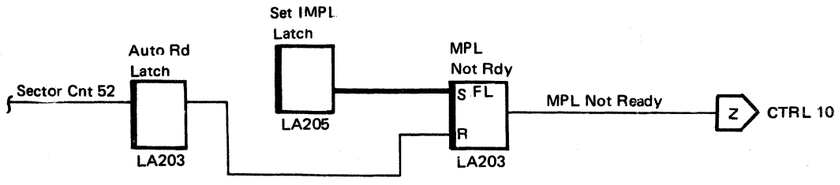
This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.



MPL FILE NOT READY

Check 1 Register Bit 14

MPL File Not Ready Error sets Bit 14 in the Check 1 Register. MPL Power On switch will turn bit 14 off after approximately four seconds unless there is an MPL File Not Ready error. The MPL Not Ready latch is set by the Set IMPL line and reset by the Auto Read line. This is conditioned by the Sector Count 52 line. If the MPL File is not ready the Sector Count 52 line will not be active. This will cause the MPL Not Ready latch to remain set and leave Bit 14 (MPL File Not Ready) light on in the Check 1 Register although the Check 1 lamp is not lit.



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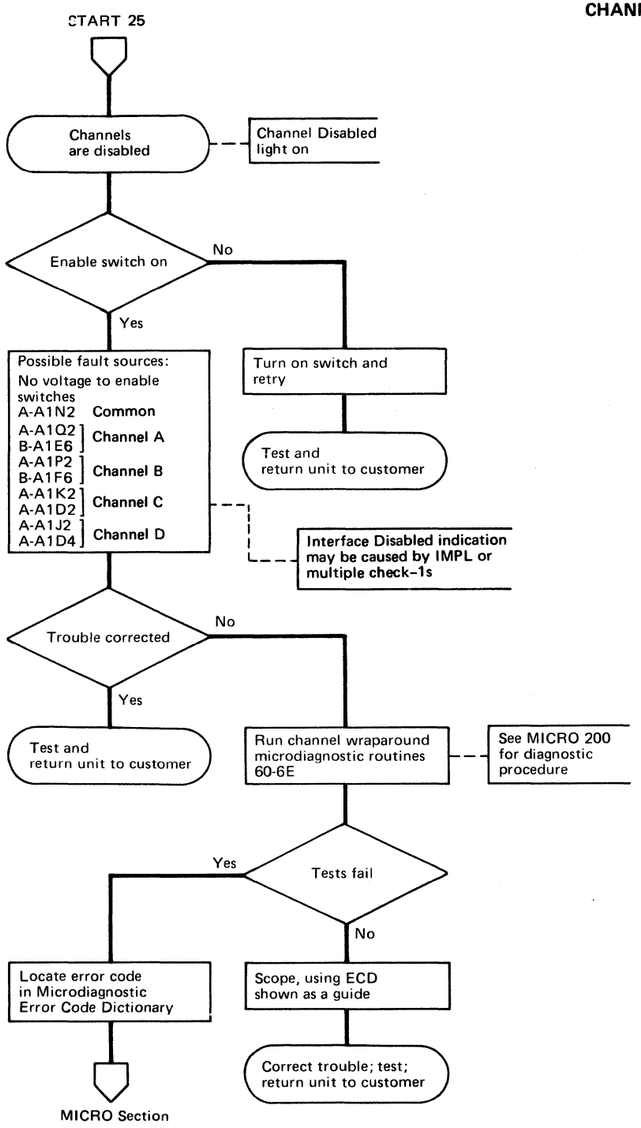
CONTENTS

CHL-I

CHANNEL DISABLED

ENABLED

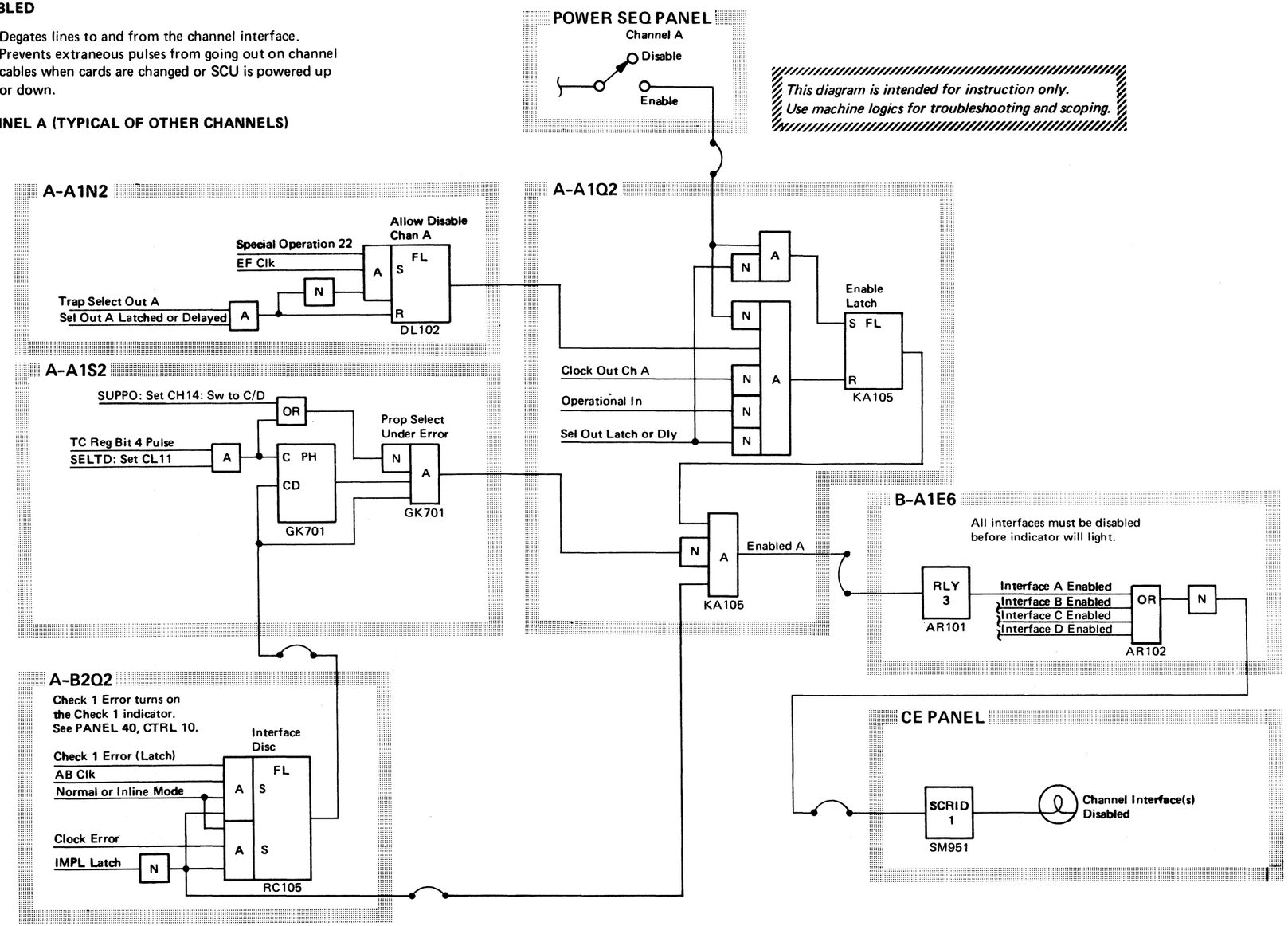
- Gates lines between the channel and the channel interface circuits.
- Allows operation of interface.



DISABLED

- Degates lines to and from the channel interface.
- Prevents extraneous pulses from going out on channel cables when cards are changed or SCU is powered up or down.

CHANNEL A (TYPICAL OF OTHER CHANNELS)



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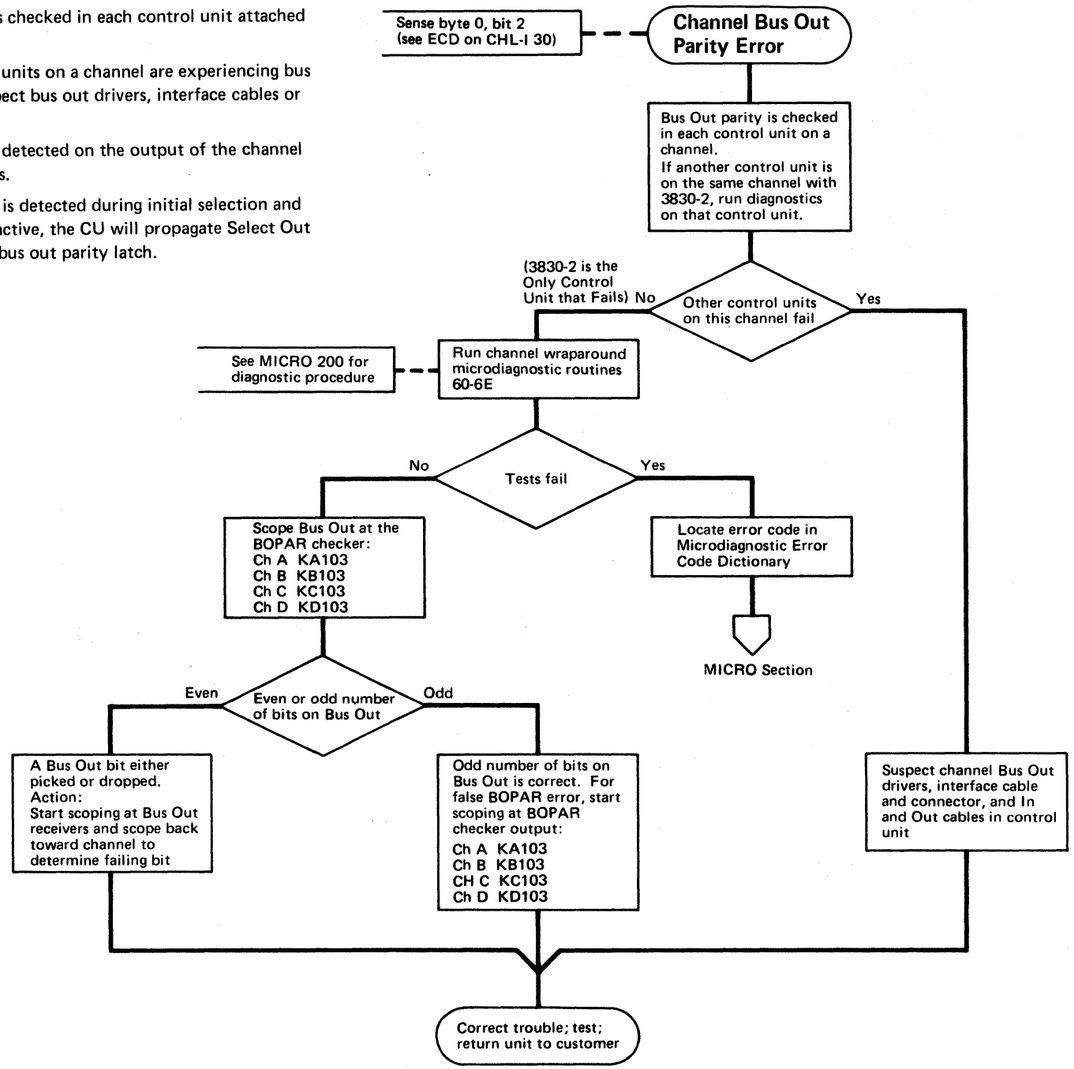
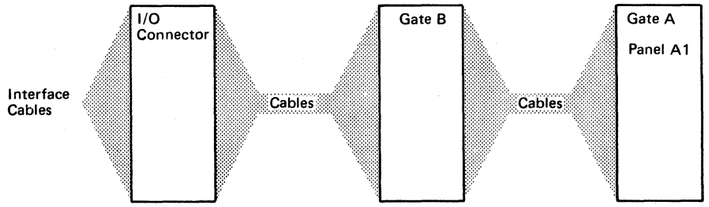
CHANNEL BUS OUT PARITY ERROR

- Bus out parity is checked in each control unit attached to a channel.
- If other control units on a channel are experiencing bus out checks, suspect bus out drivers, interface cables or connectors.
- Invalid parity is detected on the output of the channel bus out receivers.
- If invalid parity is detected during initial selection and Address Out is active, the CU will propagate Select Out and not set the bus out parity latch.



CHANNEL CABLES



Note: Interface cables from Channels C and D are routed from the I/O connector to the A gate.

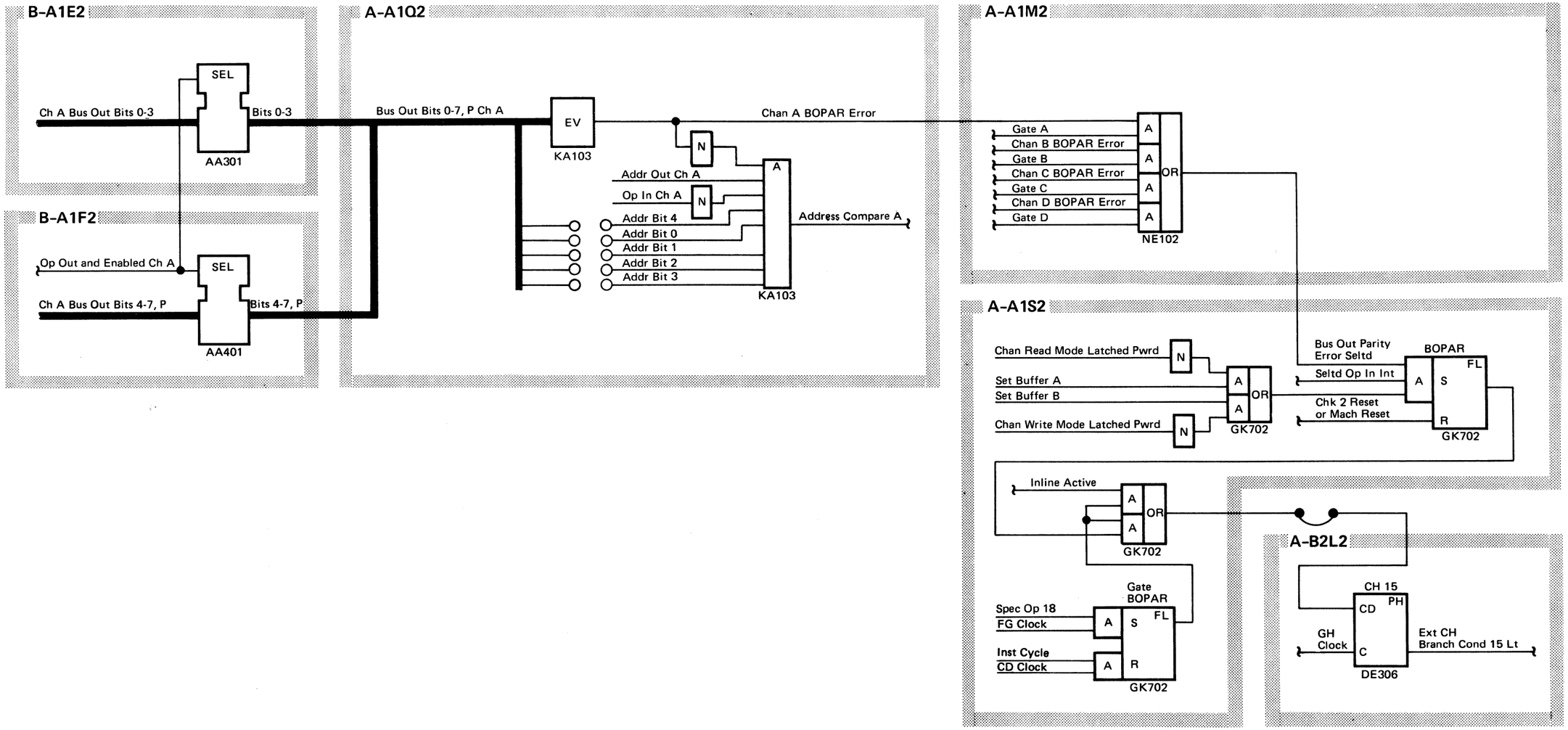
Channel Location:

Channel A (KA103)
Channel B (KB103)
Channel C (KC103)
Channel D (KD103)

CHANNEL BUS OUT PARITY ECD

CHANNEL A (TYPICAL OF OTHER CHANNELS)

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.



OVERRUN ECD

INITIAL SETUP

Xfer Latch A, Xfer Latch B, Micro Program Response, and Chan Response Latches are all off.

READ OPERATION

TC reg bit 1 (Chan Read) sets both transfer latches on. When the MD reg is set by microprogram, Xfer Latch A is reset. With Not Data Out, Not Chan Response Latch and Not Xfer Latch A, Data In to channel is raised. Channel sends Data Out, which again sets Xfer Latch A, and the Chan Response latch flips. The MD reg set pulse also flipped the Micro Program Response latch. When the MD reg is set again, Xfer Latch B is reset. This reset allows Service In to be sent to channel. Service Out will set Xfer Latch B. The operation continues until all bytes have been transferred. When Chan Read drops, all latches are reset.

WRITE OPERATION

Because both transfer latches and the Chan Response Latch are reset off, Data In may rise as soon as Chan Write comes up. Data Out causes Xfer Latch A to set and the Chan Response Latch to flip. Service In may now rise. Service Out will set Xfer Latch B and flip the Chan Response Latch again. Both buffers are now full, and further channel sequences depend on the CA of NA to cause a reset of Xfer Latch A. This reset allows Data In to channel. Data Out sets Xfer Latch B. CA of NA also causes the Micro Program Response Latch to flip. The next CA of NA causes the Xfer Latch B to reset. This reset allows Service In to channel. Service Out again sets Xfer Latch B. The operation continues until all bytes have been transferred. When Chan Write drops, all latches are reset.

OVERRUN (PERMANENT) (SENSE BYTE 0, BIT 5 AND BYTE 1, BIT 0)

This condition is set if more than ten data overruns are detected in any one CCW chain.

A data overrun is indicated (by microprogram) if Service Out or Data Out is not received by the CU within a specified time after Service In or Data In is presented to the channel, or if the duration of Service Out or Data Out is less than 80 nanoseconds. Each time that data overrun is detected, a counter in the CU error log is incremented and a request is made to the channel for command retry.

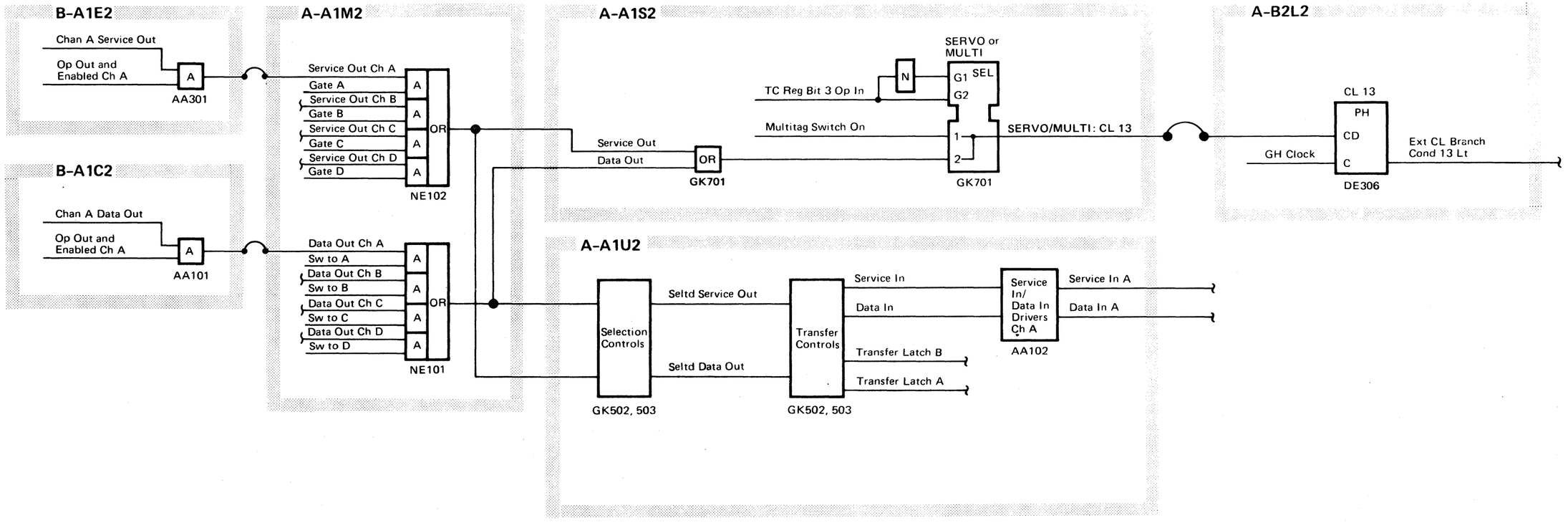
OVERRUN (NOT PERMANENT) (SENSE BYTE 0, BIT 5)

The following data overrun conditions always cause the overrun bit to be set in sense byte 0. Retry is accomplished by the system rather than channel command retry.

1. Data overruns that occur in a second or subsequent segment of an overflow operation.
2. Data overruns that occur during a format write.

CHANNEL A (TYPICAL OF OTHER CHANNELS)

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.



CONTROL UNIT INTERFACE ERRORS (Part 1 of 2)

START 30

Channel Detected Failure

1. Channel error lights.
2. CPU ROS address by:
   a. Hard stop display
   b. SEREP printout
3. Output from channel error log formatting program:
   a. EREP printout
   b. Online OLTS printout

This area deals with channel indicated control unit interface errors. (Error information is obtained by interrogating channel log out or channel error indications.) Determine type of error and use chart below to go to appropriate prodedure.

- CU Busy Check → 1
- Illegal Seq → 2
- No Response Check → 3
- UA No Compare → 4
- Log Disconnect In
- Channel Timeout
- Multiple In Tags
- Bus In Parity Check (Buffer Parity Check) → A, B, C

A → CHL-I 130
B → CHL-I 130
C → CHL-I 155

1 CONTROL UNIT BUSY CHECK

The short Control Unit Busy sequence was detected on the I/O interface during chained command reselection. Results in Interface Control Check

Possible Failing Cards			
Chan A	Chan B	Chan C	Chan D
A-A1Q2	A-A1P2	A-A1K2	A-A1J2
A-A1R2	A-A1R2	A-A1R2	A-A1R2
KA10x	KB10x	KC10x	KD10x
CS10x	CS10x	CS10x	CS10x

Card on page

Trouble corrected? Yes → Test and return unit to customer

No → Run channel wrap-around microdiagnostic routines 60-6E ↔ See MICRO 200 for diagnostic procedure

Tests fail? Yes → Locate error code in Microdiagnostic Error Code Dictionary → MICRO Section

No →

CHANNEL A (B)

Go to KA102 (KB102) and check HIO Busy Latch and its controls. Also suspect CS102 (CU Busy distribution)

CHANNEL C (D)

Go to KC102 (KD102) and check HIO Busy Latch and its controls. Also suspect CS102 (CU Busy distribution)

2 ILLEGAL SEQUENCE

Operational In fails when Select Out is active. Results in Interface Control Check

Possible Failing Cards			
Chan A	Chan B	Chan C	Chan D
A-A1Q2	A-A1P2	A-A1K2	A-A1J2
A-A1R2	A-A1R2	A-A1R2	A-A1R2
KA10x	KB10x	KC10x	KD10x
CS10x	CS10x	CS10x	CS10x

Card on page

Trouble corrected? Yes → Test and return unit to customer

No → Run channel wrap-around microdiagnostic routines 60-6E

Tests fail? Yes → Locate error code in Microdiagnostic Error Code Dictionary → MICRO Section

No →

CHANNEL A (B)

Go to KA102 (KB102) and check Op In and its associated controls. Also suspect CS101 (channel tie breaker)

CHANNEL C (D)

Go to KC102 (KD102) and check Op In and its associated controls. Also suspect CS101 (channel tie breaker)

3 NO RESPONSE CHECK

Select In response to Address Out in chained command unit selection. Results in Interface Control Check

Possible Failing Cards			
Chan A	Chan B	Chan C	Chan D
A-A1Q2	A-A1P2	A-A1K2	A-A1J2
KA10x	KB10x	KC10x	KD10x

Card on page

Troubled corrected? Yes → Test and return unit to customer

No → Run channel wrap-around microdiagnostic routines 60-6E ↔ See MICRO 200 for diagnostic procedure

Tests fail? Yes → Locate error code in Microdiagnostic Error Code Dictionary → MICRO Section

No →

CHANNEL A (B)

Go to KA103 (KB103). Address Compare, and check that address jumpers are connected properly (no shorts or opens). Also, check KA101 (KB101), Trap Select Out and control circuits. Another possibility is a bad receiver or interface cable. If this is suspected, go to CHL-I 30 and treat as a BOPAR

CHANNEL C (D)

Go to KC103 (KD103), Address Compare, and check that address jumpers are connected properly (no shorts or opens). Also check KC101 (KD101), Trap Select Out and control circuits. Another possibility is a bad receiver or interface cable. If this is suspected, go to CHL-I 30 and treat as a BOPAR

4 UA NO COMPARE

The address ent by the I/O unit does not agree with the address used by the channel. Results in Interface Control Check

Possible Failing Cards			
Chan A	Chan B	Chan C	Chan D
A-A1Q2	A-A1P2	A-A1K2	A-A1J2
KA10x	KB10x	KC10x	KD10x

Card on page

Trouble corrected? Yes → Test and return unit to customer

No → Run channel wrap-around microdiagnostic routines 60-6E ↔ See MICRO 200 for diagnostic procedure

Tests fail? Yes → Locate error code in Microdiagnostic Error Code Dictionary → MICRO Section

No →

CHANNEL A (B)

Go to KA104 (KB104), Control Unit Address, and check that jumpers are connected properly (no shorts or opens). Another possibility is a bad driver or interface cable. If this is the case, a Bus In parity check may also be detected. Go to CHL-I 155 and treat accordingly

CHANNEL C (D)

Go to KA104 (KB104), Control Unit Address, and check that jumpers are connected properly (no shorts or opens). Another possibility is a bad driver or interface cable. If this is the case, a Bus In parity check may also be detected. Go to CHL-I 155 and treat accordingly

Correct trouble; test; return unit to customer

CONTROL UNIT INTERFACE ERRORS (Part 2 of 2)

CHL-I 125 A

LOG DISCONNECT IN

A signal generated by the control unit to indicate that it cannot reliably communicate over the I/O interface. Results in Interface Control Check

ALL MACHINES

This is normally an indication that a Check 1 error was detected in the control unit. (If so, obtain sense information as on PANEL 40, then go to FSI 5 and develop fault symptom code.) If Check 1 error was not detected, it may be because of an error in Disconnect In. Another possibility, if not a Check 1 error, is a bad In Tag Driver or I/O Interface Cable

Possible Failing Units

Chan A	Chan B	Chan C	Chan D
A-A1S2	A-A1S2	A-A1S2	A-A1S2
B-A1D2	B-A1D4	A-A1G2	A-A1G4
I/O Interface Cable			
GK70x [AA20x CR10x]	GK70x [BA20x DR10x]	GK70x CA20x	GK70x DA20x

A1D2 and A1D4 are in the tailgate

Card on page

Trouble corrected — Yes → Test and return unit to customer

No

Run channel wrap-around microdiagnostic routines 60-6E — See MICRO 200 for diagnostic procedure

Tests fail — Yes → Locate error code in Microdiagnostic Error Code Dictionary → MICRO Section

Scope using ECD shown as a guide

Correct trouble; test; return unit to customer

CHL-I 125 B

Two types of timeouts exist:

1. 30 seconds from rise of Select Out to fall of Status In.
2. 30 seconds from one Device Service Request (Service In or Data In) to another request (Service In or Data In)

CHANNEL TIMEOUT

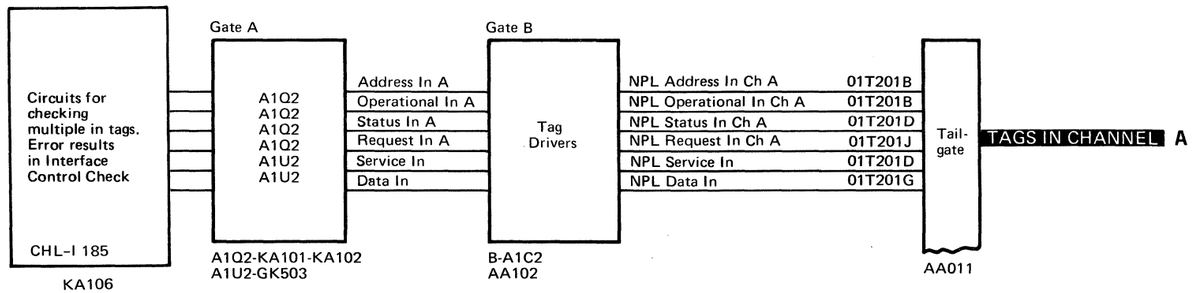
A unit selection sequence of any type on the I/O interface has exceeded a specified time period of 30 seconds or successive service requests by the device have exceeded 30 seconds.
The timing mechanism is in the channel and results in Channel Control Check

CHL-I 125 C

MULTIPLE IN TAGS

More than one in tag on the I/O interface is active at the same instant.
The in tags include Data In, Service In, Address In, and Status In.
Results in Interface Control Check

CHANNEL A (TYPICAL OF OTHER CHANNELS)



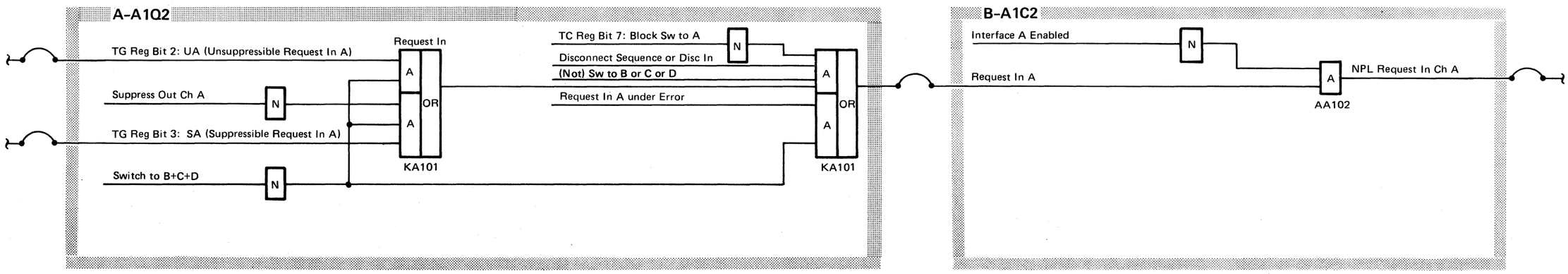
REQUEST IN

- SCU requests service of channel.
- Controlled by microprogram.
- See CHL-I 220 for additional information.

Service Tip: Check channel cable, cards, and interboard connections (A-B1 to A-A1, A-B2 to A-A1, A-A1 to B-A1).

This diagram is intended for instruction only. Use machine logics for troubleshooting and scoping.

CHANNEL A (TYPICAL OF OTHER CHANNELS)

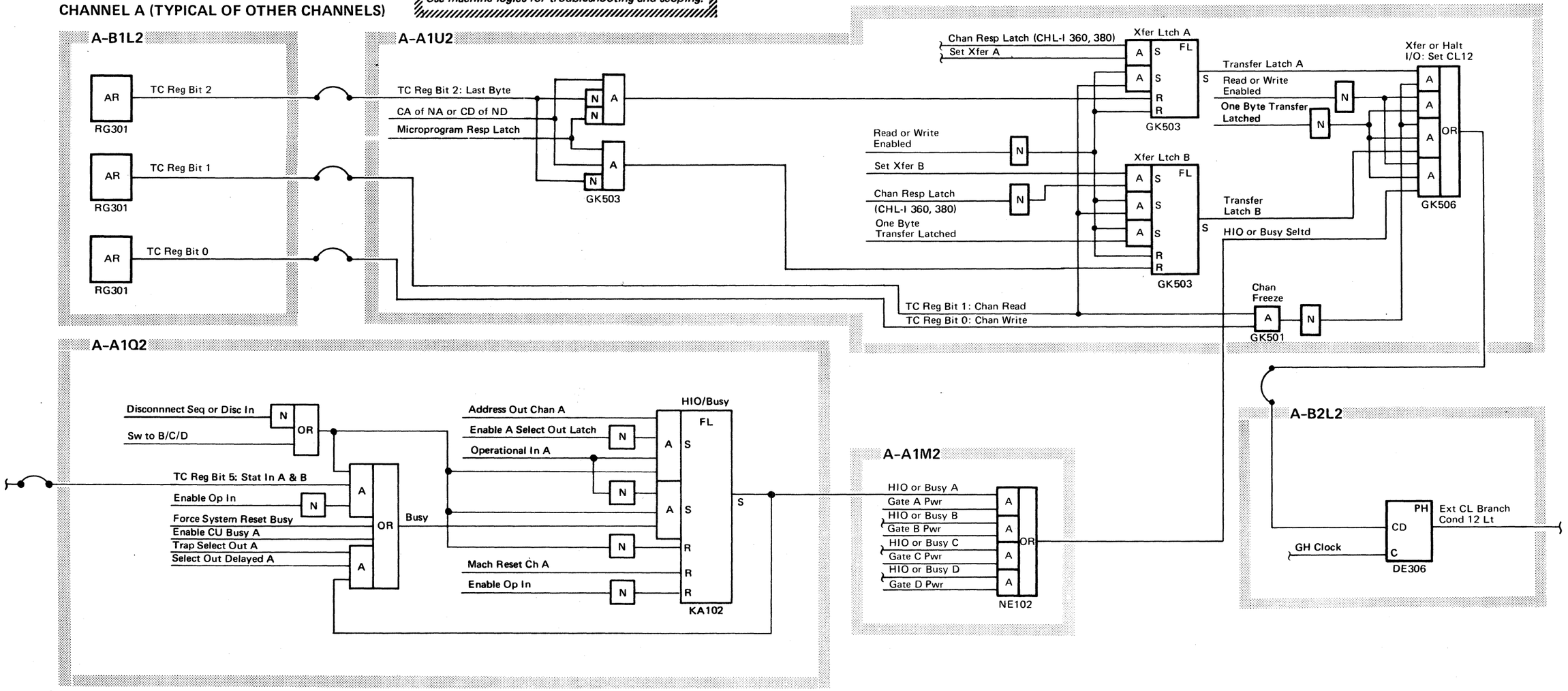


- Microprogram branch conditions.
- HLTIO indicates to the microprogram that the channel wishes to stop the selection sequence.
- XFER indicates to the microprogram that a byte of data is ready (write) or needed (read) by the channel.
- See CHL-I 200, 260 for additional information.

Service Tip: Check cards and interboard connections (A-B1 to A-A1, A-A1 to A-B2).

This diagram is intended for instruction only. Use machine logics for troubleshooting and scoping.

CHANNEL A (TYPICAL OF OTHER CHANNELS)



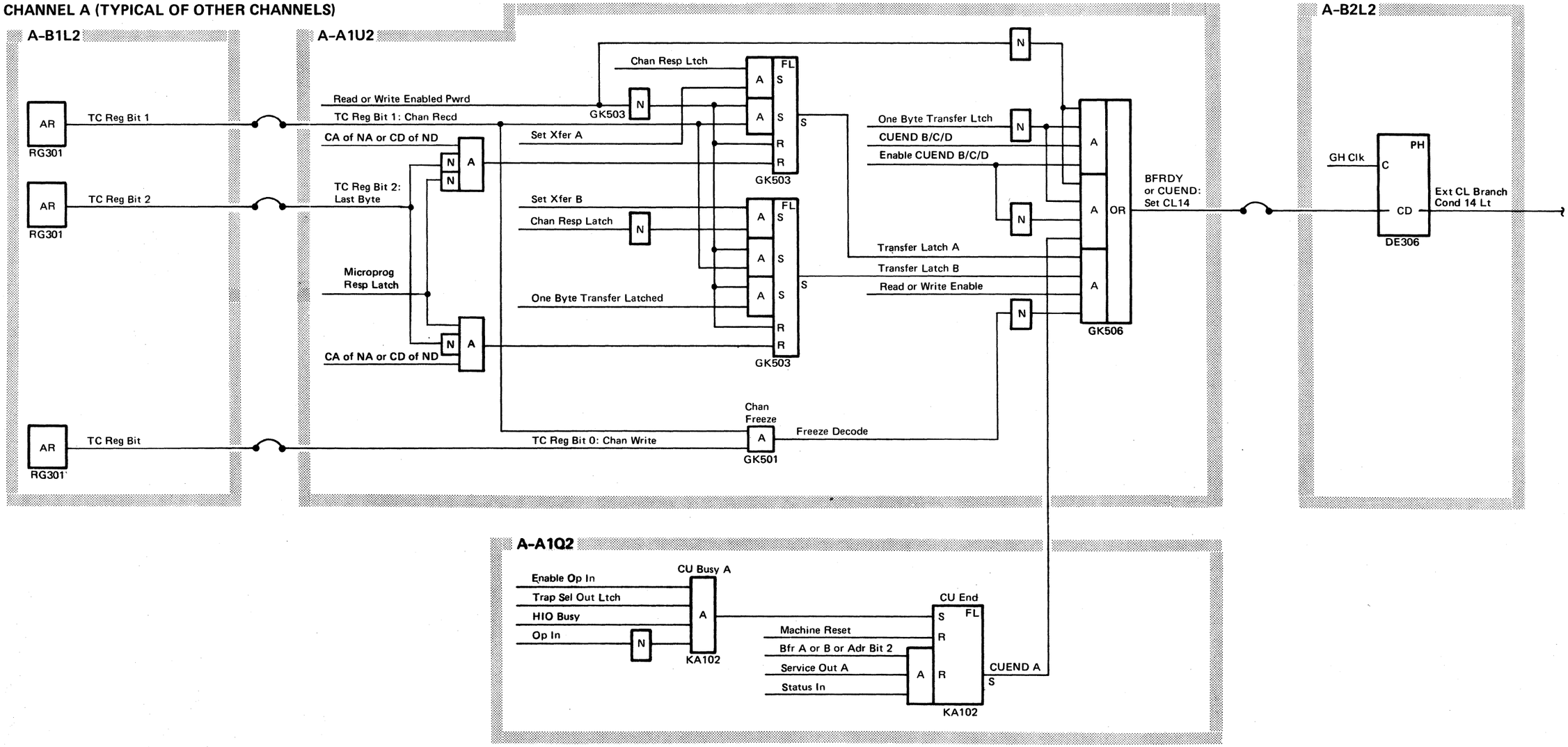
CUEND/BFRDY

- Microprogram branch conditions.
- CUEND indicates to the microprogram that the channel tried to select this SCU while the SCU was busy.
- BFRDY indicates to the microprogram that both channel interface buffers are full (write) or empty (read).
- See CHL-I 200, 260 for additional information.

Service Tip: Check cards and interboard connections (A-B1 to A-A1, A-A1 to A-B2).

This diagram is intended for instruction only. Use machine logics for troubleshooting and scoping.

CHANNEL A (TYPICAL OF OTHER CHANNELS)



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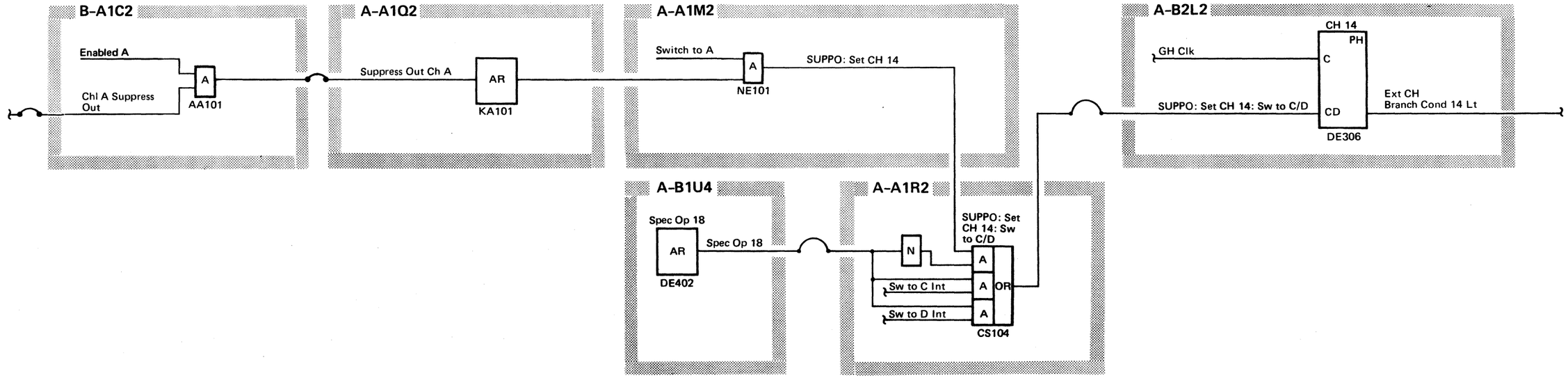
SUPPO/XCHAN

- Microprogram branch conditions.
- SUPPO indicates to the microprogram that the channel has a chain of commands for this SCU and that status and data from this SCU will be suppressed by the channel.
- XCHAN indicates to the microprogram that channel C or D has been selected, so that alternate channel controls can be set up.

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

CHANNEL A (TYPICAL OF OTHER CHANNELS)



BUFFER PARITY CHECK

Refer to CHL-I 160, 165

DESCRIPTION

A buffer parity check can occur during the following operations:

1. WRITE (TC register bit 0)
2. READ (TC register bit 1)
3. INITIAL SELECTION
   a. ADDRESS IN (TC register bit 4)
   b. STATUS IN (TC register bit 5)

When a control unit (CU) buffer parity check occurs, a check 2 error latch is set in the CU. The CU buffer parity check also causes Unit Check bit (bit 6) to be set in the status byte. A subsequent sense command sends up to 24 bytes of data to the system for analysis. The CU sense bytes contain a detailed description of the error. Refer to CTRL 650 for storage locations of the sense bytes or see SENSE or MSG section for more information.

WRITE: Data is checked for correct (odd) parity in the channel, sent over the bus out interface cable to the CU receivers, parity checked at the output of the CU receivers (BOPAR) and sent to the CU buffer. The output of the CU buffer. The output of the CU buffer is parity checked (odd) before entering the CU NA register. If even parity is detected, the buffer parity latch is set and odd parity is generated and sent to the NA register to avoid an error in the data leaving the CU buffer. The buffer parity check latch causes an attachment error (check 2 error).

READ: The control interface places data from the device into the CU MA register. The microprogram transfers the MA register contents to the MD register and sends the MD register contents to the CU buffer. The data is parity checked (odd) at the CU buffer and sent to channel over the bus-in interface cable. The channel receives the data and checks for odd parity before processing continues. A data check with a CU buffer parity error indicates that the input I/O device is failing.

ADDRESS IN/STATUS IN: The address or the status bytes are transferred to the CU MD register and the MD register contents are sent to the CU buffer. The output of the CU buffer is parity checked (odd) before being placed on the bus-in interface to the channel. A parity error during Address In or Status In causes an interface control check. See CHL-I 185 or SENSE section.

INTERPRETATION OF ERROR CONDITIONS

Note: Assume that no other error exists on the system.

Write

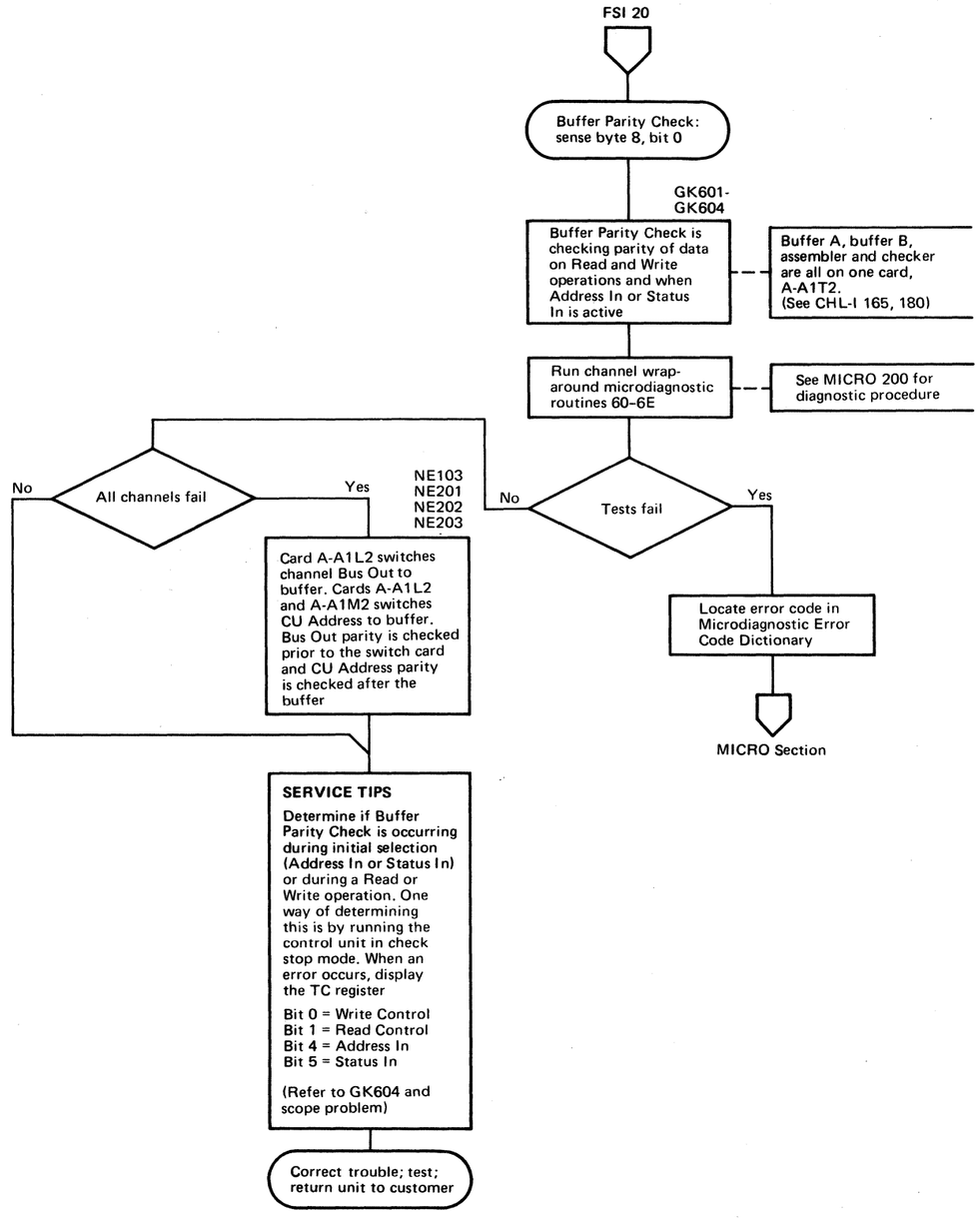
1. CU buffer parity check indicates that the failure occurred in the CU buffer or associated circuitry.
2. CU buffer parity check with CU bus out parity error (BOPAR) indicates that the channel drivers (bus out), the bus out interface cables, or the CU receivers and associated circuits could be failing.
3. CU buffer parity check with BOPAR and channel parity errors indicates a possible channel or system failure.

Read

1. CU buffer parity check indicates a parity error from the I/O device, the MA or MD register, or a CU buffer circuit failure.
2. A channel check indicates a failure in the CU drivers (bus in), the bus in interface cable, or the channel receivers (bus in).
3. CU buffer parity check with a channel check indicates a failure in the CU buffer, or more than one area of the machine is failing.
4. CU buffer parity check with a data check indicates that the I/O device is failing.

Address In/Status In

1. CU buffer parity check indicates input register errors or a failing CU buffer.
2. A channel check indicates a failure in the CU drivers (bus in), bus in interface cable or channel receivers (bus in).
3. CU buffer parity check with channel checks indicates that the CU buffer is failing or that there is more than one area failing.
4. CU buffer parity check during Address In or Status In causes an interface control check.



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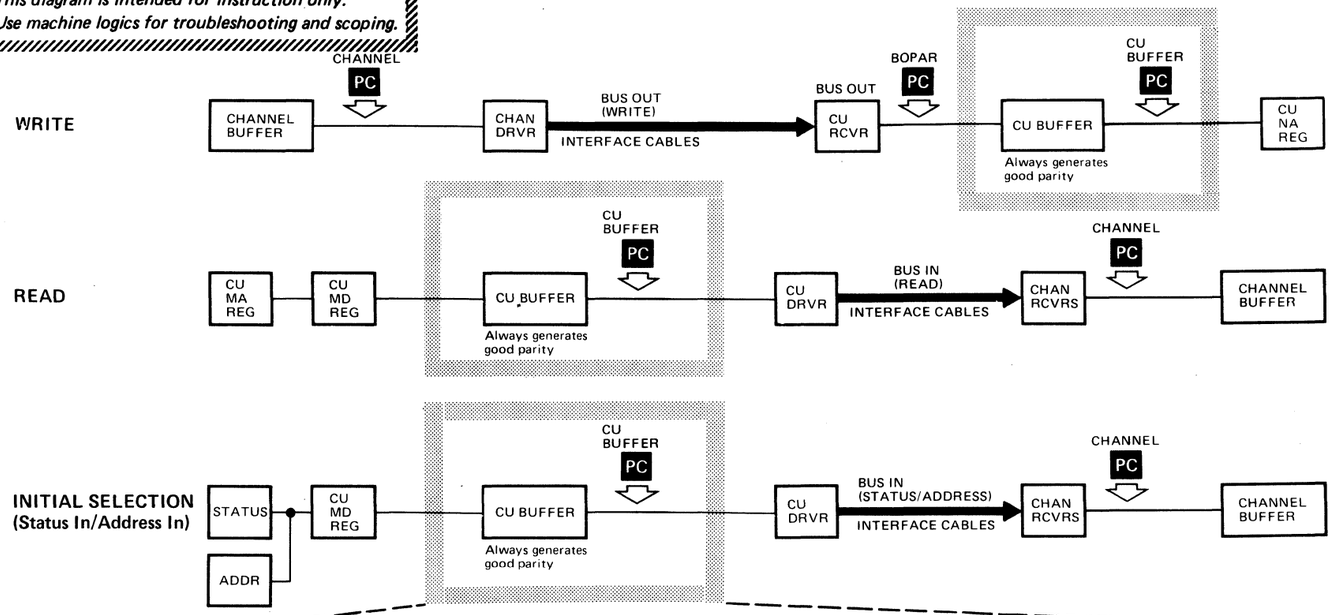
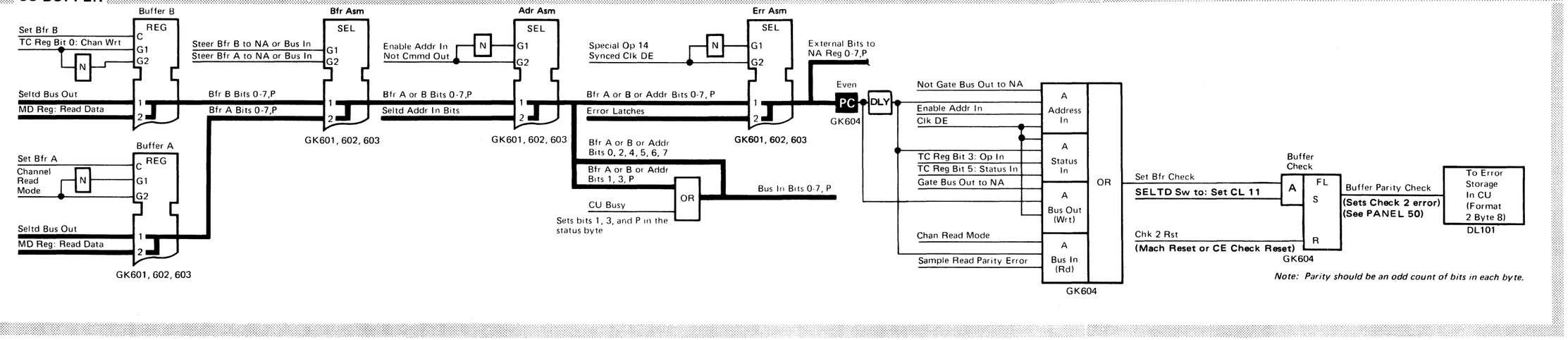
BUFFER PARITY CHECK ECD

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.



CU BUFFER



Note: Parity should be an odd count of bits in each byte.

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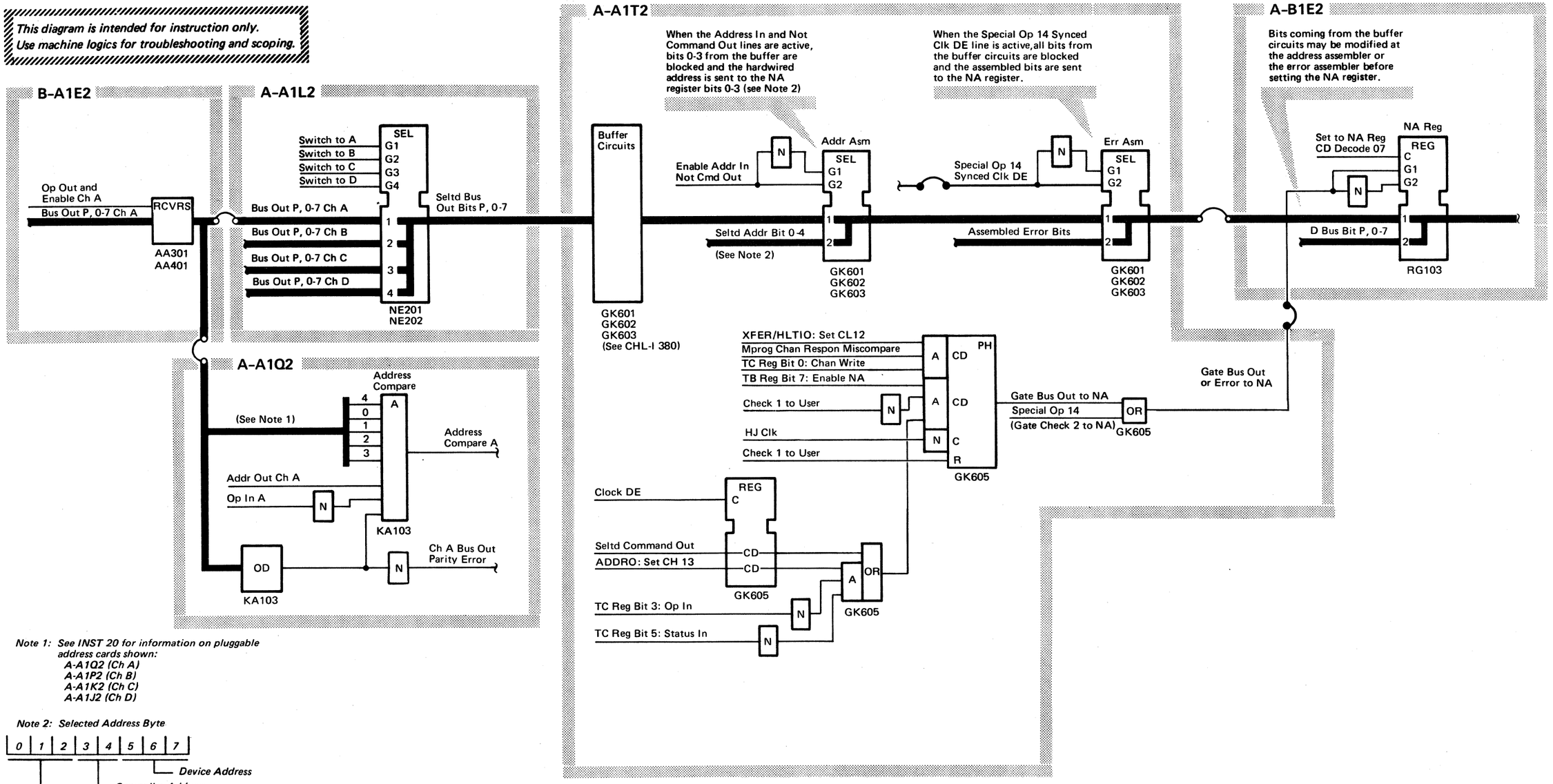
ADDRESS ASSEMBLER/ERROR ASSEMBLER

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.



Note 1: See INST 20 for information on pluggable address cards shown:
A-A1Q2 (Ch A)
A-A1P2 (Ch B)
A-A1K2 (Ch C)
A-A1J2 (Ch D)

Note 2: Selected Address Byte

With 32-drive expansion feature — Bits 0, 1 and 2 wired
Bits 3 and 4 not connected
Without 32-drive expansion feature — Bits 0, 1, 2, and 3 wired
Bit 4 not connected

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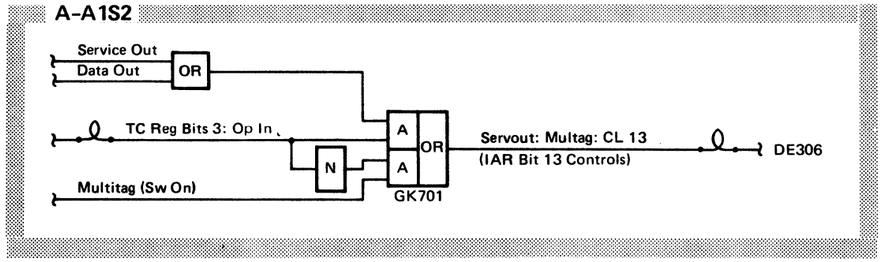
SERVO/MULTI AND RSPON/CHANB

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

SERVO/MULTI BRANCH

When the channel signals that a byte is ready, the CU microprogram branches on Servo/Multi (CL13) to service the channel request.

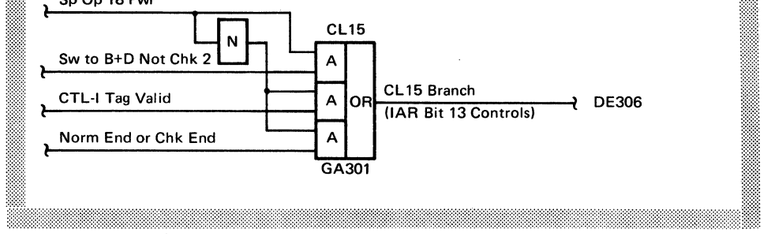
The channel interface Multitag switch (PANEL 1) is checked, and if on, the logic brings up this branch to notify the microprogram.



RSPON/CHANB BRANCH

On machines with Two Channel Switch or Two Channel Switch Additional, when the selection switch circuits are in the switched to B or D condition, the CHANB (CL 15) branch is set for microprogram checking.

This branch is also used to indicate to the microprogram that a control interface sequence is completed.

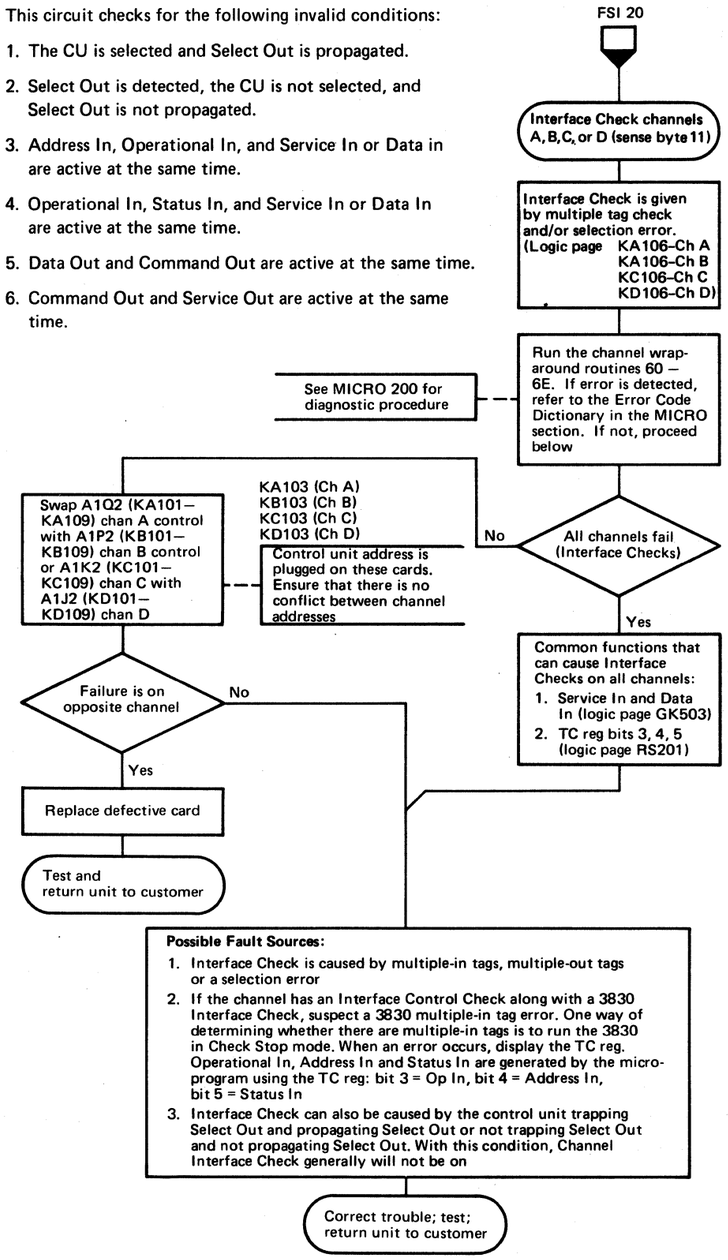


INTERFACE CHECK/MULTICONNECT ERROR

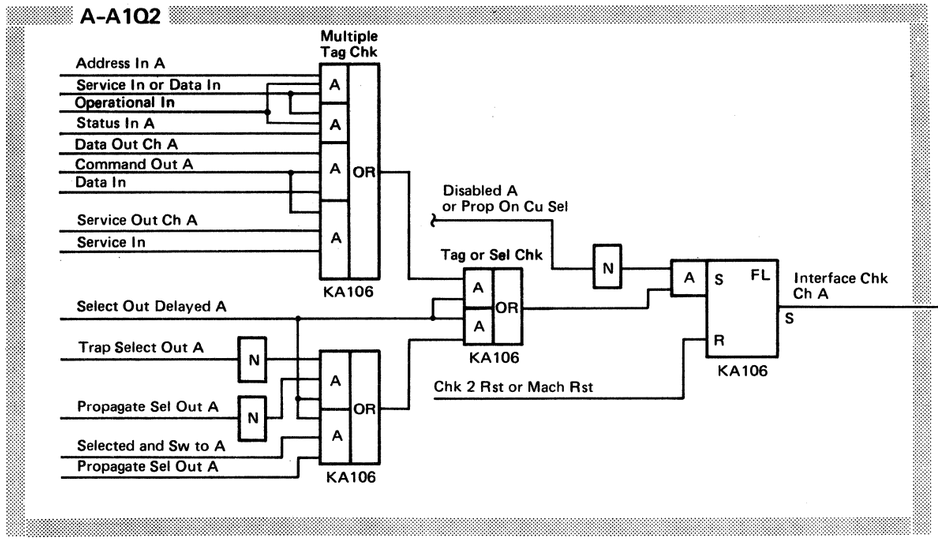
This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

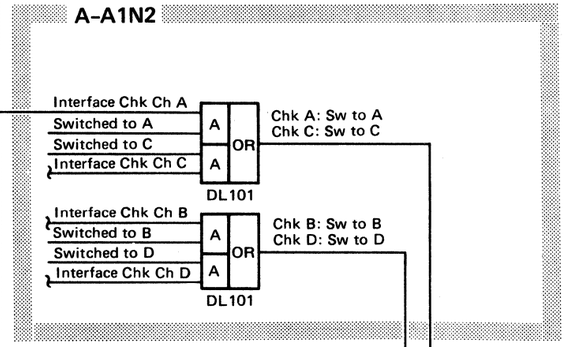
This circuit checks for the following invalid conditions:

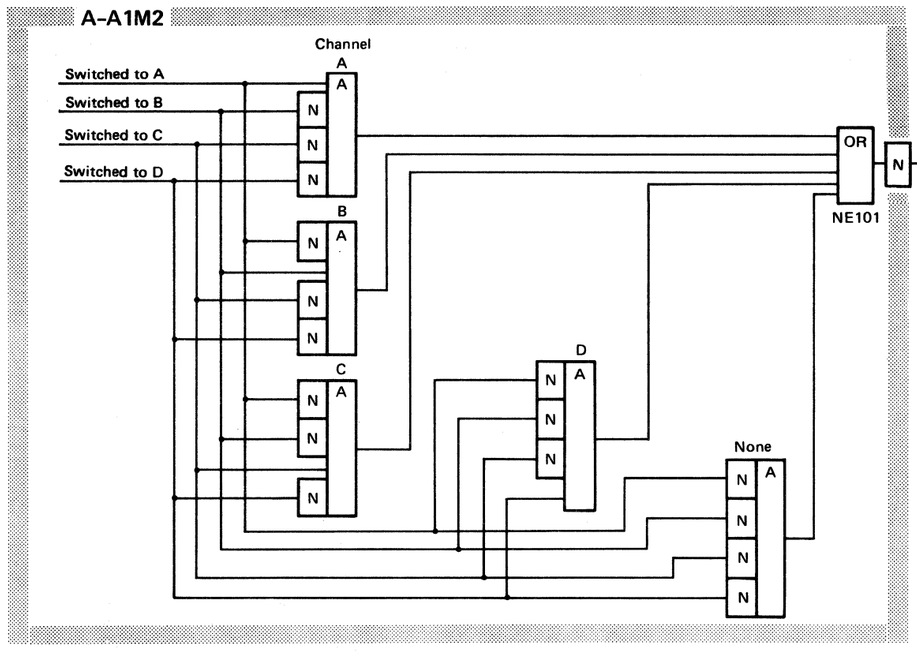
1. The CU is selected and Select Out is propagated.
2. Select Out is detected, the CU is not selected, and Select Out is not propagated.
3. Address In, Operational In, and Service In or Data in are active at the same time.
4. Operational In, Status In, and Service In or Data In are active at the same time.
5. Data Out and Command Out are active at the same time.
6. Command Out and Service Out are active at the same time.

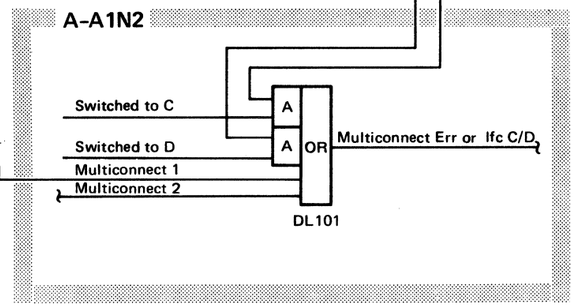


CHANNEL A (TYPICAL OF ALL CHANNELS)









BK1900 Seq. 2 of 2	2347137 Part Number	437402A 15 Mar 72	437404 23 Jun 72	437405 15 Aug 72	437408 16 Oct 72	437414 4 Jun 73	437416 11 Jan 74	

SYSTEM RESET AND SELECTIVE RESET

SELECTIVE RESET

Selective Reset is indicated whenever Suppress Out is up and Operational Out drops.

Selective Reset is issued only as a result of a malfunction detected at the channel, a time-out by the channel, or Disconnect In detected by the channel.

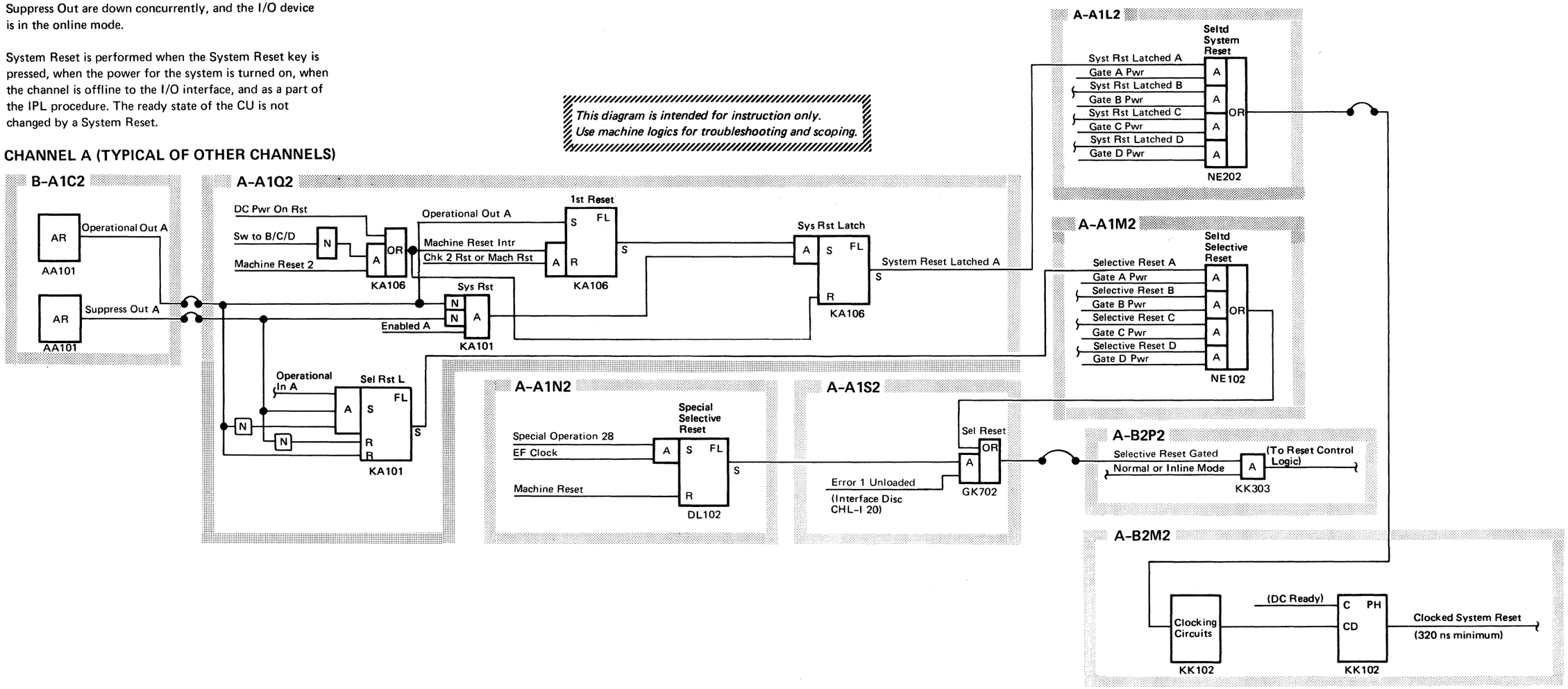
SYSTEM RESET

System Reset is indicated whenever Operational Out and Suppress Out are down concurrently, and the I/O device is in the online mode.

System Reset is performed when the System Reset key is pressed, when the power for the system is turned on, when the channel is offline to the I/O interface, and as a part of the IPL procedure. The ready state of the CU is not changed by a System Reset.

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

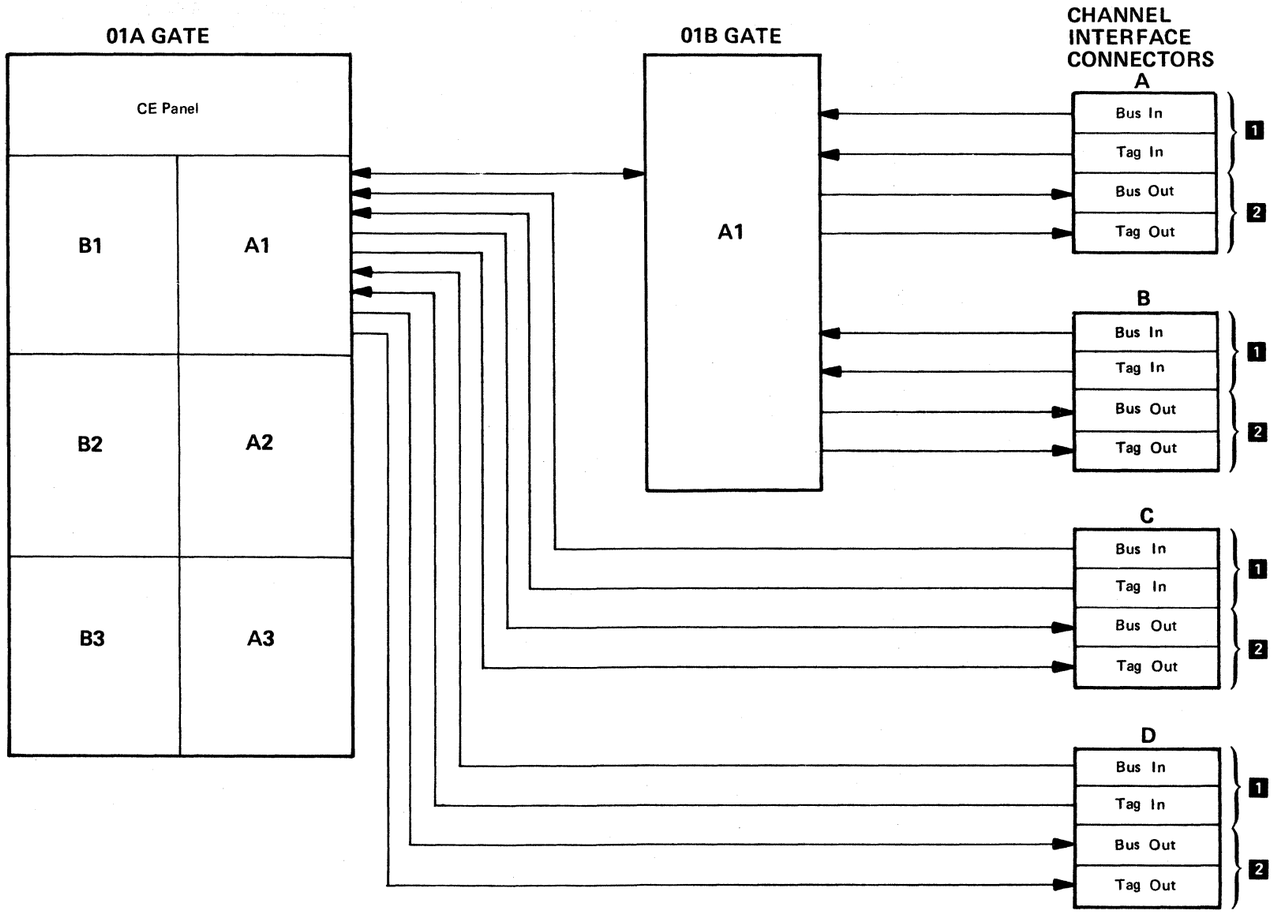
CHANNEL A (TYPICAL OF OTHER CHANNELS)



BK1920 Seq 1 of 2	2354772 Part Number	437408 16 Oct 72	437414 4 Jun 73	437416 11 Jan 74				

CHANNEL INTERBOARD WIRING CHART

CHANNEL INTERBOARD WIRING CHART CHL-I 194

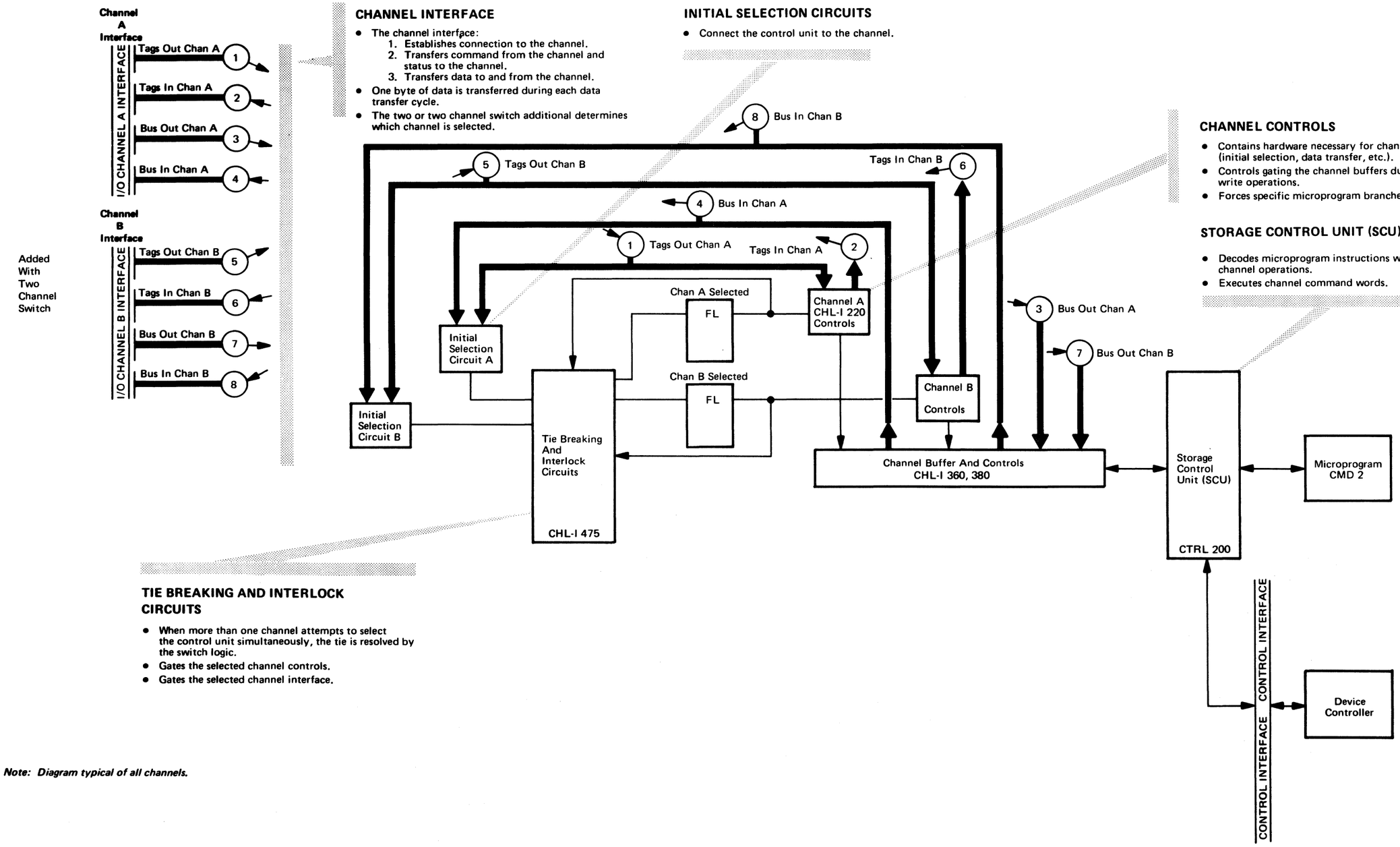


Notes:

1. *Incoming from channel or another control unit.*
2. *Outgoing to terminators or another control unit.*

BK1920 Seq 2 of 2	2354772 Part Number	437408 16 Oct 72	437414 4 Jun 73	437416 11 Jan 74				

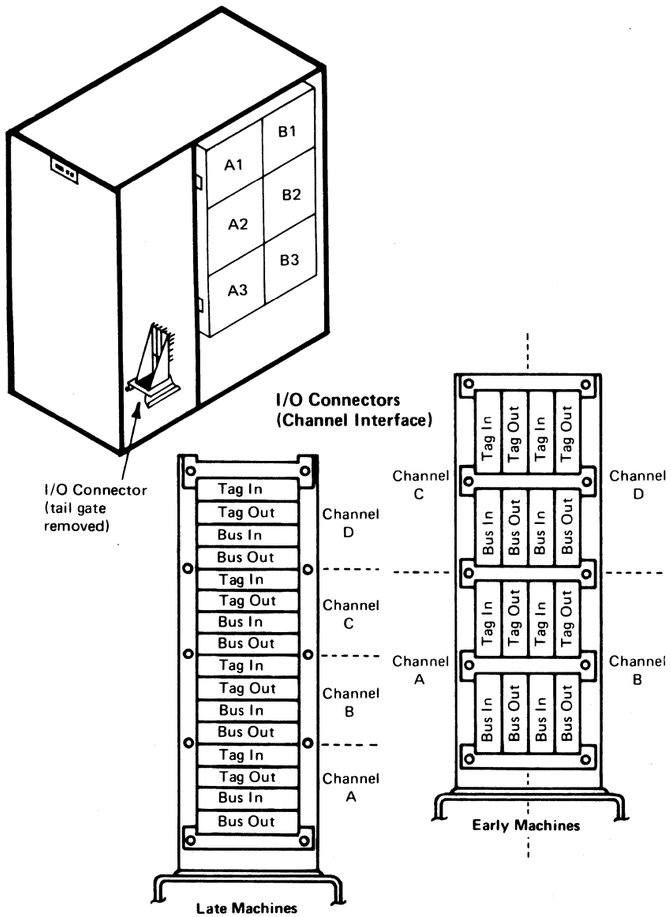
CHANNEL INTERFACE LOGIC FLOW



Note: Diagram typical of all channels.

CHANNEL INTERFACE INTRODUCTION (Part 1 of 2)

- The channel interface provides a common connection between the channel and the control unit.
- Selection lines are routed serially through each control unit to allow sequential connection to the channel.
- Information format is common to all control units.
- Designed for use with block multiplex channels.
- The control unit (CU) remains attached to the interface until it transfers all information or until the channel signals to disconnect.
- In block multiplex operation, the channel forces burst mode until Channel End time, but does not force burst mode between Channel End and Device End. The channel (by dropping Select Out) allows the control unit to disconnect following the presentation of Channel End alone even though command chaining is indicated.
- When chaining on a block multiplex channel operating in selector mode, the channel maintains selection until both Channel End and Device End have been received.
- Channel B is added with Two Channel Switch feature Channel C and D are added with Two Channel Switch Additional.
- Offset Interlock must be installed in the CU if 3350 devices are attached.



TAG OUT

- Identify the information on Bus Out lines.
- Remain active until an inbound tag responds.

A OPERATIONAL OUT

- Gates all outbound tag lines and is raised with CPU power-on reset.
- Dropped by channel for system reset.

C HOLD OUT

- Controls the effect of Select Out, allowing additional channel control of polling.
- Dropping Hold Out while Select Out is active causes the polling sequence to be terminated.

D SELECT OUT

- Used to select or poll**CU.
- Connected serially through each CU.
- Selection priority determined by internal jumpering of priority card in CU.
- If selected, CU raises Operational In. If not, Select Out is propagated to the next CU.

F ADDRESS OUT

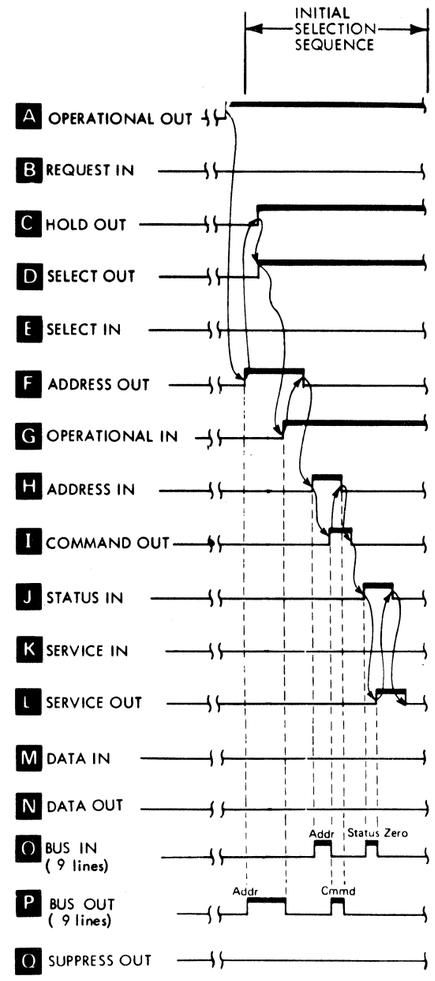
- Identifies information on bus out as being device address.
- Dropping Select Out while address is active forces a Halt I/O (HIO), and the CU disconnects from the interface.

I COMMAND OUT

- Identifies information on bus out as a command.
- Terminates current operation when used as a response to Service In/Data In.
- Causes CU to stack status when used as a response to Status In.

L SERVICE OUT

- Indicates channel has accepted data on bus in (Read operation).
- Indicates channel has provided, on bus out, the data requested by Service In (Write operation).
- Signals CU status was accepted when used as a response to Status In.



**Selecting CU means raising Select Out and Address Out. Polling CU means raising Select Out without Address Out.

TAG IN

- Identify the information on Bus-In lines
- Remain active until an outbound tag responds, unless operating in Offset mode.

B REQUEST IN*

- Invokes a reselection sequence from the channel.
- Indicates the CU is ready to present status.
- Concurrent Request Ins from two or more CUs are resolved by channel.

E SELECT IN

- The return path for Select Out.
- Indicates to channel that a CU was not selected (all CUs propagated Select Out).

G OPERATIONAL IN

- Signals the channel that a CU is selected and prevents another CU from connecting to the interface (blocks the propagation of Select Out).
- Active until all required information is transferred.

H ADDRESS IN

- Identifies information on bus in as being the device address.

J STATUS IN

- Identifies information on bus in as a status byte.
- Remains active until channel raises Service Out (accept), or Command Out (stack).

K SERVICE IN

- Signals the channel when the selected device wants to transmit or receive data.
- Remains active until channel responds with Service Out, Command Out, or Address Out, except in Offset mode, then, Service In is controlled by the data rate (See CHL-I 265).

M DATA IN

- Signals the channel when the selected device wants to transmit or receive data.
- Remains active until channel responds with Data Out, Command Out, or Address Out, except in Offset mode, then, Data In is controlled by the data rate (See CHL-I 265)

Continued on CHL-I 225

*Under microprogram control.

CHANNEL INTERFACE INTRODUCTION (Part 2 of 2)

From CHL-I 220

N Data Out

- Indicates channel has accepted data on bus in (read operation).
- Indicates channel has provided, on bus out, the data requested by data in (write operation).

( ) Bus In

- Transfers address, status, or data information to the channel.
- Signals are valid from 100ns after the rise of an identifying inbound tag to the rise of the responding outbound tag.
- Signals are valid only when Op In is active in CU busy sequence.

P Bus Out

- Transfers data, control or address information to the SCU.
- Signals are valid from the rise of the identifying outbound tag to the rise of the responding inbound tag.

( ) Suppress Out

- Used alone or with another tag to:
  a. suppress status
  b. suppress data transfer
  c. chain command control
  d. selective reset

SPECIAL CONTROL LINES

Disconnect In

- The Disconnect In line is activated by the CU whenever a catastrophic error condition prevents normal microprogram termination of the sequence (Check 1 Error).
- Disconnect In is raised by the CU only when it is connected to the channel (that is, Operational In is up). During a polling sequence, the CU will ensure that the sequence has progressed at least to the point where Address In is up before raising Disconnect In.
- The channel, in response to Disconnect In, performs a selective reset. Disconnect In does not fall after the fall of Operational In.
- The channel indicates the occurrence of Disconnect In, to the program, by causing an I/O interruption. The interface control check bit is set in the stored CSW.

Metering In

- Signals the channel that the customer meter in the CU is recording time.
- Causes the CPU customer meter to record time regardless of the CPU state.

Clock Out

- Indicates when a CU is allowed to change from Enabled to Disabled or vice versa.
- Indicates that the CPU is in a halt or wait state.

Metering Out

- Indicates to CU that the CPU customer meter is recording processing time.
- Causes all enabled CU meters to record time.

JUMPER CARD ASSIGNMENTS

Certain jumper cards in the CU have to be jumpered to match customer device addresses and CU options.

See INST 20 for location of these cards and jumper positions.

CHANNEL INTERFACE General Information (Part 1 of 6)

INTERFACE SEQUENCES

Initial Selection Sequence—CHL-I 300

The channel places the address of the desired I/O device on bus out and raises Address Out. Each CU connected to the channel attempts to decode the address on the bus.

The channel issues Select Out; when the incoming Select Out appears at the addressed CU, the CU blocks its propagation and, if not busy, raises Operational In. When Operational In rises, the channel responds by dropping Address Out. After Address Out falls and the I/O device address is on bus in, Address In rises.

After the channel checks the address, it responds by placing the command on bus out and raising Command Out. The selected CU processes the command and drops Address In which allows Command Out to fall. After Command Out drops, the CU places the status information on bus in and raises Status In.

If the channel accepts this status condition, it responds with Service Out. Service Out allows Status In to fall, completing the initial selection sequence. A Command Out response from the channel also allows Status In to fall. See Stack Status.

If, during this channel-initiated selection sequence, the I/O device is operating, the CU presents busy status. When the CU has status information for the addressed device, outstanding from a previous operation or an externally initiated status condition, it presents the busy status (except to Test I/O) along with the other status conditions in the status byte. See Unit Status Conditions.

If, for example, the command is rejected by the CU as a result of the detection of an invalid command, the CU presents unit-check status condition. No operation is initiated at the CU and no ending status is generated.

An immediate-type command or command-immediate is a command whose execution meets the following requirements:

1. Execution requires no more information than that in the command byte; that is, no data or information bytes are transferred.
2. Channel-end time coincides with initial-status time; and on a normal operation, at least Channel End instead of zero status will be in the initial status byte.

Note: A channel response of Command Out to Status In cannot prevent the execution of an immediate command.

Control Unit Busy Sequence—CHL-I 350

If an I/O device is addressed and the CU to which it is attached is busy or has status pending for an I/O device other than the one addressed, the CU responds to Select Out from the channel with Status In. The status byte indicates the Busy condition. See Busy under Status Byte. Operational In is not raised.

Note: The Control Unit Busy sequence is not used in response to an initial selection sequence addressed to a device for which chaining has just been indicated.

After accepting the status byte, the channel drops Select Out. The CU responds by dropping Status In and disconnecting from the interface. The channel must keep Address Out up until Status In drops, thus completing the Control Unit Busy sequence.

Block-Multiplex Mode—CMD 200

In block-multiplex mode, during the wait periods associated with long non data-transfer operations encountered in command chaining operations, a selector channel can disconnect from the device and initiate an I/O operation on another device. For this reason, block-multiplexing is sometimes called disconnected command chaining.

Block-multiplexing occurs in I/O operations when a selector channel in block-multiplex mode is performing a command chaining operation. When the CU presents Channel End but Device End has not yet been received (Seek or Set Sector), block-multiplexing permits the I/O device to drop offline until it is ready to signal Device End. While the device is offline, another I/O instruction can be initiated on another device attached to the same channel. In this way, a command-chaining selector channel in block-multiplexing mode functions similar to a multiplex channel.

Control-Unit-Initiated Sequence—CHL-I 300

When any CU requires service, it raises Request In to the Channel. The next time Select Out rises at any CU requiring service and no I/O selection is being attempted by the channel (Address Out down), the CU places the address of the I/O device on bus in and signals both Address In and Operational In. When the channel recognizes the address, Command Out is sent to the CU, indicating proceed. After Address In drops, the channel responds by dropping Command Out. After Command Out drops, the CU places the status information on bus in and raises Status In.

Data Transfer — CHL-I 360, 380

Two modes of data transfer are used in the 3830-2:

STANDARD 370 MODE: In the standard 370 mode, data transfer is requested by the CU after a selection sequence. To transmit data to the channel, the CU places a data byte on bus in and raises Data In; the tag and the validity of bus in is maintained until an outbound tag is raised.

To request data from the channel, Data In is raised, and the channel places the data on bus out and signals with Data Out. The channel maintains the validity of bus out until Data In faills. After Data In falls, the channel responds by dropping Data Out.

After selection, the CU remains connected to the channel for the duration of the transfer of information. The information can be a single byte of data, a status report, an initiation of a new command, a string of data bytes, or a complete operation from initiation to reception of the final status.

During data transfer, Service In and Data In are alternated, always starting with Data In. Service Out is always the response to Service In and Data Out is always the response to Data In.

The duration of the connection is under control of both the channel and the CU. To provide the channel with a method of controlling the duration of the connection, the CU cannot disconnect from the interface before Select Out (hold out) falls. However, the CU may preserve the logical connection after the channel permits the control unit to disconnect—Select Out (hold otu) down—by holding up Operational In.

OFFSET INTERLOCK MODE: Offset Interlock mode is active during file data transfers only. The CU raises Data In. When Data Out is detected the CU will drop Data In and raise Service In.

If Data Out is not detected within 700 ns from the rise of Data In (file requires service) the CU will drop Data In and raise Service In. The delayed detection of the response tag, Data Out will be accepted by the CU.

The same sequence will occur for the Service Out response to Service In.

Ending Procedure and Asynchronous Status—CHL-I 400

The ending procedure may be initiated by either the I/O device or the channel. If the procedure is initiated by the I/O device, the end of operation is completed in one signal sequence, assuming that both Channel End and Device End status conditions occur together. If the procedure is initiated by the channel, the I/O device may still require time to reach the point where the proper status information is available, in which case a second signal sequence is necessary to complete the ending procedure.

One of three situations may exist at the initiation of the ending procedure (assume selection is already obtained):

1. The channel recognizes the end of an operation before the I/O device reaches its ending point. In this situation, the CU requires service again, the CU raises Service In or Data In. The channel responds with Command Out, indicating stop. The CU drops Service In or Data In and proceeds to its normal ending point without requesting further service. The channel then drops Command Out. When the I/O device reaches the point where it normally would send Channel End, the CU places the ending status on bus in and raises Status In. The channel responds with Service Out, unless it is necessary to stack the status condition in which case the channel responds with Command Out.
2. The channel and the I/O device recognize the end of an operation simultaneously.
3. The I/O device recognizes the end of an operation before the channel reaches the end of an operation.

For situations 2 and 3, status information is available at the CU. The CU places the ending status on bus in and raises Status In.

If Device End does not occur with Channel End, Device End is presented, when it is available, and an additional status sequence is required.

Some status conditions are unrelated to any previous program-initiated command. One of these conditions is Device End, which is generated whenever the corresponding device goes from the not-ready to the ready state. These status conditions are handled in the same way as any other status information and are subject to the same rules as far as presentation to the channel and stacking are concerned.

CHANNEL INTERFACE General Information (Part 2 of 6)

CHANNEL INTERFACE General Information (Part 2 of 6)

ADDRESSING

An eight-bit address byte (plus parity) is used over the interface for direct addressing of attached I/O devices. A unique eight-bit I/O device address is assigned to each I/O device at the time a CU is installed.

Address Assignment – INST 20

At the time of installation, CU and I/O device addresses are assigned.

Disk storage units are assigned addresses within sets of contiguous numbers. The high-order bit positions of an address within a set identify the CU; the low-order bit positions designate the controller/device on the CU. For control units without the 32 Drive Expansion feature, bits 0, 1, 2, and 3 are the CU address. For control units with 32 Drive Expansion, bits 0, 1, and 2 are the CU address and bit 3 designates controller address 0/1 or 2/3.

Input/output devices accessible through more than one channel in the same system have a distinct address for each path of communications. For sets of devices connected to two or more CUs, the portion of the address identifying the device on each CU is fixed, and does not depend on the path of communications.

Except for the rules described, the assignment of channel and device addresses is arbitrary. The assignment is made at the time of installation and the addresses normally remain fixed thereafter.

Address Decoding – CHL-I 165

CUs recognize an I/O device address that meets the following conditions:

1. The address has correct parity.
2. The address is assigned to the CU.

The CU does not respond to any address outside its assigned set or sets. For example, if a CU is designed to control devices that have only bits '0000' – '0111' in the low-order position of the device address, the CU does not recognize addresses that have '1000' – '1111' in these bit positions.

If no CU responds to an address (Select Out is propagated through all CUs, and back to the channel as Select In), the device appears as nonoperational. Nonoperational may include, in addition to addresses outside an assigned set:

1. An I/O device address not installed.
2. An I/O device address partitioned out of the system by the program, operator, or customer engineer (offline, disabled, etc.).

The CU must respond to those addresses in the set which are:

1. Ready.
2. Not ready, but can be made ready by manual intervention. A device not-ready status is indicated by the Unit Check status and Intervention Required sense indicator.

The CU may respond to all addresses in the assigned set, regardless of whether the device associated with the address is installed. If a CU responds to an address for which no device is installed, the Unit Check status indicator must be turned on (as well as the appropriate sense indicator(s)).

The portion of the address decoder which identifies the CU can be set at the time of installation for any bit combination.

COMMANDS – CHL-I 165

When Command Out is up, the information on bus out is the command byte. A channel issues Command Out to initiate continue, or terminate an operation in an I/O device.

Command Byte – CMD 2

The command byte requires decoding by the CU only during a channel initiated selection sequence (when the channel addresses the I/O device). At all other times, the byte is zero (parity is immaterial). The low-order bit positions indicate the type of operation; the high-order bit positions indicate a modification code which expands the basic operation at the CU or I/O device level.

The actual modifier codes and the particular modes set or the controls performed for them are specified in CMD section.

The command byte on the interface is defined as follows:

	BIT POSITION							
	P	0	1	2	3	4	5	6	7
Test I/O*	1	0	0	0	0	0	0	0	0
Sense	P	M	M	M	M	0	1	0	0
Write	P	M	M	M	M	M	M	0	1
Read	P	M	M	M	M	M	M	1	0
Control	P	M	M	M	M	M	M	1	1

M Modifier bit
P Parity bit

*Although test I/O may be a CPU instruction, it appears over the interface as a command.

Sense, Read, and Control commands with all-zero modifier bits are decoded on all I/O devices as follows:

	BIT POSITION							
	P	0	1	2	3	4	5	6	7
Test I/O	1	0	0	0	0	0	0	0	0
Basic Write	0	0	0	0	0	0	0	0	1
Basic Read**	0	0	0	0	0	0	0	1	0
Control (No-Op)	1	0	0	0	0	0	0	1	1
Basic Sense	0	0	0	0	0	0	1	0	0

**Used for initial program load (IPL) operations.

BASIC OPERATIONS – CMD 2

The I/O operation to be executed over the interface is determined by the eight-bit coded command issued to the I/O device during a channel initiated selection sequence.

The low-order bit positions of this command byte specify the type of operation.

The high-order bit positions (modifier bits) expand the interpretation of the basic operation at the CU or I/O device level.

Note: The basic operations are expressed by the commands: Read, Write, Control, Sense and Test I/O. Test I/O is treated as a command on the I/O interface, although it may originate as either a CPU instruction or a channel-initiated sequence for the purpose of clearing or stacking interruption conditions.

A command with invalid parity is not recognizable and therefore not executable.

Note: Special diagnostic commands which permit errors to occur on the interface or introduce the possibility that subsequent commands may be executed erroneously, must be interlocked in such a fashion as to prevent inadvertent use of them.

Read – CHL-I 360

The Read command initiates execution of data transfer from the CU to the channel and the data is obtained, for example, from the record source of the particular I/O device in operation.

A Read command, with all modifiers set to zero, is an initial program loading (IPL) Read command. This command, if executed on an I/O device after a system reset, performs an IPL read.

Write – CHL-I 380

The sequence of signals over the I/O interface to perform a Write operation is the same as for a Read operation. For a Write operation, however, the data is sent from the channel to the CU for recording by the selected I/O device.

Control – CHL-I 380

The Control operation proceeds similarly as in a Write operation, except that the command modifier bits received by the CU are decoded to determine which of several possible functions is to be performed. The function may require several bytes of data to complete the Control operation. When the particular control function can be completed without involving the transfer of data, the Channel End status may be presented during the initial selection sequence.

The timing in the CU for the bytes transferred during a Control operation is normally such that the byte rate for this operation is no faster than the normal read or write rate for the same I/O device.

A Control command with all-zero modifiers performs no operation at the I/O device, except to satisfy any previously indicated chaining operations and to allow certain I/O devices to wait for conditions of checking (or any synchronizing indications) before releasing the channel. This variation of the Control command is a No-Operation control.

Sense – CHL-I 360

The Sense command proceeds exactly as a Read command, except that the data is obtained from sense indicators rather than from a record source.

The purpose of the Sense command is to extract information that concerns unusual conditions detected during the last operation and the actual state of the device.

The basic Sense command (modifier bits set to zero) initiates a Sense operation on all I/O devices. The basic Sense command must not initiate any operation other than to sense the sense indicators. The basic Sense command to an available CU must be accepted even though the addressed I/O device is in a not-ready state (mechanically unable to execute other operations). If the control unit detects an error during the sense operation, Unit Check is sent with the Channel End status condition.

Test I/O—CHL-I 420

The Test I/O command relieves the addressed I/O device path of pending status information. If no pending status information is encountered along the I/O path being tested, a zero status byte for the selected I/O device is sent to the channel for processing. If status information is available, pending status bits for the selected I/O device are transmitted to the channel.

The busy condition is defined differently with respect to Test I/O than for other commands.

The signal sequence to accomplish Test I/O is the same as any other channel initiated selection process, except that no operation is initiated.

SEQUENCE CONTROLS—CHL-I 350

The sequence controls described in this section are determined by the sequence of the signals over the interface.

Proceed — CHL-I 350

Whenever Command Out responds to Address In on a control unit initiated selection sequence, it means proceed.

Proceed indicates to the I/O device to continue the normal servicing sequences on the interface.

Stop (Also referred to as truncate) — CHL-I 350

Stop is indicated by Command Out in response to Service In, Data In, or as a result of an interface disconnect, which occurs before the normal Channel End for the operation in process. See Interface Disconnect.

Stop is used to signal the I/O device that the channel is ending the current operation. On receipt of the Stop signal, the I/O device proceeds to its normal ending point without sending any further Service In or Date In signals to the channel. In the Offset Interlock mode one additional Service In or Data In tag may be raised due to delayed detection of Command Out. The I/O device remains busy until the ending status is available, presented to, and accpeted by the channel.

Stack Status — CHL-I 350

Stack Status is indicated by a Command Out response to Status In.

The Stack Status signal causes retention of status information at the CU until that status is accepted on a subsequent status cycle with a Service Out. When Stack Status occurs, the CU disconnects from the interface after Select Out is down. Command Out remains up until Operational In falls. An attempt by the CU to initiate a selection sequence to present the status again is under control of Suppress Out. See Suppress Status. Command Out is not signaled to a zero status byte that has been provided in response to a command other than Test I/O.

Note: Rather than delay completion of an interface sequence, the channel will either stack or accept status.

Accept Data — CHL-I 350

Raising Service Out in response to Service In or Data Out in response to Data In during a Read or Sense operation indicates that the information placed on bus in has been accepted by the channel.

Data Ready — CHL-I 350

Raising Service Out in response to Service In or Data Out in response to Data In during a Write or Control operation indicates that the requested information has been placed on bus out and is ready for acceptance by the CU.

Suppress Status — CHL-I 350

Whenever the channel is unable to immediately handle interruption causing status conditions, Suppress Out may be raised. With this line up, the CU must not attempt to initiate a selection sequence to present suppressible type status information. Status is suppressible if Stack Status is received. Status that contains Channel End is not suppressible until stacked, except when Interface Disconnect is received for that address. Status that contains Device End is not suppressible, when chaining has been indicated, until it is stacked. Other asynchronous status may be suppressible at the option of the CU without being stacked.

Suppress Out must be up at least 250 nanoseconds before Select Out rises at the CU if suppression of status is to be ensured. Suppress Out suppresses only the initiation of the selection of the interface by the CU. If Suppress Out rises after a status sequence has been started, the status sequence will proceed normally.

Accept Status — CHL-I 350

Raising Service Out is response to Status In indicates that the status placed on bus in has been accepted by the channel.

Command Chaining — CHL-I 350

Command Chaining is indicated if Suppress Out is up when Service Out is raised in response to Status In. Command Chaining means that another command for the I/O device in operation will immediately follow the presentation of Device End, provided no unusual conditions were encountered during the execution of the current operation. The exact time at which the next command is presented depends on the channel.

When command chaining is indicated at the time Device End is presented, this indication will be valid until reselection is made or until Suppress Out falls.

Reselection of any I/O device attached to the CU will reset the chained command condition in the CU. Status conditions such as Unit Check, Unit Exception, or Control Unit End, will terminate command chaining in the channel.

If chaining is indicated when Device End is presented, the CU must ensure that the path to the device remains available until the chaining operation is initiated or until chaining is no longer indicated.

If chaining is indicated on an I/O device shared between more than one CU or channel, the I/O device must remain available until the chaining operation is intiated or until chaining is no longer indicated.

To ensure recognition of Command Chaining by the CU, Suppress Out must be up at least 250 nanoseconds before Service Out rises in response to Status In and must not fall before Status In. If command chaining is not to be indicated, Suppress Out must be down at least 250 nanoseconds before the rise of Service Out and must not rise before the fall of Status In.

Interface Disconnect (Also referred to as Halt I/O.) — CHL-I 350

The CU will recognize Interface Disconnect when Address Out is up and Select Out (Hold Out) is down at least 250 nanoseconds before the completion of any signal sequence. In this case, Address Out may be up concurrently with another out tag.

When Operational In drops, the channel may drop Address Out to complete the interface disconnect sequence. Address Out must be down for at least 250 nanoseconds before a new channel initiated selection sequence may be attempted.

The CU responds to the Interface Disconnect by removing all signals (with the possible exception of Request In and Metering In) from the interface. On an input operation, data on bus in need not be valid after the rise of Address Out. On an output operation, data on bus out must be valid until the fall of either Service In, Data In, or Operational In. When the CU reaches the normal ending point, it attempts to obtain selection on the interface to present and generated status to the channel.

Any abnormal device operation should be indicated by Unit Check in the status, and the sense information should provide additional details concerning the operation. See Unit Check. The CU will not generate any status as a result of the Interface Disconnect if the interface disconnect sequence is performed before initial status is accepted, or after Device End status for an operation that has been accepted by the channel.

The I/O device path will remain busy after it receives an Interface Disconnect, while performing an operation, until the Device End status is accepted by the channel. If Interface Disconnect is received when the I/O device is not busy, no status is generated nor is the I/O device made busy.

Note: If Address Out is up concurrently with another out tag, the information on bus out must remain valid until the associated in tag drops or until Operational In drops.

Disconnect In — CHL-I 300

The Disconnect In line is used by the CU whenever a catastrophic error condition occurs which prevents a normal microprogram termination of the sequence. Under certain error conditionns, when the CU is unable to complete an I/O interface sequence properly, the CU hardware interrupts the channel by using the Disconnect In line.

Disconnect In is raised by a CU only when it is connected to the channel; that is, it has Operational In up. If a catastrophic error condition occurs when the CU is not connected to the channel, the hardware generates a polling sequence and raises Disconnect In after the following channel seuqence has proceeded to the point of raising Command Out.

The channel, in response to Disconnect In, performs a selective reset. Disconnect In and Operational In will be maintained until the initiation of selective reset.

After a selective reset is issued, the CU sets up to signal unit check on the next channel initiated selection sequence. Sense information indicates equipment check.

An interface disconnect sequence will not clear Disconnect In.

CHANNEL INTERFACE General Information (Part 4 of 6)

Selective Reset—CHL-I 350

Selective Reset is indicated whenever Suppress Out is up and Operational Out drops. This condition causes Operational In to fall, and the particular I/O device in operation and its status to be reset. The operation in process will proceed to a normal stopping point, if applicable, with no further data transfer. The I/O device operating over the interface is the only device that is reset, even on multi-device control units. The particular I/O device path will be in a busy state throughout this procedure.

Device End may be returned after the reset. To be effective, Suppress Out must rise at least 250 nanoseconds before Operational Out drops and must remain up until at least 250 nanoseconds after Operational Out rises. Operational Out must stay down until Operational In falls or for at least 6 microseconds, whichever is greater, for the selective reset to be effective. The ready or not-ready state of the CU is not changed by a selective reset.

Selective Reset is issued only as a result of a malfunction detected at the channel or a time out by the channel.

System Reset—CHL-I 350

System Reset is indicated whenever Operational Out and Suppress Out are down concurrently, and the I/O device is in the online mode. This condition causes Operational In to fall, and all CUs and their attached I/O devices, along with their status, to be reset. The CUs will be in a busy state for the duration of their reset procedure. System Reset prepares an I/O device for an initial program loading sequence (IPL).

System Reset is performed when the System Reset key is pressed, when the power for the system is turned on, when the channel is offline to the I/O interface, and as a part of the IPLing procedure. The ready state of the CU is not changed by a System Reset.

To ensure a proper reset, Operational Out and Suppress Out must be down concurrently for at least 6 microseconds.

STATUS INFORMATION—CHL-I 420, CMD 180

When Status In is up, the information that appears on bus in is the status byte. The conditions reported in the status byte are the status conditions.

The status pertains to the device or implied CU whose address appeared on bus in (with Address In) during the polling or selection portion of the sequence. In the case of the Control Unit Busy sequence when no Address In occurs, it is assumed that the status pertains to the addressed device or implied CU.

Note: Unless stated otherwise, this information pertains to CUs attached to only one channel interface.

Status Byte—CHL-I 420

The status byte has the following format:

BIT POSITION	DESIGNATION
P	Parity
0	Attention (not used)
1	Status Modifier
2	Control Unit End
3	Busy
4	Channel End
5	Device End
6	Unit Check
7	Unit Exception

The status byte is transmitted to the channel in each of six situations:

1. During the Initial Selection sequence.
2. To present the Channel End status at the termination of data transfer.
3. To present the Device End signal and any associated conditions to the channel. The I/O device remains busy during an operation until the channel accepts the Device End status.
4. To present Control Unit End or Device End status which signals that the CU or device that was previously busy and then interrogated, is now free.
5. To present any previously stacked status when allowed to do so.
6. To present any externally initiated status to the channel (Attention and Device End because of not-ready-to-ready transition).

Once accepted by the channel, any given status byte is reset and is not presented again.

Unit Status Conditions—CHL-I 420

The following status conditions are detected by the I/O device or CU and are indicated to the channel over the I/O interface:

When the device is accessible from more than one channel, status resulting from channel-initiated operations is signaled to the initiating channel.

Attention (Not Used)

Status Modifier—CHL-I 420

Status Modifier is used by CUs in three situations:

1. Busy CUs present the status modifier bit with the busy bit during the initial selection procedure to differentiate a busy CU from a busy device.
2. When CUs recognize special ending conditions (Search Equal) they present the status modifier bit with Device End, when the special condition occurs.
3. This bit set in combination with the Unit Check bit indicates that an unusual condition has occurred with the last operation calling for a retry of the last channel command.

In the first case, provision is made for indicating that a busy condition pertains to a CU and not necessarily to the addressed I/O device. This condition occurs when the CU is required to perform a function that does not involve the I/O interface. The condition may also occur when the CU has status pending for an I/O device other than the one addressed.

In the second case, provision is made for CUs to recognize special ending or synchronizing conditions. If the special condition occurs, the Status Modifier bit with the Device End bit is presented during the Device End status cycle. Presence of Status Modifier and Device End indicates that the normal sequence of commands must be modified.

Control Unit End—CHL-I 420

The Control Unit End condition is provided only by channel shared CUs or CUs shared by I/O devices, and only when the following condition occurs:

The CU was interrogated while it was in the busy state. Interrogated in the busy state means that a previous Channel Initiated Selection sequence was issued to a device on the CU and the CU responded with Busy and Status Modifier in the unit status byte. See Status Modifier.

The I/O device address associated with Control Unit End is determined as follows:

1. If Control Unit End is presented during a Control Unit Initiated Selection sequence, the I/O device to be used when presenting this status is allowed to be any legitimate address associated with the CU. (A legitimate address is any address the CU is capable of recognizing, regardless of whether or not the I/O device is actually attached.)
2. If Control Unit End is to be presented during a Channel Initiated Selection sequence, the I/O device address will be the same as the address issued with Address Out.

Busy—CHL 420

Busy can occur only during a Channel Initiated Selection sequence and indicates that the I/O device or CU cannot execute the command because a previously initiated operation is being executed or because status conditions exist (or in the case of switched control units, because the path is unavailable). An operation is being executed from the time initial status is accepted until Device End is accepted. Status conditions for the addressed I/O device, if any, accompany the busy indication.

If the busy condition applies to a CU function, Busy is accompanied by Status Modifier.

Busy is indicated to test I/O only if a previously initiated operation is still being executed and no end status is available.

The busy condition causes command chaining to be suppressed.

CHANNEL INTERFACE General Information (Part 5 of 6)

STATUS INFORMATION (continued)

Channel End—CHL-I 420

Channel End is caused by the completion of the portion of an I/O operation involving transfer, if any, of data or control information between the I/O device and the channel.

Each I/O operation causes only one Channel End signal to be generated. The Channel End condition is not generated unless the command is accepted (status byte contains either all zeros or Channel End and not Busy). The exact time during an I/O operation when Channel End is generated depends on the operation. For operations such as writing, the Channel End condition is generated when the block has been written or padding is complete on a truncated operation.

During control operations, Channel End is usually generated after the control information is transferred to the CU; although for short operations, the Channel End may be delayed until completion of the operation. Operations that do not cause data to be transferred can provide the Channel End condition during the Initial Selection sequence.

Device End—CHL-I 420

Device End is caused by the completion of an I/O operation at the I/O device or, by manually changing the device from the not-ready to the ready state. The Device End condition normally indicates that the I/O device has completed the current operation.

Each I/O operation causes only one Device End condition. The Device End condition is not generated unless the command is accepted.

The Device End condition associated with an I/O operation is generated either simultaneously with the Channel End condition or later. In the case of data transfer operations, the device terminates the operation at the time Channel End is generated, and both Device End and Channel End occur together. For control operations, Device End is generated at the completion of the operation at the device. The operation may be completed at the time Channel End is generated or later.

When command chaining occurs, only the Device End of the last operation of the chain is normally made available to the program. When the Device End signal is received in the absence of any unusual conditions, it causes the channel to initiate a new I/O operation. If an unusual condition is detected during the initiation of a chained command, the chain is terminated without Device End.

An I/O device shared between more than one channel path, and which has a Device End generated because of the device going from a not-ready to a ready state, must present a Device End to all attached channels if the multitag switch is in the multitag position. If the switch is off, the Device End is accepted by only one channel.

If a device is addressed while in a busy state, a Device End must be signaled to the path that initiates the command when the I/O device becomes not busy.

Note: Not ready means that an I/O device requires operator intervention to become operational.

Unit Check — CHL-I 420

Unit Check indicates that the I/O device or control unit has detected an unusual condition that is detailed by the information available to a sense command. Unit Check may indicate that a programming or an equipment error has been detected, that the not-ready state of the device has affected the execution of the command or instruction, or that an exceptional condition other than the one identified by Unit Exception has occurred. The Unit Check bit provides a summary indication of the conditions identified by sense data.

Unit Check is indicated when the existence of the not-ready state precludes a satisfactory execution of the command, or when the command, by its nature, tests the state of the device. When no interruption condition is pending for the addressed device at the CU, the CU signals Unit Check when Test I/O or the No Operation control command is issued to a not-ready device. In the case of No Operation, the command is rejected and Channel End and Device End do not accompany Unit Check.

Unless the command is designed to cause Unit Check, Unit Check is not indicated if the command is properly executed even though the device has become not-ready during, or as a result of, the operation. Similarly, Unit Check is not indicated if the command can be executed with the device not-ready.

Selection of a device in the not-ready state does not cause a Unit Check indication when the sense command is issued, and whenever an interruption condition is pending for the addressed device at the CU.

If, during the initiation sequence, the device detects that the command cannot be executed, Unit Check is presented to the channel and it appears without Channel End, Control Unit End, or Device End. Such unit status indicates that no action has been taken at the device in response to the command.

If the condition that precludes proper execution of the operation occurs after execution has been started, Unit Check is accompanied by Channel End, Control Unit End, or Device End, depending on when the condition was detected. Errors detected after Device End is cleared may be indicated by signaling Unit Check with Control Unit End.

When Unit Check appears with Channel End and without Device End, a shared control unit must preserve the sense data and an available device path until after the Device End is accepted.

Errors, such as invalid command code or invalid command code parity, do not cause Unit Check when the device is working or contains a pending interruption condition at the time of selection. Under these circumstances, the device responds by providing the busy bit and indicating the pending interruption condition, if any. The command code validity is not indicated.

Termination of an operation with the Unit Check indication causes command chaining to be suppressed.

Unit Check without Channel End, Device End, or Control Unit End is presented when ECC correctable errors are encountered in the data field.

PROGRAMMING NOTE

If a device becomes not-ready on completion of a command, the ending interruption condition can be cleared by Test I/O without generation of Unit Check because of the not-ready state. Any subsequent Test I/O issued to the device causes a Unit Check indication.

Unit Exception—CHL-I 420

Unit Exception means that the I/O device detected an unusual condition such as end of file. Unit Exception has only one meaning for any particular command. A sense operation is not required as a response to the acceptance of a Unit Exception condition.

A Unit Exception condition can be generated only when the I/O device is executing an I/O operation, or when the device is involved with some activity associated with an I/O operation and the condition is of immediate significance. If a device detects a Unit Exception condition during the Initial Selection sequence, Unit Exception is presented to the channel and it appears without Channel End, Control Unit End, or Device End.

Such unit status indicates that no action has been taken at the device in response to the command. If the condition that precludes normal execution of the operation occurs after the execution is started, Unit Exception is accompanied by Channel End, Control Unit End, or Device End, depending on when the condition is detected. Any unusual condition associated with an operation, but detected after Device End is cleared and is indicated by signaling Unit Exception.

The Unit Exception causes command chaining to be suppressed.

SENSE INFORMATION—SENSE 10

Data transfer during a sense operation provides information concerning unusual conditions detected in the last operation and concerning the actual state of the I/O device. Information provided by the basic sense operation is more detailed than that supplied by the Unit Status byte, and may describe reasons for the Unit Check indication. It may also indicate, for example, that the I/O device is in the not-ready state.

All sense information significant to the use of the I/O device normally is provided in the first two bytes. Any bit positions that follow those used for programming information contain diagnostic information, which extends to 24 bytes.

The sense information that pertains to the last I/O operation or other unit action may be reset by the next command addressed to the CU, provided the busy bit is not included in the Initial Selection status byte, except where the command is a basic Sense, Test I/O or No-Op and it is addressed to the device that causes the Sense. The sense information may also be changed as a result of asynchronous actions such as when not-ready-to-ready Device End status is generated.

A command code with invalid parity will cause the sense information to be replaced only if Unit Check is turned on as a result of the invalid parity.

Intervention Required

Intervention Required is generated when the last operation could not be executed because of a condition that requires intervention at the I/O device. Intervention Required is also turned on when the addressed device is in the not-ready state, is in test mode, or is not provided on the CU.

CHANNEL INTERFACE General Information (Part 6 of 6)

Bus Out Check – CHL-I 30

Bus Out Check results when the I/O device or the CU receives a data byte or a command byte with invalid parity over the I/O interface.

During writing, Bus Out Check indicates that a parity error was detected and incorrect data may have been recorded at the I/O device. However, the condition does not cause the operation to be terminated prematurely, unless the operation is such that an error precludes meaningful continuation of the operation.

Sense Byte

The first six bits of the first sense data byte (sense byte 0) are common. The six bits are independent of each other and are designated as follows:

BIT	DESCRIPTION
0	Command reject
1	Intervention required
2	Bus Out check
3	Equipment check
4	Data check
5	Overrun
6	(see device MLM)
7	(see device MLM)

For additional sense information see Sense section.

SENSE CONDITIONS

Command Reject

The device detected a programming error. A command was received which the device is not designed to execute (Read Backward issued to a direct-access storage device), or which the device cannot execute because of its present state (a Write issued to a file-protected unit). In the former case, the program may have specified invalid control data. Command Reject is also indicated when an invalid sequence of commands is recognized (Write to a direct-access storage device without previously designating the data block). Command Reject is also indicated when the Unconditional Reserve command is issued to a 3350 that is operating in 3330-1 compatibility mode.

No operation is initiated if the command code has a parity error.

Equipment Check

The Equipment Check sense bit indicates detection of an equipment malfunction logically between the I/O interface and the input/output medium. On the output operations, this malfunction may have caused invalid data to be recorded. Detection of Equipment Check stops data transmission and terminates the operation prematurely when the error prevents any meaningful continuation of the operation.

Data Check

Data Check indicates that invalid data has been detected or is probable on the recording medium. This invalidity can be accurately detected only by reading the recording medium.

The CU forces correct parity on data sent to the channel. On writing, the Data Check condition indicates that incorrect data may have been recorded at the I/O device. Data errors on reading and writing cause the operation to be terminated prematurely only when the errors prevent meaningful continuation of the operation (loss of synchronization).

Overrun

Overrun results when the channel fails to respond on time to a request for service from the I/O device. Overrun can occur when data is transferred to or from a CU that operates with a moving medium, and the total activity initiated by the program exceeds the capability of the channel.

On an output operation, Overrun indicates that data recorded at the device may be invalid. In these cases, data overrun normally stops data transfer and the operation terminates as in Stop. The overrun bit is also turned on when the device receives the new command too late during command chaining.

For additional sense information see Sense section.

CHANNEL DATA TRANSFER CONTROLS Description (Part 1 of 3)

CHANNEL TRANSFER CONTROLS

Channel Buffers A and B (CHL-I 155)

Two buffers are used to provide asynchronous data transfer between control unit (CU) and channel.

During initial selection, ending sequence, and status presentation, Channel Buffer-A is used for incoming data (Address Out/Command Out) and Channel Buffer-B is used for outgoing data (Address In/Status In).

During read/write operations, Channel Buffer-A is controlled by Data In/Data Out and Channel Buffer-B is controlled by Service In/Service Out.

Data transfer can be synchronized to the CU independent of the channel, since at least one buffer is always available to either the microprogram or the channel.

Transfer Latches A and B (CHL-I 35, 140, 145)

The transfer latches, when on, indicate that a transfer to or from the respective buffer is required. When on, they block Data In/ Service In. Transfer-A latch is controlled by Data Out and Transfer-B latch is controlled by Service Out.

Channel Response Latch (without Offset) (CHL-I 35)

This latch controls the Data In/Service In alternating sequence and the gating of Buffer-A/Buffer-B to Bus In during read. It is set by Data Out and reset by Service Out.

Offset Latch (CHL-I 375, 395)

This latch controls the Data In/Service In alternating sequence and the gating of Buffer-A/Buffer-B to Bus In during read. It is set by Data Out and reset by Service Out.

Microprogram Response Flip Flop (FF) (CHL-I 35)

This latch controls the transfer of data to or from Buffer-A/ Buffer-B. It is complemented during read by the microprogram transfer into the MD register (CD of MD) or during write by the microprogram transfer from the NA register (CA of NA) thus indicating that a byte transfer has been completed by the microprogram.

CONTROL UNIT INTERFACE TO CHANNEL BUFFER CONTROLS

TB Register Bit 7 – Allow NA Load

When on, this bit allows data transfer to the NA register.

TC Register Bits 0 and 1 (CHL-I 35)

TC Bit		Decode
0	1	
0	0	Reset
0	1	Read
1	0	Write
1	1	Freeze

Freeze prevents the change of microprog resp FF, BFRDY, and shutdown cycle.

TC Register Bit 2 – Last Byte Request (CHL-I 35)

This bit is used during write, when the microprogram requests a single byte transfer or the last byte. This bit is set by the microprogram, causing the hardware to transfer one more byte to the CU and stop.

TC Register Bit 3 – Enable Operational In

This bit enables Op In, which interlocks the CU with the channel and enables channel interface controls.

TC Register Bit 4 – Enable Address In

This bit enables Address In which is used by the control unit to signify that it has placed its address on bus in. In addition, Status In causes a control unit busy sequence to be executed if a channel tries to select the CU while it is occupied with another operation.

TC Register Bit 5 – Enable Status In

This bit enables Status In which is used by the control unit to signify that it has placed its status on bus in.

CHANNEL BUFFER CONTROLS TO CONTROL UNIT

XFER Branch – CL 12 (CHL-I 140)

This branch condition is generated by either transfer latch A or B on. It indicates, to the microprogram, that a transfer is required to the MD register on a read, or from the NA register on a write.

The same condition is used to indicate that a Halt I/O sequence has been executed on the selected channel. HLTIO CL 12 raises when TC-0 and TC-1 are both zero. XFER is presented when either TC-0 or TC-1 is set. Both conditions are blocked during a freeze.

BFRDY Branch – CL 14 (CHL-I 145)

This branch condition is generated by both transfer latches A and B being on.

The same condition is used to indicate that CUEND A or CUEND B latch is on if TC-0 and TC-1 are both zero. If TC-0 or TC-1 is set, BFRDY CL12 is raised. During a freeze, (TC-0 and TC-1 both set) both conditions are blocked.

CHANNEL BUFFER CONTROL DURING INITIAL SELECTION AND STATUS PRESENTATION

Data Transfer from Channel (CHL-I 185) (Address Out/Command Out)

When the channel buffer hardware is not in read mode (TC-1), bus out is always sent to Buffer-A. Address Out or Command Out generates a set Buffer-A signal, gates Buffer-A to the NA register, and generates a synchronized set NA register signal.

The set pulses generated by Address Out are reset or blocked by the microprogram setting TC register bit 3 (Enable Op In) or by TB register bit 4 (protect NA).

The set pulses generated by Command Out are reset or blocked by the microprogram setting TB register bit 7 (Allow NA load).

Data Transfer to Channel (CHL-I 165) (Address In/Status In)

When the channel buffer hardware is not in write mode (TC-0), the MD register is always gated to Buffer-B. Address In or Operational In and Status In generate a set Buffer-B signal and gate Buffer-B to bus in.

CHANNEL BUFFER CONTROL OF DATA TRANSFER (WRITE OPERATION) (CHL-I 35)

Initially the Channel Response latch is reset enabling Data In and disabling Service In. The Microprogram Response FF is reset sending Buffer-A to the NA register.

The microprogram sets the data transfer hardware to write mode by setting TC register bit 0 = 1, bit 1 = 0. Data in rises to request the first data byte from the channel.

When the first data byte is available on bus out, the channel responds with Data Out. Data Out sets the Channel Response latch, sets the data on bus out into Buffer-A, and sets the Transfer-A latch. Because the Microprogram Response FF is reset, Buffer-A is gated to the NA register which is set at the next CD time. The Transfer-A latch sets XFER CL12 branch condition indicating to the microprogram that a byte is available in the NA register.

The set of the Channel Response latch drops Data In. Because Data In has dropped, the channel drops Data Out. Because Buffer-B is available (Transfer-B latch reset), Service In is raised to request the second data byte from the channel. When the second data byte is available on bus out, the channel responds with Service Out.

Service Out resets the Channel Response latch, sets the data on bus out into Buffer-B, and sets the Transfer B latch. The Transfer-B latch sets or maintains the XFER CL 12 branch condition. If the Microprogram Response FF is reset the first data byte is still in the NA register. Buffer-B will not be gated to the NA register and Data In will not be raised to request another byte. Service In drops.

Transfer-A and Transfer-B latches both set raise the BFRDY CL14 branch condition indicating to the microprogram that both buffers are full and no further channel transfer is possible.

If the Microprogram Response FF is set, the first data byte has been transferred from the NA register. At the next CD time Buffer-B will be set into the NA register.

Because the Channel Response latch is reset (transfer of data to Buffer-B – Service Out) and the Transfer-A latch is reset (transfer of data from NA register – CA of NA) Data In raises to request the next data byte from the channel.

The microprogram responds to the XFER CL12 branch condition (raised by the Transfer-B latch) by transferring the second data byte from the NA register. The CA decode NA (from the microprogram transfer of the NA register) complements the Microprogram Response FF which alternately resets transfer latches A and B.

Transfer-A latch reset allows Data In to request the next byte from the channel. Similarly, Transfer-B latch allows Service In to request another byte from the channel.

Data In and Service In tags are alternated by the Channel Response latch (Data In when reset, Service In when set). The Microprogram Response FF alternates transferring Buffer-A and Buffer-B into the NA register (Buffer-A when reset and Buffer-B when set).

CHANNEL DATA TRANSFER CONTROLS Description (Part 2 of 3)

Requests for data from the channel (Data In/Service In) are automatic if at least one buffer is empty. If both buffers are full data requests are under control of the microprogram (transfer of NA register - CA of NA). Because the channel data transfers must be faster than the microprogram data transfers to prevent an overrun, at least one byte is always available to the microprogram.

Last Byte Transfer (Write) (CHL-I 35)

Since the hardware automatically requests another byte from the channel for each byte the microprogram transfers from the NA register, the last byte request must be controlled by the microprogram. This is accomplished by setting TC register bit 2 (Last Byte Request) after the microprogram branches on the XFER CL12 branch condition corresponding to the next to the last byte, and before transferring this byte from the NA register.

The Last Byte Request latch is set, preventing the reset of the transfer latches, thus blocking the rise of Data In/ Service In. Two possibilities exist:

1. Only one buffer is loaded when TC register bit 2 is set. (XFER CL12 raised, BFRDY CL14 down). This indicates that the next byte has already been requested. This byte will be the last. When Data Out/Service Out responds, the corresponding transfer latch will be set. Because the previous transfer latch was not allowed to reset, BFRDY CL14 branch condition will rise indicating to the microprogram that the last byte is available in the NA register. No further Data In/Service In requests can be made because both transfer latches are set.

2. Both buffers are loaded when TC register bit 2 is set, (XFER CL12 raised, BFRDY CL14 raised). This indicates that the last byte is already in the buffer. As the Microprogram Response FF is complemented, this byte will be transferred to the NA register. BFRDY CL14 branch condition indicates to the microprogram that the last byte is available in the NA register. No further Data In/Service In requests can be made because both transfer latches are set.

Single Byte Transfer (CHL-I 35)

If the channel writes only one byte, the microprogram raises TC bit 0 (write) and TC bit 2 (single byte). Transfer B latch will be set but the corresponding XFER branch will be blocked. When the channel transfers the byte, Transfer A latch will set, causing a XFER branch. The fact that both transfer latches are now on also causes a BFRDY branch, and the operation will terminate normally.

Shutdown Cycle (CHL-I 35)

A shutdown cycle is defined from the time TC bit 0 is dropped (time FG) and until the Write Mode latch is reset (time CD). During shutdown cycle the transfer counters are compared against each other and sampled. A Transfer Error latch is set if a miscomparison occurs. If the microprogram freezes the hardware (for example, during overrun), the shutdown cycle is suppressed.

Offset Interlock During Write

When the microprogram sets TC0 (channel write mode) Data In will raise. The channel will respond with Data Out which resets Data In and raises Service In. The first data byte is now in the NA register and XFER branch is active, signaling the microprogram that a byte is available for the file.

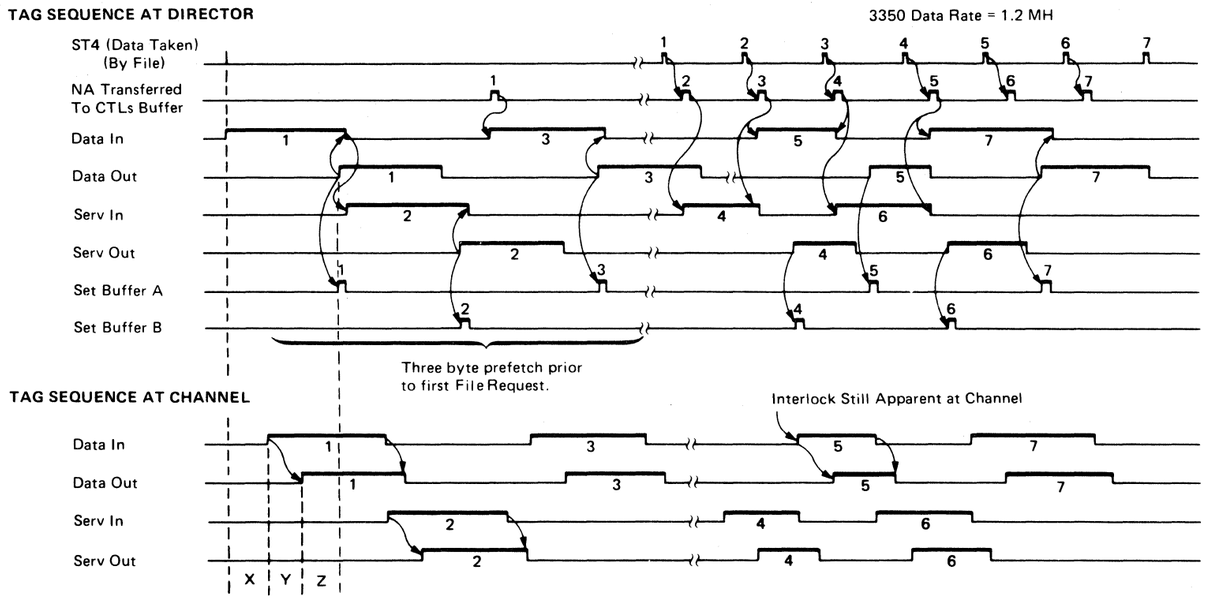
Service In is still active requesting the second data byte. It is reset by either Service Out or a CA/NA signal from the CCU, indicating the first data byte has been transferred from the NA to the TA register.

The CA/NA signal will raise Data In to request the third data byte. Data In is reset by Data Out. Three data bytes are now buffered in the control unit hardware. No further requests are made to the channel until the first Sync In from the controller is detected.

When Sync In is detected, the microprogram signals CA/NA, causing Service In to raise. The next Sync In causes another CA/NA which resets Service In and sets Data In. The In tags now continue to alternate at the frequency of the file data and are not directly interlocked with the Out tags from the channel. The delay of the late responding Out tags is eliminated.

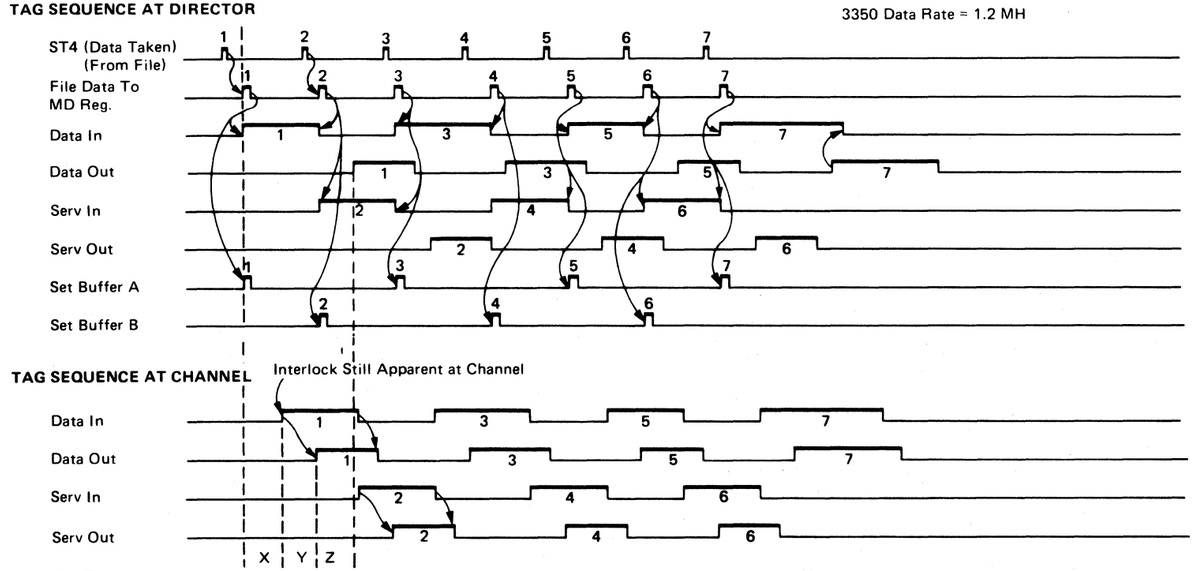
The tags alternate approximately every 830ns. The duration of each in tag is sufficient time for a data byte to be valid on the channel bus out.

OFFSET INTERLOCKING – 7 BYTE WRITE



X = To channel cable delay
Y = Channel delay
Z = From channel cable delay

OFFSET INTERLOCKING – 7 BYTE READ



X = To channel cable delay
Y = Channel delay
Z = From channel cable delay

CHANNEL DATA TRANSFER CONTROLS Description (Part 3 of 3)

CHANNEL BUFFER CONTROL OF DATA TRANSFER (Read Operation) (CHL-I 360)

Initially the Channel Response latch is reset enabling Data In and disabling Service In. The Microprogram Response FF is reset, steering the MD register to buffer A.

The microprogram sets the data transfer hardware to read mode by setting TC register bit 1, which causes both transfer latches A and B to be set. Both Data In and Service In are disabled, and both XFER CL12 and BFRDY CL14 branch conditions are raised, indicating to the microprogram that both buffer A and B are available for data transfer.

The microprogram transfers the first data byte into the MD register. The resulting CD decode MD sets the contents of the MD register into buffer A, sets the Microprogram Response FF, and resets the transfer A latch.

Data In rises, indicating to the channel that the first data byte is available on bus in. The Channel Response latch being reset gates buffer A to bus in.

The XFER CL12 branch condition (Transfer B latch on) causes the microprogram to transfer another data byte into the MD register. The resulting CD decode MD sets the contents of the MD register into buffer B, resets the Microprogram Response FF, and resets Transfer B latch. If the channel has not yet responded to the previous byte, the Channel Response latch is reset, blocking buffer B from bus in and preventing the rise of Service In.

The channel responds alternately to Data In with Data Out, and to Service In with Service Out. Data Out sets the Channel Response latch and the Transfer A latch. Sevice Out resets the Channel Response latch and sets the Transfer B latch.

The Channel Response latch, when set, drops Data In, raises Service In (provided buffer B contains a data byte – Transfer B latch reset), gates Buffer B to bus in, and blocks buffer A from bus in.

The Transfer A latch being set raises XFER CL 12 branch condition, indicating to the microprogram that the next byte can be transferred to the MD register.

The Channel Response latch, when reset, drops Service In, raises Data In (provided buffer A contains a data byte – Transfer A latch reset), gates buffer A to bus in, and blocks buffer B from bus in.

The Transfer A latch being set raises XFER CL12 branch condition, indicating to the microprogram that the next byte can be transferred to the MD register.

The Channel Response latch, when reset, drops Service In, raises Data In (provided buffer A contains a data byte – Transfer A latch reset), gates buffer A to bus in, and blocks buffer B from bus in.

Last Byte Transfer (Read) (CHL-I 35)

For each byte transfer, the channel responds with Data Out/Service Out which sets the corresponding transfer latch. When all bytes have been transferred, both transfer latches will be on, causing a BFRDY CL14 branch condition, indicating to the microprogram that all bytes have been transferred.

ENDING SEQUENCE (Channel Truncation) (CHL-I 35)

Truncation occurs if the channel raises Command Out as a response to Data In/Service In. Since the Channel Response latch remains unchanged, no further data transfers to the channel occur. When the microprogram detects truncation, TC register bits 0 (write) and 1 (read) are reset. The check counters are compensated for any byte transferred by the microprogram which have not been accepted by the channel.

Offset Interlock During Read

The microprogram sets TC1 (channel read mode). Data In and Service remain off. When the first data byte is transferred from the controller, by Sync In, the microprogram sets the byte in the MD register with a CD/MD signal. The CD/MD also sets Data In. The next Sync In causes another CD/MD signal which resets Data In and sets Service In. The In tags continue to alternate as described in the Write operation.

CHANNEL BUFFER CONTROL– ERROR CHECKING–GK505

Error checking is accomplished by using two 3-position module seven counters. They are called counter A and counter B. During a write, counter A counts the number of set pulses to buffer A or buffer B, while counter B counts the number of CA decode NA signals. In effect, counter A monitors channel transfers to the buffers while counter B monitors microprogram transfers from the buffers. During a read, counter B counts sample read parity error pulses corresponding to channel transfers, while counter A counts buffer set pulses corresponding to a microprogram transfer (CD decode MD).

At the end of a Read or Write operation (after the reset of TC-0 or 1), the counters are compared for equality. If they are not equal, the number of data transfers to or from the channel doesn't match the number of data transfers to or from the CU (NA or MD registers).

Shutdown Cycle–GK505

The shutdown cycle is defined from the time TC Bit 1 is dropped and until the Read Mode latch is reset. If a read truncate has occurred, the transfer counter B is stepped twice during the shutdown cycle, before it is sampled.

Read Truncation–GK505

If the channel truncates a read operation, the transfer counters may initially miscompare. The following two cases are illustrative.

a. Microprogram has transferred two bytes to the buffers. If these bytes have not yet been transferred to the channel, the transfer counters differ by two and both transfer latches are reset. Hardware now presents the first byte to the channel, which responds with Command Out; that is, truncates. Since the counters still miscompare by two, counter B (channel response) is updated during the shutdown cycle by stepping it twice.

b. Microprogram has transferred two bytes as above; the counters miscompare by two; and both transfer latches are off. Hardware now presents the first byte to the channel, which acknowledges it with a Data Service Out. The transfer counters now miscompare by one, and one transfer latch is on. The channel then truncates the second byte. Microprogram, however, detects a XFER branch and transfers a third byte to hardware. The transfer counters now miscompare again by two, and both transfer latches are off. At the next byte time, microprogram recognizes the truncate, and the end situation is as in a.

Write Truncation–GK505

If the channel truncates a Write operation, the transfer counters should compare equal since the exact number of bytes transferred from the channel to hardware have been transferred from hardware to microprogram. Microprogram then proceeds to a regular shutdown by resetting TC bit 0.

Other Transfer Errors

A Data Out sequence error is indicated if Transfer A latch or Channel Response latch is on and Data Out "glitches", that is, goes down and again up. **See Note 1.**

A similar Service Out sequence error is indicated if Service Out "glitches" and either Transfer B latch is on or Channel Response latch is off. **See Note 1.**

The Transfer Error latch is set during shutdown cycle if Microprogram Response FF and Channel Response latch miscompare, that is, one is on and the other off.

Data integrity of the channel buffer is maintained by parity checkers.

Write

Data to be transferred to the NA register is checked for correct parity. The parity tree is sampled with the same signal that gates the NA register. If parity is good, buffer bit P is transferred to NA register. If parity is bad, the Buffer Check latch is set, and good parity is regenerated and transferred to the NA register. This avoids an error in the CU, but generates an attachment error (Error 2). Microprogram then recovers from this type of error. If the Buffer Check latch fails to set and bad parity occurs, register NA will be set with bad parity, which will be detected in the CU.

Read

Data to be transferred to bus in is checked for correct parity. The parity tree is sampled with each channel acknowledgment. Since the same acknowledgment also sets the buffer with a new byte, a delayed parity tree output is sampled and used to set the Buffer Check latch.

NOTE 1: If Offset Interlock is installed this error sets Overrun and does not set transfer error.

INITIAL SELECTION (Part 1 of 2)

SEE ALSO CMD 170

OBJECTIVES

1. Channel sends address of requested device to all attached CUs.
2. Each CU, in order of priority, compares its address to the CU address sent by the channel.
3. If addresses compare, the CU sends its address to the channel.
4. Channel checks to ensure address received compares to address sent.
5. If addresses compare, the channel sends a command to the CU.

   If addresses don't compare, channel turns on Interface Control Check.
6. CU accepts command and sends its status to channel.
7. If status is zero, channel responds with Service Out telling CU it is ready for data transfer.

   If status is non-zero channel places status into Channel Status Word (CSW) and notifies CPU program.

INITIAL SELECTION SEQUENCE SIMPLIFIED

Channel	Control Unit
Channel raises Operational Out, Address Out, Hold Out, Select Out, and places address of requested device on bus out.	→ Compare address on bus out with address of CU (CHL-I 30). If no comparison is made, Select In is sent to next lower priority CU. If addresses compare and CU is busy, raise Status In. If addresses compare and CU is not busy, raise Operational In.
Channel recognizes Operational In and drops Address Out.	→ CU recognizes fall of Address Out, places CU and device address on bus in, and raises Address In.
Channel compares address on bus in with requested address sent to CU. If address doesn't compare channel sets Interface Control Check. If address compares, channel places command on bus out and raises Command Out.	→ CU recognizes Command Out, stores command, and drops Address In.
Channel recognizes the fall of Address In and drops Command Out.	→ CU places device status on bus in and raises Status In.
Channel checks for zero status. If non-zero, channel stores status in the Channel Status Word (CSW) in CPU storage, and notifies CPU program. If zero, channel responds with Service Out, telling CU to proceed with data transfer.	

INITIAL SELECTION SEQUENCE DETAIL

Channel	Channel Controls	Control Unit	Microprogram
Raise Operational Out, Address Out, Hold Out, Select Out, and place requested CU address on bus out.	→ Compare CU address to address on bus out. If equal, set CU Selected latch. Set Switched to A or Switched to B latch. If CU busy, (Note 1) respond to channel with Status In. If CU not busy, raise SELTD CL 11 and ADDRO CH 13 branching conditions. Set Channel Buffer B with Address Out and set address to NA register.	→ NA register contains address	→ Microprogram recognizes SELTD CL11 branch condition and sets TC Register bit 3 (Op In) and TC Register bit 4 (Address In) and places device address in MD Register. Microprogram records address from NA register for later use.
	Generate Enable Op In and Raise Operation In to channel. Generate Enable Addr In.	Set TC Register bit 3 (Op In) Set TC Register bit 4 (Addr In). MD register contains device address.	
Channel recognizes Operational In and drops Address Out.	Generate Set Buffer-B and gate unit address from MD register into Channel Buffer-B.		
	Drop Address Out Set CH13 branching condition. Raise Address In to channel.		
	Gate jumpered CU Address with the unit address, from Channel Buffer-B, onto bus in.		
Channel compares address on bus in with the requested address sent to CU to ensure they are the same. Raise Command Out and place command (Read, Write, etc.) on bus out.	→ Generate Set Buffer-A which causes the command on bus out to be loaded into Channel Buffer-A. Command Out gates Channel Buffer-A to the NA register and raises COMMO CH 12 branch condition.	→ NA Register contains command.	→ Microprogram recognizes COMMO CH12, resets TC Reg bit 4 (Addr In), and stores command from NA register in another register.
		Reset TC Register bit 4 (Addr In)	
	Drop Address In to channel.		
Channel recognizes the fall of Address In and drops Command Out.	→ Drop COMMO CH12 branch condition.		→ Microprogram recognizes the fall of COMMO CH12, determines CU status, places status in the MD register, and sets TC Register bit 5 (Status In).
		Set TC Register bit 5 (Status In). MD Register contains CU Status.	
	Gate MD Register into Channel Buffer-B and raise Status In to channel with CU Status on bus in.		
Channel checks for zero status. If non-zero status, channel drops Select Out and Hold Out. If zero status channel raises Service Out.	→ Raise SERVO MULTI CL13 branch condition.		→ Microprogram recognizes the rise of SERVO MULTI CL13 branch condition and drops TC Register bit 5 (Status In).
	Drop Status In.	Drop TC Register bit 5.	
Channel drops Service Out	→ Drop SERVO*MULTI*CL13.		→ Microprogram verifies SERVO*MULTI* CL13 branch is off, decodes command and executes command. Prepares for data transfer if command requires it.

Note 1: CU takes a polling interrupt when it goes not busy, placing CU End in the Status Byte.

INITIAL SELECTION (Part 2 of 2)

BUFFER OPERATION

Note: For use of buffers during a Read/Write command, see CHL-I 360, 380.

Address Out

At initial selection time the channel places the device address on the bus out lines and raises the Address Out tag. With Address Out and Allow NA active and Operational In and Status In inactive, the device address is sent to buffer A. The next HJ clock time the address is sent from Buffer A to the NA register.

Address In

If the address compares, Operational In becomes active. The channel recognizes Operational In from the CU and drops Address Out. The CU places the address on the bus in and raises the Address In tag. Address In ANDED with not Write Mode gates the address to the channel.

Command Out

If the address compares, the channel places a command on the bus out and raises the Command Out tag. Command Out and Allow NA gates buffer A to the NA register.

Status In

Command Out causes Address In to fall. The fall of Address In drops the Command Out tag in the channel. On the fall of Command Out the CU places status on the bus in and raises the Status In tag. Status In, Operational In and not Write Mode gate the status (bus in) from buffer B.

This diagram is intended for instruction only. Use machine logics for troubleshooting and scoping.

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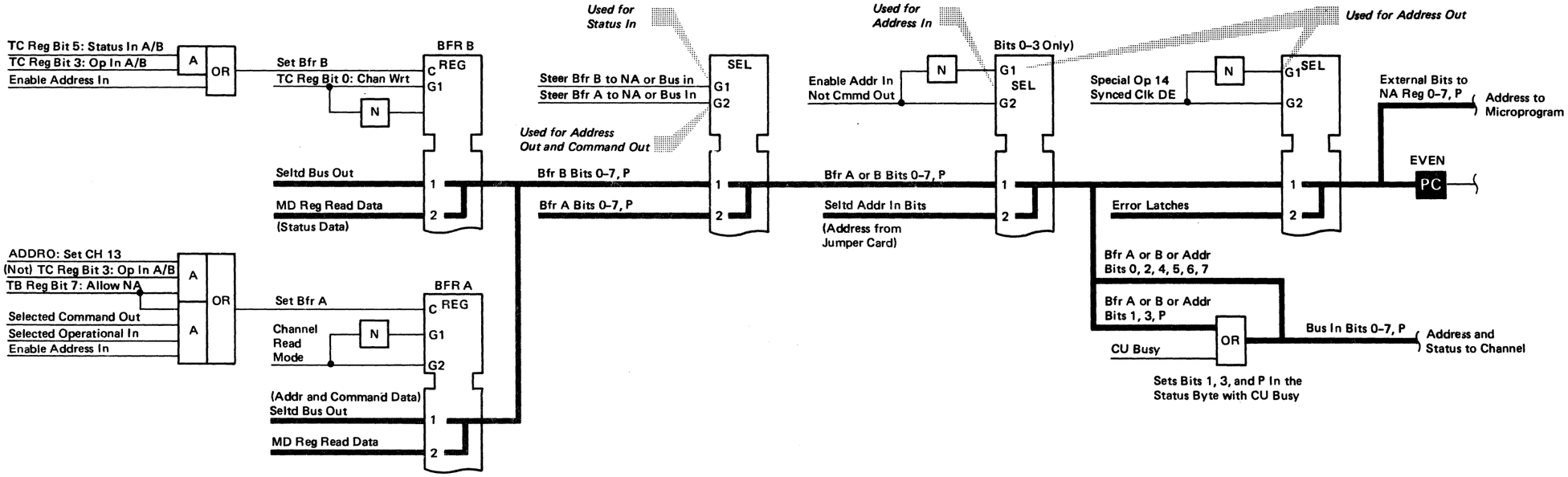

3830-2

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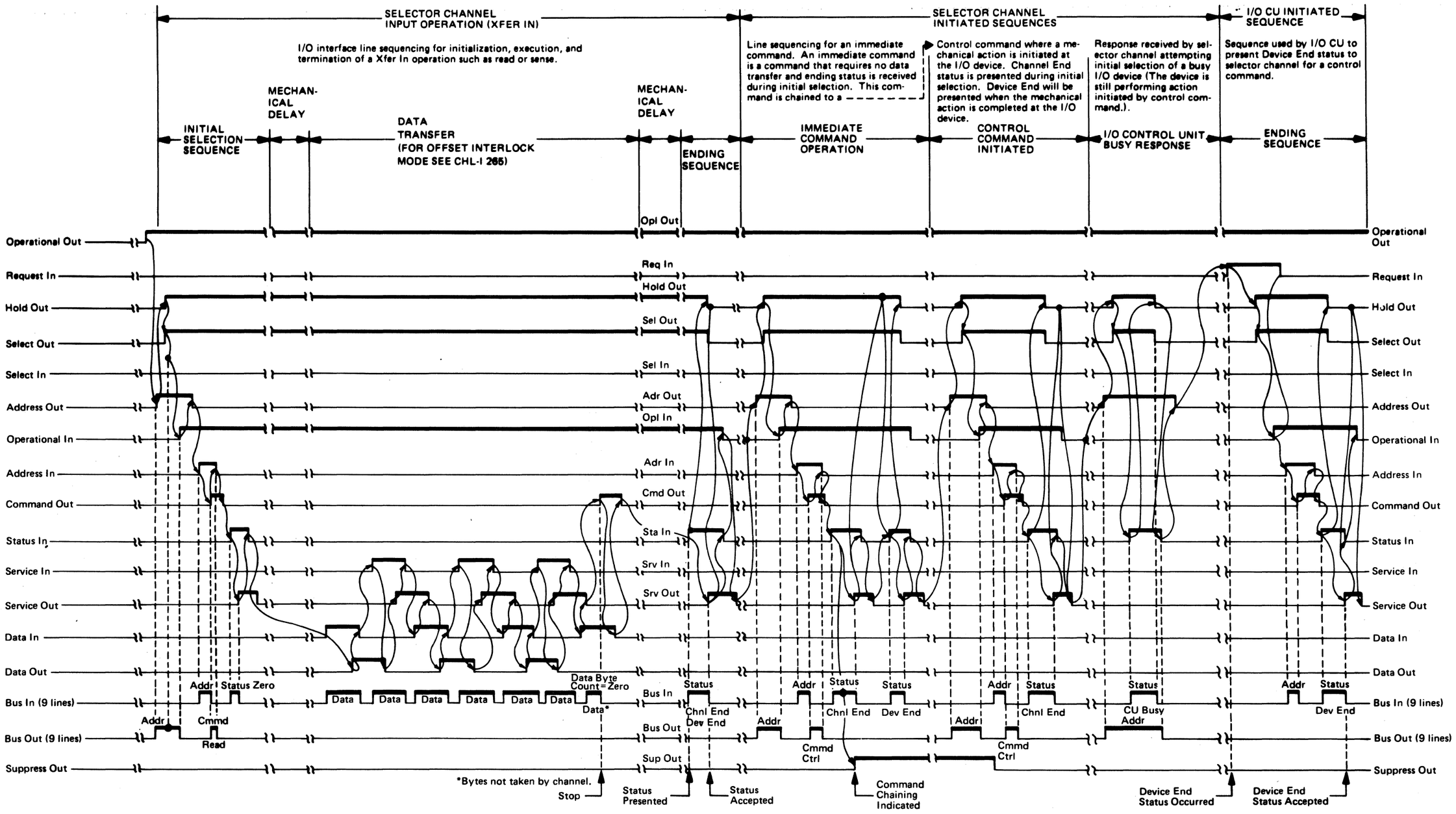
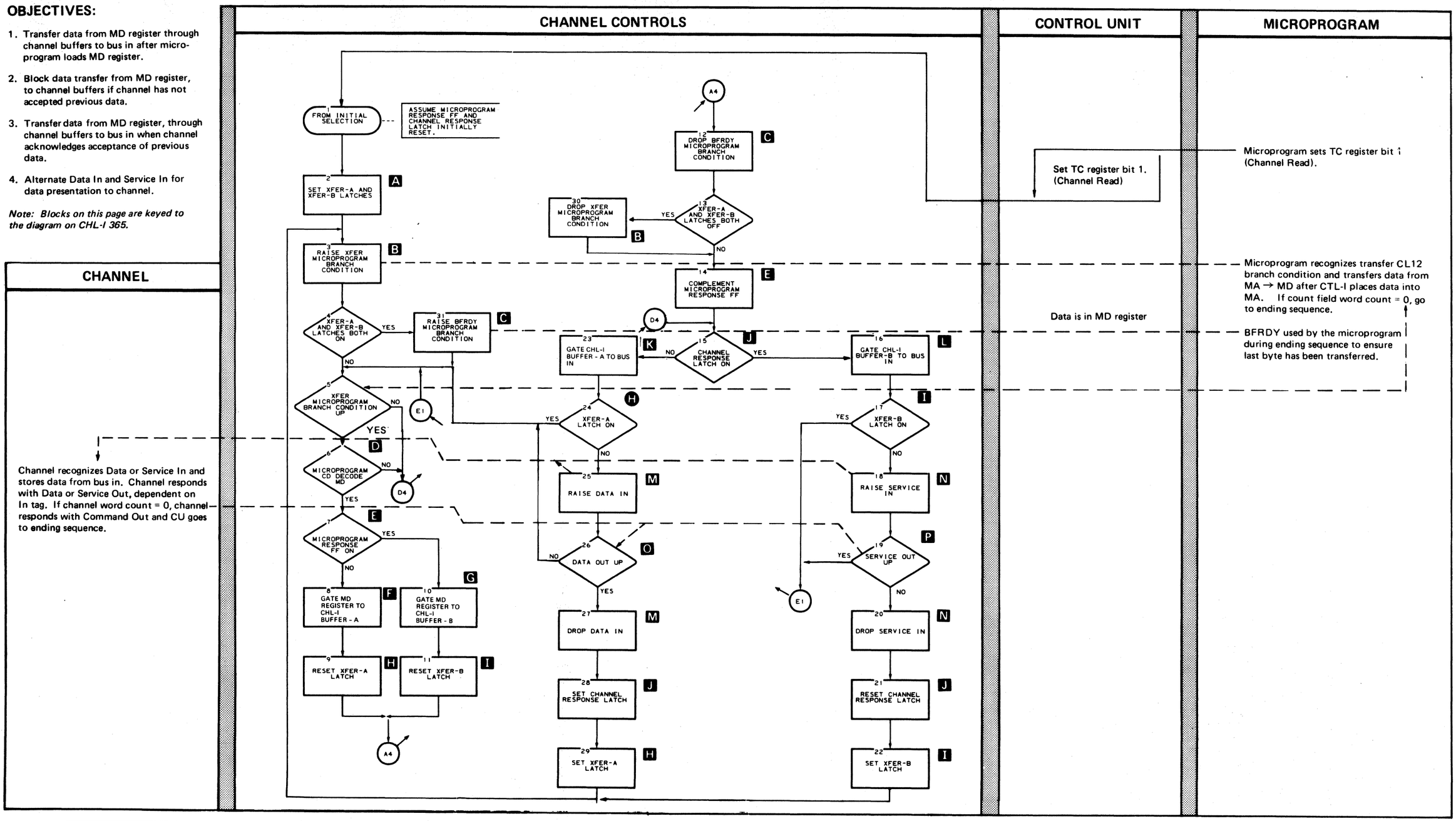
I/O CHANNEL INTERFACE TIMING (Read)



OBJECTIVES:

1. Transfer data from MD register through channel buffers to bus in after microprogram loads MD register.
2. Block data transfer from MD register, to channel buffers if channel has not accepted previous data.
3. Transfer data from MD register, through channel buffers to bus in when channel acknowledges acceptance of previous data.
4. Alternate Data In and Service In for data presentation to channel.

Note: Blocks on this page are keyed to the diagram on CHL-I 365.



READ DATA TRANSFER – SIMPLIFIED CHANNEL CONTROLS

Note: Refer to CHL-I 360 for key symbols on this page

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

CHANNEL RESPONSE LATCH (Read)

- Initially reset, steering buffer A to bus in and allowing Data In.
- Set by Data Out (acceptance of data on bus in) steering buffer B to bus in and allowing Service In.
- Reset by Service Out (acceptance of data on bus in) steering buffer A to bus in and allowing Data In.
- Alternated during subsequent data transfers.

TRANSFER LATCH B (Read)

- Initially set on, blocking Service In.
- Reset, by CD decode of MD and Microprogram Response latch, allowing Service In to gate buffer B to bus in.
- Set again, by Service Out (acceptance of data on bus in), blocking Service In.

MICROPROGRAM RESPONSE LATCH (Read)

- Initially reset, steering output of MD register to buffer A.
- Complemented by CD decode of MD (transfer of new data into MD register) alternating output of MD register to buffer B, then buffer A, etc.

CHL-I BUFFER B (Read)

- Alternates with buffer A.
- Set by CD decode of MD and Microprogram Response latch.
- Used with Service In to place data on bus in.

BFRDY (Microprogram Branch Condition – Read)

- Generated by both Transfer-A and Transfer-B latches being on.
- When up, indicates to the microprogram that both CHL-I buffers are empty.

XFER (Microprogram Branch Condition – Read)

- Generated by either Transfer-A or Transfer-B latch being on.
- When up, indicates to the microprogram that a data transfer to MD reg is required.

TRANSFER LATCH A (Read)

- Initially set on, blocking Data In.
- Reset, by CD decode of MD and not Microprogram Response latch, allowing Data In to gate buffer A to bus in.
- Set again, by Data Out (acceptance of data on bus in), blocking Data In.

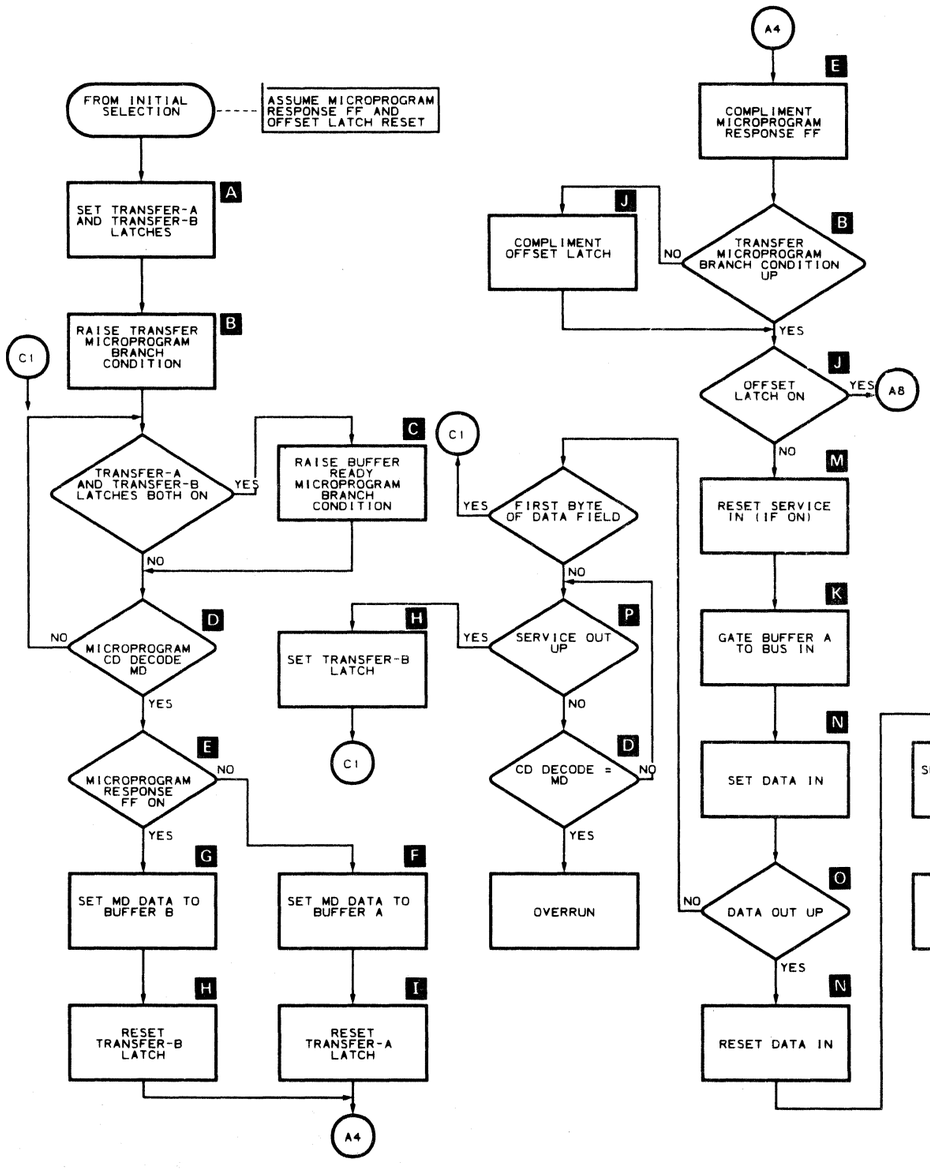
READ DATA

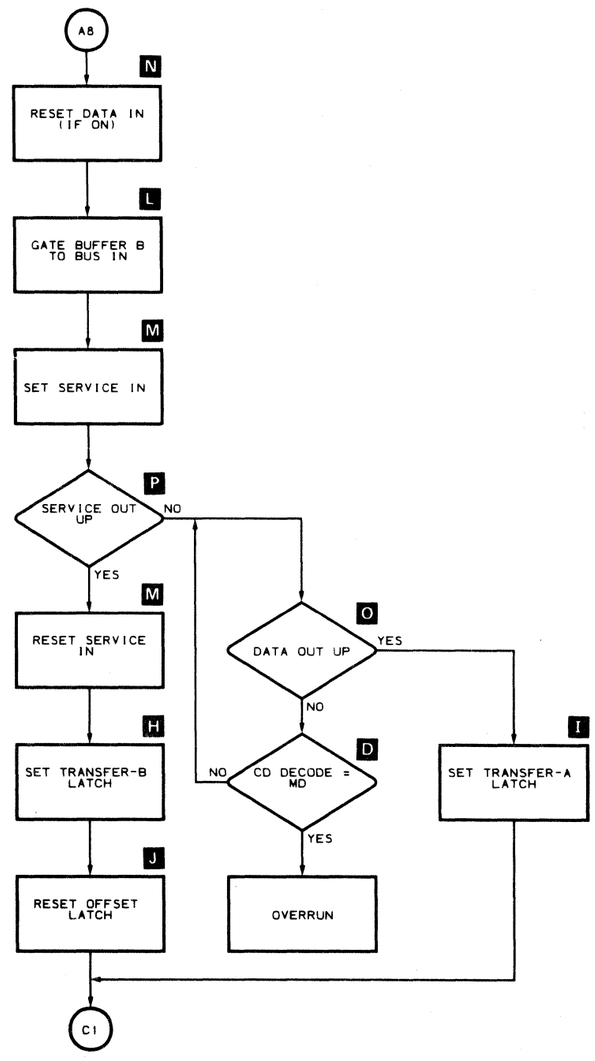
Data between the control interface (CTL-I) and the control unit is monitored by the transfer check circuitry (see CTL-I 110). Data is gated from the device to the CTL-I bus in, to the CTL-I buffer, and then to the MA register in the control unit.

CHL-I BUFFER A (Read)

- Alternates with buffer B.
- Set by CD decode of MD and not Microprogram Response latch.
- Used with Data In to place data on bus in.

NOTE: The blocks on this page are keyed to the diagram on CHL-I 375.





OFFSET READ – SIMPLIFIED CHANNEL CONTROLS

Note: Refer to CHL-I 370 for key symbols on this page.

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

OFFSET LATCH (Read)

- Initially reset, steering buffer A to bus in and allowing Data In.
- Set by Data Out (acceptance of data on bus in) steering buffer B to bus in and allowing Service In.
- Reset by Service Out (acceptance of data on bus in) steering buffer A to bus in and allowing Data In.
- Toggled by CD of MD when operating in Offset Mode.
- Alternated during subsequent data transfers.

TRANSFER LATCH B (Read)

- Initially set on, blocking Service In.
- Reset, by CD decode of MD and Microprogram Response latch, allowing Service In to gate buffer B to bus in.
- Set again, by Service Out (acceptance of data on bus in), blocking Service In.

MICROPROGRAM RESPONSE LATCH (Read)

- Initially reset, steering output of MD register to buffer A.
- Complemented by CD decode of MD (transfer of new data into MD register) alternating output of MD register to buffer B, then buffer A, etc.

CHL-I BUFFER B (Read)

- Alternates with buffer A.
- Set by CD decode of MD and Microprogram Response latch.
- Used with Service In to place data on bus in.

BFRDY (Microprogram Branch Condition – Read)

- Generated by both Transfer-A and Transfer-B latches being on.
- When up, indicates to the microprogram that both CHL-I buffers are empty.

XFER (Microprogram Branch Condition – Read)

- Generated by either Transfer-A or Transfer-B latch being on.
- When up, indicates to the microprogram that a data transfer to MD reg is required.

READ DATA

Data between the control interface (CTL-I) and the control unit is monitored by the transfer check circuitry (see CTL-I 110). Data is gated from the device to the CTL-I bus in, to the CTL-I buffer, and then to the MA register in the control unit.

CHL-I BUFFER A (Read)

- Alternates with buffer B.
- Set by CD decode of MD and not Microprogram Response latch.
- Used with Data In to place data on bus in.

TRANSFER LATCH A (Read)

- Initially set on, blocking Data In.
- Reset, by CD decode of MD and not Microprogram Response latch, allowing Data In to gate buffer A to bus in.
- Set again, by Data Out (acceptance of data on bus in), blocking Data In.

OBJECTIVES:

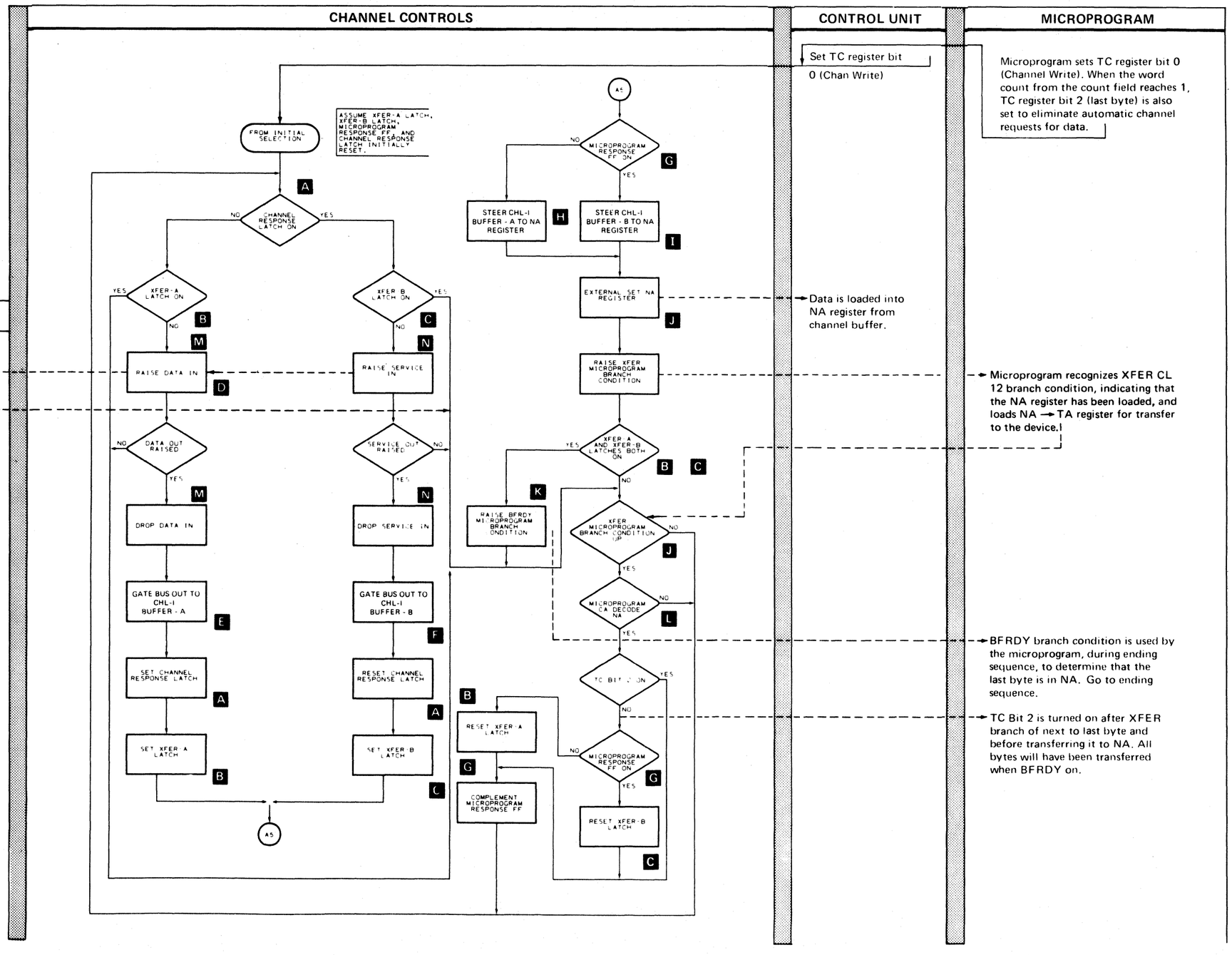
1. Transfer data from bus out, through channel buffers, into NA register.
2. Transfer data only into a channel buffer if NA register is full.
3. Transfer data from a channel buffer, into NA register, and request another data byte.
4. Notify microprogram when NA register contains a byte of data from bus out (XFER).
5. Notify microprogram when all bytes, requested from the channel, have been provided (BFRDY).
6. Microprogram detects an overrun if there is no XFER branch or COMMO branch when required by disk timing.
7. Microprogram detects truncation if there is no XFER branch but there is a COMMO branch.

Note: Blocks on this page are keyed to the diagram on CHL-I 385.

CHANNEL

Channel recognizes Data In or Service In and responds by placing data on bus out and raising Data Out or Service Out (dependent upon In-Tag)

Channel word count = zero. Channel raises Command Out in response to a request for data (Data In or Service In) and goes to Ending Sequence.



Note: Refer to CHL-I 380 for key symbols on this page.

This diagram is intended for instruction only. Use machine logics for troubleshooting and scoping.

CHANNEL RESPONSE LATCH (Write)

- Initially reset, allowing Data In to request data from channel.
- Set by Data Out (notify that data is on bus out) allowing Service In to request another byte from channel.
- Reset by Service Out (notify that data is on bus out) allowing Data In.
- Alternated during subsequent data transfers.

TRANSFER LATCH B (Write)

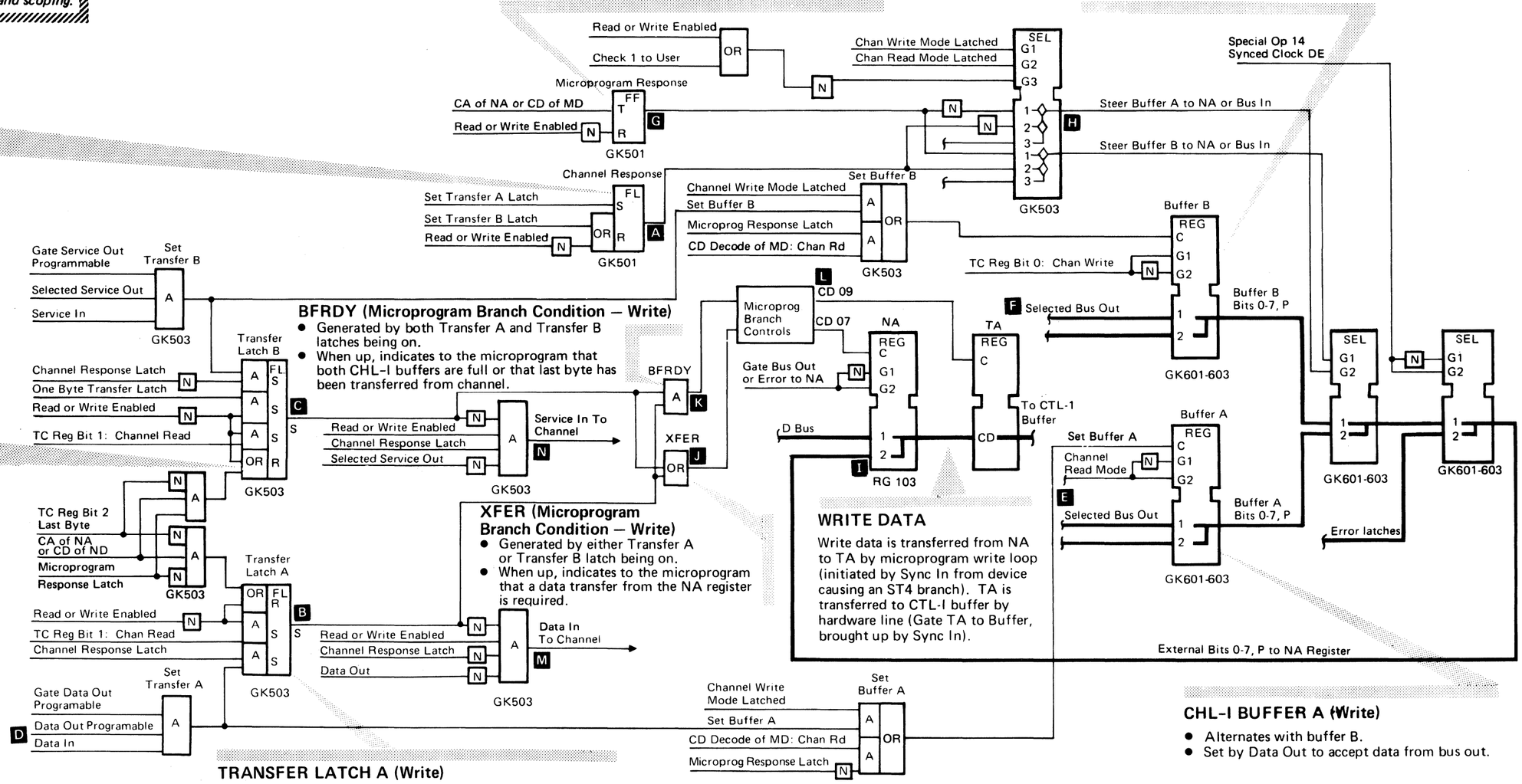
- Initially reset.
- Allows Service In, when channel response latch sets (Data Out), requesting another byte from channel.
- Set by Service Out (notify that data is on bus out) blocking Servicing In.
- Reset by CA decode of NA (notify that data was transferred from buffer) and Microprogram Response latch, allowing Service In to get another byte from channel.

MICROPROGRAM RESPONSE LATCH (Write)

- Initially reset, steering buffer A to NA register.
- Complemented by CA decode of NA (transfer of data into NA register) alternating output of buffer B to NA register then buffer A, etc.

CHL-I BUFFER B (Write)

- Alternates with buffer A.
- Set by Service Out to accept data from bus out.



TRANSFER LATCH A (Write)

- Initially reset allowing Data In.
- Set by Data Out (notify that data is on bus out) blocking Data In.
- Reset by CA decode of NA (notify that data was transferred from buffer) and not Microprogram Response latch, allowing Data In to request another byte from channel.

CHL-I BUFFER A (Write)

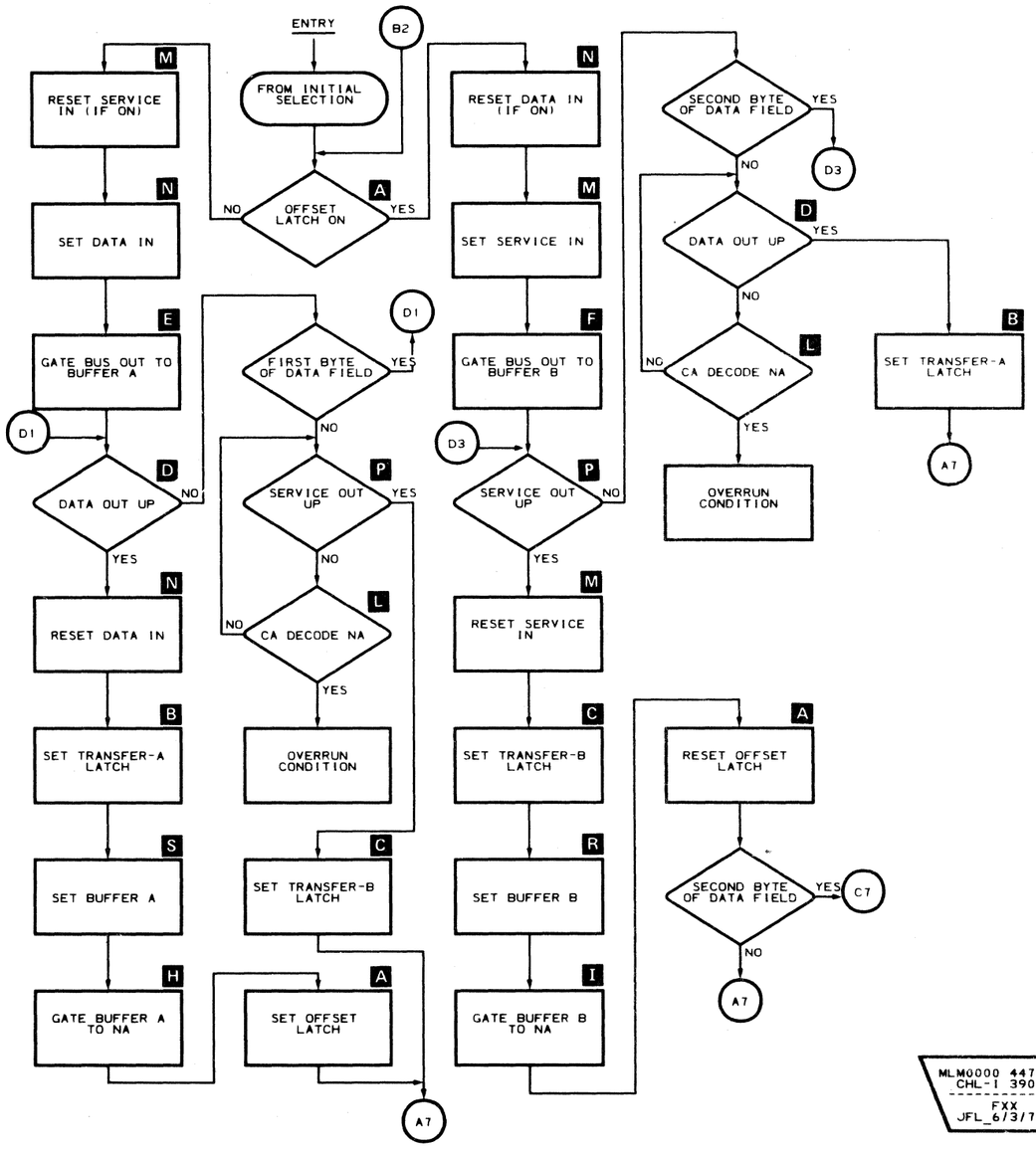
- Alternates with buffer B.
- Set by Data Out to accept data from bus out.

OFFSET WRITE

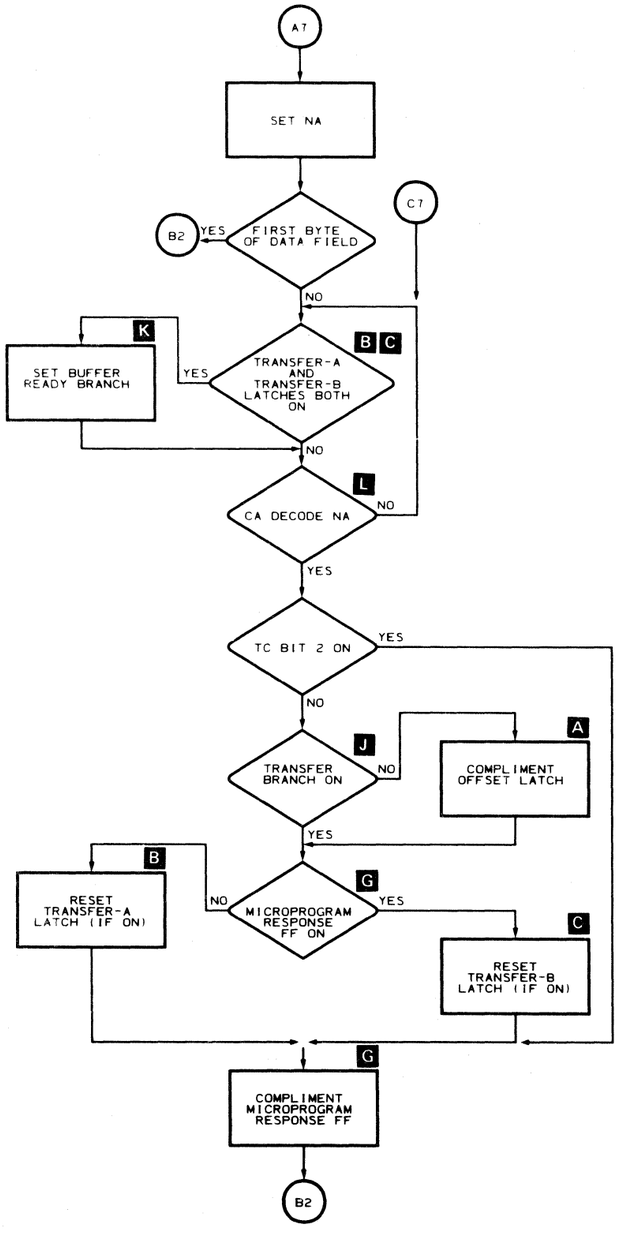
NOTES:

Assume transfer-A Latch, transfer-B Latch, microprogram response FF, and offset latch initially reset

The blocks on this page are keyed to the diagram on CHL-I 395.



MLM0000 447460
CHL-I 390-L
FXX
JFL_6/3/75



MLM0000 447460
CHL-I 390-R
GXX
JFL_6/3/75

OFFSET WRITE – SIMPLIFIED CHANNEL CONTROLS

Note: Refer to CHL-I 390 for key symbols on this page.

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

OFFSET LATCH (Write)

- Initially reset, allowing Data In to request data from channel.
- Set by Data Out (notify that data is on bus out) allowing Service In to request another byte from channel.
- Reset by Service Out (notify that data is on bus out) allowing Data In.
- Toggled by CA of NA when operating in Offset Mode.
- Alternated during subsequent data transfers.

TRANSFER LATCH B (Write)

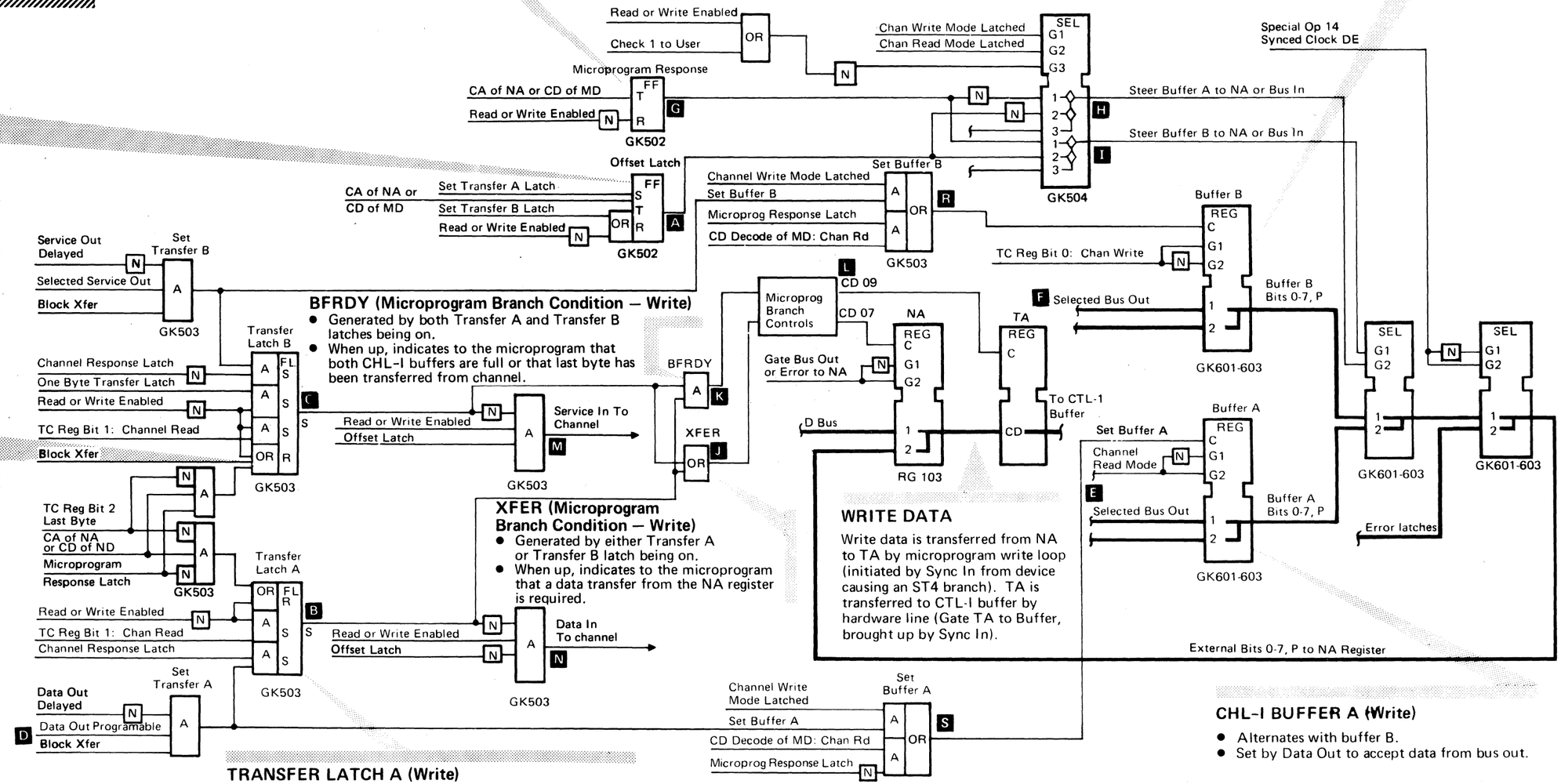
- Initially reset.
- Allows Service In, when channel response latch sets (Data Out), requesting another byte from channel.
- Set by Service Out (notify that data is on bus out) blocking Servicing In.
- Reset by CA decode of NA (notify that data was transferred from buffer) and Microprogram Response latch, allowing Service In to get another byte from channel.

MICROPROGRAM RESPONSE LATCH (Write)

- Initially reset, steering buffer A to NA register.
- Complemented by CA decode of NA (transfer of data into NA register) alternating output of buffer B to NA register then buffer A, etc.

CHL-I BUFFER B (Write)

- Alternates with buffer A.
- Set by Service Out to accept data from bus out.



TRANSFER LATCH A (Write)

- Initially reset allowing Data In.
- Set by Data Out (notify that data is on bus out) blocking Data In.
- Reset by CA decode of NA (notify that data was transferred from buffer) and not Microprogram Response latch, allowing Data In to request another byte from channel.

CHL-I BUFFER A (Write)

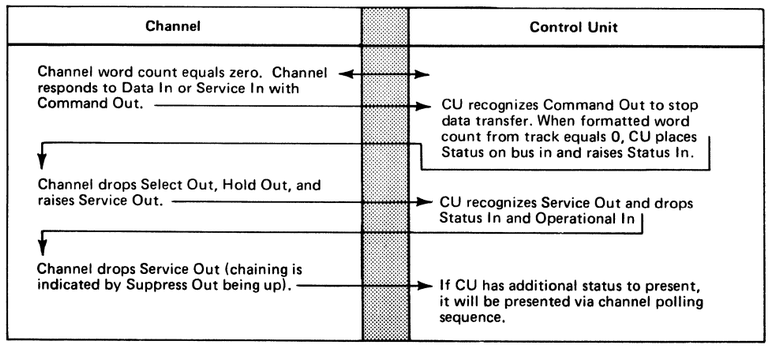
- Alternates with buffer B.
- Set by Data Out to accept data from bus out.

ENDING SEQUENCE

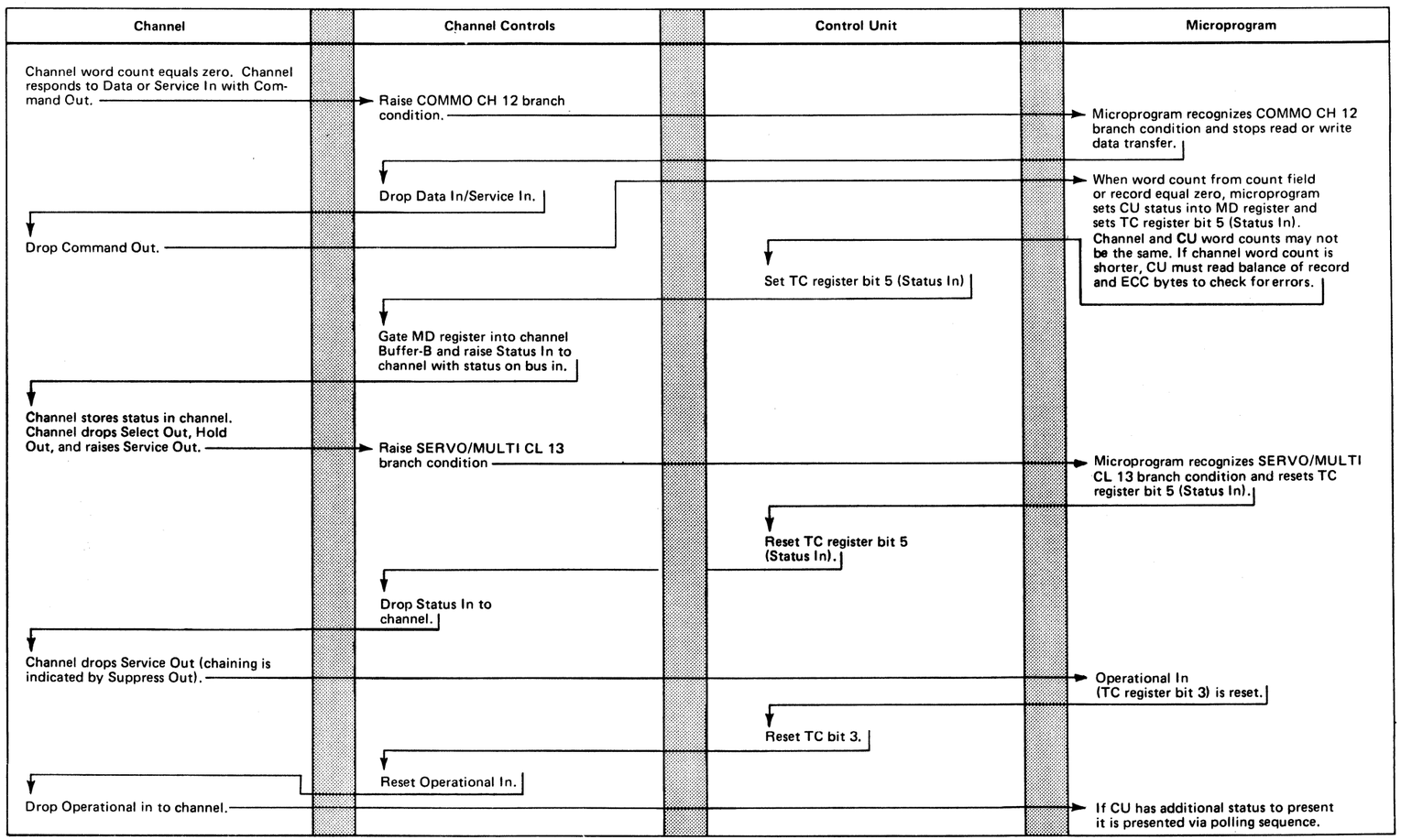
OBJECTIVES

1. Recognize word count equal to zero, either channel word count or word count from track format.
2. When channel word count equals zero, channel responds to Data or Service In with Command Out.
3. When CU formatted word count equals zero CU places status on bus in and raises Status In.
4. Channel recognizes Status In and drops Select Out, Hold Out, and raises Service Out.
5. CU drops Status In and Operational In.
6. If CU has additional status (such as Device End) it will be presented via polling sequence. See CHL-I 265.

ENDING SEQUENCE SIMPLIFIED



DETAILED ENDING SEQUENCE

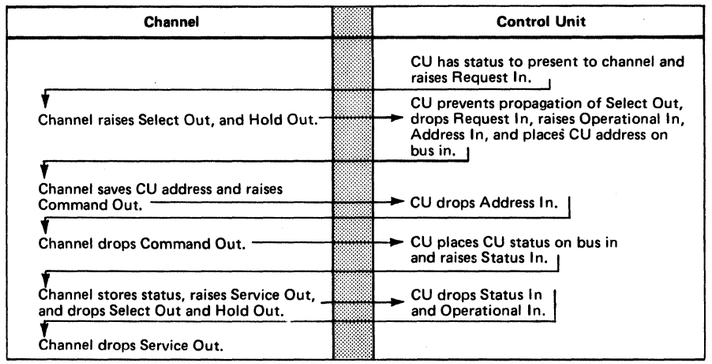


CONTROL UNIT INITIATED SEQUENCE (Polling) STATUS PRESENTATION

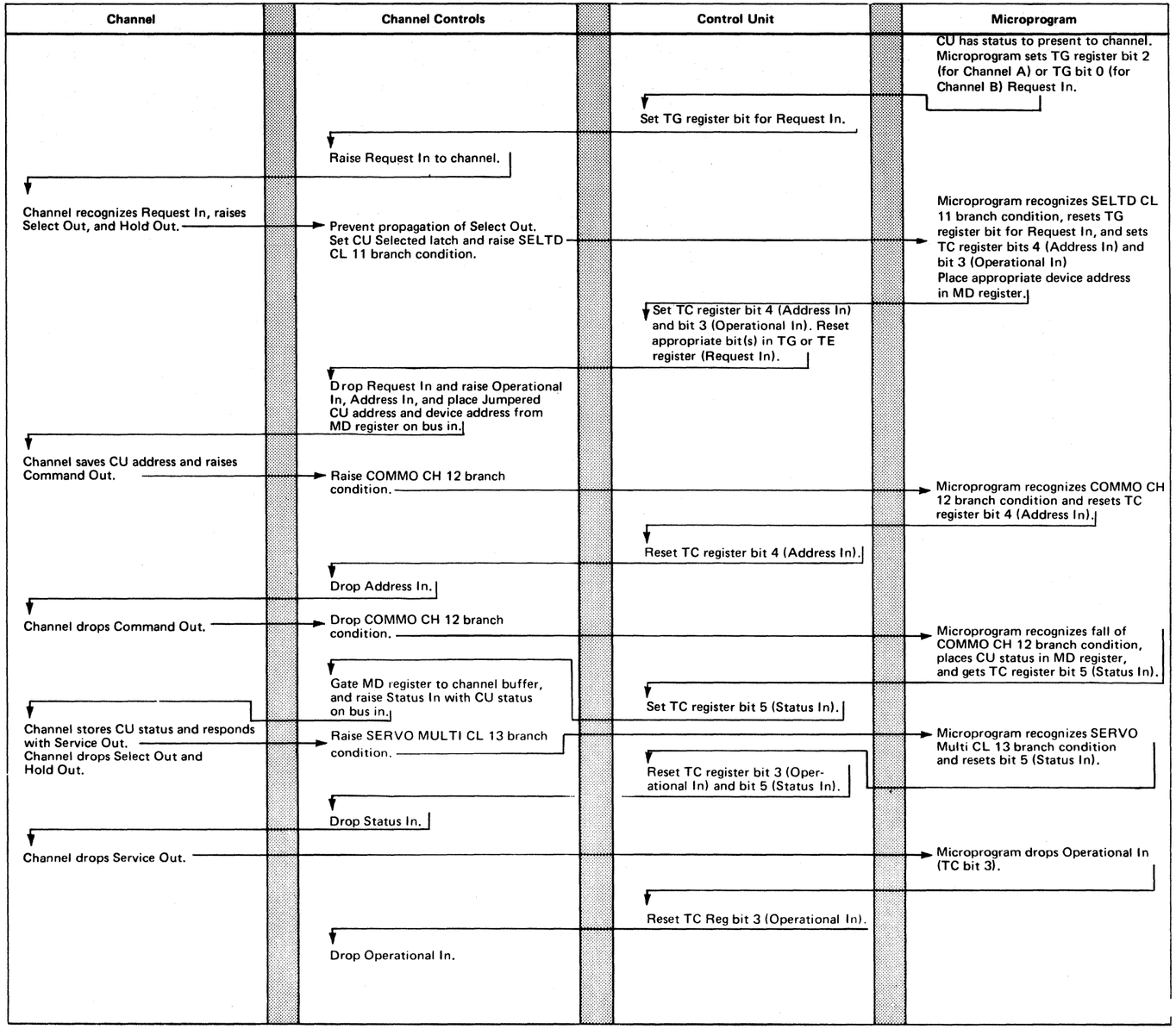
OBJECTIVES:

1. CU has status to present to channel.
2. CU raises Request In to channel.
3. Channel raises Select Out, and Hold Out.
4. CU prevents propagation of Select Out, drops Request In, raises Operational In, Address In, and places CU address on bus in.
5. Channel saves CU address and raises Command Out.
6. CU drops Address Out.
7. Channel drops Command Out.
8. CU places CU status on bus in and raises Status In.
9. Channel stores status, raises Service Out, and drops Select Out and Hold Out.
10. CU drops Status In.
11. Channel drops Service Out.

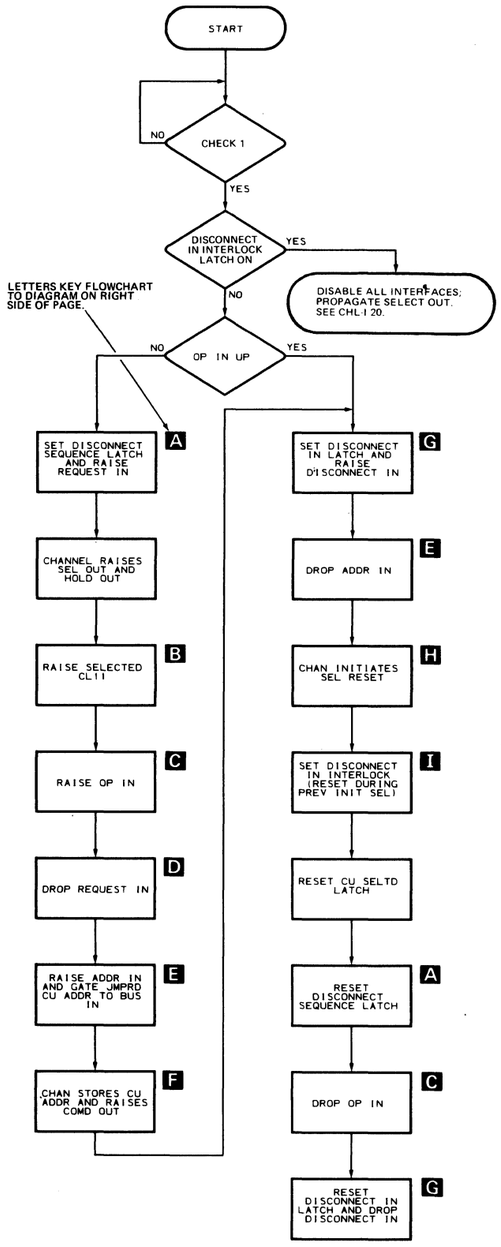
POLLING SEQUENCE SIMPLIFIED



POLLING SEQUENCE DETAIL



CONTROL UNIT INITIATED SEQUENCE (POLLING)
CHECK 1 SIMPLIFIED CONTROLS



Objectives:

Check 1 while disconnected from channel (Op In down).

1. CU has an unrecoverable error (Check 1).
2. CU raises Request In to channel.
3. Channel raises Select Out, and Hold Out.
4. CU raises Operational In and drops Request In.
5. CU raises Address In and places control unit address with device address 000 on bus in.
6. Channel stores CU address and raises Command Out.
7. CU drops Address In and raises Disconnect In.
8. Channel initiates a selective reset to CU by raising Suppress Out and dropping Operational Out.
9. CU drops Disconnect In, Operational In, and performs a selective reset.

Check 1 while connected.

1. CU has an unrecoverable error (Check 1).
2. CU raises Disconnect In.
3. Channel initiates a selective reset to CU by raising Suppress Out and dropping Operational Out.
4. CU drops Disconnect In, Operational In, and performs a selective reset.

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

Disconnect Sequence Latch

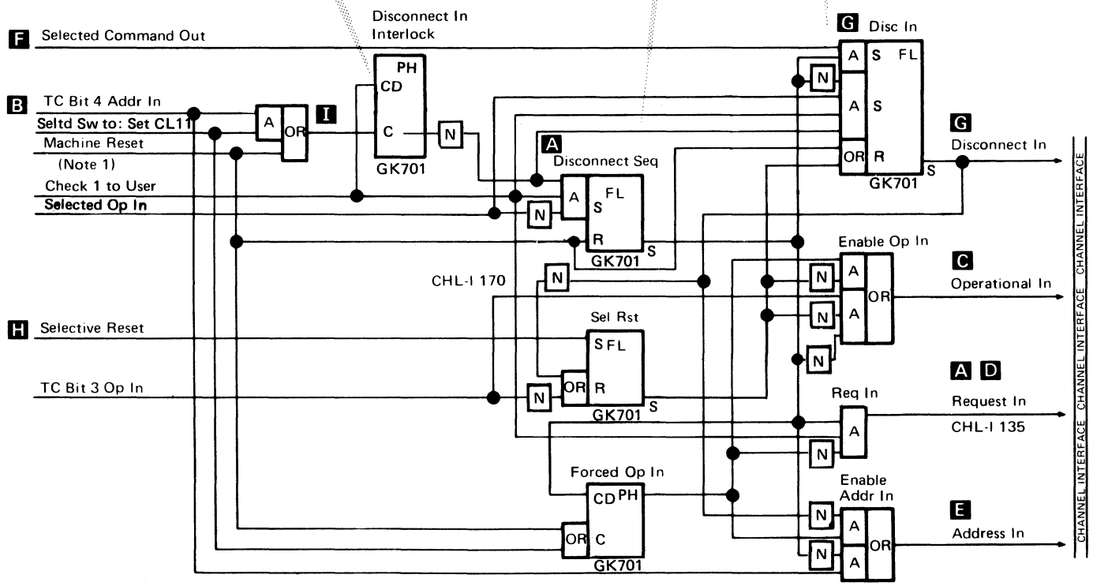
- Set by Check 1 if an initial selection sequence has occurred since last Check 1.
- When on generates Request In to channel and allows Disc In Latch to be set by Command Out.
- When off allows Check 1 to raise Disconnect In if Operational In is up.
- Reset by machine reset.

Disconnect In Interlock

- Set by machine reset and Check 1.
- When on, inhibits Check 1 from starting a Disconnect In sequence.
- Reset during initial selection by Address In.

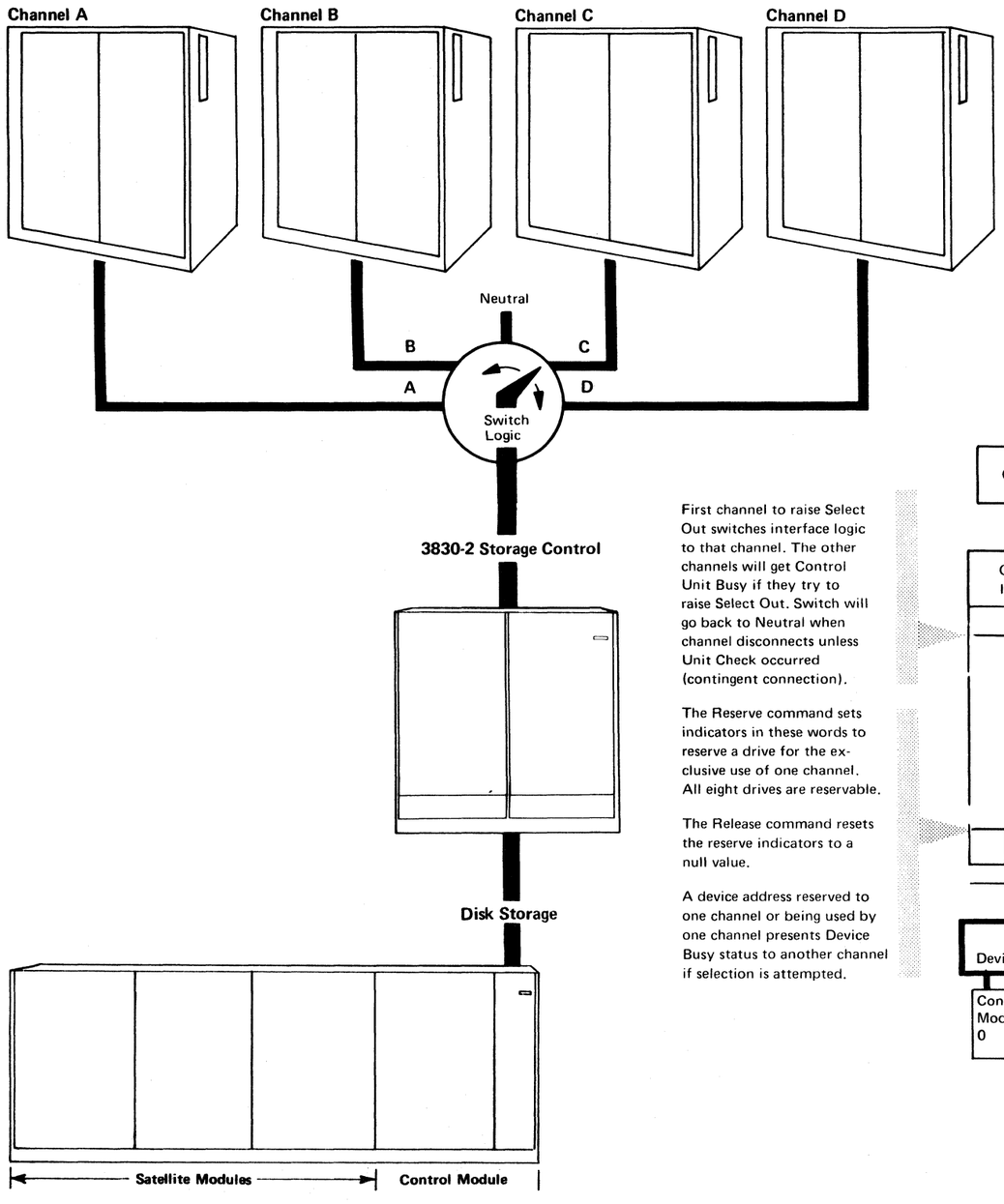
Disconnect In Latch

- Set when Check 1 occurs if CU connected. Set as response to Command Out if CU not connected when Check 1 occurs.
- When on, generates Disconnect In to Channel.
- Reset by machine reset.



Note: Machine Reset is raised by Selective Reset.

TWO CHANNEL AND TWO CHANNEL ADDITIONAL: CONCEPT AND COMMANDS



TWO CHANNEL SWITCH AND TWO CHANNEL SWITCH, ADDITIONAL, DEVICE RESERVATION CONCEPT

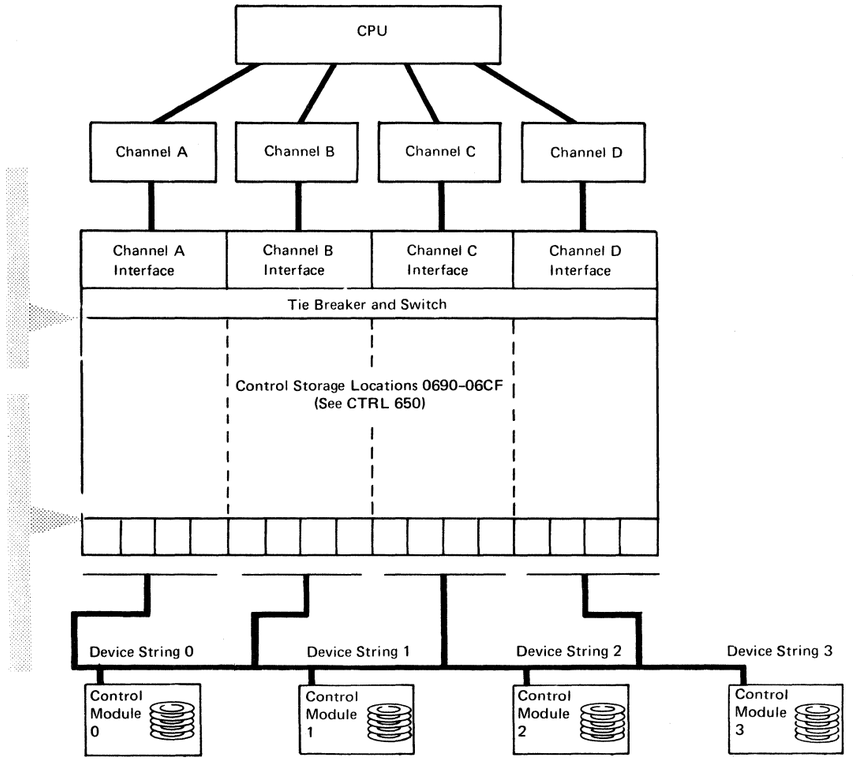
The Two Channel Switch and Two Channel Switch, Additional, enables two or four channels to share the 3830-2 and also allows individual drives to be reserved for the exclusive use of any channel. The channels may be attached to the same CPU or different CPUs. Channel switching and device reservation are made under control of the system programs. Refer to CMD 140 for descriptions of the Device Reserve and Device Release commands.

First channel to raise Select Out switches interface logic to that channel. The other channels will get Control Unit Busy if they try to raise Select Out. Switch will go back to Neutral when channel disconnects unless Unit Check occurred (contingent connection).

The Reserve command sets indicators in these words to reserve a drive for the exclusive use of one channel. All eight drives are reservable.

The Release command resets the reserve indicators to a null value.

A device address reserved to one channel or being used by one channel presents Device Busy status to another channel if selection is attempted.



BK3100	2347149	437402A	437404	437405	437408	437414	437415	
Seq 2 of 2	Part Number	15 Mar 72	23 Jun 72	15 Aug 72	16 Oct 72	4 Jun 73	2 Nov 73	

CHL-I 470

CHANNEL SWITCHING, SIMPLIFIED

The 3830-2 Storage Control contains a logical Channel Selection switch that has five positions: Channel A, Channel B, Channel C, Channel D, and Neutral. When the switch is in the Neutral position, the storage control is selected by the first channel starting a selection sequence. If multiple channels attempt to select the 3830-2 simultaneously, the tie is resolved by the switch logic.

The microprogram has the option of preventing the switch logic from switching to A, B, C, or D by raising TG bit 7, 6, 5, or 4 respectively.

The microprogram also has the ability to "freeze" the switch completely; that is, to prevent any change of position. The microprogram does this upon recognizing that a channel has initiated a select and that the switch is not in Neutral. Special Op 26 effects this freeze.

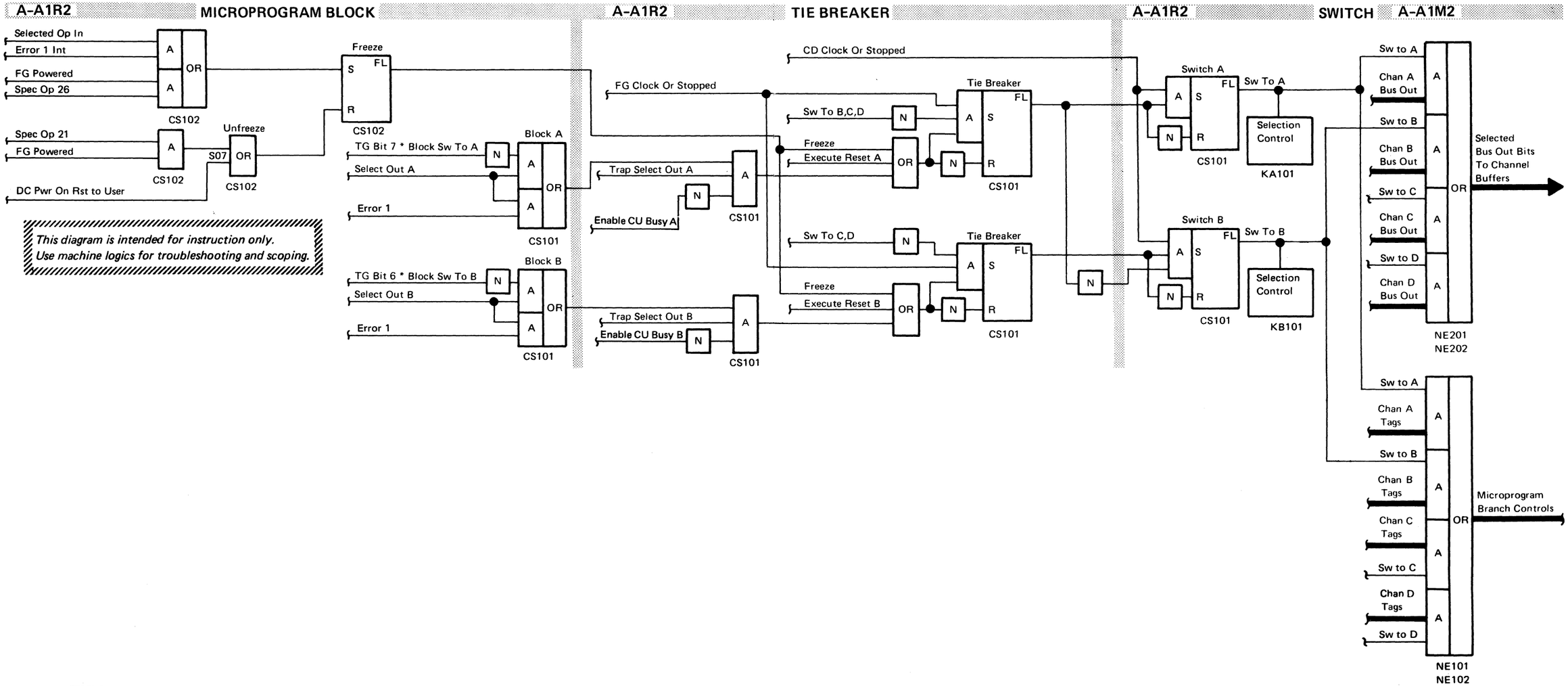
At the end of a connection, the switch is allowed to return to Neutral by unfreezing it (Special Op 21), unless any of the following conditions exist:

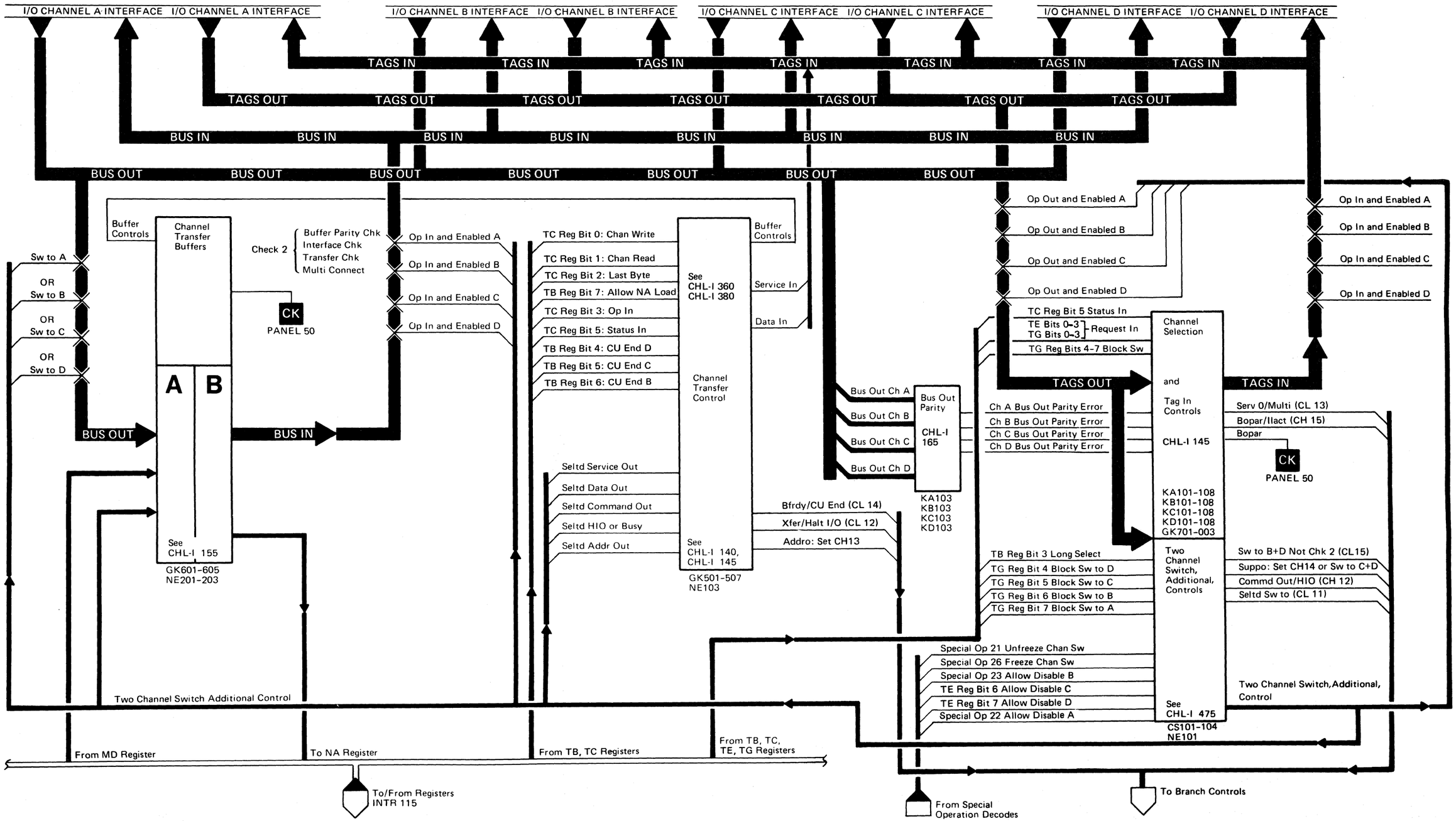
1. The channel indicates command chaining after status, including Device End.
2. The channel indicates command chaining, Device End was not included in the status, and the channel does not disconnect.
3. The channel indicates command chaining, and Device End was not included in the status. The channel disconnects, and the storage control becomes busy to allow one of the following:
   a. Storage control error recovery procedure.
   b. Diagnostic Load or Write operation.
   c. Completion of a format Write operation.
4. The channel does not indicate command chaining, and a format operation is in progress.
5. The last status byte was part of a channel-initiated signal sequence and was stacked by the channel.
6. An error occurred.

As an example, assume that channel B has selected the 3830-2. Then, if channel A attempts to select the 3830-2, the 3830-2 responds with a short Control Unit Busy sequence. After the Channel Selection switch returns to the Neutral position, the 3830-2 attempts to present a status byte containing Control Unit End to channel A. This pending Control Unit End status will not cause the 3830-2 to appear busy to channel B, provided that the Channel Selection switch is not actually connected to channel A.

The address byte connected with the Control Unit End status contains the address of a certain device. This device is the lowest numerically addressed device not implicitly connected to either interface.

Two channel commands permit reservation or release of the device. They are Device Reserve and Device Release (CMD 450).





3830-2	BK3200	2347150	437402A	437404	437405	437408	437414		
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CONTENTS

CTL-I

INTRODUCTION

System Orientation CTL-I 5

Describes where CTL-I is located within the storage control unit (CU), and where it is located within the system. This page also shows the interface lines: their names, which lines are outgoing, and which lines are incoming to the CU.

Description of Lines CTL-I 10

Describes the function of each incoming and outgoing interface line and bus lines.

Tag Sequence Definitions CTL-I 15

Describes the two basic operations of the CTL-I: immediate operation, extended operation. Also shows timing chart for each operation.

Selection (Immediate Operation) CTL-I 20

Describes selection in general. Shows how the two types of selection (select device, select controller) operate, with timing charts for each. Shows the standard bit assignments for each tag.

Polling (Immediate Operation) CTL-I 25

Describes polling in general. Shows how the two types of polling (poll device, poll controller) operate. Presents a timing chart with standard bit assignments for each tag.

Immediate Operation (Flow to/from Device) CTL-I 30

Shows data flow through the CU, CTL-I, and to/from the device, for the immediate operation (tags) only.

Data Transfer (Extended Operation) CTL-I 35

Describes data transfer in general, and both the Write and Read operation. Includes a timing chart covering read tag, data transfer, and the ending sequence.

Extended Operation (Data flow to device) CTL-I 45

Shows data flow (both write data and tags) through the CU, CTL-I, and to/from the device. This data flow is for a write data transfer only.

Extended Operation (Data flow from device) CTL-I 50

Shows data flow (both read data and tags) from/to the device and through the CTL-I and CU. This data flow is for a read data transfer only.

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Shows the data flow for the CTL-I logic failures that are detected by the CTL-I, and errors from the selected controller/device. The check 2 errors developed by these circuits are shown on PANEL 50.

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Buffer Parity Check
Unexpected End Check
Bus Out Parity Check
Tag Bus Parity Check
Transfer Error
Load S Register Check
Compare Assist Check

Load S Registers CTL-I 190

Shows the logic and describes the purpose of the load S-register circuit.

CTL-I SYSTEM ORIENTATION

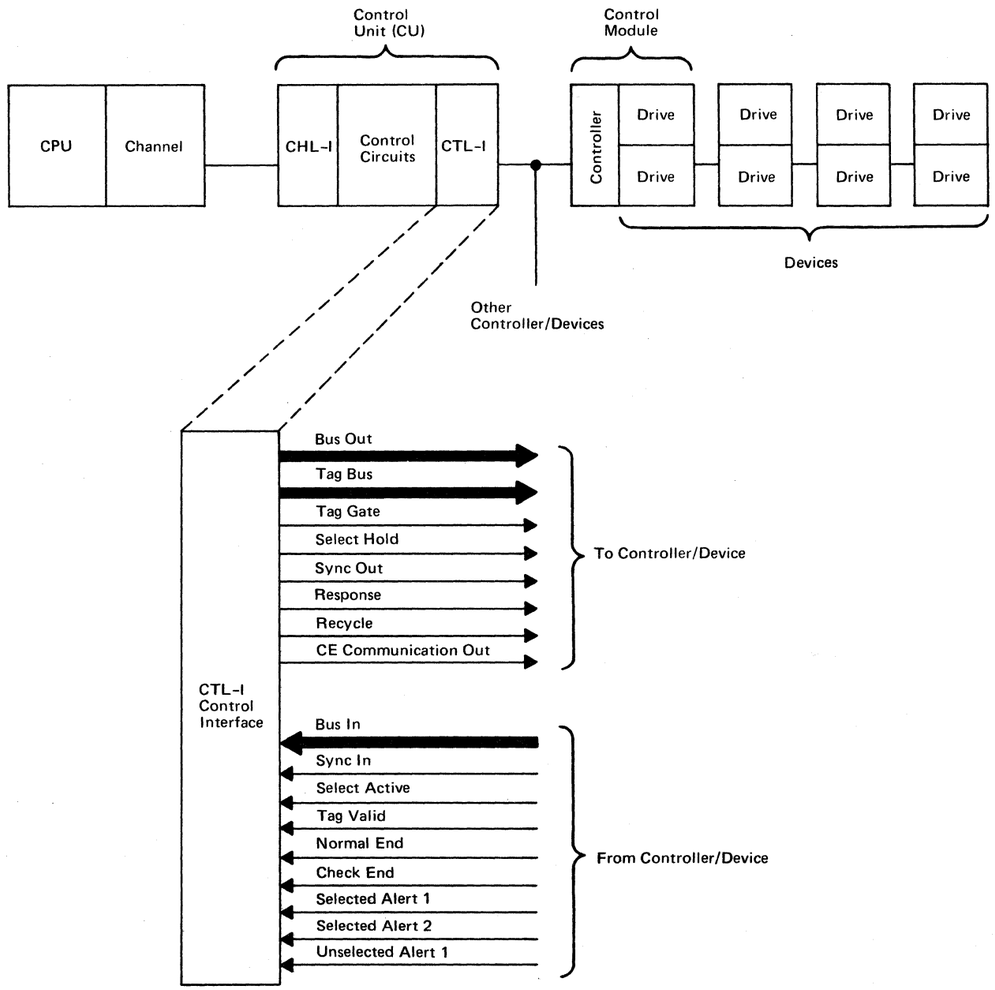
The Control Interface (CTL-I) is the communication link between the Control Unit (CU) microprogram and the controller device.

It consists of the logic, board wiring, tri-leads, cables, and connectors required to:

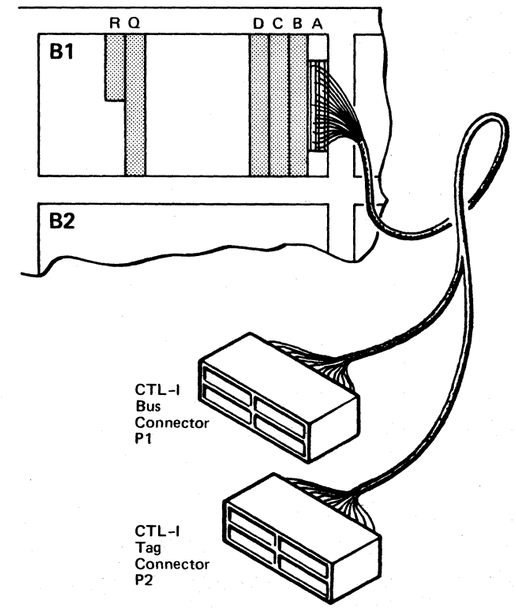
1. Transform bits in general purpose registers into signals on the interface cable to the controller/device.
2. Receive signals placed on the interface cable by the controller/device and gate them to the general purpose registers or convert them to branch conditions for use by the microprogram.
3. Control operations which require communications between the CU and the controller/device.
4. Detect malfunctions during Control Interface operations and notify the microprogram by setting Check 2 Error.

Outbound lines (bus, tag bus, and tags) are described on CTL-I 10.

Inbound lines (bus, and tags) are described on CTL-I 10.



Control Interface Logic Location



CTL-I DESCRIPTION OF LINES

OUT LINES (FROM CTL-I)

Bus Out

Transmits one byte of data (bits 0-7, P). When Sync Out is present, bus out transmits write data to the controller/device.

When Tag Gate is present, bus out transmits command information and tag modifiers.

Data must be valid before the rise of Sync Out, as the controller may take the byte on bus out immediately.

Command information and tag modifiers must be valid before the rise of tag gate.

Tag Bus

The standard tag bus is six lines to the controller/device, (five bits plus odd parity).

When Tag Gate is present, the tag bus transmits control or instruction information to the controller/device, to define the operations to be performed.

Tag Gate

Indicates to the controller/device the presence of control or instruction information on the tag bus, and the presence of tag modifiers on bus out.

Select Hold

Rises during any selection sequence. (see CTL-I 15.) Remains up to maintain selection of controller/device and cannot fall until either Normal End or Check End signals that the last operation to be performed on the device was received and acknowledged.

Sync Out

On a write data operation, Sync Out indicates to the controller/device the presence of write data on bus out.

On a read data operation, Sync Out indicates to the controller/device when each data byte was received.

Response

Indicates to the controller/device the presence of Normal End or Check End on an extended operation.

Recycle

During Read, Write, or ECC correction operations, the CU uses a 16-bit counter (MB and MC registers) to indicate the number of bytes of data remaining to be transferred. The controller/device also contains a byte counter, but it is only four bit positions wide.

Recycle is used to inform the controller/device that it should recycle its byte counter when it reaches zero because there are more bytes to be transferred. If Recycle is not active when the controller/device counter reaches zero, the controller/device initiates an end operation by raising Normal End or Check End.

At the beginning of a data transfer operation, the CTL-I byte counter is loaded with the number of bytes to be transferred, then the Recycle latch is set. Each time a byte of data is transferred the byte counter is decremented. When the count reaches seven, the Recycle latch resets.

CE Communication Out

This is a spare driver added to aid the CE when troubleshooting in the device. To use, install a trilead from ACR Sync (A-B2P2J04) or Sw Sync (A-B2J2U07) to the input pin (A-B1B4J04) of the CE Communication Out Driver. The sync pulses will be transmitted through the control interface cable and can be picked up in the device.

IN LINES (FROM CONTROLLER/DEVICE)

Bus In

Transmits one byte of data (bits 0-7, P). When Sync In is present, bus in transmits read data from the controller/device (Read Data operation).

When Normal End is present, bus in transmits a single byte describing the state of the controller/device.

When Check End is present, bus in transmits error information from the controller/device.

When Tag Valid is present, bus in transmits a byte of information from the controller/device.

Sync In

On a read data operation, Sync In indicates to the CTL-I the presence of read data on bus in.

On a write data operation, Sync In indicates to the CTL-I when each data byte was received.

Select Active

Rises as a result of a selection sequence, (see CTL-I 20), to indicate to the CTL-I that the selected controller/device is on-line to the CU.

Select active remains active to indicate proper selection as long as Select Hold is active and as long as selection of a device is correctly maintained by the controller.

Tag Valid

Indicates to the CTL-I, response to Tag Gate and that proper reception of the tag bus and bus out was received.

Normal End usually is generated with tag valid, but Check End may result if tag bus and bus out could not be decoded properly.

When Tag Valid is present, bus in may have information for the CTL-I to receive.

Normal End

Indicates to the CTL-I that the normal ending point of an operation has been reached with the expected results being present.

Normal End rises with or before Tag Valid if the end of the operation is concurrent with tag acceptance (immediate operation). For the type of operation that causes the end condition to be reached after tag valid is raised (extended operation), Normal End must not be indicated until Tag Gate is absent. Information may be placed on bus in with the rise of Normal End.

Check End

Indicates to the CTL-I that an abnormal end condition exists.

The abnormal condition is presented on bus in. Bus In must have correct parity (odd) during the time that Check End is up.

The abnormal condition is presented in place of a Normal End sequence. Check End must remain up and bus in must maintain valid parity (odd) until either (1) Tag Gate falls or (2) until Response rises to acknowledge receipt of the status information on bus in.

Selected Alert 1

Indicates to the CTL-I an error from the selected controller/device. Selected Alert 1 is accepted by the CTL-I at any time.

Selected Alert 2

Indicates to the CTL-I the index time of the selected device.

Unselected Alter 1

Indicates to the CTL-I that the execute switch is transferred in a controller. Normally this causes a polling sequence by the CU to find out which controller/device made the request.

CTL-I TAG SEQUENCES

Two basic tag sequences are defined.

1. Immediate operation.
2. Extended operation.

IMMEDIATE OPERATION

An immediate operation transfers a single control instruction to the controller and transfers a single byte of data to or from the controller.

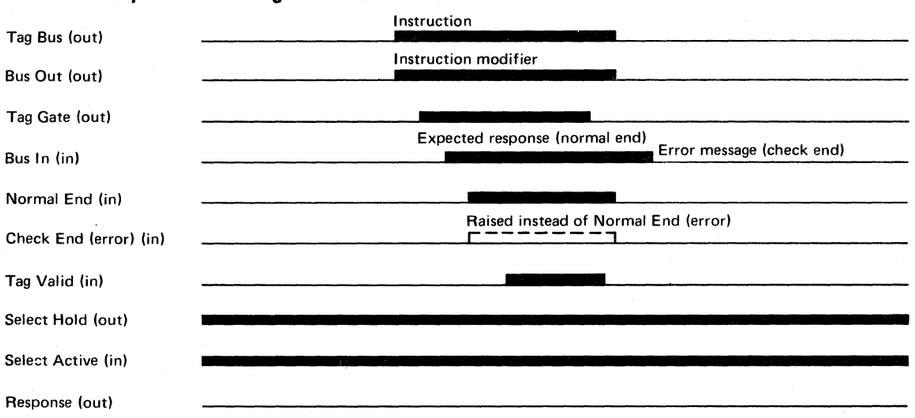
The appropriate tag is placed on tag bus. At the same time, a single byte of data, either an instruction modifier or a byte of data, may be placed on bus out. Tag Gate is raised after the controller is notified that an instruction is on tag bus and bus out.

Tag Gate is acknowledged by Tag Valid and Normal End (or Check End). Data returned by the controller appears on bus in with or before Normal End (Check End). If Normal End is returned, the data on bus in is the expected response from the controller. If Check End is returned, the data on Bus In carries an error message as defined for that device. Tag Gate drops after a timeout within the microprogram. Tag Valid and Normal End (Check End) are dropped by the controller when Tag Gate fails.

All types of immediate operations can take place within any sequence of operations. For example: on a Read or Write operation there will be several immediate operations, before and after actually reading the data. On a selection operation, the selection alone is an immediate operation, but there will be other commands and requests by the CU. For example, the CU can request to read the CE switches on the controller, or it can set a register in the controller. The CU circuits are under control of the microprogram that is loaded in control storage.

The microprogram functional program will match the device or devices, then again the diagnostic program is entirely different. The CU will do what the microprogram instructs it to do, so the cases described in this MLM must be considered as examples only.

Immediate Operation Timing Chart



EXTENDED OPERATION

An extended operation is used to initiate a sequence of events in the controller. The appropriate tag is placed on the tag bus. At the same time a single byte of data or modifying information may be placed on bus out. Tag Gate is raised later, indicating to the controller that tags are on tag bus and bus out.

Tag Valid is returned by the controller, indicating acceptance of the tag, then Tag Gate is dropped. Check End may be returned at this time if the tag is rejected, with the appropriate error message on bus in. The fall of Tag Gate resets Tag Valid and Check End.

After the completion of the operation, Normal End is raised to indicate successful execution of the operation. Check End may be returned, instead of Normal End, when exception conditions are present. Ending information may be transmitted on bus in when Normal End is raised. During Check End, error information is transmitted on bus in.

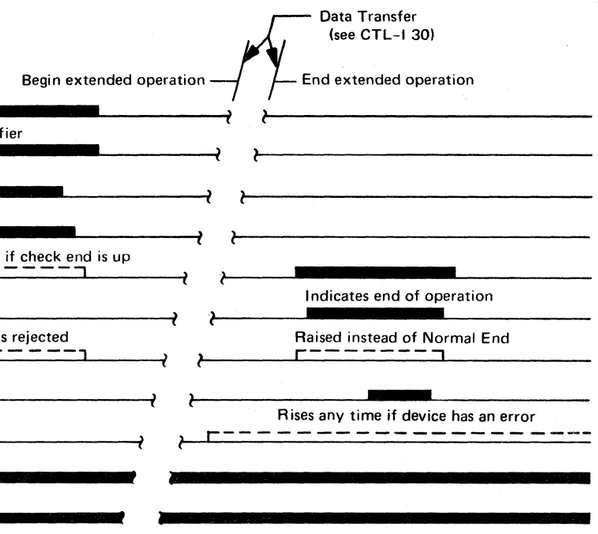
Normal End (Check End) remains up until Response is raised in acknowledgement.

The extended operation can be rather long, involving many bytes of information. The exchange of tags occurs only at the beginning and the end of the transfer of bytes. The timing chart here shows the tags at the beginning and the end, with the long transfer between not shown. See the data transfer timing charts for an example of the data transfers.

Data transfer is the prime example of an extended operation, but any transfer of more than one byte of data is an extended operation.

The difference between extended operation and an immediate operation is that the controller does not return Normal End along with the Tag Valid.

Extended Operation Timing Chart



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CTL-I SELECTION (Immediate Operation)

GENERAL DESCRIPTION

- The CU selects the controller only, or the controller/device.
- Selection and polling tags must be common to all controller/devices on this CTL-I.
- The CTL-I can only be selected for one controller or controller/device at a time.
- The CTL-I can de-select by dropping Select Hold.
- CTL-I Selection is an immediate operation.

This immediate operation is used to connect the control interface (CTL-I) to a particular controller or controller/device.

Selection tag bit patterns are standard for all controller/devices on the CTL-I, and must contain the bit patterns shown on this page.

Two types of selection exist:

1. Select device (hex 83 on tag bus) is used to select the controller and one of its devices. The controller address and the device address are on bus out.
2. Select controller (hex 03 on tag bus) is used when only the controller is needed. Controller address, but no device address is sent out on bus out. Bits 3-7 on bus out address the part of the controller the CU requires, (for example, the CE panel).

Selection must be made to a particular controller or controller/device before an instruction can be sent to it. For example, assume the CPU commands device 2 on controller 0 to seek forward 50 tracks. The CU selects controller 0 device 2, then if selection was successful, a seek forward command from the CU starts the device in motion. The CU, sensing that this is a long operation, disconnects by dropping Select Hold. (Select Active drops because Select Hold drops.) By polling (see CTL-I 25) the CU selects the device again; it does so to execute the next command from the CPU after the Seek is complete.

Selection might be attempted to a controller/device when the device is not ready. The controller responds with Normal End, Select Active, the returned address on bus in, and Tag Valid (if any device on the string has DC power on).

Immediately after a selection, the microprogram always performs a sense operation to the selected device to obtain its status. In this case (not ready) the sense instruction would not find the On Line bit up, and the CU would inform the CPU of this status, and disconnect by dropping Select Hold.

If a selection error is detected within the controller, Check End is raised instead of Normal End. In this case, error information appears on bus in, and Select Active, if present, is ignored.

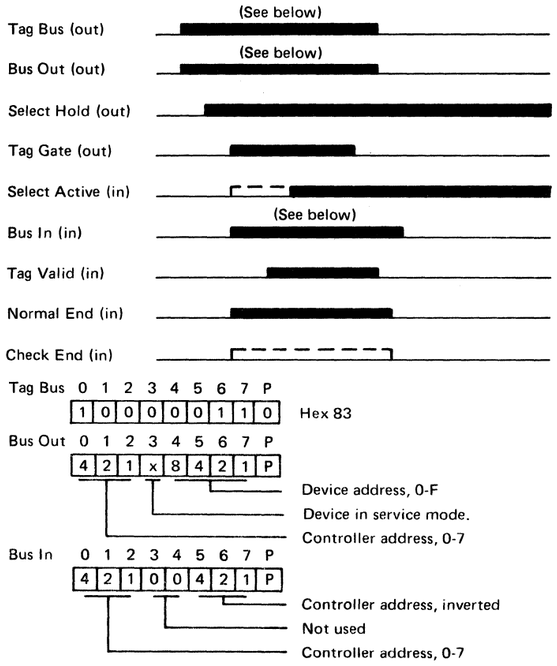
SELECT DEVICE

The select tag (hex 83) is placed on the tag bus; controller address and device address are placed on bus out. Select Hold is raised. Tag Gate is raised after data on tag bus and bus out stabilizes.

The selected controller responds with Select Active, Normal End, and the returned address on bus in. Tag Valid rises after the data on bus in stabilizes. Bus in carries the controller true address in bits 0, 1 and 2, but the inverted address in bits 5, 6, and 7. This coding is used so the CU can check for double responses from the interface.

On a select device (hex 83 on tag bus) with bit 3 set (bus out), any device on this controller string that has a service plug (LAP) installed will be addressed. The device address on bus out is ignored. This type of selection is used by the diagnostic program only.

Select Device Sequence



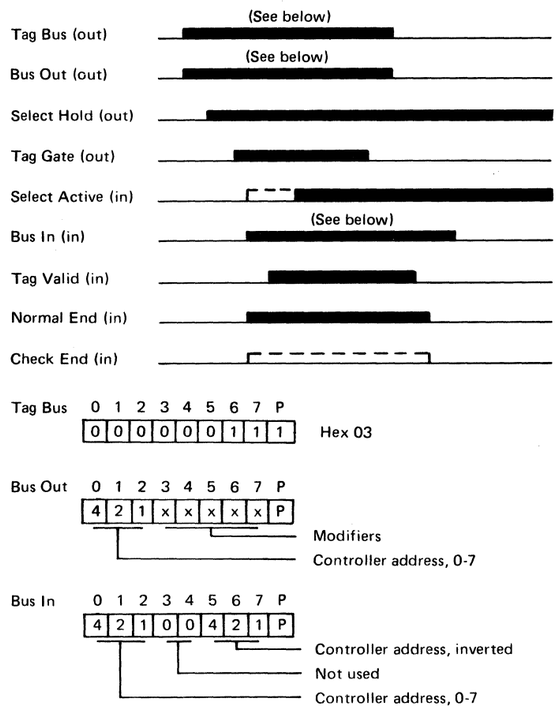
SELECT CONTROLLER

The select tag (hex 03) is placed on the tag bus; controller address and modifiers are placed on bus out. Select Hold is raised. Tag Gate is raised after data on tag bus and bus out stabilizes.

The selected controller responds with Select Active, Normal End, and the returned address on bus in. Tag Valid rises after data on bus in stabilizes. In this case Tag Valid is generated within the controller even if all devices on the string have dc power off.

Bus in carries the controller true address in bits 0, 1, and 2, but the inverted address in bits 5, 6, and 7. This coding is used so the CU can check for double responses from the interface.

Select Controller Sequence



CTL-I POLLING (Immediate Operation)

GENERAL DESCRIPTION

- The CU polls the controller/device during idle loop.
- Polling and selection tags must be common to all controller/devices on the control interface (CTL-I).
- Polling occurs when a controller/device is not selected (idle loop).
- A selection sequence occurs after an interrupt from polling occurs.
- CTL-I polling is an immediate operation.

Polling is like inquiring whether any device requires service. If a device requires service, it signals the CU with an interrupt by putting its bit (address) on bus in. If there is no bit on bus in, then no device requires service. The CU does its polling during the microprogram idle loop by putting hex 82 on tag bus (poll device), or hex 02 on tag bus (poll controller). The CU examines bus in for any bits on, if no bits, it continues with its many different polls within one idle loop.

Two types of CTL-I polling instructions exists:

1. Poll device.
2. Poll controller.

POLL DEVICE

Poll device (hex 82 on tag bus) is an immediate operation that polls the devices on one particular controller string. The controller address is on bus out (only one controller string polled). If a device has an interrupt, it puts its bit on bus in, signaling the CU that it requires service.

The CU then branches out of the idle loop and selects the controller/device. (See CTL-I 20.) The CU has the controller address from its last poll device instruction, and now it also has the device address from the bit that was on bus in during the last poll.

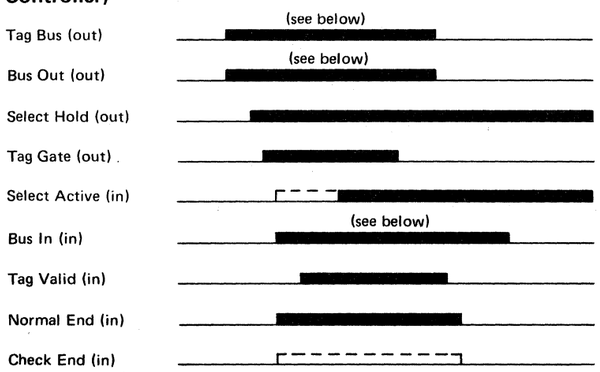
After selection, the microprogram senses the selected device and notifies the CPU of the new status of the device, and probably disconnects (drops Select Hold). Then the microprogram returns to its idle loop and continues with the polling.

The CU can further define the poll device instruction. If bit 3 is on (bus out), the CU only needs to poll the device (or devices) whose address was formerly set into a register within the controller. This register (unsuppressible register) is a mask of eight bits matching bus in on the polling reply. If the bit from the device with an interrupt, matches the bit in the unsuppressible register, the bit propagates to the bus in on the polling reply.

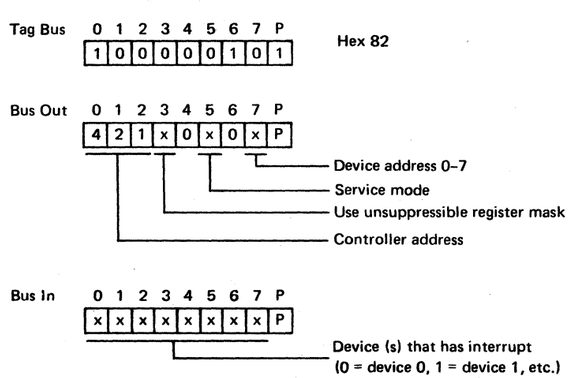
The diagnostic microprogram may set bit 5 on (bus out). In that case, the CU needs to poll only the device that is in service mode (CE mode). The device that is in service mode propagates bit 0 on bus in, signaling the CU that a device on this string is in service mode.

Bit 7 on bus out is device address 0–7; no bit 7 is device address 8–F. If more than eight devices are on one controller then the CU must take two poll device operations to cover all the devices: One poll with bit 7 (bus out), and one poll without bit 7 (bus out).

Polling Tag Sequence (For Poll Device and Poll Controller)



Poll Device Tags



POLL CONTROLLER

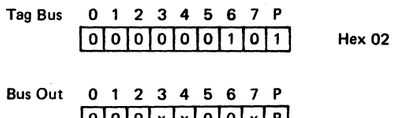
This operation is similar to poll device, but no controller address is on bus out. The microprogram usually does not poll controller unless there is more than one controller. The poll controller operation polls all controllers for an interrupt from any device. The controller with a device requiring service puts its controller address bit on bus in as shown on this page. The microprogram must then poll device to find out which device had the interrupt.

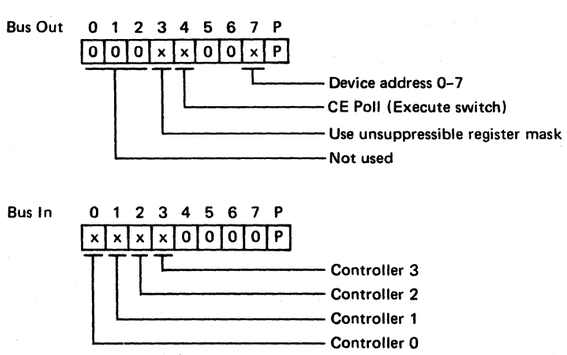
If bit 3 is on (bus out), the CU needs to poll only the controller that has an interrupt from a device (or devices) with an address that matches the unsuppressible register.

Bit 7 (bus out) on is for controllers that have an interrupt from a device address 0–7, and bit 7 off is for devices with address 8–F.

The most common use of poll controller is to have bit 4 (bus out) on. This poll is for any controller that has its CE execute switch transferred. The controller CE execute switch caused an Unselected Alert 1 line to raise, which caused the microprogram to poll the controllers with bit 4 (bus out) on. If the system only has one controller, the controllers need not be polled.

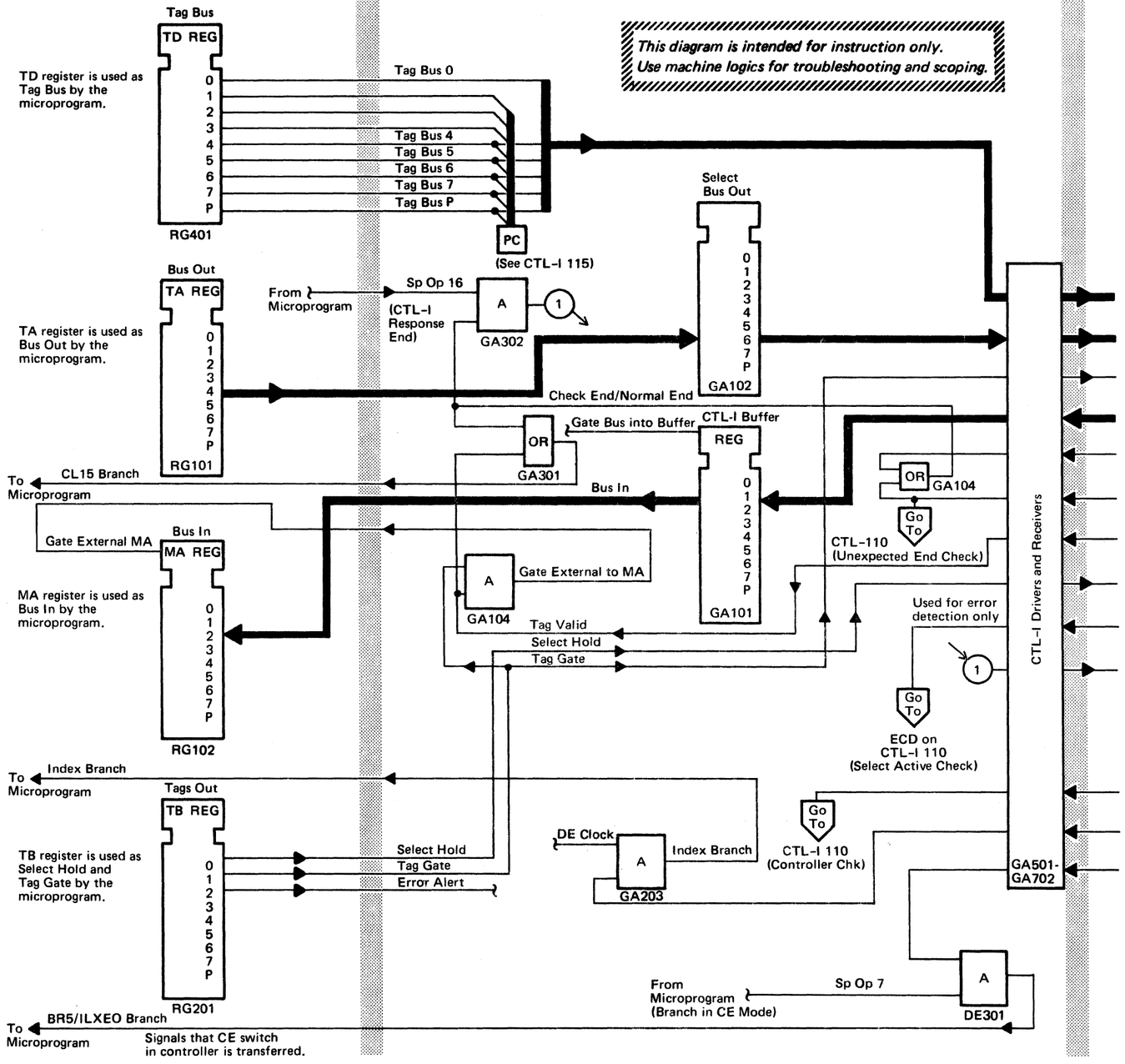
Poll Controller Tags





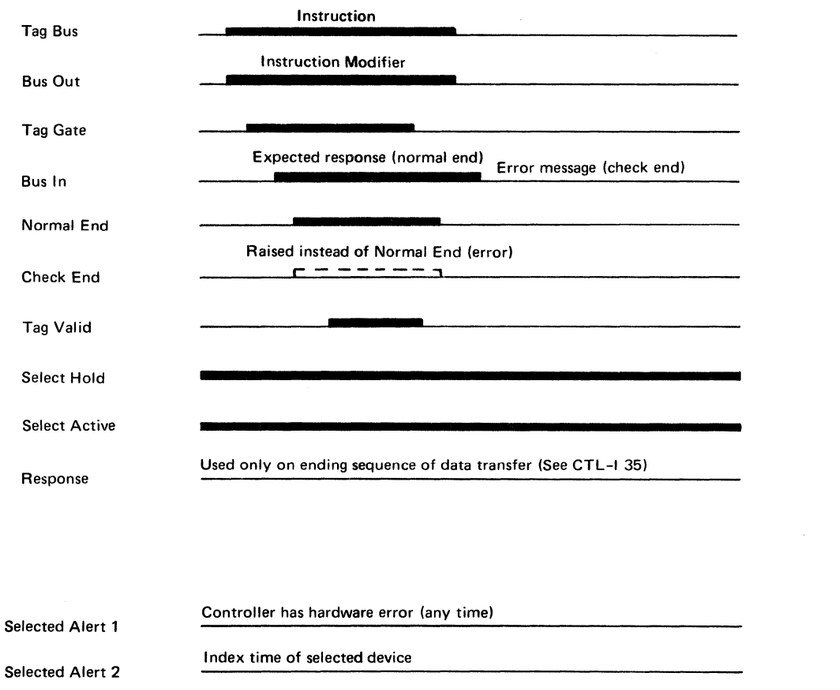
CTL-I IMMEDIATE OPERATION (Flow from/to Device)

CU | CTL-I | FROM/TO DEVICE



Refer to CTL-I 10 for line descriptions.

Immediate Operation Timing Chart



DATA TRANSFER

- Data transfer is initiated by an extended operation tag.
- Data transfer is ended by Normal End (or Check End).
- Many bytes of data are transferred on an extended operation.
- A Write operation is an extended operation (data transfer to device).
- A Read operation is an extended operation (data transferred from device).

A data transfer operation is an extended operation (see CTL-I 15) during which high speed data transfer between the CPU main storage and the device occurs. Many bytes of data transfer one way, either to the device, or from the device.

Because of the high speed of the device, the connection with the channel, CU, and the controller/device will be kept until Normal End (or Check End) from the device is reached. After selection to the controller/device is established, a data transfer instruction is given to the controller/device on tag bus to initiate the extended operation, and data begins to flow.

Two basic instructions with variations of each, handle data transfer.

1. Write (data to the device).
2. Read (data from the device).

WRITE

After selection is made (see CTL-I 20) and the Write instruction (tag bus) initiates the operation (see CTL-I 15 extended operation), a write data transfer (to the device) begins. The data bytes flow from the bus out to the device, byte by byte. The CTL-I and the device are not synchronized, so Sync Out and Sync In are used with buffers (for the data) at both ends of the interface. Sync Out signals the device when the data byte is ready on bus out. Sync In signals the CU that the device is ready for another byte. (See CTL-I 45 for data flow through the CU and CTL-I. Normal End rises at the end of the transfer, stopping data flow, and the CTL-I responds with Response. The CU will disconnect by dropping Select Hold.

If an error with the data occurs during the transfer, Check End rises instead of Normal End to signal the CU and CPU for a retry operation.

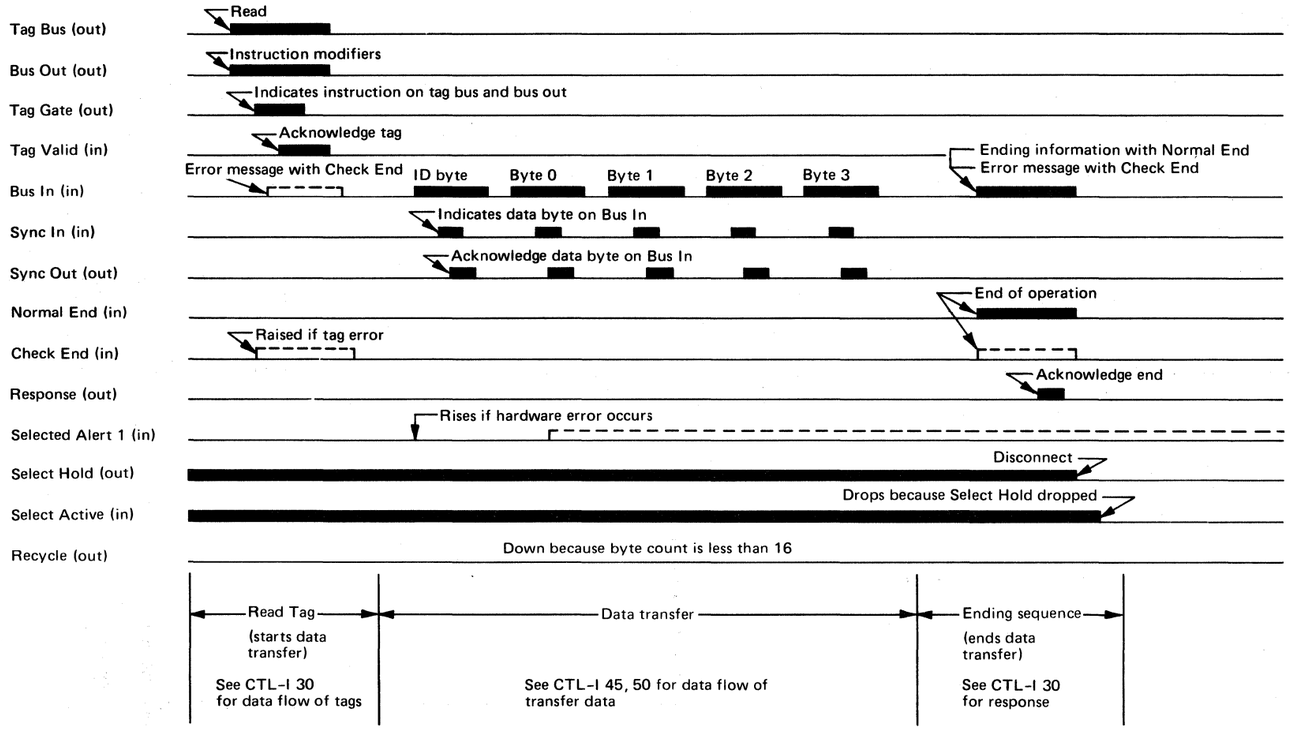
If the controller/device hardware fails during the transfer, Selected Alert 1 comes up immediately, signaling a Check 2 error to the CU. (See CTL-I 110.)

READ

The read data transfer is selected and ended the same as write data transfer. The data flows in the other direction (from the device). Sync In signals the CTL-I that a read data byte is on bus in. Sync Out signals the device that the CTL-I has received the last byte and is ready for another.

Errors are handled the same as in write data transfer and the CPU is notified accordingly.

Data Transfer Operation (Example: Read Data, Four Bytes Plus ID Byte)



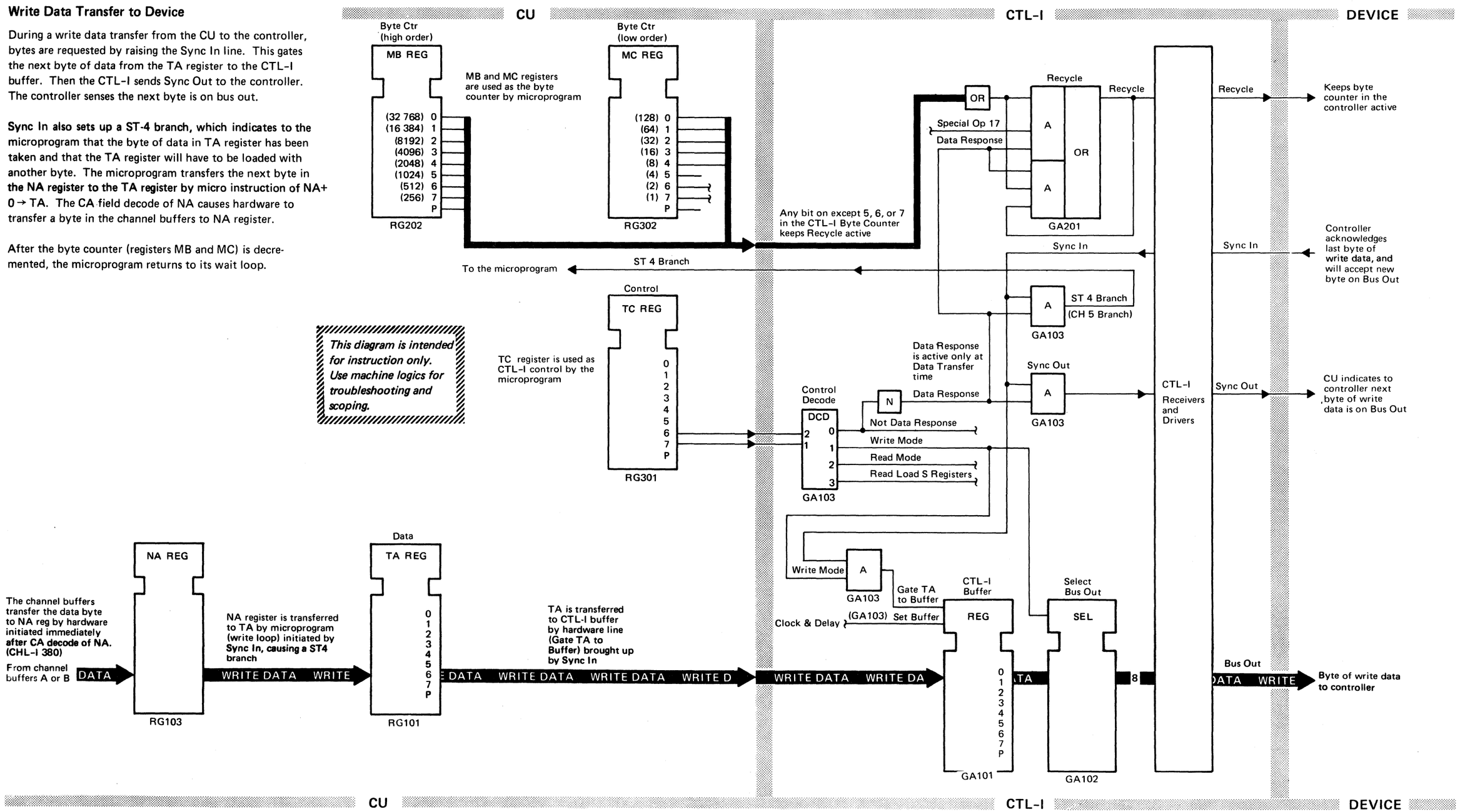
CTL-I EXTENDED OPERATION (Data Flow to Device)

Write Data Transfer to Device

During a write data transfer from the CU to the controller, bytes are requested by raising the Sync In line. This gates the next byte of data from the TA register to the CTL-I buffer. Then the CTL-I sends Sync Out to the controller. The controller senses the next byte is on bus out.

Sync In also sets up a ST-4 branch, which indicates to the microprogram that the byte of data in TA register has been taken and that the TA register will have to be loaded with another byte. The microprogram transfers the next byte in the NA register to the TA register by micro instruction of NA+ 0→ TA. The CA field decode of NA causes hardware to transfer a byte in the channel buffers to NA register.

After the byte counter (registers MB and MC) is decremented, the microprogram returns to its wait loop.



CTL-I EXTENDED OPERATION (Data Flow from Device)

READ DATA TRANSFER FROM DEVICE

During a read transfer from the device to the CU, the controller/device requests the CTL-I to take the read byte on bus in by raising Sync In.

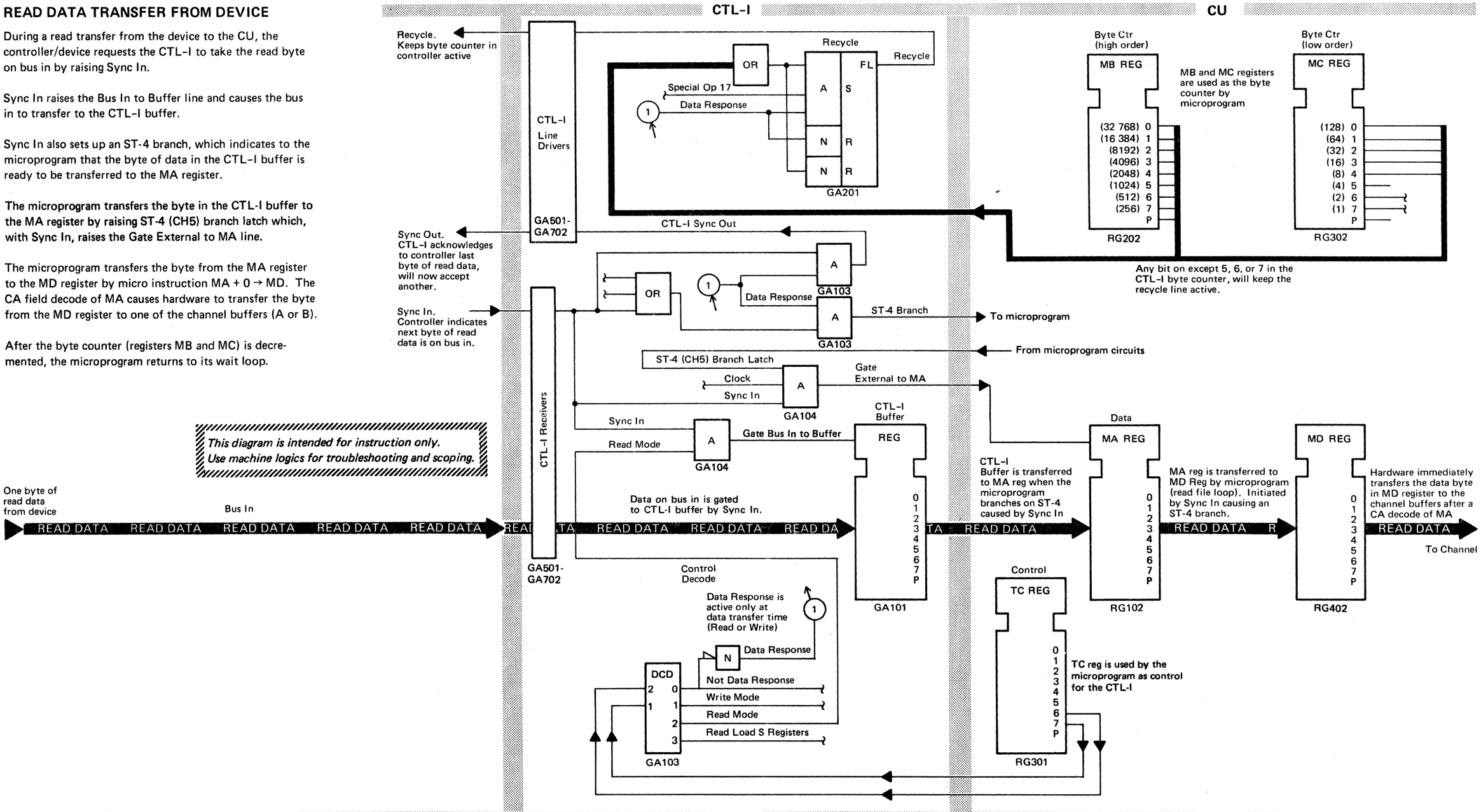
Sync In raises the Bus In to Buffer line and causes the bus in to transfer to the CTL-I buffer.

Sync In also sets up an ST-4 branch, which indicates to the microprogram that the byte of data in the CTL-I buffer is ready to be transferred to the MA register.

The microprogram transfers the byte in the CTL-I buffer to the MA register by raising ST-4 (CH5) branch latch which, with Sync In, raises the Gate External to MA line.

The microprogram transfers the byte from the MA register to the MD register by micro instruction MA + 0 → MD. The CA field decode of MA causes hardware to transfer the byte from the MD register to one of the channel buffers (A or B).

After the byte counter (registers MB and MC) is decremented, the microprogram returns to its wait loop.



This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

CTL-I ERRORS (And Controller Check ECD)

An error detected in either the CTL-I circuits or in the device sets a Check 2 Error in the CU. Special Op 13 sets the error into ND register, and Special Op 14 sets bit 4 into register NA. Selected Alert 1 is an error from the controller and device that is selected at the time of the error. Load S-Register error sets bit 5 in NA register. Compare Assist Check error sets Bit 6 into NA register.

DEVICE

Controller Check (Selected Alert 1)

If the controller detects an error during a control interface operation, it raises Selected Alert 1. If Error Alert is active Controller Check becomes set. Error Alert (TB register bit 2) is kept active during most control interface operations.

DEVICE

Select Active Check (See ECD on CTL-I 115)

If device selection is lost (loss of either Select Active or Select Hold) during a control interface operation when Error Alert (TB register bit 2) is active, Select Check becomes set. Error Alert is kept active during most control interface operations.

CTL-I Buffer Parity Check (See ECD on CTL-I 115)

Each time the CTL-I buffer is loaded, it is checked for correct parity. If parity is incorrect, correct parity is generated for the CU, and the Buffer Parity latch is set. Incorrect buffer parity is expected during some CTL-I operations (for example, polling sequences) and Buffer Parity Error is ignored by the microprogram at these times.

Unexpected End Check (See ECD on CTL-I 115)

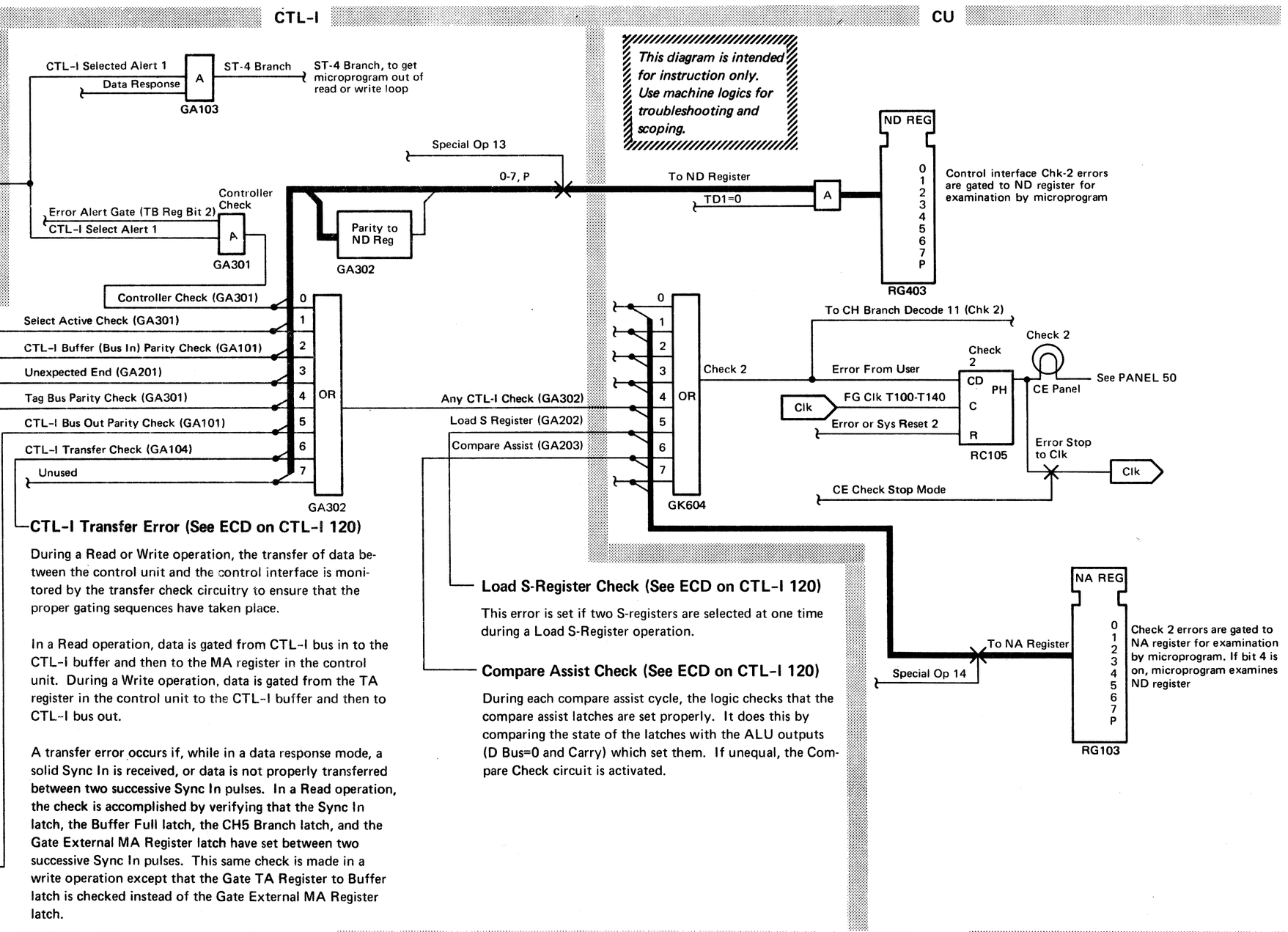
This check occurs if the device attempts to end a data transfer operation prematurely. The check is set if Normal End is received during a Write operation, or if Normal End or Check End is received after the 1st Sync In pulse during a Read operation.

Tag Bus Parity Check (See ECD on CTL-I 115)

The CTL-I tag bus (TP register) is parity checked whenever Tag Gate is raised. If there is an even number of bits, Tag Bus Parity Check is set.

Bus Out Parity Check (See ECD on CTL-I 115)

If an even number of bits is detected in the CTL-I bus out selector (bits 0-7, P), the Bus Out Parity Check latch is set.



CTL-I Transfer Error (See ECD on CTL-I 120)

During a Read or Write operation, the transfer of data between the control unit and the control interface is monitored by the transfer check circuitry to ensure that the proper gating sequences have taken place.

In a Read operation, data is gated from CTL-I bus in to the CTL-I buffer and then to the MA register in the control unit. During a Write operation, data is gated from the TA register in the control unit to the CTL-I buffer and then to CTL-I bus out.

A transfer error occurs if, while in a data response mode, a solid Sync In is received, or data is not properly transferred between two successive Sync In pulses. In a Read operation, the check is accomplished by verifying that the Sync In latch, the Buffer Full latch, the CH5 Branch latch, and the Gate External MA Register latch have set between two successive Sync In pulses. This same check is made in a write operation except that the Gate TA Register to Buffer latch is checked instead of the Gate External MA Register latch.

Load S-Register Check (See ECD on CTL-I 120)

This error is set if two S-registers are selected at one time during a Load S-Register operation.

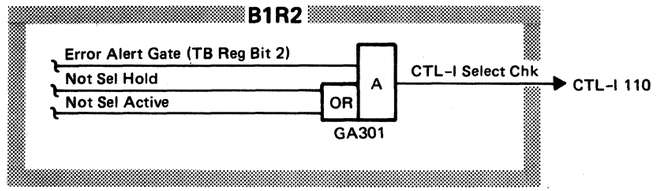
Compare Assist Check (See ECD on CTL-I 120)

During each compare assist cycle, the logic checks that the compare assist latches are set properly. It does this by comparing the state of the latches with the ALU outputs (D Bus=0 and Carry) which set them. If unequal, the Compare Check circuit is activated.

CTL-I ERROR CONDITION DIAGRAMS (Part 1 of 2)

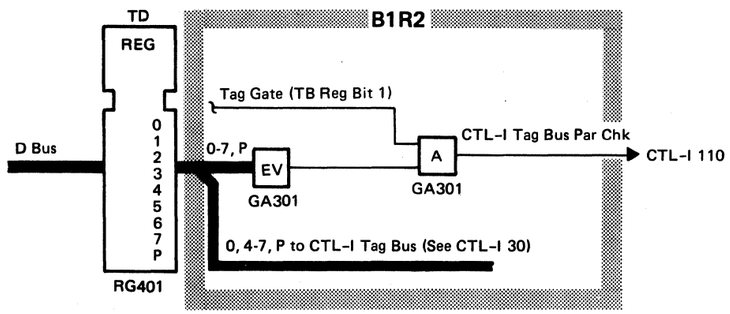
SELECT ACTIVE CHECK

If device selection is lost (loss of either Select Active or Select Hold) during a control interface operation when Error Alert is active, Select Check becomes set. Error Alert (TB register bit 2) is kept active during most control interface operations.



TAG BUS PARITY CHECK

The CTL-I tag bus (TP register) is parity checked whenever Tag Gate is raised. If there is an even number of bits Tag Bus Parity Check becomes set.



BUS OUT PARITY CHECK

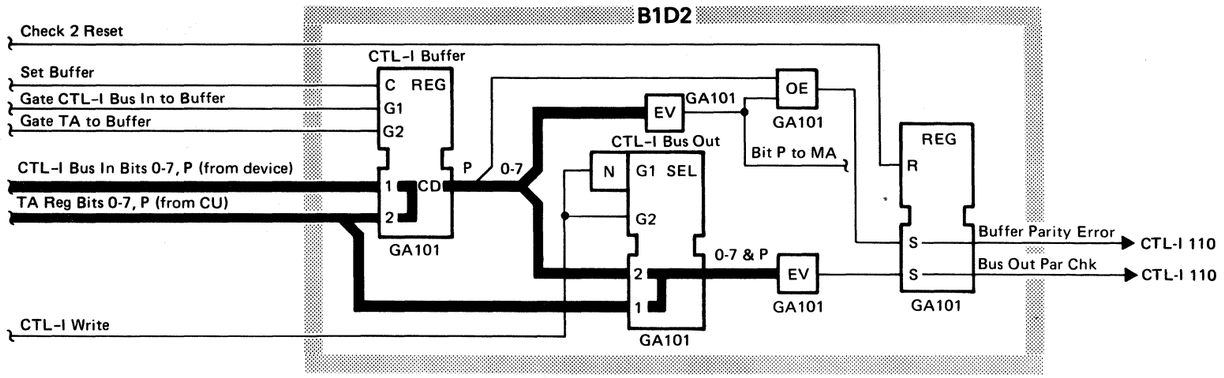
If an even number of bits is detected in the CTL-I bus out selector (bits 0-7 and P), the Bus Out Parity Check latch becomes set. It is reset by Check 2 Reset.

BUFFER PARITY CHECK

Each time the CTL-I buffer is loaded, it is checked for correct parity. If parity is incorrect, correct parity is generated for the CU, and the Buffer Parity Error latch is set.

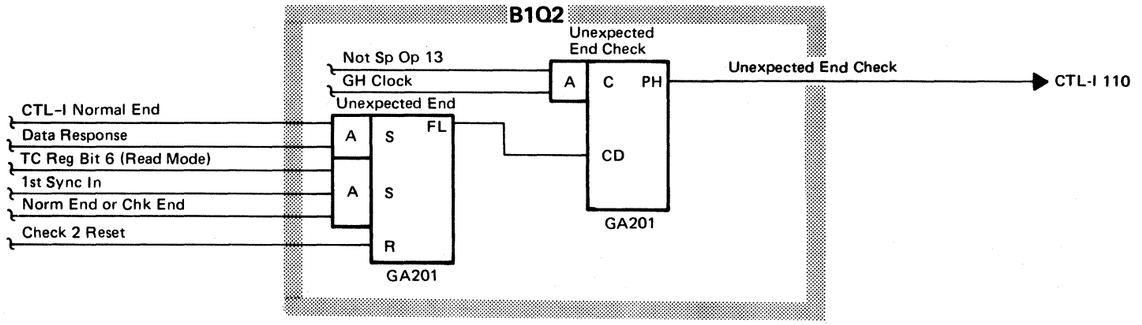
Incorrect buffer parity is expected during some CTL-I operations (for example, polling sequences) and Buffer Parity Error is ignored by the microprogram at these times.

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.



UNEXPECTED END CHECK

An Unexpected End Check occurs if the device attempts to end a data transfer operation prematurely. The check is set if Normal End is received during a Write operation, or if Normal End or Check End is received after the 1st Sync In pulse during a Read operation.



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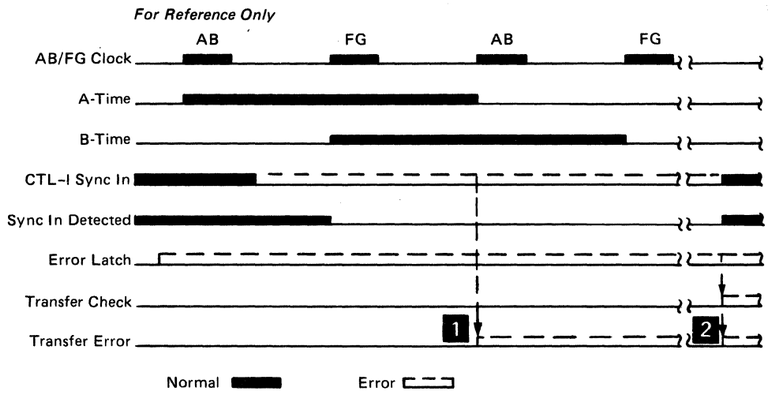
CTL-I ERROR CONDITION DIAGRAMS (Part 2 of 2)

CTL-I TRANSFER ERROR

During a Read or Write operation, the transfer of data between the control unit and the control interface is monitored by the transfer check circuitry to ensure that the proper gating sequences have taken place.

In a Read operation, data is gated from CTL-I bus in to the CTL-I buffer and then to the MA register in the control unit. During a Write operation, data is gated from the TA register in the control unit to the CTL-I buffer and then to CTL-I bus out.

A transfer error occurs if, while in a data response mode, a solid Sync In is received 1, or data is not properly transferred between two successive Sync In pulses 2. In a Read operation, the check is accomplished by verifying that the Sync In latch, the Buffer Full latch, the CH5 Branch latch, and the Gate External MA Register latch have set between two successive Sync In pulses. This same check is made in a Write operation except that the Gate TA Register to Buffer latch is checked instead of the Gate External MA Register latch.



This diagram is intended for instruction only. Use machine logics for troubleshooting and scoping.

COMPARE ASSIST LOGIC

The compare assist logic saves microprogram steps by providing hardware assistance when two fields of data are compared. Comparison is accomplished by subtracting one field from the other, a byte at a time, starting with the high-order byte. After each subtract operation, ALU is examined for a nonzero condition and for the presence of a carry out. From these ALU outputs it can be determined whether the fields being compared are equal or unequal and, if unequal, which field is high.

The logic consists of a two-position register with inputs from ALU (D=0 and Carry), a latch named D Bus Not Zero, and a check circuit.

Each time the microprogram executes a subtract operation (ALU Op 7), the state of ALU is set into the register. If the D=0 position is turned on, the register will be reset on the next machine cycle. If the D=0 position is not turned on, the D-Bus Not Zero latch is set and the register is blocked so that further subtract ops cannot change its contents.

After the last compare cycle, Special Op 24 gates the outputs of the compare assist latches to MB register bits 0 and 1 so that they may be examined by the microprogram. MB bit 1 on indicates that the D-bus was *not* zero. MB bit 0 on indicates that there was a carry.

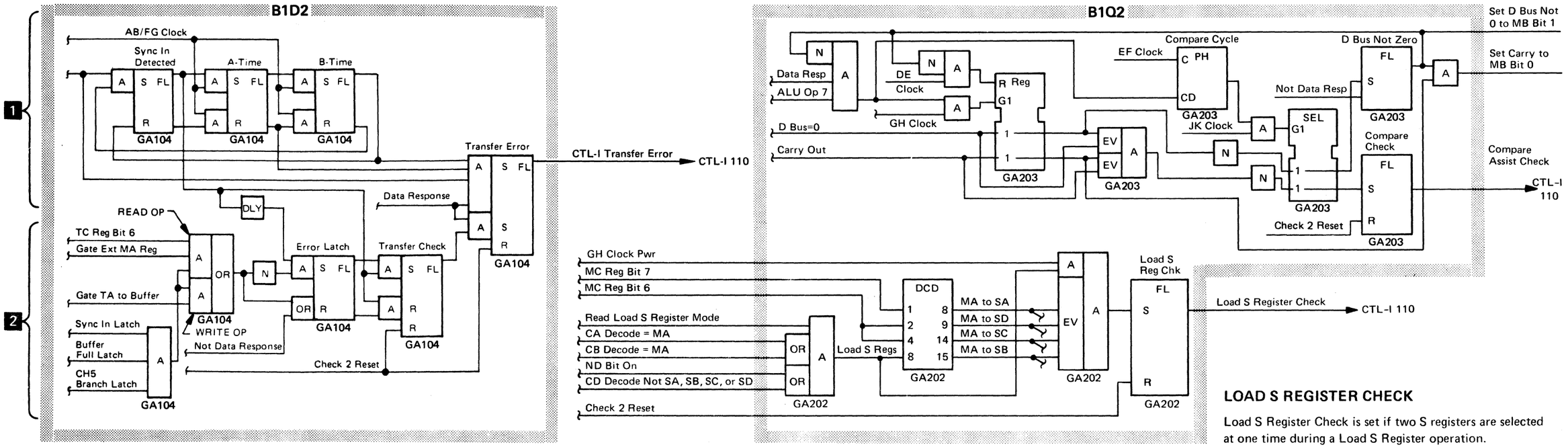
The MB bits are decoded as follows:

MB Register		Decode
Bit 0	Bit 1	
0	0	The two fields are equal
0	1	The field being subtracted is high
1	0	Cannot occur (prevented by hardware)
1	1	The field being subtracted is low

The compare assist logic is reset when the CTL-I logic leaves the data response state.

COMPARE ASSIST CHECK

During each compare cycle, the logic checks that the register latches are set properly. It does this by comparing the state of the latches with the ALU outputs (D Bus=0 and Carry) which set them. If either comparison is unequal, the compare check circuit is activated.



LOAD S REGISTER CHECK

Load S Register Check is set if two S registers are selected at one time during a Load S Register operation.

DEVICE CTL-I CU

LOAD S REGISTER OPERATION

Count and key fields read from the device are placed in the SA, SB, SC, and SD registers under control of CTL-I. At the same time the fields are transferred to the channel. After SD register is loaded, the microprogram causes a store cycle to write one word (four bytes: SA, SB, SC, SD) in control storage. The operation is repeated until the end of the field or 256 bytes have been transferred. The purpose of the Load S-Register operation is to save channel time and CU microprogram time on a retry operation.

LOAD S REGISTER LOGIC

Load S-register logic provides the ability to automatically load the contents of the MA register into the SA, SB, SC, or SD register.

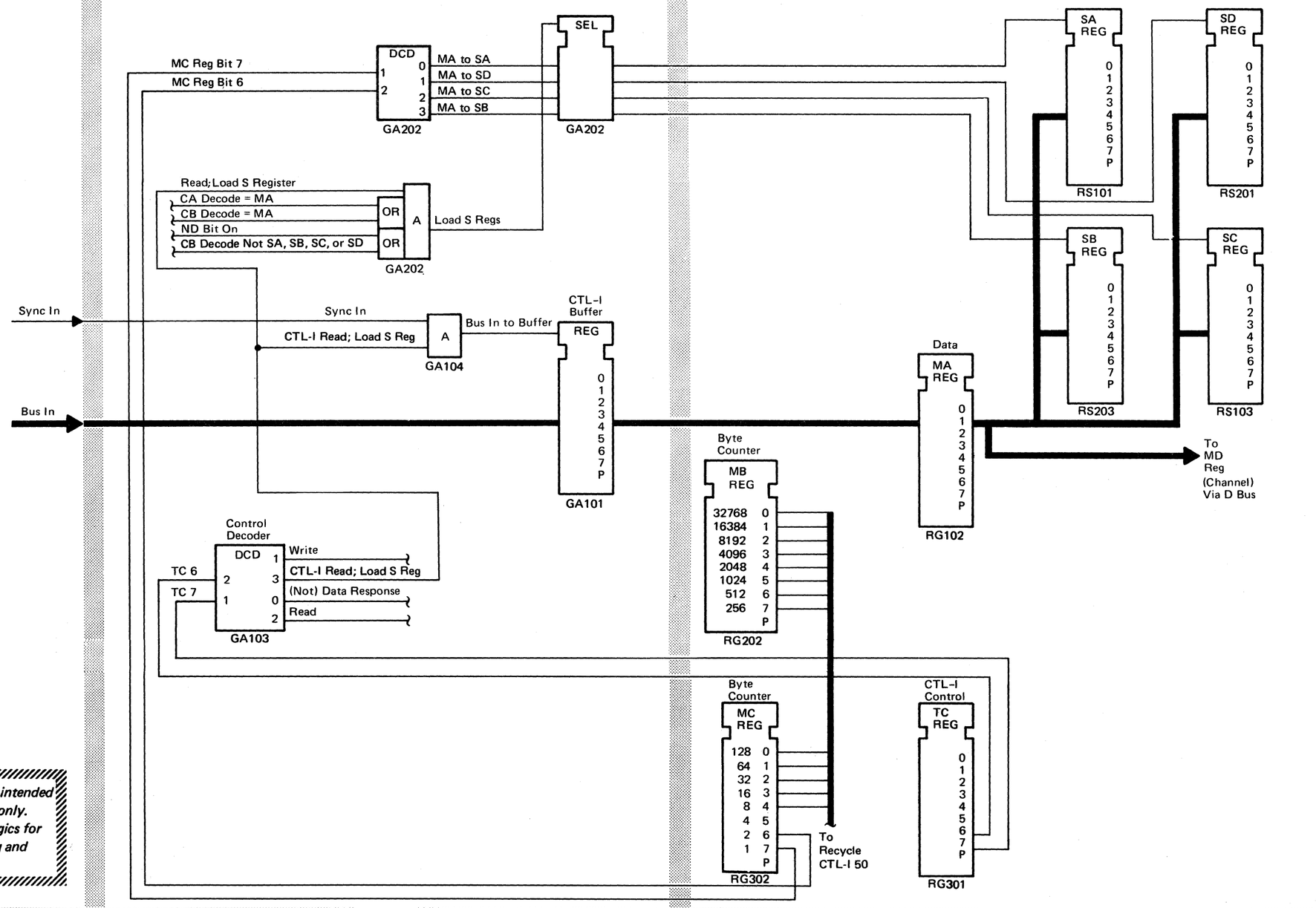
The circuitry is enabled by turning on TC register bits 6 and 7 which decode to become Read; Load S-Register.

Read; Load S-Register causes the control interface logic to function as though it were in read mode. It also automatically loads the S-registers if a microword is executed in which the MA register is gated to either the A bus or B bus *and* the D-bus has no destination (ND bit on), or is gated to any register other than SA, SB, SC, or SD.

The S-register selected depends on the state of MC register (byte counter) bits 6 and 7:

Bit 6	Bit 7	S-Register
0	0	SA
0	1	SD
1	0	SC
1	1	SB

This diagram is intended for instruction only. Use machine logics for troubleshooting and scoping.



DEVICE CTL-I CU