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IBM 7080 Principles of Operation

This manual is a comprehensive presentation of the IBM 7080 Data Processing System. It contains a general system description and detailed descriptions of each instruction; also included are descriptions on: interrupt feature, central storage, and input/output control. Programming examples are also included.

Preface

This manual is a comprehensive presentation of the operation of the IBM 7080 Data Processing System. Its purpose is twofold: (1) to provide a reference and guide for those already familiar with the system, and (2) for use as an instruction aid in the development and training of both operators and programmers. It is assumed that the reader is familiar with the information contained in *IBM General Information Manual, Introduction to IBM Data Processing Systems,* Form F22-6517, *IBM Systems Summary,* Form A22-6775, and *IBM 705 Reference Manual,* Form A22-6506-0.

The first section of the manual is general, and shows system configuration and operating features of the 7080. The CPU General Organization and Functional Logic section details description of system operation and data flow. The Instruction section presents each instruction in two ways: one part briefly presents pertinent information about the instruction; a second part is the description of the instruction in finer detail. The Components section describes the 7080 input-output devices.

The Appendix includes an alphabetic listing of 7080 instructions with their mnemonic codes, operation codes, and page references; 7080 abbreviations; symbols and formulas for calculating instruction execution times; 7080 mode chart; collating sequence; a chart comparing CPU operations for the 705 I, II, III and the 7080; a central storage chart; and a programming example showing the use of interrupt.

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This edition, Form A22-6560-4, obsoletes Form A22-6560-3. However, only an addition to the limiting factors paragraph of the blank memory 01 instruction and a change in the limiting factors paragraph of the set left instruction have been made.

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Contents

IBM 7080 Data Processing System

The IBM 7080 Data Processing System is a high-performance, solid-state data processing system adaptable to both commercial and scientific applications. With a design founded upon proved logical concepts of the IBM 705 systems but also incorporating the most recent advances in technology and machine organization, the 7080 provides many new and improved machine features.

The 7080 system offers instruction compatibility with existing 705 systems, that is, it can process 705 I, II, or III programs unaltered. Thus, a conversion from a 705 to a 7080 can be made with a minimum of effort and expense.

Data Coding

The 7080 processes either alphabetic or numerical information. All information is stored and transferred within the system as binary coded decimal (BCD) characters: letters of the alphabet, numerical digits, and symbols of punctuation and report printing. Data on magnetic tape is also handled in this form.

Data may be read from or punched into IBM cards, or prepared as printed output. Conversion is automatic from cards to BCD coding, or from BCD to card code and printed characters.

The IBM Card

All information in IBM cards is represented by punching small rectangular holes in predetermined positions (Figure 1). The card is divided into two main areas: the lower (numerical) section and the upper (zone) section.

The numerical section is further divided into ten horizontal rows, one row for each digit 0-9. The zone section is divided into three horizontal rows: 0, 11, and 12. Note that the zero row is common to both zone and numerical sections.

The standard IBM card is also divided into 80 vertical columns. To record data, a character is represented by punching one or more holes in a single column. Thus, as many as 80 characters may be punched in one card.

Holes punched in their proper rows and in specified columns can be automatically identified as characters by card readers and by other IBM card equipment attached to the 7080. Digits are represented by single holes punched in the numerical sections; letters and special characters, by combinations of zone and numerical punching.

For example, the 12 zone with one of the digits 1-9 represents the letters A-I; the 11 zone with the digits 1-9, the letters J-R; the 0 zone with the digits 2-9, S-Z.

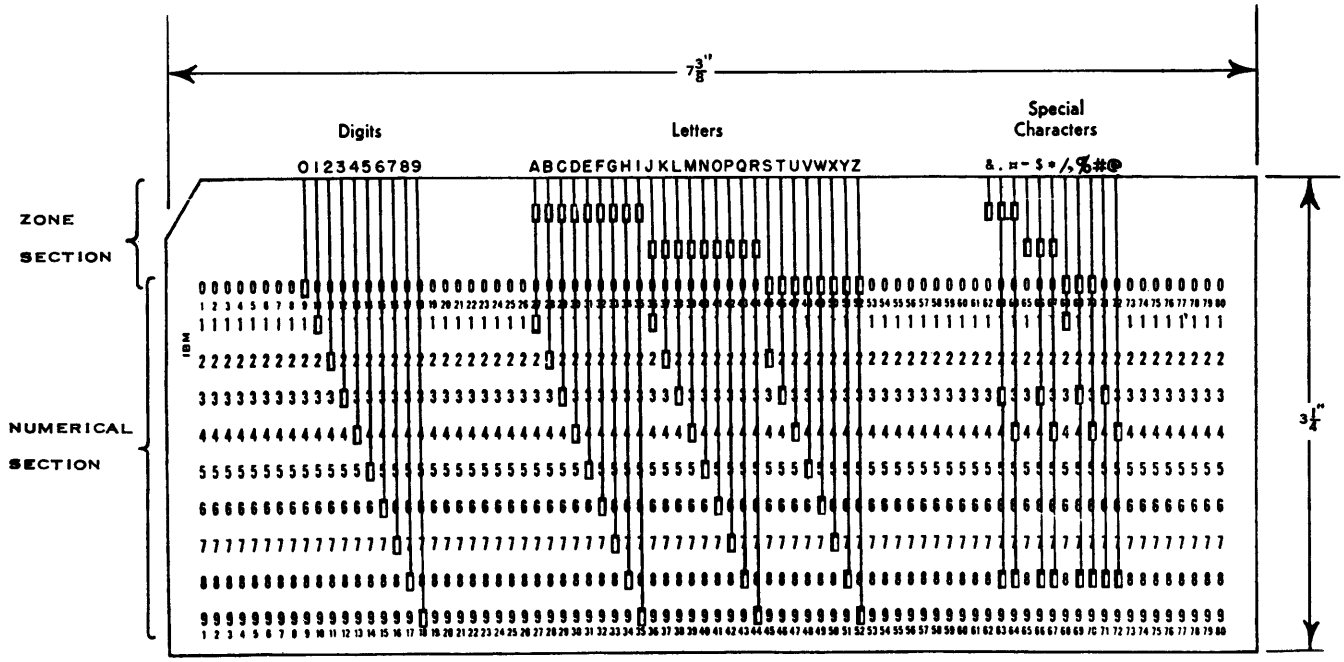


Figure 1. IBM Card Character Coding

Eleven special characters are represented by either single zone punches or combinations of zoning and multiple digit punching.

Binary Coded Decimal

The BCD character code is divided into seven positions or bits, each of which may represent either a 1 or a zero (Figure 2).

Each of four positions is assigned a numerical value of 8, 4, 2 or 1 according to the conventional system of binary notation. The digits 1-9 are represented as binary numbers by bits in these positions, as shown in the following table. A zero is represented as 1010, the binary number ten.

DECIMAL	BINARY 8421 (Place Value)
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
0	1010

Two positions indicate zones corresponding to the zoning in the IBM card. Zones are numbered in binary as 00 for no zone, 01 for zero zone, 10 for the eleven zone, and 11 for the twelve zone. Combinations of zone and numerical values represent the letters of the alphabet, special characters, and other symbols used by the 7080 to mark the ends of fields, records, or blocks of data.

The eleven and twelve zones (10 and 11) are also used to indicate the algebraic sign of fields, quantities, and the sign (plus or minus) of digits. The eleven zone signifies minus; the twelve zone, plus. The code configuration of a signed digit may thus correspond to a letter of the alphabet. For example, the code for +1 is the same as the code for the letter A. The correct interpretation of the character by the machine depends upon whether or not instructions are given to handle the information as alphabetic or numerical data.

The seventh position is used to check the validity of the character. The total number of 1's representing any character, including the check position, should always be even.

For example, the code for the letter L is 10 0011, using an odd number of 1's. Consequently, the complete code for L, with the check 1 added, is 1 10 0011. The code for the letter M is 10 0100, using an even number of 1's. No check 1 is added. The complete code for M then becomes 0 10 0100.

The zone and check positions of the code are also referred to as the A, B and C positions.

The 7080 System

The basic IBM 7080 Data Processing System (Figure 3) is made up of the following units:

IBM 7302 Core Storage (Memory or Core Memory): Model 1 provides 160,000 character positions and Model 2 provides 80,000 character positions.

IBM 7102 Arithmetic and Logical Unit: The arithmetic and logical unit (ALU) is the control center of the system. It contains the machine components and circuitry that select and execute instructions from core memory and operate the system as a single integrated machine. The ALU is composed of two physical frames. These two frames and the 7305 are placed immediately adjacent to one another when installed, giving the appearance of a large single unit.

IBM 7305 Central Storage and I-O Control: The 7305 contains three banks of central storage (banks 0, 1, and 3) and two banks of communication storage (banks 2 and 4).

The 7305 is available in two models:

Model 1 provides two communication channels in bank 2 to attach either model of the IBM 7621, Model 2 or Model 4. It also provides as many as six communication channels in bank 4 to be used in conjunction with the IBM 7908 Data Channel.

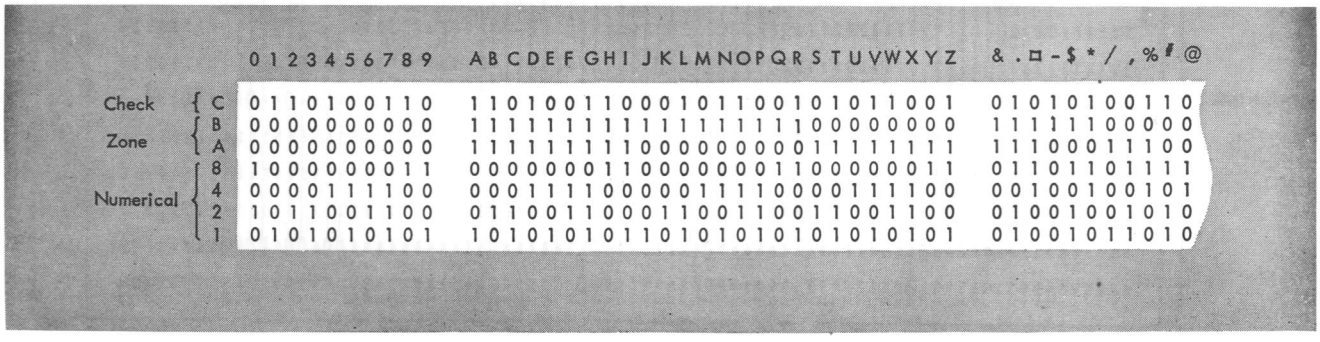


Figure 2. Binary Coded Decimal

Model 2 provides four communication channels in bank 2 to attach two of either models of the IBM 7621, Model 2 or Model 4, or one of each model. It also provides as many as six communication channels in bank 4 to be used in conjunction with the IBM 7908 Data Channel.

IBM 7908 Data Channel: The 7908 Data Channel, in conjunction with bank 4 of the 7305, provides as many as six additional channels (40, 41, 44, 45, 46, and 47) to permit the attachment of additional I-O units to the 7080 system. Channels 40 and 41 are high-speed channels. The 7908 contains the necessary paths, controls, and buffers for the transmission of data between the 7080 and the attached I-O units.

IBM 7153 Console: The console is equipped with keys, lights, and switches that provide manual control of the system. A typewriter is attached to print direct output from memory.

A maximum of 89 characters can be typed on a line by the typewriter.

System Components

A number of control and input-output units may be attached to the basic 7080 system, as shown in Figure 3.

IBM 7621 Tape Control: The 7621 Tape Control provides for the attachment of IBM 729 Magnetic Tape Units to the 7080 system. The 7621 is available in two models:

Model 2 provides for the attachment of IBM 729 II or IV Magnetic Tape Units. The tape control provides the power and serves to control data flow between the tape units and the two communication channels of the 7305. As many as twenty 729 II's or IV's, in any combination, may be attached to the tape control, up to ten tape units to each communication channel. Reading and writing of tape records can be performed simultaneously on separate channels.

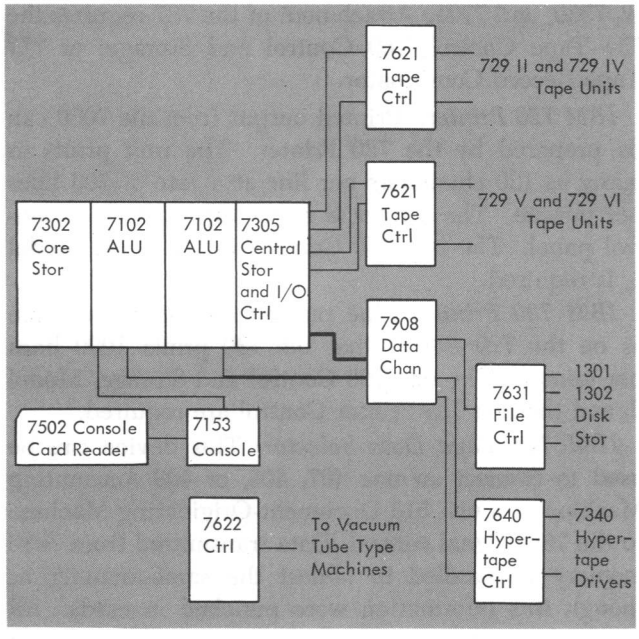


Figure 3. IBM 7080 System Layout

Model 4 provides for the attachment of IBM 729 V or VI Magnetic Tape Units. This control is similar to the Model 2, except that, in addition, it has a manually controlled three-position tape density option switch for each of the two communication channels to establish the recording densities of the attached tape units. The three switch positions correspond to the following densities:

I. 556-800 characters per inch

II. 200-800 characters per inch

III. 200-556 characters per inch

As many as twenty 729 V or VI tape units, in any combination, may be attached to the tape control, with ten tape units to each channel.

IBM 729 II and IV Magnetic Tape Units: These units read or write magnetic tape data in the BCD character coding of the 7080 system. Tape speed on the 729 II is at the rate of 75 inches per second; on the 729 IV, speed is 112.5 inches per second. Record density may be 200 or 556 characters to the inch on either model.

Density can be program-controlled by the 7080 to provide a maximum character reading or writing rate of either 15,000 or 41,667 characters per second on the 729 II and either 22,500 or 62,500 characters per second on the 729 IV.

IBM 729 V and VI Magnetic Tape Units: The 729 V and VI are similar to the 729 II and IV, respectively, except that the 729 V and VI can operate at any one of three record densities: 200, 556, or 800 characters to the inch. Tape speed for the 729 V is 75 inches per second; for the 729 VI, 112.5 inches per second.

Density can be controlled to provide a maximum character reading or writing rate of 15,000 or 41,667 or 60,000 characters per second on the 729 V, and 22,500 or 62,500 or 90,000 characters per second on the 729 VI.

Tapes prepared at a density of 200 characters to the inch can be read by the IBM 727, 729 I, II, IV, V, or VI, or 7330 Magnetic Tape Units and the IBM 7701 Magnetic Tape Transmission Terminal.

IBM 7631 File Control: One or two file controls are used to attach one to five IBM 1301 or 1302 Disk Storage Units to the 7080 system. This unit serves to control and synchronize the flow of data between disk storage and the 7080 system. A maximum of five 1301's

or 1302's can be attached, in any combination, to one or two 7631 file controls. Three models of the 7631 are available with the 7080: Model 2, normally used with one 7080 system; Model 3, for shared use with an IBM 1410 Data Processing System; Model 4, for shared use with another 7080 system or with any other IBM 7000 series system.

These units are connected to the 7080 system through the 7908 Data Channel. Each 7908 channel may have one 7631 attached to it.

IBM 1301 Disk Storage: The 1301 is a random access storage device that provides large capacity, low access time, high reliability, and advanced operational characteristics. The 1301 has a character rate of 90,000 characters per second and record lengths of as many as 2,800 characters, and stores as many as 56,000,000 characters per disk storage.

IBM 1302 Disk Storage: The 1302 is similar to the 1301 but the character rate is 184,000 characters per second, maximum record length is 5850 characters, and maximum storage capacity is 234,000,000 characters per disk storage.

IBM 7640 Hypertape Control: The 7640 Hypertape Control attaches the IBM 7340 Hypertape Drives to the 7080 system through the 7908 Data Channel. The Hypertape control controls and synchronizes data flow between the data channel and the Hypertape drives. The 7640 controls two channels. Each channel controls as many as ten Hypertape drives, providing for the attachment of a maximum of 20 Hypertape drives.

IBM 7340 Hypertape Drive: This unit reads or writes magnetic tape eight-bit character code. Translation of six-bit BCD code to and from eight-bit character code is performed by the 7908 Data Channel. The Hypertape system provides for error correction and complete error detection. Tape speed is 112.5 inches per second, record density is 1511 characters per inch, and the character rate is 170,000 characters per second.

The drive can also read the tape while it is moving backward (backward read).

The Hypertape drive uses a cartridge for tape handling. The cartridge minimizes tape load and unload time, permits unloading without rewinding at any point in the tape, and protects the tape from damage caused by tape handling and from contamination from foreign particles.

IBM 7502 Console Card Reader: IBM cards are read serially, from column 1 to column 80, at a single read station where punched holes are sensed photoelectrically. Reading speed is at the rate of 60 cards per minute. Cards may be punched in any arrangement of digits, letters of the alphabet, or special characters acceptable to the 7080.

IBM 7622 Signal Control: This unit converts the signal level of the input-output units available with the IBM 705 I and II Data Processing Systems to transistor signal levels, and vice versa. Figure 4 is the schematic of the maximum combination of 705 input-output units that can be connected to the 7080 system through the 7622. Any practical number of such devices, as described below, can be used.

IBM 714 Card Reader: Data punched in standard IBM cards may be placed in 7080 memory by the card reader. The unit operates at a speed of 250 cards a minute. Card information is selected and arranged by a control panel that may be altered by the use of external control panel wires. The IBM 759 Card Reader Control is required.

IBM 722 Card Punch: The card punch may be used to prepare IBM cards as output records from 7080 memory. Information is punched at a rate of 100 cards per minute. The unit is not equipped with a control panel. The IBM 758 Card Punch Control is required.

IBM 717 Printer: Printed output from the 7080 can be prepared by the 717. The unit prints as many as 120 characters per line at the rate of 150 lines a minute. The printer is not equipped with a control panel. The IBM 757 Printer Control is required.

IBM 727 Magnetic Tape Units: These units read or write magnetic tape data in the BCD character coding of the 7080 system. Tape speed is 75 inches per second with a character density of 200 characters to the inch. The maximum character rate for reading or writing is 15,000 characters per second. Tapes written by the 727 can be read by the IBM 729 I, 729 II, 729 IV, 7330, and 7701. Attachment of the 727 requires the 754 Tape Control, 760 Control and Storage, or 777 Tape Record Coordinator.

IBM 720 Printer: Printed output from the 7080 can be prepared by the 720 Printer. The unit prints as many as 120 characters per line at a rate of 500 lines per minute. The printer is not equipped with a control panel. The IBM 760 Control and Storage, Model 1, is required.

IBM 730 Printer: The printed output is the same as on the 720 except that the 730 prints 1000 lines per minute. The IBM 760 Control and Storage, Model 2, and the IBM 735 Printer Control are required.

IBM 774 Tape Data Selector: This device can be used to connect an IBM 407, 408, or 409 Accounting Machine or a IBM 519 Document-Originating Machine to the 7622 signal control. Data transmitted from 7080 memory is handled in almost the same manner as though this information were punched in cards. All units are equipped with control panels that provide for selecting, arranging, accumulating and manipulat-

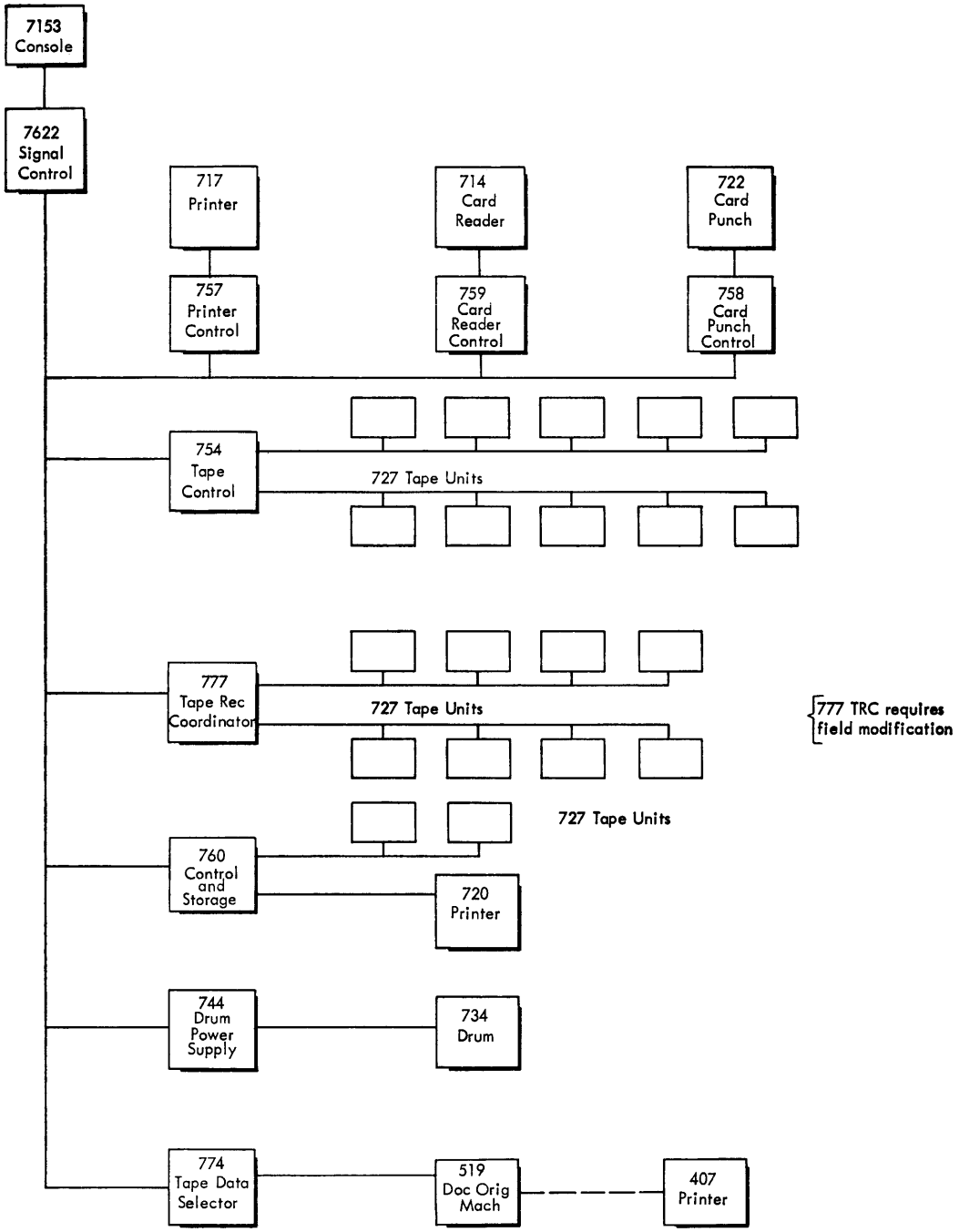


Figure 4. IBM 7080 System Diagram, 705 Input-Output Units

ing the memory data as card records. The IBM 747 TDS Power Supply is required.

IBM 734 Magnetic Drum Storage: Storage capacity of the 7080 system can be supplemented by using the 734 Magnetic Drum. Each drum has 300 addressable sections; each section can store as many as 200 characters. Average access time to a drum section is eight milliseconds. Thereafter, characters can be read or written consecutively at a rate of 40 microseconds per character. The IBM 744 Magnetic Drum Power Supply is required.

Instructions

All operations of the 7080 are controlled by fixed length instructions of five characters each. Instructions are stored in core memory and then interpreted and executed by the central processing unit. An instruction is divided into two parts, a single-character operation code and four-character operand (Figure 5).

The operation code designates the operation to be performed, such as read, write, add, or subtract. The operation code is stored as a BCD character that conforms to the established coding structure for digits,

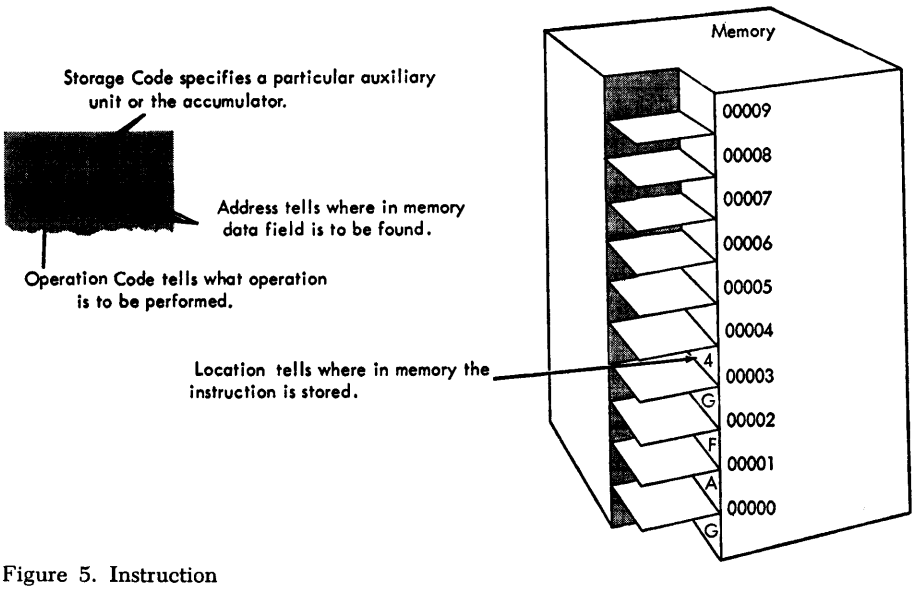


Figure 5. Instruction

letters, and symbols. For example, the letter Y means read; the letter R, write. The character is always the high-order (leftmost) position of the instruction.

Depending upon the operation code, the operand indicates a storage or memory location, a machine component, or a control function. The operand characters also conform to the BCD coding structure, but in many cases the zone portions are interpreted separately as binary numbers. In this way, as many as 160,000 memory locations can be addressed by using combinations of zones with four digits. The operand specifies a memory address and a central storage location (Figure 5).

Instructions must always be stored in memory so that the low-order (rightmost) position is placed in a location *with an address ending in 4 or 9.* There is no distinction between data and instructions in memory except that information read during instruction cycles (I time) is interpreted as instructions while information read during execution cycles (E time) is interpreted as data.

An instruction can be treated like any alphabetic or numerical field of data. One instruction can change another by directing the machine to compute an address or to otherwise modify the operand. The operation code can be changed by computation, or a new operation code can be substituted.

Stored Program

The IBM 7080 is a stored-program computer. Instructions are selected sequentially by the central processing unit from ascending locations of core memory. However, the sequence of selection is variable and can be controlled by conditional or unconditional transfer instructions. The sequence is also under control of priority processing or interrupt signals.

Execution of instructions may overlap, depending upon the operations involved. Computing or internal data transmission may occur simultaneously with reading and writing on channels.

No particular areas of memory are reserved exclusively for the program. The location of instructions, constants, or data to be processed is entirely at the discretion of the programmer.

Compatibility

The 7080 can operate as any one of three systems: 705 I-II, 705 III, or 7080 using programs prepared for any of the three systems. This program compatibility, however, assumes normal instruction usage and that the proper I-O units are available.

A 705 I-II switch and a 40K memory size switch are provided on the console for 705 compatibility and memory size. Their settings are shown below.

705 I-II SWITCH	40K MEMORY SIZE SWITCH	MODE	MEMORY SIZE
On	Off	705 I	20,000 positions
On	On	705 II	40,000 positions
Off	On	705 III	40,000 positions
Off	Off	705 III	80,000 positions

A mode chart in the Appendix lists and describes the various modes of operation and explains the methods of entering and terminating each mode.

705 I-II Mode

The 705 I-II compatibility switch establishes this mode. When the switch is on, the 7080 operates in-

ternally as a 705 I-II until program-instructed to enter the 7080 mode. Therefore, programs written for the 705 I or II require little or no modification to operate in the IBM 7080.

1. All 705 I-II input-output units must be connected to the central processing unit through the 7622 signal control.

2. All transfer instructions function exactly as they do in the 705 I or II. The 705 III transfer instructions with zoning over the tens and hundreds positions of the operand are deactivated. Operations such as add and subtract are terminated in the same manner as in the 705 I or II.

3. Indirect addressing, a feature of the 705 III, does not apply. Zoning over the units position of an instruction operand is ignored.

4. If the 40K memory size switch is off, the size of memory available to the program is restricted to 20,000 positions. If it is on, 40,000 positions are available.

5. Communication channels may not be selected.

6. Comma instructions give an operation check (00900).

7. Internal processing is carried out at the speed of the 7080.

705 III Mode

When the 705 I-II compatibility switch is off, the 7080 operates internally as a 705 III until program-instructed to enter the 7080 mode. Therefore, programs written for the 705 III will operate in the 7080 with little or no modification.

1. The 729 II or IV tape units, a 7621 tape control, and a communication channel are substituted for the 729 I or III tape units and a 767 data synchronizer. Complete 705 III program compatibility is maintained regardless of this substitution of tape units and controls. The function of a 767 data synchronizer is simulated by communication storage and a communication channel in the 7305.

2. All 705 III transfer instructions are activated.

3. The indirect method of addressing is activated and zoning over the units position of an instruction address is treated in the same way as in the 705 III.

4. If the console 40K memory size switch is off, the size of memory available to the program is restricted to 80,000 positions. If this switch is on, 40,000 positions will apply.

5. Comma instructions give an operation check (00900).

6. The internal processing is carried out at the speed of the 7080.

7080 Mode

When the system is instructed to enter the 7080 mode, all the existing features of the 705 systems are available, together with the features of the 7080.

1. The capacity of memory is 160,000 positions for the 7302 Model 1, 80,000 positions for the Model 2, regardless of the settings of the console switches.

2. Wrap-around of the memory address counters and the instruction counter will always be at 160,000 positions, in 7080 mode.

When there are only 80,000 positions of memory, instruction addresses between 80,000 and 159,999 are treated as though they were between 0 and 79,999.

3. The A bit in the units position of an instruction address specifies the memory locations 80,000 to 159,999, not indirect addressing.

4. The address modification instructions automatically handle the six-digit addresses of the 160,000 position memory.

I-O Interpret Feature

The I-O interpret feature operates in conjunction with modified conversion program, INT 580. The feature is under control of the I-O interpret switch on the console and is normally used with the 00900 switch in automatic and the non-stop switch on. The feature (in addition to normal interrupt conditions) causes a 00900 check to occur for the following instructions to force and interrupt to the address specified by interrupt word 250:

Read
Write
Write Erase
Read while Writing
Transfer on Signal
Any Control Instruction (except Enter Eighty Mode)

The limitations imposed on this feature are:

1. In the 705 II or III mode, the address of an alteration switch, program check switch, or the typewriter in the select register prevents the 00900 check or the interrupt for the above conditions.

2. In the 705 II or III mode, a select instruction address, other than those mentioned in 1., allows an interrupt for the instructions listed above.

3. In the 705 III mode, in addition to conditions of 2., exceptions causing an interrupt include the transfer-on-signal instruction with ASU coding 04-15. For information and special considerations in the use of INT 580, refer to publications listed in the *IBM 7080 Bibliography*, Form A22-6774.

Priority Processing

Priority processing in the 7080 system furnishes a means of determining the sequence of two or more operations that request the use of memory, storage, or both at the same time. The priority system:

1. Determines which operation can use memory if two or more operations want to use it at the same time.
2. Determines which operation can use storage if two or more operations want to use storage at the same time.
3. Determines when and if the operation in progress can be interrupted by a new operation that wants to use memory (or storage).
4. Determines the sequence in which automatic interrupts will be taken if two or more interrupts occur simultaneously or the automatic interrupts are awaiting processing.

In addition to the above, if the same operation wants to use memory, storage, or both memory and storage, but is prevented from doing so by the priority system, the further progress of this operation is delayed.

Interrupt

The interrupt feature of the 7080 permits several simultaneous operations, eliminating any lost time waiting for an operation to be completed. For example, CPU can initiate a communication channel operation, then continue processing the main program while the channel operation is taking place. At the completion of the channel operation, the I-O device sends an interrupt signal to CPU, resulting in a transfer to a subroutine whose address is specified by the channel interrupt word.

Interrupts result from:

1. The completion of a communication channel operation.
2. Nonstop condition.
3. The manually controlled console interrupt keys.

There is an interrupt word for each channel, one for the nonstop feature (250), and one for each of the three console interrupt keys (251, 252, and 253).

To activate the interrupt feature, the enter interrupt mode (EIM) instruction must be executed. The system remains in the interrupt mode until the leave interrupt mode (LIM) instruction is executed or by depressing one of the following keys: clear memory, auto-load, or reset.

An interrupt signal is sent to CPU at the completion of any of the following operations:

Read 00
Read 01
Write 00 (except a write to a group mark)
Write 01
Backspace 00
Backspace 01
Skip
Write a Tape Mark

An interrupt also takes place to interrupt word 250 when a nonstop interrupt condition is encountered, the nonstop switch is on, and CPU is not operating in an interrupt program.

An interrupt takes place to interrupt word 251, 252, or 253 when the correspondingly numbered console interrupt key is depressed.

An interrupt will not take place for the following operations (when used with the 7621), although any such operations must be completed before CPU can proceed to the next instruction.

Read 02
Write 02
Set Density High
Set Density Low
Turn on I-O Indicator
Turn off I-O Indicator

The following operations, when used with the 7621, will not cause an interrupt, but will release CPU after they are initiated (that is, these operations will be performed while CPU proceeds with the main program):

Read 03
Write 03
Rewind
Rewind and Unload

Read 03 and Write 03 will cause an interrupt when performed through the 7908.

Memory and Memory Addressing

Memory is a core storage device containing a specific number of character locations. When the system is operating in the 705 I-II or 705 III mode, the capacity of memory available to the program is determined by the setting of the memory size switch. Memory capacity is thus made compatible with these systems. In the 7080 mode, the capacity of memory is 160,000 positions for the 7302 Model 1 and 80,000 positions for the 7302 Model 2.

Each memory location is assigned a numerical address from zero to the end of the particular memory: 19,999, 39,999, 79,999, or 159,999. Zoning over the high- and low-order positions of the instruction operand are used to specify locations with addresses that are more than four digits in length. The A and B zones over the high-order position of the operand

have decimal values of 10,000 and 20,000, respectively; A and B zones over the low-order position have values of 80,000 and 40,000, respectively (Figure 6). The decimal values of the zones are added to the numerical portion of the operand by addressing circuitry of the CPU to produce a five- or six-digit memory address as required. A chart of numerical memory addresses with equivalent four-character coding is shown in Figure 6.

Hereafter this manual will refer to all positions of memory with either a five or six-digit address, depending upon the size of memory to be discussed. That is, memory address 525 will appear either as 00525 or 000525, 73525 either as 73525 or 073525. Exceptions will be illustrations where attention must be drawn to the zone structure of the characters. In such cases, zones will be shown above the digits as in Figure 6. where the B zone 1 or 0 is followed by the A zone 1 or 0. Thus, the address 73525 will be shown as $\overset{11}{3}\ 5\ 2\ \overset{10}{5}$.

No specific areas of memory are reserved for either data or instructions; the only distinction is the way in which the stored information is handled by the CPU. Records may be separated or defined by a special character called a *record mark*. The mark may also be used to terminate the transfer of information from one area of memory to another. The information can be either data or instructions.

Actual Memory Address	Four-Character Memory Address	
00000 to 09999	0000	9999
10000 to 19999	$\overset{01}{0}000$	$\overset{01}{9}999$
20000 to 29999	$\overset{10}{0}000$	$\overset{10}{9}999$
30000 to 39999	$\overset{11}{0}000$	$\overset{11}{9}999$
40000 to 49999	$000\overset{10}{0}$	$999\overset{10}{9}$
50000 to 59999	$\overset{01\ 10}{0000}$	$\overset{01\ 10}{9999}$
60000 to 69999	$\overset{10\ 10}{0000}$	$\overset{10\ 10}{9999}$
70000 to 79999	$\overset{11\ 10}{0000}$	$\overset{11\ 10}{9999}$
80000 to 89999	$000\overset{01}{0}$	$999\overset{01}{9}$
90000 to 99999	$\overset{01\ 01}{0000}$	$\overset{01\ 01}{9999}$
100000 to 109999	$\overset{10\ 01}{0000}$	$\overset{10\ 01}{9999}$
110000 to 119999	$\overset{11\ 01}{0000}$	$\overset{11\ 01}{9999}$
120000 to 129999	$\overset{11}{0000}$	$\overset{11}{9999}$
130000 to 139999	$\overset{01\ 11}{0000}$	$\overset{01\ 11}{9999}$
140000 to 149999	$\overset{10\ 11}{0000}$	$\overset{10\ 11}{9999}$
150000 to 159999	$\overset{11\ 11}{0000}$	$\overset{11\ 11}{9999}$

Figure 6. Memory Addressing

The end of a record, a group of records, or a block of information is normally defined by a *group mark*. When information is written from memory by an output device, the group mark can be used to terminate the writing operation by signalling that the end of a specified block of data has been reached.

The record mark is represented by the BCD configuration 1 01 1010; the group mark by 0 11 1111. Each mark occupies one character position.

Central Storage and Storage Addressing

The 7080 is provided with five 256-character banks of storage as shown in Figure 7. Although each of the banks serves a specific function, all are similar in make-up and operation and may be, with limitations, interchanged to perform alternate functions.

Normally, Bank 0 serves as the accumulator (ACC) and Bank 1 serves as auxiliary storage units (ASU), as in the IBM 705 Data Processing System series. Bank 2 and Bank 4 serve as communication storage banks, providing the channel word sets for the attachment of input-output devices. Bank 3 serves as the channel auxiliary storage units (CASU) for Bank 2. *The function performed by any bank is entirely dependent upon the current setting of the starting point counter.* The use of these banks is at the discretion of the programmer within the limitations of the system.

With the starting point counter (see Starting Point Counter instruction) set in:

1. Bank 0, 1, 2, or 3. That bank will serve as the accumulator for all instructions.

2. Bank 0 or 1. Any instruction with ASU coding will specify an ASU in Bank 1.

3. Bank 2 or 3. Any instruction with ASU coding will specify an ASU in Bank 3.

4. Bank 4. Any instruction with no ASU coding will specify Bank 4 as the ACC, and any instruction with ASU coding will specify the ASU in Bank 4. However, any position of Bank 4 that is not an active part of the channel word set will always contain a storage mark.

The banks as shown in Figure 7 illustrate the detailed make-up of central storage. Bank 0 is shown as the accumulator, a 256-character position continuous ring. Bank 1 is shown subdivided into auxiliary storage units. Banks 2 and 4 are shown subdivided into channel word sets. The corresponding shaded word sets are expanded to show the specific assignment of the words of the related word sets. Bank 3 is shown subdivided into the channel word sets to illus-

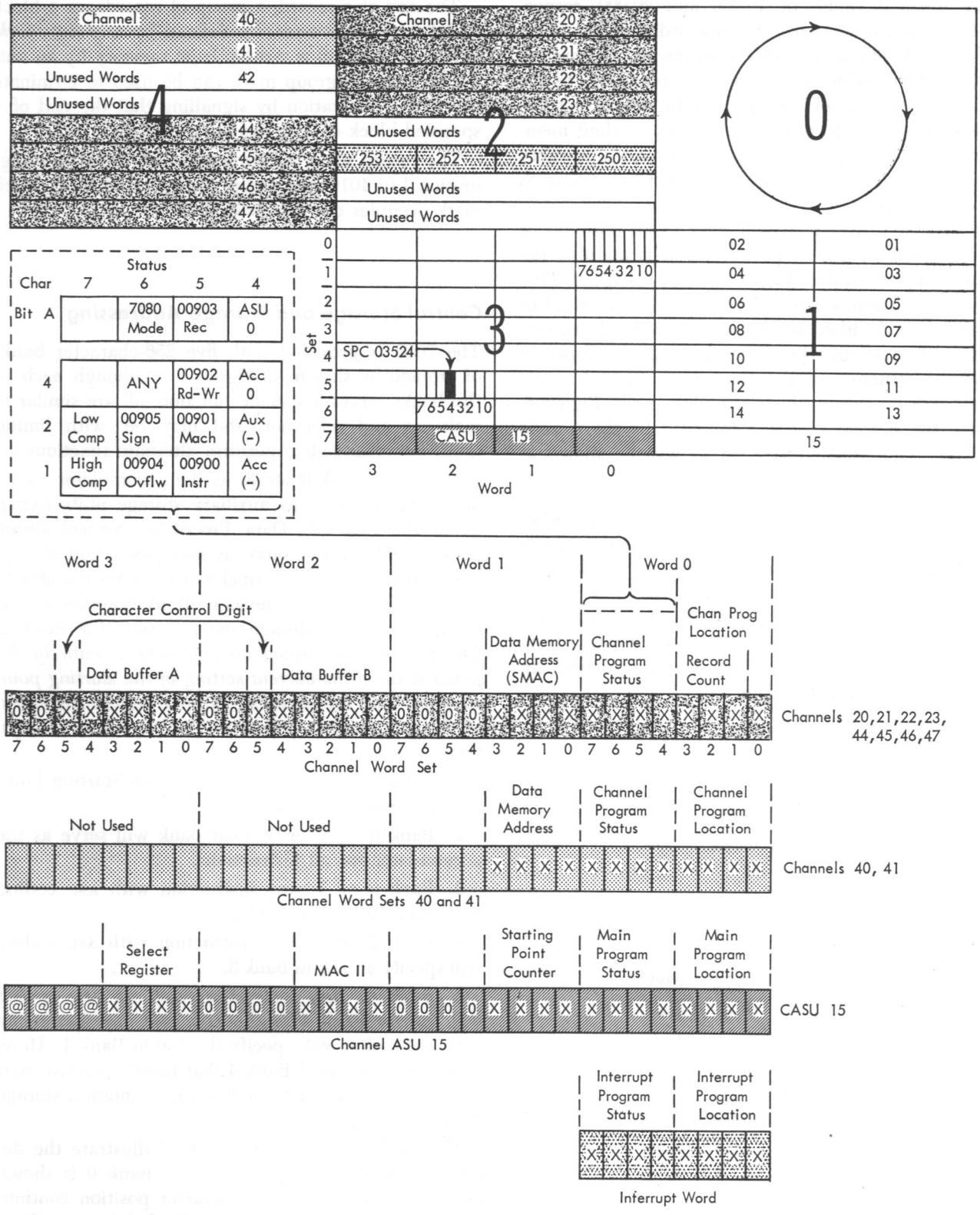


Figure 7. Central Storage Banks

trate the set starting point counter instruction addressing. Example: SPC 3524 sets the starting point counter at the fifth character of word 2 of channel word set 5 in bank 3 as shown in Figure 7.

CASU 15 is also shown expanded to show its specific assignments in the storing of the main program status.

Banks 0 and 1, Accumulator and Auxiliary Storage

Banks 0 and 1 of storage are normally used only as accumulator and auxiliary storage, respectively, in all modes of operation: 705 I-II, 705 III, and 7080. Information from memory is stored temporarily in these small core storage units. Operations may then be performed on this information without changing the original field or record that remains in memory. The various operations are not actually performed by these units, however, but are executed in the arithmetic and logical unit.

The number 00 identifies the accumulator (bank 0) as a single storage unit with a capacity of 256 characters. Bank 1 is subdivided into fifteen auxiliary units identified by the numbers 01 through 15 (Figure 8). Units 01 - 14 have a capacity of 16 characters each; unit 15 has a capacity of 32 characters.

Instructions using or involving accumulator or auxiliary storage must indicate the storage unit to be used. Zone coding (B and A bits) of the characters located in the tens and hundreds positions of the address part of the instruction specify the particular unit. The B and A bits of the character in the tens position have an assigned decimal value of 2 and 1, respectively. The B and A bits of the character in the hundreds position have an assigned decimal value of 8 and 4, respectively. The decimal sum represented by the presence of B and A bits in these two character positions indicates the addressed storage unit (Figure 9).

It will be the practice in this manual to show the ASU indication in parentheses following the address as in ADD 04759(13), unless attention is being drawn to the bits themselves. In this case, the address will be shown as 0 4 $\overset{11}{7}$ $\overset{01}{5}$ 9. Where the zoning over a digit is 00, no zoning will be shown; i.e., 0 4 $\overset{00}{7}$ $\overset{00}{5}$ 9 will be shown simply as 0 4 7 5 9.

A special character called a *storage mark* normally occupies at least one position of accumulator and auxiliary storage. The character marks the left limit of the storage contents and automatically appears in the proper position next to the highest-order character of the storage field. The mark is represented in text and programs by the letter *a* and internally in 7080

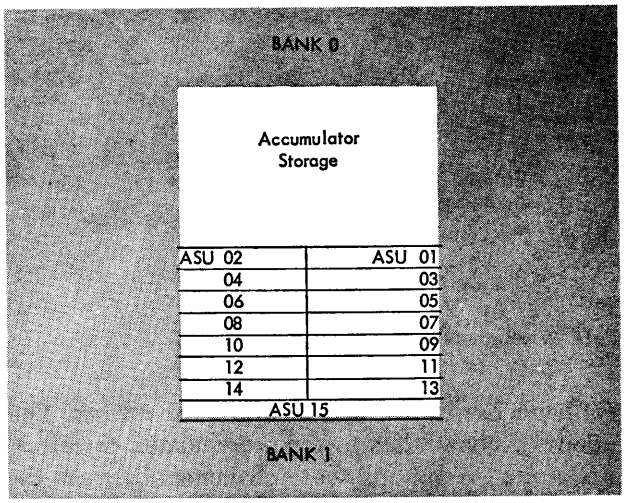


Figure 8. Divisions of Central Storage, Banks 0 and 1

storage by the BCD code 000 0000. A storage mark in memory is considered an invalid character; however, for purposes of transferring data between memory and storage, a valid equivalent character is available (see "Data Transmission Operations").

A field in either accumulator or auxiliary storage can be shortened from or extended to the left by proper positioning of the storage mark. If the field is extended, zeros are automatically inserted between the storage mark and the high-order position of the field.

The *starting point counter,* containing the location of the right-hand character of the stored field, sets the

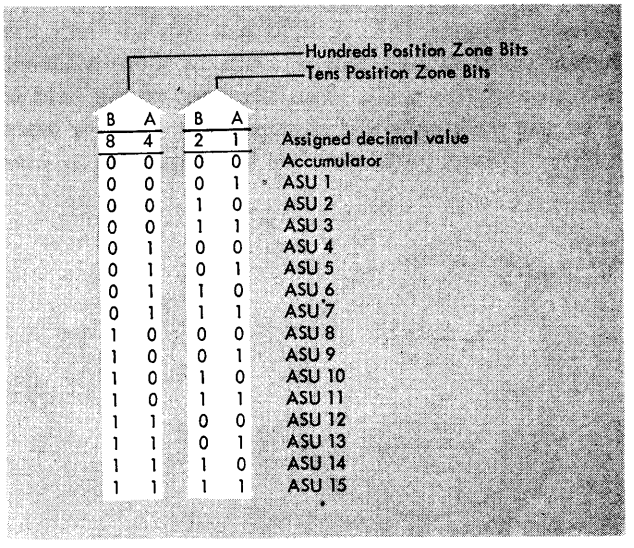


Figure 9. Chart of Storage Coding

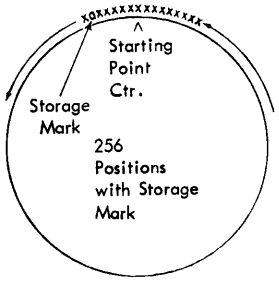


Figure 10. Accumulator Storage

right-hand limit of a field in the accumulator. Operations involving data in the accumulator, therefore, usually operate only on those characters between the storage mark and the starting point counter. However, certain instructions can handle a specified number of characters to the left of the starting point counter without regard for the position of the storage mark. Other instructions can load or unload the entire contents of the bank.

The location of a field in the accumulator can be shown by representing the bank as a circle with 256 available character positions around its circumference. Figure 10 shows a field of six positions defined by the storage mark and the starting point counter. The field can be shortened from or lengthened to the right by shifting the counter. When it is lengthened, zeros are automatically inserted as far as the new position of the counter.

The right-hand limit of a field in auxiliary storage is fixed by the arbitrary division of the storage bank into fifteen separate units. A field in auxiliary storage is therefore defined as being located between the division point of the particular unit and the *next left storage mark.* Auxiliary storage can also be represented in the form of a circle with a 256-character capacity (Figure 11). A field can extend from the division point of one unit into one or more adjacent units around the circle. The left limit of the field is set by the position of the storage mark. Two or more auxiliary storage units can thus be coupled to accommodate a field of data up to the 256-character capacity of the entire bank.

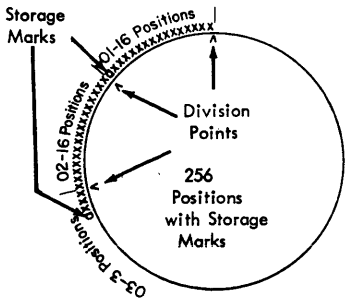


Figure 11. Auxiliary Storage

Positive and negative fields are stored as true numbers in accumulator or auxiliary storage. Two sign indicators register the sign of the fields; one serves accumulator storage, and the other serves all auxiliary storage units. The sequence of operations within a procedure may be changed depending upon whether the sign of the accumulator or auxiliary storage is plus or minus, or the result is zero.

A field in an auxiliary storage unit or in the accumulator may be compared with another field in memory. Comparison indicators register the results of the comparison as high, equal, or low. One set of indicators serves both the accumulator and all auxiliary storage units.

The sequence of operations within a program may be varied, depending upon whether the factor in the particular storage unit is higher, lower, or equal to a specified factor in memory.

When arithmetic operations are performed, the ACC or the ASU contains one of the two fields to be used in a calculation. The second field is in memory. To calculate $A + B = T$, the factor A is in a storage unit while factor B is in memory. After the addition operation is completed, the result T replaces factor A in the storage unit. The result of the calculation always replaces the original field in the ACC or the ASU, with the exception that a result may be added directly to a field in memory from a storage unit. In this instance, the ACC or the ASU remains unchanged.

Accumulator (ACC) and auxiliary storage unit (ASU) can be used to rearrange data in memory. Fields, records, or any portion of either, can be taken from one location in memory to a storage unit and from there can be relocated in another part of memory to form any desired arrangement. Data cannot be transferred directly from one storage unit to another but must first pass through memory.

Bank 2, Communication Storage

This bank is divided into two logical parts, as shown in Figure 12:

1. Four "channel word sets" each containing four 8-character words. There is a channel word set for each of the four communication channels (20-23).

2. One channel word set (25) provides four words (250-253) which serve as interrupt words.

Three channel word sets (24, 26, and 27) are not used.

CHANNEL WORD SET

Figure 13 shows the subdivision of a channel word

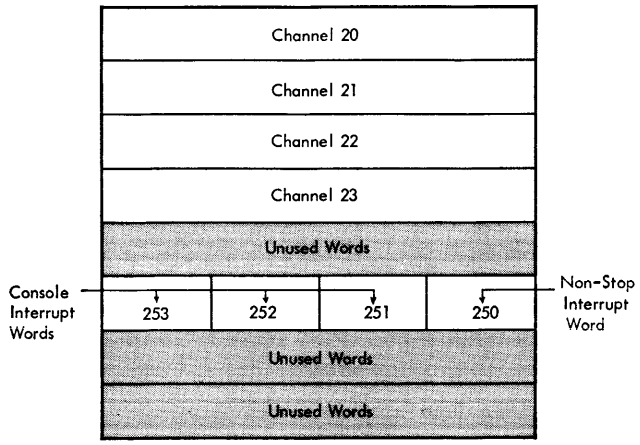


Figure 12. Communication Storage, Bank 2

set into the four 8-character words.

Words 2 and 3. Positions 0-4 (from right to left) of each of these two words serve as data buffers. Information reading into the channel from tape is placed serially, one character at a time, into one of these buffers. When a buffer is filled, the five characters are transmitted as one 5-character block into memory while the alternate buffer is being filled. If the number of characters in the record being read is not divisible by five, the final block transmitted to memory consists of the last characters of the record plus enough group mark characters to fill the buffer.

When information is written on tape from memory, the data is sent from memory to the buffer in blocks of five characters. Then the buffer is emptied, one character at a time being sent to the tape. As a buffer becomes empty, it receives another block of five characters, while the other buffer is emptied.

Character position 5 of each word contains a character control digit which controls the positioning of characters, one at a time, as they are received or sent to the I-O device. Positions 6 and 7 of both words are not used.

The data buffers operate in an identical manner in both the 7080 and 705 III modes. They perform the same functions as the input-output buffers in the 767 data synchronizer used with the 705 III system. Therefore, the 7080 can operate as a 705 III without the use of data synchronizers.

Word 1: Positions 0-3 contain the address in memory to or from which the next five-character block in the data buffer is to be transmitted. For example, in reading a tape record, the address of the read instruction is initially placed in positions 0-3. After the first five characters are read into memory, this address is incremented by five for each additional block in the record until the end-of-record gap is sensed on tape. In writing on tape, the write address is incremented in the same manner until the writing operation is terminated by sensing a group mark in memory at the end of the record. Positions 4-7 are not used.

This word performs the same functions as the SMAC in the 767 data synchronizer. At the end of a read or write operation, the counter contains a memory address five positions higher than the last memory reference, that is, the 0 or 5 address of the last group of five memory characters handled by the instruction. For a write instruction, the last group handled is the group after the one containing the group mark.

Word 0: The reading or writing of data through a communication channel is normally controlled by a separate subroutine, called the interrupt program. Positions 0-3 of word 0 contain the location of the next instruction to be executed when an automatic interrupt occurs for that particular channel.

When an automatic interrupt occurs, status indicators in the 7080 are set in accordance with the bit configuration contained in positions 4-7 of word 0 for that channel. This information includes the status of indicators for high and low comparison, accumulator minus and zero, auxiliary storage units minus and zero, indicators 00900 to 00905 on or off, transfer-any indicator on or off, and the 7080 mode indicator on or off. (The functions of each indicator are explained in detail

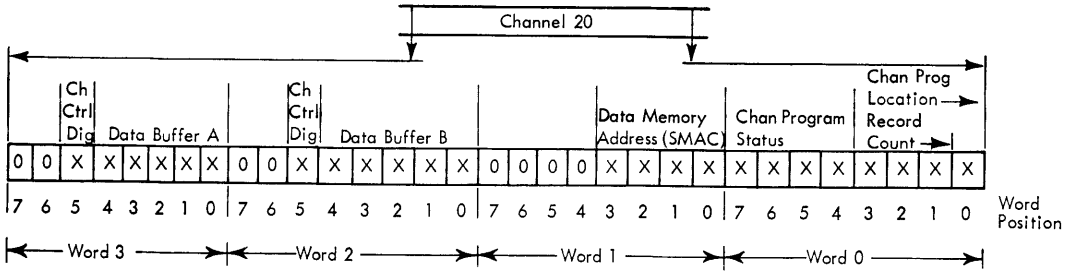


Figure 13. Channel Word Set

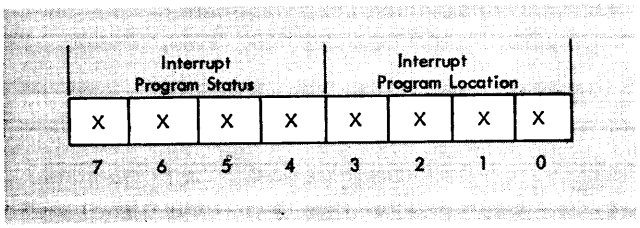


Figure 14. Interrupt Word

in the sections pertaining to those indicators.) The storage of machine status is as follows:

STATUS INDICATOR	STORAGE WORD CHARACTER	BIT POSITION	INDICATOR CONDITION, BIT STATE = 1
High comparison	7	1	on
Low comparison	7	2	on
Overflow check (00904)	6	1	on
Sign check (00905)	6	2	on
Transfer any	6	4	on
7080 mode	6	A	on
Instruction Check (00900)	5	1	on
Machine check (00901)	5	2	on
Read-write check (00902)	5	4	on
Record check (00903)	5	A	on
Accumulator sign	4	1	minus
ASU sign	4	2	minus
Accumulator zero	4	4	zero
ASU zero	4	A	zero

Thus, whenever an interrupt program is to be executed, the 7080 is automatically placed in the proper status for that particular program. All indicators are restored to the status they registered *after the completion* of the *last instruction executed* in the interrupt program. The initial status for the program is established by appropriate housekeeping.

Tape reading or writing instructions may be given that cause a specified number of records to be placed in or transmitted from memory. In this case, word 0 has an alternate use as a record counter. Such instructions are normally given only in the 705 III mode and when the machine is not in the interrupt mode. Positions 1-3 simulate the action of the record counter in the 767 data synchronizer. Positions 4-7 are not used.

INTERRUPT WORDS

The portion of bank 2 which would normally be channel 25 is divided into four interrupt words. The format and function of these words are identical to those of word 0 in a channel word set (Figure 13). Positions 0-3 contain the location of the next instruction to be executed when an interrupt occurs. Positions 4-7 are used for storage of machine status (Figure 14).

Each interrupt word is associated with a specific interrupting condition as follows:

Interrupt Word 250: This word is associated with the non-stop operation feature and its function is explained under that section.

Interrupt Words 251, 252, and 253: These words are associated with console interrupt keys 1, 2, and 3, respectively. Depression of any of the three keys causes an automatic program interrupt to the location specified in positions 0-3 of its related word.

Bank 3, Channel Auxiliary Storage Units (CASU)

Instructions in an interrupt program which specify the use of auxiliary storage automatically use these units unless special instructions are used to refer to the normal ASU's in storage bank 1. They operate in the same manner as those in storage bank 1. However, CASU 15 is used to store the status of the main program before a transfer is made to the interrupt program. For this purpose, CASU 15 is divided into four 8-character words as follows (Figure 15).

Word 0: Positions 0-3 contain the location of the next instruction to be executed in the main program when control is transferred from the interrupt program back to the main program. Positions 4-7 contain the status of indicators as previously explained for these positions in word 0 of a channel word set.

Word 1: Positions 0-3 contain the setting of the starting point counter. Positions 4-7 are not used.

Word 2: Positions 0-3 contain the address indicated by MAC II. Positions 4-7 are not used.

Word 3: The contents of the select register are stored in positions 0-3; storage marks are placed in positions 4-7.

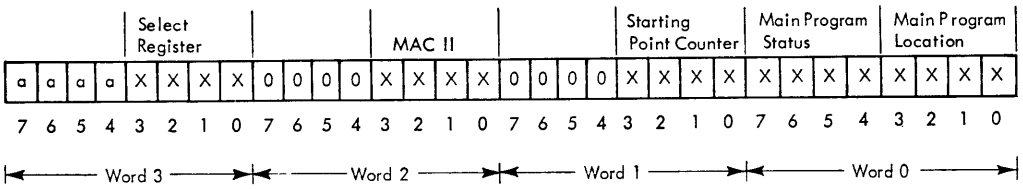


Figure 15. Channel ASU 15

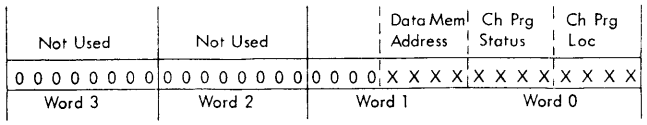


Figure 16. Channel Word Sets 40 and 41

Bank 4

This bank is similar to bank 2. The channel word sets 44-47 are identical in make-up and operation to channel word sets 20-23. However, the high-speed channel word sets 40-41 (Figure 16) are different: words 2 and 3 are not used because the assembly and disassembly of the five character blocks is performed in the 10 character buffer within the 7908 data channel.

Starting Point Counter (SPC)

All instructions that use or involve central storage are executed with reference to the previous setting of the starting point counter. One counter is provided for all banks. The counter may be set to any position within any bank by program instruction. (Refer to "Set Starting Point Counter.")

The addressing scheme for central storage is shown in Figure 17. The five 256-position banks are numbered 0, 1, 2, 3, and 4. Each bank is divided into eight 32-position word sets numbered 0-7. Each word set is further subdivided into four 8-position words numbered 0-3, and each word has eight character positions numbered 0-7. The thousands position of a set-starting-point-counter instruction address specifies the bank, the hundreds position the word set, the tens position the word within the set, and the units position the character within the word. The address 2713, for example, refers to bank 2, word set 7, word 1, and character 3.

Any instruction using storage that does not have ASU coding automatically specifies as an accumulator the bank of central storage indicated by the current setting of the starting point counter. Instructions with ASU coding specify an ASU in (a) bank 1, if the starting point counter is set to *any position* within bank 0 or 1; (b) bank 3, if the counter is set to any position within bank 2 or 3; (c) bank 4, if the starting point counter is set to any position within bank 4. However, any position addressed in bank 4 that is not an active part of a channel word set will always contain storage marks. The fixed divisions of ASU storage are maintained for all storage reference instructions that specify these units, regardless of the bank used.

The flexibility of central storage is such that any bank can be used as an accumulator, while either banks 1 or 3 can be used as ASU's by proper manipulation of the starting point counter. However, the programmer must be aware that communication storage, bank 2, and channel ASU 15, bank 3, are involved with the functions of data flow and priority processing. These positions of central storage are normally used only for this purpose.

Execution of an automatic interruption or a program transfer to an interrupt program automatically places the starting point counter at position 2000. Therefore, subsequent references to central storage without ASU coding specify communication storage, bank 2, as an accumulator. Since bank 2 is involved with the flow of data to and from the channels, all instructions in an interrupt program using central storage should refer to an ASU, thereby properly utilizing the channel ASU's in bank 3 provided for this purpose.

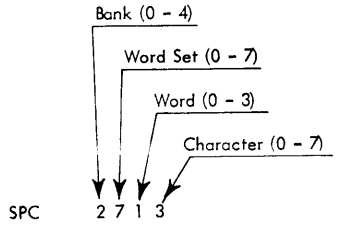


Figure 17. Central Storage Addressing

Input-Output Component Address System

Each input-output (I-O) component of the 7080 system is assigned a specific address to provide a means of selecting one particular device from all those attached to the CPU. A component address is distinguished from a memory address by the operation part of the instruction.

705 I-II MODE

Except for the typewriter and the console card reader, only input-output equipment attached to the 7622 signal control can be selected in this mode. Addresses remain the same as when this equipment is attached to a 705 I or II and the units are operated in the same manner. Communication channels are not available to the program. The following addresses are assigned:

I-O ADDRESSES	CONTROL UNIT	ATTACHED UNITS
00100-00199	759 Card Reader Control	(1) 714 Card Reader
00100-00109		(1) 7502 Card Reader

I-O ADDRESSES	CONTROL UNIT	ATTACHED UNITS
00200-00299	754 Tape Control	(10) 727 Tape Units
00200-00299	760 1 Control and Storage	(1) 720 Printer (2) 727 Tape Units
00200-00299	760 2 Control and Storage	(1) 730 Printer (2) 727 Tape Units
00300-00399	758 Card Punch Control	(1) 722 Card Punch
00400-00499	757 Printer Control	(1) 717 Printer
00400-00499	774 Tape Data Selector	(1) 407/408 Printer or 519 Punch
00500		(1) Typewriter
00600-00699	777 Tape Record Coordinator	(8) 727 Tape Units
01000-01899		(1) 734 Drum

NOTE: Addresses above 01899 are reserved for the communication channels in either the 705 III or 7080 modes.

705 III AND 7080 MODES

A 705 III program may call for the use of data synchronizers with either 729 I or III tape units. As previously stated, the 7621 tape control and a communication channel can be substituted for the data synchronizer. Tape select addresses in such a program will select instead a 7621 tape control and the attached 729 II or IV tape units. Address switches provided on the 7621 units must be set to correspond with the addresses specified by the program. For example, a 705 III select address 00214 specifies tape operation, DS 1, tape unit 4. On the 7080, SEL 00214 will specify tape operation, tape unit 4 on the communication channel whose associated 7621 address switch is set to 1. The channel word set used to simulate operation of the DS will be the one associated with the selected communication channel. This may be any one of the four communication channels available with the 7080.

When both 754 tape controls and a data synchronizer are called for by the program, the address switch of the 754 must be set to a number which does *not* correspond with the address switch of *any* 7621. For example, assume that the address switch of the 754 is 0, and that the address switches of a 7621, Model 2, are set to 1 and 2. In this case, a SEL 00204 will operate tape unit 4 attached to the 754. SEL 00214 will operate tape unit 4 attached to the first communication channel with which the 7621 is associated; SEL 00224 will operate tape unit 4 attached to the second communication channel with which the 7621 is associated.

In the 7080 mode, a tape operation using a communication channel is initiated by specifying the channel number in the two high-order positions of the select address, digits 20-23. The tens position of the address must always be zero; the units position specifies the particular tape unit required, digits 0-9. The setting of the address switch on the 7621 attached to the selected channel is immaterial. For example, SEL 02004 initiates tape operation on channel 20, tape unit 4, regardless of the setting of the 7621 address switch. The channel word set used corresponds to the channel selected.

Communication channels may also be addressed in the 705 III mode in the same manner as described for the 7080 mode, and 705 III type addressing can be used in the 7080 mode.

When 705 I-II input-output units are also used in the 7080 mode, their addresses remain the same as when used with the 705.

The addressing scheme for I-O devices connected to the system through the 7908 data channel differs from that used by the 7621. First a channel is selected; for instance, select 4000 specifies channel 40. Then a WRO 3 command is given, and data is transmitted over the selected channel to the I-O adapter. This data contains the order code and the address for selecting the specific I-O device desired. This order code and address is peculiar to each type of device and is discussed in the description of that device.

Check Indicators

Two classifications of checks are carried out by the 7080 to insure the accuracy of data processing. These are:

1. Checks on the reading and writing of data by the input-output units including channel checks, and
2. Checks on the internal processing of data within the CPU.

Each of six basic check indicators is associated with a switch (00900-00905). The switches may be set to AUTOMATIC or to PROGRAM. When the switch is set to AUTOMATIC, the error detected by the corresponding check indicator causes an automatic machine stop (except under conditions as explained in "Non-Stop Operation"). Corrective action is under manual control of the operator. Instruction executions may or may not be completed, depending upon the type of error. In the case of an error due to a 00900, 00902, or 00903, pressing the start key resets the indicator, and automatic operation is resumed. However, if the error is due to a 00901, 00904, or 00905, the machine store key or a manual keyboard operation key (display, store, instruct) must be pressed before the start key is effective in turning off the indicator and for resuming automatic operation.

When the switches are set to PROGRAM, an error does not stop the machine and corrective action may or may not be taken under program control.

Switches may be set so that some are under program control while others cause a machine stop.

Check indicators under program control are normally examined or interrogated at points in the procedure where it is desirable to check the processing. Two instructions are used: select, and transfer on signal. The select instruction address specifies the indicator; the transfer on signal is a conditional branching instruction. If the indicator is on, a transfer is made to the location of an instruction specified by the transfer-on-signal address. This transfer is usually to the first instruction of a subroutine that will direct the machine to take corrective action automatically. The indicator is turned off by the transfer-on-signal instruction. (Also, see TRS 10-15.)

All checking devices are used entirely at the discretion of the programmer. In many cases it is not necessary to interrupt machine operation when an error condition is detected. The programmer can include special branch programs to handle certain types of errors as exceptions. An error in reading a record from tape, for example, may be programmed to backspace the tape and reread the record. If a correct reading is obtained the second time, normal machine operation continues. If the error persists, machine operation can be interrupted or the incorrect record can be noted and operation continued.

Check indicators and their assigned addresses are:

Instruction Check Indicator	00900
Machine Check Indicator	00901
Read-Write Check Indicator	00902
Record Check Indicator	00903
Overflow Check Indicator	00904
Sign Check Indicator	00905

In addition to the six check indicators associated with switches, there is an additional check indicator for which there is no associated switch. This indicator, channel check, is under program control.

INSTRUCTION CHECK INDICATOR, 00900

The instruction check indicator turns on when the following conditions occur:

1 (OP CH): A character code error is detected, an invalid operation code is encountered in the operation register, the operation code is incorrectly interpreted, or any of the comma operation codes is given in any mode other than the 7080 mode.

2. (4/9 CH): The units position of the address part of any transfer instruction (add address to memory, unload address, load address, normalize and transfer, transfer to interrupt program) or a transmit instruction specifying accumulator 00, is not 4 or 9; the SEND instruction is checked in the 705 III and the 7080 modes; or, the field addressed by an indirect address coded instruction does not end in a 4 or 9. The indicator is also turned on if the address of the ten character transmit instruction does not end in 9.

3. (DR VRC): Any of the five characters from the data register is invalid (during I time) or, during IA time, an invalid character appears in character positions 1, 2, 3, or 4.

With the switch set to AUTOMATIC, the machine stops during the character cycle in which the error occurred.

MACHINE CHECK INDICATOR, 00901

The machine check indicator is turned on when a character code error is detected during the execution of all instructions in which data is transferred from central storage or memory. Exceptions are *all* read instructions and write instructions over a communication channel; errors in this case result in a channel check. The word register check circuit checks all eight characters from the storage register for a VRC, and an address check circuit for a 0/5 check in WR character 4.

When the indicator switch is turned to AUTOMATIC, the machine stops during the character cycle in which the error occurred, except when an error occurs during the execution of RWW-SND redundancy scan, set bit redundant, write, or write and erase. In these cases, the indicator will be turned on but no automatic stop will occur. The TMC instruction can detect any type of 901.

READ-WRITE CHECK INDICATOR, 00902

The read-write indicator turns on when a character code error is detected during the execution of a read, write, read-while-writing, or write-and-erase instruction except when using a communication channel. The indicator also turns on when an error is detected in reading the holes in the card or by the longitudinal check in tape reading. The indicator, therefore, checks the transmission of data to memory from all input units not on a channel. It also checks the transmission of all output data from memory to the drum, tape unit, and other input-output units that are not on a channel. The indicator also turns on if an attempt is made to read or write beyond the limits of the drum or if an error occurs in recording a tape mark.

When the indicator switch is turned to AUTOMATIC, an error stops the machine after the instruction is executed.

RECORD CHECK INDICATOR, 00903

The record check indicator turns on when an error is detected by the brush-compare method on the punch and by the echo-check method on the printer. An error in card punching is detected as the card passes a brush station after it has been punched. If an error occurs, the record check indicator turns on during the execution of the next write or write-and-erase instruction to that card punch.

An error in printing is detected by sensing the position of each print wheel during the print cycle. If an error occurs, the indicator turns on during the execution of the next write or write-and-erase instruction involving that printer.

In both cases, when the switch for this indicator is on AUTOMATIC, an error stops the machine at the end of the punching or printing cycle during which the indicator was turned on. At this time, the error card is the last card to go into the punch stacker. The incorrect line of printing immediately precedes the last printed line.

OVERFLOW CHECK INDICATOR, 00904

The overflow check indicator is turned on during an add or subtract operation when the number of digits in the result is greater than the number of digits in the longer of the two fields. An overflow is indicated as a result of a round operation, if a carry-over is made out of the high-order position of the accumulator storage field.

The indicator is turned on by a divide instruction when the divisor does not have a greater absolute value than an equal number of digits taken from the left end of the dividend. When the error switch for this indicator is turned to AUTOMATIC, an error stops the machine during the execution of the instruction.

SIGN CHECK INDICATOR, 00905

The sign check indicator turns on if a memory field addressed by an arithmetic instruction (add, subtract, multiply, etc.) does not have plus or minus zoning over the low-order digit.

When the switch for this indicator is set to AUTOMATIC, an error stops the machine in the same cycle in which the error is detected.

CHANNEL CHECK INDICATORS

There is a channel check indicator corresponding to each communication channel of the 7080. (These are located in the 7621 and the 7908). The turning on of any channel check indicator will turn on the MPX indicator on the console. There is no associated switch for these indicators. The error conditions are under program control and may be interrogated with a transfer on signal 02 or 03 (TTC or TSA) after prior selection of the channel.

The channel check indicator will turn on for any error encountered in a channel read or write operation or a 0-5 check. This indicator is similar to the PCT check indicator in the 705 III.

If an error is detected in the data memory address during a read 00 operation, the channel check indicator is turned on, the read 00 instruction is converted to a read 01 instruction, and no further data is read into memory.

Other Indicators and Switches

AUTOMATIC RESTART INDICATOR

This indicator is provided on the 7080 in addition to the 00900-00905 check indicators. There is no corresponding console switch.

The indicator is turned on whenever the machine does not complete the execution of an instruction in approximately two seconds. When the nonstop switch is set ON, an automatic restart takes place. (Refer to "Nonstop Operation.")

The automatic restart indicator can be interrogated and reset by means of the transfer-auto-restart instruction.

ANY INDICATOR

The ANY indicator turns on when:

1. Any serial device I-O indicator is turned on.
2. If the check switch (00900-00905) is set to program and a check occurs.
3. If the check switch is set to automatic, the nonstop switch is on, and the system is not operating in the interrupt program and a check occurs.

The ANY indicator does not turn on when:

1. The check switch (00900-00905) is set to automatic, the non-stop switch is off, and the system is not operating in the interrupt program when a check occurs.
2. If the 00901 results from a set bit redundant, send, write, write and erase, or RWW-SND redundancy scan instruction, regardless of the switch setting.

Special Case: If a 00901 results from an unload storage bank operation, the ANY signal indicator is turned on (check switch on or off) but the system does not stop or interrupt to word 250.

In general: if an error halt occurs, the ANY indicator does not turn on; if an error halt does not occur, the ANY indicator does turn on, and it may be interrogated by a transfer-any instruction.

When the indicator is on, the address part of the

transfer-any instruction specifies the memory location of the next instruction to be executed. The indicator is turned off if a transfer is executed.

The ANY indicator and the transfer-any instruction enable the programmer to use one instruction in the main program to test for all types of error other than channel errors. A subroutine then determines the specific cause of the error and corrective action can be taken accordingly. No corresponding switch is provided on the console.

SIGN INDICATORS

Two sign indicators are provided to register the sign of results obtained in central storage, one for the accumulator (any bank) and one for auxiliary storage units (banks 1 and 3). The indicators are automatically set according to the rules of algebra for the results of calculation, such as the algebraic sign of a sum, product, remainder, or quotient.

The indicators are also automatically set to plus (off) if a result is zero, unless an improper division operation is performed in an accumulator. In this case the accumulator sign indicator is not affected. Certain other instructions may arbitrarily set the indicators off. These conditions are noted in the descriptions given for these particular instructions.

The indicator for the auxiliary storage units always registers the sign of the field in the *last used* auxiliary storage unit, regardless of which bank is used. For example, in a sequence of instructions, assume that the result in ASU 02, bank 1, is plus. The corresponding ASU sign indicator is consequently also set to PLUS (off). Assume that the following instruction obtains a minus result in ASU 04, bank 3. The ASU sign indicator is then set to MINUS (on). If the next instruction produces a plus result in ASU 15, the ASU sign indicator is again set off, and so on.

However, if bank 1 is now used as an accumulator, the sign of the result is set in the accumulator sign indicator and the ASU sign indicator *is not affected.*

Indicators may be tested by program instructions and a conditional transfer can be executed, depending upon whether the indicator is on or off. The transfer does not affect the conditon of the indicator.

ZERO INDICATORS

Two zero indicators are provided, one for accumulator (any bank) and one for auxiliary storage units (banks 1 and 3). They are turned on when zero balances are obtained in the storage units. The zero indicators have the same function and operation as the sign indicators except that they register zero balances rather than the sign of results.

Zero indicators may also be tested by program instructions to execute a conditional transfer, depending upon whether the indicator is on or off. The transfer does not affect the condition of the indicator.

COMPARISON INDICATORS

Two comparison indicators register the results of a comparison of data in central storage with data in memory. When the storage field is higher than the field in memory, the high indicator is turned on. When the storage field is lower than the field in memory, the low indicator is turned on. Neither indicator is turned on if the fields are equal. Turning on one indicator resets the other indicator if it is on; therefore, both indicators are never on at the same time. An equal comparison resets both indicators. The indicators serve all banks of storage.

The indicators may be interrogated by conditional transfer instructions: transfer on high and transfer on equal. The condition of an indicator is not affected by a transfer, and either indicator may be interrogated any number of times during a program. The indicators are affected only by the results of a comparison.

7080 MODE INDICATOR

The 7080 mode indicator is turned on when the system is instructed to enter the 7080 mode, and off when instructed to leave the 7080 mode. It can also be turned on or off by means of an automatic interrupt or a leave interrupt instruction.

In the case of an automatic interrupt, the status of the indicator is stored (together with the status of other indicators) in word 0 of CASU 15 (Figure 11). The indicator is then set according to the contents of the interrupt word or word 0 of the interrupting channel word set.

In the case of a LIP instruction, the status of an indicator may or may not be initially stored in the interrupt word or word 0 of the channel word set, depending on the address of the instruction. In any event, however, the indicator is then set according to the contents of word 0 of CASU 15.

The status of the 7080 mode indicator is not affected by a transfer to the interrupt program instruction.

Alteration Switches

Six alteration switches are located on the 7153 console. Each switch can be turned on or off by the operator and can be interrogated by the program. Alteration switches are selected and tested by select and transfer-on-signal instructions in the same man-

ner as check indicators. However, in the 705 III or 7080 mode, a switch can be interrogated by a transfer-any instruction without a previous select instruction.

Alteration switches are assigned the addresses 00911-00916.

Nonstop Operation

The nonstop operation feature of the 7080 permits continuous operation of the machine in automatic status.

When execution of an instruction is not completed within approximately two seconds, or when manual status would normally be entered for reasons other than a manual stop, the machine may be conditioned to interrupt to a program in a location specified by interrupt word 250. This program may analyze the status of the main program to determine the cause of the interrupt. When the cause is known, corrective measures may be taken in the program or control may be returned to the operator.

This feature is under control of the non-stop switch. When the non-stop switch is on, and the machine is not processing an interrupt program, any of the following conditions will cause an automatic interrupt to the location specified by interrupt word 250:

1. A halt instruction.
2. Any condition which turns on one or more of the 00900-00905 check indicators, provided the corresponding switch for the indicator is set to automatic.
3. Any condition which turns on the automatic restart indicator.

When the non-stop switch is on, and the machine is processing an interrupt program, conditions 1 or 2 above will cause the 7080 to stop.

When the non-stop switch is off, conditions 1 and 2 above will cause the 7080 to stop.

When a program is executed with the nonstop switch on, *the 7080 should normally be in the interrupt mode* as conditioned by the instruction enter interrupt mode (EIM).

An interrupt associated with interrupt word 250 takes precedence over all other types of interrupts. Console and communication channel interrupts will be taken in turn after the interrupt with word 250 has been satisfied.

After an interrupt with word 250 has occurred, channel ASU 15 contains the status of the main program at the time the interrupt took place. The check indicators 00900-00905 are reset according to the status bits stored in the interrupt word. In order to test whether one of these indicators caused the interruption, it is necessary to test the proper status bit in CASU 15. To turn off an indicator before returning to the main program, the appropriate status bit must be set to zero.

The automatic restart indicator is not altered as a result of the interrupt nor is it stored in CASU 15. The indicator is tested and turned off in the interrupt program by execution of the TAR instruction.

Depression of the stop, machine stop, instruct, store, or display keys on the console will effect a stop regardless of the setting of the nonstop switch.

The setting of the non-stop switch may be interrogated by a transfer-any (TRA 07-TNS) instruction when the machine is operating in the 705 III or the 7080 mode.

A programming example showing the use of nonstop and interrupt word 250 is given at the end of the appendix.

This section presents a simplified explanation of the 7080 CPU operation logic and data flow, followed by a more detailed explanation of counters and registers and their function in the control of data flow.

The central processing unit operates in a prescribed logical sequence to read, interpret, and execute instructions. Control is provided by the specific instruction to be performed, together with certain timing impulses from an electronic clock. The timing impulses occur at the rate of ten million a second, or, each pulse is one-tenth microsecond long. Ten pulses constitute a machine cycle, the amount of time used to perform a specific machine function.

The first two cycles of each 7080 instruction to be performed are the instruction cycles that occur during instruction time (I time). During I time, the five characters composing a particular instruction are read from memory. The operation part of the instruction is interpreted and controlling circuits to be used in the operation are activated. The address portion of the instruction is set in certain counters and registers for reference. The instruction is then placed back in memory.

The two instruction cycles may be followed by one or more execution cycles, referred to as execution time (E time). During execution time, the operations necessary to perform the instruction are carried out. The number of cycles making up execution time depends upon the particular instruction being executed.

Data Flow

The 7080 system is divided into three parts: serial input-output (I-O) devices, the central processing unit (CPU), and parallel input-output (I-O) devices. The CPU consists of the arithmetic and logical unit, the memory, the central storage and the operator's console.

Data processing is divided into two types of processing, internal and external. Internal processing describes operations or instructions that involve CPU only. External processing is the transfer of data between memory and the input-output machines.

Internal processing and external processing with 705 type serial I-O units both use the memory buffer register and the result register. Therefore, only one can occur at a time.

Internal Processing

ALTERED DATA

Internal processing, where data undergoes a change, involves two separate groups of data to be combined or compared, such as add, subtract, or compare. This type of processing involves both serial and parallel transmission of data.

An example of this is the processing of an add instruction. An add instruction combines a group of characters in memory with another group of characters in storage. The result of this combination is placed in storage. The characters in memory are transferred through the data register to the memory buffer register in groups of five. The other group of characters is transferred as a block of eight from storage through the word register to the storage buffer register.

The low characters of both groups are routed simultaneously to the adder in order to obtain their sum. This sum is then transferred to the result register. Any carry that might occur is held in the adder to combine with the next two numbers routed to the adder. The sum of the addition of the units position in the result register is routed to the position in the storage buffer register vacated by the character sent to the adder.

This routing of a character (from memory buffer register and storage buffer register, through the adder and result register, and back into the storage buffer register) is continued until the end of the instruction or until one of the registers requires a new group of characters. New groups of characters are automatically transferred from memory to the memory buffer register or from storage to storage buffer register as they are needed. The storage buffer register accumulates the sum of the addition. This sum is placed in storage.

UNALTERED DATA

In addition, internal processing (such as load, RAD, or RSU) involves the moving between memory and storage of alphabetic or numerical information that requires no change.

The load instruction, for example, moves alphabetic or numerical information from memory to storage. No change in the information occurs during this

transfer. Five-character parallel transmission is used to move data from memory to the memory buffer register. The storage buffer register receives data from storage by eight-character parallel transmission. Single-character transmission is used to route characters from the memory buffer register to the result register. While one character moves from the memory buffer register to the result register, another character goes from the result register to the storage buffer register. When the memory buffer register requires new data, memory supplies it in blocks of five characters. When the storage buffer register becomes full, the data is transferred to storage as an eight-character group. This method of transferring data continues until the complete field is transferred to storage. An unload instruction transfers alphabetic or numerical information from storage to memory. The same method of parallel and serial transmission is used for both unload and load.

A summary of internal processing shows a pattern of data flow in the system. Five-character parallel transmission is used to move data from memory through the data register to the memory buffer register (Figure 18). Data is also moved from the memory buffer register back to memory by the same method. Information transfers from storage through the word register to the storage buffer register by eight-character parallel transmission. Data moves from the storage buffer register through the storage switch to storage by eight-character transmission.

Single-character transmission is used to route data from the memory buffer register and storage buffer registers to the adder. Information comes from the result register to the storage buffer register or memory buffer register by the same method.

Since single-character transmission involves only the memory buffer register, storage buffer, adder, and the result register for the major portion of the time, the time not used in servicing the buffer registers may be used for external processing of data to and from I-O devices through the communication channels (Figures 19 and 20). Therefore, internal processing and external processing may occur at the same time. Interlocking circuitry, called priority control, is used to determine what operation uses memory or storage first if more than one operation requests them.

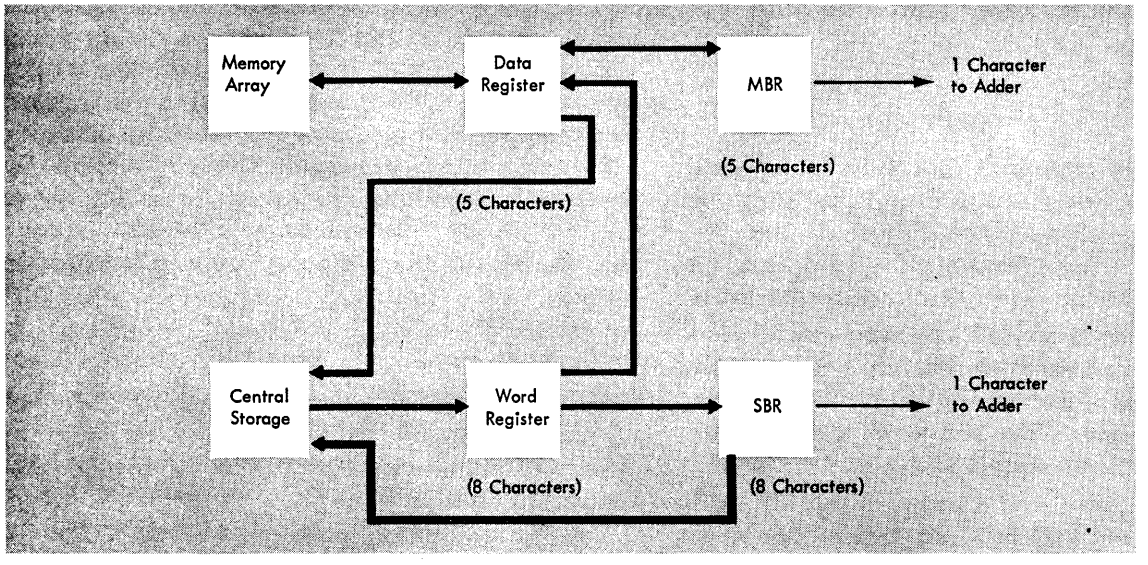


Figure 18. Parallel Transmission

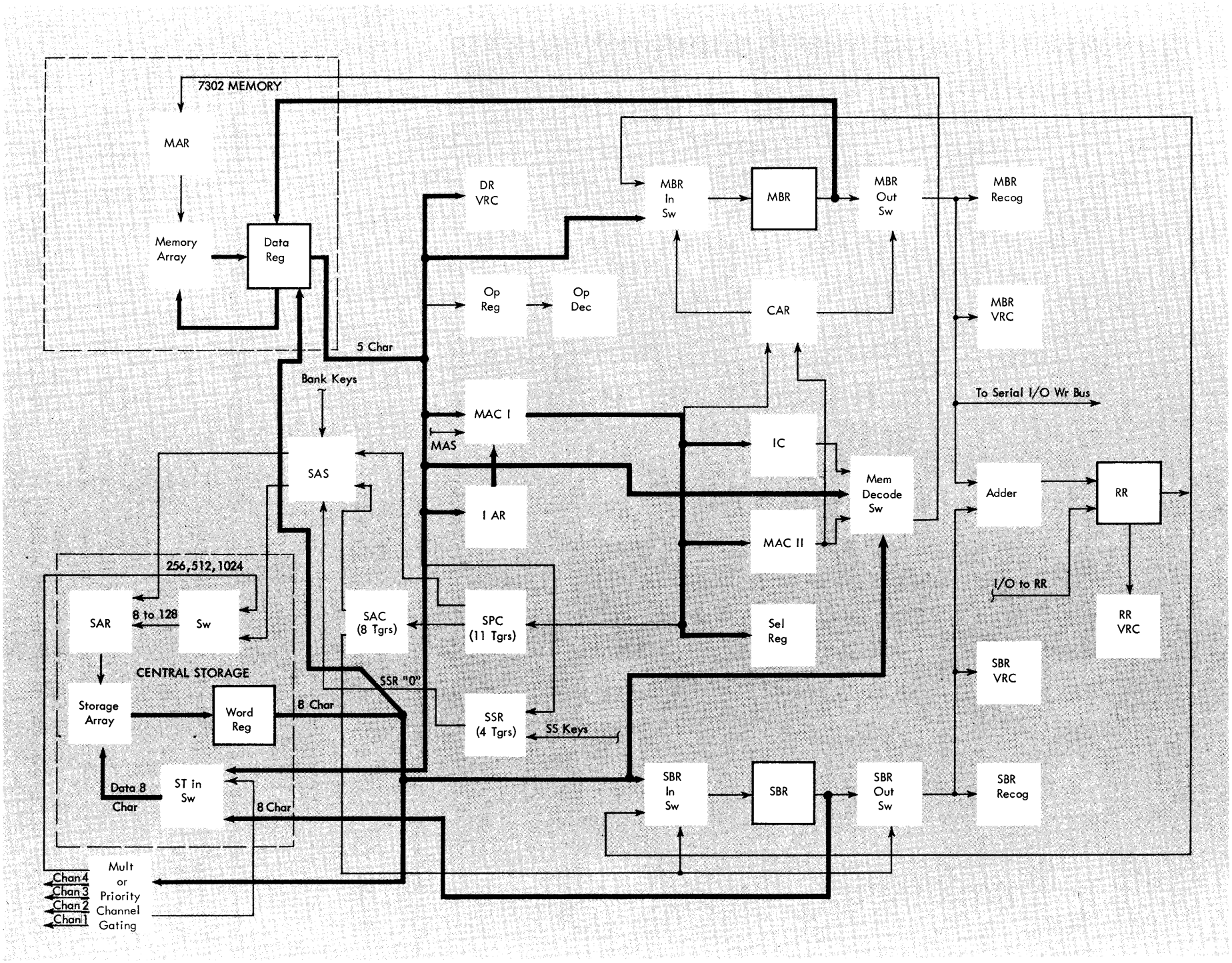


Figure 19. Data Flow

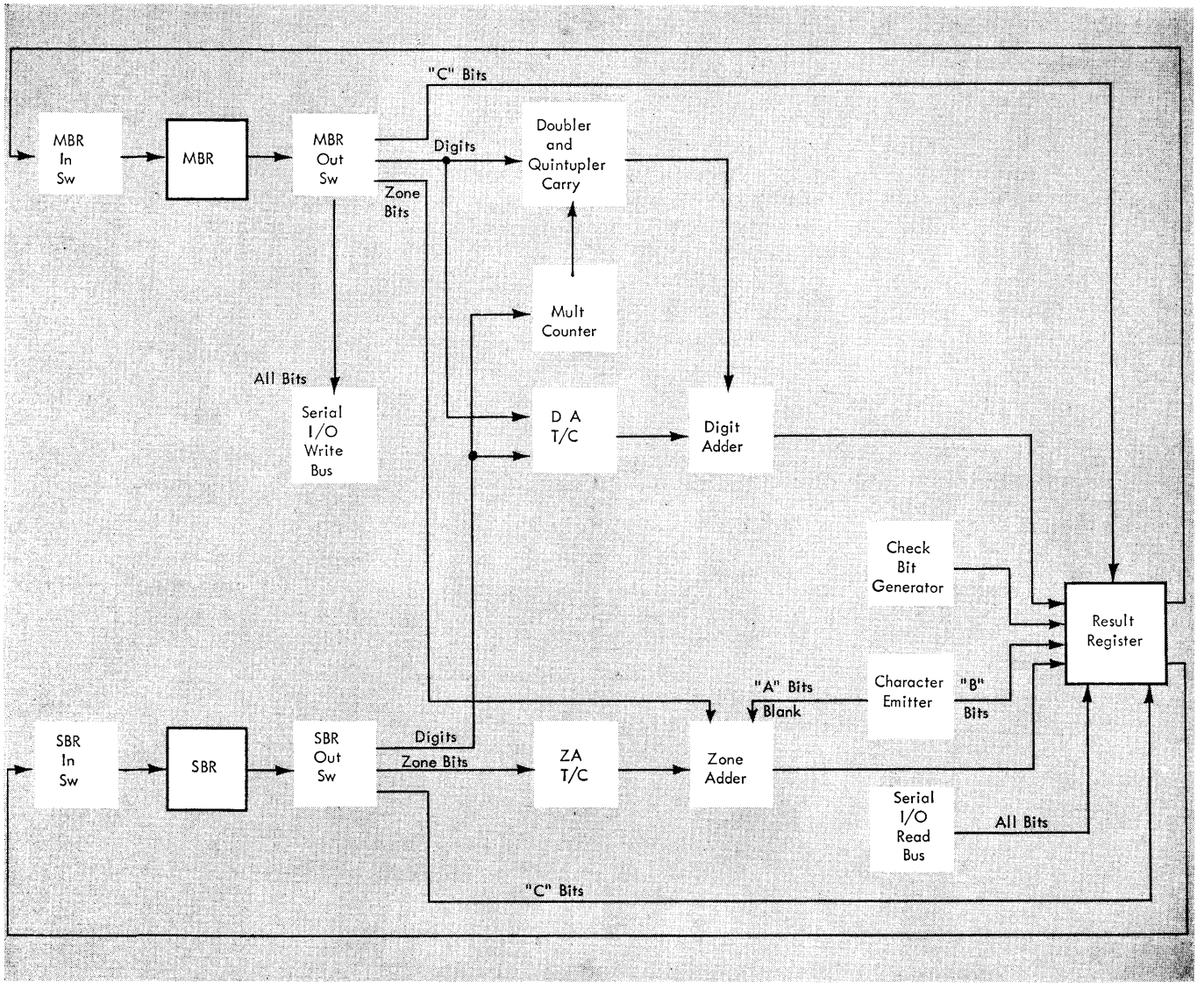


Figure 20. Simplified Data Flow, 7080 CPU

External Processing

The basic instructions involved in external processing are read and write.

WRITE (SERIAL I-O)

Data flow for a write instruction, with a 705 type output device (serial I-O) under selection, is as follows:

1. Five-character parallel transmission from memory through the data register to the memory buffer register.

2. Single-character transfer from the memory buffer register to the I-O bus in the console.

3. Single-character transfer through the 7622 signal control unit to the control unit of the device under selection. The 7622 converts from transistor levels to tube levels. An exception is that data to the typewriter is routed without the use of the 7622 or a control unit.

4. Single-character transfer from the control unit to the output machine. The rate or speed of the single-character transfer depends upon the output

machine. Only one device on the serial I-O cable may be used to write at a time.

READ (SERIAL I-O)

Data flow for a read instruction from a serial input device is as follows:

1. Single-character transfer from the machine to its control unit.
   The console card reader has no control unit; its data goes directly to the result register.
2. Single-character transfers from the control unit through the 7622 signal control unit to the result register. An exception is that data from the console card reader is routed without the use of the 7622. The 7622 converts tube levels to transistor levels. The I-O cable goes through the console, but there is no register in that unit.
3. Single-character transfer from the result register to the memory buffer register.
4. Five-character parallel transmission from the memory buffer register through the data register to memory.

The rate or speed of the single-character transfer depends upon the input machine. Only one device on the serial I-O cable may be reading at one time. Figure 4 shows the serial I-O devices that may be used with the 7080 system. All devices connected to the serial I-O cable follow the same read and write data flow.

Internal processing is prevented during external processing with the serial I-O equipment. This equipment (except the 777) may operate simultaneously with the parallel I-O equipment (units operating over 7080 channels). Priority is given to the parallel I-O equipment.

WRITE (CHANNEL I-O)

A write instruction with a parallel I-O device under selection will transfer information from memory out to a tape unit. This information will make up a record of characters on tape. The select instruction might be 22104, in which the first 2 indicates a select instruction and 2104 is the device address. A tape control unit is selected by the 21, and 04 indicates a tape unit connected to that control unit. The instruction R1000 means "write from memory address 1000." Writing starts at the character located at 1000 and continues until a group mark character is sensed.

One of the four banks of storage is assigned to serve as a buffer between memory and the tape units when processing tape through the multiplexor (I-O control). This bank (2) is called communication storage. Sections of this bank, called channel word sets, are assigned to the channels. One channel word set is assigned to each channel. The channel word set is made up of four words (Figure 13). Data words A and B serve as two five-character buffers between memory and the tape control units. The address word stores the starting address of the write instruction. The interrupt word stores the starting address of a program subroutine that will be automatically branched to at the completion of the write operation.

The multiplexor (I-O control) serves as a master control over the channel operations. Control and completion of the write instruction are handled by the tape control after being initiated by the CPU.

READ (CHANNEL I-O)

A read instruction with a parallel I-O device under selection will transfer information from a tape unit to memory. Information is transferred serially to the data words A and B. As each data word is filled, the five characters it contains are transmitted in parallel to memory. Reading is stopped by the sensing of an inter-record gap on tape. If the record length is not a multiple of five, the remainder of the last data word is filled with group marks.

The internal speed of the CPU is one cycle every 1.00 microsecond. Tape may be processed at speeds of 16, 24, 44, or 67 microseconds per character (as a function of the type of tape unit and character density on tape). Storage can complete the reading or writing of an eight-character word during one CPU cycle (one microsecond). Two CPU cycles (2.00 microseconds) are required to complete the reading or writing of a five-character word in memory.

Comparing the internal speed of the CPU with the speed of tape processing, it becomes apparent that memory and storage are idle during most of the read or write instruction. This idle time may be utilized to process other internal instructions simultaneously with the multiplexor operation. Up to four simultaneous multiplexor operations may occur if different channels are used for each I-O instruction.

The priority processing system determines what instruction will use memory and storage if more than one instruction requests them.

NOTE: The preceding discussions describe the operation of the 7621 channels. The 7908 channels operate in much the same manner, except for the high speed channels. These are discussed under the 7908 data channel.

Arithmetic Control Circuits

Internal information that is to be altered, such as arithmetic functions, is removed from memory and storage and routed through the arithmetic circuits to the result register, and then returned to memory or storage. The direction of data flow and the action of the various arithmetic circuits upon the data is determined by the instruction to be performed. Figure 20 is a schematic of data flow for the arithmetic circuit controls.

MEMORY BUFFER REGISTER OUT SWITCH

Removing data from memory places five characters in the memory buffer register (MBR). The addressed characters in MBR may be routed through the MBR-out switch and code checked. An odd number of bits, or the lack of bits in the MBR-OUT switch, turns on the MBR code check indicator (Figure 19), when required by the operation being performed. Character recognition is accomplished by MBR recognition circuits. For example, there are circuits to recognize when the MBR-OUT switch contains a zero, record mark, group mark, ampersand, and so on. Certain characters are used to modify action upon the control of the instruction being performed.

From the MBR-OUT switch, data can be routed to the serial input-output write buses or through the arithmetic circuits to the result register. Data to be written from memory during a write instruction, except when the 7080 channels are used, passes from the MBR-OUT switch, character by character, to the write buses in the input-output cable. The selected output unit then receives the characters from the write buses (via the 7622 and the control unit) and performs the writing.

The zone portion, the numerical portion, and the check bit of a character in the MBR-OUT switch to be processed have separate routes through the CPU circuitry to the result register. The particular instruction being executed determines what portion or portions of the character are to be routed into the result register.

STORAGE BUFFER REGISTER OUT SWITCH

Removing information from storage places eight characters in the storage buffer register (SBR) and routes the addressed character through the SBR OUT switch. The character held by the SBR OUT switch can be code checked. An odd number of bits in any character indicates an SBR code check error, when required by the operation being performed. SBR recognition circuits are used for recognition of the storage mark.

From the SBR-OUT switch, information can be routed through the arithmetic circuits to the result register or to the multiple register during a multiply instruction. The zone portion, the numerical portion, and the check bit of a character in the SBR-OUT switch have separate routes through the CPU to the result register. The particular instruction being executed determines what portion or portions of the character are to be routed to the result register.

NUMERICAL BIT TRANSMISSION

The numerical portion of a character routed from the MBR-OUT switch can pass to the multiply circuitry or through the true-complement (T-C) circuitry to the digit adder. The T-C circuits complement (on a tens basis) or pass unaltered the input bits, depending on the operation being performed.

The numerical bits of a character routed from the SBR-OUT switch can pass to the multiply circuitry or through the true-complement circuits to the digit adder. The T-C circuits complement (on a tens basis) or pass unaltered the input numerical bits, depending on the operation to be performed.

The digit adder can add the numerical bits of a character from the MBR-OUT switch and SBR-OUT switch, or it can allow the numerical bits from either MBR-OUT or SBR-OUT switch to pass through unaltered. When sums with a numerical value greater than nine are produced, the significant digit can be routed to the result register and the carry can be retained and added to the sum produced in the next machine cycle.

ZONE BIT TRANSMISSION

Zone bits are routed from the character registers to the result register, apart from the numerical bits. The zone bits from the MBR-OUT switch are routed to the zone adder (ZA) directly. The zone bits from the SBR-OUT switch are routed through the zone adder true-complement circuits to the zone adder. The true-complement circuits complement or pass, unaltered, the zone bit input. Complementing the zone structure of a character is done binarily by reversing the status of the bits. For example, if the zone bits are 01, the complement is 10; if the bits are 11, the complement is 00.

Zone bits from the MBR-OUT and SBR-OUT switches can be added binarily in the zone adder or can be passed, unaltered, to the result register.

CHECK BIT TRANSMISSION

A check bit in the MBR-OUT or SBR-OUT switch may be routed directly to the result register, or a check bit may be generated by the check bit generator. If the numerical and zone bits of a character are moved through the arithmetic circuits to the result register

unaltered, the check bit (if present) of that character is routed into the result register. This is done to insure a code check on the number of bits in the character, after transmission through the arithmetic circuits.

If, during any machine cycle, the numerical and zone bits have a possibility of changing legitimately within the arithmetic unit, a check bit is automatically generated and placed in the result register.

CHARACTER EMITTER

Some 7080 instructions require that certain characters or specific bits of characters be emitted (generated) within the machine. The circuitry associated with this type of operation is often referred to as the character emitter. The character emitter circuitry can emit a blank, hyphen (minus zone), ampersand (plus zone) or a numerical zero (8 and 2 bits). Changing of bits in a character by using the set-bit instruction involves the character emitter circuitry. The emitted character or bits of a character are set in the result register or zone adder.

RESULT REGISTER

The three bit parts of a processed character are assembled in the result register. They are:

1. The numerical part from the digit adder.
2. The zone part from the zone adder.
3. The C bit from MBR-OUT or SBR-OUT switch or from the C bit generator.

Characters from the serial input-output read bus are also routed into the result register during a READ instruction from a serial unit. A character in the result register can be routed to the MBR or SBR. If the character is routed to the MBR, one of the five characters in the MBR is replaced by the character from the result register. If the character is routed to the SBR, one of the eight characters in the SBR is replaced by the character from the result register.

Counters and Registers

The selection of information from memory and storage is controlled by counters and registers (Figure 20). Counters differ from registers in that counters can be incremented or decremented; both counters and registers can register or hold information. The main purpose of these counters and registers is to hold storage and memory addresses in order to direct the machine to particular information that is to be processed. The counters and switches control switching circuits so that the proper data may be processed.

Two types of counters are used in the CPU: memory address control counters and storage address control counters. The memory address control counters use a modified binary arrangement in which four triggers are arranged to represent the decimal values of 0 through 9. Four sets of these triggers in series represent 0000 through 9999. Four additional triggers in the fifth position that count up to 15 are used to include the complete memory addressing system of 00,000 through 159,999. Storage address control counters use eleven-stage binary counters, consisting of eleven triggers arranged in tandem to represent 0 through 1024.

Trigger Registers

A trigger is a bi-stable device that can be made to store information by having it stay in one of two states. When the trigger is on, it indicates a 1; when the trigger is off, it indicates a 0. Registers can hold numbers or alphabetic characters by first having all their triggers reset, and then having only those triggers turned on which are required for that particular number or character. The trigger is considered on when it is performing the function described by its name.

Trigger Counter

A trigger can be made to count by causing it to change its state. If a trigger is off it is turned on by a "step trigger on" or a "set trigger on" pulse. Likewise, if the trigger is on, it is turned off by a "reset trigger" or a "step trigger off" pulse. This pulse is a regular clock pulse lasting one tenth of a microsecond.

Because one trigger can assume only two possible states, more triggers are required if a count higher than two is desired. The triggers are connected in a serial fashion so that, when one trigger exceeds its capacity, a step pulse is passed to the next trigger. In a similar manner, each trigger influences the succeeding stage. Four triggers, connected in a modified binary arrangement, can be used to represent decimal quantities of 0 through 9. In a true binary arrangement, four triggers can be used to represent decimal quantities of 0 through 15.

Memory Address Control Counters and Registers

The memory address control associated with memory consists of three registers and three counters. The registers can retain memory addresses during the time counters are altered. Memory can be addressed from information in memory or storage. Storage may be addressed from data in memory, storage, or multiplexor.

INITIAL ADDRESS REGISTER

The initial address register (IAR) is a 20-trigger register that represents a six-digit binary-coded decimal address. During I time or IA time, IAR receives the address part of the instruction from the data register (DR). The numerical bit structure from characters 1, 2, 3, and 4 of the DR are set to the triggers of the first four orders of the IAR. The zone bits of characters 1 and 4 are set into the fifth order of the IAR. The IAR can register from 00,000 to 159,999; its primary purpose is to retain the starting position address of the field being processed in memory.

MEMORY ADDRESS COUNTER I

The memory address counter I (MAC I) is a 20-trigger counter that represents a six-digit binary-coded decimal address. At the end of each cycle (except when MAC II is used), MAC I contains the address of the information in the MBR that is to be processed in the next cycle. The MAC I is also used to address memory whenever the MBR requires a new block of data for processing. MAC I is always reset before being set to new information.

During I time or IA time, the MAC I is set to the DR, so that MAC I contains the address of the first block of characters to be operated upon during the execution cycle which follows. This information is transferred through the memory decode switch to the memory address register (MAR). This locates in memory the first block of characters that are sent to the MBR for proccessing. During the following execution cycles, MAC I is stepped, or set, to control which character is to be processed from the MBR. To monitor each character processed from the MBR, and to address new blocks of characters sent to the MBR, MAC I can be stepped plus one, minus one, or plus five.

During the execution of MPY, DIV, or ADM, some stages of the operation require that the memory information be used more than once. The IAR is not altered during the execution of an instruction so that, when necessary, MAC I can be set to IAR to set MAC I in position to use the memory information over again.

During an auto-load operation, MAC I sets to MAS. The select register is set to MAC I; MAC I is reset; MAC I (with its zero contents) is used to address memory.

For instructions like SET, LNG, RND, and SHR, MAC I is not needed to monitor memory information addresses. This allows MAC I to be used as a counter to determine the number of cycles required for the operation. At the beginning of the operation the MAC I contains the address part of the instruction. By stepping MAC I minus one, each cycle, MAC I steps down to 00,000, then to 159,999, and causes the MAC I = 0 trigger to turn on. The output of this trigger is then available to complete or alter the operation.

During a write 01 instruction on the serial I-O bus, MAC I starts with the address portion of the instruction. MAC I is stepped plus one each time a character is sent to the write bus. When MAC I reaches 19,999; 39,999; 59,999; 79,999; 99,999; 119,999; 139,999; or 159,999 and turns on a trigger (MAC I = 0), the end of a memory block is indicated and the operation is ended.

MEMORY ADDRESS COUNTER II

The memory address counter II (MAC II) is similar to MAC I but is a 20-trigger counter used to locate an address in memory during the execution of a TMT, SND, TCT, BLM, TZB, TR 01 instruction, or a RWW operation. MAC II is used to indicate the address of information going into memory, except the TZB when it contains the character address. MAC II is reset and set to MAC I or the word register (WR). When the MAC II is set to the word register, the numerical bit structure from characters 0, 1, 2, and 3 of the word register are set into the triggers of the first four positions of MAC II. The zone bits from characters 0 and 3 are set into the fifth position of MAC II. When MAC II is set to MAC I, the numerical bit lines of all five positions of MAC I set all five positions of MAC II.

During a leave interrupt program (LIP) instruction, MAC II is set to the word register to restore MAC II to its proper address. This is necessary because contents of MAC II might have been changed by the interrupt program.

The MAC II can step either plus one or plus five. By stepping plus one, the units position locates the next character in the MBR to be processed. The step plus five locates the next block of five characters to be processed.

INSTRUCTION COUNTER

The instruction counter (IC) is a 17-trigger counter that contains the address of the instruction to be executed next. The reset and clear memory keys reset the IC to 00004. During the second cycle of I time, the IC is stepped plus five. On transfer instructions, the IC is reset and set to MAC I. The address is decoded and sent to MAR (in the 7302) to locate the instruction.

The units position of the instruction counter (IC) contains only one trigger. When the trigger is off it represents a 4; when on, it represents a 9. When the IC is reset off, it automatically sets up 00004, the address of the first instruction in memory. The first stepping pulse turns on the low-order trigger to represent 9. When the IC is stepped plus five again, the trigger is turned off and a step pulse is sent to the IC-10 trigger.

An auto-check stop comes up too late to prevent the stepping of the IC. Therefore, the IC will contain the address of the next instruction when the machine stops.

During the automatic interrupt or transfer to interrupt program (TIP), the contents of the IC are sent, through CPU and the storage-in switch, to the first four positions of word 0, CASU 15. The numerical bits of the first four orders of the IC are sent to characters 0 through 3 of word 0, CASU 15. Numerical bit lines from the fifth order of the IC are converted to zones over characters 0 and 3. The zone coding is the same as that used in memory addressing.

MEMORY ADDRESS REGISTER

The memory address register (MAR) is a 15-trigger register in the 7302 memory unit, used to drive the memory selection circuits. Outputs from MAR are decoded to select a group of ten characters in memory. The MAR 3 trigger status reads out five of the ten characters selected into memory. Outputs of MAC I, MAC II, and IC may be decoded and sent to MAR. The instruction or operation calling for data from memory determines which counter or register the MAR will be set to.

Storage Address Control Counters and Registers

STORAGE ADDRESS REGISTER

The storage address register (SAR) is an 11-trigger register used to supply the proper outputs to address a block of eight characters in storage. Addressing of the block uses SAR triggers 8 through 1024 and triggers 1, 2 and 4 are used for test purposes only. SAR triggers 8 through 128 may be set to the multiplexor or the storage address switch (SAS). These may address any block of eight characters in a bank. The operation being performed will determine whether the SAR triggers 8 through 128 will be set to SAS or the multiplexor. The bank in storage to be used is controlled by the SAR triggers 256, 512 and 1024. These SAR triggers must be set to SAS. The operation being performed determines which of the triggers will be on.

STORAGE ADDRESS COUNTER

The storage address counter (SAC) is an eight-trigger binary counter. The triggers 8 through 128 can address any group of eight characters within a selected bank.

For instructions using storage with no ASU coding, SAC would be set to SPC, and thus provide the address for the block of eight characters and also the address of the units position of the storage field. For instructions with ASU coding, SAC would be set to SSR.

When ASU coding is used, the units position of the storage field is always the units position of the selected ASU unit.

STORAGE SELECT REGISTER

The storage select register (SSR) is a four-trigger register that is set to the ASU coding of the address part of the instruction. This register is used to select a particular storage unit or identify a special type of instruction. When the accumulator storage is used, there are no bits in the zone portion of characters 2 and 3 of the instruction.

STARTING POINT COUNTER

The starting point counter (SPC) is an 11-trigger binary counter that can be used to address any character in storage. During the set-SPC instruction, all eleven SPC triggers are set to MAC I. For instructions using storage that contain no ASU coding, bank zero (accumulator) is selected. The block of eight characters to be addressed in storage is under control of the SPC triggers 8 through 128. This is done by first setting SAC to SPC, then setting SAR to SAC. SPC determines the location of the units position of the field in the accumulator; the high-order limit is determined by a storage mark. SPC can be stepped plus one, minus one, or 128.

Input-Output Address Control Register

SELECT REGISTER

The select register (SR) is an 18-trigger register that can be used to address I-O components and alteration switches or check indicators. During a select instruction or an auto-load operation, the select register is reset and set to MAC I. During a TIP or automatic interrupt, the contents of the select register are stored in word 3 of CASU 15. During a LIP instruction the contents of word 3 of CASU 15 are used to restore the setting of the select register.

The select register (except as disturbed by interrupts) remains constant between select instructions. Thus, if a particlar I-O device, alteration switch, or check indicator is selected, it remains selected until a select instruction or auto-load operation changes it. The select register is also reset by the clear memory and reset keys.

Memory Address Controls

Program operation is preceded by setting the instruction counter to the memory address of the first instruction to be executed, for example, to 00004 if the first

instruction is located in the first five positions of memory. The IC can also be manually set from the console to the address of any instruction in memory.

At the beginning of the instruction cycle, the memory address register (MAR) is set to the address held by the IC. The address held by MAR is decoded and selects the five memory positions containing the complete instruction as originally indicated by the IC.

The five characters making up the instruction are removed from memory and are set in the data register (DR). These characters held by the DR during the instruction cycle are then replaced in memory at the same location from which they were removed. The bits of the characters held by the DR are also made available to the operation register (OP REG), the initial address register (IAR), storage select register (SSR), MAC I, and the memory buffer register (MBR).

Core memory design fixes a relationship between the

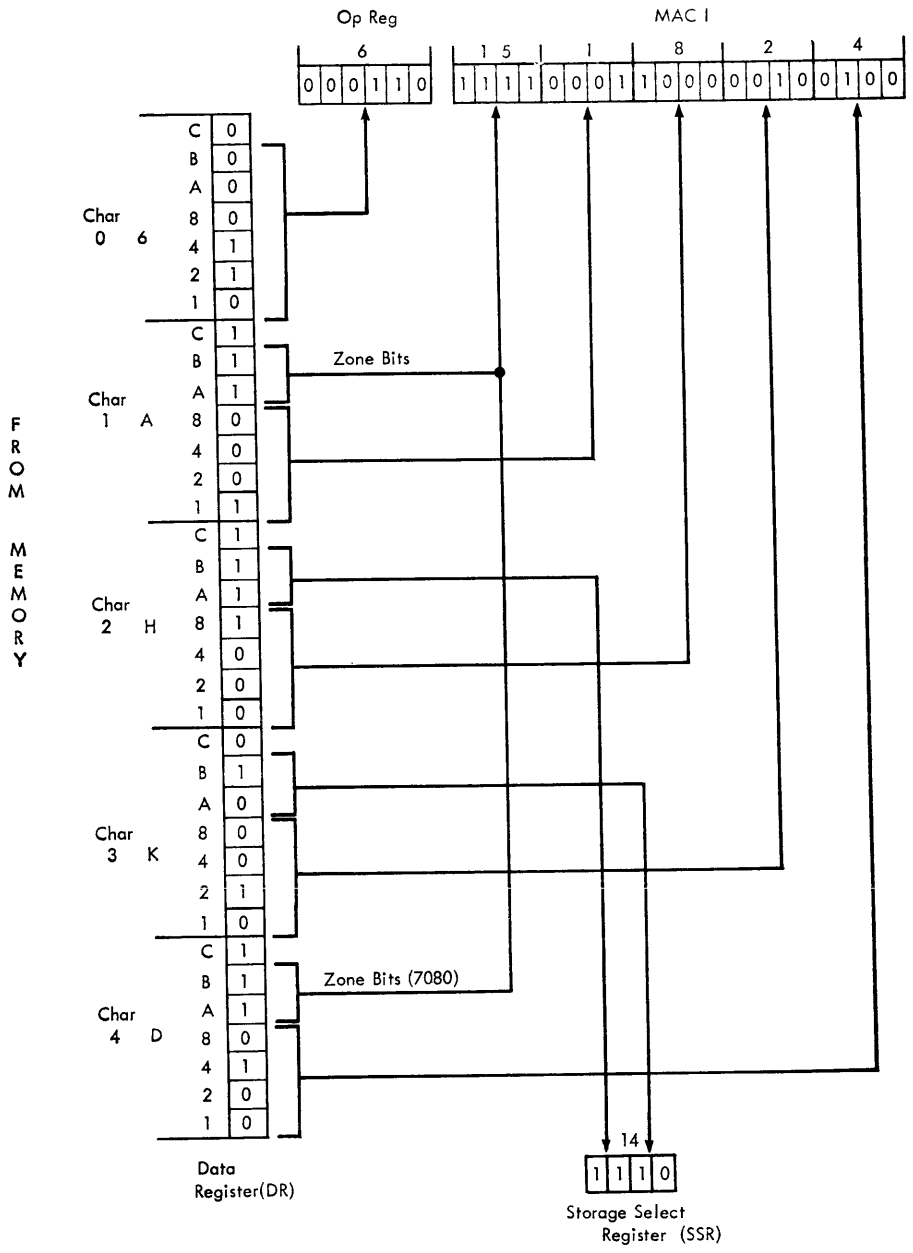


Figure 21. Data Register Operations (I-Time)

five selected memory positions and each of the five-character positions of the DR. Characters located at memory addresses ending in 0 or 5 are always placed in the character 0 position of the DR; addresses ending in 1 or 6 are placed in the character 1 position of the DR; and so on.

During the instruction cycle only, the character contained in the DR position 0 is placed in the operation register. The character is decoded to determine the operation to be performed and to activate the necessary machine circuitry to perform this instruction. If the character placed in the operation register is an invalid character, an instruction check error is indicated. An error is also indicated when the character is not one of the operation codes of the 7080. The character is held in the operation register from one instruction cycle to the next.

The four low-order positions of MAC I are set to only the numerical portion of the address part of the instruction held by the DR. The zone bits over the high- and low-order positions of the address portion of the instruction are set in the fifth position of MAC I. Zone bits over the tens and hundreds positions of the address are set in the SSR.

Figure 21 shows an instruction contained in the DR as 6AHKD, or add to memory from ASU 14, location 151824. The BCD characters are shown as they are actually represented in the register. The numerical portion of the instruction address is placed in the four low-order positions of MAC I, and the zone positions of the units and thousands positions are combined to form the fifth position of MAC I, the binary number 15 (Figure 22). The character 6 is routed to the operation register. Zone bits over the tens and hundreds positions of the address are set in the SSR, in this case the binary number 14.

In most instances, the address of the next instruction in memory is five memory positions higher than the address of the instruction being analyzed. By automatically stepping the IC plus five during the instruction cycle, the memory address of the next instruction to be used is determined.

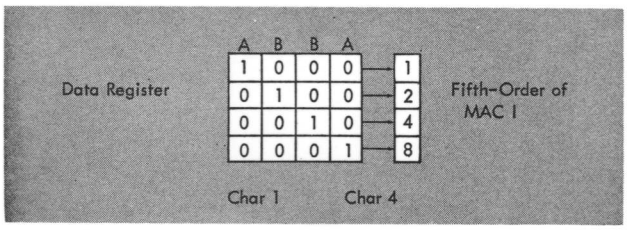


Figure 22. Zone Coding to Numerical Equivalents for the Fifth Position of MAC I

However, if the next instruction is not in sequence (for example, if a transfer is to be executed), the IC is set to MAC I. In this case, MAC I contains the address portion of the transfer instruction which is the location of the next instruction to be taken from memory.

If the address placed in MAC I during the instruction cycle is the address of an input-output unit, alteration switch, or check indicator, the select register is also set to MAC I, thereby selecting the addressed unit or device. The contents of the select register remain unchanged until another select instruction is executed.

The execution of some instructions requires the indication of two different memory addresses. A second memory address counter (MAC II) is provided for this purpose. MAC II is set to the address in the DR by first setting MAC I to the address in the DR and then setting MAC II to MAC I. The operation to be performed selects the particular memory address counter to be used.

At the beginning of an execution cycle that involves removing information from memory for processing, MAR is set to MAC I or MAC II, depending upon the instruction to be performed. During succeeding execution cycles, the memory address indicated by MAC I or MAC II can be increased or decreased (stepped) automatically under control of the instruction.

The address in MAR is decoded and the proper block of five characters is removed from memory and placed in the MBR via the DR. The addressed character of the five held by the MBR is indicated by the digit in the units position of MAC I through the character address register (CAR). The addressed character is routed from the MBR by the MBR-out switch.

From the MBR-out switch, the selected character can be routed through the arithmetic circuits to the result register. A character placed in the result register from the MBR or the SBR can be returned on the next cycle to the MBR or the SBR, depending upon the operation to be performed. If a character in the result register is to be returned to the MBR, it is routed through the MBR-in switch, to the position that originally held the address character. A character is routed from MBR to the adder each execution cycle until MBR needs new information or until the end of the instruction. Information in MBR is transferred to memory before a new group of five characters is transferred from memory to the MBR.

Storage Address Controls

A storage unit is designated by the zone information in the tens and hundreds positions of the address portion of the instruction. During the instruction cycle, the zone bits in the character 2 and 3 positions of the DR are set in the storage select register (SSR).

Storage is not used during an instruction cycle, but the particular unit to be used during the following execution time is determined. If no one bits are present

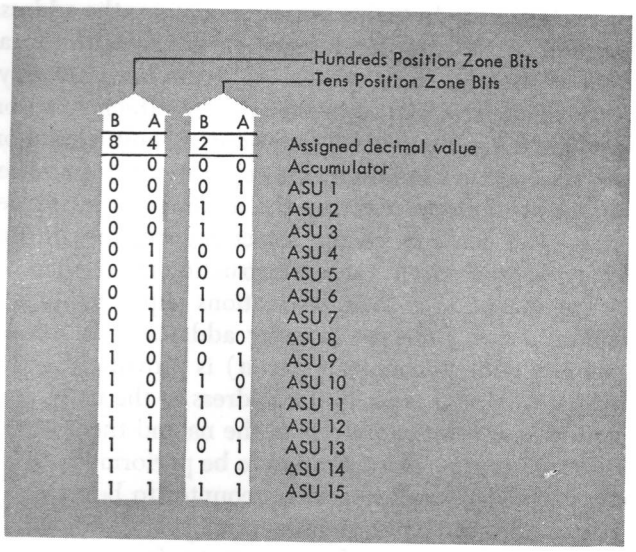


Figure 23. Storage Coding

in the SSR, accumulator storage is indicated. In this case, the storage address counter (SAC) is set to the storage position indicated by the starting point counter (SPC). This position may be within any storage bank.

One bits in the SSR indicate the use of an auxiliary storage unit or a channel auxiliary storage unit, depending upon the position of the SPC. The SAC is set to SSR and indicates the units position of the selected storage unit. Addressing any auxiliary storage unit (ASU) always sets the SAC to the units position of the addressed storage unit (Figure 23).

Some instructions have zone bits in the tens or hundreds position of the address portion of the instruction, but do not indicate the use of auxiliary storage. In this case, SSR is used only as an indicator for the selection of one of several possible types of operation. For example, the read 00 and read 01 instructions are differentiated by the fact that the read 01 instruction has zone bits over the tens position of the address portion of the instruction. Instructions using SSR as an indicator do not affect the data in storage.

At the beginning of an execution cycle involving the use of storage, the storage address register (SAR) is set to the storage address contained in SAC. The address in SAR is decoded and the proper block of eight characters is removed from storage through the word register (WR) and set in the storage buffer register (SBR). The addressed character is routed from the SBR by the SBR-out switch. The character in the SBR-out switch can be routed through the arithmetic circuits to the result register. From the result register, the character can be routed to MBR or SBR, depending upon the operation to be performed.

If the character is to be returned to SBR, it is routed from the result register one cycle later to the SBR-in switch and placed in SBR at the original address indicated by SAC. A character is routed from the SBR each execution cycle until the SBR needs new information or the operation is ended. Information in SBR is transferred to storage before a new group of eight characters is transferred to the SBR.

In the following description of the various 7080 instructions, reference is made to *accumulator* (ACC) and *storage units* (ASU). Four banks of central storage are available in the 7080 and the storage units that are used for these operations are *entirely* dependent upon the current setting of the *starting point counter* (SPC).

Any instruction that specifies the accumulator uses that bank of storage indicated by the current setting of the SPC. Instructions with ASU coding specify an ASU in:

1. Bank 1, if the SPC is set to any position within banks 0 or 1.
2. Bank 3, if the SPC is set to any position within banks 2 or 3.

Normally, bank 0 is used as the accumulator and bank 1 as auxiliary storage. However, the use of any of the banks is at the discretion of the programmer within the limitations of the system.

The SPC will always be reset to bank 0 by depression of the clear memory, auto-load, or reset keys.

Arithmetic Operations

The 7080 adds, subtracts, multiplies, and divides when given arithmetic instructions. These instructions can be applied to data stored in central storage or in memory. They are normally applied to specific numerical factors or fields, such as factors developed during calculation or fields selected from records.

To select a field from memory to be acted upon by an arithmetic instruction, the field is always addressed by the memory location of its units digit. The remaining digits of the field are automatically read from right to left until a non-numerical character is reached. All characters, including blanks, are considered non-numerical except the digits 0-9. Thus, a numerical field in memory is defined as beginning with the address of its units digit and extending to, but not including, the next left non-numerical character.

Arithmetic instructions are normally addressed to signed numerical fields. Both positive and negative fields in memory should be signed. Numerical fields are signed by placing a plus or minus sign indication over the units digit of the field. The absence of a zone or the presence of the A bit alone does not satisfy the requirements for a signed field.

The ASU coding of an arithmetic instruction, in conjunction with the prior setting of the starting point counter, defines the initial position of central storage upon which the instruction will act. The address specifies whether the accumulator or one of the auxiliary storage units is to be used. If the accumulator is addressed, the right-hand or low-order position of the storage field to be acted upon is indicated by the current setting of the starting point counter. This setting is normally in bank 0, thus defining a position within accumulator storage. If an auxiliary storage unit is addressed, the right-hand position of the storage field is the low-order position of the addressed ASU.

Reset and Add (H—RAD)

Function: This operation enters a numerical field from memory into ACC or ASU storage.

Address: The address specifies the units position of the field in memory and the storage unit to be used.

Limiting Factors: First non-numerical character to the left of the address character. Since special characters are all non-numeric, inclusion of these in a numeric field leads to incorrect results.

Mode: All.

Description: The reset and add instruction enters a numerical field from memory into central storage. If the accumulator is addressed, the first position of storage to be acted upon is indicated by the setting of the starting point counter. If an auxiliary storage unit is addressed, the first position of storage to be acted upon is the right-hand position of the addressed ASU.

Digits are entered into storage, starting with the specified right-hand digit of the memory field and continuing from right to left until a non-numerical character (any character except digits 0-9) is sensed. This non-numerical character and the zoning of the addressed digit of the memory field are not entered into storage.

The accumulator or auxiliary storage sign is set to plus when the addressed memory character has plus zoning and is set to minus when the character has minus zoning. If the addressed character has neither plus nor minus zoning, an error is indicated and the sign of the field is interpreted as plus. Refer to 'Sign Check Indicator." The sign is always set to plus when the result in storage is zero. The left-hand limit of the storage field is automatically set by a storage mark *(a)*

stored next to the last digit entered from memory.

When the memory field exceeds the capacity of an auxiliary storage unit or channel auxiliary storage unit, the field automatically extends into the adjacent unit with proper positioning of the storage mark in this unit.

The reset and add instruction does not affect the field in memory or the setting of the starting point counter.

Special Case: When the numerical portion of the character addressed by the instruction is 0000, such as characters &, –, or blank, the character is entered into storage as a zero (0 00 1010). The accumulator or auxiliary storage sign and the sign check indicator are set according to rules stated above.

EXAMPLES, RESET AND ADD

	STORAGE BEFORE		STORAGE AFTER		SIGN CHECK
MEMORY	STORAGE	SIGN	STORAGE	SIGN	IND
$\overset{+}{4}456^{-}$	a23456	+	a456	–	
$\overset{-}{4}456^{+}$	a23456	–	a456	+	
$\overset{-}{4}b56^{+}$	a1234	+	a56	+	
$\overset{+}{4}456$	a1234	–	a456	+	On
$E456^{-}$	a2345	+	a456	–	
$T000^{-}$	a1111	+	a000	+	
4bbb	a111	+	a0	+	On
ST	a4567	+	a3	+	On

Add (G—ADD)

Function: A numerical field in memory is added to a factor in central storage.

Address: The address specifies the units position of the memory field and the storage unit to be used.

Limiting Factors: The first non-numerical character to the left of the addressed memory character.

Inclusion of special characters in fields to be added leads to incorrect results.

Mode: All.

Description: The operation adds a numerical field in memory to a factor in central storage. If the accumulator is addressed, the first position of storage to be acted upon is indicated by the setting of the starting point counter. If an auxiliary storage unit is addressed, the first position of storage to be acted upon is the right-hand position of the addressed ASU.

Digits are added into storage starting with the specified right-hand digit of the memory field and continuing from right to left until a non-numerical character is sensed. This non-numerical character is not added to the storage factor.

The result in the storage unit is the sum of the storage factor and the specified memory field. The result replaces the original storage factor. The field in memory and the setting of the starting point counter are not affected.

The accumulator or auxiliary storage sign is set according to the rules of algebra for addition. When the addressed character has neither plus nor minus zoning, a sign check error is indicated and the sign of the memory field is interpreted as plus. Refer to "Sign Check Indicator." The sign is always set to plus when the result in storage is zero.

The left-hand limit of the result is automatically set by a storage mark stored next to the highest-order digit. The length of the result is equal to the longer of the two fields being added, unless a carry is made out of the high-order position. If the machine is in 705 I-II mode or the 904 switch is on program, the result is extended one position to include the carry as its most significant digit, the storage mark is positioned to the left of this digit, and the overflow check is turned on. If the machine is in 705 III or 7080 mode and the 904 is on automatic, the overflow may be detected before the 8-character storage buffer is emptied. In this case, the answer will not be in the storage unit. Refer to "Overflow Check Indicator."

When the overflow exceeds the capacity of an auxiliary storage unit, the carry is made into the adjacent unit with proper positioning of the storage mark in this unit.

EXAMPLES, ADD

	STORAGE BEFORE		STORAGE AFTER		
MEMORY	STORAGE	SIGN	STORAGE	SIGN	CHECK IND
$\overset{+}{6}234^{+}$	a23	+	a257	+	
$\overset{+}{6}235^{+}$	a23	–	a212	+	
$\overset{+}{6}235^{-}$	a23	+	a212	–	
$\overset{+}{6}235$	a23	+	a258	+	Sign Check On
$\overset{+}{1}2345$	a15	+	a2360	+	Sign Check On
$b89^{-}$	a20	–	a109	–	Overflow Check On
$b89^{-}$	a89	+	a00	+	

Execution of the add instruction in the 705 I-II mode is not completed until the end of both the memory and storage fields is reached, plus any machine cycles necessary to handle carries propagated beyond the length of the two fields.

Execution of the instruction in the 705 III or 7080 mode is terminated at the end of the memory field, plus any machine cycles necessary to handle carries propagated beyond the length of the memory field.

In the 705 I-II mode, it is possible to remove zoning

from an entire storage field by adding a zero opposite in sign to the storage field (additions involving like signs can produce an overflow condition). When operating in the 705 III or the 7080 mode, the results are:

Add:	Storage	aABCD+
	Memory	b $\bar{0}$
	Result	aAB34+

Thus to strip the zoning from the entire field when operating in the 705 III or the 7080 mode, add a field of zeros, opposite in sign to that of the storage field, and equal to the length of (or one character less than) the storage field. For example:

Add:	Storage	aABCD+
	Memory	b000$\bar{0}$
	Result	a1234+

NOTE: The addition of special characters having multiple digits whose sum exceeds 9 (8-3, 8-4 combinations) produce inconsistent results.

Reset and Subtract (Q—RSU)

Function: This operation enters a numerical field from memory into central storage.

Address: The address specifies the units position of the memory field and the storage unit to be used.

Limiting Factors: First non-numerical character to the left of the addressed character.

Inclusion of special characters in numeric fields leads to incorrect results.

Mode: All.

Description: The reset and subtract instruction enters a numerical field from memory into central storage. If the accumulator is addressed, the first position of storage to be acted upon is indicated by the setting of the starting point counter. If an auxiliary storage unit is addressed, the first position of storage to be acted upon is the right-hand position of the addressed ASU.

Digits are entered into storage, starting with the specified right-hand digit of the memory field and continuing from right to left until a non-numerical character is sensed. This non-numerical character and the zoning of the addressed digit of the memory field are not entered into storage.

The accumulator or auxiliary storage sign is set to minus when the addressed memory character has plus zoning and is set to plus when the character has minus zoning. If the addressed character has neither plus nor minus zoning, an error is indicated and the sign of the memory field is interpreted as plus, thus setting the storage sign minus. The sign is always set to plus when the result in storage is zero.

The left-hand limit of the storage field is automatically set by a storage mark (a) stored next to the last digit entered from memory.

When the memory field exceeds the capacity of an auxiliary storage unit, the field automatically extends into the adjacent unit with proper positioning of the storage mark in this unit.

The field in memory and the setting of the starting point counter are not affected by the reset and subtract instruction.

Special Case: When the numerical portion of the character addressed by the instruction is 0000 (& — blank), the character is entered into storage as a zero (0 00 1010). The accumulator and auxiliary storage sign and the sign check indicator are set according to the rules stated above.

EXAMPLES, RESET AND SUBTRACT

	STORAGE BEFORE		STORAGE AFTER		SIGN
MEMORY	STORAGE	SIGN	STORAGE	SIGN	CHECK IND
$\overset{+}{4}456\bar{}$	a11111	+	a456	+	
$\overset{+}{4}456\overset{+}{}$	a1	−	a456	−	
4b5$\overset{+}{6}$	a11	+	a56	−	
T0000	a1	−	a0000	+	On, see note
4bbb	a111	−	a0	+	On
ST	a11	−	a3	−	On
A1	a1	−	a1	−	On

NOTE: If the resulting storage field is zero (regardless of memory sign), the sign is set to plus.

Subtract (P—SUB)

Function: The subtract instruction subtracts a numerical field in memory from a factor in accumulator or auxiliary storage.

Address: The address part of the instruction specifies the location of the field in memory and the storage unit to be used.

Limiting Factors: The first non-numerical character to the left of the addressed character.

Inclusion of special characters in fields to be used in subtraction leads to incorrect results.

Modes: All.

Description: Digits are subtracted from storage starting with the specified right-hand digit of the memory field and continuing from right to left until a non-numerical character is sensed. This non-numerical character is not subtracted from storage.

The result in accumulator or auxiliary storage is the difference between the storage factor and the specified memory field. The result replaces the original storage factor.

The accumulator or auxiliary storage sign is set according to the rules of algebra for subtraction. When the addressed character has neither plus nor minus zoning, an error is indicated and the sign of the field is interpreted as plus. Refer to "Sign Check Indicator." The sign is always set to plus when the result in storage is zero.

The left-hand limit of the result is automatically set by a storage mark next to the highest-order digit.

The length of the result is determined in the same manner as for Add. See Add instruction for full explanation.

The subtract instruction does not affect the field in memory.

NOTE: See Add instruction to strip the zoning from a storage field and for terminating conditions. Also see note pertaining to addition of special characters.

Multiply (V—MPY)

Function: A factor in memory is multiplied by a factor in accumulator storage (storage bank 0). The field in memory is the multiplicand and the storage factor is the multiplier. The product is developed in accumulator storage.

Address: The address specifies the units position of the memory field.

Limiting Factors: First non-numerical character to the left of the addressed memory character.

Inclusion of special characters in multiplier or multiplicand leads to incorrect results.

Mode: All.

Description: The multiply instruction causes a field in memory (multiplicand) to be multiplied by a field in accumulator storage (multiplier) (see note). The units position of the multiplier is determined by the initial setting of the starting point counter. The product is developed in accumulator storage 128 positions away from the units position of the multiplier. At completion of the operation the starting point counter is located at the units position of the product, that is, 128 positions away from its initial position.

The number of digits in the product is equal to the sum of the number of digits in the multiplier and multiplicand. A maximum product of 128 digits can be obtained.

When the two factors differ considerably in length, some computation time can be saved by using the smaller of the two fields as the multiplier.

The accumulator sign is set to plus if both multiplier and multiplicand have like signs, and minus if they have unlike signs. When the addressed character of the field in memory has neither plus nor minus zoning, an error is indicated and the sign of the field is interpreted as plus. Refer to "Sign Check Indicator."

Only numerical fields can be used in multiplication. The use of non-numerical fields produces inconsistent results.

The multiplier may be recovered in accumulator storage by executing the instruction SHR 00128. Refer to "Shorten." If the initial setting of the starting point counter is known, the multiplier may also be obtained by executing an appropriate set-starting-point-counter instruction. Refer to "Set Starting Point Counter." The product may be half-adjusted by use of the round instruction.

EXAMPLES, MULTIPLY

	ACC 00 BEFORE		ACC 00 AFTER		
MEMORY	STORAGE	SIGN	STORAGE	SIGN	CHECK IND
280	a7	−	a560	−	
b3	a2	+	a06	+	
$ 25	a31	−	a0775	+	
65	a007	+	a0035	−	
b5	a007	+	a0035	+	Sign Check on

NOTE: It is possible to perform multiplication in storage banks other than accumulator storage. However, because of the nature of the functions which these other banks perform, it is generally impractical to perform this operation in any bank other than bank 0. For this reason, care should be taken to insure that the starting point counter is positioned within bank 0 before a multiply operation.

Divide (W—DIV)

Function: A factor normally in accumulator storage (storage bank 0) is divided by a field in memory. The memory field is the divisor and the storage factor the dividend. The quotient is developed in accumulator storage.

Address: The address specifies the units position of the memory field.

Limiting Factors: First non-numerical character to the left of the addressed memory position.

Inclusion of special characters in dividend or divisor leads to incorrect results.

Mode: All.

Description: The divide instruction causes a factor in accumulator storage specified by the location of the starting point counter to be divided by the field in memory specified by the address part of the instruction. (See Note.) Thus, the memory field is the divisor and the storage factor is the dividend. The quotient is developed in accumulator storage.

The number of digits in the quotient is equal to the number of digits in the dividend less the number of digits in the divisor, including insignificant zeros. A maximum dividend length of 128 digits can be used.

1. The dividend must contain a greater number of digits than the divisor. Otherwise, the division is ignored, the zero indicator is turned on, and the machine proceeds to the next instruction.

2. The divisor must have a greater absolute value than an equal number of digits taken from the left end of the dividend. For example, 7 ÷ 2 cannot be performed because the divisor, 2, is less than the dividend 7; 07 ÷ 2 can be performed because the divisor 2 is of greater value than the high-order digit of the dividend, 0; 1234 ÷ 13 can be performed because the divisor 13 is of greater value than the two high-order digits of the dividend, 12. This rule can be satisfied by inserting zeros in the high-order positions of the dividends as required. If this rule is not satisfied:

a. The overflow check indicator and the zero indicator turn on.

b. The division is not completed.

c. A single zero replaces the contents of accumulator storage (quotient).

d. The machine proceeds to the next instruction.

e. The accumulator sign remains the same as that of the dividend.

The accumulator sign is plus if the divisor and dividend have like signs, and minus if they have unlike signs. When the right-hand character of the field in memory has neither plus nor minus zoning, an error is indicated and the sign of the field is interpreted as plus. Refer to "Sign Check Indicator."

Only numerical fields may be used in division. Non-numerical fields produce inconsistent results.

The quotient is developed to the right of a storage mark which is positioned 128 positions to the left of the storage mark defining the dividend. At the completion of the operation, the starting point counter is positioned at the units position of the quotient. The remainder always occupies the same accumulator positions as the original dividend. For example, after dividing 02333 by 111, accumulator storage would appear as in Figure 27A.

After division, the remainder may be recovered in one of three ways:

a. By multiplying the quotient by the divisor and subtracting the result from the dividend.

b. By performing a shorten operation with an address part equal to 128 − n, where n is the number of digits in the divisor. (Refer to "Shorten.")

c. By executing an appropriate set-starting-point-counter instruction, when the setting of the SPC is known. (Refer to "Set Starting Point Counter.")

For example, if a shorten 00128 is given, the starting point counter moves 128 positions to the left and stops under the position containing the second zero to the right of the remainder storage mark (Figure 27B). However, the starting point counter is to be placed under the 2. This position is three positions (number of digits in divisor) to the right. Therefore, shorten 00125 places the starting point counter properly (Figure 27C).

Similar logic may be used in developing a proper address for a set-starting-point-counter instruction.

A storage mark is automatically placed at the right of the remainder at the beginning of the division operation and is used to stop the division.

The number of significant digits in the remainder can never exceed the number of digits in the divisor. Therefore, it is usually advantageous to set left the number of digits in the divisor before storing or using the remainder.

EXAMPLES, DIVISION

MEMORY	ACCUMULATOR BEFORE STORAGE	SIGN	ACCUMULATOR AFTER STORAGE	SIGN	CHECK INDICATOR
A50	a2501	+	a50	+	
b50	a511	+	a0	+	Zero on Overflow on
b50	a55	+	a55	+	Zero on
b50	a12700	+	a254	−	
b50	a12700	+	a254	+	Sign check on
b50	a604	−	a0	−	Zero on Overflow on

NOTE: It is possible to perform division in storage banks other than accumulator storage. However, because of the nature of the functions which these other banks perform, it is usually impractical to perform this operation in any bank other than bank 0. For this reason, care should be taken to insure that the starting point counter is positioned within bank 0 prior to a division operation.

Division by Zero

Division by zero always violates the rule that the divisor must be greater than the value of an equal number of digits taken from the left end of the dividend. However, when zero is divided by zero, the violation of this rule does not turn on the overflow check indicator.

In most divisions, it is necessary to know a great deal about the divisor and its relationship to the dividend. Where this is not the case, it is recommended that the divisor be examined to determine if it is zero. If it is zero, a transfer may be made to examine the dividend or to take other corrective action.

Store (F—ST)

Function: A numerical field in central storage is placed in memory.

Address: The address specifies the memory position (right-hand) where the field from storage is to be placed and the storage unit to be used. The storage unit addressing defines the initial position of central storage upon which the instruction will act.

Limiting Factors: First storage mark to the left of the addressed character in storage.

Mode: All.

Description: A numerical field in central storage is placed in memory by a store instruction. If the accumulator is addressed, the first position of storage to be acted upon is indicated by the setting of the starting point counter. If an auxiliary storage unit is addressed, the first position of storage to be acted upon is the right-hand position of the addressed ASU.

The right-hand digit of the storage field is stored at the specified memory address. The remaining digits to the left are stored in successively lower memory positions until the storage mark is sensed. All digits from the position of the starting point counter (or division point of an ASU) to the storage mark are stored.

The sign of the accumulator or auxiliary storage is converted to plus or minus zoning and is placed over the units position of the field in memory.

When the character in the next lower memory position is numerical, this character is signed plus to define properly the stored field. A non-numerical character is not affected. The store instruction does not affect the field in storage or the setting of the starting point counter.

EXAMPLES, STORE

ACC or AUX STORAGE	STORAGE SIGN	MEMORY BEFORE	MEMORY AFTER
a48	−	1729	1748
a67	+	1729	1767
a592	−	3415	3592
a738	+	3415	3738
a7468	−	Frame	F7468
a35	−	F16	F35

If the store instruction is used on non-numerical fields in storage, the zone information is removed and invalid characters can be placed in memory. Any character, other than the first character of the storage field, with 01 or 10 zoning produces an invalid character in memory. Characters with 11 zoning do not produce invalid characters in memory.

Add to Memory (6 — ADM)

Function: A field in central storage is added to a field in memory. The field from storage may be added to memory in two ways, depending upon whether the memory field is signed or unsigned. The result replaces the original memory field and the field in storage is unchanged.

Address: The address specifies the units position of the memory field and the storage unit to be used. The storage unit addressing defines the initial position of central storage upon which the instruction will act.

Limiting Factors: (1) Signed memory field — first non-numerical character to the left of the addressed memory character; (2) Unsigned memory field — first storage mark to the left of the addressed character in storage.

Mode: All.

Description, Signed Memory Field: The addition follows the rules of algebra. The addressed field in memory starts with its right-hand signed digit and continues to the left until a non-numerical character is reached. Any carry-over of the result into the position of the next non-numerical character in memory is ignored and the overflow check indicator is not turned on. Only numerical portions of the characters in storage are added. Both plus and minus fields in storage may be added. The proper sign of the result is placed over the addressed character in memory. The setting of the starting point counter is not affected.

NOTE: If the resulting sum in this operation is zero, the sign is not automatically set to plus as it is in the add instruction.

EXAMPLES, ADD TO MEMORY (SIGNED FIELDS)

ACC OR AUX STORAGE	SIGN	MEMORY BEFORE	MEMORY AFTER
a33	+	5663	5696
a25	−	5425	5400
a625	+	4676	4301
a676	−	4625	4051
a12676	−	4625	4051
a12121	−	B456	B335
a3	+	A&	A3

Execution of an ADM instruction (signed memory field) terminates no later than at the end of the memory field. It could terminate sooner, depending upon carry requirements, at or after the end of a shorter storage field.

Through the use of the ADM instruction (signed field), any given memory location can become an accumulative counter into which a number may be added with this one instruction.

Description, Unsigned Memory Field: The addition is not algebraic. It begins with the right-hand digit of storage and the addressed character in memory and continues from right to left until the storage mark is reached.

When non-numerical characters, including blanks, are encountered in the memory or storage fields, both zones and digits are added. The zone positions of the characters are added separately as binary numbers. Any carry-over is added to the next high-order zone position, except a carry beyond the last character of the storage field, which is disregarded.

NOTE: The addition of special characters having multiple digits whose sum exceeds ten (8-3, 8-4 combinations) produces inconsistent results. Example: The sum of a $ sign (010 1011) and a minus 0 is 3 in the 705 III mode; but in the 7080 mode, the sum is 1.

The numerical parts of the characters are added decimally. Any carry-over is added only to the numerical part of the next high-order position, except a carry-over beyond the last character of the storage field. Any carry from the numerical portion of the last character of the field is binarily added to the zone of that character. The setting of the starting point counter is not affected.

The three possible zones are indicated in the following example by placing binary notation over the numerical portion of the character. The zero zone is numbered 01, the eleven zone 10, and the twelve zone 11. In binary, this corresponds to zones 1, 2, and 3, respectively.

EXAMPLES, ADD TO MEMORY (UNSIGNED FIELDS)

ACC or AUX STORAGE	SIGN	MEMORY BEFORE	MEMORY AFTER
00 00 a 4 0	+	00 00 00 00 W 1 2 3 4	00 00 00 00 W 1 2 7 4
00 00 00 00 a 0 9 0 0	+	00 00 00 00 00 R 0 1 1 1 1	00 00 00 00 00 R 0 2 0 1 1
00 00 00 00 a 9 9 0 0	+	00 00 00 00 R 0 1 1 1	01 00 00 00 R 0 0 1 1
a &	+	00 00 2 6	00 11 2 6
a −	−	00 00 2 6	00 10 2 6
01 00 00 00 a 9 9 0 0	+	11 00 00 00 R 0 1 1 1	01 00 00 00 R 0 0 1 1

Through the use of the ADM instruction (unsigned field), a method is provided for incrementing any direct instruction address in memory, less than 40,000, to any other address less than 40,000. The instruction also can be used to change storage unit designations of instructions located in memory.

Add Address to Memory (@−AAM)

Function: Up to five digits (705 III mode) or six digits (7080 mode) in central storage are added to a four-character address in memory to develop an incremented memory address.

Address: The address, which must end in either 4 or 9, specifies the units position of the memory field and the storage unit to be used. The storage unit addressing defines the initial position of central storage upon which the instruction will act.

Limiting Factors: None.

Mode: All.

Description, 705 III Mode: A five-digit numerical field in storage is added to a four-character address in memory. The result is a new four-character address in memory with proper zoning over the units and thousands positions. The value of the five-digit storage field should be less than or equal to 79,999, wrap around occurs at 80,000, and the A bit position of the units character in memory is not affected.

If the field in storage is greater than five digits, the instruction adds only the first (low-order) five digits and ignores the remainder. The storage field may also be less than five digits, in which case it is treated as a five-digit field with 0's to the left of significant digits.

Description, 7080 Mode: A six-digit numerical field in storage is added to a four-character address in memory. The value of the six-digit storage field should be less than or equal to 159,999, and wrap-around always occurs at 160,000, regardless of the size of memory.

If the field in storage is greater than six digits, the instruction adds only the first (low-order) six digits and ignores the remainder. The storage field may also be less than six digits, in which case it is treated as a six-digit field with 0's to the left of significant digits.

In both the 705 III and 7080 modes, the zone bits over the tens and hundreds positions in memory (the ASU designation) add in binary fashion with any zoning over the corresponding positions in storage. In this regard, the AAM instruction works in the same way as the add-to-memory (ADM) instruction for an unsigned field in memory. However, it is unlike ADM in that the addition of the zones over these two digits is independent of zone addition of any other positions, and any carry from the hundreds position zone is disregarded.

All addition with the AAM instruction is non-algebraic, always adding the absolute value of the amount in storage regardless of the sign. Therefore, subtraction must be accomplished by taking advantage of wrap-around.

Sign (T—SGN)

Function: This operation removes zone bits from a memory character and places them in central storage as an ampersand or dash.

Address: The address specifies the character to be processed and the storage unit to be used. The storage unit addressing and the setting of the starting point counter together define the initial position of central storage upon which the instruction will act.

Limiting Factors: None.

Mode: All.

Description: The sign instruction is used to remove any zone from a memory character and place it in storage as an ampersand or dash. The character affected and the storage unit used are specified by the address part of the instruction. If the accumulator is addressed, the first position of storage to be acted upon is indicated by the current setting of the starting point counter. If an auxiliary storage unit is addressed, the first position of storage to be acted upon is the right-hand position of the addressed ASU when the starting point counter is positioned within storage bank 0 or 1, but it is the right-hand position of the corresponding channel ASU when the starting point counter is positioned elsewhere.

When the zoning of the addressed character in memory is minus, a dash (minus zone) is placed in storage, the storage field length is set to one position, and the storage sign is set to minus.

When the zoning of the addressed character in memory is other than minus, an ampersand (plus zone) is placed in storage and the storage field length is set to one position. The storage sign is set to plus.

The addressed character remains in memory with 00 zoning unless that character is an ampersand, a dash, or a blank. In these cases, the character remaining in memory is a blank.

The sign placed in accumulator or auxiliary storage as an ampersand (plus) or a dash (minus) may be given to any character in memory that is not already zoned. The add-to-memory is used for this purpose and the character to be signed is specified by the address part of the add-to-memory instruction.

EXAMPLES, SIGN

BEFORE			AFTER		
ACC OR AUX STORAGE	SIGN	MEMORY CHARACTER	ACC OR AUX STORAGE	SIGN	MEMORY CHARACTER
a123456	+	B	a&	+	2
aEDPM	+	R	a—	—	9
a&	+	$\bar{4}$	a—	—	4
a16AB	—	$\dot{4}$	a&	+	4
a16AB	+	&	a&	+	b
a16AB	+	—	a—	—	b
a16AB	+	b	a&	+	b

Shift Operations

The 7080 can perform shift operations to adjust field length in central storage. Fields may be lengthened to the right or left with the addition of zeros or may be shortened by moving the starting point counter or the storage mark as required. These operations are useful for eliminating insignificant zeros from calculated results, adjusting the dividend, placing the decimal in division operations, preparing storage units for load operations, and so on.

The shorten, lengthen, and round instructions may be used only by specifying the accumulator. The set left instruction may specify either the accumulator or any auxiliary storage unit. Maximum address for shift operations is 40,000. SET 51,000 will set left 11,000 positions.

Set Left (B—SET)

Function: This operation adjusts the length of a field in central storage to the left by positioning the storage mark.

Address: In an accumulator, the address indicates the number of positions the storage mark is to be located to the left of the starting point counter. In an auxiliary storage unit, the address indicates the number of positions the storage mark is to be located to the left of the low-order position of the unit.

Limiting Factors: Number of positions specified by the address portion of the instruction, up to 20,000. Since storage banks are 256 positions long, maximum effective address is 255.

Mode: All.

Description: The length of an accumulator or auxiliary storage field is adjusted to the number of characters specified by the address part of the instruction. In an accumulator, the operation starts with the character in the starting point counter position and continues to the left, character by character, until the

number of storage positions specified by the address have been examined. In an auxiliary storage unit, the operation starts at the low-order position of the specified unit.

When a storage mark is sensed, it is replaced by a zero and zeros are placed to the left in all remaining high-order positions of the adjusted field (Figure 24A). When the storage mark is not sensed, a storage mark is inserted to the left of the high-order character of the adjusted field and no characters are replaced with zeros (Figure 24B). The set left instruction may, therefore, either decrease the number of characters in the field by moving the storage mark toward the right, or add zeros by moving the storage mark toward the left, as required.

A group of adjacent auxiliary storage units may be coupled by a set left instruction. Set left 00035 specifying ASU 01 uses auxiliary storage 01, through 02, to the fourth position of storage unit 03. The length of the resulting field is 35 positions (Figure 25). Zeros are added in the normal manner when the storage mark is moved to the left, or, when a storage mark is entered before the one which previously limited one field, the number of characters in the field is decreased.

A subsequent store instruction, when addressed to auxiliary storage 01, stores all 35 positions of the field. The store instruction, addressed to storage 03, stores only the three digits from the low-order position of 03 to the storage mark.

Because each storage bank operates as a circle, an address part greater than 00256 causes the machine to examine the entire circle as many times as the number 256 can be completely subtracted from the address. The remainder following the last subtraction is the number of positions from the starting point to the storage mark (Figure 26).

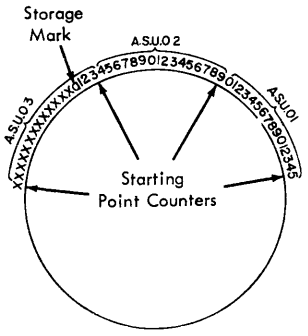


Figure 25. Auxiliary Storage Coding

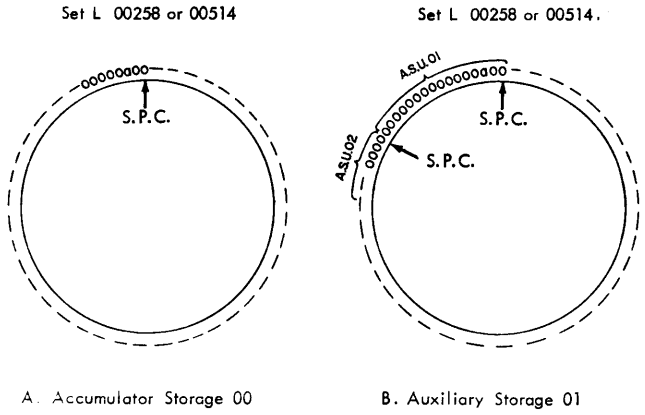


Figure 26. Set Left Instruction

All accumulator or auxiliary storage positions contain zeros following an instruction of this sort, with the exception of the position containing the storage mark. For example, set left 00258 or set left 00514

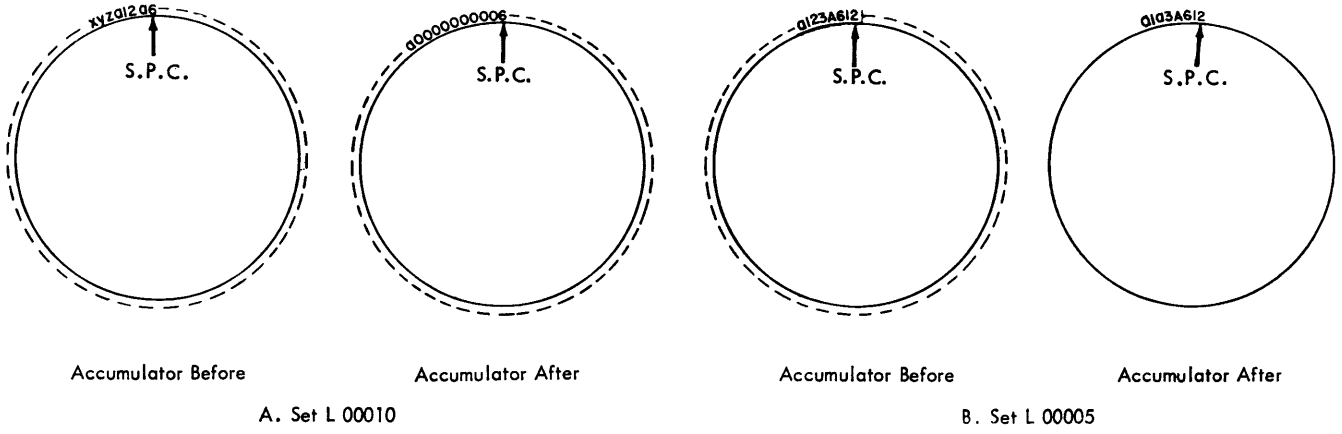


Figure 24. Set Left

places the storage mark in accumulator storage 00 in the same position as set left 00002. All positions of the resulting storage field, except the second position to the left of the starting point of the field, contain zeros.

EXAMPLES, SET LEFT

INSTRUCTION	STORAGE BEFORE	SIGN	STORAGE AFTER	SIGN
SET 00004	a52	−	a0052	−
SET 00002	a0052	+	a52	+
SET 00001	a52	+	a2	+
SET 00003	a2000	−	a000	+

The SET 00000 instruction places a storage mark at the position of the starting point of the field, turns on the zero indicator, and sets the sign of accumulator or auxiliary storage units to plus.

Shorten (C—SHR)

Function: This operation shifts the starting point counter of central storage to the left the number of positions specified by the address part of the instruction.

Address: The address indicates the number of positions the starting point counter is to be moved.

Limiting Factors: Movement of the starting point counter the specified number of positions.

Mode: All.

Description: The shorten instruction shifts the starting point counter of central storage to the left. The number of positions moved is specified by the address part of the instruction. Because the field in storage consists of those characters between the position of the starting point counter and the storage mark, the movement of the starting point counter to the left has the effect of removing characters from the right end of the storage field (Figure 27).

The shorten 00000 instruction has no effect. The position of the starting point counter, when using address parts greater than 00256, can be found by considering the circular nature of storage banks and their total capacity of 256 positions. Thus, shorten 00769, 00257, and 00001 all have the same effect.

When, as a result of a shorten instruction, the field in accumulator storage is zero, the accumulator sign is always set to plus.

EXAMPLES, SHORTEN

INSTRUCTION	ACCUMULATOR BEFORE STORAGE	SIGN	ACCUMULATOR AFTER STORAGE	SIGN
SHR 00002	a1246	+	a12	+
SHR 00001	a1246	−	a124	−
SHR 00000	a1246	−	a1246	−
SHR 00002	a0046	−	a00	+

Lengthen (D—LNG)

Function: This operation shifts the starting point counter of central storage to the right the number of positions specified by the address part of the instruction.

Address: The address indicates the number of positions the starting point counter is to be moved.

Limiting Factors: Movement of the starting point counter the specified number of positions.

Mode: All.

Description: The lengthen instruction shifts the starting point counter of central storage to the right. The address part of the instruction specifies the number of positions to be moved.

A zero is inserted to the right of the field in storage for each position moved by the starting point counter. The number of zeros inserted is designated by the address part of the instruction.

A storage mark is always placed in the position to the right of the starting point counter. This occurs even in the case of LNG 00000, which performs no

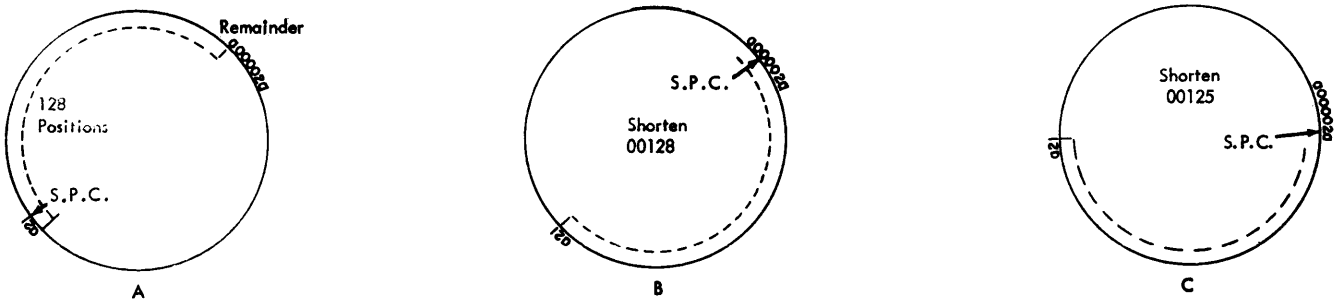


Figure 27. Shorten Instruction

lengthening function. Because of the circular nature of storage banks, an address part greater than 00254 fills a bank with 255 zeros and a storage mark. The final position of the starting point counter can be found by repetitive subtraction of 256 from the address part. The remainder, following the last subtraction, indicates the position of the counter.

EXAMPLES, LENGTHEN

INSTRUCTION	ACCUMULATOR BEFORE	ACCUMULATOR AFTER
LNG 00002	a5723	a572300
LNG 00005	a1	a100000
LNG 00001	a4689	a46890

Round (E—RND)

Function: This operation shifts the starting point counter of central storage to the left the number of positions specified by the address part of the instruction. A 5 is added to the digit to the right of the final position of the starting point counter.

Address: The address indicates the number of positions the starting point counter is to be moved.

Limiting Factors: Movement of the starting point counter the specified number of positions, addition of the numerical 5, and any resulting carries.

Mode: All

Description: The round instruction moves the starting point counter to the left the number of positions specified by the address part of the instruction. The field remaining in storage is limited to those digits between the storage mark and the new position of the starting point counter.

A 5 is added to the digit to the right of the final position of the starting point counter. Any resulting carry is added to the units digit of the remaining storage field.

When a carry is made out of the high-order position of the original field, the result is extended one position to the left to include the carry, and the overflow check indicator is turned on.

The instruction round 00000 has no effect.

When the result in storage is zero, the sign is always set to plus.

When the position where the 5 is to be added happens to contain a storage mark, the 5 is placed in storage at this point, but a storage mark is placed at the position of the starting point counter. Thus, the result has a zero field length. In this case, the overflow check indicator is turned on.

NOTE: In the 705 I-II mode, the zero indicator is turned on and the storage sign is not changed. In the 705 III and 7080 modes, the zero indicator is *not* turned on and the storage sign is not changed with the overflow switch in program position.

EXAMPLES, ROUND

INSTRUCTION	ACC 00 BEFORE STORAGE	ACC 00 BEFORE SIGN	ACC 00 AFTER STORAGE	ACC 00 AFTER SIGN	CHECK IND
RND 00002	a5653	+	a57	+	
RND 00002	a5653	−	a57	−	
RND 00004	a98912	+	a10	+	Overflow on
RND 00001	a349	+	a35	+	
RND 00002	a0049	−	a00	+	
RND 00003	a146a41	+	a14a	+	Overflow on

Set Starting Point Counter (,—SPC 00)

Function: This operation sets the starting point counter to the position of central storage specified by the address part of the instruction.

Address: The address specifies the position of storage to which the starting point counter is to be set. The storage address takes the following form:

THOUSANDS POSITION: the digits 0-3 designate one of the four 256-character storage banks.

HUNDREDS POSITION: the digits 0-7 identify one of the eight four-word sets within a bank.

TENS POSITION: the digits 0-3 identify one of the four eight-character words within a set.

UNITS POSITION: the digits 0-7 identify one of the eight characters in a word.

Limiting Factors: None.

Mode: 7080.

Description: All instructions that use central storage are handled with reference to the previous setting of the starting point counter. The counter may be positioned within any bank by the SPC instruction. Subsequent storage instruction addresses without ASU coding will automatically specify as an accumulator the bank of central storage indicated by this setting of the counter. Storage instructions with ASU coding will specify (a) bank 1, if the starting point counter is set to any position within bank 0 or 1; (b) bank 3, if the counter is set to any position within bank 2 or 3.

The SPC instruction does not affect the setting of the zero indicators. These indicators may be properly set by following SPC with a SHR 00000 instruction.

Data Transmission Operations

Various methods are used to move data in the 7080 from memory to memory, from memory to the storage units, and from storage units to memory. Data to be transmitted from one storage unit to another, however, must pass through memory. The transmission may affect an entire record in one operation or may specify particular fields, groups of fields, or individual characters.

Two or more records can be combined within the machine, either with or without calculation, to form any desired arrangement of output information for punching in cards, printing on report forms, or writing on tape. Conversely, single records can be split to form several records in any arrangement and transcribed by one or more of the output units. Any or all of the various input-output devices may be used during a single procedure to handle the record forms: cards, tape, or printed reports.

Load Storage (8 — LOD)

Function: This operation moves alphabetic or numerical information from memory to ACC or ASU storage.

Address: The address specifies the location of the right-hand character of the field in memory and the storage unit to be used.

Limiting Factors: Storage mark in the designated storage unit.

Mode: All.

Description: The load instruction permits single characters, series of characters, or fields to be entered into accumulator or auxiliary storage from memory. The number of characters or length of the field loaded into storage is determined by the position of the storage mark. The load instruction is usually preceded by a set left instruction to adjust storage to the size of the field to be loaded.

The address part of the instruction specifies the location of the right-hand character of the field in memory and the storage unit to be used. Characters are loaded from right to left from memory until the specified storage space is filled.

The accumulator or auxiliary storage sign is always set to plus by a load instruction. The field, character, or series of characters in memory are not affected by load storage.

EXAMPLES, LOAD

	STORAGE BEFORE		STORAGE AFTER	
MEMORY	STORAGE	SIGN	STORAGE	SIGN
ABCbb12345	a7310	+	a2345	+
ABCbbb12345	a12345678901	−	aABCbbb12345	+
ABCbbb12345	a00	+	a45	+
ABCbbb12345	a00000012	+	abbb12345	+

Unload Storage (7 — UNL)

Function: Numerical or alphabetic information in ACC or ASU is placed in memory.

Address: The address specifies the memory position (right-hand) where the field from storage is to be placed and the storage unit to be used.

Limiting Factors: Storage mark in the designated storage unit.

Mode: All.

Description: The unload instruction is used to place the contents of accumulator or auxiliary storage in memory. The length of the field unloaded into memory is equal to the number of positions in the storage unit.

The right-hand character of the designated storage unit is unloaded into the memory position specified by the address part of the instruction. Remaining characters in storage are entered successively into memory from right to left until a storage mark is sensed.

The accumulator or auxiliary storage sign has no effect upon the data placed in memory. The contents of accumulator or auxiliary storage are not affected by unload storage.

EXAMPLES, UNLOAD

STORAGE	SIGN	MEMORY BEFORE	MEMORY AFTER
a3748	−	B0229	B3748
a450	+	1576	1450
aAB12	+	134CD	1AB12
ab$bb	+	0000	b$bb

Load Four Characters (, — LFC 02)

Function: This operation provides a method of moving characters, usually a four-character instruction operand, from memory into central storage without requir-

ing a storage mark to the left of the storage field.

Address: The address specifies the location of the units position of the field in memory. The address must end in 4 or 9 when loading four characters. One, two, three, or five characters may also be loaded by ending the address in 1 or 6, 2 or 7, 3 or 8, or 0 or 5, respectively.

Limiting Factors: Characters are loaded from right to left up to and including the first character whose address ends in 1 or 6.

Mode: 7080.

Description: The storage field to be loaded is specified by setting of the starting point counter. Characters are loaded, starting with the addressed character, from right to left up to and including the first character whose address ends in 1 or 6.

Storage positions, other than those into which characters are loaded, are not altered. Information is placed in central storage exactly as it appears in memory, except when any of the characters is the specific bit code CBA 842, which is assumed to represent a storage mark in memory. This character is called "less than" and has < as a graphic. This character is converted to a storage mark.

The accumulator or auxiliary storage sign and zero indicators are not altered by this instruction. The field in memory is also not affected.

Unload Four Characters (, – UFC 03)

Function: This operation provides a method of moving characters, usually a four-character instruction operand, from central storage into memory without the requirement of a storage mark to the left of the storage.

Address: The address specifies the location of the units position of the field in memory. The address must end in 4 or 9 when unloading four characters. One, two, three, or five characters may also be unloaded by ending the address in 1 or 6, 2 or 7, 3 or 8, or 0 or 5, respectively.

Limiting Factors: Characters are unloaded from right to left up to and including the first character whose address ends in 1 or 6.

Mode: 7080.

Description: The storage field to be unloaded is specified by the current value of the starting point counter. Characters are unloaded, starting with the addressed character, from right to left up to and including the first character whose address ends in 1 or 6. Storage marks, if encountered, are converted to a special character in memory (C, B, A, 8, 4 and 2 bits). This character is called "less than" and has < as a graphic.

The contents of storage are not altered by this instruction. The accumulator or auxiliary storage sign has no effect on the data placed in memory.

Load Storage Bank (,—LSB 04)

Function: The 256 characters in memory are loaded into a storage bank by this instruction.

Address: The address specifies the location of the units position of the 256-character field in memory.

Limiting Factors: None.

Mode: 7080.

Description: The bank to be loaded is specified by the current value of the starting point counter, usually set by a preceding SPC instruction. Loading begins at position 000 of the storage bank indicated, regardless of the position of the starting point counter within the bank. Information is placed in storage exactly as it appears in memory, except when any of the characters is the specific bit code CBA 842, which is assumed to represent a storage mark in memory. This character is called "less than" and has < as a graphic. This character is converted to a storage mark.

The accumulator or auxiliary storage sign and zero indicators, the field in memory, and the setting of the starting point counter are not affected by this instruction.

Unload Storage Bank (,—USB 05)

Function: All 256 characters of a storage bank are placed in memory by this instruction.

Address: The address specifies the location of the units position of the 256-character field in memory.

Limiting Factors: None.

Mode: 7080.

Description: The bank to be unloaded is specified by the current value of the starting point counter, usually set by a preceding SPC instruction. Unloading begins at position 000 of the storage bank indicated, regardless of the position of the starting point counter within the bank.

Data is placed in memory exactly at is appears in storage. Storage marks, if encountered, are converted to a special character in memory (bit code CBA 842). This special character is called "less than" and has < as a graphic.

The contents of the storage bank and the setting of the starting point counter are not affected.

Load Address (# — LDA)

Function: This instruction moves a four-character instruction address from memory into central storage as:

A five-digit numerical field in the 705 III mode.

A six-digit numerical field in the 7080 mode.

Address: The address, which must end in a 4 or 9, specifies the right-hand position of the four-character field and the storage unit to be used.

Limiting Factors: None.

Mode: All.

Description: The load address instruction is used to move the address portion (four characters) of an instruction in memory into central storage as a five- or six-digit numerical field. In its completely numerical form, an instruction address is much easier to manipulate. To execute this instruction, the machine performs the following:

1. The numerical portion of the four addressed characters in memory is loaded directly into the four low-order digits in storage.
2. The A and B bits over the thousands position of the field in memory always represent the 1 and 2, respectively, in the 10,000's position. In the 7080 mode, the B and A bits over the units position represent the 4 and 8, respectively, in the 10,000's position. In the 705 III mode, the A bit (indirect addressing) over the units position (and the B bit if the console 40K switch is on) is ignored. The binary total, in decimal form, is stored into the fifth and sixth storage digits in the 7080 mode, or into the fifth digit (only) in the 705 III mode.
3. A storage mark is placed to the left of the high-order digit in storage, that is, in the sixth position in 705 III mode, and in the seventh position in 7080 mode.

Zoning over the tens and hundreds positions of the memory field is ignored.

A storage mark will be placed to the left of the high-order digit in storage. Therefore, the LDA instruction need not be preceded by a SET instruction.

EXAMPLES, 705 III MODE

MEMORY	STORAGE BEFORE	STORAGE AFTER
01 10 3 4 4 2	a	a53442
01 10 11 11 3 4 4 2	a	a53442
01 1 2 2 8	a6722481	a11228
11 01 4 8 7 7	a25	a34877
7 3 0 9	a	a07309
0 0 0 9	a	a00009

EXAMPLES, 7080 MODE

01 10 3 4 4 2	a	a053442
01 10 11 11 3 4 4 2	a	a133442
01 1 2 2 8	a6722481	a011228
11 01 4 8 7 7	a25	a114877
7 3 0 9	a	a007309
0 0 0 9	a	a000009

Unload Address (* — ULA)

Function: This instruction moves a five-digit (705 III mode) or a six-digit (7080 mode) numerical field in storage into memory as a four-character address field.

Address: The address, which must end in either 4 or 9, specifies the units position of the memory field and the storage unit to be used.

Limiting Factors: None.

Mode: All.

Description: The unload address instruction converts a five- or six-digit numerical storage field into a four-character address field in memory with the proper zoning. To execute this instruction, the machine performs the following:

1. The low-order four digits of the storage field are moved directly into the numerical portion of the four addressed characters in memory.
2. The decimal contents of the fifth and, in the 7080 mode, the sixth digit of the storage field are converted to binary representation and the resulting bits are loaded into the zone positions of the units and thousands characters of the memory field. The A and B bits over the thousands position always represent the 1 and 2, respectively, of the fifth storage digit. In the 7080 mode, the B and A bits over the units position represent the 4 and 8, respectively, of the binary representation of the fifth and sixth storage digit. In the 705 III mode, only the B bit over the units position is affected. In the 705 III mode with the 40K switch on, no zone bits are transferred to the units position.

In the 705 III mode, the value of the five-digit storage field should be less than 40,000 if the console 40K switch is on, and less than 80,000 if the switch is off. In the 7080 mode, the value of the six-digit storage field should be less than 160,000.

If the address in either case is over the limit, the address stored in memory is always that which would

be obtained by wrap-around at the limit. See examples 6 and 8.

If the storage field contains zones, they are ignored. Zones over the tens and hundreds positions of the memory field are not affected in either mode of operation. Therefore, the portion of a memory address specifying ASU's is not changed by the ULA instruction. In the 705 III mode, the A bit of the units position of the memory field (indicating an indirect address) is not affected by the ULA instruction.

If the field in storage is less than five digits (705 III mode) or less than six digits (7080 mode), it is treated as having zeros to the left of significant digits. If the field in storage is greater than five or six digits, only the numerical portions of the low-order five or six are recognized, depending upon the mode of operation.

EXAMPLES, UNLOAD ADDRESS (705 III MODE)

STORAGE	MEMORY BEFORE	MEMORY AFTER
a 5 3 4 4 2	10 5 6 4 7	01 10 3 4 4 2
a 0 0 0 2 4	11 11 11 11 11 0 0 1 4	0 0 2 4
a 7 5 5 5 5	01 01 2 2 2 2	10 01 11 10 5 5 5 5
a 2 5	3 7 3 7	0 0 2 5
a 1 1 6 2 3 0 7	01 01 11 01 4 3 2 1	10 01 11 11 2 3 0 7
a 1 1 9 2 3 0 7	4 3 2 1	01 2 3 0 7

EXAMPLES, UNLOAD ADDRESS (7080 MODE)
(First four examples same as above)

a 1 1 6 2 3 0 7	01 01 11 01 4 3 2 1	01 11 2 3 0 7
a 1 1 9 2 3 0 7	4 3 2 1	11 2 3 0 7

Store for Print (5 — SPR)

Function: A numerical or alphabetic field in central storage is placed in memory with discriminative action by the instruction.

Address: The address specifies the memory position (right-hand) where the field from storage is to be placed and the storage unit to be used.

Limiting Factors: Storage mark in the designated storage unit.

Mode: All.

Description: The store-for-print instruction normally is used to transfer a numerical field from the storage to memory. However, this instruction can also be used to store alphabetic fields from accumulator or auxiliary storage to memory.

When the sign of the storage unit is plus, a blank is stored in the memory position specified by the address part of the instruction.

When the sign of the storage unit is minus, a dash is stored in the memory position specified by the address part of the instruction.

The numerical storage field is stored in the memory positions directly to the left of the sign position. The storage mark determines the left limit of the field to be stored.

When periods or commas are encountered in memory, these memory positions are skipped and the digits are stored in successively lower address positions. the characters b & — are stored as $\overset{+}{0}$ $\overset{-}{0}$, respectively.

After the storage field has been placed in memory, the memory field is inspected from left to right, to the first significant character. Insignificant characters with zero numerical parts and insignificant commas are replaced with blanks. Zeros to the right of the decimal point are not replaced.

The field in storage remains unchanged by this operation.

EXAMPLES, STORE FOR PRINT

STORAGE	SIGN	MEMORY BEFORE	MEMORY AFTER
a007638	+	$ 21,135.146	$ 2bbb76.38b
a0071834	—	bb,bbb.bbb	bbb718.34—
a00000000	+	bbb,bbb.bbb	bbbbbbb.00b
a0473829	—	bb,bbb.bbb	b4,738.29—
aABCDE	+	bb.bbbb	AB.CDEb
a04612	+	bb.bbbb	b4.612b
aABCbD	+	bb.bbbb	AB.C‡Db

The SPR instruction is commonly used to place numerical data from storage into special memory areas for printing. These memory areas normally contain a prescribed number of positions, as well as predetermined periods and commas, for report printing. Under these circumstances, this instruction should be used with fields of known length. For example, to store in a ten-position (plus punctuation) memory field, the storage unit should contain ten digits. If it contains less, the resulting memory field may include remaining high-order digits from a previous field.

Receive (U—RCV)

Function: This operation sets MAC II to the address part of the instruction.

Address: The address designates the memory loca-

tion that is to be referenced by a subsequent TZB, TSL, TMT, SND, TCT, RWW, or BLM instruction.

Limiting Factors: None.

Mode: All.

Description: The receive instruction is used to designate the memory location that is to be referenced by a subsequent TZB, TSL, TMT, SND, RWW, or BLM instruction.

When blocks of five characters are to be processed by a subsequent instruction (TMT 00, BLM 00, or SND), the address part specifies the memory location of the low-order character of the block of data. The receive address must always end in 4 or 9 (9 only when used for a TCT).

When individual characters or fields are to be processed one character at a time (TMT 01 or BLM 01), the address specifies the memory location of the first character which is to receive data. The address may specify any memory location.

The address may also specify any memory location when the subsequent instruction is to be a TZB. If the subsequent instruction is a TSL, however, the address must have a units digit of 1 or 6.

Any ASU coding (01-15) is interpreted as 00. The mnemonic code RCVS (RCV 01) is used to distinguish receive instructions that are used with the TMT 01 instruction from those used with the TMT 00 and SND instructions.

Send (/ − SND)

Function: Data is transmitted, in blocks of five characters at a time, from a memory location specified by the address part of the instruction to a memory location specified by the address part of a previous RCV instruction.

Address: The address specifies the location in memory from which the record is to be transmitted, and the storage unit to be used. The addressed memory position must be one with a units digit of 4 or 9 and represents the location of the low-order character of the first block of characters to be transmitted.

Limiting Factors: Storage mark in the designated storage unit.

Mode: All.

Description: The send instruction causes a high-speed movement of data, in groups of five characters, from one location in memory to another, from left to right. The address part of the instruction specifies the initial location in memory from which the record is to be moved. The SND must be preceded by a receive (RCV) instruction to set MAC II at the address of the receiving location. Both the RCV and SND instructions must designate memory locations with addresses ending in either 4 or 9. This address is the low-order character of the record or block of data to be sent.

The SND instruction must also be preceded at some time by an instruction setting the storage unit at a length to control properly the amount of information that is to be moved. This preset storage unit is then designated by the send instruction (ACC or ASU coding) and five characters are sent for each position to the right of the storage mark; for example, an ASU set at four places causes four groups of five characters (20 characters) to be moved; an ASU set at 20 causes 20 groups of five characters (100) to be moved. The contents of the designated storage unit are unaffected by the execution of the SND instruction.

If a SND instruction is used without a previous RCV instruction, the operation takes place using whatever memory address is indicated by MAC II for the receiving area of memory.

If the SND instruction is preceded by a RWW instruction, the SND instruction is not executed and a check memory operation is performed. The RWW-SND sequence of instructions performs a high-speed validity check (groups of five characters) on the contents of memory, starting at the address specified by the SND instruction and continuing to the end of the 20,000 character memory block being used. Any invalid characters detected in the memory block cause the 00901 check indicator to be turned on, but do not cause a stop regardless of the setting of the 00901 switch. If the 7080 is used with 754 tape control, attached tape units should not be in a select status when the SND instruction is used in this manner.

This operation is useful to determine whether an error in memory is the cause of persistent channel check error indications during a WR instruction. Also, it can be used to check the validity of memory before taking a check point.

Transmit 00 (9—TMT)

Function: Data is transmitted, in blocks of five characters at a time, from a memory location specified by the address part of the instruction to a memory location specified by the address part of a previous RCV instruction.

Address: The address specifies the location in mem-

ory from which the record is to be transmitted. The addressed memory position must be one with a units digit of 4 or 9 and represents the location of the low-order character of the first block of characters to be transmitted.

Limiting Factors: A record mark in a memory location with a units digit of 4 or 9.

Mode: All.

Description: The transmit instruction specifies the location in memory from which a record is to be transmitted to the receiving area.

Blocks of five characters are transmitted, with the address part specifying the memory location of the fifth character. This address part must have a units digit of 4 or 9.

Transmission is limited by the record mark, which would normally be the last character of the record block. The address of this limiting mark must also have a units digit of 4 or 9. The total number of characters transmitted, including the record mark, must be evenly divisible by five. A record mark in other positions of memory is transmitted like any other character and does not limit the transmission.

The address of the transmit instruction is placed in the memory address counter I (MAC I). This counter, as well as MAC II (which holds the receiving address), advances five positions after each block of five characters has been transmitted. The original record in memory is not affected by the transmit instruction.

If a TMT instruction is used without a previous RCV instruction, the operation takes place using whatever memory address is indicated by MAC II for the receiving area of memory.

Transmit 01-15 (9—TMTS)

Function: Data is transmitted, one character at a time, from a memory location specified by the address part of the instruction to a memory location specified by the address part of a previous RCV instruction.

Address: The address specifies the location in memory from which transmission is to begin.

Limiting Factors: Storage mark in the ASU indicated by the ASU coding of the address part of the instruction.

Mode: All.

Description: Individual characters are transmitted one character at a time, with the address part of the instruction specifying the memory location of the first character to be transmitted. The address may specify any memory location. The transmit instruction must be preceded by a RCV instruction to designate the receiving location.

The storage mark in the selected ASU limits the number of characters transmitted. During transmission, the storage unit is checked for a storage mark beginning at the right-hand position. This check is made for each character transmitted until the storage mark is sensed. Sensing the storage mark stops the operation.

Any auxiliary storage unit may be used. The storage mark is usually adjusted by a set left instruction or properly positioned as a result of calculation. The transmit instruction must be preceded by a receive instruction to designate the receiving location.

The address of the transmit instruction is placed in memory address counter I (MAC I). This counter, as well as MAC II (which holds the receiving address), advances one position after each character has been transmitted. The original record in memory and the field in storage are not affected by the transmit operation.

If a TMT instruction is used without a previous RCV instruction, the operation takes place using whatever memory address is indicated by MAC II for the receiving area of memory.

Ten Character Transmit (, — TCT 08)

Function: Data is moved, in blocks of ten characters, from a memory location specified by the address part of the instruction, to another memory location specified by the address part of a previous receive (RCV) instruction.

Address: The address specifies the memory location from which the record is to be transmitted. The addressed memory position must have a units position of 9 and represent the low-order character of the first ten-character block to be transmitted. The previous RCV address must also have an address with a units position of 9.

Limiting Factors: A record mark in the memory location with a units position of 9.

Mode: 7080.

Description: Blocks of ten characters are transmitted with the address part of the instruction specifying the memory location of the tenth character. The address part must have a units digit of 9.

Transmission is limited by the record mark, which normally is the last character of the record block. The address of this limiting mark must have a units digit of 9. The total number of characters to be transmitted, including the record mark, must be evenly divisible

by 10. A record mark in any location other than 9 will be transmitted just like any other character and will not terminate the operation. At the completion of the operation, MAC I and MAC II will be ten positions higher than the last-used address in the transmission.

If the machine check 00901 switch is set to automatic and a data register VRC occurs, the operation terminates after the block in error is transmitted; MAC I and MAC II will be ten higher than the last processed block (the block containing the error). MBR will contain the character in error only if the memory unit position is 5 through 9; otherwise, it will be necessary to refer to the data register to determine which character is in error.

An instruction check (00900) results if:

1. TCT is given when not in the 7080 mode.
2. TCT address does not end in 9.

Blank Memory 00 ($ — BLM)

Function: This operation places blank characters, five at a time, in memory.

Address: The numerical value of the address indicates the number of five-character groups to be used for blanking.

Limiting Factors: Blanking occurs for as many five-character groups as indicated by the numerical value of the address, modulo 20,000.

Mode: All.

Description: The number of five-character groups that are blanked is indicated by the numerical value of the instruction address of the BLM instruction. A preceding RCV instruction specifies the address of the five-character group where blanking will begin. Blanking proceeds from left to right in memory. With high-speed mode, blanking always begins in a memory address units position of 0 or 5, meaning that the RCV instruction address must refer to an address ending in 4 or 9, respectively. Example:

```
RCV          44004
BLM 00       00015
```

These instructions cause the high-speed erasing or blanking of 15 groups of five characters (total of 75 characters), beginning with the character at location 44000 and ending, therefore, in location 44074.

If a BLM instruction is used without a previous RCV instruction, the operation takes place using whatever memory address is indicated by MAC II for the blanking area of memory.

To blank all 160,000 positions of memory, two BLM instructions must be given (for example, BLM 19,999 and BLM 12,001).

Blank Memory 01 ($ — BLMS)

Function: This operation places blank characters, one at a time, in memory.

Address: The numerical value of the address indicates the number of single characters to be blanked.

Limiting Factors: Blanking occurs for as many characters as indicated by the numerical value of the address part of the instruction, up to 20,000 characters.

Mode: All.

Description: The number of individual characters that is to be blanked is indicated by the numerical value of the instruction address. A preceding RCV instruction specifies the address of the character where the blanking will begin. This may be any address in memory. Blanking proceeds from left to right. Example:

```
RCV          44002
BLM 01       00015
```

These instructions cause the slow-speed erasing or blanking of a total of 15 characters, starting with location 44002 and ending in location 44016.

If a BLM instruction is used without a previous RCV instruction, the operation takes place using whatever memory address is indicated by MAC II for the blanking area of memory.

Decision Operations

The decision operations make it possible for the stored program to control its course of action by modifying the sequence in which any instruction or block of instructions is executed.

The results of interrogating or "looking at" a designated indicator, switch, or some other condition within the machine can be used to direct the program to one of several alternate program routines. This branch or subroutine is made up of instructions to calculate, rearrange the record, select specific input-output units, check results, perform end-of-file routines, and so on.

Compare (4 — CMP)

Function: This operation compares the contents of accumulator or auxiliary storage with a field in memory.

Address: The address specifies the units position of the memory field and the storage units to be used.

Limiting Factors: Storage mark in the storage field to be compared.

Mode: All.

Description: The compare instruction compares a field in central storage with the portion of memory specified by the address part of the instruction. The particular storage unit to be used is also specified by the address.

The comparison begins between the specified character in memory and the right-hand character of the designated storage field. It proceeds from right to left, character by character, between storage and memory until a storage mark is sensed. The results of the comparison are determined in the usual way; that is, the most significant characters are those on the left. The number of characters compared is equal to the number of positions in the storage field.

All characters that can appear in memory may be compared. Although this is rarely done, all of the special characters, including the record mark and group mark, can be compared. The ascending sequence of characters is as follows: blank . ¤ < ǂ & $ * / , % # @ 0̊ A through I 0̄ J through R ǂ S through Z 0 through 9

The symbol < is called "less than" and represents the storage mark in memory (C, B, A, 8, 4, and 2 bits).

The result of a comparison can be "interrogated" or tested by two special transfer instructions, transfer on high and transfer on equal. When the storage field is higher than the field in memory, a following transfer-on-high instruction transfers to the location of the program step specified by the address of the transfer instruction. When the two fields are equal, a transfer-on-equal instruction accomplishes the same result. If neither of these conditions exists, the storage field is lower than the field in memory. In this way, supplementary routines may be programmed to handle the results of comparisons.

Any number of tests may be made between comparisons. The result of a comparison is not changed until another comparison is made.

Either the results of calculation or data loaded into storage may be compared against a portion of memory. However, a calculated result appears in storage without a sign indication over the right-hand digit while a numerical field in memory usually appears with a signed right-hand digit. A comparison between such fields would be unequal because of the sign.

The 00901 check indicator is turned on when the compare indicators are incorrectly set after the execution of the compare instruction. See "Compare Check."

EXAMPLES, COMPARE

		CONSOLE INDICATORS	
STORAGE	MEMORY	HIGH	LOW
a1234̊	$1234̊		
a1234	$1234̊	on	
a1234̊	$2345̊		on
aTYPEb705	TYPEb704	on	
aSMITHbbb	WARFIELD		on
aSMITHbbb	SMITHbbb		

Enable Compare Backward (3-ECB 12)

Function: This instruction permits comparing fields, generated by a backward read operation, whose characters are in a reverse sequence.

Address: The address for this operation is ignored.

Limiting Factors: None.

Mode: 705 III, 7080.

Description: This instruction must precede the compare instruction to perform a compare operation on fields read into memory by a backward read operation.

Characters are read into memory position in the same sequence as they appear on tape. Therefore, during a backward read operation, information is read into memory in the opposite direction as compared with a normal read operation. For example, the record JOHN DOE 56789 would be read into memory as 98765 EOD NHOJ.

In order to compare this information properly, the field in storage must be reversed also. This can be done by program manipulation of the original record or by using the previous reversed record, as in sequence checking.

Since the fields to be compared are in reverse sequence, the enable backward compare operation must condition the normal compare operation to give the desired results. Conditioning is accomplished by controlling the termination of the compare operation; that is, by the setting of the first compare indicator (high or low). If the fields are equal, the compare operation is terminated in the normal manner: the sensing of the storage mark, in the storage field being compared, terminates the operation.

An interrupt cannot occur immediately following the ECB instruction; it is delayed until the execution of a subsequent CMP instruction is completed.

Transfer on High (K—TRH)

Function: This operation interrogates the high comparison indicator and effects a transfer if on.

Address: The address indicates the instruction location to which the machine transfers if the high comparison trigger is on.

Limiting Factors: None.

Mode: All.

Description: The transfer-on-high instruction interrogates the high comparison indicator. When the indicator is on, the machine transfers to the instruction specified by the address part of the transfer-on-high instruction. If the high indicator is not on, a transfer is not made and the machine proceeds to the next sequential instruction.

The instruction can be used during any program step after a comparison. The instruction can be used any number of times between comparisons without turning the indicator off. The indicator is turned off on the next compare instruction.

Transfer on Equal (L—TRE)

Function: This operation causes a transfer if an equal condition exists from a comparison of a memory and storage field.

Address: The address indicates the instruction location to which the machine transfers if an equal condition exists.

Limiting Factors: None.

Mode: All.

Description: The transfer-on-equal operation effects a transfer if an equal condition exists from a comparison of a memory and storage field. With an equal condition, the machine transfers to the instruction specified by the address part of the transfer-on-equal instruction.

If an equal condition is not indicated, a transfer is not made and the machine proceeds to the next instruction.

The instruction can be used during any program step following a comparison. The instruction can be used any number of times between comparisons without removing the indication.

Normalize and Transfer (X—NTR)

Function: This operation interrogates the left-hand character of a storage field. If the numerical part of the character is zero, the character is removed and a transfer is effected.

Address: The address specifies the instruction location to which the machine transfers if a zero is removed and specifies the storage unit to be used.

Limiting Factors: None.

Mode: All.

Description: The normalize-and-transfer instruction removes the left-hand character of the storage field if the numerical part of that character is a zero.

A transfer is made to the location specified by the address part of the instruction when a zero is deleted. If the numerical part of the left-hand character is not a zero, the storage field is not changed, a transfer is not made, and the machine proceeds to the next instruction.

When the storage field consists of a single zero character, the zero is not deleted and a transfer is not made.

The normalize-and-transfer instruction is useful in removing zeros, one at a time, from the left end of a factor in accumulator and auxiliary storage. A program routine may then be inserted to count the number of zeros removed, a necessary function in floating decimal or floating dollar sign operations.

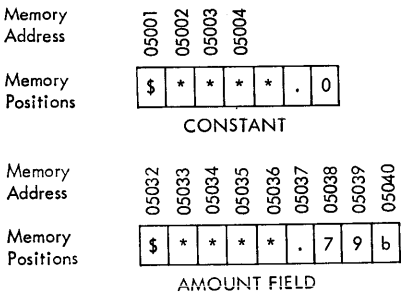


Figure 28. Normalize and Transfer

PROGRAM, NORMALIZE AND TRANSFER

Figure 28 illustrates the problem of printing asterisks in place of insignificant zeros in an amount field. Assume the following:

A six-position amount field in ACC 00 is to be stored for printing at memory address 05040. The dollar sign, asterisks to replace the insignificant zeros to the left of the decimal point, and the decimal point are to be placed in memory for proper printing of the

amount. Constant factors include a dollar sign, asterisks, a decimal point, and the memory address where they are to be placed.

Figure 29 is the program for normalize and transfer.

INSTR. LOCATION	INSTRUCTION OPER.	INSTRUCTION ADDRESS	STOR. CODE	ACCUMULATOR 00	SIGN	AUXILIARY STORAGE 01-15	SIGN
00004	SET	00007	07			a xxxxxxx	+
00009	LOD	05007	07			a$****.0	+
	Main Program						
00014	SEL						
	RD						
00099							
	Prepare for Printing						
00104	UNL	05038	07				
00109	NTR	00109	00	a00079	+		
00114	SPR	05040	00	a79	+		
00119	Write Record						
00124							
00144	TR	00014					

Figure 29. Program, Normalize and Transfer

HOUSEKEEPING

00004 and 00009. Load the print pattern into ASU 07.

MAIN PROGRAM

00014 to 00099. Read in records and calculate.

PREPARE FOR PRINTING

00104. Reset the print area.

00109. Remove the insignificant zeros to the left of the decimal point from the amount field in ACC 00.

00114. Store amount for printing.

PRINT RECORDS AND TRANSFER TO MAIN PROGRAM

00119 to 00144. Write record and repeat process.

Transfer on Zero (N—TRZ)

Function: This operation interrogates the accumulator or the auxiliary unit zero indicator and causes a transfer if the interrogated indicator is on.

Address: The address ASU coding indicates which zero indicator is to be interrogated and the instruction location to which the machine will transfer if the interrogated zero indicator is on.

Limiting Factors: None.

Mode: All.

Description: The transfer-on-zero instruction causes a program transfer when the accumulator zero indicator or the auxiliary storage unit zero indicator is on. The address part (ASU coding) of the instruction specifies which of the two zero indicators is to be interrogated and the memory location of the next instruction if a transfer is made.

The accumulator or auxiliary storage unit zero indicator is turned on when the contents of the storage last used, by an instruction that is capable of modifying storage, consist of characters having zero numerical portions. The corresponding indicator is set regardless of the bank of storage in which the starting point counter is located. Characters with zero numerical portions are zero, plus or minus signed zero, and the record mark.

Exceptions to the above conditions under which the zero indicators are set are the instructions LFC, LSB, and SPC, which have no effect on the setting of the zero indicators.

Transfer on Plus (M—TRP)

Function: This operation interrogates the accumulator or auxiliary storage unit sign and causes a transfer if the interrogated sign is plus.

Address: The address indicates which sign is to be interrogated and the instruction location to which the machine will transfer if the interrogated sign is plus.

Limiting Factors: None.

Mode: All.

Description: The transfer-on-plus instruction causes a program transfer when the sign of accumulator storage or the sign of the auxiliary storage units is plus. The address part of the instruction specifies the memory location of the next instruction to be executed after the transfer. The address must also specify either accumulator storage (00) or any of the auxiliary storage units (01-15).

When a storage field consists of characters having zero numerical portions, the sign is set to plus. Therefore, if a distinction is to be made between zero and plus, the transfer on zero must precede the transfer on plus.

NOTE: As a result of an incompleted division operation, the accumulator contents may be zero with the minus sign of the dividend. See "Divide."

Transfer (1—TR)

Function: This operation is used to transfer unconditionally to the next instruction to be executed.

Address: The address indicates the instruction location to which the machine transfers.

Limiting Factors: None.

Mode: All.

Description: The transfer instruction is used to change the sequence in which instructions of a program are executed. The address part of the instruction specifies the memory address of the right-hand digit of the next instruction to be executed. The instruction referred to by the address can be located at any point within the program. ASU coding 00-15 used with this instruction in the 705 I-II mode does not modify the operation. See the instruction transfer 01 in relation to the 705 III and 7080 modes.

Transfer 01 (1—TSL)

Function: The memory address of the next sequential instruction is placed in memory at an address indicated by MAC II and a transfer is made to a memory position as indicated by the address part of the instruction.

Address: The address indicates the instruction location to which the machine transfers.

Limiting Factors: None.

Mode: 705 III, 7080.

Description: A transfer instruction coded for ASU 01 will be interpreted as "transfer and store location" (TSL). When this instruction is executed, the five-digit instruction location address of the instruction counter is stepped by 5, converted to a four-digit memory address and placed into consecutive memory locations starting at the location specified by MAC II. The TSL instruction then effects a transfer to the location specified by the address part of the instruction.

For the TSL instruction to be executed properly, MAC II must indicate a memory address ending in 1 or 6. (See the instruction "receive" for the setting of MAC II.) ASU coding other than 01 is interpreted as a transfer (1—TR) instruction.

With this instruction, a subroutine may be called into the program without making any changes in the subroutine instructions. Only two instructions are required in the main program, the receive and TSL (transfer and store location) instructions.

Assume that an error correction subroutine is located in memory locations 08004 to 08114, with a transfer instruction at 08114. As the result of a test routine, the main program requires the correction subroutine. The following steps would take place:

00994. Test instruction. Transfer to 01004.
00999. TR 01014
01004. RCV 08111
01009. TSL 08004
01014. Proceed.
08004. First instruction. Continue to 08114.
08114. TR 01014

00994: As a result of the test routine, the program transfers to 01004.

01004: The RCV instruction places its address into MAC II. *This address must always end in a 1 or a 6 when used with a* TSL.

01009: During execution of the TSL instruction, the instruction counter (IC) is automatically increased by 5, making it 01014. The contents of the IC (01014) are then stored, in address form, at the memory location of MAC II (08111.) The TSL instruction then transfers to the memory location specified by its address (08004).

08004: This is the first instruction of the subroutine. The rest of the routine is executed normally and, when 08114 is reached, this transfer instruction now has an address which is the re-entry point to the main program.

Transfer Any (1—TRA)

Function: This operation interrogates the transfer-any indicator and causes a transfer if the indicator is on.

Address: The address indicates the instruction location to which the machine transfers if the interrogated transfer-any indicator is on.

Limiting Factors: None.

Mode: All.

Description: The transfer-any indicator is turned on whenever a 900-905 check indicator (excepting conditions discussed under "Any Indicator" on page 22), or an input-output indicator (other than that of a device on a communication channel) is turned on. When the indicator is on, a transfer is made to the memory location specified by the address part of the instruction. The transfer-any indicator is turned off by the transfer itself.

The TRA instruction used in the 705 I-II mode may have ACC or ASU coding. When used with the 705 III or 7080 modes, 00 coding must be used.

Transfer Any 01 (I — TAA)
02 (I — TAB)
03 (I — TAC)
04 (I — TAD)
05 (I — TAE)
06 (I — TAF)
07 (I — TNS)

Function: Each of these operations interrogates a specific alteration switch (00911-00916) or the non-stop switch and causes a transfer if the switch is on.

Address: The address indicates the instruction location to which the machine transfers if the interrogated switch is on.

Limiting Factors: None.

Mode: 705 III, 7080.

Description: The TRA instruction with ASU codes 01 through 07 makes possible the selection and interrogation of an alteration switch with only one instruction. The program transfers according to the setting of the various alteration switches as follows:

ASU CODE	ALTERATION SWITCH	MNEMONIC
01	00911	TAA
02	00912	TAB
03	00913	TAC
04	00914	TAD
05	00915	TAE
06	00916	TAF
07	Non-Stop	TNS

If an interrogated switch is off or ASU coding 08 through 15 is used, a NOP occurs. The transfer is not made and the machine proceeds to the next sequential instruction.

This instruction does not require the use of the select register; thus, it retains the previous selection whatever it may have been. For example, the following sequence of instructions can be given:

```
SEL    00201        Select a tape unit.
TAB    - - - - (02) Transfer on 00912.
TRS    - - - -      Transfer on signal.
```

Transfer on Signal 00 (O—TRS)

Function: This operation interrogates the previously selected input-output indicator, alteration switch, or check indicator (00900-00905) and causes a transfer if the selected indicator is on.

Address: The address indicates the memory address to which the machine transfers if the selected indicator is on.

Limiting Factors: None.

Mode: All.

Description: When the previously selected input-output indicator, alteration switch, or check indicator is on, execution of the TRS instruction transfers the machine to the instruction location specified by the address part of the instruction. In the case of a check indicator, the indicator is also automatically turned off.

Transfer on Signal 01 (O—TRR)

Function: This operation interrogates the ready indicator of the previously selected 777 tape record coordinator, 754 tape control, or communication channel. A transfer is made if the interrogated ready indicator is on.

Address: The address indicates the instruction location address to which the machine transfers if the interrogated ready indicator is on.

Limiting Factors: None.

Mode: All.

Description: When the ready indicator of the previously selected 754, 777, or communication channel is on, execution of the TRR instruction transfers the machine to the instruction location specified by the address part of the instruction. The TRR does not reset the channel indicators. The ready indicator of the 754 or the 777 is on if the selected tape unit has its ready light on. A communication channel must be idle, in addition to the above condition of the selected tape unit. When the selected ready indicator is off, a transfer is not made and the machine proceeds to the next sequential instruction.

In the 705 I-II mode, any ASU coding performs this operation, but the 705 III and 7080 modes must have 01 coding.

Transfer on Signal 02 (O—TTC)

Function: This operation interrogates the previously selected channel check indicator, which is on whenever any error occurs in the transmission of data over its corresponding channel. There are separate indicators for each channel. A transfer is made if the indicator is on.

Address: The address indicates the instruction loca-

tion in memory to which the machine will transfer if the selected channel check indicator is on.

Limiting Factors: None.

Mode: 705 III and 7080.

Description: When the channel check indicator is on for a previously selected channel, the TTC instruction transfers the machine to the instruction location in memory specified by the address part of the instruction. The TTC does not reset the channel indicators. If the channel check indicator is not on, the transfer is not made and the machine proceeds to the next sequential instruction. If the TTC instruction is given in the 705 I-II mode, the TTC instruction will be treated as a TRR instruction.

NOTE: The TTC instruction is for use with channels only.

Transfer on Signal 03 (O—TSA)

Function: This operation interrogates the channel check indicator of the selected channel and the I-O indicator of the selected tape unit. A transfer is made if either or both of these indicators are on; the ready indicator must be on before the execution of a TSA can be completed.

Address: The address indicates the instruction location address to which the machine transfers if either indicator is on.

Limiting Factors: None.

Mode: 705 III and 7080.

Description: The ready indicator of the selected channel must be on before a TSA can be executed. The communication channel must be ready and idle to be considered in the ready status.

If the ready indicator is off, the machine will hang up until it comes on. *Interrupt cannot be processed during this waiting time and will be delayed until the instruction execution is complete.* For this reason, if there is any uncertainty as to the readiness of the selected unit, the programmer should normally precede the TSA with TRR-TR waiting loop. When the ready indicator is on, the TSA will interrogate:

1. The channel check indicator of the selected channel.
2. The input-output indicator of the selected tape drive on the selected channel.

A transfer is made if either or both of these indicators is on. The TSA does not reset the channel indicators. In the case of the 7908, a transfer is made if either the channel check or the attention indicator is on.

NOTE: The TSA instruction is for use with channels only and performs a function similar to that of the TRA used for serial I-O.

Transfer on Signal 09 (O—TAR)

Function: This operation interrogates the automatic restart indicator and causes a transfer when the indicator is on.

Address: The address specifies the instruction location to which the machine transfers if the automatic restart indicator is on.

Limiting Factors: None.

Mode: 7080.

Description: The automatic restart indicator is turned on whenever the 7080 does not complete execution of an instruction within approximately two seconds. (A hang-up because of a no-response will cause this.) An exception is read or write instructions that are transmitting data to a device not on a channel. When the TAR instruction is executed, the indicator is automatically turned off and the machine transfers to the location specified by the address of the instruction. When the indicator is off, a TAR instruction has no effect and the machine continues to the next sequential instruction.

The transfer on signal 09 operates as a TAR instruction only in the 7080 mode. In the 705 III mode, the instruction is considered no operation, and in the 705 I-II mode it is considered a TRR.

Transfer on Signal 10 (O—TIC)
11 (O—TMC)
12 (O—TRC)
13 (O—TEC)
14 (O—TOC)
15 (O—TSC)

Function: Each of these operations interrogates a specific check indicator (00900-00905) and causes a transfer if the interrogated indicator is on.

Address: The address indicates the instruction location to which the machine transfers if the interrogated indicator is on.

Limiting Factors: None.

Mode: 705 III and 7080.

Description: The check indicators that are inter-

rogated by these operations are:

ASU		MNEMONIC	INDICATORS
10	(TIC)	Transfer Instruction Check	Instruction Check (00900)
11	(TMC)	Transfer Machine Check	Machine Check (00901)
12	(TRC)	Transfer Read-Write Check	Read-Write Check (00902)
13	(TEC)	Transfer Echo Check	Record Check (00903)
14	(TOC)	Transfer Overflow Check	Overflow Check (00904)
15	(TSC)	Transfer Sign Check	Sign Check (00905)

When the TRS 10-15 operations are used, the interrogated indicator, if on, will be turned off and a transfer made. If the interrogated indicator is off, a transfer is not made and the machine proceeds to the next sequential instruction.

These operations do not require selection of the check indicator, as does the TRS 00 instruction. These check indicators may be interrogated without the need of remembering, through programming, what had been previously selected. The TRS 10-15 instructions operate in this manner only in the 705 III and 7080 modes. In the 705 I-II mode, they are considered TRR instructions.

Set Bit 01-06 (% — SBZ)
07 (% — SBA)
08 (% — SBR)
09-14 (% — SBN)

Function: This operation changes any bit in an addressed character to the 0 or 1 state or reverses the status of the A bit or C bit.

Address: The address indicates the character location. The ASU coding identifies the particular bit and the type of operation.

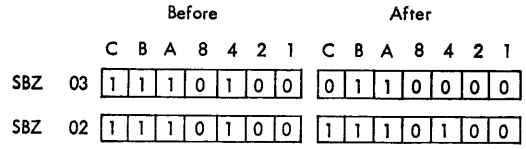
Limiting Factors: None.

Mode: All.

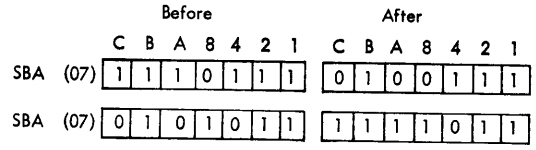
Description: The set-bit zero (SBZ) operation sets any bit position of an addressed character (except C bit) to a zero bit status. ASU zoning for the various bits of the character are as follows:

	ASU	ZONING
	01	Set 1 bit to 0
	02	Set 2 bit to 0
SBZ	03	Set 4 bit to 0
	04	Set 8 bit to 0
	05	Set A-bit to 0
	06	Set B-bit to 0

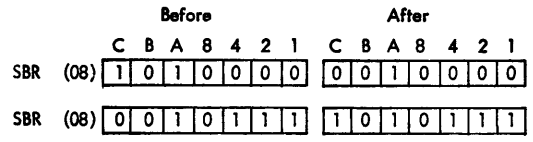
If the addressed character bit position is already in a zero bit status, no change is effected. The C bit of the character will be automatically corrected for consistency with the character code. For example:



The set-bit-alternate (SBA) operation reverses the bit status in the A bit position of the addressed character. The ASU coding used for this operation is 07. The C bit is automatically adjusted for consistency with the character code. For example:



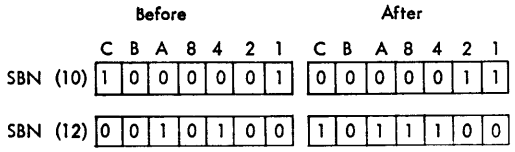
The set-bit-redundant (SBR) operation reverses the bit status in the C bit position of the addressed character. The ASU coding used for this operation is 08. The C bit is not adjusted for consistency with the character code. This instruction may be used to develop an invalid character in memory. For example:



Set bit to one (SBN) sets any bit position of an addressed character (except C bit) to a 1 bit status. ASU zoning for the various bits of the character are as follows:

	09	Set 1 bit to 1
	10	Set 2 bit to 1
SBN	11	Set 4 bit to 1
	12	Set 8 bit to 1
	13	Set A bit to 1
	14	Set B bit to 1

If the addressed character bit position is already in a 1 bit status, no change is made. The C bit of the character is automatically corrected for consistency with the character code. For example:



When using the set bit instruction in setting up code characters or a number of variables, there are three things to consider:

1. If six separate variables are to be recorded in a single character, there must not be the possibility of their all being zero at the same time. This would result in placing a storage mark in memory. The storage mark is an invalid character in memory. If this possibility exists, only five bits of the character may be used for the recording of variables and the sixth is set permanently to 1.

2. If the code character is to be written out of memory by means of the WR 00 instruction, there must not be the possibility of all the bits being at 1, since this would constitute a group mark and would terminate a WR 00 instruction. To prevent this, the programmer could use the WR 01 instruction, or plan to use only four bits for the recording of variables, with the fifth set permanently at 1 (to insure against all 0's) and the sixth set permanently at 0 (to insure against all 1's.).

3. If the code character is to be written out onto a printer, the programmer must insure that the combination of bits does not constitute some character that is not printable. To satisfy the above three considerations, programming convention establishes the B bit permanently at 1 and the 8 bit permanently at 0. Thus, the possibility of generating a storage mark, group mark or an unprintable character is removed.

Transfer on Zero Bit 01-07 (. — TZB)

Function: This operation interrogates any bit position of an addressed character and causes a transfer if the interrogated bit is zero.

Address: The address indicates the instruction location to which the machine transfers if a transfer is made. The ASU coding of the instruction indicates the specific bit of the character to be tested. The memory address of the character to be interrogated is determined by a RCV instruction which must precede the TZB.

Limiting Factors: None.

Mode: All.

Description: This instruction is preceded by a receive instruction which sets MAC II at the address of the subject character in memory. The address portion of the TZB instruction indicates where the program should transfer if the bit tested is a 0. The ASU zoning of the instruction indicates the specific bit of the character that is to be tested; thus:

BIT	ASU ZONING
1	01
2	02
4	03
8	04
A	05
B	06
C	07

ACC coding and ASU codes other than 01-07 are ignored and a NOP occurs.

If the bit tested is 0, the program will transfer; if the bit is 1, the program will proceed to the next instruction. Therefore, to test the A bit of the character in location 34660 of memory, the programming would be:

```
10004 RCV 34660
10009 TZB 20004 (05)
10014 - - -
```

If the A bit of character 34660 is 0, the program transfers to location 20004 for its next instruction. If the A bit is 1, the program proceeds to 10014 for its next instruction.

During the execution of the TZB instruction, the character designated by MAC II (the RCV instruction) is placed in MBR where the bit indicated by the ASU zoning is interrogated. MAC II remains set until a TMT, RWW or another RCV instruction is given.

By testing a bit individually, it is possible to determine the sign of any value stored in memory without first moving it to the ACC or ASU, as follows:

```
RCV --          Units position of field in question.
TZB --- (05)    Transfer if field is minus.
    --- --      No transfer if field is plus.
```

The TZB need only look at the A bit, because the B bit must always be a 1 if the field is always signed.

If the A bit is 0, the field is minus; if it is 1, the field is plus.

If it is necessary to determine which, if any, zone bits a character has, it can be done in the following manner:

```
00104  RCV ---          Character in question
00109  TZB --- (06)     00124
00114  TZB --- (05)     Zone 10
00119  TR  --- --       Zone 11
00124  TZB --- (05)     Zone 00
       --- --- --       Zone 01
```

To reverse a bit from one state to another, regard-

less of its previous state (as might be done to alternate between two numbers or addresses), the following routine could be used.

```
00104  RCV          01004  Designate character.
00109  TZB  (01)    00204  Transfer if the bit is 0.
00114  SB   (01)    01004  If bit is not 0, set it to 0.
00119  TR           00304  Continue with program.
00204  SB   (09)    01004  If bit is 0, set it to 1.
00304  ---          ----   Continue with program.
```

No Operation (A—NOP)

Function: This operation causes the machine to proceed to the next instruction in the program.

Address: The address can be any address and has no effect. But, when using a NOP as a constant, if an A bit is present in the units position (indirect address, 705 III mode), the numeric portion of the units position must be 4 or 9.

Limiting Factors: None.

Mode: All.

Description: The NOP instruction provides a means of interspersing constant data throughout the program. When the address portion is used as a constant, care must be taken; if the units position has an A bit, the numeric portion must be a 4 or 9. The numeric portion of the units position must be a 4 or 9 if the instruction is used as a NOP-TR switch. This is a programming technique whereby the NOP operation code (A) is changed to TR (1), or TR to NOP, by program steps that modify the zoning of that position. Thus, as a result of a particular decision in the program, an instruction may be changed from TR to NOP or NOP to TR in order to vary the sequence of a portion of the program.

Status and Mode Operations

This section explains those instructions which change the status of the machine or the mode in which it is operating. The TIP, LIP, EIA, CNO, and HLT operations can modify the status of the machine. The EEM, LEM, EIM, and LIM all modify the mode of operation. EEM and LEM instructions have control operation codes. However, they are discussed here and not with the rest of the control operations which have to do with I-O devices or channels.

Transfer to Interrupt Program (, — TIP 14)

Function: This operation simulates an automatic interruption. When executed, the present machine status is stored in CASU 15, and an unconditional transfer is made to an interrupt program.

Address: The address specifies the instruction location to which the machine transfers.

Limiting Factors: None.

Mode: 7080.

Description: This instruction causes the following steps to occur in sequence:

1. The contents of the instruction counter are stored in the first four positions of word 0, channel auxiliary storage unit 15. The status of indicators is stored as bits in the remaining four positions of word 0, CASU 15.

2. The contents of MAC II, the starting point counter, and the select register are stored in CASU 15 as shown in Figure 15.

3. The interrupt program indicator is turned on to prevent automatic interrupts.

4. The starting point counter is set to 2000. Thus, subsequent operations in the interrupt program that designate the accumulator automatically refer to storage bank 2, position 000; those with ASU coding refer to channel auxiliary storage units in storage bank 3.

5. The instruction counter is reset to the address of the TIP instruction.

6. The contents of MAC II and the select register remain unaltered.

The above sequence also takes place when an automatic interrupt occurs, except that the memory location of the interrupt program is obtained from positions 0-3 of word 0 in the appropriate channel word set or from the interrupt word. The address thus obtained is placed in the instruction counter. The status indicators, as stored in positions 4-7, are restored to the state that existed after the last previously executed instruction in the interrupt program. A transfer is automatically made to the interrupt program.

The machine need not be in the interrupt mode in order to execute this instruction, which will also function if the machine is already in an interrupt program. Great care must be taken if TIP is used within an interrupt program. The contents of CASU 15 must be preserved if the main program is to be re-entered. Also, on leaving the higher level interrupt program, some provision must be made to protect the original interrupt program from automatic interrupts.

A programming example illustrating the use of interrupts, and various instructions concerned with interrupt, is shown in the appendix.

Leave Interrupt Program (,—LIP 15)

Function: This operation terminates the interrupt program and returns the machine to the main program defined by the machine status stored in CASU 15.

Limiting Factors: None.

Address: The address normally specifies the storage location into which the contents of the instruction counter and status indicators are to be placed before the transfer to the main program is made. The storage address takes the following form:

THOUSANDS POSITION: This specifies the storage bank. Usually the digit 2 is used and specifies storage bank 2 in which the channel word sets or interrupt words are located.

HUNDREDS POSITION: This specifies the group of four words within the bank. The digits 0-3 specify one of the four channel word sets. The digit 5 refers to the interrupt words.

TENS POSITION: The digits 0-3 specify the proper eight-character word in a group of four. Normally the digit 0 is used when working with channel word sets.

UNITS POSITION: A zero is normally used which designates the first position of the storage word.

Mode: 7080.

Description: This instruction causes the following steps to occur in sequence:

1. The contents of the instruction counter and the status indicators are placed in the storage word specified by the address of the LIP instruction. This word is usually word 0 of the communication channel which originally initiated the interrupt, and for which a future interrupt is anticipated.

2. The contents of CASU 15 are read and the entire machine status of the main program is restored, including status indicators, MAC II, the starting point counter, and the select register. The instruction counter is set to the location of the next instruction in the main program, as previously stored in the first four positions of word 0 in CASU 15.

3. The interrupt program indicator is turned off to permit further interrupts.

Subsequent operations automatically refer to the accumulator or to auxiliary storage units in the bank specified by the restored value of the starting point counter.

Conventional procedure requires the interrupt program status to be placed in word 0 of a channel word set. However, the programmer can retain a fixed interrupt address and status by using the LIP instruction with the special address 00009. When this address is used, the contents of the instruction counter and the status triggers are not placed in storage.

The machine need not be in the interrupt mode in order to execute this instruction.

Figure 30 is a program schematic showing the use of the TIP and LIP instructions. A transfer from the main program to an input-output interrupt program is executed by the TIP instruction. A channel and a tape unit are selected. A read instruction is given to start the tape record reading into memory. While the record is reading, a LIP instruction transfers back to the main program to continue processing. As processing continues, the tape reading operation is completed, causing an automatic interrupt of the main program. When the current instruction in the main program is executed, a transfer to the next instruction in the interrupt program is made. At this point, the reading operation may be checked, a programmed record count may be incremented, or other manipulation of the record may occur. The next input-output operation for the channel is usually initiated. A LIP instruction is given to re-enter the main program.

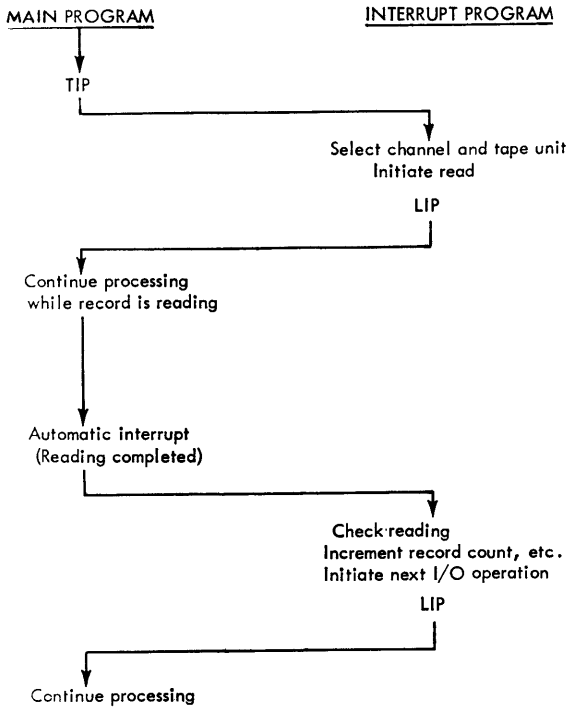


Figure 30. Program Schematic for LIP and TIP Instructions

A programming example illustrating the use of interrupts, and various instructions concerned with interrupt, is shown in the appendix.

Enter Interrupt Mode (,—EIM 06)

Function: This operation places the machine into the interrupt mode. The program may then be interrupted by any of the channels or the console interrupt key.

Address: The memory address can be any address and has no effect.

Limiting Factors: None.

Mode: 7080.

Description: Although the machine must be in the 7080 mode in order to execute EIM, as is the case for all comma operations, the interrupt is not terminated if the program should return to a 705 mode. After the EIM instruction is executed, the program may be interrupted at the end of the execution of any instruction. The following are exceptions. In these cases interrupts are delayed.

1. The machine may not be interrupted during execution of an interrupt program. That is, interrupts may not occur between any automatic interrupt or execution of a transfer to interrupt program (TIP) instruction and the following leave interrupt program (LIP) instruction.

2. An interrupt may not occur between an enable indirect address (EIA) instruction and the following instruction.

3. An interrupt may not occur between a read while write (RWW) instruction and the following read, write, or send instruction.

4. An interrupt may not occur between an enable compare backward (ECB) instruction and the following compare (CMP) instruction.

If the machine has not been in interrupt mode, but interrupt triggers are on, the associated interrupts will occur as soon as the EIM instruction is executed.

Leave Interrupt Mode (,—LIM 07)

Function: This operation terminates the interrupt mode. No further interrupts to the program can occur.

Address: The memory address can be any address and has no effect.

Limiting Factors: None.

Mode: 7080.

Description: Execution of the LIM instruction disables the interrupt feature of the 7080. Channels must then be serviced by interrogating the readiness, as in the 705 III system. All interrupting conditions which may have occurred prior to the execution of LIM are reset. All interrupt conditions which occur subsequent to the execution of LIM will not be processed unless and until an EIM instruction is executed.

Enter Eighty Mode (3—EEM 14)

Function: This operation places the machine in 7080 mode. All instructions restricted to 7080 mode are operative as well as all of the 705 I, II, and III instructions. The A bit over the units position of instruction addresses signifies the upper 80,000 positions of memory instead of indirect addressing as in 705 III mode.

Address: The memory address can be any address and has no effect.

Limiting Factors: None.

Mode: All.

Description: This operation terminates the 705 I-II or the 705 III mode and places the machine into the 7080 mode. The nature of the 7080 mode of operation is as follows:

1. All the features of the 705 systems are available to the program, together with additional features of the 7080.

2. All comma operation codes are operable, as well as the transfer to automatic restart (TAR) instructions.

3. The A bit in the units position of the instruction address specifies the memory locations 80,000 to 159,-999, not indirect addressing.

4. The address modification instructions (LDA, ULA, AAM,) automatically handle the six-digit addresses of the 160,000 position memory.

5. The size of memory available to the program is 160,000 positions for the 7302 Model 1 and 80,000 positions for the 7302 Model 2, regardless of setting of the console memory size switch. Wrap-around of MAC I, MAC II and the IC will always be at 160,000.

The memory address part of this instruction can be any address and has no effect.

This instruction and LEM have the same operation code (3) as the control operations IOF, RWD, etc.; the distinction is made via ASU coding.

Leave Eighty Mode (3—LEM 15)

Function: This instruction terminates the 7080 mode and places the machine in 705 I-II, or 705 III mode as indicated by console switch settings. All 7080 mode instructions are deactivated and the A bit over the units position of instruction addresses is treated as indirect addressing 705 III or ignored.

Address: The memory address can be any address and has no effect.

Limiting Factors: None.

Mode: All.

Description: This operation terminates the 7080 mode and places the machine into the 705 I-II or 705 III mode, depending on the current setting of the console 705 I-II compatibility switch.

When the LEM instruction is executed with the console 705 I-II compatibility switch off, the machine enters the 705 III mode. All subsequent program instructions are executed in the same manner as in the 705 III, and input-output operation is identical.

If the LEM instruction is executed with the 705 I compatibility switch on, the machine will subsequently operate as a 705 I-II.

The next instruction following the LEM is considered to be located in a memory with capacity limited by the setting of the 40K memory size switch. For example, with the console switches set for a 705 III with 40,000 positions of memory, the instruction following LEM executed in location 150,004 is automatically taken from location 30,009. For this reason the LEM instruction should be located in a section of memory that will be available in the following mode of operation.

The memory address portion of this instruction can be any address and has no effect.

This instruction and EEM have the same operation code (3) as the control operations IOF, RWD, etc.; the distinction is made via the ASU coding.

Enable Indirect Address (,—EIA 10)

Function: This operation conditions the machine to treat the instruction address of the following instruction as an indirect address.

Address: The memory address can be any address and has no effect.

Limiting Factors: None.

Mode: 7080.

Description: When the machine is operating in the 7080 mode, the indirect addressing of an instruction is accomplished by preceding it with an EIA instruction. This indirect address state applies only to the instruction immediately following EIA. When the system is in the 705 III mode, indirect addressing is designated by a 1 in the A bit position of the units character of the instruction address. This bit is used in the 7080 mode to address directly the memory positions 80,000 through 159,999.

An interrupt may not occur immediately following the EIA instruction, but is delayed until the execution of the instruction following the EIA has been completed.

No Operation (,—CNO 11)

Function: This instruction (comma no operation) causes the machine to proceed to the next instruction in the program. It may be used in the same manner as the NOP instruction available in all modes.

Address: The memory address can be any address and has no effect.

Limiting Factors: None.

Mode: 7080.

Description: Provision of the CNO instruction facilitates a convenient programming technique. The CNO and EIA instructions both have comma operation codes; ASU coding for CNO is 11; coding for EIA is 10. The difference in coding is represented by the A bit in the tens position of the address. A set bit alternate (SBA) instruction specifying the tens positions of the CNO address will convert this instruction to EIA. Conversely an SBA instruction specifying the tens position of the EIA address will convert this instruction to CNO. Thus, the address of the following instruction can be readily switched to and from direct and indirect.

Stop (J—HLT)

Function: Execution of this instruction either stops the CPU operation or results in an automatic interrupt. An interrupt occurs if the console non-stop switch is on and the machine is not executing an interrupt program. In all other cases the machine will stop.

Address: The address can be any address and has no effect.

Where several halts are programmed, the addresses may serve as identification; for instance, HLT 9999 may be "end of job."

Limiting Factors: None.

Mode: All.

Description: On the 705 I-II and the 705 III, the primary use of the HLT instruction is at various points in a program where operator intervention is required. An error in reading or writing, an end-of-file condition, or other situations may be programmed to stop or halt operation. The address part of the stop instruction can be read from the console when a stop occurs. This address may be coded to indicate to the operator why the machine operation has been stopped and what corrective measures should be taken.

With the 7080, however, it may be desirable to stay in automatic status at all times in order that interrupts can be processed. The non-stop feature of the 7080 facilitates this type of operation. When the machine is run with the console non-stop switch on, execution of an HLT instruction (other than in an interrupt program) results in an interrupt to interrupt word 250. A

subroutine may then be executed, which will type out explanatory information to the operator and proceed to a programmed waiting loop out of the interrupt program. The machine, while essentially stopped, is still in automatic status and thus able to process interrupts. The operator, by depression of a console interrupt key, may then initiate a program to read corrective routines from the 7502 console card reader.

In operating the 7080 with the console non-stop switch on, it may be, in certain instances, impossible for the machine to continue in automatic status. An HLT instruction in the interrupt program may then be executed to stop operation.

When the execution of an HLT instruction results in a machine stop, depression of the start key on the 7153 console causes the machine to read and execute the next instruction.

Control Operations

The control instructions initiate various operating features of the 7080 and its related input-output units. Control instructions associated with the 760 control and storage and the 777 tape record coordinator are discussed in the manuals related to those machines. Function, address, and limiting factors are the same for all control instructions.

After any one of the control instructions, write tape mark, backspace, backspace-file or skip, is initiated on a channel, the program proceeds to the next sequential instruction and at the completion of the operation an automatic interrupt will occur if the machine is in the interrupt mode.

After the control instruction rewind, or rewind-and-unload, is initiated, the program proceeds to the next sequential instruction, but the completion of the operation must be determined by the readiness of the channel.

Function: These operations control various features of the 7080 and its related input-output units.

Address: The address and the ASU coding specify the feature to be controlled. The address of CHR can be any address; its control is the ASU coding.

Limiting Factors: Except for CHR, SDL and SDH, these instructions are not used on the 7908 channels.

NOTE: Although EEM and LEM have control (3) operation codes, they are discussed under "Status and Mode Operations."

Control 00000 (3—IOF)

Mode: All.

Description: The input-output indicator of the unit previously selected, if on, is turned off. This instruction refers to printers, tape units, drums, and card readers.

Control 00001 (3—WTM)

Mode: All.

Description: The tape mark is written on tape by the last selected unit. The writing of this special character is checked in the same way as the writing of characters from memory.

Control 00002 (3—RWD)

Mode: All.

Description: The tape on the last selected unit is rewound.

Control 00002 (3—RUN 01)

Mode: 705 III, 7080.

Description: The tape on the last selected unit is rewound. If this unit is a 729 connected to the system through a communication channel, it is also unloaded.

Control 00003 (3—ION)

Mode: All.

Description: The input-output indicator on the tape unit last selected, if off, is turned on. The instruction may be used for tape units only.

Control 00004 (3—BSP)

Mode: All.

Description: Tape on the unit last selected is backspaced to the previous inter-record gap. Backspacing tape at load point turns on the tape indicator.

Control 00004 (3—BSF 01)

Mode: All.

Description: The tape on the unit last selected is backspaced until a tape mark or load point is reached. The tape indicator is not turned on when a tape mark is read, unless the load point is reached. This instruction cannot be under record counter control.

When executing a BSP 01, the 7621 recognizes a tape mark only as a single character record, and not as the first character of a larger record. Since a tape mark sensed during a BSP 01 may differ slightly in appearance from one sensed during a read, the programmer should take extra precaution by following any BSP 01 instruction with an IOF, then FSP and check for end of file.

Control 00005 (3—SUP)

Mode: All.

Description: This instruction applies to printers and punches only. It prevents printing or punching of information from record storage for one cycle. The instruction is normally used to prevent printing or punching when a read-write error has occurred from memory to record storage. Under program control, the record storage can be reloaded from memory after an error condition has been recognized and the corrected record printed or punched.

Control 00009 (3—SKP)

Mode: All.

Description: The tape on the unit last selected, provided it is a 729 connected to the system through a communication channel, is skipped forward 3.6 inches. During the skip, the tape is erased as it passes over the read-write head.

This instruction is intended for use with the 729 tape unit with the two-gap head. If a write error persists, the tape may be backspaced once more and skipped over what can be presumed to be an imperfection in the tape itself.

Control 00037, Set Density Low (3—SDL 00)

Mode: 705 III, 7080.

Description: This instruction conditions the previously selected 729 II or IV tape unit to read or write all subsequent records at a density of 200 characters to the inch. Tape processing is carried out at the rate of 15,000 characters per second in the 729 II and 22,500 characters per second in the 729 IV. For 729 V or VI, see the "IBM 7621 Tape Control (Model 4)" section. If this instruction is used over the 7908 Data Channel, see the "Data Compression" section.

Control 00038, Set Density High (3—SDH 00)

Mode: 705 III, 7080.

Description: This instruction conditions the previously selected 729 II or IV tape unit to read or write all subsequent records at a density of 556 characters to the inch. Tape processing is then carried out at the rate of 41,667 characters per second in the 729 II and 62,500 characters per second in the 729 IV. For 729 V or VI, see the "IBM 7621 Tape Control (Model 4)" section. If this instruction is used over the 7908 Data Channel, see the "Data Compression" section.

Channel Reset (3—CHR 13)

Mode: All.

Description: This instruction resets all check and status indicators in the communication channels and all tape control units attached. No particular channel need be selected. The contents of the channel word set are not affected.

This instruction is useful as part of a housekeeping routine at the start of a job, and exactly duplicates the function of the channel reset key on the 7153 console.

The memory address portion of this instruction can be any address and has no effect.

NOTE: If a channel reset is given at a time when tape is moving, an immediate stop takes place, in the same manner as when the 7621 reset key is depressed.

Select (2—SEL)

Function: The various components and devices of the 7080 system are selected for use by this instruction.

Address: The address portion is the assigned number or address of the particular component to be used. See "Input-Output Component Addressing."

Limiting Factors: The maximum select address is 39,999.

Mode: All.

Description: The select instruction specifies one component (I-O device, channel, alteration switch or check indicator) of the 7080 system to which future action is to be directed. The address of the component is placed in the select register. Only one component or device can be selected at a time and the device remains selected until another select instruction is given. The instruction also selects the associated input-output indicator of the addressed I-O device, except in the case of the typewriter or card punch.

Read and Write Operations

This section explains those instructions used or involved in moving information from an input unit to memory and from memory to an output unit.

Specific details concerning the operation of 7080 input-output units (used in the 705 modes) are contained in the *705 Data Processing System Reference Manual,* A22-6506.

Read 00 (Y—RD)

Function: This operation reads a record from a selected input unit, *checks* it, and stores it in memory.

Address: The address specifies the memory position into which the first character of the input record is to be placed. When communication channels are used, the memory position must be one whose address has a units digit of either 0 or 5.

Limiting Factors: The operation is limited by indication from the input unit.

Mode: All.

Description: The read instruction with no ASU coding is used to enter information into memory from a previously selected input unit. Information starts at the addressed memory position and continues to successively higher positions until terminated by a proper end-of-record-indication.

The end-of-record indications for the input units are as follows:

1. Tape—Inter-record gap
2. Reader—Reader storage mark (RSM) or last position of the record storage unit (RSU)
3. Console card reader—RSM or end of card.
4. Drum—Drum mark
5. Devices attached through the 7908—End or unusual end signal from the attached control unit.

The inter-record gap, reader storage mark or drum mark are not entered into memory as part of the input record.

When a read instruction is given to any 705 I-II input-output device attached through the 7622 signal control or to the 7502 console card reader, the program waits until the transmission of data is complete before proceeding to the next instruction. Data enters memory serially, character by character. Any character code error detected during transmission turns on the 00902 read-write check indicator and the transfer-any indicator.

When reading is through communication channels, data is entered into memory in blocks of five characters, rather than character by character. If the last block of five characters from the input record is not completely filled, group marks are inserted in the unfilled positions. Any character code error detected during transmission turns on the channel check indicator of the appropriate channel.

After the read instruction on a channel is initiated, the program proceeds to the next sequential instruction. At the completion of the read operation, an automatic interrupt results if the machine is in the interrupt mode and the program is directed to the channel interrupt word (word 0, characters 0-3) to find the address of the next instruction to be performed. If the machine is not in the interrupt mode, the completion of the read operation must be determined by interrogating the readiness of the channel.

Should a channel RD 00 instruction be given where the size of the record will exceed the end of memory, the channel check indicator will be turned on and the RD 00 instruction will be converted to an RD 01 instruction; this group of five characters and all subsequent data in this record will be checked but not entered into memory.

If a channel address check occurs, the RD 00 instruction will be converted to an RD 01 instruction, and this group of five characters and all subsequent data in this record will be checked but not entered into memory.

In programming, note that the size of memory is dependent on the setting of console switches and the operating *mode* of the machine. The changing of modes during read or write operations may lead to erroneous results. For example, consider the machine to be in the 7080 mode and the console switches 705 I-II off and 40K off; assume also that the next instruction to be executed is read 79,900, and that a 150-character record is to be read from tape. Should a leave-7080-mode instruction be executed before the read operation is completed, the record would now be subject to the memory limitations of the 705 III (80K); thus, end of memory (MAC I = 0) would be at 79,999, a channel check would result, and the last 50 characters would not enter memory. It is the mode that prevails at the instant a boundary is crossed that determines which boundary applies. The memory boundaries are:

705 III-40K switch ON.....	39,995 and 159,995
705 III-40K switch OFF.....	79,995 and 159,995
7080	159,995

With a 7080 equipped with an 80K memory, the instruction address can range all the way to 160K (hence the above boundary restriction applies) but memory will execute all the instructions so as to fall within the boundaries of 0 to 80K.

If a read instruction is given to any tape unit attached to a 7621 Tape Control and the first character

of the record is a tape mark, the RD 00 instruction will be converted to a RD 01 instruction and the record will be checked but not entered into memory.

Read 01 (Y—FSP)

Function: A record is read from a selected input unit and checked but not entered into memory.

Address: Any memory address can be used, except when a selected unit is on a communication channel. In this case, the addressed memory position must be one having a units digit of 0 or 5.

Limiting Factors: The operation is limited by an indication from the input unit.

Mode: All.

Description: The read instruction with 01 coding (forward space) permits a record to be read from a previously selected input unit, and the data checked but not entered into memory. The operation is terminated by the proper end-of-record indication, as follows:

1. Tape—Inter-record gap
2. Reader—Reader storage mark (RSM) or last position of the record storage unit (RSU)
3. Console card reader—RSM or end of card
4. Drum—Drum mark
5. Devices attached through the 7908—End or unusual end signal from the attached control unit.

The instruction is normally used to space over unwanted tape records, but it is also used to check the validity of a previously written tape. The appropriate check indicator (00902 or channel check) is set if an error is detected.

After this instruction is initiated on a channel, the program proceeds to the next sequential instruction, but at the completion of the operation, an automatic interrupt will occur if the machine is in the interrupt mode.

If the machine is not in interrupt mode, completion of the operation must be determined by interrogating the readiness of the channel.

Read 02 (Y—RMA)

Function: The operation places the data memory address of the selected communication channel word set into memory.

Address: The address indicates the memory position into which the data memory address will be placed. The address must end in 0 or 5.

Limiting Factors: The operation should be used on channels 20-23 only.

Mode: 705 III, 7080.

Description: The read instruction with 02 coding (read memory address) places the contents of word 1, positions 0-4, of the selected communications channel word set into memory starting at the location specified by the address of the instruction. Since character 4 of the word set is unused and always contains a zero, the specified location will always contain a zero after execution of the RMA. The data memory address from the word set is placed in the next four higher positions in memory. Since communication channel instruction addresses must end in 0 or 5, both the address portion of the RMA instruction and the address read from the word set must end in 0 or 5.

At the end of a read operation involving a communication channel, the corresponding word set (word 1, positions 0-3) contains a data memory address. This address (ending in 0 or 5) is five positions higher than the location of the left-hand character of the last group of five characters read into memory. For example, assume that the last group is read into memory at locations 01005-01009. The data memory address in the word set is 01010.

At the end of a write operation involving a communication channel, the corresponding word set contains a data memory address that is *ten* positions higher than the location of the left-hand character of the last group written. This address also ends in 0 or 5. For example, assume that the last five characters written on tape are in memory at locations 01005-01009. The data memory address in the word set is 01015.

If two or more consecutive RD 02 instructions are directed against the same channel, the contents of data memory address will be valid and unchanged.

NOTE: Use of RMA with 7908 channels will give inconsistent results and may result in data being read into instruction areas.

Write 00 (R—WR 00)

Function: This operation transmits data from memory to a previously selected output unit.

Address: The address specifies the memory position from which writing is to begin. If a communication channel is used, the address must end in 0 or 5.

Limiting Factors: Group mark in memory.

Mode: All.

Description: The write 00 instruction transmits a record from memory to the selected card punch, printer, tape unit, drum, typewriter or output device connected through the 7908.

Information is written from memory, from left to right, starting at the memory position specified by the address part of the instruction and continuing until a group mark is reached. The write instruction does not affect the record in memory.

No write operation occurs if the write instruction is addressed to the memory address of a group mark. A no-operation occurs and the machine proceeds to the next instruction.

For serial I-O operations, sensing the group mark in memory stops the writing operation. The group mark causes an inter-record gap to be automatically placed on tape; if the drum is used, the group mark is converted to a drum mark at the end of the drum record.

When a write instruction is given to any 705 I-II input-output device attached through the 7622 signal control, or to the typewriter, the program waits until the transmission of data is complete before proceeding to the next instruction. Data leaves memory serially, character by character. Any character code error detected during transmission turns on the 00902 read-write check indicator and the transfer-any indicator.

When writing is through communication channels, data leaves memory in blocks of five characters, rather than character by character. Any character code error detected during transmission turns on the channel check indicator of the corresponding channel. The group mark is sensed in the channel to end the operation.

After the write instruction is initiated on a channel, the program proceeds to the next sequential instruction. At the completion of the write operation, an automatic interrupt results if the machine is in the interrupt mode and the program is directed to the channel interrupt word (word 0, characters 0-3) to find the address of the next instruction. If the machine is not in the interrupt mode, the completion of the write instruction must be determined by interrogating the readiness of the channel.

The size of memory is dependent upon the setting of the console switches (705 I-II, 40K) and the operating mode of the machine.

The changing of modes during write operations may lead to erroneous results. Should a write 79,900 instruction for a 200-character record be given in the 7080 mode and if a leave-7080-mode is executed before the twentieth 5-character block is written, the machine will wrap around at the 79,999 memory position; the channel check in the 7621 tape control will turn on and any further characters written in the record will be from the wrong memory locations. For a similar condition on the 7908, the channel check does not turn on.

Write 01 (R—DMP)

Function: This operation transmits the contents of memory from the specified address to the end of the memory block to a selected output unit.

Address: The address specifies the memory position from which writing is to begin. When communication channels are used, the address must end in 0 or 5.

Limiting Factors: The end of the memory block in which writing began. Exceptions are shown in the table below.

Mode: All.

Description: The write instruction with 01 coding (dump memory) transmits data to the selected card punch, printer, tape unit, drum, or typewriter. Writing begins at the addressed memory location and continues to successively higher positions to the end of the memory block, as follows:

MODE	40 K SW	WR 01 ADDRESS	LAST MEMORY POSITION WRITTEN
705 I-II	Off	0,000-19,998	19,998
		19,999	19,999
	On	0,000-19,999	19,998
		19,999-39,998	39,998
		-39,999	39,999
705 III (Channel I-O Operation) (WR 01 address must end in 0 or 5)			
	On	0,000-19,995	19,999
		20,000-39,995	39,999
	Off	0,000-19,995	19,999
		20,000-39,995	39,999
		40,000-59,995	59,999
		60,000-79,995	79,999
705 III (Serial I-O Operation)			
	On	Same as 705 I-II with 40 K Switch on	
	Off	0,000-19,998	19,998
		19,999-39,998	39,998
		39,999-59,998	59,998
		59,999-79,998	79,998
		-79,999	79,999
7080 (Channel Operation; WR 01 address must end in 0 or 5)			
	80 K	Same as 705 III	
	160 K	0,000-19,995	19,999
		20,000-39,995	39,999
		40,000-59,995	59,999
		60,000-79,995	79,999
		80,000-99,995	99,999
		100,000-119,995	119,999
		120,000-139,995	139,999
		140,000-159,995	159,999
7080 (Serial I-O Operation)			
	80 K	0,000-19,998	19,998
		19,999-39,998	39,998
		39,999-59,998	59,998
		59,999-79,998	79,998
		79,999	19,998
	160 K	79,999-99,998	99,998
		99,999-119,998	119,998
		119,999-139,998	139,998
		139,999-159,998	159,998
		159,999	19,998

The appropriate check indicator (00902 or channel check) is set if an error is detected during transmission.

After this instruction is initiated on a channel, the program proceeds to the next sequential instruction, but at the completion of the operation, an automatic interrupt will occur if the machine is in the interrupt mode.

NOTE: A no-bit character in a memory position will terminate the operation.

Write 02 (R—SRC)

Function: This operation sets the record counter of the selected communication channel word set (word 0, positions 1, 2, and 3) to the digits contained in the tens, hundreds and thousands positions of the address. The next RD (00-01), WR (00-01), WTM, SKP or BSP instruction is then under control of the record counter.

Address: The digits in the tens, hundreds, and thousands positions of the address should represent the number of operations to be under control of the record counter.

Limiting Factors: Capacity of the counter, up to 999. This instruction should be used on channels 20-23 only.

Mode: 705 III, 7080.

Description: A write instruction with 02 coding (set record counter) places the tens, hundreds, and thousands digits of the instruction address into a record counter located in word 0, positions 1, 2, and 3 of the previously selected channel word set. A record count (RC) indicator is turned on to put the next RD (00-01), WR (00-01), WTM, SKP, or BSP instruction under control of the RC. Each time the instruction following the WR 02 is executed, the contents of the RC are reduced by one. The reading, writing, or control operation is repeated until the contents of the RC are reduced to zero.

During reading or writing under RC control, the following conditions may occur:

1. An end of reel marker can be sensed during writing.
2. A tape mark can be sensed during reading.
3. An invalid character turns on the channel check indicator.

In the case of the end-of-reel marker or invalid character, the multiple write operation is first completed before stopping. The sensing of a tape mark on a read operation, however, causes an immediate stop.

The record counter indicator may be on at the start of a program. Housekeeping instructions to reset the indicator should be included in a program which uses the communication channels for this purpose. The indicator is reset by an RD 01 and RWD instruction.

The WR 02 instruction can be used on channels 20-23 only. If the instruction is given to a 7908 channel, it is treated as a WR 00 operation. If the instruction is given to a serial I-O device, a WR 01 operation results. This instruction should not be used when the machine is in the interrupt mode.

Read While Writing (S—RWW)

Function: This operation conditions a selected input tape unit to retain its selected status, prepares the selected tape unit to read, and sets MAC II to the address part of the instruction. The operation does not apply to operations involving a communication channel.

Address: The address specifies the memory position into which the first character of the input record is to be placed.

Limiting Factors: Group mark in memory for writing; inter-record gap on tape for reading.

Mode: 705 I-II.

Description: A record or group of records can be read into memory from tape (except communication channel) and at the same time another record or group of records may be written from memory on a selected output unit (except communication channel and drum). The operation is performed by the use of four instructions: SEL, RWW, SEL, and WR or WRE.

The RWW instruction conditions a selected *input* tape unit (only tape can be used as input) to retain its selected status. It prepares the tape unit to read, but reading is not actually accomplished until a subsequent WR or WRE instruction is given to a selected output unit.

MAC II is set to the address part of the RWW instruction and indicates the memory location into which input data is to be read. When reading is completed, the setting of MAC II is equal to the address of one memory position beyond the address of the final character read.

The address part of the subsequent WR or WRE instruction specifies the memory location from which output data is to be written. It is controlled by MAC I. The read-while-writing operation cannot be performed using overlapping areas in memory.

An interrupt cannot occur immediately following the RWW instruction; it is delayed until the execution of a subsequent RD, WR, or SND instruction is completed.

The SND instruction following a RWW results in a check memory operation. Refer to send instruction for a full explanation.

Write and Erase 00 (Z—WRE)

Function: This operation transmits data from memory to a previously selected output unit and replaces the written memory positions with blank characters. The operation cannot be used with the communication channels.

Address: The address specifies the memory position from which writing begins.

Limiting Factors: Group mark in memory.

Mode: All.

Description: The WRE instruction (write and erase) transmits a record from memory to a selected output unit (cannot use a communication channel) and replaces the written memory field with blank characters.

Information is written from memory, starting at the addressed memory position and continuing to successively higher memory positions until a group mark is sensed. The group mark will be replaced by a blank.

Sensing the group mark in memory stops the WRE operation. The group mark causes an inter-record gap to be automatically placed on tape; when drum is used, the group mark is converted to a drum mark at the end of the drum record.

No operation occurs if the instruction is addressed to a memory address of a group mark. The machine automatically proceeds to the next instruction.

The instruction is normally used for printing successive lines of different field arrangement or for group indication when detail printing. Fields may also be arranged on the tape for future printing and repetitive information can be eliminated in successive records.

Write and Erase 01 (Z—WRE)

Function: This operation transmits data from memory to a selected output unit, and replaces the written memory field with blank characters. (It cannot be used with communication channels.)

Address: The address specifies the memory position from which the writing is to begin.

Limiting Factors: The end of the memory block in which the writing began.

Mode: All.

Description: The WRE 01 instruction transmits data from memory to a selected output unit (not over a communication channel), and replaces the written memory field with blank characters.

Information is written from memory, starting at the addressed memory position and continuing to successively higher memory positions until the end of the memory block is reached. The last character written and erased is located in a memory position as shown in the chart for WR 01 operation. The last position of the memory block is not written or erased but causes the proper end-of-record indication (drum mark, inter-record gap) to be recorded. Group marks have no effect upon the execution of the instruction and are written out on the selected unit with all other characters.

To write and erase the last character of a memory block, a WRE 01 instruction addressed to the last character of the memory block must be used.

Any ASU coding (01-15) is interpreted as 01.

Diagnostic Instructions

Four additional instructions have been made available on the 7621 channels to assist the customer engineer in the performance of scheduled maintenance and in diagnosing error conditions. These instructions operate in 705 III and 7080 modes only.

Read 03—Sense Status Triggers (Y—SST)

Function: This operation gives the means of interrogating for the particular error condition causing a channel check.

Address: The address specifies the memory location into which the first of two sense characters will be placed. The address must end in 0 or 5.

Limiting Factors: Only two characters are read into memory.

Mode: 705 III, 7080.

Description: The read 03 instruction will interrogate the 7621 for all ten error conditions in any of the four selected channels. The status information is read into memory starting at the location specified by the instruction address. This information is in the form of two BCD characters, which represent the following error conditions:

BIT	CHAR 1	CHAR 2
1	RW REG VRC	SKEW CHK
2	REG A VRC	DWT CHK
4	ECHO CHECK	UNANS DEMAND
8	NO ERROR	NO ERROR
A	READ LRCR	CHANNEL ID
B	COMP CHK	MPX OVFL

The presence of a bit in one of the two characters indicates that the particular error trigger was on. A C bit generator is tied into this operation to assure getting an even bit parity character into memory. If there are no bits, representing no errors for that character, an 8 and a C bit will be routed to prevent a no-bit character from entering memory.

After the instruction is initiated, the program proceeds to the next sequential instruction. Completion of the operation must be determined by interrogating channel readiness.

The RD 03 instruction, unlike other RD instructions, does not reset the channel check indicator of the 7621 nor any other error indicators.

NOTE: The RD 03 instruction is also used with the 7908 channels but performs differently. A full description is given under "7908 Data Channel Instructions."

Write 03—Set Diagnostic Register (WR 03)

This instruction, when used with the 7621 channels, has no special mnemonic.

Function: This operation sets the diagnostic register with coded information to assist the customer engineer in performance of maintenance.

Address: The address specifies the location of the single character to be routed to the diagnostic register.

Limiting Factors: The TCU switch on the 7621 must be set to "Diagnostic."

Mode: 7080.

Description: A diagnostic register is included as part of each TCU. This register consists of six triggers that can be set to the write bus from the multiplexor. The setting of this register will take place during the WR 03 operation *when the* TCU *switch is set to diagnostic.* It will function the same as a standard write instruction except that the information, in this case a single character, will be routed to the diagnostic register instead of to tape. Ten characters will be read from memory into data words A and B, but only the first character will be sent to the TCU character register and then to the diagnostic register. *No group mark is* required following the character addressed by the WR 03.

The functions performed by the diagnostic register are:

B Bit	Read Register B (RR B). This control causes data to read only via skew register B into the R-W register.
A Bit	Read Register A (RR A). This control causes data to read only via skew register A into the R-W register.
8 Bit	Force LRC (LRC). This control prevents the character from being read.
4 Bit	Compare Check while Reading (COMP). This control causes compare checking to function on read as well as write.
2 Bit	Amplifier Bias (BIAS). This control prevents write clipping on writing and causes write clipping on reading.
1 Bit	Early Sample (SKEW). This control causes an early sample of the skew register A VRC.

After the instruction is initiated, the program proceeds to the next sequential instruction. Completion of the operation must be determined by interrogating channel readiness.

NOTE: The WR 03 instruction (with a special mnemonic) is also used with the 7908 channels but performs differently. A full description is given under "7908 Data Channel Instructions."

Select 06001 and 06002

Both of these are special select instructions which allow a check to be made on the WTC and the SAR 8 error detection circuitry in the MPX. Select 06001 will hold the WTC trigger in a reset condition. Select 06002 will hold the SAR 8 trigger in a reset condition. As a result of resetting and clamping either of these two triggers in a reset condition during a read or write operation by the appropriate select instruction, the corresponding WTC or SAR 8 error trigger will be turned on by the forced error. These select instructions continue in effect until another select instruction is given.

7908 Data Channel Instructions

The 7908 channels use the RD 00, RD 01, WR 00 and WR 01 instructions in essentially the same manner as the 7621 channels. Six additional instructions can be used over the channels of the 7908. These instructions are used to transfer status from control to core storage and to transfer orders from core storage to the control.

Status data consists of a number of four-bit bytes having specific bit assignment to indicator error, unusual, and attention conditions. A byte is a group of bits occupying one character position.

An order is control data transmitted as data from core storage to the control, where the order is decoded and executed to perform a specific function.

Read 03 — Sense Status Triggers (Y — SST)

Function: This instruction results in the transfer of status data from the control and for the selected channel to core storage. The read 03 instruction is normally a diagnostic instruction when used over channels 20-23. When used over a channel of the 7908, however, it performs the function here described.

Address: The address specifies the memory location into which the first character (byte) of the status data is to be placed. This address must end in 0 or 5.

Limiting Factors: None.

Mode: 705 III, 7080.

Description: This operation instructs the control to send the status data for the selected channel to the 7080 core storage location as specified by the address. The status data indicates error and unusual conditions as well as attention conditions. The status data consists of a number of four-bit bytes from a control (10 from 7631, 14 from 7640), and one from the 7908 data channel. The four-bit bytes are transmitted on the A, 4, 2, and 1 bit lines of the 7080; the bit that would normally be the 8 bit is transmitted on the A bit line. The sense instruction is terminated when all of the sense status data has been transmitted. The 7080 emits a B bit into all status data to prevent a no-bit character from appearing in memory. The 8 bit is always set to zero to prevent the status data from forming an unwanted group mark. (See "status data" under "7640 Hypertape Control".)

The initiating of a read, write, or control instruction resets all status bits to normal (the B bit on and the 8 bit off).

Write 03 — Set Control Condition (R — SCC)

Function: This instruction transmits an order from memory to the selected control. The write 03 instruction is normally a diagnostic instruction when used over channels 20-23, but whenever this instruction is used over a channel of the 7908 it performs the function here described.

Address: The address specifies the memory location from which the writing begins. The addressed memory position must have a units position of 0 or 5.

Limiting Factors:

1. An end signal from the control terminates the operation.
2. A group mark must follow the last character of the order.

Mode: 705 III, 7080.

Description: With a channel of the 7908 selected, the write instruction with an ASU coding 03 transmits an order from the specified memory location. The order is then interpreted by the control, and executed. The operation is terminated by an end signal from the control. A group mark must follow the last character of the order.

Read 04 — Control Read (Y — CRD)

Function: This instruction performs first a write 03 instruction and then a read 00 instruction.

Address: The address specifies the location from which the writing begins. This address must end in 0 or 5. The address indirectly defines the address location into which the first character of the input record is to be placed.

Limiting Factors:

1. A group mark indicates the end of the order field.
2. When reading over channels 44-47, the read record must be at least ten characters long.
3. The read field will begin in an address block 15 higher than the address block that contains the group mark. Example: if the group mark is in the address block 1000-1004, the read 00 address is 1015.
4. Normal termination of the operation results from an end signal emitted by the control.
5. A channel check, occurring at the completion of the write 03 portion of the operation, terminates the operation.

Mode: 705 III, 7080.

Description: This instruction first performs a write 03 instruction. At the termination of the write 03 portion of the instruction, it is converted to a read 00 instruction with an address that is 15 positions higher than the block containing the group mark. When reading over channels 44-47, the record must be at least ten characters long.

This operation is normally terminated by an end signal from the control at the completion of the read 00. However, a channel check occurring at the completion of the write 03 portion of the operation will terminate the operation.

Write 04 — Control Write (R — CWR)

Function: This instruction performs first a write 03 instruction and then a write 00 instruction.

Address: The address specifies the location from which the transmission of the order begins. The units position of the address must be 0 or 5. The address also indirectly defines the write 00 address.

Limiting Factors:

1. A group mark indicates the end of the order field.
2. The write field begins at the next address block. Example: if the group mark is in the address block 1000-1004, the write address will be 1005.
3. The second group mark in memory will terminate the write 00 and the operation.
4. A channel check occurring at the completion of the write 03 will terminate the operation.

Description: This instruction first performs a write 03. Sensing a group mark terminates the write 03 and converts the instruction to a write 00, with an address of the write field beginning at the next 0 or 5

address following the block that contains the group mark. Characters are written until the sensing of a group mark terminates the operation.

A channel check occurring at the completion of the write 03 portion will terminate the operation.

Read 05 — Read Memory Block (Y — RMB)

Function: This instruction reads a record from a selected device, into memory starting at the specified address, and continuing until either the end of the record or the end of the 20K memory block is reached.

Address: The address specifies the memory location in which the first character of the record will be placed. The address must end in 0 or 5.

Limiting Factors: (1) end of the record, or (2) end of 20K block, whichever occurs first.

Mode: 705 III, 7080.

Description: This instruction is identical to a normal read operation with the exception of the termination of the operation. Termination is dependent upon one of two conditions, whichever occurs first: (1) the normal end or the physical end of the record, and (2) the end of the 20K memory block in which the reading began (similar to a write 01 operation). For example: if the read address is 18780 and the end of the record is not sensed, termination of the operation takes place after a character has been read into memory location 19999.

Write 05 — Write Multiple Control (R — WMC)

Function: This instruction performs a series of write 03 operations.

Address: The address specifies the location from which the writing of the first order begins. The units position of the address must be 0 or 5.

Limiting Factors:

1. A group mark indicates the end of each intermediate order.
2. A record mark indicates the end of the series and normally terminates the operation.
3. A group mark must *not* follow the last order.
4. A channel check occurring at the completion of any of the orders in the series terminates the operation.

Mode: 705 III, 7080.

Description: This instruction performs a series of normal write 03 operations. The address must end in 0 or 5 and specify the location from which the writing of the first order begins. A group mark indicates the end of each order. The first character of the next order is located in the first 0 or 5 address higher than the address block containing the group mark of the previous order.

This instruction is normally terminated by a record mark which indicates the end of the last order. However, a channel check resulting from any one of the orders terminates the operation immediately.

IBM 7622 Signal Control

The IBM 7622 Signal Control (Figure 31) permits the attachment of vacuum tube-type I-O units to the 7080 system. To achieve program compatibility, the 7080 system provides for the attachment of I-O devices through the 7622 to allow 705 I and II programs to operate unaltered.

The 7622 provides for the attachment of the following tube type units:

IBM 757 Printer Control and IBM 717 Printer

IBM 759 Card Reader Control and IBM 714 Card Reader

IBM 758 Card Punch Control and IBM 722 Card Punch

IBM 754 Tape Control with as many as ten IBM 727 Tape Units

IBM 777 Tape Record Coordinator with as many as eight IBM 727 Tape Units (777 requires field modification)

IBM 760 Control and Storage and up to two IBM 727 Tape Units and IBM 720 Printer or IBM 730 Printer

IBM 744 Drum Power Supply and IBM 734 Drum

IBM 774 Tape Data Selector and IBM 407, 408, or 409 Accounting Machine or an IBM 519 Document-Originating Machine

The primary function of the 7622 is to convert transistor signal levels to tube levels for output devices, and to convert tube signal levels to transistor signal levels for input devices.

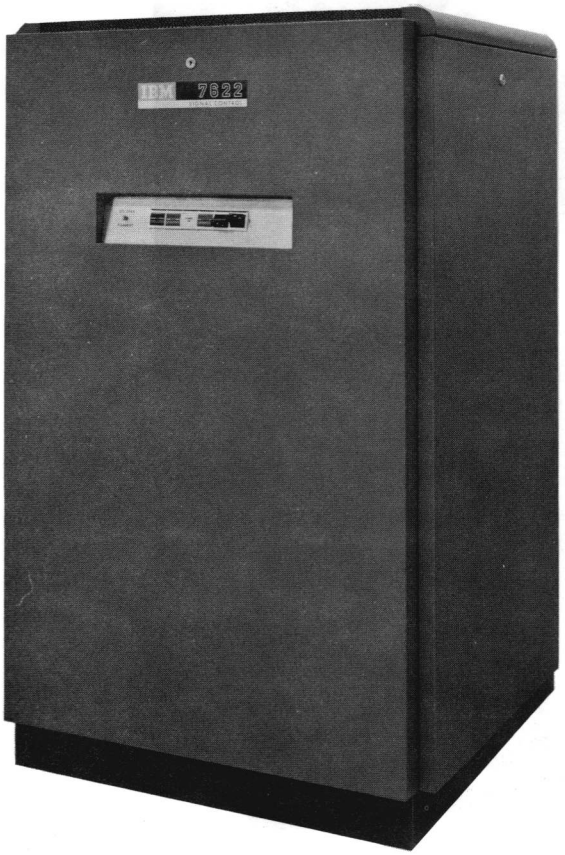


Figure 31. IBM 7622 Signal Control

IBM 7621 Tape Control

The IBM 7621 Tape Control (Figure 32), a two-channel control, provides power and serves to control the flow of data between the attached 729 tape units and the 7080. The 7621 is available in two models (both are two-channel controls):

Model 2: Attaches as many as twenty 729 II's or IV's, in any combination.

Model 4: Attaches as many as twenty 729 V's or VI's, in any combination. The primary difference between the two models consists of the mounting on the control panel of the model 4 control of two tape densities option switches, one switch for each channel. Each switch manually controls the operating densities of the tape units attached to the particular channel. Each switch is a three-position switch with settings of 200-556, 200-800, and 556-800 characters per inch. The high and low densities determined by the setting will prevail for all tape units attached to the particular channel.

The model 4 control unit can also be used with 729 II or IV tape units. Attempts to use these units at high density with the tape densities option switch at I (800/556) or II (800/200) will cause them to hang up.

IBM 729 Magnetic Tape Units

As many as ten IBM 729 II or IV Magnetic Tape Units may be connected through the IBM 7621 Tape Control to each communication channel of the 7080. Any combination of these two types of units can be used.

Except when stopping or starting, tape is driven at a

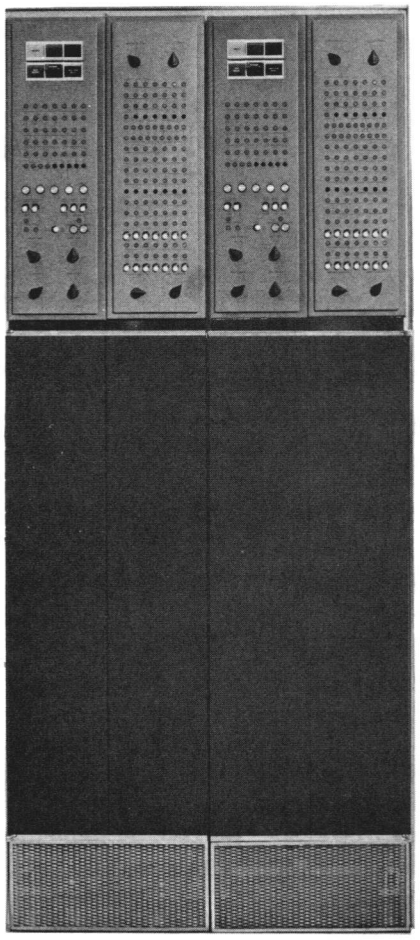


Figure 32. IBM 7621 Tape Control

constant speed of 75 inches per second on the 729 II and 112.5 inches per second on the 729 IV. Average starting and stopping time is 10.8 ms for the 729 II and 7.3 ms for the 729 IV.

Each tape unit is capable of reading or writing in either of two character density modes, low density and high density. Only the density and not the physical speed is variable. This results in two character speeds for each tape unit. For the 729 II, these speeds are 15,000 characters per second and 41,667 characters per second. These figures are arrived at by multiplying the physical speed of the tape (75 inches per second) by the character density (200 or 556 characters per inch).

The 729 IV tape unit, whose physical speed is 112.5 inches per second, has character speeds of 22,500 and 62,500 characters per second. The same character density of 200 or 556 is used.

Any tape prepared on the 729 II low density may be used on any 729 I or 727 tape unit. It may also be used with a 729 IV low density mode. Likewise, any tape prepared on the 729 IV low density may be used by a 727, 729 I or II low density. Any tape prepared by the 729 IV high density mode may be used only with another 729 II or IV high density mode tape unit or with a 729 III attached to a 705 system.

The high and low modes are under control of the program and the change-density switch (located on each tape unit).

The 729 II, IV, V, and VI are identical in appearance. Figure 33 is representative of all.

IBM 729 II and IV Magnetic Tape Units operate at a character density of 200 or 556 characters per inch. IBM 729 V and VI Magnetic Tape Units have an additional operating density of 800 characters per inch. Each tape unit is capable of reading or writing in either of two character density modes, low density or high density. In the case of the 729 V and VI, the high and low density values are determined by the manual setting of the tape densities option switch on the 7621, Model 4.

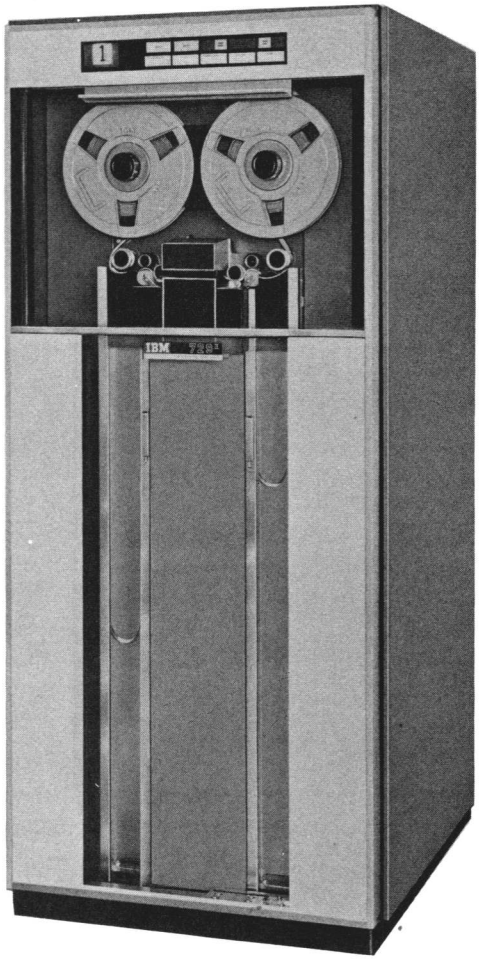


Figure 33. IBM 729 Magnetic Tape Unit

Characteristics	729 II		729 IV		729 V			729 VI		
Tape Speed (inches per second)	75		112.5		75			112.5		
Record Density (characters per inch)	200	556	200	556	200	556	800	200	556	800
Maximum Data Rate (characters per second)	15,000	41,700	22,500	62,500	15,000	41,700	60,000	22,500	62,500	90,000
Character Time (microseconds per character)	67	24	44	16	67	24	17	44	16	11
Average Access Time (milliseconds)	10.8		7.3		10.8			7.3		

Figure 34. IBM 729 Magnetic Tape Units Characteristics

TAPE DENSITIES OPTION SWITCH

SWITCH SETTING	HIGH/LOW DENSITY VALUES
I	800/556 CPI
II	800/200 CPI
III	556/200 CPI

Characteristics of the tape units at all densities are shown in Figure 34.

For details concerning 729 tape units, refer to *IBM Reference Manual, Magnetic Tape Units,* Form A22-6589, and *IBM 729 V and 729 VI Magnetic Tape Units Bulletin,* Form G22-6629-1.

IBM 7908 Data Channel

The IBM 7908 Data Channel, in conjunction with the fifth bank of central storage (bank 4), provides six additional channels for the attachment of I-O devices. Six channel word sets of bank 4 are directly associated with the channels of the 7908. That is, there is a correspondingly numbered channel in the 7908 for each of the six channel word sets used in bank 4. These are 40, 41, 44, 45, 46, and 47; channel word sets 42 and 43 are not used. Channels 40 and 41 are high-speed channels. The 7908 is available in the following models:

MODEL	AVAILABLE CHANNELS
1	44
2	44, 45
3	44, 45, 46
4	44, 45, 46, 47
5	40, 41
6	40, 41, 44
7	40, 41, 44, 45
8	40, 41, 44, 45, 46
9	40, 41, 44, 45, 46, 47

Data Flow

Channel word sets 44 through 47 serve a function identical to channel word sets 20 through 23 of bank 2, and operate in the same manner for the assembly and disassembly of five-character words.

Channels 40 and 41 are high-speed channels; that is, each is provided with a ten-character buffer in the 7908 for the independent assembly and disassembly of five-character words. Word transfers to and from memory are made directly between the channels and the 7302 core storage, through CPU. Channels 40 and 41 require fewer central storage cycles in their operation than do channels 44-47.

When writing a record over channel 40 or 41, the address of the write instruction is placed in the channel data memory address (word 1 of the channel word set). The first five characters are then read out of memory in parallel directly to the data channel, and placed into one-half of the ten-character buffer. The five characters are then sent serially to the control of the output unit. While the transmission of the characters over the channel is occurring, the data memory address is incremented by five, and the second set of five characters is read out of memory and placed in the other half of the ten-character buffer. This cycle is repeated until a group mark is sensed in one of the channel buffers, ending the operation.

In reading a record over channel 40 or 41, the above procedure is reversed. Termination of the read occurs upon receipt of an end signal from the control. If the number of characters in the record is not divisible by five, additional group marks are inserted and transferred to memory.

At the end of a read or write operation, the data memory address contains an address five positions higher that the memory address of the last group of five characters involved in the operation. For a write instruction, the last group handled is the group following the group mark. Although this additional group

is transmitted to the channel buffer, transmission to the I-O device ends with the character before the group mark. The data memory address always ends in 0 and 5.

Scheduling Simultaneous I-O Operations

The following procedure permits determination of the number of I-O devices that can operate simultaneously on the 7080 System without loss of data.

1. Select the desired devices and their respective weight factors from Table 1.

2. Assign the devices with the highest character rates to the channels with the highest priority. High to low channel priority sequence is 40, 41, 44, 45, 46, 47, 21, 22, 23, 20. If the character rates are not in descending sequence after being assigned in this order, they will be operated out of channel priority sequence.

If devices with weights of 100 or less are operated simultaneously in channel priority sequence, the total allowable weight is 100 for four or more channels, 90 for three, 75 for two. Regardless of the number of channels, maximum weight for any two is 75.

If devices with weights of 29 or less are operated simultaneously out of channel priority sequence, the total allowable weight is limited to 90, 81, and 67.

If devices with weights of more than 29 are operated simultaneously out of channel priority sequence, the total allowable weight is limited to 85, 76, and 64.

When the total weight is above these specified amounts, simultaneous operation may cause errors. Such errors cause a channel check and are recoverable.

Table 1. Weight Factors for 7080

	WEIGHTS PER CHANNEL			
DEVICE	CHARACTER RATE (KC)	LOW-SPEED	HIGH-SPEED UNPACKED	HIGH-SPEED PACKED
729 II, V (200)	15	5		
729 IV, VI (200)	22.5	7		
729 II, V (556)	41.7	11		
729 V (800)	60	14		
729 IV, VI (556)	62.5	15		
7750	71.5	15	7	
1301	90*, 140*	18	9	12
1414-6	90	18	9	
729 VI (800)	90	21		
7340	170*, 340*	39	20	35
7740	48	10	5	
1302	184*, 276**	36	18	25
7320	208*, 312**	43	21	28

* Unpacked ** Packed

7080 Example:

CHANNEL	DEVICE	DATA RATE	LOW-SPEED WEIGHT FACTOR
44	7340	170 kc	39
45	7340	170 kc	39
21	729 IV (200)	22.5 kc	7
20	729 IV (200)	22.5 kc	7
			92

This configuration will run simultaneously without loss of data.

The 7080 instruction execution times given in the appendix are valid when there is no simultaneous channel operation. When there is simultaneous channel operation, the instruction execution time is increased in relationship to the amount of data being transmitted by the channels at that time. The maximum percentage of increased instruction execution time is approximately one-half the total weight of the I-O devices operating simultaneously at that time.

Six-Bit and Eight-Bit Modes

The high-speed channels of the 7908 data channel provide the attached I-O control with data in either the six-bit or the eight-bit mode, depending upon the mode of operation of the attached I-O control. The IBM 7640 Hypertape Control always operates in the eight-bit mode. The 7631 File Control can operate in either the six-bit or the eight-bit mode under program control. The 7631 uses the six-bit mode order (09) or the eight-bit mode order (08) to set the mode of operation. The data compression feature requires the eight-bit mode of operation. The 7908 receives data from the 7080 in six-bit BCD code, and transmits data over channels to an I-O control in either six-bit or eight-bit mode. The 7908 receives data from an I-O control in either the six-bit or the eight-bit mode, and transmits the data to the 7080 in the six-bit BCD code.

Data Compression

Data compression (or character packing) consists of translating two 7080 non-zoned BCD characters into one eight-bit character. To provide program control for data compression, the normal set density high (SDH) instruction, when used over channels 40 and 41, causes the 7908 to enter the data compression mode; the normal set density low (SDL) instruction resets the mode. The data compression mode is also reset by power-on reset, clear memory key, channel reset, and auto load key.

NOTE: Data compression applies only to read and write instructions; control and sense instructions are not affected when used in the data compression mode.

Data compression imposes the following limitations:

1. Data compression can be performed on channels 40 and 41 only.

2. Zoned BCD characters (with the exception of blanks) are written as six-bit characters with ones in the bit positions 0 and 1. The one bits in these positions serve as an internal indication that data com-

pression has not occurred for this character. The following are the bit code assignments:

Eight-bit character bit code	0 1 2 3 4 5 6 7
BCD code translated to 8-bit code	0 0 B A 8 4 2 1
BCD non-zoned characters in the data compression mode	8 4 2 1 8 4 2 1

The following examples illustrate the handling of compressible and non-compressible characters:

BCD character A in 8-bit code (not in data compression mode)	0 0 1 1 0 0 0 1
BCD character A in 8-bit code (in the data compression mode)	1 1 1 1 0 0 0 1
Two BCD characters (24) (in the data compression mode)	2 4 0 0 1 0 0 1 0 0

3. Non-zoned BCD characters (8-4 combinations excluded) can be compressed. Two consecutive four-bit characters are combined into one eight-bit character. The 0, 1, 2, and 3 bit positions of the 8-bit code correspond to the 8, 4, 2, and 1 bit positions, respectively, of the first character to be combined. The 4, 5, 6, and 7 bit positions of the eight-bit code correspond to the 8, 4, 2, and 1, respectively, of the second character to be combined. (The above example of BCD 24 character sequence illustrates this.) The 8-4 combination character @ cannot be compressed since this could result in a conflict with 2. above. If the @ were the first of two non-zoned characters, compression would result in 1 bits being placed in positions 0 and 1. When this character was read back it would be treated as a non-compressed character, resulting in the loss of the @.

4. Blank characters are compressed; the A bit is dropped when compression occurs.

Figure 35 illustrates the data compression, including examples of the above limitations.

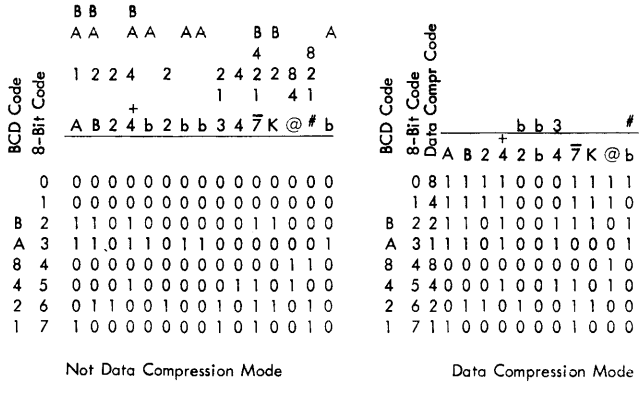


Figure 35. Data Compression

To allow for proper data decompression with the backward read feature of Hypertape, channels 40 and 41 employ a backward mode. Execution of any control order of 07 (07X—Select for Backward Reading on Hyper) causes the channel to enter this mode; a control order of 06 resets the mode. The backward mode is also reset by power-on reset, clear memory key, channel reset, and auto load key.

If a control order of 07 is issued to a device that does not read backward, any read in the data compression mode that follows results in incorrect data in memory.

NOTE: Backward mode does not cause the read-in field to be reversed in memory. It merely allows compressed data that is being read backwards to be reconstructed properly.

Example:

Field in Memory before write:

AB12b24C

Field in Memory after Read Backward, Backward Mode:

C42b21BA

Field in Memory after Read Backward, not Backward Mode:

C4b212BA

All operations in compressed mode.

Channel Interrupt

An interrupt can occur for the channels of the 7908 upon the receipt of an end, unusual end, or attention signal from the control. The control signals an end at the completion of a successful transmission of data between the I-O device and the 7080. An unusual end signal results from an error condition in the transmission of data, or an unsuccessful attempt to transmit data between the device and the 7080. An attention signal results when a device is made ready, or at the completion of an order involving a mechanical operation. If an attention is received while the channel is busy, the interrupt is suspended until the channel is ready.

Channel Indicators

Each channel of the 7908 is provided with a channel check indicator, an attention indicator, and a ready line.

The channel check indicator is turned on by an unusual end signal, or by an error detected during the transmission of data between the I-O device and the 7080. The transfer on signal 02 (TTC) may be used to interrogate the channel check indicator. The indicator

is turned off upon the execution of a subsequent read, write, control, or sense instruction over the channel.

The attention indicator is turned on by the attention signal. It may be interrogated and turned off by the transfer on signal 00 (TRS) instruction.

The ready line is up whenever the channel is not busy; that is, when the channel is not involved with a read, write, control, or sense instruction. The line may be interrogated by the transfer on signal 01 (TRR) instruction.

The transfer on signal 03 (TSA) instruction may be used to interrogate both the channel check and the attention indicators. A transfer is effected if either or both of the indicators are on. If the channel is busy, the execution of the instruction is held up until the channel becomes ready again.

Data Channel Status Character

The IBM 7908 Data Channel generates a four-bit status data character for each read, write, control, or sense operation performed over the channels of the 7908. This character is sent as the final character of the data transmitted to the 7080 as a result of a read 03 operation to indicate the status of the attached input-output unit and the 7908 channel. The four-bit character is transmitted over the A, 4, 2, and 1 bit lines. The B bit is always a 1; the 8 bit is always a 0. The bits and their assignments indicate:

- A — Channel identification (identifies the channel over which a data check, address check, or a read error has occurred)
- 4 — Read-Write Error
- 2 — Mode Check (indicates that unwanted information is being read on the 0 or 1 bit lines when the data channel is operating in the unpacked mode)
- 1 — Unusual End

Any of the four bits turn on the channel check indicator. The 7908 also generates the correct C bit.

Disk Storage

The IBM 1301 Disk Storage (Figure 36), the IBM 1302 Disk Storage and the IBM 7631 File Control are available with the 7080 system.

The 1301 Disk Storage is a random access storage device that provides large capacity, low access time, high reliability, and advanced operational characteristics. It is available in two models: model 1, containing a single module; and model 2, containing two modules. A module is 25 vertically aligned magnetically coated disks, providing 50 recording surfaces. Twenty disks (40 surfaces) serve as data recording surfaces. The remaining five disks provide alternate surfaces, a clock surface and a format surface. A surface has 250 recording tracks, and each track can store up to 2,800 characters; thus, a two-module disk storage provides a capacity of 56,000,000 characters.

Each module has an associated access mechanism that provides a read-write head for each disk surface in the module, and positions the heads in any one of the 250 track positions. The access time is 50 to 180 milliseconds, with an average rotational delay of 17 milliseconds.

The 1301 provides for variable length records, and places the format and addressing schemes under control of the programmer. It has an instantaneous character rate of 90,000 characters per second with as many as 112,000 characters available per access setting.

The 1302 Disk Storage is similar in appearance and function to the 1301 but has a larger capacity and an additional access mechanism. It is available in two models: model 1, containing a single module; and model 2, containing two modules. Each module is constructed in the same manner as those of the 1301 except that there are two access mechanisms per module and two sets (one per access) of 250 tracks per disk surface.

The recording density of the 1302 is slightly more than double that of the 1301; each track can store up to 5,850 characters. A two module 1302 can store up to 234,000,000 characters.

Access time and average rotational delay are the same as for the 1301. Instantaneous character rate is 184,000 characters per second and as many as 234,000 characters are available per access setting. Programming is similar to that used with the 1301 except for the ability to address the second access mechanism.

The 7631 File Control is available in three models for the 7080 system: model 2 for exclusive use with a 7080 system; model 3 for shared use with an IBM 1410 Data Processing System; and model 4 for shared use with another 7080 or any other 7000 series system.

The 7631 file control also provides cylinder mode operation (optional feature), allowing the reading or writing of 40 tracks of information in one operation.

The file control will attach as many as five disk storage units, giving a capacity of as many as 280,000,000 characters.

The 7631 decodes and executes orders transmitted from the 7080 system; the file control orders and their mnemonic and numeric codes are:

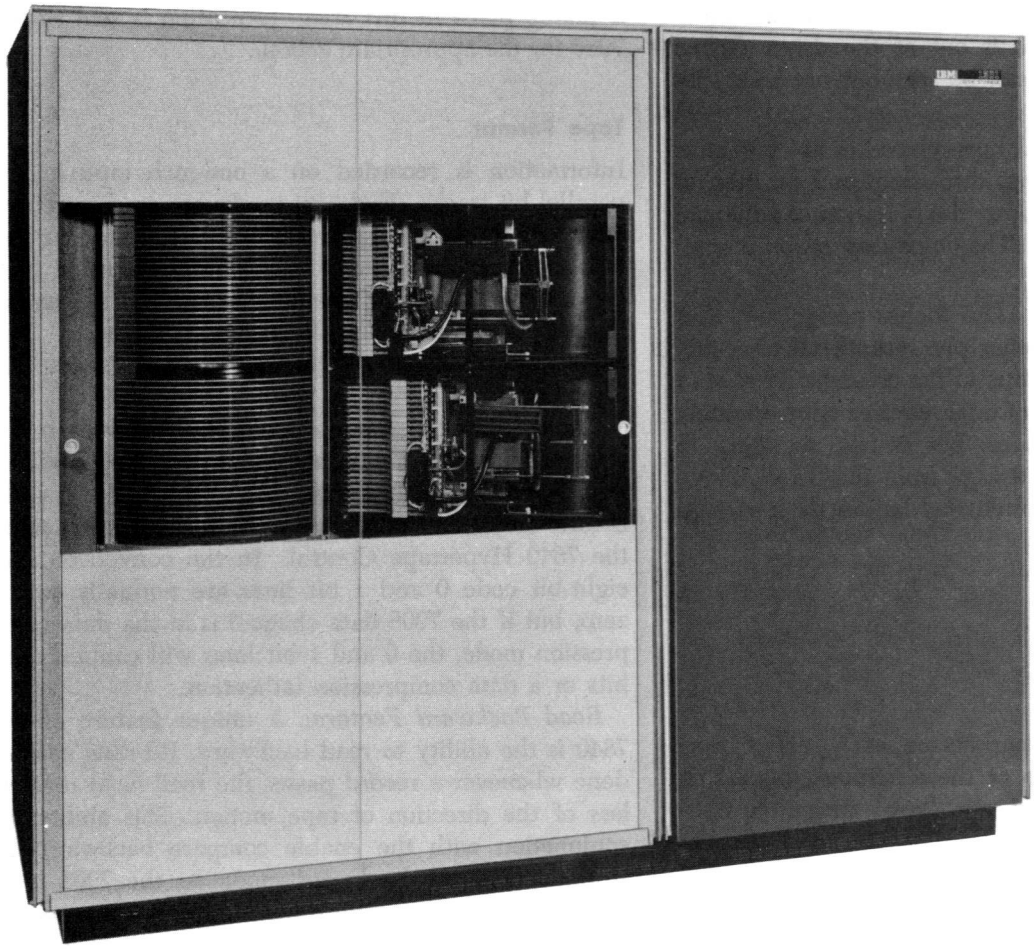


Figure 36. IBM 1301 Disk Storage

ORDERS	MNEMONIC	NUMERIC
No Operation	DNOP	00
Release	DREL	04
Eight-Bit Mode	DEBM	08
Six-Bit Mode	DSBM	09
Seek	DSEK	80
Prepare to Verify—Single Record	DVSR	82
Prepare to Write Format	DWRF	83
Prepare to Verify—Track Without Addresses or	DVTN	84
(Optional Feature) Cylinder Operation	DVCY	85
Prepare to Write Check	DWRC	86
Set Access Inoperative	DSAI	87
Prepare to Verify—Track Operation	DVTA	88
Prepare to Verify— Home Address Operation	DVHA	89

A detailed description of disk storage and the file control is contained in *IBM 1301, Models 1 and 2, Disk Storage and IBM 1302, Models 1 and 2, Disk Storage with IBM 7080 Data Processing System,* Form A22-6786.

IBM 7340 Hypertape Drive

The 7340 Hypertape Drive (Figure 37) records data on a one-inch tape in ten parallel bit tracks, at a density of 1,511 characters per inch, and a character rate of 170,000 characters per second.

Cartridge

The 7340 employs a tape-enclosing cartridge device. The cartridge is approximately 17 inches long, 10 inches high, and 2 inches wide. It encases both the supply reel and the take-up reel.

The cartridge is equipped with a file protection device; when set on, the device will prevent writing on tape. When the cartridge is file protected and is out of the 7340, file protection is indicated by a red indicator that can be seen when viewing the cartridge from the back. When the cartridge is file protected and loaded in the 7340, the file protection light is on.

The file protection device can be set or reset manually when the cartridge is out of the drive. When loaded in the drive, it can be set (but not reset) by program control.

After the cartridge has been placed in its receptacle in the drive, the loading, threading, and position of the tape are automatic upon the initiation of a manual or program load control. The unload operation is similarly automatic.

Tape is processed at 112.5 inches per second, and rewind speed is 225 inches per second; all tape motion is performed with tape in the columns. A rewind operation for a full reel of tape requires approximately one and one-half minutes, but is not necessary in order to remove the cartridge from the drive. However, the tape must be unloaded before the cartridge can be removed.

Tape Markers

There are three tape markers on each reel of tape used by the 7340. Two of these markers, beginning of tape (BOT) and end of tape (EOT), define the writing area of the tape. The third marker, end warning area (EWA), informs the operator that writing is taking place in an area that is within a specific distance from the EOT.

Beginning of Tape (BOT): This marker is similar to the load point marker used with the 727-729 tape units. The marker is a photosensed area located at the inner edge of the tape (edge nearest machine), approximately 25 feet from the physical beginning of the tape. Sensing this marker stops all machine operation involving backward tape motion, and interlocks the machine to prevent backward motion beyond this point.

End of Tape (EOT): This marker prevents any forward motion beyond this point. It is similar in size and make-up to the BOT marker. It is located at midpoint from the edges of tape, 25 feet from the physical end of tape.

End Warning Area (EWA): This marker, similar to the end-of-reel marker of the 727-729 tape units, informs the operator that writing is taking place in an area that is within 40 feet of the end of tape. This marker is located at the outer edge of the tape (edge nearest the operator), 40 feet from the EOT marker. The width of this marker is kept at a minimum since writing takes place in this area (unlike the areas involving the BOT and EOT markers, where writing never takes place). When this marker is sensed, the EWA indicator turns on and remains on as long as writing is taking place in this area. Indication is sent to the 7080 for the appropriate action.

Tape Format

Information is recorded on a one-inch tape in ten parallel bit tracks. Eight bit tracks are used to record data; two tracks are used for check bits. The recorded tape character consists of information recorded in a bit-wide column which extends across the ten tracks and is perpendicular to the edges of the tape. The check bits provide for error correction and complete error detection.

The six-bit BCD characters of the 7080 system are transmitted to the 7908 data channel in five-character groups where they are converted to the eight-bit code before they are transmitted serially by character to the 7640 Hypertape Control. In the conversion, the eight-bit code 0 and 1 bit lines are normally set to zero, but if the 7908 data channel is in the data compression mode, the 0 and 1 bit lines will contain data bits or a data compression indication.

Read Backward Feature: A unique feature of the 7340 is the ability to read backward. Reading can be done whenever a record passes the read head regardless of the direction of tape motion. This ability, in conjunction with the enable compare backward instruction and the backward mode on the 7908 high speed channels, can save rewind time on even passes of a sort program for instance. The records are assembled and transmitted to memory in the reverse order from that in which they were written. Thus a record that originally was in memory as JOHN DOE 56789, after being written and read backward would appear as 98765 EOD NOHJ. Failure to set the backward mode in the 7908 high speed channel when reading compressed data may yield incorrectly sequenced numerical data.

IBM 7640 Hypertape Control

All operations performed by the 7640 Hypertape Control and the 7340 Hypertape Drive result from four basic instructions: read, write, sense, and control. The read and write instructions perform the same function as performed by other I-O devices. The sense instruction (read 03) results in the transfer of status data from the Hypertape Control to the 7080, indicating error and attention conditions of the control channel that has been selected. The control instruction (write 03) results in the transmission of orders from the 7080 to the control in the same manner as data is transmitted. The orders are decoded and executed by the control.

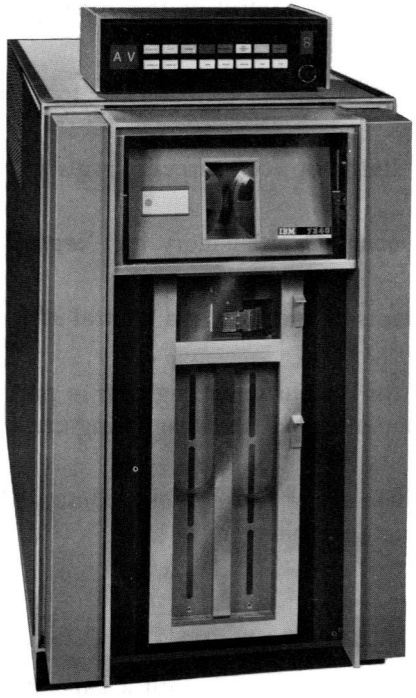


Figure 37. IBM 7340 Hypertape Drive

The 7640 Hypertape Control attaches to two channels of the 7908 data channel, and controls as many as ten Hypertape drives on each channel, providing a maximum of twenty drives. Basically, the 7640 functions as two controls, making possible simultaneous operation of the drives on opposite channels. Reference may be made to simultaneous operation of the 7640 in terms of "control-read", meaning simply that a control operation is being performed by a drive on one of the channels while a read operation is being performed by a drive on the opposite channel.

The read and write circuitry of the 7640 operates on a time-shared basis; thus, a simultaneous read-read or write-write cannot be performed. If a read instruction is given to a drive on one channel of the 7640 while the other channel is reading, the second read operation instruction is stored until the current read operation is finished. All other combinations of operations, however, can be performed simultaneously. These are:

1. Read-Write
2. Control-Control*
3. Control-Sense
4. Sense-Sense
5. Control-Read
6. Control-Write*
7. Sense-Read
8. Sense-Write

*Control operations involving the write-tapemark order have the same simultaneous operation limitations as the write-write operations.

Status Data

The status of each of the two channels of the 7640 and their associated Hypertape drives is set in and retained by the 7640 Hypertape Control, and is always in available form to be sent to the 7080 system. The error, unusual, and attention conditions are set in bit form to make up status data. The sense instruction, read 03, transfers the status data to the 7080 system.

The status data consists of 14 characters, with four bit assignments per character to indicate specific conditions. The four-bit characters of the status data are transmitted over the A, 4, 2, and 1 bit lines (the normal 8 bits are transmitted over the A bit line); a B bit is emitted into all sense data characters, and the 8 bit is always set to 0.

The selected drive addresses appear as follows in the status data:

CONTROL DRIVE ADDRESS	SENSE DRIVE ADDRESS	BCD BITS
1	J	B, 1
2	K	B, 2
3	L	B, 1, 2
4	M	B, 4
5	N	B, 1, 4
6	O	B, 2, 4,
7	P	B, 1, 2, 4
8	&	B, A
9	A	B, A, 1
0	B	B, A, 2

For a detailed description of status data, see *IBM 7340 Hypertape Drive, Reference Manual,* Form A22-6616.

Control Operation

The control instruction (write 03) results in the transmission of orders to the Hypertape Control as data. The orders are transmitted as two digits (four-bit bytes), except for select and select for backward reading, which are transmitted as three digits. After the order is transmitted to the control, the order is decoded and executed by the control.

Orders

An order is transmitted to the 7640 Hypertape Control by a special write instruction in the same manner as data. The control recognizes an order, decodes the order, and then executes it. The order consists of an operation code and, in the case of a select order, the

address of the Hypertape Drive. The control orders and mnemonic and numeric codes are:

ORDERS	MNEMONIC CODE	NUMERIC CODE
No Operation	HNOP	00
End of Sequence	HEOS	01
Reserved Light Off	HRLF	02
Reserved Light On	HRLN	03
Check Light On	HCLN	05
Select*	HSEL	06X
Select for Backward Reading*	HSBR	07X
Change Cartridge and Rewind	HCCR	28
Rewind	HRWD	30
Rewind and Unload Cartridge	HRUN	31
Erase Long Gap	HERG	32
Write Tape Mark	HWTM	33
Backspace	HBSR	34
Backspace File	HBSF	35
Space	HSKR	36
Space File	HSKF	37
Change Cartridge	HCHC	38
Unload Cartridge	HUNL	39
File Protect On	HFPN	42

* Requires a third digit (0-9, address of Hypertape Drive).

A detailed description of the above orders can be found in *IBM 7340 Hypertape Drive, Reference Manual,* Form A22-6616.

IBM 7153 Console

The operator's console (Figure 38) is a separate unit and may be placed in any convenient location within the cable length restrictions.

The console serves as the control of the 7080 system; it is used to:

1. Control the machine manually.
2. Correct errors.
3. Determine the status of 7080 circuits, registers, and counters.
4. Determine the contents of memory and central storage.
5. Revise the contents of memory and central storage.
6. Serve as an aid for the customer engineer in performing preventive maintenance and diagnosing error conditions.

Figure 39 is a schematic of the console. Descriptions of the various features follow.

Display Unit

A display unit is a projection device with a capacity of twelve individual "messages." A message, printed on the surface of a lens, is projected on a viewing screen that forms the front of the unit. The message displayed is the operation code, ASU, the address, and the counter or register containing the address. Fourteen units, from left to right, make up an operation code display, an ASU display, and an address display.

No display occurs in an address digit position containing an 8-4 or 8-2-1 bit combination.

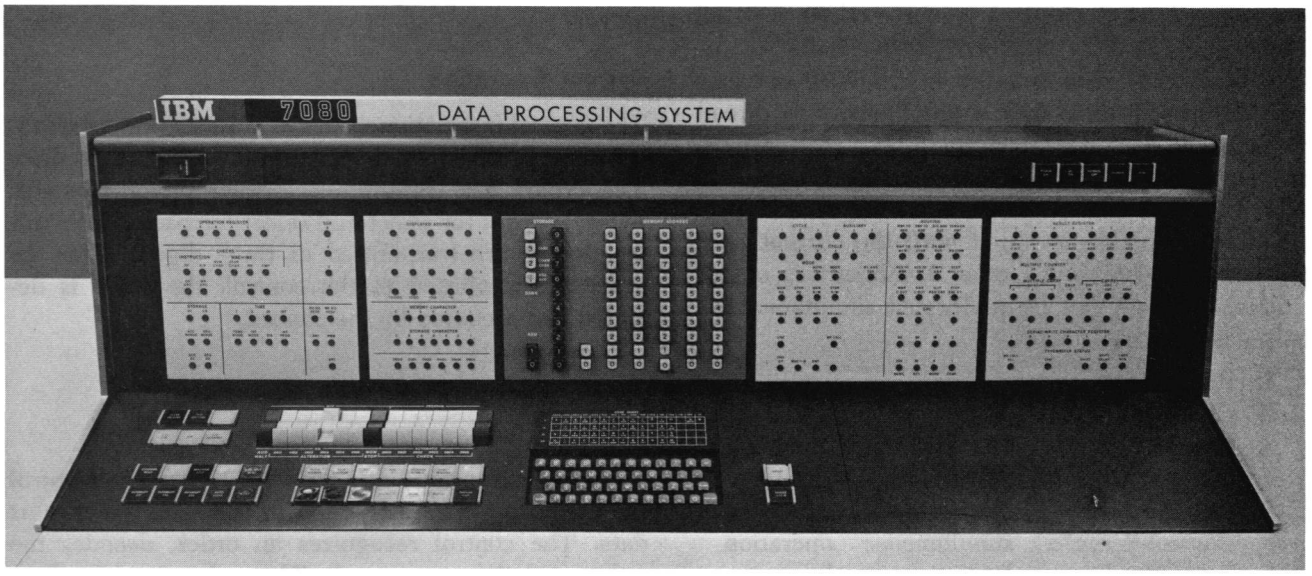


Figure 38. Console

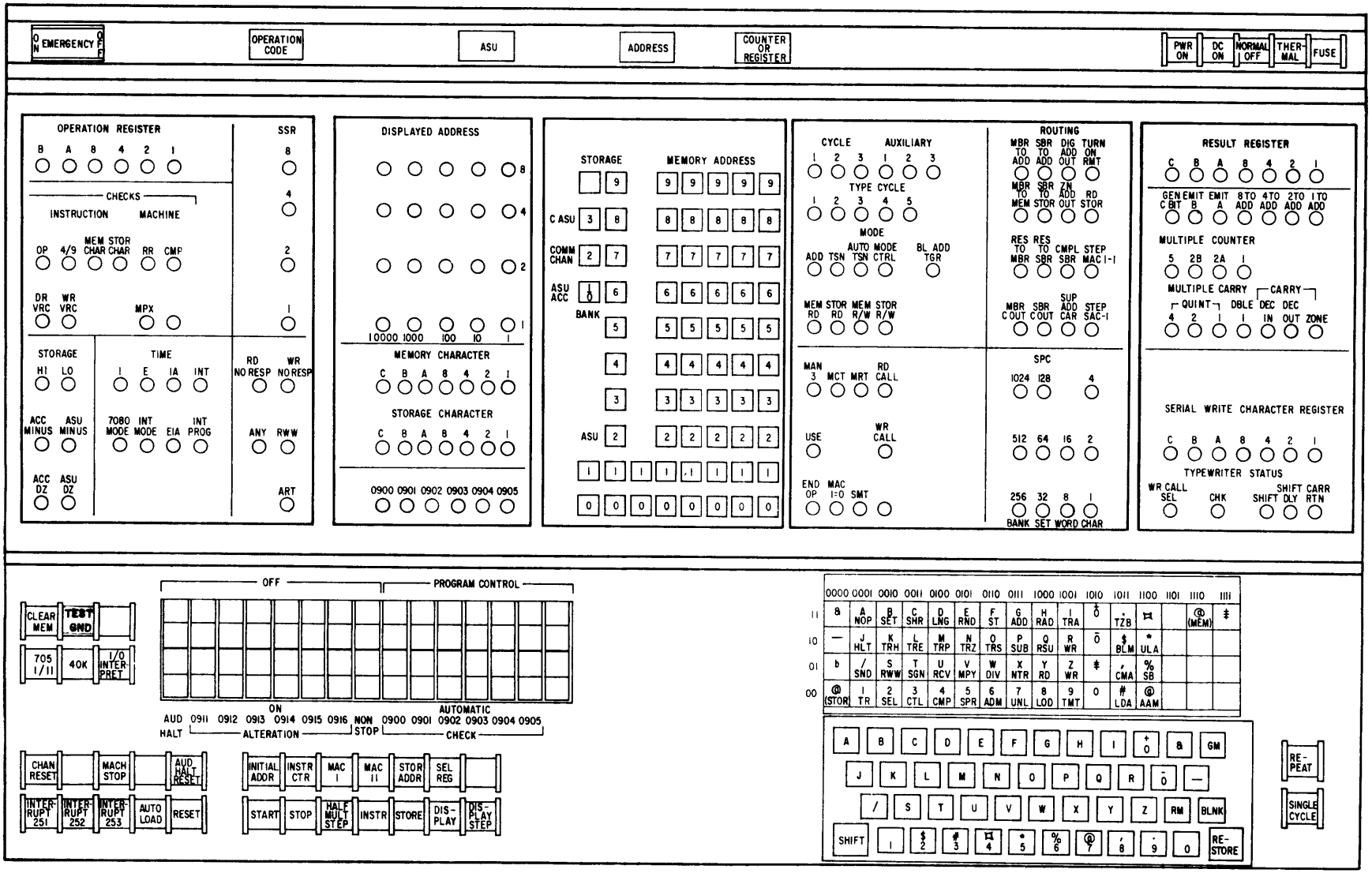


Figure 39. Console Schematic

The displays are activated under the following conditions:

1. The machine has stopped and is in manual status.
2. The machine is unable to complete the execution of an instruction. Approximately two seconds are required to recognize this condition.
3. The half-multiple step key is depressed.

Operation Code Display: This display is one of a series of mnemonic operation codes. Units are provided with a capacity of 60 distinct codes, although only 54 codes are displayed (Figure 40). The 54 codes correspond to the basic set of 42 operations for 705 III mode, plus 12 operations used only in the 7080 mode.

This display is associated directly with the internal operation register. No display will occur if the register contains an unassigned operation character.

Those instructions which have the same operation code but different mnemonics will only display the basic mnemonic associated with the operation code, i.e. EEM (Control 15), RWD, and CHR (Control 13) will all display CTL. The distinction must be made on the basis of the memory and storage addresses displayed with the mnemonic.

ASU Display: A two-digit number (00-15) is displayed, corresponding to the contents of the storage select register.

Address Display: Seven units are required for this display. The first six display a 6-digit number corresponding to the contents of any one of the following registers or counters:

Instruction Counter (IC) (Figure 41)
Initial Address Register (IAR) (Identical to MAR on 705 machines)
Memory Address Counter I (MAC I)
Memory Address Counter II (MAC II)
Select Register (SR)
Storage Address Switch (SAS)

The last unit displays the identifying tag or mnemonic code (shown above and in Figure 41) of the register or counter containing the address.

OPERATION CODES THAT CAN BE DISPLAYED

AAM	LDA	RCV	SPC	TRP
ADD	LFC	RD	SPR	TRS
ADM	LIM	RND	ST	TRZ
BLM	LIP	RSU	SUB	TZB
CMP	LNG	RWW	TCT	UFC
CNO	LOD	SB	TIP	ULA
CTL	LSB	SEL	TMT	UNL
DIV	MPY	SET	TR	USB
EIA	NTR	SGN	TRA	WR
EIM	NOP	SHR	TRE	WRE
HLT	RAD	SND	TRH	

Figure 40. Operation Codes That Can Be Displayed

REGISTER OR COUNTERS FOR WHICH ADDRESS CAN BE DISPLAYED

IAR	MAC I	SAS
IC	MAC II	SR

Figure 41. Registers or Counters Whose Address Can Be Displayed

Display Selector Keys

This group of six keys controls the information shown in the address portion of the address display unit. The keys are labeled INITIAL ADDRESS, INSTR COUNTER, MAC I, MAC II, STORAGE ADDRESS, SELECT REGISTER. The keys are back-lighted; the light is turned on when the corresponding key is depressed, indicating ON, and is turned off by depression of one of the other five keys. Once a key is depressed ON, the corresponding counter or register will continue to be selected until another key is depressed. After start, IAR display is automatically selected.

Displayed Address

Twenty indicator lamps display a five-digit BCD address corresponding to the address shown by the address display unit above. The fifth position will display full binary, making possible the display of 159,999. Multi-digit bit combinations (8-4, 8-2-1) will be displayed here, even though the corresponding digits will not be displayed in the address display.

Information displayed in the BCD indicator lamps is also under control of the display selector keys. For example, if the IC key is depressed, the address of the instruction counter will be displayed both as a six-digit number and as a five-digit character address.

The start key resets the BCD display to the IAR display.

Operation Register

The contents of the operation register are displayed as a 6-bit character in BCD code by six indicator lights. The character displayed corresponds to the mnemonic code in the operation code display unit. Illegal operation codes, while not displayed in the upper display, will be shown in the BCD lights.

Storage Select Register (SSR)

The contents of the storage select register are displayed in binary by four indicator lights. The number displayed corresponds to the two decimal digits displayed in the ASU display unit.

Checks

The check stop indicator lights display the cause of an error detected by an instruction, machine, or channel check.

INSTRUCTION CHECK LIGHTS

Operation Check (OP CHK): This indicator turns on when the operation part of an instruction is not one of the 52 operation codes of the 7080, or when comma operations are given in other than 7080 mode.

4 or 9 Check: The indicator turns on when the units position of the address of any transfer, five-character transmit, send, or indirect address instruction is not 4 or 9.

VERTICAL REDUNDANCY CHECKS (VRC)

Data Register (DR VRC): During I time, this check results if any one of the five characters from the memory data register is in error. During IA time, only characters 1, 2, 3, and 4 are checked. During E time, this check results if any one of the five characters from the memory data register is in error during parallel transmission (TMT 00, TCT, SND 00).

Word Register (WR VRC): During E time, this check results if any one of the eight characters from the storage word register is in error during a LIP or automatic interrupt.

CHANNEL CHECKS

Multiplexor Check (MPX): This indicator is turned on when any error is detected in a communication channel. This check is similar to the DSU check in the 705 III. The following checks will cause an MPX check:

1. Channel Check from channel 20-23 (indicator is in the 7621 tape control) results from: (1) A check during data transfer between the data register and storage from either a read or write instruction; (2) Any read or write operation exceeding the absolute end of memory (overflow); (3) Read errors; (4) Address check resulting from no 0 or 5 in character 4 of the memory address or a VRC in the address characters.
2. Channel Check from channels 40, 41, 44-47 (indicator is in the 7908 Data Channel) results from: (1) An unusual end signal from an I-O device attached to the channel. (2) An error detected during the transmission of data between the I-O device and the 7080.

MACHINE CHECKS

Memory Character Check (MEM CHAR): This indicator is turned on if the character from the memory buffer register is invalid.

Storage Character Check (STOR CHAR): This indicator is turned on when the character from the storage buffer register is invalid.

Result Register Check (RR CHK): This indicator is turned on when an invalid character is detected in the result register.

Compare Check (CMP CHK): This indicator is turned on, after a compare instruction, (1) if only the high or low indicator is on without the auxiliary 1 indicator, or (2) if all three indicators are on.

Storage Indicators

High (HI): This indicator is turned on (along with the auxiliary I indicator) during a compare operation when the field in storage is higher in sequence than the field in memory. The auxiliary indicator is in another section of the panel which contains those indicators primarily for the use of the customer engineer.

Low (LO): This indicator is turned on (along with the auxiliary 1 indicator) during a compare operation when the field in storage is lower in sequence than the field in memory.

Accumulator Minus (ACC MINUS): This indicator is turned on when the sign of the storage field in the accumulator is minus. Normally, the accumulator is bank 0, but, by use of SPC instruction, any bank can be made to be the accumulator.

Auxiliary Storage Unit Minus (ASU MINUS): This indicator is on when the sign of the field in the last used ASU is minus. The ASU may be any one of fifteen storage units contained in either banks 1 or 3.

Accumulator Digit Zero (ACC DZ): This indicator is on when the contents of the accumulator to the right of the first storage mark consist of characters having zero numerical portions. Accumulator may be any storage bank.

Auxiliary Storage Unit Digit Zero (ASU DZ): This indicator is on when the field in the last used ASU consists of characters with zero numerical portions. The ASU may be any of the storage units in either banks 1 or 3.

Time and Mode Indicators

The time indicators, instruction (I), execution (E), indirect address (IA), and interrupt (INT), when on, indicate the actual internal operating time in which the computer is functioning.

7080 Mode: This indicator is on when the computer is operating in the 7080 mode. The machine is normally in 705 operating status and must be programmed to enter the 7080 mode. It will remain in 7080 mode unless instructed to leave 7080 mode or by depressing the auto-load, reset, or clear memory key.

Interrupt Mode: This indicator is on when the machine is operating in the interrupt mode. The machine can enter interrupt mode by programming. It is turned off by the instruction leave interrupt mode or by the depression of the auto load, reset, or clear memory key.

Interrupt Program (INT PROG): This light is turned on by: automatic interrupt, a TIP instruction, manual interrupt key, non-stop operation, or an instruction to transfer to an interrupt program. The system remains in the interrupt program until instructed to leave and return to the main program. It is also turned off by the clear memory, reset or auto-load key.

Enable Indirect Address (EIA): This indicator is turned on when the machine is instructed to execute, via the EIA instruction, the following instruction as one having an indirect address. It is turned off during execution of the indirectly addressed instruction.

Input-Output Indicators

Read No Response (RD NO RESP): This indicator is turned on when the selected input unit does not respond. The light is turned on, for example, when an input unit, that is not connected to the system or is not in ready status, is selected and instructed to read.

Write No Response (WR NO RESP): This indicator is turned on when a selected output unit does not respond; for example, when the selected output unit is given a write instruction and it is not connected to the system or is not in ready status.

Read While Write (RWW): The indicator turns on during the execution of a read-while-write instruction (754 only).

Any: An error condition that turns on a check indicator also turns on the ANY indicator, *unless* the corresponding indicator switch (00900-00905) is set to automatic and non-stop switch is off, causing a check stop.

NOTE: The non-stop switch is considered an alteration switch. Depression of the start key *does not reset* the ANY indicator or those check indicators whose corresponding switches are set to PROGRAM. These conditions apply to *all* modes of operation, including the 705 I-II, 705 III, and 7080. However, depression of auto load, reset, or clear memory key does turn ANY off.

Automatic Restart (ART): This indicator is turned on whenever the 7080 does not complete the execution of an instruction, other than a read or write operation, in approximately two seconds. A reading or writing operation can take more than two seconds. In this case, the indicator is turned on if no data is sent or received by the CPU during a two-second interval and the read or write operation has not been completed.

The automatic restart indicator is turned off by a transfer auto restart instruction.

Character Registers

Memory Character: The seven lights display the BCD character most recently read from MBR.

Storage Character: The seven lights display the BCD character most recently read from SBR.

Check Lights

Six lights are provided; one for each of the check indicators, 00900-00905. A corresponding switch is provided for each light.

Storage Bank Selector Keys

This is a set of three keys that control storage bank addressing during manual display operations. All three keys latch in when depressed. Only one key can be depressed at a time and will reset any other key. All keys reset when the keyboard is restored.

When the CASU or COMM CHAN key is in, the corresponding central storage bank will be displayed starting at the setting of the starting point counter unless ASU keys are in. ASU keys work in conjunction with bank keys to address two words (16 characters) of a communication channel or CASU (except for CASU 15 with ASU 15 keyed in, which addresses four words). Thus, the storage select keys with the bank keys can be used to display the contents of storage units within these banks.

If none of the bank keys is in or if the 1/0 key is in, corresponding to a reset state, ACC or ASU central storage banks 0 or 1 are addressed, depending upon whether or not the storage selector keys are used. The bank keys have no effect upon operations other than display.

Storage Selector

The storage selector keys select the storage unit used in a manual instruction or in display operations. The selection is made by keying the decimal number of the storage unit (00-15): the units digit in one of the ten keys in the right-hand vertical row, the tens digit in one of the two keys in the left-hand vertical row. Each key will remain down when depressed and will release any other key in the row. Therefore, only one key in a row can be down at one time. The bank and ASU selector keys (only) are automatically restored when any of the following three situations takes place:

1. The machine leaves DISPLAY status.
2. The machine leaves INSTRUCT or STORE status for reasons other than going into DISPLAY status.
3. The RESET or MACHINE STOP keys are depressed when in other than STORE, DISPLAY, or INSTRUCT status.

Memory Address Selector

Memory address selector keys are arranged in five vertical rows of ten keys each and one row of two keys. Each row corresponds to one position of a six-digit memory address.

The memory address selector keys are used to set up an address when performing the manual operations of instruct, store, or display. Each key will remain down when depressed and will release any other key.

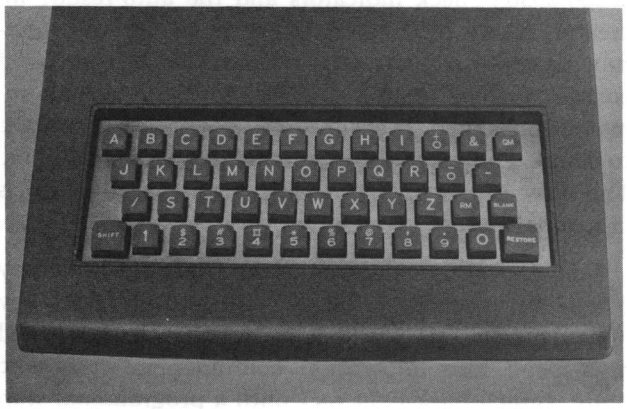


Figure 42. IBM 7080 Keyboard

Keyboard

A modified card punch keyboard (Figure 42) is used to enter data or instructions in memory while the machine is in store status. The operation part of the instruction is keyed on the keyboard while the machine is in instruct status. (Refer to "instruction" and "store" keys.)

Alphabetic characters on the keyboard are arranged in sequence from left to right on the top three rows of keys. The bottom row has numerical digits in the lower case position, and special characters in the upper case position. An upper case key and reset key are also provided.

Control Keys and Lights

Power-On (Back-lighted Key): Depressing the power-on key turns on the AC and DC voltages sequentially in the machine and turns on the back-light under the key. When the voltages are properly stabilized, the machine is automatically reset. The instruction counter is set to address 00004, all positions of central storage are set to storage marks, all memory positions are set to blanks, and all check indicators are turned off.

DC On (Light): This light indicates that DC voltages in the system are at the required levels.

Normal-Off (Key): Depressing this key turns off the AC-DC voltages sequentially in the machine. The cooling system continues to run and is automatically turned off several minutes later.

Thermal (Light): This light turns on when the temperature in any unit of the system exceeds a specified level.

Fuse (Light): This light turns on when any DC fuse in the system is blown.

Clear Memory (Key): Depressing the clear memory key, regardless of mode, in manual or automatic status resets all positions of memory to blank characters (1 01 0000) and central storage to storage marks (0 00 0000). The 00900-00905 check indicators and the auto-restart indicator are reset, and the instruction counter is set to 00004. The 7080, interrupt mode and program triggers are reset off. SPC is set to bank 0; the position within the bank remains unchanged. These functions are also performed automatically whenever the power is turned on and the machine voltages have reached their required levels.

Test Ground (Light): This light signals that (one or more of the following):

1. The CPU is in memory test or storage test.
2. The 7080 is under bias conditions (marginal check).

3. The PDF 48-volt supply is shorted to frame ground.
4. The console card reader is in test status.
5. There has been a power failure to the real-time clock.
6. All I-O cables are not connected to the 7908.
7. One of the devices connected to the 7908 is not operational. The 7631 File Control can be shared by two systems. Because the 7631 drops the "operational in" line to the 7908 while the other system has control of the 7631, the test ground light is caused to blink on and off.

Memory test and diagnostic operations are under control of the customer engineer.

705 I/II (Back-lighted Key): When this key is depressed the machine operates internally as a 705 I or II. The backlight under the key is also turned on. Depressing the key, when it is on, turns off the light and returns the machine to the 705 III mode.

40K (Back-lighted Key): Depressing this key sets the capacity of memory to 40,000 positions in the 705 I-II, or 705 III modes. The back-light under the key is also turned on. With the switch off, the capacity of memory is set to 20,000 positions in the 705 I-II mode, and to 80,000 positions in the 705 III mode. The back-light under the key is also turned off. The condition of the key has no effect when the machine is in the 7080 mode. In this case, the CPU operates as though a 160,000 position memory were being used. Actual capacity of memory, however, is determined by the model 7302 core storage unit connected to the system.

I-O Interpret (Back-lighted Key): Depressing this key permits the use of the I-O interpret feature of the 7080.

Channel Reset (Key): Depression of this key resets all check and status indicators in the communication channels and all tape controls attached. In addition a channel reset will result from power on (all operation voltage levels reached), the depression of the clear memory key, the reset key or the auto-load key.

Interrupt 251, 252, 253 (Keys): Depression of any one of these initiates an interrupt sequence commencing with the instruction whose address is in interrupt word 251, 252, or 253. The key provides a means of interrupting the program manually from the console, for example, to load a program while another program is in progress.

Machine Stop (Key): When an internal operation is being performed, depression of the machine stop key stops the 7080 immediately. The stop can occur during the execution of an instruction such as an arithmetic or writing operation. The key may be used to halt input-output operations or to stop the 7080 when the manual stop key is not effective. Depressing the key during typewriter operation stops writing with a line space and carriage return, in addition to bringing the CPU to a halt.

Auto Load (Key): The following operations are performed by depressing the auto load key:

1. An input unit is selected. For 729 tape units, the address of the channel and unit is keyed in the memory address selector (for example, 002004 will select unit 4 on channel 20). For 7340 Hypertape Drives, the unit selected is automatically 0 (the unit number in the memory select address is ignored), but the channel is keyed in the memory address selector (for example, 004001 will select 0 on channel 40).
2. The 00900-00905 check indicators and the auto-restart indicator are reset, and the instruction counter is set to 00004.
3. In 7080 mode, the interrupt mode and the interrupt program triggers are reset off, and the starting point counter is set to bank 0.
4. One record is read into memory, beginning at location 00000.
5. Automatic operation is started.

Use of this key simplifies and speeds up the loading of a program into memory.

Audible Halt (Switch): When this switch is on and the machine hangs up in automatic or enters manual status for reasons other than the depression of the stop, store, display, or instruct keys, an audible tone sounds at timed intervals. If the switch is off, the audible halt feature is inoperative.

Audible Halt Reset (Key): Depressing this key turns off the audible signal if it is on. The signal will not sound again unless the start key is depressed and another audible halt condition occurs.

Reset (Key): Depressing the reset key restores the 00900-00905 check indicators and the auto-restart indicator, resets 7080 mode, interrupt mode, and interrupt program triggers off, and sets the starting point counter to bank 0; the position within the bank remains unchanged. It also resets the instruction counter to 00004. This reset also occurs with power coming on. The reset key is operative only when the machine is in manual status.

Start (Back-lighted Key): Depressing the start key when the machine is in manual status (stop key lighted) causes the system to operate at its normal high-speed rate. Operation continues in automatic status (green back-light ON) until a programmed stop occurs or until the machine is manually stopped by

depressing machine stop, stop or other keys provided for this purpose, or an auto-stop condition occurs.

Depressing the start key resets those check indicators with corresponding switches set to AUTOMATIC, but does not reset indicators with corresponding switches set to PROGRAM.

When an instruction error (00900) occurs, and the switch (00900) is set to AUTOMATIC, the operator must manually correct the instruction or transfer to another instruction before restarting the machine.

When a machine error has occurred and its 00901 check switch is set to AUTOMATIC, the machine may stop before completely executing the instruction involving the error. Depressing the start key turns off the indicator, but an attempt to complete the instruction turns it on again at once. A correction must be made before operation can continue.

When a 00902, 00903, 00904, or 00905 error has occurred with associated switches set to AUTOMATIC, depressing the start key causes the machine to execute the next instruction. The indicator is reset off.

Stop (Back-lighted Key): Depressing the stop key causes the machine to stop after the current instruction has been executed and turns on the red backlight. This, rather than the machine stop key, is the normal way to halt machine operation. After the stop key is depressed, the machine remains in manual status and is ready to respond to any manual function or to start operation if the start key is depressed. Other keys (store, instruction, display, and half multi-step) also cause the machine to stop before their special function begins.

Half Multi-Step (Key): Depressing this key causes the machine to operate in half steps. For example, one depression causes the machine to read an instruction (I time). A second depression causes the machine to execute the instruction (E time). Indirect address time is also treated as a "half step." That is, an indirectly addressed instruction will be stepped through all three phases of its execution (I time, IA time, and E time) by three successive depressions of the key.

This feature can be helpful for investigating an error condition, program or otherwise. This feature allows the operator to "step" through a portion of the program in half steps to pinpoint the trouble area.

The displays and lights may be monitored during this stepping, to determine when an error occurs, and what caused it.

Interrupt time is also treated as a "half step." That is, if the interrupt time indicator is turned on following E time, the next depression will result in INT being executed. The key depression following that will put the machine in I time.

If the key is held depressed for more than three-fourths of a second, the machine alternately reads and executes instructions at the rate of about ten half-steps per second, as long as the key is held down. If the machine is in automatic status when the key is depressed, it stops after executing the current instruction. Depressing the start key causes the machine to enter automatic status, starting at the point where it stopped after the half multi-step key was last depressed.

Instruct (Back-lighted Key): The following procedure is used to instruct the machine manually:

1. Depress the instruct key. If the machine is in automatic status, it stops after the current instruction has been executed, exactly as if the stop key had been depressed.
2. Key the address part of the instruction in the memory address selector either before or after depressing the instruct key.
3. Key the desired storage unit in the storage selector, either before or after depressing the instruct key.
4. Key the operation part of the instruction in the keyboard. This final action causes the instruction to be executed.

NOTE: A 00900 check will occur if the program attempts to perform a 7080 instruction in any mode other than the 7080 mode, yet it is possible to perform a 7080 instruction manually, regardless of mode, and a 00900 check *will not* occur.

The machine remains in instruct status after completion of the instruction. Subsequent instructions may be keyed without further depressions of the instruct key. However, the storage selector, including bank, keys are automatically restored after each instruction execution, hence must be re-keyed.

Depressing the start key causes the machine to continue in automatic status from the point in the program where it entered instruct status unless one or more transfer instructions were executed under manual control.

Store (Back-lighted Key): The following procedure is used to store information manually in memory:

1. Depress the store key. If the machine is in automatic status, it stops after execution of the current instruction exactly as if the stop key had been depressed.

2. Key the memory location into the memory address selector where the first character (i.e., the highest order) is to be stored. (The order of 1 and 2 can be reversed.)

3. Key the characters to be stored into the keyboard. The first character is entered into memory at the location specified by the memory address selector. Successive characters are entered into successively higher address positions of memory.

After one or more characters have been stored, the operator may select another address on the memory address selector. The store key must be depressed a second time to place the next character in the memory location specified by the second setting of the memory address selector.

The store status continues (white back-light on) until superseded by another mode of operation.

Display (Back-lighted Key) and Display Step (Key): Depressing the display key when the machine is in automatic status causes the machine to stop as though the stop key had been depressed. In addition, it prepares the machine for reading a character from memory and from storage by subsequent depression of the display-step key.

The character read from memory is displayed in the memory character (MBR) lights in BCD code. If an invalid character is displayed, the MBR character check light is turned on but the error does not turn on the machine check indicator.

The first memory character displayed is the one located at the address specified by the memory address selector. Subsequent characters are displayed from successively lower memory positions by depressions of the display step key.

The character read from storage is displayed in the storage character (SBR) lights as a BCD character. If an invalid character is displayed, the SBR character check light is turned on but the error does not turn on the machine check indicator.

The first storage character displayed is the one located at the right-hand position of the storage unit selected by the storage selector switches. Successive characters to the left are displayed by additional depressions of the display step key. The bank of central storage is selected by the storage bank selector keys.

The position of the next memory character to be displayed in memory character lights is shown as the address of MAC I.

Depressing the display key after the display step key causes the next character to be displayed from the position specified by the memory address or storage selector keys. The display status continues (white back-light on) until superceded by another status.

Customer Engineer Panel Indicators

The customer engineer panel indicators are primarily for the use of customer engineers. These indicators assist in diagnosing machine performance by indicating the status of their related triggers. On an error condition, a notation of the status of these indicators can greatly assist the customer engineer in diagnosing the trouble.

The repeat and single-cycle keys are used in conjunction with the customer engineer indicators and test switch.

IBM 7502 Console Card Reader

The IBM 7502 Console Card Reader for the IBM 7080 Data Processing System is designed to handle small-volume punched card input at a modest cost when the 7080 is operated as a tape-oriented system.

The 7502 may be used to:

- Read calling cards which determine the sequence of loading operating programs from a master program tape
- Enter program patching cards
- Load sorting control cards
- Load small utility programs
- Process miscellaneous or late transactions
- Enter constant factors into memory
- Process data correction cards

IBM cards are read serially at a single read station, where punched holes are sensed photoelectrically. If none of the columns of the card contains a reader storage mark character (12-1-4-7), then columns 1 through 80 are read, checked, and stored in the 7080 memory. If a column containing the reader storage mark is encountered, then, neither that column, nor any of the following columns of that card will be stored in memory and no checking will be performed on these characters. Using the record storage mark character is the only means by which less-than-80 column record can be read into memory through the 7502 card reader. The column counter indicates how many columns passed the read station without error. Thus it usually stands at 80 after reading a card. Reading speed is 60 cards per minute. Cards may be punched in any arrangement of digits, letters of the alphabet, or special characters acceptable to the 7080. Columns may also be blank.

Each card column is translated directly into one corresponding BCD character. Translation and card registration are thoroughly checked. Unacceptable card punching or BCD coding are both treated as error conditions. When such an error is detected, the 00902 read-write and the ANY indicators in the 7080 are turned on and check lights on the 7502 display the

type of error encountered. The column counter locates the card column where the error occurred.

The 7502 operates under program control. It responds to any one select instruction with an address from 00100 to 00109 as determined by the assignment of an internally wired address in the reader. Reading, error checking, and end-of-file procedures are executed with the same program routines used with the IBM 714 Card Reader. However, the 7502 is a fixed-format device and is not equipped with a control panel. Therefore, such features as digit selection, record grouping, and character emitting are not available.

The 7502 is cable-connected to the 7153 Console and is conveniently located at the left of the card storage section of the 7153 Console.

Operating Features

The 7502 uses a modified IBM 24 Card Punch feed, transport mechanism, and stacker unit. As cards pass a reading station, the holes in each column are read by moving the card between a light source and twelve photoelectric cells, one for each of the twelve rows in the card (Figure 43). The resulting electrical impulses, column by column, are sent to a 12-to-6 translator where each card character is converted to a six-bit BCD character. The same impulses are also sent to a 12-to-1 translator where a check bit is generated for the corresponding BCD character. Each six-bit BCD character is then combined with its check bit. The completed character with check bit is sent to 7080 memory.

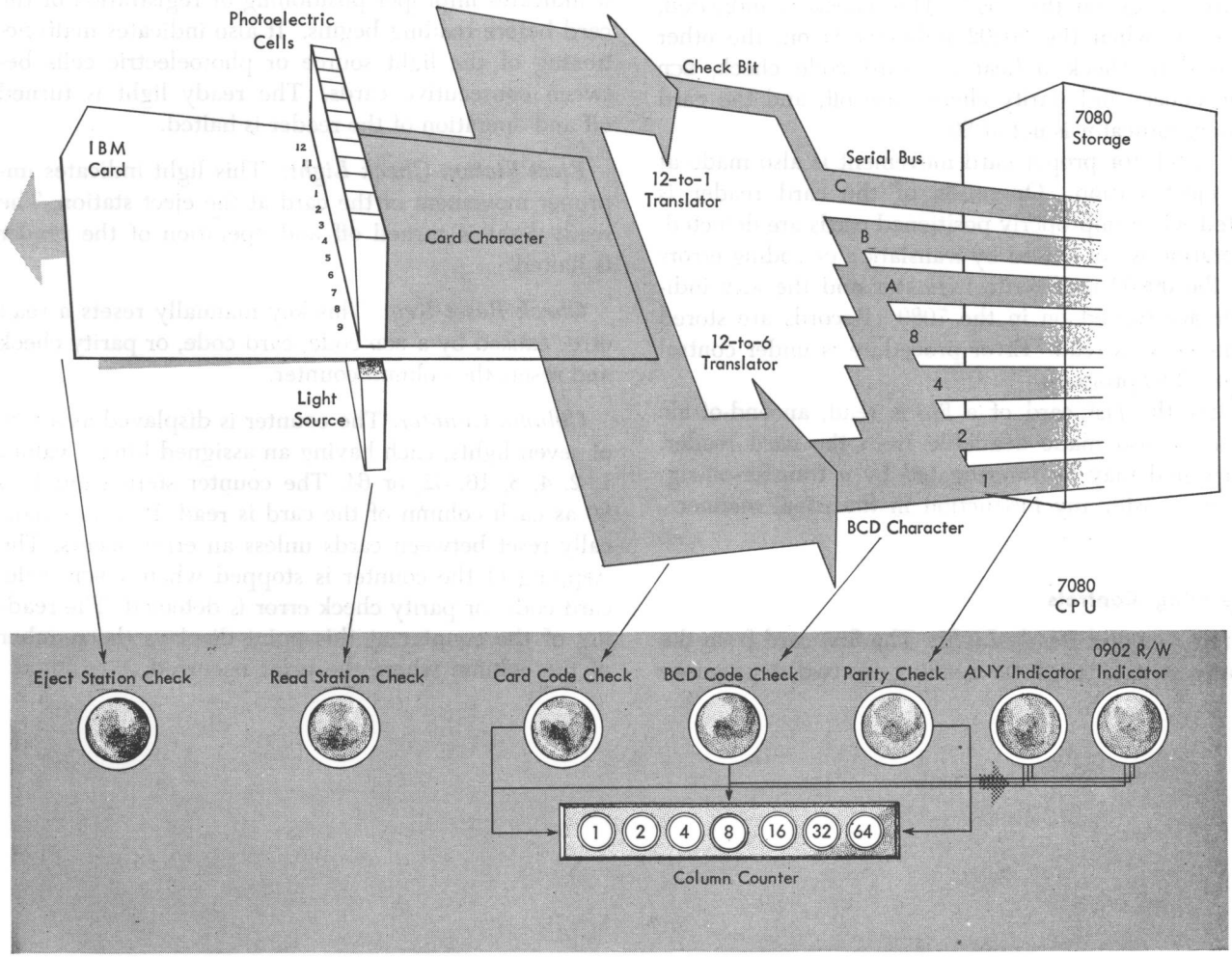


Figure 43. Data Flow and Checks, IBM 7502 Console Card Reader

Card punching is checked for unacceptable characters before translation, and each six-bit BCD character is checked for acceptability before it is combined with a check bit. Each completed character is given the normal parity check in the 7080.

As each card enters the read station, registration is checked by not sensing a hole in row 4 when the card is positioned at column 0. As the card leaves the read station, a check is also made to determine that the light source and photoelectric cells are functioning properly. Any potential reading failure due to these devices is thus immediately detected.

Another checking feature of the 7502 is the Response Check. This check insures that exactly 80 columns of the card are read. (With cards containing a reader storage mark, responses prior to the reading of the reader storage mark are counted, and column emitter pulses are counted before and after the record storage mark.) If more or less than 80 are indicated by the column counter, the read-write indicator (00902) is set.

There is no associated indicator light for the response check on the 7502. This check is indicated, however, when the 00902 indicator is on, the other three data check indicators (card code check, BCD code check, and parity check) are off, and the card column indicator is not at 80.

A check for proper card movement is also made at the eject station. Operation of the card reader is halted when improperly positioned cards are detected. Operation is not halted by translation or coding errors but the 00902 read-write indicator and the ANY indicator are turned on in the 7080. Records are stored in memory as read. Error procedure is under control of the 7080 program.

After the last card of a file is read, an end-of-file signal is also made available from the card reader. The signal may be interrogated by a transfer-on-signal or transfer-any instruction in the usual manner.

Operating Controls

Start Key and Ready Light: The first card from the hopper is positioned for reading by two depressions of the start key. The ready light is turned on to indicate that the card reader is ready for operation under program control.

Stop Key: Depressing the stop key turns off the ready light and removes the reader from 7080 program control.

Feed Key: When the ready light is off, this key provides a manual feed without reading cards. The key also turns off the read and eject station check lights.

Card Code Check Light: This light turns on when unacceptable card punching is detected in any column.

BCD Code Check Light: This light turns on when an unacceptable six-bit BCD character is detected.

Parity Check Light: This light turns on when a parity error is detected in a character sent to 7080 memory.

Read Station Check Light: When this light is on, it indicates improper positioning or registration of the card before reading begins. It also indicates malfunctioning of the light source or photoelectric cells between consecutive cards. The ready light is turned off and operation of the reader is halted.

Eject Station Check Light: This light indicates improper movement of the card at the eject station. The ready light is turned off and operation of the reader is halted.

Check Reset Key: This key manually resets a read error caused by a BCD code, card code, or parity check and resets the column counter.

Column Counter: The counter is displayed as a row of seven lights, each having an assigned binary value: 1, 2, 4, 8, 16, 32, or 64. The counter steps from 1 to 80 as each column of the card is read. It is automatically reset between cards unless an error occurs. The stepping of the counter is stopped when a BCD code, card code, or parity check error is detected. The reading of the counter at this point displays the number of the column where the error occurred.

Abbreviations for 7080

AAM	Add Address to Memory*
ACC	Accumulator
ADD	Add*
ADM	Add to Memory*
ALU	Arithmetic and Logical Unit
ART	Automatic Restart Trigger
ASU	Auxiliary Storage Unit
AWR	Address Word Register
BCD	Binary Coded Decimal
BLM	Blank Memory*
BLMS	Blank Memory Serial*
BSF	Backspace File*
BSP	Backspace*
CAR	Character Address Register
CASU	Channel Auxiliary Storage Unit
CHR	Channel Reset*
CMP	Compare*
CNO	Comma No Operation*
CPI	Characters Per Inch
CPU	Central Processing Unit
CRD	Control Read*
CTL	Control
CWR	Control Write*
CWS	Channel Word Set
DIV	Divide*
DMP	Dump Memory*
DR	Data Register
ECB	Enable Compare Backward*
EIA	Enable Indirect Address*
EIM	Enter Interrupt Mode*
EEM	Enter Eighty Mode*
FSP	Forward Space*
HLT	Stop*
IAR	Initial Address Register
IC	Instruction Counter
I-O	Input-Output
IOF	Turn Off I-O Indicator*
ION	Turn On I-O Indicator*
LDA	Load Address*
LEM	Leave Eighty Mode*
LFC	Load Four Characters*
LIM	Leave Interrupt Mode*
LIP	Leave Interrupt Program*
LNG	Lengthen*
LOD	Load
LSB	Load Storage Bank*
MAC I	Memory Address Counter I
MAC II	Memory Address Counter II
MAR	Memory Address Register
MAS	Memory Address Selector
MBR	Memory Buffer Register
MBR RECOG	Equivalent to 705 III CRI Recognition
MBR VRC	Equivalent to 705 III CRI Code Check
MDS	Memory Decode Switch
MPY	Multiply*
MPX	Multiplexor
NOP	No Operation*
NTR	Normalize and Transfer*
OP REG	Operation Register
RAD	Reset and Add*
RCV	Receive*
RD	Read*
RMA	Read Memory Address*
RMB	Read Memory Block*
RND	Round*
RR	Result Register
RSM	Record Storage Mark
RSU	Record Storage Unit
RSU	Reset and Subtract*
RUN	Rewind and Unload*
RWD	Rewind*
RWW	Read While Writing*
SAC	Storage Address Counter
SAS	Storage Address Switch
SAR	Storage Address Register
SBA	Set Bit Alternate*
SBN	Set Bit 1*
SBR	Set Bit Redundant*
SBR	Storage Buffer Register
SBR RECOG	Equivalent to 705 III CR2 Recognition
SBR VRC	Equivalent to 705 III CR2 Code Check
SBZ	Set Bit 0*
SCC	Set Control Condition*
SDH	Set Density High*
SDL	Set Density Low*
SEL	Select*
SEL REG	Select Register
SET	Set Left*
SHR	Shorten*
SGN	Sign*
SKP	Skip Tape*
SND	Send*
SPC	Set Starting Point Counter*
SPC	Starting Point Counter
SPR	Store for Printing*

SRC	Set Record Counter*
SSR	Storage Select Register
SST	Sense Status Triggers*
ST	Store*
SUB	Subtract*
SUP	Suppress Printing or Punching*
TAA	Transfer Switch A On*
TAB	Transfer Switch B On*
TAC	Transfer Switch C On*
TAD	Transfer Switch D On*
TAE	Transfer Switch E On*
TAF	Transfer Switch F On*
TAR	Transfer Auto Restart*
TAU	Tape Adapter Unit
TCT	Ten Character Transmit*
TEC	Transfer Echo Check*
TIC	Transfer Instruction Check*
TIP	Transfer to Interrupt Program*
TMC	Transfer Machine Check*
TMT	Transit*
TMTS	Transmit Serial*
TNS	Transfer Non-Stop*
TOC	Transfer Overflow Check*
TR	Transfer*
TRA	Transfer Any*
TRC	Transfer Read-Write Check*
TRE	Transfer on Equal*
TRH	Transfer on High*
TRP	Transfer on Plus*
TRR	Transfer Ready*
TRS	Transfer on Signal*
TRZ	Transfer on Zero*
TSA	Transfer Sync Any*
TSC	Transfer Sign Check*
TSL	Transfer and Store Location*
TTC	Transfer Transmission Check*
TZB	Transfer on Zero Bit*
UFC	Unload Four Characters*
ULA	Unload Address*
UNL	Unload*
USB	Unload Storage Bank*
VRC	Vertical Redundancy Check
WMC	Write Multiple Control*
WR	Write*
WRE	Write and Erase*
WTM	Write Tape Mark*

* These are all instructions.

Collating Sequence

blank . ¤ < ≠ & $ * - / , % # @ 0̇ A to I 0̄ J to R ≠ S to Z 0 to 9

Special Character Symbols, 7080—Fortran

Zone	Numeric	7080	Fortran
12	None	&	+
12	8-3	.	.
12	8-4	¤	)
11	None	—	—
11	8-3	$	$
11	8-4	*	*
0	8-3	,	,
0	8-4	%	(
None	8-3	#	=
None	8-4	@	'

7080 Instruction Variations

Instructions that may be given in 705 III or 7080 Mode

				ASU
Rewind and Unload	RUN	Ctrl	00002	01
Set Density Low	SDL	Ctrl	00037	
Set Density High	SDH	Ctrl	00038	
Channel Reset	CHR	Ctrl	xxxxx	13
Enable Compare Backward	ECB	Ctrl	xxxxx	12
Enter 7080 Mode	EEM	Ctrl	xxxxx	14
Leave 7080 Mode	LEM	Ctrl	xxxxx	15
Sense Status Trigger*	SST	RD	xxxxx	03
Control Read	CRD	RD	xxxxx	04
Read Memory Block	RMB	RD	xxxxx	05
Set Control Condition*	SCC	WR	xxxxx	03
Control Write	CWR	WR	xxxxx	04
Write Multiple Control	WMC	WR	xxxxx	05
Reset WTC Trigger*		SEL	06001	
Reset SAR 8 Trigger*		SEL	06002	
Transfer Non-Stop	TNS	TRA	xxxxx	07

Instructions that may be given only in the 7080 Mode

Transfer Auto Restart	TAR	TRS xxxx	09
Set Starting Point Counter	SPC	Comma	00
Load Four Characters	LFC	Comma	02
Unload Four Characters	UFC	Comma	03
Load Storage Bank	LSB	Comma	04
Unload Storage Bank	USB	Comma	05
Enter Interrupt Mode	EIM	Comma	06
Leave Interrupt Mode	LIM	Comma	07
Ten Character Transmit	TCT	Comma	08
Enable Indirect Address	EIA	Comma	10
Comma No Operation	CNO	Comma	11
Transfer to Interrupt Program	TIP	Comma	14
Leave Interrupt Program	LIP	Comma	15

* These four instructions are diagnostic instructions for the 7621 and are primarily for the use of the customer engineer.

SST: This instruction is used to bring the channel check error status-trigger settings into memory.

WR 03: This instruction will set a character into the diagnostic register to force errors.

SEL 06001: This instruction will cause a WTC error in the MPX.

SEL 06002: This instruction will cause a SAR 8 error in the MPX.

7080 Instruction Execution Times for All 7908 Data Channel Instructions

All times given by these formulas are the maximum, not the usual, CPU times involved (time in micro-seconds). N represents the number of characters in the record.

INSTRUCTION		CODE	TIME	
			Channels 44-47	*Channels 40-41*
Write	00	WR	13 + 8(N/5)	13 + 3(N/5)
	01	DMP	13 + 8(N/5)	13 + 3(N/5)
	03	SCC	13 + 8(N/5)	13 + 3(N/5)
	04	CWR	13 + 8(N/5)	13 + 3(N/5)
	05	WMC	13 + 8(N/5)	13 + 3(N/5)
Read	00	RD	10 + 8(N/5)	10 + 3(N/5)
	01	FSP	10 + 8(N/5)	10 + 3(N/5)
	03	SST	10 + 8(N/5)	10 + 3(N/5)
	04	CRD	10 + 8(N/5)	10 + 3(N/5)
	05	RMB	10 + 8(N/5)	10 + 3(N/5)
Transfer on Signal	00	TRS	3	3
	01	TRR	3	3
	02	TTC	3	3
	03*	TSA	3	3
Control	00037**	SDL		6
Control	00038**	SDH		6

*The time for TRS03 (TSA) assumes a ready condition on the channel at the time the instruction is issued.

** Controls 37 and 38 apply to channels 40 and 41 only.

7080 Mnemonic Codes

INSTRUCTION	MNEMONIC	CODE	PAGE
Add	ADD	G	38
Add Addr to Mem	AAM	@	46
Add to Mem	ADM	6	45
Blank Memory (BLM 00)	BLM	$	52
Blank Memory Serial (BLM 01)	BLMS	$	52
Comma 00 Set starting point counter	SPC	,	45
Comma 02 Load four characters	LFC	,	48
Comma 03 Unload four characters	UFC	,	49
Comma 04 Load storage bank	LSB	,	49
Comma 05 Unload storage bank	USB	,	49
Comma 06 Enter interrupt mode	EIM	,	64
Comma 07 Leave interrupt mode	LIM	,	64
Comma 08 Ten Character Transmit	TCT	,	54
Comma 10 Enable indirect address	EIA	,	64
Comma 14 Transfer to interrupt prog	TIP	,	62
Comma 15 Leave interrupt prog	LIP	,	63
Compare	CMP	4	54
Control 00000 Turn off I-O ind	IOF	3	65
Control 00001 Write tape mark	WTM	3	66
Control 00002 Rewind	RWD	3	66
Control 00002 (01) Rewind and unload	RUN	3	66
Control 00003 Turn on I-O ind	ION	3	66
Control 00004 Backspace	BSP	3	66
Control 00004 (01) Backspace file	BSF	3	66
Control 00005 Supp print or punch	SUP	3	66
Control 00009 Skip tape	SKP	3	66
Control xxxxx (12) Enable Compare Backward	ECB	3	55
Control xxxxx (13) Channel reset	CHR	3	66
Control xxxxx (14) Enter 7080 mode	EEM	3	67
Control xxxxx (15) Leave 7080 mode	LEM	3	67
Control 00037 Set density low	SDL	3	66
Control 00038 Set density high	SDH	3	66
Divide	DIV	W	40
Lengthen	LNG	D	44
Load	LOD	8	48
Load Address	LDA	#	49
Multiply	MPY	V	40
No Operation	NOP	A	64
No Operation, Comma (11)	CNO	,	65
Norm and Transfer	NTR	X	56
Read 00	RD	Y	67
Read 01 Forward space	FSP	Y	68
Read 02 Read memory address	RMA	Y	69
Read 03 Sense status trigger	SST	Y	72, 73
Read 04 Control Read	CRD	Y	73
Read 05 Read Memory Block	RMB	Y	74
Read while Writing	RWW	S	71
Receive	RCV	U	53
Reset and Add	RAD	H	37
Reset and Subtract	RSU	Q	39

INSTRUCTION	MNEMONIC	CODE	PAGE
Round	RND	E	44
Select	SEL	2	67
Select (Sel 06001 Reset WTC trigger)		2	72
Select (Sel 06002 Reset SAR 8 trigger)		2	72
Send	SND	/	51
Set Bit Alternate (SB 07)	SBA	%	60
Set Bit 1 (SB 09-14)	SBN	%	60
Set Bit Redundant (SB 08)	SBR	%	60
Set Bit 0 (SB 01-06)	SBZ	%	60
Set Left	SET	B	42
Shorten	SHR	C	43
Sign	SGN	T	47
Stop	HLT	J	65
Store	ST	F	45
Store for Print	SPR	5	51
Subtract	SUB	P	39
Transfer	TR	1	57
Transfer Auto Restart (TRS 09)	TAR	O	60
Tr Sw A On (00911) (TRA 01)	TAA	I	58
Tr Sw B On (00912) (TRA 02)	TAB	I	58
Tr Sw C On (00913) (TRA 03)	TAC	I	58
Tr Sw D On (00914) (TRA 04)	TAD	I	58
Tr Sw E On (00915) (TRA 05)	TAE	I	58
Tr Sw F On (00916) (TRA 06)	TAF	I	58
Tr Nonstop (TRA 07)	TNS	I	58
Tr and Store Location Ctr (Tr 01)	TSL	1	57
Tr Any	TRA	I	58
Tr Read-Write Check (TR 12)	TRC	O	60
Tr on Equal	TRE	L	56
Tr on High	TRH	K	55
Tr Instr Check (TRS 10)	TIC	O	60
Tr Machine Check (TRS 11)	TMC	O	60
Tr O'flow Check (TRS 14)	TOC	O	60
Tr on Plus	TRP	M	57
Tr Ready (TRS 01)	TRR	O	59
Tr Echo Check (TRS 13)	TEC	O	60
Tr Sign Check (TRS 15)	TSC	O	60
Tr on Signal	TRS	O	59
Tr Sync Any (TRS 03)	TSA	O	59
Tr Transmission Check (TRS 02)	TTC	O	59
Tr on Zero	TRZ	N	57
Tr on Zero Bit	TZB	.	62
Transmit	TMT	9	53
Transmit Serial (TMT 01-15)	TMTS	9	53
Unload	UNL	7	48
Unload Address	ULA	*	50
Write 00	WR	R	69
Write 01 (Dump memory)	DMP	R	70
Write 02 (Set record counter)	SRC	R	70
Write 03 (Set control condition)	SCC	R	73
Write 04 Control Write	CWR	R	74
Write 05 Write Multiple Control	WMC	R	74
Write and Erase 00	WRE	Z	71
Write and Erase 01	WRE	Z	71

NOTE: Control 00000-00038 all display CTL mnemonic; TRA 00-07 all display TRA; TRS 00-15 all display TRS.

7080 Instruction Execution Time

The following formulas can be used to compute the time required to execute the instructions on the 7080 (time in microseconds).

The symbols used in the formulas are defined as follows:

- A One cycle if the address of the instruction ends in a 0 or 5.
- B_m Number of memory boundaries crossed. Memory boundaries exist between memory addresses ending in 9 or 0 and between those ending in 4 or 5.
- B_s Number of storage word boundaries crossed.
- C_s One cycle if a carry is made into zones.
- N Number of characters.
- N_m Number of characters in memory field.
- $|N_m|$ Absolute value of quantity in memory field (magnitude without regard to sign).
- N_s Number of characters in a storage field.
- $|N_s|$ Absolute value of quantity in storage field (magnitude without regard to sign).
- N_a Address of instruction.
- N_p Number of periods or commas skipped.
- N_b Number of zeros or commas replaced by blanks.
- N_h Number of characters in the shorter of the two fields.
- Z Number of zeros in low-order positions of storage field.

For all instructions, an indirect address requires an additional two cycles.

INSTRUCTION	CODE	TIME (CYCLES)	REMARKS
Add	ADD	$6 + N_m + B_s$	Mem and stor signs alike (see note A)
			Mem and store signs unlike
		$6 + N_m + B_s$	$\|N_m\| \geqq \|N_s\|$ (see note A)
		$9 + 2N_m + 2B_s$	$\|N_m\| < \|N_s\|$ (see note A)
Add Addr to Mem	AAM	20	$\|N_m\| + \|N_s\| \geqq 100{,}000$
		18	$100{,}000 > \|N_m\| + \|N_s\| \geqq 10{,}000$
		13	$10{,}000 > \|N_m\| + \|N_s\| \geqq 0$
Add to Mem	ADM	$7 + N_h + 3B_m$	Signed mem field, mem and stor signs alike (see note A)
		$7 + N_b + 3B_m$	Mem and stor signs opposite, $\|N_m\| \geqq \|N_s\|$
		$11 + 2N_m + 6B_m$	Mem and stor signs opposite, $\|N_m\| < \|N_s\|$ (see note A)
		$7 + N_s + 3B_m + C_s$	Unsigned memory field
Blank memory	BLM 00	$4 + 2(N/5)$	Stor sel reg = 0 (Acc)
	BLM 01	$4 + 4N$	Stor sel reg ≠ 0 (ASU)
Comma 00	SPC	3	
Comma 02	LFC	$8 + B_s$	Address ending in 4 or 9
Comma 03	UFC	9	
Comma 04	LSB	291	
Comma 05	USB	413	
Comma 06	EIM	3	
Comma 07	LIM	3	
Comma 08	TCT	$2 + 4\,(4/10)$	See note B
Comma 10	EIA	3	
Comma 11	CNO	3	
Comma 14	TIP	6	
Comma 15	LIP	9	
Compare	CMP	$5 + N_s + A$	
Control 00000	IOF	8	
Control 00001	WTM	8	
Control 00002	RWD	30275 (33 ms)	
Control 00003	ION	8	
Control 00004	BSP	8	
Control 00004(01)	BSF	8	
Control 00005	SUP	5504 (6 ms)	
Control 00009	SKP	8	
Control 00037	SDL	5504 (6 ms)	
Control 00038	SDH	5504 (6 ms)	
Control (12)	ECB	3	Stor sel reg = 12
Control (13)	CHR	3	" " " = 13
Control (14)	EEM	3	" " " = 14
Control (15)	LEM	3	" " " = 15
D Divide	DIV	$18 + N_s + N_m + 44\,(N_s - N_m)$	Average formula
Load	LOD	$5 + N_s + B_s + A$	
Lengthen	LNG	$6 + N_a + 2B_s$	
Load Address	LDA	14	7080 mode
		12	Not 7080 mode
Multiply	MPY	$5 + (12 + 1.4N_m)N_s$	Average formula
No Operation	NOP	3	

INSTRUCTION	CODE	TIME (CYCLES)	REMARKS
Norm and Tr	NTR	$7 + N_s$	All cases except single zero field
		5	Single zero field
Read	RD 00	$8 + 8(N/5)$	From tape to mem through chan (see note B)
		$5 + 31N$	From card reader to memory
	RD 01	$8 + 7(N/5)$	Stor sel reg = 1 (see note B)
	RD 02	7	Stor sel reg = 2
Read while Writing	RWW	14	
Receive	RCV	3	
Reset Add	RAD	$6 + N_m + B_s$	
Reset Subtract	RSU	$6 + N_m + B_s$	
Round	RND	$9 + N_a + B_s$	See note A
Select	SEL	6	Systems without 7622 control.
		14	Systems with 7622 control.
Send	SND	$4 + 4(N/5)$	
Set Left	SET	$5 + N_a + B_s$	
Set Bit	SB	6	
Sign	SGN	$8 + B_s$	
Shorten	SHR	$6 + N_a + Z$	
Stop	HLT	3	
Store	ST	$6 + N_s + 3B_m$	
Store for Print	SPR	$9 + N_s + 2N_p + 4N_b + 3B_m$	
Subtract	SUB	$6 + N_m + B_s$	Mem and stor signs opposite*
			Mem and stor signs alike
		$6 + N_m + B_s$	$\lvert N_m\rvert \geqq \lvert N_s\rvert$ (see note A)
		$9 + 2N_m + 2B_s$	$\lvert N_m\rvert < \lvert N_s\rvert$ (see note A)
Transfer	TR 00	3	Stor sel reg = 0
	TR 01	9	" " " = 1
Transfer Any	TRA	3	
Transfer Equal	TRE	3	
Transfer High	TRH	3	
Transfer Plus	TRP	3	
Transfer on Signal	TRS	3	
Transfer Zero	TRZ	3	
Transfer Zero Bit	TZB	5	
Transmit	TMT 00	$2 + 4(N/5)$	Stor sel reg = 0
	TMT 01	$4 + 6N$	Stor sel reg $\neq$ 0
Unload	UNL	$6 + N_s + 3B_m$	
Unload Address	ULA	20	$\lvert N_s\rvert \geqq$ 100,000
		18	100,000 $> \lvert N_s\rvert \geqq$ 10,000
		13	10,000 $> \lvert N_s\rvert \geqq 0$
Write	WR 00	$8 + 8(N/5)$	From mem to tape via channel (see note B)
		$5 + 31N$	From mem to punch or printer
	WR 01	$8 + 8(N/5)$	From mem to tape via channel (see note B)
		$5 + 31N$	From mem to punch or printer
	WR 02	8	
Write Erase	WRE 00-01	Not to be used	From mem to tape via channel
		$5 + 31N$	From mem to punch or printer

* Depending on the particular integers involved, extra cycles for "carry" situations can occur while performing these classes of arithmetic. However, the timing effect of such "carries" is insignificant, and hence dropped from the formulas.

** The formulas for reading and writing through a communication channel represent the total number of CPU cycles required. Hence, they give the maximum (not the usual) amount of CPU time involved in the execution of a read or write operation. During reading or writing through a channel, transfers of individual characters from tape to communication storage (one cycle per character) and transfers of five characters from storage to memory (three cycles per group) may occur during instruction execution in such a way that the cycles are completely overlapped, or they may temporarily interrupt the processing of an instruction.

IBM 7080 Mode Chart

MODE OF 7080 OPERATION	METHOD OF ENTERING MODE	NATURE OF MODE	METHOD OF TERMINATING MODE
705 I-II	If the console 705 I-II compatibility switch is set to ON, this mode may be established by any of the following operations: 1. Depression of the console clear-memory, auto-load or reset keys. 2. Execution of the LEM instruction. 3. Execution of the LIP instruction if the 7080 mode indicator bit in CASU 15 is a zero. 4. An automatic interrupt if the 7080 mode indicator bit in the interrupt word or in word 0 of the channel word set is a zero.	1. Programs written for a 705 I or II may be processed without alteration at the increased speed of the 7080. 2. 705 I and II input-output units required by a program must be connected to the central processing unit through the 7622 signal control unit. 3. Transfer instructions which are not in the 705 I and II are not active. All transfer instructions will function exactly as they do in a 705 I or II. 4. The indirect method of addressing of the 705 III does not apply. Zoning over the units position of an instruction address is ignored. 5. Operations such as add, subtract, and add to memory are terminated in the same manner as in the 705 I or II. 6. The size of memory available to the program is restricted to 20,000 positions, and wrap-around of MAC I, MAC II, and the instruction counter will be at 20,000, if the console 40K memory size switch is off. If this switch is on, 40,000 positions will apply. 7. Communication channels may not be selected.	1. Setting the console 705 I-II switch to OFF. 2. Execution of the EEM instruction. 3. An automatic interrupt if the 7080 mode indicator bit in the interrupt word or in word 0 of the channel word set is a 1.
705 III	If the console 705 I-II compatibility switch is set to OFF, this mode may be established by any of the following operations: 1. Depression of the console clear-memory, auto-load or reset keys. 2. Execution of the LEM instruction. 3. Execution of the LIP instruction if the 7080 mode indicator bit in CASU 15 is a zero. 4. An automatic interrupt if the 7080 mode indicator bit in the interrupt word or channel word set is a zero.	1. Programs written for a 705 III may be processed without alteration at the increased speed of the 7080. 2. 705 III input-output units required by a program, with the exception of the 767 data synchronizer and 729 I or III tape units, must be connected to the central processing unit through the 7622 signal control unit. The 767 DS and 729 I or III tape units may not be attached to the 7080. Their action is simulated by communication storage, a communication channel, a 7621 tape control and 729 II or IV tape units. 3. All instructions which are provided in a 705 III will function exactly as if they were executed by a 705 III. 4. Indirect addressing is designated by an A bit over the units position of an instruction address. 5. The size of memory available to the program is restricted to 80,000 positions, and wrap-around of MAC I, MAC II, and the instruction counter will be at 80,000, if the console 40K memory size switch is off. If this switch is on, 40,000 positions will apply.	1. Setting the console 705 I-II switch to ON. 2. Execution of the EEM instruction. 3. An automatic interrupt if the 7080 mode indicator bit in the interrupt word or in word 0 of the channel word set is a 1.
7080	1. Execution of the EEM instruction. 2. An automatic interrupt if the 7080 mode indicator bit in the interrupt word or in word 0 of the channel word set is a 1.	1. All the features of 705 systems are available to the program together with the additional features of the 7080. 2. All comma operation codes are operable as well as the transfer to automatic restart (TAR) instructions. 3. The A bit in the units position of an instruction address specifies the memory locations 80,000 to 159,999, not indirect addressing. 4. The address modification instructions (LDA, ULA, AAM) automatically handle the six-digit addresses of the 160,000 position memory. 5. The 7080 mode of input-output addressing becomes applicable to all SEL instructions that refer to 7621 communication channels. The thousands and hundreds positions of the address identify the communication channel (20-24). The tens position must be zero. The units position identifies the tape unit number. 6. The size of memory available to the program is 160,000 positions for the 7302 Model 1 and 80,000 positions for the 7302 Model 2, regardless of the setting of the console memory size switch. Wrap-around of MAC I, MAC II, and the instruction counter will *always* be at 160,000.	1. Depression of the console clear-memory, auto-load or reset keys. 2. Execution of the LEM instruction. 3. Execution of the LIP instruction if the 7080 mode indicator bit in CASU 15 is a zero. 4. An automatic interrupt if the 7080 mode indicator bit in the interrupt word or in word 0 of the channel word set is a zero.

MODE OF 7080 OPERATION	METHOD OF ENTERING MODE	NATURE OF MODE	METHOD OF TERMINATING MODE
Interrupt	1. Execution of the EIM instruction.	An interrupt signal is caused either by the completion of a communication channel operation or by an interrupt word condition. With the following exceptions, this signal will initiate an automatic interrupt of the program at the completion of the instruction then in progress. 1. An interrupt may not occur after an EIA instruction. A signal received during the execution of this instruction will be delayed until the subsequent instruction is completed. If OP check occurs, then interrupt will occur. 2. An interrupt may not occur between a RWW instruction and a subsequent RD, WR, or SND instruction. A signal received in this interval will be delayed until the subsequent RD, WR, or SND instruction is completed. 3. If the machine is in an interrupt program, that is, if an automatic interrupt has been made or a TIP instruction has been executed, no interrupts may occur until the completion of a subsequent LIP instruction. A signal received in this interval will be delayed until the subsequent LIP instruction is completed. An exception is the non-stop interrupt signal to interrupt word 250. Except for auto restart, a condition that would produce a 250 interrupt if the machine were in main program status will cause the machine to stop if the condition occurs in interrupt program status. 4. An interrupt cannot occur between an ECB instruction and a subsequent CMP instruction. A signal received during the execution of this instruction is delayed until the subsequent CMP instruction is completed.	1. Depression of the console clear-memory, auto load or reset key. 2. Execution of the LIM instruction.
Non-stop	1. Setting the console non-stop switch to ON	1. The machine should always be in the interrupt mode. 2. If the machine is in the main program, the following conditions will not cause a stop, but will initiate an automatic interrupt to interrupt word 250: A halt instruction. A condition which turns on a 0900-0905 check indicator with the corresponding switch set to AUTOMATIC. A condition which turns on the automatic restart indicator.	1. Setting the console non-stop switch to OFF.

CPU Instruction Operation Chart, Internal Differences Among the 705 I and II, III, and 7080

INST	CODE	705 I AND II	705 III	7080	PROGRAMMER'S NOTES
All inst		Ignores zoning in units position.	The B bit in units position indicates upper 40K (except LNG, RND, SEL, SET, SHR). The A bit in units position indicates indirect addressing. If the A bit is present, all instructions including NOP must have a 4 or 9 in the numerical portion of the units position.	80 Mode: The A bit in units position indicates upper 80K memory positions. III Mode: same as 705 III. I & II Mode: same as 705 I & II.	
ADD	G	Execution not completed until end of both memory and storage field is reached.	Execution terminates no later than at the end of the storage or memory field, whichever is longer; but could terminate sooner, depending on carry requirements, at or after the end of the memory field.	80 & III Mode: same as 705 III. I & II Mode: same as 705 I & II.	When operating like a 705 I & II, it is possible to strip zoning from an entire storage field by subtracting a zero (additions involving like signs can produce an overflow condition). When operating like a Model III or 7080, the following results: Add: Storage aABCD + Memory b$\bar{0}$ Result aAB34 + In order to strip zoning from the entire storage field when operating like a Model III or 7080, it is necessary to subtract a field of zeros equal in length to (or one character less than) the storage field. For example: Add: Storage aABCD + Memory b 0 0 0 $\bar{0}$ Result a 1 2 3 4 +
ADM	6	Execution of ADM to signed memory field is completed at end of memory field.	Execution of ADM to a signed memory field terminates no later than at the end of the memory field; but could terminate sooner, depending on carry requirements, at or after the end of a shorter storage field.	All Modes: same as 705 III.	

INST	CODE	705 I AND II	705 III	7080	PROGRAMMER'S NOTES
CMP	4		Internal checking of the compare indicators may cause a 00901 check.	All modes: same as 705 III.	
NOP	A		When using a NOP instruction as a constant, observe that if the A bit is present in the units position, the numerical portion must be a 4 or 9.	III Mode: same as 705 III.	
RND	E	If the 5 is added to a position containing a storage mark, the 5 is placed in the accumulator at this point, but a storage mark is placed at the position of the starting point counter. Thus, the result has a zero field length, and the zero indicator is turned on.	The 5 is handled in the same way as in the 705 I & II, with the exception that the zero indicator is not turned on.	Same as 705 III.	
ST	F	Alphabetic characters may cause redundancies upon being stored, but do not cause 00901 check indication until used in subsequent operations. The units position normally does not cause a redundancy because a new C bit is generated for it.	The character in the units position is handled as in 705 II. In other positions, alphabetic characters may cause redundancies upon being stored and in any case cause an immediate 00901 check.	The character in the units position is handled as in the 705 II and III. In other positions, alphabetic characters may cause redundancies upon being stored, and only if this is so does it cause 00901 check, which, of course, is immediate.	The storing of alphabetic characters is sometimes used during 705 I and II program testing to create redundancies. For example: LOD 00(JK) ST 00 2001 SEL 0200 WR 2000 (00901 and 00902 check indication) On the 705 III and 7080, an immediate 00901 occurs when storing the alphabetic character J, but not the K; SBR (set bit redundant) is used to obtain a redundancy.
SUB	P	Same as ADD.	Same as ADD.	Same as ADD.	

INST	CODE	705 I AND II	705 III	7080	PROGRAMMER'S NOTES
TR	1	TR(00-15) = unconditional transfer.	TR00=unconditional transfer. TR01 = TSL (transfer store location). TR(02-15) = unconditional transfer.	Same as 705 III.	
TRA	I	TRA(00-15) transfers if ANY trigger is on.	TRA(00) = TR if ANY trigger is on. 01 = TAA = SEL 00911, TRS----- 02 = TAB = SEL 00912, TRS----- 03 = TAC = SEL 00913, TRS----- 04 = TAD = SEL 00914, TRS----- 05 = TAE = SEL 00915, TRS----- 06 = TAF = SEL 00916, TRS----- (07-15) = NOP	Same as 705 III, except: TRA 07 = TNS = TR if nonstop switch ON (III & 80 Mode) = NOP(I & II Mode).	
TRS	0	TRS 00 = TR if selected unit I/O indicator is on. TRS 01 — 15 = TR if selected tape exists on the 754/777, and if the ready light is on, and if tape is not rewinding. TRS 01 — 15 = NOP if the selected tape does not exist on the 754/777, or if the unit has not been placed in ready status, or if the unit is in the process of rewinding.	TRS 00 = TR if I/O indicator is on. TRS 01 = TR Ready (TRC or DS). TRS 02 = TR if DS data check indicator (PCT) is on. TRS 03 = TSA TRS 04-09 = NOP TRS 10 = TIC = SEL 00900, TRS----- TRS 11 = TMC = SEL 00901, TRS----- TRS 12 = TRC = SEL 00902, TRS----- TRS 13 = TEC = SEL 00903, TRS----- TRS 14 = TOC = SEL 00904, TRS----- TRS 15 = TSC = SEL 00905, TRS-----	See: CPU Instruction Operation Chart, Differences Between the 705 I and II, III, and 7080, with I/O Devices.	

INST	CODE	754 TAPE CONTROL and 760 CONTROL AND STORAGE		777 TAPE RECORD COORDINATOR		767 DATA SYNCHRONIZER	7621 TAPE CONTROL UNIT (7080)
		705 I and II	705 III/7080	705 I and II	705 III/7080	705 III	Addressable only when in 705 III or 7080 Mode
BSP	3	BSP(00-15)=BSP00	No change.	BSP(00-15)=BSP00	No change.	BSP00=BSP00 BSP01=BSF (backspace file) BSP(02-15)=BSP00	BSP00=BSP00 BSP01=BSF (backspace file) BSP(02-15)=BSP00
						When executing a BSP 01 instruction, the 767 DSU (on the 705 III) and the 7621 TCU (on the 7080) recognize any single-character record as a tape mark; therefore, the programmer should verify the tape mark by following any BSP 01 instruction with an IOF, then FSP and check for end-of-file.	
RD	Y	00902 indicates error when reading.	No change.	00902 indicates error when reading.	No change.	RD00=RD00 RD01 = FSP (forward space) RD02=RMA (read memory address) RD(03-15)=RD00	RD00=RD00 RD01=FSP (forward space) RD02 = RMA (read memory address) RD03=SST (sense status triggers) RD(04-15)=RD00
						1. Units position of the read address must be 0 or 5. If not, the instruction is automatically converted to FSP (RD01), the DS check indicator is turned on, and the machine will STOP at end of execution time. No characters enter memory.	1. Units position of the read address must be 0 or 5. If not, the instruction is automatically converted to FSP (RD01), the channel check is turned on, and no stoppage takes place unless programmed to do so. No characters enter memory.
						2. RD does not turn on 00902 or the ANY indicator, instead the data check or channel check indicator is turned on. No stop occurs.	
						3. Characters enter memory in blocks of five. If there are insufficient characters on tape to fill the last block, group marks are generated to fill the block.	

INST	CODE	754 TAPE CONTROL and 760 CONTROL AND STORAGE		777 TAPE RECORD COORDINATOR		767 DATA SYNCHRONIZER	7621 TAPE CONTROL UNIT (7080)
		705 I and II	705 III/7080	705 I and II	705 III/7080	705 III	Addressable only when in 705 III or 7080 Mode
						4. An RD00 instruction which has not been completed on reaching memory position 39,999 on a 40K memory, or 79,999 on an 80K memory, is automatically converted to a FSP (RD01) for the remainder of the operation, and turns on the PCT data check indicator. SMAC wraps around at 80,000 whether the memory is 40K or 80K.	4. An RD00 instruction which has not been completed on reaching certain memory boundaries causes the data memory address to wrap around to 00,000 and causes a channel check with conversion from RD00 to RD01, as follows: a. III Mode, 40K Switch ON: 39,995 159,995 b. III Mode, 40K Switch OFF: 79,995 159,995 c. 80 Mode (memory switch ignored): 159,995 The machine can change from mode to mode midway in an RD operation, without disturbing the normal completion of the RD, except that new memory boundaries now apply. It is the mode which prevails at the instant the data crosses the boundary, that determines which boundary applies. On a 7080 equipped with only an 80K memory, the instruction addresses can range all the way to 160K (hence the above boundary restrictions apply), but the memory executes all instructions so as to fall within the bounds of 0 and 80K.
						5. If two or more consecutive RD02 instructions are directed against the same DSU, only the first RD02 places a valid SMAC address in memory, thereafter SMAC takes on the address portion (plus 5) of the previous RD02 instruction.	5. If two or more consecutive RD02 instructions are directed against the same channel, the contents of SMAC are valid and unchanged. 6. The RD03 instructions, unlike the other RD instructions, does not reset the channel check indicators on the 7621.

INST	CODE	754 TAPE CONTROL and 760 CONTROL AND STORAGE		777 TAPE RECORD COORDINATOR		767 DATA SYNCHRONIZER	7621 TAPE CONTROL UNIT (7080)
		705 I and II	705 III/7080	705 I and II	705 III/7080	705 III	Addressable only when in 705 III or 7080 Mode
RWW	S	No change.		No change.		RWW initializes MAC II and turns on RWW trigger. a. Any subsequent WR causes the DS and the CPU to hang up in automatic status. b. Any subsequent RD operates as a normal RD, ignoring the RWW trigger. c. Any subsequent SND performs the normal check of memory, and resets the RWW trigger.	RWW initializes MAC II and turns on the RWW trigger. Any subsequent RD or WR operates as a normal RD or WR, ignoring the RWW trigger. Any subsequent SND performs the normal checking of memory, and resets the RWW trigger. RWW blocks interrupts until execution of a subsequent RD, WR or SND instruction.
TRA	I	TRA(00-15)=TR if ANY indicator is on.	TRA00=TR if ANY indicator is on. TRA(01-15) See: CPU Instruction Operation Chart, Internal Differences Between the 705 I and II, III, and 7080.	TRA(00-15)=(same as for 754 and 760)	TRA00=(same as for 754 and 760). TRA(01-15) See: Chart, Internal Differences.	The ANY indicator is not affected by DS or 7621 operation. See the TRS instructions below.	
TRS	O	TRS00 = TR if selected unit I/O indicator is on. TRS(01-15)=TRR See: Chart, Internal Differences.	TRS00=TR if selected I/O indicator is on. TRS01=NOP on 760, TRR on 754/777 TRS02=NOP TRS03=NOP TRS(04-09)=NOP TRS10=TIC=SEL 00900, TRS- - - - TRS11=TMC=SEL 00901, TRS- - - -	TRS00=TRS00 TRS01=TRR TRS(02-15)=TRR	TRS00=TRS00 TRS01=TRR TRS02=NOP TRS03=NOP TRS(04-09)=NOP TRS(10-15)=(same as for 754 and 760)	TRS00=TRS00 TRS01=TRR=TR *if* ready. TRS02=TTC=TR if data check (PCT) is on. TRS03=TSA=wait until ready, then TTC and TRS00 (see NOTE). TRS(04-09)=NOP TRS(10-15)=(same as for 754-760)	TRS00=TRS00 TRS01=TRR=TR *if* ready. TRS02=TTC=TR if channel check is on. TRS03=TSA=wait until ready, then TTC and TRS00 (see NOTE). TRS(04-08)=NOP TRS09=TAR=TR if auto restart ind is on. TRS(10-15)=(same as for 705 III)

INST	CODE	754 TAPE CONTROL and 760 CONTROL AND STORAGE		777 TAPE RECORD COORDINATOR		767 DATA SYNCHRONIZER	7621 TAPE CONTROL UNIT (7080)
		705 I and II	705 III/7080	705 I and II	705 III/7080	705 III	Addressable only when in 705 III or 7080 Mode
			TRS12=TRC=SEL 00902, TRS- - - - - TRS13=TEC=SEL 00903, TRS- - - - - TRS14=TOC=SEL 00904, TRS- - - - - TRS15=TSC=SEL 00905, TRS- - - - -			A series of 705 I and II instructions such as: 00204 SEL 00604 00209 TRR 00219 00214 TR - - - - - 00219 WR (≠) 00224 TRA - - - - - may be replaced in 705 III or 7080 systems by using TSA: 00204 SEL 00200 00209 TSA - - - - - NOTE: The TSA holds up all CPU operations until the DS or 7621 is ready, then a TR is executed only if the tape unit I/O indicator is on, or the data check (or channel check) indicator is on. The TRR, TTC and TSA instructions do not turn off any of the DS or 7621 indicators. The ANY indicator is never involved in DS or 7621 operations. The TRS and TTC instructions, if given while the DS or 7621 is reading or writing, test the appropriate indicator as it stands at that moment. These instructions are normally given after a TRR loop, a TSA, or an automatic interrupt.	
WR	R	WR00=WR00	WR00=WR00	Same as 754	Same as 754.	WR00=WR00 WR01=DMP(dump) WR02=SRC (set record counter) WR(03-15)=WR00	WR00=WR00 WR01=DMP(dump) WR02=SRC(set record counter), usable only when *not* in interrupt mode. WR03=SCC (set control condition), for use only by Customer Engineer, otherwise will "hang" in automatic. WR(04-15)=WR00
		WR01 writes through the respective memory block; i.e., 19998 or 39998. If addressed to 19999 on 20K system, or to 39999 on 40K system, only one character is written.	WR01 writes through the respective memory block; i.e., 19998, 39998, 59998, or 79998. On 40 K system, WR (01) 39999 causes one character to be written. On 80K, WR01 39999 causes writing up to 59998, while WR01 79998 causes one character to be written.	Same as 754	Same as 754.	1. Units position of a WR address must be 0 or 5. If not, the data check (705 III) or channel check (7080) indicator is turned on, and an address ending in 4, 5, 6, or 7 is treated as ending in 5. Address ending in a 0, 1, 2, 3, 8, or 9 is treated as ending with 0. 2. A WR00 instruction that has not been completed on reaching memory position 39,999 on a 40K memory, or 79,999 on an 80K memory, turns on the PCT data check indicator, but continues until the group mark is sensed.	2. A WR00 instruction that has not been completed on reaching certain memory boundaries causes the data memory address to *wrap around* to 00,000, and causes a channel *check* as follows: a. III Mode, 40K Switch ON: 39,995 159,995

INST	CODE	754 TAPE CONTROL and 760 CONTROL AND STORAGE		777 TAPE RECORD COORDINATOR		767 DATA SYNCHRONIZER	7621 TAPE CONTROL UNIT (7080)
		705 I and II	705 III/7080	705 I and II	705 III/7080	705 III	Addressable only when in 705 III or 7080 Mode
							b. III Mode, 40K Switch OFF: 79,995 159,995 c. 80 Mode (memory switch ignored): 159,995 The machine can change from mode to mode midway in a WR operation, without disturbing the normal completion of the WR; however, new memory boundaries now apply. It is the mode which prevails at the instant the data crosses the boundary, that determines which boundary applies. On a 7080 equipped with only an 80K memory, the instruction addresses can range all the way to 160K (hence the above boundary restrictions apply), but the memory executes all instructions so as to fall within the boundaries of 0 and 80K.
						3. The WR01 operation differs on the 7080 and the 705 III in the ending address of the address word of the 7080 and the address of SMAC for the 705 III. The address in the 7080 will be ten positions higher than that of SMAC for the 705 III. For example: if the last group of five characters written is 19,995 through 19,999, the address word is set at 20,010; the SMAC address would be set at 20,000. Or, if the 7080 is operating in the 705 III mode with the 40K switch on and the last group of five characters written is 39,995 through 39,999, the address word is set at 00010; the 705 III SMAC address would be set at 40,000.	
		WR(02-15)=WR01	No change.			4. WR01 writes through 19,999 or 39,999 or 59,999, etc., whichever quadrant is addressed. If a WR01 is given following an SRC instruction, then as many blocks of memory are written as the number set in the record counter of the selected DS or 7621 channel. If the RC is not zero when the end of memory is reached, writing continues at the beginning of memory until the RC is zero.	

INST	CODE	754 TAPE CONTROL and 760 CONTROL AND STORAGE		777 TAPE RECORD COORDINATOR		767 DATA SYNCHRONIZER	7621 TAPE CONTROL UNIT (7080)
		705 I and II	705 III/7080	705 I and II	705 III/7080	705 III	Addressable only when in 705 III or 7080 Mode
		WR(≠)=NOP, but turns on appropriate 00902, 00903, or ANY indicators if the 760 has detected an error or EOF in its last operation.		WR(≠)=NOP, but turns on appropriate 00902, 00903, or ANY indicators if the TRC has detected an error or EOF in its last operation.	No change.	5. WR (≠)=NOP. The DS or 7621 indicators are not affected. Furthermore, the 00902, 00903 and ANY indicators are not affected.	
		00901, 00902, 00903 are turned on as appropriate.		00901, 00902, 00903 are turned on as appropriate.	No change.	6. WR does not turn on 00901, 00902, 00903, or ANY indicators, instead the data check or channel check indicator is turned on. No stop will occur.	
WRE	Z	WRE00=WRE00 WRE(01-15)=WRE01	No change.	WRE00=WRE00 WRE(01-15)=WRE01	No change.	No WRE Mode. WRE00=WR00 WRE01=WR01 WRE02=WR02 WRE(03-15)=WR00	No WRE Mode. WRE00=WR00 WRE01=WR01 WRE02=WR02 WRE03=WR03 WRE(04-15)=WR00

Central Storage Chart

WORD SETS	7	6	5	4	3	2	1	0
WORDS	3 2 1 0	3 2 1 0	3 2 1 0	3 2 1 0	3 2 1 0	3 2 1 0	3 2 1 0	3 2 1 0
BANK 4	Standard Interface Channel	Standard Interface Channel	Standard Interface Channel	Standard Interface Channel			High-Speed Standard Interface Channel	High-Speed Standard Interface Channel
BANK 3	CASU 15	14 13	12 11	10 9	8 7	6 5	4 3	2 1
BANK 2			Interrupt Words 250-253		Channel for 729 Tapes	Channel for 729 Tapes	Channel for 729 Tapes	Channel for 729 Tapes
BANK 1	ASU 15	14 13	12 11	10 9	8 7	6 5	4 3	2 1
BANK 0	ACCUMULATOR							

Program Interrupt

The following program shows the use of interrupt, interrupt programming for I-O and for interrupt words 250 and 251, and the instructions TIP, LIP, and EIM.

The program reads an input tape, processes the record and writes it on an output tape. The housekeeping for the interrupt features and the interrupt programs are shown in detail, but the main portion of the program to process the record is not. The actual programs steps with explanatory comments are provided.

INSTRUCTION				
LOCATION	OPERATION	ADDRESS	STORAGE CODE	COMMENTS
Housekeeping Routine				
000004	EEM			
000009	SPC	002500		Set up interrupt words 250, 251
000014	SET	000016		
000019	LOD	010015		
000024	SPC	000000		
000029	SEL	002003		Test write tape for ready
000034	TR	000034		
000044	SEL	002104		Test write tape for ready
000049	TRR	000059		
000054	TR	000049		
000059	RD	001000		Read into area A
000064	TRR	000074		Ready loop
000069	TR	000069		Dummy transfer
000074	LDA	000049	01	Load address of read instruction
000079	TSA	004004		On error or EOF, go to appropriate routine
000084	TR	000089		Dummy transfer to save address
000089	RD	001085		Read into area B
000094	TRR	000104		Ready loop
000099	TR	000094		
000104	LDA	000084	01	Load address of read instruction
000109	TSA	004004		On error or EOF, go to appropriate routine
000114	SBZ	000999	01	Set on switch A full
000119	SBZ	000999	02	Set on switch B full
000124	SBZ	000999	03	Set on switch C empty
000129	SBZ	000999	04	Set on switch D empty
000134	RCV	000604		Set exit of record process routine and go to process A
000139	TSL	000169	01	
000144	EIM			
000149	TIP	005004		
000154	TIP	006004		
Main Program				
000159	TCV	000604		
000164	TSL	000169		Reset exit address
000169	RCV	000999		
000174	TZB	000194	01	If A is full, go to process A
000179	TZB	000214	02	If B is full, go to process B
000184	TIP	005004		Neither area full, go to read record
000189	TR	000169		Loop transfer
000194	RCV	002004		Move record in area A to work area
000199	TMT	001004		
000204	SBN	000999	09	Set off "A full" switch
000209	TR	000229		Go to process routine
000214	RCV	002004		Move record in area B to work area
000219	TMT	001089		
000224	SBN	000999	10	Set off "B full" switch
000229	RAD	002010		
Routine to Process Input Record				
000539	UNL	002080		
000544	RCV	000999		
000549	TZB	000569	03	If C is empty, go to move work to C
000554	TZB	000589	04	If D is empty, go to move work to D
000559	TIP	006004		Neither area empty, go to write record
000564	TR	000544		Loop transfer
000569	RCV	003004		Move processed record to area C
000574	TMT	002004		
000579	SBN	000999	11	Set off C empty switch

LOCATION	INSTRUCTION OPERATION	INSTRUCTION ADDRESS	STORAGE CODE	COMMENTS
000584	TR	000604		Go to exit
000589	RCV	003089		Move processed record to area D
000594	TMT	002004		
000599	SBN	000999	12	Set off D empty switch
000604	TR	000169		Exit (variable address)

Switches, Read, Write and Work Areas

000999				1 position, 4 bit switches
001004				Read area A
001084		bbb		
001089				Read area B
001169		bbb		
002004				Work area
002084				
003004				Write area C
003084				
003089				Write area D
003169				

Error and EOF Routine—Read

004004	ULA	004204	01	Set exit address
	TTC			Routine to differentiate between error and end of file and take appropriate action: backspace, error count, etc.
004204	TR	000069		Read error routine exit (adr. varies)

Error and EOF Routine—Write

004504	ULA	004804	02	Set exit address
	TTC			Routine to differentiate between error and end-of-file and take oppropriate action; backspace, error count, skip, etc.
004804	TR	006034		Write error routine exit (adr. varies)

Read Interrupt Program

005004	RCV	000999		
005009	TZB	005054	01	If A is full, check B
005014	TR	005019		Dummy transfer
005019	SEL	002104		
005024	RD	001000		Read record into area A
005029	LIP	002100		Transfer to main program
005034	LDA	005014	01	At end of RD, auto-interrupt to here save address for error routine
005039	SEL	002104		
005044	TSA	004004		On error or EOF, go to error routine
005049	SBZ	000999	01	Set on A full switch
005054	RCV	000999		
005059	TZB	005109	02	If B (and A) full, go to main program
005064	TR	005069		Dummy transfer
005069	SEL	002104		
005074	RD	001085		Read record into area B
005079	LIP	002100		Transfer to main program
005084	LDA	005064		End of RD, interrupt to here; save address for error routine
005089	SEL	002104		
005094	TSA	004004		On error or EOF, go to error routine
005099	SBZ	000999	02	Set on B full switch
005104	TR	005004		Loop transfer
005109	LIP	002100		A and B full, go to process record
005114	TR	005004		Loop transfer

Write Interrupt Program

006004	RCV	000999		
006009	TZB	006054	03	If C is empty, check D
006014	TR	006019		Dummy transfer
006019	SEL	002003		
006024	WR	003000		Write from area C
006029	LIP	002000		Go to main program
006034	LDA	006014	02	End of WR, interrupt to here; save address
006039	SEL	002003		
006044	TSA	004504		If error or EOF go to error routine
006049	SBZ	000999		Set on C empty switch
006054	RCV	000999		
006059	TZB	006109	04	If D (and C) empty, go to main program
006064	TR	006069		Dummy transfer
006069	SEL	002003		
006074	WR	003085		Write from area D

LOCATION	INSTRUCTION OPERATION	ADDRESS	STORAGE CODE	COMMENTS
006079	LIP	002000		Go to main program
006084	LDA	006064	02	End of WR, interrupt to here; save address
006089	SEL	002003		
006094	TSA	004504		If error or EOF go to error routine
006099	SBZ	000999	04	Set on D empty switch
006104	TR	006004		Loop transfer
006109	LIP	002000		Both areas empty, go to prosess record
006114	TR	006004		Loop transfer

Interrupt Word 251 Program

007004	UNL	012027	15	Save CASU 15
007009	LOD	011027	15	Load CASU 15 with new status
007014	SPC	001000		Save ASU's
007019	USB	012283		
007024	LSB	011283		Load ASU's with new information
007029	SPC	000000		
007034	USB	012539		Save ACC
007039	TRA			If error, go to correct routine
007044	LIP	000009		Return to main program

Interrupt Word 250 Program

007504	TAR	007624		Auto restart?
007509	SPC	003704		Save status from CASU 15
007514	UFC	012604		
007519	RCV	012603		Test status bits to determine cause of 250 interrupt
007524	TXB	007534	01	
007529	TR			Tr to correct 901 error
007534	TZB	007544	02	
007539	TR			Tr to correct 902 error
007604	SPC	003704		Restore CASU 15
007609	LFC	012604		
007614	TRA			
007619	LIP	000009		Return to main program
007624	SPC	003704		Save status from CASU 15
007629	UFC	012604		
007634	SBZ	012602	03	Set status bit off

Correct Error

007704	SPC	003704		Restore corrected status to CASU 15
007709	LFC	012604		
007714	TRA			
007719	LIP	000009		Return to main program

Index

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