IBM 8103 Processor

Preliminary Manual

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IBM 8103 Processor

Introduction

The IBM 8103 Processor is intended to relieve the larger systems of the series from the tasks associated with input-output processing. These important and time-consuming tasks consist of the translation, editing, format control and record grouping so common in today's data processing, and the message assembly, store and forward, data and line concentration, editing and code translation needed in Teleprocessing applications.

Simultaneous operation of input-output channels and processing is a basic feature of the system and is fully exploited by a method of automatic program queuing. The 8103 operates alone with its own integral core storage or it may operate concurrently with one of the other CPU's and share its larger and faster core storage unit. In such a combination, the 8103 enhances the concurrent input-output operation of the total system to include not just simultaneous read-write-compute but also concurrently operating translation, editing, format control, etc. The 8103 provides unusual flexibility in the input-output devices that may be attached. It can handle the slow character rates from type 1001 Data Transmission Units to the high character rates of the Advanced Tape System or the Million Character File. Future input-output devices will be readily attachable to the system because each input-output channel is terminated with the standard interface.

The system is capable of handling the peripheral input-output functions for a larger machine and is also capable of performing a complete data processing task for a small application. The equipment used for the tape to printer or card to disk operations provides,for example, the input-output equipment for the processor when used as an independent processing system.

Peripheral Operation

Independent peripheral operations may be performed by the 8103 for the other processors of the series. The 8103 in this case will communicate with the larger processors through cards, tapes and disks with a standard format. It is capable of receiving data in any code and performing a translation to another code as a by-product of the peripheral operation. These peripheral operations include:

1. card to tape or disk
2. tape or disk to printer
3. tape to and from disk

During these peripheral operations the processor will group or degroup tape records so that the larger processor may handle grouped records at all times and maintain maximum efficiency of its input-output equipment.

The stored program will be capable of detecting errors and recycling data in order to minimize operator intervention. By virtue of the stored program it is also possible to perform the functions of print editing such as: columnar rearrangement of data, punctuation control, zero suppression, accumulating totals, preparation of headings and controlling the printer and its carriage.

Teleprocessing

Telephone and teletype data may be entered into the processor through a multiplexing channel. The processor in this case provides the functions of message selection, message assembly and message queuing. The processor is designed for random access data processing. Its organization simplifies the task of selecting from a disk file the program necessary to process a particular piece of data. The actual execution of a particular program is controlled by the program queuing feature which enables the machine to link the various steps in the processing and input-output control of a given transaction while many transactions are in process at a time. This procedure is required by the fact that disk access is slow relative to processing speed.

Dynamic program relocation enables the system to fetch programs from a disk file and reassign the addresses which are part of the instructions in an efficient manner. This reassignment is necessary, since both data and instructions may be located in different storage locations each time the program is called in for processing a transaction. Program Relocation facilitates random processing of applications that require a total program storage capacity far in excess of any reasonable amount of core storage. In order to keep several transactions in process at the same time, it also permits several independent programs to coexist in core storage.

Storage protection is an additional benefit of program relocation. Because of this feature the various programs which are in the machine at one time can not affect each other. A storage allocation program assigns the storage areas which can be used by a particular processing program. Such a program has no access to any part of storage outside of its assigned areas.

Core Storage

The system may be equipped with either a 4,096 or 8,192 char-

acter core storage with an 8 microsecond cycle time as an integral part of the central processing unit. The word size is 18 bits, 16 information bits plus 2 parity checking bits. The internal logic of the system enables it to operate also with the 2 microsecond core storage units of the family, thus providing larger capacity, increased performance by a factor of 4 to 8, and the ability to share the workload with a larger system. The system is capable of addressing up to 65,536 words.

Input Output Operation

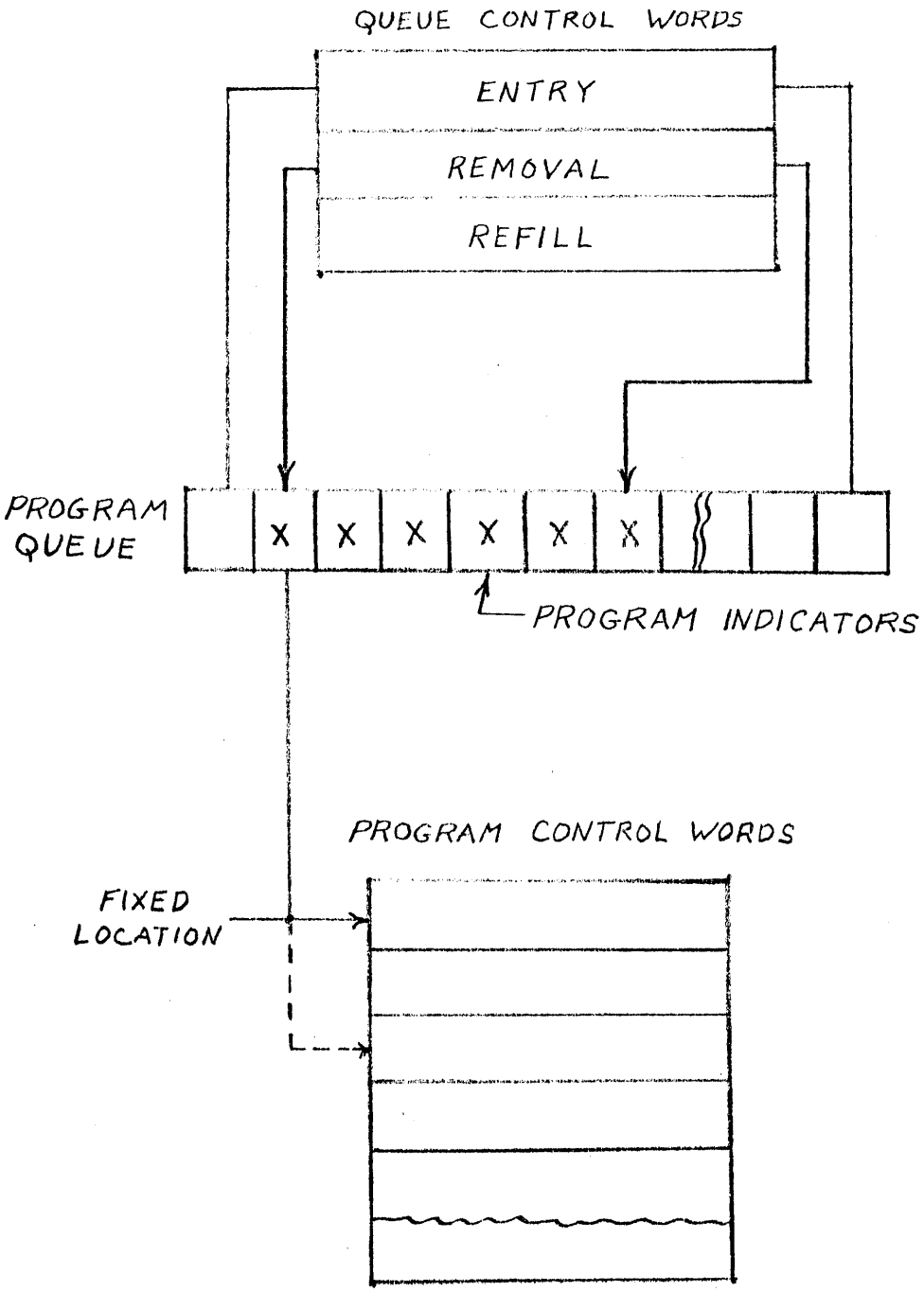
The system will include either 2 or 4 high speed data channels plus a multiplexing channel that will connect the various multiple line communication control units. All channels may be operating concurrently with processing. In the case of very high speed devices such as the Advanced Tape Unit or the Million Character File, a CPU lockout feature is provided to facilitate the handling of these higher data rates. When input-output data rates are less than 100KC the instruction sequencing and channels will operate simultaneously, sharing the same storage unit. Higher data rates are handled by utilizing the CPU registers for the buffering of data and the addressing of core storage. During the actual data transfer time the CPU is locked out.

Instruction Set

The operations provided by the processor's instruction set are primarily oriented for efficient control of input-output devices, data translation, format control and editing. Arithmetic and logical operations are performed with two-address instructions in conjunction with tables in storage. Flexibility is emphasized to enable the system to execute the common data processing instructions.

Multiple Programs

The automatic flow of stored program operations is directed by a table of program control words, which are located in core storage starting at a fixed location. A particular program is put into operation by obtaining its associated program control word from the table, using a queue of program indicators. The queue is located in core storage and is actually a string of 8-bit bytes which are used as the program indicators. The stepping of the program indicator in the queue is directed by a pair of control words. One keeps track of the next program to be placed in active status and the other controls the stacking of program indicators at the end of the queue. When the CPU initiates an input-output operation for a particular program, it places the program indicator for that program in the channel control word. That program is then automatically taken out of active status and the instruction counter is stored in the program control



8103 Program Queuing

word. The next program in the queue enters active status. At the completion of the input-output operation the program indicator that was stored in the channel control word is placed at the end of the queue.

This feature provides the automatic linking of the various elements of input-output handling and the processing of multiple items at one time.

Program Relocation

A program has associated with it a table which contains the actual storage addresses that are assigned to the various program regions by the storage allocation program. The operand address of an instruction contains two parts; the first is a symbolic address used to address the table to select the regional address; the second is the address of the operand relative to the beginning of the region.

Storage Protection

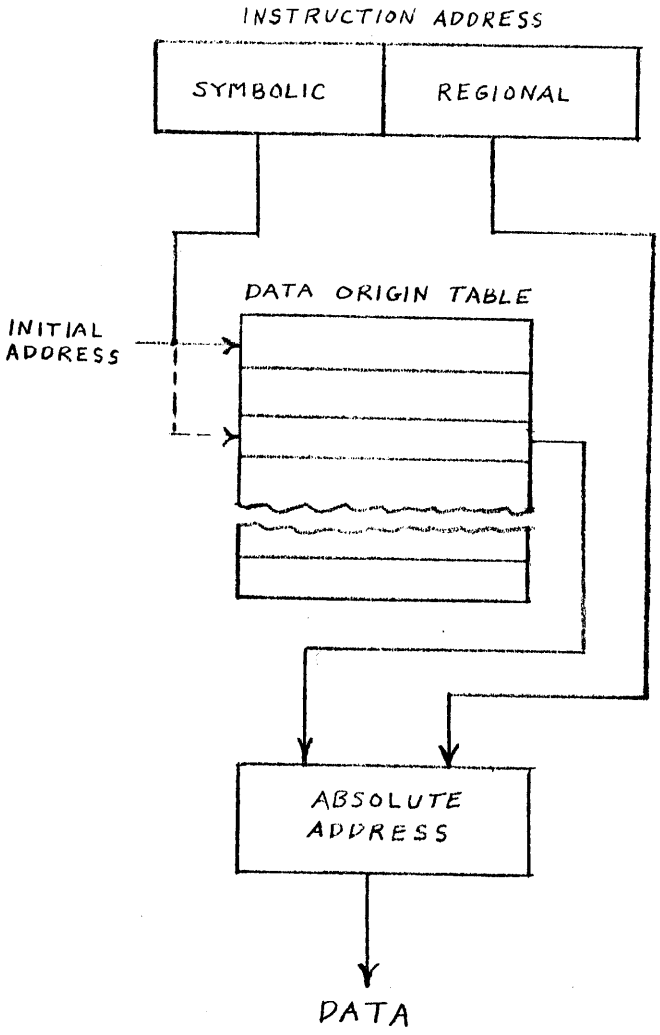
The program relocation feature of the system effectively partitions storage, giving each program certain regions. It is this partitioning that prevents one program from altering storage outside its assigned boundaries. A program can even be prevented from altering its own table of block addresses by placing the table in a block that is not addressed by any of the table entries.

Data Formats

The processor reads and writes data in the same identical format as the other CPU's in the series. Since the system uses the same input-output devices, adapters and interfaces, the recording characteristics are physically the same. Internally, the system handles bytes, fields and records in the same manner and uses the same collating sequence as the other CPU's.

Code Translation

The TRANSLATE instruction provides the ability to recode 4-bit or 8-bit bytes. It also allows expansion and compression of byte sizes between 4-bit and 8-bit byte sizes. The instruction has a three-address format. One address specifies the starting address of a table. The other two addresses each specify a source stream of bytes. The result of the translation replaces one of these streams. Bytes from one or both of the source streams are combined with the starting address to obtain a table entry address. The 4-bit or 8-bit byte at this address replaces the byte from the source stream.



8103 Program Relocation

Algebraic Addition and Subtraction

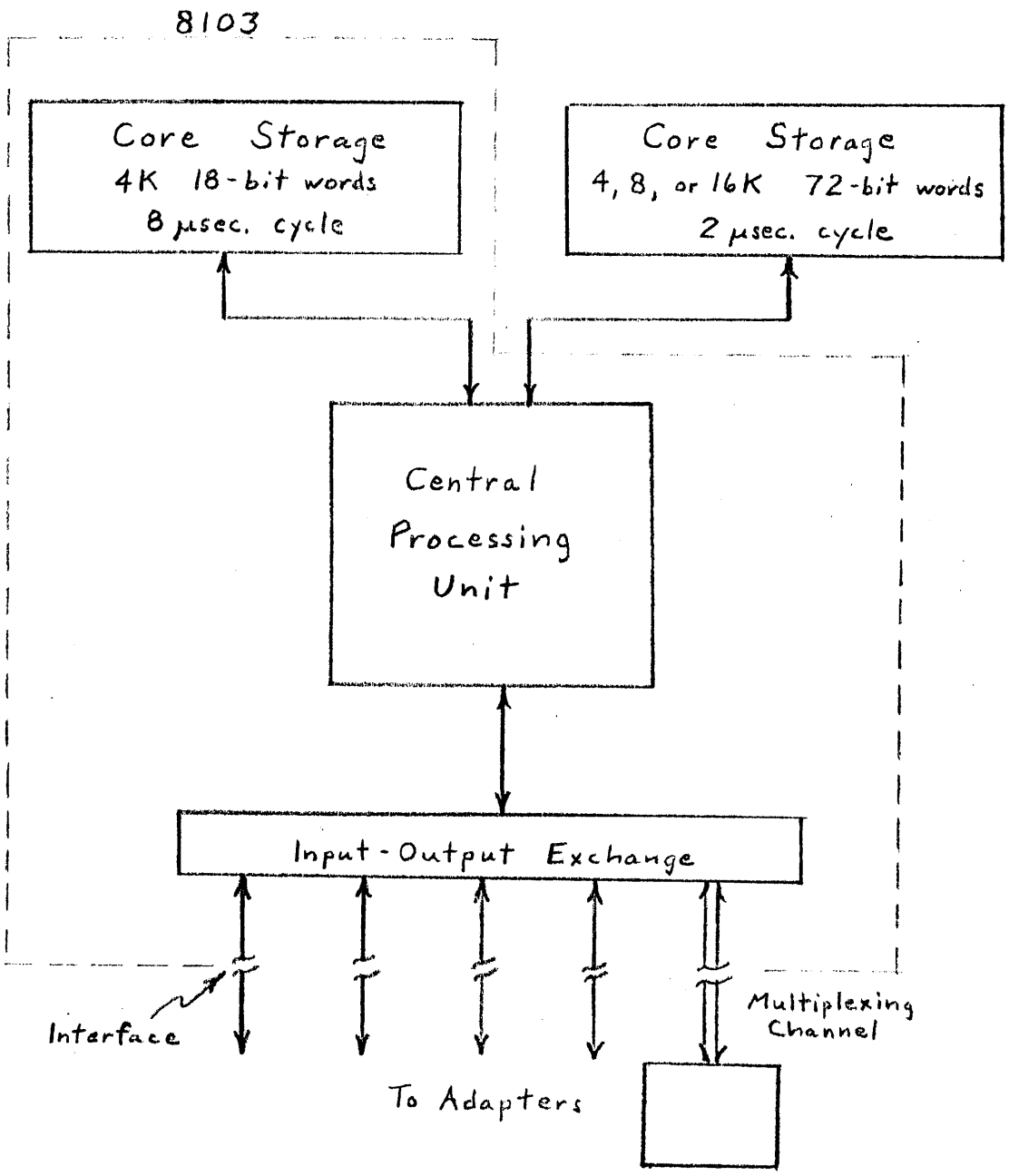
Algebraic addition and subtraction are performed by means of a special translation instruction, utilizing a table-look-up procedure. Data is processed in 4-bit bytes from right to left. If a signed operation is specified, the sign occupies the right-most byte of the operand. The translation process uses a digit from each operand to look up a sum or difference digit in a table. Also obtained from the table is a carry or borrow digit, which is placed in the condition register, where it enters into the selection of the next result digit from the table.

Modular Performance

Increased CPU performance is provided when the system works in conjunction with one of the 2 microsecond core storage units. The access time is reduced from 8 to 2 microseconds and the amount of data read out in a cycle is increased from 18 to 72 bits. The CPU data flow paths are sufficiently fast to take advantage of the reduced cycle time and the organization of the registers is such that it is possible to take advantage of the additional parallelism provided by the 72 bit readout. The processor still retains the flexible data handling characteristics of a serial machine and combines the performance virtues of a parallel machine. The logical design of the processor provides the potential of additional performance by adding hardware which will reduce the number of storage cycles required for most functions.

Reliability

The processor is constructed of highly reliable circuits and of conservative design to ensure reliable operations. The high level of reliability is consistently maintained by incorporating data flow and control checking facilities in the processor. Inherent in the basic design of the processor are facilities for duplexing the equipment to provide 24 hour operation and to maintain the rated performance of the system. For the larger systems, reduced performance processing capabilities can be maintained during service time by using this system to process the high priority data and to queue other incoming data.



8103 System Organization