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IBM **Maintenance Information**

INDEX	OLT	DEV-I	HDA	R/W	MICFL
MLX	OPER	DATA	ACC	RPI	
LGND	PANEL			PWR	
START	CTL-I			LOC	
FSI				INST	
MSG					
SENSE					
MICRO					
VOL. R01	VOL. R02	VOL. R03	VOL. R04	VOL. R05	VOL. R06

Volumes R01 through R06 accompany each Control Module and support all 3350s attached.

3350 Disk Storage

3350

GA0000 Seq. 1 of 2	2358633 Part No.	441300 31 Mar 76				

PREFACE

MAINTENANCE INFORMATION MANUAL ORDERING PROCEDURE (IBM Internal)

Individual pages of the 3350 Maintenance Information Manual can be ordered from the San Jose plant by using the Wiring Diagram/Logic Page Request (Order No. 120-1679). In the columns headed "Logic Page" enter the page identifier information: sequence number, sheet number, part number, and EC number. Groups of pages can be ordered by including a description (section, volume, etc.) and the machine serial number.

This manual was prepared by the IBM General Products Division, Technical Publishing, Department G26, San Jose, California 95193.

3350

GA0000 Seq. 2 of 2	2358633 Part No.	441300 31 Mar 76				

SAFETY

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power, ac and dc, when removing or assembling major components, working in immediate areas of power supplies, performing mechanical inspection of power supplies, or installing changes in machine circuitry.
3. After turning off wall box power switch, lock it in the Off position or tag it with a "Do Not Operate" tag, Form 229-1266. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, observe the following precautions:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Do not wear rings, wrist watches, chains, bracelets, or metal cuff links.
   c. Use only insulated pliers and screwdrivers.
   d. Keep one hand in pocket.
   e. When using test instruments, be certain that controls are set correctly and that insulated probes of proper capacity are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc.). Use suitable rubber mats, purchased locally if necessary.
5. Wear safety glasses when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power or hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Cleaning parts with solvents, sprays, cleaners, chemicals, etc.
   f. Performing any other work that may be hazardous to your eyes. REMEMBER – THEY ARE YOUR EYES.
6. Follow special safety instructions when performing specialized tasks, such as handling cathode ray tubes and extremely high voltages. These instructions are outlined in CEMs and the safety portion of the maintenance manuals.
7. Do not use solvents, chemicals, greases, or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles – this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. After maintenance, restore all safety devices, such as guards, shields, signs, and grounding wires.
12. Each Customer Engineer is responsible to be certain that no action on his part renders products unsafe or exposes customer personnel to hazards.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. Ensure that all machine covers are in place before returning machine to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it; for example, under desk or table.
16. Avoid touching moving mechanical parts when lubricating, checking for play, etc.
17. When using stroboscope, do not touch ANYTHING – it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CEs and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machine while performing and after completing maintenance.

Knowing safety rules is not enough.
An unsafe act will inevitably lead to an accident.
Use good judgment - eliminate unsafe acts.

ARTIFICIAL RESPIRATION

General Considerations

1. Start Immediately – Seconds Count
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim, or apply stimulants.
2. Check Mouth for Obstructions
   Remove foreign objects.
3. After victim is breathing by himself or when help is available:
   a. Loosen clothing.
   b. Place victim on his side.
   c. Keep victim warm.
4. Remain in Position
   After victim revives, be ready to resume respiration if necessary.
5. Call a Doctor
   Have someone summon medical aid.
6. Don't Give Up
   Continue without interruption until victim is breathing without help or is certainly dead.

Rescue Breathing for Adults

1. Place victim on back; lift neck and tilt head way back. (Quickly remove any noticeable food or objects from mouth.)

2. Pinch nose closed; make airtight seal around victim's mouth with your mouth; and forcefully breathe into victim until chest rises (expands).

3. Continue breathing for the victim 12 times per minute WITHOUT STOPPING.
4. If chest does not rise (expand), roll victim onto side and pound firmly between shoulder blades to remove blocking material. Also, try lifting jaw higher with your fingers. Resume rescue breathing.

MICFL CONTENTS

3350 MICRODIAGNOSTIC OVERVIEW

PHILOSOPHY

Purpose of Microdiagnostics:

The microdiagnostic package is designed to aid the CE in maintaining the IBM 3350 Direct Access Storage Device. This package can be used in the following ways:

- FRU List

The number of possible field replaceable units (FRUs) can be greatly reduced by a microdiagnostic that recreates the failing condition.

- Degraded Performance

The microdiagnostic package resolves failures in hardware that create a degraded product performance; for example, excessive seek errors in a particular drive.

- Adjustments

Adjustments in the servo area can be verified with microdiagnostics. The velocity gain can be adjusted entirely with a microdiagnostic, eliminating the need for a scope.

- Verification of Repair Action

The microdiagnostic package can be used to check out the 3350 after repair. This ensures a correct repair before returning the machine to the customer.

Building Block Concept

The Building Block concept tests the hardware in a logical, orderly, progressive sequence starting with the controller interface and working progressively toward the most complex areas of the machine. This type of testing first proves that a complete path from the attachment through the device is operative before attempting to test the more complex functions of the machine. This achieves a high degree of confidence in the information received in further testing of a variety of increasingly complex operations.

DEPENDENCIES

Hardcore

The hardcore of any system or subsystem is defined as the minimum amount of hardware that must be operative to execute a diagnostic and analyze the results of execution with a high degree of confidence. Because of the many attachment configurations possible with the 3350, the assumption that the hardware on the attachment side of the interface is operative must be made. This hardware, a part of the hardcore, is tested by diagnostics designed for the particular attachment, for example, the 3830-2, the Integrated Storage Control (ISC), and the 3880 Storage Control. The 3350 Control Interface consists of:

- Controller Interface Line Drivers and Receivers.
- Tag Bus and Bus Out.
- Select Hold and Tag Gate.
- Unselected Alert Line (CE Alert).
- Execute Switch and Associated Latch.
- CE Panel Switches, Registers, and Lamps.

If any of the above 3350 hardware is inoperative, it can be diagnosed from the attachment side of the interface by the Control Interface Bringup program and its associated MAPS. To further diagnose the CE panel hardware, use Routine A0, the CE panel test.

IMPLEMENTATION

Microdiagnostic Error Detection Methods.

Whenever a microdiagnostic uses an error detection circuit within the building block scheme, the circuit is first checked for correct operation before using it to test the circuit, an error condition is forced on, and verified. The error is then reset and the reset condition verified before continuing the test. The microdiagnostic package detects errors in the following ways:

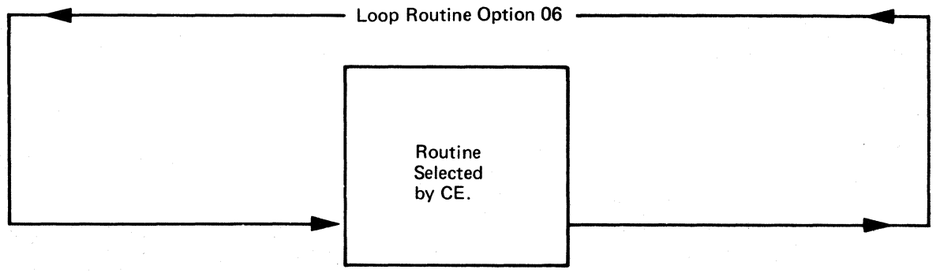
- An operation is performed and the data received is compared to the expected or normal data. If the received and expected data do not compare, an error is indicated.
- An event or series of events is timed with a microprogram controlled timer. The actual measured time is compared to an engineering specification. If the measured time is not within the limits of the engineering specification, an error is indicated.
- An operation is performed and the resultant state of an error check is tested to verify correct or incorrect operation.

3350 Linked Series Microdiagnostics

The 3350 Building Block concept consists of nine routines linked together to appear as a single routine. This is known as Linked Series.

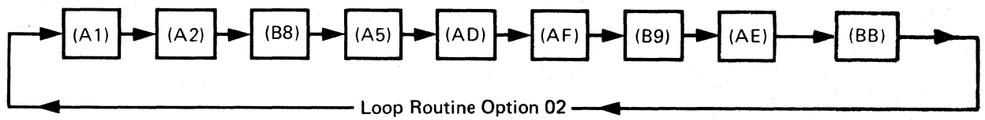
LOOP OPTIONS

Without Linked Series



Note: *Option 06 inhibits linking and continues to loop the selected routine until stopped by an error or by the run control option 00.*

With Link Series



Note: *Loop routine Option 02 starts with routine A1 and links to A2, A2 to B8, etc., until BB is completed. Routine BB then links back to A1 and the process continues until stopped by detection of an error or run control option '00'.*

GENERAL ROUTINES

SYMBOL	DESCRIPTION
DECREMENT COUNT BY (XX)	PROGRAM PROCESS
S2 ← SELECT CONTROLLER ---------- TAG'03'_BUS'XX'	TAG SEQUENCE TAG AND BUS OUT VALUES ARE SHOWN ON BOTTOM LINE (IN HEX). IF BUS VALUE IS VARIABLE XX IS USED. THE SCOPE SYNC OR SCOPE TEST POINT MAY BE INDICATED BY ALD NET REFERENCE BELOW BLOCK. A BLACK CIRCLE WITH A WHITE S PLUS A NUMBER INDICATES A SYNC POINT. THAT SYNC POINT CARRIES THE SAME NUMBER WHEREVER IT APPEARS IN A PARTICULAR TEST. SCOPE POINT IS NOT ALWAYS INDICATED.
ERROR STOP DISPLAY (MICFL 5) ERROR-CODE	
ERROR STOP DISPLAY (MICFL 5) ERROR CODE → 1	AN ERROR DETECTED BY THE PROGRAM IS INDICATED BY ANY ONE OF THE THREE BLOCKS AT LEFT. THE SCOPE SYNC POINT FOR LOOPING ON THE ERROR IS SHOWN IN A NOTE BLOCK APPEARING ELSEWHERE ON THE PAGE. THE NOTE BLOCK IS REFERRED TO BY A BLACK CIRCLE OR SQUARE CONTAINING THE NOTE NUMBER. THE NOTE BLOCK USUALLY APPEARS AT THE BOTTOM OF THE PAGE. THE POINT WHERE THE SYNC IS ISSUED CAN BE FOUND BY FOLLOWING THE FLOW CHART BACK UNTIL A BLOCK IS FOUND WITH A SYNC INDICATION. SEE SCOPE SYNC POINT DESCRIPTION BELOW. THE SUBROUTINE THAT DISPLAYS THE ERROR CODE IS DESCRIBED ON MICFL 5. GENERAL NOTES ARE IDENTIFIED WITHIN THE CIRCLE BY A NUMBER.
ERROR STOP DISPLAY (MICFL 5) ERROR CODE → 2	
DYNAMIC DISPLAY (MICFL 5) ERROR CODE → 3	
SET UP DISPLAY FOR ERROR NUMBER='XX' ERROR CODE → 4	
1 ← NOTE INFORMATION GOES IN THIS BOX	
2 ← SYNC POS CTLR J2D11 +SELECT ACTIVE ALD REF CC1011AK2 → S2	SCOPE SYNC POINT IS INDICATED WITH POLARITY (POS OR NEG); BOX (CTLR OR DRV); AND PIN, WITH ITS LOGIC NAME AND ALD NET.

MLM0006 441300
MICFL 03_L
H01
JFL_1/16/76

SYMBOL	DESCRIPTION
NO ← ERROR OCCURRED → YES	ANY DECISION SCOPE POINT MAY BE INCLUDED AS IN TAG SEQUENCE BLOCK.
INLINE CHECK (MICFL 5)	PREDEFINED PROCESS. A SUBROUTINE THAT IS DESCRIBED ELSEWHERE IN THE MICFL SECTION. THE PAGE NUMBER WITHIN OR ABOVE THE BLOCK IS WHERE THE SUBROUTINE IS DESCRIBED.
H02 A1	OFF-PAGE CONNECTOR - ENTRY CHART ID IS DESIGNATED ON FIRST LINE (H02). ENTRY BLOCK CONNECTOR ID IS DESIGNATED ON SECOND LINE (A1).
H09 A1	OFF-PAGE CONNECTOR - EXIT 'TO' CHART ID IS DESIGNATED ON FIRST LINE (H09). 'TO' BLOCK CONNECTOR ID IS DESIGNATED ON SECOND LINE (A1).
B2	INTERNAL PAGE CONNECTOR - EXIT THE EXIT CONNECTOR CONTAINS THE COORDINATE DESIGNATION OF THE NEXT BLOCK TO BE ENTERED. COORDINATES ARE A-K VERTICALLY AND 1 - 9, 0 HORIZONTALLY.
B2	INTERNAL PAGE CONNECTOR - ENTRY THE ENTRY CONNECTOR CONTAINS THE COORDINATE DESIGNATION OF THE BLOCK TO BE ENTERED. THE COORDINATE CHARACTERS MUST MATCH BETWEEN THE EXIT AND ENTRY SYMBOLS TO VERIFY THE CORRECT ENTRY.
	ABBREVIATIONS MSEC = MILLISECOND USEC = MICROSECOND CTLR = CONTROLLER DRV = DRIVE '12' = SINGLE QUOTES AROUND 'A3' A NUMBER OR SERIES OF NUMBERS INDICATE A HEXADECIMAL VALUE.
	THE BLOCK TO THE RIGHT IS USED ONLY BY THE WRITER TO IDENTIFY THE PARTICULAR CHART BEFORE IT IS AFFIXED TO THE FINAL MLM PAGE. IT HAS NO MEANING IN THE FLOW DIAGRAM AND SHOULD BE IGNORED BY THE CE.

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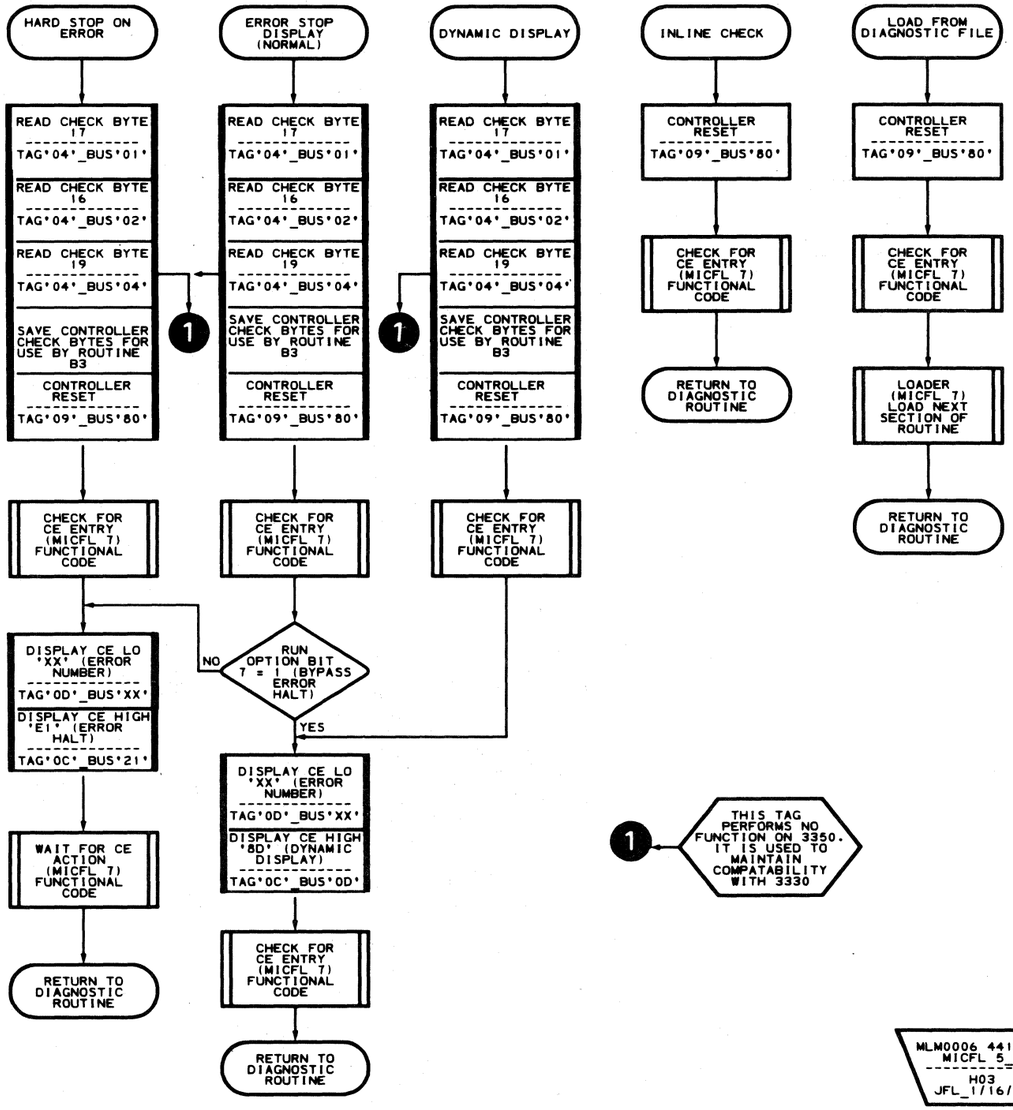
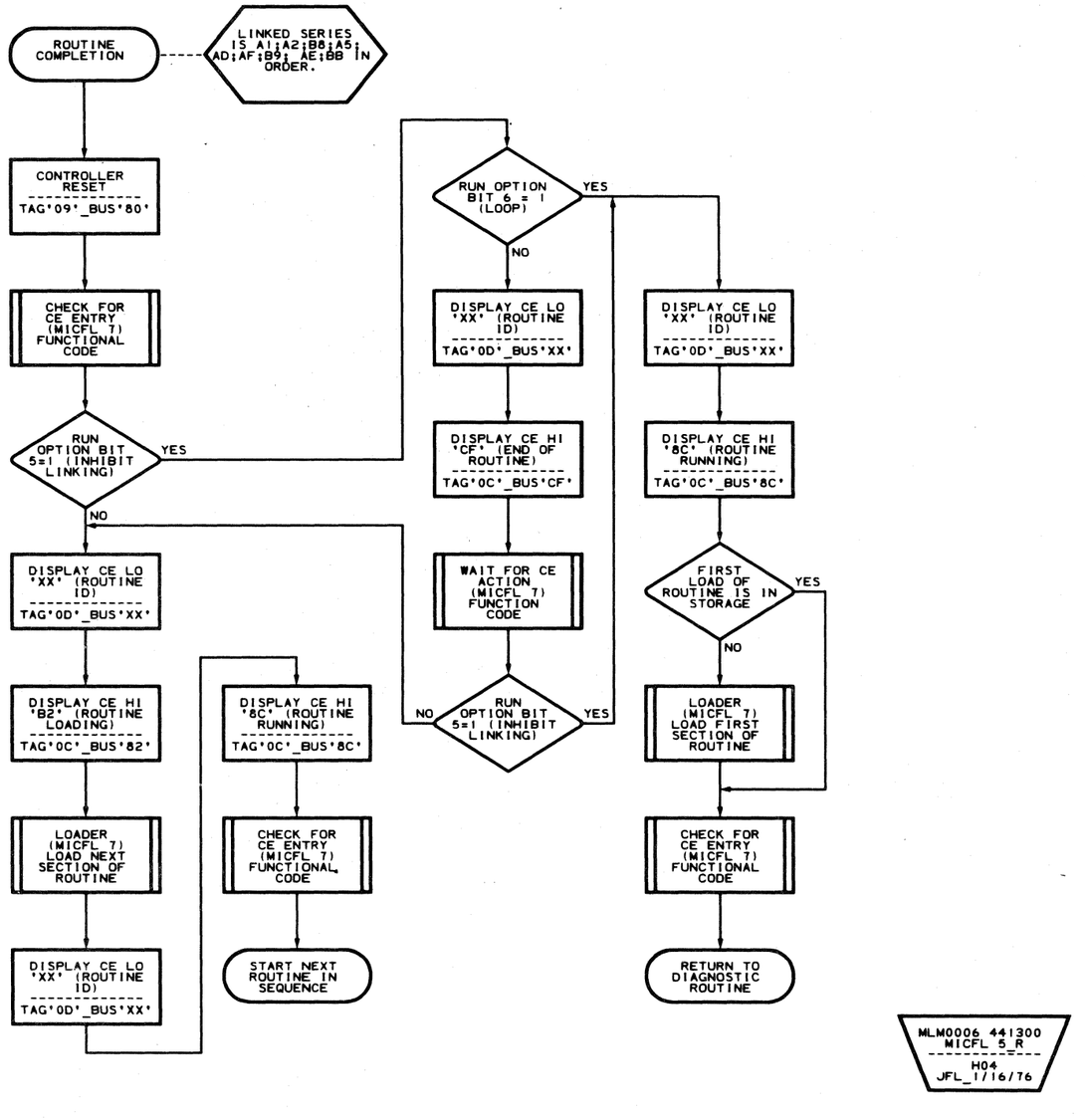
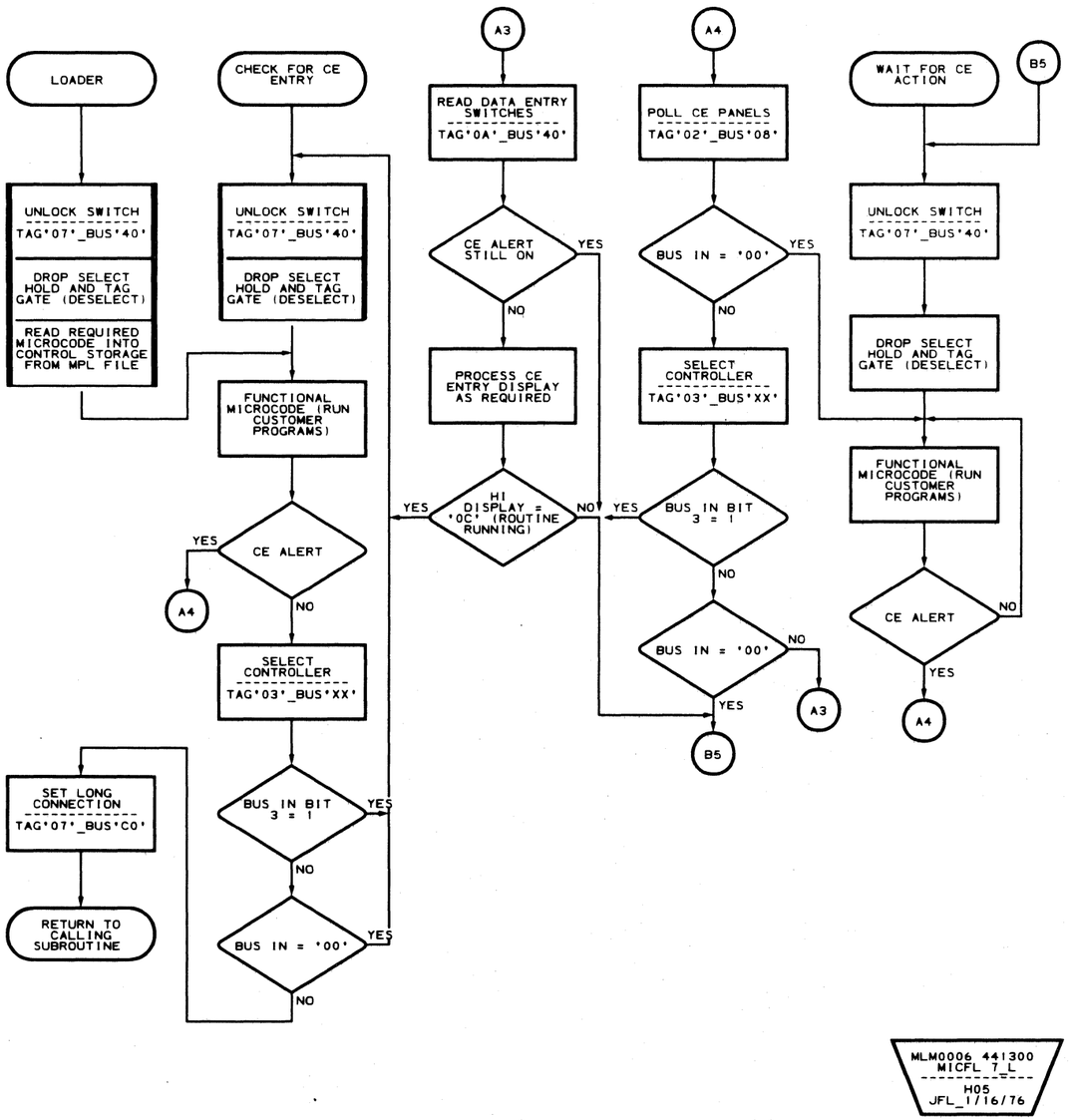
MICFL 03_R
H02
JFL_1/16/76





GENERAL ROUTINES



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MICFL 7 L
H05
JFL 1/16/76

ROUTINE A0 — CE PANEL TEST

DESCRIPTION

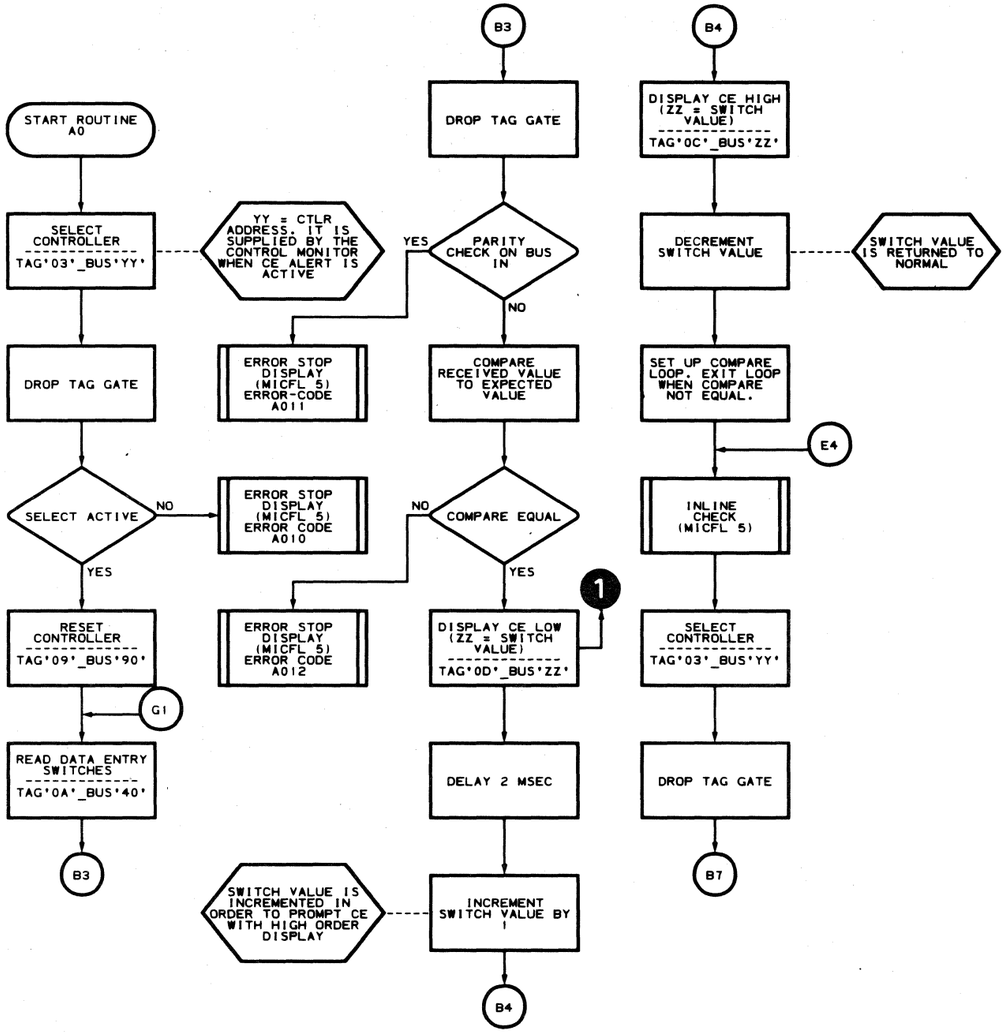
The purpose of Routine A0 is to test the CE panel hardware. The hardware to be tested consists of the Data Entry switches, the Program Control and Data Display lamps, and their associated registers. Prompting is used in this test by displaying the received and next-expected switch values simultaneously. This is done by displaying the switch value just read in the Data Display lamps, and by incrementing this value by 1 and displaying the next-expected value in the Program Control lamps. The prompting continues throughout the test until each position of both Data Entry switches has been tested.

The program ends execution when the Data Entry switches complete the entire sequence. This occurs when the switches are set from '0F' to '00'. The program can be restarted at any time by using the '00' run control option.

OPERATING PROCEDURE

- Refer to MICRO 1C and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.

ROUTINE A0 – CE PANEL TEST MICFL 13



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MICFL 13_L
HAA
JFL_1/16/76

MLM0006 441300
MICFL 13_R
HAB
JFL_1/16/76

ROUTINE A1 – 3350 CONTROLLER INTERFACE AND LOGIC TESTS

DESCRIPTION

Test 01. Controller Preselection

Test 01 verifies that there are no active lines between the 3350 controller and storage control prior to controller selection.

Test 02. Controller Selection

Test 02 verifies that certain lines between the 3350 controller and storage control remain inactive while others become active following controller selection. It also verifies that a valid 3-of-6 code is returned upon controller selection.

Test 03. Controller Tag Bus, Bus Out, and Bus In Parity Check

Test 03 verifies that the Tag Bus and Parity Checks in the 3350 controller can be forced on and then reset by a Reset Controller.

Tag Bus Parity Check is forced on by an invalid controller tag (Tag '94' Bus '00').

Bus Out Parity Check is forced on by varying the Bus Out value with Tag Gate still active.

Test 04. Controller Tag Valid/Normal End

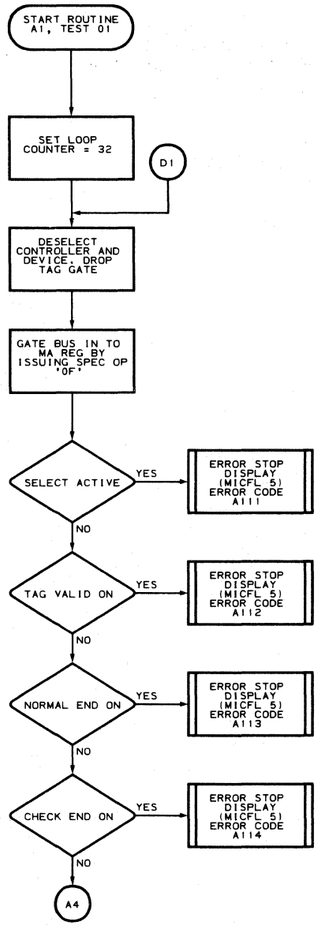
Test 04 verifies that the storage control receives Tag Valid and Normal End for all the Immediate Op Tags (0B, 01, 02, 04 through 07, 09 and 0A) and that Tag Bus and Bus Out parity checks are inactive. It also verifies that the storage control receives Tag Valid and no Normal End for all the Extended Op Tags ('08', '0E', and '0F') and that the Tag Bus and Bus Out parity checks are inactive. In addition, the test forces a Monitor Check and ensures that it can be reset following a Reset Controller command.

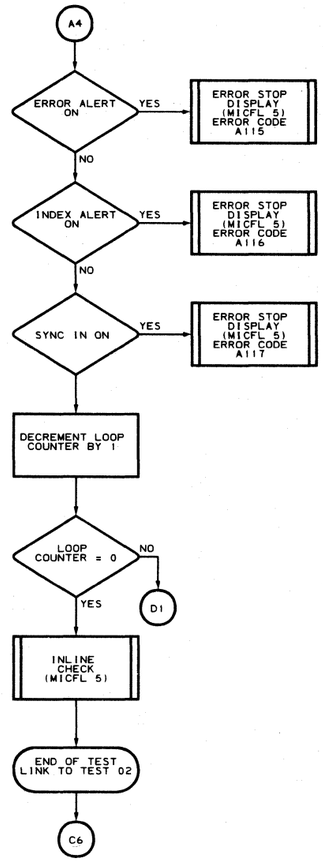
Test 05. Bus In Assembler

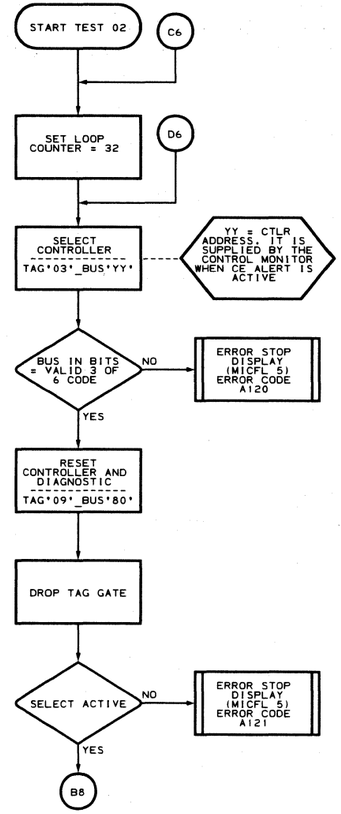
Test 05 verifies that the correct Bus In information is gated under control of the Bus In selection bits. There are four buses that are gated through the Bus In Assembler. The test also verifies that a parity check is not generated in the storage control. The controller Bus In Parity Check is also tested by the diagnostic command Invert Bus In Parity (Tag '09' Bus '20').

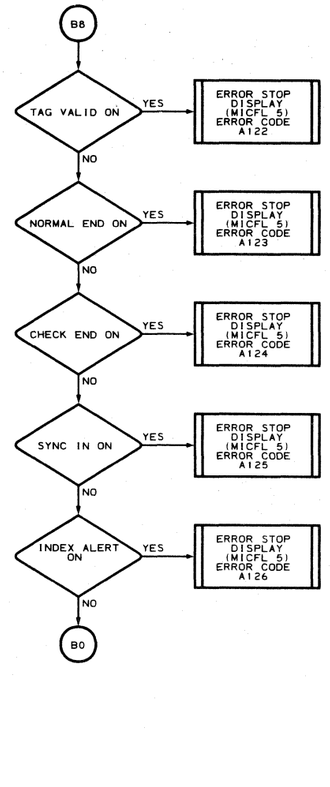
OPERATING PROCEDURE

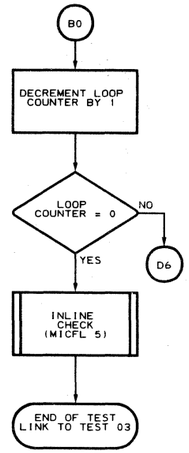
- Refer to MICRO 10 and 11 for standard operating procedure.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.











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MICFL 21 L
HAC
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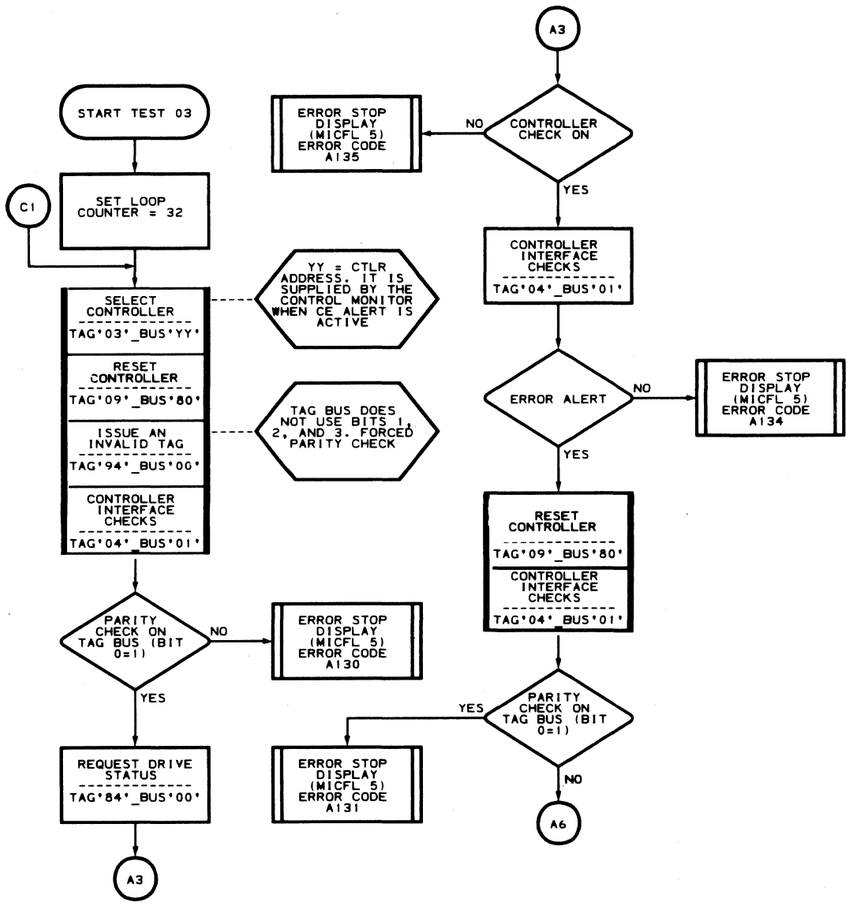
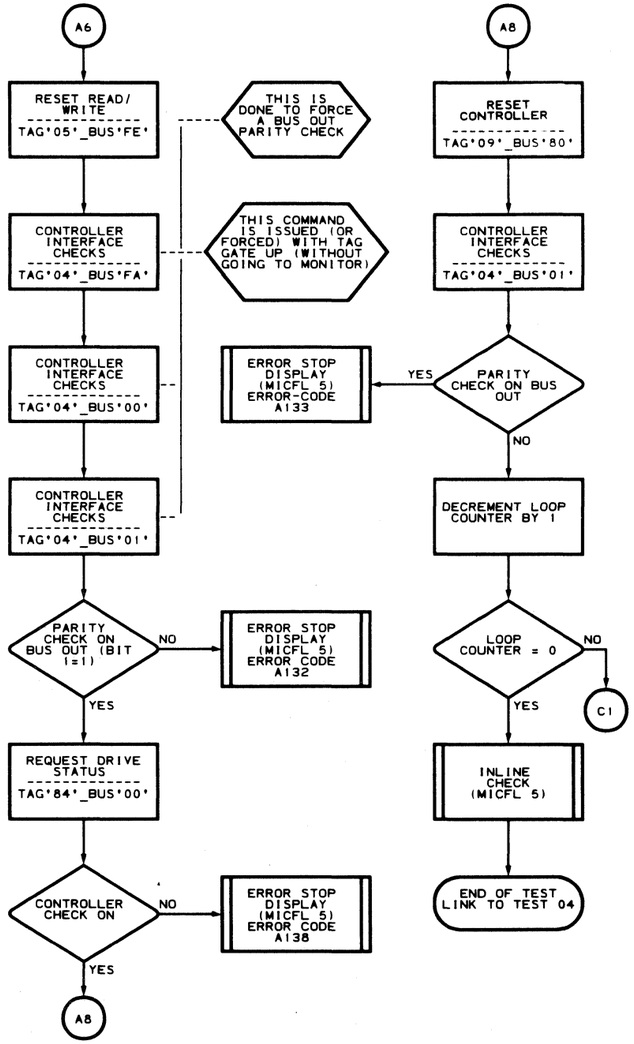
ROUTINE A1 – CONTROL INTERFACE AND LOGIC TESTS





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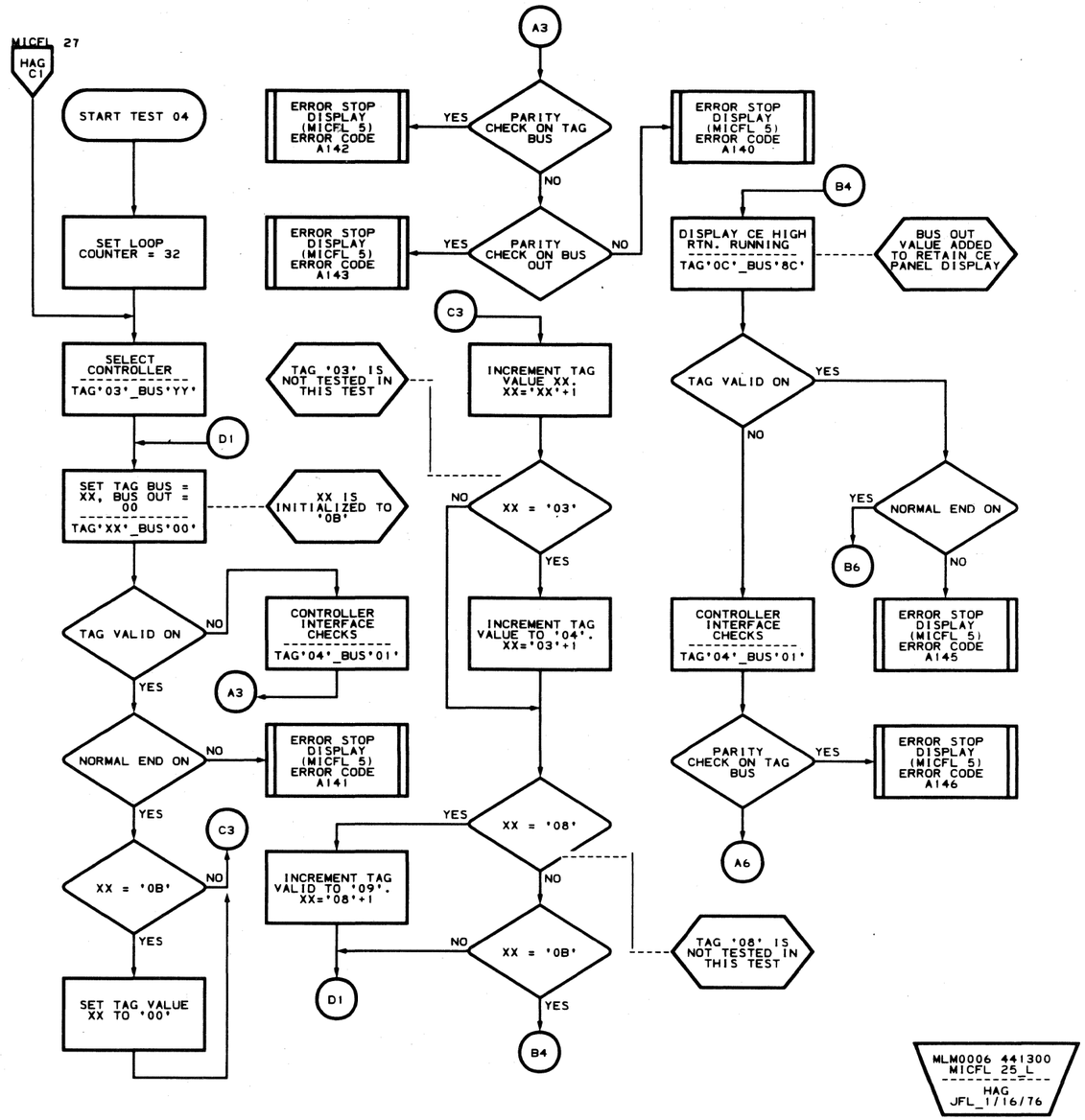
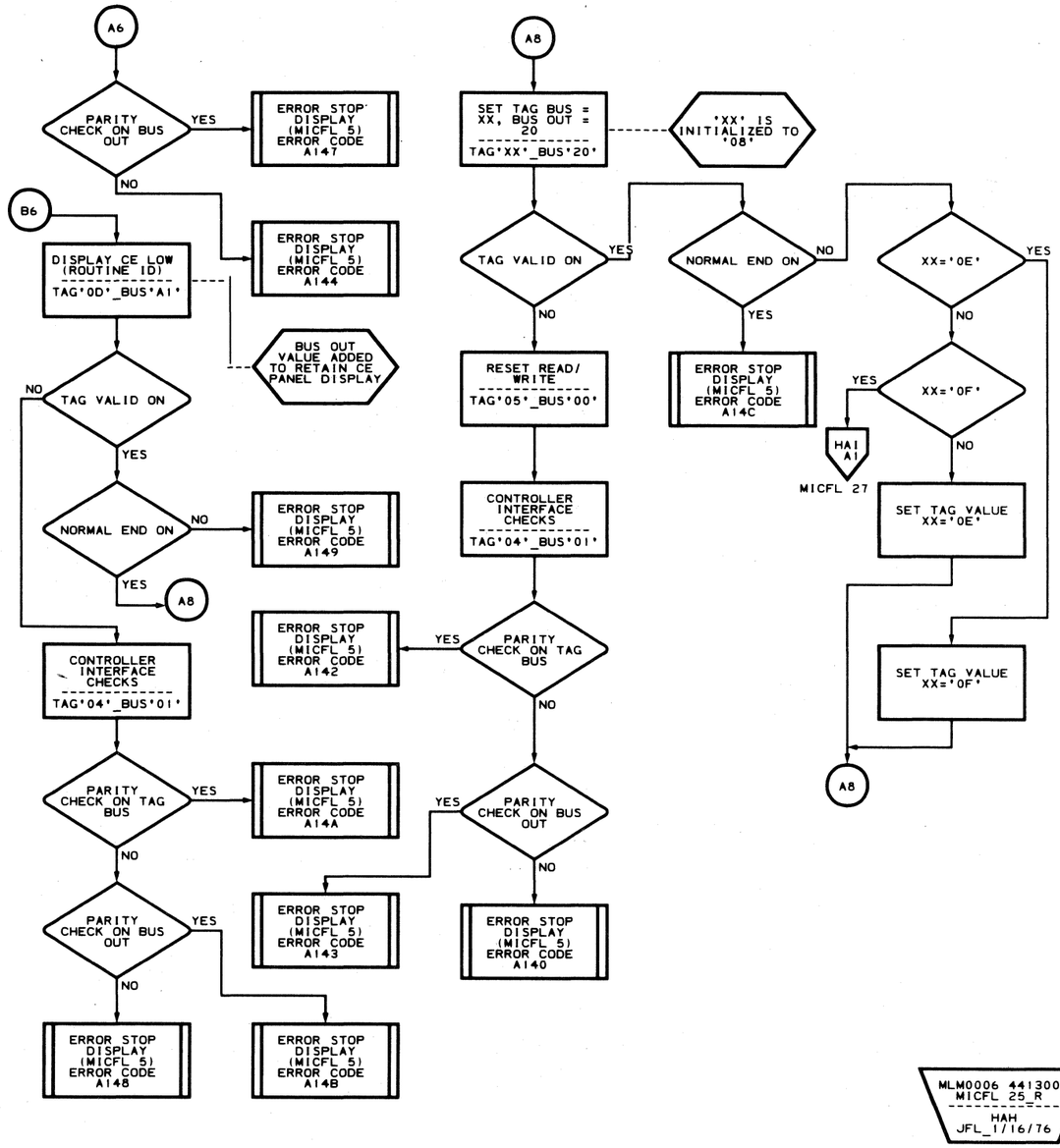
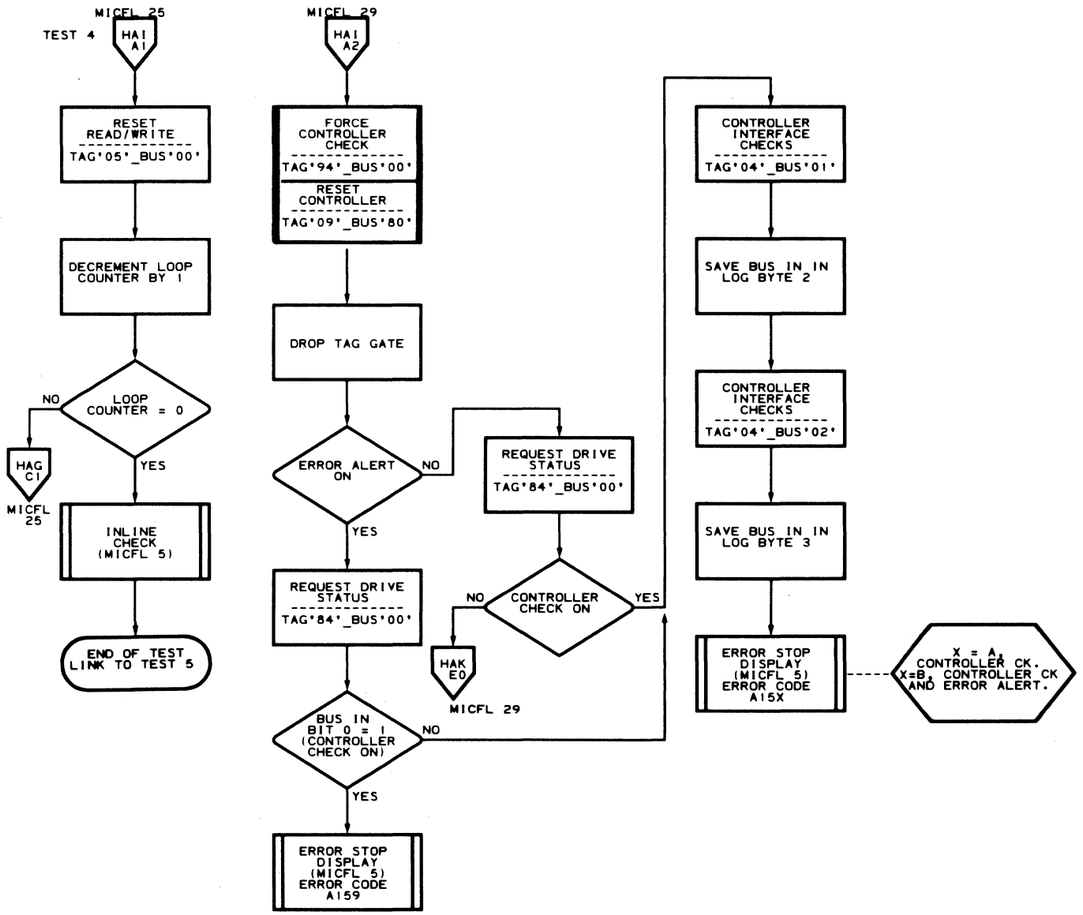




ROUTINE A1 – CONTROL INTERFACE AND LOGIC TESTS



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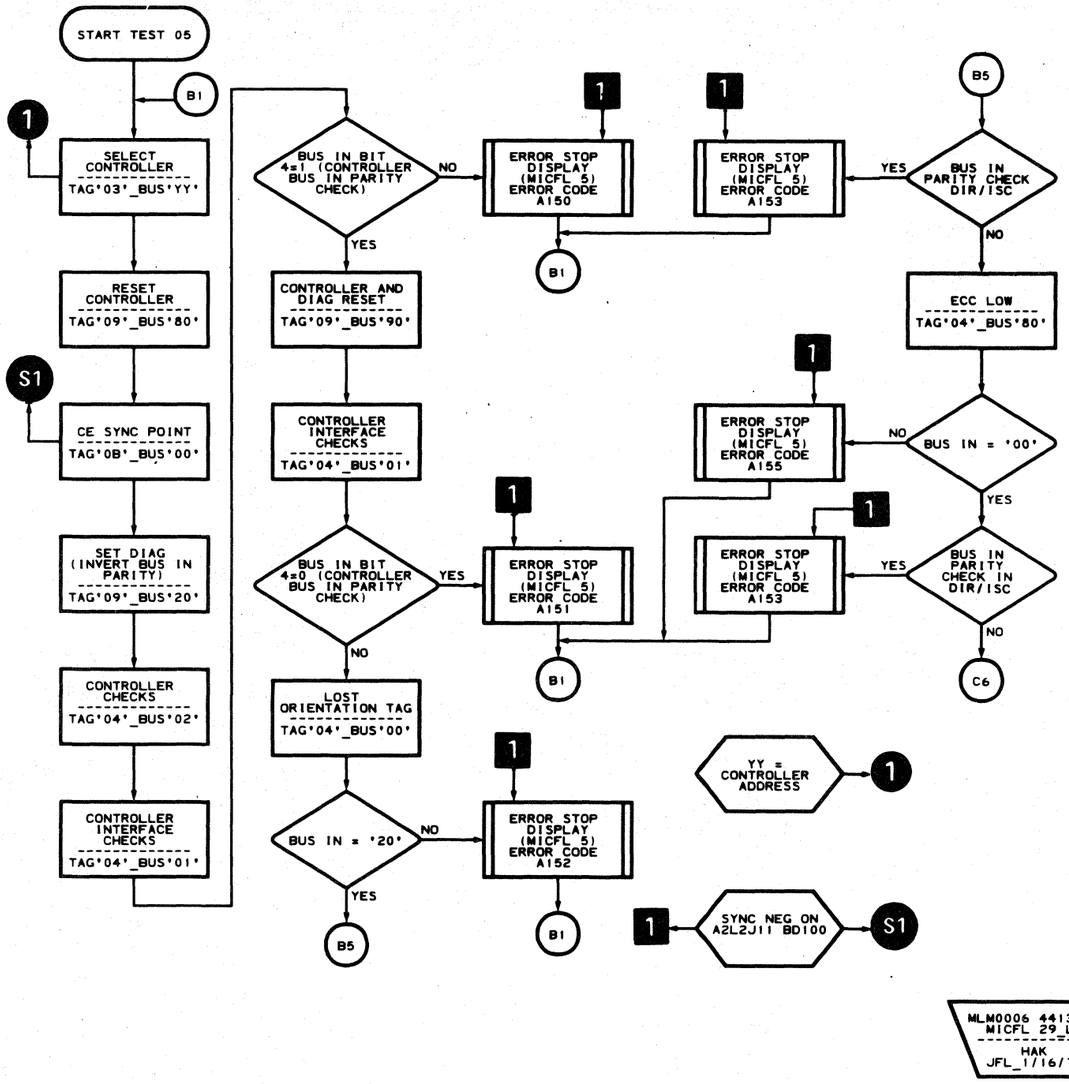
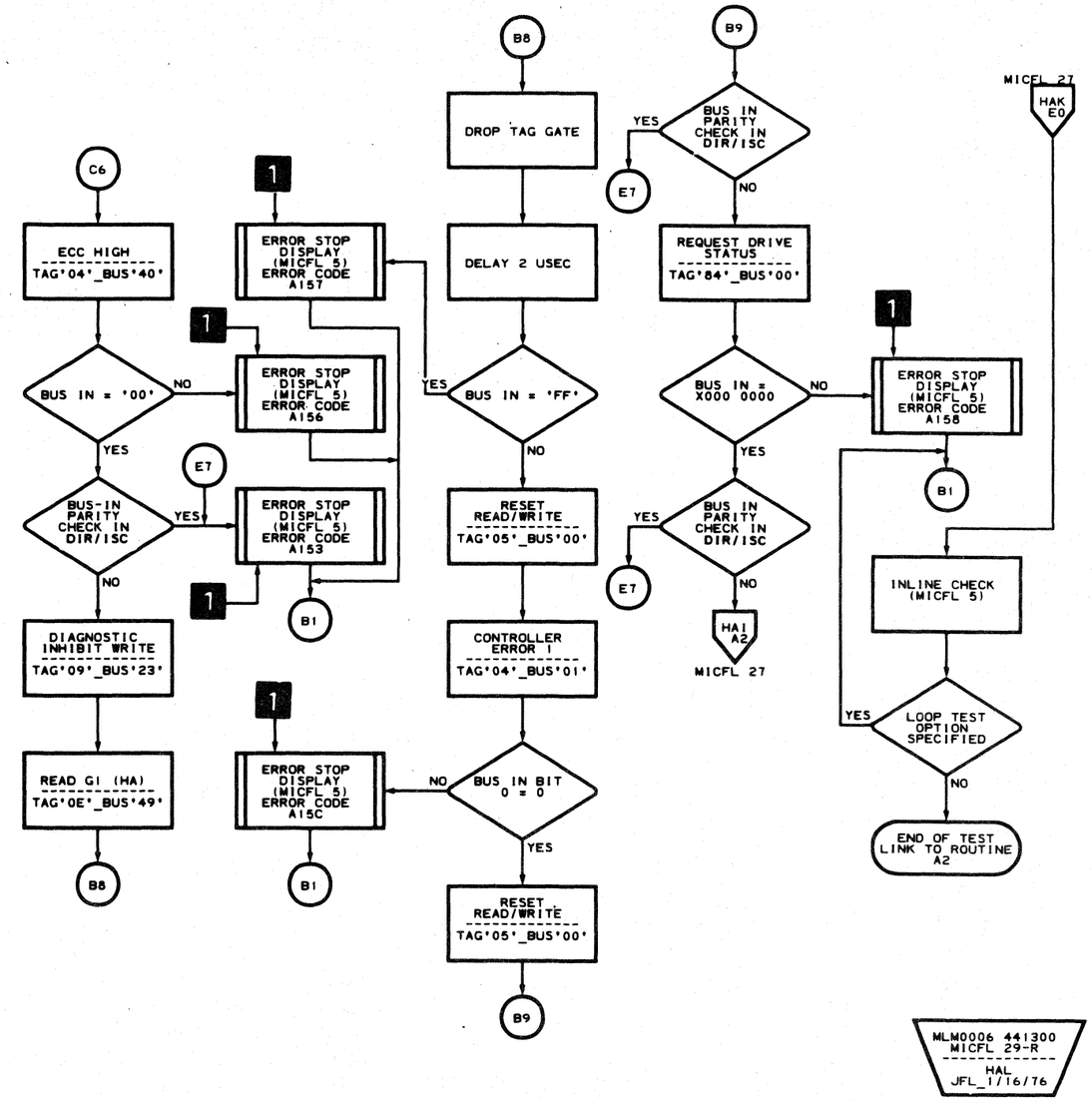
MICFL 27_L
HAI
JFL_1/16/76





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HAK
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MLM0006 441300
MICFL 29-R
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JFL_1/16/76

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ROUTINE A2 — 3350 DRIVE INTERFACE AND LOGIC TESTS

DESCRIPTION

Test 01. Drive Selection

Test 01 verifies that a 3350 drive can be selected by returning a Tag Valid response and a physical address when the drive is in CE mode. It also ensures that Drive Selection Error is active upon entry and that the drive is a 3350.

Test 02. Tag Bus and Bus Out Parity Check

Test 02 verifies that Tag Bus Parity check and Bus Out Parity check can be forced on and then reset when a Device Interface Check command is issued. It also verifies that Drive Interface check is forced on when either Tag Bus or Bus Out Parity check is active.

Both parity checks are forced on by special diagnostic commands.

Tag '09' Bus '21' inverts Tag Bus Parity in the drive.
Tag '09' Bus '22' inverts Bus Out Parity in the drive.

Test 03. Bus Out/Bus In Wrap

Test 03 verifies that a data path exists between Bus Out and Bus In on the 3350 drive. The test uses the Difference Counter for testing the integrity of the data path. If a failure occurs in the Difference Counter, the test automatically switches to the Head Address Register (HAR) and uses it as the test vehicle. If both HAR and Difference Counter fail, the test halts with an error.

The following values are placed on Bus Out:

a. All 0s
b. All 1s
c. A sliding 1s pattern

Test 04. Drive Selection/Rejection

Test 04 verifies that a drive cannot be selected when Bus Out Bit 4 is active during a selection operation (Tag '83'). This bit prevents a physical address from being returned to the storage control for any drive. The test also forces a Drive Selection Error by selecting the CE drive and any one of eight customer drives (two drives simultaneously selected).

Test 05. Drive Tag Valid/Normal End

Test 05 verifies that the storage control receives a Tag Valid response and Normal End for all the 3350 drive tags except Tag '85'. If Tag Valid is not received for a given tag, the test examines Tag Bus and Bus Out Parity checks to see if either one is active.

Test 06. Drive No Tag Valid

Test 06 verifies that Tag Valid is not returned for drive Tags '8A' — '8F' when Tag Bus Parity has been inverted. Tag Bus Parity is inverted by a diagnostic command (Tag '09' Bus '21').

Test 07. Drive Bus In Parity Check

Test 07 verifies that drive Bus In Parity checks can be forced on and then reset with the Reset Controller Command. The drive Bus In Parity check is inverted by a diagnostic command (Tag '09' Bus '20'). The test also checks for the presence of the fixed heads for proper operation. The ability to set and reset the direction bit with the Set Difference High command is checked.

Test 08. Head Address Register

Test 08 verifies that the Head Address Register (HAR) can be set to any value. The HAR is set to all 0s, all 1s, a sliding 1s pattern, and a sliding 3s pattern. Every time HAR is sensed, Bus In is examined for a parity check.

Test 09. Difference Counter Test (Part 1)

Test 09 verifies that the Difference Counter can be set to any value. The Difference Counter is set to all 0s, all 1s, a sliding 1s pattern, and a sliding 3s pattern. Every time the Difference Counter is sensed, Bus In is examined for a parity check.

Test 10. Difference Counter Test (Part 2)

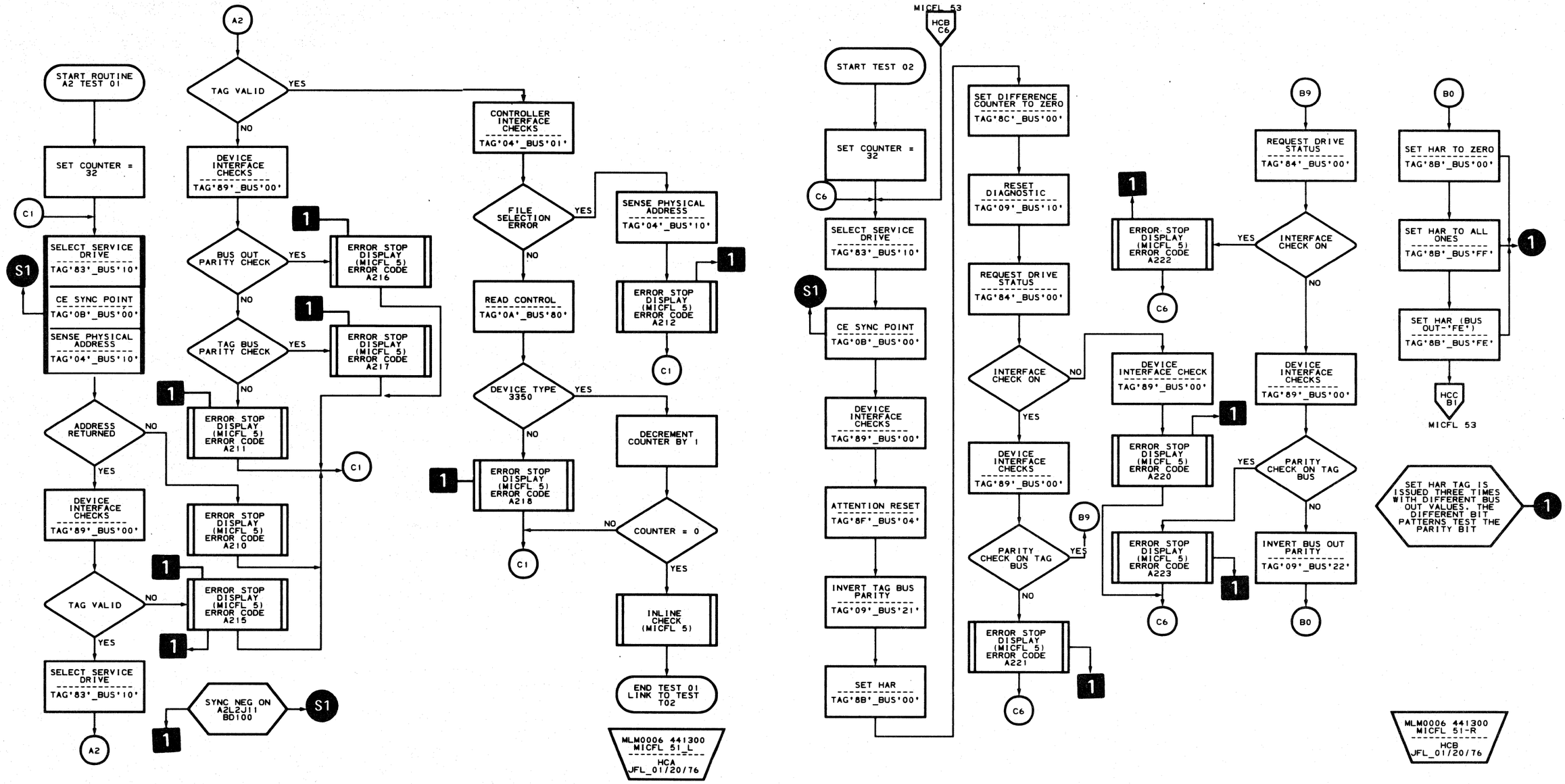
Test 10 verifies that the Difference Counter can be decremented properly by a special diagnostic command (Tag '8A' Bus '01').

Test 11. Optional Cylinder Address Register

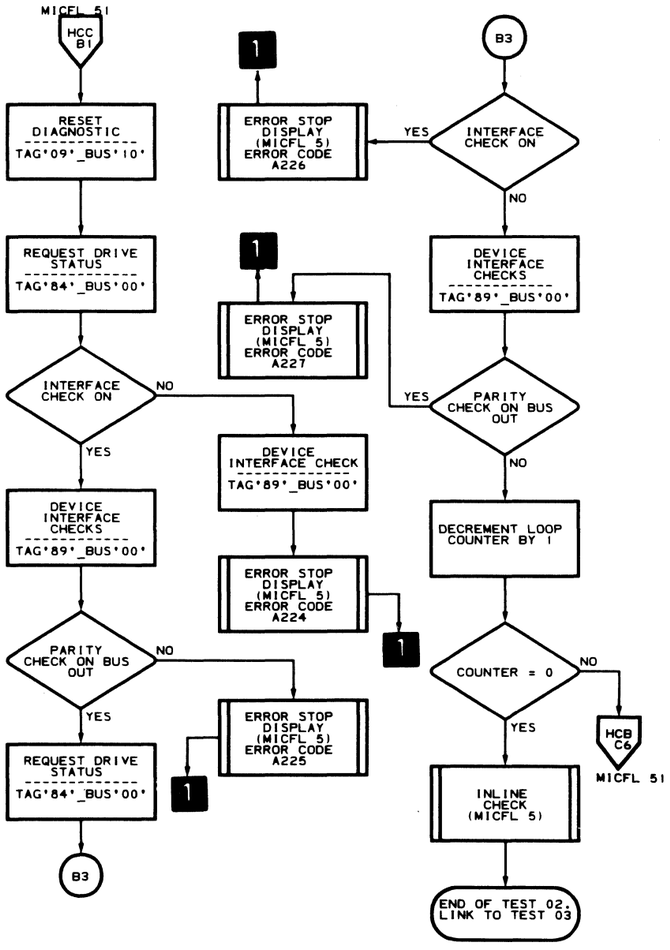
Test 11 verifies that the Cylinder Address Register (CAR) can be set to any value. The CAR is set to all 0s, all 1s, a sliding 1s pattern, and a sliding 3s pattern. Every time the CAR is sensed, Bus In is examined for a parity check.

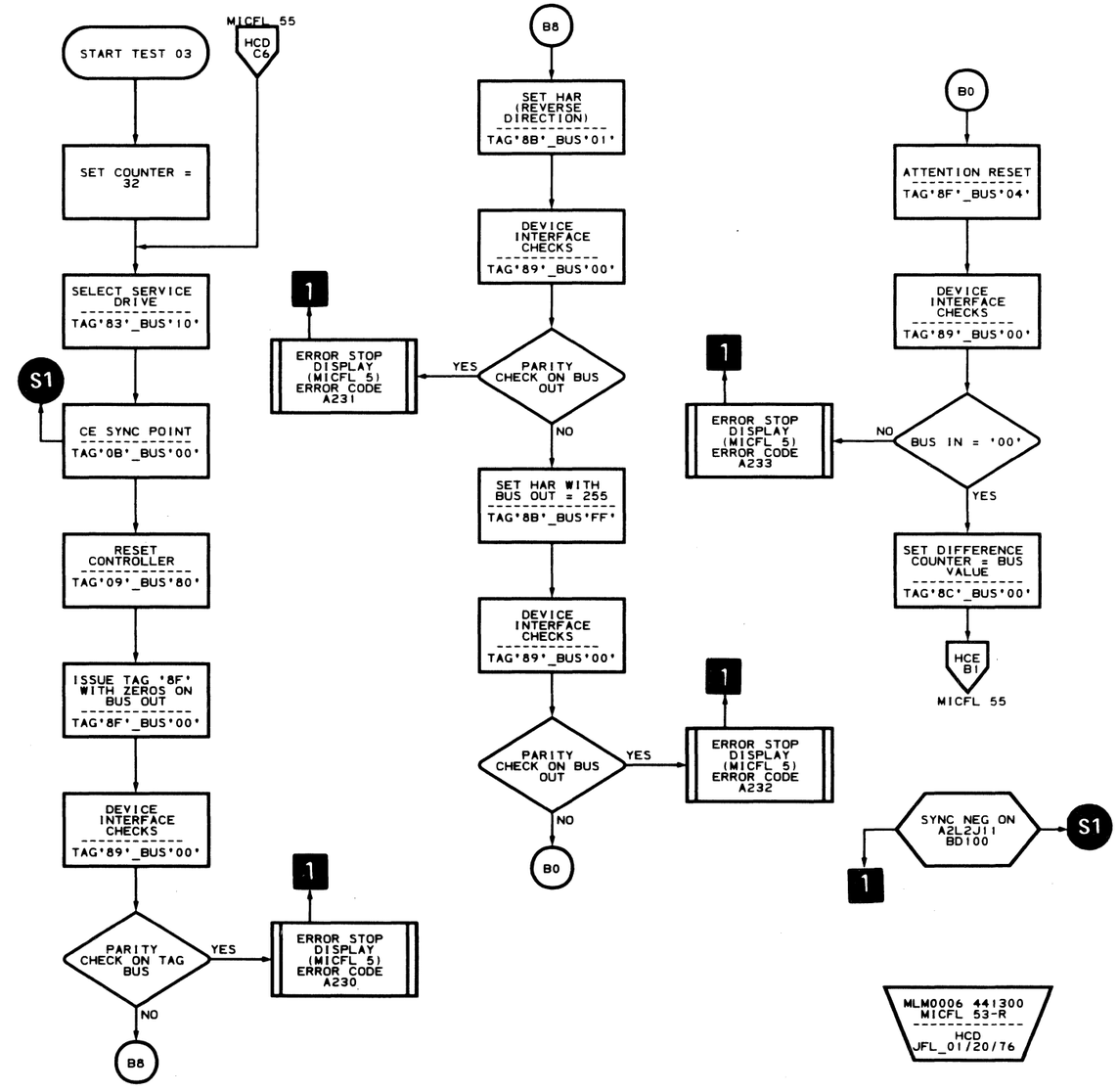
OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 20 for parameter entry.



ROUTINE A2 – DRIVE INTERFACE AND LOGIC TESTS





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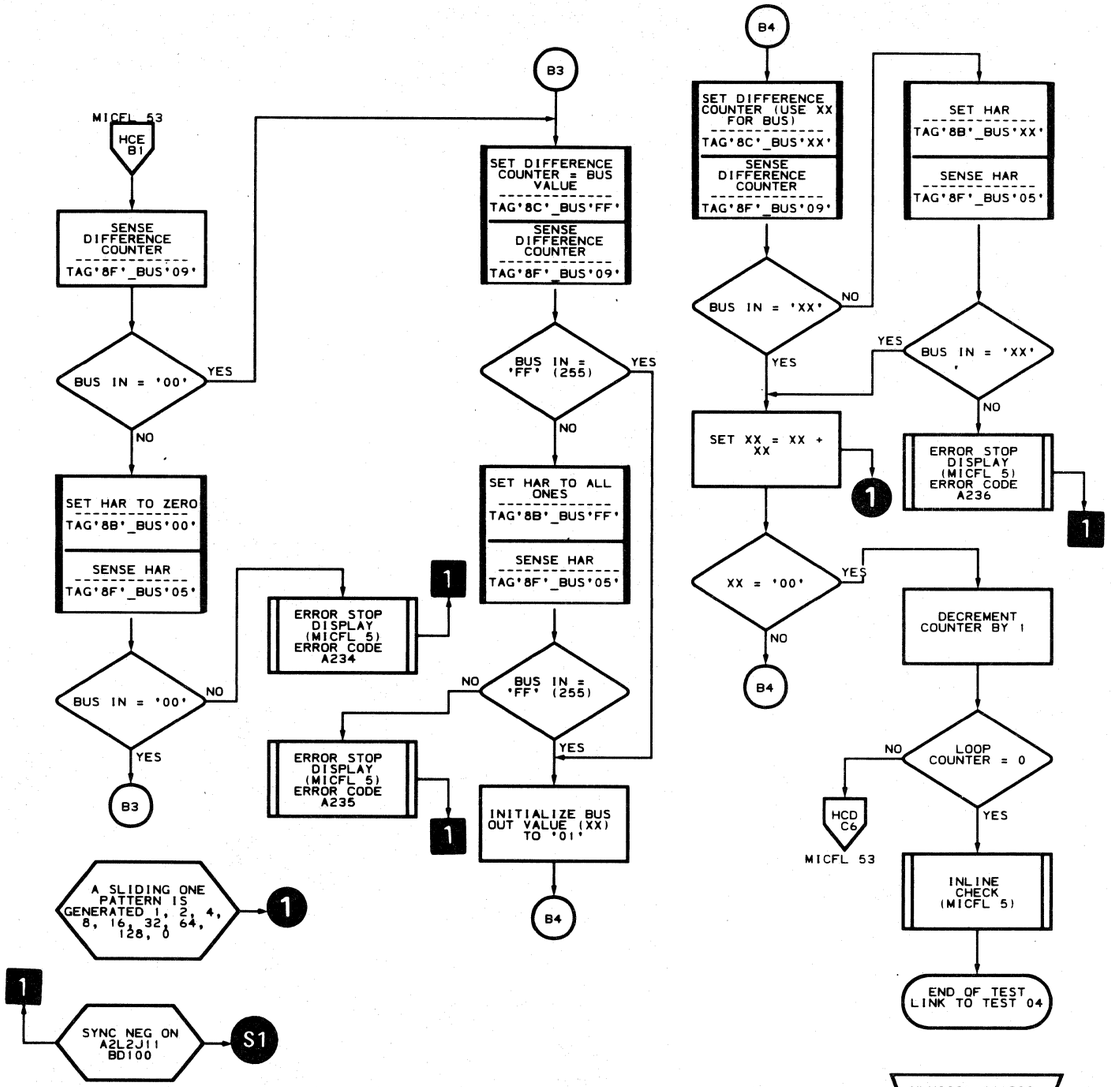
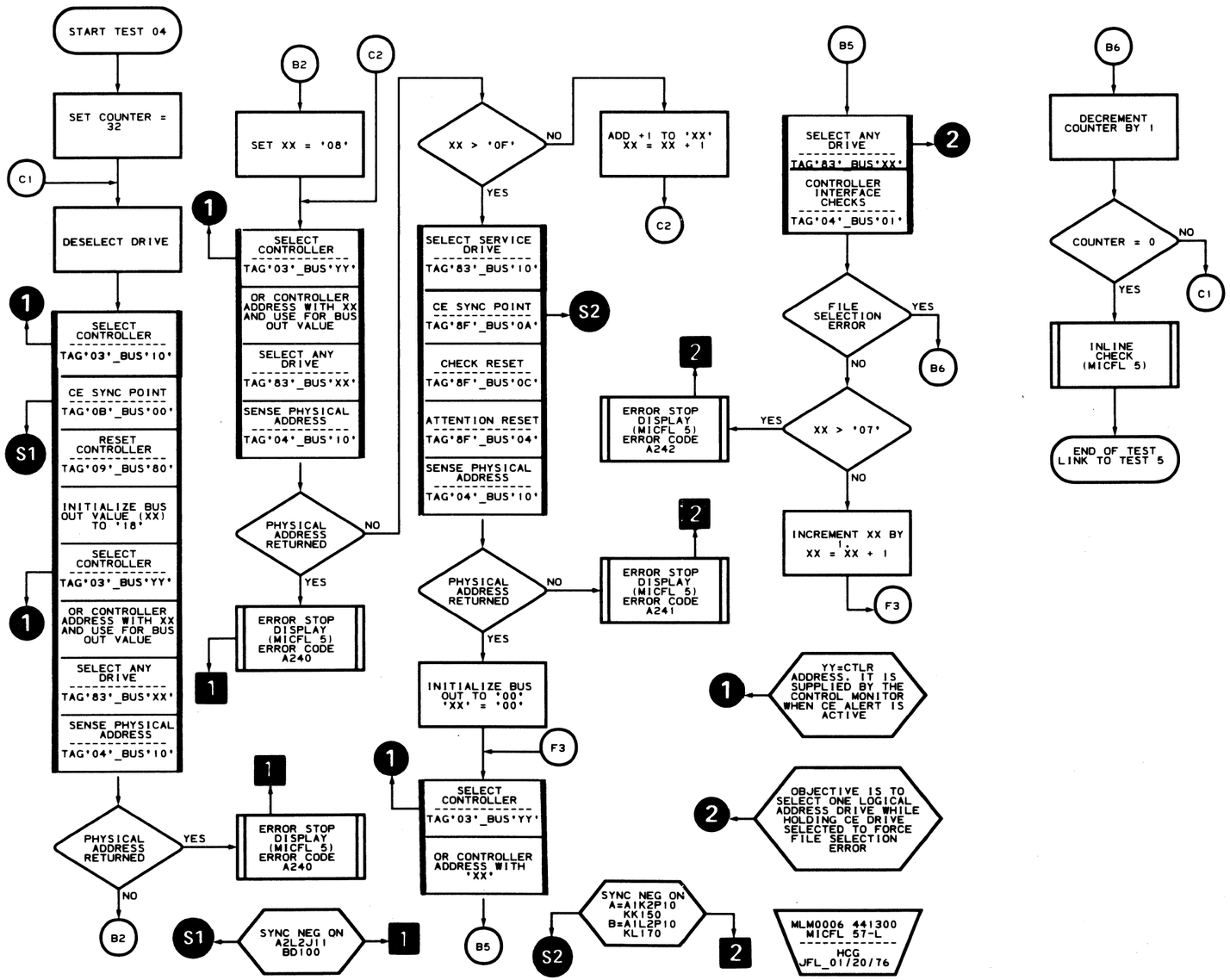
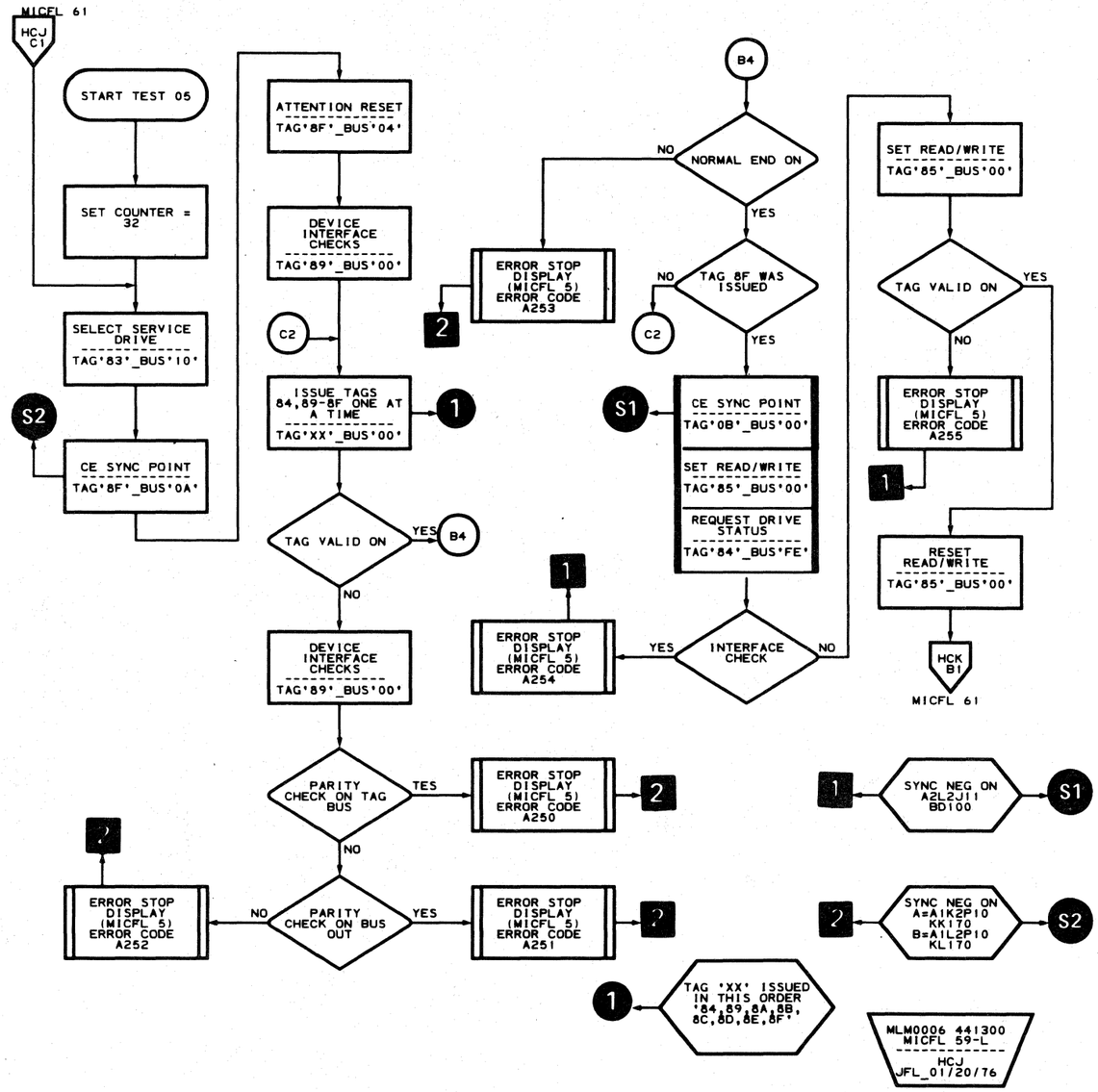
JFL_01/20/76

MLM0006 441300
MICFL 53-R
HCD
JFL_01/20/76

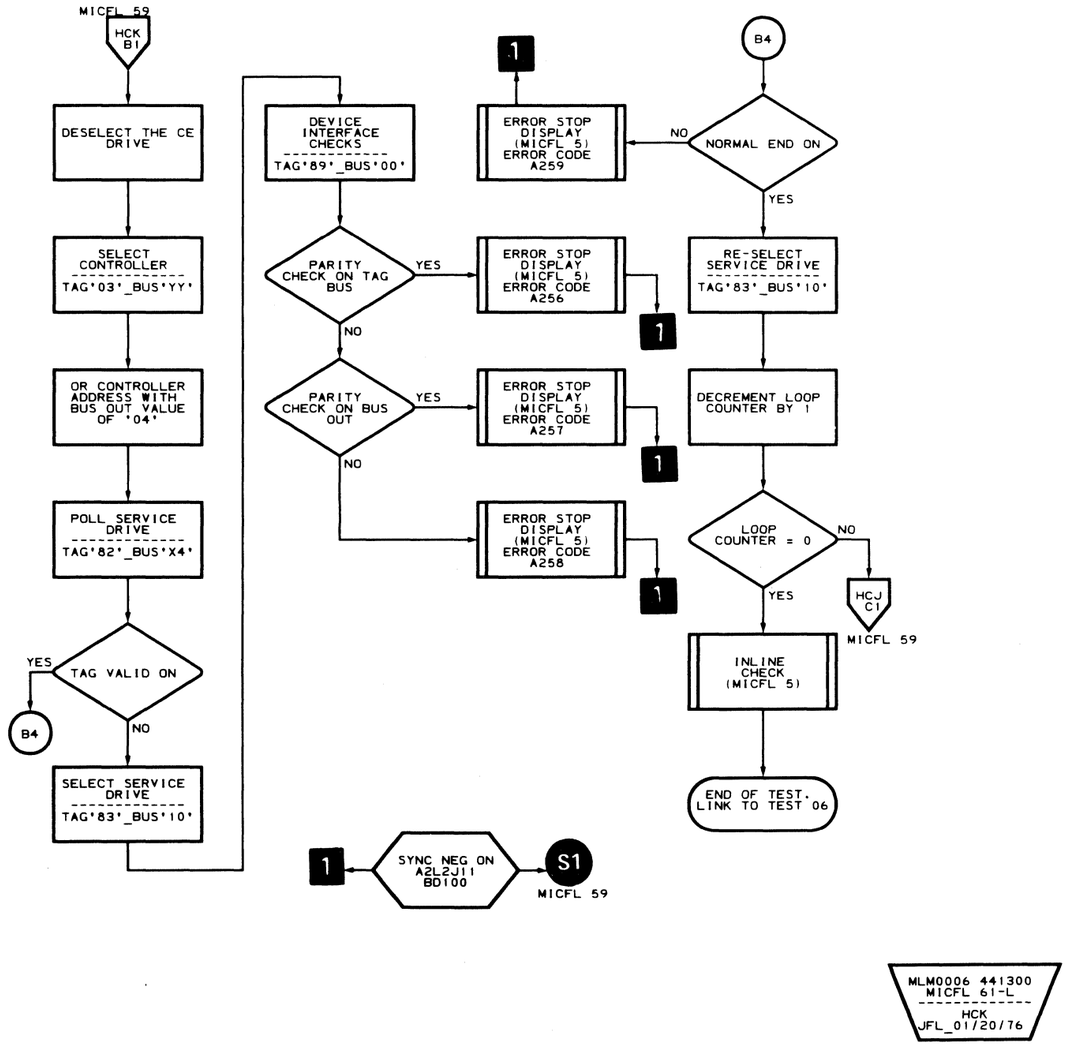


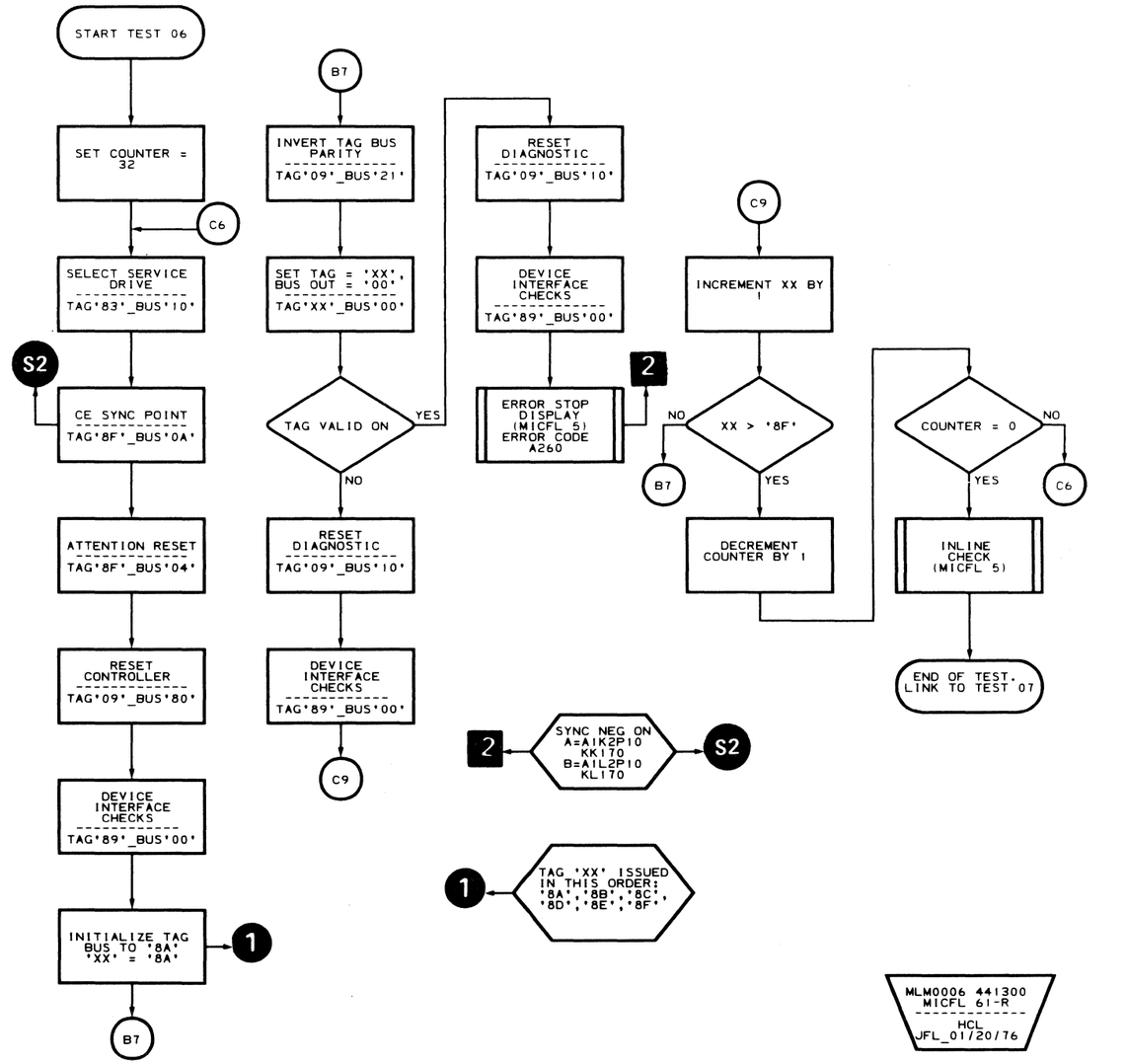
ROUTINE A2 – DRIVE INTERFACE AND LOGIC TESTS

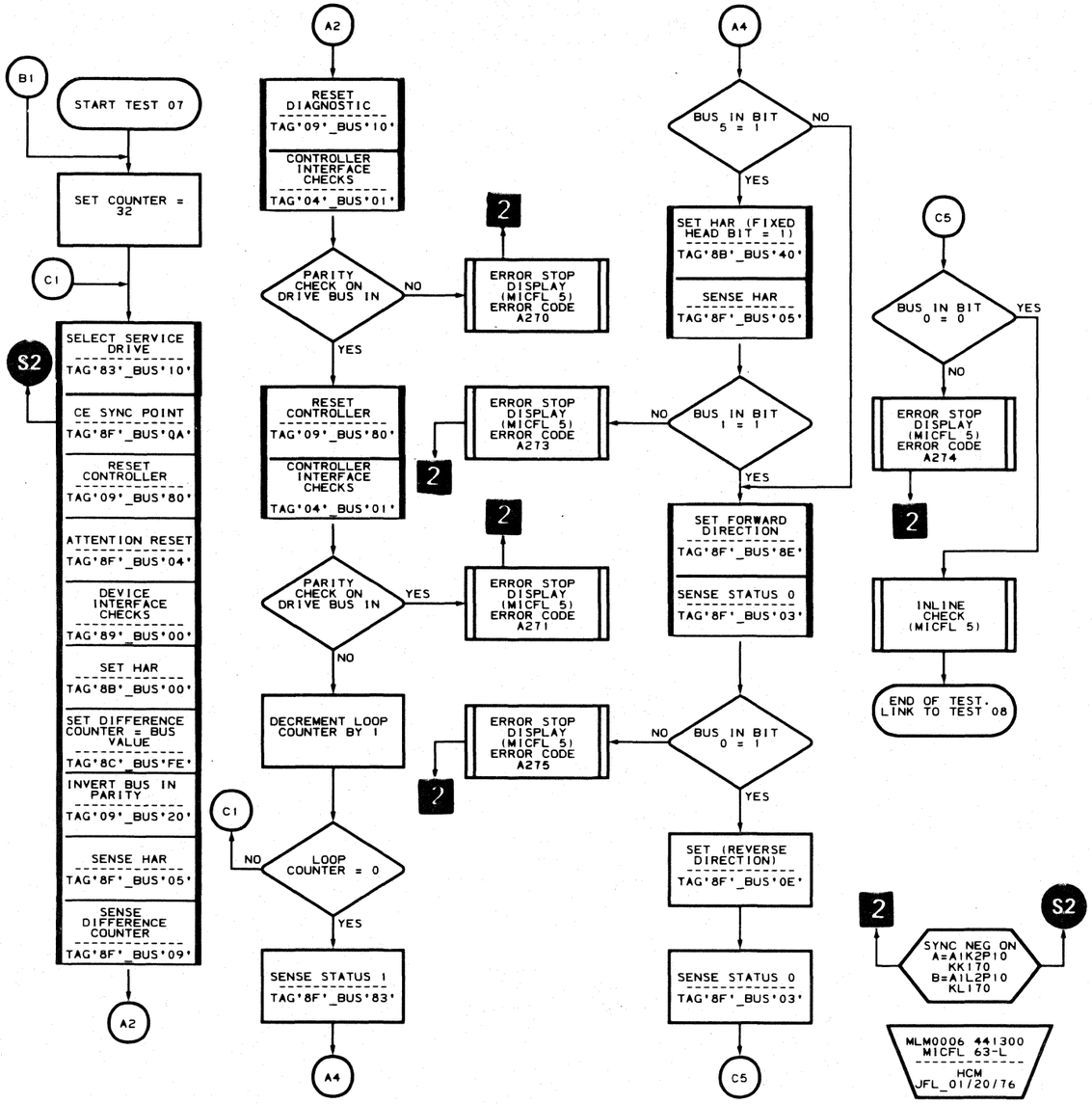


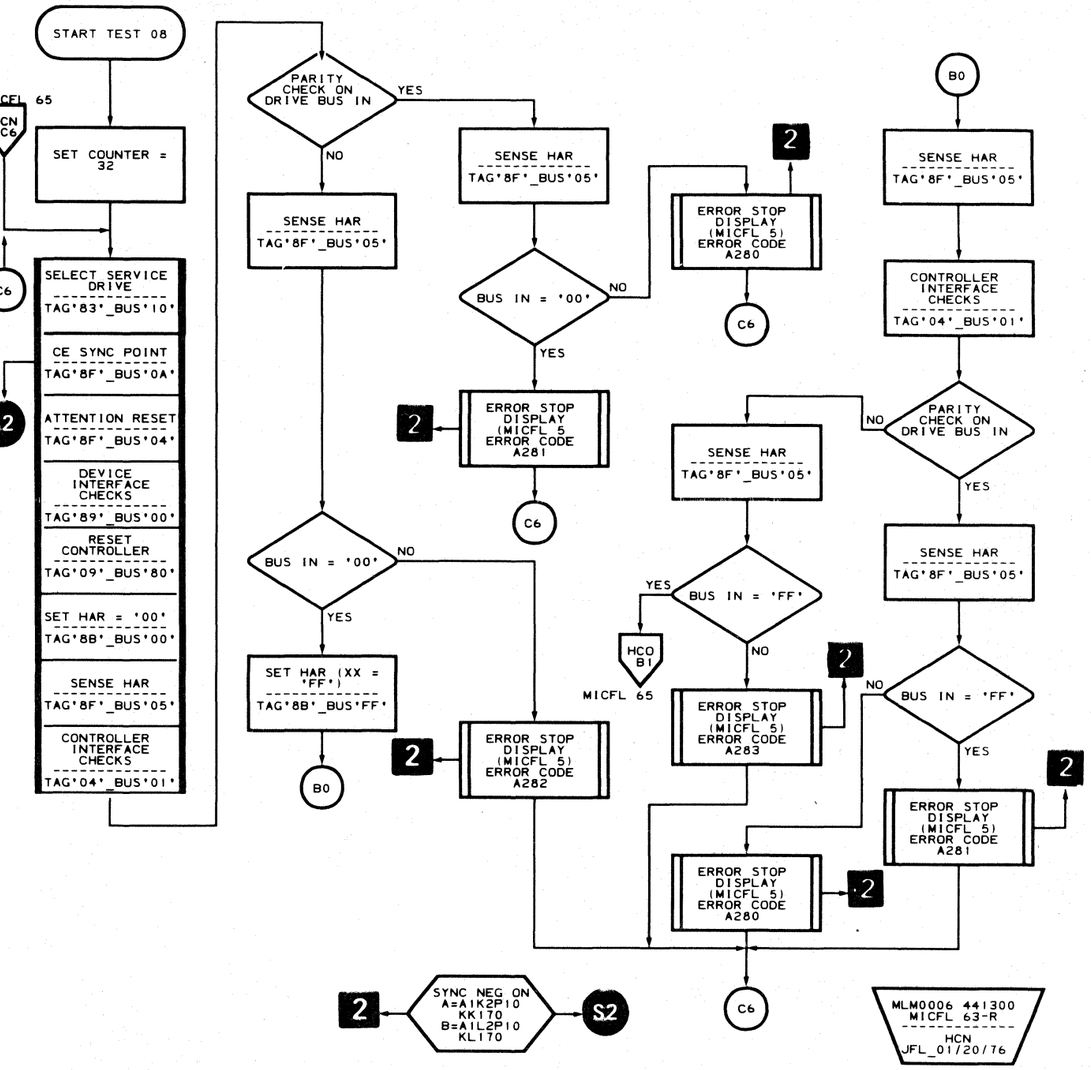


ROUTINE A2 – DRIVE INTERFACE AND LOGIC TESTS

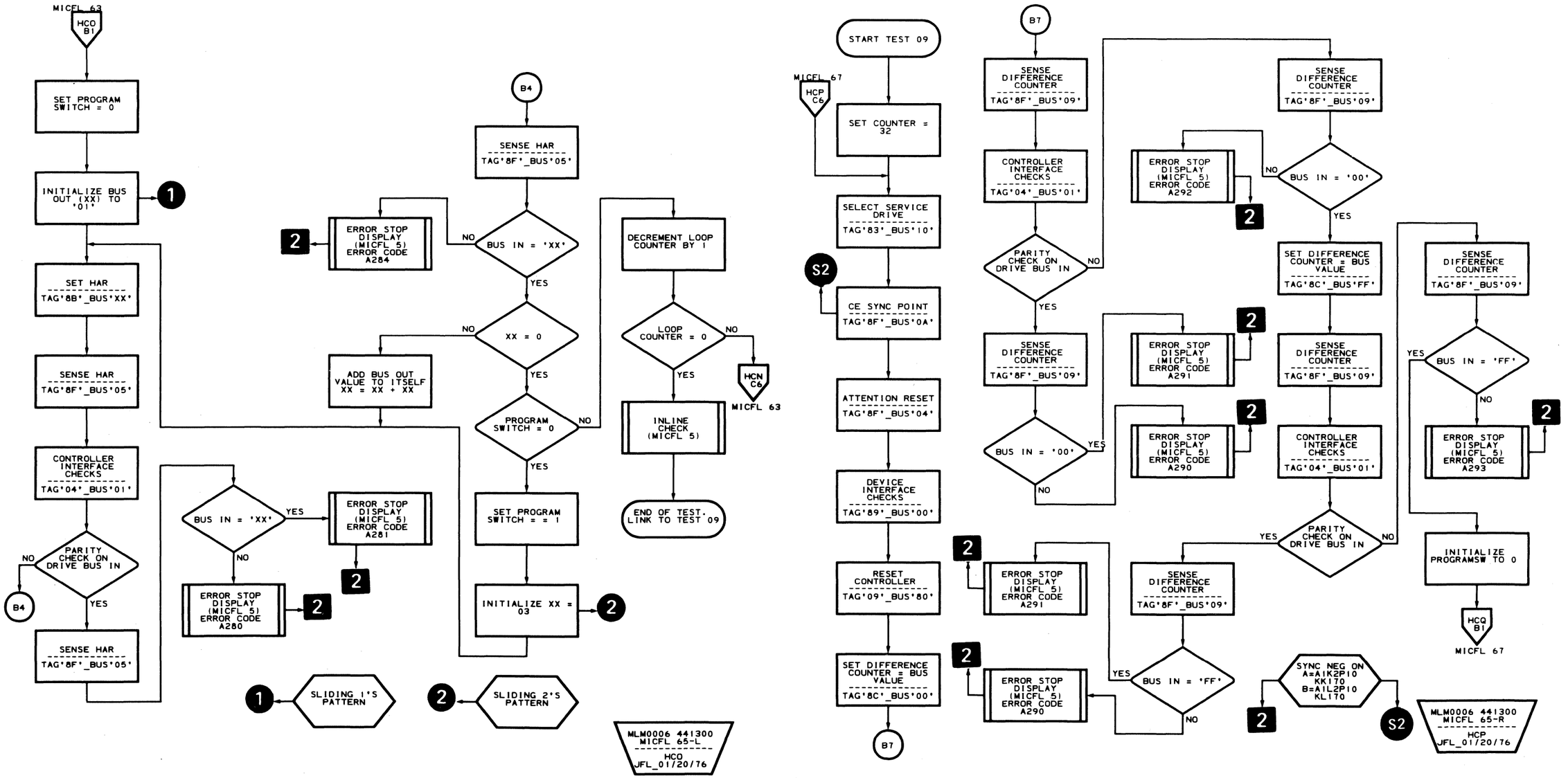


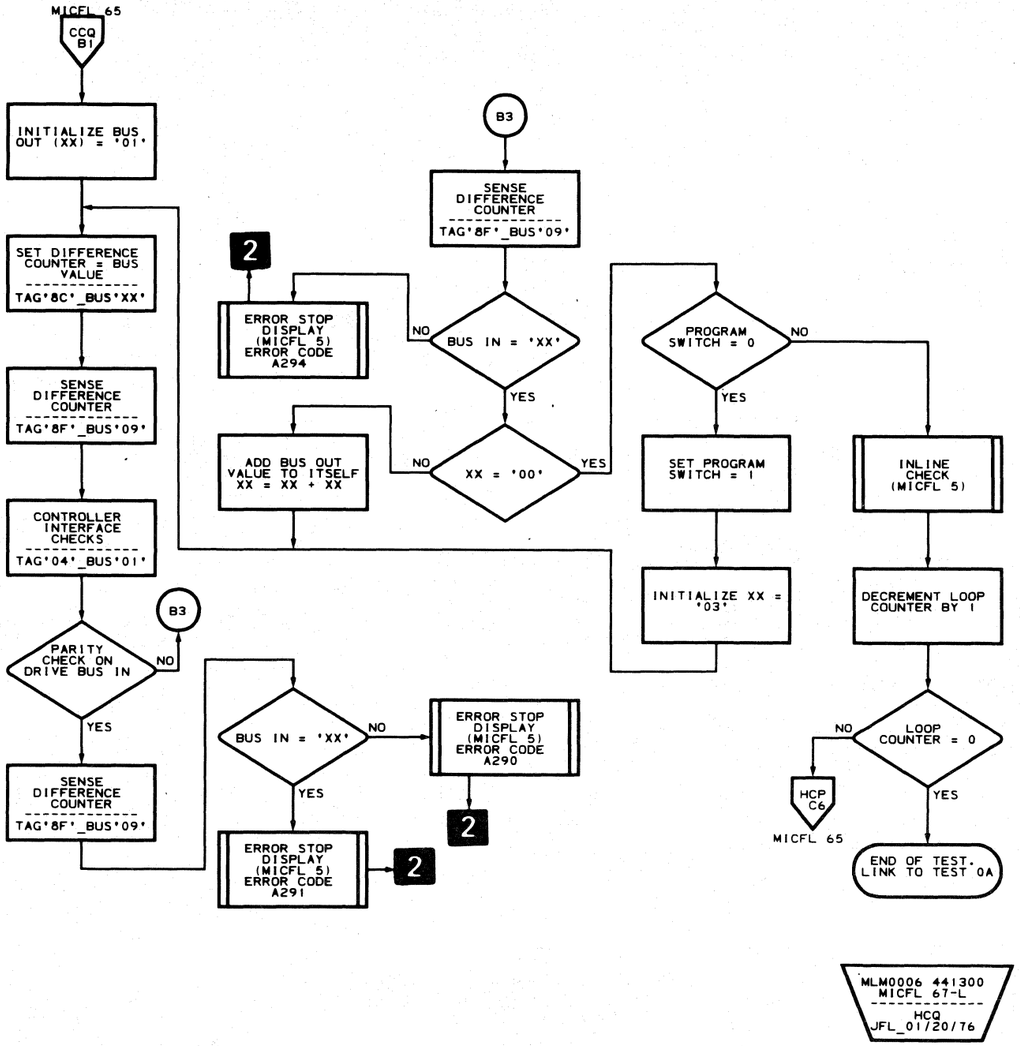


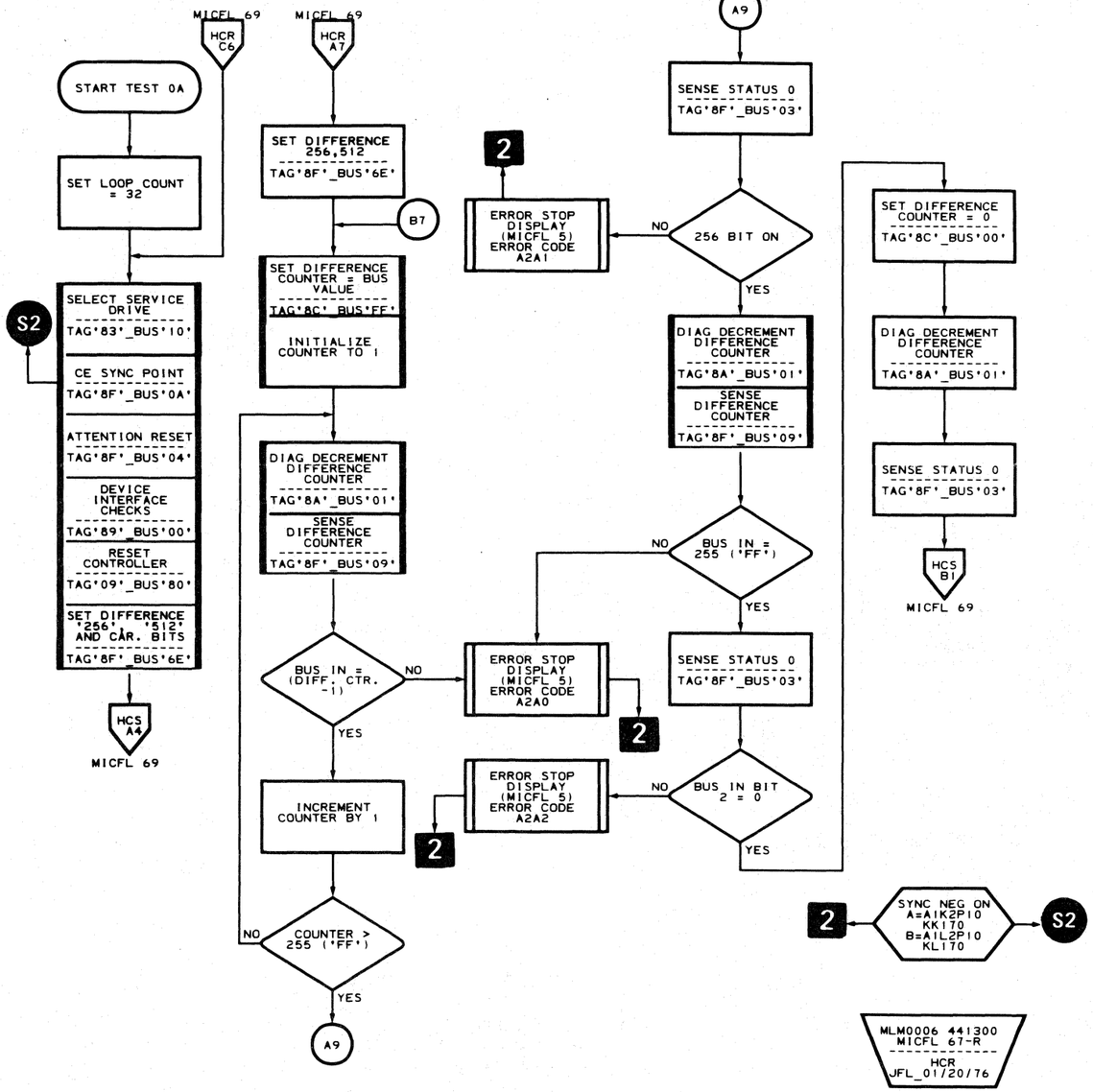




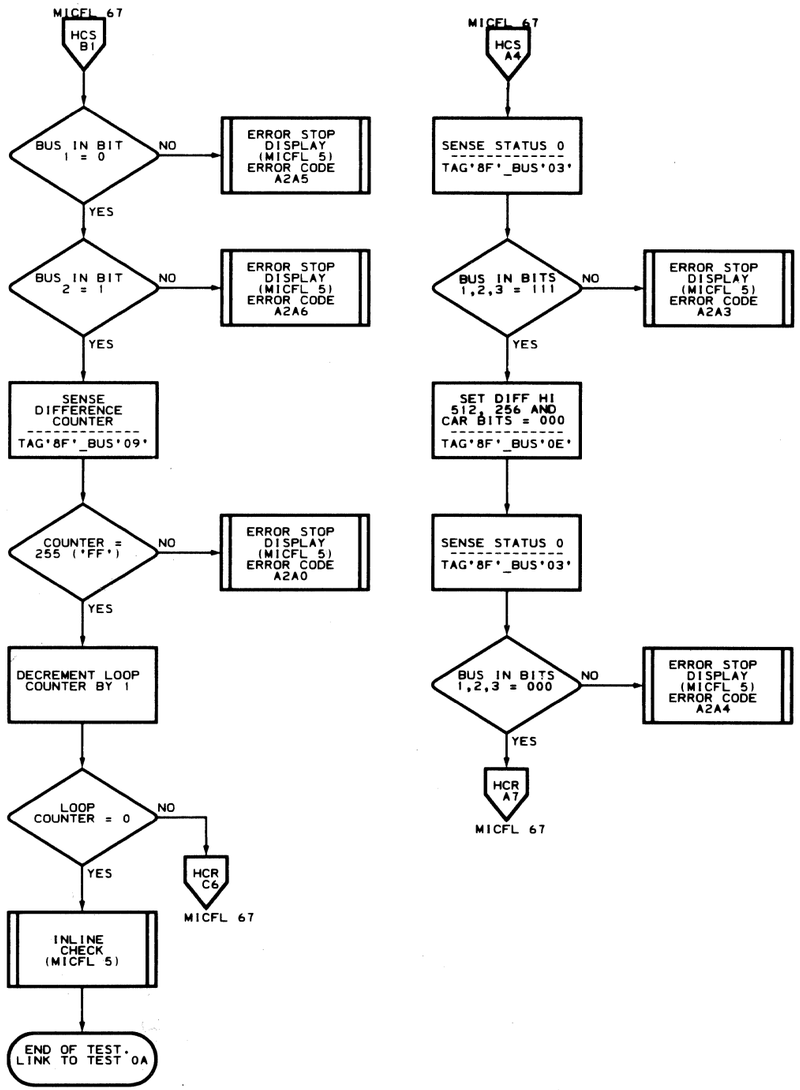
ROUTINE A2 – DRIVE INTERFACE AND LOGIC TESTS

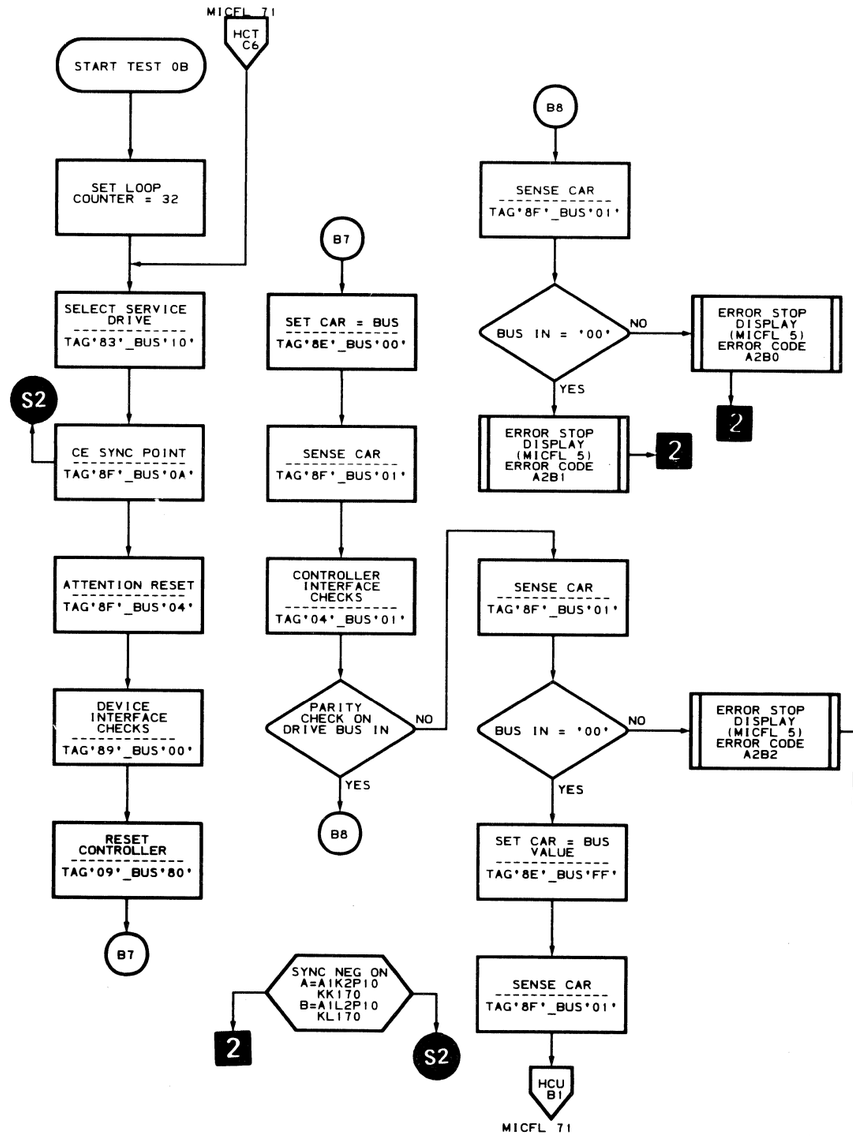






ROUTINE A2 – DRIVE INTERFACE AND LOGIC TESTS





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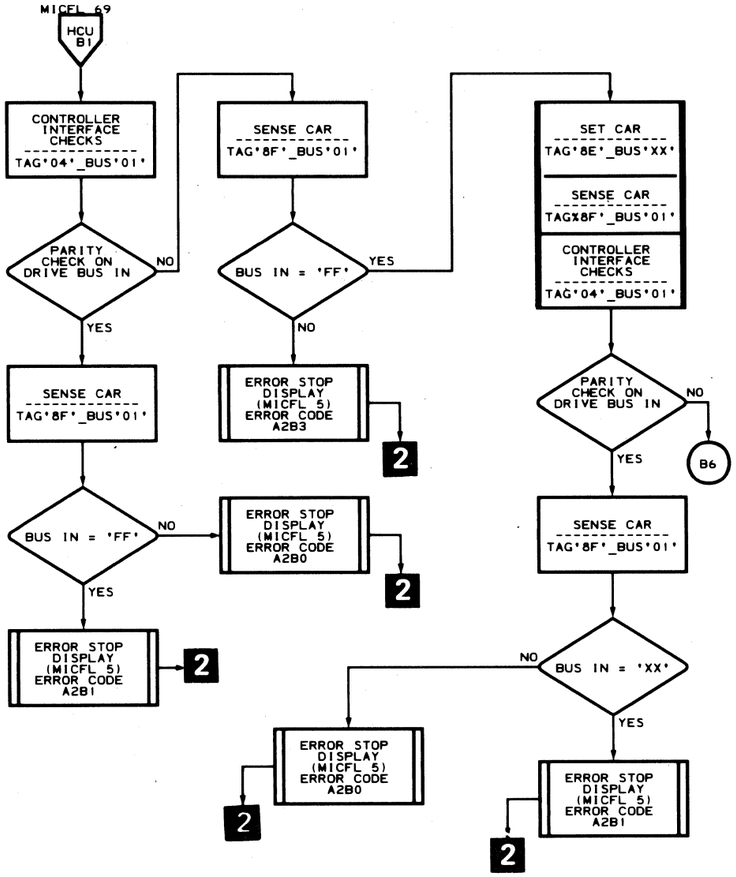
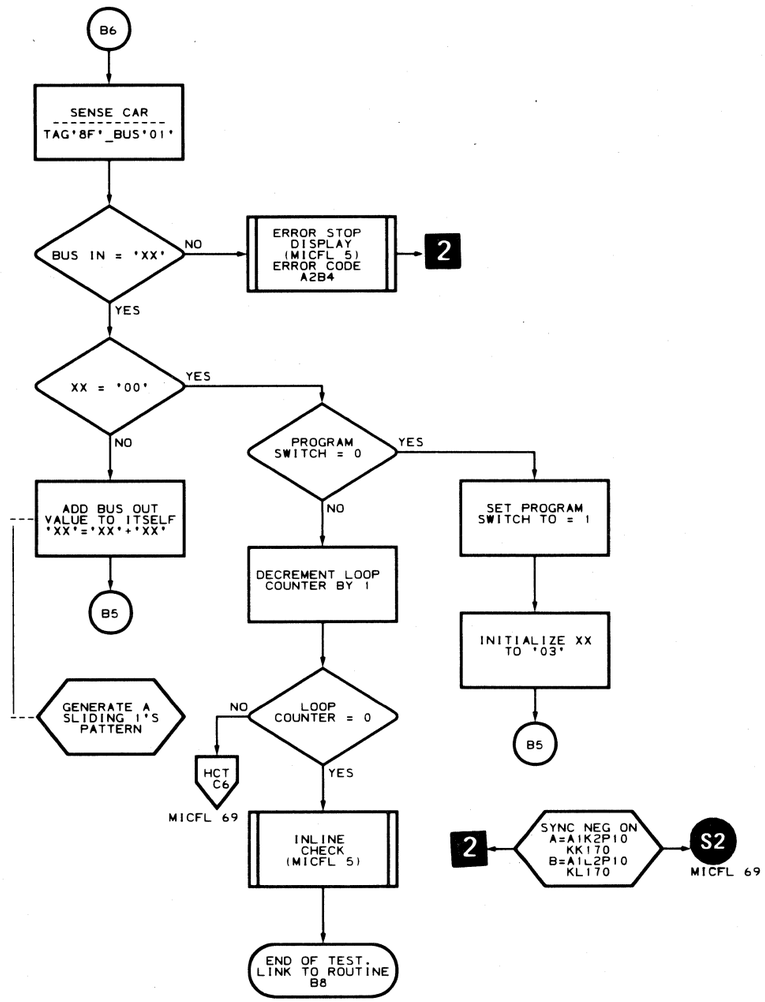
JFL_01/20/76

MLM0006 441300
MICFL 69-R
HCT
JFL_01/20/76





MLM0006 441300
MICFL 71-L
HCU
JFL_2/23/76

MLM0006 441300
MICFL 71-R
HCV
JFL_01/20/76

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L

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ROUTINE A5 – 3350 DRIVE INDEX AND SECTOR TESTS

DESCRIPTION

Test 01. Target Register

Test 01 first checks the 3350 drive RPS function. The test sets the Target Register to all 0s, all 1s, a sliding 1s pattern, and a sliding 2s pattern. Every time the Target Register is sensed, Bus In is examined for a parity check.

Test 02. Index

Test 02 performs the following functions:

1. Verifies that an Index pulse was received within 25 milliseconds.
2. Measures the width of the Index pulse as seen by the drive and verifies that the width is between 16 and 18 microseconds.
3. Measures the time between two Index Marks as seen by the drive and verifies that it is between 16.2 and 17.2 milliseconds.
4. Verifies that the Index Check functions properly.

Test 03. Force Multichip Check

Test 03 forces a Multichip Check by selecting an even head and issuing a special diagnostic command (Tag '8A' Bus '02'). The test also verifies that Read/Write Check becomes active because more than one head is selected. It also verifies that Multichip Check and Read/Write Check are reset by a Check Reset operation.

Test 04. Force Sector Compare Check

Test 04 verifies that a Sector Compare Check can be forced on and then reset. The test also verifies that an Attention is generated by the Sector Compare Check when polling the drive.

Test 05. Sector Compare Attention

Test 05 verifies that an Attention is generated from a Sector Compare when polling the drive. The test also verifies that Busy is received in response to a Set Target command.

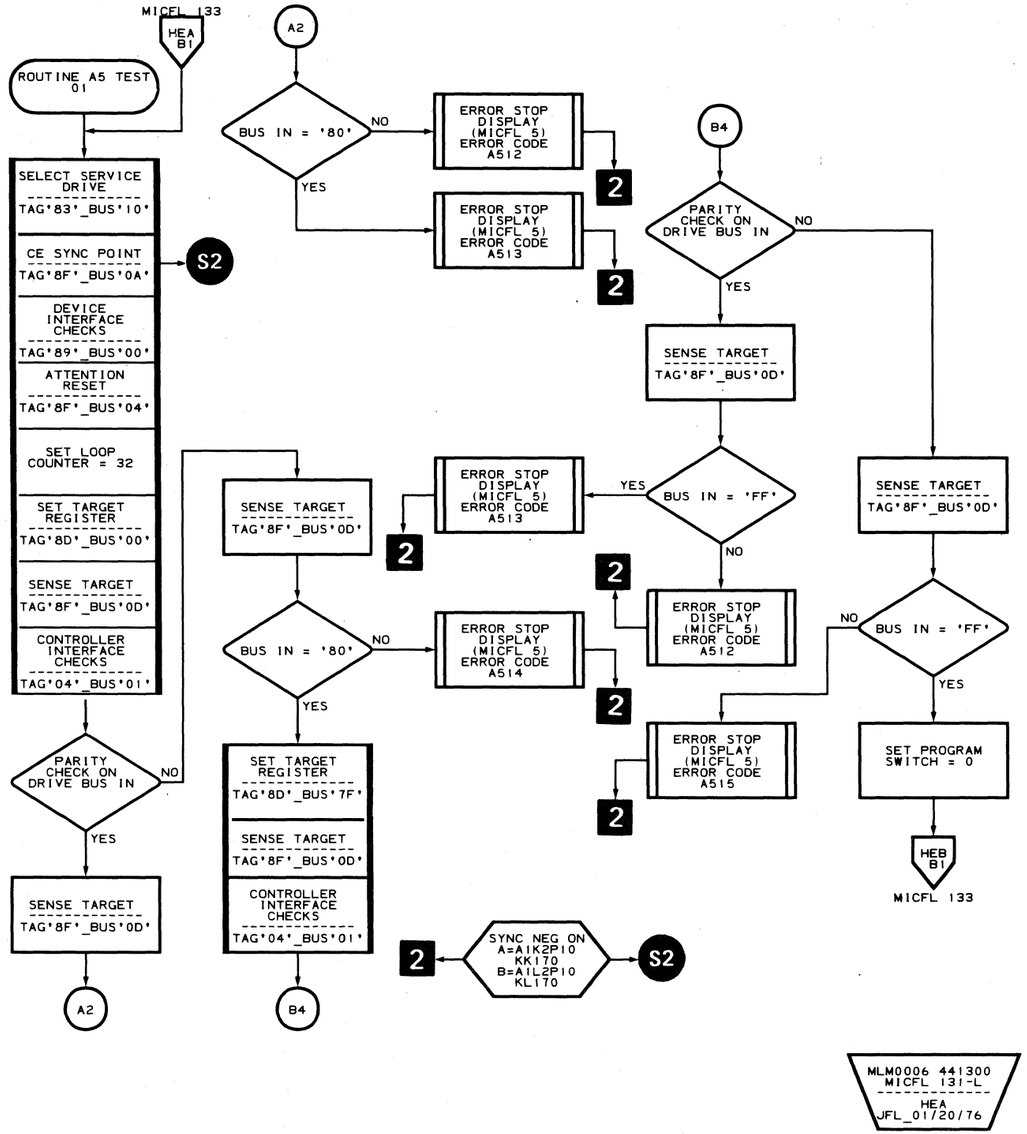
Test 06. Sector Compare

Test 06 verifies that Sector Compare is received for sectors 1, 2, 4, 16, 32 64, and 127. It also performs the following functions:

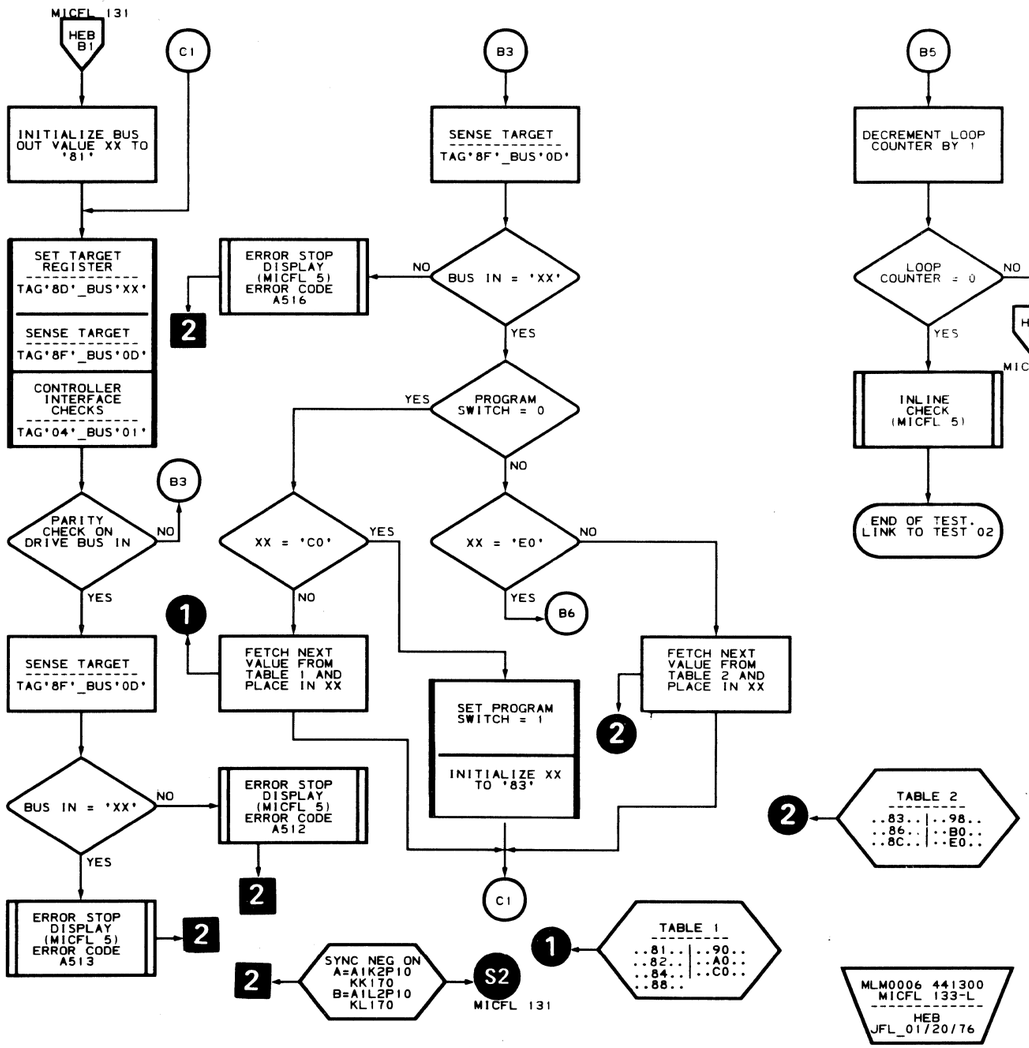
1. Measures the duration of the Sector Compare and verifies it to be between 126 and 134 microseconds. This applies to all of the previously mentioned sectors except sector 127.
2. Verifies that the Transfer Sector command transfers the contents of the Sector Counter to the Target Register for sectors 0 and 127.

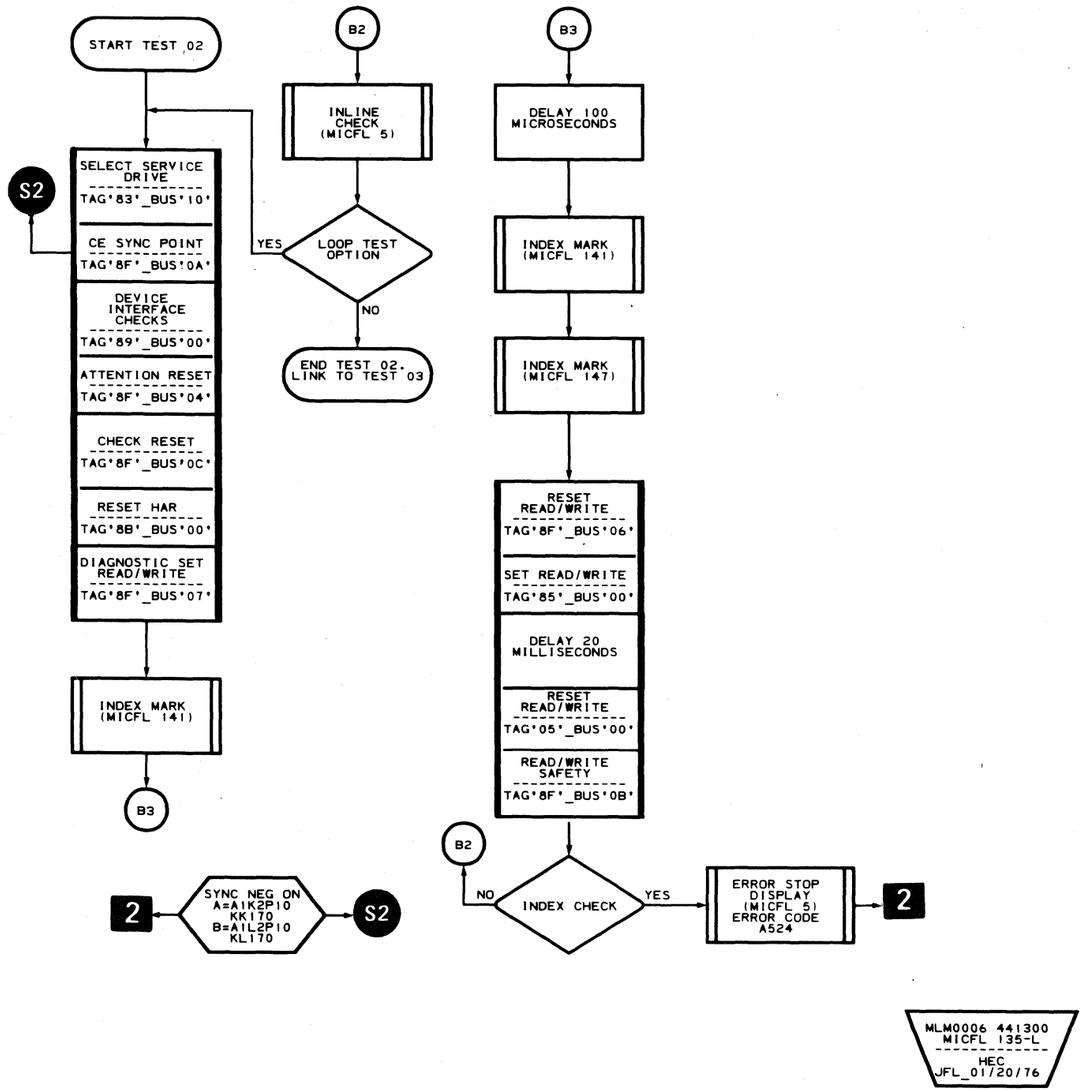
OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 24 for parameter entry.

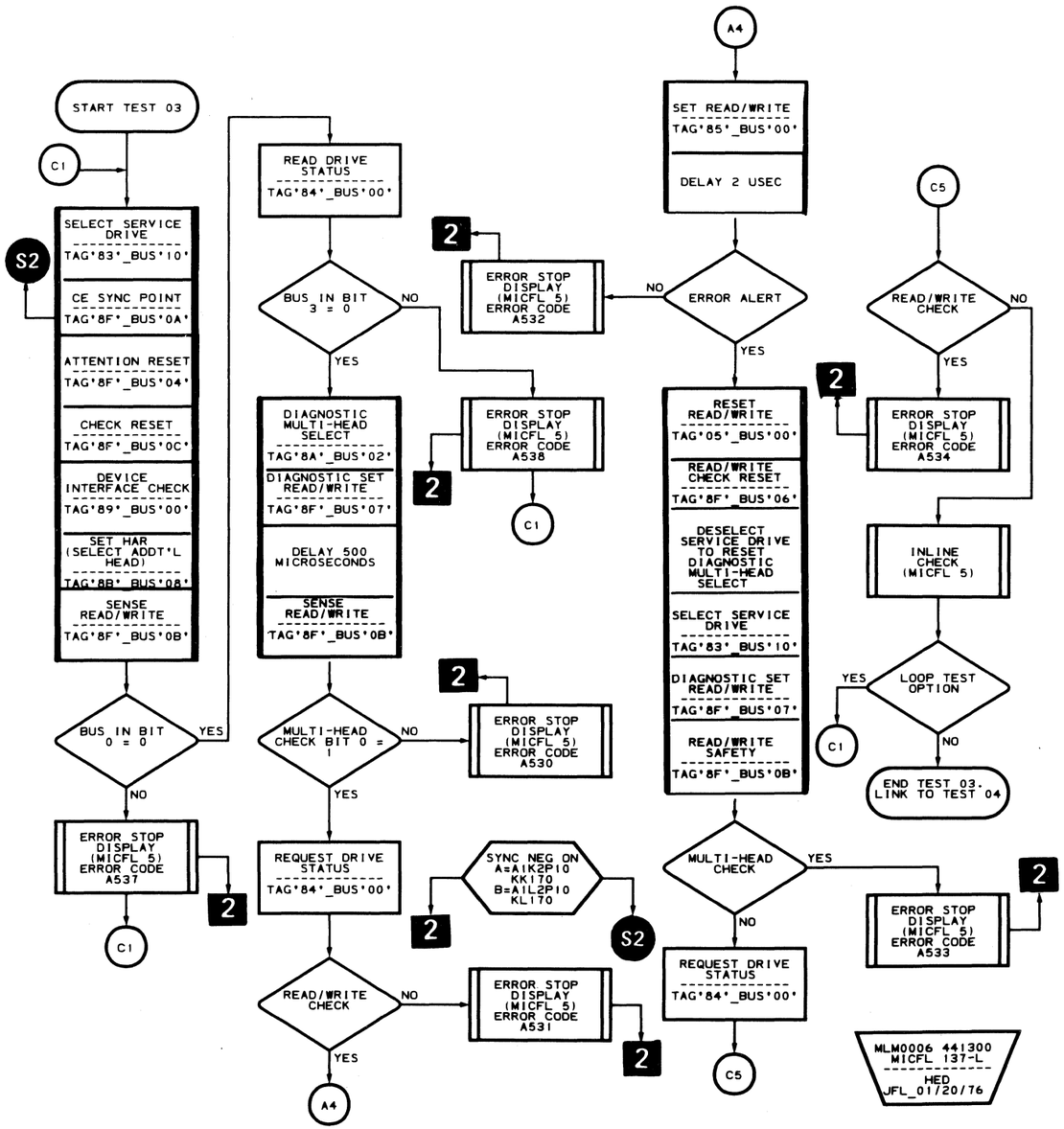


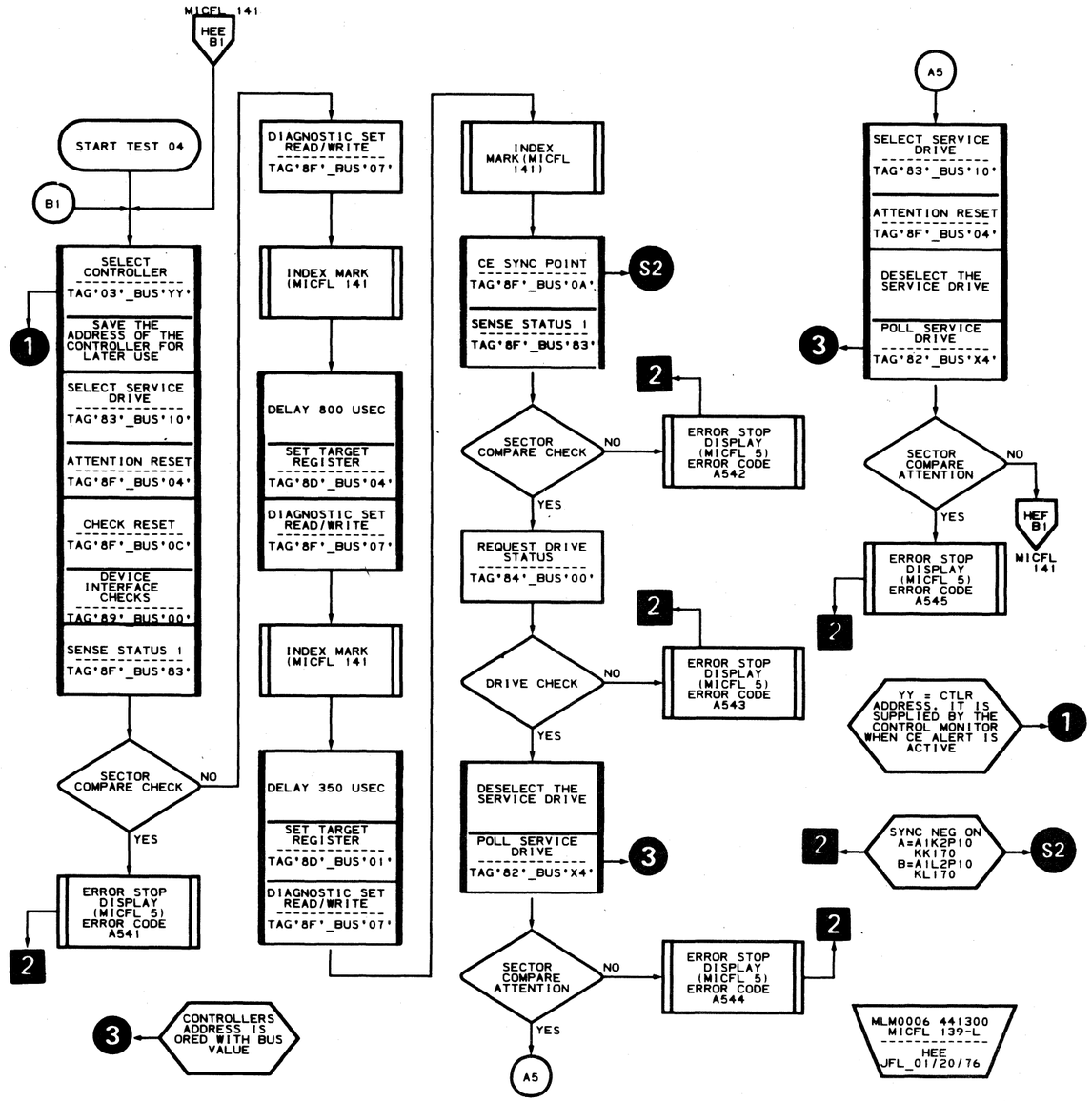
ROUTINE A5 – DRIVE INDEX AND SECTOR TESTS



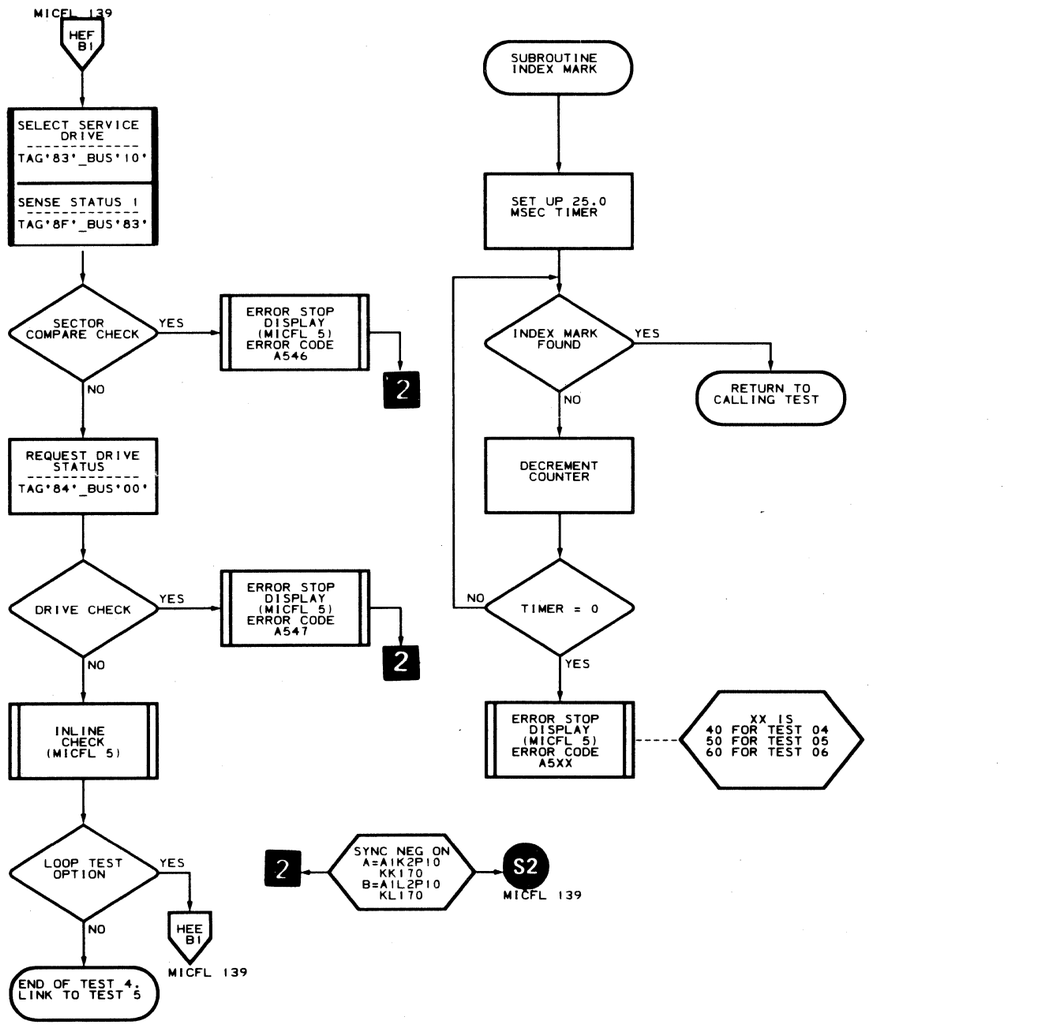


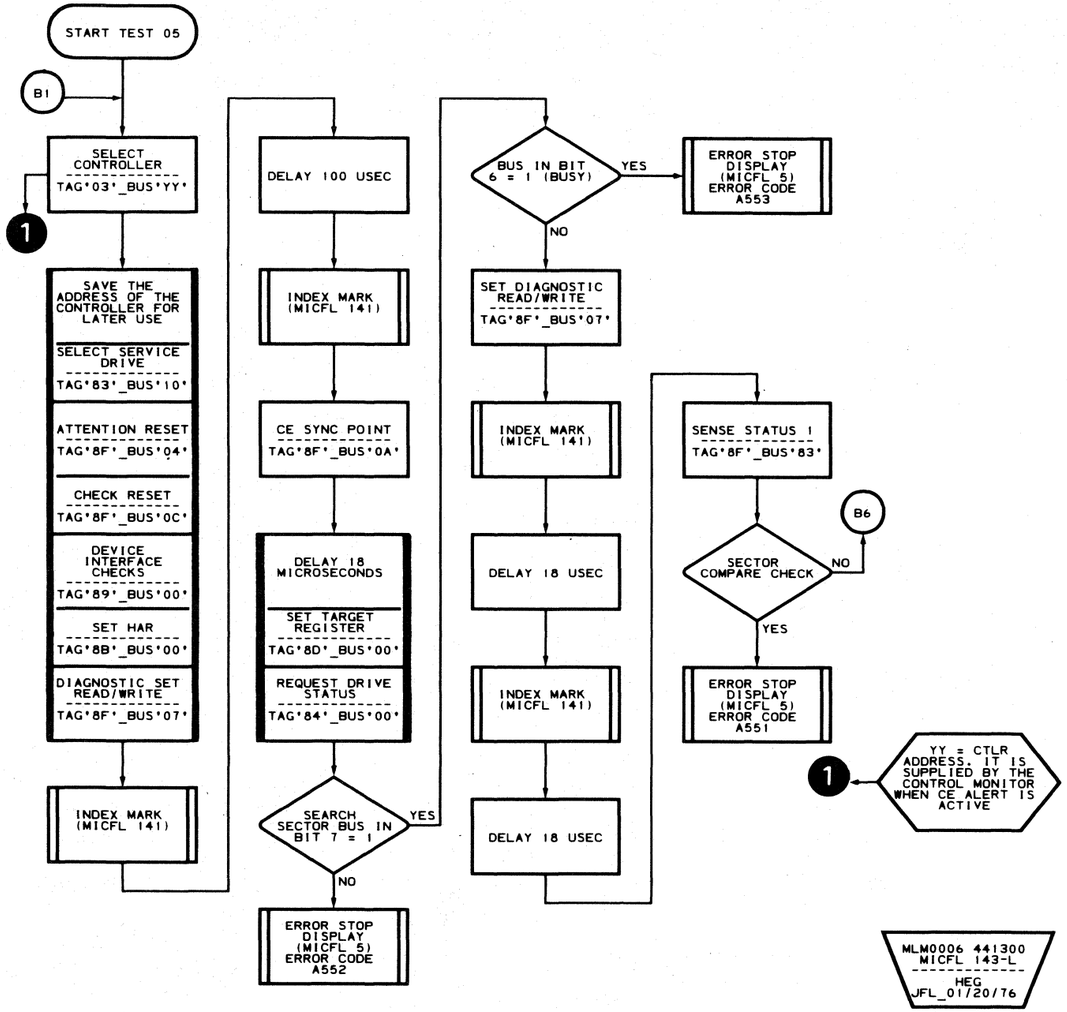
ROUTINE A5 – DRIVE INDEX AND SECTOR TESTS

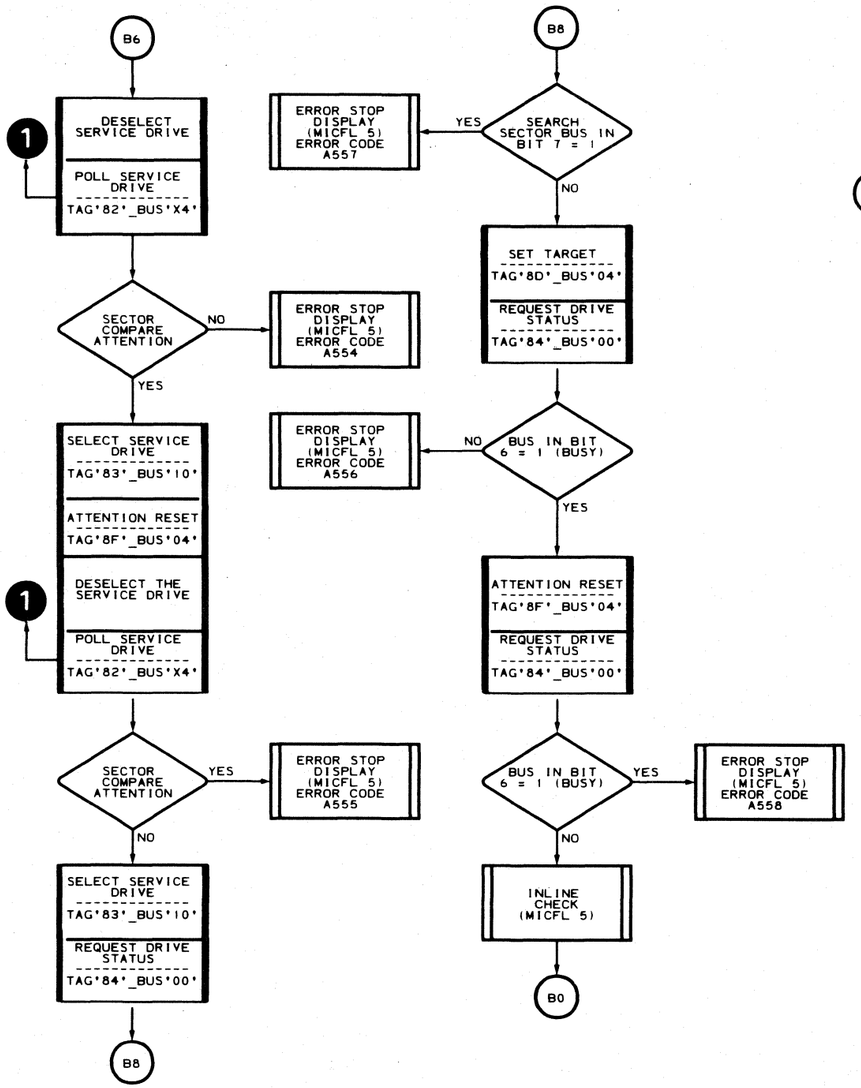




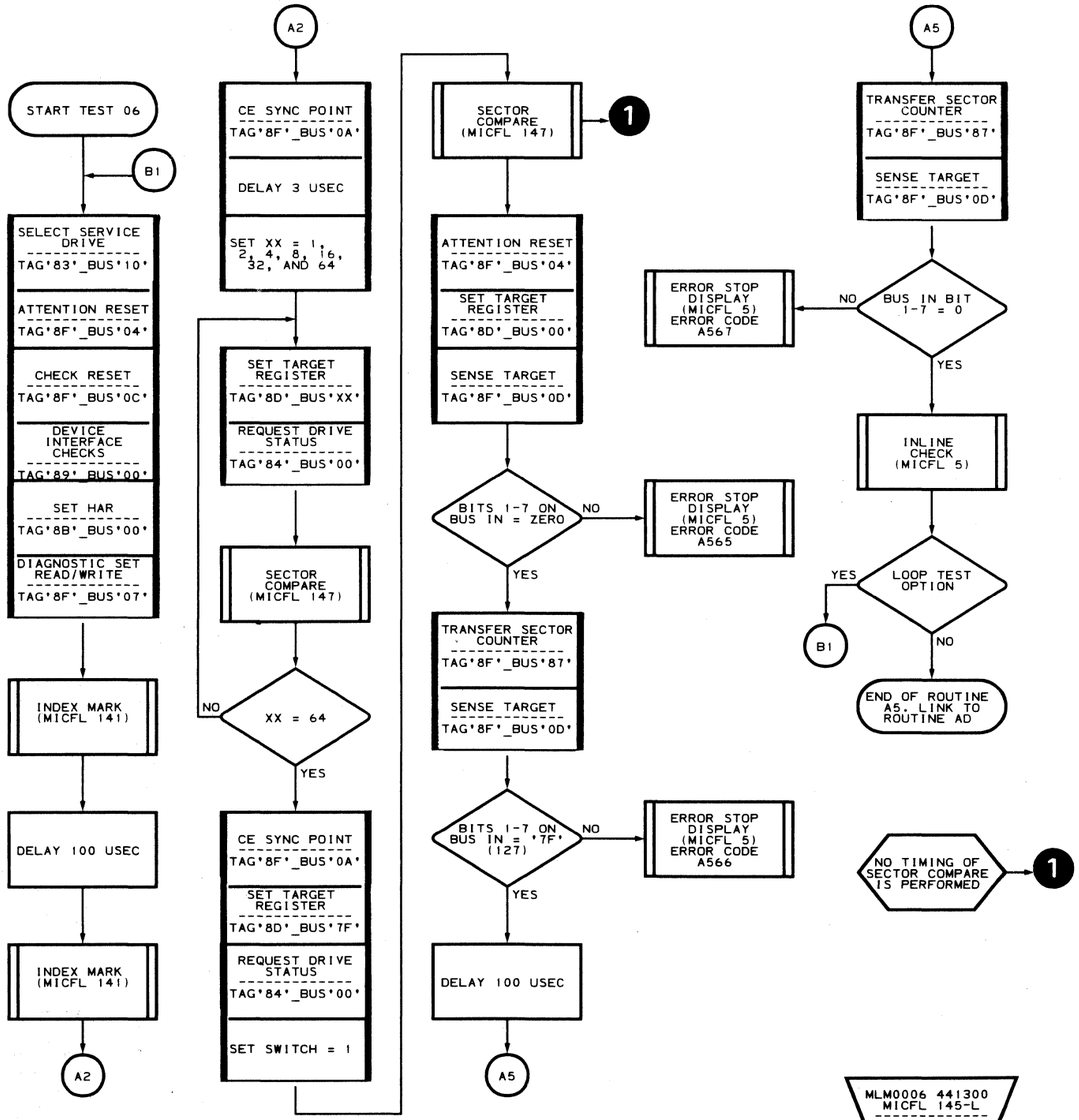
ROUTINE A5 – DRIVE INDEX AND SECTOR TESTS

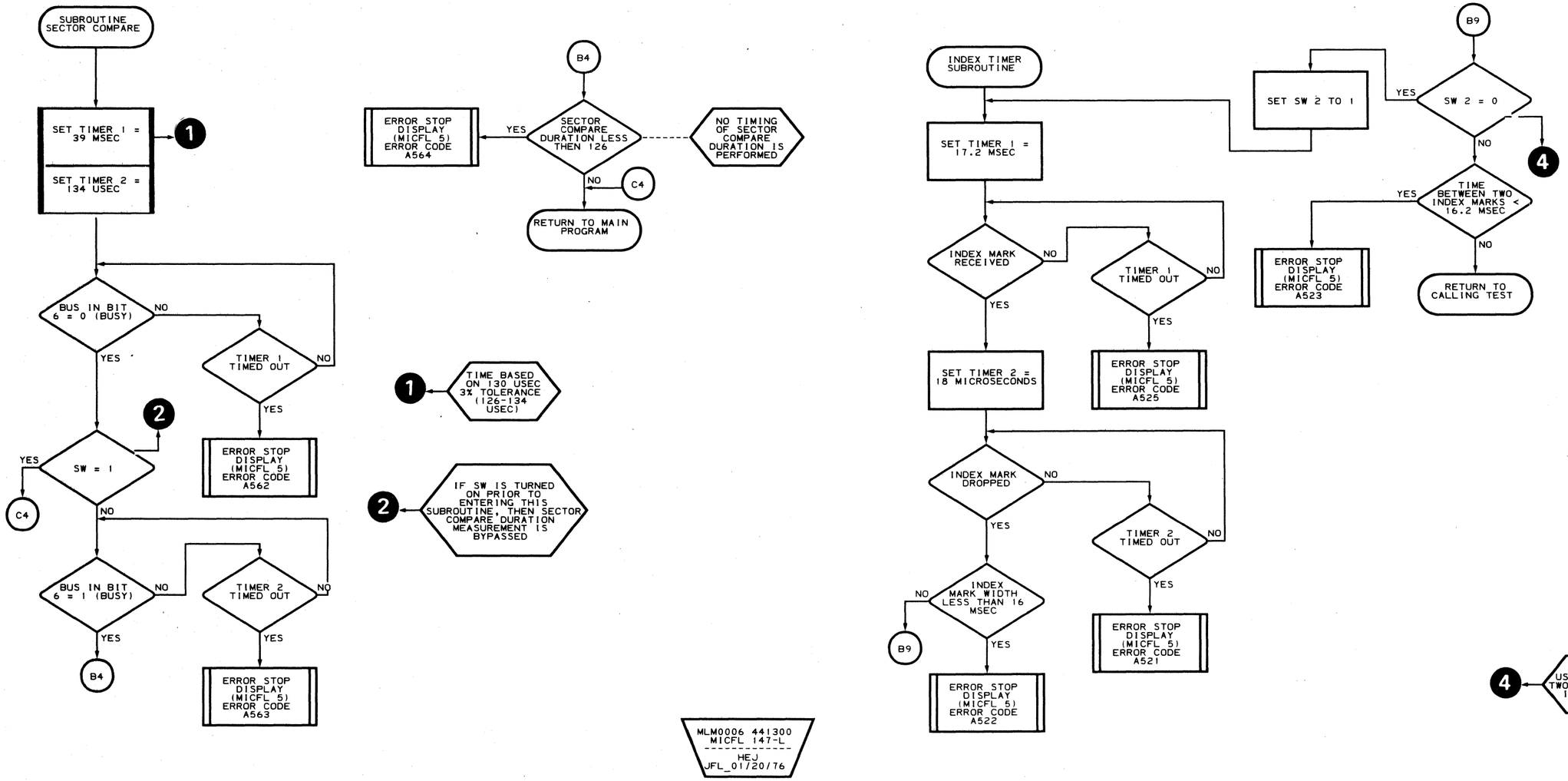






ROUTINE A5 – DRIVE INDEX AND SECTOR TESTS





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L

ROUTINE A7 – 3350 DYNAMIC SERVO ADJUSTMENT PROGRAM

DESCRIPTION

The purpose of routine A7 is to enable a complete servo adjustment to be made under microprogram control. The servo velocity can be fine tuned with this program and the entire procedure performed without the aid of an oscilloscope. The specification tolerance is 330 ± 7 microseconds. The amount of maladjustment of the servo velocity has no effect on successful execution of the program unless hardware failures are detected during execution of the test.

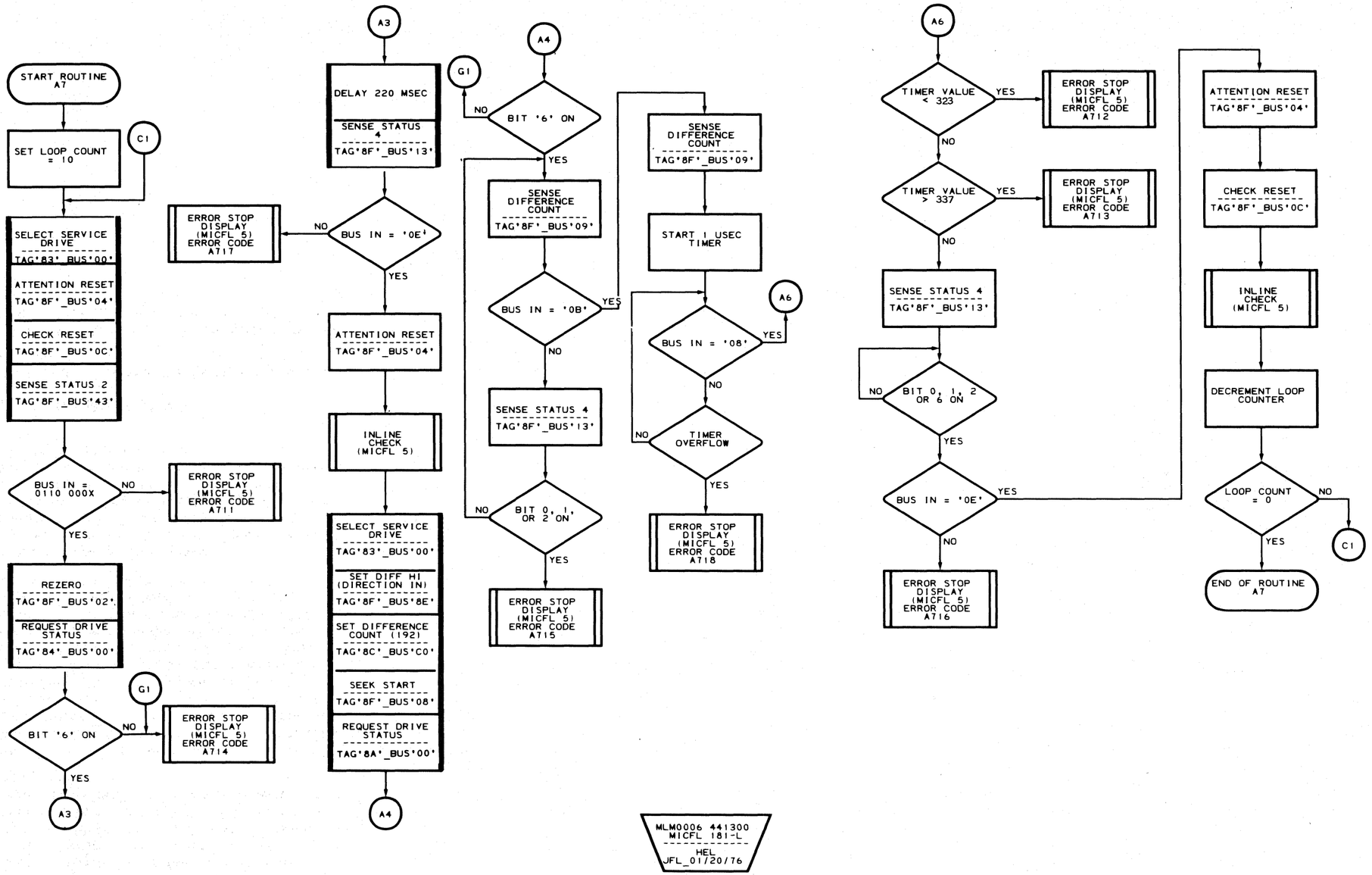
Routine A7 issues a 192-cylinder seek, starting from cylinder 0. Clocking begins from the leading edge of the first track crossing pulse after the Seek Start command to the leading edge of the 182nd track crossing pulse. A timer subroutine collects the elapsed time from the leading edge of the 182nd track crossing pulse to the leading edge of the 184th track crossing pulse. This elapsed time is measured as the Difference Counter decrements from 0A to 08 during deceleration. This measured time is then compared to the specification tolerance of 330 ± 7 microseconds.

Failure of the measured time to meet the specification (±) results in an error. The amount of deviation (from 330 ± 7 microseconds) can be displayed in byte 2 of the logout. If the specification is met, the test is repeated 10 times before normal completion. The test may be restarted as often as desired using the '00' run control option.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 24 for parameter entry.

ROUTINE A7 – DYNAMIC SERVO ADJUSTMENT ROUTINE



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ROUTINE A9 – 3350 INCREMENTAL SEEK TEST

DESCRIPTION

Routine A9 is designed to allow the CE to enter any seek increment between '01' and 'FF'. Starting at cylinder 0, the access takes multiple seeks forward in increments of the number of cylinders specified. When the maximum allowable limit in this direction is reached, reverse seeks of the same increment take place until cylinder 0 is reached.

The operation is repeated until terminated, as described in MICRO 10.

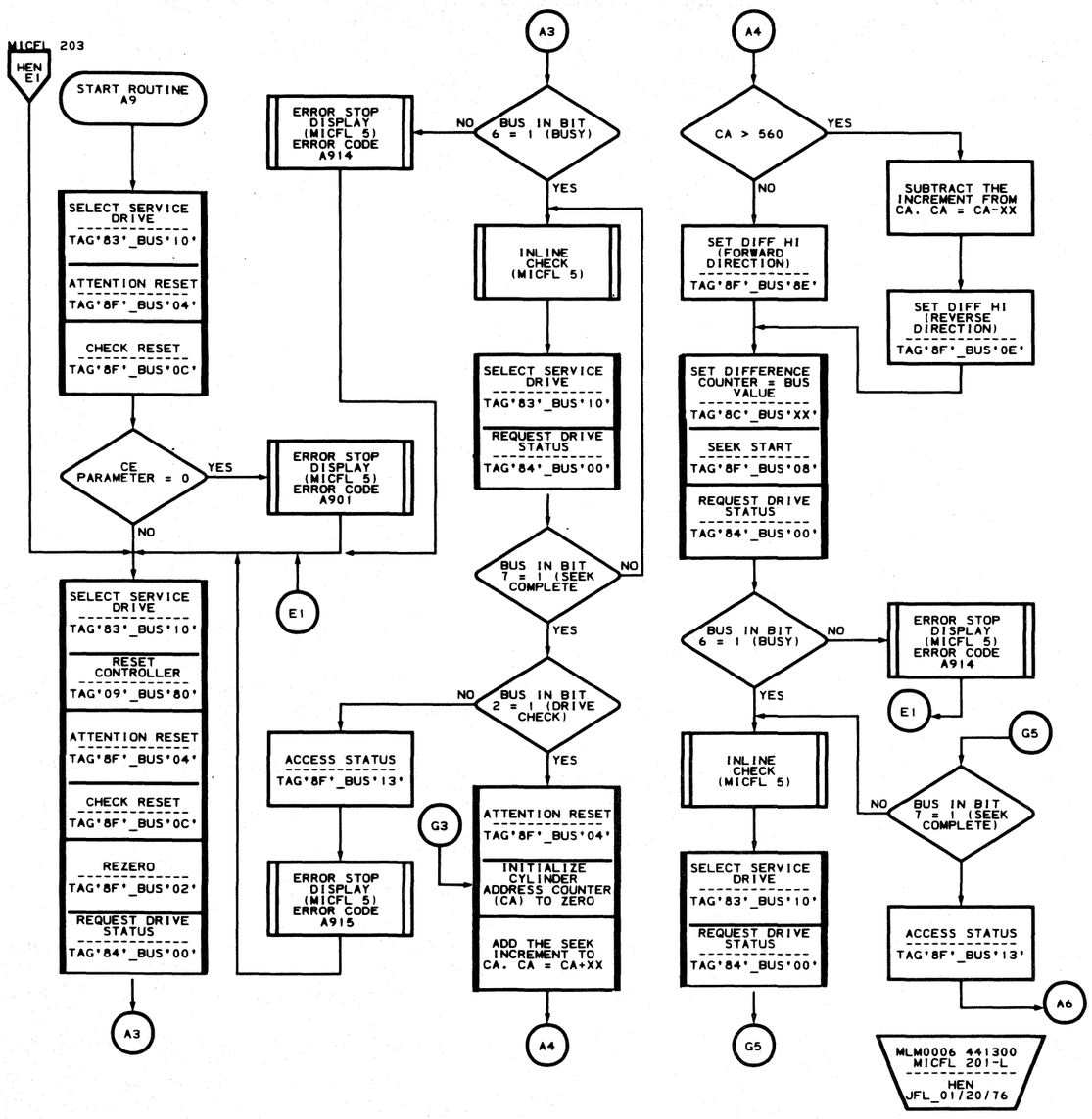
If no seek increment is specified, the test defaults to an increment of one cylinder. An increment of '00' is not allowed in this test.

Access arm position is verified by reading the Home Address. If an error occurs, the test performs a Rezero operation and continues.

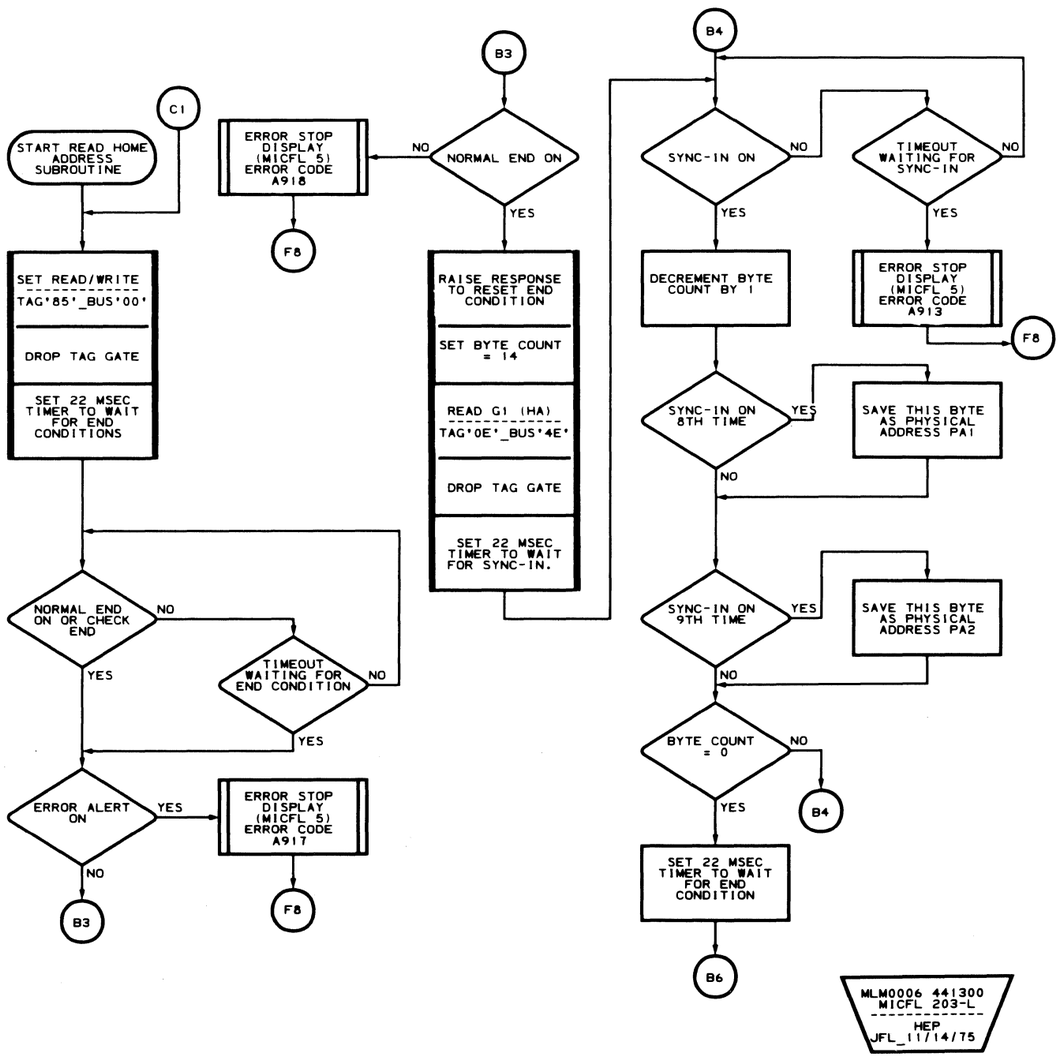
OPERATING PROCEDURE

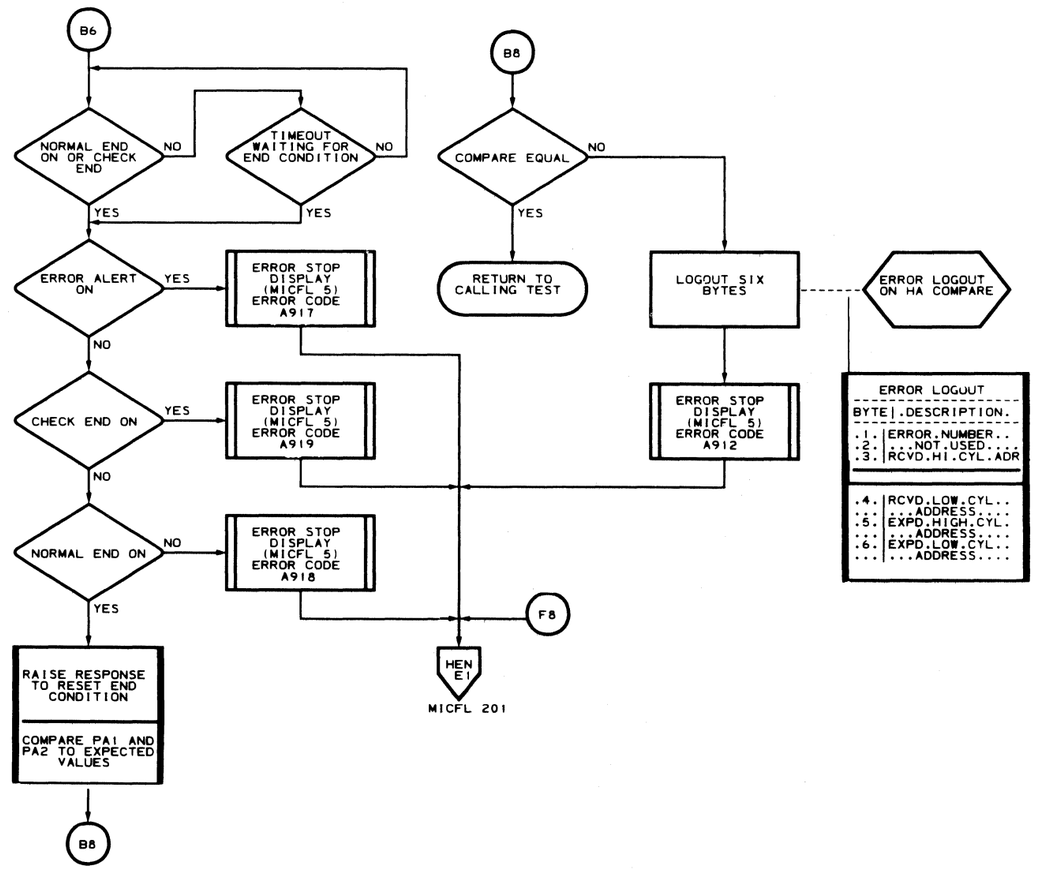
- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 24 for parameter entry. -

ROUTINE A9 – INCREMENTAL SEEK TESTS MICFL 201



ROUTINE A9 – INCREMENTAL SEEK TESTS





ROUTINE AA – 3350 CYLINDER SEEK TEST

DESCRIPTION

Routine AA using head 0, is designed to seek continuously between any two cylinders specified by the CE. See Figure 1.

Any valid physical cylinder address between 0 and 560 (decimal) can be entered by the CE.

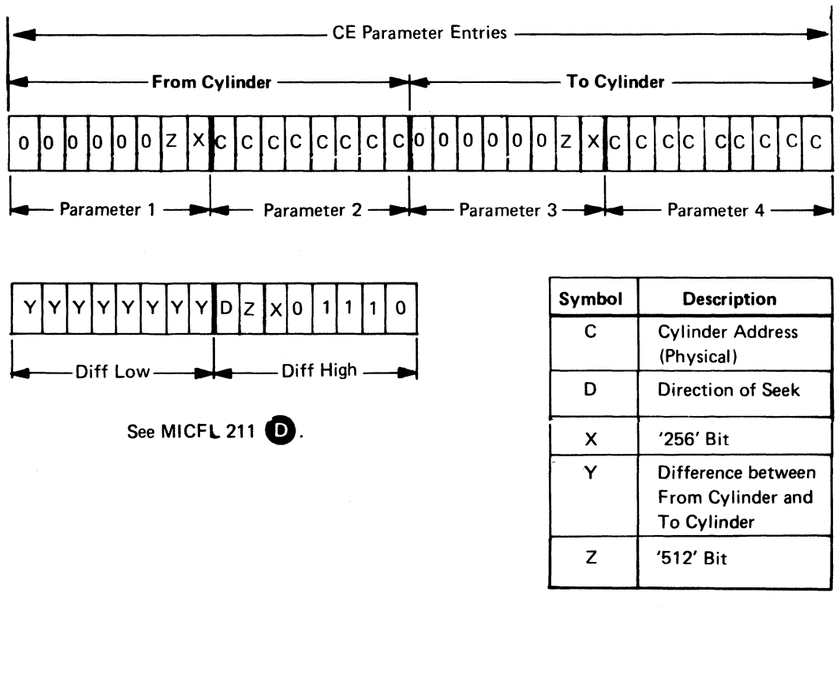
Routine AA acts as a No Motion Seek if the two cylinder addresses selected are identical. See Figure 1.

The access arm position is verified by reading Home Address. If an error occurs, the test rezeros and continues.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 28 for parameter entry.

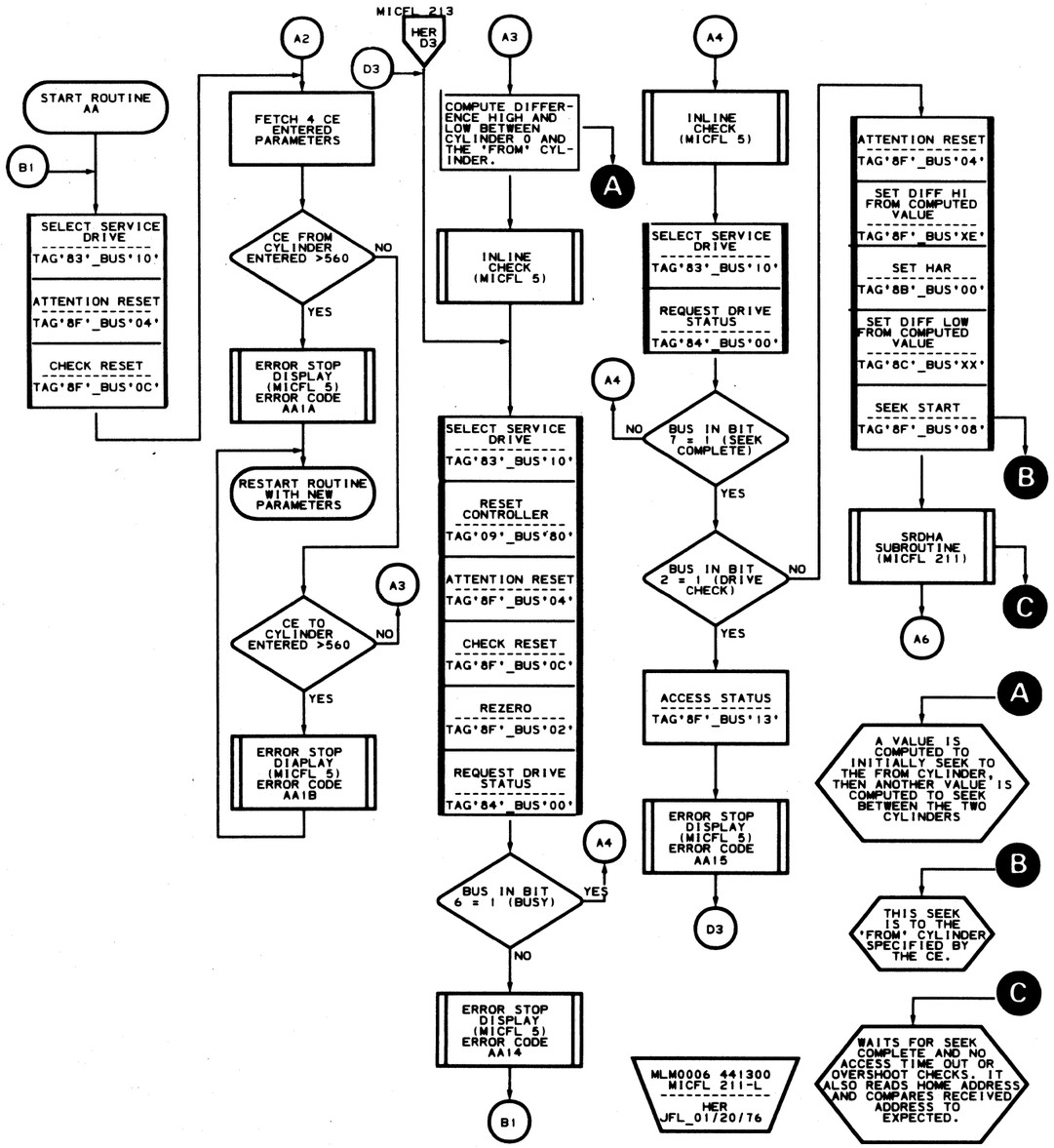
Figure 1.



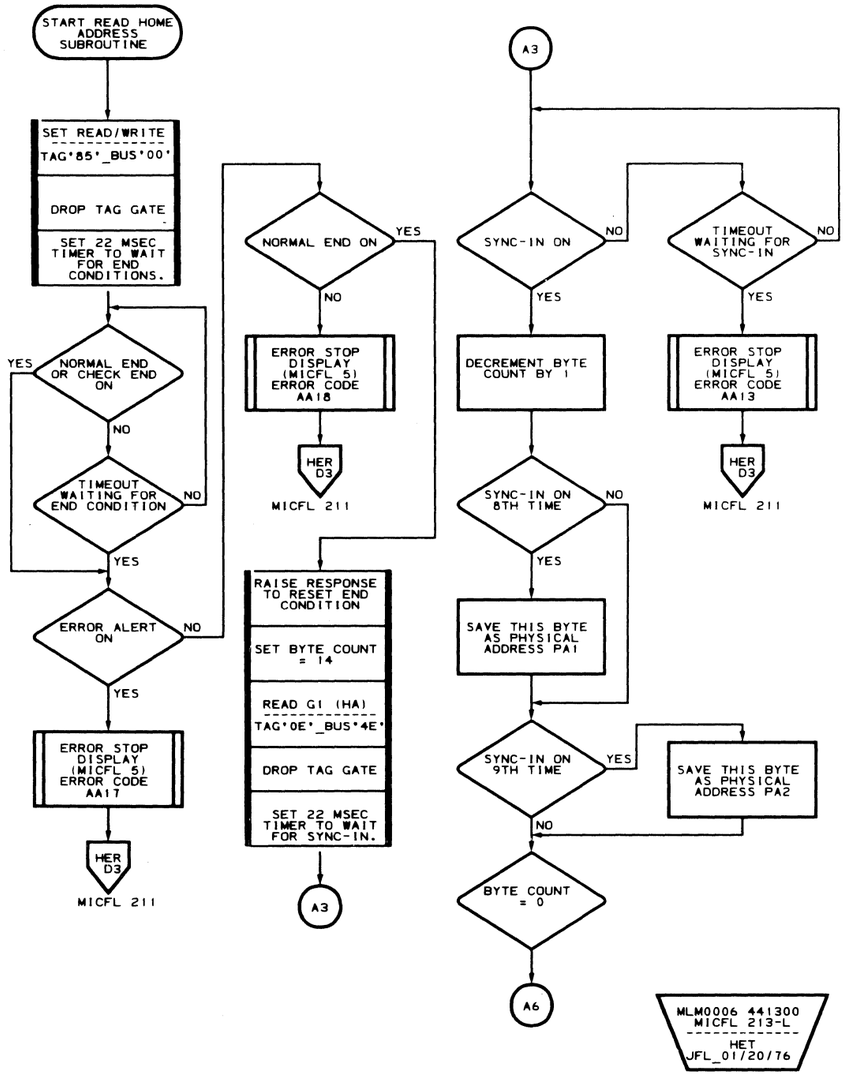
See MICFL 211 D.

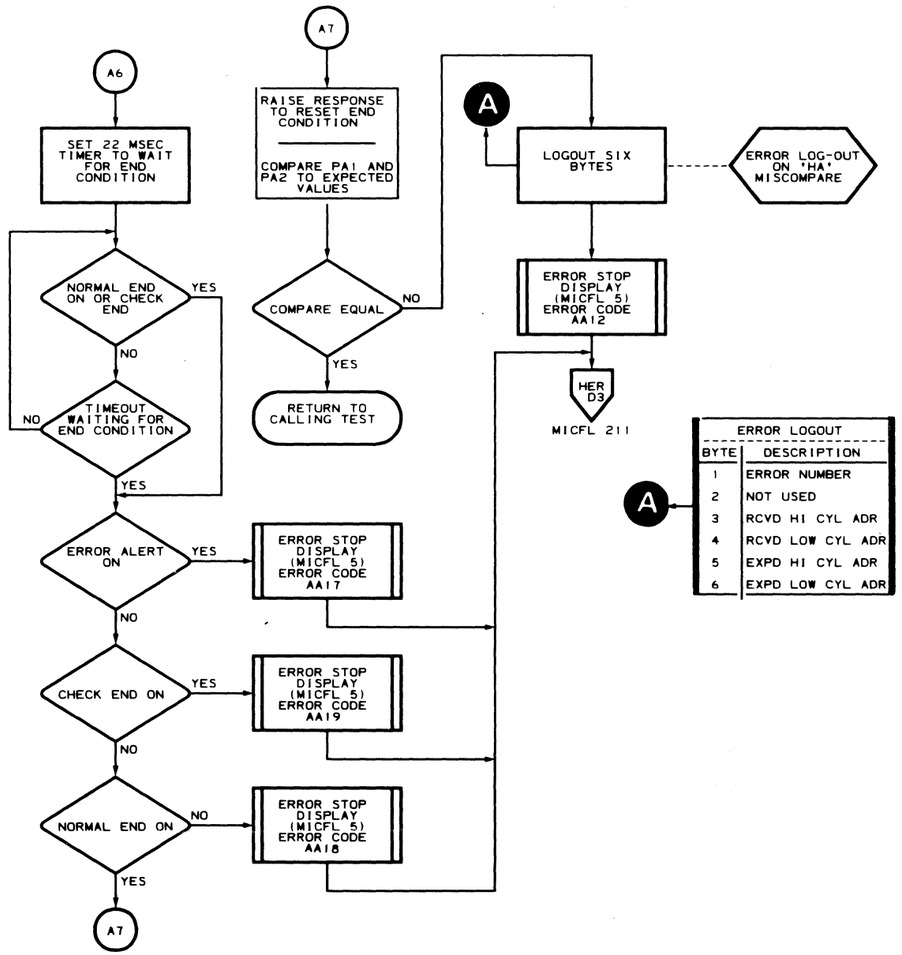
Symbol	Description
C	Cylinder Address (Physical)
D	Direction of Seek
X	'256' Bit
Y	Difference between From Cylinder and To Cylinder
Z	'512' Bit

ROUTINE AA – CYLINDER SEEK TESTS MICFL 211



ROUTINE AA – CYLINDER SEEK TESTS





ROUTINE AB — 3350 RANDOM SEEK TEST

DESCRIPTION

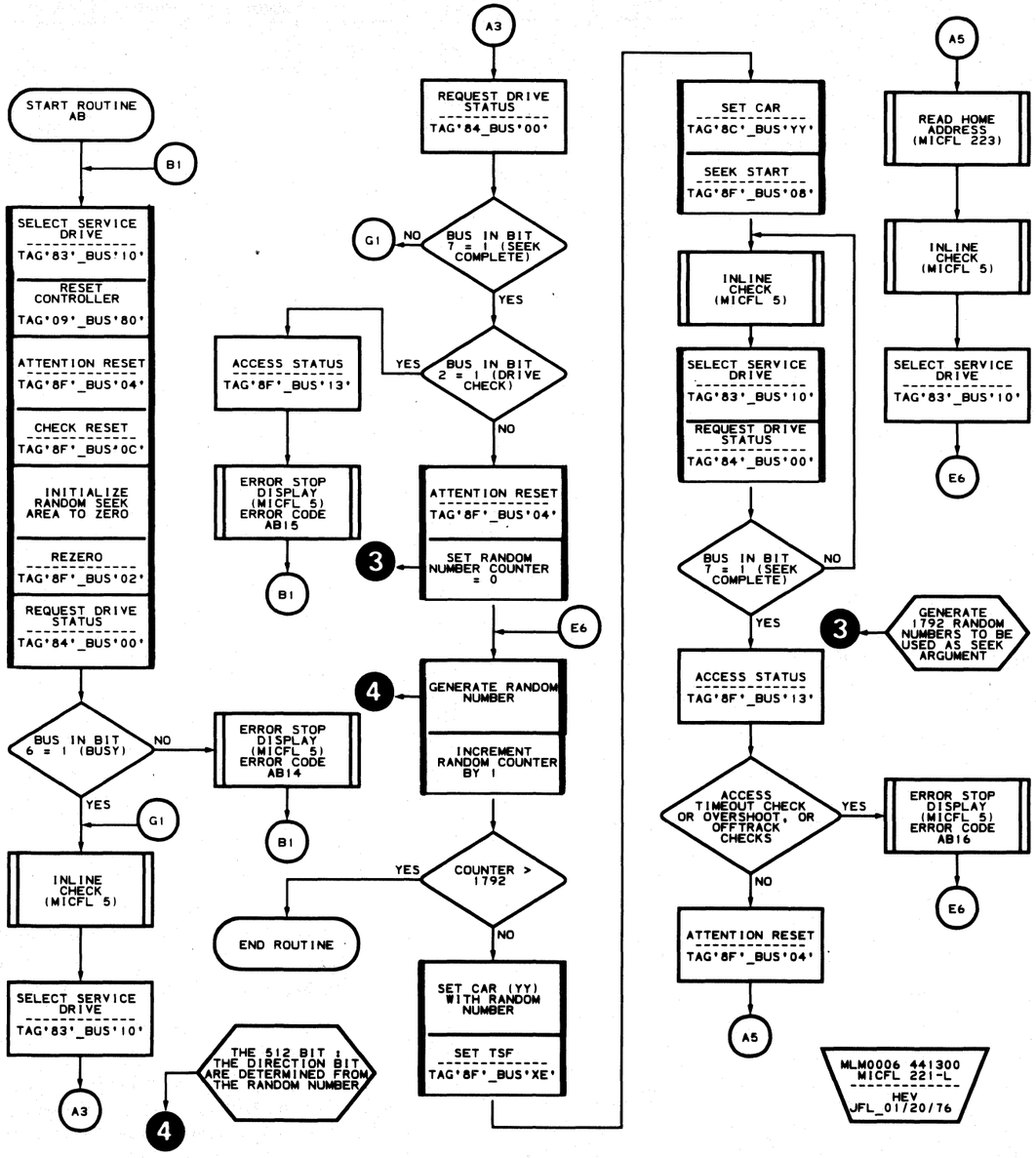
Routine AB generates 1792 random seek addresses and seeks to each cylinder. Numerous forward and reverse seeks and no motion seeks are produced. The test automatically terminates after executing the last seek.

The access arm position is verified by reading Home Address using head 0 only. If an error occurs, the test is restarted from the beginning causing a Rezero operation.

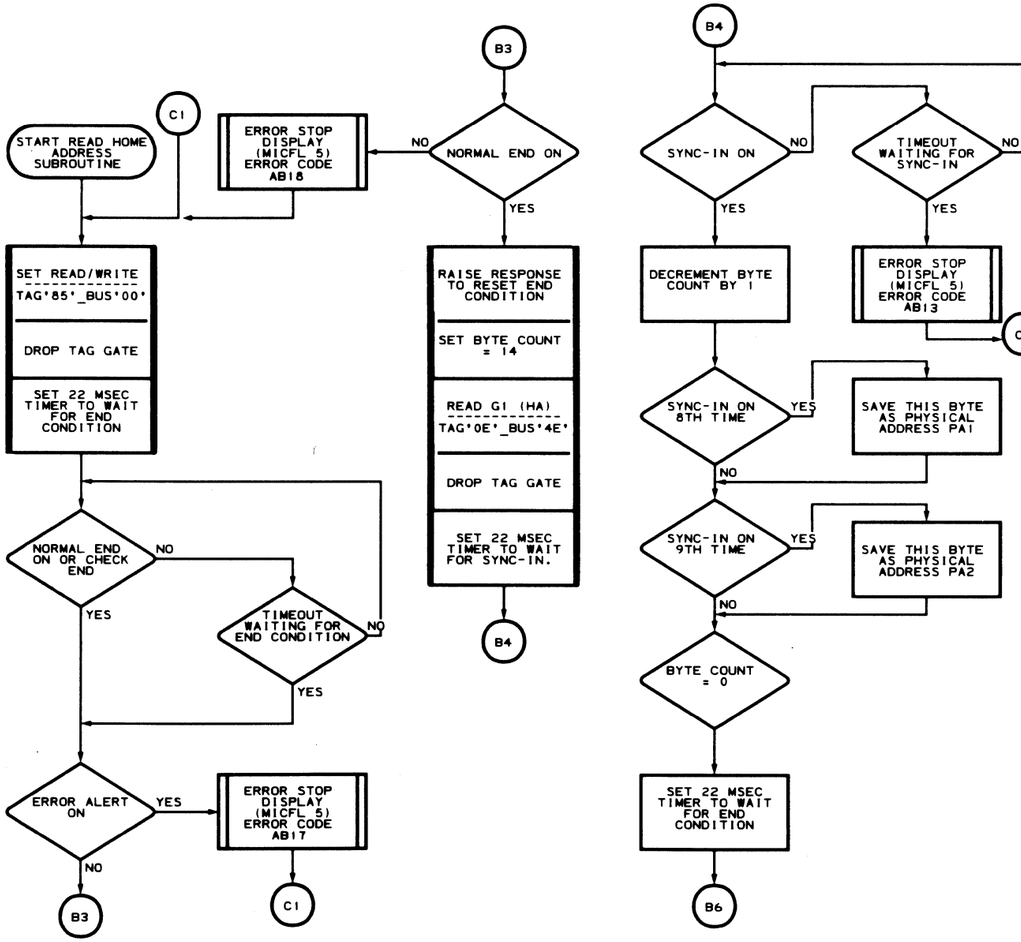
OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 28 for parameter entry.

ROUTINE AB – RANDOM SEEK TESTS



ROUTINE AB – RANDOM SEEK TESTS



MLM0006 441300
MICFL 223-L
HEW
JFL_11/14/75

MLM0006 441300
MICFL 223-R
HEX
JFL_11/14/75

ROUTINE AD – GAP COUNTER AND DATA TRANSFER TESTS

DESCRIPTION

Routine AD checks the Gap Counter and associated drive and controller circuitry. In normal operation (default parameter 1 = '00'), all tests are executed in sequence.

Optional parameter entry may be used to restrict operation to a single test. If a single test is selected, it loops indefinitely until halted by the CE or an error halt.

All tests are performed using physical cylinder 560, head 1.

Test All Initialization

Prior to the start of any test, this step verifies that the CE parameter, if any, is valid.

Routine AD verifies that:

- The CE drive is online and Write Enabled.
- A Set Read/Write operation generates a Normal End response within 500 microseconds without an Error Alert 1.
- Index is present within 21 milliseconds.

The routine then rezeros the access mechanism, checking for Busy to become active. The routine checks for normal completion of the operation within 220 milliseconds. After completion, drive status includes no Drive Check, not Busy, and Seek Complete.

The routine initiates a 560 cylinder seek operation and checks for no Error Alert and drive status following the Seek operation. After the operation, drive status includes: no Drive Check, not Busy, and Seek Complete.

Test 01. Data Transfer Checkers Check
Check Diag Inhibit Write Mode
Force Gap Ctr Parity Error
Force Write Data Check

Test 01 checks that Diagnostic Inhibit Write Gate Mode operates as follows:

1. Reads drive status
2. Looks for I Write Sense = 0 (Bit 1)
3. Orients Track Index
4. Initiates a Format G1 operation
5. Orients on Track Index
6. Waits approximately 10 microseconds
7. Reads drive status
8. Checks for I Write Sense = 1 (Bit 1)

The preceding sequence is repeated with Diagnostic Inhibit Write Gate Mode = 1 and the test checked for I Write Sense = 0.

Test 01 looks for no Gap Counter Error, initiates a Write G1 operation with Diagnostic Inhibit Write Gate and Diagnostic Invert Bus Out Parity modes active. It checks for Gap Counter error, Write Data Check and Controller Error status. The test initiates a Controller Reset operation and checks for no Gap Counter error. The test then issues a Check Reset operation to reset any errors in the drive.

Test 02. G1 Gap Tolerance

Test 02 measures the length of the G1 Gap by orienting on Track Index, initiating a Write G1 operation, orienting again on Track Index, and measuring the time to the first Sync In. The measured time is checked for optimum value of 114 byte-times (95 microseconds). Tolerance is ±3%. Valid range = 92–98 microseconds.

Note: *The normal G1 length is 116 bytes including the Sync Byte. The optimum time is (95 microseconds). During a Write operation, the first Sync In is presented two byte-times earlier at 114-byte time.*

Test 03. Extended G1 Gap Tolerance

Test 03 measures the length of an extended G1 Gap by orienting on Track Index, initiating a Write Extended G1 operation, orienting again on Track Index, and measuring the time to the first Sync In. The measured time is checked for an optimum value of 242 byte-times (202 microseconds). Tolerance is ±3%. Valid range = 196–208 microseconds.

Note: *The extended G1 length is 244 bytes + Sync Byte. The optimum time is (202 microseconds). During a Write operation, the first Sync In is presented two bytes earlier at 242 byte-time.*

Test 04. Modulo 16 Counter Function

Test 04 checks the operation of the four bit positions of the Modulo-16 Counter and the Recycle line by initiating a Write G1 operation with Diagnostic Inhibit Write Gate Mode active. Byte counts used for the Modulo-16 Counter test are 1, 2, 4, 8, and 17. The test counts the number of Sync Ins until receipt of an end condition. Any abnormal ending conditions resulting from this technique are ignored.

Test 05. G2 Gap Tolerance

Test 05 measures the length of a G2 Gap by orienting on the G1 (HA) field, initiating a Write G2 operation with Daignostic Inhibit Write Gate Mode active, and counting the time to the first Sync In. The measured time is checked for optimum value of 74 byte-times (61.71 microseconds). Tolerance is ±3%. Valid range = 60–64 microseconds.

Note: *The normal G2 length is 76 byte-times (66.46 microseconds). During a Write operation, the first Sync In is presented two byte-times earlier at byte 74 time.*

Test 06. G3 Gap Tolerance

Test 06 measures the length of a G3 Gap by orienting on the G1 (HA) field, starting a Write G3 operation with Diagnostic Inhibit Write Gate Mode active, and counting the time to the first Sync-In. The measured time is checked for an optimum value of 77 byte-times (64.30 microseconds). Tolerance is ±3%. Valid range = 62–66 microseconds.

Note: *Normal G3 gap length is 79 byte-times. During a Write operation, the first Sync In is presented 2 byte-times earlier at byte 77 time.*

Test 07. Data Transfer

Test 07 initiates a Write G1 operation with Diagnostic Inhibit Write Gate Mode active, using a data pattern of 'EB6DB6DB'. At the end of the operation, this test verifies that no ECC Check and no Write Data Check were received.

Test 08. Write Safety Checkers Check
Force Control Check
Force Write Ovrn Check
Force Transition Check (Write Intended)
Force Write I Check (Read Unsafe)

Test 08 verifies that a Check Reset resets Read/Write Check, Control Check, Write Overrun Check, Transition Check, and Write I Check. The test forces Control Check by raising Read Gate and Write Gate simultaneously.

The test forces Write Overrun Check by orienting near the end of the Active Track, raising Write Gate to the drive and holding it up through Index. The test forces Transition Check and Write I Check by raising Write Gate to the drive without Bus Out bit 4 = 1. This inhibits Current Source Unblocked. The test checks that each of the above conditions forces Read/Write Check and that it is reset by a Check Reset.

Test 09. Force Pad Gate Check
Force Head Short Check

Test 09 verifies that a Check Reset resets Read/Write Check, Pad Gate Check, and Head Short Check. The test forces a Pad Gate Check by using the Drive Diagnostic Command.

The test forces Head Short Check by raising Write Gate in the drive. The test checks that each of the above conditions forces Read/Write Check, and that it is reset by a Check Reset.

Test 0A. Gap Extension After Issuing a Special G2 04 Gap Tolerance

Test 0A verifies the length of Special G2 and normal G2 commands after the initial Special G2 is issued. These gaps should be extended to 128 byte-times. Test 10 also verifies the length of the G4 gap.

ROUTINE AD – GAP COUNTER AND DATA TRANSFER TESTS MICFL 241

DESCRIPTION (Continued)

Test 0B. Write Fail Latch

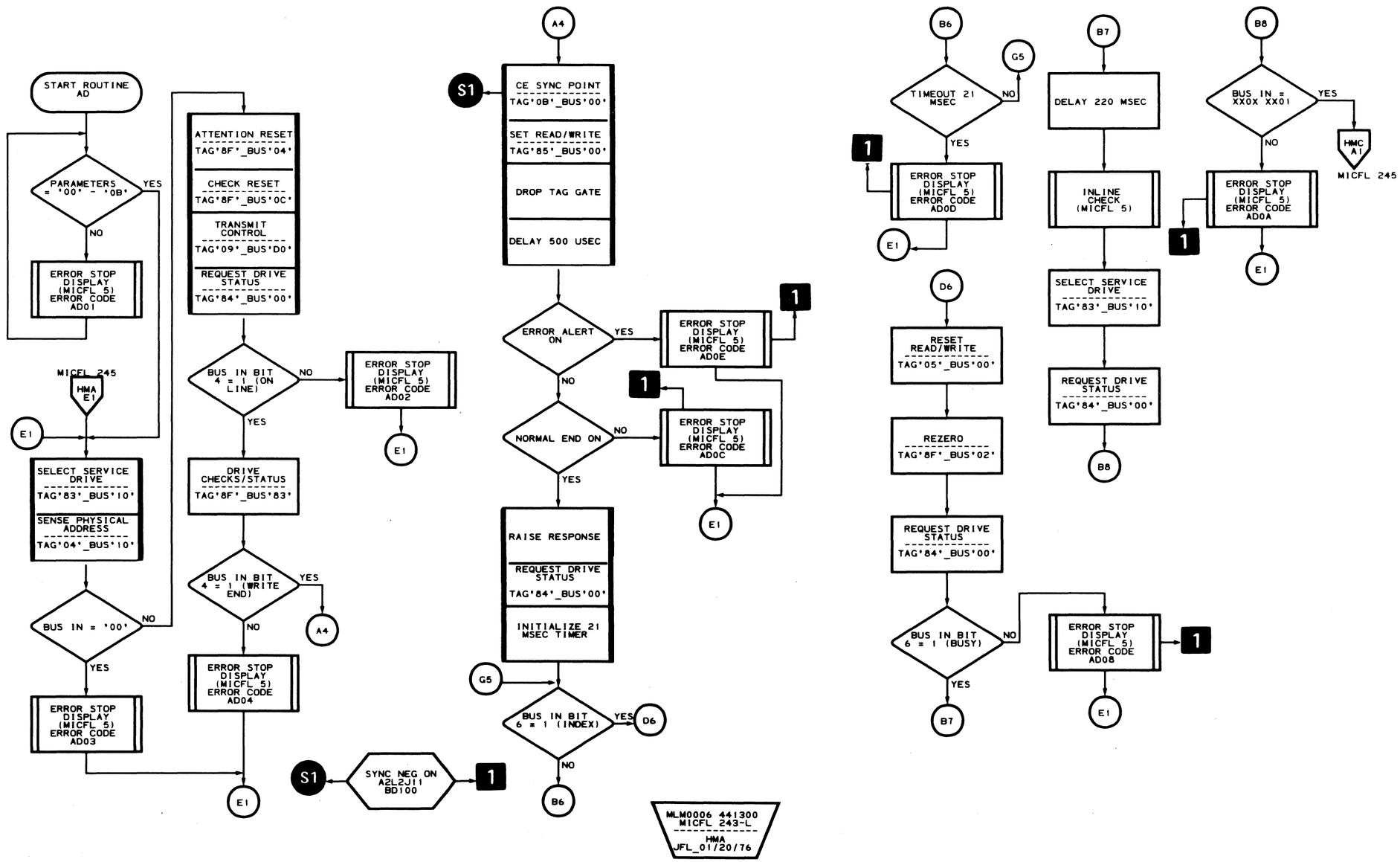
Test 0B forces a Monitor check, Multihead Select, and looks for Read/Write Check being on. The test then issues a Write G1, waits until after Index, then looks for I Write Fail, Bus In bit 5 = 1. The test issues a Check Reset, Diagnostic Reset, and Read/Write Reset; it then issues a Sense command and looks for Bus In bit 5 = 0.

OPERATING PROCEDURE

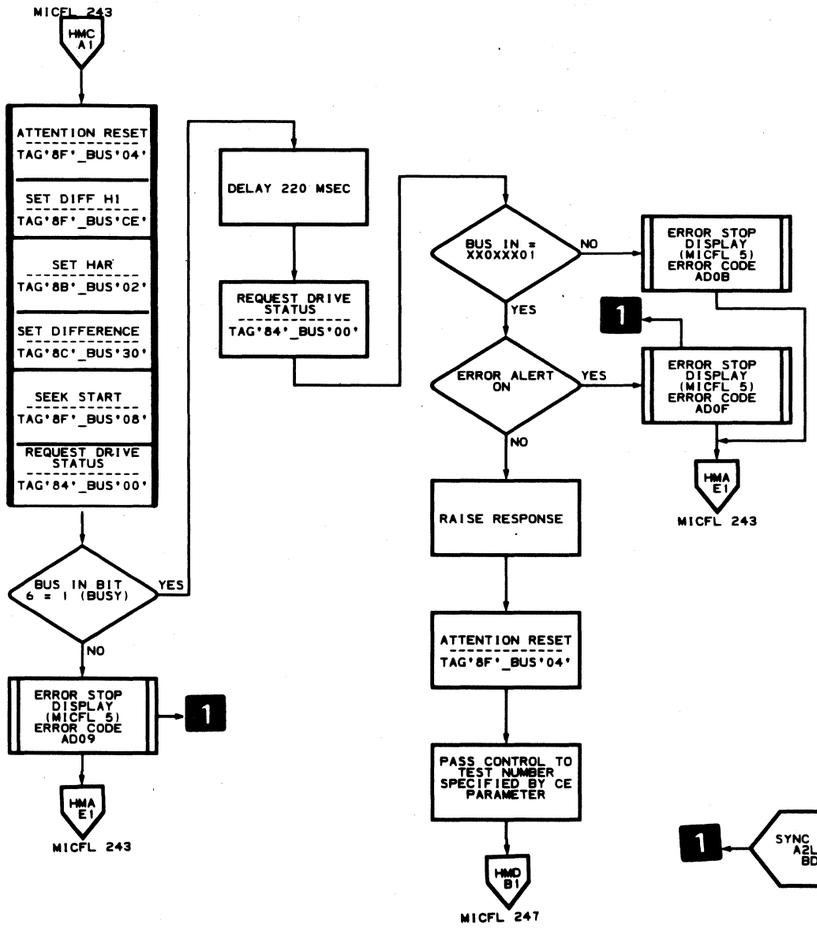
- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 30 for parameter entry.

ROUTINE AD – GAP COUNTER AND DATA TRANSFER TESTS MICFL 241

ROUTINE AD – GAP COUNTER AND DATA TRANSFER TESTS MICFL 243



ROUTINE AD – GAP COUNTER AND DATA TRANSFER TESTS MICFL 245



MLM0006 441300
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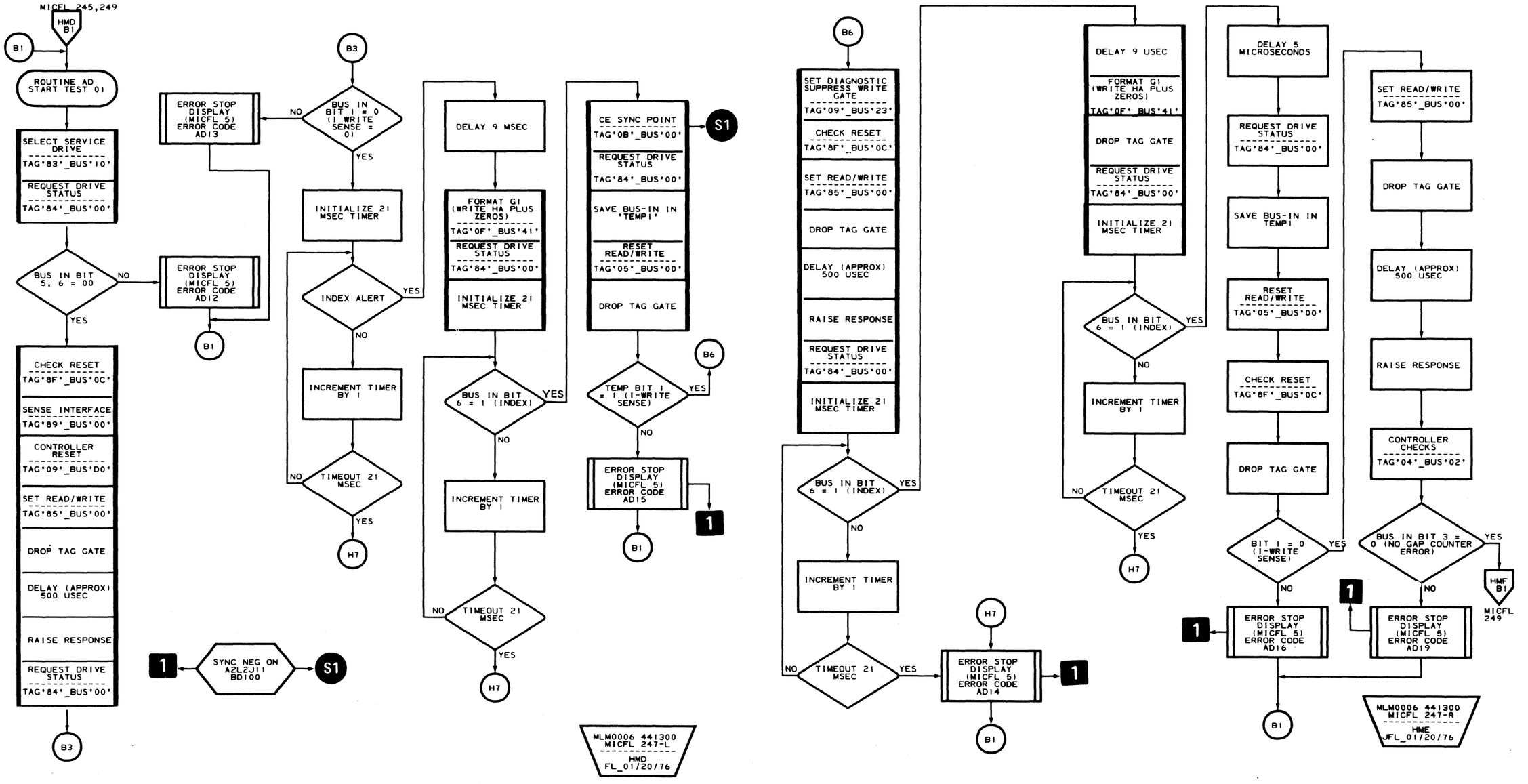
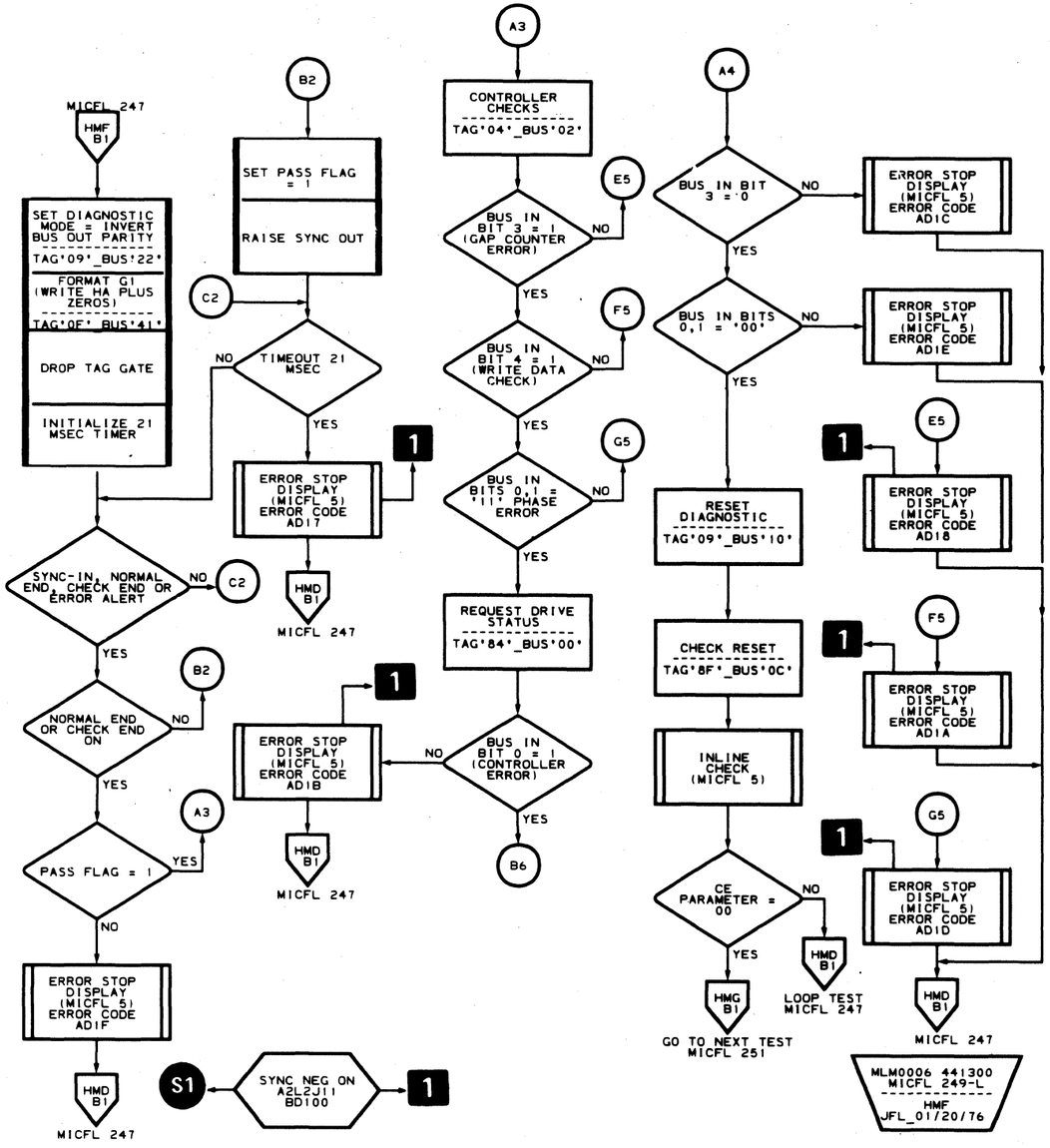
ROUTINE AD – GAP COUNTER AND DATA TRANSFER TESTS MICFL 245

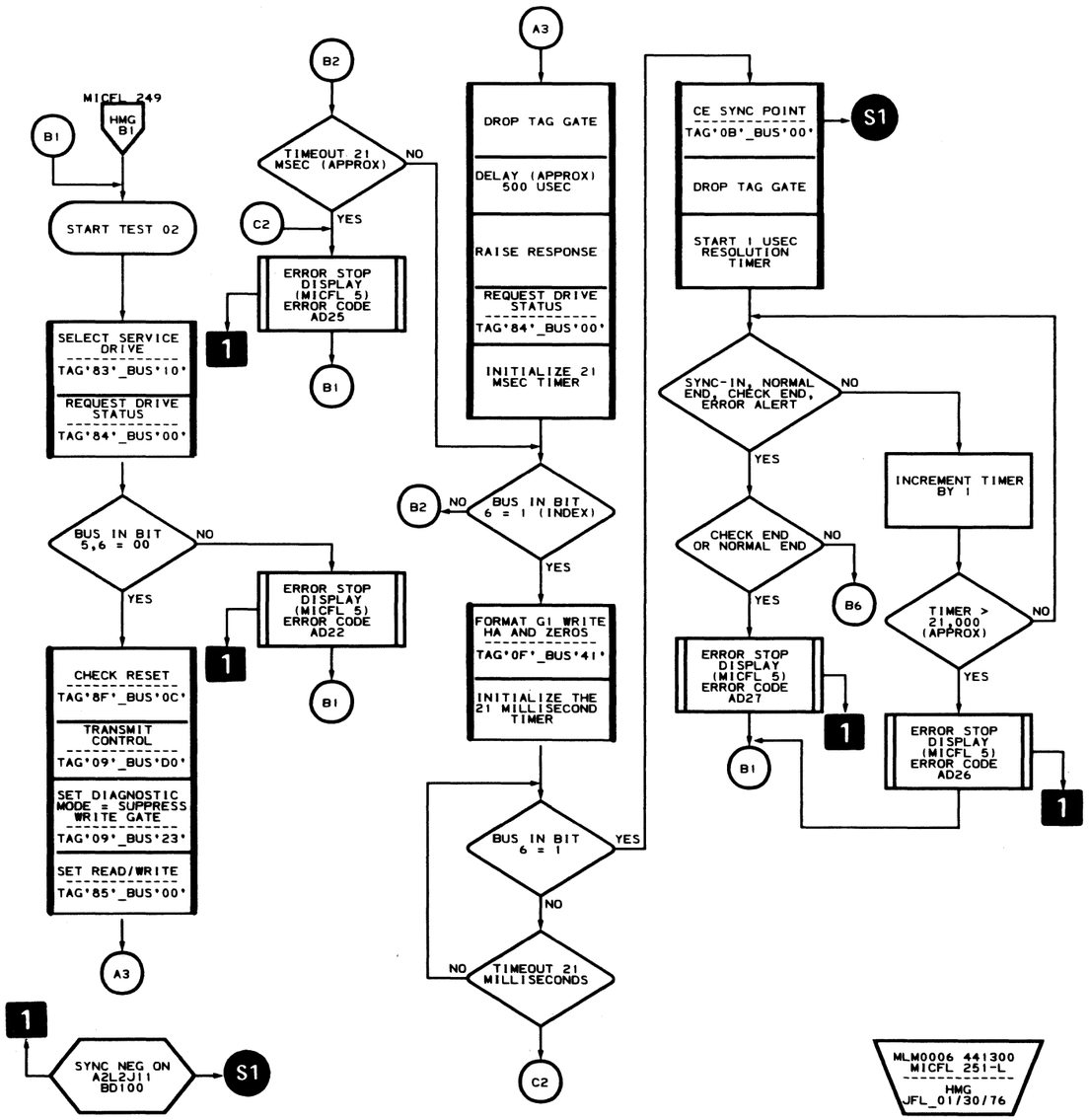
ROUTINE AD – GAP COUNTER AND DATA TRANSFER TESTS



GC0247 Seq. 1 of 2	2358407 Part No.	441300 31 Mar 76	441306 1 Apr 77			



ROUTINE AD – GAP COUNTER AND DATA TRANSFER TESTS



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MICFL 251-R
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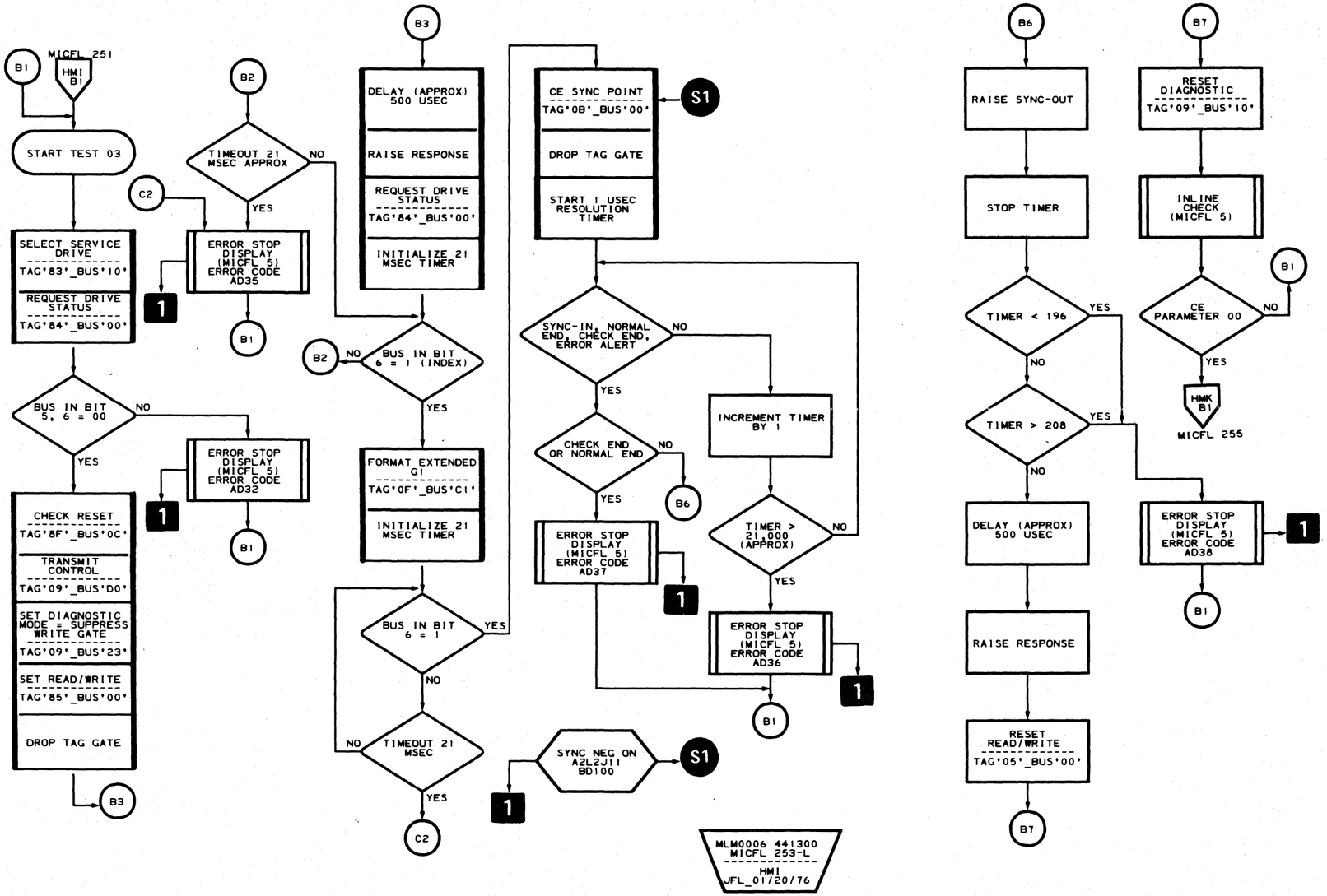
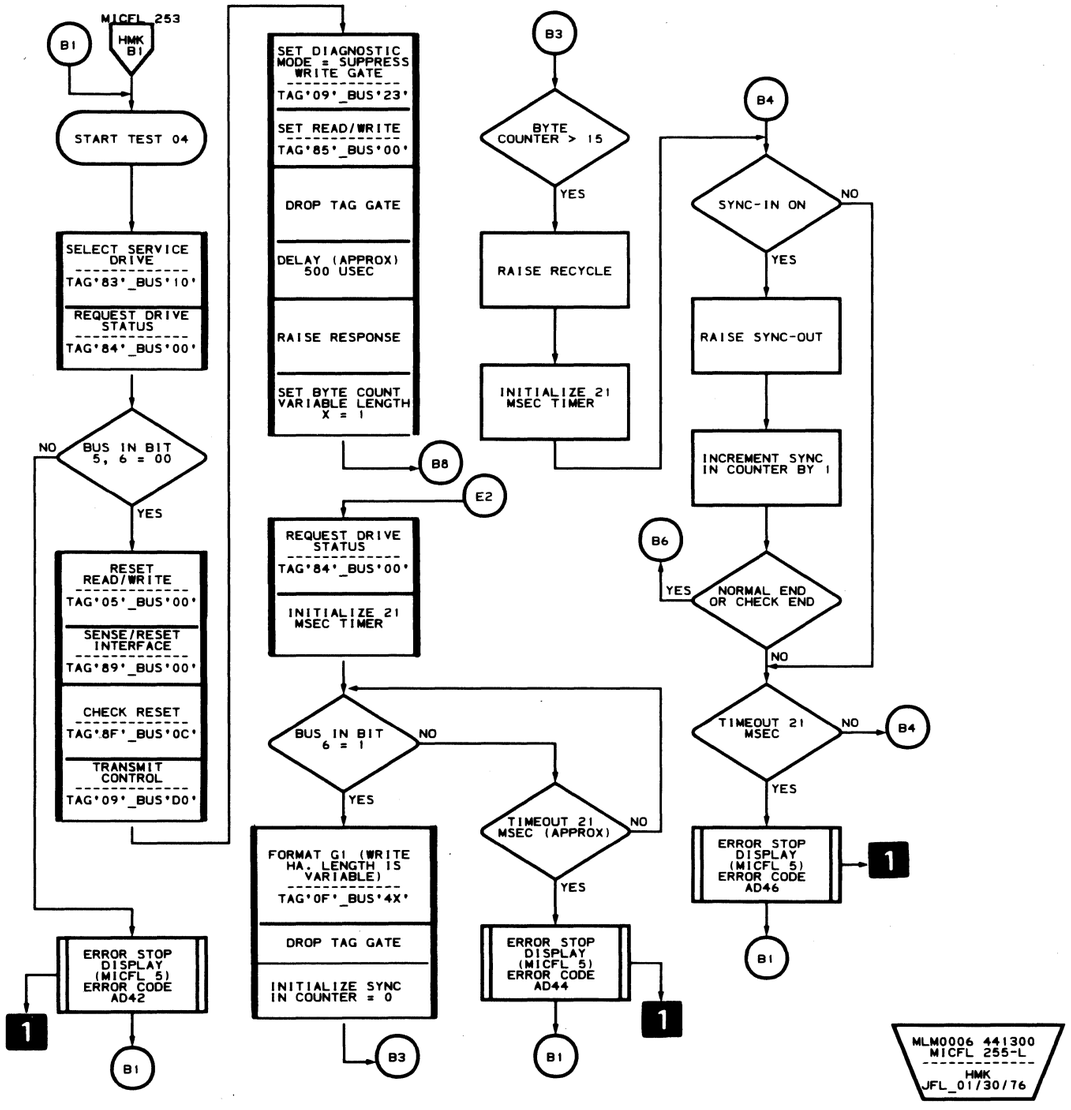
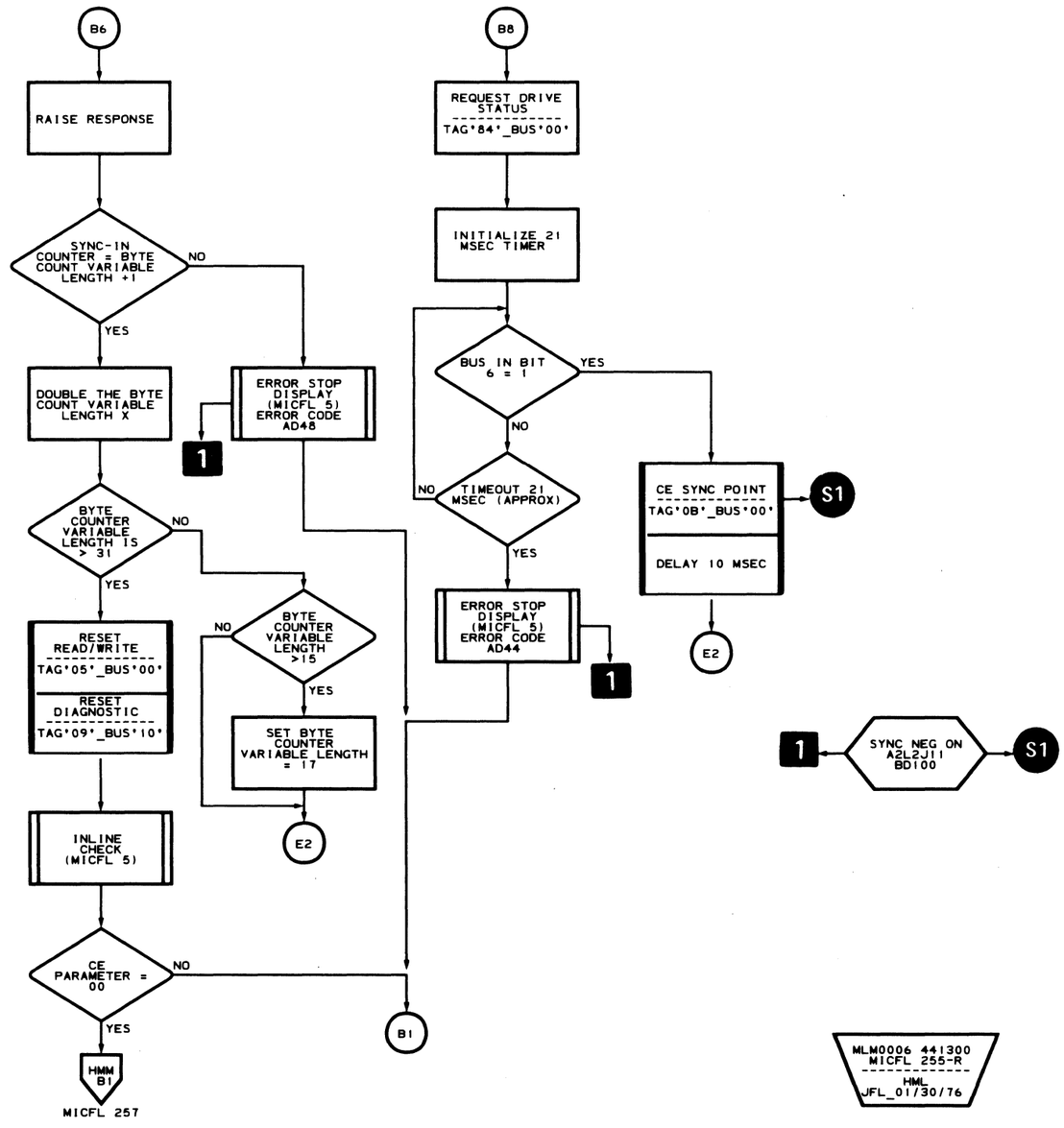
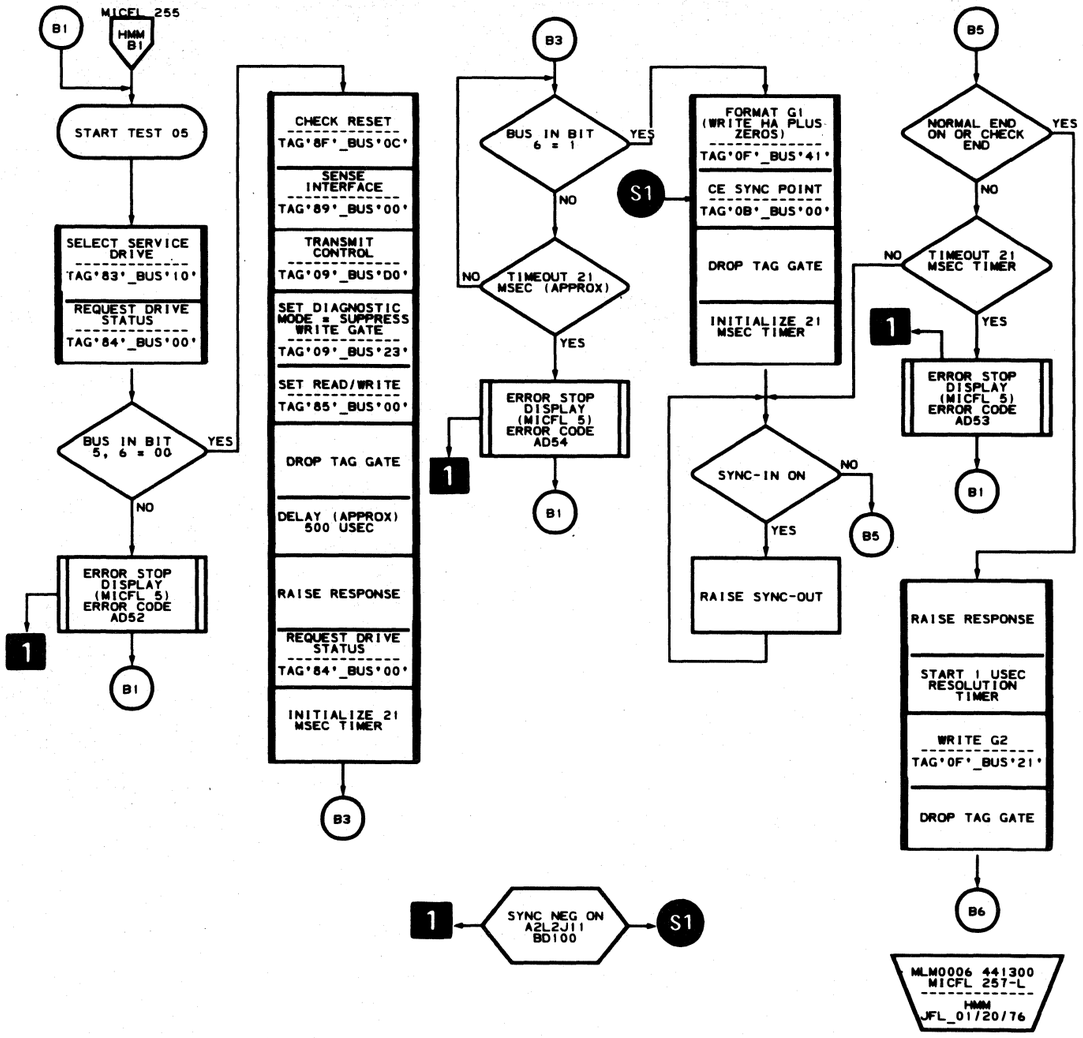


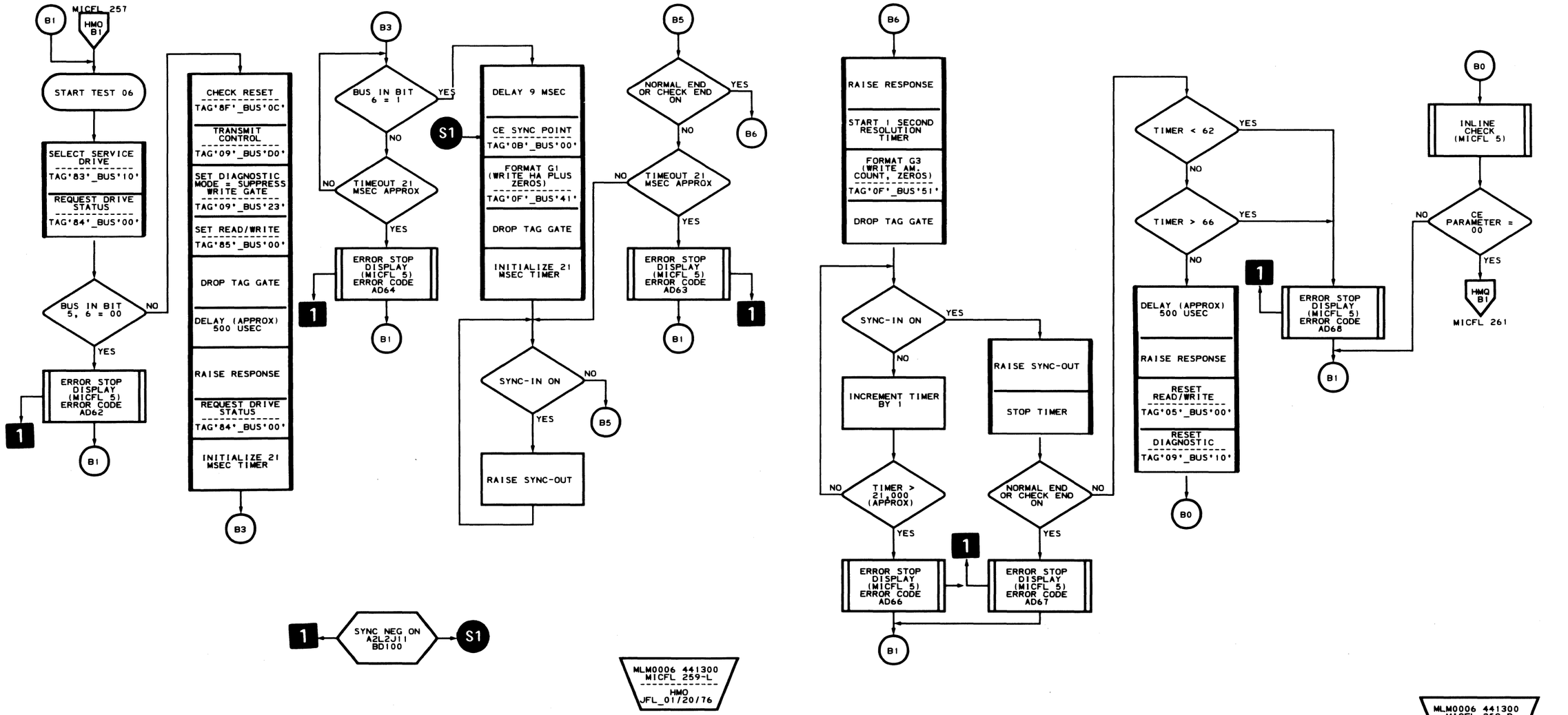
ROUTINE AD – GAP COUNTER AND DATA TRANSFER TESTS

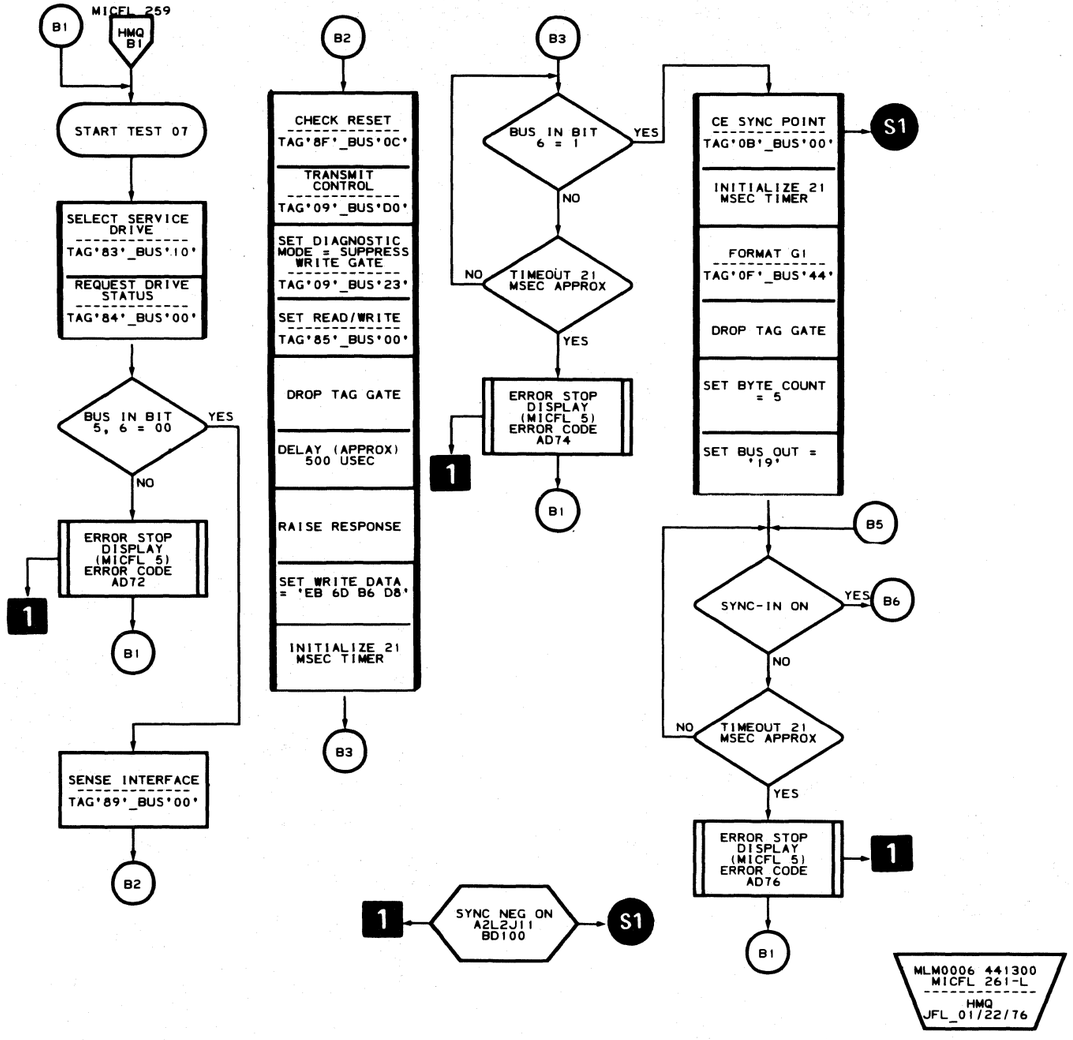


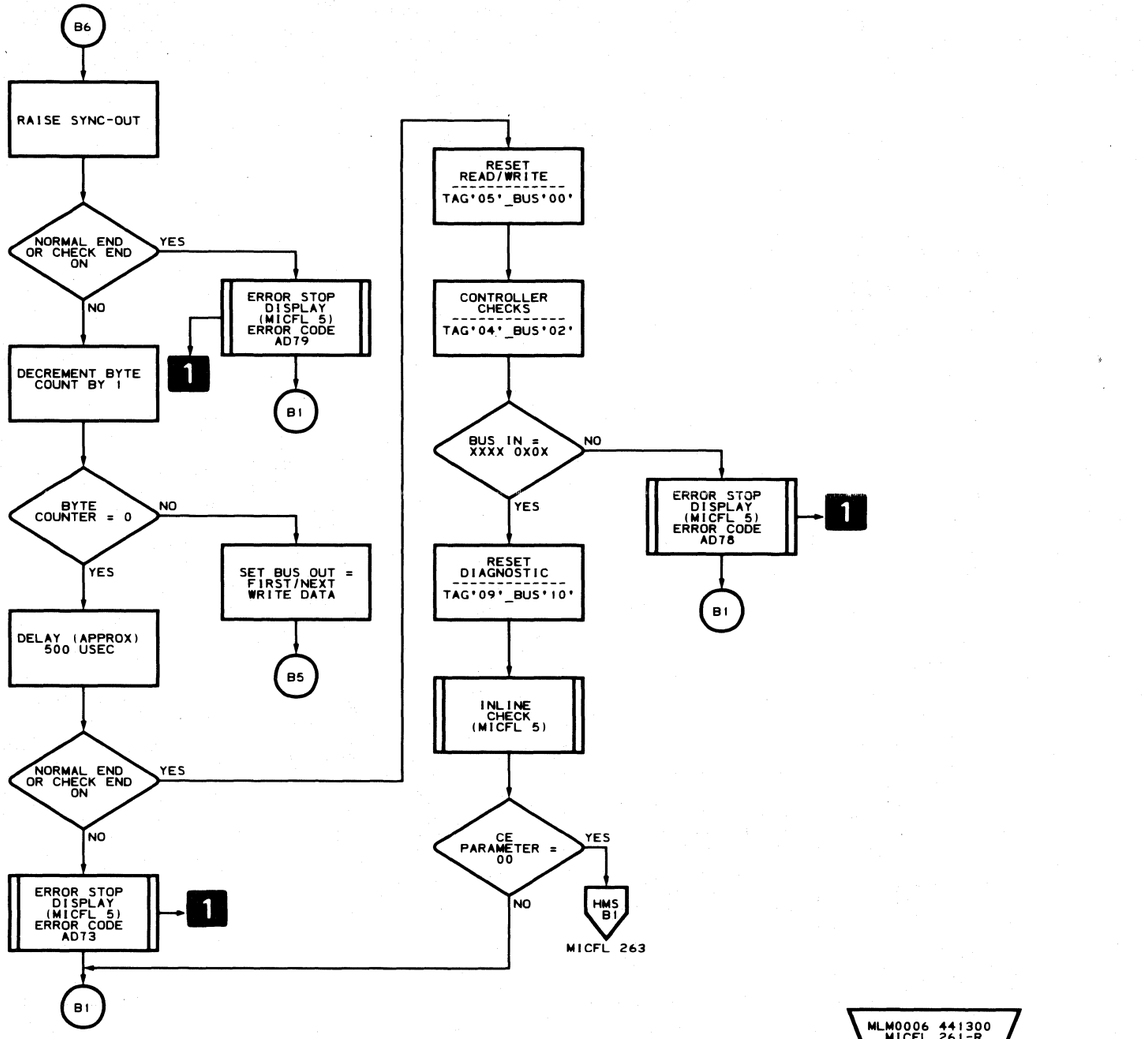




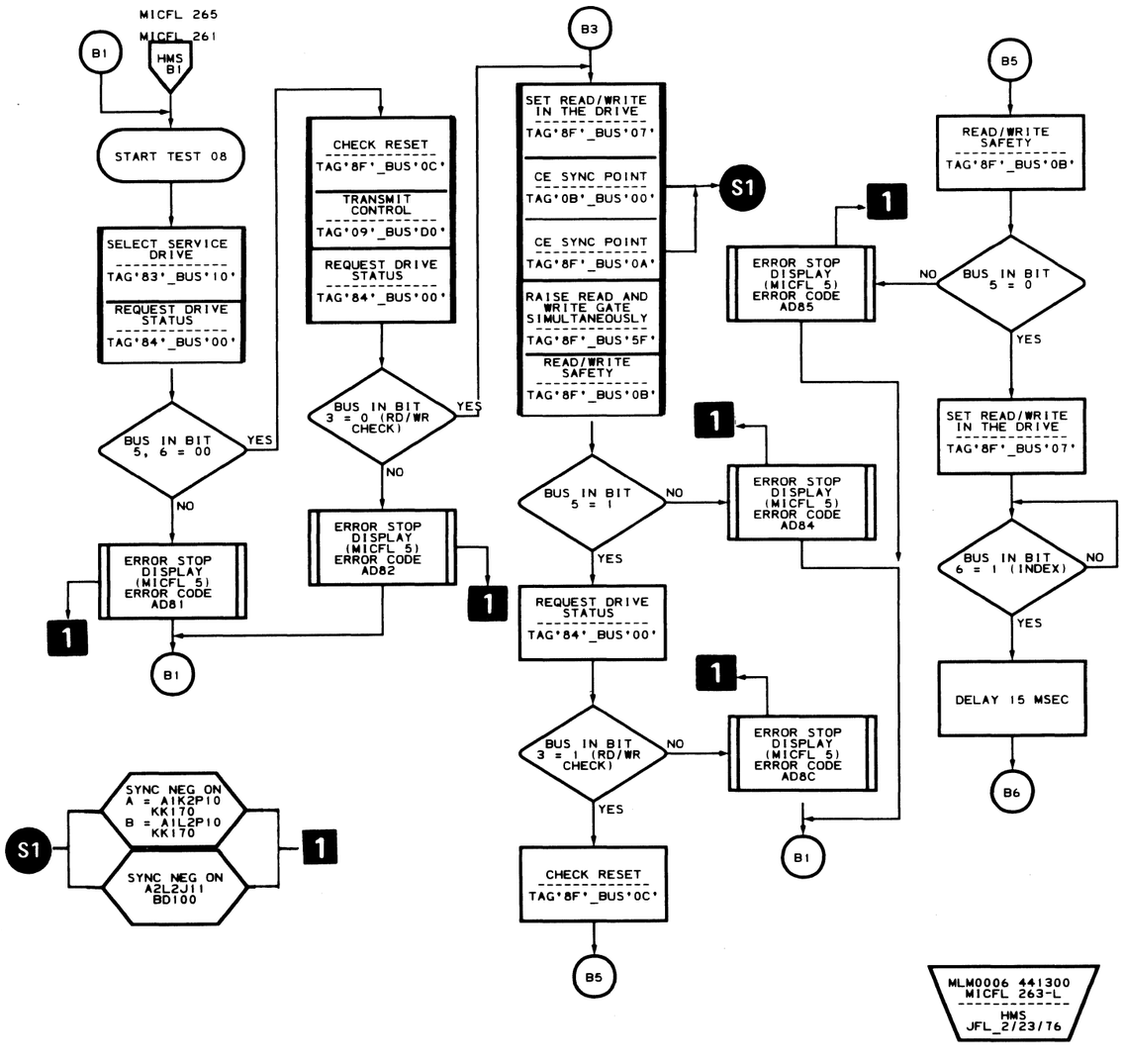
ROUTINE AD – GAP COUNTER AND DATA TRANSFER TESTS

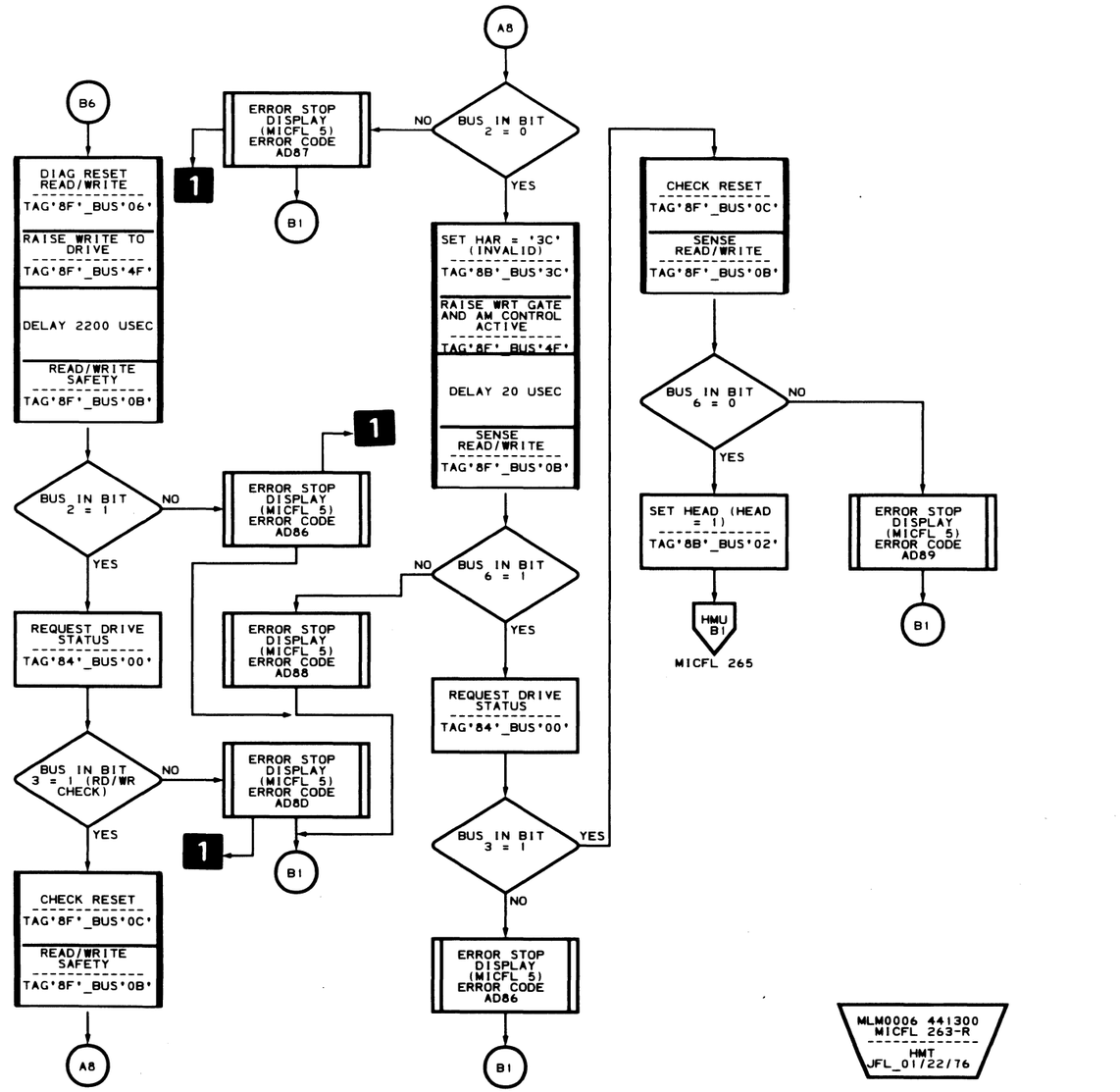






ROUTINE AD – GAP COUNTER AND DATA TRANSFER TESTS





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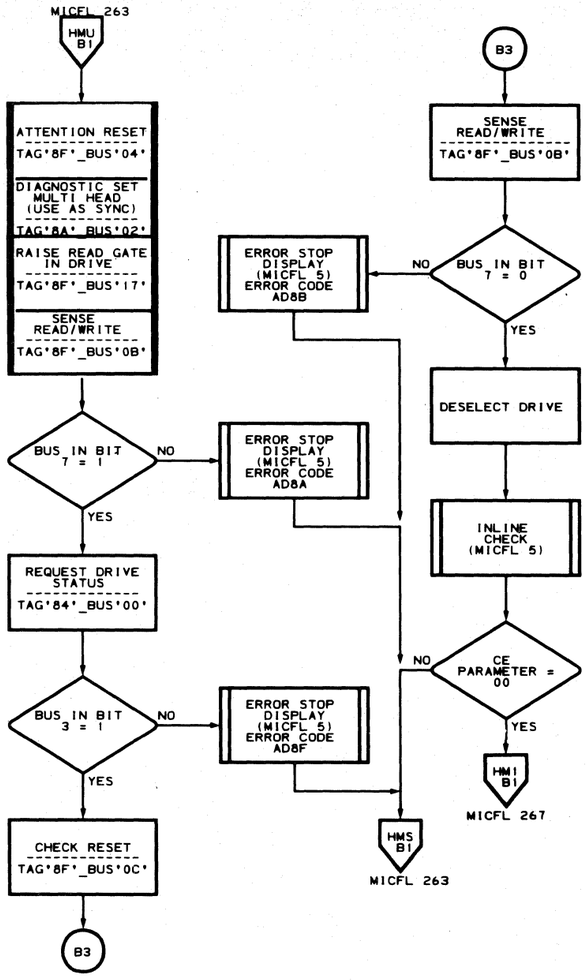

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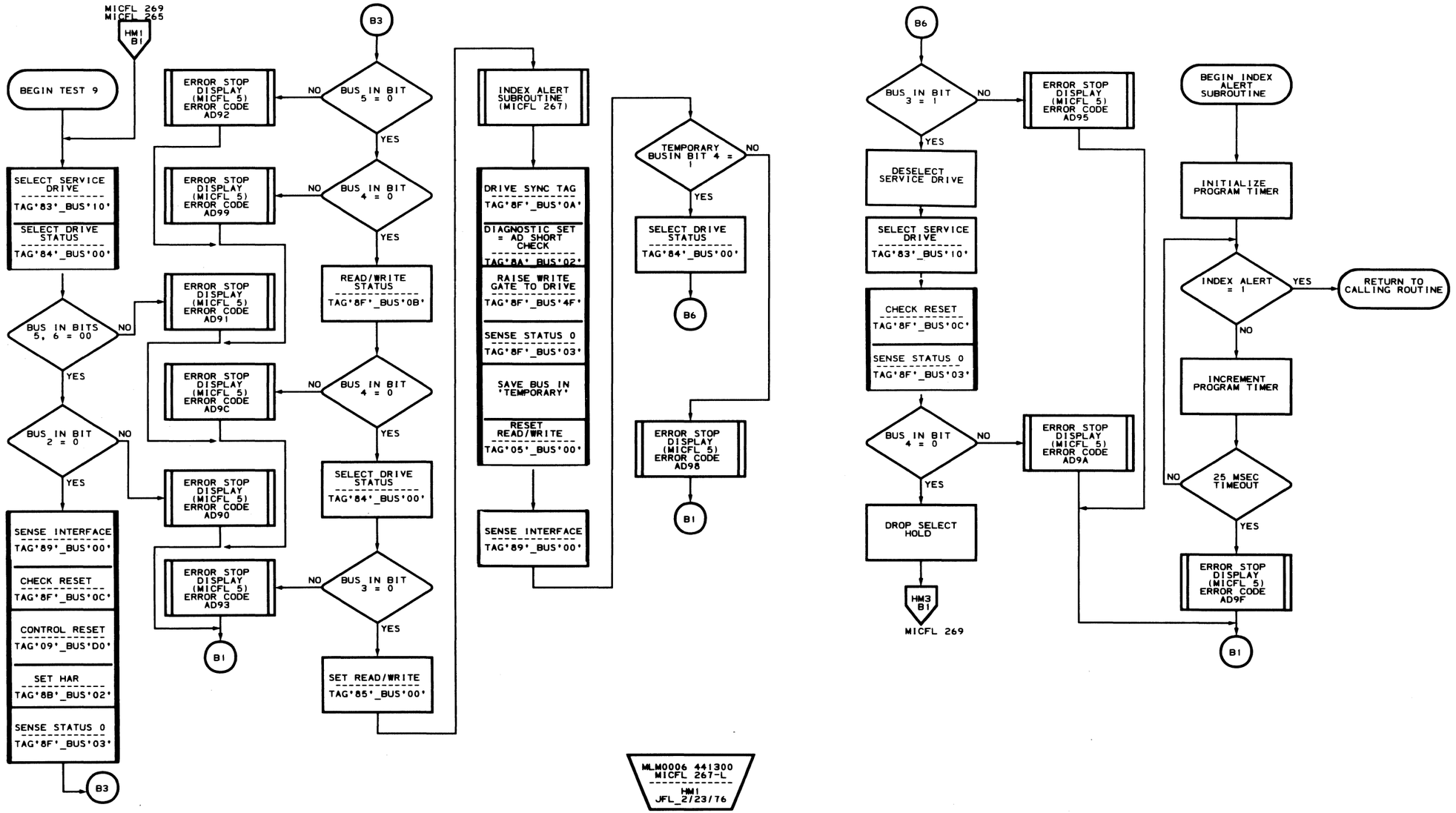
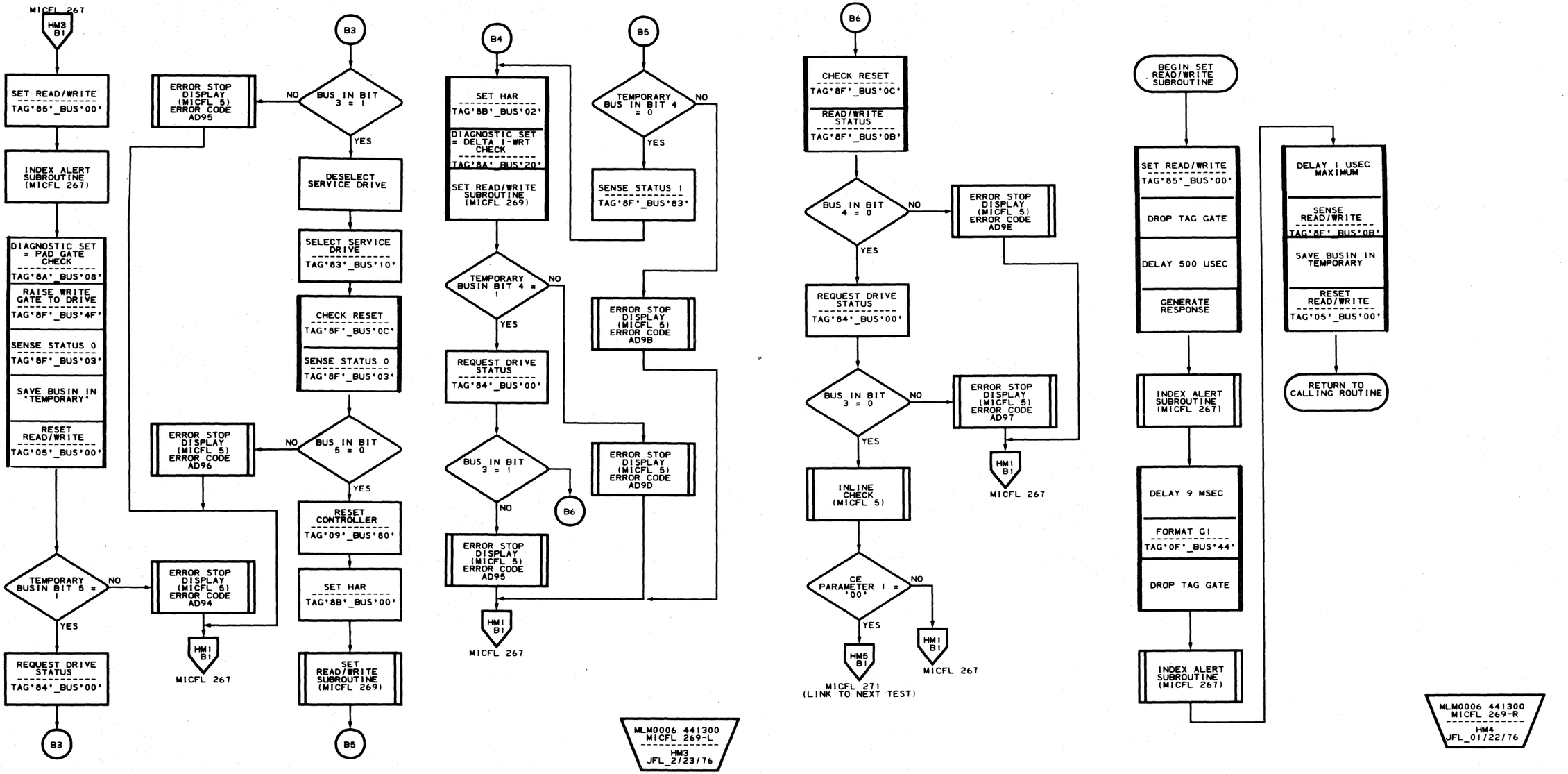
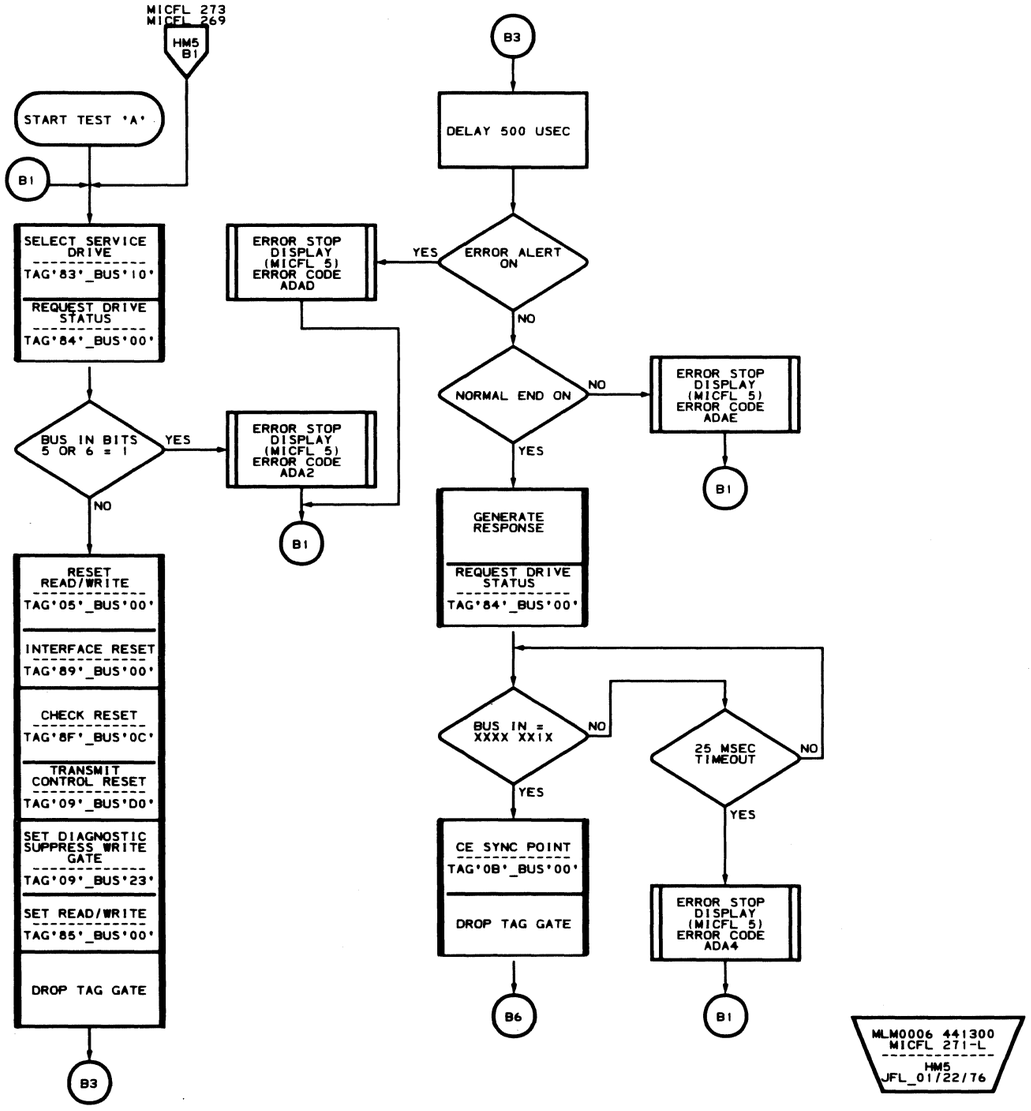
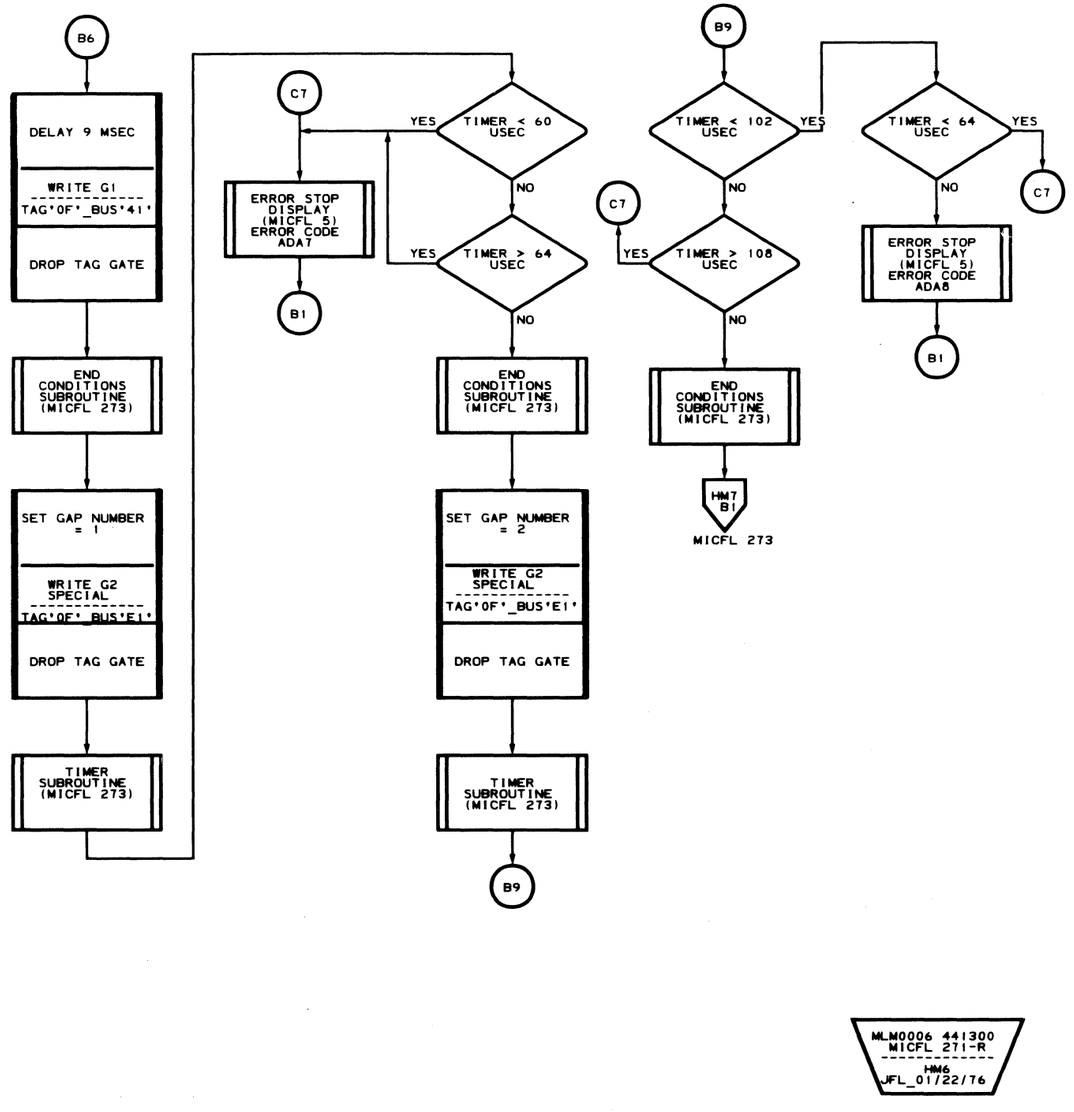
ROUTINE AD – GAP COUNTER AND DATA TRANSFER TESTS

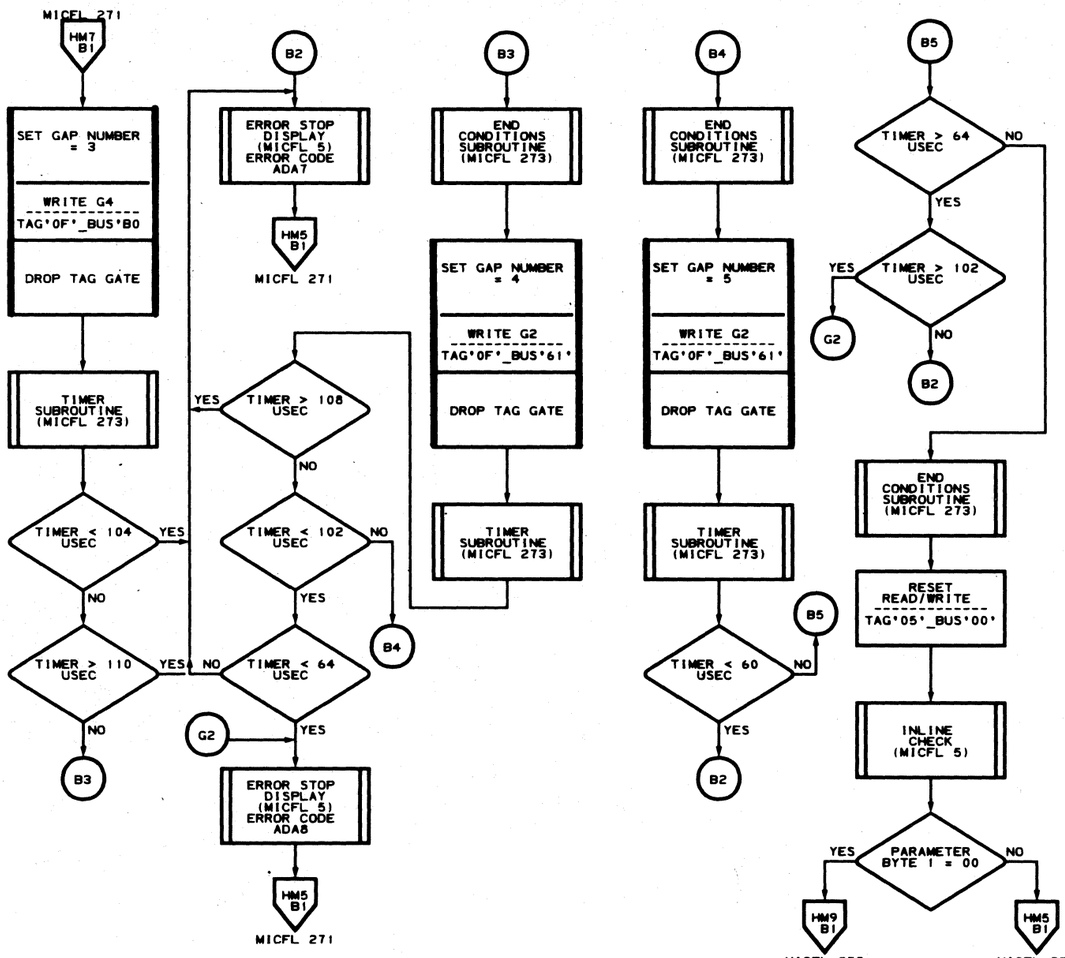


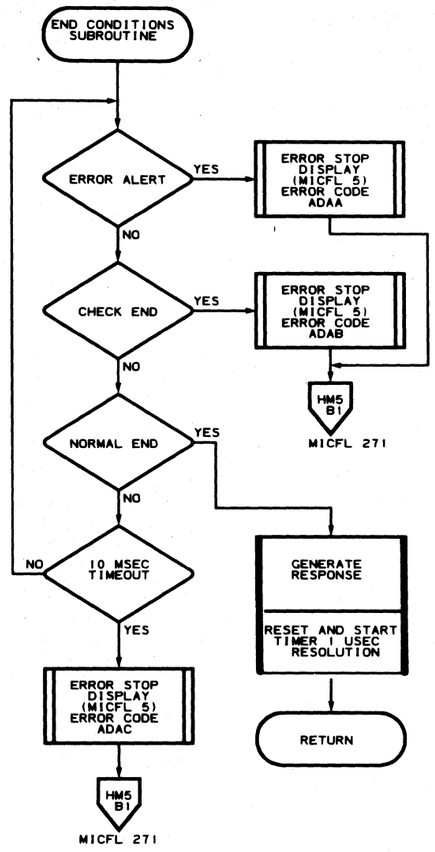


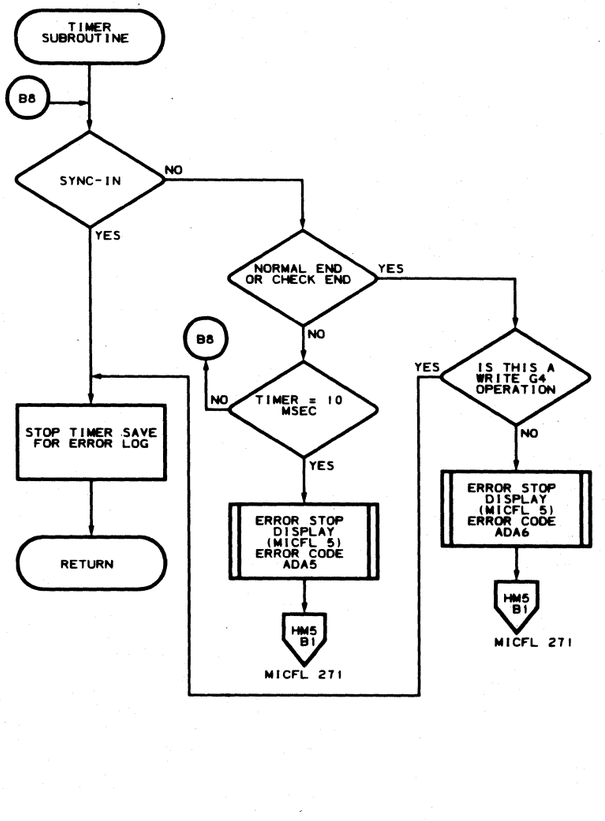
ROUTINE AD – GAP COUNTER AND DATA TRANSFER TESTS











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MICFL 273-R
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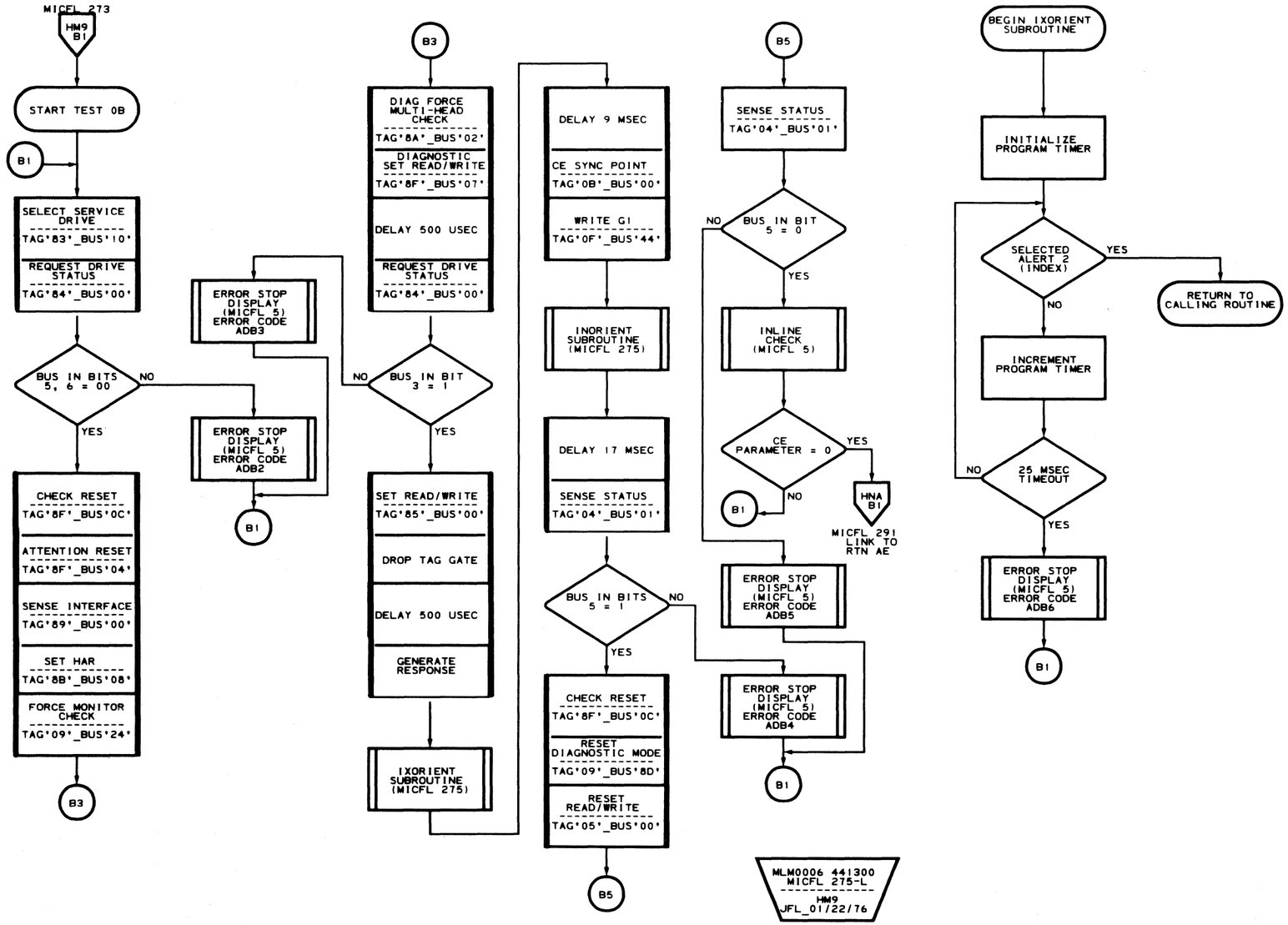
ROUTINE AD – GAP COUNTER AND DATA TRANSFER TESTS



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ROUTINE AE – 3350 ECC LOGIC TEST

DESCRIPTION

To execute routine AE, the CE drive must be Online and the R/W Read switch must be in the R/W position. Each time routine AE is selected the following initialization sequence occurs:

1. **The access is rezeroed.**
2. **A seek to the CE Write Track is issued.**
3. **Test selection is checked and execution is begun at the correct point.**

Test 01. ECC Reset

Test 01 issues a Read G1 command with a short byte count (byte count = 4). This operation allows the ECC hardware to begin check character generation in the data area and causes an ECC Data Check to occur. The ECC Zeros Detect bit is checked to be sure that the ECC registers are loaded.

Write G2 is issued and allowed to proceed to Gap G4 time (the ECC registers are reset at Gap G3). A Sense Controller Error 2 Tag is issued and the Zeros Detect bit is checked to be sure that the ECC registers are reset.

Test 02. ECC Correction Pattern Register

Test 02 checks that all bits under control of the sense correction pattern tags operate correctly. A 7-byte data pattern is written, then read back as a 1-byte pattern. The pattern is such that the correction pattern register is loaded with 'FDF5'. The remaining bits are tested during test 4.

Test 03. ECC Read Normal Data

Test 03 ensures that the ECC hardware can read an error-free data pattern and produce the correct ending conditions. The ECC write functions are not tested during this phase. During step 1 a 7-byte data pattern is written in the G2 position on the CE track. The 7-byte pattern consists of 1 byte of data and 6 bytes of simulated ECC data.

During step 2, the 1 data byte is read back and the ECC hardware generates the check characters from the remaining 6 bytes. The ending conditions are then checked for the proper results.

Test 04. ECC Read Correctable Data Check

The first two steps of Test 04 are similar to Test 03 except that the data pattern used is one that produces a correctable data check.

After the pattern has been written, read back, and the ending status checked, an ECC Correct Op Tag is issued. The correct operation is allowed to proceed to some end condition. After the end condition is received, the Displacement counter, Pattern registers, and ending status are checked for proper results.

Test 05. ECC Read Uncorrectable Data Check

Test 05 is the same as Test 04, except that an uncorrectable data pattern is used.

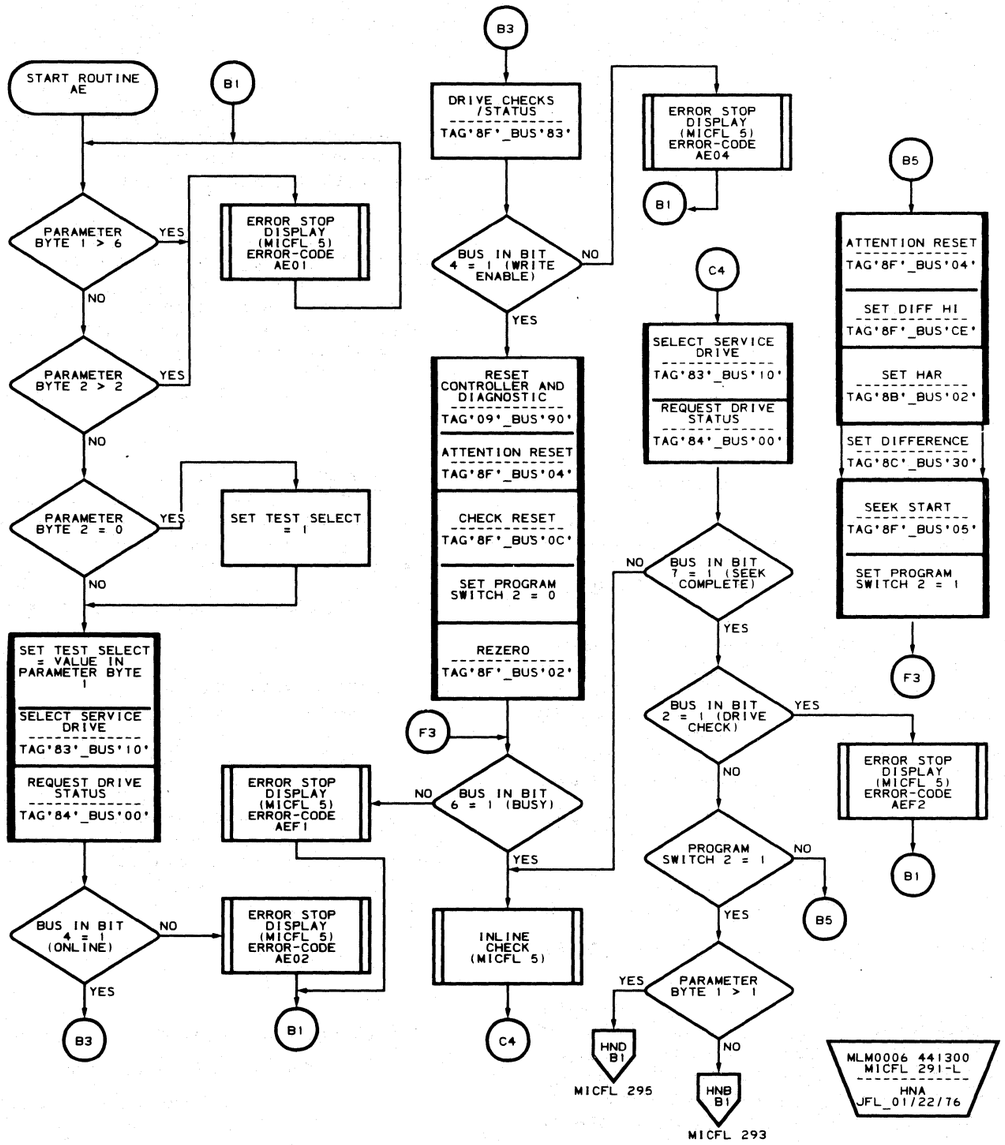
Test 06. ECC Write Burst (ECC Check Pattern)

During Test 06, the ability of the ECC hardware to gate the check character bytes to the serializer is checked by writing a 1-byte data pattern. This allows the ECC hardware to gate the 6 predetermined check bytes to the serializer. The 7-byte data and check pattern is read back (ECC Data Check is ignored) and compared byte-for-byte with what was written.

OPERATING PROCEDURE

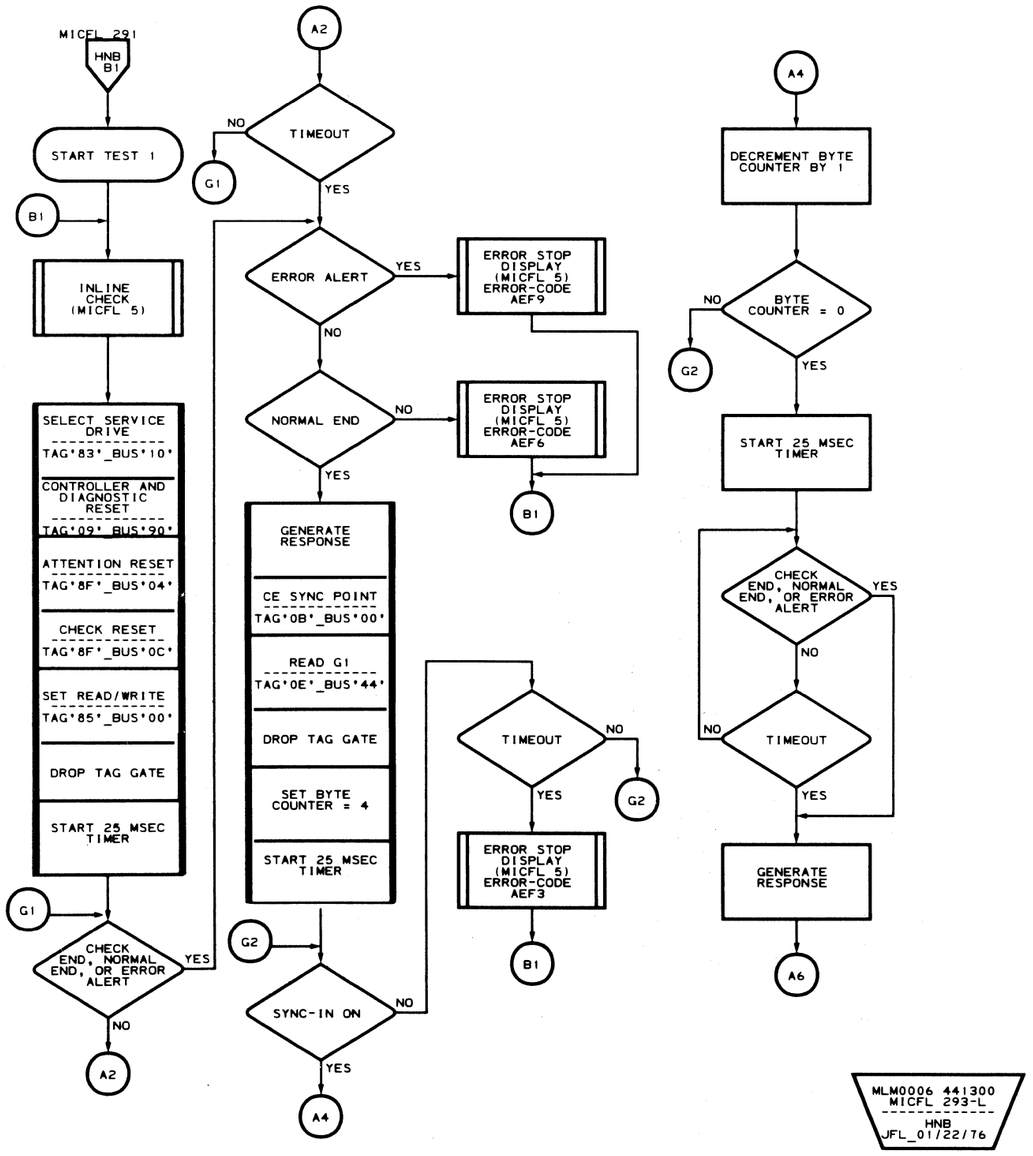
- **Refer to MICRO 10 and 11 for standard operating procedures.**
- **Refer to microdiagnostic reference charts starting on MICRO 30 for parameter entry.**

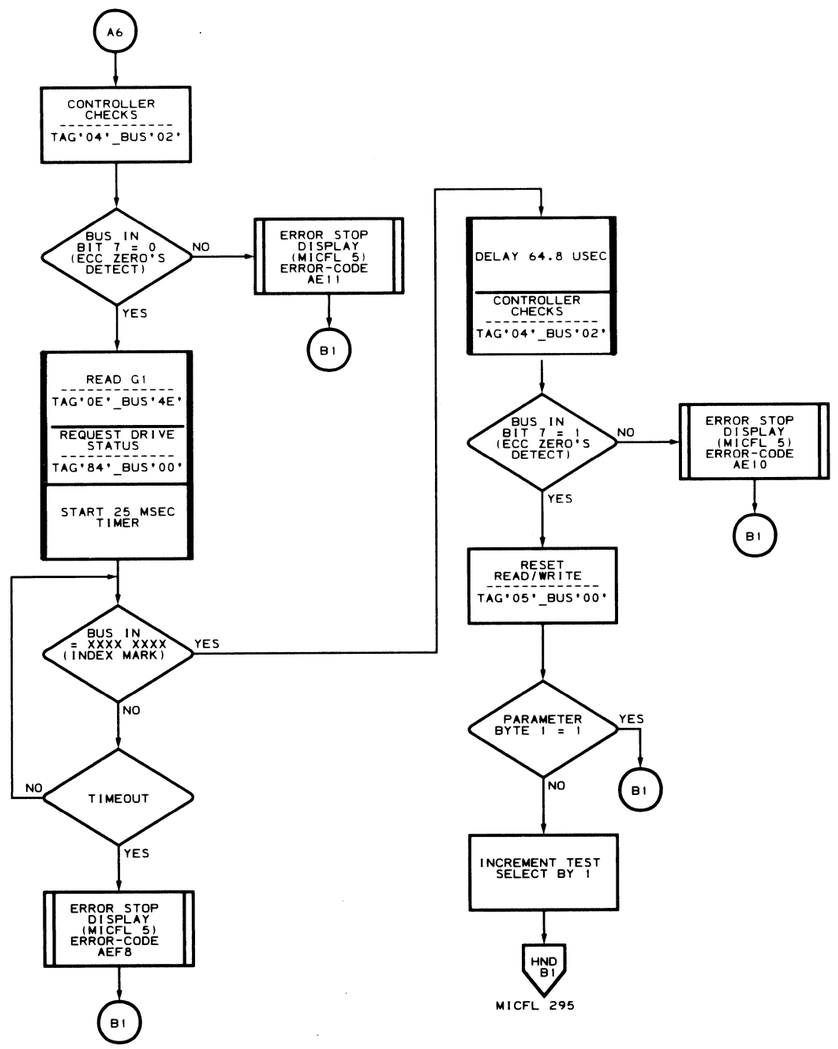
ROUTINE AE – ECC LOGIC TESTS MICFL 291

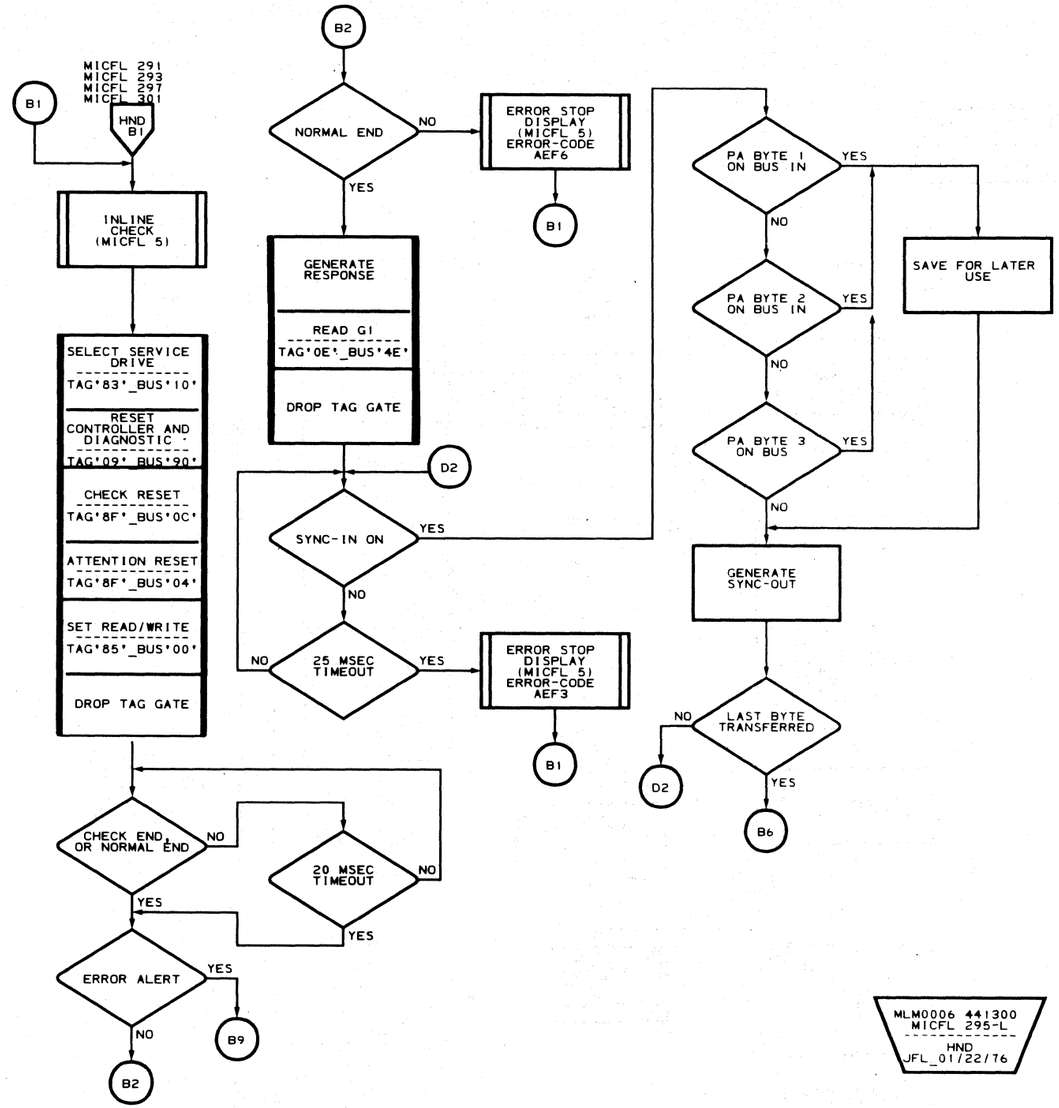


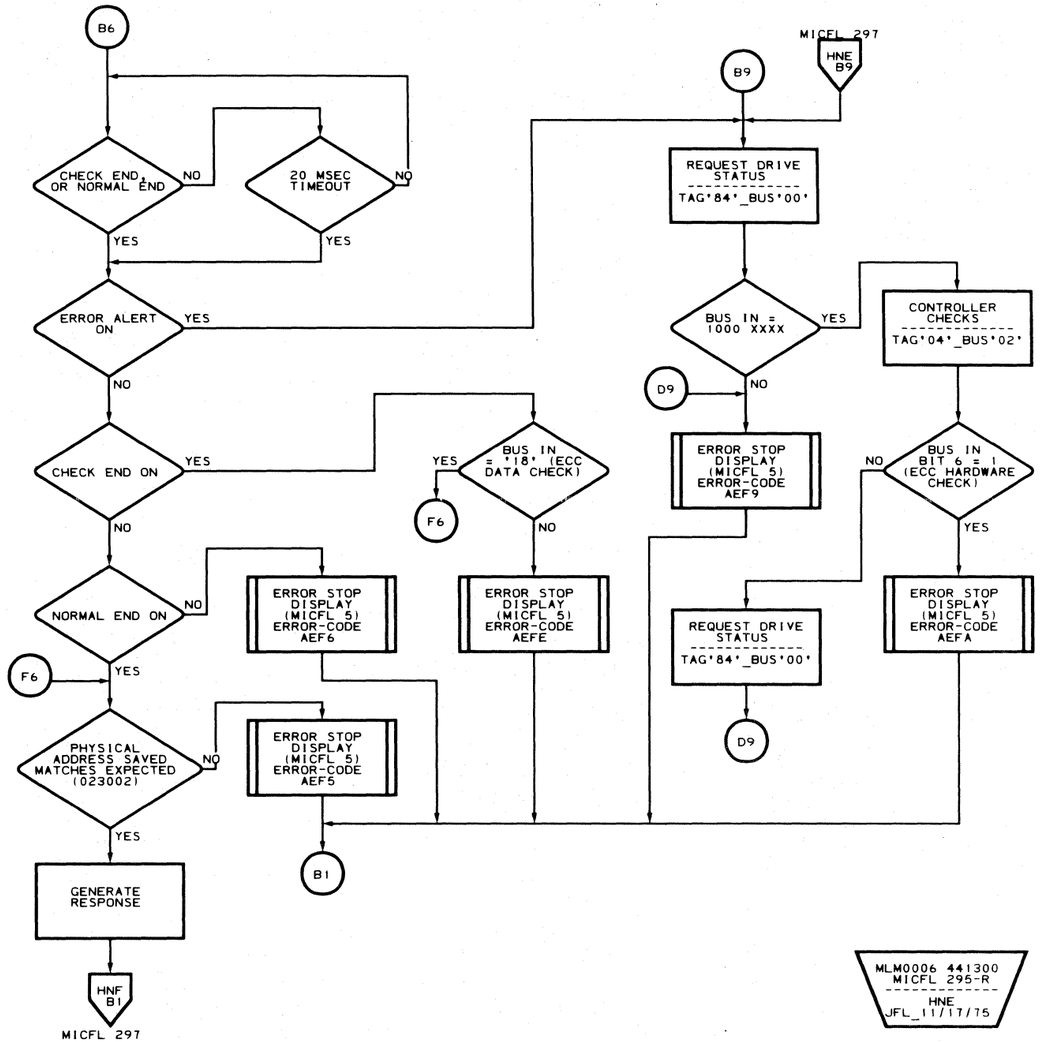
ROUTINE AE – ECC LOGIC TESTS MICFL 291

ROUTINE AE – ECC LOGIC TESTS

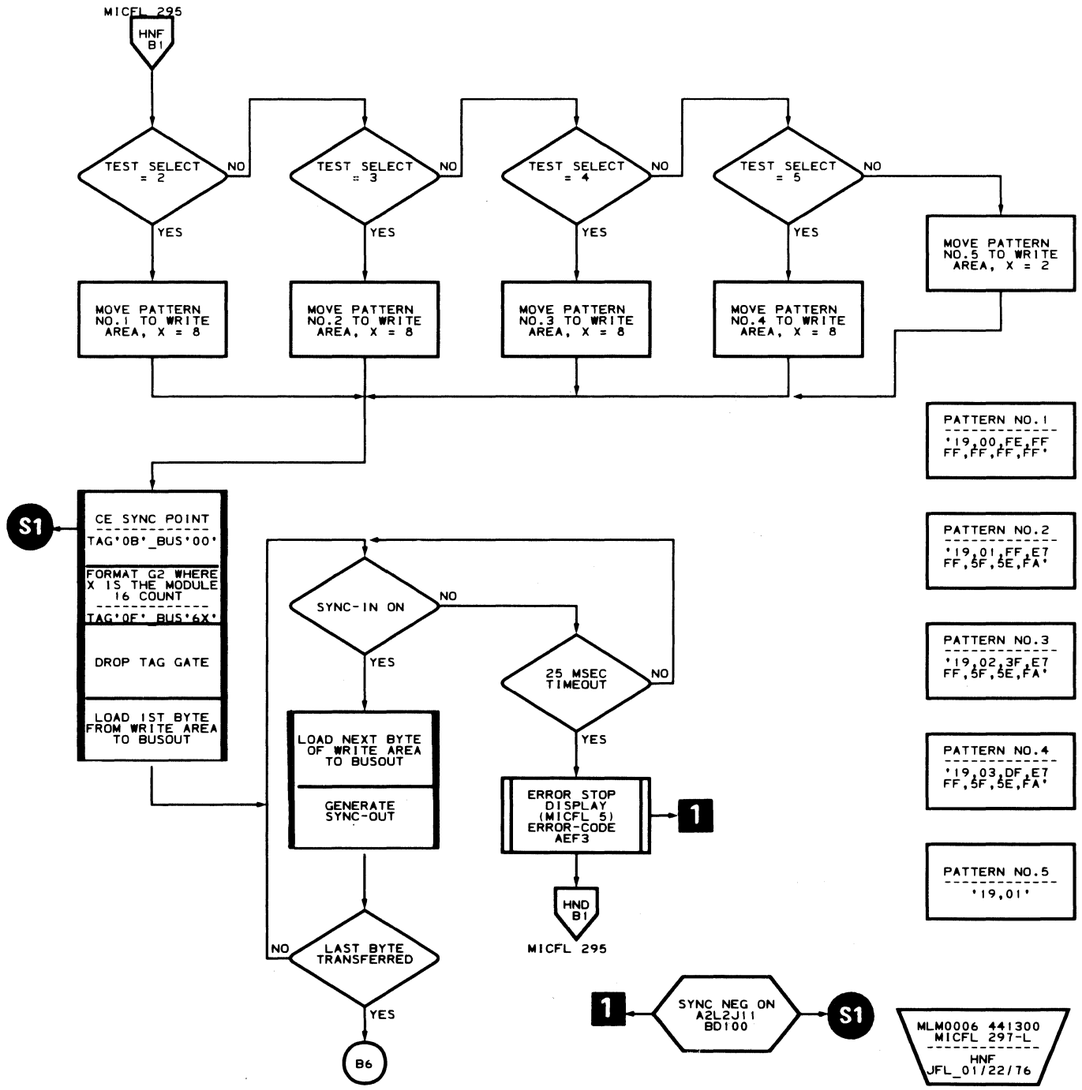


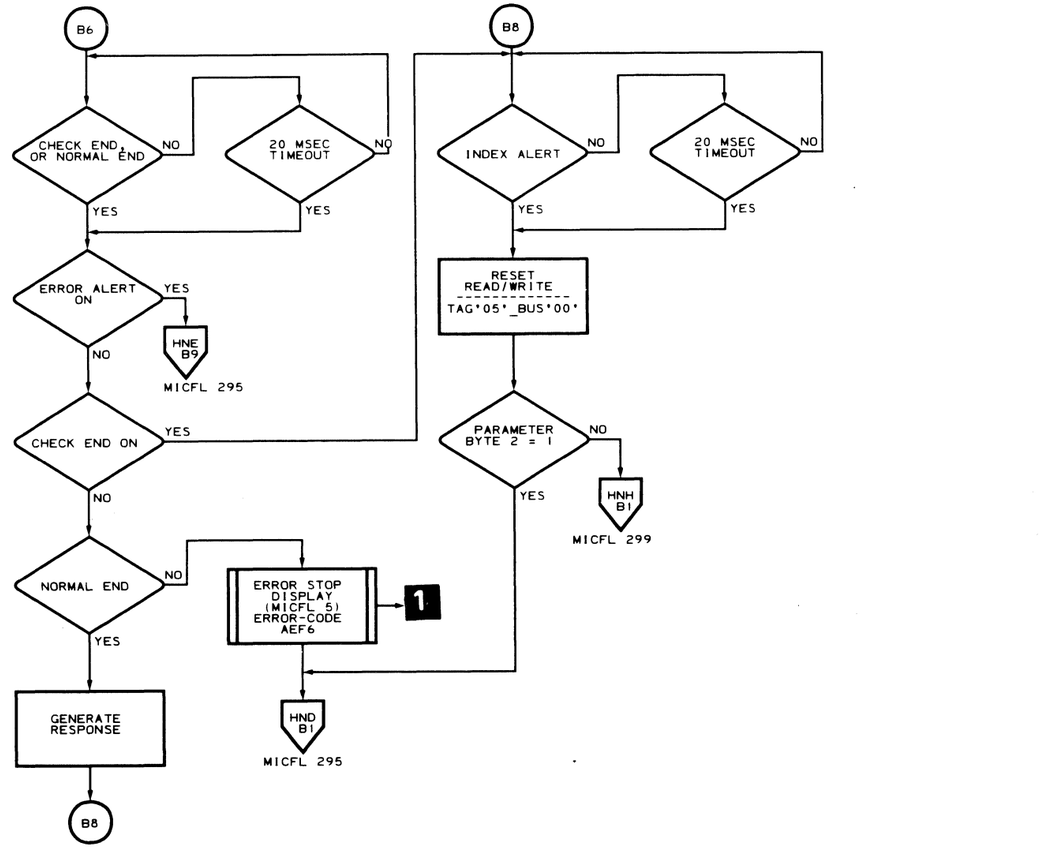


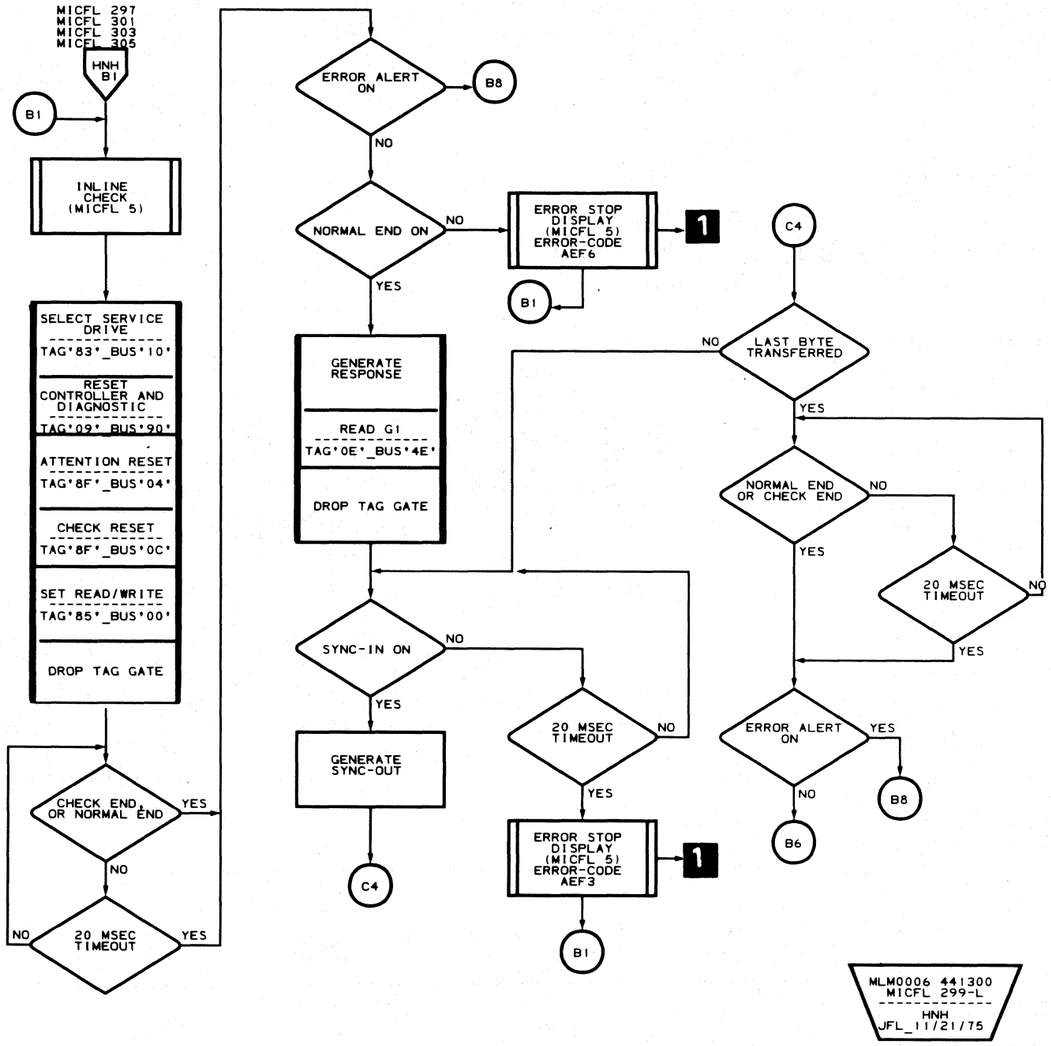




ROUTINE AE – ECC LOGIC TESTS







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MICFL 299-L
HNH
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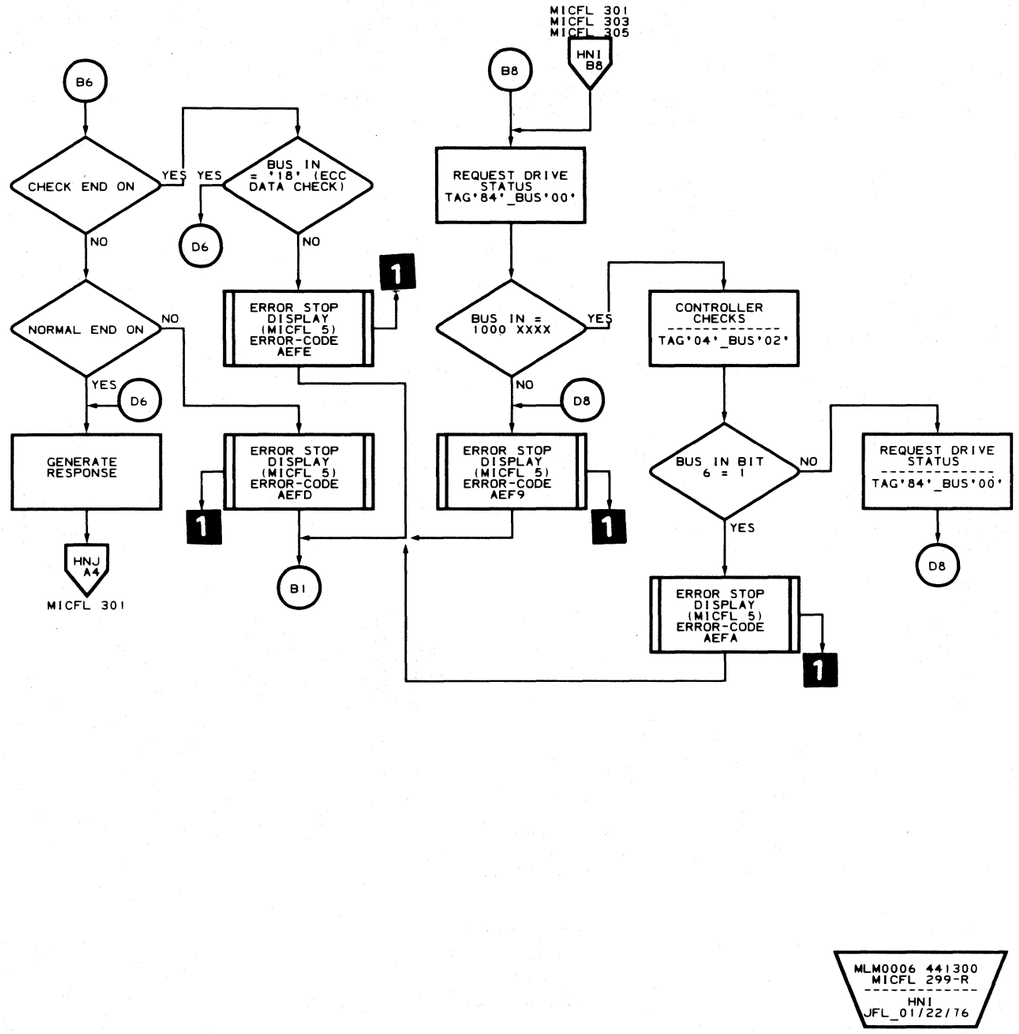

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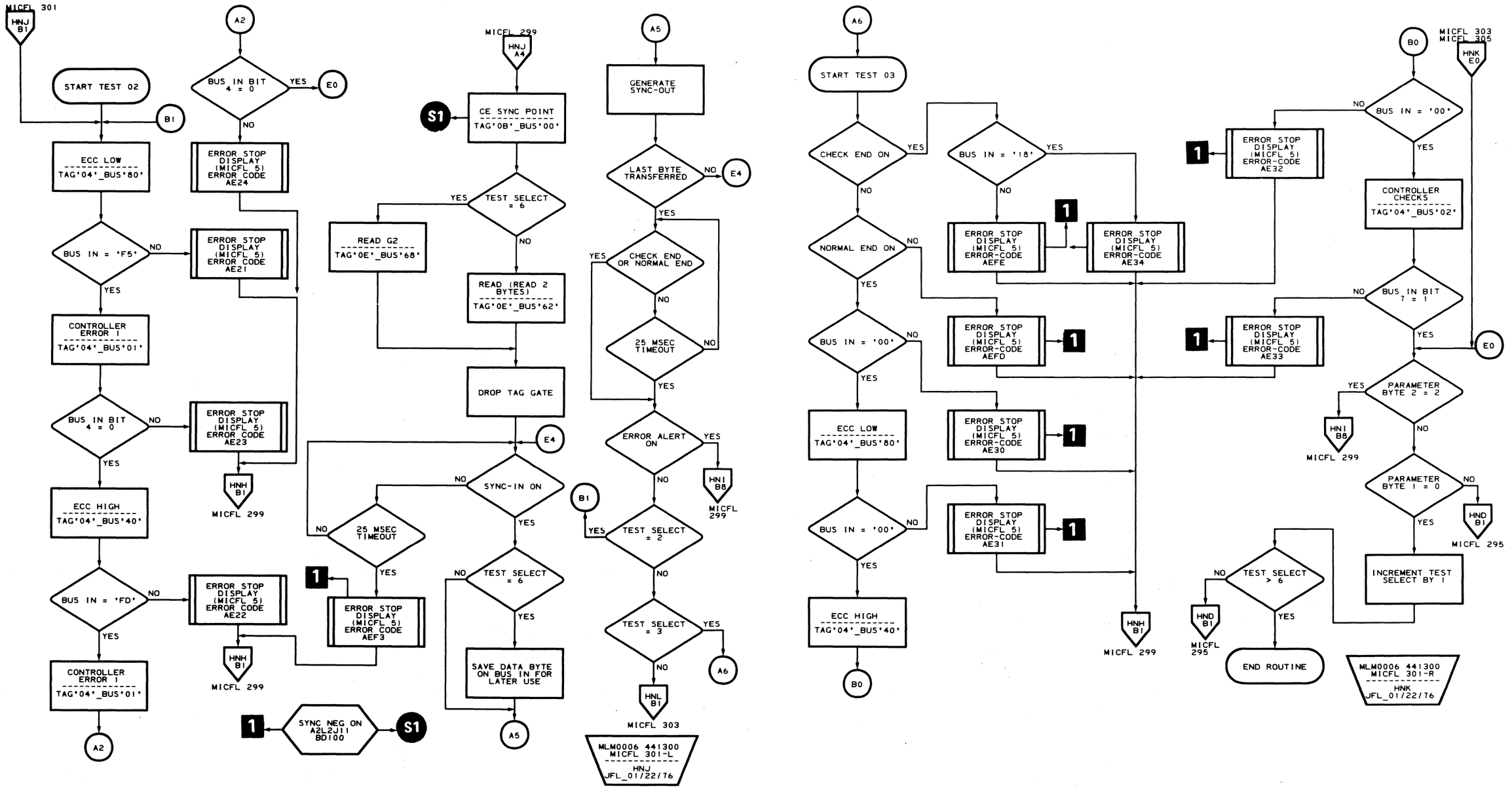
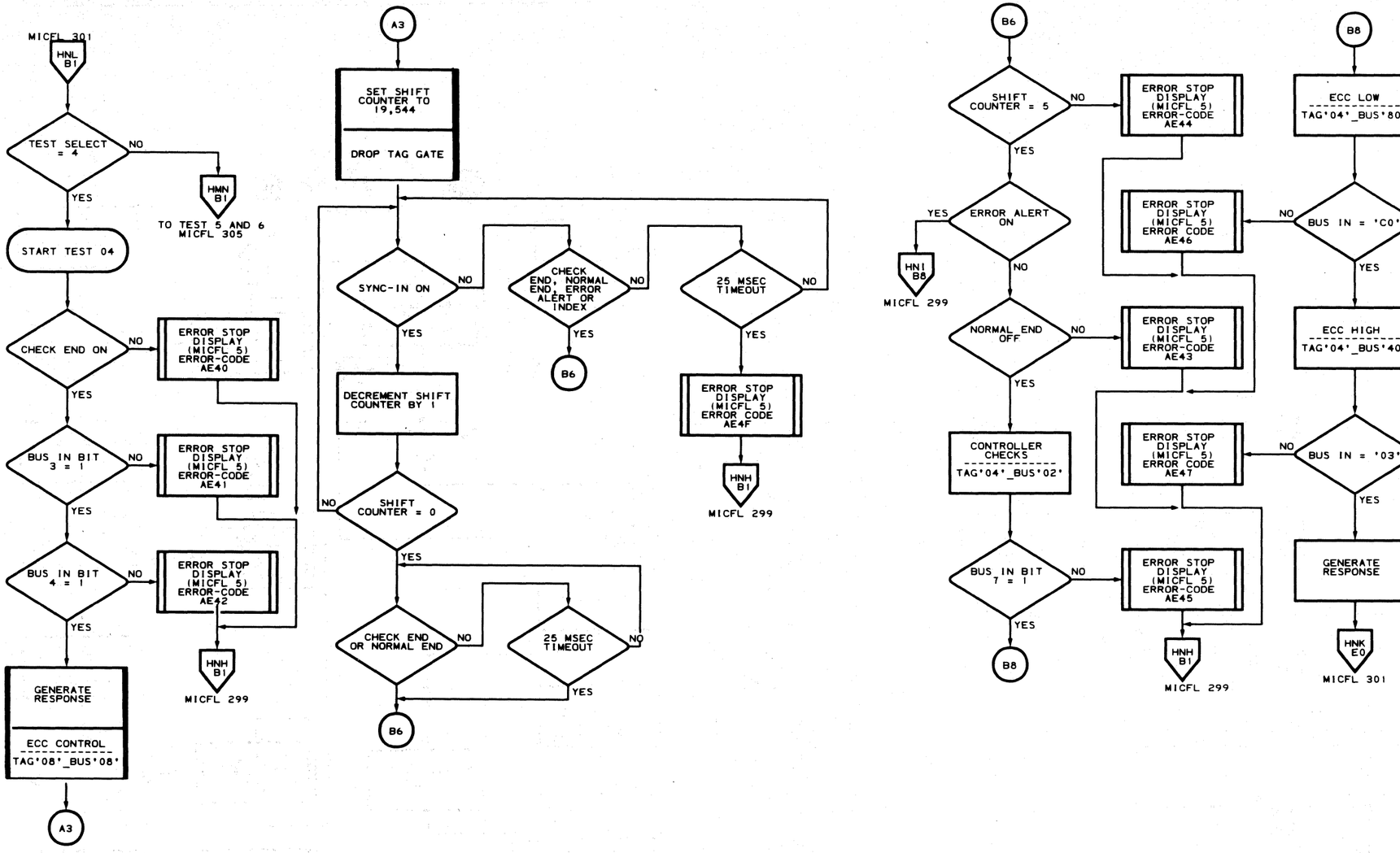
MICFL 299-R
HNI
JFL_01/22/76





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MICFL 303-R
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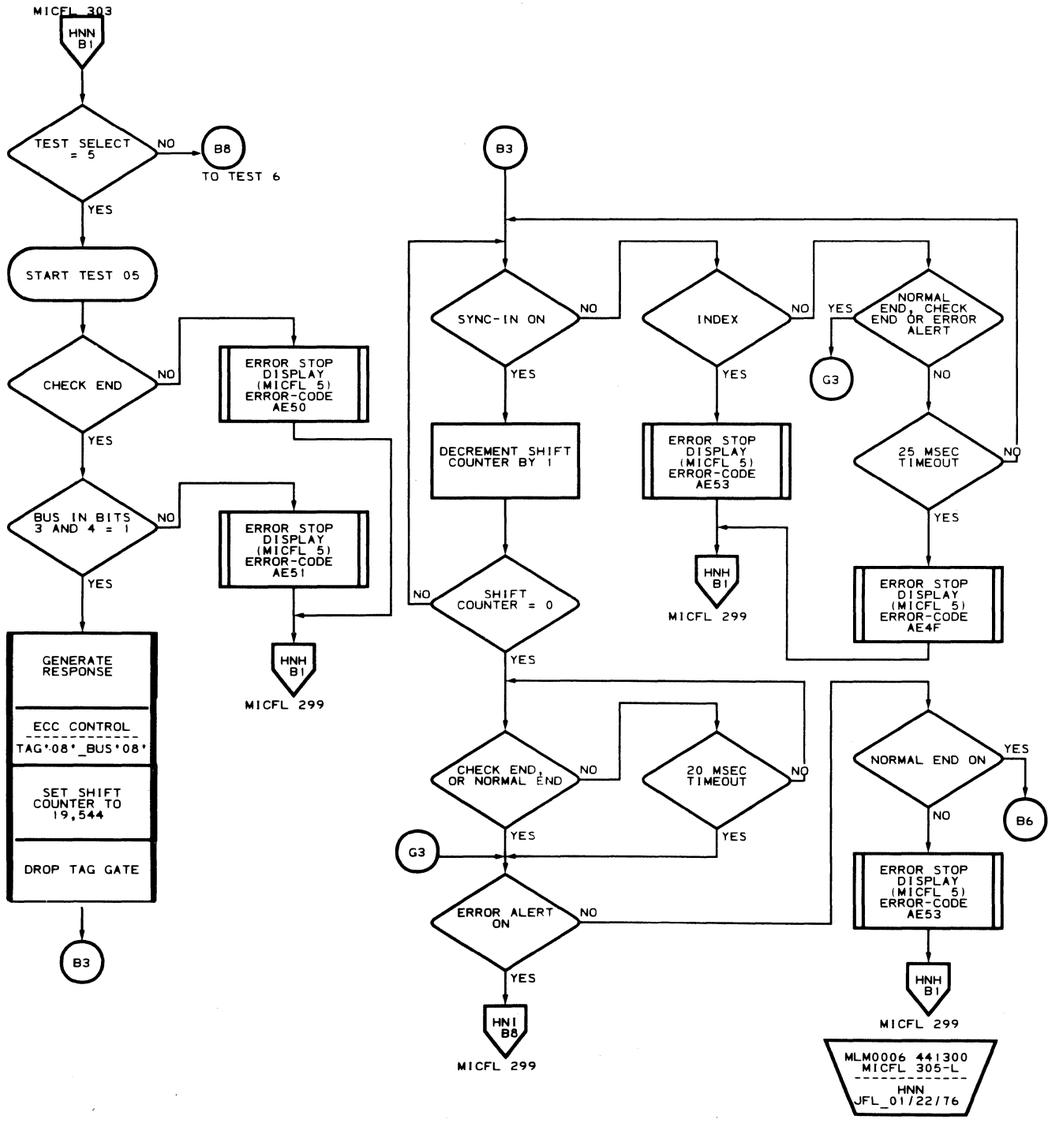
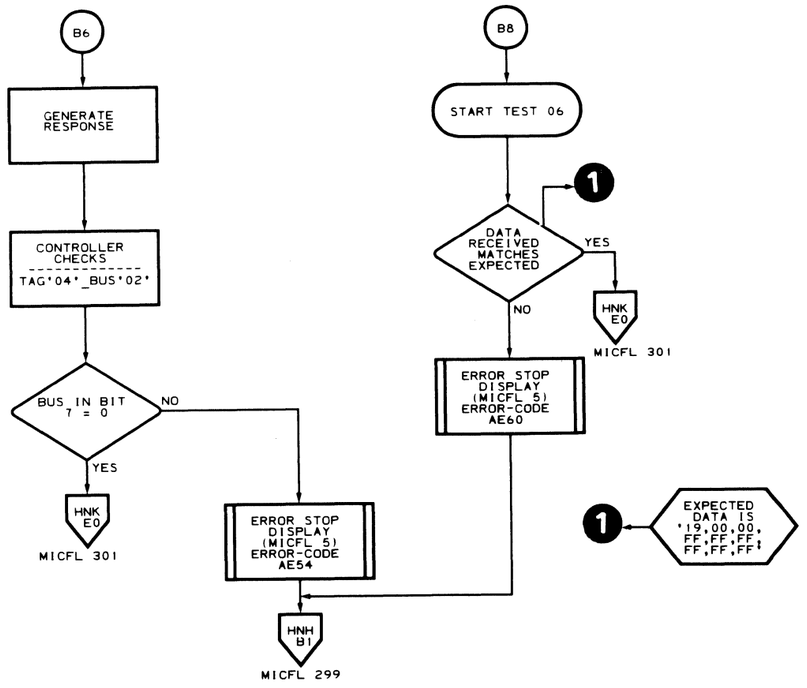
ROUTINE AE – ECC LOGIC TESTS





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ROUTINE AF – 3350 FORMAT READ/WRITE TESTS

DESCRIPTION

Routine AF, which checks the hardware associated with Read and Write commands, consists of 15 tests ('01' through '0F'). In normal operation (default Parameter 1 = '00'), all tests are executed in sequence.

Optional parameter entry may be used to restrict operation to a single test. If a single test is selected, it loops indefinitely until halted by the CE or an error halt occurs.

All tests use physical cylinder 560, Physical Head 1, odd track, with the exception of the initial seek verification (Read G1), which uses Physical Head 2, even track, of the same cylinder.

Test All Initialization

Prior to the start of any of the tests, this step verifies that the CE parameter 1 entry is valid. The routine verifies that the CE drive is Online and Write Enabled. It initiates a Rezero operation, verifies that the drive becomes Busy, and that normal completion of the operation occurs within 220 milliseconds. The routine seeks to cylinder 560 in one operation (head 01 selected), checks for normal completion of the operation within 220 milliseconds, and checks for drive status to include: No Drive Check, No Busy, and Seek Complete.

The routine verifies that Index is present within 21 milliseconds. If Index is present, the routine attempts to verify that the seek to the CE cylinder was performed correctly by reading Home Address from the Read Only track at head 02. It then compares Bytes PA1, PA2 amd PA3 for validity. If the comparison is not successful, the routine logs out an appropriate error message. The CE has the option of retrying the verification (by entering '00' to retry) or bypassing further verification of the Seek operation and going directly to the specified test through use of parameter 2.

Note: *Extreme caution must be used in exercising the option to continue the tests. It is possible to destroy customer data if a hardware malfunction occurs that prevents successful Seek operation.*

If the routine cannot successfully verify head position with a Read G1 (Home Address) operation, the password parameter allows the CE to bypass the seek verification and continue the Write G1 test for restoration of the Home Address.

Note: *This password parameter must be used very carefully and only when there is no possibility of destroying customer data. The pack must be backed up by the customer.*

If all criteria for restrictive use of parameter 2 are met, restart Routine AF by inserting Parameter 1 = Test number (format Write G1 Test = '0E') and Parameter 2 = Password (Valid Password = '02').

The routine executes the Seek and Verify operations and stops with an error command that indicates the verification failed. Enter '00', this forces the routine to reset the HAR = 01. Continue to Test '0E'. After the G1 (HA) field is successfully restored, the CE must manually stop Test '0E', restart routine 'AF', and specify the desired (or default) test. If parameters are entered by the CE, Parameter 2 should be set to '00' (default), which gives maximum protection against inadvertent destruction of customer data.

Test 01. Read G1 Unoriented Status, Read and Verify Home Address Physical Address Bytes

Test 01 verifies that Read G1 Unoriented status is not on continuously by orienting on Index, then initiating a Read G1 operation, looking for Bus In bit 6 = 0 while Tag Gate is active. The test initiates a Read G1 operation and checks the 6th, 7th, and 8th bytes for '023002', respectively (Cylinder 560 head 01). The test also verifies that Read G1 Unoriented can be set on by initiating another Read G1 after orientation has been lost and checking for the unoriented status condition on Bus In with Tag Valid status.

Test 02. Oriented/Unoriented Borderline

Test 02 attempts to locate the borderline between Oriented and Unoriented by initiating a Read G1 operation. It delays a maximum allowable time without losing orientation (41 microseconds), then initiates a Read G2 operation, and checks for no Command Overrun and no Unoriented status.

The test repeats the above sequence of events using a delay large enough to force loss of orientation (45 microseconds) and checks for Command Overrun ending status.

Test 03. Force Command Overrun and Check End

Test 03 forces Command Overrun in both Read and Write modes by orienting on Index. It then initiates a Write G2 operation (with the Diagnostic Inhibit Write Gate Mode active) and checks for a Check End response with Command Overrun ending status.

The test orients again and initiates a Read G2 operation and looks for Check End response with Command Overrun ending status.

Test 04. Force Sync Out Timing Error and Force Status Overrun Error

Test 04 forces a Sync Out timing error by initiating a Write G1 operation (with Diagnostic Inhibit Write Gate mode active). It responds to only the first Sync In (inhibits Sync Out) and checks for a Check End response with Sync Out timing error ending status.

This test checks that Status Overrun can be set on by initiating a Write G2 operation, holding Tag Gate active for 100 microseconds, then looking for Bus In bit 4 = 1. The test then drops Tag Gate and looks for Bus In bit 4 = 0.

Test 05. Allow Head Address Register (HAR) and Transfer Sector Counter

Test 05 examines the Allow HAR function during Transfer Sector Counter and Read/Write mode of operation.

Set HAR = '00'.
Sense HAR, check that HAR = '00'.
Set Read/Write.
Orient on Index.
Wait approximately 20 microseconds (into the center region of the Allow HAR window).
Set HAR = '01'.
Wait approximately 100 microseconds (beyond the Allow HAR window).
Initiate a set HAR = '02' operation and reset Read/Write.
The test performs a sense HAR and checks for HAR = '01'.
If HAR does not = '01', an error has occurred.
If HAR = '00', HAR failed to set within the Allow HAR window.
If HAR = '02', the HAR was allowed to set outside the Allow HAR window during Read/Write mode.

The test verifies that the Transfer Sector Counter logic works properly by setting the Target Register to '7F', then initiating a dummy Read G1 operation. It then checks the Target Register for a value of '80' (RPS = 1, Sector = 00).

Test 06. Write Full Track G2 Field

Test 06 clocks through the HAR (G1) field, initiates a Write G2 operation and writes a full track (R0 count field) of 13,235 bytes for compatibility mode and 19,624 bytes for native mode. The test checks for no Error Alert and no Check End response after each operation.

Test 07. Write G2, Force Track Overrun

Test 07 clocks through the HA (G1) field, initiates a Write G2 operation and then initiates a Write G2 operation of greater-than-maximum track capacity of 13,468 bytes for compatibility mode and 19,840 bytes for native mode. The test checks for no Error Alert and Check End response with Track Overrun ending status following the Write G2 operation.

Test 08. Write G2/Format Write G2

Test 08 clocks through the HA (G1) field, initiates two Write G2 operations followed by a Format Write G2 operation. The test looks for no Error Alert and no Check End response following each operation. After the end response is received following the Format G2 operation, the test waits 5 milliseconds, reads drive status, and checks for I Write Sense (Bit 1 = 1). The test initiates a Reset Read/Write operation, again reads drive status, and checks for I Write Sense = 0.

Test 09. Read G2/Clock G2, Force No Sync Found

Note: *Test 09 depends upon successful completion of Test 08.*

Test 09 clocks through the HA (G1) field, initiates a Read G2 operation and checks for no Error Alert and no Check End response. The test then initiates a Clock G2 operation and checks for no Error Alert and no Check End response. The test then initiates a Read G2 operation on a non-existent G2 field, checks for no Error Alert and a Check End response with no Sync Found ending status.

Test 0A. Format Write G3/Read G3

Test 0A clocks through the HA (G1) field, initiates a Format Write G3 operation and checks for no Error Alert and no Check End response. The test again clocks through the HA field, initiates a Read G3 operation, reading the G3 field just written, and checks for no Error Alert and no Check End response. The test initiates a Read G2, looks for Check End on, No Sync Found on, and No Data Present.

ROUTINE AF – 3350 FORMAT READ/WRITE TESTS

DESCRIPTION (Continued)

Test 0B. Clock G3/Read G3 Address Mark Search

Note: *Test 0B depends upon successful completion of Test 0A.*

Test 0B clocks through the HA (G1) field, initiates a Clock G3 operation, reads the G3 field written by the previous test, and checks for no Check End response. The test again clocks through the HA field, initiates a Read G3 AM search operation, and checks for no Check End response.

Test 0C. Format Erase, Force No Address Mark Found

Test 0C clocks through the HA (G1) field, initiates a Format Erase operation, and checks for no Error Alert and no Check End response. The test again clocks through the HA field, initiates a Read G3 AM Search operation, and checks for Check End response with No Address Mark Found ending status.

Test 0D. Special Format Write G1/Read G1

Test 0D initiates a Special Format Write G1 operation and checks for no Error Alert and no Check End response. The test writes a valid G1 on cylinder 560, head 1.

The test initiates a Read G1 operation, to read the G1 field just written, and checks for no Error Alert and no Check End response.

Test 0E. Format Write G1/Read G1

Test 0E initiates a Format Write G1 operation and checks for no Error Alert and no Check End response. The test writes a valid G1 on cylinder 560, head 1.

The test initiates a Read G1 operation and checks for no Error Alert and no Check End response.

Test 0F. Skip Displacment Fields
Format Reorient
Format G3
Special Write G2
Write G4
Format G2

Test 0F ensures that a record can be written with an embedded G4 gap (simulating a defect within a data field). It ensures that a G3 record is on the track by reading through the HA (G1) field initiating a Format G2, a Format Write G3, and checking for no Error Alert and no Check End response.

The test writes a data record around the simulated defect by initiating the operations: Read G1, Format G2, Format G3, Format Reorient, Format G3, Special Write G2, Write G4, and a Format G2. A check is made for no Error Alert and no Check End response after each operation.

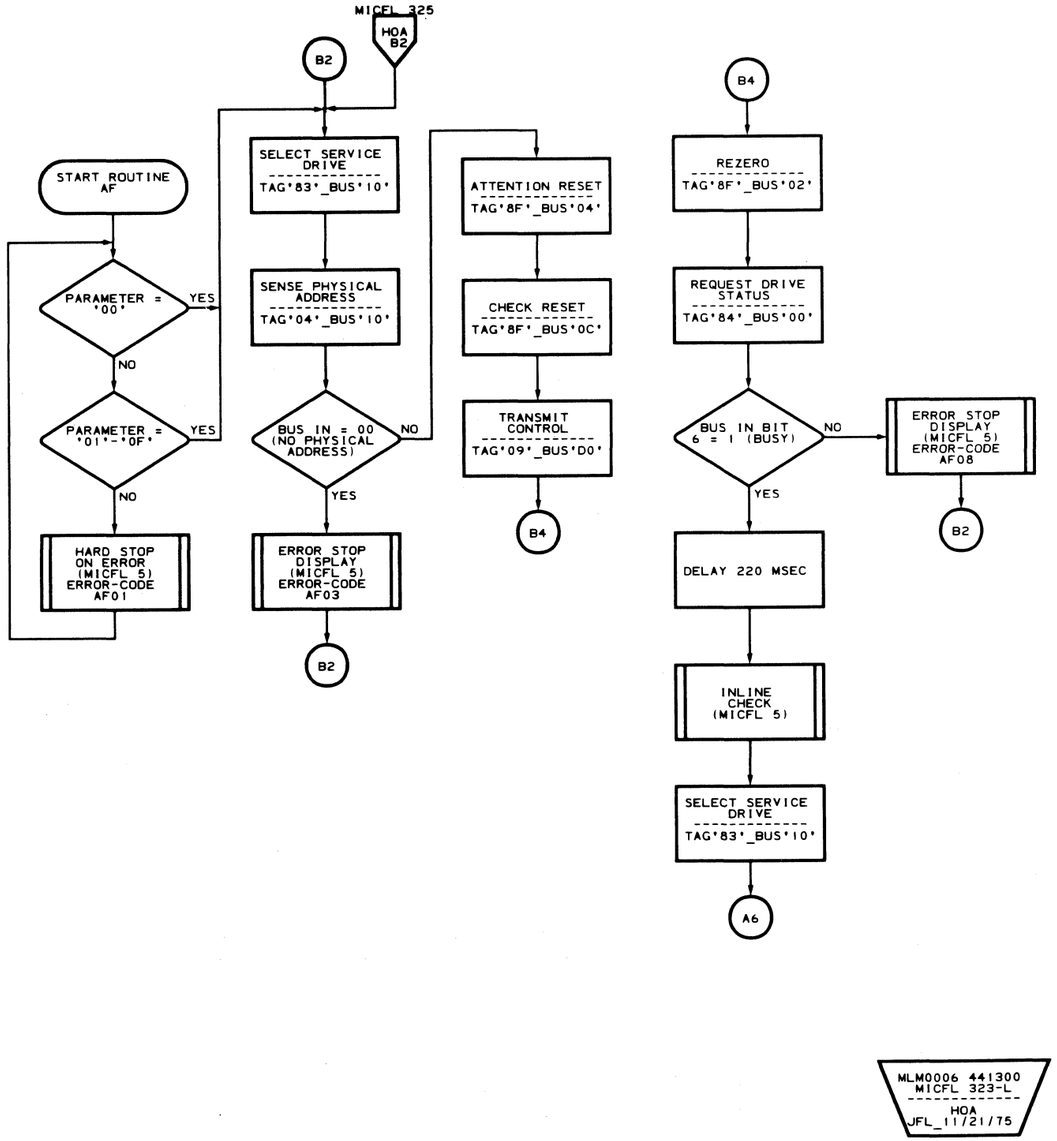
The test attempts to read back the record just written by initiating the following operations: Read G1, Read G2, Read G3, Read Special G2, Read G4, and Read G2. A check is made for no Error Alert and no Check End following each operation.

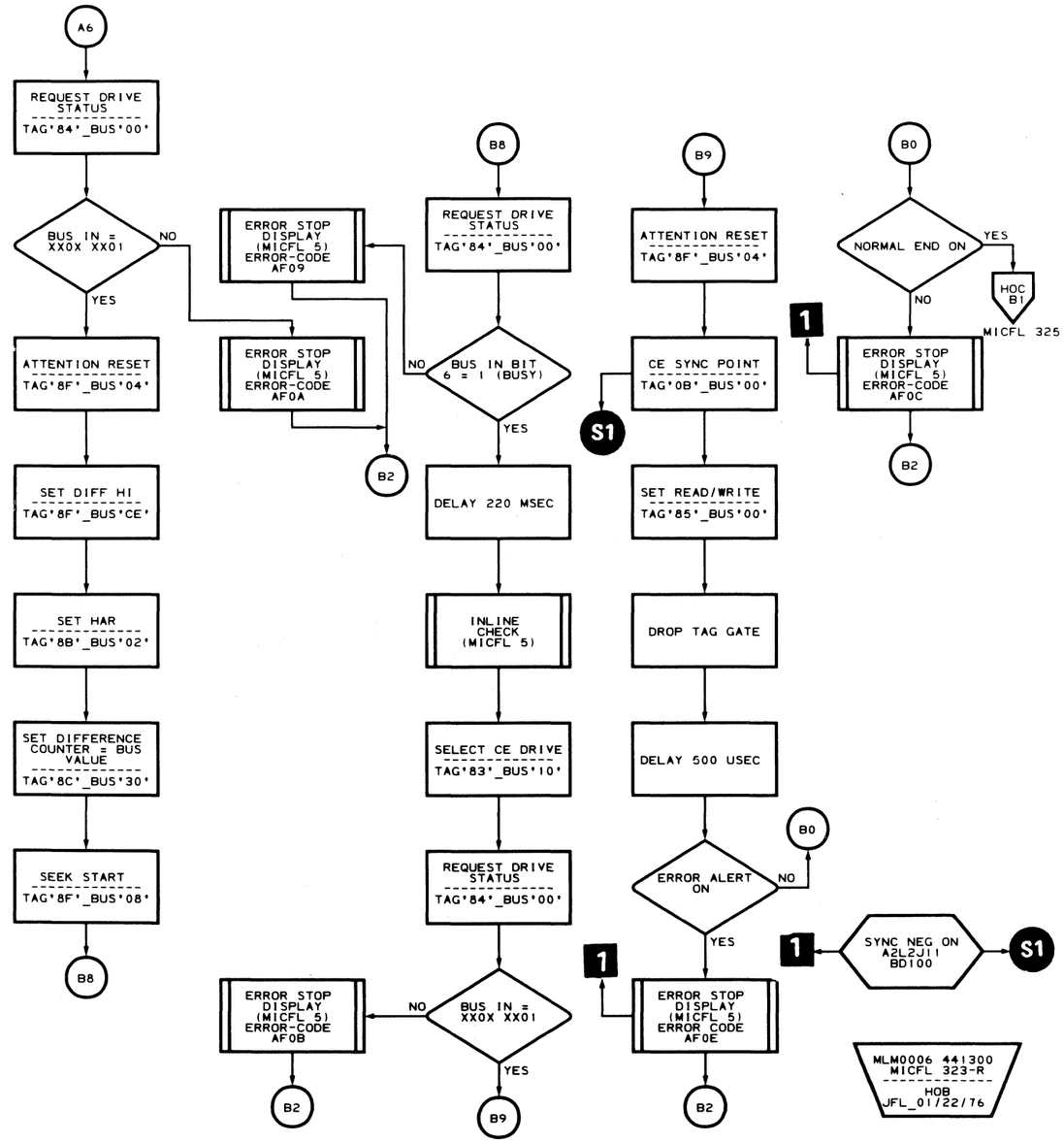
The test cleans up the track by initiating a Read G1 and a Format Erase.

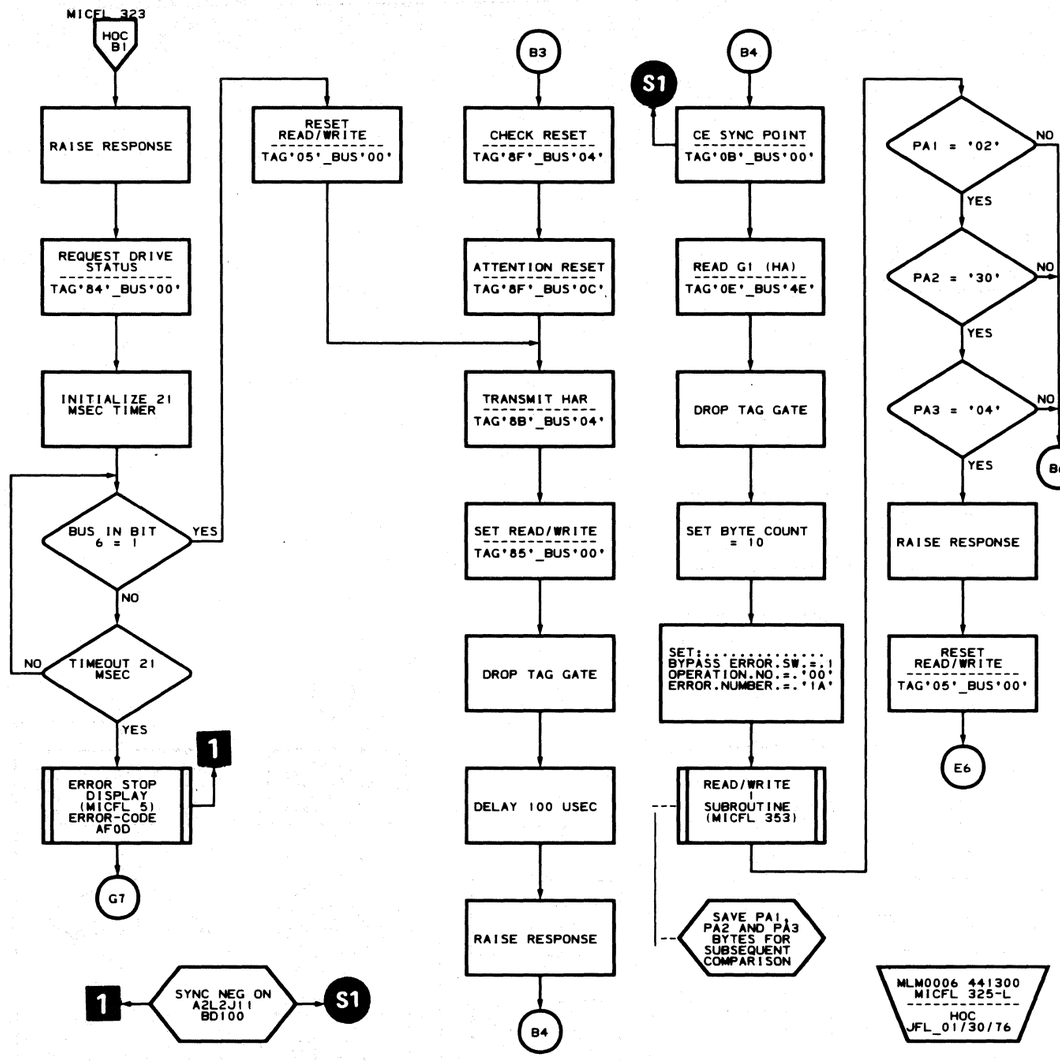
OPERATING PROCEDURE

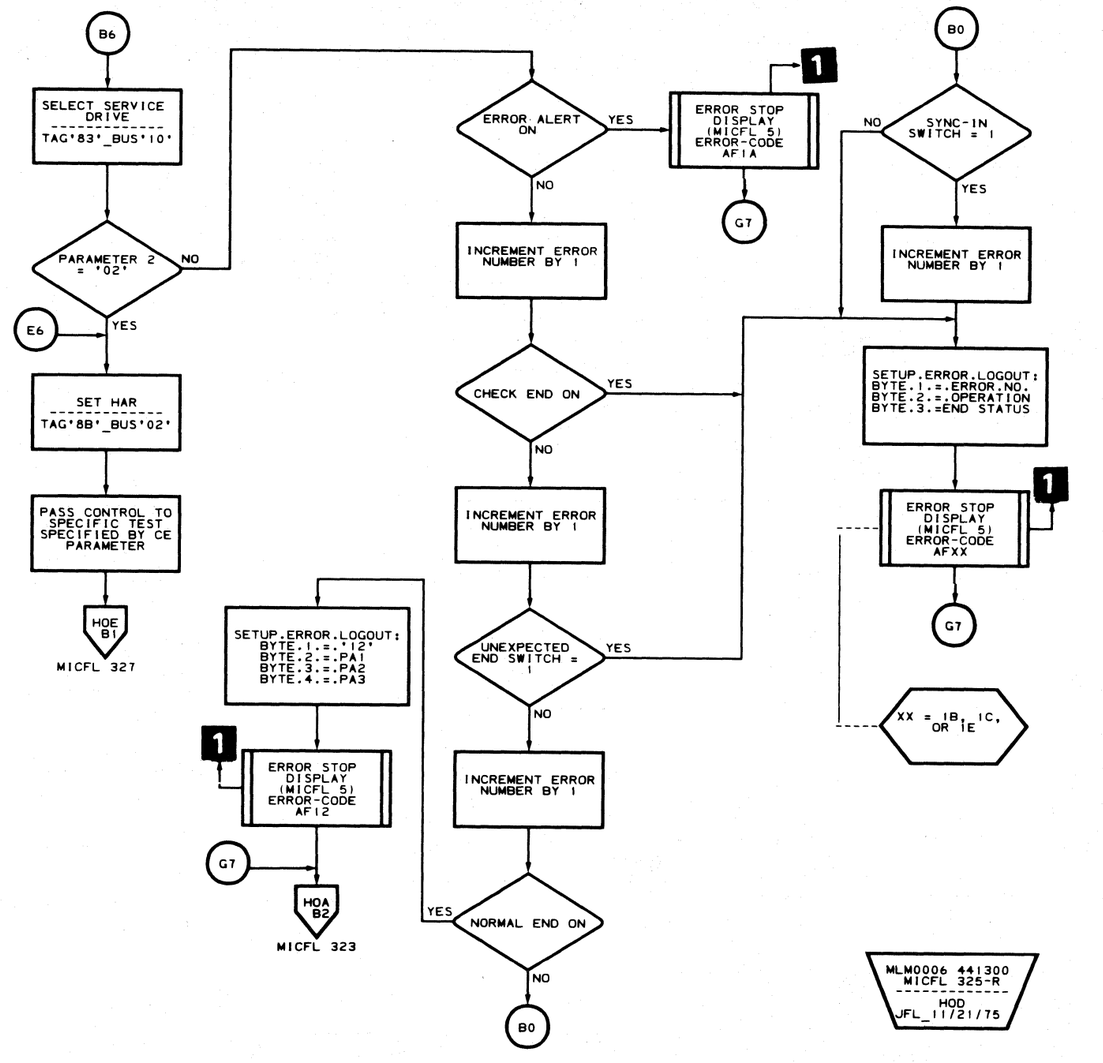
- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 32 for parameter entry.

ROUTINE AF – FORMAT READ/WRITE TESTS









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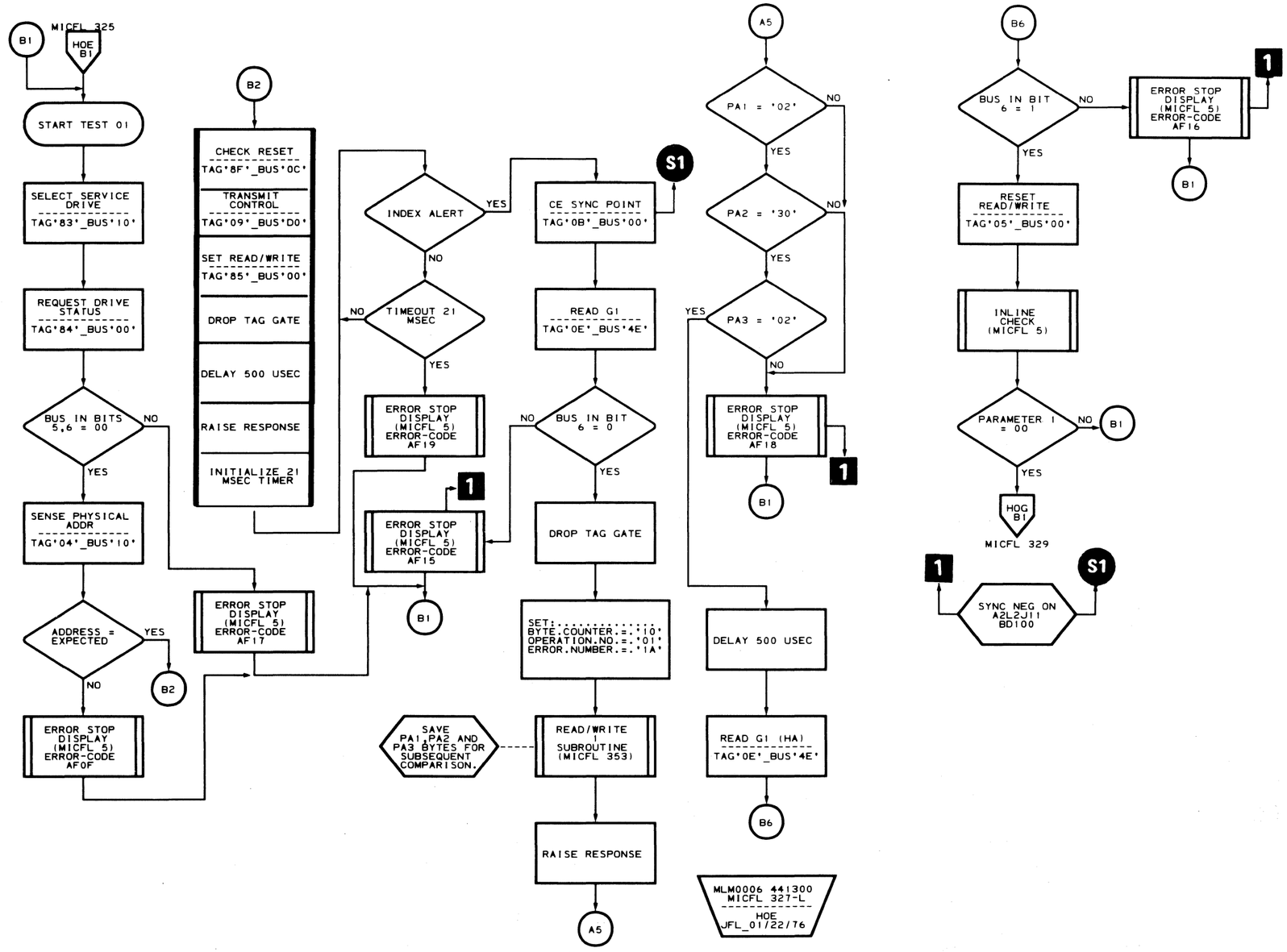
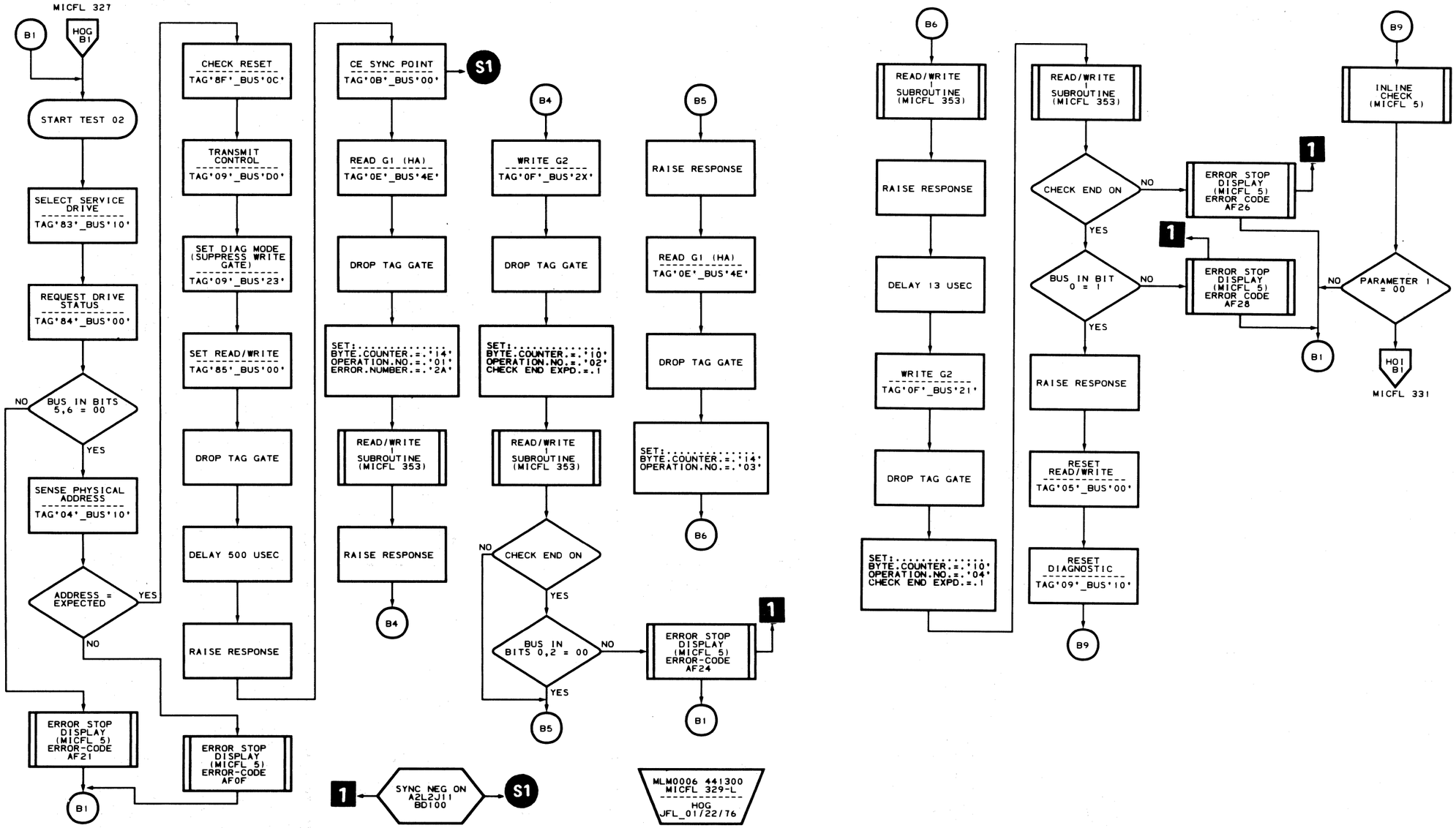
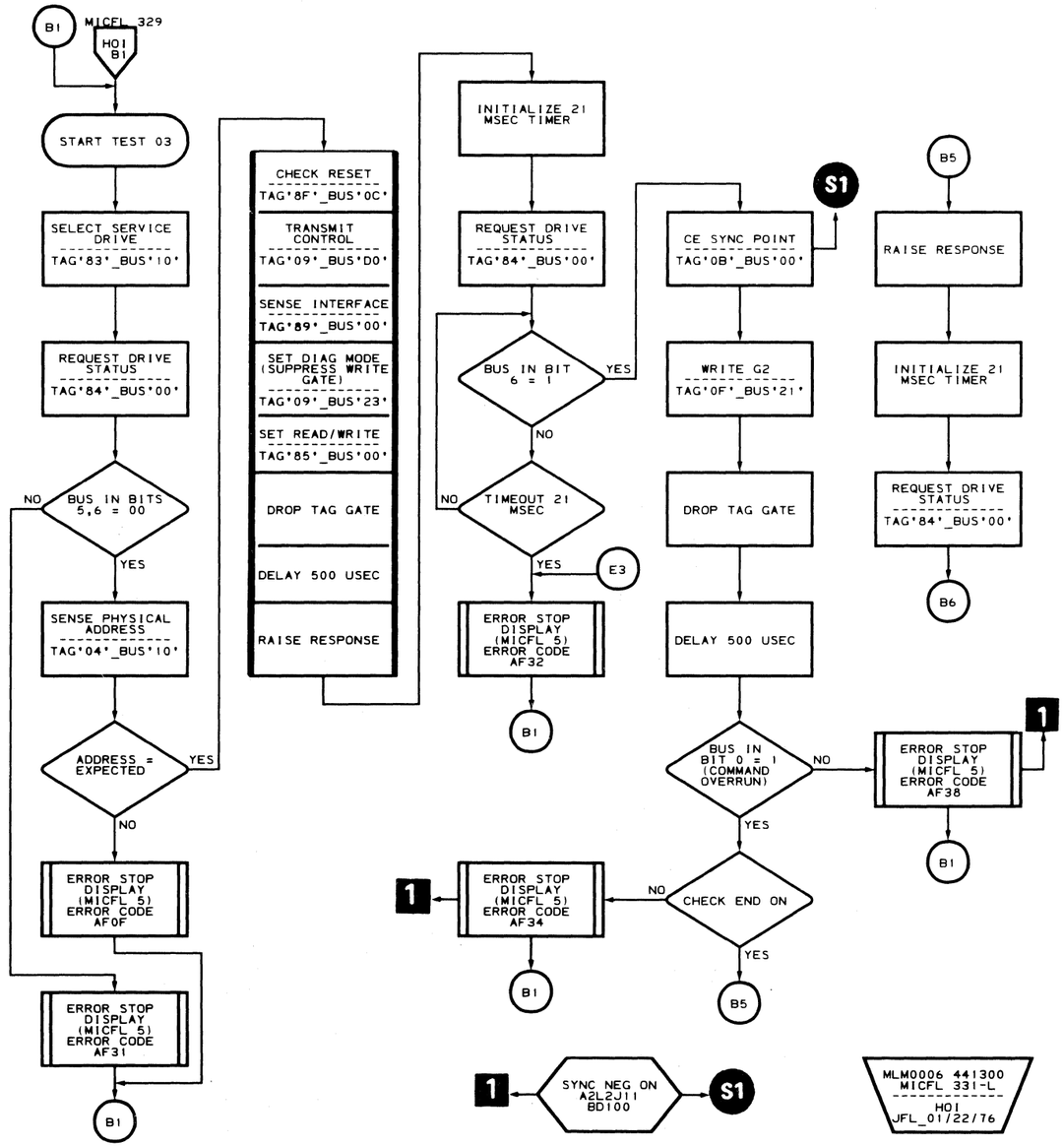
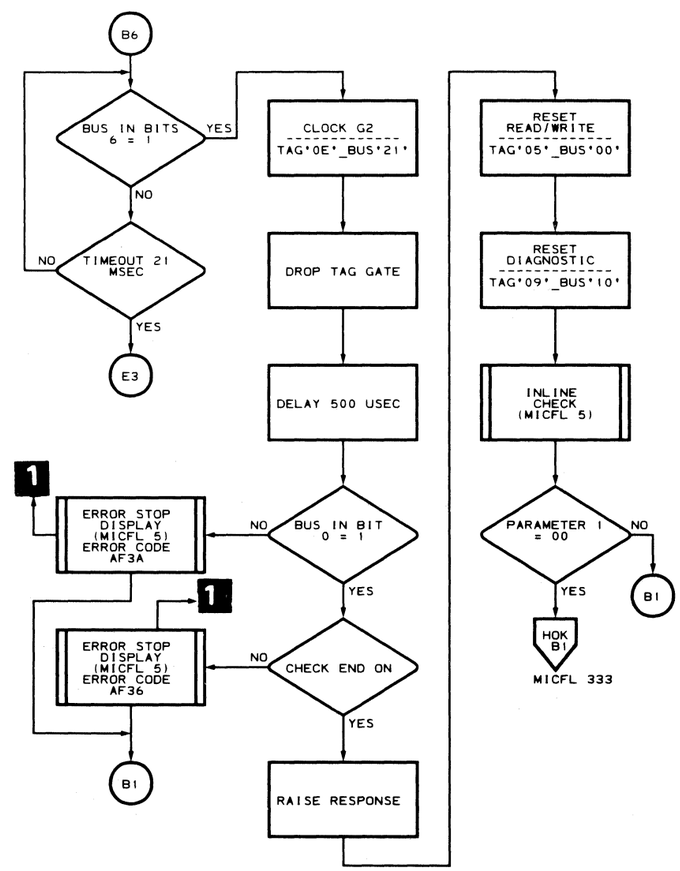
ROUTINE AF – FORMAT READ/WRITE TESTS

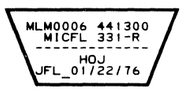


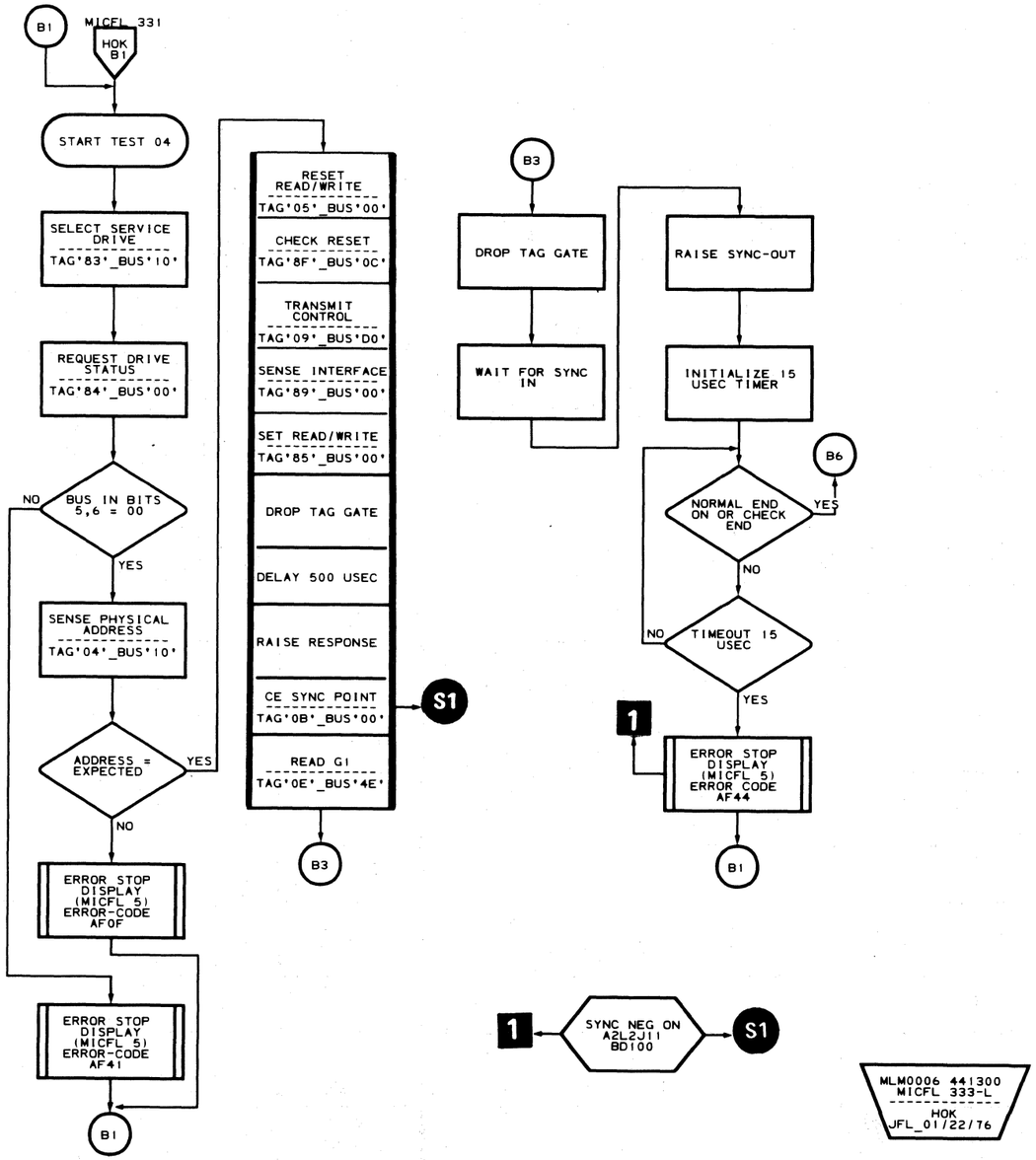


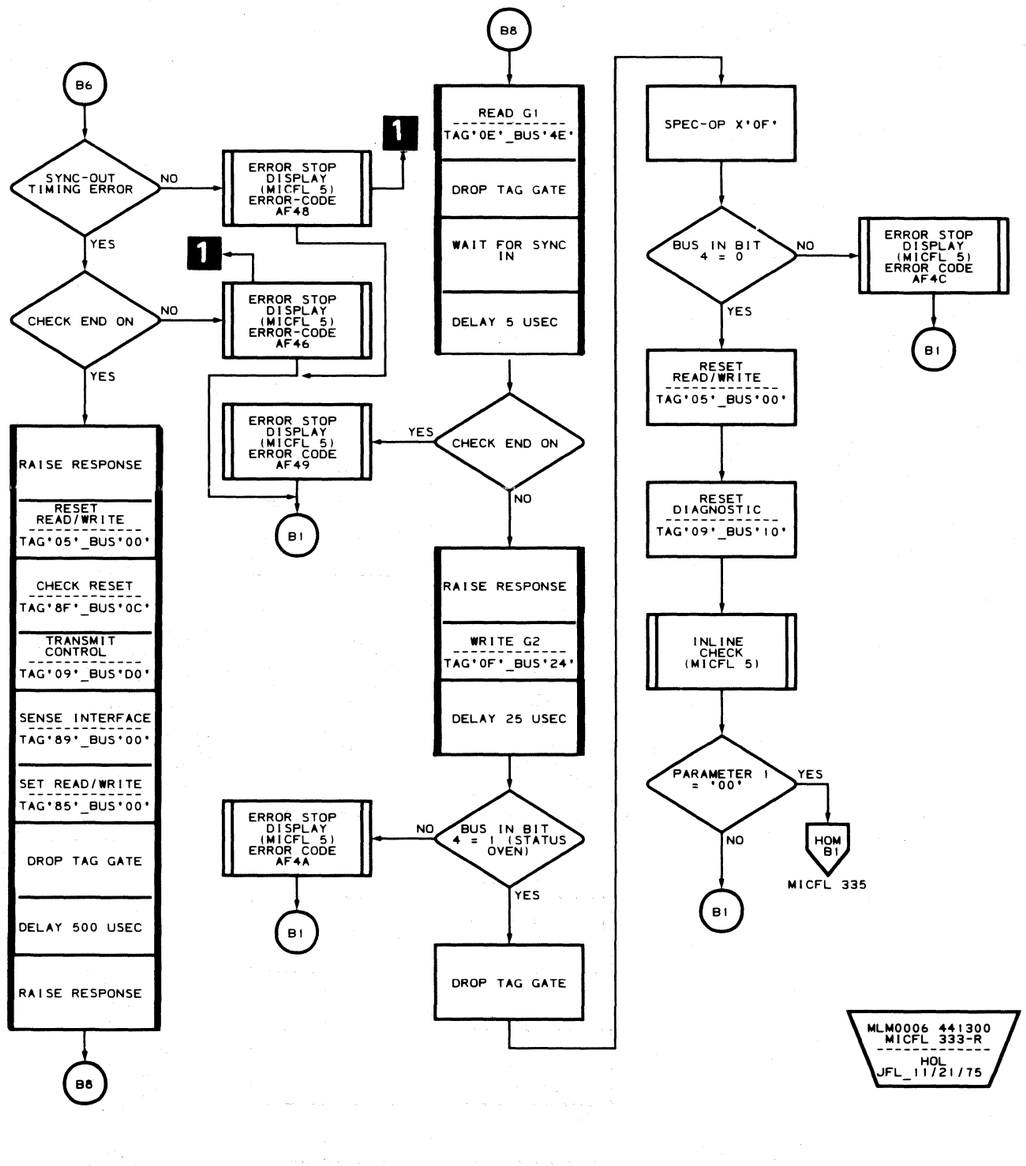
ROUTINE AF – FORMAT READ/WRITE TESTS



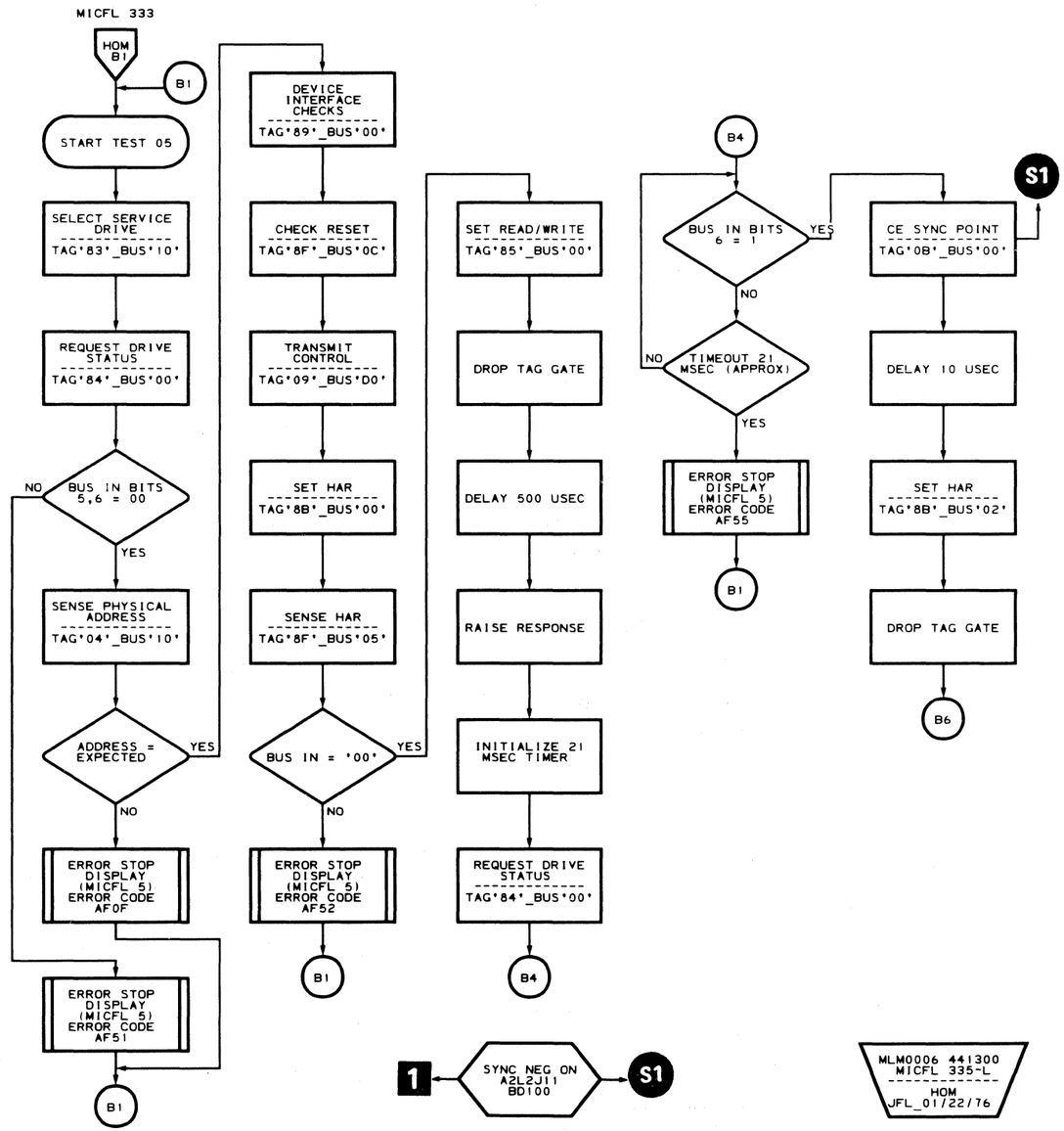


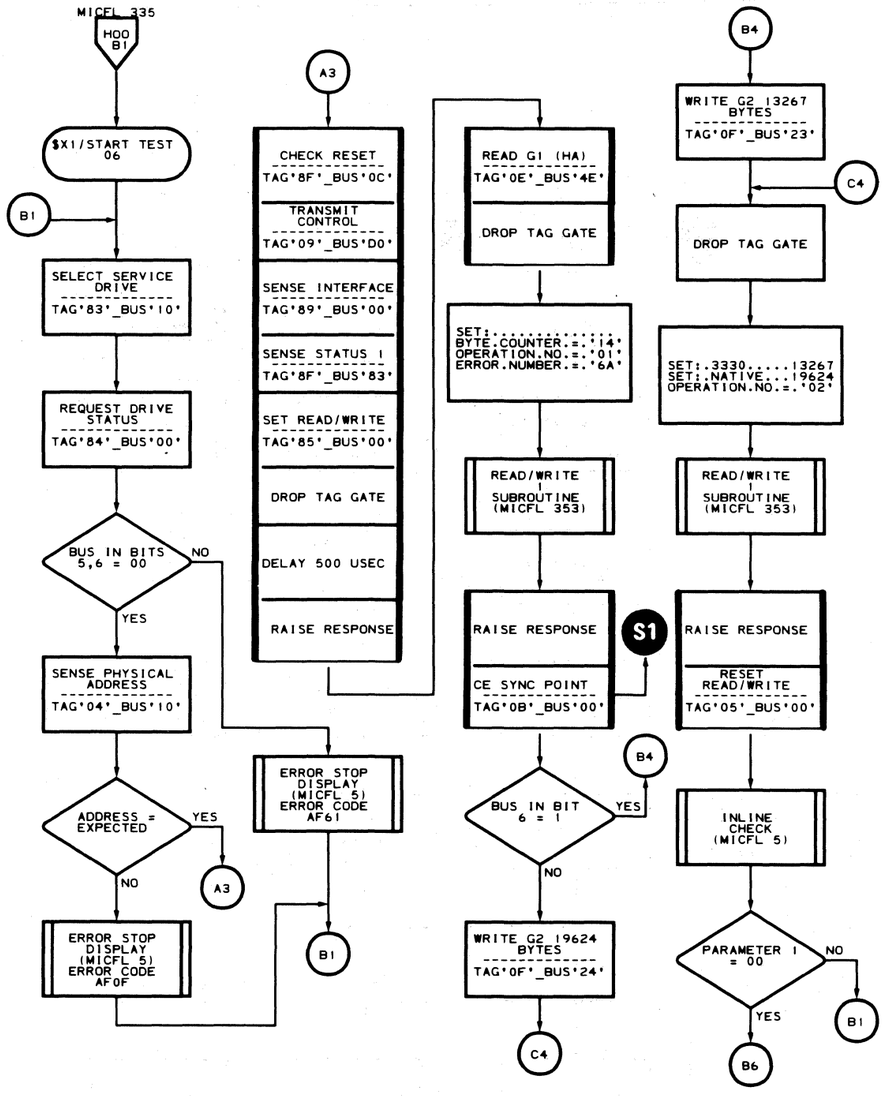






ROUTINE AF – FORMAT READ/WRITE TESTS





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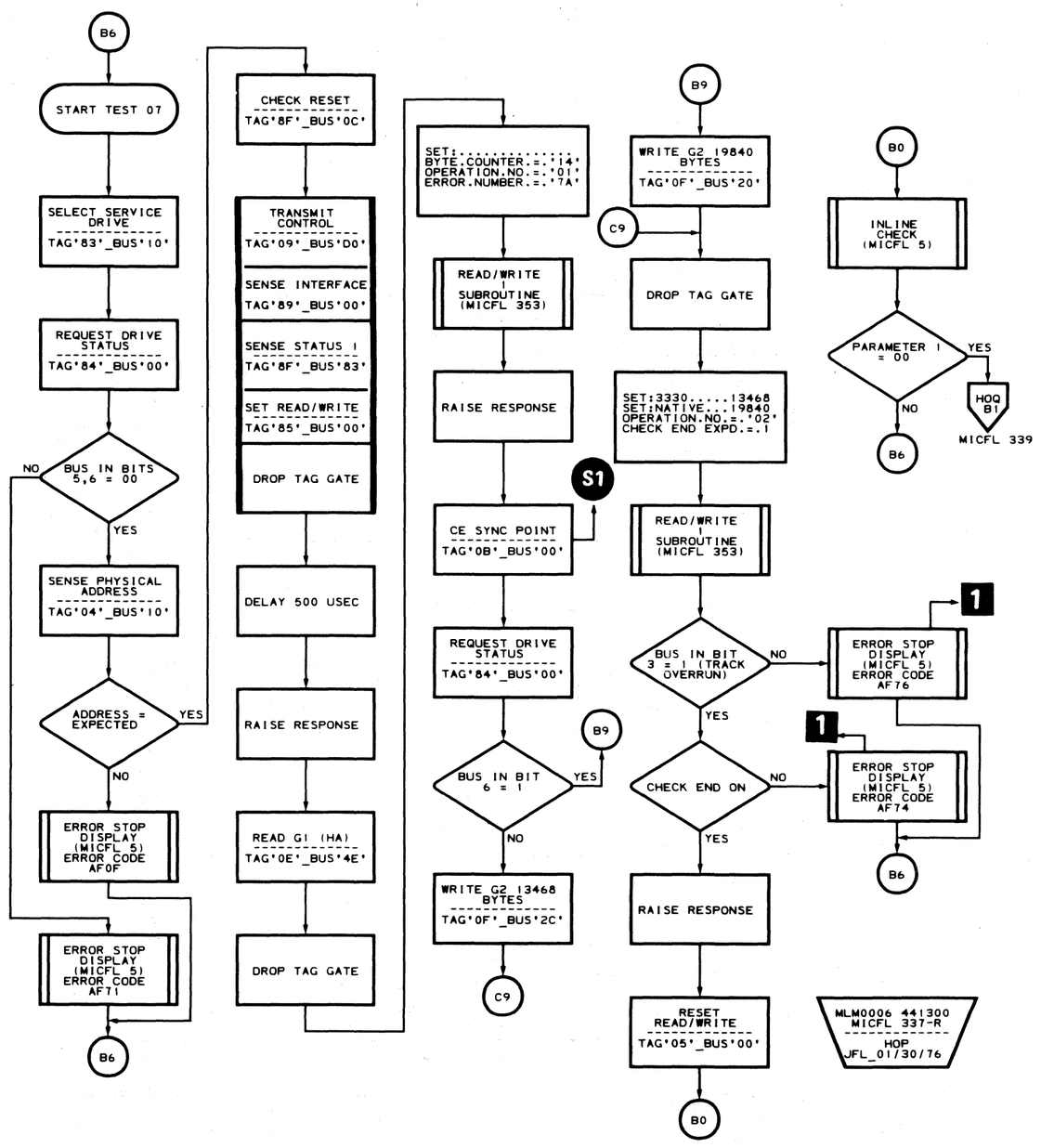

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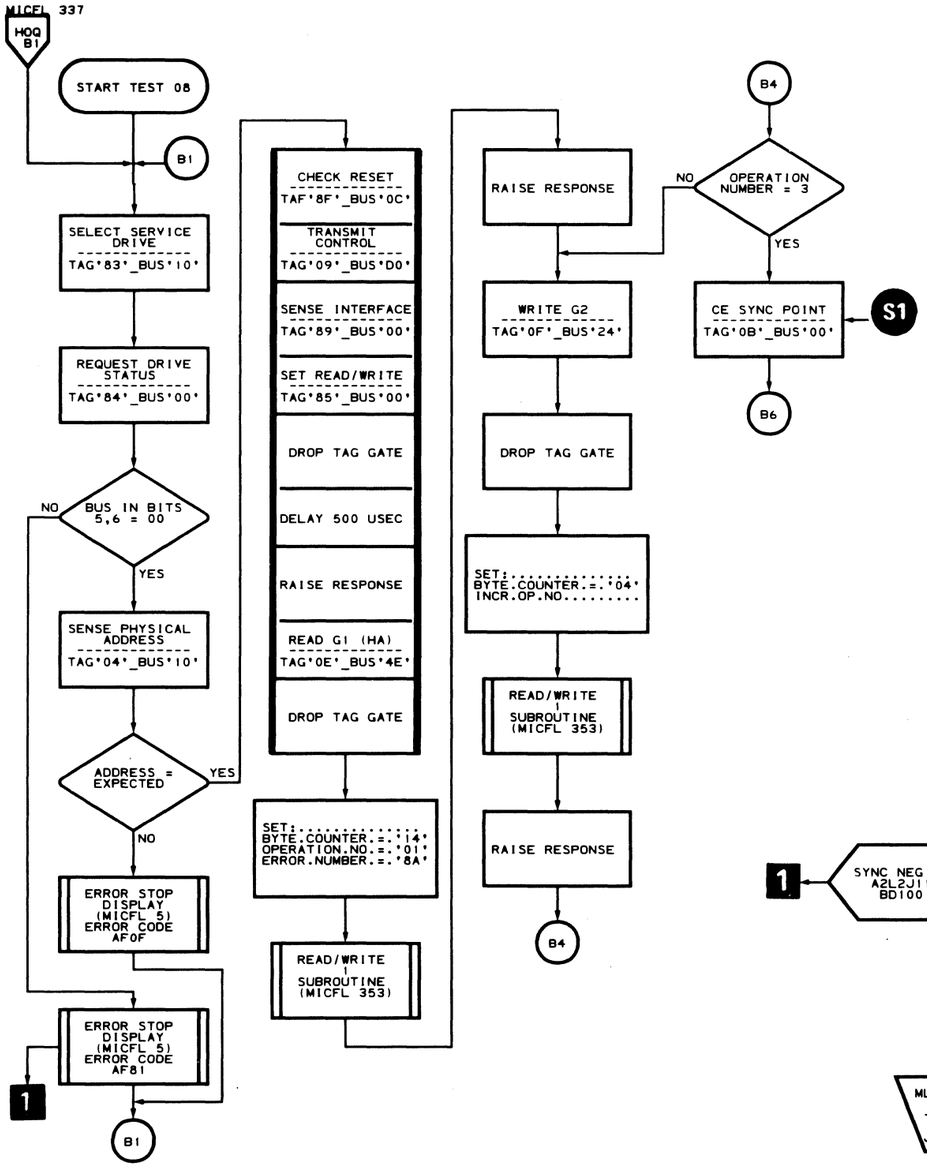
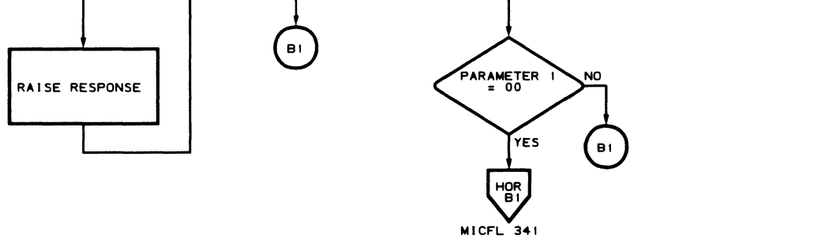
ROUTINE AF – FORMAT READ/WRITE TESTS





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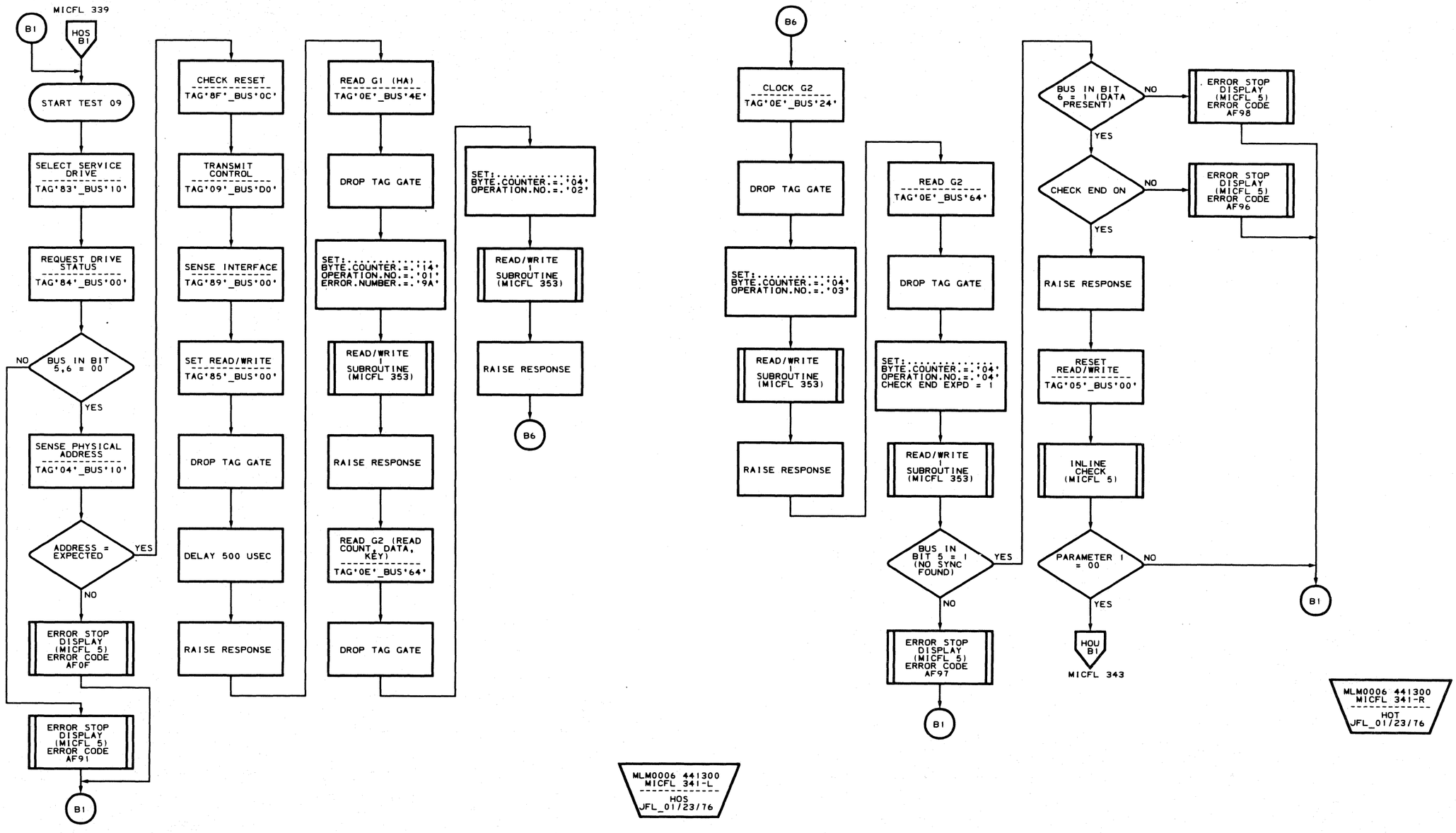
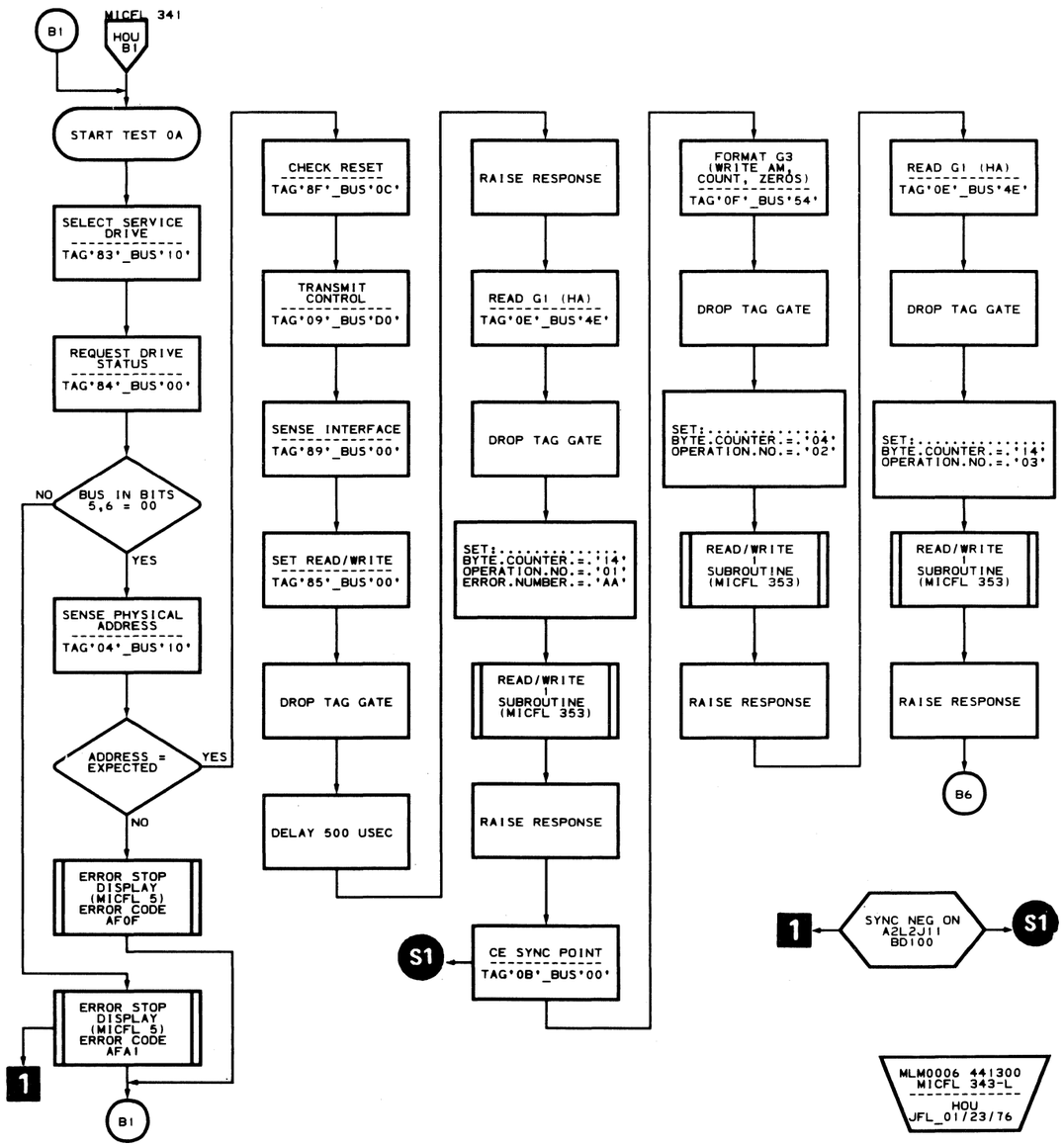
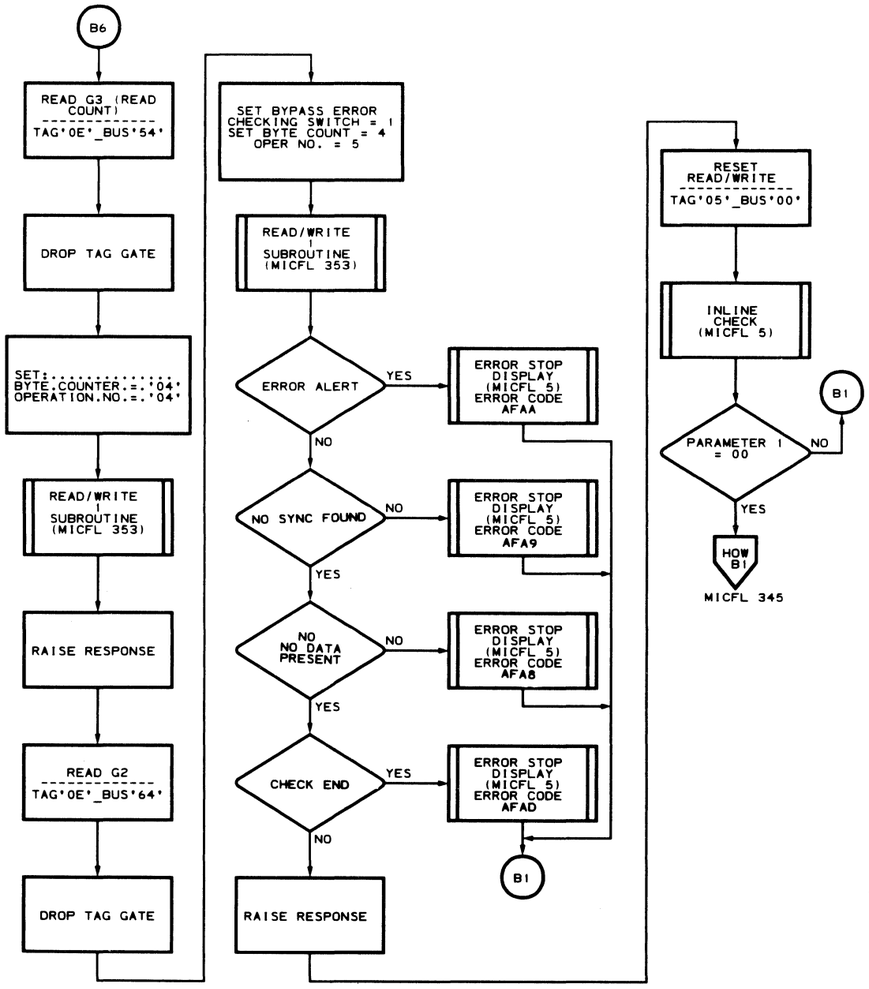
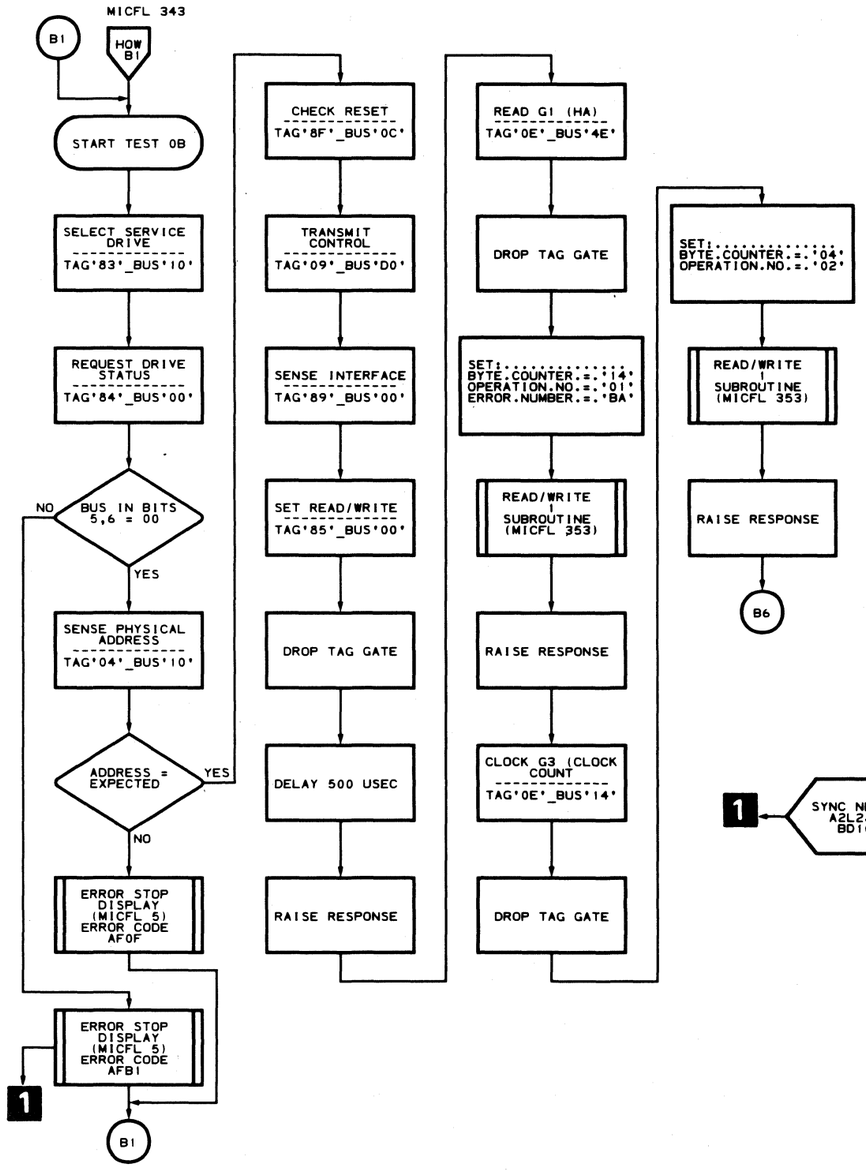


ROUTINE AF – FORMAT READ/WRITE TESTS







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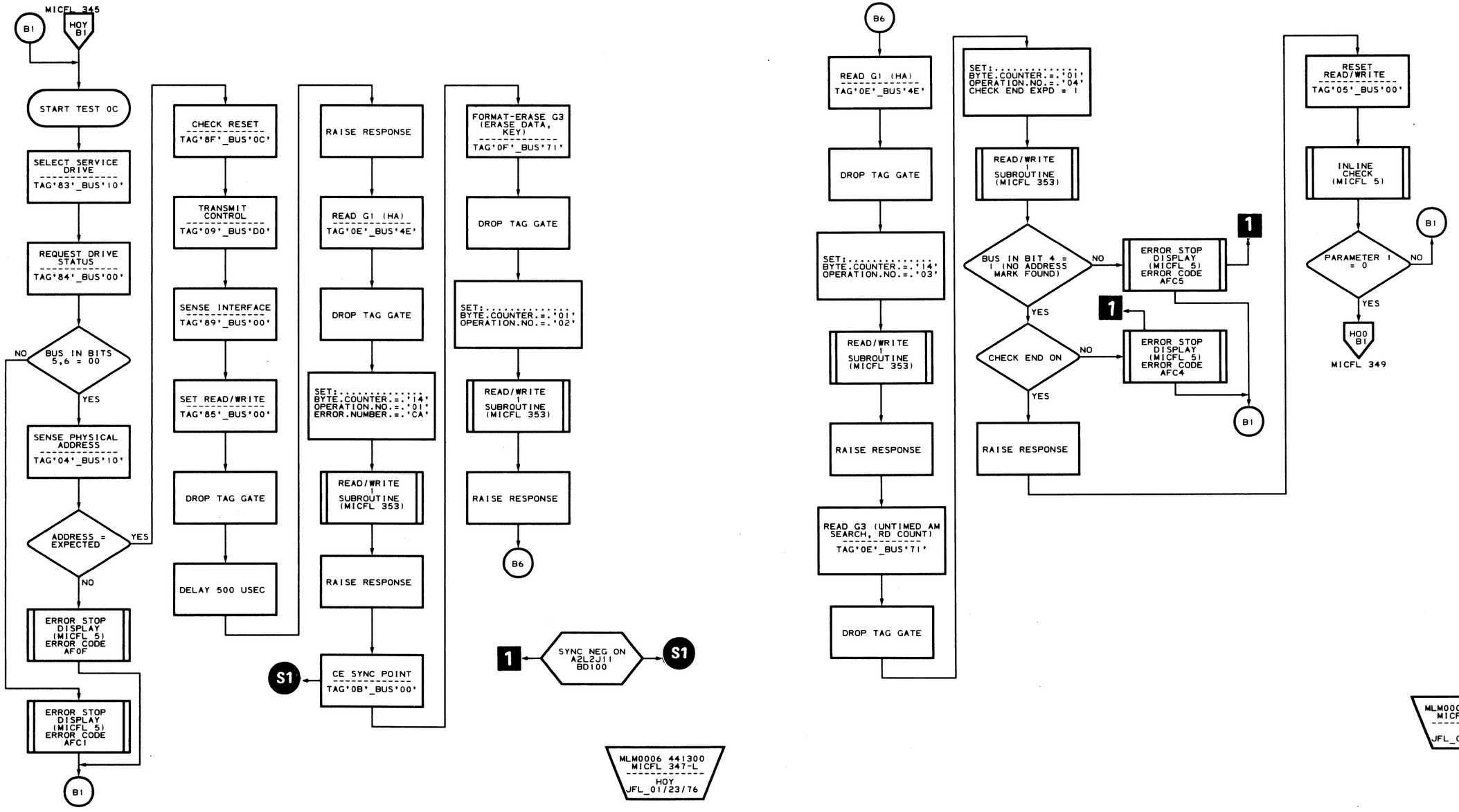
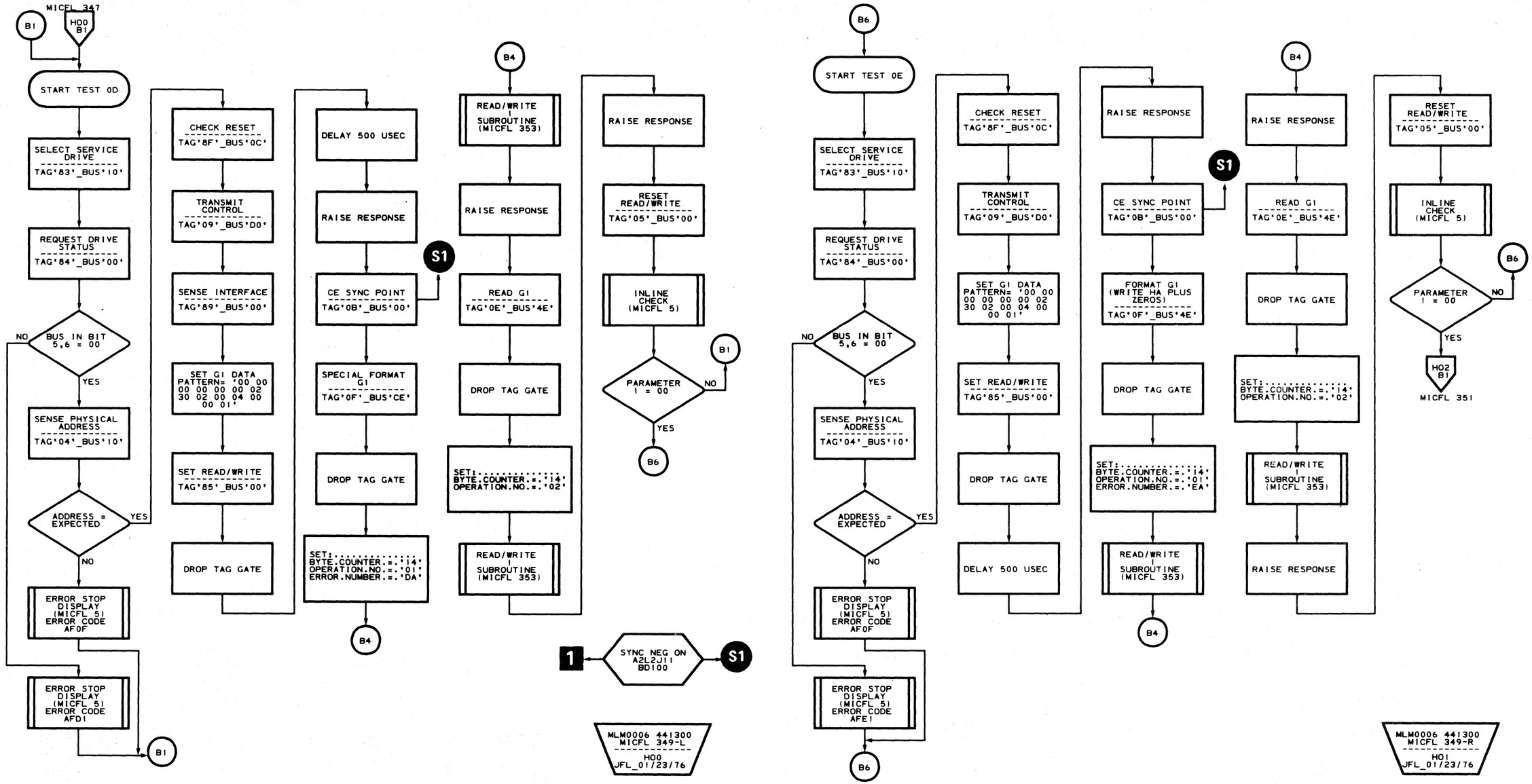
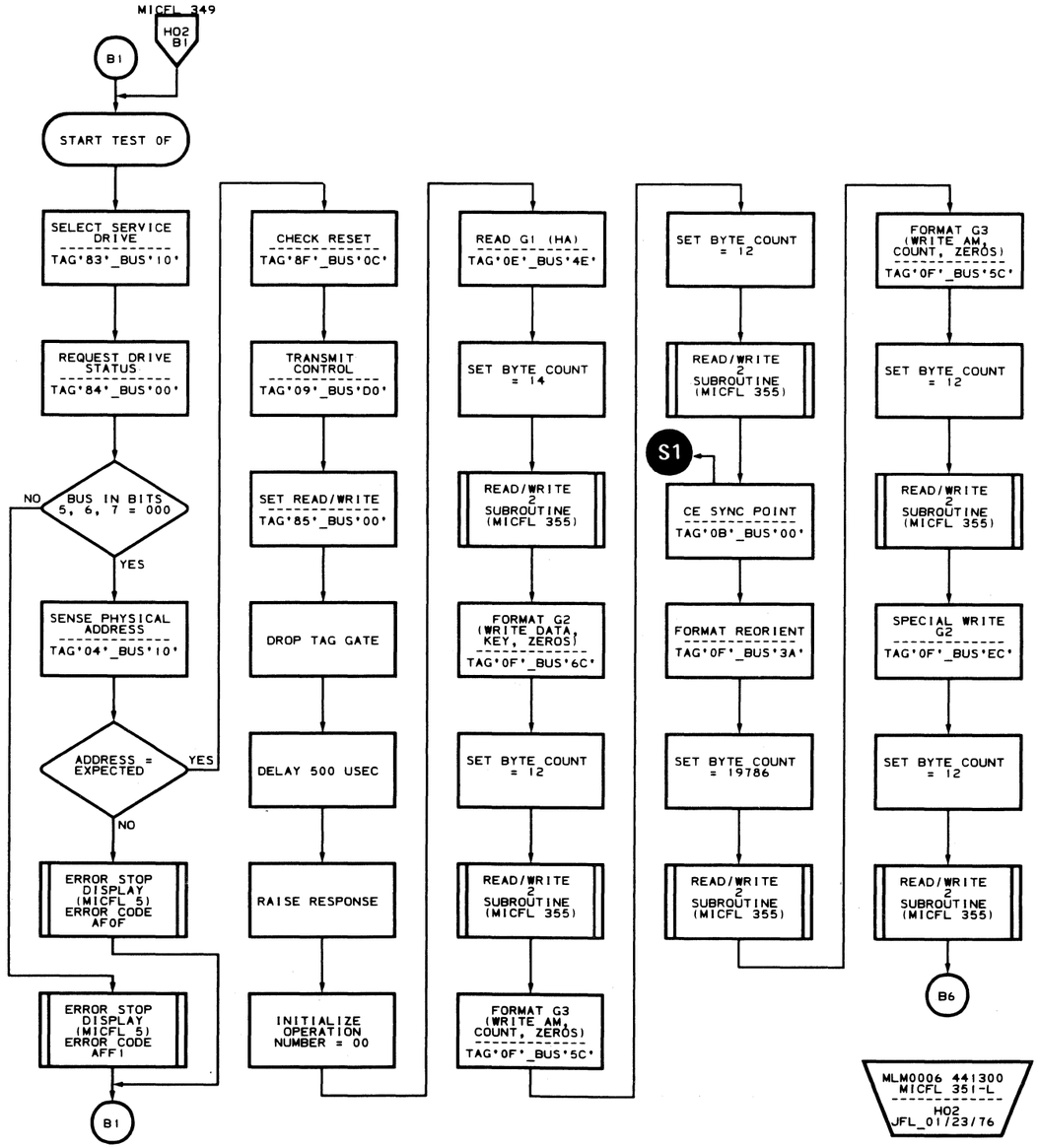
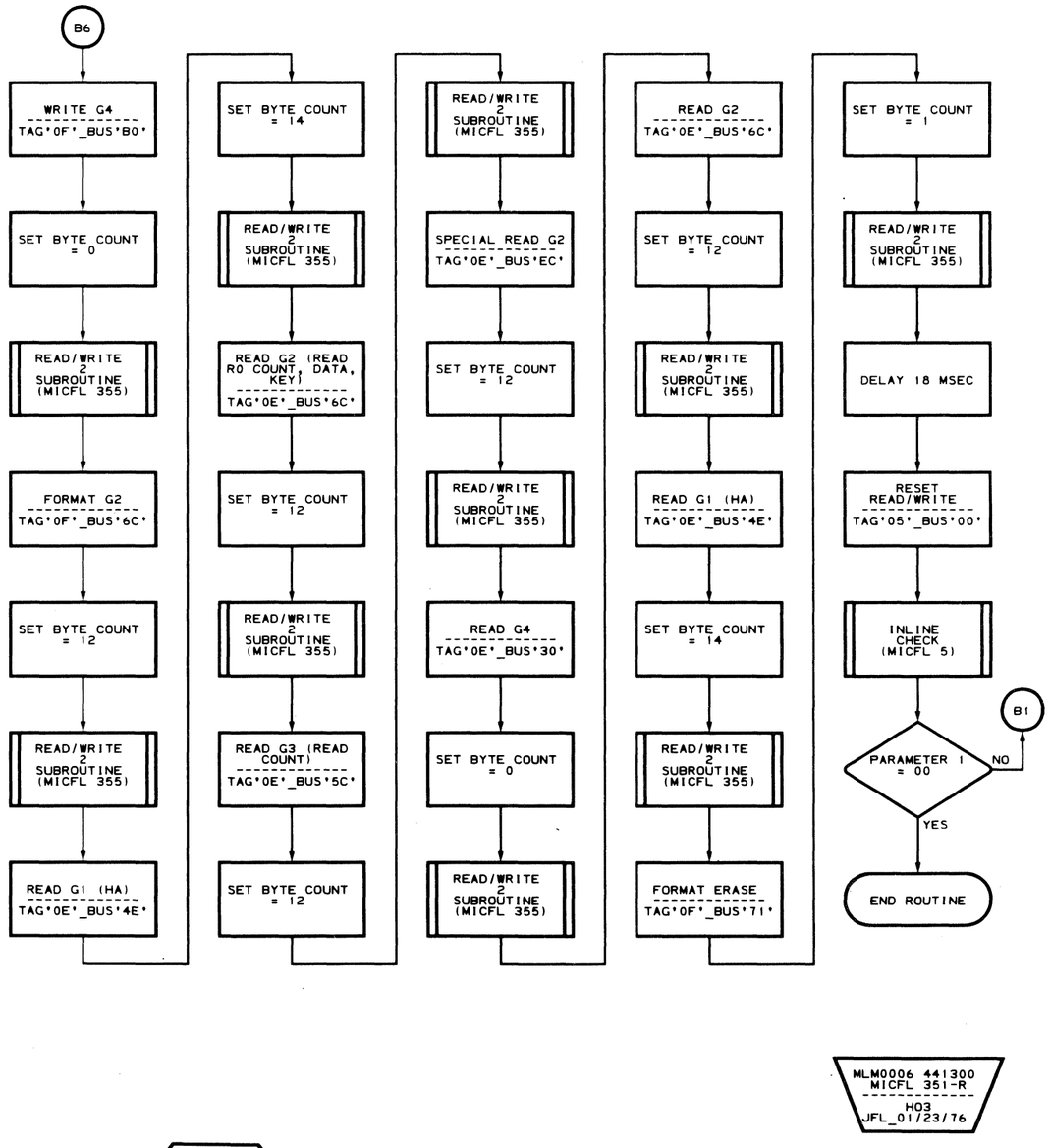
ROUTINE AF – FORMAT READ/WRITE TESTS



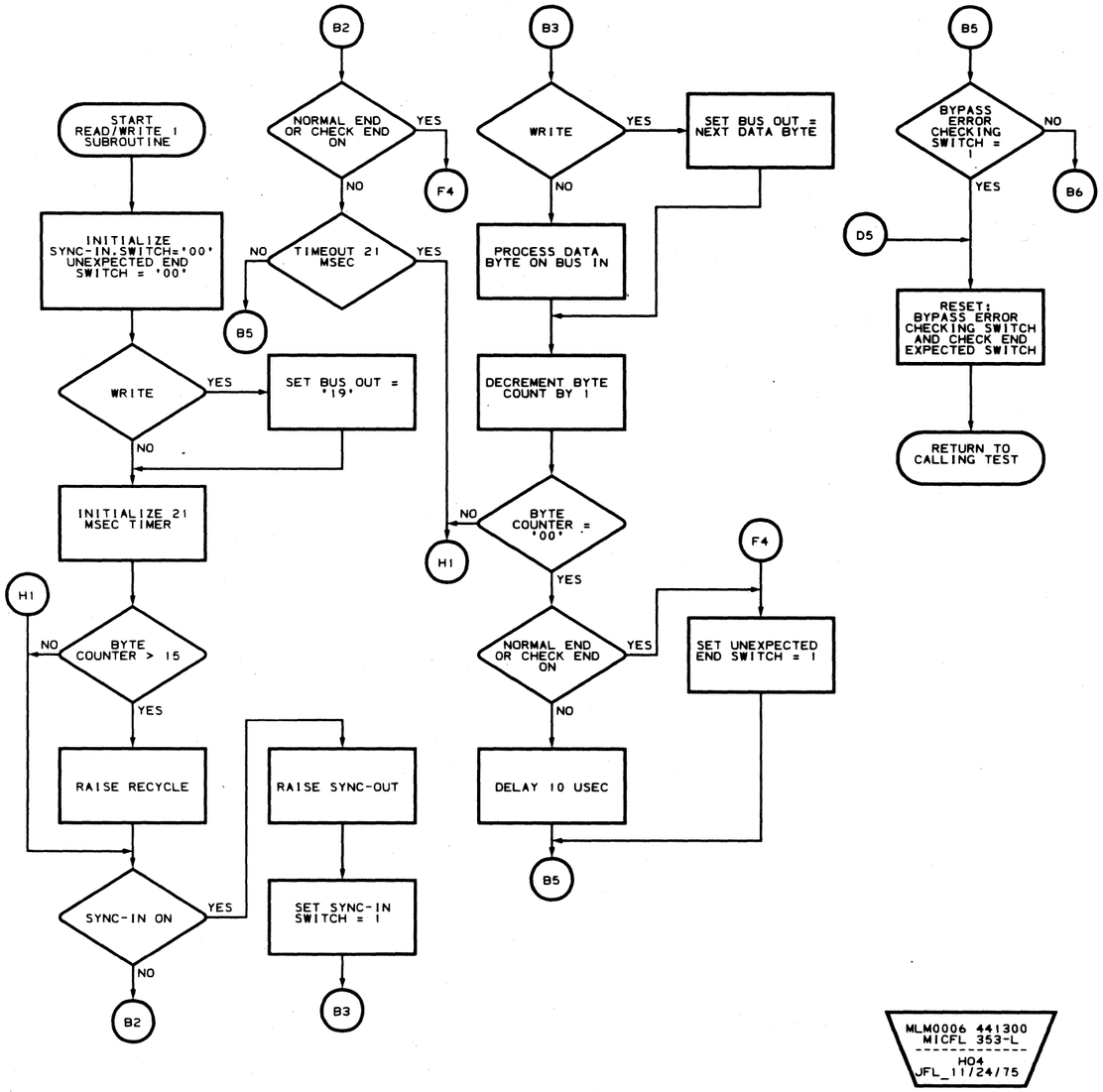


ROUTINE AF – FORMAT READ/WRITE TESTS





ROUTINE AF – FORMAT READ/WRITE TESTS MICFL 353



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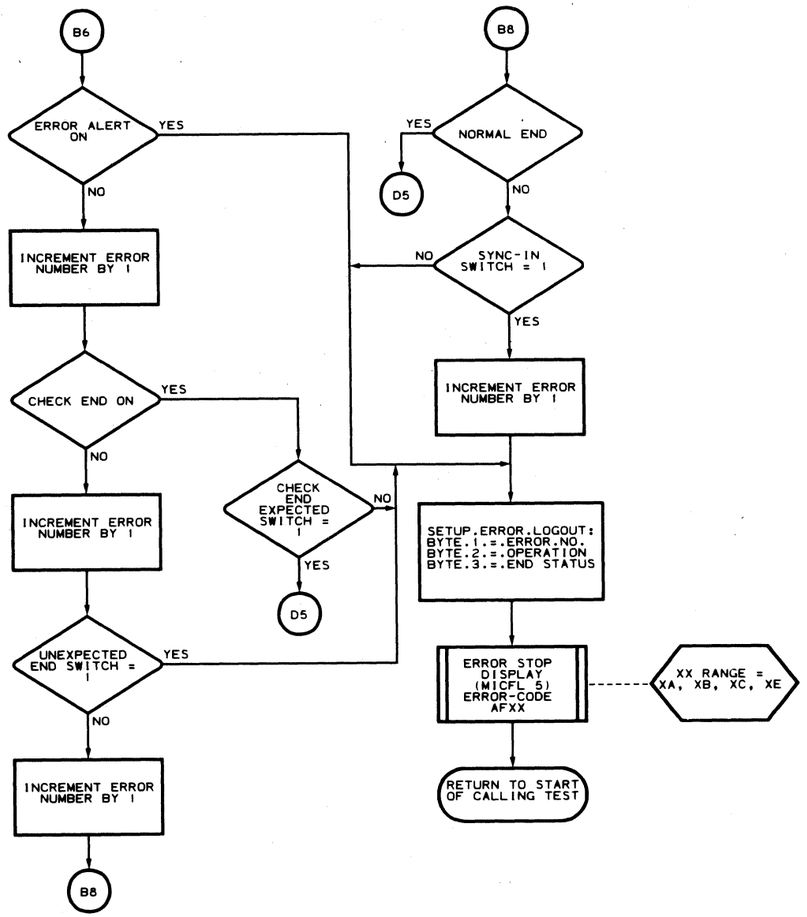

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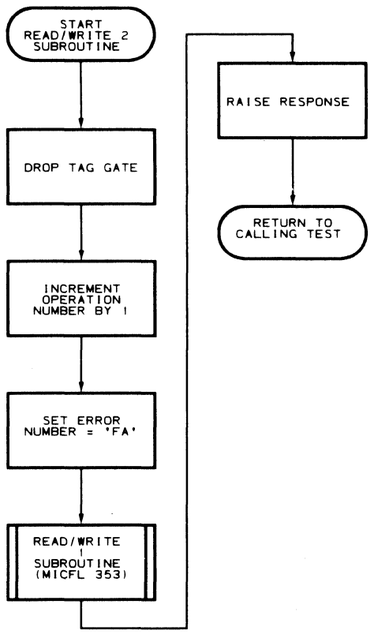
ROUTINE AF – FORMAT READ/WRITE TESTS



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ROUTINES B0,B1, and B2 – 3350 FORMAT READ/WRITE UTILITIES

DESCRIPTION

Introduction

Routine B0 is a utility microprogram designed to format one track or all tracks on the CE cylinder.

The formatting steps are as follows:

1. Verify access position
2. Write Home Address (G1)
3. Write R0 Count (G2)
4. Write R0 Data (G2)
5. Write R1 Count (G3)
6. Write R1 Data (G2) [See Figure 1.]
7. Read Home Address (G1)
8. Read R0 Count (G2)
9. Read R0 Data (G2)
10. Read R1 Count (G3)
11. Read R1 Data (G2)
12. Steps 2 through 11 are repeated for each CE track if the entire CE Cylinder is being formatted.
13. All fields on all tracks on the CE Cylinder are read, even if only one track is being formatted.

The data patterns consist of:

1. Standard Home Address (14 Bytes)
2. Standard R0 Count field (18 Bytes)
3. An R0 Data field of zeros (8 Bytes)
4. Standard R1 Count field (18 Bytes)
5. An R1 Data field-see Figure 1 (256 Bytes)

Options

Routine B0 does not run in default mode. Parameters must be entered. The two run options are

Format entire CE Cylinder and
Format single CE Track.

Operating Instructions

Refer to the flowchart on MICRO 54 for the running instruction logic of routine B0.

Introduction

Routine B1 can read data from any cylinder and/or head on the selected CE drive (including fixed heads). Correct operation is verified by not receiving any of the following:

- Equipment Check
- No Data Found
- No Sync Byte Found
- ECC Data Check

Correct operation is further verified by receiving the correct physical address (PA bytes in the Home Address and Count fields). No customer data is transferred or stored.

Default Mode

In Default Mode, the routine seeks to cylinder 4 and reads the entire cylinder. If the drive is equipped with fixed heads, the routine also seeks to the fixed-head cylinders and reads all the fixed-head tracks.

All ECC Data Check, No Sync Found, and No Data Found errors are accumulated in a summary log. The summary log may be displayed at the completion of the run. Refer to error messages 'B1FD', 'B1FE', and 'B1FF' in the Error Code Dictionary.

Options

1. *Test Cylinder:* This option is the same as the Default Mode except the cylinder number may be selected.
2. *Test Cylinder/Suppress Summary Logging:* This option is the same Test Cylinder except the routine stops on the first error. The routine can be instructed to continue to the next track address in error by using the '00' option. This option is useful for gathering additional information pertaining to the failures on a particular head.
3. *Test Track:* This option is used for performing Read operations on a specific track and stopping on an error.
4. *Scope Loop:* This option is useful for scoping a single track. All errors are bypassed.

Introduction

Routine B2 is a utility microprogram designed to format one track or all tracks on the CE cylinder.

The formatting steps are as follows:

1. Read Home Address (G1)
2. Verify access position
3. Write R0 Count (G2)
4. Write R0 Data (G2)
5. Write R1 Count (G3)
6. Write R1 Data (G2) [See Figure 1.]
7. Read Home Address (G1)
8. Read R0 Count (G2)
9. Read R0 Data (G2)
10. Read R1 Count (G3)
11. Read R1 Data (G2)
12. Steps 1 through 11 are repeated for each CE track if the entire CE Cylinder is being formatted.
13. All fields on all tracks on the CE Cylinder are read, even if only one track is being formatted.

The data patterns consist of:

1. Standard Home Address (14 Bytes)
2. Standard R0 Count field (18 Bytes)
3. An R0 Data field of zeros (8 Bytes)
4. Standard R1 Count field (18 Bytes)
5. An R1 Data field-see Figure 1 (256 Bytes)

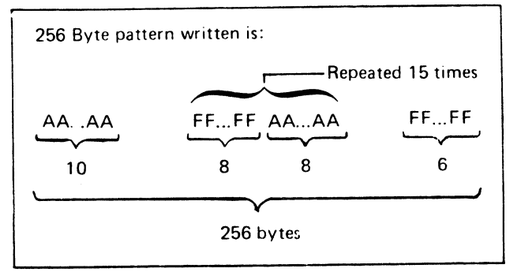
Options

1. *Default Mode.* Each track of the CE cylinder is written and verified, then the entire CE cylinder is read again and checked for errors.
2. *Single Track Mode.* The track selected by the parameter Byte 4 is written and verified. Then the entire CE cylinder is read back and checked for errors.

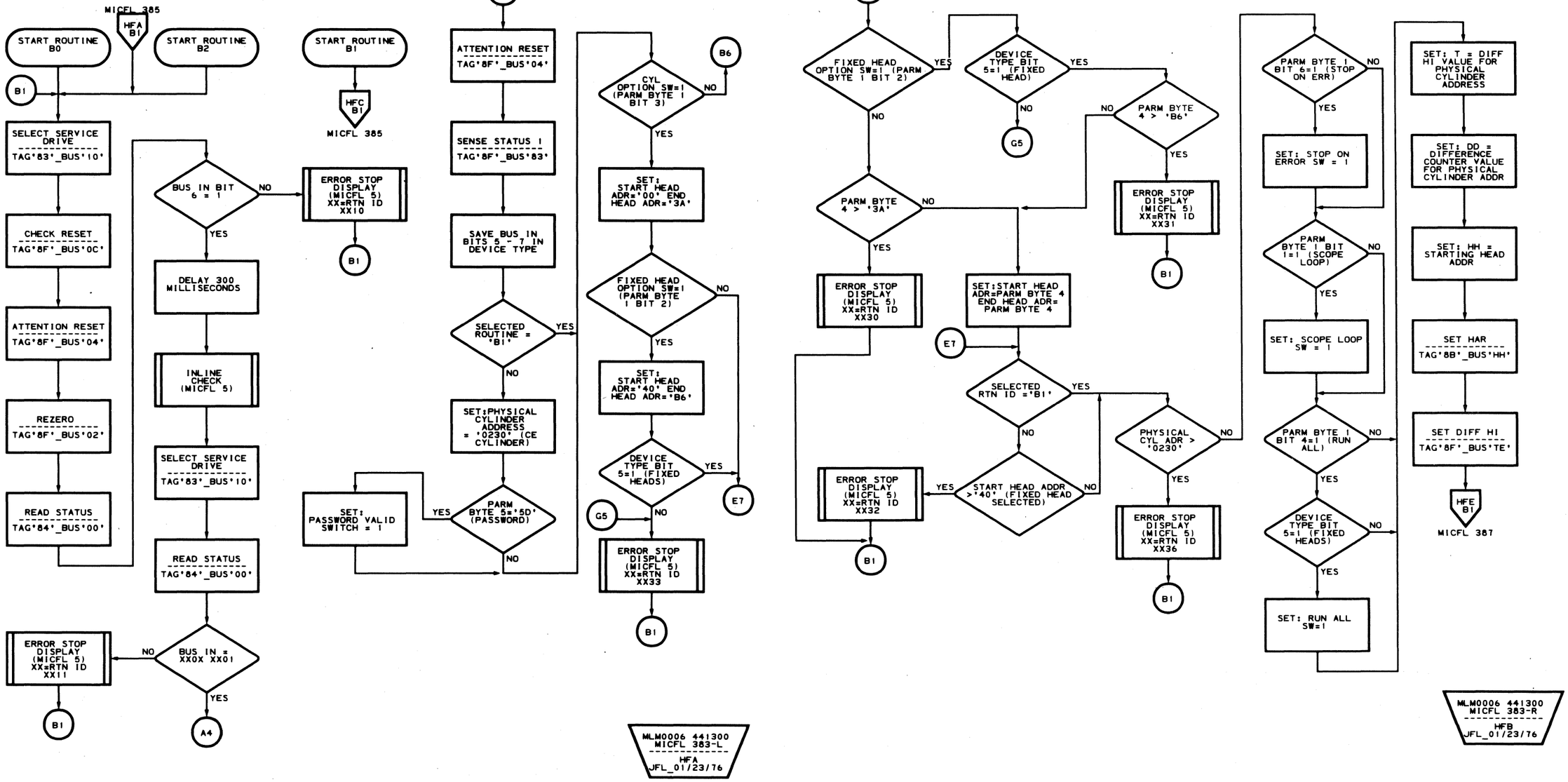
OPERATING PROCEDURE

Refer to detailed running instructions on MICRO 52, 56, and 60 for routines B0, B1 and B2, respectively.

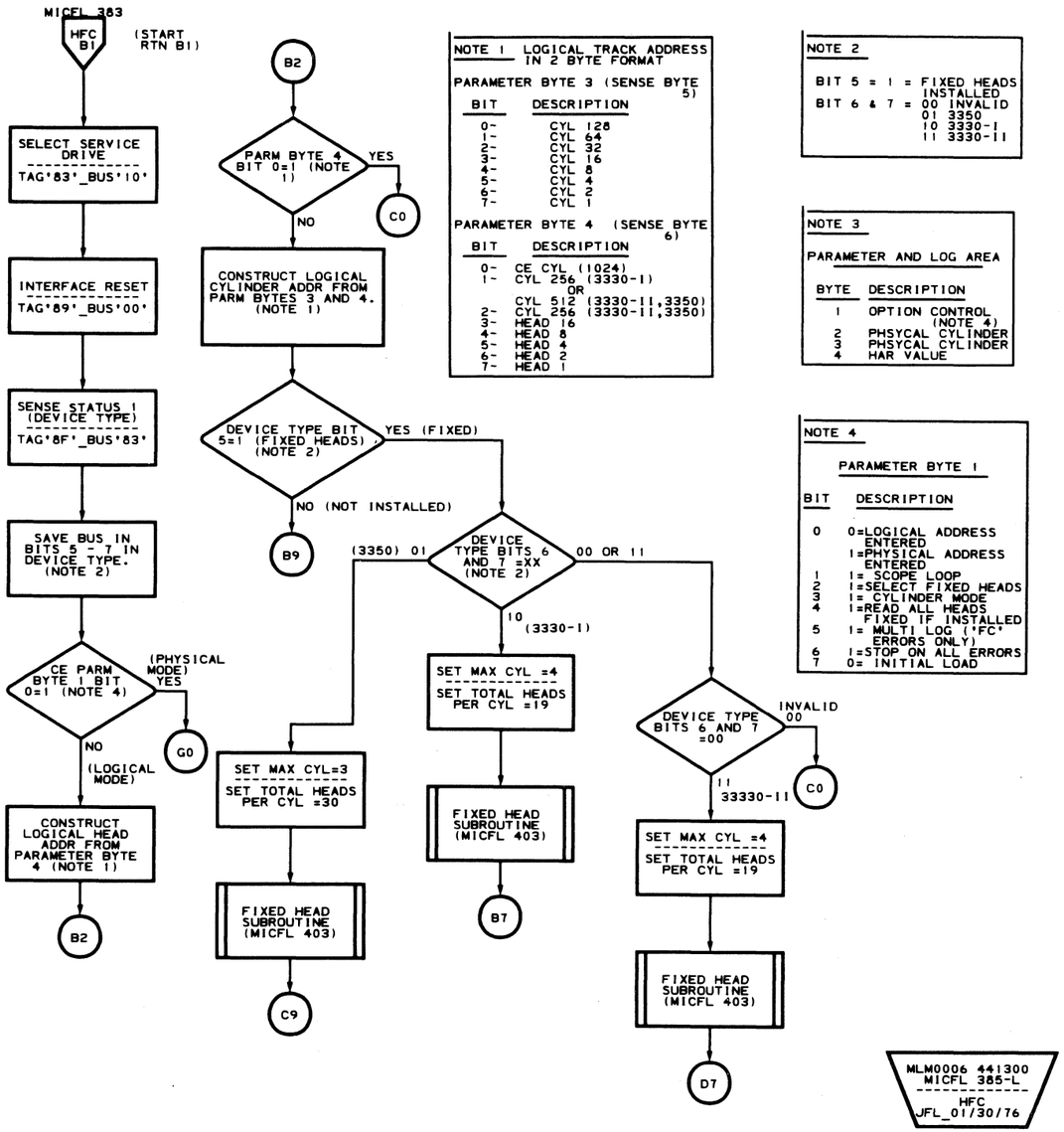
Figure 1. R1 Data Field

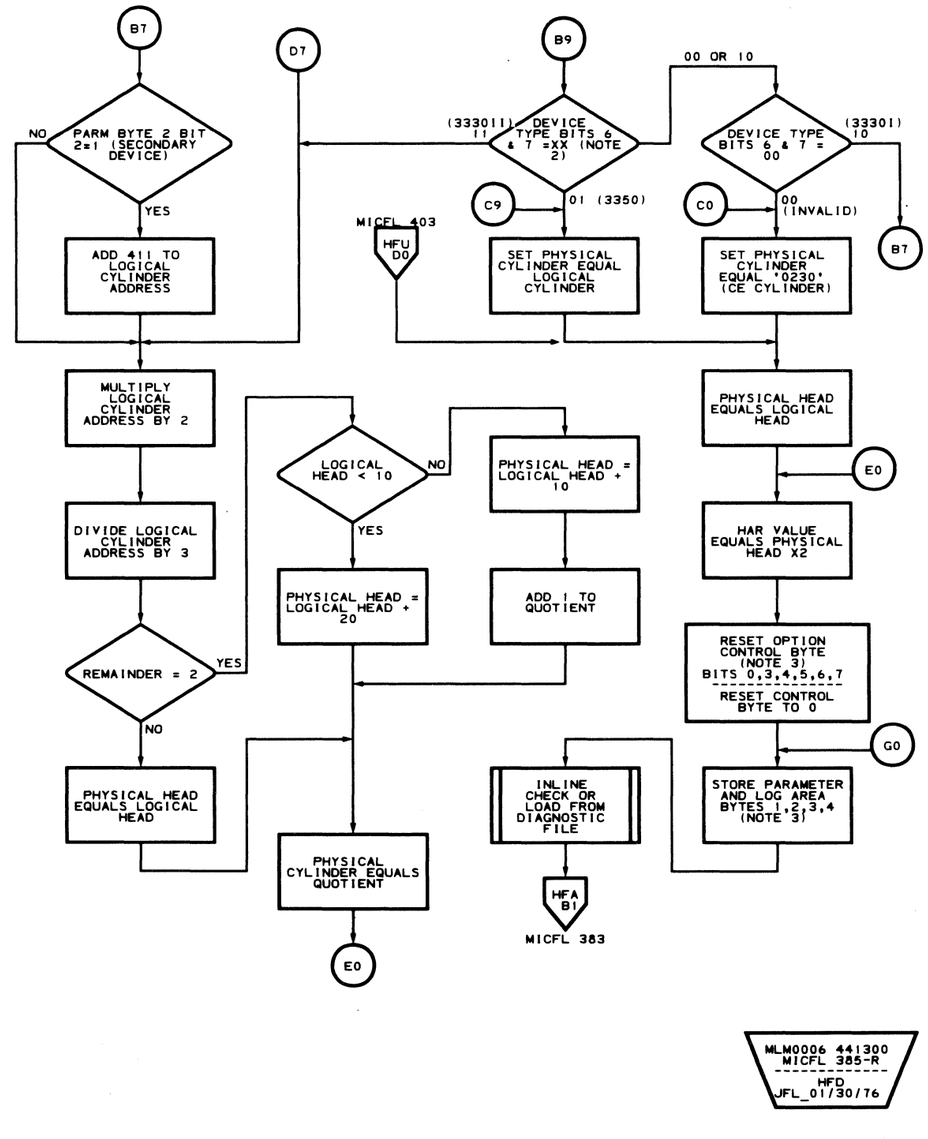


ROUTINES B0, B1, B2 – REFORMAT CE TRACKS UTILITY ROUTINES MICFL 383

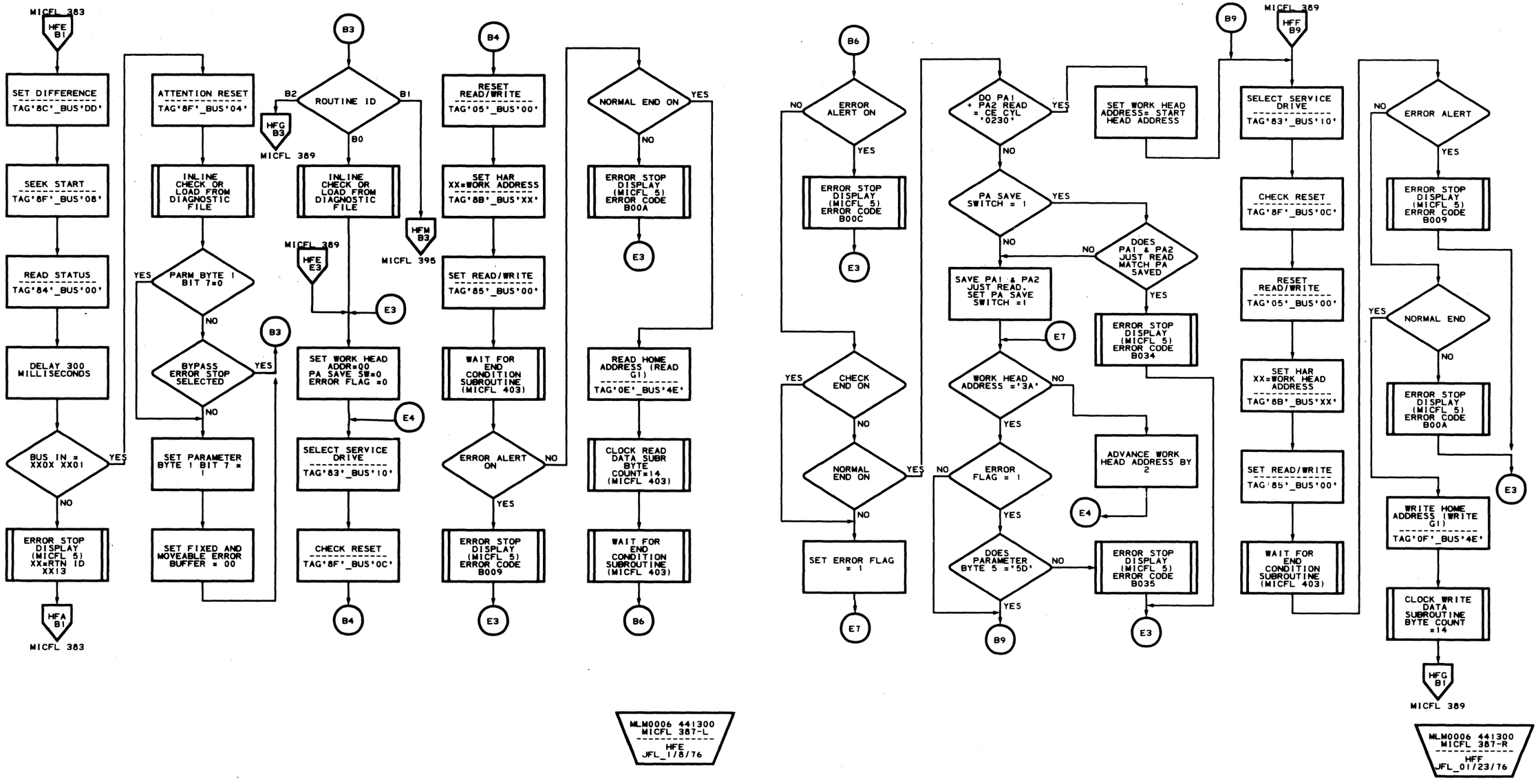


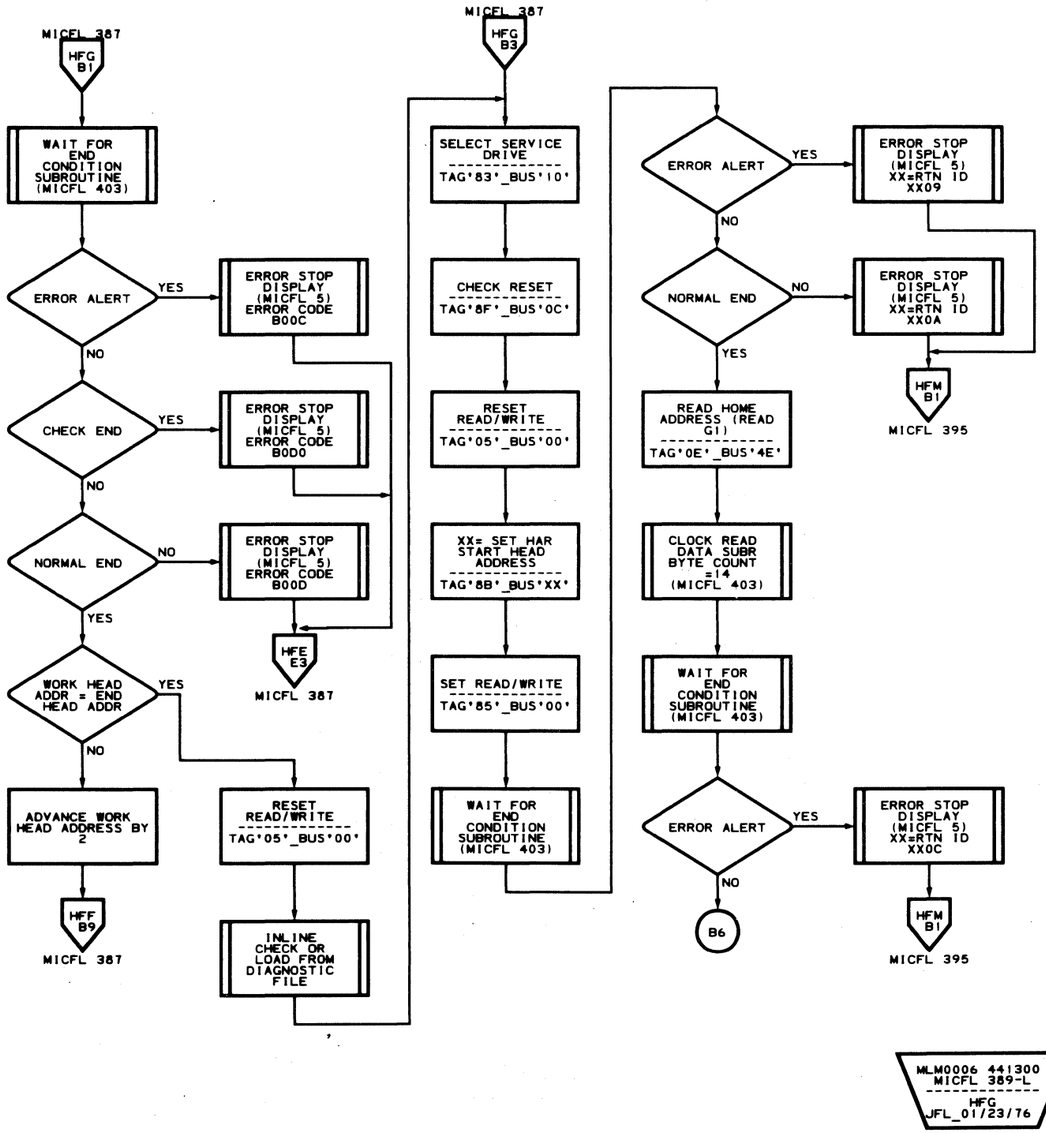
ROUTINES B0, B1, B2 – REFORMAT CE TRACKS UTILITY ROUTINES MICFL 385





ROUTINES B0, B1, B2 – REFORMAT CE TRACKS UTILITY ROUTINES





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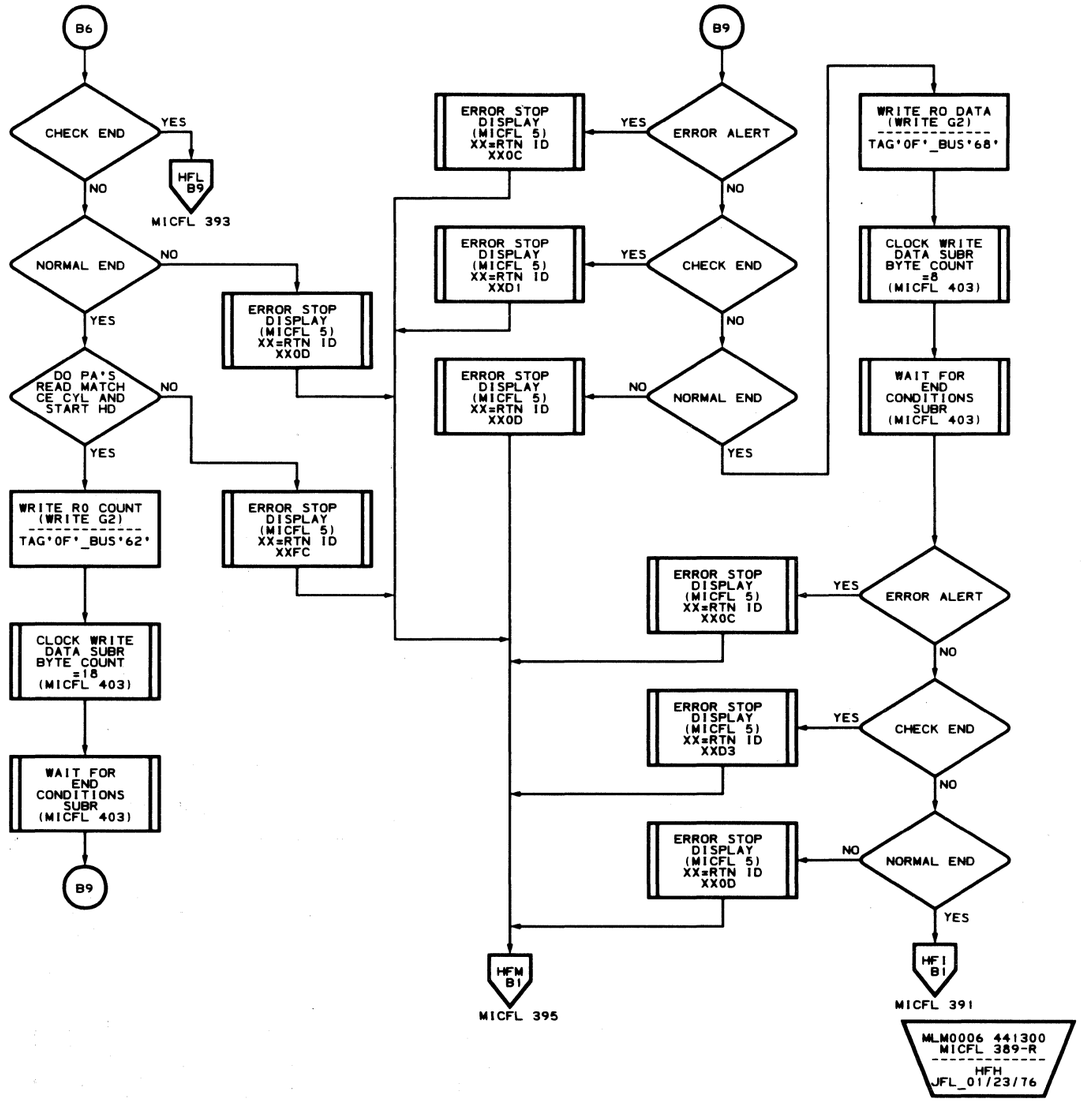
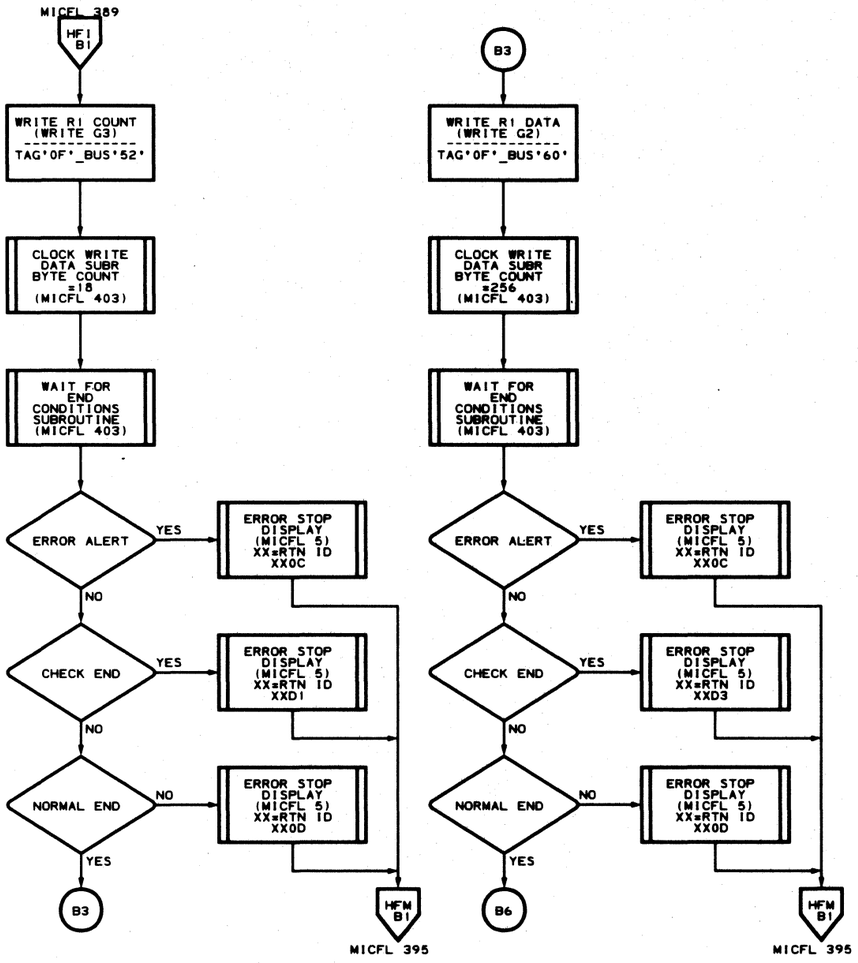
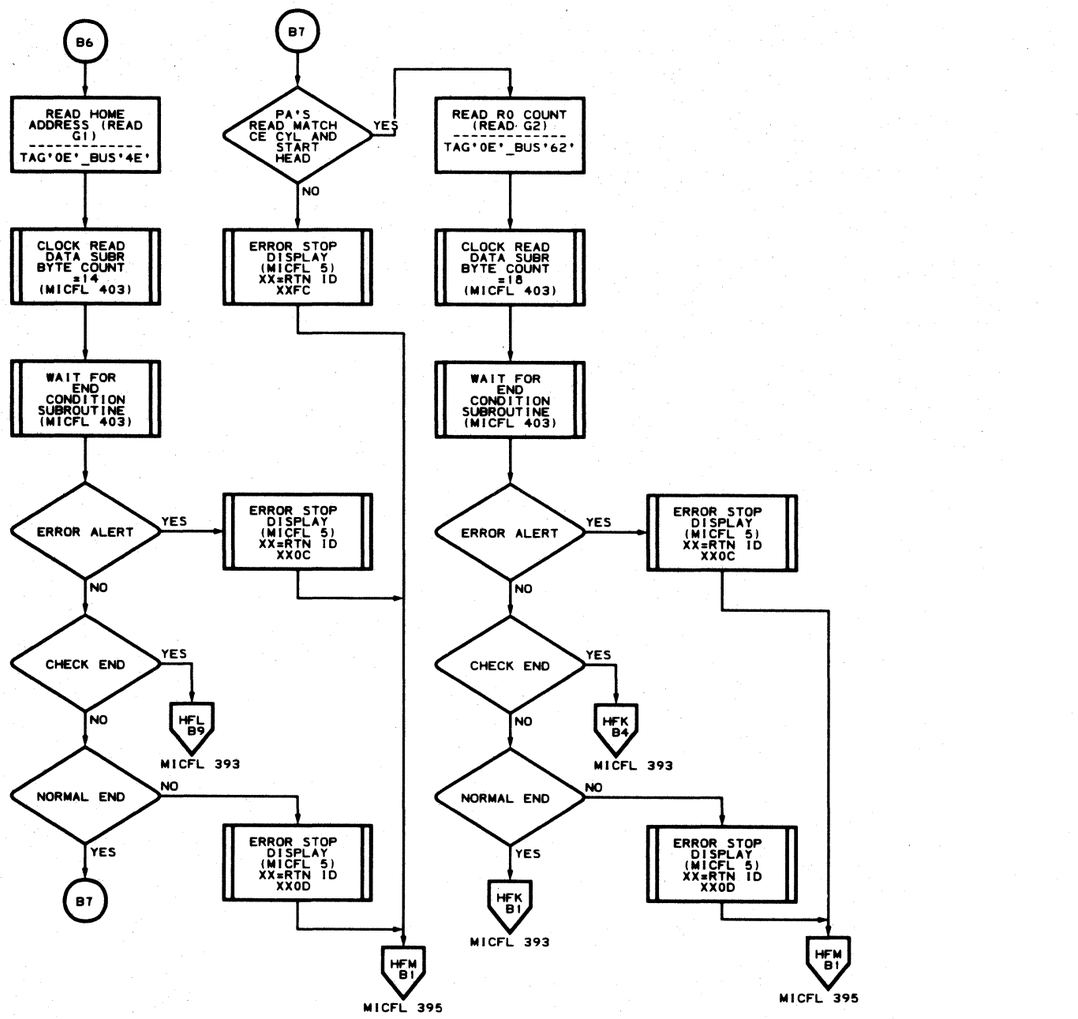


ROUTINES B0, B1, B2 – REFORMAT CE TRACKS UTILITY ROUTINES MICFL 391





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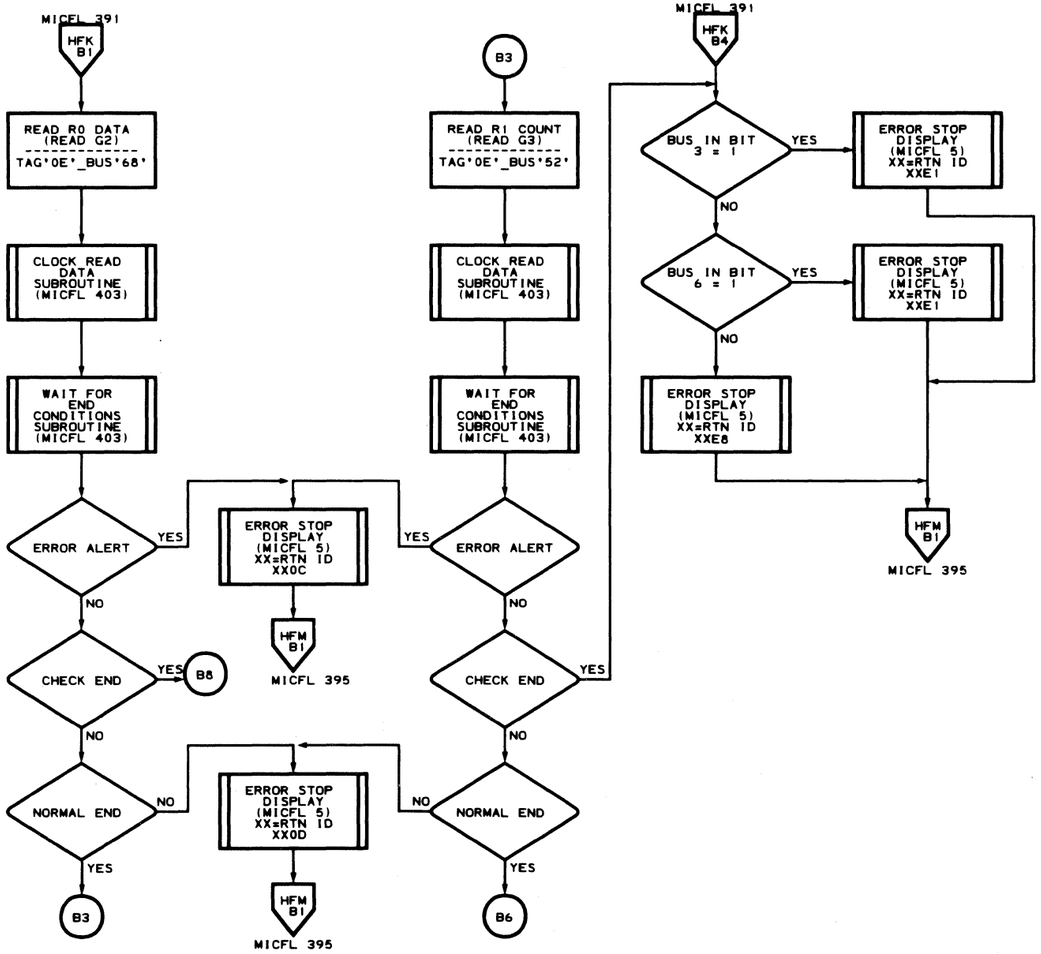
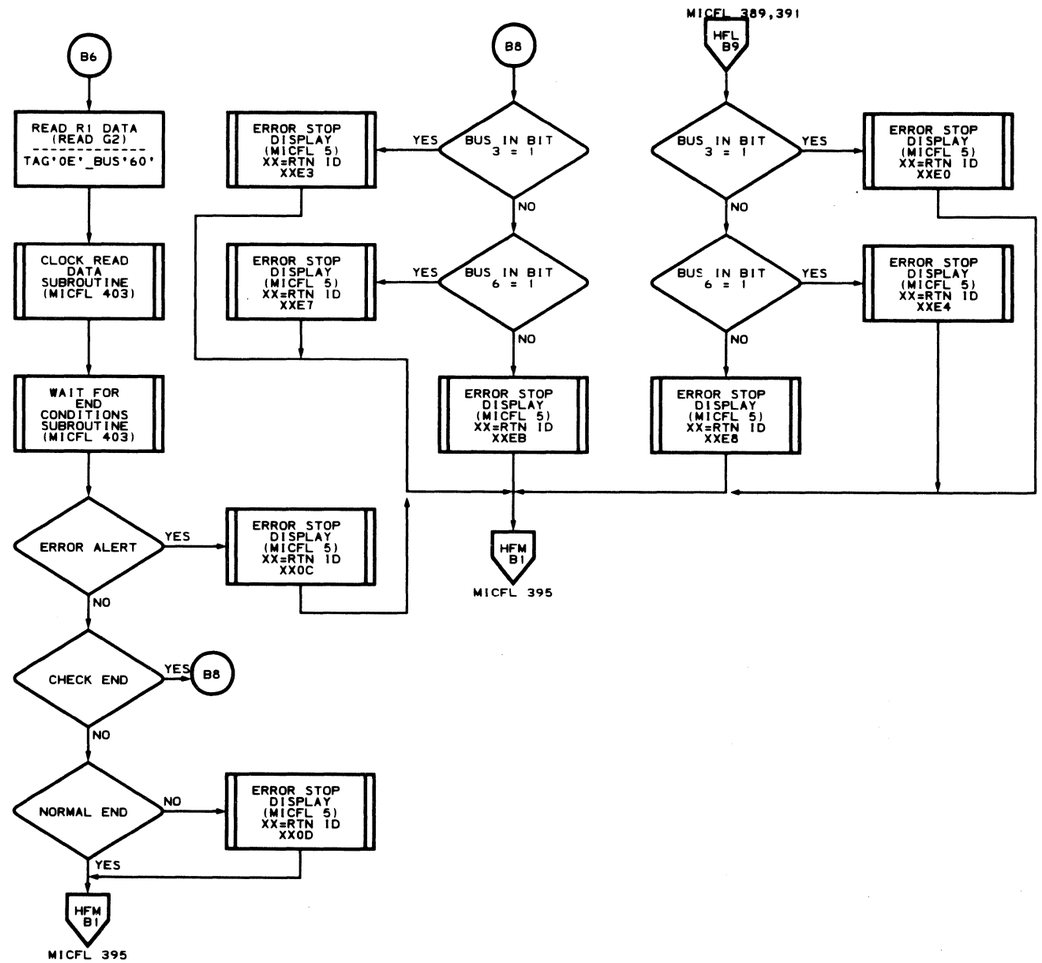
ROUTINES B0, B1, B2 – REFORMAT CE TRACKS UTILITY ROUTINES MICFL 393





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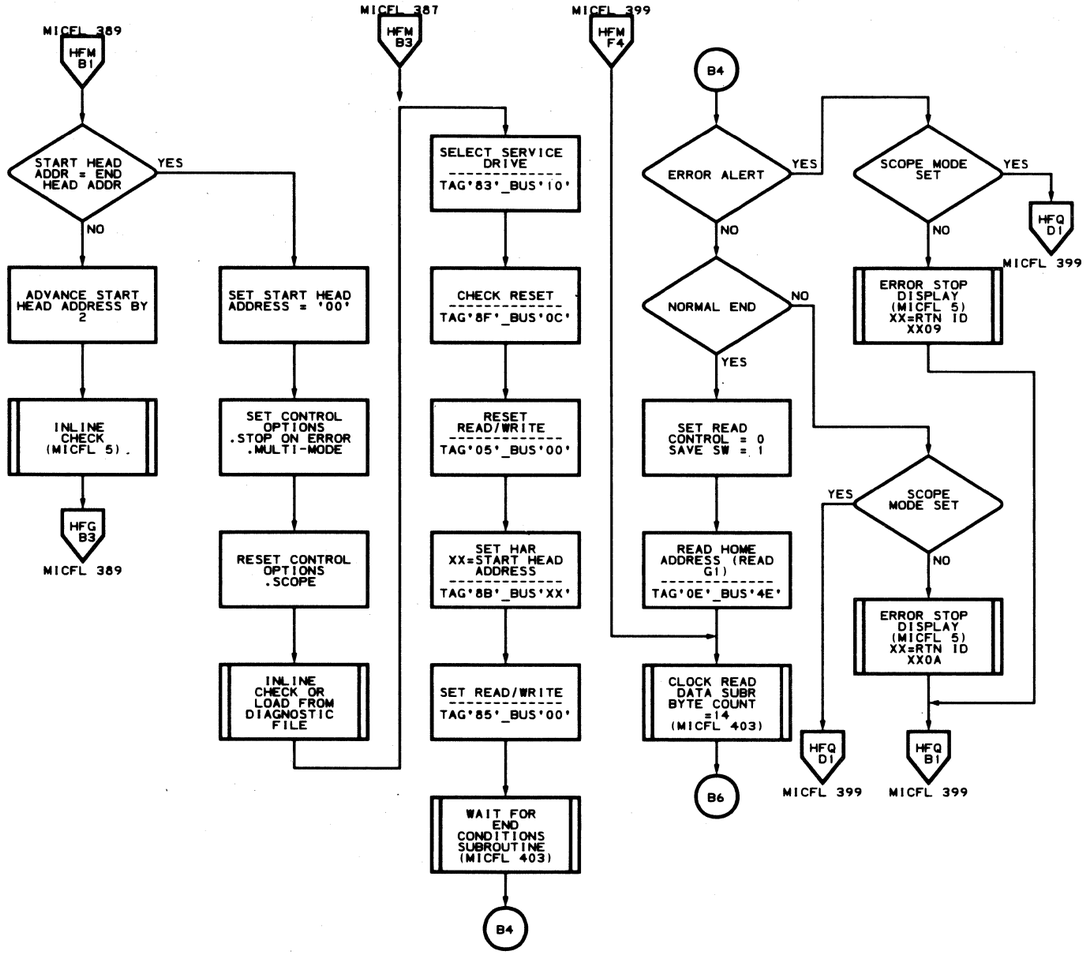
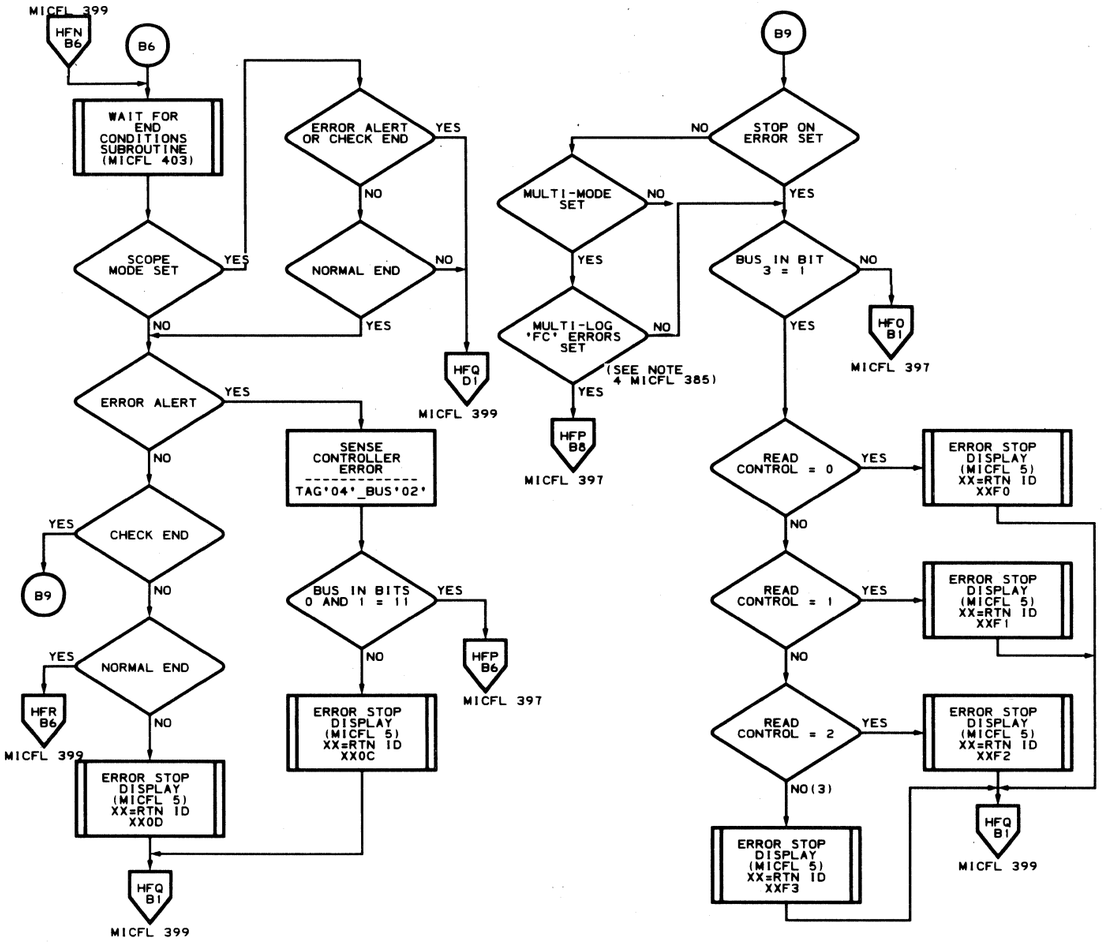
ROUTINES B0, B1, B2 – REFORMAT CE TRACKS UTILITY ROUTINES MICFL 395





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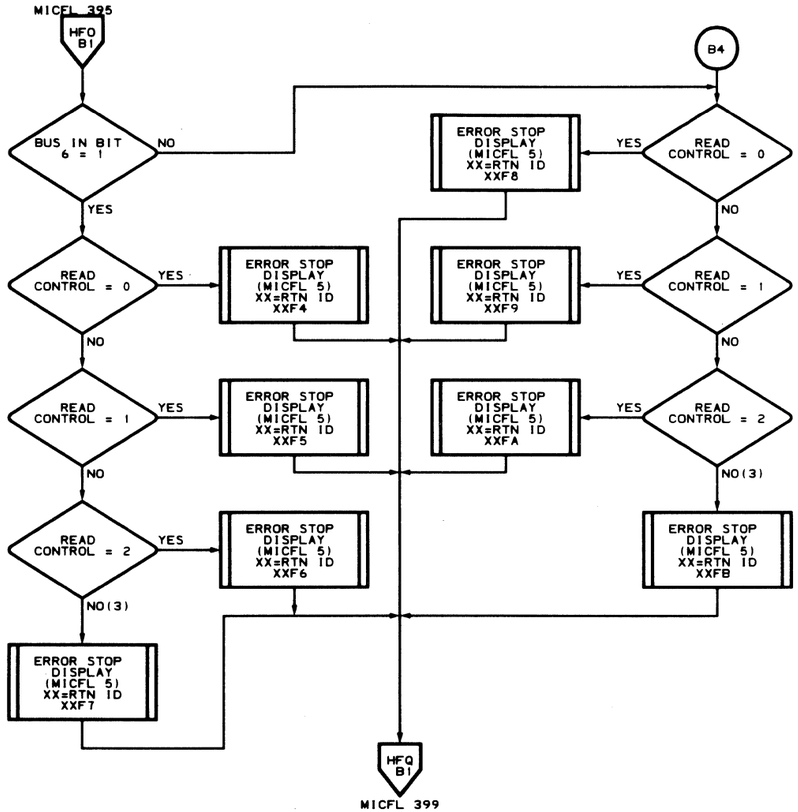

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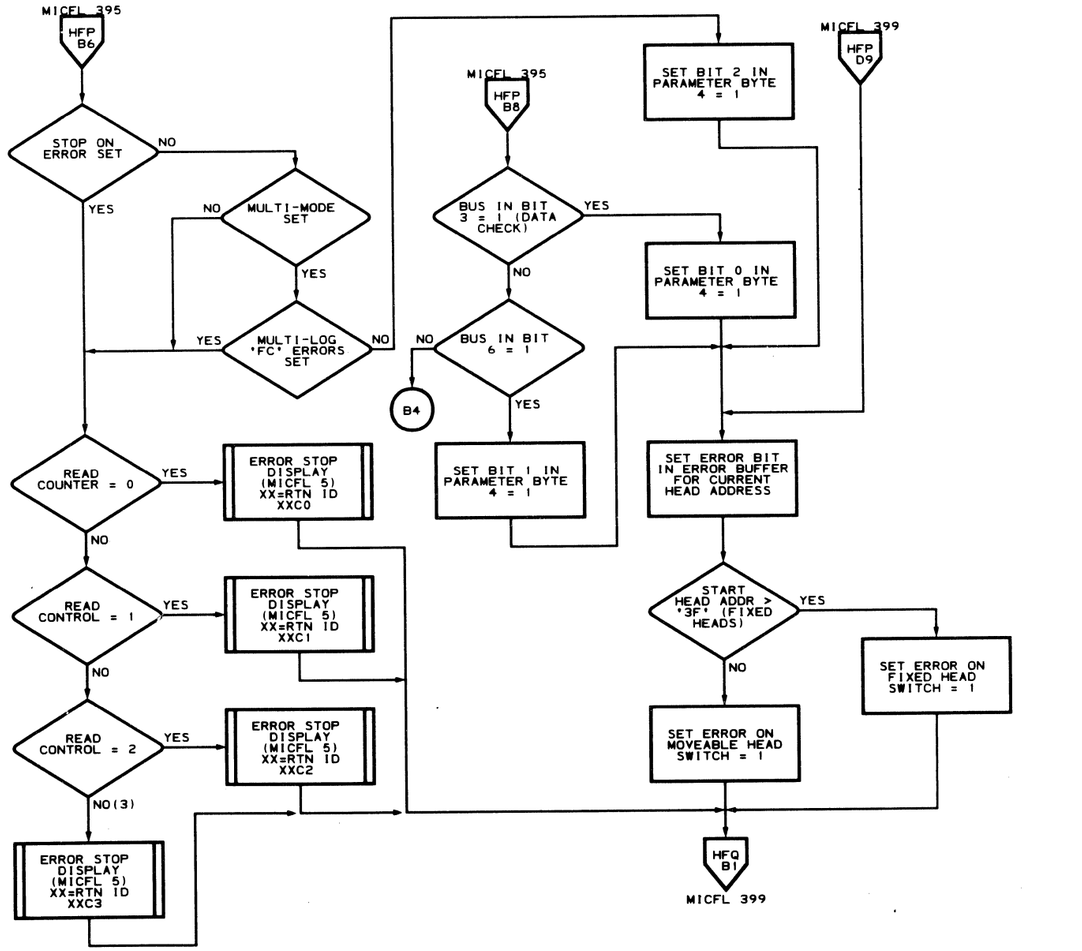

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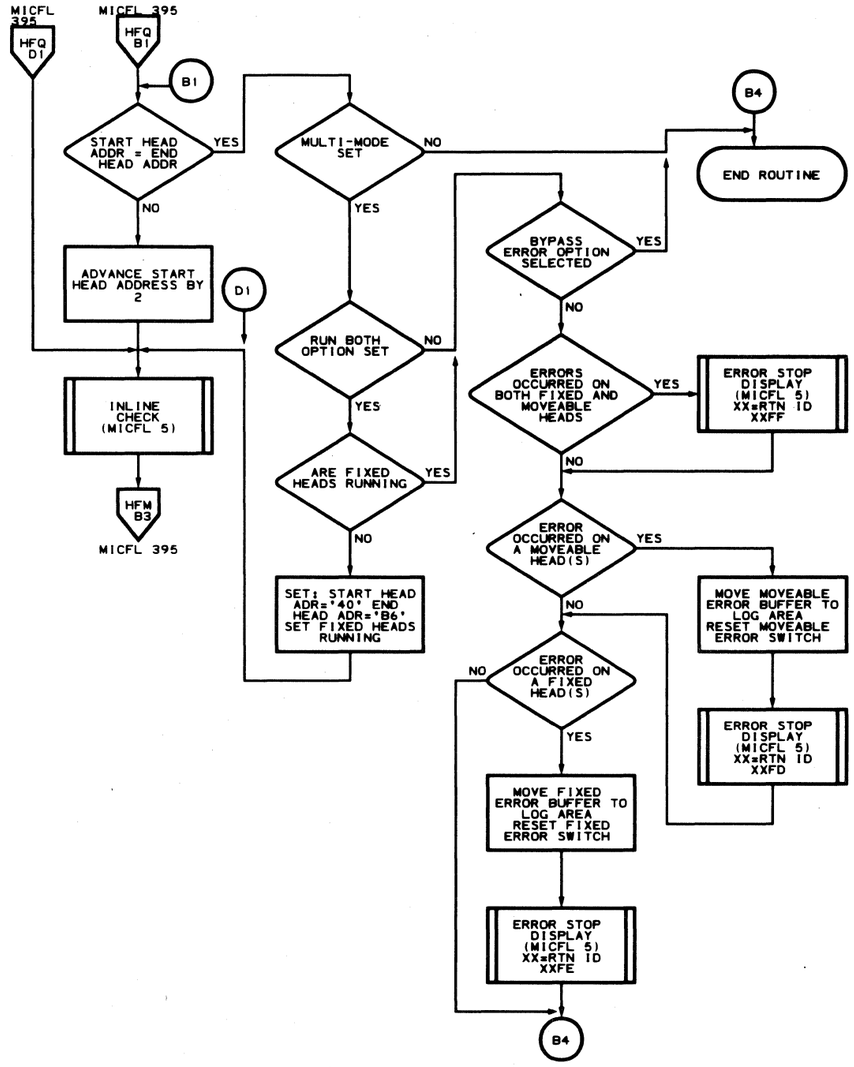

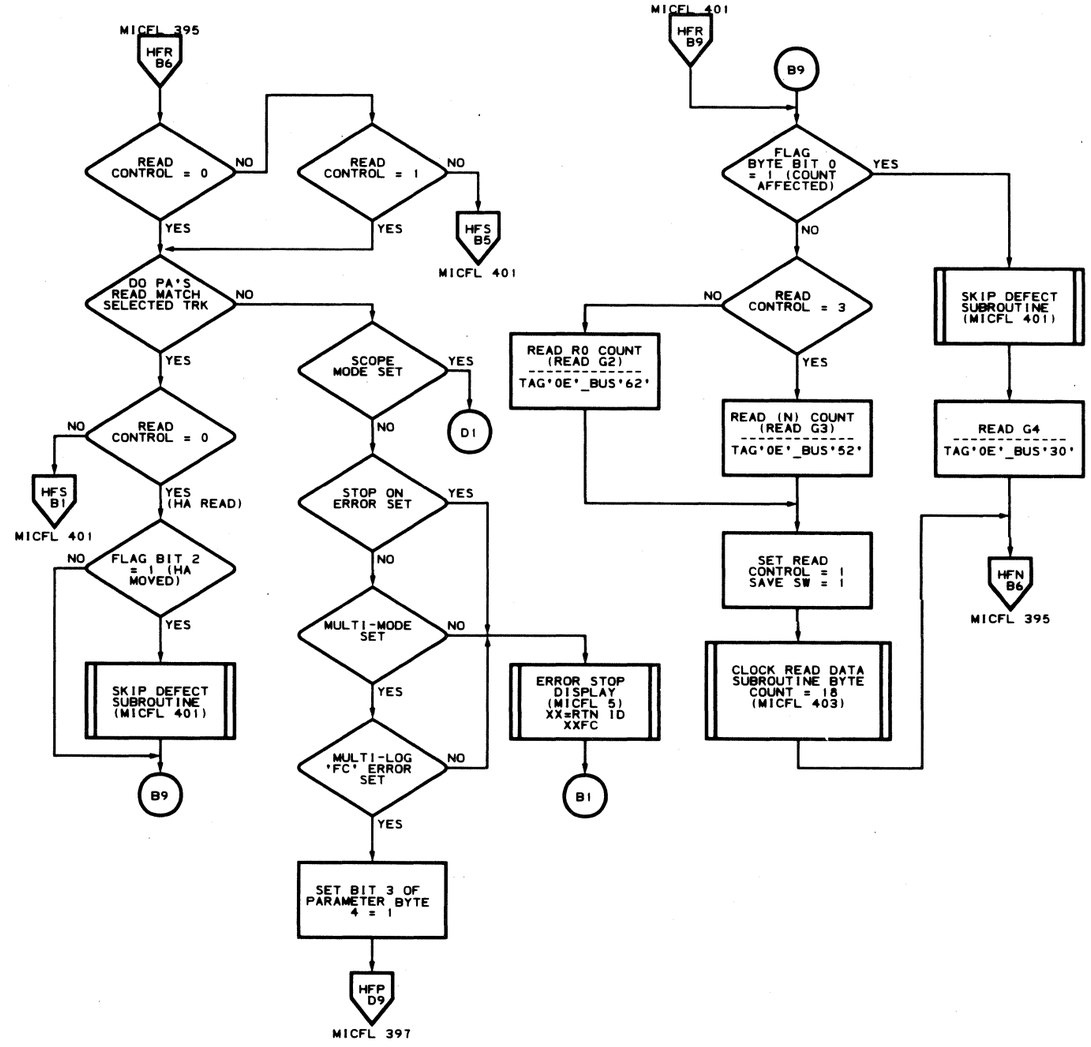

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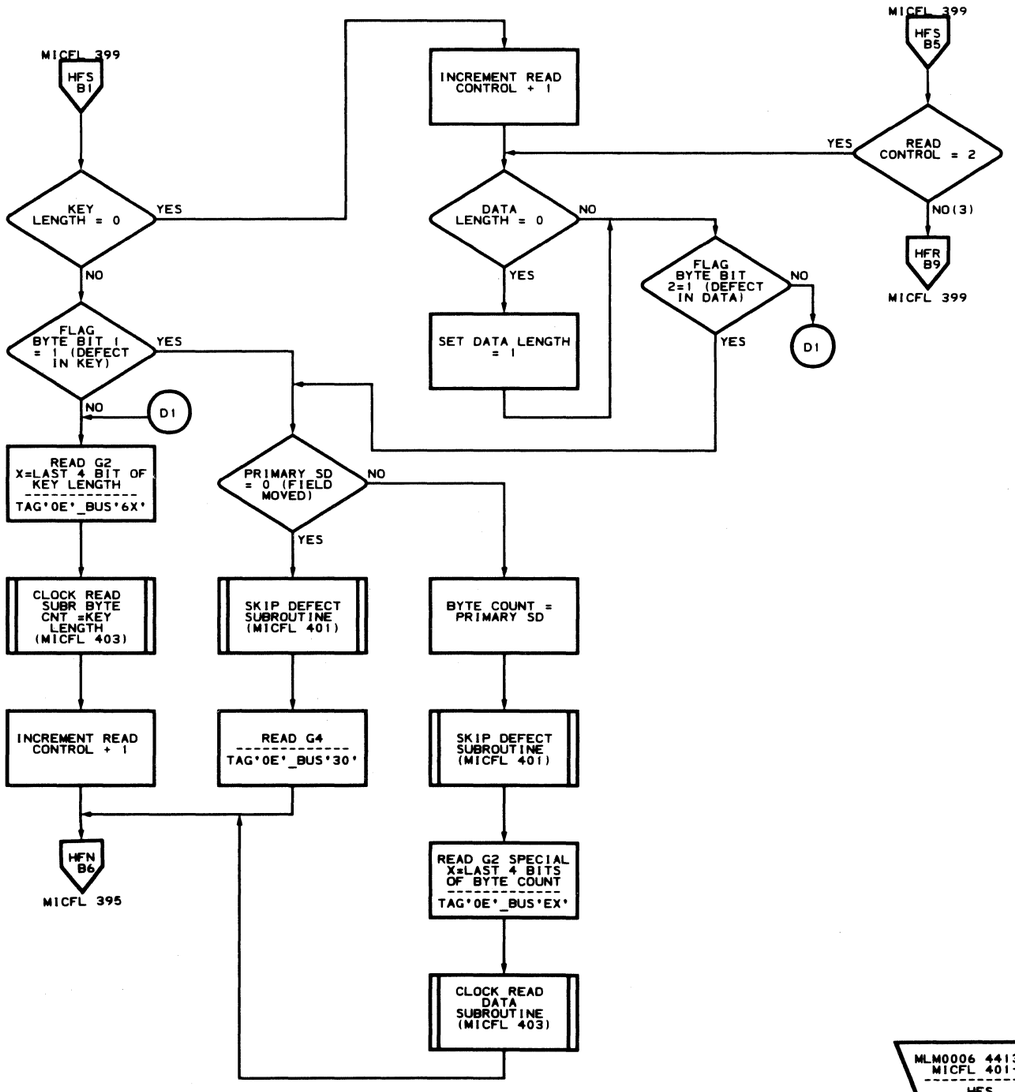

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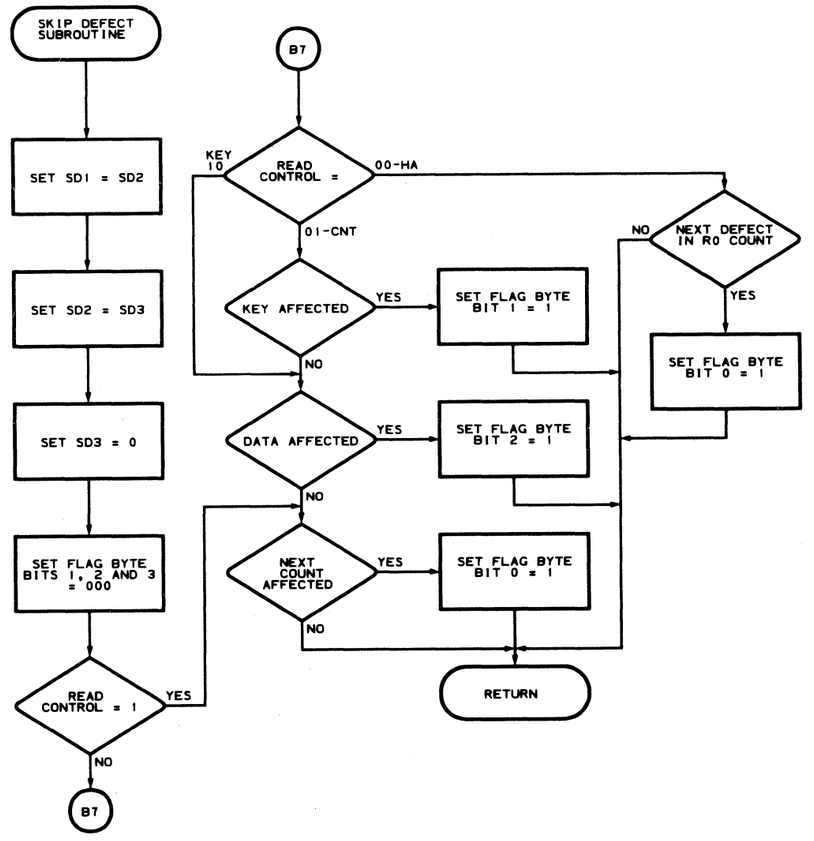

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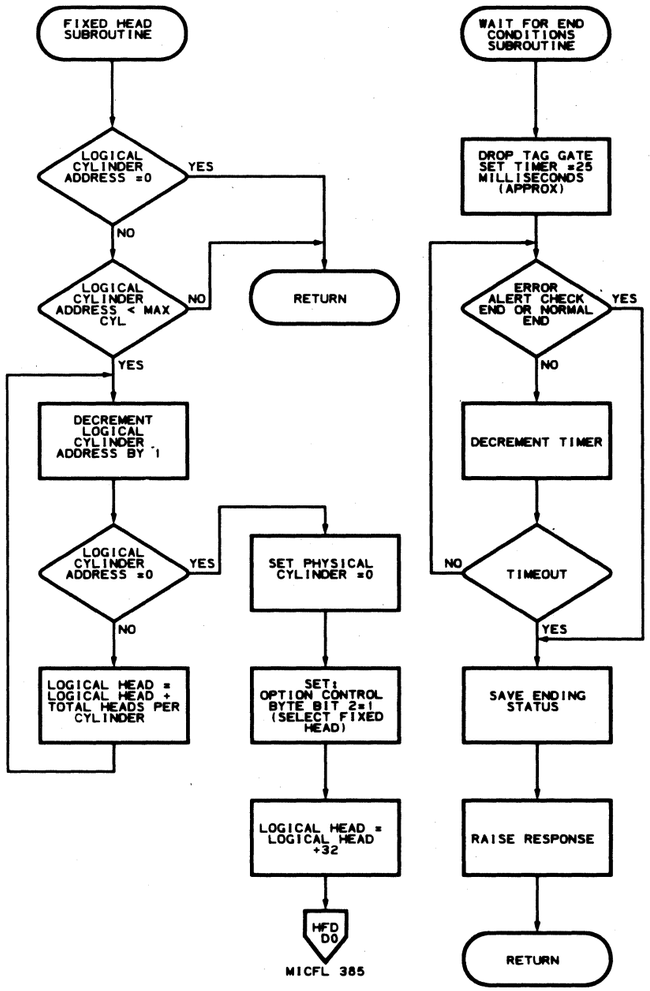
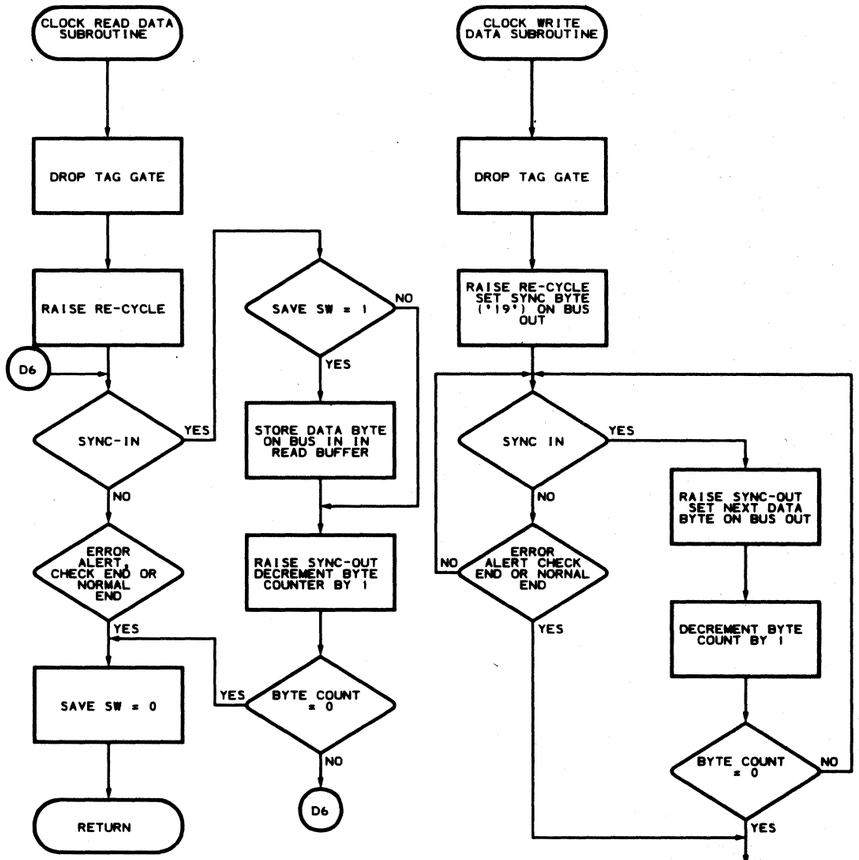
ROUTINES B0, B1, B2 – REFORMAT CE TRACKS UTILITY ROUTINES MICFL 403





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HFV
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ROUTINE B3 – 3350 DEVICE STATUS DISPLAY PROGRAM

DESCRIPTION

The purpose of Routine B3 is to provide additional information regarding the status of a given drive. Its primary function is to supplement the information obtained from running a microdiagnostic that encounters an error. A symptom code and/or 15 bytes of status information are provided. The program is designed to run in two passes as follows:

Pass 1:

Pass 1 generates a symptom code from the failing state of the device or controller. It is important that the device be left in its failing state (no resets performed). The controller may be reset, as the Controller Interface Check byte and the Controller Check bytes are stored by the diagnostic control monitor whenever a microdiagnostic detects an error. If pass 1 is unable to generate a symptom code 'E1FF' is displayed. (See FSI 60 for the flowchart logic and MICRO 64 for running instructions.)

Pass 2:

Pass 2 retrieves 12 bytes of information from the drive and 3 bytes of information from the controller. This is displayed in the Data Display lamps one byte at a time and provides the current state of a given drive and controller. (See FSI 65 for sense bytes 1 through 15 details.)

Note 1: *Reloading and restarting this routine will yield different results. This is because any error condition was reset during pass 1 (original execution of pass 1).*

Note 2: ***If the routine is restarted after Pass 2, only Pass 2 is repeated. It is necessary to reload the routine in order to repeat Pass 1.***

Note 3: *Pass 2 information is displaed in the following order:*

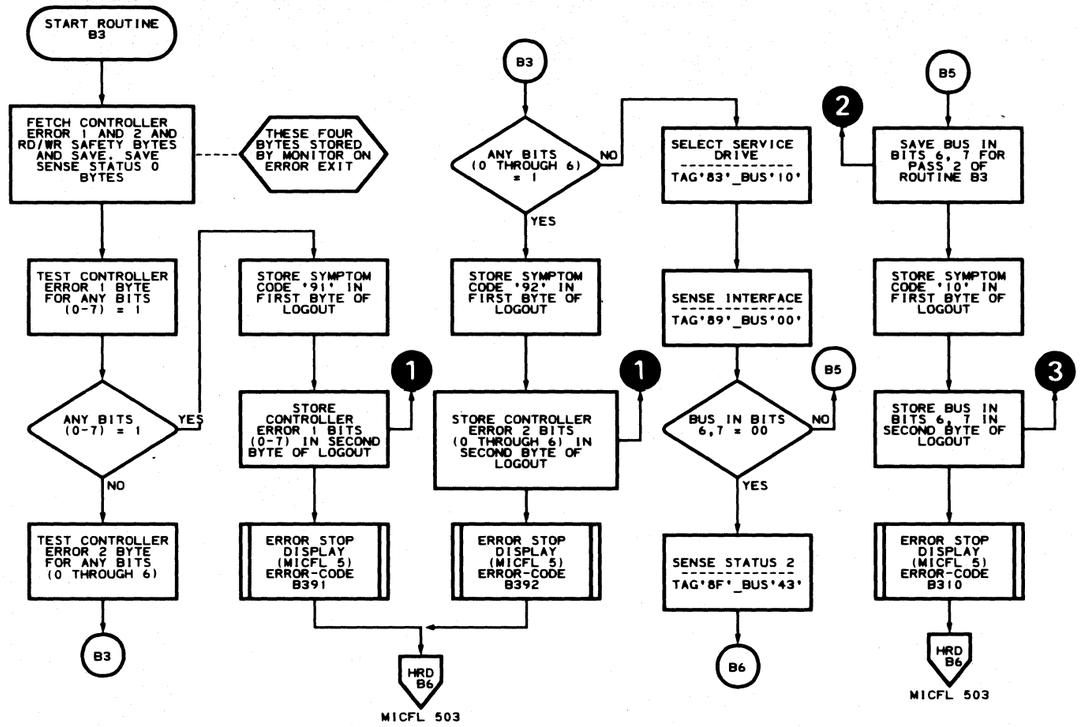
Byte	Meaning	Command Issued
1	Sense Physical Address (CE Drive Physical Address)	Tag '04' Bus '10'
2	Sense HAR	Tag '8F' Bus '05'
3	Sense Difference Counter	Tag '8F' Bus '09'
4	Request Drive Status	Tag '84' Bus '00'
5	Sense Status 1	Tag '8F' Bus '83'
6	Sense Status 2	Tag '8F' Bus '43'
7	Sense Status 3	Tag '8F' Bus '23'
8	Read/Write Safety	Fetched from Monitor
9	Sense Status 4	Tag '8F' Bus '13'
10	Controller Checks	Fetched from Monitor
11	Controller Interface Checks	Fetched from Monitor
12	Device Interface Checks	Tag '89' Bus '00'
13	Sense Target Register	Tag '8F' Bus '0D'
14	Cyl Address Register	Tag '8F' Bus '01'
15	Sense Status 0	Fetched from Monitor

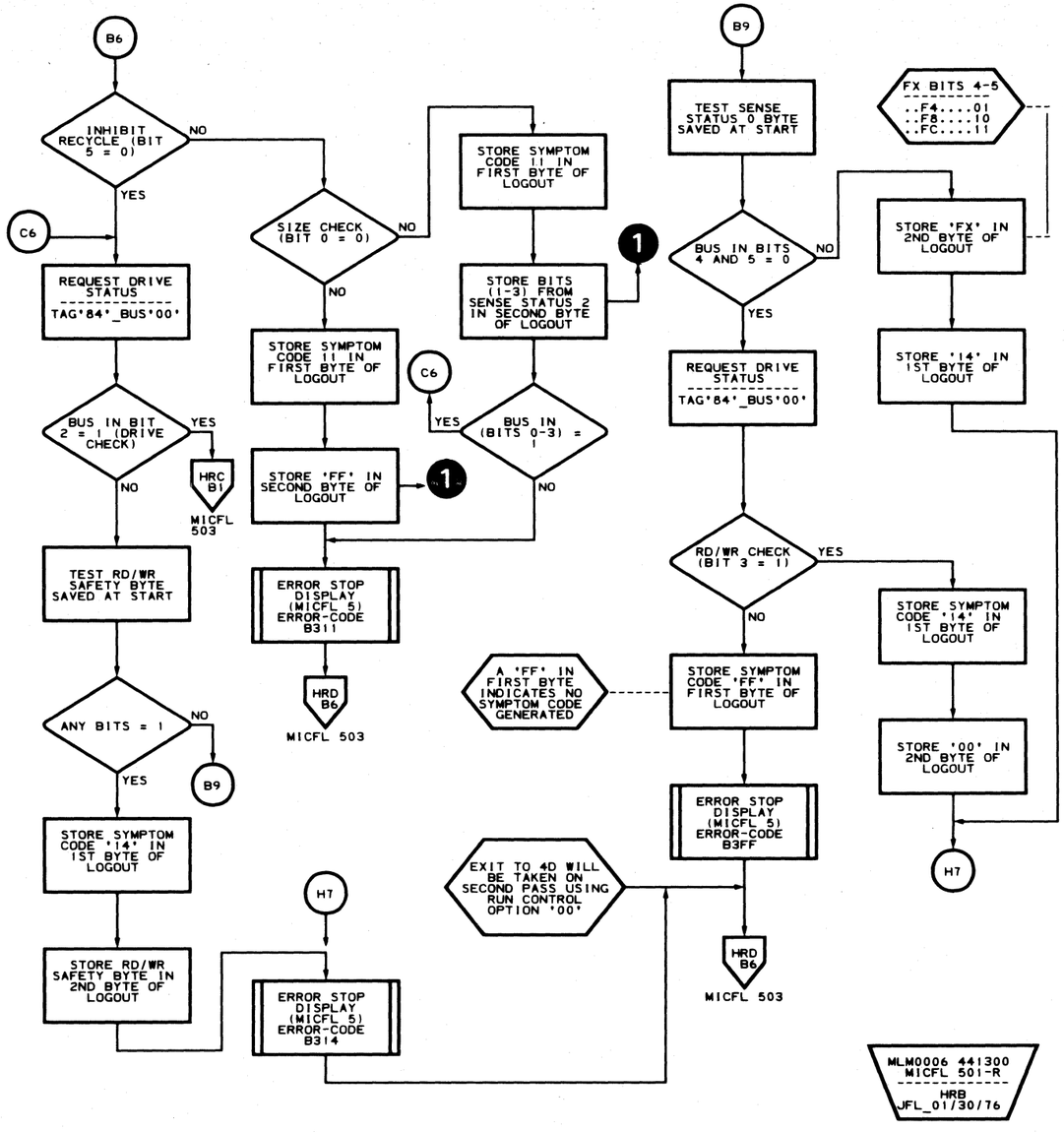
Note 4: ***When the last byte (byte 15) has been displayed, the message displayed is 'CEB3'. CE (in the Control lamps) indicates the end of logout and B3 (in the Data Display lamps) indicates the Routine ID. This is standard message display for all logouts.***

OPERATING PROCEDURE

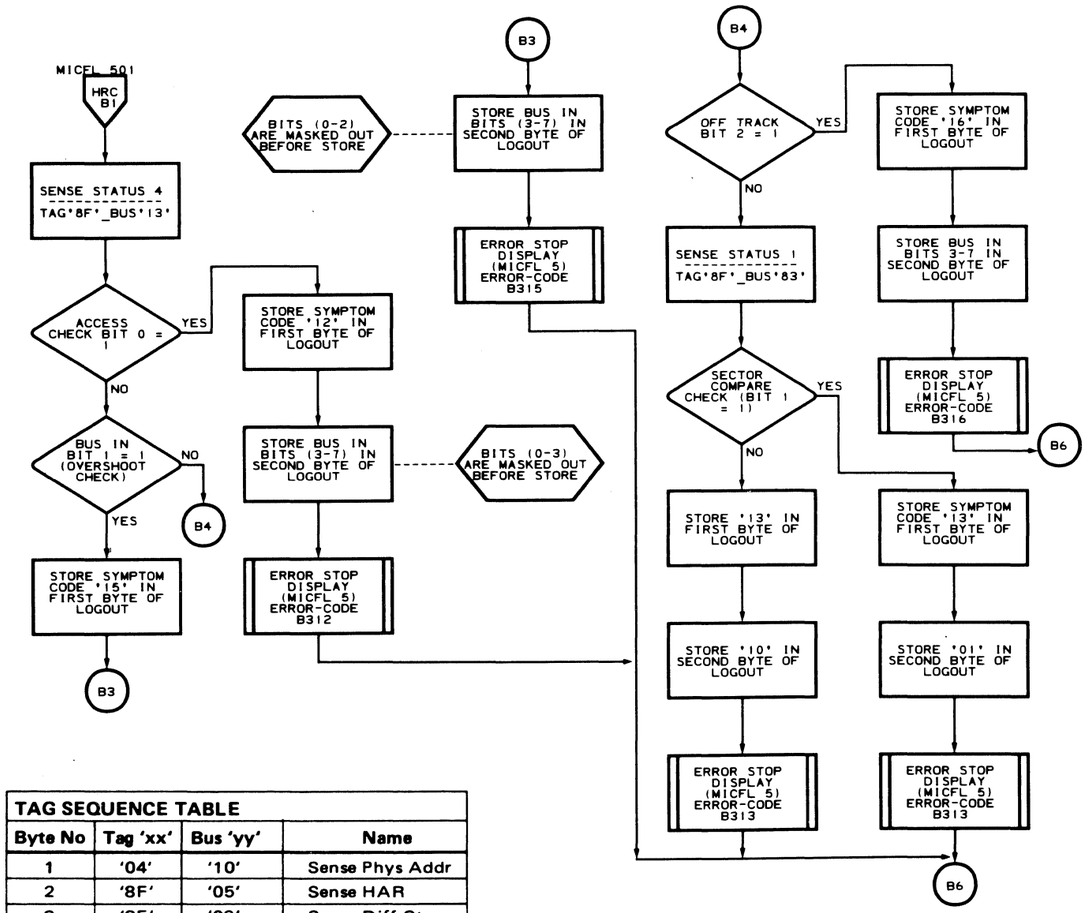
Refer to detailed run instructions on MICRO 64.

ROUTINE B3 – DEVICE STATUS DISPLAY UTILITY ROUTINE MICFL 501



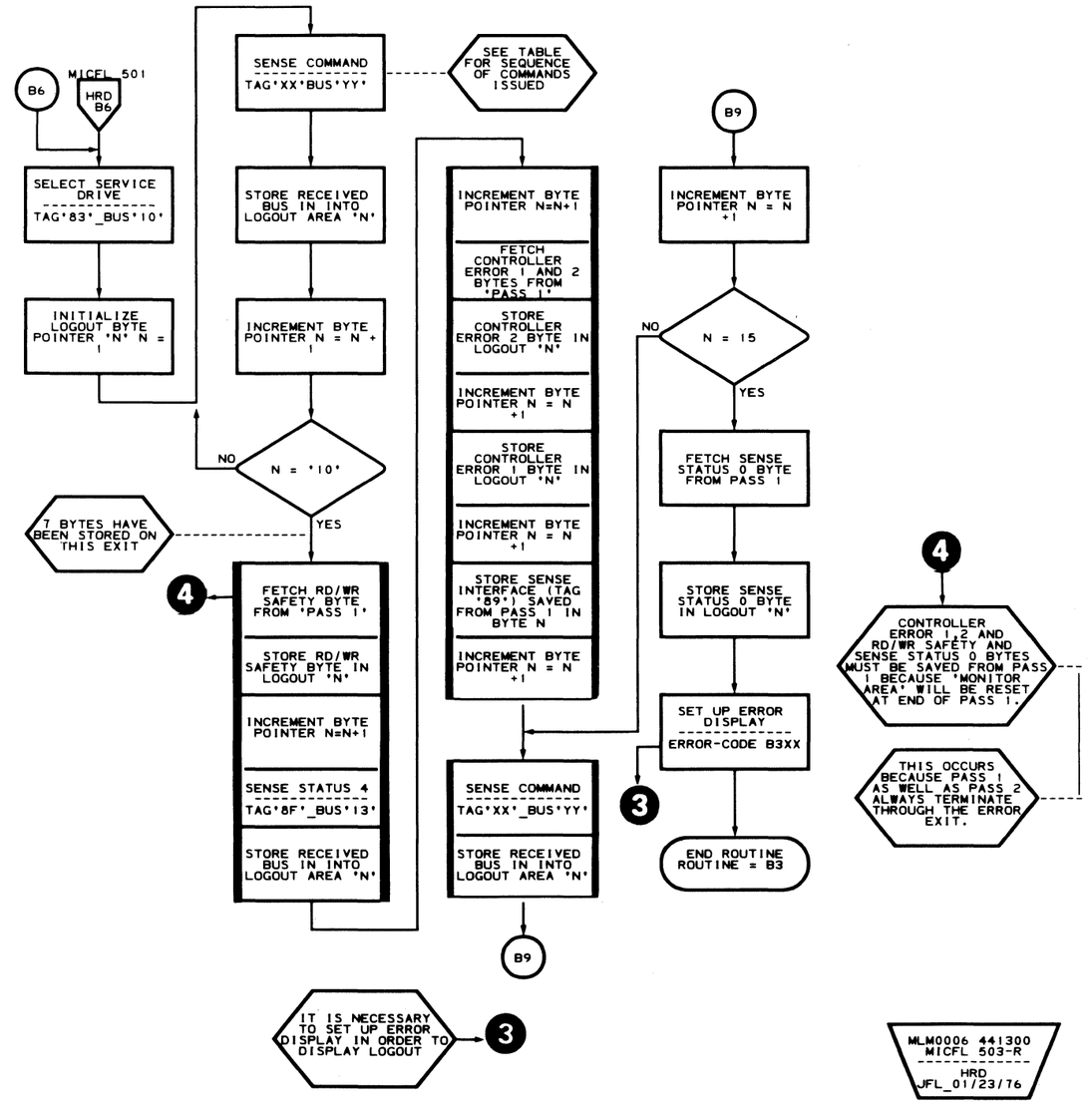


ROUTINE B3 – DEVICE STATUS DISPLAY UTILITY ROUTINE



TAG SEQUENCE TABLE			
Byte No	**Tag 'xx'**	**Bus 'yy'**	**Name**
1	'04'	'10'	Sense Phys Addr
2	'8F'	'05'	Sense HAR
3	'8F'	'09'	Sense Diff Ctr
4	'84'	'00'	Sense Dev Status
5	'8F'	'83'	Sense Status 1
6	'8F'	'43'	Sense Status 2
7	'8F'	'23'	Sense Status 3
8	Fetched From 'Error Bytes'		Sense Read/Write
9	'8F'	'13'	Sense Status 4
10	Fetched from 'Error Bytes'		Controller Error 2
11			Controller Error 1
* 12	'89'	'00'	Sense Interface
13	'8F'	'0D'	Sense Target
14	'8F'	'01'	Sense CAR
** 15	'8F'	'03'	Sense Status 0

* Sense Interface Bus-In saved from Pass 1
** FHFE only



ROUTINE B4 – 3350 TAG CYCLE UTILITY PROGRAM

DESCRIPTION

Routine B4 executes any valid tag bus or delay commands that the CE selects with parameter entry, with the exception of Write Op (Tag '0F') under drive selection, Rezero (Tag '8F' Bus '02') and Seek Start (Tag '8F' Bus '08').

Each delay or tag command consists of two bytes of entry and up to seven commands at one time. These entries are known as the command string. Following the last command, zeros must be entered to complete the parameter field.

Once the desired commands have been entered, execution can be started by the Start/Stop run control option. (Refer to MICRO 10 and 11.)

When the routine begins, the commands are executed in a sequential manner. When '00' appears in the control byte, execution halts and an inline check is performed. After the diagnostic control monitor has returned control, the routine begins command execution with the first command. This procedure provides a continuous loop.

If the command string requires modification after execution has started, the routine must be reloaded. The routine may be halted and restarted at any time by using run control option 00. (Refer to MICRO 10 and 11.)

The following describes the format of command bytes. The first byte is called the control byte. This byte is used to: (1) signal the end of the command string. (2) describe the tag or delay being issued, and (3) control the data to and from the CE panel. The second byte of the command is used for Bus Out or a base delay value depending on the command in the control byte.

Since the tag only uses 5 bits of the first byte (0,4,5,6, and 7), the remaining bits (1,2 and 3) are used for special control options. The ORing of these two fields forms the control byte.

The tags for the 3350 Drive are described on OPER 98 through 100.

Caution: Do not use Seek Start (Tag '8F' Bus '08') or Rezero (Tag '8F' Bus '02'). HDA damage may result and a B413 error stop occurs.

SPECIAL CONTROL OPTIONS

000 Forms a control byte of '0000 0000', which is used for End of String indicator.

001 The routine executes a Tag '0A' Bus '40' (Read Data Entry switches) prior to execution of the tag in bits 0,4,5,6 and 7. The value read from the Data Entry switches is used as a Bus Out value during the execution of the coded tag.

Note: *Tag '0A' Bus '40' (Read Data Entry switches) also resets the CE Alert line that is activated by the Execute switch. If this command is used, the program may require repeated operation of the Execute switch in order to stop execution.*

Example: To transmit a Set Head Address Register Tag (1000 1011) with the ability to vary the value, use option code 001. The ORing of Tag '1000 1011' and control 001 forms a control byte of '1001 1011'. Refer to sample command string on this page.

When this control byte is encountered by the program, it splits off and executes two tags:

1. Tag '0A' Bus '40' Read Data Entry switches
2. Tag '8B Bus 'xx' Set Head Address Register where xx = Data Entry switches

010 This control option is used in the same manner as option 001 except that the Bus In received from the coded tag is transmitted to the Data Display lamps.

Example: '1010 1111' control option byte (Tag '8F' and control option 010) coded with a Bus Out of '05' creates a Sense Head Address Register Tag. When this control byte is encountered by the program, the control byte issues a Data Display Tag after the coded tag was issued. (Refer to sample command string on this page.)

Tag '8F' Bus '05' Sense Head Address Register
Tag '0D' Bus 'xx' Data Display

where xx =Bus In value from the Sense Head Address Register Tag

011 This option code is used to insert microsecond delays in the command string. When this code is used, bits 4,5,6, and 7 become the delay multiplier. The base delay value is contained in the second byte of the command. See example for different values of delays. Tag Gate is dropped at beginning of any delay.

100 This option code is used to insert millisecond delays in the command string. When this code is used, bits 4,5,6, and 7 become the delay multiplier. The base delay value is contained in the second byte of the command. Tag Gate is dropped at beginning of any delay.

101 thru 111 Not used.

Example of Different Delays

	Command Entry Byte 1	Byte 2	Delay Value
a.	30	C8	200 microseconds
b.	32	C8	400 microseconds
c.	40	C8	200 milliseconds
d.	41	C8	200 milliseconds
e.	43	64	300 milliseconds

Example b: C8 (hex) = 200 (decimal)
multiplier = 2
Total = 400
3 in byte 1 = microsecond
Therefore, total delay=400 microseconds

Example e: 64 (hex) = 100 (decimal)
multiplier = 3
Total = 300
4 in byte 1 = millisecond
Therefore, total delay=300 milliseconds

Note: *0 multiplier is defaulted to 1.*

Sample Command String

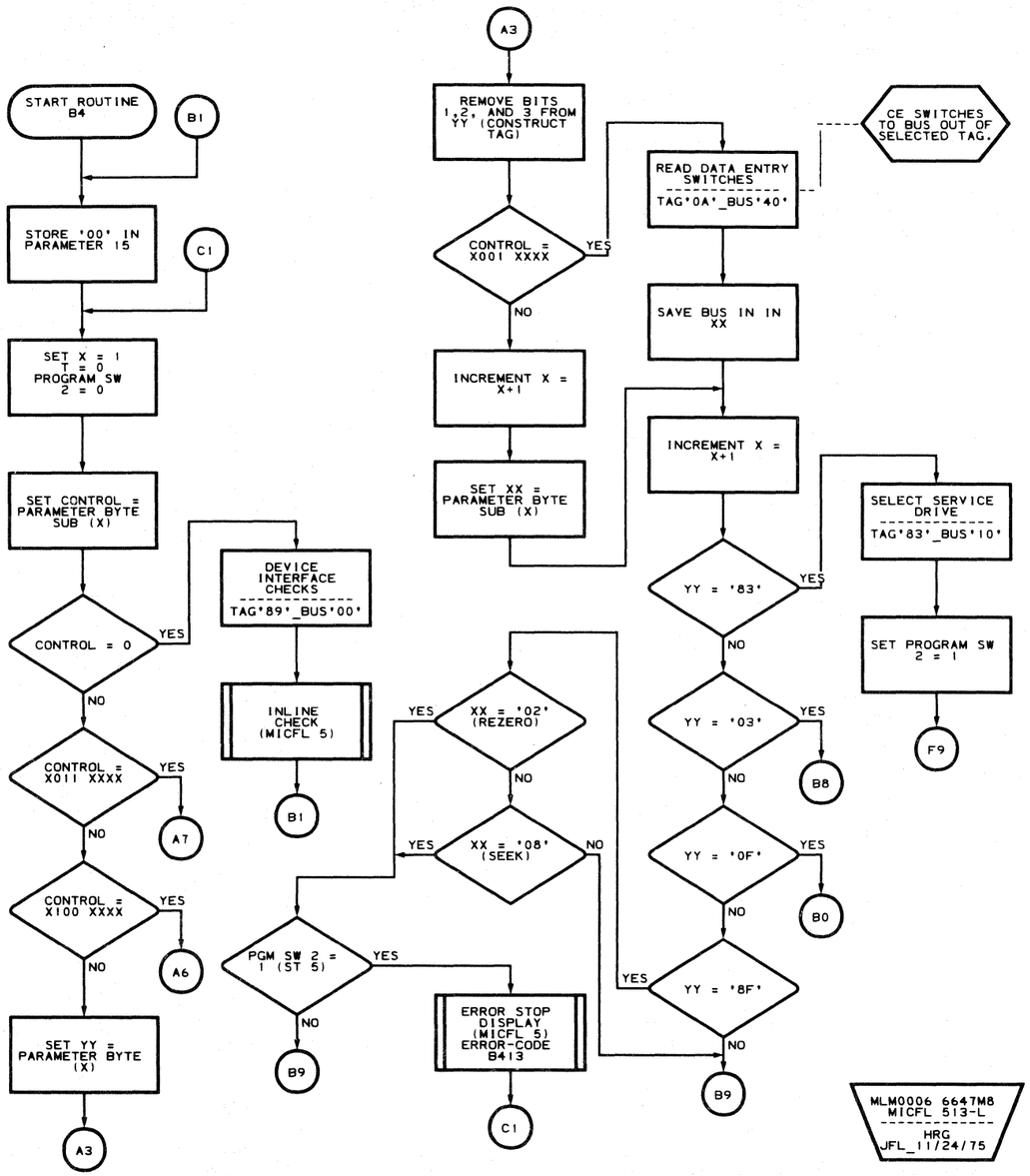
Parameter Byte	Hex Value	
1	83	Tag to Select Drive
2	XX	Bus Out is supplied by the program. (Service Drive only)
3	9B	Tag to set Head Address Register. Option Code 1001 is used so Bus Out is supplied from the Data Entry switches.
4	XX	Bus Out from CE switches.
5	AF	Tag to Sense Head Address Register (HAR). Option Code 1010 is used so received Bus In is transmitted to the Data Display lamps.
6	05	Bus Out for Sense HAR Tag
7	8C	Tag to set Difference Counter
8	FF	Bus Out value
9	8F	Tag to Sense Difference Counter
A	09	Bus Out for Sense Difference Counter
B	42	200 millisecond delay
C	64	
D	00	
E	00	Filler for remaining parameter
F	00	

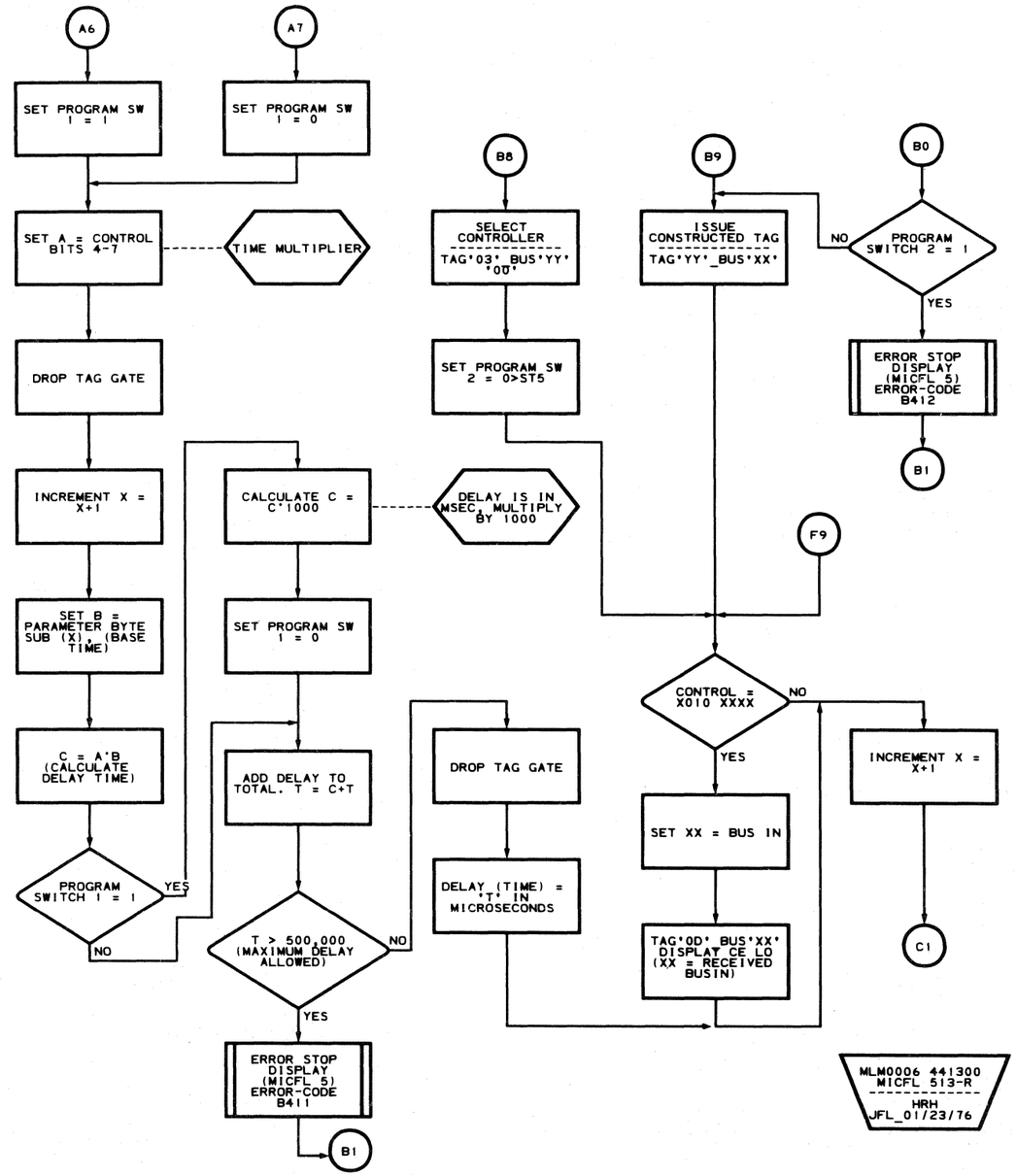
Note: *The run control option '00' must be entered to begin program execution. The desired HAR value must be set in the Data Entry switches as soon as the '8C' message is displayed in the control lamps.*

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 68 for parameter entry.

ROUTINE B4 – TAG CYCLE UTILITY





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ROUTINE B6 – 3350 STRING SWITCH

DESCRIPTION

Routine B6 checks those controller functions that are unique to a switchable controller interface. The routine must be run simultaneously on both controller interfaces.

Although the routine must be loaded and started on each controller interface, it is controlled exclusively from the interface designated as the Master. Control and error information is passed between the interfaces through registers in the service drive.

The routine contains 7 tests. Normally, tests 1 through 6 are run in sequence ending with Error Code B6E0. B6E0 is displayed to remind the CE to run test 7. Test 7 requires a special operating procedure. (See MICRO 70, Figure 1.)

Normally, tests 1 through 6 execute 8 times before linking to the next test. Tests 3 through 6 execute once with each device address (0 through 7) on each of the 8 passes. Test 7 is run only once each time it is called.

Error information is displayed at the end of the test. The Error Code is developed by ORing the error data from both interfaces. Tests 3 through 6 develop a second error byte which indicates the failing register position. For details of a specific error, see the Error Code Dictionary in the MICRO section.

OPERATING THEORY

Prior to running any test, the two interfaces must be synchronized. Once synchronized, the routine executes short sequences of operations separated by fixed time delays. The operational and delay sequences are offset in time so that each operational sequence is executed during the time delay on the other interface. In actuality, the test execution alternates between the two interfaces.

One interface is referred to as the Master, the other as the Slave. There are two flowcharts for each test in the MICFL section. One flowchart is the Master, the other is the Slave. The flowcharts are identical except for the Error Codes.

OPERATING PROCEDURES

To effectively run routine B6 microdiagnostics, two passes are required: Pass 1, in which Interface A is the Master and B is the Slave; and Pass 2 in which B is the Master and A is the Slave.

Pass 1: (A = Master)

1. Set the CE Interface Select switch to the Interface B position, then load and execute routine B6. Use standard operating procedures (MICRO 10), but **do not enter Run Options or Parameters at this time.** A few seconds after starting, the routine displays '8DFF' indicating it is ready to accept control information from the other interface.
2. Set the CE Interface Select switch to the Interface A position. Routine B6 may now be loaded and run on Interface A using standard operating procedures (MICRO 10). Run Options and/or Parameters may be entered if desired.
3. Test 7 requires a special operating procedure. Refer to Figure 1 on MICRO 70. Looping routine B6 (Loop Run Option) runs tests 1 through 6 only.

Pass 2: (B = Master)

1. Set the CE Interface Select switch to the Interface A position, then load and execute routine B6. Use standard operating procedures (MICRO 10), but **do not enter Run Options or Parameters at this time.** A few seconds after starting, the routine displays '8DFF' indicating it is ready to accept control information from the other interface.
2. Set the CE Interface Select switch to the Interface B position. Routine B6 may now be loaded and run on Interface B using standard operating procedures (MICRO 10). Run Options and/or Parameters may be entered if desired.
3. Test 7 requires a special operating procedure. Refer to Figure 1 on MICRO 70. Looping routine B6 (Loop Run Option) runs tests 1 through 6 only.

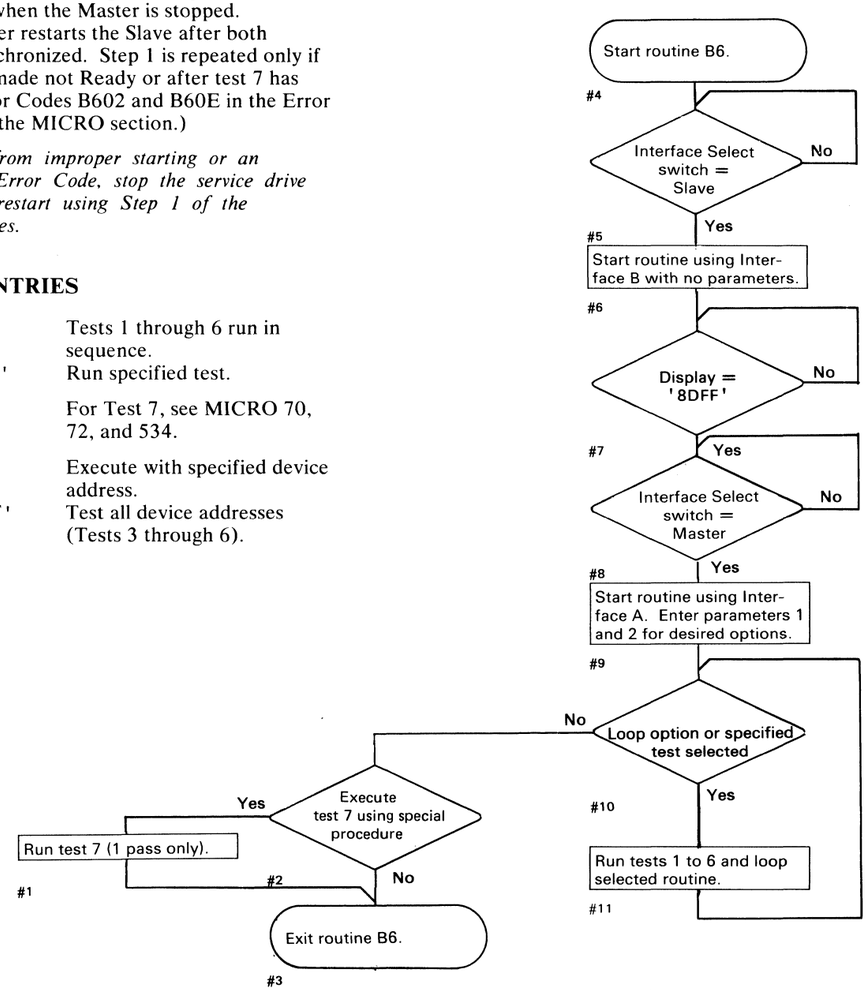
RESTART PROCEDURES

To restart (Pass 1 or Pass 2), begin at Step 2. The Slave enters an idle loop when the Master is stopped. Restarting the Master restarts the Slave after both interfaces are resynchronized. Step 1 is repeated only if the service drive is made not Ready or after test 7 has been run. (See Error Codes B602 and B60E in the Error Code Dictionary in the MICRO section.)

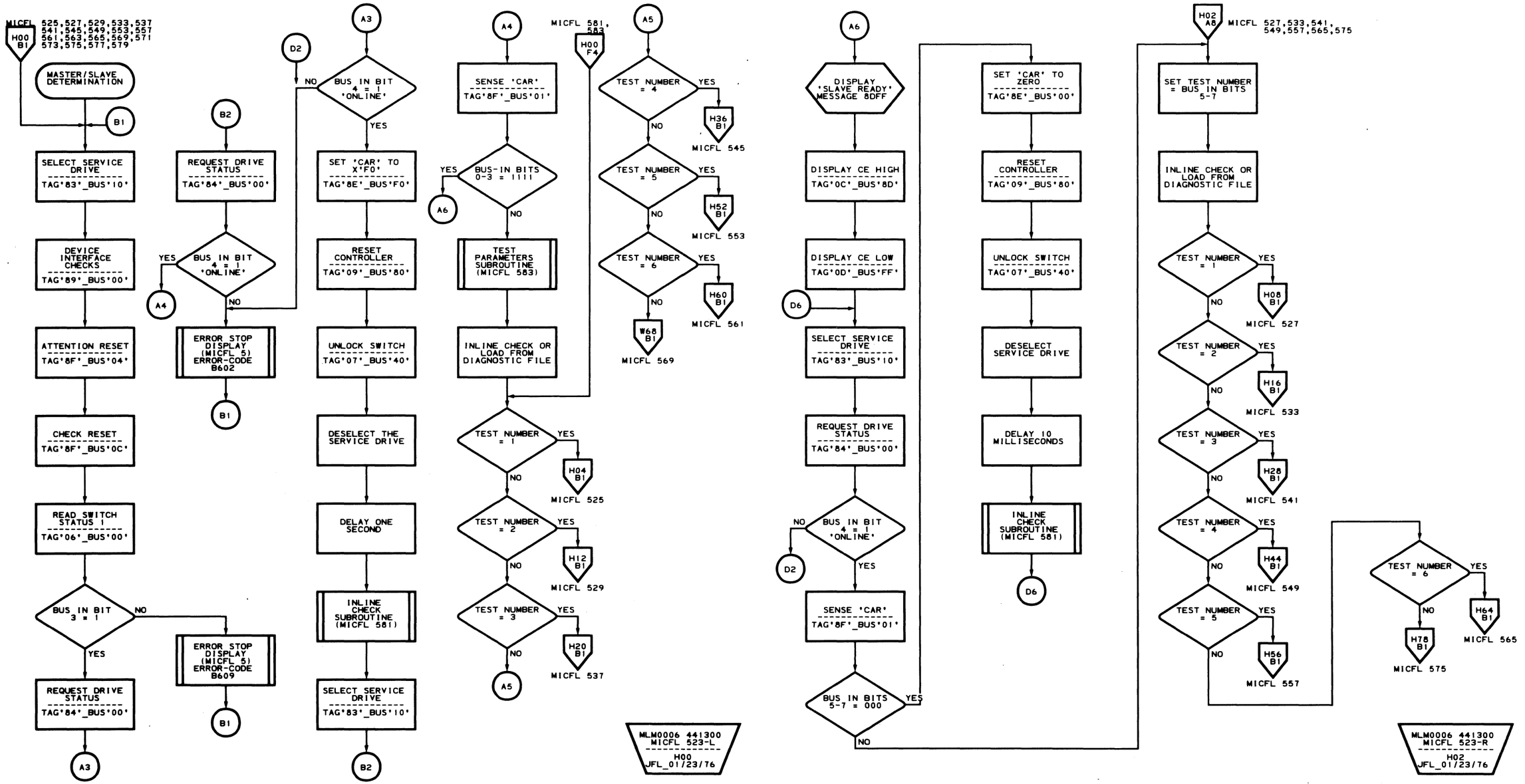
Note: *To recover from improper starting or an unexpected 8DFF Error Code, stop the service drive momentarily, then restart using Step 1 of the Operating Procedures.*

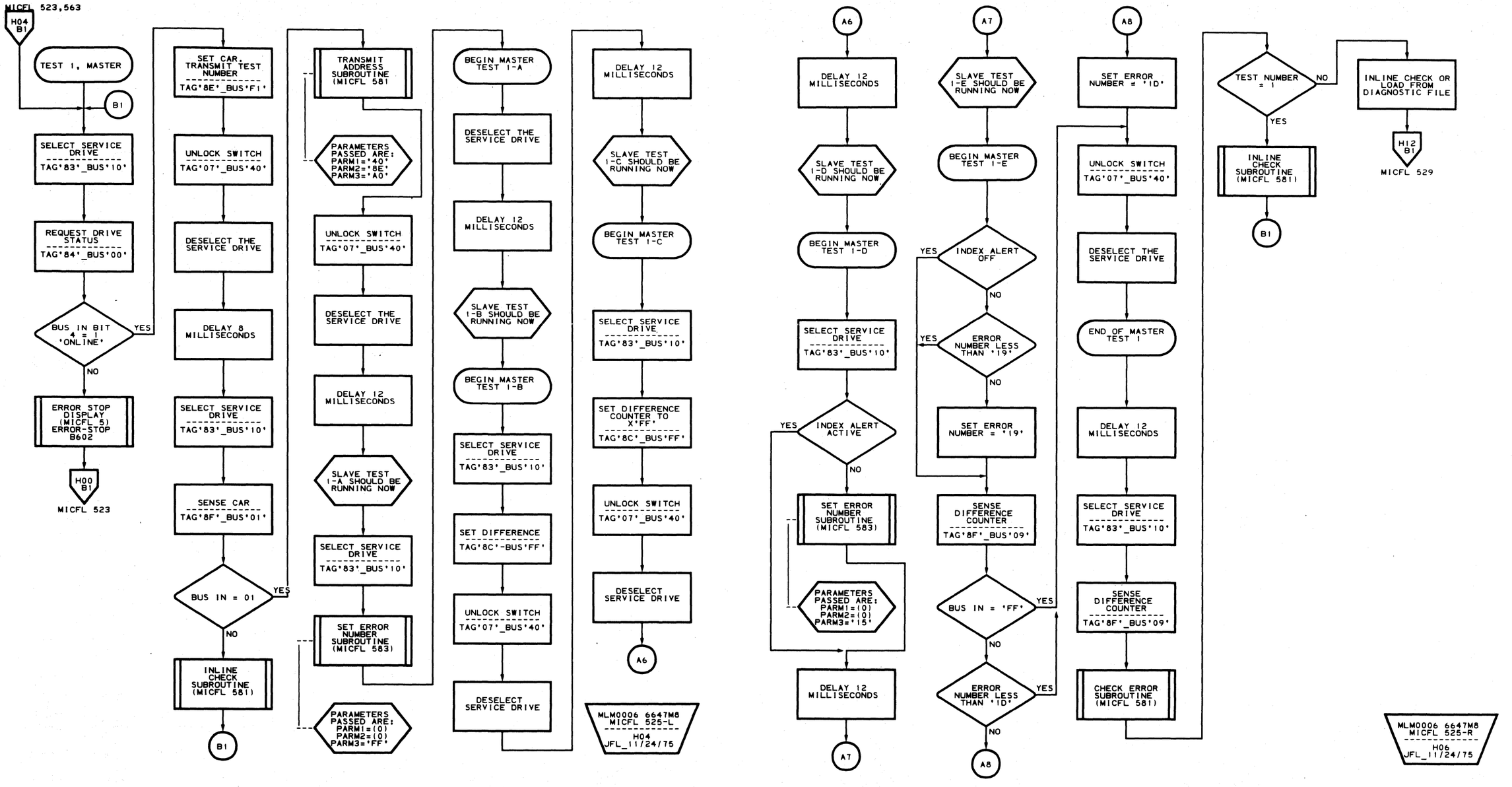
PARAMETER ENTRIES

Entry 1. '00'	Tests 1 through 6 run in sequence.
'01'—'06'	Run specified test. For Test 7, see MICRO 70, 72, and 534.
Entry 2. '00—'07'	Execute with specified device address.
'08'—'FF'	Test all device addresses (Tests 3 through 6).

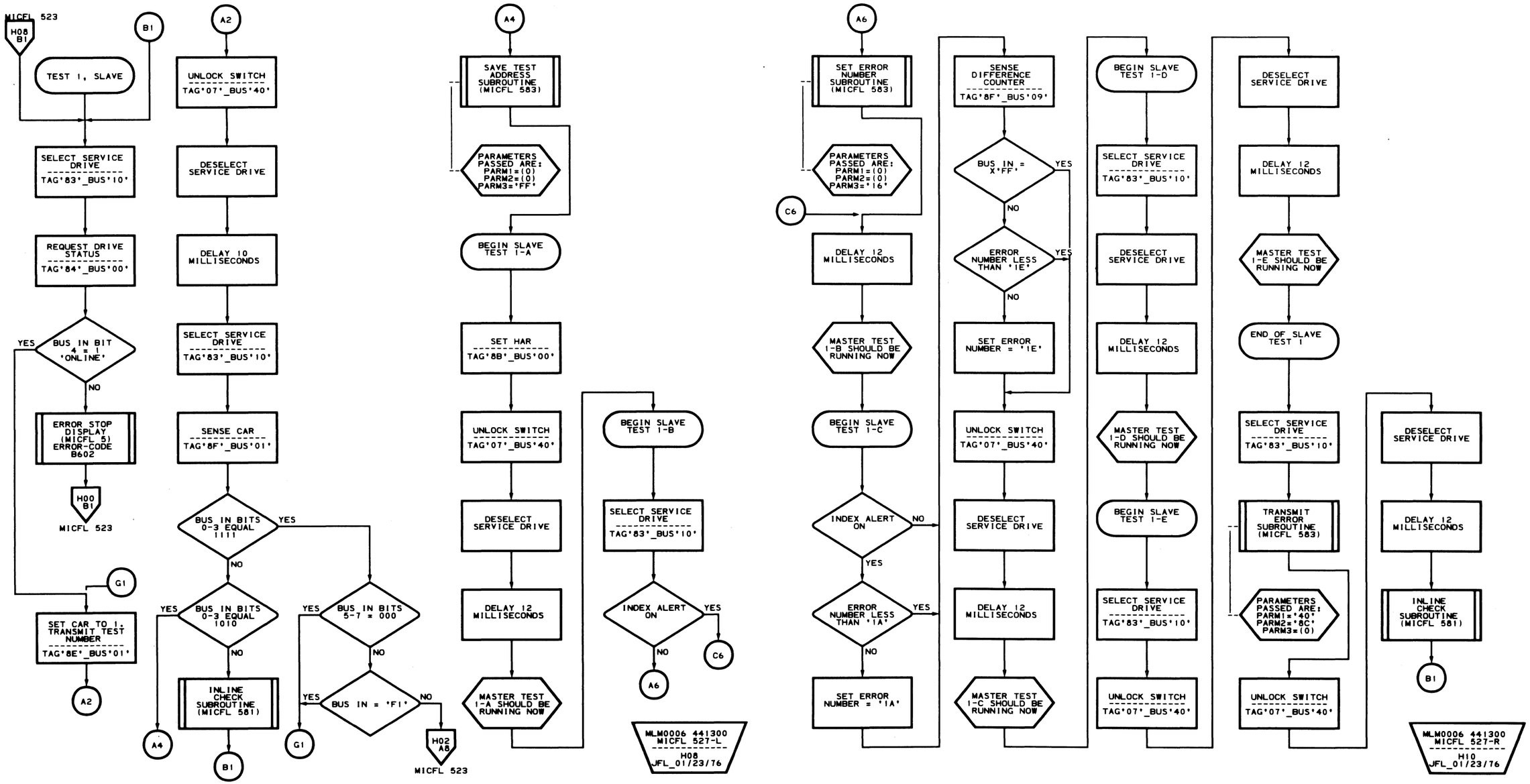


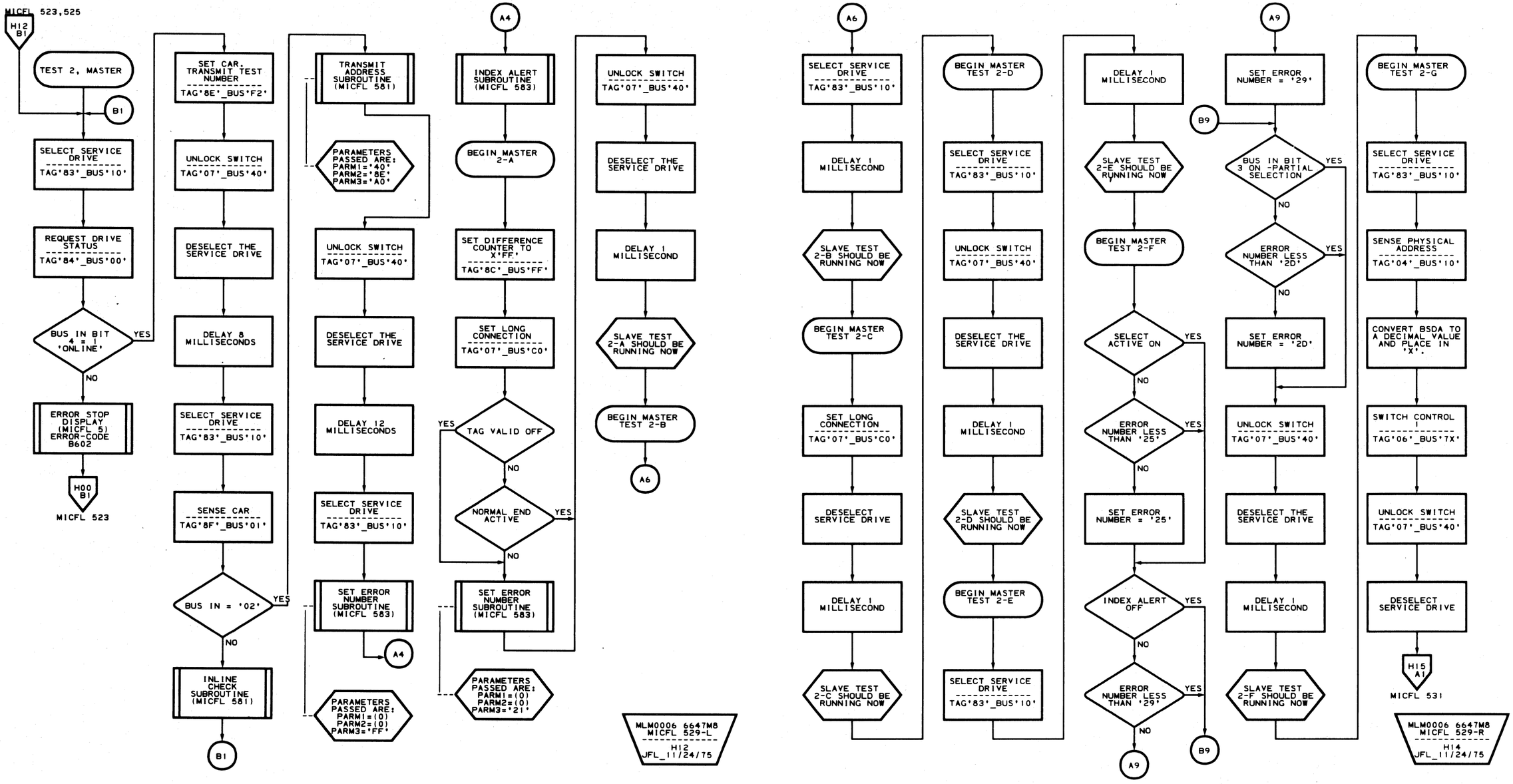
ROUTINE B6 – STRING SWITCH TESTS



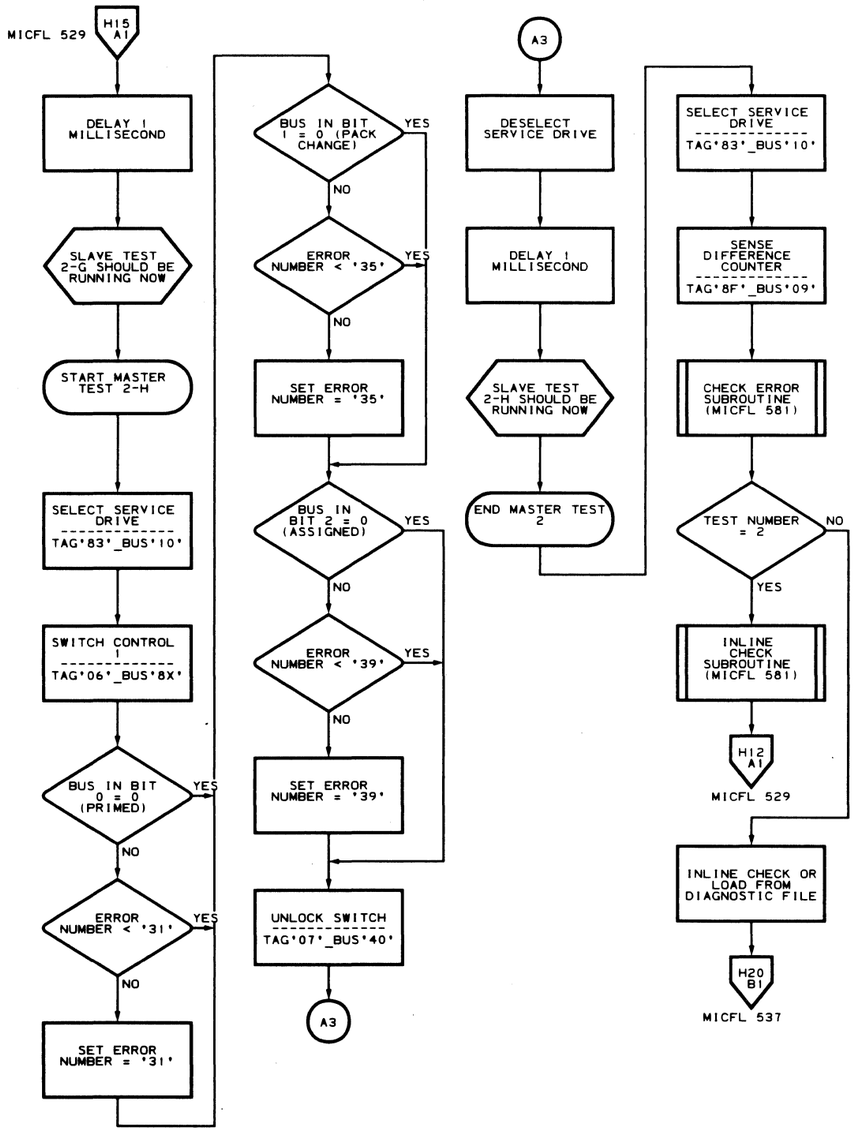


ROUTINE B6 – STRING SWITCH TESTS





ROUTINE B6 – STRING SWITCH TESTS



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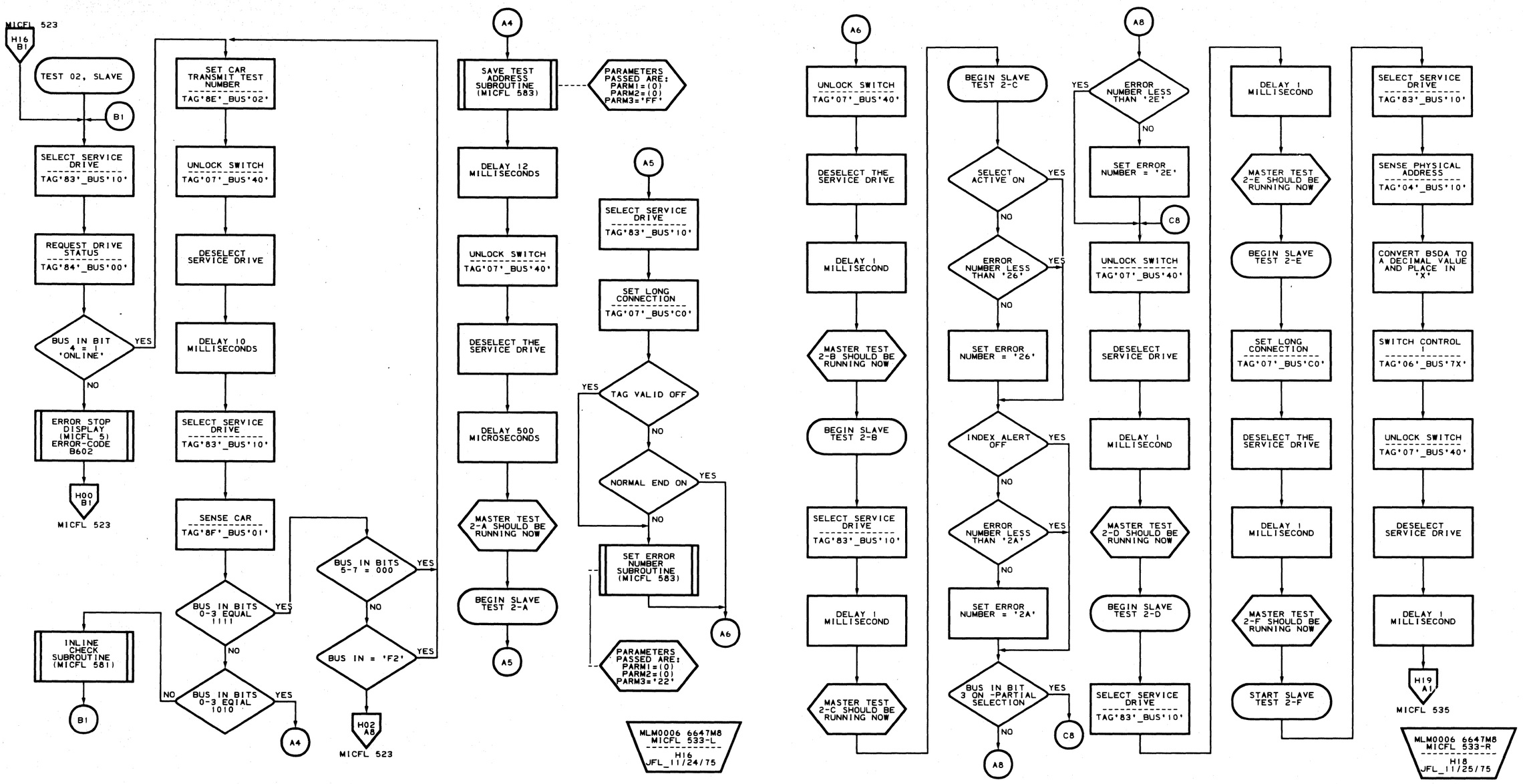
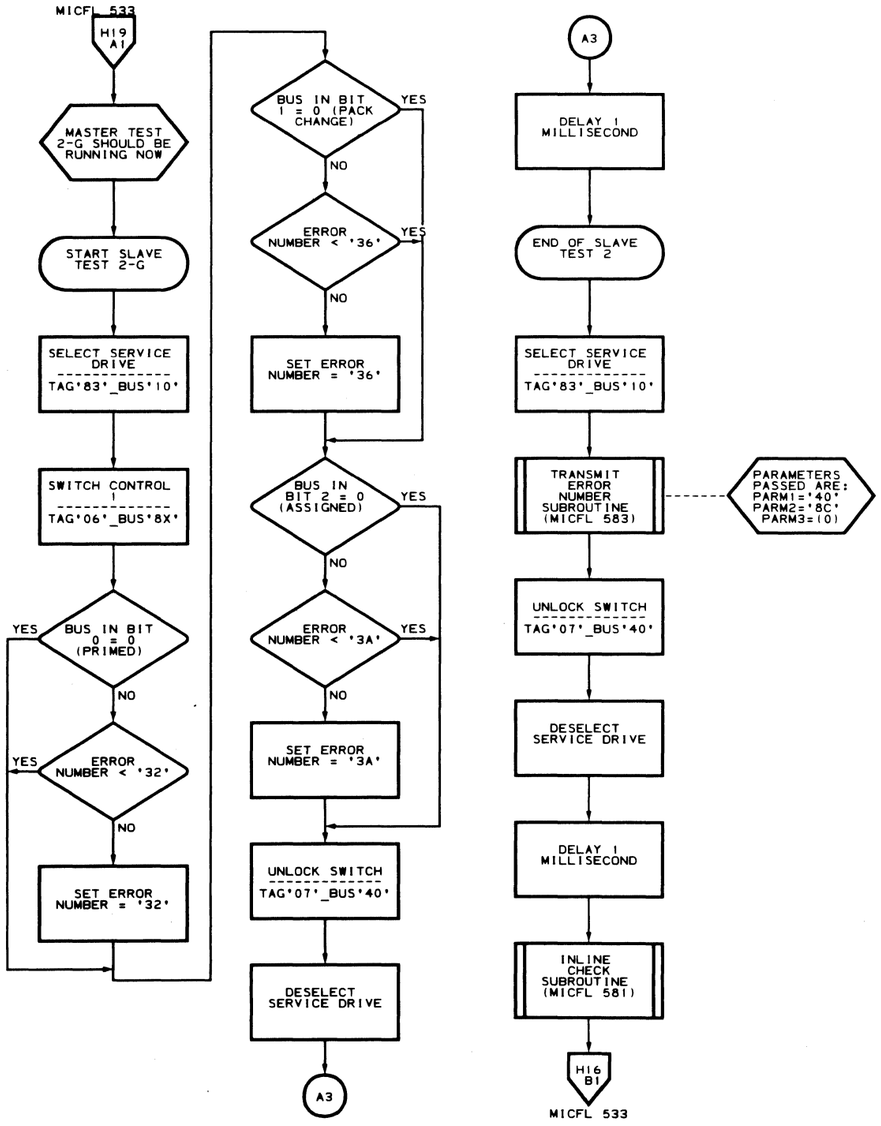


ROUTINE B6 – STRING SWITCH TESTS



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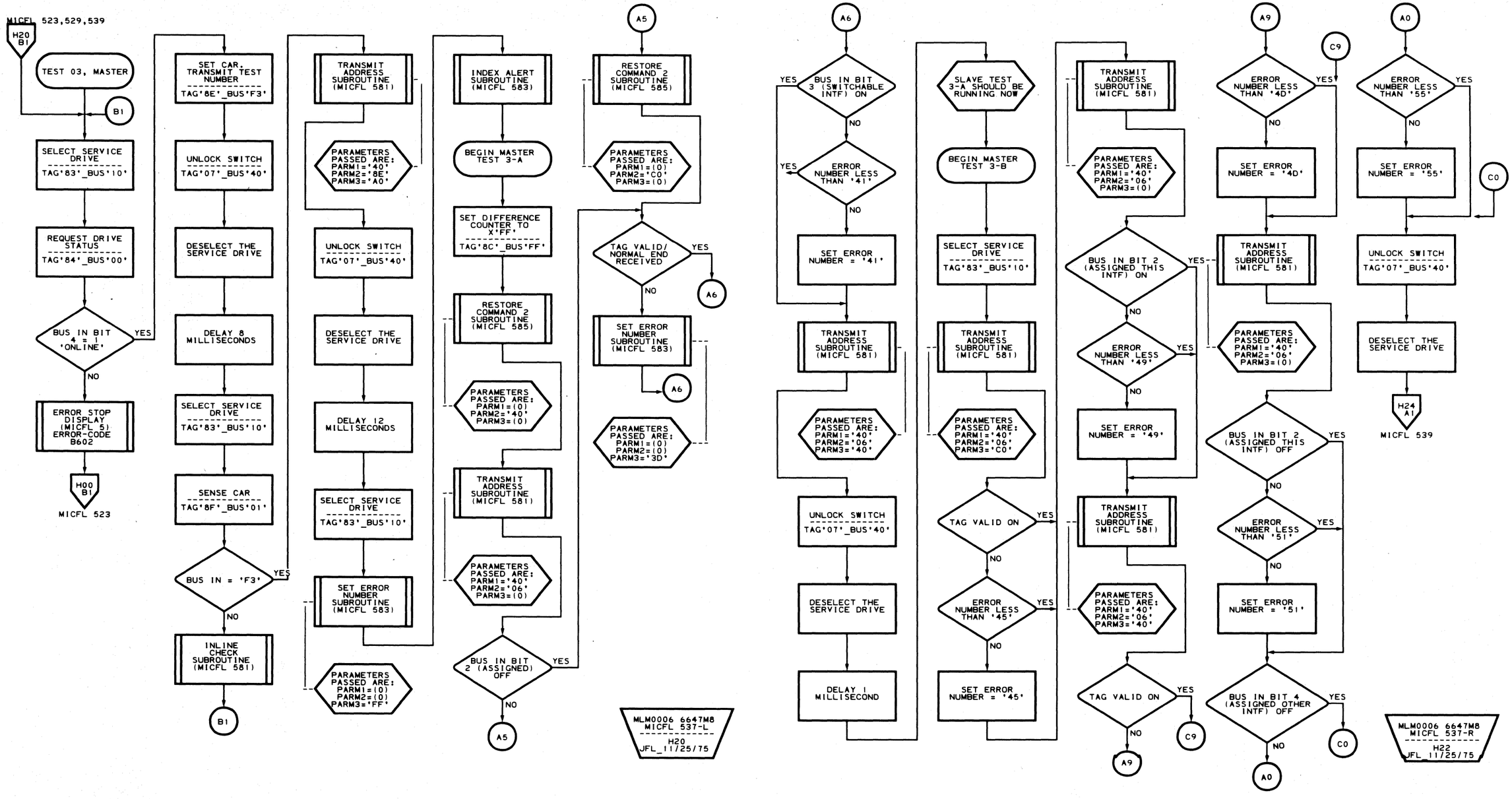

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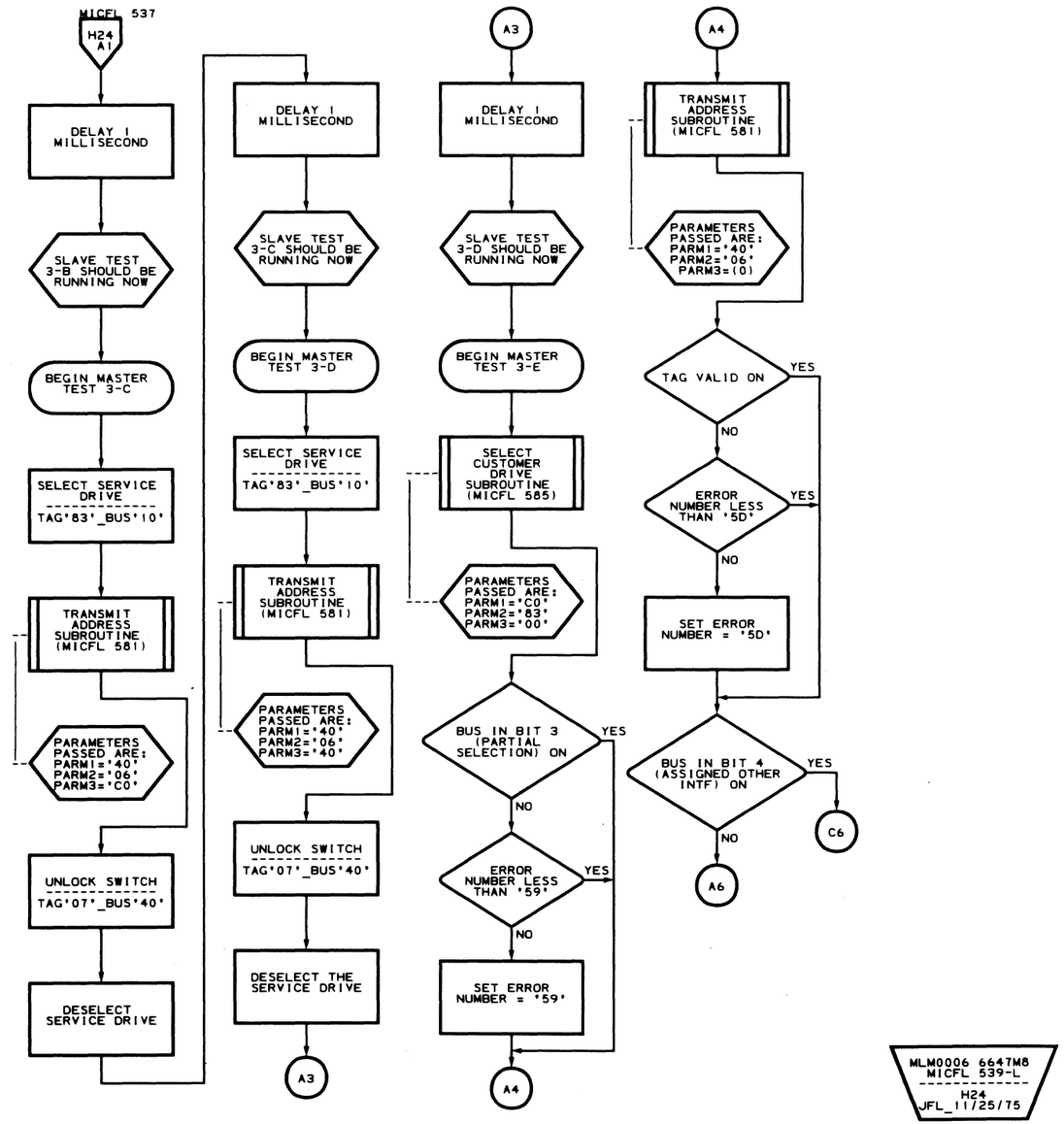
ROUTINE B6 – STRING SWITCH TESTS



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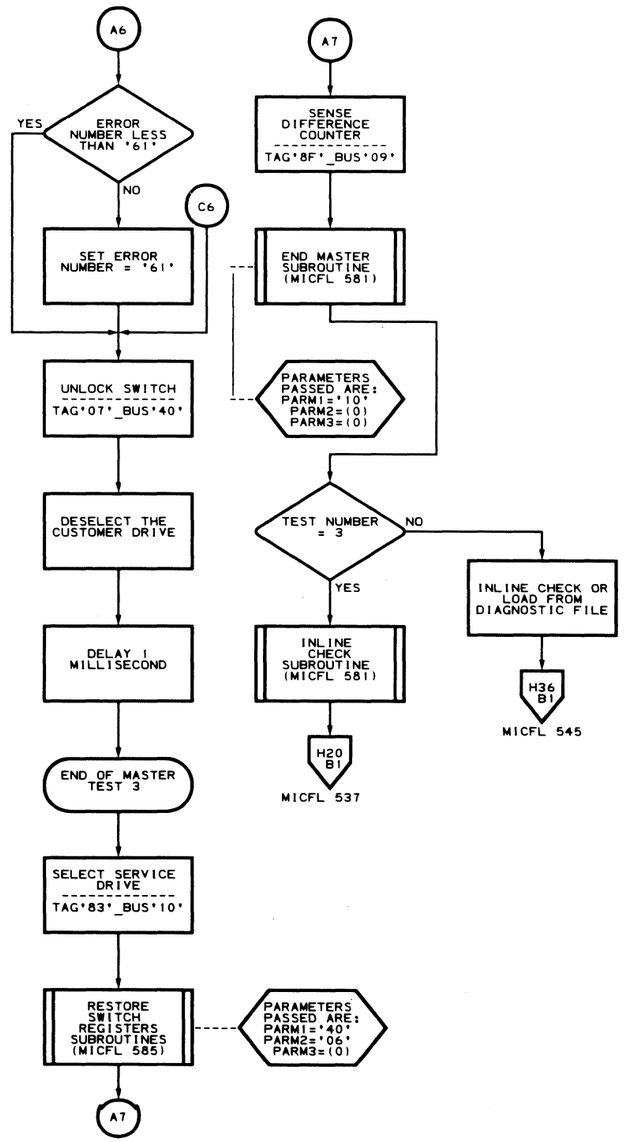

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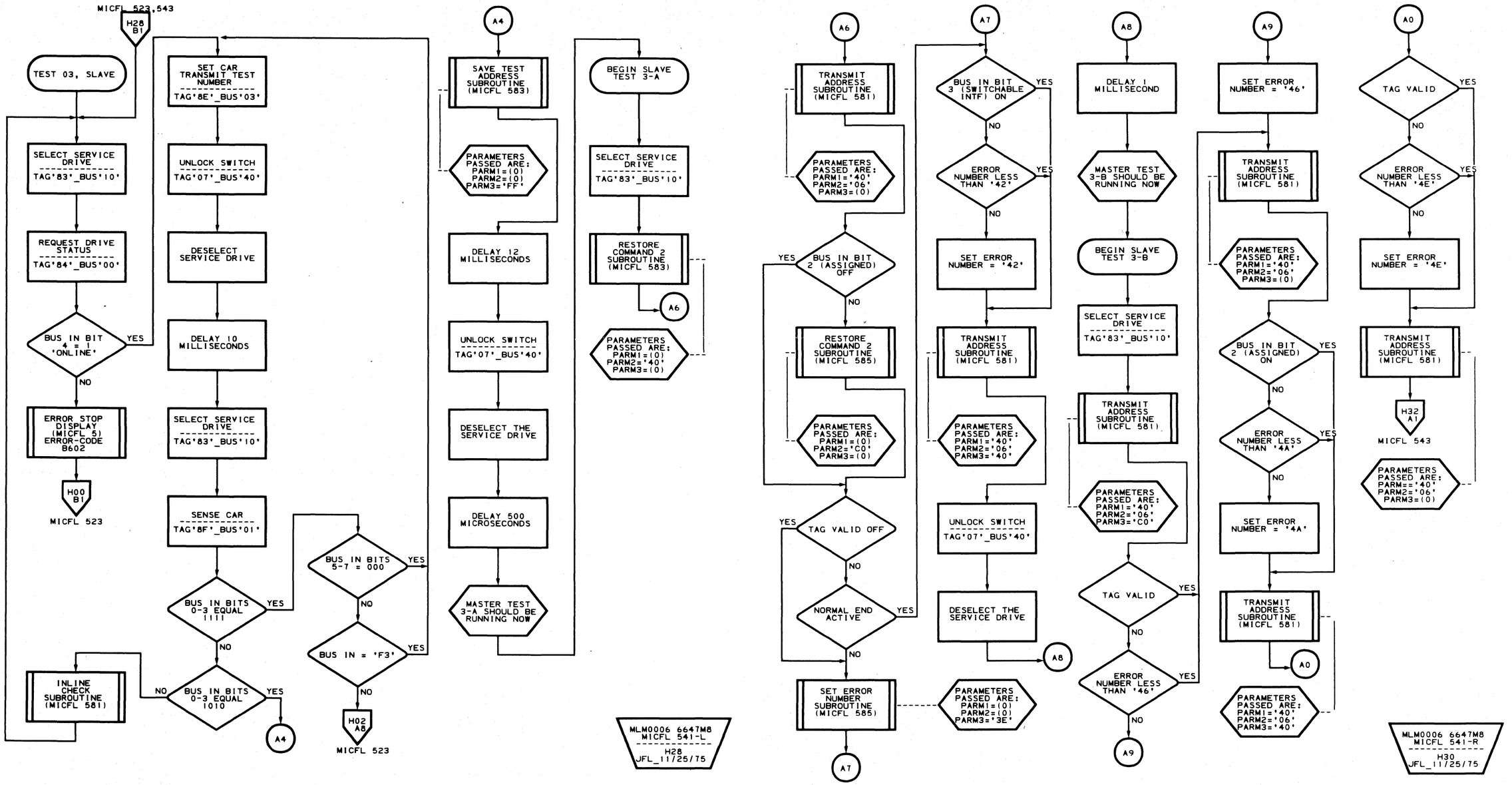
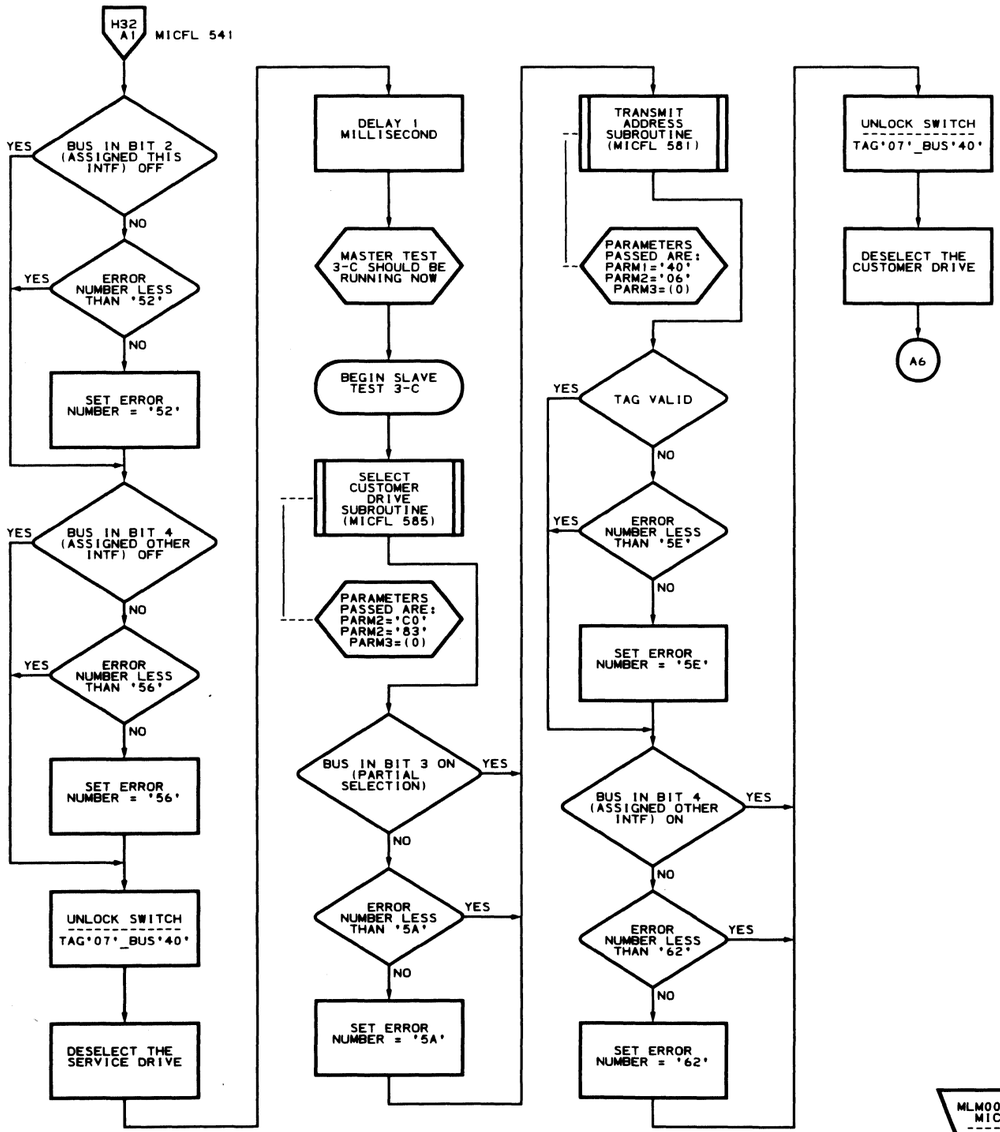
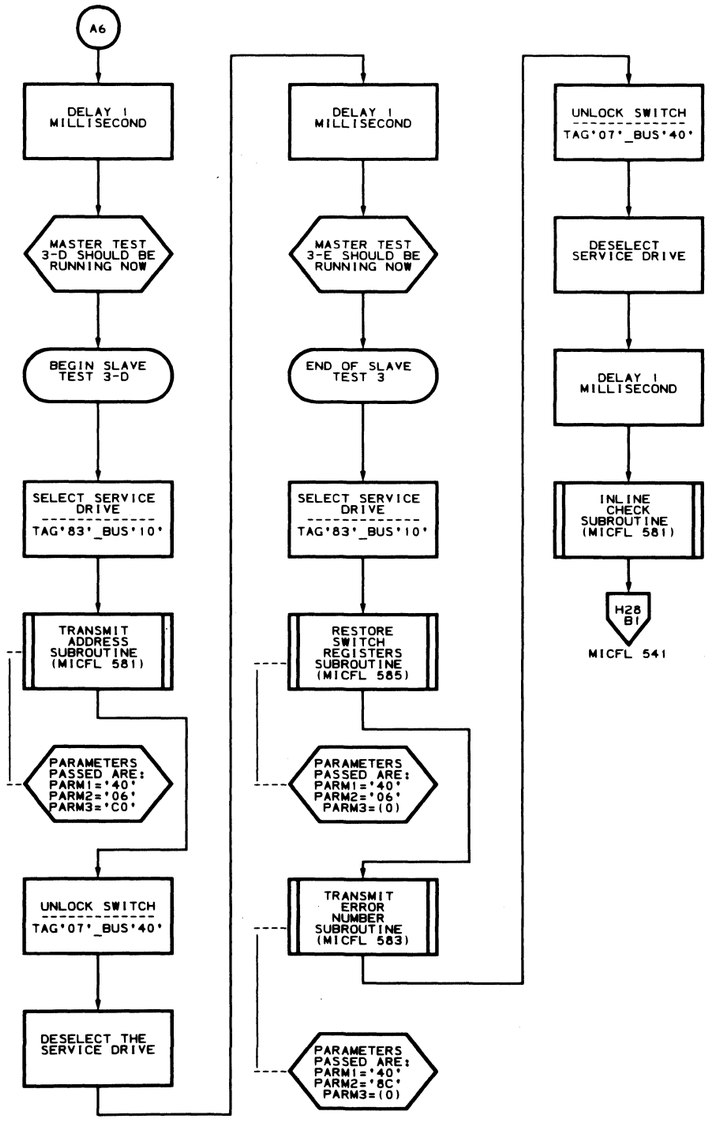


ROUTINE B6 – STRING SWITCH TESTS





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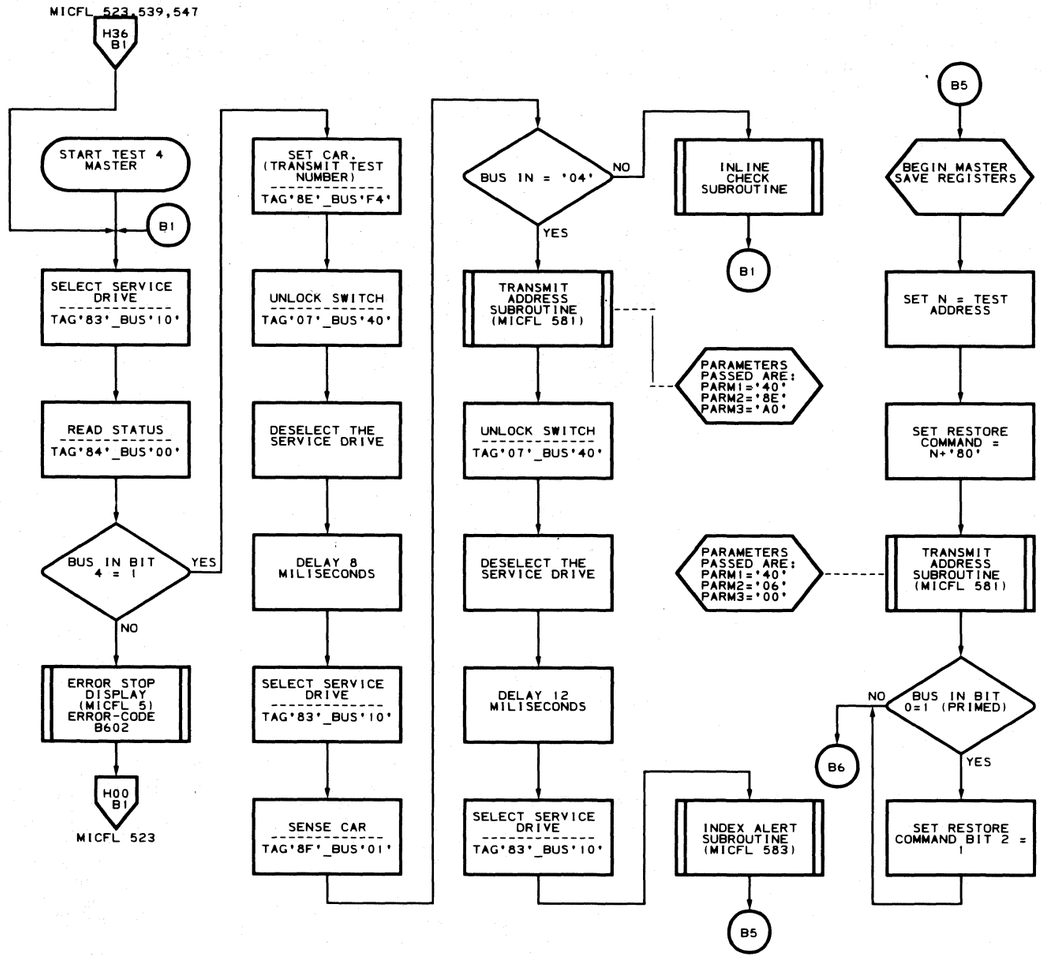

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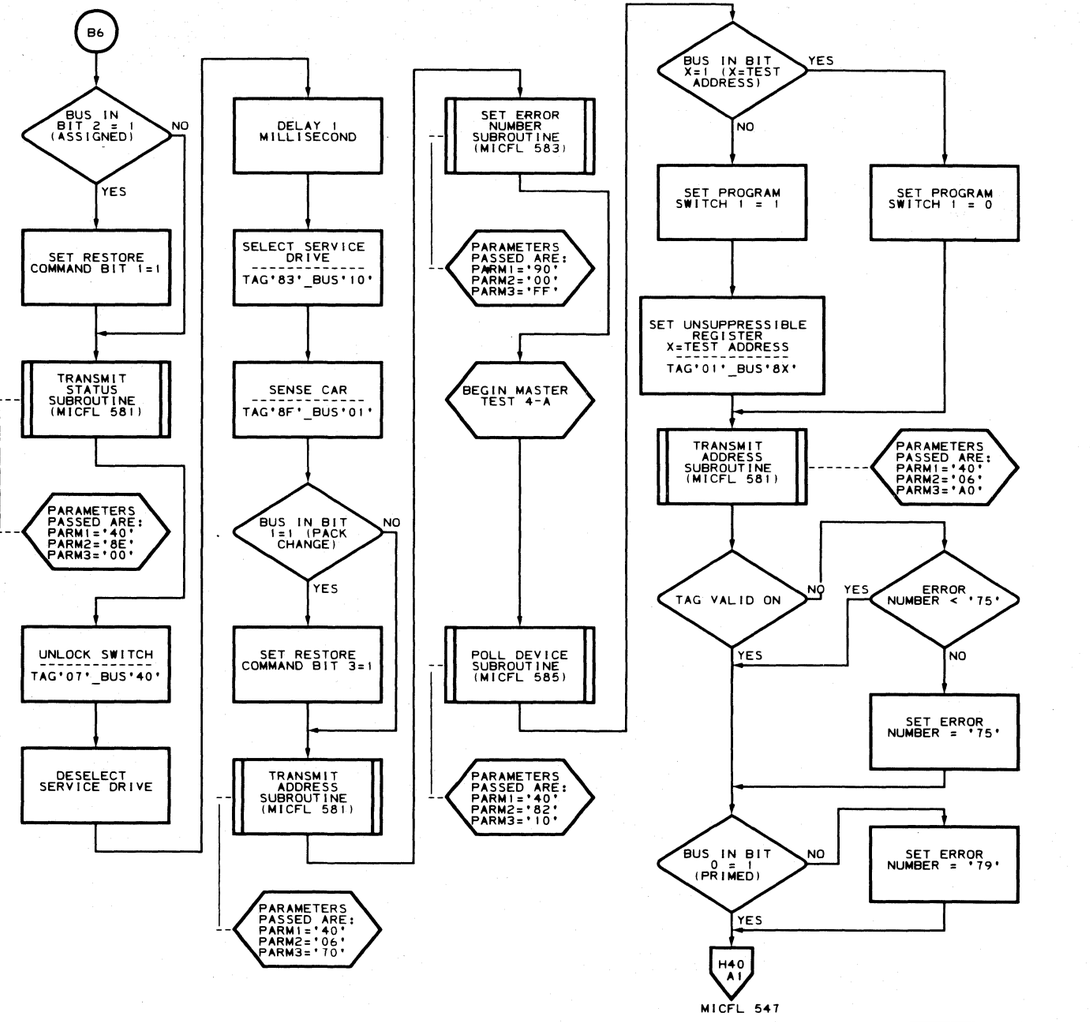

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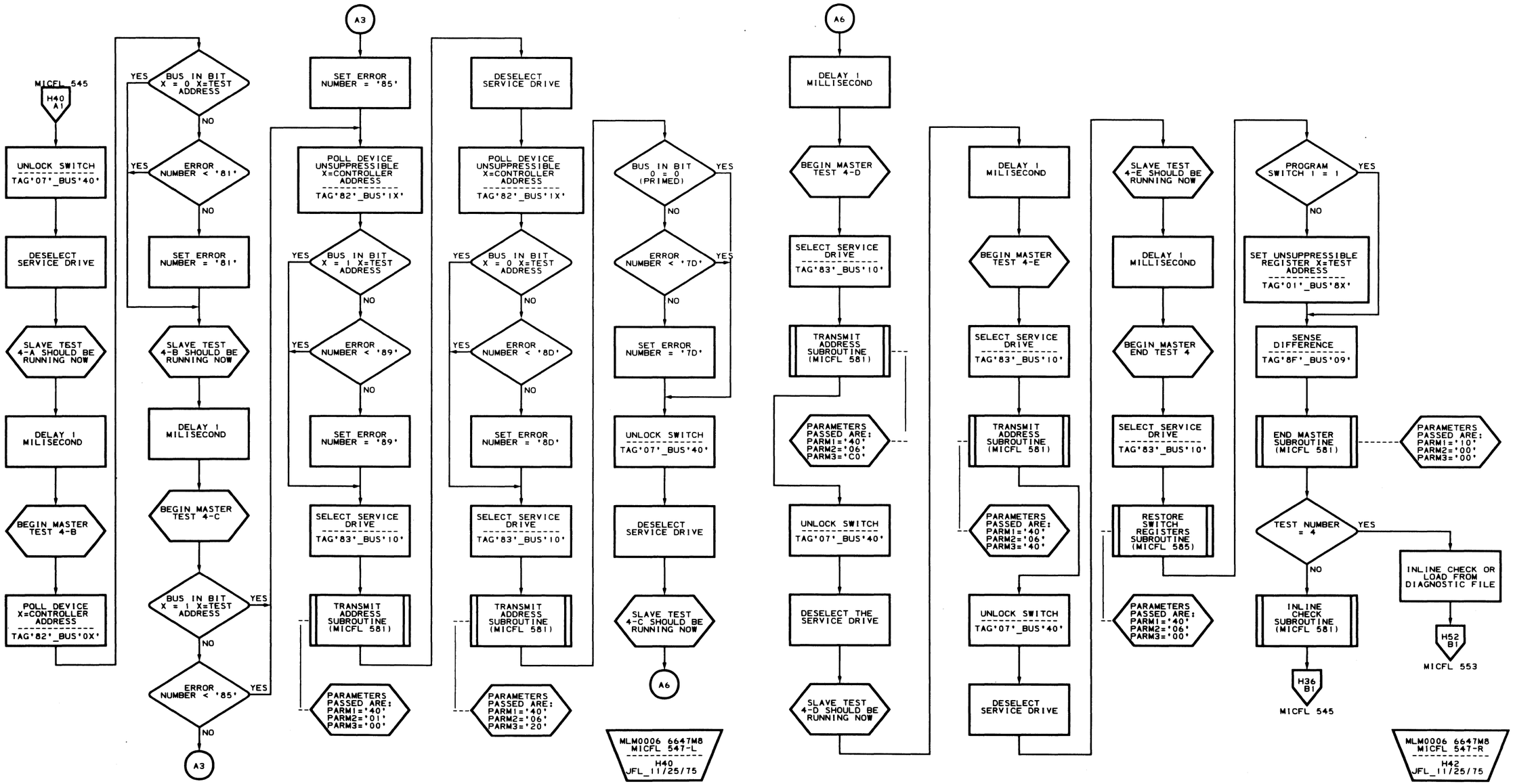
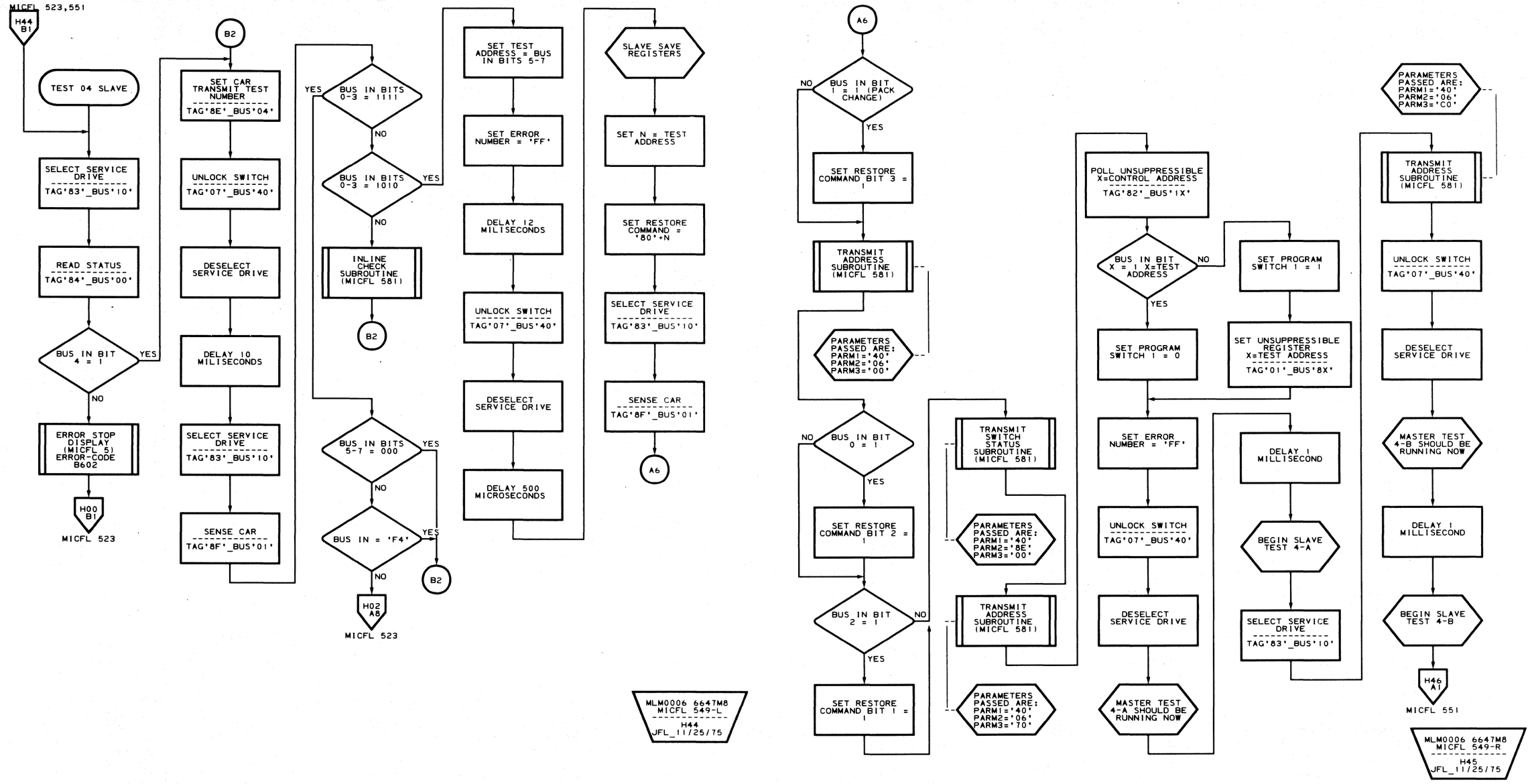
JFL_11/25/75

ROUTINE B6 – STRING SWITCH TESTS

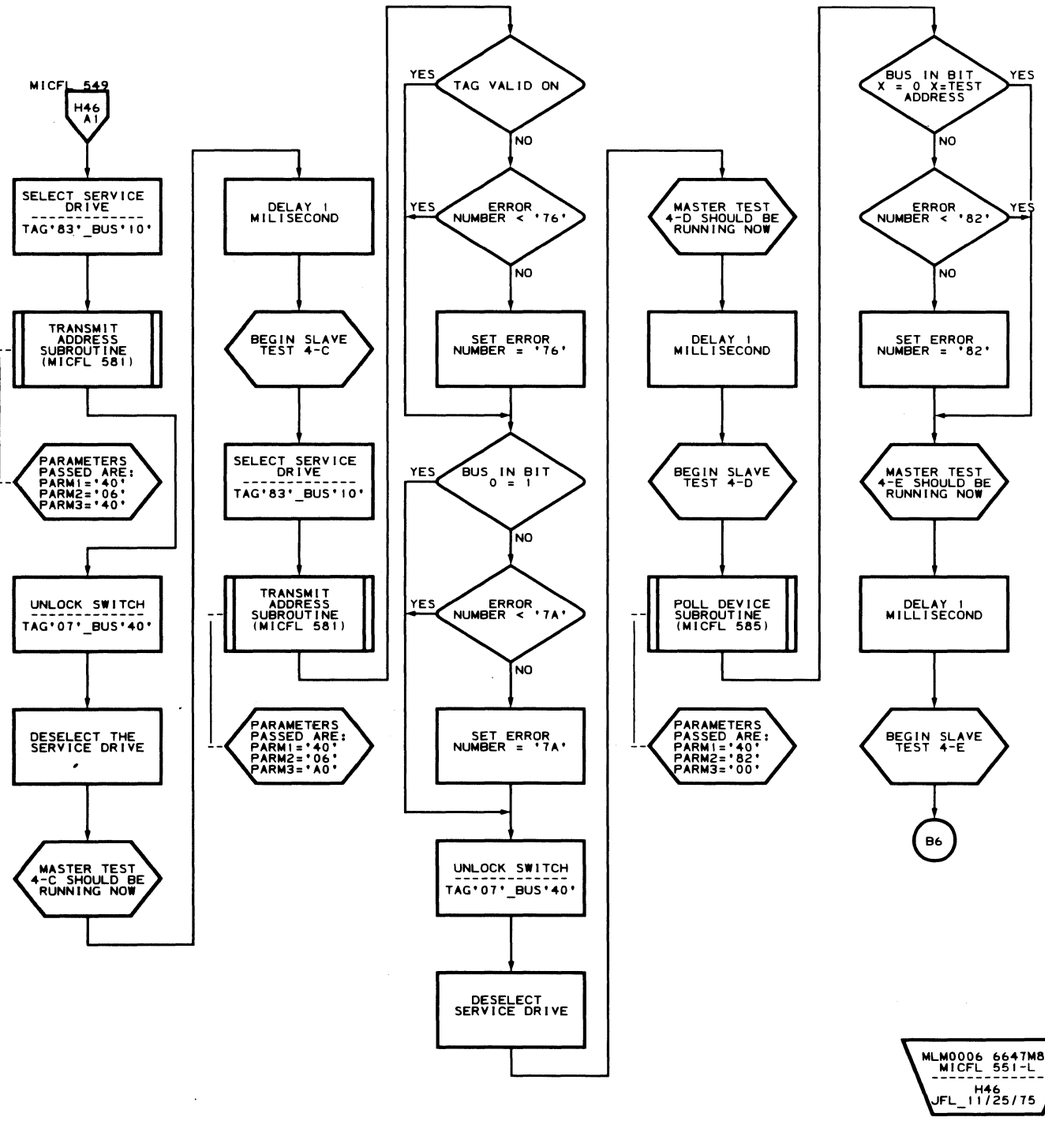


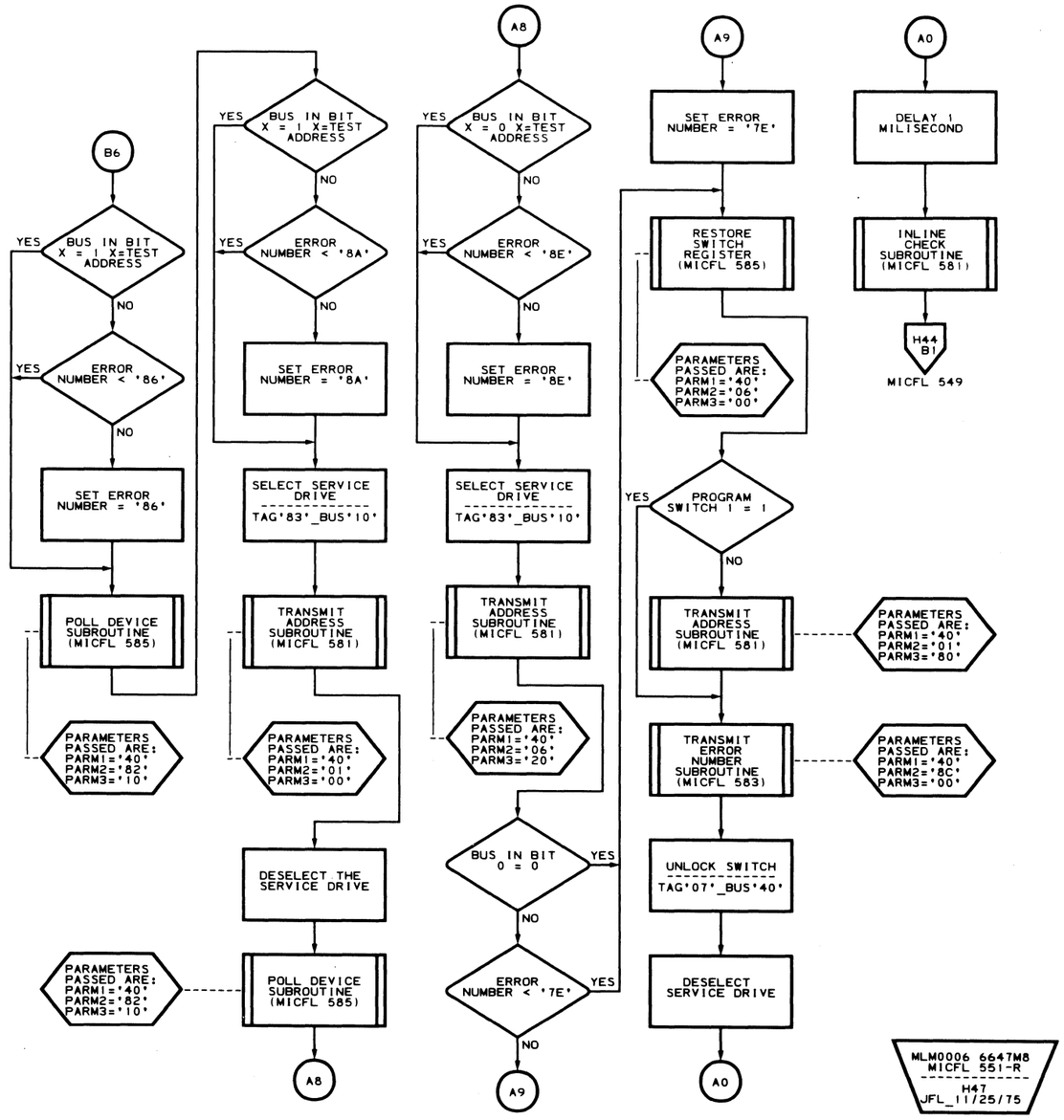
GC0547 Seq. 1 of 2	2358444 Part No.

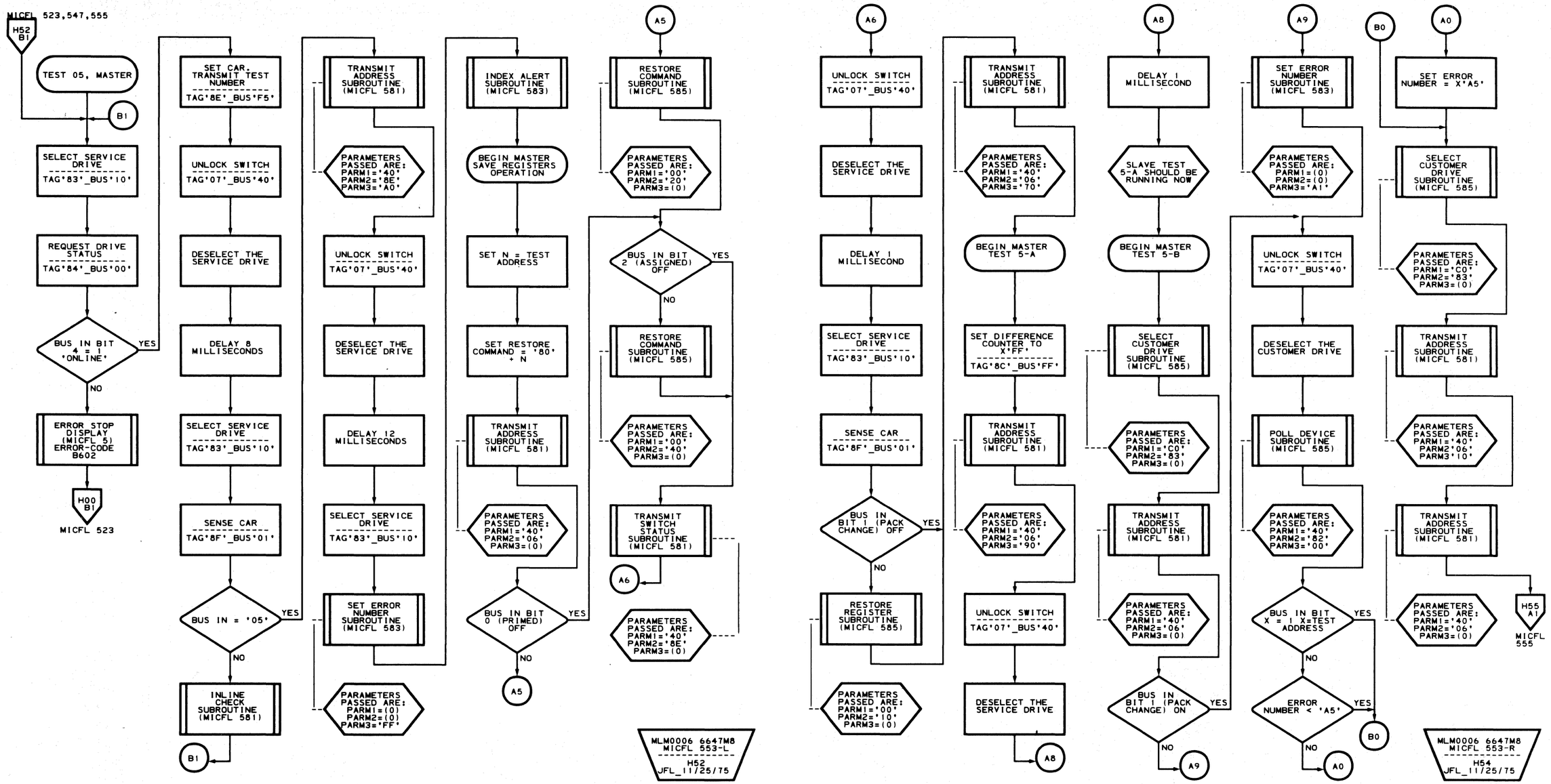
441300 31 Mar 76				



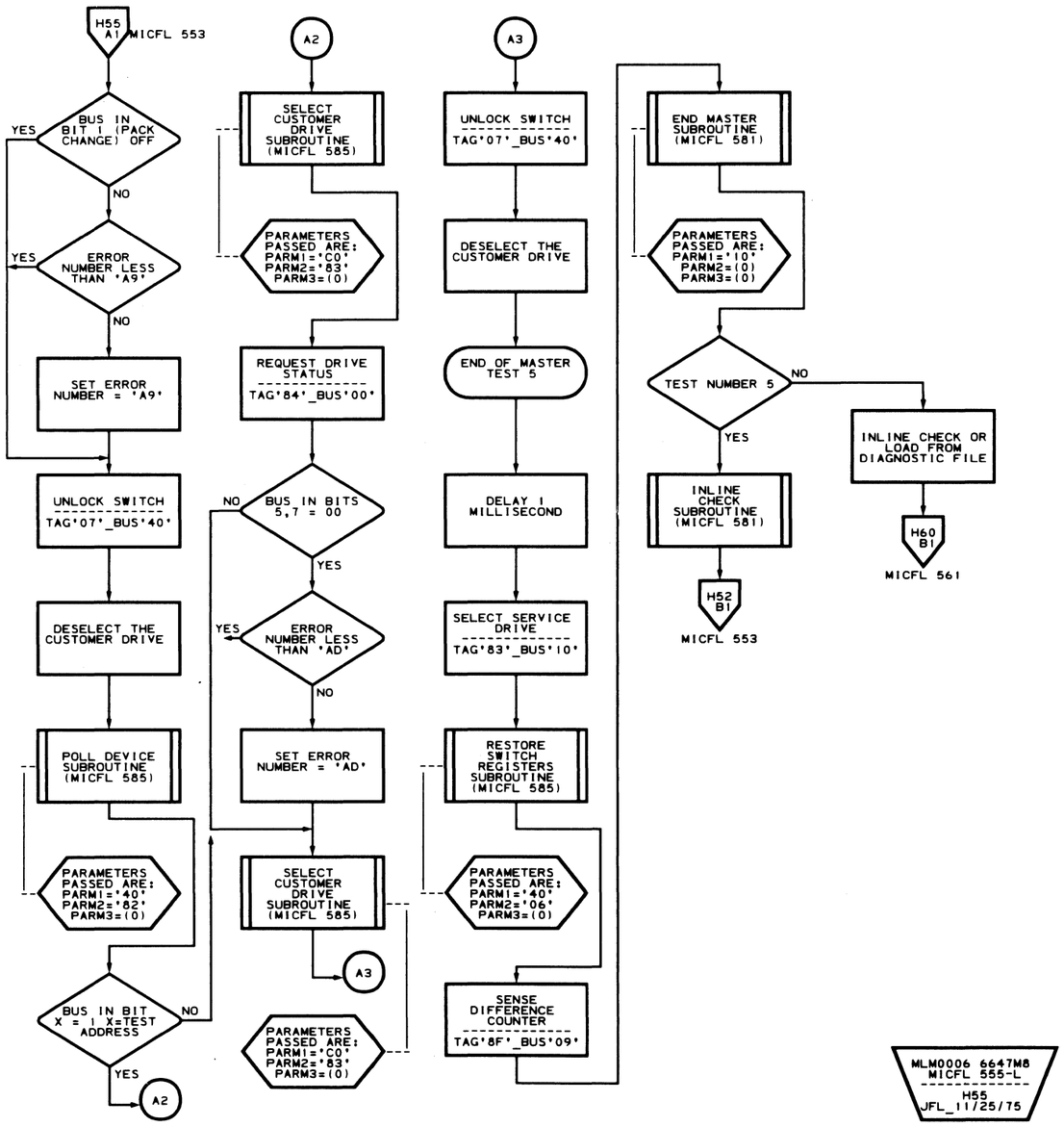
ROUTINE B6 – STRING SWITCH TESTS

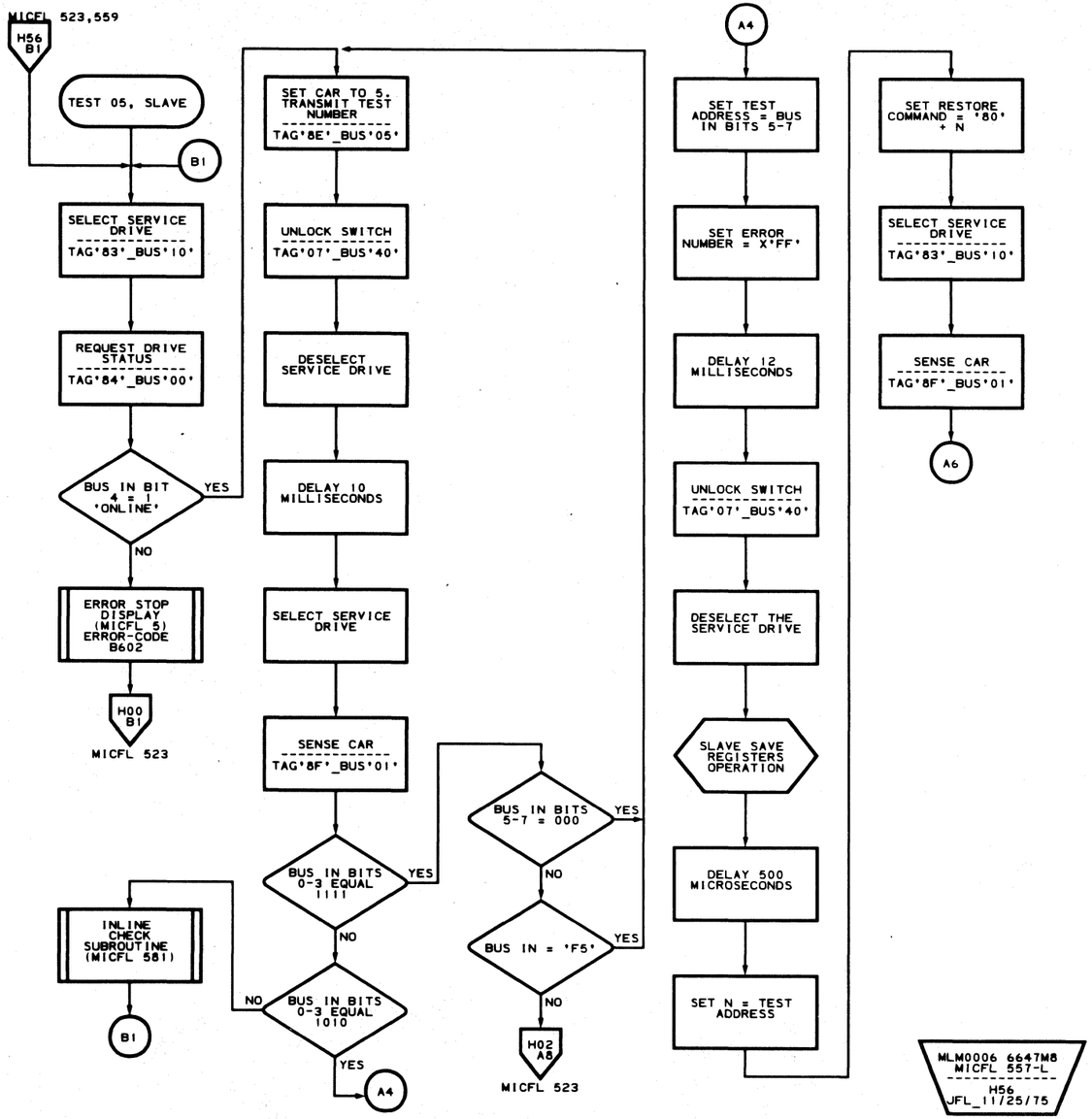


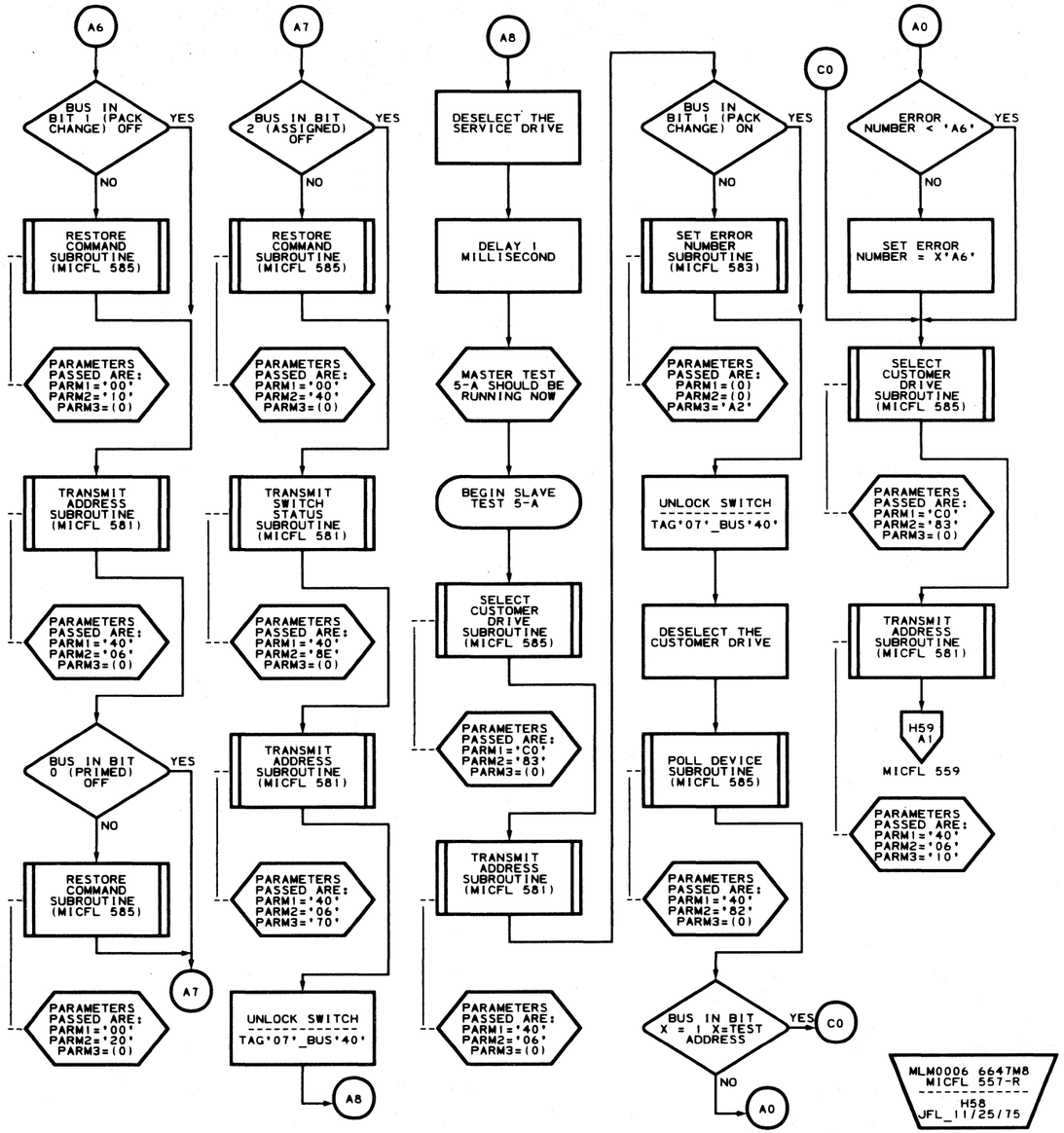




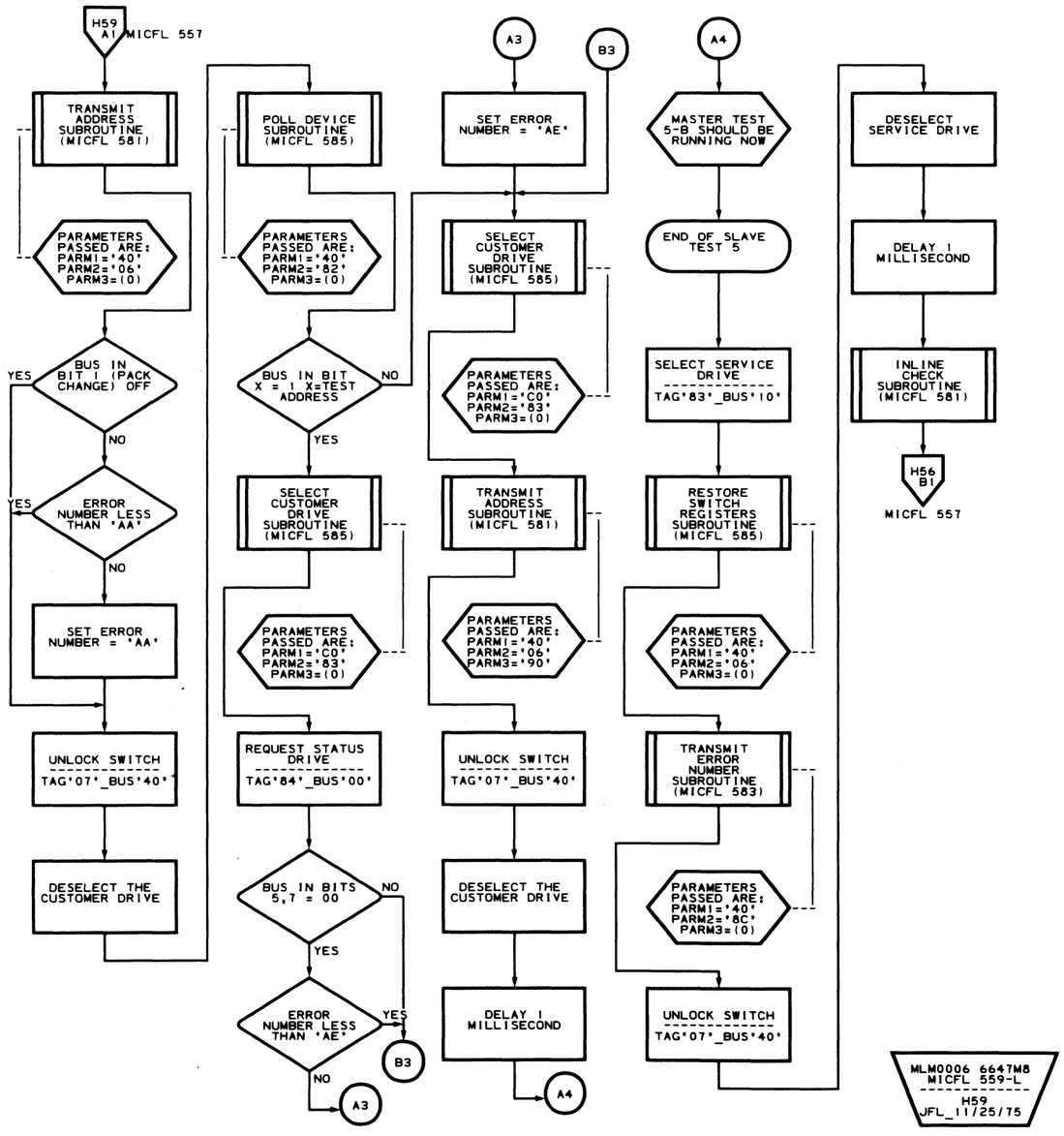
ROUTINE B6 – STRING SWITCH TESTS

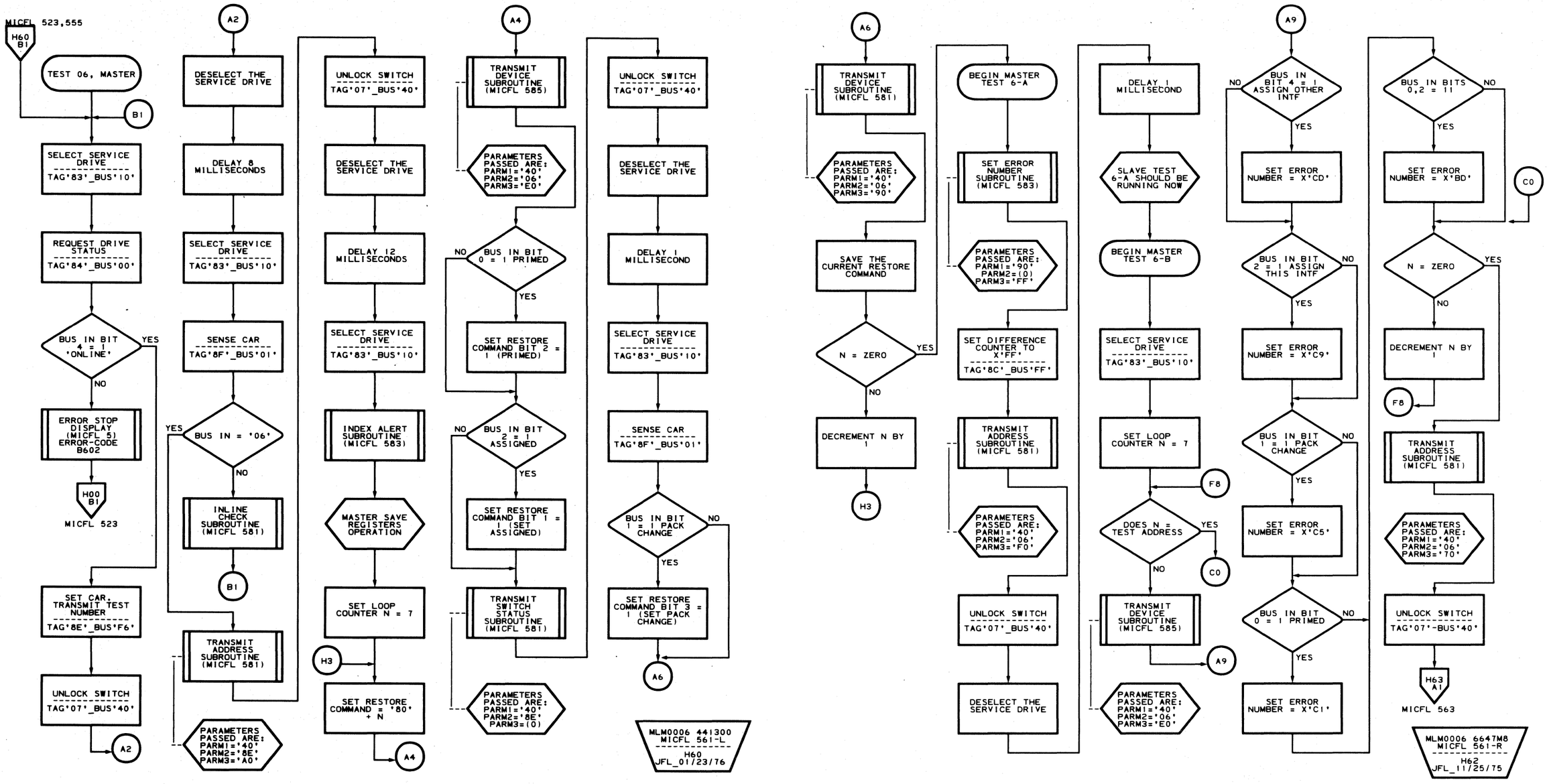






ROUTINE B6 – STRING SWITCH TESTS





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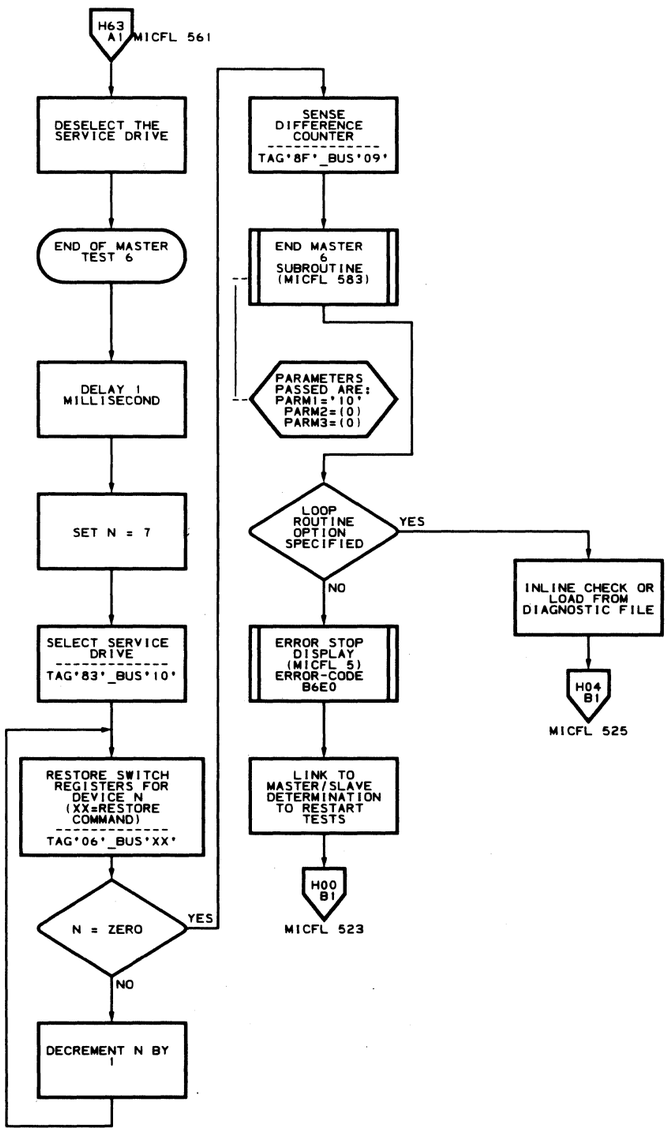

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H63
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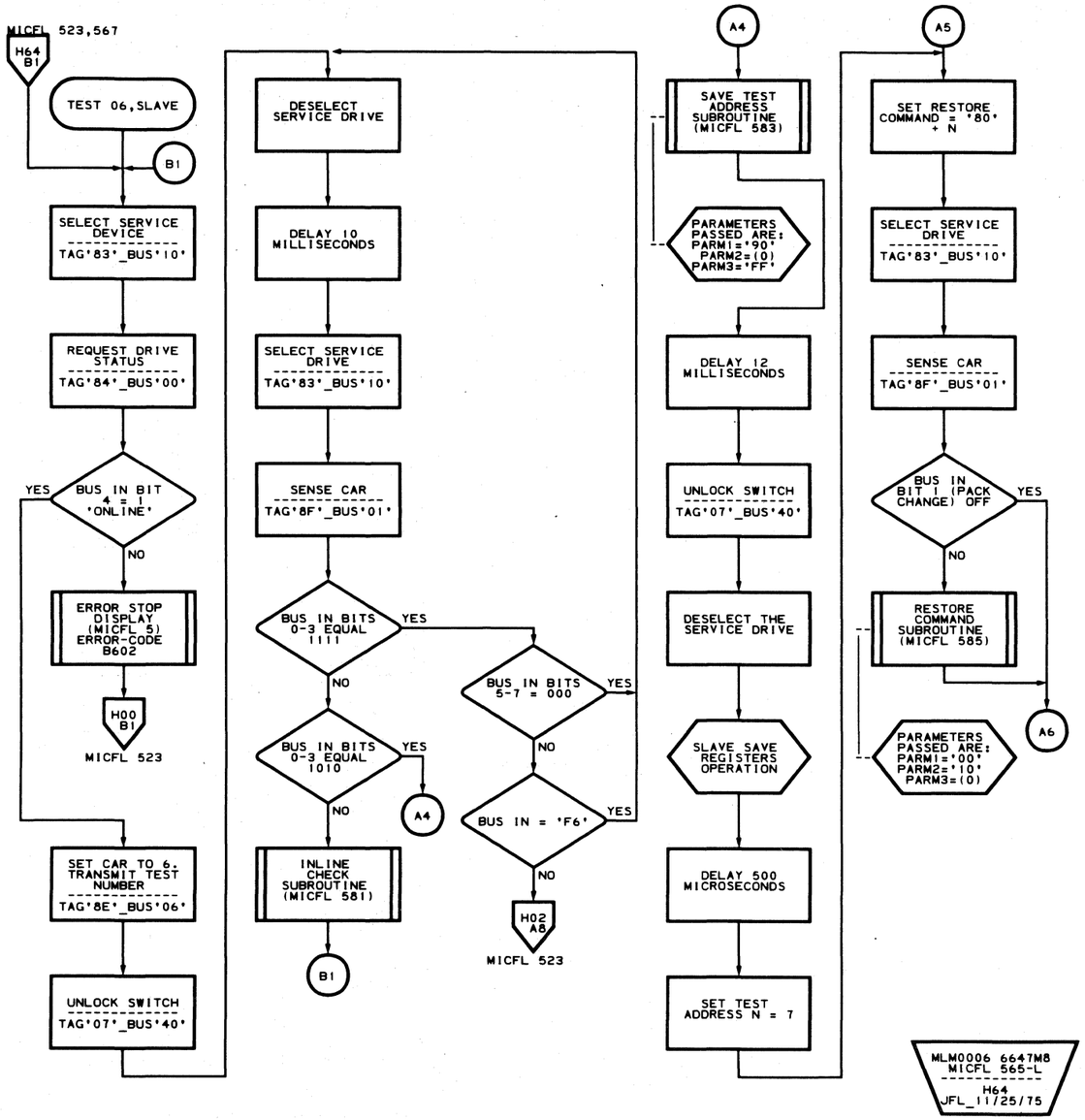

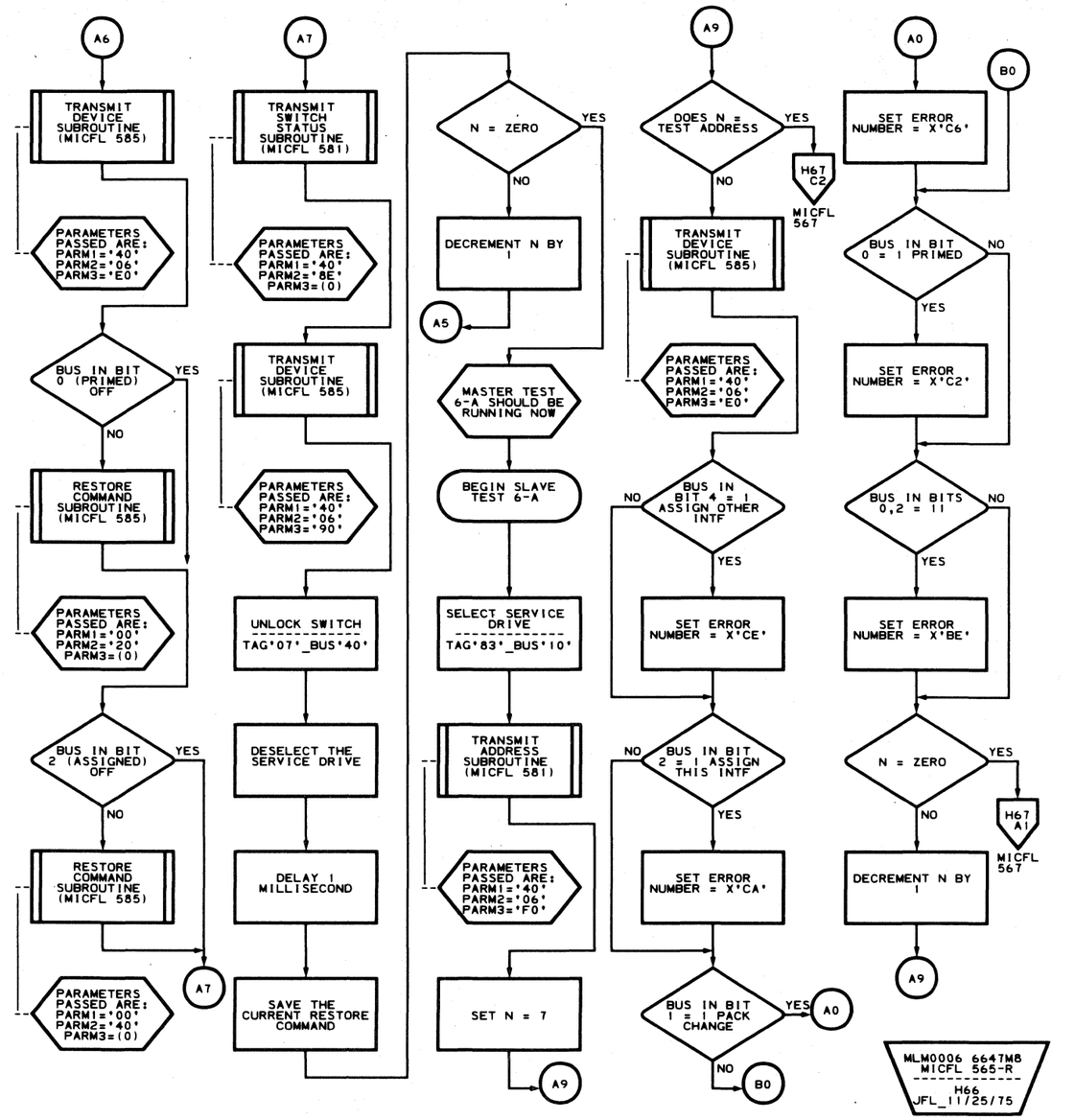

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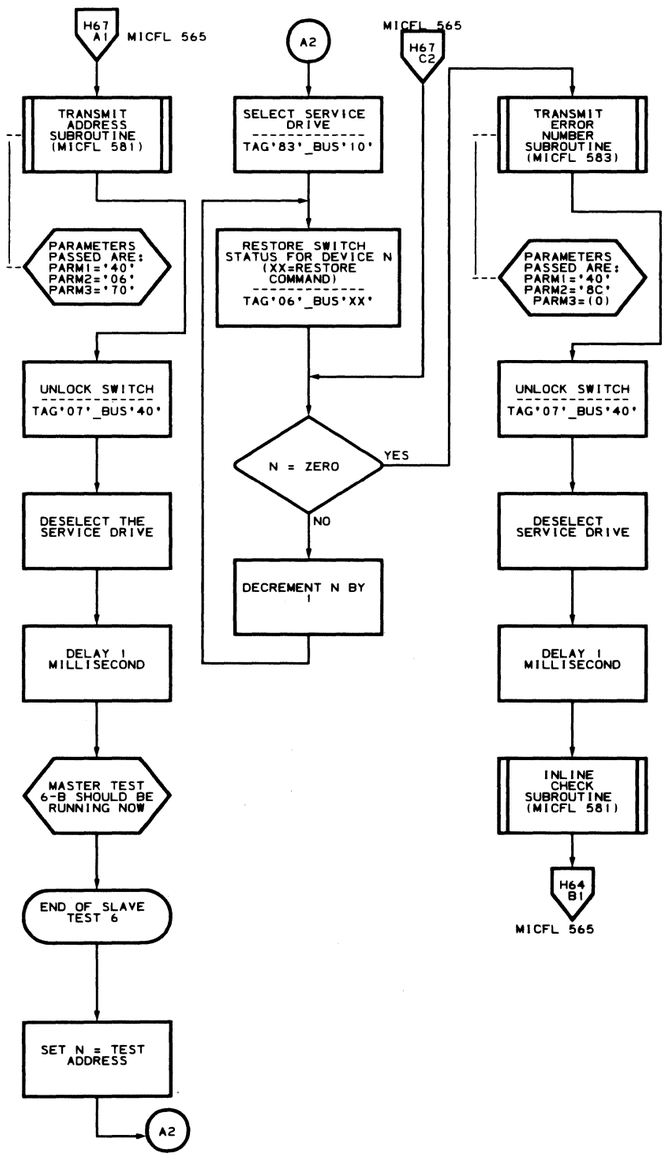

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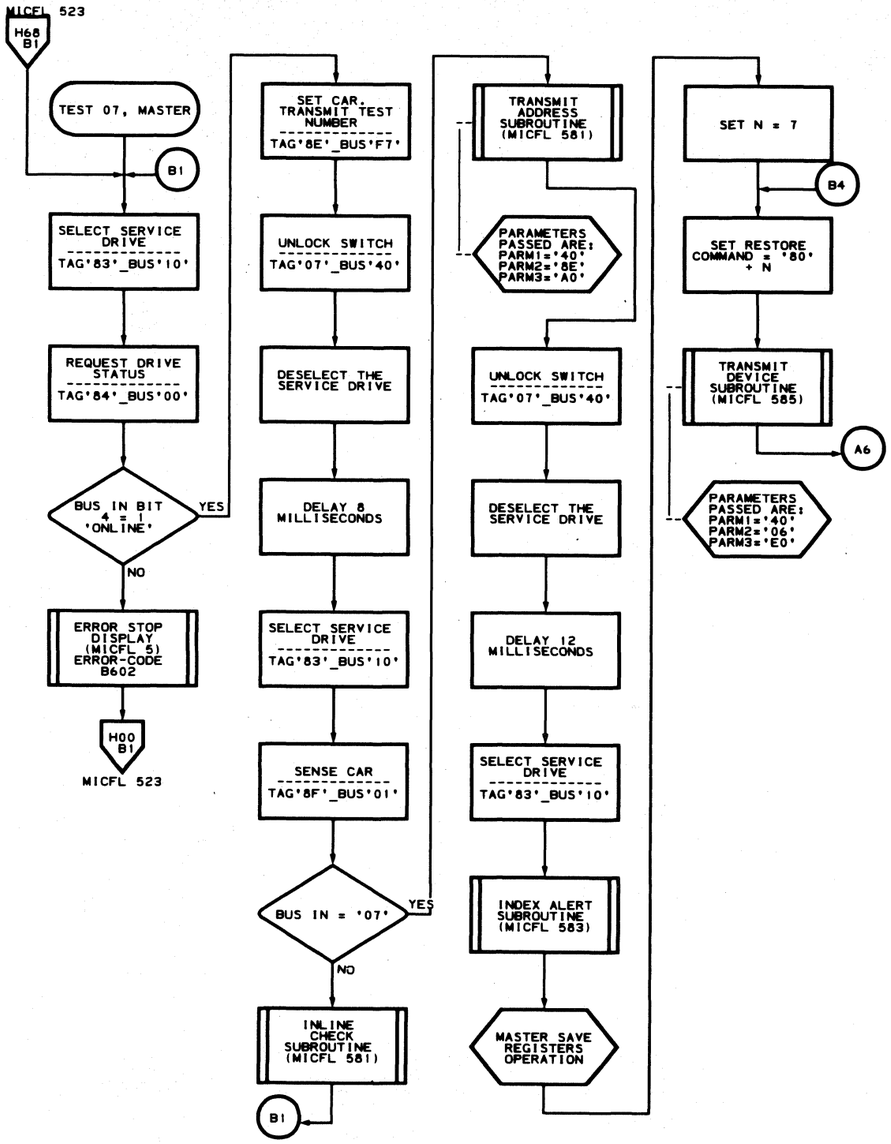

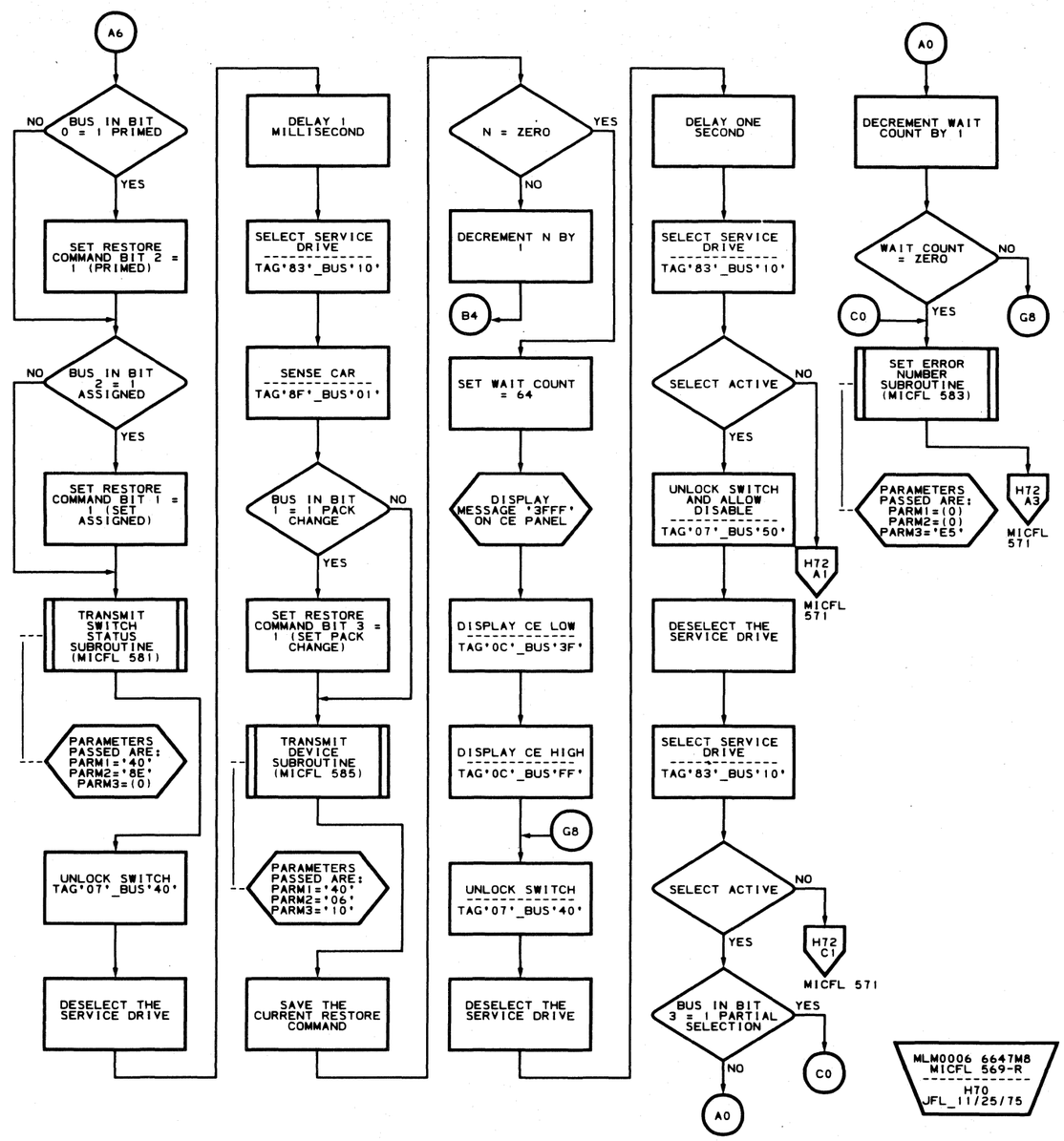

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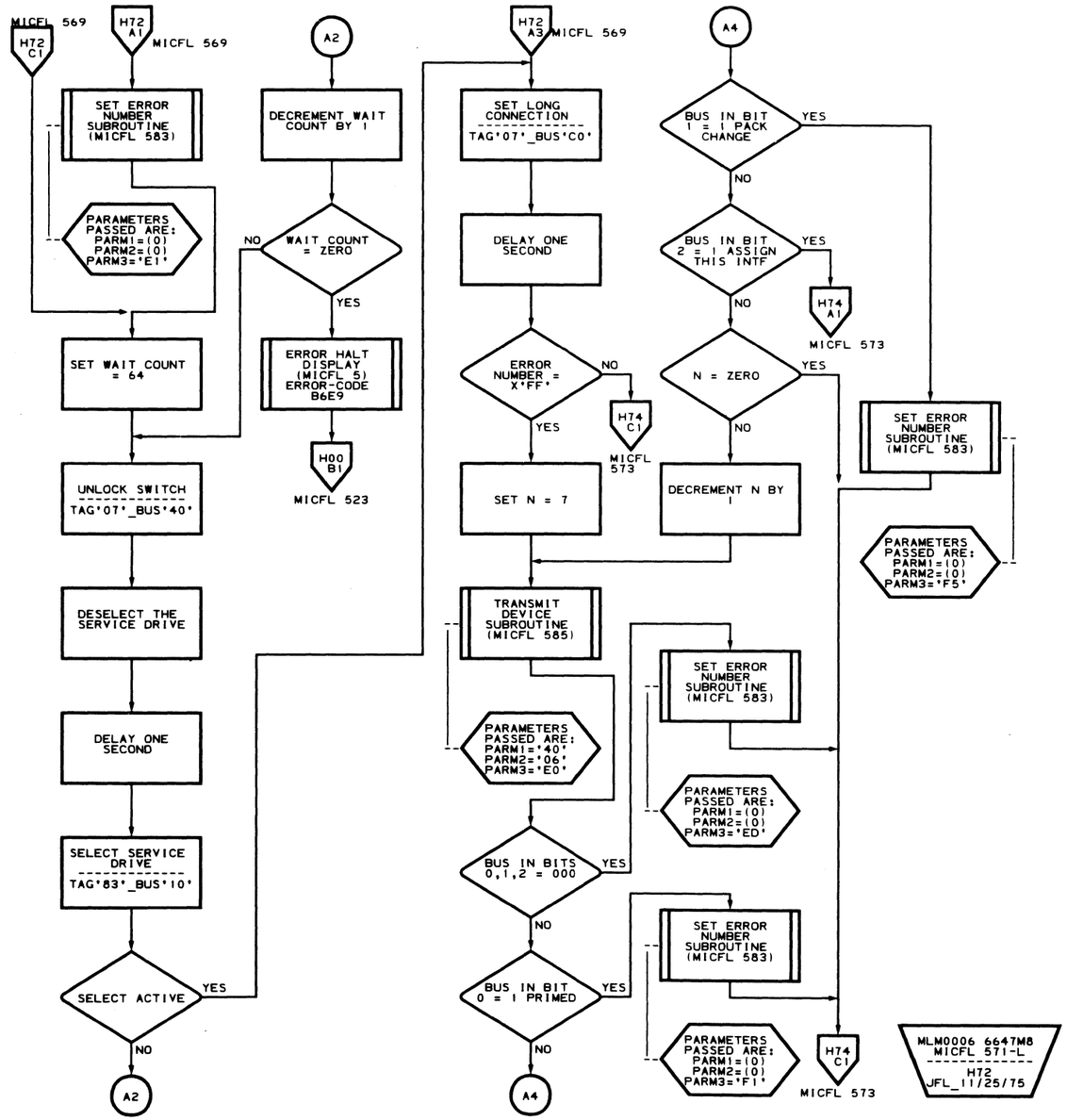
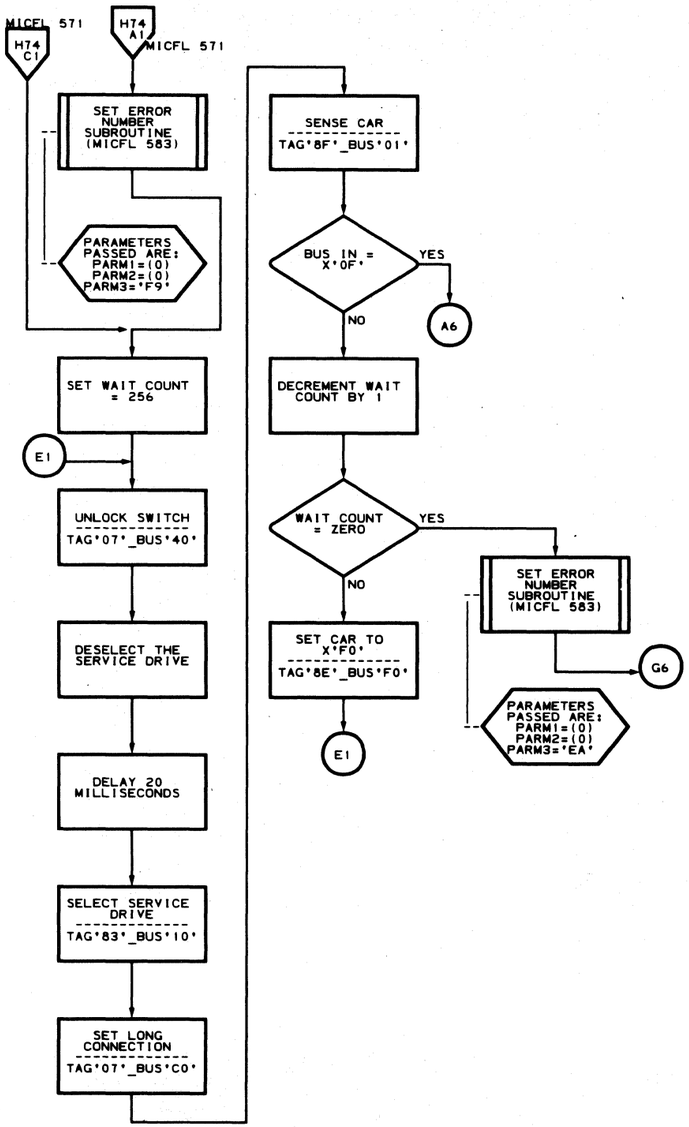
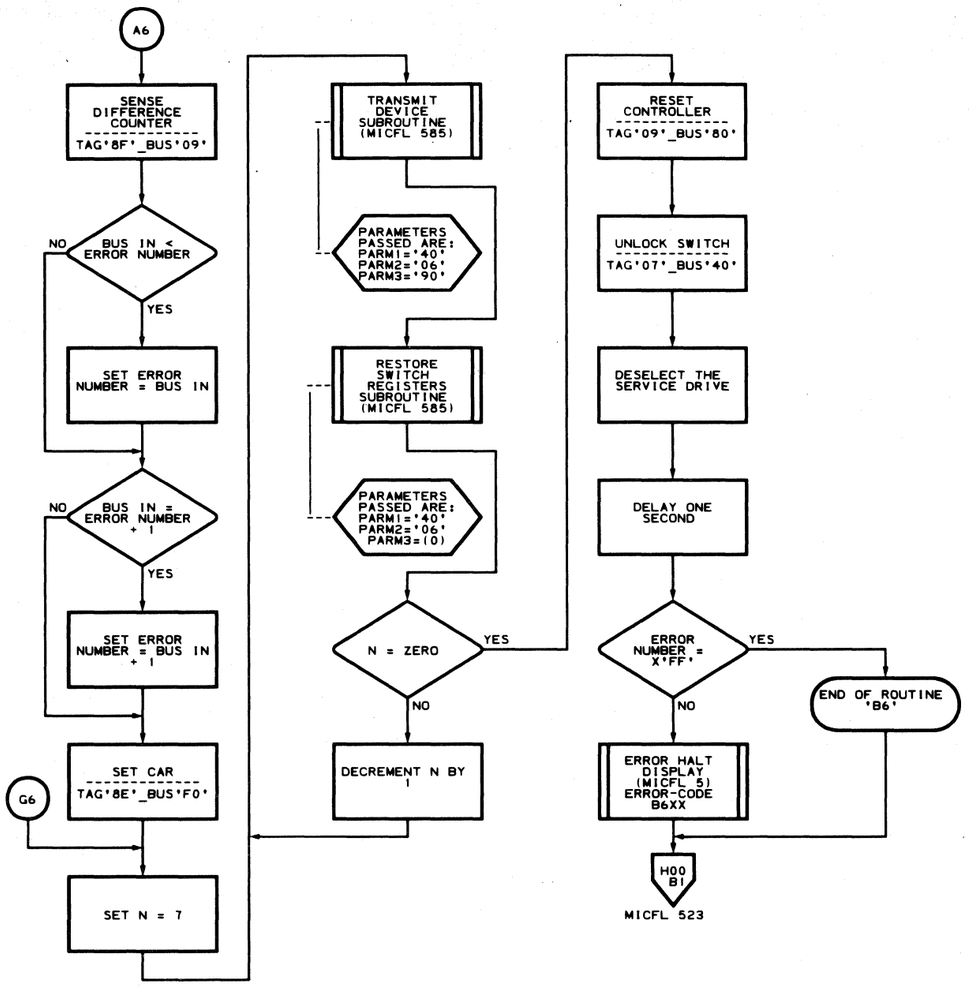
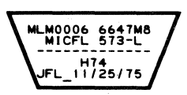
JFL_11/25/75

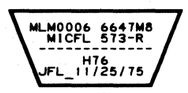
ROUTINE B6 – STRING SWITCH TESTS



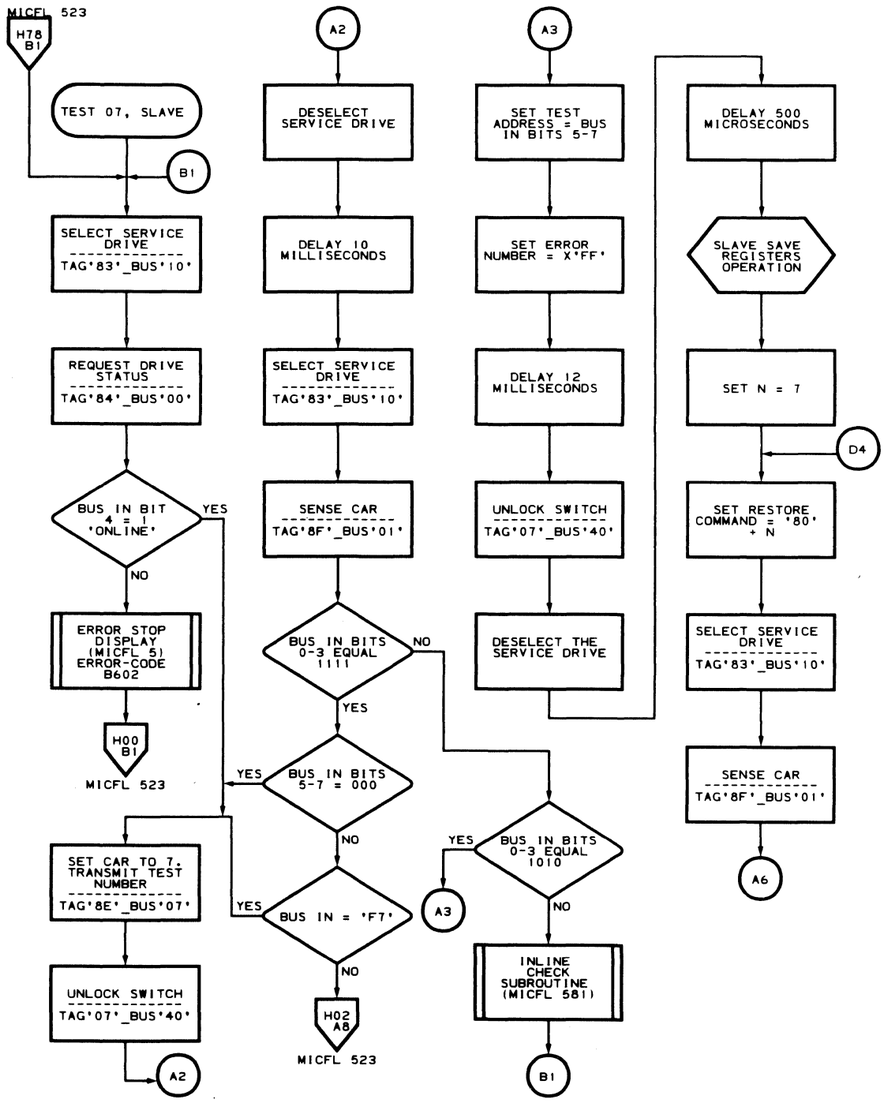


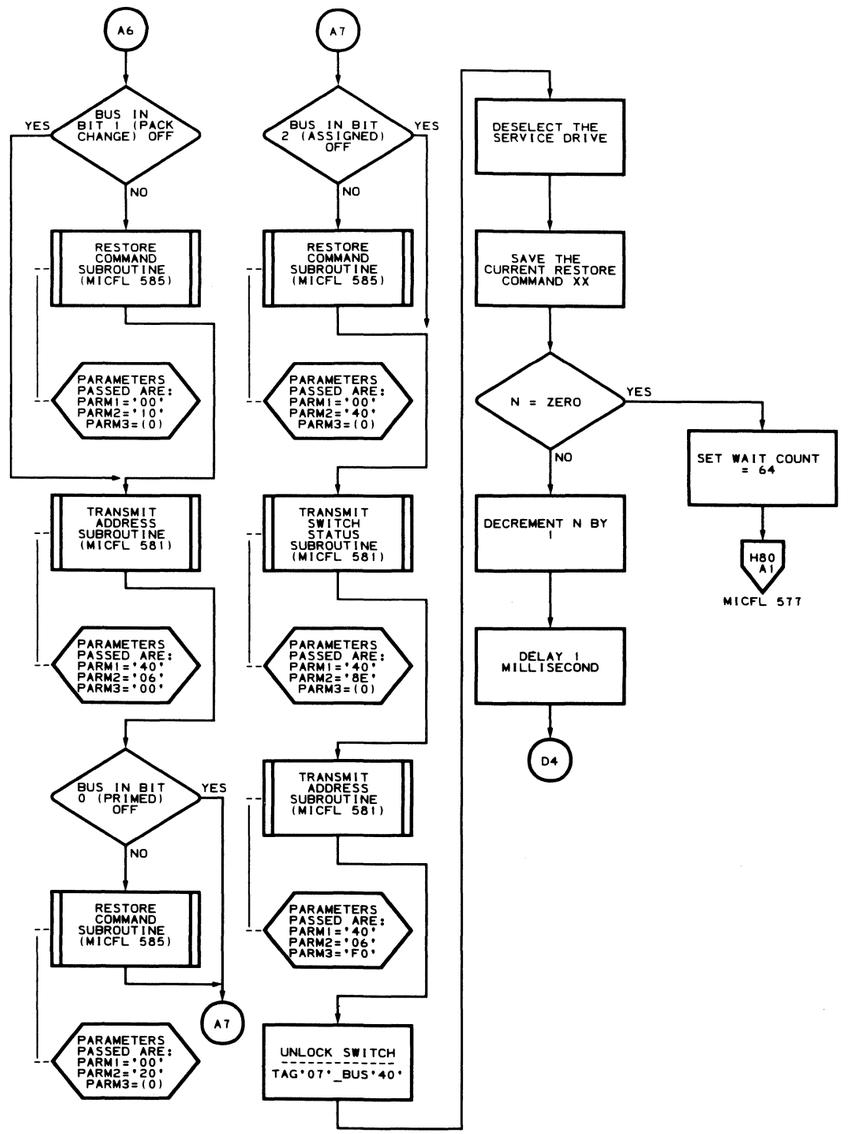






ROUTINE B6 – STRING SWITCH TESTS





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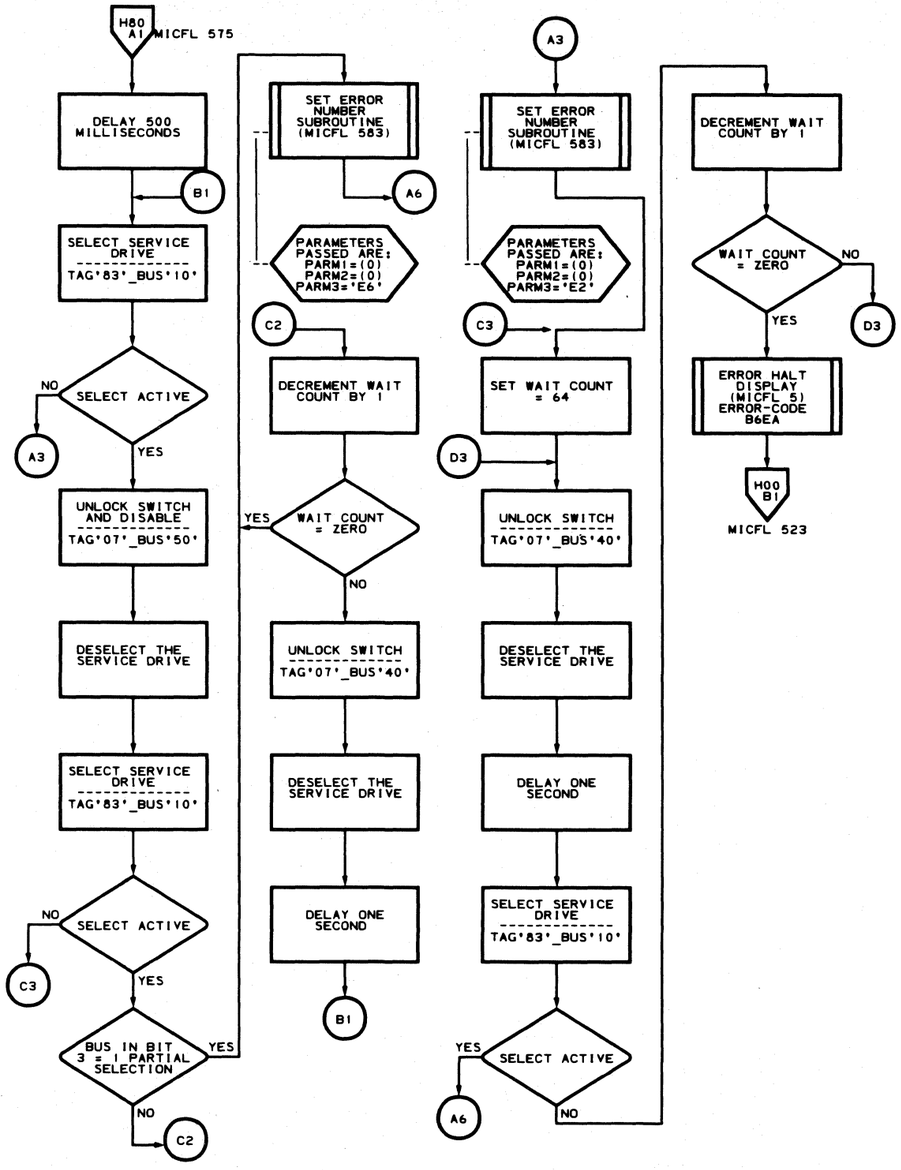
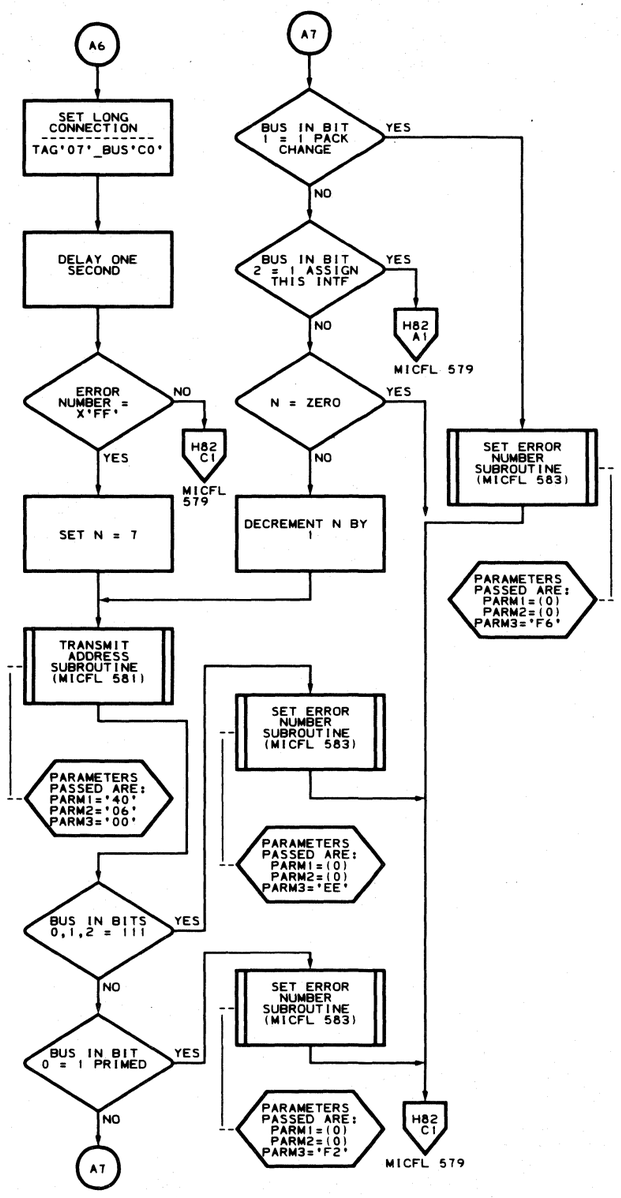
H79
JFL_12/01/75





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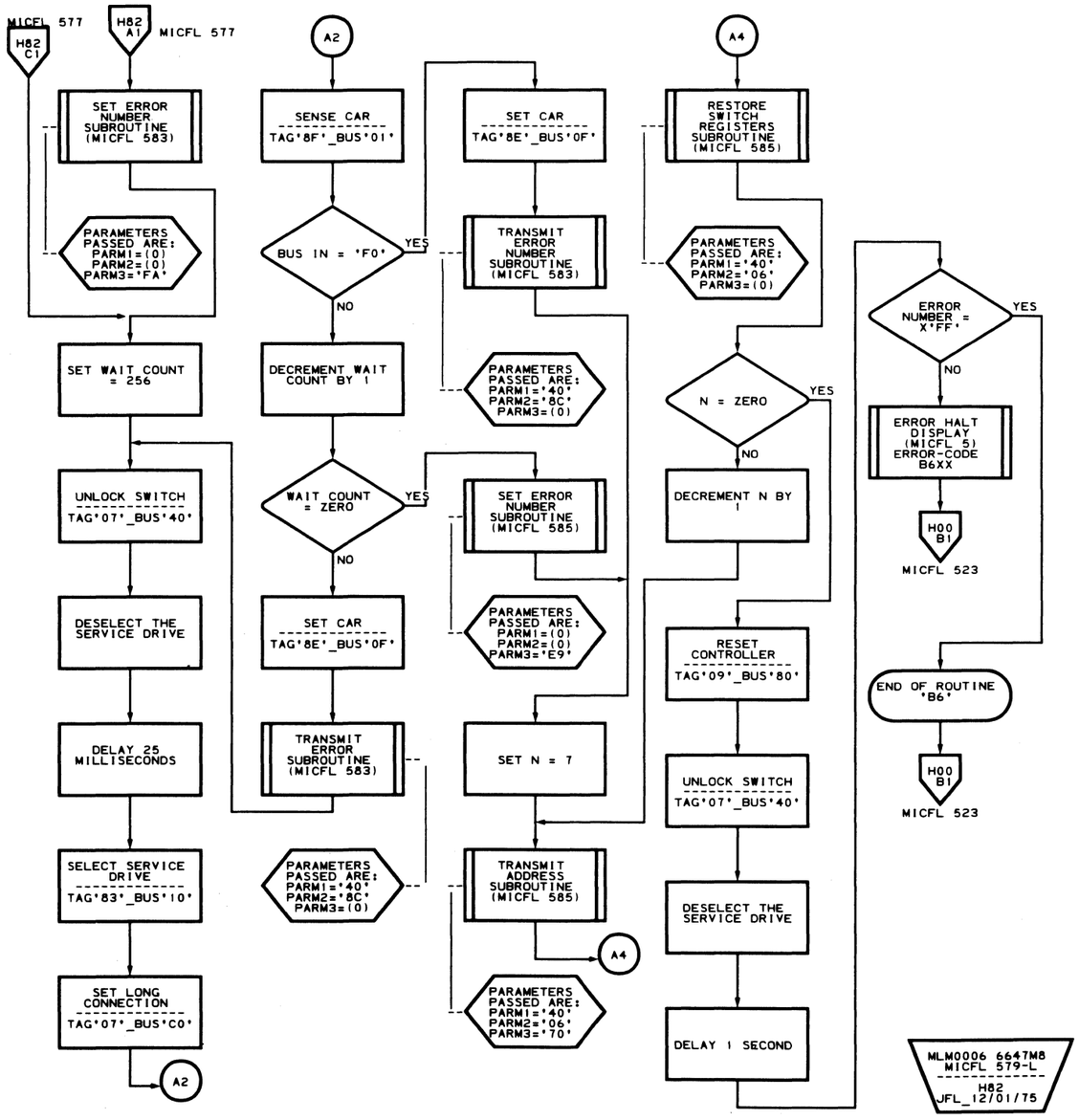
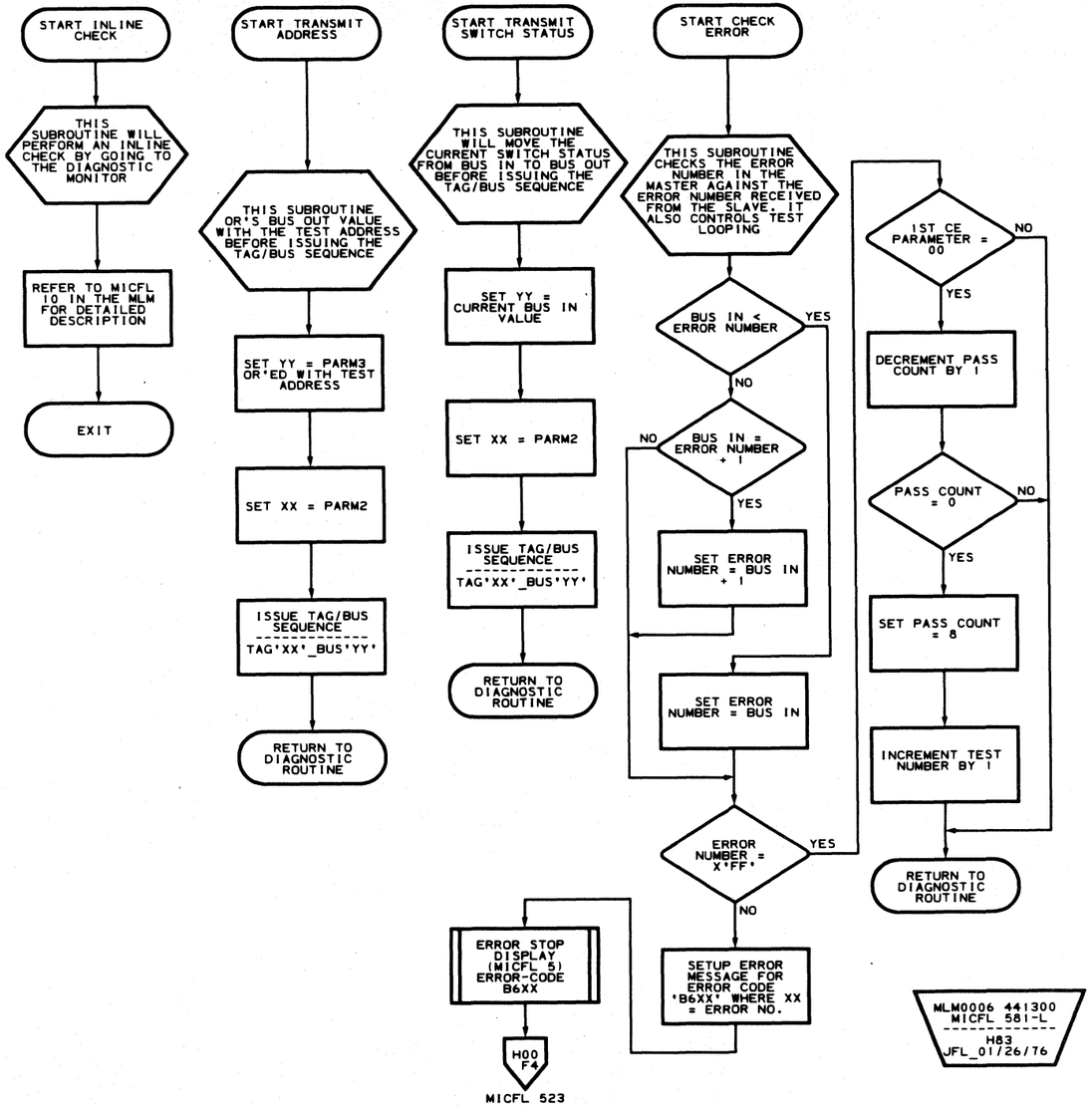
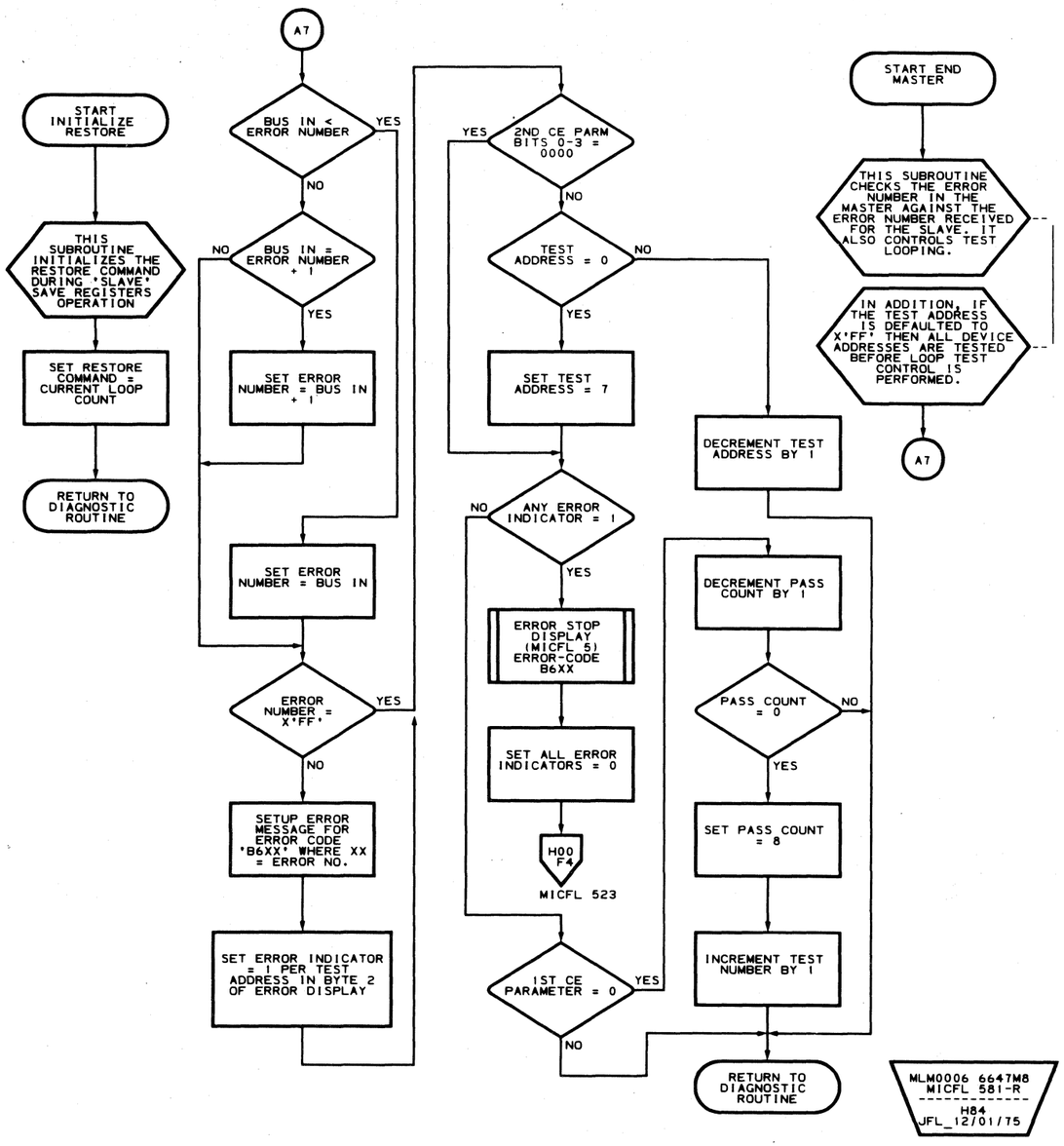
ROUTINE B6 – STRING SWITCH TESTS







GC0579 Seq. 2of 2	2358452 Part No.

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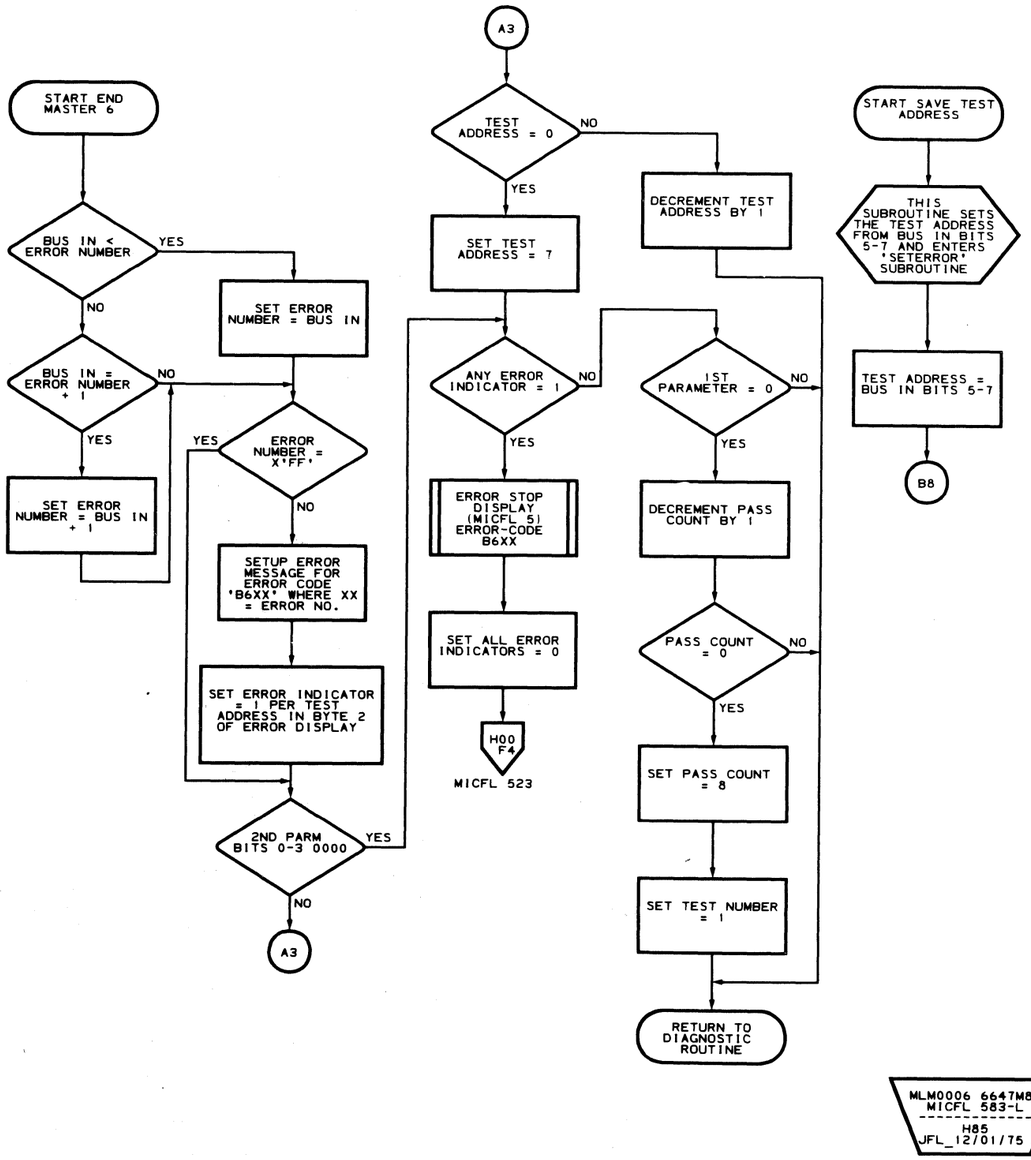
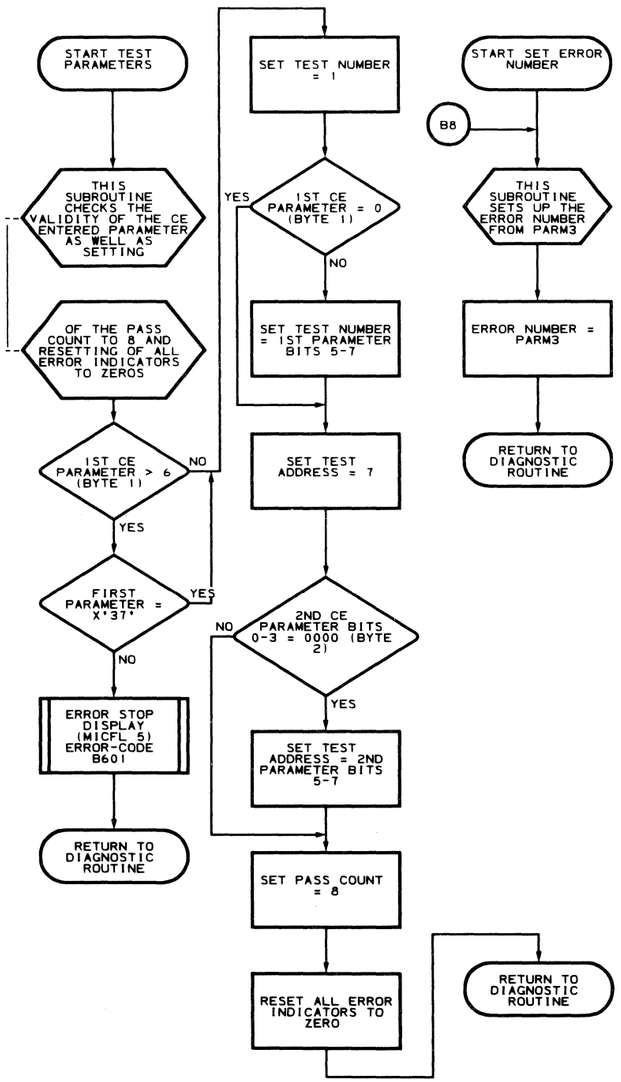
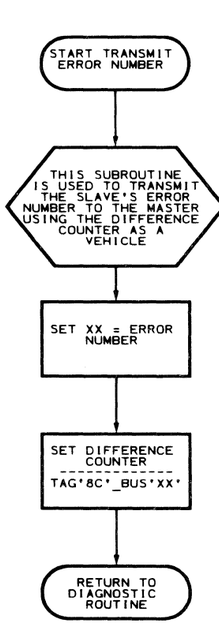
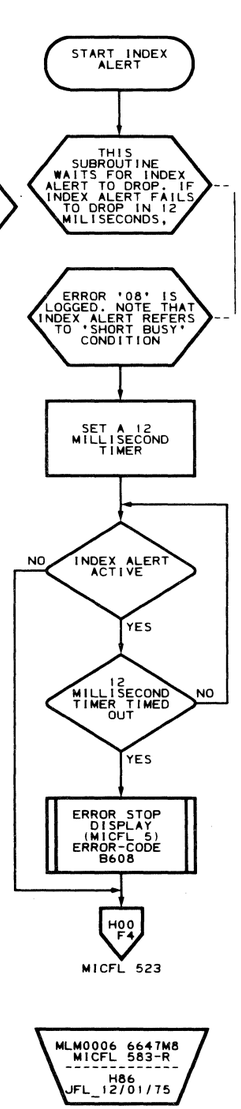
ROUTINE B6 – STRING SWITCH TESTS

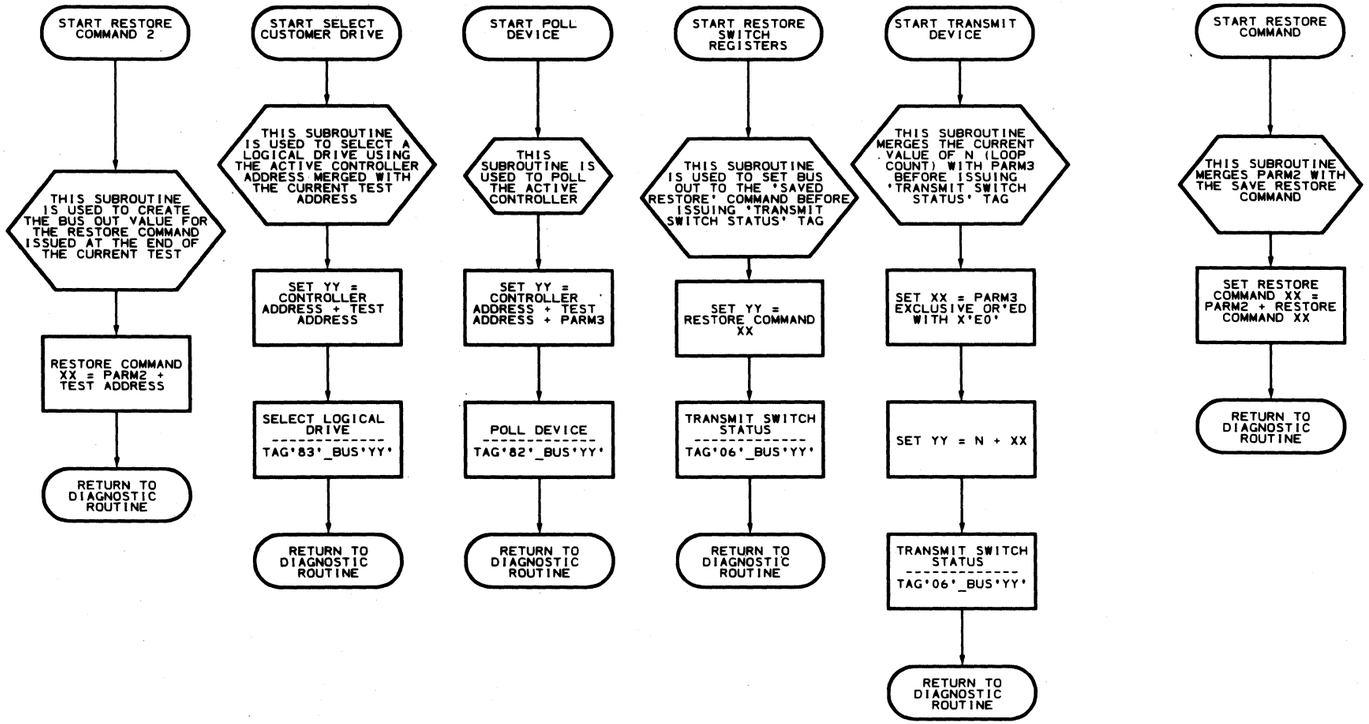








ROUTINE B6 – STRING SWITCH TESTS MICFL 585



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H87
JFL_12/01/75

MLM0006 6647M8
MICFL 585-R
H88
JFL_12/01/75

F
L

ROUTINE B8 – HDA AND CONTROL LOGIC TESTS

DESCRIPTION

Test 01. Head Disk Assembly Status

The purpose of Test 01 is to verify that when an HDA is cycled on for the first time, proper status is returned. (0110 000x) The test also ensures that there are no outstanding attentions after issuing an Attention Reset to the drive.

TEST 02. Access Timer Accuracy

The purpose of Test 02 is two fold:

1. To verify that an Access Timeout check comes on if a Seek Start is issued while the Access Control is forced into Zero mode.
2. To verify that correct status is produced by the Access Timeout condition. The Access Timer selects and times out in 180 milliseconds (+40 milliseconds.

Test 03. Rezero Operation Verification

Test 03 verifies that the HDA is turning and that a servo signal is being detected. The test then verifies that the servo responds to a Rezero command with carriage movement.

Test 04. Rezero Operation Verification – From Outer Stop – Part 2

Test 04 forces the servo into Zero Mode with the carriage at the outer crash stop via a diagnostic Go Home command + reverse direction. The test then verifies the ability of the access mechanism to respond to a Rezero command and advance through the prescribed state sequence and return to Track Zero.

Test 05. Rezero From Track 0

Test 05 checks the ability of the access control to perform a Rezero operation initiated from Track 0. The servo is verified for initiating movement in the reverse direction and advancing through the prescribed states to return the carriage to Track 0.

Test 06. No Motion Seek

The purpose of Test 06 is to ensure that Seek Complete is present immediately after issuing a Seek Start with the HAR and Difference Counter both zero. This test verifies that an Attention is received when Polling Device Tag '82' is issued.

Test 07. Seek Movement – Basic

Test 07 verifies that a seek start command Difference Counter (D = 8) causes the servo to start carriage movement in the proper direction.

Test 08. Overshoot Check

Test 08 verifies the Overshoot Check Safety circuits via two methods.

Method 1:
With the carriage track following at track zero, a 1-track seek is initiated in the reverse direction to force the carriage into the outer guardband area. An Overshoot Check should result. Drive Check is verified and the reset conditions are checked after a Check Reset.

Method 2:
Method 2 issues a 128-cylinder seek, resets the Difference Counter after a delay of 2.5 milliseconds, and tests that Overshoot Check does not become active before the third off-to-on transision of the track crossing pulses. Overshoot is tested for being active after this time along with Drive Check. The reset condition of these checks is also tested.

Test 09. Difference Counter Verification – Part 1

Test 09 sets the Difference Counter to 128 and issues a Forward Seek. The Difference Counter is sensed after each track crossing pulse to verify one decrement for each pulse received. If the Difference Counter does not compare to the Program Pulse Counter, then an error halt occurs. The 2nd, and 3rd bytes will contain the received and expected Difference Counter values, respectively.

Test 0A. Velocity Gain Calibration Check

Test 0A performs a 192-track forward seek operation and loops the test 10 times. The Access Control is monitored for accelerate-to-decelerate state advance and the Difference Counter is checked to be within specification at that time. Velocity gain is checked according to the operating range specifications (330 microsecond ± 20 microsecond) between Difference Counter = 'A' and Difference Counter = '8'.

Test 0B. Overshoot Check

Test 0B forces an Overshoot Check by moving the access into the inner guardband by issuing four cylinder seeks until the ID pattern is found. This in turn forces an Overshoot Check.

Test 0C. Unsuppressible Register

Test 0C ensures that the Unsuppressible Register sets and resets correctly. In addition, the test verifies that the correct Bit Significant Device Address (BSDA) is returned when there is Normal or Unsuppressible polling.

This test is bypassed if the string switch feature is installed. The string switch Unsuppressible Register test is in routine B6, Test 4.

Test 0D. Set Read/Write

The purpose of Test 0D is to ensure that the set Read/Write Tag '85' operates error free and Normal End is received from the tag. Moreover, the test also verifies that Normal End resets after issuing a Response. The test forces a Monitor Check, then verifies it can be set and reset.

Test 0E. Force No-PLO Input

The purpose of Test 0E is to ensure that No PLO input and Missing Data Input errors can be forced on and reset. The test verifies that Controller errors are forced on by these errors.

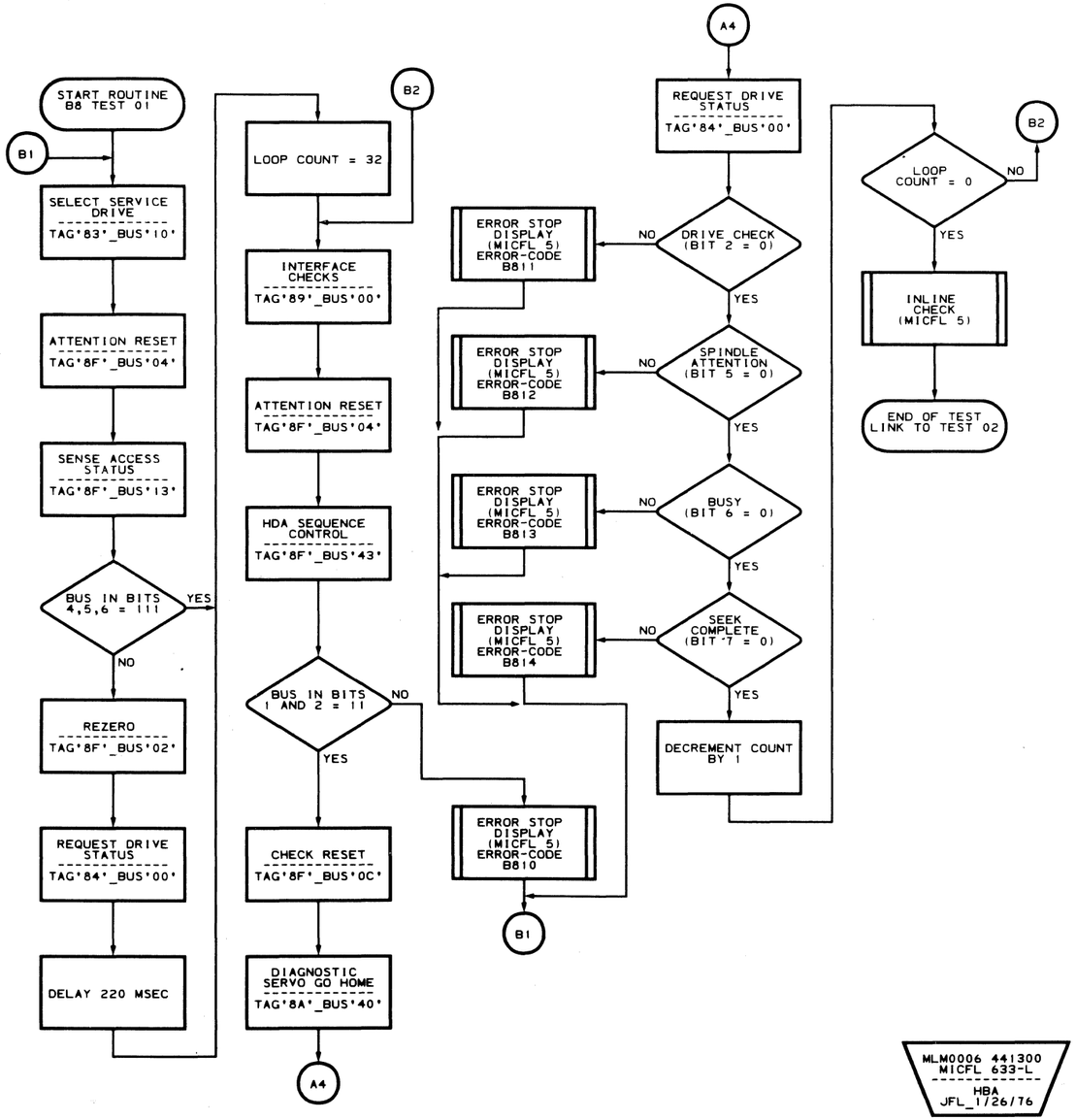
Test 0F. Servo Off-Track Error Verification

Test 0F verifies that the Servo Off-Track error check logic is operable. This error generates a Drive Check, a Read/Write Capable/Enable, and a Read/Write Check. The test also verifies that Index Check is present when forcing the Servo Off-Track error.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 72 for parameter entry.

ROUTINE B8 – HDA/CONTROL LOGIC TESTS



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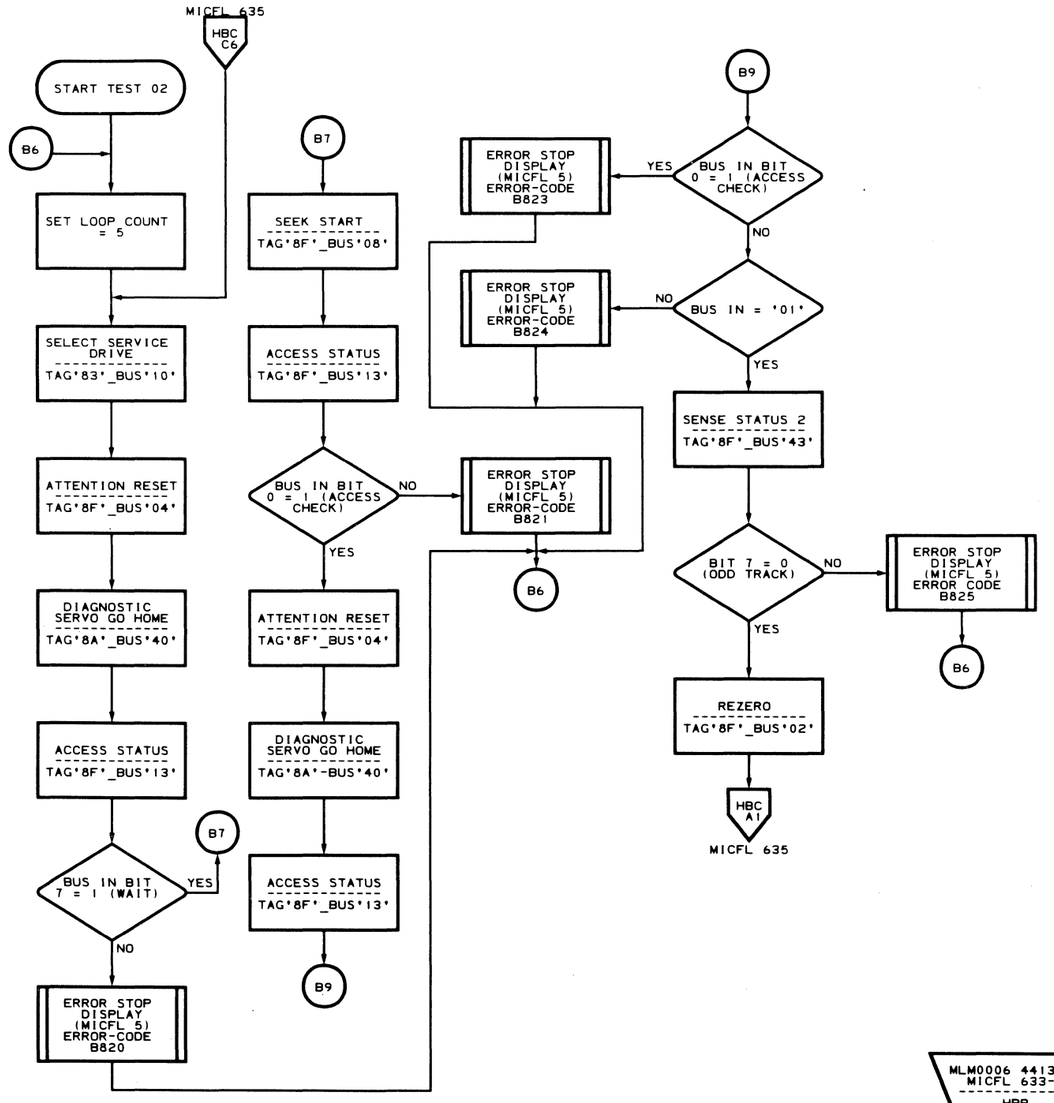
MICFL 633-L
HBA
JFL_1/26/76



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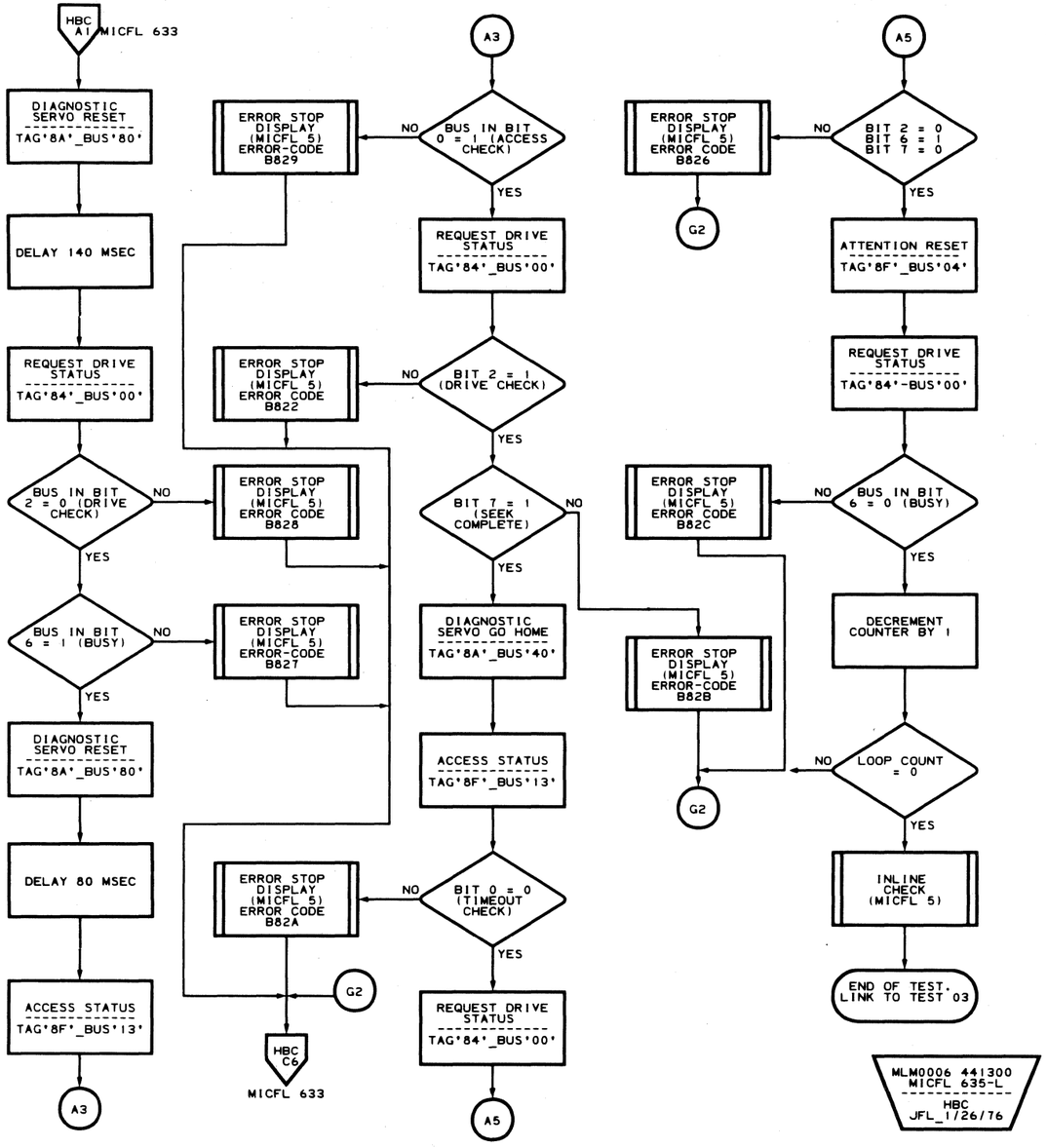
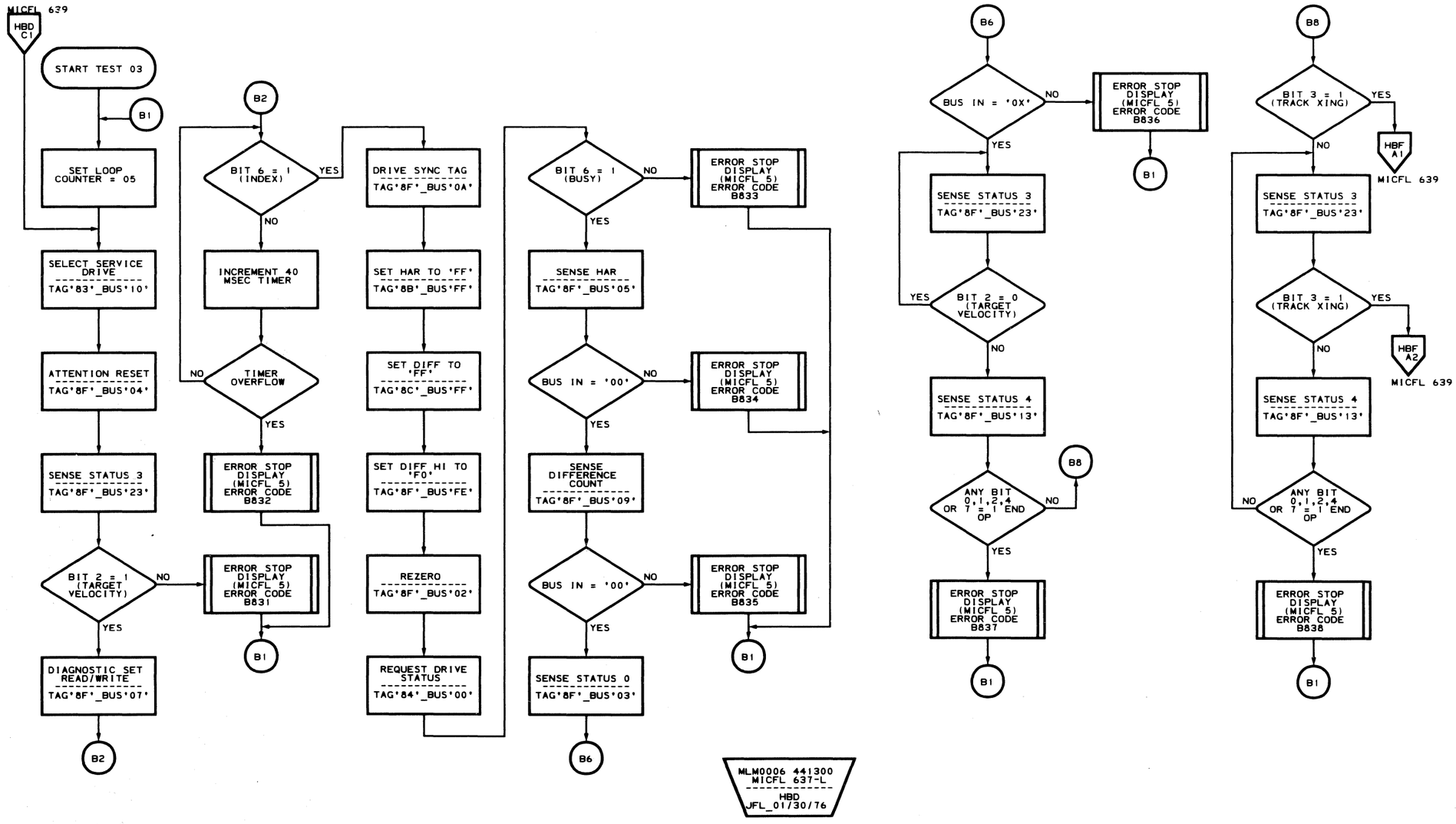


ROUTINE B8 – HDA/CONTROL LOGIC TESTS



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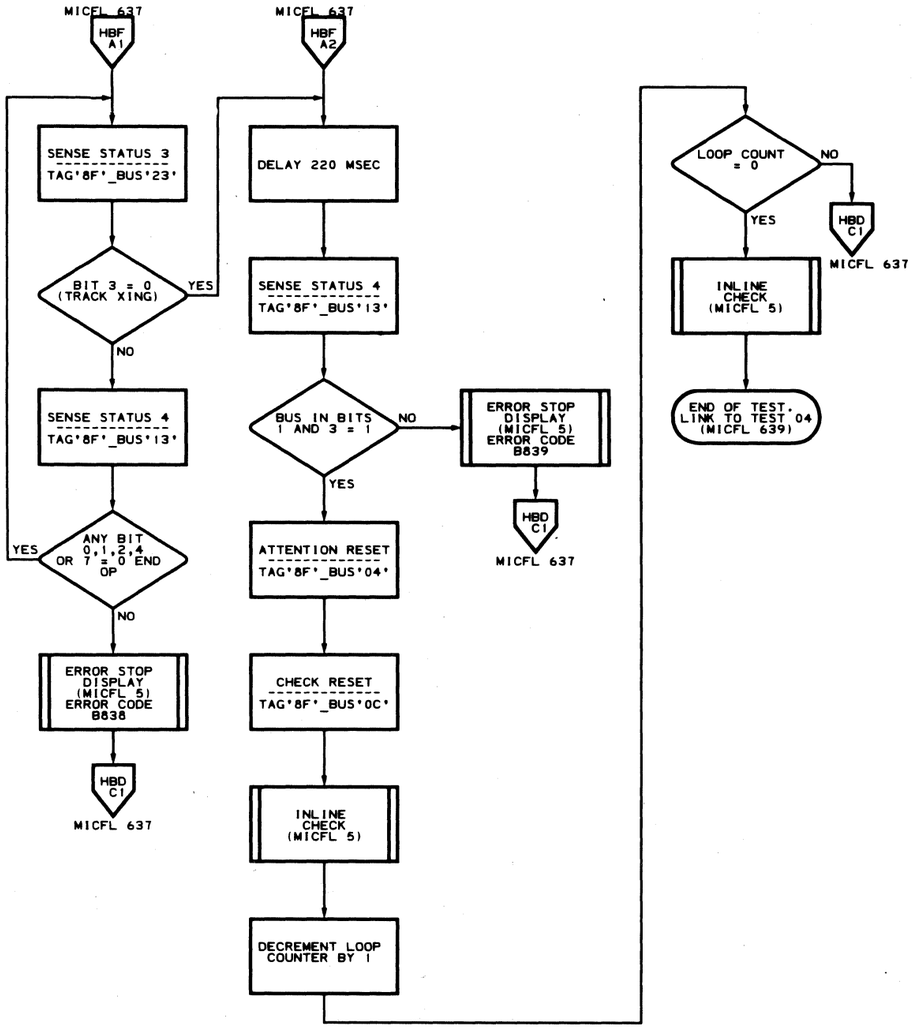

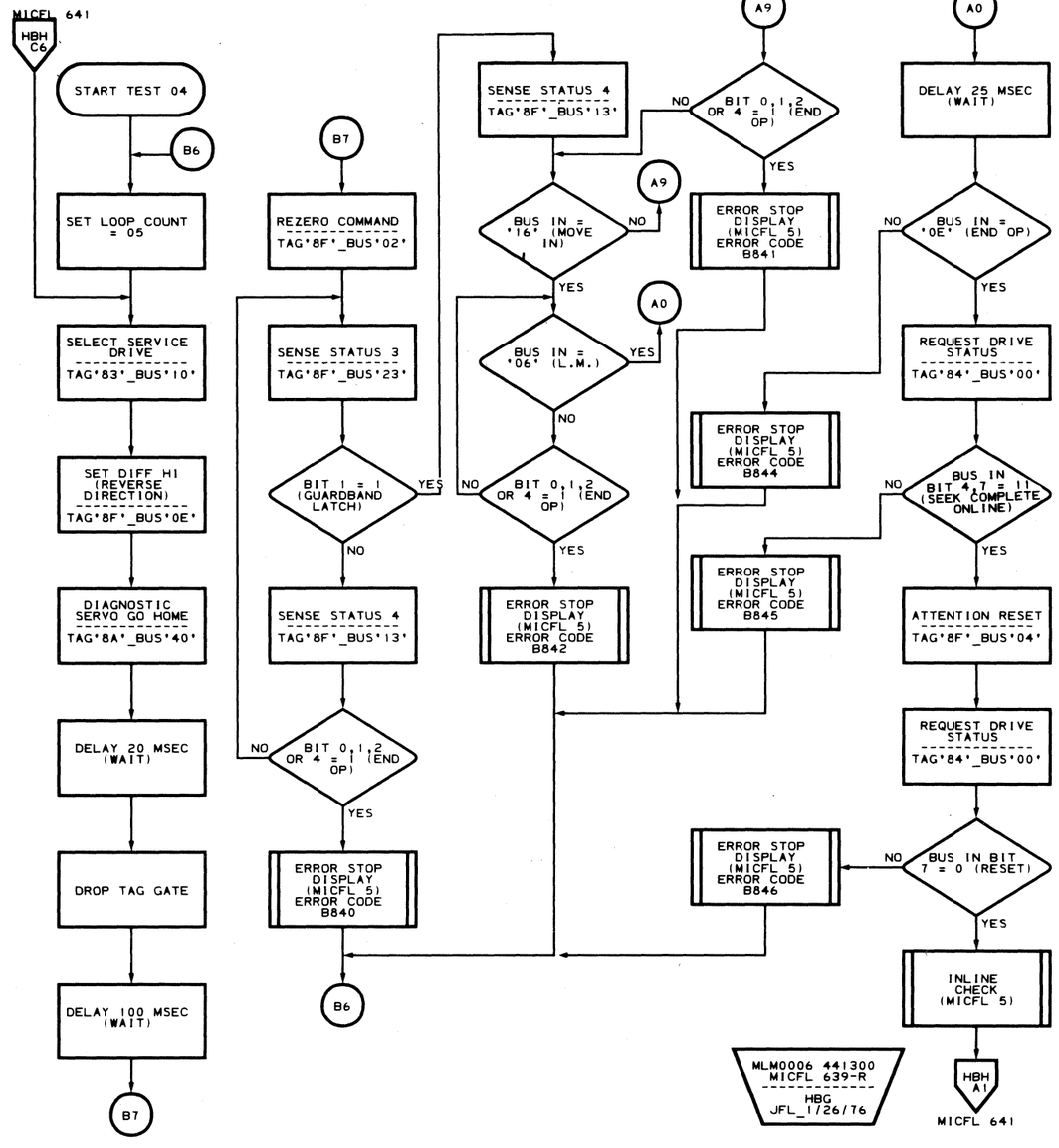

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MICFL 639-L
HBF
JFL_01/30/76

MLM0006 441300
MICFL 639-R
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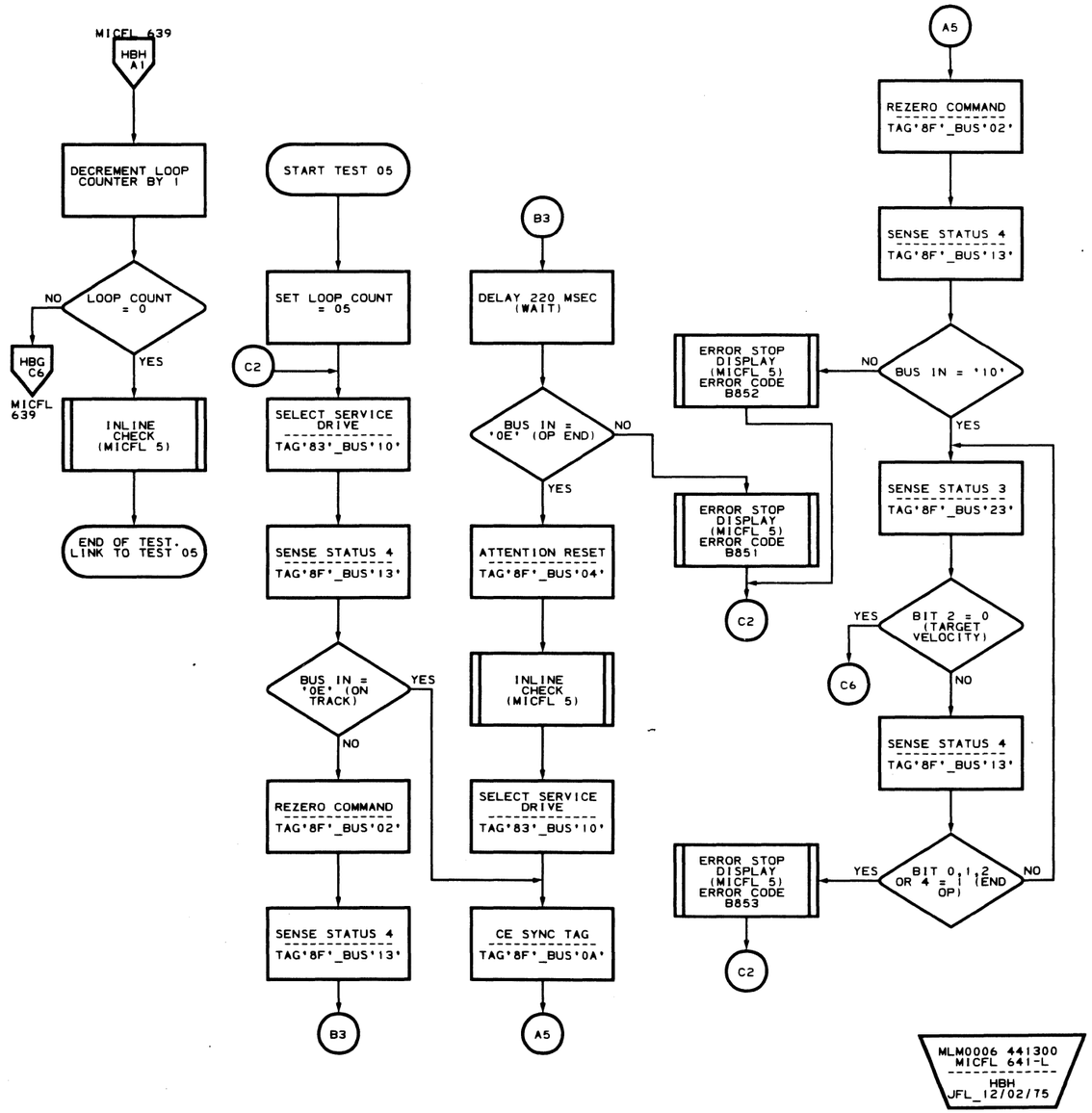
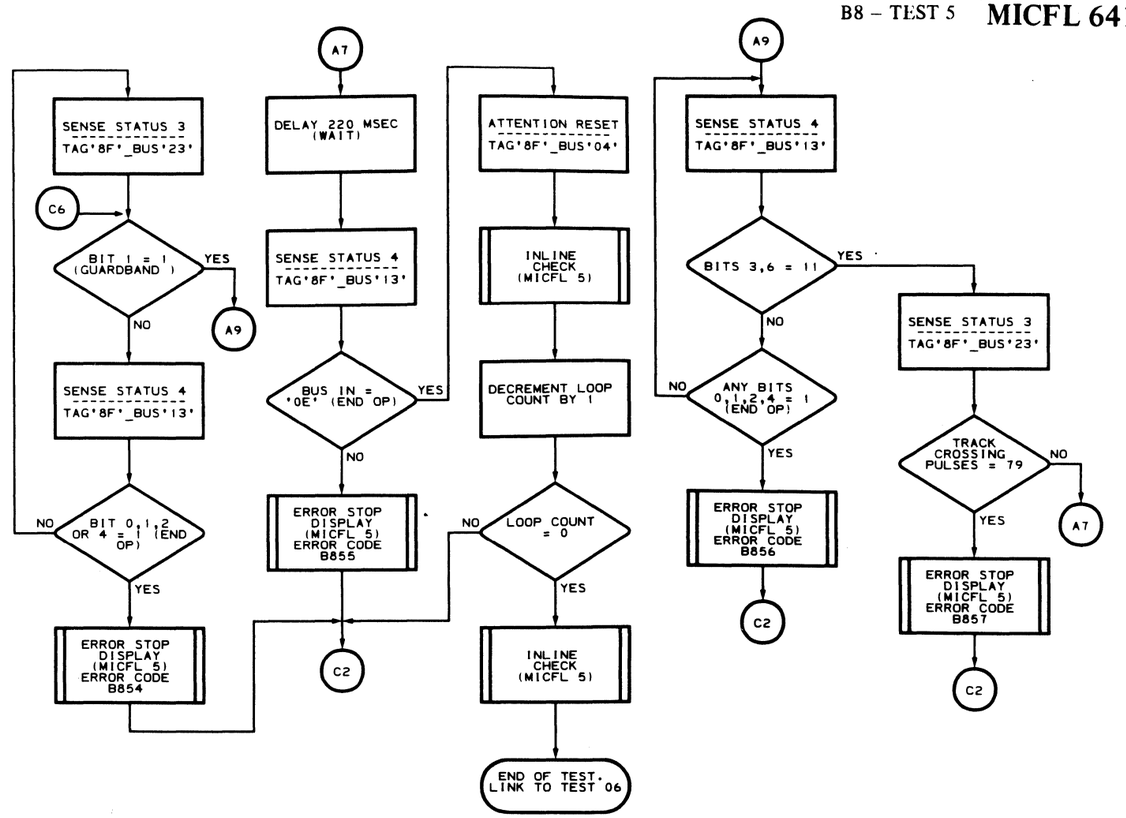
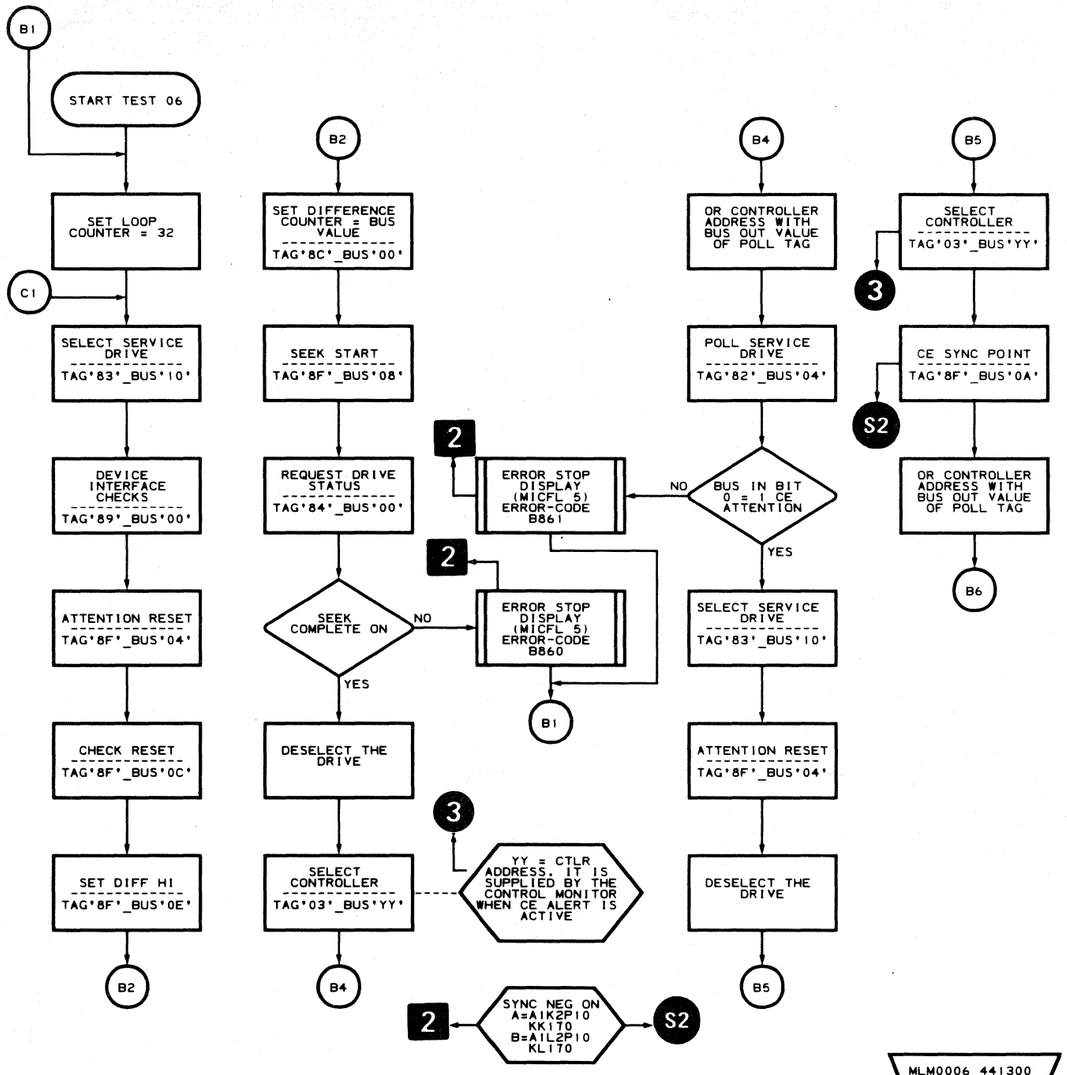
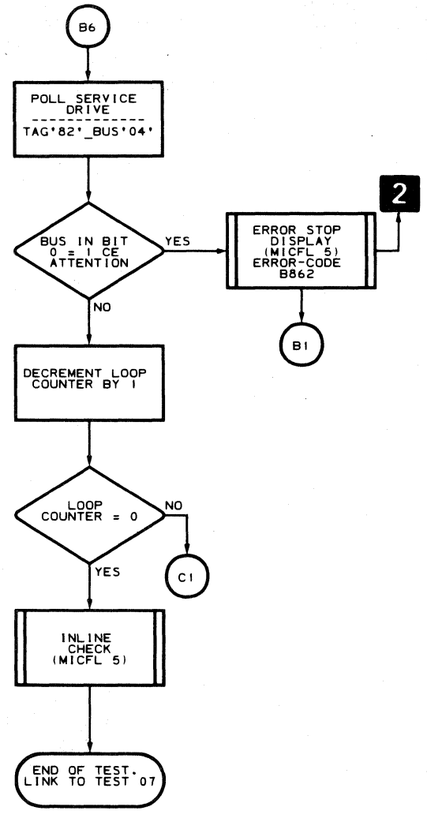
JFL_1/26/76

ROUTINE B8 – HDA/CONTROL LOGIC TESTS









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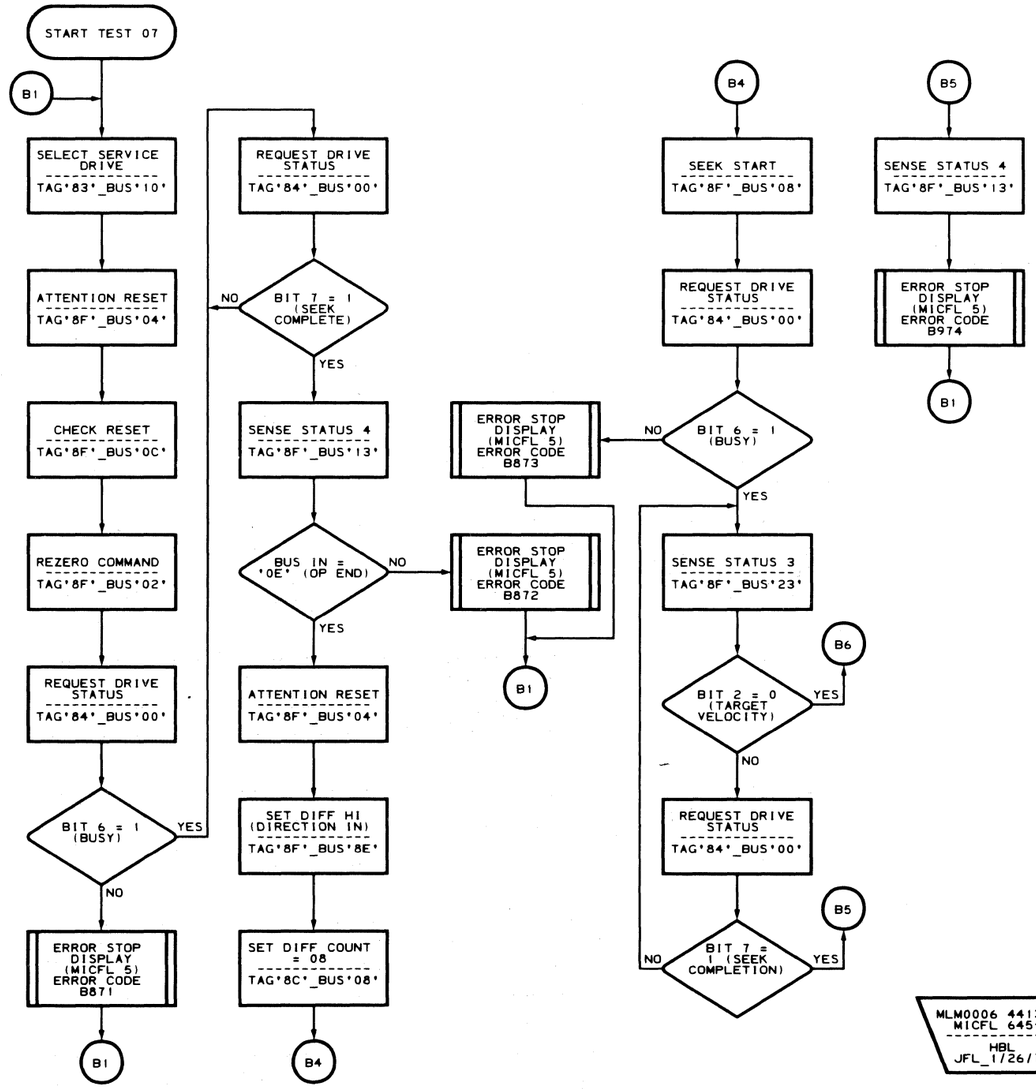
ROUTINE B8 – HDA/CONTROL LOGIC TESTS



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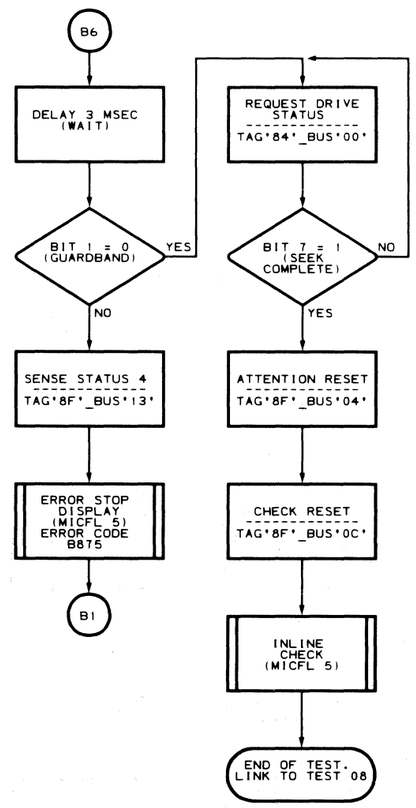

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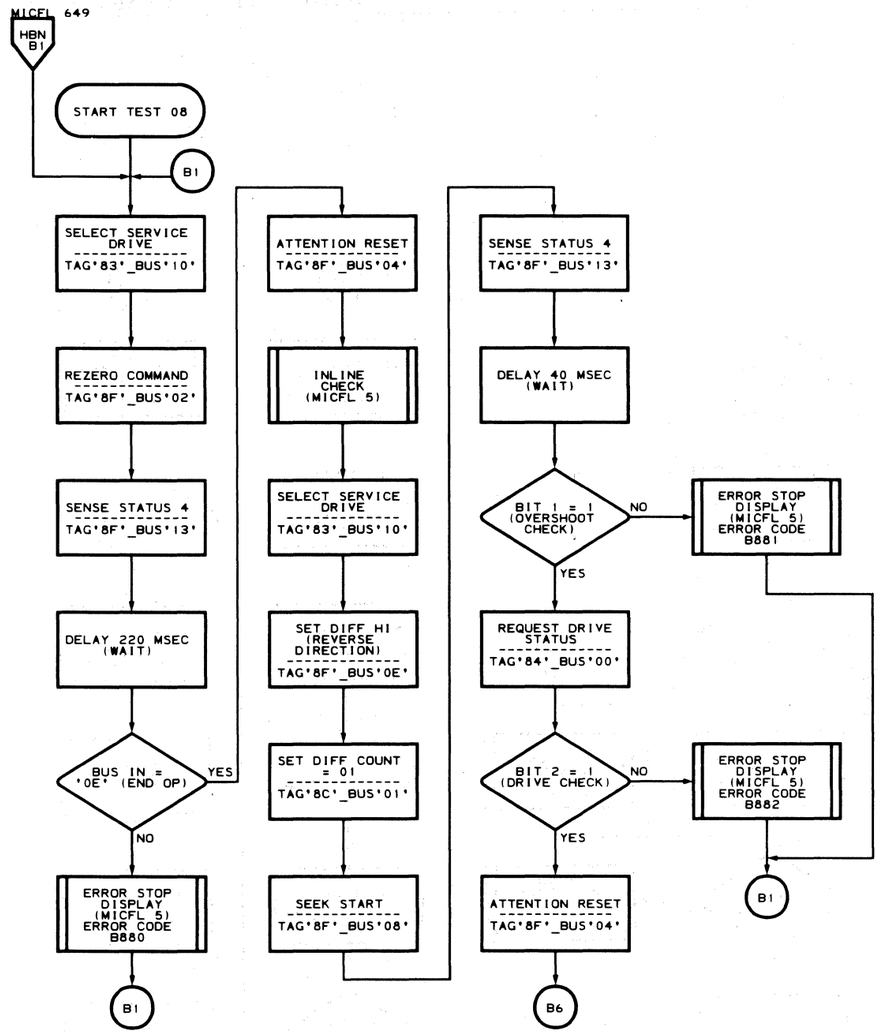
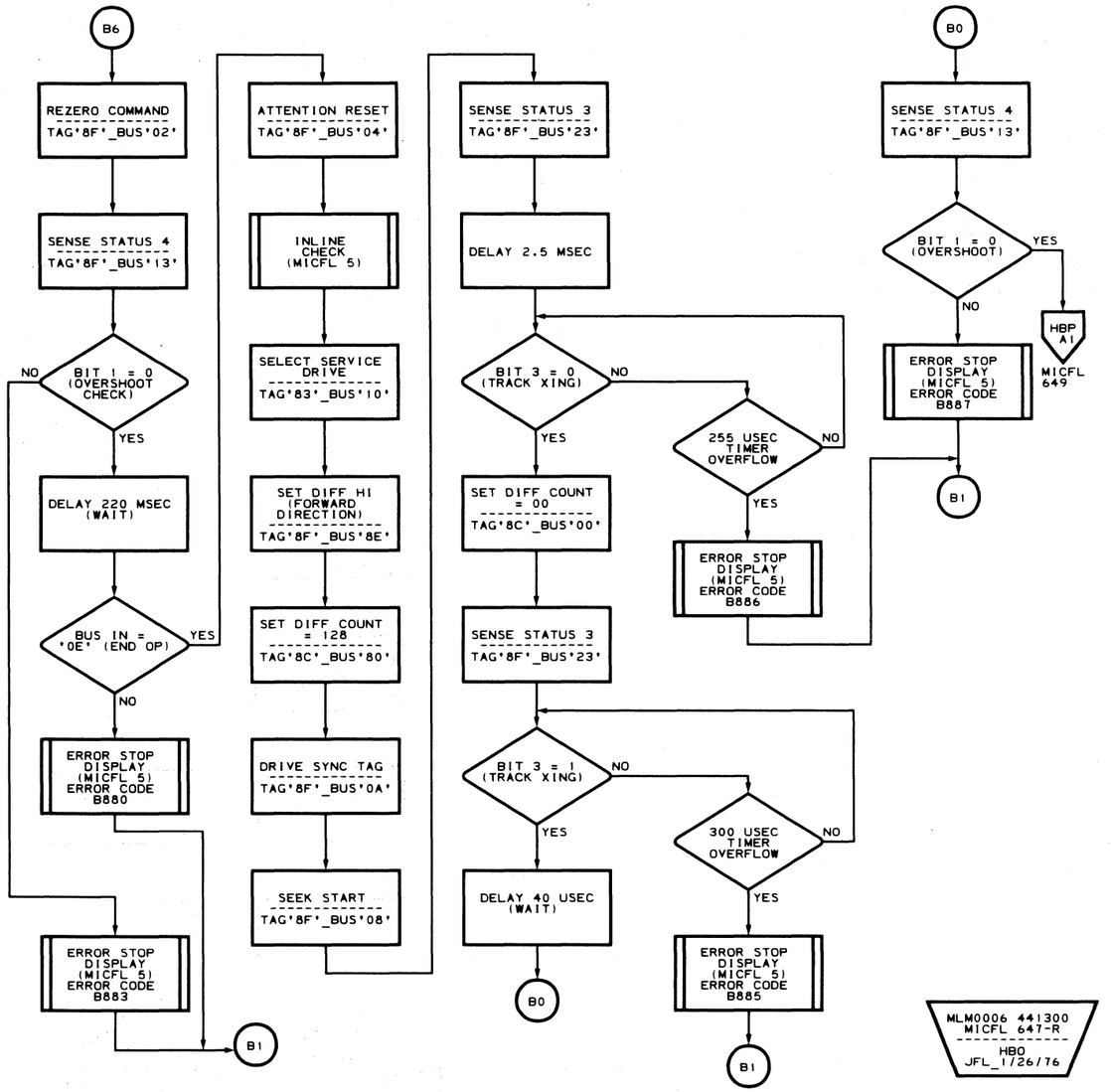
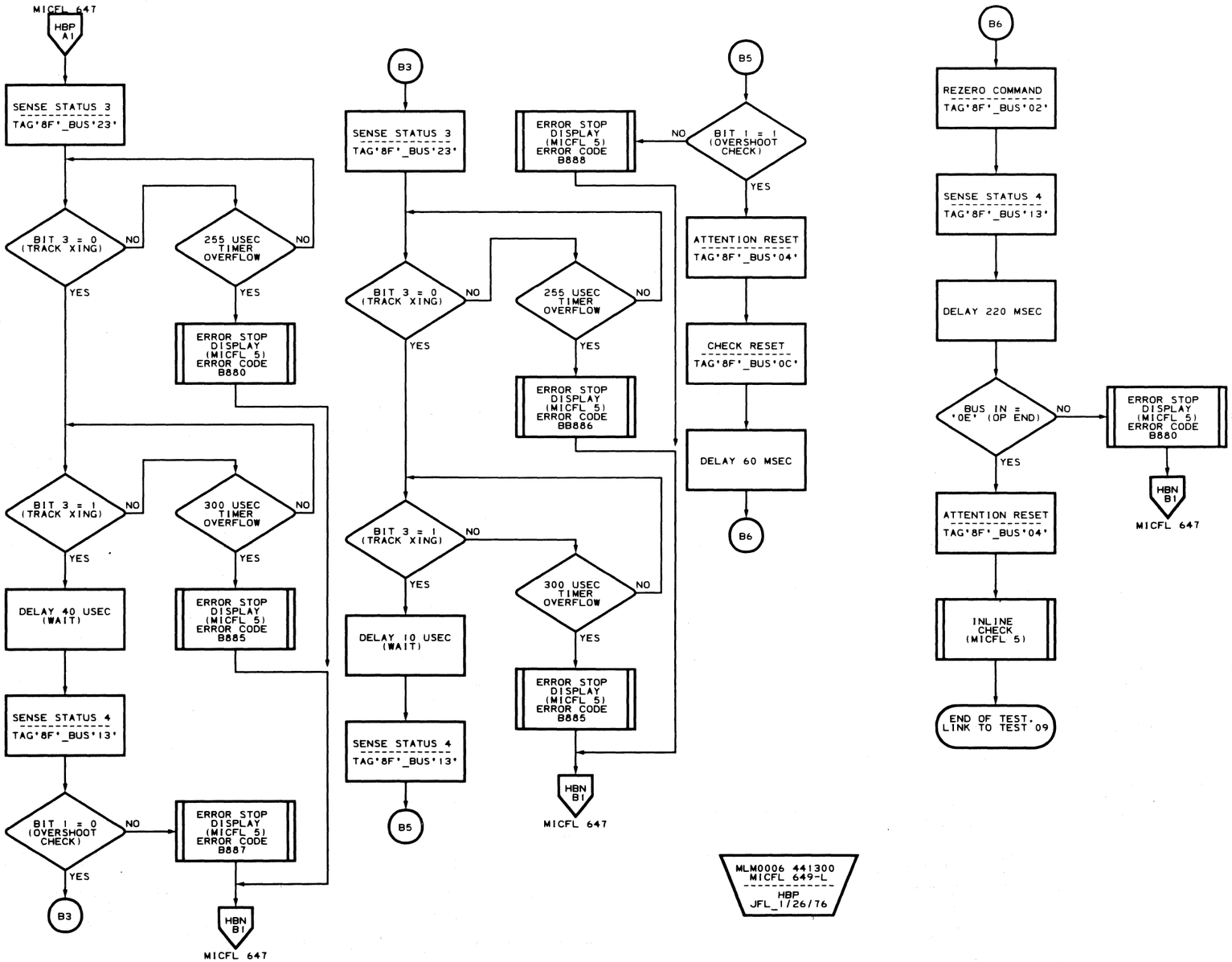


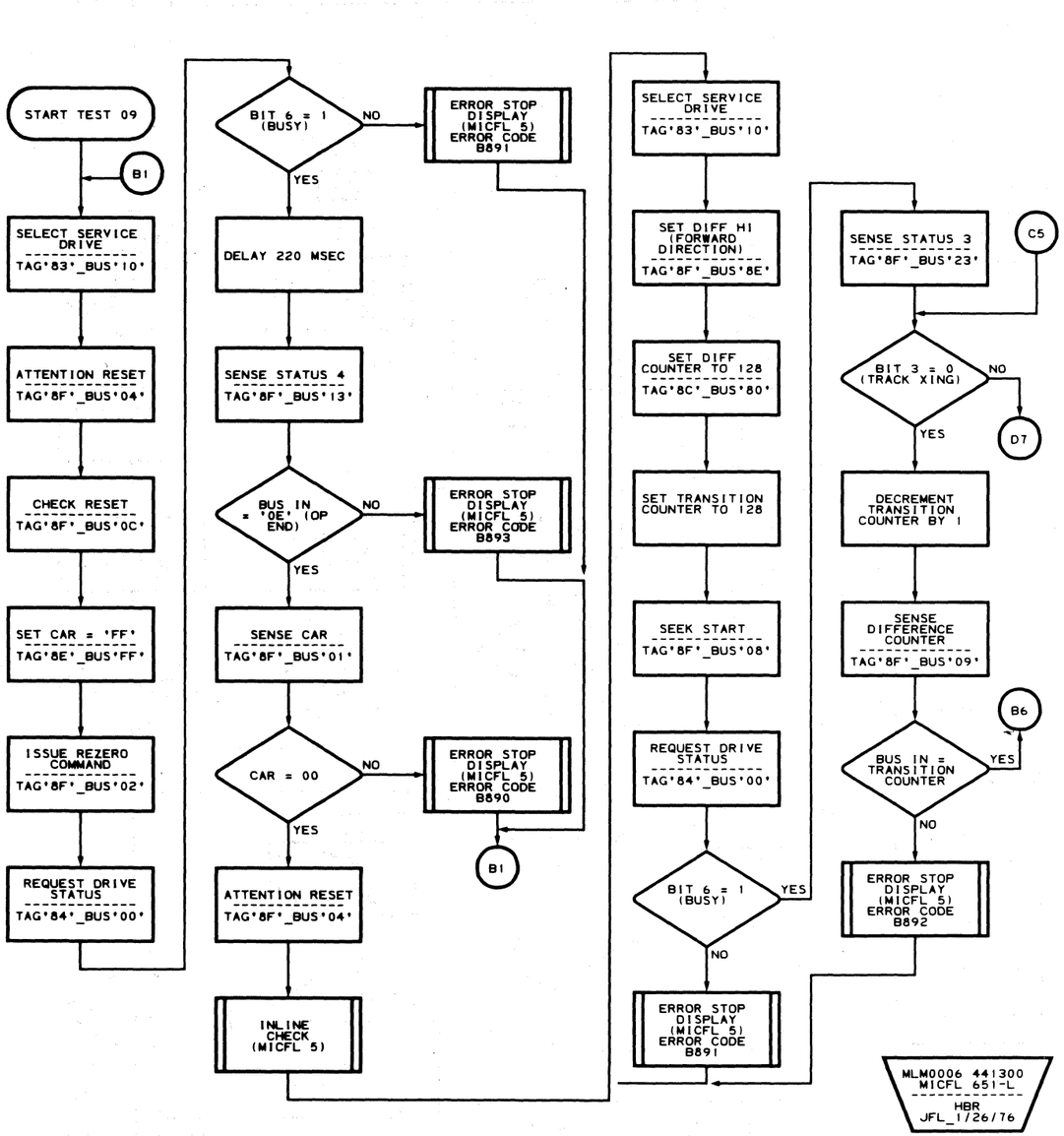


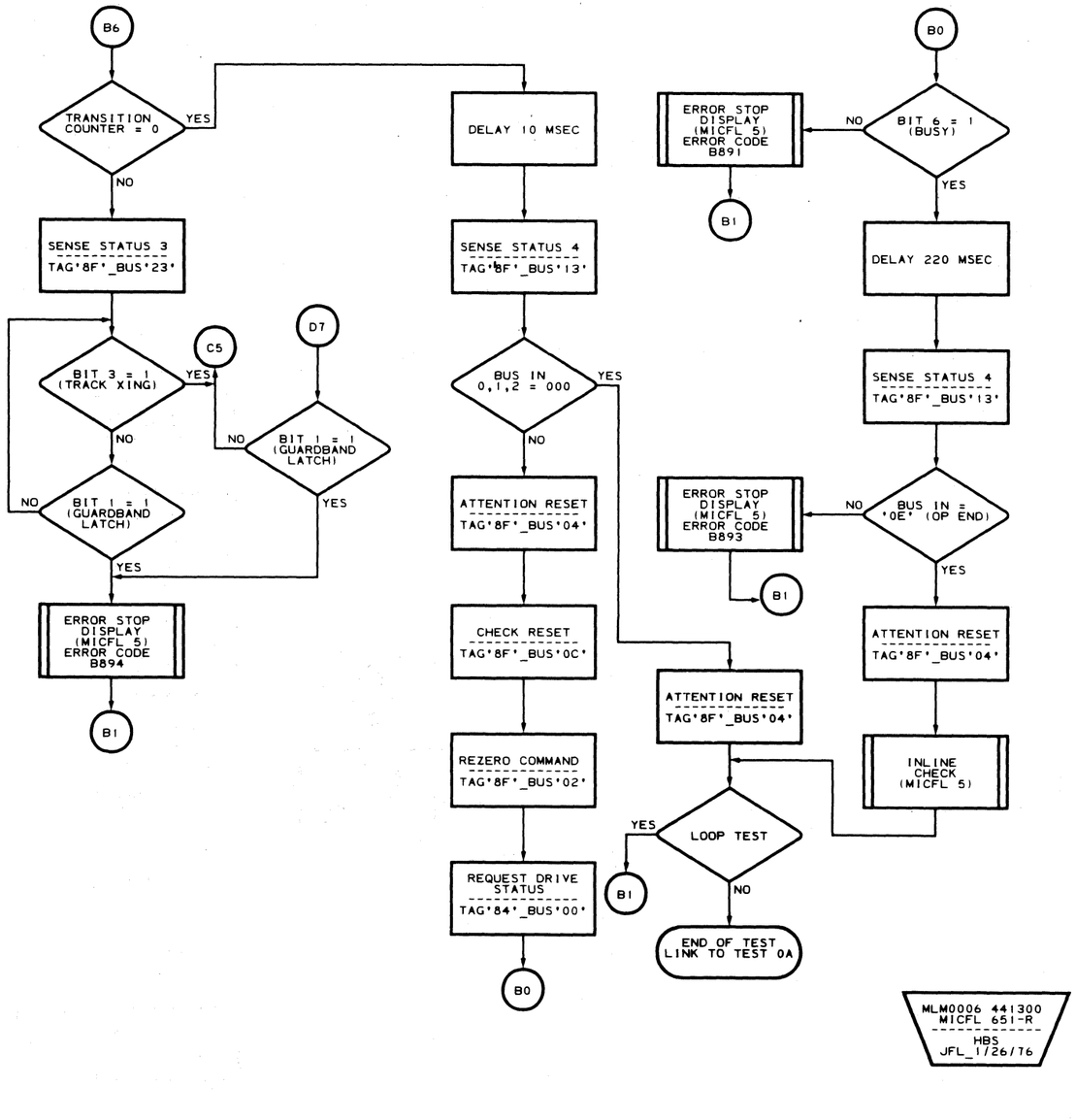
MLM0006 441300
MICFL 647-L
HBN
JFL_1/26/76

MLM0006 441300
MICFL 647-R
HBO
JFL_1/26/76

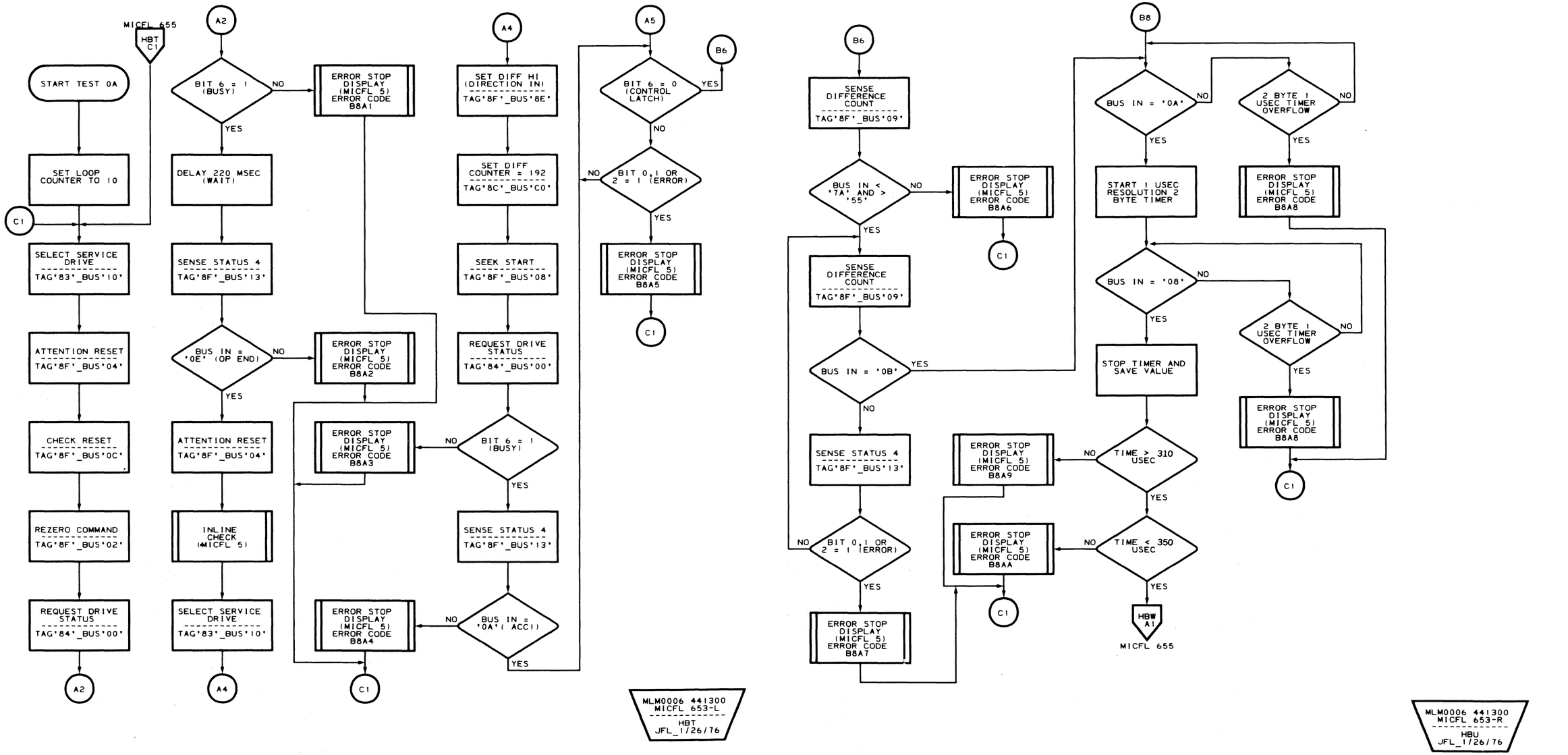
ROUTINE B8 – HDA/CONTROL LOGIC TESTS

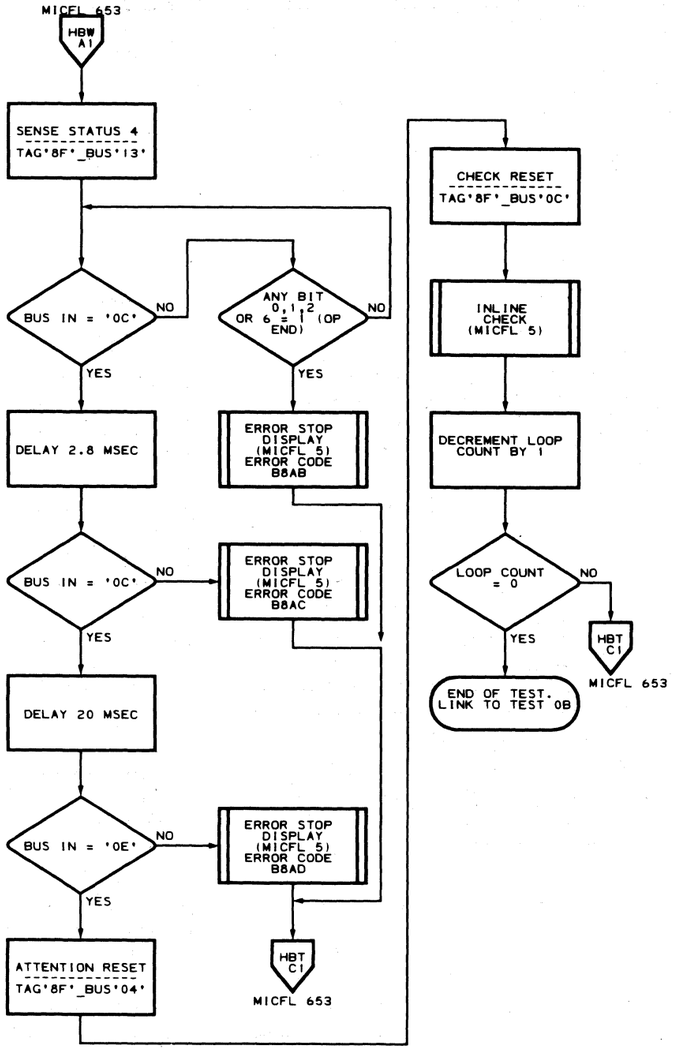


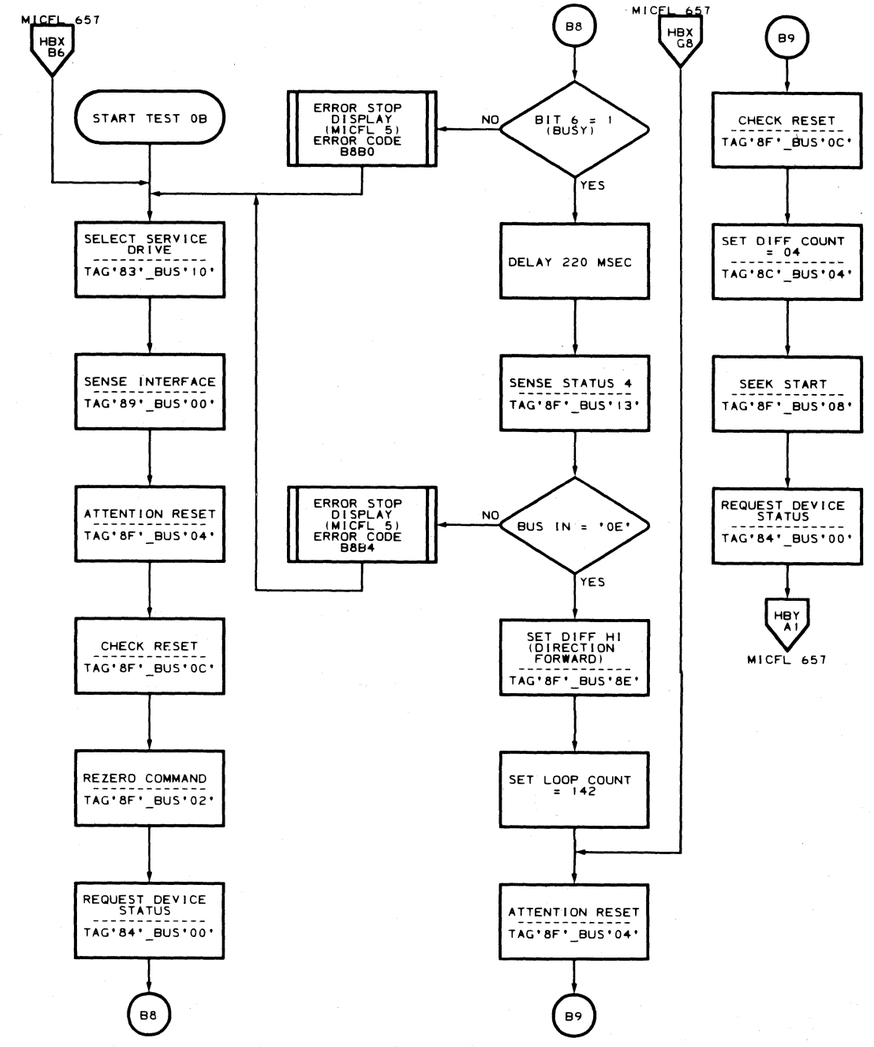




ROUTINE B8 – HDA/CONTROL LOGIC TESTS



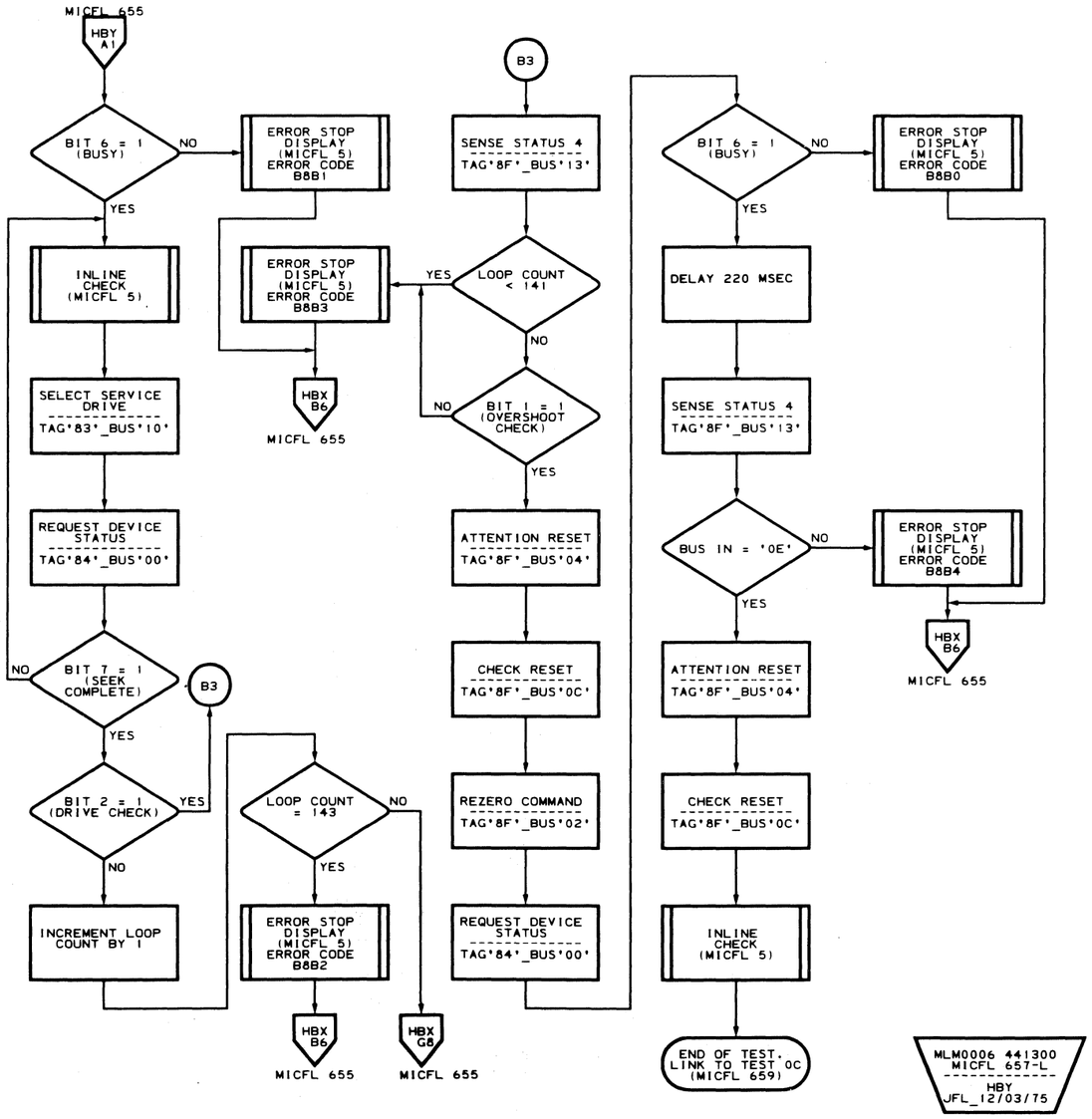


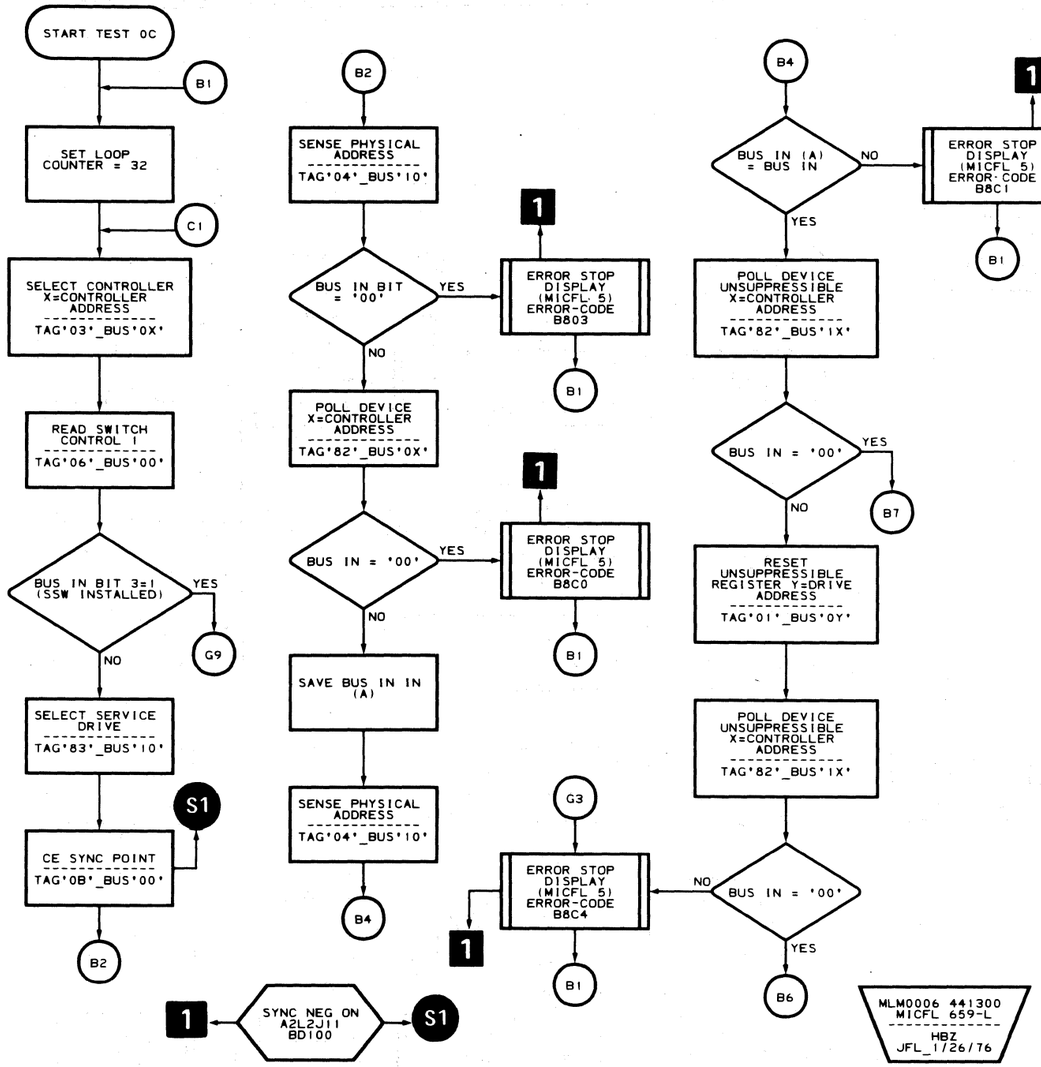


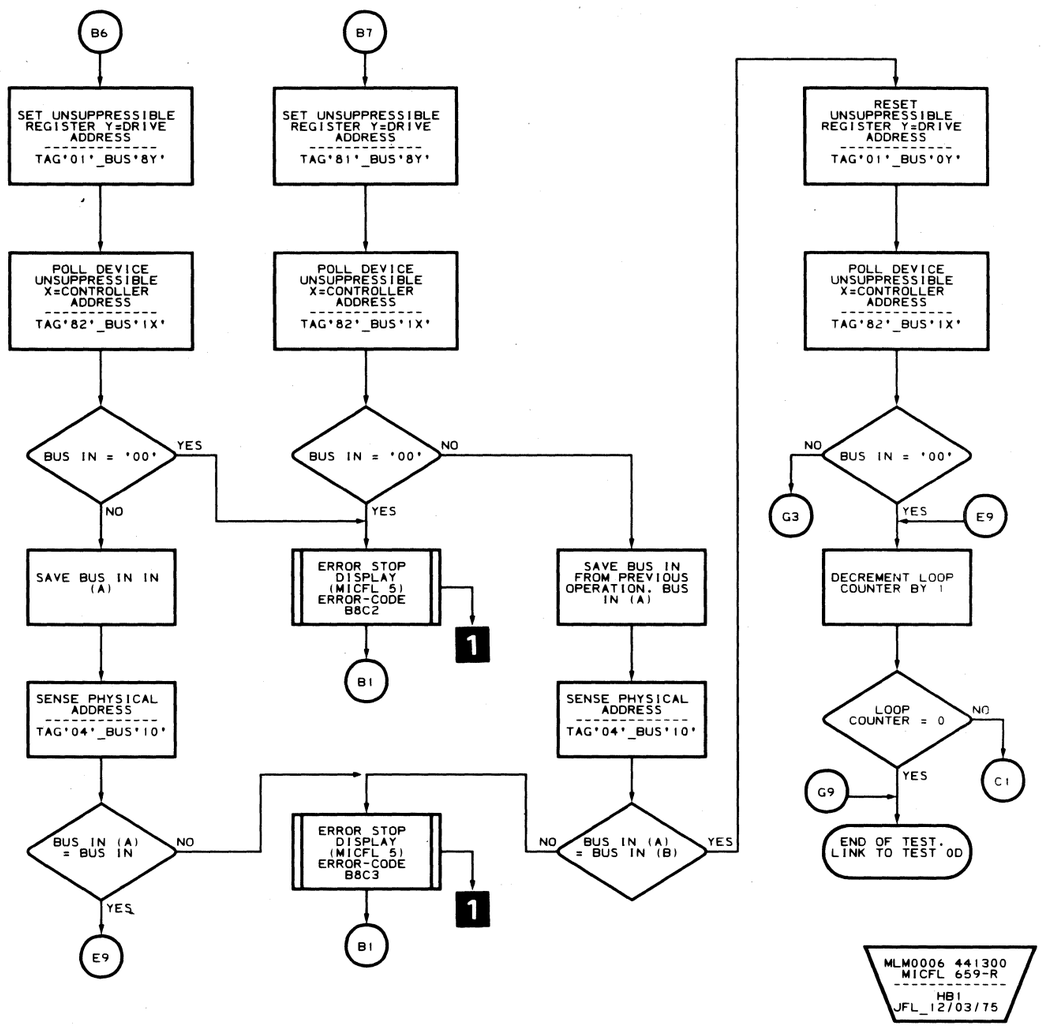
MLM0006 441300
MICFL 655-L
HBW
JFL_01/30/76

MLM0006 441300
MICFL 655-R
HBX
JFL_1/26/76

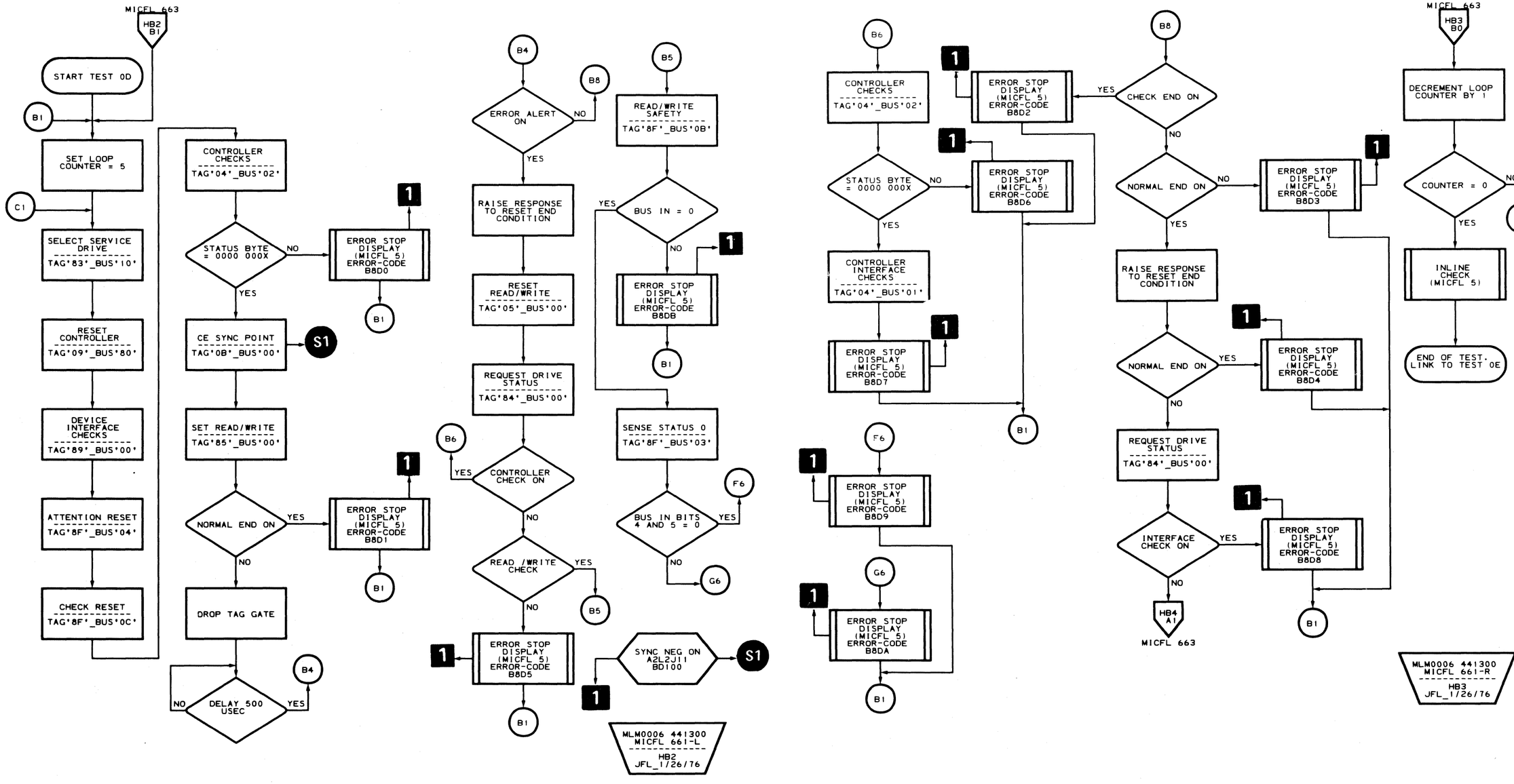
ROUTINE B8 – HDA/CONTROL LOGIC TESTS

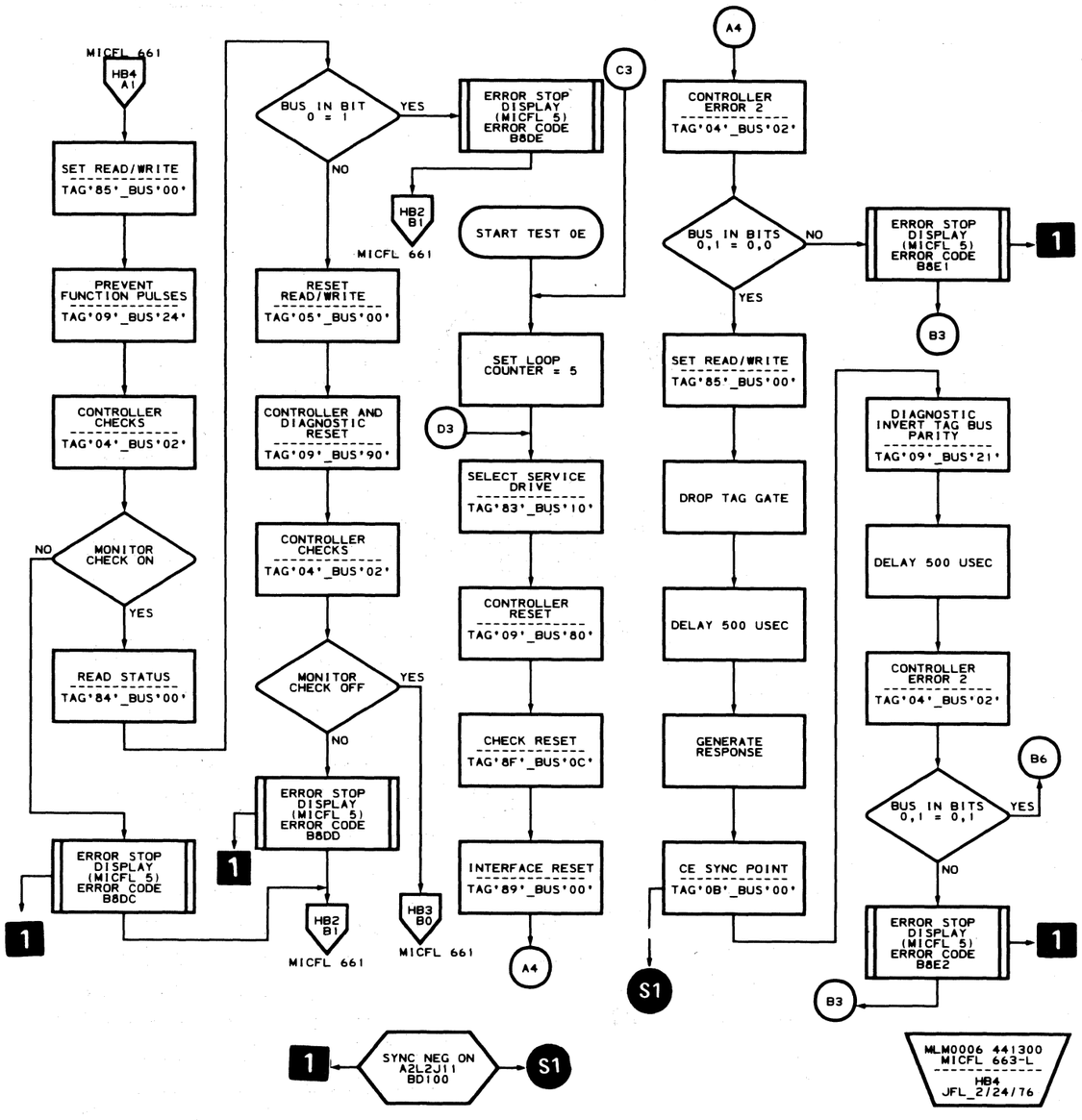


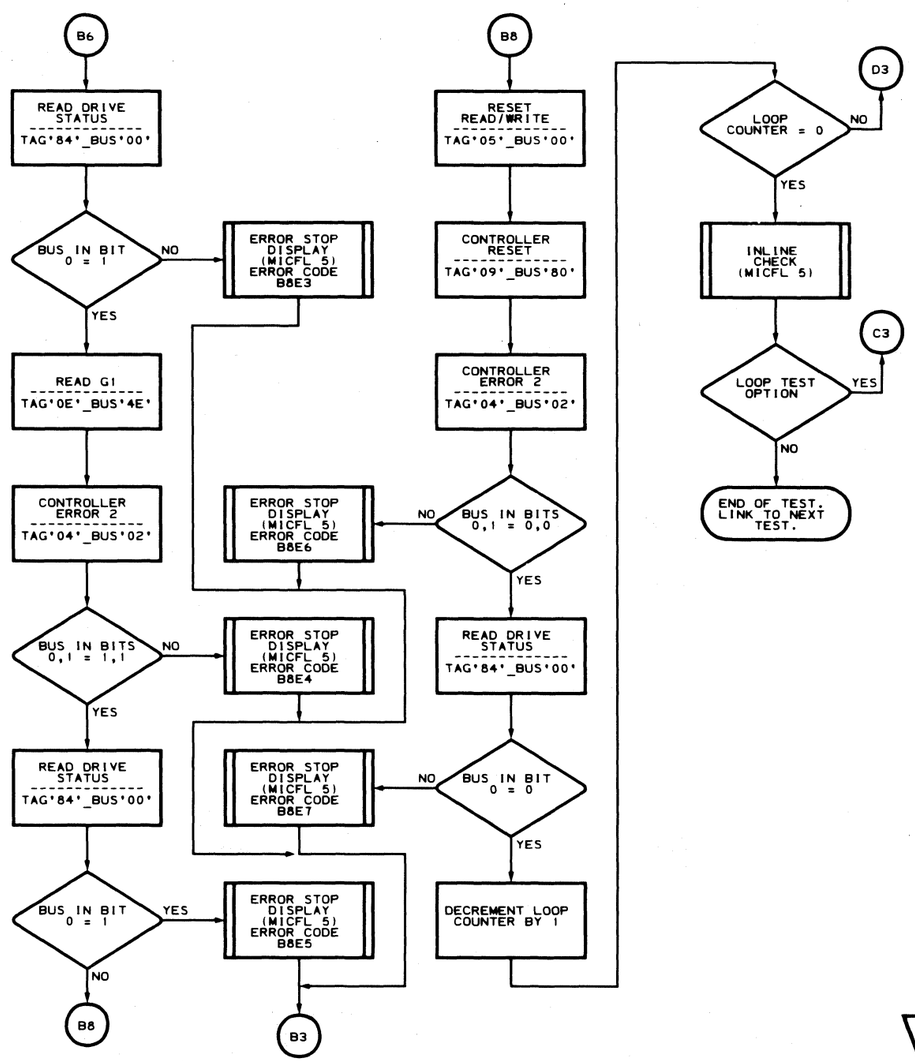




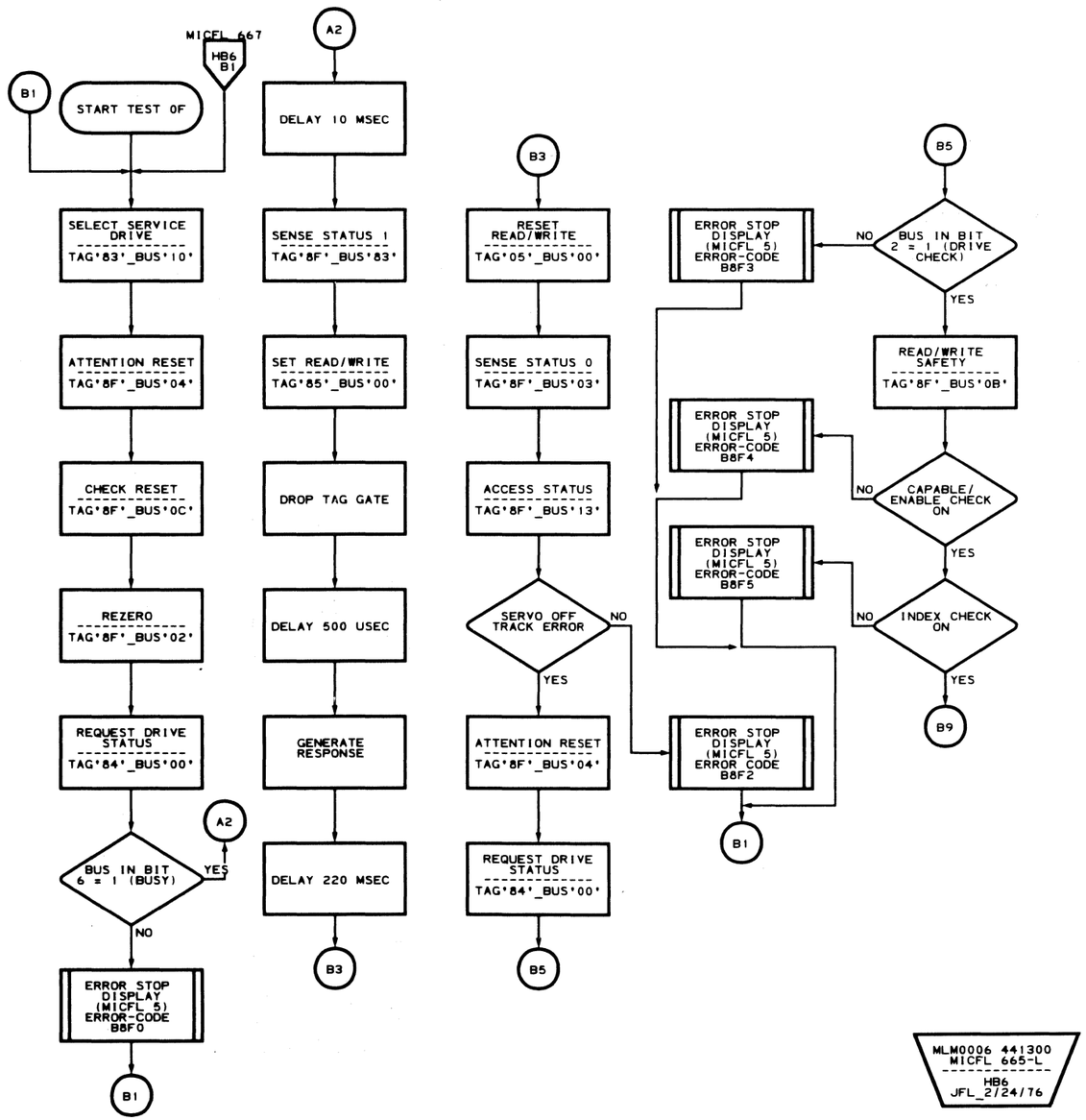
ROUTINE B8 – HDA/CONTROL LOGIC TESTS

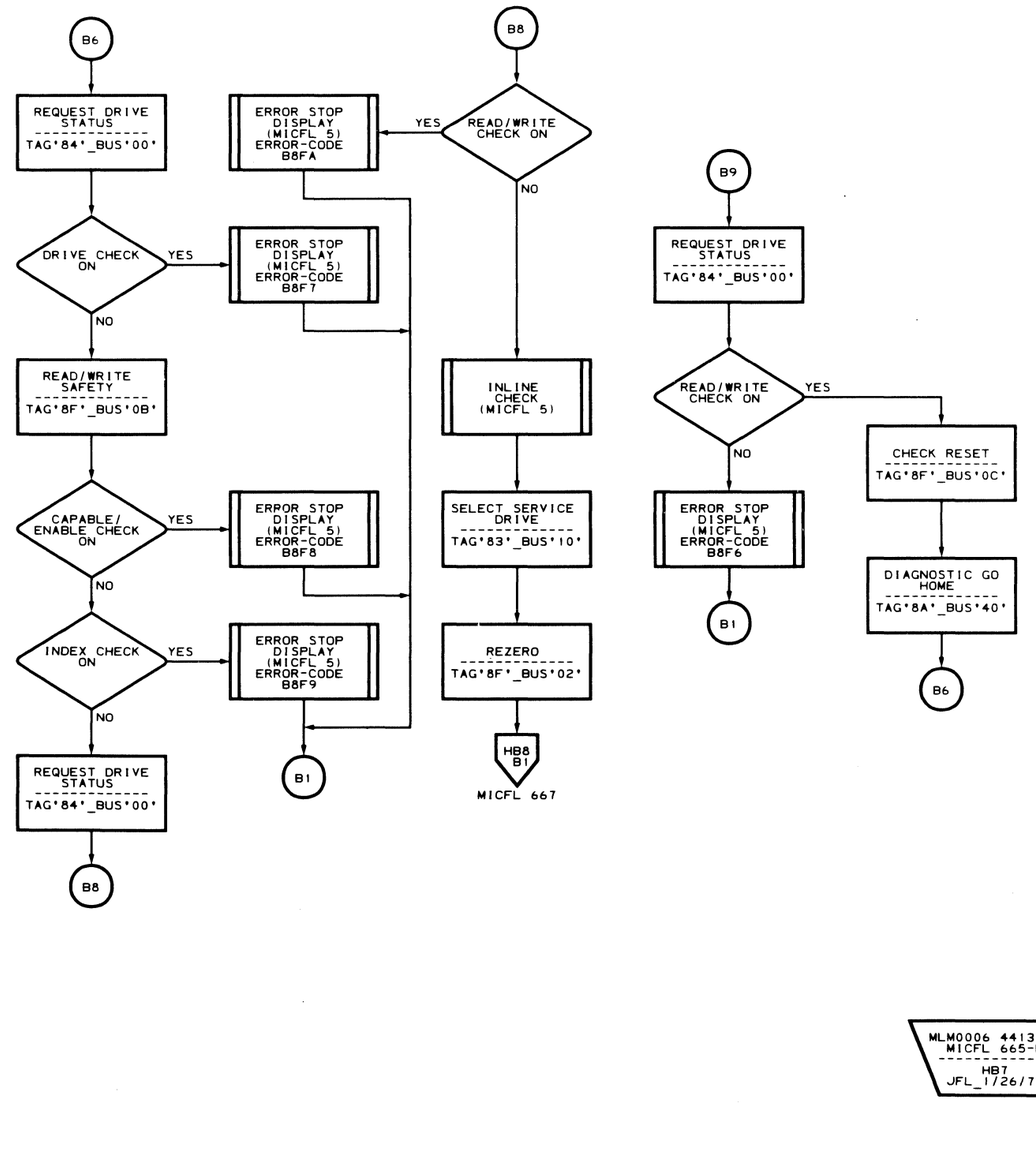


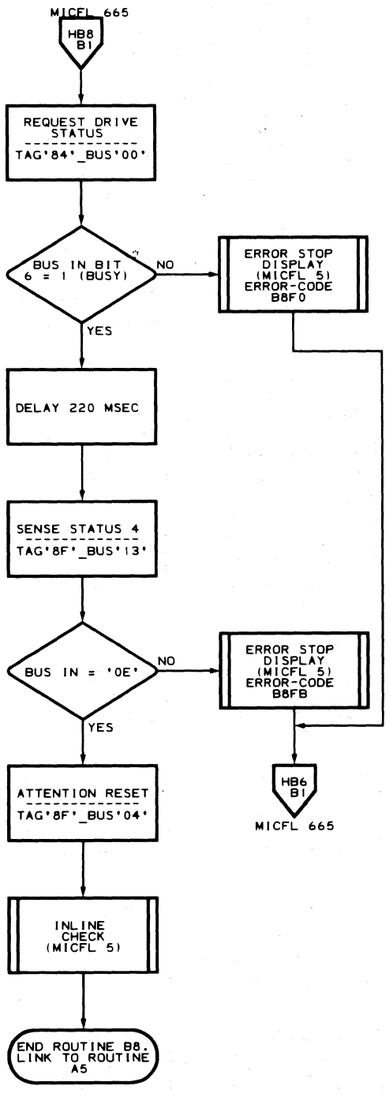




ROUTINE B8 – HDA/CONTROL LOGIC TESTS







MLM0006 441300
MICFL 667-L
HB8
JFL_12/03/75

ROUTINE B9 – 3350 DYNAMIC SERVO TESTS PART II

DESCRIPTION

Routines B8 and B9 are dynamic servo tests. Routine B9 consists of seven tests designed to test the servo area in a progressive building-block fashion. Access positioning is verified by reading the Home Address (using Head 0) in all tests.

Test 01. Rezero, Read Home Address

Test 01 issues the Rezero command, testing to ensure that Busy becomes active, and then testing for Seek Complete. When Seek Complete is received, a test for Drive Check is made to ensure that no access errors have occurred. An Attention Reset is issued to reset Seek Complete and the Home Address is read to verify correct access positioning on cylinder 0. Test 01 is repeated 10 times before linking to Test 02 in normal operation.

Test 02. Difference Counter Verification, Part 2

Test 02 sets the Difference Counter with a sliding 1s pattern (1 to 256) and issues both a forward and a reverse Seek, starting with a 1-cylinder Seek. The Difference Counter is sensed after each track crossing pulse to verify one decrement for each pulse received. If the Difference Counter does not compare to the Program Pulse Counter, then an error halt occurs. This test links to Test 03 after a successful completion.

Test 03. Incremental Seek (Increment = 1)

Test 03 seeks from cylinder 0 to cylinder 11 and back to cylinder 0 in 1-cylinder increments. The access position is verified after each Seek by reading the Home Address with Head 0. A comparison is made between the actual status of Odd Track (bit 7 under data module sequence control) and the expected type of track (odd or even). An error stop occurs if a noncompare results. This test links to Test 04 when the access has returned to cylinder 0 in normal operation.

Test 04. Incremental Seek (Increment = 2)

Test 04 seeks from cylinder 0 to cylinder 22 and back to cylinder 0 in 2-cylinder increments. Conditions tested are identical to those in Test 03. This test links to Test 05 when the access has returned to cylinder 0 in normal operation.

Test 05. Incremental Seek (Increment = 70)

Test 05 seeks from cylinder 0 to cylinder 560 and back to cylinder 0 in 70-cylinder increments. Conditions tested are identical to those in Test 03. This test links to Test 06 when the access has returned to cylinder 0 in normal operation.

Test 06. Incremental Seek (Increment = 280)

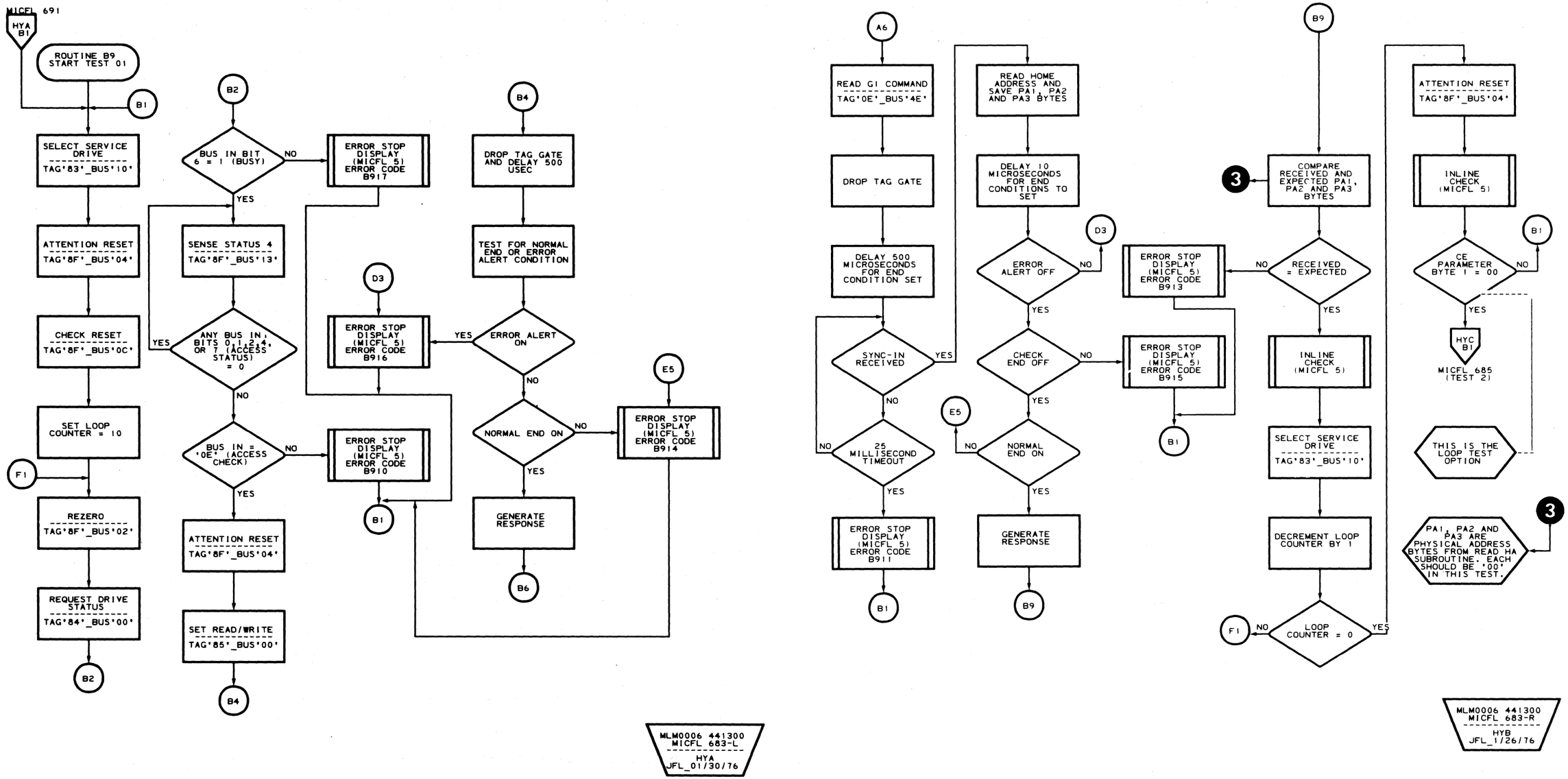
Test 06 seeks from cylinder 0 to cylinder 560 and back to cylinder 0 in 280-cylinder increments. Conditions tested are identical to those in Test 03. This test links to Test 07 when the access has returned to cylinder 0 in normal operation.

Test 07. Incremental Seek (Increment = 560)

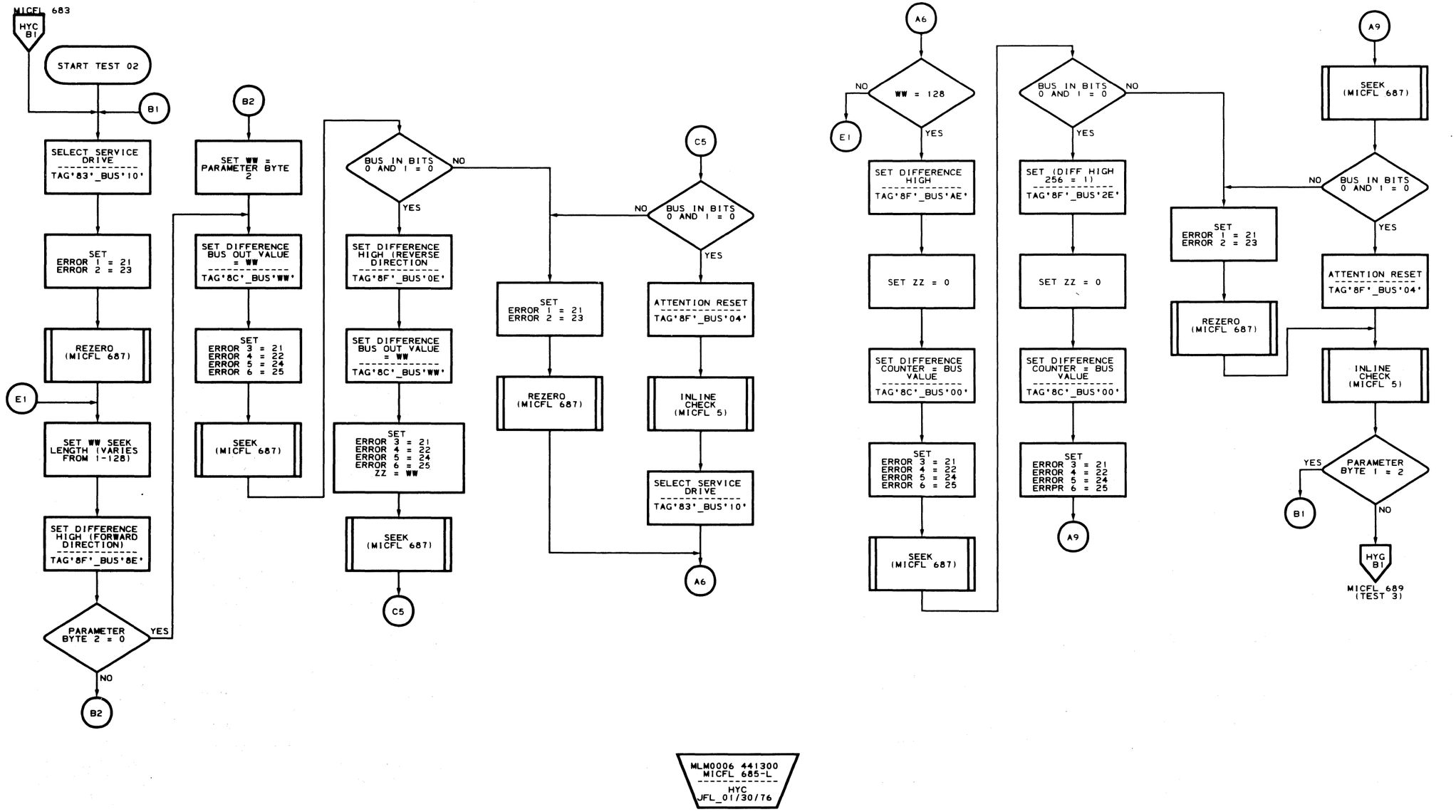
Test 07 seeks from cylinder 0 to cylinder 560 and back to cylinder 0 in one 560-cylinder increment. Conditions tested are identical to those in Test 03. This test links to routine AE when the access has returned to cylinder 0 in normal operation.

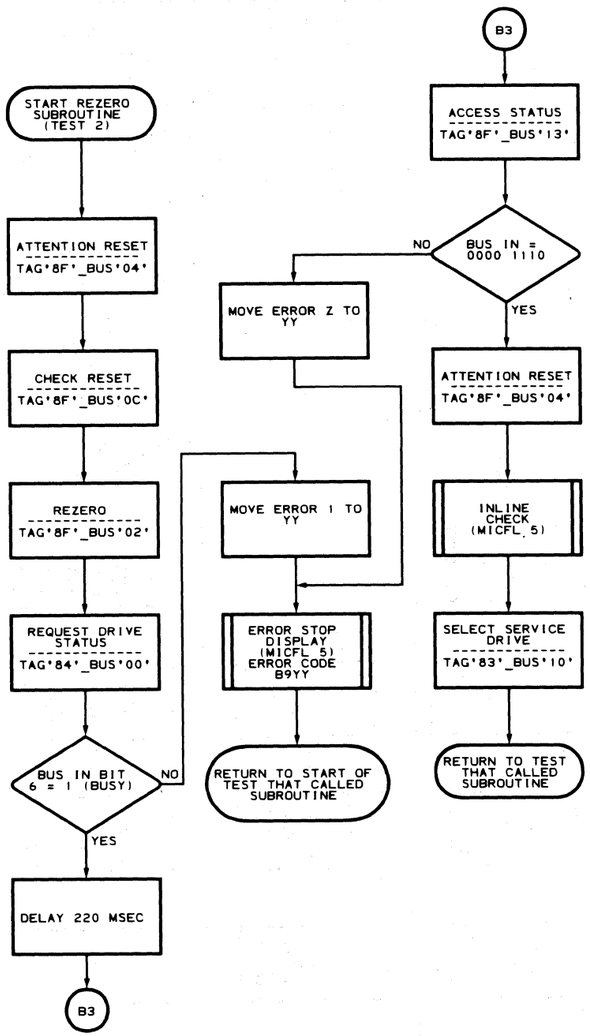
OPERATING PROCEDURE

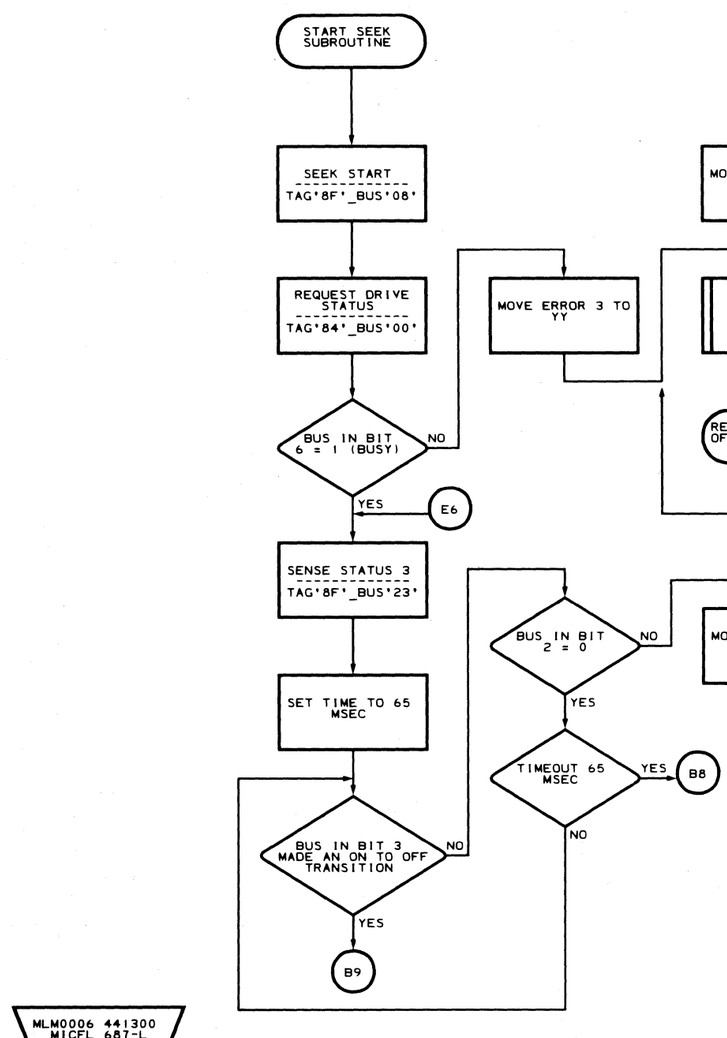
- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 72 for parameter entry.

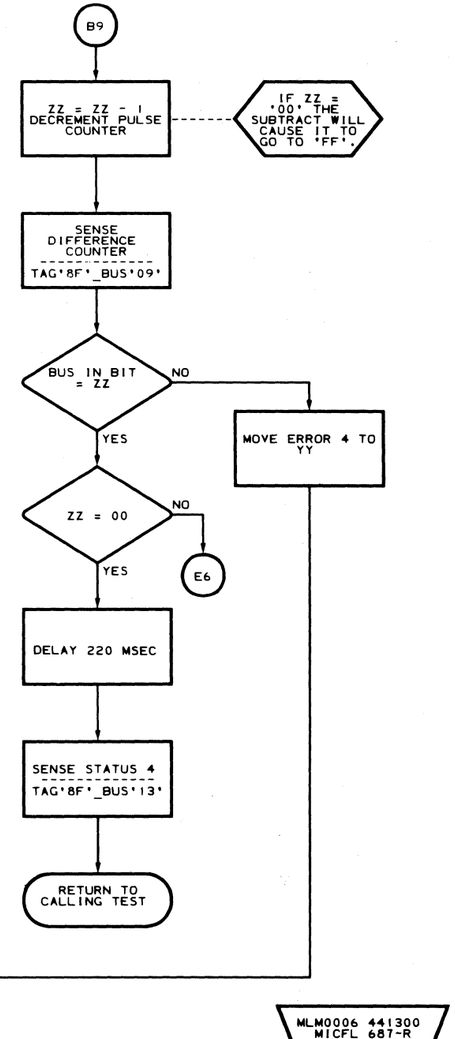


ROUTINE B9 – DYNAMIC SERVO TESTS







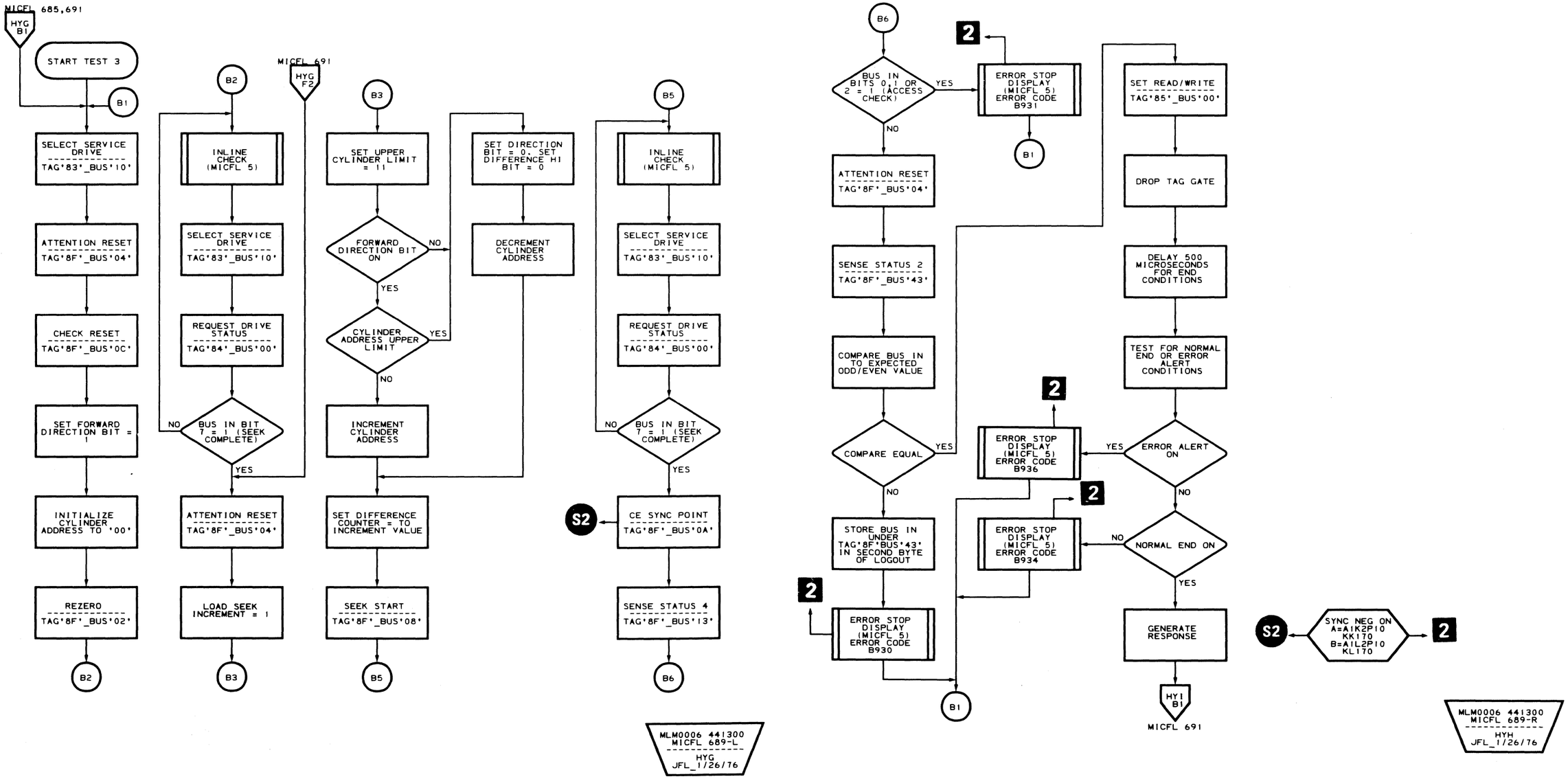


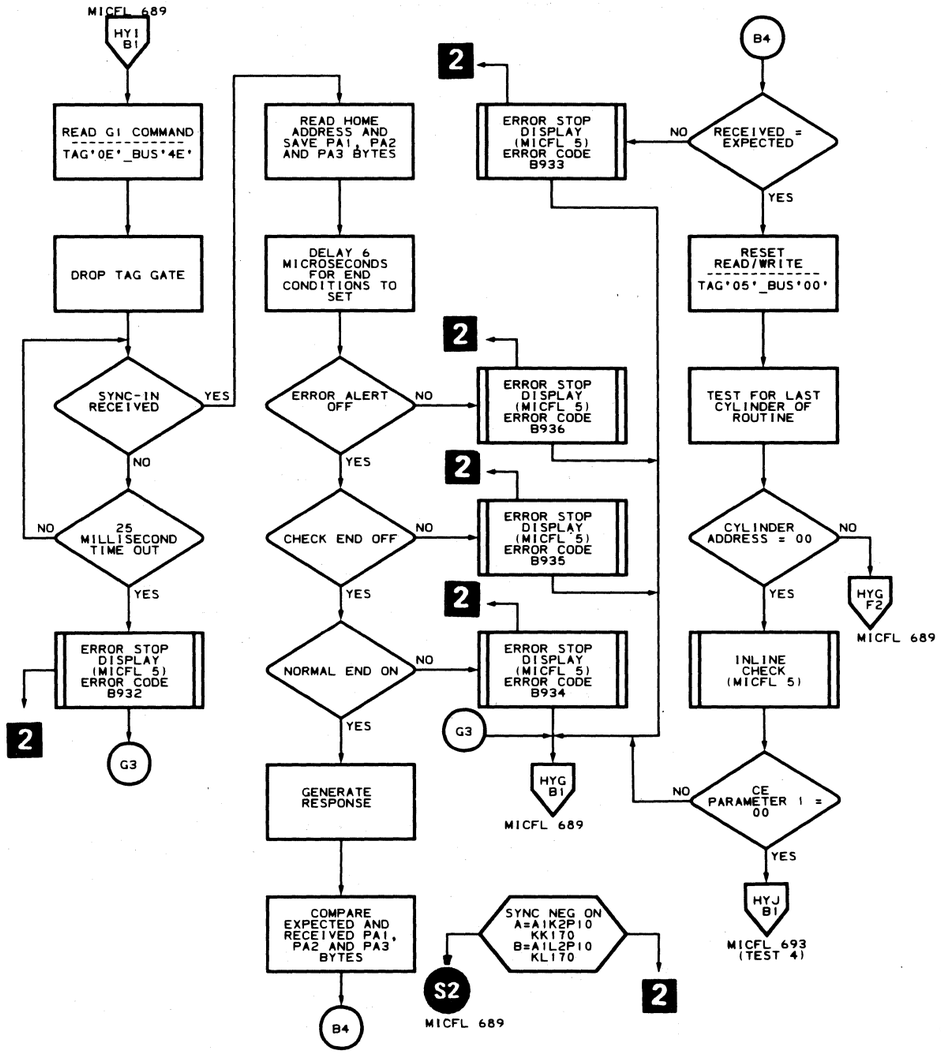
MLM0006 441300
MICFL 687-L
HYE
JFL_12/05/75

MLM0006 441300
MICFL 687-R
HYF
JFL_1/26/76

GC0685 Seq. 2 of 2	2358465 Part No.	441300 31 Mar 76				

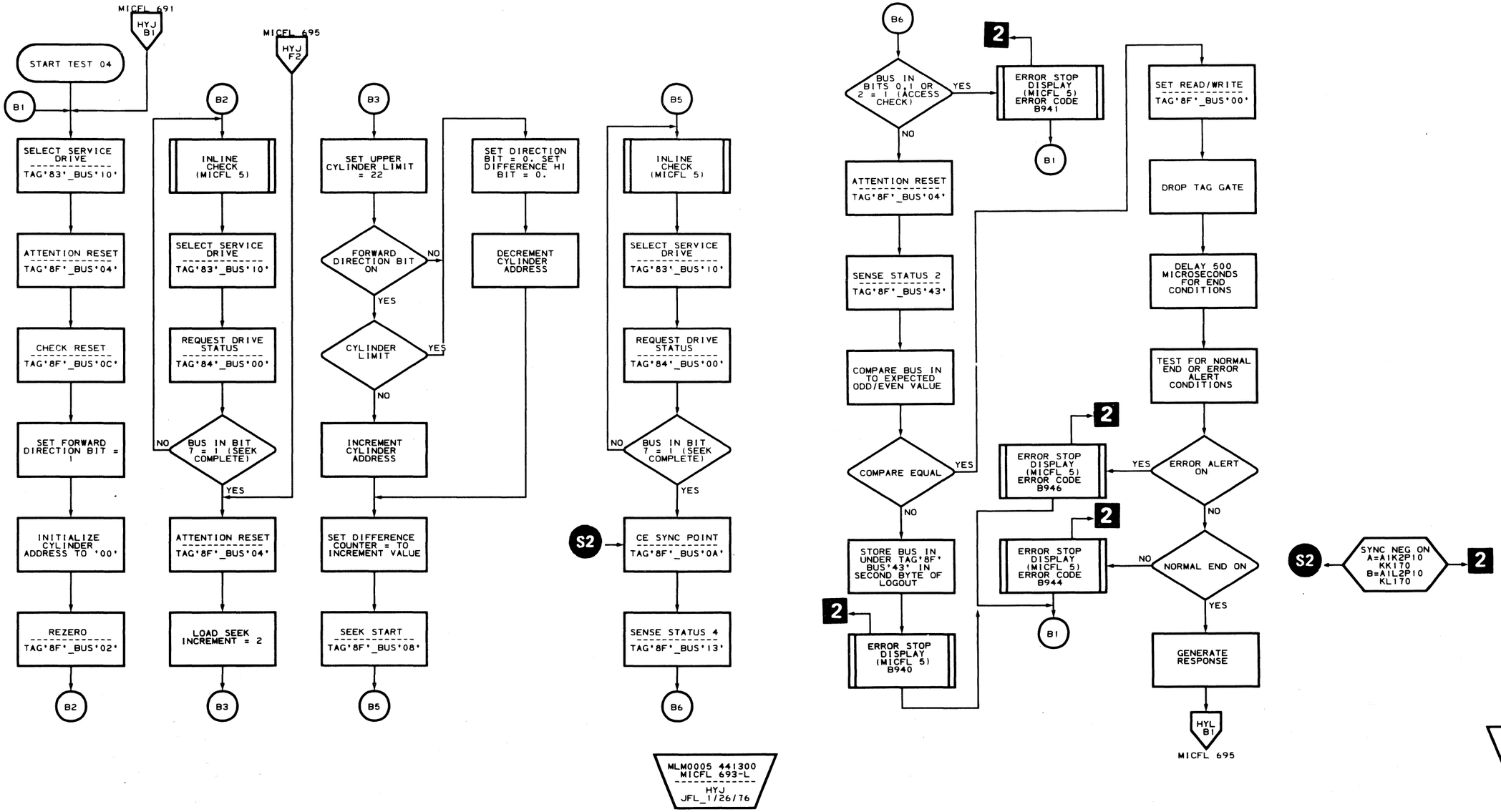
ROUTINE B9 – DYNAMIC SERVO TESTS



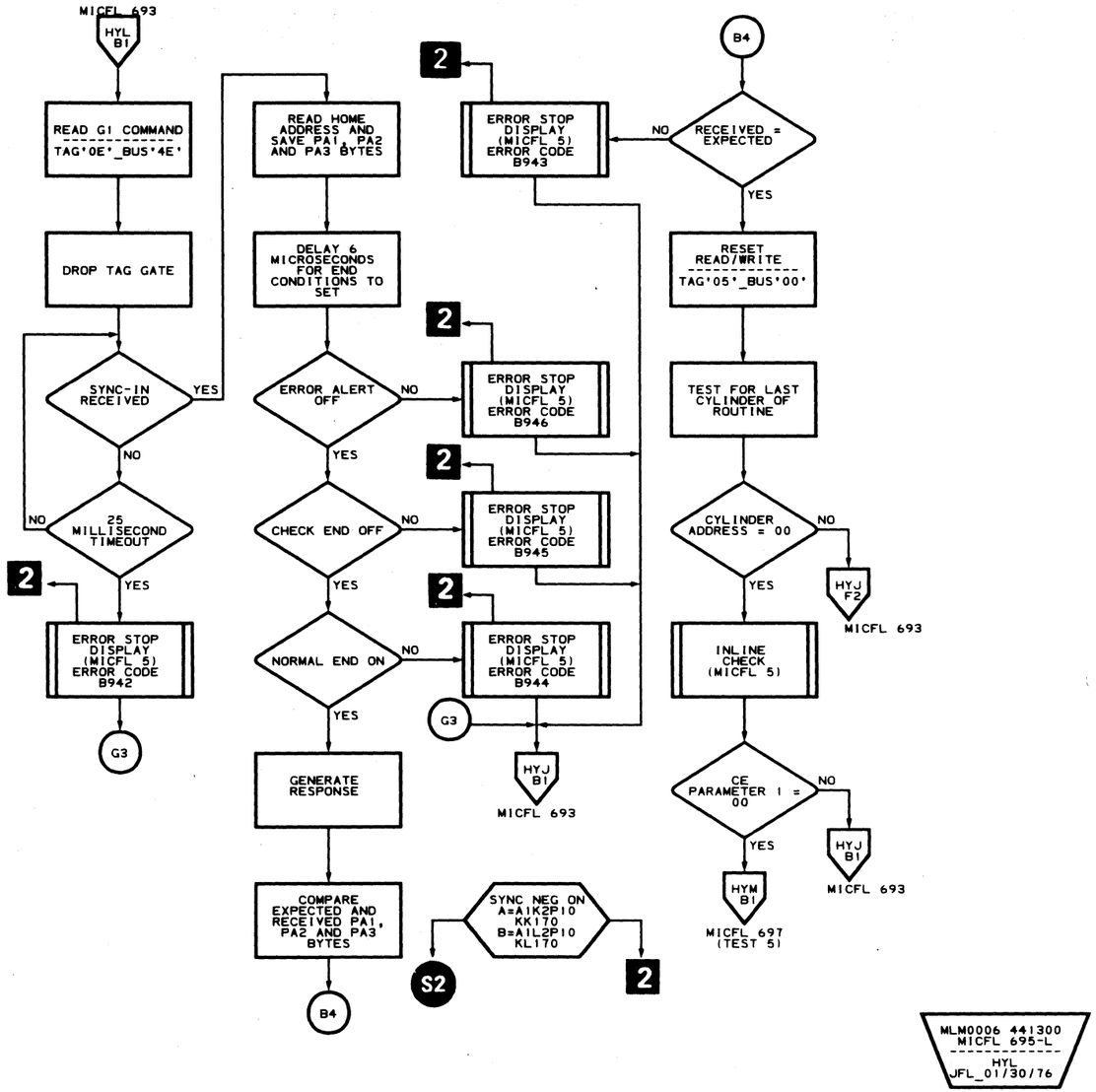


MLM0006 441300
MICFL 691-L
HY1
JFL_1/26/76

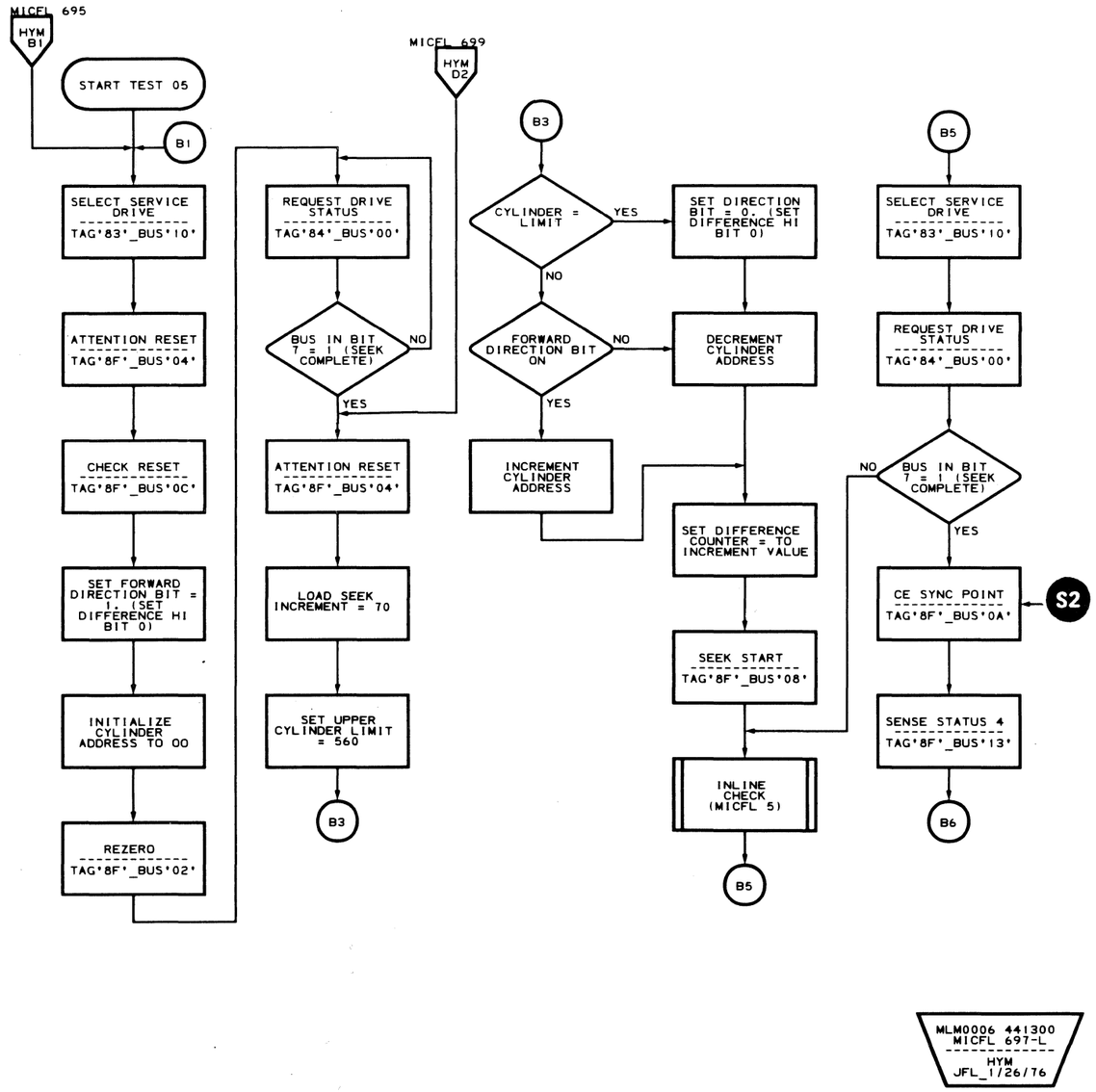
ROUTINE B9 – DYNAMIC SERVO TESTS

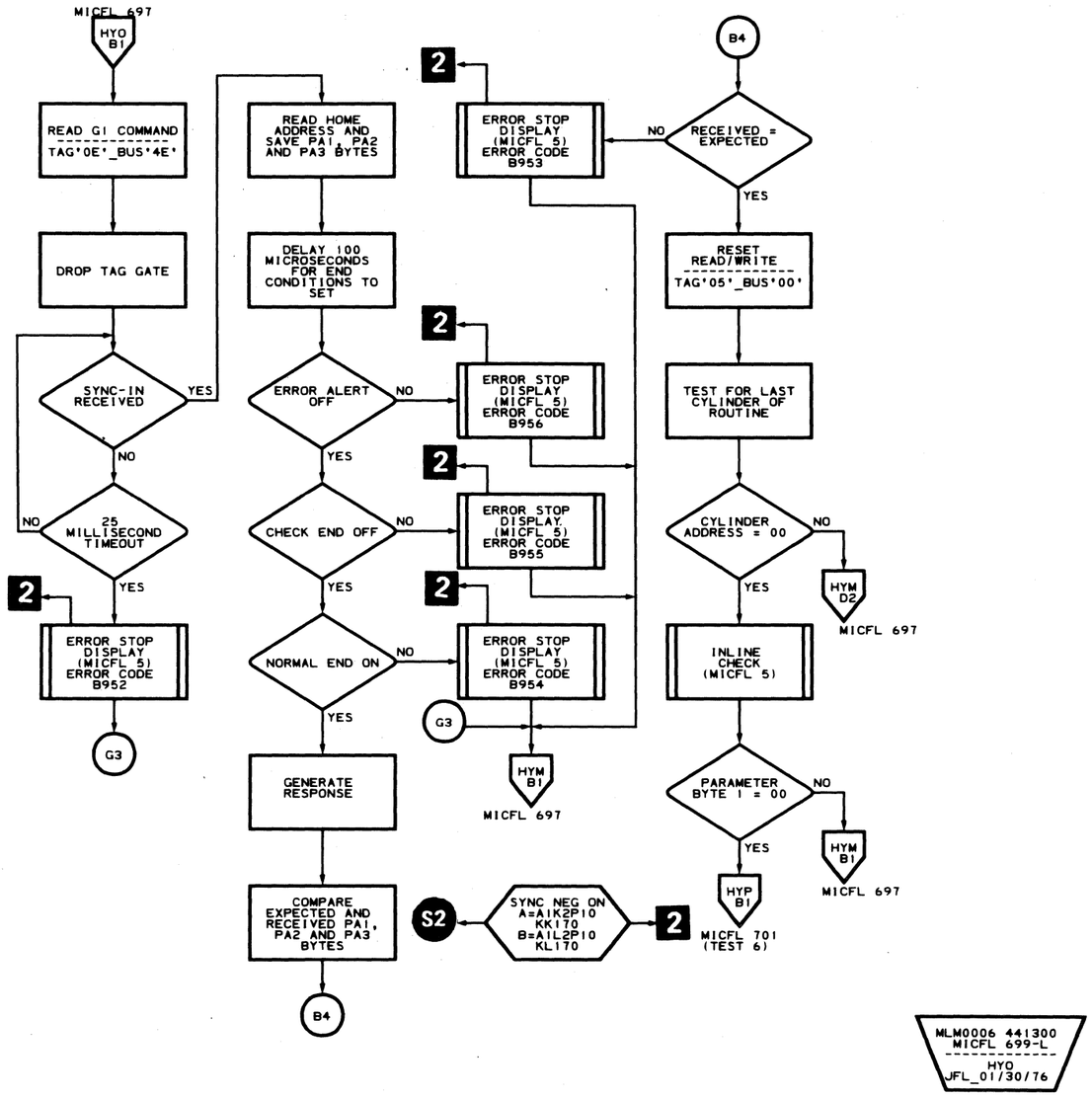


ROUTINE B9 – DYNAMIC SERVO TESTS

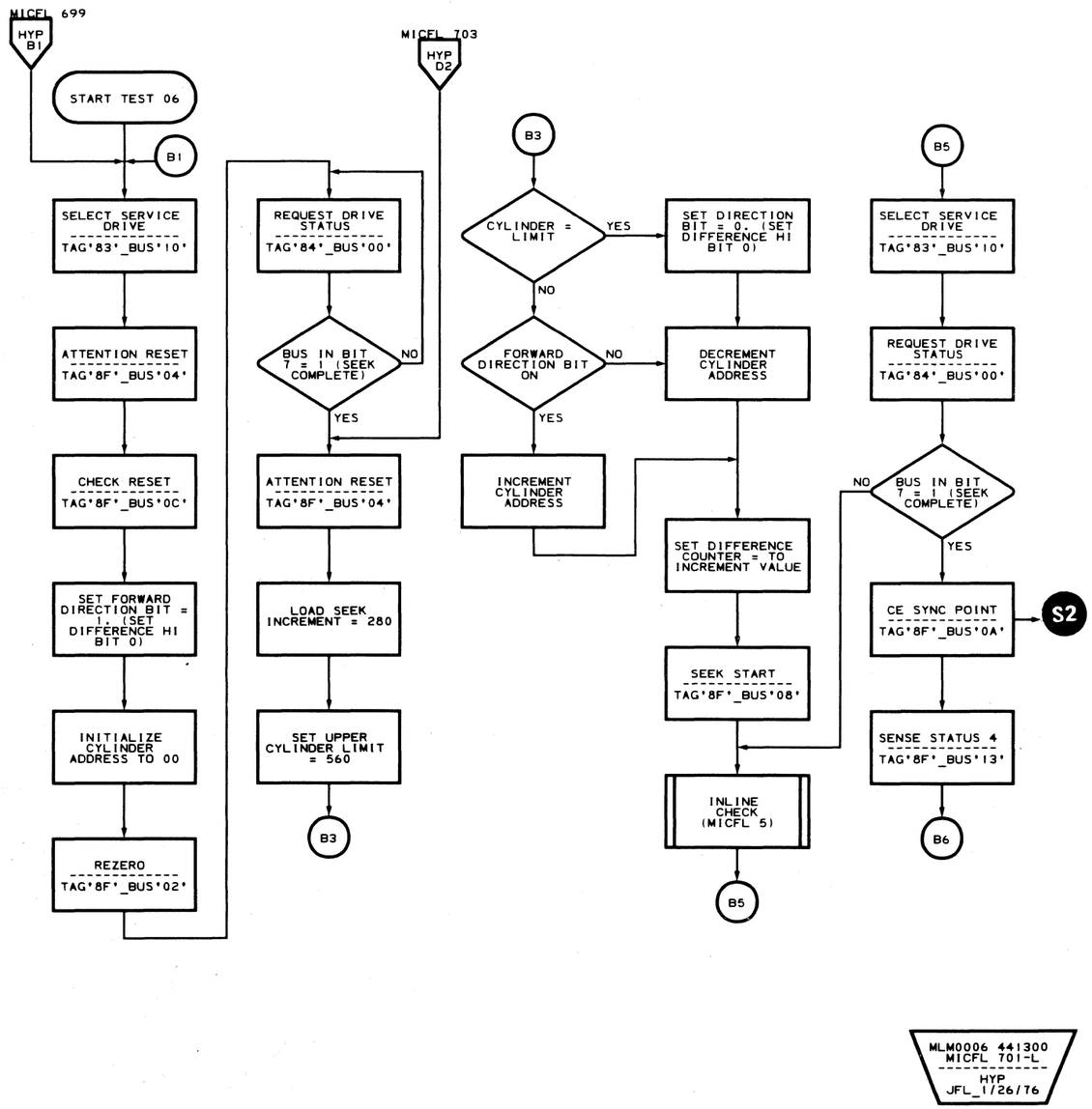


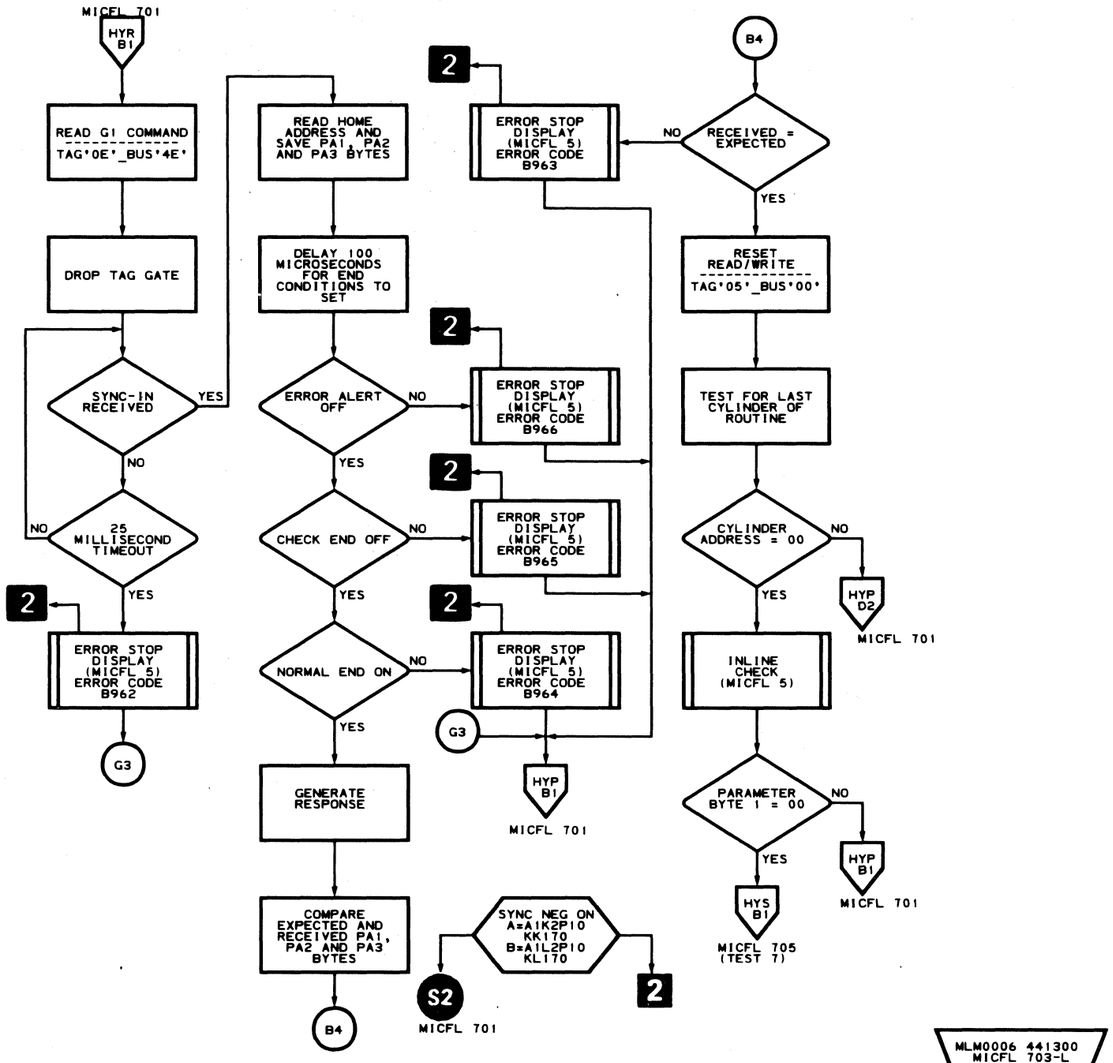
ROUTINE B9 – DYNAMIC SERVO TESTS





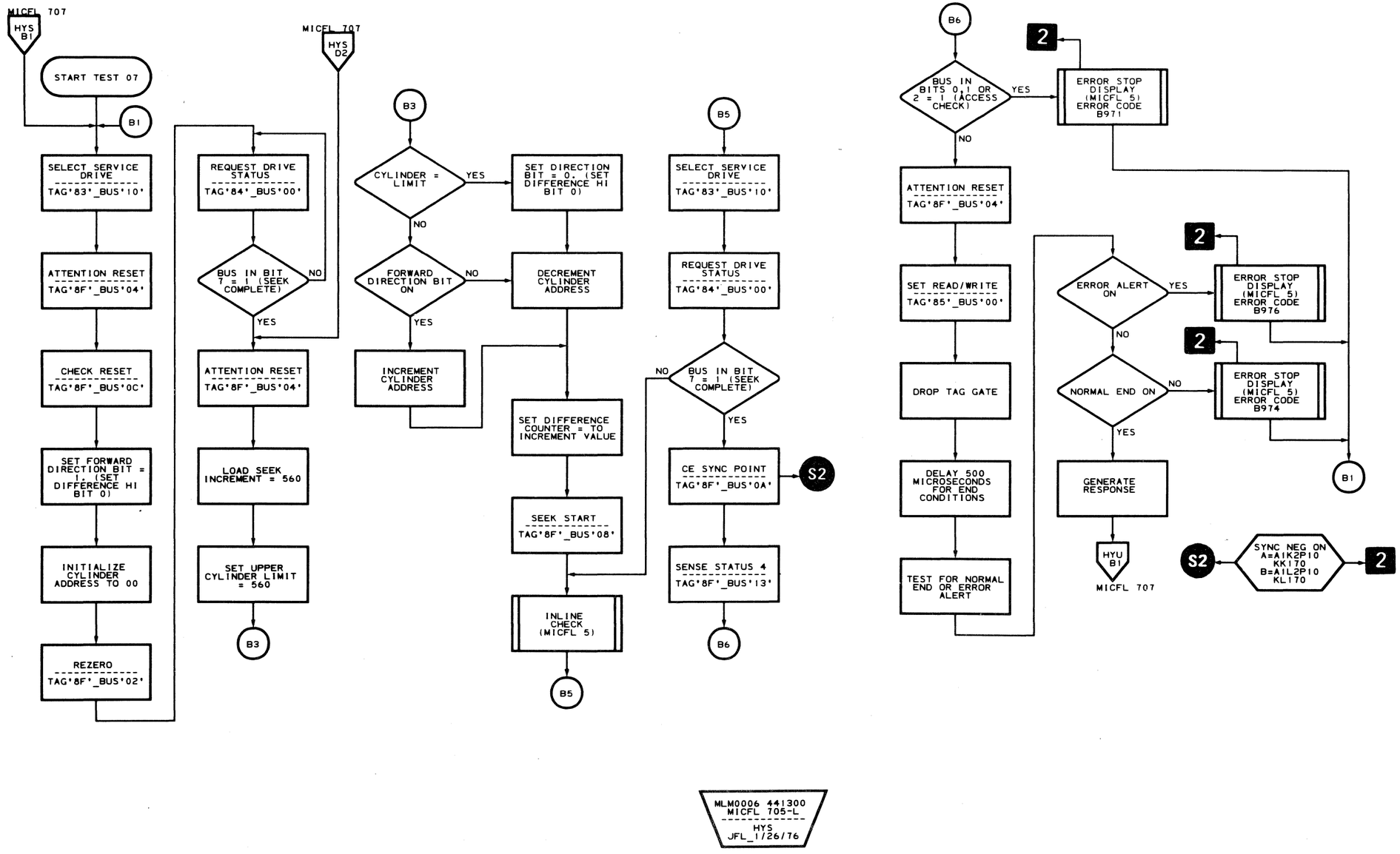
ROUTINE B9 – DYNAMIC SERVO TESTS

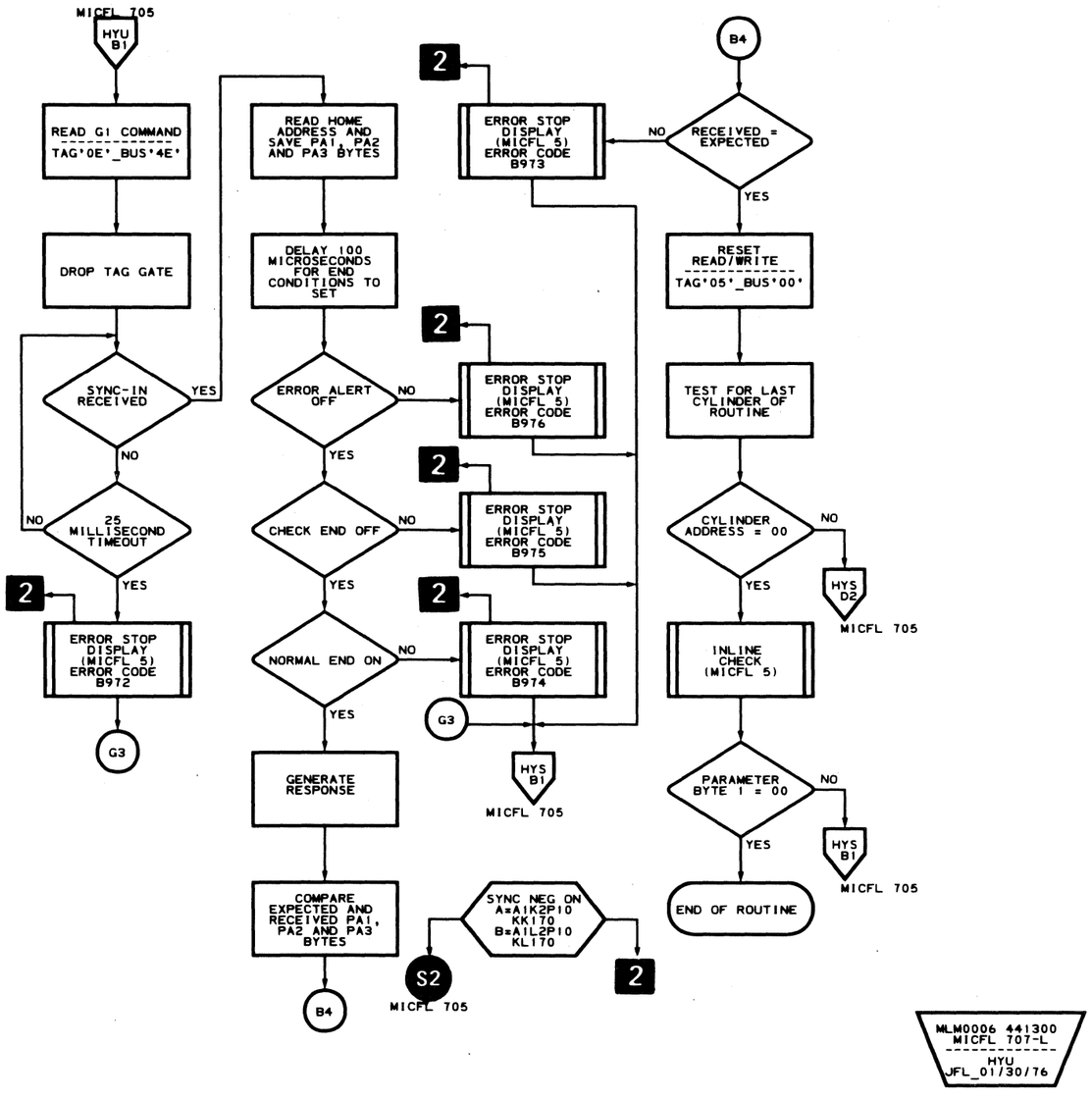




MLM0006 441300
MICFL 703-L
HYR
JFL_01/30/76

ROUTINE B9 – DYNAMIC SERVO TESTS





F
L

ROUTINE BA – 3350 HEAD DISK ASSEMBLY STATE ANALYSIS

DESCRIPTION

Routine BA analyzes Head Disk Assembly (HDA) sequencer failures by examining certain bits in the error status bytes in a prescribed sequence. Unique error numbers are produced, based upon the values contained within these bytes. Refer to the routine flowchart for detailed sequence of analysis of specific bytes/bits.

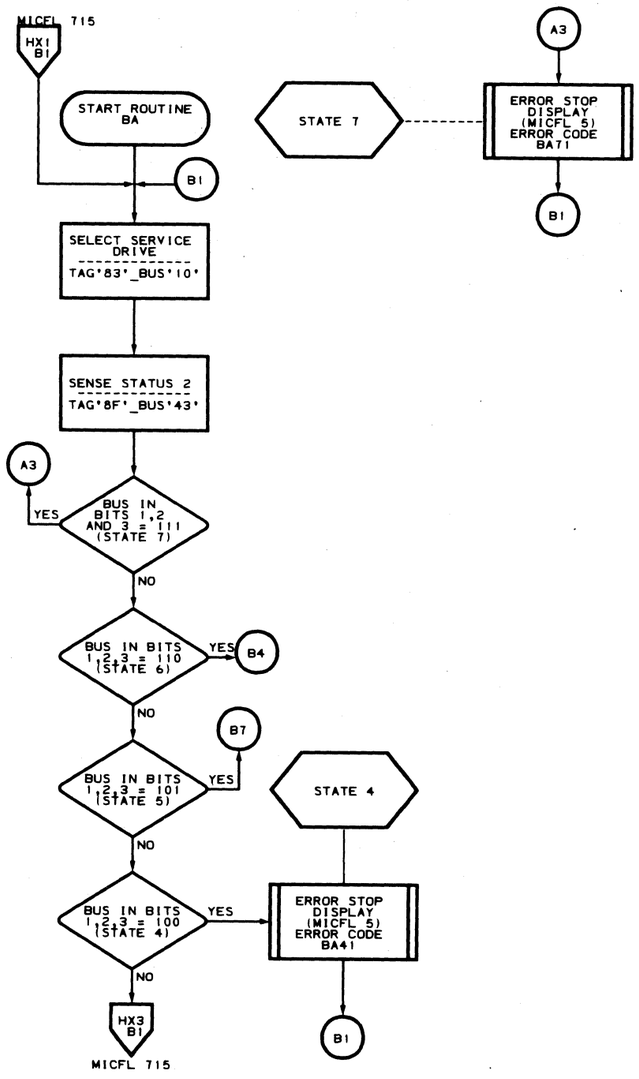
Sense Status 1	Tag '8F' Bus '83'	(Drive Checks Status)
Sense Status 2	Tag '8F' Bus '43'	(HDA Sequence Control)
Sense Status 3	Tag '8F' Bus '23'	(Load Switch Status)
Sense Satus 4	Tag '8F' Bus '13'	(Access Status)

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 76 for parameter entry.

ROUTINE BA – 3350 HEAD DISK ASSEMBLY STATE ANALYSIS MICFL 710

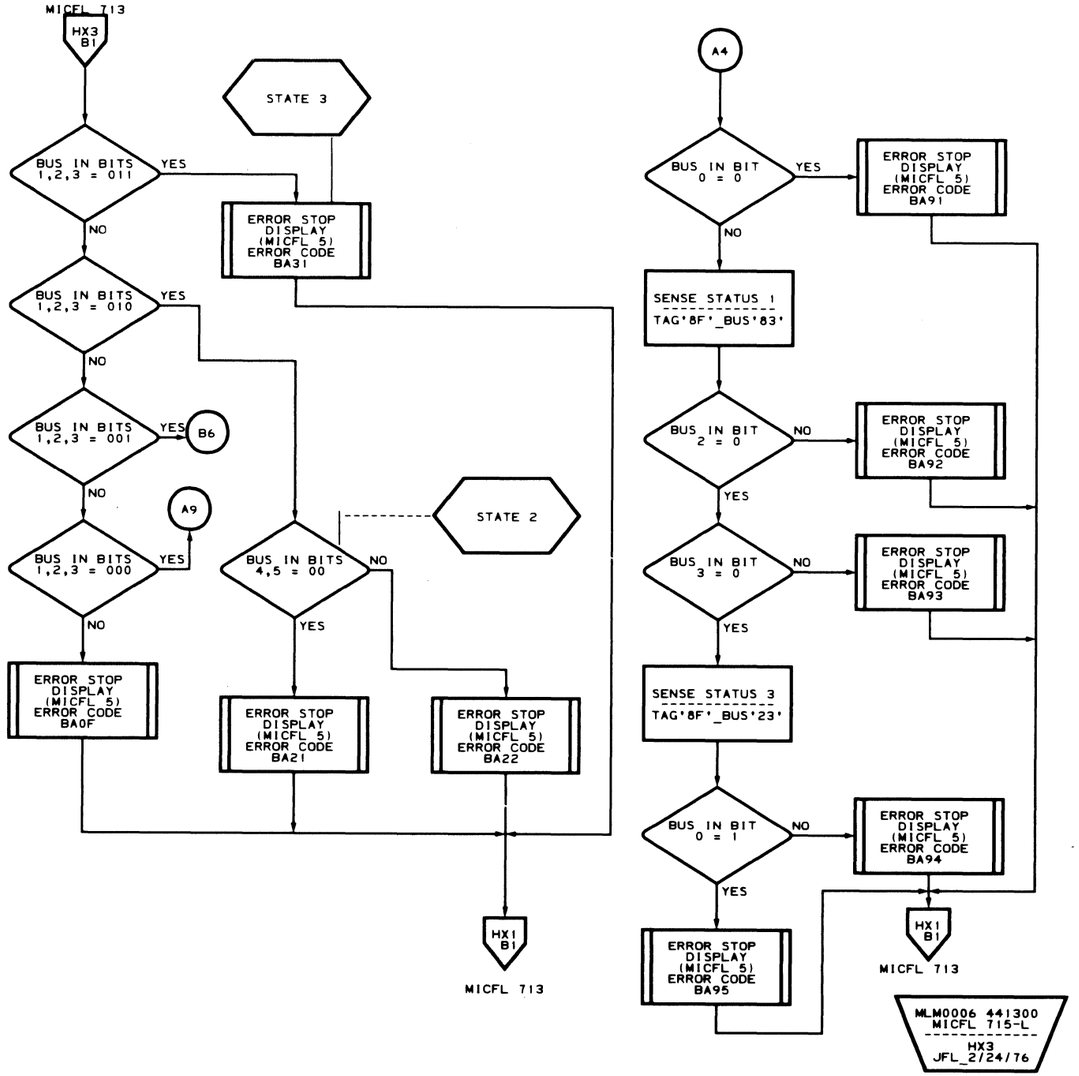
ROUTINE BA – HDA STATE ANALYSIS TESTS MICFL 713

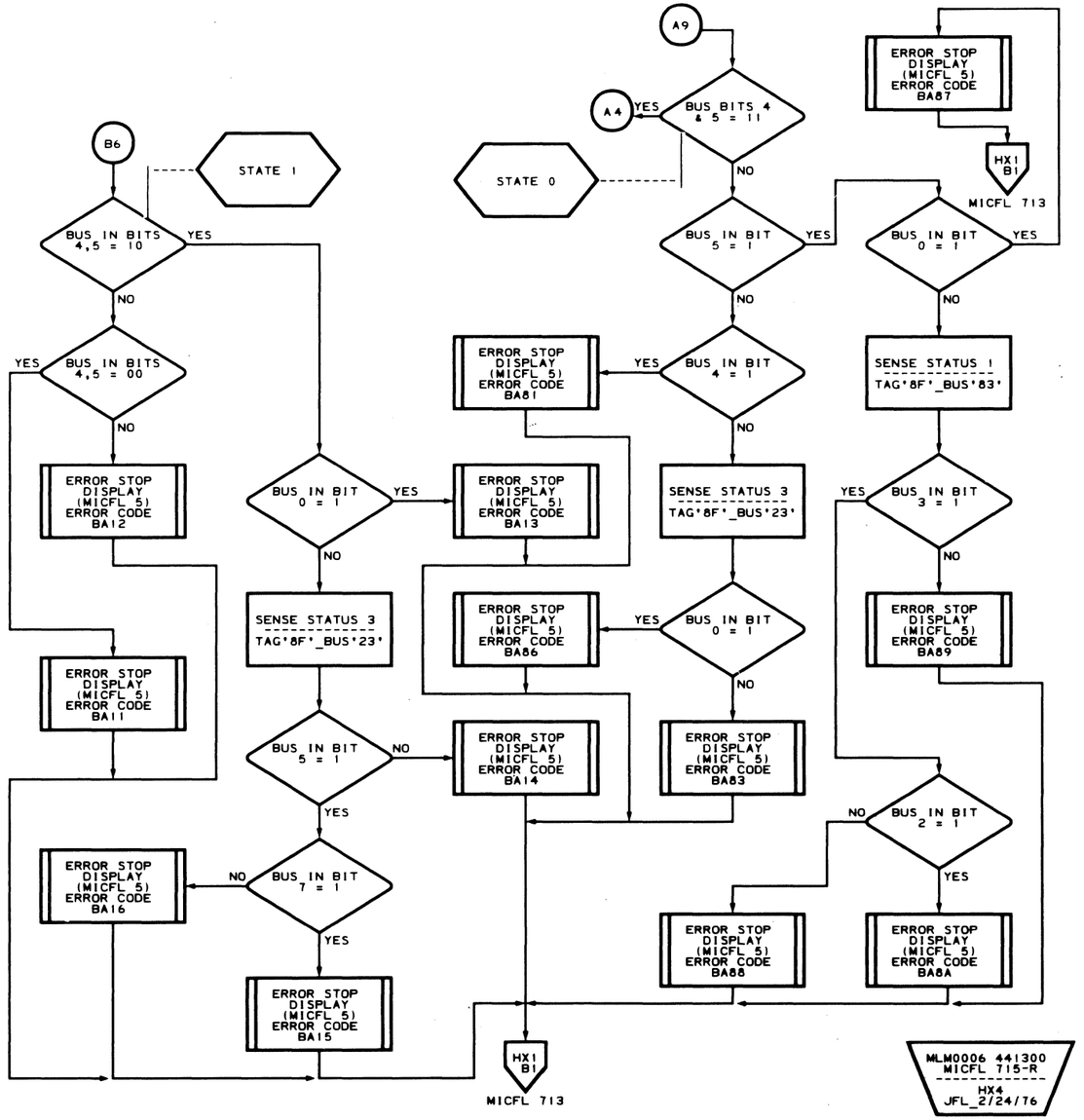


MLM0006 441300
MICFL 713-L
HX1
JFL)2/24/76

MLM0006 441300
MICFL 713-R
HX2
JFL_2/24/76

ROUTINE BA – HDA STATE ANALYSIS TESTS MICFL 715





ROUTINE BB - TRACK USED (TR) AND REORIENT COUNTER TESTS

DESCRIPTION

Routine BB checks the Pad-in-Progress function, the Track Used Counter, and the Reorient Counter circuits. At the end of the test a valid R0 Data field is written. Mode Selection is the final test and must be selected in order to test the function.

Test 01. Drive Write Padding

Test 01 selects a CE drive, Writes G3, looks for Pad-in-Progress, waits for at least 17 milliseconds for the padding to be completed, then checks to see that Pad-in-Progress is not present, and that Pad Complete is active.

Test 02. Reorient Counter

Test 02 examines the Reorient Counter. The test reads G1, then senses the Reorient Counter searching for bit 5 (Index field) within a specific time. The test then reads G1 searching for the first Sync In within a specific time, and verifies that the PA bytes are valid.

The test then reads G1, then writes a 1-byte G3 field and senses the Reorient Counter looking for bit 6 (of the AM field) within a specific time, and reads G3 to verify the field is a G3 field.

The test checks Index field for early or late start. It measures the length of the AM field and determines if it started early with respect to Index.

Test 03. Verify Track Used Counter Zero Reset

Test 03 verifies, in the Native Mode, that the Track Used Counter can be reset to zero at Index time by reading HA, writing a 10-byte G3 field, and then checking the Track Used Counter for '0000'. In the 3330 Compatibility Mode, the Track Used Counter is tested by reading the HA and then checking the Track Used Counter for '0000'.

Test 04. Verify Track Used Counter Zeros

Test 04 verifies that the Track Used Counter can be loaded with zeros by reading HA, writing a 10-byte G3 field which contains a field of '0000F0', reading HA, then reading a truncated 1-byte G3 field. This loads the zeros into the Track Used Counter, where it is checked for '0000'.

Test 05. Verify Track Used Counter For Ones

Test 05 verifies that the Track Used Counter can be loaded with ones by reading HA, writing a 10-byte G3 field which contains a field of '7FFE60', reading HA, then reading a truncated 1-byte G3 field. This loads the ones into the Track Used Counter where it is checked for 'FEFE' on Bus In. This is equivalent to 'FFFC' in the Track Register.

Test 06. Force Track Used Counter Check

Test 06 forces a Track Used Counter Check by writing a 10-byte G3 field, containing a data pattern that results in a Track Used Counter error. The field is then read as a truncated G3 field of 1 byte. The Track Used Counter Check and Controller error are expected to be on. The test then issues a Reset Controller and verifies that the errors are reset.

Test 07. Track Used Counter Serialization - Part 1

Test 07 verifies proper operation of the Track Used Counter during the serialization of the unique Track Used Counter pattern '3F0E20'. Data pattern results in a Track Used Counter pattern of '7E88XX' following the writing of a second G3 field on the track. This verifies that the Track Used Counter will run after being loaded.

Test 08. Track Used Counter Serialization - Part 2

Test 08 verifies the proper operation of the Track Used Counter during the serialization of the unique Track Used Counter pattern '40F0B0'. This data pattern results in a Track Used Counter pattern of '826AXX' following writing of a second G3 field on the track. This verifies that the Track Used Counter will run after being loaded.

Test 09. Track Used Index

Test 09 verifies that Track Used Index is working properly by reading HA, then writing a 13,300-byte G2 field, checking for Check End, Track Used Overrun, and Index Alert at the proper time.

Test 0A. Write Valid R0 Record

Test 0A is a utility used for cleaning up the track prior to terminating the linked series diagnostics. It reads the HA, then writes a R0 Count field and R0 Data field consisting of 8 bytes of '00'.

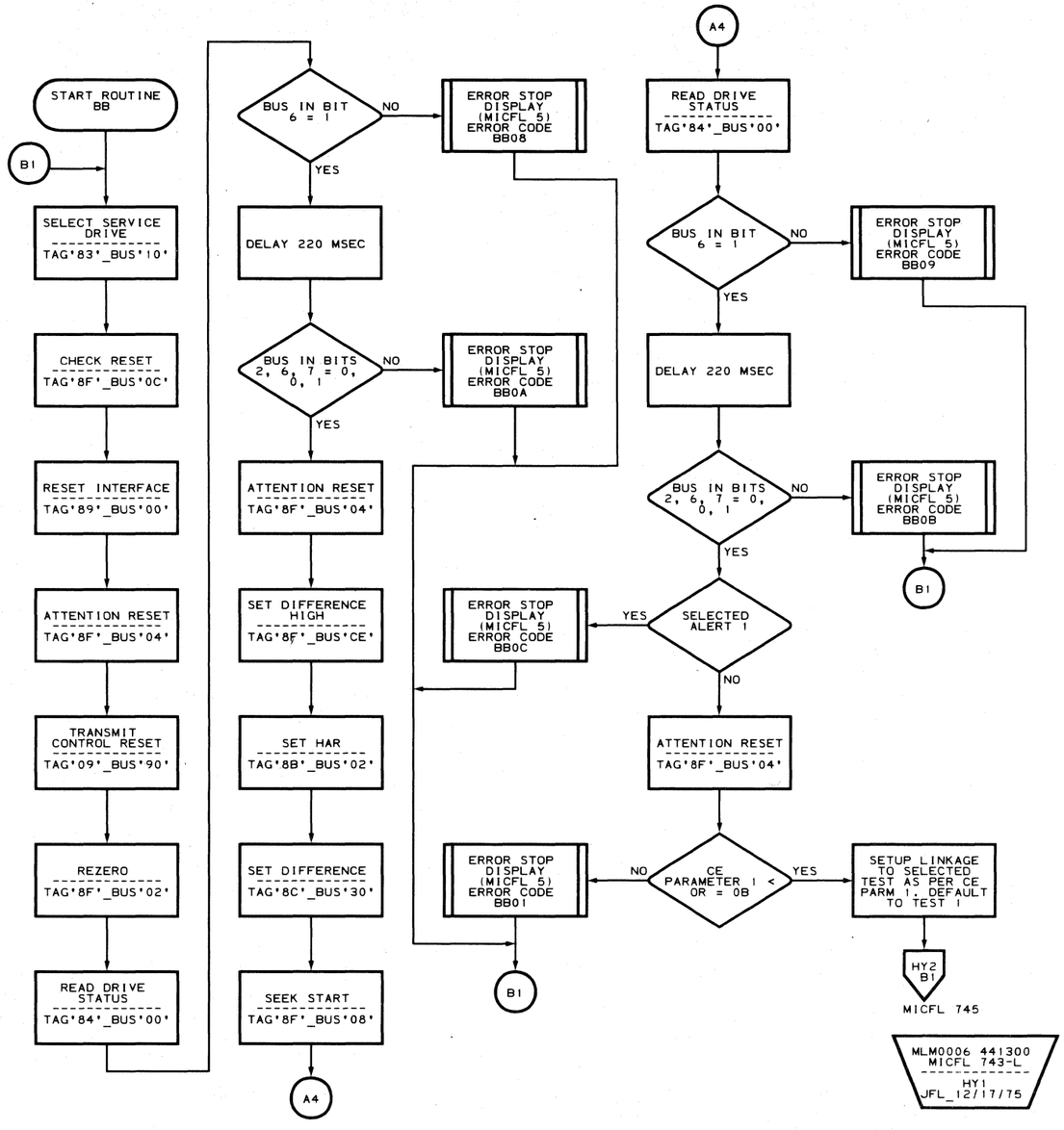
Test 0B. Drive Mode Check

Test 0B checks for compatibility between the hard wired Mode Control Code presented on the Interface Bus and that which is entered by the field engineer using the test options.

OPERATING PROCEDURE

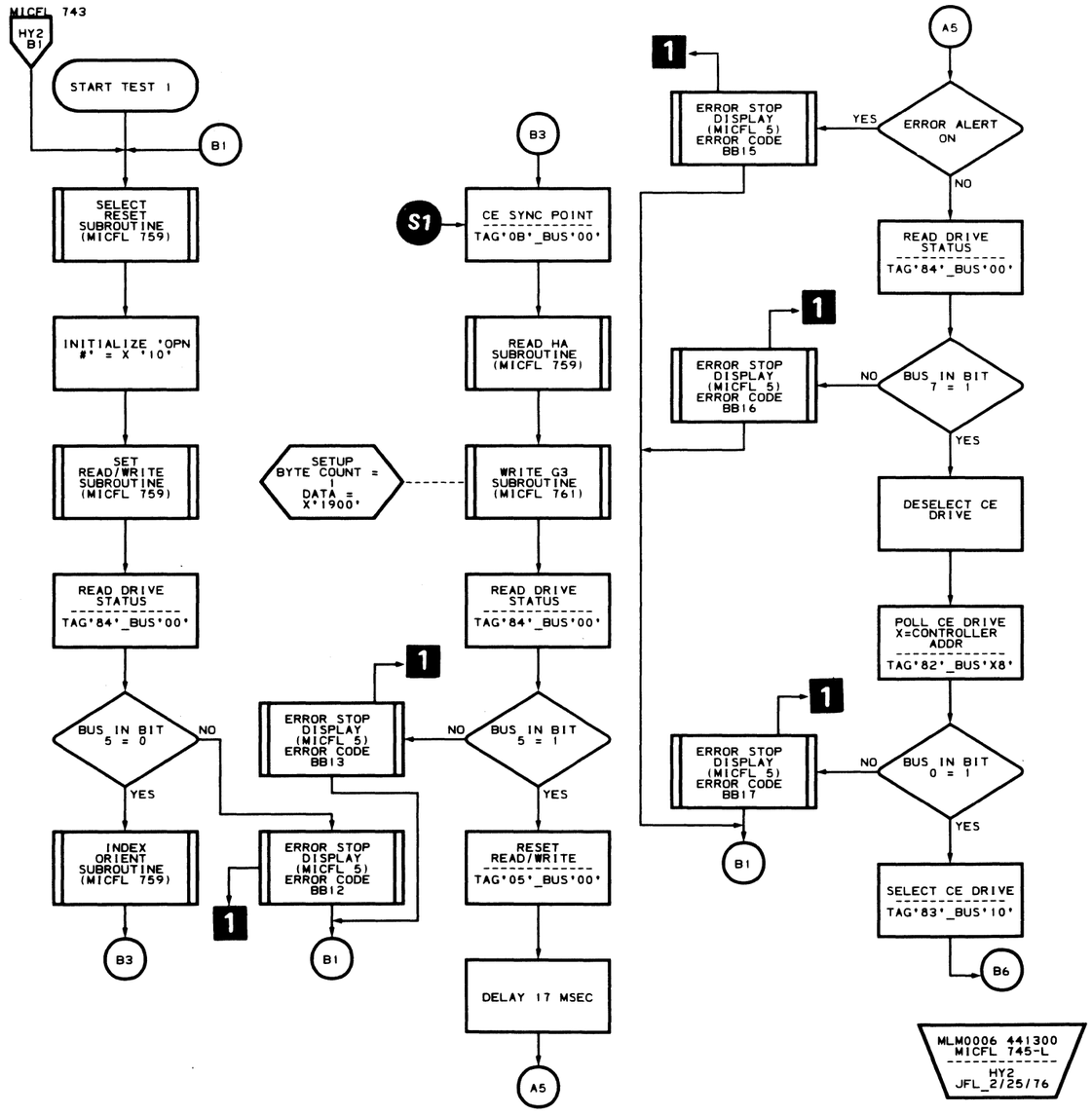
- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 80 for parameter entry.

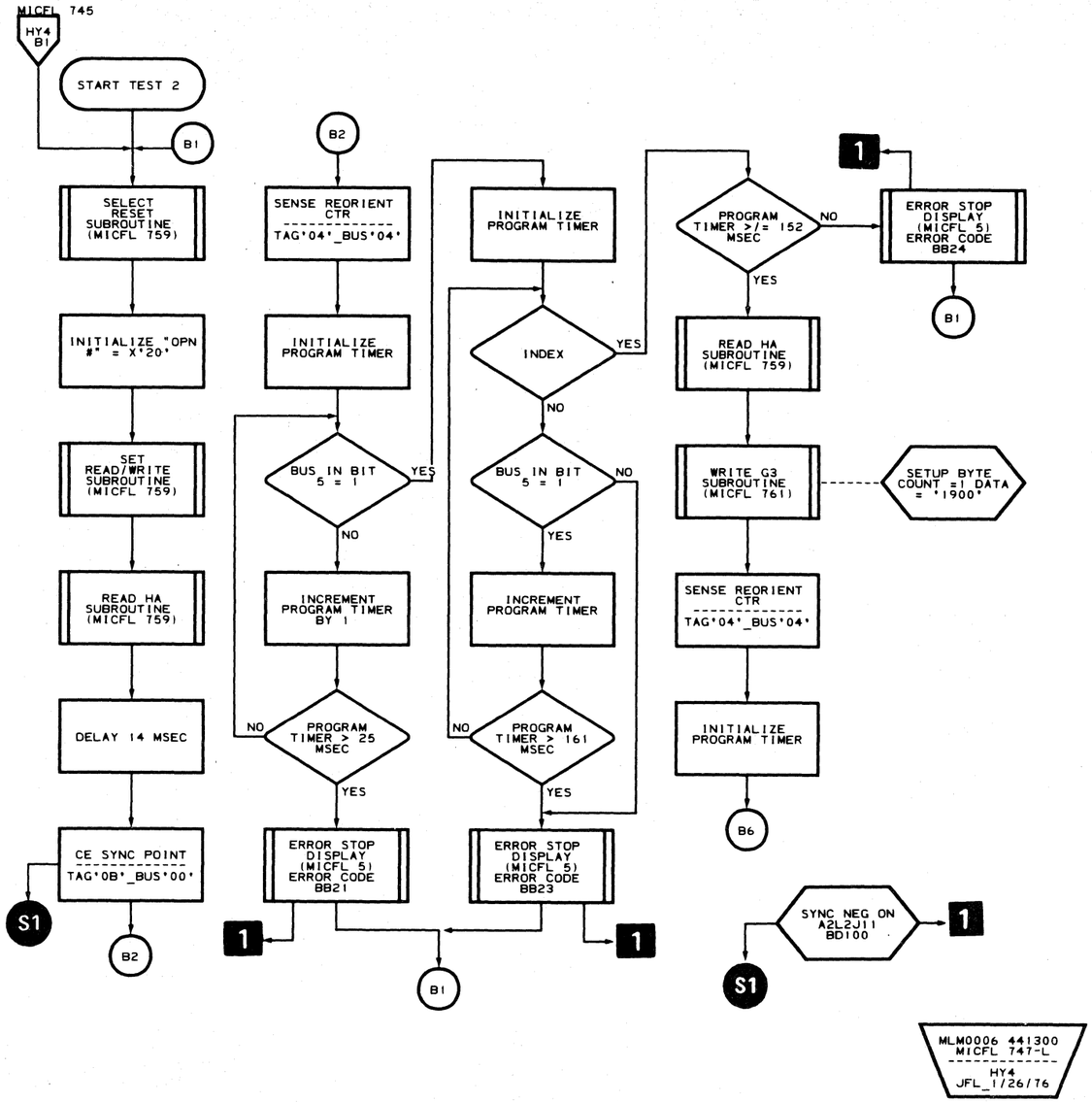
ROUTINE BB – 3330 COMPATIBILITY MODE AND OTHER SPECIAL TESTS MICFL 743

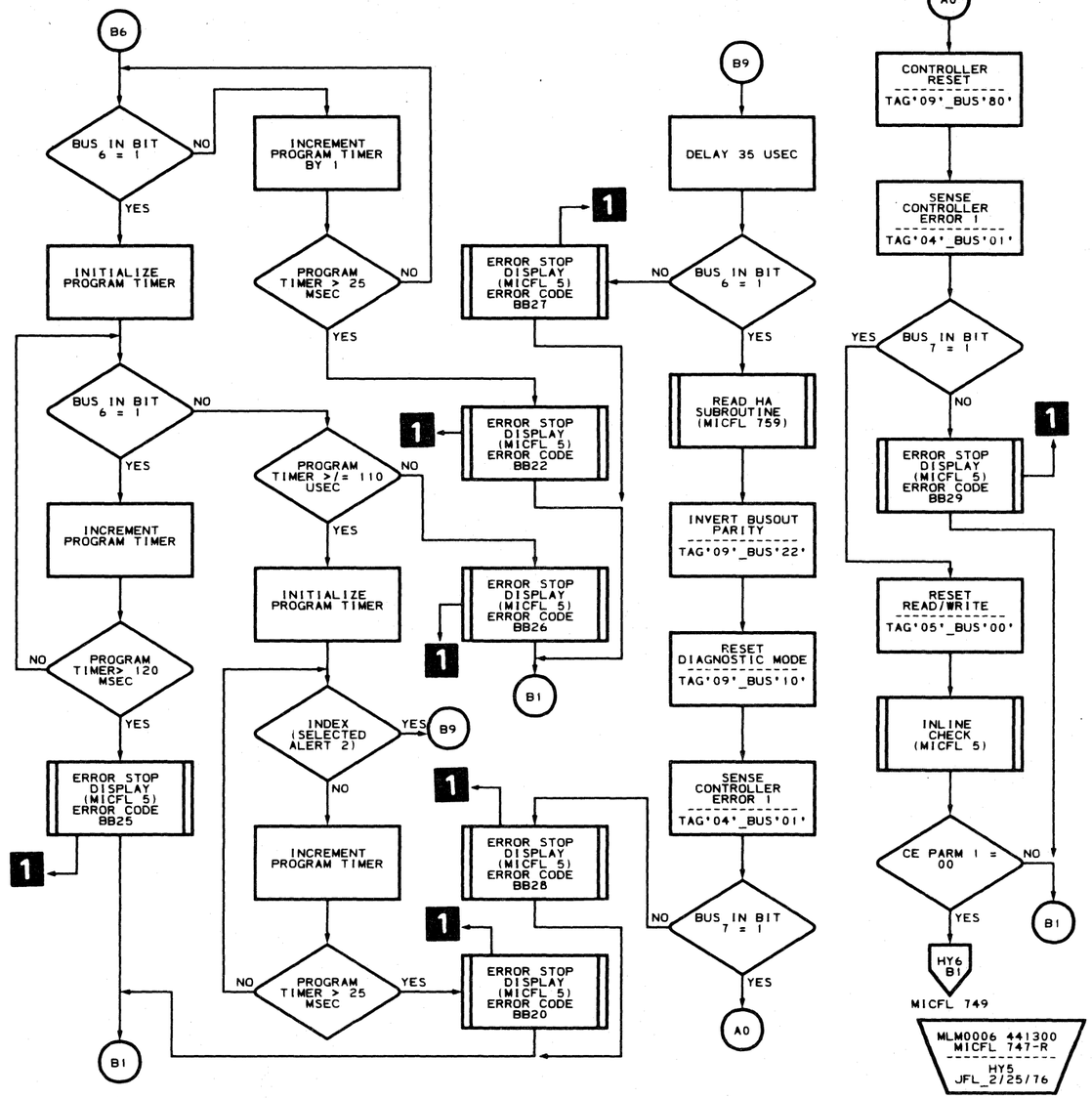


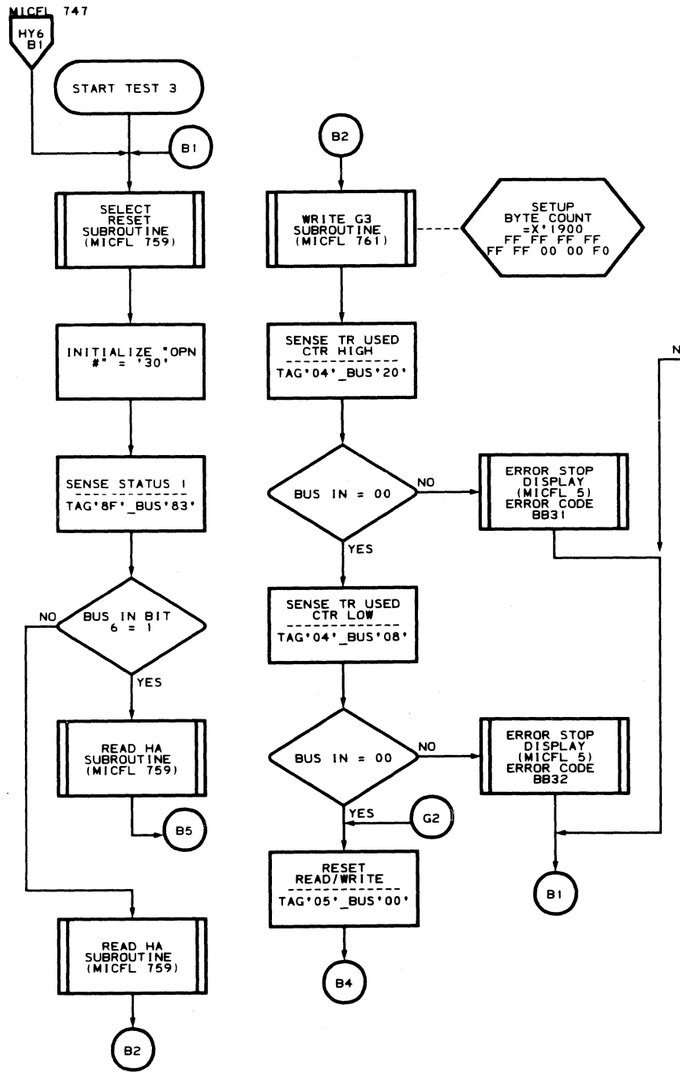
ROUTINE BB – 3330 COMPATIBILITY MODE AND OTHER SPECIAL TESTS MICFL 743

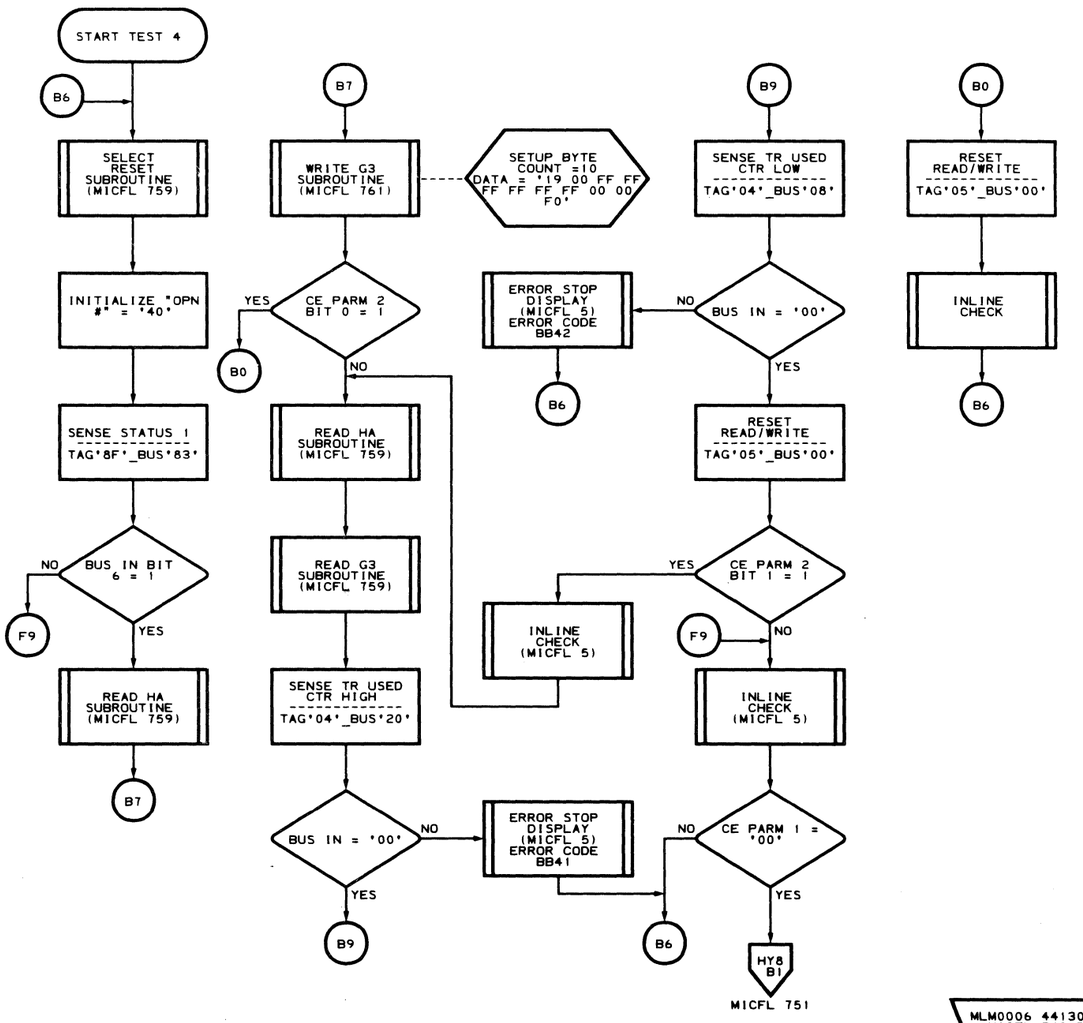
ROUTINE BB – 3330 COMPATIBILITY MODE AND OTHER SPECIAL TESTS

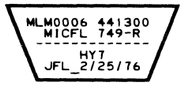


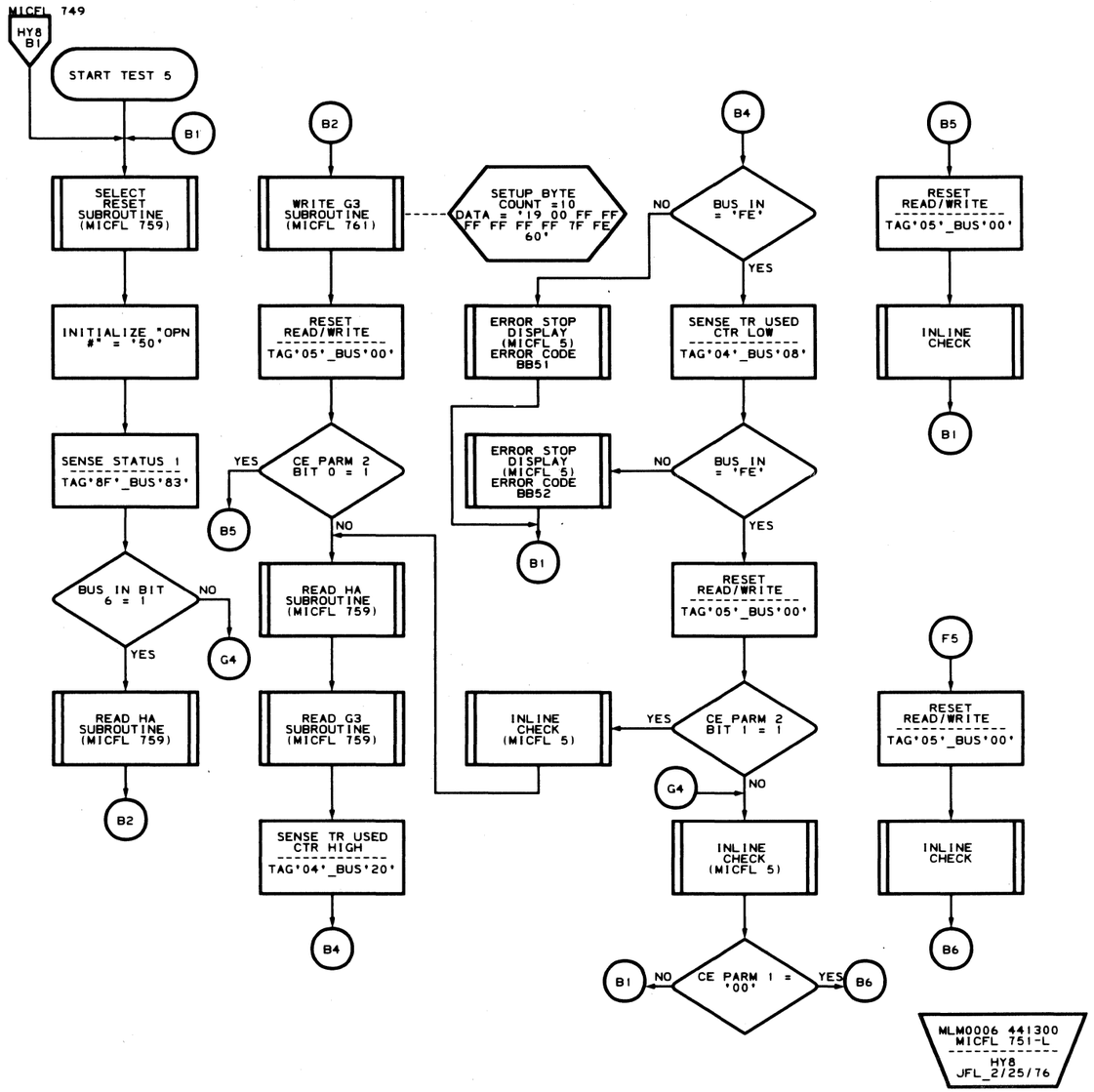


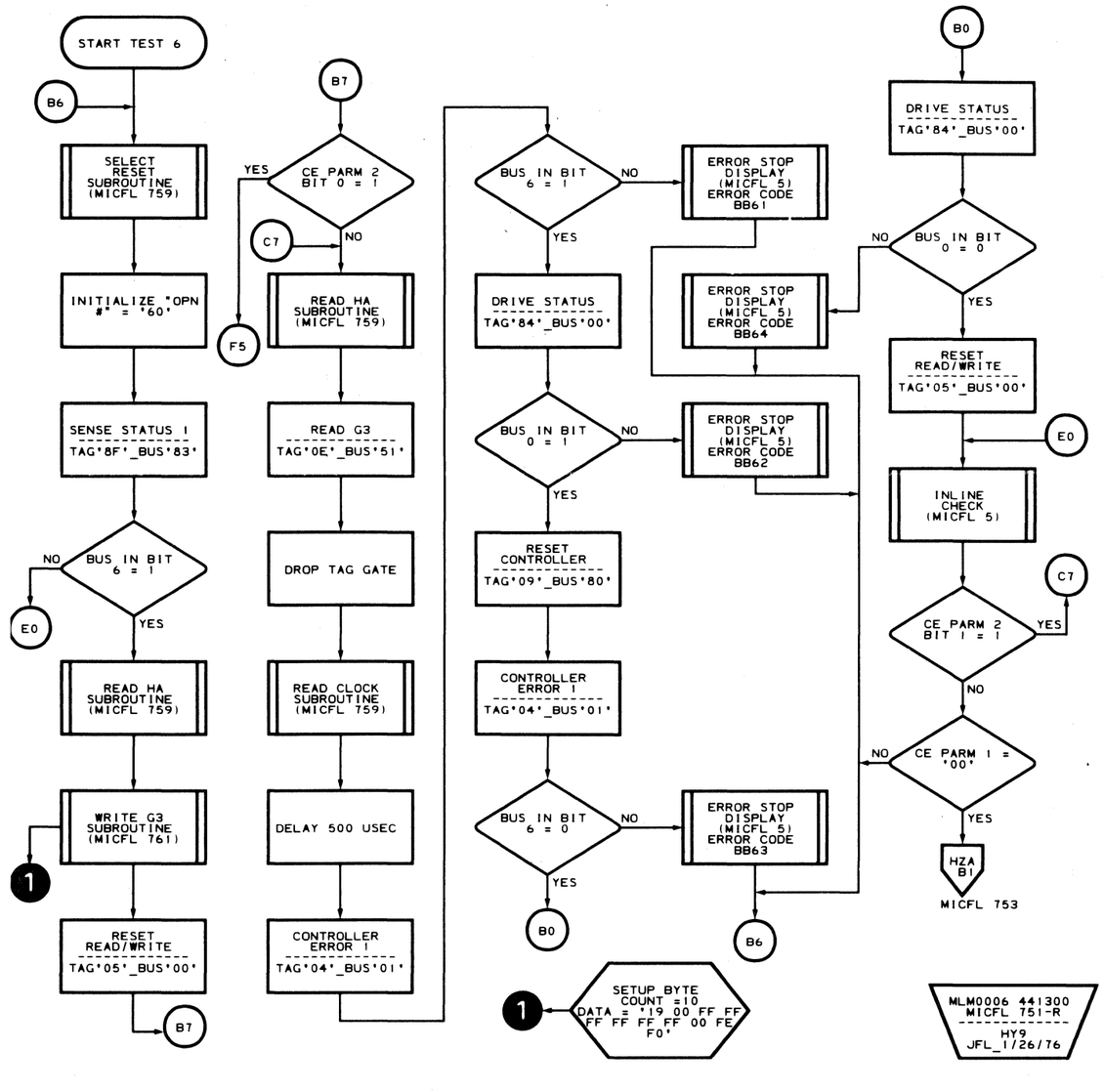




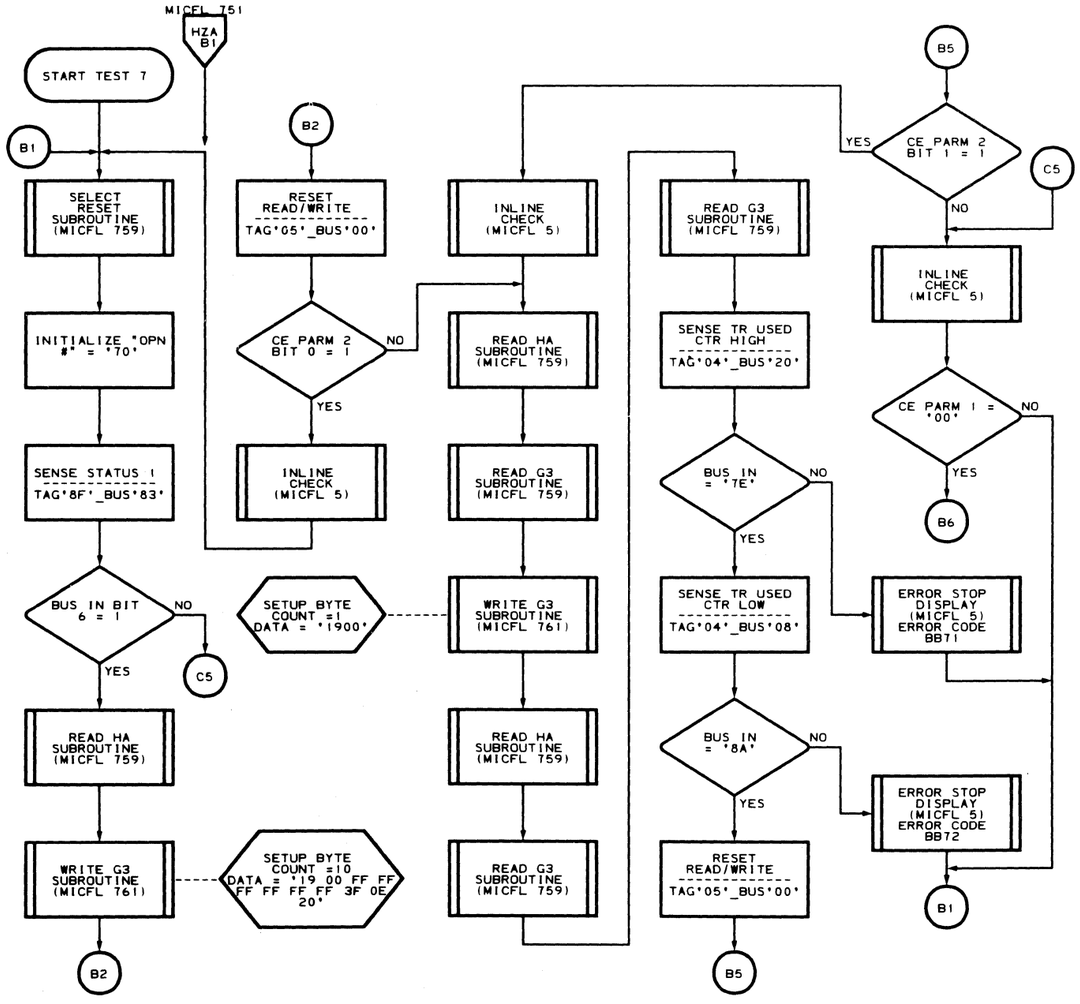


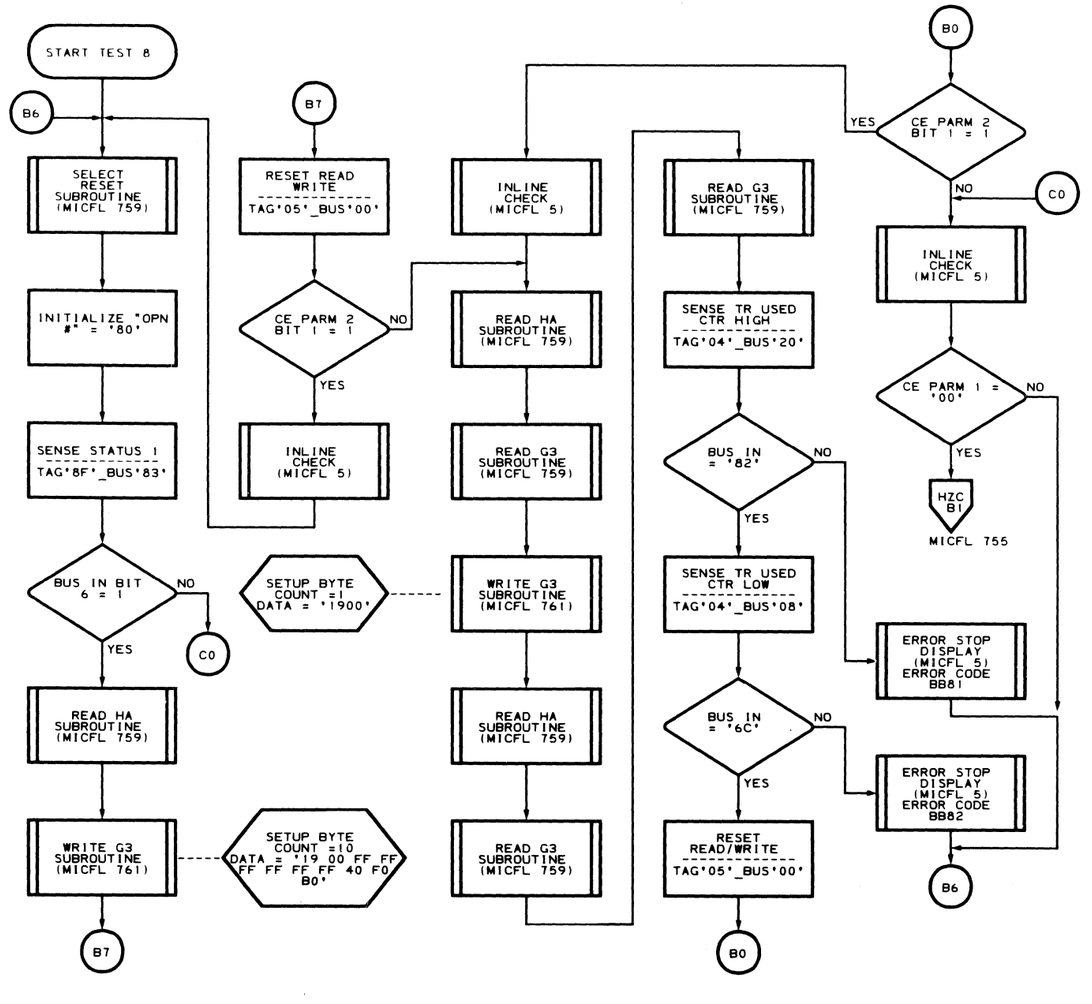


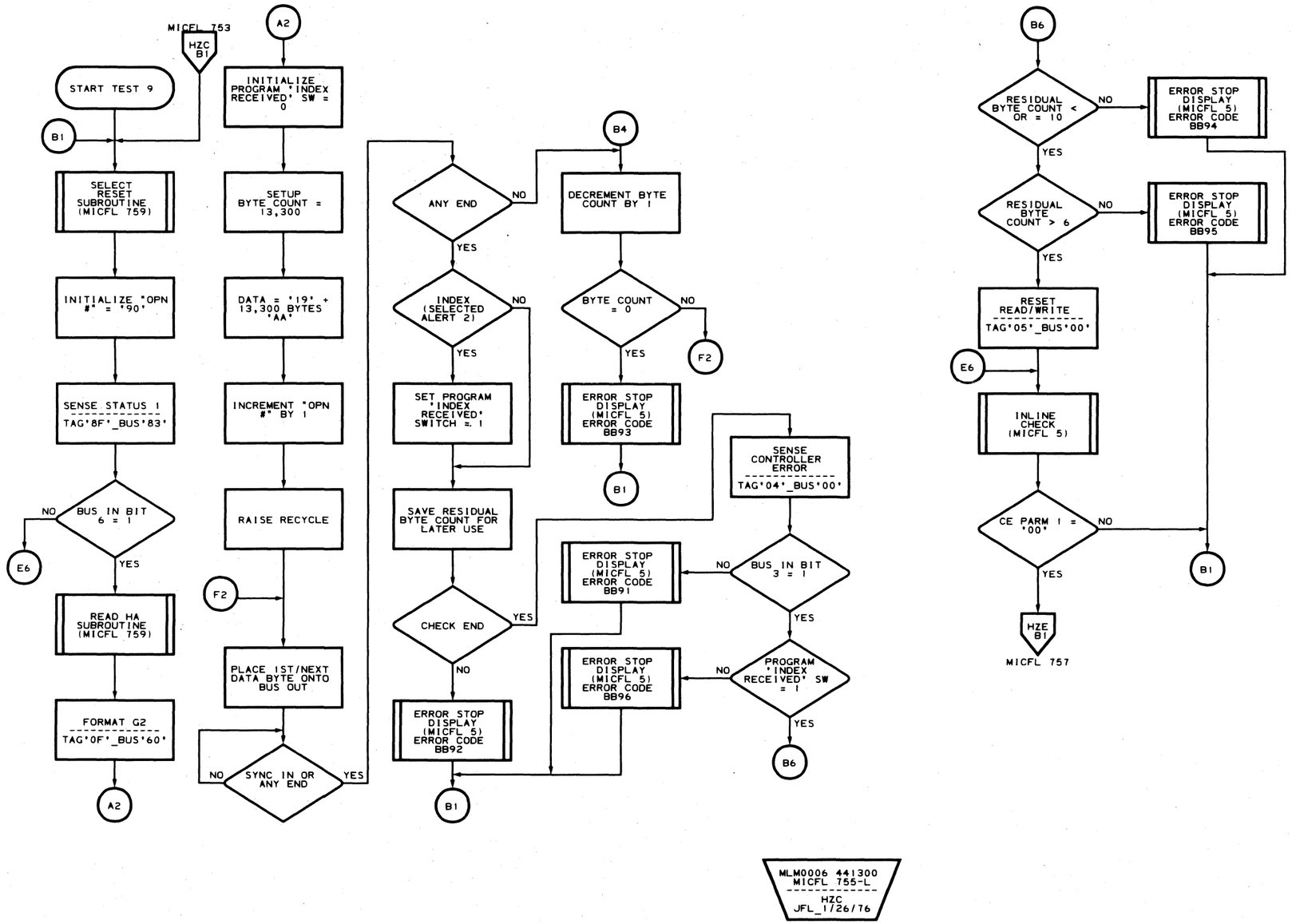




ROUTINE BB – 3330 COMPATIBILITY MODE AND OTHER SPECIAL TESTS



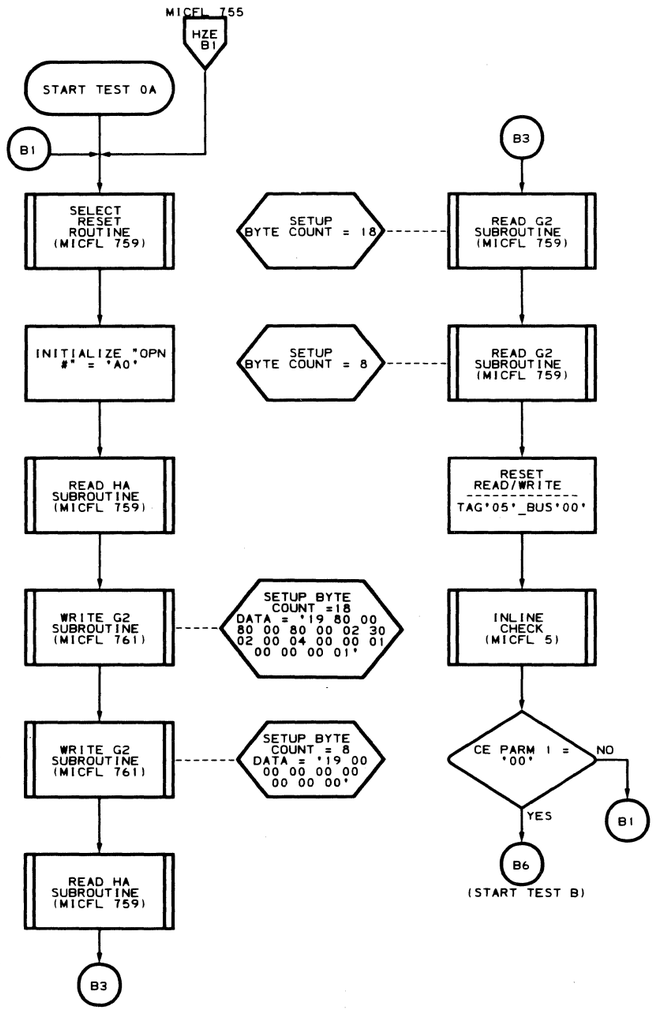


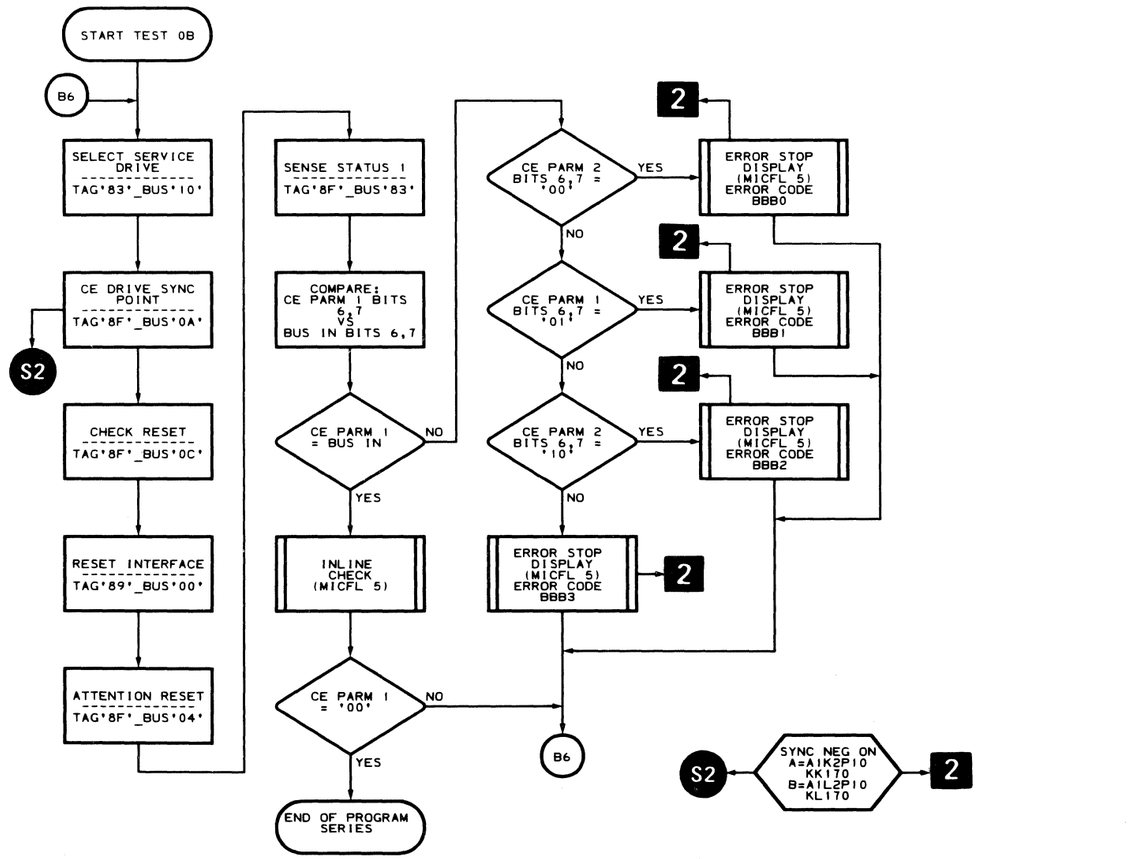


MLM0006 441300
MICFL 755-L
HZC
JFL_1/26/76

MLM0006 441300
MICFL 755-R
HZD
JFL_2/25/76

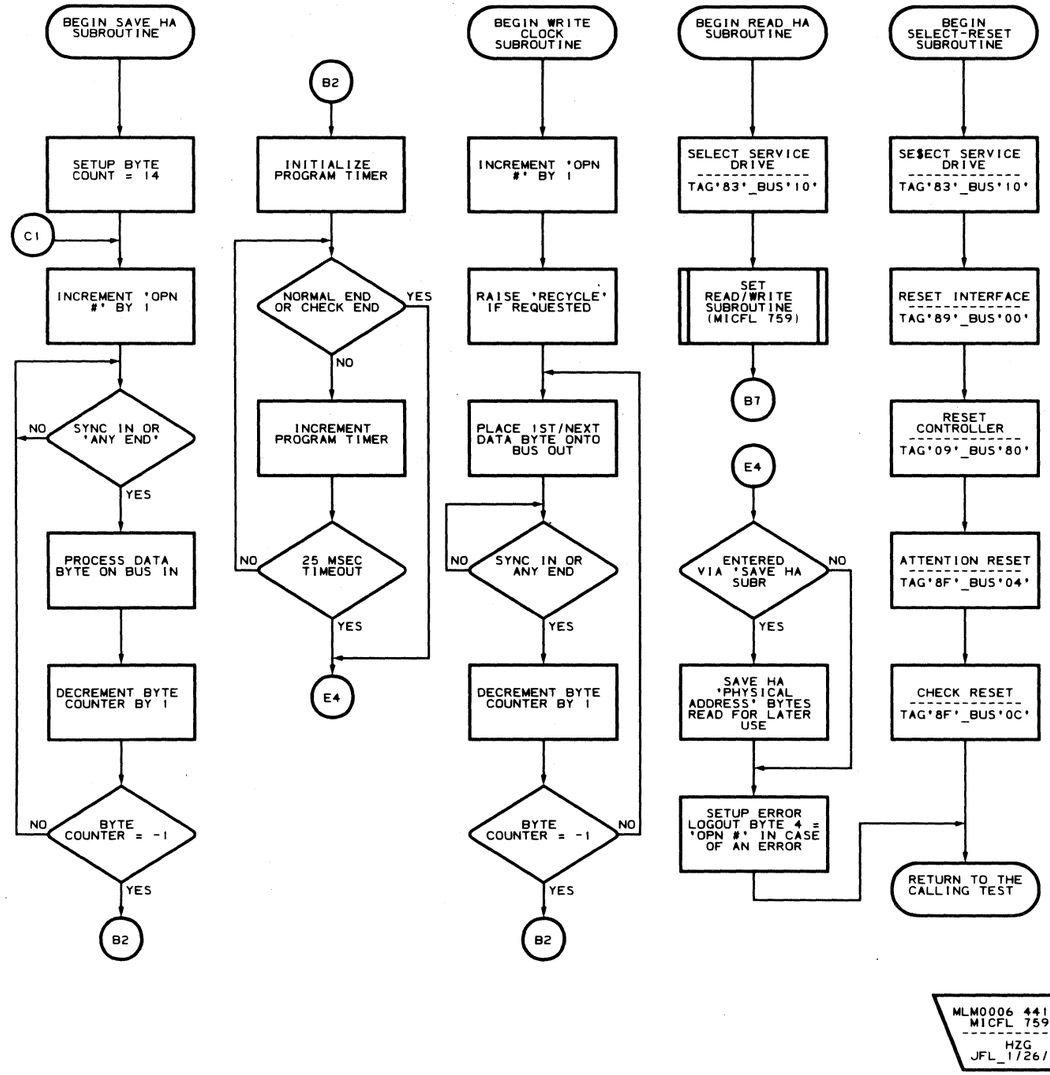
ROUTINE BB – 3330 COMPATIBILITY MODE AND OTHER SPECIAL TESTS

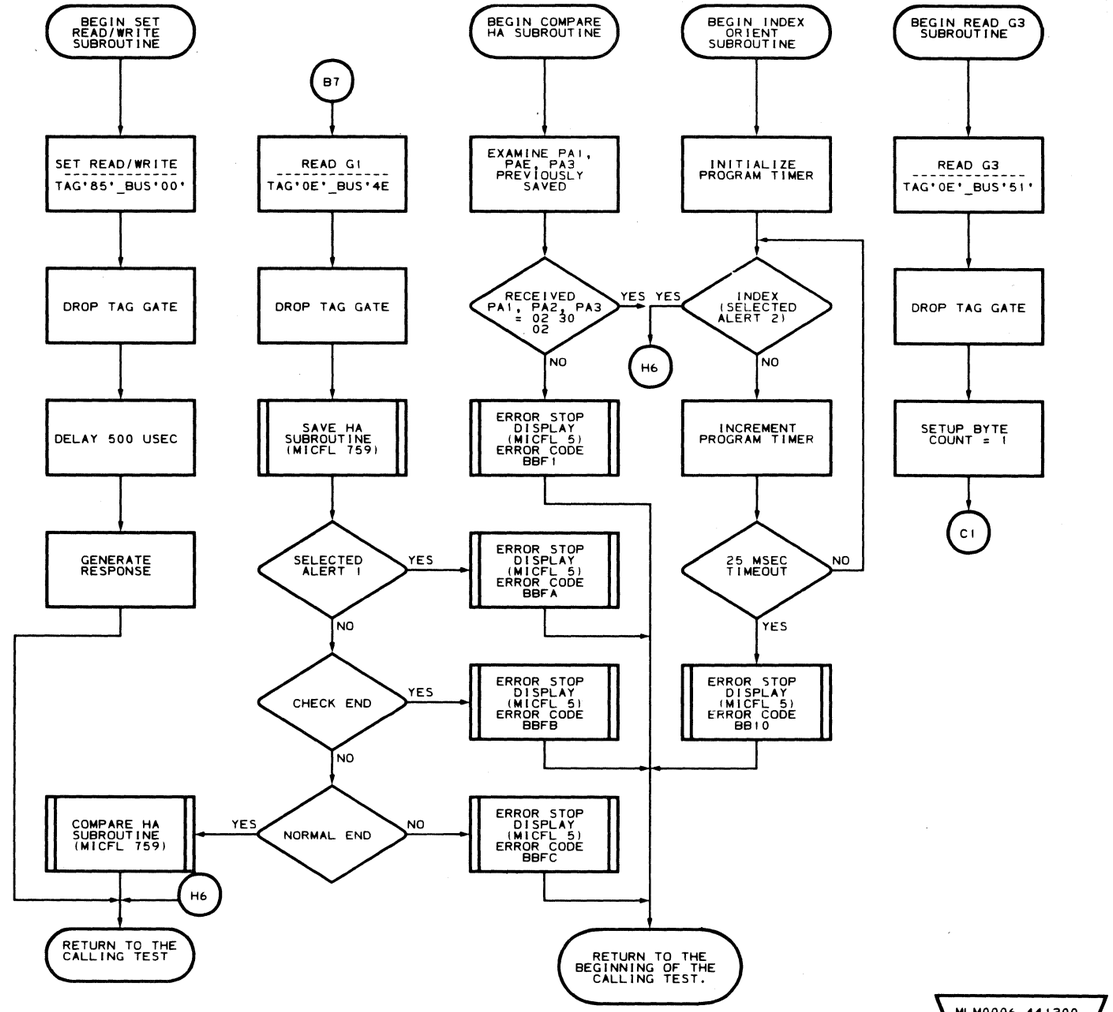




MLM0006 441300
MICFL 757-L
HZE
JFL_1/26/76

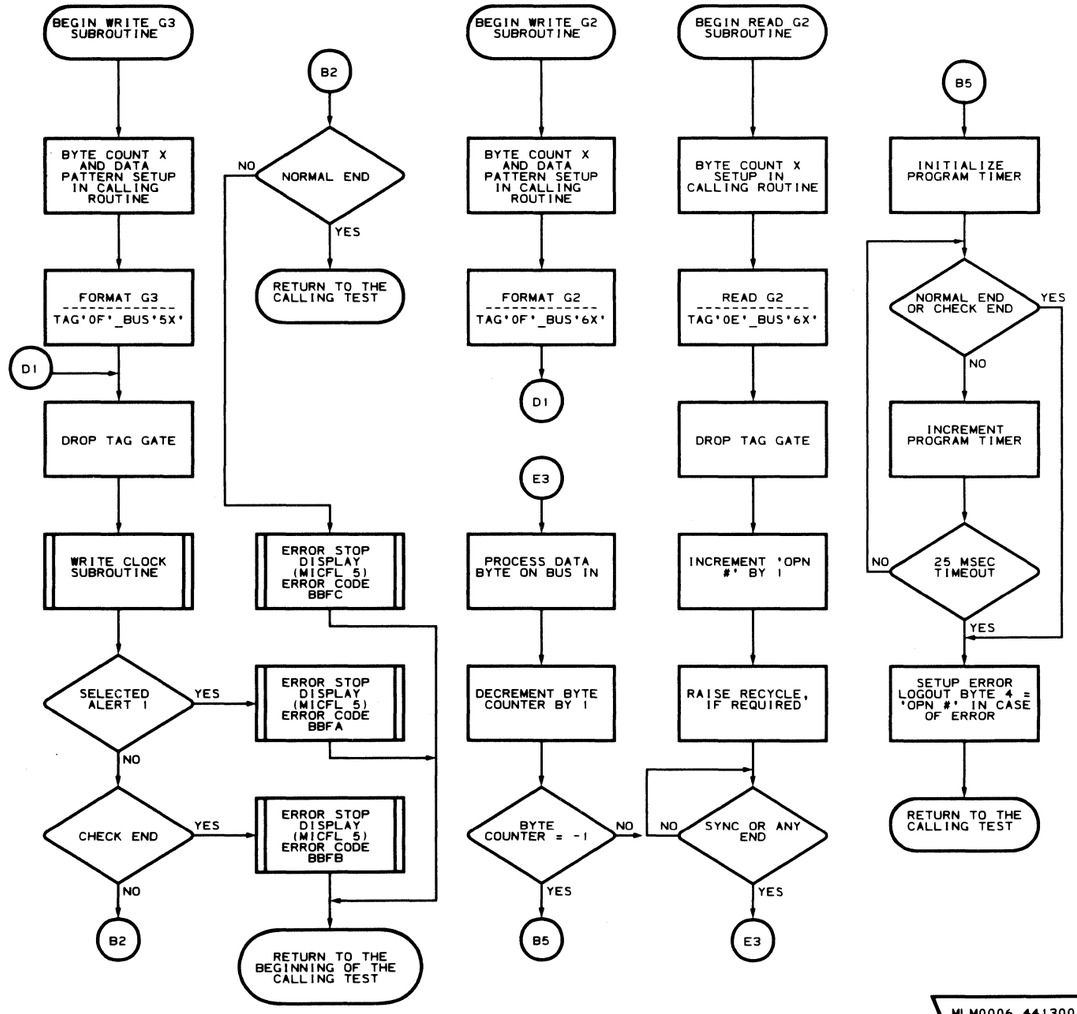
MLM0006 441300
MICFL 757-R
HZF
JFL_1/26/76





ROUTINE BB – 3330 COMPATIBILITY MODE AND OTHER SPECIAL TESTS

ROUTINE BB – 3330 COMPATIBILITY MODE AND OTHER SPECIAL TESTS MICFL 761



ROUTINE BB – 3330 COMPATIBILITY MODE AND OTHER SPECIAL TESTS MICFL 761

ROUTINE BC – 3350 UNCONDITIONAL RESERVE

DESCRIPTION

Routine BC (Unconditional Reserve microdiagnostic) checks only the ability of the hardware to release one path to a device by forcing the string switch to neutral. The function of device reserve contained in the UR (Unconditional Reserve) command is not checked as this is a normal device function checked by the string switch microdiagnostics.

Routine BC checks the ability of one interface to force the string switch to neutral when it is locked to the other interface.

Although the routine must be loaded and started on each controller interface, it is controlled exclusively from the interface designated as the Master. Control and error information is passed between the interfaces through registers in the service drive.

Error information is displayed at the end of the test. The Error Code is developed by ORing the error data from both interfaces. For details of a specific errors, see the Error Code Dictionary in the MICRO section.

OPERATING THEORY

Prior to running the test, the two interfaces must be synchronized. Once synchronized, the routine executes short sequences of operations separated by fixed time delays. The operational and delay sequences are offset in time so that each operational sequence is executed during the time delay on the other interface. In actuality, the test execution alternates between the two interfaces.

One interface is referred to as the Master, the other as the Slave. There are two flowcharts for each test in the MICFL section. One flowchart is the Master, the other is the Slave. The flowcharts are identical except for the Error Codes.

OPERATING PROCEDURES

To effectively run routine BC microdiagnostics, two passes are required: Pass 1, in which Interface A is the Master and B is the Slave; and Pass 2 in which B is the Master and A is the Slave.

Pass 1: (A = Master)

1. Set the CE Interface Select switch to the interface B position, then load and execute routine BC. Use standard operating procedures (MICRO 10), but do not enter Run Options or Parameters at this time. A few seconds after starting, the routine displays '8DFF' indicating it is ready to accept control information from the other interface.

2. Set the CE Interface Select switch to the Interface A position. Routine BC may now be loaded and run on Interface A using standard operating procedures (MICRO 10). Run Options and/or Parameters may be entered if desired.

Pass 2: (B = Master)

1. Set the CE Interface Select switch to the Interface A position, then load and execute routine BC. Use standard operating procedures (MICRO 10), but do not enter Run Options or Parameters at this time. A few seconds after starting, the routine displays '8DFF' indicating it is ready to accept control information from the other interface.

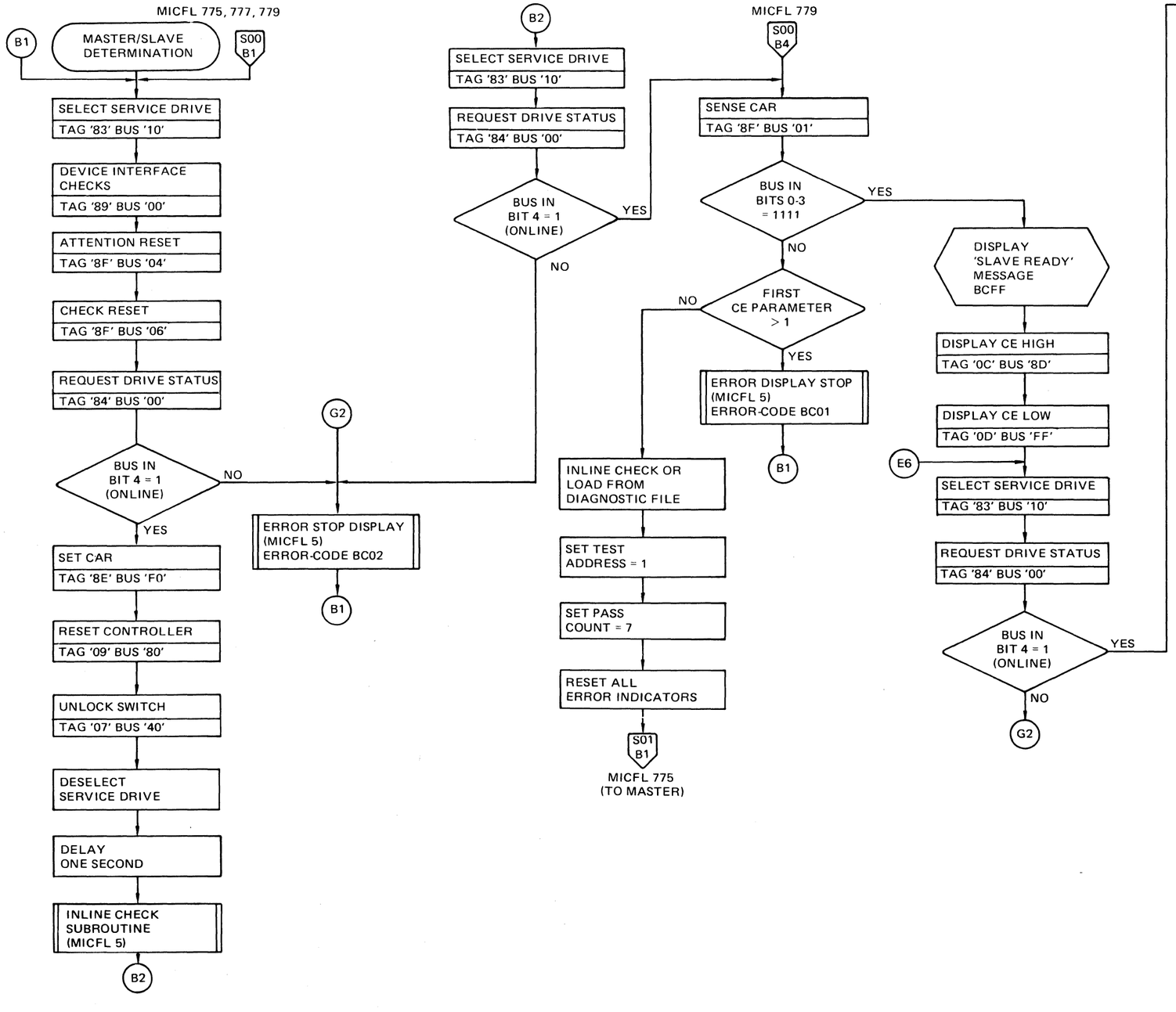
2. Set the CE Interface Select switch to the Interface B position. Routine BC may now be loaded and run on Interface B using standard operating procedures (MICRO 10). Run Options and/or Parameters may be entered if desired.

RESTART PROCEDURES

To restart (Pass 1 or Pass 2), begin at Step 2. The Slave enters an idle loop when the Master is stopped. Restarting the Master restarts the Slave after both interfaces are resynchronized. Step 1 is repeated only if the service drive is made not Ready.

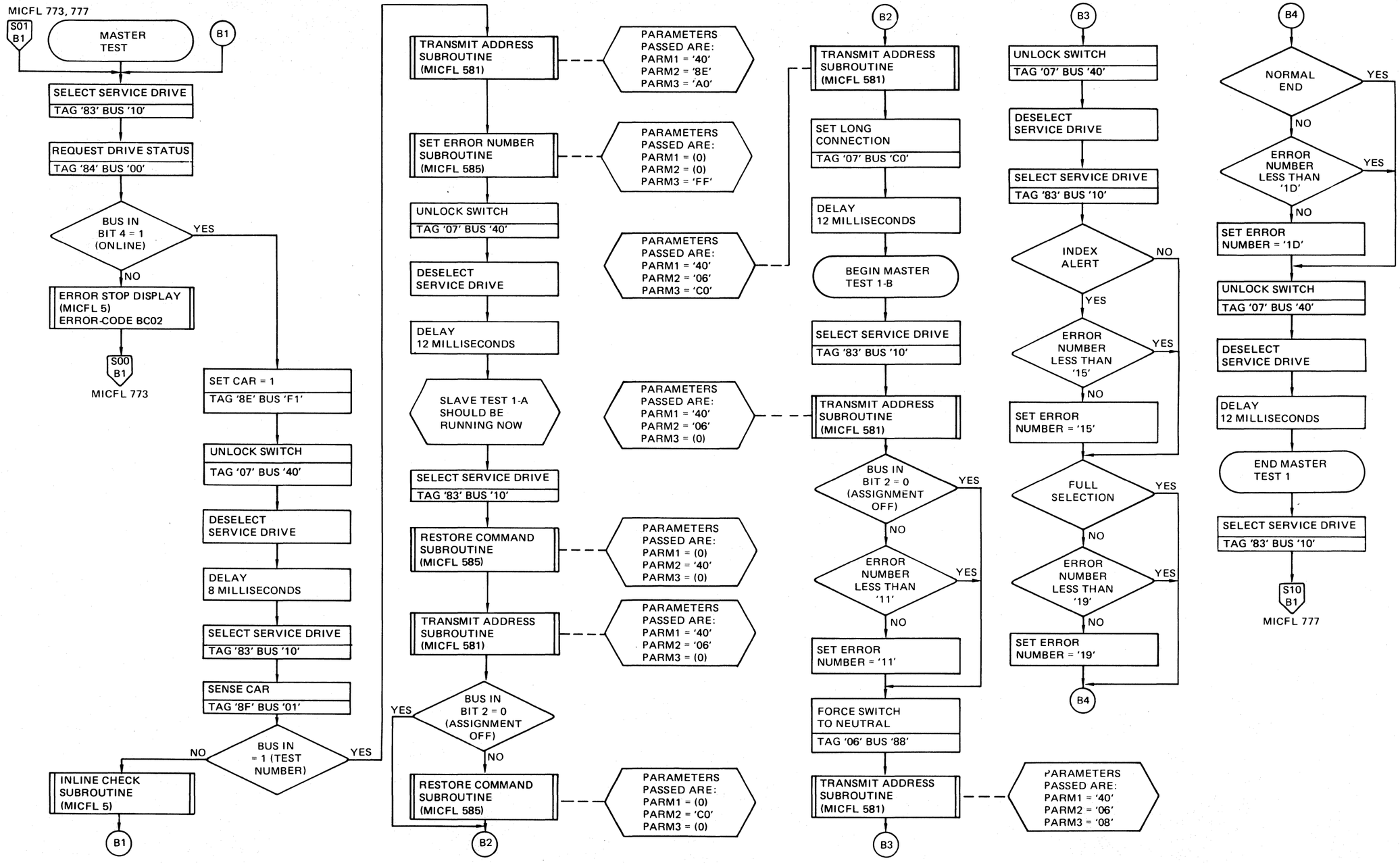
Note: *To recover from improper starting or an unexpected '8DFF' Error Code, stop the service drive momentarily, then restart using Step 1 of the Operating Procedures.*

ROUTINE BC – 3350 UNCONDITIONAL RESERVE TESTS



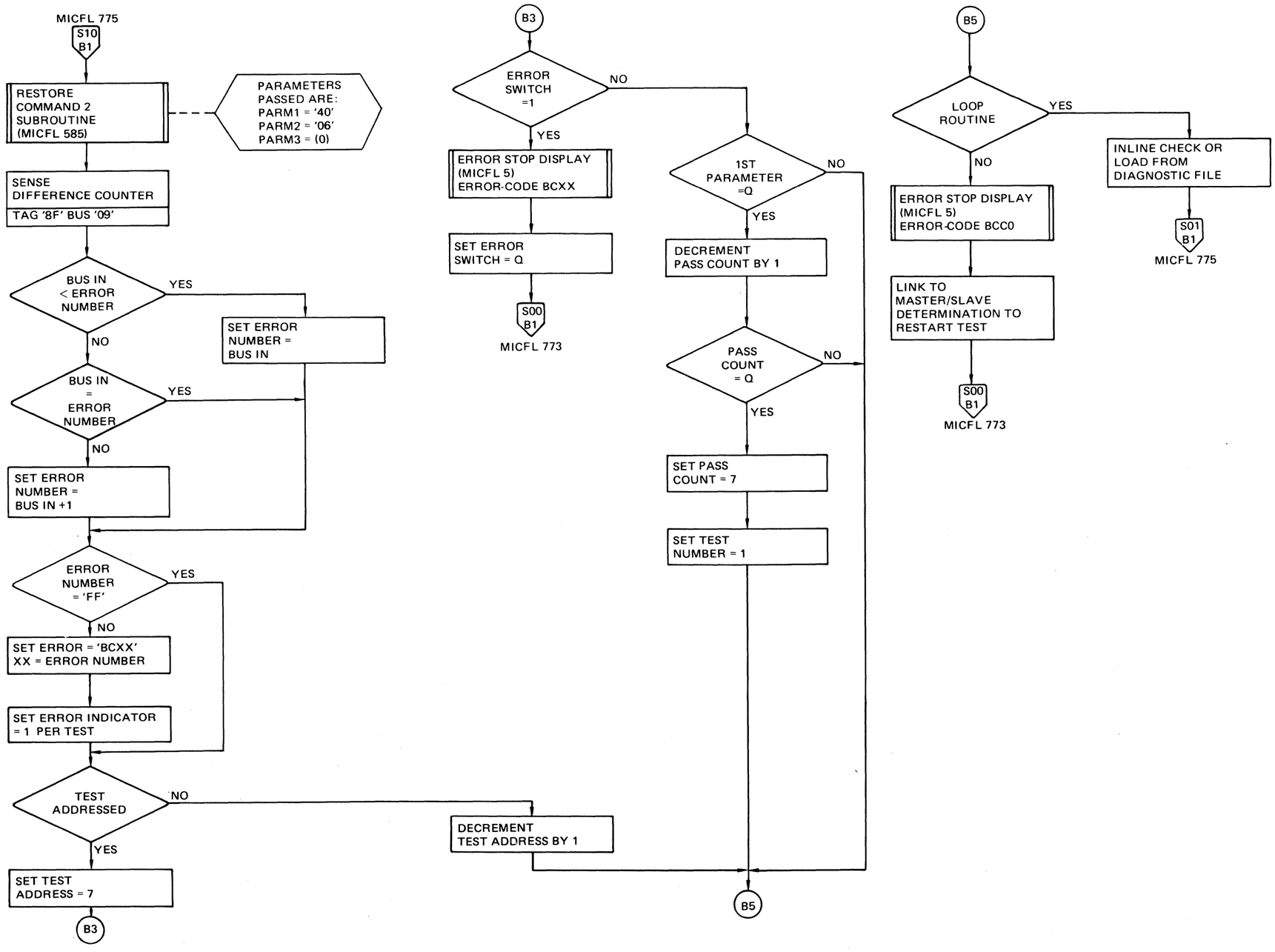
3350	GC0773 Seq. 1 of 2	2358798 Part No.	441305 29 Oct 76	441306 1 Apr 77			

ROUTINE BC – 3350 UNCONDITIONAL RESERVE TESTS

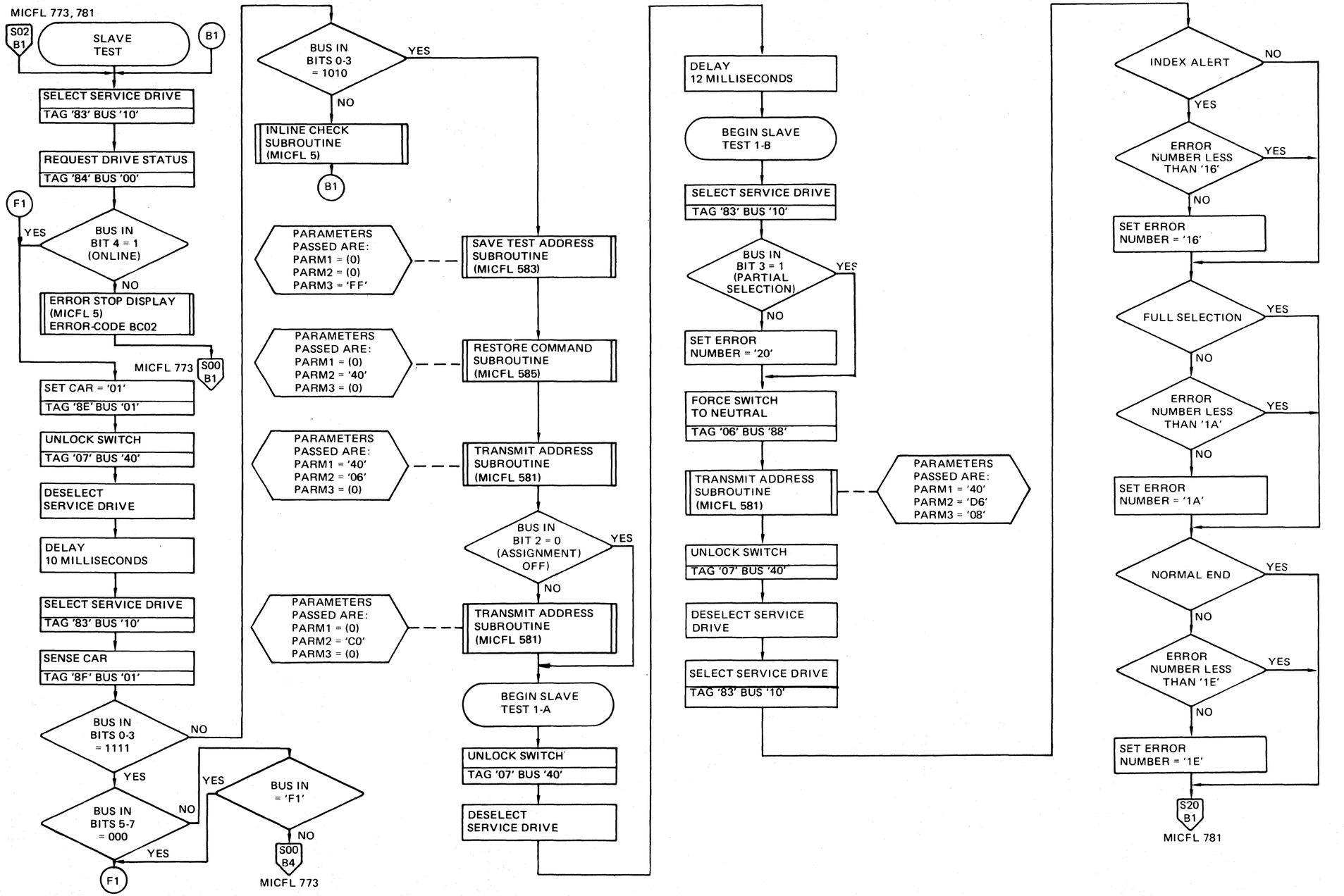


3350	GC0773 Seq. 2 of 2	2358798 Part No.	441305 29 Oct 76	441306 1 Apr 77			

ROUTINE BC – 3350 UNCONDITIONAL RESERVE TESTS

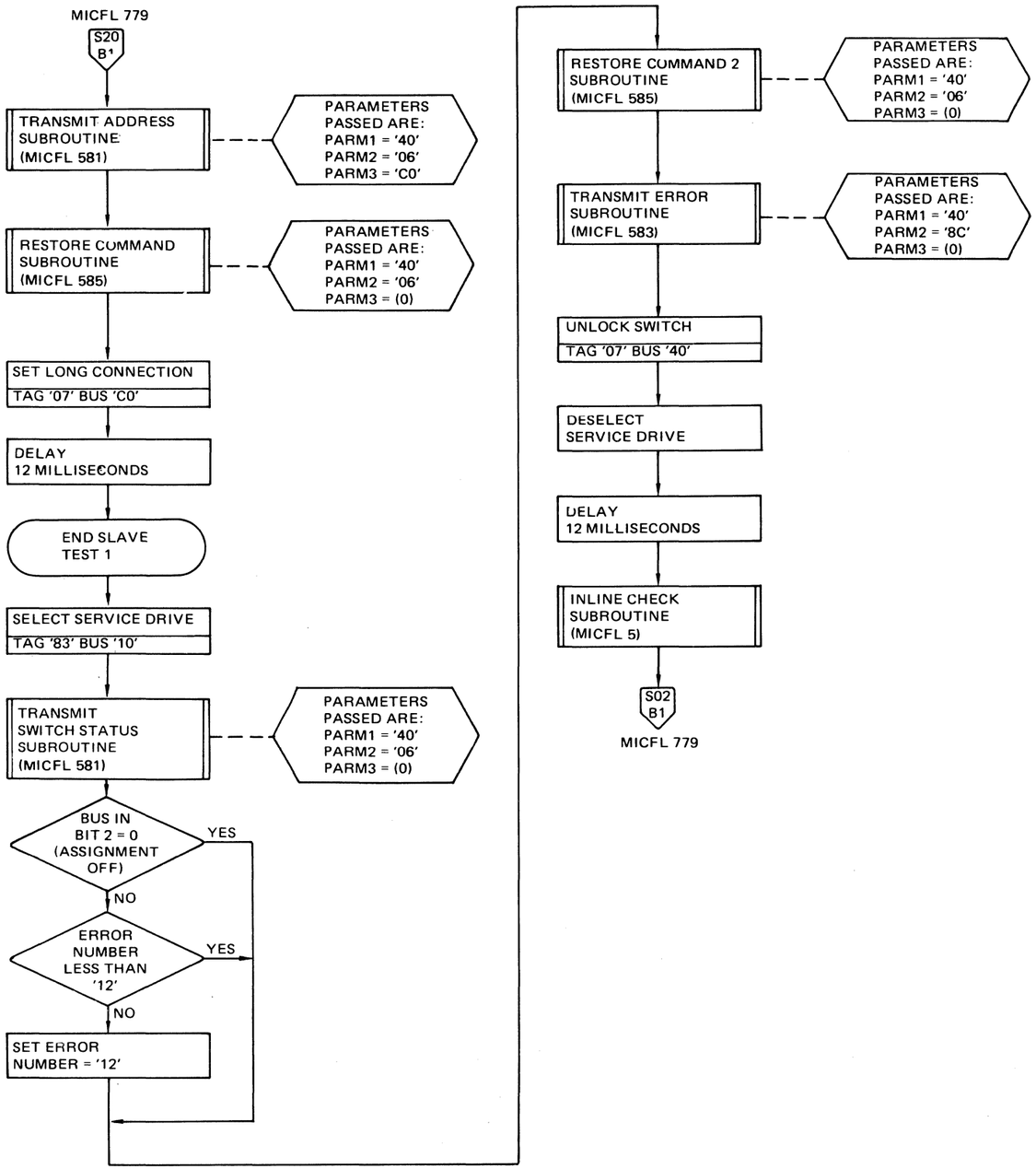


3350	GC0777 Seq. 1 of 2	2358799 Part No.	441305 29 Oct 76	441306 1 Apr 77			



3350	GC0777 Seq. 2 of 2	2358799 Part No.	441305 29 Oct 76	441306 1 Apr 77			

ROUTINE BC – 3350 UNCONDITIONAL RESERVE TESTS



3350	GC0781 Seq. 1 of 1	2358800 Part No.	441305 29 Oct 76	441306 1 Apr 77			

ROUTINE BD – 3350 VIBRATION TOLERANCE TEST

DESCRIPTION

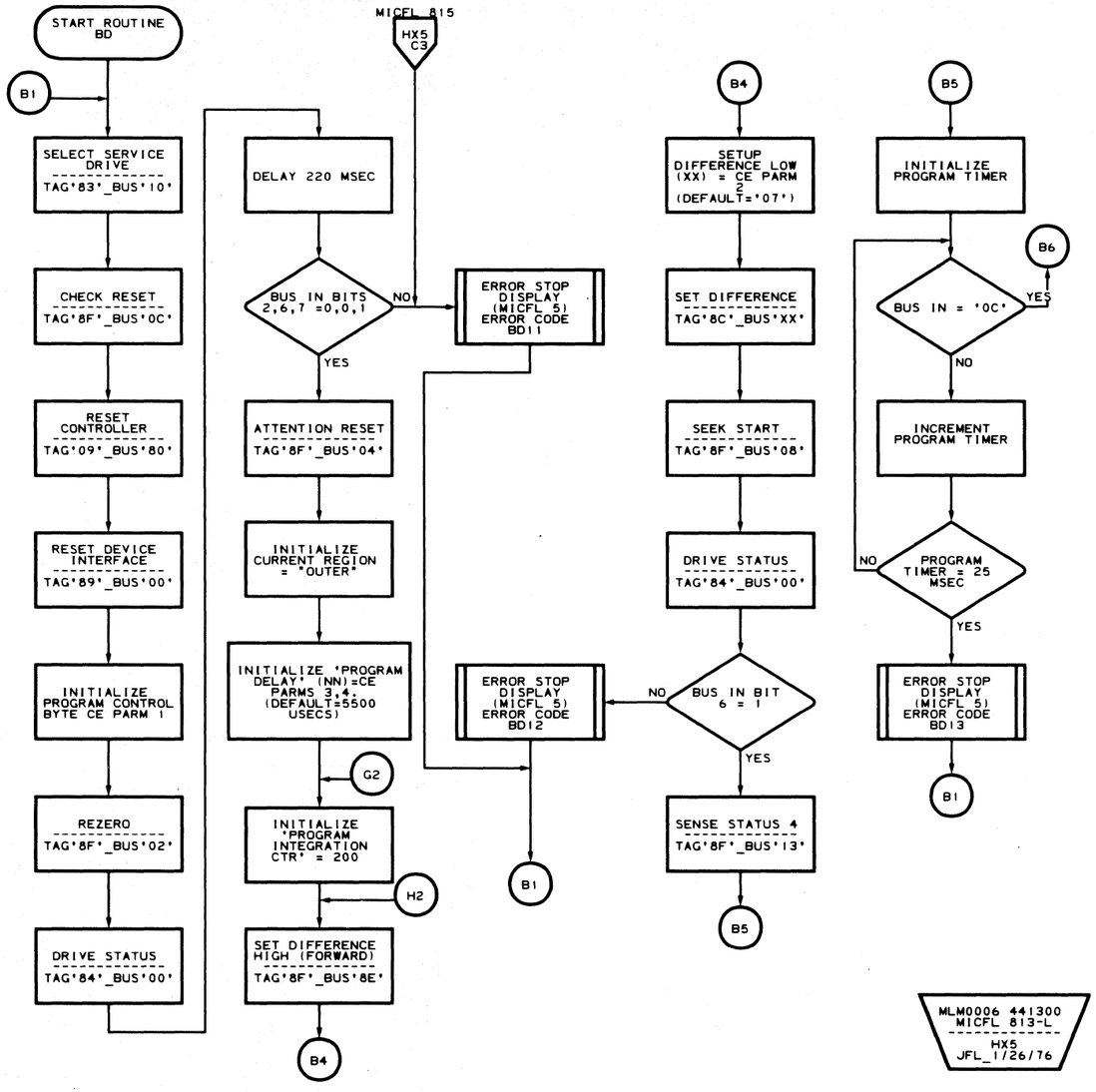
Routine BD attempts to excite the servo mechanism into mechanical resonance. The test resets the drive, Rezero, then initiates a series of forward/reverse seeks from cylinder 0 to cylinder 'nnn' (where 'nnn' is equal to the variable seek length that may be specified by the CE). Default value = 007), varying the delay time from receipt of Access Status = '0C' to the following Seek Start operation. The delay time ranges from 7.0 milliseconds to 10.0 milliseconds in 0.1 millisecond increments. If no Servo Off-Track errors are encountered, the program repeats the process between cylinders 560 and cylinder (560-nnn). A total of 400 seek operations are executed at each delay time value (200 forward, 200 reverse). There are 30 unique delay values used at each of 2 regions (outer, inner), for a grand total of 24,000 seek operations. The program overhead is approximately 41 microseconds from receipt of Access Status = '0C' until the next Seek Start operation (rise of Tag Gate). This overhead is not included in the posted delay values, but is in addition to them.

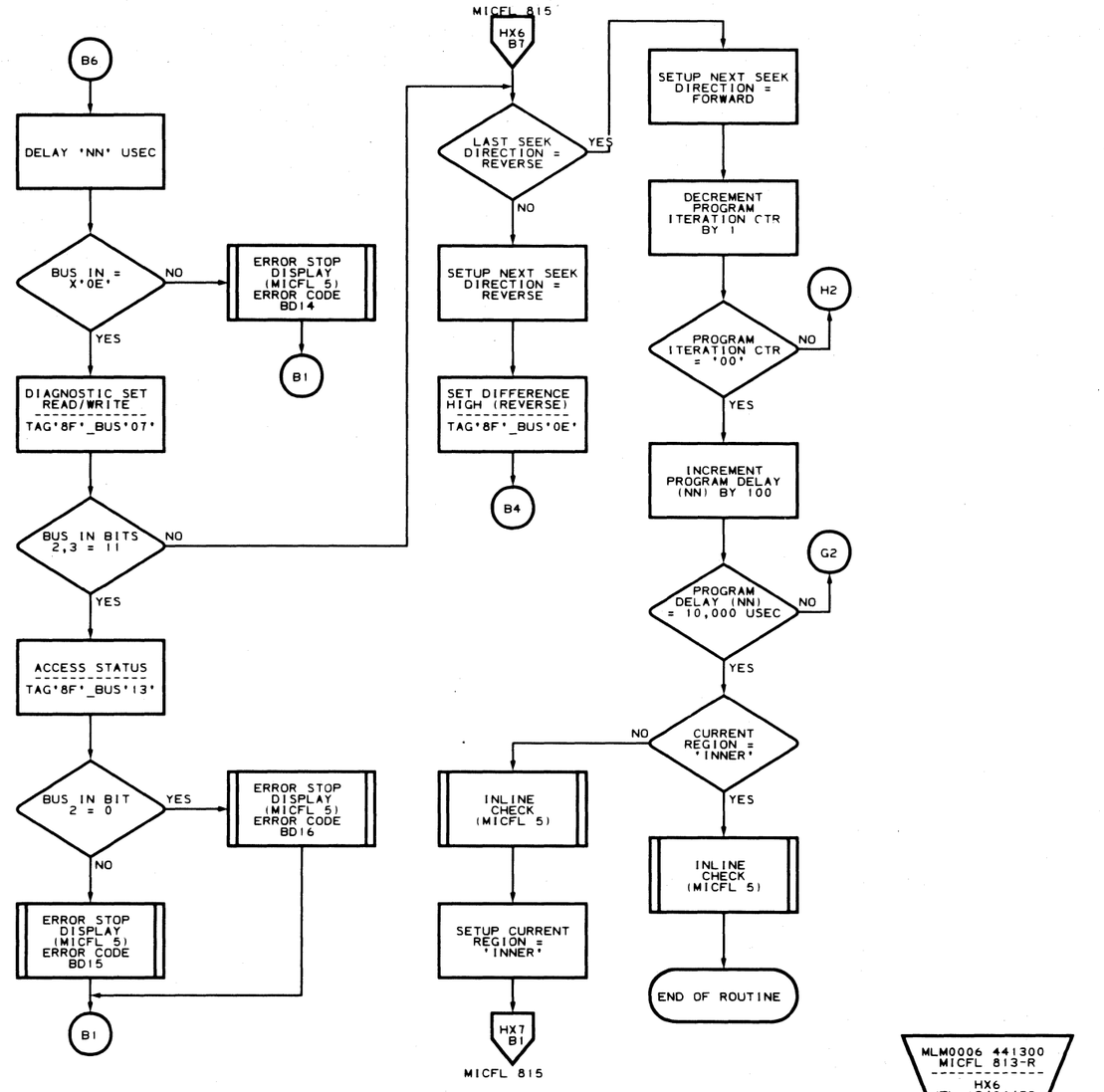
Optional parameter entry may be used to force the program to use only one delay value, specify the seek length to be used, and specify the starting delay value.

OPERATING PROCEDURE

- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to microdiagnostic reference charts starting on MICRO 84 for parameter entries.

ROUTINE BD – VIBRATION TOLERANCE TESTS MICFL 813

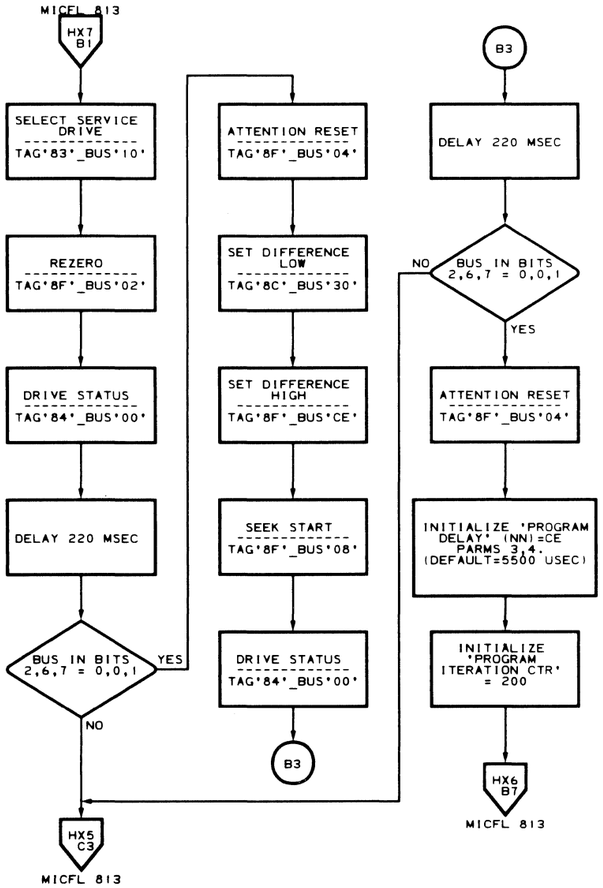




ROUTINE BD – VIBRATION TOLERANCE TESTS MICFL 813

ROUTINE BD – VIBRATION TOLERANCE TESTS

ROUTINE BD – VIBRATION TOLERANCE TESTS MICFL 815



MLM0006 441300
MICFL 815-L
HX7
JFL_12/04/75

ROUTINE BF – 3350 CONTROL INTERFACE UTILITY

DESCRIPTION

Routine BF is a utility routine designed to assist the CE in the bring-up of control interfaces. This routine runs in conjunction with the Interface Test Card and must be run from the Storage Control CE Panel or Maintenance Device.

Test 01. Outbound Tag and Bus

Test 01 checks for swapped cables. (Tag and Bus). This test can only check for cables interchanged on one end. The test cannot determine if the cable(s) are swapped end for end.

Test 01 also verifies that all inbound lines can be set off and then set on.

Test 02. Inbound Line Isolation

Test 02 checks that the inbound lines are not shorted together. Each line must have the ability to be activated without activating any other line. To accomplish this, each outbound line is activated one at a time and the corresponding inbound line is checked. Only the inbound line designated should be active. If any other line is active, an error is displayed.

If an error (two or more inbound lines active at the same time) is detected, a test is made for a shorted condition. If a shorted condition is not indicated, the extra inbound line is assumed to be in a continually active state.

Test 03. Sync-In, Sync-Out, Test Card

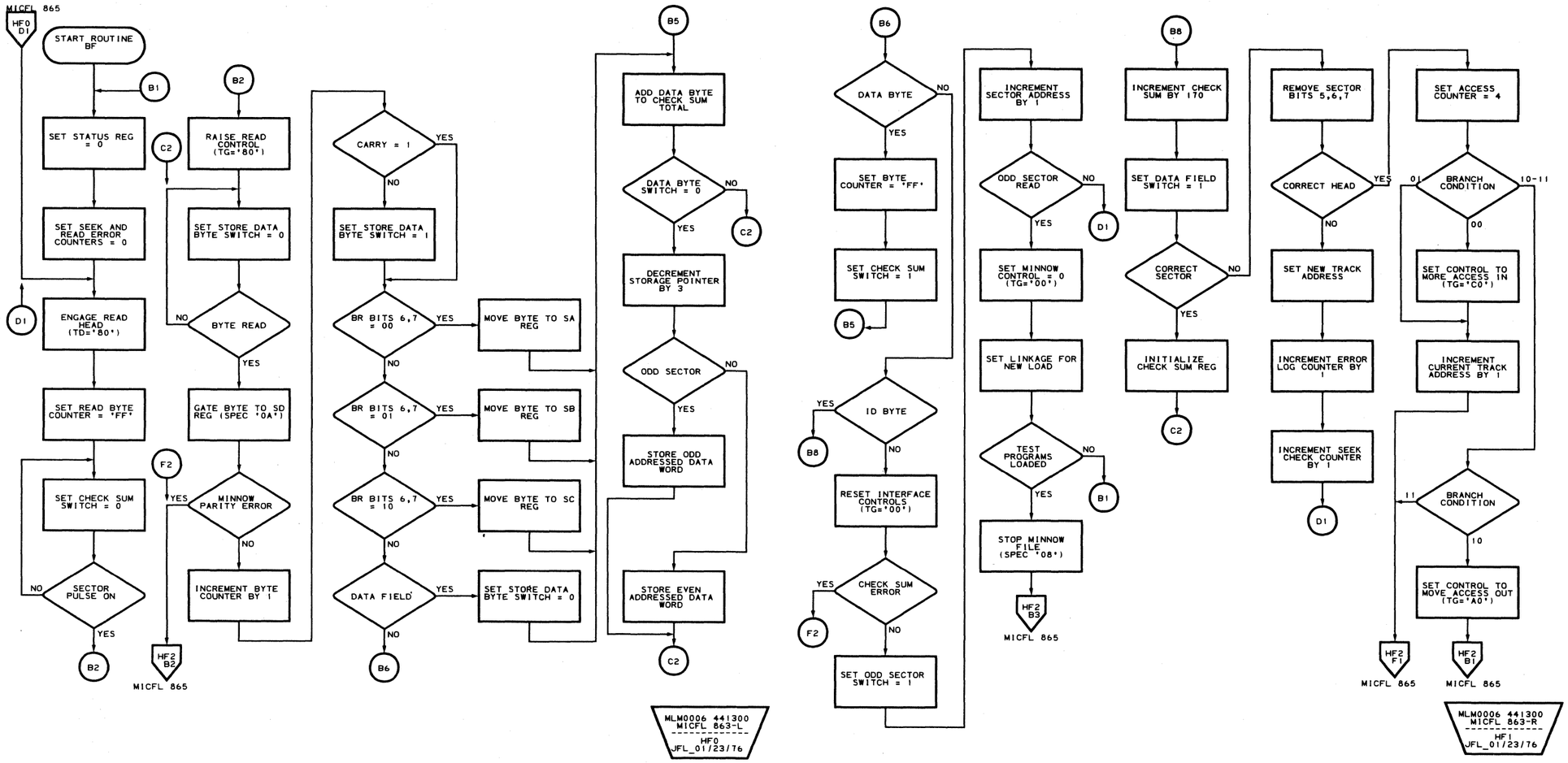
Test 03 sets the Sync-In line active by setting Tag Bus bit 0=1. With the 3830 in Data Response Mode, a Sync Out is returned. This Sync Out is latched in the Test Card and returned as Normal End. The Response line is used to reset the latch, hence the Response is tested for not being open.

A test for open Recycle line is performed by setting the Byte Counter greater than 15 (3830 MC Register) and issuing a 3830 Special Op '11'.

OPERATING PROCEDURE

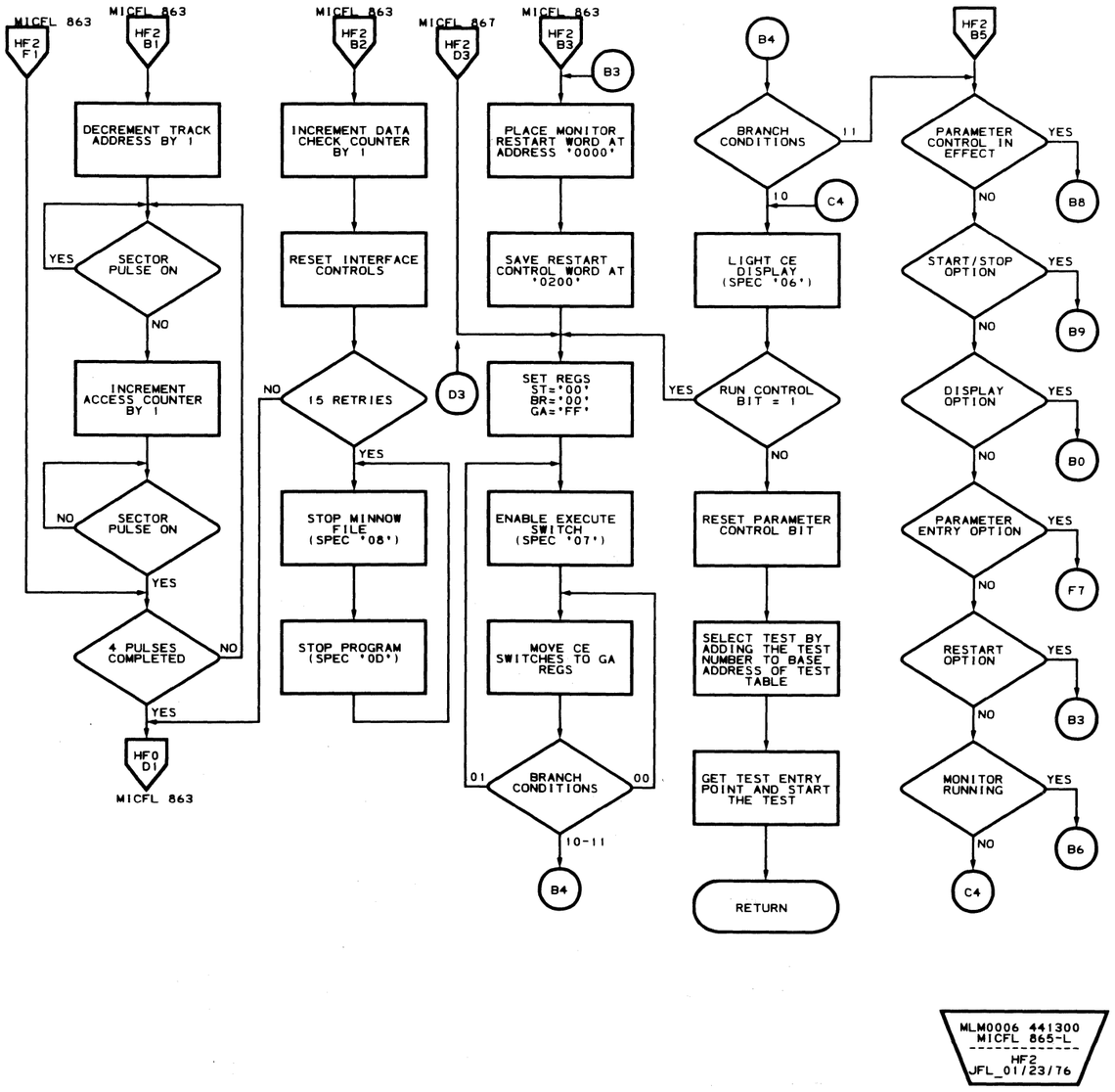
- Refer to MICRO 10 and 11 for standard operating procedures.
- Refer to CTL-I 100 and CTL-I 102 for the Interface Analysis Procedure.

ROUTINE BF – CTL INTERFACE BRINGUP ROUTINE MICFL 863

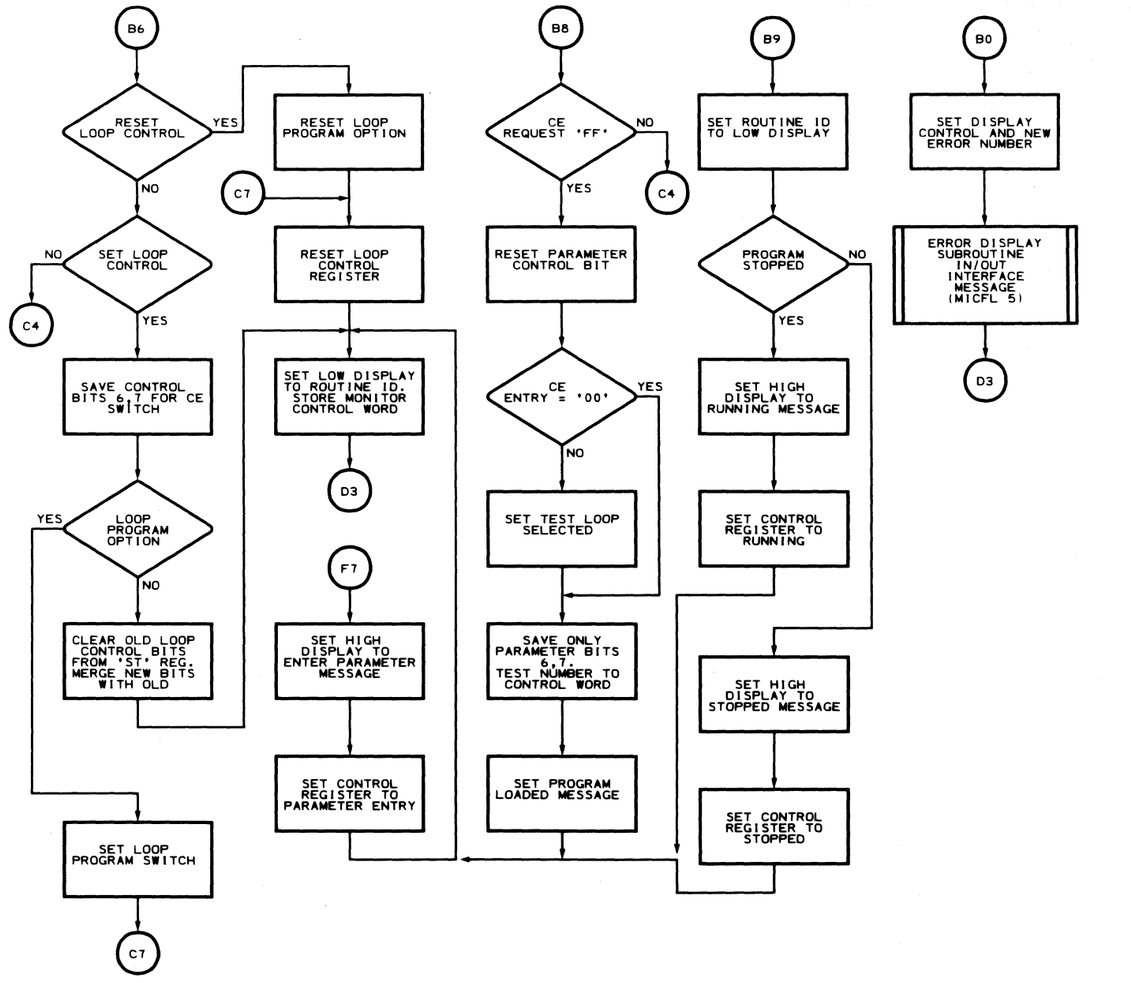


3350	GC0860	2358481	441300	441309	441310		
	Seq. 2 of 2	Part No.	31 Mar 76	15 Jul 79	27 Jun 80		

ROUTINE BF – CTL INTERFACE BRINGUP ROUTINE

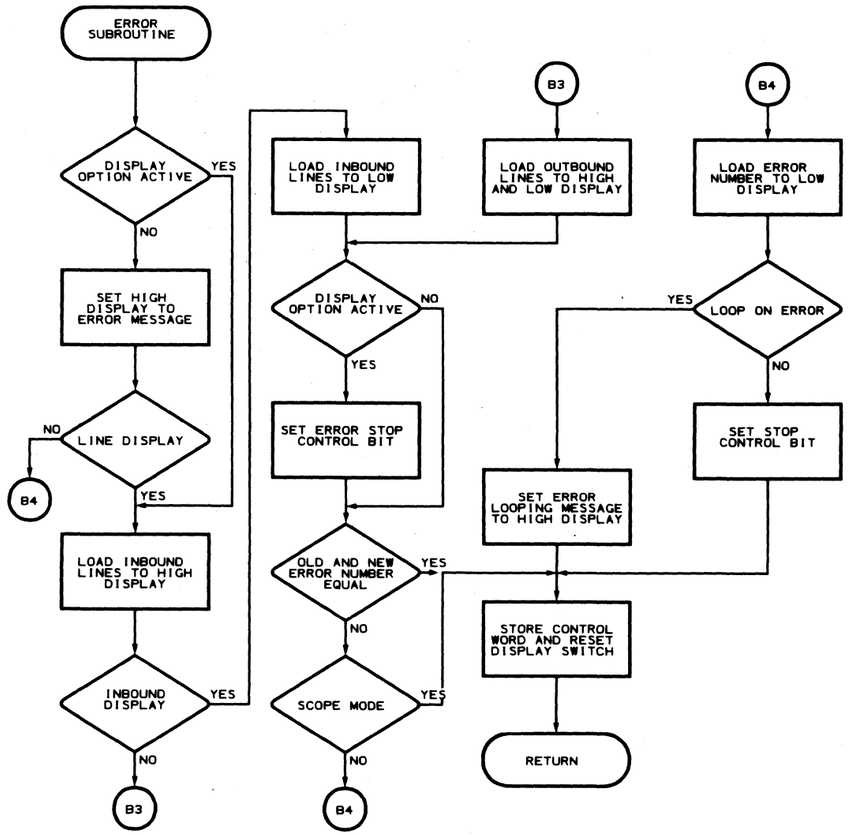


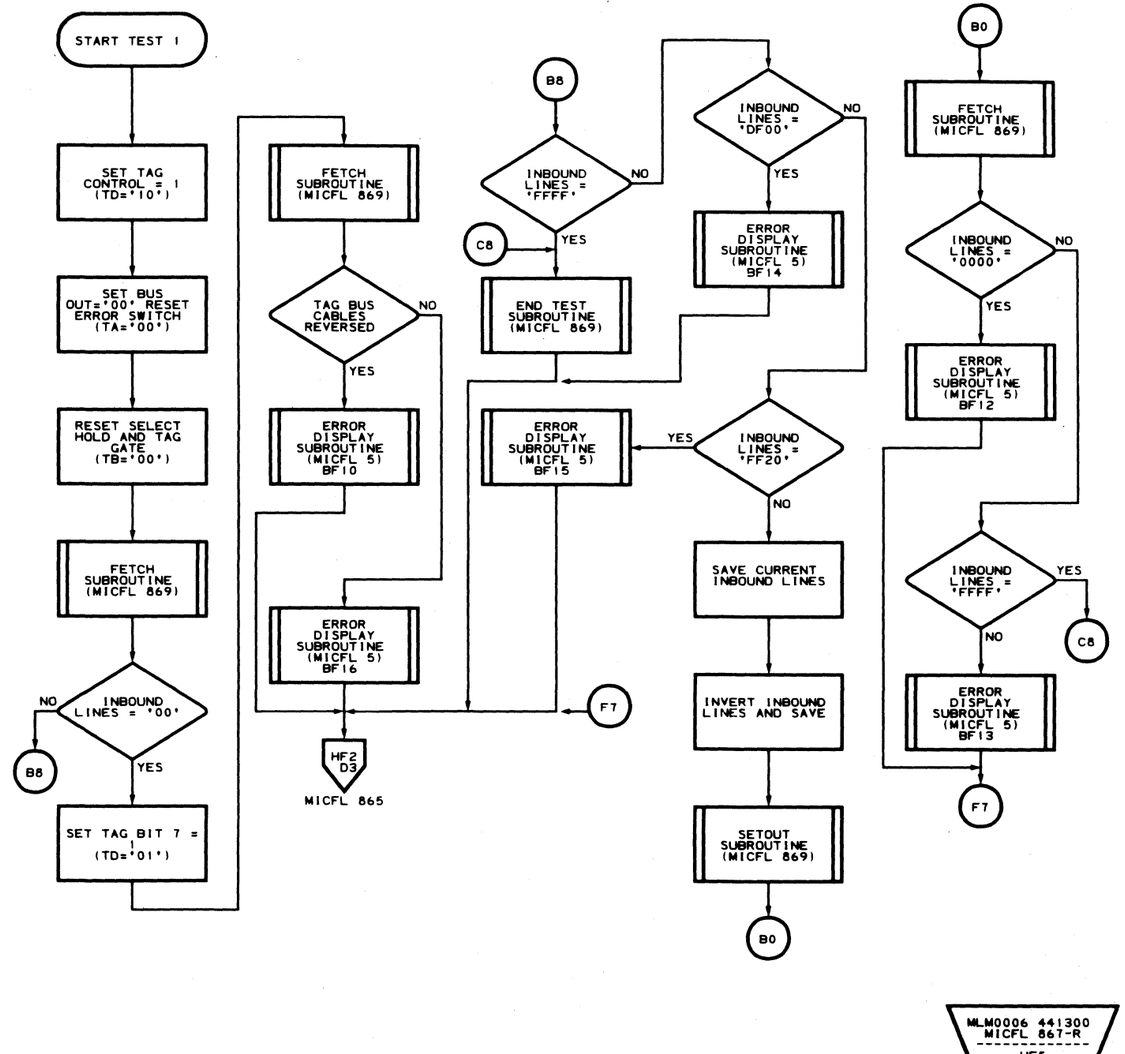
MLM0006 441300
MICFL 865-L
HF2
JFL_01/23/76



MLM0006 441300
MICFL 865-R
HF3
JFL_01/23/76

ROUTINE BF – CTL INTERFACE BRINGUP ROUTINE

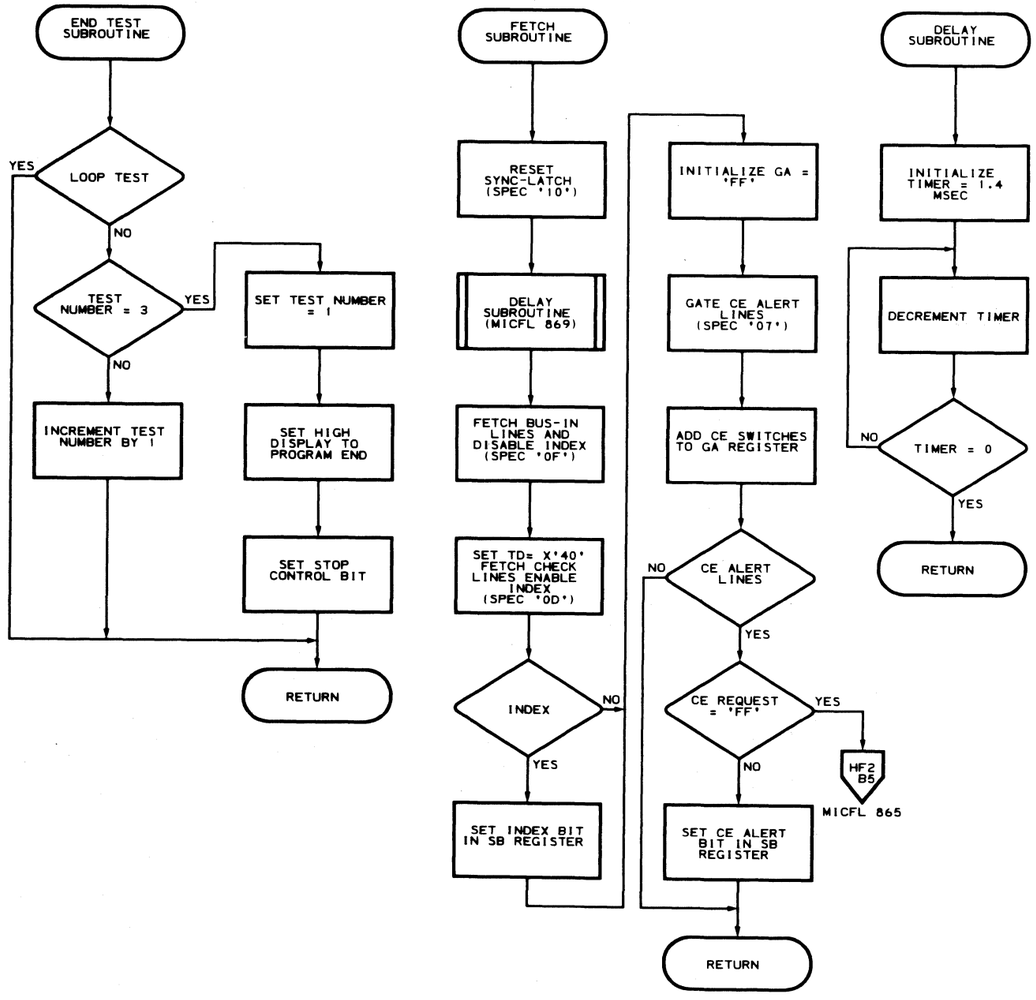




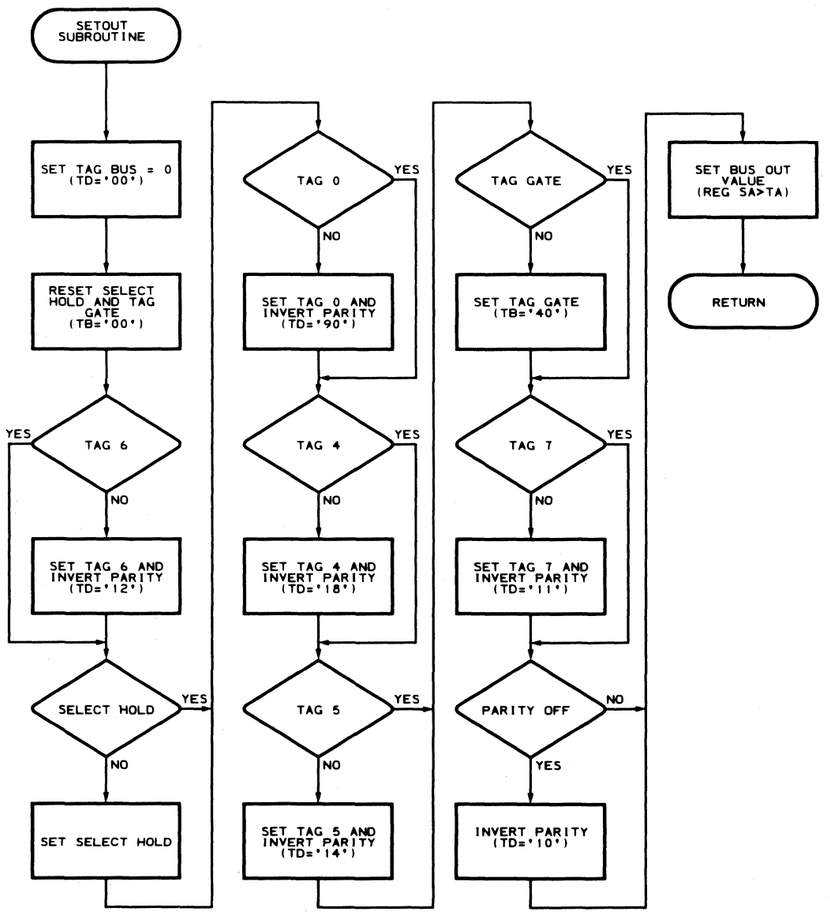
MLM0006 441300
MICFL 867-L
HF4
JFL_1/14/76

MLM0006 441300
MICFL 867-R
HF5
JFL_01/23/76

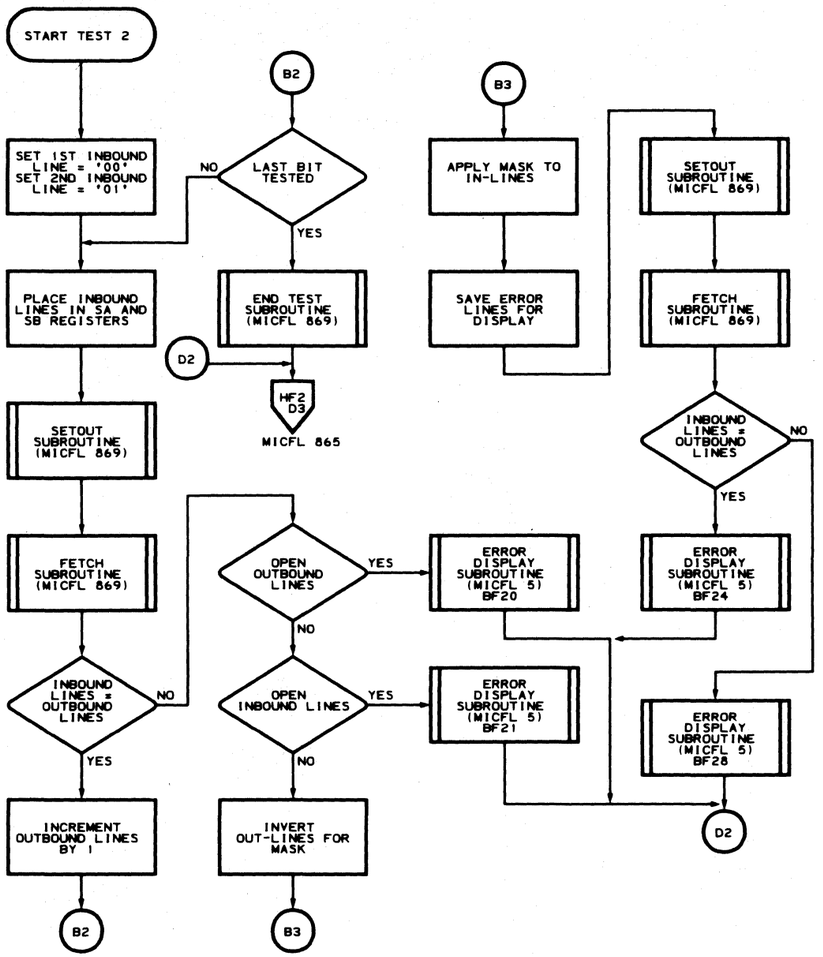
ROUTINE BF – CTL INTERFACE BRINGUP ROUTINE

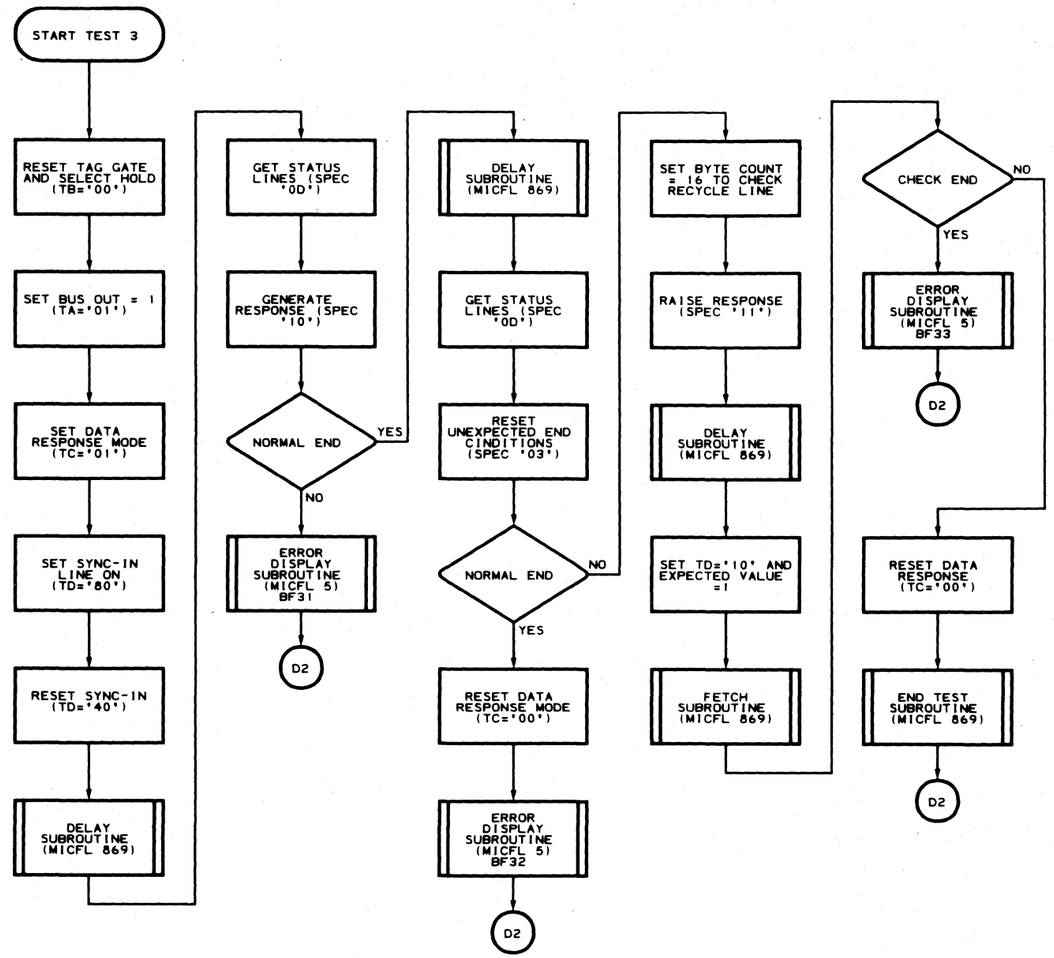


MLM0006 441300
MICFL 869-L
HF6
JFL_01/23/76



MLM0006 441300
MICFL 869-R
HF7
JFL_01/23/76





MLM0006 441300
MICFL 871-L
HF8
JFL_01/23/76

MLM0006 441300
MICFL 871-R
HF9
JFL_01/23/76