IBM Customer Engineering

Manual of Instruction

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DDTL Component Circuits

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Manual of Instruction

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Preface

Double Diffused Transistor Logic (DDTL) is a moderately fast, inexpensive, group of transistor circuits that have found wide application. These circuits use germanium diodes to perform logic functions and germanium mesa transistors to power the signals. These efficient circuits consume little power and perform logic decisions in 15 to 100 nanoseconds.

The DDTL circuit group includes nearly 300 circuits. These circuits are packaged in various combinations and inter-connections to make up hundreds of unique SMS printed circuit cards. Thousands of these cards are inter-connected to perform logic decisions in IBM machines, including the 7040, 7044, 7640, 7710, 7750, and 7908.

This instruction manual describes the characteristics of the DDTL circuits and gives detailed information on those circuits that are most frequently used. There are many special circuits used for unique applications that are not described here; these circuits are described in the CE Manuals for the machines that use these circuits.

This manual assumes a knowledge of transistor theory and basic transistor circuits such as presented in the *Transistor Theory and Application, IBM Customer Engineering Manual of Instruction,* Form 223-6783-2. From the basic knowledge assumed, three levels of circuit detail are given in this manual. The introduction deals with general characteristics and simplified explanations of common circuits. The "Circuit Operation" section gives the relation of inputs to outputs, circuit theory, and important input and output requirements for specific circuits. The Appendix has very detailed circuit analysis information on delays, transitions, and so forth, for a few of the most common circuits.

Each DDTL circuit is assigned a unique code number, usually beginning with H, for identification by engineering personnel. This H code, or block identification number, is generally printed underneath each ALD block to identify the circuit represented by that block. If two circuits differ in any way, a unique H code is assigned to each; thus, if several circuits are identical except for the value of the load resistor, each circuit has its own H code.

In this manual, circuits that are almost identical are grouped and covered as a single circuit; one circuit explanation may apply to several H codes. Use the H code index in Appendix B of this manual to locate the circuit diagram and description of a particular ALD block.

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Contents

General Circuit Group Characteristics

During 1954 and 1955, IBM developed a group of transistor component circuits. Although these circuits provided the three necessary functions (AND, OR, invert) to perform logic decisions, constant work improving speed, reliability, and flexibility, reducing cost and power consumption, and building special-purpose circuits has produced an overwhelming array of circuits since that time. This flood of ever-improving circuits has been partially caused by the continual improvement in speed, and reduction in cost and size of circuit components such as transistors, resistors, and capacitors.

Most of the circuits developed fall into groups (or "families") according to speed, transistor type, powering circuit, and the method used to make logic decisions (Figure 1). Because the circuit used to power signals and the method used to make logic decisions are key characteristics for understanding a new group of circuits, these characteristics are discussed in the following paragraphs.

Recall from transistor theory that signals can be powered by three different transistor circuit configurations: grounded (or common) emitter, grounded collector, and grounded base (Figure 2). The grounded emitter circuit is more commonly called an inverter, or invert block. The grounded collector configuration is more commonly called an emitter follower. By combining the inverter and the emitter follower, a configuration called a split-load circuit, or phase splitter, is obtained (Figure 3).

In addition to the basic transistor configurations, the transistors may be operated as linear amplifiers (small input signals) or they may be switched between saturation and cutoff (large input signals). See Figure 4.

Although each circuit group uses more than one circuit configuration for powering lines, each has a basic circuit that is used for all normal powering applications. For example, VMTL, CTRL, CTDL, SDTRL, SDTDL and DDTL use a saturating inverter; DEFL uses an emitter follower; ACM and DCM use a non-saturating split-load circuit and a non-saturating grounded base amplifier.

The three types of logic-performing circuits, diode, resistor, and transistor, are named for the major components in the circuits (Figure 5). Regardless of the type of input components, circuits for a particular

Group	Name	Application Example	Normal Packaging	Primary Transistor	Approx Dly Per Decision
VMTL	Voltage Mode Transistor Logic	608	608 Card	01, 051	1-5 usec
DCM (CSDBTL)	Diffused Current Mode (Current Switching Diffused Base Transistor Logic)	7030, 7090, 7080	Single and Double SMS Cards	015, 065	10-30 ns
ACM (CSAJTL)	Alloy Current Mode (Current Switching Alloy Junction Transistor Logic)	7030, 7090 7070, 7080	Single SMS Card	013, 063	50-200 ns
CTRL (NOR I)	Complementary Transistor Resistor Logic (Negated OR)	1620, 729 (NOR) 7701, 7702, 7330	Single SMS Card	033, 083	1-3 usec
CTDL	Complementary Transistor Diode Logic	7070, 1401	Single SMS Card	034, 083	0.3-1.5 usec
SDTRL (NOR II)	Saturating Drift Transistor Resistor Logic	7074, 1410, 1620, 7631	Single and Stan-Pac SMS Cards	101	50-150 ns
SDTDL	Saturating Drift Transistor Diode Logic (Negated AND)	7074, 1410, 7631	Single and Stan-Pac SMS Cards	102	50-100 ns
DEFL	Diode Emitter Follower Logic	7302 (Serial 12,000 & Above)	Stan-Pac SMS Card	098	3-10 ns
DDTL	Double Diffused Transistor Logic	7750, 7908, 7040, 7640	Single and Twin SMS Cards	152, 153	15-100 ns

Figure 1. Component Circuit Groups

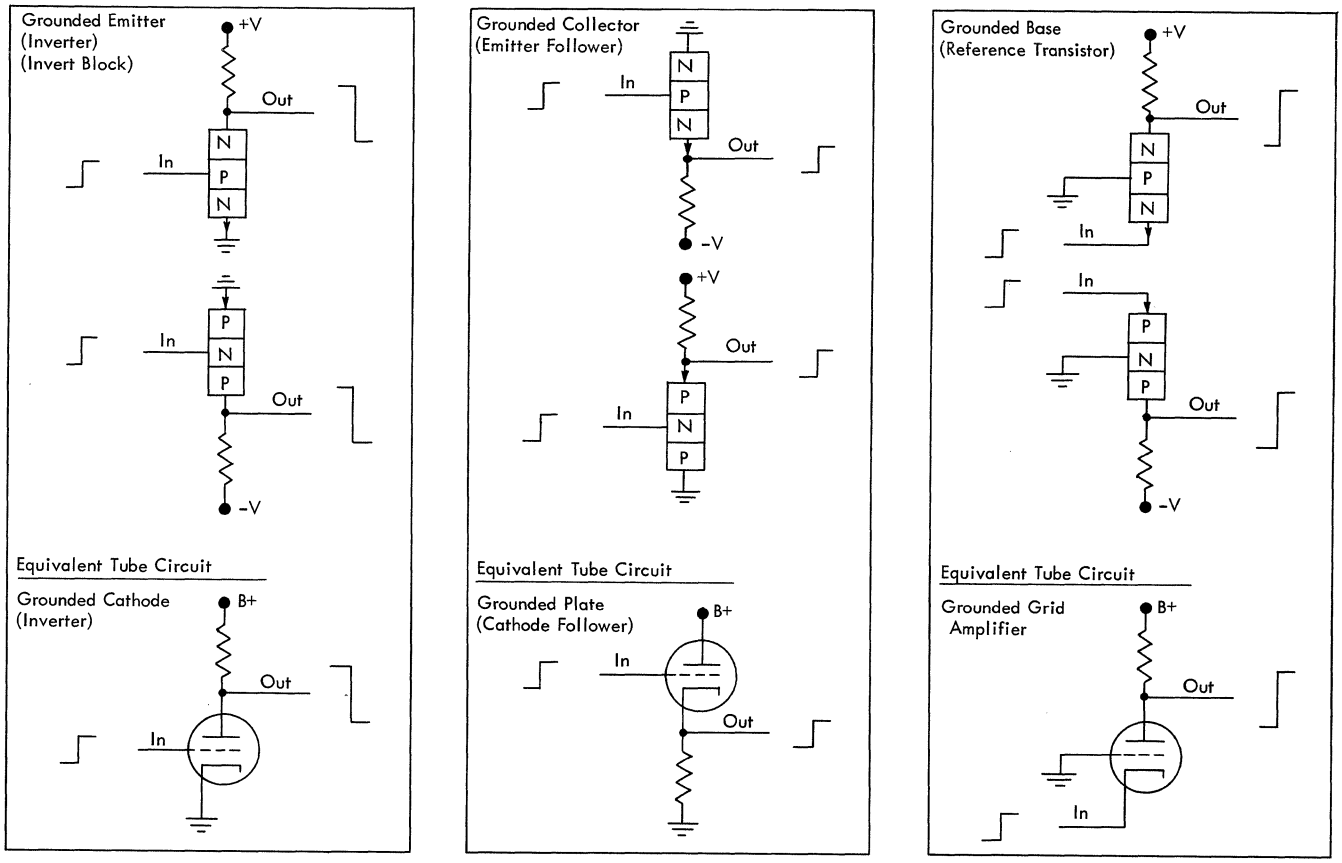


Figure 2. Transistor Circuit Configurations

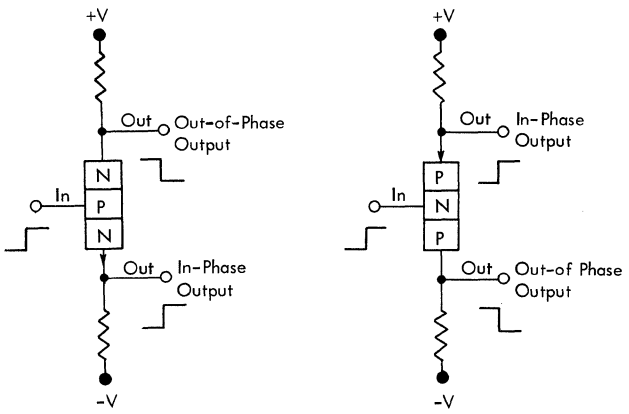


Figure 3. Split-Load Configuration

logic decision produce identical results: in the diode +AND circuit, input 1, input 2, and input 3 must be positive to prevent diode conduction; in the resistor +AND, all inputs must be plus to prevent current flow; in the transistor +AND, all inputs must be plus to hold the transistors cut off. In each of these cases, the +AND function is satisfied by preventing current flow through the load resistor and allowing the circuit output to rise to +6v.

In the +OR circuits, input 1 plus, input 2 plus, or input 3 plus causes current flow through the load transistor to bring the output plus.

Figure 6 summarizes characteristics (powering circuit and logic-performing circuit) of the most widely-used circuit groups.

In addition to the circuit characteristics discussed, a circuit group may use either positive or negative logic; also, the circuits may be translating or non-translating.

In the preceding discussion of logic-performing circuits, positive logic was assumed; that is, the up or more positive state of input and ouptut lines was considered more important, or active. The AND function was preceded by a plus sign and described as input 1 (plus), input 2 (plus), and input 3 (plus), causing a plus output. In many cases, it is desirable to use the down, or more negative, state of lines as the active

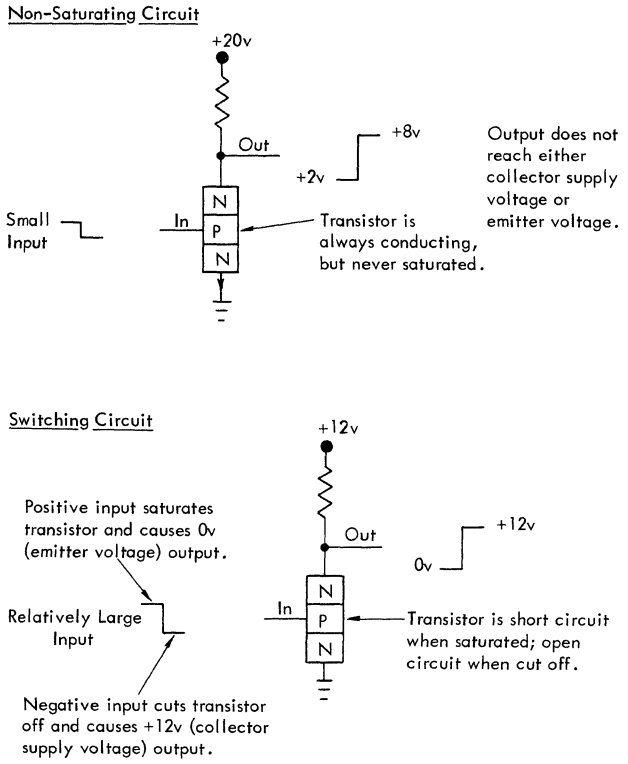


Figure 4. Transistor Operating Modes

level; thus often eliminating the need for inverters. When negative levels are considered active, the logic of a +AND is −OR (Figure 7); input 1 minus, input 2 minus, or input 3 minus causes a minus output. Similarly, a +OR is a −AND; input 1 minus, input 2 minus, and input 3 minus produce a minus output. Whenever the down or more negative state of circuit inputs is considered more important (active), the result is negative logic.

Positive logic – Up level active (+A, +O)
Negative logic – Down level active (−A, −O)

These descriptions of positive and negative logic show that any circuit can be used to make either positive or negative logic decisions; generally, machine logic is a mixture of the two. Some of the inverting circuit groups, particularly NOR (negated OR), are designed so that one basic circuit performs most machine logic. The scheme alternates between positive and negative logic to take advantage of the inverter powering circuit (Figure 8).

Translating circuits alternate NPN and PNP transistors to reduce the number of circuit components. In some CTRL circuits, for example, the output of an NPN transistor is an R line and is used as the input to PNP transistors; the output of a PNP transistor is an S line and is used as the input to NPN transistors (Figure 9). The two line types result from the difference in collector supply voltages for NPN and PNP transistors.

DDTL Characteristics

Computing equipment is built in wide ranges of size, speed, and complexity. As applications grow, so does the gap between the largest and smallest; the cheapest and most expensive; the fastest and slowest. No single circuit group can meet the cost, speed, reliability, and flexibility requirements of all machines; however, the DDTL circuit group is much more flexible than older groups and, therefore, covers a much wider range of applications. There are two types of powering circuits: inverters and emitter followers; there are three variations of the inverter circuit: basic (low-speed), low-power (high-speed), and level setter; there are two kinds of collector load networks: clamped and unclamped. Including special-purpose circuits and all the standard circuit variations, the DDTL group comprises nearly 300 circuits.

The following paragraphs explain the general characteristics of standard DDTL circuits; details of specific circuits are presented under "Circuit Operation."

In DDTL circuits, diodes make the logic decisions. Two different diode circuits are used (Figure 10), and can be arranged in either single-level or double-level configurations. Single-level is one diode circuit between powering (transistor) circuits; double-level is two diode circuits between powering circuits (Figure 11). Double-level logic can be either diode AND's feeding a diode OR, or diode OR's feeding a diode AND. For simplicity, Figure 11 shows only two inputs to each diode circuit; most diode circuits, however, can have up to six, seven, or eight inputs, and a few can have as many as 12 inputs.

Although double-level logic is sometimes made up (shown in ALD's) of individual circuits like those shown in Figure 11, the second level of diodes is usually combined with a powering circuit such as an inverter (Figure 12). Diode logic is also combined with other DDTL powering circuits (Figure 13). Inputs to diode circuits included with powering circuits may be from other powering circuits as well as from first-level diode blocks (one or two levels of logic).

Note that the placement of a block output line in Figures 12 and 13 and in ALD's (automated logic diagrams) is significant: if the output level is in phase with the active state of the inputs (as is the case for all diode circuits), the output line is from the lower half of the block; out-of-phase outputs leave the upper half of a block. As previously explained, the sign of a

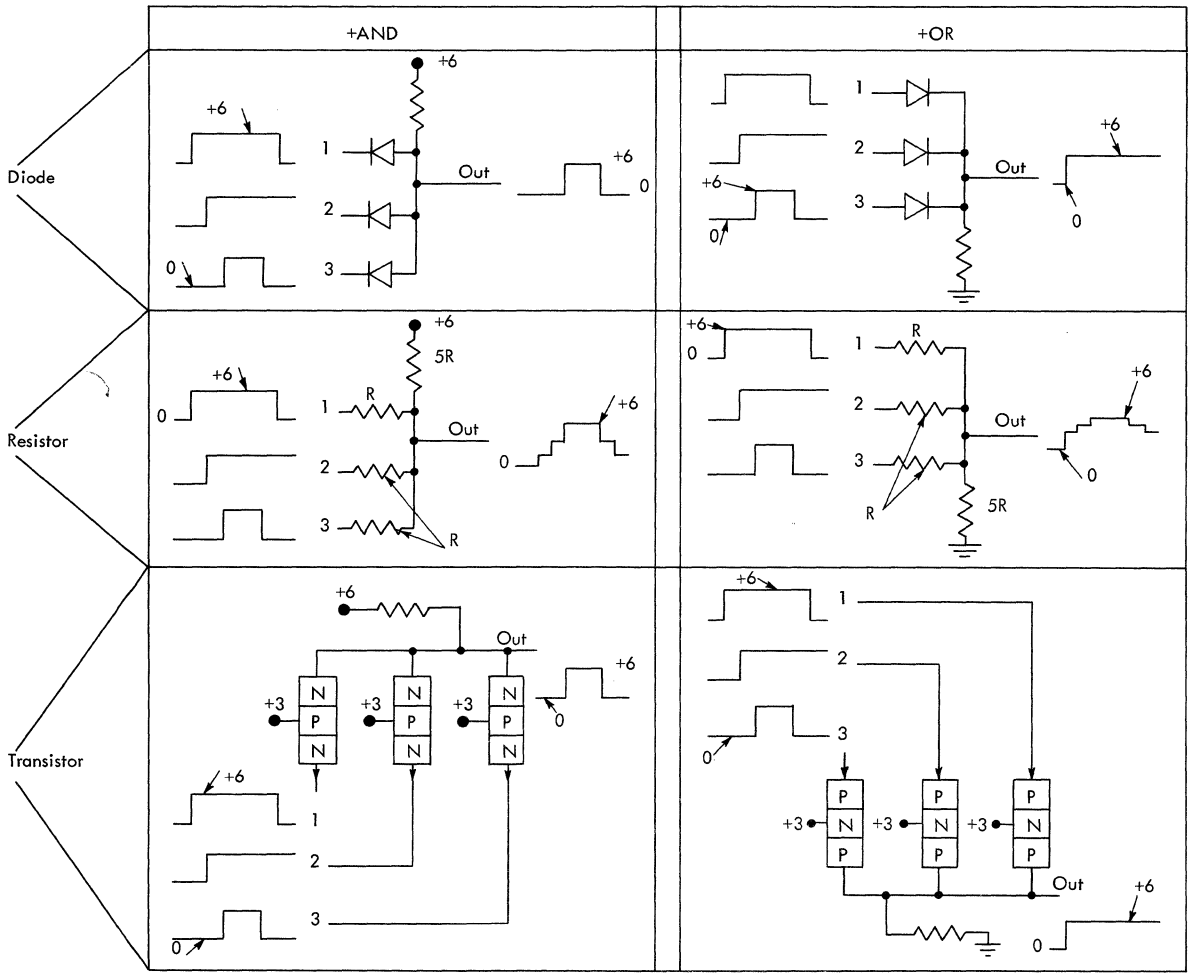


Figure 5. Logic-Performing Circuits

Group	Principal Powering Circuit(s)	Saturating	Decision Components	Comments
VMTL	Inverter	Yes	Diodes	First IBM transistor circuits. Converted tube circuits.
DCM	Split-Load and Grounded Base	No	Transistors	Designed for maximum speed. First use: 7030
ACM	Split-Load and Grounded Base	No	Transistors	Same concepts as DCM, but lower cost where slower speed acceptable.
CTRL	Inverter	Yes	Resistors	Simple, low-cost circuits for slow-speed applications.
CTDL	Inverter	Yes	Diodes	Three times faster than CTRL. Fills gap between CTRL and ACM.
SDTRL	Inverter	Yes	Resistors	Diffused mesa transistors in CTRL circuits. Gives moderate speed from simple circuits.
SDTDL	Inverter	Yes	Diodes	Uses PNP diffused mesa transistors.
DEFL	Emitter Follower	No	Diodes	Very high-speed. Uses Silicon transistors.
DDTL	Inverter	Yes	Diodes	Simple circuits using NPN diffused mesa transistors.

Figure 6. Circuit Group Characteristics

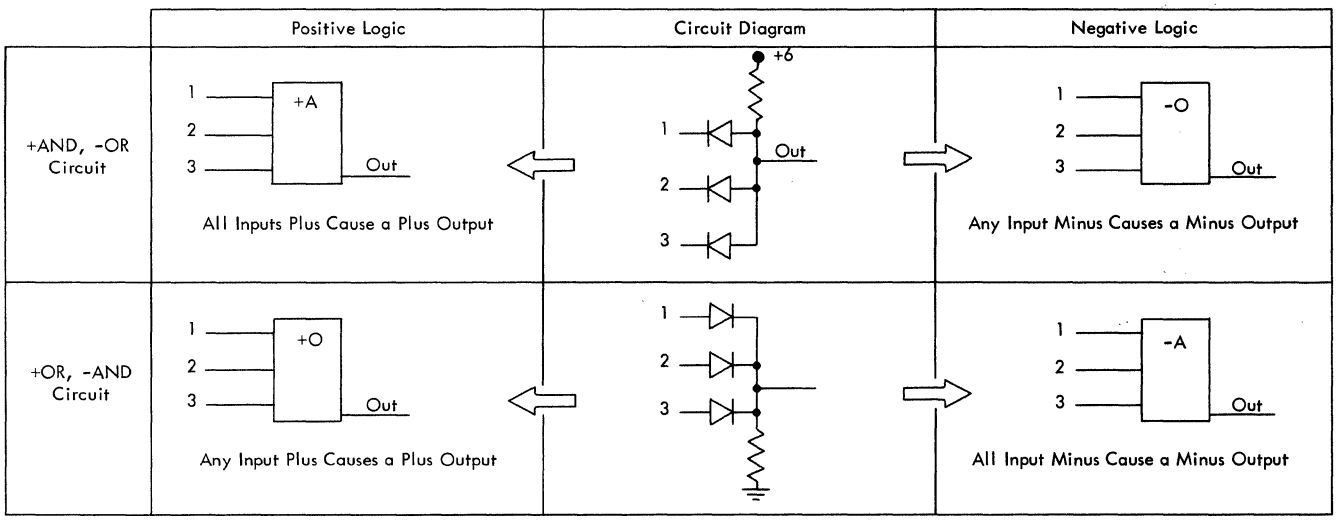


Figure 7. Positive and Negative Logic

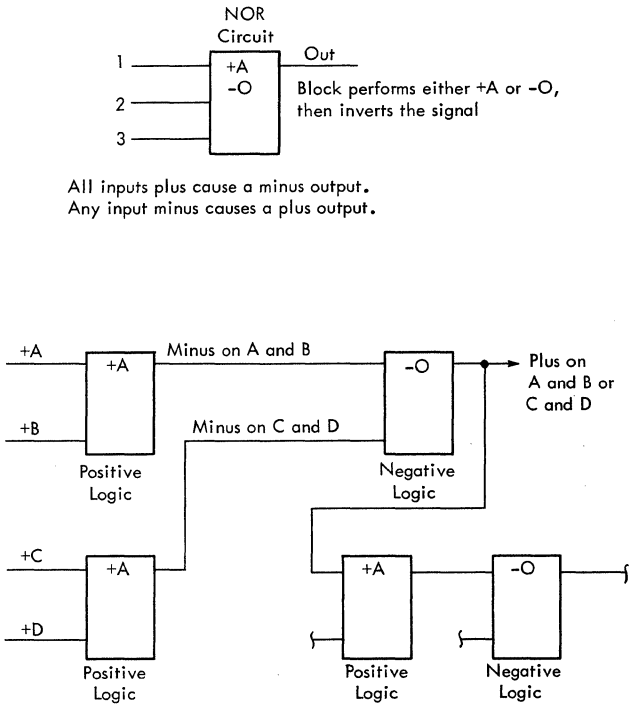


Figure 8. Alternate Positive and Negative Logic

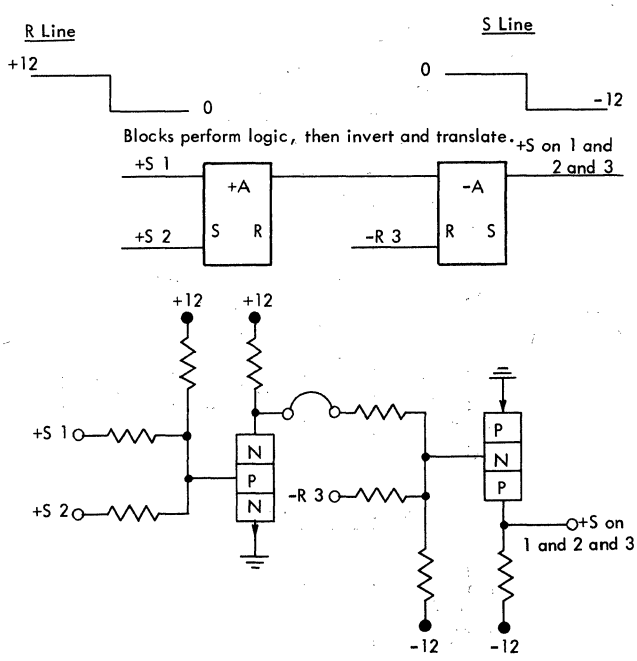


Figure 9. CTRL Translating Circuits

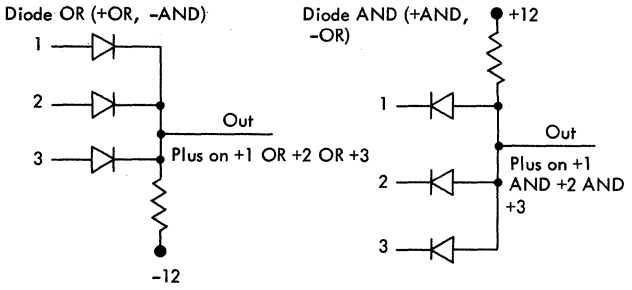


Figure 10. DDTL Diode Circuits

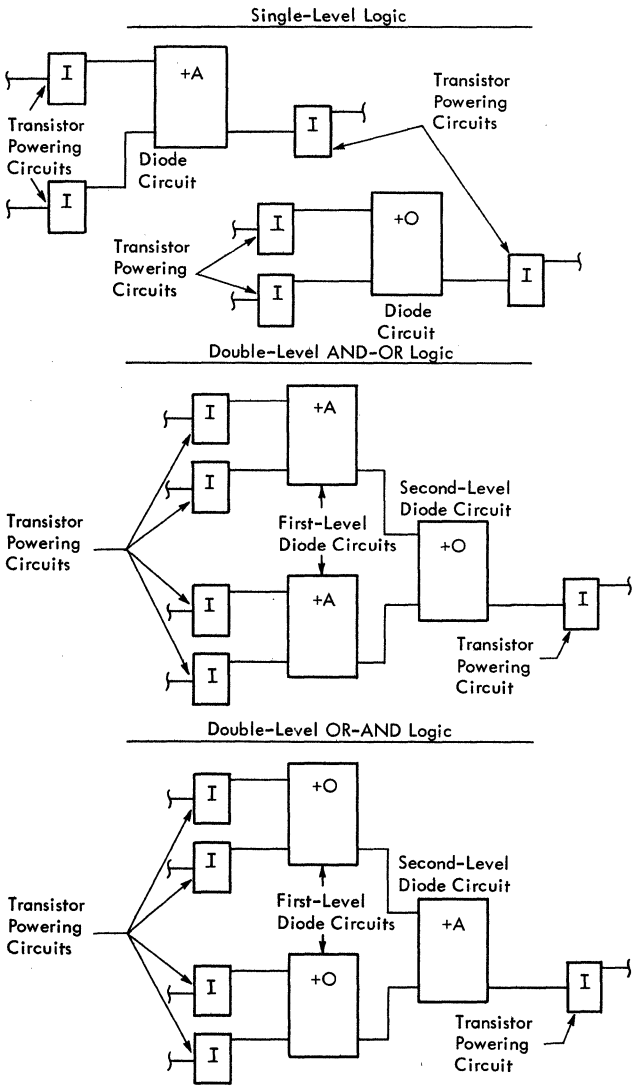


Figure 11. Single-Level and Double-Level Logic

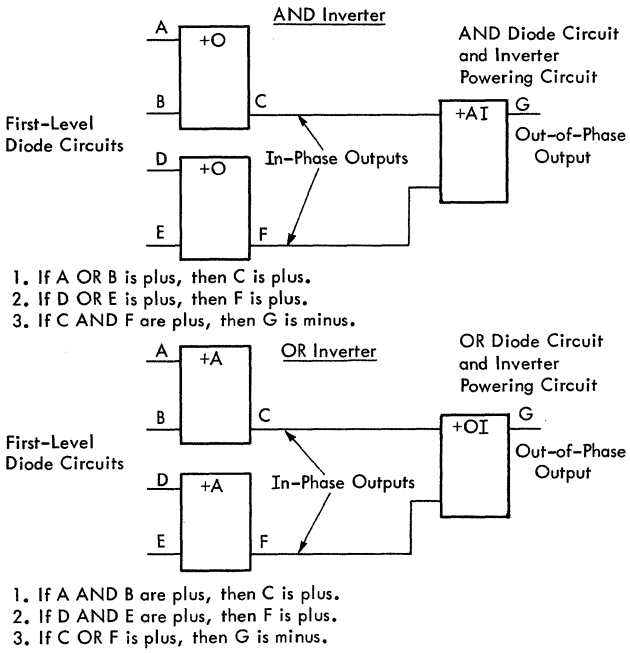


Figure 12. Combination Diode and Inverter Circuits

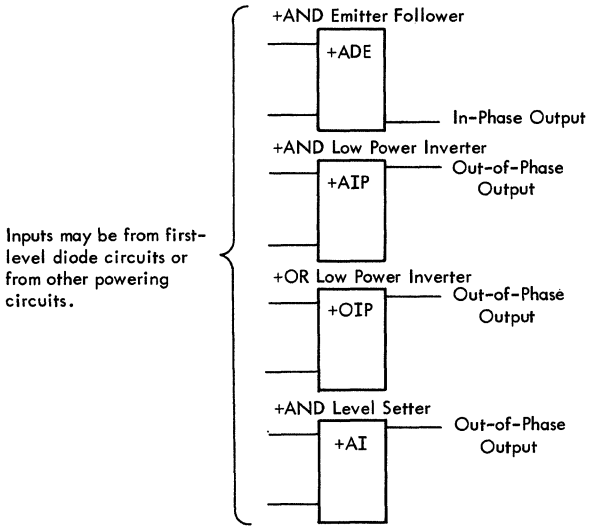


Figure 13. Combination Diode and Powering Circuit Examples

block tells whether the positive or the negative condition of inputs is active. Therefore, the reference for the system of output line placement is the sign of the block; thus, an in-phase output of a +A or a +O is plus, the out-of-phase output is minus.

DDTL circuits are non-translating. The single line level, B, is near +6v, when up, and approximately 0v, when down; each of the DDTL powering circuits, however, has unique voltage tolerances for the up and down B levels in and out. For example, an acceptable +B level can be as low as +2.7v or as high as +6.84v.

The simplest and most widely used DDTL powering circuit is the basic inverter (Figure 14). Either one or two levels of diode logic may be connected to the input of this circuit. In addition, the basic inverter may be used without diode logic to simply invert a line.

Note that the basic inverter has only four components; Figure 14 shows the general purpose of each component. The basic inverter operates as a switch; that is, with a +B input, the transistor is saturated and, therefore, is a short circuit; the output is approximately 0v. With a −B input, the transistor is cut off and, therefore, is an open circuit; the output is +6v.

The basic inverter load resistor can be one of several values. The proper value is selected depending on the number and type of loads (circuit inputs) connected to the output of the inverter. Loads can be either positive or negative; that is, a circuit may cause current to flow when given a +B (up) level or it may cause current to flow when given a −B (down) level (Figure 15). In DDTL, positive loads cause electron current to flow *into* the powering circuit; negative loads cause electron current to flow *out* of the powering circuit. Thus, positive loads lower the +B level by dropping voltage across the collector resistor; negative loads raise the −B level because they pull current from the transistor.

If the loads driven are all positive (for example, other basic inverters, Figure 15), the collector resistor value is decreased for an increased number of loads. That is, to maintain an acceptable +B level, the collector resistor of a basic inverter must be decreased in value for increased current passed through the resistor when the transistor is cut off. The value of a basic inverter collector resistor is scaled the opposite way for negative loads (current drawn when input is −B). When more negative loads are driven, a larger collector resistor is used; thus, the current that a transistor can carry in saturation is used to supply following circuits instead of simply generating heat in the collector resistor.

When a circuit drives both positive and negative loads, the value of the collector resistor must be a compromise. The compromise is necessary because *decreasing* the value of the collector resistor increases the number of positive loads that can be driven but decreases the number of negative loads that can be driven; *increasing* the collector resistor has the opposite effect.

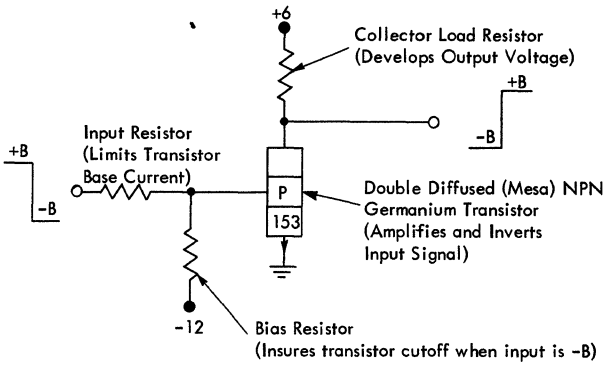


Figure 14. Basic Inverter

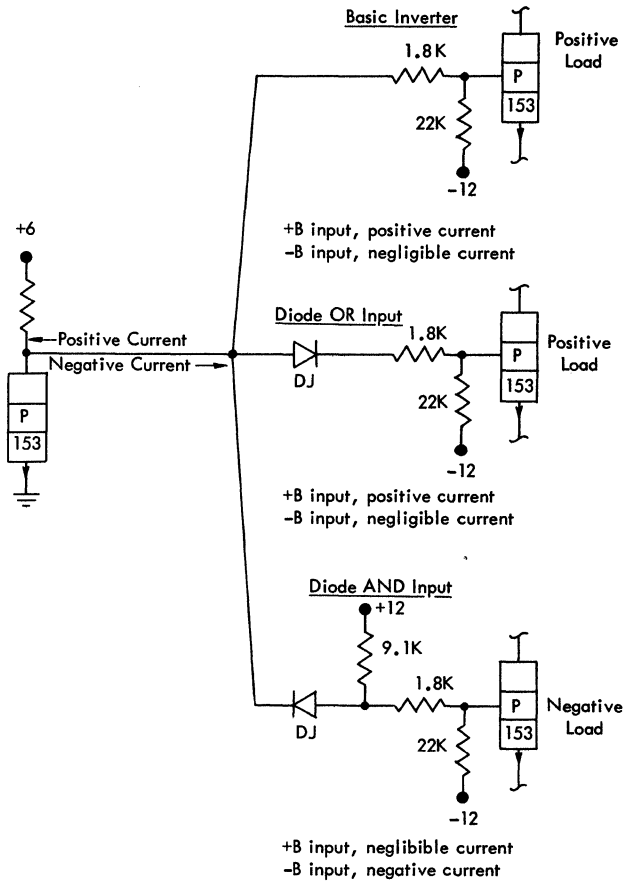


Figure 15. Types of Loads

In addition to various load resistor values, two or more basic inverters may share the same load resistor. Known as a DOT function, or DOT OR, in DDTL circuits this sharing of a common load takes the place of an AND circuit (Figure 16). The figure shows the logic of the DOT function referenced to the output of the circuits; that is, a DOT AND means that the equivalent logic is a +AND (or −OR) circuit substituted for the junction of the transistor collectors.

In Figure 16, basic inverters are used to illustrate the DOT function; the DOT function is not restricted to the basic inverter, however, and may be used with most circuits that contain a transistor. In ALD's, attention is usually called to a DOT function by an additional letter in the functional symbol; for example, two +AND inverters DOT OR'ed might be designated +AOI or +AAI. Because the sign of the DOT symbol is not designated, and because the symbol may be referenced to either the circuit inputs or the circuit outputs, the logic of these circuits is best determined by recalling (or drawing) the basic DDTL DOT as shown in Figure 16. Once you determine the convention for designating DOT functions within a particular machine, DOT logic is easily followed.

Another variation of the basic inverter is a clamped output (Figure 17). The clamped output is used when driving OR blocks to improve the rise transition of the output signal. The rise transition at the output of unclamped basic inverters is slower than the fall transition (Figure 18). The fall transition is produced when

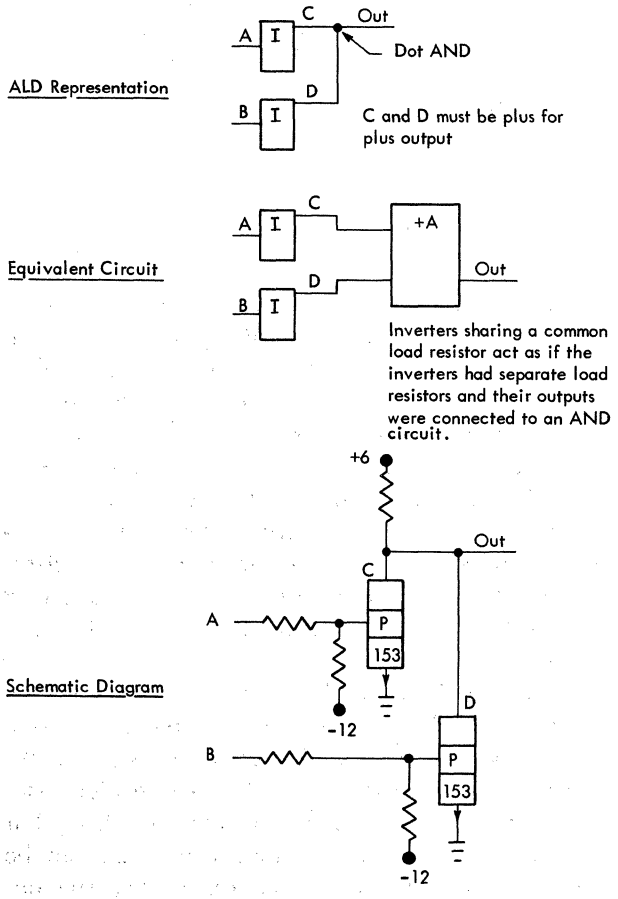


Figure 16. DOT Function

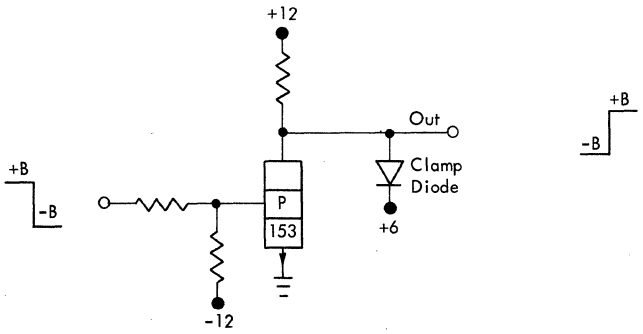
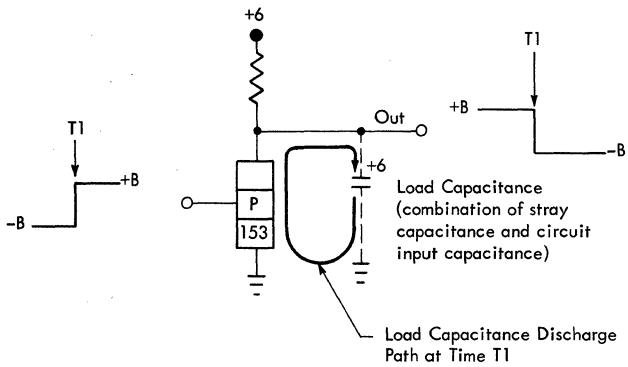
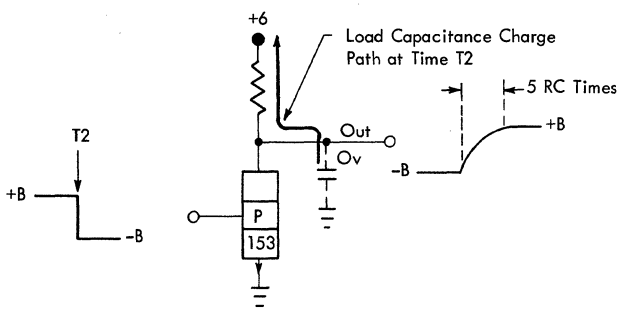


Figure 17. Basic Inverter with Clamped Output



A. Unclamped Basic Inverter Output Has Fast Fall From +B to -B.



B. Unclamped Basic Inverter Output Has Slow Rise from -B to +B.

Figure 18. Basic Inverter Output Rise and Fall

the input goes to +B and saturates the transistor (time T1, A in Figure 18). Before T1, the load capacitance (a combination of stray capacitance and the driven circuit input capacitance) was charged to +6v and must be discharged before a −B output can be obtained. At time T1, the saturated transistor is practically a short circuit across the load capacitance and, therefore, the capacitance discharges rapidly through the transistor. The slope of the fall transition is mainly determined by how fast the transistor saturates.

The output rise transition occurs at time T2 when the input falls to −B and cuts off the transistor (B in Figure 18). On this transition, the load capacitance must charge through the load resistor before the output is +B. Recall from the RC time constant theory that approximately five RC times are required for a capacitor to reach the applied voltage.

The clamped output improves the output rise transition because a greater voltage (+12) is used to charge the load capacitance (Figure 19). Because a capacitor charges to 63 percent of the applied voltage in one RC time, less than one RC time is required for the output of a clamped circuit to reach +B.

The logical low power inverter is another DDTL powering circuit. This circuit is faster than the basic inverter, and where it is used as the primary powering circuit, the logic is called high-speed DDTL, or compensated DDTL. Although the resistor values are different and a different transistor is used, except for the addition of a capacitor, the configuration of the low-power inverter is identical to the configuration of the basic inverter (Figure 20). The compensating capacitor speeds the switching time of the circuit as follows.

Because the gain of a transistor is higher at low frequencies, lower frequencies are amplified more than high frequencies. If the input to a transistor is a signal with a sharp-rising transition, the leading edge of the output loses the steepness of the input. The compensating capacitor is a short circuit to the leading edge of the signal; this supplies an instantaneous change in base current that is very large compared to the base current that is supplied through the input resistor after the compensating capacitor has fully charged. A large, instantaneous base current causes a large output and compensates for the decreased gain of the transistor at high frequencies; hence "compensating" capacitor. Similarly, the compensating capacitor bypasses the input resistor on the fall transition, cutting the transistor off more quickly; however, the compensating capacitor affects the fall transition much less than the rise transition. On the fall transition, the transistor is cut off and the principal cause of slope comes from charging the load capacitance as explained in the discussion of clamped outputs.

The compensating capacitor speeds circuit operation by shorting the input resistor (for rapid changes); however, this same action makes the circuit more

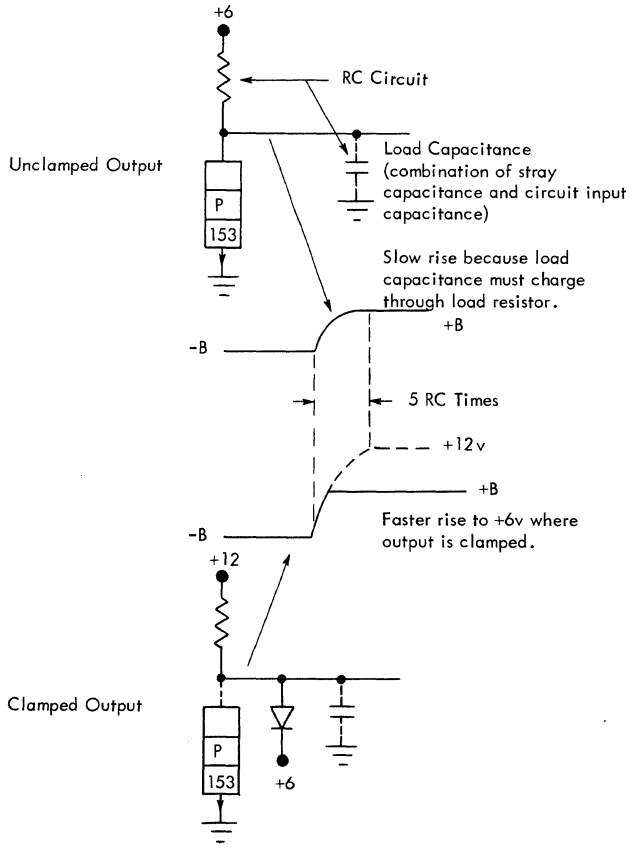


Figure 19. Rise Times of Clamped and Unclamped Outputs

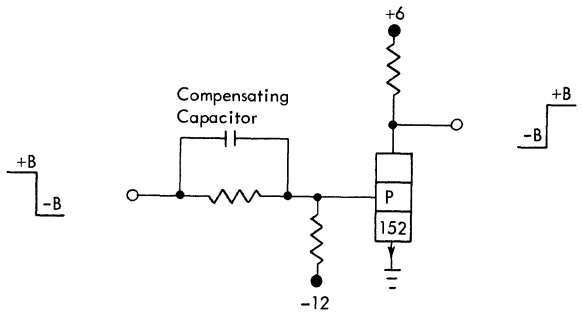


Figure 20. Logical Low Power Inverter

susceptible to noise. Because diode logic connected to the input of the circuit reduces the noise problem, the low power inverter is never used without at least one diode.

As with the basic inverter, the collector load resistor of the low power inverter can be one of several values depending on the load driven. Also, low power inverters may share a common load network to form a DOT AND; the load network can be either clamped or unclamped.

To distinguish between the basic inverter (or level setter, discussed later) and the low power inverter, ALD blocks containing a basic inverter or a level setter are labeled I, AI, or OI; those containing low power inverters are labeled IP, AIP, or OIP.

The emitter follower is another circuit used to power DDTL lines (Figure 21). Unlike the inverter circuits, the output of the emitter follower is in phase with the input, and the transistor is never saturated or cut off. Because the transistor is always conducting, the circuit output responds very rapidly to input changes. Because of the load capacitance, a peaking coil is used in the emitter circuit to further improve the square-wave response of the circuit.

A disadvantage of emitter followers is that they shift the output signal an amount equal to the emitter-to-base voltage drop of the transistor. This shift is usually about 0.4v. If several emitter followers are used in series, the signal is soon degraded to the extent that it is not a reliable input for standard DDTL circuits (Figure 22).

Because emitter followers do not exactly reproduce input voltage levels, no more than three emitter followers can be used in series; another circuit, the level setter, is required to terminate the chain and restore the degraded signal (Figure 23). Except for resistor values, the level setter is identical to the basic inverter. Each circuit in an emitter follower chain (including the level setter) can have either one or two levels of diode logic. Depending on the configuration of diode logic used, the level shift (example, Figure 22) can be aggravated by the voltage drop of the diodes; this is partly responsible for the limit of three emitter followers in any one chain.

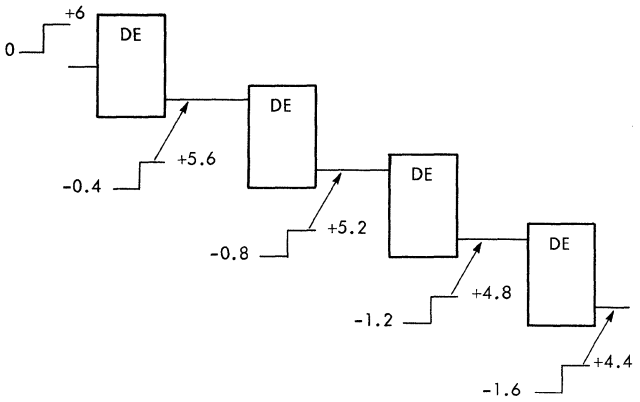


Figure 22. Characteristic Level Shift of Emitter Followers

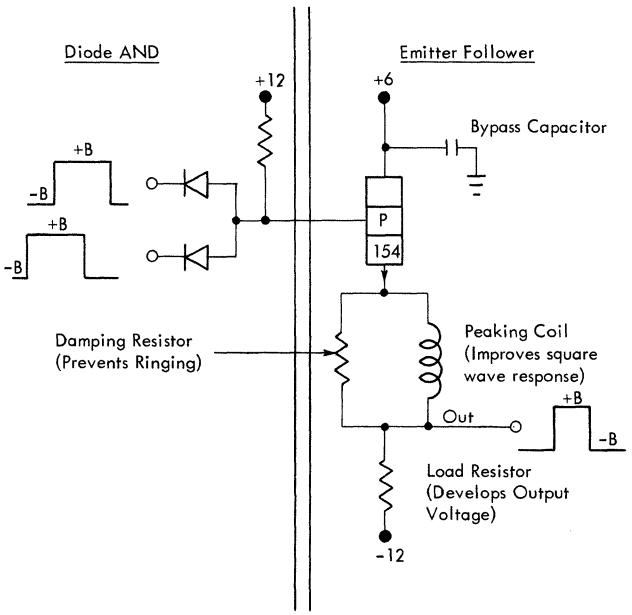


Figure 21. Emitter Follower

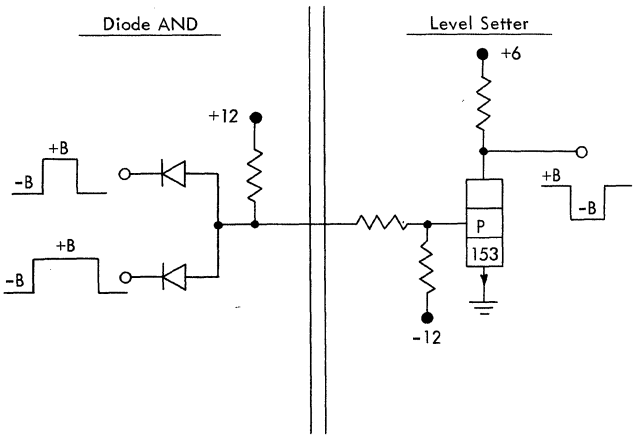


Figure 23. Level Setting Circuit

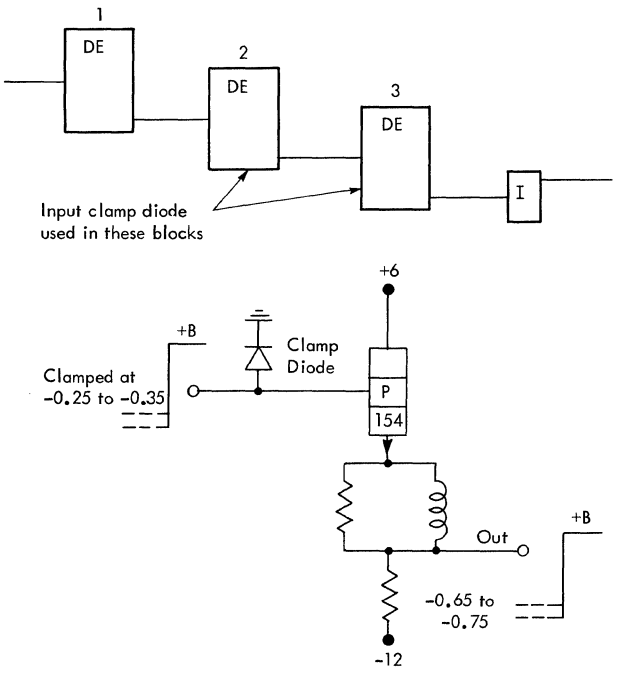


Figure 24. Clamped Emitter Follower

As with basic inverters and low power inverters, emitter follower load resistors can be one of several values depending on the load driven. In addition, an input clamping diode is usually used in an emitter follower that is the second or third circuit of a chain. This clamping diode prevents shifting the –B level below approximately –0.75v (Figure 24).

The primary characteristics of DDTL circuits are summarized in Figure 25. The "Circuit Operation" section explains standard DDTL circuits in more detail. If still greater detail is desired, refer to the Appendix for sample circuit characteristics such as currents, turn-on delays, turn-off delays, rise transitions and fall transitions.

Transistors	Double diffused (mesa) NPN germanium, operated as switches (saturated or cut off) except for emitter follower circuits.
Decision Circuits	Single or double-level diode circuits.
Powering Circuits	1. Basic Inverter 2. Low Power Inverter 3. Emitter Follower 4. Level Setter
Line Level	B Line (0 or +6) only (non-translating)
Logic	Positive, negative, or mixed logic (+AND and +OR circuits provided)

Figure 25. DDTL Characteristics

Circuit Operation

Understanding a transistor circuit can be simply knowing the logic relation of the inputs to the outputs or it can involve knowing the power dissipation of components and the relation of loading and input transition times to circuit delays. Somewhere between these extremes is an understanding of how the circuit components use the input signals to generate the output signals, and the circuit input and output requirements that must be met for proper operation.

Because this manual is for those who must service, rather than design, machines that use DDTL circuits, the depth of circuit information in this section is generally restricted to:

1. Relation of circuit inputs to circuit outputs.
2. How the circuit converts input signals to output signals.
3. Important input and output requirements.

Sample detailed characteristics such as currents, delays, rise and fall transitions, and loading requirements are included in the Appendix for those who desire more detail than is presented in this section.

This manual describes only those DDTL circuits that are most widely used. Special circuits used by a particular machine are covered in the CE manuals for that machine.

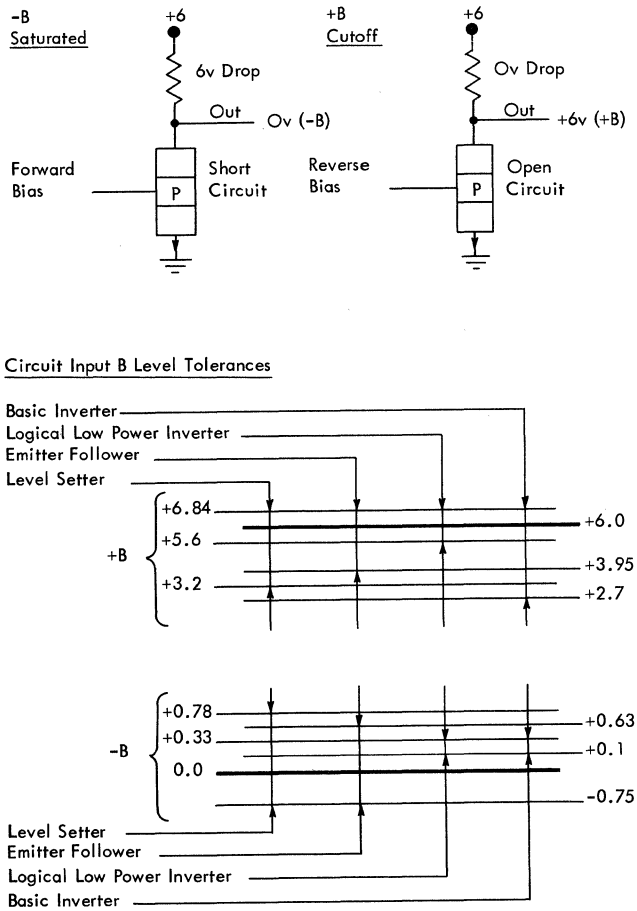


Figure 26. B Levels

Fundamental Characteristics

Line Levels

DDTL circuits are non-translating; the single line level, B, is near +6v when up, and approximately 0v, when down. The origin of the –B level is the collector of a saturated transistor whose emitter is connected to ground (Figure 26). The origin of the +B level is the collector of a cutoff transistor whose load resistor is connected to +6v.

There are four kinds of DDTL powering circuits: the basic inverter (low-speed or uncompensated DDTL), the logical low-power inverter (high-speed or compensated DDTL) the emitter follower, and the level setter. Each of these circuits has unique input voltage requirements (Figure 26). Although the nominal value for +B is 6v, note that an acceptable +B level may be as low as +2.7v or as high as +6.84v. Likewise, an acceptable –B level can be as low as –0.75v or as high as +0.78v.

Single and Double Level Diode Logic

In DDTL, diode +OR circuits and diode +AND circuits make the logic decisions. These diode circuits can be arranged in either single-level or double-level configurations. Single-level is one diode circuit between powering (transistor) circuits; double-level is two diode circuits between powering circuits (Figure 11). Double-level logic can be either diode AND's feeding a single diode OR or diode OR's feeding a single diode AND. A double-level configuration of OR's into an OR, or AND's into an AND is never used.

Diode circuits (first and second level) are generally limited to six inputs, although in a few cases, diode

circuits have up to 12 inputs. Inputs to a second-level circuit can be from transistor circuits as well as from first-level diode circuits (Figure 13).

Loading

The DDTL powering circuits can have one of several load resistors. The load resistor is the resistor in the collector circuit of an inverter, or the resistor in the emitter circuit of an emitter follower. The load resistor value is selected depending on the number and type of loads (circuit inputs) driven by a powering circuit.

Loads can be either positive or negative. A positive load is one that causes current flow when given a +B level; a negative load causes current flow when given a −B level. In DDTL, the direction of current flow caused by a positive load is opposite to the direction of current flow caused by a negative load.

Consider an inverter powering circuit and the two kinds of loads (Figure 15). Positive loads lower the +B level by dropping voltage across the collector (load) resistor; negative loads raise the −B level by dropping voltage across the transistor. To drive more positive loads, the load resistor must be decreased to prevent excessive voltage drop that would result in a +B level too low to operate the driven circuits. The limit for lowering the collector resistor is set by the maximum current that can be carried by the transistor; that is, as the collector resistor is lowered, more current must be carried by the transistor when it is turned on.

As an example of positive loading, assume that a basic inverter is to drive other basic inverters. With a collector resistor of 470 ohms (minimum value used) 7 ma (assuming an unclamped collector) of positive current will drop the +B level to +2.7v; this is the minimum allowable input to basic inverters.

$470\Omega \times 7 \text{ ma} = 3.3\text{v}$

$6.0\text{v} - 3.3\text{v} = 2.7\text{v}$

Because each basic inverter draws about 1.5 ma with a +2.7v input, one to four basic inverters can be driven. With the 470-ohm collector resistor, no negative loads can be driven because this resistor draws the maximum allowable current through the transistor when it is saturated.

The value of a basic inverter collector resistor is scaled the opposite way for negative loads. When more negative loads are driven, a larger collector resistor is used; thus, the current that a transistor can carry in saturation is used to supply the following circuits instead of simply generating heat in the collector resistor.

As an example of negative loading, assume that a basic inverter is to drive diode AND inputs that are connected to other basic inverters (Figure 15). If the collector resistor is 1.8K (maximum value used), an external current of 10.2 ma (negative current) can be safely drawn through the transistor. This current is in addition to that drawn by the 1.8K collector resistor. Because each AND input draws approximately 1 ma, one to ten of these inputs can be driven.

When a circuit drives both positive and negative loads, the value of the collector resistor must be a compromise. The compromise is necessary because decreasing the value of the collector resistor increases the number of positive loads that can be driven but decreases the number of negative loads that can be driven; increasing the collector resistor has the opposite effect.

DOT Function

By sharing a common collector resistor, DDTL inverter powering circuits can perform an additional logic decision. As many as six inverter collectors may be connected together and share a single resistor (Figure 16). Known as a DOT function, or DOT OR, in DDTL circuits this sharing of a common load resistor takes the place of a +AND or a −OR. In a DOT configuration, the conduction of any transistor drops the output to −B; therefore, the logic performed by the DOT is −OR. Considering the DOT in positive logic, all transistors must be cut off to obtain a +B output (+AND).

In ALD's, attention is usually called to a DOT function by an additional letter in the functional symbol; for example, two +AND inverters DOT OR'ed might be designated +AOI or +AAI. Because the sign of a DOT symbol is not designated, and because the symbol may be referenced to either the circuit inputs or the circuit outputs, the logic of these circuits is best determined by the recalling (or drawing) the basic DDTL DOT as shown in Figure 16. Once the convention for designating DOT functions within a particular machine is determined, the DOT logic is easily followed.

Basic Circuits

Diode Circuits

There are two DDTL diode circuits: +AND and +OR (Figure 27). These diode circuits are primarily for first-level or single-level use and are shown as a separate block in Systems. Second-level diode circuits are normally part of an inverter or emitter follower powering circuit and are included in the Systems block with the powering circuit (e.g., +OI, +ADE).

The limit on the number of inputs used in diode circuits is set because of diode back-current. Although reverse biased diodes have a high resistance, a small current flows from the anode to the cathode. For example, consider the diode +AND with one input at

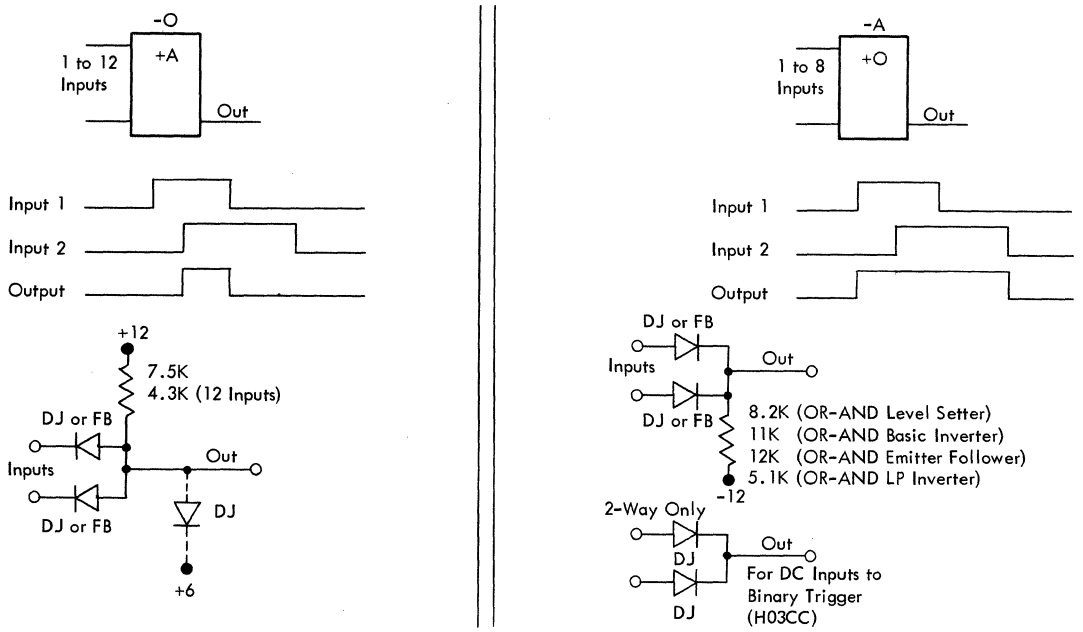


Figure 27. Diode Circuits

−B and all other inputs at +B. The −B input will hold the common anode at 0v; a small reverse current will flow through each of the remaining diodes and these currents will add to the current flowing through the one forward-biased diode. These back currents cause additional loading on the one −B input and, if too many inputs are added, the maximum current capacity of this diode will be exceeded.

Basic Inverter

The basic inverter is the simplest DDTL powering circuit. It is the most widely used powering circuit in uncompensated (low-speed) DDTL logic.

The basic inverter can be used alone, or with one or two levels of input diode logic. Because the diode circuits may be either +AND or +OR, five basic inverter configurations are used (Figure 28):

1. Basic inverter (I).
2. AND inverter (+AI).
3. OR − AND inverter (+O, +AI).
4. OR inverter (OI).
5. AND − OR inverter (+A, +OI).

Considering the basic inverter used alone, a −B input places the transistor base at about −0.6v to −0.8v, depending on whether the −B input is near +0.1v or +0.33v. This base voltage results from the voltage divider from −12M (1.8K and 22K resistors). The negative bias is sufficient to keep the transistor cut off; the output is +B from the collector supply voltage through the collector resistor.

With a +B input, the transistor base is driven positive and the transistor saturates. When saturated, the transistor draws base current sufficient to place the base at +0.44v. The 1.8K input resistor limits this base current to a safe value for the range of acceptable +B inputs (+2.7v to +6.84v).

The basic inverter may have either a clamped or an unclamped collector circuit. The unclamped circuit is simply a resistor to +6v. The resistor is one of four values, depending on the load to be driven (Figure 28). The clamped circuit is a resistor to +12v and a clamp diode that prevents the output from rising higher than about +6.84v. The extra 0.84v (above 6.0v) is caused by the drop of the DJ clamp diode and allowable variations of the +6v power supply. The resistor used in the clamped circuit can also be one of four values depending on the load to be driven.

The clamped output gives a faster rise from −B to +B as explained previously (Figure 19). In addition, a clamped basic inverter will drive a greater number of positive loads than an unclamped inverter. Recall from the discussion of loading that the limit for lowering a collector resistor (to increase positive load driving capabilities) is set by the maximum current capability of the transistor. Consider clamped and unclamped circuits such as shown in Figure 19. If the collector resistor in the clamped circuit is twice as

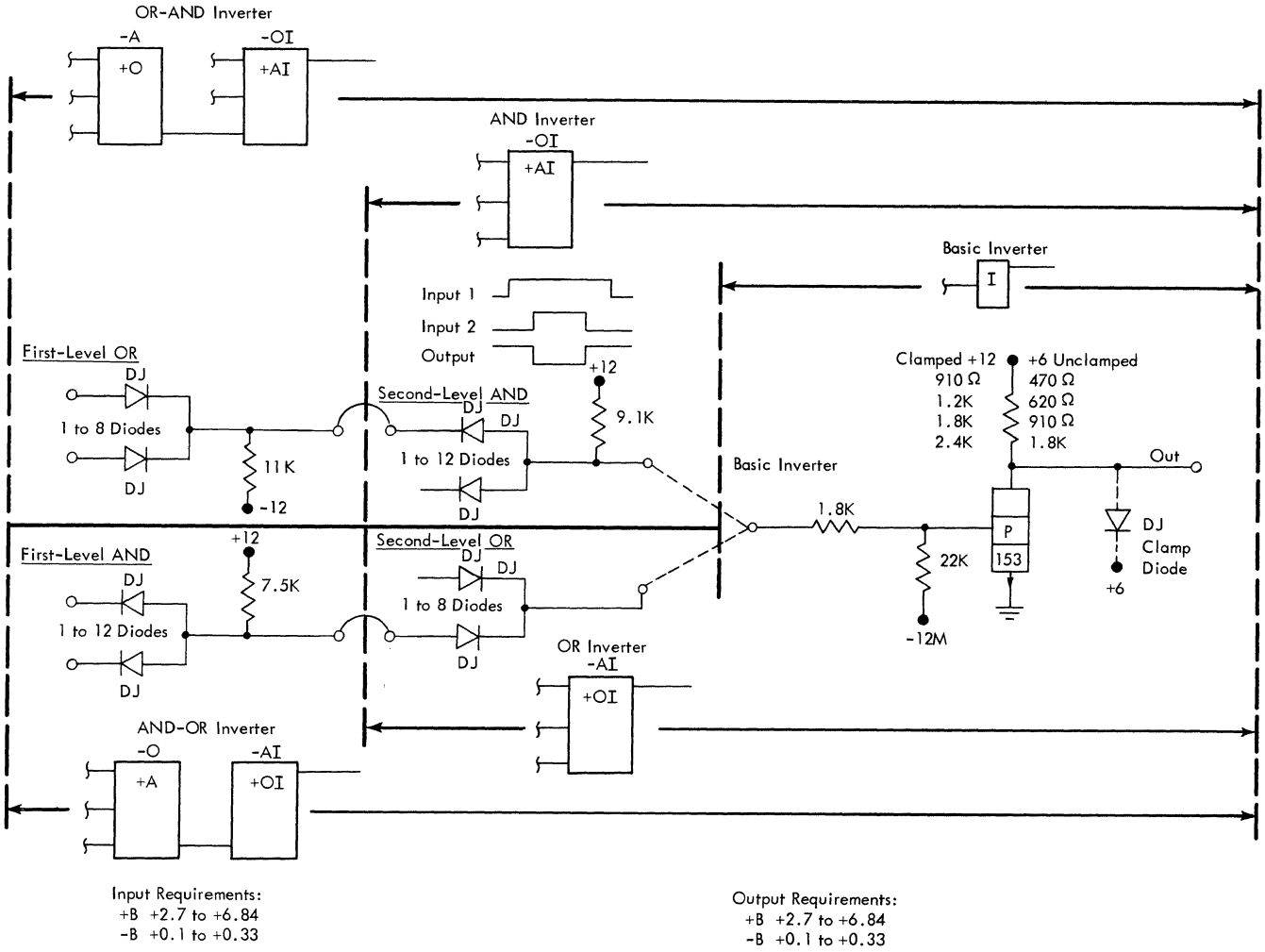


Figure 28. Basic Inverter with Diode Logic

large as the collector resistor in the unclamped circuit, an equal amount of current will flow through the two resistors when the transistors are saturated. When the transistors are cut off, the clamped load resistor can drop 9.3v before the lower +B limit of +2.7v is reached; the unclamped resistor can drop only 3.3v. Because the clamp circuit resistor is twice as large as the unclamped resistor, the current that drops the unclamped output 3.3v will drop the clamped output 6.6v. A drop of 3.3v is the limit for the unclamped output and the +B level is +2.7v. A drop of 6.6v on the clamped output, however, is not the limit and the +B level is +12v −6.6v = +5.4v. Additional positive loads can be tied to the clamped output until the +B level drops to +2.7v.

Consider the AND inverter (Figure 28). If any input is −B, the common anode of the diodes is clamped to −B and the basic inverter receives a −B input to supply a +B output. If all inputs are +B, the +12v source supplies the basic inverter with a plus voltage through the 9.1K resistor. The basic inverter transistor is driven to saturation and the output is −B. In this condition, the input diodes are reverse biased because the transistor base is clamped to about +0.44v when the transistor is saturated. The voltage divider, consisting of the 1.8K and the 9.1K resistors, places the input diode anode at about +1.9v and the diodes are cut off.

Inputs to the AND inverter can be from transistor circuits or from first-level OR's. In the latter case, the entire circuit becomes an OR-AND inverter (Figure 28).

In the +OR inverter, any +B input clamps the common diode cathodes to +B, reverse biasing all other input diodes. The output of the basic inverter is −B.

If all inputs are at −B, the diode cathodes follow the −12M supply down to the most positive −B input; this input clamps the cathodes to its voltage. The −B input to the basic inverter cuts off the transistor, causing a +B output.

Inputs to the OR inverter can be from transistor circuits or from first-level AND's. If first-level AND's are used, the circuit becomes an AND − OR inverter (Figure 28).

Logical Low Power Inverter

The logical low power inverter is the primary powering circuit for compensated (high-speed) DDTL logic. The circuit configuration is similar to the basic inverter; however, note the following differences (Figure 29):

1. Different transistor.
2. Different resistor values.
3. Addition of a compensating capacitor.
4. Cannot be used without diode logic.
5. Different input and output requirements.

The logical low power inverter is faster than the basic inverter primarily because of the compensating capacitor. This capacitor speeds the switching time of the circuit because it shorts the input resistor during signal transitions. This shorting supplies a momentary large base current that forces the transistor to react faster. Although the compensating capacitor affects both rise and fall transitions, the output rise transition (input fall) is not improved as much as the fall transition. A clamped output is used when a sharper rise transition is required. Refer to the "DDTL Characteristics" section for a more detailed discussion of the compensating capacitor.

The operation of the low power inverter is identical to the operation of the basic inverter: a −B input cuts the transistor off and the output is +B from the collector supply voltage; a +B input saturates the transistor and the output is −B (Figure 29).

As with the basic inverter, both clamped and unclamped collector circuits are used. Also, the load resistor value is changed to meet the requirements for the number and type of loads driven.

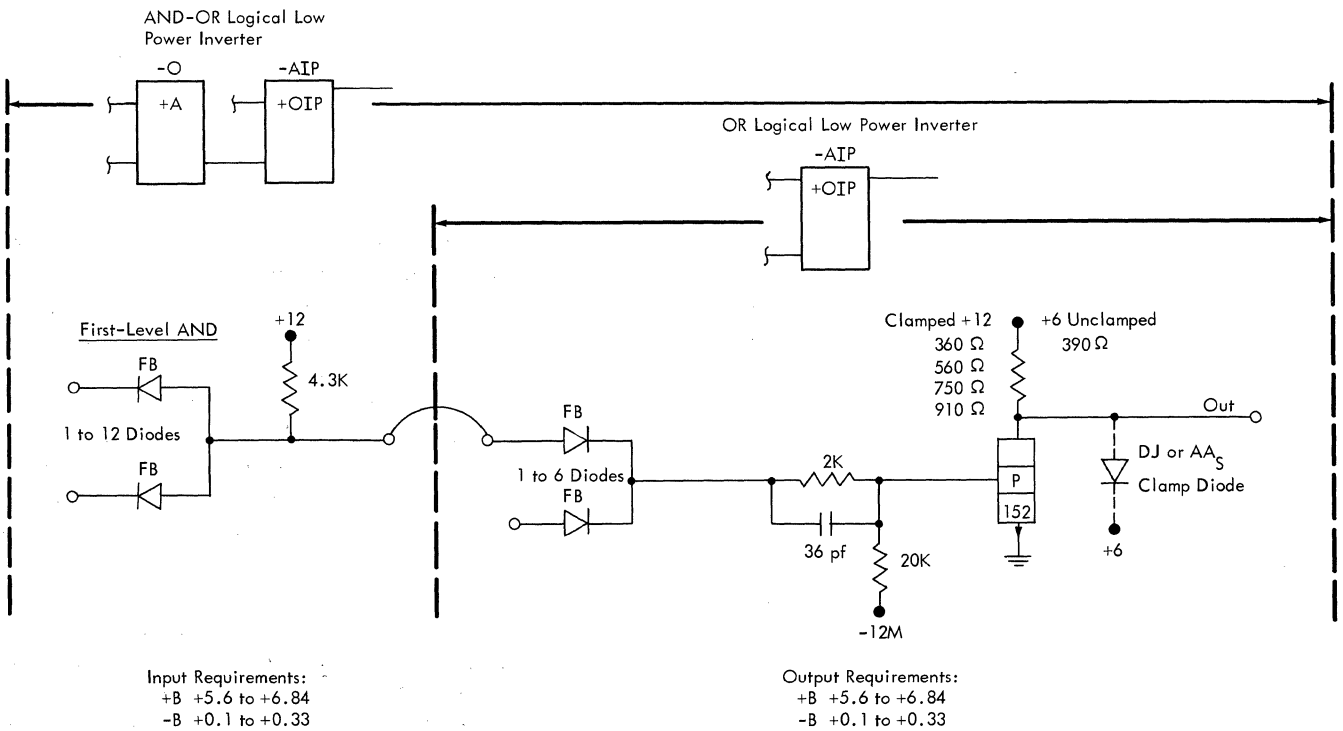


Figure 29. OR Logical Low Power Inverter

Either one or two levels of diode logic can be used at the input of the low power inverter. As with the basic inverter, the double level configurations are AND – OR inverter (Figure 29) and OR – AND inverter (Figure 30). The diode circuits perform logic exactly as the diode circuits described for the basic inverter. Note, however, that these circuits are not interchangeable with the diode circuits used with the basic inverter; a different type of diode is used and the resistor values are different.

Because of the compensating capacitor, the logical low power inverter is more sensitive to noise than the basic inverter. To reduce the possibility of noise pulses operating these circuits, input signals to the low power inverter must pass through at least one diode. If the circuit is used simply as an inverter, a +OIP, or a +AIP with only one input diode is used. In this case, the Systems block will have only one input and may be labeled IP.

Systems blocks containing +OIP's and +AIP's are sometimes labeled +O, +A, and I, or +OI, +AI, and I. These cases generally occur where an entire machine uses compensated DDTL (no basic inverters) or where there is a DOT function. Because a DOT function adds an additional letter to the functional symbol, the Systems block limit of four characters is exceeded when a +AIP or a +OIP is DOT'ed. For example, in one convention used, a DOT'ed +OIP (+OOIP) is shortened to +OO; a DOT'ed +OI (basic inverter) has its full designation of +OOI.

Emitter Follower Chain

Emitter follower chains consist of emitter followers and level setters. Because emitter followers shift the input signal an amount equal to the base-to-emitter drop of the transistor used, the purpose of the level setters is to restore the degraded B level at the end of the emitter follower chain. The chains are limited to three emitter followers (Figure 31). In an emitter follower chain, each emitter follower and the level setter can have one or two levels of diode logic.

The speed of an emitter follower chain is comparable to the speed of an equivalent number of logical low power inverters; therefore, these circuits can be used in compensated logic. Like the low power inverter, signals into an emitter follower must pass through at least one diode. However, unlike the low power inverter, only a +AND emitter follower is used. The only double-level logic configuration is the OR – AND emitter follower (Figure 32).

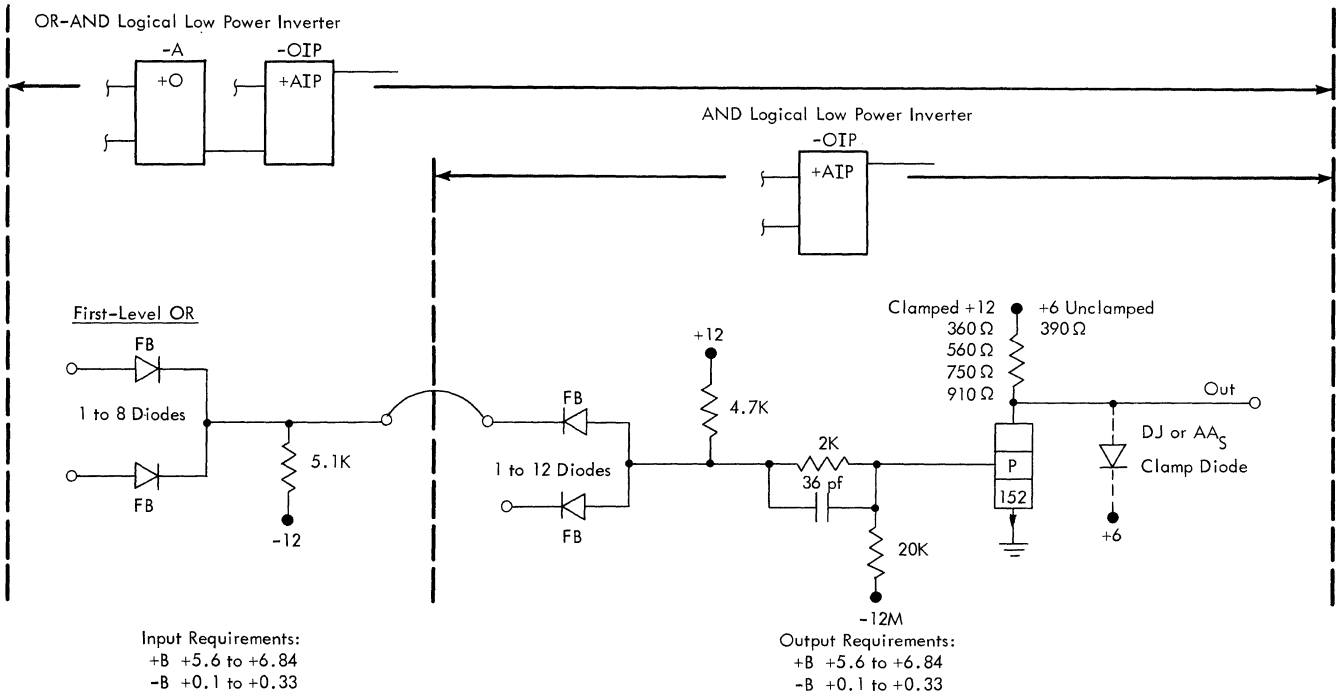


Figure 30. AND Logical Low Power Inverter

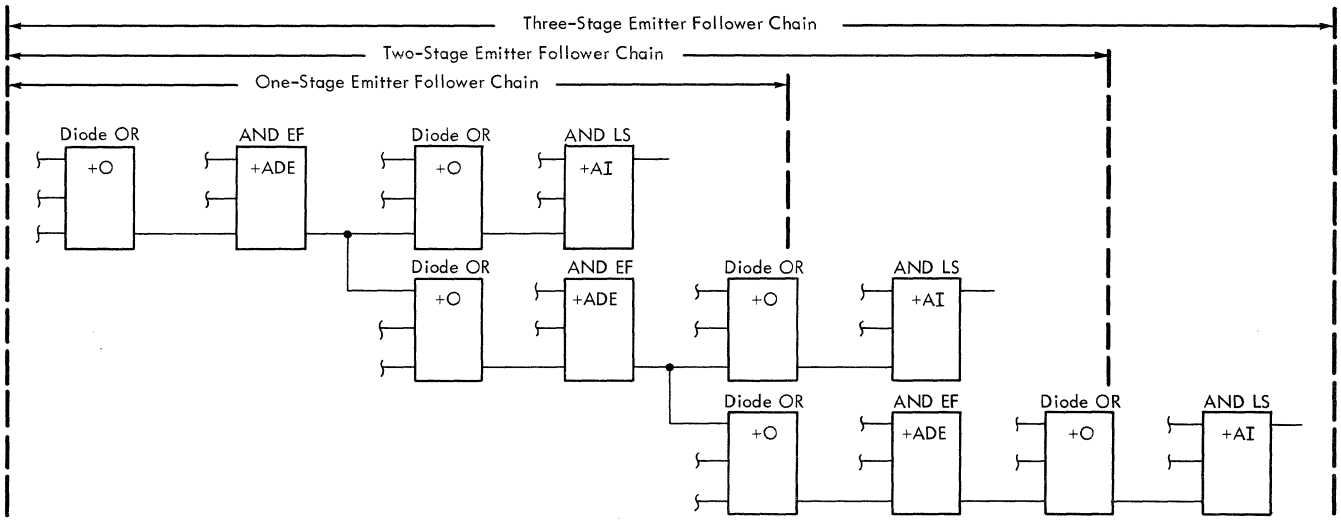
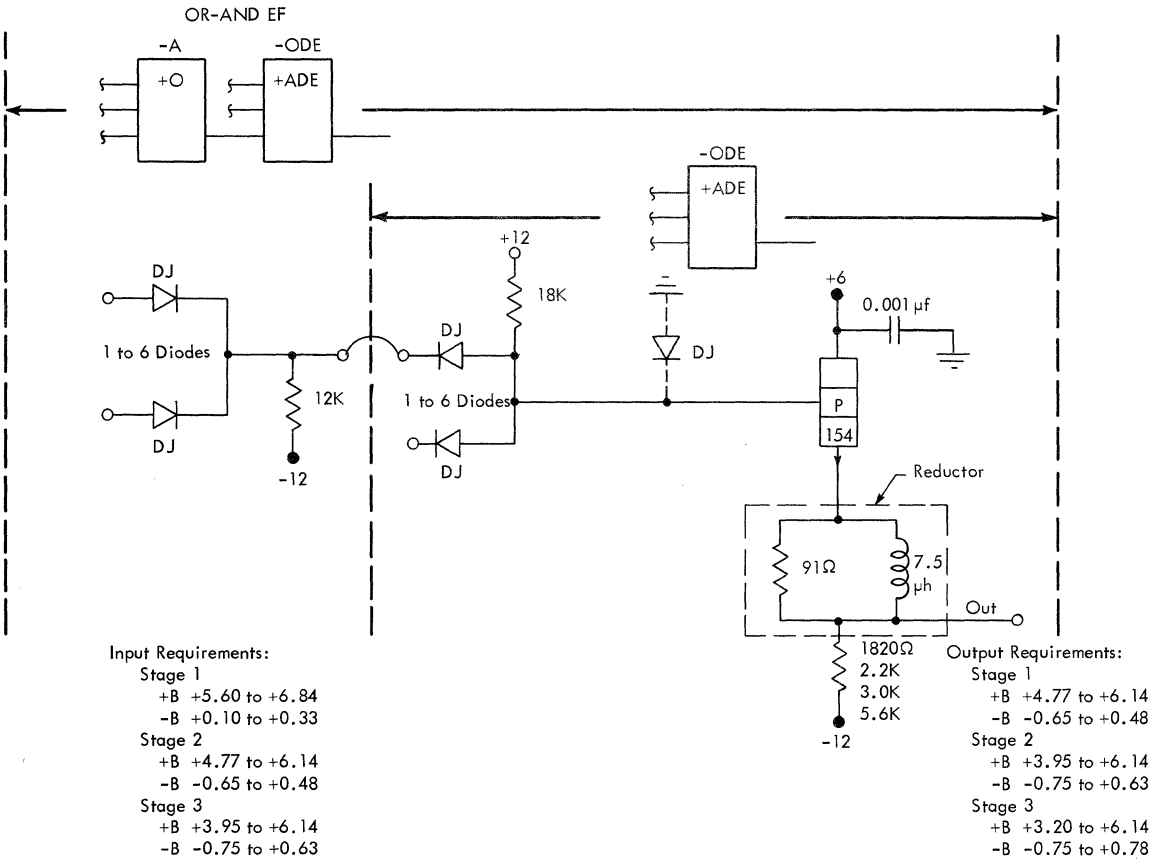


Figure 31. Emitter Follower Chain



Input Requirements:
Stage 1
+B +5.60 to +6.84
-B +0.10 to +0.33
Stage 2
+B +4.77 to +6.14
-B -0.65 to +0.48
Stage 3
+B +3.95 to +6.14
-B -0.75 to +0.63

Output Requirements:
Stage 1
+B +4.77 to +6.14
-B -0.65 to +0.48
Stage 2
+B +3.95 to +6.14
-B -0.75 to +0.63
Stage 3
+B +3.20 to +6.14
-B -0.75 to +0.78

Figure 32. AND Emitter Follower

An emitter follower transistor always conducts and is never saturated or cut off. The circuit responds rapidly to input changes because the transistor does not have to be brought out of saturation or cut off to the opposite extreme. Unlike inverters, the emitter follower load resistor is in the emitter circuit (Figure 32) and the output is in phase with the input. Note that the load resistor can be one of four values depending on the number and type of loads driven.

The DDTL emitter follower operates much the same as a tube cathode follower. As the input goes to +B, the transistor conducts harder dropping more voltage across the load resistor until the emitter voltage closely approximates the base voltage. The emitter voltage, however, is slightly negative (about 0.4v) with respect to the base. This is the bias, or the base-to-emitter voltage drop, of the transistor. On the signal swing from +B to −B, the transistor conduction reduces until the emitter voltage is again about 0.4v more negative than the base.

The coil resistor combination (reductor) in the emitter circuit helps compensate for the capacitance of the load and thereby improves the squarewave response of the circuit. The 0.001 uf bypass capacitor prevents coupling the rapid current changes to other circuits.

The DJ clamp diode at the transistor base is used only if the circuit is the second or third emitter follower in a chain. This diode prevents the base voltage from going more negative than approximately −0.3v (drop of DJ diode). By using the clamp diode, the −B output of second and third stage emitter followers will not go below −0.75v (drop of DJ diode plus transistor emitter-to-base drop).

To restore the degrated B level from emitter followers, a level setter (Figure 33) terminates each chain. Except for resistor values, the level setter is identical to the basic inverter. Note that this difference of resistor values results in different input voltage requirements; these voltages match the B levels out of emitter followers.

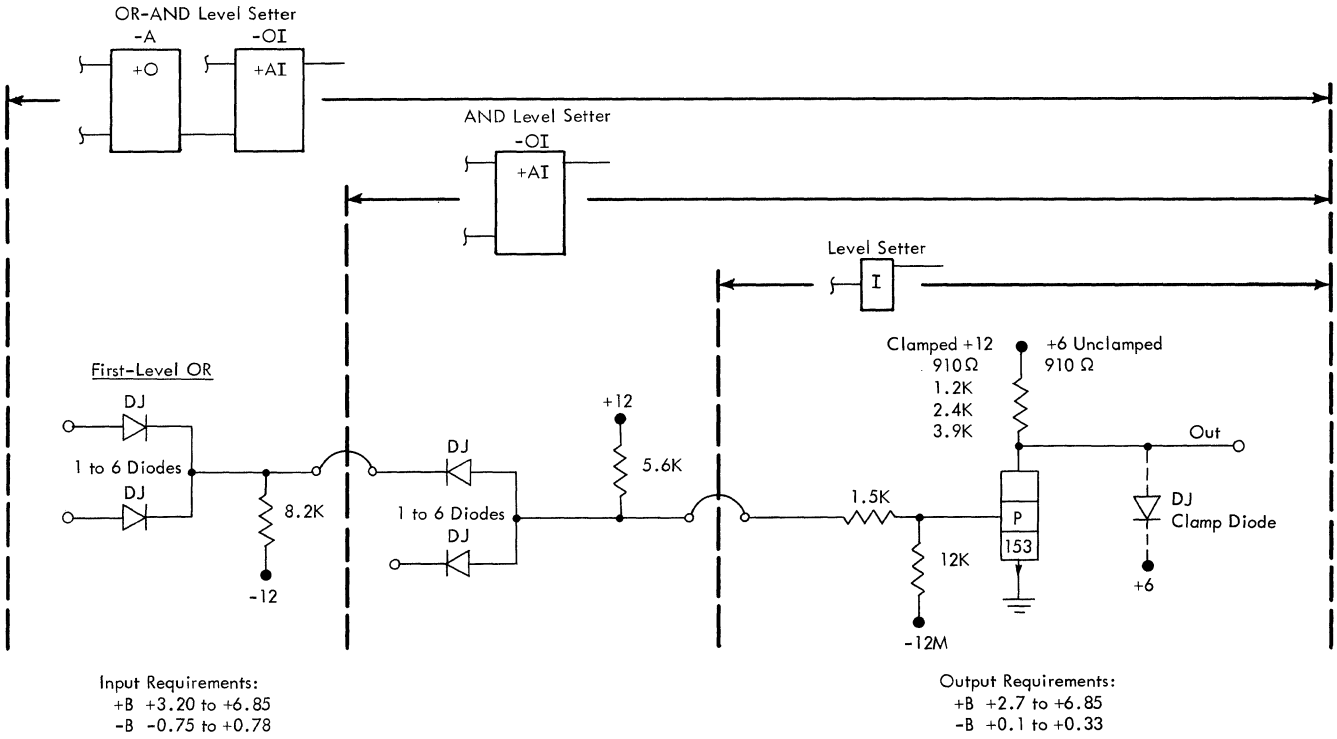


Figure 33. Level Setter

A level setter may be used alone or with one or two levels of diode logic. The configurations used are level setter (I), AND level setter (+AI), and OR – AND level setter (+O, +AI). As with the basic inverter, the output may be either clamped or unclamped.

Powered Inverter

The powered inverter (Figure 34) is used to drive loads that are too great for an inverter or a level setter. The circuit has two out-of-phase outputs; one is a low-power output, the other is a high-power output.

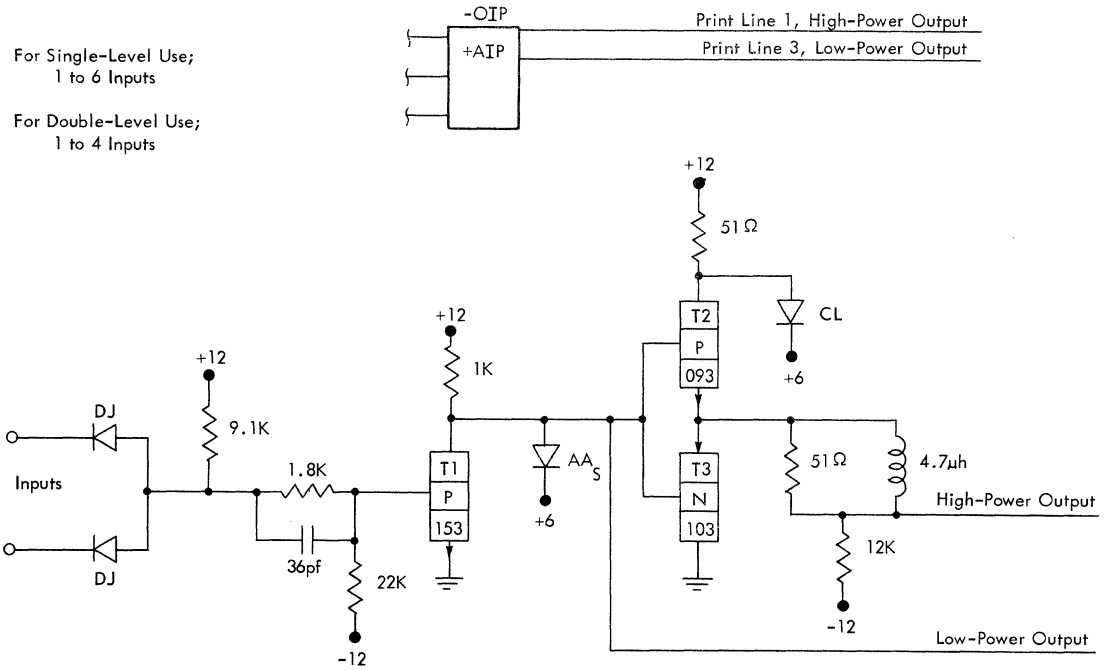
This circuit is a combination of a clamped AND low power inverter and a pair of complementary emitter followers. The inverter works the same as the low power inverter and the low power output is from this circuit. The low power inverter output also feeds the complementary emitter followers. The output from the emitter followers is never passive; one transistor drives it in the positive direction and the other, in the negative direction.

When the low power inverter output is +B, T2 conducts to bring the common emitter circuit (and the output) to approximately the same voltage applied to the T2 base. (If the T2 input is too positive, the CL diode will clamp the T2 collector, thereby limiting the +B output to about +6.75v.) In this state, T3 is cut off because its base is positive with respect to its emitter by an amount equal to the emitter-to-base voltage drop of T2. As the low power inverter output goes to –B, T3 turns on and T2 is cut off by the emitter-to-base voltage drop of T3.

Triggers and Latches

Triggers and latches are bi-stable circuits that store one of two conditions. Among their many applications, they are used for registers, counters, and rings.

A trigger is a bi-stable multivibrator and usually requires an AC shift (trigger) to change it from one state to the other. Included in the circuit, however, there may be provisions for gating (AND function) and



Input Requirements:

+B +2.7 to +6.84
-B +0.1 to +0.33

Output Requirements:

High-Power Output	+B +5.58 to +6.75 -B -0.32 to +0.33
Low-Power Output	+B +2.70 to +6.84 -B +0.10 to +0.33

Figure 34. Powered Inverter

for DC sets and resets. This circuit is also called a flip-flop.

A latch is a DC device, usually made up of an AND and an OR, two AND's or two OR's (Figure 35). The output of each half of a latch is one input to the other half. This arrangement is called cross-coupling and the lines from one half of the latch to the other half are called feedback or latchback lines. The latchback lines hold the latch in the state caused by the last active input (set or reset), even if this input has returned to its inactive state. The state of a latch is changed by breaking the active latchback loop; this, in turn, activates the other latchback loop.

Three common DDTL triggers and a latch are described in this section. The latch is one shown as a single block in Systems diagrams. Many other latches are used; however, these are made up of two or more standard circuits with the cross coupling shown on the Systems diagrams. A number of latch examples taken from Systems are shown and described in the "Packaging and ALD Information" section of this manual.

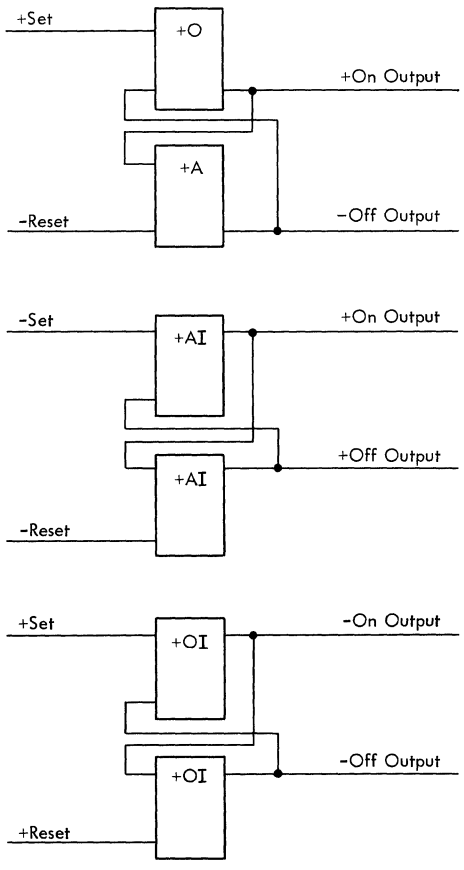


Figure 35. Example Latches

Binary Trigger

The binary trigger is the simplest and most commonly used DDTL trigger. The circuit has only two transistors (Figure 36).

The ALD representation of this circuit is shown at the top of the figure. Note that input and output lines are labeled according to the vertical position where they enter or leave the block. This designation of the lines is necessary because card pin letters are unique for a particular card; a DDTL circuit is not restricted to a particular card. In fact, in most cases, a given circuit is packaged on a great number of different cards. In addition, a circuit may be duplicated several times on one card; each circuit on a card necessarily has unique input and output pins.

The binary trigger has —AC set and reset inputs, +DC set and reset inputs, and sometimes has collector pullover set and reset inputs. The two AC inputs may come from separate sources, or they may be connected together and driven from a single source. In the latter case, each minus shift causes the trigger to change state; if the first shift turns the trigger on, the second will turn it off, the third will again turn it on, and so forth. This change of status from a single input is called binary operation, or complementing the trigger. When this arrangement is used, the Systems block will either show the single AC input connected to both 4 and 7 or connected to only 4 with no input at 7. The AC input must have a fall transition of 125 ns or less, measured from the 10 percent to 90 percent points on the waveform.

The DC inputs cannot be connected together to cause binary operation of the trigger. These inputs must be driven from separate sources. Both the AC and the DC inputs must be driven from a clamped inverter (or level setter) circuit.

Like the DC inputs, the collector pullover inputs must be driven from separate sources. Each of these inputs is a DOT connection to one of the trigger transistors. For example, assume that a collector pullover transistor is connected to input 2 (Figure 36). If either T2 or the collector pullover transistor conducts, the on output (3) is —B. The feedback from the on output (T1 collector) to the T2 base cuts off T2.

As previously discussed, simultaneous AC set and reset inputs change the state of the trigger. Simultaneous DC set and reset inputs, or simultaneous collector pullover set and reset inputs hold both on and off outputs at —B. Also, both outputs are active if one transistor is held in conduction by a DC input and the other output held at —B by a collector pullover. In these cases, the final state of the trigger is controlled by the last remaining active input.

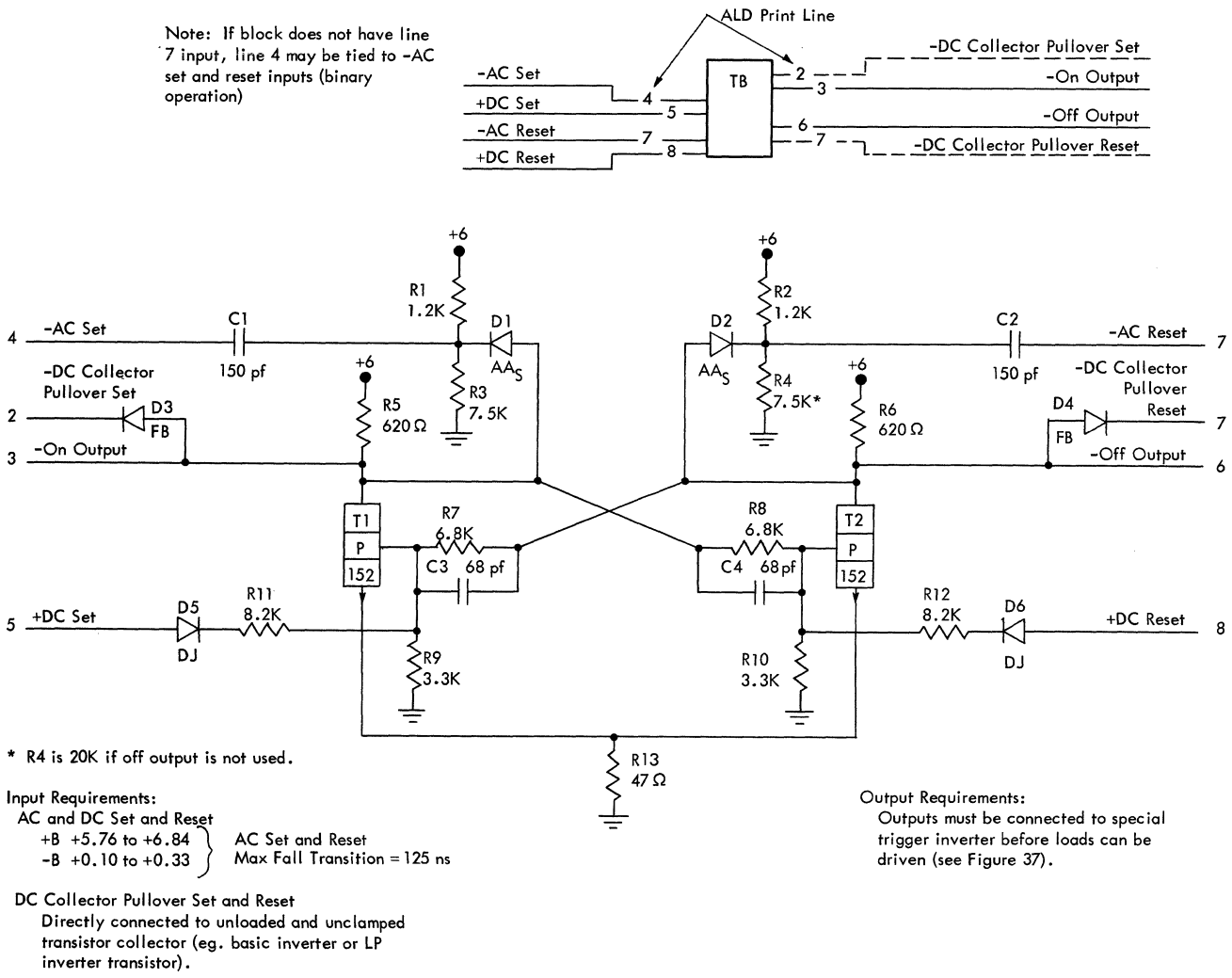


Figure 36. Binary Trigger

The operation of the binary trigger is as follows (Figure 36). Assume that the trigger is off; transistor T2 is conducting and its current sets the common emitters slightly positive (about +1.0v). The T2 collector is slightly positive with respect to the common emitters because of the voltage drop across the transistor. The T2 collector is about +1.5v. The voltage divider consisting of R7 and R9 places the T1 base at about +0.5v (one-third of the T2 collector voltage). Because the T1 base is 0.5v negative with respect to the common emitters, T1 is held cut off.

With T1 cut off, its collector is positive and this voltage is applied through R8 to keep T2 in full conduction. In this state, D2 is reverse biased; a reset input at 7 would not be coupled through D2 and, therefore, would not affect the circuit.

With the trigger off, assume that a −AC set input is received (4). Diode D1 is forward biased; the negative shift is coupled through D1 and R8 to the T2 base, cutting off T2. The common emitters go to ground potential, and at the same time, the T2 collector goes positive driving the T1 base positive through R7. Transistor T1 is forward biased and begins conducting. The common emitters go slightly positive again, this time because of the T1 conduction. The low T1 collector voltage through R8 holds T2 cut off, the same way that T1 was previously held off by the T2 collector. The on output is near ground and the off output is at +6v.

Capacitors C3 and C4 speed the switching time of the transistors by shorting the base resistors during transitions.

If the AC set and reset inputs are tied common, a negative shift will reach only the conducting transistor base because one of the two input diodes (D1 or D2) is always reverse biased.

A DC input forces the appropriate transistor into conduction by driving its base positive. Once conduction has started, the low collector voltage cuts off the other transistor.

A collector pullover input pulls the collector of the non-conducting transistor to −B. This voltage cuts off the conducting transistor, allowing its collector to rise to +B. The positive collector voltage brings the other transistor into conduction and the trigger remains in its new state even though the pullover transistor is turned off.

The binary trigger cannot directly drive standard DDTL circuits for two reasons:

1. The −B output of the trigger is more positive than the acceptable limit for standard circuits.
2. Loads would upset the balance of the circuit unless the on and off output were loaded exactly the same.

A special circuit, the binary trigger inverter (Figure 37), is used as a buffer between the binary trigger and the load to be driven. This circuit operates the same as a clamped low power inverter, but different resistor values are used to compensate for the abnormal −B level from the binary trigger.

If a binary trigger inverter is used only on the on output of the binary trigger, resistor R4 in the binary trigger (Figure 36) is changed from 7.5K to 20K. This resistor change adds positive loading to the off output to keep the trigger balanced.

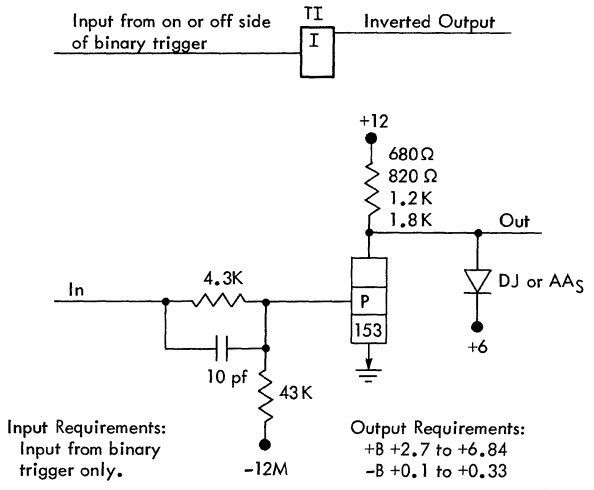


Figure 37. Binary Trigger Inverter

Control Trigger

The control trigger is a four-transistor circuit, operated only by negative AC shift inputs (Figure 38). For operation below 1 mc, clamped inverters (including level setters) may drive the input; for operation over 1 mc (up to 3 mc), a pulse generator, and possibly a cell driver, must be used. These two circuits are described in the "Shift Cell Circuits" section.

As with the binary trigger, the set and reset inputs to the control trigger can be driven from separate sources, or these inputs (1 and 5) can be tied common and driven from a single source for binary operation.

Transistors T1 and T2 make up the multivibrator portion of the circuit. The common emitter circuit used in the binary trigger is eliminated by introducing a negative bias through resistors R15 and R16. The collectors of T1 and T2 are returned to +12v and clamped to +6v; this makes it possible to drive indicator driver circuits directly from the multivibrator outputs.

Transistors T3 and T4 are trigger inverters for the off and on sides of the multivibrator; these circuits take the place of the external trigger inverters used with the binary trigger. Because trigger inverters are included in the circuit, the control trigger can drive loads directly.

Assume the trigger is off (Figure 38); transistor T1 is conducting and its collector is between +0.10v and +0.33v. This −B level is supplied through R5 to the T3 base and through R8 to the T2 base. Because of the voltage divider to −12M, consisting of R5 and R17, T3 is held cut off. Because of the voltage divider to −12M, consisting of R8 and R16, T2 is held cut off. The off output (6) from the T3 collector is +B.

Because transistor T2 is cut off, its collector attempts to go to +12v, but is clamped to near +6v by diode D2. The positive T2 collector voltage is supplied through R7 to keep T1 in full conduction and through R6 to keep T4 in full conduction. The on output (3) from the T4 collector is −B.

Assume that a negative shift arrives at the set input (1) or at both set and reset inputs (1 and 5). In this condition (trigger off), diode D4 is reverse biased so that if inputs 1 and 5 are common, a negative shift will reach only the T1 base. The negative shift is coupled through C4 and D3 to the T1 base, cutting off T1. As T1 cuts off, its collector goes positive turning on T2 and T3. The T2 collector drops to −B holding T1 and T4 cut off. The trigger is now on; the on output (3) is +B and the on DI output (2) is +B.

Capacitors C1, C2, C3, and C4 speed the switching time of the circuit by shorting the transistor base resistors during transitions.

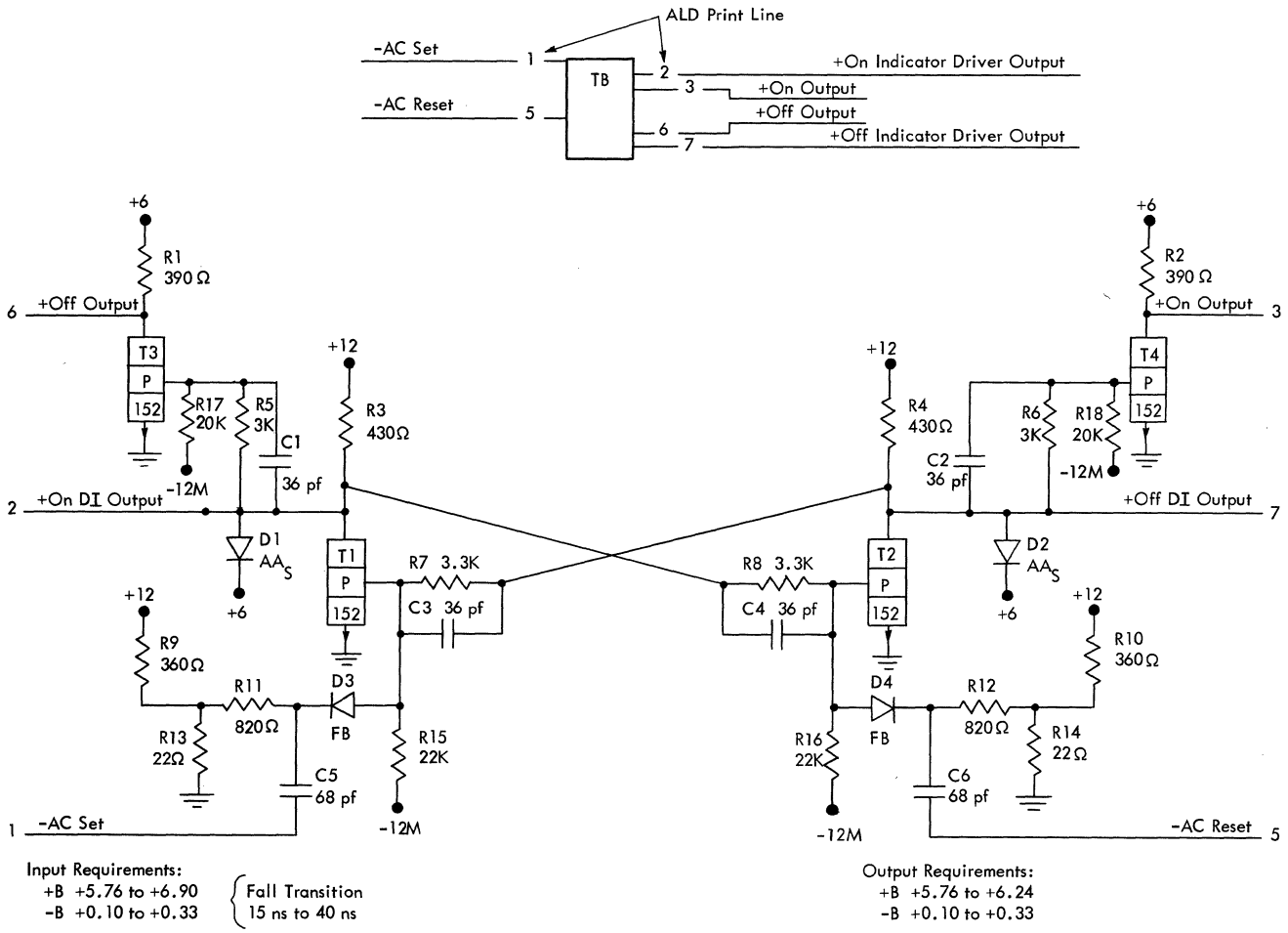


Figure 38. Control Trigger

AC Trigger

The AC trigger is a six-transistor circuit with AC set and reset inputs and collector pullover set and reset inputs (Figure 39). There are two major differences between the AC trigger and the control trigger:

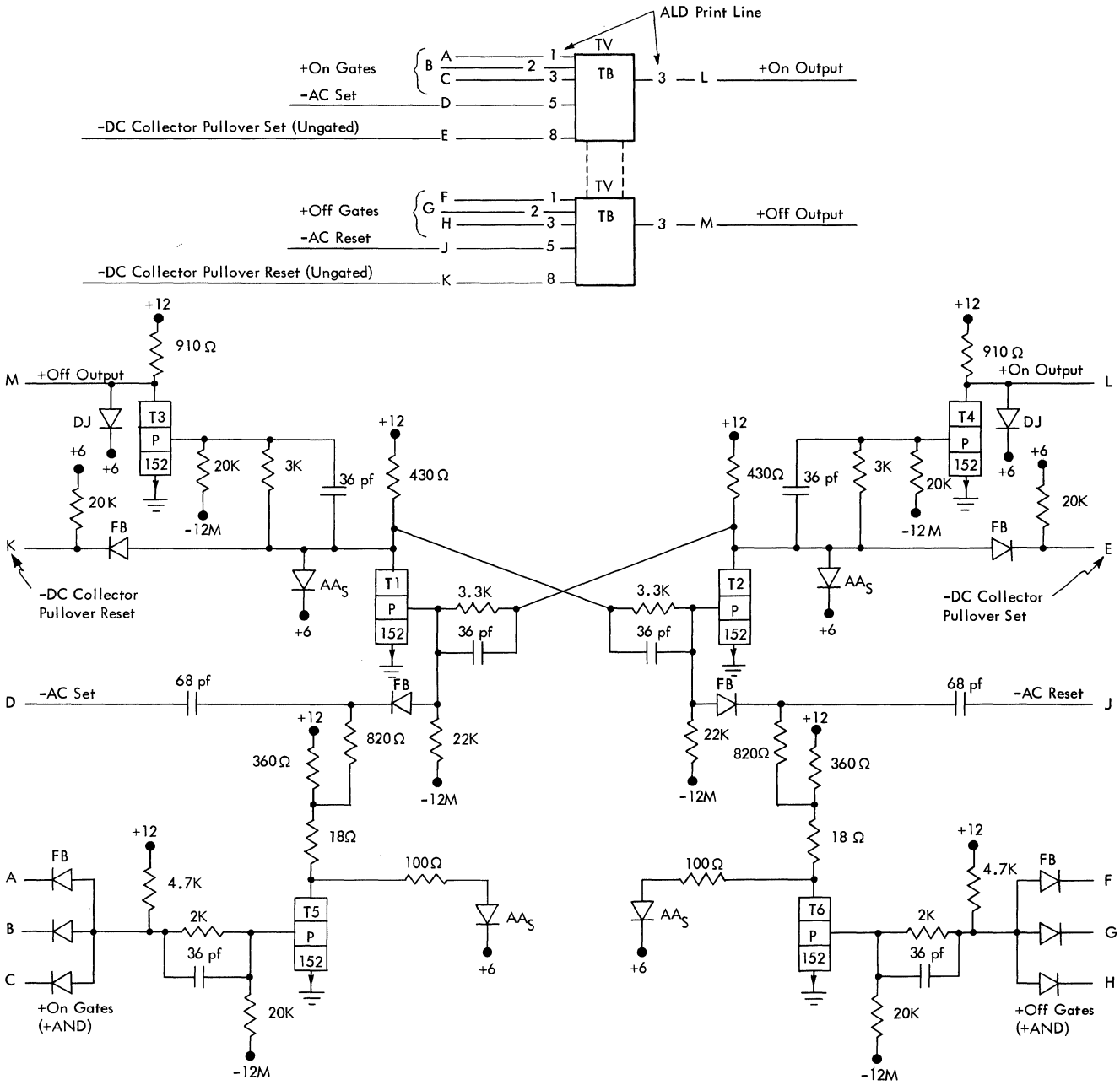
1. AC trigger has collector pullover inputs.
2. AC trigger has AC inputs gated.

Only these differences are discussed in detail; refer to "Control Trigger" for a complete explanation of the trigger.

The portion of the AC trigger consisting of T1, T2, T3, and T4 is essentially the control trigger. The collector pullover inputs (K and E) on the AC trigger are the major differences. These pullover inputs operate the same as the binary trigger pullover inputs. For example, assume that the trigger is off (Figure 39). Transistor T1 is conducting and the −B level at its collector is holding T3 and T2 cut off. The +B level at the T2 collector is holding T1 and T4 in full conduction. The on output (L) is at −B; the off output (M) is at +B. A collector pullover set input consists of an inverter transistor collector DOT'ed to input E. If this pullover transistor is turned on, conduction through the 20K resistor will drop input E to −B. This minus level is coupled through the diode to the T2 collector. The minus voltage at the T2 collector turns off transistors T1 and T4.

When transistor T1 turns off, its collector goes positive turning on T2. The trigger is now on, and will remain in this state even though the pullover transistor is turned off.

The T5 circuit is a +AND inverter used to gate the AC set (D) input. The T6 circuit is a +AND inverter used to gate the AC reset (J) input. Because these



Input Requirements:
AC Set and Reset
+B +5.76 to +6.90
-B +0.10 to +0.33
Fall Transition 15 ns to 40 ns

On and Off Gates
+B +5.60 to +6.84
-B +0.10 to +0.33
Gates must be active at least 200 ns before AC shift

DC Collector Pullover Set and Reset
Directly Connected to Unloaded and Unclamped Transistor Collector

Output Requirements:
+B +5.76 to +6.84
-B +0.10 to +0.33

Figure 39. AC Trigger

circuits are identical, only the T5 circuit is described in detail.

Assume that one or more of the on gates (A, B, and C) is at −B. The common diode anodes are held at −B and the voltage divider to −12M is holding T5 cut off. The T5 collector attempts to go to +12v; however, the clamp diode to +6v and the voltage divider in the T5 collector circuit hold the T5 collector at about +8v. This voltage is applied through the 820-ohm resistor to reverse bias the T1 input diode. (The T1 base is about +0.44v if the trigger is off). With this diode reverse biased, a negative shift at the set input (D) cannot turn off T1. The trigger will remain off until all on gates go to +B and a minus shift is applied to the set input.

Assume that all on gate inputs (A, B, and C) are at +B. The common anodes of the gate diodes go positive, turning on T5. The T5 collector goes to near ground, removing the reverse bias from the set input diode. When a minus shift arrives at the set input (D), it will cut off T1, thereby turning the trigger on.

The off gate circuit (T6) operates exactly like the on gate circuit to control the AC reset (J) input.

The time relation between an AC set or reset input and its gate inputs is very important. Because the on and off gate circuits are +AND inverters, these circuits have a delay of about 200 ns. This is a long delay in comparison to the length of time that an AC input is effective (approximately 50 ns). Therefore, if an AC shift is applied at the same time that its gate inputs are activated, the trigger will not change state; a gate input must have been active at least 200 ns before the shift input arrived. Because of the gate delay, a shift input will be effective even if its active gate is removed slightly prior (up to about 100 ns) to the arrival of the shift.

This delayed action gating is an extremely useful characteristic of the AC trigger. The triggers can be used to gate each other in applications such as shift registers and clock rings. In these applications, the AC set and reset inputs of each trigger are tied common, and the shift input is applied to all triggers simultaneously. Each trigger changes in accordance with the gating that it received prior to the shift. The delayed action of the gating prevents the triggers from changing more than one time during one shift pulse.

Negative Latch

The negative latch consists of an OR-AND basic inverter cross-coupled with a low power inverter, or an OR-AND level setter cross-coupled with a low power inverter (Figure 40). A −B level applied to one of the three set inputs turns the latch on; a +B level applied to one of the three reset inputs turns the latch off.

Assume the latch is off. Transistor T1 is conducting and the on output is −B. This −B level is applied to the input of the low power inverter, holding T2 cut off. The off output is +B. The off output is applied to the reset +OR to hold the latch off, even though all reset inputs have returned to −B.

When one of the set inputs goes to −B, the common anodes of the −OR are clamped at this level. The resistor divider to −12M cuts off T1, allowing its collector to rise to +B. This +B level at the on output is applied to the low power inverter, forcing T2 to saturate. The T2 collector drops to −B. If the input that turned the latch on returns to +B, the latch remains on because the output of the reset +OR is minus; this minus level is one input to the set −OR, and the latch is held in the on state.

To reset the latch, a +B must be applied to one of the reset inputs and all of the set inputs must have returned to +B. These conditions allow the T1 base to go positive, turning on T1. The latch then returns to the off condition.

If a set and a reset input are simultaneously active, the latch is on with output 3 at +B and output 6 at −B. The final condition of the latch is determined by the last remaining active input.

Shift Cell Circuits

Three circuits comprise the shift cell group:

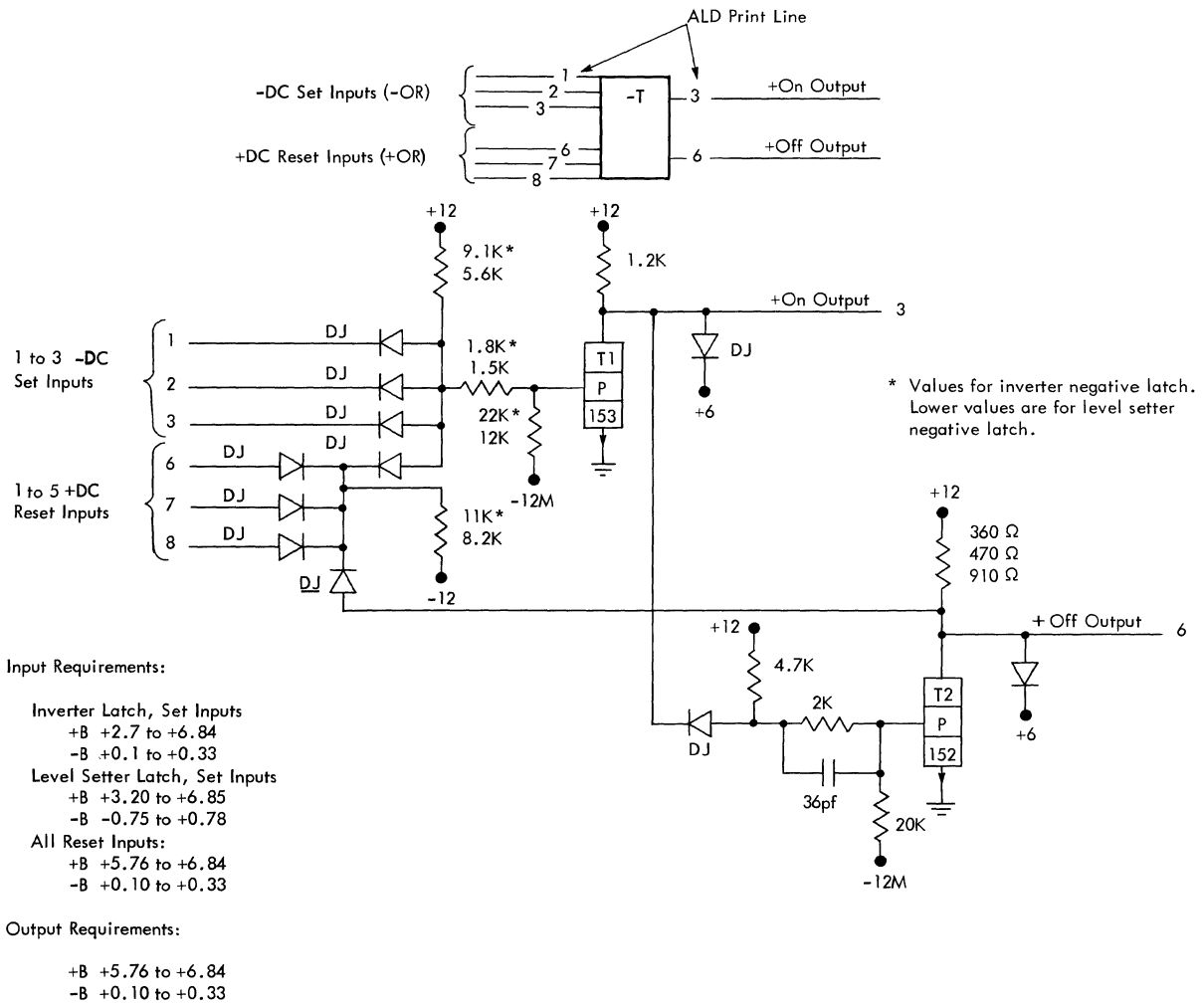
1. Shift Cell
2. Cell Driver
3. Pulse Generator

The function of these circuits is as follows (Figure 41). The pulse generator uses the −B to +B shift of any standard circuit to generate a very narrow positive spike that has an extremely sharp leading edge. The cell driver amplifies and inverts this pulse so that up to four shift cells can be driven in parallel. The shift cell is similar to a trigger, and like a trigger, its purpose is to store one of two conditions. When given a negative AC pulse, the shift cell turns on or off as follows:

1. +B gate and shift pulse turn cell off
2. −B gate and shift pulse turn cell on

A clock timing ring is an example of how shift cell circuits are used (Figure 42). Note that the shift cells gate each other through inverters. The inverters are used because shift cells cannot directly feed on each other; the gate input must be driven from one to four unloaded transistor collectors.

The shift cell clock ring produces repetitive clocking pulses (Figure 42). Assume that all shift cells are off; the +B off output of clock 3 is inverted to give a −B gate input to clock 1. When the first shift



Input Requirements:

Inverter Latch, Set Inputs
+B +2.7 to +6.84
-B +0.1 to +0.33
Level Setter Latch, Set Inputs
+B +3.20 to +6.85
-B -0.75 to +0.78
All Reset Inputs:
+B +5.76 to +6.84
-B +0.10 to +0.33

Output Requirements:

+B +5.76 to +6.84
-B +0.10 to +0.33

Figure 40. Negative Latch

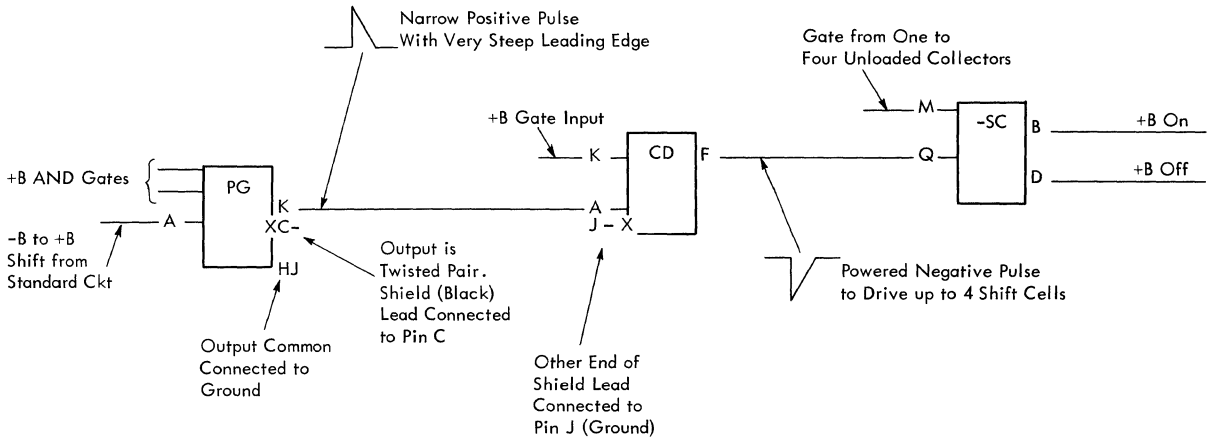


Figure 41. Shift Cell Circuits

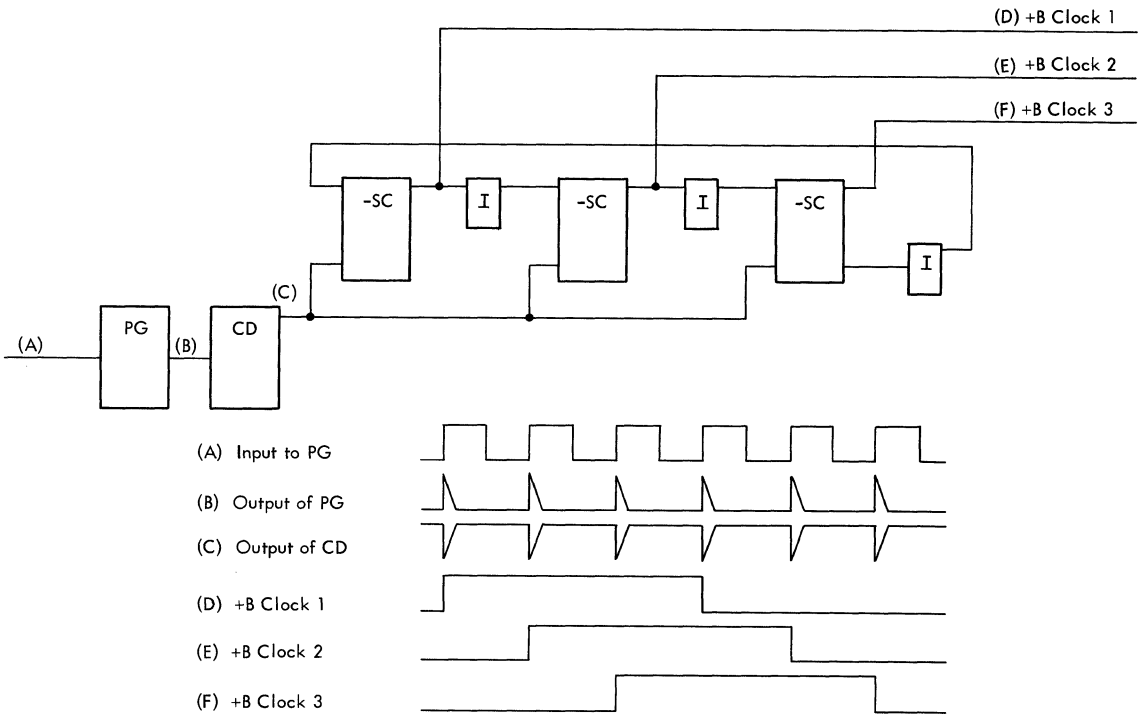


Figure 42. Shift Cell Clock Ring

input (point C) arrives, shift cell 1 turns on; shift cells 2 and 3 remain off because their gate inputs were +B prior to the arrival of the shift input. On the second shift input, shift cell 2 turns on; on the third, shift cell 3 turns on. With 3 on, shift cell 1 is conditioned to turn off when the fourth shift input arrives.

The clock ring makes one, and only one, change at each shift pulse because of the characteristics of the shift cell circuits. The gate input to a shift cell requires about 200 ns to become effective; this is a long time in comparison to the length of time that the shift is effective (approximately 50 ns). Therefore, even though the gate to one shift cell in the clock ring is always changed during the shift pulse, this gate change is not effective until the following shift pulse.

Shift Cell

The shift cell is a bi-stable device very similar to a trigger. It has on and off outputs, and it stores one of two conditions. Instead of separate AC set and reset inputs, however, the single shift input is connected to both sides of the shift cell the same as a trigger is connected for binary operation (Figure 43). The single gate input determines which side of the shift cell is affected by the shift input. If the gate is −B, the shift input turns the cell on; if the gate is +B, the shift input turns the cell off.

Transistors T1 and T2 form a bi-stable multivibrator identical to the ones used in the control trigger and the AC trigger. Transistors T3 and T4 are trigger inverters for the off and on sides of the cell respectively. These circuits are also identical to the trigger inverters used in the control and AC triggers. As with the control trigger, indicator drivers can be driven directly from the multivibrator transistor collectors.

The gating arrangement distinguishes the shift cell from the AC and control triggers. Assume that the cell is off and that the gate input is −B (Figure 43). Transistors T1 and T4 are conducting; off outputs 6 and 7 are +B, and on outputs 2 and 3 are −B.

The −B gate is applied to the gate inverter, T5, through the 3K input resistor. The voltage divider to −12M holds T5 cut off; the T5 collector is approximately +8v because of the voltage divider and the clamp diode to +6v. This positive voltage from the T5 collector holds the input diode to T2 reverse biased; a negative shift input cannot reach the T2 base.

The input diode to T1 is controlled directly by the gate input. With the gate at −B and with T1 conducting, this diode has very nearly the same voltage applied to both sides (about +0.4v). The negative shift at input 5 is readily coupled through this diode to the T1 base, cutting off T1. When T1 cuts off, the cell switches on because the positive T1 collector turns

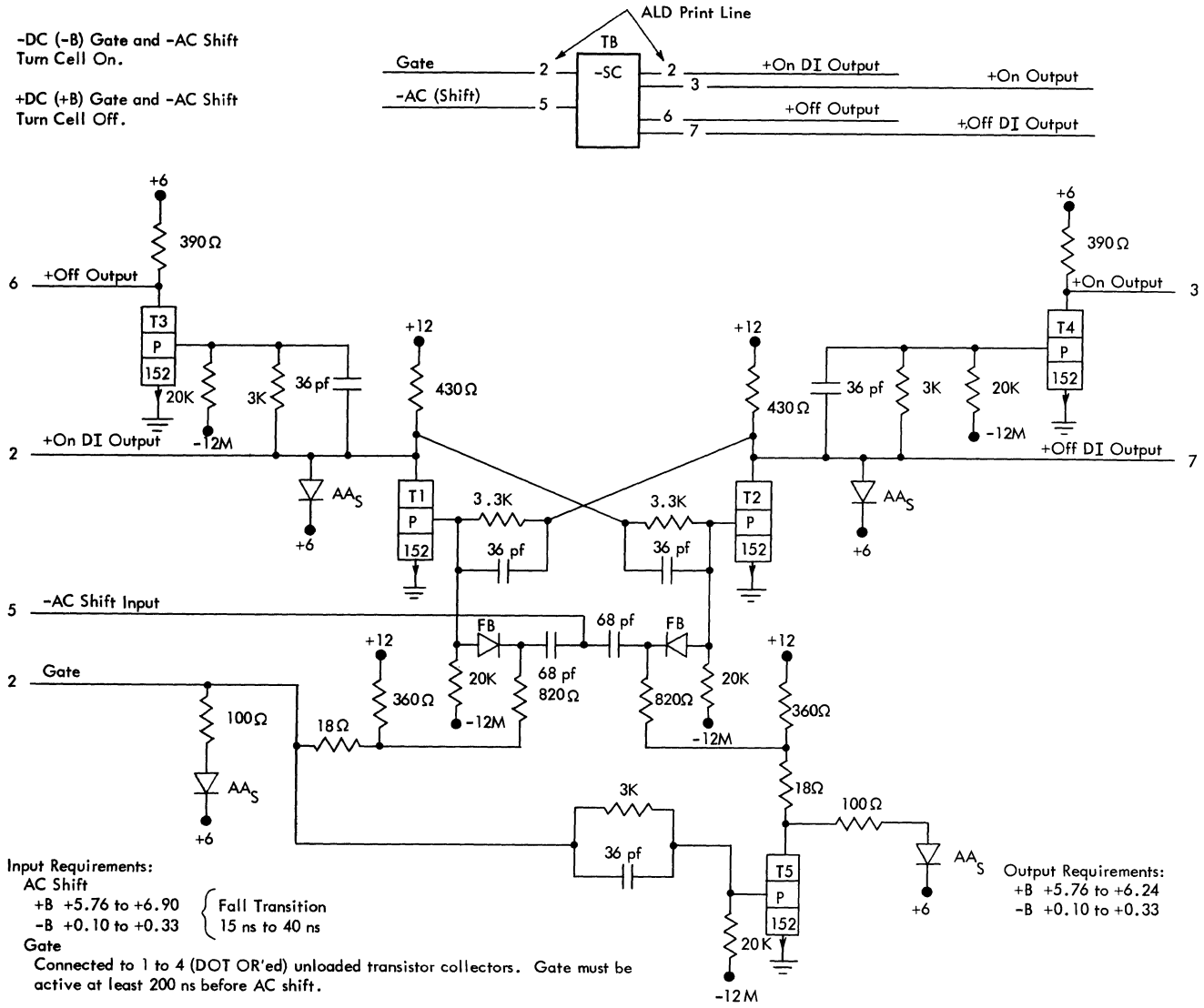


Figure 43. Shift Cell

on T2 and T3; the negative T2 collector holds T1 and T4 cut off.

Assume that another shift input occurs with the gate still at −B. The positive output from the T5 collector again keeps this shift from being coupled to T2 base. The shift is gated to the T1 base, but because T1 is already off, the cell does not switch.

When the gate input is changed to +B, the T1 input diode is reverse biased. The gate inverter, T5, saturates and its output drops to near 0v. The next shift input cuts off T2, returning the cell to its off state.

If more than one transistor collector is connected to the gate input, the gate drops to −B when any of the transistors conduct. This arrangement allows a cell to be turned on from more than one source.

The gate input to a shift cell requires about 200 ns to become effective. This is a long time in comparison to the length of time that the shift input is effective (about 50 ns). Therefore, if the gate changes at the same time that a shift input is applied, the shift cell will change according to the previous state of the gate. Because of this gate delay, a shift cell will actually follow the old state of a gate that was changed up to about 100 ns prior to the arrival of the shift pulse.

Cell Driver

Most shift cell applications require that a number of cells simultaneously receive a negative shift (for example, the shift cell clock ring, Figure 42). The cell

driver provides this shift to as many as four shift cells. The cell driver is made up of a diode AND, followed by an emitter follower, followed by an inverter (Figure 44). The diode AND allows the cell driver to be disabled by a −B input. If either the shift or the gate input is at −B, a change on the remaining input will not be coupled through the 68 pf capacitor to the T1 base.

Statically, T1 and T2 are off. The forward drop of the CD diode holds the T2 base slightly negative; the forward drop of the FB diode holds the T1 base slightly more negative than the T1 emitter. The T2 collector attempts to go to +12v, but is clamped to +6v.

When the gate input is +B and a plus shift is received, the output of the diode AND goes positive. This plus shift is coupled through the 68 pf capacitor to the T1 base. Transistor T1 turns on and its emitter goes positive, turning on T2. The T2 collector drops quickly to near ground. The two transistors conduct only momentarily; either the plus shift returns to −B, or if not, the 68 pf coupling capacitor to T1 charges so that the T1 base is no longer positive. In either case, T1 and T2 return to their static cutoff condition and the output returns to +B.

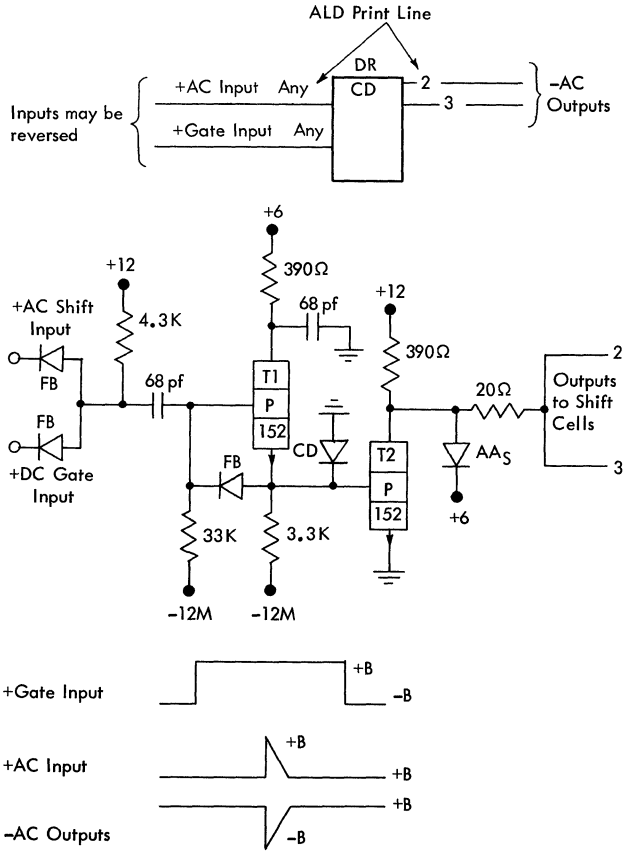


Figure 44. Cell Driver

Pulse Generator

The pulse generator gives a narrow, sharp-rising pulse with the coincidence of up to three +B inputs (Figure 45). The positive pulse output is normally used to drive cell drivers that, in turn, drive shift cells. One special application of the pulse generator connects the output to obtain a negative pulse. This negative pulse is obtained by connecting one of the two normal outputs (4 or 6) to a plus voltage; one of the normal ground outputs (5, 7, or 8) is then used to drive the AC trigger.

Assume that one or more of the circuit inputs is −B (Figure 45). Transistor T1 (an emitter follower) is held cut off by the FB diode between its emitter and its base. The T1 emitter is held at about +0.5v because of the forward drop of the FB diode between the T1 emitter and ground.

Transistors T2 and T3 are fed in parallel from the T1 emitter; the collectors of these transistors are tied common to feed parallel primaries of the output transformer. Statically, T2 and T3 are held cut off by the voltage dividers to −12M at their bases.

When the last −B input goes to +B, a positive shift is coupled through the 68 pf capacitor to the T1 base. Transistor T1 turns on bringing its emitter positive. The positive shift at the T1 emitter is coupled through 100 pf capacitors to both T2 and T3 bases. Transistors T2 and T3 conduct through the parallel primaries of the output transformer; the expanding magnetic field cuts the secondary turns producing the circuit output. The 470 pf capacitors were charged to +12v before T2 and T3 were turned on. These capacitors momentarily provide a 12v source for the transistors, forcing them to conduct very hard through the transformer primaries. The conduction path for each transistor is from the capacitor plate at the transistor emitter through the transistor, through the transformer primary, and back to the other capacitor plate. Because the transistors momentarily force a large current through the transformer, the output pulse rises very quickly.

Two actions influence the turn off of T2 and T3. First, as current flows through the transformer primaries, the 470 pf capacitors discharge. As the capacitors discharge, an increasing amount of the current flows through the four 100-ohm resistors. Current through the emitter resistors brings the emitters positive, reducing conduction in the transistors. Second,

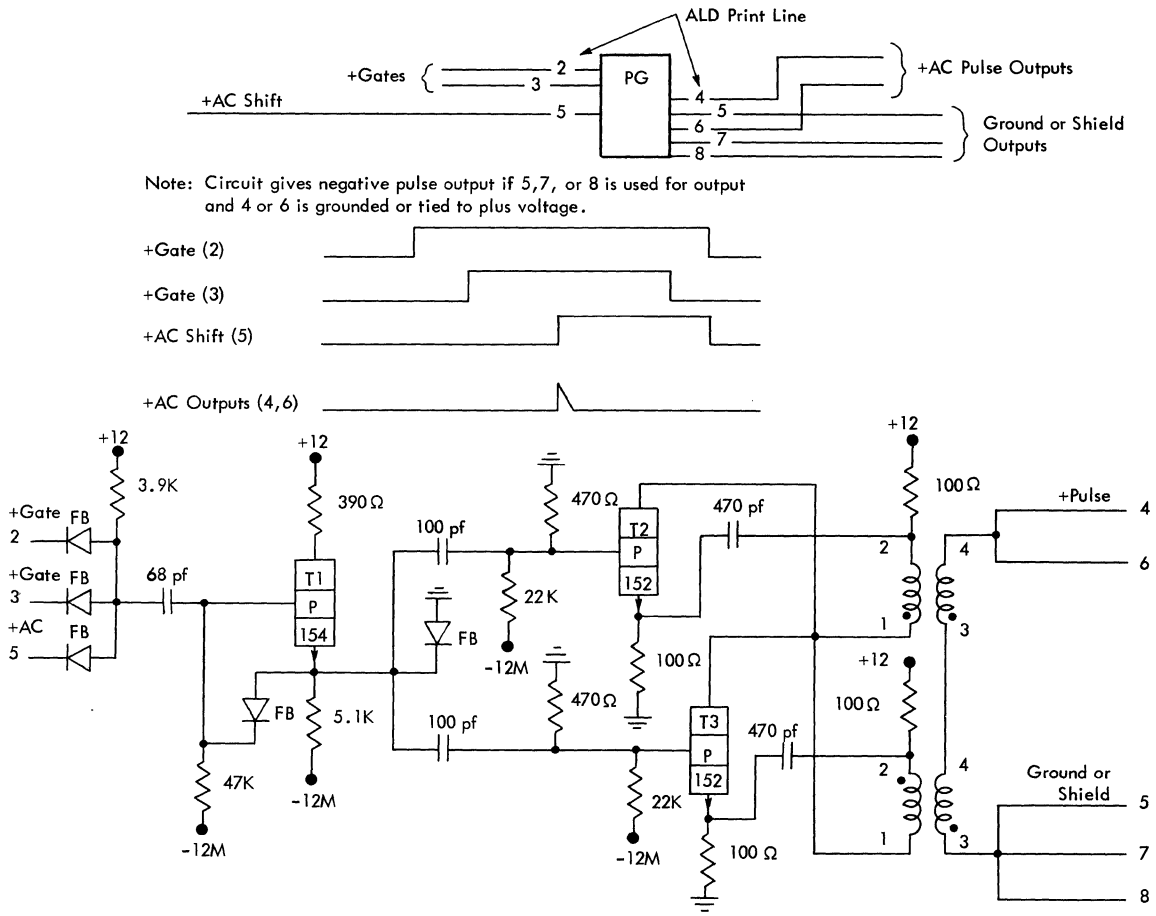


Figure 45. Pulse Generator

the RC network at the bases of the two transistors begins lowering the base voltage. This action also reduces the conduction of the transistors. The result of these two actions is to return T2 and T3 to cut off much slower than they were forced into conduction. Because the magnetic field of the transformer does not collapse suddenly, the output is comparatively free of overshoot.

Single-Shots

Single-shots generate a timed output that is partially or completely independent of the input pulse width. Generally, a single-shot is used to perform one of the following logic functions:

1. Lengthen or shorten a pulse. The single-shot takes a shift input and converts it to a timed pulse output.
2. Delay an event to allow time for a mechanical or some other electrical event to complete.
3. Detect the presence or absence of periodic pulses.

Most single-shots are activated, or fired, by an AC shift input. When the shift occurs, the output goes active for the time duration of the single-shot. Because these single-shots are activated by a shift input, the output times out even if the input returns to its inactive condition. A few single-shots are activated by a DC level. The DC input single-shots normally require an active input that is at least as long as the time duration of the single-shot. Often, these circuits have a diode OR input to allow the single-shot output to be latched back to one input. When this is done, a narrow input can activate one of these single-shots; once activated, the output holds the input active until the single-shot times out.

Some single-shots have a holdover input. An active holdover input immediately causes an active output that is held (does not begin timing out) until the holdover input goes inactive. When the holdover input goes inactive, the output remains active for the time duration of the single-shot. If the active holdover input is frequent enough to prevent the single-shot

from timing out, the output remains active, indicating the presence of periodic inputs.

Variable Single-Shot

The variable single-shot is activated by a +B DC level; however, this circuit has an internal latchback so that the input can be as short as 75 ns (Figure 46). The active output is a −B level for the time duration of the circuit.

The time duration is controlled in two ways: the selection of a timing capacitor (determines range of timing) and adjustment of a potentiometer in the circuit (exact timing within range of selected capacitor). Most DDTL variable single-shots have several internal timing capacitors that may be selected by back panel wiring. Any combination of these capacitors can be connected in parallel to give various timing ranges. In addition, most circuits have a capacitor extender input that allows external timing capacitors (capacitors on another card) to be backpanel wired into the circuit.

Two DDTL variable single-shots are represented by Figure 46. One (H21AF) has a single timing capacitor that gives a timing range of 900 μs to 1190 μs. There are no provisions to change the timing range. The other circuit represented (H21AE) has one capacitor permanently wired (430 pf) so that the minimum timing range of the circuit is about 2.5 μs to 3.8 μs. Three other capacitors can be added individually or in combinations to extend the timing range in steps to a maximum of about 2 seconds.

The operation of the variable single-shot follows (Figure 46). Assume a static condition where the input is −B and the circuit is not timing out; the output is +B. Transistors T1 and T3 are cut off; transistor T2 is conducting. The −B input and the resistor divider to −12M are holding T1 off. The +6v source through the 10K potentiometer, 3.16K resistor, and the CE diode gives T2 positive bias to keep it in saturation. The T2 collector is near 0v; this potential and the resistor divider to −12M holds T3 cut off. The T3 collector (circuit output) is at +B.

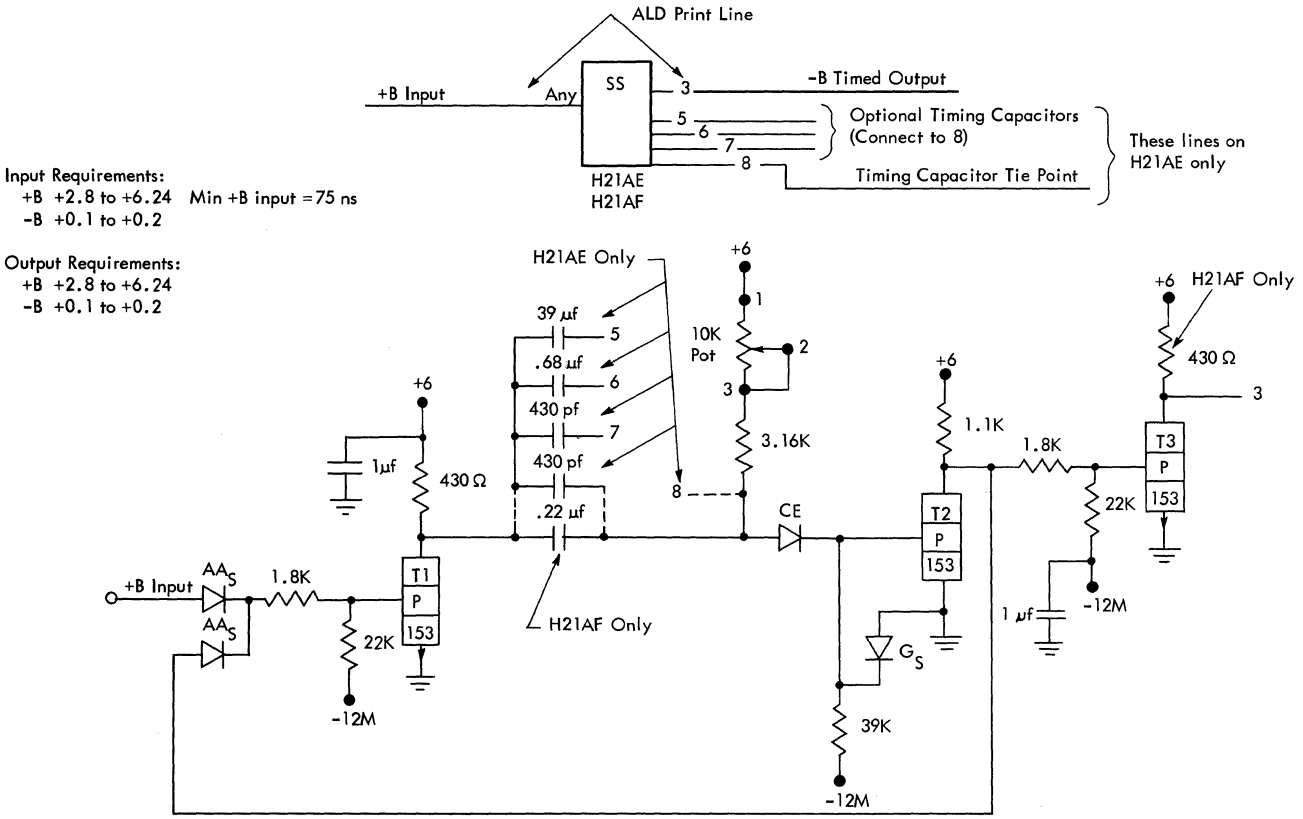


Figure 46. Variable Single-Shot

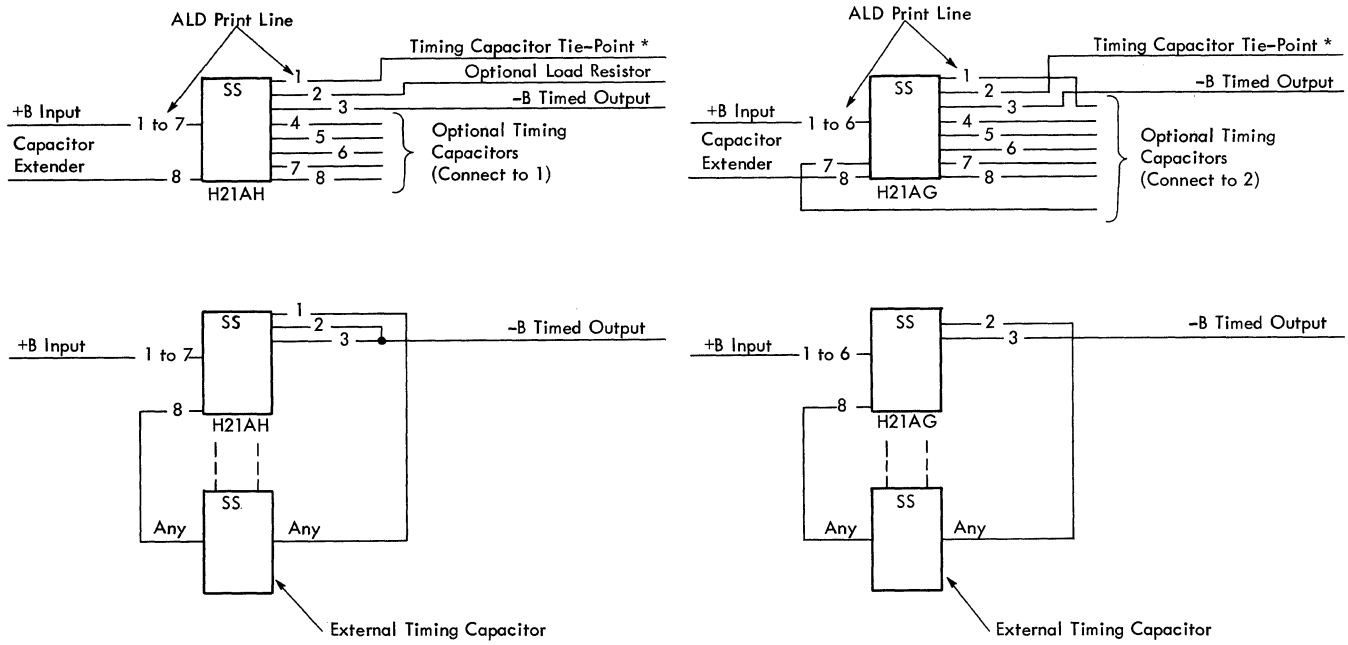
Assume that the input goes to +B. Because the input diodes constitute a +OR, the T1 base is driven positive causing T1 to saturate. The negative shift from +6v to near 0v at the T1 collector is coupled through the timing capacitor(s) to reverse bias the CE diode. The −12M source pulls the T2 base down to about −1v where it is clamped by the base-to-emitter diode. This negative bias cuts off T2, allowing its collector to go positive. The positive T2 collector turns on T3 causing a −B output. The positive T2 collector also latches back to the input +OR to keep T1 conducting even if the circuit input returns to −B.

The T1 side of the timing capacitor(s) was at +6v in the static condition; the T2 side was at about +1v because of the voltage drop of the CE diode and the emitter-to-base drop of T2. The capacitor(s) must now discharge by transferring electrons from the T2 side to the T1 side. The discharge path is through the 3.16K resistor and the 10K potentiometer, through the +6v power supply to ground, and through T1 to the other side. Discharge current flowing up through the 3.16K resistor and the potentiometer drops voltage to hold the anode of the CE diode negative. The RC time constant of the timing capacitor(s), the 3.16K resistor, and the resistance (setting) of the potentiometer determines the time duration of the output.

As the timing capacitor(s) charge, the current through the 3.16K resistor and the potentiometer decreases, allowing the voltage at the anode of the CE diode to rise. When positive enough, this voltage forward biases the CE diode and overcomes the negative T2 bias. Transistor T2 begins conducting and its collector drops to near 0v. Transistor T3 is cut off and the output returns to +B. The feedback path from the T2 collector goes negative and T1 turns off if the circuit input has returned to −B.

The static charge on the timing capacitor(s) is restored when the circuit has timed out and the input has returned to −B. At this time, T1 cuts off and the T1 side of the capacitor(s) charges to +6v through the 430-ohm T1 collector resistor. The T2 side of the capacitor(s) is clamped to about +1v by the T2 emitter-to-base voltage drop and the voltage drop of the CE diode.

Two common variations of the variable single-shots just described are shown in Figure 47. These circuits differ from those shown in Figure 46 by the addition of a capacitor extender and by a different line place-



* No internal capacitor is wired; the capacitor tie-point must be wired to a capacitor

Figure 47. Variable Single-Shot Variations

ment of circuit inputs and outputs. When an external timing capacitor is used with these circuits, the ALD representation shows two single-shot blocks, usually connected by dashed lines (Figure 47).

Holdover Single-Shot

The DDTL holdover single-shot operates as either a holdover single-shot or as a normal shift input single-shot (Figure 48). A plus shift at input 6 is coupled through a capacitor into the circuit and causes a −B timed output. A +B holdover input at 3 holds the output at −B; when the holdover input returns to −B, the output remains at −B for the time duration of the single-shot. If either these two inputs is not used, it can be left floating without interfering with the operation of the circuit by the remaining input.

The timing range of the holdover single-shot is selected by backpanel wiring one or more of the internal timing capacitors to the capacitor tie point, by wiring one or more external capacitors between the

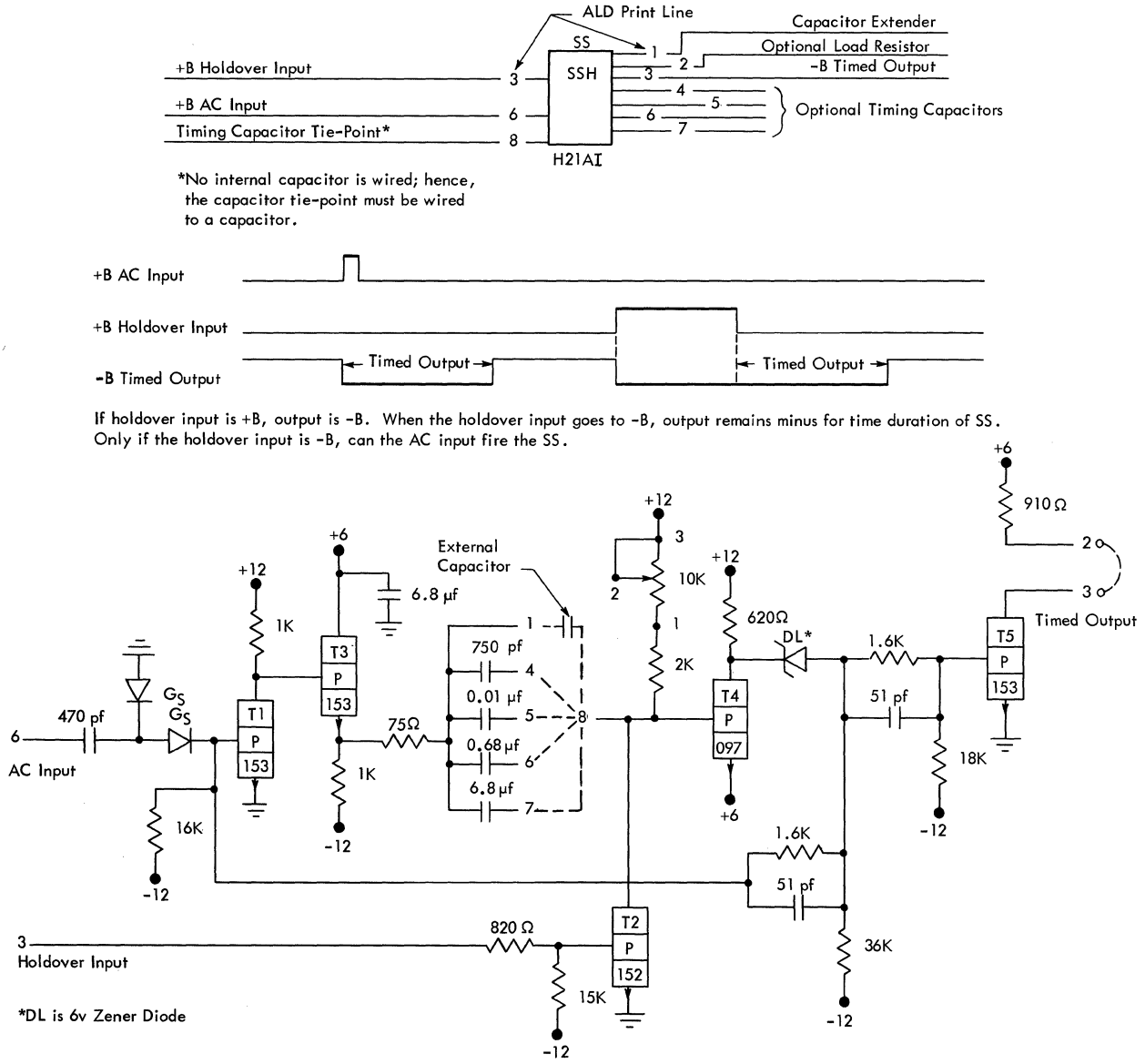


Figure 48. Holdover Single-Shot

capacitor extender and the capacitor tie point, or by wiring a combination of internal and external capacitors. A specific timing within the range selected is obtained by adjusting a potentiometer in the timing capacitor discharge path.

Assume that the holdover input is not being used, or that this input is −B (Figure 48). In either case, T2 is held cut off by the resistor network to −12v. Before a +B shift is applied to 6, transistors T1 and T5 are also cut off because of negative bias supplied through base resistors from −12v. Transistor T3 is saturated because of the positive T1 collector. Because T3 is saturated, the T3 emitter is near +6v, and therefore, the T3 side of the timing capacitor(s) is near +6v. Transistor T4 is saturated because of positive bias through the 10K potentiometer and the 2K resistor. The T4 base is at about +6.4v because of the emitter-to-base drop of T4. The timing capacitor(s) has practically no charge because approximately the same voltage is applied to both plates. The T4 collector is slightly more positive than +6v because T4 is saturated. The DL Zener diode is conducting in the reverse direction; however, a characteristic of this diode is that it drops 6v when conducting in its Zener region. The anode of the DL diode is, therefore, only slightly above 0v.

Assume that a −B to +B shift is applied to 6. Transistor T1 turns on and saturates rapidly because, while T1 was off, the clamp diode to ground allowed the T1 base to go only negative enough to hold T1 cut off. The minus shift at the T1 collector reduces the conduction of T3 (an emitter follower) so that the T3 emitter goes from +6v to near 0v. This negative shift is coupled through the timing capacitor(s) to cut off T4. The T4 collector rises to near +12v, bringing the anode of the DL diode to about +6v. Transistor T5 turns on, bringing the output to −B. The +6v at the DL anode is fed back (through 1.6K and 51 pf) to the T1 base to hold T1 in conduction until the single-shot times out.

Transistor T4 is held off by curent flow from the T4 side of the timing capacitor(s) to the T3 side (capacitor(s) charging). The charge path is up through the 2K resistor, the potentiometer, +12v power supply, the −12v power supply, and through the 1K and 75-ohm resistors to the other side of the capacitor(s). The capacitor charge current causes a voltage drop across the 2K resistor and the potentiometer, holding T4 off.

As the timing capacitor(s) charges, the current flow reduces until the T4 base becomes more positive than +6v. When this happens, T4 goes back into conduction, bringing the T4 collector to near +6v. Transistors T5 and T1 are cut off, the output returns to +B, and the conduction of T3 increases to rapidly discharge the timing capacitor(s).

If the holdover input (3) is brought to +B, T2 saturates, dropping the T4 base to near 0v. Transistor T4 cuts off, turning on T5 and T1. The output is −B and the circuit cannot time out because the T4 base is held at about 0v by the conduction of T2. When T1 turns on, the conduction of T3 is reduced so that the timing capacitor(s) is quickly returned to near neutral charge with about 0v on both plates.

When the holdover input returns to −B, T2 cuts off, but its collector does not immediately go positive. The timing capacitor(s) must charge through the 2K resistor and the potentiometer. The T2 collector and the T4 base slowly rise until they are slightly more positive than +6v, at which time T4 is again forward biased. When T4 conducts, the circuit returns to its static condition, bringing the output to +B.

Pulse Former Single-Shot

The pulse former single-shot is a simple circuit used for short time durations (Figure 49). Instead of an RC network, the timing component of the pulse former single-shot is a coil. The circuit uses the principle that a coil offers a high impedence to DC current flow until the magnetic field builds up.

The widest application of the pulse former single-shot circuit is for time durations in the nanosecond range; however, a pulse-forming network of several coils and capacitors is sometimes used to extend the range of the circuit to about 50 μs. Longer time durations are not practical because they would require large coils.

The pulse former single-shot, shown in Figure 49, has a three-way diode +OR input. Any +B input causes a timed +B output. The input level must be as long as, or longer than, the time duration of the circuit. This requirement is often met by latching-back the output to one of the inputs (Figure 49).

With all inputs at −B, the static condition of the circuit is: T7 cut off because of the voltage divider to −12M; T6 minimum conduction (emitter and base are at the same potential); T5 minimum conduction because of minus voltage applied through pulse-forming network; T4 saturated because of the positive T5 collector. With T4 saturated, the output is −B.

When a +B input is received, T7 saturates; the T7 collector goes to near 0v, forward biasing T6. The T6 collector immediately goes positive because the coil of the pulse-forming network is a high impedence load until its magnetic field builds up. The positive T6 collector turns on T5. The T5 collector drops from +6v to about −1v where it is clamped by the CD diode.

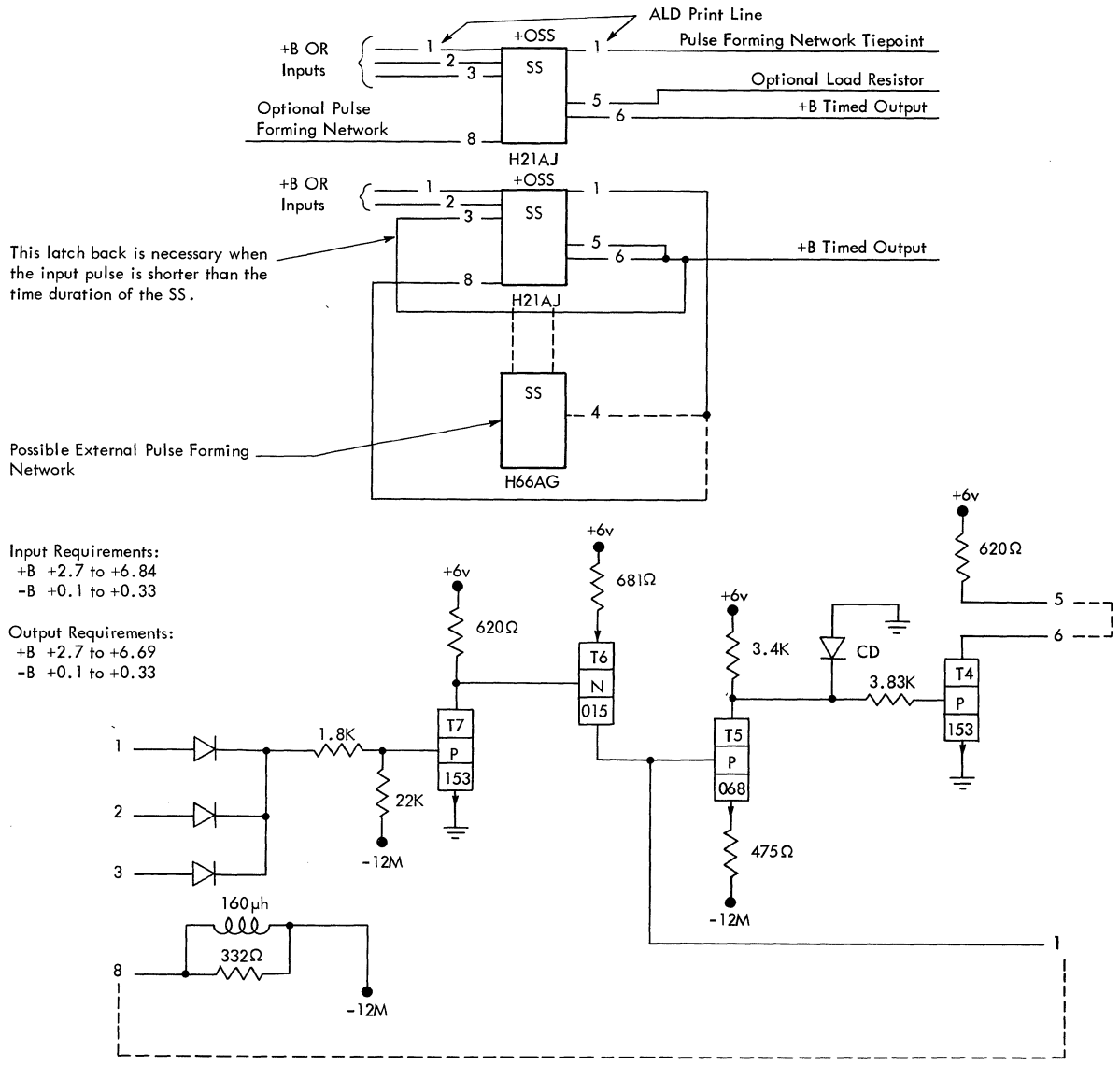


Figure 49. Pulse Former Single-Shot

This voltage is sufficient to cut off T4, allowing the output to rise to +B.

When the magnetic field of the pulse-forming network coil reaches maximum, the impedence of the pulse-forming network drops to the DC resistance of the coil. Because this resistance is very low, the T6 collector goes negative, reducing the conduction through T5. The T5 collector goes positive enough to turn on T4, bringing the output down to –B.

The circuit remains in this state until all inputs return to –B; then, T7 cuts off, restoring the circuit to its static condition.

The optional pulse-forming network in the circuit shown gives an output of approximately 600 ns. For other time durations, an external pulse-forming network is backpanel wired to 1. Other pulse former single-shots have up to six +OR inputs and do not have an optional pulse-forming network included in the circuit (Figure 50). The pulse-forming network tie-point for these circuits is 4 instead of 1.

Indicator and Relay Drivers

Indicator Drivers

DDTL indicator drivers convert a B level input to an output that lights a filament-type indicator lamp. All

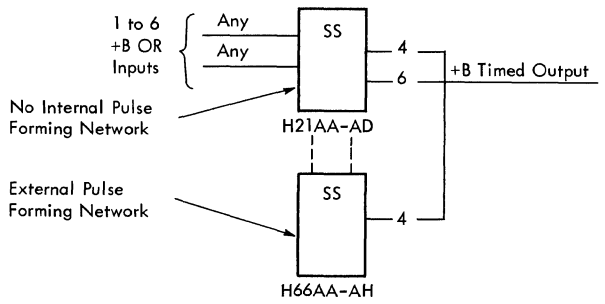


Figure 50. Pulse Former Single-Shot without Internal Network

of the drivers require a +B level input to turn on the associated lamp (Figure 51); a −B level input extinguishes the lamp.

The 15 and 40 ma input drivers operate as follows (upper left of Figure 51). With a −B input, the transistor is reverse biased off. A pre-energization current is supplied by the resistor from collector to ground. This current (about 3.5 ma in the 15 ma drivers) is insufficient to light the lamp, but it keeps the filament warm so that the lamp will light more quickly; also, the resistor to ground carries some of the current when the lamp is lighted so that less current is demanded from the transistor.

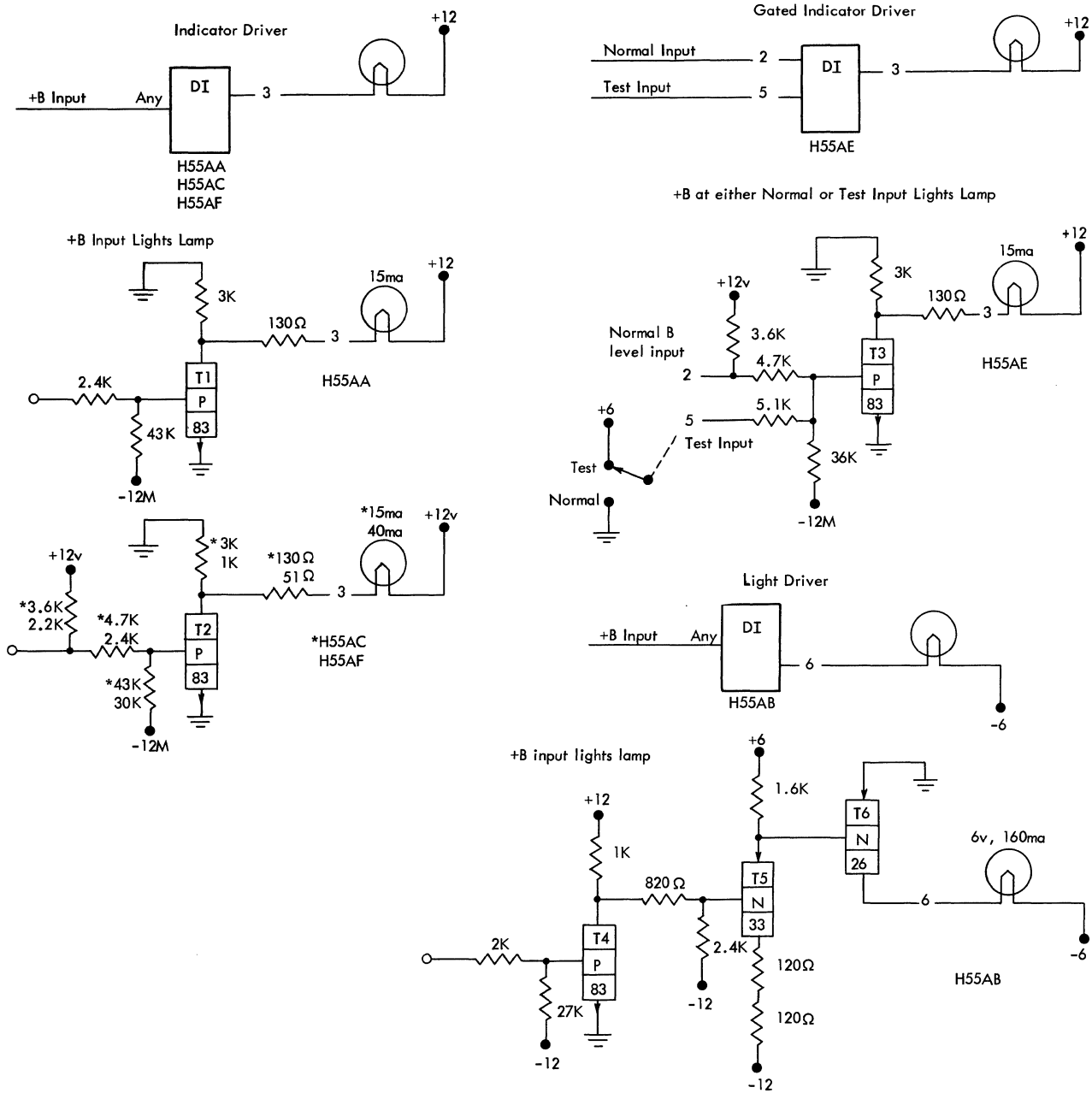


Figure 51. Indicator Driver

When the input shifts to +B, the transistor saturates and appears as a low resistance in parallel with the pre-energization resistor. The transistor collector drops to near 0v; nearly 12v is across the lamp. The lamp quickly lights to full brilliance.

The gated indicator driver (upper right, Figure 51) has a test input in addition to the normal input. The test input is under manual switch control so that the lamp and the driver are easily tested. A +B level at either the normal or the test input saturates the transistor, causing the lamp to light.

The light driver (lower, Figure 51) is used to light large lamps that illuminate printed translucent inserts. Unlike the smaller drivers, no pre-energization resistor is used in the circuit. With a −B input, transistor 4 is cut off and supplies a positive input to emitter follower T5. Very little current flows through T5 and its emitter is near +6v. Transistor T6 is cut off and only a small leakage current (less than 3 ma) flows through the lamp.

With a +B input, T4 saturates and supplies near 0v to the 820-ohm resistor; the divider to −12v puts a negative voltage on the T5 base. The T5 emitter follows the base negative to forward bias T6. The conduction of T6 turns on the lamp.

Relay Drivers

The three commonly used relay drivers (Figure 52) have differing current capabilities that range from 75 ma to 700 ma. Although these drivers are usually used to pick relays, they are sometimes used to drive other high current loads such as magnet coils and large indicator lamps.

The 700-ma driver (leftmost, Figure 52) requires a +B input to supply current to its load. With a −B input, T1 is cut off, emitter follower T2 conducts minimum, and T3 is cut off. Only a very small leakage current is supplied to the load. When the input shifts to +B, T1 saturates, T2 increases conduction, and T3 supplies high current to pick the relay.

The 125 to 300 ma relay driver requires a −B input to pick the load relay. The single transistor is an inverter that is held cut off by a +B input, and is saturated by a −B input.

The 75-ma driver is also an inverter stage that saturates with a −B input, thereby picking the relay. This circuit has a diode in parallel with the relay coil to shunt the large negative voltage generated by the coil when T8 cuts off. This shunting allows the relay to drop more quickly and prevents excessive voltage which might damage the transistor.

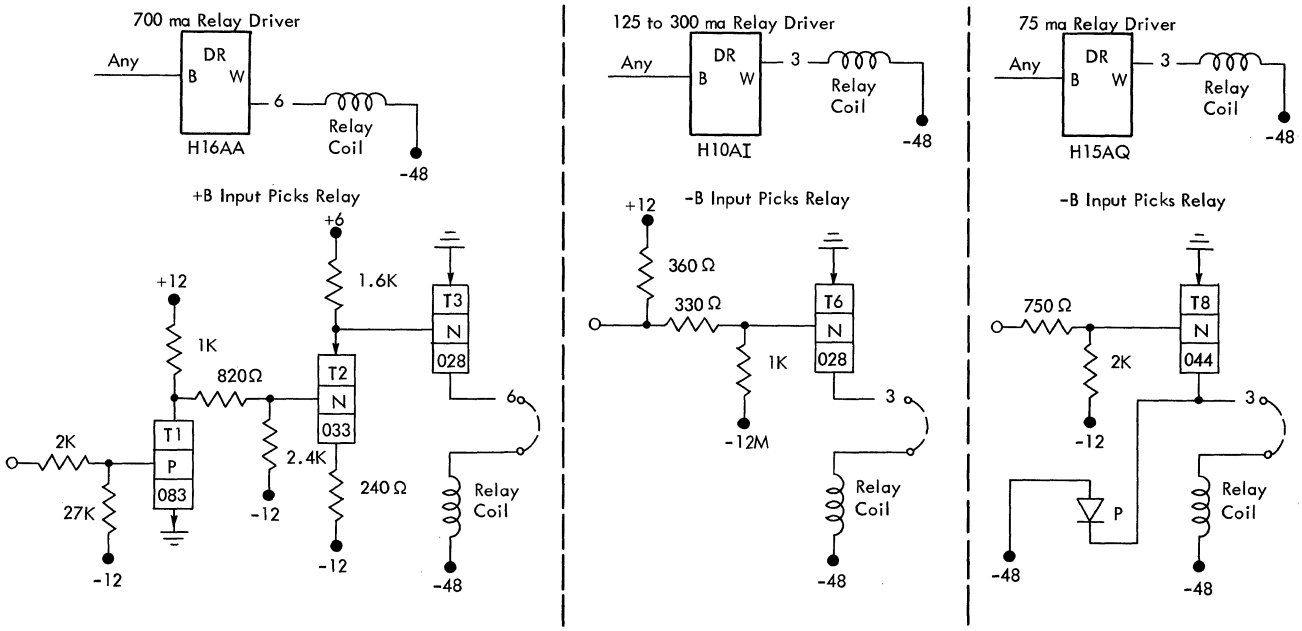


Figure 52. Relay Driver

Oscillators

Crystal Controlled Oscillators

There are many DDTL crystal-controlled oscillators. Normally, each circuit has only one application, because a unique frequency is generally required for a particular application within a machine. The oscillator circuits vary depending on the frequency for which they are designed; however, all of the circuits generate a B level squarewave output. The output frequency is set by the natural vibration frequency of a crystal; positive feedback is used to sustain crystal oscillation. Two examples of DDTL crystal-controlled oscillators are shown in Figures 53 and 54 and explained as follows.

The oscillator circuit shown in Figure 53 uses a 2 mc crystal to generate 0.5 μs alternate intervals of +B and −B. Transistors T1 and T2 are a common emitter current switching circuit, such that the full conduction of one of the transistors holds the other cut off. Transistor T3 is an inverter output stage and is very similar to other DDTL inverters.

When power is applied to the circuit, both T1 and T2 are forward-biased; however, T1 gains control because its base and collector resistances are lower. In addition, the conduction of T1 causes its base to go positive; this positive shift is coupled through the crystal to decrease the conduction of T2. When T1 saturates, T2 is cut off because of the combination of the low (near +6v) common emitter voltage and the positive coupling into the T2 base. The output of the circuit is +B because inverter T3 is cut off by negative bias.

Once T1 saturates, two actions work to change the state of the circuit. First, the crystal was flexed by the positive shift supplied from the T1 collector; it now begins vibrating at its natural frequency. The piezoelectric action of the crystal generates a negative voltage to the T2 base as the crystal flexes back through its neutral position. Second, the crystal action is aided by the R-C-L tank circuit at the T1 collector. This circuit is tuned to the resonate frequency of the crystal. The conduction of T1 starts oscillation in the tank circuit; the T1 collector drops negative to aid the crystal in turning on T2.

The conduction of T2 cuts off T1 because of the common emitter circuit. T3 is driven to saturation, bringing the output to −B.

The crystal continues to oscillate at its natural frequency, turning T2 off and on. The oscillation of the R-C-L tank continues to supply power to the crystal; each time T2 cuts off, T1 conducts to supply power to the tank circuit.

The oscillator shown in Figure 54 is an example of those circuits that use a crystal between the emitters

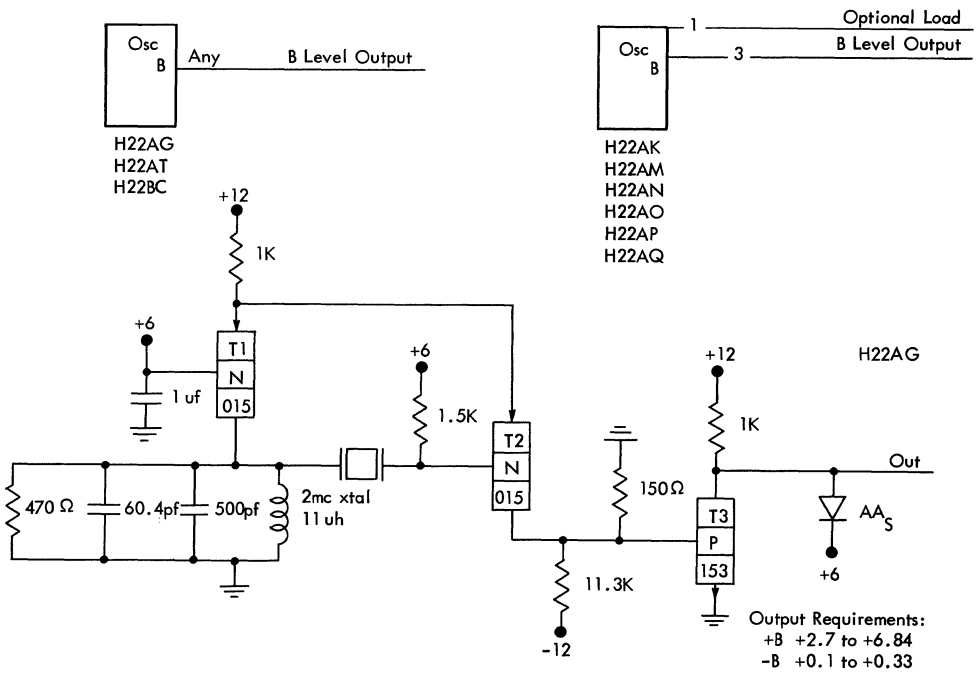


Figure 53. Crystal-Controlled Oscillator, Example 1

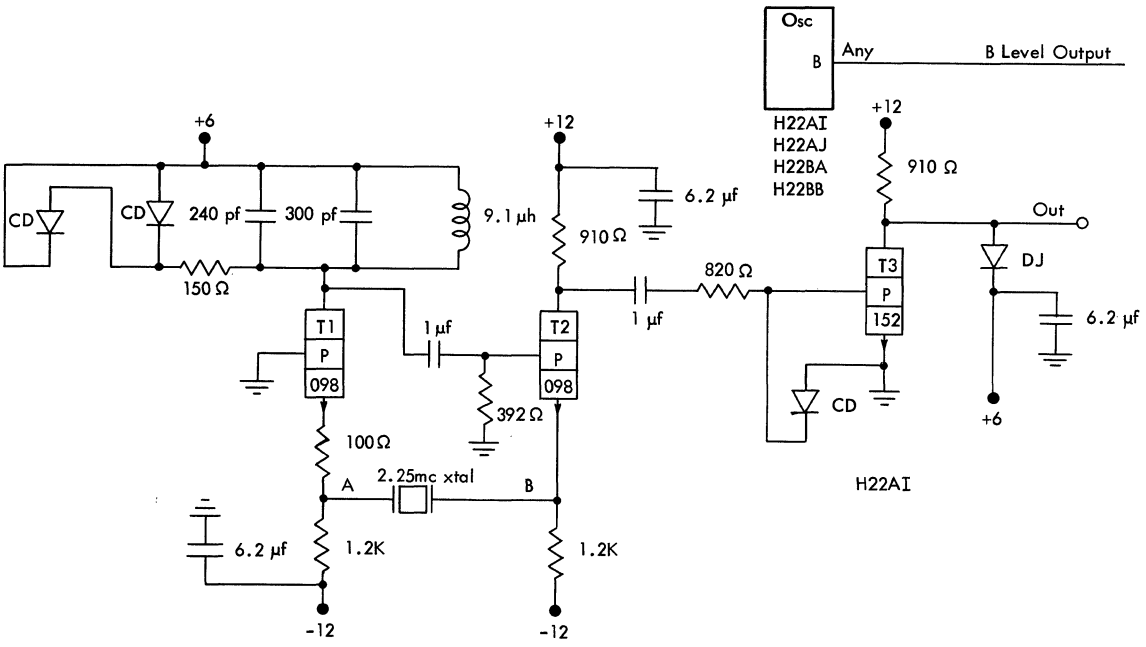


Figure 54. Crystal-Controlled Oscillator, Example 2

of two NPN transistors to establish the output frequency. Transistor T3 is a conventional clamped inverter output stage driven by T2.

When power is applied to this circuit, the initial conduction of T1 and T2 shocks the crystal into vibration. Once set into motion, the crystal behaves as if it were a coil and a capacitor in series and attempts to alternately transfer energy from the coil to the capacitor at the natural resonant frequency of the crystal. As with any crystal oscillator, vibration continues because of energy coupled back to the crystal with the proper phase to reinforce the vibration.

The feedback loop is from point A, through T1 to the T2 base, and back to the other side of the crystal at point B. Transistors T1 and T2 do not saturate or cut off, but increase and decrease their conduction according to the emitter voltage supplied by the vibrating crystal. The power gain of the transistors overcomes losses in the feedback circuit so that the oscillations do not die out.

The tank circuit at the T1 collector is resonate at a slightly higher frequency than the crystal; this causes the tank to appear slightly inductive to compensate for the capacitance in the feedback loop. Because of this compensation, the energy coupled back to the crystal is of the correct phase to reinforce the crystal vibration.

Gated Oscillator

The DDTL gated oscillator (Figure 55) has up to three inputs used to start and stop the circuit. The logic of the inputs is +OR (any +B stops the oscillator) or −AND (all inputs must be −B to allow the oscillator to run). The output frequency of this circuit is controlled by an R-C-L circuit instead of a crystal.

As soon as at least one of the inputs is +B (Figure 55), transistor T1 (an input inverter) is saturated. The voltage divider from the T1 collector places the T2 base at about +5v to forward bias T2. The conduction of T2 puts the common emitters of T2, T3, and T5 near +5v. T3 and T5 are cut off. The input voltage divider to T6 holds T6 cut off; the circuit output is +B. As long as one of the circuit inputs remains at +B, the output remains at +B. When all inputs fall to −B, T1 is reverse biased, and the voltage divider from the T1 collector places the T2 base at about +6.5v. Transistor T2 cuts off and will remain off as long as all inputs are −B.

Transistor T2 cuts off because its base goes positive and its emitter will not rise above about 6v; T5 starts conducting. The conduction of T5 drives T6 (output inverter) into saturation dropping the output to −B.

Transistors T3 and T5 make up a current switching circuit controlled by T4 and the R-C-L network. Transistor T4 conducts at all times, passing current through

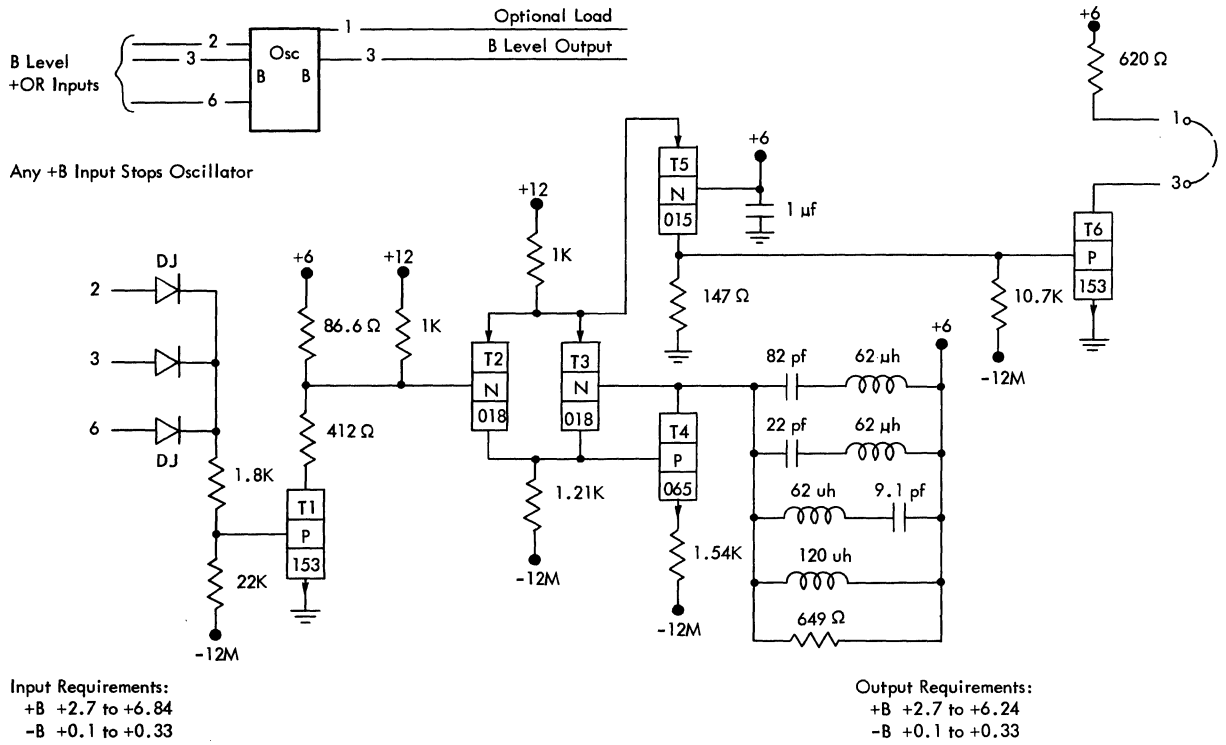


Figure 55. Gated Oscillator

the R-C-L network. When T2 cut off, however, the T4 base went negative, causing T4 to reduce its conduction. The reduced current of T4 was a sudden current decrease through the R-C-L network. This network responds by providing a negative voltage shift to the T3 base after a time interval determined by the components of the network.

When the R-C-L network produces a negative shift, T3 turns on; the emitter circuit turns off T5 and the circuit output goes to +B because T6 is cut off. The conduction of T3 brings the T4 base positive; T4 increases its conduction, driving the T3 base more negative and giving a sudden current increase to R-C-L network. The circuit remains in this state until the delayed response of the R-C-L network drives the T3 base positive. At this time, T3 turns off and T5 turns on, completing the cycle of oscillation.

The R-C-L network components are chosen to give the desired frequency output. Note from the circuit operation that the output is a steady +B level while the circuit is gated off. If the output is +B when the +B input arrives, the oscillator stops immediately; if the output is −B when the +B input arrives, the output shifts to +B. When the oscillator is gated on, the output immediately changes to −B and remains there for the normal time duration.

Line Drivers and Line Terminators

Line drivers and terminators are used when signals must be transferred between widely separated points such as from one frame to another. Line drivers are often called transmitters and line terminators are often called receivers. These circuits are used to reduce the effects of line capacitance and stray noise which rapidly deteriorate large voltage changes.

The line driver converts a B level input to a current line; that is, the line driver provides relatively large current changes into a low impedance at the line terminator. The two input states (+B and −B) are transferred between the line driver and the line terminator as two amounts of current; one high current, the other low current. The line terminator uses the current changes to reproduce the B levels supplied to the line driver.

Driver and Terminator (Q Level)

The line driver and line terminator (Figure 56), normally used to transfer B levels between remote groups of DDTL logic, use a Q level transmission line. These circuits are also called DOT OR driver and multiple line receiver because up to ten drivers and up to ten receivers may be connected to the same transmission line. If the DOT feature is used, however, circuit timing

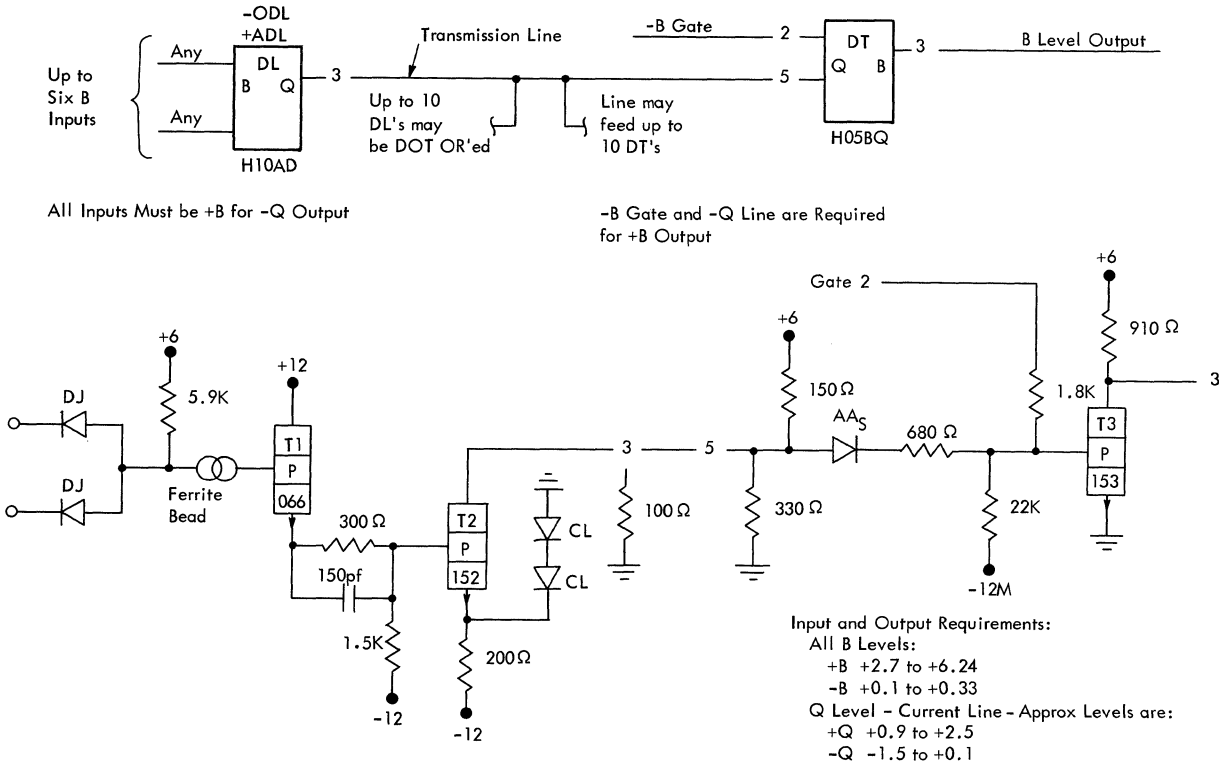


Figure 56. Line Driver and Line Terminator

must be such that only one driver conducts at any one time.

The line driver (Figure 56) will drive up to 300 feet of coaxial cable. This circuit has up to six input diodes that form a +AND circuit controlling emitter follower T1. The ferrite bead around the T1 base lead compensates for stray capacitance to speed the circuit response.

If any input is −B, T1 conducts minimum, supplying a negative voltage (about −1.5v) to the T2 base. The two CL diodes clamp the T2 emitter so that T2 is cut off and only a small leakage current (about 0.04 ma) flows in the transmission line. The resistor divider network at the terminator supplies a plus voltage to saturate T3, regardless of whether the gate input is +B or −B. The terminator output is −B.

When all inputs to the driver are +B, T1 conducts harder to place the T2 base at about −0.5v. T2 conducts into the resistor divider network at the terminator. The current through T2 is approximately 43 ma. If the terminator gate input is +B, the input diode is reverse biased, T3 is forward biased, and the terminator output remains at −B. If, however, the gate input is −B, T3 is cut off, causing a +B output.

The 100-ohm resistor at the driver output prevents line reflections and is considered part of the terminator.

Delay Line Driver and Terminator

Whenever a pulse must be delayed, either a single-shot or a delay line is used. If the delay required is relatively short (for example, in the nanosecond region), a delay line is the usual choice.

A delay line delays a pulse by simulating a long length of coaxial cable. A coaxial cable has inductance and capacitance that cause it to act like a long series of LC circuits. Through a coaxial cable, the propagation of a pulse is considerably slowed, because of the time required to charge the small units of capacitance through an inductance. Delay lines have relatively large inductance and capacitance per unit length to reduce their size.

The problem of driving and terminating a delay line is identical to the problem of transferring a signal over a long distance, because a delay line electrically acts like a long coaxial cable. The delay line, its driver, and its terminator (Figure 57) make up a single circuit that accepts a B level input and delivers a delayed B level output.

Assume a −B input to the delay line driver (Figure 57). Emitter follower T1 conducts minimum and provides the T2 base with a negative voltage. T2 is cut off. The two FC diodes clamp the T2 emitter to about −1.8v and the FB diode clamps the T2 base slightly

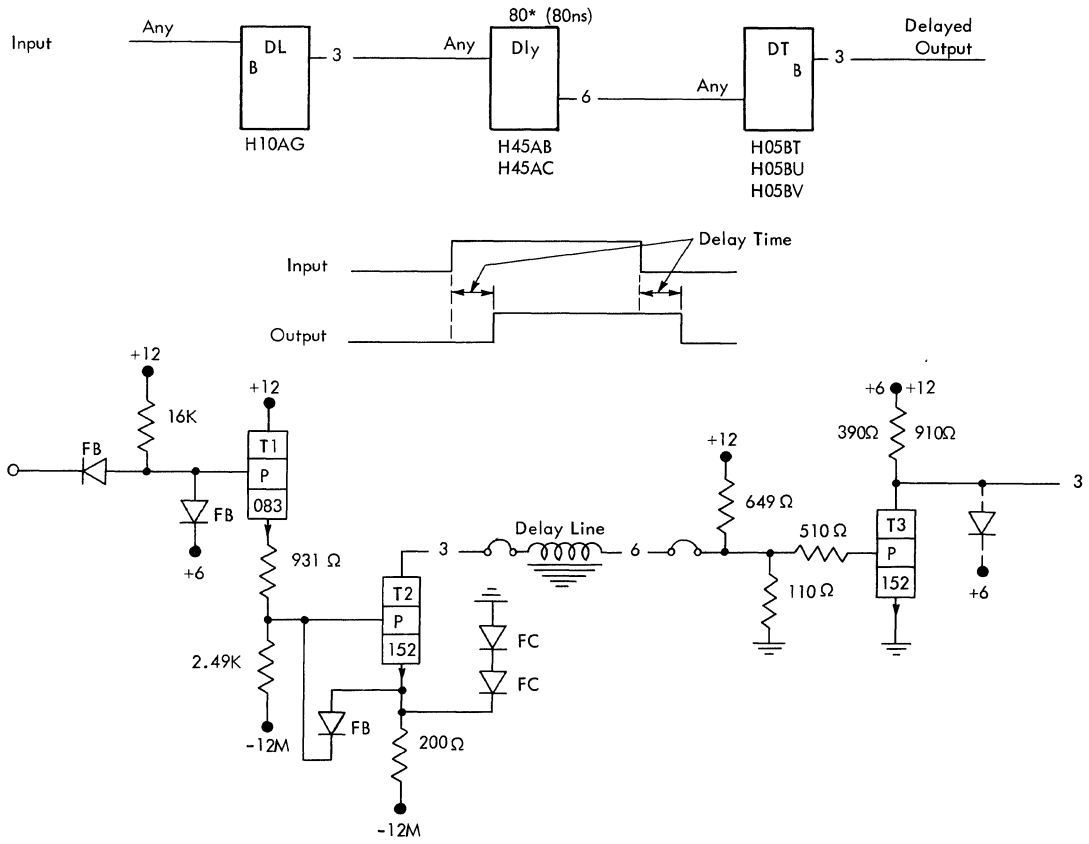


Figure 57. Delay Line Driver and Terminator

more negative than the emitter. The resistor divider network at the terminator holds T3 in saturation, giving a −B output.

When the driver input goes to +B, T1 conducts hard enough to forward bias T2. T2 conducts into the delay line, and after the time delay determined by the delay line, current flows into the resistor divider at the terminator. The T3 base is lowered enough to cut off T3, causing the output to rise to +B.

C Level Driver and Terminator

The C level driver and terminator (Figure 58) are generally used to drive and terminate lines to and from standard computer interfaces. These circuits perform the same function as the Q level driver and terminator, but operate with different values of current.

Both driver and terminator (Figure 58) are inverters. With a −B input, T1 is cut off and only a small leakage current flows through the transmission line. T2 is saturated causing a −B output regardless of whether the gate input is +B or −B.

When the driver input goes to +B, T1 conducts and passes from 13.5 to 50 ma of current into the terminator. If the gate input is +B, the input diode is cut off and T2 remains saturated. If the terminator gate is −B, however, T2 is cut off and the output rises to +B.

V or Q Level Data Set Driver and Terminator

Unlike the other line drivers and line terminators, the data set line driver usually does not drive the terminator. These circuits were designed to transmit and receive signals from a high-speed data set where the following requirements were specified by the company who manufactures the data set:

1. The up level from the driver must be greater than or equal to +1.0v with a current of at least 23 ma when terminated by a 100-ohm resistive load.
2. The driver down level must be −0.7v, or lower, with a current less than, or equal to, 5 ma.
3. The terminator input impedance should be 100 ohms resistive; the terminator is supplied with signals as specified for the driver output.

The driver (Figure 59) is an emitter follower that conducts minimum with a −B input and maximum with a +B input. The 160-ohm collector resistor limits the output current to about 39 ma with the output terminal shorted to ground (thus protecting the circuit).

The terminator conducts with a +Q input unless the gate inputs are used, and one of the switches is set to inhibit. If T2 conducts, the output drops from +B to −B.

Converters and Integrators

EIA Data Set Converters

Most data sets require (and deliver) an E level (often called a V level). This level was established by the Electronics Industries Association so that companies who manufacture data transmission equipment could build compatible machines. The limits established for a +E level are +3v to +25v; −E limits are −3v to −25v. The IBM EIA converters usually supply about +6v for a +E level and about −6v for a −E level.

One B to E converter and three E to B converters are shown in Figure 60. The B to E converter is a PNP inverter that cuts off with a +B input and saturates with a −B input. The 150-ohm resistor protects the circuit in the event that the output should become shorted to ground.

The two inverting E to B converters (lower left and upper right, Figure 60) are very similar. The diode-resistor input network limits the E level to a safe value for the NPN transistor. The transistor is saturated by a +E level and gives a +B output.

The gated non-inverting converter (lower right, Figure 60) has two inverter stages. If the gate input is +B, T4 is held in saturation regardless of the E level input. When T4 is saturated, T5 is cut off and the output is +B. If the gate input is −B, T4 conducts

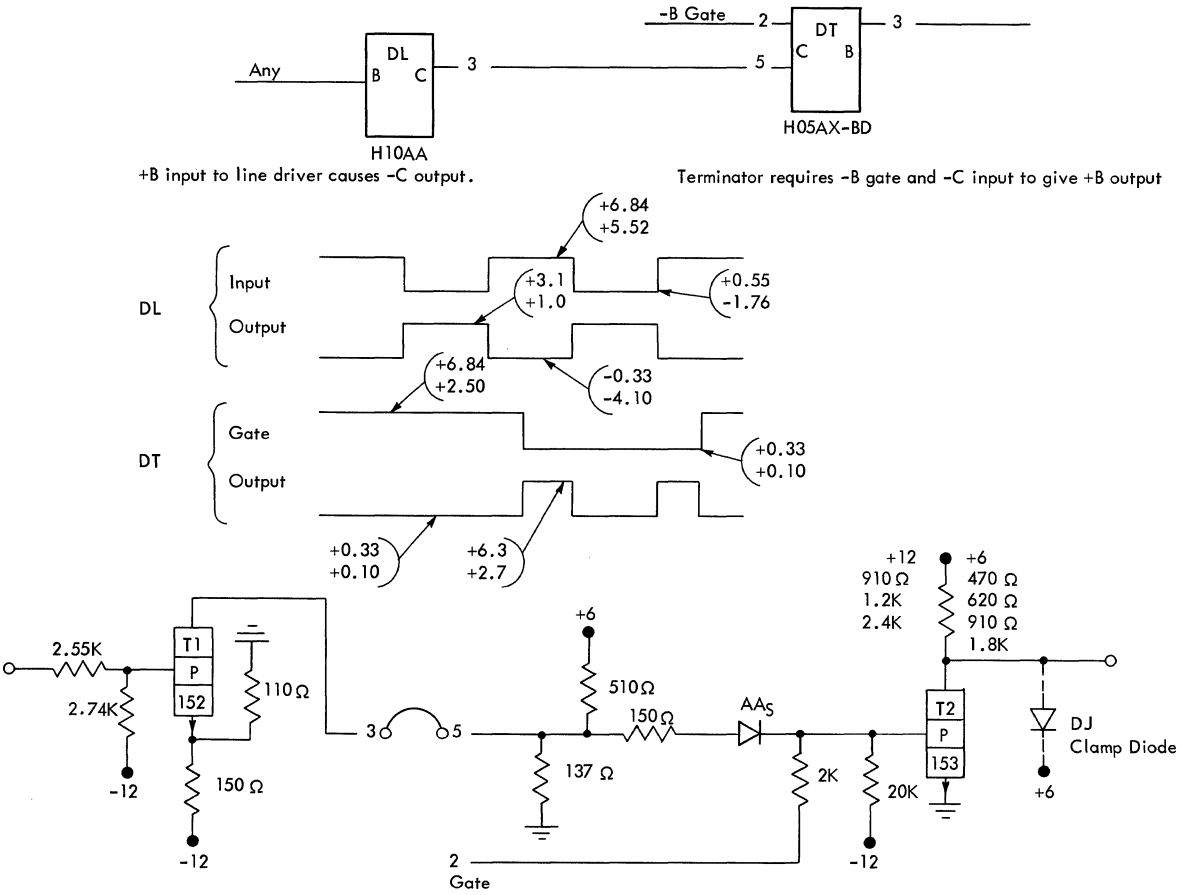


Figure 58. C Level Driver and Terminator

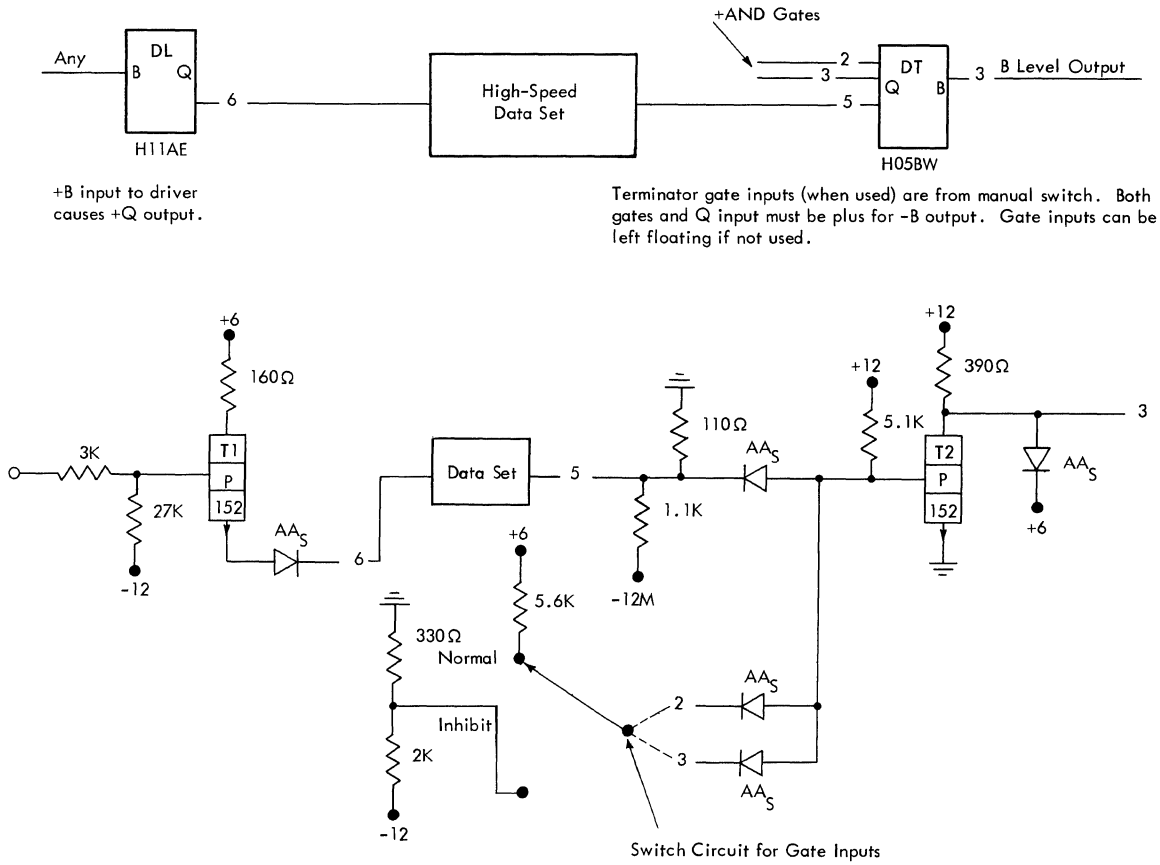


Figure 59. V or Q Level Data Set Driver and Terminator

with a +E input and cuts off with a −E input. When T4 is cut off, T5 is saturated and gives a −B output.

Current Switching Converters

To transfer DDTL signals to current switching circuits, B to P and B to N converters (Figure 61) are necessary. These circuits are essentially line drivers because P and N lines are high-current, low voltage levels.

The B to P converter is a PNP inverter that conducts into the terminating circuit. The transistor does not cut off or saturate, but conducts maximum with a −B input and minimum with a +B input. When terminated properly, the circuit output is an inverted P level.

The inverting B to N converter (upper right, Figure 61) uses a PNP inverter (T2) and an NPN grounded base amplifier (T3). A +B input causes minimum conduction of T2 and maximum conduction of T3 (−N output). A −B input causes maximum conduction of T2 and minimum conduction of T3 (+N output).

The non-inverting B to N converter (lower right, Figure 61) uses a PNP emitter follower. A +B input cuts off the input diode and causes minimum conduction of T4 (+N output). A −B input causes T4 to conduct harder, yielding a −N output.

To convert current switching signals to DDTL signals, P to B and N to B converters (Figure 62) are necessary. The inverting P to B converter uses a grounded base amplifier (T1) and an inverter (T2). A +P input causes minimum conduction of T1 and saturates T2 (−B output). A −P input causes maximum conduction of T1 and holds T2 cut off (+B output).

The non-inverting P to B converter uses a current switching circuit (T3 and T5) and an inverter (T4). A +P input causes T3 to conduct and cuts off T5 (common emitter). The conduction of T3 also holds T4 off, causing a +B output. A −P input cuts off T3 and allows T5 to conduct. T4 is saturated, causing a −B output.

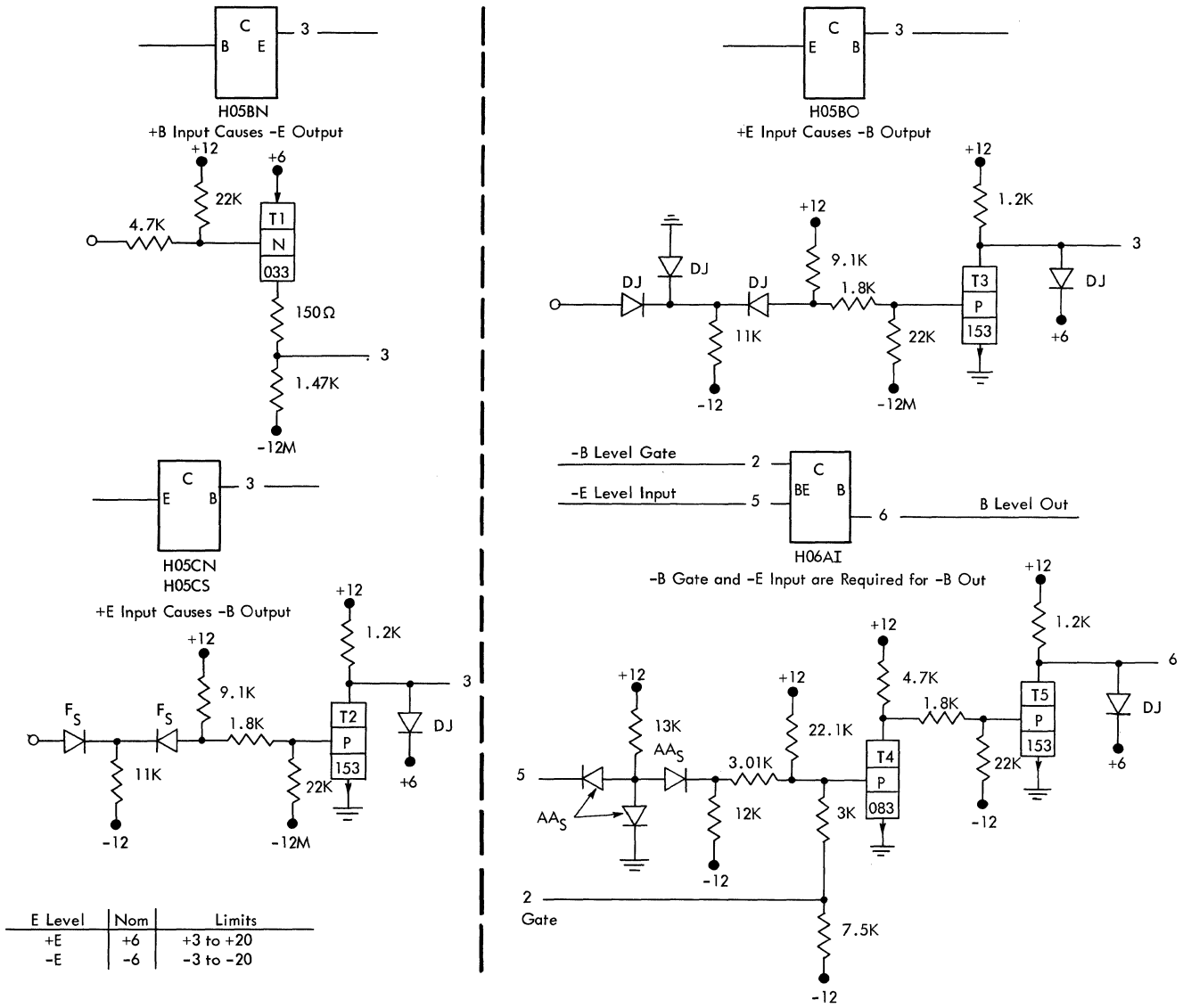


Figure 60. B to E and E to B Converters

The N to B converter uses a grounded base amplifier (T6) and an inverter (T7). A −N input causes minimum conduction of T6 and cuts off T7 (output is +B). A +N input causes maximum conduction of T6 and allows T7 to saturate. With T7 saturated the output is −B.

S Level Converters

A B to S converter and an S to B converter are shown in Figure 63. The B to S converter is a grounded base amplifier that gives an in-phase output. A +B input causes T1 to saturate so that its collector is at very nearly the same potential as its base (about 0v). This is a +S output. If the input is −B, T1 is cut off, causing a −S output.

The S to B converter is an emitter follower with a clamp diode on the output. A +S input is converted to a positive voltage on the T2 base because of the resistor network to +12v; the T2 emitter follows, giving a +B output. A −S input cuts off T2 because the T2 emitter is clamped to the ground; the output is −B.

V Level Converters and Integrators

Switch contacts, relay points, and circuit breakers usually give an open circuit in one position and a

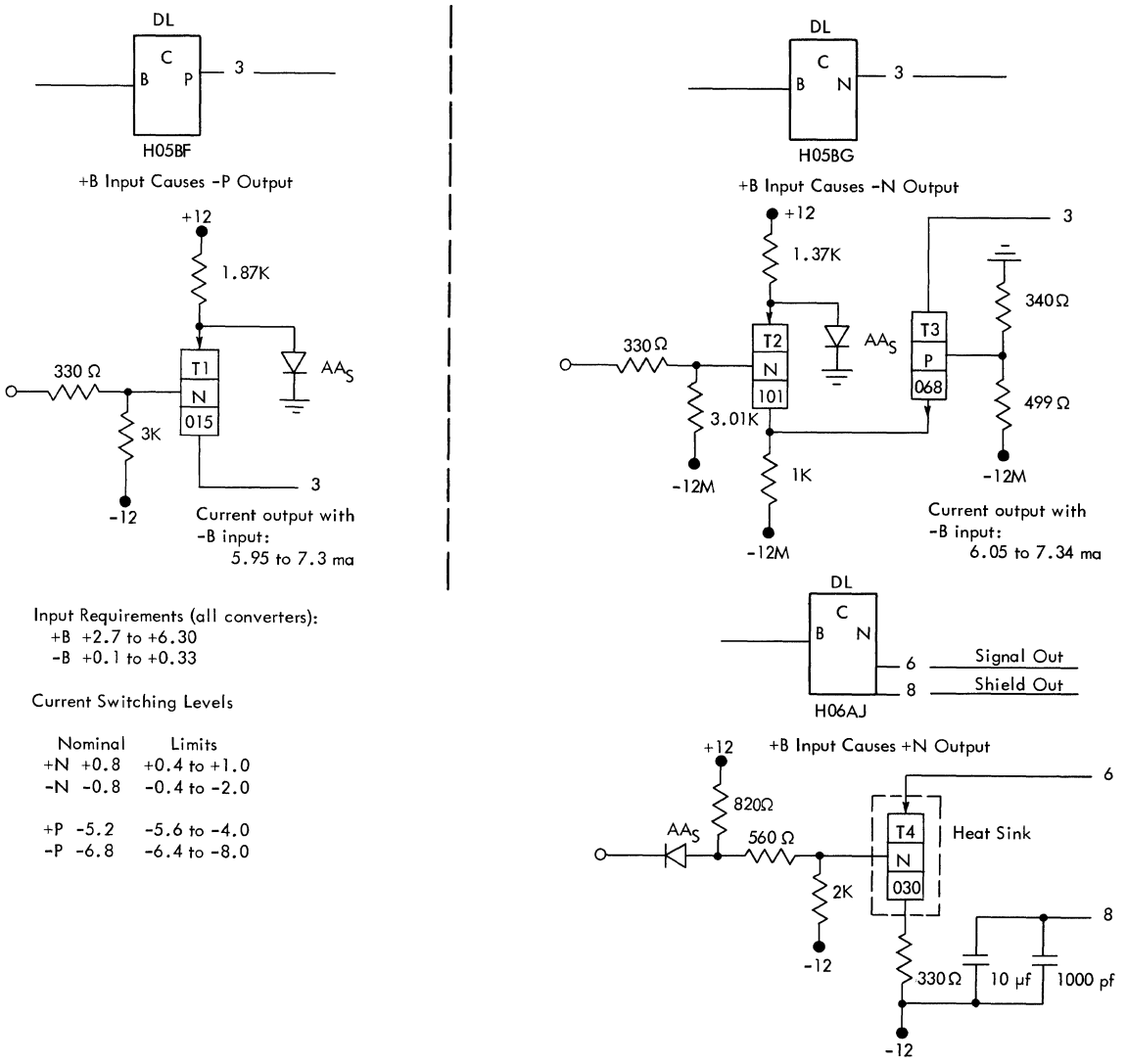


Figure 61. DDTL to Current Switching Converters

power supply voltage in the other position. The V to B converters (Figure 64) accept these inputs and convert them to B levels.

The –12v converter (leftmost, Figure 64) gives a –B output with a –12v input. The diode resistor network gives a +B output when the input is an open circuit.

The –48v converter (center, Figure 64) is identical to the –12v converter except for resistance values.

The passive integrator (rightmost, Figure 64) is used when the input is from relay points or key contacts that may bounce. The input resistor and capacitor prevent fast input changes from affecting the output. When –48v is applied, the capacitor discharges through the 3K input resistor until the output is clamped at ground (–B). When the –48v is removed, the capacitor charges through the 1.2K resistor until the output is clamped at +6v (+B).

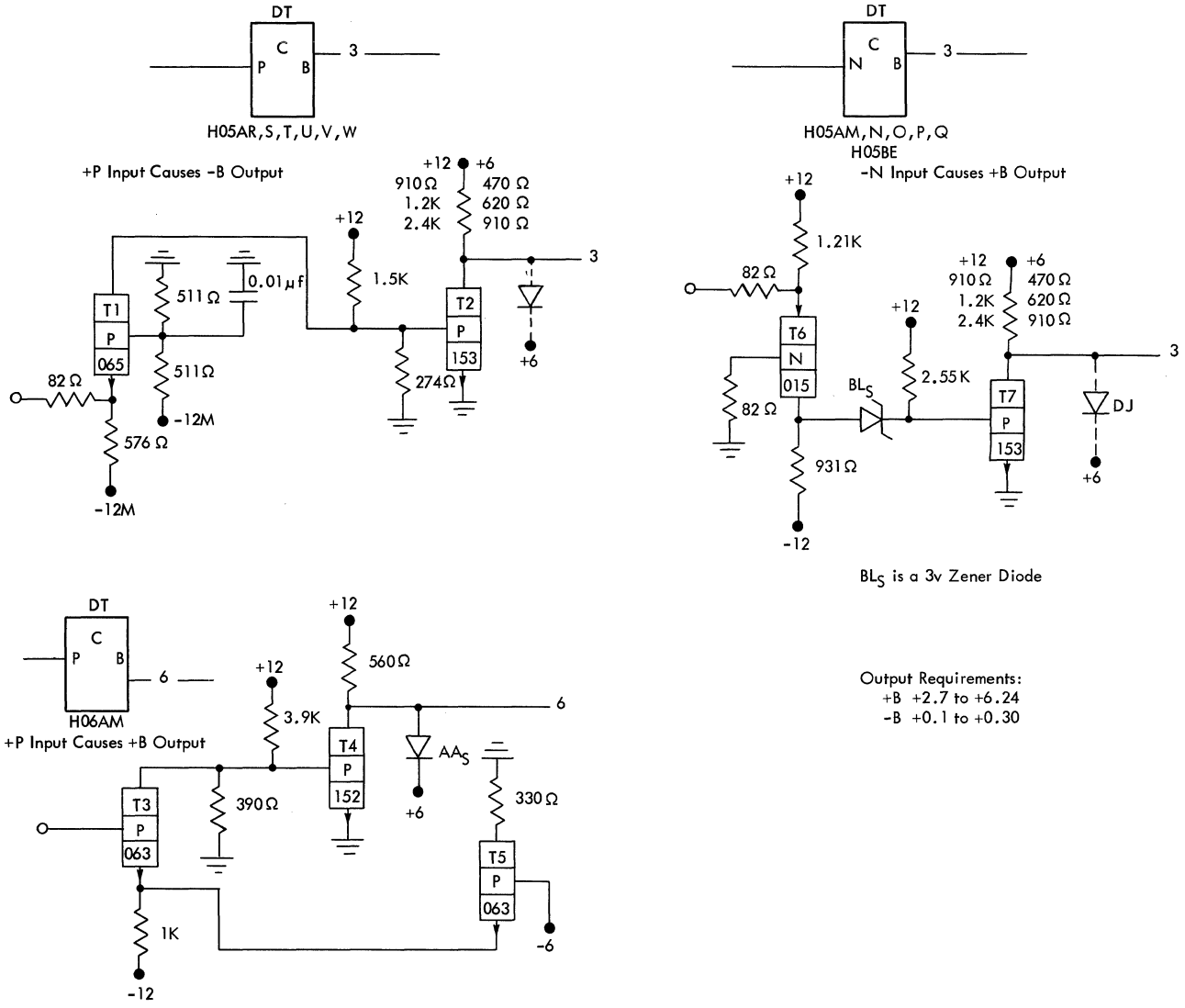
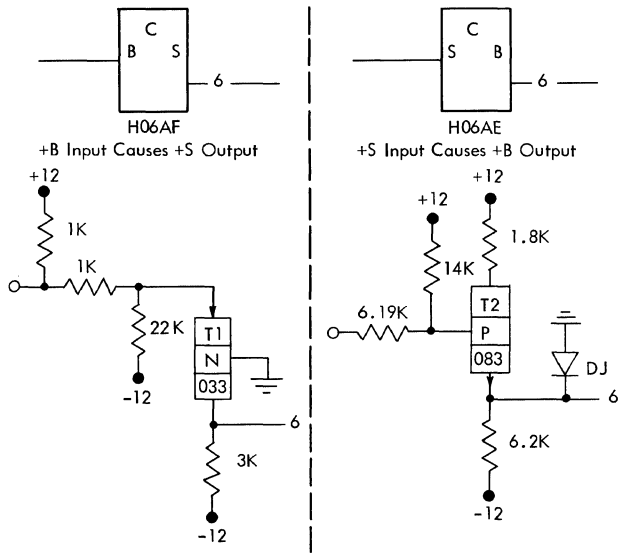


Figure 62. Current Switching to DDTL Converters



B Level Requirements:
+B +2.7 to +6.84
-B +0.1 to +0.33

S Level Requirements:
+S -0.45 to -0.05
-S -12.48 to -5.56

Figure 63. B to S and S to B Converters

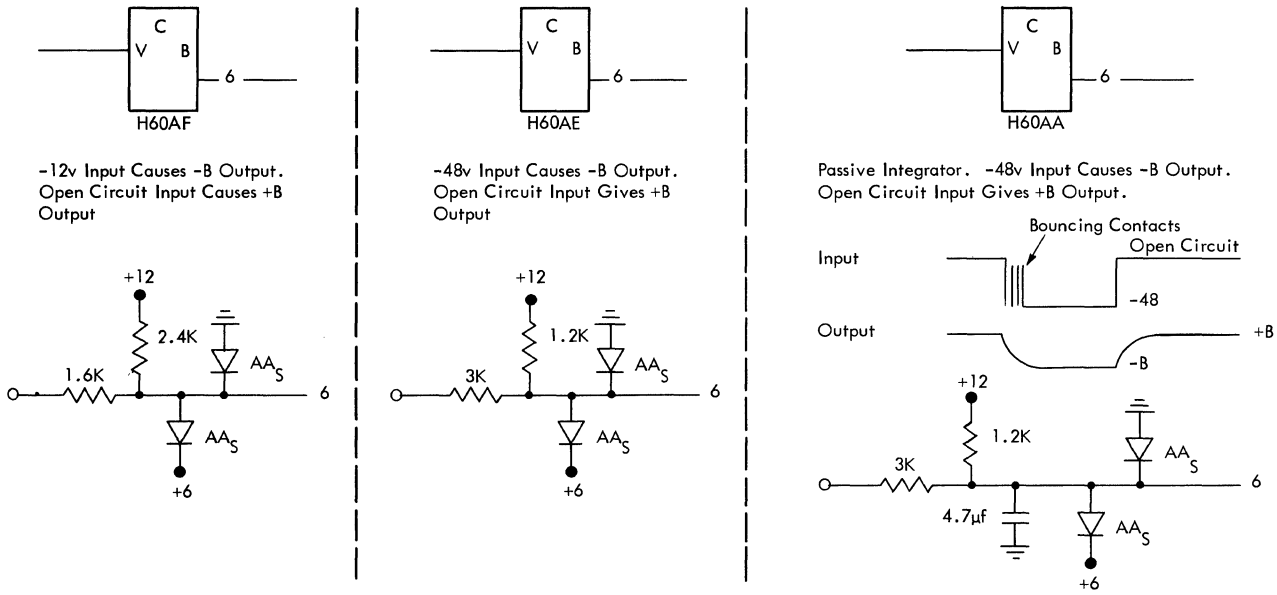


Figure 64. V to B Converters

DDTL circuits are packaged on SMS single cards and SMS twin cards. Both single and twin cards can be plugged into any of the SMS modules. (Refer to the *IBM Customer Engineering Instruction-Reference Manual, Standard Modular System,* Form 223-6900 for information on the various SMS modules.) Because SMS single cards are commonly used with other circuit groups and are described in detail in the *IBM Customer Engineering Manual of Instruction, Transistor Components Circuits,* Form 223-6889, this section describes DDTL circuit packaging on SMS twin cards only.

In addition to packaging information, this section discusses characteristics and shows examples of DDTL ALD's.

SMS Twin Cards

SMS twin cards are physically twice the size of single cards and plug into two vertically adjacent SMS card sockets (Figure 65). Components are mounted across the card; leads go through pre-drilled holes arranged in a fixed matrix.

The twin card has printed wiring on one side of the card only; the remainder of card wiring is accomplished by wire jumpers on the component side. As with other SMS cards, printed contacts on the wiring side of the card mate with the card socket contacts.

Systems diagrams list the location of a twin card as the top socket occupied by the card. As with single cards, pin numbers are from A through R for the top socket, but continue with S through 8 on the bottom socket, instead of repeating (Figure 65).

Voltage Pin Assignments

The last six pins of a twin card are normally used for power supply voltages (Figure 66). A card generally is wired only for the voltages required by the circuits on that card; voltage pins not used can be used for signals. Except for special cases, DDTL circuits require only ground, +6v, +12v, −12v, and −12M.

Note that the voltage pin assignments are very similar to those for single cards. Excess circuit inputs are normally connected to a power supply voltage to give a steady B level input. The two pins most often used are J when a −B is required, and 3 when a +B is required. If the circuit is packaged on a single card, J and L give −B and +B, respectively.

Twin Card Layout

Because most DDTL circuits contain few components and the components used are very small, many DDTL circuits can be packaged on one twin card. The automated method used to generate Systems diagrams is also used to lay out DDTL circuits on twin cards. Figure 67 is the automated circuit layout of the card shown in Figure 65. The layout shows what circuits are on the card and how they are interconnected; these circuits do not necessarily appear together or in the same format in the Systems diagrams where this card is used. Because one twin card has a number of interconnected circuits, the application of a particular card is very limited. Generally, twin cards used in a machine are unique to that machine.

Many circuit outputs are not wired to a backpanel pin (Figure 67); the output of these circuits cannot be scoped unless card extenders are used. Generally however, enough test points are available so that a trouble can be isolated to a particular card without using card extenders. In cases where a circuit output not available at a backpanel pin must be scoped, card reference sheets are necessary to locate the circuit on the card. There are three sheets for each card: sheet 1 is the logic layout (example, Figure 67), sheet 2 is a schematic of the entire card, and sheet 3 shows the physical location of all components on the card.

Unused Twin Card Circuits

Because many interconnected circuits are packaged on one twin card, often one or more circuits on a card are not needed. These unused circuits are shown on Systems unless their inputs and outputs are completely isolated from all other circuits on the card. An unused circuit has one input tied to a voltage that prevents an active output (Figure 68).

Unused circuits on ALD pages are a source of confusion; one of these circuits can only be identified by the one input pin connected to a voltage source that renders the circuit inactive. This voltage can be either ground or +6v depending on the logic of the unused circuit and that of the following circuit.

Unused circuits are not always accidental; they are sometimes included for future expansion (for example, center circuit in Figure 68).

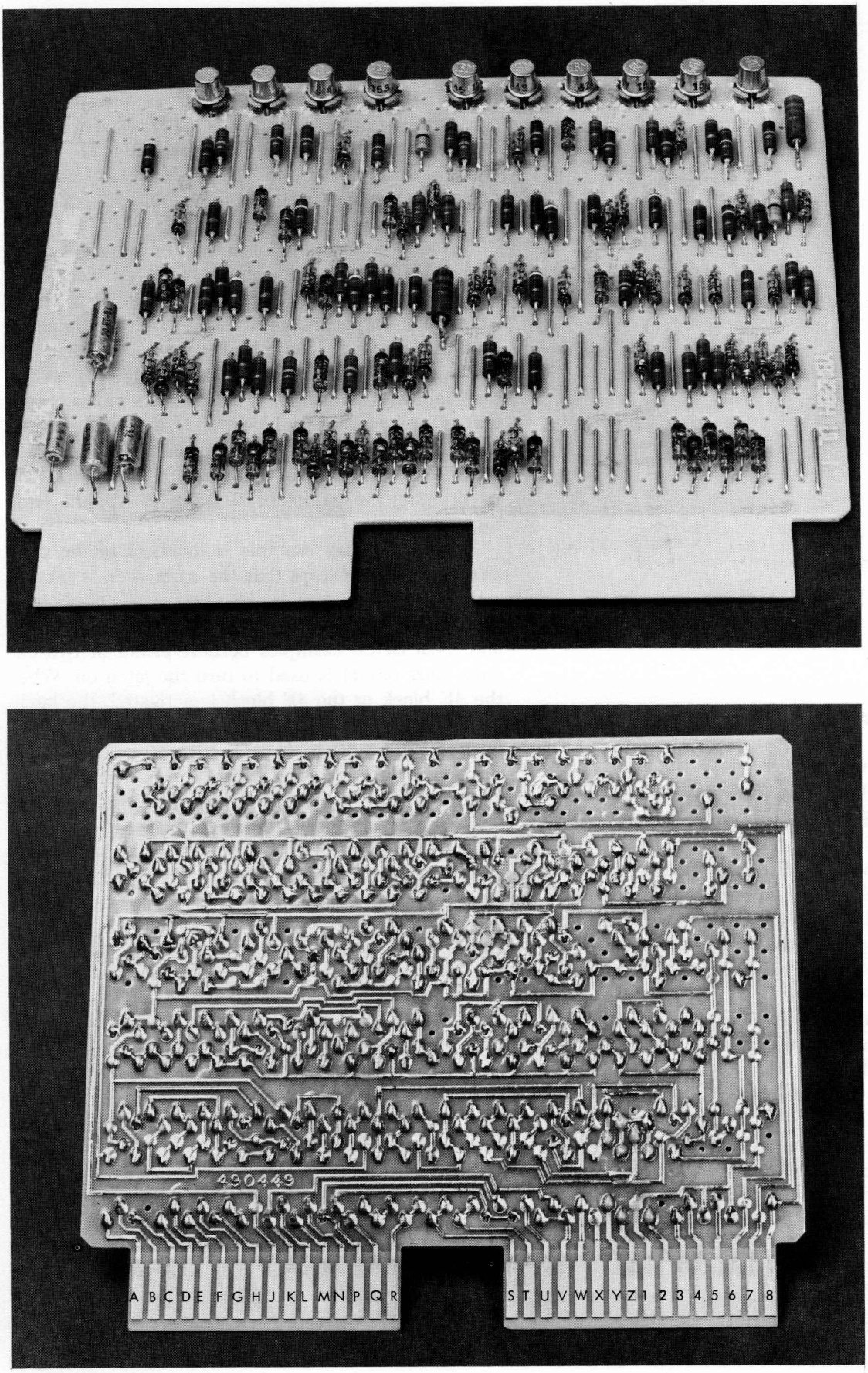


Figure 65. SMS Twin Card

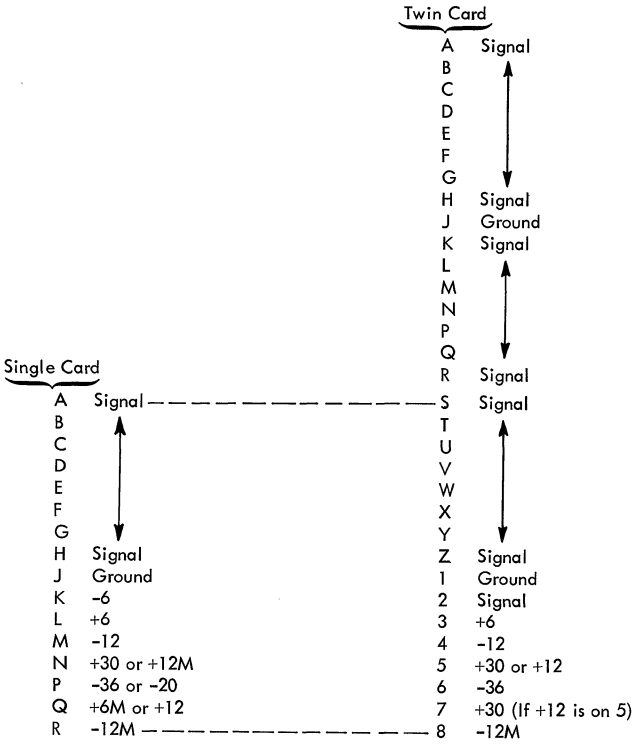


Figure 66. Single and Twin Card Voltage Assignments

Example DDTL Latches

7040-7044 Example Latches

Four examples of the latches used in the 7040-7044 are shown in Figure 69. The top example shows a register position. The latch operates as follows. Any +B input to the 3E block causes a −B output, turning the latch on. The latch is held in the on condition by the latchback from the 2E inverter to the +AND at 4E. As long as the reset line is at +B, the 3E OR has a +B input; when the reset line goes to −B, the latchback is broken and the latch turns off.

The second example shown (FORM DLY 2) is identical to the first example, except that the blocks are arranged differently and the inverter is labeled TI (trigger inverter). The set AND (5H) is not part of the latch circuit.

The BUFFER GO example is identical to the FORM DLY 2 example except that the OR is labeled TO. Again, the set AND's shown are not part of the latch circuit.

The PTR BUSY example is a basic OR-AND latch. A minus input to the 3G block causes a plus output that completes the 3H AND if the resets are inactive. The minus output of the AND is latched back to the OR, holding the latch set. A minus at either reset input breaks the latchback circuit, turning the latch off.

7640 Example Latches

Six latches taken from the 7640 are shown in Figure 70. The STOP SR example is turned on by a −B input to the 4H block. The plus output of the 4H block causes a minus output from the 4I block if the reset input is not active. The minus output from the 4I block is latched back to the 4H block, holding the latch on. A minus input to the 4I block breaks the latchback circuit, turning the latch off.

The EARLY ST example is turned on by a −B input to the 4H block. The plus output of the 4H block completes the 4I AND block if neither reset input is active. The minus output of the 4I block holds the latch on until the latchback loop is broken by a −B reset input.

The CNTR LATCH example operates with +B set and reset inputs. A plus input to 2H causes a minus output that is latched back to block 2I. If the reset input is also minus, the output of 2I is plus and the latch is held on. A +B input to 2I breaks the latchback loop by bringing the output of 2I down to −B; the latch turns off.

The LONG DELAY example is identical to the CNTR LATCH example, except that the reset +OR is labeled −AND.

The TRK START latch differs from the LONG DELAY and CNTR LATCH examples because either of two circuits (DOT OR'ed) is used to turn the latch on. When the 4E block or the 4F block is activated, the latchback to 4G goes minus. If the reset input is down, the latchback from 4G to 4F goes plus, to hold the latch set. Activating the reset input breaks the latchback circuit, turning the latch off. The set AND's (5F and 5G) are not part of the latch circuit.

The CTL DEGATE latch is like the TRK START latch, except that a +AND is DOT'ed to the top half of the latch instead of a +OR.

7710 Example Latches

Six 7710 latches are shown in Figure 71. The PROG CHECK latch is two cross-coupled −OR inverters. A −B input to block 2D causes a plus output that is fed to block 2E. If the two reset inputs are inactive, the output of block 2E is minus. This minus level is coupled back to 2D, holding the latch on. A plus level into either reset input breaks the latchback loop, causing the latch to turn off.

The DATA REG 1 example consists of five blocks. Blocks 1B, 1C, and 4A are DOT OR'ed and make up the on portion of the latch. Block 3A is the off portion; block 5B allows the latchback loop to be broken so that the latch can be reset. The latch is turned on by satisfying the AND at 1B, satisfying the AND at 1C, or bringing a plus input to block 4A. Any of these conditions causes a minus output from 4A that is inverted

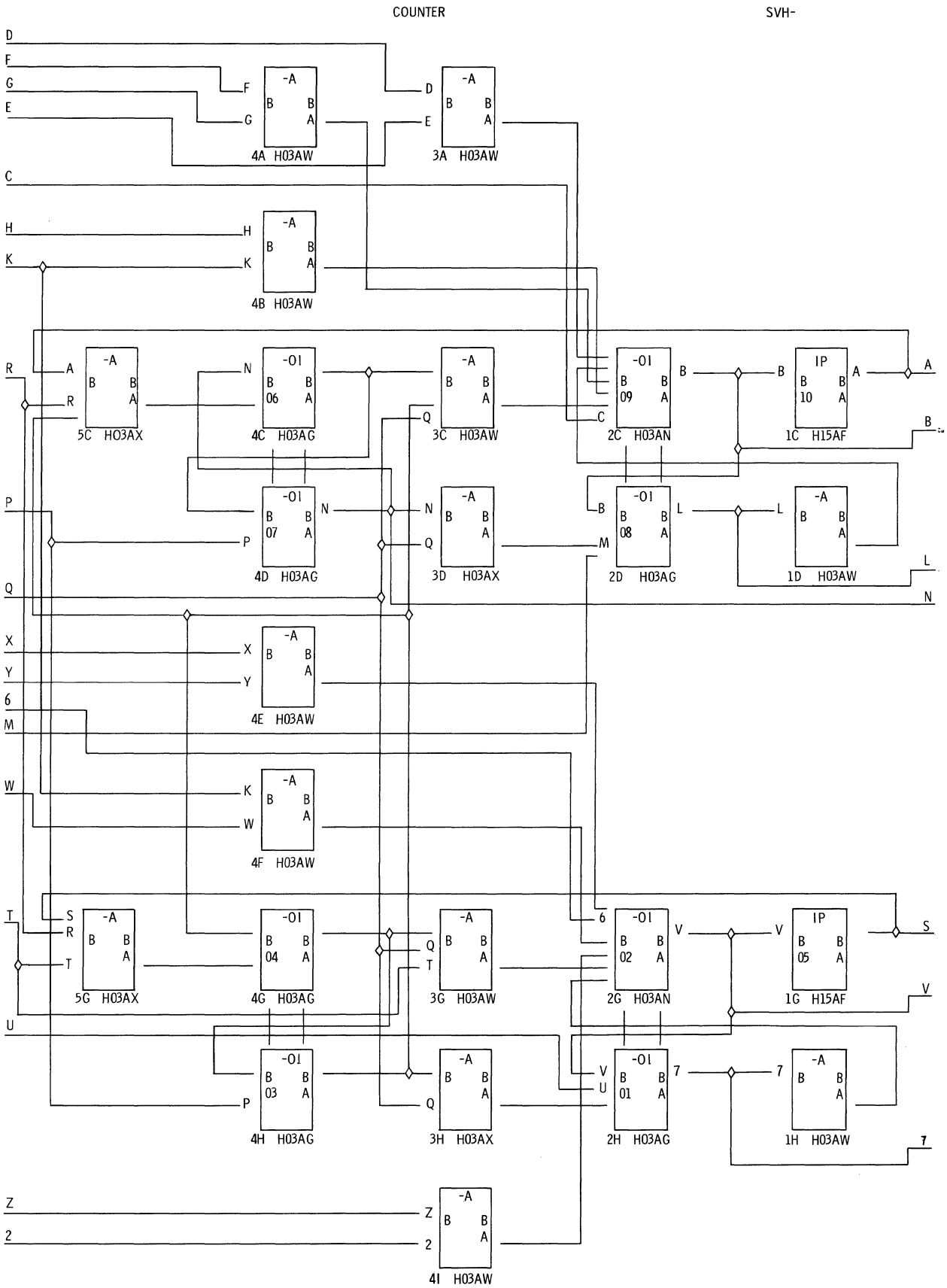


Figure 67. Example of Logic on One Twin Card

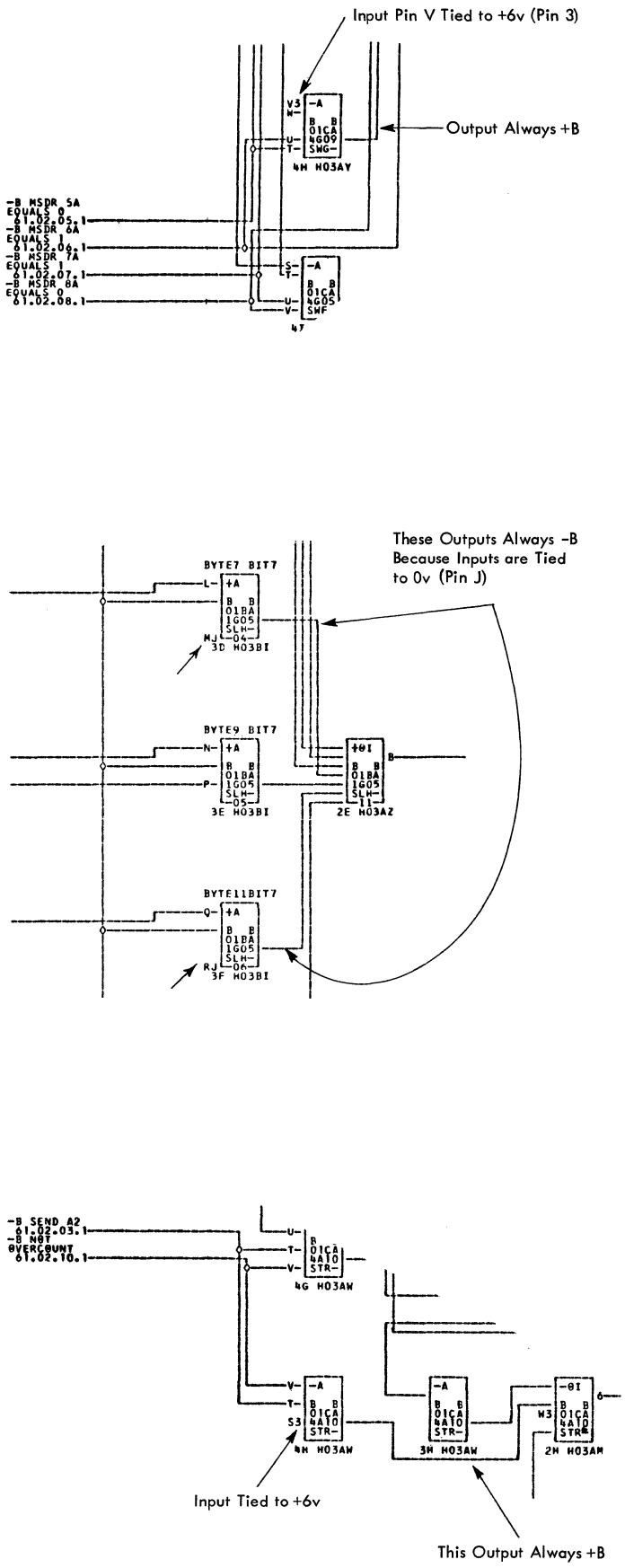


Figure 68. Unused Twin Card Circuits

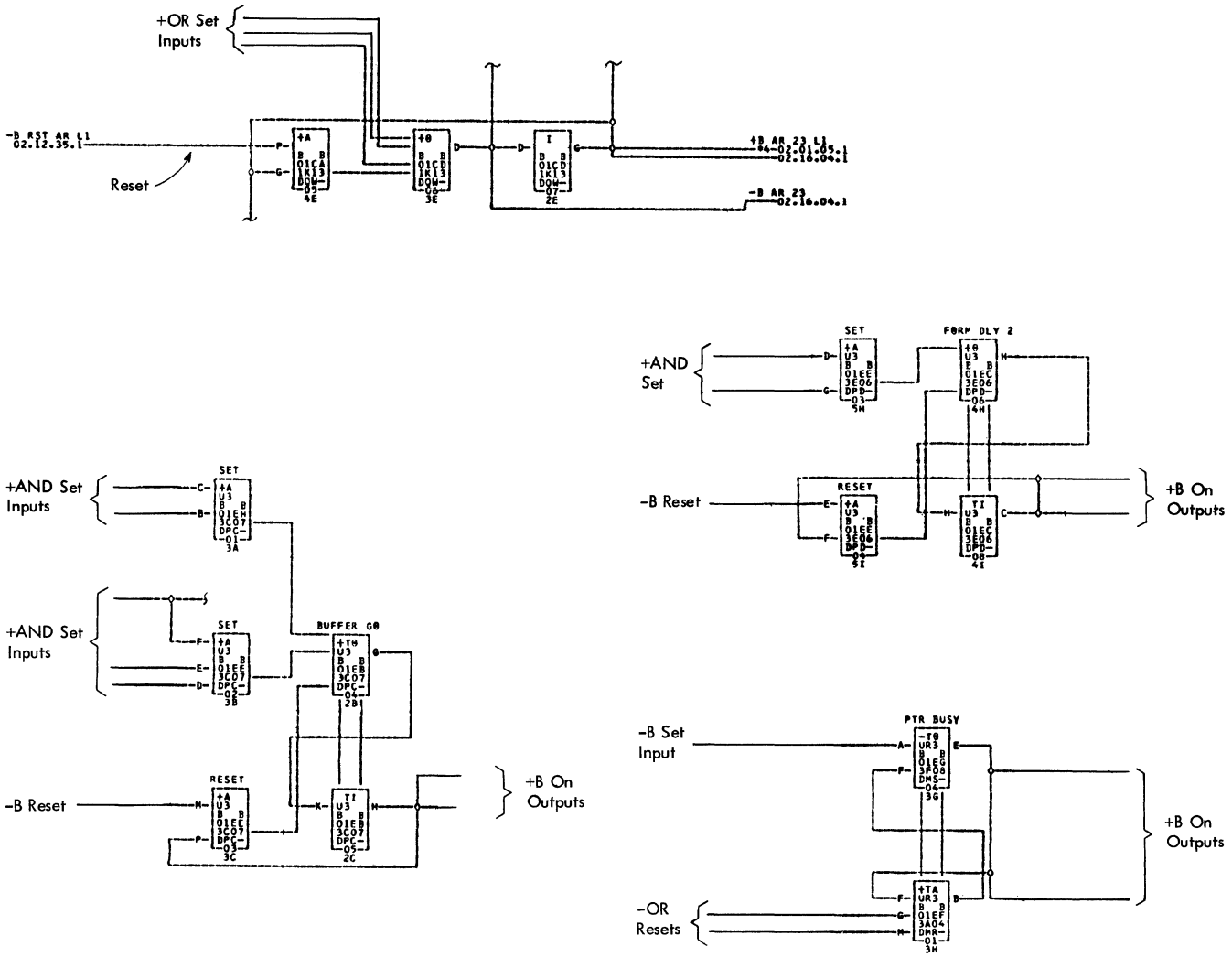


Figure 69. 7040-7044 Latch Examples

by 3A and latched back through 5B, holding the latch on. A minus input to 5B breaks the latchback loop, causing the latch to turn off.

The center left example is a pair of cross-coupled +OR inverters. Blocks 3F and 3G are one-input AND circuits in the latchback loops and have no logical effect on the latch. A plus input to 2F causes a minus output that is coupled through 3G to 2G. Block 2G gives a plus output to hold the latch set if the reset input is inactive. A plus input to 2G turns the latch off.

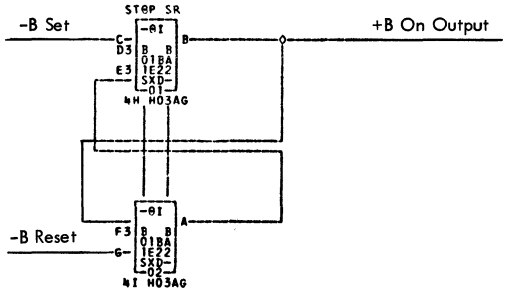
The RECORD CTL latch is cross-coupled +OR inverters identical to the latch just described except for the labeling of the blocks.

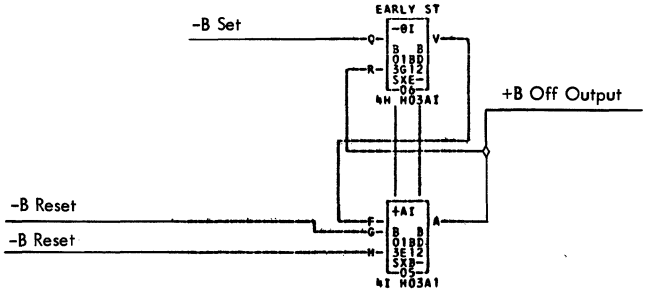
The lower left example is cross-coupled −OR inverters. A minus to block 3D causes a plus output that is latched back to 3E. Block 3E gives a minus output to hold the latch set, if the reset input is inactive. A minus input to 3E breaks the latchback loop, resetting the latch.

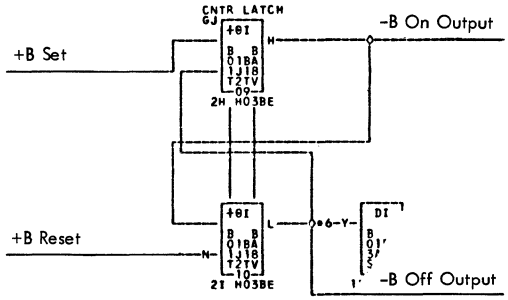
The WRITE LT has two DOT OR'ed blocks (2B and 2C) for the on half of the latch and an inverter (1C) for the off half. Satisfying the AND at 2B or bringing a plus level into 2C sets the latch. Either of these conditions causes a minus into 1C. The plus output of 1C is latched back through 3C, holding the latch on. A minus at either reset input (block 3C) breaks the latchback loop, causing the latch to turn off.

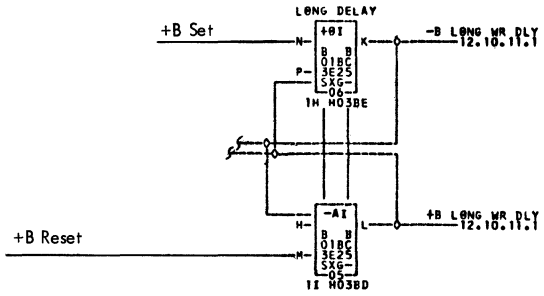
7750 Example Latches

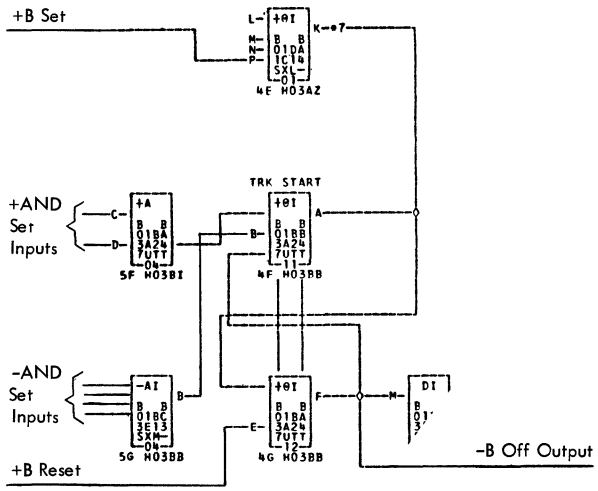
Eight latches from the 7750 are shown in Figure 72. The P-CSDR 4 latch is made up of cross-coupled −OR inverters. The latchback lines are routed through single-input −AND circuits (blocks 3F and 3G) that have no logical effect on the circuit. A minus level into 4F sets the latch; the plus output from 4F is routed through 3F to 4G. If the reset input is inactive, the output of 4G is minus. This minus level is routed











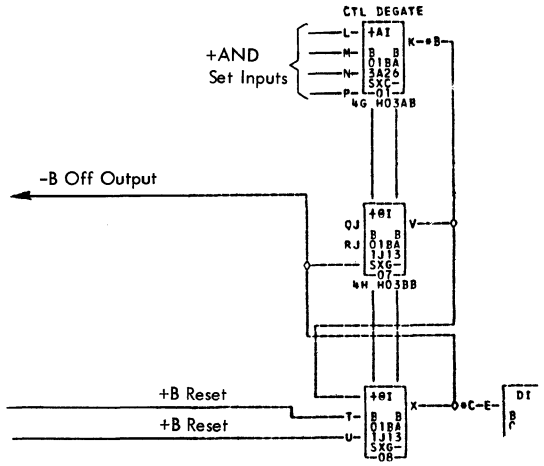


Figure 70. 7640 Latch Examples

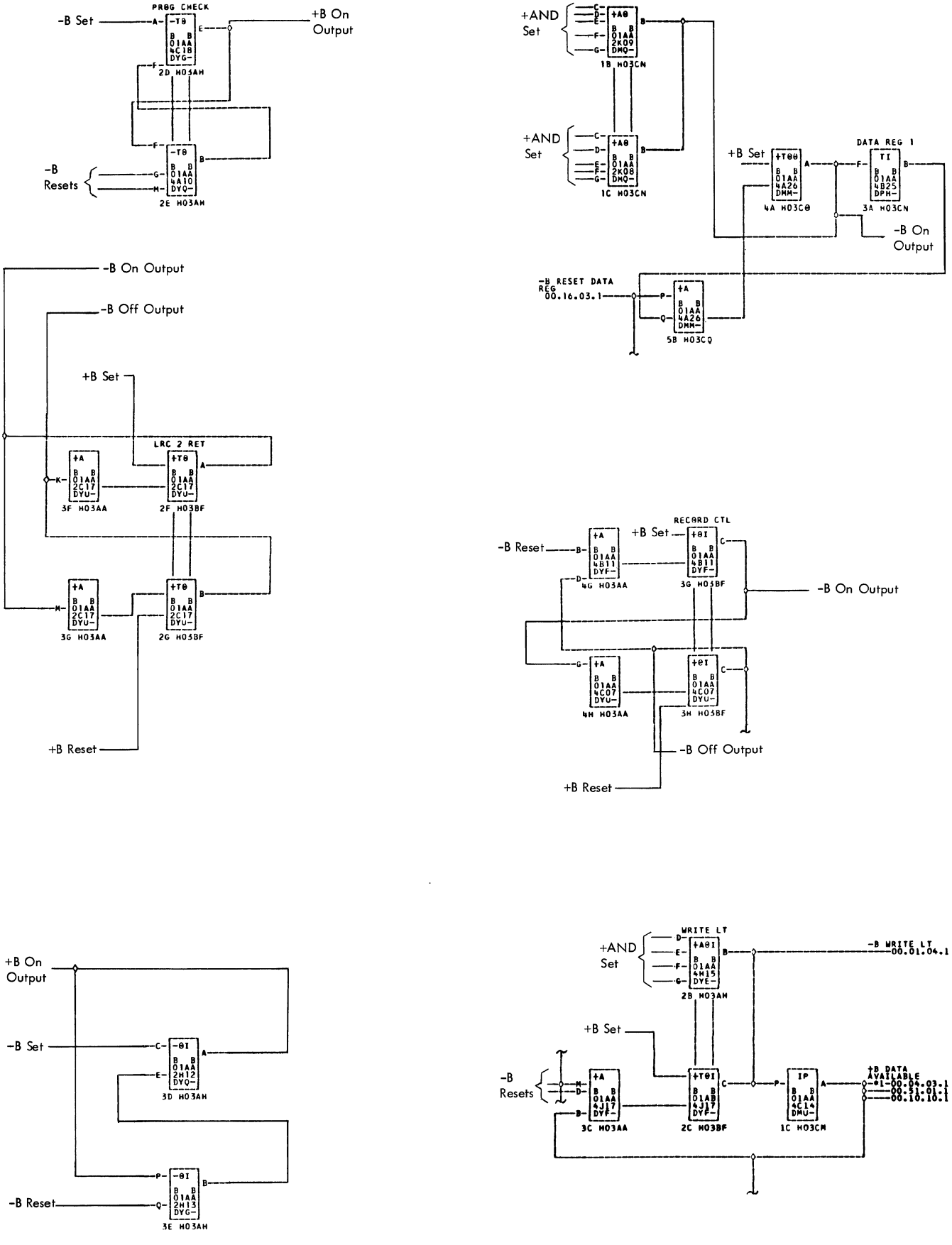


Figure 71. 7710 Latch Examples

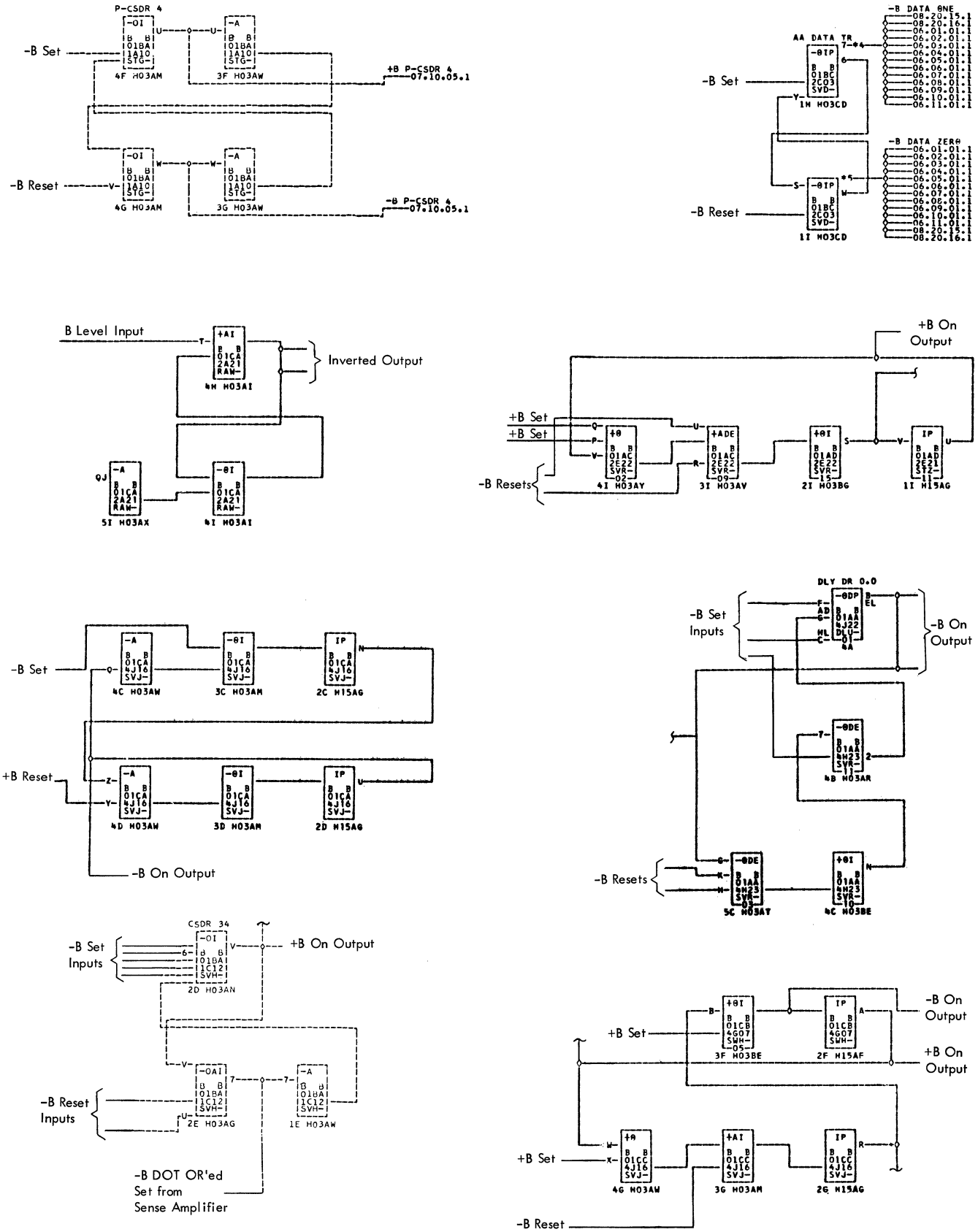


Figure 72. 7750 Latch Examples

through 3G back to 4F, holding the latch on. The latch is reset by breaking the latchback loop when a minus input is applied to block 4G.

The AA DATA TR latch is also made up of cross-coupled –OR inverters. This latch is identical to the P-CSDR 4 latch except that it uses powered inverters (low-power and high-power outputs) and does not have the single-input diode circuits in the latchback loops.

The +AI, – OI example is wired so that it does not function as a latch. Because of the ground input to block 5I, a constant reset is applied to 4I. The output of the circuit is the inverted input to block 4H.

The example consisting of a +O, a +ADE, a +OI, and an IP is turned on by a plus input to block 4I. The plus output of 4I satisfies the +ADE if neither reset is active. The plus output of 3I is converted to a minus from 2I and back to a plus from 1I. The plus output of 1I is latched back to 4I, holding the latch on. The latch turns off when the latchback chain is broken by a minus input to block 3I.

The –A, –OI, IP combination latch is turned on by a minus input to block 3C. The plus output of 3C is converted to a minus output from 2C and combined with the reset input at block 4D. If the reset is inactive, block 3D receives a minus input and gives a plus output. The plus output from 3D is converted to a minus output from 2D and coupled through 4C to 3C, holding the latch on. The latch turns off when a plus input to 4D breaks the latchback loop.

The CSDR 34 latch is turned on in one of two ways: a minus input to block 2D or the conduction of a sense amplifier into block 2E that lowers the output of 2E to –B. Either of these conditions causes a minus level to be coupled back into block 2D, holding the latch on. A minus into block 2E resets the latch.

The DLY DR 0.0 latch is turned on by a minus into either block 4A or 4B. Either of these inputs causes a plus level from 4A that is fed to 5C. If the reset inputs are inactive, the output of 5C is plus and the output of 4C is minus; the latch is held on by the minus input to 4B. A minus input to 5C breaks the latchback loop, turning the latch off.

The lower right latch is turned on by a plus input to either 3F or 4G. If the plus input is to 3F, the minus output from 3F is converted to a plus level from 2F and fed to 4G. The plus level from 4G is converted to a minus level from 3G, if the reset input is inactive. The minus level from 3G is converted to a plus level from 2G and coupled back to 3F, holding the latch set. A plus input to 4G activates the same loop by causing a plus output from 4G, a minus output from 3G, a plus output from 2G, a minus output from 3F, and a plus output from 2F that is coupled back to 4G. The latch turns off when the latchback loop is broken by a minus input to 3G.

7908 Example Latches

Two latches from the 7908 are shown in Figure 73. The MODE CHK latch is set by a minus input to block 3E. The plus output from 3E is converted to a minus output from 3F and coupled through 4F back to 3E, holding the latch set. The latch is reset by bringing a plus input to 4F, breaking the latchback circuit.

The WR 05 CTRL latch is set by a minus input to 3H. This minus input causes a plus output that is latched back to 3I. If the reset input is inactive (plus), the output of 3I is minus to hold the latch on. A minus into 3I breaks the latchback loop, turning the latch off.

Example Shift Cell Circuits

An example of the shift cell circuits is shown in Figure 74. The 5A block is an oscillator that gives a B level square wave output. This output is inverted by block 5B and delivered to the pulse generator at 4B.

If the gate input to the pulse generator is –B, the output from this circuit is a steady –B level. If, however, the gate input is +B, every –B to +B shift from 5B causes a very narrow, sharp rising, positive pulse from the pulse generator. Each pulse is delayed 30 nanoseconds by the delay network at 3B and then delivered to the cell driver at 4I. The cell driver powers the pulse so that several shift cells can be driven in parallel. In addition to powering, the cell driver inverts the pulse so that the shift cells are given a sharp, narrow spike that goes from +B to –B. At each negative shift, the shift cells may change their state, depending on the gate input. A negative gate causes a shift cell to turn on with the next pulse input; a positive gate causes a cell to turn off with the next pulse input. If a shift cell is already in the correct state, a pulse input has no effect.

Binary Latch Configuration

Normally, AC operated triggers are used for applications that require binary operation (complementing). When the set and reset inputs to these AC operated circuits are connected together, an active input causes the trigger to change states: if it was on, it turns off; if it was off, it turns on.

Two latch circuits with appropriate gating are sometimes used to duplicate this binary operation (Figure 75). The circuit shown is an LRC register position that remembers whether there is an even or an odd number of bits. When the first bit is sent (+B 8 bit,

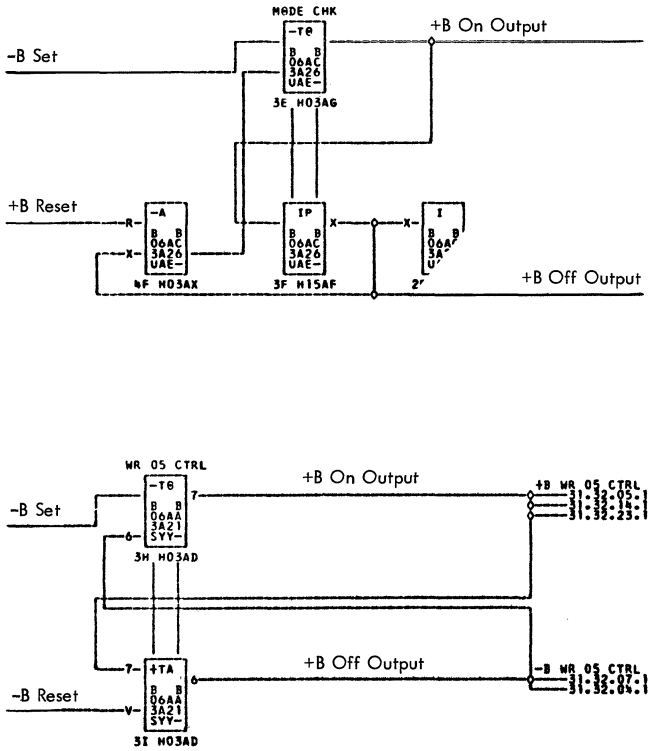


Figure 73. 7908 Latch Examples

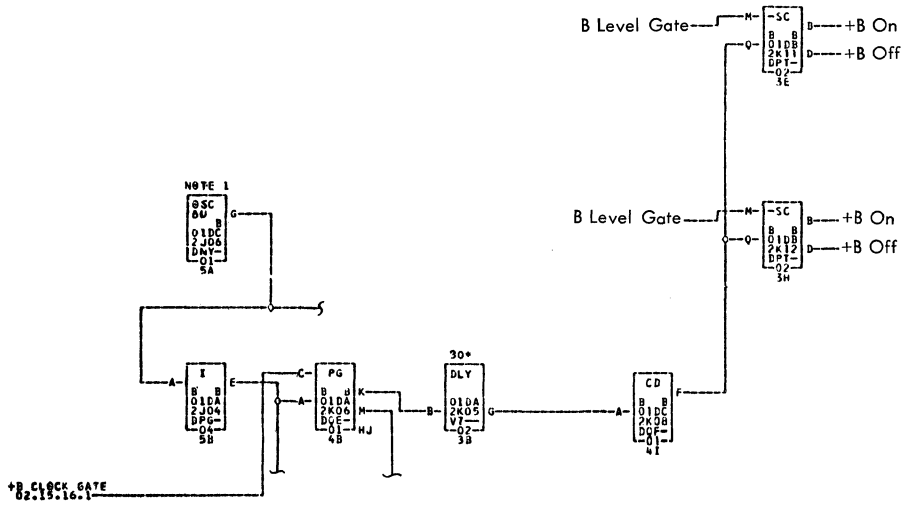


Figure 74. 7040-7044 PG, CD, and SC Example

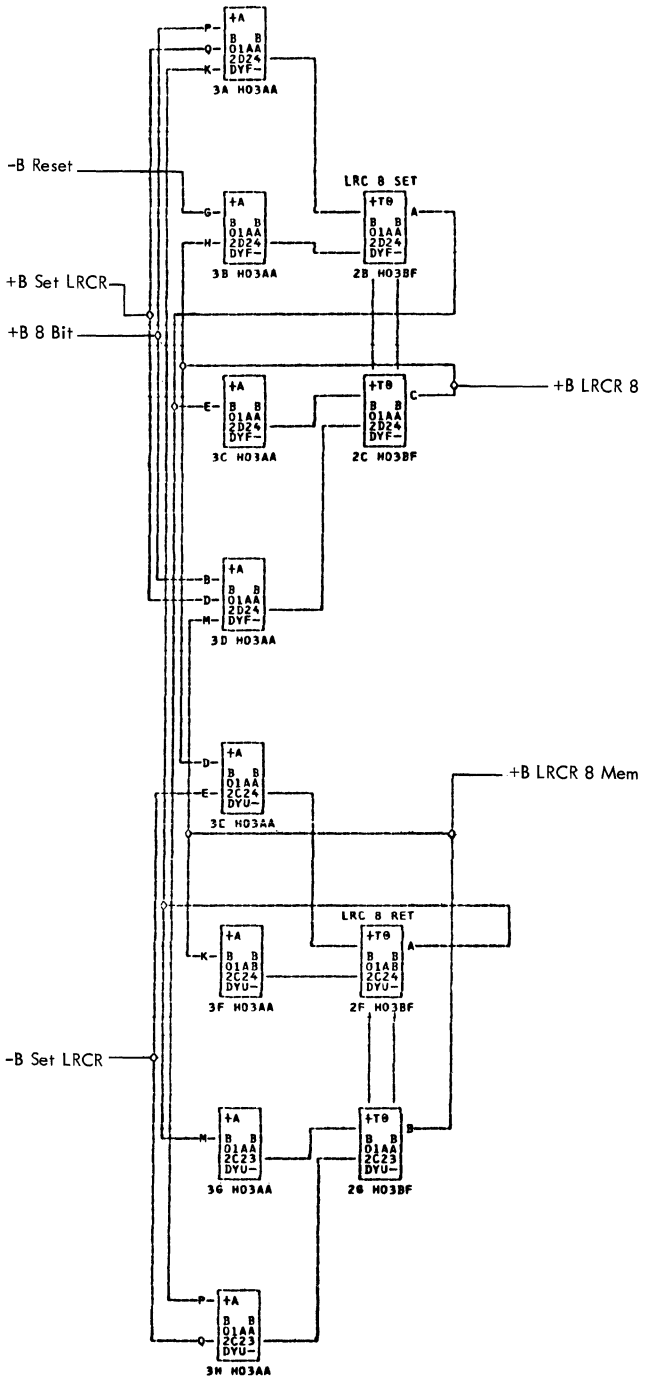


Figure 75. Latch Configuration for Binary Operation

Figure 75), this position of the register should turn on; the second bit should turn the register position off; the third should again turn it on.

Assume that the register has been reset; the LRCR 8 latch and the LRCR 8 memory latch (lower latch) are off. The +B 8 bit line goes plus, indicating the presence of an 8 bit. While the +B 8 bit line is up, a timing pulse (set LRCR) is applied to the circuit. This timing pulse arrives at every bit time regardless of whether there is a bit to be counted. Both polarities of the timing pulse are used: +B set LRCR and −B set LRCR.

With both + B 8 bit and +B set LRCR lines up, the 3A AND is conditioned (third input is +B memory latch off). The +B output of 3A turns on the LRCR 8 latch. The circuit remains in this state (LRCR 8 on, LRCR 8 memory off) until the timing pulse falls. When the timing pulse falls, the −B set LRCR line goes plus conditioning the 3E AND. The +B output of 3E turns the LRCR 8 memory latch on.

With the memory latch on, the next time +B 8 bit and +B set LRCR lines are up, the 3D AND is conditioned to turn off the LRCR 8 latch. When the timing pulse falls this time, the 3H AND turns off the LRCR 8 memory latch.

Each time there is a bit, the timing pulse changes the state of the LRCR 8 latch; when the timing pulse falls, the memory latch records the new state and gates the LRCR 8 latch so that it will go to the opposite state on the next bit.

Exclusive OR Configuration

An exclusive OR circuit has two inputs; it gives an active output if either:

1. Input 1 is active and input 2 is inactive.
2. Input 2 is active and input 1 is inactive.

The name, exclusive OR, was given to this circuit because it gives an active output if either input is present, exclusive of the other input. All other input combinations cause an inactive output.

Figure 76 is an example of an exclusive OR circuit, using two information bits (bit I1 and bit I4) for inputs. An active output (+B) is present only if both inputs to block 4A are −B. (The block performs a −AND function.) Block 4A has two −B inputs only if block 5B is conditioned and block 5A is not conditioned. Bit I1 and not bit I4 or bit I4 and not bit I1 meet this requirement and cause a +B output from the circuit. If both I1 and I4 are present, 5A is conditioned, causing a −B output from the circuit. If neither I1 nor I4 is present, 5B is not satisfied and the circuit output is again −B.

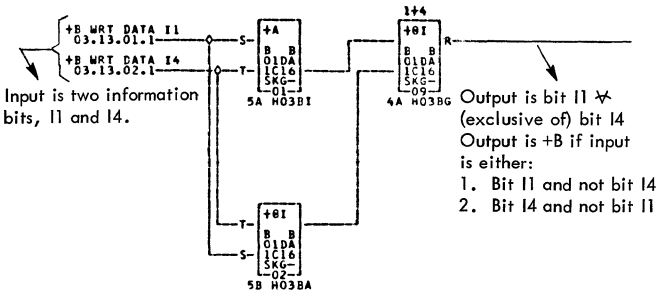


Figure 76. Exclusive OR

Circuit Jumpering for Troubleshooting

There are many techniques for troubleshooting; each person relies mainly on the methods that seem to work best for him. To prove whether a particular section of circuitry is or is not the source of trouble, a jumpering technique is sometimes used. Using this technique, the output (s) of the circuitry in question is jumpered to a power supply voltage so that it is always active (tied up) or always inactive (tied down). If the machine operates without error when the jumper(s) is in, the jumpered circuitry is probably the source of trouble; if the machine does not operate properly, the trouble is elsewhere and the jumper(s) is moved to another section of the machine.

Jumpering should not be used as a primary troubleshooting technique; dense back panel pins often cause mistakes when placing jumpers. These mistakes usually ruin a transistor and adds a second trouble to the machine. Some circumstances, however, warrant the risk involved with jumpering. Generally, these cases arise because of occasional random pulses or other conditions that prevent useful oscilloscope presentations.

If jumpering is used, several precautions must be observed to prevent circuit damage. First, it is the driving circuit and not the driven circuit(s) that require attention; all circuits accept both down and up level inputs without damage. Second, the output of some circuits cannot be connected to a steady level. Third, a circuit that can be jumpered will be ruined if its output is connected to the wrong level. Fourth, extreme care must be used to place the jumper on the correct pins; the chances of jumpering a wrong pin without causing damage are small.

The DDTL circuits that can have their outputs jumpered without damage, and the correct jumpering levels are shown in Figure 77.

Circuit	Jumper Output to		Comment
	Ground	+6v	
Diode +AND (-OR)	X		
Diode +OR (-AND)		X	
All Inverters and Level Setters Except Powered Inverters	X		
Powered Inverters (H15AU, H15AV, H15AW)			Jumper Low-Power Output Only to Ground (High-Power Output will Follow)
Emitter Followers		X	
Binary Triggers			Tie Output of Trigger Inverters to Ground for -B Outputs. If Circuit has Collector Pullover Inputs, These can be Tied to Ground for +B Outputs
AC Triggers			Tie Outputs to Ground for -B Outputs, Collector Pullover Inputs to Ground for +B Outputs
Negative Latches	X		
Shift Cells and Control Triggers			Tie Outputs to Ground for -B Outputs. Tie Off DI Output to Ground for +B On Output; On DI Output to Ground for +B Off Output.
Cell Drivers	X		
Single-Shots	X		
Relay Drivers	X		Picks Relay
Oscillators	X		

Note: Do not jumper the output of circuits not listed.

Figure 77. Circuit Output Jumpering

Appendix A — Examples of Circuit Details

The data presented in this Appendix are intended as examples of DDTL details (such as loading, transition times, and delays). The data are presented for those who desire more detail than is presented in the main body of the manual. From this data, two things can be extracted:

1. The many factors that influence a particular circuit behavior or characteristic (e.g., circuit delay).
2. Approximations of DDTL delays, transitions, driving currents, and so forth.

The data presented here are not intended to guide circuit designers; this data should not be used as a reference in any application where complete, specific DDTL characteristics are needed.

Loading

Figure 78 shows the number of loads than can be driven if no more than four input diodes are used. Where more than four input diodes are used, the branching factor equations must be used to calculate loadings.

Branching Factor Equations

DRIVING RULES

1. The first stage in a chain of emitter followers and the low-power inverter must be driven by a clamped 6-volt output.
2. A chain of two emitter followers may be driven by a 5v swing.
3. A chain of one emitter follower may be driven by a 4v swing.
4. The maximum consecutive number of emitter follower stages is limited to three.
5. The minimum UP level for both the OR and AND inputs of the +0 +ALS is 3.2 volts.
6. The maximum number of inputs to the AND section of the +0 +AI is four.
7. One AND input of the +A +OI must be clamped to a 6-volt supply.
8. The DDTL emitter follower cannot drive any double-level basic inverter logic blocks, or any +AND basic inverter logic blocks. The reason for this limitation is the possible rise of the −B level through an emitter follower.
9. The first and second stages of an emitter follower chain can drive the Basic Inverter block directly, and can drive the +OR basic inverter block where the +OR has up to six inputs.
10. The third stage of an emitter follower chain can drive a +OR basic inverter block. The +OR can have up to six inputs, provided no other input is driven by an emitter-follower third stage.

POSITIVE DRIVE

a = Total number of collectors tied to the output node, where $1 \leq a \leq 6$.
n = Total number of fan-in diodes including the driven diode of each block.
V = number of OR inputs of +0, +A, EF
W = number of OR inputs of +0, +A, I
X = number of OR inputs of +0, I
Y = number of OR inputs of +0, +A, LS
Z = number of inputs of basic inverter

Clamped Inverters (basic inverter, level setter, low-power inverter): Collector supply at 12 volts.

1. @ 6.3 v

   $1.65V + 1.80W + 3.48X + 2.38Y + 3.63Z \leq I - n\,(.03) - a\,(.03)$

   Rc = 360Ω, I = 13.8ma ⎫ Used only
   Rc = 470Ω, I = 10.6ma ⎭ with LPI
   Rc = 910Ω, I = 5.46ma
   Rc = 1.2k, I = 4.0ma
   Rc = 2.4k, I = 2.0ma
   Rc = 3.9k, I = 1.27ma

2. @ 3.2 v

   $1.48W + 1.70X + 1.99Y + 1.81Z \leq I - n\,(.03) - a\,(.03)$

   Rc = 360Ω, I = 21.9ma ⎫ Used only
   Rc = 470Ω, I = 16.8ma ⎭ with LPI
   Rc = 910Ω, I = 8.65ma
   Rc = 1.2k, I = 6.58ma
   Rc = 2.4k, I = 3.29ma
   Rc = 3.9k, I = 2.03ma

3. @ 2.7 v

   $1.43W + 1.40X + 1.52Z \leq I - n\,(.03) - a\,(.03)$

   Rc = 360Ω, I = 23.4ma ⎫ Used only
   Rc = 470Ω, I = 17.8ma ⎭ with LPI
   Rc = 910Ω, I = 9.23ma
   Rc = 1.2k, I = 7.0ma
   Rc = 2.4k, I = 3.5ma
   Rc = 3.9k, I = 2.15ma

Unclamped Inverters (basic inverter): Collector supply at 6 volts.

1. @ 3.2 v

   $1.48W + 1.70X + 1.99Y + 1.81Z \leq I - n\,(.03) - a\,(.03)$

   Rc = 470Ω, I = 5.18ma
   Rc = 620Ω, I = 3.93ma
   Rc = 910Ω, I = 2.68ma
   Rc = 1.8k, I = 1.35ma

DRIVING LOAD RULES

DRIVERS						LOAD	POSITIVE LOADS					NEGATIVE LOADS			
							△ O - I	△ O-A-I	BASIC I	O-A-LS	DI	△ A - I	△ A-O-I	LPI #2	ALS
						V IN UP	6.3 / 2.7	6.3 / 2.7	6.3 / 2.7	6.3 / 3.2	6.3 / 2.7	V IN DWN / +.1	+.1	+.1	+.1
						I IN ma	3.57 / 1.47	1.89 / 1.52	3.62 / 1.52	2.57 / 2.18	2.7 / 1.2	-0.98	-1.84	-2.37	-1.6
CIRCUITS			V OUT	+I ma	-I ma										
INVERTERS	UNCLAMPED	470Ω	2.7	6.2	0	4	4	4	2**	5	0	0	-	-	
		620Ω	2.7	4.7	-3.4	3	3	3	1**	3	3	1	-	-	
		910Ω	2.7	3.2	-6.6	2	2	2	1**	2	6	3	-	-	
		1.8K	2.7	1.61	-10.2	1	1	1	0**	1	10	5	-	-	
	CLAMPED	910Ω	6.3 / 2.7	5.46 / 9.23	0	1 / 6	2 / 6	1 / 6	2 / 3**	2 / 7	0	0	0*	0	
		1.2k	6.3 / 2.7	4.0 / 7.0	-3.2	1 / 4	2 / 4	1 / 4	1 / 3**	1 / 6	3	1	1*	2	
		2.4k	6.3 / 2.7	2.0 / 3.5	-8.6	0 / 2	1 / 2	0 / 2	0 / 1**	0 / 2	8	4	3*	5	
		3.9k	6.3 / 2.7	1.27 / 2.15	-10.7	0 / 1	0 / 1	0 / 1	0 / 0**	0 / 1	10	5	4*	6	
LOW PWR INVERTER		IP 360Ω	6.3 / 2.7	13.8 / 23.4	0	3 / 15	7 / 15	3 / 15	5 / 10**	5 / 19	0	0	0*	0	
		IP 470Ω	6.3 / 2.7	10.6 / 17.8	-8.5	3 / 12	5 / 11	2 / 11	4 / 7**	3 / 14	8	4	3	5	
		IP 910Ω	6.3 / 2.7	5.46 / 9.23	-21.7	1 / 6	2 / 6	1 / 6	2 / 3**	2 / 7	22	11	9*	13	
TRIGGER INVERTER		680Ω	6.3 / 2.7	7.2 / 12.3	-1.1	2 / 8	3 / 8	1 / 8	2 / 5**	2 / 10	1	0	0*	0	
		820Ω	6.3 / 2.7	5.7 / 9.8	-7.6	1 / 6	3 / 6	1 / 6	2 / 4**	2 / 8	7	4	3*	4	
		1.2K	6.3 / 2.7	3.65 / 6.5	-10.8	1 / 4	1 / 4	1 / 4	1 / 3**	1 / 5	11	5	4*	6	
		1.8K	6.3 / 2.7	2.0 / 3.9	-16.2	0 / 2	1 / 2	0 / 2	0 / 2**	0 / 3	16	8	6*	10	

Note:

* Driver must be loaded as to have at least a 6 v output for UP case.

△ Loadings calculated for no greater fan - in than 4 ON driven blocks - if greater fan is desired, use equations to calculate loadings.

** Computed with V_{out} = 3.2v

Figure 78. Example Load Chart

2. @ 2.7 v

1.43W + 1.40X + 1.52Z ≤ I − n (.03) − a (.03)

Rc = 470Ω, I = 6.20ma
Rc = 620Ω, I = 4.70ma
Rc = 910Ω, I = 3.20ma
Rc = 1.8k, I = 1.61ma

Emitter Followers: Re is the emitter resistor.

1. First Stage @ 4.77 v

1.50V + 2.59X + 2.19Y + 2.73Z ≤ I − n (.03)

Re = 5.6k, I = 11.5ma
Re = 3.0k, I = 8.71ma
Re = 2.2k, I = 6.51ma
Re = 1.82k, I = 4.78ma

2. Second Stage @ 3.95 v

1.43V + 2.11X + 2.08Y + 2.25Z ≤ I − n (.03)

Re = 5.6k, I = 11.0ma
Re = 3.0k, I = 8.32ma
Re = 2.2k, I = 6.22ma
Re = 1.82k, I = 4.58ma

3. Third Stage @ 3.2 v

1.69X + 1.99Y ≤ I − n (.03)

Re = 5.6k, I = 6.39ma
Re = 3.0k, I = 3.84ma
Re = 2.2k, I = 1.84ma
Re = 1.82k, I = 0.27ma

NEGATIVE DRIVE

n = Total number of fan-in diodes including the driven diode of each block.
P = Number of AND inputs of +0, +A, EF
Q = Number of AND inputs of +A, I
R = Number of AND inputs of +A, +0, I
S = Number of AND inputs of +0, +A, LS
T = Number of inputs of L P I

Clamped Inverters (basic inverter, level setter): Collector supply at 12 volts.

@ +0.1 v

0.72P + 0.95Q + 1.72R + 1.45S + 2.21T ≤ I − n (.03)

Rc = 910Ω, I = 0.0ma
Rc = 1.2k, I = 3.2ma
Rc = 2.4k, I = 8.6ma
Rc = 3.9k, I = 10.7ma

Unclamped Inverters (basic inverter): Collector supply at 6 volts.

@ +0.1 v

0.72P + 0.95Q + 1.72R + 1.45S + 2.21T ≤ I − n (.03)

Rc = 470Ω, I = 0.0ma
Rc = 620Ω, I = 3.4ma
Rc = 910Ω, I = 6.6ma
Rc = 1.8k, I = 10.2ma

Low-Power Inverters

@ +0.1 v

0.72P + 0.95Q + 1.71R + 1.45S + 2.21T ≤ I − n (.03)

Rc = 360Ω, I = 0.0ma
Rc = 470Ω, I = 8.5ma
Rc = 910Ω, I = 21.3ma
Rc = 1.2k, I = 24.6ma

Emitter Followers: Re is the emitter resistor.

1. First Stage @ −0.65 v

.76P + 1.67S ≤ I −n (.03)

Re = 5.6k, I = −0.15ma
Re = 3.0k, I = 1.45ma
Re = 2.2k, I = 2.70ma
Re = 1.82k, I = 3.68ma

2. Second Stage @ −0.75 v

.77P + 1.68S ≤ I − n (.03)

Re = 5.6k, I = −0.17ma
Re = 3.0k, I = 1.42ma
Re = 2.2k, I = 2.65ma
Re = 1.82k, I = 3.63ma

3. Third Stage ≤ @ −0.75 v

1.68S ≤ I −n (.03)

Re = 5.6k, I = −0.17ma
Re = 3.0k, I = 1.42ma
Re = 2.2k, I = 2.65ma
Re = 1.82k, I = 3.63ma

Basic Inverter

Input Current

Figure 79 shows the input current requirements for basic inverters and their associated diode networks.

Basic Inverter

Transistor State	Input Voltage	Input Current (ma)
ON	+6.84v to +2.7v	+1.52 max*
OFF	+0.7v to +0.1v	----------

* at +2.7v

Diode Networks

Diode Networks	Input Level	Input Voltage	Input Current (ma)
#I O or (OI)	+B -B	2.7v to 6.84v 0.1v to 0.33v	3.48*, 1.70**, 1.40*** ----
#II A of (AI)	+B -B	2.7v to 6.84v 0.1v to 0.33v	---- -0.95
#III O of (OAI)	+B -B	2.7v to 6.84v 0.1v to 0.33v	1.80*, 1.48**, 1.43*** ----
#IV A of (AOI)	+B -B	2.7v to 6.84v 01.v to 0.33	---- -1.72

* at 5.3 volts
** at 3.2 volts
*** at 2.7 volts

Figure 79. Basic Inverter Input Current

Delays and Transitions

Figure 80 shows the turn-on and turn-off delays of basic inverter circuits for sample input transitions. Figure 81 shows turn-on transition times with an input rise time of 80 ns. Refer to Figures 82 through 93 for basic inverter delays and transitions under other input conditions.

Available Output Current

The available negative current from a basic inverter is shown in Figure 94. Available positive current is shown in Figure 95.

Marginal Checking

The basic inverter is marginally checked by varying the −12M supply to −9v and −15v. The results of the check should be within the following limits for a circuit in normal operating condition:

1. With −12M supply at −9 volts.
   a. The increase in turn-off delay $\leq$ 30 ns
   b. The increase in turn-off transition $\leq$ 50 ns
   c. The decrease in turn-on delay $\leq$ 20 ns
   d. The decrease in turn-on transition $\leq$ 30 ns
2. With −12M supply at −15 volts.
   a. The decrease in turn-off delay $\leq$ 30 ns
   b. The decrease in turn-off transition $\leq$ 40 ns
   c. The increase in turn-on delay $\leq$ 20 ns
   d. The increase in turn-on transition $\leq$ 30 ns

AND Logical Low Power Inverter (+AIP)

Input and Output Current

Figure 96 shows input and output currents of the AND logical low power inverter (AND LLPI).

Delays and Transitions

Figure 97 gives the turn-on and turn-off delays of the AND LLPI for sample input rise and fall transitions. Refer to Figures 98 and 99 for turn-on and turn-off delays under other input conditions. Figures 98 and 100 give the circuit fall and rise transition times.

Marginal Checking

The AND LLPI is marginally checked by varying the −12M supply to −9v and −15v. The results of the check should be within the following limits for a circuit in normal operating condition:

1. With −12M supply at −9 volts.
   a. The increase in turn-off delay $\leq$ 15 ns
   b. The increase in turn-off transition $\leq$ 15 ns
   c. The decrease in turn-on delay $\leq$ 10 ns
   d. The decrease in turn-on transition $\leq$ 10 ns
2. With −12M supply at −15 volts.
   a. The decrease in turn-off delay $\leq$ 15 ns
   b. The decrease in turn-off transition $\leq$ 15 ns
   c. The increase in turn-on delay $\leq$ 10 ns
   d. The increase in turn-on transition $\leq$ 10 ns

Emitter Follower Chains

Input and Output Voltage and Current

Figure 101 gives data on the voltage levels and currents into and out of each stage of an emitter follower chain.

Delays and Transitions

Figure 102 shows the delays and transition times of emitter follower chains.

Binary Trigger

Input Requirements

The binary trigger must be driven by a clamped inverter or level setter. Figure 103 shows the sources that can be used to drive the AC *inputs*. The maximum rise transition from these driving sources is shown in Figure 104.

The DC inputs require 0.70 ma and the minimum pulse width for these inputs is 150 ns.

Delays and Transitions

Figure 105 shows the binary trigger delays and transition times.

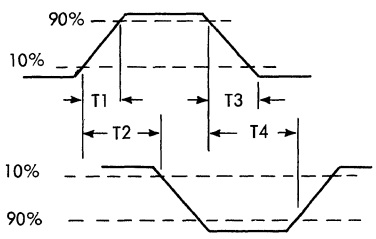
3 Volt Input Swing

Circuit	Input Rise or Fall Time (ns)	Turn-On Delays (ns)		Turn-Off Delays (ns)	
		Min	Max	Min	Max
Basic Inverter	20	20	80	10	94
	40	25	90	20	110
	60	31	100	30	125
	80	36	110	40	140
	120	46	130	80	175
OR - Inverter	20	20	80	10	76
	40	25	90	20	90
	60	31	100	30	105
	80	36	110	40	120
	120	46	130	60	155
AND - Inverter	20	22	74	42	58
	40	27	84	45	80
	60	31	93	47	102
	80	36	102	50	122
	120	45	120	54	152
AND - OR - Inverter	20	36	91	23	76
	40	38	100	28	90
	60	40	109	33	105
	80	42	118	38	120
	120	46	136	48	155
OR - AND - Inverter	20	13	82	23	64
	40	19	94	25	80
	60	24	107	27	98
	80	30	120	30	117
	120	41	144	34	155

6 Volt Input Swing

Circuit	Input Rise or Fall Time (ns)	Turn-On Delays (ns)		Turn-Off Delays (ns)	
		Min	Max	Min	Max
Basic Inverter	20	12	28	30	108
	40	16	38	40	122
	60	20	48	50	136
	80	25	58	60	150
	120	35	78	80	186
OR - Inverter	20	8	28	25	96
	40	12	38	34	110
	60	16	48	43	124
	80	20	58	52	138
	120	27	78	70	178
AND - Inverter	20	18	44	34	58
	40	20	47	48	84
	60	22	51	62	110
	80	23	55	76	136
	120	25	60	104	186
AND - OR - Inverter	20	16	44	25	74
	40	16	49	34	92
	60	16	54	42	110
	80	17	59	50	128
	120	18	70	68	165
OR - AND - Inverter	20	14	61	25	62
	40	15	66	35	84
	60	16	71	45	106
	80	17	75	55	128
	120	20	83	75	172

MEASUREMENT TECHNIQUES



T1 = Rise Transition (Turn - On)
T2 = Turn - On Delay
T3 = Fall Transition (Turn - Off)
T4 = Turn - Off Delay

Figure 80. Delays for Sample Input Transitions (Basic Inverter)

Circuit	Input Voltage*	Turn-On (Fall) Transition (ns)	
		Min	Max
Basic Inverter	3	25	110
OR - Inverter	3	25	120
AND - Inverter	3	25	110
AND - OR - Inverter	3	25	110
OR - AND - Inverter	3	25	110
Basic Inverter	6	20	50
OR - Inverter	6	20	50
AND-Inverter	6	20	80
AND-OR-Inverter	6	20	70
OR-AND-Inverter	6	20	80

*Input rise at 80 ns

Figure 81. Turn-On (Fall) Transitions with 80 ns Input Rise

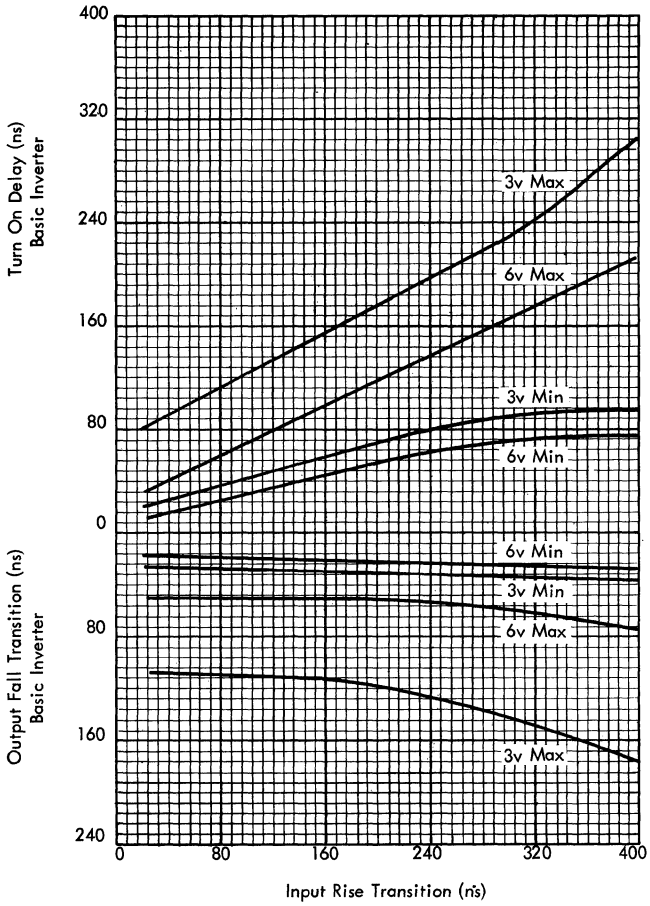


Figure 82. Turn-On Delay and Fall Transition of Basic Inverter

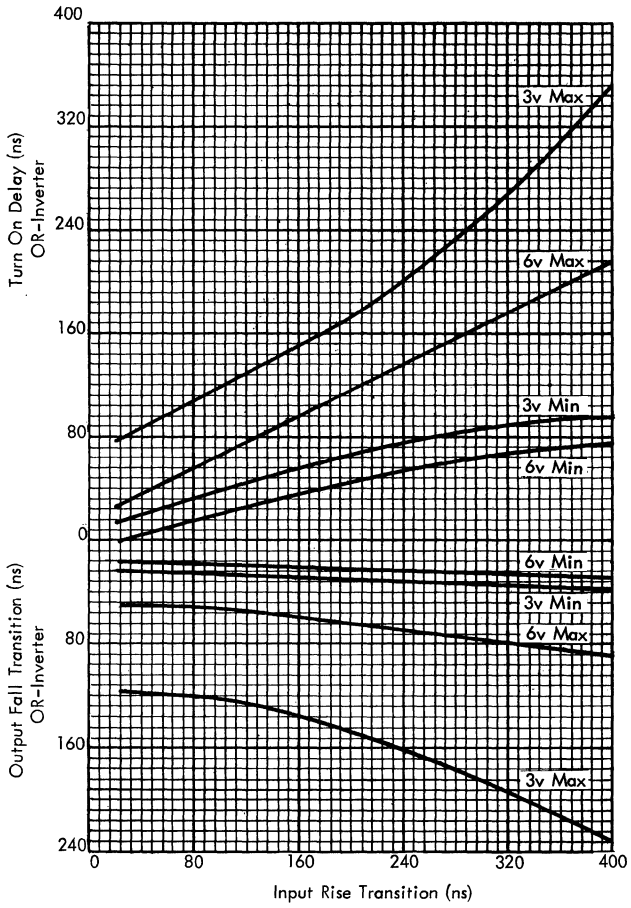


Figure 83. Turn-On Delay and Fall Transition of OR Inverter

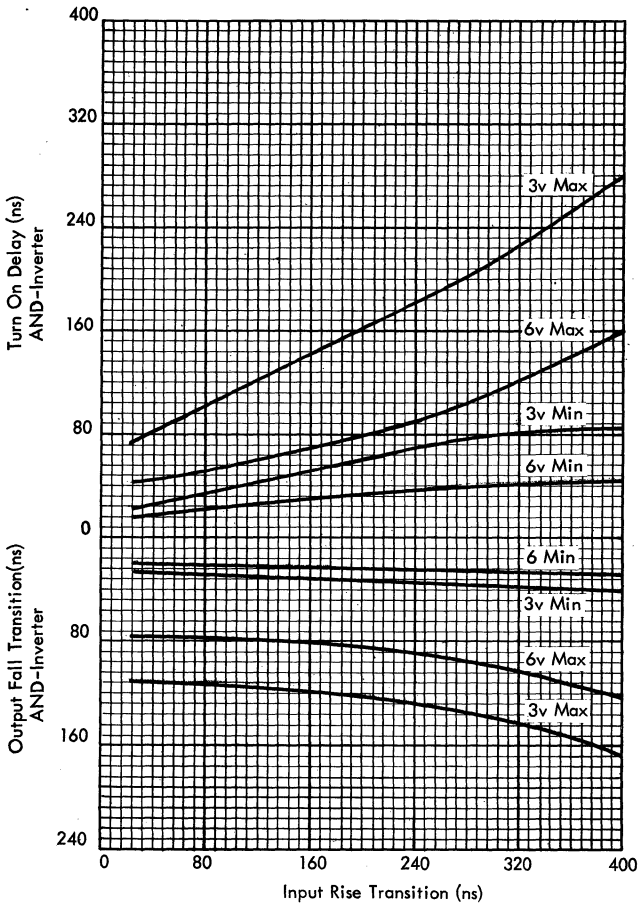


Figure 84. Turn-On Delay and Fall Transition of AND Inverter

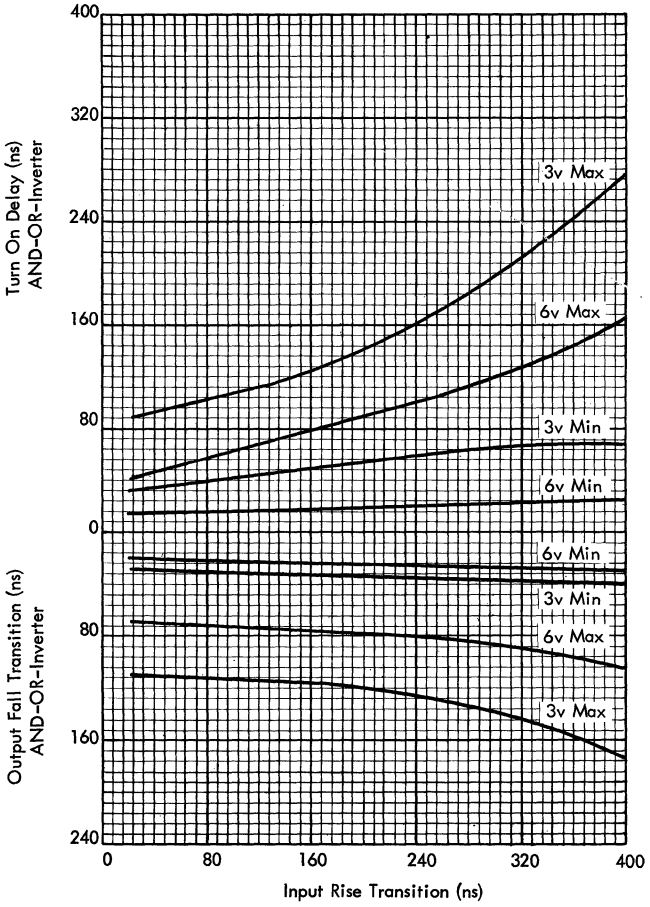


Figure 85. Turn-On Delay and Fall Transition of AND-OR Inverter

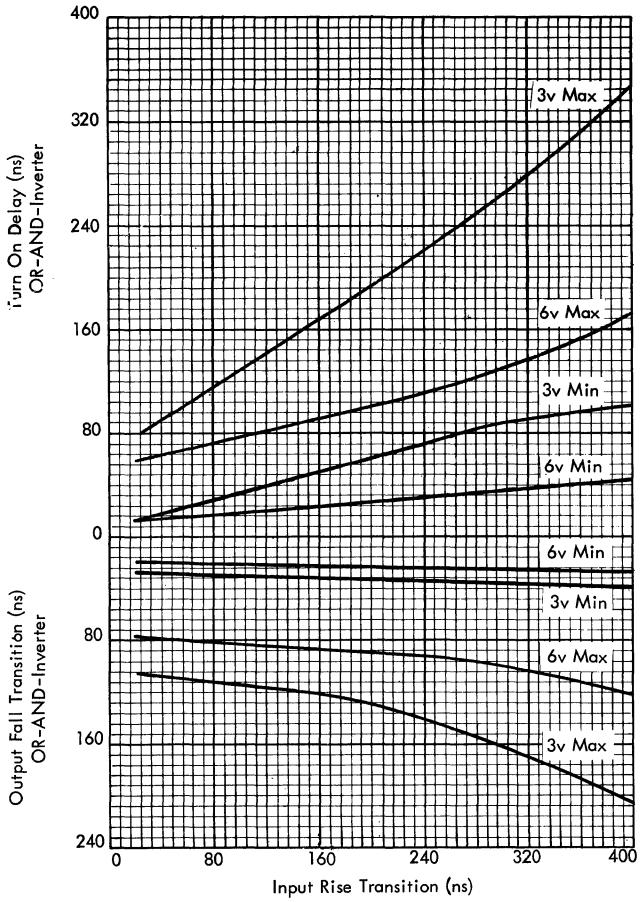


Figure 86. Turn-On Delay and Fall Transition of OR-AND Inverter

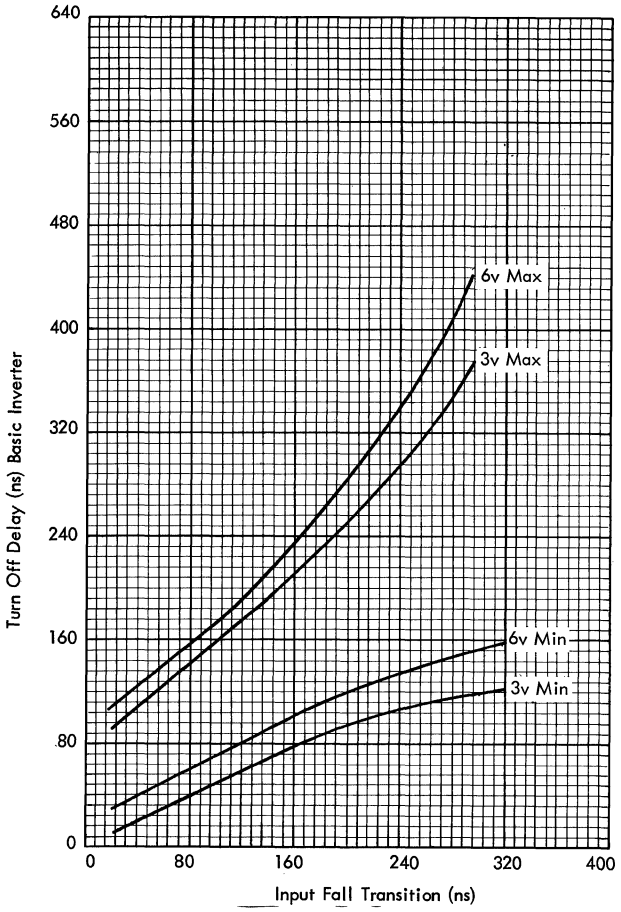


Figure 87. Turn-Off Delay of Basic Inverter

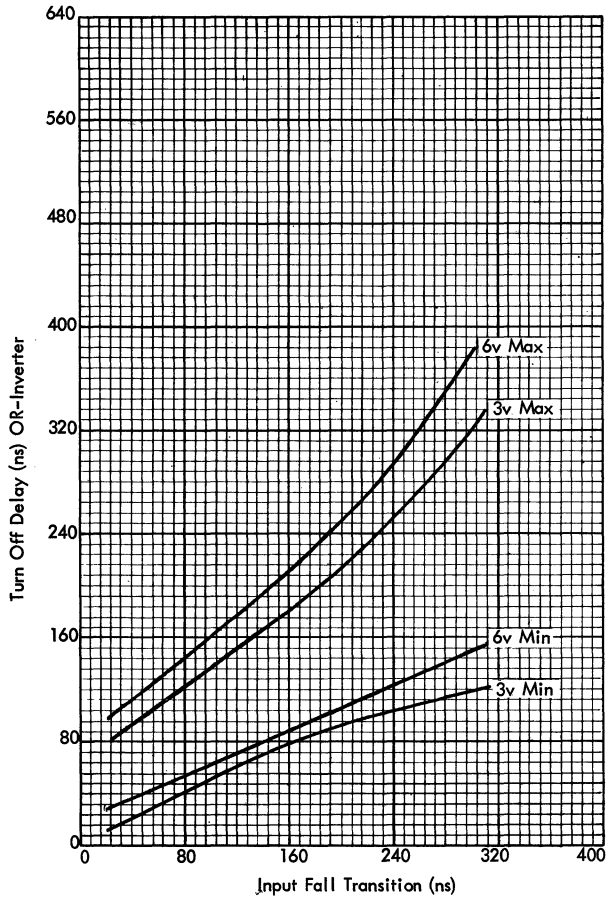


Figure 88. Turn-Off Delay of OR Inverter

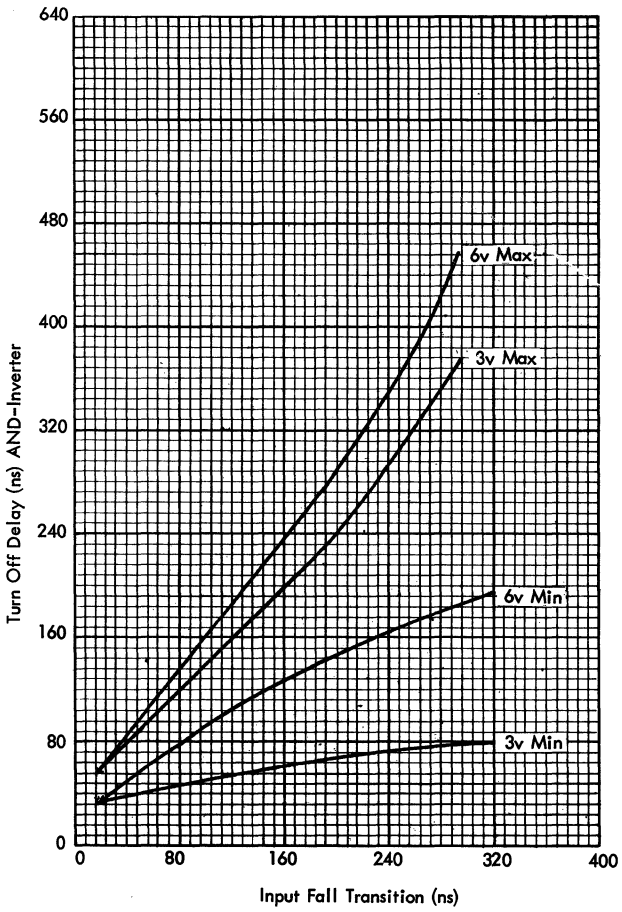


Figure 89. Turn-Off Delay of AND Inverter

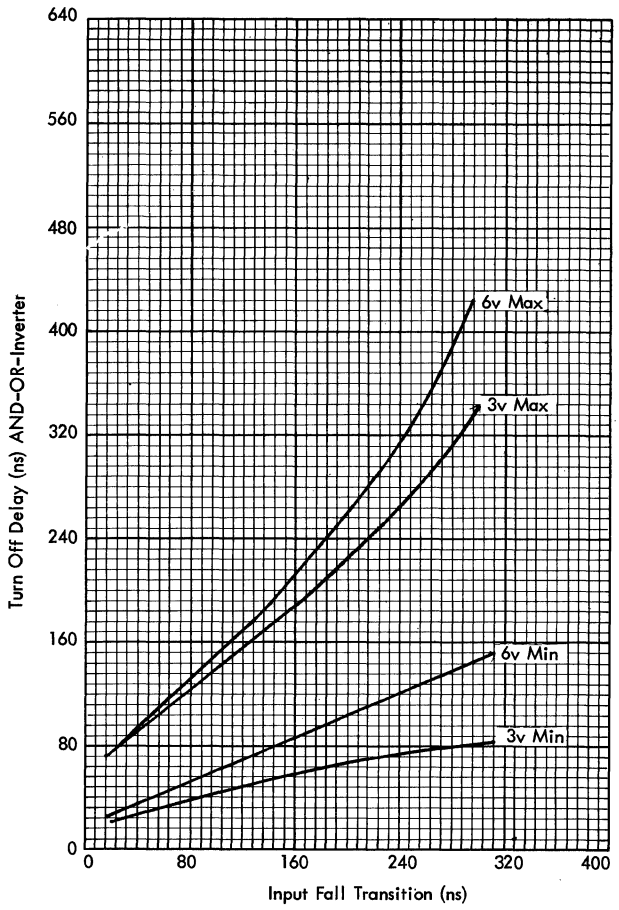


Figure 90. Turn-Off Delay of AND-OR Inverter

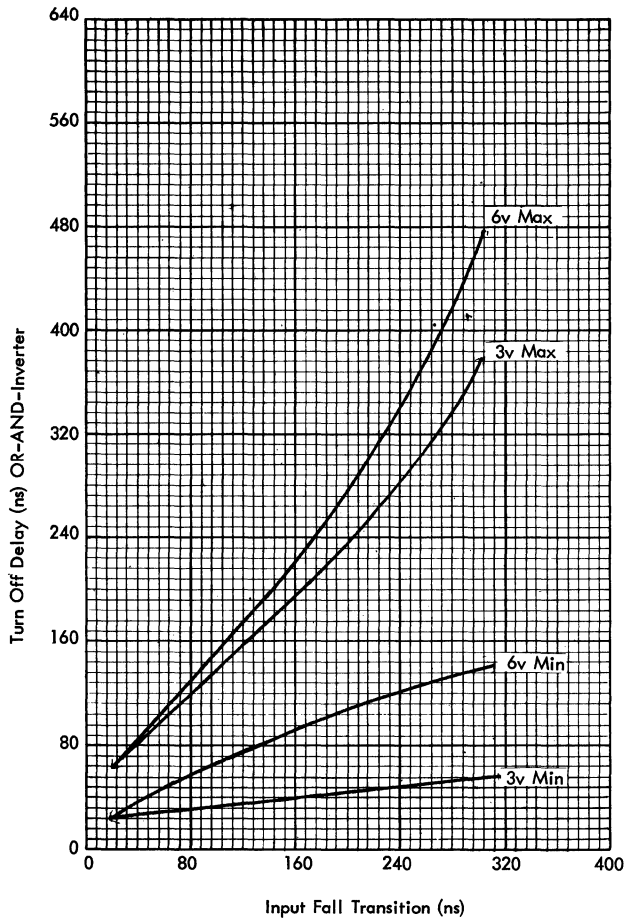
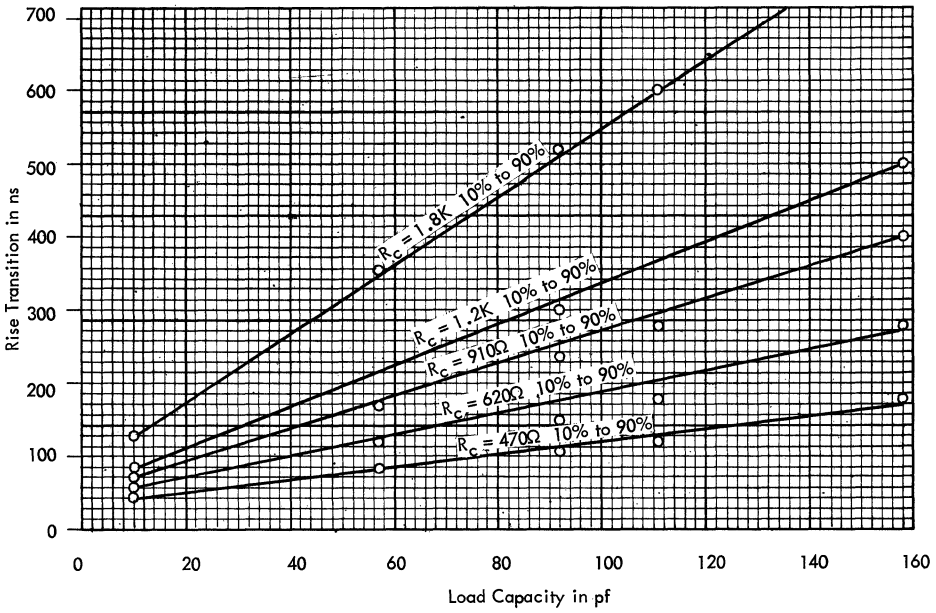


Figure 91. Turn-Off Delay of OR-AND Inverter



Load	Equivalent Capacity (pf)	
	Vc = 12 Volts	Vc = 6 Volts
Low Power Inverter 2	4	10
AND-OR-Inverter	6	20
AND-Level Setter	6	20
AND-Inverter	6	20
AND-Emitter Follower	10	20
Basic Inverter	4	6
OR-Inverter	4	6
OR-AND-Inverter	20	30
OR-AND-Level Setter	20	30
OR-AND-Emitter Follower	20	

Figure 92. Output Rise Transition of Unclamped Basic Inverter

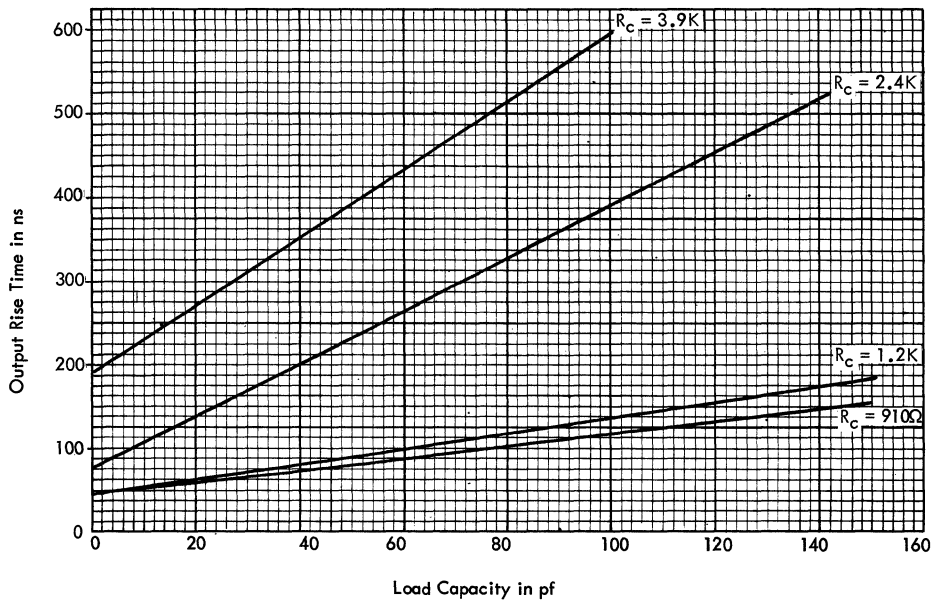


Figure 93. Output Rise Transition of Clamped Basic Inverter

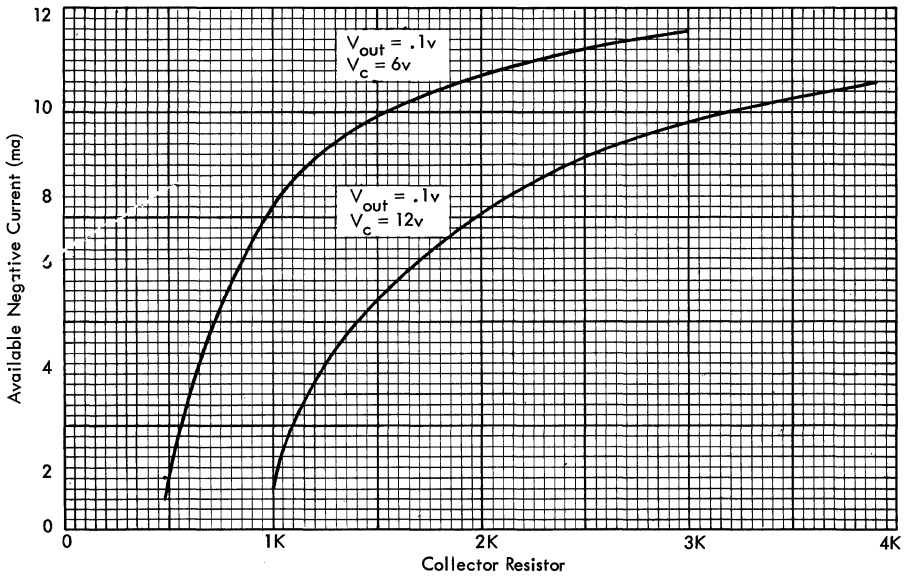


Figure 94. Available Negative Current from a Basic Inverter

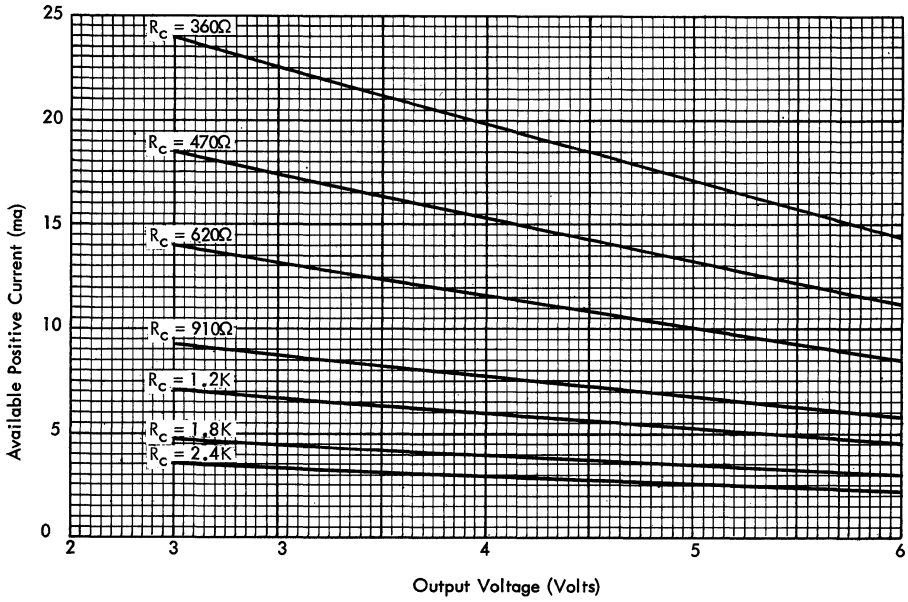
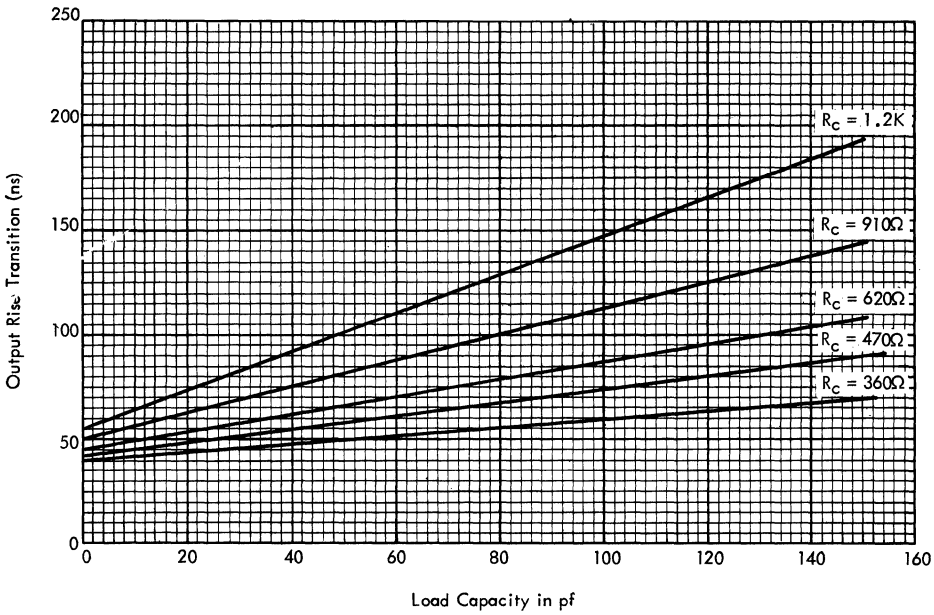


Figure 95. Available Positive Current from a Basic Inverter



Load	Equivalent Capacity (pf)	
	V_c = 12 volts	V_c = 6 volts
Low Power Inverter 2	4	10
AND-OR-Inverter	6	20
AND-Level Setter	6	20
AND-Inverter	6	20
AND-Emitter Follower	10	20
Basic Inverter	4	6
OR-Inverter	4	6
OR-AND-Inverter	20	30
OR-AND-Level Setter	20	30
OR-AND-Emitter Follower	20	

Wire Capacity is 1.2 pf/in.
Oscilloscope Capacity is about 12 pf.

Figure 100. Output Rise Transition of AND LLPI

Input Voltage Requirements

	Stage 1	Stage 2	Stage 3
"Up" Level = +B =	5.80v to 6.84	4.77v to 6.14v	3.95v to 6.14v
"Down" Level = -B =	0.10v to +0.33v	-0.65v to 0.48v	-0.75v to 0.63v

Output Voltage Requirements

	Stage 1	Stage 2	Stage 3
"Up" Level = +B =	4.77v to 6.14v	3.95v to 6.14v	3.20v to 6.14v
"Down" Level = -B =	-0.65v to 0.48v	-0.75v to +0.53v	-075v to 0.78v

Input Current

Transistor State	Stage	Section	Input Voltage	Input Current (ma) Max
ON	1	OR AND	6.30 5.60	1.81 -0.58
	2	OR AND	6.14 4.77	1.79 -0.63
	3	OR AND	6.14 3.95	1.78 -0.67
OFF	1	OR AND	0.33 0.10	1.28 -0.90
	2	OR AND	0.43 -0.65	1.29 -0.94
	3	OR AND	0.63 -0.75	+1.31 -0.95

Output Current

Transistor State	Max DC Level Shift	Min Output Voltage per Stage		Output Current, Min (ma)			
		Stage	Voltage	Re = 5.6K	Re = 3.3K	Re = 2.2K	Re = 1.82K
ON	6.14v to 3.20v	1 2 3	4.77 3.95 3.20	11.5 11.0 6.39	8.71 8.32 3.84	6.51 6.22 1.84	4.78 4.58 0.27
OFF	0.78v to -0.75v	1 2 3	-0.65 -0.75 -0.75	0.15 0.17 0.17	-1.45 -1.42 -1.42	-2.70 -2.65 -2.65	-3.68 -3.63 -3.63

Figure 101. Emitter Follower Input and Output Voltage and Current

Positive Loading

	Emitter Resistor		Input Transition (ns)	Emitter Follower Output Transition (ns)	Delay Worst Case (ns)
Chain of Three Emitter Followers with identical emitter resistors	5.6K	Turn-On Turn-Off	<100 < 80	160 500	225 480
	3.0K	Turn-On Turn-Off	<100 < 80	150 225	170 250
	2.2K 1.82K	Turn-On Turn-Off	<100 < 80	140 140	150 160
Chain of Two Emitter Followers	5.6K	Turn-On Turn-Off	<100 < 80	160 500	200 470
	3.0K	Turn-On Turn-Off	<100 < 80	150 225	135 180
	2.2K 1.82K	Turn-On Turn-Off	<100 < 80	140 140	115 130
Chain of One Emitter Follower	5.6K	Turn-On Turn-Off	<100 < 80	150 270	140 200
	3.0K	Turn-On Turn-Off	<100 < 80	130 150	115 140
	2.2K 1.82K	Turn-On Turn-Off	<100 < 80	125 100	110 140

Negative Loading

	Emitter Resistor		Input Transition (ns)	Emitter Follower Output Transition (ns)	Delay Worst Case (ns)
Chain of Three Emitter Followers	Stages 1 and 2 1.82K Stage 3 5.6K	Turn-On Turn-Off	<100 < 80	160 240	125 235
Chain of Two Emitter Followers	Stage 1 1.82K Stgge 2 5.6K	Turn-On Turn-Off	<100 < 80	160 200	100 180
Chain of One Emitter Follower	2.2K	Turn-On Turn-Off	<100 < 80	160 150	100 140

Figure 102. Emitter Follower Delays and Transitions

Source (All Clamped)	Allowed Input to Source	Allowed Additional Loading at Source	Maximum Number of Triggers Driven from Source*	Maximum Fall Transition at Source (ns)
Trigger Inverter R_c = 680 Ω , 820 Ω 1.2K, 1.8K	------	Normal Complement of + and - Loads	1	125
Trigger Inverter R_c = 1.8K	------	+ Only	2	125
Basic Inverter OI or I R_c = 910 Ω 1.2K, 2.4K	Restricted $\Delta v \geq 0.33$ to 5.76v at $\leq$ 120 ns	Normal Complement of + and - Loads	1	55
			2	65
			3	95
Basic Inverter OI or I R_c = 1.2K	Same Restriction as Above	+ Only	4	125
Basic Inverter any Input Network R_c = 1.2K	Restricted $\frac{dv}{dt} \geq \frac{5.76 - 0.33v}{120\ ns}$	None	1	125
Level Setter Any Input Network R_c = 1.2K	Normal i.e.; $\frac{dv}{dt} \geq \frac{3.2 - 0.78v}{120\ ns}$	None	1	125
Low Power Inverter R_c = 360 Ω	Normal ie $\Delta v \geq 0.33$ to 5.76v at 120 ns	Normal + Complement	1	80
			2	125
Low Power Inverter R_c = 910Ω	Normal as Above	Normal + and - Complement	1	80
			2	125
		Normal + Complement Only	1	55
			2	70
			3	95
			4	125

* (a) A "1/2 load" is one trigger input when trigger is used as an R-S trigger
(b) A "1 load" is one trigger connected as a binary counter or two separate R-S inputs.
(c) A "2 load" is two binary triggers, etc.

Figure 103. Binary Trigger Driving Sources

Two, or Less, Trigger Loads *

Source Collector Resistor	Maximum Rise Transition at Sources (ns)								
	Maximum Additional Capacitive Load								
	0 pf			50 pf			130 pf		
	No. of Triggers Driven			No. of Triggers Driven			No. of Triggers Driven		
	1/2	1	2	1/2	1	2	1/2	1	2
1.8K No + Load	200	390	780	290	460	900	410	600	980
1.8K + Loaded	580	930	1560	710	1060	1680	820	1140	1700
1.2K No + Load	130	200	480	150	250	540	240	340	640
1.2K + Loaded	390	700	1200	440	760	1270	570	840	1400
910Ω No + Load	130	140	350	130	160	360	170	200	420
910Ω + Loaded	250	510	870	280	540	900	370	620	960
820Ω No + Load	120	130	300	120	150	330	160	200	380
820Ω + Loaded	230	440	780	270	510	840	360	540	910
680Ω No + Load	120	120	220	120	140	240	140	170	300
680Ω + Loaded	150	370	680	190	400	700	280	470	770
360Ω No + Load	110	120	130	120	140	170	110	120	150
360Ω + Loaded	150	270	490	160	290	500	170	310	510
2.4K No + Load	240	560	1100	350	650	1200	530	820	1330
2.4K + Loaded	640	1100	2050	800	1280	2120	1280	1520	2160

More Than Two Trigger Loads *

Source Collector Resistors	Maximum Rise Transition At Sources (ns)	
	Number of Triggers Driven (Additional Capacitance ≤ 50 pf)	
	3	4
910Ω No + Load	730	940
910Ω + Loaded	1430	1760
1.2K No + Load	970	1350
1.2K + Loaded	1760	2200
1.8K No + Load	1430	----
1.8K + Loaded	2700	
2.4K No + Load	1980	3200
2.4K + Loaded	3700	4600

*(a) A "1/2 load" is one trigger input when trigger is used as an R-S trigger
(b) A "1 load" is one trigger connected as a binary counter or two separate R-S inputs.
(c) A "2 load" is two binary triggers, etc.

Figure 104. Maximum Input Rise Transition

Turn-On Delay

AC Input

Turn-On Delay (ns)	
Minimum	Maximum
36	190

DC Reset, Set Drive

Input Rise Time (ns)	Turn-On Delay (ns)
	Maximum
120	250

Turn-Off Delay

AC Input

Input Fall Time (ns)	Turn-Off Delay (ns)	
	Minimum	Maximum
<50	10	86
50	22	86
90	28	98
125	34	124

DC Reset, Set Drive

Input Rise Time (ns)	Turn-Off Delay (ns)
	Maximum
120	180

Turn-On Transition (AC and DC Inputs). No trigger loads, equivalent load capacity <100 pf.

Minimum	20 ns
Maximum	115 ns

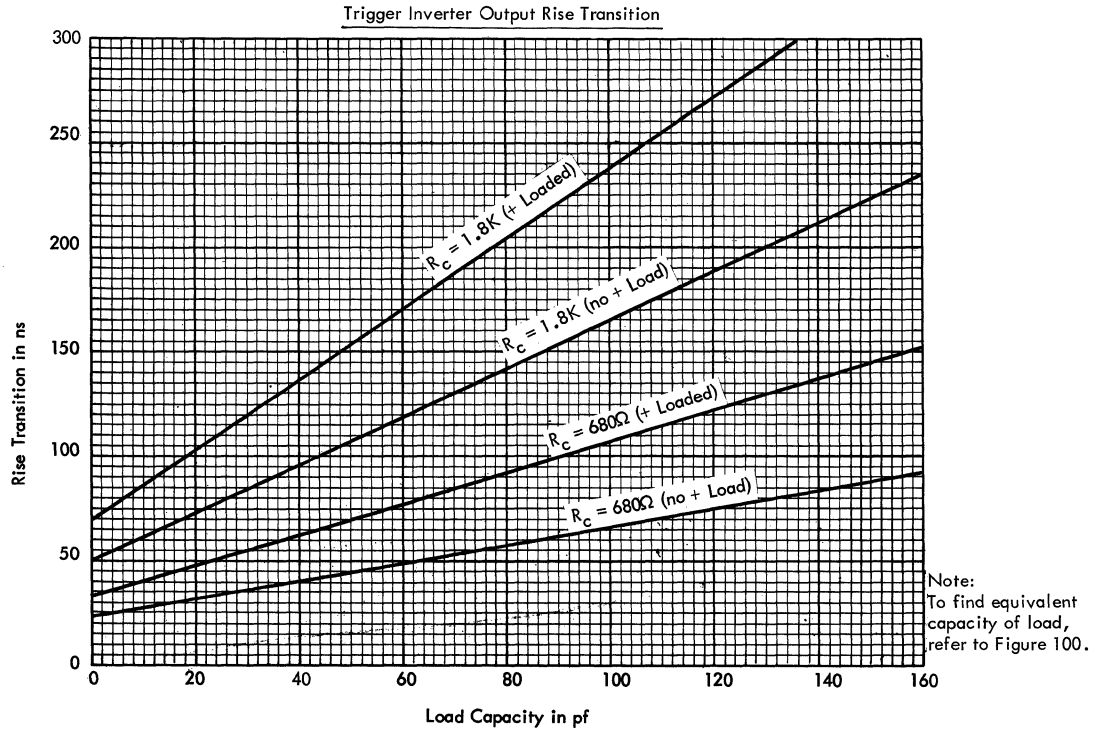


Figure 105. Binary Trigger Delays and Output Transitions

NOTE: Special Circuits are not listed, refer to the CE manuals for the machine using these circuits.

H CODE	CIRCUIT TITLE	FIGURE	PAGE
H05AF	Basic Inverter, 1.2K, Clamped	28	19
H05AG	Basic Inverter, 1.8K, Clamped	28	19
H05AH	Basic Inverter, 2.4K, Clamped	28	19
H05AI	Level Setter, No Load	33	23
H05AJ	Level Setter, 910 ohm, Clamped	33	23
H05AK	Level Setter, 1.2K, Clamped	33	23
H05AL	Level Setter, 2.4K, Clamped	33	23
H05AM	Converter, N to B, 620 ohm, Unclamped	62	52
H05AN	Converter, N to B, 910 ohm, Unclamped	62	52
H05AO	Converter, N to B, 470 ohm, Unclamped	62	52
H05AP	Converter, N to B, 910 ohm, Clamped	62	52
H05AQ	Converter, N to B, 2.4K, Clamped	62	52
H05AR	Converter, P to B, 470 ohm, Unclamped	62	52
H05AS	Converter, P to B, 620 ohm, Unclamped	62	52
H05AT	Converter, P to B, 910 ohm, Unclamped	62	52
H05AU	Converter, P to B, 910 ohm, Clamped	62	52
H05AV	Converter, P to B, 1.2K, Clamped	62	52
H05AW	Converter, P to B, 2.4K, Clamped	62	52
H05AX	Standard Interface Line Terminator, 470 ohm, Unclamped	58	48
H05AY	Standard Interface Line Terminator, 620 ohm, Unclamped	58	48
H05AZ	Standard Interface Line Terminator, 910 ohm, Unclamped	58	48
H05BA	Standard Interface Line Terminator, 1.8K, Unclamped	58	48
H05BB	Standard Interface Line Terminator, 910 ohm, Clamped	58	48
H05BC	Standard Interface Line Terminator, 1.2K, Clamped	58	48
H05BD	Standard Interface Line Terminator, 2.4K, Clamped	58	48
H05BE	Converter, N to B, 1.2K, Clamped	62	52
H05BF	Converter, B to P	61	51
H05BG	Converter, B to N	61	51
H05BH	Binary Tgr Inverter, 680 ohm, Clamped	37	27
H05BI	Binary Tgr Inverter, 820 ohm, Clamped	37	27
H05BN	Converter, B to E	60	50
H05BO	Converter, E to B, 1.2K, Clamped	60	50
H05BQ	Gated Line Terminator, 910 ohm, Clamped	56	46
H05BT	Delay Line Terminator, No Load	57	47
H05BU	Delay Line Terminator, 390 ohm, Unclamped	57	47
H05BV	Delay Line Terminator, 910 ohm, Clamped	57	47
H05BW	Data Set Line Terminator	59	49
H05BY	Shift Cell Driver	44	34
H05CN	Converter, E to B, 1.2K, Clamped	60	50
H05CS	Converter, E to B, 1.2K, Clamped	60	50
H06AE	Converter, S to B	63	53
H06AF	Converter, B to S	63	53
H06AI	Converter, E to B, Gated, Not-Invert	60	50
H06AJ	Converter, B to N, Non-Invert	61	51
H06AM	Converter, P to B, Non-Invert	62	52

H CODE	CIRCUIT TITLE	FIGURE	PAGE
H10AA	Standard Interface Line Driver	58	48
H10AD	Gated DOT OR Line Driver	56	46
H10AG	93-ohm Line Driver	57	47
H10AI	125-300 ma Relay Driver	52	42
H11AE	Data Set Line Driver	59	49
H15AA	+OR Logical Low Power Inverter, 200 ohm, Unclamped	29	20
H15AB	+OR Logical Low Power Inverter, 360 ohm, Clamped	29	20
H15AC	+OR Logical Low Power Inverter, 620 ohm, Unclamped	29	20
H15AD	+OR Logical Low Power Inverter, 910 ohm, Clamped	29	20
H15AE	+AND Logical Low Power Inverter, No Load	30	21
H15AF	+AND Logical Low Power Inverter, 360 ohm, Clamped	30	21
H15AG	+AND Logical Low Power Inverter, 910 ohm, Clamped	30	21
H15AH	+AND Logical Low Power Inverter, 470 ohm, Clamped	30	21
H15AI	Negative Latch, Inverter, 360 ohm	40	31
H15AK	Negative Latch, Inverter, 910 ohm	40	31
H15AL	Negative Latch, Level Setter, 360 ohm	40	31
H15AM	Negative Latch, Level Setter, 470 ohm	40	31
H15AN	Negative Latch, Level Setter, 910 ohm	40	31
H15AP	+AND Logical Low Power Inverter, 1.2K, Clamped	30	21
H15AQ	75 ma Relay Driver	52	42
H15AR	+AND Logical Low Power Inverter, 720 ohm, Clamped	30	21
H15AU	+AND Powered Inverter, 133 ohm	34	24
H15AV	+AND Powered Inverter, 180 ohm	34	24
H15AW	+AND Powered Inverter, 510 ohm	34	24
H16AA	700 ma Relay Driver	52	42
H20AB	Binary Tgr for Both Output Inverters	36	26
H20AC	Binary Tgr for One Output Inverter	36	26
H20AD	Binary Tgr Inverter, 1.2K, Clamped	37	27
H20AE	Binary Tgr Inverter, 1.8K, Clamped	37	27
H20AI	AC Tgr	39	29
H20AJ	Shift Cell, Off Output	43	33
H20AK	Shift Cell, Both Outputs	43	33
H20AL	Shift Cell, On Output	43	33
H20AN	Binary Tgr for Both Output Inverters	36	26
H20AS	Control Tgr	38	28
H21AA	Pulse Former Single-Shot, 1.2K, Clamped	50	41
H21AB	Pulse Former Single-Shot, 910 ohm, Clamped	50	41
H21AC	Pulse Former Single-Shot, 2.4K, Clamped	50	41
H21AD	Pulse Former Single-Shot, 1.2K, Unclamped	50	41
H21AE	Variable Single-Shot, 2.5 μs to 2 μs	46	36
H21AF	Variable Single-Shot, 900 μs to 1190 μs	46	36
H21AG	Variable Single-Shot, 350 ns to 115 ms	47	37
H21AH	Variable Single-Shot, 2.5 μs to 1.7 sec	47	37
H21AI	Variable Holdover Single-Shot	48	38
H21AJ	Pulse Former Single-Shot, Internal Pulse Former	49	40

H CODE	CIRCUIT TITLE	FIGURE	PAGE
H22AG	2 mc Crystal-Controlled Osc	53	43
H22AI	2.25 mc Crystal-Controlled Osc	54	44
H22AJ	2.4 mc Crystal-Controlled Osc	54	44
H22AK	272 kc Crystal-Controlled Osc	53	43
H22AM	160 kc Crystal-Controlled Osc	53	43
H22AN	10 kc Crystal-Controlled Osc	53	43
H22AO	748 kc Crytsal-Controlled Osc	53	43
H22AP	612 kc Crystal-Controlled Osc	53	43
H22AQ	680 kc Crystal-Controlled Osc	53	43
H22AR	856 kc Gated Osc	55	45
H22AS	333 kc Gated Osc	55	45
H22AT	2.5 mc Crystal-Controlled Osc	53	43
H22BA	2 mc Crystal-Controlled Osc	54	44
H22BB	128 kc Crystal-Controlled Osc	54	44
H22BC	76.8 kc Crystal-Controlled Osc	53	43
H45AB	Delay Line, 620 ns, Var	57	47
H45AC	Delay Line, 1270 ns, Var	57	47

H CODE	CIRCUIT TITLE	FIGURE	PAGE
H55AA	15 ma Indicator Driver	51	41
H55AB	160 ma Light Driver	51	41
H55AC	15 ma Indicator Driver	51	41
H55AE	Gated Indicator Driver	51	41
H55AF	40 ma Indicator Driver	51	41
H60AA	Converter Integrator, −48v to B	64	53
H60AE	Converter, −48v to B	64	53
H60AF	Converter, −12v to B	64	53
H65AG	Pulse Generator	45	35
H66AA	Pulse Former, 400 ns	50	41
H66AB	Pulse Former, 1.7 μs	50	41
H66AC	Pulse Former, 45 μs	50	41
H66AD	Pulse Former, 200 ns	50	41
H66AE	Pulse Former, 1 μs	50	41
H66AF	Pulse Former, 300 ns	50	41
H66AG	Pulse Former, 500 ns	50	41
H66AH	Pulse Former, 10 μs	50	41

Input Current

Transistor State	Input Voltage	Input Current (ma)
ON	5.76v to 6.84v	------
OFF	0.1v to 0.33v	-2.21*

* at +0.1v

Output Current

Transistor State	Output Voltage	Output Current		
		R_c = 360	R_c - 470	R_c = 910
ON	0.1v to 0.33v	0	-8.5	-21.3
OFF	2.7v to 6.84v	13.8* 21.9** 23.4***	10.6* 16.8** 17.8***	5.46* 8.65** 9.23***

* at 6.3v
** at 3.2v
*** at 2.7v

Figure 96. Input and Output Current of the AND LLPI

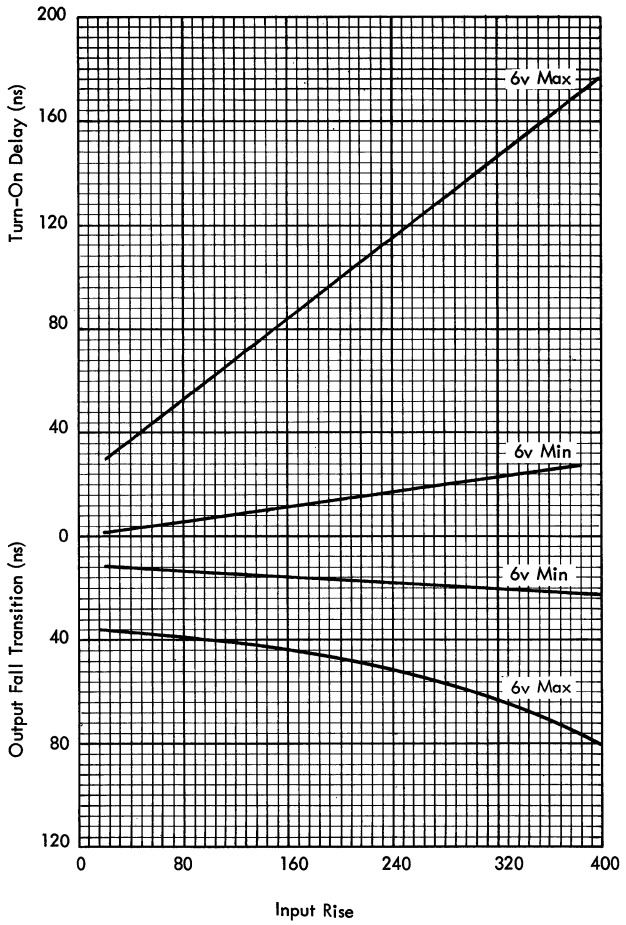


Figure 98. Turn-On Delay and Fall Transition of AND LLPI

Input Rise or Fall Time (ns)	Turn-On Delay (ns)		Turn-Off Delay (ns)	
	Min	Max	Min	Max
20	2	30	10	45
40	4	37	10	60
60	5	45	20	80
80	7	53	30	100
100	8	60	38	120

Figure 97. Sample Delays of the AND LLPI

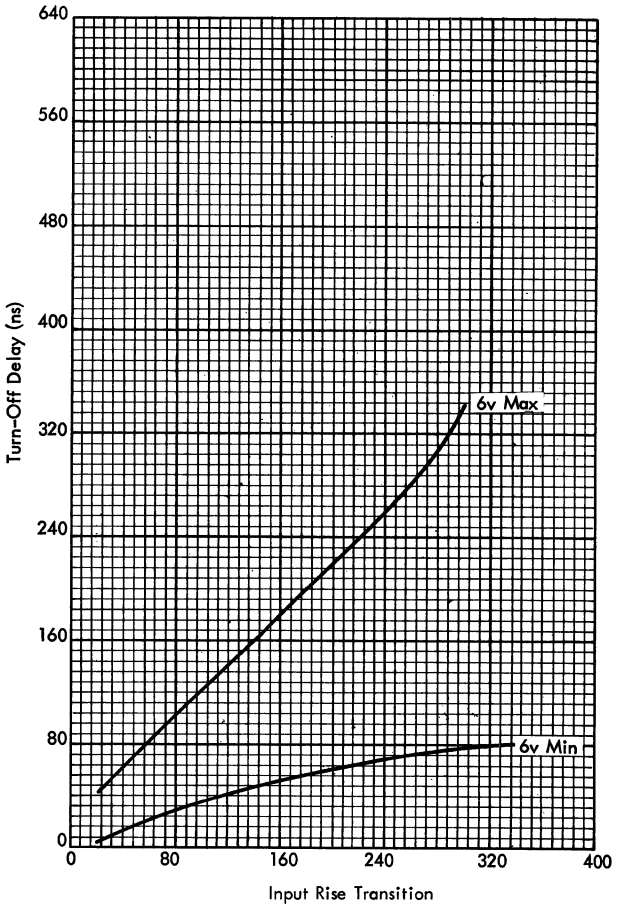
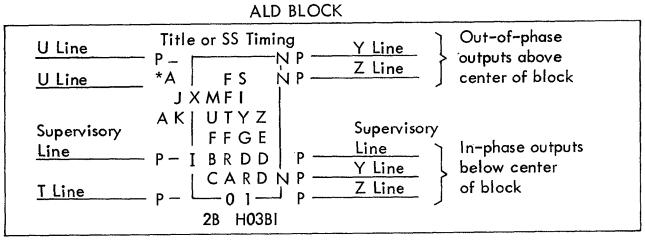


Figure 99. Turn-Off Delay of AND LLPI

Appendix C — ALD Reference Information

ALD BLOCK



FS - Functional symbol (up to four characters -A, -TO, SS, ---)
MFI - Machine feature index or special note (up to four characters)
UT - Line type in
YZ - Line type out
FF - Frame (01 - 99)
G - Sliding gate (A, B, C, D) or module (A, B, C, ---)
E - Engineering change level tag (A, B, C, ---)
B - Chassis (1 - 6) or swinging gate (1 - 8)
R - Chassis Row (A - K) or swinging gate column (A - F)
DD - Chassis column (01 - 28) or swinging gate row (01 - 26)
P - Card socket pin (single card:A-R; double, Stan-Pac, or twin:A-8)
*A - Edge Connector, Test Point given in Note A
JX - Shield lead connected to pin J (X = twisted pair; * = coaxial cable)
AK - Pin A backpanel wired to pin K
CARD - Card code
2B - Page coordinates
H03BI - For engineering use; block identification (circuit type)
01 - For engineering use; block configuration (01, 02, 03, ---)
N - When used means normal (not supervisory) output, load in this block.
I - One of six symbols:
- 3 - Third level input, load in this block
- ◊ - Third level input, load elsewhere
- S - Split level input, load in this block
- 2 - Split level input, load elsewhere
- C - Cascode level input, load in this block
- H - Cascode level input, load elsewhere

LINE LEVELS

Line Type	Ideal Swing (volts)	Down Levels (volts) Low	Down Levels (volts) High	Up Levels (volts) Low	Up Levels (volts) High	Application
B	0 to + 6	+ 0.1	+ 0.3	+2.7	+6.8	DDTL, Uncompensated
B	0 to + 6	+ 0.1	+ 0.3	+5.6	+6.8	DDTL, Compensated
B	0 to + 6	- 0.8	+ 0.8	+3.2	+6.8	DDTL, DE Chain
C	0 to 15 ma	- 4.1	- 0.3	+0.6	+3.1	Std Interface DL, DT
D	-2.5 to +2.5	- 5.0	- 0.7	+0.7	+5.0	DEFL
E	-6 to +6	- 25.0	- 3.0	+3.0	+25.0	EIA Std Data Sets
N	± from 0 ref	- 3.0	- 0.4	+0.4	+1.2	Alloy Current Sw
N	± from 0 ref	- 0.9	- 0.4	+0.4	+0.6	Diffused Current Sw
P	± from -6 ref	- 7.2	- 6.4	-5.6	-3.0	Alloy Current Sw
P	± from -6 ref	- 6.6	- 6.4	-5.6	-5.2	Diffused Current Sw
Q	0 to 40 ma	- 3.8	- 0.5*	+0.6	+2.4	DL and DT
R	0 to +12	- 0.4	+ 0.2	+5.6	+12.5	CTRL
S	-12 to 0	-12.5	- 5.6	-0.2	+0.4	CTRL
S	-12 to 0	-12.5	- 6.9	-0.5	0.0	SDTRL
S'	-6 to 0	- 6.9	- 5.9	-0.5	0.0	Clamped SDTDL and SDTRL (7074)
T	-6 to +6	- 6.2	- 0.7	+1.4	+6.2	CTDL
U	-12 to 0	-12.5	- 7.4	-5.3	+0.2	CTDL
V	Any					Special
W	# 0 to -48	-53.0	- 43.0	-2.0	0.0	Relays
X	-30 to +10	-60.0	- 18.3	+5.5	+40.0	Tubes
Y	-6 to 0	- 8.8	- 5.8	-0.7	-0.1	SDTDL
Z	-6 to +6	- 7.0	- 4.2	+3.0	+6.2	Magnetic Shift Cores

* High down level can go to +0.1 on some circuits
\# 0 to relay source voltage; typically, 0 to -48

NORMAL PIN ASSIGNMENTS FOR POWER SUPPLY VOLTAGES

Card Type	Gnd	-6v	+6v	-12v	+30v	+12M	-36v	-20v	+6M	+12v	-12M	+20v
All Single	J	K	L	M	N*	N*	P*	P*	Q*	Q*	R	
Double**	J&1	K	L	M	N*	N*	P*	P*	Q*	Q*	R	
Stan-Pac(7104)	1	2	3	4		5						
Stan-Pac(7302§)	J&1		5					6			8	7
Twin#	J&1		3	4	5*or7		6			5*	8	

* One of two voltages that may be on this pin
** Current switching circuits (1410, 7030, 7070, 7074, 7080, 7090, 7094)
§ Serial 12000 and above (DEFL circuits)
\# DDTL circuits (7040, 7044, 7640, 7710, 7750, 7908)

CURRENT SWITCHING SUPERVISORY LEVELS

Line Name	Ref	Down Levels* (volts) L	Down Levels* (volts) N	Down Levels* (volts) H	Up Levels* (volts) L	Up Levels* (volts) N	Up Levels* (volts) H
Third-Level N	0.0	- 2.0	- 1.6	- 1.2	+ 0.4	+ 0.5	+ 0.5
Third-Level P	- 6.0	- 6.5	- 6.5	- 6.4	- 4.8	- 4.4	- 4.0
Split-Level N	0.0	- 2.0	- 1.6	- 1.2	- 0.2	0.0	+ 0.2
Split-Level P	- 6.0	- 6.2	- 6.0	- 5.8	- 4.8	- 4.4	- 4.0
Cascode N (N')	+ 6.0	+ 5.0	+ 5.3	+ 5.6	+ 6.4	+ 6.5	+ 6.5
Cascode P (P')	-12.0	-12.5	-12.5	-12.4	-11.6	-11.3	- 7.0

* L - Low limit for typical circuits using this line type
* N - Nominal voltage level
* H - High limit for typical circuits using this line type

7070 SPECIAL CORE DRIVE LEVELS

Line Name	Down Levels (volts) Low	Down Levels (volts) Nom	Down Levels (volts) High	Up Levels (volts) Low	Up Levels (volts) Nom	Up Levels (volts) High
A Drive (ROD)	+ 1.1	+ 10.0	+ 17.9	+ 28.7	+ 30.0	+ 31.2
B Drive (RID)	- 6.2	- 6.0	- 5.2	+ 12.2	+ 17.0	+ 20.9
B Drive (DRID)	- 5.9	- 5.8	- 5.7	+ 10.8	+ 11.0	+ 11.9
C Drive (ROCD)	+ 6.4	+ 6.4	+ 7.2	+ 11.7	+ 12.0	+ 17.0

Note: This information is available on a pocket-size card, IBM Component Circuits Reference Card, Form 223-2596.

CUT ALONG LINE

COMMENT SHEET

DDTL COMPONENT CIRCUITS

CUSTOMER ENGINEERING MANUAL OF INSTRUCTION, FORM 223-2618

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1. Does this manual serve your needs?
2. Does the manual adequately explain all standard DDTL circuits?
3. Is some of the information unnecessary?
4. Was the introduction helpful?
5. Have you ever referred to the information in the Appendices?

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NOTE: Suggestions giving specific solutions, and intended for award consideration, should be submitted through the IBM Suggestion Plan.

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