Integrated Circuit Systems, Inc.

Data Book • June, 1995

ICS Product Data Book

ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.

ICS does not assume any liability arising out of or associated with the application or use of any product or integrated circuit or component described herein. ICS does not convey any license under its patent rights or the patent rights of others described herein. In the absence of a written or prior stated agreement to the contrary, the terms and conditions stated on the back of the ICS order acknowledgment obtain.

ICS makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose.

ICS products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any nuclear facility application, or for any other application in which the failure of the ICS product(s) could create a situation where personal injury or death may occur. ICS will not knowingly sell its products for use in such applications, and the buyer shall indemnify and hold harmless ICS and its officers, employees, subsidiaries, affiliates, representatives and distributors against all claims, costs, damages, expenses, tort and attorney fees arising out of directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ICS was negligent regarding the design or manufacture of the part.

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Using the ICS Data Book

The ICS Spring 1995 Data Book includes all of ICS's standard products in each of the following product lines: frequency timing generators, GENDACs,™ data and telecommunications, multimedia audio and video and QuickSaver® battery charge controllers. The manual is organized by product lines, which are further subdivided into product categories. Each product section includes an introduction, a product selection guide with applications information, data classification definitions and the pertinent data sheets for the ICS standard products within those categories.

Application notes for ICS's products are incorporated within the appropriate sections. General applications notes stand alone at the end of the chapter, while the more product-specific are located at the end of their respective data sheets. You can find the general application notes easily in the Alpha Numeric Index located on page A-3.

The individual data sheets include block diagrams with a package designation, pin descriptions, electrical characteristics, absolute maximum ratings and ordering information. Package dimensions are located in a separate section at the back of the book (Section K). The block diagram data notes the page on which the actual package drawing is located.

Other sections in the 1995 edition of the Data Book include a Table of Contents, Alpha Numeric Index, Ordering Information and Master Selection Guide (Section A), a description of our ASIC capabilities and Quality Assurance procedures (Section J) and a complete list of ICS's sales reps and distributors (Section L).

Product samples or demo boards can be obtained by contacting any of the sales reps or distributors. For further information, contact ICS Customer Service.

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Any errors in content can be directed to MarCom at the above address.

About ICS

Integrated Circuit Systems, Inc. designs, develops and markets standard and application specific integrated circuits utilizing mixed analog/digital technology. Founded in 1976 to provide custom IC designs and product sourcing services to OEMs, ICS created its own sophisticated design tools, analog and digital cell libraries and quality assurance testing methods. In 1988, these unique tools and mixed signal design capabilities enabled ICS to create the first commercially viable video timing generator using advanced frequency synthesis technology. The ICS1394 pioneered the transition from multiple crystal oscillators to a single IC and emerged as the industry standard for producing the high frequency video dot timing function in IBM-compatible personal computers.

ICS has extended its knowledge of frequency timing into new products for PC multimedia sound and video. These include products that synchronize PC video images with live or recorded television video, and products that create real, digitized sound. To expand on the capabilities of its PC sound/video design expertise, ICS formed the Multimedia Components Division in July, 1993 and merged with Turtle Beach Systems, Inc., a provider of PC-based hardware and software products for professional-quality sound generation and editing in multimedia applications.

Additionally ICS has leveraged its core technology into the communications arena, designing a Bellcore-compliant clock generation and recovery circuit and parlaying its technology to create a family of highly integrated, physical layer transceivers for Fast Ethernet/FDDI, ATM and SONET data rates.

ICS is meeting the increasing demand for controlled, rapid NiCd or NiMH battery recharging for laptop and notebook computers with a family of power management integrated circuits. Using inflection point termination technology to fast charge batteries prolongs battery life and eliminates the memory effect. In fact, NASA has judged ICS's battery charging IC the safest of the new rapid-charge products.

Our goal at ICS is to produce and deliver products of exceptional quality and reliability. To achieve that goal, we control every phase of manufacturing and quality assurance at all locations. We dedicate our efforts to meeting your technical expectations, your delivery deadlines and your competitive pricing needs. We strive to achieve a total quality process that provides customers with products and services that meet or exceed specification and performance requirements, quality expectations and support needs before and after delivery.

Our unique partnerships with international experts in wafer fabrication and assembly provide our customers with the highest quality and performance in each integrated circuit chip. We routinely produce both application specific integrated circuits (ASICs) and customized versions of our standard masks.

We are confident that ICS can provide you with the optimum IC solutions, outstanding customer service and dedication to quality to suit your needs.

Dr. David Sear, President and CEO

Integrated Circuit Systems . . . Where the Digital World Meets the Real World.

Contents

Pentium is a trademark of Intel Corporation.

Contents *(continued)*

Alpha Numeric Index of ICS Products

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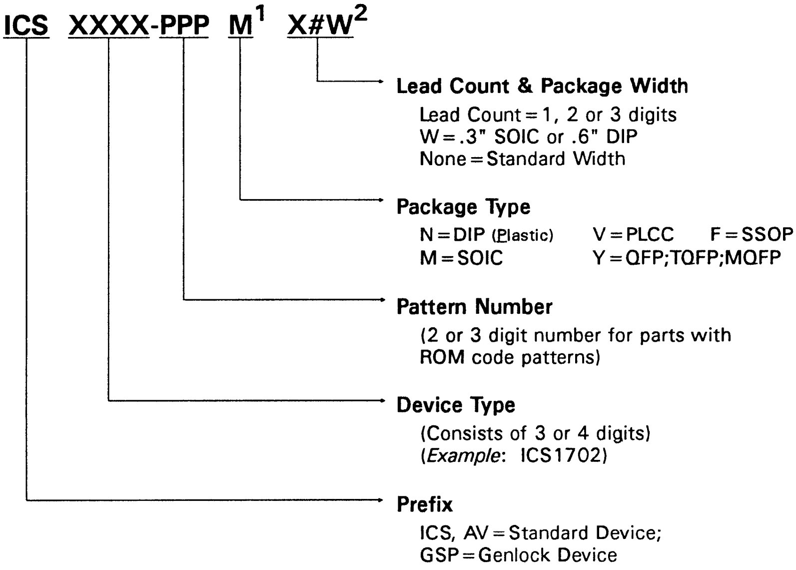
Sound Blaster is a trademark of Creative Technologies, Inc.; RAMBUS is a trademark of Rambus, Inc.; Pentium is a trademark of Intel Corporation; PowerPC is a trademark of Motorola Corporation.

ICS Ordering Information

Device Identification

All ICS standard circuits are marked as shown in the following example:

Ordering Information



ICS XXXX-PPP M[1] X#W[2]

Lead Count & Package Width
Lead Count = 1, 2 or 3 digits
W = .3" SOIC or .6" DIP
None = Standard Width

Package Type

N = DIP (Plastic)	V = PLCC	F = SSOP
M = SOIC	Y = QFP;TQFP;MQFP	

Pattern Number
(2 or 3 digit number for parts with
ROM code patterns)

Device Type
(Consists of 3 or 4 digits)
(*Example*: ICS1702)

Prefix
ICS, AV = Standard Device;
GSP = Genlock Device

Package Type

Specific dimensions for each package can be found in the Standard Package Dimensions (section K) section of this catalog.
Each data sheet references the respective package type and page number where it can be located within section K.

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[1] In some cases the Package Type may appear before the Pattern Number.
[2] Note: THIS SECTION IS ONLY INCLUDED ON OLDER AV OR ICS PARTS.

ICS Product Selection Guide

Video Timing Generator Products

PRODUCT APPLICATION	ICS DEVICE TYPE	DESCRIPTION	MAX FREQUENCY	CLOCK OUTPUTS	PACKAGE TYPES	PAGE
PC Graphics Clock Generators	ICS1494	Buffered XTAL Out, Lock Detect Output.	135 MHz	1 TTL	20-Pin DIP, SOIC	B-3
	ICS2494/ ICS2494A	Buffered XTAL Out, Lock Detect Output.	135 MHz	2 TTL	20-Pin DIP, SOIC	B-11
	ICS2495	Small Footprint, Narrow Body SOIC Package.	135 MHz	2 TTL	16-Pin DIP, SOIC	B-21
	ICS2496	Low Voltage, 3/5 Volt Operation for Laptop/Notebook Applications. Power-down Mode.	85/135 MHz	2 TTL	16-Pin DIP, SOIC	B-29
	ICS2595	Programmable Dual ICS2494 Pin compatible.	135 MHz	2 TTL	20-Pin DIP, SOIC	B-37
	ICS82C404	Dual Programmable Graphics Clock Generator. ICD82C404 compatible.	120 MHz	2 TTL	16-Pin DIP, SOIC	B-47
	ICS9161A	Dual Programmable Graphics Clock Generator. ICD2061 compatible.	135 MHz	3 TTL	16-Pin DIP, SOIC	B-89
Western Digital Compatible Graphics Clock Generators	ICS90C61A	Drop-in upgrade for the WD90C61. Integral Loop Filters.	80 MHz	2 TTL	20-Pin DIP, SOIC PLCC	B-61
	ICS90C64A	WD90C31 VGA Controller compatible. Enhanced Version. Integral Loop Filter. (Replaces ICS90C63, ICS90C64.)	80 MHz	2 TTL	20-Pin DIP, SOIC PLCC	B-71
	ICS90C65	Low Voltage, 3/5 Volt. Power-down Mode. WD90C26 VGA Controller compatible.	80 MHz	2 TTL	20-Pin DIP, SOIC PLCC	B-81

Motherboard Timing Generator Products

PRODUCT APPLICATION	ICS DEVICE TYPE	DESCRIPTION	NUMBER OF OUTPUTS	NUMBER OF PLL's	PACKAGE TYPES	PAGE
Motherboard	ICS2407 ICS2409 ICS2419 ICS2439	IMI407, IMI409 and IMI439 compatible.	6 9 10 9	2 2 2 2	18-Pin DIP, SOIC 24-Pin DIP, SSOP 24-Pin DIP, SSOP 24-Pin DIP, SSOP	C-3
	ICS2492	Buffered XTAL Out. Tristate PLL Outputs.	3	2	20-Pin DIP, SOIC	C-11
	ICS2494-244 ICS2494A-317	Buffered XTAL Out. *Note*: See Video Dot Clock Section for Data.	3	2	20-Pin DIP, SOIC	B-11
	ICS2694	9 Fixed, CPU-CPU/2 Selectable Provides CPU, Co-Processor, Hard and Floppy Disk, Kbd, Ser. Port, Bus CLK Function.	11	2	24-Pin DIP, SOIC	C-17
	AV9107C	CPU Clock Generator.	2	1	8-Pin DIP, SOIC 14-Pin DIP, SOIC	C-23
	ICS9108	3 Volt CPU Clock Generator.	2	1	8 or 14-Pin DIP, SOIC	C-29
Audio Synthesis	ICS9120-08/ ICS9120-09	3 Volt Multimedia Audio Synthesizer Clock Generator.	4	1	8-Pin SOIC	C-35

Motherboard Timing Generator Products *(continued)*

PRODUCT APPLICATION	ICS DEVICE TYPE	DESCRIPTION	NUMBER OF OUTPUTS	NUMBER OF PLL's	PACKAGE TYPES	PAGE
Notebook	ICS9131	32 kHz Input Generates CPU Clocks.	3	2	16-Pin SOIC, PDIP	C-41
	ICS9133X	32 kHz Input Generates CPU Clock and System Clock and Two Fixed Clocks.	6	3	20-Pin SOIC, PDIP	C-49
Sub-Notebook	ICS9134-06 ICS9134-07	32 kHz Motherboard Frequency Generator. Generated CPU, Reference and One Fixed Clock.	6	3	16-Pin SOIC	C-55
Pentium and Green PC Systems	AV9154A	Low Cost 16-Pin Clock Generator. Generates CPU Clock, Keyboard Clock, System Clock and I/O Clock.	7	2	16-Pin DIP, SOIC	C-61
OPTi Notebook	AV9154A-06 AV9154A-060	Clock Generator Designed for OPTi Chip set.	5	2	16-Pin PDIP 16-Pin Narrow SOIC	C-71
Motherboard	AV9155A	Motherboard Clock Generator. Produces CPU Clock, Keyboard Clock, System Clock and I/O Clock.	8	2	20-Pin DIP, SOIC	C-77
Desktop/Notebook	ICS9158	Clock Generator with Integrated Buffers.	11	2	24-Pin SOIC	C-89
Pentium Systems	ICS9159-02	Clock Generator and Integrated Buffers.	14	2	28-Pin SOIC	C-95
PowerPC Systems	ICS9160-03	Clock Generator for PowerPC 603 Systems.	15	2	32-Pin SOIC	C-99
	ICS9178-02	Clock Generator for PowerPC 601/601+ Systems.	14	1	44-Pin PQFP	C-103

Special Purpose ICs (Disk Drive, Low Skew (Pentium)

PRODUCT APPLICATION	ICS DEVICE TYPE	DESCRIPTION	NUMBER OF OUTPUTS	NUMBER OF PLL's	PACKAGE TYPES	PAGE
Motherboard	ICS1694A	Single Crystal Generates Three Low-Jitter Clocks.	3	1	8-Pin DIP, SOIC	D-3
Disk Drive or Video	AV9110	User-Programmable "On-the-Fly"; Low-Jitter makes it ideal for Disk Drive or Video Applications.	1	1	14-Pin DIP, SOIC	D-7
RAMBUS	ICS9111-01	High Frequency Clock for RAMBUS Systems.			8-Pin SOIC	D-17
Modem Ethernet AD1848	ICS9123	High Resolution Clock Generator; One Channel has Accuracy to within 50 PPM.	6	3	16- or 20-Pin DIP, SOIC	D-19
Telecom Radio Video Motherboard	AV9170	Clock Synchronizer and Multiplier.	2	1	8-Pin DIP, SOIC	D-21
Pentium	AV9172	Low Skew Output Buffer. Low Skew and Jitter make it ideal for Pentium Applications.	6	1	16-Pin DIP, SOIC	D-37
Video Genlock	AV9173	Lost Cost Video Genlock PLL.	2	1	8-Pin DIP, SOIC	D-45
Pentium PCs or Workstations	ICS9175	Low Skew Output Buffer Crystal Generates Six Low Skew, Low-Jitter Clocks.	6	1	16-Pin DIP, SOIC	D-51
Pentium or PLI	ICS9176	Input Clock Generates I/O Low Skew, Low-Jitter Outputs. Ideal for Pentium or PLI Applications.	11	1	28-Pin PLCC	D-57
High Frequency Motherboard	ICS9177	High Frequency Clock Generator. High-Performance, Low Skew, PECL and TTL Output Motherboard Clock Generator.	14	1	52-Pin QFP	D-63

High-Performance Video Timing Generator Products

PRODUCT APPLICATION	ICS DEVICE TYPE	DESCRIPTION	MAX FREQUENCY	CLOCK OUTPUTS	PACKAGE TYPES	PAGE
Projection LCD **Large-Panel LCD** **Medical Imaging Systems** **Virtual Reality Systems**	ICS1522	User-Programmable Frequencies; 'Line Lock' Capability. 15 kHz to 1 MHz reference to 230 MHz output.	230 MHz	Diff ECL	24-Pin SOIC	E-3
Mask Programmed Workstation	ICS1561A	÷2,4,8 TTL Out. Integral Loop Filter. Replaces ICS1561 to 230 MHz, ROM-based.	180 MHz	Diff ECL	20-Pin DIP, SOIC	E-23
High-Performance Workstation	ICS1562A	User-Programmable Frequencies. RAMDAC Reset Logic (Brooktree compatible) to 400 MHz.	230 MHz [320+MHz] [Special-Pin]	Diff ECL	16-Pin Narrow SOIC	E-31
Workstation Clock Generators	ICS1567	32 Frequency ROM-based Clock Reset Logic (Brooktree compatible) to 180 MHz.	180 MHz	Diff ECL	20-Pin DIP, SOIC	E-51
Mid-Range Workstation	ICS1572	User-Programmable Frequencies. RAMDAC Reset Logic (Brooktree compatible) to 180 MHz.	180 MHz	Diff ECL	20-Pin SOIC	E-61
Laser Printers	ICS1574	Laser Engine Pixel Clock to 400 MHz.	400 MHz	1 TTL	16-Pin Narrow SOIC	E-79
Motherboard	ICS1577	DEC Alpha™ CPU Clock to 466 MHz.	466 MHz	Diff ECL	14-Pin DIP	E-91
Mid-Range Workstation	ICS2572	User-Programmable Dual PLL 16V+4M Locations.	185 MHz	Diff ECL	20-Pin DIP, SOIC	E-99

Notes:
1. All products have internal loop filters except as noted.
2. All products operate at 5 volts typ. except as noted.

Alpha is a trademark of Digital Equipment Corporation.

Communications Products

PRODUCT APPLICATION	ICS DEVICE TYPE	DESCRIPTION	PACKAGE TYPES	PAGE
Caller I.D.	ICS1660	FSK Signal Interface Device.	18-Pin DIP 20-Pin SOIC	F-3
LAN/WAN Communications Systems	ICS1884	SONET/SDH Clock Recovery On-chip VCXO, 51/155 Mb, Bellcore Compliance.	28-Pin SOIC	F-15
	ICS1885	LAN/WAN Transceiver 26, 44, 51, 155 Mb.	28-Pin SOIC	F-27
	ICS1886	LAN/WAN Transceiver 32, 34, 97 139 Mb.	28-Pin SOIC	F-33
	ICS1887	FDDI/Fast ENET Transceiver 100Mb, Full duplex.	28-Pin SOIC	F-39
	ICS1888	High-Performance Twisted Pair Communication PHYceiver.	*to be determined*	F-45
	ICS1889	100Base-FX Integrated PHYceiver.	52-Pin MQFP	F-47
	ICS1890	10Base-T/100Base-TX Integrated PHYceiver.	52-Pin MQFP	F-49
	ICS1891	100Base-TX Integrated PHYceiver for Repeaters.	52-Pin MQFP	F-51

Multimedia Products

PRODUCT APPLICATION	ICS DEVICE TYPE	DESCRIPTION	PACKAGE TYPES	PAGE
Video Graphics	GSP500 GSP500 Application Notes	**VGA/NTSC Genlock.**	**68-Pin PLCC**	**G-3**
	GSP600 GSP600 Application Notes	**VGA/PAL Genlock.**	**68-Pin PLCC**	**G-49**
	ICS1522	*Note:* See High-Performance section for data.	24-Pin SOIC	E-3
Codecs	ICS2002	**Business Audio Codec.**	44-Pin PLCC	G-85
Sound/Video Synchronization	ICS2008A	Improved SMPTE-MIDI Peripheral	44-Pin PLCC	G-105
Audio Mixers	ICS2101	5 Channel Digitally Controlled Audio Mixer.	28-Pin DIP, SOIC	G-123
	ICS2102	Sound Blaster Compatible Mixer.	28-Pin SOIC	G-131
Wavetable Synthesis	ICS2115	WaveFront MIDI Synthesizer.	84-Pin PLCC 100-Pin TQFP	G-141
	ICS2116	WaveFront ISA Interface.	100-Pin PQFP	G-171
	ICS2122	WaveFront Sounds 2Mb General MIDI.	44-Pin SOIC	G-185
	ICS2124-001/ ICS2124-002	WaveFront Sounds 512kb General MIDI ROM.	44-Pin SOIC	G-189
	ICS2125	WaveFront Sounds 4Mb CMOS Mask ROM.	32-Pin SOIC	G-193
Audio Synthesis Clock Geernator	ICS9120-08/-09	Clock for Audio Systems. *Note*: See Motherboard section for data.	8-Pin SOIC	C-35

GENDAC Products

PRODUCT APPLICATION	ICS DEVICE TYPE	DESCRIPTION	PACKAGE TYPES	PAGE
Personal Computer and Engineering Work Station Computer Graphics	ICS5300	Integrated Dual Clock. 8-bit Generic.	44-Pin PLCC	H-3
	ICS5301	Integrated Dual Clock. 8-bit Tseng Compatible.	44-Pin PLCC	H-33
	ICS5340	Integrated Dual Clock. 16-bit Generic.	68-Pin PLCC	H-63
	ICS5341	Integrated Dual Clock. 16-bit Tseng Compatible.	68-Pin PLCC	H-97
	ICS5342	16-bit Integrated Clock, Palette RAM and DACs.	68-Pin PLCC	H-101

Power Management Products

CHARGE TERMINATION METHODS	ICS DEVICE TYPE	DESCRIPTION	MINIMUM CHARGE RATE	PACKAGE TYPES	PAGE
Voltage Slope Maximum Temperature Charge Timer	ICS1700A	Hot Battery Shutdown. Cold Battery Charge.	Four Rates (C2/ to 4C)	16-Pin DIP 20-Pin SOIC	I-3
Voltage Slope Temperature Slope Maximum Temperature Charge Timers	ICS1702	Six Auxiliary Modes. Hot Battery Shutdown. Cold Battery Charge. Adjustable Battery Detection.	Nine Rates (C/4 to 4C)	20-Pin DIP 20-Pin SOIC	I-27
Voltage Slope Temperature Slope Maximum Temperature Charge Timer	ICS1712	Hot Battery Shutdown. Cold Battery Charge.	Four Rates (C/2 to 4C)	16-Pin DIP 16-Pin SOIC	I-57
Voltage Slope Charge Timers	ICS1722	Six Auxiliary Modes. Adjustable Battery Detection.	Nine Rates (C/4 to 4C)	16-Pin DIP 16-Pin SOIC	I-79

ICS
Video Timing Generator Products

ICS is the recognized world leader in frequency synthesis technology. Our frequency generators have revolutionized the way systems manufacturers generate and control clocks. We have obsoleted the need for expensive, inflexible crystal oscillators by replacing them with solid state CMOS clock generation. ICS's low cost, high quality and excellent service are some of the reasons why our frequency generators are the industry's first choice. First and foremost, however, is our product diversity.

ICS has continued to build on its solid foundation, bringing the most requested features to market. In particular, ICS has expanded video clock product offerings to provide a truly complete selection unequaled in performance, breadth and value. We provide the perfect system clock solution for a range of microprocessors including advanced Pentium and Power PC systems. Moreover, ICS has double the design of its competitors in motherboards, graphics, disk drivers and modems.

As a market-oriented company, ICS welcomes inquiries concerning our new product areas or other frequency synthesis applications.

ICS Video Timing Generator Selection Guide

Product Application	ICS Device Type	Description	Max Frequency	Clock Outputs	Package Types	Page
PC Clocks	ICS1494	Buffered XTAL Out, Lock Detect Output.	135 MHz	1 TTL	20-Pin DIP, SOIC	B-3
	ICS2494/94A	Buffered XTAL Out, Lock Detect Output.	135 MHz	2 TTL	20-Pin DIP, SOIC	B-11
	ICS2495	Small Footprint, Narrow Body SOIC Package.	135 MHz	2 TTL	16-Pin DIP, SOIC	B-21
	ICS2496	Low Voltage, 3/5 Volt Operation for Laptop/Notebook Applications. Power-down Mode.	85/135 MHz	2 TTL	16-Pin DIP, SOIC	B-29
	ICS2595	Programmable Dual ICS2494 Pin Compatible.	135 MHz	2 TTL	20-Pin DIP, SOIC	B-37
	ICS82C404	Dual Programmable Graphics Clock Generator. ICD82C404 Compatible.	120 MHz	2 TTL	16-Pin DIP, SOIC	B-47
	ICS9161A	Dual Programmable Graphics Clock Generator. ICD2061 Compatible	135 MHz	3 TTL	16-Pin PDIP, SOIC	B-89
Western Digital Compatible Clock Generators	ICS90C61A	Drop-in upgrade for the WD90C61. Integral Loop Filters.	80 MHz	2 TTL	20-Pin DIP, SOIC, PLCC	B-61
	ICS90C64A	WD90C31 VGA Controller Compatible. Enhanced Version. Integral Loop Filter. (Replaces ICS90C63, ICS90C64.)	80 MHz	2 TTL	20-Pin DIP, SOIC, PLCC	B-71
	ICS90C65	Low Voltage, 3/5 Volt. Power-down Mode. WD90C26 VGA Controller Compatible.	80 MHz	2 TTL	20-Pin DIP, SOIC, PLCC	B-81

Notes:

1. All products have internal loop filters except as noted.
2. All products operate at 5 volts typ. except as noted.

Integrated
Circuit
Systems, Inc.

ICS1494

Enhanced Video Dot Clock Generator

Features

- Low cost - eliminates need for multiple crystal clock oscillators in video display subsystems
- Mask-programmable frequencies
- Pre-programmed versions for Industry Standard VGA chips
- Glitch-free frequency transitions
- Provision for external frequency input
- Excellent power supply rejection
- Small footprint - 20-pin DIP or SOIC

Applications

- Higher Frequency applications
- EGA - VGA - Super VGA-XGA video adapters
- High resolution MAC II displays
- Workstations
- LCD and other flat panel display systems
- 8514A - TMS 34010 - TMS 34020
- Motherboard - PS2™ display systems

Description

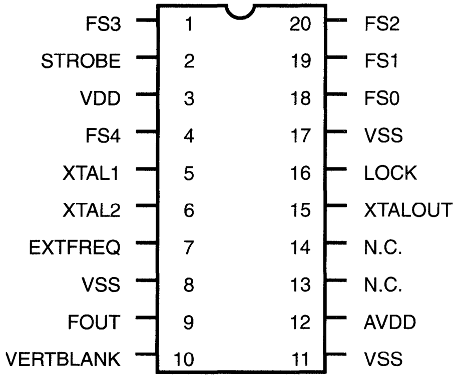
The **ICS1494** Dot Clock Generator is an integrated circuit capable of generating up to 32 video dot clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS1494** provides a low power, small footprint, low cost solution to the generation of video dot clocks. Outputs are compatible with **VGA, EGA, XGA, MCGA, CGA, MDA,** as well as the higher frequencies needed for advanced applications in desktop publishing and workstation graphics. Provision is made via a single-level custom mask to implement customer-specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

In addition to providing 32 clock rates, the **ICS1494** has provisions to multiplex an externally-generated signal source into the **FOUT** signal path. The **ICS1494** can also be programmed to select the crystal oscillator signal as the **FOUT** output. Internal phase-locked frequencies continue to remain locked at their preset values when these modes are selected. This feature permits instantaneous transition from an external frequency to an internally-generated frequency. Printed circuit board testing is simplified by the use of these modes, as an external clock generated by the ATE tester can be fed through, permitting synchronous testing of the entire graphics system.

Features

- 135 MHz Guaranteed Performance
- Fast acquisition of selected frequencies
- Internal loop filter eliminates noise pickup
- Advanced PLL for low phase-jitter
- Improved loop stability over entire frequency range
- Frequency change synchronized to vertical retrace
- Frequency change-detection circuitry enhances new frequency acquisition
- Lock Detect Output
- Buffered XTAL Out

Pin Configuration



20-Pin DIP or SOIC
K-4, K-7

Notes:

1 In applications where the external frequency input is not specified, EXTFREQ must be tied to V_{DD}.

2. ICS1494M(SOIC) pinout is identical to ICS1494N(DIP).

Circuit and Application Options

The **ICS1494** will typically derive its frequency reference from a series-resonant crystal connected between pins 5 and 6. Where a high quality reference signal is available, such as in an application where the graphics subsystem is resident on the motherboard, this reference may directly replace the crystal. This signal should be coupled to pin 1. If the reference signal amplitude is less than 3.5 volts, a .047 microfarad capacitor should be used to couple the reference signal into XTAL1. Pin 6 must be left open.

The **ICS1494** is capable of multiplexing an externally generated frequency source of **FOUT** via a mask option, in addition to its internally generated clock.

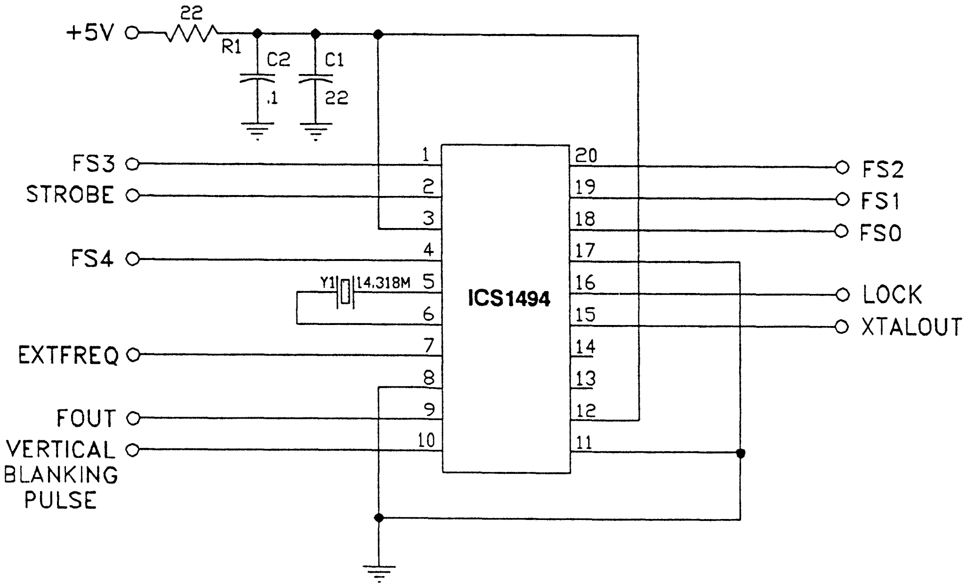
This is input via **EXTFREQ (7)**. When an external source is selected the PLL remains locked to the value specified in the selected address. This provision facilitates the ability to rapidly change frequencies. When this option is not specified in the ROM pattern, pin 7 is internally tied to VDD and should be connected to VDD on the PCB.

Power Supply Conditioning

The **ICS1494** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in Figures 1 or 2. Figure 1 is the normal configuration for 5 Volt only applications. Which of the two provides superior performance depends on the noise content of the power supplies. In general, the configuration of Figure 1 is satisfactory. Figure 2 is the more conventional if a 12 Volt analog supply is available, although the improved performance comes at a cost of an extra component. The cost of the discretes used in Figure 2 is less than the cost of Figure 1's discrete components.

The number and differentiation of the analog and digital supply pins are intended for maximum performance products. In most applications, all VDDs may be tied together. The function of the multiple pins is to allow the user to realize the maximum performance from the silicon with a minimum degradation due to the package and PCB. At the frequencies of interest, the effects of the inductance of the bond wires and package lead frame are non-trivial. By using the multiple pins, ICS minimized the effect of packaging and minimized the interaction of the digital and analog supply currents.

Figure 1



Applications

Layout Considerations

Utilizing the **ICS1494** in video graphics adapter cards or on PS2 motherboards is simple but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised in ensuring that components not related to the **ICS1494** do not share its ground. In applications utilizing a multi-layer board, V_{SS} should be directly connected to the ground plane. Multiple pins are utilized for all analog and digital Vss and Vdd connections to permit extended frequency **VCLK** operation to 135 MHz. However, in all cases, all V_{SS} and V_{DD} pins should be connected.

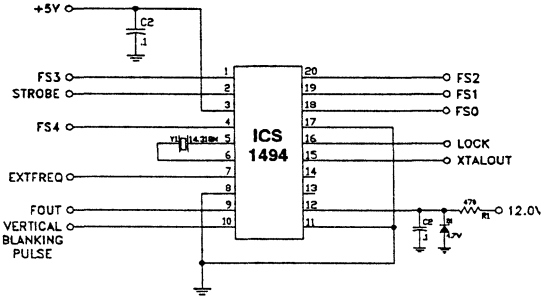


Figure 2

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series-resonant crystal should be connected between **XTAL1 (5)** and **XTAL2 (6)**. In IBM-compatible applications this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10MHz and 25MHz have been tested. Maintain short lead lengths between the crystal and the **ICS1494**. In some applications, it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to **XTAL1 (5)**. If the signal amplitude is less than 3.5 volts, connect the clock through a .047 microfarad capacitor to **XTAL1 (5)**, and keep the lead length of the capacitor to **XTAL1 (5)** to a minimum to reduce noise susceptibility. This input is internally biased at $V_{DD}/ 2$. Since TTL compatible clocks typically exhibit a V_{OH} of 3.5V, capacitively coupling the input restores noise immunity. The **ICS1494** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (6)** must be left open in this configuration.

LOCK

LOCK(16) is an output signal which may be monitored to indicate when the **ICS1494** has achieved phase lock after a change in frequency has been selected. In systems where it is used, it is tied to an interrupt input to the microprocessor. When high, it indicates phase lock has been achieved.

Buffered XTALOUT

In motherboard applications, it may be desirable to have the **ICS1494** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. To do this, the **XTALOUT (15)** output should be buffered with a CMOS driver.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **FOUT(9)** and other components in the system should be kept as short as possible. The **ICS1494** outputs have been designed to minimize overshoot. In addition it may be helpful to place a ferrite bead in this signal path to limit the propagation of high order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS1494**. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may reduce phase-jitter as well as EMI.

External Frequency Sources

EXTFREQ (7), on versions so equipped by the programming, is an input to a digital multiplexer. When this input is enabled, signals driving the input will appear at **FOUT(9)** instead of the PLL output. Internally, the PLL will remain in lock at the frequency selected by the ROM code. **If this option is not specified, pin (7) is connected to VDD internally, and MUST be connected to VDD or left open, not grounded!**

Digital Inputs

FS0 (18), FS1 (19), FS2 (20),FS3(1), and **FS4 (4)**, are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (2),** when high, allows new data into the frequency select latches; and when low, prevents address changes per Figure 3. The internal power-on-clear signal will force an initial frequency code corresponding to an all zeros input state. **VERTBLANK (10),** when low, inhibits the transfer of new frequency select information. Enabling this pin during the vertical blanking interval causes the change in frequency to happen at this time and prevents any visible glitch when a new frequency is selected. If this feature is not required, this pin may be left open.

Absolute Maximum Ratings

Supply Voltage	V_{DD}	-0.5V to +7V
Input Voltage	V_{IN}	-0.5V to V_{DD}+0.5V
Output Voltage	V_{OUT}	-0.5V to V_{DD}+0.5V
Clamp Diode Current	V_{IK} & I_{OK}	±30mA
Output Current per Pin	I_{OUT}	±50mA
Operating Temperature	T_O	0 °C to 70 °C
Storage Temperature	T_S	-85 °C to +150 °C
Power Dissipation	P_D	500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to >= V_{SS} and <=V_{DD}.

DC Characteristics (0 °C to 70 °C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{dd}	Operating Voltage Range	4.0	5.5	V	
V_{il}	Input Low Voltage	V_{ss}	0.8	V	V_{dd} = 5V
V_{ih}	Input High Voltage	2.0	V_{dd}	V	V_{dd} = 5V
I_{lh}	Input Leakage Current	-	10	uA	V_{in} = V_{cc}
V_{ol}	Output Low Voltage	-	0.4	V	I_{ol} = 4.0 mA
V_{oh}	Output High Voltage	2.4	-	V	I_{oh} = 4.0 mA
I_{dda}	Analog Supply Current	-	5	mA	V_{dd} = 5.0V, FOUT = 25 MHz
I_{dda}	Analog Supply Current	-	7	mA	V_{dd} = 5.0V, FOUT = 110 MHz
I_{ddd}	Digital Supply Current	-	12	mA	V_{dd} = 5.0V, FOUT = 25 MHz
I_{ddd}	Digital Supply Current	-	25	mA	V_{dd} = 5.0V, FOUT = 110 MHz
R_{up} *	Internal Pull-up Resistors	50	200	K Ohm	V_{dd} = 5V, V_{in} = 0V
C_{in}	Input Pin Capacitance	-	8	pF	F_c = 1 MHz
C_{out}	Output Pin Capacitance	-	12	pF	F_c = 1 MHz

* The following inputs have pull-ups: FS0-4, STROBE, EXTFREQ, VERTBLANK.

AC Timing Characteristics

The following notes apply to all parameters presented in this section:

1. Xtal Frequency = 14.31818 MHz
2. All units are in nanoseconds (ns).
3. Rise and fall time is between 0.8 and 2.0 VDC.
4. Output pin loading = 15pF
5. Duty cycle is measured at 1.4V.
6. Supply Voltage Range = 4.75 to 5.25 Volts
7. Temperature Range = 0 °C to 70 °C

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	10	-	
	FOUT TIMING			
Tr	Rise Time	-	3	
Tf	Fall Time	-	3	
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	15	ns
	Duty Cycle	40%	60%	110 MHz or less

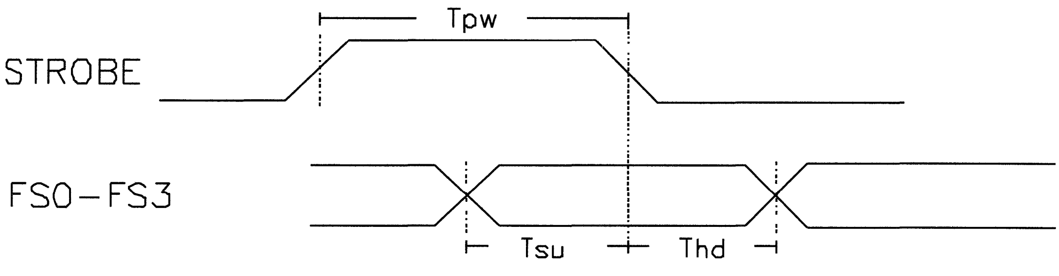


Figure 3

Ordering Information

ICS1494AN-XXX or ICS1494AM-XXX

Example:

ICS XXXX M -XXX

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type

N=DIP (Plastic)
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV=Standard Device; GSP=Genlock Device

ICS1494 Pattern Request Form

ICS produces a selection of standard pattern **ICS1494**'s pre-programmed for compatibility with many popular VGA chipsets. Custom patterns are also available, although a significant volume commitment and/or one-time mask charge will apply. Contact ICS sales for details.

ICS Part Number	ICS1494-523	ICS 1494-527	ICS1494-530	ICS1494-535	ICS 1494-539	ICS1494-540	ICS1494 543	ICS1494 544
Compatible VGA Chipsets	Tseng Labs ET4000	Cirrus Logic GD5320 GD6410	NCR 77C22E	ATI	Tseng Labs ET4000 (2X Freq.)	Radius	Supermac	Seiko-Epson
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	25.175	XTAL	XTAL	42 950	25.175	57.283	14 318	28 636
1	28.322	16.257	16.257	48.770	28 332	12.273	EXT	42 105
2	32.514	EXTFREQ	EXTFREQ	92 400	32.514	14.500	12.273	47.846
3	36.000	32.514	32.514	36.000	36.000	15 667	15 667	78 431
4	40.000	25.175	25.175	50 350	40.000	112 000	17 734	XTAL
5	44.900	28.322	28 322	56.644	44 900	126.000	25 175	21 053
6	65.000	24.000	24 000	EXT	50.350	30 240	30 240	50.350
7	84.000	40.000	40.000	44.900	65.000	91.200	13.500	25 175
8	25.175	XTAL	25.175	30.240	33 400	120.000	14.750	EXT
9	28.322	16.257	28.322	32.000	37.575	48.000	14.187	3.000
A	40.000	EXTFREQ	36.000	110.000	31.480	50.675	55.000	6.000
B	44.900	36.000	65.000	80.000	41.750	55.300	57 283	8.000
C	32.514	25.175	44.900	39.910	55.110	64.000	64.000	10.000
D	28.322	28.332	50.000	44.900	74 160	68.750	80.000	12.000
E	36.000	24.000	56.000	75.000	77.250	88.500	100 000	16.000
F	65.000	40.000	75.000	65.000	80.000	51.270	130.480	20 000
10	25.175	XTAL	25.175	42.950	50.350	100.000	28.322	25.000
11	28.322	65.028	28.322	48.770	56.664	95.200	36.000	30 000
12	32.514	EXTFREQ	40.000	92.400	65.028	55.000	40.000	32.000
13	36.000	36.000	65.000	36.000	72.000	60.000	40.900	33.000
14	40.000	25.175	44.900	50.350	80.000	63.000	44.900	40 000
15	44.900	28.332	50.000	56.644	89.800	99.522	50.000	44.000
16	56.000	24.000	56.000	EXT	75.000	130.000	62.000	46.000
17	65.000	40.000	75.000	44.900	108.000	80.000	65.000	50 000
18	25.175	44.900	25.175	30.240	70.000	25.175	75.000	60.000
19	28.322	50.344	28.322	32.000	75.000	28 322	89.211	66.000
1A	32.514	16.257	EXTFREQ	110.000	85.000	48.000	99.522	70.000
1B	40.000	32.514	EXTFREQ	80.000	90.000	76.800	103 140	80.000
1C	44.900	56.644	60.000	39.910	95.000	38 400	107.350	90.000
1D	60.000	20.000	80.000	44.900	110.000	43.200	111.518	100 000
1E	80.000	50.000	EXTFREQ	75.000	115.000	61.440	113.484	110.000
1F	84.000	80.000	EXTFREQ	65.000	120.000	EXT	122 320	120.000

Standard frequency patterns are available and are included as an example.
Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.
All standard patterns shown above use 14.31818 MHz as the input reference frequency.
If the internal frequency to which the ICS1494 remains locked when EXTFREQ is selected is critical, it should be specified.
Order info: ICS1494M-XXX or ICS1494N-XXX (M= SOIC pkg., N= DIP pkg., XXX = Pattern number)

Integrated
Circuit
Systems, Inc.

ICS2494
ICS2494A

Dual Video/Memory Clock Generator

Features

- World standard **ICS2494A** has been reconfigured to allow 8 memory frequencies.
- Mask-programmable frequencies
- Pre-programmed versions for Industry Standard VGA chips
- Glitch-free frequency transitions
- Provision for external frequency input
- Internal clock remains locked when the external frequency input is selected
- Low power CMOS device technology
- Small footprint - 20-pin DIP or SOIC

New Features

- Buffered XTAL Out
- Integral loop filter components
- Fast acquisition of selected frequencies, strobed or non-strobed
- Guaranteed performance up to 135 MHz
- Excellent power supply rejection
- Advanced PLL for low phase-jitter
- Frequency change detection circuitry which enhances new frequency acquisition and eliminates problems caused by programs that rewrite frequency information.
- Improved pinout - easier board layout.

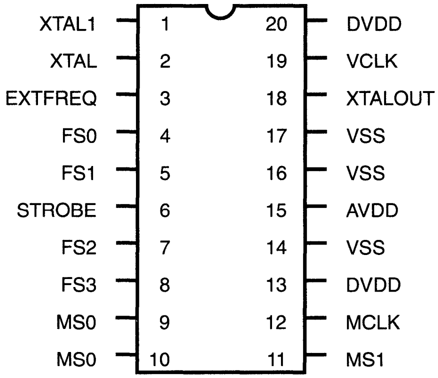
Applications

- VGA-Super VGA-XGA video adapters
- Workstations
- 8514A-TMS34010-TMS34020
- Motherboard

Description

The Dot Clock Generator is an integrated circuit dual phase-locked loop frequency synthesizer capable of generating sixteen video dot clock frequencies and eight memory clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS2494/94A** provides a low-power, small-footprint, low-cost solution to the generation of video dot clocks. Outputs are compatible with XGA, VGA, EGA, MCGA, CGA, MDA, as well as the higher frequencies needed for advanced applications in desktop publishing and workstation graphics. Provision is made via a single-level custom mask to implement customer-specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

Pin Configuration



20-Pin DIP or SOIC
K-4, K-7

Notes:

1. In applications where the external frequency input is not specified, EXTFREQ must be tied to V_{SS}.
2. ICS2494/94AM(SOIC) pinout is identical to ICS2494/94AN(DIP)

Circuit and Application Options

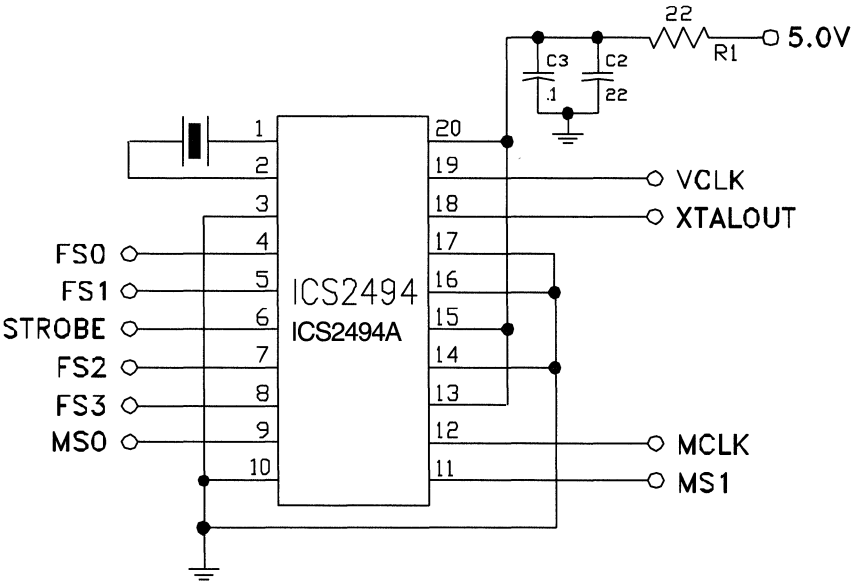
The **ICS2494/94A** will typically derive its frequency reference from a series-resonant crystal connected between pins 1 and 2. Where a high quality reference signal is available, such as in an application where the graphics subsystem is resident on the motherboard, this reference may directly replace the crystal. This signal should be coupled to pin 1. If the reference signal amplitude is less than 3.5 volts, a .047 microfarad capacitor should be used to couple the reference signal into **XTAL1**. Pin 2 must be left open.

Power Supply Conditioning

The **ICS2494/94A** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in Figures 1 or 2. Figure 1 is the normal configuration for 5 volt only applications. Which of the two provides superior performance depends on the noise content of the power supplies. In general, the configuration of Figure 1 is satisfactory. Figure 2 is the more conventional if a 12 volt analog supply is available, although the improved performance comes at a cost of an extra component. The cost of the discretes used in Figure 2, however, are less than the cost of Figure 1's discrete components.

The number and differentiation of the analog and digital supply pins are intended for maximum performance products. In most applications, all VDDs may be tied together. The function of the multiple pins is to allow the user to realize the maximum performance from the silicon with a minimum degradation due to the package and PCB. At the frequencies of interest, the effects of the inductance of the bond wires and package lead frame are non-trivial. By using the multiple pins, ICS minimized the effect of packaging and minimized the interaction of the digital and analog supply currents.

Figure 1

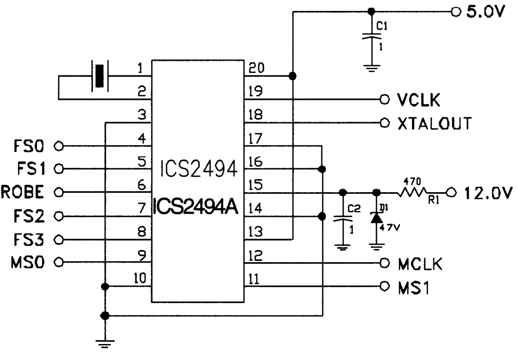


Applications

Layout Considerations

Utilizing the **ICS2494/94A** in video graphics adapter cards or on PS2 motherboards is simple but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised in ensuring that components not related to the **ICS2494/94A** do not share its ground. In applications utilizing a multi-layer board, VSS should be directly connected to the ground plane. Multiple pins are utilized for all analog and digital VSS and VDD connections to permit extended frequency VCLK operation to 135 MHz. However, in all cases, all VSS and VDD pins should be connected.

Figure 2



Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series-resonant crystal should be connected between **XTAL1 (1)** and **XTAL2 (2)**. In IBM-compatible applications this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10 MHz and 25 MHz have been tested. Maintain short lead lengths between the crystal and the **ICS2494/94A**. In some applications, it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to **XTAL1 (1)**. If the signal amplitude is less than 3.5 volts, connect the clock through a .047 microfarad capacitor to **XTAL1 (1)**, and keep the lead length of the capacitor to **XTAL1 (1)** to a minimum to reduce noise susceptibility. This input is internally biased at VDD/2. Since TTL compatible clocks typically exhibit a VOH of 3.5V, capacitively coupling the input restores noise immunity.

The **ICS2494/94A** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (2)** must be left open in this configuration.

Buffered XTALOUT

In motherboard applications it may be desirable to have the **ICS2494/94A** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. To do this, the **XTALOUT (18)** output should be buffered with a CMOS driver.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **VCLK (19) or MCLK (12)** and other components in the system should be kept as short as possible. The **ICS2494/94A** outputs have been designed to minimize overshoot. In addition it may be helpful to place a ferrite bead in these signal paths to limit the propagation of high order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS2494/94A**. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may reduce phase-jitter as well as EMI.

Digital Inputs

FS0 (4), FS1 (5), FS2 (7), and **FS3 (8)** are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (6)**, when high, allows new data into the frequency select latches; and when low, prevents address changes per Figure 3. The internal power-on-clear signal will force an initial frequency code corresponding to an all zeros input state. **MS0 (9), MS1 (11)** and **MS2 (3)** are the corresponding memory select inputs and are not strobed.

Absolute Maximum Ratings

Supply Voltage	V_{DD}	-0.5V to +7V
Input Voltage	V_{IN}	-0.5V to V_{DD}+0.5V
Output Voltage	V_{OUT}	-0.5V to VDD+0.5V
Clamp Diode Current	V_{IK} & I_{OK}	±30mA
Output Current per Pin	I_{OUT}	±50mA
Operating Temperature	T_o	0 °C to 70 °C
Storage Temperature	T_S	-85 °C to +150 °C
Power Dissipation	P_D	500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to >= V_{SS} and <=V_{DD}.

DC Characteristics (0 °C to 70 °C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range	4.0	5.5	V	
V_{IL}	Input Low Voltage	V_{ss}	0.8	V	V_{dd} = 5V
V_{IH}	Input High Voltage	2.0	V_{dd}	V	V_{dd} = 5V
I_{IH}	Input Leakage Current	-	10	*u*A	V_{in} = V_{cc}
V_{OL}	Output Low Voltage	-	0.4	V	I_{ol} = 4.0 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{oh} = 4.0 mA
I_{DD}	Supply Current	-	35	mA	V_{dd} = 5V, VCLK = 80 MHz
R_{UP} *	Internal Pull-up Resistors	50	200	K Ohm	V_{dd} = 5V, V_{in} = 0V
C_{in}	Input Pin Capacitance	-	8	pF	F_c = 1 MHz
C_{out}	Output Pin Capacitance	-	12	pF	F_c = 1 MHz

* The following inputs have pull-ups: FS0-3, MS0-1, STROBE.

Frequency Pattern Availability

ICS offers the largest variety of standard frequency patterns in the industry, supporting all popular VGA controller devices. The attached listing provides the selection as of this publication date. Contact your local ICS sales office for latest frequency pattern availability.

AC Timing Characteristics

The following notes apply to all parameters presented in this section:

1. Xtal Frequency = 14.31818 MHz
2. $T_C = 1/ F_C$
3. All units are in nanoseconds (ns).
4. Rise and fall time is between 0.8 and 2.0 VDC.
5. Output pin loading = 25pF
6. Duty cycle is measured at 1.4V.
7. Supply Voltage Range = 4.0 to 5.5 Volts
8. Temperature Range = 0 °C to 70 °C

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	10	-	
	MCLK AND VCLK TIMINGS			
Tr	Rise Time	-	3	Duty Cycle 40% min. to 60% max.
Tf	Fall Time	-	3	
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	15	ns

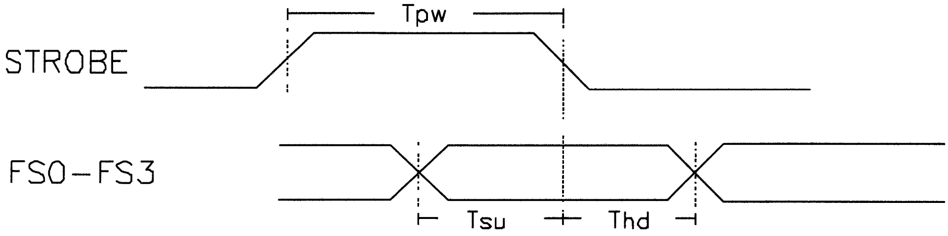


Figure 3

Ordering Information

ICS2494AN-XXX or ICS2494AM-XXX

Example:

ICS XXXX M -XXX

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type

N=DIP (Plastic)

M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV=Standard Device; GSP=Genlock Device

ICS2494 Standard Patterns

ICS produces a selection of standard pattern **ICS2494**'s pre-programmed for compatibility with many popular VGA chipsets. Custom patterns are also available, although a significant volume commitment and/or one-time mash charge will apply. Contact ICS sales for details.

ICS Part Number	ICS2494-236 ICS2494A-310*[1]	ICS 9294-237 ICS2494A-304*[2]	ICS2494-240	ICS2494-244 ICS2494A 317*[3]	ICS2494-245/307	ICS2494-247	ICS2494-253	ICS2494-256
Compatible VGA Chipsets	Cirrus Logic GD6410	Tseng Labs ET4000 ET400-W32 Acer M3125	Texas. Instr. TMS34010 TMS34020	Motherboard Applications (CPU Clocks)		Cirrus Logic GD5320	NCR 77C22E	S3 86C911 86C924
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	XTAL	50.350	25.175	20.000	50.350	XTAL	25.175	25.175
1	65.028	56.644	28.332	24.000	56.644	16.257	28.322	28.322
2	EXTFREQ	65.000	28.636	32.000	65.000	EXTFREQ	40.000	40.000
3	36.000	72.000	36.000	40.000	72.000	32.514	65.000	EXTFREQ
4	25.175	80.000	40.000	50.000	80.000	25.175	44.900	50.000
5	28.322	89.800	42.954	66.667	89.800	28.322	50.000	77.000
6	24.000	63.000	44.900	80.000	63.000	24.000	130.000	36.000
7	40.000	75.000	57.272	100.000	75.000	40.000	75.000	44.889
8	44.900	25.175	60.000	54.000	25.175	XTAL	25.175	130.000
9	50.350	28.322	63.960	70.000	28.322	16.257	28.322	120.000
A	16.257	31.500	75.000	90.000	31.500	EXTFREQ	EXTFREQ	80.000
B	32.514	36.000	80.000	110.000	36.000	36.000	EXTFREQ	31.500
C	56.644	40.000	85.000	25.000	40.000	25.175	60.000	110.000
D	20.000	44.900	99.000	33.333	44.900	28.322	80.000	65.000
E	41.539	50.000	102.000	40.000	50.000	24.000	EXTFREQ	75.000
F	80.000	65.000	108.000	50.000	77.500	40.000	EXTFREQ	72.000
Memory Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	32.900	40.000	64.000	16.000	40.000	31.000	50.000	55.000
1	35.600	41.612	40.000	24.000	41.612	36.400	60.000	75.000
2	43.900	44.744	48.000	50.000	44.744	43.900	65.000	70.000
3	49.100	50.000	60.000	66.667	50.000	49.100	75.000	80.000

*1 ICS2494A-310 directly replaces ICS2494-236.
*2 ICS2494A-304 directly replaces ICS2494-237.
*3 ICS2494A-317 directly replaces ICS2494-244.
*4 ICS2494A-318 directly replaces ICS2494-266.

Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.

All standard patterns shown above use 14.31818 MHz as the input reference frequency.

Order info: ICS2494M-XXX or ICS2494N-XXX (M= SOIC pkg., N= DIP pkg., XXX= Pattern number)
ICS2494AM-XXX or ICS2494AN-XXX (M= SOIC pkg., N= DIP pkg., XXX= Pattern number)

ICS Part Number	ICS2494-260	ICS2494-263	ICS2494 266 ICS2494-318*[4]	ICS2494-271/321	ICS2494-273	ICS2494-275	ICS2494-277	ICS2494-280	ICS2494-281
Compatible VGA Chipsets	Weitek W5086 W5186	NCR 77C22E	Cirrus Logic GD5410		Headland HT216 HT216-32	S3 86C801 86C805 86C928	NCR 77C22E+	S3 86C801 86C805	Tseng
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	50.350	25.175	30.250	25.175	25.175	25.175	25.175	25.175	50.350
1	56.644	28.322	65.000	28.322	28.322	28.322	28.322	28.322	56.644
2	33.250	36.000	85.000	EXT	40.000	40.000	36.000	40.000	65.000
3	52.000	65.000	36.000	44.900	32.500	EXTFREQ	65.000	EXT	72.000
4	80.000	44.900	25.175	41.539	50.350	50.000	44.900	50.000	80.000
5	63.000	50.000	283.322	78.000	65.000	77.000	50.000	77.000	89.800
6	EXTFREQ	80.000	34.000	79.200	38.000	36.000	80.000	36.000	63.000
7	75.000	75.000	40.000	80.000	44.900	44.889	75.000	44.889	75.000
8	25.175	25.175	44.900	31.469	31.500	130.000	56.644	130.000	83.078
9	28.322	28.322	50.350	35.402	36.000	120.000	63.000	120.000	93.463
A	31.500	EXTFREQ	31.500	EXTFREQ	80.000	80.000	72.000	80.000	100.000
B	36.000	EXTFREQ	32.500	56.125	63.000	31.500	130.000	31.500	104.000
C	40.000	60.000	63.000	51.924	50.000	110.000	90.000	110.000	108.000
D	44.900	80.000	72.000	91.000	100.00	65.000	100.000	65.000	120.000
E	50.000	EXTFREQ	75.000	87.406	76.000	75.000	110.000	75.000	130.000
F	65.000	EXTFREQ	80.000	36.000	110.000	94.500	120.000	94.500	134.700
Memory Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	40.000	50.000	36.000	51.924	70.000	45.000	50.000	55.000	50.000
1	33.333	40.000	44.000	41.539	63.830	38.000	60.000	60.000	55.000
2	45.000	65.000	49.000	44.900	60.000	52.000	65.000	70.000	60.000
3	50.000	75.000	40.000	56.125	81.000	50.000	75.000	65.000	65.000

*1 ICS2494A-310 directly replaces ICS2494-236.
*2 ICS2494A-304 directly replaces ICS2494-237.
*3 ICS2494A-317 directly replaces ICS2494-244.
*4 ICS2494A-318 directly replaces ICS2494-266.
Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.
All standard patterns shown above use 14.31818 MHz as the input reference frequency.
Order info: ICS2494M-XXX or ICS2494N-XXX (M= SOIC pkg., N= DIP pkg., XXX= Pattern number)
ICS2494AM-XXX or ICS2494AN-XXX (M= SOIC pkg., N= DIP pkg., XXX= Pattern number)

ICS Part Number	ICS2494A-305	ICS2494-306	ICS2494-314	ICS2494A-319	ICS2494A-320	ICS2494A-322	ICS2494A-324
Compatible VGA Chipsets	S3 86C924	Cirrus Logic GD6410 GD6412	Texas Instruments		AdvanceLogic ALG2101 ALG2201		Tseng Labs ET4000 ET4000 W32
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	25.175	XTAL	12.273	25.175	50.350	20.000	50.000
1	28.322	65.000	13.500	28.322	56.644	20.480	56.644
2	40.000	EXTFREQ	14.750	40.000	89.800	24.576	65.000
3	EXTFREQ	36.000	25.175	72.000	72.000	24.704	72.000
4	50.000	25.175	28.322	50.000	75.000	25.216	80.000
5	77.000	28.322	36.000	77.500	65.000	25.248	89.800
6	36.000	24.000	40.000	36.000	63.000	25.600	63.000
7	44.889	40.000	44.900	44.900	80.000	26.000	75.000
8	130.000	44.900	50.000	63.000	57.272	28.800	83.078
9	120.000	50.350	64.000	100.000	85.000	29.491	93.463
A	80.000	16.257	75.000	80.000	94.000	30.720	100.000
B	31.500	32.514	80.000	31.500	96.000	32.768	104.000
C	110.000	56.644	100.000	110.000	100.000	33.6000	108.000
D	65.000	20.000	108.000	65.000	108.000	44.736	120.000
E	75.000	41.539	120.000	75.000	110.000	9.600	130.000
F	94.500	80.000	135.000	94.500	77.000	20.500	134.700
Memory Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	55.000	32.900	32.000	48.000	76.000	15.360	50.000
1	75.000	35.600	40.000	52.500	80.000	13.947	56.000
2	70.000	43.900	48.000	55.000	85.000	13.947	60.000
3	80.000	39.900	60.000	50.000	90.000	24.000	65.000

*1 ICS2494A-310 directly replaces ICS2494-236.
*2 ICS2494A-304 directly replaces ICS2494-237.
*3 ICS2494A-317 directly replaces ICS2494-244.
*4 ICS2494A-318 directly replaces ICS2494-266.
Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.
All standard patterns shown above use 14.31818 MHz as the input reference frequency.
Order info: ICS2494M-XXX or ICS2494N-XXX (M= SOIC pkg., N= DIP pkg., XXX= Pattern number)
ICS2494AM-XXX or ICS2494AN-XXX (M= SOIC pkg., N= DIP pkg., XXX= Pattern number)

ICS Part Number	ICS2494-325	ICS2494-326	ICS2494-330	ICS2494-334	ICS2494-	ICS2494	ICS2494-
Compatible VGA Chipsets	Maxtek						
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	25.175	66.000	18.432	25.175			
1	28.322	62.000	31.470	28.322			
2	31.500	61.236	50.000	31 500			
3	36.000	61.000	EXTFREQ	36.000			
4	40.000	60.500	48.000	40.000			
5	44.900	60.000	54.000	44.900			
6	50.350	59.300	59.200	50 000			
7	65.000	59.000	75 500	65.000			
8	56.644	58.968	96.000	75.000			
9	72.00	57.200	108.778	77 500			
A	75.000	56.200	73.410	80.000			
B	77.000	55.500	50.490	90.000			
C	80.000	40.000	110.439	100.000			
D	94.500	38.200	100.000	110.000			
E	120.000	32.500	125.000	126.000			
F	108.000	30.500	135.000	135.000			
Memory Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	45.000	48.000	47.720	60.000			
1	50.000	50.000	45.000	50.000			
2	65.000	40.000	40.000	55.000			
3	70.000	60.000	50.000	50.000			

*1 ICS2494A-310 directly replaces ICS2494-236.
*2 ICS2494A-304 directly replaces ICS2494-237.
*3 ICS2494A-317 directly replaces ICS2494-244.
*4 ICS2494A-318 directly replaces ICS2494-266.
Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.
All standard patterns shown above use 14.31818 MHz as the input reference frequency.
Order info: ICS2494M-XXX or ICS2494N-XXX (M= SOIC pkg., N= DIP pkg., XXX= Pattern number)
ICS2494AM-XXX or ICS2494AN-XXX (M= SOIC pkg., N= DIP pkg., XXX= Pattern number)

Integrated
Circuit
Systems, Inc.

Dual Video/Memory Clock Generator

Features

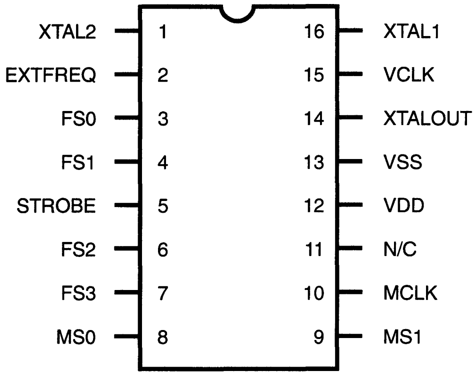
- Low cost - eliminates need for multiple crystal clock oscillators in video display subsystems
- Mask-programmable frequencies
- Pre-programmed versions for Industry Standard VGA chips
- Glitch-free frequency transitions
- Internal clock remains locked when the external frequency input is selected
- Low power CMOS device technology
- Small footprint - 16-pin DIP or SOIC
- Buffered Xtal Out
- Integral Loop Filter components
- Fast acquisition of selected frequencies, strobed or non-strobed
- Guaranteed performance up to 135 MHz
- Excellent power supply rejection
- Advanced PLL for low phase-jitter
- Frequency change detection circuitry enhances new frequency acquisition and eliminates problems caused by programs that rewrite frequency information

Description

The **ICS2495** Clock Generator is an integrated circuit dual phase-locked loop frequency synthesizer capable of generating 16 video frequencies and 4 memory clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS2495** provides a low-power, small-footprint, low-cost solution to the generation of video dot clocks. Outputs are compatible with **XGA**, **VGA**, **EGA**, **MCGA**, **CGA**, **MDA**, as well as the higher frequencies needed for advanced applications in desktop publishing and workstation graphics. Provision is made via a single level custom mask to implement customer specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

In addition to providing 16 clock rates, the **ICS2495** has provisions to multiplex an externally-generated signal source into the VCLK signal path. Internal phase-locked frequencies continue to remain locked at their preset values when this mode is selected. This feature permits instantaneous transition from an external frequency to an internally-generated frequency. Printed circuit board testing is simplified by the use of these modes as an external clock generated by the ATE tester can be fed through, permitting synchronous testing of the entire system.

Pin Configuration



16-Pin DIP or SOIC
K-4, K-6

Notes:
1. ICS2495M(SOIC) pinout is identical to ICS2495N(DIP).

Reference Oscillator & Crystal Selection

In cases where the on-chip crystal oscillator is used to generate the reference frequency, the accuracy of the crystal oscillation frequency will have a very small effect on output accuracy.

The external crystal and the on-chip circuit implement a Pierce oscillator. In a Pierce oscillator, the crystal is operated in its parallel-resonant (also called anti-resonant mode). This means that its actual frequency of oscillation depends on the effective capacitance that appears across the terminals of the quartz crystal. Use of a crystal that is characterized for use in a series-resonant circuit is fine, although the actual oscillation frequency will be slightly higher than the value stamped on the crystal can (typically 0.025%-0.05% or so). Normally, this error is not significant in video graphics applications, which is why the **ICS2495** will typically derive its frequency reference from a series resonant crystal connected between pins 1 and 16.

As the entire operation of the phase-locked loop depends on having a stable reference frequency, the crystal should be mounted as close as possible to the package. Avoid routing digital signals or the **ICS2495** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

Power Supply Conditioning

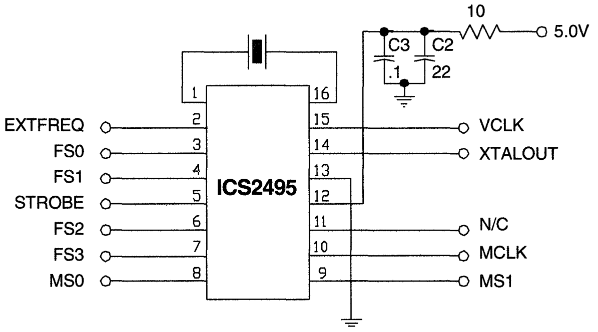
The **ICS2495** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in Figure 1.

Layout Considerations

Utilizing the **ICS2495** in video graphics adapter cards or on PS2 motherboards is simple, but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised to ensure that components not related to the **ICS2495** do not share its ground. In applications utilizing a multi-layer board, V_{SS} should be directly connected to the ground plane.

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate crystal should be connected between **XTAL1 (16)** and **XTAL2 (1)**. In IBM compatible applications this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10 MHz and 25 MHz have been tested. Maintain short lead lengths between the crystal and the **ICS2495**. In some applications, it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to **XTAL1 (16)**. If the signal amplitude is less than 3.5 volts, connect the clock through a .047 microfarad capacitor to **XTAL1 (16)**, and keep the lead length of the capacitor to **XTAL1 (16)** to a minimum to reduce noise susceptibility. This input is internally biased at $V_{DD}/2$. Since TTL compatible clocks typically guarantee a V_{OH} of only 2.8V, capacitively coupling the input restores noise immunity. The **ICS2495** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (1)** must be left open in this configuration.



NOTES: FS3-FS0, MS1-MS0, EXTFREQ, and STROBE inputs are all equipped with pull-ups and need not be tied high.
Mount decoupling capacitors as close as possible to the device and connect device ground to the ground plane where available.
Mount crystal and its circuit traces away from switching digital lines and the VCLK, MCLK and XTALOUT lines.

Figure 1

Buffered XTALOUT

In motherboard applications it may be desirable to have the **ICS2495** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. Depending on the load, it may be judicious to buffer XTALOUT when using it to provide the system clock.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **VCLK** or **MCLK** and other components in the system should be kept as short as possible. The **ICS2495** outputs have been designed to minimize overshoot. In addition, it may be helpful to place a ferrite bead in these signal paths to limit the propagation of high-order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS2495**. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may thereby reduce phase jitter as well as EMI.

External Frequency Sources

EXTFREQ on versions so equipped by the programming, is an input to a digital multiplexer. When this input is enabled by the FS0-3 selection, the signal driving pin 2 will appear at **VCLK (15)** instead of the PLL output. Internally, the PLL will remain in lock at the frequency selected by the ROM code.

The programming option also exists to output the crystal oscillator output on VCLK. In the case where XTAL1 is being driven by an external oscillator, then this frequency would appear on VCLK if so programmed.

Digital Inputs

FS0 (3), **FS1 (4)**, **FS2 (6)**, and **FS3 (7)**, are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (5)** when high, allows new data into the frequency select latches; and when low, prevents address changes per Figure 2. The internal power-on-clear signal will force an initial frequency code corresponding to an all zeros input state. **MS0 (8)** and **MS1 (9)** are the corresponding memory select inputs and are not strobed.

Pin Descriptions

The following table provides the pin description for the 16-pin **ICS2495** packages.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	XTAL2	OUT	Crystal interface
2	EXTFREQ	IN	External clock input (if so programmed)
3	FS0	IN	Control input for VCLK selection
4	FS1	IN	Control input for VCLK selection
5	STROBE	IN	Strobe for latching FS (0-3) (*High enable*)
6	FS2	IN	Control input for VCLK selection
7	FS3	IN	Control input for VCLK selection
8	MS0	IN	Select input for MCLK selection
9	MS1	IN	Select input for MCLK selection
10	MCLK	OUT	Memory Clock Output
11	N/C	-	Not Connected
12	VDD	-	Power
13	VSS	-	Ground
14	XTALOUT	OUT	Buffered Crystal Output
15	VCLK	OUT	Video Clock Output
16	XTAL1	IN	Reference input clock from system

Absolute Maximum Ratings

Ambient Temperature under bias	0 °C to 70 °C
Storage temperature	-40 °C to 125 °C
Voltage on all inputs and outputs with respect to V_{SS}	0.3 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (OV Ground). Positive current flows into the referenced pin.

Operating Temperature range	0 °C to 70 °C
Power supply voltage	4.75 to 5.25 Volts

DC Characteristics at 5 Volts V_{DD}

SYMBOL	PARAMETER		MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range		4.75	5.25	V	
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	$V_{DD} = 5V$
V_{IH}	Input High Voltage		2.0	V_{DD}	V	$V_{DD} = 5V$
I_{IH}	Input Leakage Current		-	10	μA	$V_{in} = V_{CC}$
V_{OL}	Output Low Voltage:	VCLK, MCLK	-	0.4	V	$I_{OL} = 8.0$ mA
		XTALOUT	-	0.4	V	$I_{OL} = 4.0$ mA
V_{OH}	Output High Voltage:	VCLK, MCLK	2.4	-	V	$I_{OH} = 8.0$ mA
		XTALOUT	2.4	-	V	$I_{OH} = 4.0$ mA
I_{DD}	Supply Current		-	30	mA	VDD = 5V
R_{UP}	Internal Pullup Resistors		50	-	K ohms	$V_{IN} = 0.0V$
C_{in}	Input Pin Capacitance		-	8	pF	$F_C = 1$ MHz
C_{out}	Output Pin Capacitance		-	12	pF	$F_C = 1$ MHz

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section.

1. REFCLK = 14.318 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns).
4. Maximum jitter within a range of 30 μs after triggering on a 400 MHz scope.
5. Rise and fall time between 0.8 and 2.0 VDC unless otherwise stated.
6. Output pin loading = 15pF.
7. Duty cycle measured at 1.4 volts.

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	10	-	
	MCLK and VCLK TIMINGS			
Tr	Rise Time	-	2	Duty Cycle 40% min. to 60% max.
Tf	Fall Time	-	2	
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	20	ns
-	Output Enable to Tristate (into and out of) time		15	ns

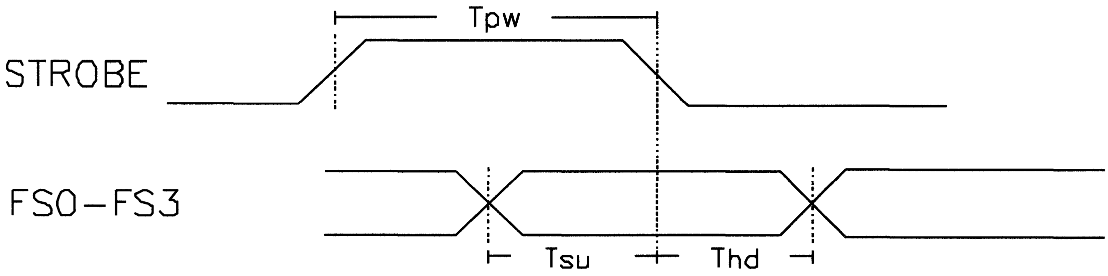


Figure 2

Ordering Information

ICS2495N-XXX or ICS2495M-XXX

Example:

ICS XXXX M -XXX

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type

N=DIP (Plastic)
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV=Standard Device; GSP=Genlock Device

ICS2495 Pattern Request Form

Custom patterns are also available, although a significant volume commitment and/or one-time mask charge will apply. Contact ICS sales for details.

ICS Part Number	ICS2495-	ICS2495-
Compatible VGA Chipsets	Custom Pattern # 1	Custom Pattern # 2
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)
0		
1		
2		
3		
4		
5		
6		
7		
8		
9		
A		
B		
C		
D		
E		
F		
Memory Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)
0		
1		
2		
3		

Custom pattern # 1 reference frequency = __________
Custom pattern # 2 reference frequency = __________
Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.
All standard patterns shown above use 14.31818 MHz as the input reference frequency.
If the internal frequency to which the ICS2495 remains locked to is critical when EXTFREQ is selected, it should be specified.
Order info: ICS2495M-XXX or ICS2495N-XXX (M= SOIC pkg., N= DIP pkg., XXX= Pattern number)

Integrated Circuit Systems, Inc.

ICS2496

Dual Voltage Video/Memory Clock Generator

Features

- Specified for dual voltage operation (VDD = 3.3V or 5V) but operates continuously from 3.0V to 5.25V
- Power-down input for extended battery life in portable applications
- Guaranteed performance up to 110 MHz (at 3.3V) or 135 MHz (at 5V)
- Advanced PLL for low phase-jitter
- Low power CMOS device technology
- Excellent power supply rejection
- Integral Loop Filter components
- Mask-programmable frequencies
- Small footprint - 16-pin DIP or SOIC
- Generates 16 video clock frequencies derived from a 14.318 MHz system clock reference frequency
- Provision for external frequency input
- Video clock is selectable among the 16 internally generated clocks, one external clock, or the buffered crystal oscillator
- Internal clock remains locked when the external frequency input is selected
- On-chip generation of four memory clock frequencies
- Patented technique eliminates cross-interference between video and memory clocks
- Fast acquisition of selected frequencies, strobed or non-strobed

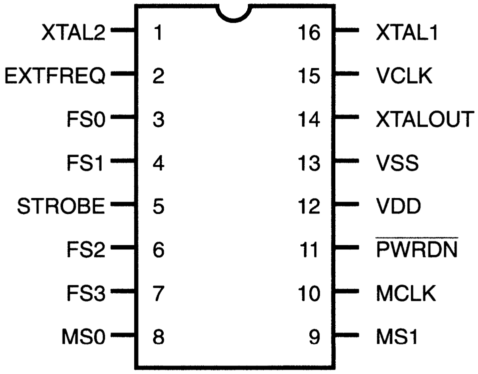
Description

The **ICS2496** has been specifically designed to serve the portable PC market with operation at either 3.3V or 5V with a comprehensive power-saving shut down mode.

The **ICS2496** Clock Generator is a dual phase-locked loop frequency synthesizer capable of generating 16 video frequencies and four memory clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS2496** provides a low power, small footprint, low cost solution to the generation of video dot clocks. Provision is made via a single level custom mask to implement customer specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

In addition to providing 16 clock rates, the **ICS2496** has provisions to multiplex an externally-generated signal source into the **VCLK** signal path. Internal phase-locked frequencies continue to remain locked at their preset values when this mode is selected. This feature permits instantaneous transition from an external frequency to an internally-generated frequency. Printed circuit board testing is simplified by the use of these modes, as an external clock generated by the ATE tester can be fed through, permitting synchronous testing of the entire system.

Pin Configuration



16-Pin DIP or SOIC
K-4, K-6

Notes:
1. ICS2496M(SOIC) pinout is identical to ICS2496N(DIP).

Circuit Function and Application

"Power-down"

The **ICS2496** has been optimized for use in battery operated portables. It can be placed in a power-down mode which drops its supply current requirement below 1 microamp. When placed in this mode, the digital inputs FS0-3, STROBE, MS0-1, and EXTFREQ may be either high or low or floating without causing an increase in the **ICS2496** supply current.

The PWRDN pin must be low (It has an internal pull-down.) in order to place the device in its low power state. The output pins (VCLK and MCLK) are driven high and XTALOUT is driven low by the **ICS2496** when it is in its low power state.

If a crystal is being used, nothing needs to be done to achieve low power. If XTAL1 is being driven by an external source, it may be driven low or high without a power penalty. If XTAL1 is at an intermediate voltage (V_{SS} +0.5V < V_{IN} < V_{DD} -0.5), there will be a small increase in supply current. If XTAL1 is driven at 14.318 MHz while the chip is in power-down, the **ICS2496** supply current will increase to approximately 1.2 mA.

The STROBE (pin 5) may be used to guard against inadvertent frequency changes during power-down/power-up sequences. By holding the STROBE low during power-down and power-up sequences, the **ICS2496** will retain the most recent video frequency selection.

Reference Oscillator and Crystal Selection

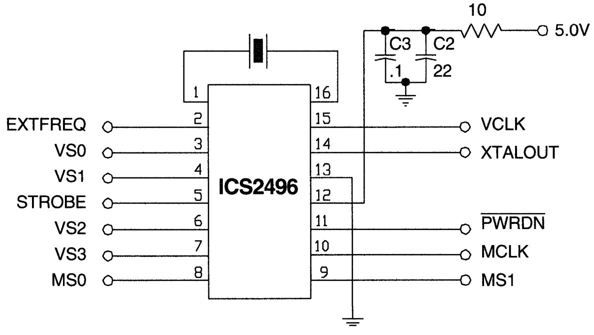
In cases where the on-chip crystal oscillator is used to generate the reference frequency, the accuracy of the crystal oscillation frequency will have a very small effect on output accuracy.

The external crystal and the on-chip circuit implement a Pierce oscillator. In a Pierce oscillator, the crystal is operated in its parallel-resonant (also called anti-resonant) mode. This means that its actual frequency of oscillation depends on the effective capacitance that appears across the terminals of the quartz crystal. Use of a crystal that is characterized for use in a series-resonant circuit is fine, although the actual oscillation frequency will be slightly higher than the value stamped on the crystal can (typically 0.025%-0.05% or so). Normally, this error is not significant in video graphics applications, which is why the **ICS2496** will typically derive its frequency reference from a series-resonant crystal connected between pins 1 and 16.

As the entire operation of the phase-locked loop depends on having a stable reference frequency, the crystal should be mounted as close as possible to the package. Avoid routing digital signals or the **ICS2496** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

Power Supply Conditioning

The **ICS2496** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in Figure 1.



NOTES: FS3-FS0, MS1-MS0, EXTFREQ, and STROBE inputs are all equipped with pull-ups and need not be tied high.
PWRDN input has an internal pull-down and must be driven or tied high for full device function
Mount decoupling capacitors as close as possible to the device and connect device ground to the ground plane where available.
Mount crystal and its circuit traces away from switching digital lines and the VCLK, MCLK, and XTALOUT lines.

Figure 1

Layout Considerations

Utilizing the **ICS2496** in video graphics adapter cards or on PS2 motherboards is simple, but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised in ensuring that components not related to the **ICS2496** do not share its ground. In applications utilizing a multi-layer board, V_{SS} should be connected directly to the ground plane.

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate crystal should be connected between **XTAL1 (16)** and **XTAL2 (1)**. In IBM-compatible applications this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10 MHz and 25 MHz have been tested. Maintain short lead lengths between the crystal and the **ICS2496**. In some applications, it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to **XTAL1 (16)**. If the signal amplitude is less than 3.5 volts, connect the clock through a .047 microfarad capacitor to **XTAL1 (16)**, and keep the lead length of the capacitor to **XTAL1 (16)** to a minimum to reduce noise susceptibility. This input is internally biased at $V_{DD}/ 2$. Since TTL compatible clocks typically guarantee a V_{OH} of only 2.8V, capacitively coupling the input restores noise immunity. The **ICS2496** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (1)** must be left open in this configuration.

Buffered XTALOUT

In motherboard applications it may be desirable to have the **ICS2496** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. Depending on the load, it may be judicious to buffer XTALOUT when using it to provide the system clock.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **VCLK** or **MCLK** and other components in the system should be kept as short as possible. The **ICS2496** outputs have been designed to minimize overshoot. In addition, it may be helpful to place a ferrite bead in these signal paths to limit the propagation of high order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS2496**. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may thereby reduce phase-jitter as well as EMI.

External Frequency Sources

EXTFREQ on versions so equipped by the programming, is an input to a digital multiplexer. When this input is enabled by the FS0-3 selection, the signal driving pin 2 will appear at **VCLK (15)** instead of the PLL output. Internally, the PLL will remain in lock at the frequency selected by the ROM code.

The programming option also exists to output the crystal oscillator output on VCLK. In the case where XTAL1 is being driven by an external oscillator, then this frequency would appear on VCLK if so programmed.

Digital Inputs

FS0 (3), **FS1 (4)**, **FS2 (6)**, and **FS3 (7)**, are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (5)**, when high, allows new data into the frequency select latches; and when low, prevents address changes per Figure 2. The internal power-on-clear signal will force an initial frequency code corresponding to an all-zeros input state. **MS0 (8)** and **MS1 (9)** are the corresponding memory select inputs and are not strobed.

Pin Descriptions

The following table provides the pin description for the 16-pin **ICS2496** packages:

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	XTAL2	OUT	Crystal interface
2	EXTFREQ	IN	External clock input (if so programmed)
3	FS0	IN	Control input for VCLK selection
4	FS1	IN	Control input for VCLK selection
5	STROBE	IN	Strobe for latching FS (0-3) (*High enable*)
6	FS2	IN	Control input for VCLK selection
7	FS3	IN	Control input for VCLK selection
8	MS0	IN	Select input for MCLK selection
9	MS1	IN	Select input for MCLK selection
10	MCLK	OUT	Memory Clock Output
11	PWRDN	IN	Power-down Control (low for power-down)
12	VDD	-	Power
13	VSS	-	Ground
14	XTALOUT	OUT	Buffered Crystal Output
15	VCLK	OUT	Video Clock Output
16	XTAL1	IN	Reference input clock from system

Absolute Maximum Ratings

Ambient Temperature under bias	0 °C to 70 °C
Storage temperature	-40 °C to 125 °C
Voltage on all inputs and outputs with respect to VSS	0.3 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Operating Temperature range	0 °C to 70 °C
Power supply voltage	3.0 to 5.25 Volts

DC Characteristics at 5 Volts V_{DD}

SYMBOL	PARAMETER		MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range		4.75	5.25	V	
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	$V_{DD} = 5V$
V_{IH}	Input High Voltage		2.0	V_{DD}	V	$V_{DD} = 5V$
I_{IH}	Input Leakage Current		-	10	µA	$V_{in} = V_{CC}$
V_{OL}	Output Low Voltage:	VCLK, MCLK	-	0.4	V	$I_{OL} = 8.0$ mA
		XTALOUT	-	0.4	V	$I_{OL} = 4.0$ mA
V_{OH}	Output High Voltage:	VCLK, MCLK	2.4	-	V	$I_{OH} = 8.0$ mA
		XTALOUT	2.4	-	V	$I_{OH} = 4.0$ mA
I_{DD}	Supply Current		-	30	mA	VDD = 5V
R_{UP}	Internal Pull-up Resistors		50	-	K ohms	$V_{IN} = 0.0V$
C_{in}	Input Pin Capacitance		-	8	pF	$F_C = 1$ MHz
C_{out}	Output Pin Capacitance		-	12	pF	$F_C = 1$ MHz
I_{PN}	Power-down Supply Current		-	1.0	µA	V_{DD}=3.3V
R_{DN}	Internal Pull-down Equivalent		20	-	K ohms	V_{IN}=V_{DD}=5V

DC Characteristics at 3.3 Volts V_{DD}

SYMBOL	PARAMETER		MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range		3.0	3.6	V	
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	$V_{DD} = 3.3V$
V_{IH}	Input High Voltage		2.0	V_{DD}	V	$V_{DD} = 3.3V$
I_{IH}	Input Leakage Current		-	10	µA	$V_{in} = V_{DD}$
V_{OL}	Output Low Voltage:	VCLK, MCLK	-	0.4	V	$I_{OL} = 3.0$ mA
		XTALOUT	-	0.4	V	$I_{OL} = 1.5$ mA
V_{OH}	Output High Voltage:	VCLK, MCLK	2.4	-	V	$I_{OH} = 3.0$ mA
		XTALOUT	2.4	-	V	$I_{OL} = 1.5$ mA
I_{DD}	Supply Current		-	20	mA	$V_{DD} = 3.3V$
R_{UP}	Internal Pull-up Resistors		100	-	K ohms	$V_{IN} = 0.0V$
C_{in}	Input Pin Capacitance		-	8	pF	$F_C = 1$ MHz
C_{out}	Output Pin Capacitance		-	12	pF	$F_C = 1$ MHz
I_{PN}	Power-down Supply Current		-	1.0	µA	V_{DD} =3.3V
R_{DN}	Internal Pulled-down Equivalent		50	-	K ohms	V_{IN} =V_{DD} =3.3V

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section:

1. REFCLK = 14.318 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns).
4. Maximum jitter is within a range of 30 µs after triggering on a 400 MHz scope.
5. Rise and fall time is between 0.8 and 2.0 VDC unless otherwise stated.
6. Output pin loading = 15pF
7. Duty cycle is measured at $V_{DD}/2$ unless otherwise stated.

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	10	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	2	-	
	MCLK and VCLK TIMINGS @ **5.0V**			
Tr	Rise Time	-	2	Duty Cycle 40% min. to 60% max.
Tf	Fall Time	-	2	
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	20	ns
-	Output Enable to Tristate (into and out of) time		15	ns
	MCLK and VCLK TIMINGS @ **3.3V**			
Tr	Rise Time	-	3	Duty Cycle 40% min. to 60% max.
Tf	Fall Time	-	3	
-	Frequency Error		.5	%
-	Maximum Frequency		110	MHz
-	Propagation Delay for Pass Through Frequency	-	30	ns
-	Output Enable to Tristate (into and out of) time		20	ns

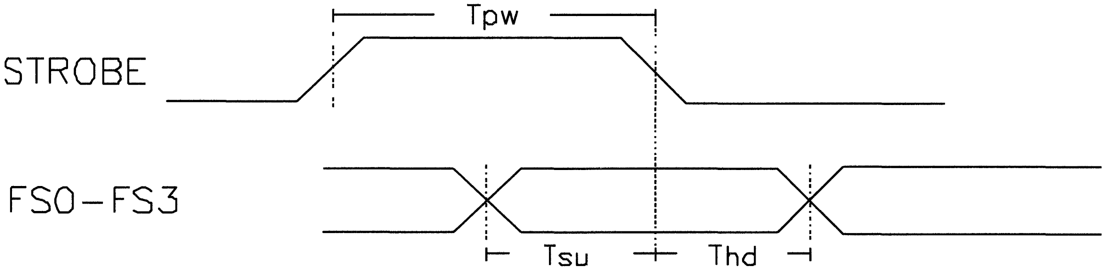


Figure 2

Ordering Information

ICS2496N-XXX or ICS2496M-XXX

Example:

ICS XXXX M -XXX

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type

N=DIP (Plastic)
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV=Standard Device; GSP=Genlock Device

ICS2496 Pattern Request Form

ICS produces a selection of standard pattern **ICS2496**'s pre-programmed for compatibility with many popular VGA chipsets. Custom patterns are also available, although a significant volume commitment and/or one-time mask charge will apply. Contact ICS sales for details.

ICS Part Number	ICS2496-452	ICS2496-454	ICS2496-456
Compatible VGA Chipsets	Cirrus Logic GD6410	Cirrus Logic GD6412	Motherboard Applications (CPU Clocks)
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	XTAL	XTAL	20.000
1	65.000	65.000	24.000
2	EXTFREQ	EXTFREQ	32.000
3	36.000	36.000	40.000
4	25.175	25.175	50.000
5	28.322	28.322	66.667
6	24.000	24.000	80.000
7	40.000	40.000	100.000
8	44.900	44.900	54.000
9	50.350	50.350	70.000
A	16.257	16.257	90.000
B	32.514	32.514	110.000
C	56.644	56.444	25.000
D	20.000	20.000	33.333
E	41.539	41.539	40.000
F	80.000	80.000	50.000
Memory Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	32.900	32.900	16.000
1	35.600	35.600	24.000
2	43.900	43.900	50.000
3	49.100	39.900	66.667

Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.
All standard patterns shown above use 14.31818 MHz as the input reference frequency.
Order info: ICS2496M-XXX or ICS2496N-XXX (M= SOIC pkg., N= DIP pkg., XXX= Pattern number)

Integrated
Circuit
Systems, Inc.

ICS2595

Advance Information

User-Programmable Dual High-Performance Clock Generator

Description

The **ICS2595** is a dual-PLL (phase-locked loop) clock generator specifically designed for high-resolution, high-refresh rate, video applications. The video PLL generates any of 16 pre-programmed frequencies through selection of the address lines **FS0-FS3**. Similarly, the auxiliary PLL can generate any one of four pre-programmed frequencies via the **MS0 & MS1** lines.

A unique feature of the **ICS2595** is the ability to redefine frequency selections in both the VCLK and MCLK synthesizers after power-up. This permits complete set-up of the frequency table upon system initialization.

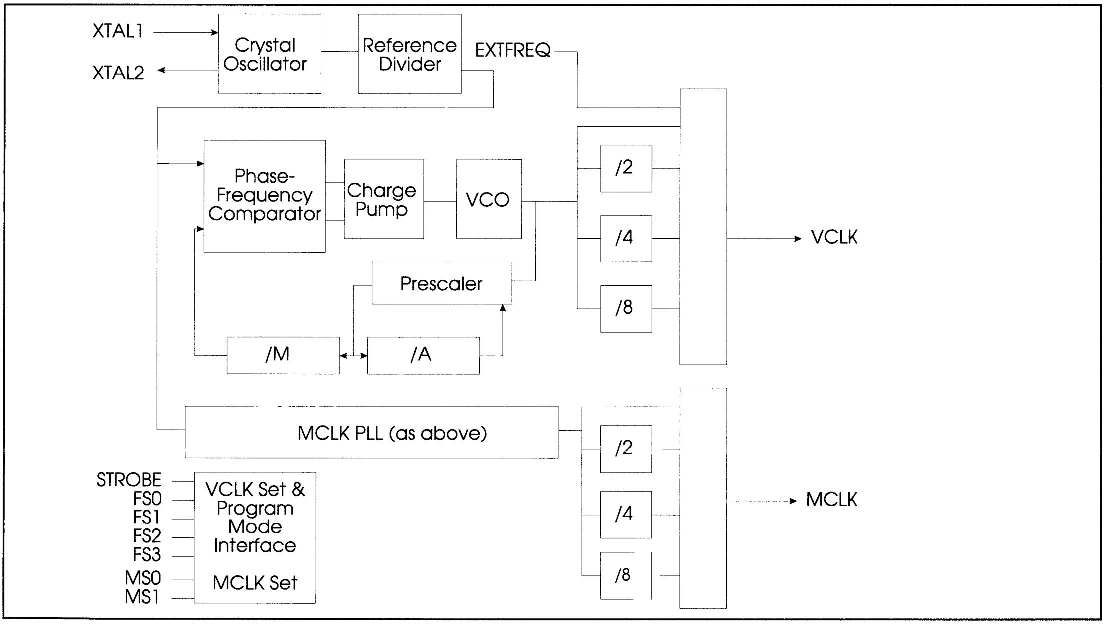
Features

- Advanced ICS monolithic phase-locked loop technology for extremely low jitter
- Supports high-resolution graphics - **VCLK** output to 145 MHz
- Completely integrated - requires only external crystal (or reference frequency and decoupling)
- Powerdown modes support portable computing
- Sixteen selectable **VCLK** frequencies (all user re-programmable)
- Four selectable **MCLK** frequencies (all user re-programmable)

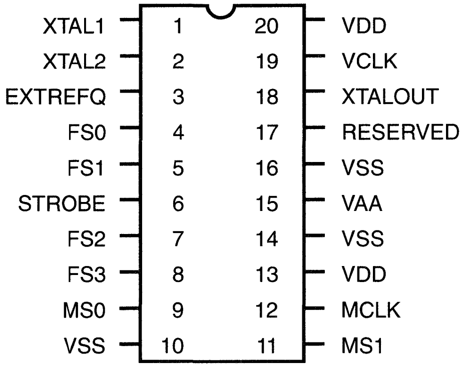
Applications

- PC Graphics
- VGA/Super VGA/XGA Applications

Block Diagram



Pin Configuration



20-Pin DIP or SOIC
K-4, K-7

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	XTAL1	A	Quartz crystal connection 1/Reference Frequency Input.
2	XTAL2	A	Quartz crystal connection 2.
3	EXTFREQ	I	External Frequency Input
4	FS0	I	VCLK PLL Frequency Select LSB.
5	FS1	I	VCLK PLL Frequency Select Bit.
7	FS2	I	VCLK PLL Frequency Select Bit.
8	FS3	I	VCLK PLL Frequency Select MSB.
6	STROBE	I	Control for Latch of VCLK Select Bits (FS0-FS3).
9	MS0	I	MCLK PLL Frequency Select LSB.
11	MS1	I	MCLK PLL Frequency Select MSB.
19	VCLK	O	VCLK Frequency Output
18	XTALOUT	O	Buffered Referenced Clock Output
12	MCLK	O	MCLK Frequency Output
17	RESERVED	-	Must Be Connected to VSS.
10, 14, 16	VSS	P	Device Ground. All pins must be connected.
13, 20	VDD	P	Output Stage Vdd. All pins must be connected.
15	VAA	P	Synthesizer Vdd.

Digital Inputs

The **FS0-FS3** pins and the **STROBE** pin are used to select the desired operating frequency of the **VCLK** output from the 16 pre-programmed/user-programmed selections in the **ICS2595**. These pins are also used to load new frequency data into the registers.

The standard interface for the **ICS2595** matches the interface of the industry standard ICS2494. That is, the FS0-FS3 inputs access the device internals transparently when the STROBE pin is high.

Optional configurations of the **STROBE** input include: positive-edge triggered, negative-edge triggered, and low-level transparent (See Ordering Information).

VCLK Output Frequency Selection

To change the **VCLK** output frequency, simply write the appropriate data to the **ICS2595 FS** inputs. Do not perform any further writes to the device for at least 50 milliseconds (assumes a 14.318 MHz reference). The synthesizer will output the new frequency programmed into that location after a brief delay (see time-out specifications).

Upon device power-up, the selected frequency will be the frequency pre-programmed into address 0 until a device write is performed.

MCLK Output Frequency Selection

The MS0-MS1 pins are used to directly select the desired operating frequency of the MCLK output from the four pre-programmed/user-programmed selections in the **ICS2595**. These inputs are not latched, nor are they involved with memory programming operations.

Programming Mode Selection

A programming sequence is defined as a period of at least 50 milliseconds (assumes 14.318 MHz reference) of no data writes to the **ICS2595** (to clear the shift register) followed by a series of data writes (as shown here):

FS0	FS1	FS2	FS3
X	X	**START** bit (must be "0")	0
X	X	”	1
X	X	**R/W*** control	0
X	X	”	1
X	X	**LO** (location LSB)	0
X	X	”	1
X	X	**L1**	0
X	X	”	1
X	X	**L2**	0
X	X	”	1
X	X	**L3**	0
X	X	”	1
X	X	**L4** (location MSB)	0
X	X	”	1
X	X	**N0** (feedback LSB)	0
X	X	”	1
X	X	**N1**	0
X	X	”	1
X	X	**N2**	0
X	X	”	1
X	X	**N3**	0
X	X	”	1
X	X	**N4**	0
X	X	”	1
X	X	**N5**	0
X	X	”	1
X	X	**N6**	0
X	X	”	1
X	X	**N7** (feedback MSB)	0
X	X	”	1
X	X	**EXTFREQ** bit (selected if "1")	0
X	X	”	1
X	X	**D0** (post-divider LSB)	0
X	X	”	1
X	X	**D1** (post-divider MSB)	0
X	X	”	1
X	X	**STOP1** bit (must be "1")	0
X	X	”	1
X	X	**STOP2** bit (must be "1")	0
X	X	”	1

Observe that the internal shift register is "clocked" by a transition of **FS3** data from "0" to "1." If an extended sequence of register loading is to be performed (such as a power-on initialization sequence), note that it is not necessary to implement the 50 millisecond delay between them. Simply repeat the sequence above as many times as desired. Writes to the FS port will not be treated as frequency select data until up to 50 milliseconds have transpired since the last write. Note that FS0 and FS1 inputs are "don't care."

Data Description

Location Bits (L0-L4)

The first five bits after the start bit control the frequency location to be re-programmed according to this table. The rightmost bit (the LSB) of the five shown in each selection of the table is the first one sent.

Table 1 - Location Bit Programming

L[4-0]	LOCATION
00000	VCLK Address 0
00001	VCLK Address 1
00010	VCLK Address 2
00011	VCLK Address 3
00100	VCLK Address 4
00101	VCLK Address 5
00110	VCLK Address 6
00111	VCLK Address 7
01000	VCLK Address 8
01001	VCLK Address 9
01010	VCLK Address 10
01011	VCLK Address 11
01100	VCLK Address 12
01101	VCLK Address 13
01110	VCLK Address 14
01111	VCLK Address 15
10000	MCLK Address 0
10001	MCLK Address 1
10010	MCLK Address 2
10011	MCLK Address 3

Feedback Set Bits (N0-N7)

These bits control the feedback divider setting for the location specified. The modulus of the feedback divider will be equal to the value of these bits + 257. The least significant bit (N0) is sent first.

Post-Divider Set Bits (D0-D1)

These bits control the post-divider setting for the location specified according to this table. The least significant bit (D0) is sent first.

Table 2 - Post-Divider Programming

D[1-0]	POST-DIVIDER
00	8
01	4
10	2
11	1

Read/Write* Control Bit

When set to a "0," the **ICS2595** shift register will transfer its contents to the selected memory register at the completion of the programming sequence outlined above.

When this bit is a "1," the selected memory location will be transferred to the shift register to permit a subsequent readback of data. No modification of device memory will be performed.

To readback any location of memory, perform a "dummy" write of data (complete with start and stop bits) to that location but set the **R/W*** control bit (make it "1"). At the end of the sequence (i.e. after the stop bits have been "clocked"), "clocking" of the FS3 input 11 more times will output the data bits only in the same sequence as above on the FS0 pin.

EXTFREQ Input

The **EXTFREQ** input allows an externally generated frequency to be routed to the VCLK or MCLK output pins under device programming control. If the EXTFREQ bit is set (logic "1") at the selected address location, the frequency applied to the **EXTFREQ** input will be routed to the output instead of the frequency generated by the **VCLK** (or MCLK) PLL.

When setting the EXTFREQ bit to a "1," be sure that the D0 and D1 bits are not both set to "1" also, unless it is intended that the phase-locked loop be shutdown as well.

Power Conservation

The **ICS2595** supports power conservation by permitting either or both of the phase-locked loops to be disabled. This can be done by programming a particular address to have EXTFREQ, D0, & D1 bits set to a logic "1." Any frequency applied to the EXTFREQ pin will still be passed through the output multiplexer and appear at the respective output.The crystal oscillator is not affected by this power-down function and will continue to operate normally.

Frequency Synthesizer Description

Refer to Figure 1 for a block diagram of the **ICS2595**.

The **ICS2595** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL. The phase-frequency detector shown in the block diagram drives the VCO to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F_{VCO}=F_{XTAL1} * \frac{N}{R}$$

where N is the effective modulus of the feedback divider chain and R is the modulus of the reference divider chain.

The feedback divider on the **ICS2595** may be set to any integer value from 257 to 512. This is done by the setting of the **N0-N7** bits. The standard reference divider on the **ICS2595** is fixed to a value of 43 (this may be set to a different value via ROM programming; contact factory). The **ICS2595** is equipped with a post-divider and multiplexer that allows the output frequency range to be scaled down from that of the VCO by a factor of 2, 4, or 8.

Therefore, the VCO frequency range will be from 5.976 to 11.906 (257/43 to 512/43) of the reference frequency. The output frequency range will be from 0.747 to 11.906 times the reference frequency. Worst case accuracy for any desired frequency within that range will be 0.2%.

If a 14.31818 MHz reference is used, the output frequency range would be from 10.697 MHz to 170.486 MHz (but the upper end is first limited to 145 MHz by the **ICS2595** output driver).

Programming Example

Suppose that we want differential CLK output to be 45.723 MHz. We will assume the reference frequency to be 14.31818 MHz.

The VCO frequency range will be 85.565 MHz to 170.486 MHz (5.976 * 14.31818 to 11.906 * 14.31818). We will need to set the post-divider to two to get an output of 45.723 MHz.

The VCO will then need to be programmed to two times 45.723 MHz, or 91.446 MHz. To calculate the required feedback divider modulus we divide the VCO frequency by the reference frequency and multiply by the reference divider:

$$\frac{91.446}{14.31818}*43=274.62$$

which we round off to 275. The exact output frequency will be:

$$\frac{275}{43}*14.31818*\frac{1}{2}=45.784\text{ MHz}$$

The value of the **N** programming bits may be calculated by subtracting 257 from the desired feedback divider modulus. Thus, the **N** value will be set to 18 (275-257) or 00010010_2. The **D** bit programming is 10_2 (from Table 2).

Reference Oscillator & Crystal Selection

The **ICS2595** has on-board circuitry to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in parallel-resonant (also called anti-resonant mode). See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Crystals characterized for their series-resonant frequency may also be used with the **ICS2595**. Be aware that the oscillation frequency in circuit will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS2595** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

External Reference Sources

An external frequency source may be used as the reference for the VCLK and MCLK PLLs. To implement this, simply connect the reference frequency source to the XTAL1 pin of the **ICS2595**. For best results, insure that the clock edges are as clean and fast as possible and that the input voltage thresholds are not violated.

Power Supply

The **ICS2595** has three VSS pins to reduce the effects of package inductance. All pins are connected to the same potential on the die (the ground bus). ALL of these pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS2595** has two **VDD** pins which supply of +5 volt power to the output stages. These pins should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, use low-capacitors should have low series inductance and be mounted close to the **ICS2595**.

The VAA pin is the power supply for the synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects.

Absolute Maximum Ratings

Supply voltage	-.5V to +7V
Logic inputs	.5V to VDD +.5V
Ambient operating temp	0 to 70°C
Storage temperature	-85 to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TTL-Compatible Inputs						
(VS0-3, MS0-1, STROBE):						
Input High Voltage	V_{ih}		2.0		VDD=0.5	V
Input Low Voltage	V_{il}		VSS-0.5		0.8	V
Input High Current	I_{ih}				10	uA
Input Low Current	I_{il}				200	uA
Input Capacitance	C_{in}				8	pF
XTAL1:						
Input High Voltage	Vxh		VDD*0.75		VDD+0.5	V
Input Low Voltage	Vxl		VSS-0.5		VDD*0.25	V
VCLK, MCLK Outputs:						
Output High Voltage	Voh		2.4			V
@Ioh=0.4mA						
Output Low Voltage	Vol				0.4	V
@Iol=8.0mA						

AC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Phase-Locked Loop:						
VCLK, MCLK VCO Frequency	Fvco		60		185	MHz
PLL Acquire Time	T_{lock}			500		uSec
Crystal Oscillator						
Crystal Frequency Range	F_{xtal}		5		25	MHz
Parallel Loading Capacitance				20		pf
XTAL1 Minimum High Time	Txhi		8			nSec
XTAL1 Minimum low Time	Txlo		8			nSec
Power Supplies:						
VDD Supply Current	idd				35	mA
VAA Supply Current	Iaa				10	mA
Digital Outputs:						
VCLK, MCLK, XTALOUT Rise Time @Cload=20pf	Tr				2	nSec
VCLK, MCLK, STALOUT Fall Time @Cload=20pf	Tf				2	nSec

PATTERN	ICS2595-01			
Reference Divider	43			
VCLK ADDR	FbkDiv/PostDiv - F_{VCLK}(MHz)			
0	300/1- 99.89			
1	378/1 - 125.87			
2	277/1 - 92.24			
3	432/4 - 35.96			
4	302/2 - 50.28			
5	340/2 - 56.61			
6	EXTFREQ-			
7	270/2 - 44.95			
8	405/1 - 134.86			
9	384/4 - 31.97			
A	330/1 - 109.88			
B	481/2 - 80.08			
C	479/4 - 39.87			
D	270/2 - 44.95			
E	450/2 - 74.92			
F	390/2 - 64.93			
MCLK ADDR	FbkDiv/PostDiv - F_{MCLK}			
0	481/4 - 40.04			
1	270/2 - 44.95			
2	396/4 - 32.97			
3	300/2 - 49.95			

Ordering Information

ICS2595N-SXX or ICS2595M-SXX (0.300" DIP or SOIC Package)

Example:

ICS XXXX N -SXX

S=Strobe Option/XX=Default Frequencies

Package Type

N=DIP (Plastic)
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV=Standard Device; GSP=Genlock Device

Where:

"s" denotes strobe option:	A - positive level transparent (i.e., 2494 interface compatible)
"xx" denotes default frequencies:	B - negative level transparent
	C - positive edge triggered
	D - negative edge triggered

Integrated
Circuit
Systems, Inc.

ICS82C404

Advance Information

Dual Programmable Graphics Frequency Generator

Features

- **Pin for pin and function compatible with ICD's version of the 82C404**
- **Dual programmable graphics clock generator**
- **Memory and video clocks are individually programmable on-the-fly**
- **Ideal for designs where multiple or varying frequencies are required**
- **Increased frequency resolution from optional pre-divide by 2 on the M counter**
- **Output enable feature available for tri-stating outputs**
- **Independent clock outputs range from 390 kHz to 120 MHz**
- **Operation up to 140 MHz available**
- **Power-down capabilities**
- **Low power, high speed 0.8 µ CMOS technology**
- **Glitch-free transitions**
- **Available in 16 pin PDIP or SOIC package**

General Description

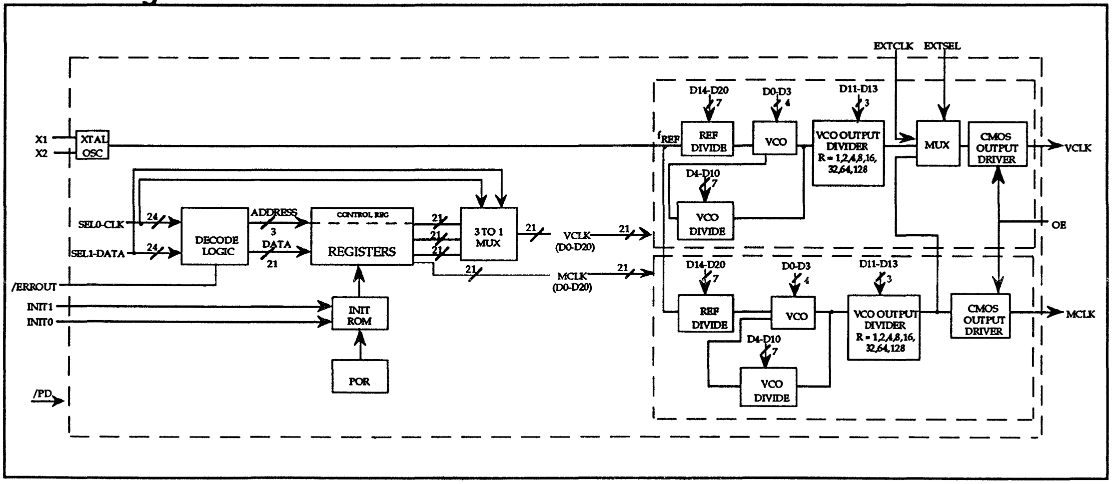
The ICS82C404 is a fully programmable graphics clock generator. It can generate user specified clock frequencies using an externally generated input reference or a single crystal. The output frequency is programmed by entering a 24 bit digital word through the serial port.

Two fully user-programmable phase-locked loops are offered in a single package. One PLL is designed to drive the memory clock, while the second drives the video clock. The outputs may be changed on-the-fly to any desired frequency between 390 kHz and 120 MHz. The ICS82C404 is ideally suited for any design where multiple or varying frequencies are required.

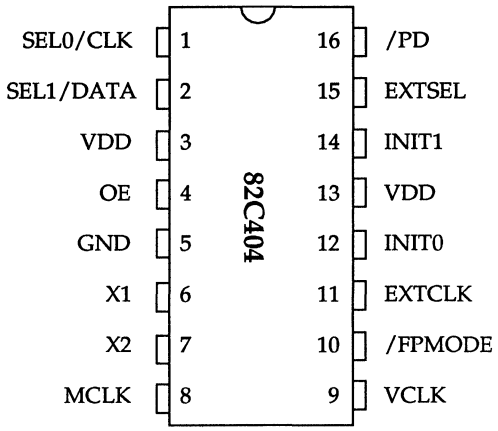
This part is ideal for graphics applications. It generates low jitter, high speed pixel clocks. It can be used to replace multiple, expensive high speed crystal oscillators. The flexibility of the device allows it to generate non-standard graphics clocks.

The leader in the area of multiple output clocks on a single chip, ICS has been shipping graphics frequency generators since October, 1990, and is constantly improving the phase locked loop. The ICS82C404 incorporates a patented fourth generation PLL that offers the best jitter performance available.

Block Diagram



Pin Configuration



16-Pin DIP or SOIC
K-4, K-6

Pin Description

Pin Name	Pin #	Description
SEL0-CLK	1	Clock input in serial programming mode Clock select pin in operating mode
SEL1-DATA	2	Data input in serial programming mode Clock select pin in operating mode
AVDD	3	Power
OE	4	Tri-states outputs when low
GND	5	Ground
X1	6	Crystal input
X2	7	Crystal output
MCLK	8	Memory clock output
VCLK	9	Video clock output
/FPMODE	10	Clock select input used to force REG2 programmed frequency
EXTCLK	11	External clock input
INIT0	12	Selects initial power-up conditions, LSB
VDD	13	Power
INIT1	14	Selects initial power-up conditions, MSB
EXTSEL	15	Selects external clock input (EXTCLK) as VCLK output
/PD	16	Power-down pin, active low

Register Definitions

The register file consists of the following six registers:

Register Addressing

Address	Register	Definition
000	REG0	Video Clock Register 1
001	REG1	Video Clock Register 2
010	REG2	Video Clock Register 3
011	MREG	Memory Register
100	PWRDWN	Divisor for Power-down mode
110	CNTL REG	Control Register

The ICS82C404 places the three video clock registers and the memory clock register in a known state upon power-up. The registers are initialized based on the state of the INIT1 and INIT0 pins at application of power to the device. The INIT pins must ramp up with VDD if a logical 1 on either pin is required. These input pins are internally pulled down and will default to a logical 0 if left unconnected.

The registers are initialized as follows:

Register Initialization

INIT1	INIT0	MREG	REG0	REG1	REG2
0	0	32.500	25.175	28.322	28.322
0	1	40.000	25.175	28.322	28.322
1	0	50.350	40.000	28.322	28.322
1	1	56.644	40.000	50.350	50.350

Register Selection

When the ICS82C404 is operating, the video clock output is controlled with a combination of the SEL0, SEL1, /PD, and OE pins. The video clock is also multiplexed to an external clock (EXTCLK) which can be selected with the EXTSEL pin. The VCLK Selection Table shows how VCLK is selected.

VCLK Selection

OE	/PD	EXTSEL	/FPMODE	SEL1	SEL0	VCLK
0	x	x	x	x	x	Tri-State
1	0	x	x	x	x	Forced High
1	1	x	1	0	0	REG0
1	1	x	1	0	1	REG1
1	1	0	1	1	0	EXTCLK
1	1	1	1	1	x	REG2
1	1	x	1	1	1	REG2
1	1	x	0	x	x	REG2

As seen in the table above, OE acts to tri-state the output. The /PD pin forces the VCLK signal high while powering down the part. The EXTCLK pin will only be multiplexed in when EXTSEL and SEL0 are logic 0 and SEL1 is a logic 1.

The memory clock outputs are controlled by /PD and OE as follows:

MCLK Selection

OE	/PD	MCLK
0	x	Tri-State
1	1	MREG
1	0	PWRDWN

The Clock Select pins SEL0 and SEL1 have two purposes. In serial programming mode, these pins act as the clock and data pins. New data bits come in on SEL1 and these bits are clocked in by a signal on SEL0. While these pins are acquiring new information, the VCLK signal remains unchanged. When SEL0 and SEL1 are acting as register selects, a timeout interval is required to determine whether the user is selecting a new register or wants to program the part. During this initial timeout, the VCLK signal remains at its previous frequency. At the end of this timeout interval, a new register is selected. A second timeout interval is required to allow the VCO to settle to its new value. During this period of time, typically 5 msec, the input reference signal is multiplexed to the VCLK signal.

When MCLK or the active VCLK register is being reprogrammed, then the reference signal is multiplexed glitch-free to the output during the first timeout interval. A second timeout interval is also required to allow the VCO to settle. During this period, the reference signal is multiplexed to the appropriate output signal.

Control Register Definition

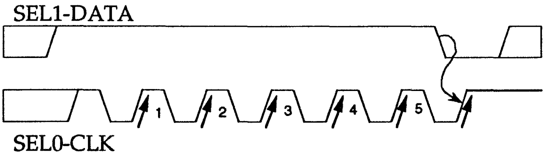
The control register allows the user to adjust various internal options. The register is defined as follows:

Bit	Bit Name	Default Value	Description
9	C5	0	This bit determines which power-down mode the /PD pin will implement. Power-down mode 1, C5 = 0, forces the MCLK signal to be a function of the power-down register. Power-down mode 2, C5 = 1, turns off the crystal and disables all outputs.
8	C4	0	This bit determines which clock is multiplexed to VCLK during frequency changes. C4 = 0 multiplexes the reference frequency to the VCLK output. C4 = 1 multiplexes MCLK to the VCLK output for applications where the graphics controller cannot run as slow as f_{REF}.
7	C3	0	This bit determines the length of the timeout interval. The timeout interval is derived from the MCLK VCO. If this VCO is programmed to certain extremes, the timeout interval maybe too short. C3 = 0, normal timeout. C3 = 1, doubled timeout interval.
6	C2	0	Reserved, must be set to 0.
5	C1	1	This bit adjusts the duty cycle. C1 = 0 causes a 1ns decrease in output high time. C1 = 1 causes no adjustment. If the load capacitance is high, the adjustment can bring the duty cycle closer to 50%.
4	C0	0	Reserved, must be set to 0.
3	NS2	0	Acts on register 2. NS2 = 0 prescales the N counter by 2. NS2 = 1 prescales the P counter value to 4.
2	NS1	0	Acts on register 1. NS1 = 0 prescales the N counter by 2. NS1 = 1 prescales the P counter value to 4.
1	NS0	0	Acts on register 0. NS0 = 0 prescales the P counter by 2. NS0 = 1 prescales the P counter value to 4.

Serial Programming Architecture

The pins SEL0 and SEL1 perform the dual functions of selecting registers and serial programming. In serial programming mode, SEL0 acts as a clock pin while SEL1 acts as the data pin. The ICS82C404-01 may not be serially programmed when in power-down mode.

In order to program a particular register, an unlocking sequence must occur. The unlocking sequence is detailed in the following timing diagram:



The unlock sequence consists of at least 5 low-to-high transitions of CLK while data is high, followed immediately by a single low-to-high transition while data is low. Following this unlock sequence, data can be loaded into the serial data register.

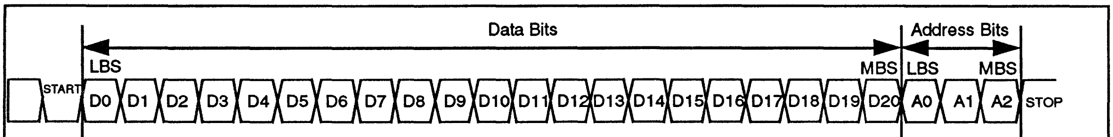
Following any transition of CLK or DATA, the watchdog timer is reset and begins counting. The watchdog timer ensures that successive rising edges of CLK and DATA do not violate the timeout specification of 2ms. If a timeout occurs, the lock mechanism is reset and the data in the serial data register is ignored. Since the VCLK registers are selected by the SEL0 and SEL1 pins, and since any change in their state may affect the output frequency, new data input on the selection bits is only permitted to pass through the decode logic after the watchdog timer has timed out. This delay of SEL0 or SEL1 data permits a serial program cycle to occur without affecting the current register selection.

Serial Data Register

The serial data is clocked into the serial data register in the order described in figure 1 below (Serial Data Timing).

The serial data is sent as follows: An individual data bit is sampled on the rising edge of CLK. The complement of the data bit must be sampled on the previous falling edge of CLK. The setup and hold time requirements must be met on both CLK edges. For specifics on timing, see the timing diagrams on pages 10, 11, and 12.

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit. A total of 24 bits must always be loaded into the serial data register or an error is issued. Following the entry of the last data bit, a stop bit or load command is issued by bringing DATA high and toggling CLK high-to-low and low-to-high. The unlocking mechanism then resets itself following the load. Only after a timeout period are the SEL0 and SEL1 pins allowed to return to a register selection function.



START	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	A0	A1	A2	STOP
BIT#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	BIT#
VCO Prog-Word	M'0	M'1	M'2	M'3	M'4	M'5	M'6	R0	R1	R2	N'0	N'1	N'2	N'3	N'4	N'5	N'6	I0	I1	12	13	A0	A1	0	VCO Prog-Word
CNTL Reg	0	0	0	0	0	0	0	0	0	0	0	0	PS0	PS1	PS2	C0	C1	C2	C3	C4	C5	0	1	1	CNTL Reg
PWRDWN Reg	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P0	P1	P2	P3	0	0	1	PWRDWN Reg

Figure 1 - Serial Data Timing

The serial data register is exactly 24 bits long, enough to accept the data being sent. The stop bit acts as a load command that passes the contents of the Serial Data Register into the register indicated by the three address bits. If a stop bit is not received after the serial register is full, and more data is sent, all data in the register is ignored and an error issued. If correct data is received, then the unlocking mechanism rearms, all data in the serial data register is ignored, and an error is issued.

Programming the ICS82C404

The ICS82C404 has a wide operating range, but it is recommended that it is operated within the following limits:

1 MHz < F_{REF} < 60 MHz	F_{REF} = Input Reference Frequency
200 KHz < $F_{REF/M}$ < 5 MHz	M = Reference divide 3 to 129
50 MHz < F_{VCO} < 120 MHz	F_{VCO} = VCO output frequency
$F_{CLK} \leq$ 120 MHz	F_{CLK} = output frequency

The frequency of the programmable oscillator F_{VCO} is determined by the following fields:

Field	# of Bits
Index (I)	4
N counter value (N')	7
Mux (R)	3
M counter value (M')	7

Where the least significant bit is the last bit of M and the most significant bit is the first bit of I.

The equations used to determined the oscillator frequency are:

$$N = N' + 3 \qquad M = M' + 2$$

$$F_{VCO} = \text{Prescale} \cdot N/M \cdot F_{CLK}$$

$$\text{where } 3 \leq M \leq 129 \text{ and } 4 \leq N \leq 130$$

$$\text{and prescale} = 2 \text{ or } 4\text{, as set in the control register}$$

The value of F_{VCO} must remain between 50 MHz and 120 MHz. As a result, for output frequencies below 50MHz, F_{VCO} must be brought into range. To achieve this, an output divisor is selected by setting the values of the Mux Field (R) as follows:

Output Divisor

R	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

Unlike the ICD's 82C404, the ICS82C404's VCO does not require tuning to place it in certain ranges. The ICS82C404's VCO will operate from 50 MHz to 120 MHz without adjusting the VCO gain. However, to maintain compatibility, the I bits are programmed as in the ICD2061A.

These bits are dummy bits except for the following two cases:

Index Field (I)

I	VCLK F_{VCO}	MCLK F_{VCO}
1110	Turn off VCLK	50-120 MHz
1111	Mux MCLK to VLCK	50-120 MHz

When the index field is set to 1111, VCLK is turned off and both channels run from the same MCLK VCO. This is done in an effort to reduce jitter, which may increase when VCOs run at 2^n multiples of one another. If the two outputs must be multiples of one another, it is best to mux MCLK over to the output of the VCLK VCO, and to power-down the VCLK VCO. The multiplexed frequency will be divided down by the correct divisor (M) and output on VCLK.

Power Management Issues

Power-down mode 1

The ICS82C404 contains a mechanism to reduce the quiescent power when stand-by operation is desired. Power-down mode 1 is invoked by pulling /PD low and having the proper CNTL register bit set to zero. In this mode, VCOs are shut down, the VCLK output is forced high, and the MCLK output is set to a user-defined low frequency value to refresh dynamic RAM.

The power-down MCLK value is determined by the following equation:

$MCLK_{PD} = F_{REF}$ / (PWRDWN register divisor value)

The power-down register divisor is determined according to the 4-bit word programmed into the PWRDWN register (see table below).

Power-down mode 2

When there is no need for any output during power-down, an alternate mode is available which will completely shut down all outputs and the reference oscillator, but still preserves all register contents. Power-down mode 2 is invoked by first programming the power-down bit in the CNTL register and then pulling the /PD pin low.

The /PD pin

The /PD pin has a standard internal pull-up resistor during normal operation. When the chip goes into power-down mode 1 or 2, the normal pull-up resistor is dynamically switched to a weak pull-up, which reduces power consumption. If the /PD pin is allowed to float after it has been pulled down, the weak pull-up will bring the signal high and allow the device to resume operation.

Power Down Register Code

PWRDWN bits P3	P2	P1	P0	PWRDWN Register Value	Power-down Divisor	$MCLK_{PD}$ (f_{REF}=14.31818)
0	0	0	0	0	n/a	n/a
0	0	0	1	1	32	447.4 KHz
0	0	1	0	2	30	477.3 KHz
0	0	1	1	3	28	511.4 KHz
0	1	0	0	4	26	550.7 KHz
0	1	0	1	5	24	596.6 KHz
0	1	1	0	6	22	650.8 KHz
0	1	1	1	7	20	715.9 KHz
1	0	0	0	8 (default)	18	795.5 KHz
1	0	0	1	9	16	894.9 KHz
1	0	1	0	A	14	1.02 MHz
1	0	1	1	B	12	1.19 MHz
1	1	0	0	C	10	1.43 MHz
1	1	0	1	D	8	1.79 MHz
1	1	1	0	E	6	2.39 MHz
1	1	1	1	F	4	3.58 MHz

Absolute Maximum Ratings

VDD referenced to GND..7V
Operating temperature under bias............. 0°C to +70°C

Storage temperature................................ -40°C to +150°C
Voltage on I/O pins referenced to GND...... GND -0.5V to VDD +0.5V
Power dissipation.. 0.5 Watts

Note: Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

Electrical Characteristics

(VDD= +5V ± 5%, 0°C ≤ $T_{AMBIENT}$ ≤ +70°C unless otherwise stated)

Device Specifications

Maximum Ratings

Name	Description	Min	Max	Units
VDD	Supply voltage relative to GND	-0.5	7.0	Volts
V_{IN}	Input voltage with respect to GND	-0.5	VDD + 0.5	Volts
T_{OPER}	Operating temperature	0	+70	°C
T_{STOR}	Storage temperature	-65	+150	°C
T_{SOL}	Max soldering temperature (10 sec)		+260	°C
T_j	Junction temperature		+125	°C
P_{DISS}	Package power dissipation		350	mWatts

DC Characteristics

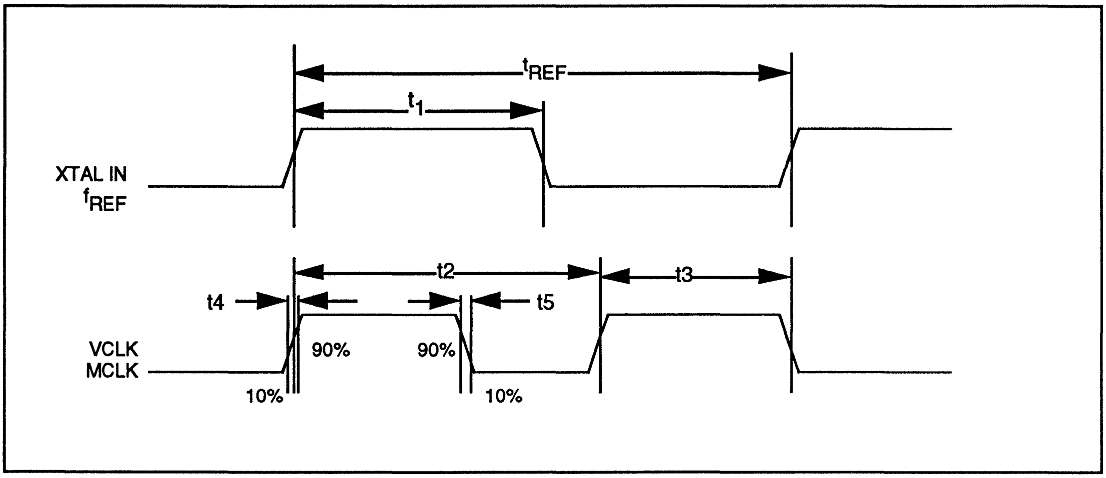
Name	Description	Min	Typ	Max	Units	Conditions
V_{IH}	High level input voltage	2.0			V	
V_{IL}	Low level input voltage			0.8	V	
V_{OH}	High level CMOS ouput voltage	3.84			V	I_{OH} = -4 ma
V_{OL}	Low level output voltage			0.4	V	I_{OL} = 4 ma
I_{IH}	Input high current			100	µa	V_{IH} = 5.25 V
I_{IL}	Input low current			-250	µa	V_{IL} = 0V
I_{OZ}	Output leakage current			10	µa	(tri-state)
I_{DD}	Power supply current	15		65	ma	
I_{DD-TYP}	Power supply current (typical)		35		ma	@60 MHz
I_{ADD}	Analog power supply current			10	ma	
I_{PD1}	Power-down current (Mode 1)		6	7.5	ma	
I_{PD2}	Power-down current (Mode 2)		25	50	µa	
C_{IN}	Input capacitance			10	pf	

AC Characteristics

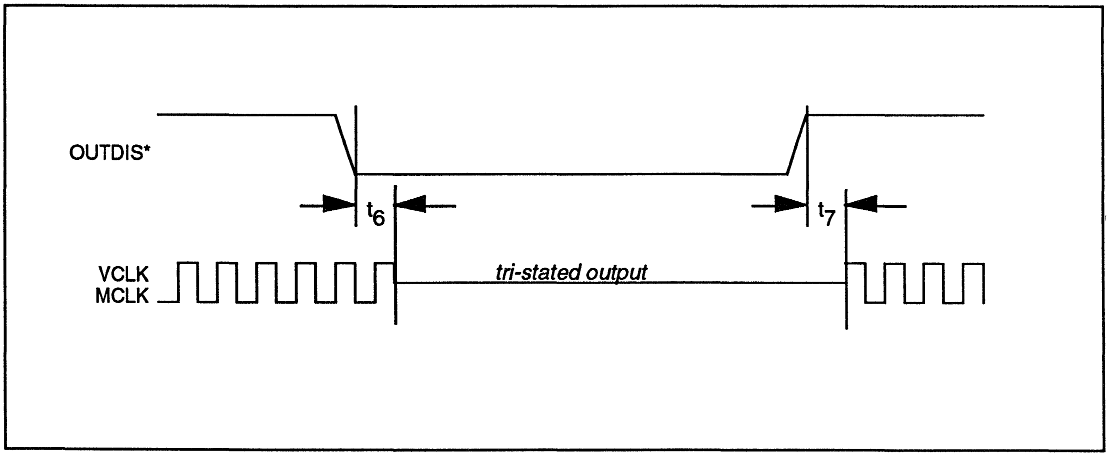
Symbol	Name	Description	Min	Typ	Max	Units
f_{REF}	Reference frequency	Reference oscillator value (note 1)	1	14.31818	60	Mhz
t_{REF}	Reference period	$1/f_{REF}$	16.6		1000	ns
t_1	Input duty cycle	Duty cycle for the input oscillator defined as t_1/t_{REF}	25%		75%	
t_2	Output clock periods	Output oscillator values	8.33 (120 MHz)		2564 (390 MHz)	ns
t_3	Output duty cycle	Duty cycle for the output oscillators (note 2)	45%		55%	
t_4	Rise times	Rise time for the output oscillators into a 25 pf load			3	ns
t_5	Fall times	Fall time for the output oscillator into a 25 pf load			3	ns
t_{freq1}	freq1 output	Old frequency output				
t_{freq2}	freq2 output	New frequency output				
t_A	f_{REF} mux time	Time clock output remains high while output muxes to reference frequency	$^{0.5}\ t_{REF}$		$^{1.5}t_{REF}$	ns
$t_{timeout}$	Timeout internal	Interval for serial programming and for VCO changes to settle (note 3)	2	5	10	ns
t_B	t_{freq2} muxtime	Time clock ouput remains high while output muxes to new frequency value	$^{0.5}\ t_{REF}$	$^{1.5}t_{REF}$		ns
t_6	Tri-state	Time for the ouput oscillators to go into tri-state mode after OUTDIS -signal assertion	0		12	ns
t_7	CLK valid	Time for the output oscillators to recover from tri-state mode after OUTDIS -signal goes high	0		12	ns
t_8	Power-Down	Time for power-down mode of operation to take effect			12	ns
t_9	Power-Up	Time for recovery from power-down mode of operation			12	ns
t_{10}	MCLKOUT high	Time for MCLK to go high after PWRDWN is asserted high	0		t_{PWRDWN}	ns
t_{11}	MCLKOUT delay	Delay of MCLK prior to f_{MCLK} signal at output	$^{0.5}t_{MCLK}$		$^{1.5}\ t_{MCLK}$	ns
t_{serclk}		Clock period of serial clock	$2 \cdot t_{REF}$		2	msec
t_{SU}		Setup time	20			ns
t_{HD}		Hold time	10			ns
t_{ldcmd}		Load command	0		t_1+30	ns

NOTES

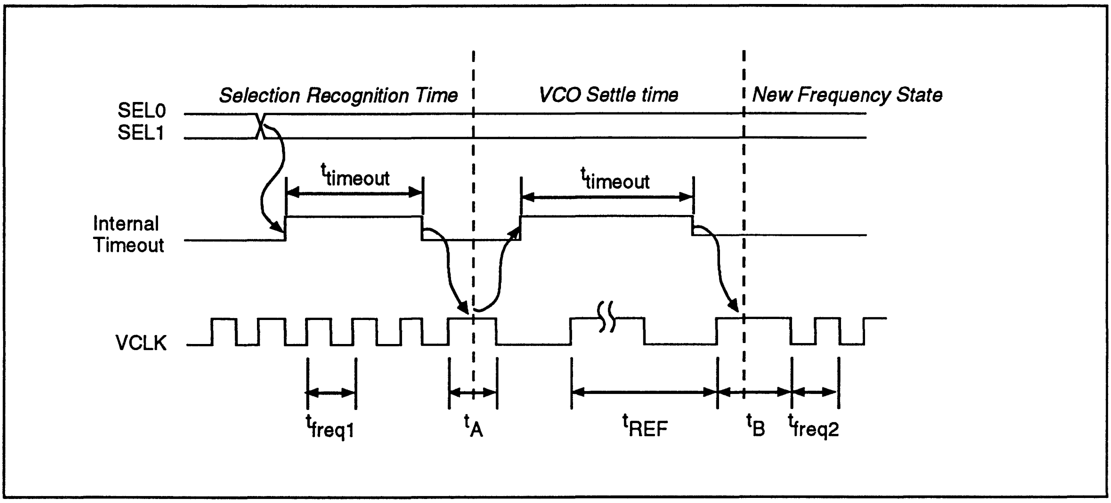
1. For reference frequencies other than 14.81818 MHz, the pre-loaded ROM frequencies will shift proportionally.
2. Duty cycle is measured at CMOS threshold levels. At 5 volts, V_{TH} = 2.5 volts).
3. If the interval is too short, see the timeout interval section in the control register definition.



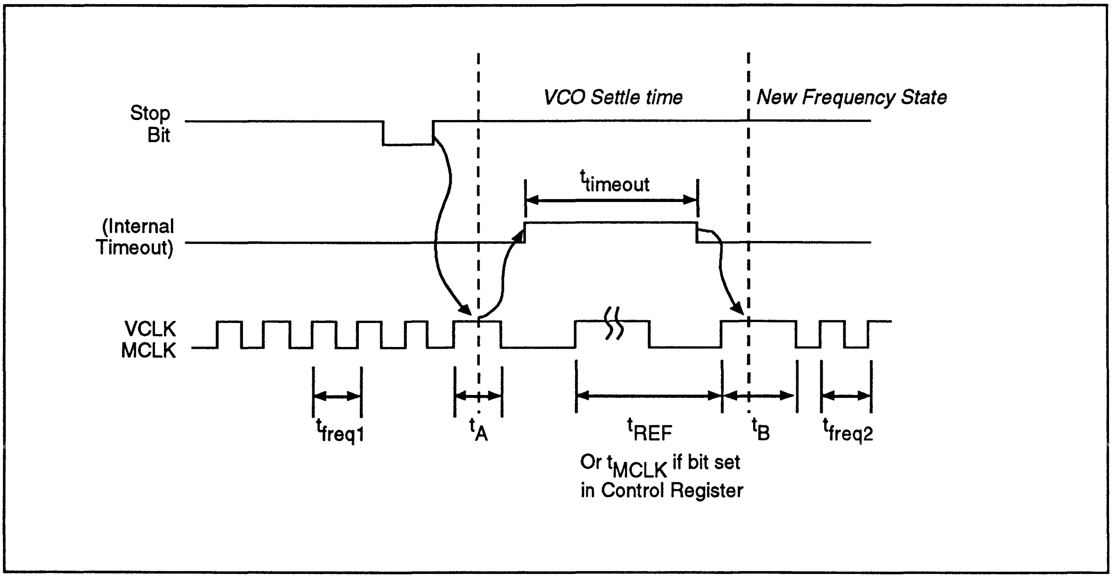
Rise and Fall Times



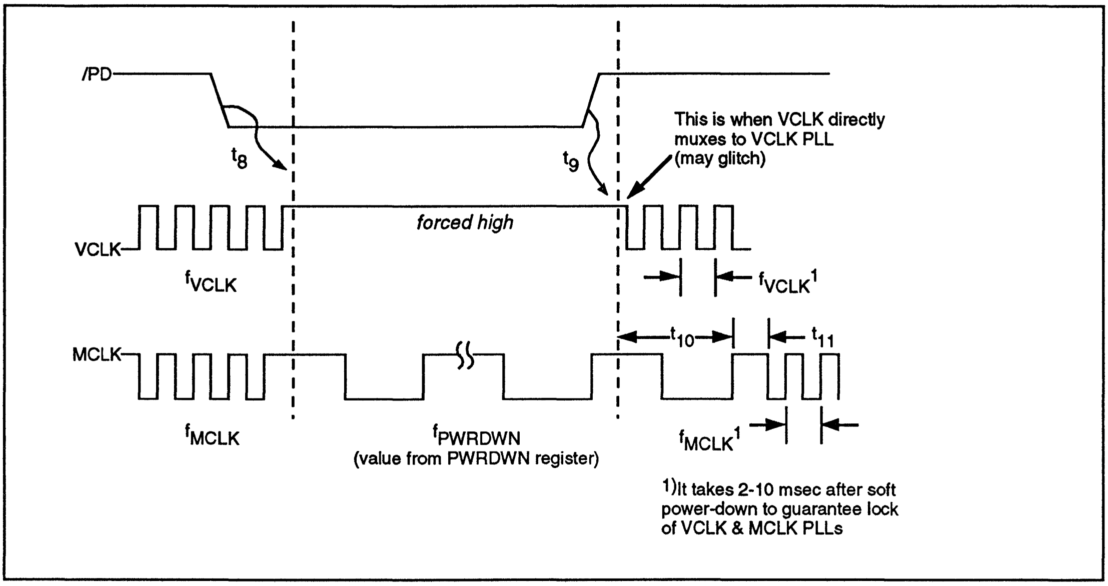
Tri-Stated Timing



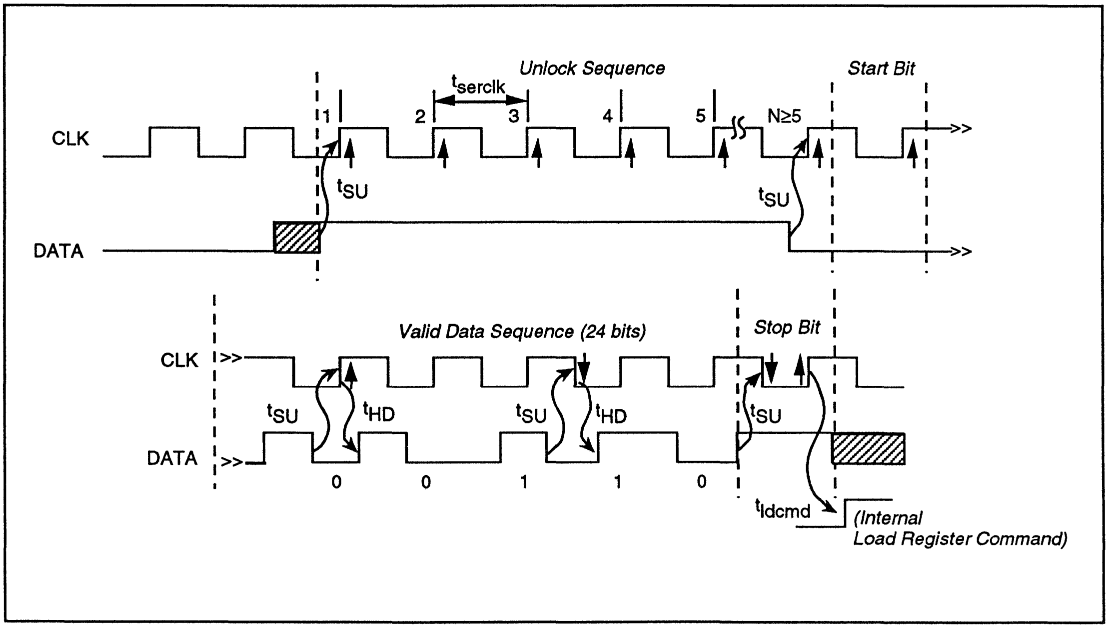
Selection Timing



MCLK & Active VCLK Register Programming Timing



Soft Power-Down Timing (Mode 2)



Serial Programming Timing

ORDERING INFORMATION

Part Number	Temperature Range	Package Type
ICS82C404-xxCW16	0°C to +70°C	16 lead Plastic SOIC
ICS82C404-xxCN16	0°C to +70°C	16 lead Plastic DIP

Integrated Circuit Systems, Inc.

ICS90C61A

Dual Video/Memory Clock Generator

Introduction

The Integrated Circuit Systems **ICS90C61A** is a dual clock generator for VGA applications. It simultaneously generates two clocks. One clock is for the video memory, and the other is the video dot clock.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, AC/DC characteristics, timing diagrams, and package mechanical information.

Description

The Integrated Circuit Systems Video Graphics Array Clock Generator (**ICS90C61A**) is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with Western Digital Imaging Video Graphics Array and 8514/A devices to optimize video subsystem performance.

The video dot clock output may be one of seven internally-generated frequencies or two external inputs. The selection of the video dot clock frequency is done through four inputs.

- SEL0
- SEL1
- VGATTL
- FCLKSEL

SEL0 and SEL1 are latched by the SELEN signal. VGATTL and FCLKSEL are used as direct inputs to the VCLK selection. Table 1-1 is the truth table for VCLK selection.

The input and truth table have been designed to allow a direct connection to one of the many Western Digital Imaging VGA controllers or 8514/A chip sets.

The MCLK output is one of four internally-generated frequencies as shown in Table 1-2. The various VCLK and MCLK frequencies are derived from the 14.318 MHz input frequency.

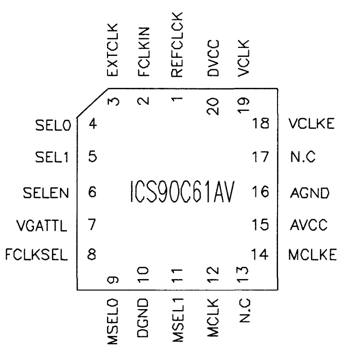
The VCLKE and MCLKE input can tristate the VCLK and MCLK outputs to facilitate board level testing.

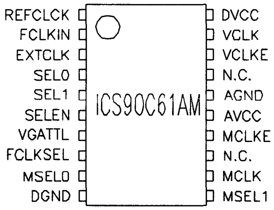
The **ICS90C61A** is capable of extended frequency output up to 80 MHz in custom applications. See page 5 for details.

Features

- Dual Clock generator for the IBM-compatible Western Digital Imaging Video Graphics Array (VGA) LSI devices, and 8514/A chip sets
- Integral loop filter components
- Generates seven video clock frequencies derived from a 14.318 MHz system clock reference frequency
- Video clock which is selectable among the seven internally generated clocks and two external clocks
- On-chip generation of four memory clock frequencies
- CMOS technology
- Available in 20-pin PLCC, SOIC, and DIP packages
- Extended frequency capabilities to 80 MHz in custom frequency patterns

Pin Configuration





20-Pin PLCC, SOIC,DIP
K-10, K-7, K-4

Note: ICS90C61AN (DIP) pinout is identical to ICS90C61AM (SOIC) pinout.

ICS90C61A VGA Interface

The **ICS90C61A** has two system interfaces: System Bus and VGA Controller, and six user-programmable inputs. Figure 2-1 shows how the Integrated Circuit Systems VGA Clock **ICS90C61A** is connected to a VGA controller. Western Digital Imaging VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs, VCLK1 and VCLK2, to outputs. These outputs are used to select the required video frequency.

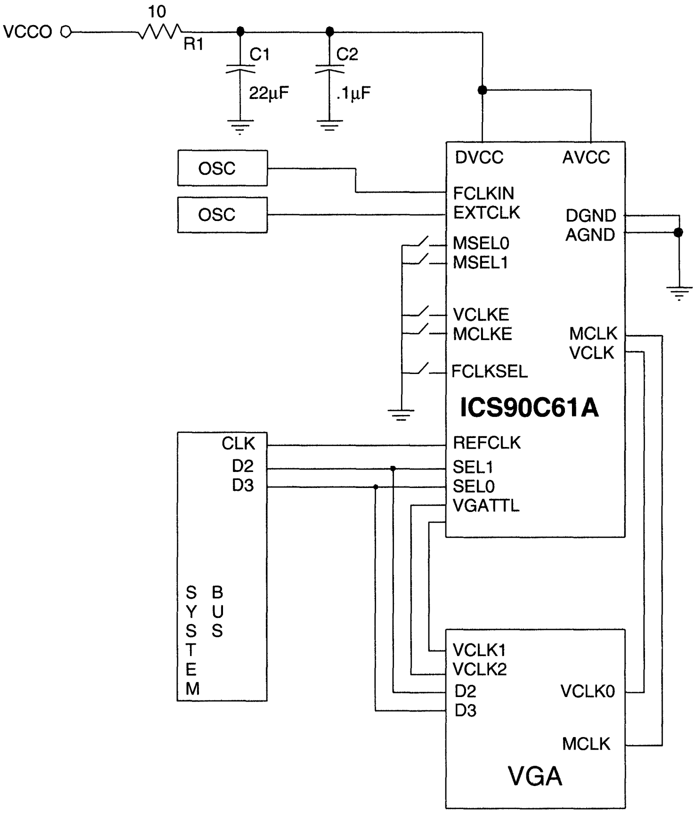


Figure 2-1 ICS90C61A Interface

Note:

C2 should be placed as close as possible to the **ICS90C61A** AVCC pin.

System Bus Inputs

The system bus inputs are:

- REFCLK
- SEL0
- SEL1

The **ICS90C61A** uses the system bus 14.318 MHz clock as a reference to generate all its frequencies for both video and memory clocks. Data lines D2 and D3 are commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

Inputs from VGA Controller

The VGA controller input to the **ICS90C61A** is:

- SELEN

The **ICS90C61A** is programmed to generate different video clock frequencies using the inputs of SEL0, SEL1, VGATTL, and FCLKSEL. The signals VGATTL and FCLKSEL may be supplied by the VGA controller as is the case in Western Digital Imaging VGA controllers. The inputs SEL0-1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital Imaging VGA controllers during I/O writes to internal register 3C2h.

Note: Only SEL0 and SEL1 are latched with signal SELEN.

Outputs to VGA Controller

The outputs from the **ICS90C61A** to the VGA controller are:

- MCLK
- VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

Analog Filters

The analog filters are integral to the **ICS90C61A** device. No external components are required. This feature reduces PC board space requirements and component costs. Phase jitter is reduced as externally-generated noise cannot easily influence the phase-locked loop filter.

User-Definable Inputs

The user-definable inputs are:

- EXTCLK
- FCLKIN
- VLCKE, MCLKE
- MSELO-1
- VGATTL, FCLKSEL

EXTCLK and FCLKIN are additional inputs that may be internally routed to the VCLK output. The additional inputs are useful for supporting modes that require frequencies not provided by the **ICS90C61A**.

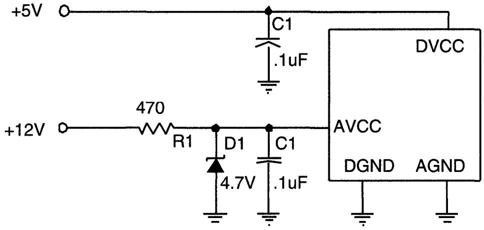
VCLKE and MCLKE are the output enable signals for VCLK and MCLK.When low, the respective output is tristated.

MSEL0-1 are the memory clock (MCLK) select lines. Table 1-2 shows how MCLK frequencies are selected. All signals in this group have internal pull-up resistors.

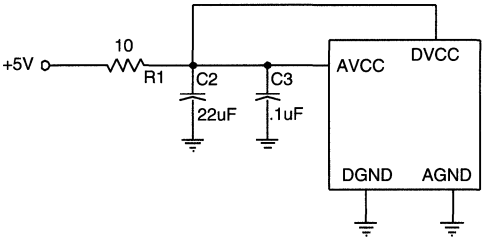
VGATTL and FCLKSEL are video clock (VCLK) select lines that can select additional VCLK frequencies. See Table 1-1.

Power Considerations

The **ICS90C61A** product requires an AV$_{CC}$ supply free of fast rise time transients. This requirement may be met in several ways and is highly dependent on the characteristics of the host system. A VGA adapter card is unique in that it must function in an unknown environment. +5 Volt power quality is dependent not only on the quality of the power supply resident in the host system, but also on the other cards plugged into the host's backplane. Power supply noise ranges from fair to terrible. As the VGA adapter manufacturer has no control over this, he must assume the worst. The best solution is to create a clean +5 Volts by deriving it from the +12 Volt supply by using a zener diode and dropping resister. A 470 Ohm resistor and 4.7 Volt Zener diode are the least costly way to accomplish this. A .047 to .1 microfarad bypass capacitor tied from AV$_{CC}$ to AGND insures good high-frequency decoupling of this point.



Laptop and notebook computers have entirely different problems with power. Typically they have no +12 Volt supply; however, they are much quieter electrically. Because the designer has complete control of the system architecture, he can place sensitive components and systems such as the RAMDAC and Dual Video/Memory Clock away from DRAM and other noise-generating components. Most systems provide power that is clean enough to allow for jitter-free Dual Video/Memory Clock performance if the +5 Volt supply is decoupled with a resistor and 22 microfarad Tantalum capacitor. Digital inputs that are desired to be held at static logical high level should not be tied to +5 Volts as this will result in excessive current drain through the ESD protection diode. The internal pull-up resistors will adequately keep these inputs high.



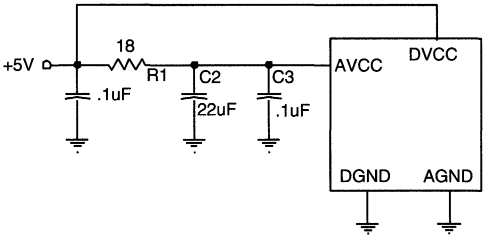


Table 1-1 VCLK SELECTION

FCLKSEL	VGATTL	SEL0	SEL1	VCLK FREQUENCY (MHz)
				ICS90C61A-PR2**
1	0	0	0	REFCLK
1	0	0	1	16.108
1	0	1	0	32.216
1	0	1	1	44.744
1	1	0	0	25.057
1	1	0	1	28.089
1	1	1	0	EXTCLK*
1	1	1	1	36.242
0	X	X	X	FCLKIN*

Table 1-2 MCLK SELECTION

MSEL1	MSEL0	MCLK FREQUENCIES (MHz)
		ICS90C61A-PR2**
0	0	41.612
0	1	37.585
1	0	36.242
1	1	44.744

*Note: FCLKIN and EXTCLK may be programmed to output custom frequencies up to 80 MHz in applications which require this capability. Custom frequencies in these addresses require a significant volume committment and/or one-time mask charge. Contact ICS Sales for details.

**Note: If no “dash number” is specified, then the “–PR2” will be supplied since this version is completely compatible with the original WD90C61 frequency set.

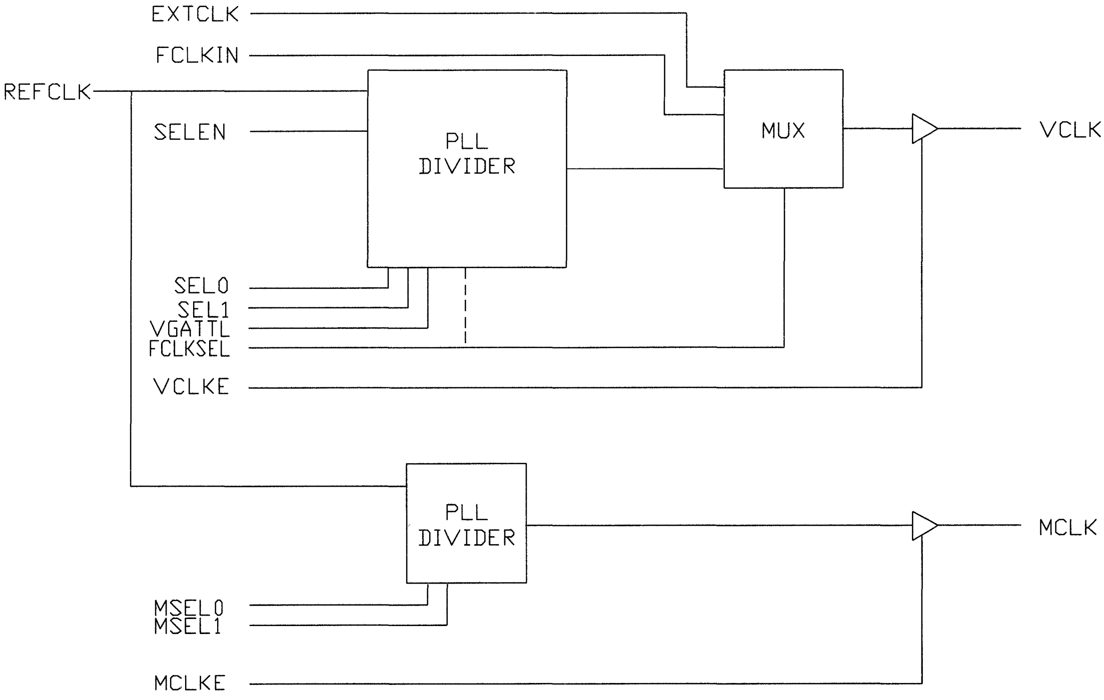


Figure 2-2 ICS90C61A Functional Block Diagram

Pin Descriptions

The following table provides the pin descriptions for the 20-pin **ICS90C61A** packages:

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	REFCLK	IN	Reference input clock from system
2	FCLKIN	IN	Feature clock input pin
3	EXTCLK	IN	External clock input for an additional frequency
4	SEL0	IN	Control input for VCLK selection
5	SEL1	IN	Control input for VCLK selection
6	SELEN	IN	Strobe for latching VSEL(0,1) *(Low enable)*
7	VGATTL	IN	Control input for VCLK selection
8	FCLKSEL	IN	Control input for FCLK selection
9	MSEL0	IN	Select input for MCLK selection
10	DGND	-	Ground for Digital Circuit
11	MSEL1	IN	Select input for MCLK selection
12	MCLK	OUT	Memory Clock Output
13	N.C.	-	No Connection
14	MCLKE	IN	Enable input for MCLK output *(high enables output)*
15	AVCC	-	Power supply for analog circuit
16	AGND	-	Ground for analog circuit
17	N.C.	-	No Connection
18	VCLKE	IN	Enable input for VCLK output *(high enables output)*
19	VCLK	OUT	Video Clock Output
20	DVCC	-	Power supply for Digital Circuit

NOTE:

CLK1, EXTCLK, FCLKIN, SEL0, SEL1,VGATTL, FCLKSEL, SELEN, MSEL0, MSEL1, VCLKE, and MCLKE - input pins have internal pull-up resistors.

Absolute Maximum Ratings

Ambient temperature under bias	0 °C to 70 °C
Storage temperature	-40 °C to 125 °C
Voltage on all inputs and outputs with respect to V_{SS}	0.5 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (OV Ground). Positive current flows into the referenced pin.

Operating temperature range	0 °C to 70 °C
Power supply voltage	4.75 to 5.25 Volts

DC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS	PINS
V_{IL}	Input Low Voltage	V_{SS}	0.8	V	$V_{CC} = 5V$	SEL0-1, SELEN, VGATTL, MSEL0-1, FCLKSEL, VCLKE, MCLKE, EXTCLK
V_{IH}	Input High Voltage	2.0	V_{CC}	V	$V_{CC} = 5V$	SEL0-1, SELEN, VGATTL, MSEL0-1, FCLKSEL, VCLKE, MCLKE, EXTCLK
V_{IL}	Input Low Voltage	Vss	1.5	V	$V_{CC} = 5V$	FCLKIN
V_{IH}	Input High Voltage	V_{CC} -1.5	V_{CC}	V	$V_{CC} = 5V$	FCLKIN
I_{IH}	Input Leakage Current	-	20	µA	$V_{in} = V_{CC}$	
V_{OL}	Output Low Voltage	-	0.4	V	$I_{OL} = 6.0$ mA	
V_{OH}	Output High Voltage	2.4	-	V	$I_{OH} = 4.0$ mA	
I_{CCD}	Digital Supply Current	-	35	mA	$V_{CC} = 5V$, $C_L = 15pF$	
I_{CCA}	Analog Supply Current	-	10	mA	$V_{CC} = 5V$	
R_{UP}	Internal pull-up Resistors	25	-	K ohms	$V_{CC} = 5V$	
C_{in}	Input Pin Capacitance	-	8	pF	$F_C = 1$ MHz	
C_{out}	Output Pin Capacitance	-	12	pF	$F_C = 1$ MHz	

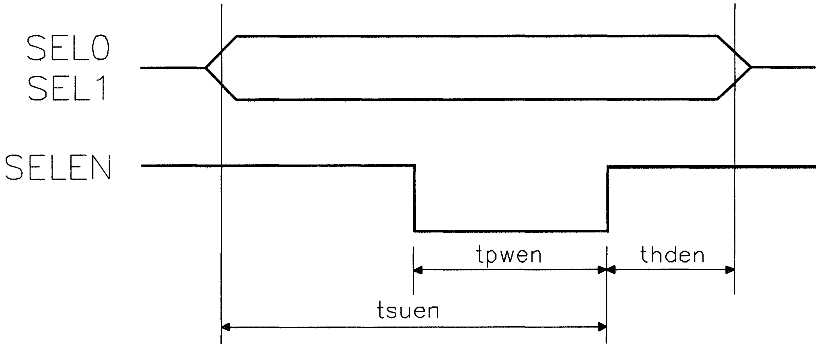
AC Timing Characteristics

The following notes apply to all of the parameters presented in this section.

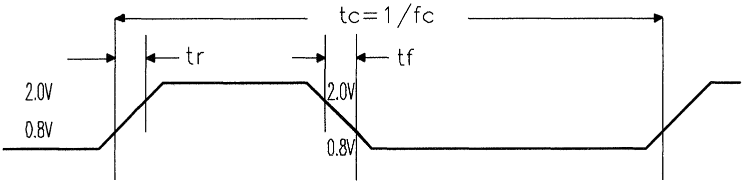
1. REFCLK = 14.318 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns).
4. Maximum jitter is within a range of 30 μ s after triggering on a 400 MHz scope.
5. Rise and fall time between 0.8 and 2.0 VDC.
6. Output pin loading = 15pF
7. Duty cycle is measured at 1.4V

SYMBOL	PARAMETER	MIN	MAX	NOTES
SELEN TIMING				
T_{pwen}	Enable Pulse Width	20	-	
T_{suen}	Setup Time Data to Enable	20	-	
T_{hden}	Hold Time Data to Enable	10	-	
REFERENCE INPUT CLOCK				
Tr	Rise Time	-	10	Phase-Jitter 1 ns max.
Tf	Fall Time	-	10	Duty Cycle 42.5% min. to 57.5% max.
MCLK and VCLK TIMINGS				
Tr	Rise Time	-	3	Phase-Jitter 3 ns max.
Tf	Fall Time	-	3	Duty Cycle 40%min. to 60% max.
-	Frequency Error		1.0	%
-	Maximum Frequency		80	MHz
-	Propagation Delay for Pass Through Frequency	-	20	ns
-	Output Enable to Tristate (into and out of) time		15	ns

ENABLE TIMING



CLOCK WAVEFORM



Ordering Information

ICS90C61A-XXXN or ICS90C61A-XXXM or ICS90C61A-XXXV

Example:

ICS XXXX-XXX N

Package Type
N=DIP (Plastic) V=PLCC
M=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)
Note: Unless a specific pattern is ordered, PR2 will be shipped.

Device Type (consists of 3-6 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated Circuit Systems, Inc.

ICS90C64A

Dual Video/Memory Clock Generator

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This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, AC/DC characteristics, timing diagrams, and package mechanical information.

Description

The Integrated Circuit Systems Video Graphics Array Clock Generator (**ICS90C64A**) is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with Western Digital Imaging Video Graphics Array and 8514/A devices to optimize video subsystem performance.

The video dot clock output may be one of fifteen internally-generated frequencies or one external input. The selection of the video dot clock frequency is done through four inputs.

- VSEL0
- VSEL1
- VSEL2
- VSEL3

VSEL0 and VSEL1 are latched by the SELEN signal. VSEL2 and VSEL3 are used as direct inputs to the VCLK selection. Table 1-1 is the truth table for VCLK selection.

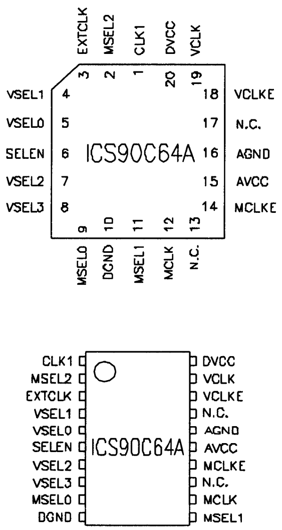
The input and truth table have been designed to allow a direct connection to one of the many Western Digital Imaging VGA controllers or 8514/A chip sets.

The MCLK output is one of eight internally-generated frequencies as shown in Table 1-2. The various VCLK and MCLK frequencies are derived from the 14.318 MHz Input frequency.

The VCLKE and MCLKE input can tristate the VCLK and MCLK outputs to facilitate board level testing.

Features

- Improved compatibility with Western Digital Controllers
- 100% backward compatible with ICS90C63 and ICS90C64
- Dual Clock generator for the IBM compatible Western Digital Imaging Video Graphics Array (VGA) LSI devices, and 8514/A chip sets
- Integral loop filter components. Reduce cost and phase-jitter
- Generates 15 video clock frequencies (including 25.175 and 28.322 MHz) derived from a 14.318 MHz system clock reference frequency
- On-chip generation of eight memory clock frequencies.
- Video clock is selectable among the fifteen internally generated clocks and one external clock
- CMOS technology
- Available in 20-pin PLCC, SOIC, and DIP packages



20-Pin PLCC, SOIC,DIP
K-10, K-7, K-4

Note:ICS90C64AN (DIP) pinout is identical to ICS90C64AM (SOIC) pinout.

ICS90C64A VGA Interface

The **ICS90C64A** has two system interfaces: System Bus and VGA Controller, as well as analog filters and seven user programmable inputs. Figure 2-1 shows how the Integrated Circuit Systems VGA Clock **ICS90C64A** is connected to a VGA controller. Western Digital Imaging VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs, VCLK1 and VCLK2, to outputs. These outputs are used to select the required video frequency.

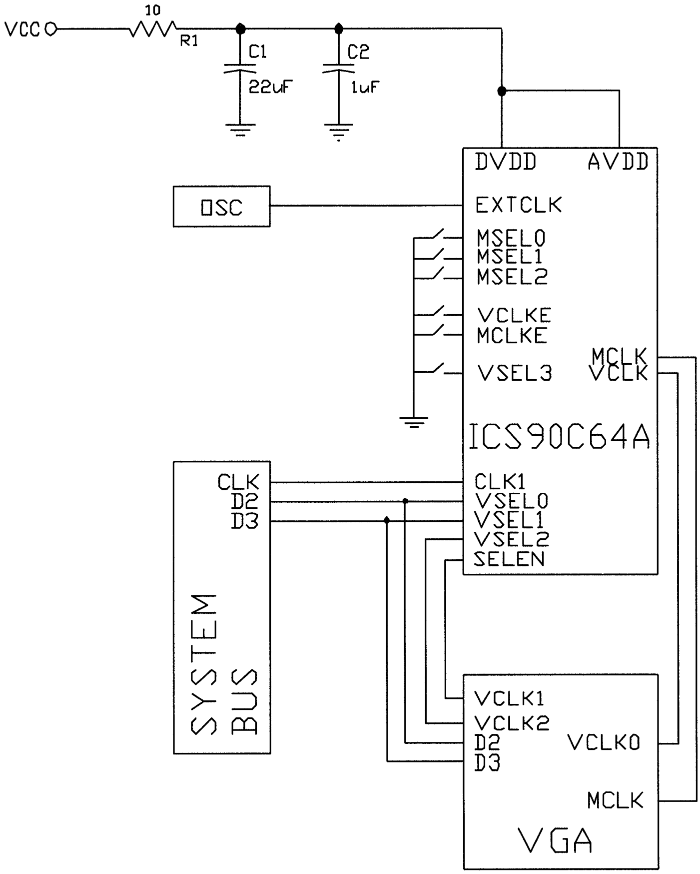


Figure 2-1 ICS90C64A Interface

Note:

C2 should be placed as close as possible to the **ICS90C64A** AVDD pin.

System Bus Inputs

The system bus inputs are:

- CLK1
- VSEL0
- VSEL1

The **ICS90C64A** uses the system bus 14.318 MHz clock as a reference to generate all its frequencies for both video and memory clocks. Data lines D2 and D3 are commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

Inputs from VGA Controller

The VGA controller input to the **ICS90C64A** is:

- SELEN

The **ICS90C64A** is programmed to generate different video clock frequencies using the inputs of VSEL0, VSEL1, VSEL2, and VSEL3. The signals VSEL2 and VSEL3 may be supplied by the VGA controller as is the case in Western Digital Imaging VGA controllers. The inputs VSEL0-1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital Imaging VGA controllers during I/O writes to internal register 3C2h.

Note: Only VSEL0 and VSEL1 are latched with signal SELEN.

Outputs to VGA Controller

The outputs from the **ICS90C64A** to the VGA controller are:

- MCLK
- VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

Analog Filters

The analog filters are integral to the **ICS90C64A** device. No external components are required. This feature reduces PC board space requirements and component costs. Phase-jitter is reduced as externally-generated noise cannot easily influence the phase-locked loop filter.

User-Definable Inputs

The user-definable inputs are:

- EXTCLK
- VLCKE, MCLKE
- MSELO-2
- VSEL2, VSEL3

EXTCLK is an additional input that may be internally routed to the VCLK output. This additional input is useful for supporting modes that require frequencies not provided by the **ICS90C64A**.

VCLKE and MCLKE are the output enable signals for VCLK and MCLK. When low, the respective output is tristated.

MSEL0-2 are the memory clock (MCLK) select lines. Table 1-2 shows how MCLK frequencies are selected. All signals in this group have internal pull-up resistors.

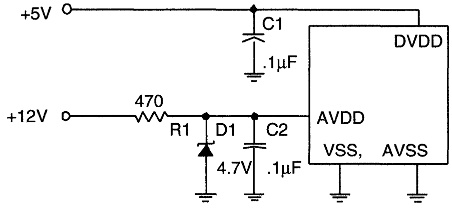
VSEL2 and VSEL3 are video clock (VCLK) select lines that can select additional VCLK frequencies. See Table 1-1.

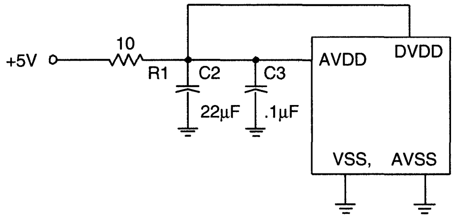
VSEL2 and VSEL3 have internal pull-ups.

Power Considerations

The **ICS90C64A** product requires an AV_{DD} supply free of fast rise time transients. This requirement may be met in several ways and is highly dependent on the characteristics of the host system. A VGA adapter card is unique in that it must function in an unknown environment. +5 Volt power quality is dependent not only on the quality of the power supply resident in the host system, but also on the other cards plugged into the host's backplane. Power supply noise ranges from fair to terrible. As the VGA adapter manufacturer has no control over this, he must assume the worst. The best solution is to create a clean +5 Volts by deriving it from the +12 Volt supply by using a zener diode and dropping resistor. A 470 Ohm resistor and 5.1 Volt Zener diode are the least costly way to accomplish this. A .047 to .1 microfarad bypass capacitor tied from AV_{DD} to AV_{SS} insures good high-frequency decoupling of this point.

Laptop and notebook computers have entirely different problems with power. Typically they have no +12 Volt supply; however, they are much quieter electrically. Because the designer has complete control of the system architecture, he can place sensitive components and systems such as the RAMDAC and Dual Video/Memory Clock away from DRAM and other noise-generating components. Most systems provide power that is clean enough to allow for jitter- free Dual Video/Memory Clock performance if the +5 Volt supply is decoupled with a resistor and 22 microfarad Tantalum capacitor. Digital inputs that are desired to be held at a static logical high level should not be tied to +5 Volts as this will result in excessive current drain through the ESD protection diode. The internal pull-up resistors will adequately keep these inputs high.





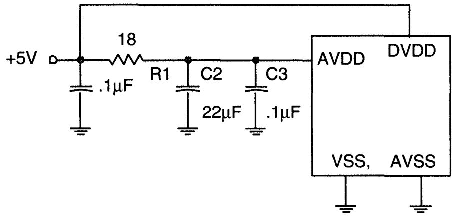


Table 1-1 VCLK Selection

3	2	1	0	VCLK Frequency (MHz)			
				ICS90C64A	ICS90C64A-903	ICS90C64A-907	ICS90C64A-909
0	0	0	0	30.0	30.0	30.250	30.0
0	0	0	1	77.25	77.25	77.25	77.25
0	0	1	0	EXTCLK	EXTCLK	EXTCLK	EXTCLK
0	0	1	1	80.0	80.0	80.0	80.0
0	1	0	0	31.5	31.5	31.5	31.5
0	1	0	1	36.0	36.0	35.5	36.0
0	1	1	0	75.0	75.0	75.0	75.0
0	1	1	1	50.0	50.0	72.0	50.0
1	0	0	0	40.0	40.0	40.0	40.0
1	0	0	1	50.0	50.0	50.0	50.0
1	0	1	0	32.0	32.0	32.0	32.0
1	0	1	1	44.9	44.9	44.9	44.9
1	1	0	0	25.175	25.175	25.175	25.175
1	1	0	1	28.322	28.322	28.322	28.322
1	1	1	0	65.0	65.0	65.0	65.0
1	1	1	1	36.0	36.0	36.0	36.0

Table 1-2 MCLK Selection

2	1	0	MCLK Frequencies (MHz)			
			ICS90C64A	ICS90C64A-903	ICS90C64A-907	ICS90C64A-909
0	0	0	33.0	33.0	65.0	75.0
0	0	1	49.218	49.218	49.218	40.0
0	1	0	60.0	60.0	60.0	45.0
0	1	1	30.5	30.5	62.5	50.0
1	0	0	41.612	41.612	41.612	55.0
1	0	1	37.5	37.5	37.5	60.0
1	1	0	36.0	36.0	55.0	65.0
1	1	1	44.296	44.296	44.296	70.0

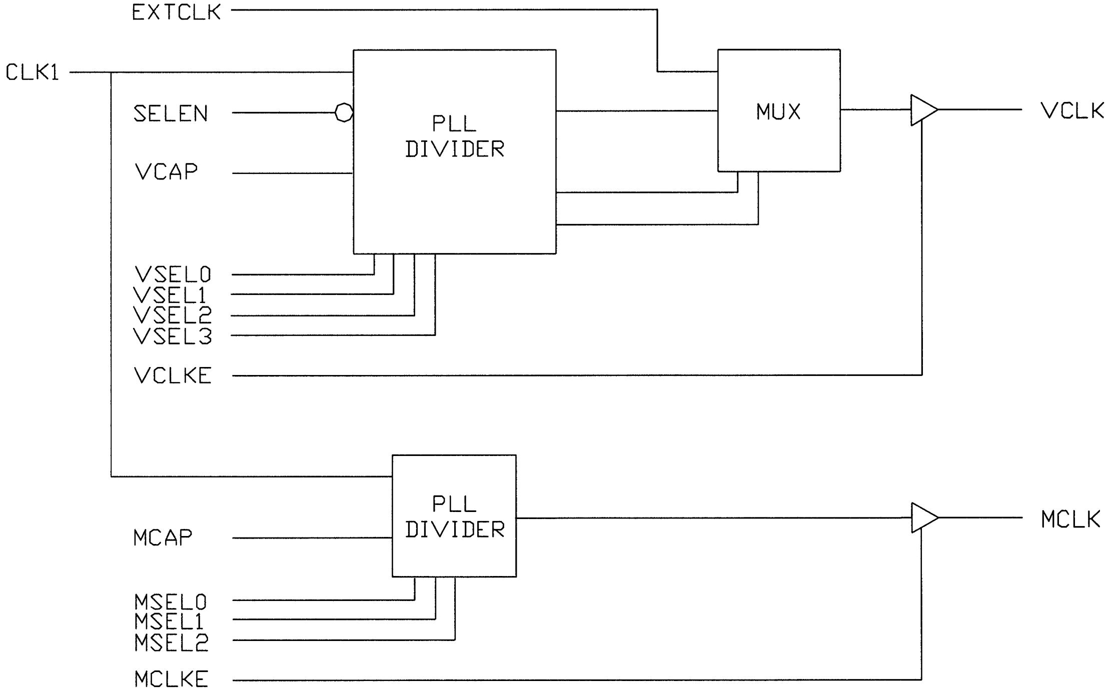


Figure 2-2 ICS90C64A Functional Block Diagram

Pin Descriptions

The following table provides the pin descriptions for the 20-pin **ICS90C64A** packages.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	CLK1	IN	Reference input clock from system
2	MSEL2	IN	Select input for MCLK selection
3	EXTCLK	IN	External clock input for an additional frequency
4	VSEL1	IN	Control input for VCLK selection
5	VSEL0	IN	Control input for VCLK selection
6	SELEN	IN	Strobe for latching VSEL(0,1) *(Low enable)*
7	VSEL2	IN	Control input for VCLK selection
8	VSEL3	IN	Control input for VCLK selection
9	MSEL0	IN	Select input for MCLK selection
10	DGND	-	Ground for Digital Circuit
11	MSEL1	IN	Select input for MCLK selection
12	MCLK	OUT	Memory Clock Output
13	N.C.	-	No connection
14	MCLKE	IN	Enable input for MCLK output *(high enables output)*
15	AVDD	-	Power supply for analog circuit
16	AGND	-	Ground for analog circuit
17	N.C.	-	No connection
18	VCLKE	IN	Enable input for VCLK output *(high enables output)*
19	VCLK	OUT	Video Clock Output
20	DVDD	-	Power supply for Digital Circuit

Note:
CLK1, EXTCLK,VSEL0, VSEL1,VSEL2, VSEL3, SELEN, MSEL0, MSEL1, MSEL2, VCLKE, and MCLKE - input pins have internal pull-up resistors.

Absolute Maximum Ratings

Ambient Temperature under bias	0 °C to 70 °C
Storage temperature	-40 °C to 125 °C
Voltage on all inputs and outputs with respect to V_{SS}	0.5 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (OV Ground). Positive current flows into the referenced pin.

Operating Temperature range	0 °C to 70 °C
Power supply voltage	4.75 to 5.25 Volts

DC Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	V_{SS}		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{DD}	V	
I_{IH}	Input Leakage Current	-		10	µ A	$V_{in} = V_{DD}$
V_{OL}	Output Low Voltage	-		0.4	V	$I_{OL} = 8.0$ mA
V_{OH}	Output High Voltage	V_{DD}-.4		-		$I_{OH} = 4.0$mA
V_{OH}	Output High Voltage	2.4		-	V	$I_{OH} = 8.0$ mA
I_{CC}	Supply Current	-	20	28	mA	No load VCLK = 28 MHz MCLK = 40 MHz
I_{CC}	Supply Current	-	27	35	mA	No load VCLK = 80 MHz MCLK = 40 MHz
R_{UP}	Internal Pull-up Resistors	50		-	k ohms	$V_{DD} = 5V$
C_{in}	Input Pin Capacitance	-		8	pF	$F_C = 1$ MHz
C_{out}	Output Pin Capacitance	-		12	pF	$F_C = 1$ MHz

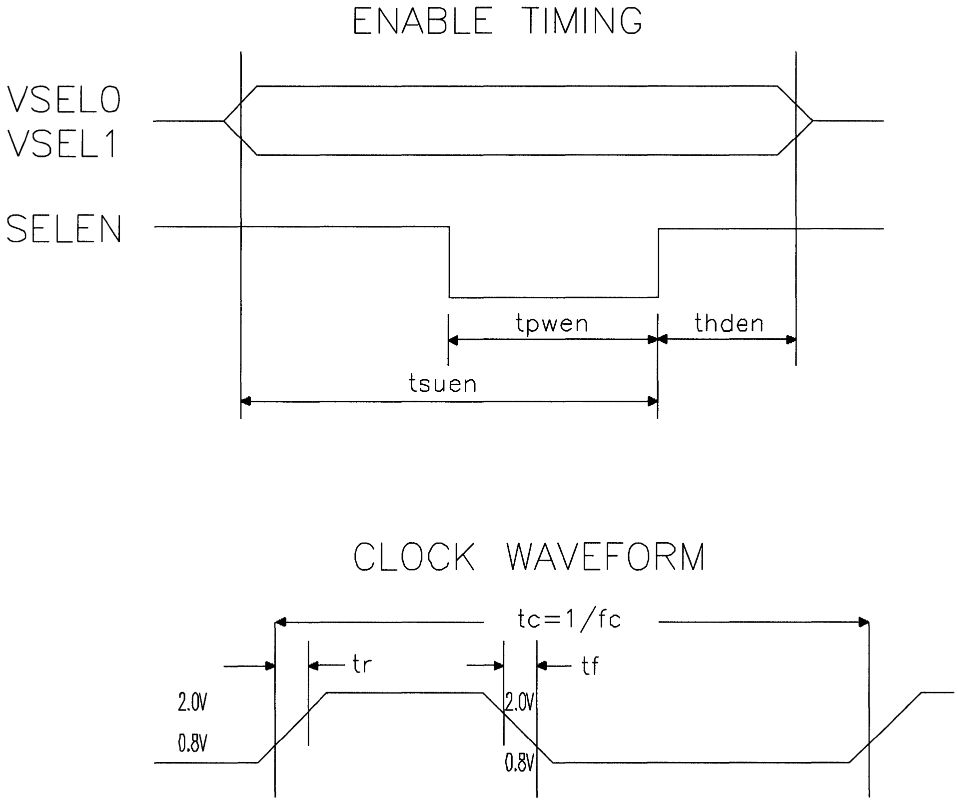
AC Timing Characteristics

The following notes apply to all of the parameters presented in this section:

1. REFCLK = 14.318 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns), unless labeled otherwise.
4. Output pin loading = 15pF

SYMBOL	PARAMETER	MIN	TYP	MAX	NOTES
SELEN TIMING					
T_{pwen}	Enable Pulse Width	20			
T_{suen}	Setup Time Data to Enable	20			
T_{hden}	Hold Time Data to Enable	10			
Reference Input Clock					
Tr	Rise Time			10	Phase-Jitter 1 ns max.
Tf	Fall Time			10	Duty Cycle 42.5% min. to 57.5% max.
MCLK and VCLK TIMINGS					
Tr	Rise Time		.9	1.5	.8V-2.0V*
Tf	Fall Time		.9	1.5	2.0V-.8V
Tr	Rise Time		1.2	2.0	.3 V_{DD}-.7 V_{DD}
Tf	Fall Time		1.2	2.0	.7 V_{DD}-.3 V_{DD}
T_{high}	Duty Cycle	50%		60%	1.4V Switch Point
T_{high}	Duty Cycle	45%		55%	V_{DD}/2 Switch Point
	Frequency Error			0.5	%
	Maximum Frequency			135	MHz
	Propagation Delay for Pass Through Frequency			20	ns
	Output Enable to Tri-State (into and out of) time			15	ns

* WD90C11 Video Controller is designed with TTL level input thresholds on the inputs driven by the ICS90C64A VCLK and MCLK outputs. The later controllers (WD90C20, WD90C22, WD90C26, WD90C30, and WD90C31) are designed with input switch points of VCC/2 (CMOS)


ENABLE TIMING

CLOCK WAVEFORM

Figure 5-1 ICS90C64A Timing

Ordering Information

ICS90C64A-XXXN or ICS90C64A-XXXM or ICS90C64A-XXXV

Example:

ICS XXXX- XXX N

Package Type
N=DIP (Plastic) V=PLCC
M=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3-6 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated Circuit Systems, Inc.

ICS90C65

Dual Voltage Video/Memory Clock Generator

Introduction

The Integrated Circuit Systems **ICS90C65** is a dual clock generator for VGA applications. It simultaneously generates two clocks. One clock is for the video memory, and the other is the video dot clock.

The **ICS90C65** has been specifically designed to serve the portable PC market with operation at either 3.3V or 5V with a comprehensive power-saving shut-down mode.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, AC/DC characteristics, timing diagrams, and package mechanical information.

Description

The Integrated Circuit Systems Video Graphics Array Clock Generator (**ICS90C65**) is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with Western Digital Imaging Video Graphics Array and 8514/A devices to optimize video subsystem performance.

The video dot clock output may be one of 15 internally-generated frequencies or one external input. The selection of the video dot clock frequency is done through four inputs.

- VSEL0
- VSEL1
- VSEL2
- VSEL3

VSEL0 and VSEL1 are latched by the SELEN signal. VSEL2 and VSEL3 are used as direct inputs to the VCLK selection. Table 1-1 is the truth table for VCLK selection.

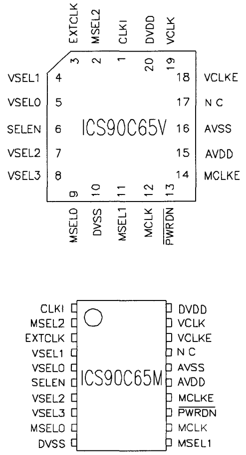
The input and truth table have been designed to allow a direct connection to one of the many Western Digital Imaging VGA controllers or 8514/A chip sets.

The MCLK output is one of eight internally-generated frequencies as shown in Table 1-2. The various VCLK and MCLK frequencies are derived from the 14.318 MHz input frequency.

The VCLKE and MCLKE input can tristate the VCLK and MCLK outputs to facilitate board level testing.

Features

- Specified for dual voltage operation (V_{DD}=3.3V or 5V), but operates continuously from 3.0V to 5.25V
- Designed to be powered-down for extended battery life
- Backward compatibility to the ICS90C64 and ICS90C63
- Dual Clock generator for the IBM-compatible Western Digital Imaging Video Graphics Array (VGA) LSI devices, and 8514/A chip sets
- Integral loop filter components, reduce cost and phase jitter
- Generates fifteen video clock frequencies (including 25.175 and 28.322 MHz) derived from a 14.318 MHz system clock reference frequency
- On-chip generation of eight memory clock frequencies
- Video clock is selectable among the 15 internally generated clocks and one external clock
- CMOS technology
- Available in 20-pin PLCC, SOIC and DIP packages



**20-Pin PLCC, SOIC,DIP
K-10, K-7, K-4**

Note:ICS90C65N (DIP) pinout is identical to ICS90C65M (SOIC) pinout

ICS90C65 VGA Interface

The **ICS90C65** has two system interfaces: System Bus and VGA Controller, as well as other programmable inputs. Figure 1 shows how the Integrated Circuit Systems' VGA Clock **ICS90C65** is connected to a VGA controller. Western Digital Imaging VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs to outputs. They are theVCLK1/VCSLD/VCSEL and VCLK2/VCSEL/ VCSELH outputs and they are used to select the required video frequency.

When the power-down capabilities are used, the control signal for $\overline{\text{PWRDN}}$ is normally held in one of a group of latches. If the power-down function is not to be used, ***PWRDN must be tied to V_{DD}***, otherwise the internal pull-down will place the chip in the power-down mode.

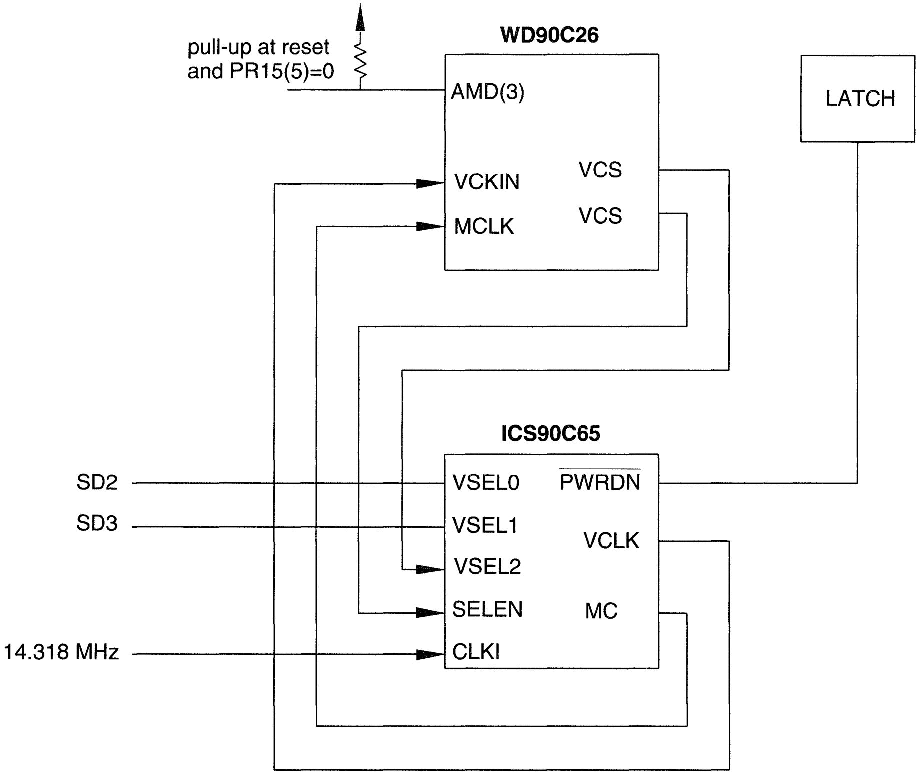


Figure 1

System Bus Inputs

The system bus inputs are:

- CLKI
- VSEL0
- VSEL1

The **ICS90C65** uses the system bus 14.318 MHz clock as a reference to generate all its frequencies for both video and memory clocks. Data lines D2 and D3 are commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

Inputs from VGA Controller

The VGA controller input to the **ICS90C65** is:

- SELEN

The **ICS90C65** is programmed to generate different video clock frequencies using the inputs of VSEL0, VSEL1, VSEL2, and VSEL3. The signals VSEL2 and VSEL3 may be supplied by the VGA controller as is the case in Western Digital Imaging VGA controllers. The inputs VSEL0-1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital Imaging VGA controllers during I/O writes to internal register 3C2h.

Note: Only VSEL0 and VSEL1 are latched with signal SELEN.

Outputs to VGA Controller

The outputs from the **ICS90C65** to the VGA controller are:

- MCLK
- VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

Analog Filters

The analog filters are integral to the **ICS90C65** device. No external components are required. This feature reduces PC board space requirements and component costs. Phase-jitter is reduced as externally-generated noise cannot easily influence the phase-locked loop filter.

User-Definable Inputs

The user definable inputs are:

- EXTCLK
- VLCKE, MCLKE
- MSEL0-2
- VSEL2, VSEL3
- $\overline{\text{PWRDN}}$

EXTCLK is an additional input that may be internally routed to the VCLK output. This additional input is useful for supporting modes that require frequencies not provided by the **ICS90C65** or for use during board test.

VCLKE and MCLKE are the output enable signals for VCLK and MCLK. When low the respective output is tristated.

MSEL0-2 are the memory clock (MCLK) select lines. Table 1-2 shows how MCLK frequencies are selected. All signals in this group have internal pull-up resistors.

VSEL2 and VSEL3 are video clock (VCLK) select lines that can select additional VCLK frequencies. See Table 1-1.

VSEL2 and VSEL3 have internal pull-ups.

$\overline{\text{PWRDN}}$ can place the **ICS90C65** in a power-down mode which drops its supply current requirement below 1 microamp. When placed in this mode, the digital inputs may be either high or low or floating without causing an increase in the **ICS90C65** supply current.

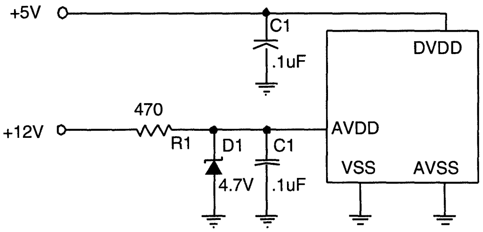
The $\overline{\text{PWRDN}}$ pin must be low (It has an internal pull-down.) in order to place the device in its low power state. The output pins (VCLK and MCLK) are driven high by the **ICS90C65** when it is in its low power state.

If CLKI is being driven by an external source, it may be driven low or high without a power penalty. If CLKI is at an intermediate voltage ($V_{SS}+0.5 < V_{IN} < V_{DD}-0.5$), there will be a small increase in supply current. If CLKI is driven at 14.318 MHz while the chip is in power-down, the **ICS90C65** supply current will increase to approximately 1.2 mA.

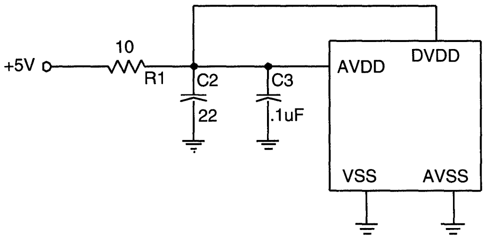
The SELEN (pin 6) may be used to guard against inadvertent frequency changes during power-down/powerup sequences. By holding the SELEN low during power-down and power-up sequences, the **ICS90C65** will retain the most recent video frequency selection.

Power Considerations

The **ICS90C65** product requires an AVDD supply free of fast rise time transients. This requirement may be met in several ways and is highly dependent on the characteristics of the host system. A VGA adapter card is unique in that it must function in an unknown environment. +5 Volt power quality is dependent not only on the quality of the power supply resident in the host system, but also on the other cards plugged into the host's backplane. Power supply noise ranges from fair to terrible. As the VGA adapter manufacturer has no control over this, he must assume the worst. The best solution is to create a clean +5 Volts by deriving it from the +12 Volt supply by using a zener diode and dropping resistor. A 470 Ohm resistor and 5.1 Volt Zener diode are the least costly way to accomplish this. A .047 to .1 microfarad bypass capacitor tied from AVDD to AVSS insures good high- frequency decoupling of this point.



Laptop and notebook computers have entirely different problems with power. Typically they have no +12 Volt supply; however, they are much quieter electrically. Because the designer has complete control of the system architecture, he can place sensitive components and systems such as the RAMDAC and Dual Video/Memory Clock away from DRAM and other noise-generating components. Most systems provide power that is clean enough to allow for jitter- free Dual Video/Memory Clock performance if the +5 Volt supply is decoupled with a resistor and 22 microfarad Tantalum capacitor. Digital inputs that are desired to be held at a static logical high level should not be tied to +5 Volts as this may result in excessive current drain through the ESD protection diode. The internal pull-up resistors will adequately keep these inputs high.



Pin Descriptions

The following table provides the pin descriptions for the 20-pin **ICS90C65** packages.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	CLKI	IN	Reference input clock from system
2	MSEL2	IN	Select input for MCLK selection
3	EXTCLK	IN	External clock input for an additional frequency
4	VSEL1	IN	Control input for VCLK selection
5	VSEL0	IN	Control input for VCLK selection
6	SELEN	IN	Strobe for latching VSEL(0,1) *(Low enable)*
7	VSEL2	IN	Control input for VCLK selection
8	VSEL3	IN	Control input for VCLK selection
9	MSEL0	IN	Select input for MCLK selection
10	DVSS	-	Ground for Digital Circuit
11	MSEL1	IN	Select input for MCLK selection
12	MCLK	OUT	Memory Clock Output
13	$\overline{\text{PWRDN}}$	IN	Power Down Control
14	MCLKE	IN	Enable input for MCLK output *(high enables output)*
15	AVDD	-	Power supply for analog circuit
16	AVSS	-	Ground for analog circuit
17	N.C.	-	No connection
18	VCLKE	IN	Enable input for VCLK output *(high enables output)*
19	VCLK	OUT	Video Clock Output
20	DVDD	-	Power supply for Digital Circuit

Note:
CLKI, EXTCLK,VSEL0, VSEL1,VSEL2, VSEL3, SELEN, MSEL0, MSEL1, MSEL2, VCLKE, and MCLKE - input pins have internal pull-up resistors. $\overline{\text{PWRDN}}$ has an internal pull-down resistor.

Absolute Maximum Ratings

Ambient Temperature under bias	0 °C to 70 °C
Storage temperature	-40 °C to 125 °C
Voltage on all inputs and outputs with respect to V_{SS}	0.3 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (OV Ground). Positive current flows into the referenced pin.

Operating Temperature range	0 °C to 70 °C
Power supply voltage	3.0 to 5.25 Volts

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section:

1. REFCLK = 14.318 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns).
4. Maximum jitter is within a range of 30 µs after triggering on a 400 MHz scope.
5. Rise and fall time is between 0.8 and 2.0 VDC unless otherwise stated.
6. Output pin loading = 15pF
7. Duty cycle is measured at $V_{DD}/2$ unless otherwise stated.

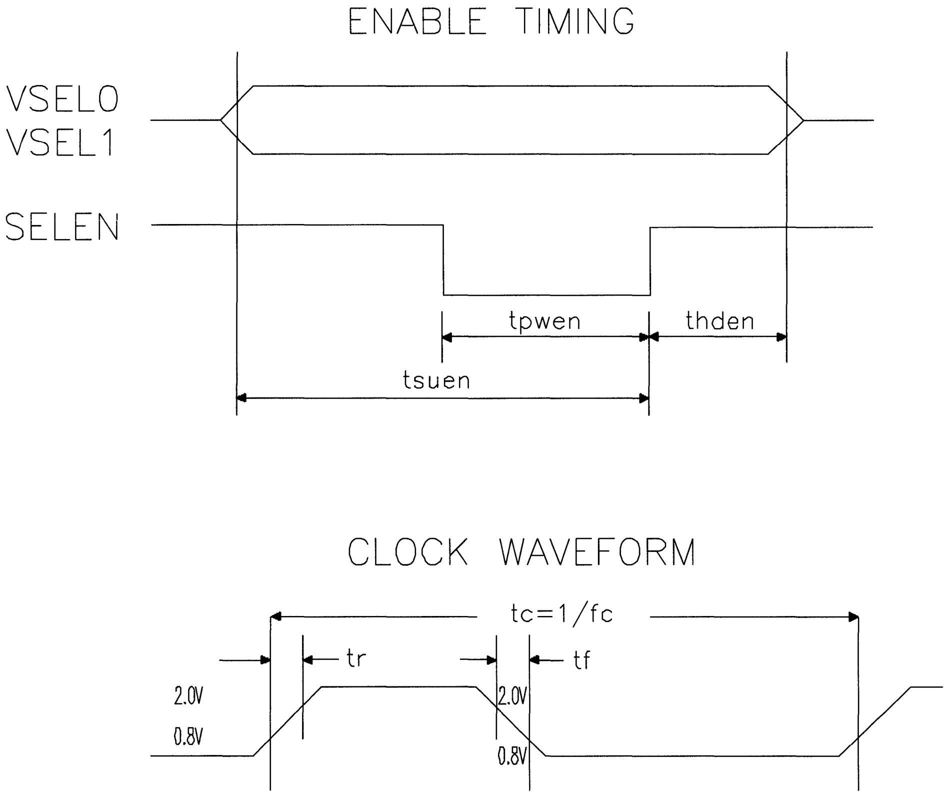
SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	20	-	
Thd	Hold Time Data to Strobe	10	-	
	MCLK and VCLK TIMINGS @ **5.0V**			
Tr	Rise Time	-	2	Duty Cycle 40% min. to 60% max.
Tf	Fall Time	-	2	
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	20	ns
-	Output Enable to Tristate (into and out of) time		15	ns
	MCLK and VCLK TIMINGS @ **3.3V**			
Tr	Rise Time	-	3	Duty Cycle 40% min. to 60% max.
Tf	Fall Time	-	3	
-	Frequency Error		.5	%
-	Maximum Frequency		110	MHz
-	Propagation Delay for Pass Through Frequency	-	30	ns
-	Output Enable to Tristate (into and out of) time		20	ns

DC Characteristics at 5 Volts V_{DD}

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range	4.75	5.25	V	
V_{IL}	Input Low Voltage	V_{SS}	0.8	V	$V_{DD} = 5V$
V_{IH}	Input High Voltage	2.0	V_{DD}	V	$V_{DD} = 5V$
I_{IH}	Input Leakage Current	-	10	µA	$V_{IN} = V_{CC}$
V_{OL}	Output Low Voltage	-	0.4	V	$I_{OL} = 8.0$ mA
V_{OH}	Output High Voltage	2.4	-	V	$I_{OH} = 8.0$ mA
I_{DD}	Supply Current	-	30	mA	VDD = 5V
R_{UP}	Internal pull-up Resistors	50	-	K ohms	$V_{IN} = 0.0V$
C_{in}	Input Pin Capacitance	-	8	pF	$F_C = 1$ MHz
C_{out}	Output Pin Capacitance	-	12	pF	$F_C = 1$ MHz
I_{PN}	Power-down Supply Current	-	1.0	µA	V_{DD}=3.3V
R_{DN}	Internal pull-down Equivalent	20	-	K ohms	V_{IN}=V_{DD}=5V

DC Characteristics at 3.3 Volts V_{DD}

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range	3.0	3.6	V	
V_{IL}	Input Low Voltage	V_{SS}	0.8	V	$V_{DD} = 3.3V$
V_{IH}	Input High Voltage	2.0	V_{DD}	V	$V_{DD} = 3.3V$
I_{IH}	Input Leakage Current	-	10	µA	$V_{in} = VDD$
V_{OL}	Output Low Voltage	-	0.4	V	$I_{OL} = 3.0$ mA
V_{OH}	Output High Voltage	2.4	-	V	$I_{OH} = 3.0$ mA
I_{DD}	Supply Current	-	20	mA	$V_{DD} = 3.3V$
R_{UP}	Internal pull-up Resistors	100	-	K ohms	$V_{IN} = 0.0V$
C_{in}	Input Pin Capacitance	-	8	pF	$F_C = 1$ MHz
C_{out}	Output Pin Capacitance	-	12	pF	$F_C = 1$ MHz
I_{PN}	Power-down Supply Current	-	1.0	µA	V_{DD} =3.3V
R_{DN}	Internal pull-down Equivalent	50	-	K ohms	V_{IN} =V_{DD} =3.3V



ICS90C65 Timing

Ordering Information

ICS90C65-XXXN or ICS90C65-XXXM or ICS90C65-XXXV

Example:

ICS XXXX-XXX N

Package Type
N=DIP (Plastic) V=PLCC
M=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3-6 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS9161A

Dual Programmable Graphics Frequency Generator

General Description

The **ICS9161** is a fully programmable graphics clock generator. It can generate user-specified clock frequencies using an externally generated input reference or a single crystal. The output frequency is programmed by entering a 24-bit digital word through the serial port. Two fully user-programmable phase-locked loops are offered in a single package. One PLL is designed to drive the memory clock, while the second drives the video clock. The outputs may be changed on-the-fly to any desired frequency between 390 kHz and 120 MHz. The **ICS9161** is ideally suited for any design where multiple or varying frequencies are required.

This part is ideal for graphics applications. It generates low jitter, high speed pixel clocks. It can be used to replace multiple, expensive high speed crystal oscillators. The flexibility of the device allows it to generate non-standard graphics clocks.

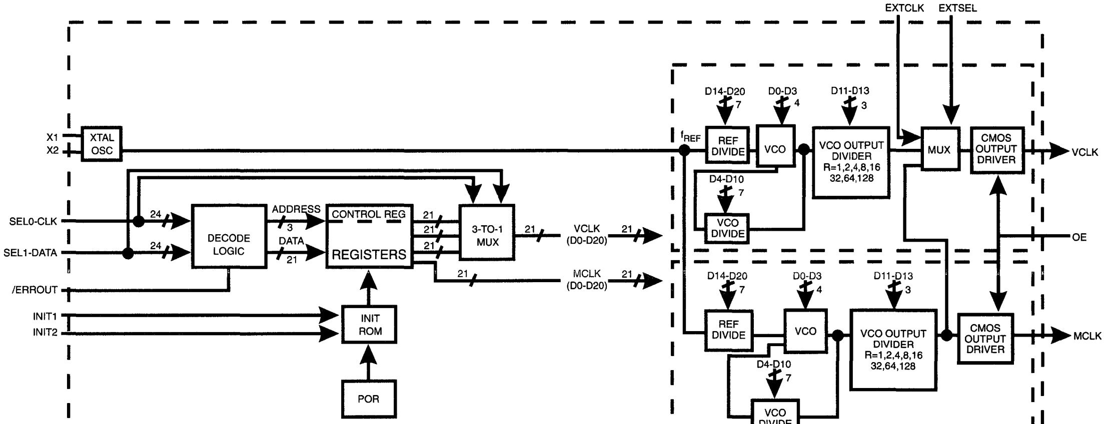
The **ICS9161** is also ideal in disk drives. It can generate zone clocks for constant density recording schemes. The low profile, 16-pin SOIC or PDIP package and low jitter outputs are especially attractive in board space critical disk drives.

The leader in the area of multiple output clocks on a single chip, ICS has been shipping graphics frequency generators since October, 1990, and is constantly improving the phase-locked loop. The **ICS9161** incorporates a patented fourth generation PLL that offers the best jitter performance available.

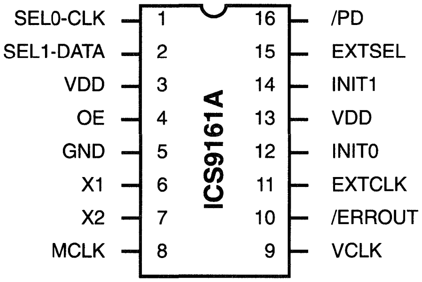
Features

- Pin-for-pin and function compatible with ICD2061A
- Dual programmable graphics clock generator
- Memory and video clocks are individually programmable on-the-fly
- Ideal for designs where multiple or varying frequencies are required
- Increased frequency resolution from optional pre-divide by 2 on the M counter
- Output enable feature available for tristating outputs
- Independent clock outputs range from 390 kHz to 120 MHz
- Operation up to 140 MHz available
- Power-down capabilities
- Low power, high speed 0.8µ CMOS technology
- Glitch-free transitions
- Available in 16-pin SOIC or PDIP package

Block Diagram



Pin Configuration



16-Pin SOIC or PDIP
K-6, K-4

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	SEL0-CLK		Clock input in serial programming mode Clock select pin in operating mode
2	SEL1-DATA		Data input in serial programming mode Clock select pin in operating mode
3	AVDD		Power
4	OE		Tristates outputs when low
5	GND		Ground
6	X1		Crystal input
7	X2		Crystal output
8	MCLK		Memory clock output
9	VCLK		Video clock output
10	/ERROUT		Output low signals an error in the serially programmed word
11	EXTCLK		External clock input
12	INIT0		Selects initial power-up conditions, LSB
13	VDD		Power
14	INIT1		Selects initial power-up conditions, MSB
15	EXTSEL		Selects external clock input (EXTCLK) as VCLK output
16	/PD		Power-down pin, active low

Register Definitions

The register file consists of the following six registers:

Register Addressing

Address	Register	Definition
000	REG0	Video Clock Register 1
001	REG1	Video Clock Register 2
010	REG2	Video Clock Register 3
011	MREG	Memory Register
100	PWRDWN	Divisor for Power-down mode
110	CNTL REG	Control Register

The **ICS9161** places the three video clock registers and the memory clock register in a known state upon power-up. The registers are initialized based on the state of the INIT1 and INIT0 pins at application of power to the device. The INIT pins must ramp up with VDD if a logical 1 on either pin is required. These input pins are internally pulled down and will default to a logical 0 if left unconnected.

The registers are initialized as follows:

Register Initialization

INIT1	INIT0	MREG	REG0	REG1	REG2
0	0	32.500	25.175	28.322	28.322
0	1	40.000	25.175	28.322	28.322
1	0	50.350	40.000	28.322	28.322
1	1	56.644	40.000	50.350	50.350

Register Selection

When the **ICS9161** is operating, the video clock output is controlled with a combination of the SEL0, SEL1, /PD and OE pins. The video clock is also multiplexed to an external clock (EXTCLK) which can be selected with the EXTSEL pin. The VCLK Selection Table shows how VCLK is selected.

VCLK Selection

OE	/PD	EXTSEL	SEL1	SEL0	VCLK
0	x	x	x	x	Tristate
1	0	x	x	x	Forced High
1	1	x	0	0	REG0
1	1	x	0	1	REG1
1	1	0	1	0	EXTCLK
1	1	1	1	x	REG2
1	1	x	1	1	REG2

As seen in the VCLK Selection table, OE acts to tristate the output. The /PD pin forces the VCLK signal high while powering down the part. The EXTCLK pin will only be multiplexed in when EXTSEL and SEL0 are logic 0 and SEL1 is a logic 1.

The memory clock outputs are controlled by /PD and OE as follows:

MCLK Selection

OE	/PD	MCLK
0	x	Tristate
1	1	MREG
1	0	PWRDWN

The Clock Select pins SEL0 and SEL1 have two purposes. In serial programming mode, these pins act as the clock and data pins. New data bits come in on SEL1 and these bits are clocked in by a signal on SEL0. While these pins are acquiring new information, the VCLK signal remains unchanged. When SEL0 and SEL1 are acting as register selects, a time-out interval is required to determine whether the user is selecting a new register or wants to program the part. During this initial time-out, the VCLK signal remains at its previous frequency. At the end of this time-out interval, a new register is selected. A second time-out interval is required to allow the VCO to settle to its new value. During this period of time, typically 5 msec, the input reference signal is multiplexed to the VCLK signal.

When MCLK or the active VCLK register is being re-programmed, then the reference signal is multiplexed glitch-free to the output during the first time-out interval. A second time-out interval is also required to allow the VCO to settle. During this period, the reference signal is multiplexed to the appropriate output signal.

Control Register Definitions

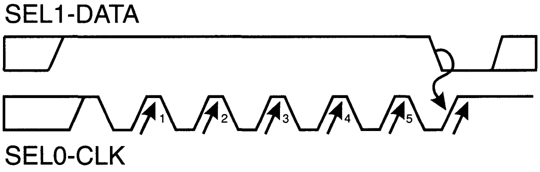
The control register allows the user to adjust various internal options. The register is defined as follows:

Bit	Bit Name	Default Value	Description
9	C5	0	This bit determines which power-down mode the /PD pin will implement. Power-down mode 1, C5=0, forces the MCLK signals to be a function of the power-down register. Power-down mode 2, C5=1, turns off the crystal and disables all outputs.
8	C4	0	This bit determines which clock is multiplexed to VCLK during frequency changes. C4=0 multiplexes the reference frequency to the VCLK output. C4=1 multiplexes MCLK to the VCLK output for applications where the graphics controller cannot run as slow as f_{REF}.
7	C3	0	This bit determines the length of the time-out interval. The time-out interval is derived from the MCLK VCO. If this VCO is programmed to certain extremes, the time-out interval may be too short. C3=0, normal time-out. C3=1, doubled time-out interval.
6	C2	0	Reserved, must be set to 0.
5	C1	1	This bit adjusts the duty cycle. C1=0 causes a 1ns decrease in output high time. C1=1 causes no adjustment. If the load capacitance is high, the adjustment can bring the duty cycle closer to 50%.
4	C0	0	Reserved, must be set to 0.
3	NS2	0	Acts on register 2. NS2=0 prescales the N counter by 2. NS2=1 prescales the P counter value to 4.
2	NS1	0	Acts on register 1. NS1=0 prescales the N counter by 2. NS1=1 prescales the P counter value to 4.
1	NS0	0	Acts on register 0. NS1=0 prescales the N counter by 2. NS0=1 prescales the P counter value to 4.

Serial Programming Architecture

The pins SEL0 and SEL1 perform the dual functions of selecting registers and serial programming. In serial programming mode, SEL0 acts as a clock pin while SEL1 acts as the data pin. The **ICS9161-01** may not be serially programmed when in power-down mode.

In order to program a particular register, an unlocking sequence must occur. The unlocking sequence is detailed in the following timing diagram:



The unlock sequence consists of at least five low-to-high transitions of CLK while data is high, followed immediately by a single low-to-high transition while data is low. Following this unlock sequence, data can be loaded into the serial data register.

Following any transition of CLK or DATA, the watchdog timer is reset and begins counting. The watchdog timer ensures that successive rising edges of CLK and DATA do not violate the time-out specification of 2ms. If a time-out occurs, the lock mechanism is reset and the data in the serial data register is ignored.

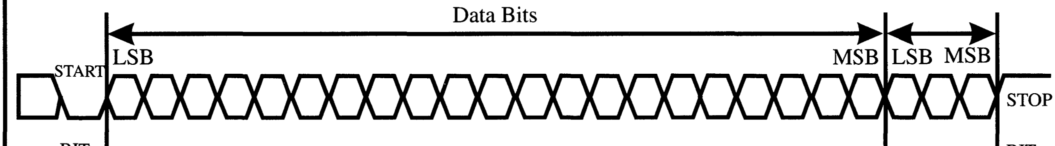
Since the VCLK registers are selected by the SEL0 and SEL1 pins, and since any change in their state may affect the output frequency, new data input on the selection bits is only permitted to pass through the decode logic after the watchdog timer has timed out. This delay of SEL0 or SEL1 data permits a serial program cycle to occur without affecting the current register selection.

Serial Data Register

The serial data is clocked into the serial data register in the order described in Figure 1 below (Serial Data Timing).

The serial data is sent as follows: An individual data bit is sampled on the rising edge of CLK. The complement of the data bit must be sampled on the previous falling edge of CLK. The setup and hold time requirements must be met on both CLK edges. For specifics on timing, see the timing diagrams on pages 10, 11 and 12.

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit. A total of 24 bits must always be loaded into the serial data register or an error is issued. Following the entry of the last data bit, a stop bit or load command is issued by bringing DATA high and toggling CLK high-to-low and low-to-high. The unlocking mechanism then resets itself following the load. Only after a time-out period are the SEL0 and SEL1 pins allowed to return to a register selection function.



BITs	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	BITs
VCO Prog-Word	M'0	M'1	M'2	M'3	M'4	M'5	M'6	R0	R1	R2	N'0	N'1	N'2	N'3	N'4	N'5	N'6	I0	I1	I2	I3	A0	A1	A2	VCO Prog-Word
CNTL Reg	0	0	0	0	0	0	0	0	0	0	0	0	PS0	PS1	PS2	C0	C1	C2	C3	C4	C5	0	1	1	CNTL Reg
PWRDWN Reg																									PWRDWN Reg

Figure 1: Serial Data Timing

The serial data register is exactly 24 bits long, enough to accept the data being sent. The stop bit acts as a load command that passes the contents of the Serial Data Register into the register indicated by the three address bits. If a stop bit is not received after the serial register is full, and more data is sent, all data in the register is ignored and an error issued. If correct data is received, then the unlocking mechanism re-arms, all data in the serial data register is ignored, and an error is issued.

/ERROUT Operation

Any error in programming the **ICS9161** is signaled by /ERROUT. When the pin goes low, an error has been detected. It stays low until the next unlock sequence. The signal is invoked for any of the following errors: incorrect start bit, incorrect data encoding, incorrect length of data word, and incorrect stop bit.

Programming the ICS9161

The **ICS9161** has a wide operating range, but it is recommended that it is operated within the following limits:

1 MHz <F_{REF} <60 MHz	F_{REF}=Input Reference Frequency
200 kHz <$F_{REF/M}$ <5 MHz	M=Reference divide 3 to 129
50 MHz < F_{VCO} <120 MHz	F_{VCO}=VCO output frequency
$F_{CLK} \leq$ 120 MHz	F_{CLK}=output frequency

The frequency of the programmable oscillator F_{VCO} is determined by the following fields:

Field	# of Bits
Index (I)	4
N counter value (N')	7
Mux (R)	3
M counter value (M')	7

Where the least significant bit is the last bit of M and the most significant bit is the first bit of I.

The equations used to determine the oscillator frequency are:

$$N=N' + 3 \quad M=M' + 2$$

$$F_{VCO}=\text{Prescale} \bullet N/M \bullet F_{REF}$$

$$\text{where } 3 \leq M \leq 129 \text{ and } 4 \leq N \leq 130$$

and prescale=2 or 4, as set in the control register

The value of F_{VCO} must remain between 50 MHz and 120 MHz. As a result, for output frequencies below 50 MHz, F_{VCO} must be brought into range. To achieve this, an output divisor is selected by setting the values of the Mux Field (R) as follows:

Output Divisor

R	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

Unlike the ICD2061A, the **ICS9161**'s VCO does not require tuning to place it in certain ranges. The **ICS9161**'s VCO will operate from 50 MHz to 120 MHz without adjusting the VCO gain. However, to maintain compatibility, the I bits are programmed as in the ICD2061A.

These bits are dummy bits except for the following two cases:

Index Field (I)

I	VCLK F_{VCO}	MCLK F_{VCO}
1110	Turn off VCLK	50 - 120 MHz
1111	Mux MCLK to VLCK	50 - 120 MHz

When the index field is set to 1111, VCLK is turned off and both channels run from the same MCLK VCO. This is done in an effort to reduce jitter, which may increase when VCOs run at 2^n multiples of one another. If the two outputs must be multiples of one another, it is best to mux MCLK over to the output of the VCLK VCO, and to power-down the VCLK VCO. The multiplexed frequency will be divided down by the correct divisor (M) and output on VCLK.

Power Management Issues

Power-down mode 1

The **ICS9161** contains a mechanism to reduce the quiescent power when stand-by operation is desired. Power-down mode 1 is invoked by polling /PD low and having the proper CNTL register bit set to zero. In this mode, VCOs are shut down, the VCLK output is forced high, and the MCLK output is set to a user-defined low frequency value to refresh dynamic RAM.

The power-down MCLK value is determined by the following equation:

$$MCLK_{PD} = F_{REF}/(\text{PWRDWN register divisor value})$$

The power-down register divisor is determined according to the 4-bit word programmed into the PWRDWN register (see table below).

Power-down mode 2

When there is no need for any output during power-down, an alternate mode is available which will completely shut down all outputs and the reference oscillator, but still preserves all register contents. Power-down mode 2 in invoked by first programming the power-down bit in the CNTL register and then pulling the /PD pin low.

The /PD pin

The /PD pin has a standard internal pull-up resistor during normal operation. When the chip goes into power-down mode 1 or 2, the normal pull-up resistor is dynamically switched to a weak pull-up, which reduces power consumption. If the /PD pin is allowed to float after it has been pulled down, the weak pull-up will bring the signal high and allow the device to resume operation.

Power-Down Register Table

PWRDWN bits				PWRDWN Register Value	Power-down Divisor	$MCLK_{PD}$ (f_{REF}=14.31818)
P3	P2	P1	P0			
0	0	0	0	0	n/a	n/a
0	0	0	1	1	32	447.4 kHz
0	0	1	0	2	30	477.3 kHz
0	0	1	1	3	28	511.4 kHz
0	1	0	0	4	26	550.7 kHz
0	1	0	1	5	24	596.6 kHz
0	1	1	0	6	22	650.8 kHz
0	1	1	1	7	20	715.9 kHz
1	0	0	0	8 (default)	18	795.5 kHz
1	0	0	1	9	16	894.9 kHz
1	0	1	0	A	14	1.02 MHz
1	0	1	1	B	12	1.19 MHz
1	1	0	0	C	10	1.43 MHz
1	1	0	1	D	8	1.79 MHz
1	1	1	0	E	6	2.39 MHz
1	1	1	1	F	4	3.58 MHz

Absolute Maximum Ratings

VDD referenced to GND	7V
Operating temperature under bias	0°C to 70°C
Storage temperature	-40°C to +150°C
Voltage on I/O pins referenced to GND	GND -0.5V to VDD +0.5V
Power dissipation	0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} = +5V ± 5%, 0°C ≤ $T_{AMBIENT}$ ≤ +70°C unless otherwise stated

Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply voltage relative to GND	VDD	-0.5	7.0	Volts
Input voltage with respect to GND	V_{IN}	-0.5	VDD +0.5	Volts
Operating temperature	T_{OPER}	0	+70	°C
Storage temperature	T_{STOR}	-65	+150	°C
Max soldering temperature (10 sec)	T_{SOL}		+260	°C
Junction temperature	T_j		+125	°C
Package power dissipation	P_{DISS}		350	mWatts

DC Characteristics

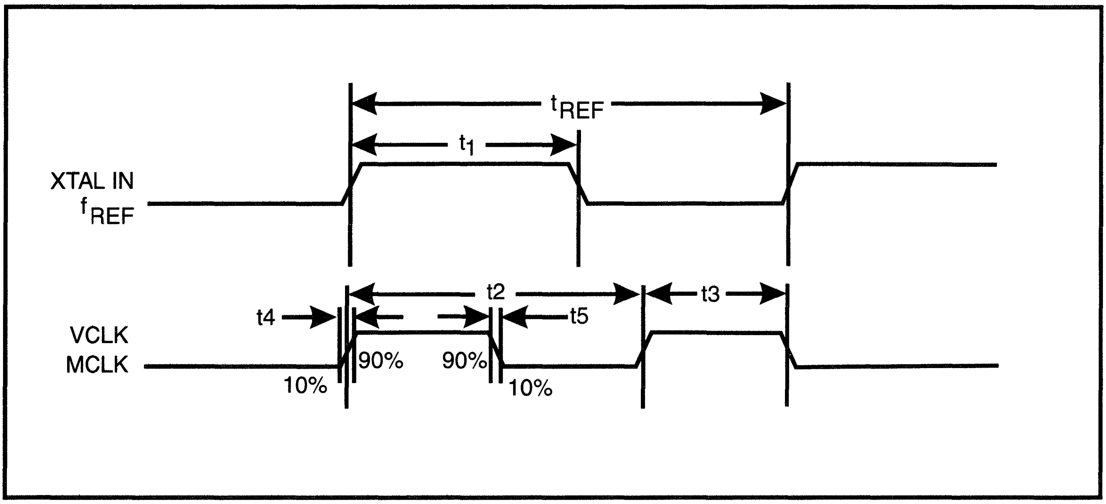
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
High level input voltage	V_{IH}		2.0			V
Low level input voltage	V_{IL}				0.8	V
High level CMOS output voltage	V_{OH}	I_{OH}=-4ma	3.84			V
Low level output voltage	V_{OL}	I_{OL}=4ma			0.4	V
Input high current	I_{IH}	V_{IH}=5.25V			100	µA
Input low current	I_{IL}	V_{IL}=0V			-250	µA
Output leakage current	I_{OZ}	(tristate)			10	µA
Power supply current	I_{DD}		15		65	ma
Power supply current (typical)	$I_{DD\text{-}TYP}$	@60 MHz		35		ma
Analog power supply current	I_{ADD}				20	ma
Power-down current (Mode 1)	I_{PD1}			6	7.5	ma
Power-down current (Mode 2)	I_{PD2}			25	50	µA
Input capacitance	C_{IN}				10	pf

Electrical Characteristics *(continued)*

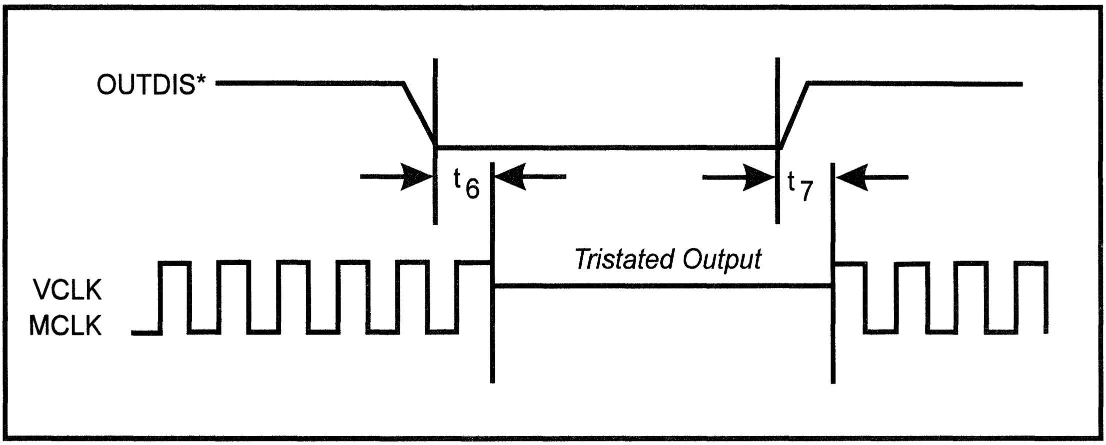
AC Characteristics						
DESCRIPTION	NAME	SYMBOL	MIN	TYP	MAX	UNITS
Reference oscillator value (Note 1)	Reference frequency	f_{REF}	1	14.31818	60	MHz
1/f_{REF}	Reference period	t_{REF}	16.6	69.8408	1000	ns
Duty cycle for the input oscillator defined as t_1/t_{REF}	Input duty cycle	t_1	25%		75%	
Output oscillator values	Output clock periods	t_2	8.33 (120 MHz)		2564 (390 kHz)	ns
Duty cycle for the output oscillators (note 2)	Output duty cycle	t_3	45%		55%	
Rise time for the output oscillators into a 25pf load	Rise times	t_4			3	ns
Fall time for the output oscillators into a 25pf load	Fall times	t_5			3	ns
Old frequency output	freq1 output	t_{freq1}				
New frequency output	freq2 output	t_{freq2}				
Time clock output remains high while output muxes to reference frequency	f_{REF} mux time	t_A	0.5t_{REF}		1.5t_{REF}	ns
Interval for serial programming and for VCO changes to settle (Note 3)	Time-out interval	$t_{time\text{-}out}$	2	5	10	ms
Time clock output remains high while output muxes to new frequency value	t_{freq2}muxtime	t_B	$^{0\ 5}t_{REF}$	$^{1\ 5}t_{REF}$		ns
Time for the output oscillators to go into tristate mode after OUTDIS-signal assertion	Tristate	t_6		25		ns
Time for the output oscillators to recover from tristate mode after OUTDIS-signal goes high	CLK valid	t_7		12		ns
Time for power-down mode of operation to take effect	Power-Down	t_8		25		ns
Time for recovery from power-down mode to a valid CLK	Power-Up	t_9		12		ns
Time for MCLK to go high after PWRDWN is asserted high	MCLKOUT high	t_{10}	0		t_{PWRDWN}	ns
Delay of MCLK prior to f_{MCLK} signal at output	MCLKOUT delay	t_{11}	$^{0.5}t_{MCLK}$		$^{1\ 5}t_{MCLK}$	ns
Clock period of serial clock		t_{serclk}	2 • t_{REF}		2	msec
Set-up time		t_{SU}	20			ns
Hold time		t_{HD}	10			ns
Load command		t_{ldcmd}	0		t_1+30	ns

Notes:

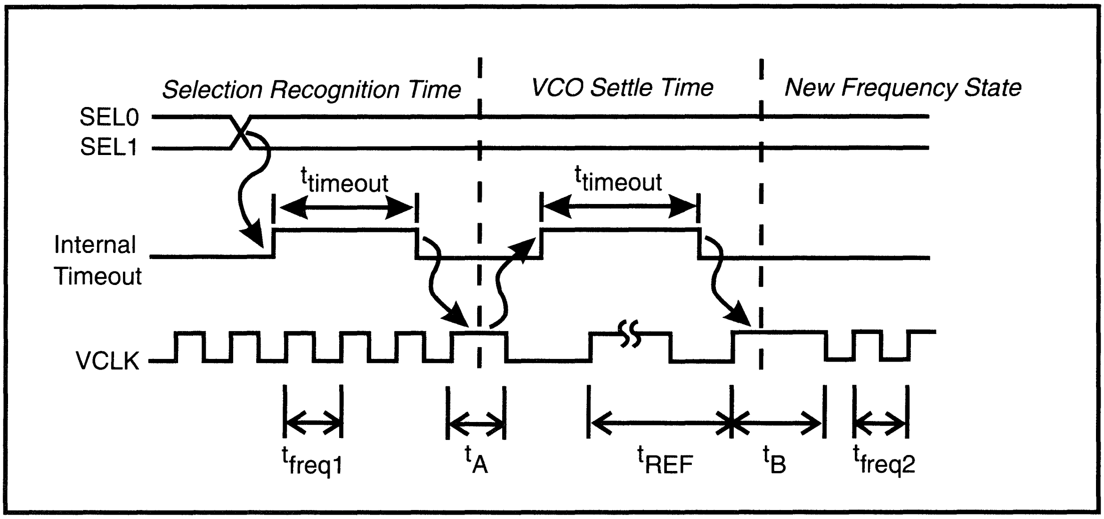
1. For reference frequencies other than 14.81818 MHz, the pre-loaded ROM frequencies will shift proportionally.
2. Duty cycle is measured at CMOS threshold levels. At 5 volts, V_{TH}=2.5 volts.
3. If the interval is too short, see the time-out interval section in the control register definition.



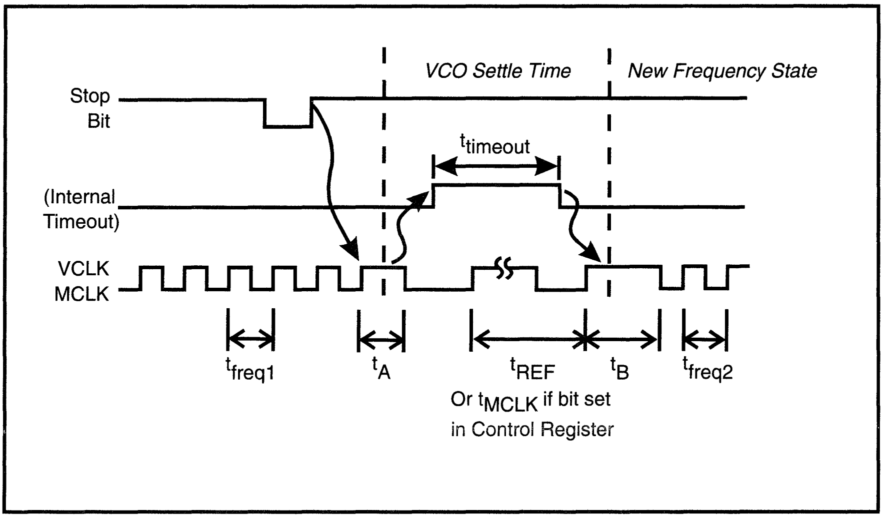
Rise and Fall Times



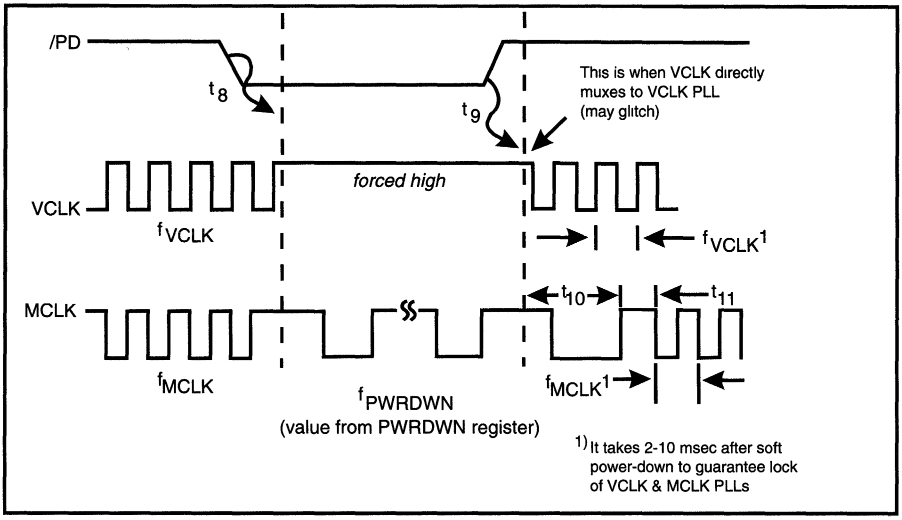
Tristated Timing



Selection Timing

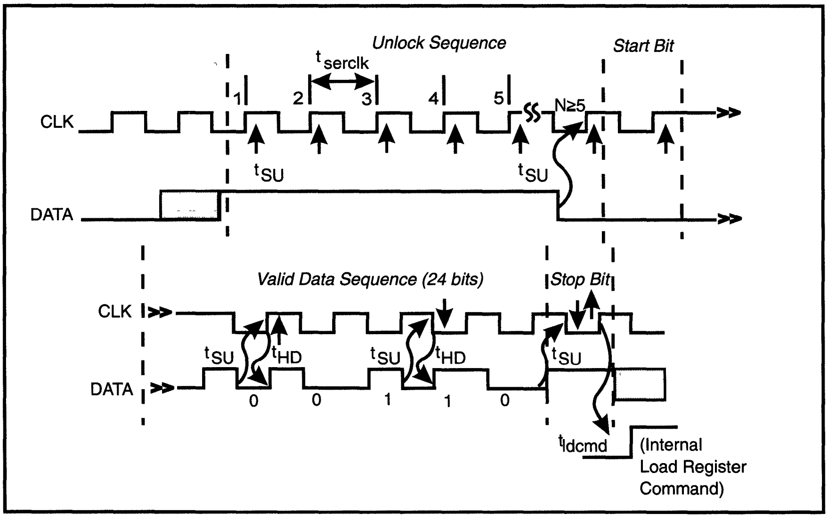


MCLK and Active VCLK Register Programming Timing



1) It takes 2-10 msec after soft power-down to guarantee lock of VCLK & MCLK PLLs

Soft Power-Down Timing (Mode 2)



Serial Programming Timing

Ordering Information

ICS9161CN16 or ICS9161CW16

Example:

ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
N=DIP (Plastic)
W=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns, if applicable)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

ICS

Video Timing Generator Applications

Integrated
Circuit
Systems, Inc.

AN01

Clock Generators Application Note

Designing with ICS Video Dot Clock Generators

The ICS family of dot clock generators is a simple to use, cost-effective solution to the generation of dot clock frequencies required by VGA and other graphics subsystems. Application of these parts is fairly straightforward; however, certain precautions should be taken to insure a low phase jitter implementation when laying out circuit boards. The ICS dot clock products are high-speed high-performance mixed analog/digital IC products. As such they are capable of generating very fast risetime signals (<1.5 nanoseconds). Although ICS dot clock generators have digital inputs and outputs, they are **precision analog ICs**. They are dependent internally on stable, noise-free analog signals in the microvolt region for jitter-free operation.

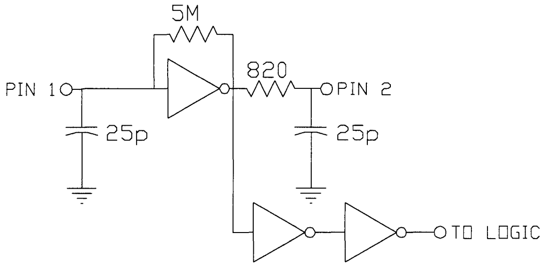
Grounding

The most common reason for poor performance of graphics subsystems products is inadequate grounding. To achieve maximum performance, a ground plane layer will be required for the area on which the dot clock generator is placed. Typical graphics cards already have this layer as many other parts of the subsystem such as the DRAM and Ramdac require this as well. To prevent ground loops and circulating currents associated with other parts of the subsystem from generating differential voltages across the circuitry used with the dot clock, a cut should be made in the groundplane layer surrounding the dot clock circuitry so that it connects with the main part of the groundplane at one point. Preferably this will lead to a low noise area close to the card edge connector. This insures that signals related to logic, DRAM memory, and other circuitry will not be superimposed on VCO control inputs.

The Two-Layer VGA Board

Recently, competitive pressure in the VGA adapter market has resulted in a high level of interest in designing a two-layer VGA PC board. With some compromise in jitter performance, a successful two layer design may be achieved. **The success of a two layer design is totally dependent on board layout.** Video RAM represents a highly capacitive load to the VGA controller. Read/write operations result in high currents in the order of amperes on the VGA board. If these current pulses interact with the dot clock generator via common ground paths, etc. the result will be highly unsatisfactory. If the ground paths to the VGA controller are not robust, the relative ground bounce of the VGA controller, dot clock generator, and Ramdac will create visually apparent problems. Component placement must be carefully thought out with respect to ground currents if a two layer design is to be successful. We strongly suggest that you contact ICS applications engineering and submit a copy of your layout and PCB artwork to us before you purchase boards.

Internal Crystal Oscillator



Crystal Oscillator & Crystal Selection

Most of the ICS family of dot clock generators have circuitry onboard to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode. See the AC Characteristics in the appropriate data sheet for the effective capacitive loading to specify when ordering crystals.

So called series-resonant crystals may also be used with the ICS dot clock generators. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.005-0.01%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. As it is necessary for this circuitry to be biased into the linear region to implement the oscillator function these pins are susceptible to noise pickup. Avoid routing digital signals or the dot clock generator outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

Reference Frequency

Alternatively, the bus clock signal at 14.31818 may be used. If this is done, an on-board buffer should be used to clean up this signal, and prevent problems with noise, ringing, and overshoot. If a bipolar buffer is used, the signal should be capacitively coupled to XTAL1 as the internal oscillator is internally biased to a $V_{DD}/2$ threshold. A .047 or .1 microfarad capacitor is recommended for this application. HCMOS buffers may be directly connected to XTAL1 through a 33 ohm series resistor. XTAL2 must be left unconnected if an external clock is used.

Bypassing

High frequency bypassing of the ICS dot clock generator is mandatory for proper operation. Short, low inductance connections are important between the analog and digital V_{DD} pins to the bypass capacitors and from the capacitor to ground. When selecting capacitors to bypass this or any other high-frequency device, the frequency of most concern is not the operating frequency of the device, but the frequency equivalent to 1/risetime, in this case 500 MHz. Multiple bypass capacitors are preferable, with a small ceramic disk placed as close as possible to the supply pin. The capacitor, its leads, and the interconnect leads form a series resonant circuit. This circuit should be resonant at a frequency well above the frequency of interest (500 MHz). Therefore capacitor values of .047 microfarad or less will provide more effective bypassing, forcing the bypassing to operate on the capacitive side of resonance. A larger (1 microfarad or greater) tantalum bypass should parallel this to reject lower frequency noise.

"Microphonics"

ICS applications engineering occasionally receives complaints about graphics subsystems being "microphonic." It is claimed that our parts are subject to output jitter if they are tapped on or vibrated. These problems invariably show up on surface-mount board designs. When investigated, the problem always turns out to be ceramic capacitors.

Small surface-mount ceramic capacitors are made with barium titanate dielectric material. Barium titanate is also used to make microphones, ultrasonic transducers etc., as it is one of the most efficient piezoelectric material. Soldering these capacitors to a G10 glass epoxy PC board results in the capacitor being placed in mechanical compression, as the glass/epoxy material has a much higher coefficient of thermal expansion than does the barium titanate, a ceramic. When the PCB cools after a soldering operation the capacitor is partially compressed and rigidly atached to the board. Any vibration transmitted to the board results in flexure of the capacitor which outputs a resultant voltage. Although the same materials are used to make leaded components, the wire leads decouple the mechanical stress and vibration from the capacitor, and no problem results.

This phenomenon caused difficulties with graphics subsystems that used our first generation devices such as the ICS1394, ICS1560, and ICS90C63 which had external-loop filter components. The advent of second generation dot clock devices with integral loop filters has all but eliminated this problem if double bypassing is used. The larger tantalum capacitor is non-microphonic even in surface mount, and readily absorbs mechanically generated voltage spikes from the smaller (but more effective at high frequencies) ceramic capacitor.

Soldering Considerations

A problem that ICS applications engineering is beginning to see quite often is related to the new water-based fluxes. Until quite recently most fluxes used for PC board assembly were of the activated rosin type. Wave soldering machines sprayed flux directly on the solder side of the PCB, then the board traveled through the solder wave. Boards were then run through a vapor degreaser where trichlorethelyne (TCE) or Freon were used to remove residual flux. Environmental considerations have all but eliminated the use of these substances for flux removal.

Rosin based fluxes are very stable non-conductive materials at room temperatures and cause few problems even when poorly cleaned. Water-based fluxes are hygroscopic, that is they absorb water from the water vapor present in air. As they are ionic compounds, they can cause a resistive film to be left on boards that have been improperly cleaned. In addition, the incresased usage of surface mount technology has resulted in components being much closer to the PC board surface, making it harder to adequately remove flux from under these components. The smaller lead spacing and higher density of these boards results in shorter leakage paths, and a higher probability of leakage related problems. The problem typically manifests itself as a crystal oscillator startup problem. A customer will call ICS and say that one of our dot clock generator products refused to start. Replacing the device fixed the problem. As they have experienced the problem several times they are requesting ICS Quality Assurance to run a failure analysis. When we retest their parts all appear to work normally.

When the customer replaced the part he inadvertently fixed the problem. Board repair is invariably done with a soldering iron and rosin core solder. Most often an aerosol can of flux remover is used to clean up after a repair. Heating the solder pads to remove and replace the suspected device will drive any moisture from the PC board. The rosin flux has substances to entrap or neutralize ionic contaminants and, even if not properly cleaned, leaves a waterproof coating. With the offending conductive residue removed, the crystal oscillator circuitry is now capable of biasing itself back into the linear region and will be able to start.

This source of problems could also cause jitter related problems in first generation devices with external loop filter components, as this circuitry exhibits very high impedances. Straight digital circuitry is relatively immune to these problems; however, it may be causing similar problems with Ramdac circuitry.

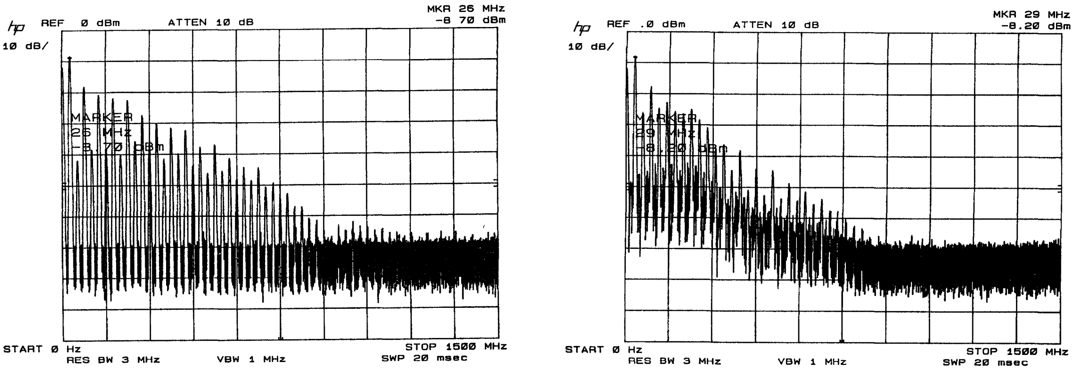
Make sure your PC board assembly operation is regularly tested for ionic contamination and you will never see this problem.

Output Considerations

The output circuitry of the ICS family of dot clock generator products exhibits a characteristic impedance of approximately 33 ohms. A series resistor of 33 ohms and an inexpensive ferrite bead in series with the output will greatly reduce the radiated harmonics of the output signal without otherwise impairing performance. This may be helpful in meeting FCC requirements. The ICS dot clock generator has consistently produced less interference than fixed frequency crystal oscillators in this respect, as it is only producing one frequency at a time and has nicely controlled rise and fall times. See the comparative spectral plots of the ICS dot clock generators and crystal oscillators and note the relatively rapid rate that high frequency harmonics fall off for the dot clock generator. **In no case should a capacitor be connected from the output signal to ground.** At the frequency equivalent to the risetime (500MHz) even a 6 picofarad oscilloscope probe is equivalent to a 50 ohm reactance. The current, to charge and discharge this capacitor, has to be provided from V_{DD} and ground. This capacitive loading defeats the purpose of our carefully controlled bypassing circuitry, and is not required for meeting FCC interference requirements, if the series resistor and ferrite bead are used.

Power Supply Considerations

ICS dot clock generators function as phase-locked loops. A stable reference frequency is generated by the crystal oscillator. This frequency is divided down by a variable modulus frequency divider and fed to the reference input of the phase comparator. The feedback input of this phase comparator is fed by a second variable modulus frequency divider; however, this divider chain is driven by a voltage-controlled oscillator (VCO). The output of the phase comparator is a tristate signal which produces a pulse which has a width proportional to the phase difference between the reference and feedback inputs. The polarity of these error pulses is dependent on whether the feedback input leads or lags the reference input. These correction pulses are integrated in the loop filter and are applied to the VCO input in such a polarity as to minimize the phase error. In a perfect system this loop would settle with no remaining phase error and remain there until a new frequency was required and different modulo divisors were selected. In practice, the loop can correct for external disturbances as long as these disturbances occur more slowly than the loop natural frequency. Changes in power supply voltage affect the gain of the VCO, and the phase comparator. If they happen slowly enough, the loop compensates and no error is introduced. Step changes cannot be compensated for and must be eliminated.



XTAL OSC

ICS Dot Clock Generator

Output Spectrum

When a higher voltage supply is available, the simplest approach is to regulate the analog supply voltage and eliminate the disturbance. In desktop PCs the +12 volt supply can be used either with a three terminal regulator or a zener diode and dropping resistor.

Laptop and notebook computers pose a more difficult problem in that a higher voltage supply is not usually available. The laptop/notebook electrical environment is more benign than the desktop computer environment, as there is no provision for using add-on boards that may inject unknown quantities of noise into the system. ICS dot clock generators are not particularly critical as to absolute supply voltage level, only to step disturbances. A series resistor and bypass tantalum electrolytic capacitor can be used to limit the rate of change in supply voltage to a rate that can be handled by the phase-locked loop. Two configurations are shown. Figure B is probably better where the VGA controller presents steady-state frequency-select information to the dot clock generator. In applications where the VGA controller presents frequency-select information on a bus and strobes the dot clock generator when frequency-select data is valid. Figure C is probably more appropriate because the bus signals may overshoot and inject noise through the input protection diodes.

Summary

ICS dot clock generators have revolutionized the personal computer and workstation graphics function.The capability to generate virtually any desired frequency at less cost than a single crystal oscilator has expanded the versatility of today's graphics systems for the PC beyond where high end workstation performance was a few years ago. Size, PC board real estate, and power requirements have shrunk to the point where today's laptop and notebook computers have graphics performance nearly as good as desktop machines. Systems design of a high-performance graphics system has been simplified so that with a few design precautions outlined above high-performance graphics can be implemented in any system.

Typical Power Supply Configurations

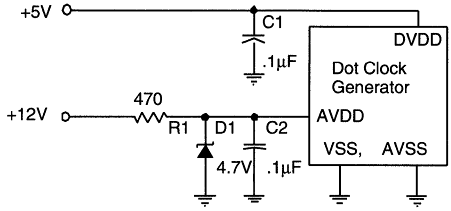


FIGURE A
OPTIMUM DESKTOP POWER CIRCUITRY

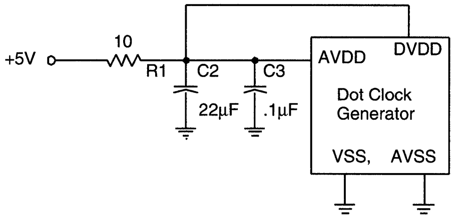


FIGURE B
LAPTOP/NOTEBOOK COMPUTER POWER CIRCUITS

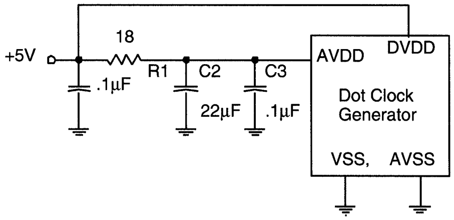
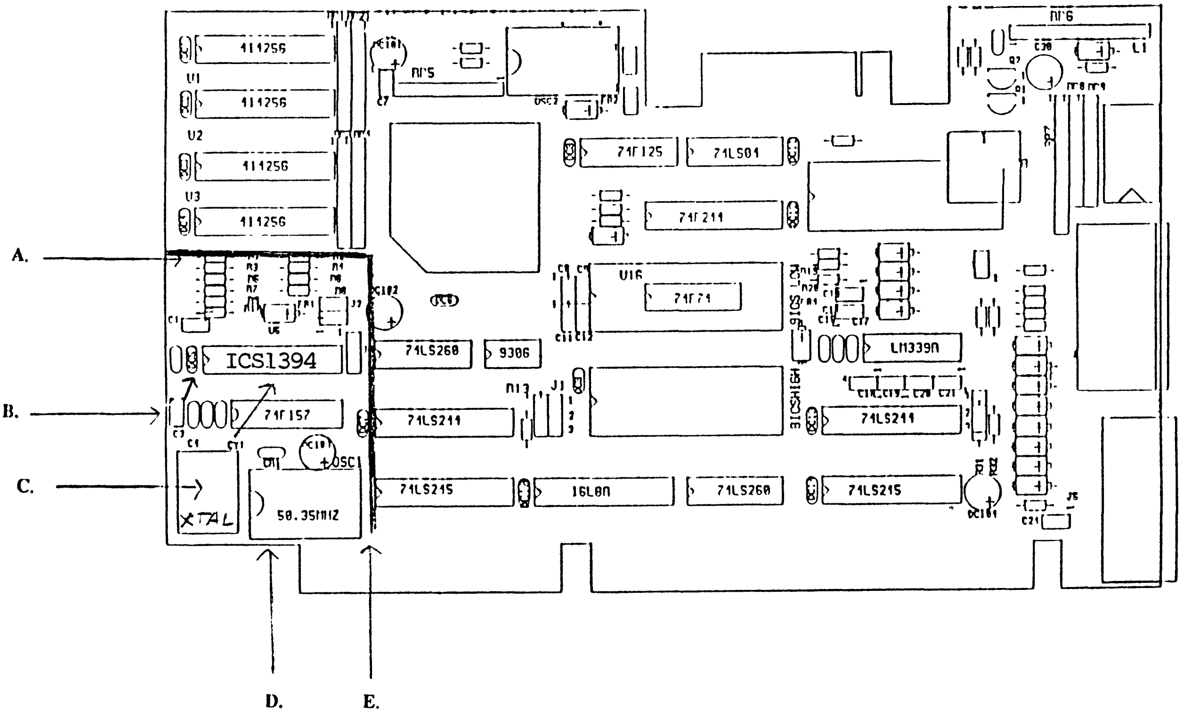


FIGURE C
LAPTOP/NOTEBOOK COMPUTER POWER CIRCUITS

Common VGA Board Layout Mistakes



Suggestions for a better layout:

A. Keep loop filter components (where required) close to dot clock generator and away from high speed DRAM circuitry.

B. Keep by-pass capacitor close to AV_{DD} pin.

C. Move XTAL close to pins XTAL1 and XTAL2. Keep fast logic signals away from this area.

D. Move oscillator can up between RAM and dot clock passive components.

E. Break ground plane level to create unipotential ground connection for dot clock circuitry.

Understanding ICS Data Sheet Jitter Specifications

Introduction

ICS clock generator devices utilize frequency synthesis based on phase locked loop (PLL) technology. Unless carefully designed, PLL-based clock generators are subject to excessive period variation, or "jitter." This applications brief will help in the understanding of ICS jitter specifications.

In most processor and time keeping applications, an excess of clock jitter does not affect operation. However, in other applications such as video, data acquisition or data recovery, clock jitter characteristics can be an important system design consideration. ICS is the most experienced manufacturer of video and processor clock devices and has perfected PLL based clock design. ICS produces clock devices exhibiting the lowest jitter and the least susceptibility to power supply noise.

Understanding ICS Jitter Specifications

Many of the ICS clock generator data sheets list output clock jitter specifications in the AC Characteristics section. ICS defines clock jitter as the difference in time of any given clock period as compared to the mean clock period, which is defined as 1/frequency. This can be expressed as time (psec) or as a percentage of the clock period.

Jitter, Absolute is the maximum deviation that would be expected (plus or minus) from a mean clock period.

Jitter, 1 Sigma is similar to an *average* deviation that would be expected (plus or minus).from a mean clock period. This specification assumes that, statistically, a sample of clock cycle periods follow a normal probability function, which indeed it typically does. *Jitter, 1 Sigma* is the jitter value at one standard deviation (one sigma) of the jitter measurement population. This specification is useful in graphics applications.

How ICS Clock Jitter is Measured

ICS characterizes output clock jitter using a Stanford Research SR620 Time Interval Analyzer. This instrument is set up to take 10,000 clock period samples over a several second period, therefore, random noncontiguous clock periods are sampled. The measure data provided by the instrument is the ***typical*** value listed in the data sheet (the SR620 provides both *1 Sigma* and *Absolute* measurements). The ***maximum*** value listed is the worst case measurement expected over the output frequency range, changes in operating conditions such as supply voltage and temperature, and changes in the semiconductor process.

Integrated Circuit Systems, Inc.

AN03

Clock Generators Application Note

Clock Output Frequency Accuracy and Input Reference Topics

This application note addresses output frequency accuracy of ICS Clock Synthesizers. Output frequency accuracy is determined both by the programmable set size of the PLL and input reference frequency accuracy. Input reference circuits are also discussed, with emphasis on using a discrete quartz crystal device.

Determining Your Frequency Accuracy Needs

ICS clock synthesizer devices are used in a diversity of applications all of which have different clock accuracy requirements. For example, in VGA graphics applications, the pixel clock frequency can easily tolerate an inaccuracy of 0.5% (5,000 ppm or part-per-million) or more since CRT timing is uncritical. This is also true for the CPU and other system clocks in motherboard applications, as long as maximum clock rates are not taken too literally. There are, however, motherboard applications that must have greater accuracy. Floppy disk drive control chips typically require a 24 MHz reference clock that is accurate to 0.1% (1,000 ppm). Modem and SCSI chips typically specify 0.002-0.005% (20-50 ppm) accuracy. Clocks used on the motherboard for time keeping purposes will create a 1 minute-per-month inaccuracy for every 0.0023% (23 ppm) deviation from ideal frequency. Musical instrument synthesis demands highly accurate clocks since even a small error can produce audible beating with another instrument.

With improved clock frequency accuracy comes increased component cost and design complexity. System clock accuracy requirements should, therefore, be approached realistically.

Clock Synthesizer Multiplication Ratio Granularity

ICS frequency generator ICs use the common PLL (Phase-Locked-Loop) technique for clock generation. Figure 1 shows a simplified block diagram of a PLL based clock generator which is applicable to all ICS clock generators. This approach to clock generation uses an input reference frequency that is multiplied by an integer ratio to obtain the desired output frequency. Once the PLL is "in lock" (typically, several milli-seconds after power-up), the output frequency of the chip is related to the reference frequency *exactly* by this programmed multiplication ratio.

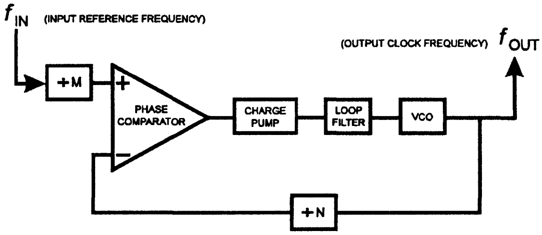


Figure 1: Simplified Diagram of PLL-Based Clock Generator Circuit

Referring to the PLL circuit in Figure 1.

$$f_{OUT} = f_{IN}\frac{N}{M}.$$

Thus, a desired output frequency (the target frequency) may not be hit exactly with a given reference frequency. The size of the minimum frequency steps will be determined by the devices *N* and *M* range. As an example, in the AV9107, *N* can be assigned integer values from 2 to 128 and *M* from 2 to 32. Using a 14.31818 MHz reference, if an output frequency of 50 MHz is desired, the closest output frequencies achievable are 49.88 MHz (N/M = 108/31) or 50.11 MHz (N/M = 7/2). In general, the AV9107 will have an approximate frequency error of 0.25% due to the programming granularity.

Some of the ICS clock synthesizer data sheets list both *target* and *actual* frequencies of the device. The *target frequency* is the typical value required for the intended application. For example, for processor clock devices, target frequencies are typically round numbers such as 20, 25, 33.3 or 50 MHz relating to the rated CPU speed. However, because the typical processor clock IC uses a 14.31818 MHz reference frequency, these exact target frequencies cannot be obtained within practical limits of *N* and *M* values. (The reference frequency of 14.31818 MHz is chosen because it is a common system clock frequency and quartz crystals at this frequency are readily available.) Furthermore, there is no reason for a processor clock to be extremely accurate (although it should be stable with little jitter and maintain a good duty cycle).

The *actual frequency* listed in the data sheet represents the output frequency of the device as determined by multiplying the *ideal* reference frequency of the device (exactly 14.31818 MHz) by the preprogrammed PLL ratio. Again, the PLL ratio is programmed to obtain an *actual frequency* as close to the *target frequency* as possible, within the limitation of the device's *N* and *M* integer ranges.

INPUT REFERENCE CLOCKS

Again by nature of the PLL technique, there will be a direct correlation between the accuracy of the input reference frequency and that of the output frequency. A +0.1 % error in the reference frequency will result in a +0.1 % error in the output frequency (deviation from *actual frequency* where applicable).

When choosing a reference frequency generator, precision is associated with cost. The most accurate and costly reference is a crystal oscillator module. The more common and less expensive approach is to use a discrete external quartz device (most ICS clock chips have built in crystal oscillator circuitry).

Any stable and continuous clock signal (within the specified frequency range) can be used as a reference clock for ICS clock chips. Special circuit considerations are advised when a clock signal, such a system clock or crystal oscillator module output, is used to drive an ICS clock generator that contains an integrated crystal oscillator circuit. Please refer to the device data sheet or contact ICS Applications Engineering.

Use of the Crystal Oscillator Module

A crystal oscillator module is a hybrid device that contains a quartz crystal, an oscillator circuit and an output buffer for the clock output. Since the internal circuit is trimmed during manufacturing, very good frequency accuracy and stability are achieved. These devices commonly yield accuracy's of +\- 20 ppm and exhibit excellent stability over time, temperature, and power supply voltage. The device requires a power supply and typically outputs a CMOS TTL-compatible output clock signal.

Use of the Discrete Quartz Crystal Device

Most ICS frequency generators contain an integral crystal oscillator circuit. With such devices, an external quartz crystal is connected between two specified device pins. This forms a complete parallel-resonant crystal oscillator circuit (also known as a Pierce oscillator). In most cases the only external component required is the quartz crystal, since the required load capacitors and feedback resistor are integrated onto the chip as well. The complete oscillator circuit is shown in Figure 2. With careful design, accuracy to within +/- 100 ppm can be achieved.

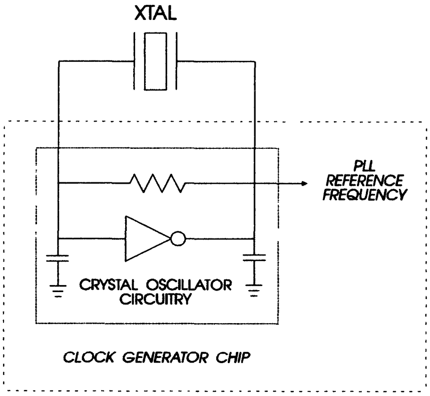


Figure 2
ICS Clock Generator
Crystal Oscillator Circuit

Quartz crystal devices can be specified by the crystal manufacturer for either series or parallel resonant operation. All ICS clock generator devices use parallel resonant operation, sometime referred to as "parallel mode". Parallel resonant crystals specify a load capacitance value which must be observed to ensure an accurate oscillation frequency.

Table 1 lists the load capacitance applied to the external crystal by various ICS clock generators. This is the total measured load capacitance which accounts for stray capacitance in the device package and printed circuit traces (short lead length used).

The load capacitance on the crystal can be increased by applying external load capacitors as shown in Figure 3. This is useful when the crystal's specified load capacitance is above that provided the provided by the clock generator. This is also used when no internal load capacitors are provided (refer to device data sheet).

ICS DEVICE	LOAD CAPACITANCE TO CRYSTAL
AV9107	12 pf
AV9110	12 pf
AV9128	12 pf
AV9129	12 pf
AV9154	12 pf
AV9155	12 pf
ICS1494	15 pf
ICS1562	11 pf
ICS1567	15 pf
ICS1694	15 pf
ICS2407	15 pf
ICS2409	15 pf
ICS2439	15 pf
ICS2494	15 pf
ICS2595	15 pf
ICS2655	15 pf
ICS5300	12 pf
ICS9132	7.5 pf

Table 1
ICS Clock Generator
Capacitive Load to Crystal

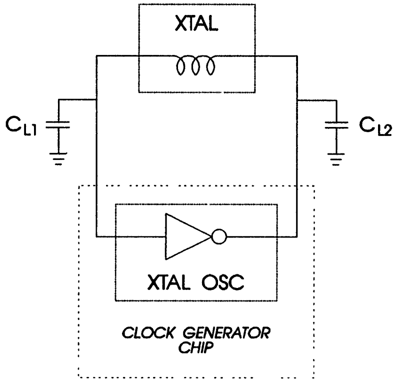


Figure 3
Connection of External Load Capacitors to Clock Generator Chip

The load presented to the crystal in Figure 3 is

$$C_L = \frac{C_{L1} \cdot C_{L2}}{C_{L1} + C_{L2}}.$$

C_{L1} and C_{L2} should be equivalent values.

Calculating Crystal Oscillation Frequency Accuracy

When a quartz crystal is operated in a series resonant oscillator, the crystal oscillates at it's series resonant frequency determined by L_M and C_M (the crystal's motional inductance and capacitance) as shown in Figure 4.

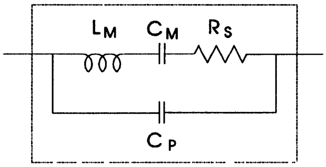


Figure 4
Electrical Model of Quartz Crystal

In a parallel resonant crystal oscillator circuit, such as used in ICS clock synthesizer devices, an LC tank circuit is created as illustrated in Figure 5. C_{EFF} is the lump capacitance consisting of C_M, C_P, and external C_L:

$$C_{EFF} = \frac{(C_L + C_P) \bullet C_M}{(C_L + C_P) + C_M}$$

The resonant frequency can then be calculated as:

$$f_{RESONANCE} = \frac{1}{2p\sqrt{L_M C_{EFF}}}.$$

The resistance R_S in the crystal has no effect on resonance frequency. However, the active circuitry of the oscillator, represented by the inverter in Figure 5, must have enough "negative resistance" to overcome the loss imposed by R_S. This allows the LS tank voltage amplitude to increase and maintain a full oscillation voltage swing. Most crystal manufactures recommend a negative resistance magnitude of at least five times the R_S (or ESR) value to ensure oscillator start up; ICS crystal oscillator circuits have a negative resistance magnitude above 250 ohms.

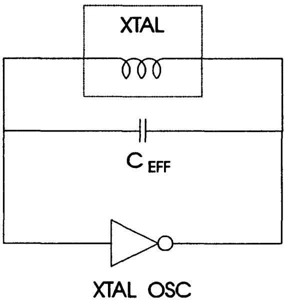


Figure 5
Electrical Model of Parallel Resonant Quartz Crystal Oscillator Circuit

The parallel resonant frequency of the crystal oscillator is higher than the series resonant frequency of the crystal. The fractional frequency "pulling" or the fractional amount that the parallel resonant frequency will be above the series resonate frequency can be calculated as

$$P = \frac{C_M}{2 \cdot C_L}.$$

If we know f_S, the series resonant frequency of the crystal, we can then calculate f_P, the parallel resonant frequency as

$$f_P = (1 + P) f_S.$$

Let's take the example of a series 14.31818 MHz crystal used with the AV9155. A typical value of C_M is 20×10^{-15} farad (the crystal manufacturer can give you this information). From Table 1, we find that C_L presented by the AV9155 is 12 pf. In this case, P is calculated to be 0.0008333 and f_P is calculated to be 14.33011 MHz which is 833 ppm (parts per million) above the series resonant frequency.

We can also use the above equations to determine oscillation error caused by total C_L error. In the example of using the AV9155 where typical circuit C_L is 12 pf, if we assume that total C_L variation can be +/- 3 pf, then oscillation frequency error will be from -166.7 ppm to +277.8 ppm. Even if assuming that external circuit capacitance can be controlled, just considering the variation of the AV9155's internal load capacitors, which vary -/- 10% or +/- 1 pf, would account for a oscillation frequency error of -166 ppm to +75 ppm. Remember that oscillator error due to C_L deviation is in addition to other errors such as the rated crystal frequency tolerance and the effects of crystal temperature and aging (consult the crystal's data sheet).

Crystal Power Dissipation

Crystal manufactures typically specify a suggested crystal power dissipation range. This is the range within which the crystal's temperature will not rise to the point of causing excessive oscillation frequency drift. Maximum crystal power dissipation is also typically listed. Well above the suggested dissipation range, this is the limit above which crystal damage can occur (it will stop working), over a period of time.

Most through-hole mount crystals specify a suggested power dissipation of about 1 mW, well suited for ICS clock generators. This is also true for the standard larger-sized surface mount crystals.

Problems can arise with some smaller types of surface mount crystals. A typical 14.318 MHz surface mount crystal used with an ICS clock generator will dissipate about 200 to 500 micro watts, depending on which clock generator is used. Maximum crystal power ratings of only 100 micro watts or lower are not uncommon, however most crystal manufactures will admit that this figure can be exceeded by 5-10 times. For maximum power dissipation it is best to consult directly with the crystal manufacturer.

Calculating Crystal Power Dissipation

Power dissipation within the quartz crystal is caused by oscillation current flowing through the crystal's effective series resistance, shown as R_S in Figure 4. This is commonly listed as 'ESR' (Effective Series Resistance) in the crystal data sheet. Power dissipation can be calculated as

$$P_D = I_{LC}{}^2 R_S,$$

where I_{LC} is the oscillation current in the LC tank circuit shown in Figure 5. It is difficult to measure I_{LC} during oscillation, therefore we measure differential voltage across the crystal and make the following substitution:

$$P_{DISS} = \left(\frac{V_{XTAL}}{|Z_{XTAL}|} \right)^2 R_S$$

Where V_{XTAL} is the RMS voltage across the crystal. Z_{XTAL} consists of both the reactance of the inductor shown in Figure 5 and resistance R_S not shown. However, at oscillation the inductive reactive is much larger than R_S and so the contribution of R_S to Z_{XTAL} can be ignored. Therefore we can make the approximation that

Substituting in the earlier equation we get

$$P_D \cong \left(\frac{V_{XTAL}}{\omega L_M} \right)^2 R_S.$$

By definition of a resonant circuit, the reactance's of the crystal's inductance and the external load capacitance are equal. This can be stated as

Again through substitution we now get

$$P_D \cong (V_{XTAL} \bullet \omega C_L)^2 R_S$$

or

$$P_D \cong \left(\frac{\sqrt{2}}{2} V_{PK} \bullet 2\pi f C_L \right)^2 R_S,$$

where f is the frequency of oscillation and V_{PK} is the peak voltage across the crystal. Our final simplified equation is now

$$P_D \cong (1.414 \bullet V_{PK} \bullet \pi f C_L)^2 R_S.$$

Using the final equation it is easy to calculate approximate power dissipation with readily obtainable values. V_{PK} can be measured with a high speed differential oscilloscope (low capacitance probes must be used), or the curves of Figures 6 or 7 can be used for the following list of devices: AV9107, AV9110, AV9128, AV9129, AV9154, AV9155.

As an example, lets say that we are operating an AV9155 with a VDD of 5 volts using a 14.318 MHz crystal with an R_S (or ESR) rating of 35 ohms. From Table 1 we find that C_L = 12 pf and from Figure 6 we find that V_{PK} = 2.5 volts. Substituting values in the final equation above we determine that crystal power dissipation is approximately 127 micro-watts.

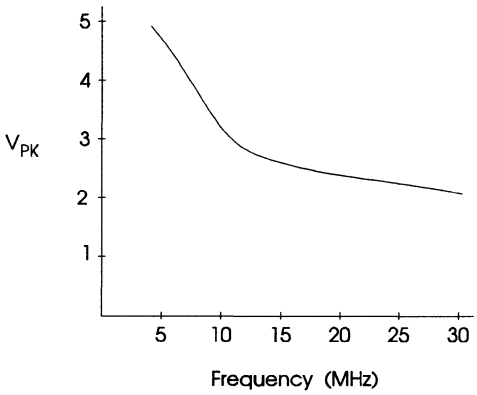


Figure 6
Peak Voltage Across Crystal
With VDD = 5.0 Volts

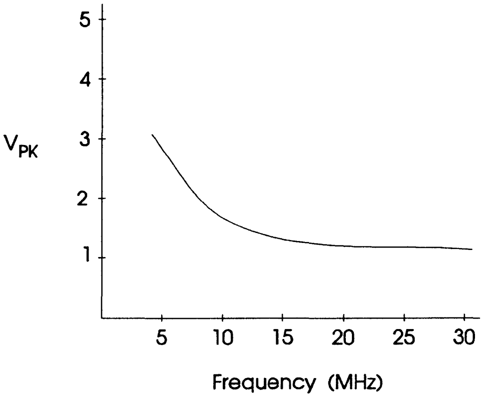


Figure 7
Peak Voltage Across Crystal
With VDD = 3.0 Volts

Clock Reference Guidelines for ICS Clock Generators

Most ICS Clock Generator ICs are designed to use an external quartz crystal to establish the needed reference frequency. This application note discusses crystal selection and use. Occasionally, it is desirable to instead use an external clock reference; design considerations for this approach are also discussed.

ICS Crystal Oscillator Circuitry

Figure 1 shows a schematic of the ICS crystal oscillator circuitry. Combined with the external crystal, this implements a Pierce oscillator circuit. Figure 2 shows the oscillator inverter circuit in further detail. This inverter is unlike the CMOS inverter commonly used by other clock generator devices. The advantage of the ICS inverter is that it provides higher circuit gain, which guarantees crystal start-up and provides a wider frequency range. It also provides a TTL level input threshold voltage at pin X1 (approximately 1.4 volts), which provides compatibility with an external TTL reference clock. Typically duty cycle of REFOUT is 43% (High)/57% (Low) when a 14.318 MHz crystal is used.

Guidelines for Crystal Selection

The ICS crystal oscillator circuitry operates the crystal in parallel-resonant mode. Although most oscillator circuits are designed to use parallel-resonant crystals, the least expensive crystals are series-resonant devices. Using a series-resonant crystal with an ICS clock generator will give excellent results but will usually result in reference frequency that is about 0.1% too fast. Normally, this error is not significant for most CPU or graphics applications.

If a higher clock accuracy is required, then a parallel-resonant crystal must be used; a load capacitance value of 10-20pf should be specified when ordering the crystal.

To further improve clock frequency accuracy, an external capacitor can be connected between pin X1 and ground. The capacitance value is typically between 10 and 20pf. The actual value will vary depending on the crystal manufacturer and is found experimentally, using the crystal type intended for volume production.

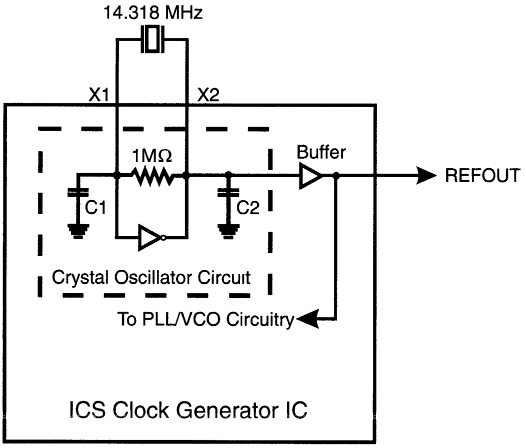


Figure 1
Simplified Schematic of
ICS Crystal Oscillator Circuitry

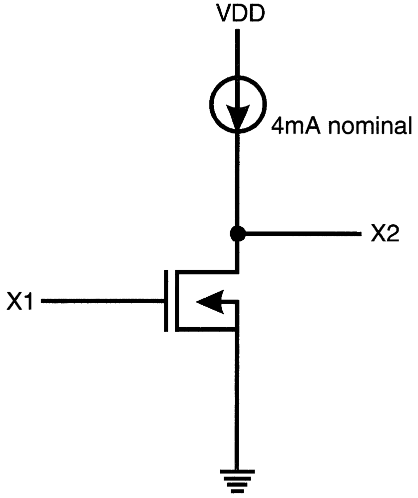


Figure 2
ICS Crystal Oscillator Inverter Schematic

Guidelines for Using an External Reference Clock

The recommended method of driving an ICS clock generator with an external clock is shown in Figure 3, along with the resulting waveforms. The positive-going ramp of the X2 output is caused by the charging of capacitor C2 by the current source when the N-channel FET is off (refer to Figure 2). V_{TH}, the input threshold of the REFOUT buffer, is approximately 1.4 volts. External resistor R1 aids the inverter's current source in charging C2 and accordingly improves the duty cycle of REFOUT.

The use of an appropriate R1 value will result in a near 50% duty cycle from REFOUT. This also ensures reliable operation of the VCO/PLL circuitry and further maintains good clock jitter performance, which can be degraded by poor duty cycle.

The guidelines for R1 value selection are as follows:

1. If reference clock duty cycle is greater than 50% (high time), R1 should be between 1 and 2 kohm. Actual value should be determined experimentally; the value should be adjusted for nominal duty cycle of 50% from REFOUT. An R1 value of 1 kohm should cover most instances.
2. If reference clock duty cycle is less than 50% (high time), R1 may still be used but is not required. For example, REFOUT from one ICS clock generator (duty cycle 43%) can drive X1 of a second ICS clock generator without the use of R1.

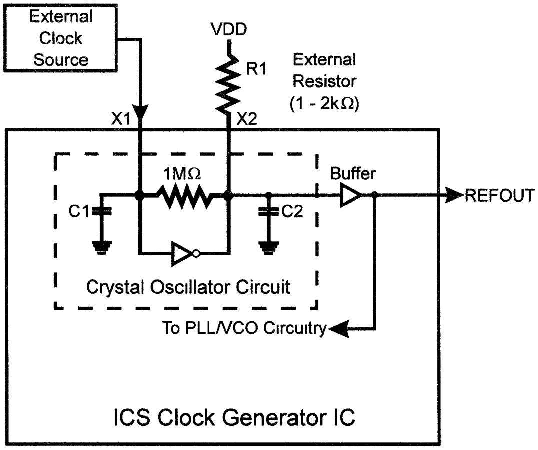


Figure 3
Driving an ICS Clock Generator with an External Clock

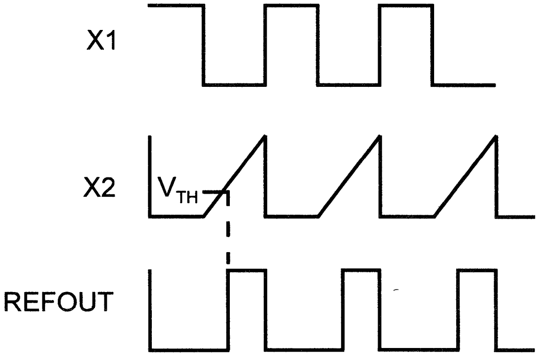


Figure 4
Waveforms of Figure 3

ICS
Motherboard Timing Generator Products

In this latest issue of the ICS Data Book, ICS continues to lead the market by offering the industry's widest selection of advanced motherboard and CPU clock generators found anywhere. New products include designs to address a wide variety of uses, including disk drive, modem, advanced Pentium and PowerPC clocking applications. This is all in addition to the widest choice of advanced desktop and laptop motherboard and CPU systems clock generators in the industry.

As a market-oriented company, ICS designs products with and for you, our customers, and we welcome inquiries concerning new product ideas for any of the above applications.

ICS Timing Generator Selection Guide

Motherboard Clock Products

Product Application	ICS Device Type	Description	Number of Outputs	Number of PLL's	Package Types	Page
Motherboard	ICS2407 ICS2409 ICS2419 ICS2439	IMI407, IMI409 and IMI439 Compatible.	6 9 10 9	2 2 2 2	18-Pin DIP, SOIC 24-Pin DIP, SSOP 24-Pin DIP, SSOP 24-Pin DIP, SSOP	C-3
	ICS2492	Buffered XTAL Out. Tristate PLL Outputs.	3	2	20-Pin DIP, SOIC	C-11
	ICS2494-244 ICS2494A-317	Buffered XTAL Out. *Note*: See Video Dot Clock Section for Data.	3	2	20-Pin DIP, SOIC	B-11
	ICS2694	9 Fixed, CPU-CPU/2 Selectable Provides CPU, Co-Processor, Hard and Floppy Disk, Kbd, Ser. Port, Bus Clk. Function.	11	2	24-Pin DIP, SOIC	C-17
	AV9107C	CPU Clock Generator.	2	1	8 or 14-Pin DIP, SOIC	C-23
	ICS9108	3 Volt CPU Clock Generator.	2	1	8 or 14-Pin DIP, SOIC	C-29
Audio Synthesis	ICS9120-08 ICS9120-09	3 Volt Multimedia Audio Synthesizer Clock Generator.	4	1	8-Pin SOIC	C-35
Notebook	ICS9131	32 kHz Input Generates CPU Clocks.	3	2	16-Pin DIP, PDIP	C-41
	ICS9133X	32 kHz Input Generates CPU Clock and System Clock and Two Fixed Clocks.	6	3	20-Pin SOIC, PDIP	C-49
Sub-Notebook	ICS9134-06 ICS9134-07	32 kHz Motherboard Frequency Generator. Generated CPU, Reference and One Fixed Clock.	6	3	16-Pin SOIC	C-55
Pentium and Green PC Systems	AV9154A	Low Cost 16-Pin Clock Generator. Generates CPU Clock, Keyboard Clock, System Clock and I/O Clock.	7	2	16-Pin DIP, SOIC	C-61
Laptop/ Notebook	AV9154-06 AV9154A-60	Clock Generator for OPTi Chip Set.	5	2	16-Pin SOIC	C-71
Motherboard	AV9155A	Motherboard Clock Generator. Produces CPU Clock, Keyboard Clock, System Clock and I/O Clock.	8	2	20-Pin DIP, SOIC	C-77
Desktop/Notebook	ICS9158	Clock Generator with Integrated Buffers.	11	2	24-Pin SOIC	C-89
Pentium Systems	ICS9159-02	Clock Generator for Pentium Systems.	14	2	28-Pin SOIC	C-95
PowerPC Systems	ICS9160-03	Clock Generator for PowerPC 603 Systems.	15	2	32-Pin SOIC	C-99
	ICS9178-02	Clock Generator for PowerPC 601/601+ Systems.	14	1	44-Pin PQFP	C-103

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. ICS reserves the right to change or discontinue these products without notice.

Integrated Circuit Systems, Inc.

ICS2407
ICS2409
ICS2419
ICS2439

Dual-PLL Motherboard Frequency Generator

Description

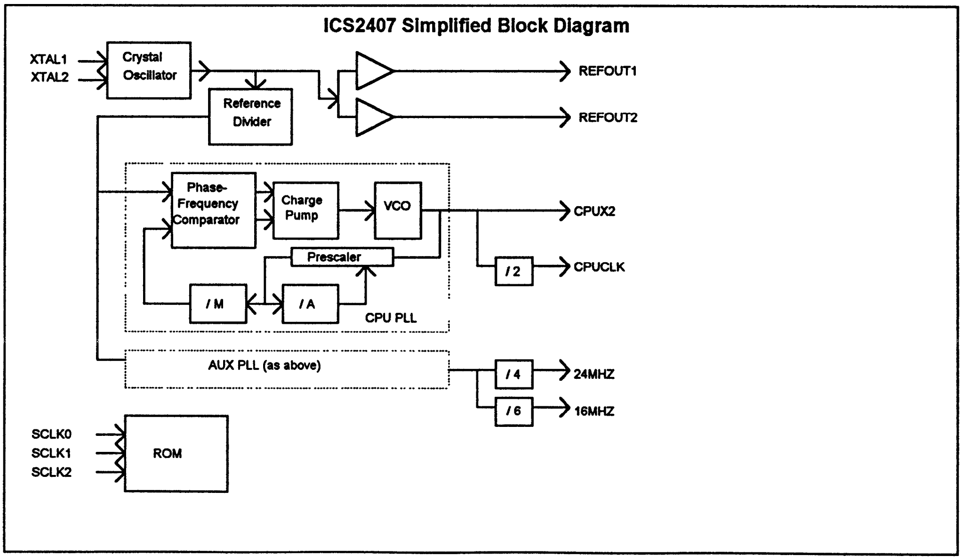
This ICS family of motherboard frequency generators all stem from the same basic design. They are dual-PLL (phase-locked loop) clock generators specifically designed for motherboard applications. Metal layer and assembly options are used to generate the three separate device types in order to optimize the functionality for specific applications. All frequencies are synthesized from a single reference clock which may be generated by the on-chip crystal oscillator or an external reference clock.

The CPU clock PLL is ROM-programmed to generate any of seven customer specified frequencies through selection of the address lines **SCLK0-SCLK2**. *In the ICS2409, ICS2419 and ICS2439 versions the SCLK3 input selects those frequencies directly or divided by two for the CPUX2 output.* The **CPUX2** output is then divided by two to generate the **CPUCLK** output. A power-down mode may be selected with the **SCLK** inputs to reduce standby current consumption to a few microamperes.

The auxiliary (AUX) PLL generates the fixed frequencies shown in Table 1 for other system uses. A buffered reference frequency output is available on the **REFOUT** pin. Two non-dedicated buffers are provided on the **ICS2409, ICS2419** and **ICS2439** for additional drive capability without adding external buffers and their board space.

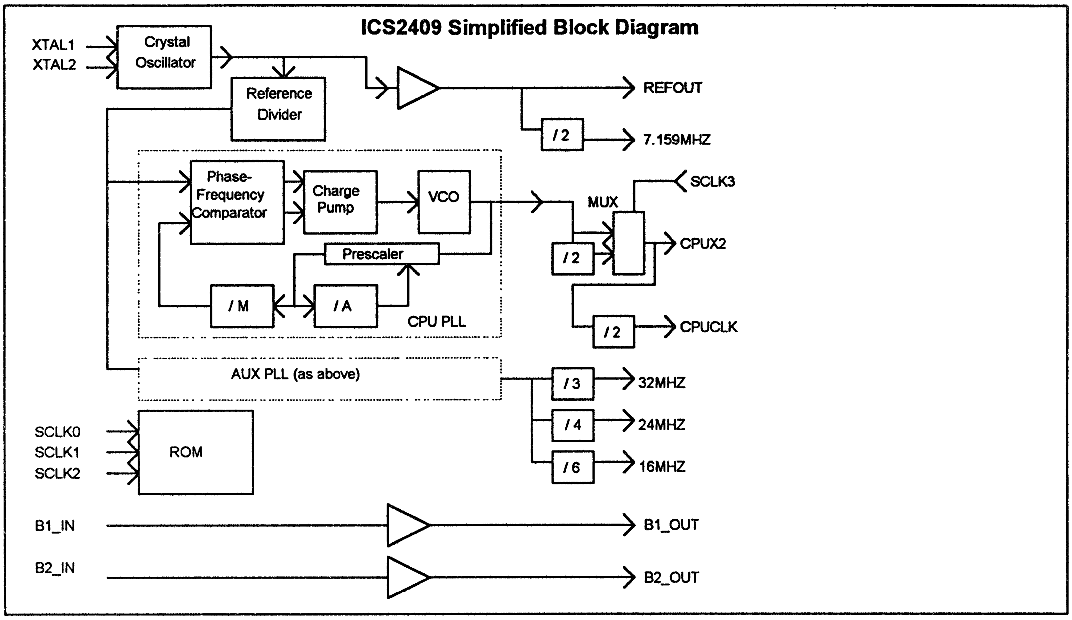
Features

- Supports 286, 386, & 486 desktop and notebook motherboard designs
- Advanced ICS monolithic phase-locked loop technology for low short-term and "cumulative" jitter
- Completely integrated - no external loop filter capacitors required
- Dual-modulus prescaler permits high-speed operation with no sacrifice in accuracy
- Power-down mode for low standby power consumption
- Low-skew between **CPUX2** and **CPUCLK** outputs (<1 nsec)
- 3-volt supply capability to 85 MHz (**CPUX2** output)
- Output enable (**OE**‾) pin for tristate of device outputs
- **ICS2409, ICS2419** and **ICS2439** offer 24-pin PDIP (0.3") and 24-pin SSOP (5.3mm) package options
- **ICS2407** offers 18-pin PDIP (0.3") and 18-pin SOIC (0.3") package options

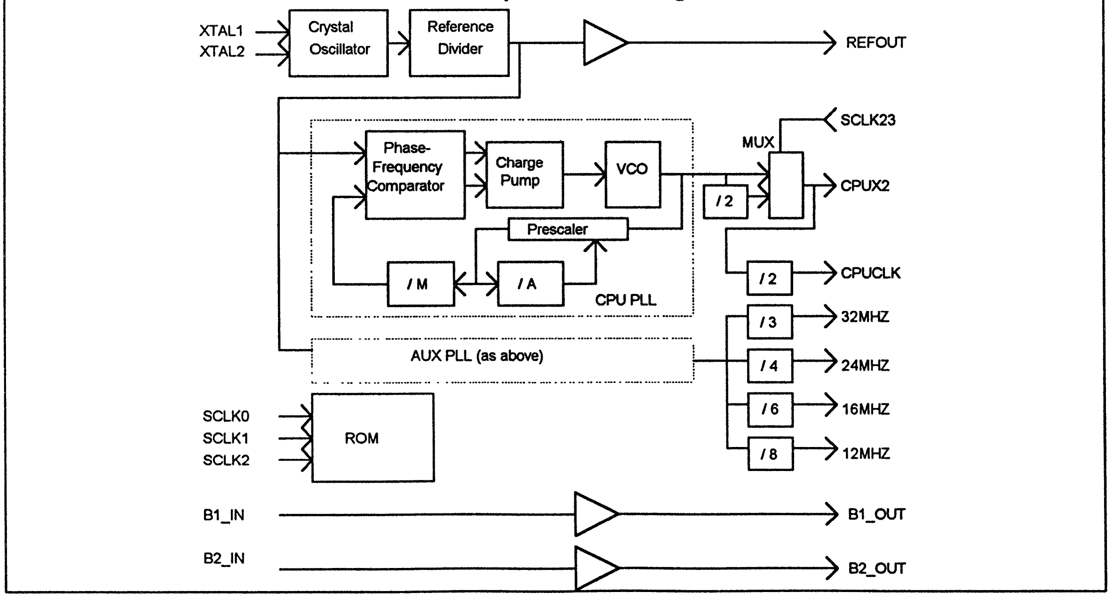


ICS2407 Simplified Block Diagram

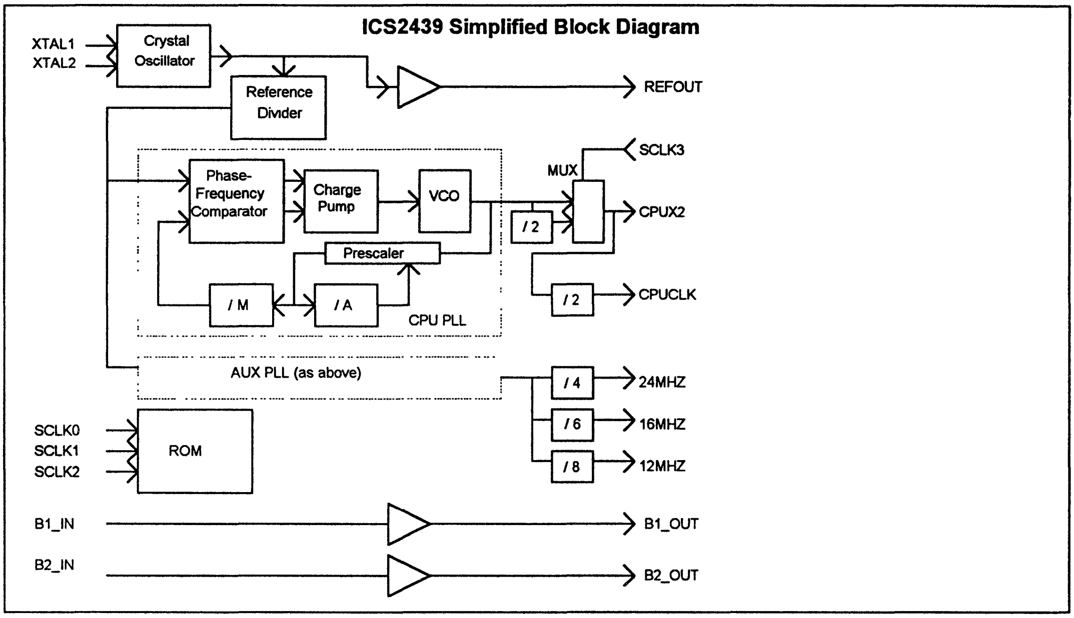
ICS2409 Simplified Block Diagram



ICS2419 Simplified Block Diagram



ICS2439 Simplified Block Diagram



Circuit Function and Application

Fixed Frequencies

The ICS motherboard family supplies "fixed" frequencies normally used to provide several system functions:

- 32 MHz - ISA Bus Clock
- 24 MHz - Floppy Drives
- 16 MHz - AT Bus Clock Output
- 12 MHz - Keyboard Clock
- 7.149 MHz - Keyboard Clock

Selectable CPU Clock Frequencies

The **ICS2407**, **ICS2409**, **ICS2419** and **ICS2439** are designed to generate CPU clock options ranging from 24 MHz, to 88 MHz. For added flexibility, the **ICS2409, ICS2419** and **ICS2439** allow the user to select each of these frequencies divided by 2.

Buffered Output Pins

In addition, the **ICS2409, ICS2419** and **ICS2439** provide 2 non-dedicated buffers for additional flexibility. This allows for extra drive capability without sacrificing the extra board space required for external buffers.

Buffered XTALOUT

In motherboard applications it may be desirable to have the **ICS2439** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator on the system, saving money as well as board space. Depending on the load, it may be judicious to buffer REFOUT when using it to provide the system clock. On the **ICS2407**, there are two identical outputs, REFOUT1 and REFOUT2.

Power-Down Mode

All three devices have been optimized for use in battery operated portables. It can be placed in a power-down mode which drops its supply current requirement below 1µA(typical).

Pin Description

Input Pins

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate crystal should be connected between XTAL1 (1) and XTAL2 (2). In IBM compatible applications this will typically be a 14.31818 MHz crystal.

Digital Inputs

SCLK0, SCLK1, SCLK2 and SCLK3 *(ICS2409, ICS2419 and ICS2439 only)* are the TTL compatible frequency select inputs for the binary code corresponding to the desired frequency. All select pins have internal pull-up devices built in *(See Table 2 for a complete list of available frequencies).*

Buffer Inputs (ICS2409, ICS2419 & ICS2439)

B1_IN and B2_IN (3, 7) provide additional buffering needed on a typical board design without the added cost of external components.

Output Enable

An output enable pin OE~allows the user to tristate the device outputs. When this pin is high, all outputs are in tristate mode. When low, all outputs are enabled. This pin has an internal pull-down to enable all outputs when the pin is N/C.

ICS2407 Pinout

1	XTAL1	REFOUT1	18
2	XTAL2	VDD	17
3	VSS	N/C	16
4	REFOUT2	16MHZ	15
5	SCLK0	24MHZ	14
6	N/C	VSS	13
7	VDD	CPUX2	12
8	SCLK1	SCLK2	11
9	CPUCLK	OE~	10

18-Pin PDIP or SOIC
K-4, K-7

ICS2409 Pinout

1	XTAL1	REFOUT	24
2	XTAL2	B1_OUT	23
3	B1_IN	VDD	22
4	VSS	N/C	21
5	7 159MHZ	16MHZ	20
6	SCLK0	24MHZ	19
7	B2_IN	32MHZ	18
8	N/C	B2_OUT	17
9	VDD	VSS	16
10	SCLK1	CPUX2	15
11	SCLK3	SCLK2	14
12	CPUCLK	OE~	13

24-Pin PDIP or SSOP
K-5, K-9

ICS2439 Pinout

1	XTAL1	REFOUT	24
2	XTAL2	B1_OUT	23
3	B1_IN	VDD	22
4	VSS	N/C	21
5	12MHZ	16MHZ	20
6	SCLK0	24MHZ	19
7	B2_IN	RESERVED	18
8	N/C	B2_OUT	17
9	VDD	VSS	16
10	SCLK1	CPUX2	15
11	SCLK3	SCLK2	14
12	CPUCLK	OE~	13

24-Pin PDIP or SSOP
K-5, K-9

ICS2419 Pinout

1	XTAL1	REFOUT	24
2	XTAL2	B1_OUT	23
3	B1_IN	VDD	22
4	VSS	N/C	21
5	12MHZ	16MHZ	20
6	SCLK0	24MHZ	19
7	B2_IN	32MHZ	18
8	N/C	B2_OUT	17
9	VDD	VSS	16
10	SCLK1	CPUX2	15
11	SCLK3	SCLK2	14
12	CPUCLK	OE~	13

24-Pin PDIP or SSOP
K-5, K-9

Absolute Maximum Ratings

Supply Voltage	V_{DD}	-0.5V to +7V
Input Voltage	V_{IN}	-0.5V to V_{DD} + 0.5V
Output Voltage	V_{OUT}	-0.5V to V_{DD} + 0.5V
Clamp Diode Current	V_{IK} & I_{OK}	±30mA
Output Current per Pin	I_{OUT}	±50mA
Operating Temperature	T_O	0°C to 70°
Storage temperature	T_S	-85°C to 150°
Power Dissipation	P_D	500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than themaximum rated voltages. For proper operation it is recommended that Vin and Vout be constrained to >=V_{SS} and <=V_{DD}.

DC Characteristics at 5 Volts V_{DD}

(0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Operating Voltage Range	V_{DD}		4.5	5.5	V
Input Low Voltage	V_{IL}	V_{DD}=5V	V_{SS}	0.8	V
Input High Voltage	V_{IH}	V_{DD}=5V	2.0	V_{DD}	V
Input Leakage Current	I_{IH}	V_{IN}=V_{DD}	-	10	µA
Output Low Voltage	V_{OL}	I_{OL}=1.20mA	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=1.20mA	2.4	0	V
Supply Current	I_{DD}	VCLK=40MHz	-	40	mA
Supply Current	I_{DD}	VCLK=88MHz	-	50	mA
Internal Pull-up Current	R_{UP}	V_{IN}=0.0V	30	100	µA
Internal Pull-down Current	R_{DOWN}	V_{IN}=0.0V	30	100	µA
Input Pin Capacitance	C_{IN}	F_C=1MHz	-	8	pF
Output Pin Capacitance	C_{OUT}	F_C=1MHz	-	12	pF
Power-down Supply Currrent	I_{PN}	V_{DD}=3.3V	-	1	µA

DC Characteristics at 3.3 Volts V_{DD}

(0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Operating Voltage Range	V_{DD}		3.0	3.6	V
Input Low Voltage	V_{IL}	V_{DD}=3.3V	V_{SS}	0.8	V
Input High Voltage	V_{IH}	V_{DD}=3.3V	2.0	V_{DD}	V
Input Leakage Current	I_{IH}	V_{IN}=V_{DD}	-	10	µA
Output Low Voltage	V_{OL}	I_{OL}=8.0mA	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=8.0mA	2.4	0	V
Supply Current	I_{DD}	CPUX2=40MHz	-	35	mA
Supply Current	I_{DD}	CPUX2=88MHz	-	25	mA
Internal Pull-up Current	R_{UP}	V_{IN}=0.0V	20	70	µA
Internal Pull-down Current	R_{DOWN}	V_{IN}=0.0V	20	70	µA
Input Pin Capacitance	C_{IN}	F_C=1MHz	-	8	pF
Output Pin Capacitance	C_{OUT}	F_C=1MHz	-	12	pF
Power-down Supply Currrent	I_{PN}	V_{DD}=3.3V	-	1	µA

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section.
1. REFCLK = 14.31818 MHz
2. $t_c = 1/f_c$
3. All units are in nanoseconds (ns)
4. Rise and fall time between .8 and 2.0 VDX unless otherwise stated.
5. Output pin loading = 15pF
6. Duty cycle measured at $V_{DD}/2$ unless otherwise stated.

SYMBOL	PARAMETER	MIN	MAX	NOTES
OUTPUT TIMING @5v				
Tr	Rise Time	-	2	
Tf	Fall Time	-	2	
-	Frequency Error	-	0.5	%
Tak	Clock Skew (CPUCLK & CPUX2)	-	1.0	nSec
-	Duty Cycle	45	55	%
-	Output Enable to Tristate (into and out of) time	-	15	nSec
OUTPUT TIMING @3.3v				
Tr	Rise Time	-	3	
Tf	Fall Time	-	3	
-	Frequency Error	-	0.5	%
Tak	Clock Skew (CPUCLK & CPUX2)	-	1.5	nSec
-	Duty Cycle	45	55	%
-	Output Enable to Tristate (into and out of) time	-	20	nSec

Table 1: Fixed Output Frequencies

ICS2439	ICS2419	ICS2409	ICS2407
24 MHz	32 MHz	32 MHz	24 MHz
16 MHz	24 MHz	24 MHz	16 MHz
12 MHz	16 MHz	16 MHz	
	12 MHz	7.159 MHz	

Table 2: CPU Clock Frequency Selection

SCLK3	SCLK2	SCLK1	SCLK0	ICS2439 Pattern 001	ICS2419 Pattern 001	ICS2409 Pattern 409	ICS2407 Pattern 407
0	0	0	0	12 MHz	12 MHz	12 MHz	12 MHz
0	0	0	1	16	16	16	16
0	0	1	0	20	20	20	20
0	0	1	1	25	25	25	25
0	1	0	0	33.33	33.33	33.33	33.33
0	1	0	1	40	40	40	40
0	1	1	0	30	30	44	44
0	1	1	1	Power-down	Power-down	Power-down	Power-down
1	0	0	0	24	24	24	
1	0	0	1	32	32	32	
1	0	1	0	40	40	40	
1	0	1	1	50	50	50	
1	1	0	0	66.66	66.66	66.66	
1	1	0	1	80	80	80	
1	1	1	0	60	60	88	
1	1	1	1	TEST	TEST	TEST	

Ordering Information

ICS2407-XXXN, ICS2407-XXXM; ICS2409-XXXN, ICS2409-XXXF
ICS2419-XXXN, ICS2419-XXXF; ICS2439-XXXN, ICS2439-XXXF

Example:

ICS XXXX-XXX M

Package Type
N=DIP (Plastic) F=SSOP
M=SOIC (SOP)
Pattern Number (2 or 3 digit number for parts with ROM code patterns)
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

CPU Clock Generator

Description

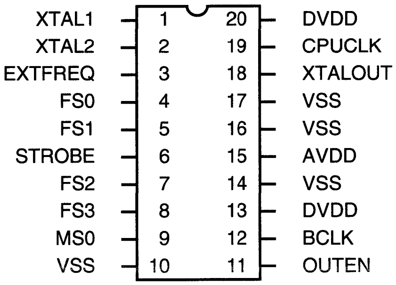
The **ICS2492** CPU Clock Generator is an integrated circuit dual phase locked loop frequency synthesizer capable of generating 16 CPU frequencies and two other clock frequencies for use with high performance personal computer motherboards. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS2492** provides a low-power, small footprint, low-cost solution to the generation of CPU clocks. Provision is made via a single level custom mask to implement customer-specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

The **ICS2492** is fully pin and function compatible with ICS's industry-standard ICS2494 dual clock generator except that an output enable function has been added to pin 11. A pre-programmed version with a full selection of CPU clocks is available as part number **ICS2492-453**. The frequencies in this pattern are essentially identical to those in the ICS2494-244 standard pattern.

Features

- Low cost - eliminates need for multiple crystal clock oscillators in motherboard applications
- Mask-programmable frequencies
- Pre-programmed versions for a selection of CPU clocks
- Glitch-free frequency transitions
- Provision for external frequency input
- Internal clock remains locked when the external frequency input is selected
- Low power CMOS device technology
- Small footprint - 20-pin DIP or SOIC
- Buffered XTAL Out
- Integral Loop Filter components
- Fast acquisition of selected frequencies, strobed or non-strobed
- Guaranteed performance up to 135 MHz
- Excellent power supply rejection
- Advanced PLL for low phase-jitter
- Output Enable function for tristate control of the two clock outputs.

Pin Configuration



20-Pin DIP or SOIC
K-4, K-7

Notes:
1. In applications where the external frequency input is not specified, EXTFREQ must be tied to V_{SS}.
2. ICS2492M(SOIC) pinout is identical to ICS2492N(DIP).

Circuit and Application Options

The **ICS2492** will typically derive its frequency reference from a series-resonant crystal connected between pins 1 and 2. Where a high quality reference signal is available, such as in an application where the graphics subsystem is resident on the motherboard, this reference may directly replace the crystal. This signal should be coupled to pin 1. If the reference signal amplitude is less than 3.5 volts, a .047 microfarad capacitor should be used to couple the reference signal into **XTAL1**. Pin 2 must be left open.

The **ICS2492** is capable of multiplexing an externally generated frequency source of **VCLK** via a mask option, in addition to its internally-generated clock.

This is input via **EXTFREQ (3)**. When an external source is selected, the PLL remains locked to the value specified in the selected address. This provision facilitates the ability to rapidly change frequencies. When this option is not specified in the ROM pattern, pin 3 is internally tied to V_{SS} and should be connected to V_{SS} on the PCB.

Power Supply Conditioning

The **ICS2492** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in Figures 1 or 2. Figure 1 is the normal configuration for 5 Volt only applications. Which of the two provides superior performance depends on the noise content of the power supplies. In general, the configuration of Figure 1 is satisfactory. Figure 2 is the more conventional if a 12 Volt analog supply is available, although the improved performance comes at a cost of an extra component; however, the cost of the discretes used in Figure 2 is less than the cost of Figure 1's discrete components.

The number and differentiation of the analog and digital supply pins are intended for maximum performance products. In most applications, all V_{DDs} may be tied together. The function of the multiple pins is to allow the user to realize the maximum performance from the silicon with a minimum degradation due to the package and PCB. At the frequencies of interest, the effects of the inductance of the bond wires and package lead frame are non-trivial. By using the multiple pins, ICS has minimized the effect of packaging and has minimized the interaction of the digital and analog supply currents.

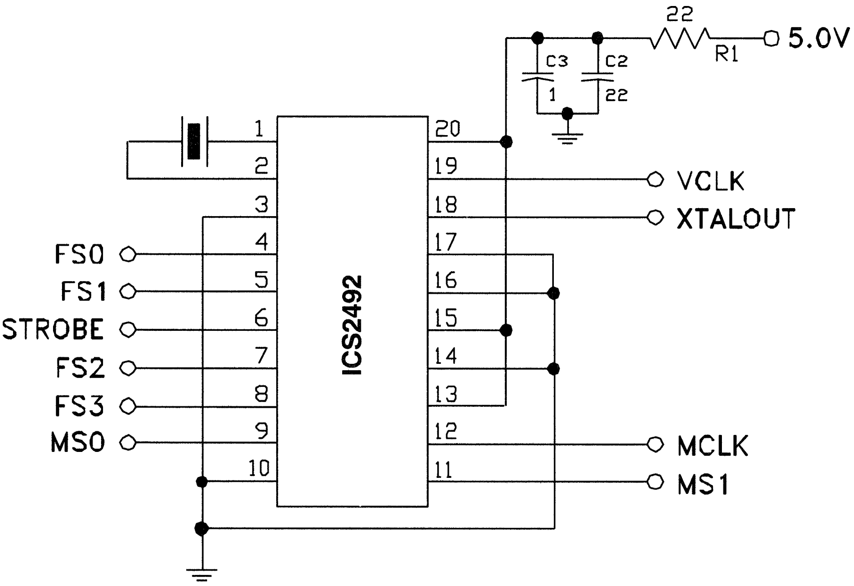


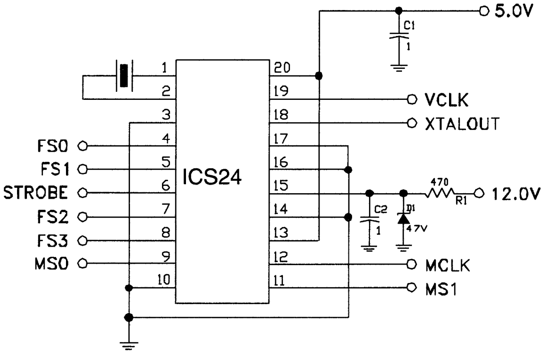
Figure 1

Applications

Layout Considerations

Utilizing the **ICS2492** in video graphics adapter cards or on PS2 motherboards is simple, but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised in ensuring that components not related to the **ICS2492** do not share its ground. In applications utilizing a multi-layer board, V_{SS} should be directly connected to the ground plane. Multiple pins are utilized for all analog and digital Vss and Vdd connections to permit extended frequency **VCLK** operation to 135 MHz. However, in all cases, all V_{SS} and V_{DD} pins should be connected.

Figure 2



Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series-resonant crystal should be connected between **XTAL1 (1)** and **XTAL2 (2)**. In IBM-compatible applications this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10 MHz and 25 MHz have been tested. Maintain short lead lengths between the crystal and the **ICS2492**. In some applications, it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to **XTAL1 (1)**. If the signal amplitude is less than 3.5 volts, connect the clock through a .047 microfarad capacitor to **XTAL1 (1)**, and keep the lead length of the capacitor to **XTAL1 (1)** to a minimum to reduce noise susceptibility. This input is internally biased at $V_{DD}/ 2$. Since TTL compatible clocks typically exhibit a V_{OH} of 3.5V, capacitively coupling the input restores noise immunity.

The **ICS2492** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (2)** must be left open in this configuration.

Buffered XTALOUT

In motherboard applications it may be desirable to have the **ICS2492** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. To do this, the **XTALOUT (18)** output should be buffered with a CMOS driver.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **VCLK (19) or MCLK (12) and other components in the system should be kept as short as possible. The ICS2492** outputs have been designed to minimize overshoot. In addition, it may be helpful to place a ferrite bead in these signal paths to limit the propagation of high order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS2492**. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may reduce phase-jitter as well as EMI.

External Frequency Sources

EXTFREQ (3) on versions so equipped by the programming, is an input to a digital multiplexer. When this input is enabled, signals driving the input will appear at **VCLK (19)** instead of the PLL output. Internally, the PLL will remain in lock at the frequency selected by the ROM code.

Digital Inputs

FS0 (4), FS1 (5), FS2 (7), and **FS3 (8)**, are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (6),** when high, allows new data into the frequency select latches; and when low, prevents address changes per Figure 3. The internal power-on-clear signal will force an initial frequency code corresponding to an all-zeros input state. **MS0 (9)** and **MS1 (11)** are the corresponding memory select inputs and are not strobed.

Absolute Maximum Ratings

Supply Voltage	V_{DD}	-0.5V to +7V
Input Voltage	V_{IN}	-0.5V to V_{DD}+0.5V
Output Voltage	V_{OUT}	-0.5V to VDD+0.5V
Clamp Diode Current	V_{IK} & I_{OK}	+/ -30mA
Output Current per Pin	I_{OUT}	+/ -50mA
Operating Temperature	T_o	0°C to 70°C
Storage Temperature	T_S	-85 °C to +150°C
Power Dissipation	P_D	500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to >= V_{SS} and <=V_{DD}.

DC Characteristics (0°C to 70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Operating Voltage Range	V_{DD}		4.0	5.5	V
Input Low Voltage	V_{IL}	V_{DD} = 5V	V_{SS}	0.8	V
Input High Voltage	V_{IH}	V_{DD} = 5V	2.0	V_{DD}	V
Input Leakage Current	I_{IH}	$V_{IN} = V_{cc}$	-	10	*u*A
Output Low Voltage	V_{OL}	I_{OL} = 4.0 mA	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = 4.0 mA	2.4	-	V
Supply Current	I_{DD}	V_{DD} = 5V, VCLK = 80 MHz	-	27	mA
Internal Pull-up Resistors	R_{UP} *	V_{dd} = 5V, V_{in} = 0V	50	200	k ohm
Input Pin Capacitance	C_{in}	F_c = 1 MHz	-	8	pf
Output Pin Capacitance	C_{out}	F_c = 1 MHz	-	12	pf

* The following inputs have pull-ups: FS0-3, MS0-1, STROBE.

AC Timing Characteristics

The following notes apply to all parameters presented in this section:

1. Xtal Frequency = 14.31818 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns).
4. Rise and fall time is between 0.8 and 2.0 VDC.
5. Output pin loading = 25pF
6. Duty cycle is measured at 1.4V.
7. Supply Voltage Range = 4.0 to 5.5 Volts
8. Temperature Range = 0 °C to 70 °C

SYMBOL	PARAMETER	MIN	MAX	NOTES
STROBE TIMING				
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	10	-	
MCLK AND VCLK TIMINGS				
Tr	Rise Time	-	3	Duty Cycle 40% min. to
Tf	Fall Time	-	3	60% max.
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	15	ns

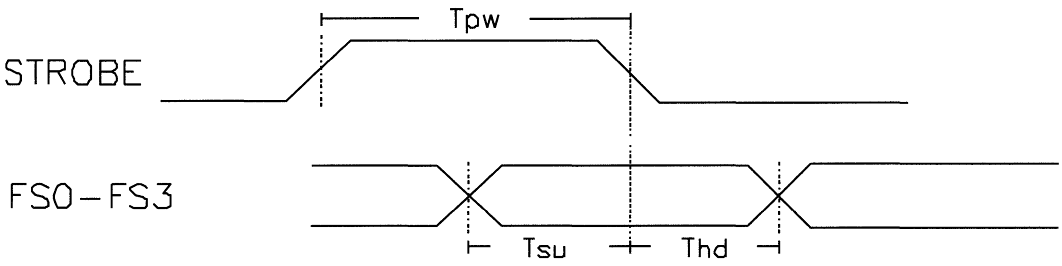


Figure 3

ICS2492 Pattern Request Form

In addition to the pattern below, custom patterns are also available, although a significant volume commitment and/or one-time mask charge will apply. Contact ICS sales for details.

ICS Part Number	ICS2492-453		ICS2492-Custom Pattern #1
Address FS3-0 (Hex)	Frequency (MHz)	Application	Frequency (MHz)
0	20	286-10	
1	24	-12	
2	32	386-16	
3	40	-20	
4	50	-25	
5	66.6	-33	
6	80	-40	
7	100	-50	
8	54	TURBO-27	
9	70	-35	
0	90	-45	
B	110	-55	
C	25	486-25	
D	33.3	-33	
E	40	-40	
F	50	-50	
Address MS0 (Hex)	Frequency (MHz)	Application	Frequency (MHz)
0	16	AT-BUS	
1	24	FDC	

Custom pattern #1 reference frequency = ______________

The standard frequency shown has been specified by and is supported by the respective VGA manufacturer.
The standard pattern shown above uses _____ MHz as the input reference frequency.
Order Information: ICS2492M-XXX or ICS2492N-XXX (XXX=Pattern number)

Ordering Information

ICS2492N-XXX or ICS2492M-XXX

Example:

ICS XXXX N -XXX

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type

N=DIP (Plastic)
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS2694

Motherboard Clock Generator

Description

The **ICS2694** Motherboard Clock Generator is an integrated circuit using PLL and VCO technology to generate virtually all the clock signals required in a PC. The use of the device can be generalized to satisfy the timing needs of most digital systems by reprogramming the VCO or reconfiguring the counter stages which derive the output frequencies from the VCO's.

The primary VCO is customarily used to generate the CPU clock and is so labeled on the **ICS2694**. Pre-programmed frequency sets are listed on page 6. These choices were made to match the major microprocessor families. CPUSEL (0-3) allow the user to select the appropriate frequency for the application.

Due to the filter in the phase-locked loop, the CPUCLK will move in a linear fashion from one frequency to a newly-selected frequency without glitches. If a fixed CPUCLK value is desired, CPUSEL (0-3) may be hard wired to the desired address with STROBE tied high. (It has a pull-up.) For board test and debug, pulling OUTPUTE to Ground will tristate all the outputs.

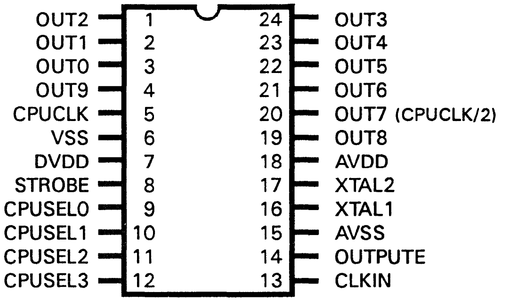
Features

- Low cost - eliminates multiple oscillators and Count Down Logic
- Primary VCO has 16 Mask Programmable frequencies (normally CPU clock)
- Secondary VCO has 1 Mask Programmable frequency (usually 96 MHz)
- Pre-programmed versions for typical PC applications
- 10 Outputs in addition to the primary CPU clock
- Capability to reconfigure counter stages to change the frequencies of the outputs via mask options
- Advanced PLL design
- On-chip PLL filters
- Very Flexible Architecture

Applications

- CPU clock and Co-processor clock
- Hard Disk and Floppy Disk clock
- Keyboard clock
- Serial Port clock
- Bus clock
- System counting or timing functions

Pin Configuration



24-Pin DIP or SOIC
K-5, K-7

Pin Description

PIN NUMBER	NAME	DESCRIPTION
1	OUT2	4mA Output
2	OUT1	4mA Output
3	OUT0	4mA Output
4	OUT9	4mA Output
5	CPUCLK	4mA Output driven by Voltage Controlled Oscillator 1 (VC01). VC01 is controlled by a 16 word ROM.
6	VSS	Ground for digital portion of chip
7	DVDD	Plus supply for digital portion of chip
8	STROBE	Input control for transparent latches associated with CPU (0-3) which select one of 16 values for CPUCLK. Holding STROBE high causes the latches to be transparent.
9	CPUSEL0	LSB CPUCLK address bit
10	CPUSEL1	CPUCLK address bit
11	CPUSEL2	CPUCLK address bit
12	CPUSEL3	MSB CPUCLK address bit
13	CLKIN	An alternative input for the reference clock. The crystal oscillator output and CLKIN are gated together to generate the reference clock for the VCO's. If CLKIN is used, XTAL1 should be held high and XTAL2 left open. If the internal oscillator is used, hold CLKIN high.
14	OUTPUTE	Pulling this line low tristates all outputs.
15	AVSS	Ground for analog portion of chip
16	XTAL1	Input of internal crystal oscillator stage
17	XTAL2	Output of internal crystal oscillator stage. This pin should have nothing connected to it but one of the quartz crystal terminals.
18	AVDD	Positive supply for analog portion of chip.
19	OUT8	4mA Output
20	OUT7	4mA Output (Usually assigned as CPUCLK/2 for co-processor use)
21	OUT6	4mA Output
22	OUT5	4mA Output
23	OUT4	4mA Output
24	OUT3	4mA Output

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series-resonant crystal should be connected between XTAL1 (1) and XTAL2 (2). In IBM-compatible applications, this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10 MHz and 25 MHz have been tested. Maintain short lead lengths between the crystal and the **ICS2694**. In order to optimize the quality of the quartz crystal oscillator, the input switching threshold of XTAL1 is VDD/2 rather than the conventional 1.4 V of TTL. Therefore, XTAL1 may not respond properly to a legal TTL signal since TTL is not required to exceed VDD/2. Therefore, another clock input CLKIN (pin 13) has been added to the chip which is sized to have an input switching point of 1.4 V. Inside the chip, these two inputs are ANDED. Therefore, when using the XTAL1 and XTAL2, CLKIN should be held high. (It has a pull-up.) When using CLKIN, XTAL1 should be held high. (It does not have a pull-up because a pull-up would interfere with the oscillator bias.)

It is anticipated that some applications will use both clock inputs, properly gated, for either board test or unique system functions. By generating all the system clocks from one reference input, the phase and delay relationships between the various outputs will remain relatively fixed, thereby eliminating problems arising from totally unsynchronized clocks interacting in a system.

Power Supply Conditioning

The **ICS2694** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in some applications it may be judicious to decouple the power supply as shown in Figures 1 or 2. Figure 1 is the normal configuration for 5 Volt only applications. Which of the two provides superior performance depends on the noise content of the power supplies. In general, the configuration of Figure 1 is satisfactory. Figure 2 is the more conventional if a 12 Volt analog supply is available, although the improved performance comes at a cost of an extra component; however, the cost of the discretes used in Figure 2 are less than the cost of Figure 1's discrete components.

Since the **ICS2694** outputs a large number of high-frequency clocks, conservative design practices are recommended. Care should be exercised in the board layout of supply and ground traces, and adequate power supply decoupling capacitors consistent with the application should be used.

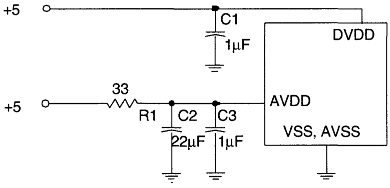


Figure 1

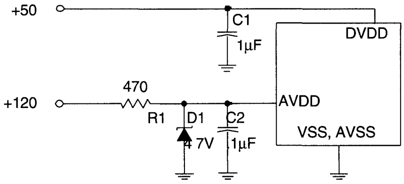


Figure 2

Absolute Maximum Ratings

Supply Voltage	V_{DD}	-0.5V to +7V
Input Voltage	V_{IN}	-0.5V to VDD +0.5V
Output Voltage	VOUT	-0.5V to VDD +0.5V
Clamp Diode Current	V_{IK} & I_{OK}	±30mA
Output Current per Pin	I_{OUT}	±50mA
Operating Temperature	T_O	0°C to + 150°C
Storage Temperature	T_S	-85°C to + 150°C
Power Dissipation	P_D	500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to > = V_{SS} and < = V_{DD}.

DC Characteristics (0°C to 70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Operating Voltage Range	V_{DD}		4.0	5.5	V
Input Low Voltage	V_{IL}	V_{DD} = 5V	VSS	0.8	V
Input High Voltage	V_{IH}	V_{DD} = 5V	2.0	V_{DD}	V
Input Leakage Current	I_{IH}	V_{IN} = V_{cc}	-	10	*u*A
Output Low Voltage	V_{OL}	I_{OL} = 4.0 mA	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = 4.0 mA	2.4	-	V
Supply Current	I_{DD}	V_{DD} = 5V, CPUCLK = 80 MHz	-	55	mA
Internal pull-up Resistors	R_{UP} *	V_{DD} = 5V, V_{in} = 0V	50	-	k ohm
Input Pin Capacitance	C_{in}	F_c = 1 MHz	-	8	pf
Output Pin Capacitance	C_{out}	F_c = 1 MHz	-	12	pf

* The following inputs have pull-ups: OUTPUTE, STROBE, CPUSEL (0-3), CLKIN.

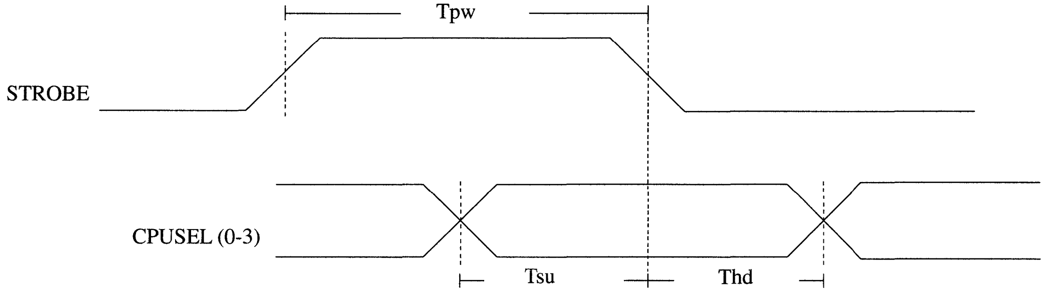
AC Timing Characteristics

The following notes apply to all parameters presented in this section:

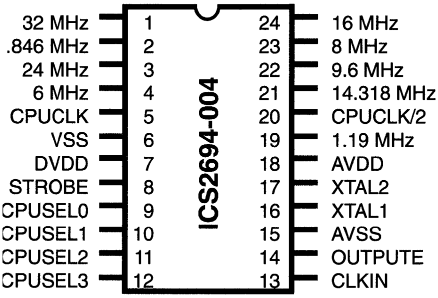
1. Xtal Frequency = 14.31818 MHz
2. All units are in nanoseconds (ns).
3. Rise and fall time is between 0.8 and 2.0 VDC.
4. Output pin loading = 15pF
5. Duty cycle is measured at 1.4V.
6. Supply Voltage Range = 4.5 to 5.5 Volts
7. Temperature Range = 0 °C to 70 °C

SYMBOL	PARAMETER	MIN	MAX	NOTES
STROBE TIMING				
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	10	-	
FOUT TIMING				
Tr	Rise Time	-	3	Duty Cycle 40% min. to 60% max.
Tf	Fall Time	-	3	at 80 MHz
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz

Note:
Pattern -004 has rising edges of CPUCLK and CPUCLK/2 matched to ± 2 ns.



ICS2694 Standard Patterns



CPUSEL0-3 (Hex)	CPUCLK OUTPUT (Pin 5) (MHz)
0	2
1	10
2	20
3	24
4	25
5	32
6	33.33
7	40
8	48
9	50
10	54
11	66.67
12	68
13	80
14	100
15	16

Note: Pattern -004 has rising edges of CPUCLK and CPUCLK/2 matched to ± 2 ns.

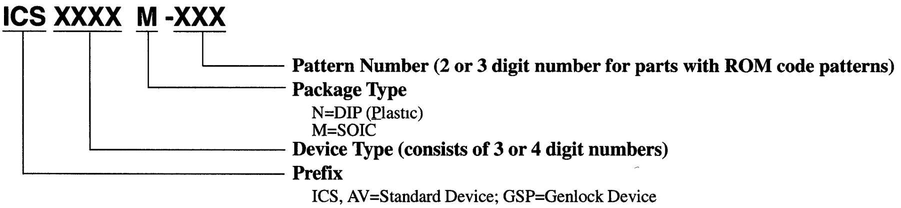
Another alternative for CPU CLOCK generation is the ICS2494-244 if the additional functions of the **ICS2694** are not needed in the application.

ICS Part Number	ICS2494-244
Address FS3-0 (Hex)	Frequency (MHz)
0	20
1	24
2	32
3	40
4	50
5	66.6
6	80
7	100
8	54
9	70
0	90
B	110
C	25
D	33.3
E	40
F	50
Address MS1-0 (Hex)	Frequency (MHz)
0	16
1	24
2	50
3	66.6

Ordering Information

ICS2694N-XXX or ICS2694M-XXX

Example:



Integrated
Circuit
Systems, Inc.

AV9107C

CPU Frequency Generator

General Description

The **AV9107C** offers a tiny footprint solution for generating two simultaneous clocks. One clock, the REFCLK, is a fixed output frequency which is the same as the input reference crystal (or clock). The other clock, CLK1, can vary between 2 and 120 MHz, with up to 16 selectable preprogrammed frequencies stored in internal ROM (frequency range depends on design option).

The device has advanced features which include on-chip loop filters, tristate outputs, and power-down capability. A minimum of external components - two decoupling capacitors and an optional ferrite bead - are all that are required for jitter-free operation. Standard versions for computer motherboard applications are the **AV9107C-03**, and **AV9107C-05**. Custom masked versions, with customized frequencies and features, are available in 6-8 weeks for a small NRE.

Features

- Patented on-chip Phase-Locked Loop with VCO for clock generation
- Provides reference clock and synthesized clock
- Generates frequencies from 2 to 120 MHz (depending on option)
- 8-pin DIP or SOP package or 14-pin DIP or SOP package
- 2 to 32 MHz input reference frequency (depending on option)
- On-chip loop filter
- Up to 16 frequencies stored internally
- Low power CMOS technology
- Single +3.3 or +5 volt power supply

Applications

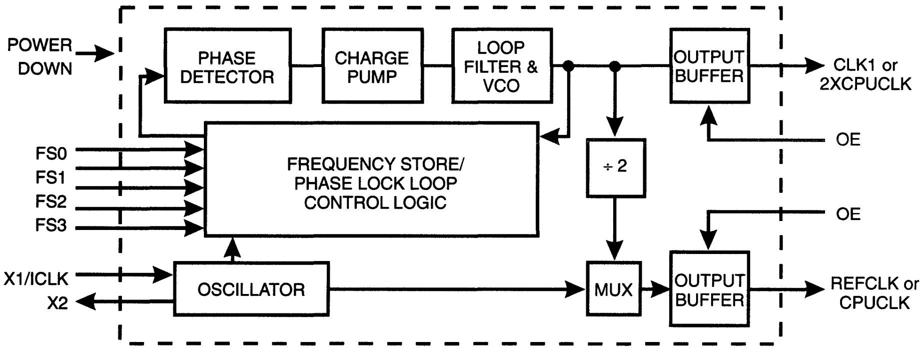
Graphics: The **AV9107C** is the easiest to use, lowest cost, and smallest footprint frequency generator for graphics applications. It can generate up to 16 different frequencies, including all frequencies necessary for VGA standards. It should be used in place of the AV9105/6 when the reference clock is also needed.

Computer: The **AV9107C** is the ideal solution for replacing high speed oscillators and for reducing clock speeds to save power in computers. The device provides smooth, glitch-free frequency transitions so that the CPU can continue to operate during slow down or speed up. The rate of frequency change makes the **AV9107C** compatible with all 386DX, 386SX, 486DX, 486DX2, and 486SX devices. Standard versions include the **AV9107C**-03, -05, -10, -11.

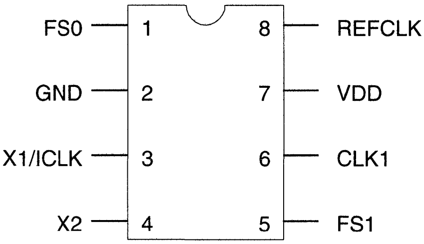
Disk Drives: Smaller than a single crystal or an oscillator, the tiny SOIC package can be used for any general purpose frequency generation in disk drives. The most popular application is for Constant Density Recording, where its low jitter output clock provides the necessary frequencies for reading and recording. Another popular application is for slowing the disk drive CPU to save power.

High Speed Systems: The **AV9107C** can be used as a proximity oscillator - using a low frequency (down to 2 MHz) input to generate a high frequency clock (up to 120 MHz) near the device requiring the high frequency (depending on option). This avoids the need to route high speed traces over a long distance.

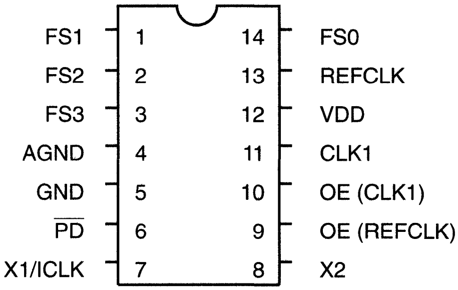
Block Diagram



Pin Configuration



AV9107C-05/-10
8-Pin DIP, SOIC
K-3, K-6



AV9107C-03/-11
14-Pin DIP, SOIC
K-3, K-6

Pin Descriptions for AV9107C-03, AV9107C-05 and AV9107C-10

PIN NUMBER		PIN NAME	TYPE	DESCRIPTION
-05/-10	-03			
1	14	FS0	Input	Frequency Select 0 for CLK1 (-03 has pull-up).
5	1	FS1	Input	Frequency Select 1 for CLK1 (-03 has pull-up).
	2	FS2	Input	Frequency Select 2 for CLK1 (-03 has pull-up).
	3	FS3	Input	Frequency Select 3 for CLK1 (-03 has pull-up).
	4	AGND	-	Analog GROUND.
2	5	GMD	-	Digital GROUND.
	6	$\overline{\text{PD}}$	Input	POWER-DOWN. Shuts off chip when low. Internal pull-up.
3	7	X1/ICLK	Input	CRYSTAL OUTPUT or INPUT CLOCK frequency. Typically 14.318 MHz system clock.
4	8	X2	Output	CRYSTAL OUTPUT (No Connect when clock used.).
	9	OE(REFCLK)	Input	OUTPUT ENABLE. Tristates REFCLK when low. Pull-up.
	10	OE(CLK1)	Input	OUTPUT ENABLE. Tristates CLK1 when low. Pull-up.
6	11	CLK1	Output	CLOCK1 Output (see decoding tables).
7	12	VDD	-	Digital power supply (+5V DC).
8	13	REFCLK	Output	REFERENCE CLOCK output. Produces a buffered version of the input clock or crystal frequency (typically 14.318 MHz).

Frequency Accuracy and Calculation

The accuracy of the frequencies produced by the **AV9107C** depends on the input frequency and the desired actual output frequency. The formula for calculating the exact frequency is as follows:

$$\text{Output Frequency} = \text{Input Frequency} \times \frac{A}{B}$$

where A=2, 3, 4 ... 128, and
B=2, 3, 4 ... 32.

For example, to calculate the actual output frequency for a video monitor expecting a 44.900 MHz clock and using a 14.318 MHz input clock, the closest A/B ratio is 69/22, which gives an output of 44.906 MHz (within 0.02% of the target frequency). Generally, the **AV9107C** can produce frequencies within 0.1% of the desired output.

Allowable Input and Output Frequencies for Possible Options

The input frequency should be between 2 and 32 MHz, depending on options, and the A/B ratio should not exceed 24. The output should fall in the range of 2-120 MHz, depending on options.

Output Enable

The Output Enable feature tristates the specified output clock pins. This places the selected output pins in a high impedance state to allow for system level diagnostic testing.

Power-Down

If equipped, the power-down shuts off the specified PLL or entire chip to save current. A few milliseconds are required to reach full functioning speed from a power-down state.

Frequency Transitions

A key **AV9107C** feature is the ability to provide glitch-free frequency transitions across its output frequency range. The **AV9107C-03** provides smooth transitions between any of the two groups of eight frequencies (when FS3=0 or FS3=1), so that the device will switch glitch-free between 4-100 MHz and 2-50 MHz.

Absolute Maximum Ratings

AVDD, VDD referenced to GND 7V
Operating temperature under bias . . . . 0°C to +70°C
Storage temperature . . . . -65°C to +150°C
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V
Power dissipation . . . . 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5V

Operating V_{DD} = +4.5V to +5.5V; T_A =0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-	6.0	16.0	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-2.0	-	2.0	µA
Output Low Voltage, Note 1	V_{OL}	I_{OL}=10mA	-	0.15	0.40	V
Output High Voltage, Note 1	V_{OH}	I_{OH}=-30mA	2.4	3.25	-	V
Output Low Current, Note 1	I_{OL}	V_{OL}=0.8V	22.0	35.0	-	mA
Output High Current, Note 1	I_{OH}	V_{OH}=2.0V	-	-50.0	-35.0	mA
Supply Current	I_{CC}	Unload, 50 MHz	-	18.0	42.0	mA
Supply Current	I_{CC} (PD low)	Unload, Logic Inputs 000	-	38.0	100.0	µA
Supply Current	I_{CC} (PD low)	Unload, Logic Inputs 111	-	14.0	40.0	µA
Pull-up Resistor, Note 1	R_{pu}		-	380.0	700.0	k ohms
AC Characteristics						
Rise Time 0.8 to 2.0V, Note 1	T_r	15pf load	-	0.60	1.40	ns
Fall Time 2.0 to 0.8V, Note 1	T_f	15pf load	-	0.40	1.00	ns
Rise Time 20% to 80%, Note 1	T_r	15pf load	-	2.0	3.5	ns
Fall Time 80% to 20%, Note 1	T_f	15pf load	-	1.0	2.5	ns
Duty Cycle, Note 1	D_t	15pf load @ 1.4V	45.0	50.0	55.0	%
Jitter, One Sigma, Note 1	T_{jis}	From 20 to 100 MHz	-	50.0	150.0	ps
Jitter, One Sigma, Note 1	T_{jis}	From 14 to 16 MHz		100.0	200.0	ps
Jitter, One Sigma, Note 1	T_{jis}	From 14 to Below		0.2	1.0	%
Jitter, Absolute, Note 1	T_{jab}	From 20 to 100 MHz	-250.0		250.0	ps
Jitter, Absolute, Note 1	T_{jab}	From 14 to 16 MHz	-500.0		500.0	ps
Jitter, Absolute, Note 1	T_{jab}	From 14 to Below		1.0	3.0	%
Input Frequency, Note 1	F_I		11.0	14.3	19.0	MHz
Output Frequency	F_o		2.0	-	120.0	MHz
Power-up Time, Note 1	T_{pu}		-	7.58	18.0	ms
Transition Time, Note 1	T_{ft}	8 to 66.6 MHz	-	6.0	13.0	ms

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

Operating V_{DD} = +3.0V to +3.7V; T_A =0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.20V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-	2.5	7.0	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-2.0	-	2.0	µA
Output Low Voltage, Note 1	V_{OL}	I_{OL}=6mA	-	0.15	0.1	V
Output High Voltage, Note 1	V_{OH}	I_{OH}=-5mA	0.85	0.92	-	V
Output Low Current, Note 1	I_{OL}	V_{OL}=$0.2V_{DD}$	15.0	22.0	-	mA
Output High Current, Note 1	I_{OH}	V_{OL}=$0.7V_{DD}$	-	-17.0	-10.0	mA
Supply Current	I_{CC}	Unloaded, 50 MHz	-	22.0	40.0	mA
Supply Current	I_{CC} (PD low)	Unload, Logic Inputs 000	-	13.0	40.0	µA
Supply Current	I_{CC} (PD low)	Unload, Logic Inputs 111	-	4.0	12.0	µA
Pull-up Resistor	R_{pu}		-	550.0	900.0	k ohms
AC Characteristics						
Rise Time 20% to 80%, Note 1	T_r	15pf load	-	2.2	3.5	ns
Fall Time 80% to 20%, Note 1	T_f	15pf load	-	1.2	2.5	ns
Duty Cycle, Note 1	D_t	15pf load @ 50%	40.0	46.0	53.0	%
Jitter, One Sigma, Note 1	T_{j1s}	From 25 to 85 MHz	-	50.0	150.0	ps
Jitter, One Sigma, Note 1	T_{j1s}	From 14 to 20 MHz		100.0	200.0	ps
Jitter, One Sigma, Note 1	T_{j1s}	From 14 to Below		0.4	1.0	%
Jitter, Absolute, Note 1	T_{jab}	From 25 to 85 MHz	-250.0		250.0	ps
Jitter, Absolute, Note 1	T_{jab}	From 14 to 20 MHz	-500.0		500.0	ps
Jitter, Absolute, Note 1	T_{jab}	From 14 to Below		1.0	3.0	%
Input Frequency, Note 1	F_I		13.3	14.3	15.3	MHz
Output Frequency, Note 1	F_O		2.0	-	66.6	MHz
Power-up Time, Note 1	T_{pu}		-	7.58	18.0	ms
Transition Time, Note 1	T_{ft}	8 to 66.6 MHz	-	6.0	13.0	ms

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Actual Frequencies

Decoding Table for AV9107C-05, 14.318 input

FS1	FS0	CLK1
0	0	40.01 MHz
0	1	50.11 MHz
1	0	66.61 MHz
1	1	80.01 MHz

*5V only

Decoding Table for AV9107C-03, 14.318 input

FS3	FS2	FS1	FS0	CLK1
0	0	0	0	16.00 MHz
0	0	0	1	39.99 MHz
0	0	1	0	50.11 MHz
1	0	1	1	80.01 MHz
0	1	0	0	66.58 MHz
0	1	0	1	100.23 MHz
0	1	1	0	8.02 MHz
0	1	1	1	4.01 MHz
1	0	0	0	8.02 MHz
1	0	0	1	20.00 MHz
1	0	1	0	25.06 MHz
1	0	1	1	40.01 MHz
1	1	0	0	33.29 MHz
1	1	0	1	50.11 MHz
1	1	1	0	4.01 MHz
1	1	1	1	2.05 MHz

*5V only

Decoding Table for AV9107C-11 (in MHz)

FS3	FS2	FS1	FS0	CLK1
0	0	0	0	16.00 MHz
0	0	0	1	33.99 MHz
0	0	1	0	50.11 MHz
1	0	1	1	80.01 MHz
0	1	0	0	66.58 MHz
0	1	0	1	100.23 MHz
0	1	1	0	60.00 MHz
0	1	1	1	4.01 MHz
1	0	0	0	8.02 MHz
1	0	0	1	20.00 MHz
1	0	1	0	25.06 MHz
1	0	1	1	39.99 MHz
1	1	0	0	33.25 MHz
1	1	0	1	50.11 MHz
1	1	1	0	30.00 MHz
1	1	1	1	4.01 MHz

*5V only

Decoding Table for AV9107C-10, 14.318 Input

FS1	FS0	CLK1
0	0	25.057 MHz
0	1	33.289 MHz
1	0	40.006 MHz
1	1	50.113 MHz

*5V only

Ordering Information

AV9107C-05CN8, AV9107C-10CN8, AV9107C-03CN14, AV9107C-11CN14 or
AV9107C-05CS8, AV9107C-10CS8, AV9107C-03CS14, AV9107C-11CS14

Example:

XXX XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
N=DIP (Plastic)
S=SOP

Pattern Number (2 or 3 digit number for parts with ROM code patterns, if applicable)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

ICS9108

CPU Frequency Generator

General Description

The **AV9108** offers a tiny footprint solution for generating two simultaneous clocks. One clock, the REFCLK, is a fixed output frequency which is the same as the input reference crystal (or clock). The other clock, CLK1, can vary between 2 and 120 MHz, with up to 16 selectable preprogrammed frequencies stored in internal ROM.

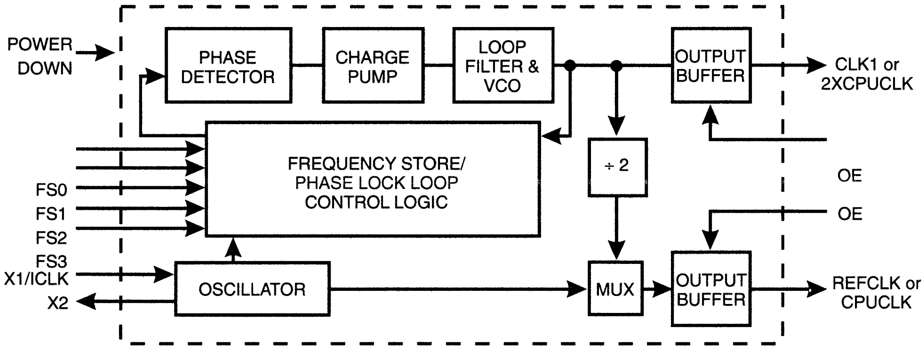
The **ICS9108** is ideal for use in a 3.3V system. It can generate a 66.66 MHz clock at 3.3V. In addition, the **ICS9108** provides a symmetrical wave form with a worst case duty cycle of 45/55. The **ICS9108** has very tight edge control between the CPU clock and 2XCPU clock outputs, with a worst case skew of 250ps.

The device has advanced features which include on-chip loop filters, tristate outputs, and power-down capability. A minimum of external components - two decoupling capacitors and an optional ferrite bead - are all that are required for jitter-free operation. Standard versions for computer motherboard applications are the **AV9108-03**, **AV9108-05** and the **ICS9108-10**. Custom masked versions, with customized frequencies and features, are available in 6-8 weeks for a small NRE fee.

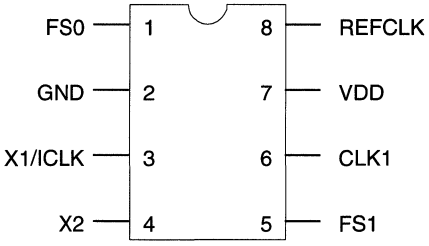
Features

- Runs up to 80 MHz at 3.3V
- 50/50 typical duty cycle at 5V
- ±250ps absolute jitter
- Generates frequencies from 2 to 140 MHz
- 2 to 32 MHz input reference frequency
- Up to 16 frequencies stored internally
- Patented on-chip Phase Locked Loop with VCO for clock generation
- Provides reference clock and synthesized clock
- On-chip loop filter
- Low power 0.8µ CMOS technology
- 8-pin or 14-pin DIP or SOIC package

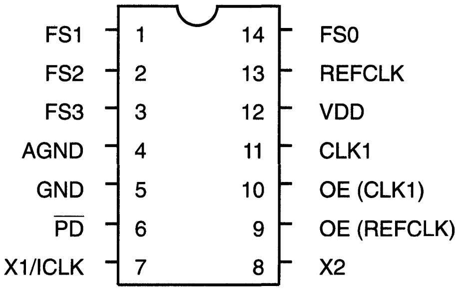
Block Diagram



Pin Configuration



AV9108-05/-10
8-Pin DIP, SOIC
K-3, K-6



AV9108-03/-11
14-Pin DIP, SOIC
K-3, K-6

Pin Descriptions for AV9108-03, AV9108-05 and AV9108-10

PIN NUMBER		PIN NAME	TYPE	DESCRIPTION
-05/-10/-13	-03			
1	14	FS0	Input	Frequency Select 0 for CLK1 (-03 has pull-up).
5	1	FS1	Input	Frequency Select 1 for CLK1 (-03 has pull-up).
	2	FS2	Input	Frequency Select 2 for CLK1 (-03 has pull-up).
	3	FS3	Input	Frequency Select 3 for CLK1 (-03 has pull-up).
	4	AGND	-	Analog GROUND.
2	5	GMD	-	Digital GROUND.
	6	$\overline{PD}$	Input	POWER-DOWN. Shuts off chip when low. Internal pull-up.
3	7	X1/ICLK	Input	CRYSTAL OUTPUT or INPUT CLOCK frequency. Typically 14.318 MHz system clock.
4	8	X2	Output	CRYSTAL OUTPUT (No Connect when clock used.).
	9	OE(REFCLK)	Input	OUTPUT ENABLE. Tristates REFCLK when low. Pull-up.
	10	OE(CLK1)	Input	OUTPUT ENABLE. Tristates CLK1 when low. Pull-up.
6	11	CLK1	Output	CLOCK1 Output (see decoding tables).
7	12	VDD	-	Digital power supply (+3V DC).
8	13	REFCLK	Output	REFERENCE CLOCK output. Produces a buffered version of the input clock or crystal frequency (typically 14.318 MHz).

Actual Frequencies

Decoding Table for AV9108-05, 14.318 input

FS1	FS0	CLK1
0	0	40.01 MHz
0	1	50.11 MHz
1	0	66.61 MHz
1	1	80.01 MHz

Decoding Table for AV9108-03, 14.318 input

FS3	FS2	FS1	FS0	CLK1
0	0	0	0	16.00 MHz
0	0	0	1	39.99 MHz
0	0	1	0	50.11 MHz
1	0	1	1	80.01 MHz
0	1	0	0	66.58 MHz
0	1	0	1	100.23 MHz
0	1	1	0	8.02 MHz
0	1	1	1	4.01 MHz
1	0	0	0	8.02 MHz
1	0	0	1	20.00 MHz
1	0	1	0	25.06 MHz
1	0	1	1	40.01 MHz
1	1	0	0	33.29 MHz
1	1	0	1	50.11 MHz
1	1	1	0	4.01 MHz
1	1	1	1	2.05 MHz

Decoding Table for AV9108-10, 14.318 input

FS1	FS0	CLK1
0	0	25.057 MHz
0	1	33.289 MHz
1	0	40.006 MHz
1	1	50.113 MHz

Decoding Table for AV9108-11 (in MHz)

FS3	FS2	FS1	FS0	CLK1
0	0	0	0	16.00 MHz
0	0	0	1	33.39 MHz
0	0	1	0	50.11 MHz
1	0	1	1	80.01 MHz
0	1	0	0	66.58 MHz
0	1	0	1	100.23 MHz
0	1	1	0	60.00 MHz
0	1	1	1	4.01 MHz
1	0	0	0	8.02 MHz
1	0	0	1	20.05 MHz
1	0	1	0	25.06 MHz
1	0	1	1	39.99 MHz
1	1	0	0	33.25 MHz
1	1	0	1	50.11 MHz
1	1	1	0	30.00 MHz
1	1	1	1	4.01 MHz

Note: The dash number following ICS9108 must be included when ordering product since it specifies the frequency decoding table being ordered. Decoding options can be created by a simple metal mask change.

Frequency Accuracy and Calculation

The accuracy of the frequencies produced by the **ICS9108** depends on the input frequency and the desired actual output frequency. The formula for calculating the exact frequency is as follows:

$$\text{Output Frequency} = \text{Input Frequency} \times \frac{A}{B}$$

where A=2, 3, 4 ... 128, and
B=2, 3, 4 ... 32.

For example, to calculate the actual output frequency for a video monitor expecting a 44.900 MHz clock and using a 14.318 MHz input clock, the closest A/B ratio is 69/22, which gives an output of 44.906 MHz (within 0.02% of the target frequency). Generally, the **ICS9108** can produce frequencies within 0.1% of the desired output.

Allowable Input and Output Frequencies

The input frequency should be between 2 and 32 MHz and the A/B ratio should not exceed 24. The output should fall in the range of 2-120 MHz.

Output Enable

The Output Enable feature tristates the specified output clock pins. This places the selected output pins in a high impedance state to allow for system level diagnostic testing.

Power-Down

If equipped, the power-down shuts off the specified PLL or entire chip to save current. A few milliseconds are required to reach full functioning speed from a power-down state.

Frequency Transitions

A key **ICS9108** feature is the ability to provide glitch-free frequency transitions across its output frequency range. The **ICS9108** provides smooth transitions between any of the two groups of eight frequencies (when FS3=0 or FS3=1), so that the device will switch glitch-free between 4-100 MHz and 2-50 MHz.

Absolute Maximum Ratings

AVDD, VDD referenced to GND 7V
Operating temperature under bias .... 0°C to +70°C
Storage temperature .... -65°C to +150°C
Voltage on I/O pins referenced to GND........... GND -0.5V to VDD +0.5V
Power dissipation .... 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5V

(Operating V_{DD} = +4.5V to +5.5V; T_A =0°C to 70°C unless otherwise stated)

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-	6.0	16	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-2.0	-	2.0	µA
Output Low Voltage	V_{OL}	I_{OL}=10mA	-	0.15	0.40	V
Output High Voltage, Note 1	V_{OH}	I_{OH}=-30mA	2.4	3.25	-	V
Output Low Current, Note 1	I_{OL}	V_{OL}=0.8V	22.0	35.0	-	mA
Output High Current, Note 1	I_{OH}	V_{OH}=2.0V	-	-50.0	-35.0	mA
Supply Current	I_{CC}	Unload, 50 MHz	-	18.0	42.0	mA
Supply Current	I_{CC} (PD low)	Unload, Logic Inputs 000	-	38.0	100.0	µA
Supply Current	I_{CC} (PD low)	Unload, Logic Inputs 111	-	14.0	40.0	µA
Pull-up Resistor, Note 1	R_{pu}		-	380.0	700.0	k ohms
AC Characteristics						
Rise Time 0.8 to 2.0V, Note 1	T_r	15pf load	-	0.60	1.40	ns
Fall Time 2.0 to 0.8V, Note 1	T_f	15pf load	-	0.40	1.00	ns
Rise Time 20% to 80%, Note 1	T_r	15pf load	-	2.0	3.5	ns
Fall Time 80% to 20%, Note 1	T_f	15pf load	-	1.0	2.5	ns
Duty Cycle, Note 1	D_t	15pf load @ 1.4V	45.0	50.0	55.0	%
Jitter, One Sigma, Note 1	T_{jis}	From 20 to 100 MHz	-	50.0	150.0	ps
Jitter, One Sigma, Note 1	T_{jis}	From 14 to 16 MHz		100.0	200.0	ps
Jitter, One Sigma, Note 1	T_{jis}	From 14 to Below		0.2	1.0	%
Jitter, Absolute, Note 1	T_{jab}	From 20 to 100 MHz	-250.0		250.0	ps
Jitter, Absolute, Note 1	T_{jab}	From 14 to 16 MHz	-500.0		500.0	ps
Jitter, Absolute, Note 1	T_{jab}	From 14 to Below		1.0	3.0	%
Input Frequency, Note 1	F_i		11.0	14.3	19.0	MHz
Output Frequency	F_o		2.0	-	120.0	MHz
Power-up Time, Note 1	T_{pu}		-	7.58	18.0	ms
Transition Time, Note 1	T_{ft}	8 to 66.6 MHz	-	6.0	13.0	ms

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

(Operating V_{DD} = +3.0V to +3.7V; T_A =0°C to 70°C unless otherwise stated)

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.20V_{DD}	V
Input High Voltage	V_{IH}		0.7V_{DD}	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-	2.5	7.0	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-2.0	-	2.0	µA
Output Low Voltage	V_{OL}	I_{OL}=6mA	-	0.15	0.1	V
Output High Voltage	V_{OH}	I_{OH}=-5mA	0.85	0.92	-	V
Output Low Current	I_{OL}	V_{OL}=0.2V_{DD}	15.0	22.0	-	mA
Output High Current	I_{OH}	V_{OL}=0.7V_{DD}	-	-17.0	-10.0	mA
Supply Current	I_{CC}	Unloaded, 50 MHz	-	22.0	40.0	mA
Supply Current	I_{CC} (PD low)	Unload, Logic Inputs 000	-	13.0	40.0	µA
Supply Current	I_{CC} (PD low)	Unload, Logic Inputs 111	-	4.0	12.0	µA
Pull-up Resistor	R_{pu}		-	550.0	900.0	k ohms
AC Characteristics						
Rise Time 20% to 80%, Note 1	T_r	15pf load	-	2.2	3.5	ns
Fall Time 80% to 20%	T_f	15pf load	-	1.2	2.5	ns
Duty Cycle	D_t	15pf load @ 50%	40.0	46.0	60.0	%
Jitter, One Sigma	T_{jis}	From 25 to 85 MHz	-	50.0	150.0	ps
Jitter, One Sigma	T_{jis}	From 14 to 20 MHz		100.0	200.0	ps
Jitter, One Sigma	T_{jis}	From 14 to Below		0.4	1.0	%
Jitter, Absolute	T_{jab}	From 25 to 85 MHz	-250.0		250.0	ps
Jitter, Absolute	T_{jab}	From 14 to 20 MHz	-500.0		500.0	ps
Jitter, Absolute	T_{jab}	From 14 to Below		1.0	3.0	%
Input Frequency	F_i		13.3	14.3	15.3	MHz
Output Frequency	F_o		2.0	-	90.0	MHz
Power-up Time, Note 1	T_{pu}		-	7.58	18.0	ms
Transition Time, Note 1	T_{ft}	8 to 66.6 MHz	-	6.0	13.0	ms

Parameter is guaranteed by design and characterization.

Ordering Information

ICS9108-05CN8, ICS9108-05CS8; ICS9108-10CN8, ICS91808-10CS8;
ICS9108-03CN14, ICS9108-03CS14; ICS9108-11CN14, ICS9108-11CS14

Example:

XXX XXXX -XX M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width
Package Type
N=DIP (Plastic); S=SOIC
Pattern Number (2 or 3 digit number for parts with ROM code patterns)
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS9120-08
ICS9120-09
Product Preview

Frequency Generator for Multimedia Audio Synthesis

General Description

The **ICS9120-08** and **ICS9120-09** are high performance frequency generators designed to support stereo audio codec systems. They offer both clock frequencies required by stereo codecs such as the CS4231 and the AD1848 plus the clock needed for the OPL4 FM synthesizer. These frequencies can be synthesized from the existing 14.318 MHz system clock or from the on-chip oscillator using a 14.318 MHz crystal (-08 only).

High accuracy, low jitter PLLs meet the 0.10% frequency tolerance and -96dB signal-to-noise ratios required by 16-bit audio systems. Fast output clock edge rates minimize board induced jitter.

Unlike competitive devices, the **ICS9120-08** and **ICS9120-09** operate over the entire 3.0-5.5V range, with the -09 providing power-down to minimize energy consumption.

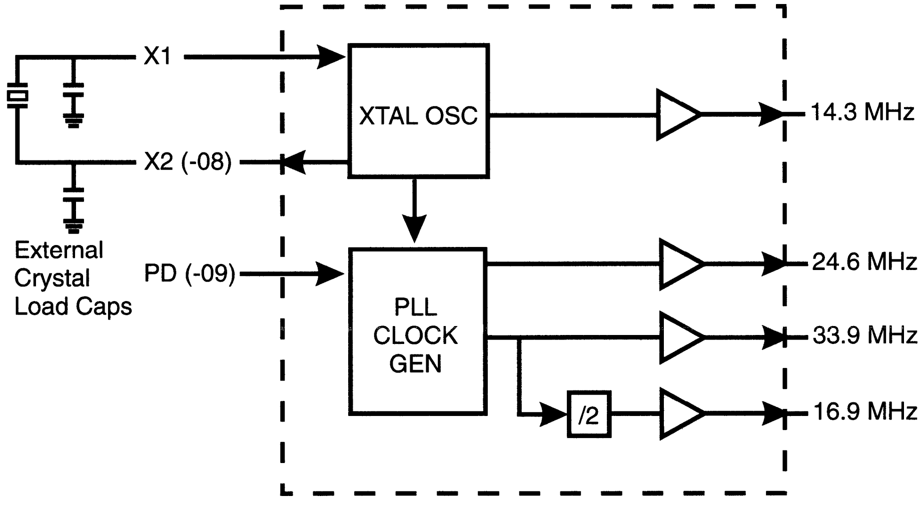
Features

- Generates 16.9344 MHz and 24.576 MHz stereo codec clocks plus the 33.868 MHz OPL4 clock
- Single 14.318 MHz crystal or system clock reference
- Buffered REFCLK output
- 0.10% frequency accuracy meets OPL4 specifications
- 85ps one sigma jitter maintains 16-bit performance
- Output rise/fall times less than 2.0ns
- On-chip loop filter components
- 3.3V-5V supply range
- 8-pin, 150-mil SOIC

Applications

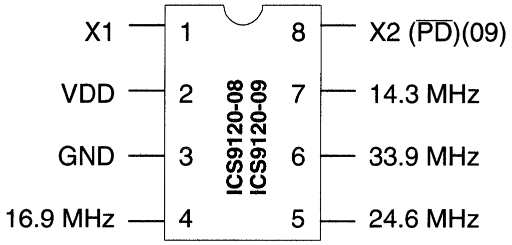
- Specifically designed to support the high performance requirements of multimedia audio systems

Block Diagram



ICS9120-08
ICS9120-09

Pin Configuration



8-Pin SOIC
K-6

Functionality (ICS9120-08, ICS9120-09)

VDD=3.0-5.5V, TEMP=0-70°C

X1, X2 (MHz)	(-09 only) PD\	33.9 (MHz)	16.9 (MHz)	24.6 (MHz)	14.3 (MHz)
-	0	Low	Low	Low	Low
14.318	1	33.868	16.934	24.576	14.318

Note: $\overline{PD}$ (Pin 8) is internally pulled-up to VDD and therefore may be left disconnected or driven by open collector logic.

Pin Descriptions for ICS9120-08

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	X1	Input	Crystal or external clock source
2	VDD	Power	+Power supply input
3	GND	Power	Ground return for Pin 2
4	CLK3	Output	16.9 MHz clock output
5	CLK1	Output	24.6 MHz clock output
6	CLK2	Output	33.9 MHz clock output
7	REF	Output	14.318 MHz reference clock output
8	X2	Output	Crystal output drive

Pin Descriptions for ICS9120-09

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	X1	Input	Crystal or external clock source
2	VDD	Power	+Power supply input
3	GND	Power	Ground return for Pin 2
4	CLK3	Output	16.9 MHz clock output
5	CLK1	Output	24.6 MHz clock output
6	CLK2	Output	33.9 MHz clock output
7	REF	Output	14.318 MHz reference clock output
8	$\overline{PD}$	Input	Power-down input powers down entire device when low; has pull-up

Absolute Maximum Ratings

AVDD, VDD referenced to GND	7V
Operating temperature under bias	0°C to +70°C
Storage temperature	-65°C to +150°C
Voltage on I/O pins referenced to GND	GND -0.5V to VDD +0.5V
Power dissipation	0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5V

Operating V_{DD} = +4.5V to +5.5V; T_A =0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V *(For -09 only)*	-	-8.3	-18.0	µA
Input High Current	I_{IH}	V_{IN}=V_{DD} *(For -09 only)*	-	-	5.0	µA
Output Low Voltage	V_{OL}*	I_{OL}=+10mA	-	0.15	0.4	V
Output High Voltage	V_{OH}*	I_{OH}=-30mA	2.4	3.7	-	V
Output Low Current	I_{OL}*	V_{OL}=0.8V	25.0	45.0	-	mA
Output High Current	I_{OH}*	V_{OH}=2.4V	-	-53.0	-35.0	mA
Supply Current	I_{CC}	Unloaded	-	22.0	50.0	mA
Supply Current	I_{CC}	Unloaded *(For -09 only)*	-	180.0	500.0	µA
Pull-up Resistor Value	R_{pu}*	*(For -09 only)*	-	400.0	800.0	k ohm
AC Characteristics						
Rise Time 0.8 to 2.0V	T_r*	15pf load	-	0.9	2.0	ns
Fall Time 2.0 to 0.8V	T_f*	15pf load	-	0.7	1.5	ns
Rise Time 20% to 80%	T_r*	15pf load	-	1.8	3.25	ns
Fall Time 80% to 20%	T_f*	15pf load	-	1.4	2.5	ns
Duty Cycle	D_t*	15pf load @ 50% of VDD; Except REFCLK	45.0	50.0	55.0	%
Duty Cycle	D_t*	15pf load @ 50% of VDD; REFCLK only	40.0	50.0	60.0	%
Jitter, One Sigma	T_{j1s}*	For all frequencies except REFCLK	-	85.0	-	ps
Jitter, Absolute	T_{jab}	For all frequencies except REFCLK	-700.0	380.0	700.0	ps
Jitter, One Sigma	T_{j1s}*	REFCLK only	-	266.0	600.0	ps
Jitter, Absolute	T_{jab}	REFCLK only	-1.5	380.0	1.5	ns
Input Frequency	F_i*		11.0	14.0	17.0	MHz
Output Frequency	F_o*		11.0	-	42.0	MHz
Power-up Time	T_{pu}*	0 to 33.8 MHz	-	5.5	12.0	ms
Crystal Input Capacitance	C_{inx}*	X1 (Pin 1), X2 (Pin 8; -08 only)	-	5	-	pf

* Parameter guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

Operating V_{DD} = +3.0V to +3.7V; T_A =0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V *(For -09 only)*	-	-3.6	-8.0	µA
Input High Current	I_{IH}	V_{IN}=V_{DD} *(For -09 only)*	-	-	5.0	µA
Output Low Voltage	V_{OL}*	I_{OL}=6mA	-	$0.05V_{DD}$	0.1	V
Output High Voltage	V_{OH}*	I_{OH}=-4.0mA	$0.85V_{DD}$	$0.94V_{DD}$	-	V
Output Low Current	I_{OL}*	V_{OL}=$0.2V_{DD}$	15.0	24.0	-	mA
Output High Current	I_{OH}*	V_{OH}=$0.7V_{DD}$	-	-13.0	-8.0	mA
Supply Current	I_{CC}	Unloaded	-	13.0	32.0	mA
Supply Current	I_{CC}(PD)	Unloaded *(For -09 only)*	-	50.0	110.0	µA
Pull-up Resistor Value	R_{pu}*	*(For -09 only)*	-	620.0	900.0	k ohm
AC Characteristics						
Rise Time 0.8 to 2.0V	T_r*	15pf load	-	1.5	4.0	ns
Fall Time 2.0 to 0.8V	T_f*	15pf load	-	1.0	3.0	ns
Rise Time 20% to 80%	T_r*	15pf load	-	2.2	4.0	ns
Fall Time 80% to 20%	T_f*	15pf load	-	1.5	3.0	ns
Duty Cycle	D_t*	15pf load @ 50% of VDD; Except REFCLK	45.0	50.0	55.0	%
Duty Cycle	D_t*	15pf load @ 50% of VDD; REFCLK only	40.0	45.0	60.0	%
Jitter, One Sigma	T_{jis}*	For all frequencies except REFCLK	-	100.0	-	ps
Jitter, Absolute	T_{jab}	For all frequencies except REFCLK	-900.0	380.0	900.0	ps
Jitter, One Sigma	T_{jis}*	REFCLK only	-	266.0	600.0	ps
Jitter, Absolute	T_{jab}	REFCLK only	-1.5	380.0	1.5	ns
Input Frequency	F_i*		11.0	14.3	15.0	MHz
Output Frequency	F_o*		11.0	-	38.0	MHz
Power-up Time	T_{pu}*	0 to 33.8 MHz	-	5.5	12.0	ms
Crystal Input Capacitance	C_{inx}*	X1 (Pin 1), X2 (Pin 8; -08 only)	-	5	-	pf

* Parameter guaranteed by design and characterization. Not 100% tested in production.

Ordering Information

ICS9120M-08, ICS9120M-09

Example:

XXX XXXX M-PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

ICS9131

Advance Information

32 kHz Motherboard Frequency Generator

General Description

The **ICS9131** offers a tiny footprint solution for generating a selectable CPU clock from a 32.768 kHz crystal. The device allows a variety of microprocessors to be clocked by changing the state of address lines FS0, FS1, and FS2. The **ICS9131** is the ideal solution for replacing high speed oscillators and for reducing clock speeds to save power in computers. The device provides smooth, glitch-free frequency transitions so that the CPU can continue to operate during slow down or speed up. The rate of frequency change makes the **ICS9131** compatible with all 386DX, 386SX, 486DX, 486DXZ, 486SX and Pentium™ microprocessors.

The **ICS9131** is driven from a single 32.768 kHz crystal. The only external components required are the crystal and a 10M ohm resistor. The device generates the 14.318 MHz system clock, eliminating the need for a 14.318 MHz crystal. High-Performance applications may require high speed clock termination components.

VDD32 Supply

The **ICS9131** has a separate power supply for the 32.768 kHz oscillator circuitry. This allows the 32 kHz clock to run from a battery or other source while the main power to the chip is disconnected. The VDD32 supply is guaranteed to operate down to +2.0V, with the clock consuming less than 10μA at +3.3V and the main VDD at 0V.

The frequencies and power-down options in the **ICS9131** are mask programmable. Customer specific masks can be made and prototypes delivered within 6-8 weeks from receipt of order. ICS also offers standard versions, such as those described in this data sheet.

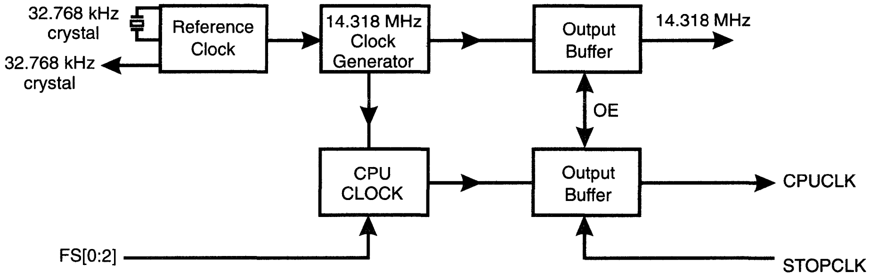
Features

- Single 32.768 kHz crystal generates system clock and selectable CPU clock
- Generates CPU clocks from 8 MHz to 100 MHz.
- Operates from 3.3V or 5.0V supply
- Operates up to 66 MHz at 3.3V
- Separate VDD for 32 kHz clock enables it to run from battery
- STOPCLK feature allows for a glitch-free on and turn-off of the CPU clock to static processors
- Output enable tristates outputs
- 16-pin PDIP or SOIC package
- Frequency selects allow for a smooth transition of the CPUCLK

Applications

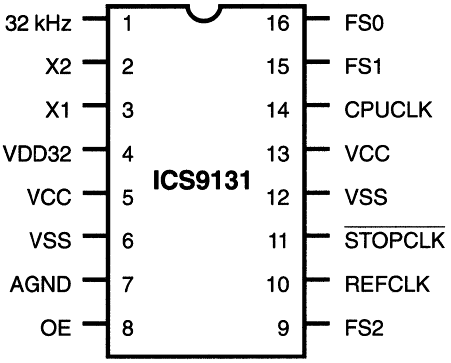
Notebook/Palmtop Computers: The **ICS9131** works with +3V and +5V and a single 32.768 kHz crystal, making it the ideal solution for generating clocks in portables with minimum board space. The user can save power by using this single part instead of oscillators or other frequency generators. The **ICS9131** further reduces the current consumption by having the ability to completely shut down the individual clocks when not in use, while still maintaining the separately powered 32.768 kHz clock.

Block Diagram



Pentium is a trademark of Intel

Pin Configuration



16-Pin PDIP or SOIC
K-4, K-6

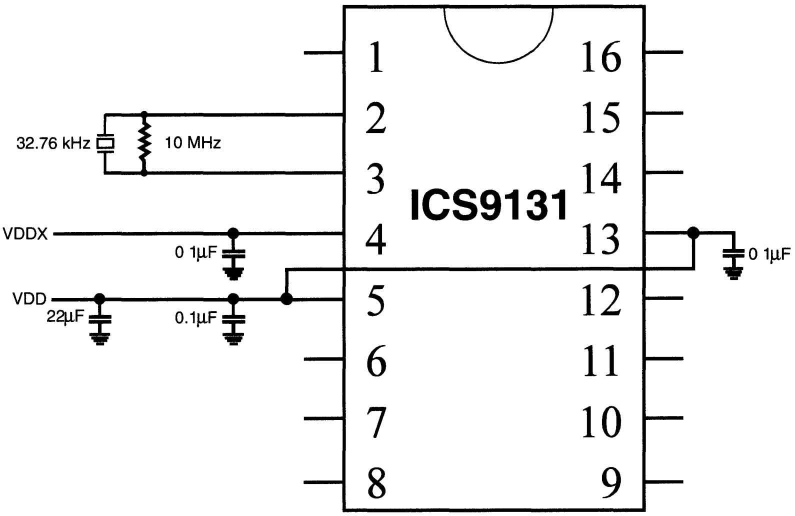
Decoding Table for CPU Clock

FS2	FS1	FS0	CPUCLK	ACTUALS
0	0	0	16	16.004
0	0	1	25	25.059
0	1	0	33.3	33.412
0	1	1	40	40.095
1	0	0	50	50.119
1	0	1	60	60.142
1	1	0	66.6	66.484
1	1	1	80	80.190

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	32 kHz	OUTPUT	32.768 kHz output
2	X2	OUTPUT	Connect 32 kHz crystal
3	X1	INPUT	Connect 32 kHz crystal
4	VDD32		Power Supply for 32 kHz oscillator
5	VCC		Power Supply (+3.3V - 5.0V)
6	VSS		Ground
7	AGND		Analog Ground
8	OE	INPUT	OE tristates outputs when low
9	FS2	INPUT	CPU clock frequency select 2
10	REFCLK	OUTPUT	14.318 MHz output
11	$\overline{\text{STOPCLK}}$	INPUT	Stops CPU clock when low
12	VSS		Ground
13	VCC		Power supply (+3.3V - 5.0V)
14	CPUCLK	OUTPUT	CPU clock output (see Decoding table)
15	FS1	INPUT	CPU clock frequency select 1
16	FS0	INPUT	CPU clock frequency select 0

Recommended External Circuit



Notes:

1) The external components shown should be placed as close to the device as possible.
2) Pins 5 and 13 should be connected together externally. One decoupling capacitor may suffice for both pins.

Absolute Maximum Ratings

VDD referenced to GND	7V
Operating temperature under bias	0°C to +70°C
Storage temperature	-40°C to +150°C
Voltage on I/O pins referenced to GND	GND -0.5V to VDD+0.5V
Power dissipation	0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5V

Operating V_{DD} = +4.5V to +5.5V; T_A =0°C to 70°C unless otherwise stated

DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-	6.0	15.0	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-2.0	-	2.0	µA
Pull-up Resistor	R_{pu}	V_{IN}=V_{DD}-1V, Note 1	-	400	700	k ohms
Output Low Current	I_{OL}	V_{OUT}=0.8V, Note 1	25	45	-	mA
Output High Current	I_{OH}	V_{OUT}=2.0V, Note 1	-	-53	-35	mA
Output Low Voltage	V_{OL}	I_{OL}=10mA	-	0.15	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-30mA, Note 1	2.4	3.7	-	V
Supply Current	I_{DD}	No load, at 50 MHz	-	18	35	mA
Output Frequency Change over Supply and Temperature	F_d	With respect to typical frequency, Note 1	-	0.002	0.05	%
Standby Supply Current	$I_{DDSTDBY}$	Note 2, unloaded	-	12	25	µA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.
Note 2: With the STOPCLK pin low (active).
Note 3: Absolute Jitter measured as the shortest and longest period difference to the mean period of the sample set.

Electrical Characteristics at 5V

Operating V_{DD} = +4.5V to +5.5V; T_A =0°C to 70°C unless otherwise stated

AC Characteristics

Output Frequency	f_o	Clock1, Note 1	12.0	-	100	MHz
Input Frequency	f_i	Note 1	2.0	32	38	kHz
Output Rise time, 0.8 to 2.0V	t_r	15 pf load, Note 1	-	0.60	1.4	ns
Rise time, 20% to 80% V_{DD}	t_r	15 pf load, Note 1	-	1.6	3.0	ns
Output Fall time, 2.0V to 0.8V	t_f	15 pf load, Note 1	-	0.50	1.2	ns
Fall time, 80% to 20% V_{DD}	t_f	15 pf load, Note 1	-	0.9	2.5	ns
Duty cycle	d_t	15 pf load, Note 1	45	50	55	%
Jitter, 1 sigma from 33-80 MHz	T_{jis}	10,000 samples, Note 1	-	50	150	ps
Jitter, Absolute from 33-80 MHz	T_{jabs}	10,000 samples, Notes 1, 3	-250	-	250	ps
Jitter, 1 sigma from 16-25 MHz	T_{jis}			60	150	ps
Jitter, Absolute from 16-25 MHz	T_{jabs}		-600	-	600	ps
Jitter, 1 sigma from 14 to below	T_{jis}		-	1	3	%
Jitter, Absolute from 14 to below	T_{jabs}		-	2%	5	%
Frequency Transition time	t_{ft}		2.0	5.0	10.0	mS
Power-up time	t_{pu}	Note 1	3.0	7.5	15	mS

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.
Note 2: With the STOPCLK pin low (active).
Note 3: Absolute Jitter measured as the shortest and longest period difference to the mean period of the sample set.

Electrical Characteristics at 3.3V

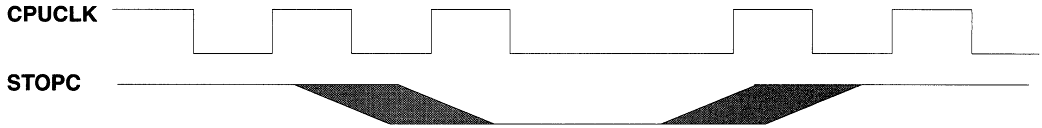
Operating V_{DD} = +3.3V to +3.7V; T_A =0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.2 Vdd	V
Input High Voltage	V_{IH}		0.7 V_{dd}	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-	2.5	7.0	μA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-2.0	-	2.0	μA
Pull-up Resistor	R_{pu}	V_{IN}=V_{DD}-1V, Note 1	-	600	900	k ohms
Output Low Current	I_{OL}	V_{OUT}=0.2V, Note 1	15	24	-	mA
Output High Current	I_{OH}	V_{OUT}=0.7V, Note 1	-	-13	-8	mA
Output Low Voltage	V_{OL}	I_{OL}=60mA	-	0.05 V_{dd}	0.1 V_{dd}	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA, Note 1	6.85 V_{dd}	0.94 V_{dd}	-	V
Supply Current	I_{DD}	No load, at 50 MHz	-	13	25	mA
Output Frequency Change over Supply and Temperature	F_d	With respect to typical frequency, Note 1	-	0.002	0.05	%
Standby Supply Current	$I_{DDSTDBY}$	Note 2, No load	-	8	15	mA
AC Characteristics						
Output Frequency	f_o	Clock1, Note 1	12.0	-	100	MHz
Input Frequency	f_I	Note 1	2.0	32	38	kHz
Rise time, 20% to 80% V_{DD}	t_r	15 pf load, Note 1	-	2.2	3.5	ns
Fall time, 80% to 20% V_{DD}	t_f	15 pf load, Note 1	-	1.2	2.5	ns
Duty cycle	d_t	15 pf load, Note 1	43	-	53	%
Jitter, 1 sigma	T_{jis}	10,000 samples, Note 1	-	50	150	ps
Jitter, Absolute	T_{jabs}	10,000 samples, Notes 1, 3	-250		250	ps
Jitter, 1 sigma from 16-25 MHz	T_{jis}		-	60	150	ps
Jitter, Absolute from 16-25 MHz	T_{jabs}		-600	-	600	ps
Jitter, 1 sigma from 14 to below	T_{jis}		-	1	3	%
Jitter, Absolute from 14 to below	T_{jabs}		-	2	5	%
Frequency Transition time	t_{ft}			6.7	14.0	mS
Power-up time	t_{pu}	Note 1	-	8.55	17.0	mS

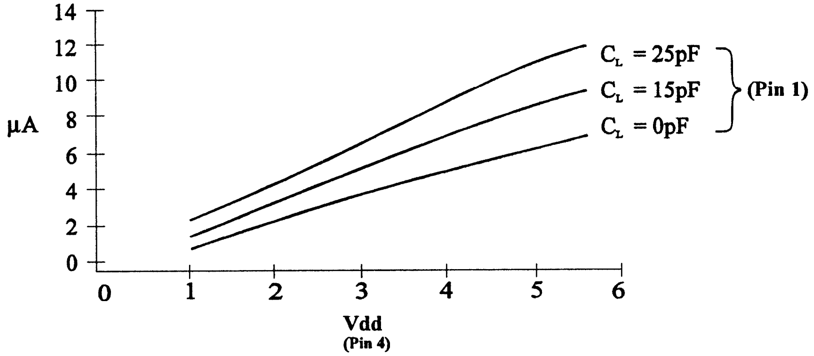
Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.
Note 2: With the STOPCLK pin low (active).
Note 3: Absolute Jitter measured as the shortest and longest period difference to the mean period of the sample set.

Stop Clock Feature

The **ICS9131** incorporates a unique stop clock feature compatible with static logic processors. When the stop clock pin goes low, the CPUCLK will go low after the next occuring falling edge. When STOPCLK again goes high, CPUCLK resumes on the next rising edge of the internal clock. This feature enables fast, glitch-free starts and stops of the CPUCLK and is useful in Energy Star motherboard applications.



32 kHz Supply Current



Ordering Information

ICS9131N16 or ICS9131M16

Example:

ICS XXXX M

Package Type

N=DIP (Plastic)
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV=Standard Device; GSP=Genlock Device

Integrated Circuit Systems, Inc.

ICS9133X

Advance Information

32 kHz Motherboard Frequency Generator

General Description

The **ICS9133X** is designed to generate clocks for all 286, 386, 486, Pentium and RISC-based motherboards, including laptops and notebook computers. The only external components required are a 32.768 kHz crystal and decoupling capacitors. The device generates the 14.318 MHz system clock, eliminating the need for a 14.318 MHz crystal. High performance applications may require high speed clock termination components. The chip includes three independent clock generators plus the 32.768 kHz reference clock to produce all necessary frequencies, including real time clock/DRAM refresh, master clock, CPU clock, twice CPU clock frequency, keyboard clock, floppy disk controller clock, serial communications clock and bus clocks. Different frequencies from clocks #2 and #3 can be selected using the frequency select pins, but clock #1 will be at 14.318 MHz for all standard versions.

VDD32 Supply

The **ICS9133X** has a separate power supply for the 32.768 kHz oscillator circuitry. This allows the 32 kHz clock to run from a battery or other source while the main power to the chip is disconnected. The VDD32 supply is guaranteed to operate down to +2.0V, with the clock consuming less than 10µA at +3.3V with the main VDD at 0V.

The frequencies and power-down options in the **ICS9133X** are mask programmable. Customer specific masks can be made and prototypes delivered within 6-8 weeks from receipt of order. Integrated Circuit Systems also offers standard versions, such as that described in this data sheet.

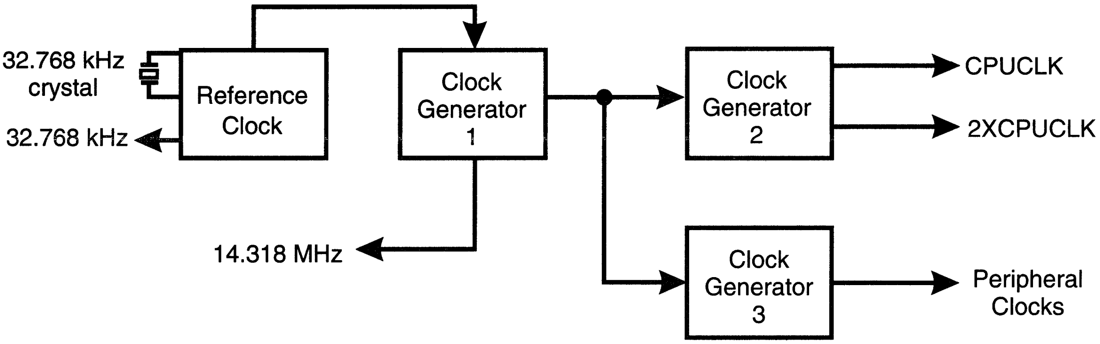
Features

- Single 32.768 kHz crystal generates all PC motherboard clocks
- Cost-reduced version of popular ICS9132
- 3 independent clock generators
- Generates CPU clocks from 12.5 to 100 MHz
- Up to 7 output clocks
- Separate VDD for 32 kHz clock
- Output enable tristates outputs
- Power-down options available
- Operates from 3.3V or 5.0V supply
- Operates up to 66 MHz at 3.3V
- Skew controlled 2x and 2x CPU clocks
- 20-pin PDIP or SOIC package

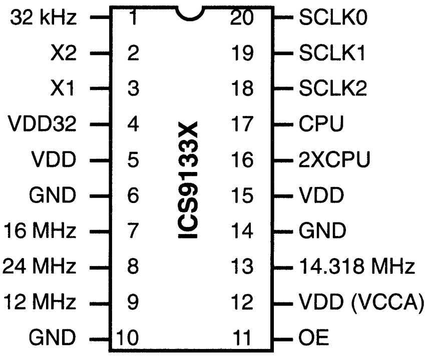
Applications

Notebook/Palmtop Computers: The **ICS9133X** works with +3V and +5V and a single 32.768 kHz crystal, making it the ideal solution for generating clocks in portables with minimum board space. The user can save power by using this single part instead of oscillators or other frequency generators. The **ICS9133X** further reduces the current consumption by having the ability to completely shut down the individual clocks when not in use, while still maintaining the separately powered 32.768 kHz clock.

Block Diagram



Pin Configuration



20-Pin PDIP or SOIC
K-4, K-7

Decoding Table for CPU Clock

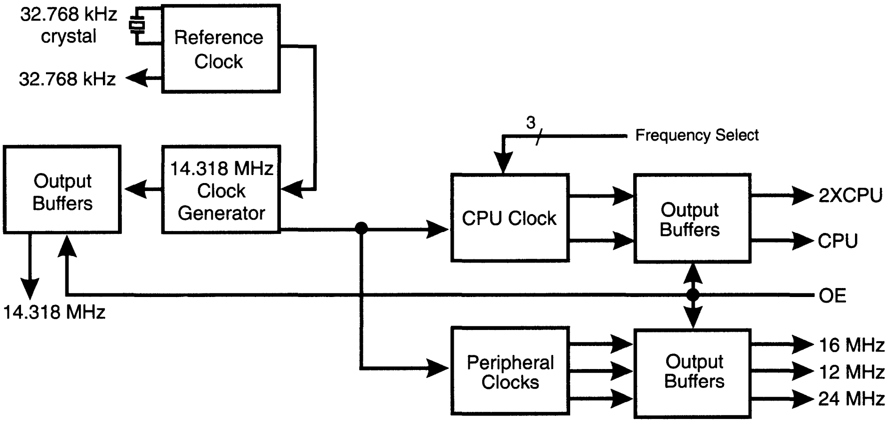
SCLK22	SCLK21	SCLK20	2XCPU	CPU
0	0	0	8	4
0	0	1	16	8
0	1	0	32	16
0	1	1	40	20
1	0	0	50	25
1	0	1	66.6	33.3
1	1	0	80*	40*
1	1	1	100*	50*

* Only at 5V supply voltage

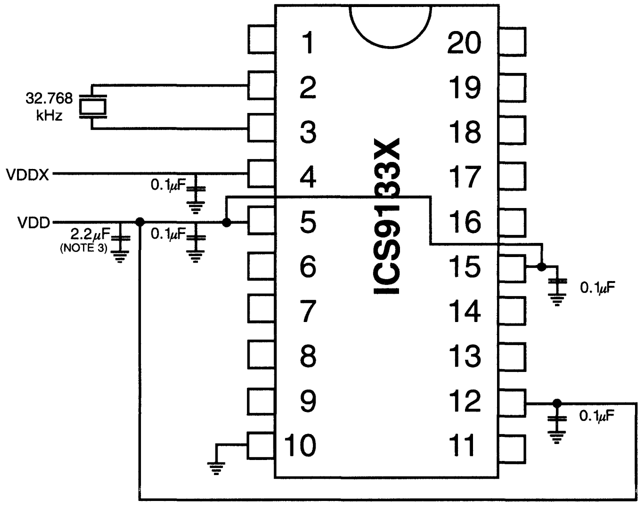
Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	32 kHz	Output	32.768 kHz output
2	X2	Output	Connect 32 kHz crystal
3	X1	Input	Connect 32 kHz crystal
4	VDD32	-	Power supply for 32 kHz oscillator only
5	VDD	-	Power supply (+3.3 to +5.0V)
6	GND	-	GROUND
7	16 MHz	Output	16 MHz clock output
8	24 MHz	Output	24 MHz clock output
9	12 MHz	Output	12 MHz clock output
10	GND	-	GROUND
11	OE	Input	OE tristate outputs when low. Has internal pull-up.
12	VDD	-	Power supply (+3.3 to +5.0V)
13	14.318 MHz	Output	14.318 MHz clock output
14	GND	-	GROUND
15	VDD	-	Power supply (+3.3 to +5.0V)
16	2XCPU	Output	2XCPU clock output (see decoding table)
17	CPU	Output	CPU clock output (see decoding table)
18	SCLK2	Input	CPU clock frequency SELECT2. Has internal pull-up.
19	SCLK1	Input	CPU clock frequency SELECT1. Has internal pull-up.
20	SCLK0	Input	CPU clock frequency SELECT0. Has internal pull-up.

Block Diagram for ICS9133X



Recommended External Circuit



NOTES:

1. The external components shown should be placed as close to the device as possible.
2. Pins 5 and 15 should be connected together externally. One decoupling capacitor may suffice for both pins.
3. May be part of system decoupling.

Absolute Maximum Ratings

VDD referenced to GND	7V
Operating temperature under bias	0°C to +70°C
Storage temperature	-40°C to150°C
Voltage on I/O pins referenced to GND	GND -0.5V to VDD +0.5V
Power dissipation	0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} = +3.0 to 3.7V, T_A=0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.2V_{DD}	V
Input High Voltage	V_{IH}		0.7V_{DD}	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V (Pull-up)	-	-	12	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-	-	2*	µA
Output Low Voltage	V_{OL}	I_{OL}=4mA	-	-	0.1	V
Output High Voltage	V_{OH}	I_{OH}=-1mA	V_{DD}-.1V	-	-	V
Output High Current	V_{OH}	IOH=-4mA	-	-	-	V
Output High Current	V_{OH}	IOH=-8mA	2.4	-	-	V
Output Frequency Change over Supply and Temperature	F_D	With respect to typical frequency[1]	-	.005	0.05	%
Short circuit current	I_{SC}	Each output clock	-	15	-	mA
Supply Current	I_{CC}	No load, 40 MHz	-	10	-	mA
Pull-up resistor value	R_{pu}		-	620	-	kΩ
AC Characteristics						
Input Clock Rise Time	t_{ICr}		-	-	5	µs
Input Clock Fall Time	t_{ICf}		-	-	5	µs
Output Rise time, 0.8 to 2.0V	t_r	15 pf load	-	1.5	2	ns
Rise time, 20% to 80% V_{DD}	t_f	15 pf load	-	2.5	4	ns
Output Fall time, 2.0 to 0.8V	t_f	15 pf load	-	1.5	2	ns
Fall time, 80% to 20% V_{DD}	t_f	15 pf load	-	2.5	4	ns
Duty cycle	d_t	15 pf load	43/57	48/52	57/43	%
Duty cycle, reference clocks	d_t	15 pf load, Note 1	40/60	43/57	60/40	%
Jitter, one sigma		As compared with clock period.	-	1	3	%
Jitter, absolute	t_{jab}		-	2	5	%
Input Frequency	f_i		25	32.768	40	kHz
Clock skew between any Clock #2 outputs	T_{sk}		-	100	500	ps
Power-up time	t_{pu}	From off to 40 MHz	-	1,000	-	ms

NOTE 1: 32 kHz output duty cycle is dependent on crystal used.

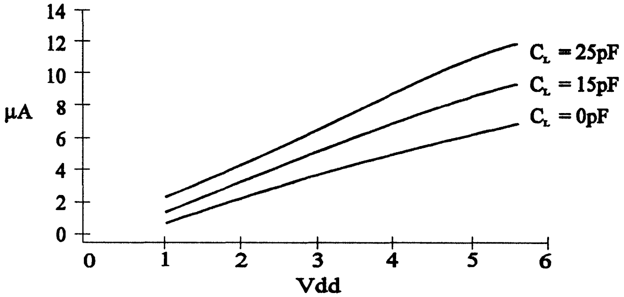
Electrical Characteristics

V_{DD} = +5V±10%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.2V_{DD}	V
Input High Voltage	V_{IH}		0.7V_{DD}	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V (Pull-up)	-	-	15	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-	-	2*	µA
Output Low Voltage	V_{OL}	I_{OL}=4mA	-	-	0.1	V
Output High Voltage	V_{OH}	I_{OH}=-1mA	V_{DD}-.1V	-	-	V
Output High Voltage	V_{OH}	I_{OH}=-4mA	-	-	-	V
Output High Voltage	V_{OH}	I_{OH}=-8mA	2.4	-	-	V
Output Frequency Change over Supply and Temperature	F_D	With respect to typical frequency	-	.005	0.05	%
Short circuit current	I_{SC}	Each output clock	-	33	-	mA
Supply Current	I_{CC}	No load, 40 MHz	-	17	-	mA
Pull-up resistor value	R_{pu}	Note 1	-	380	-	kΩ
AC Characteristics						
Input Clock Rise Time	t_{ICr}		-	-	5	µs
Input Clock Fall Time	t_{ICf}		-	-	5	µs
Output Rise time, 0.8 to 2.0V	t_r	15 pf load	-	1	1.5	ns
Rise time, 20% to 80% V_{DD}	t_r	15 pf load	-	2	3	ns
Output Fall time, 2.0 to 0.8V	t_f	15 pf load	-	1	1.5	ns
Fall time, 80% to 20% V_{DD}	t_f	15 pf load	-	2	3	ns
Duty cycle	d_t	15 pf load	43/57	48/52	57/43	%
Duty cycle, reference clocks	d_t	15 pf load, Note 1	40/60	43/57	60/40	%
Jitter, one sigma	t_{j1s}	As compared with clock period	-	1	3	%
Jitter, absolute	t_{jab}		-	2	5	%
Input Frequency	f_i		25	32.768	40	kHz
Clock skew between any Clock #2 outputs	T_{sk}		-	100	500	ps
Power-up time	t_{pu}	From off to 40 MHz	-	10	-	ms

NOTE 1: 32 kHz output duty cycle is dependent on crystal used.

32 kHz Supply Current



Ordering Information

ICS9133XN20 (DIP) or ICS9133XM20 (SOIC)

Example:

ICS XXXX M

Package Type
N=DIP (Plastic)
M=SOIC
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS=Standard Device

ICS9134-06
ICS9134-07
Advance Information

32 kHz Motherboard Frequency Generator

General Description

The **ICS9134-06** and **ICS9134-07** are designed to generate clocks for all 286, 386, 486, Pentium and RISC-based motherboards, including laptops and notebook computers. The only external components required are a 32.768 kHz crystal and decoupling capacitors. The device generates the 14.318 MHz system clock, eliminating the need for a 14.318 MHz crystal. High performance applications may require high speed clock termination components. The chip includes three independent clock generators plus the 32.768 kHz reference clock to produce all necessary frequencies, including real time clock/DRAM refresh, master clock, CPU clock, keyboard clock, floppy disk controller clock, serial communications clock and bus clocks. Different frequencies from clocks #2 can be selected using the frequency select pins, but clock #1 will be at 14.318 MHz for all standard versions.

VDD32 Supply

The **ICS9134-06** and **ICS9134-07** have a separate power supply for the 32.768 kHz oscillator circuitry. This allows the 32 kHz clock to run from a battery or other source while the main power to the chip is disconnected. The VDD32 supply is guaranteed to operate down to +2.0V, with the clock consuming less than 10μA at +3.3V with the main VDD at 0V.

The frequencies and power-down options in the **ICS9134-06** and **ICS9134-07** are mask programmable. Customer specific masks can be made and prototypes delivered within 6-8 weeks from receipt of order. Integrated Circuit Systems also offers standard versions, such as that described in this data sheet.

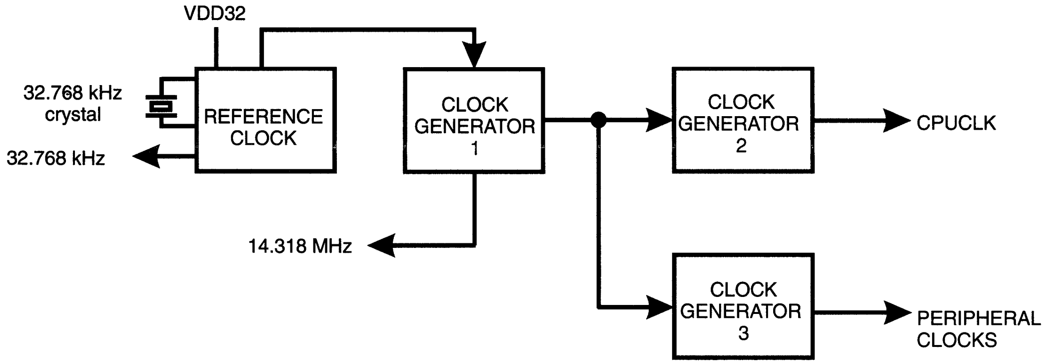
Features

- I_{DD} <10 μA when 32 kHz is running
- Single 32.768 kHz crystal generates all PC motherboard clocks
- 3 independent clock generators
- Generates CPU clocks from 4.0 to 80 MHz
- Up to 5 output clocks
- Separate VDD for 32 kHz clock
- Power-down options available
- Operates from 3.3V or 5.0V supply
- Operates up to 66 MHz at 3.3V
- Supports OPTi 80C463/5 and Fir™ chipsets
- 16-pin, 300 mil, SOIC package

Applications

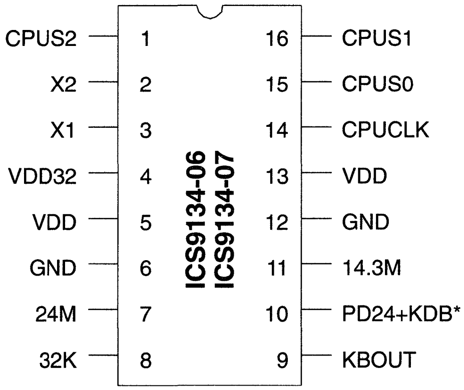
Notebook/Palmtop Computers: The **ICS9134-06** and **ICS9134-07** work with +3.3V and +5V and a single 32.768 kHz crystal, making it the ideal solution for generating clocks in portables with minimum board space. The user can save power by using this single part instead of oscillators or other frequency generators. The **ICS9134-06** and **ICS9134-07** further reduce the current consumption by having the ability to completely shut down the individual clocks when not in use, while still maintaining the separately powered 32.768 kHz clock.

Block Diagram



Fir is a trademark of Picopower Corporation

Pin Configuration



16-Pin SOIC
K-6

Decoding Table for CPU Clock

CPUS2	CPUS1	CPUS0	CPUCLK (MHz)
0	0	0	Off+14M off
0	0	1	80.00
0	1	0	25.00
0	1	1	66.66
1	0	0	20.00
1	0	1	50.00
1	1	0	33.33
1	1	1	4.00

ICS9134 Option

KEYBOARD CLOCK	-06	-07
KBOUT	16 MHz	12 MHz

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	CPUS2	I	Select 2 for 2XCPU and CPU frequencies. See Table above.
2	X2	O	Crystal connection. Connect to 32.768 kHz crystal.
3	X1	I	Crystal connection. Connect to 32.768 kHz crystal.
4	VDD32	P	Separate power supply connection for 32.768 kHz clock. Will operate to 2.0V.
5	VDD	P	Connect to +3.3V or +5V.
6	GND	P	Connect to ground.
7	24M	O	24 MHz floppy (or super I/O) clock output.
8	32K	O	32.768 kHz square wave clock output.
9	KBOUT	O	Keyboard clock output, fixed 16 MHz (-06) or 12 MHz (-07).
10	PD24+KBD*	I	Power-down 24M+keyboard. Shuts off both clock outputs, pins 7 & 9 when low.
11	14.3M	O	14.318 MHz system clock output.
12	GND	P	Connect to ground.
13	VDD	P	Connect to +3.3V or +5V.
14	CPUCLK	O	CPUCLK output. See Table above.
15	CPUS0	I	Select 0 for 2XCPU and CPU frequencies. See Table above.
16	CPUS1	I	Select 1 for 2XCPU and CPU frequencies. See Table above.

Absolute Maximum Ratings

VDD referenced to GND 7V
Operating temperature under bias . . . . 0°C to 70°C
Storage temperature . . . . -40°C to +150°C
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V
Power dissipation . . . . 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} = +3.0 to 3.7V, T_A=0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.2V_{DD}	V
Input High Voltage	V_{IH}		0.7V_{DD}	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-	-7	-15	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-2	-	2	µA
Output Low Voltage	V_{OL}	I_{OL}=6mA, Note 1	-	-	0.1	V
Output High Voltage	V_{OH}	I_{OH}=-4mA, Note 1	0.85V_{DD}	0.9V_{DD}	-	V
Output Low Current	I_{OL}	V_{OL}=0.2V_{DD}, Note 1	15	24	-	mA
Output High Current	I_{OH}	V_{OH}=0.7V_{DD}, Note 1	-	-13	-8	mA
Supply Current	I_{CC}	No load @ 33 MHz	-	9	17	mA
Supply Current	I_{CC}	No load @ 66.6 MHz	-	12	24	mA
V_{DD}32 Supply Current	I_{DD}32	No load	-	4.6	12	µA
Pull-up Resistor Value	R_{pu}	Note 1	370	530	650	k ohm
AC Characteristics						
Rise Time 0.8 to 2.0V	t_r	15pf load, Note 1	-	1.5	2	ns
Fall Time 2.0 to 0.8V	t_f	15 pf load, Note 1	-	1.5	2	ns
Rise to 20% to 80%	t_r	15pf load, Note 1	2	2.5	3.5	ns
Fall Time 80% to 20%	t_f	15pf load, Note 1	2	2.5	3.5	ns
Duty Cycle	d_t	15pf load, Note 1	40	50	55	%
Jitter, One Sigma	t_{jis}	As compared with clock period. Note 1	-	1	2	%
Jitter, Absolute	t_{jab}		-	2	5.5	%
Input Frequency	f_i	Note 1	25	32.768	40	kHz
Power-up Time	t_{pu}	Off to 33.3 MHz, Note 1	-	4	8	ms
Transition Time	t_{ft}	4 to 66.6 MHz, Note 1	-	-	4.8	ms

NOTE 1: Parameter guaranteed by design and characterization. Not 100% tested in production.

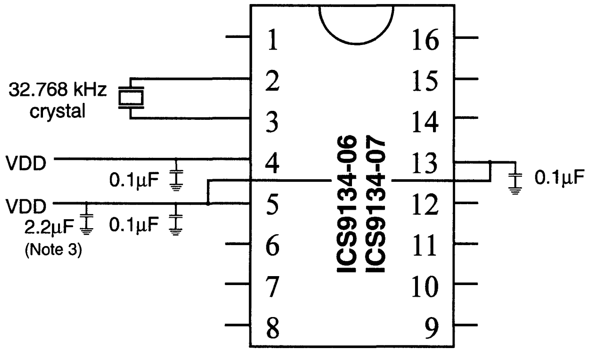
Electrical Characteristics

V_{DD} = +5V±10%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-	-10	-22	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-2	-	2	µA
Output Low Voltage	V_{OL}	I_{OL}=10mA, Note 1	-	0.15	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-30mA, Note 1	2.4	3.7	-	V
Output Low Current	I_{OL}	V_{OL}=0.8V, Note 1	25	45	-	mA
Output High Current	I_{OH}	V_{OH}=2.0V, Note 1	-	-58	-35	mA
Supply Current	I_{CC}	No load @ 33 MHz		15	28	mA
Supply Current	I_{CC}	No load @ 80 MHz	-	22	35	mA
V_{DD}32 Supply Current	$I_{DD}32$	No load	-	7.5	20	µA
Pull-up Resistor Value	R_{pu}	Note 1	380	550	680	k ohm
AC Characteristics						
Rise Time 0.8 to 2.0V	t_r	15pf load, Note 1	-	1	1.5	ns
Fall Time 2.0 to 0.8V	t_f	15 pf load, Note 1	-	1	1.5	ns
Rise to 20% to 80%	t_r	15pf load, Note 1	-	2	3	ns
Fall Time 80% to 20%	t_f	15pf load, Note 1	-	2	3	ns
Duty Cycle	d_t	15pf load, Note 1	48	52	58	%
Jitter, One Sigma	t_{jis}	As compared with clock period. Note 1	-	1	2	%
Jitter, Absolute	t_{jab}		-	2	5	%
Input Frequency	f_i	Note 1	25	32.768	40	kHz
Power-up Time	t_{pu}	Off to 80 MHz, Note 1	-	7	14	ms
Transition Time	t_{ft}	4 to 80 MHz, Note 1	-	-	5	ms

NOTE 1: Parameter guaranteed by design and characterization. Not 100% tested in production.

Recommended External Circuit



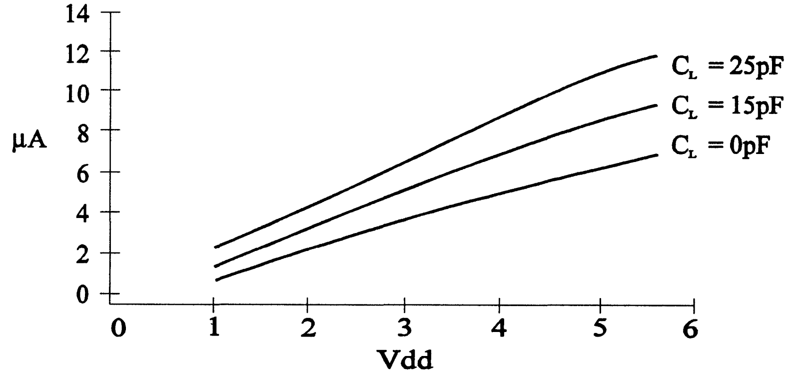
Notes:

1) The external components shown should be placed as close to the device as possible.

2) Pins 5 and 13 should be connected together externally. One decoupling capacitor may suffice for both pins.

3) May be part of system decoupling.

32 kHz Supply Current



Ordering Information

ICS9134-06M or ICS9134-07M

Example:

ICS XXXX-PPP M

Package Type
M=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated Circuit Systems, Inc.

AV9154A

Low-Cost 16-Pin Frequency Generator

General Description

The **AV9154A** is a 0.8µ version of the industry leading AV9154. Like the AV9154, the **AV9154A** is a low-cost frequency generator designed for general purpose PC and disk drive applications. However, because the **AV9154A** uses 0.8µ technology and the latest phase-locked loop architecture, it offers performance advantages that enable the device to be sold into Pentium™ systems.

The **AV9154A** guarantees a 45/55 duty cycle over all frequencies. In addition, a worst case jitter of ±250ps is specified at Pentium frequencies.

The CPU clock offers the unique feature of smooth, glitch-free transitions from one frequency to the next, making this the ideal device to use when slowing the CPU speed. The **AV9154A** makes a gradual transition between frequencies so that it obeys the Intel cycle-to-cycle timing specifications for 486 and Pentium systems.

The **AV9154A**-42 and **AV9154A**-43 devices offer features specifically for green PCs. The **AV9154A**-42 and -43 have a single pin that, when pulled low, will smoothly slow the 2XCPU clock to 8 MHz. This is ideal for dynamic DX microprocessors. The **AV9154A**-43 not only has the slow clock feature, but also offers a glitch-free stop clock for static SX microprocessors. The $\overline{\text{STOPCLK}}$ pin, when pulled low, enables the 2XCPU clock to go low only after completing its last full cycle. The clock continues to run internally, and will be output again on the first full cycle immediately following stop clock disable.

The simultaneous 2X and 1X CPU clocks offer controlled skew to within 500ps of each other (-42 only).

ICS has been shipping motherboard frequency generators since April 1990, and is the leader in the area of multiple output clocks on a single chip. Consult ICS for all your clock generation needs.

Features

- Compatible with 386, 486 and Pentium CPUs
- 45/55 Duty cycle
- Runs up to 66 MHz at 3.3V
- Single pin can slow clock to 8 MHz (on -42 and -43)
- Single pin can stop the CPU clock glitch-free (on -43)
- Very low jitter, ±250ps for Pentium frequencies
- 1X and 2X CPU clocks skew controlled to ±250ps (-42 only)
- Smooth transitions between all CPU frequencies
- Slow frequency ramp at power-on avoids CPU lock-up
- 16-pin PDIP or 150 mil skinny SOIC packages
- 0.8µ CMOS technology

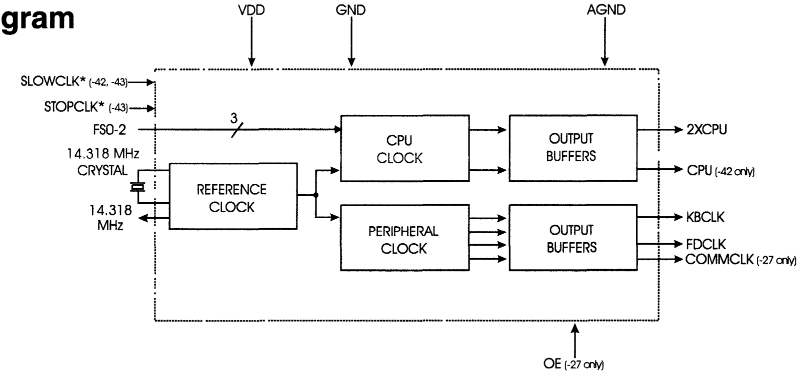
Applications

Computer motherboards: The **AV9154A** replaces crystals and oscillators, saving board space, component cost, part count and inventory costs. It produces a switchable CPU clock and up to four fixed clocks to drive floppy disk, communications, super I/O, Bus, and/or keyboard devices. The small package and 3.3V operation is perfect for handheld computers.

For specific applications of **AV9154A** devices, consult the following table:

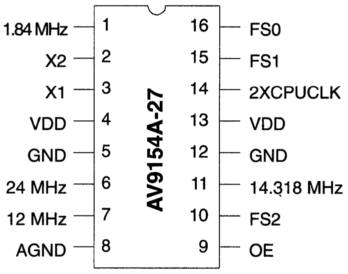
DEVICE	APPLICATION
AV9154A-27	Pentium and 486 systems
AV9154A-42	Pentium and 486 systems
	Dynamic green PC systems
AV9154A-43	Pentium and 486 systems
	Dynamic or static green PC systems

Block Diagram

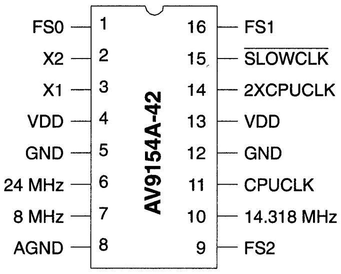


AV9154ARevB092894

Pin Configuration



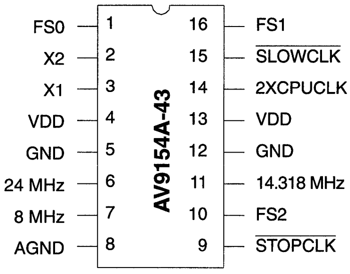
16-Pin PDIP or SOIC
AV9154A-27
K-4, K-6



16-Pin PDIP or SOIC
AV9154A-42
K-4, K-6

Description of new pin:

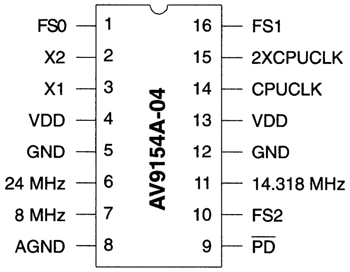
$\overline{\text{SLOWCLK}}$ forces 2XCPUCLK output to ramp smoothly to 8 MHz and CPUCLK output to 4 MHz when pulled low.



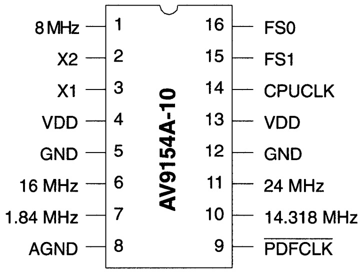
16-Pin PDIP or SOIC
AV9154A-43
K-4, K-6

Description of new pins:

$\overline{\text{SLOWCLK}}$ forces 2XCPUCLK output to ramp smoothly to 8 MHz when pulled low. $\overline{\text{STOPCLK}}$ provides glitch-free stop of the 2XCPUCLK output when pulled low. When raised back high, the 2XCPUCLK output clock resumes full speed operation (no clock frequency ramp up since the internal VCO is not stopped).

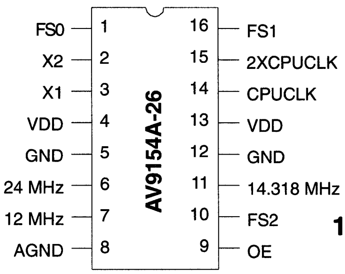


16-Pin PDIP or SOIC
AV9154A-04
K-4, K-6



* Active Low

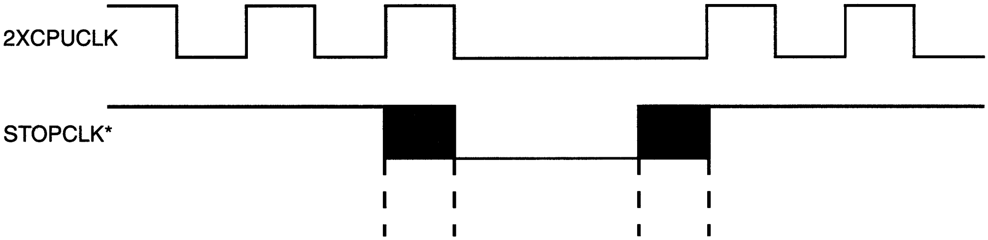
16-Pin PDIP or SOIC
AV9154A-10
K-4, K-6



16-Pin PDIP or SOIC
AV9154A-26
K-4, K-6

Stop Clock Feature

The **ICS9154A**-43 incorporates a unique stop clock feature compatible with static logic processors. When the stop clock pin goes low, the 2XCPUCLK will go low after the next occurring falling edge. When STOPCLK again goes high, 2XCPUCLK resumes on the next rising edge of the internal clock. This feature enables fast, glitch-free starts and stops of the 2XCPUCLK and is guaranteed that the CPU does not receive any short period clocks.



Pin Descriptions

(Frequencies based on 14.318 MHz input)

PIN NUMBER						PIN NAME	TYPE	DESCRIPTION
-4	-10	-26	-27	-42	-43			
4	4	4	4	4	4	VDD	P	Digital power (+3.3 or +5V)
13	13	13	13	13	13	VDD	P	Digital power (+3.3 or +5V)
5	5	5	5	5	5	GND	P	Digital ground
12	12	12	12	12	12	GDD	P	Digital ground
8	8	8	8	8	8	AGND	P	Analog ground
1	16	1	16	1	1	FS0	I	Frequency select 0 for CPU clock (has internal pull-up)*
16	15	16	15	16	16	FS1	I	Frequency select 1 for CPU clock (has internal pull-up)*
10	-	10	10	9	10	FS2	I	Frequency select 2 for CPU clock (has internal pull-up)*
-	-	9	9	-	-	OE	I	Tristates outputs when low (has internal pull-up)*
-	-	-	-	15	15	$\overline{\text{SLOWCLK}}$	I	Slows 2XCPU clock to 8 MHz (active low) (has internal pull-up)
-	-	-	-	-	9	$\overline{\text{STOPCLK}}$	I	Stops 2XCPU clock glitch-free (active low) (has internal pull-up)
3	3	3	3	3	3	X1	I	Crystal In
2	2	2	2	2	2	X2	O	Crystal Out
11	10	11	11	10	11	14.318 MHz	O	14.318 MHz reference clock output
-	7		1	-	-	1.84 MHz	O	1.84 MHz (comm) clock output
6	11	6	6	6	6	24 MHz	O	24 MHz (floppy disk) clock output
-	6	-	-	-	-	16 MHz	O	16 MHz clock output
-	-	7	7	-	-	12 MHz	O	12 MHz keyboard clock output
7	1	-	-	7	7	8 MHz	O	8 MHz keyboard clock output
14	14	14	-	11	-	CPUCLK	O	CPU clock output
15	-	15	14	14	14	2XCPUCLK	O	2X CPU clock output
9	-	-	-	-	-	$\overline{\text{PD}}$	I	Power-Down All (active low) (has internal pull-up)
-	9	-	-	-	-	$\overline{\text{PDFCLK}}$	I	Power-Down Fixed Clock (1.84, 8, 16, 24) (active low)**

Internal Pull-up Resistors

* -04 and -10 have no pull-ups or frequency select pins
** -10 has no pull-up or Pin 9 PDFCLK

Clock Tables

(using 14.318 MHz input, all frequencies in MHz)

FS2	FS1	FS0	-27 2XCPUCLK	-42		-43 2XCPUCLK
				2XCPUCLK	CPUCLK	
0	0	0	75*	16	8	16
0	0	1	32	40	20	40
0	1	0	60	33.33	16.67	33.33
0	1	1	40	25	12.50	25
1	0	0	50	60	30	60
1	0	1	66.66	20	10	20
1	1	0	80*	66.66	33.33	66.66
1	1	1	52	50	25	50

Actual Frequencies

(using 14.318 MHz input, all frequencies in MHz)

			-27	-42		-43
FS2	FS1	FS0	2CPUCLK	2XCPUCLK	CPUCLK	2XCPUCLK
0	0	0	75.17*	16.00	8.00	16.00
0	0	1	31.94	40.09	20.05	40.09
0	1	0	60.14	33.41	16.71	33.41
0	1	1	40.09	25.06	12.55	25.06
1	0	0	50.11	60.14	30.07	60.14
1	0	1	66.48	20.05	10.03	20.05
1	1	0	80.18*	66.48	33.24	66.48
1	1	1	51.90	50.11	25.06	50.11

* (5V only)

Fixed Clock Output Actual Frequencies

(using 14.318 MHz input, all frequencies in MHz)

14.318
1.84
24.0
12.0
8.0

*These selections will only operate at 5V.

Clock Tables in MHz for -04 and -10

(operating at 3V)

FS(3:0)	-04		-10
	2XCPU	CPU	CPUCLK
0	100*	50*	PDCPU
1	80*	40*	40
2	66.6*	33.3*	50
3	50	25	66.6*
4	40	20	-
5	32	16	-
6	24	12	-
7	16	8	-

Clock Table for AV9154A-26

FS(2:0)	2XCPU (MHz)	CPUCLK (MHz)
0	100.23*	50.11
1	80.18*	40.09
2	66.48*	33.24
3	50.11	25.06
4	40.09	20.05
5	32.22	16.11
6	24.23	12.12
7	15.75	7.88

Absolute Maximum Ratings

VDD referenced to GND	7V
Voltage on I/O pins referenced to GND	GND -0.5V to VDD +0.5V
Operating temperature under bias	0°C to +70°C
Power dissipation	0.5 Watts
Storage temperature	-40° to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = +3.3V±10%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}				0.2 V_{DD}	V
Input High Voltage	V_{IH}		0.7 V_{DD}			V
Input Low Current	I_{IL}	VIN=0V (pull-up pin)		2.5	7.0	μA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5.0		5.0	μA
Output Low Voltage	V_{OL}	I_{OL}=6mA		0.05 V_{DD}	0.1 V_{DD}	V
Output High Voltage[1]	V_{OH}	I_{OH}=-4mA	0.85 V_{DD}	0.94 VDD		V
Output Low Current[1]	I_{OL}	V_{OL}=0.2V_{DD}	15.0	24		mA
Output High Current[1]	I_{OH}	V_{OH}=0.7V_{DD}		-13	-8.0	mA
Supply Current	I_{DD}	Unloaded, 60 MHz		16	34	mA
Output Frequency Change over Supply and Temperature[1]	F_D	With respect to typical frequency		0.002	0.01	%
Short circuit current[1]	I_{SC}	Each output clock	20	30		mA
Input Capacitance[1]	C_I	Except X1, X2			10	pF
Load Capacitance[1]	C_L	Pins X1, X2		20		pF
Pull-up Resistor[1]	R_{pu}	at V_{DD} -0.5V		620	900	k ohm

NOTES:

1 Parameter is guaranteed by design and characterization.

Electrical Characteristics at 3.3V

V_{DD} = +3.3V±10%, T_A=0°C to 70°C unless otherwise stated

AC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Rise Time[1]	t_{ICr}				20	ns
Input Clock Fall Time[1]	t_{ICf}				20	ns
Rise time, 20% to 80% V_{DD}[1]	t_r	15pf load	-	2.2	3.5	ns
Fall time, 80% to 20% V_{DD}[1]	t_f	15pf load	-	1.2	2.5	ns
Duty cycle at 50% V_{DD}[1]	d_t	15pf load	40/60	48/52	60/40	%
Duty cycle, reference clocks[1]	d_t	15pf load	50/65	43/57	65/50	%
Jitter, one sigma, 20-66 MHz clocks[1]	t_{jls}	10,000 cycles		100	200	ps
Jitter, one sigma, clocks below 20 MHz[1]	t_{jls}	10,000 cycles		1.0	2.0	%
Jitter, absolute, 20-66 MHz clocks[1]	t_{jab}	10,000 cycles	-350		350	ps
Jitter, absolute, clocks below 20 MHz[1]	t_{jab}	10,000 cycles		1.5	4.0	%
Input Frequency[1]	f_{in}		2	14.318	32	MHz
Maximum Output Frequency[1]	f_{out}		70			MHz
Clock skew between CPU and 2XCPU outputs[1]	T_{sk}	AV9154A-42		220	500	ps
Power-up Time[1]	t_{tPO}	off to 50 MHz		6	12	ms
Frequency Transition Time[1]	t_{ft}	from 8 to 50 MHz		4.5	10	ms

NOTES:

1 Parameter is guaranteed by design and characterization, not subject to production testing.

Electrical Characteristics at 5V

V_{DD} = +5V±10%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD}=5V			0.8	V
Input High Voltage	V_{IH}	V_{DD}=5V	2.0			V
Input Low Current	I_{IL}	VIN=0V (pull-up pin)		6	15	μA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5		5	μA
Output Low Voltage	V_{OL}	I_{OL}=10mA		0.15	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-30mA	2.4	3.7		V
Output Low Current[1]	I_{OL}	V_{OL}=0.8	25	45		mA
Output High Current[1]	I_{OH}	V_{OH}=2.4V		-53	-35	mA
Supply Current	I_{DD}	Unloaded, 66 MHz		25	50	mA
Output Frequency Change over Supply and Temperature[1]	F_D	With respect to typical frequency		0.002	0.01	%
Short circuit current[1]	I_{SC}	Each output clock	25	40		mA
Input Capacitance[1]	C_I	Except X1, X2			10	pF
Load Capacitance[1]	C_L	Pins X1, X2		20		pF
Pull-up Resistor[1]	R_{pu}	A +V_{DD} -1V		400	700	k ohm

NOTES:

1 Parameter is guaranteed by design and characterization, not subject to production testing.

Electrical Characteristics at 5V

V_{DD} = +5V±10%, T_A=0°C to 70°C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Rise Time[1]	t_{ICr}				20	ns
Input Clock Fall Time[1]	t_{ICf}				20	ns
Output Rise time, 0.8 to 2.0V_1	t_r	15pf load	-	1.5	2	ns
Rise time, 20% to 80% V_{DD}[1]	t_r	15pf load	-	2.0	3	ns
Output Fall time, 2.0 to 0.8V[1]	t_f	15pf load	-	0.5	1.5	ns
Fall time, 80% to 20% V_{DD}[1]	t_f	15pf load	-	2.0	3.0	ns
Duty cycle at 1.4V[1]	d_t	15pf load, V_{DD}=5V±5%	45/55	48/52	55/45	%
Duty cycle, reference clocks[1]	d_t	15 pf load	40/65	43/57	65/40	%
Jitter, one sigma, 20 MHz-80 MHz clocks[1]	t_{jls}	10,000 cycles		70	140	ps
Jitter, one sigma, clocks below 20 MHz[1]	t_{jls}	10,000 cycles		0.8	2.0	%
Jitter, absolute, 20 MHz-80 MHz clocks[1]	t_{jab}	10,000 cycles	-250		250	ps
Jitter, absolute, clocks below 20 MHz[1]	t_{jab}	10,000 cycles		1.0	3.0	%
Input Frequency	f_{in}		2	14.318	32	MHz
Maximum Output Frequency[1]	f_{out}		140			MHz
Clock skew between CPU and 2XCPU outputs[1]	T_{sk}	AV9154A-42		140	400	ps
Power-up Time[1]	t_{tPO}	to 80 MHz		8	15	ms
Frequency Transition Time[1]	t_{ft}	from 8 to 66.66 MHz		6.5	12	ms

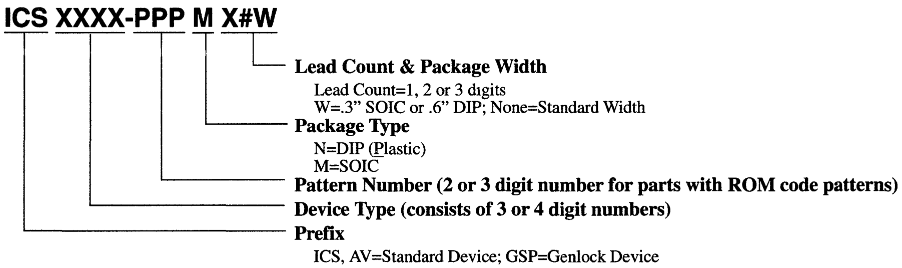
NOTES:

1 Parameter is guaranteed by design and characterization, not subject to production testing.

Ordering Information

AV9154A-42CN16	**AV9154A-26CN16**	**AV9154A-42CM16**	**AV9154A-26CM16**
AV9154A-43CN16	**AV9154A-10CN16**	**AV9154A-43CM16**	**AV9154A-10CM16**
AV9154A-27CN16	**AV9154A-04CN16**	**AV9154A-27CM16**	**AV9154A-04CM16**

Example:



ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
N=DIP (Plastic)
M=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

AV9154A-06
AV9154A-60

OPTi Notebook Frequency Generator

General Description

The **AV9154A-06/60** is a low cost frequency generator designed for general purpose PC and disk drive applications. Its CPU clocks provide all necessary frequencies for 286, 386 and 486 systems, including support for the latest speeds of processors. The standard devices use a 14.318 MHz crystal to generate the CPU and peripheral clocks for integrated desktop and notebook motherboards.

The **AV9154A-06** and **AV9154A-60** are specifically designed for use with OPTi core logic chip sets. The only noticeable difference between the two parts is in their CPU clock selection tables as shown on page three.

The **AV9154A-06** and **AV9154A-60** can operate at 5.0V±10% or 3.3V±10%, but the CPU frequencies are limited (see the asterisks on the selection tables on page three) during 3.3V operation. The parts have two power-down pins. One shuts off the CPU clock to a low state when the power-down pin is taken high, and the other turns off the 14.318 MHz output in the same manner.

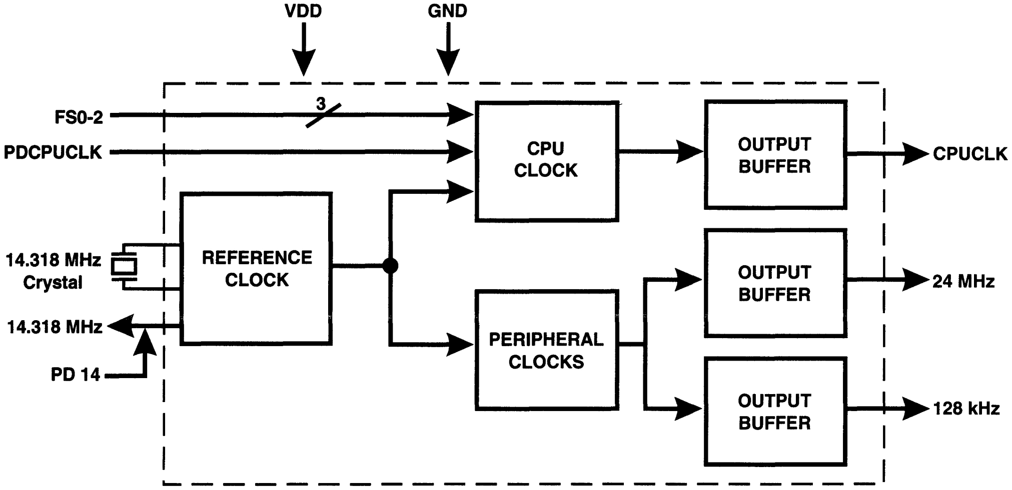
Features

- Compatible with 286, 386, and 486 CPUs
- Up to 66.6 MHz (-60) or 80 MHz (-06) CPU clocks
- All loop filter components internal
- 3V and 5V operation
- 16-pin 150 mil SOIC
- Power-down control of CPU clock

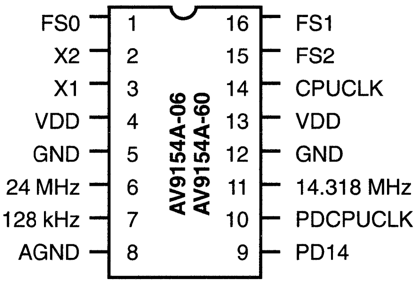
Applications

Computer Motherboards: The **AV9154A-06/60** replaces crystals and oscillators, saving board space, component cost, part count and inventory costs. It produces switchable CPU clock and up to four fixed clocks to drive floppy disk, communications, super I/O, bus and/or keyboard devices. The small package and 3V operation is perfect for handheld computers.

Block Diagram



Pin Configuration



16-Pin SOIC
K-6

Clock Tables for AV9154A-06/60

(in MHz)

FS(2:0)	-06 CPUCLK	-60 CPUCLK
0	16	8
1	20	16
2	25	20
3	33.33	25
4	40	33.33
5	50	40*
6	66.66	50*
7	80*	66.66*

Actual Output Frequencies

(in MHz)

FS(2:0)	-06 CPUCLK	-60 CPUCLK
0	16.11	8.182
1	20.05	16.11
2	25.06	20.05
3	33.24	25.06
4	40.09	33.24
5	50.11	40.09*
6	66.48	50.11*
7	80.18*	66.48*

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FS0	I	Frequency Select 0 for CPUCLK
2	X2	O	Crystal out. Connect a 14.318 MHz crystal to this pin.
3	X1	I	Crystal in. Connect a 14.318 MHz crystal to this pin.
4	VDD	P	Digital Power (+3.3V or +5V)
5	GND	P	Digital Ground
6	24 MHz	O	24 MHz clock output
7	128 kHz	O	128 kHz clock output
8	AGND	P	Analog Ground
9	PD14	I	Power-down 14.318 MHz output (active high)
10	PDCPUCLK	I	Power-down CPu clock (active high)
11	14.318 MHz	O	14.318 MHz reference clock output
12	GND	P	Digital Ground
13	VDD	P	Digital Power (+3.3V or +5V)
14	CPUCLK	O	CPU Clock output determined by status of FS0 - FS2
15	FS2	I	Frequency Select 2 for CPUCLK
16	FS1	I	Frequency Select 1 for CPUCLK

NOTE:
No internal pull-ups on any Inputs.

Absolute Maximum Ratings

VDD referenced to GND 7V
Operating temperature under bias . . . . 0°C to +70°C
Storage temperature . . . . -40°C to +150°C
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V
Power dissipation . . . . 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5V

V_{DD} =+5V±10%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD}=5V			0.8	V
Input High Voltage	V_{IH}	V_{DD}=5V	2.0			V
Input Low Current	I_{IL}	V_{IN}=0V			-5	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}			5	µA
Output Low Voltage	V_{OL}	I_{OL}=4mA			0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1mA	V_{DD}-.4V			V
Output High Voltage	V_{OH}	I_{OH}=-4mA	V_{DD}-.8V			V
Output High Voltage	V_{OH}	I_{OH}=-8mA	2.4			V
Supply Current	I_{DD}	No load[1]		25	40	mA
Output Frequency Change over Supply and Temperature	F_D	With respect to typical frequency		0.002	0.01	%
Short circuit current	I_{SC}	Each output clock	25	40		mA
Input Capacitance	C_i	Except X1, X2			10	pF
Load Capacitance	C_L	Pins X1, X2		20		pF
Supply Current, lowest	I_{DDSTBY}	When powered-down		20		mA

NOTE:

1 All clocks on AV9154A-06 or -60 running at highest possible frequencies.

Electrical Characteristics at 5V

V_{DD} =+5V±10%, T_A=0°C to 70°C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Rise Time	t_{ICr}				20	ns
Input Clock Fall Time	t_{ICf}				20	ns
Output Rise time, 0.8 to 2.0V	t_r	15pf load	-	1	2	ns
Rise time, 20% to 80% V_{DD}	t_r	15pf load	-	2	4	ns
Output Fall time, 2.0 to 0.8V	t_f	15pf load	-	1	2	ns
Fall time, 80% to 20% V_{DD}	t_f	15pf load	-	2	4	ns
Duty cycle	d_t	15pf load	40/60	48/52	60/40	%
Duty cycle, reference clock	d_t	15pf load	40/60	43/57	60/40	%
Duty cycle, CPU clock -06	d_t	15pf load	40/60	42/58	60/40	%
Jitter, one sigma	T_{jls}	As compared with clock period		±0.8	±2.5	%
Jitter, absolute	T_{jab}			±2	±5	%
Jitter, absolute	T_{jab}	16-80 MHz clocks			700	ps
Input Frequency	f_i			14.318		MHz
Frequency Transition time	t_{ft}	from 16 to 80 MHz		15	20	ms
Power-up time	t_{pu}	from off to 50 MHz		15		ms

NOTE:

1 All clocks on AV9154A-06 or -60 running at highest possible frequencies.

Electrical Characteristics at 3.3V

Operating V_{DD} =+3.0V to +3.7V, T_A=0°C to 70°C unless otherwise stated

DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.15V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-5	-	5	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5	-	5	µA
Output Low Voltage	V_{OL}	I_{OL}=8mA	-	-	0.1	V
Output High Voltage	V_{OH}	I_{OH}=-4mA	V_{DD}-.1V	-	-	V
Supply Current	I_{DD}	Note 1	-	15		mA
Output Frequency Change over Supply and Temperature	F_d	With respect to typical frequency	-	0.002	0.01	%
Input Capacitance	C_i	Except X1, X2			10	pF
Load Capacitance	C_L	Pins X1, X2		20		pF
Supply Current, lowest	I_{DDL}	When powered-down		14		mA
Short Circuit Current	I_{SC}			30		mA

Note 1: AV9154A with no load, with 14.318 MHz crystal input, and CPUCLK running at 33 MHz. Power supply current varies with frequency. Consult ICS for actual current at different frequencies.

Electrical Characteristics at 3.3V

(Operating V_{DD} =+3.0V to +3.7V, T_A=0°C to 70°C unless otherwise stated)

AC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Rise Time	t_{ICr}				20	ns
Input Clock Fall Time	t_{ICf}				20	ns
Rise time	t_r	15 pf load	-	-	4	ns
Fall time	t_f	15 pf load	-	-	4	ns
Duty cycle, fixed clocks	d_t	15 pf load	40/60	48/52	60/40	%
Duty cycle, CPU clock -06	d_t	15 pf load	40/60	42/58	60/40	%
Duty cycle, reference clock	d_t	15 pf load	40/60	43/57	60/40	%
Jitter, one sigma	T_{jls}	All frequencies		±0.5	±2	%
Jitter, absolute	T_{jabs}	All frequencies		±3	±5	%
Frequency Transition time	t_{ft}	from 8 to 33 MHz			20	ms
Power-up time	t_{pu}	from off to 50 MHz		15		ms
Output Frequency	f_o	Will operate up to 50 MHz for -06 version	2		33	MHz
Input Frequency	f_i			14.318		MHz

Note 1: AV9154A with no load, with 14.318 MHz crystal input, and CPUCLK running at 33 MHz. Power supply current varies with frequency. Consult ICS for actual current at different frequencies.

Ordering Information

AV9154A-06CS16 or AV9154A-60CS16

Example:

ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
S=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

AV9155A

Low Cost 20-Pin Frequency Generator

General Description

The **AV9155A** is a low cost frequency generator designed specifically for desktop and notebook PC applications. Its CPU clocks provide all necessary CPU frequencies for 286, 386 and 486 systems, including support for the latest speeds of processors. The device uses a 14.318 MHz crystal to generate the CU and all peripheral clocks for integrated desktop motherboards.

The dual 14.318 MHz clock outputs allows one output for the system and one to be the input to an ICS graphics frequency generator such as the AV9194.

The CPU clock offers the unique feature of smooth, glitch-free transitions from one frequency to the next, making this ideal device to use whenever slowing the CPU speed. The **AV9155A** makes a gradual transition between frequencies, so that it obeys the Intel cycle-to-cycle timing specification for 486 systems. The simultaneous 2X and 1X CPU clocks offer controlled skew to within 1.5ns (max) of each other.

ICS offers several versions of the **AV9155A**. The different devices are shown below:

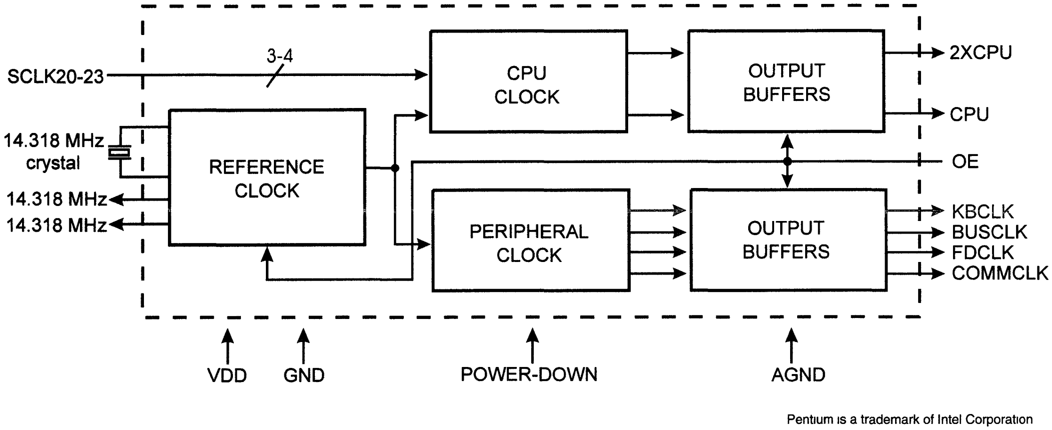
PART	DESCRIPTION
AV9155A-01	Motherboard clock generator with 16 MHz BUS CLK
AV9155A-02	Motherboard clock generator with 32 MHz BUS CLK
AV9155A-03	Special frequencies for both 386 and 486 CPUs
AV9155A-23	Includes Pentium™ frequencies
AV9155A-36	Features a special 40 MHz SCSI clock

Features

- Compatible with 286, 386, and 486 CPUs
- Supports turbo modes
- Generates communications clock, keyboard clock, floppy disk clock, system reference clock, bus clock and CPU clock
- Output enable tristates outputs
- Up to 100 MHz at 5V, 66.6 MHz at 3.3V
- 20-pin DIP or SOIC
- All loop filter components internal
- Skew-controlled 2X and 1X CPU clocks
- Power-down option

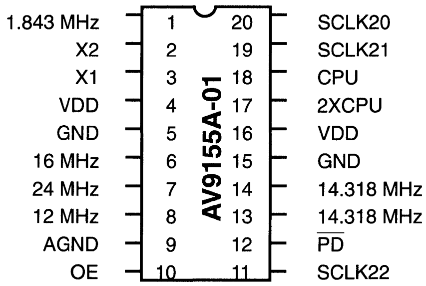
ICS has been shipping motherboard frequency generators since April 1990, and is the leader in the area of multiple output clocks on a single chip. The **AV9155A** is a third generation device, and uses ICS's patented analog CMOS phase-locked loop technology for low phase jitter. ICS offers a broad family of frequency generators for motherboards, graphics and other applications, including cost-effective versions with only one or two output clocks. Consult ICS for all of your clock generation needs.

Block Diagram

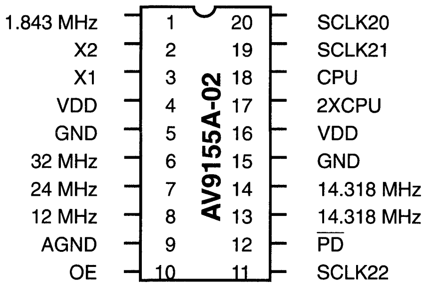


Pentium is a trademark of Intel Corporation

Pin Configuration



20-Pin DIP or SOIC
K-4, K-7



20-Pin DIP or SOIC
K-4, K-7

Pin Descriptions for AV9155A-01, -02

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	1.843 MHz	Output	1.84 MHz clock output
2	X2	Output	CRYSTAL connection
3	X1	Input	CRYSTAL connection
4	VDD	-	DIGITAL POWER SUPPLY (+5V)
5	GND	-	Digital GROUND
6	16 MHz/32 MHz	Output	16 MHz (AV9155-01) or 32 MHz (AV9155-02) clock output
7	24 MHz	Output	24 MHz floppy disk/combination I/O clock output
8	12 MHz	Output	12 MHz keyboard clock output
9	AGND	-	ANALOG GROUND (original version)
10	OE	Input	OUTPUT ENABLE. Tristates all outputs when low. (Has internal pull-up.)
11	SCLK22	Input	CPU CLOCK frequency SELECT #2. (Has internal pull-up.)
12	AVDD	-	ANALOG POWER SUPPLY (+5V)
12	$\overline{PD}$	Input	POWER-DOWN. Shuts off entire chip when low. (Has internal pull-up.)
13	14.318 MHz	Output	14.318 MHz reference clock output
14	14.318 MHz	Output	14.318 MHz reference clock output
15	GND	-	Digital GROUND
16	VDD	-	DIGITAL POWER SUPPLY (+5V)
17	2XCPU	Output	2X CPU clock output
18	CPU	Output	1X CPU clock output
19	SCLK21	Input	CPU CLOCK frequency SELECT #1. (Has internal pull-up.)
20	SCLK20	Input	CPU CLOCK frequency SELECT #0. (Has internal pull-up.)

Decoding and Clock Tables AV9155A-01

(using 14.318 MHz input. All frequencies in MHz.)

CLOCK#2 CPU and 2XCPU

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	8	4
0	0	1	16	8
0	1	0	32	16
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80*	40*
1	1	1	100*	50*

* 5V only

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	16	24	12

REFERENCE CLOCKS

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

Decoding and Clock Tables AV9155A-02

(using 14.318 MHz input. All frequencies in MHz.)

CLOCK#2 CPU and 2XCPU

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	8	4
0	0	1	16	8
0	1	0	32	16
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80*	40*
1	1	1	100*	50*

* 5V only

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	32	24	12

REFERENCE CLOCKS

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

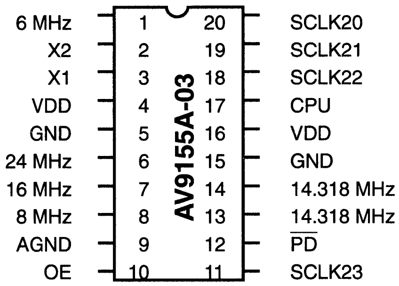
Frequency Transitions

A key feature of the **AV9155A** is its ability to provide smooth, glitch-free frequency transitions on the CPU and 2XCPU clocks when the frequency select pins are changed. These frequency transitions do not violate the Intel 486 specification of less than 0.1% frequency change per clock period.

Using an Input Clock as Reference

The **AV9155A** is designed to accept a 14.318 MHz crystal as the input reference. With some external changes, it is possible to use a crystal oscillator or clock input. Please see application note AAN04 for details on driving the **AV9155A** with a clock.

Pin Configuration



20-Pin DIP or SOIC
K-4, K-7

Pin Descriptions for AV9155A-03

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	6 MHz	Output	6 MHz clock output
2	X2	Output	CRYSTAL connection
3	X1	Input	CRYSTAL connection
4	VDD	-	DIGITAL POWER SUPPLY (+5V)
5	GND	-	Digital GROUND
6	24 MHz	Output	24 MHz (-03) floppy disk
7	16 MHz	Output	16 MHz (-03) bus clock output
8	8 MHz	Output	8 MHz (-23) keyboard clock output
9	AGND	-	ANALOG GROUND
10	OE	Input	OUTPUT ENABLE. Tristates all outputs when low. (Has internal pull-up.)
11	SCLK23	Input	CPU CLOCK frequency. (Has internal pull-up.)
12	$\overline{PD}$	Input	POWER-DOWN. Shuts off entire chip when low. (Has internal pull-up.)
13	14.318 MHz	Output	14.318 MHz reference clock output
14	14.318 MHz	Output	14.318 MHz reference clock output
15	GND	-	Digital GROUND
16	VDD	-	DIGITAL POWER SUPPLY (+5V)
17	CPU	Output	CPU clock output/2XCPU clock output
18	SCLK22	Input	CPU CLOCK frequency SELECT #2. (Has internal pull-up.)
19	SCLK21	Input	CPU CLOCK frequency SELECT #1. (Has internal pull-up.)
20	SCLK20	Input	CPU CLOCK frequency SELECT #0. (Has internal pull-up.)

Decoding and Clock Tables AV9155A-03

(using 14.318 MHz input. All frequencies in MHz.)

CLOCK#2 CPU

SCLK23 (Pin 11)	SCLK22 (Pin 18)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	CPU (Pin 17)
0	0	0	0	16
0	0	0	1	40
0	0	1	0	50
0	0	1	1	80*
0	1	0	0	66.66
0	1	0	1	100*
0	1	1	0	8
0	1	1	1	4
1	0	0	0	8
1	0	0	1	20
1	0	1	0	25
1	0	1	1	40
1	1	0	0	33.3
1	1	0	1	50
1	1	1	0	4
1	1	1	1	2

486

386

* 5V only

Smooth, glitch-free frequency transitions are guaranteed if the state of SCLK23 (pin 11) is not changed (smooth transitions are guaranteed in either the top or bottom half of the frequency decode table).

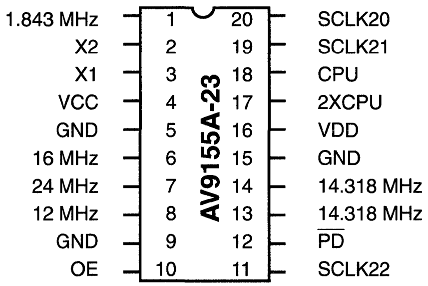
PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 7)	FDCLK (Pin 6)	KBCLK (Pin 8)
6 MHz	16 MHz	24 MHz	8 MHz

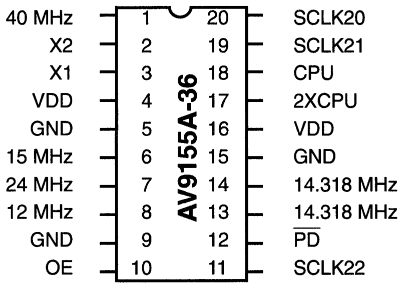
REFERENCE CLOCKS

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

Pin Configuration



20-Pin DIP or SOIC
K-4, K-7



20-Pin DIP or SOIC
K-4, K-7

Pin Descriptions for AV9155-23, -36

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	1.843/40 MHz	Output	1.84 MHz 40 MHz SCSI clock output
2	X2	Output	CRYSTAL connection
3	X1	Input	CRYSTAL connection
4	VDD	-	DIGITAL POWER SUPPLY (+5V)
5	GND	-	Digital GROUND
6	16 MHz/15 MHz	Output	16 MHz/15 MHz clock output
7	24 MHz	Output	24 MHz floppy disk/combination I/O clock output
8	12 MHz	Output	12 MHz keyboard clock output
9	AGND	-	ANALOG GROUND (original version)
10	OE	Input	OUTPUT ENABLE. Tristates all outputs when low. (Has internal pull-up.)
11	SCLK22	Input	CPU CLOCK frequency SELECT #2. (-23 has internal pull-up.)
12	AVDD	-	ANALOG POWER SUPPLY (+5V)
12	$\overline{\text{PD}}$	Input	POWER-DOWN. Shuts off entire chip when low. (Has internal pull-up.)
13	14.318 MHz	Output	14.318 MHz reference clock output
14	14.318 MHz	Output	14.318 MHz reference clock output
15	GND	-	Digital GROUND
16	VDD	-	DIGITAL POWER SUPPLY (+5V)
17	2XCPU	Output	2X CPU clock output
18	CPU	Output	1X CPU clock output
19	SCLK21	Input	CPU CLOCK frequency SELECT #1. (-23 has internal pull-up.)
20	SCLK20	Input	CPU CLOCK frequency SELECT #0. (-23 has internal pull-up.)

Decoding and Clock Tables AV9155A-23

(using 14.318 MHz input. All frequencies in MHz.)

CLOCK#2 CPU and 2XCPU

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	75*	37.5*
0	0	1	32	16
0	1	0	60	30
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80*	40*
1	1	1	52	26

* 5V only

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	16	24	12

REFERENCE CLOCKS

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

Decoding and Clock Tables AV9155A-36

(using 14.318 MHz input. All frequencies in MHz.)

CLOCK#2 CPU and 2XCPU

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	8	4
0	0	1	16	8
0	1	0	60	30
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80*	40*
1	1	1	100*	50*

* 5V only

PERIPHERAL CLOCKS

SCSICLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
40	15	24	12

REFERENCE CLOCKS

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

Absolute Maximum Ratings

AVDD, VDD referenced to GND	7V
Operating temperature under bias	0°C to +70°C
Storage temperature	-40°C to +150°C
Voltage on I/O pins referenced to GND	GND -0.5V to VDD +0.5V
Power dissipation	0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} =+5V±10%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD}=5V			0.8	V
Input High Voltage	V_{IH}	V_{DD}=5V	2.0			V
Input Low Current	I_{IL}	V_{IN}=0V			-5	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}			5	µA
Output Low Voltage	V_{OL}	I_{OL}=4mA			0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1mA, V_{DD}=5.0V	V_{DD}-.4V			V
Output High Voltage	V_{OH}	I_{OH}=-4mA, V_{DD}=5.0V	V_{DD}-.8V			V
Output High Voltage	V_{OH}	I_{OH}=-8mA	2.4			V
Supply Current	I_{CC}	No load[1]		40		mA
Supply Current, Power-Down	I_{CDSTBY}	No load		35	70	µA
Output Frequency Change over Supply and Temperature	F_D	With respect to typical frequency		0.002	0.01	%
Short circuit current	I_{SC}	Each output clock	25	40		mA
Pull-up resistor value	R_{PU}	Pin 10 (and 12, U only)		680		kΩ
Input Capacitance	C_i	Except X1, X2			10	pF
Load Capacitance	C_L	Pins X1, X2		20		pF
AC Characteristics						
Output Rise time, 0.8 to 2.0V	t_r	25pf load	-	1	2	ns
Rise time, 20% to 80% V_{DD}	t_r	25pf load	-	2	4	ns
Output Fall time, 2.0 to 0.8V	t_f	25pf load	-	1	2	ns
Fall time, 80% to 20% V_{DD}	t_f	25pf load	-	2	4	ns
Duty cycle	d_t	25pf load	40/60	48/52	60/40	%
Duty cycle, reference clocks	d_t	25pf load	40/60	43/57	60/40	%
Jitter, one sigma	f_{j1s}	As compared with clock period		0.8	2.5	%
Jitter, absolute	t_{jab}	16-100 MHz clocks		2	5	%
Jitter, absolute	t_{jab}				700	ps
Input Frequency	f_i			14.318		MHz
Clock skew between CPU and 2XCPU outputs	T_{sk}	(1.0ns max on U parts)		1	1.5	ns
Frequency Transition time	t_{ft}	From 8 to 100 MHz		15	20	ms

Notes:

1. All clocks on AV9155A-01 running at highest possible frequencies. Power supply current can change substantially with different mask configurations. Consult ICS.

Actual Output Frequencies

(using 14.318 MHz input. All frequencies in MHz.)

AV9155A-01 and AV9155-02

CLOCK#2 CPU and 2XCPU

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	7.50	3.75
0	0	1	15.51	7.76
0	1	0	32.22	16.11
0	1	1	40.09	20.05
1	0	0	50.11	25.06
1	0	1	66.82	33.41
1	1	0	80.18*	40.09*
1	1	1	100.23*	50.11*

* 5V only

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.846	32.01 or 16.00	24.00	12.00

AV9155A-23

CPU CLOCK

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	75.170*	37.585*
0	0	1	31.940	15.970
0	1	0	60.136	30.068
0	1	1	40.090	20.045
1	0	0	50.113	25.057
1	0	1	66.476	33.238
1	1	0	80.181*	40.091*
1	1	1	51.903*	25.952

* 5V only

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.846	16.00	24.00	12.00

AV9155A-03

CLOCK#2 CPU

SCLK23 (Pin 11)	SCLK22 (Pin 18)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	CPU (Pin 17)
0	0	0	0	15.51
0	0	0	1	40.09
0	0	1	0	50.11
0	0	1	1	80.18*
0	1	0	0	66.82
0	1	0	1	100.23*
0	1	1	0	7.58
0	1	1	1	4.30
1	0	0	0	7.76
1	0	0	1	20.05
1	0	1	0	25.06
1	0	1	1	40.09
1	1	0	0	33.41
1	1	0	1	50.11
1	1	1	0	3.79
1	1	1	1	2.15

* 5V only

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 7)	FDCLK (Pin 6)	KBCLK (Pin 8)
6.00	16.00	24.00	8.00

AV9155A-36

CPU CLOCK

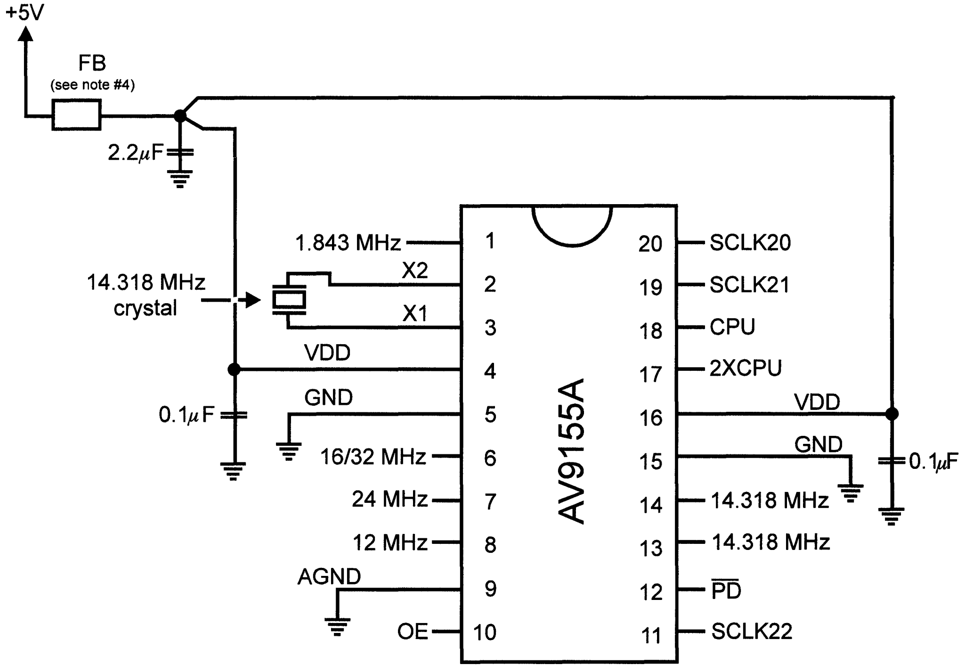
SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	8.054	4.027
0	0	1	16.002	8.001
0	1	0	59.875	29.936
0	1	1	39.886	19.943
1	0	0	50.113	25.057
1	0	1	66.476	33.238
1	1	0	80.181*	40.091*
1	1	1	100.226*	50.113*

* 5V only

PERIPHERAL CLOCKS

SCSICLK (Pin 1)	BUSCLK (Pin 7)	FDCLK (Pin 6)	KBCLK (Pin 8)
40.00	15.00	24.00	12.00

AV9155A Recommended External Circuit



NOTES:

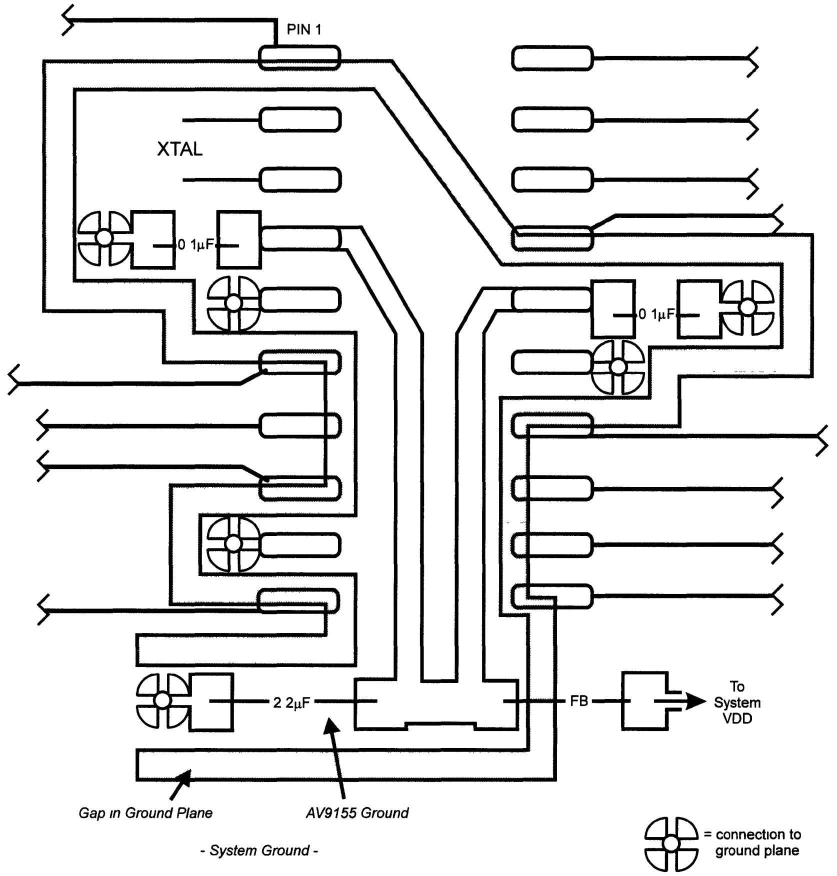
1. ICS recommends the use of an isolated ground plane for the **AV9155A**. All grounds shown on this drawing should be connected to this ground plane. This ground plane should be connected to the system ground plane at a single point. Please refer to **AV9155A** Board Layout Diagram.

2. A single power supply connection for all VDD lines at the 2.2µF decoupling capacitor is recommended to reduce interaction of analog and digital circuits. The 0.1µF decoupling capacitors should be located as close to each VDD pin as possible.

3. A 33Ω series termination resistor should be used on any clock output which drives more than one load or drives a long trace (more than about two inches), especially when using high frequencies (>50 MHz). This termination resistor is put in series with the clock output line close to the clock output. It helps improve jitter performance and reduce EMI by damping standing waves caused by impedance mismatches in the output clock circuit trace.

4. The ferrite bead does not enhance the performance of the **AV9155A**, but will reduce EMI radiation from the VDD line.

AV9155A Recommended Board Layout



This is the recommended layout for the **AV9155A** to maximize clock performance. Shown are the power and ground connections, the ground plane, and the input/output traces.

Use of the isolated ground plane and power connection, as shown, will prevent stray high frequency ground and system noise from propagating through the device. When compared to using the system ground and power planes, this technique will minimize output clock jitter. The isolated ground plane should be connected to the system ground plane at one point, near the 2.2µF decoupling cap. For lowest jitter performance, this isolated ground plane should be kept away from clock output pins and traces. Keeping the isolated ground plane area as small as possible will minimize EMI radiation. Use a sufficient gap between the isolated ground plane and system ground plane to prevent AC coupling. The ferrite bead in the VDD line optional, but will help reduce EMI.

The traces to distribute the output clocks should be over a system ground or power supply plane. The trace width should be about two times the thickness of the PC board between the trace and the underlying plane. These guidelines help minimize clock jitter and EMI radiation. The traces to distribute power should be as wide as possible.

Ordering Information

AV9155A-01CN20, AV9155A-02CN20, AV9155A-03CN20, AV9155A-23CN20, AV9155A-36CN20

Example:

ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
N=DIP (Plastic) T&R=Tape and Reel

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

AV9155A-01CW20, AV9155A-02CM20, AV9155A-03CM20, AV9155A-23CM20, AV9155A-36CM20

Example:

ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
W=SOIC T&R=Tape and Reel

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

NOTES:
Tape and reel packaging should be ordered with the suffix T&R. For instance, if the -01 in DIP and tape & reel is required, order the part as AV9155-01CN20T&R.

ICS9158

Integrated Buffer and Motherboard Frequency Generator

General Description

The **ICS9158** is a low cost frequency generator designed specifically for desktop and notebook PC applications. Eight high drive, skew-controlled copies of the CPU clock are available, eliminating the need for an external buffer.

Each high drive (50mA) output is capable of driving a 30pf load and has a typical duty cycle of 50/50. The CPU clock outputs are skew-controlled to within ±250ps. The CPU clocks provide all necessary frequencies for 286, 386, 486 and Pentium systems, including support for the latest speeds of processors.

The CPU clock offers the unique feature of smooth, glitch-free transitions from one frequency to the next, making this the ideal device to use whenever slowing the CPU speeds. The **ICS9158** makes a gradual transition between frequencies so that it meets the Intel cycle-to-cycle timing specification for 486 systems.

ICS has been shipping Motherboard Frequency Generators since April 1990, and is the leader in the area of multiple output clocks on a single chip. The **ICS9158** is a third generation device, and uses ICS's patented analog CMOS Phase-Locked Loop technology for low phase jitter. ICS offers a broad family of frequency generators for motherboards, graphics and other applications, including cost effective versions with only one or two output clocks. Consult ICS for all of your clock generation needs.

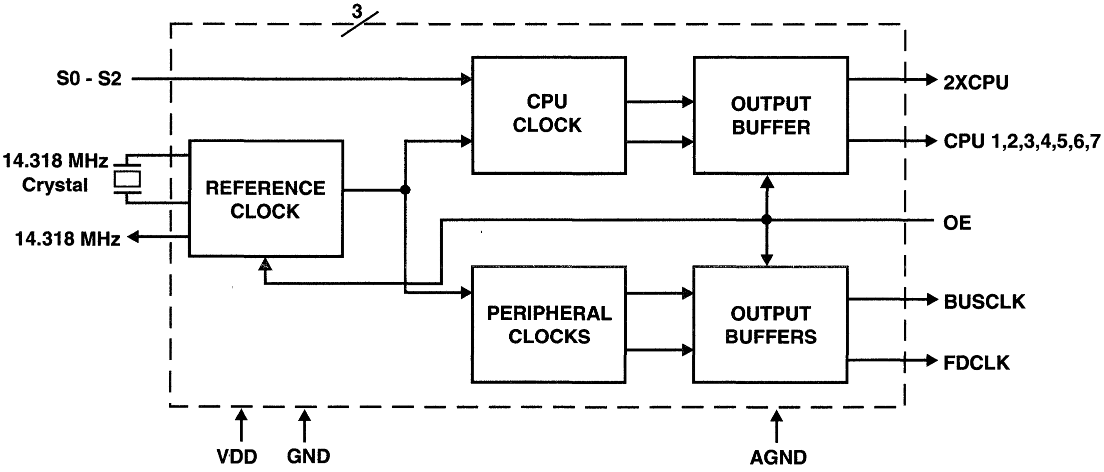
Features

- Eight skew-free, high drive CPU clock outputs
- Up to 100 MHz output at 5V
- ±250ps skew between CPU and 2XCPU outputs
- Outputs can drive up to 30pf load
- 50mA output drivers
- Typical 50/50 duty cycle
- Compatible with 486 and Pentium CPUs
- Glitch-free start and stop clock option
- Optional power-down mode supports Energy Star ("green") PCs
- On-chip loop filter components
- Low power, high speed 0.8µ CMOS technology
- 24-pin PDIP or SOIC package

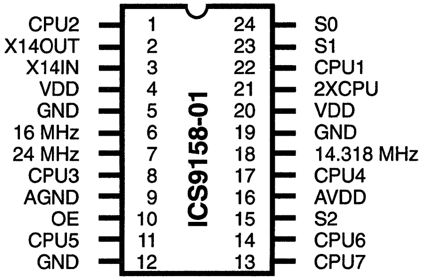
Clock Table (in MHz)

Clock	ICS9158-01
BUSCLK	16
FDCLK	24
14.318	14.318
CPUCLK	4,8,30,20,25,33.3,40, or 50
2XCPUCLK	8,16,60,40,50,66.6,80, or 100

Block Diagram



Pin Configuration



24-Pin PDIP or SOIC
K-5, K-7

Pin Descriptions for ICS9158-01

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	CPU2	Output	CPU clock output
2	X14OUT	-	Crystal connection
3	X14IN	-	Crystal connection
4	VDD	-	Digital POWER SUPPLY (+5V)
5	GND	-	Digital GROUND
6	16 MHz	Output	16 MHz clock output
7	24 MHz	Output	24 MHz floppy disk/combination I/O clock output
8	CPU3	Output	CPU clock output
9	AGND	-	ANALOG GROUND
10	OE	Input	OUTPUT ENABLE. Tristates all outputs when low.
11	CPU5	Output	CPU clock output
12	GND	-	Digital GROUND
13	CPU7	Output	CPU clock output
14	CPU6	Output	CPU clock output
15	S2	Input	CPU clock frequency select 2
16	AVDD	-	ANALOG power supply (+5V)
17	CPU4	Output	CPU clock output
18	14.318 MHz	Output	14.318 MHz clock output
19	GND	-	Digital GROUND
20	VDD	-	Digital POWER SUPPLY (+5V)
21	2XCPU	Output	2X CPU clock output
22	CPU1	Output	CPU clock output
23	S1	Input	CPU clock frequency select #1
24	S0	Input	CPU clock frequency select #0

Absolute Maximum Ratings

AVDD, VDD referenced to GND 7V
Operating temperature under bias . . . . 0°C to +70°C
Storage temperature . . . . -40°C to +150°C
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V
Power dissipation . . . . 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5V

V_{DD} = +5V±10%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Input Low Current	I_{IL}	V_{IN}=0V	-5		5	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5		5	µA
Output Low Voltage	V_{OL}	I_{OL}=20.0mA		0.25	0.4	V
Output High Voltage (Note 1)	V_{OH}	I_{OH}=-30mA	2.4	3.5		V
Output Low Current (Note 1)	I_{OL}	V_{OL}=0.8V	45	65		mA
Output High Current (Note 1)	I_{OH}	V_{OH}=2.0V		-55	-35	mA
Supply Current	I_{DD}	No load, 80 MHz		43	65	mA
Output Frequency Change over Supply and Temperature (Note 1)	F_D	With respect to typical frequency		0.002	0.01	%
Short circuit current (Note 1)	I_{SC}	Each output clock	25	56		mA
Pull-up resistor value (Note 1)	R_{PU}	Input pin		680		kΩ
Input Capacitance (Note 1)	C_i	Except X1, X2			8	pf
Load Capacitance (Note 1)	C_L	Pins X1, X2		20		pf

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics *(continued)*

V_{DD} = +5V±10%, T_A=0°C to 70°C unless otherwise stated

AC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Rise time, 0.8 to 2.0V (Note 1)	t_r	30pf load	-	1	2	ns
Rise time, 20% to 80% V_{DD} (Note 1)	t_r	30pf load	-	2.5	3	ns
Output Fall time, 2.0 to 0.8V (Note 1)	t_f	30pf load	-	0.5	1	ns
Fall time, 80% to 20% V_{DD} (Note 1)	t_f	30pf load	-	1.5	2	ns
Duty cycle (Note 1)	d_t	30pf load	40/60	48/52	60/40	%
Jitter, one sigma (Note 1)	t_{j1s}	As compared with clock period		0.5	2.0	%
Jitter, absolute	t_{jab}			2	5	%
Jitter, absolute	t_{jab}	16-100 MHz clocks			500	ps
Input Frequency	f_i			14.318		MHz
Clock skew between CPU and 2XCPU outputs	T_{sk}			100	250	ps
Frequency Transition time (Note 1)	t_{ft}	From 4 to 50 MHz		13	20	ms

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

ICS9158-01 CPU Clock Decoding Table

(using 14.318 MHz input. All frequencies in MHz)

CLOCK#2 CPU and 2XCPU

S2 (Pin 15)	S1 (Pin 23)	S0 (Pin 24)	2XCPU (Pin 21)	CPU
0	0	0	7.580	3.790
0	0	1	15.511	7.756
0	1	0	59.875	29.938
0	1	1	40.090	20.045
1	0	0	50.113	25.057
1	0	1	66.476	33.238
1	1	0	79.772*	39.886*
1	1	1	100.226*	50.113*

*5V only

Peripheral Clocks

BUSCLK (Pin 6)	FDCLK (Pin 7)
16.002	24.003

Reference Clock

REFCLK1 (Pin 18)
14.318

Frequency Transitions

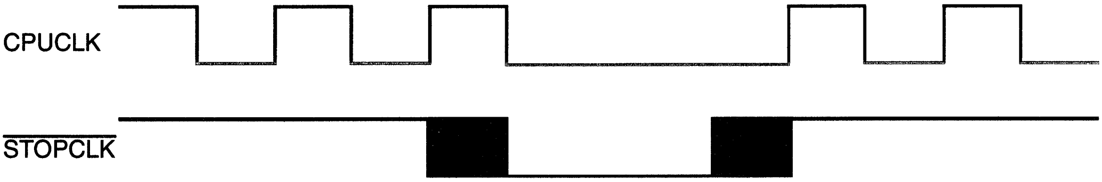
A key feature of the **ICS9158** is its ability to provide smooth, glitch-free frequency transitions on the CPU and 2XCPU clocks when the frequency select pins are changed. The frequency transition rate does not violate the Intel 486 or Pentium specification of less than 0.1% frequency change per clock period.

Using an Input Clock as a Reference

The **ICS9158** is designed to accept a 14.318 MHz crystal as the input reference. With some external changes, it is possible to use a crystal oscillator or other clock sources. Please see application note AAN04 for details on driving the **ICS9158** with a clock.

Stop Clock Feature (Optional Mask Version)

The **ICS9158** incorporates a unique stop clock feature compatible with static logic processors. When the stop clock pin goes low, the CPUCLK will go low after the next occurring falling edge. When STOPCLK again goes high, CPUCLK resumes on the next rising edge of the internal clock. This feature enables fast, glitch-free starts and stops of the CPUCLK and is useful in Energy Start motherboard applications.



Ordering Information

ICS9158-01N

Example:

ICS XXXX-PPP M

Package Type
N=DIP (Plastic)

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

ICS9158-01M

Example:

ICS XXXX-PPP M

Package Type

M=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS9159-02

Product Preview

Frequency Generator and Integrated Buffer for PENTIUM™

General Description

The **ICS9159-02** generates all clocks required for high speed RISC or CISC microprocessor systems such as 486, Pentium, PowerPC,™ etc. Four different reference frequency multiplying factors are externally selectable with smooth frequency transitions. These multiplying factors can be customized for specific applications. A test mode is provided to drive all clocks directly.

High drive BCLK outputs provide greater than 1V/ns slew rate into 30pf loads. PCLK outputs provide better than 1V/ns slew rate into 20pf loads while maintaining ±5% duty cycle.

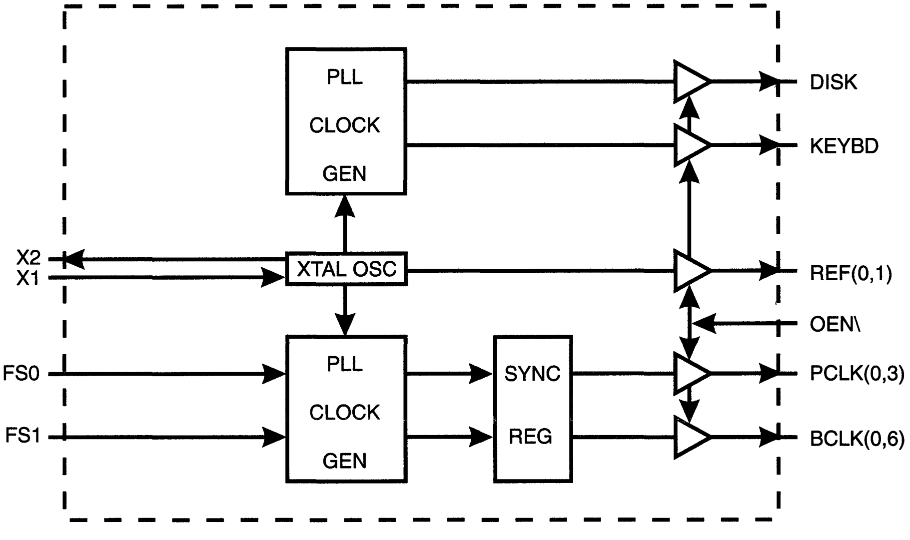
Features

- Generates up to four processor and six bus clocks, plus disk, keyboard and reference clocks
- Synchronous clocks skew matched to ±250ps
- Output frequency ranges to 100 MHz
- Test clock mode eases system design
- Selectable multiplying and processor/bus ratios
- Stop clock control stops clocks glitch-free
- Custom configurations available
- 3.0V - 5.5V supply range
- 28-pin SOIC package

Applications

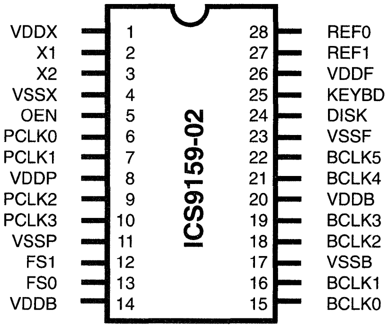
- Ideal for high-speed RISC or CISC systems such as 486, Pentium, PowerPC, etc.

Block Diagram



Pentium is a trademark of Intel Corporation
PowerPC is a trademark of Motorola Corporation

Pin Configuration



28-Pin SOIC
K-7

ICS9159-02 Functionality

FS1	FS0	*VCO	X1, REF (MHz)	PCLK(0,3) (MHz)
0	0	230/33x X1	14.31818	50
0	1	176/21x X1	14.31818	60
1	0	212/23x X1	14.31818	66
1	1	Test mode	TCLK	TCLK/2

*VCO range is limited from 60 - 200 MHz.

PCLK(0,3)	BCLK(0,5)	DISK	KEYBD
VCO/2	PCLK/2	24 MHz	12 MHz
TCLK/2	TCLK/4	TCLK/4	TCLK/8

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2	X1	IN	XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 10 - 30 MHz XTAL
3	X2	OUT	XTAL output which includes XTAL load capacitance.
1 4	VDDX VSSX	PWR	XTAL oscillator circuit power supplies.
6, 7, 9, 10	PCLK(0,3)	OUT	Processor clock outputs which are a multiple of the input reference frequency as shown in the table below. Duty cycle is 50/50±5% with a maximum frequency of 100 MHz. Custom multiplying configurations are available
8 11	VDDP VSSP	PWR	PCLK power supplies. VSSP and VDDP power PCLK(0,3) outputs and the internal PCLK PLL.
13, 12	FS(0,1)	IN	Frequency multiplier select pins See table below. These inputs have internal pull-up devices.
15, 16, 18 19, 21, 22	BCLK(0,5)	OUT	Bus clock outputs are fixed at ½ the PCLK frequency. In all cases, the duty cycle is 50/50±5%.
17 14, 20	VSSB VDDB	PWR	BCLK power supplies VSSB and VDDB power BCLK(0,5) outputs. Output levels can be customized by connecting VDDB to voltages less than VDDF
5	OEN	IN	OEN tristates all outputs when low. This input has an internal pull-up device.
24	DISK	OUT	The DISK controller clock is fixed at 12 MHz.
25	KEYBD	OUT	The KEYBD clock is fixed at 12 MHz.
23 26	VSSF VDDF	PWR	Fixed clock (DISK and KEYBD) output and PLL power supplies.
28, 27	REF(0,1)	OUT	REF is a buffered copy of the crystal oscillator or reference input clock, nominally 14.31818 MHz

Timing Specifications

3.3V ±5% or 5.0V ±5% VDD, 0-70°C, measured at 1.5V, Cload=20pf

PIN	JITTER cycle-cycle	SKEW to PCLK	SKEW to BCLK	SLEW, LOAD	DUTY CYCLE
PCLK(0,3)	<±200ps	<±250ps	<±750ps	>1.0V/ns, 20pf	<±5%
BCLK(0,5)	<±300ps	<±750ps	<±500ps	>1.0V/ns, 30pf	<±5%

Absolute Maximum Ratings

Supply voltage . . . . 7.0 V
Logic inputs . . . . GND -0.5V to V_{DD} +0.5V
Ambient operating temp . . . . 0 to +70°C
Storage temperature . . . . -65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3V

V_{DD} =3.0 - 3.7V

DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.2V_{DD}	V
Input High Voltage	V_{IH}		0.7V_{DD}	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-	10.5	28.0	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5.0	-	5.0	µA
Output Low Current	I_{OL}	V_{OL}=0.8V; for PCLKS & BCLKS	30.0	47.0	-	mA
Output High Current	I_{OH}	V_{OL}=2.0V; for PCLKS & BCLKS	-	-66.0	-42.0	mA
Output Low Current	I_{OL}	V_{OL}=0.8V; for fixed CLKs	25.0	38.0	-	mA
Output High Current	I_{OH}	VOL=2.0V; for fixed CLKs	-	-47.0	-30.0	mA
Output Low Voltage	V_{OL}	I_{OL}=15mA; for PCLKS & BCLKS	-	0.3	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-30mA; for PCLKS & BCLKS	2.4	2.8	-	V
Output Low Voltage	V_{OL}	I_{OL}=12.5mA; for fixed CLKs	-	0.3	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-20mA; for fixed CLKs	2.4	2.8	-	V
Supply Current	I_{CC}	@66.66 MHz; all outputs unloaded	-	55	110	mA

Electrical Characteristics at 3V

V_{DD} =3.0 - 3.7V

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time 0.8 to 2.0V	T_r	20pf load	-	1.5	3	ns
Fall Time 2.0 to 0.8V	T_f	20pf load	-	0.9	2	ns
Rise Time 20% to 80%	T_r	20pf load	-	2	4.5	ns
Fall Time 80% to 20%	T_f	20pf load	-	1.8	4.25	ns
Duty Cycle	D_t	20pf load	40	50	60	%
Jitter, One Sigma	T_{jis}	CPU & Bus Clocks; Load=20pf, FOUT>25 MHz	-	50	150	ps
Jitter, Absolute	T_{jab}	CPU & Bus Clocks; Load=20pf, FOUT>25 MHz	-250	-	250	ps
Jitter, One Sigma	T_{jis}	Fixed CLK; Load=20pf; Comp. to the period	-	1	3	%
Jitter, Absolute	T_{jab}	Fixed CLK; Load=20pf; Comp. to the period	-	2	5	%
Input Frequency	F_i		-	14.318	-	MHz
Clock Skew	T_{sk}	PCLK to PCLK; Load=20pf; @1.4V	-	50	250	ps
Clock Skew	T_{sk}	BCLK to BCLK; Load=20pf; @1.4V	-	90	500	ps
Clock Skew	T_{sk}	PCLK to BCLK; Load=20pf; @1.4V	1	2.6	5	ns

Ordering Information

ICS9159-02M

Example:

ICS XXXX-PPP M

Package Type
W=SOIC, SOP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS9160-03

Product Preview

Frequency Generator and Integrated Buffer for PowerPC™

General Description

The **ICS9160** generates all clocks required for high speed RISC microprocessor systems based on the PowerPC 603 and 604. Five different frequency multiplying factors are selectable and offer smooth frequency transitions. BCLK signals are synchronous to PCLK and operate at PCLK/2 for optimum synchronous PCI bus performance. The multiplying and ratio factors can be customed for specific applications.

Both individual and group glitch-free stop and start of the clock signals are provided, as well as a power-down mode to minimize power consumption. The individual stop and start is provided through a serial interface control.

A global output enable pin simplifies production board testing, and a test mode is available to aid in system design and diagnostics.

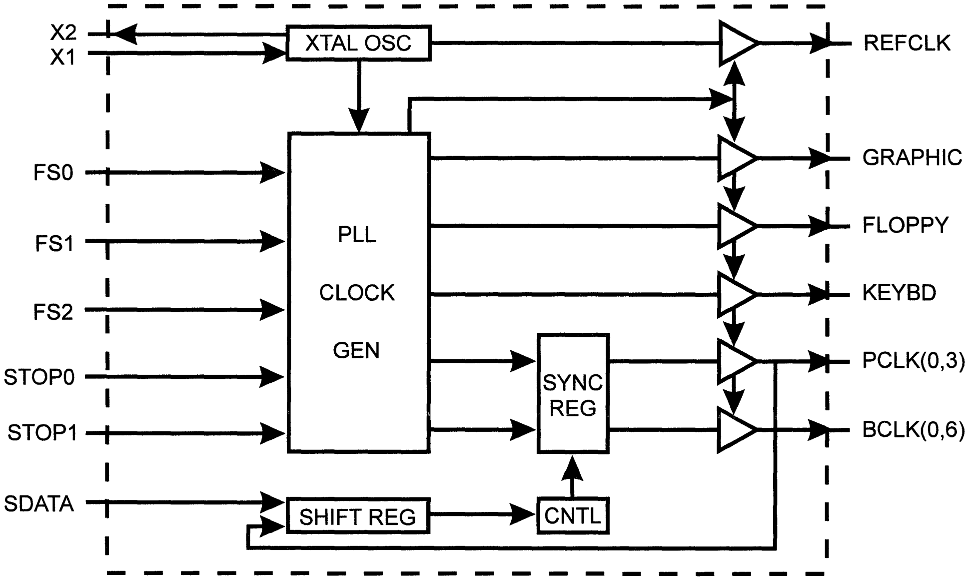
Features

- Generates four processor and seven synchronous bus clocks plus graphic, floppy, keyboard and reference clocks
- Selectable 33.3/50/60/66.6/80 MHz PCLKs
- ±150ps maximum PowerPC PLL in-band jitter
- All synchronous clocks skew matched to ±200ps
- Individual or group stop-clock control
- Power-down modes minimize standby current
- Custom configurations available
- 3.0V - 5.5 supply range
- 32-pin SOIC package

Applications

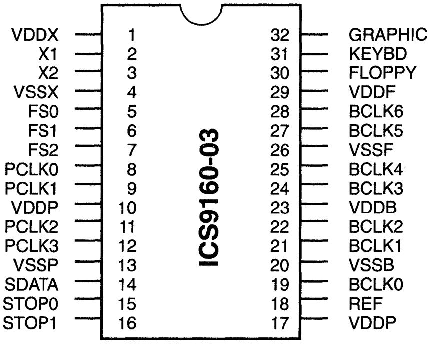
- Ideal for RISC systems based on the PowerPC 603 and 604 microprocessors.

Block Diagram



PowerPC is a trademark of Motorola Corporation

Pin Configuration



32-Pin SOP
K-7

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2	X1	IN	XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 10-30 MHz XTAL.
3	X2	OUT	XTAL output which includes XTAL load capacitance.
1 4	VDDX VSSX	PWR	XTAL oscillator circuit and REFCLK output power supplies.
8, 9, 11	PCLK(0,3)	OUT	Processor clock outputs which are a multiple of the input reference frequency as shown in the table below. Duty cycle is 50% with a maximum frequency of 100 MHz. Custom multiplying configurations are available.
10, 17 13	VDDP, VSSP	IN	PCLK power supplies. VDDP powers the internal PCLK PLL and the PCLK(0,3) outputs. Operation at 5.0V±10% or 3.3V±10% is possible with a maximum PCLK speed of 150 MHz and 100 MHz, respectively.
14	SDATA (First in - REFCLK, PCLK(0,4) BCLK(0,5) FLOPPY, KEYBD, GRAPHIC - last in)	IN	Serial stop clock data is clocked in on the rising edge of BCLK. A total of 15 bits must be clocked in using the following protocol. SDATA is sampled on the rising edge of BCLK, so the data generator should change data on the rising edge of BCLK to ensure proper communication. SDATA must be low for one BCLK period as a start bit. The next 15 rising edges of SCLK will clock data in serially. The 16th clock enables the serial data to take effect. Outputs associated with serial data bits that are a one will continue without interruption. Clocks associated with serial data bits that are a zero will be stopped in the low state glitch-free, that is, no short clocks with the exception of REFCLK which is asynchronously forced low. This input has an internal pull-up device.
15, 16	STOP(0,1)	IN	Stop clock control pins used for glitch-free start and stop of the clock outputs as described in the table on the next page. These inputs have internal pull-up devices.
18	REFCLK	OUT	Buffered copy of the crystal reference frequency.
19, 21, 22, 24, 25, 27, 28	BCLK(0,6)	OUT	Bus clock outputs having selectable frequency based on the FS(0,2) inputs (see table on next page). In all cases, the duty cycle is 50%.
20 23	VSSB VDDB	PWR	BCLK power supplies. VSSB and VDDB power BCLK(0,6).
26 29	VSSF VDDF	PWR	Fixed clock power supplies. VSSF and VDDF power GRAPHIC, FLOPPY and KEYBD outputs plus the fixed clock PLL.
30	FLOPPY	OUT	The floppy clock output operates at 24 MHz.
31	KEYBD	OUT	The keyboard clock output operates at 12 MHz.
32	GRAPHIC	OUT	The graphics system clock output operates at 40 MHz.

Timing Specifications

3.3V±5%VDD, 0-70°C, measured at 1.5V, Cload=20pf

PIN	JITTER max*	SKEW to PCLK	SKEW to BCLK	SLEW, LOAD	DUTY CYCLE
PCLK(0,5)	<±200ps	<±150ps	<±200ps	>1.0V/ns, 20pf	<±500ps
BCLK(0,3)	<±200ps	<±200ps	<±150ps	>1.0V/ns, 30pf	<±500ps
FLOPPY	<±250ps	n/a	n/a	>0.8V/ns, 20pf	<±5%
GRAPHIC	<±300ps	n/a	n/a	>0.8V/ns, 20pf	<±5%

* Jitter spectrum meets PowerPC PLL natural frequency in band requirements of less than ±150ps.

5.0V±5%VDD, 0-70°C, measured at 1.5V, Cload=20pf

PIN	JITTER max*	SKEW to PCLK	SKEW to BCLK	SLEW, LOAD	DUTY CYCLE
PCLK(0,5)	<±250ps	<±150ps	<±200ps	>1.0V/ns, 20pf	<±500ps
BCLK(0,3)	<±250ps	<±200ps	<±150ps	>0.8V/ns, 30pf	<±500ps
FLOPPY	<±300ps	n/a	n/a	>0.8V/ns, 20pf	<±5%
GRAPHIC	<±350ps	n/a	n/a	>0.8V/ns, 20pf	<±5%

* Jitter spectrum meets PowerPC PLL natural frequency in band requirements of less than ±150ps.

Functionality

FS2	FS1	FS0	X1, REFCLK (MHz)	PCLK(0,4) (MHz)	BCLK(0,5) (MHz)	GRAPHIC (MHz)	FLOPPY (MHz)	KEYBD (MHz
0*	0*	0*	Tristate	Tristate	Tristate	Tristate	Off	Tristate
0*	0*	1*	14.318	Off	Off	40.0	24.0	12.0
0	1	0	14.318	33.3	16.6	40.0	24.0	12.0
0	1	1	14.318	50.0	25.0	40.0	24.0	12.0
1	0	0	14.318	60.0	30.0	40.0	24.0	12.0
1	0	1	14.318	66.6	33.3	40.0	24.0	12.0
1	1	0	14.318	80.0	40.0	40.0	24.0	12.0
1	1	1	TCLK**	TCLK/2	TCLK/4	TCLK/3	TCLK/5	TCLK/10

* The oscillator and all PLLs are stopped to minimize power consumption in modes '000' and '001.' All outputs maintain their last stable value in mode '001.' Control signals STOP0 and STOP1 can be used to ensure glitch-free sart and stop when entering mode '001,' provided mode '001' is entered after the clocks have stopped and exited 10ms (maximum PLL lock time) prior to starting clocks.

** X1 is externally driven with TCLK in mode '111.'

Group Clock Control

STOP1 +	STOP0 +	SDATA *	PCLK(0,1)	PCLK(2,4)	BCLK(0,5)	GRAPHIC, FLOPPY	KEYBD, REFCLK
0	0	1	Low	Low	Low	Low	Running
0	1	1	Low	Low	Running	Running	Running
1	0	1	Low	Running	Running	Running	Running
1	1	1	Running	Running	Running	Running	Running

Outputs stop and start glitch-free within on clock period. Outputs will not change state if the PLLs are off.
* Each output can be stopped and started glitch-free as described in the SDATA pin description above.
+SDATA control and STOP(0,1) control are logically ORed for each individual clock.

Ordering Information

ICS9160-03M

Example:

ICS XXXX-PPP M

Package Type
M=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development Characteristic data and other specifications are design goals ICS reserves the right to change or discontinue these products without notice

Integrated
Circuit
Systems, Inc.

ICS9178-02

240 MHz Clock Generator and Integrated Buffer for PowerPC™

General Description

The **ICS9178-02** generates all clocks required for high speed PowerPC RISC microprocessor systems. Generating clocks in phase with an external reference frequency allows the **ICS9178-02** to be used as a multiplying zero delay buffer. Three different multiplying factors are externally selectable. These factors can be customized for specific applications. An external frequency can be directly applied to aid system testing. With 2X processor clock speeds up to 240 MHz, PECL outputs are provided. User selectable frequency ratios are available for PCLK/BCLK and PCLK/XCLK. Each pair of clocks outputs have separate supply pins to minimize output jitter and allow them to operate at 5V, 3.3V or custom voltage levels.

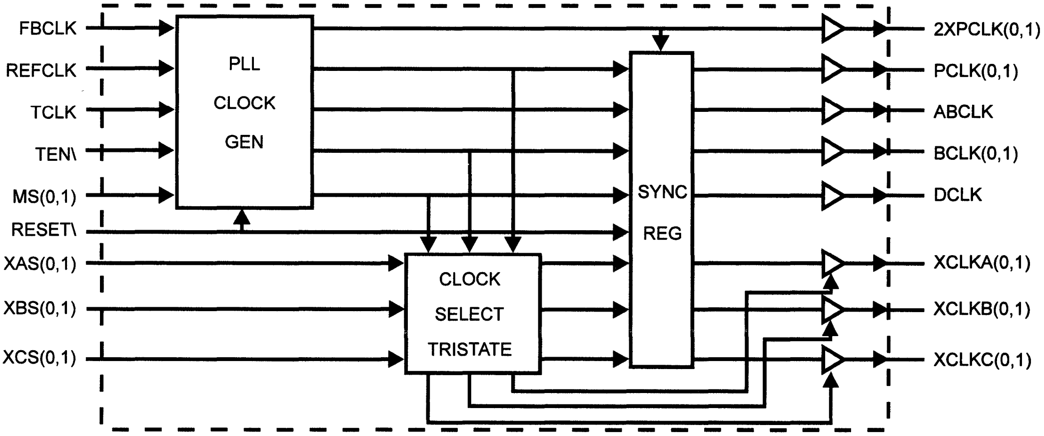
Features

- Generates 2 PECL 2x processor, 2 TTL/CMOS 1x processor and 10 selectable bus clocks
- 2XPCLK ranges from 75 MHz to 240 MHz (5V or 5V/3.3V mixed supply) or 60 to 150 MHz (3.3V only)
- Asymmetric duty cycle bus clock for PowerPC
- Bus to processor clock skews less than ±250ps
- 2XPCLK to PCLK skew controlled at 750 ±500ps
- Selectable reference multiplying factors
- Selectable PCLK/BCLK and PCLK/XCLK ratios
- Separate supplies allow 5V and 3.3V output mix
- 3.0V - 5.5V supply range
- 44-pin PQFP package

Applications

- Ideal for high-speed systems based on PowerPC

Block Diagram



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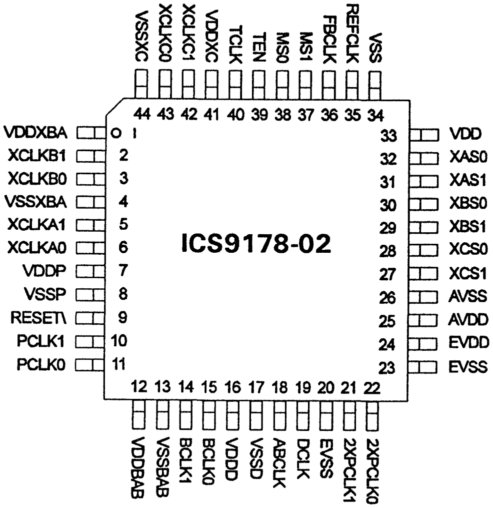
Pin Configuration



44-Pin PQFP
K-11

*VCO range is limited from 75- 240 MHz at 5V ±5% and 60 - 150 MHz at 3.3V ±5%. Divide ratios assume BCLK is externally feedback to FBCLK.

Rising edge of ABCLK is coincident with rising edges of 2XPCLK, PCLK and other BCLKs.

X_S1	X_S0	XCLK_(0,1)
0	0	PCLK
0	1	BCLK
1	0	DCLK
1	1	Tristate

_=A,B,C

ICS9178-02 Functionality

MS1	MS0	RST\	TEN	*VCO	2XPCLK	PCLK	ABCLK (H/L%)	BCLK	DCLK
0	0	1	0	6x X1	VCO	VCO/2	VCO/6 (66/33)	VCO/6	VCO/12
0	1	1	0	8x X1	VCO	VCO/2	VCO/8 (75/25)	VCO/8	VCO/16
1	0	1	0	12x X1	VCO	VCO/2	VCO/12 (66/33)	VCO/12	VCO/24
1	1	1	0	X	1	1	1	1	1
X	X	0	X	X	0	0	0	0	0
0	0	1	1	TCLK	TCLK	TCLK/2	TCLK/6 (66/33)	TCLK/6	TCLK/12
0	1	1	1	TCLK	TCLK	TCLK/2	TCLK/8 (75/25)	TCLK/8	TCLK/16
1	0	1	1	TCLK	TCLK	TCLK/2	TCLK/12 (66/33)	TCLK/12	TCLK/24
1	1	1	1	TCLK	TCLK	TCLK/2	TCLK/2	TCLK/2	TCLK/2

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
32	XAS0	Input	LSB Programmable Group A frequency selector
31	XAS1	Input	MSB Programmable Group A frequency selector
6	XCLKA0	Output	TTL/CMOS group A programmable clock output
5	XCLKA1	Output	TTL/CMOS group A programmable clock output
30	XBS0	Input	LSB Programmable Group B frequency selector
29	XBS1	Input	MSB Programmable Group B frequency selector
3	XCLKB0	Output	TTL/CMOS Group B programmable clock output
2	XCLKB1	Output	TTL/CMOS Group B programmable clock output
1	VDDXBA	—	Power for programmable Group A and B buffers (Pins 2, 3, 5, 6)
4	VSSXBA	—	Ground for programmable Group A and B buffers (Pins 2, 3, 5, 6)
44	VSSXC	—	Ground for the programmable Group C buffers (Pins 42 and 43)
43	XCLKC0	Output	TTL/CMOS Group C programmable clock output
42	XCLKC1	Output	TTL/CMOS Group C programmable clock output
41	VDDXC	—	Power for the XC signal output buffers (Pins 42 and 43)
28	XCS0	Input	LSB Programmable Group C frequency selector
27	XCS1	Input	MSB Programmable Group C frequency selector
11	PCLK0	Output	TTL/CMOS 1X Processor clock output
10	PCLK1	Output	TTL/CMOS 1X Processor clock output
8	VSSP	—	Ground for PCLK output buffers (Pins 11 and 10)
7	VDDP	—	Power for PCLK output buffers (Pins 11 and 10)
22	2XPCLK0	Output	PECL 2X Processor clock output
21	2XPCLK1	Output	PECL 2X Processor clock output
24	EVDD	—	Power for PECL buffers (Pins 21 and 22)
23	EVSS	—	Ground for PECL buffers (Pins 21 and 22)
20	EVSS	—	Ground for PECL buffers (Pins 21 and 22)
38*	MS0	Input	LSB frequency select PLL (divider mode control)
37*	MS1	Input	MSB frequency select PLL (divider mode control)
36	FBCLK	Input	External PLL feedback path from one of the BCLK outputs
35	REFCLK	Input	External reference clock input
25	AVDD	—	Power for the analog PLL circuitry
26	AVSS	—	Ground for the analog PLL circuitry
19	DCLK	Output	TTL/CMOS D clock output
16	VDDD	—	Power for D output buffers (Pin 19)
17	VSSD	—	Ground for D output buffer (Pin 19)
15	BCLK0	Output	TTL/CMOS B (Bus) clock output
14	BCLK1	Output	TTL/CMOS B (Bus) clock output
13	VSSBAB	—	Ground for output buffers AB and B clocks (Pins 14, 15 & 18)
12	VDDBAB	—	Power for output buffers AB and B clocks (Pins 14, 15 & 18)
18	ABCLK	Output	TTL/CMOS AB Bus clock (has Asymmetric duty cycle)
40	TCLK	Input	External test clock input
39	TEN	Input	Test enable (tie low)
9	RESET\	Input	Sync register reset (active low)
33	VDD	—	Digital power supply for 5.0 or 3.3V
34	VSS	—	Digital ground supply

*=Pin is pulled-up to VDD internally by the device.

Absolute Maximum Ratings

VDD referenced to GND	7V
Operating temperature under bias	0°C to +70°C
Storage temperature	-40°C to -150°C
Voltage on I/O pins referenced to GND	GND -0.5V to VDD +0.5V
Power dissipation	0.9 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

Device Specifications

Maximum Ratings				
DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Supply voltage relative to GND	VDD	-0.5	7.0	V
Input voltage with respect to GND	V_{IN}	-0.5	VDD +0.5	V
Operating temperature	T_{OPER}	0	+70	°C
Storage temperature	T_{STOR}	-65	+150	°C
Max soldering temperature (10 sec)	T_{SOL}		+260	°C
Junction temperature	T_J		+135	°C
Package power dissipation	P_{DISS}	800	900	mWatts

DC Characteristics

V_{DD} =+5V ±5%, 0°C ≤ $T_{AMBIENT}$ ≤ +70°C unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
High level input voltage	V_{IH}		2.0			V
Low level input voltage	V_{IL}				0.8	V
High level CMOS output voltage	V_{OH}	I_{OH}=-25ma	2.4			V
Low level CMOS output voltage	V_{OL}	I_{OL}=25ma			0.4	V
High level PECL output voltage (2XPCLK)	V_{OHP}	110 ohm load to ground	2.2	2.5		V
Low level PECL output voltage (2XPCLK)	V_{OLP}	110 ohm load to ground		0.3	0.6	V
Input high current	I_{IH}	V_{IH}=VDD	-10		10	µa
Input low current (MSX pins, pull-up)	I_{IL1}	V_{IL}=0V			-150	µa
Input low current (other inputs)	I_{IL2}	V_{IL}=0V	-10		10	µa
Output leakage current (XCLKs)	I_{OZ}	(tristate)	-10		10	µa
Power supply current	I_{DD}	@240 MHz on 2XPCLK		145	165	ma
Power supply current (typical) (Note 1)	I_{DD-TYP}	@75 MHz on 2XPCLK		80	90	ma
Input capacitance (Note 1)	C_{IN}				8	pf

Note 1: Parameter is guaranteed by design and characterization. Not tested 100% in production.

AC Characteristics

V_{DD} =+5V ±5%, 0°C ≤ $T_{AMBIENT}$ ≤ +70°C unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Frequency (Note 1)	f_I		8	40.0	50.0	MHz
Input Clock Rise time (Note 1)	I_{CLKr}		-	-	3	ns
Input Clock Fall time (Note 1)	I_{CLKf}		-	-	3	ns
Output Frequency (2XPCLK)	$f_{o2XPCLK}$	6X mode	75 (60 @ 3.3V V_{DD})		240 (150 @ 3.3V)	MHz
Output Frequency (2XPCLK)	$f_{o2XPCLK}$	8X mode	75	-	-	MHz
Output Frequency (2XPCLK)	$f_{o2XPCLK}$	12X mode	75	-	-	MHz
Output Rise time, 0.8 to 2.0V 20% to 80% (Note 1)	$t_{r2XPCLK}$	15pf load	- -	- -	1.2 2.0	ns ns
Fall Time 2.0 to 0.8 80% to 20% (Note 1)	$t_{f2XPCLK}$	15pf load	- -	-	1.2 2.0	ns ns
Output Rise time 80% to 20% (Note 1)	$t_{(TTL)r}$	15pf load	-	-	3.0	ns
Output Fall time 80% to 20% (Note 1)	$t_{(TTL)f}$	15pf load	-	-	3.0	ns
Duty cycle 2XPCLK (Note 1)	d_{t1}	200 to 240 MHz @ 1.4V 110 ohm, 15pf load	42.5	50	57.5	%
Duty cycle 2XPCLK (Note 1)	d_{t2}	160 to 200 MHz @ 1.4V 100 ohm, 15pf load	40	50	60	%
Duty cycle ABCLK (Note 1)	d_{t3}	15pf load @ 1.4V (8X mode)	70	75	80	%
Duty cycle ABCLK (Note 1)	d_{t4}	15pf load @ 1.4V (6X and 12X mode)	61	66	71	%
Duty cycle TTL (other clocks) (Note 1)	d_{t5}	15pf load @ 1.4V	45	50	55	%
Jitter 1 Sigma 2XPCLK (10,000 samples) (Note 1)	T_{j1s1}	for 200 to 240 MHz on 2XPCLK	-	40	-	ps
Jitter 1 Sigma 1XPCLK B & D (10,000 samples) (Note 1)	T_{j1s2}	for 200 to 240 MHz on 2XPCLK	-	50	-	ps
Jitter 1 Sigma AB clock (10,000 samples) (Note 1)	T_{j1s3}	for 200 to 240 MHz on 2XPCLK	-	60	-	ps
Jitter Absolute 2XPCLK (Note 1)	T_{jabs1}	for 200 to 240 MHz on 2XPCLK	-150	80	+150	ps
Jitter Absolute 1XPCLK, B, D clocks (Note 1)	T_{jabs2}	for 200 to 240 MHz on 2XPCLK	-200	110	+200	ps
Jitter Absolute AB clock (Note 1)	T_{jabs3}	for 200 to 240 MHz on 2XPCLK	-250	120	+250	ps

AC Characteristics *(continued)*

V_{DD} =+5V ±5%, 0°C ≤ $T_{AMBIENT}$ ≤ +70°C unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Jitter Absolute 2XPCLK (Note 1)	T_{jabs4}	for 200 to 240 MHz on 2XPCLK at VDD 4.9 to 5.2V	-125	80	+125	ps
Jitter Absolute 1XPCLK, B, D clocks (Note 1)	T_{jabs5}	for 200 to 240 MHz on 2XPCLK at VDD 4.9 to 5.2V	-160	110	+160	ps
Jitter Absolute 2XPCLK (Note 1)	T_{jabs6}	for ≤ 200 MHz on 2XPCLK	-200	-	+200	ps
Jitter Absolute 1XPCLK (Note 1)	T_{jabs7}	for ≤ 200 MHz on 2XPCLK	-250	-	+250	ps
Jitter Absolute AB clock (Note 1)	T_{jabs8}	for ≤ 200 MHz on 2XPCLK	-300	-	+300	ps
Skew, output to output (P, B, D and AB) (Note 1)	T_{skew1}	@ 1.4V	-250	-	+250	ps
Skew, Feedback into RefCLK Input (Note 1)	T_{skew2}	@ 1.4V	-250	-125	0	ps
Skew, 2XPCLK to PCLK (2XPCLK is later than PCLK) (Note 1)	T_{skew3}	@ 1.4V	+250	750	+1250	ps

Note 1: Parameter is guaranteed by design and characterization. Not tested in 100% production.

Ordering Information

ICS9178-02CY44

Example:

ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
Y=QFP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated Circuit Systems, Inc.

AN05

Pentium Applications Note

Clocking Intel Pentium-Based Systems

The Intel Pentium processor brings new levels of performance to PC-based desktop systems. Unfortunately for the system designer, it also places higher demands on the system clocking. Jitter, high and low time, and skew are carefully specified. Oscillators may be expensive or difficult to obtain for the frequencies needed. Clock skew can be difficult to control.

ICS offers a number of solutions for the Pentium system designer, from our workhorse, AV9155A, proven in millions of 386 and 486 systems, to the ICS9175, with its six skew controlled outputs. The AV9172 and ICS9176 are pin and function compatible CMOS alternatives to GA1210 and GA1086 GaAs PLL clock drivers.

For low cost systems, where only the processor is clocked, the simplest solution is to use the AV9155A-23, shown in Figure 1. This clock generator features fixed outputs of 1.84, 16, 24, 12 and two 14.318 MHz. The CPU output can be selected with the three address pins to one of eight frequencies, including 66.66, 60, and 52 MHz. A CPU/2 output is also provided, which is skew matched to typically 200ps.

The AV9154A-27, shown in Figure 2, offers the most commonly used system clocks of 1.84, 24, 12 and 14.318 MHz, as well as a single CPU output which can be set to one of eight frequencies. The 16-pin package uses very little board space.

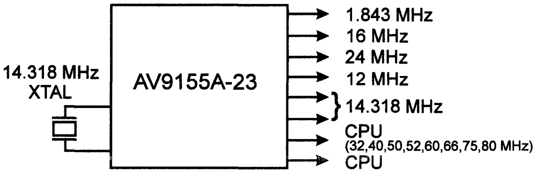


Figure 1

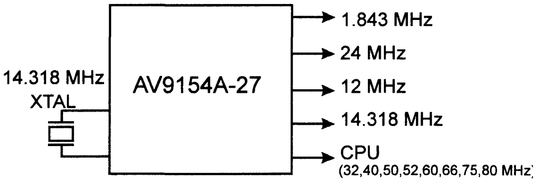


Figure 2

High performance systems have more demanding clock requirements. The processor, cache controller, local bus accelerators, and PCI-EISA bridge require low skew, low jitter clocks. The AV9172 is a phase-locked loop buffer with six outputs - four at the CPU frequency and two at 1/2 CPU frequency. Two of the CPU outputs can be configured as non-overlapping clocks. The AV9172 has guaranteed skew of 250ps between outputs running at the same frequency (50ps typical) and 500ps between 1x and 1/2x outputs. A typical configuration is shown in Figure 3. The output frequency is exactly 1x or 2x the input frequency with ±500ps skew between input and output.

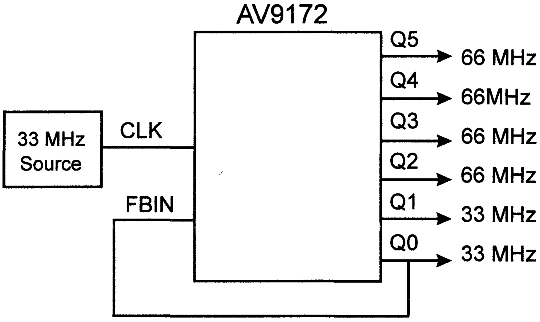
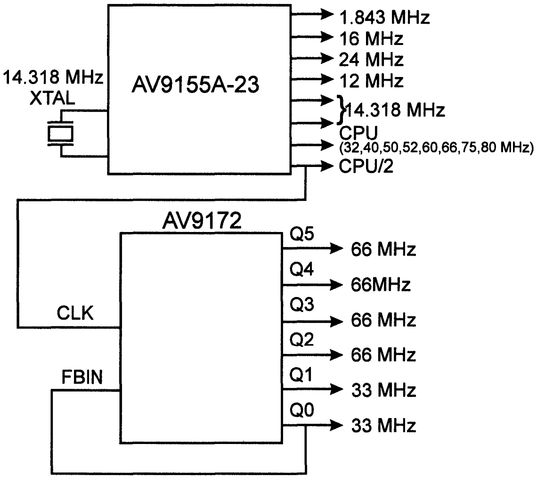


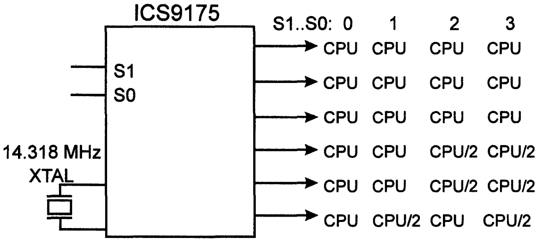
Figure 3

An ideal source for the 1/2x clock required by the AV9172 is the AV9155A-23 mentioned earlier. This gives the system designer all the fixed clocks that he requires, as well as low jitter, skew matched copies of the CPU and 1/2CPU clocks (Figure 4). The AV9172 is a direct replacement for the Gazelle GA1210, but fabricated in a high speed CMOS process rather than expensive gallium arsenide.



ALL CPU AND CPU/2 OUTPUTS SKEW CONTROLLED

Figure 4

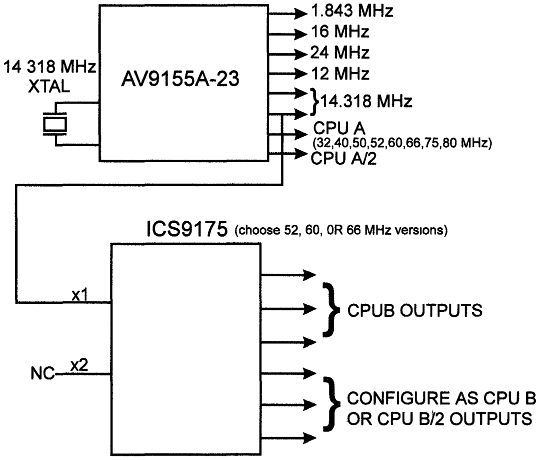


VERSIONS AVAILABLE FOR CPU = 52, 60, AND 66 MHz

Figure 5

The ICS9175 is a single frequency clock generator which synthesizes standard Pentium system frequencies from a low cost 14.318 MHz crystal. Using the select pins, the designer can allocate the six outputs to be either 1x or 1/2x outputs as shown in Figure 5. The ICS9175 may also be driven directly from the 14.318 MHz output of the AV9155A-23, as shown in Figure 6. This gives the system designer all required fixed clocks, six skew matched CPU clocks plus another CPU and 1/2 CPU output, which can be independently varied in frequency.

The ICS9176 is a direct replacement for the Gazelle GA1086, which features ten skew matched outputs. Additional information will be forthcoming.



ALL CPU A AND CPU B FREQUENCIES ARE INDEPENDENT

Figure 6

ICS
Special Purpose IC Products

With a well established foundation in both video and motherboard clock generators, ICS is committed to providing our customers with any form of products that will produce tighter integration, reduced component costs and lower manufacturing costs.

In this issue of the ICS Data Book, ICS provides many special purpose clock generators that address the audio, embedded system and high accuracy needs of our customers.

As a market-oriented company, ICS welcomes inquires concerning our new product areas or other frequency synthesis applications.

Special Purpose IC Products Guide

Product Applications	ICS Device Type	Description	Package Types	Page
Motherboard	ICS1694A	Single Crystal Generates Three Low-Jitter Clocks.	8-Pin DIP, SOIC	D-3
Disk Drive or Video	AV9110	User-Programmable "On-the-Fly"; Low-Jitter makes it ideal for Disk Drive or Video Applications.	14-Pin DIP, SOIC	D-7
RAMBUS	ICS9111-01	High Frequency Clock for RAMBUS Systems.	8-Pin SOIC	D-17
Modem **Ethernet** **AD1848**	ICS9123	High Resolution Clock Generator; One Channel has Accuracy to within 50 PPM and making it ideal for Modem, Ethernet and AD1848 Applications.	16- or 20-Pin DIP, SOIC	D-19
Telecom, Radio, Video, Motherboard	AV9170	Clock Synchronizer and Multiplier.	8-Pin DIP, SOIC	D-21
Pentium	AV9172	Low Skew Output Buffer. Low Skew and Jitter make it ideal for Pentium Applications.	16-Pin DIP, SOIC	D-37
Video Genlock	AV9173	Low Cost Video Genlock PLL.	8-Pin DIP, SOIC	D-45
Pentium PCs or Workstations	ICS9175	Low Skew Output Buffer Crystal Generates Six Low Skew, Low-Jitter Clocks.	16-Pin DIP, SOIC	D-51
Pentium or PLI	ICS9176	Input Clock Generates I/O Low Skew, Low-Jitter Outputs. Ideal for Pentium or PLI Applications.	28-Pin PLCC	D-57
High Frequency Motherboard	ICS9177	High Frequency Clock Generator. High-Performance, Low Skew, PECL and TTL Output Motherboard Clock Generator.	52-Pin QFP	D-63

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. ICS reserves the right to change or discontinue these products without notice.

Integrated
Circuit
Systems, Inc.

ICS1694A

Product Preview

Mini-Motherboard Clock Generator

Description

The **ICS1694A** Mini-Motherboard Clock Generator has been developed to give designers a unique, efficient (cost, size, and power) means of generating the various clocks required in a digital system. The initial patterns being offered as standards are summarized in Table 1.

The low cost and small size of the **ICS1694A** allow the designer to use multiple devices (different patterns) in a system in order to generate the clock signals physically close to the requirement, instead of having long PCB board traces transmitting (and radiating) the signals.

The **ICS1694A** contains all the passive components required for a crystal oscillator or it may be driven by a clock signal. In some applications, one of the outputs of one **ICS1694A** will be used as the clock input of a second or third **ICS1694A**, thus requiring only one quartz crystal for the system and, in the process, synchronizing all the clock signals to the crystal oscillator.

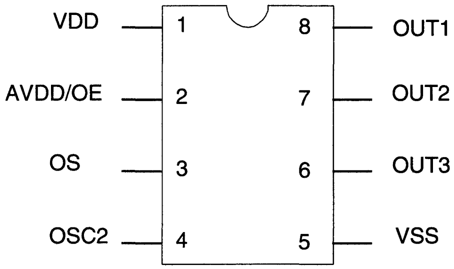
The **ICS1694A** contains a single PLL. Therefore all output frequencies, other than the buffered crystal oscillator, must be the result of an integer division of the PLL frequency. For instance, if the PLL operates at 120 MHz, the outputs could be a selection of three of any of the following: 120 MHz, 60 MHz, 40 MHz, 30 MHz, 24 MHz, 20 MHz, 15 MHz, 12 MHz, 10 MHz, 8 MHz, 6 MHz, etc. More detail concerning the options is given in the section titled PATTERNS.

Features

- Low Cost Motherboard Clock Generator
- Small Footprint, space-saving package
- Very Flexible Architecture
- Advanced PLL design
- Upgraded the ICS1694 to include Output Enable and higher frequency capabilities
- Many standard patterns available

Applications

- Any design requiring clocking signals or count down chains derived from a clock signal
- Memory refresh
- Keyboard
- Serial port
- Floppy Disk
- Hard Disk
- CPU
- Co-processor



8-Pin DIP or SOIC
K-3, K-6

Options

Pin 2 may be bonded to serve as either AVDD (analog positive supply) or OE (output enable). The outputs (OUT1, OUT2, and OUT3) will be enabled when OE is held high. OE has internal pull-up so it may be allowed to float.

If particularly stable outputs are required, the option with pin 2 bonded as AVDD is recommended. AVDD should be driven by the system's analog supply, if available. In some applications where only a digital supply is available, AVDD can be driven from the digital VDD supply through a simple RC decoupling circuit. The voltage drop across the series resistor should be held to less than 250 mv. It is difficult to generalize across all applications, but in the majority of cases the performance of the **ICS1694A** is completely satisfactory when used with power supplied only to pin 1 and pin 2 bonded as Output Enable.

Patterns

A number of standard patterns will be offered which will satisfy most of the typical requirements of the PC market. New patterns are continuously being added as new applications surface. ICS welcomes suggestions for new patterns and will also fabricate custom patterns as described in the following paragraph.

The **ICS1694A** contains one PLL-VCO which is mask programmable to any frequency up to 180 MHz. The chip contains a number of counter stages which can be used to count the VCO frequency down to the desired output frequencies. The output frequencies are derived by dividing the VCO frequency by an integer.This is a limitation on the frequencies which can be generated in the same chip since each frequency must be derived from the same VCO frequency.

For instance, pattern 010 programs the VCO to 120 MHz. Then a divide by 3 yields 40 MHz; a divide by 4 yields 30 MHz; and a divide by 5 yields 24 MHz. Obviously, some of the divide chains can and are combined. An output may also be the crystal oscillator frequency or that frequency divided by an integer.

It should also be considered that the input does not have to be 14.318 MHz, but can be any fundamental mode crystal up to 25 MHz. Table 1 lists the frequencies available from the various patterns. For any of these patterns, the crystal frequency (and thus the PLL-VCO frequency) may be changed and the output frequencies will be scaled accordingly. For instance, if the crystal frequency used is one half of that listed in Table 1, the actual output frequencies will be one half those listed in the table. Also options are available which will work with an overtone crystal.

Absolute Maximum Ratings

Supply Voltage	V_{DD}	-0.5V to +7V
Input Voltage	V_{IN}	-0.5V to V_{DD}+0.5V
Output Voltage	V_{OUT}	-0.5V to V_{DD}+0.5V
Clamp Diode Current	V_{IK} & I_{OK}	+/-30mA
Output Current per Pin	I_{OUT}	+/-50mA
Operating Temperature	T_o	0 °C to 70 °C
Storage Temperature	T_S	-85 °C to +150 °C
Power Dissipation	P_D	300mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to >= V_{SS} and <=V_{DD}.

DC Characteristics (0°C to 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
5.0V ± 5% OPERATION					
V_{DD}	Operating Voltage Range	4.75	5.25	V	
V_{IL}	Input Low Voltage	V_{ss}	0.8	V	$V_{DD} = 5V$
V_{IH}	Input High Voltage	2.0	V_{DD}	V	$V_{DD} = 5V$
I_{LH}	Input Leakage Current	--	10	µA	$V_{IN} = V_{cc}$
V_{OL}	Output Low Voltage	--	0.4	V	$I_{OL} = 4.0$ mA
V_{OH}	Output High Voltage	2.4	--	V	$I_{OH} = 4.0$ mA
I_{DD}	Digital Supply Current	--	30	mA	$V_{DD} = 5V$, VCO = 120 MHz
I_{AA}	Analog Supply Current		8	mA	$V_{DD} = 5V$, VCO = 120 MHz
C_{in}	Input Pin Capacitance	--	8	pF	$F_c = 1$ MHz
C_{out}	Output Pin Capacitance	--	12	pF	$F_c = 1$ MHz
3.3V ± 10% OPERATION					
I_{DD}	Digital Supply Current	-	20	mA	$V_{DD} = 3.3V$, VCO = 120 MHz
I_{AA}	Analog Supply Current	-	6	mA	$V_{DD} = 3.3V$, VCO = 120 MHz

If the OE option is used, IDD will be the sum of both the digital and analog supply currents.

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section:

1. Xtal Frequency = 14.318 MHz, unless otherwise noted.
2. All units are in nanoseconds (ns).
3. Rise and fall time is between 0.8 and 2.0 VDC at 5.0V.
4. Output pin loading = 15pF
5. Duty cycle is measured at 1.4V at 5.0V.
6. Temperature Range = 0 °C to 70 °C

5.0V ± 5% OPERATION

SYMBOL	PARAMETER	MIN	MAX	NOTES
MCLK AND VCLK TIMING				
Tr	Rise Time	--	2	
Tf	Fall Time	--	2	
Dc	Duty Cycle	45	55	%
Fm	Maximum Frequency		180	MHz

3.0V ± 10% OPERATION

SYMBOL	PARAMETER	MIN	MAX	NOTES
MCLK AND VCLK TIMING				
Tr	Rise Time	--	3	
Tf	Fall Time	--	3	
Dc	Duty Cycle	45	55	%
Fm	Maximum Frequency		120	MHz

Standard Frequency Patterns (MHz)
Table 1

PINS	FUNCTION	PATTERNS							
		010	011	012	013	014	015	016	017
8	OUT1	24	25	12	6	24	24	XTAL	XTAL
7	OUT2	40	40	40	60	40	XTAL	16	12
6	OUT3	30	30	30	20	20	40	24	24
5	VSS								
4	XTAL2	25	25	25	25	14.318	14.318	14.318	14.318
3	XTAL1								
2	AVDD/OE								
1	VDD								

PINS	FUNCTION	PATTERNS							
8	OUT1								
7	OUT2								
6	OUT3								
5	VSS								
4	XTAL2								
3	XTAL1								
2	AVDD/OE								
1	VDD								
8									

Ordering Information

ICS1694AN-XXX or ICS1694AM-XXX

Example:

ICS XXXX M -XXX

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type

N=DIP (Plastic)
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

AV9110

Serially Programmable Frequency Generator

General Description

The **AV9110** generates user specified clock frequencies using an externally generated input reference, such as 14.318 MHz or 10.00 MHz crystal connected between pins 1 and 2. Alternately, a TTL input reference clock signal can be used. The output frequency is determined by a 24-bit digital word entered through the serial port. The serial port enables the user to change the output frequency on-the-fly.

The clock outputs utilize CMOS level output buffers that operate up to 130 MHz.

Features

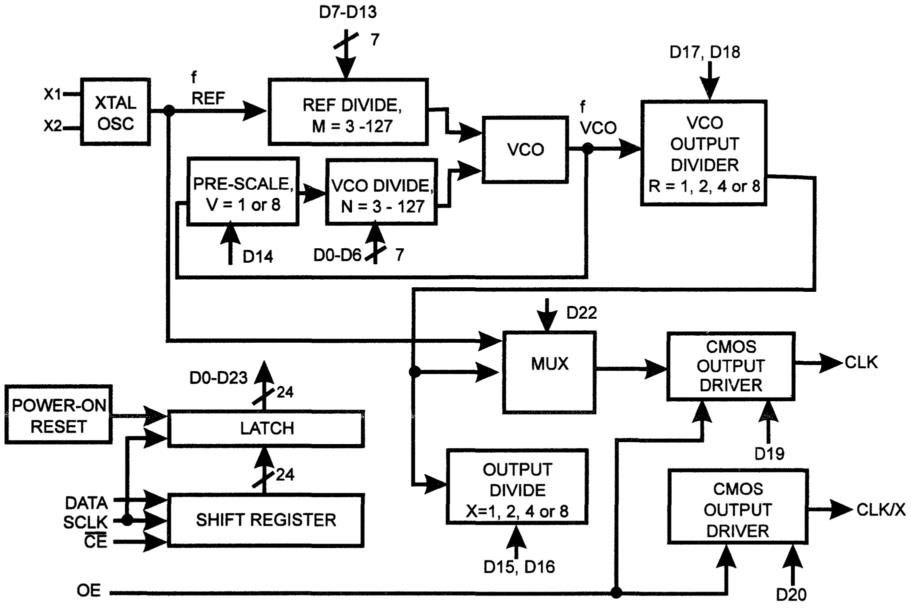
- Complete user programmability of output frequency through serial input data port
- On-chip Phase-Locked Loop for clock generation
- Generates accurate frequencies up to 130 MHz
- Tristate CMOS outputs
- 5 volt power supply
- Low power CMOS technology
- 14-pin DIP or 150 mil SOIC
- Very low jitter
- Wide operating range VCO

D

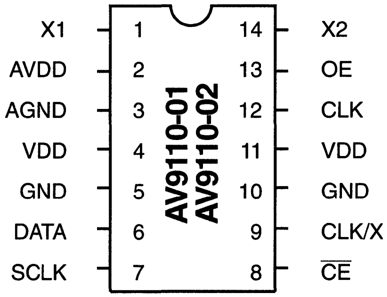
Applications

Graphics: The **AV9110** generates low jitter, high speed pixel (or dot) clocks. It can be used to replace multiple expensive high speed crystal oscillators. The flexibility of this device allows it to generate non-standard graphics clocks, allowing the user to program frequencies on-the-fly.

Block Diagram



Pin Configuration



14-Pin DIP, SOIC
K-3, K-6

Clock Reference Implementations:

AV9110-01 vs. AV9110-02

The **AV9110** requires a stable reference clock (5 to 32 MHz) to generate a stable, low-jitter output clock. The **AV9110-01** is optimized to use an external quartz crystal as a frequency reference, without the need of additional external components. The **AV9110-02** is optimized to accept an TTL clock reference. Either device can be used with an external crystal or accept a TTL clock reference, although extra components may be required. The various combinations implied are summarized in Figure 2 (see page 7).

Pin Descriptions

PIN NUMBER	PIN NAME	PIN TYPE	DESCRIPTION
1	X1	Input	Crystal input or TTL reference clock
2	AVDD	Power	ANALOG power supply. Connect to +5V
3	AGND	Power	ANALOG GROUND
4	VDD	Power	Digital power supply. Connect to +5V
5	GND	Power	Digital GROUND
6	DATA	Input	Serial DATA pin
7	SCLK	Input	SERIAL CLOCK. Clocks shift register
8	$\overline{\text{CE}}$	Input	CHIP ENABLE. Active low, controls data transfer
9	CLK/X	Input	CMOS CLOCK divided by X output
10	GND	Power	Digital GROUND
11	VDD	Power	Digital power supply. Connect to +5V
12	CLK	Output	CMOS CLOCK output
13	OE	Input	OUTPUT ENABLE. Tristates both outputs when low
14	X2	Input	Crystal input or TTL reference clock

Absolute Maximum Ratings

AVDD, VDD referenced to GND 7V
Operating temperature under bias .... 0°C to +70°C
Voltage on I/O pins referenced to GND........... GND -0.5V to V_{DD} + 0.5V
Power dissipation .... 0.8 Watts
Storage temperature .... -65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} = +5V±10%, T_A = 0°C to 70°C unless otherwise stated

DC/STATIC						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD} = 5V	-	-	0.8	V
Input High Voltage	V_{IH}	V_{DD} = 5V	2.0	-	-	V
Input Low Current	I_{IL}	V_{IN} = OV	-	-	-5	µA
Input High Current	I_{IH}	V_{IN} = V_{DD}	-	-	5	µA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = 8mA	2.4	-	-	V
Input Clock Rise Time	$ICLK_r$		-	-	20	ns
Input Clock Fall Time	$ICLK_f$		-	-	20	ns
Supply Current	I_{DD}	No load	-	25		mA
AC/DYNAMIC						
Output frequency range	f_o		0.78	-	130	MHz
Rise time, 20-80%	t_r	25pF load	-	-	3	ns
Fall time, 80-20%	t_f	25pF load	-	-	3	ns
Duty cycle	d_t	25pF load	40		60	%
Jitter, 1 sigma				±40	-	ps
Jitter, absolute				±125	-	ps
Input reference freq.; AV9110-01	f_{REF}	Crystal input	5	14.318	32	MHz
Input reference freq.; AV9110-02	f_{REF}	TTL input	0.6	14.318	32	MHz
Input DATA or SCLK frequency	f_{DATA}				32	MHz

Serial Programming

The **AV9110** is programmed to generate clock frequencies by entering data through the shift register. Figure 1 displays the proper timing sequence. On the negative going edge of CE, the shift register is enabled and the data at the DATA pin is loaded into the shift register on the rising edge of the SCLK. Bit D0 is loaded first, followed by D1, D2, etc. This data consists of the 24 bits shown in the Shift Register Bit Assignment in Table 1, and therefore takes 24 clock cycles to load. An internal counter then disables the input and transfers the data to internal latches on the rising edge of the 24th cycle of the SCLK. Any data entered after the 24th cycle is ignored until CE must remain low for a minimum of 24 SLCK clock cycles. If CE is taken high before 24 clock cycles have elapsed, the data is ignored (no frequency change occurs) and the counter is reset. Tables 1 and 2 display the bit location for generating the output clock frequency and the output divider circuitry, respectively.

Table 1: Shift Register Bit Assignment

BIT	ASSIGNMENT	EQUATION VARIABLE	DEFAULT -01	DEFAULT -02	BIT
0	VCO frequency divider (LSB)	N Integer	1	1	0
1	"		1	1	1
2	"		1	1	2
3	"		1	1	3
4	"		1	1	4
5	"		1	1	5
6	VCO frequency divider MSB)		1	1	6
7	Reference frequency divider	M Integer	0	0	7
8	"		1	1	8
9	"		0	0	9
10	"		0	0	10
11	"		1	1	11
12	"		0	0	12
13	Reference frequency divider		0	0	13
14	VCO pre-scale divide (0=divide by 1, 1= divide by 8	V	0	0	14
15	CLK/X output divide CODO (see Table 2)	X	0	1	15
16	CLK/X output divide CODO (see Table 2)		1	0	16
17	VCO output divide VODO (see Table 2)	R	0	0	17
18	VCO output divide VODO (see Table 2)		1	1	18
19	Output enable CLK (0=tristate)		1	1	19
20	Output enable CLK/X (0=tristate)		1	1	20
21	Reserved. Should be programmed low (0)		1	1	21
22	Reference clock select on CLK (1 = reference frequency)		0	0	22
23	Reserved. Should be programmed high (1)		1	1	23

Output Divider Truth Tables

Table 2

COD1	COD0	CLK/X Output Divide (X)
0	0	1
0	1	2
1	0	4
1	1	8

Table 3

VOD1	VOD0	VCO Output Divide (R)
0	0	1
0	1	2
1	0	4
1	1	8

Programming the PLL

The **AV9110** has a wide operating range but it is recommended that it is operated within the following limits:

$2\text{ MHz} < f_{REF} < 32\text{ MHz}$	f_{REF} = Input reference frequency
$200\text{ kHz} < \frac{f_{REF}}{M} < 5\text{ MHz}$	M = Reference divide, 3 to 127
$50\text{ MHz} < f_{VCO} < 250\text{ MHz}$	f_{VCO} = VCO output frequency
$f_{VCO} < 250\text{ MHz}$	f_{CLK} = CLK or CLK/X output frequency

The **AV9110** is a classical PLL circuit and the VCO output frequency is given by:

$$f_{VCO} = \frac{N \bullet V \bullet f_{REF}}{M}$$

where N = VCO divided, 3 to 127
M = Reference divide, 3 to 127
V = Prescale, 1 or 8

The 2 output drivers then give the following frequencies:

$$f_{CLK} = \frac{f_{VCO}}{R} = \frac{N \bullet V \bullet f_{REF}}{M \bullet R}$$ or f_{REF} (output muxable by bit 17)

$$f_{CLK/X} = \frac{f_{VCO}}{R \bullet X} = \frac{f_{VCLK}}{X}$$ Where R, X = output dividers 1, 2, 4 or 8

Notes:
1. Output frequency accuracy will depend solely on input reference frequency accuracy.
2. For output frequencies below 125 MHz, it is recommended that the VCO output divide, R, should be 2 or greater. This will give improved duty cycle.
3. The minimum output frequency step size is approximately 0.2% due to the divider range provided.

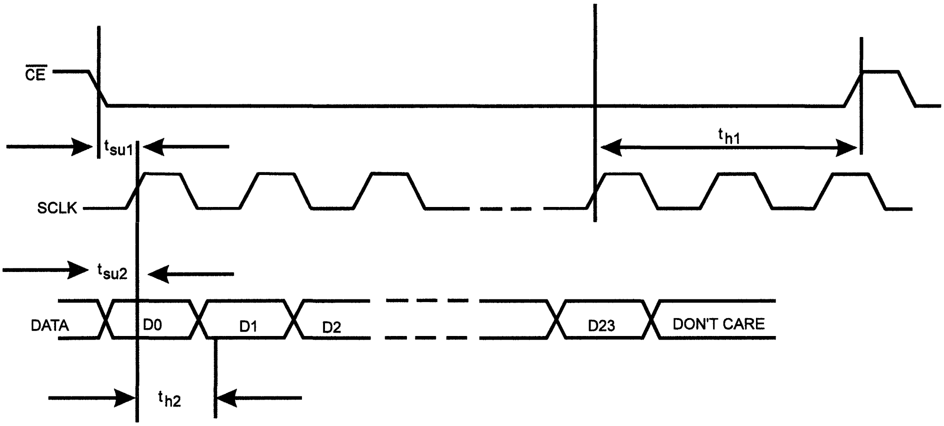


Figure 1 - Serial Programming

AC Timing

Parameter	Minimum time (ns)
t_{su1}	10
t_{su2}	10
t_{h1}	10
t_{h2}	10

Frequency Acquisition Time

Frequency acquisition (or "lock") time is the time that it takes to change from one frequency to another, and is a function of the difference between the old and new frequencies. The **AV9110** can typically lock to within 1% of a new frequency in less than 200µs. This is also true with power-on.

Power-On Reset

Upon power-up the internal latches are preset to provide the following output clock frequencies (14.318 MHz reference assumed):

Device	CLK output	CLK/X output
AV9110-01	25.175 MHz	6.29 MHz
AV9110-02	25.175 MHz	12.59 MHz

These preset default frequencies can be changed with a custom metal mask, as can other attributes.

Jitter

For high performance applications, the **AV9110** offers extremely low jitter and excellent power supply rejection. The one sigma jitter distribution is typically less than ±125ps. For optimum performance, the device should be decoupled with both a 2.2µF and a 0.1µF capacitor. Refer to Recommended Board Layout diagram on page 8.

Output Enable

The **AV9110** outputs can be disabled with either the OE pin or through serial programming. Setting the OE pin low tristates CLK and CLK/X. Alternatively, setting bits D19 and D20 low in the serial word will tristate the two outputs. Both the OE pin and D19 or D20 must be high to enable an output.

Frequency Transition Glitches

The **AV9110** starts changing frequency on the rising edge of the 24th serial clock. If the programming of any output divider is changed, the output clock may glitch before locking to the new frequency in less than 200µs with no output glitches (no partial clock cycles).

AV9110 Quartz Crystal Selection

When an external quartz crystal will be used as a frequency reference for the **AV9110**, attention needs to be given to crystal selection if accurate reference frequency and output frequency is desired. The **AV9110** uses a Pierce oscillator design which operates the quartz crystal in parallel-resonant mode. It requires a quartz crystal cut for parallel-resonant operation to ensure an accurate frequency of oscillation (a less expensive series-resonant crystal can be used with the device but it will oscillate approximately 0.1% too fast). The **AV9110-01** has internal crystal load capacitors which result in a total crystal load capacitance of approximately 12pF±10%. The **AV9110-02** does not have internal load capacitors, but contributes about 3pF load capacitance to the crystal.

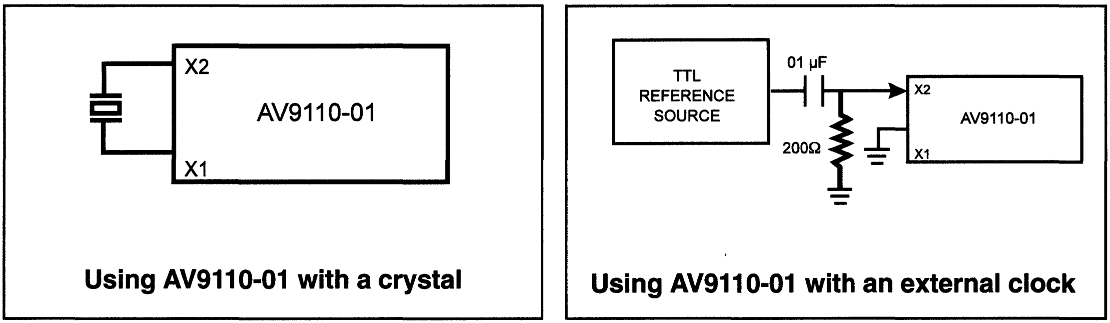
Following is a list of recommended crystal devices for the **AV9110**. They have been tested by the crystal manufacturer to operate suitably with the AV91xx-series crystal oscillator design, having load capacitance characteristics that are compatible with the **AV9110-01**.

Toyocom

Part Number	
TN4-30374	14.318 MHz surface mount crystal
TN4-30375	20 MHz surface mount crystal
TN4-30376	14.318 MHz through-hole crystal
TN4-30377	20 MHz through-hole crystal

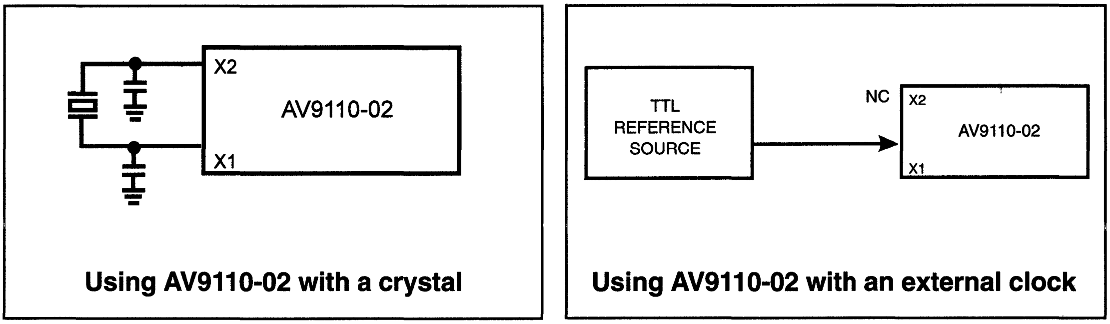
Epson

Part Number	
MA-505 or MA-506	Surface mount crystal
CA-301	Through-hole crystal



Using AV9110-01 with a crystal

Using AV9110-01 with an external clock

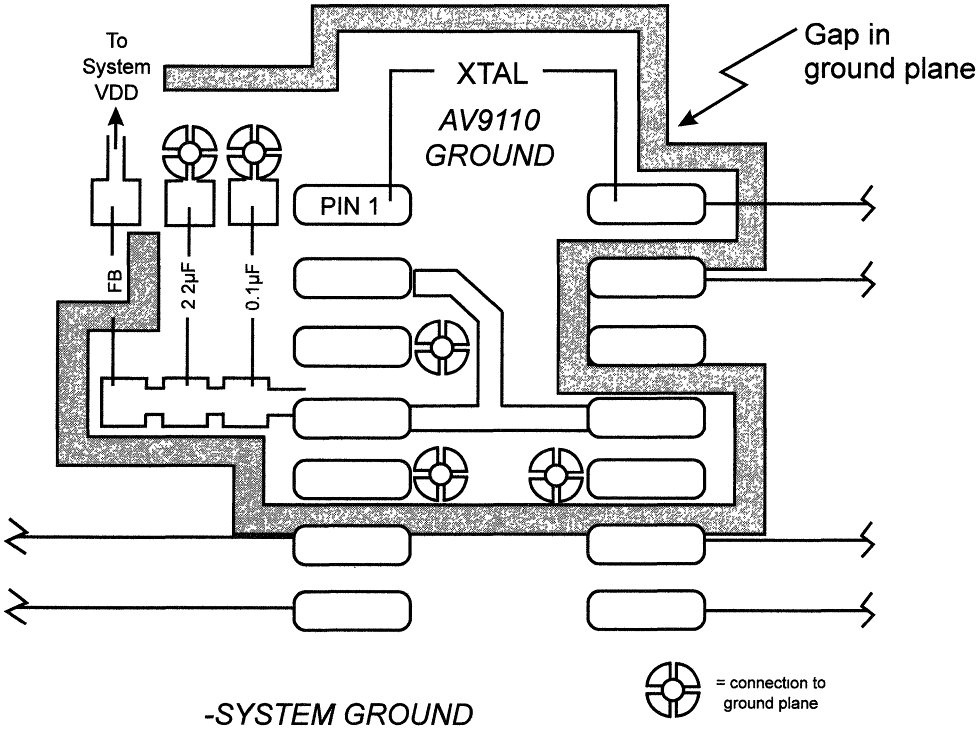


Using AV9110-02 with a crystal

Using AV9110-02 with an external clock

Figure 2 - Clock Reference Combinations

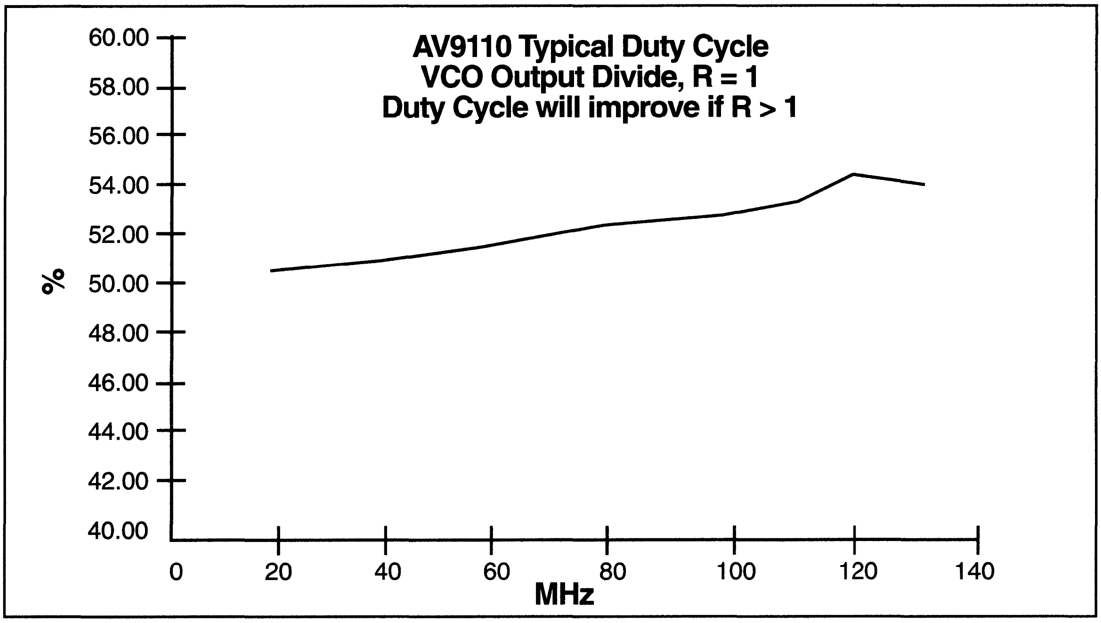
AV9110 Recommended Board Layout

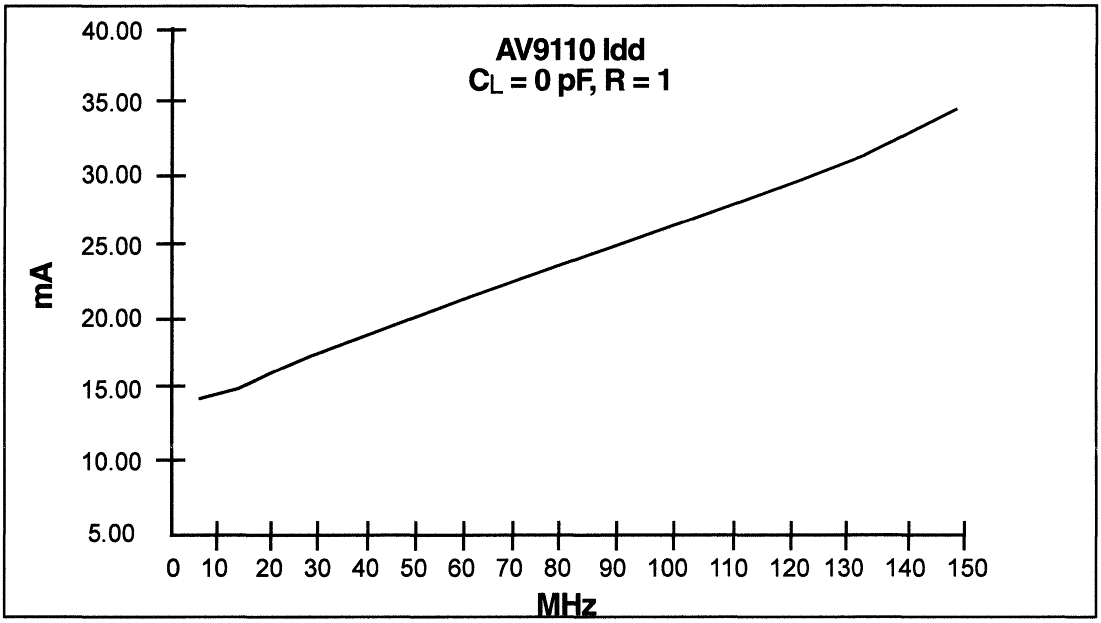


This is the recommended layout for the **AV9110** to maximize clock performance. Shown are the power and ground connections, the ground plane, and the input/output traces.

Use of the isolated ground plane and power connection, as shown, will prevent stray high frequency ground and system noise from coupling to the **AV9110**. As when compared to using the system ground and power planes, this technique will lessen output clock jitter. The isolated ground plane should be connected to the system ground plane at one point near the 2.2µF decoupling cap. For lowest jitter performance, the isolated ground plane should be kept away from clock output pins and traces. Keeping the isolated ground plane area as small as possible will minimize EMI radiation. Use a sufficient gap between the isolated ground plane and system ground plane to prevent AC coupling. The ferrite bead in the VDD line is optional, but will help reduce EMI.

The traces to distribute the output clocks should be over an unbroken system ground or power supply plane. The trace width should be about two times the thickness of the PC board between the trace and the underlying plane. These guidelines help minimize clock jitter and EMI radiation. The traces to distribute power should be as wide as possible.


AV9110 Typical Duty Cycle
VCO Output Divide, R = 1
Duty Cycle will improve if R > 1
60.00
58.00
56.00
54.00
52.00
50.00
48.00
46.00
44.00
42.00
40.00
%
0
20
40
60
80
100
120
140
MHz


AV9110 Idd
C_L = 0 pF, R = 1
40.00
35.00
30.00
25.00
20.00
15.00
10.00
5.00
mA
0
10
20
30
40
50
60
70
80
90
100
110
120
130
140
150
MHz

Ordering Information

AV9110-01CN14, AV9110-02CN14

Example:

ICS XXXX-PPP M X#W

Lead Count
Lead Count=1, 2 or 3 digits

Package Type
N=DIP

Pattern Number (2 or 3 digit number for parts with ROM code patterns, if applicable)
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

AV9110-01CS14, AV9110-02CS14

Example:

ICS XXXX-PPP M X#W

Lead Count
Lead Count=1, 2 or 3 digits

Package Type
S=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns, if applicable)
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS9111-01

Product Preview

250 MHz Clock Generator for RAMBUS™ Systems

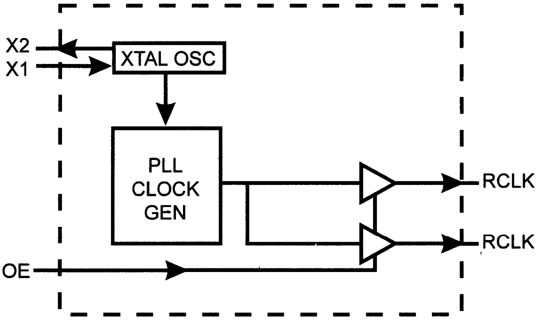
General Description

The **ICS9111-01** is a high speed clock generator designed to support the 533Mbit/line data transfer rates made possible by local phase alignment technologies such as RAMBUS.™ Generating RCLK rates as high as 267 MHz in 3V systems from either a 14.31818 MHz crystal or external system reference, the **ICS9111-01** is ideal for graphics applications.

Two buffered PCLK outputs are provided for highly specialized systems such as video games.

The RCLK open collector buffer output impedance is less than 10Ω to allow external terminating impedance and voltage combinations that meet RAMBUS system specifications. Cycle-to-cycle jitter and output skew are less than 150ps and the 50% duty cycle is maintained to within ±5% for series terminations to Vterm.

Block Diagram



Functionality

VDD=3.3V±10%, TEMP=0-70°C

Option	RCLK Ratio	X1, X2 (MHz)	OE	RCLK (MHz)	PCLK (MHz)
-01	56/3	14.31818	1	267.27	-
		14.31818	0	Tristate	-
-xx	n/m	10-20	1	n/m*x1	RCLK/N

Features

- 267 MHz RCLK meets RAMBUS specifications
- Less than 150ps cycle-to-cycle jitter
- 50±5% duty cycle
- Open drain drivers allow matched termination
- PCLK (RCLK/4) supports 66 MHz processing
- 14.318 MHz crystal or extended reference
- Buffered reference clock output
- On-chip loop filter components
- 3.0V - 3.6V supply range
- 8-pin 150-mil SOIC package
- Custom options capable

Applications

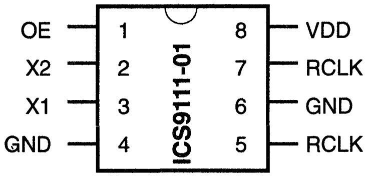
- Specifically designed to support the high speed clocking requirements of systems based on RAMBUS technology

Electrical Specifications

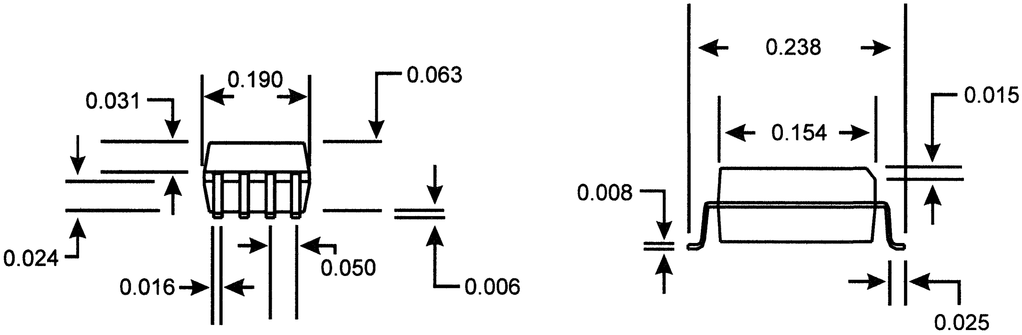
3.3V±10%, 0-70°C

ITEM	LIMIT	UNITS	NOTE
VIL/VIH	<20/>80	%VDD	Pin OE
RUP	<200,<800	k Ohm	Pin OE
FOUT	<100,>267	MHz	Pin RCLK
LOCK TIME	<10	ms	To 0.1%
ROUT	<10	Ohm	Pin RCLK
SKEW	<150	ps	Equal load
ABS JITTER	<150 cyc-to-cyc	ps	Pin RCLK
DUTY CYC	50±5	%	Vptp/2
IDD	<40	mA	Unloaded

Pin Configuration



8-Pin SOIC
K-6



8-Pin SOIC Package

Ordering Information

ICS9111M-01

Example:

ICS XXXX M-PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)
Package Type
M=SOIC
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS9123

Advance Information

High Resolution Frequency Generator

General Description

The **ICS9123** is a multiple output frequency generator utilizing PLL (Phase Lock Loop) frequency synthesis. It contains three PLL frequency synthesizers and an internal crystal oscillator reference circuit. Thus, with only an external crystal and the necessary power supply decoupling capacitors, four different output clock frequencies can be provided.

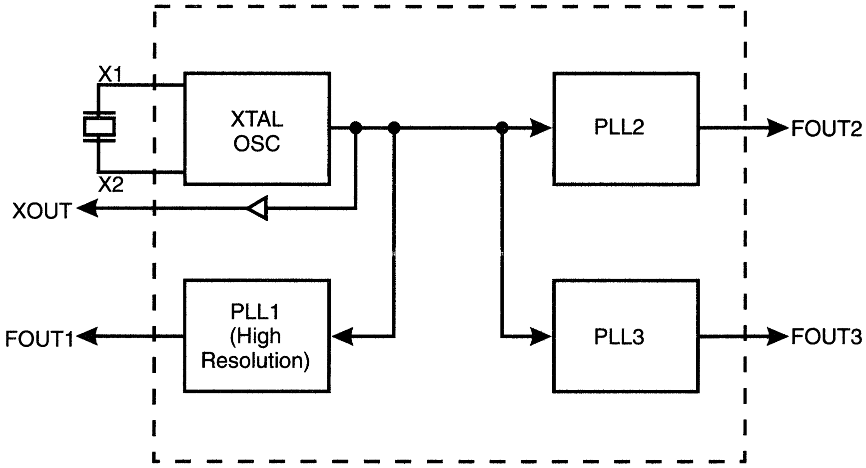
PLL1 of the device has the ability to provide high output frequency resolution (±50 ppm). This makes it suitable for providing clocks for system functions such as modems, ethernet, and sound synthesis. PLL2 and PLL3 provide output clocks for other system applications such as microprocessors and DSP chips. For example, in modem applications, the **ICS9123** generates the high resolution clock generator for the A/D converter and two lower resolution clocks for the microprocessor and DSP.

Each of the PLL clock generators has a ROM based frequency selection table which is addressed through device input pins. PLL1 has eight frequency select locations; PLL2 and PLL3 each has four. The ROM based tables are preprogrammed. However, they can be customized for the user specific applications.

Features

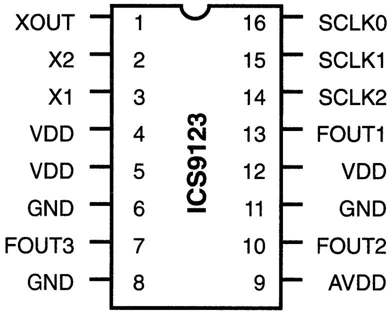
- Cost effective solution for MODEM, ETHERNET and AD1848 applications
- Three independent PLLs
- Four clock frequencies generated from one crystal
- One high resolution PLL provides ±50 ppm accuracy
- Eight ROM based frequency selections for the high resolution PLL1
- Four ROM based frequency selections each for PLL2 and PLL3
- 3.3V or 5V power supply
- On-chip loop filter components
- Low power CMOS technology
- 20- or 16-pin PDIP or SOIC package

Block Diagram



ICS9123

Pin Configuration



16-Pin PDIP or SOIC
K-4, K-6

Decoding Table for Clock Frequency

(using 14.318 MHz Input Frequency)

SCLK2	SCLK1	SCLK0	FOUT1* (MHz)	FOUT2 (MHz)	FOUT3 (MHz)
0	0	0	8.06400	19.7	29.5
0	0	1	19.66080	29.5	8.06
0	1	0	29.49120	8.06	19.7
0	1	1	11.05920	14.6	16.5
1	0	0	13.82400	19.7	29.5
1	0	1	3.68640	29.5	8.06
1	1	0	14.74560	8.06	19.7
1	1	1	16.00031	14.6	16.5

*FOUT1 frequencies shown are accurate to within 2 PPM.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	XOUT	Output	Crystal buffered output
2	X2	Output	Connect crystal
3	X1	Input	Connect crystal
4	VDD	-	3V or 5V power supply
5	VDD	-	3V or 5V power supply
6	GND	-	GROUND
7	FOUT3	Output	Output frequency of one of 3 PLLs
8	GND	-	GROUND
9	VDD	-	3V or 5V power supply
10	FOUT2	Output	Output frequency of one of 3 PLLs
11	GND	-	GROUND
12	VDD	-	3V or 5V power supply
13	FOUT1	Output	Output frequency of the high resolution PLL
14	SCLK2	Input	CPU clock frequency SELECT2 (has pull-up)
15	SCLK1	Input	CPU clock frequency SELECT1 (has pull-up)
16	SCLK0	Input	CPU clock frequency SELECT0 (has pull-up)

Ordering Information

ICS9123N or ICS9123M

Example:

ICS XXXX M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width
Package Type
N=DIP (Plastic) M=SOIC
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
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AV9170

Clock Synchronizer and Multiplier

General Description

The **AV9170** generates an output clock which is synchronized to a given continuous input clock with zero delay (±1ns). Using ICS's proprietary phase-locked loop (PLL) analog CMOS technology, the **AV9170** is useful for regenerating clocks in high speed systems where skew is a major concern. By the use of the two select pins, multiples or divisions of the input clock can be generated with zero delay (see Tables 2 and 3). The standard versions produce two outputs, where CLK2 is always a divide by two version of CLK1.

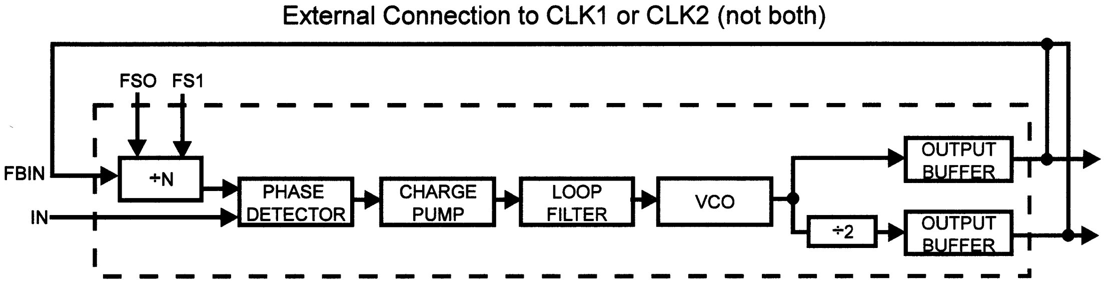
The **AV9170** is also useful to recover poor duty cycle clocks. A 50 MHz signal with a 20/80% duty cycle, for example, can be regenerated to the 48/52% typical of the part.

The **AV9170** allows the user to control the PLL feedback, making it possible, with an additional 74F240 octal buffer (or other such device that offers controlled skew outputs), to synchronize up to 8 output clocks with zero delay compared to the input (see Figure 1). Application notes for the **AV9170** are available. Please consult ICS.

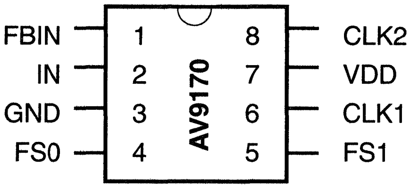
Features

- On-chip Phase-Locked Loop for clocks synchronization
- Synchronizes frequencies up to 100 MHz (output)
- ±1ns skew (max) between input and output clocks
- Can recover poor duty cycle clocks
- CLK1 and CLK2 skew controlled to within ±1ns
- 5 volt only power supply
- Low power CMOS technology
- Small 8-pin DIP or SOIC package
- On chip loop filter
- **AV9170-01**, -04 for output clocks 20-100 MHz
- **AV9170-02**, -05 for output clocks 5-25 MHz

Block Diagram



Pin Configuration



8-Pin DIP or SOIC
K-3, K-6

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FBIN	Input	FEEDBACK INPUT
2	IN	Input	INPUT for reference clock
3	GND	-	GROUND
4	FS0	Input	FREQUENCY SELECT 0
5	FS1	Input	FREQUENCY SELECT 1
6	CLK1	Output	CLOCK output 1 (See Tables 1, 2, 3, 6, 7 for values)
7	VDD	-	Power Supply (+5V)
8	CLK2	Output	CLOCK output 2 (See Tables 1, 2, 3, 6, 7 for values)

Using the AV9170

The **AV9170** has the following characteristics:

1. Rising edges at IN and FBIN are lined up.
   Falling edges are not synchronized.
2. The relationship between the frequencies at FBIN and IN is shown in Table 1.

Table 1

FS1	FS0	f_{FBIN}(-01, -02)	f_{FBIN}(-04, -05)
0	0	2 • f_{IN}	3 • f_{IN}
0	1	4 • f_{IN}	5 • f_{IN}
1	0	f_{IN}	6 • f_{IN}
1	1	8 • f_{IN}	10 • f_{IN}

3. The frequency of CLK2 is half the CLK1 frequency.
4. The CLK1 frequency ranges are:

AV9170-01, -04	20	<	f_{CLK1}	<	100 MHz
AV9170-01, -05	5	<	f_{CLK1}	<	25 MHz

The **AV9170** will only operate correctly within these frequency ranges.

Eliminate High Speed Clock Routing Problems

The **AV9170** makes it possible to route lower speed clocks over long distances on the PC board and to place an **AV9170** next to the device requiring a higher speed clock. The multiplied output can then be used to produce a phase locked, higher speed output clock.

Compensate for Propagation Delays

Including an **AV9170** in a timing loop allows the use of PALs, gate arrays, etc., with loose timing specifications. The **AV9170** compensates for the delay through the PAL and synchronizes the output to the input reference clock.

Operating Frequency Range

The **AV9170** is offered in versions optimized for operation in two frequency ranges. The -01 and -04 cover high frequencies, 20 to 100 MHz. The -02 and -05 operate from 5 to 25 MHz. The **AV9170** can be supplied with custom multiplication factors and operating ranges. Consult ICS for details.

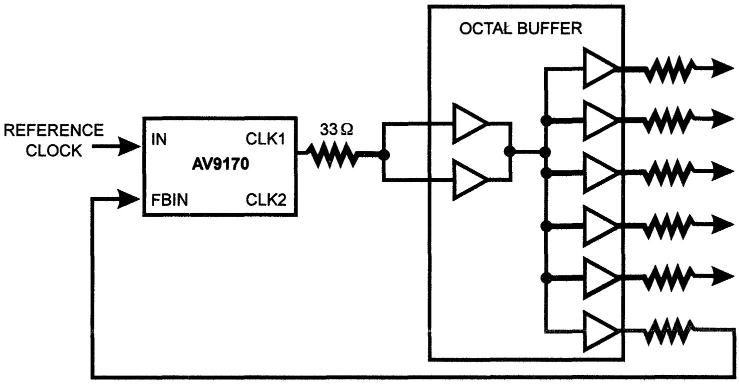


Figure 1: Application of AV9170 for Multiple Outputs

Using CLK2 Feedback

Connecting CLK2 to FBIN as shown in Figure 2 will cause all of the rising edges to be aligned (Figure 4)

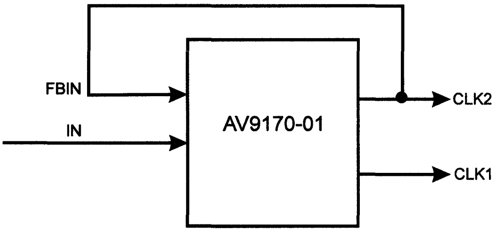


Figure 2

For CLK2 frequencies 10 - 50 MHz (-01)
For CLK2 frequencies 2.5 - 12.5 MHz (-02)

Using CLK1 Feedback

With CLK1 connected to FBIN as shown in Figure 3, the input and CLK1 output will be aligned on the rising edge, but CLK2 can be either rising or falling (Figure 5). Consult ICS if the CLK1 frequency is desired to be higher than 100 MHz.

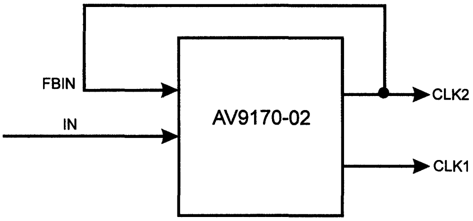


Figure 3

For CLK1 frequencies 20 - 100 MHz (-01)
For CLK1 frequencies 5 - 25 MHz (-02)

Table 2: Decoding Table for AV9170-01, -02 with CLK2 Feedback

FS1	FS0	CLK1	CLK2
0	0	INx4	INx2
0	1	INx8	INx4
1	0	INx2	IN
1	1	INx16	INx8

Table 3: Decoding Table for AV9170-01, -02 with CLK1 Feedback

FS1	FS0	CLK1	CLK2
0	0	INx2	IN
0	1	INx4	INx2
1	0	IN	IN÷2
1	1	INx8	INx4

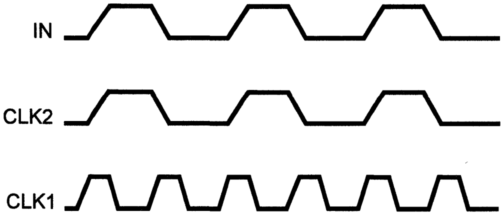


Figure 4: Input and Output Clock Waveforms with CLK2 Connected to FBIN

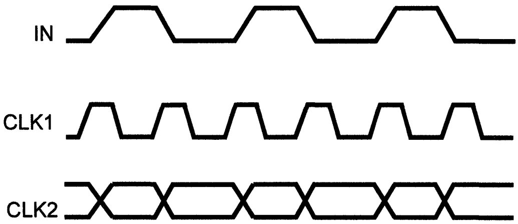


Figure 5: Input and Output Clock Waveforms with CLK1 Connected to FBIN

Using CLK2 Feedback

Connecting CLK2 to FBIN as shown in Figure 2 will cause all of the rising edges to be aligned (Figure 4)

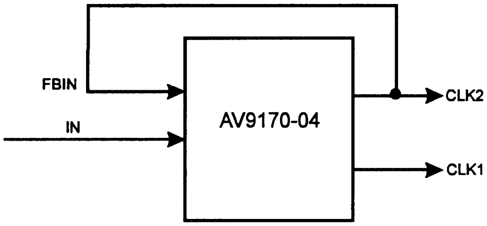


Figure 6

For CLK2 frequencies 10 - 50 MHz (-04)
For CLK2 frequencies 2.5 - 12.5 MHz (-05)

Table 4: Decoding Table for AV9170-04, -05 with CLK2 Feedback

FS1	FS0	CLK1	CLK2
0	0	INx4	INx2
0	1	INx8	INx4
1	0	INx2	IN
1	1	INx16	INx8

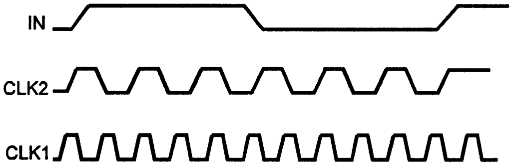


Figure 8: Input and Output Clock Waveforms with CLK2 Connected to FBIN

Using CLK1 Feedback

With CLK1 connected to FBIN as shown in Figure 3, the input and CLK1 output will be aligned on the rising edge, but CLK2 can be either rising or falling (Figure 5). Consult ICS if the CLK1 frequency is desired to be higher than 100 MHz.

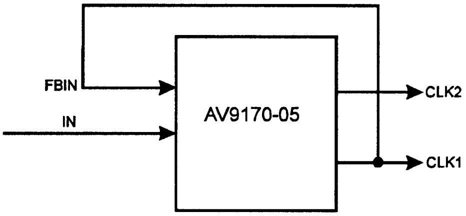


Figure 7

For CLK1 frequencies 20 - 100 MHz (-04)
For CLK1 frequencies 5 - 25 MHz (-05)

Table 5: Decoding Table for AV9170-04, -05 with CLK1 Feedback

FS1	FS0	CLK1	CLK2
0	0	INx2	IN
0	1	INx4	INx2
1	0	IN	IN÷2
1	1	INx8	INx4

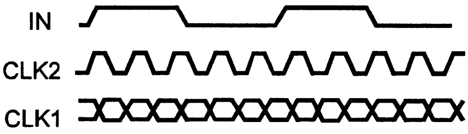


Figure 9: Input and Output Clock Waveforms with CLK1 Connected to FBIN

Absolute Maximum Ratings

VDD referenced to GND 7V
Operating temperature under bias . . . . 0°C to +70°C
Storage temperature . . . . -65°C to +150°C
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V
Power dissipation . . . . 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} = +5V±5%, T_A=0°C to 70°C (unless otherwise stated)

DC/CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD} = 5V	-	-	0.8	V
Input High Voltage	V_{IH}	V_{DD} = 5V	2.0	-	-	V
Input Low Current	I_{IL}	V_{IN} = 0V	-5	-	5	µA
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5	-	5	µA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} =-1mA, V_{DD} = 5.0V	V_{DD}-.4V	-	-	V
Output High Voltage	V_{OH}	I_{OH} =-4mA, V_{DD} =5.0V	V_{DD}-.8V	-	-	V
Output High Voltage	V_{OH}	I_{OH} =-8mA	2.4	-	-	V
Supply Current	I_{DD}	Unloaded, 100 MHz	-	20	50	mA
AC/CHARACTERISTICS						
Input Clock Rise Time	$ICLK_r$		-	-	10	ns
Input Clock Fall Time	$ICLK_f$		-	-	10	ns
Output Rise time, 0.8 to 2.0V	t_r	15pF load	-	1	2	ns
Rise time, 20% to 80%V_{DD}	t_r	15pF load	-	2	4	ns
Output Fall time, 2.0 to 0.8V	t_f		-	1	2	ns
Fall time, 80% to 20% V_{DD}	t_f		-	2	48/52	ns
Output Duty Cycle, AV9170-01	d_t	15pF load. Note 2,3	40	48/52	60	%
Output Duty Cycle, AV9170-02	d_t	15pF load. Note 2,3	45	49/51	55	%
Jitter, 1 sigma	T_{1s}		-200	±120	300	ps
Jitter, absolute	T_{abs}	For CLK1 >10 MHz	-500	±250	500	ps
Jitter, absolute	T_{abs}	For CLK1 <10 MHz	-2%		2	%
Input Frequency	f_i	Note 1	1		67	MHz
Output Frequency CLK1	f_o	AV9170-01, - 04	20		100	MHz
Output Frequency CLK1	f_o	AV9170-01, - 05	5		25	MHz
FBIN to IN skew	t_{skew1}	Note 2,4. Input rise time <5ns	-1	0.4	1	ns
FBIN to IN skew	t_{skew1}	Note 2,4. Input rise time <10ns	-2	0.6	2	ns
CLK1 to CLK2 skew	t_{skew2}	Note 2,4	-1	0.4	1	ns

NOTES:
1. It may be possible to operate the AV9170 outside of these ranges. Consult ICS for your specific application.
2. All AC Specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges.

Ordering Information

AV9170-xxCN8 (8 Lead Plastic DIP (300 mils)
AV9170-xxCS8 (8 Lead SOIC (150 mils)*
AV9170-xxCC8 (8 Lead CERDIP)

Example:

ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width
Package Type
N=DIP (Plastic)
S=SOIC C=CERDIP
Pattern Number (2 or 3 digit number for parts with ROM code patterns)
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS=Standard Device; GSP=Genlock Device; AV=ICS (West Coast)

For the SOIC package, the AV9170-01 is marked ICS70-1 and the AV9170-02 is marked ICS70-2.

Clock Synchronizer and Multiplier

Overview

This **AV9170** Application Note provides theory of operation, application examples, and design hints for the device. It is intended to provide the reader a broader understanding of the device beyond the scope of the **AV9170** data sheet.

Theory of Operation

To gain maximum benefit from the **AV9170**, it is first important to understand how the **AV9170** works.

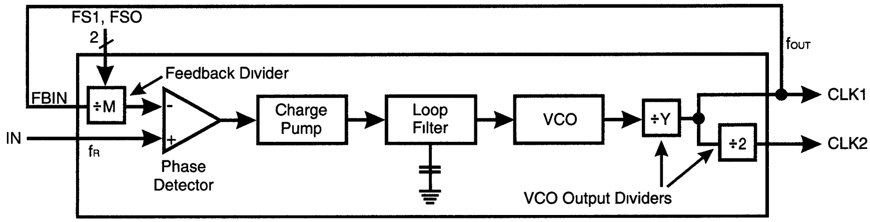
The **AV9170** is a basic PLL (Phase-Locked Loop) analog building block that is optimized for system clock applications. A complete block diagram of the **AV9170**-01/02 is shown in Figure 1. Unlike a simple clock buffer, the **AV9170** contains an internal analog oscillator which generates a clock signal. This clock is kept in phase-lock with an input reference clock by the PLL.

Principles of Phase-Lock Operation

Figure 1 displays a block diagram of a typical phase-locked loop system. The elements of the system are a phase detector, charge pump, loop filter, Voltage Controlled Oscillator (VCO), and divider block.

The VCO is an oscillator whose output clock frequency is proportional to its input voltage. During normal operation, this input voltage to this oscillator is forced to a given value to produce the desired output frequency. The phase detector has two input clocks, one that is the input reference frequency (f_R), and a second that is a scaled version of the output; f_{OUT}/M (M is an integer value). The output of the phase detector is a low frequency signal that is proportional to the phase difference between the rising edges of these two input signals. The phase detector then controls the charge pump. The loop filter converts the output of the charge pump to a voltage and eliminates any high frequency components. The loop filter voltage is the VCO input voltage, completing the loop. The phase-locked loop system causes the frequencies f_R and f_{OUT}/M to be equal. If, for example, f_{OUT}/M drifts to a higher frequency, an error signal is generated by the phase detector to reduce the input voltage to the VCO, causing the output frequency to be forced back to the desired value. Because of this feedback mechanism, a stable output frequency can be synthesized that is proportional to a reference frequency. The relationship between f_{OUT} and f_R can be summarized by the following equation:

$$f_{OUT} = (M)(f_R)$$



FS1	FS0	÷M -01, 02	÷M -04, 05
0	0	2	3
0	1	4	5
1	0	1	6
1	1	8	10

DEVICE	÷Y
AV9170-01, -04	1
AV9170-02, 05	4

Figure 1: AV9170 Complete Block Diagram

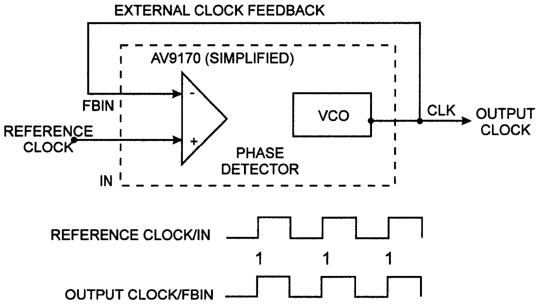


Figure 2: Phase-Locked Loop Principle of AV9170

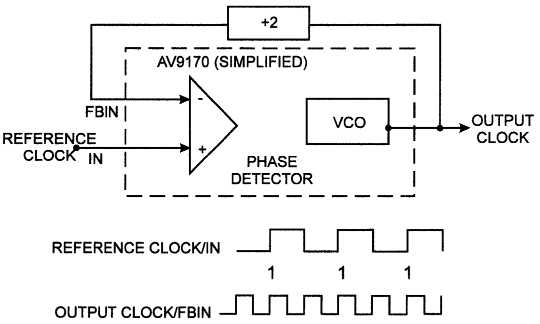


Figure 3: Example of Clock Multiplication by PLL

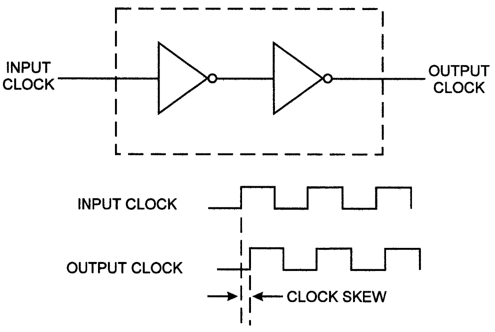


Figure 4a: Example of Delay in Clock Line

Figure 2 shows a simplified block diagram of the **AV9170** and the relationship between the input and output clock when the loop is stable and no feedback division is used. The rising edges of "IN" and "FBIN" will occur within 1ns of each other. Figure 3 illustrates the resulting clock multiplication when a feedback divider (internal or external) is used.

AV9170 VCO Parameters

The **AV9170**'s internal clock oscillator is a VCO that runs optimally over the range of 20-100 MHz. This operation range will provide duty cycle and jitter performance which is guaranteed in the **AV9170** data sheet. In Figure 1 it can be seen that the VCO output can pass through one or two dividers, depending on which output is used. By using these dividers, this 20-100 MHz VCO frequency range can be translated to lower clock output frequencies. For example, the **AV9170-02** can provide final clock output range as low as 1.25-6.25 MHz at CLK2 (the VCO frequency divided by 16).

Actual minimum speed of the **AV9170** VCO operation is about 4 MHz. For example, when no reference clock is present at pin IN, the VCO will slow down to this minimum speed but will not stop.

The **AV9170** loop filter adds the low-pass loop compensation necessary for loop stability. The **AV9170-01** and **AV9170-02** are compensated such that the VCO can make full range frequency changes and settle within approximately 200µsec.

AV9170 Applications

Compensating for Circuit Delay in the Clock Path

Figure 4A illustrates an important problem associated with the distribution of high-speed clocks. Any time the clock signal passes through circuitry (gates, gate arrays, PALs, buffers, etc.) it acquires a time delay. Uncontrolled delays cause the set-up and hold times of various integrated circuits to be violated. Also, race conditions between two signals can be generated when the proper timing sequence is corrupted.

By virtue of the external clock feedback path, the **AV9170** can be used to overcome such circuit delay so that the input and output clocks are in phase with no skew. This is illustrated by Figure 4b. In this circuit, the **AV9170** is actually producing a clock output that is skewed *ahead* of the input reference clock to compensate for the circuit delay. The circuit delay represented in Figure 4b must be constant and continuous for the VCO/PLL to remain in lock. The circuit delay can be of any magnitude (even many clock cycles) and also inverted, but these parameters must remain constant.

Figure 4c shows an example of the **AV9170** used to compensate for clock delay caused by a particular digital IC. In this example, the IC causes clock delay and also internally divides the clock by two. The divide-by-two in the digital IC is compensated for by the feedback loop such that the frequencies at IN and FBIN are identical as selected by FS0 and FS1.

Clock Buffering Using the AV9170

Alone, the **AV9170** is designed to drive loads of up to 25pF. Additional buffering can be accomplished with the simple circuit of Figure 5 (using either an inverting or non-inverting logic buffer). Because of transmission line effects involved when using high speed clocks (standing wave, etc.), it is a good idea to drive only one or two loads per clock driver. It is, therefore, best to use multiple output buffers when driving multiple loads.

Figure 6 shows a multiple output clock buffer implementation using the **AV9170** and an octal buffer IC, such as the 74F240 family. The buffers are cascaded to avoid exceeding the output load capacitance limit of the **AV9170** or the buffer circuits. Since the buffers are all integrated on a single monolithic device, clock delay is typically well matched. Thus, one buffer output can be used for the clock feedback, and then all the outputs are de-skewed to the reference clock. To ensure good phase matching between outputs, it is important that the outputs are similarly loaded (with about the same load capacitance). Optimum results are achieved when the buffer used for clock feedback is used for no other purpose. Otherwise, additional noise and/or standing waves caused by multiple loading could impose unwanted clock jitter or poor skew control characteristics.

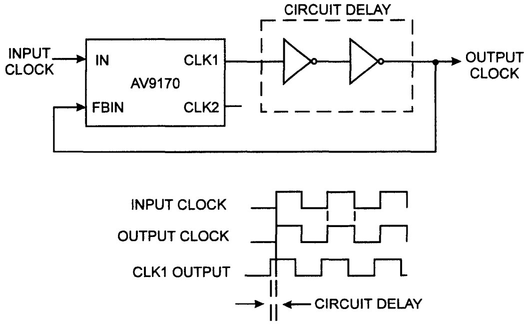


Figure 4b: Overcoming Circuit Delay with the AV9170

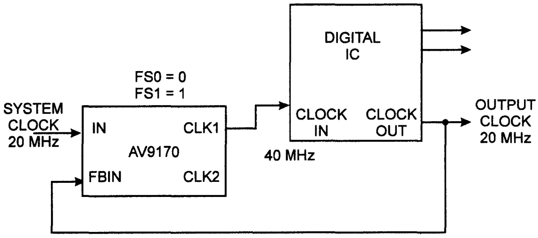


Figure 4c: Example of Restoring Clock Skew with the AV9170

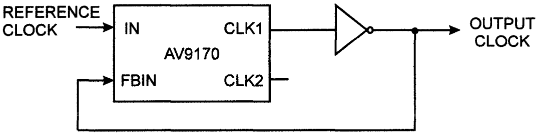


Figure 5: Simple Clock Buffer

Additional Output Clock Frequency Multiplication

Figure 7 illustrates the use of an external divider circuit in the **AV9170** feedback path. By compounding the total divide ratio in the clock feedback path, this can be used to further multiply the VCO or output frequency. This is because the feedback loop maintains the frequency relationship between f_{IN} and f_{FBIN} as described in the data sheet. Input to output skew integrity is not maintained by this circuit, however, due to logic delay in the feedback path. Also keep in mind that VCO frequency must be kept within 20-100 MHz for stable operation. IN and FBIN signal frequencies should be kept within 0.5-67 MHz.

Restoring Clock Duty Cycle

The **AV9170** output clocks, generated by the internal VCO, maintains excellent duty cycle characteristics. Output duty cycle from CLK1 and CLK2 is typically close to 50/50% (logic high time/logic low time), but will be within 40/60-60/40%, as specified in the **AV9170** data sheet. But, because the **AV9170** only responds to rising clock edges at pin IN and FBIN, the device is less sensitive to input duty cycle than most logic chips. Thus, the **AV9170** can be used in applications where duty cycle needs to be restored, as illustrated in Figure 8.

Many digital IC have a specified duty cycle limit on the clock input. Some clock sources, even some crystal oscillators, produce poor duty cycles or output waveforms which can violate these input clock specifications. Such waveforms are acceptable, however, for driving the **AV9170**. This is where using the **AV9170** as a clock buffer can be useful. Duty cycle and clean clock edges are particularly important for those device that utilize both the rising and falling edge of the input clock.

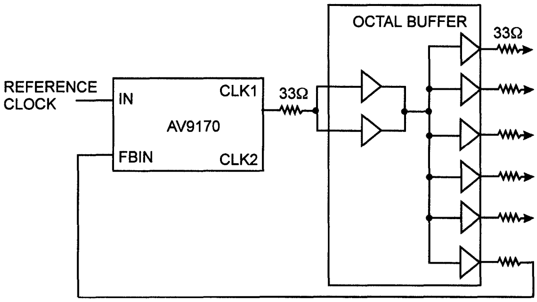


Figure 6: Zero Skew Multiple Output Clock Buffer

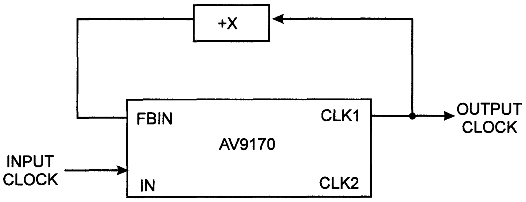


Figure 7: Additional Clock Output Frequency Multiplication by Factor "X"

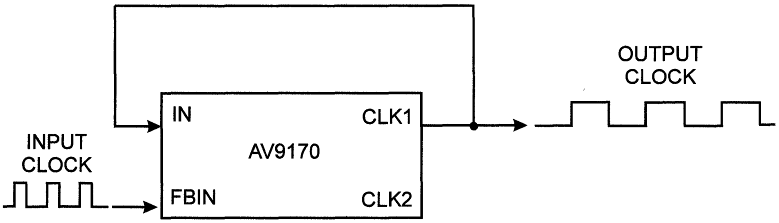


Figure 8: Restoring Clock Duty Cycle

Reducing Clock Distribution Frequency

One of the difficulties with high frequency system clocks is distribution. For example, clocks above 50 MHz or so can be difficult to pass through an edge connector bandwidth limitations. A long, high frequency clock trace can also produce undesirable EMI. One way around these problems is to use a lower clock frequency for distribution and then multiply up the frequency at the destination with the **AV9170**.

Figure 9 illustrates such an application. Here, an AV9155 is used to provide a 2X local CPU clock. The otherwise unused AV9155 1X output clock is used for remote distribution across a board connector. An **AV9170** is then used to create the de-skewed 2X clock at the destination.

Practical Design Considerations

Circuit Skew Rates

For good output skew control, it is important that the circuitry driving IN and FBIN have similar rise times. Fast rise times are safest to avoid false triggering by noise (a fast rise time essentially functions as a low pass filter).

Input threshold voltage of IN and FBIN is typically 1.4 volts (halfway between the Vil and Vih specifications). The outputs CLK1 and CLK2 have a typical rise time of 2ns.

Input Reference Clock Requirements

Since the **AV9170** operation depends on a stable VCO/PLL condition, it can only operate with continuous frequency clock signals. It cannot be applied to non-continuous digital signals. The device will track a changing clock frequency (the VCO can change over its entire range in about 100μsec), but may require about 200μsec to fully lock in, depending on rate of change. In most applications, a few missing clock pulses will not greatly upset the stability of the output clock but may cause cycle slip. These input requirements are true for both the IN and FBIN inputs.

Circuit and Layout Considerations

When using the **AV9170** in a digital system clock application, an inherently sensitive analog IC is placed in an environment with digital noise. Noise is easily coupled into the device via ground and VDD connections and through input and output pins. The **AV9170** is designed to have excellent power supply rejection, but care must be used in circuit design and layout to minimize noise coupling. Using the guidelines given below will help ensure stable, low-jitter clock performance.

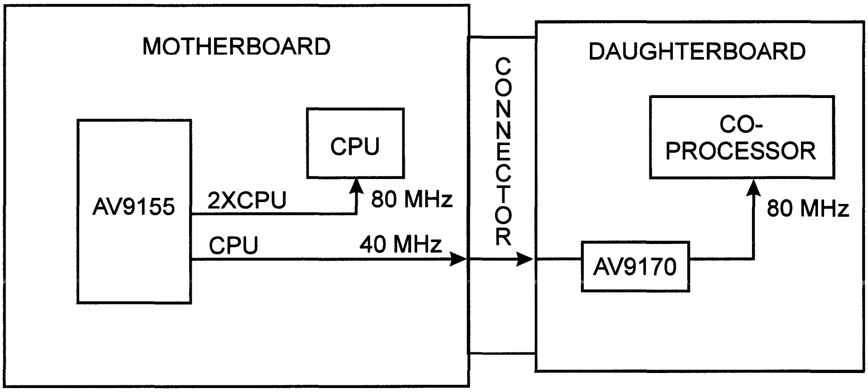


Figure 9: Lower Speed Clock Distribution

For EMI sensitive applications, clock signals are one of the biggest causes for FCC rejection. This is due to their continuous, single-frequency character that is easily picked up in the narrow band emitted frequency test. Following the circuit and layout guidelines below will help reduce EMI.

Figure 10 provides the **AV9170** recommended external circuit, not including any additional feedback circuitry. A single power supply connection should be used to all device pins. The 0.1µF decoupling capacitor should be located as close tot he VDD pin as possible. Above 50 MHz output frequencies, it may be helpful to replace the 0.1µF capacitor with a lower value, such as 0.01µF, to better decouple higher frequencies. The ferrite bead shown in the VDD line does not enhance the **AV9170** performance, but it will reduce EMI radiation from the VDD line caused by **AV9170** dynamic loading. External feedback circuitry should have its own power supply connection and decoupling capacitors.

Except for very short clock output lines going to only one load, it is good practice to use a 33 ohm series termination resistor on the output clock line, as shown in Figure 10. It should be placed close to the **AV9170** output. This will help reduce EMI and apparent clock jitter by damping standing waves caused by wave reflection at the end of the signal trace (which acts as a transmission line).

The recommended **AV9170** PC board layout is shown in Figure 11. The optional 33 ohm output termination resistors or ferrite bead are not shown.

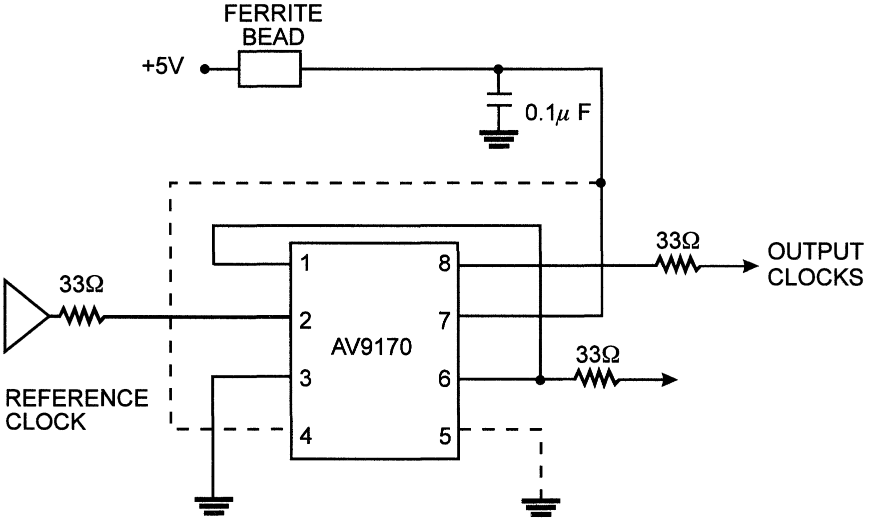


Figure 10: AV9170 Recommended Circuit Configuration
(arbitrary configuration of CLK1 feedback and pin 4, 5 logic states)

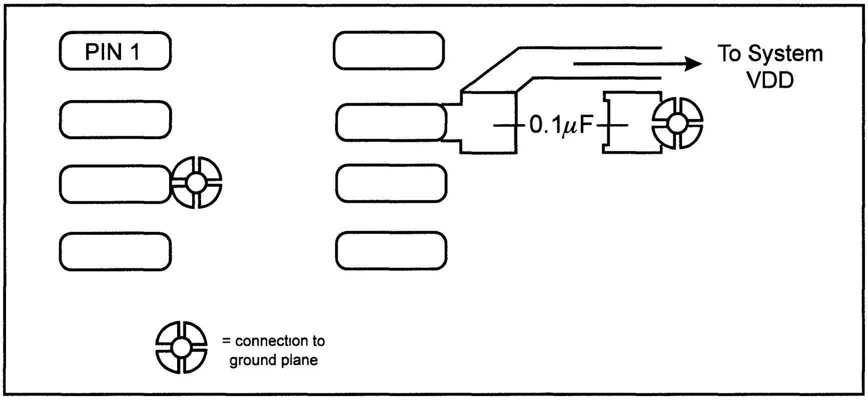


Figure 11: AV9170 Board Layout

Summary

The **AV9170** is extremely flexible and provides utility in a wide range of system clock and other applications, not limited to those discussed in this application note. A related product is the AV9173, which is designed for video genlock (clock recovery) applications. Please refer to the AV9173 data sheet. The **AV9170** may have applications in similar circuits as well. If this application note does not answer all of your **AV9170** questions, please call ICS's applications department.

AV9172

Advance Information

Low Skew Output Buffer

General Description

The **AV9172** is designed to generate low skew clocks for clock distribution in high-performance PCs and workstations. It uses phase-locked loop technology to align the phase and frequency of the output clocks with an input reference clock. Because the input to output skew is guaranteed to ±500ps, the part acts as a "zero delay" buffer.

The **AV9172** has six configurable outputs. The **AV9172-01** version has one output that runs at the same phase and frequency as the reference clock. A second output runs at the same frequency as the reference, but can either be in phase or 180° out of phase from the input clock. Two outputs are provided that are at twice the reference frequency and in phase with the reference clock. The final outputs can be programmed to be replicas of the 2x clocks or non-overlapping two phase clocks at twice the reference frequency. The **AV9172-01** operates with input clocks from 25 MHz to 50 MHz while producing outputs from 25 MHz to 100 MHz.

The use of a phase-locked loop (PLL) allows the output clocks to run at multiples of the input clock. This permits routing of a lower speed clock and local generation of a required high speed clock. Synchronization of the phase relationship between the input clock and the output clocks is accomplished when one output clock is connected to the input pin FBIN. The PLL circuitry matches rising edges of the input clock and output clocks.

Features

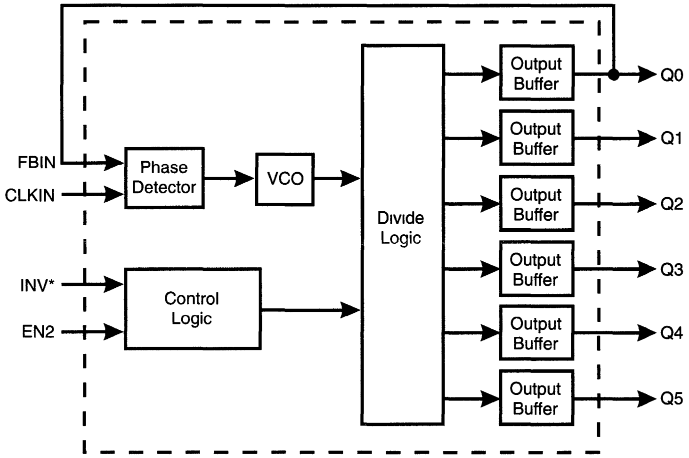
- **AV9172-07** input is 66 MHz with 66 and 33 MHz output buffers
- **AV9172-01** is pin compatible with Gazelle GA1210E
- ±250ps skew (max) between outputs
- ±500ps skew (max) between input and outputs
- Input frequency range from 25 Mhz to 50 MHz
- Output frequency range from 25 MHz to 100 MHz
- Special mode for two-phase clock generation
- Inputs and outputs are fully TTL-compatible
- CMOS process results in low power supply current
- High drive, 25mA outputs
- Low cost
- 16-pin SOIC (300 mil) or 16-pin PDIP package

The **AV9172** is fabricated using CMOS technology which results in much lower power consumption and cost compared with the gallium arsenide-based GA1210E. The typical operating current for the **AV9172** is 50mA versus 120mA for the GA1210E.

ICS offers several versions of the **AV9172**. The different devices are shown below:

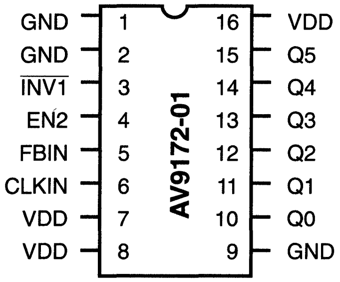
PART	DESCRIPTION
AV9172-01	Second source of GA1210E
AV9172-03	Clock doubler and buffer
AV9172-07	Clock buffer for 66 MHz input

Block Diagram



AV9172RevA093094

Pin Configuration



16-Pin SOIC or 16-Pin PDIP
K-6, K-4

Configuration Table for AV9172-01

EN2	$\overline{\text{INV}}$	Q0	Q1	Q2	Q3	Q4	Q5
0	0	1X	$\overline{\text{1X}}$	2X	2X	2X	2X
0	1	1X	1X	2X	2X	2X	2X
1	0	1X	$\overline{\text{1X}}$	2X	2X	Ø1	Ø2
1	1	1X	1X	2X	2X	Ø1	Ø2

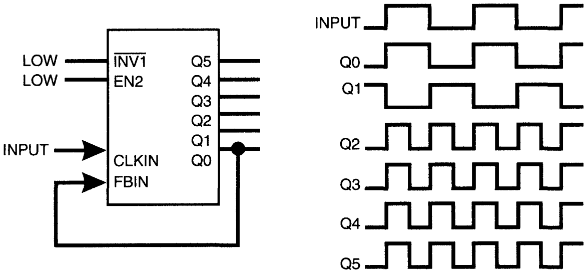
NOTES:
1. 1X designates that the output is a replica of CLKIN
2. 2X designates that the output is twice the frequency of CLKIN, and in phase
3. $\overline{\text{1X}}$ means that the output is at the same frequency and 180°C out of phase (inverted) from CLKIN
4. Ø1 will produce a ¼ duty cycle clock of CLKIN
5. Ø2 will produce a ¼ duty cycle clock delayed 180° from CLKIN

Pin Description for AV9172-01

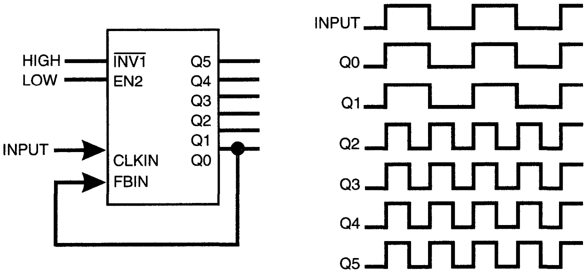
PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	GND	-	GROUND
2	GND	-	GROUND
3	$\overline{\text{INV}}$	Input	$\overline{\text{INV}}$ Inverts Q1 when low
4	EN	Input	EN converts Q4 and Q5 to phase clocks when high
5	FBIN	Input	FEEDBACK INPUT from output Q0
6	CLKIN	Input	INPUT for reference clock
7	VDD	-	Power supply (+5V)
8	VDD	-	Power supply (+5V)
9	GND	-	GROUND
10	Q0	Output	Q0 phase and frequency same as input (1X). Feed back to pin 5.
11	Q1	Output	Q1 is a 1x clock in phase or 180° out of phase with input
12	Q2	Output	Q2 twice the frequency of Q0 (2x)
13	Q3	Output	Q3 twice the frequency of Q0 (2x)
14	Q4	Output	Q4 is either a 2X clock or a two-phase clock - see configuration table
15	Q5	Output	Q5 is either a 2X clock or a two-phase clock - see configuration table
16	VDD	-	Power supply (+5V)

Timing Diagrams for AV9172-01

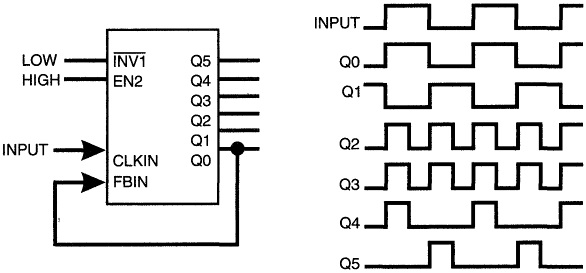
EN2 = 0 $\overline{\text{INV1}}$ = 0
FBIN = Q0



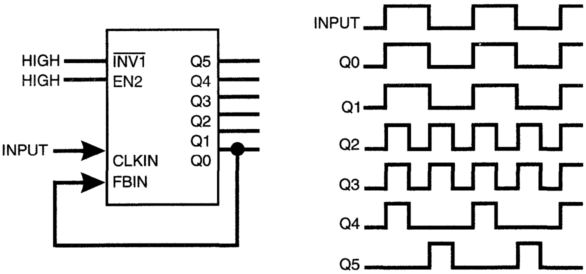
EN2 = 0 $\overline{\text{INV1}}$ = 1
FBIN = Q0



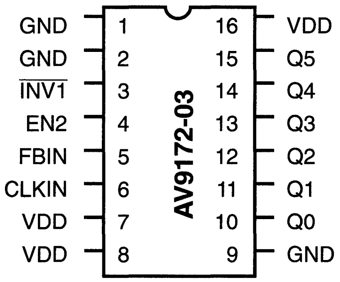
EN2 = 1 $\overline{\text{INV1}}$ = 0
FBIN = Q0



EN2 = 1 $\overline{\text{INV1}}$ = 1
FBIN = Q0



Pin Configuration



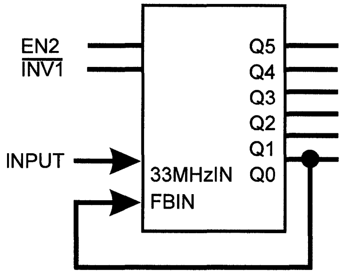
16-Pin SOIC or 16-Pin PDIP
K-6, K-4

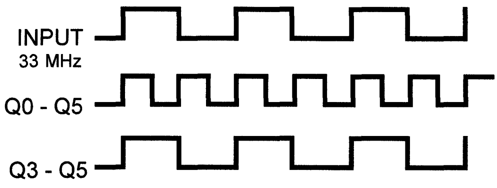
Configuration Table for AV9172-03

(33 MHz input, all frequencies in MHz.)

EN2	INV*	Q0	Q1	Q2	Q3	Q4	Q5
0	0	66	66	66	66	66	66
1	0	66	66	66	66	66	33
0	1	66	66	66	33	33	66
1	1	66	66	66	33	33	33

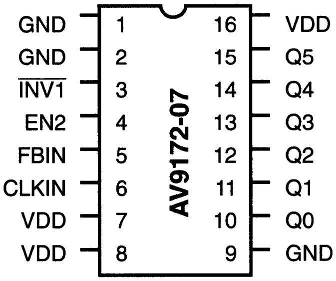
Timing Diagram for AV9172-03





(If 33 MHz modes selected)

Pin Configuration



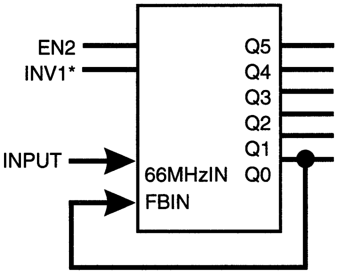
16-Pin SOIC or 16-Pin PDIP
K-6, K-4

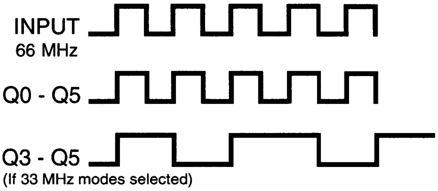
Configuration Table for AV9172-07

(66 MHz input, all frequencies in MHz.)

EN2	INV*	Q0	Q1	Q2	Q3	Q4	Q5
0	0	66	66	66	66	66	66
0	1	66	66	66	66	66	33
1	0	66	66	66	33	33	66
1	1	66	66	66	33	33	33

Timing Diagram for AV9172-07





Absolute Maximum Ratings

VDD referenced to GND 7V
Operating temperature under bias .... 0°C to 70°C
Storage temperature .... -65°C to +150°C
Voltage on I/O pins referenced to GND........... GND -0.5V to VDD +0.5V
Power dissipation .... 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

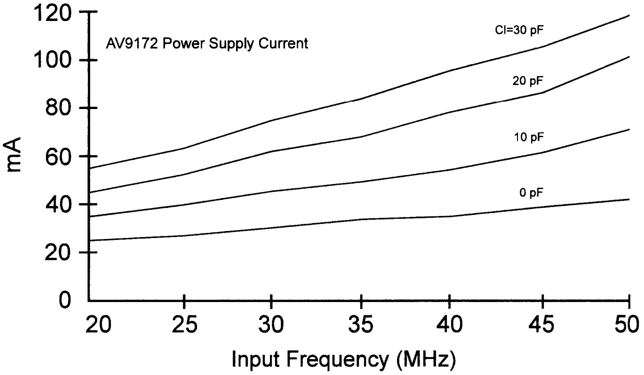
Electrical Characteristics

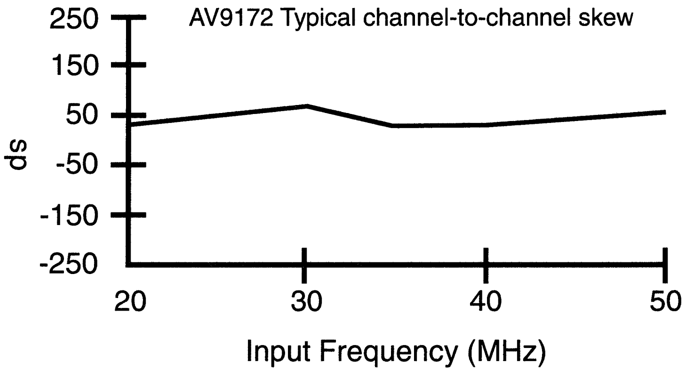
V_{DD} =+5V±5%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD}=5V	-	-	0.8	V
Input High Voltage	V_{IH}	V_{DD}=5V	2.0	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-5	-	5	µA
Input High Current	I_{IH}	V_{IN}=V	-5	-	5	µA
Output Low Voltage	V_{OL}	I_{OL}=25mA	-	0.5	0.8	V
Output High Voltage	V_{OH}	I_{OH}=-25mA	2.4	-	-	V
Supply Current	I_{DD}	Unloaded	-	35	60	mA
AC Characteristics						
Input Clock Rise Time	$ICLK_r$		-	-	10	ns
Input Clock Fall Time	$ICLK_f$		-	-	10	ns
Output Rise time, 0.8 to 2.0V	t_r	15 pf load	-	0.7	1	ns
Rise time, 20% to 80% V_{DD}	t_r	15 pf load	-	1.2	2	ns
Output Fall time, 2.0 to 0.8V	t_f	15 pf load	-	0.7	1	ns
Fall time, 80% to 20% V_{DD}	t_f	15 pf load	-	1.2	2	ns
Output Duty cycle	d_t	15 pf load	45	49/51	55	%
Jitter, 1 sigma	T_{1s}			60		ps
Jitter, absolute	T_{abs}			±200		ps
Input Frequency (-01,-03)	f_i	Note 1	25		50	MHz
Output Frequency (-01,-03)	f_o		25		100	MHz
FBIN to IN skew	t_{skew1}	Note 2, 4. Input rise time < 3ns	-500	-300	500	ps
FBIN to IN skew	t_{skew1}	Note 2, 4. Input rise time < 10ns	1000	-500	1000	ps
Skew between any 2 outputs at same frequency	t_{skew2}	Note 2, 4	-250	±50	250	ps
Skew between any 2 outputs at different frequencies		Note 2, 4			500	ps

NOTES:
1. It may be possible to operate the **AV9172** outside of these ranges. Consult ICS for your specific application.
2. All skew specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges. Loading must be equal on outputs.

Typical Performance Characteristics





Ordering Information

AV9172-01CN16, AV9172-03CN16, AV9172-07CN16 or
AV9172-01CS16, AV9172-03CS16, AV9172-07CS16

Example:

ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or 6" DIP; None=Standard Width

Package Type
N=DIP (Plastic)
M=SOIC S=SOP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device

Integrated
Circuit
Systems, Inc.

AV9173

Video Genlock PLL

General Description

The **AV9173** provides the analog circuit blocks required for implementing a video genlock dot (pixel) clock generator. It contains a phase detector, charge pump, loop filter, and voltage-controlled oscillator (VCO). By grouping these critical analog blocks into one IC and utilizing external digital functions, performance and design flexibility are optimized as are development time and system cost.

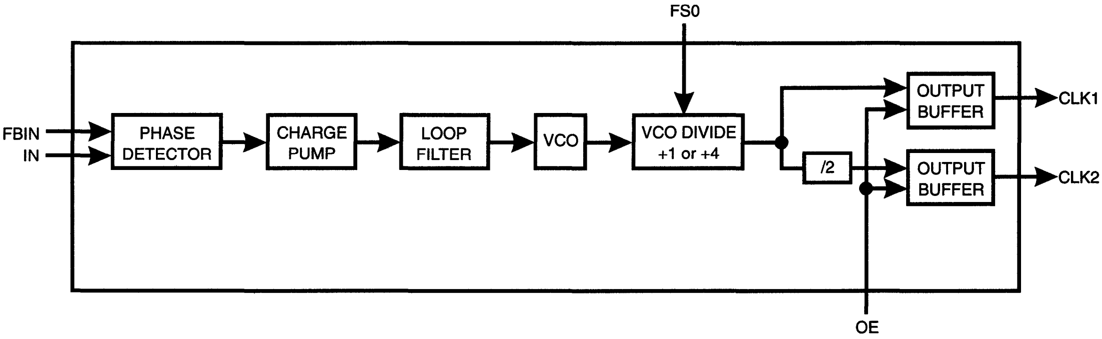
When used with an external clock divider, the **AV9173** forms a Phase-Locked Loop configured as a frequency synthesizer. The **AV9173** is designed to accept video horizontal synchronization (h-sync) pulses and produce a video dot clock. A separated, negative-going sync input reference pulse is required at pin2 (IN).

The **AV9173** is also suited for other clock recovery applications in such areas as data communications.

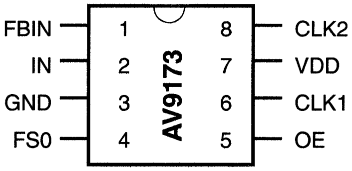
Features

- Phase-detector/VCO circuit block
- Ideal for genlock system
- Reference clock range 25 kHz to 1 MHz
- Output clock range 1.25 to 50 MHz
- On-chip loop filter
- Single 5 volt power supply
- Low power CMOS technology
- Small 8-pin DIP or SOP package

Block Diagram



Pin Configuration



8-Pin DIP or SOP
K-3, K-6

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FBIN	Input	Feedback Input
2	IN	Input	Input for reference sync pulse
3	GND	-	Ground
4	FS0	Input	Frequency Select 0 input
5	OE	Input	Output Enable
6	CLK1	Output	Clock output 1
7	VDD	-	Power supply (+5V)
8	CLK2	Output	Clock output 2 (Divided-by-2 from Clock 1)

Using the AV9173

Most video sources, such as video cameras, are asynchronous, free-running devices. To digitize video or synchronize one video source to another free-running reference video source, a video "genlock" (generator lock) circuit is required. The **AV9173** integrates the analog blocks which make the task much easier.

In the complete video genlock circuit, the primary function of the **AV9173** is to provide the analog circuitry required to generate the video dot clock within a PLL. This application is illustrated in Figure 1. The input reference signal for this circuit is the horizontal synchronization (h-sync) signal. If a composite video reference source is being used, the h-sync pulses must be separated from the composite signal. A video sync separator circuit, such as the national Semiconductor LM1881, can be used for this purpose.

The clock feedback divider shown in Figure 1 is a digital divider used within the PLL to multiply the reference frequency. Its divide ratio establishes how many video dot clock cycles occur per h-sync pulse. For example, if 880 pixel clocks are desired per h-sync pulse, then the divider ratio is set to 880. Hence, together the h-sync frequency and external divider ratio establish the dot clock frequency:

$f_{OUT} = f_{IN} \bullet N$ where N is external divide ratio

Both **AV9173** input pins IN and FBIN respond only to negative-going clock edges of the input signal. The h-sync signal must be constant frequency in the 25 kHz to 1 MHz range and stable (low clock jitter) for creation of a stable output clock.

The output hook-up of the **AV9173** is dictated by the desired dot clock frequency. The primary consideration is the internal VCO which operates over a frequency range of 10 MHz to 50 MHz. Because of the selectable VCO output divider and the additional divider on output CLK2, four distinct output frequency ranges can be achieved. The following table lists these ranges and the corresponding device configuration.

FS0 State	Output Used	Frequency Range
0	CLK1	10 - 50 MHz
0	CLK2	5 - 25 MHz
1	CLK1	2.5 - 12.5 MHz
1	CLK2	1.25 - 6.25 MHz

Note that both outputs, CLK1 nd CLK2, are available during operation even though only one is fed back via the external clock divider.

Pin 5, OE, tristates both CLK1 and CLK2 upon logic low input. This feature can be used to revert dot clock control to the system clock when not in genlock mode (hence, when in genlock mode the system dot clock must be tristated).

When unused, inputs FS0 and OE must be tied to either GND (logic low) or VDD (logic high).

For further discussion of VCO/PLL operation as it applies to the **AV9173**, please refer to the AV9170 application note. The AV9170 is a similar device with fixed feedback dividers for skew control applications.

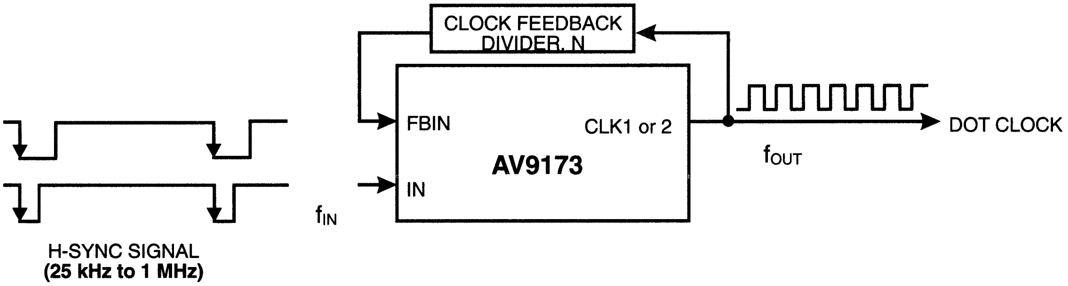


Figure 1: Typical Application of AV9173 in a Video Genlock System

Absolute Maximum Ratings

VDD referenced to GND 7V
Operating temperature under bias . . . . 0°C to +70°C
Storage temperature . . . . -65°C to +150°C
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V
Power dissipation . . . . 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} =+5V± 5%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD}=5V	-	-	0.8	V
Input High Voltage	V_{IH}	V_{DD}=5V	2.0	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-5	-	-	μA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5	-	5	μA
Output Low Voltage	V_{OL}	I_{OL}=8mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1mA, V_{DD}=5.0V	V_{DD}-.4V	-	-	V
Output High Voltage	V_{OH}	I_{OH}=-4mA, V_{DD}=5.0V	V_{DD}-.8V	-	-	V
Output High Voltage	V_{OH}	I_{OH}=-8mA	2.4	-	-	V
Supply Current	I_{DD}	Unloaded, 50 MHz	-	20	50	mA
AC Characteristics						
Input Clock Rise Time	$ICLK_r$	Note 1	-	-	10	ns
Input Clock Fall Time	$ICLK_f$	Note 1	-	-	10	ns
Output Rise Time, 0.8 to 2.0V	t_r	15 pf load	-	1	2	ns
Rise time, 20% to 80%V_{DD}	t_r	15 pf load	-	2	4	ns
Output Fall time, 2.0 to 0.8V	t_f	15 pf load	-	1	2	ns
Fall time, 80% to 20% V_{DD}	t_f	15 pf load	-	2	4	ns
Output Duty Cycle	d_t	15 pf load. Note 1	40	48/52	60	%
Cycle-to-cycle jitter, 1 sigma	T_{1s}		-	120	300	ps
Cycle-to-cycle jitter, absolute	T_{abs}		-500	±250	500	ps
Line-to-line jitter, absolute	TL_{abs}	Note 2		-±4	-	ns
Input Frequency, IN or FBIN	f_i		25	-	1000	kHz
VCO clock speed	f_{VCO}		10	-	50	MHz

NOTES:

1. Duty cycle measured at 1.4V.
2. Input Reference Frequency = 25 kHz, Output Frequency = 25 MHz.

Ordering Information

AV9173-01N8 or AV9173-01S8

Example:

XXX XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
N=DIP (Plastic)
S=SOP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

ICS9175

Low Skew Output Buffer

General Description

The **ICS9175** is designed to generate low skew clocks for clock distribution in high performance PCs and workstations. Using a 14.318 MHz crystal and phase-locked loop technology, six output clocks are produced at a master frequency or one half of the master frequency. The rising edges of the output clocks are guaranteed to be within 250ps of one another.

There are three versions of the **ICS9175**, each designed to support a different Pentium CPU frequency.

Part Number	CPU Frequency
ICS9175-04	66.6
ICS9175-05	60
ICS9175-06	52

The **ICS9175** is ideal for generating multiple, high-drive CPU clocks for Pentium applications. It meets the typical system specification for maximum skew between outputs (250ps) and clock stability (±250ps).

The use of a phase-locked loop allows the output clocks to run at multiples of the input crystal. The patented VCO design is capable of achieving internal frequencies of greater than 150 MHz operation. In the design of the **ICS9175**, the PLL is programmed to produce internal clocks at twice the desired frequency. The output is divided in half at the output to produce symmetric waveforms. Typical duty cycle is 50% ± 1%.

Features

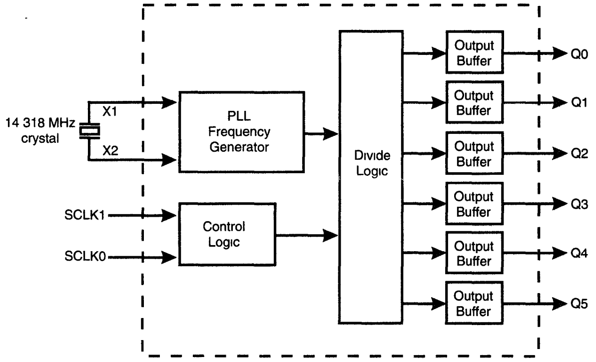
- Generates low skew clocks for Pentium™ microprocessor
- One 14.318 MHz crystal produces six output clocks
- 52 MHz, 60 MHz, and 66 MHz versions available
- ±250ps skew (max) between outputs
- 16-pin SOIC (300 mil) or 16-pin PDIP package
- Inputs and outputs are fully TTL-compatible
- CMOS process results in low power supply current
- High drive, 25mA outputs
- Low cost

The **ICS9175** is capable of producing half speed CPU clocks. Up to three of the six outputs can be configured as half speed CPU clocks. The skew matched circuitry matches rising edges of all CPU clocks and half speed clocks, guaranteeing low skew between outputs.

The **ICS9175** is fabricated using CMOS technology which results in much lower power consumption and cost compared with similar devices based on Gallium arsenide or BiCMOS technology. The typical operating current for the **ICS9175** is 35mA.

The frequencies in the **ICS9175** are mask programmable. Customer specific masks can be made and prototypes delivered within 6-8 weeks from receipt of order. ICS also offers standard versions such as those offered in this data sheet.

Block Diagram



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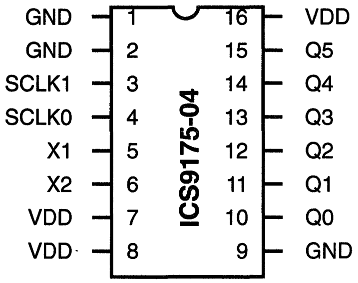
Pin Configuration



16-Pin SOIC or PDIP
K-6, K-4

Configuration Table - ICS9175-04

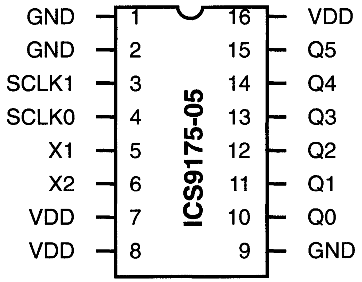
(using 14.318 MHz input)

SCLK1	SCLK0	Q0	Q1	Q2	Q3	Q4	Q5
0	0	66	66	66	66	66	66
0	1	66	66	66	66	66	33
1	0	66	66	66	33	33	66
1	1	66	66	66	33	33	33

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	GND	-	GROUND
2	GND	-	GROUND
3	SCLK1	Input	SCLK1 selects number of ½ speed clocks
4	SCLK0	Input	SCLK0 selects number of ½ speed clocks
5	X1	Input	X1 crystal output
6	X2	Input	X2 crystal output
7	VDD	-	Power supply (+5V)
8	VDD	-	Power supply (+5V)
9	GND	-	GROUND
10	Q0	Output	Q0 is a 66 MHz clock
11	Q1	Output	Q1 is a 66 MHz clock
12	Q2	Output	Q2 is a 66 MHz clock
13	Q3	Output	Q3 can be 66 MHz or 33 MHz clock
14	Q4	Output	Q4 can be 66 MHz or 33 MHz clock
15	Q6	Output	Q5 can be 66 MHz or 33 MHz clock
16	VDD	-	Power supply (+5V)

Pin Configuration



16-Pin SOIC or PDIP
K-6, K-4

Configuration Table - ICS9175-05

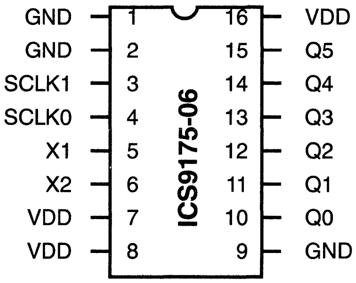
(using 14.318 MHz input)

SCLK1	SCLK0	Q0	Q1	Q2	Q3	Q4	Q5
0	0	60	60	60	60	60	60
0	1	60	60	60	60	60	30
1	0	60	60	60	30	30	60
1	1	60	60	60	30	30	30

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	GND	-	GROUND
2	GND	-	GROUND
3	SCLK1	Input	SCLK1 selects number of ½ speed clocks
4	SCLK0	Input	SCLK0 selects number of ½ speed clocks
5	X1	Input	X1 crystal output
6	X2	Input	X2 crystal output
7	VDD	-	Power supply (+5V)
8	VDD	-	Power supply (+5V)
9	GND	-	GROUND
10	Q0	Output	Q0 is a 60 MHz clock
11	Q1	Output	Q1 is a 60 MHz clock
12	Q2	Output	Q2 is a 60 MHz clock
13	Q3	Output	Q3 can be 60 MHz or 30 MHz clock
14	Q4	Output	Q4 can be 60 MHz or 30 MHz clock
15	Q6	Output	Q5 can be 60 MHz or 30 MHz clock
16	VDD	-	Power supply (+5V)

Pin Configuration



16-Pin SOIC or PDIP
K-6, K-4

Configuration Table - ICS9175-06

(using 14.318 MHz input)

SCLK1	SCLK0	Q0	Q1	Q2	Q3	Q4	Q5
0	0	52	52	52	52	52	52
0	1	52	52	52	52	52	26
1	0	52	52	52	26	26	52
1	1	52	52	52	26	26	26

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	GND	-	GROUND
2	GND	-	GROUND
3	SCLK1	Input	SCLK1 selects number of ½ speed clocks
4	SCLK0	Input	SCLK0 selects number of ½ speed clocks
5	X1	Input	X1 crystal output
6	X2	Input	X2 crystal output
7	VDD	-	Power supply (+5V)
8	VDD	-	Power supply (+5V)
9	GND	-	GROUND
10	Q0	Output	Q0 is a 52 MHz clock
11	Q1	Output	Q1 is a 52 MHz clock
12	Q2	Output	Q2 is a 52 MHz clock
13	Q3	Output	Q3 can be 52 MHz or 26 MHz clock
14	Q4	Output	Q4 can be 52 MHz or 26 MHz clock
15	Q5	Output	Q5 can be 52 MHz or 26 MHz clock
16	VDD	-	Power supply (+5V)

Absolute Maximum Ratings

VDD referenced to GND 7V
Operating temperature under bias .... 0°C to 70°C
Storage temperature .... -65°C to 150°C
Voltage on I/O pins referenced to GND........... GND -0.5V to VDD +0.5V
Power dissipation .... 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} = +5V±5%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD}=5V	-	-	0.8	V
Input High Voltage	V_{IH}	V_{DD}=5V	2.0	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-5	-	5	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5	-	5	µA
Output Low Voltage	V_{OL}	I_{OL}=25mA	-	0.5	0.8	V
Output High Voltage	V_{OH}	I_{OH}=-25mA	2.4	-	-	V
Supply Current	I_{DD}	Unloaded, SCLK=00	-	35	60	mA
AC Characteristics						
Output Rise time, 0.8 to 2.0V	t_r	15 pf load	-	0.7	1	ns
Rise time, 20% to 80%V	t_r	15 pf load	-	1.2	2	ns
Output Fall time, 2.0 to 0.8V	t_f	15 pf load	-	0.7	1	ns
Fall time, 80% to 20% VDD	t_f	15 pf load	-	1.2	2	ns
Output Duty cycle	d_t	15 pf load	45	49/51	55	%
Jitter, 1 sigma	T_{1s}		-	60	-	ps
Jitter, absolute	T_{abs}		-	±200	-	ps
Input Frequency	f_I	Note 1	-	14.318	-	MHz
Output Frequency	f_O		-	-	100	MHz
Skew between any 2 outputs at same frequency	t_{skew2}	Note 2, 4	-250	±50	250	ps
Skew between any 2 outputs at different frequencies		Note 2, 4	-	-	500	ps

NOTES:

1. It may be possible to operate the **ICS9175** outside of these ranges. Consult ICS for your specific application.
2. All skew specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges. Loading must be equal on outputs.

Ordering Information

ICS9175-04CS16 or ICS9175-05CS16 or ICS9175-06CS16 (SOIC)
ICS9175-04CN16 or ICS9175-05CN16 or ICS9175-06CN16 (DIP)

Example:

ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
S=SOIC
N=DIP (Plastic)

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS9176

Low Skew Output Buffer

General Description

The **ICS9176** is designed specifically to support the tight timing requirements of high-performance microprocessors and chip sets. Because the jitter of the device is limited to ±250ps, the **ICS9176** is ideal for clocking Pentium™ systems. The 10 high drive (40mA), low-skew (±250ps) outputs make the **ICS9176** a perfect fit for PCI clocking requirements.

The **ICS9176** has 10 outputs synchronized in phase and frequency to an input clock. The internal phase locked loop (PLL) acts either as a 1X clock multiplier or a 1/2X clock multiplier depending on the state of the input control pins T0 and T1. With metal mask options, any type of ratio between the input clock and output clock can be achieved, including 2X.

The PLL maintains the phase and frequency relationship between the input clock and the outputs by externally feeding back FBOUT to FBIN. Any change in the input will be tracked by all 10 outputs. However, the change at the outputs will happen smoothly so no glitches will be present on any driven input. The PLL circuitry matches rising edges of the input clock and the output clock. Since the input to FBIN skew is guaranteed to ±500ps, the part acts as a "zero delay" buffer.

The **ICS9176** has a total of eleven outputs. Of these, FBOUT is dedicated as the feedback into the PLL and another, Q/2, has an output frequency half that of the remaining nine. These nine outputs can either be running at the same speed as the input, or at half the frequency of the input. With Q/2 as the feedback to FBIN, the nine 'Q' outputs will be running at twice the input frequency in the normal divide-by-1 mode. In this case, the output can go to 120 MHz with a 60 MHz input clock. The maximum rise and fall time of an output is 14ns and each is TTL-compatible with a 40mA symmetric drive.

The **ICS9176** is fabricated using CMOS technology which results in much lower power consumption and cost compared with the gallium arsenide based 1086E. The typical operating current for the **ICS9176** is 60mA versus 115mA for the GA1086E.

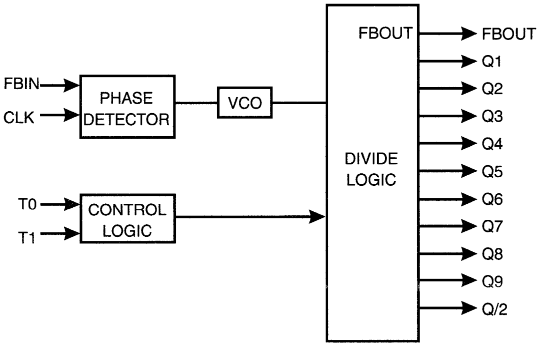
Features

- **ICS9176-01** is pin compatible with Triquint GA1086
- ±500ps skew (max) between input and outputs
- ±250ps skew (max) between outputs
- 10 symmetric, TLL-compatible outputs
- 28-pin PLCC surface mount package
- High drive, 40mA outputs
- Power-down option
- Output frequency range 20 MHz to 120 MHz
- Input frequency range 20 MHz to 100 MHz
- Ideal for PCI bus applications

Selection Table

T1	T0	DESCRIPTION
0	0	Power-down
0	1	Test Mode (PLL Off CLK=outputs)
1	0	Normal (PLL On)
1	1	Divide by 2 Mode

Block Diagram



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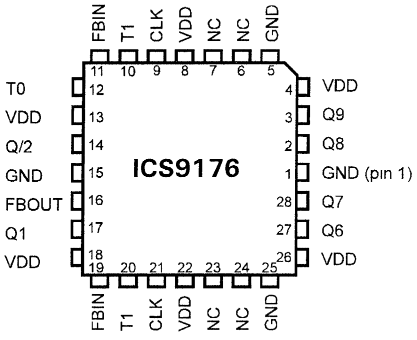
Pin Configuration

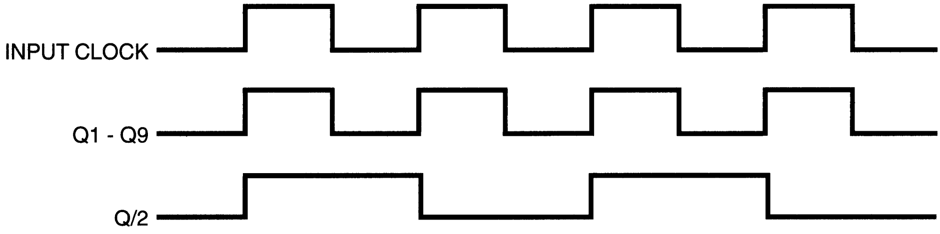


28-Pin PLCC
K-10

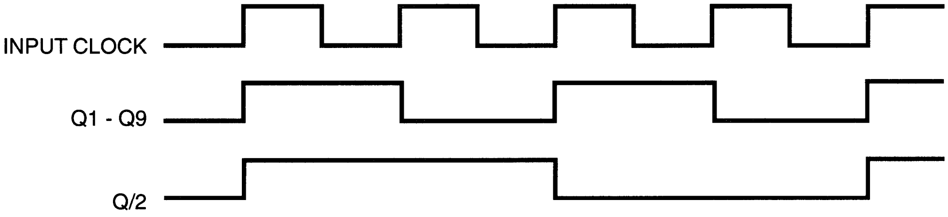
Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	GND	-	GROUND.
2	Q8	Output	Output clock 8.
3	Q9	Output	Output clock 9.
4	VDD	-	Power supply (+5V).
5	GND	-	GROUND.
6	NC	-	No Connect.
7	NC	-	No Connect.
8	VDD	-	Power supply (+5V).
9	CLK	Input	Input for reference clock.
10	T1	Input	T1 selects normal operation, power-down, or test mode.
11	FBIN	Input	FEEDBACK INPUT from output FBOUT.
12	T0	Input	T0 selects normal operation, power-down, or test mode.
13	VDD	-	Power Supply (+5V).
14	Q/2	Output	Half-clock output.
15	GND	-	GROUND.
16	FBOUT	Output	FEEDBACK OUTPUT to Input FBIN.
17	Q1	Output	Output clock 1.
18	VDD	-	Power Supply (+5V).
19	GND	-	GROUND.
20	Q2	Output	Output clock 2.
21	Q3	Output	Output clock 3.
22	VDD	-	Power supply (+5V).
23	Q4	Output	Output clock 4.
24	Q5	Output	Output clock 5.
25	GND	-	GROUND.
26	VDD	-	Power Supply (+5V).
27	Q6	Output	Output clock 6.
28	Q7	Output	Output clock 7.

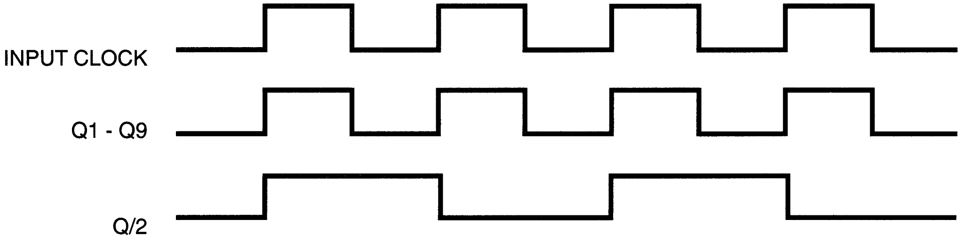
Timing Diagrams



Timing in Divide by 1 Mode

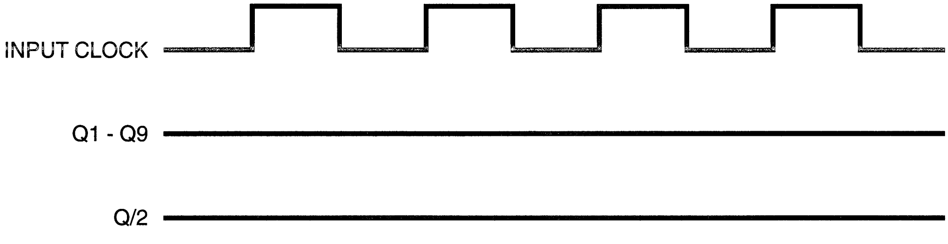


Timing in Divide by 2 Mode



Timing in Eliminate by Test Mode

Note: In test mode, the VCOs are bypassed. The test clock input is simply buffered, then output. The part is transparent. Damage to the device may occur if an output is shorted or forced to ground or VDD.



Timing in Power-down Mode

Absolute Maximum Ratings

VDD referenced to GND	7V
Operating Temperature under bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on I/O pins referenced to GND	GND -0.5V to VDD +0.5V
Power Dissipation	0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

DC Characteristics

V_{DD} = +5V±5%, T_A=0°C to 70°C unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD}=5V	-	-	0.8	V
Input High Voltage	V_{IH}	V_{DD}=5V	2.0	-	-	V
Input Current	I_I	V_{IN}=0V, 5V	-5	-	5	µA
Output Low Voltage	V_{OL}	@I_{OL}=14mA	-	0.25	0.4	V
Output Low Current	I_{OL}	@V_{OL}=0.8V	33	42	-	mA
Output High Voltage	V_{OH}	@I_{OH}=-38mA	2.4	-	-	V
Output High Current	I_{OH}	@V_{OH}=2.0V	-	-59	-41	mA

AC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Pulse Width*	CLK_W	Vdd=4.5V, f_{CLK}=100 MHz	2.5	-	7.5	ns
Output Rise time, 0.8 to 2.0V*	t_r	15 pf load	-	0.7	1	ns
Rise time, 20% to 80% V_{DD}*	t_r	15 pf load	-	1.5	2	ns
Output Fall time, 2.0V to 0.8V*	t_f	15 pf load	-	0.7	1	ns
Fall time, 80% to 20% V_{DD}*	t_f	15 pf load	-	1.2	2	ns
Output Duty cycle*	d_t	15 pf load	45	49/51	55	%
Jitter, 1 sigma*	T_{1s}			60		ps
Jitter, absolute*	T_{abs}		-250	±100	250	ps
Input Frequency	f_I		20		100	MHz
Output Frequency (Q outputs)	f_O		20		120	MHz
FBIN to IN skew	t_{skew1}	Note 1, 3. Input rise time <3ns	-500	250	0	ps
Skew between any 2 outputs at same frequency	t_{skew2}	Note 1, 3.	-250	50	250	ps
Skew between any 1 output and Q/2					3	ns

NOTES:
1. All skew specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
2. Duty cycle measured at 1.4V.
3. Skew measured at 1.4V on rising edges. Loading must be equal on outputs.

* Guaranteed by design and characterization. Not subject to 100% test.

Applications

FBOUT is normally connected to FBIN to facilitate input to output skew control. However, there is no requirement that the external feedback connection be a direct hardwire from an output pin to the FBIN pin. As long as the signal at FBIN is derived directly from the FBOUT pin and maintains its frequency, additional delays can be accommodated. The clock phase of the outputs (rising edge) will be adjusted so that the phase of FBIN and the input clock will be the same. See Figure 1 for an example.

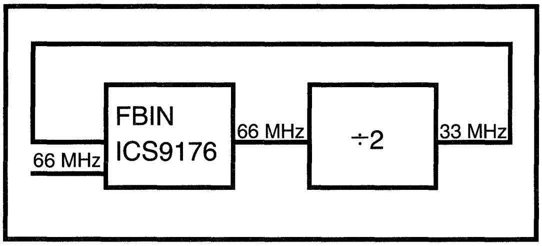


Figure 1

In Figure 1, the propagation delay through the divide by 2 circuit is eliminated. The internal phase-locked loop will adjust the output clock on the **ICS9176** to ensure zero phase delay between the FBIN and CLK signals, as a result, the rising edge at the output of the divide by two circuit will be aligned with the rising edge of the 66 MHz input clock. This type of configuration can be used to eliminate propagation delay as long as the signal at FBIN is continuous and is not gated or conditional.

The **ICS9176** is also ideal for clocking multi-processor systems. The 10 outputs can be used to synchronize the operation of CPU cache and memory banks operating at different speeds. Figure 2 depicts a 2-CPU system in which processors and associated peripherals are operating at 66 MHz. Each of the nine outputs operating at 66 MHz are fully utilized to drive the appropriate CPU, cache and memory control logic. The 33 MHz output is used to synchronize the operation of the slower memory bank to the restart of the system.

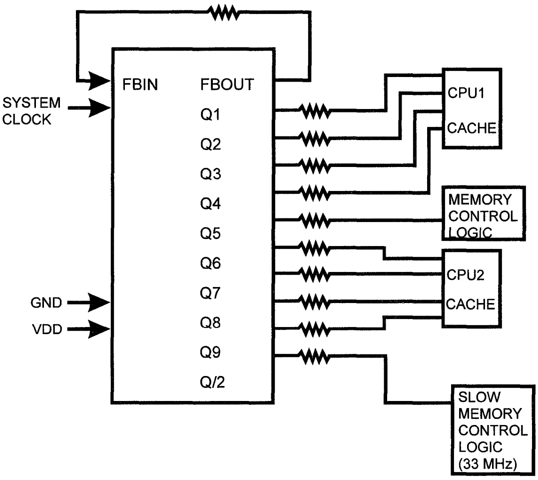


Figure 2

Ordering Information

ICS9176-01CQ28

Example:

ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width
Package Type
Q=PLCC
Pattern Number (2 or 3 digit number for parts with ROM code patterns)
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS9177

Advance Information

High Frequency System Clock Generator

General Description

The **ICS9177** is a multiple output clock generator ideal for high speed processor system applications. A single high-speed internal VCO is utilized to derive up to four simultaneous clock output frequencies. This enables output clock skew matching and the minimization of clock jitter. The internal VCO operates up to 350 MHz providing edge skew matched output clocks.

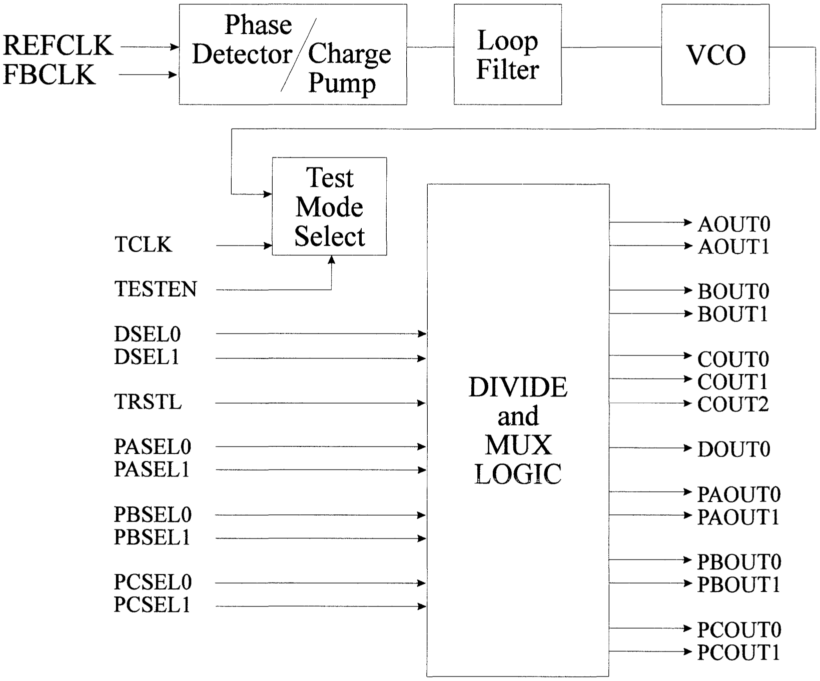
One differential PECL (Positive ECL) output pair provides a high speed processor clock. 12 TTL clock outputs are also provided for other system functions, such as bus clocks. Input selection pins are used to select the TTL output clock frequencies.

For information about **ICS9177** customization optics, please contact ICS.

Features

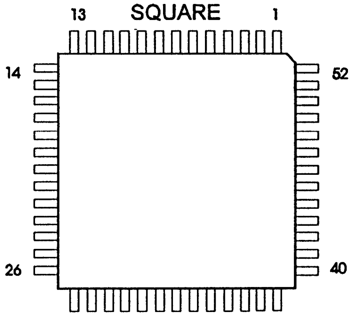
- Provides output frequencies up to 175 MHz
- Internal VCO is divided into four skew-matched output frequencies (Out A, B, C, D)
- External clock feedback provides input to output skew matching
- Differential PECL clock output pair provided for high speed output (Out A)
- 12 TTL clock outputs (for Out B, C, D)
- Single 5 volt power supply voltage
- Internal loop filters
- 52-pin QFP package

Block Diagram



Pin Configuration

52-Pin QFP
K-11



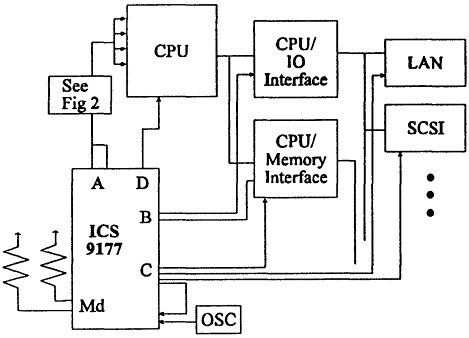
Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	GND		
2	REFCLK	INPUT	from external oscillator
3	FBCLK	INPUT	external PLL Feedback path from one of the OutC outputs
4	$\overline{\text{DSEL1}}$	INPUT	PLL divider mode control (*Contains internal pull-up resistors*)
5	$\overline{\text{DSEL0}}$	INPUT	
6	TESTEN	INPUT	Test mode ENABLE pin
7	TSTCLK	INPUT	External Test Clk
8	NC		
9	VCC		
10	GND		
11	PCOUT1	OUTPUT	TTL - Group 2 Programmable clock outputs
12	PCOUT0	OUTPUT	
13	GND		
14	VCC		
15	PBOUT1	OUTPUT	TTL - Group 1 Programmable clock outputs
16	PBOUT0	OUTPUT	
17	VCC		
18	GND		
19	PAOUT1	OUTPUT	TTL - Group 0 Programmable clock outputs
20	PAOUT0	OUTPUT	
21	VCC		
22	GND		
23	RESETL	INPUT	Low true divider reset pin
24	BOUT1	OUTPUT	TTL - 50 MHz output clock
25	BOUT0	OUTPUT	
26	VCC		
27	GND		

* Internal pull-up resistor

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
28	COUT2	OUTPUT	TTL - 25 MHz output clock
29	COUT1	OUTPUT	
30	VCC		
31	GND		
32	COUT0		TTL - 25 MHz output clock
33	DOUT0		TTL - 12.5 MHz output clock
34	GND		
35	NC		
36	AOUT1	OUTPUT	ECL - 100 MHz, 75 MHz or 50 MHz based on DSEL(1:0) pins
37	AOUT0	OUTPUT	
38	NC		
39	GND		
40	ECL+5V (same as VCC)		
41	NC		
42	NC		
43	ANALOG +5V		
44	ANALOG +5V		
45	AGND		
46	PCSEL1	INPUT	Programmable clock Group C select
47	PCSEL0	INPUT	
48	PBSEL1	INPUT	Programmable clock Group B select
49	PBSEL0	INPUT	
50	PASEL1	INPUT	Programmable clock Group A select
51	PASEL0	INPUT	
52	VC		

Typical System Usage



Example of System Block Diagram - Clocking

D

Function Tables

Table 1: Primary Function Table

REF IN (MHx)	DSEL 1	DSEL 0	RSTL	TEST	f^1	OUT A	OUT B	OUT C	OUT D	DESCRIPTION
25	0	0	1	0	200 MHz	f/4	f/4	f/8	f/16	Mode 0 - 1/1
25	0	1	1	0	300 MHz	f/4	f/6	f/12	f/24	Mode 1 - 3/2
33	1	0	1	0	200/264 MHz	f/2	f/4	f/8	f/16	Mode 2 - 2/1
25	1	1	1	0	X	1	1	1	1	Mode 3 - All 1
-	X	X	0	X	X	0	0	0	0	Reset Mode
-	0	0	1	1	TCLK	f/2	f/2	f/4	f/8	Test Mode 0
-	0	1	1	1	TCLK	f/2	f/3	f/6	f/12	Test Mode 1
-	1	0	1	1	TCLK	f/1	f/2	f/4	f/8	Test Mode 2
-	1	1	1	1	TCLK	f/2	f/2	f/2	f/2	Test Mode 3

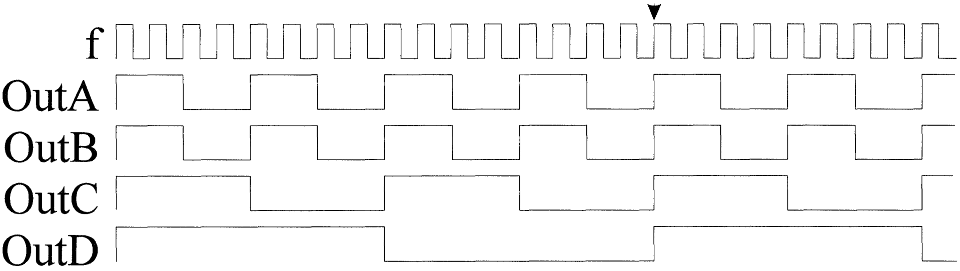
Table 2: CLOCK SELECT Blocks Function Table

PxSEL 1	PxSEL 0	Function of CLOCK SELECT Blocks
0	0	Both outputs at the same frequency as Out **B**.
0	1	Both outputs at the same frequency as Out **C**.
1	0	Both outputs at the same frequency as Out **D**.
1	1	Both outputs disabled in the high state.

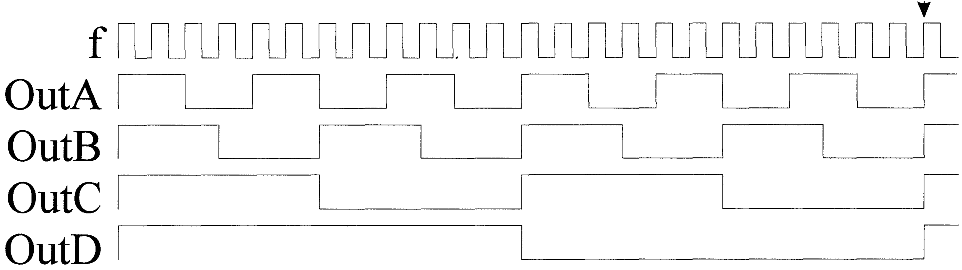
Note: x=A, B, or C. *(See Figure 1.)*

Clock Output Timing Diagrams

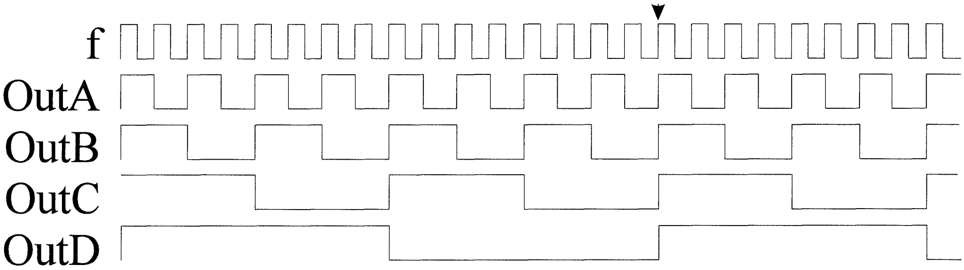
1:1 frequency ratio - Mode 0



3:2 frequency ratio - Mode 1



2:1 frequency ratio - Mode 2



Note: The arrow indicates the point where the clock sequence starts to repeat.

Absolute Maximum Ratings

Supply voltage . . . . 7.0 V
Logic inputs . . . . GND -.05V to VDD +.05V
Ambient operating temp . . . . 0 to 70°C
Storage temperature . . . . -65°C to 150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Power Supply Specifications *(Total Power consumption: approximately 750 mw)*

Table 3: DC Specifications

Supply	I(typ)	I(max)	V(min)	V(typ)	V(max)
VDD	150 mA	200 mA	4.75V	5V	5.25V

AC/DC Input Specification

Table 4: AC Specification of Inputs

Pin Type	Vih(min)	Vil(max)	tr	tf
All	2V	0.8V	3	3

Note: tr and tf are typical values for input

AC/DC Characteristics

Table 5: AC Specification type Out A.pecl Pins *(CPUCLK)*

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage[1]	Voh		3.87		4.67	volts
Output Low Voltage[1]	Vol		2.63		3.19	volts
Output High Current	Ioh		38.7		46.7	ma
Output Low Current	Iol		26.3		31.9	ma
Rise Time 10-90%	tr				1	ns
Fall Time 10-90%	tf				1	ns
Duty cycle at 100 MHz[2, 3]	dcyc		45		55	%

Test Load Conditions: 100Ω, 15 pf.

Note 1: The pecl levels are standard 10 kH positive ECL values as shown in the table above.
Note 2: Pin skew and Duty cycle are measured at the signal swing mid-point.
Note 3: The skew and duty cycle numbers reflect the recommended clock distribution method shown in Figure 2.

Table 6: AC Specification type Out B.ttl Pins *(50 Mhz)*

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	Voh		2.4	3.2	5	volts
Output Low Voltage	Vol		0	0.3	0.8	volts
Output High Current	Ioh		16			ma
Output Low Current	Iol				24	ma
Rise Time 10-90%	tr		1	2	3	ns
Fall Time 10-90%	tf		1	2	3	ns
Pin skew to other OutB.ttl signals[1]	tsk			250	500	ps
Duty cycle at 1.5V	dcyc		45		55	%
Delay from OutA.pecl signals[2]	tdly			.2	.5	ns
Skew associated with above delay[3]	tdlyskw				±0.5	ns

Test Load Conditions: 500Ω, 15 pf.

Note 1: Pin skew is measured from the earliest rising edge of the group to the latest rising edge of the group.

Note 2: Delay is the intrinsic delay between the TTL drivers switching and the PECL driver switching. This is measured from the OutA.pecl signal at the signal swing mid-point to max output of the OutB.ttl signal's rising edge.

Table 7: AC Specification type Out C.ttl Pins *(25 Mhz)*

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	Voh		2.4	3.2	5	volts
Output Low Voltage	Vol		0	0.3	0.8	volts
Output High Current	Ioh		16			ma
Output Low Current	Iol				24	ma
Rise Time 10-90%	tr		1	2	3	ns
Fall Time 10-90%	tf		1	2	3	ns
Pin skew to other OutC.ttl signals[1]	tsk			250	500	ps
Duty cycle at 1.5V	dcyc		45		55	%
Spread to OutB.ttl signals[2]	tspb				500	ps

Test Load Conditions: 500Ω, 15 pf.

Note 1: Pin skew is measured from the earliest rising edge of the group to the latest rising edge of the group.

Note 2: Spread is the absolute difference between the rising edge of any OutC.ttl signal and the rising edge of any OutB.ttl signal.

Table 8: AC Specification type Out D.ttl Pins *(12.5 Mhz)*

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	Voh		2.4	5	3.2	volts
Output Low Voltage	Vol		0	0.8	0.3	volts
Output High Current	Ioh		16			ma
Output Low Current	Iol			24		ma
Rise Time 10-90%	tr		1	3	2	ns
Fall Time 10-90%	tf		1	3	2	ns
Pin skew to other OutD.ttl signals	tsk			500	250	ps
Duty cycle at 1.5V	dcyc		45	55		%
Delay from OutA.pecl signals[1]	tdly			.5		ns
Skew associated with above delay[2]	tdlyskw			±1.3		ns

Test Load Conditions: 500Ω, 15 pf.

Note 1: Delay is the intrinsic delay between the TTL drivers switching and the PECL driver switching. This is measured from the OutA.pecl signal at the signal swing mid-point to max output of the OutD.ttl signal's rising edge.

Ordering Information

ICS9177-01CF52

Example:

ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
F=QFP

Pattern Number (2 or 3 digit number for parts with ROM code patterns, if applicable)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

ICS
High-Performance Products

ICS continues to lead the marketplace in advanced high speed frequency synthesis technology. This issue of the ICS databook includes the addition of high speed PLL clock products for laser engine (ICS1574), and high speed CPU applications (ICS1577), offering system performance to 466 MHz. These products allow the system designer to achieve new levels of pixel resolution with the lowest jitter performance available. Other ICS products address advanced video, multimedia, imaging, and workstation graphics.
As always, ICS High Performance Products offer the designer:

- User Programmable, designer friendly interface feature set.
- Extremely low jitter performance with full device integration.
- Advanced CMOS technology offering the highest speed VCO/PLL performance in the industry.
- Full applications evaluation kits and technical support.

ICS High Performance Products are designed with and for you, the customer, in mind. Our customer dialog is continuous, and we welcome the opportunity to discuss how ICS advanced frequency synthesis capability can solve your high speed system requirements.

ICS High-Performance Product Selection Guide

Product Applications	ICS Device Type	Description	Package Types	Page
Projection LCD **Large-Panel LCD** **Medial Imaging Systems** **Virtual Reality Systems**	ICS1522	User-Programmable Frequencies, 'Line Lock' Capability. 15 kHz to 1 MHz reference to 230 MHz output.	24-Pin SOIC	E-3
Mask Programmed Workstation	ICS1561A	÷2, 4, 8 TTL Out. Integral Loop Filter. Replaces ICS1561 to 230 MHz, ROM-based.	20-Pin DIP, SOIC	E-23
High-Performance Workstation	ICS1562A	User-Programmable Frequencies. RAMDAC Reset Logic (Brooktree compatible) to 400 MHz.	16-Pin Narrow SOIC	E-31
Workstation Clock Generators	ICS1567	32 Frequency ROM-based RAMDAC Reset Logic (Brooktree compatible) to 180 MHz.	20-Pin DIP, SOIC	E-51
Mid-Range Workstation	ICS1572	User-Programmable Frequencies. RAMDAC Reset Logic (Brooktree compatible) to 180 MHz	20-Pin SOIC	E-61
Laser Printers	ICS1574	Laser Engine Pixel Clock to 400 MHz.	16-Pin Narrow SOIC	E-79
Motherboard	ICS1577	DEC Alpha™ CPU Clock to 466 MHz.	14-Pin DIP	E-91
Mid-Range Workstation	ICS2572	User-Programmable Dual PLL. 16V+4M Locations.	20-Pin DIP, SOIC	E-99

Notes:
1. All products have internal loop filters except as noted.
2. All products operate at 5V typ. except as noted.

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ICS1522

Integrated Circuit Systems, Inc.

User-Programmable Video Clock Generator/ Line-Locked Clock Regenerator

Description

The **ICS1522** is a very high performance monolithic phase-locked loop (PLL) frequency synthesizer. Utilizing ICS's advanced CMOS mixed-mode technology, the **ICS1522** provides a low-cost solution for high-end video clock generation where synchronization to an external video source is required.

The **ICS1522** has differential video clock outputs (**CLK+** and **CLK-**) that are compatible with industry standard video DAC.

Operating frequencies are fully programmable with direct control provided for reference divider, feedback divider and post-scaler.

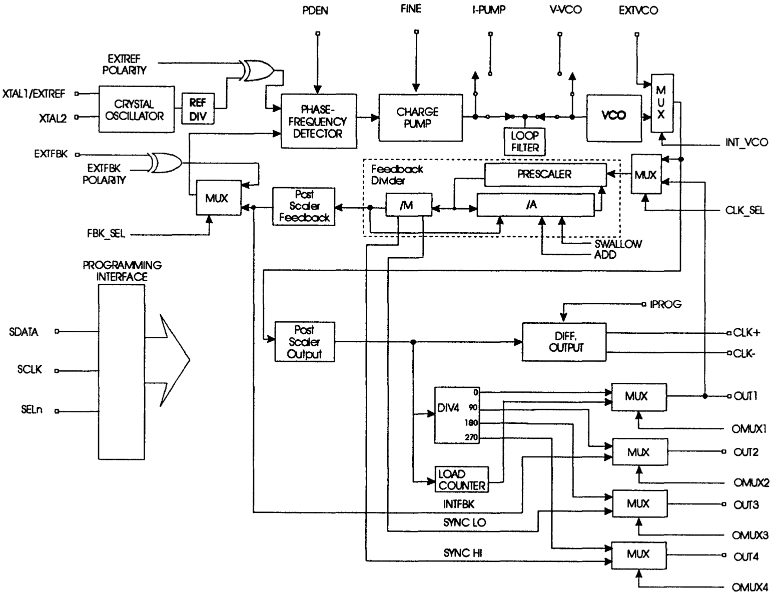
Features

- Serial programming: Feedback and reference divisors, VCO gain, phase comparator gain, relative phase and test modes
- Supports high-resolution graphics - Differential CLK outputs to 230 MHz
- Eliminates need for multiple ECL output voltage controlled crystal oscillators and external components
- Fully-programmable synthesizer capability - not just a clock multiplier
- Line-locked clock generation capability; 15 - 100 kHz
- External feedback loop capability allows graphics system to be used as the feedback divisor with synchronous switchover to internal feedback
- Small footprint 24-pin SOP
- Coarse and fine phase adjustment permits precise clocking in video recovery application

Applications

- LCD Projector Systems
- Multimedia video line locking
- Genlock applications

Block Diagram



Overview

The **ICS1522** is ideally suited to provide the graphics system clock signals required by high-performance video DACs. Fully programmable feedback and reference divider capability allow virtually any frequency to be generated, not just simple multiples of the reference frequency. The **ICS1522** uses the latest generation of frequency synthesis techniques developed by ICS and is completely suitable for the most demanding video applications.

PLL Synthesizer Description - Ratiometric Mode

The **ICS1522** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL (see Block Diagram). The reference frequency is generated by an on-chip crystal oscillator or the reference frequency may be applied to the **ICS1522** from an external frequency source, typically horizontal sync from another display system.

The phase-frequency detector shown in the Block Diagram drives the voltage-controlled oscillator, or VCO, to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F(\mathrm{VCO}) := \frac{F(\mathrm{XTAL1}) \cdot \text{Feedback Divider}}{\text{Reference Divider}}$$

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly programmed dividers).

The VCO gain is programmable, which permits the **ICS1522** to be optimized for best performance at all operating frequencies.

The feedback divider may be programmed for any modulus from 64 to 2048 in steps of one followed by a divide by 1, 2, 4 or 8 feedback post-scaler.

The reference divider may be programmed for any modulus from 1 to 1024 in steps of one.

Output Post-scaler

A programmable post-scaler may be inserted between the VCO and the CLK+ and CLK- outputs of the **ICS1522.** This is useful in generating of lower frequencies, as the VCO has been optimized for high-frequency operation.

The post-scaler allows the selection of dividing the VCO frequency by either 1, 2, 4 or 8.

Load Clock Divider

The **ICS1522** has an additional programmable divider (referred to in the Block Diagram as the load counter) that is used to generate the LOAD clock frequency for the video DAC. The modulus of this divider may be set to 3, 4, 5, 6, 8, or 10 under register control. The design of this divider permits the output duty factor to be 50/50, even when odd modulus is selected. The input frequency to this divider is the output of the output post-scaler described above.

Digital Inputs - ICS1522

The programming of the **ICS1522** is performed serially by using the **SDATA**, **SCLK**, and **SELn** pins to load the 7, 11 bit internal memory locations.

Single bit changes are accomplished by addressing the appropriate memory location and writing only 11 bits of data, not by writing all 77 data bits.

For proper programming of the **ICS1522**, it is important that all transitions of the **SELn** input occur during the same state of the **SCLK** input.

SDATA is shifted into a 15 bit serial register on the rising edge of **SCLK** while **SELn** is low. The first bit loaded is R/Wn followed by a 3 bit address and 11 bit data (both address & data are LSB first). When a rising edge of **SCLK** occurs while **SELn** is high (**SDATA** ignored), the contents of the serial register are loaded into the addressed 11 bit memory location if R/Wn is low. If R/Wn is high upon the above condition, the data from the addressed memory location is loaded into the serial shift register and **SDATA** is set as an output. The 3 bit address and 11 bit data will be serially shifted out of the **ICS1522** on the **SDATA** pin on the rising edge of **SCLK** while **SELn** is low (see Timing Diagram).

An additional control pin on the **ICS1522**, **PDEN** can be used to disable the phase-frequency detector in line-locked applications. When disabled, the phase detector will ignore any inputs and allow the VCO to coast. This feature is useful in systems using composite sync.

Output Description

The differential output drivers, **CLK+** and **CLK-**, are current-mode and are designed to drive resistive terminations in a complementary fashion. The outputs are current-sinking only, with the amount of sink current programmable via the **IPRG** pin. The sink current, which is steered to either **CLK+** or **CLK-**, is four times the current supplied to the **IPRG** pin. For most applications, a resistor from VDDO to IPRG will set the current to the necessary precision.

Reference Oscillator and Crystal Selection

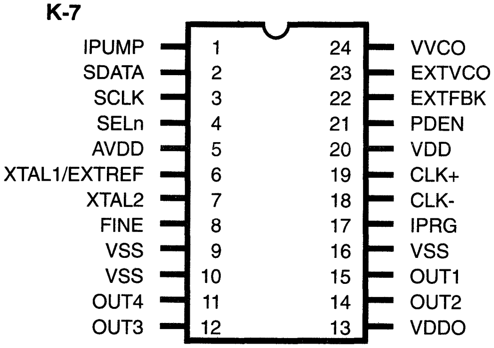
The **ICS1522** has circuitry on-board to implement a Pierce oscillator with the addition of a quartz crystal and two external loading capacitors (EXTREF bit must be set to logic 0). Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode.

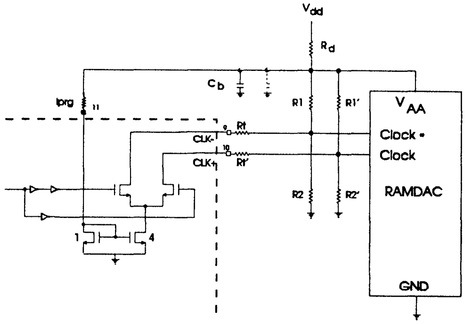
Series-resonant crystals may also be used with the **ICS1522.** Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1522** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

If an external reference frequency source is to be used with the **ICS1522,** it is important that it be jitter-free. The rising and falling edges of that signal should be fast and free of noise for best results. The loop phase is locked to the rising edge of the XTAL1/EXTREF input signal, if REF_POL is set to logic 0. Additionally, the EXTREF bit should be set to logic 1 to switch in a TTL-compatible buffer at this input.

24-Pin SOP
K-7





Typical Output Circuitry Configuration

Line-Locked Operation

Some video applications require a clock to be generated that is a multiple of horizontal sync. The **ICS1522** supports this mode of operation. The reference divider should be set to divide by one and the desired polarity (rising or falling) of lock edge should be selected. By using the phase detector hardware disable mode (PDEN), the PLL can be made to free-run at the beginning of the vertical interval of the external video, and can be reactivated at its completion.

External Feedback Operation

The **ICS1522** option also supports the inclusion of an external counter as the feedback divider of the PLL. This mode is useful in graphic systems that must be "genlocked" to external video sources.

When the FBK_SEL bit is set to logic 0, the phase-frequency detector will use the **EXTFBK** pin as its feedback input. The loop phase will be locked to the rising edges of the signal applied to the EXTFBK input if FBK_POL is set to logic 0 Synchronous switchover to the internal feedback can be accomplished by setting the FBK-SEL bit to logic 1 while an active feedback source exists on the EXTFBK pin.

Fine Phase Adjustment

The **ICS1522** has the capability of adjusting the pixel clock phase relative to the input reference phase. Entire pixels can be added or removed under register control with sub-pixel adjustment accomplished by a control voltage on the FINE input pin. By utilizing the fine phase adjust, after first synchronously switching from external feedback to internal feedback, the graphics system phase can be precisely controlled relative to the input horizontal sync.

Power-On Initialization

The **ICS1522** has an internal power-on reset circuit that sets the frequency of the CLK+and CLK- outputs to be half the crystal or reference frequency assuming that they are between 10 MHz and 25 MHz (refer to default settings in Register Definition). Because the power-on reset circuit is on the VDD supply, and because that supply is filtered, care must be taken to allow the reset to de-assert before programming. A safe guideline is to allow 20 microseconds after the VDD supply reaches four volts.

Board Test Support

It is often desirable to statically control the levels of the output pins for circuit board test. The **ICS1522** supports this through a register programmable mode, AUXEN. When this mode is set, AUXCLK will directly control the logic levels of the CLK+ and CLK- pins while OMUX1, OMUX2, OMUX3, and OMUX4 will control OUT1, OUT2, OUT3 and OUT4, respectively.

Power Supplies and Decoupling

The **ICS1522** has three **VSS** pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). These pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS1522** has a **VDDO** pin which is the supply of +5 volt power to all output drivers. This pin should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, capacitors should have low series inductance and be mounted close to the **ICS1522**.

The **VDD** pin is the power supply pin for the PLL synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	IPUMP	OUT	Charge Pump Output (External loop filter applications)
2	SDATA	IN/OUT	Serial Data Input/Output
3	SCLK	IN	Serial Clock Input
4	SELn	IN	Serial Port Enable (Active Low)
5	AVDD	PWR	Analog +5 Volt Supply
6	XTAL1/EXTREF	IN	External Reference Input / Xtal Oscillator Input
7	XTAL2	OUT	Xtal Oscillator Output
8	FINE	IN	Fine Phase Adjust Input
9	VSS	PWR	Ground
10	VSS	PWR	Ground
11	OUT4	OUT	Output 4
12	OUT3	OUT	Output 3
13	VDDO	PWR	Output Driver +5 Volt Supply
14	OUT2	OUT	Output 2
15	OUT1	OUT	Output 1
16	VSS	PWR	Ground
17	IPRG	IN	Output Driver Current Programming Input
18	CLK-	OUT	Differential CLK- Output
19	CLK+	OUT	Differential CLK+ Output
20	VDD	PWR	Digital +5 Volt Supply
21	PDEN	IN	Phase Detector Enable (Active High)
22	EXTFBK	IN	External Feedback Input
23	EXTVCO	IN	External VCO Input
24	VVCO	IN	VCO Control Voltage Input (External loop filter applications)

ICS1522 Register Definition

REG#	BIT(S)	BIT REF.	DESCRIPTION
0	0-10	F[0:10]	Feedback Divider (Default=04F, Modulus=80) Divides the VCO by the set modulus Modulus Range=64 to 2048; Modulus=Value+1
1	0-7	LO[0:7]	Feedback Sync Pulse LO (Default=03) Feedback Divider output, but with programmable phase; LO[0:7] ≤F[3:10].
2	0-7	HI[0:7]	Feedback Sync Pulse HI (Default=06) Feedback Divider output, but with programmable phase; HI[0:7] ≤F[3:10].
3	0-9	R[0:9]	Reference Divider (Default=013, Modulus=20) Divides the XTAL/EXTREF by the set modulus Modulus Range=1 to 1024; Modulus=Value+1
3	10	REF_POL	External Reference Polarity (Default=0) 0=Positive Edge; 1=Negative Edge
4	0-2	VCO[0:2]	VCO Gain (Default=4)

VCO[2]	VCO[1]	VCO[0]	VCO GAIN
0	0	0	10 MHz/V
0	0	1	15 MHz/V
0	1	0	20 MHz/V
0	1	1	25 MHz/V
1	0	0	45 MHz/V
1	0	1	60 MHz/V
1	1	0	75 MHz/V
1	1	1	90 MHz/V

E

REG#	BIT(S)	BIT REF.	DESCRIPTION
4	3-5	PFD[0:2]	Phase Frequency Detector Gain (Default=3)

PFD[2]	PFD[1]	PFD[0]	PFD GAIN	FINE PHASE ADJ.
0	0	0	.2344uA/2πrad	3ns/V
0	0	1	.9375uA/2πrad	3ns/V
0	1	0	3.750uA/2πrad	3ns/V
0	1	1	15.00uA/2πrad	3ns/V
1	0	0	1.875uA/2πrad	6ns/V
1	0	1	7.500uA/2πrad	6ns/V
1	1	0	30.00uA/2πrad	1.5ns/V
1	1	1	120.0uA/2πrad	.375ns/V

REG#	BIT(S)	BIT REF.	DESCRIPTION
4	6	PDEN	Phase Frequency Detector Enable (Default=1) 0=PFD Disable; 1=PFD Enable
4	7	INT_FLT	Loop Filter Select (Default=1) 0=External Loop Filter (IPUMP & VVCO active) 1=Internal Loop Filter
4	8	INT_VCO	VCO Select (Default=1) 0=External VCO (EXTVCO active) 1=Internal VCO
4	9	CLK_SEL	Feedback Divider Clock Input Select (Default=0) 0=VCO; 1=OUT1
4	10	RESERVED	Must be set to one.
5	0	FBK_SEL	Feedback Select (Default=1) 0=External Feedback (EXTFBK active) 1=Internal Feedback An active external feedback signal at EXTFBK is necessary to synchronously switch to internal.
5	1	FBK_POL	External Feedback Polarity (Default=0) 0=Positive Edge; 1=Negative Edge
5	2	ADD	Addition of 1 VCO Cycle (Default=0) Toggle (0 to 1 to 0) to add 1 VCO cycle.
5	3	SWLW	Removal of 1 VCO Cycle (Default=0) Toggle (0 to 1 to 0) to remove 1 VCO cycle.

REG#	BIT(S)	BIT REF.	DESCRIPTION
5	4-5	PDA[0:1]	Output Post-scaler (Default=0) Input=VCO; Output=Differential Output

PDA[1]	PDA[0]	DIVIDE BY
0	0	8
0	1	4
1	0	2
1	1	1

REG#	BIT(S)	BIT REF.	DESCRIPTION
5	6-7	PDB[0:1]	Feedback Post-scaler (Default=3) Input=Feedback Divider; Output=PFD

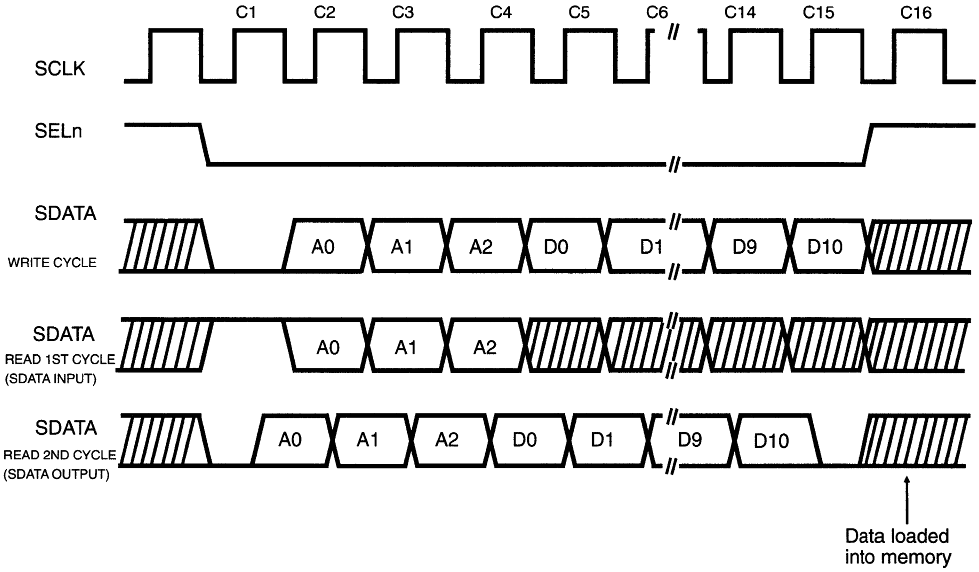
PDB[1]	PDB[0]	DIVIDE BY
0	0	8
0	1	4
1	0	2
1	1	1

REG#	BIT(S)	BIT REF.	DESCRIPTION
5	8	LD_LG	Fine Phase Adjust Lead/Lag (Default=1) 1=FBK will lag REF at input to PFD 0=FBK will lead REF at input to PFD
5	9	F_EN	Fine Phase Adjust Enable (Default=0) 0=Disable; 1=Enable
5	10	RESERVED	Must be set to one.
6	0-2	L[0:2]	Load Counter (Default=7)

L[2]	L[1]	L[0]	DIVIDE BY
0	0	0	3 1-pos, 0-neg
0	0	1	4 pos edge
0	1	0	4 neg edge
0	1	1	5 1-neg, 0-pos
1	0	0	6 pos edge
1	0	1	8 pos edge
1	1	0	8 neg edge
1	1	1	10 neg edge

REG#	BIT(S)	BIT REF.	DESCRIPTION
6	3	OMUX1	OUT1 Select (Default=0) 0=Load Counter Output 1=Diff. Output Divided by 4 at 0 Degrees OUT1 will track OMUX1 when AUXEN=1
6	4	OMUX2	OUT2 Select (Default=0) 0=Internal Feedback Pulse 1=Diff. Output Divided by 4 at 90 Degrees OUT2 will track OMUX2 when AUXEN=1
6	5	OMUX3	OUT3 Select (Default=0) 0=Feedback Sync Pulse LO 1=Diff. Output Divided by 4 at 180 Degrees OUT3 will track OMUX3 when AUXEN=1
6	6	OMUX4	OUT4 Select (Default=1) 0=Feedback Sync Pulse HI 1=Diff. Output Divided by 4 at 270 Degrees OUT4 will track OMUX4 when AUXEN=1
6	7	DACRST	Output Reset (Default=0) When set to one, the CLK+ output is kept high and the CLK- output is kept low. When returned to zero, the CLK+ and CLK- outputs will resume toggling on a rising edge of the OUT1 output (programmed for Load Counter) within +/- 1 clock period.
6	8	AUXEN	Output Test Mode (Default=0) 0=Normal Output Operation 1=Output Test Mode (see OMUX1-4 and AUXCLK)
6	9	AUXCLK	Output Clock when in Test Mode (Default=0) CLK+ and CLK- will track AUXCLK when AUXEN=1
6	10	EXTREF	XTAL/EXTREF Input Buffer (Default=0) 0=Crystal Input Operation 1=External Reference Input Operation

Serial Programming Timing Diagram



NOTES:

1. R/Wn, READ=1 and WRITE=0
2. Address and data transmitted least significant bit first
3. 16 Positive-edge clocks required for complete data read/write
   (1-R/Wn, 3-Address, 11-Data, and 1 load data W/SELn HIGH)
4. SELn's positive and negative transitions must occur on the same state of SCLK
5. An ICS1522 read consists of two consecutive cycles
   (1st cycle - SDATA is an input, 2nd cycle - SDATA is an output)

Absolute Maximum Ratings

V_{DD}, V_{DDO} (measured to V_{SS})	7.0V
Digital Inputs	V_{SS} -0.5 to V_{DD} to 0.5V
Digital Outputs	V_{SS} -0.5 to V_{DDO} to +0.5V
Ambient operating temp	-55 to 125 °C
Storage temperature	-65 to 150 ° C
Junction temperature	175° C
Soldering temperature	260°C

Recommended Operating Conditions

V_{DD}, V_{DDO} (measured to V_{SS})	4.75 to 5.25V
Operating Temperature (Ambient)	0 to 70°C

DC Characteristics

TTL-Compatible Inputs

PDEN, EXTFBK, SDATA, SCLK, SELn, and XTAL1/EXTREF (when EXTREF bit set to 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{ih}		2.0	V_{DD} + 0.5	V
Input Low Voltage	V_{il}		V_{SS} - 0.5	0.8	V
Input Hysteresis			.20	.60	V
Input High Current	I_{ih}	$V_{ih} = V_{DD}$	-	10	uA
Input Low Current	I_{il}	$V_{il} = 0.0$	-	200	uA
Input Capacitance	C_{in}		-	8	pf

EXTVCO Input

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	Vxh		3.75	V_{DD} + 0.5	V
Input Low Voltage	Vxl		V_{SS} - 0.5	1.25	

CLK+, CLK- Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Differential Output Voltage			0.6	-	V

OUT1, OUT2, OUT3, OUT4 Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output High Voltage (Ioh=4.0mA)			2.4	-	V
Output Low Voltage (Iol=8.0mA)			-	0.4	V

AC Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
F_{vco}	VCO Frequency	14		230	MHz
F_{xtal}	Crystal Frequency	5		20	MHz
Cpar	Crystal Oscillator Loading Capacitance		20		pF
F_{HSYNC}	Horizontal Sync Rate	15		100	kHz
T_{xhi}	XTAL1 High Time (when driven externally)	8			ns
T_{xlo}	XTAL1 Low Time (when driven externally)	8			ns
T_{JIT}	Phase Jitter (see Note 1)			1	ns
T_{lock}	PLL Acquire Time (to within 1%)			500	µs
I_{dd}	V_{DD} Supply Current		15		mA
I_{ddo}	VDDO Supply Current (excluding CLK+/– termination)		20		mA
	ANALOG INPUTS				
T_{FINE}	Fine Phase Adjustment Range	0		15	ns
V_{FINE}	Control Voltage for FINE	0		5	VDC
	FINE Input Bias Current			20	nA
	Capacitance of FINE Input			100	pf
	Bandwidth of FINE Input (3dB)	0.5		1.5	kHz
	DIGITAL INPUT				
	SELn, SDATA Setup Time	10			ns
	SELn, SDATA Hold Time	10			ns
	SCLK Pulse Width (T_{hi} or T_{lo})	20			ns
	SCLK Frequency			20	MHz
	Phase-frequency detector enable time			50	ns
	Phase-frequency detector disable time			50	ns
	DIGITAL OUTPUTS				
T_{SKEW}	Time Skew between CLK+, CLK–			500	ps
F_{CLK}	CLK+ and CLK– Clock Rate			230	MHz
	GAINS				
VCO	VCO Gain, VCO(0:2)	10		90	MHz/V
PFD	Phase Detector Gain, PFD (0:2)	.23		120	µA/2πrad

Note 1: T_{JIT} is the total uncertainty of the phase measured at the start of a video line on a 350 MHz oscilloscope under these conditions: HSYNC pin driven with crystal oscillator at 48.363 kHz; F_{VCO} = 65.000 MHz; M =0 (divide by 1 on the output; and N = 1343 (1344 clocks per line).

Memory Definition

ICS1522 memory is loaded serially with the least significant bit clocked into the device first. After the R/Wn bit, the next three bits of the programming word (15 bits) hold the memory location to be loaded. The least significant 11 bits are the data to be loaded (see Timing Diagram).

MEMORY ADDRESS	DATA BITS	DEFAULT VALUES (HEX)	NAME	DESCRIPTION
000	0-10	04F	F(0:10)	Feedback Divider Modulus (Modulus = Value +1)
001	0-7	03	LO(0:7)	M Counter Lo Sync State
001	8-10	0		Don't Care
010	0-7	06	HI(0:7)	M Counter Hi Sync State
010	8-10	0		Don't Care
011	0-9	013	R(0:9)	Reference Divider Modulus (Modulus = Value + 1)
011	10	0	REF_POL	External Reference Polarity (1 =Invert)
100	0-2	4	VCO(0:2)	VCO Gain
100	3-5	3	PFD(0:2)	Phase Detector Gain
100	6	1	PDEN	Phase Detector Enable (1 =Enable)
100	7	1	INT_FLT	Internal Loop Filter (1 = Internal)
100	8	1	INT_VCO	Internal VCO (1 = Internal)
100	9	0	CLK_SEL	Internal feedback input clock select (0 = VCO Output)
100	10	1	Reserved	Reserved - Set to One
101	0	1	FBK_SEL	Feedback Select (1 =Internal)
101	1	0	FBK_POL	External Feedback Polarity (1 =Invert)
101	2	0	ADD	Addition of 1 VCO Cycle (0 to 1 = Add)
101	3	0	SWLW	Removal of 1 VCO Cycle (0 to 1 = Swallow)
101	4-5	0	PDA(0:1)	Output Post-Scaler
101	6-7	3	PDB(0:1)	Feedback Post-Scaler
101	8	1	LD_LG	Fine Phase Adj. Lead/Lag (1=Lead)
101	9	0	F_EN	Fine Phase Adj. Enable (1=Enable)
101	10	1	Reserved	Reserved - Set to One
110	0-2	7	L(0:2)	Load Counter
110	3	0	OMUX1	OUT1 Select (0 = Load Cntr, 1 = Div By 4 0Deg)
110	4	0	OMUX2	OUT2 Select (0 = Int Fbk, 1 = Div By 4 90Deg)
110	5	0	OMUX3	OUT3 Select (0 = Sync Lo, 1 = Div By 4 180Deg)
110	6	1	OMUX4	OUT4 Select (0 = Sync Hi, 1 = Div By 4 270Deg)
110	7	0	DACRST	Output Reset (CLK+ = 1, CLK- = 0)
110	8	0	AUXEN	Output Test Mode (1 = Test, See Board Test Support)
110	9	0	AUXCLK	Output Clock When in Test Mode
110	10	0	EXTREF	XTAL/EXTREF Input Buffer (1=EXTREF)

Pixel-by-Pixel Adjustment of Genlocking Phase (ICS1522 Application)

To understand the operation of the pixel-by-pixel phase adjustment feature, imagine that the modulus of the on-chip divider is equivalent to the graphics system overall divide. Also, imagine that the overflow of the internal divider occurs at the same time as the overflow of the graphics system line counter. Initial synchronization is accomplished by switching from the external feedback source (graphics system HSYNC) to the internal feedback. Let us assume that we are now using the internal divider.

Now, imagine that the programmed value of the divider (really a prescaler) is increased by one for a single pass-through that prescaler (think of this as "swallowing" a feedback pulse). We will lose exactly one CLK period of phase in the feedback path. The VCO will speed up momentarily to compensate for that, and re-lock the loop.

In doing so, the graphics system will receive exactly one extra CLK cycle, advancing the phase of the graphics system HSYNC by one CLK period relative to the reference HSYNC. In a similar fashion, we can decrease the programmed value of the prescaler ("adding" a pulse) to retard the phase of the graphics system. Additionally, sub-pixel phase adjustment is provided through varying the voltage at the FINE input pin.

Ordering Information

ICS1522M

Example:

ICS XXXX M

Package Type
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS1522

Application Note

Line-Locked Applications Design Supplement

Line-Locked Applications

The term "Line-Locked" refers to **ICS1522** applications where one of the outputs of the **ICS1522** will be locked to some multiple of a reference frequency provided to it. A typical application of the **ICS1522** is generation of a sampling clock for an A/D converter that is digitizing the video output of a PC. Normally, this sampling clock should be of the same frequency as the clock which generated the video for best performance (fewest artifacts in the reproduction). Such a clock can be generated by the **ICS1522** by using the PC's HSYNC signal as the reference for the **ICS1522** and programming it to multiply that frequency.

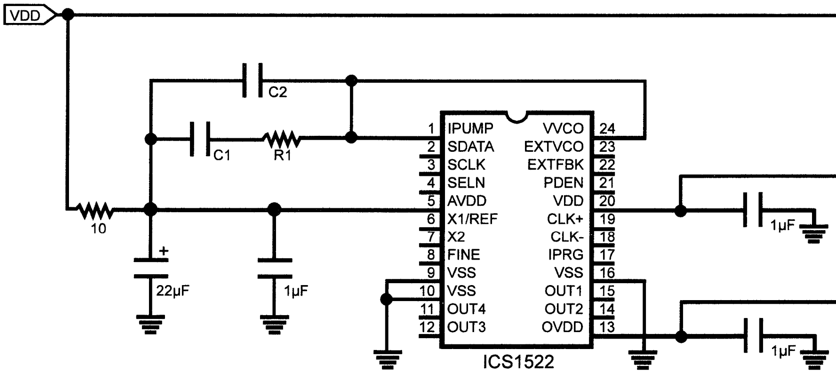
A step-by-step procedure for determining loop filter values and other programmable parameters follows.

Selection of External Components for Line-Locked Applications

ICS generally recommends use of an external loop filter with the **ICS1522** for line-locked applications. The fixed internal loop filter cannot achieve a good compromise over the full range of line-locked applications that the **ICS1522** can handle. Hence, the tuning of the filter values was skewed for normal clock synthesis (similar to ICS1562 "loop tuning"). Much better phase margin and loop damping will be achieved with an external loop filter. This document should help designers quickly arrive at the correct component values for the external loop filter and the correct programming of the device itself. Calculation for Section I is normally done once for a given application, calculation of Sections II & III should be done for all expected cases (or the calculation should be imbedded within the application firmware).

ICS1522 External Loop Filter

Recommended Power Distribution and Filter Configuration



Possible External
Component Values

R1=51k
C1=.01µF
C2= 001µF

(Reg. 4, Bit 7=0)

Approx. Internal
Component Values

R1=120k
C1=110pF
C2=11pF

(Reg 4, Bit 7=1)

PFD & VCO Gains, In addition to the External Loop Filter values, might require adjustment to achieve the desired PLL performance.

I. Calculation of External Loop Filter Component Values

Enter the **lowest** reference frequency that will be used in the application (usually 15 kHz for TV, 31.5 kHz for VGA):

$$F_{reference} = 15 \text{ kHz}$$

We next set the modulus of the Reference Divider. This should always be set to one for a line-locked application:

$$N_{reference} = 1$$

Select the phase detector gain to be used. We recommend that the higher gain settings be used to minimize the resulting impedances of the loop filter components. Normally, set:

PFD_Gain_Setting=6

From the data sheet, we enter the actual value at a setting of 6 into a variable:

$$Gain_{PFD} = \frac{30\mu A}{2\pi rad}$$

We next calculate the value of the resistor in the loop filter as a function of that gain. A good compromise is obtained when:

$$R = \frac{0.33 \text{ volt}}{Gain_{PFD}} \qquad R = 69.115k\Omega$$

... we substitute the nearest 5% value:

$$R = 68K\Omega$$

The value of the capacitor in series with the resistor sets the damping of the loop. Again, a good compromise will be achieved when:

$$C_1 = \frac{50}{2\pi F_{reference} R} \qquad C_1 = 7.802nF$$

... we substitute the nearest 10% value.

$$C_1 = 8.2nF$$

Next, we calculate the value of the capacitor connected in parallel with the series R & C_1 combination:

$$C_2 = \frac{C_1}{100} \qquad C_2 = 82pF$$

This capacitor gives improved high-frequency noise rejection, but is not necessary for loop stability.

II. Calculation of Divider Parameters within the ICS1522

As stated above, the Reference Divider modulus will be set to divided-by-1 in a line-locked application. The Feedback Divider Post-Scaler is also normally set to divide-by-1. The selection of the input source for the Feedback Divider will normally also be set to OUT1. When these options have been set, the phase of one of the OUT1 edges will be aligned with the reference clock. This is normally what is desired. This allows for correct alignment of the pixel boundaries in multiple-byte-per-pixel applications, such as true-color. It also allows for proper alignment of multi-byte interface RAMDAC™ s in line-locked applications, (i.e., the RAMDAC LOAD clock will be consistently aligned with the reference clock).

Next, the Feedback Divider Modulus, LOAD Counter/Divider Modulus (or the modulus of the Divide-by-4, if used instead), Output Post Scaler, and VCO Gain must be selected. First, determine if the line-locked clock frequency is to be taken from the differential CLK outputs of the **ICS1522**, or the OUT1 pin of the **ICS1522**.

II(a). Line-Locked Output Taken from CLK Outputs

If the output is to be taken from the differential CLK outputs, the product of the LOAD Divider Modulus, Feedback Divider Modulus, and Feedback Post-Scaler (=1) must be set equal to the desired number of cycles of the CLK output per reference period. For this example, we assume that 1000 CLK cycles per reference clock is desired, and the RAMDAC used requires the LOAD Counter/Divider Modulus to be 8.

First, we set the modulus of the feedback divider post scaler:

$$N_{feedback\_post\_scaler} = 1$$

Then, we set the number of clocks desired per reference period

$$N_{clocks\_per\_reference} = 1000$$

Next, we set the modulus of the LOAD Counter/Divider (or the modulus of the separate multi-phase divide-by-4, if used):

$$N_{LOAD} = 8$$

RAMDAC is a trademark of Brooktree Corporation

We calculate the required modulus of the feedback divider as:

$$N_{feedback} = \frac{N_{clocks\_per\_reference}}{N_{LOAD} N_{feedback\_post\_scaler}} \quad N_{feedback} = 125$$

The frequency of the CLK output will then be the product of those dividers times the reference frequency:

$$F_{CLK} = F_{reference} N_{feedback} N_{feedback\_post\_scaler} N_{LOAD}$$

$$F_{CLK} = 15\ \mathrm{MHz}$$

That frequency is relatively low for the VCO. We recommend that the VCO be operated at the highest frequency within its range. Therefore, we will set the Output Post-Scaler to divide-by-8.

$$N_{output\_post\_scaler} = 8$$

The VCO frequency can then be calculated:

$$F_{vco} = F_{CLK} N_{output\_post\_scaler} \quad F_{vco} = 120\ \mathrm{MHz}$$

... which is within the VCO maximum frequency limit.

II(b). Line-Locked Output Taken from OUT1 output.

Once again:

$$N_{feedback\_post\_scaler} = 1$$

If the pixel clock is to be taken from the OUT1 output, the product of the Feedback Divider and Feedback Post-Scaler (= 1) must be equal to the desired number of OUT1 clocks per line. Suppose that we want 800 OUT1 cycles per reference clock. We simply then set the Feedback Divider Modulus to be:

$$N_{feedback} = 800$$

Perhaps we would like the frequency of the CLK outputs to be three times the OUT1 frequency (as in a true-color, three-bytes per pixel, application). We would set the LOAD Counter/ Divider Modulus:

$$N_{LOAD} = 3$$

and then the frequency of the CLK outputs will be ...

$$F_{CLK} = F_{reference} N_{feedback} N_{feedback\_post\_scaler} N_{LOAD}$$

$$F_{CLK} = 36\ \mathrm{MHz}$$

Once again, that frequency is relatively low for the VCO. Therefore, we will set the Output Post-Scaler to divide-by-4.

$$N_{output\_post\_scaler} = 4$$

The VCO frequency (for this case) will be:

$$F_{vco} = F_{CLK} N_{output\_post\_scaler} \quad F_{vco} = 144\ \mathrm{MHz}$$

III. Calculation of VCO Gain Required:

We establish the minimum VCO gain needed as the following function of the VCO frequency (using the Fvco calculation of II(b). above):

$$gain_{vco\_minimum} = \frac{F_{vco}}{3.5\ \mathrm{volt}} \quad gain_{vco\_minimum} = 41.143 \frac{\mathrm{MHz}}{\mathrm{volt}}$$

From the data sheet we see that a VCO gain of 4 is the lowest setting that will meet the requirement, and we set the programming value:

$$VCO\_Gain\_Setting = 4$$

We also make a variable that contains that VCO gain value:

$$Gain_{vco} = \frac{45\ \mathrm{MHz}}{\mathrm{volt}}$$

IV. Programming Summary

We now have all of the information that we need to program the **ICS1522**. Summarizing all of the above calculations and using the example shown in IIb above:

$N_{feedback}$=800

$N_{reference}$=1

VCO_Gain_Setting=4

PFD_Gain_Setting=6

We convert the modulus of the Output Post-Scaler, Feedback Post-Scaler, and LOAD Divider/Counter to programming of the PDA, PDB, and L bits respectively by looking it up from the data sheet:

$N_{output\_post\_scaler}$ =4	--- >	PDA =1
$N_{feedback\_post\_scaler}$ =1	--- >	PDB =8
N_{LOAD} =3	--- >	L =0

Other parameters that must be set are (some of these will vary depending on the specifics of the application):

LO =0	< --- sets phase of auxiliary (LO) feedback divider output
HI =0	< --- sets phase of auxiliary (HI) feedback divider output
REF_POL =1	< --- "O" for positive edge locking, "1" for negative edge
PDEN =1	< --- "0" to disable PLL locking, "1" to enable it
INT_FLT =0	< --- selects external loop filter
INT_VCO =1	< --- "0" to substitute external VCO, "1" for internal VCO
CLK_SEL =1	< --- "0" for locking CLK to reference, "1" for locking OUT1 to reference
FBK_SEL =1	< --- "0" for external feedback, "1" for internal feedback
FBK_POL =0	< --- "0" for locking to reference positive edge; "1" for internal feedback
ADD =0	< --- toggle "0" to "1" to "0" to add increment
SWLW =0	< --- "0" for external feedback, "1" for internal feedback
LD_LG =0	< --- "0" causes reference to lag feedback, "1" causes reference to lead feedback when Fine Phase Adjust is enabled
F_EN =0	< --- "0" disables, "1" enables Fine Phase Adjust
OMUX1 =0	< --- "0" for LOAD Divider/ Counter, "1" for multi-phase divide-by-four (0° phase)
OMUX2 =0	< --- "0" for output of internal feedback divider chain, "1" for multi-phase divide-by-four (90° phase)
OMUX3 =0	< --- "0" for feedback sync pulse LO, "1" for multi-phase divide-by-four (180° phase)
OMUX4 =0	< --- "0" for feedback sync pulse HI, "1" for multi-phase divide-by-four (270° phase)
DACRST =0	< --- "0" for normal operation, "1" to reset pipeline delay of Brooktree RAMDACs
AUXEN =0	< --- "0" for normal operation, "1" for output test mode
AUXCLK =0	< --- selects level on CLK outputs when AUXEN ="1"
EXTREF =1	< --- "0" for crystal oscillator, "1" for external reference
RESERVED =1	

V. Calculate Register Values

$R_0 = N_{feedback} - 1$

$R_1 = \text{LO}$

$R_2 = \text{HI}$

$R_3 = (N_{reference} - 1) + \text{REF\_POL } 2^{10}$

$R_4 = (\text{VCO\_Gain\_Setting } 2^{0)} + (\text{PFD\_Gain\_Setting } 2^3) + (\text{PDEN } 2^6) \ldots$
$+ (\text{INT\_FLT } 2^7) + (\text{INT\_VCO } 2^8) + (\text{CLK\_SEL } 2^9) \ldots$
$+ (\text{RESERVED } 2^{10})$

$R_5 = \text{FBK\_SEL} + (\text{FBK\_POL } 2^1) + (\text{ADD } 2^2) + (\text{SWLW } 2^3) + (\text{PDA } 2^4) \ldots$
$+ (\text{PDB } 2^6) + (\text{LD\_LG } 2^8) + (\text{F\_EN } 2^9) + (\text{RESERVED } 2^{10})$

$R_6 = (\text{L } 2^0) + (\text{OMUX1 } 2^3) + (\text{OMUX2 } 2^4) + (\text{OMUX3 } 2^5) + (\text{OMUX4 } 2^6) \ldots$
$+ (\text{DACRST } 2^7) + (\text{AUXEN } 2^8) + (\text{AUXCLK } 2^9) + (\text{EXTREF } 2^{10})$

With the above values:

$R_0 = 799$	or:	$R_0 = 31\text{fh}$
$R_1 = 0$	or:	$R_1 = 1$
$R_2 = 0$	or:	$R_2 = 0$
$R_3 = 1024$	or:	$R_3 = 400\text{h}$
$R_4 = 1908$	or:	$R_4 = 774\text{h}$
$R_5 = 1553$	or:	$R_5 = 611\text{h}$
$R_6 = 1024$	or:	$R_6 = 400\text{h}$

Integrated Circuit Systems, Inc.

ICS1561A

Product Preview

Differential Output PLL Clock Generator

Description

The **ICS1561A** is a very high performance monolithic PLL frequency synthesizer. Utilizing ICS's advanced CMOS mixed mode technology, the **ICS1561A** provides a low cost solution for high-end video clock or Teleclock™ generation.

The **ICS1561A** has differential clock outputs (CLK and CLK*) that are compatible with industry standard video DACs & RAMDACs™. Additional clock outputs, FDIV2, FDIV4 and FDIV8, provide frequencies which are 1/2, 1/4 and 1/8 the main clock frequency.

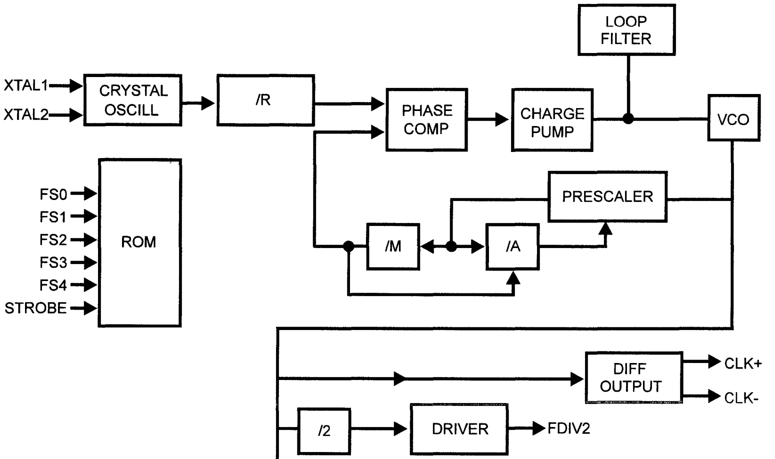
Operating frequencies are selectable from a preprogrammed (customer defined) table. An on-chip crystal oscillator for generating the reference frequency is provided on the **ICS1561A**.

The **ICS1561A-728** is an excellent low-jitter 155.52 MHz Teleclock source for communications systems. When addressed at 19_{10} (13 hex) with a 19.44 MHz reference, the **ICS1561A-728** provides an STS-3 (STM-1) differential clock that is compatible with SONET and ATM transmitters.

Features

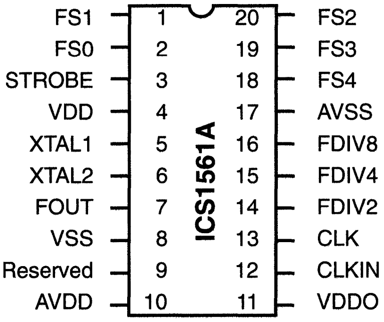
- High Frequency operation for extended video modes - up to 230 MHz
- Compatible with Brooktree high performance RAMDACs
- Low Cost - Eliminates need for multiple ECL crystal clock oscillators in video display subsystems
- Advanced PLL for low phase-jitter
- Dynamic control of VCO sensitivity provides optimized loop gain over entire frequency range
- Strobed/Transparent frequency select options
- Small footprint - 20-pin DIP or SOIC packages available
- Fully backward compatible to ICS1561
- -728 option capable of STS-3/STM-1 communication clock generation

Block Diagram



RAMDAC is a trademark of Brooktree Corporation
Teleclock is a trademark of Integrated Circuit Systems, Inc

Pin Configuration



20-Pin DIP or SOIC
K-4, K-7

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FS1		Frequency select input, TTL compatible
2	FS0		Frequency select input, TTL compatible (LSB)
3	STROBE		Negative edge clock for select inputs, TTL compatible
4	VDD		5V power pin
5	XTAL1		Crystal interface/Ext. oscillator input
6	XTAL2		Crystal interface
7	FOUT		Clock output, TTL compatible
8	VSS		Digital ground
9	Phase-out		Phase comparator output
10	AVDD		Analog VDD input
11	VDDO		Output stage VDD supply pin
12	CLOCKN		Complementary clock output, positive ECL
13	CLOCK		Clock output, positive ECL
14	FDIV2		Clock/2 output, TTL compatible
15	FDIV4		Clock/4 output, TTL compatible
16	FDIV8		Clock/8 output, TTL compatible
17	AVSS		Analog ground
18	FS4		Frequency select input, TTL compatible
19	FS3		Frequency select input, TTL compatible
20	FS2		Frequency select input, TTL compatible

Absolute Maximum Ratings

Supply voltage	V_{DD}	-0.5V to +7V
Ambient operating temp	T_O	0°C to 70°C
Storage temperature	T_S	-85°C to +150°C
Input Voltage	V_{IN}	-0.5V to VDD+0.5V
Output Voltage	V_{OUT}	-0.5V to VDD+0.5V
Clamp Diode Current	V_{IK} & I_{OK}	±30mA
Output Current per Pin	I_{OUT}	±50mA
Power Dissipation	P_D	500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation, it is recommended that Vin and Vout be constrained to >=V_{SS} and <=V_{DD}.

DC Characteristics

(Power Supply Voltage 4.75-5.25 Volts)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD}=5V	V_{SS}		0.8	V
Input High Voltage	V_{IH}	V_{DD}=5V	2.0		V_{DD}	V
Input Leakage Current	I_{IH}	V_{IN}=VDD	-		10	µA
Output Low Voltage	V_{OL}	I_{OL}=8.0mA	-		0.4	V
Output High Voltage	V_{OH}	I_{OH}=4.0mA	2.4		-	V
Supply Current	I_{DD}	V_{DD}=5V	-		30	mA
Internal Pull-up Current	R_{UP}	V_{DD}=5V	25		100	µA
Input Pin Capacitance	C_{IN}	F_C=1MHz	-		8	pf
Output Pin Capacitance	C_{OUT}	F_C=1MHz	-		12	pf

Circuit Description

Overview

The **ICS1561A** is designed to provide the graphics system clock signals required by industry standard RAMDACs. One of 32 pre-programmed (user definable) frequencies may be selected under digital control. Fully programmable feedback and reference divider capability allow virtually any frequency to be generated, not just simple multiples of the reference frequency. The **ICS1561A** uses the latest generation of frequency synthesis techniques developed by ICS and is completely suitable for the most demanding video applications.

Digital Inputs

The FS0-FS4 pins and the STROBE pin are used to select the desired operating frequency from the 32 pre-programmed frequencies in the ROM table of the **ICS1561A**. The FS0-FS4 and STROBE pins are each equipped with a pull-up and will be at a logic HIGH level when not connected.

Transparent Mode - When the STROBE pin is held HIGH, the FS0 through FS4 inputs are transparent; that is, they directly access the ROM table. The synthesizer will output the frequency programmed into the location addressed by the FS0-FS4 pins.

Latched Mode - When the STROBE pin is held LOW, the FS0-FS4 pins are ignored. The synthesizer will output the frequency corresponding to the state of the FS0-FS4 pins when the STROBE pin was last HIGH. In the event that the **ICS1561A** is powered-up with the STROBE pin held LOW, the synthesizer will output the frequency programmed into address 0 (i.e., the one selected with FS0 through FS4 at a logic LOW level).

Divided Dot clock Outputs

The **ICS1561A** has additional outputs which provide a /2, /4 and /8 of the main frequency.

Output Stage Description

The CLK and $\overline{\text{CLK}}$ outputs are each connected to the drains of P-Channel MOSFET devices. The source of each of these devices is connected to VDDO. Typical on resistance of each device is 15 Ohms. These outputs will drive the clock and clock* of a RAMDAC device when a resistive network is utilized.

The divided outputs are high current CMOS type drives.

Frequency Synthesizer Description

The reference frequency is generated by an on-chip crystal oscillator, or the reference frequency may be applied to the **ICS1561A** from an external frequency source.

The **ICS1561A** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL. The phase-frequency detector shown in the block diagram drives the VCO to a frequency that will cause the two inputs to the phase frequency detector to be matched in frequency and phase. This occurs when:

$$F_{(VCO)}= \frac{F(XTAL1) * \text{Feedback Divider}}{\text{Reference Divider}}$$

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly programmed dividers). The divider programming is one of the functions performed by the ROM lookup table in the **ICS1561A**. The VCO gain is also ROM programmable which permits the **ICS1561A** to be optimized for best performance at each frequency in the table.

The feedback divider makes use of a dual modulus prescaler technique that allows construction of a programmable counter to operate at high speeds while still allowing the feedback divider to be programmed in steps of 1. This is an improvement over conventional fixed prescaler architectures that typically impose a factor-of-four penalty (or larger) in this respect.

A post divider may be inserted between the VCO and the CLK and $\overline{\text{CLK}}$ outputs of the **ICS1561A**. This is useful in generation of lower frequencies, as the VCO has been optimized for high frequency operation. Different post divider settings may be used for each frequency in the table.

Application Information

Power Supplies

The **ICS1561A** has a VDDO pin which is the supply of +5 volt power to all output stages. This pin should be connected to the power plane (or bus) using standard high frequency decoupling practice. This decoupling consists of a low series inductance bypass capacitor, using the shortest leads possible, mounted close to the **ICS1561A**.

The AVDD pin is the power supply for the synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects.

Crystal Oscillator and Crystal Selection

The **ICS1561A** has circuitry onboard to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti (also called parallel) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

So-called series resonant crystals may also be used with the **ICS1561A**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.0050.01%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1561A** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

Bus Clock Interface

In some applications, it may be desirable to utilize the bus clock. To do this, connect the clock through a .047uF capacitor to XTAL1 (5) and keep the lead length of the capacitor to XTAL1 (5) to a minimum to reduce noise susceptibility. This input is internally biased at VDD/2. Since TTL compatible clocks typically exhibit a VOH of 3.5V, capacitively coupling the input restores noise immunity. The **ICS1561A** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of the bus clock is typically outside the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. XTAL2 (6) must be left open in this configuration.

ICS1561A Interface

The **ICS1561A** should be located as close as possible to the video DAC or RAMDAC. The differential output CLOCK drivers are current sourcing only and are designed to drive resistive terminations in a complementary fashion. CLK and $\overline{\text{CLK}}$ connections should follow good ECL interconnection practice. Terminating resistors should be as close as possible to the RAMDAC.

ICS1561A Standard Patterns

ICS produces standard frequency patterns for the **ICS1561A**. These patterns include the majority of frequencies most customers require. Custom patterns are also available, although a significant volume commitment and/or one-time mask charge will apply. Contact ICS sales for details.

ICS Part Number	ICS1561A-706	ICS1561A-707	ICS1561A-723	ICS1561A-724	ICS1561A-725	ICS1561A-726	ICS1561A-727	ICS1561A-728
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	12.273	25.144	100.227	100.227	150.340	87.954	119.999	20.045
1	14.560	28.188	104.999	101.911	151.772	80.181	124.090	24.971
2	15.619	32.454	109.963	104.132	154.285	66.818	132.167	30.000
3	25.199	36.060	115.387	106.123	155.590	60.000	136.022	35.000
4	27.862	37.447	119.999	108.181	158.454	49.943	139.999	40.090
5	30.320	39.841	124.958	109.963	160.363	10.090	143.999	44.999
6	31.500	44.822	130.024	111.860	162.272	32.005	147.954	49.943
7	38.571	57.272	135.104	113.703	163.636	24.080	151.772	54.981
8	43.388	64.145	139.999	115.847	165.893	43.977	155.590	59.999
9	50.400	65.082	145.090	117.914	167.999	40.090	160.363	64.982
A	50.664	72.344	149.999	120.000	169.970	33.409	163.636	69.999
B	51.244	74.454	154.636	122.255	171.818	30.000	168.000	74.895
C	54.981	76.363	160.363	124.090	173.553	24.971	171.818	80.181
D	57.272	80.181	164.945	125.999	175.909	20.045	175.909	84.985
E	62.999	84.401	169.970	128.021	178.181	150.000	179.999	89.999
F	64.010	98.181	174.832	130.024	179.999	160.363	183.933	95.215
10	68.727	100.227	179.999	132.167	182.045	169.970	188.181	99.886
11	75.170	107.386	184.704	133.917	183.933	180.000	191.505	104.999
12	88.111	107.807	190.431	136.022	186.136	190.431	196.363	109.963
13	99.272	110.139	194.727	137.975	188.181	200.454	199.772	114.545
14	99.272	111.449	200.454	140.000	190.431	209.999	203.823	119.999
15	100.227	129.818	204.976	141.880	191.505	219.927	208.264	124.958
16	111.531	134.759	209.999	144.000	193.772	230.775	212.245	129.965
17	125.999	139.999	214.772	146.197	196.363	240.000	216.363	134.999
18	139.999	160.363	219.927	147.954	198.545	249.917	219.927	139.999
19	160.363	169.328	225.511	150.340	200.454	259.930	223.721	144.971
1A	179.999	179.999	230.775	151.772	202.140	269.999	227.406	149.790
1B	200.454	200.454	235.119	154.285	203.823	279.999	231.694	154.896
1C	216.363	126.602	239.999	155.590	206.181	289.943	235.828	160.363
1D	59.999	128.021	245.454	158.454	208.264	299.580	239.999	164.945
1E	249.917	132.631	249.917	160.363	209.999	309.793	248.181	169.970
1F	7.860	136.636	255.123	162.272	212.245	PwrDwn	PwrDwn	174.832
Reference Frequency	14.31818 MHz	14.31818 MHz	14.31818 MHz	14.31818 MHz	14.31818 MHz	14.31818 MHz	14.31818 MHz	19.44 MHz

Note: All frequencies above 180 MHz in the standard patterns shown above are experimental and are not guaranteed.

Order info: ICS1561AM-XXX or ICS1561AN-XXX (M = SOIC pkg., N = DIP pkg., XXX = Pattern number)

Ordering Information

ICS1561AN-XXX or ICS1561AM-XXX

Example:

ICS XXXX M -XXX

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  - N=DIP (Plastic)
  - M=SOIC
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  - ICS, AV=Standard Device; GSP=Genlock Device

**Integrated
Circuit
Systems, Inc.**

User Programmable Differential Output Graphics Clock Generator

Description

The **ICS1562A** is a very high performance monolithic phase-locked loop (PLL) frequency synthesizer. Utilizing ICS's advanced CMOS mixed-mode technology, the **ICS1562A** provides a low cost solution for high-end video clock generation.

The **ICS1562A** has differential video clock outputs (CLK+ and CLK-) that are compatible with industry standard video DAC. Another clock output, LOAD, is provided whose frequency is derived from the main clock by a programmable divider. An additional clock output is available, LD/N2, which is derived from the LOAD frequency and whose modulus may also be programmed.

Operating frequencies are fully programmable with direct control provided for reference divider, prescaler, feedback divider and post-scaler.

Reset of the pipeline delay on Brooktree RAMDAC™s may be performed under register control. Outputs may also be set to desired states to facilitate circuit board testing.

Features

- Two programming options:
  ICS1562A-001 (Parallel Programming)
  ICS1562A-201 (Serial Programming)
- Supports high-resolution graphics - CLK output to 260 MHz, with 400 MHz options available
- Eliminates need for multiple ECL output crystal oscillators
- Fully programmable synthesizer capability - not just a clock multiplier
- Circuitry included for reset of Brooktree RAMDAC pipeline delay
- VRAM shift clock generation capability (-201 option only)
- Line-locked clock generation capability
- External feedback loop capability (-201 option only)
- Compact - 16-pin 0.150" skinny SOIC package
- Fully backward compatible to ICS1562

Simplified Block Diagram - ICS1562A

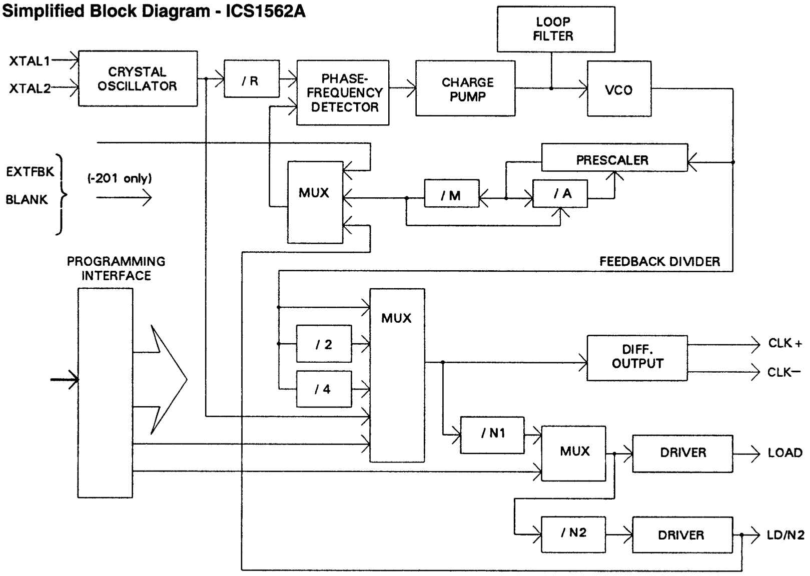
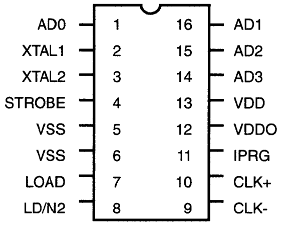


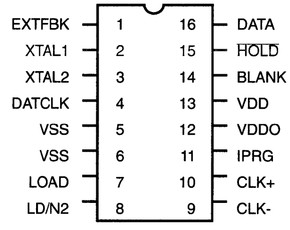
Figure 1

ICS1562A - 001 Pinout



**16-Pin SOIC
K-6**

ICS1562A - 201 Pinout



**16-Pin SOIC
K-6**

RAMDAC is a trademark of Brooktree Corporation

Overview

The **ICS1562A** is ideally suited to provide the graphics system clock signals required by high-performance video DACs. Fully programmable feedback and reference divider capability allow virtually any frequency to be generated, not just simple multiples of the reference frequency. The **ICS1562A** uses the latest generation of frequency synthesis techniques developed by ICS and is completely suitable for the most demanding video applications.

PLL Synthesizer Description - Ratiometric Mode

The **ICS1562A** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL (see Figure 1). The reference frequency is generated by an on-chip crystal oscillator or the reference frequency may be applied to the **ICS1562A** from an external frequency source.

The phase-frequency detector shown in the block diagram drives the voltage-controlled oscillator, or VCO, to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F(\text{VCO}) := \frac{F(\text{XTAL1}) \cdot \text{Feedback Divider}}{\text{Reference Divider}}$$

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly programmed dividers).

The VCO gain is programmable, which permits the **ICS1562A** to be optimized for best performance at all operating frequencies.

The reference divider may be programmed for any modulus from 1 to 128 in steps of one.

The feedback divider may be programmed for any modulus from 37 through 448 in steps of one. Any even modulus from 448 through 896 can also be achieved by setting the "double" bit which doubles the feedback divider modulus. The feedback divider makes use of a dual-modulus prescaler technique that allows the programmable counters to operate at low speed without sacrificing resolution. This is an improvement over conventional fixed prescaler architectures that typically impose a factor-of-four penalty (or larger) in this respect.

Table 1 permits the derivator of "A" & "M" converter programming directly from desired modulus.

PLL Post-Scaler

A programmable post-scaler may be inserted between the VCO and the CLK+ and CLK- outputs of the **ICS1562A**. This is useful in generating lower frequencies, as the VCO has been optimized for high-frequency operation.

The post-scaler allows the selection of:

- VCO frequency
- VCO frequency divided by 2
- VCO frequency divided by 4
- Internal register bit (AUXCLK) value

Load Clock Divider

The **ICS1562A** has an additional programmable divider (referred to in Figure 1 as the N1 divider) that is used to generate the LOAD clock frequency for the video DAC. The modulus of this divider may be set to 3, 4, 5, 6, 8, 10, 12, 16 or 20 under register control. The design of this divider permits the output duty factor to be 50/50, even when an odd modulus is selected. The input frequency to this divider is the output of the PLL post-scaler described above. Additionally, this divider can be disabled under register control.

Digital Inputs - ICS1562A-001 Option

The AD0-AD3 pins and the STROBE pin are used to load all control registers of the **ICS1562A** (-001 option). The AD0-AD3 and STROBE pins are each equipped with a pull-up and will be at a logic HIGH level when not connected. They may be driven with standard TTL or CMOS logic families.

The address of the register to be loaded is latched from the AD0-AD3 pins by a negative edge on the STROBE pin. The data for that register is latched from the AD0-AD3 pins by a positive edge on the STROBE pin. See Figure 2 for a timing diagram. After power-up, the **ICS1562A-001** requires 32 register writes for new programming to become effective. Since only 13 registers are used at present, the programming system can perform 19 "dummy" writes to address 13 or 14 to complete the sequence.

This allows the synthesizer to be completely programmed for the desired frequency before it is made active. Once the part has been "unlocked" by the 32 writes, programming becomes effective immediately.

ALL registers identified in the data sheet (0-9, 11, 12 & 15) MUST be written upon initial programming. The programming registers are not initialized upon power-up, but the latched outputs of those registers are. The latch is made transparent after 32 register writes. If any register has not been written, the state upon power-up (random) will become effective. Registers 13 & 14 physically do not exist. Register 10 does exist, but is reserved for future expansion. To insure compatibility with possible future modifications to the database, ICS recommends that all three unused locations be written with zero.

ICS1562A-001 Register Loading

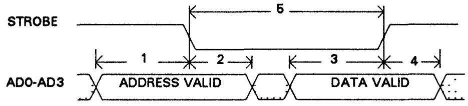


Figure 2

Digital Inputs - ICS1562A-201 Option

The programming of the **ICS1562A-201** is performed serially by using the DATCLK, DATA, and HOLD~pins to load an internal shift register.

DATA is shifted into the register on the rising edge of DATCLK. The logic value on the HOLD~pin is latched at the same time. When HOLD~ is low, the shift register may be loaded without disturbing the operation of the **ICS1562A**. When high, the shift register outputs are transferred to the control registers, and the new programming information becomes active. Ordinarily, a high level should be placed on the HOLD~ pin when the last data bit is presented. See Figure 3 for the programming sequence.

ICS1562A-201 Register Loading

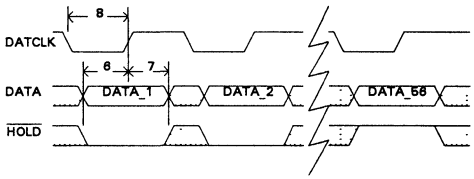


Figure 3

An additional control pin on the **ICS1562A-201**, BLANK can perform either of two functions. It may be used to disable the phase-frequency detector in line-locked applications. Alternatively, the BLANK pin may be used as a synchronous enable for VRAM shift clock generation. See sections on Line-Locked Operations and VRAM shift clock generation for details.

Output Description

The differential output drivers, CLK+ and CLK, are current-mode and are designed to drive resistive terminations in a complementary fashion. The outputs are current-sinking only, with the amount of sink current programmable via the IPRG pin. The sink current, which is steered to either CLK+or CLK-, is four times the current supplied to the **IPRG** pin. For most applications, a resistor from VDDO to IPRG will set the current to the necessary precision. Additionally, minor adjustment to the duty factor can be achieved under register control.

The LOAD output is a high-current CMOS type drive whose frequency is controlled by a programmable divider that may be selected for a modulus of 3, 4, 5, 6, 8, 10, 12, 16 or 20. It may also be suppressed under register control. The load output may be programmed to output the VCO frequency divided by 2 (see AUX_N1 description in Register Mapping section), independent of the differential output and N1 divider modulus.

The LD/N2 output is high-current CMOS type drive whose frequency is derived from the LOAD output. The programmable modulus may range from 1 to 512 in steps of one.

Pipeline Delay Reset Function

The **ICS1562A** implements the clocking sequence required to reset the pipeline delay on Brooktree RAMDACs when the LOAD output is programmed for a modulus of either 3, 4, 5, 6, 8 or 10. This sequence can be generated by setting the appropriate register bit (DACRST) to a logic 1 and then resetting to logic 0.

When changing frequencies, it is advisable to allow 500 microseconds after the new frequency is selected to activate the reset function. The output frequency of the synthesizer should be stable enough at that point for the video DAC to correctly execute its reset sequence. See Figure 4 for a diagram of the pipeline delay reset sequence.

Pipeline Delay Reset Timing

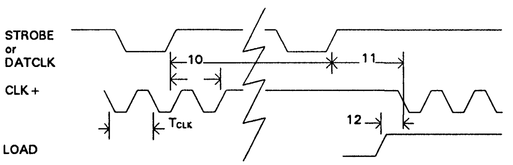


Figure 4

Reference Oscillator and Crystal Selection

The **ICS1562A** has circuitry on-board to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Series-resonant crystals may also be used with the **ICS1562A**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1562A** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

If an external reference frequency source is to be used with the **ICS1562A**, it is important that it be jitter-free. The rising and falling edges of that signal should be fast and free of noise for best results.

The loop phase is locked to the falling edges of the XTAL1 input signals if the REFPOL bit is set to logic 0.

Line-Locked Operation

The **ICS1562A** supports line-locked clock applications by allowing the LOAD (N1) and N2 divider chains to act as the feedback divider for the PLL.

The N1 and N2 divider chains allow a much larger modulus to be achieved than the PLL's own feedback divider. Additionally, the output of the N2 counter is accessible off-chip for performing horizontal reset of the graphics system, where necessary. This mode is set under register control (ALTLOOP bit). The reference divider (R counter) will ordinarily be set to divide by 1 in this mode, and the HSYNC signal of the external video will be supplied to the XTAL1 input. The output frequency of the synthesizer will then be:

$$F_{(CLK)} : = F\ (XTAL1) \cdot N1 \cdot N2.$$

By using the phase-detector hardware disable mode, the PLL can be made to free-run at the beginning of the vertical interval of the external video, and can be reactivated at its completion.

ICS1562A-001 The **ICS1562A-001** supports phase detector disable via a special control mode. When the PDRSTEN (phase detector reset enable) bit is set and the last address latched is 15 (0Fh), a high level on AD3 will disable PLL locking.

ICS1562A-201 The **ICS1562A-201** supports phase detector disable via the BLANK pin. When the PDRSTEN bit is set, a high level on the BLANK input will disable PLL locking.

External Feedback Operation

The **ICS1562A-201** option also supports the inclusion of an external counter as the feedback divider of the PLL. This mode is useful in graphic systems that must be "genlocked" to external video sources.

When the EXTFBEN bit is set to logic 1, the phase-frequency detector will use the EXTFBK pin as its feedback input. The loop phase will be locked to the rising edges of the signal applied to the EXTFBK input if the FBKPOL bit is set to logic 0.

VRAM Shift Clock Generation

The **ICS1562A-201** option supports VRAM shift clock generation and interruption. By programming the N2 counter to divide by 1, the LD/N2 output becomes a duplicate of the LOAD output. When the SCEN bit is set, the LD/N2 output may be synchronously started and stopped via the blank pin. When BLANK is high, the LD/N2 will be free-running and in phase with LOAD. When BLANK is taken low, the LD/N2 output is stopped at a low level. See Figure 5 for a diagram of the sequence. Note that this use of the **BLANK** pin precludes its use for phase comparator disable (see Line-Locked Operation).

VRAM Shift Clock Control

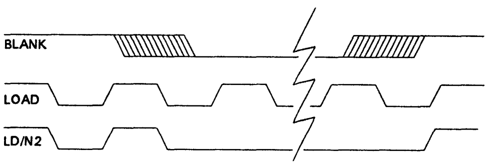


Figure 5

Power-On Initialization

The **ICS1562A** has an internal power-on reset circuit that performs the following functions:

1) Sets the multiplexer to pass the reference frequency to the CLK+ and CLK- outputs.

2) Selects the modulus of the N1 divider (for the LOAD clock) to be four.

These functions should allow initialization of most graphics systems that cannot immediately provide for register programming upon system power-up.

Because the power-on reset circuit is on the VDD supply, and because that supply is filtered, care must be taken to allow the reset to de-assert before programming. A safe guideline is to allow 20 microseconds after the VDD supply reaches 4 volts.

Programming Notes

- VCO Frequency Range: Use the post-divider to keep the VCO frequency as high as possible within its operating range.
- Divider Range: For best results in normal situations (i.e, pixel clock generation for hi-res displays), keep the reference divider modulus as short as possible (for a frequency at the output of the reference divider in the few hundred kHz to several MHz range). If you need to go to a lower phase comparator reference frequency (usually required for increased frequency accuracy), that is acceptable, but jitter performance will suffer somewhat.
- VCO Gain Programming: Use the minimum gain which can reliably achieve the VCO frequency desired, as shown on the following page:

VCO GAIN	MAX FREQUENCY
4	120 MHz
5	200 MHz
6	260 MHz
7	*

*SPECIAL APPLICATION. Contact factory for custom product above 260 MHz.

- Phase Detector Gain: For most graphics applications and divider ranges, set P[1, 0] = 10 and set P[2] = 1. Under some circumstances, setting the P[2] bit "on" can reduce jitter. During 1562 operation at exact multiples of the crystal frequency, P[2] bit = 0 may provide the best jitter performance.

Board Test Support

It is often desirable to statically control the levels of the output pins for circuit board test. The **ICS1562A** supports this through a register programmable mode, AUXEN. When this mode is set, two register bits directly control the logic levels of the CLK+/CLK- pins and the LOAD pin. This mode is activated when the S[0] and S[1] bits are both set to logic 1. See Register Mapping for details.

Power Supplies and Decoupling

The **ICS1562A** has two VSS pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS1562A** has a VDDO pin which is the supply of +5 volt power to all output drivers. This pin should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, capacitors should have low series inductance and be mounted close to the **ICS1562A**.

The VDD pin is the power supply pin for the PLL synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects. See Figure 6 for typical external circuitry.

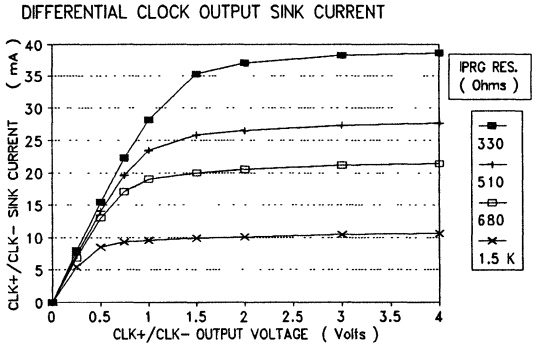
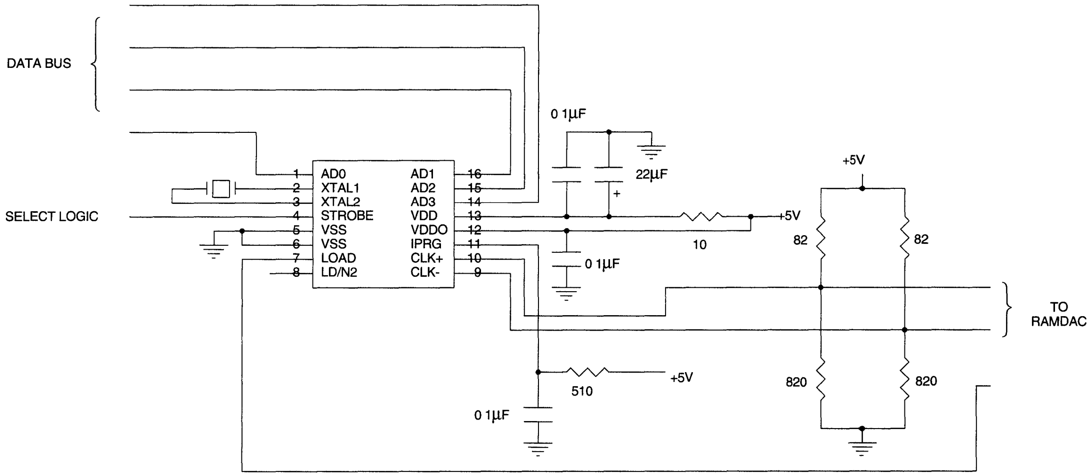


Figure 6

a)

ICS1562A-001 Typical Interface



b)

ICS1562A-201 Typical Interface

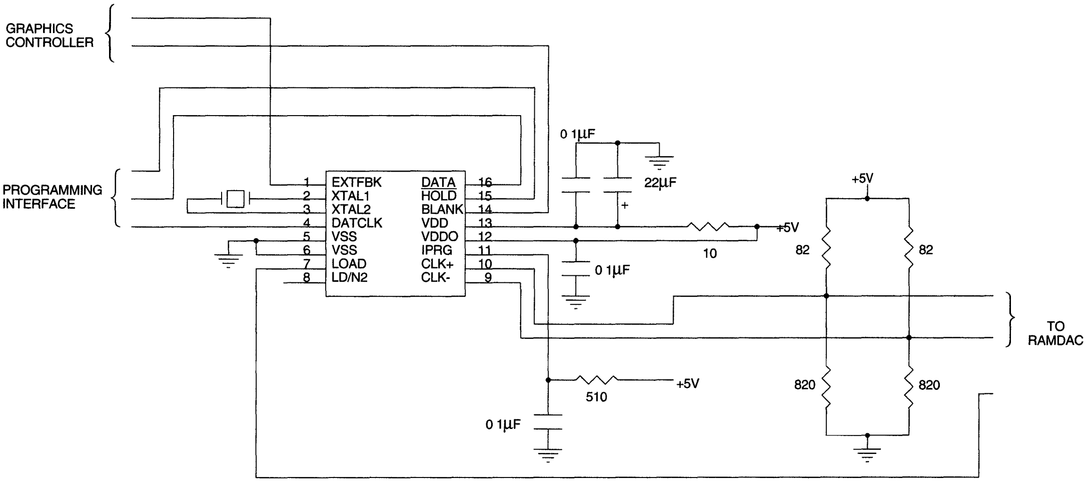


Figure 7

Register Mapping - ICS1562A-001 (Parallel Programming Option)

NOTE: IT IS NOT NECESSARY TO UNDERSTAND THE FUNCTION OF THESE BITS TO USE THE ICS1562A. PC SOFTWARE IS AVAILABLE FROM ICS TO AUTOMATICALLY GENERATE ALL REGISTER VALUES BASED ON REQUIREMENTS. CONTACT FACTORY FOR DETAILS.

REG#	BIT(S)	BIT REF.	DESCRIPTION
0	0-3	R[0]..R[3]	Reference divider modulus control bits
1	0-2	R[4]..R[6]	Modulus = value + 1
1	3	REFPOL	PLL locks to the rising edge of XTAL1 input when REFPOL=1 and to the falling edge of XTAL1 when REFPOL=0.
2	0-3	A[0]..A[3]	Controls A counter. When set to zero, modulus=7. Otherwise, modulus=7 for "value" underflows of the prescaler, and modulus=6 thereafter until M counter underflows.
3	0-3	M[0]..M[3]	M counter control bits
4	0-1	M[4]..M[5]	Modulus = value + 1
4	2	FBKPOL	External feedback polarity control bit. The PLL will lock to the falling edge of EXTFBK when FBKPOL=1 and to the rising edge of EXTFBK when FBKPOL=0.
4	3	DBLFREQ	Doubles modulus of dual-modulus prescaler (from 6/7 to 12/14).
5	0-3	N1[0]..N1[3]	Sets N1 modulus according to this table. These bits are set to implement a divide-by-four on power-up.

N1[3]	N1[2]	N1[1]	N1[0]	RATIO
0	0	0	0	3
0	0	0	1	4
0	0	1	0	4
0	0	1	1	5
0	1	0	0	6
0	1	0	1	8
0	1	1	0	8
0	1	1	1	10
1	X	0	0	12
1	X	0	1	16
1	X	1	0	16
1	X	1	1	20

X=Don't Care

REG#	BIT(S)	BIT REF.	DESCRIPTION
6 7	0-3 0-3	N2[0]..N2[3] N2[4]..N2[7]	Sets the modulus of the N2 divider. The input of the N2 divider is the output of the N1 divider in all clock modes except AUXEN.
8	3	N2[8]	
8	0-2	V[0]..V[1]	Sets the gain of the VCO.

V[2]	V[1]	V[0]	VCO GAIN (MHz/VOLT)
1	0	0	30
1	0	1	45
1	1	0	60
1	1	1	80

REG#	BIT(S)	BIT REF.	DESCRIPTION
9	0-1	P[0]..P[1]	Sets the gain of the phase detector according to this table.

P[1]	P[0]	GAIN (uA/radian)
0	0	0.05
0	1	0.15
1	0	0.5
1	1	1.5

REG#	BIT(S)	BIT REF.	DESCRIPTION
9	3	[P2]	Phase detector tuning bit. Normally should be set to one.
10	1	LOADEN~	Load clock divider enable (active low). When set to logic 1, the LOAD and LD/N2 outputs will cease toggling.
10	2	SKEW-	Differential output duty factor adjust.
10	3	SKEW+	

SKEW+	SKEW-	
0	0	Default
0	1	Reduces THIGH by approximately 100 ps
1	0	Increases THIGH by approximately 100 ps
1	1	Do not use

REG#	BIT(S)	BIT REF.	DESCRIPTION
11	0-1	S[0]..S[1]	PLL post-scaler/test mode select bits

S[1]	S[0]	DESCRIPTION
0	0	Post-scaler=1. F(CLK)=F(PLL). The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
0	1	Post-scaler=2. F(CLK)=F(PLL)/2. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
1	0	Post-scaler=4. F(CLK)=F(PLL)/4. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
1	1	AUXEN CLOCK MODE. The AUXCLK bit drives the differential outputs CLK+ and CLK- and the AUXN1 bit drives the LOAD output which, in turn, drives the N2 divider.

REG#	BIT(S)	BIT REF.	DESCRIPTION
11	2	AUX_CLK	When in the AUXEN clock mode, this bit controls the differential outputs.
11	3	AUX_N1	When in the AUXEN clock mode, this bit controls the LOAD output (and consequently the N2 output according to its programming). When not in the AUXEN clock mode, this bit, if set to one, will override the N1 divider modulus and output the VCO frequency divided by two [F(PLL)/2] at the LOAD output.
12	0	RESERVED	Must be set to zero.
12	1	JAMPLL	Tristates phase detector outputs; resets phase detector logic, and resets R, A, M, and N2 counters.
12	2	DACRST	Set to zero for normal operation. When set to one, the CLK+output is kept high and the CLK- output is kept low. (All other device functions are unaffected.) When returned to zero, the CLK+ and CLK- outputs will resume toggling on a rising edge of the LD output (+/- 1 CLK period). To initiate a RAMDAC reset sequence, simply write a one to this register bit followed by a zero.
12	3	SELXTAL	When set to logic 1, passes the reference frequency to the post-scaler.
15	0	ALTLOOP	Controls substitution of N1 and N2 dividers into feedback loop of PLL. When this bit is a logic 1, the N1 and N2 dividers are used.
15	3	PDRSTEN	Phase-detector reset enable control bit. When this bit is set, the AD3 pin becomes a transparent reset input to the phase detector. See LINE-LOCKED CLOCK GENERATION section for more details on the operation of this function.

Register Mapping - ICS1562A-201 (Serial Programming Option)

NOTE: IT IS NOT NECESSARY TO UNDERSTAND THE FUNCTION OF THESE BITS TO USE THE ICS1562A. PC SOFTWARE IS AVAILABLE FROM ICS TO AUTOMATICALLY GENERATE ALL REGISTER VALUES BASED ON REQUIREMENTS. CONTACT FACTORY FOR DETAILS

BIT(S)	BIT REF.	DESCRIPTION
1-4	N1[0]..N1[3]	Sets N1 modulus according to this table. These bits are set to implement a divide-by-four on power-up.

N1[3]	N1[2]	N1[1]	N1[0]	RATIO
0	0	0	0	3
0	0	0	1	4
0	0	1	0	4
0	0	1	1	5
0	1	0	0	6
0	1	0	1	8
0	1	1	0	8
0	1	1	1	10
1	X	0	0	12
1	X	0	1	16
1	X	1	0	16
1	X	1	1	20

BIT(S)	BIT REF.	DESCRIPTION
5	RESERVED	Must be set to zero.
6	JAMPLL	Tristates phase detector outputs, resets phase detector logic, and resets R, A, M, and N2 counters.
7	DACRST	Set to zero for normal operations. When set to one, the CLK+ output is kept high and the CLK- output is kept low. (All other device functions are unaffected.) When returned to zero, the CLK+ and CLK- outputs will resume toggling on a rising edge of the LD output (+/–1 CLK period). To initiate a RAMDAC reset sequence, simply write a one to this register bit followed by a zero.
8	SELXTAL	When set to logic 1, passes the reference frequency to the post-scaler.
9	ALTLOOP	Controls substitution of N1 and N2 dividers into feedback loop of PLL. When this bit is a logic 1, the N1 and N2 dividers are used.
10	SCEN	VRAM shift clock enable bit. When logic 1, the BLANK pin can be used to disable the LD/N2 output.
11	EXTFBKEN	External PLL feedback select. When logic 1, the EXTFBK pin is used for the phase-frequency detector feedback input.
12	PDRSTEN	Phase detector reset enable control bit. When this bit is set, a high level on the BLANK input will disable PLL locking. See LINE-LOCKED CLOCK GENERATION section for more details on the operation of this function.

BIT(S)	BIT REF.	DESCRIPTION
13-14	S[0]..S[1]	PLL post-scaler/test mode select bits.

S[1]	S[0]	DESCRIPTION
0	0	Post-scaler=1. F(CLK)=F(PLL). The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
0	1	Post-scaler=2. F(CLK)=F(PLL)/2. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
1	0	Post-scaler=4. F(CLK)=F(PLL)/4. The output of the N1 divder drives the LOAD output which, in turn, drives the N2 divider.
1	1	AUXEN CLOCK MODE. The AUXCLK bit drives the differential outputs CLK+ and CLK- and the AUXN1 bit drives the LOAD output which, in turn, drives the N2 divider.

BIT(S)	BIT REF.	DESCRIPTION
15	AUX_CLK	When in the AUXEN clock mode, this bit controls the differential outputs.
16	AUX_N1	When in the AUXEN clock mode, this bit controls the N1 output (and consequently the N2 output according to its programming). When not in the AUXEN clock mode, this bit, if set to one, will override the N1 divider modulus and output the VCO frequency divided by two [F(PLL)/2] at the LOAD output.
17-24 28	N2[0]..N2[7] N2[8]	Sets the modulus of the N2 divider. The input of the N2 divider is the output of the N1 divider in all clock modes except AUXEN.
25-27	V[0]..V[2]	Sets the gain of VCO according to this table.

V[2]	V[1]	V[0]	VCO GAIN (MHz/VOLT)
1	0	0	30
1	0	1	45
1	1	0	60
1	1	1	80

BIT(S)	BIT REF.	DESCRIPTION
29-30	P[0]..P[1]	Sets the gain of the phase detector according to this table.

P[1]	P[0]	GAIN (uA/radian)
0	0	0.05
0	1	0.15
1	0	0.5
1	1	1.5

BIT(S)	BIT REF.	DESCRIPTION
31	RESERVED	Set to zero.
32	P[2]	Phase detector tuning bit. Should normally be set to one.

BIT(S)	BIT REF.	DESCRIPTION
33-38	M[0]..M[5]	M counter control bits Modulus = value +1
39	FBKPOL	External feedback polarity control bit. The PLL will lock to the falling edge of EXTFBK when FBKPOL=1 and to the rising edge of EXTFBK when FBKPOL=0.
40	DBLFREQ	Doubles modulus of dual-modulus prescaler (from 6/7 to 12/14).
41-44	A[0]..A[3]	Controls A counter. When set to zero, modulus=7. Otherwise, modulus=7 for "value" underflows of the prescaler, and modulus=6 thereafter until M counter underflows.
45	RESERVED	Set to zero.
46	LOADEN~	Load clock divider enable (active low). When set to logic 1, the LOAD and LD/N2 outputs will cease toggling.
47 48	SKEW- SKEW+	Differential output duty factor adjust.

SKEW+	SKEW-	
0	0	Default
0	1	Reduces T_{HIGH} by approximately 100 ps
1	0	Increases T_{HIGH} by approximately 100 ps
1	1	Do not use

BIT(S)	BIT REF.	DESCRIPTION
49-55	R[0]..R[6]	Reference divider modulus control bits Modulus = value + 1
56	REFPOL	PLL locks to the rising edge of XTAL1 input when REFPOL=1 and to the falling edge of XTAL1 when REFPOL=0.

Table 1 - "A" & "M" Divider Programming
Feedback Divider Modulus Table

A[2]..A[0]-	001	010	011	100	101	110	111	000
M[5]..M[0]								
000000								7
000001	13							14
000010	19	20						21
000011	25	26	27					28
000100	31	32	33	34				35
000101	37	38	39	40	41			42
000110	43	44	45	46	47	48		49
000111	49	50	51	52	53	54	55	56
001000	55	56	57	58	59	60	61	63
001001	61	62	63	64	65	66	67	70
001010	67	68	69	70	71	72	73	77
001011	73	74	75	76	77	78	79	84
001100	79	80	81	82	83	84	85	91
001101	85	86	87	88	89	90	91	98
001110	91	92	93	94	95	96	97	105
001111	97	98	99	100	101	102	103	112
010000	103	104	105	106	107	108	109	119
010001	109	110	111	112	113	114	115	126
010010	115	116	117	118	119	120	121	133
010011	121	122	123	124	125	126	127	140
010100	127	128	129	130	131	132	133	147
010101	133	134	135	136	137	138	139	154
010110	139	140	141	142	143	144	145	161
010111	145	146	147	148	149	150	151	168
011000	151	152	153	154	155	156	157	175
011001	157	158	159	160	161	162	163	182
011010	163	164	165	166	167	168	169	189
011011	169	170	171	172	173	174	175	196
011100	175	176	177	178	179	180	181	203
011101	181	182	183	184	185	186	187	210
011110	187	188	189	190	191	192	193	217
011111	193	194	195	196	197	198	199	224

A[2]..A[0]-	001	010	011	100	101	110	111	000
M[5]..M[0]								
100000	199	200	201	202	203	204	205	231
100001	205	206	207	208	209	210	211	238
100010	211	212	213	214	215	216	217	245
100011	217	218	219	220	221	222	223	252
100100	223	224	225	226	227	228	229	259
100101	229	230	231	232	233	234	235	266
100110	235	236	237	238	239	240	241	273
100111	241	242	243	244	245	246	247	280
101000	247	248	249	250	251	252	253	287
101001	253	254	255	256	257	258	259	294
101010	259	260	261	262	263	264	265	301
101011	265	266	267	268	269	270	271	308
101100	271	272	273	274	275	276	277	315
101101	277	278	279	280	281	282	283	322
101110	283	284	285	286	287	288	289	329
101111	289	290	291	292	293	294	295	336
110000	295	296	297	298	299	300	301	343
110001	301	302	303	304	305	306	307	350
110010	307	308	309	310	311	312	313	357
110011	313	314	315	316	317	318	319	364
110100	319	320	321	322	323	324	325	371
110101	325	326	327	328	329	330	331	378
110110	331	332	333	334	335	336	337	385
110111	337	338	339	340	341	342	343	392
111000	343	344	345	346	347	348	349	399
111001	349	350	351	352	353	354	355	406
111010	355	356	357	358	359	360	361	413
111011	361	362	363	364	365	366	367	420
111100	367	368	369	370	371	372	373	427
111101	373	374	375	376	377	378	379	434
111110	379	380	381	382	383	384	385	441
111111	385	386	387	388	389	390	391	448

Notes:

To use this table, find the desired modulus in the table. Follow the column up to find the A divider programming values. Follow the row to the left to find the M divider programming. Some feedback divisors can be achieved with two or three combinations of divider settings. Any are acceptable for use.

The formula for the effective feedback modulus is: $N = [(M + 1) \cdot 6] + A$

except when A=0, then: $N = (M + 1) \cdot 7$

Under all circumstances: $A \le M$

Pin Descriptions - ICS1562A-001

PIN#	NAME	DESCRIPTION
10	CLK+	Clock out (non-inverted)
9	CLK–	Clock out (inverted)
7	LOAD	Load output. This output is normally at the CLK frequency divided by N1.
2	XTAL1	Quartz crystal connection 1/external reference frequency input
3	XTAL2	Quartz crystal connection 2
1	AD0	Address/Data Bit 0 (LSB)
16	AD1	Address/Data Bit 1
15	AD2	Address/Data Bit 2
14	AD3	Address/Data Bit 3 (MSB)
8	LD/N2	Divided LOAD output. See text.
4	STROBE	Control for address/data latch
13	VDD	PLL system power (+5V. See application diagram.)
12	VDDO	Output stage power (+5V)
11	IPRG	Output stage current set
5,6	VSS	Device ground. Both pins must be connected to the same ground potential.

Pin Descriptions - ICS1562A-201

PIN#	NAME	DESCRIPTION
10	CLK+	Clock out (non-inverted)
9	CLK–	Clock out (inverted)
7	LOAD	Load output. This output is normally at the CLK frequency divided by N1.
2	XTAL1	Quartz crystal connection 1/external reference frequency input
3	XTAL2	Quartz crystal connection 2
4	DATCLK	Data Clock (Input)
16	DATA	Serial Register Data (Input)
15	HOLD~	$\overline{\text{HOLD}}$ (Input)
14	BLANK	Blanking (Input). See Text.
8	LD/N2	Divided LOAD output/shift clock. See text.
1	EXTFBK	External feedback connection for PLL (input). See text.
13	VDD	PLL system power (+5V. See application diagram.)
12	VDDO	Output stage power (+5V)
11	IPRG	Output stage current set
5,6	VSS	Device ground. Both pins must be connected.

Absolute Maximum Ratings

VDD, VDDO (measured to V_{SS})	7.0 V
Digital Inputs	V_{SS}-0.5 to VDD + 0.5 V
Digital Outputs	V_{SS}-0.5 to VDDO + +0.5 V
Ambient Operating Temperature	-55 to 125°C
Storage Temperature	-65 to 150°C
Junction Temperature	175°C
Soldering Temperature	260°C

Recommended Operating Conditions

VDD, VDDO (measured to V_{SS})	4.75 to 5.25 V
Operating Temperature (Ambient)	0 to 70°C

DC Characteristics

TTL-Compatible Inputs
001 Option - (AD0-AD3, STROBE),
201 Option - (DATCLK, DATA, HOLD, BLANK, EXTFBK)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{ih}		2.0	V_{DD}+0.5	V
Input Low Voltage	V_{il}		V_{SS}-0.5	0.8	V
Input High Current	I_{ih}	V_{ih}=VDD	-	10	uA
Input Low Current	I_{il}	V_{il}=0.0	-	200	uA
Input Capacitance	C_{in}		-	8	pf
Hysteresis (STROBE/DATCLK)	V_{hys}	V_{DD}=5V	.20	.60	V

XTAL1 Input

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{xh}		3.75	V_{DD}+0.5	V
Input Low Voltage	V_{xl}		V_{SS}-0.5	1.25	

CLK+, CLK- Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Differential Output Voltage			0.6	-	V

LOAD, LD/N2 Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output High Voltage (Ioh = 4.0mA)			2.4	-	V
Output Low Voltage (Iol = 8.0mA)			-	0.4	V

AC Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
F_{vco}	VCO Frequency (see Note 1)	40		260	MHz
F_{xtal}	Crystal Frequency	5		20	MHz
Cpar	Crystal Oscillator Loading Capacitance		20		pf
F_{load}	LOAD Frequency			80	MHz
T_{xhi}	XTAL1 High Time (when driven externally)	8			ns
T_{xlo}	XTAL1 Low Time (when driven externally)	8			ns
T_{lock}	PLL Acquire Time (to within 1%)		500		µs
I_{dd}	VDD Supply Current		15	t.b.d.	mA
I_{ddo}	VDDO Supply Current (excluding CLK+/– termination)		20	t.b.d.	mA
T_{high}	Differential Clock Output Duty Cycle (see Note 2)	45		55	%
J_{clk}	Differential Clock Output Cumulative Jitter (see Note 3)		<0.06		pixel
DIGITAL INPUTS - ICS1562A-001					
1	Address Setup Time	10			ns
2	Address Hold Time	10			ns
3	Data Setup Time	10			ns
4	Data Hold Time	10			ns
5	STROBE Pulse Width (T_{hi} or T_{lo})	20			ns
DIGITAL INPUTS - ICS1562A-201					
6	DATA/HOLD~ Setup Time	10			ns
7	DATA/HOLD~ Hold Time	10			ns
8	DATCLK Pulse Width (T_{hi} or T_{lo})	20			ns
PIPELINE DELAY RESET					
9	Reset Activation Time			2*Tclk	ns
10	Reset Duration	4*Tload			ns
11	Restart Delay			2*Tload	ns
12	Restart Matching	-1*Tclk		+1.5*Tclk	ns
DIGITAL OUTPUTS					
13	CLK+/CLK– Clock Rate			260	MHz
14	LOAD To LD/N2 Skew (Shift Clock Mode)	-2	0	+2	ns

Note 1: Use of the post-divider is required for frequencies lower than 40 MHz on CLK+ & CLK- outputs. Use of the post-divider is recommended for output frequencies lower than 65 MHz.

Note 2: Using load circuit of Figure 6. Duty cycle measured at zero crossings of difference voltage between CLK+ and CLK-.

Note 3: Cumulative jitter is defined as the maximum error (in the domain) if any CLK edge, at any point in time, compared with the equivalent edge generated by an ideal frequency source.
ICS laboratory testing indicates that the typical value shown above can be treated as a maximum jitter specification in virtually all applications. Jitter performance can depend somewhat on circuit board layout, decoupling, and register programming.

Ordering Information

ICS1562AM-001 or ICS1562AM-201

Example:

ICS XXXX M -XXX

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

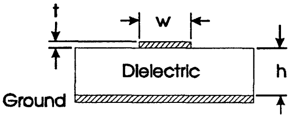
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Output Circuit Considerations for the ICS1562A

Output Circuitry

The dot clock signals CLK and CLK- are typically the highest frequency signals present in the workstation. To minimize problems with EMI, crosstalk, and capacitive loading extra care should be taken in laying out this area of the PC board. The **ICS1562A** is packaged in a 0.2"-wide 16-pin SOIC package. This permits the clock generator, crystal, and related components to be laid out in an area the size of a postage stamp. The **ICS1562A** should be placed as close as possible to the RAMDAC. The CLK and CLK- pins are running at VHF frequencies; one should minimize the length of PCB trace connecting them to the RAMDAC so that they don't become radiators of RF energy.

At the frequencies that the **ICS1562A** is capable of, PC board traces may be long enough to be a significant portion of a wavelength of that frequency. PC traces for CLK and CLK- should be treated as transmission lines, not just interconnecting wires. These lines can take two forms: microstrip and stripline. A microstrip line is shown below:



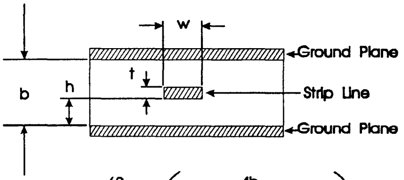
$$Z_o = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8w+t}\right)$$

Dimensions in Inches

Microstrip Line

Essentially, the microstrip is a copper trace on a PCB over a ground plane. Typically, the dielectric is G10 glass epoxy. It differs from a standard PCB trace in that its width is calculated to have a characteristic impedance. To calculate the characteristic impedance of a microstrip line one must know the width and thickness of the trace, and the thickness and dielectric constant of the dielectric. For G10 glass epoxy, the dielectric constant (e_r) is about 5. Propagation delay is strictly a function of dielectric constant. For G10 propagation, delay is calculated to be 1.77 ns/ft.

Stripline is the other form a PCB transmission line can take. A buried trace between ground planes (or between a power plane and a ground plane) is common in multi-layer boards. Attempting to create a workstation design without the use of multi-layer boards would be adventurous to say the least, the issue would more likely be whether to place the interconnect on the surface or between layers. The between layer approach would work better from an EMI standpoint, but would be more difficult to lay out. A stripline is shown below:



$$Z_o = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4b}{0.067\pi w\left(0.8 + \frac{t}{w}\right)}\right)$$

Dimensions in Inches

Stripline

Using 1 oz. copper (0.0015" thick) and 0.040" thickness G10, a 0.010" trace will exhibit a characteristic impedance of 75Ω in a stripline configuration.

Typically, RAMDACs require a V_{ih} of V_{AA}-1.0 Volts as a guaranteed logical "1" and a V_{il} of V_{AA}-1.6 as a guaranteed logical "0." Worst case input capacitance is 10 pf.

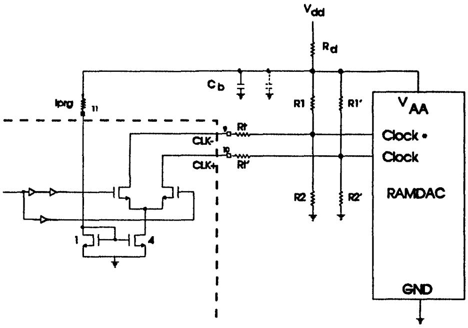
Output circuitry for the **ICS1562A** is shown in the following diagram. It consists of a 4/1 current mirror, and two open drain output FETs along with inverting buffers to alternately enable each current-sinking driver. Both CLK and CLK- outputs are connected to the respective CLOCK and $\overline{\text{CLOCK}}$ inputs of the RAMDAC with transmission lines and terminated in their equivalent impedances by the Thevenin equivalent impedances of R1 and R2 or R1' and R2'.

The **ICS1562A** is incapable of sourcing current, so V_{ih} must be set by the ratios of these resistors for each of these lines. R1 and R2 are electrically in parallel from an AC standpoint because V_{dd} is bypassed to ground through bypass-capacitor network C_b. If we picked a target impedance of 75Ω for our transmission line impedance, a value of 91Ω for R1 and R1' and a value of 430Ω for R2 and R2' would yield a Thevinin equivalent characteristic impedance of 75.1Ω and a V_{ih} value of V_{AA}-.873 Volts, a margin of 0.127 Volts. This may be adequate; however, at higher frequencies one must contend with the 10 pf input capacitance of the RAMDAC. Values of 82Ω for R1 and R1' and 820Ω for R2 and R2' would give us a characteristic impedance of 74.5Ω and a V_{ih} value of V_{AA}-.45. With a .55 Volt margin on V_{ih}, this voltage level might be safer.

To set a value for V_{il}, we must determine a value for I_{prg} that will cause the output FET's to sink an appropriate current. We desire V_{il} to be V_{AA}-1.6 or greater. V_{AA}-2 would seem to be a safe value. Setting up a sink current of 25 milliamperes would guarantee this through our 82Ω pull-up resistors. As this is controlled by a 4/1 current mirror, 7 mA into I_{prg} should set this current properly. A 510Ω resistor from V_{dd} to I_{prg} should work fine.

Resistors Rt and Rt' are shown as series terminating resistors at the **ICS1562A** end of the transmission lines. These are not required for operation, but may be useful for meeting EMI requirements. Their intent is to interact with the input capacitance of the RAMDAC and the distributed capacitance of the transmission line to soften up rise and fall times and consequently cut some of the high-order harmonic content that is more likely to radiate RF energy. In actual usage they would most likely be 10 to 20Ω resistors or possibly ferrite beads.

C_b is shown as multiple capacitors. Typically, a 22 μf tantalum should be used with separate .1 μF and 220pf capacitors placed as close to the pins as possible. This provides low series inductance capacitors right at the source of high frequency energy. R_d is used to isolate the circuitry from external sources of noise. Five to ten ohms should be adequate.



ICS1562A Output Circuitry

Great care must be used when evaluating high frequency circuits to achieve meaningful results. The 10 pf input capacitance and long ground lead of an ordinary scope probe will make any measurements made with it meaningless. A low capacitance FET probe with a ground connection directly connected to the shield at the tip will be required. A 1GHz bandwidth scope will be barely adequate, try to find a faster unit.

Integrated
Circuit
Systems, Inc.

ICS1567

Differential Output Video Dot Clock Generator

General Description

The **ICS1567** is a very high performance monolithic PLL frequency synthesizer. Utilizing ICS's advanced CMOS mixed-mode technology, the **ICS1567** provides a low cost solution for high-end video clock generation, and for telecom system clock generation.

The **ICS1567** has differential video clock outputs (CLK and $\overline{\text{CLK}}$) that are compatible with industry standard video DACs & RAMDACs. An additional clock output, $\overline{\text{LD}}$, is provided, whose frequency is divided down from the main clock by a programmable divider.

Operating frequencies are selectable from a pre-programmed (customer-defined) table. An on-chip crystal oscillator for generating the reference frequency is provided on the **ICS1567**.

Programming of the **ICS1567** is accomplished via frequency select pins on the package. The **ICS1567** has five lines plus a STROBE pin which permits selection of 32 frequencies. Reset of the pipeline delay on Brooktree RAMDACs is automatically performed on a rising edge of the STROBE line.

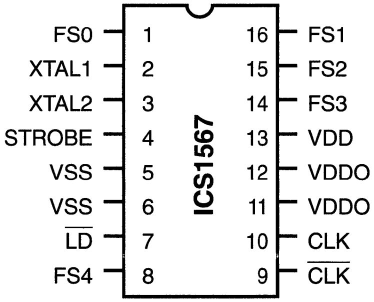
Features

- High frequency operation for extended video modes - up to 180 MHz
- Compatible with Brooktree high performance RAMDACs
  a) Differential output clocks with ECL logic levels
  b) Programmable divider modulus for load clock
  c) Circuitry included for automatic reset of Brooktree RAMDAC pipeline delay
- Low cost - eliminates need for multiple ECL crystal clock oscillators in video display systems
- Strobed/Transparent frequency select options
- 32-user selected mask-programmable frequencies
- Fast acquisition of selected frequencies, strobed or non-strobed
- Advanced PLL for low phase-jitter
- Dynamic control of VCO sensitivity providing optimized loop gain over entire frequency range
- Small footprint - 16-pin wide body (300 mil) SOIC

Applications

- Workstations
- High-resolution PC and MAC displays
- 8514A - TMS340X0 systems
- EGA - VGA - Super VGA video
- Telecom reference clock generation - suitable for Sonet, ATM and other data rates up to 155.52Mb.

Pin Configuration



16-Pin SOIC
K-6

Block Diagram

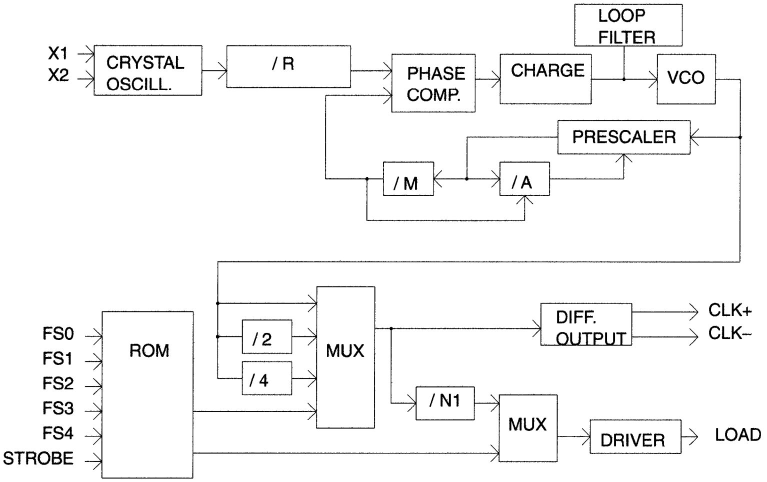


Figure 1

System Schematic

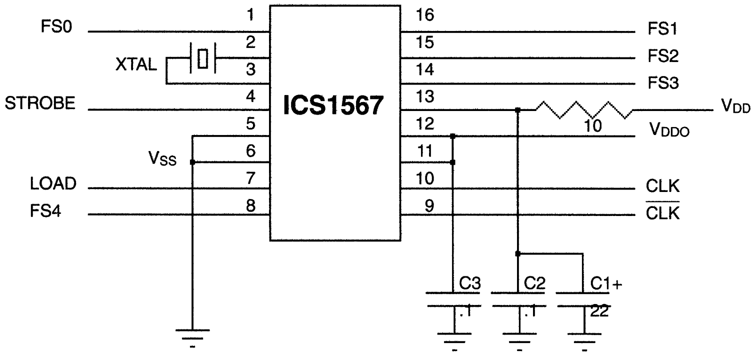
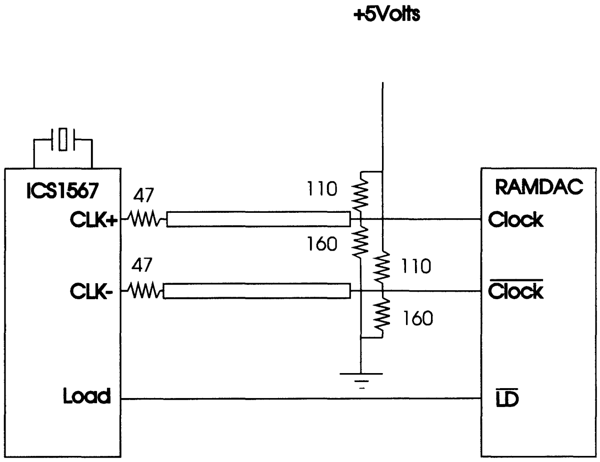


Figure 2

Typical Output Configuration



Notes:
CLK & $\overline{CLK}$ outputs are pseudo-ECL. Logic low level is set by the ratio of the resistors stacked across the power supply V_{LO} = (V supply • 160)/(110 +160) in the example shown above.
The above values are a good starting point for RAMDAC or clock generator interface.

Figure 3

Pin Description

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	• FS0	IN	Frequency Select LSB
2	XTAL1	IN	Crystal Interface/External Oscillator Input
3	XTAL2	OUT	Crystal Interface
4	• STROBE	IN	Control For Frequency Select Latch, also performs automatic RAMDAC reset
5	VSS	--	Device Ground (Both pins must be connected.)
6	VSS	--	Device Ground (Both pins must be connected.)
7	$\overline{LD}$	OUT	Load Output. This output is at CLK frequency divided by N1.
8	• FS4	IN	Frequency Select MSB
9	$\overline{CLK}$	OUT	Clock Output Inverted
10	CLK	OUT	Clock Output Non-Inverted
11	VDDO	--	Output Stage Power (Both pins must be connected)
12	VDDO	--	Output Stage Power (Both pins must be connected)
13	VDD	--	PLL System Power
14	• FS3	IN	Frequency Select
15	• FS2	IN	Frequency Select
16	• FS1	IN	Frequency Select

• = inputs with internal pull-up resistor

Circuit Description

Overview

The **ICS1567** is designed to provide the graphics system clock signals required by industry standard RAMDACs. One of 32 pre-programmed (user-definable) frequencies may be selected under digital control. Fully programmable feedback and reference divider capability allow virtually any frequency to be generated, not just simple multiples of the reference frequency. The **ICS1567** uses the latest generation of frequency synthesis techniques developed by ICS and is completely suitable for the most demanding video applications.

Digital Inputs

The FS0-FS4 pins and the STROBE pin are used to select the desired operating frequency from the 32 pre-programmed frequencies in the ROM table of the **ICS1567**. The STROBE pin also controls activation of the pipeline delay RESET function included in the **ICS1567** (see PIPELINE DELAY RESET section for details). The FS0-FS4 and STROBE pins are each equipped with a pull-up and will be at a logic HIGH level when not connected.

Transparent Mode - When the STROBE pin is held HIGH, the FS0 through FS4 inputs are transparent; that is, they directly access the ROM table. The synthesizer will output the frequency programmed into the location addressed by the FS0-FS4 pins.

Latched Mode - When the STROBE pin is held LOW, the FS0-FS4 pins are ignored. The synthesizer will output the frequency corresponding to the state of the FS0-FS4 pins when the STROBE pin was last HIGH. In the event that the **ICS1567** is powered-up with the STROBE pin held LOW, the synthesizer will output the frequency programmed into address 0 (i.e., the one selected with FS0 through FS4 at a logic LOW level).

Frequency Synthesizer Description

Refer to Figure 1 for a block diagram of the **ICS1567**. The reference frequency is generated by an on-chip crystal oscillator, or the reference frequency may be applied to the **ICS1567** from an external frequency source.

The **ICS1567** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL. The phase-frequency detector shown in the block diagram drives the VCO to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F(\text{vco}) = \frac{F(\text{XTAL1}) \bullet \text{Feedback Divider}}{\text{Reference Divider}}$$

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly-programmed dividers). The divider programming is one of the functions performed by the ROM look-up table in the **ICS1567**. The VCO gain is also ROM programmable which permits the **ICS1567** to be optimized for best performance at each frequency in the table.

The feedback divider makes use of a dual-modulus prescaler technique that allows construction of a programmable counter to operate at high speeds while still allowing the feedback divider to be programmed in steps of 1. This is an improvement over conventional fixed prescaler architectures that typically impose a factor-of-four penalty (or larger) in this respect.

A post-divider may be inserted between the VCO and the CLK and $\overline{\text{CLK}}$ outputs of the **ICS1567**. This is useful in generation of lower frequencies, as the VCO has been optimized for high-frequency operation. Different post-divider settings may be used for each frequency in the table.

Load Clock Divider

The **ICS1567** has an additional programmable divider that is used to generate the LOAD frequency. The modulus of this divider may be set to 3, 4, 5, 6, 8, or 10. The design of this divider permits the output duty factor to be 50/50, even when an odd modulus is selected.

The selection of the modulus is done by the ROM look-up table. A different modulus may, therefore, be selected for each frequency address.

Pipeline Delay Reset Function

The **ICS1567** implements the clocking sequence required to reset the pipeline delay on Brooktree RAMDACs. This sequence is automatically generated by the **ICS1567** upon any rising edge of the STROBE line.

When the frequency select inputs (FS0-FS4) are used in a transparent mode, simply lower and raise the STROBE line to activate the function. When the frequency select inputs are latched, simply load the same frequency into the **ICS1567** twice.

When changing frequencies, it is advisable to allow 500uSec after the new frequency is selected to activate the reset function. The output frequency of the synthesizer should be stable enough at that point for the RAMDAC to correctly execute its reset sequence.

See Figure 4 for a diagram of the clock sequencing.

Output Stage Description

The CLK and $\overline{\text{CLK}}$ outputs are each connected to the drains of P-Channel MOSFET devices. The source of each of these devices is connected to VDDO. Typical on resistance of each device is 15 Ohms. These outputs will drive the clock and $\overline{\text{clock}}$ of a RAMDAC device when a resistive network equivalent to Figure 3 is utilized.

The $\overline{\text{LD}}$ output is a high-current CMOS type drive whose frequency is controlled by a programmable divider that may be selected for a modulus of 3, 4, 5, 6, 8, or 10. Under control of the ROM, this output may also be suppressed (logic low level) at any frequency select address, if desired.

Application Information

Power Supplies

The **ICS1567** has two VSS pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS1567** has two VDDO pins which are the supply of +5 volt power to all output stages. Again, both VDDO pins connect to the same point on the die. BOTH of these pins should be connected to the power plane (or bus) using standard high-frequency decoupling practice. This decoupling consists of a low series inductance bypass capacitor, using the shortest leads possible, mounted close to the **ICS1567**.

The VDD pin is the power supply for the synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects.

Crystal Oscillator and Crystal Selection

The **ICS1567** has circuitry on-board to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

So-called series-resonant crystals may also be used with the **ICS1567**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.005-0.01%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1567** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

Application Notes *(continued)*

Bus Clock Interface

In some applications, it may be desirable to utilize the bus clock. To do this, connect the clock through a .047uF capacitor to XTAL1 (2) and keep the lead length of the capacitor to XTAL1 (2) to a minimum to reduce noise susceptibility. This input is internally biased at VDD/2. Since TTL compatible clocks typically exhibit a VOH of 3.5V, capacitively coupling the input restores noise immunity. The **ICS1567** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of the bus clock is typically outside the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. XTAL2 (3) must be left open in this configuration.

ICS1567 Interface

The **ICS1567** should be located as close as possible to the video DAC or RAMDAC. Figure 3 illustrates interfacing the **ICS1567** to a RAMDAC. The differential output CLOCK drivers are current sourcing only and are designed to drive resistive terminations in a complementary fashion CLK and $\overline{\text{CLK}}$ connections should follow good ECL interconnection practice. Terminating resistors should be as close as possible to the RAMDAC.

Absolute Maximum Ratings

Ambient Temeperature under bias	T_O	0°C to 70°C
Supply Voltage	V_{DD}	-0.5V to +7V
Input Voltage	V_{IN}	-0.5V to V_{DD} + 0.5V
Output Voltage	V_{OUT}	-0.5V to V_{DD} + 0.5V
Clamp Diode Current	V_{IK} & I_{OK}	±30mA
Output Current per Pin	I_{OUT}	±50mA
Storage Temperature	T_S	-85°C to + 150°C
Power Dissipation	P_D	500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to > = V_{SS} and < = V_{DD}.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to VSS (OV Ground). Positive current flows into the referenced pin.

Operating Temperature range	0°C to 70°C
Power supply voltage	4.75 to 5.25 Volts

DC Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITIONS
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.5	V	
Input Low Voltage	V_{IL}	V_{SS} -0.5	0.8	V	
Input High Current	I_{IH}		10	uA	$V_{IN} = V_{DD}$
Input Low Current	I_{IL}		-200	uA	$V_{IN} = V_{SS}$
LOAD OUTPUT					
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -4.0 mA
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 6.0 mA
CLOCK OUTPUTS					
Differential Output Voltage ($CLK-\overline{CLK}$)	V_{OD}	1.2		V	See Figure 4
XTAL1 INPUT					
Input High Voltage	V_{XH}	3.75	V_{DD} + 0.5	V	
Input Low Voltage	V_{XL}	VSS -0.5	1.25	V	
Operating Current	I_{DD}		50	mA	Outputs Unloaded
Input Pin Capacitance	C_{IN}		8	pF	F_C = 1 MHz
Output Pin Capacitance	C_{OUT}		12	pF	F_C = 1 MHz

AC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK and $\overline{CLK}$ TIMING						
Duty Cycle	T_{HIGH}	40		60	%	3, 4, 9
Frequency Error				0.5	%	
Rise Time	T_r			2	ns	5, 9
Fall Time	T_f			2	ns	5, 9
VCO Frequency	F_{VCO}	20		180	MHz	1
PLL Acquire Time	T_{LOCK}		500		uS	
LD* TIMING						
Duty Cycle	T_{HIGH}	40		60	%	6
Load Frequency	F_{LOAD}			60	MHz	
Rise Time	T_r			2	ns	7, 8
Fall Time	T_f			2	ns	7, 8
REFERENCE INPUT CLOCK						
Crystal Frequency	F_{XTAL}	5		20	MHz	
Crystal Oscillator Loading Capacitance	C_{PAR}		20		pF	
XTAL1 High Time	T_{XHI}	8			ns	2
XTAL1 Low Time	T_{XLO}	8			ns	2
Rise Time	T_r			10	ns	2, 7
Fall Time	T_f			10	ns	2, 7
DIGITAL INPUTS						
Frequency Select Setup Time	1	10			ns	10
Frequency Select Hold Time	2	10			ns	10
Strobe Pulse Width	3	20			ns	10
PIPELINE DELAY RESET						
Reset Activation	4			2*T_{CLK}	ns	10
Reset Duration	5	4*T_{CLK}			ns	10
Restart Delay	6	-1*T_{CLK}		+1.5*T_{CLK}	ns	10

Notes:

1. Use of the post-divider is required for frequencies lower than 20 MHz on CLK and $\overline{CLK}$ outputs. Use of the post-divider is recommended for output frequencies lower than 65 MHz.
2. Values for XTAL1 driven by an external clock
3. Duty Cycle for Differential Output (CLK- $\overline{CLK}$)
4. Duty cycle measured at VOD/2 for Differential CLK Output
5. Rise and fall time between 20% and 80% of VOD
6. Duty cycle measured at 1.4V for TTL I/O
7. Rise and fall time between 0.8 and 2.0 VDC for TTL I/O
8. Output pin loading = 15 pf
9. See Figure 3.
10. See Figure 4.

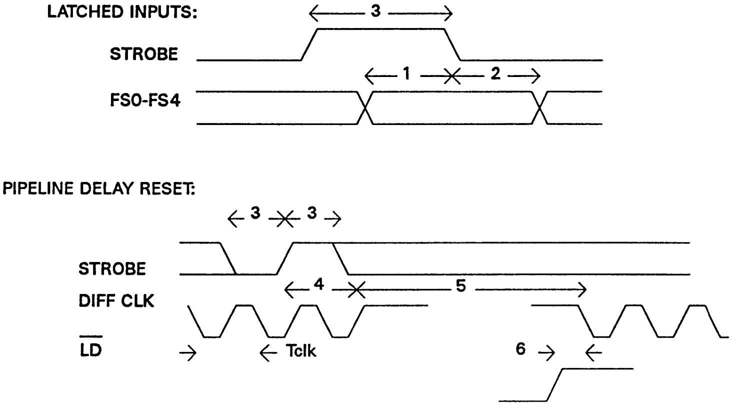

LATCHED INPUTS:
3
STROBE
1
2
FS0-FS4
PIPELINE DELAY RESET:
3
3
STROBE
4
5
DIFF CLK
LD
Tclk
6

Figure 4

ICS1567 Pattern Request Form

Custom patterns are also available, although a significant volume commitment and/or one-time mask charge will apply. Contact ICS Sales for details.

ICS Part Number	ICS1567-742	ICS1567-Custom Pattern #1
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)
0	112.000	
1	148.000	
2	OFF	
3	135.000	
4	31.500	
5	105.500	
6	78.000	
7	86.000	
8	108.000	
9	120.000	
10	128.000	
11	93.000	
12	112.000	
13	148.000	
14	135.000	
15	89.210	
16	105.500	
17	112.000	
18	25.000	
19	45.000	
20	64.000	
21	75.000	
22	78.000	
23	86.000	
24	103.000	
25	108.000	
26	120.000	
27	127.000	
28	128.000	
29	135.000	
30	112.000	
31	148.000	

Custom pattern #1 reference frequency = _____________

Standard pattern shown above uses 16.000 MHz as the input reference frequency.

Ordering Information

ICS1567M-XXX

Example:

ICS XXXX M -XXX

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS1572

User Programmable Differential Output Graphics Clock Generator

Description

The **ICS1572** is a high performance monolithic phase-locked loop (PLL) frequency synthesizer. Utilizing ICS's advanced CMOS mixed-mode technology, the **ICS1572** provides a low cost solution for high-end video clock generation in workstations and high-end PC applications.

The **ICS1572** has differential video clock outputs (CLK+ and CLK-) that are compatible with industry standard video DACs. Another clock output, LOAD, is provided whose frequency is derived from the main clock by a programmable divider. An additional clock output is available, LD/N2, which is derived from the LOAD frequency and whose modulus may also be programmed.

Operating frequencies are fully programmable with direct control provided for reference divider, pre-scaler, feedback divider and post-scaler.

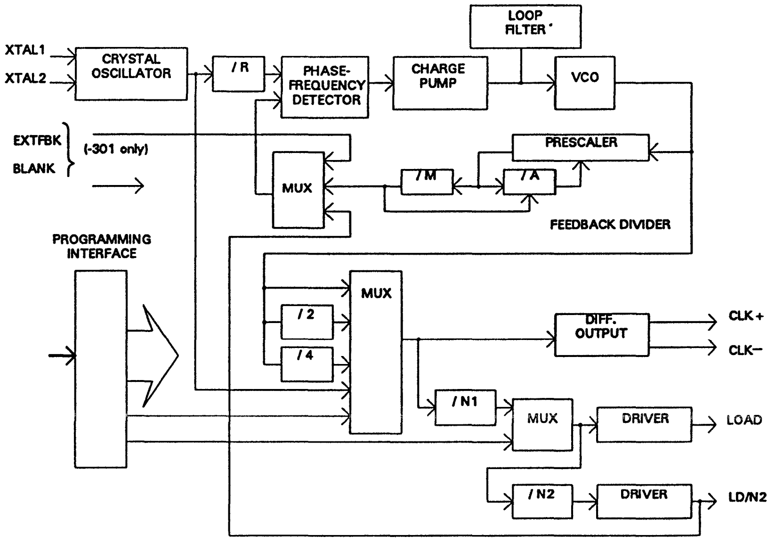
Reset of the pipeline delay on Brooktree RAMDACs™ may be performed under register control. Outputs may also be set to desired states to facilitate circuit board testing.

Features

- Supports high-resolution graphics - CLK output to 180 MHz
- Eliminates need for multiple ECL output crystal oscillators
- Fully programmable synthesizer capability - not just a clock multiplier
- Available in 20-pin 300 mil wide body SOIC package
- Available in both parallel (101) and serial (301) programming versions
- Circuit included for reset of Brooktree RAMDAC pipeline delay

Applications

- Workstations
- AutoCad Accelerators
- High-end PC graphics systems



ICS1572-101 Pinout
K-7

N.C.	1	20	N.C.
AD0	2	19	AD1
XTAL1	3	18	AD2
XTAL2	4	17	VDD
STROBE	5	16	VDD
VSS	6	15	VDDO
VSS	7	14	IPRG
LOAD	8	13	CLK+
LD/N2	9	12	CLK-
N.C	10	11	N.C.

ICS1572-301 Pinout
K-7

N.C.	1	20	N.C.
AD0	2	19	AD1
XTAL1	3	18	AD2
XTAL2	4	17	VDD
STROBE	5	16	VDD
VSS	6	15	VDDO
VSS	7	14	IPRG
LOAD	8	13	CLK+
LD/N2	9	12	CLK-
N.C.	10	11	N.C

Figure 1

RAMDAC is a trademark of Brooktree Corporation.

Overview

The **ICS1572** is ideally suited to provide the graphics system clock signals required by high-performance video DACs. Fully programmable feedback and reference divider capability allow virtually any frequency to be generated, not just simple multiples of the reference frequency. The **ICS1572** uses the latest generation of frequency synthesis techniques developed by ICS and is completely suitable for the most demanding video applications.

PLL Synthesizer Description - Ratiometric Mode

The **ICS1572** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL (see Figure 1). The reference frequency is generated by an on-chip crystal oscillator or the reference frequency may be applied to the **ICS1572** from an external frequency source.

The phase-frequency detector shown in the block diagram drives the voltage-controlled oscillator, or VCO, to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F(\text{VCO}):=\frac{F(\text{XTAL1})\cdot \text{Feedback Divider}}{\text{Reference Divider}}$$

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly programmed dividers).

The VCO gain is programmable, which permits the **ICS1572** to be optimized for best performance at all operating frequencies.

The reference divider may be programmed for any modulus from 1 to 128 in steps of one.

The feedback divider may be programmed for any modulus from 37 through 391 in steps of one. Any even modulus from 392 through 782 can also be achieved by setting the "double" bit which doubles the feedback divider modulus. The feedback divider makes use of a dual-modulus prescaler technique that allows the programmable counters to operate at low speed without sacrificing resolution. This is an improvement over conventional fixed prescaler architectures that typically impose a factor-of-four penalty (or larger) in this respect.

Table 1 permits the derivation of "A" & "M" counter programming directly from desired modulus.

PLL Post-Scaler

A programmable post-scaler may be inserted between the VCO and the CLK+ and CLK- outputs of the **ICS1572.** This is useful in generating of lower frequencies, as the VCO has been optimized for high-frequency operation.

The post-scaler allows the selection of:

- VCO frequency
- VCO frequency divided by 2
- VCO frequency divided by 4
- Internal register bit (AUXCLK) value

Load Clock Divider

The **ICS1572** has an additional programmable divider (referred to in Figure 1 as the N1 divider) that is used to generate the LOAD clock frequency for the video DAC. The modulus of this divider may be set to 3, 4, 5, 6, 8, or 10 under register control. The design of this divider permits the output duty factor to be 50/50, even when an odd modulus is selected. The input frequency to this divider is the output of the PLL post-scaler described above.

Digital Inputs - ICS1572-101 Option

The AD0-AD3 pins and the STROBE pin are used to load all control registers of the **ICS1572** (-101 option). The AD0-AD3 and STROBE pins are each equipped with a pull-up and will be at a logic HIGH level when not connected. They may be driven with standard TTL or CMOS logic families.

The address of the register to be loaded is latched from the AD0-AD3 pins by a negative edge on the STROBE pin. The data for that register is latched from the AD0-AD3 pins by a positive edge on the STROBE pin. See Figure 2 for a timing diagram. After power-up, the **ICS1572-101** requires 32 register writes for new programming to become effective. Since only 13 registers are used at present, the programming system can perform 19 "dummy" writes to address 13 or 14 to complete the sequence.

This allows the synthesizer to be completely programmed for the desired frequency before it is made active. Once the part has been "unlocked" by the 32 writes, programming becomes effective immediately.

ALL registers identified in the data sheet (0-9, 11, 12 & 15) MUST be written upon initial programming. The programming registers are not initialized upon power-up, but the latched outputs of those registers are. The latch is made transparent after 32 register writes. If any register has not been written, the state upon power-up (random) will become effective. Registers 13 & 14 physically do not exist. Register 10 does exist, but is reserved for future expansion. To insure compatibility with possible future modifications to the database, ICS recommends that all three unused locations be written with zero.

ICS1572-101 Register Loading

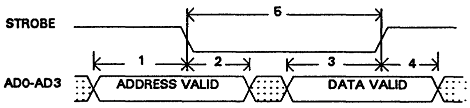


Figure 2

Digital Inputs - ICS1572-301 Option

The programming of the **ICS1572-301** is performed serially by using the DATCLK, DATA, and HOLD~pins to load an internal shift register.

DATA is shifted into the register on the rising edge of DATCLK. The logic value on the HOLD~ pin is latched at the same time. When HOLD~ is low, the shift register may be loaded without disturbing the operation of the **ICS1572**. When high, the shift register outputs are transferred to the control registers, and the new programming information becomes active. Ordinarily, a high level should be placed on the HOLD~ pin when the last data bit is presented. See Figure 3 for the programming sequence.

ICS1572-301 Register Loading

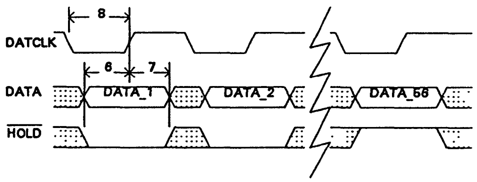


Figure 3

An additional control pin on the **ICS1572-301**, BLANK can perform either of two functions. It may be used to disable the phase-frequency detector in line-locked applications. Alternatively, the BLANK pin may be used as a synchronous enable for VRAM shift clock generation. See sections on Line-Locked Operations and VRAM shift clock generation for details.

Output Description

The differential output drivers, CLK+ and CLK, are current-mode and are designed to drive resistive terminations in a complementary fashion. The outputs are current-sinking only, with the amount of sink current programmable via the IPRG pin. The sink current, which is steered to either CLK+ or CLK-, is approximately four times the current supplied to the **IPRG** pin. For most applications, a resistor from VDDO to IPRG will set the current to the necessary precision. See Figure 6 for output characteristics.

The LOAD output is a high-current CMOS type drive whose frequency is controlled by a programmable divider that may be selected for a modulus of 3, 4, 5, 6, 8, or 10. It may also be suppressed under register control.

The LD/N2 output is high-current CMOS type drive whose frequency is derived from the LOAD output. The programmable modulus may range from 1 to 512 in steps of one.

Pipeline Delay Reset Function

The **ICS1572** implements the clocking sequence required to reset the pipeline delay on Brooktree RAMDACs. This sequence can be generated by setting the appropriate register bit (DACRST) to a logic 1 and then resetting to logic 0.

When changing frequencies, it is advisable to allow 500 microseconds after the new frequency is selected to activate the reset function. The output frequency of the synthesizer should be stable enough at that point for the video DAC to correctly execute its reset sequence. See Figure 4 for a diagram of the pipeline delay reset sequence.

Pipeline Delay Reset Timing

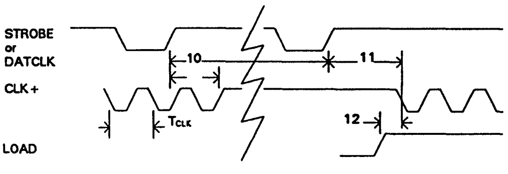


Figure 4

Reference Oscillator and Crystal Selection

The **ICS1572** has circuitry on-board to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Series-resonant crystals may also be used with the **ICS1572**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1572** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

If an external reference frequency source is to be used with the **ICS1572**, it is important that it be jitter-free. The rising and falling edges of that signal should be fast and free of noise for best results.

The loop phase is locked to the falling edges of the XTAL1 input signals.

Line-Locked Operation

The **ICS1572** supports line-locked clock applications by allowing the LOAD (N1) and N2 divider chains to act as the feedback divider for the PLL.

The N1 and N2 divider chains allow a much larger modulus to be achieved than the PLL's own feedback divider. Additionally, the output of the N2 counter is accessible off-chip for performing horizontal reset of the graphics system, where necessary. This mode is set under register control (ALTLOOP bit). The reference divider (R counter) is set to divide by 1 in this mode, and the HSYNC signal of the external video will be supplied to the XTAL1 input. The output frequency of the synthesizer will then be:

$$F_{(CLK)} : = F\ (XTAL1) \cdot N1 \cdot N2.$$

By using the phase-detector hardware disable mode, the PLL can be made to free-run at the beginning of the vertical interval of the external video, and can be reactivated at its completion.

ICS1572-101	The **ICS1572-101** supports phase detector disable via a special control mode. When the PDRSTEN (phase detector reset enable) bit is set, a high level on AD3 will disable PLL locking.
ICS1572-301	The **ICS1572-301** supports phase detector disable via the BLANK pin. When the PDRSTEN bit is set, a high level on the BLANK input will disable PLL locking.

External Feedback Operation

The **ICS1572-301** option also supports the inclusion of an external counter as the feedback divider of the PLL. This mode is useful in graphic systems that must be "genlocked" to external video sources.

When the EXTFBEN bit is set to logic 1, the phase-frequency detector will use the EXTFBK pin as its feedback input. The loop phase will be locked to the rising edges of the signal applied to the EXTFBK input.

VRAM Shift Clock Generation

The **ICS1572-301** option supports VRAM shift clock generation and interruption. By programming the N2 counter to divide by 1, the LD/N2 output becomes a duplicate of the LOAD output. When the SCEN bit is set, the LD/N2 output may be synchronously started and stopped via the blank pin. When BLANK is high, the LD/N2 will be free-running and in phase with LOAD. When BLANK is taken low, the LD/N2 output is stopped at a low level. See Figure 5 for a diagram of the sequence. Note that this use of the BLANK pin precludes its use for phase comparator disable (see Line-Locked Operation).

VRAM Shift Clock Control

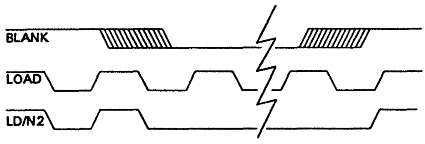


Figure 5

Power-On Initialization

The **ICS1572** has an internal power-on reset circuit that performs the following functions:

1) Sets the multiplexer to pass the reference frequency to the CLK+ and CLK- outputs.

2) Selects the modulus of the N1 divider (for the LOAD clock) to be four.

These functions should allow initialization of most graphics systems that cannot immediately provide for register programming upon system power-up.

Because the power-on reset circuit is on the VDD supply, and because that supply is filtered, care must be taken to allow the reset to de-assert before programming. A safe guideline is to allow 20 microseconds after the VDD supply reaches 4 volts.

Programming Notes

- VCO Frequency Range: Use the post-divider to keep the VCO frequency as high as possible within its operating range.
- Divider Range: For best results in normal situations (i.e., pixel clock generation for hi-res displays), keep the reference divider modulus as short as possible (for a frequency at the output of the reference divider in the few hundred kHz to several MHz range). If you need to go to a lower phase comparator reference frequency (usually required for increased frequency accuracy), that is acceptable, but jitter performance will suffer somewhat.
- VCO Gain Programming: Use the minimum gain which can reliably achieve the VCO frequency desired, as shown here:

VCO GAIN	MAX FREQUENCY
4	120 MHz
5	200 MHz
6	230 MHz
7	*

* SPECIAL APPLICATION. Contact factory for custom product above 230 MHz.

- Phase Detector Gain: For most graphics applications and divider ranges, set P[1,0] = 10 and set P[2] = 1. Under some circumstances, setting the P[2] bit "on" can reduce jitter. During 1572 operation at exact multiples of the crystal frequency, P[2] bit = 0 may provide the best jitter performance.

Board Test Support

It is often desirable to statically control the levels of the output pins for circuit board test. The **ICS1572** supports this through a register programmable mode, AUXEN. When this mode is set, two register bits directly control the logic levels of the CLK+/CLK- pins and the LOAD pin. This mode is activated when the S[0] and S[1] bits are both set to logic 1. See Register Mapping for details.

Power Supplies and Decoupling

The **ICS1572** has two VSS pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS1572** has a VDDO pin which is the supply of +5 volt power to all output drivers. This pin should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, capacitors should have low series inductance and be mounted close to the **ICS1572**.

The VDD pin is the power supply pin for the PLL synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects. See Figure 7 for typical external circuitry.

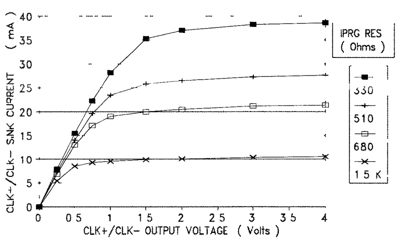


Figure 6

ICS1572 Typical Interface

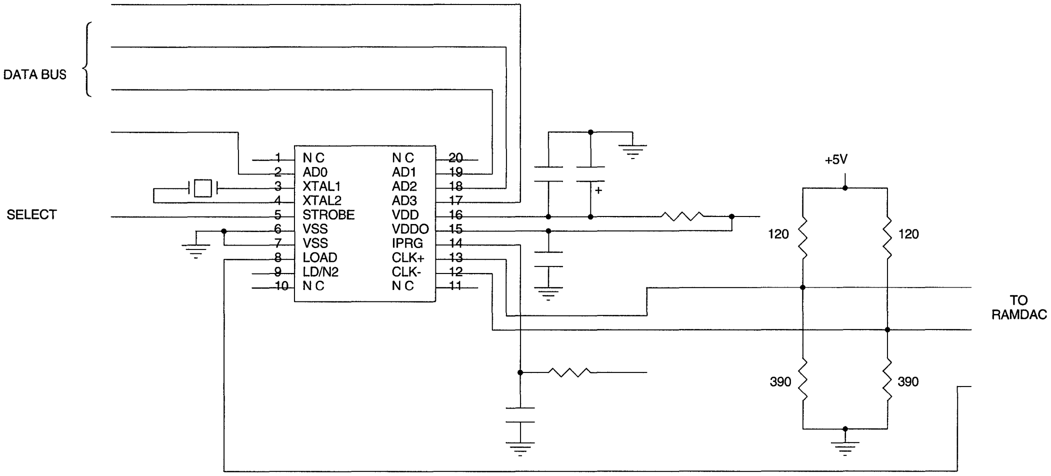


Figure 3

Register Mapping - ICS1572-101 (Parallel Programming Option)

NOTE: IT IS NOT NECESSARY TO UNDERSTAND THE FUNCTION OF THESE BITS TO USE THE ICS1572. PC SOFTWARE IS AVAILABLE FROM ICS TO AUTOMATICALLY GENERATE ALL REGISTER VALUES BASED ON REQUIREMENTS. CONTACT FACTORY FOR DETAILS.

REG#	BIT(S)	BIT REF.	DESCRIPTION
0	0-3	R[0]..R[3]	Reference divider modulus control bits
1	0-2	R[4]..R[6]	Modulus = value + 1
2	0-3	A[0]..A[3]	Controls A counter. When set to zero, modulus=7. Otherwise, modulus=7 for “value” underflows of the prescaler, and modulus=6 thereafter until M counter underflows.
3	0-3	M[0]..M[3]	M counter control bits
4	0-1	M[4]..M[5]	Modulus = value + 1
4	3	DBLFREQ	Doubles modulus of dual-modulus prescaler (from 6/7 to 12/14).
5	0-2	N1[0]..N1[2]	Sets N1 modulus according to this table. These bits are set to implement a divide-by-four on power-up.

N1[2]	N1[1]	N1[0]	RATIO
0	0	0	3
0	0	1	4
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	8
1	1	1	10

REG#	BIT(S)	BIT REF.	DESCRIPTION
6	0-3	N2[0]..N2[3]	Sets the modulus of the N2 divider. Modulus = value + 1
7	0-3	N2[4]..N2[7]	The input of the N2 divider is the output of the N1 divider in all clock modes except AUXEN.
8	3	N2[8]	
8	0-2	V[0]..V[1]	Sets the gain of the VCO.

V[2]	V[1]	V[0]	VCO GAIN (MHz/VOLT)
1	0	0	30
1	0	1	45
1	1	0	60
1	1	1	80

<table>
<tr><th>REG#</th><th>BIT(S)</th><th>BIT REF.</th><th>DESCRIPTION</th></tr>
<tr><td>9</td><td>0-1</td><td>P[0]..P[1]</td><td>Sets the gain of the phase detector according to this table.
<table>
<tr><th>P[1]</th><th>P[0]</th><th>GAIN (uA/radian)</th></tr>
<tr><td>0</td><td>0</td><td>0.05</td></tr>
<tr><td>0</td><td>1</td><td>0.15</td></tr>
<tr><td>1</td><td>0</td><td>0.5</td></tr>
<tr><td>1</td><td>1</td><td>1.5</td></tr>
</table></td></tr>
<tr><td>9</td><td>3</td><td>[P2]</td><td>Phase detector tuning bit. Normally should be set to one.</td></tr>
<tr><td>11</td><td>0-1</td><td>S[0]..S[1]</td><td>PLL post-scaler/test mode select bits
<table>
<tr><th>S[1]</th><th>S[0]</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>0</td><td>Post-scaler=1. F(CLK)=F(PLL). The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.</td></tr>
<tr><td>0</td><td>1</td><td>Post-scaler=2. F(CLK)=F(PLL)/2. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.</td></tr>
<tr><td>1</td><td>0</td><td>Post-scaler=4. F(CLK)=F(PLL)/4. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.</td></tr>
<tr><td>1</td><td>1</td><td>AUXEN CLOCK MODE. The AUXCLK bit drives the differential outputs CLK+ and CLK- and the AUXN1 bit drives the LOAD output which, in turn, drives the N2 divider.</td></tr>
</table></td></tr>
<tr><td>11</td><td>2</td><td>AUX_CLK</td><td>When in the AUXEN clock mode, this bit controls the differential outputs.</td></tr>
<tr><td>11</td><td>3</td><td>AUX_N1</td><td>When in the AUXEN clock mode, this bit controls the LOAD output (and consequently the N2 output according to its programming).</td></tr>
<tr><td>12</td><td>0</td><td>RESERVED</td><td>Must be set to zero.</td></tr>
<tr><td>12</td><td>1</td><td>JAMPLL</td><td>Tristates phase detector outputs; resets phase detector logic, and resets R, A, M, and N2 counters.</td></tr>
<tr><td>12</td><td>2</td><td>DACRST</td><td>Set to zero for normal operation. When set to one, the CLK+ output is kept high and the CLK- output is kept low. (All other device functions are unaffected.) When returned to zero, the CLK+ and CLK- outputs will resume toggling on a rising edge of the LD output (+/- 1 CLK period). To initiate a RAMDAC reset sequence, simply write a one to this register bit followed by a zero.</td></tr>
<tr><td>12</td><td>3</td><td>SELXTAL</td><td>When set to logic 1, passes the reference frequency to the post-scaler.</td></tr>
<tr><td>15</td><td>0</td><td>ALTLOOP</td><td>Controls substitution of N1 and N2 dividers into feedback loop of PLL. When this bit is a logic 1, the N1 and N2 dividers are used.</td></tr>
<tr><td>15</td><td>3</td><td>PDRSTEN</td><td>Phase-detector reset enable control bit. When this bit is set, the AD3 pin becomes a transparent reset input to the phase detector. See LINE-LOCKED CLOCK GENERATION section for more details on the operation of this function.</td></tr>
</table>

Register Mapping - ICS1572-301 (Serial Programming Option)

NOTE: IT IS NOT NECESSARY TO UNDERSTAND THE FUNCTION OF THESE BITS TO USE THE ICS1572. PC SOFTWARE IS AVAILABLE FROM ICS TO AUTOMATICALLY GENERATE ALL REGISTER VALUES BASED ON REQUIREMENTS. CONTACT FACTORY FOR DETAILS.

<table>
<tr><th>BIT(S)</th><th>BIT REF.</th><th>DESCRIPTION</th></tr>
<tr><td>1-3</td><td>N1[0]..N1[2]</td><td>Sets N1 modulus according to this table. These bits are set to implement a divide-by-four on power-up.
<table>
<tr><th>N1[2]</th><th>N1[1]</th><th>N1[0]</th><th>RATIO</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>8</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>8</td></tr>
</table></td></tr>
<tr><td>4</td><td>RESERVED</td><td>Set to zero.</td></tr>
<tr><td>5</td><td>RESERVED</td><td>MUST be set to zero.If this bit is ever programmed for a logic one, device operation will cease and further serial data load into the registers will be inhibited until a power-off/power-on sequence.</td></tr>
<tr><td>6</td><td>JAMPLL</td><td>Tristates phase detector outputs, resets phase detector logic, and resets R, A, M, and N2 counters.</td></tr>
<tr><td>7</td><td>DACRST</td><td>Set to zero for normal operations. When set to one, the CLK+ output is kept high and the CLK- output is kept low. (All other device functions are unaffected.) When returned to zero, the CLK+ and CLK- outputs will resume toggling on a rising edge of the LD output (+/–1 CLK period). To initiate a RAMDAC reset sequence, simply write a one to this register bit followed by a zero.</td></tr>
<tr><td>8</td><td>SELXTAL</td><td>When set to logic 1, passes the reference frequency to the post-scaler.</td></tr>
<tr><td>9</td><td>ALTLOOP</td><td>Controls substitution of N1 and N2 dividers into feedback loop of PLL. When this bit is a logic 1, the N1 and N2 dividers are used.</td></tr>
<tr><td>10</td><td>SCEN</td><td>VRAM shift clock enable bit. When logic 1, the BLANK pin can be used to disable the LD/N2 output.</td></tr>
<tr><td>11</td><td>EXTFBKEN</td><td>External PLL feedback select. When logic 1, the EXTFBK pin is used for the phase-frequency detector feedback input.</td></tr>
<tr><td>12</td><td>PDRSTEN</td><td>Phase detector reset enable control bit. When this bit is set, a high level on the BLANK input will disable PLL locking. See LINE-LOCKED CLOCK GENERATION section for more details on the operation of this function.</td></tr>
</table>

BIT(S)	BIT REF.	DESCRIPTION
13-14	S[0]..S[1]	PLL post-scaler/test mode select bits.

S[1]	S[0]	DESCRIPTION
0	0	Post-scaler=1. F(CLK)=F(PLL). The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
0	1	Post-scaler=2. F(CLK)=F(PLL)/2. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
1	0	Post-scaler=4. F(CLK)=F(PLL)/4. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
1	1	AUXEN CLOCK MODE. The AUXCLK bit drives the differential outputs CLK+ and CLK- and the AUXN1 bit drives the LOAD output which, in turn, drives the N2 divider.

BIT(S)	BIT REF.	DESCRIPTION
15	AUX_CLK	When in the AUXEN clock mode, this bit controls the differential outputs.
16	AUX_N1	When in the AUXEN clock mode, this bit controls the N1 output (and consequently the N2 output according to its programming).
17-24 28	N2[0]..N2[7] N2[8]	Sets the modulus of the N2 divider. The input of the N2 divider is the output of the N1 divider in all clock modes except AUXEN.
25-27	V[0]..V[2]	Sets the gain of VCO.

V[2]	V[1]	V[0]	VCO GAIN (MHz/VOLT)
1	0	0	30
1	0	1	45
1	1	0	60
1	1	1	80

BIT(S)	BIT REF.	DESCRIPTION
29-30	P[0]..P[1]	Sets the gain of the phase detector according to this table.

P[1]	P[0]	GAIN (uA/radian)
0	0	0.05
0	1	0.15
1	0	0.5
1	1	1.5

BIT(S)	BIT REF.	DESCRIPTION
31	RESERVED	Set to zero.
32	P[2]	Phase detector tuning bit. Should normally be set to one.

BIT(S)	BIT REF.	DESCRIPTION
33-38	M[0]..M[5]	M counter control bits Modulus = value +1
39	RESERVED	Set to zero.
40	DBLFREQ	Doubles modulus of dual-modulus prescaler (from 6/7 to 12/14).
41-44	A[0]..A[3]	Controls A counter. When set to zero, modulus=7. Otherwise, modulus=7 for "value" underflows of the prescaler, and modulus=6 thereafter until M counter underflows.
45-48	RESERVED	Set to zero.
49-55	R[0]..R[6]	Reference divider modulus control bits Modulus = value + 1
56	RESERVED	Set to zero.

Table 1 - "A" & "M" Divider Programming
Feedback Divider Modulus Table

A[2]..A[0]-	001	010	011	100	101	110	111	000
M[5]..M[0]								
000000								7
000001	13							14
000010	19	20						21
000011	25	26	27					28
000100	31	32	33	34				35
000101	37	38	39	40	41			42
000110	43	44	45	46	47	48		49
000111	49	50	51	52	53	54	55	56
001000	55	56	57	58	59	60	61	63
001001	61	62	63	64	65	66	67	70
001010	67	68	69	70	71	72	73	77
001011	73	74	75	76	77	78	79	84
001100	79	80	81	82	83	84	85	91
001101	85	86	87	88	89	90	91	98
001110	91	92	93	94	95	96	97	105
001111	97	98	99	100	101	102	103	112
010000	103	104	105	106	107	108	109	119
010001	109	110	111	112	113	114	115	126
010010	115	116	117	118	119	120	121	133
010011	121	122	123	124	125	126	127	140
010100	127	128	129	130	131	132	133	147
010101	133	134	135	136	137	138	139	154
010110	139	140	141	142	143	144	145	161
010111	145	146	147	148	149	150	151	168
011000	151	152	153	154	155	156	157	175
011001	157	158	159	160	161	162	163	182
011010	163	164	165	166	167	168	169	189
011011	169	170	171	172	173	174	175	196
011100	175	176	177	178	179	180	181	203
011101	181	182	183	184	185	186	187	210
011110	187	188	189	190	191	192	193	217
011111	193	194	195	196	197	198	199	224

A[2]..A[0]-	001	010	011	100	101	110	111	000
M[5]..M[0]								
100000	199	200	201	202	203	204	205	231
100001	205	206	207	208	209	210	211	238
100010	211	212	213	214	215	216	217	245
100011	217	218	219	220	221	222	223	252
100100	223	224	225	226	227	228	229	259
100101	229	230	231	232	233	234	235	266
100110	235	236	237	238	239	240	241	273
100111	241	242	243	244	245	246	247	280
101000	247	248	249	250	251	252	253	287
101001	253	254	255	256	257	258	259	294
101010	259	260	261	262	263	264	265	301
101011	265	266	267	268	269	270	271	308
101100	271	272	273	274	275	276	277	315
101101	277	278	279	280	281	282	283	322
101110	283	284	285	286	287	288	289	329
101111	289	290	291	292	293	294	295	336
110000	295	296	297	298	299	300	301	343
110001	301	302	303	304	305	306	307	350
110010	307	308	309	310	311	312	313	357
110011	313	314	315	316	317	318	319	364
110100	319	320	321	322	323	324	325	371
110101	325	326	327	328	329	330	331	378
110110	331	332	333	334	335	336	337	385
110111	337	338	339	340	341	342	343	392
111000	343	344	345	346	347	348	349	399
111001	349	350	351	352	353	354	355	406
111010	355	356	357	358	359	360	361	413
111011	361	362	363	364	365	366	367	420
111100	367	368	369	370	371	372	373	427
111101	373	374	375	376	377	378	379	434
111110	379	380	381	382	383	384	385	441
111111	385	386	387	388	389	390	391	448

Notes:

To use this table, find the desired modulus in the table. Follow the column up to find the A divider programming values. Follow the row to the left to find the M divider programming. Some feedback divisors can be achieved with two or three combinations of divider settings. Any are acceptable for use.

The formula for the effective feedback modulus is: $N = [(M + 1) \cdot 6] + A$

except when A=0, then: $N = (M + 1) \cdot 7$

Under all circumstances: $A \leq M$

Pin Descriptions - ICS1572-101

PIN#	NAME	DESCRIPTION
13	CLK+	Clock out (non-inverted)
12	CLK–	Clock out (inverted)
8	LOAD	Load output. This output is normally at the CLK frequency divided by N1.
3	XTAL1	Quartz crystal connection 1/external reference frequency input
4	XTAL2	Quartz crystal connection 2
2	AD0	Address/Data Bit 0 (LSB)
19	AD1	Address/Data Bit 1
18	AD2	Address/Data Bit 2
17	AD3	Address/Data Bit 3 (MSB)
9	LD/N2	Divided LOAD output. See text.
5	STROBE	Control for address/data latch
16	VDD	PLL system power (+5V. See application diagram.)
15	VDDO	Output stage power (+5V)
14	IPRG	Output stage current set
6,7	VSS	Device ground. Both pins must be connected to the same ground potential.
1,10,11,20	NC	Not connected

Pin Descriptions - ICS1572-301

PIN#	NAME	DESCRIPTION
13	CLK+	Clock out (non-inverted)
12	CLK–	Clock out (inverted)
8	LOAD	Load output. This output is normally at the CLK frequency divided by N1.
3	XTAL1	Quartz crystal connection 1/external reference frequency input
4	XTAL2	Quartz crystal connection 2
5	DATCLK	Data Clock (Input)
19	DATA	Serial Register Data (Input)
18	HOLD~	$\overline{\text{HOLD}}$ (Input)
17	BLANK	Blanking (Input). See Text.
9	LD/N2	Divided LOAD output/shift clock. See text.
2	EXTFBK	External feedback connection for PLL (input). See text.
16	VDD	PLL system power (+5V. See application diagram.)
15	VDDO	Output stage power (+5V)
14	IPRG	Output stage current set
6,7	VSS	Device ground. Both pins must be connected.
1,10,11,20	NC	Not connected

Absolute Maximum Ratings

VDD, VDDO (measured to VSS)	7.0V
Digital Inputs	V_{SS}-0.5 to V_{DD} + 0.5V
Digital Outputs	V_{SS}-0.5 to V_{DDO} + 0.5V
Ambient Operating Temperature	-55 to 125°C
Storage Temperature	-65 to 150°C
Junction Temperature	175°C
Soldering Temperature	260°C

Recommended Operating Conditions

VDD, VDDO (measured to VSS)	4.75 to 5.25V
Operating Temperature (Ambient)	0 to 70°C

DC Characteristics

TTL-Compatible Inputs
101 Option - (AD0-AD3, STROBE),
301 Option - (DATCLK, DATA, $\overline{\text{HOLD}}$, BLANK, EXTFBK)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{ih}		2.0	V_{DD}+0.5	V
Input Low Voltage	V_{il}		V_{SS}-0.5	0.8	V
Input High Current	I_{ih}	V_{ih} =VDD	-	10	uA
Input Low Current	I_{il}	V_{il} =0.0	-	150	uA
Input Capacitance	C_{in}		-	8	pf

XTAL1 Input

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{xh}		3.75	V_{DD}+0.5	V
Input Low Voltage	V_{xl}		V_{SS}-0.5	1.25	

CLK+, CLK- Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Differential Output Voltage			0.6	-	V

LOAD, LD/N2 Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output High Voltage (Ioh=4.0mA)			2.4	-	V
Output Low Voltage (Iol=8.0mA)			-	0.4	V

AC Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
F_{vco}	VCO Frequency (see Note 1)	20		160	MHz
F_{xtal}	Crystal Frequency	5		20	MHz
C_{par}	Crystal Oscillator Loading Capacitance		20		pf
F_{load}	LOAD Frequency			80	MHz
T_{xhi}	XTAL1 High Time (when driven externally)	8			ns
T_{xlo}	XTAL1 Low TIme (when driven externally)	8			ns
T_{high}	Differential Clock Output Duty Cycle (see Note 2)	45		55	%
J_{clk}	Differential Clock Output Cumulative Jitter (see Note 3)		<0.06		pixel
T_{lock}	PLL Acquire Time (to within 1%)		500		µs
I_{dd}	VDD Supply Current		15	t.b.d.	mA
I_{ddo}	VDDO Supply Current (excluding CLK+/- termination)		20	t.b.d.	mA
DIGITAL INPUTS - ICS1572-101					
1	Address Setup Time	10			ns
2	Address Hold Time	10			ns
3	Data Setup Time	10			ns
4	Data Hold Time	10			ns
5	STROBE Pulse Width (T_{hi} or T_{lo})	20			ns
DIGITAL OUTPUTS - ICS1572-301					
6	DATA/HOLD~Setup Time	10			ns
7	DATA/HOLD~Hold Time	10			ns
8	DATCLK Pulse Width (T_{hi} or T_{lo})	20			ns
PIPELINE DELAY RESET					
9	Reset Activation Time			2*Tclk	ns
10	Reset Duration	4*Tload			ns
11	Restart Delay			2*Tload	ns
12	Restart Matching	-!*Tclk		+1.5*Tclk	ns
DIGITAL OUTPUTS					
13	CLK+/CLK- Clock Rate			180	MHz
14	LOAD To LD/N2 Skew (Shift Clock Mode)	-2	0	+2	ns

Note 1: Use of the post-divider is required for frequencies lower than 20 MHz on CLK+ & CLK- outputs. Use of the post-divider is recommended for output frequencies lower than 65 MHz.

Note 2: Using load circuit of Figure 6. Duty cycle measured at zero crossings of difference voltage between CLK+ and CLK-.

Note 3: Cumulative jitter is defined as the maximum error (in the time domain) of any CLK edge, at any point in time, compared with the equivalent edge generated by an ideal frequency source.

ICS laboratory testing indicates that the typical value shown above can be treated as a maximum jitter specification in virtually all applications. Jitter performance can depend somewhat on circuit board layout, decoupling, and register programming.

Ordering Information

ICS1572M-101 or ICS1572M-301

Example:

ICS XXXX M -XXX

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

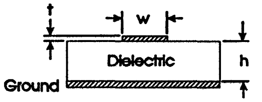
Prefix
ICS, AV=Standard Device; GSP=Genlock Devic

Output Circuit Considerations for the ICS1572

Output Circuitry

The dot clock signals CLK and CLK- are typically the highest frequency signals present in the workstation. To minimize problems with EMI, crosstalk, and capacitive loading extra care should be taken in laying out this area of the PC board. The **ICS1572** is packaged in a 0.3"-wide 20-pin SOIC package. This permits the clock generator, crystal, and related components to be laid out in an area the size of a postage stamp. The **ICS1572** should be placed as close as possible to the RAMDAC. The CLK and CLK- pins are running at VHF frequencies; one should minimize the length of PCB trace connecting them to the RAMDAC so that they don't become radiators of RF energy.

At the frequencies that the **ICS1572** is capable of, PC board traces may be long enough to be a significant portion of a wavelength of that frequency. PC traces for CLK and CLK- should be treated as transmission lines, not just interconnecting wires. These lines can take two forms: microstrip and stripline. A microstrip line is shown below:



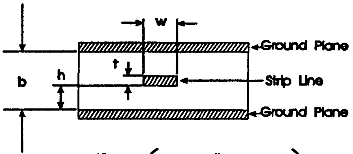
$$Z_o = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8w+t}\right)$$

Dimensions in Inches

Microstrip Line

Essentially, the microstrip is a copper trace on a PCB over a ground plane. Typically, the dielectric is G10 glass epoxy. It differs from a standard PCB trace in that its width is calculated to have a characteristic impedance. To calculate the characteristic impedance of a microstrip line one must know the width and thickness of the trace, and the thickness and dielectric constant of the dielectric. For G10 glass epoxy, the dielectric constant (e_r) is about 5. Propagation delay is strictly a function of dielectric constant. For G10 propagation, delay is calculated to be 1.77 ns/ft.

Stripline is the other form a PCB transmission line can take. A buried trace between ground planes (or between a power plane and a ground plane) is common in multi-layer boards. Attempting to create a workstation design without the use of multi-layer boards would be adventurous to say the least, the issue would more likely be whether to place the interconnect on the surface or between layers. The between layer approach would work better from an EMI standpoint, but would be more difficult to lay out. A stripline is shown below:



$$Z_o = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4b}{0.067 \pi w\left(0.8 + \frac{t}{w}\right)}\right)$$

Dimensions in Inches

Stripline

Using 1oz. copper (0.0015" thick) and 0.040" thickness G10, a 0.010" trace will exhibit a characteristic impedance of 75Ω in a stripline configuration.

Typically, RAMDACS require a V_{ih} of V_{AA}-1.0 Volts as a guaranteed logical "1" and a V_{il} of V_{AA}-1.6 as a guaranteed logical "0." Worst case input capacitance is 10 pf.

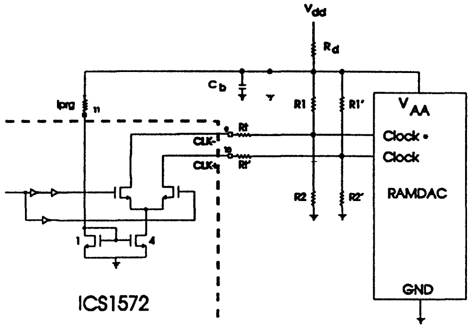
Output circuitry for the **ICS1572** is shown in the following diagram. It consists of a 4/1 current mirror, and two open drain output FETs along with inverting buffers to alternately enable each current-sinking driver. Both CLK and CLK- outputs are connected to the respective CLOCK and CLOCK* inputs of the RAMDAC with transmission lines and terminated in their equivalent impedances by the Thevenin equivalent impedances of R1 and R2 or R1' and R2'.

The **ICS1572** is incapable of sourcing current, so V_{ih} must be set by the ratios of these resistors for each of these lines. R1 and R2 are electrically in parallel from an AC standpoint because V_{dd} is bypassed to ground through bypass-capacitor network C_b. If we picked a target impedance of 75Ω for our transmission line impedance, a value of 91Ω for R1 and R1' and a value of 430Ω for R2 and R2' would yield a Thevinin equivalent characteristic impedance of 75.1W and a Vih value of VAA-.873 Volts, a margin of 0.127Volts. This may be adequate; however, at higher frequencies one must contend with the 10 pF input capacitance of the RAMDAC. Values of 82Ω for R1 and R1' and 820Ω for R2 and R2' would give us a characteristic impedance of 74.5Ω and a V_{ih} value of V_{AA}-.45. With a .55 Volt margin on V_{ih}, this voltage level might be safer.

To set a value for V_{il}, we must determine a value for I_{prg} that will cause the output FET's to sink an appropriate current. We desire V_{il} to be V_{AA}-1.6 or greater. V_{AA}-2 would seem to be a safe value. Setting up a sink current of 25 milliamperes would guarantee this through our 82Ω pull-up resistors. As this is controlled by a 4/1 current mirror, 7 mA into I_{prg} should set this current properly. A 510Ω resistor from V_{dd} to I_{prg} should work fine.

Resistors Rt and Rt' are shown as series terminating resistors at the **ICS1572** end of the transmission lines. These are not required for operation, but may be useful for meeting EMI requirements. Their intent is to interact with the input capacitance of the RAMDAC and the distributed capacitance of the transmission line to soften up rise and fall times and consequently cut some of the high-order harmonic content that is more likely to radiate RF energy. In actual usage they would most likely be 10 to 20Ω resistors or possibly ferrite beads.

C_b is shown as multiple capacitors. Typically, a 22 µF tantalum should be used with separate .1 µF and 220pf capacitors placed as close to the pins as possible. This provides low series inductance capacitors right at the source of high frequency energy. R_d is used to isolate the circuitry from external sources of noise. Five to ten ohms should be adequate.



ICS1572 Output Circuitry

Great care must be used when evaluating high frequency circuits to achieve meaningful results. The 10pf input capacitance and long ground lead of an ordinary scope probe will make any measurements made with it meaningless. A low capacitance FET probe with a ground connection directly connected to the shield at the tip will be required. A 1GHz bandwidth scope will be barely adequate, try to find a faster unit.

Integrated Circuit Systems, Inc.

ICS1574

User Programmable Laser Engine Pixel Clock Generator

Description

The **ICS1574** is a very high performance monolithic phase-locked loop (PLL) frequency synthesizer designed for laser engine applications. Utilizing ICS's advanced CMOS mixed-mode technology, the **ICS1574** provides a low cost solution for high-end pixel clock generation for a variety of laser engine product applications.

The pixel clock output (PCLK) frequency is derived from the main clock by a programmable resettable divider.

Operating frequencies are fully programmable with direct control provided for reference divider, feedback divider and post-scaler.

Features

- Supports high resolution laser graphics. PLL/VCO frequency re-programmable through serial interface port to 400 MHz; allows less than ±1.5ns pixel clock resolution.
- Laser pixel clock output is synchronized with conditioned beam detect input
- Ideal for laser printer, copier and FAX pixel clock applications
- On-chip PLL with internal loop filter
- On-chip XTAL oscillator frequency reference
- Resettable, programmable counter gives glitch-free clock alignment
- Single 5 volt power supply
- Low power CMOS technology
- Compact - 16-pin 0.150" skinny SOIC package
- User re-programmable clock frequency supports zoom and gray scale functions

Block Diagram

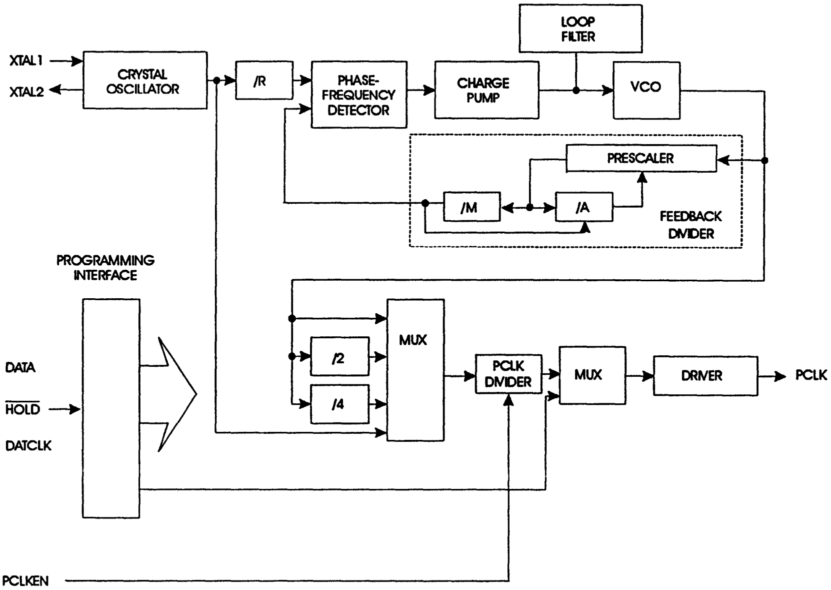
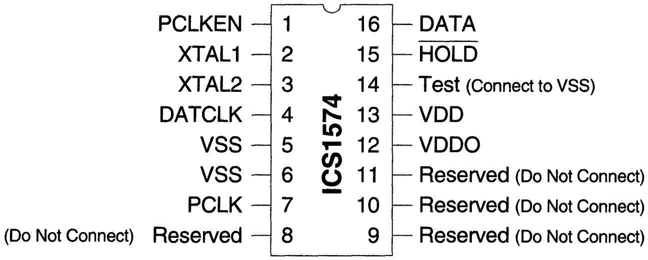


Figure 1

Pin Configuration



16-Pin skinny SOIC
K-6

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
7	PCLK	Pixel clock output.
1	PCLKEN	PCLK Enable (Input).
2	XTAL1	Quartz crystal connection 1 / external reference frequency input.
3	XTAL2	Quartz crystal connection 2.
4	DATCLK	Data Clock (Input).
16	DATA	Serial Register Data (Input).
15	$\overline{\text{HOLD}}$	$\overline{\text{HOLD}}$ (Input).
14	Test	Test. (Must be connected to VSS.)
8, 9, 10, 11	Reserved	Reserved. (Do Not Connect.)
13	VDD	PLL system power (+5V. See application diagram).
12	VDDO	Output stage power (+5V).
5, 6	VSS	Device ground. (Both pins must be connected.)

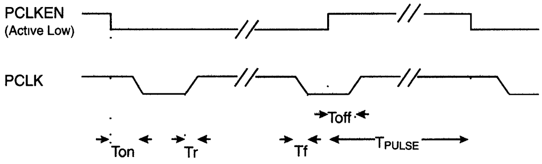
PCLK Programmable Divider

The **ICS1574** has a programmable divider (referred to in Figure 1 as the PCLK divider) that is used to generate the PCLK clock frequency for the pixel clock output. The modulus of this divider may be set to 3, 4, 5, 6, 8, 10, 12, 16 or 20 under register control. The design of this divider permits the output duty factor to be 50/50, even when an odd modulus is selected. The input frequency to this divider is the output of the PLL post-scaler described below:

The phase of the PCLK output is aligned with the internal high frequency PLL clock (F_{VCO}) immediately after the assertion of the PCLKEN input pulse (active low if PCLKEN_POL bit is 0 or active high if PCLKEN_POL bit is 1).

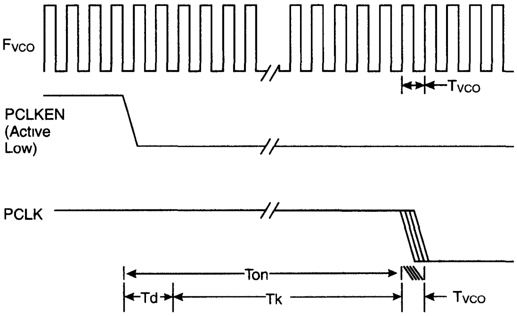
When PCLKEN is deasserted, the PCLK output will complete its current cycle and remain at VDD until the next PCLKEN pulse. The minimum time PCLKEN must be disabled (T_{PULSE}) is $1/F_{PCLK}$.

See Figure 2a for an example of PCLKEN enable (negative polarity) vs. PCLK timing sequences.



$T_{off} < T_{PCLK}$, $T_{PCLK} = 1/F_{PCLK}$
$T_{PULSE} > T_{PCLK}$

Figure 2a



$T_K = K \bullet T_{VCO}$
T_d=LOGIC PROP.DELAY TIME
(typically 9ns with a 10pF load on PCLK)
$T_{VCO} = 1/F_{VCO}$

Figure 2b

The resolution of Ton is one VCO cycle.

The time required for a PCLK cycle start following a PCLKEN enable is described by Figure 2b and the following table:

K Values	
PCLK Divider	**K**
3	2
4a	3.5
4b	3
5	4.5
6	3.5
8a	5.5
8b	5
10	7
12	6.5
16a	9.5
16b	9
20	12

Typical values for Tr and Tf with a 10pF load on PCLK are 1ns.

PLL Post-Scaler

A programmable post-scaler may be inserted between the VCO and the PCLK divider of the **ICS1574**. This is useful in generating lower frequencies, as the VCO has been optimized for high-frequency operation. The post-scaler is not affected by the PCLKEN input.

The post-scaler allows the selection of:

- VCO frequency
- VCO frequency divided by 2
- VCO frequency divided by 4
- AUX-EN Test Mode

PLL Synthesizer Description - Ratiometric Mode

The **ICS1574** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL (see Figure 1). The reference frequency is generated by an on-chip crystal oscillator or the reference frequency may be applied to the **ICS1574** from an external frequency source.

The phase-frequency detector shown in the block diagram drives the voltage-controlled oscillator, or VCO, to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F(\text{VCO}) := \frac{F(\text{XTAL1}) \cdot \text{Feedback Divider}}{\text{Reference Divider}}$$

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly programmed dividers).

The VCO gain is programmable, which permits the **ICS1574** to be optimized for best performance at all operating frequencies.

The reference divider may be programmed for any modulus from 1 to 128 in steps of one.

The feedback divider may be programmed for any modulus from 37 through 392 in steps of one. Any even modulus from 392 through 784 can also be achieved by setting the "double" bit which doubles the feedback divider modulus. The feedback divider makes use of a dual-modulus prescaler technique that allows the programmable counters to operate at low speed without sacrificing resolution. This is an improvement over conventional fixed prescaler architectures that typically impose a factor-of-four (or larger) penalty in this respect.

Table 1 permits the derivation of "A" & "M" converter programming directly from desired modulus.

Digital Inputs

The programming of the **ICS1574** is performed serially by using the DATCLK, DATA, and $\overline{\text{HOLD}}$ pins to load an internal shift register.

DATA is shifted into the register on the rising edge of DATCLK. The logic value on the $\overline{\text{HOLD}}$ pin is latched at the same time. When $\overline{\text{HOLD}}$ is low, the shift register may be loaded without disturbing the operation of the **ICS1574**. When high, the shift register outputs are transferred to the control registers, and the new programming information becomes active. Ordinarily, a high level should be placed on the $\overline{\text{HOLD}}$ pin when the last data bit is presented. See Figure 3 for the programming sequence.

The PCLKEN input polarity may be programmed under register control via Bit 39.

ICS1574 Register Loading

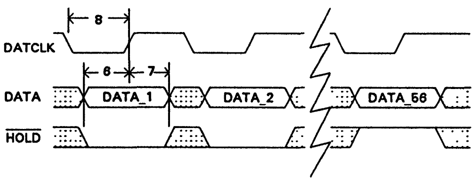


Figure 3

Output Description

The PCLK output is a high-current CMOS type drive whose frequency is controlled by a programmable divider that may be selected for a modulus of 3, 4, 5, 6, 8, 10, 12, 16 or 20. It may also be suppressed under register control via Bit 46.

Reference Oscillator and Crystal Selection

The **ICS1574** has circuitry on-board to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Series-resonant crystals may also be used with the **ICS1574**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1574** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

If an external reference frequency source is to be used with the **ICS1574**, it is important that it be jitter-free. The rising and falling edges of that signal should be fast and free of noise for best results.

The loop phase can be locked to either the rising or falling edges of the XTAL1 input signals, and is controlled by Bit 56.

Power-On Initialization

The **ICS1574** has an internal power-on reset circuit that performs the following functions:

1) Selects the modulus of the PCLK divider to be four (4).

2) Sets the multiplexer to pass the reference frequency to PCLK divider input.

These functions should allow initialization for most applications that cannot immediately provide for register programming upon system power-up.

Because the power-on reset circuit is on the VDD supply, and because that supply is filtered, care must be taken to allow the reset to de-assert before programming. A safe guideline is to allow 20 microseconds after the VDD supply reaches 4 volts.

Programming Notes

- VCO Frequency Range: Use the post-divider to keep the VCO frequency as high as possible within its operating range.
- Divider Range: For best results in normal situations keep the reference divider modulus as short as possible (for a frequency at the output of the reference divider in the few hundred kHz to several MHz range). If you need to go to a lower phase comparator reference frequency (usually required for increased frequency accuracy), that is acceptable, but jitter performance will suffer somewhat.
- VCO Gain Programming: Use the minimum gain which can reliably achieve the VCO frequency desired, as shown here:

VCO GAIN	MAX FREQUENCY
4	100 MHz
5	200 MHz
6	300 MHz
7	400 MHz

- Phase Detector Gain: For most applications and divider ranges, set P[1,0] = 10 and set P[2] = 1. Under some circumstances, setting the P[2] bit "on" can reduce jitter. During operation at exact multiples of the crystal frequency, P[2] bit = 0 may provide the best jitter performance.

Board Test Support

It is often desirable to statically control the levels of the output pins for circuit board test. The **ICS1574** supports this through a register programmable mode, AUX-EN. When this mode is set, a register bit directly controls the logic level of the PCLK pin. This mode is activated when the S[0] and S[1] bits are both set to logic 1. See Register Mapping for details.

Power Supplies and Decoupling

The **ICS1574** has two VSS pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the PCB as close to the package as is possible.

The **ICS1574** has a VDDO pin which is the supply of +5 volt power to the output driver. This pin should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, capacitors should have low series inductance and be mounted close to the **ICS1574**.

The VDD pin is the power supply pin for the PLL synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects. See Figure 4 for typical external circuitry.

a)

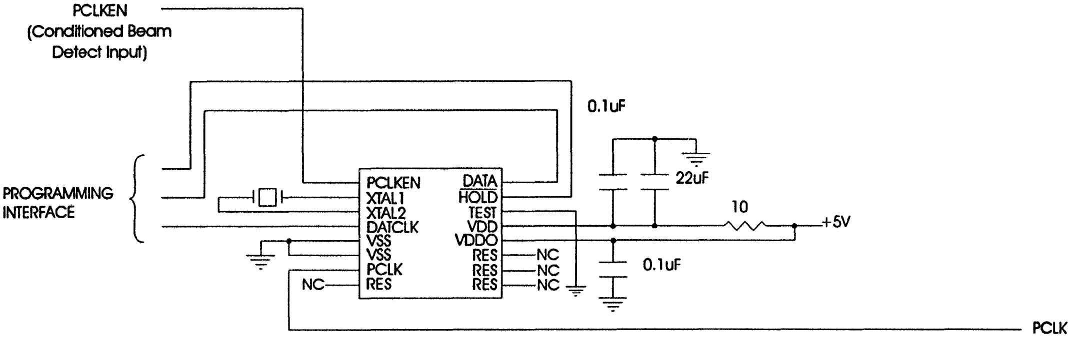

PCLKEN
(Conditioned Beam
Detect Input)
PROGRAMMING
INTERFACE
PCLKEN
XTAL1
XTAL2
DATCLK
VSS
VSS
PCLK
RES
NC
DATA
HOLD
TEST
VDD
VDDO
RES
RES
RES
NC
NC
NC
0.1uF
22uF
10
+5V
0.1uF
PCLK

Figure 4

Register Mapping - ICS1574

NOTE: IT IS NOT NECESSARY TO UNDERSTAND THE FUNCTION OF THESE BITS TO USE THE ICS1574. PC SOFTWARE IS AVAILABLE FROM ICS TO AUTOMATICALLY GENERATE ALL REGISTER VALUES BASED ON REQUIREMENTS. CONTACT FACTORY FOR DETAILS.

BIT(S)	BIT REF.	DESCRIPTION
1-4	PCLK[0]..PCLK[3]	Sets PCLK divider modulus according to this table. These bits are set to implement a divide-by-four on power-up.

PCLK[3]	PCLK[2]	PCLK[1]	PCLK[0]	MODULUS
0	0	0	0	3
0	0	0	1	4(a)
0	0	1	0	4(b)
0	0	1	1	5
0	1	0	0	6
0	1	0	1	8(a)
0	1	1	0	8(b)
0	1	1	1	10
1	X	0	0	12
1	X	0	1	16(a)
1	X	1	0	16(b)
1	X	1	1	20

X=Don't care

5, 6	Reserved	Must be set to 0.
7	Reserved	Must be set to 1.
8	SELXTAL	Normally set to 0. When set to logic 1, passes the reference frequency to the post-scaler instead of the PLL output (defaults to 1 on power-up).
9	Reserved	Must be set to 0.
10	Reserved	Must be set to 1.
11, 12	Reserved	Must be set to 0.
13-14	S[0]..S[1]	PLL post-scaler/test mode select bits.

S[1]	S[0]	DESCRIPTION
0	0	Post-scaler=1. F(CLK)=F(PLL). The output of the PCLK divider drives the PCLK output.
0	1	Post-scaler=2. F(CLK)=F(PLL)/2. The output of the PCLK divider drives the PCLK output.
1	0	Post-scaler=4. F(CLK)=F(PLL)/4. The output of the PCLK divder drives the PCLK output.
1	1	AUX-EN TEST MODE. The AUX_PCLK bit dirves the PCLK output.

BIT(S)	BIT REF.	DESCRIPTION
15	Reserved	Must be set to 0.
16	AUX_PCLK	Must be set to 0 except when in the AUX-EN test mode. When in the AUX-EN test mode, this bit controls the PCLK output.
17-24	Reserved	Must be set to 0.
25-27	V[0]..V[2]	Sets the gain of VCO.

V[2]	V[1]	V[0]	VCO GAIN (MHz/VOLT)
1	0	0	30
1	0	1	45
1	1	0	60
1	1	1	80

28	Reserved	Must be set to 1.
29-30	P[0]..P[1]	Sets the gain of the phase detector according to this table.

P[1]	P[0]	GAIN (uA/radian)
0	0	0.05
0	1	0.15
1	0	0.5
1	1	1.5

31	Reserved	Must be set to 0.
32	P[2]	Phase detector tuning bit. Should normally be set to one. See text.
33-38	M[0]..M[5]	M counter control bits Modulus = value +1
39	PCLKEN_POL	When=0, PCLK output enabled when PCLKEN input is low. When=1, PCLK output enabled when PCLKEN input is high.
40	DBLFREQ	Doubles modulus of dual-modulus prescaler (from 6/7 to 12/14).
41-44	A[0]..A[3]	Controls A counter. When set to zero, modulus=7. Otherwise, modulus=7 for "value" underflows of the prescaler, and modulus=6 thereafter until M counter underflows.

BIT(S)	BIT REF.	DESCRIPTION
45	Reserved	Must be set to 1.
46	PCLK_EN	Must be set to 0. Disables the PCLK divider when set to 1 regardless of PCLKEN input state.
47, 48	Reserved	Must be set to 0.
49-55	R[0]..R[6]	Reference divider modulus control bits Modulus = value + 1
56	REF_POL	PLL locks to rising edge of XTAL1 input when REFPOL=1, falling edge of XTAL1 when REFPOL=0

Table 1 - "A" & "M" Divider Programming
Feedback Divider Modulus Table

A[2]..A[0]-	001	010	011	100	101	110	111	000
M[5]..M[0]								
000000								7
000001	13							14
000010	19	20						21
000011	25	26	27					28
000100	31	32	33	34				35
000101	37	38	39	40	41			42
000110	43	44	45	46	47	48		49
000111	49	50	51	52	53	54	55	56
001000	55	56	57	58	59	60	61	63
001001	61	62	63	64	65	66	67	70
001010	67	68	69	70	71	72	73	77
001011	73	74	75	76	77	78	79	84
001100	79	80	81	82	83	84	85	91
001101	85	86	87	88	89	90	91	98
001110	91	92	93	94	95	96	97	105
001111	97	98	99	100	101	102	103	112
010000	103	104	105	106	107	108	109	119
010001	109	110	111	112	113	114	115	126
010010	115	116	117	118	119	120	121	133
010011	121	122	123	124	125	126	127	140
010100	127	128	129	130	131	132	133	147
010101	133	134	135	136	137	138	139	154
010110	139	140	141	142	143	144	145	161
010111	145	146	147	148	149	150	151	168
011000	151	152	153	154	155	156	157	175
011001	157	158	159	160	161	162	163	182
011010	163	164	165	166	167	168	169	189
011011	169	170	171	172	173	174	175	196
011100	175	176	177	178	179	180	181	203
011101	181	182	183	184	185	186	187	210
011110	187	188	189	190	191	192	193	217
011111	193	194	195	196	197	198	199	224

A[2]..A[0]-	001	010	011	100	101	110	111	000
M[5]..M[0]								
100000	199	200	201	202	203	204	205	231
100001	205	206	207	208	209	210	211	238
100010	211	212	213	214	215	216	217	245
100011	217	218	219	220	221	222	223	252
100100	223	224	225	226	227	228	229	259
100101	229	230	231	232	233	234	235	266
100110	235	236	237	238	239	240	241	273
100111	241	242	243	244	245	246	247	280
101000	247	248	249	250	251	252	253	287
101001	253	254	255	256	257	258	259	294
101010	259	260	261	262	263	264	265	301
101011	265	266	267	268	269	270	271	308
101100	271	272	273	274	275	276	277	315
101101	277	278	279	280	281	282	283	322
101110	283	284	285	286	287	288	289	329
101111	289	290	291	292	293	294	295	336
110000	295	296	297	298	299	300	301	343
110001	301	302	303	304	305	306	307	350
110010	307	308	309	310	311	312	313	357
110011	313	314	315	316	317	318	319	364
110100	319	320	321	322	323	324	325	371
110101	325	326	327	328	329	330	331	378
110110	331	332	333	334	335	336	337	385
110111	337	338	339	340	341	342	343	392
111000	343	344	345	346	347	348	349	399
111001	349	350	351	352	353	354	355	406
111010	355	356	357	358	359	360	361	413
111011	361	362	363	364	365	366	367	420
111100	367	368	369	370	371	372	373	427
111101	373	374	375	376	377	378	379	434
111110	379	380	381	382	383	384	385	441
111111	385	386	387	388	389	390	391	448

Notes:

To use this table, find the desired modulus in the table. Follow the column up to find the A divider programming values. Follow the row to the left to find the M divider programming. Some feedback divisors can be achieved with two or three combinations of divider settings. Any are acceptable for use.

The formula for the effective feedback modulus is: $N =[(M +1) \cdot 6] +A$

except when A=0, then: $N=(M +1) \cdot 7$

Under all circumstances: $A \leq M$

Absolute Maximum Ratings

VDD, VDDO (measured to V_{SS})	7.0 V
Digital Inputs	V_{SS}-0.5 to V_{DD} + 0.5 V
Digital Outputs	V_{SS}-0.5 to V_{DDO} + +0.5 V
Ambient Operating Temperature	-55 to 125°C
Storage Temperature	-65 to 150°C
Junction Temperature	175°C
Soldering Temperature	260°C

Recommended Operating Conditions

VDD, VDDO (measured to V_{SS})	4.75 to 5.25 V
Operating Temperature (Ambient)	0 to 70°C

DC Characteristics

TTL-Compatible Inputs
(DATCLK, DATA, $\overline{\text{HOLD}}$, PCLKEN)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{ih}		2.0	V_{DD}+0.5	V
Input Low Voltage	V_{il}		V_{SS}-0.5	0.8	V
Input High Current	I_{ih}	V_{ih}=VDD	-	10	uA
Input Low Current	I_{il}	V_{il}=0.0	-	200	uA
Input Capacitance	C_{in}		-	8	pF
Hysterisis (DATCLK input)	V_{HYS}	VDD=5V	.20	.60	V

XTAL1 Input (External Reference Frequency)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{xh}		3.75	V_{DD}+0.5	V
Input Low Voltage	V_{xl}		V_{SS}-0.5	1.25	

PCLK

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output High Voltage (Ioh = 4.0mA)			2.4	-	V
Output Low Voltage (Iol = 8.0mA)			-	0.4	V

AC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
VCO Frequency	F_{vco}	40		400	MHz
Crystal Frequency	F_{xtal}	5		20	MHz
Crystal Oscillator Loading Capacitance	C_{par}		20		pF
XTAL1 High Time (when driven externally)	T_{xhi}	8			ns
XTAL1 Low Time (when driven externally)	T_{xlo}	8			ns
PLL Acquire Time (to within 1%)	T_{lock}		500		µs
VDD Supply Current	I_{dd}		15	t.b.d.	mA
VDDO Supply Current	I_{ddo}		20	t.b.d.	mA
DIGITAL INPUTS					
DATA/HOLD˜ Setup Time		10			ns
DATA/HOLD˜ Hold Time		10			ns
DATCLK Pulse Width (T_{hi} or T_{lo})		20			ns
DIGITAL OUTPUT					
PCLK output rate	FP_{CLOCK}			130	MHz

16-Pin Skinny SOIC Package

Ordering Information

ICS1574M / ICS1574EB

Example:

ICS XXXX M

Package Type
M=SOIC
EB=Evaluation Board
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated Circuit Systems, Inc.

ICS1577

Advance Information

High Performance DEC Alpha™ CPU Clock

Description

The **ICS1577** is a high performance monolithic phase locked loop (PLL) frequency synthesizer. Utilizing ICS's advanced CMOS mixed mode technology, the **ICS1577** provides a low cost solution for high-end DEC Alpha CPU clock generation.

The **ICS1577** has differential CPU clock outputs (CLK+ and CLK-) that are compatible with the DEC Alpha CPU operating up to 466 MHz. The differential output frequency on this version of the **ICS1577** is set to an exact multiple (28 times) of the crystal oscillator or reference frequency.

Features

- CLK operation to 466 MHz
- Operates from a single crystal or reference frequency
- User-programmable output voltage levels
- Independent PLL synthesizer and output driver power supply inputs - provides voltage isolation for improved high frequency operation
- Fully user-programmable version available - allows "on-the-fly" output frequency changes useful for 'power-down' modes or 'low power' applications. Contact factory for information.
- 100ps max cycle-to-cycle jitter
- Low power consumption CMOS technology
- 14-pin DIP package

Simplified Block Diagram - ICS1577

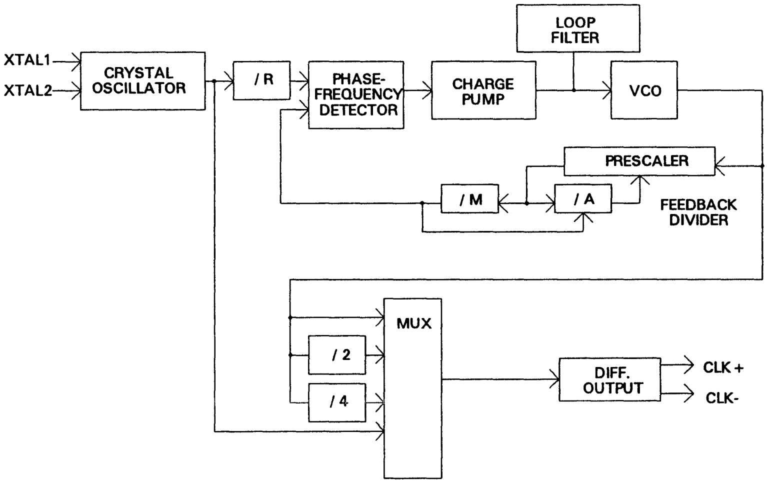
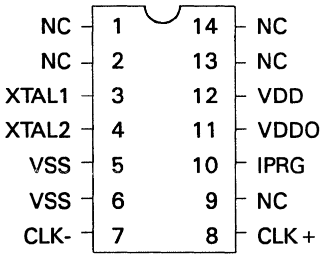


Figure 1



14-Pin DIP package K-3

Alpha is a trademark of Digital Equipment Corporation

Overview

The **ICS1577** is ideally suited to provide the CPU clock signals required by high-performance Alpha processors. The **ICS1577** provides up to a 466 MHz (Fxtal x 28) low jitter clock.

Output Description

The differential output drivers, CLK+ and CLK, are current-mode and are designed to drive resistive terminations in a complementary fashion. The outputs are current-sinking only, with the amount of sink current programmable via the IPRG pin. The sink current, which is steered to either CLK+ or CLK-, is approximately four times the current supplied to the **IPRG** pin. For most applications, a resistor from VDDO to IPRG will set the current to the necessary precision. See Figure 2 for output characteristics.

Reference Oscillator and Crystal Selection

The **ICS1577** has circuitry on-board to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Series-resonant crystals may also be used with the **ICS1577**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1577** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

If an external reference frequency source is to be used with the **ICS1577**, it is important that it be jitter-free. The rising and falling edges of that signal should be fast and free of noise for best results.

The loop phase is locked to the falling edges of the XTAL1 input signals.

Power-On Initialization

The **ICS1577** version has a fixed internal power-on reset circuit that performs the following function:

> Sets the multiplexer to pass the VCO frequency (Fxtal x 28).

Power Supplies and Decoupling

The **ICS1577** has two VSS pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the CPU board as close to the package as is possible.

The **ICS1577** has a VDDO pin which is the supply of +5 volt power to all output drivers. This pin should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, capacitors should have low series inductance and be mounted close to the **ICS1577**.

The VDD pin is the power supply pin for the PLL synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects. See Figure 3 for typical external circuitry.

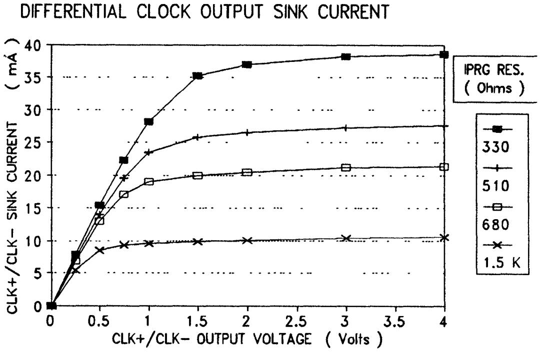


Figure 2

ICS1577 Typical Interface

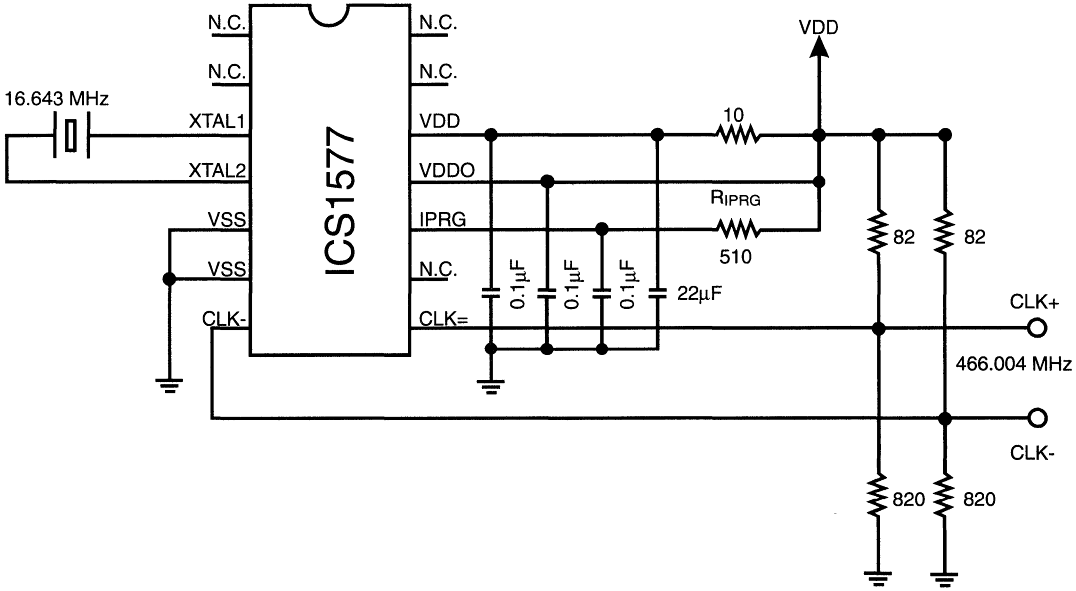


Figure 3

fXTAL	fOUT
11.786 MHz	330.000 MHz
14.318 MHz	400.904 MHz
16.643 MHz	466.004 MHz

Pin Description

PIN NUMBER	NAME	DESCRIPTION
3	XTAL1	Quartz crystal connection 1/external reference frequency input
4	XTAL2	Quartz crystal connection 2/No connect for EXT REF
5, 6	V_{SS}	Device Ground. Both pins must be connected.
7	CLK-	Clock Out (inverted)
8	CLK+	Clock Out
10	IPRG	Output stage current/voltage set.
11	V_{DDO}	Output stage power (+5.0V)
12	V_{DD}	PLL system power (+5V. See application diagram.)
1, 2, 9, 13, 14	N.C.	No connection.

Absolute Maximum Ratings

VDD, VDDO (measured to V_{SS})	7.0 V
Digital Inputs	V_{SS}-0.5 to V_{DD} + 0.5 V
Digital Outputs	V_{SS}-0.5 to V_{DDO} + +0.5 V
Ambient Operating Temperature	-55 to 125°C
Storage Temperature	-65 to 150°C
Junction Temperature	175°C
Soldering Temperature	260°C

Recommended Operating Conditions

VDD, VDDO (measured to V_{SS})	4.75 to 5.25 V
Operating Temperature (Ambient)	0 to 50°C

The **ICS1577** can be operated at 3.3V with reduced operating performance. Contact factory for information.

DC Characteristics

XTAL1 Input (External reference)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{xh}		3.75	V_{DD}+0.5	V
Input Low Voltage	V_{xl}		V_{SS}-0.5	1.25	

CLK+, CLK- Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Differential Output Voltage			0.6	-	V

AC Characteristics @ 25°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
F_{vco}	VCO Frequency	140		500	MHz
F_{xtal}	Crystal Frequency	5		18	MHz
Cpar	Crystal Oscillator Loading Capacitance		20		pF
T_{xhi}	XTAL1 High Time (when driven externally)	8			ns
T_{xlo}	XTAL1 Low Time (when driven externally)	8			ns
T_{high}	Differential Clock Output Duty Cycle (see Note 1)	40		60	%
J_{clk}	Differential Clock Output Cumulative Jitter (see Note 2)		<.06	.075	VCO cycle
	Differential Clock Output Cumulative Jitter @ 466 MHz			375	ps peak to peak
J_p	Differential Clock Output Cycle-to-Cycle Jitter			100	ps peak to peak
T_{lock}	PLL Acquire Time (to within 1%)		500		µs
I_{dd}	VDD Supply Current (excluding external CLK+/– output termination), 466 MHz.			50	mA

Note 1: Using load circuit of Figure 3. Duty cycle measured at zero crossings of difference voltage between CLK+ and CLK-.

Note 2: Cumulative jitter is defined as the maximum error (in the domain) if any CLK edge, at any point in time, compared with the equivalent edge generated by an ideal frequency source.
ICS laboratory testing indicates that the typical value shown above can be treated as a maximum jitter specification in virtually all applications. Jitter performance can depend somewhat on circuit board layout, decoupling, and register programming.

Ordering Information

ICS1577N

Example:

ICS XXXX M

Package Type
N=DIP (Plastic)

Device Type (consists of 3 or 4 digit numbers)

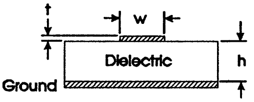
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Output Circuit Considerations for the ICS1577

Output Circuitry

The dot clock signals CLK and CLK- are typically the highest frequency signals present in the workstation. To minimize problems with EMI, crosstalk, and capacitive loading extra care should be taken in laying out this area of the PC board. The **ICS1577** is packaged in a 0.2"-wide 16-pin SOIC package. This permits the clock generator, crystal, and related components to be laid out in an area the size of a postage stamp. The **ICS1577** should be placed as close as possible to the CPU. The CLK and CLK- pins are running at VHF frequencies; one should minimize the length of PCB trace connecting them to the termination so that they don't become radiators of RF energy.

At the frequencies that the **ICS1577** is capable of, PC board traces may be long enough to be a significant portion of a wavelength of that frequency. PC traces for CLK and CLK- should be treated as transmission lines, not just interconnecting wires. These lines can take two forms: microstrip and stripline. A microstrip line is shown below:



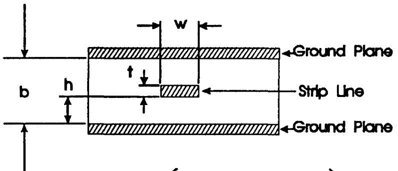
$$Z_o = \frac{87}{\sqrt{e_r + 1.41}}\ \ln\left(\frac{5.98h}{0.8w+t}\right)$$

Dimensions in Inches

Microstrip Line

Essentially, the microstrip is a copper trace on a PCB over a ground plane. Typically, the dielectric is G10 glass epoxy. It differs from a standard PCB trace in that its width is calculated to have a characteristic impedance. To calculate the characteristic impedance of a microstrip line one must know the width and thickness of the trace, and the thickness and dielectric constant of the dielectric. For G10 glass epoxy, the dielectric constant (e_r) is about 5. Propagation delay is strictly a function of dielectric constant. For G10 propagation, delay is calculated to be 1.77 ns/ft.

Stripline is the other form a PCB transmission line can take. A buried trace between ground planes (or between a power plane and a ground plane) is common in multi-layer boards. Attempting to create a workstation design without the use of multi-layer boards would be adventurous to say the least, the issue would more likely be whether to place the interconnect on the surface or between layers. The between layer approach would work better from an EMI standpoint, but would be more difficult to lay out. A stripline is shown below:



$$Z_o = \frac{60}{\sqrt{e_r}}\ \ln\left(\frac{4b}{0.067\ \pi\ w\left(0.8+\frac{t}{w}\right)}\right)$$

Dimensions in Inches

Stripline

Using 1oz. copper (0.0015" thick) and 0.040" thickness G10, a 0.010" trace will exhibit a characteristic impedance of 75Ω in a stripline configuration.

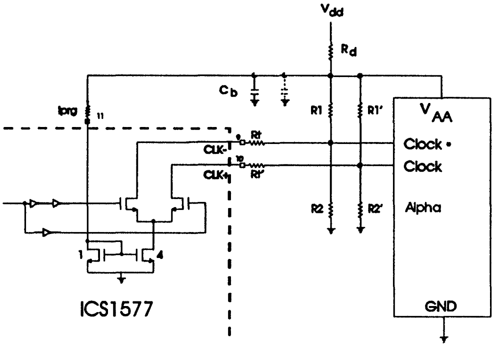
Output circuitry for the **ICS1577** is shown in the following diagram. It consists of a 4/1 current mirror, and two open drain output FETs along with inverting buffers to alternately enable each current-sinking driver. Both CLK and CLK- outputs are connected to the respective CLOCK and CLOCK* inputs of the termination with transmission lines and terminated in their equivalent impedances by the Thevenin equivalent impedances of R1 and R2 or R1' and R2'.

The **ICS1577** is incapable of sourcing current, so V_{ih} must be set by the ratios of these resistors for each of these lines. R1 and R2 are electrically in parallel from an AC standpoint because V_{dd} is bypassed to ground through bypass-capacitor network C_b. If we picked a target impedance of 75Ω for our transmission line impedance, a value of 91Ω for R1 and R1' and a value of 430Ω for R2 and R2' would yield a Thevinin equivalent characteristic impedance of 75.1W and a V_{ih} value of V_{AA}-.873 Volts, a margin of 0.127 Volts. This may be adequate; however, at higher frequencies one must contend with the input capacitance of the termination. Values of 82Ω for R1 and R1' and 820Ω for R2 and R2' would give us a characteristic impedance of 74.5Ω and a V_{ih} value of V_{AA}-.45. With a .55 Volt margin on Vih, this voltage level might be safer.

To set a value for V_{il}, we must determine a value for I_{prg} that will cause the output FET's to sink an appropriate current. We desire V_{il} to be V_{AA}-1.6 or greater. VAA-2 would seem to be a safe value. Setting up a sink current of 25 milliamperes would guarantee this through our 82Ω pull-up resistors. As this is controlled by a 4/1 current mirror, 7 mA into I_{prg} should set this current properly. A 510Ω resistor from V_{dd} to I_{prg} should work fine.

Resistors Rt and Rt' are shown as series terminating resistors at the **ICS1577** end of the transmission lines. These are not required for operation, but may be useful for meeting EMI requirements. Their intent is to interact with the input capacitance of the termination and the distributed capacitance of the transmission line to soften up rise and fall times and consequently cut some of the high-order harmonic content that is more likely to radiate RF energy. In actual usage they would most likely be 10 to 20Ω resistors or possibly ferrite beads.

Cb is shown as multiple capacitors. Typically, a 22 μF tantalum should be used with separate .1 μF and 220pF capacitors placed as close to the pins as possible. This provides low series inductance capacitors right at the source of high frequency energy. R_d is used to isolate the circuitry from external sources of noise. Five to ten ohms should be adequate.



ICS1577 Output Circuitry

Great care must be used when evaluating high frequency circuits to achieve meaningful results. The 10 pF input capacitance and long ground lead of an ordinary scope probe will make any measurements made with it meaningless. A low capacitance FET probe with a ground connection directly connected to the shield at the tip will be required. A 1 GHz bandwidth scope will be barely adequate, try to find a faster unit.

Integrated
Circuit
Systems, Inc.

ICS2572

User-Programmable Dual High-Performance Clock Generator

Description

The **ICS2572** is a dual-PLL (phase-locked loop) clock generator with differential video outputs specifically designed for high-resolution, high-refresh rate, video applications. The video PLL generates any of 16 pre-programmed frequencies through selection of the address lines **FS0-FS3.** Similarly, the auxiliary PLL can generate any one of four pre-programmed frequencies via the **MS0** & **MS1** lines.

A unique feature of the **ICS2572** is the ability to redefine frequency selections after power-up. This permits complete set-up of the frequency table upon system initialization.

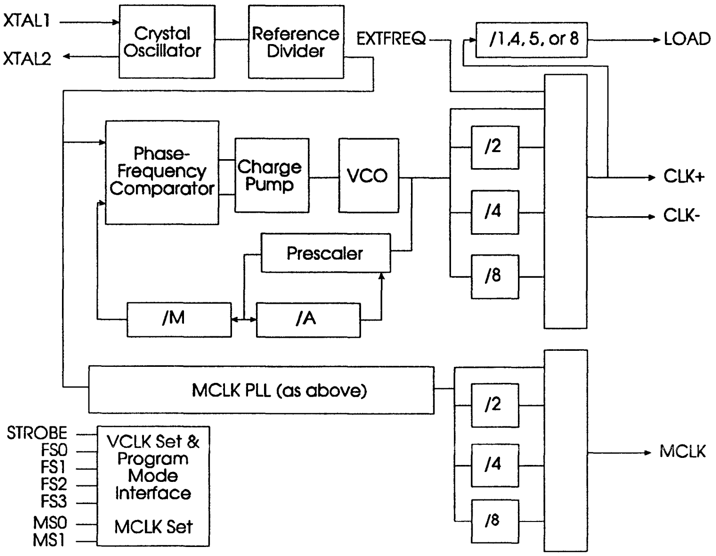
Features

- Advanced ICS monolithic phase-locked loop technology
- Supports high-resolution graphics - differential **CLK** output to 185 MHz
- Divided dotclock output (**LOAD**) available
- Simplified device programming
- Sixteen selectable **VCLK** frequencies (all user re-programmable)
- Four selectable **MCLK** frequencies (all user re-programmable)
- Windows NT compatible

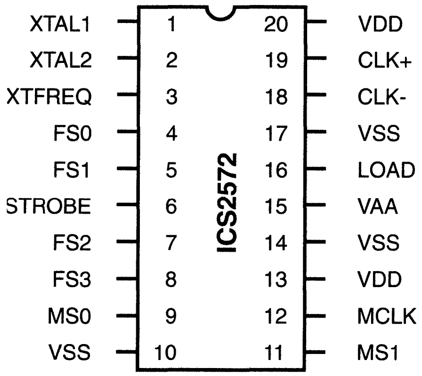
Applications

- High end PC/low end workstation graphics designs requiring differential output
- X Terminal graphics

Block Diagram



Pin Configuration



20-Pin DIP or SOIC
K-4, K-7

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	XTAL1	A	Quartz crystal connection 1/Reference Frequency Input.
2	XTAL2	A	Quartz crystal connection 2.
3	EXTFREQ	I	External Frequency Input
4	FS0	I	VCLK PLL Frequency Select LSB.
5	FS1	I	VCLK PLL Frequency Select Bit.
7	FS2	I	VCLK PLL Frequency Select Bit.
8	FS3	I	VCLK PLL Frequency Select MSB.
6	STROBE	I	Control for Latch of VCLK Select Bits (FS0-FS3).
9	MS0	I	MCLK PLL Frequency Select LSB.
11	MS1	I	MCLK PLL Frequency Select MSB.
19	CLK+	O	Pixel Clock Output (not inverted)
18	CLK-	O	Pixel Clock Output (inverted)
16	LOAD	O	Divided Dotclock (/4, 5, or 8)
12	MCLK	O	MCLK Frequency Output
17	RESERVED	-	Must Be Connected to VSS.
10, 14	VSS	P	Device Ground. All pins must be connected.
13, 20	VDD	P	Output Stage Vdd. All pins must be connected.
15	VAA	P	Synthesizer Vdd.

Digital Inputs

The **FS0-FS3** pins and the **STROBE** pin are used to select the desired operating frequency of the **VCLK** output from the 16 pre-programmed/user-programmed selections in the **ICS2572**. These pins are also used to load new frequency data into the registers.

Available configurations for the **STROBE** input include: positive-edge triggered, negative-edge triggered, high-level transparent, and low-level transparent (see Ordering Information).

VCLK Output Frequency Selection

To change the **VCLK** output frequency, simply write the appropriate data to the **ICS2572 FS** inputs. Do not perform any further writes to the device for 50 milliseconds (assumes a 14.318 MHz reference). The synthesizer will output the new frequency programmed into that location after a brief delay (see timeout specifications).

MCLK Output Frequency Selection

The **MS0-MS1** pins are used to directly select the desired operating frequency of the **MCLK** output from the four pre-programmed/user-programmed selections in the **ICS2572.** These inputs are not latched, nor are they involved with memory programming operations.

Programming Mode Selection

A programming sequence is defined as a period of at least 50 milliseconds of no data writes to the **ICS2572** (to clear the shift register) followed by a series of data writes (as shown here):

FS0	FS1	FS2	FS3
X	X	**START** bit (must be “0”)	0
X	X	”	1
X	X	**R/W*** control	0
X	X	”	1
X	X	**L0** (location LSB)	0
X	X	”	1
X	X	**L1**	0
X	X	”	1
X	X	**L2**	0
X	X	”	1
X	X	**L3**	0
X	X	”	1
X	X	**L4** (location MSB)	0
X	X	”	1
X	X	**N0** (feedback LSB)	0
X	X	”	1
X	X	**N1**	0
X	X	”	1
X	X	**N2**	0
X	X	”	1
X	X	**N3**	0
X	X	”	1
X	X	**N4**	0
X	X	”	1
X	X	**N5**	0
X	X	”	1
X	X	**N6**	0
X	X	”	1
X	X	**N7** (feedback MSB)	0
X	X	”	1
X	X	**EXTFREQ** bit (selected if “1”)	0
X	X	”	1
X	X	**D0** (post-divider LSB)	0
X	X	”	1
X	X	**D1** (post-divider MSB)	0
X	X	”	1
X	X	**STOP1** bit (must be “1”	0
X	X	”	1
X	X	**STOP2** bit (must be “1”)	0
X	X	”	1

Observe that the internal shift register is "clocked" by a transition of **FS3** data from "0" to "1." If an extended sequence of register loading is to be performed (such as a power-on initialization sequence), note that it is not necessary to implement the 50 millisecond delay between them. Simply repeat the sequence above as many times as desired. Writes to the **FS** port will not be treated as frequency select data until up to 50 milliseconds have transpired since the last write. Note that **FS0** and **FS1** inputs are "don't care."

Data Description

Location Bits (L0-L4)

The first five bits after the start bit control the frequency location to be re-programmed according to this table. The rightmost bit (the LSB) of the five shown in each selection of the table is the first one sent.

Table 1 - Location Bit Programming

L[4-0]	LOCATION
01100	VCLK Address 12
01101	VCLK Address 13
01110	VCLK Address 14
01111	VCLK Address 15
10010	MCLK Address 2
10011	MCLK Address 3

Feedback Set Bits (N0-N7)

These bits control the feedback divider setting for the location specified. The modulus of the feedback divider will be equal to the value of these bits + 257. The least significant bit (N0) is sent first.

Post-Divider Set Bits (D0-D1)

These bits control the post-divider setting for the location specified according to this table. The least significant bit (D0) is sent first.

Table 2 - Post-Divider Programming

D[1-0]	POST-DIVIDER
00	9
01	4
10	2
11	1

Read/Write* Control Bit

When set to a "0," the **ICS2572** shift register will transfer its contents to the selected memory register at the completion of the programming sequence outlined above.

When this bit is a "1," the selected memory location will be transferred to the shift register to permit a subsequent readback of data. No modification of device memory will be performed.

To readback any location of memory, perform a "dummy" write of data (complete with start and stop bits) to that location but set the **R/W*** control bit (make it "1"). At the end of the sequence (i.e., after the stop bits have been "clocked"), "clocking" of the **FS3** input 11 more times will output the data bits only in the same sequence as above on the FS0 pin.

EXTFREQ Input

The **EXTFREQ** input allows an externally generated frequency to be routed to the **VCLK** output pin under device programming control. If the EXTFREQ bit is set (logic "1") at the selected address location (*VCLK addresses only*), the frequency applied to the EXTFREQ input will be routed to the **VCLK** output.

Frequency Synthesizer Description

Refer to Figure 1 for a block diagram of the **ICS2572**.

The **ICS2572** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL. The phase-frequency detector shown in the block diagram drives the VCO to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F_{VCO}=F_{XTAL1}*\frac{N}{2}$$

where N is the effective modulus of the feedback divider chain and R is the modulus of the reference divider chain.

The feedback divider on the **ICS2572** may be set to any integer value from 257 to 512. This is done by the setting of the **N0-N7** bits. The standard reference divider on the **ICS2572** is fixed to a value of 43 (this may be set to a different value via ROM programming; contact factory). The **ICS2572** is equipped with a post-divider and multiplexer that allows the output frequency range to be scaled down from that of the VCO by a factor of 2, 4, or 8.

Therefore, the *VCO* frequency range will be from 5.976 to 11.906 (257/43 to 512/43) of the reference frequency. The *output* frequency range will be from 0.747 to 11.906 times the reference frequency. Worst case accuracy for any desired frequency within that range will be 0.2%.

If a 14.31818 MHz reference is used, the output frequency range would be from 10.697 MHz to 170.486 MHz.

Programming Example

Suppose that we want differential **CLK** output to be 45.723 MHz. We will assume the reference frequency to be 14.31818 MHz.

The VCO frequency range will be 85.565 MHz to 170.486 MHz (5.976 * 14.31818 to 11.906 * 14.31818). We will need to set the post-divider to two to get an output of 45.723 MHz. The VCO will then need to be programmed to two times 45.723 MHz, or 91.446 MHz. To calculate the required feedback divider modulus we divide the VCO frequency by the reference frequency and multiply by the reference divider:

$$\frac{91.446}{14.31818}*43=274.62$$

which we round off to 275. The exact output frequency will be:

$$\frac{275}{43}*14.31818*\frac{1}{2}=45.784 \text{ MHz}$$

The value of the **N** programming bits may be calculated by subtracting 257 from the desired feedback divider modulus. Thus, the **N** value will be set to 18 (275-257) or 00010010_2. The **D** bit programming is 10_2 (from Table 2).

LOAD Frequency Selection

The LOAD (or divided dotclock) output frequency will be the CLK+/CLK- frequency divided by 1, 4, 5, or 8. The choice of modulus is a factory option, and is specified along with the ROM frequencies in the VCLK and MCLK tables by way of the two-digit suffix of the part number.

Reference Oscillator & Crystal Selection

The **ICS2572** has on-board circuitry to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in parallel-resonant (also called anti-resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Crystals characterized for their series-resonant frequency may also be used with the **ICS2572**. Be aware that the oscillation frequency in circuit will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS2572** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

External Reference Sources

An external frequency source may be used as the reference for the VCLK and MCLK PLLs. To implement this, simply connect the reference frequency source to the XTAL1 pin of the **ICS2572**. For best results, insure that the clock edges are as clean and fast as possible and that the input voltage thresholds are not violated.

Power Supply

The **ICS2572** has two **VSS** pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS2572** has a **VDD** pin which is the supply of +5 volt power to all output stages. This pin should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, use low-capacitors should have low series inductance and be mounted close to the **ICS2572**.

The **VAA** pin is the power supply for the synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects.

Absolute Maximum Ratings

Supply voltage	-.5V to +7V
Logic inputs	-.5V to V_{DD} +.5V
Ambient operating temp	0 to 70°C
Storage temperature	-85 to + 150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TTL-Compatible Inputs						
(FS0-3, MS0-1, STROBE):						
Input High Voltage	V_{ih}		2.0		VDD+0.5	V
Input Low Voltage	V_{il}		VSS-0.5		0.8	V
Input High Current	I_{ih}				10	uA
Input Low Current	I_{il}				200	uA
Input Capacitance	C_{in}				8	pf
XTAL1:						
Input High Voltage	Vxh		VDD*0.75		VDD+0.5	V
Input Low Voltage	Vxl		VSS-0.5		VDD*0.25	V
CLK+/CLK- Output Sink Current	Isink					mA
High Voltage (Other Outputs)	Voh		4			V
@Ioh=0.4mA						
Low Voltage (Other Outputs)	Vol				0.4	V
@Iol=8.0mA						

AC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Phase-Locked Loop:						
VCLK, MCLK VCO Frequency	Fvco		100		235	MHz
PLL Acquire Time	Tlock			500		uSec
Crystal Oscillator						
Crystal Frequency Range	Fxtal		5		25	MHz
Parallel Loading Capacitance				20		pf
XTAL1 Minimum High Time	Txhi		8			nSec
XTAL1 Minimum Low Time	Txlo		8			nSec
Power Supplies:						
VDD Supply Current	idd				35	mA
VAA Supply Current	Iaa				10	mA
Digital Outputs:						
CLK+/CLK- Recommended Termination			50		2	ohms
Other Outputs Rise Time @ Cload=20pf	Tf				2	nSec
Other Outputs Fall Time @ Cload=20pf	Tf					nSec

PATTERN	ICS2572-01			
Reference Divider	43			
VCLK ADDR	FbkDiv/PostDiv - F_{VCLK}(MHz)			
0	300/1- 99.89			
1	378/1 - 125.87			
2	277/1 - 92.24			
3	432/4 - 35.96			
4	302/2 - 50.28			
5	340/2 - 56.61			
6	EXTFREQ-			
7	270/2 - 44.95			
8	405/1 - 134.86			
9	384/4 - 31.97			
A	330/1 - 109.88			
B	481/2 - 80.08			
C	479/4 - 39.87			
D	270/2 - 44.95			
E	450/2 - 74.92			
F	390/2 - 64.93			
MCLK ADDR	FbkDiv/PostDiv - F_{MCLK}			
0	481/4 - 40.04			
1	270/2 - 44.95			
2	396/4 - 32.97			
3	300/2 - 49.95			

E

Ordering Information

ICS2572N-SXX or ICS2572M-SXX (0.300" DIP or SOIC Package)

Example:

ICS XXXX N-SXX

S=Strobe Option/XX=Default Frequencies

Package Type

N=DIP (Plastic)
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV=Standard Device; GSP=Genlock Device

Where:

"s" denotes strobe option:	A - positive level transparent (i.e., 2494 interface compatible)
"xx" denotes default frequencies:	B - negative level transparent
	C - positive edge triggered
	D - negative edge triggered

ICS
Communications
Products

This issue of the ICS data book introduces an exciting new family of advanced physical layer clock recovery and transceiver High Speed Communications products designed for ATM, SONET, FDDI, Fast Ethernet, and similar local and wide area network applications.

These new products span both domestic and international transmission frequencies from 25Mb to 155Mb data rates, offer the advantages of low power CMOS technology, and bring many innovative features to the designer not found in competitive solutions. Examples of various product features of this family (ICS1884 through ICS1891) include:

- Integrated on-chip, VCXO, Full Bellcore jitter compliance
- Fully independent, duplex transmit and receive operation
- Selectable clock generation from either recovered or independent source
- Integrated crystal oscillator multiple data rate capability

These innovative features offer the designer a new level of system integration, performance, and cost effectiveness. ICS has made a significant commitment to this growing marketplace, and will continue to introduce additional highly integrated solutions in the months ahead. Look for fully integrated physical layer solutions for ATM UTP, Fast Ethernet, FDDI, and other applications. Please contact one of our sales offices for advance information on these exciting, system level integration products, all using advanced CMOS technology.

ICS Communications Product Selection Guide

Product Applications	ICS Device Type	Description	Package Types	Page
Caller I.D.	ICS1660	Caller I.D. Receiver with Ring Detect.	18-Pin DIP 20-Pin SOIC	F-3
LAN/WAN Communications Systems	ICS1884	SONET/SDH Clock Recovery On-Chip VCXO, 51/155Mb, Bellcore compliance.	28-Pin SOIC	F-15
	ICS1885	LAN/WAN Transceiver 26, 44, 51, 155Mb.	28-Pin SOIC	F-27
	ICS1886	LAN/WAN Transceiver 32, 34, 97, 139Mb.	28-Pin SOIC	F-33
	ICS1887	FDDI/Fast ENET Transceiver 100Mb, Full duplex.	28-Pin SOIC	F-39
	ICS1888	High-Performance Twisted Pair Communication PHYceiver.	*to be determined*	F-45
	ICS1889	100Base-FX Integrated PHYceiver.	52-Pin MQFP	F-47
	ICS1890	10Base-T/100Base-TX Integrated PHYceiver.	52-Pin MQFP	F-49
	ICS1891	100Base-TX Integrated PHYceiver for Repeaters.	52-Pin MQFP	F-51

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. ICS reserves the right to change or discontinue these products without notice.

Integrated
Circuit
Systems, Inc.

Incoming Call Line Identification (ICLID) Receiver with Ring Detection

Description

The **ICS1660** "ICLID" circuit is a monolithic CMOS VLSI device that decodes and detects the Frequency Shift Keying (FSK) signals used in caller identification telephone service. The **ICS1660**, when used in conjunction with some external components, amplifies, filters and demodulates the FSK data transmitted from the central office to the telephone subscriber.

The **ICS1660** detects the first power ring signal and demodulates the 1200 baud FSK data transmitted during the silent interval between the first and second power ring. The FSK data is transmitted from the central office switch to the subscriber line as part of the CLASS service of Calling Number Delivery (CND). This data is then demodulated, amplified and filtered by the **ICS1660** and digitally transmitted to the host controller/processor.

The **ICS1660** is designed to be powered by any off-the-shelf 9.0 volt battery. The on-chip 5.0 voltage regulator powers the host microprocessor and any external circuitry supported by the **ICS1660**. This portion of the circuit can be overridden by connecting the V_{IN} pin (18) to the V_{DD} pin (1) for a common power supply. A low battery detection circuit is also provided on-chip and signals the microprocessor on the FSK/BAT pin (17) when the PWR pin (16) input is pulled low.

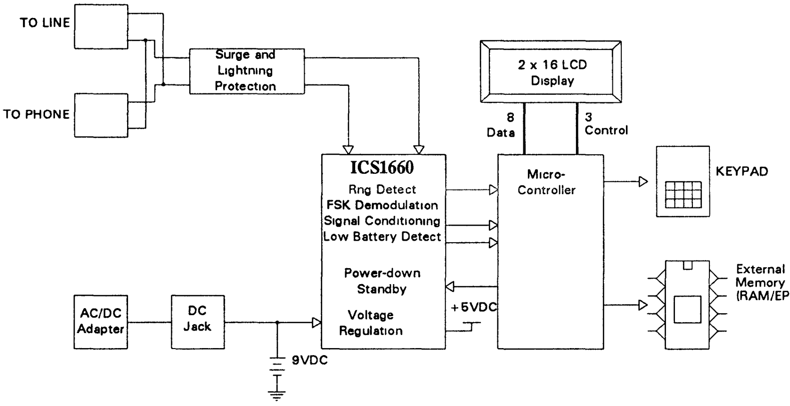
Features

- Ring Detection
- Low Battery Detection
- Internal 5V Regulator - can externally source 25mA
- FSK Demodulation
- Power-down in Standby Mode
- Direct Interface to Host Microprocessor or Microcomputer

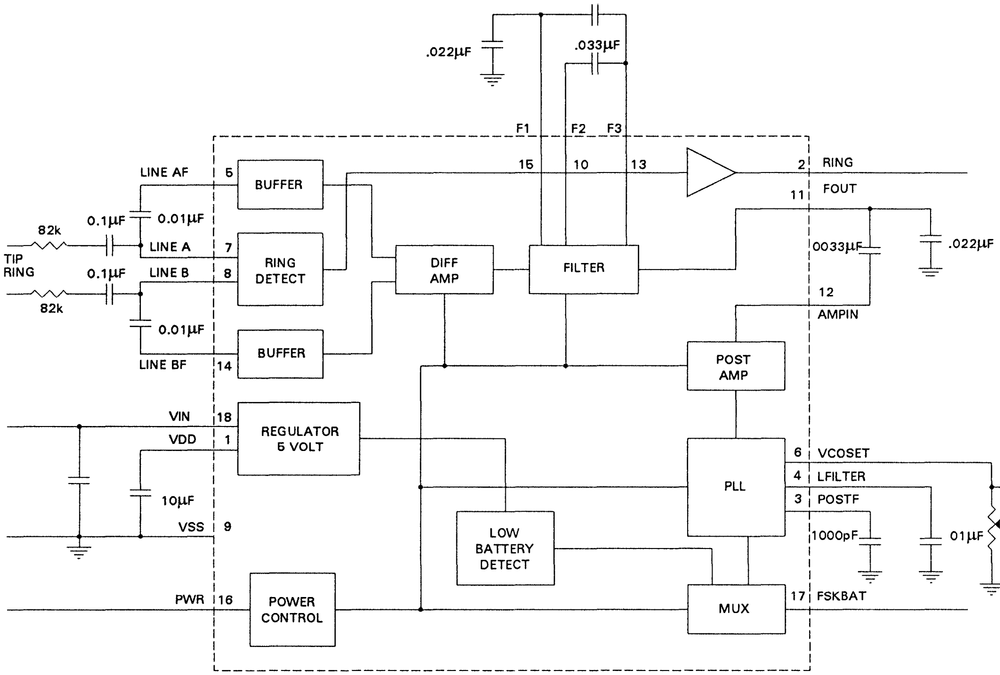
Applications

- Telephones
- Facsimile Machines
- Modems
- Telephone Interface Equipment
- Stand-alone ICLID products

ICLID Block Diagram



Block Diagram



Function Description

Power Supply

The **ICS1660** is designed to be powered by a standard 9.0 volt battery. The chip contains a voltage regulator that powers external circuitry and provides the supply voltage for all digital I/O on the circuit. This allows easy interface between the **ICS1660** and other standard logic working at 5.0V. This regulator has short circuit protection and requires an external filter/compensation capacitor with a minimum value of 10uf.

In the event that an external regulated 5.0V supply is available, the V_{IN} and V_{DD} pins can be shorted to permit the entire system to work from a common supply.

A low battery detection circuit is provided. This circuit is designed for a typical trip point of 6.0V with hysteresis of about 200mV above the trip point. This signal is low active and is multiplexed to the FSKBAT output pin when the PWR input is low.

In an effort to keep power dissipation to a minimum and extend battery life, most of the analog circuits are turned off when the circuit is at rest waiting for a ring detect, (PWR pin low). During this time only the regulator, low battery detect, reference generator, and ring detect circuits are active. When the PWR pin is high, all circuits are active.

Ring Detect

As shown in the attached block diagram, the LINEA and LINEB inputs should be connected to the telephone line through external 82kΩ resistors and 0.1uf capacitors. This provides DC isolation and sets up a voltage divider with internal resistors that will detect 35.0V RMS typically. This voltage is applied across the LINEA and LINEB inputs. The design value of the internal resistors is 8.1KΩ ± 20% with relative accuracy of 2%. The RING output is high active.

Differential Front End

As shown in the attached block diagram, the LINEA and LINEB inputs go into a differential amplifier which in turn drives a filter. All resistors are internal to the chip while capacitors are connected as shown in the block diagram. After filtering, the signal is AC coupled into a high gain amplifier that converts the signal to digital. This digital signal in turn acts as the reference frequency for the phase comparator section of the phase locked loop.

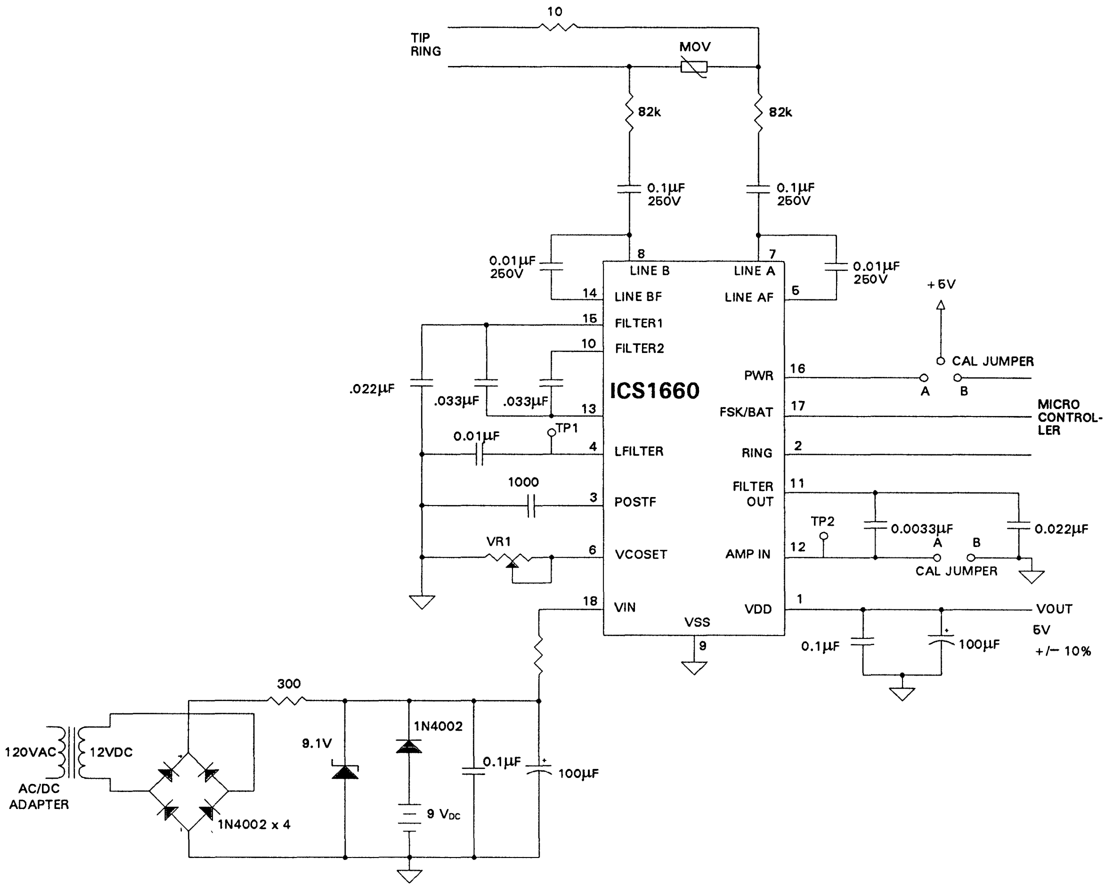
FSK Demodulation

After the signal from the telephone line has been filtered, amplified and converted to digital, it acts as an input to a phase locked loop. This PLL does FSK demodulation. The summing amplifier shown in the block diagram provides a signal to the VCO that should be about 0.5V for MARK frequency (1200 HZ), and 2.0V for SPACE frequency (2200 HZ).

As shown in the block diagram, the LFILTER (loop filter) output has a post filter attached to it. This POSTF signal is sent to a comparator. The other side of the comparator is set to approximately 2.5V. This comparator has a small amount (200 mV) of hysteresis and its output is the demodulated FSK data. The FSK output is high for MARK frequency and low for SPACE frequency. FSK data is multiplexed out of the FSKBAT pin when the PWR input is high.

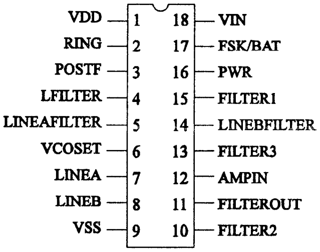
The VCO frequency is set with one external resistor with a value in the range of 300K for a center frequency of 1700 HZ. The lock range will be 660 HZ to 2630 HZ typical. The center frequency reproducibility will be ±15%. The center frequency can be adjusted in the system by connecting AMPIN to VSS, PWR to VDD, and adjusting the external resistor for 1700 HZ. This frequency can be observed at the LFILTER output or the FSK/BAT output.

Typical Application

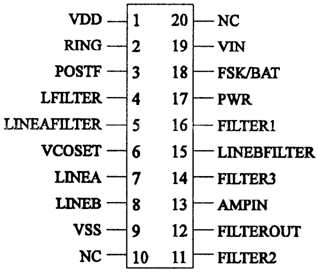


Pin Descriptions

PIN NUMBER		NAME	DESCRIPTION
DIP	SO		
1	1	VDD	Supply voltage pin to external circuits. Output of 5.0 volt regulator.
2	2	RING	Ring detect output signal to the host microprocessor.
3	3	POSTF	Post loop filter signal used by demodulator.
4	4	LFILTER	Loop filter for PLL.
5	5	LINEAFILTER	Filter input from line "A."
6	6	VCOSET	Center frequency adjustment pin.
7	7	LINEA	"Tip" input from telephone line.
8	8	LINEB	"Ring" input from telephone line.
9	9	VSS	Ground.
10	11	FILTER2	Active filter pin.
11	12	FILTEROUT	Active filter pin.
12	13	AMPIN	Input from active filter.
13	14	FILTER3	Active filter pin.
14	15	LINEBFILTER	Filter input from line "B."
15	16	FILTER1	Active filter pin.
16	17	PWR	Logic input signal to switch from low current standby mode.
17	18	FSK/BAT	Multiplexed output signal controlled by PWR pin. In standby mode, this is a low battery (active low) signal. During FSK demodulation, this is the data line to the µP (mark = high).
18	19	VIN	Input power supply pin.
10	20	NC on SOIC	



18 PIN
DIP
K-4



20 PIN
SOIC
K-7

Input/Output Specifications

Digital

RING and FSKBAT outputs are standard CMOS outputs with voltage swings between V_{SS} and V_{DD}.

PWR is a logic input. A level converter circuit is on chip to allow the logic signal that swing between V_{SS} and V_{DD} to be internally converted to signals that swing between V_{SS} and V_{IN}. It should be noted that to minimize power consumption caused by through current in logic gates, the PWR input should always swing to within 100 mV of V_{SS} or V_{DD}. The PWR input signal is low when the **ICS1660** is in lower power mode waiting for an incoming call.

The LFILTER output is a standard CMOS output powered from VDD. This output has an internal resistor with a typical value of 30kΩ. This is used in conjunction with the external capacitor shown in the block diagram to form the loop filter for the PLL.

Analog

The value of the ring detect is as previously discussed 35.0V RMS typical. The actual value is set by the choice of the external resistors that are connected to the LINEA and LINEB inputs. The matching of these resistors to the internal 8.1kΩ resistors is also a factor. The signal level at the chip that will cause a ring is the bandgap voltage, (1.25V) or below.

The chip is designed for an input signal level of -12.5dbm to -28.5dbm into 900 ohms. This translates to a signal that is between 100 mV and 636 mV peak to peak.

The filter section should be connected as shown in the block diagram. Using the external capacitors as shown, and assuming nominal values on the internal resistors, the corner frequencies are 900 HZ and 3860 HZ.

An external resistor with a value of approximately 330kΩ is connected between the LFILTER and POSTF pads. This resistor along with the external capacitor shown in the block diagram form the post filter. This post filter is used in conjunction with the comparator to do the FSK demodulation.

Absolute Maximum Ratings*

(Voltages referenced to V_{SS})

Supply Voltage . . . . V_{IN} . . . . -0.5V to +10V
Voltage at any Input . . . . -0.5V to V_{DD} + 0.5V
Operation Temperature Range . . . . -55°C to +125°C
Storage Temperature Range . . . . -50°C to 150°C

* Absolute maximum ratings are those values beyond which the safety of this device cannot be guaranteed. These values are NOT RECOMMENDED operating conditions.

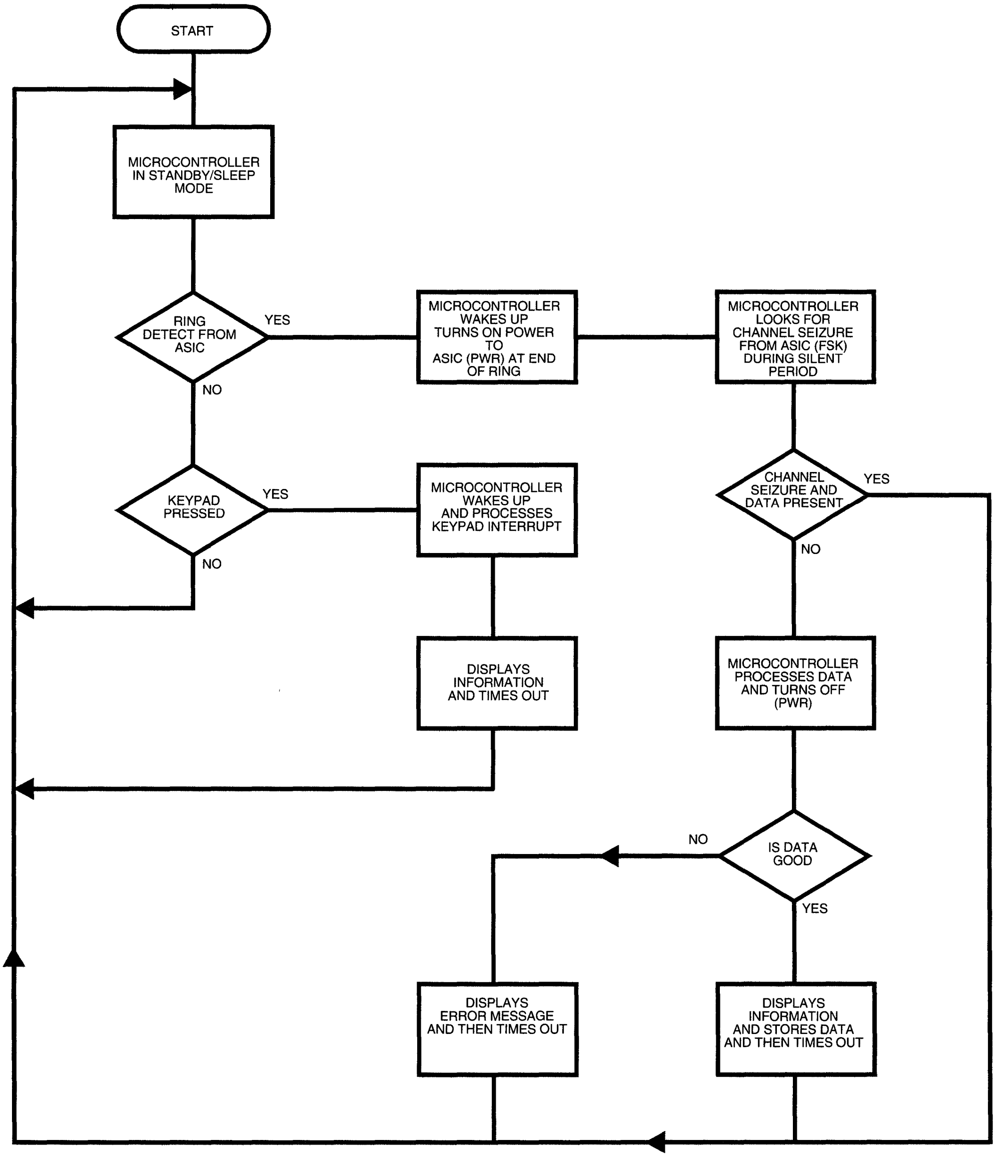
DC Characteristics

V_{IN} = 4.5V - 10.0V; T_A = 0 °C - 70 °C, Recommended Operating Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Standby Current	I_{IN}	PWR LOW, V_{IN} =9.0V, I_{DD}=2µA	-	20	30	uA
Active Current	I_{IN}	PWR HIGH, V_{IN}=9.0V VCOSET=300k	-	-	10	mA
Regulator Output Voltage	V_{DD}		4.5	5.0	5.5	Volts
Regulator Output Current	I_{DD}	Output Current	2.0		25.0	mA
Regulator Dropout	V_{IN}			0.5	1.0	Volts
Low Battery Detect				6.0		Volts
Low Battery Detect Hysteresis		Low Battery Detect - Hysteresis		200		mV
OUTPUT CURRENT SINK/SOURCE						
Ring Source Current	I_{OUT}	$VOUT_H = V_{DD} - 0.5V$	-500	-	-	uA
FSKBAT and Ring Sink Current	I_{OUT}	$VOUT_L = V_{SS} + 0.4V$	-	-	500	uA

ICLID Process Flowchart

(for Microprocessor and ASIC (ICS1660) Interface)



Ordering Information

ICS1660N or ICS1660M

Example:

ICS XXXX M

Package Type
N=DIP (Plastic)
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device, GSP=Genlock Device

ICS1660 ICLID Demonstration Board

Overview

The **DB1660** ICLID demonstration board is intended to be used to demonstrate the function of the **ICS1660** Incoming Call Line Identification Receiver IC. It provides a full-function incoming call display unit to verify the proper function of the **ICS1660** ICLID device.

NOTE: The only device that Integrated Circuit Systems Inc. is able to supply is the ICS1660. The other semiconductor devices and the display used on this board are proprietary designs and are not available from ICS.

Operation

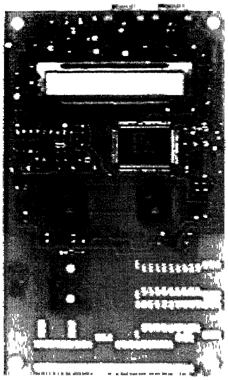
To use the **ICS1660** ICLID demo board, install a 9 volt alkaline battery in the battery clip on the board, and attach the battery connector. Facing the connector end of the board with the board "battery side up," the RJ11 connector on the right should be connected to a standard modular phone jack. The connector at the center of the board may be connected to the telephone instrument removed from the modular connector. Turn the board over so that the display is facing up and the two push buttons are toward you. Assuming that caller ID is available in your area, when your telephone begins ringing, the display will show the telephone number of your caller. After 20 seconds the display will return to its normal (blank) mode and the number will be stored in memory as the most recent call. When someone calls you from an area where the telephone company is not offering caller ID service or an area that is not yet providing caller ID information via the long distance network, the display will say "OUT-OF-AREA." In some areas, the calling party may be able to block their number from appearing on your call display. In this case, the display will say "PRIVATE." If the **DB1660** receives garbled data, a "?" will appear in every digit location that has unrecognized numbers. If all digits are garbled, the display will read "ERROR" but will not be stored in memory. In some areas, the local phone company will send a long-distance indicator which will show as an "L" on the display either with or without the incoming number.

Pushbutton Functions

Two pushbuttons exist on the **DB1660** board. The button to the left when facing the board, display up and buttons toward you is the **TIME** button. The button to your right is the **REVIEW** button. When the **REVIEW** button is pressed the phone number of the most recent call will be displayed. Each additional time the **REVIEW** button is pressed (within 20 seconds) the next most recent call is displayed. When the last call stored in memory has been reviewed, the next press of the **REVIEW** button will display "END."

Features

- Fully functional system permits verification of results obtained in a product application.
- Displays ICLID function without extensive design effort.



If **REVIEW** is pressed again within 20 seconds, it will bring you back to the start of the memory list and the most recent call will be displayed. If more than 20 seconds have elapsed before the **REVIEW** button is pressed, the display will blank and the next time **REVIEW** is pressed the most recent call will be displayed.

The time and date of an incoming call can be viewed by first pressing the **REVIEW** button until the selected number is displayed, and then pressing the **TIME** button. If the **TIME** button is pressed again within 20 seconds, the telephone number will again be displayed. This allows the **TIME** button to be used as a toggle between the telephone number and the date/time of the particular call.

NOTE: The **REVIEW** and **TIME** buttons are not operative during the interval when a new incoming phone number is being received.

When the ten call memory of the **DB1660** is full, the oldest call will automatically be erased to make room for the next call that comes in. To manually remove all calls, press the **TIME** button while the **REVIEW** button is pressed. This will also cause all the segments of the LCD display to be visible for as long as both of these buttons are pressed.

F

Integrated Circuit Systems, Inc.

ICS1884

Advance Information

SONET/ATM Teleclock™ Recovery/Generator Unit

General Description

The **ICS1884** Teleclock is designed to provide high performance clock recovery and generation for either 51.84 Mbit/s OC/STS-1 or 155.52 Mbit/s OC/STS-3/STM-1 SONET/SDH and ATM applications. ***The ICS1884 meets Bellcore TR-NWT-000253 requirements for jitter tolerance and jitter transfer and is ideal for loop timing applications.***

In the clock recovery mode, the **ICS1884** receives the 51.84 Mbit/s or 155.52 Mbit/s, NRZ or NRZI data stream and extracts the bit clock from this data. The chip uses differential PECL to output the regenerated data along with two bit clocks. A 6.48 MHz or 19.44 MHz reference byte clock is also available on a TTL output. System clock generation (loop timing) can be achieved simultaneously by utilizing the second pair of clock outputs. Using this method, the incoming data clock frequency is utilized as the transmit clock.

The **ICS1884** can also be used as a high performance 51.84 MHz or 155.52 MHz system clock generator by utilizing the VCXO free run mode.

The **ICS1884** utilizes advanced CMOS phase-locked loop technology which combines high performance and low power at a greatly reduced cost.

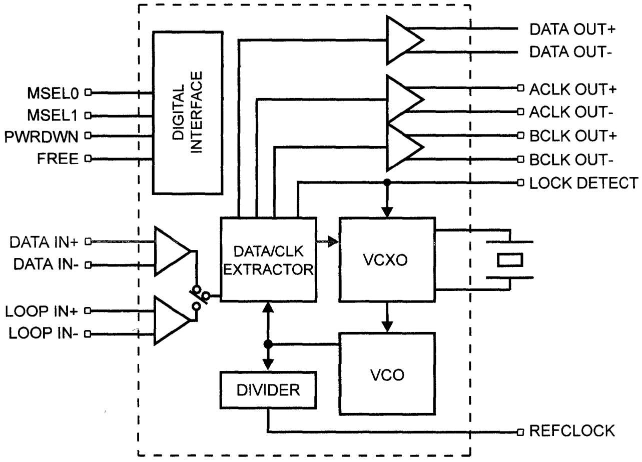
Features

- Internal VCXO
- Supports clock generation for either 51.84 Mbit/s OC/STS-1 or 155.52Mbit/s OC/STS-3/STM-1 SONET/SDH and ATM applications
- Provides continuous clock output if loss of input data stream
- Bellcore jitter compliance (tolerance and transfer)
- Supports clock recovery for 51.84 Mbit/s or 155.52 Mbit/s NRZ/NRZI data
- Complies with ANSI, Bellcore, and CCITT specifications
- Lowest power CMOS technology: Pd=250mW typical at 155 MHz
- Lock detect output monitors transition density and run length
- Available in space-saving 28-pin SOIC

Applications

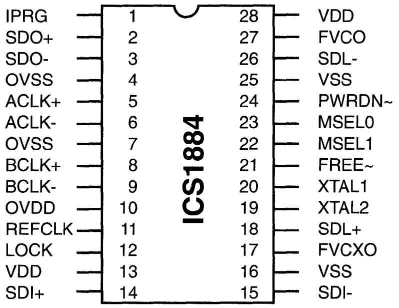
- SONET and ATM applications which require loop timing operation
- Wide area network (WAN) Bellcore compliant applications such as SONET STS-3 and SDH STM-1
- 51.84 Mbit/s or 155.52 Mbit/s ATM UNI
- SONET Add/Drop Multiplexers, Terminal Multiplexers, and Regenerators
- Line timing, loop timing and through-timing applications
- Consult ICS for other bit rate application (e.g., 25.6Mb, 100Mb, etc.)

Block Diagram



Teleclock is a trademark of Integrated Circuit Systems, Inc

Pin Configuration



28-Pin 300 MIL
K-7

Table 1 - Device Clock Selection

MODE	MSEL1	MSEL0	INPUT	REFCLK OUT	OUTPUT f
OC/STS-3	VDD	VDD	Data	19.44M	155.52M
OC/STS-1	VDD	VSS	Data	6.48M	51.84M
OC/STS-3	VSS	VDD	Loop	19.44M	155.52M
OC/STS-1	VSS	VSS	Loop	6.48M	51.84M

Note: Clock generation mode is obtained by setting pin 21 (FREEn) low.

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	IPRG	PECL output stage current set
2	SDO+	Positive re-timed serial data out
3	SDO-	Negative re-timed serial data out
4	OVSS	Output negative supply voltage
5	ACLK+	Positive recovered bit clock output A
6	ACLK-	Negative recovered bit clock output A
7	OVSS	Output negative supply voltage
8	BCLK+	Positive recovered bit clock output B
9	BCLK-	Negative recovered bit clock output B
10	OVDD	Output positive supply voltage
11	REFCLK	Reference clock output
12	LOCK	Lock detect output
13	VDD	Positive supply voltage
14	SDI+	Positive serial data input
15	SDI-	Negative serial data input
16	VSS	Negative supply voltage
17	FVCXO	VCXO external loop filter
18	SDL+	Positive serial loop data input
19	XTAL2	Negative reference clock/crystal input
20	XTAL1	Positive reference clock/crystal input
21	FREEn	VCXO free-run input (active low)
22	MSEL1	Mode select 1 input
23	MSEL0	Mode select 0 input
24	PWRDNn	Power down input (active low)
25	VSS	Negative supply voltage
26	SDL-	Negative serial loop data input
27	FVCO	VCO external loop filter
28	VDD	Positive supply voltage

Absolute Maximum Ratings

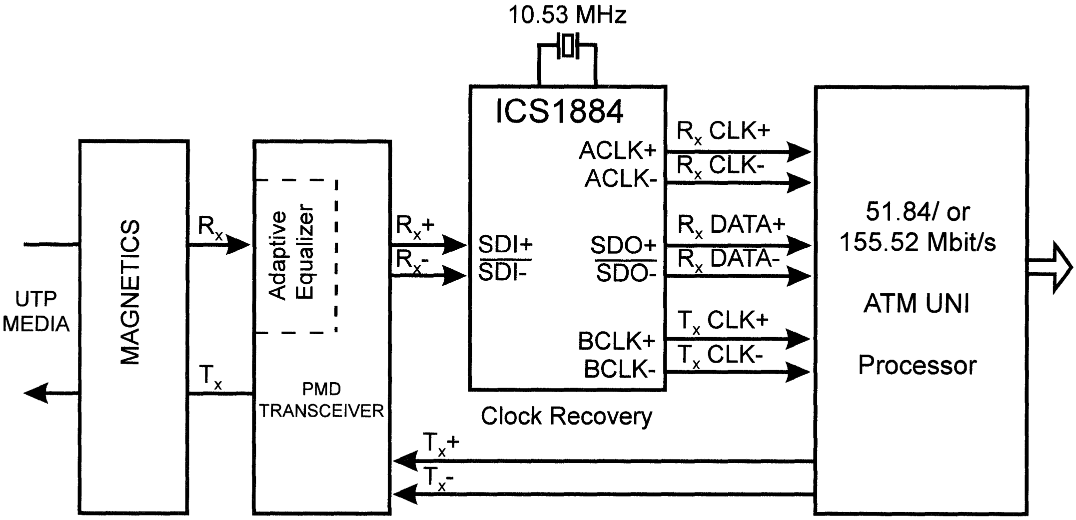
V_{DD} (measured to V_{SS}) 7.0V
Ambient Operating Temperature . . . . -55 to 125 °C
Storage Temperature. . . . . -65 to 150°C
Junction Temperature . . . . 175°C
Soldering Temperature . . . . 260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

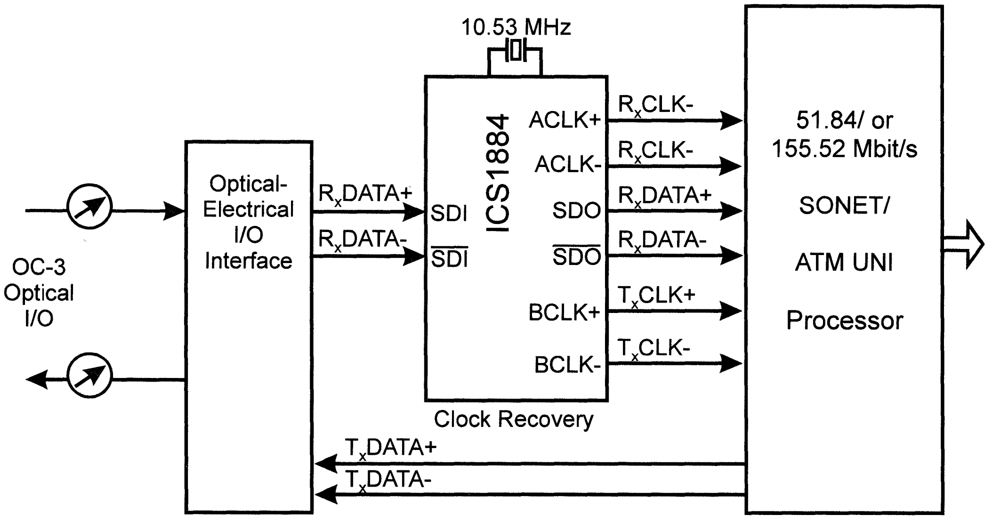
Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Ambient Operating Temp.	T_A		0	+70	°C
Using a Negative Supply	V_{SS} V_{DD}		-4.95 0.0	-5.45 0.0	V V
Using a Positive Supply	V_{SS} V_{DD}		0.0 +4.75	0.0 +5.25	V V

ICS1884 Loop Timing Mode Application Diagram (LAN/UTP Interface)



ICS1884 Loop Timing Mode Application Diagram (Optical Interface LAN/WAN)



Interfacing the ICS1884 to the IgT WAC-013-B ATM UNI Processor or the PMC-Sierra PM5345 SUNI Processor

DC Characteristics

(V_{DD} = V_{MIN} to V_{MAX}, V_{SS} = OV, T_A = T_{MIN} to T_{MAX})

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Supply current	I_{SS}	V_{DD}=+5.0V, V_{SS}=0.0V		50	mA

ECL Input/Output

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
ECL Input High Voltage	V_{IH}		V_{DD} - 1.16	V_{DD} - 0.88	V
ECL Input Low Voltage	V_{IL}		V_{DD} - 1.81	V_{DD} - 1.47	V
ECL Output High Voltage	V_{OH}		V_{DD} - 1.02		V
ECL Output Low Voltage	V_{OL}			V_{DD} - 1.62	V

TTL Input/Output

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
TTL Input High Voltage	V_{IH}	VDD=5V, VSS=0V	2.0		V
TTL Input Low Voltage	V_{IL}	VDD=5V, VSS=0V		0.8	V
TTL Output High Voltage	V_{OH}	VDD=5V, VSS=0V	2.7		V
TTL Output Low Voltage	V_{OL}	VDD=5V, VSS=0V		0.5	V
TTL Driving CMOS, Output High Voltage	V_{OH}	VDD=5V, VSS=0V	3.68		V
TTL Driving CMOS, Output Low Voltage	V_{OL}	VDD=5V, VSS=0V		0.4	V
TTL/CMOS Output Sink Current	I_{OL}	VDD=5V, VSS=0V		8	mA
TTL/CMOS Output Source Current	I_{OH}	VDD=5V, VSS=0V		-0.4	mA

Recovery Mode Crystal Parameters

Center Frequency:	10.530 MHz
Load Capacitance:	10-20 pf
Motional Cap.:	>30 pf
Oscillation Mode:	Fundamental
Max ESR:	350
Stability:	10-20 ppm
Operating Temp.:	0-70°C

Suggested Crystal Manufacturers

- Fox Crystal, Ft. Myers, FL (813) 693-0099
- Pletronics, Lynnwood, WA (206) 776-1880

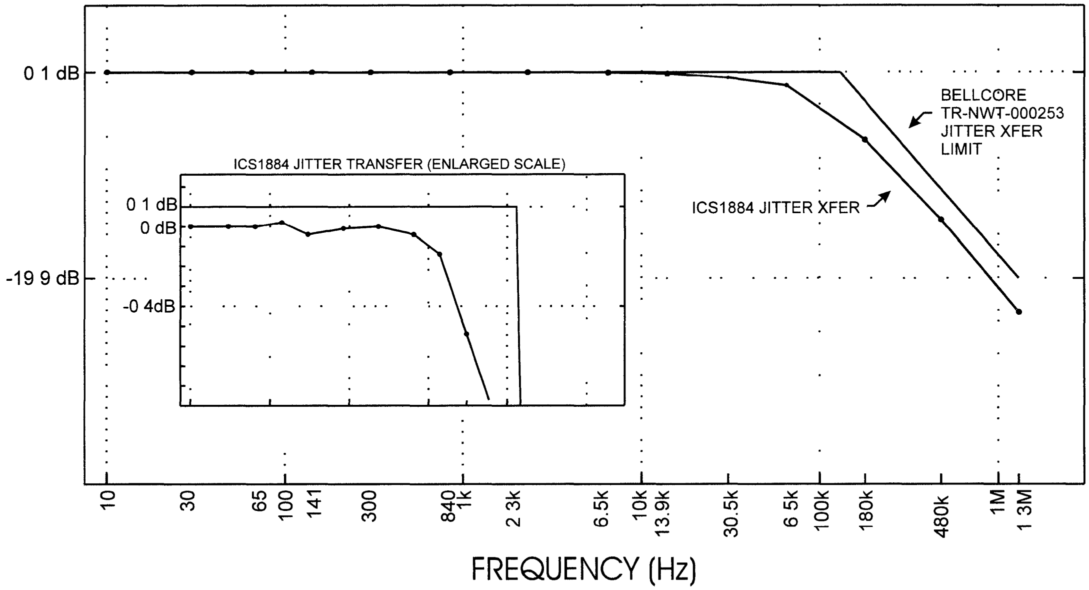
AC Characteristics

($V_{DD} = V_{MIN}$ to V_{MAX}, V_{SS} = OV, $T_A = T_{MIN}$ to T_{MAX})

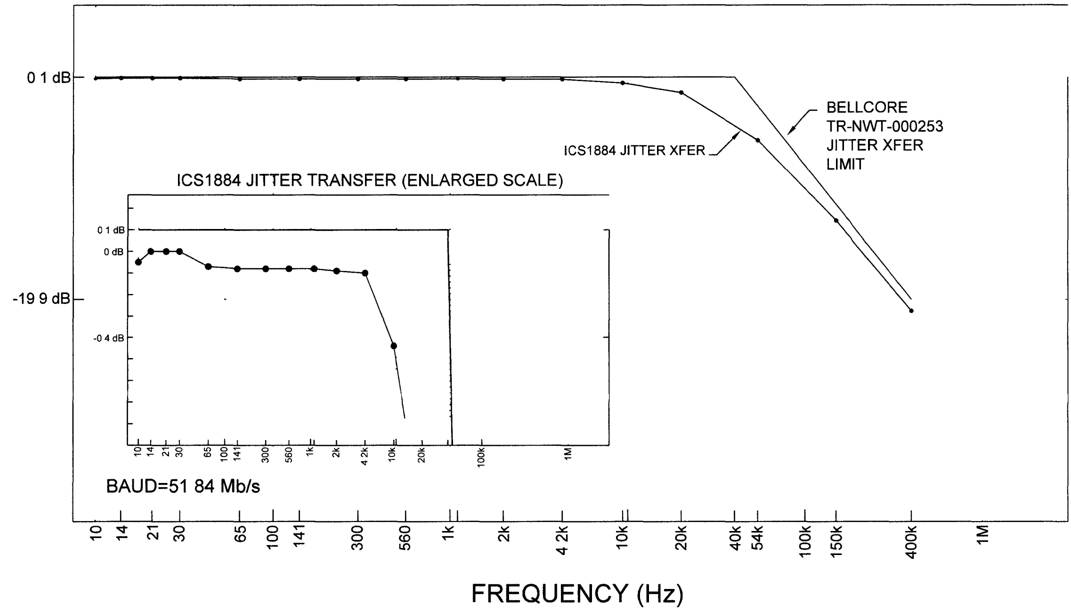
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Nominal Center Frequency	OC/STS-1 OC/STS-3		51.84 155.52		MHz
Tracking Range	Minimum Data Transition Density, D_T = 1/5	-100		100	ppm
Capture Range	Minimum D_T = 1/5	-100		100	ppm
Acquisition Time	From loss of signal or no signal to D_T = 1/2		20		µs
Bit Error Rate, BER	Minimum UI of 30% of data bit time			1×10^{-12}	BER
Output Jitter Generation	D_T = 1/2 2^7-1 PRBS 2^{23}-1PRBS			0.01 0.01 0.01	UIrms UIrms UIrms
Jitter Tolerance *see plot	f = 10 Hz f = 30 Hz f = 300 Hz f = 6.5 kHz (OC-3), 2kHz (OC-1) f = 65 kHz (OC-3), 20kHz (OC-1)	15 15 1.5 1.5 0.15			UIp-p UIp-p UIp-p UIp-p UIp-p
Jitter Transfer *see plot Peaking Bandwidth	 OC-3 OC-1			 0.1 130 40	 dB kHz kHz
Recovered Clock Output Duty Cycle D_T=1/2		48		52	%
If EXT VCXO REF is used: Reference Clock Input Frequency Tolerance	Clock Recovery Mode Clock Synthesis Mode	-100 -20		100 20	ppm ppm
Reference Clock Input Jitter Tolerance	Clock Synthesis Mode, Input Jitter from 12 kHz to 1 MHz	14			ps rms
If EXT VCXO REF is used: Reference Clock Input Rise/Fall Time Reference Clock Input Duty Cycle	10%-90%	 45		 2.0 55	 ns %
If EXT VCXO REF is used: TTL Output Rise Time TTL Output Fall Time	 C_{LOAD}=20pf, 10%-90% C_{LOAD}=20pf, 90%-10%	 2.0 2.0		 6.0 6.0	 ns ns
Transitionless Data Run (Loss of Data)			244		bit periods

Note: Consult ICS for external VCXO operation.

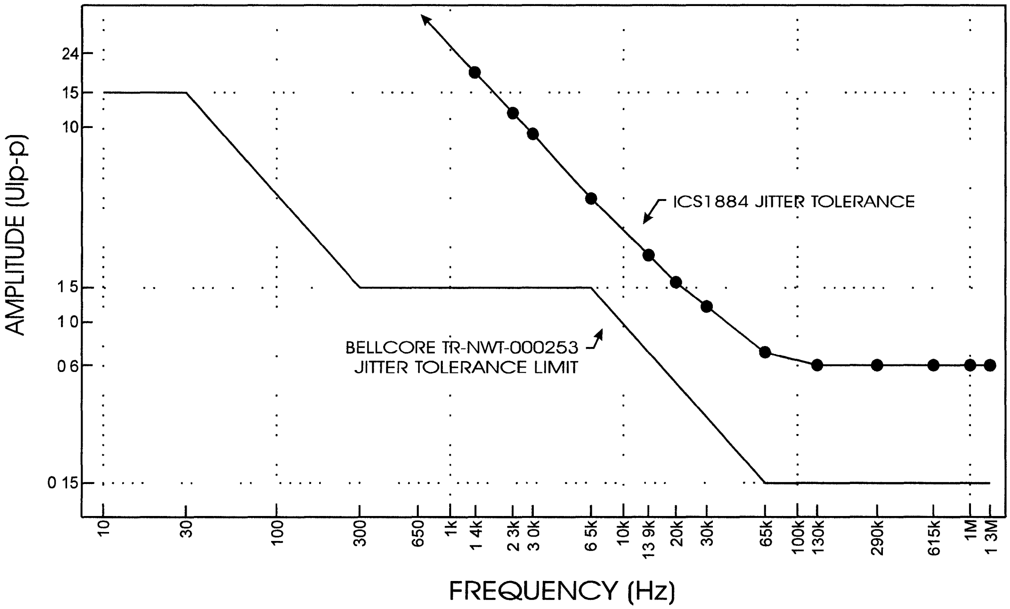
ICS1884 OC/STS-3 JITTER TRANSFER



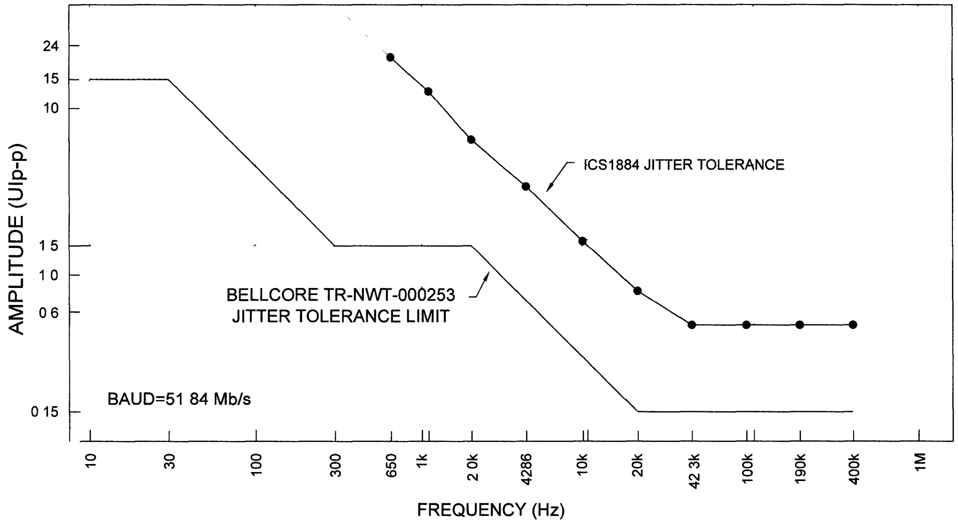
ICS1884 OC/STS-1 JITTER TRANSFER



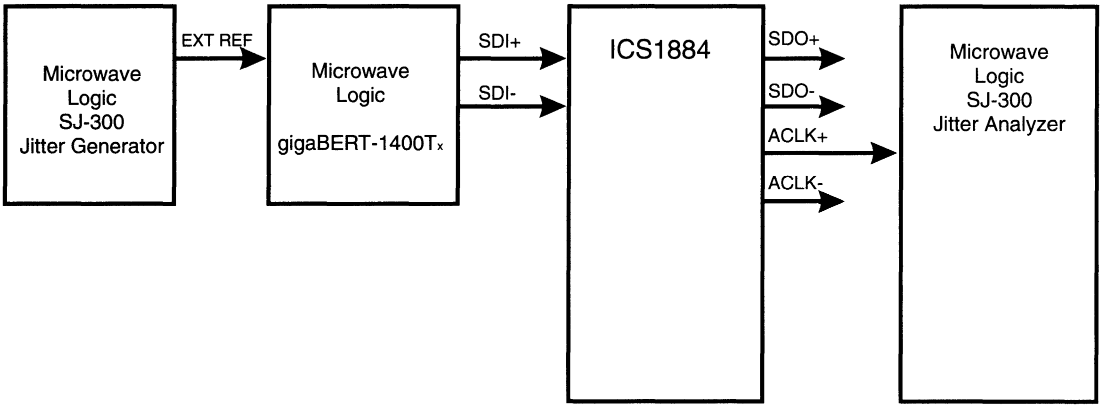
ICS1884 JITTER TOLERANCE



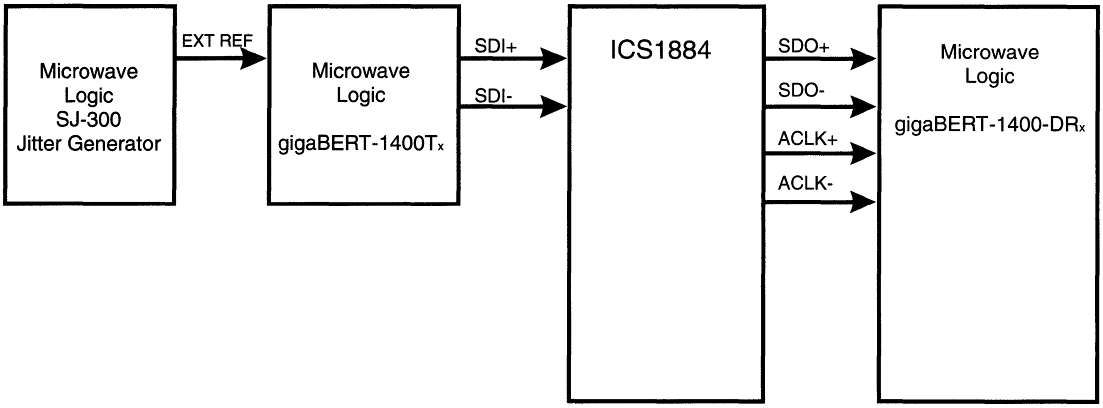
ICS1884 OC/STS-1 JITTER TOLERANCE



Jitter Transfer Test Setup



Jitter Tolerance Test Setup



Functional Description

Clock Recovery Mode

In the clock recovery mode, the **ICS1884** supports clock and data recovery for either OC/STS-1 or OC/STS-3/STM-1 line rate. ECL differential NRZ serial data is input to the **ICS1884** at either 51.84 Mb/s or 155.52 Mb/s rate. Clock and data recovery is performed on this incoming data stream. Regenerated serial data and recovered clock are output from the **ICS1884** as differential ECL. A 10.53 MHz crystal is required to properly operate the internal VCXO for this mode of operation.

Pin Descriptions

Inputs

Serial Data Differential ECL (SDI+ and SDI-)
In the clock recovery mode, input from which receive bit clock is recovered and receive data is regenerated when MSEL1 is high or unconnected. In the clock synthesis mode, one input should be connected to VDD with the other input connected to VSS.

Serial Loop Differential ECL (SDL+ and SDL-)
In the clock recovery mode, input from which transmit bit clock is recovered and transmit data is regenerated when MSEL1 is low. In the clock synthesis mode, one input should be connected to VDD with the other input connected to VSS.

External Crystal or Reference Clock (XTAL1 and XTAL2)
In the clock recovery mode, a 10.53 MHz crystal with associated capacitors should be connected to these pins. In the clock synthesis mode, either a 10.53 MHz input reference frequency or crystal should be connected to these pins. The reference signal can use either PECL or TTL-compatible levels. For PECL levels, the differential signal is simply connected to XTAL1 and XTAL2. A TTL type reference is input at XTAL1 with XTAL2 left open.

Mode Select (MSEL0 and MSEL1)
Selects the operating mode and frequency. See Table 1. Internal pull-ups set both inputs high when unconnected.

VCXO Free Run (FREEn)
Active low input which, when in the clock recovery mode, forces the internal VCXO to free run. For clock synthesis mode operation, this input should be connected to VSS.

Power Down (PWRDNn)
Active low input which stops all operations and puts the **ICS1884** into a low power sleep mode.

VCXO External Loop Filter (FVCXO)
External VCXO loop filter connection.

VCO External Loop Filter (FVCO)
External VCO loop filter connection.

Outputs

Serial Data Differential ECL (SDO+ and SDO-)
In the clock recovery mode, this is the regenerated data derived from the serial data input which is phase-aligned with the clock output.

A Clock Differential ECL (ACLK+ and ACLK-)
In the clock recovery mode, this is the 51.84 MHz or 155.52 MHz clock which is phase-aligned with the serial data output. In the clock synthesis mode, this is the 51.84 MHz or 155.52 MHz clock derived from the reference clock input.

B Clock Differential ECL (BCLK+ and BCLK-)
In the clock recovery mode, this is the 51.84 MHz or 155.52 MHz bit clock which is phase-aligned with the serial data output (typically used for loop timing applications). In the clock synthesis mode, this is the 51.84 MHz or 155.52 MHz clock derived from the reference clock input.

Reference Clock (REFCLK)
This output will be either a 6.48 MHz or 19.44 MHz clock derived from the 51.84 MHz or 155.52 MHz bit clock.

Lock/Loss Detect (LOCK)
Set high when the clock recovery has locked onto the incoming data. Set low when there is no incoming data, which in turn causes the VCXO to free run. This signal can be used to indicate or 'alarm' the next receive stage that the incoming serial data at SDI± has stopped (Loss Detect).

Output Description

The differential output drivers are current mode and are designed to drive resistive terminations in a complementary fashion. The outputs are current-sinking only, with the amount of sink current programmable via the **IPRG** pin. The sink current, which is steered to SDO, ACLK and BCLK is four times the current supplied to the **IPRG** pin. For most applications, a resistor from OVDD to IPRG will set the current of the necessary precision.

Definition of Terms

Tracking Range
The range of input data rates over which the PLL will remain in lock.

Capture Range
The range of input data rates over which the PLL can acquire lock.

Acquisition Time
The transient time required for the PLL to lock on input data from its free-running state.

Static Phase Error
The steady-state phase difference between the recovered clock sampling edge and the optimum sampling instant. This optimum instant is assumed to be halfway between the rising and falling edges of data bit.

Data Transition Density
The ratio of data transitions (i.e. 0 to 1, 1 to 0) to clock periods. $0 \leq D_T \leq 1$

Jitter
The dynamic displacement of digital signal edges from their long-term average positions.

Output Jitter
This is the jitter on the re-timed data due to a specific or some pseudo-random input data sequence PRBS.

Jitter Tolerance
The measure of the PLL's ability to track a jittered input data signal.

Ordering Information

ICS1884M

Example:

ICS XXXX M

Package Type
M=SOIC

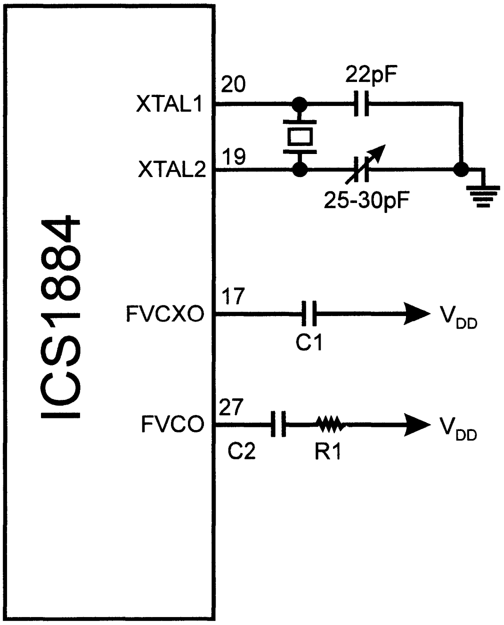
Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Jitter Transfer
The PLL exhibits a low-pass filter response to jitter applied to its input data.

Bandwidth
The frequency at which the PLL attenuates sinusoidal input jitter by 3dB.

Peaking
The maximum jitter gain of the PLL in dB.



Suggested Crystal & Loop Filter Component Values

MODE	C1	C2	R1
OC/STS-1	470pF	4.7µF	1kΩ
OC/STS-3	150pF	.68µF	1.8kΩ

Integrated Circuit Systems, Inc.

ICS1885

Product Preview

High-Performance Communications PHYceiver™

General Description

The **ICS1885** is designed to provide high performance clock recovery and generation for either 25.92 MHz, 44.736 MHz, 51.84 MHz, or 155.52 MHz NRZ or NRZI serial data streams. The **ICS1885** is ideally suited for LAN transceiver applications in either SONET, ATM, FDDI or Fast Ethernet environments.

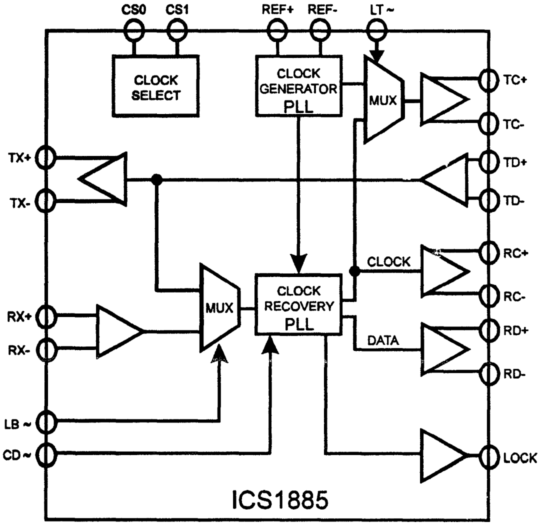
Clock and data recovery is performed on an input serial data stream or the buffered transmit data depending upon the state of the loopback input. A continuous clock source will continue to be present even in the absence of input data. All internal timing is derived from either a low cost crystal, differential or single-ended source.

The **ICS1885** utilizes advanced CMOS phase-locked loop technology which combines high performance and low power at a greatly reduced cost.

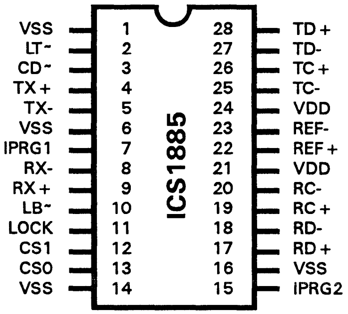
Features

- Data and clock recovery for:
  25.92 MHz (OC-½)
  44.736 MHz (T3 & DS3)
  51.84 MHz (OC-1 & STS-1)
  155.52 MHz (OC-3 & STS-3)
- Clock multiplication from either a crystal, differential or single-ended timing source
- Continuous clock in the absence of data
- no external PLL components
- Lock/Loss status indicator output
- Loopback mode for system diagnostics
- Selectable loop timing or independent timing modes
- PECL drivers with settable sink current
- Meets Bellcore TR-NWT-000253 jitter tolerance requirements

Block Diagram



Pin Configuration



28-Pin SOIC
K-7

PHYceiver is a trademark of Integrated Circuit Systems, Inc.

Table 1 - Device Clock Selection

CS1	CS0	LOOP	CLOCK RECOVERY INPUT	CLOCK FREQ	MODE	REF FREQ or CRYSTAL
VSS	VSS	VSS	Tx Data	25.92 MHz	OC-½	3.24 MHz
VSS	VDD	VSS	Tx Data	44.736 MHz	T3/DS3	5.592 MHz
VDD	VSS	VSS	Tx Data	51.84 MHz	OC-1/STS-1	6.48 MHz
VDD	VDD	VSS	Tx Data	155.52 MHz	OC-3/STS-3	19.44 MHz
VSS	VSS	VDD	Rx Data	25.92 MHz	OC-½	3.24 MHz
VSS	VDD	VDD	Rx Data	44.736 MHz	T3/DS3	5.592 MHz
VDD	VSS	VDD	Rx Data	51.84 MHz	OC-1/STS-1	6.48 MHz
VDD	VDD	VDD	Rx Data	155.52 MHz	OC-3/STS-3	19.44 MHz

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VSS		Negative supply voltage
2	LT~		Loop Timing mode select*
3	CD~		Carrier Detect input*
4	TX+		Positive Transmit serial data output
5	TX-		Negative Transmit serial data output
6	VSS		Negative supply voltage
7	IPRG1		PECL Output stage current set (TX)
8	RX-		Negative Receive serial data input
9	RX+		Positive Receive serial data input
10	LB~		Loop Back mode select*
11	LOCK		Lock detect output
12	CS1		Clock select 1 input
13	CS0		Clock select 0 input
14	VSS		Negative supply voltage
15	IPRG2		PECL Output stage current set (TC, RC and RD)
16	VSS		Negative supply voltage
17	RD+		Positive recovered data output
18	RD-		Negative recovered data output
19	RC+		Positive recovered clock output
20	RC-		Negative recovered clock output
21	VDD		Positive supply voltage
22	REF+		Positive reference clock/crystal input
23	REF-		Negative reference clock/crystal input
24	VDD		Positive supply voltage
25	TC-		Negative Transmit clock output
26	TC+		Positive Transmit clock output
27	TD-		Negative Transmit data input
28	TD+		Positive Transmit data input

* Active Low Input.

Absolute Maximum Ratings

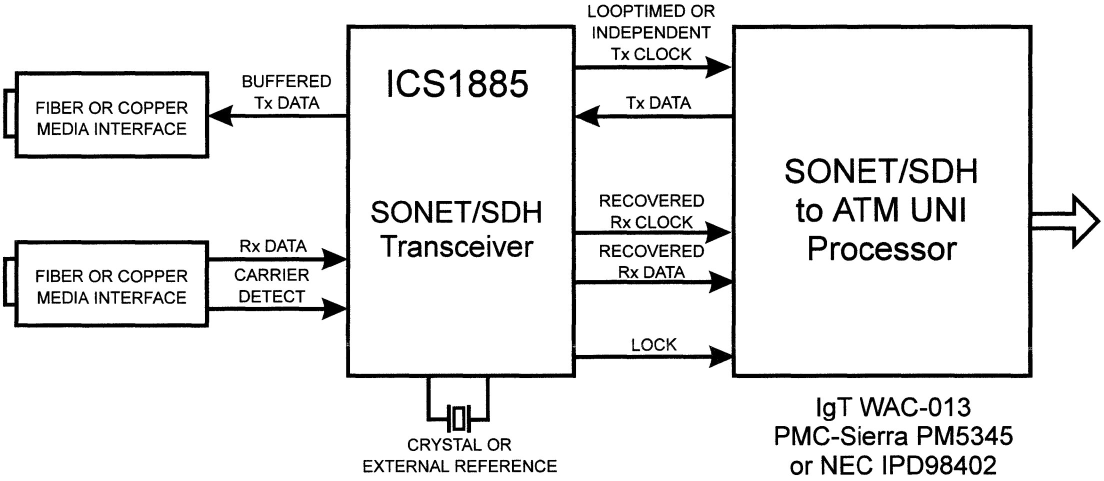
V_{DD} (measured to V_{SS})	7.0V
Ambient Operating Temperature	-55 to 125°C
Storage Temperature	-65 to 150°C
Junction Temperature	175°C
Soldering Temperature	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Ambient Operating Temp.	T_A		0	+70	°C
Using a Negative Supply	V_{SS} V_{DD}		-4.95 0.0	-5.45 0.0	V V
Using a Positive Supply	V_{SS} V_{DD}		0.0 +4.75	0.0 +5.25	V V

ICS1885 SONET/SDH to ATM Interface (Example)



DC Characteristics

($V_{DD} = V_{MIN}$ to V_{MAX}, V_{SS} = OV, $T_A = T_{MIN}$ to T_{MAX})

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Supply current	I_{SS}	V_{DD}=+5.0V, V_{SS}=0.0V		50	mA

ECL Input/Output

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
ECL Input High Voltage	V_{IH}		V_{DD} - 1.16	V_{DD} - 0.88	V
ECL Input Low Voltage	V_{IL}		V_{DD} - 1.81	V_{DD} - 1.47	V
ECL Output High Voltage	V_{OH}		V_{DD} - 1.02		V
ECL Output Low Voltage	V_{OL}			V_{DD} - 1.62	V

TTL Input/Output

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
TTL Input High Voltage	V_{IH}	VDD=5V, VSS=0V	2.0		V
TTL Input Low Voltage	V_{IL}	VDD=5V, VSS=0V		0.8	V
TTL Output High Voltage	V_{OH}	VDD=5V, VSS=0V	2.7		V
TTL Output Low Voltage	V_{OL}	VDD=5V, VSS=0V		0.5	V
TTL Driving CMOS, Output High Voltage	V_{OH}	VDD=5V, VSS=0V	3.68		V
TTL Driving CMOS, Output Low Voltage	V_{OL}	VDD=5V, VSS=0V		0.4	V
TTL/CMOS Output Sink Current	I_{OL}	VDD=5V, VSS=0V		8	mA
TTL/CMOS Output Source Current	I_{OH}	VDD=5V, VSS=0V		-0.4	mA

Input Pin Descriptions

Transmit Data Input (TD+ and TD-)
For normal operation this differential input is transferred to the TX± output through a PECL buffer. In loopback testing mode, this input is multiplexed to the input of the device clock recovery section.

Receive Data Input (RX+ and RX-)
The clock recovery and data regenerator from the receive buffer are driven from this PECL input. During loopback testing mode this input is ignored.

Clock Select (CS0 and CS1)
Selects the operating frequency according to Table 1. Internal pull-up resistors set both inputs high when left unconnected.

Carrier Detect (CD~)
Active low input which forces the VCO to free run. Upon receipt of a loss of input signal (such as from an optical-to-electrical transducer), the internal phase-lock loop will free-run at the selected operating frequency. Also, when asserted, CD will set the lock output low.

Loop Timing Mode (LT~)
Active low input which routes the recovered receive clock to the TC± outputs as well as the RC± outputs. Forces the transmit clock to be 'loop-timed' to the system clock derived from the incoming data.

Loopback Mode (LB~)
Active low input which causes the clock recovery PLL to operate using the transmit TD± input data and ignore the receive RX± data. Utilized for system loopback testing.

External Crystal or Reference Clock (REF+ and REF-)
This oscillator input can be driven from either a fundamental mode crystal or a stable reference. For either method, the reference frequency is $\frac{1}{8}$ the operating frequency.

Output Pin Descriptions

Transmit Data Differential ECL (TX+ and TX-)
This differential output is buffered TD± data. This output remains active during loopback mode.

Transmit Clock Differential ECL (TC+ and TC-)
Differential output clock used by the SONET/SDH-ATM processor for clocking out transmit data. This clock can be derived from either an independent clock source **or** from the recovered data clock (system loop time mode).

Receive Data Differential ECL (RD+ and RD-)
The regenerated differential data derived from the serial data input. In loopback mode this data is regenerated from the transmit data input (TD±). This data is phase-aligned with the negative edge of the RC clock output.

Receive Clock Differential ECL (RC+ and RC-)
The differential clock recovered with the internal clock recovery PLL. In loopback mode this clock is recovered from the transmit data (TD±) input.

Lock/Loss Detect (LOCK)
Set high when the clock recovery PLL has locked onto the incoming data. Set low when there is no incoming data, which in turn causes the PLL to free-run. This signal can be used to indicate or 'alarm' the next receive stage that the incoming serial data has stopped.

Output Description

The differential output drivers are current mode and are designed to drive resistive terminations in a complementary fashion. The outputs are current-sinking only, with the amount of sink current programmable via the **IPRGx** pins. The amount of sink current is equal to four times IPRGx current. For most applications, a resistor from VDD to IPRGx will set the current to the necessary precision. **IPRG1** supplies the current minor for the TX± output. **IPRG2** supplies the current mirrors for the RD±, RC± and TC± outputs.

Ordering Information

ICS1885M

Example:

ICS XXXX M

Package Type
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated Circuit Systems, Inc.

ICS1886

Product Preview

High-Performance Communications PHYceiver™

General Description

The **ICS1886** is designed to provide high performance clock recovery and generation for either 32.064 MHz, 34.368 MHz, 97.728 MHz or 139.264 MHz NRZ or NRZI serial data streams. The **ICS1886** is ideally suited for LAN transceiver applications in either European or Japanese communication environments.

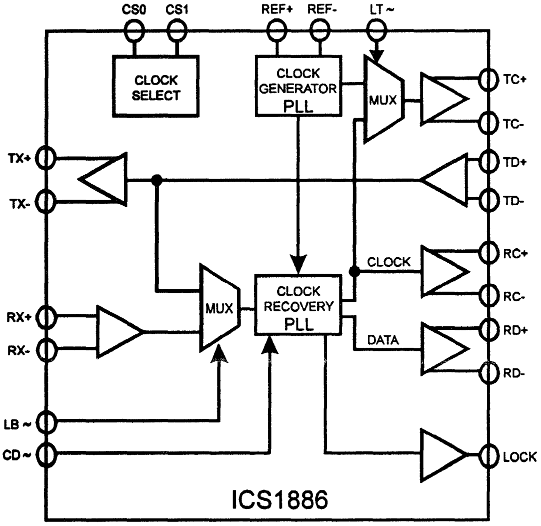
Clock and data recovery is performed on an input serial data stream or the buffered transmit data depending upon the state of the loopback input. A continuous clock source will continue to be present even in the absence of input data. All internal timing is derived from either a low cost crystal, differential or single-ended source.

The **ICS1886** utilizes advanced CMOS phase-locked loop technology which combines high performance and low power at a greatly reduced cost.

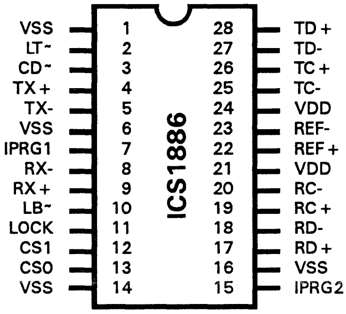
Features

- Data and clock recovery for:
  32.064 MHz (Japan)
  34.368 MHz (Europe - E3)
  97.728 MHz (Japan)
  139.264 MHz (Europe - E4)
- Clock multiplication from either a crystal, differential or single-ended timing source
- Continuous clock in the absence of data
- No external PLL components
- Lock/Loss status indicator output
- Loopback mode for system diagnostics
- Selectable loop timing mode
- PECL drivers with settable sink current

Block Diagram



Pin Configuration



28-Pin SOIC
K-7

PHYceiver is a trademark of Integrated Circuit Systems, Inc.

Table 1 - Device Clock Selection

CS1	CS0	LOOP	INPUT	CLOCK FREQ	MODE	REF FREQ or CRYSTAL
VSS	VSS	VSS	Rx Data	32.064 MHz	Japan	4.008 MHz
VSS	VDD	VSS	Rx Data	34.368 MHz	Europe - E3	4.296 MHz
VDD	VSS	VSS	Rx Data	97.728 MHz	Japan	12.216 MHz
VDD	VDD	VSS	Rx Data	139.264 MHz	Europe - E4	17.408 MHz
VSS	VSS	VDD	Tx Data	32.064 MHz	Japan	4.008 MHz
VSS	VDD	VDD	Tx Data	34.368 MHz	Europe - E3	4.296 MHz
VDD	VSS	VDD	Tx Data	97.728 MHz	Japan	12.216 MHz
VDD	VDD	VDD	Tx Data	139.264 MHz	Europe - E4	17.408 MHz

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VSS		Negative supply voltage
2	LT~		Loop Timing mode select*
3	CD~		Carrier Detect input*
4	TX+		Positive Transmit serial data output
5	TX-		Negative Transmit serial data output
6	VSS		Negative supply voltage
7	IPRG1		PECL Output stage current set (TX)
8	RX-		Negative Receive serial data input
9	RX+		Positive Receive serial data input
10	LB~		Loop Back mode select*
11	LOCK		Lock detect output
12	CS1		Clock select 1 input
13	CS0		Clock select 0 input
14	VSS		Negative supply voltage
15	IPRG2		PECL Output stage current set (TC, RC and RD)
16	VSS		Negative supply voltage
17	RD+		Positive recovered data output
18	RD-		Negative recovered data output
19	RC+		Positive recovered clock output
20	RC-		Negative recovered clock output
21	VDD		Positive supply voltage
22	REF+		Positive reference clock/crystal input
23	REF-		Negative reference clock/crystal input
24	VDD		Positive supply voltage
25	TC-		Negative Transmit clock output
26	TC+		Positive Transmit clock output
27	TD-		Negative Transmit data input
28	TD+		Positive Transmit data input

* Active Low Input.

Absolute Maximum Ratings

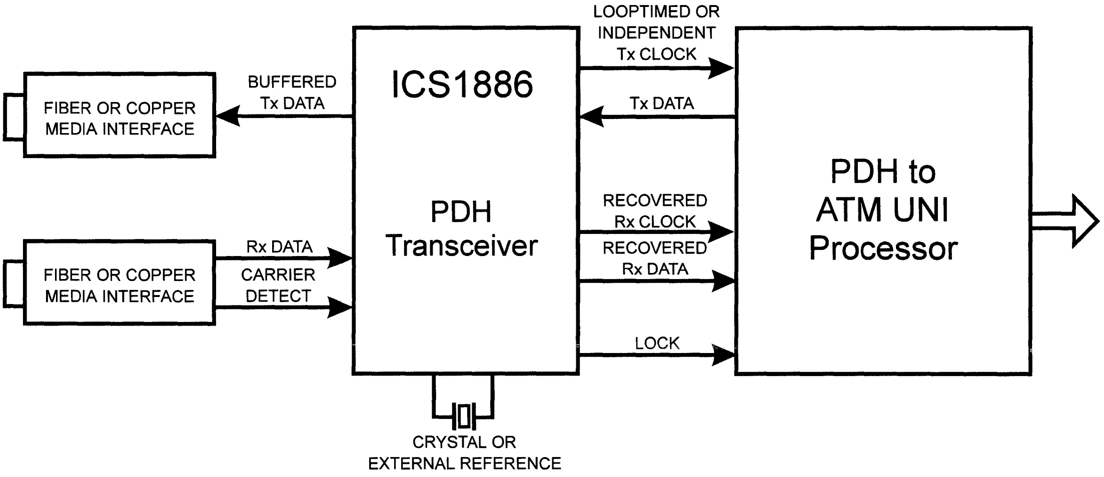
V_{DD} (measured to V_{SS})	7.0V
Ambient Operating Temperature	-55 to 125°C
Storage Temperature	-65 to 150°C
Junction Temperature	175°C
Soldering Temperature	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Ambient Operating Temp.	T_A		0	+70	°C
Using a Negative Supply	V_{SS} V_{DD}		-4.95 0.0	-5.45 0.0	V V
Using a Positive Supply	V_{SS} V_{DD}		0.0 +4.75	0.0 +5.25	V V

ICS1886 SONET/SDH to ATM Interface (Example)



DC Characteristics

(V_{DD} = V_{MIN} to V_{MAX}, V_{SS} = OV, T_A = T_{MIN} to T_{MAX})

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Supply current	I_{SS}	V_{DD}=+5.0V, V_{SS}=0.0V		50	mA

ECL Input/Output

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
ECL Input High Voltage	V_{IH}		V_{DD} - 1.16	V_{DD} - 0.88	V
ECL Input Low Voltage	V_{IL}		V_{DD} - 1.81	V_{DD} - 1.47	V
ECL Output High Voltage	V_{OH}		V_{DD} - 1.02		V
ECL Output Low Voltage	V_{OL}			V_{DD} - 1.62	V

TTL Input/Output

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
TTL Input High Voltage	V_{IH}	VDD=5V, VSS=0V	2.0		V
TTL Input Low Voltage	V_{IL}	VDD=5V, VSS=0V		0.8	V
TTL Output High Voltage	V_{OH}	VDD=5V, VSS=0V	2.7		V
TTL Output Low Voltage	V_{OL}	VDD=5V, VSS=0V		0.5	V
TTL Driving CMOS, Output High Voltage	V_{OH}	VDD=5V, VSS=0V	3.68		V
TTL Driving CMOS, Output Low Voltage	V_{OL}	VDD=5V, VSS=0V		0.4	V
TTL/CMOS Output Sink Current	I_{OL}	VDD=5V, VSS=0V		8	mA
TTL/CMOS Output Source Current	I_{OH}	VDD=5V, VSS=0V		-0.4	mA

Input Pin Descriptions

Transmit Data Input (TD+ and TD-)
For normal operation this differential input is transferred to the TX± output through a PECL buffer. In loopback testing mode, this input is multiplexed to the input of the device clock recovery section.

Receive Data Input (RX+ and RX-)
The clock recovery and data regenerator from the receive buffer are driven from this PECL input. During loopback testing mode this input is ignored.

Clock Select (CS0 and CS1)
Selects the operating frequency according to Table 1. Internal pull-up resistors set both inputs high when left unconnected.

Carrier Detect (CD~)
Active low input which forces the VCO to free run. Upon receipt of a loss of input signal (such as from an optical-to-electrical transducer), the internal phase-lock loop will free-run at the selected operating frequency. Also, when asserted, CD will set the lock output low.

Loop Timing Mode (LT~)
Active low input which routes the recovered receive clock to the TC± outputs as well as the RC± outputs. Forces the transmit clock to be 'loop-timed' to the system clock derived from the incoming data.

Loopback Mode (LB~)
Active low input which causes the clock recovery PLL to operate using the transmit TD± input data and ignore the receive RX± data. Utilized for system loopback testing.

External Crystal or Reference Clock (REF+ and REF-)
This oscillator input can be driven from either a fundamental mode crystal or a stable reference. For either method, the reference frequency is $1/8$ the operating frequency. See Table 1 for more information.

Output Pin Descriptions

Transmit Data Differential ECL (TX+ and TX-)
This differential output is buffered TD± data. This output remains active during loopback mode.

Transmit Clock Differential ECL (TC+ and TC-)
Differential output clock used by the PDH/ATM processor for clocking out transmit data. This clock can be derived from either an independent clock source **or** from the recovered data clock (system loop time mode).

Receive Data Differential ECL (RD+ and RD-)
The regenerated differential data derived from the serial data input. In loopback mode this data is regenerated from the transmit data input (TD±). This data is phase-aligned with the negative edge of the RC clock output.

Receive Clock Differential ECL (RC+ and RC-)
The differential clock recovered with the internal clock recovery PLL. In loopback mode this clock is recovered from the transmit data (TD±) input. This clock is phase-aligned with the RD data output.

Lock/Loss Detect (LOCK)
Set high when the clock recovery PLL has locked onto the incoming data. Set low when there is no incoming data, which in turn causes the PLL to free-run. This signal can be used to indicate or 'alarm' the next receive stage that the incoming serial data has stopped.

Output Description

The differential output drivers are current mode and are designed to drive resistive terminations in a complementary fashion. The outputs are current-sinking only, with the amount of sink current programmable via the **IPRGx** pins. The sink current is equal to four times the IPRGx current. For most applications, a resistor from VDD to IPRGx will set the current to the necessary precision. **IPRG1** supplies the current minor for the TX± output. **IPRG2** supplies the current mirrors for the RD±, RC± and TC± outputs.

Ordering Information

ICS1886M

Example:

ICS XXXX M

Package Type
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated Circuit Systems, Inc.

ICS1887

Product Preview

FDDI/Fast Ethernet PHYceiver™

General Description

The **ICS1887** is designed to provide high performance clock recovery and generation for 125 MHz serial data streams. The **ICS1887** is ideally suited for LAN transceiver applications in either FDDI or Fast Ethernet environments. The **ICS1887** converts NRZ to/from NRZI data in addition to providing a 5-bit parallel digital data transmit and receive interface.

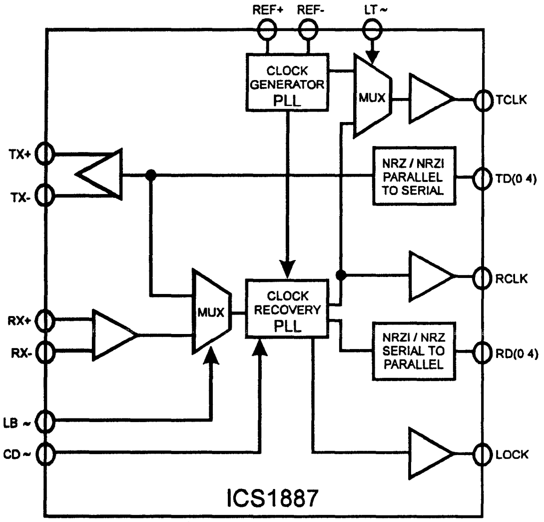
Clock and data recovery is performed on an input serial data stream or the buffered transmit data depending upon the state of the loopback input. A continuous clock source will continue to be present even in the absence of input data. All internal timing is derived from either a low cost crystal, differential or single-ended source.

The **ICS1887** utilizes advanced CMOS phase-locked loop technology which combines high performance and low power at a greatly reduced cost.

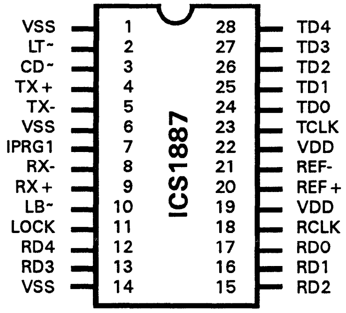
Features

- Single IC solution to existing designs requiring multiple devices
- Data and clock recovery for 125 MBaud FDDI or Fast Ethernet applications
- Clock multiplication from either a crystal, differential or single-ended timing source
- Continuous clock in the absence of data
- No external PLL components
- Lock/Loss status indicator output
- Loopback mode for system diagnostics
- Selectable loop timing mode
- PECL driver with settable sink current
- Parallel digital transmit and receive data interface
- NRZ to/from NRZI data conversion
- Consult ICS for optional configurations and data rates

Block Diagram



Pin Configuration



28-Pin SOIC
K-7

PHYceiver is a trademark of Integrated Circuit Systems, Inc.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VSS		Negative supply voltage
2	LT~		Loop Timing mode select*
3	CD~		Carrier Detect input*
4	TX+		Positive Transmit serial data output
5	TX-		Negative Transmit serial data output
6	VSS		Negative supply voltage
7	IPRG1		PECL Output stage current set (TX)
8	RX-		Negative Receive serial data input
9	RX+		Positive Receive serial data input
10	LB~		Loop Back mode select*
11	LOCK		Lock detect output
12	RD4		Recovered data output 4
13	RD3		Recovered data output 3
14	VSS		Negative supply voltage
15	RD2		Recovered data output 2
16	RD1		Recovered data output 1
17	RD0		Recovered data output 0
18	RCLK		Recovered Receive clock output
19	VDD		Positive supply voltage
20	REF+		Positive reference clock/crystal input
21	REF-		Negative reference clock/crystal input
22	VDD		Positive supply voltage
23	TCLK		Transmit clock output
24	TD0		Transmit data input 0
25	TD1		Transmit data input 1
26	TD2		Transmit data input 2
27	TD3		Transmit data input 3
28	TD4		Transmit data input 4

* Active Low Input.

Absolute Maximum Ratings

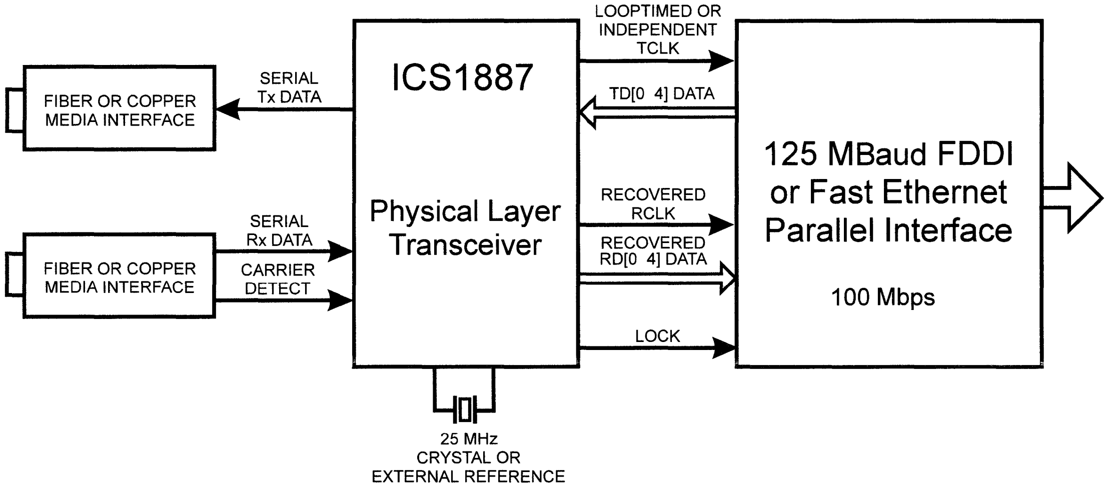
V_{DD} (measured to V_{SS}) 7.0V
Ambient Operating Temperature . . . . -55 to 125°C
Storage Temperature. . . . . -65 to 150°C
Junction Temperature . . . . 175°C
Soldering Temperature . . . . 260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Ambient Operating Temp.	T_A		0	+70	°C
Using a Negative Supply	V_{SS} V_{DD}		-4.95 0.0	-5.45 0.0	V V
Using a Positive Supply	V_{SS} V_{DD}		0.0 +4.75	0.0 +5.25	V V

ICS1887 FDDI/Fast Ethernet



DC Characteristics

(V_{DD} = V_{MIN} to V_{MAX}, V_{SS} = OV, T_A = T_{MIN} to T_{MAX})

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Supply current	I_{SS}	V_{DD}=+5.0V, V_{SS}=0.0V		50	mA

ECL Input/Output

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
ECL Input High Voltage	V_{IH}		V_{DD} - 1.16	V_{DD} - 0.88	V
ECL Input Low Voltage	V_{IL}		V_{DD} - 1.81	V_{DD} - 1.47	V
ECL Output High Voltage	V_{OH}		V_{DD} - 1.02		V
ECL Output Low Voltage	V_{OL}			V_{DD} - 1.62	V

TTL Input/Output

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
TTL Input High Voltage	V_{IH}	VDD=5V, VSS=0V	2.0		V
TTL Input Low Voltage	V_{IL}	VDD=5V, VSS=0V		0.8	V
TTL Output High Voltage	V_{OH}	VDD=5V, VSS=0V	2.7		V
TTL Output Low Voltage	V_{OL}	VDD=5V, VSS=0V		0.5	V
TTL Driving CMOS, Output High Voltage	V_{OH}	VDD=5V, VSS=0V	3.68		V
TTL Driving CMOS, Output Low Voltage	V_{OL}	VDD=5V, VSS=0V		0.4	V
TTL/CMOS Output Sink Current	I_{OL}	VDD=5V, VSS=0V		8	mA
TTL/CMOS Output Source Current	I_{OH}	VDD=5V, VSS=0V		-0.4	mA

Input Pin Descriptions

Parallel Transmit Data (TD0 .. TD4)
Five bit TTL compatible digital input, which is received by the **ICS1887** on the positive edge of TCLK. High impedance input drivers routed to the serial NRZ to NRZI converter. In loopback testing mode, this NRZI data is multiplexed to the input of the device clock recovery section.

Differential ECL Receive Data Input (RX+ and RX-)
The clock recovery and data regenerator from the receive buffer are driven from this PECL input. During loopback testing mode this input is ignored.

Carrier Detect (CD~)
Active low input which forces the VCO to free run. Upon receipt of a loss of input signal (such as from an optical-to-electrical transducer), the internal phase-lock loop will free-run at the selected operating frequency. Also, when asserted, CD will set the lock output low.

Loop Timing Mode (LT~)
Active low input which routes the recovered receive clock to the TCLK output as well as the RCLK output. Forces the transmit clock to be 'loop-timed' to the system clock derived from the incoming data.

Loopback Mode (LB~)
Active low input which causes the clock recovery PLL to operate using the transmit input data reference and ignore the receive RX± data. Utilized for system loopback testing.

External Crystal or Reference Clock (REF+ and REF-)
This oscillator input can be driven from either a fundamental mode crystal or a stable reference. For either method, the reference frequency is 25.00 MHz.

Output Pin Descriptions

Differential ECL Transmit Data (TX+ and TX-)
This differential output is converted TD[0..4] serial data. This output remains active during loopback mode.

Transmit Clock (TCLK)
TTL compatible 25 MHz clock used by the parallel processor transmitter for clocking out transmit data. This clock can be derived from either an independent clock source **or** from the recovered data clock (system loop time mode).

Parallel Receive Data (RD0 .. RD4)
The regenerated five bit parallel data derived from the serial data input. In loopback mode this data is regenerated from the transmit data. This data is phase-aligned with the negative edge of RCLK clock output.

Receive Clock (RCLK)
A 25 MHz digital clock recovered with the internal clock recovery PLL. In loopback mode this clock is recovered from the transmit data.

Lock/Loss Detect (LOCK)
Set high when the clock recovery PLL has locked onto the incoming data. Set low when there is no incoming data, which in turn causes the PLL to free-run. This signal can be used to indicate or 'alarm' the next receive stage that the incoming serial data has stopped.

Output Description

The differential driver for the TX± is current mode and is designed to drive resistive terminations in a complementary fashion. The output is current-sinking only, with the amount of sink current programmable via the **IPRG1** pin. The sink current is equal to four times the IPRGx current. For most applications, a resistor from VDD to IPRG1 will set the current to the necessary precision.

Ordering Information

ICS1887M

Example:

ICS XXXX M

Package Type
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

ICS1888
Product Preview

High Performance Twisted Pair Communication PHYceiver™

Description

The **ICS1888** is an integrated PHY interface solution providing a complete UTP/STP to UNI (User Network Interface) solution for SONET, ATM and B-ISDN like communication over CAT-5 type cable. The **ICS1888** is designed to provide high performance adaptive equalization, clock recovery and data regeneration for 155.52 Mb/s serial NRZ data streams.

The **ICS1888** is capable of receiving and transmitting 155.52 Mb/s NRZ data rates over Category 5 UTP/STP (Unshielded Twisted Pair/ShieldedTP) cables at up to distances of 100 meters. The internal adaptive equalizer corrects for any phase or amplitude distortion.

A continuous clock source will continue to be present even in the absence of input data. All internal timing is derived from a low cost crystal or either a differential or single-ended timing source.

The **ICS1888** utilizes advanced CMOS phase-locked loop technology which combines high performance and low power at a greatly reduced cost.

Features

- Adaptive equalization with clock recovery
- Interfaces to Category 5 STP/UTP cables
- Data regeneration and clock recovery for:

  155.52 MHz (STS-3/OC-3)
- Clock multiplication from either a crystal, differential or single-ended timing source
- Continuous clock in the absence of data
- No external PLL components required
- Lock/Loss status indicator output
- Loopback mode for system diagnostics
- Selectable looptiming mode
- PECL Drivers with settable sink current
- Low power CMOS technology
- Consult ICS for optional data rates and coding

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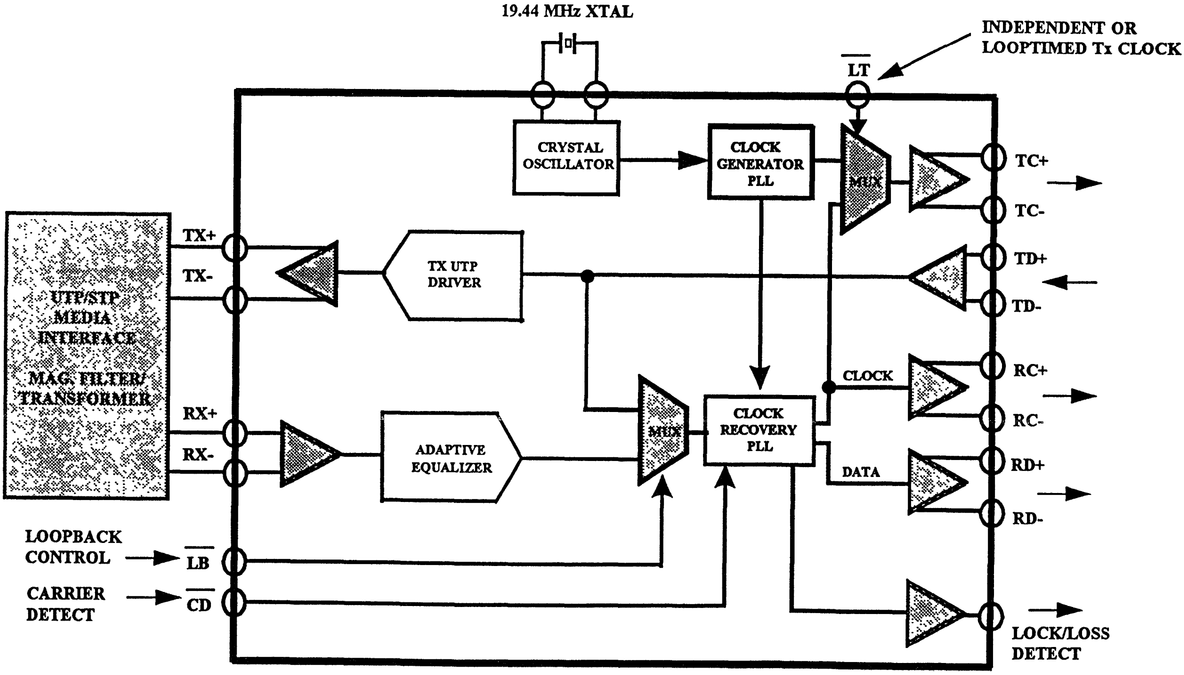
Block Diagram



Integrated
Circuit
Systems, Inc.

ICS1889

Product Preview

100Base-FX Integrated PHYceiver™

General Description

The **ICS1889** is a fully integrated physical layer device supporting 100 Megabits per second CSMA/CD Ethernet fiber optic applications. It is designed to support the requirements of DTEs (adapter cards), and hub or router ports. It is compliant with the ISO/IEC 8802 Fast Ethernet standard for 100Base-FX. It provides a Media Independent Interface allowing direct chip-to-chip connection, motherboard-to-daughter board connection or connection via a cable in a similar manner to the AUI approach used with 10Base-T systems. A station management interface is provided to enable it to receive command information and send status information. It transmits and receives NRZI data and interfaces directly to the optical transceiver. It can operate in either half duplex or full duplex.

Features

- One chip integrated physical layer
- ISO/IEC 8802-3 CSMA/CD compliant
- 100 Base-FX Half & Full Duplex
- Far end fault detection
- Media Independent Interface (MII)
- Station management interface
- Extended register set
- Transmit clock synthesis
- Receive clock and data recovery
- Detailed receive error reporting
- Extended Test Modes

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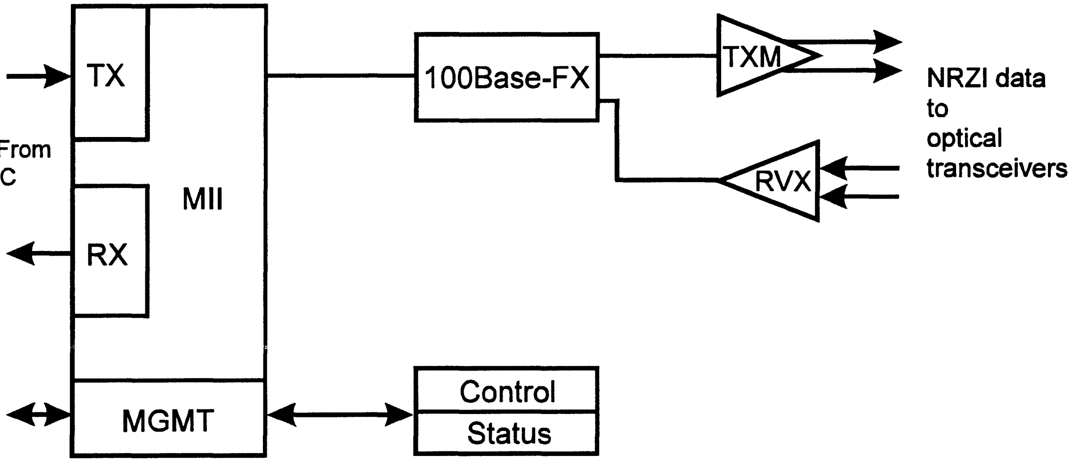
Block Diagram



PHYceiver is a trademark of Integrated Circuit Systems, Inc.

Integrated
Circuit
Systems, Inc.

ICS1890

Product Preview

10Base-T/100Base-TX Integrated PHYceiver™

General Description

The **ICS1890** is a fully integrated physical layer device supporting 10 and 100 Megabits per second CSMA/CD Ethernet applications. It is designed to support the requirements of DTEs (adapter cards or motherboards), switching hubs, concentrators (repeaters) and router ports. It is compliant with the ISO/IEC 8802-3 Ethernet standard. It provides a Media Independent Interface allowing direct chip-to-chip connection, motherboard-to-daughter board connection or connection via a cable in a similar manner to the AUI approach used with 10Base-T systems. A station management interface is provided to enable it to receive command information and send status information. It interfaces directly to a single transmit and receive isolation transformers and can support shielded twisted pair (STP) and unshielded twisted pair (UTP) category 5 cables up to 105 meters. It can operate in half duplex or full duplex at either 10 or 100 Mbps and electronically switch between the two modes. By employing auto-negotiation and sense logic it is able to determine the technology capabilities of it's remote partner and then adjust its operating mode to match the highest performance common operating mode.

Features

- One chip integrated physical layer
- ISO/IEC 8802-3 CSMA/CD compliant
- 100 Base-TX Half & Full Duplex
- 10 Base-T Half & Full Duplex
- Stream Cipher Scrambler/Descrambler
- MLT-3 Encoder/Decoder
- Adaptive Equalization & DC Restoration
- Auto Sense & Negotiation (N-Way)
- Integrated 10/100 switch
- Enhanced Status & Configuration
- Media Independent Interface (MII)
- Station management interface

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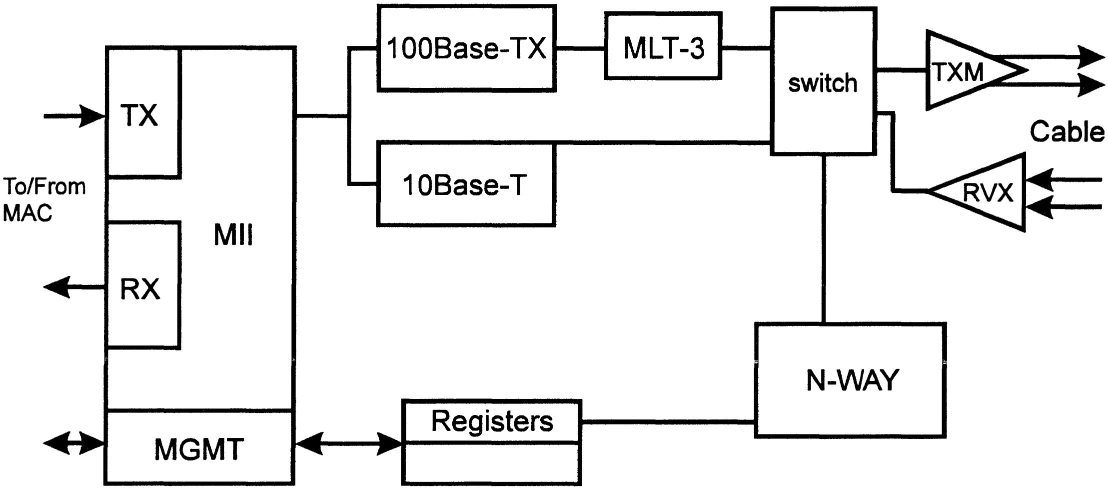
Block Diagram



PHYceiver is a trademark of Integrated Circuit Systems, Inc.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. ICS reserves the right to change or discontinue these products without notice.

Integrated
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Systems, Inc.

ICS1891

Product Preview

100Base-TX Integrated PHYceiver™ for Repeaters

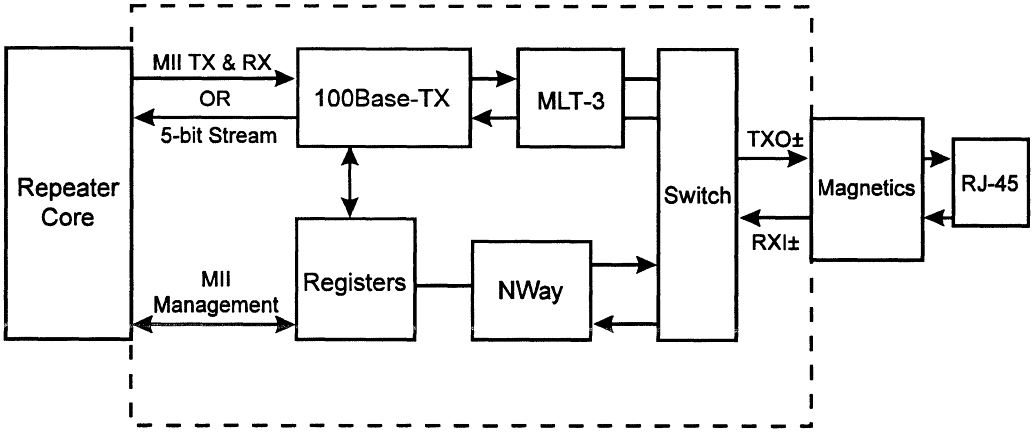
General Description

The **ICS1891** is a fully integrated physical layer device supporting 100 Megabits per second CSMA/CD Ethernet Repeater applications. It is designed to meet the specific requirements of repeater applications such as small PCB footprint and low power. It is compliant with the ISO/IEC 8802-3 Ethernet standard. It provides a Media Independent Interface allowing direct chip-to-chip connection, motherboard-to-daughter board connection, or connection via a cable in a similar manner to the AUI approach used with 10Base-T systems. A Stream Interface may also be used to enable class 2 repeater designs. A station management interface is provided to enable it to receive command information and send status information. It interfaces directly to a single transmit and receive isolation transformers and can support shielded twisted pair (STP) and unshielded twisted pair (UTP) category 5 cables up to 105 meters. Auto-negotiation and sense logic allows repeater management to determine the technology capabilities of its remote partner and ensure a proper connection at 100 Megabits per second.

Features

- One chip integrated physical layer
- ISO/IEC 8802-3 CSMA/CD compliant
- Small 14mm x 14mm QFP package
- Low Power Consumption
- 5-bit Stream Interface
- Full 100 Base-TX support
- Stream Cipher Scrambler/Descrambler
- MLT-3 Encoder/Decoder
- Adaptive Equalization & DC Restoration
- Auto Sense & Negotiation (N-Way)
- Enhanced Status & Configuration
- Media Independent Interface (MII)
- Station management interface

Block Diagram



ICS
Multimedia
Products

At ICS, the digital world meets the real world with multimedia products for adding audio and motion video to computer and consumer electronics products. We combine our experience in phase-locked loop, digital signal processing, and mixed-signal design to produce multimedia ICs for OEMs around the world. Our solutions in audio and video are matched to OEM requirements for cost-effective products.

In video, ICS offers the GSP and 2008 product lines. The GSP family offers Genlocking to enable full-motion, computer-generated text and graphics to be overlayed on any standard video signal, such as TV, camcorder, VCR, or video disc. It also supports easy recording of the enhanced video image onto videotape. The ICS2008A line implements VITC and LTC read and write of the standard SMPTE Time Code data, synchronized with MTC (MIDI time code) output.

In audio, ICS offers Wavedec and WaveFront. Wavedec, our digital audio codec for computer and consumer electronics products, records and plays 16-bit compatible files for applications running in MS DOS or MS Windows platforms. WaveFront, our wavetable synthesizer, creates the audio subsystem required for producing the full General MIDI patch set on next-generation, 16 bit sound cards and consumer electronics products.

Most importantly, we understand the systems-integration challenges of adding multimedia capabilities to your products. Our applications engineering team includes engineers responsible for the Multisound product from our Turtle Beach Systems division and for the Jazz 16™ multimedia audio chipset from Media Vision. ICS views our multimedia IC business as a systems business and we can assist you with your systems-integration needs. We look forward to partnering with you and making you and your new products succeed in the marketplace.

Jazz 16 is a trademark of Media Vision.

ICS Multimedia Product Selection Guide

Product Applications	ICS Device Type	Description	Package Types	Page
Video Graphics	GSP500	NTSC Genlock.	68-Pin PLCC	G-3
	GSP600	PAL Genlock.	68-Pin PLCC	G-49
Codecs	ICS2002	Business Audio Codec.	44-Pin PLCC	G-85
Sound/Video Synchronization	ICS2008A	Improved SMPTE-MIDI Peripheral.	44-Pin PLCC	G-105
Audio Mixers	ICS2101	5 Channel Digitally Controlled Audio Mixer.	28-Pin DIP, SOIC	G-123
	ICS2102	Sound Blaster Compatible Mixer.	28-Pin SOIC	G-131
Wavetable Synthesis	ICS2115	WaveFront MIDI Synthesizer.	84-Pin PLCC 100-Pin TQFP	G-141
	ICS2116	WaveFront ISA Interface.	100-Pin PQFP	G-171
	ICS2122	WaveFront Sounds 2Mb General MIDI.	44-Pin SOIC	G-185
	ICS2124	WaveFront Sounds 512kb General MIDI ROM.	44-Pin SOIC	G-189
	ICS2125	WaveFront Sounds 4Mb General MIDI ROM.	32-Pin SOIC	G-193
Audio Synthesis Clock Generator	ICS9120-08/ ICS9120-09	Clock for Audio Systems.	8-Pin SOIC	C-35

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. ICS reserves the right to change or discontinue these products without notice.

Integrated
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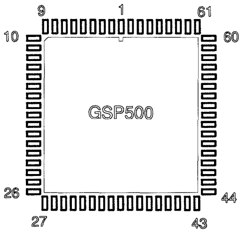
GSP500

VGA/NTSC Video Genlock Processor with Overlay

Overview

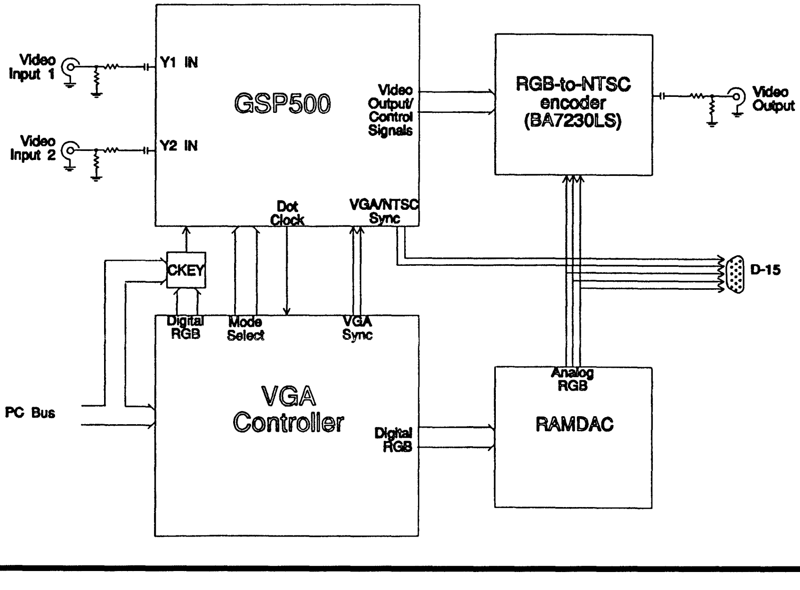
The **GSP500** allows the text and graphic images of VGA and Super VGA controllers to be displayed on standard NTSC televisions or recorded on a VCR. Additionally, the **GSP500** accepts external video input from a camcorder or a VCR and will synchronize (genlock) the VGA or Super VGA controller to the external video. The **GSP500** also allows VGA and video images to be overlaid on the same television screen. The **GSP500** meets or exceeds all RS-170A broadcast standards for timing accuracy and allows the VGA controller to maintain true NTSC compatibility at all times. The **GSP500** is compatible with virtually all VGA controllers. Tseng Labs, Oak Technology, Trident Microsystems, S3, and NCR already have full BIOS support available for the **GSP500**.



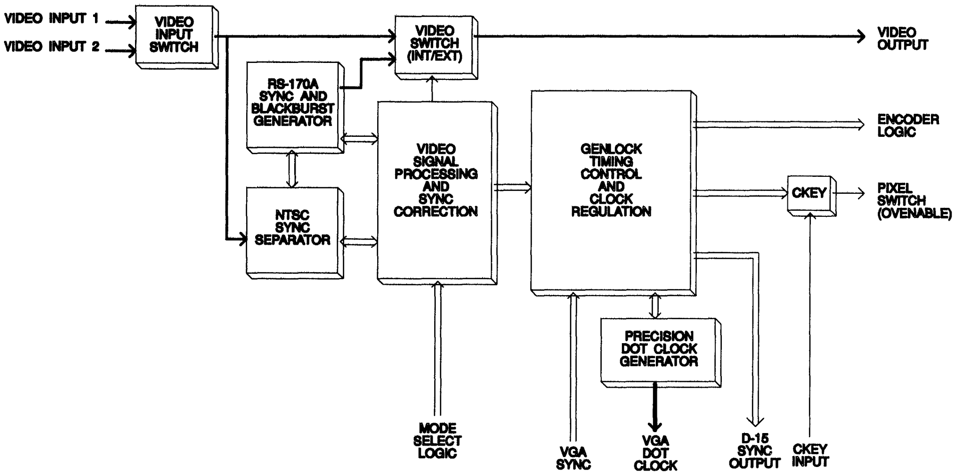
68-Pin PLCC
K-10

Features

- Direct input of NTSC or S-Video (S-VHS and Hi-8 video).
- On board NTSC/S-Video sync and black burst generation for local video operation. Video chroma burst separate with 3.579545 MHz and 14.31818 MHz phase locked outputs.
- Meets or exceeds alltiming specifications for studio and broadcast television.
- High efficiency NTSC/S-Video conversion that maintains VGA performance.
- Dynamic overscan and underscan adjustment of NTSC/S-Video modes under BIOS and/or software control.
- Software selection between all VGA and NTSC/S-Video modes.
- NTSC/S-Video conversion support for all VGA and Extended VGA modes with 480 or fewer lines.
- Built-in dot clock circuitry to eliminate crystal oscillators for VGA, plus extended VGA operation up to 135 MHz.
- Low power consumption, ideal for laptop computers.



Internal Block Diagram



Theory of Operation

The **GSP500** can be thought of as an extremely sophisticated dot clock generator. In its simplest form, the **GSP500** will generate all of the dot clock frequencies necessary to drive VGA and Super VGA controllers. The different frequencies are selected with the **MODE SELECT LOGIC** from the VGA chip. Selection is similar to selecting frequencies on any of the ICS dot clock generators (i.e., ICS1394, ICS1494, ICS1561, ICS2494, etc.). Additionally, there are four reserved frequency addresses. These are labeled GL (genlock), OV (overlay), VO (video only), and GO (graphics only). Choosing any of these addresses will switch the **GSP500** from VGA mode to NTSC mode. Under NTSC mode, the **GSP500** accepts vertical and horizontal **VGA SYNC** from the VGA controller and uses the sync to generate and adjust the **VGA DOT CLOCK**. The **GSP500** will automatically vary the frequency of the dot clock in order to synchronize the VGA sync signals with an NTSC reference signal. This reference signal can be derived from a video device (such as a camcorder) connected to **VIDEO INPUT 1** or **VIDEO INPUT 2**. The **GSP500** provides an RGB-to-NTSC encoder with the **VIDEO OUTPUT** signal which is either **VIDEO INPUT 1**, **VIDEO INPUT 2**, or an internally generated black burst signal. All of the necessary **ENCODER LOGIC** signals to properly drive the encoder are provided by the **GSP500**.

During NTSC modes the **GSP500** also creates the **D-15 SYNC OUTPUT** for the monitor connection to allow for TV projection output of the VGA images. The **PIXEL SWITCH** information derived from external **CKEY INPUT** tells the encoder whether to display the VGA image or external video for each pixel. Assuming the images are genlocked, this creates the overlay effect.

Block definition

Video Input Switch

The Video Input Switch selects whether the **GSP500** uses VIDEO INPUT 1 or VIDEO INPUT 2 as the external video source. It is controlled by an external pin of the **GSP500**.

NTSC Sync Separator

The **GSP500** contains a high quality sync separator to allow direct input of NTSC, S-VHS, or HI-8 video signals from camcorders, VCRs, and other video products. The **GSP500** utilizes a differential video input circuitry for maximum noise immunity. It also employs digital noise filtering and enhanced digital signal tracking technology to ensure maximum compatibility with consumer, industrial, and broadcast video signals. Although low cost video sync separator products are commonly available, they are primarily designed for television and video monitor use. The simple diode clamping circuit used in these devices does not have the accuracy or noise immunity required for genlocking.

RS-170A Sync and Black Burst Generator

RS170A Sync Generator

The studio quality built-in video sync generator allows the **GSP500** to operate without an external video input and still maintain broadcast video timing. This assures NTSC compatibility at all times. When external video is present, the sync generator works in conjunction with the sync separator to isolate sync from noisy video signals.

Black Burst Generation

Most RGB-to-NTSC encoders synchronize a crystal oscillator to the chroma burst signal of the external video signal. This provides the color reference portion of the video signal. If an external video signal is not available, the crystal oscillator will free run, creating screen artifacts such as 45 degree moving lines in constant color portions of the screen. To eliminate this problem, the **GSP500** generates a black burst video signal. Black burst video is an analog signal containing both sync and a correctly phased chroma burst signal. This ensures proper color reference generation at all times. The **GSP500** provides black burst output to the encoder when external video is either missing or not selected (non-genlock mode).

INT/EXT Video Switch

The Internal/External Video Switch determines whether the encoder uses external video or the black burst signal. If external video is chosen, the **GSP500** will simply pass the external video signal through to the encoder, unaffected. Black burst is used when external video is not present. The switch is controlled by the Video Signal Processing and Sync Correction circuitry.

Video Signal Processing and Correction

Video Signal Processing

The Video Signal Processing circuitry of the **GSP500** measures the incoming video signal for basic timing accuracy and signal noise. It contains intelligent circuitry to remove extraneous portions of the video signal that would normally be incorrectly categorized as sync. This is extremely important when using a VCR as a video input. If there is an interruption of the external video signal, this circuit will automatically switch inputs from the external video signal to the internal sync generator. When the external video signal resumes, the circuit will automatically switch back to the external video. The Video Signal Processing accepts the MODE SELECT LOGIC from the VGA chip. This logic chooses either VGA or NTSC operation and selects whether genlock to external video is to be enabled.

Sync Correction

The Sync Correction circuitry looks for missing sync pulses, block sync, single field video, and phase shift errors caused by the head switching zone of a VCR. It assures proper genlock during all of these problems common in consumer video products.

Genlock Timing Control and Clock Regulation

The **GSP500** looks at the input sync from the VGA controller and determines how to alter the dot clock to create RS-170A timing. Both the frequency and the method can change with different VGA modes. The **GSP500** enables virtually any VGA controller capable of interlacing to create RS-170A timing. The **GSP500**'s unique architecture provides ultra-high efficiency and flexibility and allows the frequency of the dot clock to be controlled totally under BIOS or software control. Screen attributes such as horizontal width and position can be individually programmed for each mode while maintaining genlock integrity. This circuit will modify the timing of virtually any mode, with 480 or fewer lines, to meet RS-170A NTSC specifications. The **GSP500** genlock timing control and clock regulation design is awaiting patent approval.

Precision Dot Clock Generator

The **GSP500** uses the same state-of-the-art dot clock technology that has made ICS the premier supplier of VGA dot clock generators. ICS offers the highest accuracy and lowest jitter products available.

CKEY

The ckey (or color-key) circuitry creates the pixel switch for the encoder. This signal determines whether the VGA image or external video is displayed for each pixel. Ckey is modified by the **GSP500** to ensure that the pixel switch signal is delayed (to make up for delays in the RAMDAC) and that it has proper levels during sync and blanking. If the VGA and external signals are genlocked, this pixel switch will create an overlay effect.

PIN NUMBER	NAME	DESCRIPTION
1	VLE	VERTICAL LOCK ENABLE. HIGH for VGA controllers. LOW disables vertical lock feature, may be useful for Non-VGA Operation.
2	ODD/EVEN	ODD/EVEN FIELD IDENTIFICATION. HIGH indicates odd numbered field, LOW indicates even numbered field.
3	BP	BACK PORCH PULSE. Negative polarity TTL level signal used by some RGB-to-NTSC encoders.
4	DATAIN	Data input for inserting SMPTE time code in video signal.
5	CB	COMPOSITE BLANKING OUTPUT. Indicates non-screen data portions of NTSC signal.
6	CS	COMPOSITE SYNC. NTSC Composite sync output for RGB-to-NTSC encoders. Gated off during VGA modes.
7	CKEY	COLOR KEY. Resultant input from the 8-bit compare of digital RGB (P0-P7) and a software selectable byte. This color key determines which pixels display VGA and which display external video in overlay mode. See Hardware Interface Manual for more details.
8	TEST	For ICS use only.
9	VSYNCOUT	VERTICAL SYNC OUTPUT. Vsync output for DB-15 connector.
10	DATAFRAME	TTL level framing signal active during lines 10-20. For use in time code applications.
11	OVENABLE	OVERLAY ENABLE. Fast pixel rate switch. HIGH displays NTSC output, LOW display RGB output. Used for overlay encoders. See Application Notes for wiring details.
12	I/ES	INT./EXT. SYNC. Determines sync selection in OVENABLE signal. Tie LOW normally.
13	LOC/REM	LOCAL/REMOTE. A LOW output state signifies REMOTE status indicating that external video is present and a genlock mode has been selected. If external video goes away or a non-genlock mode is selected, LOCAL/REMOTE will go HIGH.
14	BRSTACT	For ICS use only.
15	$\overline{\text{FRTSTOUT}}$	For ICS use only, wire to pin 37.
16	HS	HORIZONTAL SYNC. For some RGB-to-NTSC encoders. Gated off during VGA modes.
17	$\overline{\text{HRSTOUT}}$	For ICS use only.
18	HSYNCOUT	HORIZONTAL SYNC OUTPUT. Hsync output for DB-15 connector.
19	VSS	Digital ground. We strongly recommend the use of a multilayer board and a ground plane.
20	VDD	5 Volt digital power. We strongly recommend the use of a multilayer board and a power plane.
21	VDD	5 Volt digital power. We strongly recommend the use of a multilayer board and a power plane.
22	VSS	Digital ground. We strongly recommend the use of a multilayer board and a ground plane.
23	FS5	Frequency Select 5. Selects between multiple VGA Dot Clock frequencies, Genlock modes and NTSC frequencies. See Dot Clock Generation and NTSC Mode Selection sections for a more detailed description. Also see Application Notes for wiring diagrams and BIOS Interface Manual for details.

PIN NUMBER	NAME	DESCRIPTION
24	FS4	Frequency Select 4. Selects between VGA Dot Clock frequencies and NTSC modes.
25	FS3	Frequency Select 3. Selects between VGA Dot Clock frequencies and NTSC modes.
26	FS2	Frequency Select 2. Selection between VGA Dot Clock frequencies and NTSC modes.
27	FS1	Frequency Select 1. Selects between VGA Dot Clock frequencies and NTSC modes.
28	FS0	Frequency Select 0. Selects between VGA Dot Clock frequencies and NTSC modes.
29	EXTSYNC	For ICS use only.
30	VCR1	HIGH permits using VCRs as an input.
31	CLAMPLEV	Clamping level adjustment for video input. See Application Notes for more details.
32	Y2	NTSC video input number 2. Note: This is also the Y (luminance) input for S-Video systems.
33	Y1	NTSC video input number 1. Note: This is also the Y (luminance) input for S-Video systems.
34	C2	C (Chrominance) input number 2 for S-Video systems.
35	C1	C (Chrominance) input number 1 for S-Video systems.
36	3.58SC	3.579545 MHz SUBCARRIER OUTPUT. Phase-locked to the chroma burst signal to allow encoders to maintain proper SCH phasing.
37	$\overline{\text{FRSTIN}}$	For ICS use only, wire to pin 15.
38	AVDD	5 Volt analog power. We strongly recommend the use of a multilayer board and a power plane.
39	GFF	Inverts field 1 and field 2 of VGA sync. Normally tied HIGH.
40	VCOLF	VCO LOOP FILTER CIRCUIT. External RC circuit used in VCO circuitry. See Application Notes for component values.
41	SYNCTHRS	Sync threshold adjustment for video input. See Application Notes schematic.
42	VGAO/E	VGA ODD/EVEN FIELD IDENTIFICATION. HIGH indicates odd numbered field, LOW indicates even numbered field.
43	COUT	C (Chrominance) OUTPUT. C output for S-Video systems.
44	$\overline{\text{RST}}$	Chip reset pulse. This to be tied high through a resistor. Do not tie to the computer reset line.
45	YOUT	Y (Luminance) OUTPUT. NTSC video output when the NTSC/SVID input is in the HIGH state. Y output for S-Video systems when the NTSC/SVID input is in the LOW state.
46	$\overline{\text{HALIGNOUT}}$	For ICS use only, wire to pin 62.
47	SYSLF	SYSTEM CLOCK LOOP FILTER CIRCUIT. External RC circuit used in the chroma burst phase locking circuit. See Application Notes for component values.
48	XTALI	14.31818 MHz crystal circuit. See Application Notes for parts specifications and wiring diagrams.
49	XTALO	14.31818 MHz crystal circuit. See Application Notes for parts specifications and wiring diagrams.

PIN NUMBER	NAME	DESCRIPTION
50	AVSS	Analog ground. We strongly recommend the use of a multilayer board and a ground plane.
51	VID1/2	Input selector. High for Y1/C1, Low for Y2/C2.
52	VCOOUT	For ICS use only, do not wire.
53	FILTSEL	For ICS use only, wire to pin 57.
54	DOTCLOCK	Clock signal input for VGA chip.
55	VFF	Inverts field 1 and field 2 of NTSC sync. Normally tied HIGH.
56	$\overline{\text{VCR2}}$	LOW modifies sync characteristics to permit operation with VCR input.
57	VGA/NTSC	Mode identification output signal. HIGH indicates a VGA mode, LOW indicates an NTSC mode.
58	$\overline{\text{BG}}$	BURST GATE PULSE. Negative polarity TTL level signal used by RGB-to-NTSC encoders.
59	LOC/REM IN	For ICS use only, wire to pin 13.
60	VGAHSYNC	VGA HORIZONTAL SYNC. HSYNC signal from VGA chip. See BIOS Interface Manual for programming details.
61	VGAVSYNC	VGA VERTICAL SYNC. VSYNC signal from VGA chip. See BIOS Interface Manual for programming details.
62	$\overline{\text{HALIGNIN}}$	For ICS use only, wire to pin 46.
63	NTSC/SVID	NTSC/S-VIDEO. Selects between NTSC and S-Video output. HIGH=NTSC; Low=S-Video.
64	VS	VERTICAL SYNC. NTSC Vsync output for RGB-to-NTSC encoders. Gated off during VGA modes.
65	4XSC	4 TIMES SUBCARRIER OUTPUT. 14.31818 MHz signal phase-locked to the chroma burst signal.
66	PCLK	PCLK from VGA chip.
67	DATAOUT	TTL level output. This reads data during lines 10-20 and outputs it as a digital signal. For use in time code applications.
68	SCH	SCH PULSE. Positive polarity TTL level signal to distinguish between fields 1 and 3 or 2 and 4. Not necessary for most encoders.

BIOS Programming Example

BIOS support is currently available from Tseng Labs, Oak Technology, Trident Microsystems, S3, and NCR. Other VGA manufacturers have support programs underway. If you use one of these VGA controllers that have completed BIOS support, you can ignore this section. The following information may be helpful to VGA manufacturers and software developers. These tables represent register settings one particular VGA controller. Others are listed in the BIOS Interface Manual. This particular controller does not interlace text modes and uses an 8 x 8 font for modes 0, 1, 2 , 3, and 7. The horizontal registers are adjusted to produce underscan for text modes and overscan for graphics modes.

Horizontal CRTC Registers

CRTC INDEX	CRTC REGISTER	Modes: 00, 01, 04, 05, 0D	Modes: 02, 03, 06, 07, 0E, 0F, 10	Modes: 11, 12, 13
00	HT	35	6B	66
01	HDE	27	4F	4F
02	SHB	2A	53	52
03	EHB	96	8B	87
04	SHR	30	5B	58
05	EHR	92	83	80

Vertical CRTC Registers

CRTC INDEX	CRTC REGISTER	200 Line Modes: (Non-Interlaced) 00, 01, 02, 03, 07, 04, 05, 06, 0D, 0E, 13	350 Line Modes: (Interlaced) 0F, 10	480 Line Modes: (Interlaced) 12, 13
06	VT	05	05	05
07	OVERFLOW	11	11	11
10	VRS	E0	D3	F4
11	VRE	84	87	88
12	VDE	C7	AE	EF
15	SVB	DC	CF	F0
16	EVB	F2	E5	06

Note: The MSB of the MSL register (INDEX 09) must be turned OFF in 200 line NTSC modes. When using an 8 x 8 font for text (modes 00, 01, 02, 03, 07) the 4 LSB of this register will change from F to 7.

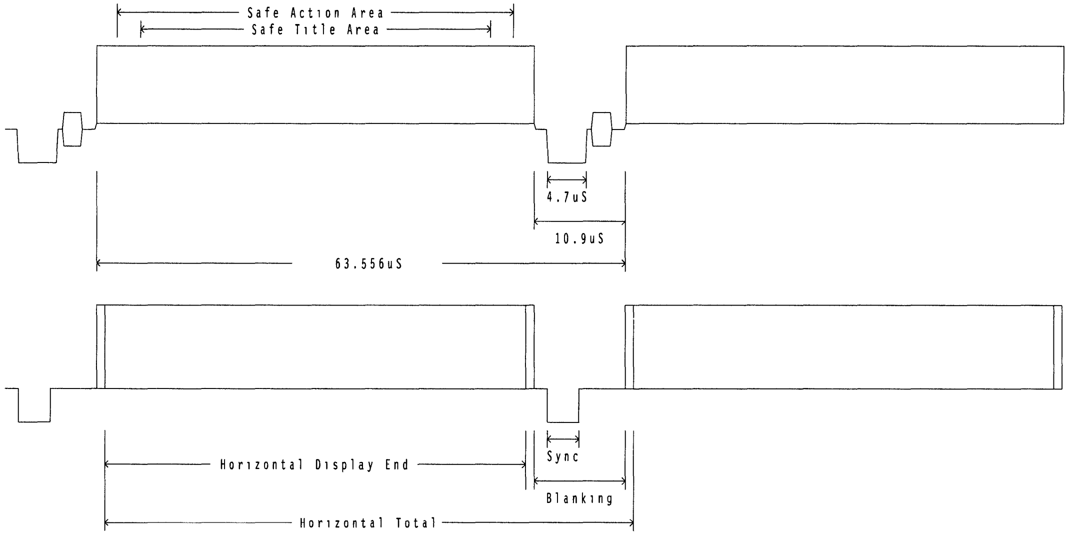
Miscellaneous Output Register

NTSC mode	Color Modes: 00, 01, 02, 03, 04, 05, 06, 0D, 0E, 10, 11, 12, 13	Monochrome Modes: 07, 0F
Genlock (GL)	23	22
Overlay (OV)	27	26
Video Only (VO)	2B	2A
Graphics Only (GO)	2F	2E

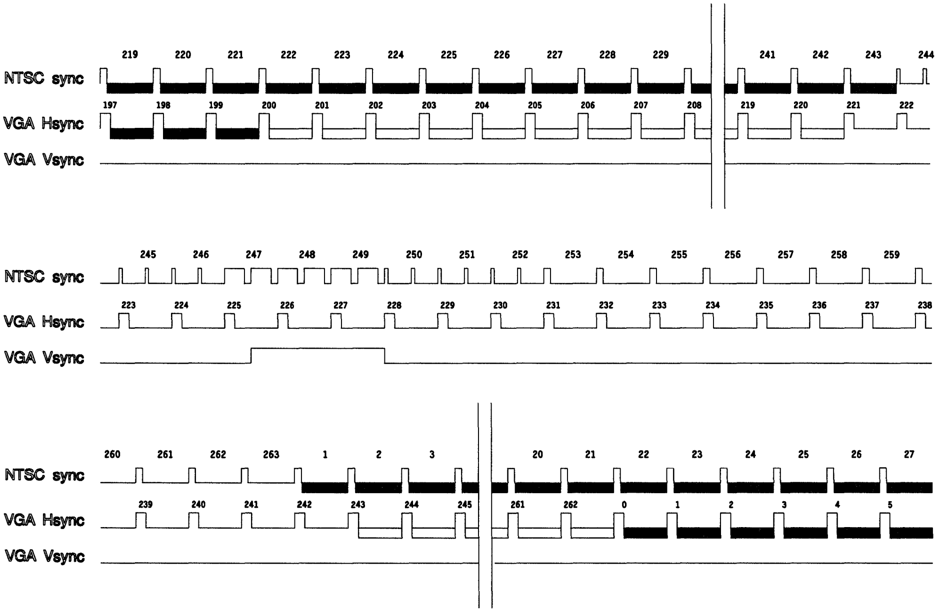
Extended Registers

Turn OFF all DOTCLOCK/2 bits.

NTSC vs VGA Horizontal Timing



NTSC vs VGA Vertical Timing (200 line mode)



Electrical Specifications

Operating temperature range 0°C to 70°C

Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Analog Supply	A_{VDD}	4.5	5.0	5.5	Volts
Digital Supply	D_{VDD}	4.5	5.0	5.5	Volts
Operating Current - VGA Mode	I_{DD} (VGA)		35		mA
Operating Current - NTSC Mode	I_{DD} (NTSC)		50		mA

Input Signals

SIGNAL TITLE	PIN #	TYPICAL VALUE	OPERATING CONDITIONS
Y1	33	1 V_{P-P}	75 Ohm load
C1	35	1V_{P-P}	75 Ohm load
Y2	32	1V_{P-P}	75 Ohm load
C2	34	1V_{P-P}	75 Ohm load
VID1/2	51	TTL/CMOS	High = Y1,C1; Low = Y2,C2
NTSC/SVID	63	TTL/CMOS	High = NTSC; Low = S-Video
VGAVSYNC	61	TTL/CMOS	Positive polarity
VGAHSYNC	60	TTL/CMOS	Positive polarity
FS0-5	28-23	TTL/CMOS	Address/mode select
CKEY	7	TTL/CMOS	High = RGB; Low = NTSC
PCLK	66	TTL/CMOS	Pixel (DAC) Clock from VGA
I/ES	12	TTL/CMOS	High = Internal sync Low = External sync
DATAIN	4	TTL/CMOS	Active during DATAFRAME
CLAMPLEV	31	1-1.5 V	
SYNCTHRS	41	CLAMPLEV +0.1 V	
VLE	1	TTL/CMOS	Tie to V_{DD} through resistor
RST/	44	TTL/CMOS	Tie to V_{DD} through resistor

Output Signals

SIGNAL TITLE	PIN#	TYPICAL VALUE	OPERATING CONDITIONS
VSYNCOUT	9	TTL	Positive polarity during NTSC modes
HSYNCOUT	18	TTL	Composite sync during NTSC modes
VS	64	$1V_{P-P}$	Positive polarity
HS	16	$1V_{P-P}$	Positive polarity
CS	6	$1V_{P-P}$	Positive polarity
DOTCLOCK	54	TTL	
YOUT	45	$1V_{P-P}$	75 Ohm load
COUT	43	$1V_{P-P}$	75 Ohm load
3.58SC	36	TTL	3.579545 MHz
4XSC	65	TTL	14.31818 MHz
LOC/REM	13	TTL	High = local; Low = remote
OVENABLE	11	TTL	High = NTSC; Low = RGB
VGA/NTSC	57	TTL	High = VGA; Low = NTSC
CB	25	TTL	Positive polarity
ODD/EVEN	2	TTL	High = odd field; Low = even field
VGAO/E	42	TTL	High = VGA odd field Low = VGA even field
BG/	58	TTL	Negative polarity
FP/	3	TTL	Negative polarity
SCH	68	TTL	Positive polarity
DATAFRAME	10	TTL	Lines 10-20
DATAOUT	67	TTL	Active during DATAFRAME

Dot Clock Selection

The following charts represent two of the many dot clock frequency selection tables supported by **GSP500**. See the BIOS manual or contact ICS applications engineering for additional information.

FREQUENCY (MHz)	FS5	FS4,FS3,FS2	FS1	FS0
50.350	0	1	0	0
56.644	0	1	0	1
65.028	0	1	1	0
72.000	0	1	1	1
75.000	1	0	0	0
80.000	1	0	0	1
89.800	1	0	1	0
110.000	1	0	1	1
GenLock	1	1	0	0
OVerlay	1	1	0	1
Video Only	1	1	1	0
Graphics Only	1	1	1	1

FREQUENCY (MHz)	FS5,FS3	FS4, FS2	FS1	FS0
25.175	0	1	0	0
28.322	0	1	0	1
40.000	0	1	1	0
44.900	0	1	1	1
GenLock	1	1	0	0
OVerlay	1	1	0	1
Video Only	1	1	1	0
Graphics Only	1	1	1	1

Ordering Information

GSP500V

Example:

ICS XXXX V

Package Type
V=PLCC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device, GSP=Genlock Device

GSP500 Frequently Asked Technical Questions.

1. What will the GSP500 do for me?

The GSP500 adjusts the timing of a VGA controller to conform to RS-170A NTSC (television) specifications. The GSP500 accepts direct video input from video cameras, videodisc players or other video sources and will synchronize (genlock) a VGA controller to either the external video input or an internal NTSC sync generator. The GSP500 also contains a dot clock generator to eliminate the need for crystal oscillators or other dot clock generators.

2. How does the GSP500 differ from other genlock devices?

Other genlock devices, such as the Motorola MC1378, are very effective at genlocking two NTSC signals together and are generally used in consumer electronics products such as video window-in-a-window devices. The GSP500 is specifically designed to genlock a computer graphics controller to NTSC video and overcomes all of the incompatibilities between VGA and NTSC. Additionally, the GSP500 contains an NTSC sync generator and maintains chrominance phase lock in local modes. This allows the GSP500 to maintain RS-170A NTSC timing without an external video input. Furthermore, the sync separator circuit of the GSP500 is designed to satisfy the low jitter tolerances demanded by discriminating VGA customers.

3. Isn't genlock simply a phased-lock loop?

Phase locking two similar signals is fairly straightforward as long as phase jitter is not critical. As an example, ICS is one of the few companies able to successfully build phase-locked loop dot clock generators with low enough phase jitter for computer graphics display. Additionally, the differences between VGA and NTSC signals further complicate the genlock procedure. The GSP500 has patents applied for for the most advanced computer video genlock methods in the industry. These methods assure you of the highest possible quality product.

4. Most Genlock and Overlay products have a lot of discrete components with trimmer capacitors and potentiometers. All these adjustments can become very expensive in a mass production environment. How much external circuitry does the GSP500 require?

Although the GSP500 can be run with no trimmer capacitors or potentiometers, one trimmer capacitor should be used to meet the NTSC frequency tolerance of the chroma burst. This is a free running frequency and is very simple (and fast) to adjust. Additionally, the GSP500 uses high speed digital circuitry to eliminate virtually all discrete components. Only a few external components are needed for full operation.

5. Do I need an RGB-to-NTSC encoder with the GSP500?

Yes, an external RGB-to-NTSC encoder is needed. The encoder must be matched to the target audience. The GSP500 can be used under broadcast television scrutiny and most broadcast video equipment perform the encoding entirely with discrete components. As this may prove too costly and/or may use too much board space, the GSP500 contains all of the necessary signals to drive virtually any encoder. The GSP500's generous supply of timing signals will also drive external circuitry to turn off the encoder for laptop applications.

6. Why do I need the GSP500. Can't I program a VGA controller for NTSC sync and just drive an RGB-to-NTSC encoder?

NTSC sync contains equalizing pulses, blanking signals and pulse widths that are impossible to create under normal VGA control. Although marginal display quality is achievable on a television without adhering to the RS-170A standard, compatibility with other NTSC equipment is compromised. As an example, depending on which edge of horizontal sync the monitor triggers on will determine how far an incorrect width horizontal sync pulse will skew the screen. Additionally, it becomes virtually impossible to assure proper chroma burst (SCH) phasing. The GSP500 sync generator meets or exceeds all NTSC RS-170A broadcast standards for timing accuracy assuring you of maximum compatibility and ultimate quality.

7. National sells a sync separator for less than $2 while the Brooktree part costs over $50. What is the difference and how does the sync separator in the GSP500 compare?

The sync separation circuitry in the National part is a simple diode clamp. Although this may be adequate for driving a picture tube, the lack of noise and jitter immunity make it unsuitable for genlock applications. Additionally, the analog vertical sync detection circuit of these type of devices will not accurately track a VCR signal. The Brooktree device represents a mixed-mode approach to sync separation. By utilizing a fast analog circuitry coupled with high speed digital logic, noise and jitter immunity can be optimized. The GSP500 also uses a mixed mode approach specifically optimized for genlock operation yet the incorporation of a sync generator allows signal analysis not possible with other devices.

8. Is the GSP500 compatible with any VGA controller?

VGA controllers need to have two features to work with the GSP500. First, they need to be able to interlace - if your controller can display 1024 x 768 resolution, then it can probably interlace (the additional 256K memory is not necessary). Second, the controller must have at least three clock select lines for external dot clock generator support. Virtually all current VGA controllers have this feature. Check with your VGA controller manufacturer or ICS if you are unsure.

9. How do I turn the NTSC on and off and control it?

The GSP500 uses the three clock select lines to support 4 VGA clocks and 4 NTSC modes. The VGA clocks are available in 7 different patterns (i.e. 25.175, 28.322, 40.000, 65.000 is one pattern). The 4 NTSC modes are Genlock, Overlay, Graphics Only, and Video Only. The selection between any NTSC mode or between NTSC and VGA is done entirely under BIOS or software control.

10. Why did you incorporate a dot clock generator in the GSP500?

The GSP500 works by modifying the dot clock input for the VGA controller. It essentially is a dot clock generator designed for NTSC genlock. The dot clock generator is not so much of an extra feature as it is a subset of the genlock design. Consequently, this unity design assures you of a reliable glitch-free solution.

11. When the GSP500 displays an Overlay, how do I determine which part of the screen displays graphics and which is VGA?

The GSP500 uses a technique called Color-Key to determine where to display the external video. This Color-Key color is based on the VGA color number. Therefore, no colors are actually lost. As an example, the background color is always Color 0. When Color-Keying on Color 0, the screen will appear to have a background of the external video. The actual color that the VGA assigns to Color 0 does not matter. Any of the 256 color numbers can be assigned to be a Color-Key. Although the GSP500 modifies the Color-Key input, the Color-Key selection is done by an external 8 bit digital compare.

12. Why is the Color-Key selection external to the GSP500?

Color-Key selection is done with an 8 bit compare of the digital RGB signals with a preassigned byte. The digital RGB data comes from the VGA controller and the preassigned byte normally comes from the IBM bus via a port selection. The output of this comparison is fed into the CKEY (Color-Key) input of the GSP500. Although this Color-Key method will satisfy 95% of all customers, the external design allows other schemes with multiple or different comparison options. Additionally, since all of these signals are already available inside the VGA controller, many manufacturers have announced plans to incorporate the Color-Key function inside the VGA controller.

13. What about PAL and/or SECAM compatibility?

ICS is presently working on a PAL version of the GSP500. In its current implementation, it will be pin compatible with the GSP500 but require different values for the discrete components and will also need a different crystal oscillator. Although a SECAM version is technically possible, due to the uncertain market potential product development is not currently underway.

14. Can I look forward to a combination PAL and NTSC product?

Unfortunately, the amount of circuitry common to both a PAL and an NTSC version is minimal. Separate versions are currently the lowest cost solution. Although the crystal frequency, some discrete components and the Bios would have to change, the same board layout could support both standards by simply changing the parts list.

15. Does the GSP500 accept multiple video inputs? What about an S-Video input?

The GSP500 has two independent video inputs. Either input can be used or they can both be disabled. Either input can be wired to accept either S-Video or NTSC. Selection between the two inputs is performed under hardware control.

16. Why doesn't the GSP500 incorporate audio?

The NTSC and S-Video baseband signals do not have a provision for audio. This means that the video and audio signals are completely separate signals at all times. ICS offers audio products for the multimedia market that can be incorporated into the design but allows the designer maximum flexibility by keeping them separate products.

17. Can I use the GSP500 with an RF modulator?

Yes, but the quality of the image may suffer. When NTSC is modulated up to RF frequencies, audio is modulated onto a 4.5 MHz carrier and the video is limited to a maximum frequency of 4.2 MHz. Although 4.2 MHz may be sufficient for moving images it can be limiting for high resolution computer graphics. This problem is magnified because the majority of RF modulators are very low quality devices. Additionally, even if a high quality RF modulation is obtained, the signal may still be degraded by the RF demodulator inside the television set. ICS does recognize the these limitations may be outweighed by the user-friendliness and compatibility of the RF standard. High quality RF modulators are available and the GSP500 does have the necessary signals for support but these issues should be carefully weighed before implementation.

18. Can the GSP500 display NTSC video on my VGA screen?

No, in order to display NTSC video at 31.5 KHz, it is necessary to convert NTSC into component form, digitize it in real time, and store at least one frame of video. Although technology exists to accomplish this, the price-to-performance ratio of these products is too high for mass market acceptance at this time.

19. Is there any question that I forgot to ask?

Yes, when I use a graphics program, I find the borders very distracting yet I need the borders in text modes to insure that I can read the DOS prompt. Can the GSP500 help me with this problem? The GSP500 has the ability to adjust the width of the screen totally under Bios control. This means that you can have limited overscan in mode 13, minor underscan in mode 3 and generous overscan in mode 12. Software drivers can even be written to dynamically change the screen width with the cursor keys.

20. Does this mean I can change the height of the screen also?

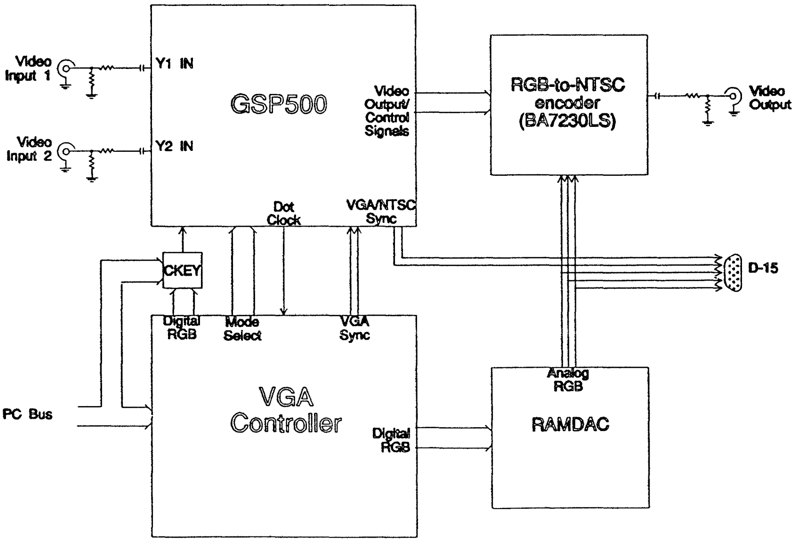
NTSC has a fixed number of lines. In order to change the vertical size, the screen data must be compressed or expanded into fewer or greater lines. This can be accomplished in a text mode by changing the font size or in a graphics mode with linear interpolation. The GSP500 always maintains an exact one-to- one correlation between the NTSC and VGA line position and therefore does not support vertical sizing.

21. Where do I get a development kit for the GSP500?

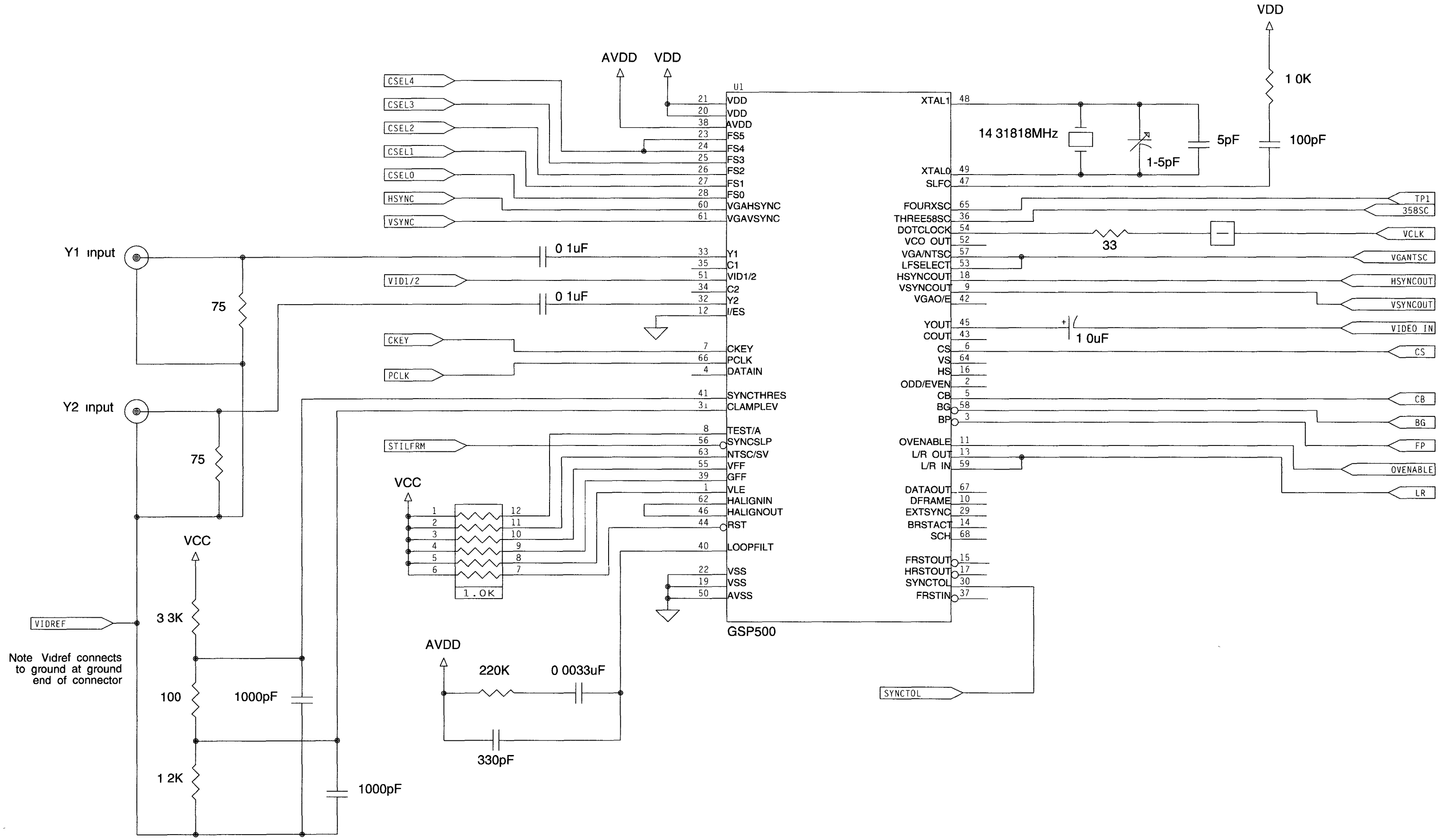
Call ICS at (800) 220-3366 for more information. We will put you in touch with a local rep. who will be more than happy to supply you with a full GSP500 development kit. The ICS full service support organization is always ready to help you with the latest in Multimedia solutions.

Using the GSP500 with a Rohm BA7230LS Encoder

Contents

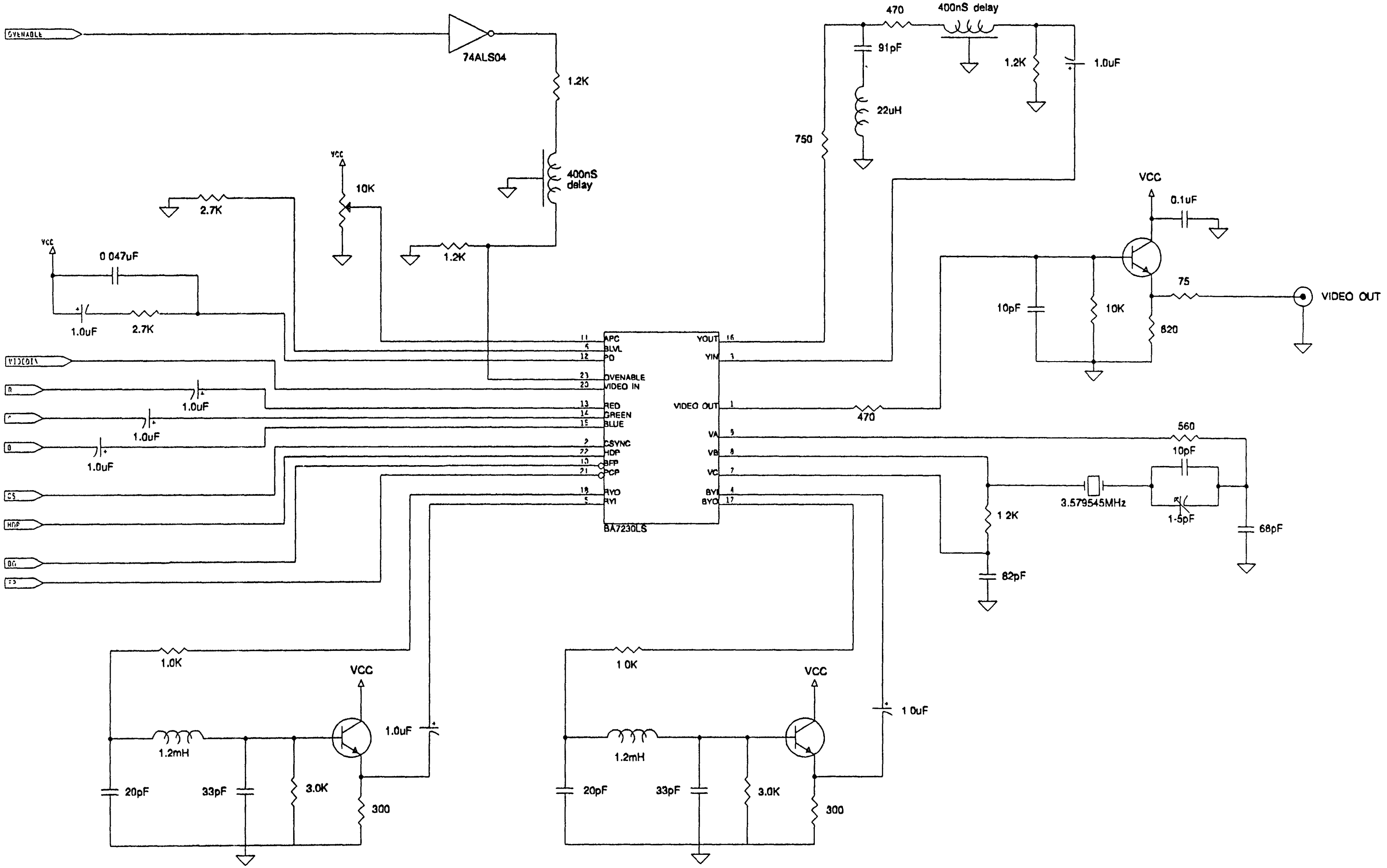


GSP500 Schematic, page 1 of 3: GSP500 Wiring

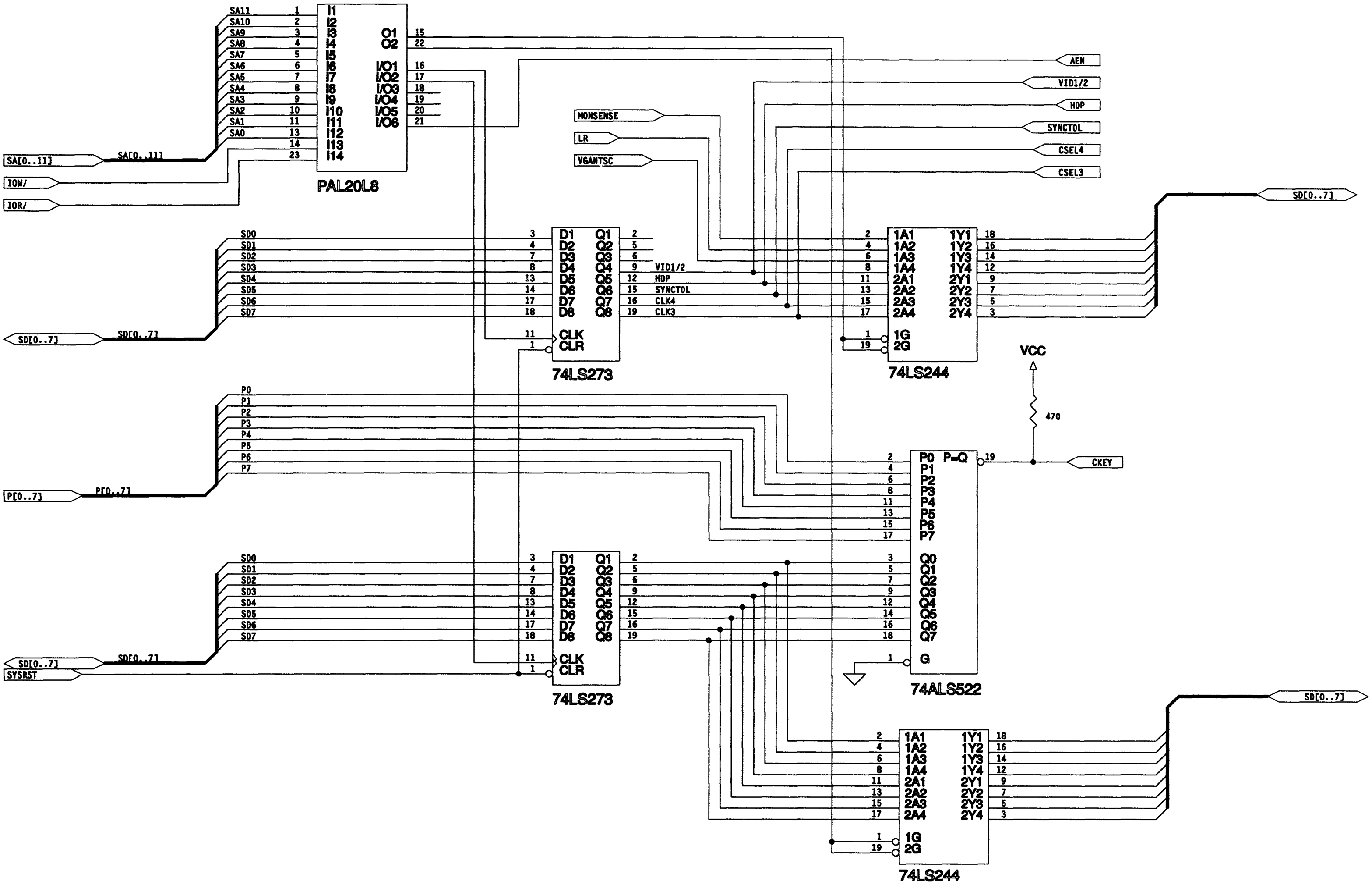


Note Vidref connects to ground at ground end of connector

GSP500 Schematic, page 2 of 3: BA7230LS Wiring



GSP500 Schematic, page 3 of 3: Port Selection Wiring



PAL Equations - Expanded Product terms

HOLD1 = SA11
SA10
!SA9
!SA8
SA7
SA6
SA5

HOLD2 = SA4
SA3
!SA2

R306 = AEN & HOLD1 & HOLD2 & IOR & !IOW & !SA0 & SA1

R307 = AEN & HOLD1 & HOLD2 & IOR & !IOW & SA0 & SA1

W306 = AEN & HOLD1 & HOLD2 & !IOR & IOW & !SA0 & SA1

W307 = AEN & HOLD1 & HOLD2 & !IOR & IOW & SA0 & SA1

AEN.oe = 0

HOLD1.oe = 1

HOLD2.oe = 1

R306.oe = 1

R307.oe = 1

W306.oe = 1

W307.oe = 1

PAL Equations - Symbol Table

Pin Polarity	Variable Name	Ext	Pin	Type	Pterms used	Max Pterms	Min Level
!	AEN		21	V	—	—	—
	HOLD1		18	V	7	7	1
	HOLD2		19	V	3	7	1
!	IOR		23	V	—	—	—
!	IOW		14	V	—	—	—
!	R306		22	V	1	7	1
!	R307		15	V	1	7	1
	SA0		13	V	—	—	—
	SA1		11	V	—	—	—
	SA2		10	V	—	—	—
	SA3		9	V	—	—	—
	SA4		8	V	—	—	—
	SA5		7	V	—	—	—
	SA6		6	V	—	—	—
	SA7		5	V	—	—	—
	SA8		4	V	—	—	—
	SA9		3	V	—	—	—
	SA10		2	V	—	—	—
	SA11		1	V	—	—	—
!	W306		17	V	1	7	1
!	W307		16	V	1	7	1
	AEN	oe	21	D	1	1	0
	HOLD1	oe	18	D	1	1	0
	HOLD2	oe	19	D	1	1	0
	R306	oe	22	D	1	1	0
	R307	oe	15	D	1	1	0
	W306	oe	17	D	1	1	0
	W307	oe	16	D	1	1	0

LEGEND			
	F: field	D: default variable	M: extended node
	N: node	I: intermediate variable	T: function
	V: variable	X: extended variable	U: undefined

Critical Layout Areas

A) **GSP500 VCXO input (pins 48 and 49 of GSP500)**
Keep etches as short as possible. Keep all etches, especially high speed digital, away from circuit area.

B) **GSP500 VCXO loop filter (pin 47 of GSP500)**
Try to keep components near GSP500. Keep all etches, especially high speed digital, away from circuit area.

C) **VCLK dotclock connection (pin 54 of GSP500)**
Keep etch as short as possible. Keep all etches, especially high speed digital, away from connection.

D) **GSP500 VCO loop filter (pin 40 of GSP500)**
Try to keep components near GSP500. Keep all etches, especially high speed digital, away from circuit area.

E) **GSP500 Video input ground connection**
Connect one of the video input jack pins to the ground plane. Connect all VIDREF connections to this point with at least a 20 mil etch. Keep 75 Ohm resistors close to the connectors.

F) **GSP500 Video inputs (pins 32 and 33 of GSP500)**
Try to guard band video inputs to GSP500. Signal etches should be at least 20 mil thick.

G) **Encoder VCXO loop filter (pin 12 of BA7230LS)**
Try to keep components near encoder. Keep all etches, especially high speed digital, away from circuit area.

H) **Luminance delay (pins 16 and 3 of BA7230LS)**
Keep etches as short as possible. Keep all etches, especially high speed digital, away from circuit area.

I) **Encoder VCXO crystal (pins 7 and 8 of BA7230LS)**
Keep etches as short as possible. Keep all etches, especially high speed digital, away from circuit area.

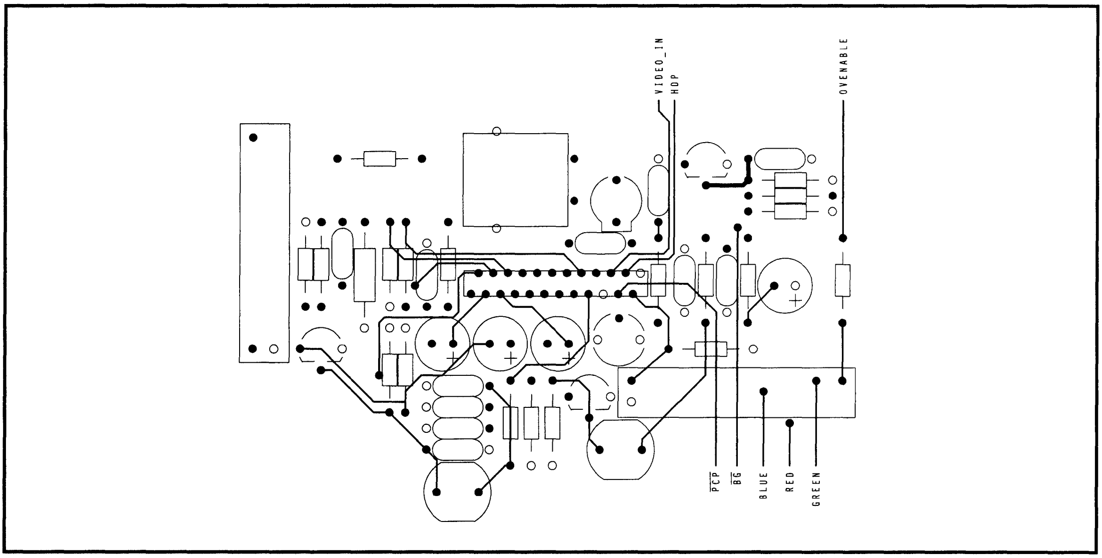
J) **Power supply and loop filter pull-up voltage for GSP500 and encoder (pins 20, 21, 38, 40, and 47 of GSP500, pins 12 and 24 of BA7230LS)**
Regulate all power supply and loop filter voltages.

GSP500 Pin Names

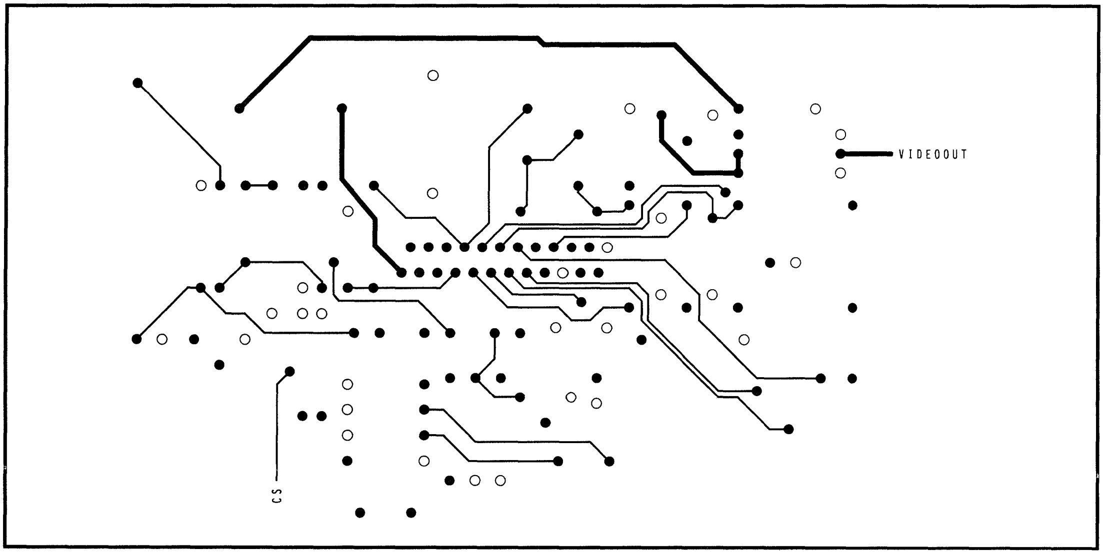
1	VLE	23	FS0	45	YOUT
2	ODD/EVEN	24	FS1	46	HALIGNOUT/
3	FP/	25	FS2	47	SYSLF
4	DATAIN	26	FS3	48	XTALI
5	CB	27	FS4	49	XTALO
6	CS	28	FS5	50	AVSS
7	CKEY	29	EXTSYNC	51	VID1/2
8	TEST	30	SYNCTOL	52	VCOOUT
9	VSYNCOUT	31	CLAMPLEV	53	FILTSEL
10	DATAFRAME	32	Y2	54	DOTCLOCK
11	OVENABLE	33	Y1	55	VFF
12	I/ES	34	C2	56	STILLFRAME
13	L/R OUT	35	C1	57	VGA/NTSC
14	BRSTACT	36	3.58SC	58	BG/
15	FRTSTOUT/	37	FRSTIN	59	L/R IN
16	HS	38	AVDD	60	VGAHSYNC
17	HRSTOUT/	39	GFF	61	VGAVSYNC
18	HSYNCOUT	40	VCOLF	62	HALIGNIN/
19	VSS	41	SYNCTHRS	63	NTSC/SVID
20	VDD	42	VGAO/E	64	VS
21	VDD	43	COUT	65	4XSC
22	VSS	44	RST/	66	PCLK

BA7230LS Pin Names

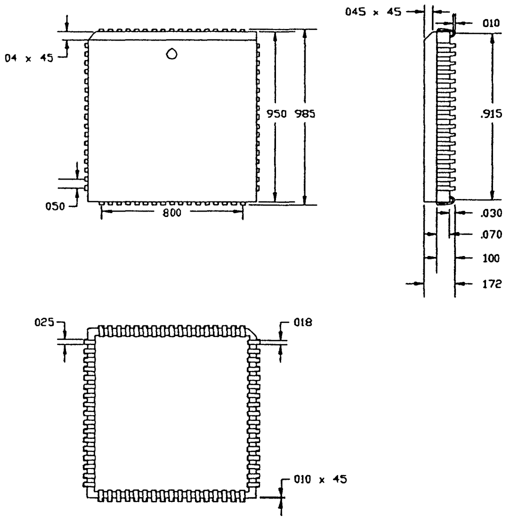
1	VIDEO OUT	13	RED
2	SYNC IN	14	GREEN
3	Y IN	15	BLUE
4	B-Y IN	16	Y OUT
5	R-Y IN	17	B-Y OUT
6	BURST LEVEL ADJ.	18	R-Y OUT
7	VC	19	GND
8	VB	20	VIDEO IN
9	VA	21	PCP IN (FP/)
10	BPF IN (BG/)	22	HDP IN
11	APC PHASE ADJ.	23	YS IN (OVENABLE/)
12	PD	24	VCC



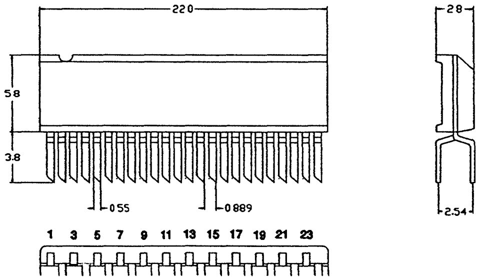
BA7230LS Test Layout
Component Side



BA7230LS Test Layout
Solder Side



GSP500 Physical Specifications
(All dimensions are in inches)



BA7230LS Physical Specifications
(All dimensions are in millimeters)

Adjustment Features

GSP500

Set the **GSP500** for non-NTSC operation(any VGA mode). Adjust the variable capacitor (between pins 48 and 49 of the **GSP500**) until pin 65 of the **GSP500** reads 14.31818 MHz. If you are unable to adjust it far enough, you may have to increase or decrease the size of the capacitor parallel to the variable capacitor.

BA7230LS

Step 1

Adjust the variable resistor (pin 11 of the BA7230LS) until pin 11 reads 3.9 volts DC.

Step 2

Place GSP500 in genlock mode. Attach a vectorscope to the video output connector. Create a colorbar pattern on the computer screen (available from ICS). Adjust the variable capacitor until the vectorscope displays the proper phase.

Sources for Specialized Components

Encoders:

BA7230LS
ROHM Corporation
USA Headquarters
8 Watney
Irvine CA 92718
(714)855-2131 FAX:(714)855-1669

Delay Lines:

H321LNP-1436PBAB (400nsec)
TOKO America, Inc.
Corporate Headquarters
1250 Feehanville Drive
Mount Prospect, IL 60056
(708)297-0070 FAX:(708)699-7864

Inductors:

RC-875/122J-50 (1.2mH)
Sumida Electric Co., Ltd.
USA Head Office
637 East Golf Road
Suite 209
Arlington Heights, IL 60005
(708)956-0666 FAX:(708)956-0702

B230-52 (22uH)
J.W. Miller
306 E. Alondra Blvd.
Gardena, CA 90247-1059
(213)515-1720 FAX:(213)515-1962

Crystals:

143-20 (14.31818 MHz), 036S (3.579545 MHz)
Fox Electronics
5570 Enterprise Parkway
Fort Myers, FL 33905
(813)693-0099 FAX:(813)693-1554

Phono Connectors:

901
Keystone Manufacturers
31-07 20th Road
Astoria, NY 11105-2017
(718)956-8900 FAX:(718)956-9040

Variable Capacitors:

GKG7R011 (2-5pf)
Sprague/Goodman
134 Fulton Ave.
Garden City Pk, NY 11040
(516)746-1385 FAX:(516)746-1396

Potentiometers:

3321+R (10K)
Murata-Erie
2200 Lake Park
Smyrna, GA 30080
(404)436-1300 FAX:(404)436-3030

EVM-SOGA01B14 (10K)
Panasonic
Box 511
Secaucus, NJ 07096
(201)348-5266 FAX:(201)392-4782

Distributors:

Digi-Key
701 Brook Ave South
Thief River Falls, MN 56701
(800)344-4539

Integrated
Circuit
Systems, Inc.

AN502

Application Note

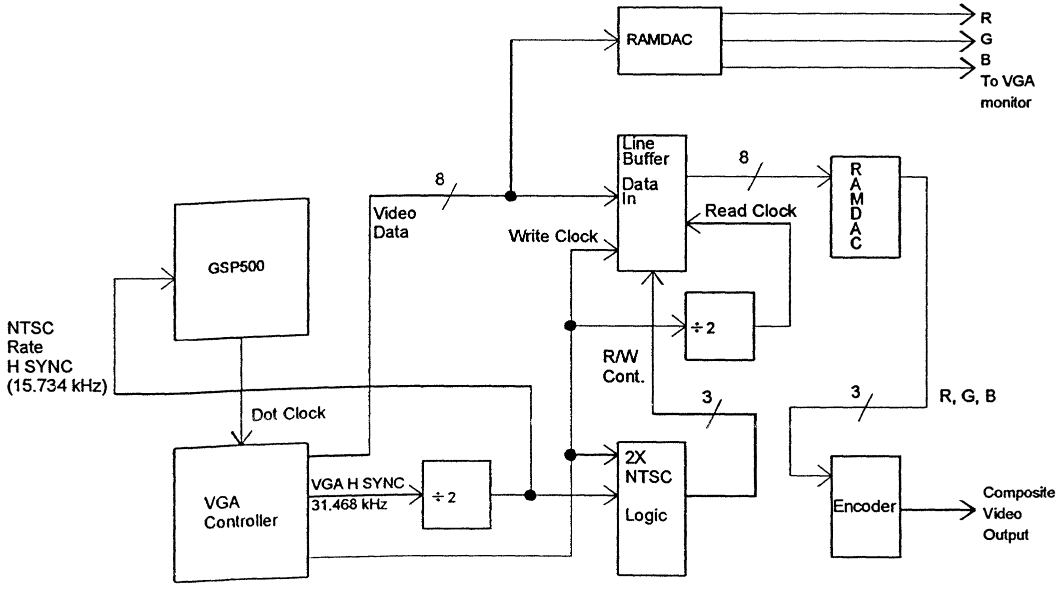
Theory of Operation for a GSP500 Circuit Operating the VGA display at 2xNTSC Frequency

Introduction

In its minimal configuration the GSP500 with a VGA controller chip puts out both RGB to a VGA monitor and composite video in the NTSC format. However, due to the fact that NTSC video is interlaced, the minimal configuration requires that the VGA controller be programmed for interlaced operation; this allows the same RAMDAC to be used for both the VGA and the NTSC outputs (of course the NTSC output also must be encoded). Unfortunately, the VGA picture is somewhat degraded by interlacing - and even worse, some VGA monitors won't lock up to the interlaced signal. If this situation is not acceptable, a solution is available that only requires a few additional parts at minimal cost.

The solution is to run the VGA circuitry at exactly twice the NTSC rate and in a non-interlaced mode. This preserves the full quality of the VGA display while the VGA is still being gen-locked to an external NTSC signal. Of course, now that the VGA RAMDAC is running at a higher speed, another RAMDAC will be required which runs at the NTSC rate. Also, some means will be required to accept the fast data rate VGA output and put out the slower rate NTSC data. Under these circumstances, the VGA circuitry will be producing twice as much data as can be displayed in NTSC and therefore some of it will have to be discarded. All of the VGA lines are used in the NTSC frame, but each line is only used for every other NTSC field. In other words all the odd numbered VGA lines may be output to NTSC field 1 and all the even numbered VGA lines may be output to NTSC field 2 while both odd and even numbered lines are put out to the VGA display in every vertical period. The VGA frame rate is then the same as the NTSC field rate; the NTSC field simply has half as many horizontal lines.

Block Diagram



Application Circuit

One possible implementation of this idea is shown in the accompanying schematic. Only the additional circuitry required for the 2xNTSC enhancement is shown. Following is a detailed description of the operation of the circuit; please refer to the schematic as you read it.

U5B divides the frequency of the VGA HSync signal VHS by two, producing a 50% duty cycle square wave with a frequency of 15.734 kHz. This signal essentially becomes the Write Enable signal at U4 pin 22 and is also sent to the GSP500 pin 60 as the Horizontal Sync signal. Note that the addition of a divide by 2 in the overall loop which the GSP500 controls forces the VGA chip to clock at twice the rate that it otherwise would, producing a VGA HSync frequency of 31.468 kHz.

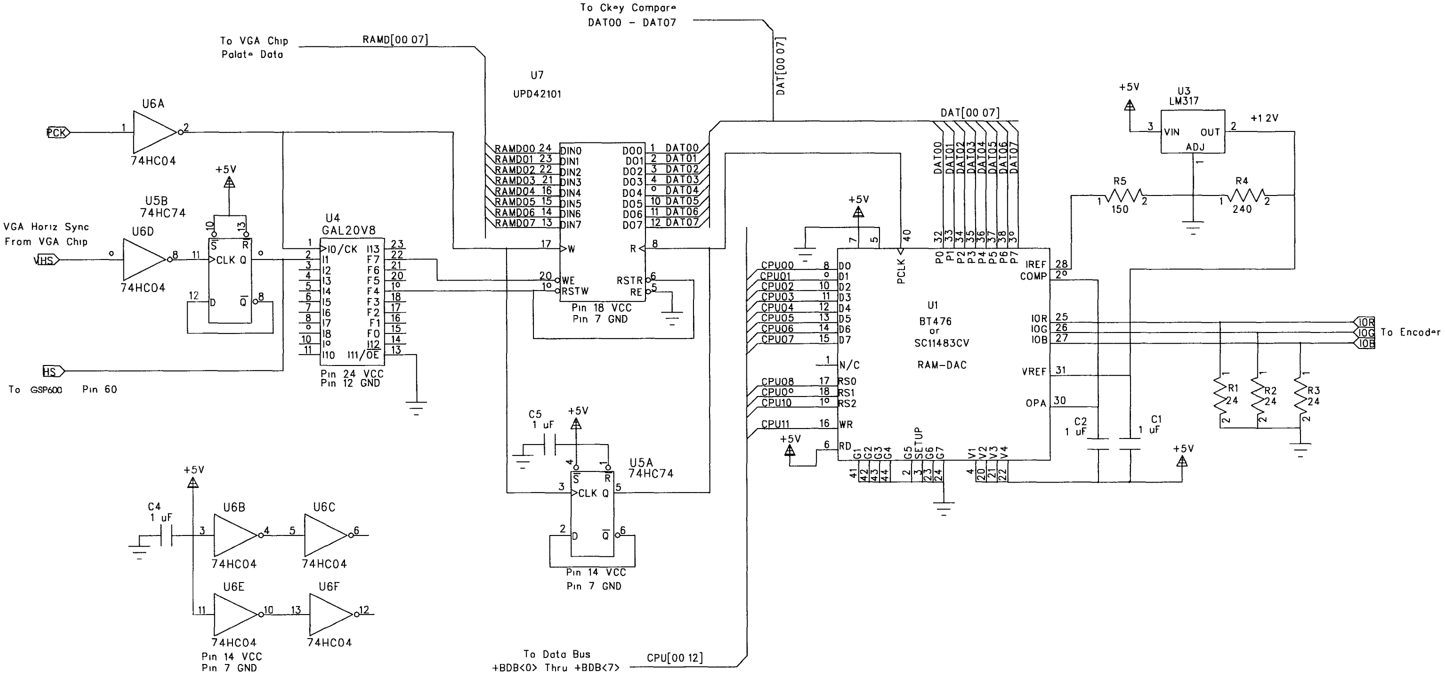
U7 is a line buffer memory which can hold up to 910 pixels with a width of 8 bits; it has individual write and read clocks with associated address pointers. Programmable logic device U4 provides a write enable and pointer reset signals to the line memory. Note that the write clock to U7 (pin 17) is the same rate as the VGA pixel clock; therefore every VGA pixel will be written in to the memory when write enable (pin 20) is active (low). The write enable is only active for every other line, however, since it is frequency divided by 2 from the VGA HSync as previously noted. This essentially discards half the VGA lines each NTSC field, by virtue of the fact that they are not written into memory. The time to write a complete line into memory is 1 VGA line time or 31.778µs. The read clock for U7 is simply the write clock frequency divided by 2 by U5A. Thus to read all the pixels out of the memory will require twice as long as to write them, or 63.557µs. This is the length of an NTSC line. Therefore, over the span of 2 VGA lines, 1 VGA line is written and 1 NTSC line is read, although the writing takes place at twice the NTSC rate.

Data read out from U7 at NTSC rate is fed to RAMDAC U1, which has its control lines paralleled across the main VGA RAMDAC, except that the active low read enable (pin 6) is permanently disabled by tying it to +5V. In this way anything written to the VGA RAMDAC (such as changes to the palette) will also be written to U1, but any reads will not cause a conflict with the main VGA RAMDAC. The analog RGB outputs of U1 are sent to the NTSC encoder to produce a composite video output. U3 provides a reference for the RAMDAC. Instead of a reference for each RAMDAC, it may be possible to use 1 voltage reference for both RAMDACs in the system if they can be configured to use a voltage reference as shown in the schematic.

Further Enhancement

Although the VGA at 2xNTSC enhancement is better than the minimal GSP500 configuration, it is still less than ideal with respect to the NTSC picture quality. It is probably intuitively obvious to most people that throwing away half the VGA data will result in a loss of picture quality on the NTSC output. The practically observed result of this is what is generally known as "flicker," and it should be noted that this problem plagues all scan converters and VGA-to-NTSC boards. It is worst when there is a lot of detail along the vertical axis of the VGA image. The most annoying example is probably a thin, bright white horizontal line made up of a single line on the VGA display. For an example case, imagine that line 100 of the VGA display contains the white line and the rest of the display is black. Then the white line would appear somewhere around line 50 of field 2 in the NTSC output, but not at all on field 1. The result will be a flashing of the line with a period of 33.33 ms (due to 30Hz frame rate). This is visually very noticeable and irritating. Because of this, many scan converters and VGA-to-NTSC boards have a "flicker filter." Interestingly, most flicker filters can be turned off, indicating that they are less than desirable in some situations.

A discussion of flicker filtering and how to implement it with the GSP500 will be the subject of another application note.


To Ckey Compare
DAT00 - DAT07
To VGA Chip
Palate Data
RAMD[00 07]
U7
UPD42101
DAT[00 07]
U6A
74HC04
PCK
+5V
U5B
74HC74
VGA Horiz Sync
From VGA Chip
U6D
74HC04
VHS
U4
GAL20V8
Pin 24 VCC
Pin 12 GND
HS
To GSP600 Pin 60
RAMD00
RAMD01
RAMD02
RAMD03
RAMD04
RAMD05
RAMD06
RAMD07
DIN0
DIN1
DIN2
DIN3
DIN4
DIN5
DIN6
DIN7
DO0
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DAT00
DAT01
DAT02
DAT03
DAT04
DAT05
DAT06
DAT07
W
WE
RSTW
R
RSTR
RE
Pin 18 VCC
Pin 7 GND
U3
LM317
VIN
OUT
ADJ
+12V
R5
150
R4
240
PCLK
P0
P1
P2
P3
P4
P5
P6
P7
CPU00
CPU01
CPU02
CPU03
CPU04
CPU05
CPU06
CPU07
CPU08
CPU09
CPU10
CPU11
D0
D1
D2
D3
D4
D5
D6
D7
N/C
RS0
RS1
RS2
WR
RD
U1
BT476
or
SC11483CV
RAM-DAC
IREF
COMP
IOR
IOG
IOB
VREF
OPA
To Encoder
R1
24
R2
24
R3
24
C2
1 uF
C1
1 uF
G1
G2
G3
G4
G5
SETUP
G6
G7
V1
V2
V3
V4
C5
1 uF
U5A
74HC74
Pin 14 VCC
Pin 7 GND
C4
1 uF
U6B
74HC04
U6C
74HC04
U6E
74HC04
U6F
74HC04
Pin 14 VCC
Pin 7 GND
To Data Bus
+BDB<0> Thru +BDB<7>
CPU[00 12]

CRTC Registers

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	HT	35	35	6B	6B	35	35	62	6C	35	62	62	62	62	62	62	62
01	HDE	27	27	4F	4F	27	27	4F	4F	27	4F	4F	4F	4F	4F	04	4F
02	SHB	2A	28	57	57	2A	2A	50	54	2A	50	50	50	50	50	50	50
03	EHB	95	96	8B	8B	96	96	85	8B	96	85	85	85	84	84	85	84
04	SHR	2E	2E	5D	5D	2F	2F	58	5D	2F	58	58	58	54	57	58	57
05	EHR	A0	A0	8C	8C	80	80	9B	83	80	9B	9B	9B	82	82	9B	82
06	VT	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B
07	OVERFLOW	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E
08	PRS	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
09	MSL	4F	4F	4F	4F	C1	C1	C1	4F	C0	C0	40	40	40	40	C0	40

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
0A	CS	0D	0D	0D	0D	00	00	00	0D	00	00	00	00	00	00	00	00
0B	CE	0E	0E	0E	0E	00	00	00	0E	00	00	00	00	00	00	00	00
0C	SAH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0D	SAL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0E	CLH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0F	CLL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
10	VRS	BE	BE	BE	BE	C5	C5	C5	BE	C5	C5	A7	A7	F4	F4	C5	EF
11	VRE	22	22	22	22	88	88	88	82	88	88	8B	8B	87	87	88	87
12	VDE	8F	8F	8F	8F	8F	8F	8F	8F	8F	8F	5D	5D	DF	DF	8F	DF
13	OFFSET	14	14	28	28	14	14	28	28	14	28	28	28	28	28	28	50
14	UNDERLINE	1F	1F	1F	1F	00	00	00	1F	00	00	0F	0F	00	00	40	60
15	SVB	B8	B8	B8	B8	C2	C2	C2	B8	C2	C2	9F	9F	E0	E0	C2	E0
16	EVB	E3	E3	E3	E3	05	05	05	E3	05	05	CA	CA	0C	0C	05	0C
17	MC	A3	A3	A3	A3	A2	A2	C2	A3	E3	E3	E3	E3	E3	E3	A3	AB
18	LC	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
*	INTERLACE																

* = Interlace Bit must be turned off for all modes

General Register

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	MISC OUT	#	#	#	#	#	#	#	@	#	#	@	#	#	#	#	#

#	@
23 = GenLock (GL)	22 = GenLock (GL)
27 = OVerlay (OV)	26 = OVerlay (OV)
2B = Video Only (VO)	2A = Video Only (VO)
2F = Graphics Only (GO)	2E = Graphics Only (GO)

Sequence Registers

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	CLK MODE	09	09	01	01	09	09	01	00	09	01	01	01	01	01	01	01

** = 640 x 480 x 256 colors

Source Code for PLD U4 (GAL20V8) in CUPL™ Language

```
Name        2ntsc;
Partno      XXXXX;
Date        12/07/92  02:12pm;
Revision    02;
Designer    Todd K. Moyer;
Company     Integrated Circuit Systems;
Assembly    XXXXX;
Location    XXXXX;

/***********************************************************************/
/*                                                                     */
/* VGA @ 2xNTSC rate controller                                        */
/*                                                                     */
/*                                                                     */
/***********************************************************************/
/*                                                                     */
/* Allowable Target Device Types:  g20v8                                              */
/*                                                                     */
/***********************************************************************/

/** Inputs **/

Pin 1         =    clock         ;     /* VGA p-clock                  */
Pin 2         =    h_sync_NTSC ;       /*                              */

Pin 12        =    GND           ;
Pin 13        =    !OE           ;
Pin 24        =    VCC           ;

/** Outputs **/

Pin [15..18]  =    [HSN_S0..3];        /* used by state machine        */
Pin 19        =    !line_start;        /* pointer reset line mem, act lo */
Pin 20        =    !write_enable_B;    /* not used by 2xNTSC           */
Pin 21        =    !write_enable_A;    /* not used by 2xNTSC           */
Pin 22        =    !write_enable;      /*                              */

/** Declarations and Intermediate Variable Definitions **/

Field    State_HSync          = [HSN_S0..3];

/** Logic Equations **/
```

```
/** State machine definition **/

Sequence State_HSync
{
      present 0
                  if h_sync_NTSC next 1
                          out line_start out line_startAB
                          out write_enable out write_enable_A;
                  if !h_sync_NTSC next 0
                          out write_enable;
      present 1
                  if h_sync_NTSC next 2
                          out line_start out line_startAB
                          out write_enable out write_enable_A;
                  if !h_sync_NTSC next 0;
      present 2
                  if h_sync_NTSC next 3
                          out line_start out line_startAB
                          out write_enable out write_enable_A;
                  if !h_synch_NTSC next 0;
      present 3
                  if !h_sync_NTSC next 4;
                          /* out write_enable; */
                  if h_sync_NTSC next 3
                          out write_enable_A;
      present 4
                  if !h_sync_NTSC next A;
                  if h_sync_NTSC next 3;
      present A
                  if !h_sync_NTSC next 5;
                  if h_sync_NTSC next 3;
      present 5
                  if h_sync_NTSC next 6
                          out line_start out line_startAB
                          out write_enable out write_enable_B;
                  if !h_sync_NTSC next 5
                          out write_enable;
      present 6
                  if h_sync_NTSC next 7
                          out line_start out line_startAB
                          out write_enable out write_enable_B;
                  if !h_sync_NTSC next 5;
      present 7
                  if h_sync_NTSC next 8
                          out line_start out line_startAB
                          out write_enable out write_enable_B;
                  if !h_sync_NTSC next 5;
      present 8
                  if !h_sync_NTSC next 9;
                          /* out write_enable; */
                  if h_sync_NTSC next 8
                  out write_enable_B;
```

```
        present 9
                        if !h_sync_NTSC next B;
                        if h_sync_NTSC next 8;
        present B
                        if !h_sync_NTSC next 0;
                        if h_sync_NTSC next 8;

        present C
                        next 0;
        present D
                        next 0;
        present E
                        next 0;
        present F
                        next 0;
}
```

Bill of Materials for 2xNTSC

Item	Qty	Part Name	Description	Manufacturer
1	1	74HC04	HEX INVERTER	Motorola
2	1	74HC74	DUAL D FLIP FLOP	Motorola
3	1	SC11483CV	RAM-DAC	Sierra
4	1	GAL20V8	PLD	Lattice
5	1	LM317	Adjustable Regulator	National
6	1	UPD42101	910x8 FIFO	NEC
7	7	CAP	.1µF Cap	
8	1	R1/4W	240 ohm	
9	1	R1/4W	150 ohm	
10	3	R1/4W	24 ohm	

Integrated
Circuit
Systems, Inc.

AN503

Application Note

Flicker Reduction Circuit for use with the GSP500

Introduction

Although a minimal configuration GSP500 VGA/NTSC system uses all of the lines of the graphics image to generate the NTSC picture, the resulting NTSC display is not (and cannot be) as good as the original VGA display. Despite the fact that all the lines are used, on the standard non-interlaced VGA display *every* line is used for *every* vertical period of about 16.7 ms, while it takes twice as long to put out all the lines to the NTSC picture (33.33 ms). This is accomplished in practice by one of two ways: 1) interlacing the VGA (slowing it down to NTSC rates), or 2) using odd numbered lines for odd NTSC fields and even numbered lines for even fields, essentially discarding half the lines that are output from the VGA (see the Application Note, AN502: *Theory of Operation for a GSP500 Circuit Operating the VGA Display at 2 x NTSC Frequency*). It is probably intuitively obvious that either slowing the VGA down or throwing away half the VGA data will result in the NTSC output looking less pleasing than the standard VGA display. The practically observed result of this is what is generally known as "flicker," and it should be noted that this problem plagues all scan converters and VGA-to-NTSC boards; it is a fundamental limitation of the NTSC standard. It is worst when there is a lot of detail along the vertical axis of the VGA image. The most annoying example is a thin, bright white horizontal line made up of a single line on the VGA display. For an example case, imagine that line 100 of the VGA display contains the white line and the rest of the display is black. Then the white line would appear somewhere around line 50 of field 2 in the NTSC output, but not at all on field 1. The result will be a flashing of the line with a period of 33.33 ms (reciprocal of the 30 Hz frame rate). This is very noticeable and quite irritating to the eye.

Knowing that displaying a VGA image on an NTSC monitor is at best a compromise, we would at least like to achieve the best possible performance from the conversion. Because of this, most scan converters and VGA-to-NTSC boards have a "flicker filter." It is enlightening to note that most flicker filters can be turned off, indicating that they are less than desirable in some situations. In fact, they reduce the spatial "bandwidth" in the vertical direction, or in other words reduce the vertical resolution. A particularly simple and effective flicker reduction scheme (which can be implemented in software) is to repeat every other VGA line in both fields of the NTSC signal. This method, however, requires that half the VGA lines never get to the NTSC display; in other words the vertical resolution is cut in half.

A single horizontal line in the VGA image has only a 50/50 chance of being displayed in NTSC, depending on which line number it appears on. Obviously, this method leaves a lot to be desired, since some details in the VGA image can be completely absent from the NTSC signal; most people would judge it unacceptable.

You can get a feel for how a better typical flicker filter works by thinking about the example above of a single white horizontal line on scan line 50 of field 2. Imagine "spreading" the line so that some of it spills into the scan lines adjacent to the original line. In an interlaced system such as NTSC this means reducing the brightness of line 50 of field 2 (thereby making it gray), and putting some darker shade of gray into lines 50 and 51 of field 1, which are above and below line 50 of field 2, respectively, once the complete frame has been scanned. If done properly, in the right proportions, and viewed from a sufficient distance, the new wide line looks to be of the same brightness as the original single white line. This can significantly reduce the flicker, since there is no longer the situation of black on field 1 and white on field 2 rapidly alternating. However, as you can imagine, any rapid vertical transitions would also become smeared or blurred with such a scheme. The typical complaint is that when trying to display text on an NTSC display, a flicker filter will make the text less readable (if it remains readable at all). This type of flicker reduction works best if only the luminance portion of the signal is filtered, since the mixing of several VGA lines to make one NTSC line can significantly change the saturation and hue of the color displayed, seriously altering the picture when compared with the VGA display. It is primarily changes in luminance level that cause flicker, so that leaving the chrominance portion of the signal unchanged does not seriously degrade the flicker reduction that is achieved, while it does tend to preserve the look of the image.

To boil all this down, there is a trade-off between flicker reduction and vertical resolution, and it bears repeating that it is a practical impossibility to make an NTSC image look just as good as a high resolution VGA image. To try and work around this trade-off, some sophisticated flicker filters are "adaptive," which essentially means that they will dynamically turn themselves on when especially needed to reduce flicker and off when the loss of vertical resolution is especially detrimental. Predictably, this approach is rather expensive and takes up a lot of circuit board space, at least until the time when this function is incorporated into a monolithic integrated circuit. At any rate, a flicker filter of the more basic variety is presented here for use with GSP500 applications.

Application Circuit

In the accompanying schematic and block diagram an implementation of a simple luminance-only flicker filter which works with the **GSP500** in a VGA-to-NTSC system is shown. The schematic details only the portion of the system specific to the flicker filter function, since the VGA portion will vary depending on the VGA chip used. Please refer to the schematic when reading the following detailed circuit description.

U8B divides the frequency of the **VGA_HSYNC** signal **VHS** by two, producing a 50% duty cycle square wave with a frequency of 15.734 kHz. This signal essentially becomes the Write Enable signal at U5 pin 22 and is also sent to the GSP500 pin 60 as the Horizontal Sync signal **NTSC_RATE_HS**. Note that the addition of a divide by 2 in the overall loop which the GSP500 controls forces the VGA chip to clock at twice the rate that it otherwise would, producing a VGA HSync frequency of 31.468 kHz.

U2 is a line buffer memory which can hold up to 910 pixels with a width of 8 bits; it has individual write and read clocks with associated address pointers. Programmable logic device **U5** provides a write enable and pointer reset signals to the line memory. Note that the write clock to U2 (pin 17) is the same rate as the VGA pixel clock; therefore, every VGA pixel will be written in to the memory when write enable (pin 20) is active (low). The write enable is only active for every other line, however, since it is frequency divided by 2 from the VGA HSync as previously noted. This essentially discards half the VGA lines each NTSC field, by virtue of the fact that they are not written into memory. The time to write a complete line into memory is 1 VGA line time or **31.778μs**. The read clock for U2 is simply the write clock frequency divided by 2 by U8A. Thus, to read all the pixels out of the memory will require twice as long as to write them, or **63.557μs**. This is the length of an NTSC line. Therefore, over the span of 2 VGA lines, 1 VGA line is written and 1 NTSC line is read, although the writing takes place at twice the rate.

Data read out from U2 at NTSC rate is fed to RAMDAC U9, which has its control lines paralleled across the main VGA RAMDAC, except that the active low read enable (pin 6) is permanently disabled by tying it to +5V. In this way anything written to the VGA RAMDAC (such as changes to the palette) will also be written to U9, but any reads will not cause a conflict with the main VGA RAMDAC. The analog RGB outputs of U9 are sent to the NTSC encoder to produce the chrominance component of the composite video output. U6 provides the required voltage reference to U9. Also, the RGB outputs from U9 are combined by resistor matrix in the right proportions to create a luminance signal which can be summed with the adjacent lines' luminance signals, thereby spatially lowpass filtering the luminance signal in the vertical dimension.

Up to this point the circuitry described is basically the same as is required to make the VGA run at 2 x NTSC rates (see the Application Note AN502: *Theory of Operation for a GSP500 Circuit Operating the VGA Display at 2 x NTSC Frequency*). Note that there are an additional 2 line buffers (U3 and U4), 2 RAMDACs (U10 and U1), and 2 current references (U7A, Q1, and Q2). The additional 2 line buffers store the VGA lines before and after the current line being output via U2 and U9. The RGB current outputs from the RAMDACs U10 and U1 are connected together, summing the two sets of RGB currents together. The combined RGB signals from U10 and U1 are then matrixed together in the proper proportions to produce an adjacent-lines luminance signal. This signal amplitude is independent of the main luminance signal so that the ratio of adjacent line to main line luminance can be set to any desired value, primarily by adjusting R1, which controls the reference currents into U10 and U1.

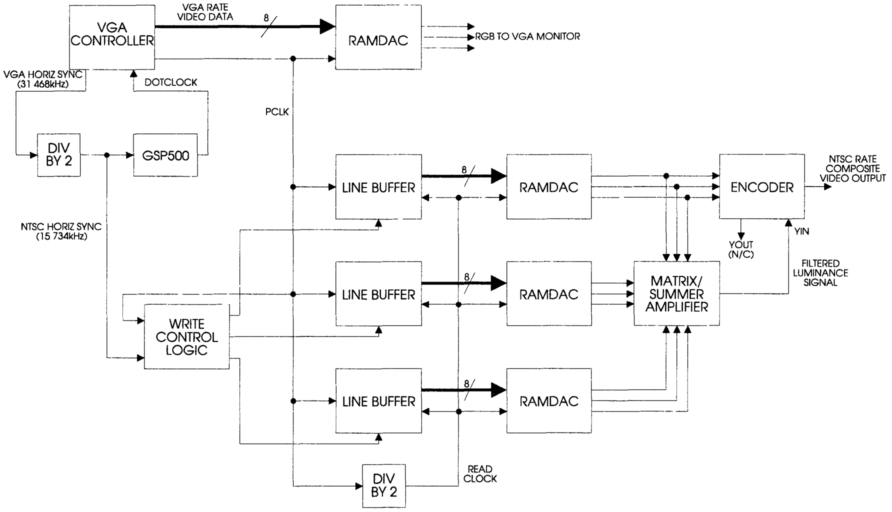


Figure 1

The two luminance signals are connected together, summing them at the input to amplifier U11. U11 then makes up for the resistive losses in the RGB matrices and drives the luminance delay line, whose output is the luminance component of the encoded composite signal. Most encoders have a luminance output and input which allows for an external delay line; not using the output provided while driving the input with an alternate luminance signal of the right amplitude, delay, and polarity allows convenient summing with the chrominance signal generated by the encoder to create the composite video signal.

Programmable logic chip U5 controls the writing of VGA lines into the line buffers such that U2 receives every other line, U3 receives every fourth line, and U4 receives every fourth line, as shown by the timing diagram in Figure 2. Note that only one line buffer is write enabled at a time and every line is written to a line buffer. With this scheme U2 always contains the main VGA line which is going out to the NTSC encoder, while U3 and U4 contain the lines adjacent to the main line. The CUPL™ language source code for PLD U5 is included later in this note.

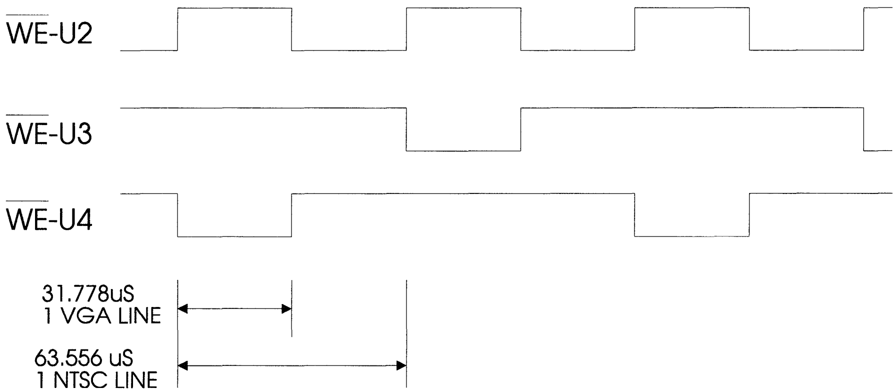


Figure 2

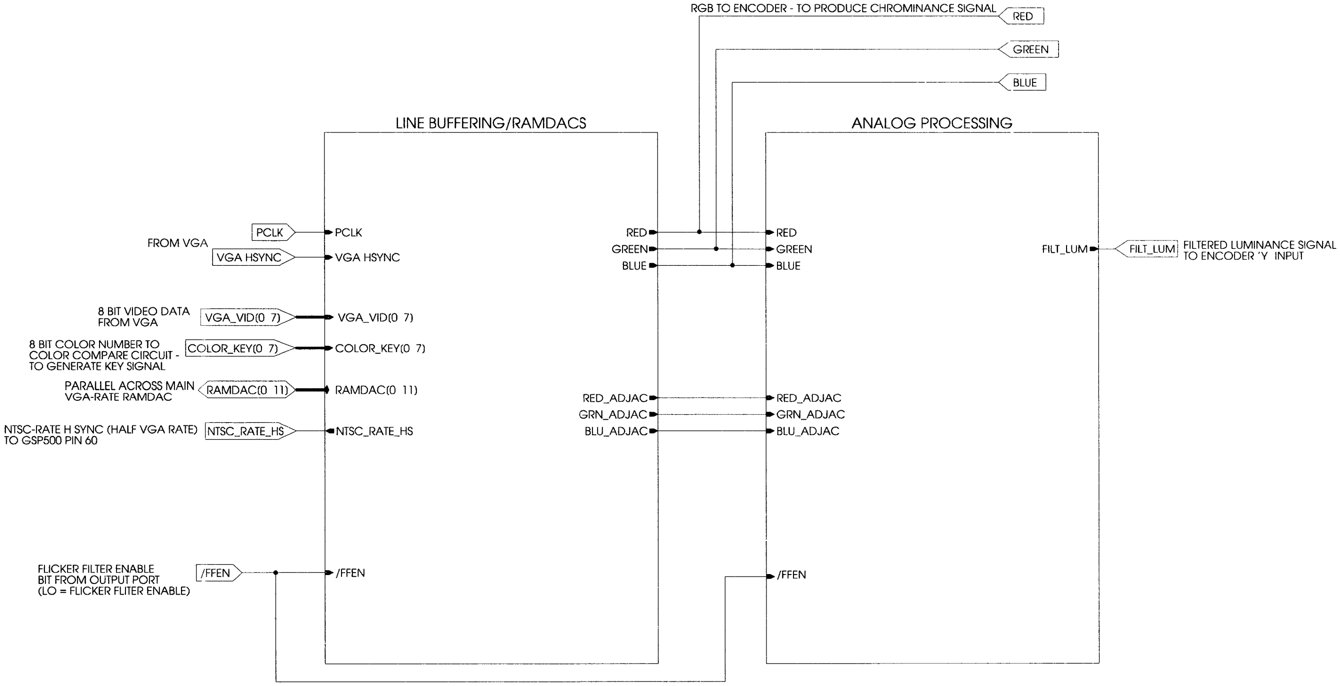
All of the line buffers are continuously read enabled, such that the RGB signal output to the encoder is a combination of the main line and the 2 adjacent line signals. U7A, Q1, and Q2 make up a dual matched current reference for RAMDACs U10 and U1. The amplitude of the adjacent line video signals summed in with the main line is adjustable with R1; the optimum value could be determined so that R1 could be replaced with a fixed divider to save the cost of the trimmer. The amplitude of the main line video signal is controllable by the value of R6 if it is necessary to adjust the proportion of the main line signal that gets summed into the final output. The relative weight of the 2 adjacent line signals in the output is the same due to the matching of the current references into U10 and U1; this should be best for most applications since it is symmetrical about the main line.

The luminance amplitude is controllable by varying the gain of U11 (set by the value of R22); this should normally be set so that luminance levels on any given line are somewhat lower than they would be without filtering. An optional feature shown in the schematic is the ability to switch off the flicker filtering with an I/O bit. Switches Q3 and Q4 turn on when the filter is disabled. In this state Q3 cuts the reference current into U10 and U1, thereby turning off the adjacent line luminance; while Q4 boosts the gain of U11 (by an amount set by R23) to what it should normally be without flicker reduction.

Since when a large area of high luminance level occurs, the video output could exceed the maximum allowed voltage, Q5 and Q6 are used as a positive luminance peak clipper. R27 can be set so that the peak luminance level at the final video output is 714 mV.

BIOS

The video BIOS for the circuit presented here will have to be modified from the typical GSP500 VGA/NTSC system; therefore, register setups for various video modes are given in several tables later in this note.



Flicker Filter Circuit for GSP500

Figure 3 - Flicker Filter Top Level Schematic

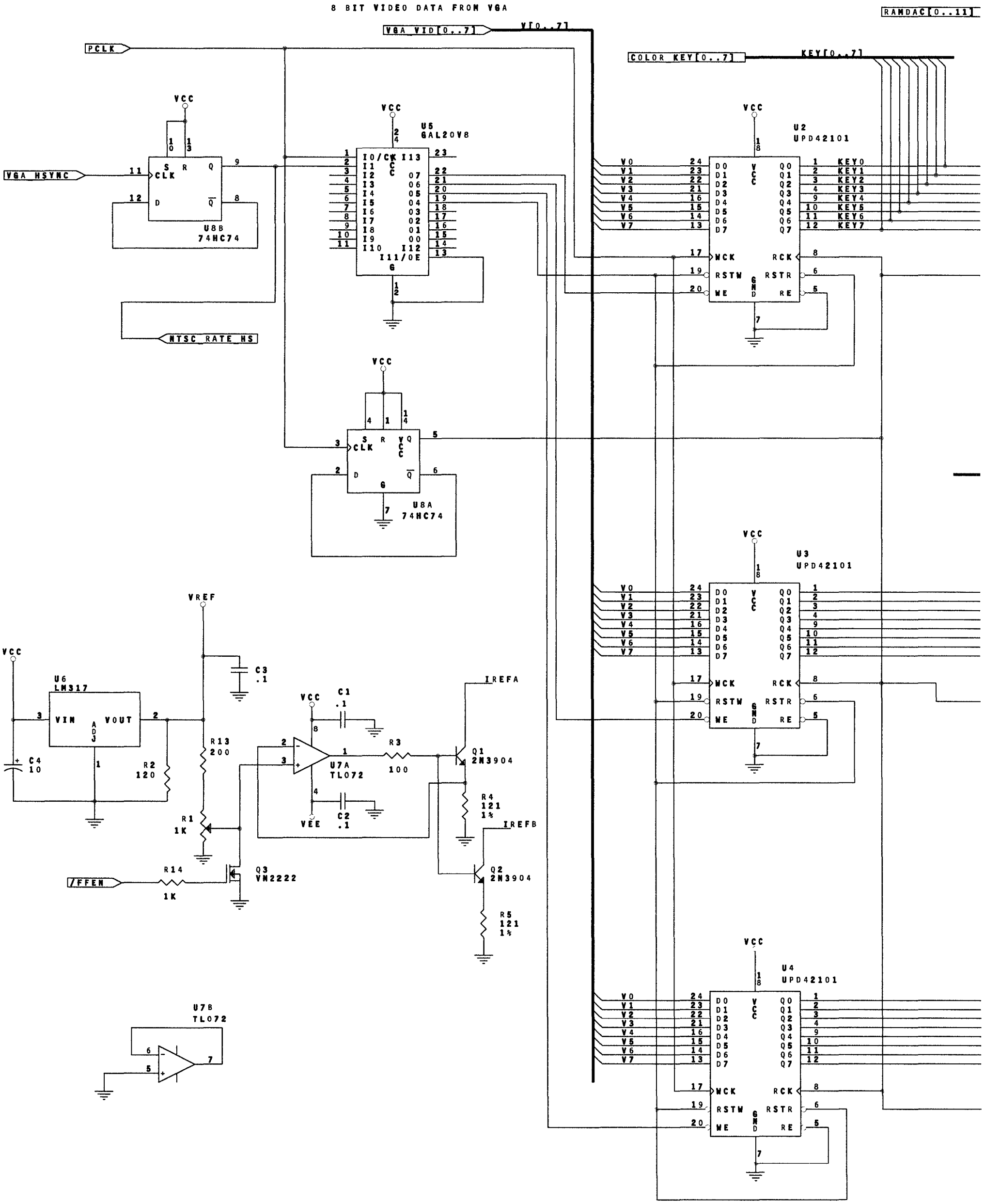
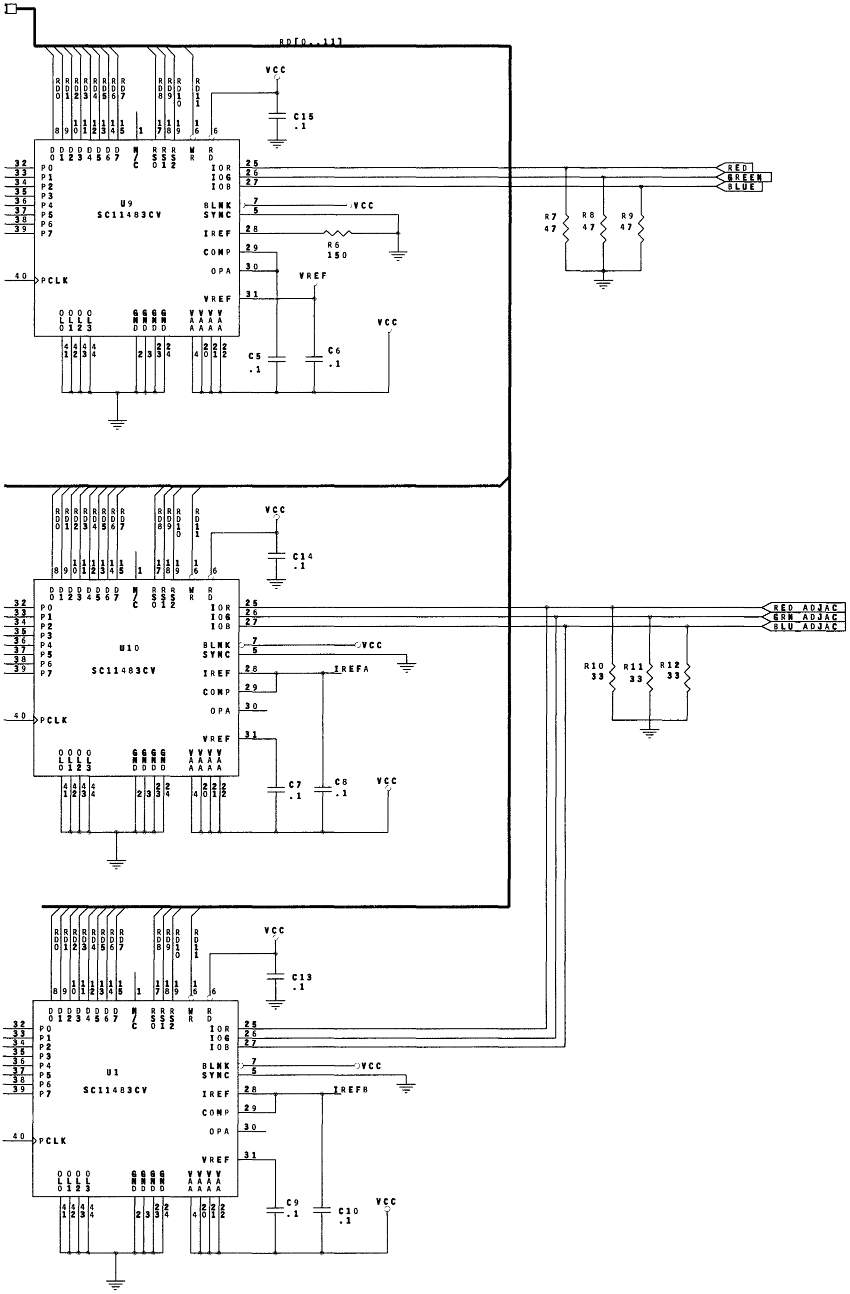
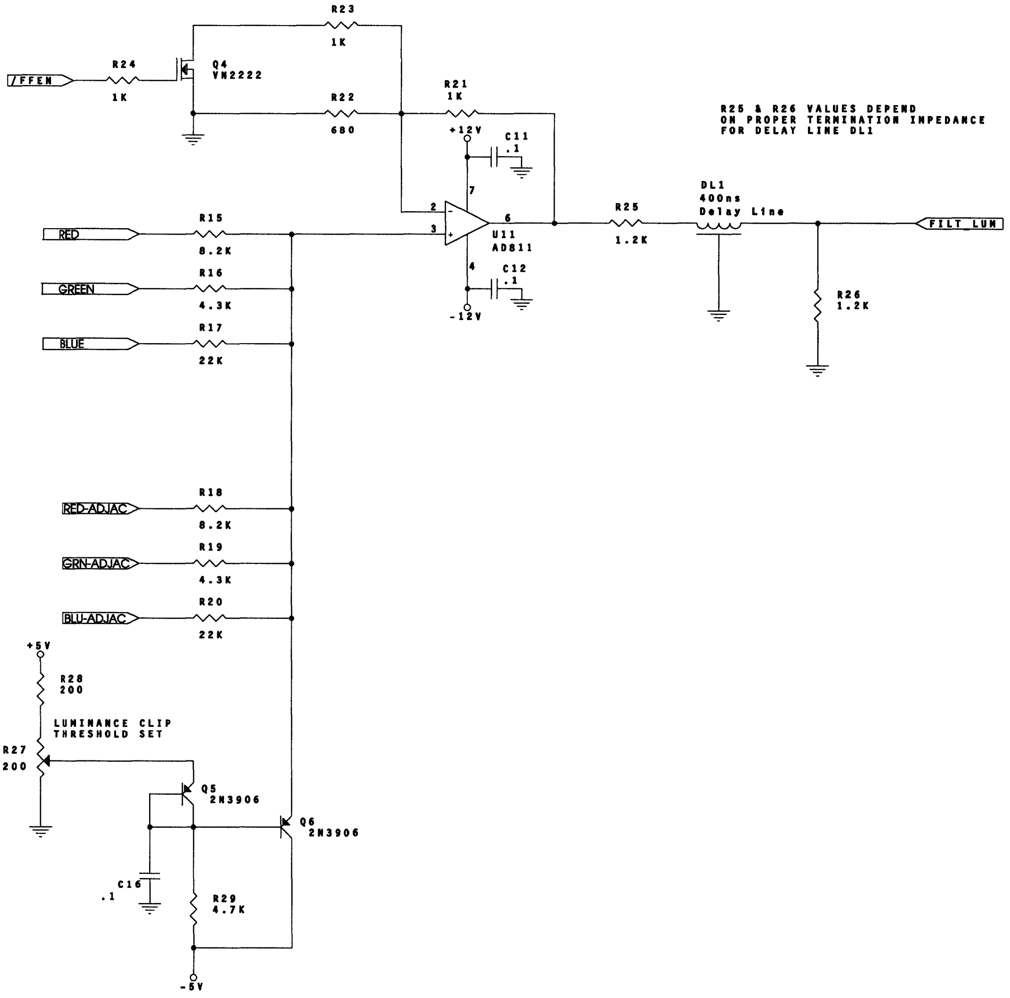

8 BIT VIDEO DATA FROM VGA
VGA_VID[0..7]
V[0..7]
RAMDAC[0..11]
COLOR_KEY[0..7]
KEY[0..7]
PCLK
VGA_HSYNC
NTSC_RATE_HS
VCC
U8B
74HC74
U5
GAL20V8
U8A
74HC74
U2
UPD42101
U3
UPD42101
U4
UPD42101
V0
V1
V2
V3
V4
V5
V6
V7
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
KEY0
KEY1
KEY2
KEY3
KEY4
KEY5
KEY6
KEY7
WCK
RSTW
WE
RCK
RSTR
RE
GND
CLK
IO/CK
I11/OE
VREF
U6
LM317
VIN
VOUT
ADJ
C4
10
R2
120
C3
.1
R13
200
R1
1K
C1
.1
C2
.1
VEE
U7A
TL072
R3
100
Q1
2N3904
IREFA
R4
121
1%
IREFB
Q2
2N3904
R5
121
1%
/FFEN
R14
1K
Q3
VN2222
U7B
TL072

Figure 4 -



Flicker Filter Line Buffering/Ramdacs



R25 & R26 VALUES DEPEND
ON PROPER TERMINATION IMPEDANCE
FOR DELAY LINE DL1

Figure 5 - Flicker Filter Analog Processing

CRTC Registers

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	HT	35	35	6B	6B	35	35	62	6C	35	62	62	62	62	62	62	62
01	HDE	27	27	4F	4F	27	27	4F	4F	27	4F	4F	4F	4F	4F	04	4F
02	SHB	2A	28	57	57	2A	2A	50	54	2A	50	50	50	50	50	50	50
03	EHB	95	96	8B	8B	96	96	85	8B	96	85	85	85	84	84	85	84
04	SHR	2E	2E	5D	5D	2F	2F	58	5D	2F	58	58	58	54	57	58	57
05	EHR	A0	A0	8C	8C	80	80	9B	83	80	9B	9B	9B	82	82	9B	82
06	VT	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B
07	OVERFLOW	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E
08	PRS	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
09	MSL	4F	4F	4F	4F	C1	C1	C1	4F	C0	C0	40	40	40	40	C0	40

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
0A	CS	0D	0D	0D	0D	00	00	00	0D	00	00	00	00	00	00	00	00
0B	CE	0E	0E	0E	0E	00	00	00	0E	00	00	00	00	00	00	00	00
0C	SAH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0D	SAL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0E	CLH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0F	CLL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
10	VRS	BE	BE	BE	BE	C5	C5	C5	BE	C5	C5	A7	A7	F4	F4	C5	EF
11	VRE	22	22	22	22	88	88	88	82	88	88	8B	8B	87	87	88	87
12	VDE	8F	8F	8F	8F	8F	8F	8F	8F	8F	8F	5D	5D	DF	DF	8F	DF
13	OFFSET	14	14	28	28	14	14	28	28	14	28	28	28	28	28	28	50
14	UNDERLINE	1F	1F	1F	1F	00	00	00	1F	00	00	0F	0F	00	00	40	60
15	SVB	B8	B8	B8	B8	C2	C2	C2	B8	C2	C2	9F	9F	E0	E0	C2	E0
16	EVB	E3	E3	E3	E3	05	05	05	E3	05	05	CA	CA	0C	0C	05	0C
17	MC	A3	A3	A3	A3	A2	A2	C2	A3	E3	E3	E3	E3	E3	E3	A3	AB
18	LC	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
*	INTERLACE																

* = Interlace Bit must be turned off for all modes

General Register

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	MISC OUT	#	#	#	#	#	#	#	@	#	#	@	#	#	#	#	#

#	@
23 = GenLock (GL)	22 = GenLock (GL)
27 = OVerlay (OV)	26 = OVerlay (OV)
2B = Video Only (VO)	2A = Video Only (VO)
2F = Graphics Only (GO)	2E = Graphics Only (GO)

Sequence Registers

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	CLK MODE	09	09	01	01	09	09	01	00	09	01	01	01	01	01	01	01

** = 640 x 480 x 256 colors

Source Code for PLD U5 (GAL20V8) in CUPL™ Language

```
Name        ff;
Partno      ff01;
Date        1/20/93;
Revision    01;
Designer    Todd K. Moyer;
Company     Integrated Circuit Systems;
Assembly    Flicker Filter;
Location    U5;

/**********************************************************************/
/*                                                                    */
/* VGA @ 2xNTSC rate controller with basic line flicker filtering     */
/*                                                                    */
/*                                                                    */
/**********************************************************************/
/*                                                                    */
/* Allowable Target Device Types:  g20v8                              */
/*                                                                    */
/**********************************************************************/

/** Inputs **/

Pin 1        =   clock        ;    /* VGA PCLK signal                   */
Pin 2        =   h_sync_NTSC  ;    /*                                   */
Pin 12       =   GND          ;
Pin 13       =   !OE          ;
Pin 24       =   VCC          ;

/** Outputs **/

Pin [15..18] =   [HSN_S0..3];      /* used by state machine             */
Pin 19       =   !line_start;      /* pointer reset line mem, act lo    */

Pin 20       =   !write_enable_B;  /*                                   */
Pin 21       =   !write_enable_A;  /*                                   */
Pin 22       =   !write_enable;    /*                                   */

/** Declarations and Intermediate Variable Definitions **/

Field   State_HSync         = [HSN_S0..3];

/** Logic Equations **/
```

```
/** State machine definition **/

Sequence State_HSync
{
        present 0
                        if h_sync_NTSC next 1
                                out line_start out line_startAB
                                out write_enable out write_enable_A;
                        if !h_sync_NTSC next 0
                                out write_enable;
        present 1
                        if h_sync_NTSC next 2
                                out line_start out line_startAB
                                out write_enable out write_enable_A;
                        if !h_sync_NTSC next 0;
        present 2
                        if h_sync_NTSC next 3
                                out line_start out line_startAB
                                out write_enable out write_enable_A;
                        if !h_synch_NTSC next 0;
        present 3
                        if !h_sync_NTSC next 4;
                                /* out write_enable; */
                        if h_sync_NTSC next 3
                                out write_enable_A;
        present 4
                        if !h_sync_NTSC next A;
                        if h_sync_NTSC next 3;
        present A
                        if !h_sync_NTSC next 5;
                        if h_sync_NTSC next 3;
        present 5
                        if h_sync_NTSC next 6
                                out line_start out line_startAB
                                out write_enable out write_enable_B;
                        if !h_sync_NTSC next 5
                                out write_enable;
        present 6
                        if h_sync_NTSC next 7
                                out line_start out line_startAB
                                out write_enable out write_enable_B;
                        if !h_sync_NTSC next 5;
        present 7
                        if h_sync_NTSC next 8
                                out line_start out line_startAB
                                out write_enable out write_enable_B;
                        if !h_sync_NTSC next 5;
        present 8
                        if !h_sync_NTSC next 9;
                                /* out write_enable; */
                        if h_sync_NTSC next 8
                        out write_enable_B;
```

```
     present 9
                    if !h_sync_NTSC next B;
                    if h_sync_NTSC next 8;
     present B
                    if !h_sync_NTSC next 0;
                    if h_sync_NTSC next 8;

     present C
                    next 0;
     present D
                    next 0;
     present E
                    next 0;
     present F
                    next 0;
}
```

Bill of Materials

Item	Qty	Reference	Part
1	15	C1, C2, C3, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16	.1µF
2	1	C4	10µF
3	1	DL1	400 ns
4	2	Q1, Q2	2N3904
5	2	Q3, Q4	VN2222
6	2	Q5, Q6	2N3906
7	5	R1, R14, R21, R23, R24	1K
8	1	R2	120
9	1	R3	100
10	2	R4, R5	121
11	1	R6	150
12	3	R7, R8, R9	47
13	3	R10, R11, R12	33
14	3	R13, R27, R28	200

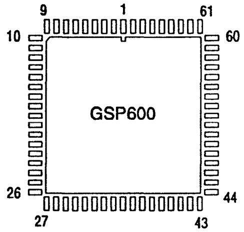
Item	Qty	Reference	Part
15	2	R15, R18	8.2K
16	2	R16, R19	4.3K
17	2	R17, R20	22K
18	1	R22	680
19	2	R25, R26	1.2K
20	1	R29	4.7K
21	3	U1, U9, U10	SC11483CV
22	3	U2, U3, U4	UPD42101
23	1	U5	GAL20V8
24	1	U6	LM317
25	1	U7	TL072
26	1	U8	74HC74
27	1	U11	AD811

Integrated
Circuit
Systems, Inc.

VGA/PAL Video Genlock Processor with Overlay

Overview

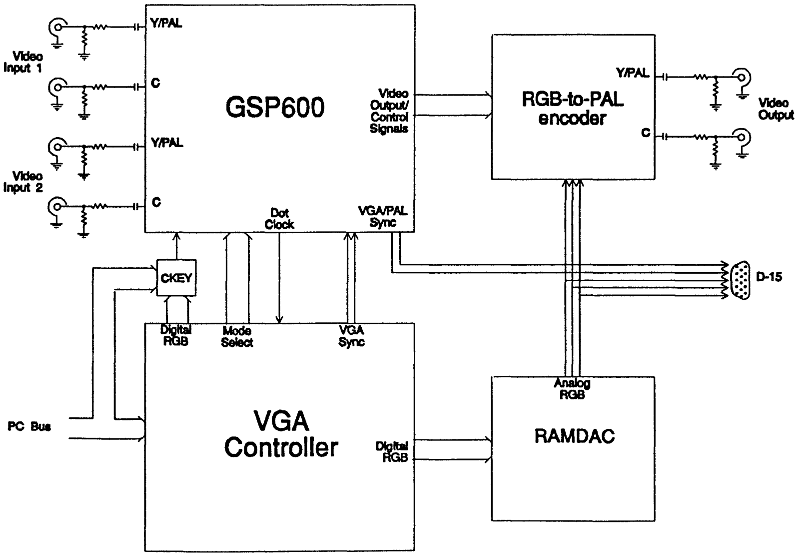
The **GSP600** allows the text and graphic images of VGA and Super VGA controllers to be displayed on standard PAL televisions or recorded on a VCR. Additionally, the **GSP600** accepts external video input from a camcorder or a VCR and will synchronize (genlock) the VGA or Super VGA controller to the external video. The **GSP600** also allows VGA and video images to be overlaid on the same television screen. The **GSP600** meets or exceeds all PAL broadcast standards for timing accuracy and allows the VGA controller to maintain true PAL compatibility at all times. The **GSP600** is compatible with virtually all VGA controllers. Tseng Labs, Oak Technology, Trident Microsystems, S3, and NCR have BIOS support available for the GSP family of products.



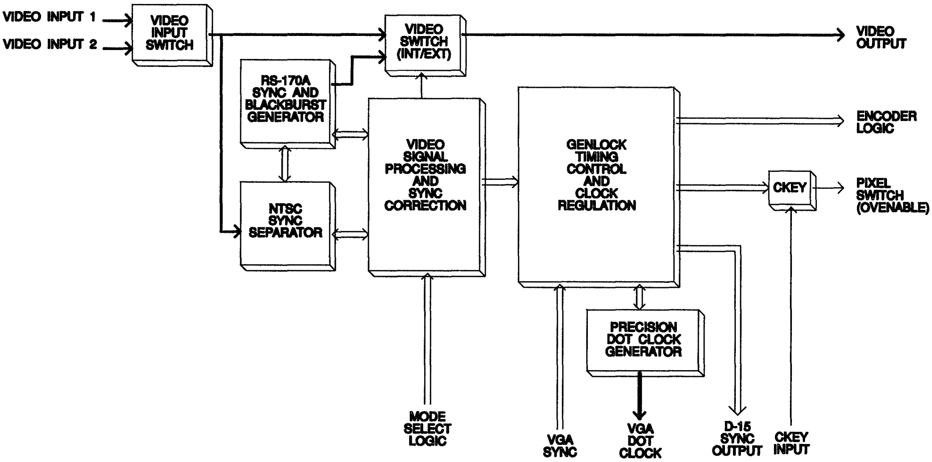
68-Pin PLCC
K-10

Features

- Direct input of PAL or S-Video (S-VHS and Hi-8 video).
- On board PAL/S-Video sync and black burst generation for local video operation. Video chroma burst separate with 4.433618 MHz and 17.734475 MHz phase locked outputs.
- Meets or exceeds all timing specifications for studio and broadcast television.
- High efficiency PAL/S-Video conversion that maintains VGA performance.
- Dynamic overscan and underscan adjustment of PAL/S-Video modes under BIOS and/or software control.
- Software selection between all VGA and PAL/S-Video modes.
- PAL/S-Video conversion support for all VGA and Extended VGA modes with 600 or fewer lines.
- Built-in dot clock circuitry to eliminate crystal oscillators for VGA,plus extended VGA operation up to 135 MHz.
- Low power consumption, ideal for laptop computers.



Internal Block Diagram



Theory of Operation

The **GSP600** can be thought of as an extremely sophisticated dot clock generator. In its simplest form, the **GSP600** will generate all of the dot clock frequencies necessary to drive VGA and Super VGA controllers. The different frequencies are selected with the **MODE SELECT LOGIC** from the VGA chip. Selection is similar to selecting frequencies on any of the ICS dot clock generators (i.e., ICS1394, ICS1494, ICS1561, ICS2494, etc.). Additionally, there are four reserved frequency addresses. These are labeled GL (genlock), OV (overlay), VO (video only), and GO (graphics only). Choosing any of these addresses will switch the **GSP600** from VGA mode to PAL mode. Under PAL mode, the **GSP600** accepts vertical and horizontal **VGA SYNC** from the VGA controller and uses the sync to generate and adjust the **VGA DOT CLOCK**. The **GSP600** will automatically vary the frequency of the dot clock in order to synchronize the VGA sync signals with a PAL reference signal. This reference signal can be derived from a video device (such as a camcorder) connected to **VIDEO INPUT 1** or **VIDEO INPUT 2**. The **GSP600** provides an RGB-to-PAL encoder with the **VIDEO OUTPUT** signal which is either **VIDEO INPUT 1**, **VIDEO INPUT 2**, or an internally generated black burst signal. All of the necessary **ENCODER LOGIC** signals to properly drive the encoder are provided by the **GSP600**.

During PAL modes the **GSP600** also creates the **D-15 SYNC OUTPUT** for the monitor connection to allow for TV projection output of the VGA images. The **PIXEL SWITCH** information derived from external **CKEY INPUT** tells the encoder whether to display the VGA image or external video for each pixel. Assuming the images are genlocked, this creates the overlay effect.

Block definition

Video Input Switch

The Video Input Switch selects whether the **GSP600** uses VIDEO INPUT 1 or VIDEO INPUT 2 as the external video source. It is controlled by an external pin of the **GSP600**.

PAL Sync Separator

The **GSP600** contains a high quality sync separator to allow direct input of PAL, S-VHS, or HI-8 video signals from camcorders, VCRs, and other video products. The **GSP600** utilizes a differential video input circuitry for maximum noise immunity. It also employs digital noise filtering and enhanced digital signal tracking technology to ensure maximum compatibility with consumer, industrial, and broadcast video signals. Although low cost video sync separator products are commonly available, they are primarily designed for television and video monitor use. The simple diode clamping circuit used in these devices does not have the accuracy or noise immunity required for genlocking.

PAL Sync and Black Burst Generator

PAL Sync Generator

The studio quality built-in video sync generator allows the **GSP600** to operate without an external video input and still maintain broadcast video timing. This assures PAL compatibility at all times. When external video is present, the sync generator works in conjunction with the sync separator to isolate sync from noisy video signals.

Black Burst Generation

Most RGB-to-PAL encoders synchronize a crystal oscillator to the chroma burst signal of the external video signal. This provides the color reference portion of the video signal. If an external video signal is not available, the crystal oscillator will free run, creating screen artifacts such as 45 degree moving lines in constant color portions of the screen. To eliminate this problem, the **GSP600** generates a black burst video signal. Black burst video is an analog signal containing both sync and a correctly phased chroma burst signal. This ensures proper color reference generation at all times. The **GSP600** provides black burst output to the encoder when external video is either missing or not selected (non-genlock mode).

INT/EXT Video Switch

The Internal/External Video Switch determines whether the encoder uses external video or the black burst signal. If external video is chosen, the **GSP600** will simply pass the external video signal through to the encoder, unaffected. Black burst is used when external video is not present. The switch is controlled by the Video Signal Processing and Sync Correction circuitry.

Video Signal Processing and Correction

Video Signal Processing

The Video Signal Processing circuitry of the **GSP600** measures the incoming video signal for basic timing accuracy and signal noise. It contains intelligent circuitry to remove extraneous portions of the video signal that would normally be incorrectly categorized as sync. This is extremely important when using a VCR as a video input. If there is an interruption of the external video signal, this circuit will automatically switch inputs from the external video signal to the internal sync generator. When the external video signal resumes, the circuit will automatically switch back to the external video. The Video Signal Processing accepts the MODE SELECT LOGIC from the VGA chip. This logic chooses either VGA or PAL operation and selects whether genlock to external video is to be enabled.

Sync Correction

The Sync Correction circuitry looks for missing sync pulses, block sync, single field video, and phase shift errors caused by the head switching zone of a VCR. It assures proper genlock during all of these problems common in consumer video products.

Genlock Timing Control and Clock Regulation

The **GSP600** looks at the input sync from the VGA controller and determines how to alter the dot clock to create PAL timing. Both the frequency and the method can change with different VGA modes. The **GSP600** enables virtually any VGA controller capable of interlacing to create PAL timing. The **GSP600**'s unique architecture provides ultra-high efficiency and flexibility and allows the frequency of the dot clock to be controlled totally under BIOS or software control. Screen attributes such as horizontal width and position can be individually programmed for each mode while maintaining genlock integrity. This circuit will modify the timing of virtually any mode, with 600 or fewer lines, to meet PAL specifications. The **GSP600** genlock timing control and clock regulation design is awaiting patent approval.

Precision Dot Clock Generator

The **GSP600** uses the same state-of-the-art dot clock technology that has made ICS the premier supplier of VGA dot clock generators. ICS offers the highest accuracy and lowest jitter products available.

CKEY

The ckey (or color-key) circuitry creates the pixel switch for the encoder. This signal determines whether the VGA image or external video is displayed for each pixel. Ckey is modified by the **GSP600** to ensure that the pixel switch signal is delayed (to make up for delays in the RAMDAC) and that it has proper levels during sync and blanking. If the VGA and external signals are genlocked, this pixel switch will create an overlay effect.

PIN NUMBER	NAME	DESCRIPTION
1	VLE	VERTICAL LOCK ENABLE. HIGH for VGA controllers. LOW disables vertical lock feature, may be useful for Non-VGA Operation.
2	ODD/EVEN	ODD/EVEN FIELD IDENTIFICATION. HIGH indicates odd numbered field, LOW indicates even numbered field.
3	BP	BACK PORCH PULSE. Negative polarity TTL level signal used by some RGB-to-PAL encoders.
4	DATAIN	Data input for inserting SMPTE time code in video signal.
5	CB	COMPOSITE BLANKING OUTPUT. Indicates non-screen data portions of PAL signal.
6	CS	COMPOSITE SYNC. PAL composite sync output for RGB-to-PAL encoders. Gated off during VGA modes.
7	CKEY	COLOR KEY. Resultant input from the 8-bit compare of digital RGB (P0-P7) and a software selectable byte. This color key determines which pixels display VGA and which display external video in overlay mode. See Hardware Interface Manual for more details.
8	TEST	For ICS use only.
9	VSYNCOUT	VERTICAL SYNC OUTPUT. Vsync output for DB-15 connector.
10	DATAFRAME	TTL level framing signal active during lines 10-20. For use in time code applications.
11	OVENABLE	OVERLAY ENABLE. Fast pixel rate switch. HIGH displays PAL output, LOW display RGB output. Used for overlay encoders. See Application Notes for wiring details.
12	I/ES	INT./EXT. SYNC. Determines sync selection in OVENABLE signal. Tie LOW normally.
13	LOC/REM	LOCAL/REMOTE. A LOW output state signifies REMOTE status indicating that external video is present and a genlock mode has been selected. If external video goes away or a non-genlock mode is selected, LOCAL/REMOTE will go HIGH.
14	BRSTACT	For ICS use only.
15	$\overline{\text{FRTSTOUT}}$	For ICS use only.
16	HS	HORIZONTAL SYNC. For some RGB-to-PAL encoders. Gated off during VGA modes.
17	$\overline{\text{HRSTOUT}}$	For ICS use only.
18	HSYNCOUT	HORIZONTAL SYNC OUTPUT. Hsync output for DB-15 connector.
19	VSS	Digital ground. We strongly recommend the use of a multilayer board and a ground plane.
20	VDD	5 Volt digital power. We strongly recommend the use of a multilayer board and a power plane.
21	VDD	5 Volt digital power. We strongly recommend the use of a multilayer board and a power plane.
22	VSS	Digital ground. We strongly recommend the use of a multilayer board and a ground plane.
23	FS5	Frequency Select 5. Selects between multiple VGA Dot Clock frequencies, Genlock modes and PAL frequencies. See Dot Clock Generation and PAL Mode Selection sections for a more detailed description. Also see Application Notes for wiring diagrams and BIOS Interface Manual for details.

PIN NUMBER	NAME	DESCRIPTION
24	FS4	Frequency Select 4. Selects between VGA Dot Clock frequencies and PAL modes.
25	FS3	Frequency Select 3. Selects between VGA Dot Clock frequencies and PAL modes.
26	FS2	Frequency Select 2. Selection between VGA Dot Clock frequencies and PAL modes.
27	FS1	Frequency Select 1. Selects between VGA Dot Clock frequencies and PAL modes.
28	FS0	Frequency Select 0. Selects between VGA Dot Clock frequencies and PAL modes.
29	EXTSYNC	For ICS use only.
30	VCR1	HIGH permits using VCRs as an input.
31	CLAMPLEV	Clamping level adjustment for video input. See Application Notes for more details.
33	Y1	PAL video input number 1. Note: This is also the Y (luminance) input for S-Video systems.
32	Y2	PAL video input number 2. Note: This is also the Y (luminance) input for S-Video systems.
34	C2	C (Chrominance) input number 2 for S-Video systems.
35	C1	C (Chrominance) input number 1 for S-Video systems.
36	4.43SC	4.433618 MHz SUBCARRIER OUTPUT. Phase-locked to the chroma burst signal to allow encoders to maintain proper SCH phasing.
37	$\overline{\text{FRSTIN}}$	For ICS use only.
38	AVDD	5 Volt analog power. We strongly recommend the use of a multilayer board and a power plane.
39	GFF	Inverts field 1 and field 2 of VGA sync. Normally tied HIGH.
40	VCOLF	VCO LOOP FILTER CIRCUIT.External RC circuit used in VCO circuitry. See Application Notes for component values.
41	SYNCTHRS	Sync threshold adjustment for video input. See Application Notes schematic.
42	VGAO/E	VGA ODD/EVEN FIELD IDENTIFICATION. HIGH indicates odd numbered field, LOW indicates even numbered field.
43	COUT	C (Chrominance) OUTPUT. C output for S-Video systems.
44	$\overline{\text{RST}}$	Chip reset pulse. This to be tied high through a resistor. Do not tie to the computer reset line.
45	YOUT	Y (Luminance) OUTPUT. PAL video output when the PAL/SVID input is in the HIGH state. Y output for S-Video systems when the PAL/SVID input is in the LOW state.
46	$\overline{\text{HALIGNOUT}}$	For ICS use only, wire to pin 62.
47	SYSLF	SYSTEM CLOCK LOOP FILTER CIRCUIT. External RC circuit used in the chroma burst phase locking circuit. See Application Notes for component values.
48	XTALI	17.734475 MHz crystal circuit. See Application Notes for parts specifications and wiring diagrams.
49	XTALO	17.734475 MHz crystal circuit. See Application Notes for parts specifications and wiring diagrams.

PIN NUMBER	NAME	DESCRIPTION
50	AVSS	Analog ground. We strongly recommend the use of a multilayer board and a ground plane.
51	VID1/2	Input selector. High for Y1/C1, Low for Y2/C2.
52	VCOOUT	For ICS use only, do not wire.
53	FILTSEL	For ICS use only, wire to pin 57.
54	DOTCLOCK	Clock signal input for VGA chip.
55	VFF	Inverts field 1 and field 2 of PAL sync. Normally tied HIGH.
56	$\overline{\text{VCR2}}$	LOW modifies sync characteristics to permit operation with VCR input.
57	VGA/PAL	Mode identification output signal. HIGH indicates a VGA mode, LOW indicates a PAL mode.
58	$\overline{\text{BG}}$	BURST GATE PULSE. Negative polarity TTL level signal used by RGB-to-PAL encoders.
59	LOC/REM IN	For ICS use only, wire to pin 13.
60	VGAHSYNC	VGA HORIZONTAL SYNC. HSYNC signal from VGA chip. See BIOS Interface Manual for programming details.
61	VGAVSYNC	VGA VERTICAL SYNC. VSYNC signal from VGA chip. See BIOS Interface Manual for programming details.
62	$\overline{\text{HALIGNIN}}$	For ICS use only, wire to pin 46.
63	PAL/SVID	PAL/S-VIDEO. Selects between PAL and S-Video output. HIGH=PAL; Low=S-Video.
64	VS	VERTICAL SYNC. PAL Vsync output for RGB-to-PAL encoders. Gated off during VGA modes.
65	4XSC	4 TIMES SUBCARRIER OUTPUT. 17.734475 MHz signal phase-locked to the chroma burst signal.
66	PCLK	PCLK from VGA chip.
67	DATAOUT	TTL level output. This reads data during lines 10-20 and outputs it as a digital signal. For use in time code applications.
68	SCH	SCH PULSE. Positive polarity TTL level signal to distinguish between fields 1 and 3 or 2 and 4. Not necessary for most encoders.

BIOS Programming Example

BIOS support is currently available from Tseng Labs, Oak Technology, Trident Microsystems, S3, and NCR. Other VGA manufacturers have support programs underway. If you use one of these VGA controllers that have completed BIOS support, you can ignore this section. The following information may be helpful to VGA manufacturers and software developers. These tables represent register settings one particular VGA controller. Others are listed in the BIOS Interface Manual. This particular controller does not interlace text modes and uses an 8 x 8 font for modes 0, 1, 2 , 3, and 7. The horizontal registers are adjusted to produce underscan for text modes and overscan for graphics modes.

Horizontal CRTC Registers

CRTC INDEX	CRTC REGISTER	Modes: 00, 01, 04, 05, 0D	Modes: 02, 03, 06, 07, 0E, 0F, 10	Modes: 11, 12, 13
00	HT	35	6B	66
01	HDE	27	4F	4F
02	SHB	2A	53	52
03	EHB	96	8B	87
04	SHR	30	5B	58
05	EHR	92	83	80

Vertical CRTC Registers

CRTC INDEX	CRTC REGISTER	200 Line Modes: (Non-Interlaced) 00, 01, 02, 03, 07, 04, 05, 06, 0D, 0E, 13	350 Line Modes: (Interlaced) 0F, 10	480 Line Modes: (Interlaced) 12, 13
06	VT	05	05	05
07	OVERFLOW	11	11	11
10	VRS	E0	D3	F4
11	VRE	84	87	88
12	VDE	C7	AE	EF
15	SVB	DC	CF	F0
16	EVB	F2	E5	06

Note: The MSB of the MSL register (INDEX 09) must be turned OFF in 200 line NTSC modes. When using an 8 x 8 font for text (modes 00, 01, 02, 03, 07) the 4 LSB of this register will change from F to 7.

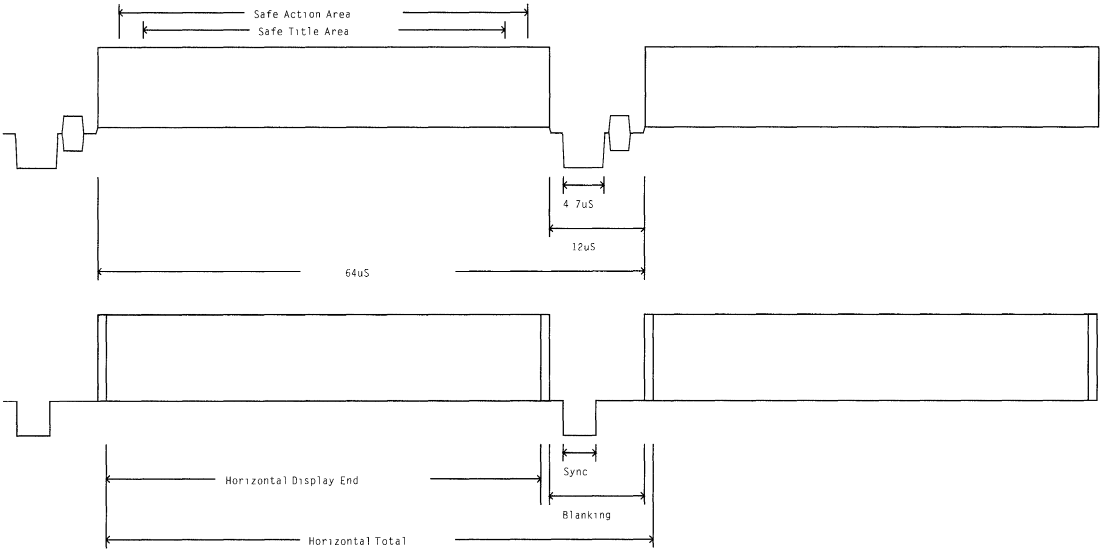
Miscellaneous Output Register

NTSC mode	Color Modes: 00, 01, 02, 03, 04, 05, 06, 0D, 0E, 10, 11, 12, 13	Monochrome Modes: 07, 0F
Genlock (GL)	23	22
Overlay (OV)	27	26
Video Only (VO)	2B	2A
Graphics Only (GO)	2F	2E

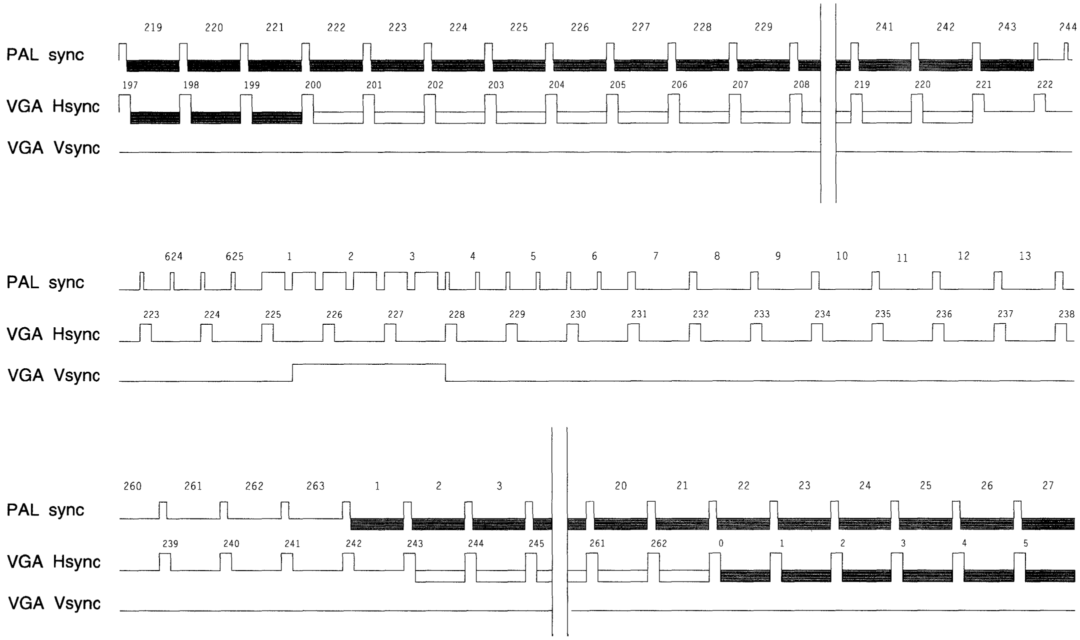
Extended Registers

Turn OFF all DOTCLOCK/2 bits.

PAL vs VGA Horizontal Timing



PAL vs VGA vertical timing (200 line mode)



Electrical Specifications

Operating temperature range 0°C to 70°C

Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Analog Supply	A_{VDD}	4.5	5.0	5.5	Volts
Digital Supply	D_{VDD}	4.5	5.0	5.5	Volts
Operating Current - VGA Mode	I_{DD} (VGA)		35		mA
Operating Current - PAL Mode	I_{DD} (PAL)		50		mA

Input Signals

SIGNAL TITLE	PIN #	TYPICAL VALUE	OPERATING CONDITIONS
Y1	33	1 V_{P-P}	75 Ohm load
C1	35	1V_{P-P}	75 Ohm load
Y2	32	1V_{P-P}	75 Ohm load
C2	34	1V_{P-P}	75 Ohm load
VID1/2	51	TTL/CMOS	High = Y1,C1; Low = Y2,C2
PAL/SVID	63	TTL/CMOS	High = PAL; Low = S-Video
VGAVSYNC	61	TTL/CMOS	Positive polarity
VGAHSYNC	60	TTL/CMOS	Positive polarity
FS0-5	28-23	TTL/CMOS	Address/mode select
CKEY	7	TTL/CMOS	High = RGB; Low = PAL
PCLK	66	TTL/CMOS	Pixel (DAC) Clock from VGA
I/ES	12	TTL/CMOS	High = Internal sync Low = External sync
DATAIN	4	TTL/CMOS	Active during DATAFRAME
CLAMPLEV	31	1-1.5 V	
SYNCTHRS	41	CLAMPLEV +0.1 V	
VLE	1	TTL/CMOS	Tie to V_{DD} through resistor
RST/	44	TTL/CMOS	Tie to V_{DD} through resistor

Output Signals

SIGNAL TITLE	PIN#	TYPICAL VALUE	OPERATING CONDITIONS
VSYNCOUT	9	TTL	Positive polarity during PAL modes
HSYNCOUT	18	TTL	Composite sync during PAL modes
VS	64	$1V_{P-P}$	Positive polarity
HS	16	$1V_{P-P}$	Positive polarity
CS	6	$1V_{P-P}$	Positive polarity
DOTCLOCK	54	TTL	
YOUT	45	$1V_{P-P}$	75 Ohm load
COUT	43	$1V_{P-P}$	75 Ohm load
4.43SC	36	TTL	4.433618 MHz
4XSC	65	TTL	17.734475 MHz
LOC/REM	13	TTL	High = local; Low = remote
OVENABLE	11	TTL	High = PAL; Low = RGB
VGA/PAL	57	TTL	High = VGA; Low = PAL
CB	25	TTL	Positive polarity
ODD/EVEN	2	TTL	High = odd field; Low = even field
VGAO/E	42	TTL	High = VGA odd field Low = VGA even field
BG/	58	TTL	Negative polarity
FP/	3	TTL	Negative polarity
SCH	68	TTL	Positive polarity
DATAFRAME	10	TTL	Lines 10-20
DATAOUT	67	TTL	Active during DATAFRAME

Dot Clock Selection

The following charts represent two of the many dot clock frequency selection tables supported by **GSP600**. See the BIOS manual or contact ICS applications engineering for additional information.

FREQUENCY (MHz)	FS5	FS4,FS3,FS2	FS1	FS0
50.350	0	1	0	0
56.644	0	1	0	1
65.028	0	1	1	0
72.000	0	1	1	1
75.000	1	0	0	0
80.000	1	0	0	1
89.800	1	0	1	0
110.000	1	0	1	1
Gen**L**ock	1	1	0	0
OVerlay	1	1	0	1
Video **O**nly	1	1	1	0
Graphics **O**nly	1	1	1	1

FREQUENCY (MHz)	FS5,FS3	FS4, FS2	FS1	FS0
25.175	0	1	0	0
28.322	0	1	0	1
40.000	0	1	1	0
44.900	0	1	1	1
Gen**L**ock	1	1	0	0
OVerlay	1	1	0	1
Video **O**nly	1	1	1	0
Graphics **O**nly	1	1	1	1

Ordering Information

GSP600V

Example:

ICS XXXX V

Package Type
V=PLCC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device, GSP=Genlock Device

GSP600 Frequently Asked Technical Questions.

1. What will the GSP600 do for me?

The GSP600 adjusts the timing of a VGA controller to conform to PAL (television) specifications. The GSP600 accepts direct video input from video cameras, videodisc players or other video sources and will synchronize (genlock) a VGA controller to either the external video input or an internal PAL sync generator. The GSP600 also contains a dot clock generator to eliminate the need for crystal oscillators or other dot clock generators.

2. How does the GSP600 differ from other genlock devices?

Other genlock devices, such as the Motorola MC1378, are very effective at genlocking two PAL signals together and are generally used in consumer electronics products such as video window-in-a-window devices. The GSP600 is specifically designed to genlock a computer graphics controller to PAL video and overcomes all of the incompatibilities between VGA and PAL. Additionally, the GSP600 contains an PAL sync generator and maintains chrominance phase lock in local modes. This allows the GSP600 to maintain PAL timing without an external video input. Furthermore, the sync separator circuit of the GSP600 is designed to satisfy the low jitter tolerances demanded by discriminating VGA customers.

3. Isn't genlock simply a phased-lock loop?

Phase locking two similar signals is fairly straightforward as long as phase jitter is not critical. As an example, ICS is one of the few companies able to successfully build phase-locked loop dot clock generators with low enough phase jitter for computer graphics display. Additionally, the differences between VGA and PAL signals further complicate the genlock procedure. The GSP600 has patents applied for for the most advanced computer video genlock methods in the industry. These methods assure you of the highest possible quality product.

4. Most Genlock and Overlay products have a lot of discrete components with trimmer capacitors and potentiometers. All these adjustments can become very expensive in a mass production environment. How much external circuitry does the GSP600 require?

Although the GSP600 can be run with no trimmer capacitors or potentiometers, one trimmer capacitor should be used to meet the PAL frequency tolerance of the chroma burst. This is a free running frequency and is very simple (and fast) to adjust. Additionally, the GSP600 uses high speed digital circuitry to eliminate virtually all discrete components. Only a few external components are needed for full operation.

5. Do I need an RGB-to-PAL encoder with the GSP600?

Yes, an external RGB-to-PAL encoder is needed. The encoder must be matched to the target audience. The GSP600 can be used under broadcast television scrutiny and most broadcast video equipment perform the encoding entirely with discrete components. As this may prove too costly and/or may use too much board space, the GSP600 contains all of the necessary signals to drive virtually any encoder. The GSP600's generous supply of timing signals will also drive external circuitry to turn off the encoder for laptop applications.

6. Why do I need the GSP600. Can't I program a VGA controller for PAL sync and just drive an RGB-to-PAL encoder?

PAL sync contains equalizing pulses, blanking signals and pulse widths that are impossible to create under normal VGA control. Although marginal display quality is achievable on a television without adhering to the PAL standard, compatibility with other PAL equipment is compromised. As an example, depending on which edge of horizontal sync the monitor triggers on will determine how far an incorrect width horizontal sync pulse will skew the screen. Additionally, it becomes virtually impossible to assure proper chroma burst (SCH) phasing. The GSP600 sync generator meets or exceeds all PAL broadcast standards for timing accuracy assuring you of maximum compatibility and ultimate quality.

7. National sells a sync separator for less than $2 while the Brooktree part costs over $50. What is the difference and how does the sync separator in the GSP600 compare?

The sync separation circuitry in the National part is a simple diode clamp. Although this may be adequate for driving a picture tube, the lack of noise and jitter immunity make it unsuitable for genlock applications. Additionally, the analog vertical sync detection circuit of these type of devices will not accurately track a VCR signal. The Brooktree device represents a mixed-mode approach to sync separation. By utilizing a fast analog circuitry coupled with high speed digital logic, noise and jitter immunity can be optimized. The GSP600 also uses a mixed mode approach specifically optimized for genlock operation yet the incorporation of a sync generator allows signal analysis not possible with other devices.

8. Is the GSP600 compatible with any VGA controller?

VGA controllers need to have two features to work with the GSP600. First, they need to be able to interlace - if your controller can display 1024 x 768 resolution, then it can probably interlace (the additional 256K memory is not necessary). Second, the controller must have at least three clock select lines for external dot clock generator support. Virtually all current VGA controllers have this feature. Check with your VGA controller manufacturer or ICS if you are unsure.

9. How do I turn the PAL on and off and control it?

The GSP600 uses the three clock select lines to support 4 VGA clocks and 4 PAL modes. The VGA clocks are available in 7 different patterns (i.e. 25.175, 28.322, 40.000, 65.000 is one pattern). The 4 PAL modes are Genlock, Overlay, Graphics Only, and Video Only. The selection between any PAL mode or between PAL and VGA is done entirely under BIOS or software control.

10. Why did you incorporate a dot clock generator in the GSP600?

The GSP600 works by modifying the dot clock input for the VGA controller. It essentially is a dot clock generator designed for PAL genlock. The dot clock generator is not so much of an extra feature as it is a subset of the genlock design. Consequently, this unity design assures you of a reliable glitch-free solution.

11. When the GSP600 displays an Overlay, how do I determine which part of the screen displays graphics and which is VGA?

The GSP600 uses a technique called Color-Key to determine where to display the external video. This Color-Key color is based on the VGA color number. Therefore, no colors are actually lost. As an example, the background color is always Color 0. When Color-Keying on Color 0, the screen will appear to have a background of the external video. The actual color that the VGA assigns to Color 0 does not matter. Any of the 256 color numbers can be assigned to be a Color-Key. Although the GSP600 modifies the Color-Key input, the Color-Key selection is done by an external 8 bit digital compare.

12. Why is the Color-Key selection external to the GSP600?

Color-Key selection is done with an 8 bit compare of the digital RGB signals with a preassigned byte. The digital RGB data comes from the VGA controller and the preassigned byte normally comes from the IBM bus via a port selection. The output of this comparison is fed into the CKEY (Color-Key) input of the GSP600. Although this Color-Key method will satisfy 95% of all customers, the external design allows other schemes with multiple or different comparison options. Additionally, since all of these signals are already available inside the VGA controller, many manufacturers have announced plans to incorporate the Color-Key function inside the VGA controller.

13. What about NTSC and/or SECAM compatibility?

ICS has an NTSC version of the GSP600 (the GSP500). In its current implementation, it is pin compatible with the GSP600 but require different values for the discrete components and will also need a different crystal oscillator. Although a SECAM version is technically possible, due to the uncertain market potential product development is not currently underway.

14. Can I look forward to a combination PAL and NTSC product?

Unfortunately, the amount of circuitry common to both a PAL and an NTSC version is minimal. Separate versions are currently the lowest cost solution. Although the crystal frequency, some discrete components and the Bios would have to change, the same board layout could support both standards by simply changing the parts list.

15. Does the GSP600 accept multiple video inputs? What about an S-Video input?

The GSP600 has two independent video inputs. Either input can be used or they can both be disabled. Either input can be wired to accept either S-Video or PAL. Selection between the two inputs is performed under hardware control.

16. Why doesn't the GSP600 incorporate audio?

The PAL and S-Video baseband signals do not have a provision for audio. This means that the video and audio signals are completely separate signals at all times. ICS offers audio products for the multimedia market that can be incorporated into the design but allows the designer maximum flexibility by keeping them separate products.

17. Can I use the GSP600 with an RF modulator?

Yes, but the quality of the image may suffer. When PAL is modulated up to RF frequencies, audio is modulated onto a 4.5 MHz carrier and the video is limited to a maximum frequency of 4.2 MHz. Although 4.2 MHz may be sufficient for moving images it can be limiting for high resolution computer graphics. This problem is magnified because the majority of RF modulators are very low quality devices. Additionally, even if a high quality RF modulation is obtained, the signal may still be degraded by the RF demodulator inside the television set. ICS does recognize that these limitations may be outweighed by the user-friendliness and compatibility of the RF standard. High quality RF modulators are available and the GSP600 does have the necessary signals for support but these issues should be carefully weighed before implementation.

18. Can the GSP600 display PAL video on my VGA screen?

No, in order to display PAL video at 31.25 KHz, it is necessary to convert PAL into component form, digitize it in real time, and store at least one frame of video. Although technology exists to accomplish this, the price-to-performance ratio of these products is too high for mass market acceptance at this time.

19. Is there any question that I forgot to ask?

Yes, when I use a graphics program, I find the borders very distracting yet I need the borders in text modes to insure that I can read the DOS prompt. Can the GSP600 help me with this problem? The GSP600 has the ability to adjust the width of the screen totally under Bios control. This means that you can have limited overscan in mode 13, minor underscan in mode 3 and generous overscan in mode 12. Software drivers can even be written to dynamically change the screen width with the cursor keys.

20. Does this mean I can change the height of the screen also?

PAL has a fixed number of lines. In order to change the vertical size, the screen data must be compressed or expanded into fewer or greater lines. This can be accomplished in a text mode by changing the font size or in a graphics mode with linear interpolation. The GSP600 always maintains an exact one-to- one correlation between the PAL and VGA line position and therefore does not support vertical sizing.

21. Where do I get a development kit for the GSP600?

Call ICS at (800) 220-3366 for more information. We will put you in touch with a local rep. who will be more than happy to supply you with a full GSP600 development kit. The ICS full service support organization is always ready to help you with the latest in Multimedia solutions.

Integrated
Circuit
Systems, Inc.

AN602

Application Note

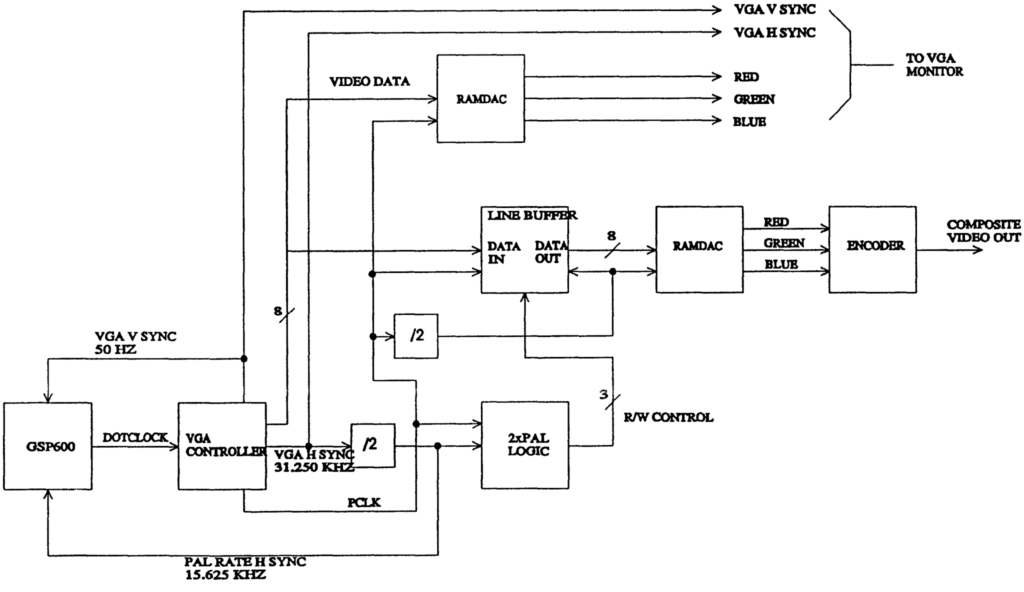
Theory of Operation for a GSP600 Circuit Operating the VGA Display at 2xPAL Frequency

Introduction

In its minimal configuration the **GSP600** with a VGA controller chip puts out both RGB to a VGA monitor and composite video in the PAL format. However, due to the fact that PAL video is interlaced, the minimal configuration requires that the VGA controller be programmed for interlaced operation; this allows the same RAMDAC™ to be used for both the VGA and the PAL outputs (of course the PAL output also must be encoded). Unfortunately, the VGA picture is somewhat degraded by interlacing - and even worse, some VGA monitors won't lock up to the interlaced signal. If this situation is not acceptable, a solution is available that only requires a few additional parts at minimal cost.

The solution is to run the VGA circuitry at exactly twice the PAL rate and in a non-interlaced mode. This preserves the full quality of the VGA display while the VGA is still being gen-locked to an external PAL signal. Of course, now that the VGA RAMDAC is running at a higher speed, another RAMDAC will be required which runs at the PAL rate. Also, some means will be required to accept the fast data rate VGA output and put out the slower rate PAL data. Under these circumstances, the VGA circuitry will be producing twice as much data as can be displayed in PAL and therefore some of it will have to be discarded. All of the VGA lines are used in the PAL frame, but each line is only used for every other PAL field. In other words all the odd numbered VGA lines may be output to PAL field 1 and all the even numbered VGA lines may be output to PAL field 2 while both odd and even numbered lines are put out to the VGA display in every vertical period. The VGA frame rate is then the same as the PAL field rate; the PAL field simply has half as many horizontal lines.

Block Diagram



RAMDAC is a trademark of Brooktree Corporation

Application Circuit

One possible implementation of this idea is shown in the accompanying schematic. Only the additional circuitry required for the 2xPAL enhancement is shown. Following is a detailed description of the operation of the circuit; please refer to the schematic as you read it.

U5B divides the frequency of the VGA HSync signal VHS by two, producing a 50% duty cycle square wave with a frequency of 15.625 kHz. This signal essentially becomes the Write Enable signal at U4 pin 22 and is also sent to the **GSP600** pin 60 as the Horizontal Sync signal. Note that the addition of a divide by 2 in the overall loop which the **GSP600** controls forces the VGA chip to clock at twice the rate that it otherwise would, producing a VGA HSync frequency of 31.650 kHz.

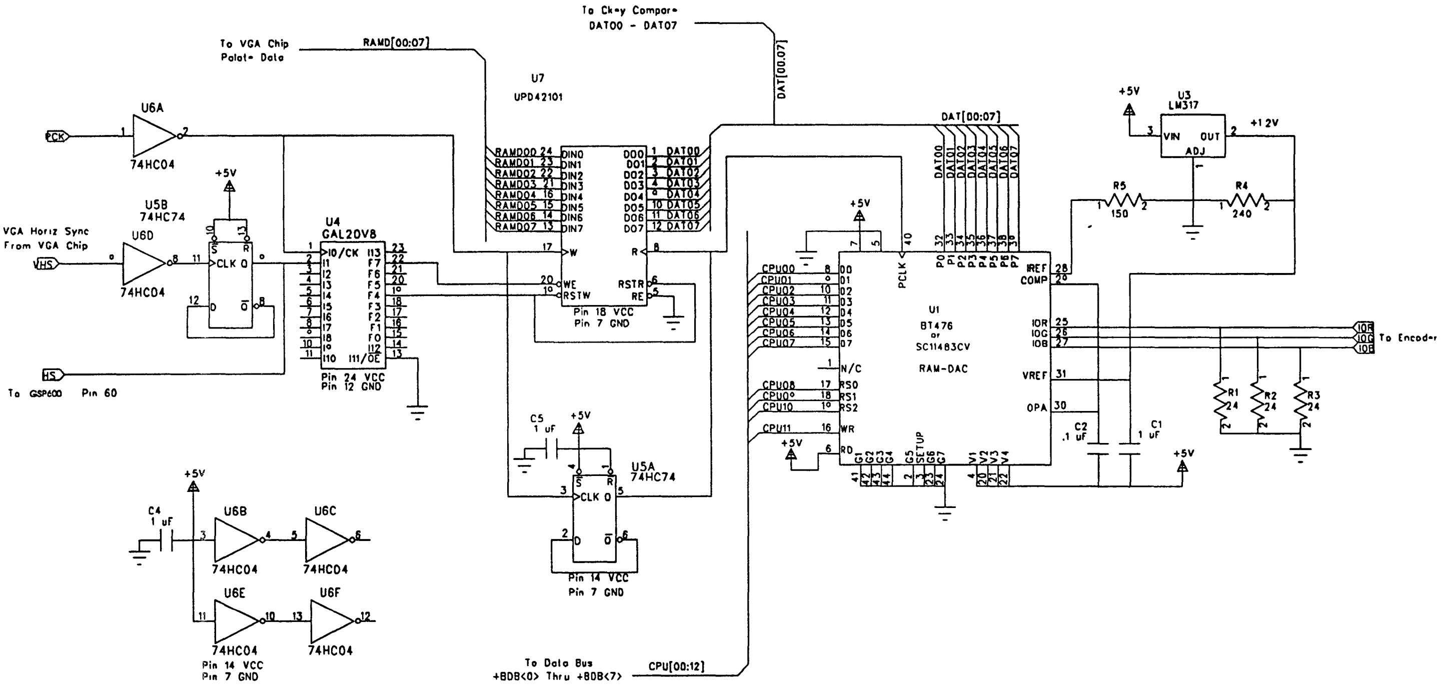
U7 is a line buffer memory which can hold up to 910 pixels with a width of 8 bits; it has individual write and read clocks with associated address pointers. Programmable logic device U4 provides a write enable and pointer reset signals to the line memory. Note that the write clock to U7 (pin 17) is the same rate as the VGA pixel clock; therefore, every VGA pixel will be written in to the memory when write enable (pin 20) is active (low). The write enable is only active for every other line, however, since it is frequency divided by 2 from the VGA HSync as previously noted. This essentially discards half the VGA lines each PAL field, by virtue of the fact that they are not written into memory. The time to write a complete line into memory is 1 VGA line time or 32.0µs. The read clock for U7 is simply the write clock frequency divided by 2 by U5A. Thus to read all the pixels out of the memory will require twice as long as to write them, or 64.0µs. This is the length of a PAL line. Therefore, over the span of 2 VGA lines, 1 VGA line is written and 1 PAL line is read, although the writing takes place at twice the PAL rate.

Data read out from U7 at PAL rate is fed to RAMDAC U1, which has its control lines paralleled across the main VGA RAMDAC, except that the active low read enable (pin 6) is permanently disabled by tying it to +5V. In this way anything written to the VGA RAMDAC (such as changes to the palette) will also be written to U1, but any reads will not cause a conflict with the main VGA RAMDAC. The analog RGB outputs of U1 are sent to the PAL encoder to produce a composite video output. U3 provides a reference for the RAMDAC. Instead of a reference for each RAMDAC, it may be possible to use 1 voltage reference for both RAMDACs in the system if they can be configured to use a voltage reference as shown in the schematic.

Further Enhancement

Although the VGA at 2xPAL enhancement is better than the minimal **GSP600** configuration, it is still less than ideal with respect to the PAL picture quality. It is probably intuitively obvious to most people that throwing away half the VGA data will result in a loss of picture quality on the PAL output. The practically observed result of this is what is generally known as "flicker," and it should be noted that this problem plagues all scan converters and VGA-to-PAL boards. It is worst when there is a lot of detail along the vertical axis of the VGA image. The most annoying example is probably a thin, bright white horizontal line made up of a single line on the VGA display. For an example case, imagine that line 100 of the VGA display contains the white line and the rest of the display is black. Then the white line would appear somewhere around line 50 of field 2 in the PAL output, but not at all on field 1. The result will be a flashing of the line with a period of 40.0 ms (due to 25 Hz frame rate). This is visually very noticeable and irritating. Because of this, many scan converters and VGA-to-PAL boards have a "flicker filter." Interestingly, most flicker filters can be turned off, indicating that they are less than desirable in some situations.

A discussion of flicker filtering and how to implement it with the **GSP600** is the subject of Application Note AN603.


To Ck-y Compare
DAT00 - DAT07
To VGA Chip
Palat- Data
RAMD[00:07]
DAT[00:07]
U7
UPD42101
U6A
PCK
74HC04
+5V
U5B
74HC74
VGA Horiz Sync
From VGA Chip
VHS
U6D
74HC04
CLK Q
D
Q̄
U4
GAL20V8
I0/CK
Pin 24 VCC
Pin 12 GND
HS
To GSP600 Pin 60
RAMD00 24 DIN0
RAMD01 23 DIN1
RAMD02 22 DIN2
RAMD03 21 DIN3
RAMD04 16 DIN4
RAMD05 15 DIN5
RAMD06 14 DIN6
RAMD07 13 DIN7
DO0 1 DAT00
DO1 2 DAT01
DO2 3 DAT02
DO3 4 DAT03
DO4 9 DAT04
DO5 10 DAT05
DO6 11 DAT06
DO7 12 DAT07
W
WE
RSTW
R
RSTR
RE
Pin 18 VCC
Pin 7 GND
C5
1 uF
U5A
74HC74
Pin 14 VCC
Pin 7 GND
C4
1 uF
U6B
U6C
U6E
U6F
74HC04
Pin 14 VCC
Pin 7 GND
To Data Bus
+BDB<0> Thru +BDB<7>
CPU[00:12]
CPU00 D0
CPU01 D1
CPU02 D2
CPU03 D3
CPU04 D4
CPU05 D5
CPU06 D6
CPU07 D7
N/C
CPU08 RS0
CPU09 RS1
CPU10 RS2
CPU11 WR
RD
PCLK
P0 P1 P2 P3 P4 P5 P6 P7
U1
BT476
or
SC11483CV
RAM-DAC
G1 G2 G3 G4 G5 SETUP G6 G7
V1 V2 V3 V4
IREF
COMP
IOR
IOG
IOB
VREF
OPA
C2
.1 uF
C1
1 uF
U3
LM317
VIN
OUT
ADJ
+12V
R5
150
R4
240
R1
24
R2
24
R3
24
IOR
IOG
IOB
To Encoder

CRTC Registers

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	HT	35	35	6B	6B	35	35	62	6C	35	62	62	62	62	62	62	62
01	HDE	27	27	4F	4F	27	27	4F	4F	27	4F	4F	4F	4F	4F	04	4F
02	SHB	2A	28	57	57	2A	2A	50	54	2A	50	50	50	50	50	50	50
03	EHB	95	96	8B	8B	96	96	85	8B	96	85	85	85	84	84	85	84
04	SHR	2E	2E	5D	5D	2F	2F	58	5D	2F	58	58	58	54	57	58	57
05	EHR	A0	A0	8C	8C	80	80	9B	83	80	9B	9B	9B	82	82	9B	82
06	VT	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B
07	OVERFLOW	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E
08	PRS	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
09	MSL	4F	4F	4F	4F	C1	C1	C1	4F	C0	C0	40	40	40	40	C0	40

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
0A	CS	0D	0D	0D	0D	00	00	00	0D	00	00	00	00	00	00	00	00
0B	CE	0E	0E	0E	0E	00	00	00	0E	00	00	00	00	00	00	00	00
0C	SAH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0D	SAL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0E	CLH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0F	CLL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
10	VRS	BE	BE	BE	BE	C5	C5	C5	BE	C5	C5	A7	A7	F4	F4	C5	EF
11	VRE	22	22	22	22	88	88	88	82	88	88	8B	8B	87	87	88	87
12	VDE	8F	8F	8F	8F	8F	8F	8F	8F	8F	8F	5D	5D	DF	DF	8F	DF
13	OFFSET	14	14	28	28	14	14	28	28	14	28	28	28	28	28	28	50
14	UNDERLINE	1F	1F	1F	1F	00	00	00	1F	00	00	0F	0F	00	00	40	60
15	SVB	B8	B8	B8	B8	C2	C2	C2	B8	C2	C2	9F	9F	E0	E0	C2	E0
16	EVB	E3	E3	E3	E3	05	05	05	E3	05	05	CA	CA	0C	0C	05	0C
17	MC	A3	A3	A3	A3	A2	A2	C2	A3	E3	E3	E3	E3	E3	E3	A3	AB
18	LC	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
*	INTERLACE																

* = Interlace Bit must be turned off for all modes

General Register

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	MISC OUT	#	#	#	#	#	#	#	@	#	#	@	#	#	#	#	#

#	@
23 = GenLock (GL)	22 = GenLock (GL)
27 = OVerlay (OV)	26 = OVerlay (OV)
2B = Video Only (VO)	2A = Video Only (VO)
2F = Graphics Only (GO)	2E = Graphics Only (GO)

Sequence Registers

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	CLK MODE	09	09	01	01	09	09	01	00	09	01	01	01	01	01	01	01

** = 640 x 480 x 256 colors

Source Code for PLD U4 (GAL20V8) in CUPL™ Language

```
Name        2PAL;
Partno      XXXXX;
Date        12/07/92  02:12pm;
Revision    02;
Designer    Todd K. Moyer;
Company     Integrated Circuit Systems;
Assembly    XXXXX;
Location    XXXXX;

/**********************************************************************/
/*                                                                    */
/* VGA @ 2xPAL rate controller                                        */
/*                                                                    */
/*                                                                    */
/**********************************************************************/
/*                                                                    */
/* Allowable Target Device Types:  g20v8                              */
/*                                                                    */
/**********************************************************************/

/** Inputs **/

Pin 1        =   clock       ;      /* VGA p-clock                    */
Pin 2        =   h_sync_PAL ;       /*                                */

Pin 12       =   GND         ;
Pin 13       =   !OE         ;
Pin 24       =   VCC         ;

/** Outputs **/

Pin [15..18] =   [HSN_S0..3];       /* used by state machine          */
Pin 19       =   !line_start;       /* pointer reset line mem, act lo */
Pin 20       =   !write_enable_B;   /* not used by 2xPAL              */
Pin 21       =   !write_enable_A;   /* not used by 2xPAL              */
Pin 22       =   !write_enable;     /*                                */

/** Declarations and Intermediate Variable Definitions **/

Field    State_HSync          = [HSN_S0..3];

/** Logic Equations **/
```

```
/** State machine definition **/

Sequence State_HSync
{
      present 0
                  if h_sync_PAL next 1
                        out line_start out line_startAB
                        out write_enable out write_enable_A;
                  if !h_sync_PAL next 0
                        out write_enable;
      present 1
                  if h_sync_PAL next 2
                        out line_start out line_startAB
                        out write_enable out write_enable_A;
                  if !h_sync_PAL next 0;
      present 2
                  if h_sync_PAL next 3
                        out line_start out line_startAB
                        out write_enable out write_enable_A;
                  if !h_synch_PAL next 0;
      present 3
                  if !h_sync_PAL next 4;
                        /* out write_enable; */
                  if h_sync_PAL next 3
                        out write_enable_A;
      present 4
                  if !h_sync_PAL next A;
                  if h_sync_PAL next 3;
      present A
                  if !h_sync_PAL next 5;
                  if h_sync_PAL next 3;
      present 5
                  if h_sync_PAL next 6
                        out line_start out line_startAB
                        out write_enable out write_enable_B;
                  if !h_sync_PAL next 5
                        out write_enable;
      present 6
                  if h_sync_PAL next 7
                        out line_start out line_startAB
                        out write_enable out write_enable_B;
                  if !h_sync_PAL next 5;
      present 7
                  if h_sync_PAL next 8
                        out line_start out line_startAB
                        out write_enable out write_enable_B;
                  if !h_sync_PAL next 5;
      present 8
                  if !h_sync_PAL next 9;
                        /* out write_enable; */
                  if h_sync_PAL next 8
                  out write_enable_B;
```

```
        present 9
                        if !h_sync_PAL next B;
                        if h_sync_PAL next 8;
        present B
                        if !h_sync_PAL next 0;
                        if h_sync_PAL next 8;

        present C
                        next 0;
        present D
                        next 0;
        present E
                        next 0;
        present F
                        next 0;
}
```

Bill of Materials

Item	Qty	Part Name	Description	Manufacturer
1	1	74HC04	HEX INVERTER	Motorola
2	1	74HC74	DUAL D FLIP FLOP	Motorola
3	1	SC11483CV	RAM-DAC	Sierra
4	1	GAL20V8	PLD	Lattice
5	1	LM317	Adjustable Regulator	National
6	1	UPD42101	910x8 FIFO	NEC
7	7	CAP	.1µF Cap	
8	1	R1/4W	240 ohm	
9	1	R1/4W	150 ohm	
10	3	R1/4W	24 ohm	

Integrated
Circuit
Systems, Inc.

Flicker Reduction Circuit for use with the GSP600

Introduction

Although a minimal configuration **GSP600** VGA/PAL system uses all of the lines of the graphics image to generate the PAL picture, the resulting PAL display is not (and cannot be) as good as the original VGA display. Despite the fact that all the lines are used, on the standard non-interlaced VGA display *every* line is used for *every* vertical period of about 20.0 ms, while it takes twice as long to put out all the lines to the PAL picture (40 ms). This is accomplished in practice by one of two ways: 1) interlacing the VGA (slowing it down to PAL rates), or 2) using odd numbered lines for odd PAL fields and even numbered lines for even fields, essentially discarding half the lines that are output from the VGA (see the Application Note AN602, *Theory of Operation for a GSP600 Circuit Operating the VGA Display at 2 x PAL Frequency*). It is probably intuitively obvious that either slowing the VGA down or throwing away half the VGA data will result in the PAL output looking less pleasing than the standard VGA display. The practically observed result of this is what is generally known as "flicker," and it should be noted that this problem plagues all scan converters and VGA-to-PAL boards; it is a fundamental limitation of the PAL standard. It is worst when there is a lot of detail along the vertical axis of the VGA image. The most annoying example is a thin, bright white horizontal line made up of a single line on the VGA display. For an example case, imagine that line 100 of the VGA display contains the white line and the rest of the display is black. Then the white line would appear somewhere around line 50 of field 2 in the PAL output, but not at all on field 1. The result will be a flashing of the line with a period of 40.0 ms (reciprocal of the 25 Hz frame rate). This is very noticeable and quite irritating to the eye.

Knowing that displaying a VGA image on an PAL monitor is at best a compromise, we would at least like to achieve the best possible performance from the conversion. Because of this, most scan converters and VGA-to-PAL boards have a "flicker filter." It is enlightening to note that most flicker filters can be turned off, indicating that they are less than desirable in some situations. In fact they reduce the spatial "bandwidth" in the vertical direction, or in other words reduce the vertical resolution. A particularly simple and effective flicker reduction scheme (which can be implemented in software) is to repeat every other VGA line in both fields of the PAL signal. This method, however, requires that half the VGA lines never get to the PAL display; in other words, the vertical resolution is cut in half. A single horizontal line in the VGA image has only a 50/50 chance of being displayed in PAL, depending on which line number it appears on. Obviously, this method leaves a lot to be desired, since some details in the VGA image can be completely absent from the PAL signal; most people would judge it unacceptable.

You can get a feel for how a better typical flicker filter works by thinking about the example above of a single white horizontal line on scan line 50 of field 2. Imagine "spreading" the line so that some of it spills into the scan lines adjacent to the original line. In an interlaced system such as PAL this means reducing the brightness of line 50 of field 2 (thereby making it gray), and putting some darker shade of gray into lines 50 and 51 of field 1, which are above and below line 50 of field 2, respectively, once the complete frame has been scanned. If done properly, in the right proportions, and viewed from a sufficient distance, the new wide line looks to be of the same brightness as the original single white line. This can significantly reduce the flicker, since there is no longer the situation of black on field 1 and white on field 2 rapidly alternating. However, as you can imagine, any rapid vertical transitions would also become smeared or blurred with such a scheme. The typical complaint is that when trying to display text on an PAL display, a flicker filter will make the text less readable (if it remains readable at all). This type of flicker reduction works best if only the luminance portion of the signal is filtered, since the mixing of several VGA lines to make one PAL line can significantly change the saturation and hue of the color displayed, seriously altering the picture when compared with the VGA display. It is primarily changes in luminance level that cause flicker, so that leaving the chrominance portion of the signal unchanged does not seriously degrade the flicker reduction that is achieved, while it does tend to preserve the look of the image.

To boil all this down, there is a trade-off between flicker reduction and vertical resolution, and it bears repeating that it is a practical impossibility to make an PAL image look just as good as a high resolution VGA image. To try and work around this trade-off, some sophisticated flicker filters are "adaptive," which essentially means that they will dynamically turn themselves on when especially needed to reduce flicker and off when the loss of vertical resolution is especially detrimental. Predictably, this approach is rather expensive and takes up a lot of circuit board space, at least until the time when this function is incorporated into a monolithic integrated circuit. At any rate, a flicker filter of the more basic variety is presented here for use with **GSP600** applications.

AN603RevA101993

Application Circuit

In the accompanying schematic and block diagram an implementation of a simple luminance-only flicker filter which works with the **GSP600** in a VGA-to-PAL system is shown. The schematic details only the portion of the system specific to the flicker filter function, since the VGA portion will vary depending on the VGA chip used. Please refer to the schematic when reading the following detailed circuit description.

U8B divides the frequency of the **VGA_HSYNC** signal **VHS** by two, producing a 50% duty cycle square wave with a frequency of 15.625 kHz. This signal essentially becomes the Write Enable signal at U5 pin 22 and is also sent to the **GSP600** pin 60 as the Horizontal Sync signal **PAL_RATE_HS**. Note that the addition of a divide by 2 in the overall loop which the GSP600 controls forces the VGA chip to clock at twice the rate that it otherwise would, producing a VGA HSync frequency of 31.25 kHz.

U2 is a line buffer memory which can hold up to 910 pixels with a width of 8 bits; it has individual write and read clocks with associated address pointers. Programmable logic device **U5** provides a write enable and pointer reset signals to the line memory. Note that the write clock to U2 (pin 17) is the same rate as the VGA pixel clock; therefore, every VGA pixel will be written in to the memory when write enable (pin 20) is active (low). The write enable is only active for every other line, however, since it is frequency divided by 2 from the VGA HSync as previously noted. This essentially discards half the VGA lines each PAL field, by virtue of the fact that they are not written into memory. The time to write a complete line into memory is 1 VGA line time or **32.0** µs. The read clock for U2 is simply the write clock frequency divided by 2 by U8A. Thus, to read all the pixels out of the memory will require twice as long as to write them, or **64.** µs. This is the length of a PAL line. Therefore, over the span of 2 VGA lines, 1 VGA line is written and 1 PAL line is read, although the writing takes place at twice the rate.

Data read out from U2 at PAL rate is fed to RAMDAC U9, which has its control lines paralleled across the main VGA RAMDAC, except that the active low read enable (pin 6) is permanently disabled by tying it to +5V. In this way anything written to the VGA RAMDAC (such as changes to the palette) will also be written to U9, but any reads will not cause a conflict with the main VGA RAMDAC. The analog RGB outputs of U9 are sent to the PAL encoder to produce the chrominance component of the composite video output. U6 provides the required voltage reference to U9. Also, the RGB outputs from U9 are combined by resistor matrix in the right proportions to create a luminance signal which can be summed with the adjacent lines' luminance signals, thereby spatially lowpass filtering the luminance signal in the vertical dimension.

Up to this point the circuitry described is basically the same as is required to make the VGA run at 2 x PAL rates (see the Application Note AN602,*Theory of Operation for a GSP600 Circuit Operating the VGA Display at 2 x PAL Frequency*). Note that there are an additional 2 line buffers (U3 and U4), 2 RAMDACs (U10 and U1), and 2 current references (U7A, Q1, and Q2). The additional 2 line buffers store the VGA lines before and after the current line being output via U2 and U9. The RGB current outputs from the RAMDACs U10 and U1 are connected together, summing the two sets of RGB currents together. The combined RGB signals from U10 and U1 are then matrixed together in the proper proportions to produce an adjacent-lines luminance signal. This signal amplitude is independent of the main luminance signal so that the ratio of adjacent line to main line luminance can be set to any desired value, primarily by adjusting R1, which controls the reference currents into U10 and U1.

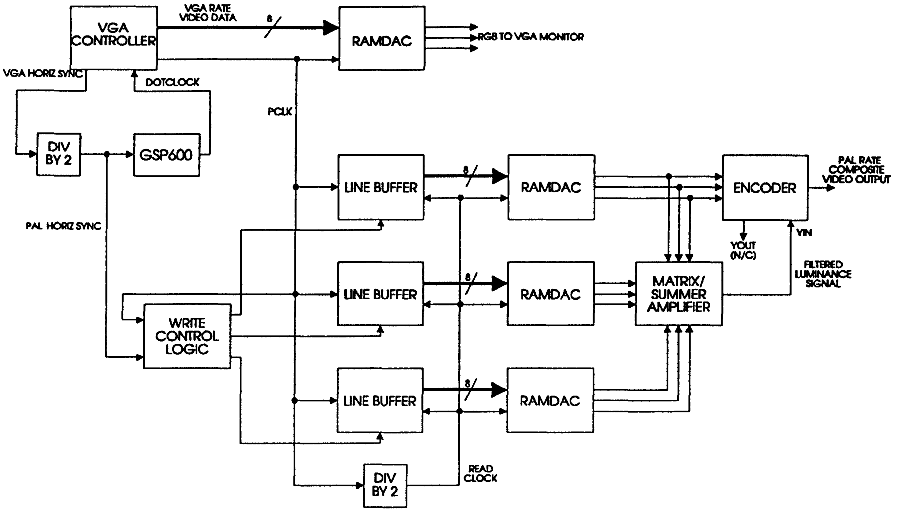


Figure 1

The two luminance signals are connected together, summing them at the input to amplifier U11. U11 then makes up for the resistive losses in the RGB matrices and drives the luminance delay line, whose output is the luminance component of the encoded composite signal. Most encoders have a luminance output and input which allows for an external delay line; not using the output provided while driving the input with an alternate luminance signal of the right amplitude, delay, and polarity allows convenient summing with the chrominance signal generated by the encoder to create the composite video signal.

Programmable logic chip U5 controls the writing of VGA lines into the line buffers such that U2 receives every other line, U3 receives every fourth line, and U4 receives every fourth line, as shown by the timing diagram in Figure 2. Note that only one line buffer is write enabled at a time and every line is written to a line buffer. With this scheme U2 always contains the main VGA line which is going out to the PAL encoder, while U3 and U4 contain the lines adjacent to the main line. The CUPL™ language source code for PLD U5 is included later in this note.

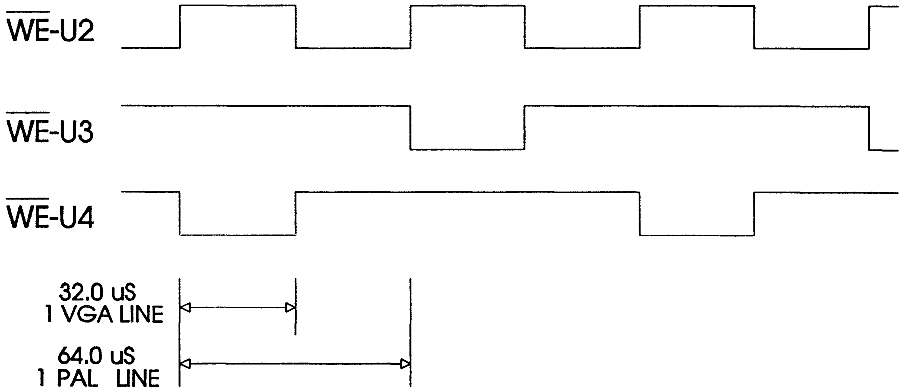


Figure 2

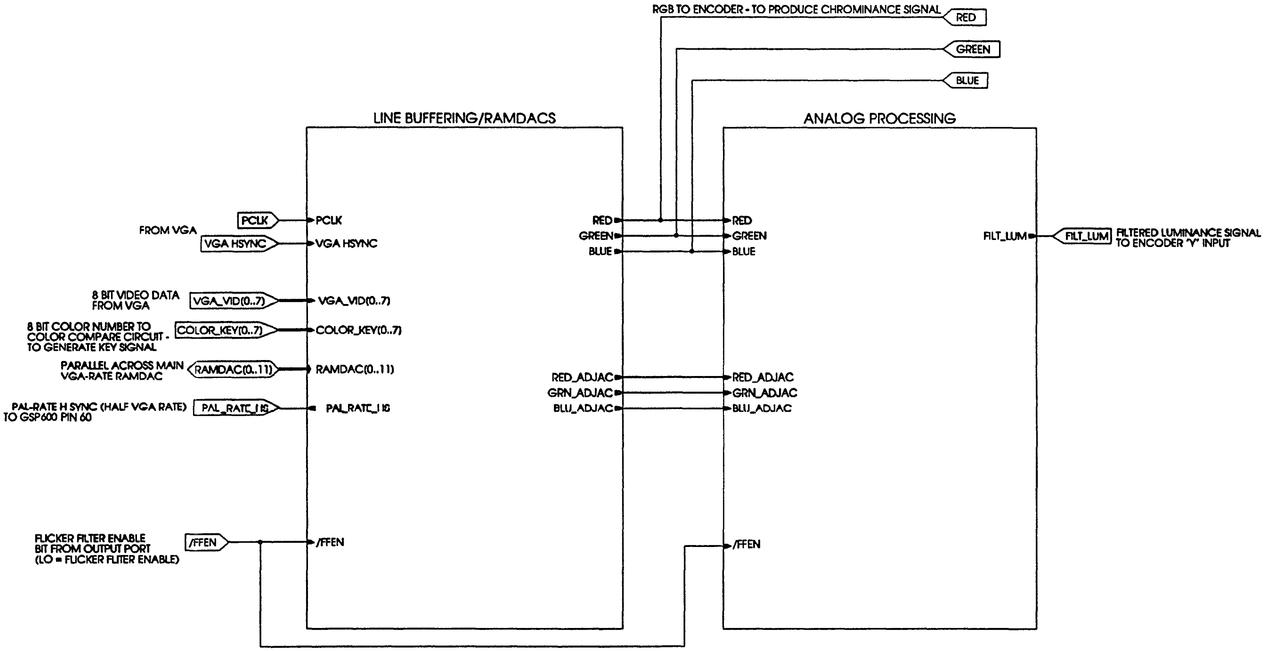
All of the line buffers are continuously read enabled, such that the RGB signal output to the encoder is a combination of the main line and the 2 adjacent line signals. U7A, Q1, and Q2 make up a dual matched current reference for RAMDACs U10 and U1. The amplitude of the adjacent line video signals summed in with the main line is adjustable with R1; the optimum value could be determined so that R1 could be replaced with a fixed divider to save the cost of the trimmer. The amplitude of the main line video signal is controllable by the value of R6 if it is necessary to adjust the proportion of the main line signal that gets summed into the final output. The relative weight of the 2 adjacent line signals in the output is the same due to the matching of the current references into U10 and U1; this should be best for most applications since it is symmetrical about the main line.

The luminance amplitude is controllable by varying the gain of U11 (set by the value of R22); this should normally be set so that luminance levels on any given line are somewhat lower than they would be without filtering. An optional feature shown in the schematic is the ability to switch off the flicker filtering with an I/O bit. Switches Q3 and Q4 turn on when the filter is disabled. In this state Q3 cuts the reference current into U10 and U1, thereby turning off the adjacent line luminance; while Q4 boosts the gain of U11 (by an amount set by R23) to what it should normally be without flicker reduction.

Since when a large area of high luminance level occurs, the video output could exceed the maximum allowed voltage, Q5 and Q6 are used as a positive luminance peak clipper. R27 can be set so that the peak luminance level at the final video output is 714 mV.

BIOS

The video BIOS for the circuit presented here will have to be modified from the typical **GSP600** VGA/PAL system; therefore, register setups for various video modes are given in several tables later in this note.



Flicker Filter Circuit for GSP 600

Figure 3 - Flicker Filter Top Level Schematic

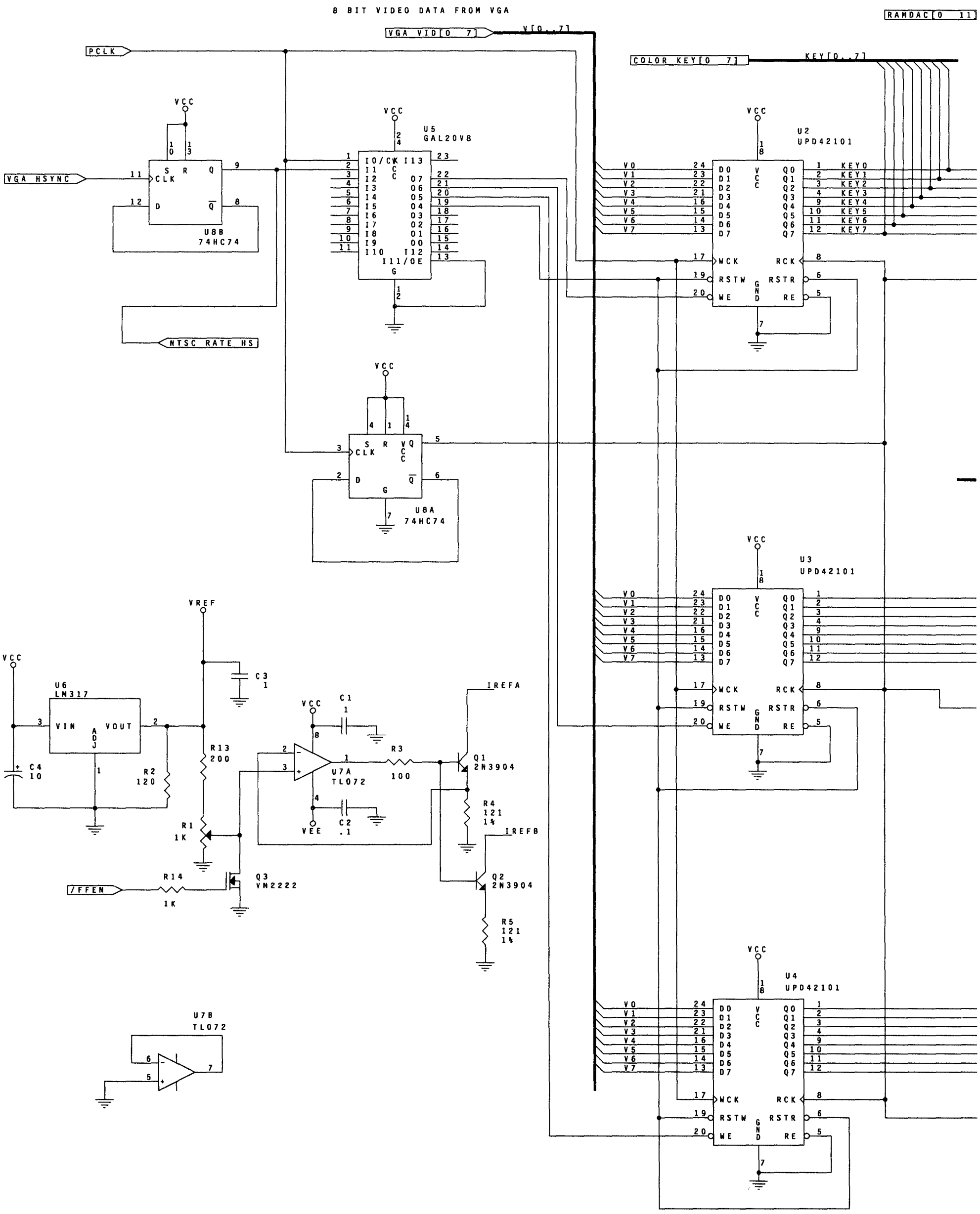
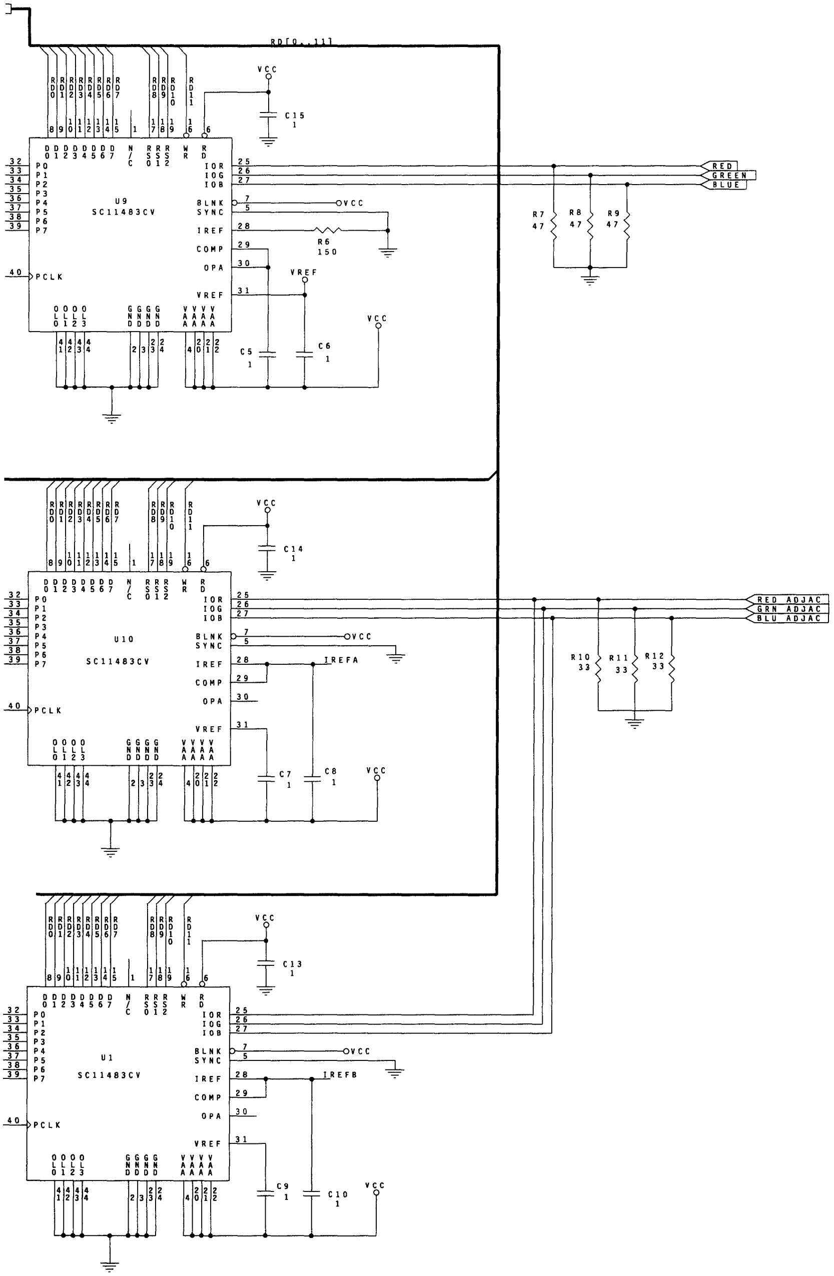

8 BIT VIDEO DATA FROM VGA
VGA VID[0..7]
V[0..7]
RAMDAC[0..11]
PCLK
COLOR KEY[0..7]
KEY[0..7]
VCC
VGA HSYNC
CLK
S
R
Q
D
U8B
74HC74
U5
GAL20V8
I0/CK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I13
O7
O6
O5
O4
O3
O2
O1
O0
I12
I11/OE
NTSC RATE HS
U8A
74HC74
U2
UPD42101
U3
UPD42101
U4
UPD42101
V0
V1
V2
V3
V4
V5
V6
V7
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
KEY0
KEY1
KEY2
KEY3
KEY4
KEY5
KEY6
KEY7
WCK
RSTW
WE
RCK
RSTR
RE
GND
VREF
U6
LM317
VIN
ADJ
VOUT
C4
10
R2
120
C3
1
R13
200
R1
1K
R14
1K
/FFEN
Q3
VN2222
C1
1
C2
.1
VEE
U7A
TL072
R3
100
IREFA
Q1
2N3904
R4
121
1%
IREFB
Q2
2N3904
R5
121
1%
U7B
TL072

Figure 4 -



Flicker Filter Line Buffering/Ramdacs

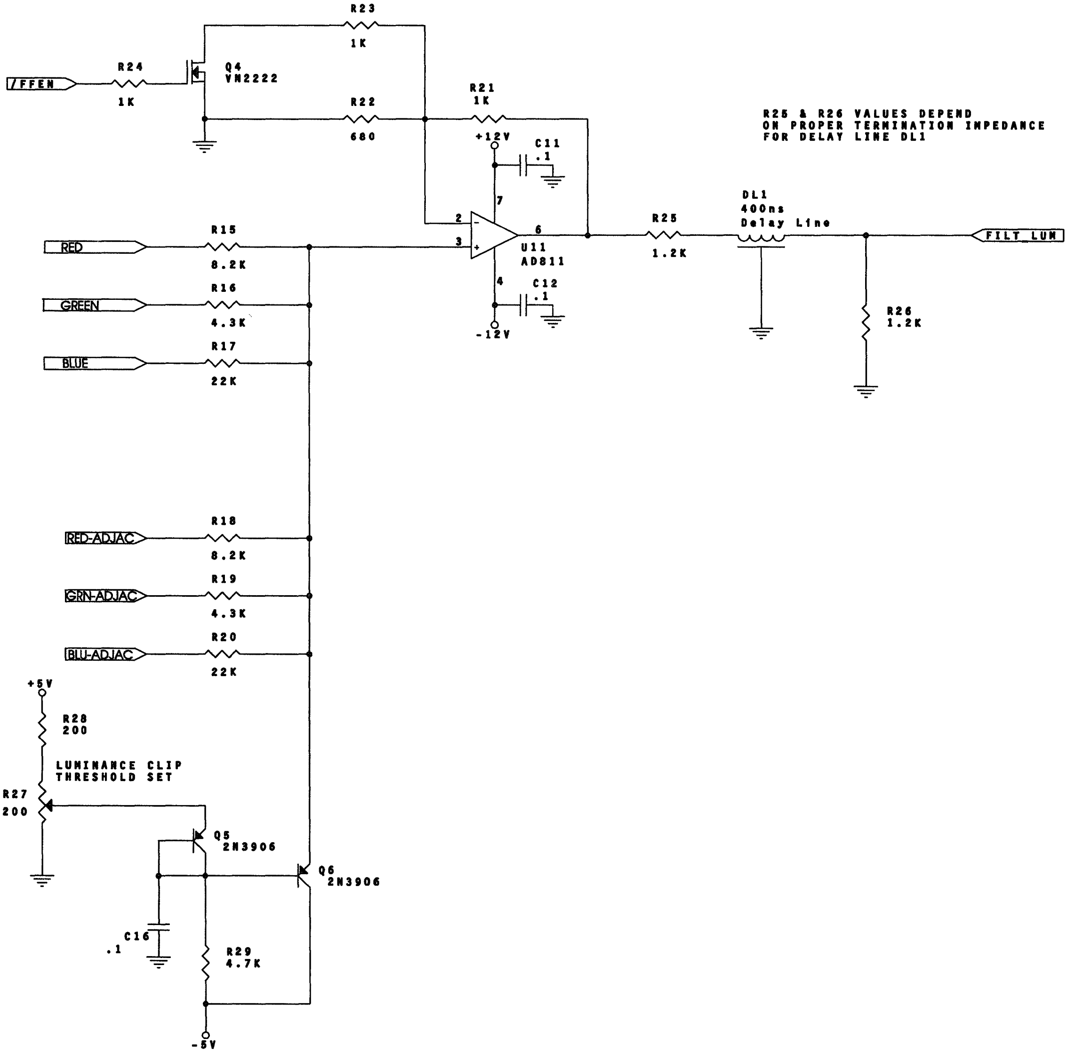


Figure 5 - Flicker Filter Analog Processing

CRTC Registers

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	HT	35	35	6B	6B	35	35	62	6C	35	62	62	62	62	62	62	62
01	HDE	27	27	4F	4F	27	27	4F	4F	27	4F	4F	4F	4F	4F	04	4F
02	SHB	2A	28	57	57	2A	2A	50	54	2A	50	50	50	50	50	50	50
03	EHB	95	96	8B	8B	96	96	85	8B	96	85	85	85	84	84	85	84
04	SHR	2E	2E	5D	5D	2F	2F	58	5D	2F	58	58	58	54	57	58	57
05	EHR	A0	A0	8C	8C	80	80	9B	83	80	9B	9B	9B	82	82	9B	82
06	VT	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B
07	OVERFLOW	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E
08	PRS	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
09	MSL	4F	4F	4F	4F	C1	C1	C1	4F	C0	C0	40	40	40	40	C0	40

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
0A	CS	0D	0D	0D	0D	00	00	00	0D	00	00	00	00	00	00	00	00
0B	CE	0E	0E	0E	0E	00	00	00	0E	00	00	00	00	00	00	00	00
0C	SAH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0D	SAL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0E	CLH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0F	CLL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
10	VRS	BE	BE	BE	BE	C5	C5	C5	BE	C5	C5	A7	A7	F4	F4	C5	EF
11	VRE	22	22	22	22	88	88	88	82	88	88	8B	8B	87	87	88	87
12	VDE	8F	8F	8F	8F	8F	8F	8F	8F	8F	8F	5D	5D	DF	DF	8F	DF
13	OFFSET	14	14	28	28	14	14	28	28	14	28	28	28	28	28	28	50
14	UNDERLINE	1F	1F	1F	1F	00	00	00	1F	00	00	0F	0F	00	00	40	60
15	SVB	B8	B8	B8	B8	C2	C2	C2	B8	C2	C2	9F	9F	E0	E0	C2	E0
16	EVB	E3	E3	E3	E3	05	05	05	E3	05	05	CA	CA	0C	0C	05	0C
17	MC	A3	A3	A3	A3	A2	A2	C2	A3	E3	E3	E3	E3	E3	E3	A3	AB
18	LC	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
*	INTERLACE																

* = Interlace Bit must be turned off for all modes

General Register

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	MISC OUT	#	#	#	#	#	#	#	@	#	#	@	#	#	#	#	#

#	@
23 = GenLock (GL)	22 = GenLock (GL)
27 = OVerlay (OV)	26 = OVerlay (OV)
2B = Video Only (VO)	2A = Video Only (VO)
2F = Graphics Only (GO)	2E = Graphics Only (GO)

Sequence Registers

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	CLK MODE	09	09	01	01	09	09	01	00	09	01	01	01	01	01	01	01

** = 640 x 480 x 256 colors

Source Code for PLD U5 (GAL20V8) in CUPL™ Language

```
Name        ff;
Partno      ff01;
Date        1/20/93;
Revision    01;
Designer    Todd K. Moyer;
Company     Integrated Circuit Systems;
Assembly    Flicker Filter;
Location    U5;

/************************************************************************/
/*                                                                   */
/* VGA @ 2xPAL rate controller with basic line flicker filtering     */
/*                                                                   */
/*                                                                   */
/************************************************************************/
/*                                                                   */
/* Allowable Target Device Types: g20v8                              */
/*                                                                   */
/************************************************************************/

/** Inputs **/

Pin 1        =  clock      ;    /* VGA PCLK signal                  */
Pin 2        =  h_sync_PAL ;    /*                                  */
Pin 12       =  GND        ;
Pin 13       =  !OE        ;
Pin 24       =  VCC        ;

/** Outputs **/

Pin [15..18] =  [HSN_S0..3];    /* used by state machine            */
Pin 19       =  !line_start;    /* pointer reset line mem, act lo   */

Pin 20       =  !write_enable_B;  /*                                */
Pin 21       =  !write_enable_A;  /*                                */
Pin 22       =  !write_enable;    /*                                */

/** Declarations and Intermediate Variable Definitions **/

Field    State_HSync         = [HSN_S0..3];

/** Logic Equations **/
```

```
/** State machine definition **/

Sequence State_HSync
{
      present 0
                    if h_sync_PAL next 1
                          out line_start out line_startAB
                          out write_enable out write_enable_A;
                    if !h_sync_PAL next 0
                          out write_enable;
      present 1
                    if h_sync_PAL next 2
                          out line_start out line_startAB
                          out write_enable out write_enable_A;
                    if !h_sync_PAL next 0;
      present 2
                    if h_sync_PAL next 3
                          out line_start out line_startAB
                          out write_enable out write_enable_A;
                    if !h_synch_PAL next 0;
      present 3
                    if !h_sync_PAL next 4;
                          /* out write_enable; */
                    if h_sync_PAL next 3
                          out write_enable_A;
      present 4
                    if !h_sync_PAL next A;
                    if h_sync_PAL next 3;
      present A
                    if !h_sync_PAL next 5;
                    if h_sync_PAL next 3;
      present 5
                    if h_sync_PAL next 6
                          out line_start out line_startAB
                          out write_enable out write_enable_B;
                    if !h_sync_PAL next 5
                          out write_enable;
      present 6
                    if h_sync_PAL next 7
                          out line_start out line_startAB
                          out write_enable out write_enable_B;
                    if !h_sync_PAL next 5;
      present 7
                    if h_sync_PAL next 8
                          out line_start out line_startAB
                          out write_enable out write_enable_B;
                    if !h_sync_PAL next 5;
      present 8
                    if !h_sync_PAL next 9;
                          /* out write_enable; */
                    if h_sync_PAL next 8
                    out write_enable_B;
```

```
    present 9
                  if !h_sync_PAL next B;
                  if h_sync_PAL next 8;
    present B
                  if !h_sync_PAL next 0;
                  if h_sync_PAL next 8;

    present C
                  next 0;
    present D
                  next 0;
    present E
                  next 0;
    present F
                  next 0;
}
```

Bill of Materials

Item	Qty	Reference	Part
1	15	C1, C2, C3, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16	.1µF
2	1	C4	10µF
3	1	DL1	400 ns
4	2	Q1, Q2	2N3904
5	2	Q3, Q4	VN2222
6	2	Q5, Q6	2N3906
7	5	R1, R14, R21, R23, R24	1K
8	1	R2	120
9	1	R3	100
10	2	R4, R5	121
11	1	R6	150
12	3	R7, R8, R9	47
13	3	R10, R11, R12	33
14	3	R13, R27, R28	200
15	2	R15, R18	8.2K
16	2	R16, R19	4.3K
17	2	R17, R20	22K
18	1	R22	680
19	2	R25, R26	1.2K
20	1	R29	4.7K
21	3	U1, U9, U10	SC11483CV
22	3	U2, U3, U4	UPD42101
23	1	U5	GAL20V8
24	1	U6	LM317
25	1	U7	TL072
26	1	U8	74HC74
27	1	U11	AD811

Integrated Circuit Systems, Inc.

ICS2001

Sound Output Circuit

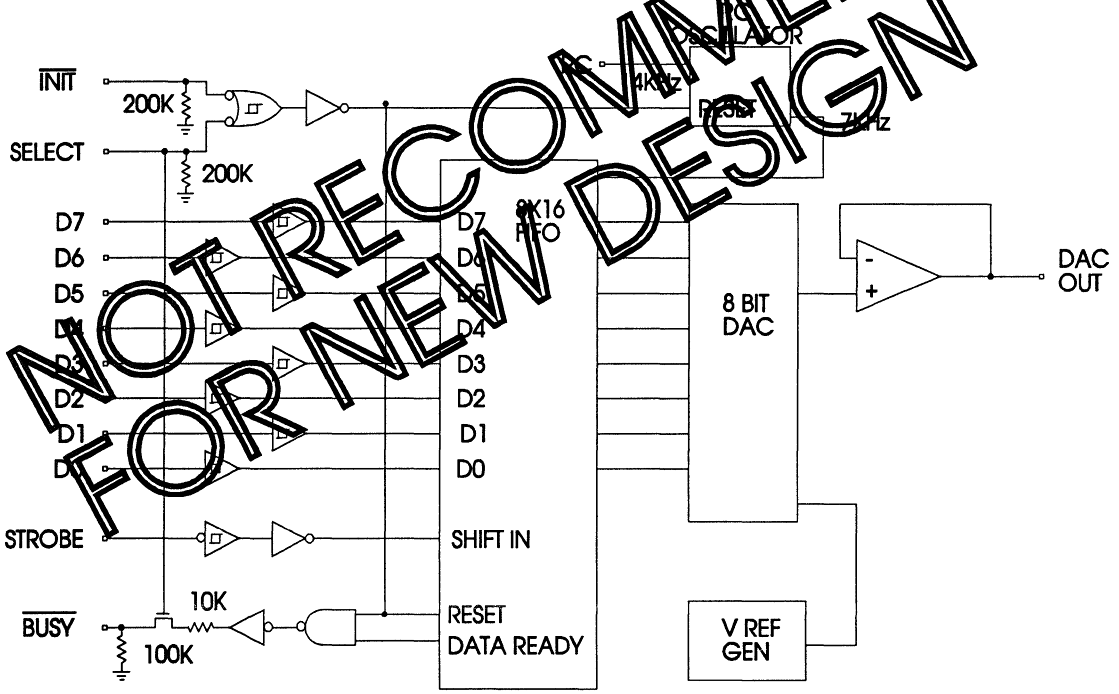
General Description

The **ICS2001** is a CMOS integrated circuit containing an 8-bit digital to analog converter fed by a 16-byte FIFO memory array. This device is intended to form the nucleus of a low-cost audio-output subsystem for personal computers, workstations, games, and talking books. The **ICS2001** is the core of the Disney Sound Source.™

Features

- 8-bit D/A converter
- 16-byte FIFO
- 5V and 9V operation
- TTL-level inputs with hysteresis
- RC clock oscillator
- Software drivers for DOS and Windows

Block Diagram



Sound Source is a trademark of Walt Disney Computer Software Incorporated.

Integrated
Circuit
Systems, Inc.

ICS2002

Wavedec™ Digital Audio Codec

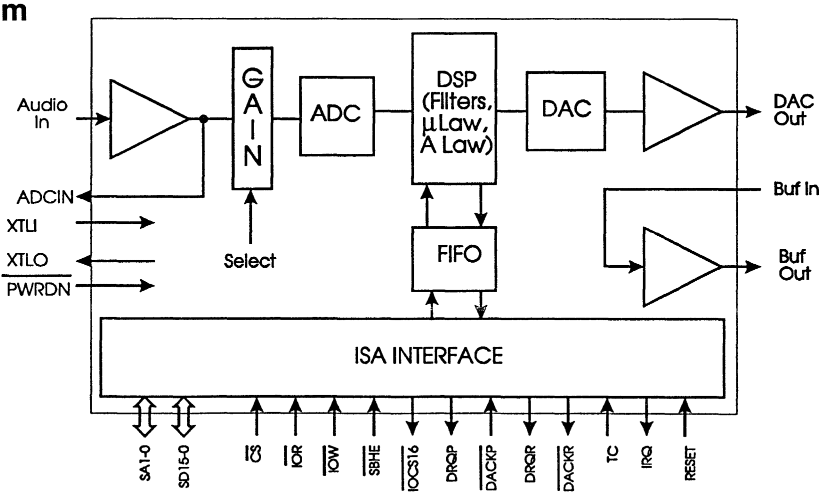
Description

The **ICS2002** is a mixed-signal integrated circuit providing a low-cost recording and playback solution for multimedia audio applications. These applications include document annotation, voice mail, interactive games, multimedia sound record/playback, and Windows™ sound production. The **ICS2002** supports the record and playback of 16-bit audio data, and provides a 8/16-bit parallel interface to the industry standard PC bus.

Features

- Digital audio 8/16-bit record/playback
- Fully programmable sample rates including industry standards:
  - 44.1 kHz
  - 22.050 kHz
  - 11.025 kHz
  - 8.00 kHz
  - 5.513 kHz
- DAC output oversampled to simplify external filtering.
- Four data formats:
  - 16 bit linear
  - 8 bit linear
  - 8 bit u-law
  - 8 bit a-law
- 16 step analog output level control, -1.5dB/step
- 8-bit log scale digital volume control
- Oversampling ADC with input filter.
- Programmable IIR filters for input anti-aliasing and output reconstruction.
- ISA bus interface
- 8/16-bit DMA and I/O transfer modes
- Input/output FIFO buffer
- Power-down mode
- 44-pin PLCC package

Block Diagram

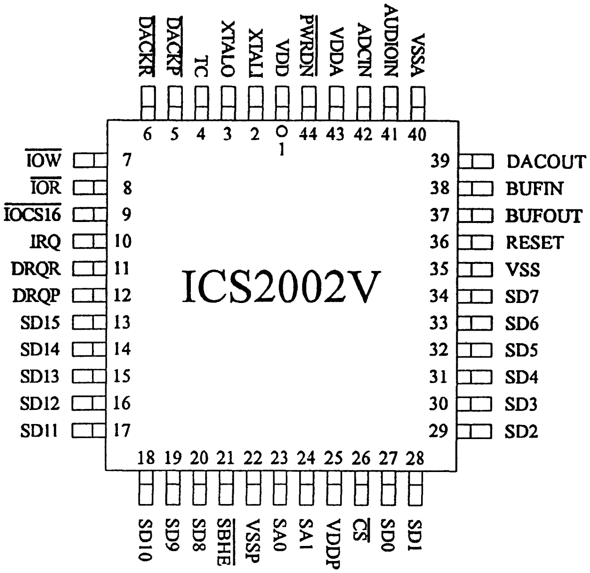


Wavedec is a trademark of Integrated Circuit Systems, Inc

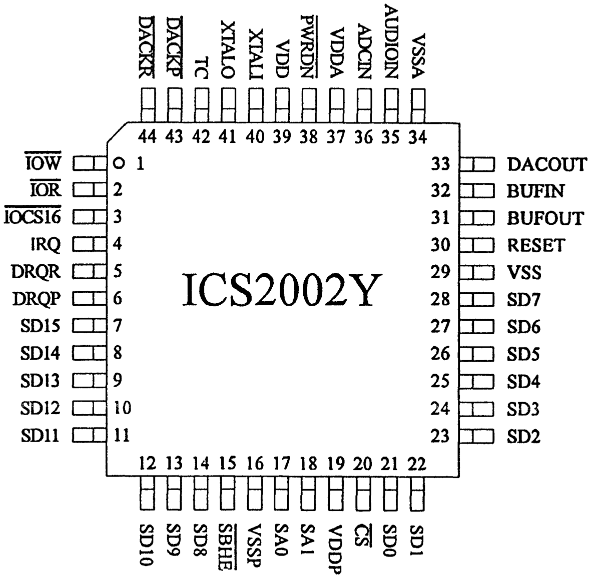
Pin Descriptions

PIN	TYPE	DESCRIPTION
SD15 - SD0	I/O	Data bus
SA1 - SA0	I	Address
$\overline{CS}$	I	Chip select (active low)
$\overline{IOW}$	I	Write strobe (active low)
$\overline{IOR}$	I	Read strobe (active low)
$\overline{SBHE}$	I	System High Byte Enable (active low)
$\overline{IOCS16}$	OC	Indicates that the access register can support 16 bit transfer.
DRQP	O	DMA Request (play channel)
DRQR	O	DMA Request (record channel)
$\overline{DACKP}$	I	DMA Acknowledge (play channel)
$\overline{DACKR}$	I	DMA Acknowledge (record channel)
TC	I	DMA terminal count
IRQ	O	Interrupt request (active high, open drain)
RESET	I	Reset (active high)
XTLI	I	Crystal oscillator
XTLO	O	Crystal oscillator
$\overline{PWRDN}$	I	Power-down (active low)
AUDIOIN	AI	Audio buffer input
ADCIN	AO	Audio buffer output/input to ADC
DACOUT	AO	DAC audio output
BUFIN	AI	Uncommitted audio buffer input
BUFOUT	AO	Uncommitted audio buffer output
VDD	P	Digital +5V supply
VDDA	P	Analog +5V supply
VDDP	P	Digital +5V supply
VSS	P	Digital GND
VSSA	P	Analog GND
VSSP	P	Digital GND

Package Pinout



44-Pin PLCC
K-10



44-Pin TQFP
K-12

Absolute Maximum Ratings

Supply Voltage .... -0.5V to 7.0V
Logic Inputs.................... -0.5V to V_{DD} + 0.5V
Ambient Operating Temperature.......... 0°C to 70°C
Storage Temperature .... -65°C to 150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} = 5.0V ± 10%; GND = 0V; T_A = 0°C to +70°C

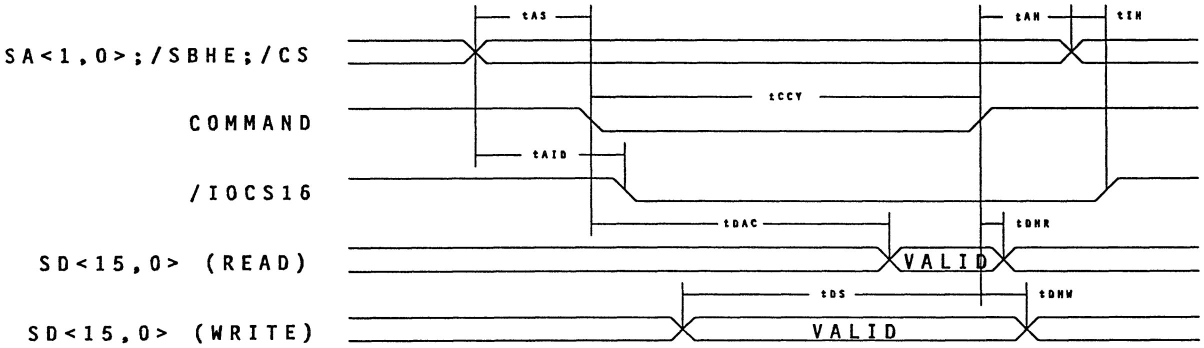
DC/STATIC					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Digital Inputs					
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input High Voltage	V_{IH}	2.0		V_{DD} + 0.3	V
Input Leakage Current	I_{LI}			1	µA
Input Capacitance	C_{IN}			7	pF
Digital Outputs					
Output Low Voltage (I_{OL} = 4.0mA)	V_{OL}			0.4	V
Output High Voltage (I_{OH} = 0.4mA)	V_{OH}	2.4			V
Tristate Current	I_{OZ}			10	µA
Output Capacitance				10	pF
Bi-directional Capacitance				10	pF
Analog Inputs					
Audio Input Voltage			0.7		Vrms
Audio Input Impedance		500k			ohm
Buffer Input Impedance		500k			ohm
Audio Outputs					
Audio Output Voltage			0.7		Vrms
DACOUT, BUFOUT Output Impedance				1k	ohm
Digital Supply Current	I_{CC1}			1	mA
Analog Supply Current	I_{DD2}			35	mA
Power-Down Mode				1	mA
Play Only Mode				15	mA
Record Mode				30	mA

Electrical Characteristics

V_{DD} = 5.0V ± 10%; GND =0V; T_A = 0°C to +70°C

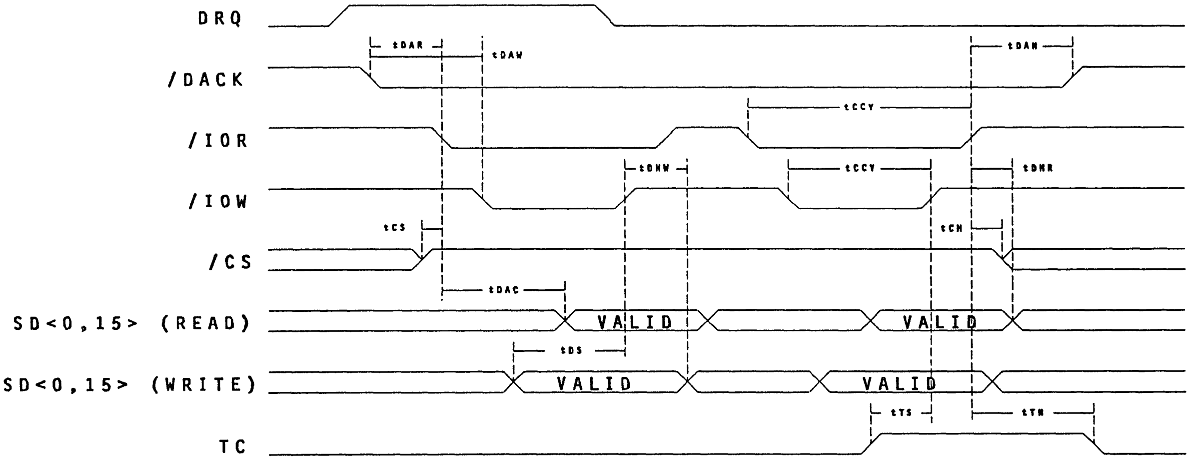
AC/DYNAMIC					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Address setup to command	t_{AS}	10			ns
Address hold from command	t_{AH}	10			ns
Command cycle time	t_{CCY}	100			ns
Address valid to /IOCS16 delay	t_{AID}			50	ns
IOCS16 hold from address invalid	t_{IH}	0			ns
Data valid to /IOW	t_{DS}	50			ns
/IOR active to valid data	t_{DAC}			60	ns
Data hold after /IOR	t_{DHR}	0			ns
Data hold after /IOW	t_{DHW}	10			ns
/DACK setup to /IOR	t_{DAR}	30			ns
/DACK setup to /IOW	t_{DAW}	50			ns
/DACK hold from command	t_{DAH}	50			ns
/CS setup to command	t_{CS}	10			ns
/CS hold from command	t_{CH}	10			ns
TC setup to command inactive	t_{TS}	25			ns
TC hold from command	t_{TH}	0			ns

Timing Diagrams



I/O Cycle Timing

Timing Diagrams



DMA Cycle Timing

Digital Audio Playback

To play digital audio files, the chip is programmed for the desired sample rate, data type, DMA channel width, and output volume.

For DMA mode playback, DRQ generation is programmable for servicing the FIFO at several levels. This allows optimal performance with a variety of hosts. When TC is received, the chip will optionally generate an interrupt to the host to indicate the need to service the DMA controller.

For I/O Mode playback, data is written to the FIFO until it is full. This is determined by polling the "DIR" bit of the status register. Once the FIFO is full, an interrupt will be generated optionally at one of several selectable points: 1/4, 1/2, or 3/4 full. The host can then burst a predetermined amount of data to the FIFO and wait for the next interrupt.

Digital Audio Recording:
Audio recording operates in a DMA or I/O mode similarly to audio playback with the audio input programmable as a line or microphone level input. Simultaneous record and playback is supported and permits the recorded file to be synchronized to an existing file. The new and existing file can then be mixed digitally for high quality results.

Data Processing:
To simplify the external circuitry associated with the analog input and output signals of the chip, input and output sample rates are oversampled. This allows simple RC filters to be used.

For playback, the output data is oversampled, interpolated, filtered and scaled. Since the DSP is fully programmable, various sample rates and filter shapes can be implemented. The processed data is then output to the DAC. The DAC output passes through an analog volume control (4 bits, 1.5dB steps) before being passed to the analog filter stage.

For recording, the input data is first filtered, removing most of the frequency content above the Nyquist frequency. The resulting data stream is then undersampled to the desired sample rate and fed into the FIFO for transfer to the host.

Power Management:
The $\overline{\text{PWRDN}}$ input can be programmed to act as an immediate hardware power control, or as an interrupt source for a software driven power management routine. The software driven option allows the driver to cleanly shut down to chip, thus preventing unwanted noise. When active, the power-down function disables all analog components including the oscillator, and causes the chip to enter a low power mode.

Miscellaneous Functions:
The chip has a full complement of status and control functions. All significant functions are capable of generating interrupts and/or being polled.

The DMA can be run in single or demand mode (for bursts of data in programmed sizes).

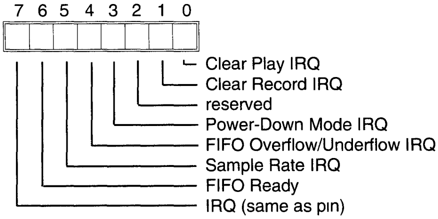
The FIFO has programmable interrupt and DMA request capacities, and also indicates when overflow or underflow conditions occur.

The processor interface is designed for simple connection to the ISA bus. For best noise performance, isolating the data lines from the ISA bus is recommended. In general, feed through of digital noise is reduced by minimizing the load which the digital outputs are driving.

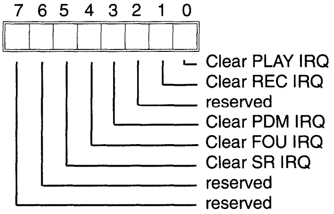
Direct Register Descriptions

The base address is determined externally by an address decoder which selects the chip via the $\overline{CS}$ input.

Status (Base + 0 read)



IRQ Reset (Base + 0 write)



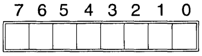
This register provides the driver software easy access to the interrupt source when read. Note that bit 7 indicates the state of the IRQ pin, and hence will be zero when the MIE bit is zero (see "Interrupt Enable" register).

A write to the register is performed to clear interrupts. Writing a one to a given bit will cause the associated interrupt to be cleared. To release the clear interrupt bit and allow further interrupts to occur, a zero must be written back to the bit of interest (some bits have alternate methods of clearing described later). This feature ensures that if the interrupt condition still exists, an edge will be generated on the IRQ pin, thus ensuring recognition on platforms that are edge sensitive. This also allows for a return from interrupt instruction to be executed on the platform while the IRQ line is inactive.

Bit 6 is a special case. There is no IRQ associated with this bit. It is located here for use in Sound Source Emulation Mode, and represents the BUSY status of a Sound Source. When the STATUS is read and tested with 40h, a zero result indicates that the play FIFO is full.

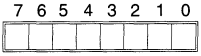
Note that this register can only be read in STAND ALONE mode. Hence, indirect access to this register has been provided at RA=83h for use in COMPANION mode.

Register Address (RA) (Base + 1)

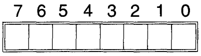


This register is the indirect pointer to direct data transfers to and from the data registers. It is a read/write register. Note that this register can only be read if the chip is in STAND ALONE mode.

Data Low Byte/Word (DLW)



Data High Byte (DH) (Base + 3)



These two addresses are used to accomplish all internal register reading and writing. Most internal registers are 8-bit or less. These are accessed by first writing the appropriate value to the DW, then writing (reading) the data byte to (from) DLW.

I/O Mode FIFO data (RA=0Bh), Algorithm RAM, and Coefficient RAM are always treated as 16-bit entities, and can be transferred in two ways:

- a single operation to/from DLW with $\overline{SBHE}$ = 0
- two successive operations, low byte to/from DLW with $\overline{SBHE}$ = 1, then high byte to/from DH.

Indirect Register Map

Indirect Address	Register
4E	Companion Select Register (write only)
80	Chip Control
81	Interrupt Enables
82	reserved
83	Interrupt status
84	Sample Rate Low 8 bits
85	Sample Rate High 4 bits
86	Sample Rate Control/Status
87	reserved
88	Play DMA Control
89	Play DMA Burst Count
8A	Play DMA Mode
8B	DMA IO Mode Data Port
8C	FIFO Enable/Status
8D	FIFO IRQ Mode
8E	reserved
8F	reserved
90	Power Enable/Status
91	Power Mode
92	reserved
93	reserved
94	DSP Control/Status
95	DSP RAM Address Latch
96	Code RAM Data Port (8/16-bit)
97	Data RAM Data Port (8/16-bit)
98	Record DMA Control
99	Record DMA Burst Count
9A	Record DMA Mode
9B	reserved

Indirect Address	Register
9C	Record FIFO Enable/Status
9D	Record FIFO IRQ Mode
9E	reserved
9F	reserved
A0	Digital Master Volume
A1	DAC Deglitcher Control
A2	reserved
A3	reserved
A4	ADC Control
A5	Analog Volume/Mute
A6	ADC Timing Control
A7	reserved

Indirect Register Definitions

All writeable bits/registers are also readable. In addition, there are some read only bits/registers, which are noted where appropriate.

Reserved bits should be written to zero, and read back zeros. Reserved registers should not be written or read.

Except where noted, registers should be accessed as 8 bit registers via address BASE+2.

General Purpose Registers

IR4E Register Access Mode Select

This register must be written to 01h for any other indirect (or direct) accesses to occur, except for RA writes, which always occur based on chip select. This indirect address allows multiple companion chips to share resources in a system (such as bus buffers, address decodes, interrupts, and DMA channels).

This register is cleared only by hardware reset, and in unaffected by MCR (see below).

IR80 Chip Control

Bits 7:3 - reserved

Bit 2 - Sound Source Emulation Mode (SSMODE)

This bit sets the chip to operate in Sound Source Emulation mode. In Sound Source Emulation Mode, the two address pins (SA1, SA0) are mapped to match the PC parallel port as used by the Sound Source as follows:

Chip Address	Sound Source	IC2002
0	Data	DH
1	Status	Status
2	Control	DL
3	unused	RA

To use this mode, the chip must be configured before the Sound Source compatible application is run (I/O Mode DMA, DSP loaded and running, SR running, etc.). Then, the **IC2002** is put in SSMODE and RA (now at address 3) is written to 8Bh. In the PC, the BIOS pointer to the parallel port is changed to the base address of the **IC2002** chip, and the application can then be started.

This bit is reset by MCR. Hence, it must be set after MCR is set, on a second write to this register.

Bit 1 - Chip STAND ALONE Mode

This bit sets the chip to operate in STAND ALONE mode. In STAND ALONE mode, the STATUS and RA registers are accessible at BASE+0 and BASE+1. This mode should be used to speed register access when the **ICS2002** is being used by itself, without other ICS chips sharing resources (such as address decodes, interrupts, DMA channels, bus buffers, etc.).

When bit 1 is zero, the **ICS2002** will operate in COMPANION mode. In this mode, the STATUS register is mapped only to indirect address 83h. This is done to avoid conflict with other ICS chips that will provide STATUS and RA read back at the first two base addresses.

In addition, STAND ALONE mode configures the DRQP, DRQR, and IRQ pins to operate as outputs, with both one and zero levels being actively driven. When in COMPANION mode, these pins have a strong source for the high state and a weak sink for the low state to allow wire-and connections to other ICS chips.

This bit is reset by hardware reset only, not by MCR.

Bit 0 - Master Chip Reset (MCR)

0 - Hold chip in reset

1 - Remove reset

This bit is cleared to zero by a hardware reset. Thus, any functions reset by MCR are also reset by the RESET pin.

IR81 Interrupt Enables

Bit 7 - Master Interrupt Enable (MIE)
In the zero state, this bit prevents the IRQ pin from going active (high) regardless of the state of any of the individual interrupt sources. It is cleared to zero by MCR. A zero in this bit does not prevent an individual interrupt source from being active in the STATUS register. This allows interrupts to be masked while allowing their status to be polled.

Bit 6 - reserved

Bit 5 - Sample Rate Interrupt Enable (SRIE)

Bit 4 - FIFO Overflow/Underflow Interrupt Enable (FOUIE)

Bit 3 - Power-down Mode Change Interrupt Enable (PMCIE)

Bit 2 - reserved

Bit 1 - Record FIFO Interrupt Enable (RFIE)

Bit 0 - Play FIFO Interrupt Enable (PFIE)
Each of these bits individually enables, one, or disables, zero, their respective interrupt sources from being active in the STATUS register. In addition, there will be no IRQ generated if MIE is one when an individual enable bit is zero. The state of this bit does not affect the source of these interrupts in any way, and they may be polled for activity in the appropriate register for each interrupt type. These bits are all cleared to zero by MCR.

IR83 Status

This register is the same as the direct access status register, except that it can be read in COMPANION mode.

Sample Rate Generator Registers

IR84 Sample Rate Low 8 bits (SRL)

Bits 7:0 - Sample Rate Bits 7:0

IR85 Sample Rate High 4 bits (SRH)

Bits 3:0 - Sample Rate Bits 11:8
Together, these two registers define the record and playback sample rate. Based on the crystal frequency FXtal, and a 12 bit value SR (the concatenation of the two registers), the sample rate will be:

Sample Rate = FXtal * SR / 524288

These registers are **not** initialized by any of the reset mechanisms. Note that the Sample Rate Counter should always be stopped via SRCS bit 0 when these two registers are changed.

IR86 Sample Rate Control/Status (SRCS)

Bits 7:2 - reserved

Bit 1 - Sample Rate Interrupt (SRIRQ) - Read Only
This is set by the hardware whenever the sample rate counter overflows, indicating that a new sample is being input or generated. This bit is cleared by any of the following actions:

- Master Chip Reset
- Sample Rate Run = 0 (SRR bit 0)
- a write to STATUS with bit 5 = 1
- any write to SRCS

Bit 0 - Sample Rate Run (SRR)
This bit resets the Sample Rate Counter, the SRIRQ bit, and shuts down the sampling and playback pro-cesses when written to a zero. When written to a one, the sample rate generator runs at the programmed rate. SRR is internally synchronized to the master clock to provide clean starts and stops of the counter. MCR clears this bit.

Play DMA Control and Status Registers

IR88 Play DMA Control (DMACTL)

Bits 7 - reserved

Bit 6 - TC Reset Mask

When set to 1, this bit masks the 'DMA Run' bit reset upon receipt of TC, terminal count, signal from the ISA bus. When reset to 0, the 'DMA Run' bit will be reset upon receipt of TC.

Bits 5:1 - reserved

Bit 0 - DMA Run

This bit enables the DMA hardware to begin transferring data when set to one. It is cleared by either MCR or receipt of a TC when 'TC Reset Mask' is a zero (see the DMAMODE register for details).

IR89 Play DMA Burst Count (DMABC)

Bits 7:6 - reserved

Bits 5:0 - DMA Burst Count

This value determines the number of DMA transfers that take place for each DMA request issued to the host. The actual number of transfers will be DMABC+1. Thus, for single transfer mode, program this register to zero. The burst counter is automatically preset to the burst count whenever the DACKP input is high. Thus, there is no need to reprogram the count value after TC, since the next transfer will use the full programmed count value. This register has no affect on I/O Mode data transfers, since its only influence is over the DRQP output. This register is not initialized by any means other than a direct write, and hence must be written to before DMA is enabled.

IR8A Play DMA Mode (DMAMODE)

All bits in this register are cleared by MCR.

Bits 7:6 - reserved

Bit 5 - Terminal Count Interrupt (TCIRQ) - (read only)

This bit indicates that a Terminal Count has been received on the last DMA operation. If the PFIE and PLAYIRQ bits have been programmed to a one, an interrupt will be generated at the end of the last DMA operation. This bit is cleared by MCR or a write to STATUS with bit 0 = one. The reset state is then removed by either writing the STATUS bit 0 to zero.

Bit 4 - I/O Mode Transfer (IOXFER)

When this bit is a one, the DMA hardware (DRQP and TCIRQ) is disabled. Data transfers take place via IR8Bh, and are required to be treated as 16-bit transfers. Thus, data should be written to DLW (with SBHE = low, 16-bit data) or to DLW (with SBHE = high, 8-bit data low byte) followed by DH (8-bit data, high byte). It is also the programmers responsibility to ensure that DMAMODE bit 2 (DMA16) is set to a one for all I/O mode transfers.

Bit 3 - Unsigned Data (USIGN)

When set to a one, this bit expects to receive (and will generate) unsigned data. The native data format is Signed Binary Twos Complement. This bit will invert the most significant bit of each data byte (or word, depending on the state of DATATYPE). Note that this bit should be zero when the DATATYPE indicates u-law or A- law data formats.

Bit 2 - 16 Bit Data (DMA16)

When set to a one, this bit causes the hardware to expect data to be sent in 16-bit words. When low, the hardware expects 8-bit bytes. This bit must be set to one when performing I/O mode transfers, as all I/O transfers are treated as 16 bit values.

Bit 1:0 - Data Type (DATATYPE)

These bits direct the hardware how to interpret the outgoing data. This is independent of the DMA or I/O data width. It effects how data is signed and how data is packed to and unpacked from the Play FIFO. The DATATYPE field selects the format of data for playback.

Value	Data Type
00	8-bit linear
01	16-bit linear
10	8-bit µ256 Law
11	8-bit A-Law

IR8B DMA I/O Mode Data Port (DMADATA) (8/16-bit)

This register address is used to trap I/O mode data to and from the FIFOs. It is only used in I/O mode. See the description of the IOXFER bits for more details.

When DMA16 is one, this register MUST be accessed as a sixteen bit value. Note that this can be done from either an eight or sixteen bit ISA slot, since the chip used SBHE to determine the proper byte swapping.

FIFO Control/Status Registers

IR8C FIFO Enable/Status (FES)

Bit 0 - FIFO Enable (FE)

This bit holds the FIFO in a reset state when low, and enables the FIFO to operate when high. This bit is reset by MCR. This bit, when low, also resets all FIFO related conditions (see the following bits) and prevents DMA start requests from being issued. It does not reset the FIFO IRQ Mode register.

Bit 1 - FIFO Overflow (read only)

This bit is set when a FIFO shift in command is generated (by either DMA, I/O, or the DSP) with the FIFO full, and indicates an error condition. This bit will cause the FOUIRQ bit to go active, generating an IRQ if enabled. This bit is reset by writing to STATUS with bit 4 = 1, and re-enabled by writing to STATUS with bit 4 = 0. FE low also resets this bit.

Bit 2 - FIFO Underflow (read only)

This bit is set when a FIFO shift out command is generated (by either DMA, I/O, or the DSP) with the FIFO empty, and indicates an error condition. This bit will cause the FOUIRQ bit to go active, generating an IRQ if enabled. This bit is reset by writing to STATUS with bit 4 = 1, and re-enabled by writing to STATUS with bit 4 = 0. FE low also resets this bit.

Bit 3 - FIFO 25% Full (read only)

This bit goes high after 4 words (or 8 bytes) have been loaded into the FIFO, and low again when 13 words (or 26 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 4 - FIFO 50% Full (read only)

This bit goes high after 8 words (or 16 bytes) have been loaded into the FIFO, and low again when 9 words (or 18 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 5 - FIFO 75% Full (read only)

This bit goes high after 12 words (or 24 bytes) have been loaded into the FIFO, and low again when 5 words (or 10 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 6 - FIFO DIR (read only)

This bit goes high when a single word (or two bytes) may be written to the FIFO. There is no interrupt associated with this bit directly. Note that this bit resets to a one because when the FIFO is reset it is forced to be empty, and hence is ready to accept data.

Bit 7 - FIFO DOR (read only)

This bit goes high when a single word (or two bytes) may be read from the FIFO. There is no interrupt associated with this bit directly.

IR8D FIFO IRQ Mode

This register must never be written to when the FIFO is enabled. Invalid interrupts and DMA requests could be generated as a result.

Bits 7:4 - reserved

Bit 3 - FIFO IRQ Enable (FIE)

This bit enables the various FIFO capacity thresholds to generate interrupts (as PLAYIRQ) when one. When zero, this bit prevents FIFO capacity IRQ generation when operating in DMA mode, which only needs TCIRQ.

Bits 2:0 - FIFO Ready IRQ Mode Selection

This field defines FIFO utilization for both DMA and I/O mode data transfers. In I/O mode, it is used to generate interrupts (FRDYIRQ) when the FIFO capacity reaches a predefined point. For DMA transfers, it signals the DMA logic to request a transfer at those same predefined points. By programming the DMA Burst Count appropriately, the FIFO may be easily kept near the desired capacity.

The following table describes the selections available:

Bits 2:0	IRQ/DRQ Source	Notes
000	DIR	Ready to take 1 word from HOST
001	EMPTY 75%	Ready to take 13 words from HOST
010	EMPTY 50%	Ready to take 9 words from HOST
011	EMPTY 25%	Ready to take 5 words from HOST
100	DOR	Ready to provide 1 word to DSP
101	FULL 25%	Ready to provide 4 words to DSP
110	FULL 50%	Ready to provide 8 words to DSP
111	FULL 75%	Ready to provide 12 words to DSP

Note that for byte transfers (DMA16=0), the numbers listed above should be doubled.

This must be programmed before the FIFO is enabled. It may be changed while the FIFO is enabled, if necessary. This register is cleared by MCR, but not by FE low.

IR8E reserved

IR8F Play FIFO Output Data Read Back (8/16 bit)

This register is provided for test use only, although it may find system level use as a diagnostic tool.

Power Control and Status

IR90 Power Enable/Status (PEST)

Bit 7 - PWRIRQ (read only)

This bit is a one when either edge has occurred on the $\overline{\text{PWRDN}}$ pin, and the edge enable in the Power Mode register is set. If bit 3 of the MIE is one, this will also generate an external interrupt. In any case, this bit is also visible as STATUS register bit 3. PWRIRQ is reset by disabling both edge enable bits or resetting the edge interrupts (see below).

Bits 6:5 - reserved

Bit 4 - ADCPWR Disable

This bit controls the power state of the ADC analog circuitry. When 0, ADC analog power is controlled by the SOFTPWR bit the same as the DAC analog power is. When this bit is set to a 1, the ADC analog power is turned off independent of the state of SOFTPWR.

This feature is included for advanced power management routines, as chip power dissipation can be reduced by almost half by turning ADC power off when not in use. Note, however, that several milliseconds of settling time is required after power is turned on before the ADC functions properly.

Bit 3 - $\overline{\text{PWRDN}}$ Pin Value (read only)

This bit indicates the state of the $\overline{\text{PWRDN}}$ pin.

Bit 2 - FALLIRQ (read only)

This bit is set when the $\overline{\text{PWRDN}}$ pin makes a transition from high to low. If PWRMODE bit 2 (FALLIE) is one, this will cause PWRIRQ to go high as well. This bit is reset by one of the following:

- MCR
- any write to PEST
- a write to STATUS with bit 3 set to one. This will hold the bit reset until released by a write to STATUS with bit 3 cleared to zero.

Note that FALLIE does not mask this bit, allowing polling to be performed.

Bit 1 - RISEIRQ (read only)

This bit is set when the $\overline{\text{PWRDN}}$ pin makes a transition from low to high. If PWRMODE bit 1 (RISEIE) is one, this will cause PWRIRQ to go high as well. This bit is reset by one of the following:

- MCR
- any write to PEST
- a write to STATUS with bit 3 set to one. This will hold the bit reset until released by a write to STATUS with bit 3 cleared to zero.

Note that RISEIE does not mask this bit, allowing polling to be performed.

Bit 0 - Soft Power (SOFTPWR)

The function of this bit depends on the status of the "SWMODE" bit (bit 0 of PWRMODE). When SWMODE is zero, writes to this bit have no affect. Reads will return the state of the PWRDN* pin, which is also the state of the on chip PWRON control signal. When SWMODE is a one, a write of one to this bit turns on power to the chip analog circuitry, while a zero clears this bit and puts the chip in a low power mode. Reads will return the last value written.

IR91 Power Mode (PWRMODE)

All bits in this register are cleared by MCR.

Bits 7:3 - reserved

Bit 2 - Fall IRQ Enable (FALLIE)

When set to one, this bit allows a falling edge on $\overline{\text{PWRDN}}$ to cause PWRIRQ to go high. It does not mask PEST bit 2.

Bit 1 - Rise IRQ Enable (RISEIE)

When set to one, this bit allows a rising edge on $\overline{\text{PWRDN}}$ to cause PWRIRQ to go high. It does not mask PEST bit 1.

Bit 0 - Software Mode (SWMODE)

When cleared to zero, this bit causes the chip to operate in a "hardware driven" mode; that is, the $\overline{\text{PWRDN}}$ pin directly controls the chip analog power (for low power consumption). In this mode, a low on $\overline{\text{PWRDN}}$ puts the chip in low power mode, while a high enables normal operation. When set to a one, this bit causes the chip to operate in a "software driven" mode. In this mode, changes on the $\overline{\text{PWRDN}}$ pin only generate interrupts. The hardware low power mode is then controlled (via software) by SOFTPWR (bit 0 of PEST). This function allows "clean" software controlled turn on and off of the analog circuitry power.

IR92 reserved

IR93 reserved

IR94 DSP Control/Status (DSPCS)

Bits 7:4 - Index Counter Value (Read Only)

This value indicates the current contents of the DSP address Index Counter, and is provided as a code debug aid for use in Step Mode. In normal operation it should be ignored. It is reset to zero when the DSP is not running, and increments by one at the completion of each "pass" of the DSP engine.

Bit 3 - DSP Sequence Complete (Read only)

This bit is set each time the DSP completes its sequence and restarts. It is reset to zero when the DSPRUN bit is zero or after a read of this register.

Bit 2 - DSP Output Saturation Detect

This bit is set to one whenever the DSP output value written to any output destination (DATA RAM, DAC, or Record FIFO) exceeds a sixteen bit signed range. In these cases, the DSP output saturates to $7FFF or $8000 (for positive or negative values) rather than overflowing. It is reset to zero when the DSPRUN bit is zero or after a read of this register.

Bit 1 - DSP Step Mode

This bit is intended as a DSP code debug aid only. When set to a one, this bit halts the DSP microcode sequencer at the end of each "pass" of code. This enables the host to read the DATA RAM contents to check the results of the previous calculations. Note that writes to the Record FIFO and DAC will be captured by the DATA RAM "under" them to aid with debug efforts. For normal operation, this bit **MUST** be set to a zero.

Bit 0 - DSP Run

When written to one, this bit starts the DSP engine running. A zero stops and resets the DSP engine execution. This bit is reset by MCR.

Before running the DSP, the Code and Data RAMs must be loaded. To do this, perform the following:

1) write 95h (DSPRA) to the desired address
2) write 96h (Code Ram data) or 97h (Data RAM data) to the desired 16-bit value.
3) repeat 1 and 2 for all RAM locations of both RAMs.
4) when done, write any data to DSPRA to reset the load logic.

ICS will provide algorithm and constants data supporting filtering functions for various sample rates.

Note that when the DSP is running, it is forbidden to read or write either the Code or Data RAMs (except when halted in STEP mode, see above). Also, after writing to the Code or Data RAMs to load them, and before starting the DSP, you must reset the RAM load hardware by writing to the DSPRA register (the value written is ignored).

IR95 DSP RAM Address Latch (DSPRA) (write only)

Bit 7 - Read

When one, this bit indicates that the next DSP RAM operation is a read. Zero indicates a write operation.

Bits 5:0 - DSP RAM Address

These bits are the address for the next DSP RAM data transfer. Note that the Code RAM address can be $00 through $3f, and the Data RAM address can be $00 through $1F.

IR96 Code RAM Data Port (8/16-bit)

Bits B:0 - Code RAM Data

This 8/16-bit port is data to be read from/written to the DSP Code RAM. The data is the low 12 bits of the word.

IR97 Data RAM Data Port (8/16-bit)

Bits F:0 - Data RAM Data

This 8/16-bit port is the data to be read from/written to the DSP Data RAM. The data is a full 16-bit word.

Record DMA Control and Status Registers

IR98 Record DMA Control (DMACTL)

Bits 7 - reserved

Bit 6 - TC Reset Mask

When set to 1, this bit masks the 'DMA Run' bit reset upon receipt of TC, terminal count, signal from the ISA bus. When reset to 0, the 'DMA Run' bit will be reset upon receipt of TC.

Bits 5:1 - reserved

Bit 0 - DMA Run

This bit enables the DMA hardware to begin transferring data when set to one. It is cleared by either MCR or receipt of a TC when 'TC Reset Mask' is a zero (see the DMAMODE register for details).

IR99 Record DMA Burst Count (RDMABC)

Bits 7:6 - reserved

Bits 5:0 - Record DMA Burst Count

This value determines the number of DMA transfers that take place for each DMA request issued to the host. The actual number of transfers will be RDMABC + 1. Thus, for single transfer mode, program this register to zero. The burst counter is automatically preset to the burst count whenever the $\overline{DACKR}$ input is high. Thus, there is no need to reprogram the count value after TC, since the next transfer will use the full programmed count value. This register has no affect on I/O Mode data transfers, since its only influence is over the DRQR output. This register is not initialized by any means other than a direct write, and hence must be written to before DMA is enabled.

IR9A Record DMA Mode (RDMAMODE)

All bits in this register are cleared by MCR.

Bits 7:6 - reserved

Bit 5 - Terminal Count Interrupt (RTCIRQ) (read only)

This bit indicates that a Terminal Count has been received on the last DMA operation. If the RECIE bit has been programmed to a one, an interrupt will be generated at the end of the last DMA operation. This bit is cleared by MCR or a write to STATUS with bit 1 = 1. The reset state is then removed by either writing the STATUS bit 0 to 0, or by the next DMA operation. Hence, there is no need to "remove" this reset as there is for other IRQ reset operations.

Bit 4 - Record I/O Mode Transfer (RIOXFER)

When this bit is a one, the DMA hardware (DRQR and RTCIRQ) is disabled. Data transfers take place via RA $8B (NOT $9B), and are required to be treated as 16-bit transfers. Thus, data should be read from DLW (with $\overline{SBHE}$ = 0, 16-bit data) or from DLW (with $\overline{SBHE}$ = 1, 8-bit data low byte) followed by DH (8-bit data, high byte). It is also the programmers responsibility to ensure that RDMAMODE bit 1 (RDMA16) is set to a one for all I/O mode transfers.

Bit 3 - Unsigned Data (RUSIGN)

When set to a one, the record FIFO will generate unsigned data. The native data format is Signed Binary Twos Complement. This bit will invert the most significant bit of each data byte (or word, depending on the state of RDATATYPE).

Bit 2 - 16-Bit DMA (RDMA16)

When set to a one, this bit causes the hardware to expect data to be sent in 16-bit words. When low, the hardware expects 8-bit bytes. This bit must be set to one when performing I/O mode transfers, as all I/O transfers are treated as 16-bit entities.

Bits 1:0 - Record Data Type (RDATATYPE)

These bits direct the hardware how to interpret the incoming data. Note that this is independent of the DMA or I/O data width. It effects how data is "signed" and how data is packed to/unpacked from the Record FIFO.

Value	Data Type
00	8-bit linear
01	16-bit linear
10	reserved
11	reserved

IR9B reserved

Record FIFO Control/Status Registers

IR9C Record FIFO Enable/Status (RFES)

Bit 0 - Record FIFO Enable (RFE)

This bit holds the record FIFO in a reset state when low, and enables the FIFO to operate when high. This bit is reset by MCR. This bit, when low, also resets all FIFO related conditions (see the following bits) and prevents DMA start requests from being issued. It does not reset the Record FIFO IRQ Mode register.

Bit 1 - FIFO Overflow (read only)

This bit is set when a FIFO shift in command is generated (by either DMA, I/O, or the DSP) with the FIFO full, and indicates an error condition. This bit will cause the FOUIRQ bit to go active, generating an IRQ if enabled. This bit is reset by writing to STATUS with bit 4 = 1, and re-enabled by writing to STATUS with bit 4 = 0. FE low also resets this bit.

Bit 2 - FIFO Underflow (read only)

This bit is set when a FIFO shift out command is generated (by either DMA, I/O, or the DSP) with the FIFO empty, and indicates an error condition. This bit will cause the FOUIRQ bit to go active, generating an IRQ if enabled. This bit is reset by writing to STATUS with bit 4 = 1, and re-enabled by writing to STATUS with bit 4 = 0. FE low also resets this bit.

Bit 3 - FIFO 25% Full (read only)
This bit goes high after 4 words (or 8 bytes) have been loaded into the FIFO, and low again when 5 words (or 10 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 4 - FIFO 50% Full (read only)
This bit goes high after 8 words (or 16 bytes) have been loaded into the FIFO, and low again when 9 words (or 18 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 5 - FIFO 75% Full (read only)
This bit goes high after 12 words (or 24 bytes) have been loaded into the FIFO, and low again when 13 words (or 26 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 6 - FIFO DIR (read only)
This bit goes high when a single word (or two bytes) may be written to the FIFO. There is no interrupt associated with this bit directly. Note that this bit resets to a one because when the FIFO is reset it is forced to be "empty," and hence is ready to accept data.

Bit 7 - FIFO DOR (read only)
This bit goes high when a single word (or two bytes) may be read from the FIFO. There is no interrupt associated with this bit directly.

IR9D Record FIFO IRQ Mode

Bits 7:4 - reserved

Bit 3 - FIFO IRQ Enable (RFIE)
This bit enables the various FIFO capacity thresholds to generate interrupts (as RECIRQ) when one. When zero, this bit prevents FIFO capacity IRQ generation when operating in DMA mode, which only needs RTCIRQ.

Bits 2:0 - FIFO Ready IRQ Mode Selection
This register defines FIFO utilization for both DMA and I/O mode data transfers. In I/O mode, it is used to generate interrupts (RECIRQ) when the FIFO capacity reaches a predefined point. For DMA transfers, it signals the DMA logic to request a transfer at those same predefined points. By programming the Record DMA Burst Count appropriately, the FIFO may be easily kept near the desired capacity.

The following table describes the selections available:

Bits 2:0	Source	Notes
000	DIR	Ready to take 1 word from DSP
001	EMPTY 75%	Ready to take 13 words from DSP
010	EMPTY 50%	Ready to take 9 words from DSP
011	EMPTY 25%	Ready to take 5 words from DSP
100	DOR	Ready to provide 1 word to HOST
101	FULL 25%	Ready to provide 4 words to HOST
110	FULL 50%	Ready to provide 8 words to HOST
111	FULL 75%	Ready to provide 12 words

Note that for byte transfers (RDMA16=0), the numbers listed above should be doubled.

This must be programmed before the FIFO is enabled. It may be changed while the FIFO is enabled if necessary. This register is cleared by MCR, but not by RFE low.

IR9E reserved

IR9F reserved

Miscellaneous Registers

IRA0 Digital Master Volume

Bits 7:0 - Volume
This value is used to scale all values that are output from the DSP to the DAC. It may be written while the DSP is running.

The value written is interpreted as to give a log scale output response of 0.1875dB per step. The value for nominal (0dB attenuation) is E0h. A value of FFh gives 5.8125dB of gain. Note that any value above E0h may result in digital saturation of the internal 16 bit data value.

IRA1 DAC De-glitcher Control

Bits 7:3 - Volume bits 7:3 (read only)

Bit 2 - DAC Enable Bit (read only, for test)

Bits 1:0 - DAC De-glitch Width

Code	Notes
00	De-glitcher disabled
01	Minimum de-glitch width
10	Nominal de-glitch width
11	Maximum de-glitch width

This value is determined by the clock rate at which the chip is run. ICS will provide the proper value for an application. This register is also used for test purposes.

This register is not initialized in any way and should be programmed before muting is removed.

IRA2 reserved

IRA3 reserved

ADC and Analog Control Registers

IRA4 ADC Control

Bits 7:3 - reserved

Bit 2 - ADC Test Mode

This bit is for factory testing use only, and must always be programmed to zero by an application. It is reset to zero by a zero in ADCRUN, and hence takes two writes of $05 to this register to activate for safety.

Bit 1 - reserved

Bit 0 - ADC Run

When written to a one, this bit enables the ADC hardware to run. Note that the ADC Timing Control register should be programmed appropriately first. Also note that the DSP must be running (and programmed properly) for the conversion results to be retrieved. The Sample Rate Generator determines the rate at which the conversion data is loaded into the Record FIFO.

This bit is cleared to zero by MCR.

Note that this bit, when 0, shuts down the successive approximation logic, the dynamic comparators and various logic functions. When the ADC is not being used, disabling it via this bit reduces background noise in the playback section and power consumption, and thus is recommended.

IRA5 Analog Volume/Mute

Bits 7:5 - reserved

Bits 4:1 - Analog Volume

These bits set the analog output level, in 1.5dB steps. All bits one gives 0dB attenuation of the DAC output signal, and all bits zero gives full attenuation. These bits are unaffected by any reset mechanism.

Bit 0 - Audio Enable

This bit disconnects the audio output of the output buffer amp and sets the BUFOUT pin to the nominal bias voltage when cleared to zero. When set to one, it passes the output of the output buffer amp to the BUFOUT pin.

The main function of this bit is to prevent sudden DC offset changes on the BUFOUT pin when entering and leaving power-down mode. By proper software procedure, noiseless transitions can be made.

This bit is cleared to zero by MCR.

IRA6 ADC Timing Control

This register is used to control the ADC internal operation timing.

Bits 7:4 - Comparator Timing Control

These bits control the time of comparator input switching. Bits 7:5 are the count, and bit 4 is 0 for half cycle and 1 full cycle delays.

Bits 3:1 - Cycle Timing Control

These bits control the number of clocks used for each step of the successive approximation process. For the full 64 step DSP cycle, the value of these bits should be 7. For a 40 step cycle, the value should be 4.

Bit 0 - reserved

Ordering Information

ICS2002V or ICS2002Y

Example:

ICS XXXX M

Package Type
V=PLCC; Q=QFP
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated Circuit Systems, Inc.

ICS2008A

Advance Information

SMPTE Time Code Receiver/Generator

General Description

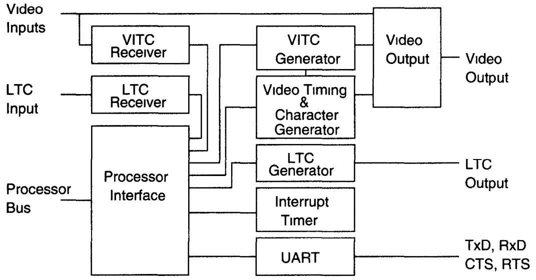
The **ICS2008A**, SMPTE Time Code Receiver/Generator chip, is a VLSI device designed in a low power CMOS process. This device provides the timing coordination for Multimedia sight and sound events. Although it is aimed at a PC Multimedia environment, the **ICS2008A** is easily integrated into products requiring SMPTE time code generation and/or reception in LTC (Longitudinal Time Code) and/or VITC (Vertical Interval Time Code) formats and MTC (MIDI Time Code) translation.

Taking its input from composite video, S-Video, or an audio track, the **ICS2008A** can read SMPTE time code in VITC and LTC formats. Time code output formats are LTC and VITC. All are available simultaneously. A UART is provided for the user to support MTC or tape transport control.

The processor interface is compatible with the IBM PC and ISA bus compatible computers and is easily interfaced to other processors.

The **ICS2008A** is an improved version of the **ICS2008**, with additional features and capabilities.

Block Diagram



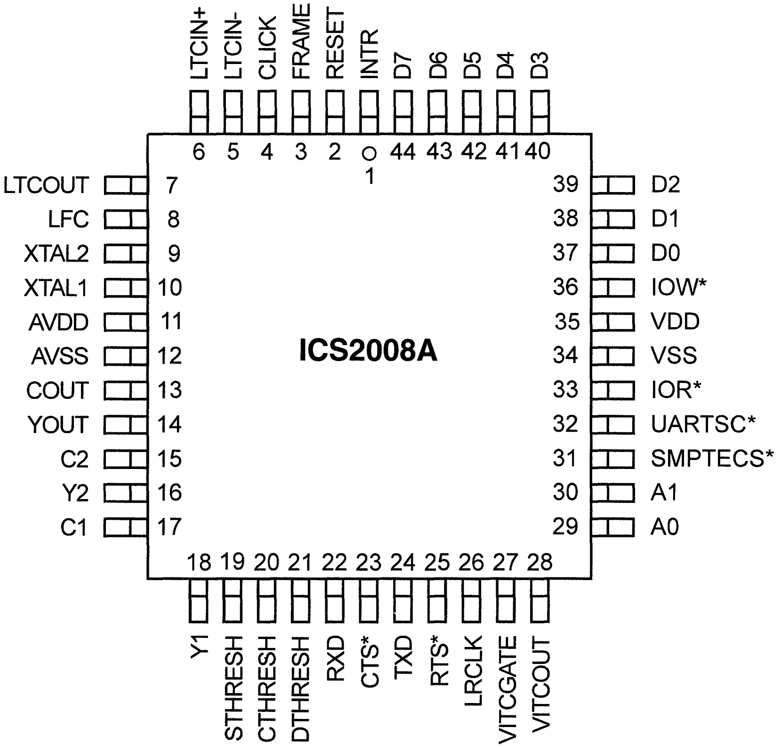
Features

- Internal and external sync sources
  - Genlock to video or house sync inputs
  - Internally generated timing from oscillator input
  - External click input
- LTC and VITC Generators
  - Real Time SMPTE Rates: 30 Hz, 29.97 Hz, 25 Hz, 24 Hz
  - Time Code Modes: Drop Frame and Color Frame
  - VITC can be inserted on two lines from 10-40 (SMPTE specifies lines 10-20)
  - Jam Sync, freewheeling, error bypass/correction, and plus-one-frame capability
- LTC Receiver
  - Meets SMPTE and EBU LTC specifications
  - Synchronize bit rates from 1/30th nominal to 80X nominal playback speed.
- VITC reader
  - Reads code from any or all selected scan lines.
  - Meets SMPTE VITC specifications

New, Improved Features

- Time Code Burn-in Window with programmable position, size and character attributes
- Internal Timer, allows 1/4 Frame MIDI Time Code Messages
- LTC edge rate control, conforms to EBU Tr and Tf specification
- Improved video timing lock during VCR pause and shuttle modes
- VITC search mode, will search through VBI lines until VITC is found
- New UART frequency of 38.4 K baud for tape transport control
- Improved video output performance

Package Pinout



44-Pin PLCC
K-10

Pin Description

PIN	TYPE	DESCRIPTION
Y1, Y2	AI	Video inputs from camera or other source. NOTE: This is also the Y (Luma) input for S-VHS and HI-8 systems.
C1, C	AI	C (Chroma) inputs for S-VHS and HI-8 systems. In NTSC systems, this pin should be tied to its respective Y input.
DTHRESH	AI	Data Threshold bypass input.
STHRESH	AI	SYNC Threshold bypass input.
CTHRESH	AI	Clamp Threshold bypass input.
YOUT	AO	Video output. This is also the Y (Luma) output in S-Video mode.
COUT	AO	C (Chroma) output for S-VHS and HI-8 systems.
FRAME	AI	Color Frame A/B input. This input is self biased. (See Applications section.)
CLICK	AI	LTC SYNC input. This input is self biased. (See Applications section.)
LTCIN+	AI	SMPTE LTC input+. This input is self biased. (See Applications section.)
LTCIN-	AI	SMPTE LTC input-. This input is self biased. (See Applications section.)
LTCOUT	AO	SMPTE LTC output.
LRCLK	O	SMPTE LTC receive clock output.
VITC	O	SMPTE VITC output to video mixer circuit.
VITCGATE	O	VITC gate indicates VITC code is being output for video overlay.
TxD	O	UART Transmit Data.
RxD	I	UART Receive Data.
CTS*	I	Clear to Send.
RTS*	O	Ready to Send.
XTAL1	I	14.318 MHz crystal input. This pin may be driven directly from a TTL 14.318 MHz source.
XTAL2	O	14.318 MHz crystal oscillator output.
LFC	AI	External RC circuit.
A1-A0	I	Address bus
IOR*	I	Read Enable (active low)
IOW*	I	Write Enable (active low)
SMPTEC*	I	SMPTE port chip select (active low)
UARTCS*	I	UART chip select (active low)
RESET	I	Master reset (active high)
D7-D0	I/O	Bi-directional data bus
INTR	O	Interrupt Request (active high)
AVDD	P	Analog V_{DD}
AGND	P	Analog Ground
VDD	P	Digital V_{DD}
GND	P	Digital Ground

A - Analog I - Input
P - Power O - Output

Functional Description

The following is a functional description of the hardware registers in the **ICS2008A** chip. It also describes how those registers can be utilized by the software to facilitate specific application services.

Hardware Environments

The **ICS2008A** operates as a peripheral to a processor such as a PC or a single chip microprocessor. Many of the real time requirements are satisfied by double buffering both incoming and outgoing time codes.

LTC Input

LTCIN is a differential analog input feeding a comparator with hysteresis. It requires capacitive coupling to the LTC source. The output of the comparator goes to the LTC receiver, which is capable of receiving LTC in a forward or backward direction at a rate from 1/30th to 80x nominal frame rates. The incoming LTC data is sampled with a phase-locked clock and loaded into the receive buffer following the receipt of a valid LTC SYNC pattern. When a complete frame has been received, an interrupt is generated.

LTC Output

The LTC output can be analog or digital. When set up as an analog output, it can drive a high impedance load.

The LTC generator outputs a LTC frame at the selected frame rate, such as 24 Hz, 25 Hz, 29.97 Hz or 30 Hz, and starts the frame based on a start time generated by the selected LTC SYNC source.

The output edge rate is programmable for SMPTE code (25µsec) and EBU code (50µsec) rise and fall times.

Video Inputs

There are two sets of video inputs. In a composite NTSC or PAL system, the Y input is the only one used. It is capacitively coupled to the source. In S-Video systems, capacitively couple Y and C to their respective sources. Proper termination of the source should be observed. One of the two video sources is selected by the VIDSEL bit in the SMPTE control registers as the video SYNC source. Internal timers are synchronized with the incoming video to extract timing information used to receive and generate VITC.

The VITC receiver samples the incoming video looking for a valid VITC code on selected scan lines. When a valid code is received it is written to a VITC receive buffer. More than one line can contain VITC code, and the codes can be different. For this reason, VITC codes from selected lines of a frame are written to separate VITC buffers.

Video Output

The video output combines the selected video input with the outputs from the VITC generator and the character generator. It can be a composite or an S-Video output as selected by the SVID bit in the SMPTE control registers.

VITC code is generated from data in the VITC generator buffer and output during the selected line time(s). The CRC and synchronizing bits are automatically generated by the VITC generator, but all of the data fields are sent directly from the buffer with no modification.

A character generator is provided to insert the time code in a burn-in window which overlays the incoming video. The vertical and horizontal position of the burn-in window is programmable.

SMPTE SYNC Sources

A time code generator must have a SYNC input from a stable source in order to position the LTC code properly on a audio track of video tape or film. Three SYNC sources, video, click input, and free running, are available. In the case of a video tape, LTC code must start within plus or minus one line of the beginning of line 5. This requires "Genlocking" to the incoming video. The video timing section locks to the video's horizontal and vertical SYNC signal and generates a SMPTE SYNC. If some external SYNC source is available it can be input on the CLICK input. Otherwise, a free running SMPTE SYNC is generated from the oscillator at the selected frame rate.

Video Timing Generator

The video timing generator is "Genlocked" to the video input's SYNC separator. It extracts NTSC or PAL timing information from the video input and generates line and pixel rate timing for the VITC receiver, VITC generator, LTC generator and character generator. If no video input is present, it generates free running timing.

Overlay Character Generator

It is sometimes desirable to display the time code on a video display along with the picture. A character generator is provided for that purpose. The time code display, or burn-in window, can be positioned anywhere on the screen. It can be displayed in two sizes with white or black characters on a black, white or live video background.

UART

A general purpose UART is provided for MIDI, video transport control, etc. Most serial interface transport controls use 9600 and 38.4K BAUD. The CTS and RTS modem controls are needed in these applications. MIDI ports use 31.25K BAUD, but they do not require modem controls. The receiver includes a four byte FIFO to reduce the real time interrupt servicing requirements. This is particularly important in MIDI applications because of the high data rate and the fact that many MIDI messages are three bytes long. The transmitter is doubled buffered. Interrupts can be generated on both receiver data available and/or transmit buffer empty.

Interrupt Timer

The interrupt timer is a general purpose 10 bit timer with three clock sources (100 kHz, the LTC receive clock and the LTC transmit clock). Although the timer is general purpose in nature, its main purpose is to facilitate the timed generation of MIDI time code messages.

Processor Interface

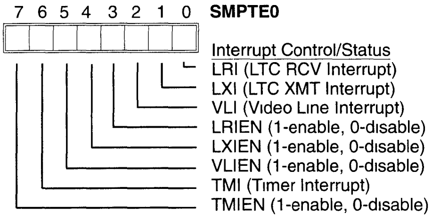
The **ICS2008A** supports standard microprocessor interfaces and busses, such as the PC bus, to allow access to six control/status and data registers. These six registers are organized into two groups, one set of four for SMPTE control and the other set of two for direct UART port control. Each set of registers is selected with its own chip select, SMPTECS* and UARTCS*.

SMPTE Registers

The SMPTE register set allows access to four direct and 64 indirect registers. The first two direct access registers addressed at locations 0 and 1 are for status and interrupt control. The 64 indirect registers are accessed by writing an indirect address into SMPTE2 and reading from or writing to SMPTE3. If the AUTOINC bit in SMPTE2 is set to 1, the indirect register address is automatically incremented after an access to SMPTE3. This eases the task of reading or writing sequential indirect locations.

SMPTECS*	A1	A0	REGISTER
0	0	0	SMPTE0 Interrupt Control/Status
0	0	1	SMPTE1 SMPTE Status
0	1	0	SMPTE2 Indirect Register Address
0	1	1	SMPTE3 Indirect Register Data

The SMPTE0 Register contains the SMPTE interrupt controls and status and the VITC read status. The four interrupt bits, LRI, LXI, VLI and TMI reflect the status of the potential interrupt sources to the processor. When a bit is set to one and the corresponding enable bit, LRIEN, LXIEN or VLIEN, is also set, the INTR output will be activated. Interrupts are cleared by reading SMPTE0.



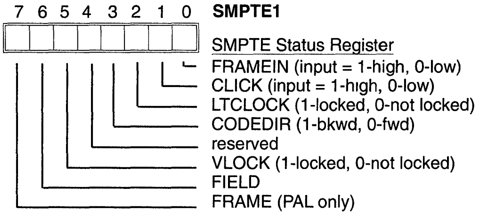
LRI - This bit indicates that a LTC receive interrupt has occurred. In order for an actual processor interrupt to occur, the LRIEN bit must also be set. An LRI interrupt occurs upon reception of the last byte of LTC receive data which was preceded by a valid LTC SYNC pattern. That is after the 64th LTC receive bit time in the forward direction. At normal frame rates, if the LTC transmitter is synchronized with the LTC receiver, there is about 3 milliseconds after this interrupt before the LTC transmit data for the next output frame is transferred to the output buffer.

LXI - This bit indicates that a LTC transmit interrupt has occurred. When this bit is set, and the corresponding LXIEN bit has been set, the INTR output will be activated. The LTC transmit interrupt is activated after the transfer of LTC transmit data to the output buffer. This occurs after LTXEN is set to one and after the 72nd LTC transmits bit time of the current frame, "N." Data loaded after this interrupt will appear in output frame "N+2" since the transmitter is double buffered.

VLI - This is a status bit that indicates that the video line selected via the Video Interrupt Line Register, VR9, has passed. When the VLIEN bit is also set, the processor will be interrupted. This interrupt can be used by the processor to determine when to sample the VITC time code when time locked to a video source. It will also be used to facilitate detection of LTC time code dropout and off speed LTC code, e.g. shuttling operations.

TMI - This bit indicates that a timer interrupt has occurred. When the TMIEN bit is also set to a one, the INTR output will be activated. This interrupt is intended to facilitate timing MIDI clocks and MIDI Quarter Frame messages.

The SMPTE Status Register is a read only register which contains video and LTC status.



FRAMEIN - This bit indicates the state of the FRAME input pin. It is used as an alternate source for B/A frame status. This is useful when the quality of the video signal is not good enough to extract the B/A frame status.

CLICK - This bit indicates the state of the CLICK input pin. It can be used as a synchronization source for the LTC transmitter.

LTCLOCK - When a valid forward or backward LTC sync pattern is detected, this bit is set to one. It is reset to zero when an expected LTC sync pattern is missed or an invalid LTC bit is detected.

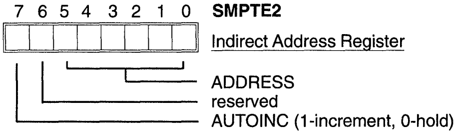
CODEDIR - The code direction bit works in conjunction with the LTCLOCK bit. When the LTCLOCK bit is set to one, the CODEDIR bit is valid. Otherwise, it is not. See the table below.

LTCLOCK	CODEDIR	LTC RECEIVER STATUS
0	X	Looking for SYNC pattern
1	0	receiving LTC (FORWARD)
1	1	receiving LTC (BACKWARD)

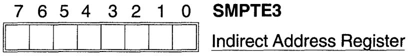
VLOCK - This is a hardware driven bit which indicates that genlock has been achieved with the selected video SYNC source.

FRAME & FIELD - The hardware SYNC separator detects the field and frame from the selected video input. The even/odd fields are identified by a 1/0 in bit 6. Bit 7, FRAME, is valid for PAL video after line 6. Bit 6, FIELD, is valid after line 5 in NTSC mode or line 2 in PAL mode.

The SMPTE2 register is the register which points to the 57 indirect registers. When reading or writing an indirect register, the value in the ADDRESS pointer, SMPTE2 bits 5 to 0, is the address of the register accessed through SMPTE3. If the AUTOINC bit is set to one, at the end of an access cycle to SMPTE3, ADDRESS will automatically increment. Otherwise, ADDRESS holds its value.



SMPTE3 is the data register through which all of the indirect registers are accessed. The address for a given register must first be set in SMPTE2 before accessing that register.



Indirect Registers

The following describes the functions controlled by the indirect registers. A map of the indirect registers follows this section.

LTC Read Registers **IR0-IR7** (read-only)
These read only registers contain the LTC data as received. Both forward and backward frames are stored with LTC bit 0 in the LSB of IR0 and LTC bit 63 in the MSB of IR7.

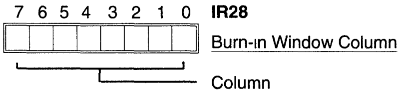
LTC Write Registers **IR8-IRF**
These registers contain the data to be sent by the LTC transmitter. The LSB of IR8 is sent as LTC bit 0, and the MSB of IRF is sent as LTC bit 63. The data is transmitted as it is stored in IR8-IRF.

VITC Read 1 Registers **IR10-IR17** (read-only)
These read only registers contain the VITC data as received from the video line selected in IR30. The frame is stored with VITC bit 2 in the LSB of IR10 and VITC bit 80 in the MSB of IR17. Note that a binary 10 sync pattern precedes every eight data bits of the VITC frame. The 10 sync pattern is not stored. The CRC is checked by the VITC receiver, and the result is reported in IR30.

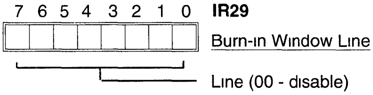
VITC Read 2 Registers **IR18-IR1F** (read-only)
As with the VITC Read 1 registers, these read only registers contain the VITC data as received from the video line selected in IR31. The frame is stored with VITC bit 2 in the LSB of IR18 and VITC bit 80 in the MSB of IR1F. The result of the CRC check is reported in IR31.

VITC Write Registers **IR20-IR27**
These registers contain the data to be output by the VITC generator. The VITC frame is output with the LSB of IR20 in VITC bit 2 and the MSB of IR27 in VITC bit 80. Note that the binary 10 sync pattern which precedes every eight data bits of the VITC frame is automatically generated by the VITC generator. The CRC is also automatically generated by the VITC generator.

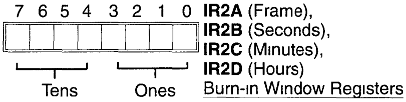
BI Window Registers **IR28 & 29**
The next two registers control the position of the SMPTE video display, burn-in, window within the video raster. IR28 selects the video column (horizontal position) in which the burn-in window starts.



IR29 selects the video line which starts the SMPTE video display window in the video output. When this register is set to zero, there will be no Burn-In Window displayed in the video output.

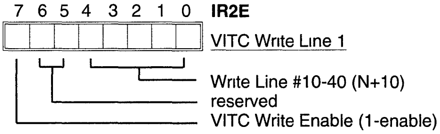


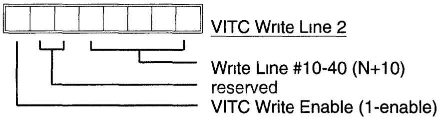
BI Character Registers **IR2A-IR2D**
These registers contain the character codes used for the SMPTE time code in the burn-in window which overlays the source in the video output. An internal character generator converts the BCD nibbles to display characters.



CODE	CHARACTER	CODE	CHARACTER
0	0	8	8
1	1	9	9
2	2	A	Do Not Use
3	3	B	?
4	4	C	_
5	5	D	□
6	6	E	■

VITC Write Line Select Registers **IR2E & IR2F**
VITC code is normally output on two separate video lines in each field for redundancy. These two registers allow the individual line selection and output enables for the two VITC lines.

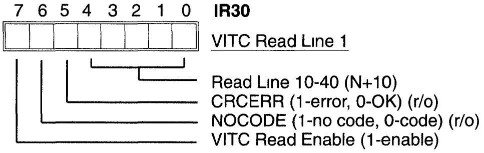


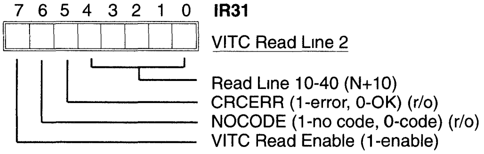


Write Line - Selects the video line on which the VITC code will be output. The video line on which the code is output will be the number in this register plus 10; e.g. writing a one to this register will cause the code to be output on line 11.

VITC Write Enable - Enables the output of VITC code on the specified line.

VITC Read Line Select Registers **IR30 & IR31**





As with the VITC Write Line Register, these registers allow control of the individual redundant VITC read lines. The processor can also reprogram these dynamically to allow for scanning of VITC code when the source lines are unknown.

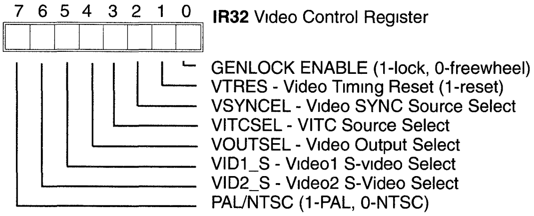
Read Line - Selects the line from which VITC code is to be read within each field. It works identically to the Write Line in that the video line selected is the number in this register plus 10.

Auto line scanning is enabled by writing a 1Fh to the Read Line field. This causes the VITC reader to search for time code. If VITC Read Line 1 is set to search, it starts with line 10 and quits when it finds a valid time code or when it reaches line 41. Searching with VITC Read Line 2 starts after VITC Read Line 1. In the case of searching for both VITC Read Lines 1 and 2, VITC Read Line 2 starts searching after the first valid time code has been found. However, if VITC Read Line 1 is set to a specific line, VITC Read Line 2 starts after that specified line regardless of whether valid time code was received. In any case, the search terminates after line 41.

CRCERR - This bit is reset to zero when a valid VITC code has been received. It is valid from the end of the selected video line until the end of the selected line in the next field.

NOCODE - This bit is set when a framing error occurs in the VITC code, i.e. not all the bits of the code were received by the time the end of the video line occurred. Both CRCERR and NOCODE must be zero to qualify a VITC code.

Video Control Register **IR32**



GENLOCK ENABLE - When set to one, this bit enables the genlock circuits to sync to the selected video input signal. When reset to 0, the video sync will "freewheel," generating video timing from the internal oscillator. The freewheel mode would be selected when striping LTC to allow synchronization with a MIDI sequencer or other strictly timed audio source.

VTRES - When set to one, this bit clears the video timing counters to dot zero of line 1 of field 1. This is useful when the video is free running, not genlocked and LTC sync needs to be synchronized to an event such as the CLICK input.

VSYNCSEL - When set to one, this bit selects the video input source from Video2 (Y2) to be the SYNC source for the internal video timing. Otherwise, when reset to zero, Video1 (Y1) is selected.

VITCSEL - When set to one, this bit selects the video input source from Video2 (Y2) to be the VITC time code source for the VITC receiver. Otherwise, when reset to zero, Video1 (Y1) is selected.

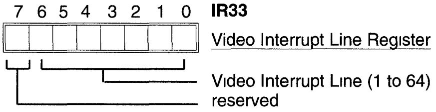
VOUTSEL - When set to one, this bit selects the video input source from Video2 (Y2, C2) to be output on the video outputs (YOUT, COUT). When reset to zero, Video1 (Y1, C1) are selected.

VID1_S - When set to one, this bit causes the Video1 source to be treated as S-Video. Otherwise, when cleared to zero, the Video1 source is treated as composite video.

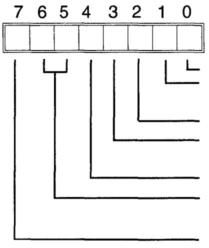
VID2_S - When set to one, this bit causes the Video2 source to be treated as S-Video. Otherwise, when cleared to zero, the Video2 source is treated as composite video.

PAL/NTSC - When set to one, this bit causes the video to be synchronized with PAL timing. Otherwise, when cleared to zero, video is synchronized with NTSC timing.

Video Interrupt Line Register **IR33**
This register selects the video line after which the Video Line Interrupt will occur. The actual video line number is the number in the register plus one.



LTC Control Registers **IR34-IR37**



IR34

LTC Control Register 1

EDGERATE -(0-25usec., 1-50usec.)
LXTFREE - (0-LTCYNC start)
(1-free start)
reserved (set to zero)
LXCLKSEL - (0-internal clock)
(1-LTC receive clock)
LTXEN - LTC Transmit Enable
LTC SYNC - (00-video, 01-CLICK)
(10-LTC RCV, 11-Software)
LTCOUTSEL -(1-digital, 0-analog)

EDGERATE - This bit selects the LTC output edge rate. SMPTE specifies 25 µsec rise and fall times while EBU specifies 50 µsec.

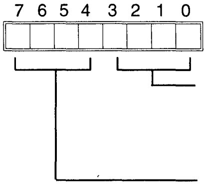
LTXFREE - This bit controls the LTC frame start of the LTC transmitter. When reset to zero, the start of a LTC output frame is triggered by the selected LTC SYNC source. Otherwise, when set to one, the end of a LTC frame will trigger the start of the next. The first LTC transmit frame must be triggered by one of the SYNC sources.

LXCLKSEL - This bit controls the source for the LTC transmit clock divider input. A 0 selects the internal 14.318 MHz clock and a 1 selects the LTC receive clock. When the LTC receive clock is selected as the source to the LTC transmit clock divider, the clock rate is first doubled before being input to the divider so that loading a divider value of 001 will result in the LTC transmit clock running at the exact same rate as the LTC receive clock.

LTXEN - This bit, when set to 1, enables output of LTC code on the LTCOUT output pin. LTXEN is synchronized with the selected LTC SYNC source to ensure that only complete LTC frames are transmitted. The data to be sent by the LTC transmitter should be loaded into the associated RAM buffer before the LTCEN bit is set.

LTC SYNC - These bits select the LTC transmit sync source. Values 00, 01, 10 and 11 select start of video line 5, rising edge of CLICK, LTC receive sync pattern detect and write to IR3F respectively as the sync event. Care should be taken to disable LTXEN before changing the LTC SYNC select. Otherwise, an erroneous sync may be generated.

LTCOUTSEL - This bit, when set to 1, causes the LTCOUT pin to be a digital output. When cleared to 0, the LTCOUT pin is an analog output with gain control.



IR35

LTC Control Register 2

LTCGAIN - LTC Output Gain

0· off	4. -24dB	8. -12dB	C· 0dB
1	5 -21dB	9· -9dB	D. 3dB
2:	6 -18dB	A -6dB	E: 6dB
3	7. -15dB	B -3dB	F: 9dB

reserved

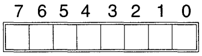
LTCGAIN - This bit sets the signal gain on the LTC audio output. The output gain is selectable in 3dB increments from -24dB to +9dB referenced to 0VU = -10dbV. When this register is set to zero, there is no LTC audio output.

These next two write only registers, IR36 and IR37, control the LTC transmit bit rate. The transmit clock generator is a 12-bit divider. The upper four bits of IR37 are not used. Each bit requires two clocks. Therefore, the LTC transmit bit rate is the input clock divided by the divider value + 1, then divided by two. Since there are 80 bit times for each LTC frame, the LTC frame rate is the bit rate divided by 80.

LTC Tx Clock = 14.318 MHz/(Divider Value + 1)
LTC Bit Rate = LTC Tx Clock/2
LTC Frame Rate = LTC Bit Rate/80

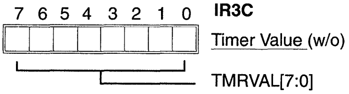
The table below shows the divider values for some of the most commonly used LTC frame rates.

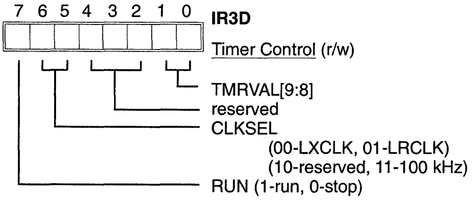
LTC FRAME RATE	DIVIDER VALUE
30 Hz	BA6h
29.97 Hz	BA9h
25 Hz	DFBh
24 Hz	E90h



IR36 [low byte]
IR37 [high byte]
LTC Bit Time (write only)

Timer Control Registers **IR3C & IR3D**
These two registers control the interrupt timer. It should be noted that IR3C is a write only register, while IR3D is a read/write register.



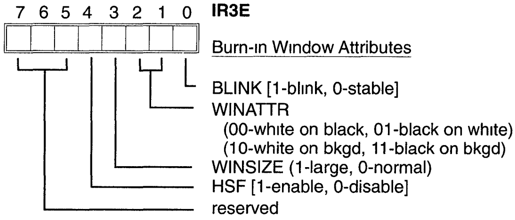


TMRVAL - These ten bits set the divder value for the interrupt timer. The interrupt rate is the input clock rate divided by the value plus one.

Interrupt Rate = CLOCK/(TMRVAL+1)

CLKSEL - This 2 bit field selects the clock source for the interrupt timer. The 100 kHz input is actually 100.126 kHz. It is the crystal frequency divided by 143.

RUN - This bit starts and stops the timer. When set to one, the timer is running. When set to zero, the timer is stopped.



BLINK - This bit controls the upper dot of the right-most colon in the burn-in-window. When set to zero, the upper dot is on. When set to one, it is off. This feature can be used to indicate odd and even fields in the time code display window.

WINATTR - These two bits control the color of the characters and the background in the burn-in window. When the most significant bit of this field is a one, the background is the incoming video.

WINSIZ - This bit controls the size of the burn-in window. The difference in size between a large and a normal-sized window is 32 scan lines high, while a large window is 64 scan lines high.

HSF (Head Switch Filter) - When set to one, this bit causes the clamp circuit to ignore head switch transients and horizontal sync during the last six to seven lines before the vertical front porch. Otherwise, the clamp circuit responds always.

LTC Soft Sync **IR3F**
IR3f is not a register at all. It is simply an address which, when written and the LTC SYNC select is set for Soft SYNC, generates LTC SYNC for the LTC transmitter.

Indirect Register Map

		7	6	5	4	3	2	1	0
LTC	00	BINARY GROUP 1				FRAME UNITS			
Read	01	BINARY GROUP 2				COLR FRAME	DROP FRAME	FRAMES TENS	
	02	BINARY GROUP 3				SECONDS UNITS			
	03	BINARY GROUP 4				PHASE CORR	SECONDS TENS		
	04	BINARY GROUP 5				MINUTES UNITS			
	05	BINARY GROUP 6				BG FLAG 55	MINUTES TENS		
	06	BINARY GROUP 7				HOURS UNITS			
	07	BINARY GROUP 8				BG FLAG 75	UNASSIGNED	HOURS TENS	
LTC	08	SAME BIT DEFINITION AS LTC READ BUFFER							
Write	...								
	OF								
VITC	10	BINARY GROUP 1				FRAME UNITS			
READ1	11	BINARY GROUP 2				COLR FRAME	DROP FRAME	FRAMES TENS	
	12	BINARY GROUP 3				SECONDS UNITS			
	13	BINARY GROUP 4				FIELD MARK	SECONDS TENS		
	14	BINARY GROUP 5				MINUTES UNITS			
	15	BINARY GROUP 6				BG FLAG 55	MINUTES TENS		
	16	BINARY GROUP 7				HOURS UNITS			
	17	BINARY GROUP 8				BG FLAG 75	UNASSIGNED	HOURS TENS	
VITC	18	SAME BIT DEFINITION AS VITC READ1 BUFFER							
Read2	...								
	1F								
VITC	20	SAME BIT DEFINITION AS VITC READ1 BUFFER							
Write	...								
	27								
Regs	28	BURN-IN WINDOW COLUMN							
	29	BURN-IN WINDOW LINE							
	2A	FRAMES							
	2B	SECONDS							
	2C	MINUTES							
	2D	HOURS							
	2E	VITC1WE	0	0	VITC WRITE LINE 1				
	2F	VITC2WE	0	0	VITC WRITE LINE 2				
	30	VITC1RE	NOCODE1	CRCERR1	VITC WRITE LINE 1				
	31	VITC2RE	NOCODE2	CRCERR2	VITC READ LINE 2				
	32	PAL	VID2_S	VID1_S	VOUTSEL	VITCSEL	VSYNCSEL	VTRES	GEN_EN
	33	0	0	VIDEO LINE INTERRUPT (LINE#)					
	34	LTCOUTSEL	LTCSYNCSEL		LTXEN	LXCLKSEL	0	LTXFREE	EDGE RATE
	35	0	0	0		LTC GAIN			
	36	FRAME RATE (low byte, write only)							
	37	0	0	0	0	FRAME RATE (high byte, write only)			
	38	reserved							
	39	reserved							
	3A	reserved							
	3B	reserved							
	3C	TIMER VALUE (low byte, write only)							
	3D	RUN	CLKSEL		0	0	0	TIMER VALUE (high)	
	3E	0	0	0	HSF	WIN_SIZE	WINDOW ATTRIBUTE		BLINK
	3F	SOFT LTC SYNC (write only, no data)							

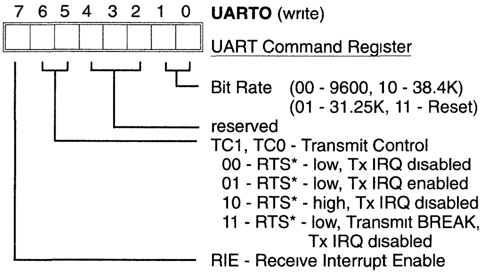
UART Registers

The UART emulates a 6850. Since the UART is tailored to MIDI applications, some of the generic 6850 functions have been omitted. The registers described below reflect that.

The two UART registers, Command/Status and Data, are accessible to the processor as shown in the following map.

UARTCS*	A1	A0	REGISTER
0	X	0	UART Command/Status Register
0	X	1	UART Data Register

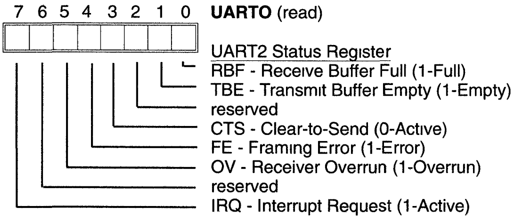
UART Command/Status Register



Bit Rate - This field selects the bit rate for data transmit and receive. After a master reset, its value is 11. One of the three bit rates must be selected in order to start the UART's operation. Writing a 11 will reset the UART.

TC1,TC0 - Bits 6 and 5, Transmit Control, provide control for transmit interrupt (when TBE is true), RTS control, and transmit BREAK level.

RIE - Bit 7, Receive interrupt enable, when set to one, enables the UART to interrupt the processor when the receive buffer is full or a receive overrun has occurred.



RBF - Bit 0, Receive Buffer Full, is set to 1 when read data is available in the UART data register. It is cleared to 0 when the UART data register is read.

TBE - Bit 1, Transmit Buffer Empty, is cleared to 0 when data is written to the UART data register. It is set to 1 when the UART transfers that data to its output shift register.

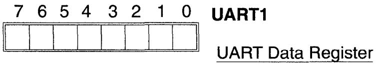
CTS - Bit 3, Clear-to-Send, is an active low status bit indicating the state of the CTS* input pin. A 0 in this bit position indicates that the modem or receiving device is ready to receive characters. A 1 indicates not ready. When CTS is inactive, 1, TBE is held at 0, the not-empty state.

FE - Bit 4, Framing Error, when set to 1, indicates that the receive character was improperly framed by the start and stop bits. It is detected by the absence of the first stop bit. This indicator is valid as long as the character data is valid.

OV - Bit 5, Receiver Overrun, is an error flag indicating that one or more characters in the data stream has been lost. It is set to 1 when a new character overwrites an old character which has not been read. The overrun error is cleared to 0 when a character is read from the UART data register.

IRQ - Bit 7, Interrupt Request, is a status bit which reflects the state of the interrupt request from the UART to the processor. When IRQ is 1, an interrupt is pending. Otherwise, no interrupt is pending.

The UART data register is actually two registers, a transmit buffer and a receive buffer. Writing to the data register causes the transmit buffer to be written. Reading from the data register causes the receive buffer to be read.



Absolute Maximum Ratings

Operating Temperature	0 °C to +70 °C
Storage Temperature	-65 °C to +150 °C
Voltage on any pin to GND	-0.5V to V_{DD} + 0.5V
Voltage on V_{DD} to GND	-0.5V to +7.0V
Power Dissipation	1.0 watt

Note: Stress above that listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Operating the device at these levels is not recommended, and specifications are not implied.

DC Characteristics T_A=0 °C to +70 °C; V_{DD} = 5V±10%; GND = 0V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Digital Inputs					
Input Low Voltage	V_{IL}	-0.5		0.8	V
Input High Voltage	V_{IH}	2.0		V_{DD}+0.5	V
Input Leakage Current	I_{LI}			10	uA
Input Capacitance	C_{IN}			7	pF
Digital Outputs					
Output Low Voltage (I_{OL} = 4.0mA)	V_{OL}			0.4	V
Output High Voltage (I_{OH} = 0.4mA)	V_{OH}	2.4			V
Tri-State Current	I_{OZ}			10	uA
Output Capacitance				10	pF
Bi-Directional Capacitance				10	pF
Analog Inputs					
Video Input Voltage (Y1, Y2, C1, C2)			1.0		V_{p-p}
LTC Differential Input Voltage		0.1			V_{p-p}
LTCIN+, LTCIN-, CLICK, FRAME input voltage		-0.3		V_{DD}+0.3	V
CLICK and FRAME bias voltage			V_{DD}/3		V
Analog Outputs					
Video output Voltage (YOUT, COUT)			1.0		V_{p-p}
LTC Output Voltage (Volume set at max.; I_{out} = 35mA)			2.0		V_{p-p}
LTC Output Voltage Amplitude Control Step			3		dB
LTC Output Voltage Amplitude Range			33		dB
Analog V_{DD} Supply Current	I_{DD1}			50	mA
Digital V_{DD} Supply Current	I_{DD2}			5	mA

AC Characteristics T_A=0 °C to +70 °C; V_{DD} = 5V±10%; GND = 0V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Address setup to IOR* or IOW* command	t_{ACS}	20			ns
Address hold from IOR* or IOW* command	t_{AH}	10			ns
Read pulse width	t_{RD}	150			ns
Access time	t_{ACC}			150	ns
Output enable access time	t_{OE}			50	ns
Data hold from IOR* high	t_{RDH}	10			ns
Read command inactive time	t_{RHRL}	70			ns
Write pulse width	t_{WR}	150			ns
Write data setup to IOW* high	t_{WDS}	20			ns
Write data hold from IOW* high	t_{WDH}	10			ns
Write command inactive time	t_{WHWL}	70			ns
CS* inactive time (Note 1)	t_{CHCL}	20			ns
UART Port Bit Rate (Command Register [1:0]=00)			9.6		kHz
(Command Register [1:0]=01)			31.25		kHz
(Command Register [1:0]=10)			38.4		kHz

Note 1: This timing parameter must be met for proper operation of indirect register access using auto-increment.

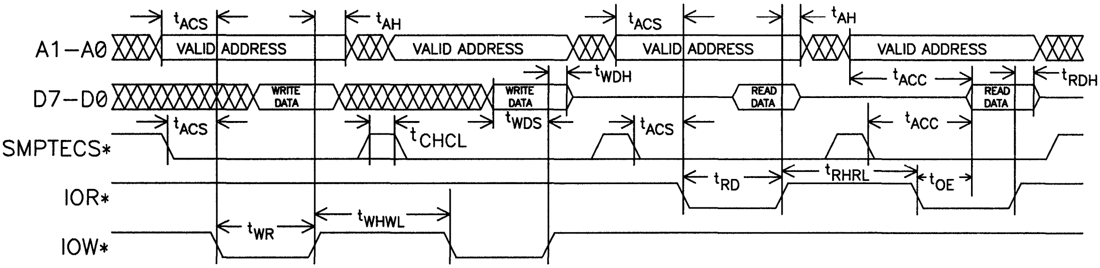


Figure 3 - Host Processor Bus Timing

Applications

Crystal Oscillator

This oscillator will operate properly with either a serial or parallel resonant crystal. If frequency accuracy is critical, a parallel resonant crystal is recommended.

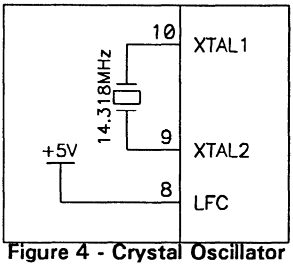


Figure 4 - Crystal Oscillator

Threshold Bypass Pins

These pins provide access to the internal references for clamp level (CTHRESH), SYNC slicer (STHRESH), and data slicer (DTHRESH). In general, these pins are left open, and the levels are output. However, should the user want to set other levels, these pins can be over-driven with the desired threshold level(s).

CTHRESH is the threshold to which the input video sync tips are clamped. The CTHRESH level is nominally 1.3V. With the incoming video riding on this 1.3V DC level, the internal SYNC separator sizes the video at 20 IRE up from the SYNC tips. This level, STHRESH, is nominally 0.14V above CTHRESH. The SYNC separator ignores short pulses which fall below the STHRESH level such as these that come from the chroma component of the video. DTHRESH is the data slicer reference. It is nominally 0.57V above CTHRESH.

Video Inputs

Y1, Y2, C1 and C2 pins must be capacitively coupled to the terminated video source(s). These inputs are clamped to the CTHRESH level. A typical coupling capacitance is .1uF.

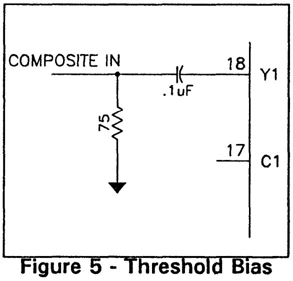


Figure 5 - Threshold Bias

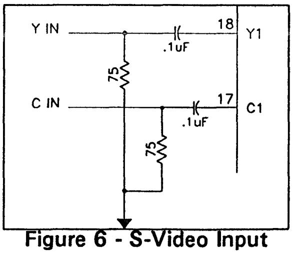


Figure 6 - S-Video Input

Video Outputs

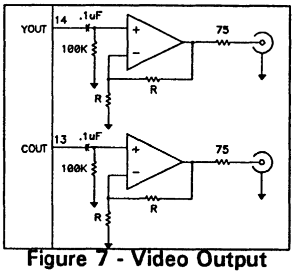


Figure 7 - Video Output

YOUT and COUT are outputs of analog multiplexers which select the video source from Y1, C1 or Y2, C2. These outputs are not buffered. This minimizes signal distortion. It is, therefore, important to keep the capacitive and resistive load on the YOUT and COUT pins to a minimum. A video output buffer is shown in Figure 7. If DC coupling is desired, the plus input of the opamp should be high impedance with a low bias current, and its output should be able to drive a 75 ohm load with an appropriate video bandwidth. In general, composite NTSC and S-video signals have a bandwidth of 4.2 MHz. A minimum output buffer bandwidth of 10 MHz is recommended.Care should be taken in board layout to minimize stray capacitance on the YOUT and COUT pins. Otherwise, there could be high frequency roll-off which could result in a loss of chrominance amplitude.

Self Biased Inputs

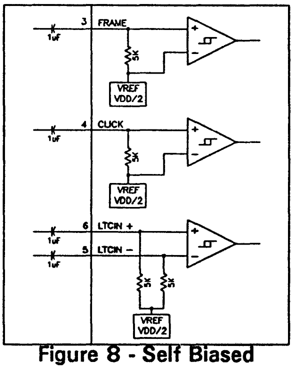


Figure 8 - Self Biased Inputs

The CLICK and FRAME inputs are biased to 1/2 VDD and connected to plus inputs of two comparators. The minus inputs are internally biased to 1/2 VDD. When CLICK or FRAME sources are analog, they should be capacitively coupled to the input pin. However, if the sources are digital, they may be tied to the pins directly. It is important to make sure that the digital levels into these pins swing above and below the 1/2 VDD threshold of the comparators. This is not a problem with digital CMOS sources, but it could be with TTL sources.

LTCIN+ and LTCIN- are comparator inputs for the LTC input. This differential input is provided to maximize noise immunity. If the LTC source is single ended, the LTCIN- should be capacitively coupled to the ground reference of that source. If the LTC source is digital, set the LTCIN- to the desired threshold, and connect the digital source to LTCIN+.

Programming

The **ICS2008A** is a SMPTE time code input/output device with a UART which can be used as a MIDI UART or transport control UART. All of the time critical functions to read and generate time code are performed by the chip's hardware, but all of the intelligence for processing time codes and generating the time code values are performed via an external processor. This makes the **ICS2008A** flexible enough for a broad range of applications without making the processing requirements on the host system too great.

Indirect Register Access

Indirect registers are accessed via the SMPTE2 (address) and SMPTE3 (data) registers. To read an indirect register, the program must first write its address to SMPTE2. Then the data is read from SMPTE3. Writing to an indirect register is similar. First, the address is written to SMPTE2. Then the data is written to SMPTE3.

In order to minimize the number of accesses required to read or write a block of registers, an auto-increment function is provided. If the MSB of SMPTE2 is written to a one with the address, the address is incremented after each read or write access to SMPTE3. For example, if one wants to read the LTC Read registers, IR0 to IR7, SMPTE2 is written to a 80h. Then read SMPTE3 eight times. The first byte read is from IR0 followed by IR1, etc.

Interrupt Processing

Interrupts can be generated from five sources, LTC receiver, LTC generator, video line count, timer and UART. The interrupt status of the first four interrupts, LRI, LXI, VLI and TMI are in the SMPTE0 register. After this register is read, all four interrupts are cleared. It is, therefore, necessary to save the state of the interrupt status and process all active interrupts.

The UART interrupt status is in the UART0 register. The receive interrupt is cleared by reading the receive data register, UART1. The transmit interrupt is cleared by writing data to the transmit data register, UART1.

Reading LTC

When LTC data is received, it is placed into a temporary buffer and transferred into the LTC read register (IR0 to IR7) when the last bit of LTC data has been received. It should be noted that the data is transferred before the SYNC pattern has been received. Once the data is in the LTC receive buffer, the LRI bit is set to one in the SMPTE0 register. If the LRIEN bit (SMPTE0) is set to a one, an interrupt will be generated. The interrupt is cleared when the SMPTE0 register is read. The data in the LTC receive buffer remains valid until the next LTC frame has been completely received.

LTC input data is available in the LTC Read registers after the last LTC data bit has been received. It is not necessary to wait for the LTC SYNC pattern to be complete. When LTC read data is available the LRI bit in SMPTE0 is set to one. If LRIEN is also set to one, an interrupt is generated. LRI and the interrupt are cleared by reading SMPTE0. Data will remain valid until the last LTC data bit of the next frame has been received.

The SMPTE1 register contains two status bits which indicate whether LTC data is being received and if so which direction. LTCLOCK is set to one when the LTC receiver has received a valid LTC SYNC pattern and data is still coming in. CODEDIR indicates the direction of the LTC SYNC pattern. This is useful to tell whether a tape with LTC is shuttling forwards or backwards.

Generating LTC

The LTC generator transfers data from the LTC Write registers (IR8 to IRF) to the output buffer when the LTC generator is enabled; LTCEN is set to one. Data transfers for subsequent LTC frames occur eight bit times before the end of the LTC frame being output. Remember that a LTC frame ends with a 16 bit SYNC pattern. The LXI interrupt bit in SMPTE0 is set to one when LTC Write register data is transferred to the output buffer.

A typical program for generating LTC output would first setup the LTC control registers and the LTC bit time registers. Then time code data would be written to the LTC Write register. Once this setup is done the LTC output would be enabled by setting LTCEN to a one. LTC output starts when a LTC SYNC is received. The LTC SYNC source is selected as part of the setup. While the LTC generator is waiting for SYNC, the data in the LTC Write register is transferred to the output buffer. When the transfer is complete the LXI status but is set to a one. The data for the next LTC output frame can then be loaded. The LXI status bit will be set to a one after the data transfer at the end of the first LTC output frame. At this point the LTC Write register is ready to receive data for a third LTC output frame.

Reading VITC

To read VITC code one must first setup IR30 thru IR33. The VITC Read Line registers, IR30 and IR31, select the video line from which VITC code is to be read. The MSB is the enable for VITC reading. The Read Line field, bits 4 to 0, should be programmed with the desired line number minus ten. So, if line 15 is desired, a 5 should be programmed in the Read Line field. If the read line field is set to 1Fh, this puts the VITC receiver into a scan mode. In scan mode, the VITC receiver looks for a valid time code starting at line 10 for VITC1 or VITC Read Line 1 for VITC2. The scan terminates when a valid time code is received or the line count reads line 41.

IR32 selects the source and type of video. The GENLOCK ENABLE bit must be set to a one, and the VTRES bit must be set to a zero. The Video Interrupt Line register, IR33 should be set to a line after all VITC read and write lines. This allows all of the VITC receive and generate operations to be complete before processing VITC.

The VLOCK bit in the SMPTE1 register indicates whether the **ICS2008A** is genlocked to the selected video source. Without the VLOCK status set to one, no VITC read will occur.

When VLOCK is set to one and the control registers are properly initialized, VITC data are received a byte at a time from the video signal and written to the VITC Read registers. At the end of the VITC data frame the CRC byte is checked, and the result reported in bit 5 of IR30 and IR31. In addition to the CRC check, if a full VITC data frame is not received, the NOCODE bit, bit 6, is set to a one.

Generating VITC

Like reading VITC, IR2E, IR2F, IR32 and IR33 must be setup in order to generate VITC. The VITC Write Line registers, IR2E and IR2F, select the video line to which VITC code is to be written. The MSB is the enable for VITC generation. The Write Line field, bits 4 to 0, should be programmed with the desired line number minus ten. So, if line 12 is desired, a 2 should be programmed in the Write Line field. IR32 selects the source and type of video. The GENLOCK ENABLE bit must be set to a one, and the VTRES bit must be set to a zero. The Video Interrupt Line register, IR33 should be set to a line after all VITC read and write lines. This allows all of the VITC receive and generate operations to be complete before processing VITC.

With the VITC generator setup properly, when the selected video line starts, the VITC data in the VITC Write buffer, IR20 to IR27, is output. The video line interrupt, VLI in SMPTE0, is provided to allow ample processing time for VITC generation.

Burn-in Window

The burn-in window can be placed anywhere on the video display. The position of the upper left corner of the window is selected by the values written in IR28 and IR29. IR28 controls the horizontal position. Values from 00h to 71h put the corner in the first half of a video line (starting from the falling edge of HSYNC). Values from 80h to F1h put the corner in the second half of a video line. Any other values will not display the window. Care should be taken not to choose values which put the window in any part of the blanking area. IR29 controls the vertical position. The value written here is the video line number divided by 2.

IR3E controls the burn-in window character attributes. It controls the size, normal and large, and the color of the characters and background.

IR2A to IR2D, are the registers which control the characters displayed in the burn-in window.

UART

The UART is accessed via two directly addressable registers, the command/status register and the data register. On reset, the UART is not operational. The command register must be initialized before the UART will function.

Band rates are controlled in UART0 bits 1 and 0. 31.25 kHz supports MIDI communications. 9600 Hz and 38.4 kHz support most serial VTR transport controls.

The UART has a four deep FIFO for its receive buffer. This allows for relaxed interrupt latency requirements. In the case of MIDI bit rates, the receiver will not overflow even if the interrupt response delay is 1msec.

The UART's transmitter has a buffer in front of the output shift register so that a byte can be loaded and waiting for the output shifter to be empty.

Ordering Information

ICS2008AV

Example:

ICS XXXX M

Package Type
V=PLCC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS,AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS2101

Digitally Controlled Audio Mixer

Description

The **ICS2101** is a CMOS digitally controlled multi-channel line-level stereo audio mixer for use in multimedia applications. High performance attenuators provide precision gain control in -0.5dB increments. The ten input channels may be used as mono inputs, pairs of stereo inputs, or any combination of mono and stereo inputs appropriate for the application. Stereo balance and mono panning functions are fully supported. The **ICS2101** is compatible with the ISA industry standard bus.

Features

- Five stereo input pairs
- One stereo output pair
- Precision gain control in -0.5dB steps
- Separate attenuation and balance control for each input pair
- Mono input mode with panning capability
- Master attenuation and balance control for output
- Low noise, low distortion
- ISA compatible
- 28-pin DIP or SOIC package

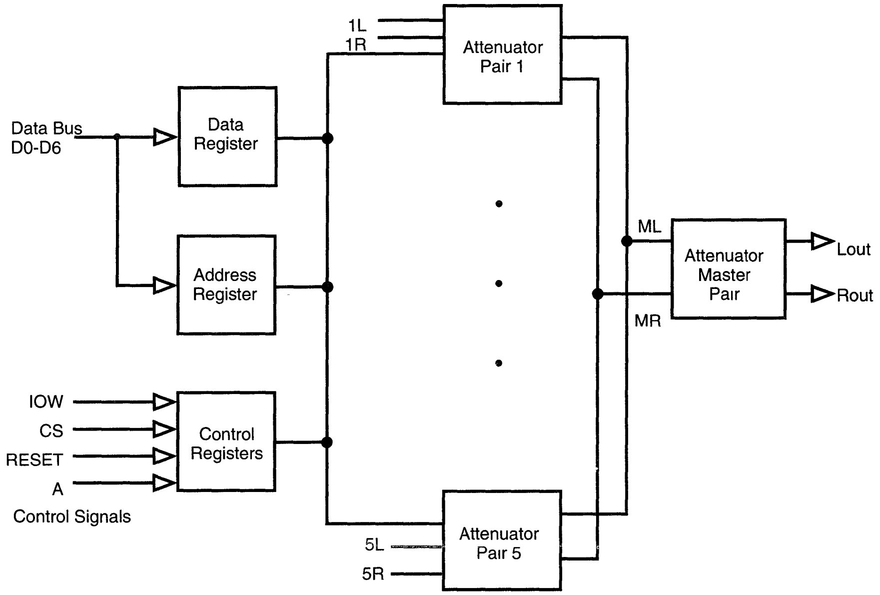
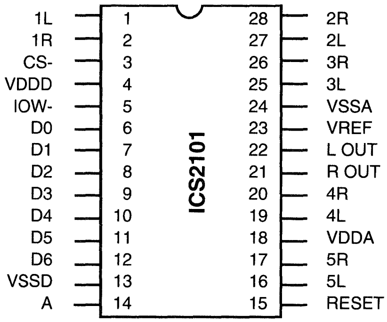


Figure 1 - Block Diagram



28-Pin DIP
28-Pin SOP
K-5, K-8

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 2, 16, 17, 19, 20, 25, 26, 27, 28	1L-5L, IR-5R	AI	Audio inputs (left and right) for attenuators 1 through 5. An external coupling capacitor should be connected to each input.
3	CS-	I	Chip select, active low.
5	IOW-	I	Input/output write, active low. Data is latched on the rising edge.
6, 7, 8, 9, 10, 11, 12	D0-D6	I	Data bus, active high.
14	A	I	Address/data select. Low input selects the data register, high input selects the address register.
15	RESET	I	Resets all registers to OOH, active high.
21, 22	Rout, Lout	AO	Line level audio outputs.
23	V_{REF}	P	Reference voltage of $0.44V_{DDA}$. A 1000 pf capacitor should be connected between V_{DDA} and V_{SSA}.
4	V_{DDD}	P	Digital power.
18	V_{DDA}	P	Analog power.
13	V_{SSD}	P	Digital ground.
24	V_{SSA}	P	Analog ground.

I=Input; O=Output; P=Power; A=Analog

Absolute Maximum Ratings

Storage Temperature. . . . . -65°C to 150°C
Voltage on any pin with
respect to ground . . . . -0.3V to V_{DDD}+0.3V
Maximum V_{DDD}. 7V
Power Dissipation. 1W

Standard Test Conditions

Operating Temperature Range . . 0°C to 70°C
Power Supply Voltage . . . . 4.75 to 5.25 Volts

DC Characteristics

V_{DDD} = 5V ± 5%, V_{SSD} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IH}	Logical 1 Input Voltage	2.4		V_{DDD}	V	
V_{IL}	Logical 0 Input Voltage	0		0.8	V	
I_{IL}	Input Leakage Current	-1		1	uA	$0 < V_{IN} < V_{DDD}$
I_{OH}	Output Source Current	-100			mA	$V_{OUT} = V_{REF} + 1V$ Master attenuator off
I_{OL}	Output Sink Current			100	mA	$V_{OUT} = V_{REF} - 1V$ Master attenuator off
V_{REF}	Internal Reference V		.44 V_{DDD}		V	
I_{ADD}	Analog Supply Current		7	10	mA	
I_{DDD}	Digital Supply Current		10	100	µA	

AC Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
ANALOG						
V_{AI}	Analog Input Voltage			3	Vp-p	AC coupled
A_F	Analog Frequency Range	20		20,000	Hz	
R_{IN}	Attenuator Input Resistance	20	32		k ohm	Gain = 0dB
T_{HD}	Total Harmonic Distortion		0.2		%	2Vp-p, 1 kHz, Gain = 0dB
S_{NR}	Signal to Noise Ratio		86		dB	Gain = 0dB BW = 20 to 20 kHz
R_{MONO}	Mono Switch Resistance	100	200	400	ohms	
N_{CR}	Crosstalk - L/R Channel		78		dB	1 kHz, 2 V_{P-P} Gain = 0db
ΔG	Analog Output Step		0.5		dB	Atten. value 127 through 16
DIGITAL						
T_{RESET}	Reset Pulse Width	200			ns	
T_{IOWL}	IOW Pulse Width Low	80			ns	
T_{IOWH}	IOW Pulse Width High	120			ns	
T_{CSS}	Chip Select Setup Time	25			ns	
T_{CSH}	Chip Select Hold Time	25			ns	
T_{DS}	Data Setup Time	25			ns	
T_{DH}	Data Hold Time	25			ns	

Timing Diagram

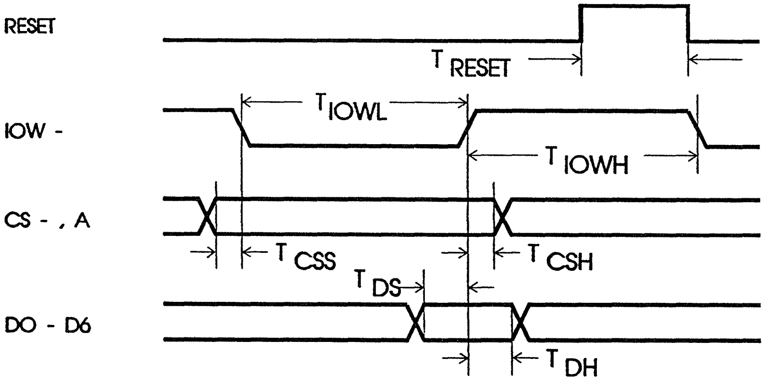


Figure 2 - Input Bus Timing

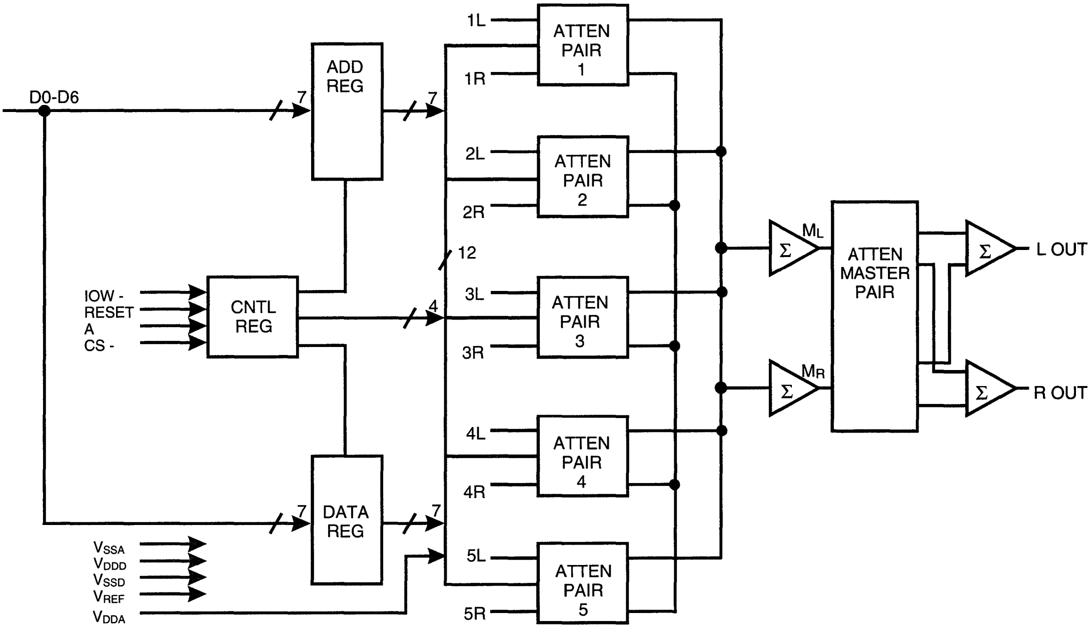
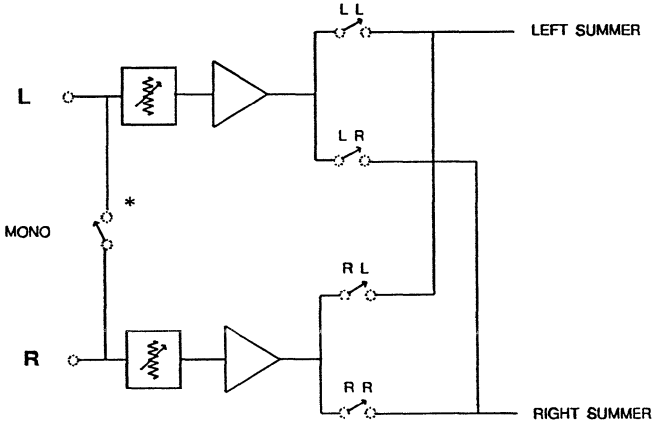


Figure 3 - Block Diagram



* The master attenuator pair does not have a mono switch; the connection between the left and right inputs is open.

Figure 4 - Attenuator Pair Detail

Programming

The **ICS2101** mixer provides two write-only registers (address and data) the host processor can use. Typically the host writes a value to the address register, selecting the appropriate data register for the subsequent data-write operations. For applications such as gradually fading one attenuator, the address register can be written to once at the beginning of the operation. A new data value is needed only when a different attenuator is selected.

Address Register

The address register is used to point to internal registers (attenuator and control).

Data Definition

D6	D5	D4	D3	D2	D1	D0
X	-	-	-	-	-	-

Attenuator Selection Control Selection

Attenuator and Control Register Selection

D6	D5	D4	D3	D2	D1	D0	Attenuator and Control Register Definition
X	X	X	X	0	0	0	Control Left
X	X	X	X	0	0	1	Control Right
X	X	X	X	0	1	0	Attenuator Left
X	X	X	X	0	1	1	Attenuator Right
X	X	X	X	1	0	X	Pan/Balance
X	0	0	0	X	X	X	Pair 1
X	0	0	1	X	X	X	Pair 2
X	0	1	0	X	X	X	Pair 3
X	0	1	1	X	X	X	Pair 4
X	1	0	0	X	X	X	Pair 5
X	1	0	1	X	X	X	Master

Attenuation Register

Each attenuator is controlled by a 7-bit value written to the control register. The values of 127 through 16 will increase the attenuation linearly in one-half decibel (dB) increments. Values of 15 through 0 will cause the attenuation to increase at an increasing rate, with a value of 00H corresponding to maximum attenuation. The channel is off when the control register value is 00H and at maximum volume (completely on) with a value of 7FH.

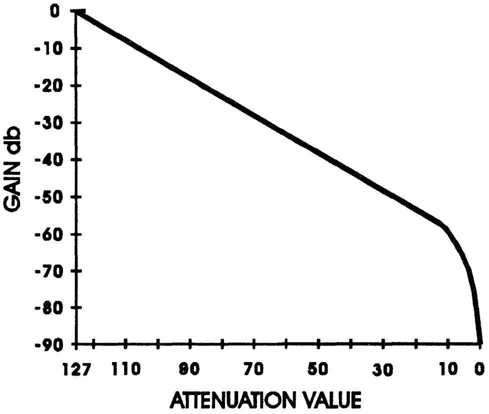


Figure 5 - Gain vs. Control Value

Modes of Operation

Each attenuator pair may operate in one of three modes:

- Normal mode
- Stereo mode
- Balance/Pan mode

Normal Mode

Normal mode is used for applications with mono inputs. In this mode, both internal attenuator (left and right) and control registers (left and right) are utilized. Each may be controlled separately.

Stereo Mode

The operation of the attenuator pair in stereo mode is controlled by the left control register. The data written to the left control register is also written to the right control register; therefore, application software need not write to the right control or right attenuation register while operating in this mode. The gain of both channels will be identical in stereo mode. The master attenuator pair does not have a mono switch and cannot be operated in any mode requiring the mono switch to be in the closed (or on) position.

Balance/Pan Mode

The operation of the attenuator pair in balance/pan mode is controlled by the left control register. The data written to the left control register is also written to the right control register; therefore, need not write to the right control or right attenuation register while operating in this mode. The balance/pan register controls the gain of the attenuator pair by regulating the balance and the pan position of the output signals. The master attenuator pair does not have a mono switch and cannot be operated in any mode requiring the mono switch to be in the closed (or on) position. The master attenuator pair cannot be used in pan mode.

In the pan/balance mode, two separate registers are used to control the attenuator pair. The attenuation value directed to the left attenuator register is modified by the contents of the pan/balance register, and the appropriate values are then written to the left and right attenuator registers. When the pan/balance register of a channel is modified, the data value has no effect on the attenuator settings until the next value is written to the left attenuator register.

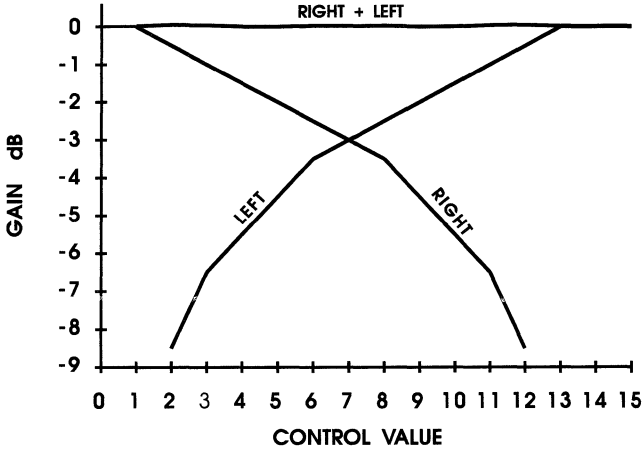


Figure 6 - Gain vs. Control Value

Modes of Operation - Data Values and Switch Settings

Right Control Register

D6	D5	D4	D3	D2	D1	D0	LL	LR	RL	RR	Mono	Mode of Operation
X	X	X	0	0	0	0	X	X	Off	Off	Off	Normal
X	X	X	0	0	0	1	X	X	On	Off	Off	Normal
X	X	X	0	0	1	0	X	X	Off	On	Off	Normal
X	X	X	0	0	1	1	X	X	On	On	Off	Normal

Left Control Register

D6	D5	D4	D3	D2	D1	D0	LL	LR	RL	RR	Mono	Mode of Operation
X	X	X	0	0	0	0	Off	Off	X	X	Off	Normal
X	X	X	0	0	0	1	On	Off	X	X	Off	Normal
X	X	X	0	0	1	0	Off	On	X	X	Off	Normal
X	X	X	0	0	1	1	On	On	X	X	Off	Normal
X	X	X	0	1	0	0	On	Off	Off	On	Off	Stereo - Normal
X	X	X	0	1	0	1	Off	On	On	Off	Off	Stereo - Reversed Channels
X	X	X	0	1	1	0	On	Off	Off	On	On	Mono
X	X	X	0	1	1	1	Off	On	On	Off	On	Mono (Reserved)
X	X	X	1	0	0	0	On	Off	Off	On	Off	Balance - Normal
X	X	X	1	0	0	1	Off	On	On	Off	Off	Balance - Reversed Channels
X	X	X	1	0	1	0	On	Off	Off	On	On	Pan - Normal
X	X	X	1	0	1	1	Off	On	On	Off	On	Pan - Reversed

Ordering Information

ICS2101N or ICS2101M

Example:

ICS XXXX M

Package Type
N=DIP (Plastic)
M=SOIC,
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

ICS2102

Sound Blaster™ Compatible Mixer

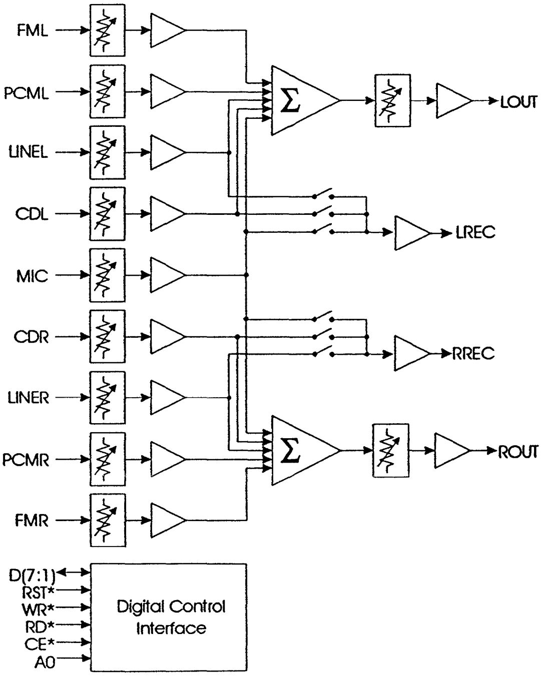
General Description

The **ICS2102** is a CMOS integrated circuit that provides mixing of 4 stereo and 1 monaural audio signals as well as master volume control. These functions are digitally controlled through Sound Blaster compatible mixer registers, an 8 bit parallel interface. The monaural microphone input has 4 levels of attenuation. The remaining 8 input channels have 8 levels of attenuation. The four stereo channels and one monaural channel are summed to form a composite signal before global volume controls are added. The master volume may be programmed with one of 8 levels of attenuation. This component performs all the necessary audio mixing for a product that is compatible with Sound Blaster Pro.™

Features

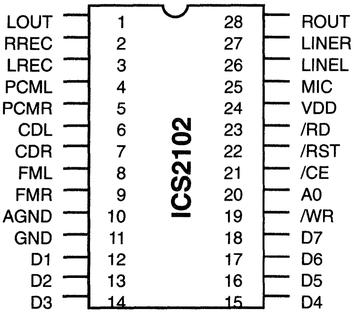
- 4 channel stereo and 1 monaural mixing
- 8 levels of independent channel input attenuation control, except microphone (4 levels)
- 8 level master volume control
- 5V CMOS process
- 28-pin SOIC package

Block Diagram



Sound Blaster and Sound Blaster Pro are trademarks of Creative Technologies, Inc

Pin Configuration



28-Pin SOIC
K-7

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
4	PCML	Analog input	Left PCM input channel
5	PCMR	Analog input	Right PCM input channel
8	FML	Analog input	Left FM input channel
9	FMR	Analog input	Right FM input channel
6	CDL	Analog input	Left CD input channel
7	CDR	Analog input	Right CD input channel
26	LINEL	Analog input	Left line input channel
27	LINER	Analog input	Right line input channel
25	MIC	Analog input	Microphone input channel
19	/WR	Digital input	Write Enable
23	/RD	Digital input	Read Enable
21	/CE	Digital input	Chip Enable
22	/RST	Digital input	Hardware Reset
20	A0	Digital input	Address bit 0
12	D1	Digital input	Data bit 1
13	D2	Digital input	Data bit 2
14	D3	Digital input	Data bit 3
15	D4	Digital input	Data bit 4
16	D5	Digital input	Data bit 5
17	D6	Digital input	Data bit 6
18	D7	Digital input	Data bit 7
1	LOUT	Analog output	Left audio output
28	ROUT	Analog output	Right audio output
3	LREC	Analog output	Left record output
2	RREC	Analog output	Right record output
11	DGND	Power	Digital ground
10	AGND	Power	Analog ground
24	V_{DD}	Power	Positive supply voltage

Pin Descriptions

xL, xR: Left and right channel inputs. These pins are used as the four pairs of inputs for the audio signals to be attenuated and then mixed. The signals applied to these pins should not exceed the supply voltage.

MIC: Microphone input. This analog signal is first attenuated and then routed to both left and right channels. It is the only mono input routed to both channels.

LOUT, ROUT: Audio output left and right. These pins are connected to buffer amplifiers that are in turn driven from the volume control. This output should be used to drive the amplifier section of the final sound reproduction system.

LREC, RREC: A second set of audio outputs used for recording one of three inputs: LINE, CD or MIC. The Input Selection Register determines which source is connected to the LREC and RREC outputs.

VDD: Digital and Analog supply. This pin supplies the analog section and digital interface of the mixer and should not be greater than 5V above the analog ground (AGND).

AGND: Analog ground. This pin is used as the negative supply of the analog section.

DGND: Digital ground. This pin is used as a reference for the digital section of the mixer. The potential at this pin should be externally tied to the chasis ground on the board where AGND is also connected.

A0: Address bit 0. This pin, when driven low, determines that the incoming data is an index. When high, the incoming data is data to set the register indicated on the previous data transfer.

/WR: Write Pulse (Low Active). The write line is pulsed low while the chip enable line is a low. A 7 bit data load will occur using data pins 1 to 7.

/RD: Read Pulse (Low Active). The read line is pulsed low while the chip enable line is low. A 7 bit data read will occur using data pins 1 to 7.

/CE: Chip Enable (Low Active). This line should be pulsed low in order to initiate a transfer of control information to the digital control section. If this line and the write line are low, a byte transfer will occur.

/RST: Hardware Reset (Low Active). This line resets the default setting of the mixer. The application circuit will use the inverted version of the PC reset line.

D1-7: Data bits 1-7: These lines are used for parallel transfers to the digital control section. A parallel transfer occurs when both the chip enable (/CE) and write pulse (/WR) or read pulse (/RD) lines are low. D0 (LSB), not having any impact on both index (address) decoding or actual data, has been omitted.

Registers

Overview

Communication to each internal register of the mixer requires that two byte transfers are completed. The first byte must contain the index (or address) of the register which is to be loaded. The second byte should contain the data that is to be written. The external address line A0 is used to discriminate between an index write and a data write. If the A0 is set to a logic 0, it is identified as an index transfer and if it is set to a logic 1, then the transfer is identified as data. The data transfer is valid only when /CE pin is pulsed low. In this manner an 8 bit bus with multiple uses can be shared for communication.

Register Maps

Address transfer definitions

An address transfer is one in which A0 bit is set to a logic 0, whatever the base address might be. The decode of this address is as follows:

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Accessed Register** (Hex)
Mixer Data Reset							00/01
Left PCM Input			X/1	Right PCM Input			04/05
		X/0	X/1	X/0	MIC Input		0A/0B
		X/0	X/1	X/0	Input Sel.		0C/0D
L. Master Volume			X/1	R. Master Volume			22/23
Left FM Input			X/1	Right FM Input			26/27
Left CD Input			X/1	Right CD Input			28/29
Left Line Input			X/1	Right Line Input			2E/2F

X/1=Ignored on write operations, read back as 1
X/0=Ignored on write operations, read back as 0

Ghost Address definitions

Some of the actual registers described on the previous page are duplicated by partial decoding. Omitting certain address bits for decoding, the decode is as follows:

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Accessed Register** (Hex)
L. Master V. Ghost			X/1	R. Master V. Ghost			02/03
Left FM Ghost			X/1	"Right" FM Ghost			06/07
Left CD Ghost			X/1	"Right" CD Ghost			08/09

Channel control register (except Microphone input)

D3/D7	**D2/D6**	**D1/D5**	**D4**	**Function**
0	0	0	X/1	Mute this channel
0	0	1	X/1	28dB attenuation
0	1	0	X/1	21.5dB attenuation
0	1	1	X/1	16dB attenuation
1	0	0	X/1	11dB attenuation
1	0	1	X/1	7dB attenuation
1	1	0	X/1	3.3dB attenuation
1	1	1	X/1	0dB attenuation

There are 5 control registers in the **ICS2102**. The higher 3 bits of each nibble register selects the desired level of attenuation for that channel. The lowest level of attenuation (or highest volume) corresponds to a setting of all 1s for the attenuation field. Attenuation steps increase at varying dB per step until 28dB is reached with a register value in the attenuation field of 001x. The final step does not simply add an additional 6dB attenuation but acts as a mute function by completely killing the input.

The only exception to this is the Microphone input attenuation control that uses D[2-1] for the 8 levels.

Microhone Input Control Register

D2	D1	Function
0	0	Mute this channel (Default)
0	1	19dB attenuation
1	0	11dB attenuation
1	1	6dB attenuation

Input Selection Register

D2	D1	Function
0	0	Microphone (Default)
0	1	CD Input
1	0	Microphone
1	1	Line-In

Default Settings

The default values are set when the part is powered on. The same default values are also set when a hardware reset (low active, pin /RST) occurs. When reset by writing to 00 index (Data Reset register), the **ICS2102** sets the input attenuations of the FM, PCM inputs and the master volume to 99h, while all others are muted (00h). The recording selector switch connects the microphone input to the recording path.

Register Descriptions

Reset Register (Index 00)

When the PC writes any value to this register, the mixer will reset, and all registers will return to their default values. The reset occurs with a write to this register. The default values will load once the data is also written.

PCM Volume Register (Index 04)

The PC uses this register to set the PCM input attenuation level. This register can also be programmed by writing to the lower nibble of index register 24h. When programmed in this way, the lower nibble written will set both the left and right PCM volumes. The default value for this register is 99h.

MIC Input Attenuation Register (Index 0A)

The recording volume of the microphone input is set through this register. The setting of the levels is described in a previous table. The default value for this register is 00h.

Input Selector for Recording (Index 0C)

The recording of a single channel is defined through the selection described in the previous table.

Master Volume Register (Index 22)

The PC uses this register to set the overall volume level. This register can also be programmed via the lower nibble of index register 02h. When programmed this way, the nibble written will set both the left and right master volumes. The default value for this register is 99h.

FM Volume Register (Index 26)

The PC uses this register to set the FM input attenuation level. This register can also be programmed by writing to the lower nibble of index register 06h. When programmed this way, the lower nibble will set both the left and right FM volume settings. The default value for this register is 99h.

CD Volume Register (Index 28)

The PC uses this register to set the CD input attenuation level. This register can also be programmed by writing to the lower nibble of index register 08h. When programmed this way, the lower nibble will set both the left and right CD volume settings. The default value for this register is 00h.

Line In Volume Register (Index 2E)

The PC uses this register to set the line-in input attenuation level. The default value for this register is 00h.

Ghost Registers

Master Volume Ghost Register (Index 02)

When this register is written, the lower nibble (bits 3-0) are written to both the left and right Master volume settings at index register 22h. The default value for this register is 99h.

FM Volume Ghost Register (Index 06)

When this register is written, the lower nibble (bits 3-0) are written to both the left and right FM volume settings at index register 26h. The default value for this register is 99h.

CD Volume Ghost Register (Index 08)

When this register is written, the lower nibble (bits 3-0) are written to both the left and right CD volume settings at index register 28h. The default value for this register is 00h.

Absolute Maximum Ratings

All voltages measured with respect to ground potential node where AGND and DGND are connected.

T_A=0°C to 70°C unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT	UNIT
Positive Supply Voltage	V_{DD}	V_{DD}	-0.3 to +7.0	V
Digital Input Voltage	V_{IN}	All digital inputs	-0.3 to V_{DD}+0.3	V
Analog Input Voltage	V_{INA}	All analog inputs	V_{SS}-0.3 to V_{DD}+0.3	V
Storage Temperature	T_{stg}		-25 to 120	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

T_A=0°C to 70°C unless otherwise noted

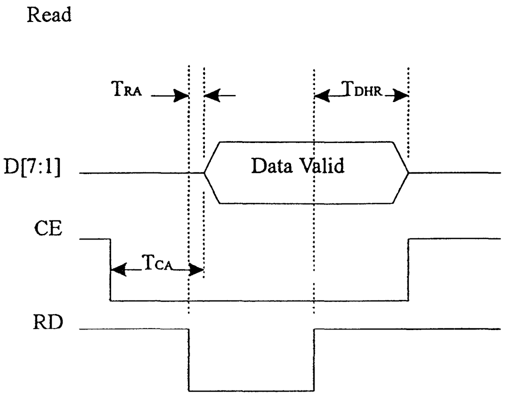
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive Supply Voltage	V_{DD}	V_{DD}	4.75	5	5.25	V
Digital Input Voltage	V_{IN}	All digital inputs	-0.3		V_{DD} +0.3	V
Analog Input Voltage	V_{INA}	All analog inputs	V_{SS} -0.3		V_{DD} +0.3	V
Storage Temperature	T_{stg}		0		70	°C

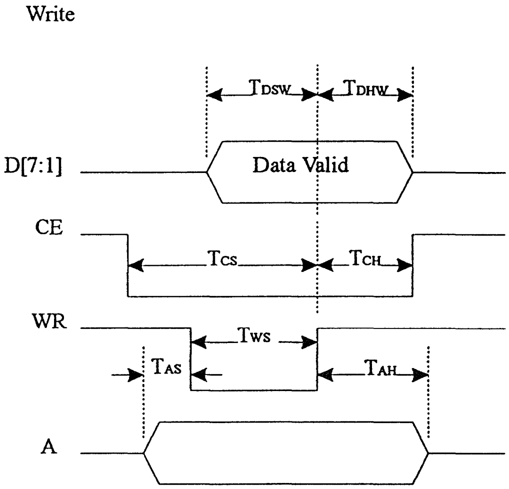
Electrical Characteristics

The following characteristics apply for DV_{DD}=5V, V_{DD}=5V supply voltage, f_{IN}=1 kHz and V_{IN}=.3V_{rms} input signal; master volume and input attenuation all 0dB, unless otherwise specified. All limits apply for T=25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{VDD}	All xL/xR inputs, volumes mute; all digital inputs at GND level, except /CE, A0, /WR and /RD at V_{DD}		12	15	mA
Input Voltage (RMS)	V_{IN}	THD=0.5%, RL=10kΩ	1			V
Total Harmonic Distortion	THD	1 V_{rms}, R_L=10kΩ; f_{IN}=100 Hz		.08	0.5	%
		f_{IN}=1 kHz		.13	0.5	
		f_{IN}=10 kHz		.65	0.8	
DC Operating Voltage	V_O	@ LOUT, ROUT		2.14		V
AC Output Impedance	r_{out}	LOUT, ROUT, R_L=10kΩ		100	1k	Ω
Input Impedance	r_{in}	xL, xR	100k	300k		Ω
Volume Control		Maximum setting (0dB)	-0.5	0	0.5	dB
		Minimum setting (28db)	-26	-28	-29	
Volume Step Size Error		(Actual-Nom)/Nom			5	%
Channel Separation		Inputs mute. Drv xL, monitor xR	-60			dB
Input Attenuation Control		Maximum setting (0db)	-0.5	0	0.5	dB
except Microphone input)		Minimum setting (28dB)	-26	-28	-29	
(Microphone input only)		Minimum setting (-19dB)	-18	-19	-20	
Input Attenuation Step Size Error					5	%
Mute Attenuation		V_{IN}=1V_{rms}, xL, xR	72			dB
Frequency Response		f_{IN}=0.02-20 kHz, rel. to 1 kHz			±0.2	dB
Signal-to-Noise Ratio	SNR	V_{IN}=1V_{rms}	72	85		dB
Power Supply Rejection Ratio	PSRR	Apply .2V_{rms}, 100 Hz to V_{DD}; mute inputs. Check LOUT		-6		dB
Read Access Time	T_{RA}		50			ns
Chip Enable Access Time	T_{CA}		50			ns
Data Read Hold Time	T_{DHR}		25			ns
Chip Enable Setup Time	T_{CS}		50			ns
Write Strobe Time	T_{WS}		20			ns
Address Setup Time	T_{AS}		5			ns
Address Hold Time	T_{AH}		5			ns
Chip Enable Hold Time	T_{CH}		5			ns
Data Write Setup Time	T_{DSW}		20			ns
Data Write Hold Time	T_{DHW}		5			ns
Logic "1" Input	VIH	Digital signals	2.0			V
Logic "0" Input	VIL	Digital signals			0.8	V

Interface Timing Definitions





Ordering Information

ICS2102M

Example:

ICS XXXX M

Package Type
M=SOIC
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS2115

WaveFront™ Synthesizer

General Description

The WaveFront Synthesizer, **ICS2115**, is an audio synthesis chip which utilizes wavetable lookup to produce 16-bit, CD quality sound. The internal memory management unit allows both ROM, for standard samples, and low cost DRAM, for soft loadable samples, to be connected directly to the **ICS2115**. The WaveFront Synthesizer presents the audio output in 16-bit linear form for conversion by a low cost CD-type DAC.

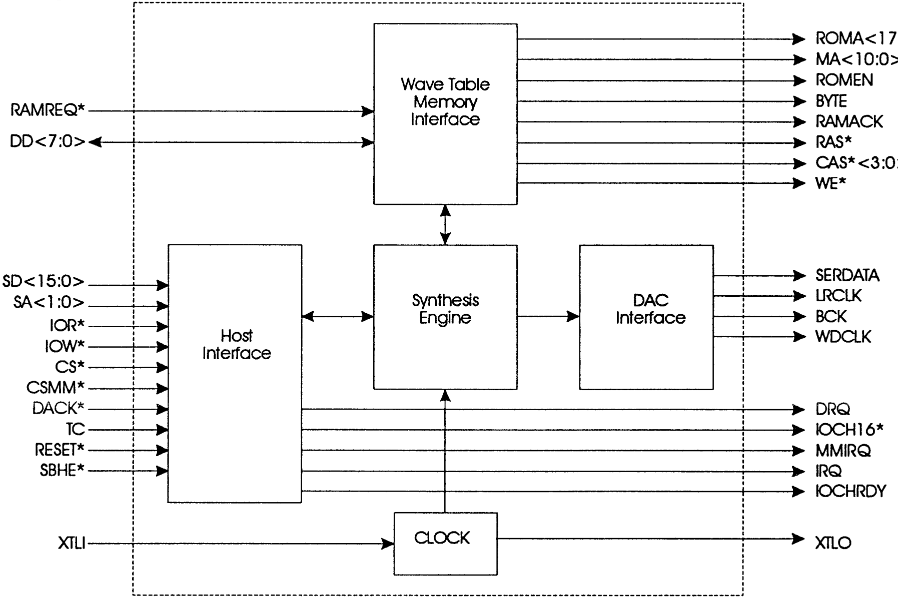
Features

- Capable of addressing up to 32 MB of wavetable ROM and up to 16 MB of wavetable DRAM
- Variable Polyphony Rates: 24 voices at 44.1 kHz through 32 voices at 33.8 kHz
- Uses 16 bit linear, 8 bit linear, and 8 bit u-Law wavetable data.
- Serial output for a CD player-type DAC
- Capable of using either a 68EC000 (with the ICS2116) or an ISA-based host for software control
- Part of a complete design package that includes software drivers for Windows and DOS

Applications

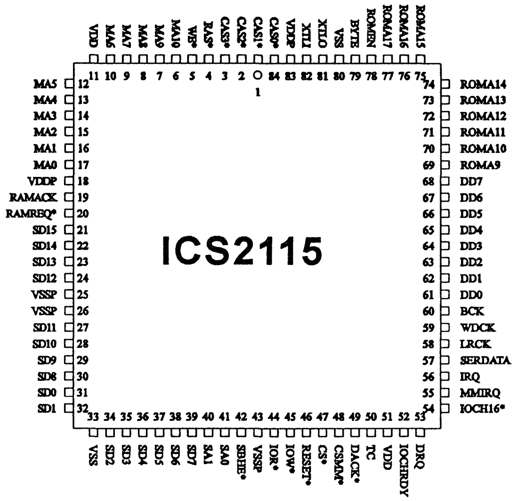
- ISA based sound cards
- Wavetable synthesizer daughter cards
- External sound modules that connect to a PC's serial or parallel port
- Any system requiring a self contained unit that provides high quality music synthesis of General MIDI sounds, in a low cost design

Block Diagram

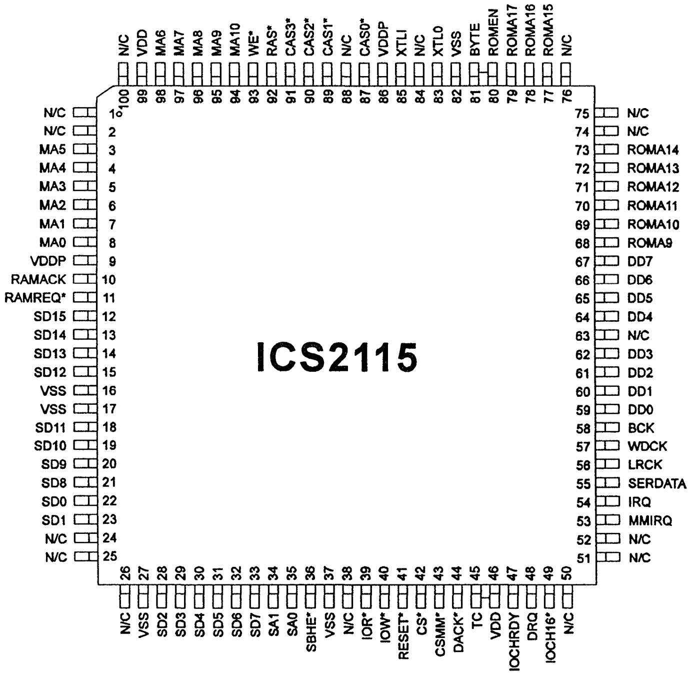


WaveFront is a trademark of Integrated Circuit Systems, Inc

Pin Configuration



84-Pin PLCC
K-10



100-Pin TQFP
K-12

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
6-10, 12-17	MA<10:0>	TPUP2	Wavetable Muxed Address Bus
69-77	ROMA<17:9>	O	Wavetable ROM Address
1-3, 84	/CAS<3:0>	O2	Wavetable DRAM Column Address Strobe
61-68	DD<7:0>	B	Wavetable Data Bus
4	/RAS	O2	Wavetable DRAM Row Address Strobe
5	/WE	TPUP	Wavetable DRAM Write Enable
78	ROMEN	O	Wavetable ROM Enable/Byte Enable
79	BYTE	O	Wavetable ROM Byte Mode
20	/RAMREQ	IPUP	Wavetable DRAM cycle request
19	RAMACK	O	Wavetable DRAM cycle acknowledge
27-32, 34-39	SD<15:0>	B	Host Interface Data Bus
40-41	SA<1:0>	I	Host Interface Address Bus
44	/IOR	I	Host Interface Read Strobe (Active Low)
45	/IOW	I	Host Interface Write Strobe (Active Low)
42	/SBHE	IPUP	Host Interface Sixteen Bit Hardware Enable
54	/IOCS16	SINK	Host Interface I/O Channel Sixteen Wide
47	/CS	I	Host Interface Synthesizer Chip Enable
48	/CSMM	I	Host Interface Chip Select for MIDI Interface Emulation
53	DRQ	SOURCE	Host Interface DMA Request
49	/DACK	I	Host Interface DMA Acknowledge
50	TC	I	Host Interface DMA Terminal Count
52	IOCHRDY	SINK	Host Interface I/O Channel Ready
56	IRQ	B2	Host Interface Synthesizer IRQ
55	MMIRQ	SOURCE	Host Interface MIDI IRQ
46	/RESET	IPUPS	Hardware Reset (Active Low)
57	SERDATA	O	Serial Data Output
58	LRCK	O	Left/Right Clock
59	WDCK	O	Word Clock
60	BCK	O	Bit Clock
81	XTLO	O (special)	Crystal or N/C
82	XTL1	I (special)	Crystal or Clock Input
11, 51	VDD	PWR	Power for chip core
18, 83	VDDP	PWR	Power for pad ring
33, 80	VSS	GND	Ground for chip core
25, 26, 43	VSSP	GND	Ground for pad ring

Pin Type Descriptions

PIN TYPE	INPUT TYPE	DRIVE	PULLUP R	PULL-DOWN R	NOTES
I	TTL	none	none	none	TTL Input
IPUP	TTL	none	yes	none	TTL Input with pull-up
IPUPS	SCHMIDT	none	yes	none	SCHMIDT Input with pull-up
O	n/a	standard	none	none	Output
O2	n/a	high	none	none	High Drive Output (200pf max load)
B	TTL	standard	none	none	TTL Bi-directional
B2	SCHMIDT	standard	none	yes	Drive only with pull-up
TPUP	n/a	standard	yes	none	Tristate with pull-up
TPUP2	n/a	medium	yes	none	Tristate (medium drive) with pull-up (125pF max load)
SINK	n/a	standard	yes	none	Drive low only with pull-up
SOURCE	n/a	standard	none	yes	Drive high only with pull-down
PWR	n/a	n/a	none	none	Power terminal
GND	n/a	n/a	none	none	Ground terminal

Absolute Maximum Ratings

Supply Voltage	-0.5V to 7.0V
Logic inputs	-0.5V to V_{DD} + 0.5V
Ambient operating temp.	0°C to 70°C
Storage temperature	-65°C to 150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

DC Electrical Characteristics

$V_{CC} = 5.0V \pm 10\%$; GND = 0V; $T_A = 0°C$ to $70°C$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		4.75	5.00	5.25	V
TTL Input Voltage Low	V_{IL}		-0.30		0.80	V
TTL Input Voltage High	V_{IH}		2.20		VDD+0.30	V
Schmidt Input Voltage Low	V_{ILS}		-0.30		1.50	V
Schmidt Input Voltage High	V_{IHS}		3.00		VDD+0.30	V
XTLI Input Voltage Low	V_{ILX}		-0.30		1.50	V
XTLI Input Voltage High	V_{IHX}		3.50		VDD+0.30	V
Output Low Current Standard Drive	I_{OL}	V_{OL}=0.4V	4.0	6.0		mA
Output High Current Standard Drive	I_{OH}	V_{OH}=2.8V		-6.0	-4.0	mA
Output Low Current Medium Drive	I_{OL2}	V_{OH}=0.4V	6.0	9.0		mA
Output High Current Medium Drive	I_{OH2}	V_{OH}=2.8V		-9.0	-6.0	mA
Output Low Current High Drive	I_{OL3}	V_{OH}=0.4V	9.0	12.0		mA
Output High Current High Drive	I_{OH3}	V_{OH}=2.8V		-12.0	-9.0	mA
Input Leakage Current Standard Inputs	I_{IN}	VSS < V_{IN} < VDD	-1.0		1.0	uA
pull-up Current	I_{PUP}	V_{IN} = VSS	15.0	30.0	50.0	uA
pull-down Current	I_{PDN}	V_{IN} = VDD	50.0	90.0	150.0	uA
XTLI Input/ Output Capacitance	C_{XTL}			20.0		pf

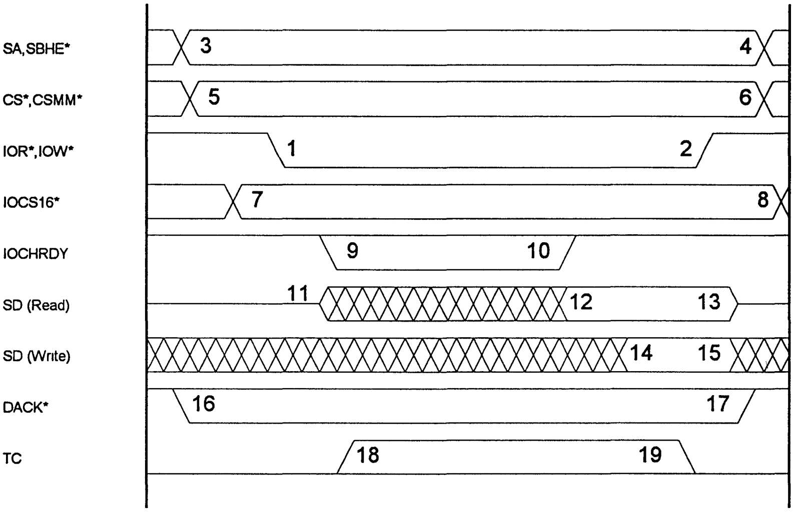
Note: All pins have a maximum capacitive load of 50pf unless noted otherwise.

AC Electrical Characteristics

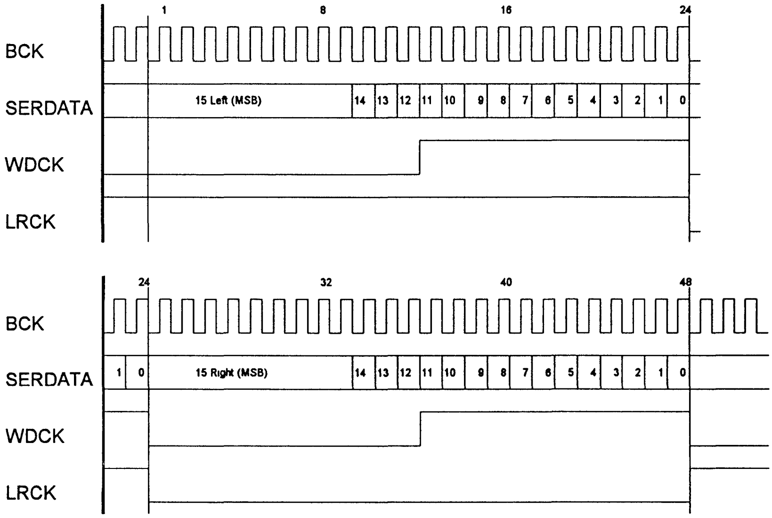
Please reference the timing diagram titled *Host Interface Timing*, below.

HOST INTERFACE AC TIMING PARAMETERS						
PARAMETER	SYMBOL	FROM	TO	MIN	MAX	UNITS
Address setup to command	t_{AS}	3	1	10	-	nS
Chip select setup to command	t_{CS}	5	1	10	-	nS
Address hold from command	t_{AH}	2	4	10	-	nS
Chip select hold from command	t_{CH}	2	6	10	-	nS
Command width	t_{CW}	1	2	100	-	ns
Address valid to /IOCS16 delay	t_{AID}	3, 5	7	0	50	nS
/IOCS16 hold from address invalid	t_{IH}	4, 6	8	0	50	nS
Write data setup	t_{DS}	14	2	50	-	nS
Write data hold	t_{DHW}	2	15	10	-	nS
Read data delay (ready access)	t_{DD}	1	12	0	60	nS
Read data hold	t_{DHR}	2	13	0	20	nS
/DACK setup to command	t_{DAS}	16	1	20	-	nS
/DACK hold after command	t_{DAH}	2	17	50	-	nS
TC setup to command	t_{TS}	18	2	25	-	nS
TC hold after command	t_{TH}	2	19	n/a	-	nS
TC width	t_{TW}	18	19	20	-	nS

Timing Diagrams

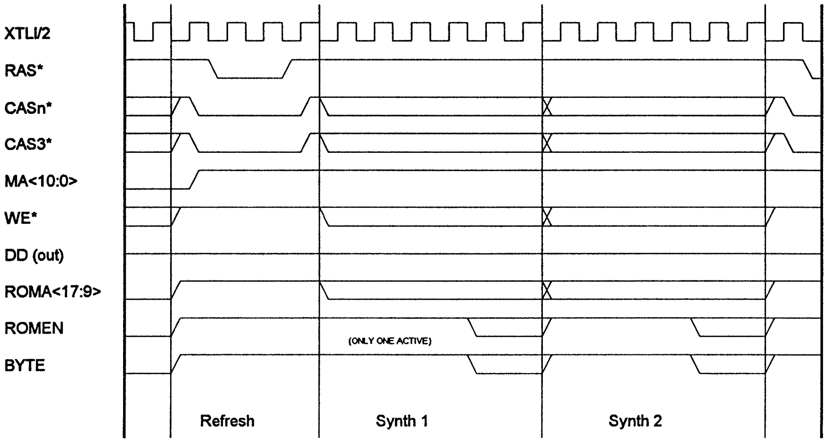


Host Interface Timing

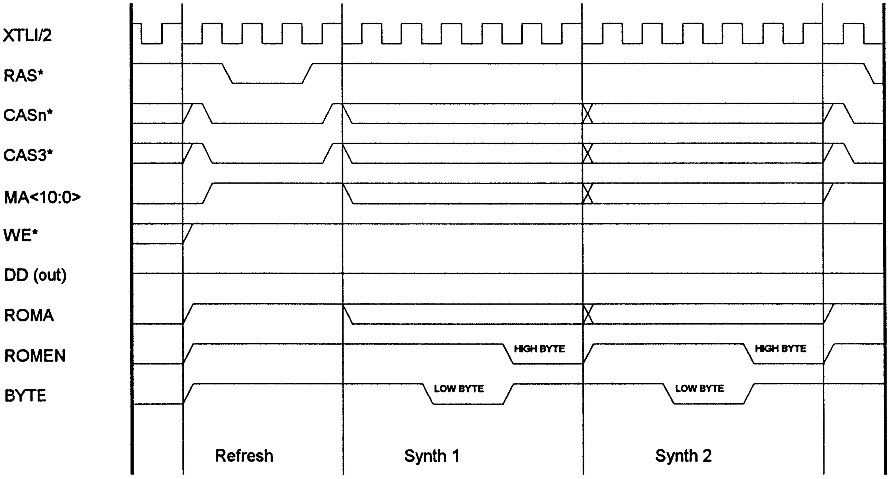


Notes:
- BCK is XTLI frequency divided by four
- 'Extra' cycles are appended as needed for the number of voices
- BCK continues to run for all 'extra' cycles

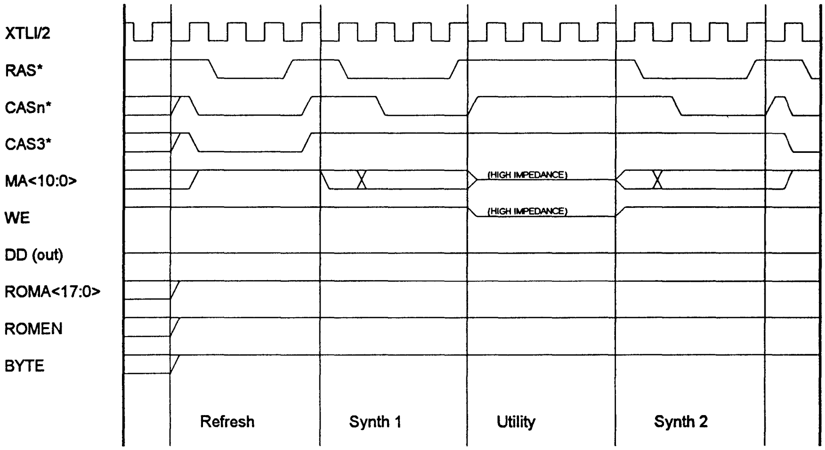
DAC Output Timing



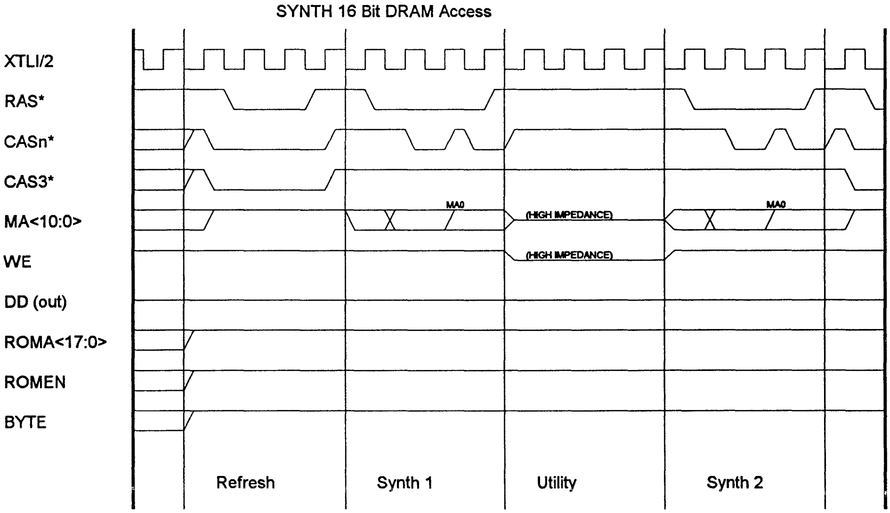
8 Bit/u-Law Access of Wavetable ROM



16 Bit Access of Wavetable ROM



8 BIt/u-Law Access of Wavetable DRAM



16 Bit Access of Wavetable DRAM

Miscellaneous Pins

VDD, VDDP

These are the chip power supply pins. VDD pins power the core logic, while VDDP pins power the pad ring. This arrangement helps prevent switching spikes due to output transitions from disturbing the internal operation of the chip. These pins MUST be at the same potential externally.

VSS, VSSP

These are the chip ground pins. VSS pins ground the core logic, while VSSP pins ground the pad ring. This arrangement helps prevent switching spikes due to output transitions from disturbing the internal operation of the chip. These pins MUST be at the same potential externally.

XTLI, XTLO

These pins comprise a self-contained oscillator circuit for primary chip clock generation. No external components (other than the crystal itself) are required for fundamental mode operation. There is approximately 20pF of capacitance at each pin, and a DC bias feedback between the pins for startup and biasing.The standard crystal frequency is 33.868800 MHz (for 24 oscillators at 44.1 kHz or 32 oscillators at 33.8 kHz). Due to the expense of fundamental mode crystals of this frequency, the oscillator can be operated in 3rd overtone mode with the addition to the XTLO pin of a series network to ground of a 1.0H inductor and a 0.001F capacitor. In this case, the crystal fundamental frequency will be 11.2896 MHz.

When an external clock is supplied, XTLO should be left floating. XTLI should be connected to the clock source via a series capacitor (0.001uF is recommended). Duty factor is not critical, since the clock is internally divided by two.

Host Interface

The **ICS2115** can interface with the ISA bus or directly with the ICS2116. For more information, refer to the WaveFront Application Notes. (Please reference the timing diagram titled *Host Interface Timing*, above.)

/CS

This input pin selects read/write access to the internal indirect registers, as selected by SA<1:0>. This signal must be stable before, during, and after /IOR or /IOW strobes.

/CSMM

This input pin selects read/write access to the Media Master and MIDI interface emulation registers, as selected by SA<1:0>. This signal must be stable before, during, and after /IOR or /IOW strobes.

SA<1:0>

These address input pins select one of four direct mapped registers as determined by the /CS and /CSMM pins. These signals must be stable before, during, and after /IOR or /IOW strobes.

/SBHE

This input pin determines the access width for even addresses, and is ignored for odd addresses. It should be connected directly to the ISA bus for a 16-bit card. For 8-bit cards, it should be tied high.

/IOCS16

This output pin indicates to the host that the current address is accessible as a word-wide (sixteen bit) data entity. It is based on the current value of the indirect register address, SA<1:0>, and /CS selecting a word-wide internal register. Under these conditions, /IOCS16 drives low; otherwise, it is a resistive high. This output pin is unused with systems that contain the ICS2116. /IOCS16 requires an external pull-up of 3.3K.

SD<15:0>

This is the bi-directional data bus used for all register data transfers.

/IOR

This input pin is used to read registers when low. SA<1:0>, /CS, /CSMM, and /SBHE must be stable before, during, and after the active low pulse on /IOR.

/IOW

This input pin is used to write registers when low. SA<1:0>, /CS, /CSMM, and /SBHE must be stable before, during, and after the active low pulse on /IOW. SD<15:0> must be stable before, during, and after the trailing (rising) edge of /IOW.

IOCHRDY

This output pin is normally in a resistive pull-up state. During /IOR or /IOW low times, this pin can become active (drive low) to indicate to the host that the requested data transfer is not ready, and that /IOR or /IOW should be held (stretched) until ready is signaled by IOCHRDY deactivating (resistive high). IOCHRDY requires an external pull-up of 3.3K.

/DACK

This input, when low, identifies the current IO operation as a DMA acknowledge operation. The current IO operation will interact with the DMA control logic in the **ICS2115** as programmed, and cause DRQ to be de-asserted. This input must be held before, during, and after the IO command signal (/IOR or /IOW low).

TC

This input (along with /DACK being low) signals that the current DMA operation is the last transfer, and that the **ICS2115** should shutdown its DMA logic after the current transfer is complete.

DRQ

This output pin is normally in a resistive low state. When DMA operation has been programmed and the proper status exists, the DRQ pin will drive high to indicate that the **ICS2115** is ready to accept a DMA data transfer. Upon receipt of a low on the /DACK input, DRQ will return to the resistive low state. When the **ICS2115** is ready to continue DMA transfers, DRQ will again be asserted. This sequence repeats until DMA is terminated by either TC or a register write. DRQ requires an external pull-down of 1K.

MMIRQ

This output is normally in a resistive low state. Whenever an active *Media Master* interrupt occurs, it will drive high. When the interrupt condition is cleared, the pin returns to a resistive low state. MMIRQ requires an external pull-down of 1K.

IRQ

This output is normally in a resistive low state. Whenever an active internal interrupt occurs, it will drive high. When the interrupt condition is cleared, the pin returns to a resistive low state. IRQ requires an external pull-down of 1K.

/RESET

This input is the active low hardware reset for the **ICS2115**.

DAC Output

The **ICS2115** is designed to directly interface with consumer CD player type digital to analog converters. The interface is a 48 clock, MSB first, left/right multiplexed data stream. Depending on the number of oscillators enabled, there will be additional idle clocks generated after the data is output. (Please reference the timing diagram titled *DAC Output Timing*, above.)

Some DACs that may be used are:

- Phillips TDA1545
- NEC UDP6376

BCK

This output pin is the bit clock for the DAC. The frequency of BCK is the frequency of XTLI divided by four. It always runs, even when the system has not initialized itself. The other DAC interface signals change on the falling edge of BCK, and are stable on the rising edge of BCK.

SERDATA

This output is the accumulated data of all **ICS2115** oscillators, presented as signed binary two's complement data, MSB first. The internal 16 bit data is sign-extended to 24 bits, and presented left then right.

LRCK

LRCK indicates the stereo channel of the data just shifted out. It will transition high to low after bit 0 of the left data has been output, and transition low to high after bit 0 of the right data has been output.

WDCK

WDCK indicates the framing of the data being shifted out. It will transition low to high between bits 12 and 11 of both the left and right data words. It transitions high to low after bit 0 of both the left and right data words.

Wavetable Memory Interface

(Please reference the timing diagrams that show the wavetable memory access cycles, above.) The **ICS2115** is designed to directly interface to the following memory components:

- dynamic RAM meeting the following parameters:
  - 80nS access time
  - Fast Page mode operations
  - CAS-before-RAS auto-refresh
  - 256K (9 addresses) to 4M (11 addresses) by 1 or 4 (configured as byte wide)

SIMM's with an access time better than 80ns can also be used.

- ROM meeting the following parameters:
  - 150nS address access time
  - 70nS output enable access times
  - byte-wide output

The ICS2122-001, ICS2124-001 and ICS2124-002 comprise the ICS 2 MB and 4 MB patch sets respectively. Users of the WaveFront chipset can either buy ROMs directly from ICS or purchase the mask and produce the wavetable ROMs independently.

Pin descriptions follow.

DD<7:0>

This bus is a bi-directional data bus for the wavetable data. It functions as an input under all operations except for DMA writes to DRAM. This bus connects directly to the data pins of all wavetable DRAM and ROM.

MA<10:0>

This output bus drives addresses to both DRAM and ROM wavetable memory.

/CAS<3:0>

These outputs function as both /CAS inputs to up to four banks of DRAM and as addresses to ROM. For a DRAM cycle, only one of these four outputs will toggle active (low) at a time. For a refresh cycle, they all toggle low to refresh all DRAM simultaneously.

/RAS

This output connects to the /RAS pin of all wavetable DRAM chips /RAS is generated for all DRAM access and refresh cycles, and remains high for all ROM cycles so that the /CAS pins can be used as ROM addresses.

/WE

This tristate output connects to the /WE pin of all wavetable DRAM. It is normally in a driven (or resistive) high state. It toggles low only for DMA write cycles.

ROMA<17:9>

This bus provides addresses for ROM based oscillators. During refresh and DRAM cycles, these pins are driven high. The MA<10:0> and CAS<3:0> multiplex to provide the other address bits for the wavetable ROM. The table below shows the exact relation.

Wavetable ROM address	ICS2115 Signal
A0	MA<0>
A1	MA<1>
A2	MA<2>
A3	MA<3>
A4	MA<4>
A5	MA<5>
A6	MA<6>
A7	MA<7>
A8	MA<8>
A9	RA<9>
A10	RA<10>
A11	RA<11>
A12	RA<12>
A13	RA<13>
A14	RA<14>
A15	RA<15>
A16	RA<16>
A17	RA<17>
A18	/CAS<3>
A19	MA<9>
A20	MA<10>
A21	/CAS<0>
A22	/CAS<1>
A23	/CAS<2>

BYTE

BYTE functions as Low Byte /OE for the low byte ROM of a 16-bit ROM pair. When using the ICS2122-001, this connects to the output enable on the ROM. When using the 4 MB patch set, BYTE connects to the /OE on the ICS2124-001.

ROMEN

ROMEN functions as High Byte /OE for the high byte ROM of a 16-bit ROM pair. For systems using the ICS2122-001, this pin is unused. When using the 4 MB patch set, ROMEN connects to the /OE on the ICS2124-002.

/RAMREQ

This input pin is used to request an external memory cycle. Its function is unused in the present design. /RAMREQ should be tied high.

RAMACK

This output pin provides acknowledgment of an external memory cycle. It is unused in the current design.

MPU-401/6850 Emulation Registers

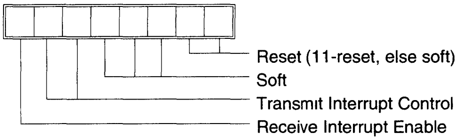
These 4 registers will be mapped at an offset determined by the /CSMM input. The WaveFront Synthesizer only decodes the least significant 2 address bits. For identification purposes, this document refers to these registers as Emulation Base + 0 through Emulation Base + 3.

MIDI Emulation Control/Status Register

The MIDI Control Status register can be configured as either a 6850 compatible or an MPU-401 compatible UART. The WaveFront Operating System writes to the InDEmulMode Register to indicate the mode of emulation.

6850 Mode Control (Emulation Base + 0) (Write Only)

The host can access this MIDI control register by writing to this address. The control register is mapped as follows.



MIDI (6850) Control Register

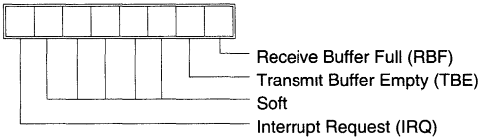
1:0 - Reset - Resets the MIDI Port
- 11 = Reset (Resets Receive Interrupt and Receive Interrupt Enable)
- 00, 01 and 10 = No Reset

4:2 - Soft - Software controlled functions
6:5 - Transmit Buffer Empty Interrupt Control
- 01 = Interrupts are enabled
- 00, 10 and 11 = Interrupts disabled

7: - Receive Buffer Full Interrupt Enable
- 1 = Interrupts enabled
- 0 = Interrupts disabled

6850 Mode Status (Emulation Base + 0) (Read Only)

The host can access this MIDI status register by reading this address. The status register is mapped as follows.



MIDI (6850) Status Register

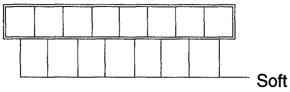
0: - Receive Buffer Full
- 1 = full
- 0 = empty

1: - Transmit Buffer Empty
- 1 = empty
- 0 = full

6:2 - Soft
7: - Interrupt Request
- 1 = Interrupt pending
- 0 = Interrupt not pending

MPU-401 Mode Control (Emulation Base + 1) (Write Only)

The host can access this MIDI control register by writing to this address. The control register mapping is software dependent.

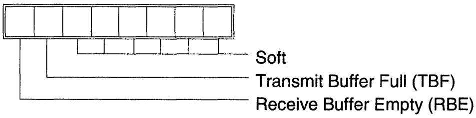


MIDI (MPU-401) Control Register

7:0 - Soft - Software controlled functions

MPU-401 Mode Status (Emulation Base + 1) (Read Only)

The host can access this MIDI status register by reading this address. The status register is mapped as follows.



MIDI (MPU-401) Status Register

5:0 - Soft
6: - Transmit Buffer Full
    1 = full
    0 = empty
7: - Receive Buffer Empty
    1 = empty
    0 = full

MIDI Emulation Data Register

This register is the MIDI data port for writing and reading MIDI data. The host can transfer MIDI data between itself and the WaveFront Operating System via this register.

6850 Mode Data (Emulation Base + 1) (Read/Write)

Eight bit data.

MPU-401 Mode Data (Emulation Base + 0) (Read/Write)

Eight Bit data

Registers Emulation Base + 2 and Emulation Base + 3

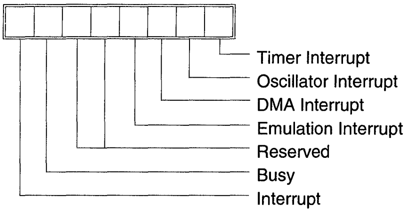
These registers are reserved when the **ICS2115** is in the host configuration

Synthesizer Registers

In the **ICS2115**, the Synthesis and General Purpose registers are accessed indirectly via the Indirect I/O Registers. These 4 registers will be mapped at an offset determined by the /CS input. For identification, this document refers to these registers as Synthesizer Base + 0 through Synthesizer Base + 3.

Synthesizer Base + 0	R	IRQ/Status
Synthesizer Base + 1	R/W	Register Address
Synthesizer Base + 2	R/W	Data Low Byte/Word
Synthesizer Base + 3	R/W	Data High Byte/Byte

Interrupt status (Synthesizer Base + 0) Read Only



Interrupt Status Register

Note: Reading this Register does NOT clear any of the bits.

0: - Timer Interrupt
    This indicates that one or both of the 2 internal WaveFront timers has expired.
1: - Oscillator Interrupt
    When this interrupt occurs the WaveFront Operating Systems reads the Oscillator Interrupt Address register to determine the oscillator that needs servicing.
2: - DMA Interrupt
    The DMA channel has completed a transfer.
3: - Emulation Interrupt
    When this occurs it indicates that a read or write has occurred with one of the High Level Emulation Control or Data registers
4: - Reserved
5: - Reserved
6: - Busy
    Status bit which indicates that the previous write operation to an internal register has not yet completed and thus a new write should not be initiated.
7: - Interrupt
    This is the Operating System interrupt from the **ICS2115**.

Indirect Register Access

There are two types of indirect registers in the chips; Synthesizer and General Purpose. Due to the timing restrictions on access to the internal indirect registers, access to the two types of registers are handled differently. In **ICS2115**, register addresses $00 through $3F are Synthesizer registers (for both read and write), and all others are for General Purpose use.

General Purpose registers are immediately available for access. Synthesizer registers are internally buffered so that the chip hardware completes the data transfers at the required times.

The WaveFront Operating System can read and write internal Synthesizer registers using 8 or 16 bit reads and writes. Access is accomplished via the 3 indirect registers:

Indirect Address (Synthesizer Base + 1)

This will contain the address of the internal Synthesizer register.

Indirect Data Lo (Synthesizer Base + 2)

Contains the Least significant 8 bits of the data to be written to or read from the internal Synthesizer register addressed by the Indirect Address register.

Indirect Data Hi (Synthesizer Base + 3)

Contains the Most significant 8 bits of the data to be written to or read from the internal Synthesizer register addressed by the Indirect Address register.

Register Map

The following list includes all the internal registers of the **ICS2115** chip and their associated "indirect" addresses. All registers can be read and written unless otherwise indicated.

Synthesizer Register Definitions

Indirect Address	Rd/Wr	Size	Mnemonic	Description
00	R/W	8	OscConf	Oscillator Configuration
01	R/W	16	OscFC	Wavesample Frequency (6 Integer, 9 Fraction)
02	R/W	16	OscStrtH	Wavesample Loop Start Address (16 Integer)
03	R/W	8	OscStrtL	Wavesample Loop Start Address (4 Integer, 4 Fraction)
04	R/W	16	OscEndH	Wavesample Loop End Address (16 Integer)
05	R/W	8	OscEndL	Wavesample Loop End Address (4 Integer, 4 Fraction)
06	R/W	8	VIncr	Volume Increment
07	R/W	8	VStart	Volume Start Value
08	R/W	8	VEnd	Volume End Value
09	R/W	16	VolAcc	Volume Accumulator
0A	R/W	16	OscAccH	Wavesample Address (16 Integer)
0B	R/W	16	OscAccL	Wavesample Address (4 Integer, 9 Fraction)
0C	R/W	8	OscPan	Pan Value (Note - 10 Bits on 2210)
0D	R/W	8	VCtl	Volume Envelope Control
0E	R/W	8	ActiveOsc	Active Voices
0F	Rd	8	IRQV	Interrupt Source/Oscillator
10	R/W	8	OscCtl	Oscillator Control
11	R/W	8	OscSAddr	Static Address Bits 27-20
12	R/W	8	VMode	Reserved (Write 0)
13-3F	-	X	RESERVED	Do Not Access

General Purpose Register Definitions				
Indirect Address	Rd/Wr	Size	Mnemonic	Description
40	Wr	8	Timer1	Timer Preset 1
41	Wr	8	Timer2	Timer Preset 2
42	Wr	8	Timer1PreS	Prescaler 1
43	R/W	8	Timer2PreS_S	Prescaler 2 (wr) and Timer Status (Rd)
44	Wr	8	DMAddrLo	DMA Start Address Low [11:4]
45	Wr	8	DMAddrMd	DMA Start Address Medium [19:12]
46	Wr	8	DMAddrHi/Data	DMA Start Address high [21:20]
47	R/W	8	DMACS	DMA Control/Status
48	Rd	8	AccMonS	Accumulator Monitor Status
49	Rd	16	AccMonData	Accumulator Monitor Data
4A	R/W	8	DOCIntCS	DOC Interrupt (Read) Int Enable (Write)
4B	Rd	8	IntOscAddr	Address of interrupting Oscillator
4C	R/W	8	MemCfg_Rev	Memory Config. (WR) & Chip Rev. # (Rd)
4D	R/W	8	SysCtrl	System Control
4E	-	X	RESERVED	Do Not Access
4F	R/W	8	OscNumber	Oscillator Address being programmed
50	R/W	8	IndMIDIData	MIDI Data Register
51	R/W	8	IndMIDICS	MIDI Control/Status Register
52	R/W	8	IndHostData	Host Data Register
53	R/W	8	IndHostCS	Host Control/Status Register
54	R/W	8	IndMIDIIntC	MIDI Emulation interrupt Control
55	R/W	8	IndHostIntC	Host Emulation Interrupt Control
56	R/W	8	IndIntStatus	Host/MIDI Emulation Int. Status (Rd)
57	R/W	8	IndEmulMode	Emulation Mode
58-7F	-	X	RESERVED	Do Not Access

Ordering Information

ICS2115V or ICS2115Y

Example:

ICS XXXX M

Package Type
V=PLCC
Y=TQFP
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Application Note for WaveFront Lite™ A Host Assisted Wavetable Synthesizer

General Description

Applications for wavetable synthesizers come in many shapes and sizes. For low cost systems that reside on a ISA card or daughter card, the designer can remove significant expense by controlling the wavetable synthesizer using the host CPU. This configuration is easily implemented with the WaveFront Synthesizer, ICS2115. The purpose of this application note is to provide full descriptions of the **WaveFront Lite** design. This configuration uses an ICS2115 with either the ICS2122 (2 MB patch set) or the ICS2125 (512 KB patch set).

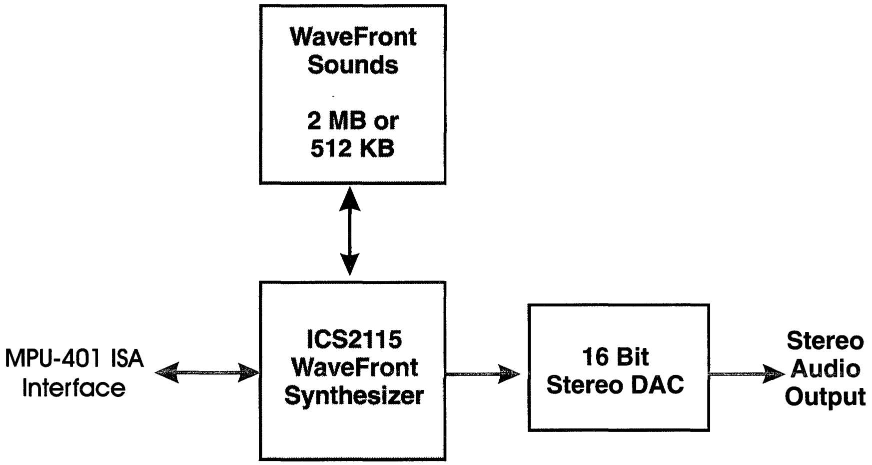
Features

- Supplied with both Windows 3.1 and DOS drivers
- MPU-401 compatible
- MT-32 compatible
- Complete General MIDI sound set
- Reduces part count and expense of conventional designs

Applications

- ISA-based sound cards
- Wavetable daughter card upgrades
- Motherboard wavetable systems

Block Diagram



WaveFront Lite is a trademark of Integrated Circuit Systems, Inc

Suggested Circuit Design

The following sections detail the specific implementations of the **WaveFront Lite** design.

ISA Interface-Inputs and Data bus

Please reference Figure 1.

Generating Chip Selects and Enable Data Bus Buffers

Signals CS*, CSMM* and GATE* can easily be generated by a 16V8 PAL device. Inputs PA1 and PA0 allows the user to select four different port addresses using two jumpers. CS* designates the location of the synthesizer registers. CSMM* selects the location for the MPU-401 registers. Together, the ICS2115 requires eight address locations. Adding AEN to the decode prevents the system from reacting to DMA operations. The equations for the PAL device follow:

```
/* Intermediate variable for address 210H */
ADDR0=SA9 & !SA8 & !SA7 & !SA6 & !SA5 & SA4 & !SA3 & !PA1 & !PA0;

/* Intermediate variable for address 230H */
ADDR1=SA9 !SA8 & !SA7 & !SA6 & SA5 & SA4 & !SA3 & !PA1 & PA0;

/* Intermediate variable for address 260H */
ADDR2=SA9 & !SA8 & !SA7 & SA6 & SA5 & !SA4 & !SA3 & PA1 & !PA0;

/* Intermediate variable for address 330H */
ADDR3=SA9 & SA8 & !SA7 & !SA6 & SA5 & SA4 & !SA3 & PA1 & PA0;

/** Logic Equations **/

CSn=!((ADDR0 # ADDR1 # ADDR2 # ADDR3) & !AEN & SA2);

CSMMn=!((ADDR0 # ADDR1 # ADDR2 # ADDR3) & !AEN & !SA2);

GATEn=!((ADDR0 # ADDR1 # ADDR2 # ADDR3) & !AEN);
```

*SBHE**

For eight bit operation, tie SBHE* pin high on the ICS2115.

SD<7,0>

Since the ICS2115 is only capable of driving a maximum of 4mA on each data pin, a bus buffer is required. A 74LS245 is a suitable candidate.

*RESET**

The ICS2115 RESET* input is active low compared with the ISA signal that is active high.

*RAMREQ**

This input pin is used to request an external memory cycle. Its function is unused in the present design. RAMREQ* should be tied high.

DACK & TC*

These pins are used to transfer sample data to and from the wavetable DRAM. For designs that do not support this capabilitiy, DACK* should be tied high and TC should be tied low. For designs that use wavetable RAM, contact ICS for more information.

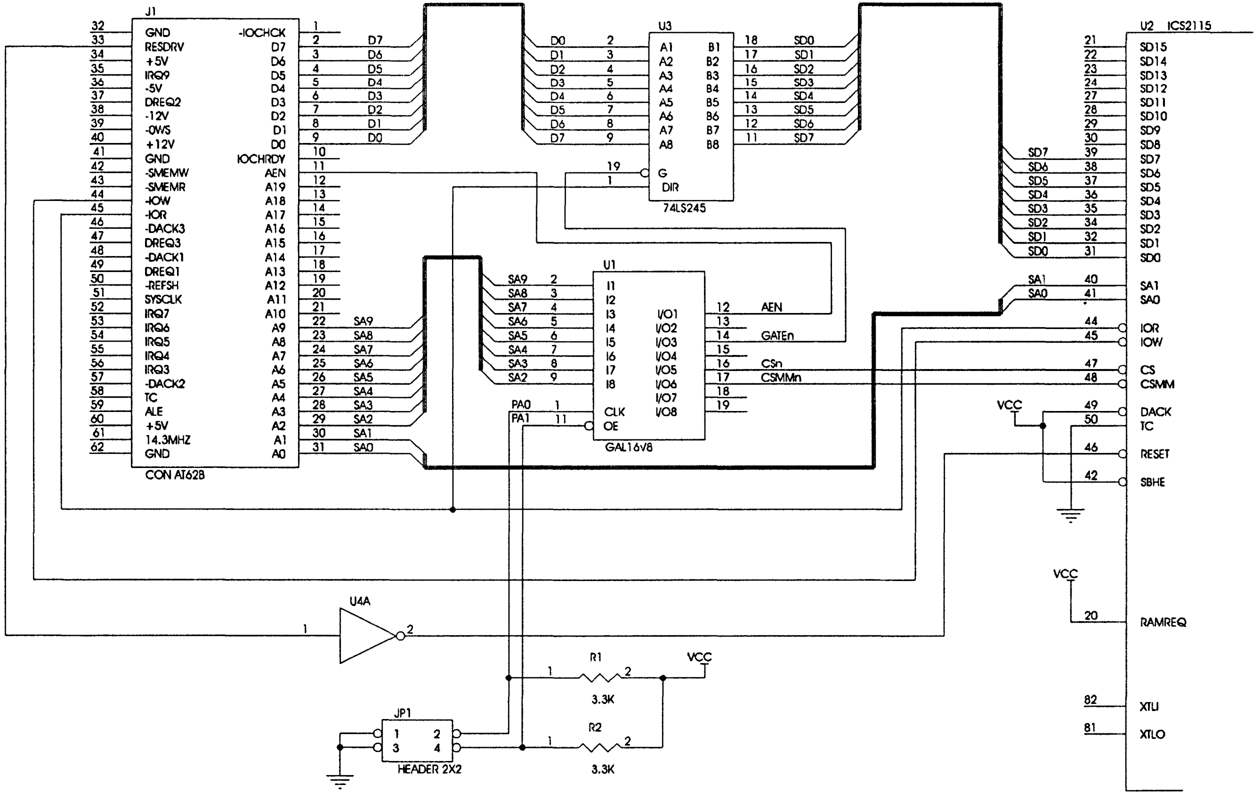


Figure 1: ISA Interface-Inputs and Data Bus

Designing WaveFront Lite into a circuit that already has a MPU-401 port

WaveFront Lite can coexist with other devices that contain a hardware MPU-401 port. The theory behind it is quite simple. In this explanation, "second MPU-401" port will refer to any device that contains a MPU-401 port that sends or receives serial MIDI. (For example, the ICS2003 performs this function.) By mapping both MPU-401 ports to the same location, the two devices act as one. The second MPU-401 will respond to both read and write operations. But, the MPU-401 portion of WaveFront Lite will serve as a write only device. It is important that the synthesizer registers, selected with CS*, are still readable and writable. Another consideration is that now both MPU-401 ports must reside at the same location for proper DOS operation. If the user changes the address of the MPU-401 port on one device, they must also change the other device. Otherwise, the application software will not recognize the **WaveFront Lite** hardware. These considerations only apply to DOS. In Windows, **WaveFront Lite** does not use the MPU-401 port. Instead, it addresses the synthesizer registers directly.

The circuitry in Figure 2 shows how to implement "WaveFront Lite Write Only for MPU-401" in hardware. Notice the addition of U5A and R3. These components allow the host to only read the ICS2115 synthesizer registers. ICS has reference designs available that show MPU-401 sharing between the ICS2003 and ICS2115. For further information, please contact the factory.

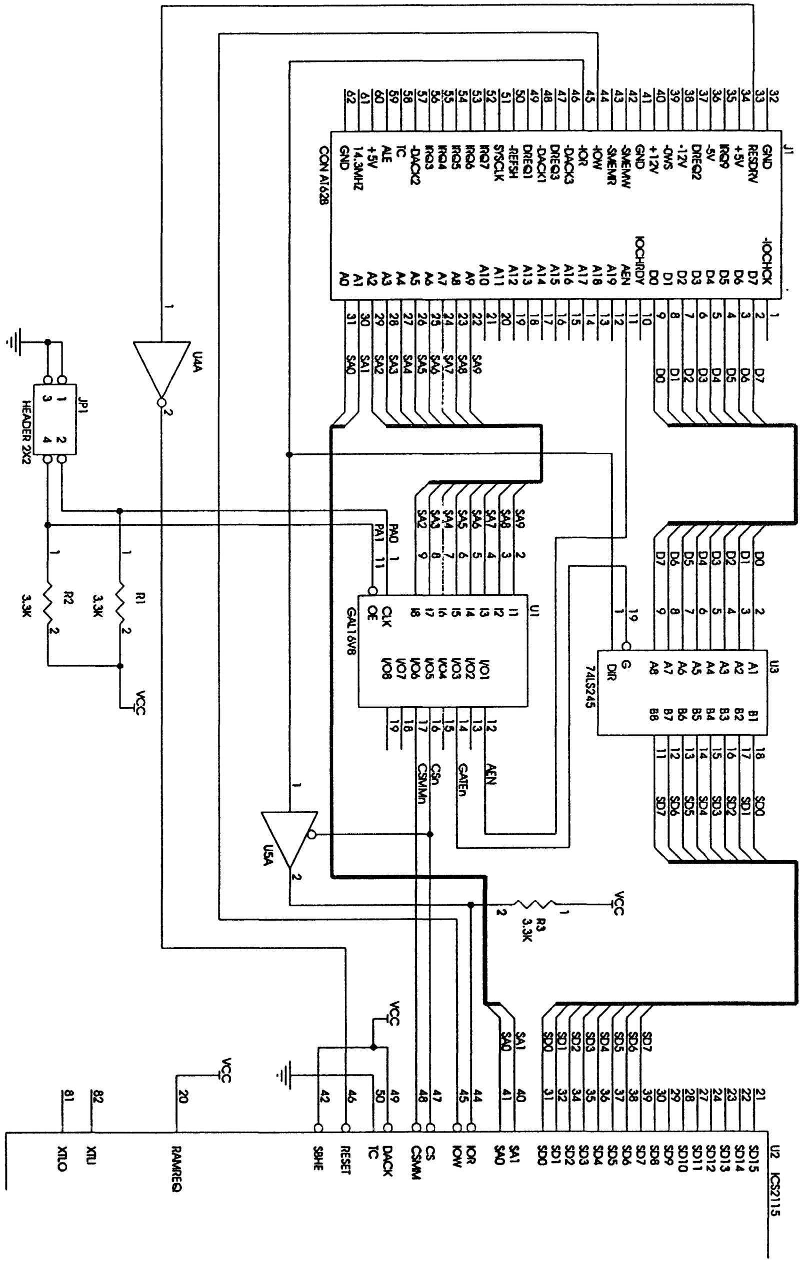


Figure 2: ISA Interface-Inputs and Data Bus using MPU-401 Sharing

ISA Interface-Outputs

Please reference Figure 3.

IOCHRDY

This is an open collector output that requires a non-inverting buffering to drive the ISA bus. A pull-up of approximately 2.2k is recommended on the IOCHRDY pin of the ICS2115.

IRQ

This is the main interrupt for the DOS TSR. This ICS2115 output has an open emitter with a weak internal pull-down. Externally, it requires a 1k pull-down resistor. An open-collector inverter should be used to connect this pin to the ISA bus NMI line. (A tristate gate can achieve the same results.)

A 1k pull-down resistor is suitable for two reasons: First, the low-level DC voltage should be significantly less than the TTL low threshold of 800mV. Since most LS type inputs have an I_L of 400uA, a 1k pull-down on the input achieves a low level voltage of 400mV (worst case). Second, the maximum drive current of the ICS2115, 4mA, should produce a high-level DC voltage that significantly exceeds the TTL high threshold of 2V. Using Ohm's Law, one can show that a 4mA current through a 1k resistor produces a voltage of 4V.

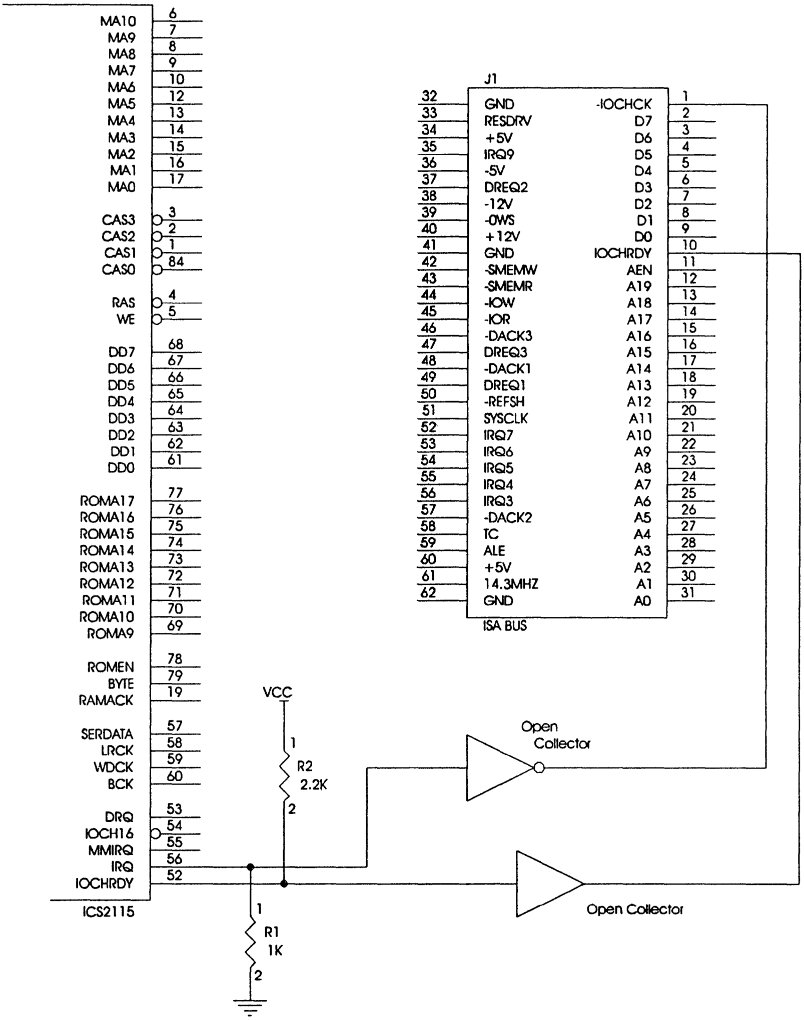


Figure 3: ISA Interface-Outputs

Clock Input

The ICS2115 requires an input clock frequency of 33.8688 MHz. Figure 4 shows how to connect a third harmonic crystal to the ICS2115. For fundamental mode crystals, remove the capacitor and inductor.

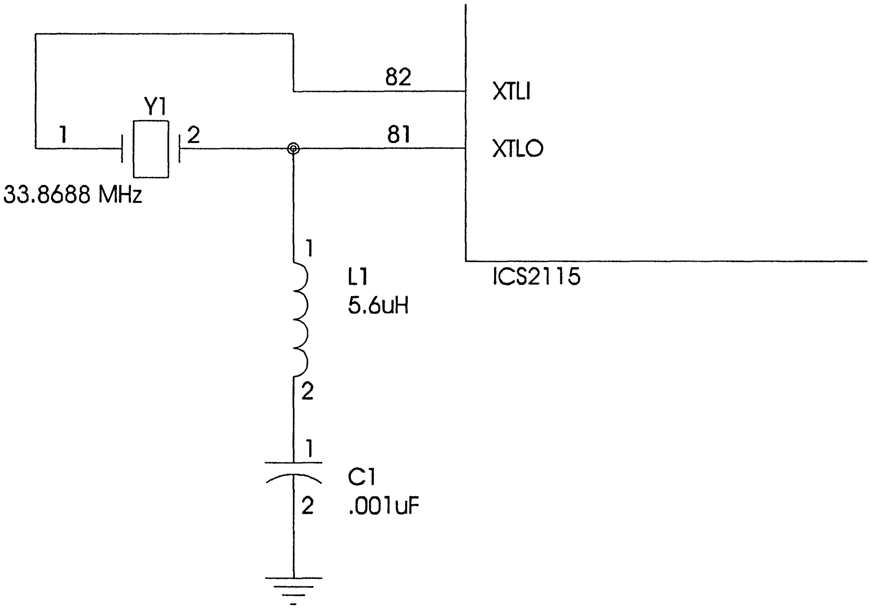


Figure 4

Wavetable ROM Interface

WaveFront Lite uses a General MIDI ROM sound set. The designer can choose either the 2 MB set or the 512 KB set based on sound quality and cost. Please reference the appropriate section below.

2 MB Sound Set

To accommodate the ROM memory space, the ICS2115 uses the RA<17,10>, MA<10,0>, and CAS3 outputs to form the ROM address bus. On the wavetable ROM, ICS2122, the OE* pin connects directly to the ROMEN* on the ICS2115, and the CE* should be tied low. With the BYTE* pin tied low, the ROM is in 2 MB x 8 mode. Therefore, the D<7,0> pins on the ICS2115, and the D<15,0> pins are unused. Figure 5 shows this graphically.

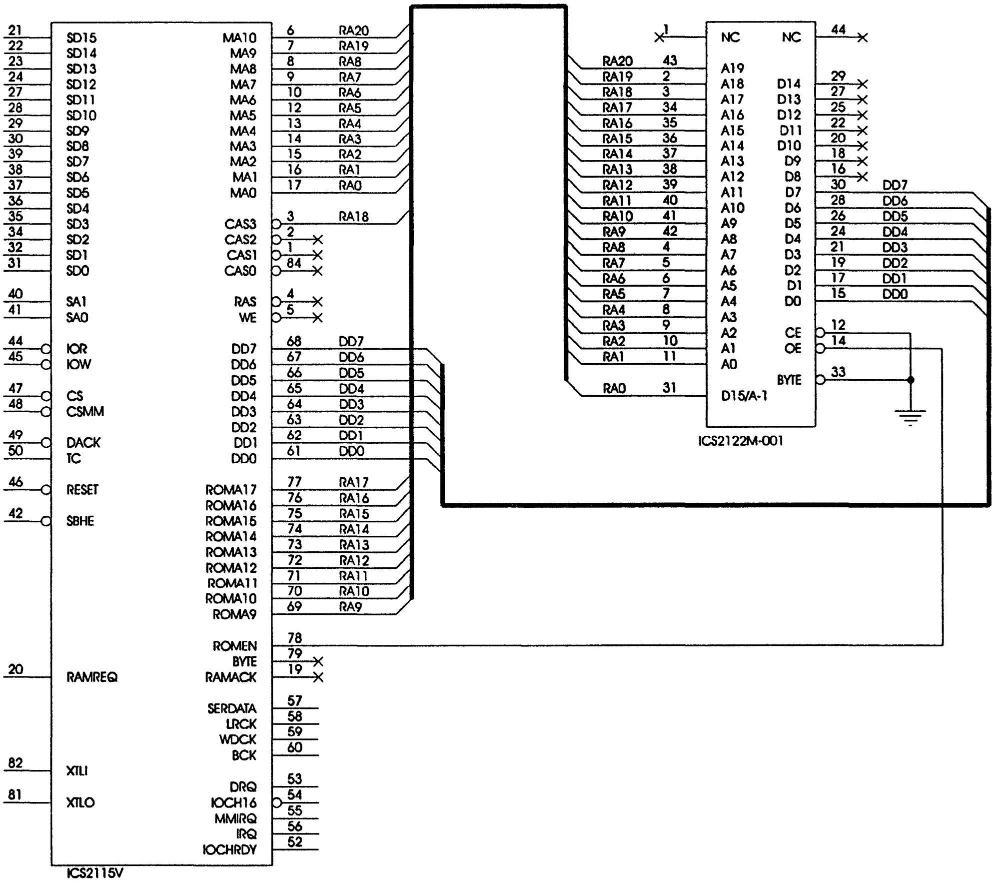


Figure 5: 2 MB Wavetable Memory Interface

512 KB Sound Set

To accommodate the ROM memory space, the ICS2115 uses its RA<17,10>, MA<8,0>, and CAS3 outputs to form the ROM address bus. On the wavetable ROM, ICS2125, the OE* pin connects directly to the ROMEN* on the ICS2115, and the CE* should be tied low. Figure 6 shows this graphically.

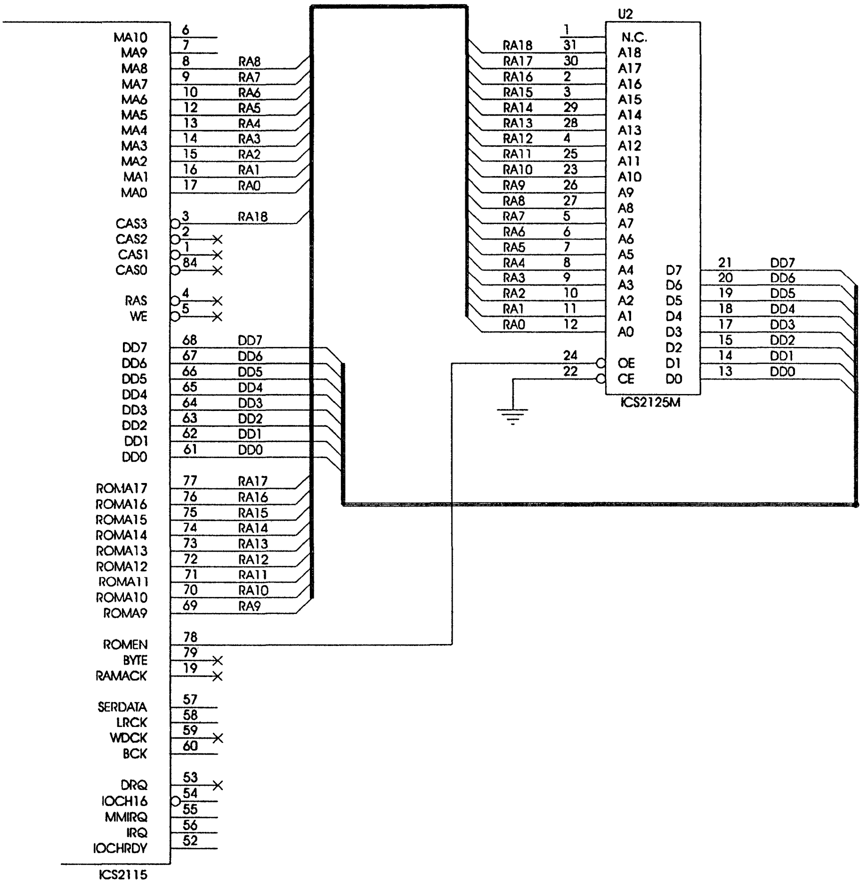


Figure 6: 512 KB Wavetable Memory Interface

DAC Outputs

Figure 7 shows how to connect an inexpensive DAC from NEC to operate with the ICS2115.

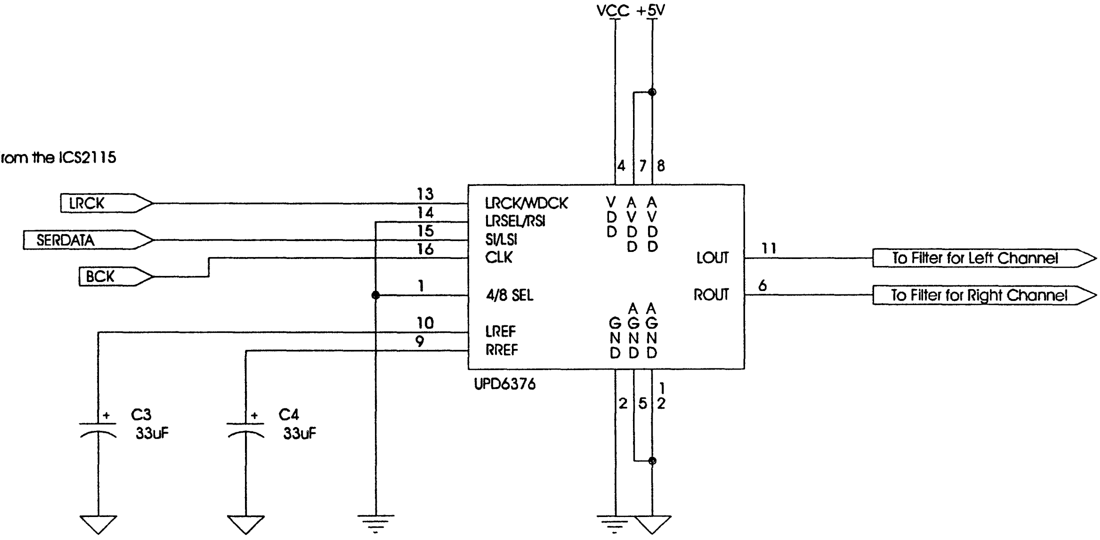


Figure 7: DAC Configuration

Analog Filtering

The circuit in Figure 8 is a 2-pole Chebyshev filter with a 3-dB cut-off of approximately 15 kHz. The cut-off value represents half the output sampling rate of 33.8 kHz. The Chebyshev configuration provides a slight treble boost of about 2 dB for brightness in the sound. The 75 Ohm resistor in series with the output serves as disaster protection. Dead shorts of the output will not damage the amplifier.

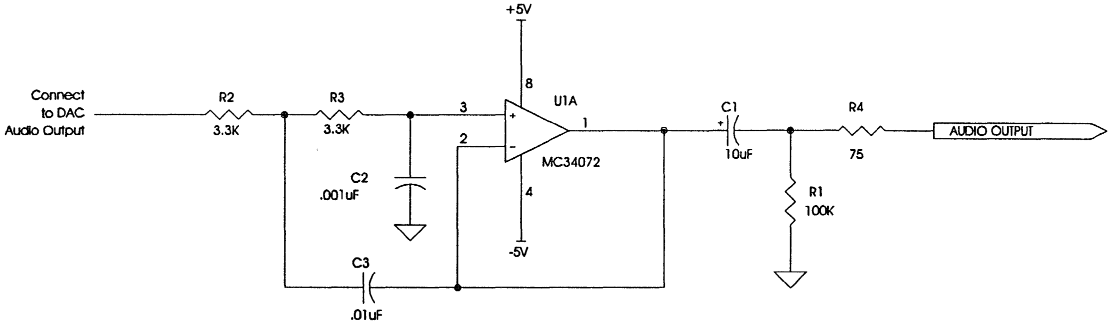


Figure 8: Analog Anti-Aliasing Filter for the DAC Outputs

Integrated
Circuit
Systems, Inc.

ICS2116

WaveFront™ Interface

General Description

The **ICS2116** is the interface component of the WaveFront wavetable synthesis chip set. The interface chip monitors and controls the activities of the 68EC000 processor and 256K x 4 DRAM including address decoding and data buffering to and from the input source. The input can be serial, parallel, MIDI or the ISA bus emulating the MPU-401 or 6850 UART.

For systems not using the ISA bus, the WaveFront Interface can convert the serial output of the synthesizer into a form that the optional Motorola 56001 DSP can read. This option provides global digital effects like chorus and reverb to enhance the audio signal.

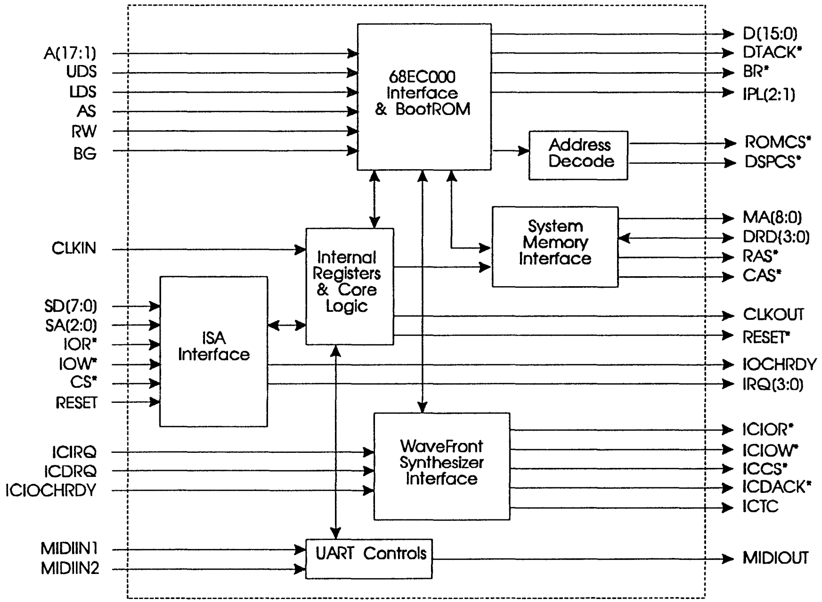
Features

- WaveFront interface to serial, parallel, MIDI and ISA bus
- Provides the majority of system “glue” logic, keeping parts count down and cost low
- Uses a single inexpensive 256K x 4 DRAM as system memory
- Contains small code ROM, which eliminates the code ROM in an ISA design
- Soft select of 4 different IRQs
- Part of a complete design package that includes software drivers for Windows and DOS

Applications

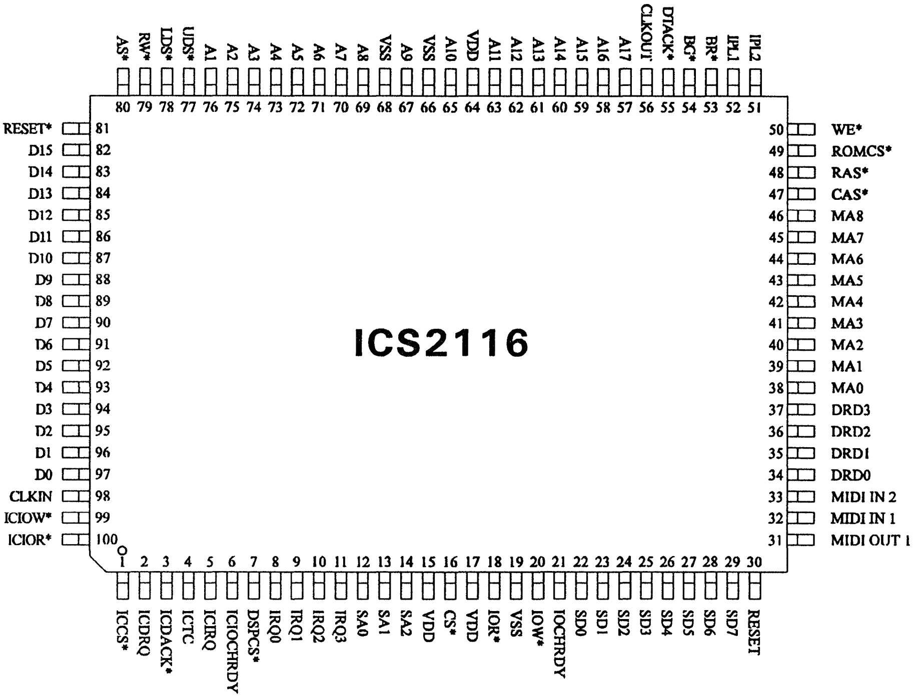
- ISA based sound cards
- Wavetable synthesizer daughter cards
- External sound modules that connect to a PC’s serial or parallel port
- Any system requiring a self contained unit that provides high quality music synthesis of General MIDI sounds, in a low cost design

Block Diagram



WaveFront is a trademark of Integrated Circuit Systems, Inc

Pin Configuration



100-Pin PQFP
K-11

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
12, 13, 14	SA<2:0>	I	Host Port Address Bits A2 through A0**
22-29	SD<7:0>	I/O	Host Bi-directional Data Bus
16	/CS	I	Host port Chip Select (Active Low)
18	/IOR	I	Host Read Enable (Active Low)**
20	/IOW	I	Host Write Enable (Active Low)
21	IOCHRDY	O	Host I/O Channel Ready (Active High)**
8, 9, 10, 11	IRQ<3:0>	O	Decoded Host IRQ selects. One is active, the others float in the high impedance state. (Active High)**
30	RESET	I	Master Reset (Active High)
57-63, 65, 67, 69-76	A<17:1>	I	68EC000 Address Bus
82-97	D<15:0>	I/O	68EC000 Bi-directional Data Bus
77	/UDS	I	68EC000 Upper Data Strobe (Active Low)
78	/LDS	I	68EC000 Lower Data Strobe (Active Low)
79	/RW	I	68EC000 Read/Write (Active Low)
80	/AS	I	68EC000 Address Strobe (Active Low)
55	/DTACK	O	68EC000 Data Acknowledge (Active Low)
51, 52	IPL<2:1>	O	68EC000 Interrupt Priority level (Active High)
53	/BR	O	68EC000 Bus Request (Active Low)
54	/BG	I	68EC000 Bus Grant (Active Low)
56	CLKOUT	O	CLKIN/2 for the 68EC000
81	/RESET	O	Conditioned RESET input for the 68EC000 and ICS2115 (Active Low)
1	/ICCS	O	ICS2115 Chip Select (Active Low)
100	/ICIOR	O	ICS2115 Read Enable (Active Low)
99	/ICIOW	O	ICS2115 Write Enable (Active Low)
5	ICIRQ	I	ICS2115 Interrupt Request (Active High)
6	ICIOCHRDY	I	ICS2115 I/O Channel Ready (Active High)
2	ICDRQ	I	ICS2115 DMA Request (Active High)
3	/ICDACK	O	ICS2115 DMA Acknowledge (Active Low)
4	ICTC	O	ICS2115 Terminal Count (Active High)
38-46	MA<8:0>	O	Operating System DRAM Muxed Address Bus
34-37	DRD<3:0>	I/O	Operating System DRAM Data Bus
47	/CAS	O	Operating System DRAM Column Address Strobe (Active Low)
48	/RAS	O	Operating System DRAM Row Address Strobe (Active Low)
49	/ROMCS	O	Operating System ROM Chip Select (Active Low)
7	DSPCS	O	Chip Select for a Digital Signal Processor (Active Low)
32	MIDI IN 1	I	Serial MIDI Input #1
33	MIDI IN 2	I	Serial MIDI Input #2
31	MIDI OUT 1	O	Serial MIDI Output
98	CLKIN	I	Clock Input
64, 15, 17	VDD	P	Power Supply
66, 68, 19	VSS	P	Ground

Absolute Maximum Ratings

Supply Voltage . . . . -0.5 to 7.0V
Logic inputs . . . . -0.5 to V_{DD}+0.5V
Ambient operating temp. . . . . 0°C to 70°C
Storage temperature . . . . -65°C to 150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

DC Electrical Characteristics

V_{CC}=5.0V ± 5%; GND=0V; T_A=0°C to 70°C

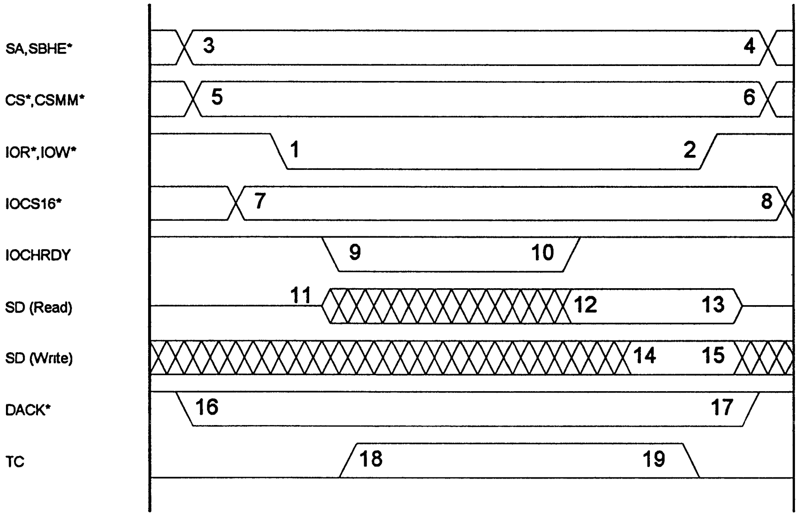
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		4.75	5.00	5.25	V
TTL Input Voltage Low	V_{IL}		-0.30		0.80	V
TTL Input Voltage High	V_{IH}		2.20		VDD+0.30	V
Schmidt Input Voltage Low	V_{ILS}		-0.30		1.50	V
Schmidt Input Voltage High	V_{IHS}		3.00		VDD+0.30	V
XTLI Input Voltage Low	V_{ILX}		-0.30		1.50	V
XTLI Input Voltage High	V_{IHX}		3.50		VDD+0.30	V
Output Low Current= Standard Drive	I_{OL}	V_{OL}=0.4V	4.0	6.0		mA
Output High Current Standard Drive	I_{OH}	V_{OH}=2.8V		-6.0	-4.0	mA
Output Low Current Medium Drive	I_{OL2}	V_{OH}=0.4V	6.0	9.0		mA
Output High Current Medium Drive	I_{OH2}	V_{OH}=2.8V		-9.0	-6.0	mA
Output Low Current High Drive	I_{OL3}	V_{OH}=0.4V	9.0	12.0		mA
Output High Current High Drive	I_{OH3}	V_{OH}=2.8V		-12.0	-9.0	mA
Input Leakage Current Standard Inputs	I_{IN}	VIN=V_{SS}	-1.0		1.0	uA
Pull-up Current	I_{PUP}	VIN=V_{DD}	15.0	30.0	50.0	uA
Pull-down Current	I_{PDN}		50.0	90.0	150.0	uA

Note: All pins have a maximum capacitive load of 50pf unless noted otherwise.

AC Electrical Characteristics

Please reference the timing diagram titled *Host Interface Timing*, below.

HOST INTERFACE AC TIMING PARAMETERS						
PARAMETER	SYMBOL	FROM	TO	MIN	MAX	UNITS
Address setup to command	t_{AS}	3	1	10	-	nS
Chip select setup to command	t_{CS}	5	1	10	-	nS
Address hold from command	t_{AH}	2	4	10	-	nS
Chip select hold from command	t_{CH}	2	6	10	-	nS
Command width	t_{CW}	1	2	100	-	ns
Write data setup	t_{DS}	14	2	50	-	nS
Write data hold	t_{DHW}	2	15	10	-	nS
Read data delay (ready access)	t_{DD}	1	12	0	60	nS
Read data hold	t_{DHR}	2	13	0	20	nS
DACK* setup to command	t_{DAS}	16	1	20	-	nS
DACK* hold after command	t_{DAH}	2	17	50	-	nS
TC setup to command	t_{TS}	18	2	25	-	nS
TC hold after command	t_{TH}	2	19	n/a	-	nS
TC width	t_{TW}	18	19	20	-	nS



Host Interface Timing

Miscellaneous Pins

VDD, VDDP

These are the chip power supply pins. VDD pins power the core logic, while VDDP pins power the pad ring. This arrangement helps prevent switching spikes due to output transitions from disturbing the internal operation of the chip by confining large switching currents to bond wires for pad supplies. These pins MUST be at the same potential externally.

VSS, VSSP

These are the chip ground pins. VSS pins ground the core logic, while VSSP pins ground the pad ring. This arrangement helps prevent switching spikes due to output transitions from disturbing the internal operation of the chip by confining large switching currents to bond wires for pad supplies. These pins MUST be at the same potential externally.

CLKIN

This input requires a 20 MHz clock source. Internally, the **ICS2116** divides this signal by two and sends it to the 68EC000 through the CLKOUT output.

ISA Host Interface

Note: This section applies to PC Mode and not Stand-Alone Mode. If /IOR is low when the /RESET input goes low, the chip enters Stand-Alone Mode, otherwise it remains in PC Mode. Stand-Alone Mode is covered in the following section. Pin descriptions for PC mode follow:

/CS

This input pin selects read/write access to emulation registers for the MIDI interface, the Media Master Interface, and the DMA transfer registers. This signal must be stable before, during, and after /IOR or /IOW strobes.

SA<2:0>

These address input pins select one of eight direct mapped registers as determined by the /CS pin. These signals must be stable before, during, and after /IOR or /IOW strobes.

SD<7:0>

This is the bi-directional data bus used for all register data transfers.

/IOR

This input pin is used to read registers when low. SA<2:0> and /CS must be stable before, during, and after the active low pulse on /IOR. If this signal is low when the /RESET input goes low, the **ICS2116** enters stand-alone mode. See the Stand-Alone Mode section for more information.

/IOW

This input pin is used to write registers when low. SA<2:0> and /CS must be stable before, during, and after the active low pulse on /IOW. SD<7:0> must be stable before, during, and after the trailing (rising) edge of /IOW.

IOCHRDY

This output pin is normally in a resistive pull-up state. During /IOR or /IOW low times, this pin can be driven low to indicate to the host that the requested data transfer is not ready, and that /IOR or /IOW should be held low until IOCHRDY goes high.

IRQ<3:0>

These outputs allow the host to choose which of four IRQs the **ICS2116** should use. Immediately following power-up, these pins are all in the high-impedance state. Software on the host side will then write to the Board Hardware Initialization Register to select one of the four IRQs. The selected IRQ will then operate as a standard TTL output, while the other IRQs remain in the high impedance-state.

RESET

This input is the active high input for the synthesizer system. When the input goes high, the /RESET output is latched low (reset state).

68EC000 Interface

The 68EC000 microprocessor communicates with the PC through the Media Master registers, located in the **ICS2116**. The **ICS2116** buffers the registers so that both the PC and the 68EC000 can access them at the same time.

To transfer blocks of data, the **ICS2116** performs a DMA-type operation. The host platform writes the desired byte or word to the Sample Transfer port, which the **ICS2116** transfers to the ICS2115 as a DMA cycle. During this operation, the **ICS2116** takes control of the data bus by requesting and receiving data from the 68EC000 (using signals /BR and /BG).

The **ICS2116** decodes the 68EC000's address lines to connect it to all of the other devices, both internal and external. Since the compact memory map is only 128K x 16, the **ICS2116** does not decode address bits 18 through 23. As a result, the map images 64 times in the 16 MB address space. The **ICS2116** does not decode A0 because address bit 0 is invalid for the 68EC000 processor in 16-bit mode.

The fixed Hardware vector, mapped in the lowest 8 bytes, points to the BootROM. This allows the 68EC000 to initialize itself with the BootROM in the **ICS2116**. Afterwards, it must load the Synthesizer operating system into OSRAM from one of three sources: the O.S. Code ROM, wavetable ROM, or from the PC via the Media Master Port.

The address space of the **ICS2116** is as follows (listed as byte addresses):

Address Definitions

Address	Size	Content
3FFFF 3FC30	488 Words	488 x 16-bit BootROM (Internal)
3FC2F 3FC20	8 Words	DSP Subsystem (Asserts /DSPCS with special timing
3FC1F 3FC18	4 Words	External I/O - /DSPCS with address timing
3FC17 3FC10	4 Words	6850 MIDI UART Configuration, Baud Rate Generator and Misc Status (Internal)
3FC0F 3FC08	4 Words	MPU-401/6850 & Media Master Interface Registers (Internal)
3FC07 3FC00	4 Words	ICS2115 Indirect Registers (Drives /ICCS, /ICIOR, & /ICIOW)
3FBFF 20000	63K Words	Optional O.S. Code ROM (Asserts /ROMCS)**
1FFFF 00008	64K Words minus 4 Words	64K x 16-bit OSRAM (Externally a 256K x 4 DRAM)
00007 00000	4 Words	Fixed H/W Vector to BootROM Address 0003FC30 (Internal)

**When disable BootROM is set, the upper 488 words of the optional external 64K OSROM replace the on chip ROM.

A<17:1>

This is the local address bus for the wavetable synthesis system.

D<15:0>

This is the local data bus for the wavetable synthesis system.

/UDS

This input connects directly to the 68EC000's Upper Data Strobe.

/LDS

This input connects directly to the 68EC000's Lower Data Strobe.

/RW

This input connects directly to the 68EC000's Read/Write Strobe.

/AS

This input connects directly to the 68EC000's Address Strobe.

/DTACK

This output connects directly to the 68EC000's Data Acknowledge.

IPL<2:1>

These outputs connect directly to the 68EC000's Interrupt Priority Levels 2 and 1.

/BG

This output connects directly to the 68EC000's Bus Grant.

/BR

This output connects directly to the 68EC000's Bus Receive.

CLKOUT

This output provides a 10 MHz clock source for the 68EC000.

/RESET

/RESET is a conditioned version of the reset input from the host. When the RESET input goes high, the /RESET output is latched low (reset state). The host software changes the /RESET output to the non-reset state, by writing the appropriate data to the Hardware Initialization Register.

ICS2115 Interface

Based on the address decoding and the 68EC000 signals /UDS and /LDS, the **ICS2116** drives the /IOR and /IOW inputs on the ICS2115. The 68EC000 signals A1 and A2 tie directly to the ICS2115 SA0 and SA1 inputs respectively. The host interface can pass sample data to the ICS2115 through a DMA-type operation.

/ICCS

This output is the active low chip select for the ICS2115.

/ICIOR

This output is the active low read strobe for the ICS2115.

/ICIOW

This output is the active low write strobe for the ICS2115.

ICIRQ

This input accepts the hardware interrupt requests from the ICS2115.

ICIOCHRDY

This input receives the I/O Channel Ready input from the ICS2115.

ICDRQ

This input receives DMA Requests from the ICS2115.

/ICDACK & TC

These outputs operate during a DMA transfer to and from the ICS2115. /ICDACK indicates that the /ICIOR or /ICIOW is a DMA transfer. TC connects with the Terminal Count input on the ICS2115.

System DRAM Interface

The **ICS2116** interfaces with a 256K x 4 DRAM in such a way that it appears as 64K x 16 RAM to the microprocessor. The BootROM contains the code to load the synth operating system into this DRAM.

MA<8:0>

MA<8:0> are the multiplexed address lines.

DRD<3:0>

This is the four bit data bus.

/CAS

Column address Strobe for the System DRAM.

/RAS

Row address Strobe for the System DRAM.

Serial MIDI Interface

MIDI IN 1 & MIDI IN 2

These two serial MIDI inputs are switched internally, to use only one UART. The initialization register determines which MIDI input controls the synthesizer.

MIDI OUT 1

MIDI OUT 1 is a serial MIDI output.

ROM and DSP Interface

/ROMCS
This output enables the Operating System ROM. Upon initialization, the code in the BootROM transfers the operating system from the ROM to the system RAM. Afterwards, it begins execution from RAM and never accesses the Operating System ROM.

/DSPCS
This output is an address decode for a Motorola DSP.

Stand-Alone Mode

When the **ICS2116** enters Stand-Alone Mode, some of the ISA interface pins assume different functions. This is illustrated below. The chip detects this mode by checking the IOR signal when reset goes low. If IOR is low at that instant, the **ICS2116** enters "Stand-Alone Mode" and remains that way until reset or power-down occurs.

/IOR
/IOR should be tied low to signify stand-alone mode.

/BG
This input selects which baud rate the operating system will receive data on the MIDI IN 1 input. The high state indicates the standard MIDI baud rate, 31.25K. A low level indicates a rate suitable for the serial port on the PC, 38400 baud.

MIDI IN 1
This is the only usable serial input in stand-alone mode.

MIDI IN 2
MIDI IN 2 is not available in stand-alone mode.

Parallel Port Interface

/IOW
This serves as a /STROBE input for the parallel port. The **ICS2116** latches the data on SD<7:0> when the rising edge occurs.

IRQ<0>
This output serves as a Transmit Data Ready indicator for the parallel port BUSY input.

SD<7:0>
This serves a unidirectional data bus for parallel input.

/CS
This input still serves as a chip select for the parallel port. To enable the parallel interface, tie this pin low. Otherwise, tie it high.

Serial DSP Interface

SA<0>
This input receives the bit clock from the ICS2115.

SA<1>
This input receives the left/right clock from the ICS2115.

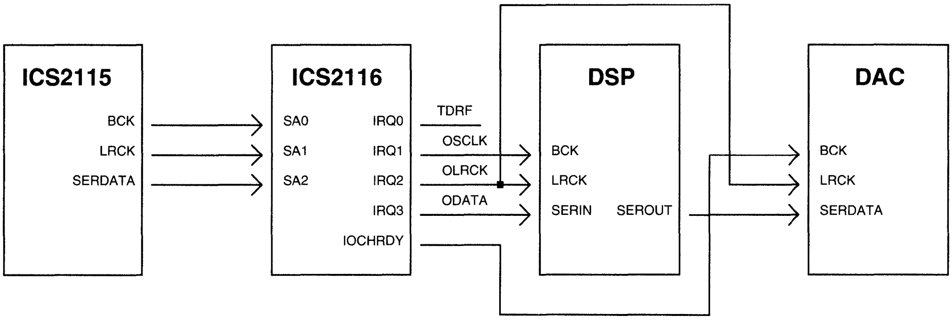
SA<2>
This input receives the serial audio data from the ICS2115.

IOCHRDY
This output is the bit clock for the serial DAC when the optional DSP is used.

IRQ<1>
This output is the bit clock for the DSP.

IRQ<2>
This output is the left/right clock for the DSP.

IRQ<3>
This output is the serial audio data for the DSP.



Host Interface Register Descriptions

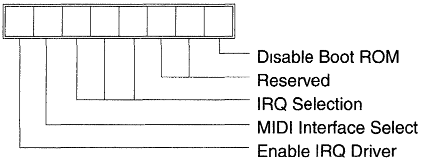
ICS provides a program named SETUPSND.EXE that initializes the **ICS2116** and downloads the Operating System to the system RAM. Using command line parameters, the user can specify the options that are contained in the Hardware Initialization Register.

The /CS input enables the Host Interface for I/O transfers. Using three address lines, the **ICS2116** has the following registers:

Base Address Offset	Function
7	Sample Data Transfer with Terminal Count (High Byte)
6	Sample Data Transfer with Terminal Count (Low Byte)
5	Sample Data Transfer (High Byte)
4	Sample Data Transfer (Low Byte)
3	Media Master Control
2	Media Master Data
1	MPU-401/6850 Port
0	MPU-401/6850 Port (Hardware Initialization Register, see below)

Hardware Initialization Register

Following power-on or a hard reboot of the host PC, the **ICS2116** resets its /RESET output which will hold the 68000 and ICS2115 in the reset state. An initialization program, running in the PC, writes to the Initialization Register. This sets the /RESET output and removes the Hardware Initialization Register from the register set. Then, the Base+0 register becomes the MPU-401/6850 Port. The format of this register is as follows:



Board H/W Initialization Register: (Base+0)

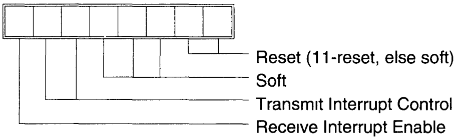
Bit 7 - Enable IRQ Driver
  0 - Tristate the **ICS2116** IRQ outputs 3-0.
  1 - Enable IRQ selected by bits 5:3 to be driven onto the PC Bus.
Bit 6 - MIDI Interface Select
  0 - Use the MIDI Input 1
  1 - Use the MIDI Input 2
Bits 5:3 - IRQ Selection
  0 0 0 - IRQ0
  0 0 1 - IRQ1
  0 1 0 - IRQ2
  0 1 1 - IRQ3
  1 X X - All IRQs Disabled
Bits 2:1 - Reserved
Bit 0 - Disable Boot ROM. When set to 1, the **ICS2116** selects the external ROM instead of the internal Boot ROM mapped at 03FC30-03FFFFH.

MIDI Emulation Control/Status Register

The MIDI Control Status register can be configured as either a 6850 compatible or an MPU-401 compatible sets. The MIDI Emulation Mode bit in the Media Master Emulation Mode Register will indicate which emulation mode is used. Using SETUPSND.EXE, the user can change the emulation mode.

6850 Mode Control (Base + 0) (Write Only)

The PC host application program can access this MIDI control register by writing to this address. The control register is mapped as follows.



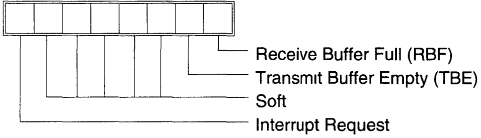
MIDI (6850) Control Register

1:0 - Reset - Resets the MIDI Port
  11 = Reset (Resets Receive Buffer Full Interrupt (to the Host) and Receive Interrupt Enable)
  00, 01 and 10 = No Reset
4:2 - Soft - Software controlled functions
6:5 - Transmit Buffer Empty Interrupt Control
  01 = Interrupts are enabled
  00, 10 and 11 = Interrupts disabled
7: - Receive Buffer Full Interrupt Enable
  1 = Interrupts enabled
  0 = Interrupts disabled

6850 Mode Status (Base + 0) (Read Only)

The PC host application program can access this MIDI status register by reading this address. The status register is mapped as follows.

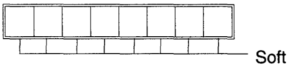
MIDI (6850) Status Register



0: - Receive Buffer Full
  1 = full
  0 = empty
1: - Transmit Buffer Empty
  1 = empty
  0 = full
6:2 - Soft
7: - Interrupt Request
  1 = Interrupt pending
  0 = Interrupt not pending

MPU-401 Mode Control (Base + 1) (Write Only)

The PC host application program can access this MIDI control register by writing to this address. The control register mapping is software dependent.



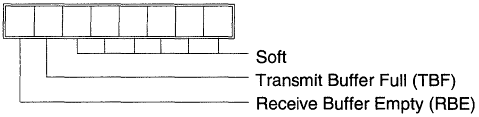
MIDI (MPU-401) Control Register

7:0 - Soft - Software controlled functions

MPU-401 Mode Status (Base + 1) (Read Only)

The PC host application program can access this MIDI status register by reading this address. The status register is mapped as follows.

MIDI (MPU-401) Status Register



5:0 - Soft
6: - Transmit Buffer Full
  1 = full
  0 = empty
7: - Receive Buffer Empty
  1 = empty
  0 = full

MIDI Emulation Data Register

This register is the MIDI data port for writing and reading MIDI data. The PC host application program can transfer MIDI data between itself and the WaveFront Operating System via this register.

6850 Mode Data (Base + 1) (Read/Write)

Eight bit data.

MPU-401 Mode Data (Base + 0) (Read/Write)

Eight bit data.

Media Master Registers

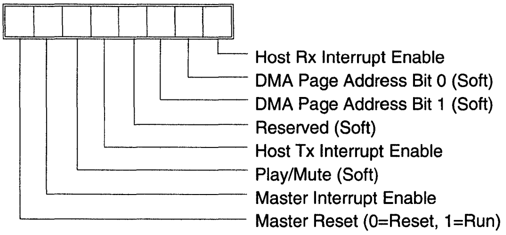
The Media Master interface provides access to the more sophisticated features of the operating system. Host programs use these registers to download wavetable data. The descriptions follow:

Host Data (Base + 2) (Read/Write)

Eight bit data register. The PC host application program can write and read this register to exchange commands and data with the WaveFront.

Host Control*/Status (Base + 3) (Write Only)*

The Host Control/Status register will have the following bit meanings when written to by the PC host application program.

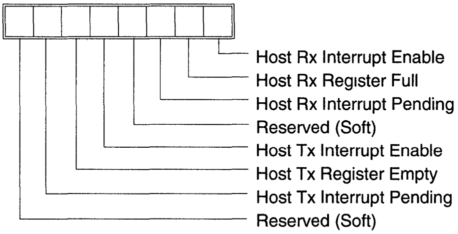


Host Control Register

0: - Host Data Receive Interrupt Enable
    1 = enable
    0 = disable
2:1 - DMA Page Address (2 bits) (Soft)
3: - Reserved (Soft)
4: - Host Data Transmit Interrupt Enable
    1 = enable
    0 = disable
5: - Play/Mute (Soft)
    1 = play
    0 = mute
6: - Host Data Master Interrupt enable
    This bit enables or disables all interrupts from the WaveFront subsystem to the PC host application program. Note that this includes the MIDI emulation mode interrupts from the MIDI Emulation Status register. It does not affect the interrupts for the WaveFront Operating System.
    1 = enable
    0 = disable
7: - Master Reset
    This bit will cause a Soft Reset to occur which resets the WaveFront chip.
    1 = run
    0 = reset (WaveFront chip soft reset)

*Host Control/*Status *(Base + 3) (Read Only)*

The Host Control/Status register will have the following bit meanings when read by the PC host.



Host Status Register

0: - Host Data Receive Interrupt Enabled
    1 = enabled
    0 = disabled
1: - Host Data Receive Register Full
    1 = full
    0 = empty
2: - Host Data Receive Interrupt Pending
    1 = Pending
    0 = Not Pending
3: - Reserved (Soft)
4: - Host Data Transmit Interrupt Enabled
    1 = enabled
    0 = disabled
5: - Host Data Transmit Register Empty
    1 = empty
    0 = full
6: - Host data Transmit Interrupt Pending
    1 = Pending
    0 = Not Pending
7: - Reserved (Soft)

Ordering Information

ICS2116Y

Example:

ICS XXXX M

- **Package Type**
  - Y=QFP
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  - ICS, AV=Standard Device; GSP=Genlock Device

WaveFront™ Sounds (16M Bit CMOS Mask ROM)

Description

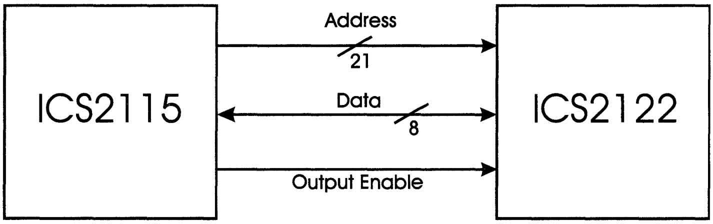
WaveFront Sounds are masked ROMs that serve as the wavetable for the ICS2115 WaveFront Synthesizer. Each sound set, 4 MB, 2 MB and 512 KB, contains the musical data needed to synthesize the instruments from the General MIDI specification. The 4 MB sound set consists of two 2 MB ROMs, the **ICS2124M-001** and **ICS2124M-002**. The 2 MB sound set consists of one 2 MB ROM, the **ICS2122M-001**. The 512 KB sound set consists of one 512 KB ROM, the **ICS2125M-001**.

Features

- Complete set of General MIDI sounds, which contains 128 instruments and 69 drum sounds.
- Available in three sizes, 4 MB, 2 MB & 512 KB, to provide the optimal balance between price and performance for many applications.
- 16-bit linear wavetable (ICS2124-001/-002), compressed wavetable (ICS2122-001), or full-featured wavetable (ICS2125-001).
- Uses 2M x 8 MROMs in 44-pin SOP packages.

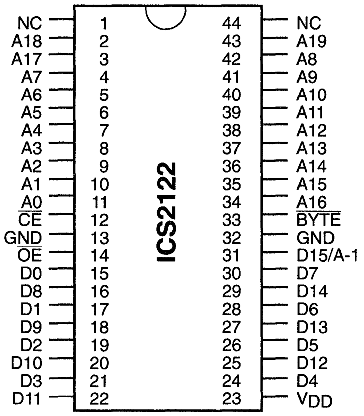
Block Diagram

2 MB Patch Set



WaveFront is a trademark of Integrated Circuit Systems, Inc

Pin Configuration



44-Pin SOP
K-8

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2-11, 34-43	A0-A19	I	Address Inputs
15-22, 24-30	D0-D14	O	Data Outputs
12	$\overline{CE}$	I	Chip Enable Input
14	$\overline{OE}$	I	Output Enable Input
31	D15/A-1	I/O	Data Output/Address Input
33	$\overline{BYTE}$	I	Word, Byte selection Input tied low for byte operation
23	V_{DD}	P	Power Supply
13, 32	GND	P	Ground
1, 44	NC	-	No Connection

Absolute Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-0.5~V_{DD}	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	1.0/0.6	W
T_{STG}	Storage Temperature	-55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

AC Characteristics

T_A = 0~70°C, V_{DD}=5±10%

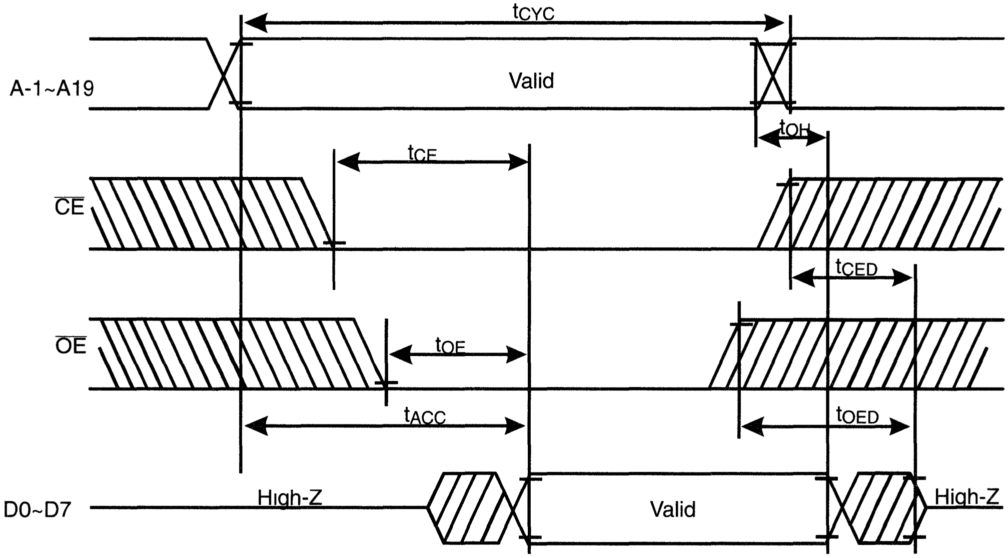
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Cycle Time	t_{CYC}	150	-	-	ns
Address Access Time	t_{ACC}	-	-	150	ns
Chip Enable Access Time	t_{CE}	-	-	150	ns
Output Enable Access Time	t_{OE}	-	-	70	ns
Output Disable Time from $\overline{CE}$	t_{CED}	-	-	40	ns
Output Disable Time from $\overline{OE}$	t_{OED}	-	-	40	ns
Output Hold Time	t_{OH}	5	-	-	ns

AC Test Conditions

Output Load: 100pf + 1TTL
Input Levels: 0.6V, 2.4V
Timing Measurement Reference Levels/Input: 0.8V, 2.2V
Timing Measurement Reference Levels/Output: 0.8V, 2.0V
Input Rise and Fall Time: 5ns

Timing Waveform

BYTE-WIDE READ MODE



Note: $\overline{BYTE}=V_{IL}$

Ordering Information

ICS2122-001M

Example:

ICS XXXX-PPP M

Package Type
M=SOP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS2124-001
ICS2124-002

WaveFront™ Sounds (16M Bit CMOS Mask ROM)

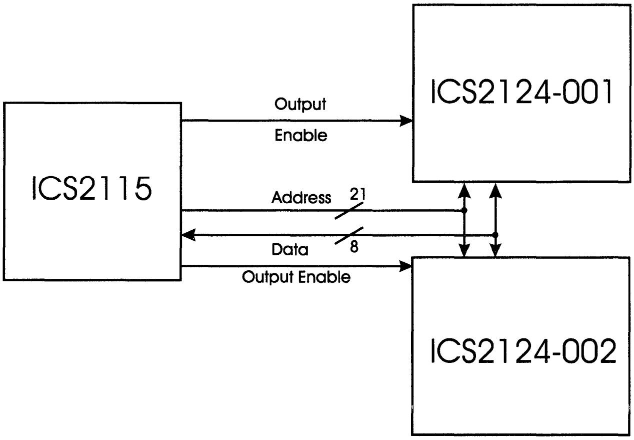
Description

WaveFront Sounds are masked ROMs that serve as the wavetable for the ICS2115 WaveFront Synthesizer. Each sound set, 4 MB, 2 MB and 512 KB, contains the musical data needed to synthesize the instruments from the General MIDI specification. The 4 MB sound set consists of two 2 MB ROMs, the **ICS2124M-001** and **ICS2124M-002**. The 2 MB sound set consists of one 2 MB ROM, the **ICS2122M-001**. The 512 KB sound set consists of one 512 KB ROM, the **ICS2125M-001**.

Features

- Complete set of General MIDI sounds, which contains 128 instruments and 69 drum sounds.
- Available in three sizes, 4 MB, 2 MB & 512 KB, to provide the optimal balance between price and performance for many applications.
- 16-bit linear wavetable (ICS2124-001/-002), compressed wavetable (ICS2122-001), or full-featured wavetable (ICS2125-001).
- Uses 2M x 8 MROMs in 44-pin SOP packages.

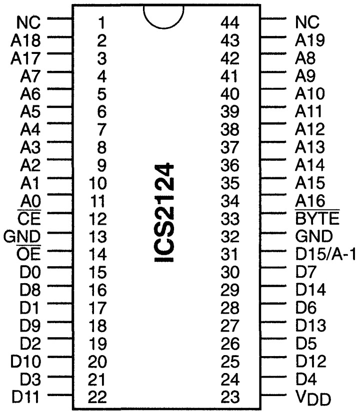
Block Diagram



4 MB Patch Set

WaveFront is a trademark of Integrated Circuit Systems, Inc

Pin Configuration



44-Pin SOP
K-8

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2-11, 34-43	A0-A19	I	Address Inputs
15-22, 24-30	D0-D14	O	Data Outputs
12	$\overline{CE}$	I	Chip Enable Input
14	$\overline{OE}$	I	Output Enable Input
31	D15/A-1	I/O	Data Output/Address Input
33	$\overline{BYTE}$	I	Word, Byte selection Input tied low for byte operation
23	V_{DD}	P	Power Supply
13, 32	GND	P	Ground
1, 44	NC	-	No Connection

Absolute Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-0.5~V_{DD}	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	1.0/0.6	W
T_{STG}	Storage Temperature	-55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

AC Characteristics

T_A = 0~70°C, V_{DD}=5±10%

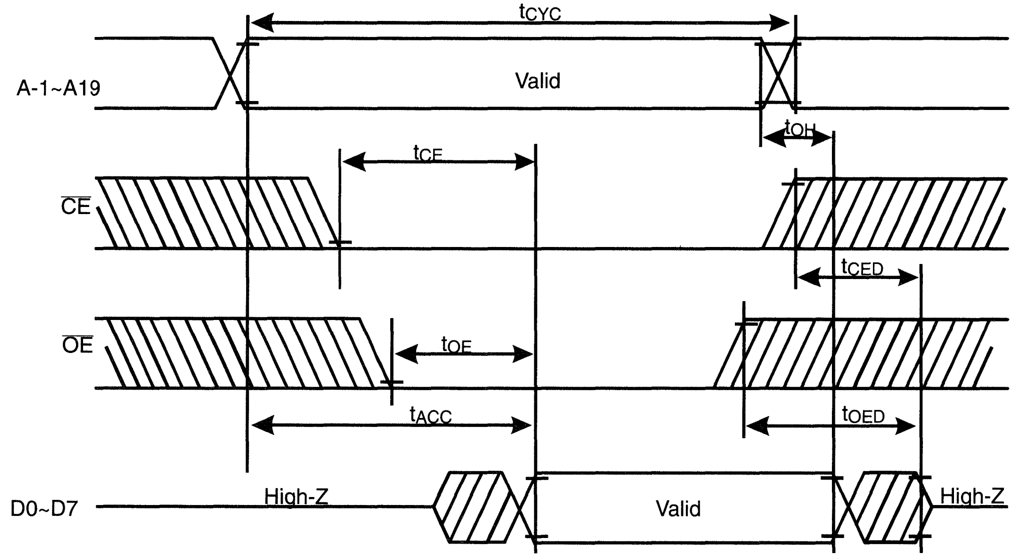
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Cycle Time	t_{CYC}	150	-	-	ns
Address Access Time	t_{ACC}	-	-	150	ns
Chip Enable Access Time	t_{CE}	-	-	150	ns
Output Enable Access Time	t_{OE}	-	-	70	ns
Output Disable Time from $\overline{CE}$	t_{CED}	-	-	40	ns
Output Disable Time from $\overline{OE}$	t_{OED}	-	-	40	ns
Output Hold Time	t_{OH}	5	-	-	ns

AC Test Conditions

Output Load: 100pf + 1TTL
Input Levels: 0.6V, 2.4V
Timing Measurement Reference Levels/Input: 0.8V, 2.2V
Timing Measurement Reference Levels/Output: 0.8V, 2.0V
Input Rise and Fall Time: 5ns

Timing Waveform

BYTE-WIDE READ MODE



Note: $\overline{BYTE}=V_{IL}$

Ordering Information

ICS2124-001M or ICS2124-002M

Example:

ICS XXXX-PPP M

Package Type
M=SOP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS2125

Product Preview

WaveFront™ Sounds (4M bit CMOS Mask ROM)

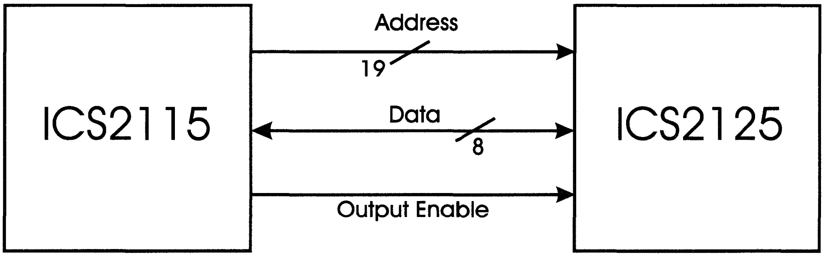
General Description

WaveFront Sounds are masked ROMs that serve as the wavetable for the ICS2115 WaveFront Synthesizer. Three different sounds sets are available: 4 MB (ICS2124-001 and ICS2124-002), 2 MB (ICS2122) and 512 KB (ICS2125). Each sound set contains the musical data needed to synthesize instruments from the General MIDI specification. The 512 KB sound set consists of one 512 KB ROM.

Features

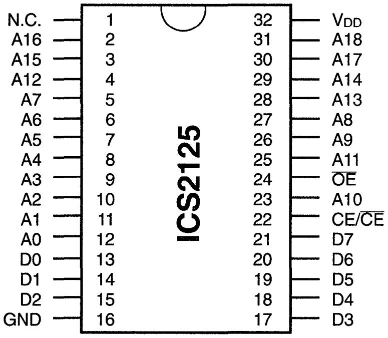
- Full featured set of General MIDI sounds.
- Available in three sizes, 4 MB, 2 MB, and 512 KB to provide the optimal balance between price and performance for many applications.
- Uses 512K Word X 8 bit ROM in a 32-pin SOP package.

Block Diagram



512K Patch Set

Pin Configuration



32-Pin SOP
K-8

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2-12, 23, 25-31	A0 through A18	I	Address Inputs
13-15, 17-21	D0 through D7	O	Data Outputs
24	$\overline{\text{OE}}$	I	Output Enable Input
22	$\overline{\text{CE}}$	I	Chip Enable Input
32	V_{DD}	P	Power Supply
16	GND	P	Ground
1	N.C.	-	No Connection

Absolute Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5-7.0	V
V_{IN}	Input Voltage	-0.5-V_{DD}	V
V_{OUT}	Output Voltage	0 - V_{DD}	V
P_D	Power Dissipation	1.0/0.6	W
T_{STG}	Storage Temperature	-55 to 150	° C
T_{OPR}	Operating Temperature	0 - 70	° C
T_{SOLDER}	Soldering Temperature - Time	260 - 10	° C - sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

AC Characteristics

T_A = 0~70°C, V_{DD}=5±10%

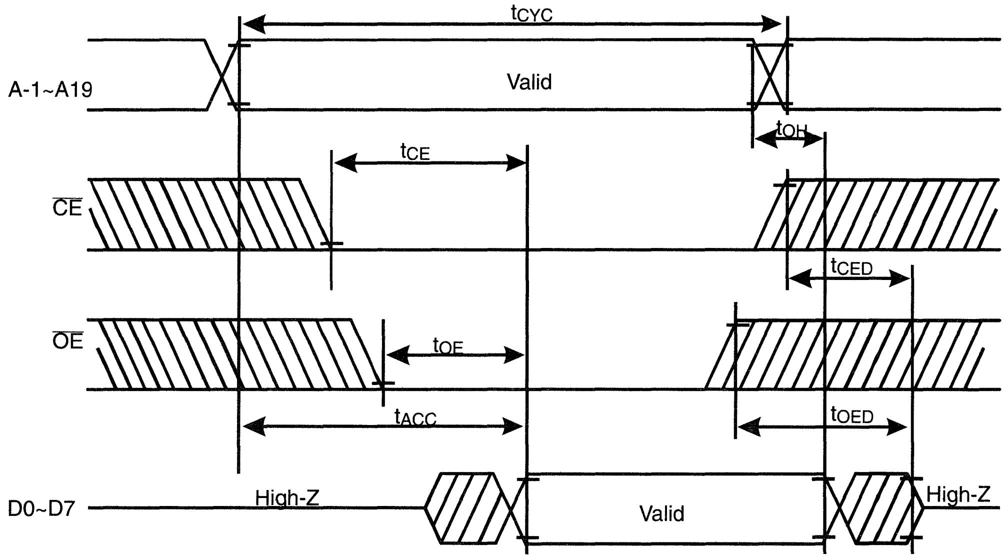
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Cycle Time	t_{CYC}	150	-	-	ns
Address Access Time	t_{ACC}	-	-	150	ns
Chip Enable Access Time	t_{CE}	-	-	150	ns
Output Enable Access Time	t_{OE}	-	-	70	ns
Output Disable Time from $\overline{CE}$	t_{CED}	-	-	40	ns
Output Disable Time from $\overline{OE}$	t_{OED}	-	-	40	ns
Output Hold Time	t_{OH}	5	-	-	ns

AC Test Conditions

Output Load: 100pf + 1TTL
Input Levels: 0.6V, 2.4V
Timing Measurement Reference Levels/Input: 0.8V, 2.2V
Timing Measurement Reference Levels/Output: 0.8V, 2.0V
Input Rise and Fall Time: 5ns

Timing Diagram

BYTE-WIDE READ MODE



Note: $\overline{\text{BYTE}}$=V_{IL}

Ordering Information

ICS2125M

Example:

ICS XXXX M

Package Type
M=SOP

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

ICS
GENDAC
Products

ICS GENDACs provide highly integrated mixed-signal solutions for advanced VGA controllers. These products have been designed utilizing ICS's proven technology for exceptionally low-jitter video clock synthesizers and high-accuracy video DACs. The definitions for these products were written with the close cooperation of VGA controller manufacturers to ensure our customers maximum design flexibility. Our 16-bit pixel path devices are leading-edge components for video systems and establish the industry standard with 70 hertz refresh requirements at resolutions of 1280 x 1024 pixels.

ICS GENDAC Products Selection Guide

Product Applications	ICS Device Type	Description	Package Types	Page
Personal Computer and Engineering Work Station Computer Graphics	ICS5300	8-bit Pixel Port, Triple 8-bit Video DACs, Operation to 135 MHz. 8 Selectable P-Clock Frequencies (6 Programmable).	44-Pin PLCC	H-3
	ICS5301	Tseng Compatibility, 8-bit Pixel Port, Triple 8-bit Video DACs, Operation to 135 MHz. 8 Selectable P-Clock Frequencies (6 Programmable).	44-Pin PLCC	H-33
	ICS5340	16-bit Pixel Port, Triple 8-bit Video DACs, Operation to 135 MHz. 2:1 Pixel Multiplexing. 8 Selectable P-Clock Frequencies (6 Programmable). 2 Selectable and Programmable M-Clock Frequencies.	68-Pin PLCC	H-63
	ICS5341	Tseng Compatibility, 16-bit Pixel Port, Triple 8-bit Video DACs, Operation to 135 MHz. 2:1 Pixel Multiplexing. 8 Selectable P-Clock Frequencies (6 Programmable). 2 Selectable and Programmable M-Clock Frequencies.	68-Pin PLCC	H-97
	ICS5342	S3 SDAC compatible, 16-bit Pixel Port, Triple 8-bit video DACs, Operation to 135 MHz. 2:1 Pixel Clock Doubler. 8 Selectable P clock frequencies (8 Programmable). 2 Selectable and Programmable M-Clock Frequencies. 24-bit Packed Pixel Support. On-the-Fly mode Select Pin Allows Pixel Color Depth Switching.	68-Pin PLCC	H-101

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. ICS reserves the right to change or discontinue these products without notice.

Integrated
Circuit
Systems, Inc.

ICS5300
GENDAC

8-bit Integrated Clock-LUT-DAC

General Description

The ICS5300 GENDAC is a combination of dual programmable clock generators, a 256 x 18-bit RAM, and a triple 8-bit video DAC. The GENDAC supports 8-bit pseudo color applications, as well as 15-bit, 16-bit and 24-bit True Color bypass for high speed, direct access to the DACs.

The RAM makes it possible to display 256 colors selected from a possible 262, 144 colors. The dual clock generators use Phase Locked Loop (PLL) technology to provide programmable frequencies for use in the graphics subsystem. The video clock contains 8 frequencies, 6 of which are programmable by the user. The memory clock has one programmable frequency location.

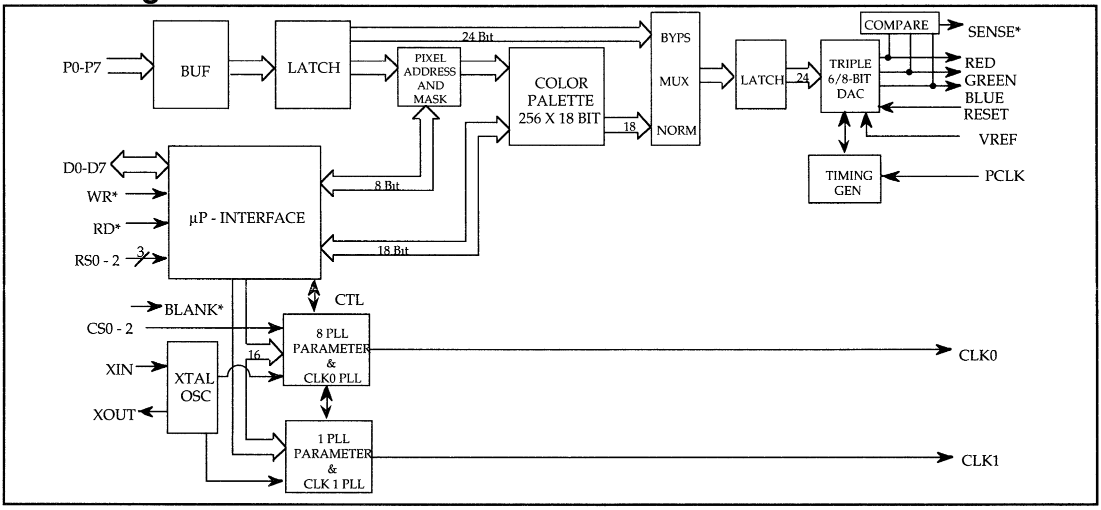
The three 8-bit DACs on the ICS5300 are capable of driving singly or doubly-terminated 75Ω loads to nominal 0 - 0.7 volts at pixel rates up to 135 MHz. Differential and integral linearity errors are less than 1 LSB over full temperature and V_{DD} ranges. Monotonicity is guaranteed by design. On-chip pixel mask register allows displayed colors to be changed in a single write cycle rather than by modifying the color palette.

ICS is the world leader in all aspects of frequency (clock) generation for graphics, using patented techniques to produce low jitter video timing.

Features

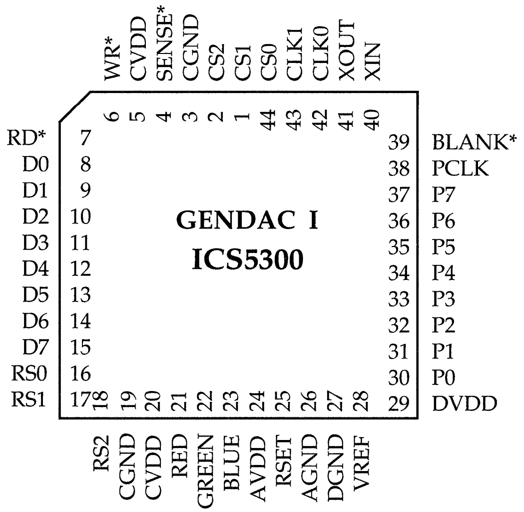
- **Triple video DAC, dual clock generator, and a color palette**
- **24, 16, 15, or 8-bit pseudo color pixel mode supports True Color, Hi-Color, and VGA modes**
- **High speed 256 x 18 color palette (135 MHz) with bypass mode and 8-bit DACs**
- **Two fixed, six programmable video (pixel) clock frequencies (CLK0)**
- **One programmable memory (controller) clock frequency (CLK1)**
- **DAC power down in blanking mode**
- **Low power operation**
- **Anti-sparkle circuitry**
- **On-chip loop filters reduce external components**
- **Standard CPU interface**
- **Single external crystal (typically 14.318 MHz)**
- **Monitor Sense**
- **Internal voltage reference**
- **135 MHz (-3), 110 MHz (-2) & 80 MHz (-1) versions**
- **Very low clock jitter**

Block Diagram



ICS5300
GENDAC

Pin Configuration



Pin Description (68 pin PLCC) K-10

Symbol	Pin #	Type	Description
CS1	1	Input	Clock select 1. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output.
CS2	2	Input	Clock select 2. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output.
CGND	3	-	Ground for clock circuits. Connect to ground.
SENSE*	4	Output	Monitor Sense, active low. This pin is low when any of the red, green, or blue outputs have exceeded 335mV. The chip has on-board comparators and an internal 335mV voltage reference. This is used to detect monitor type.
CVDD	5	-	Clock Power Supply. Connect to DVDD
WR*	6	Input	RAM/PLL Write Enable, active low. This signal controls the timing of the write operation on the microprocessor interface inputs, D0-D7.
RD*	7	Input	RAM/PLL Read Enable, active low. This is the READ bus control signal. When active, any information present on the internal data bus is available on the Data I/O lines, D0-D7.
D0 - D7	8 - 15	I/O	System data bus I/O. These bidirectional Data I/O lines are used by the host microprocessor to write (using active low WR*) information into, and read (using active low RD*) information from the six internal registers (Pixel Address, Color Value, Pixel Mask, PLL Address, PLL Parameter, and Command). During the write cycle, the rising edge of WR* latches the data into the selected register (set by the status of the three RS pins). The rising edge of RD* determines the end of the read cycle. When RD* is a logical high, the Data I/O lines no longer contain information from the selected register and will go into a tri-state mode.

Pin Description (continued)

Symbol	Pin #	Type	Description
RS0 RS1 RS2	16 17 18	Input Input Input	Register Address Select 0. These inputs control the selection of one of the six internal registers. They are sampled on the falling edge of the active enable signal (RD* or WR*).
CGND	19	-	Ground for clock circuits. Connect to ground
CVDD	20	-	Clock Power Supply. Connect to AVDD
RED GREEN BLUE	21 22 23	Output Output Output	Color Signals. These three signals are the DACs' analog outputs. Each DAC is composed of several current sources. The outputs of each of the sources are added together according to the applied binary value. These outputs are typically used to drive a CRT monitor.
AVDD	24	-	Analog power supply. Connect to AVDD
RSET	25	Input	Resistor Set. This pin is used to set the current level in the analog outputs. It is usually connected through a 140Ω, 1% resistor to ground.
AGND	26	-	Analog Ground. Connect to ground
DGND	27	-	Digital Ground. Connect to ground
VREF	28	Input	Internal Reference Voltage. Normally connects to a 0.1µF cap to ground. To use an external Vref, connect a 1.235V reference to this pin.
DVDD	29	-	Digital power supply.
P0 - P7	30 - 37	Input	Pixel Address Lines. This byte-wide information is latched by the rising edge of PCLK when using the Color Palette, and is masked by the Pixel Mask register. These values are used to specify the RAM word address in the default mode (accessing RAM). In the Hi-Color XGA, and True Color modes, they represent color data for the DACs. These inputs should be grounded if they are not used.
PCLK	38	Input	Pixel Clock. The rising edge of PCLK controls the latching of the Pixel Address Anding inputs. This clock also controls the progress of these values through the three-stage pipeline of the Color Palette RAM, DAC, and outputs.
BLANK*	39	Input	Composite BLANK* Signal, active low. When BLANK* is asserted, the outputs of the DACs are zero and the screen becomes black. The DACs are automatically powered down to save current during blanking. The color palette may still be updated through D0-D7 during blanking.
XIN	40	Input	Crystal input. A 14.318 MHz crystal should be connected to this pin.
XOUT	41	Output	Crystal output. A 14.318 MHz crystal should be connected to this pin.
CLK0	42	Output	Video clock output. Provides a CMOS level pixel or dot clock frequency to the graphics controller. The output frequency is determined by the values of the PLL registers.
CLK1	43	Output	Memory clock output. Used to time the video memory.
CS0	44	Input	Clock select 0. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output.

Internal Registers

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
				There is a single Pixel Address register within the GENDAC. This register can be accessed through either register address 0,0,0 or register address 0,1,1. A read from address 0,0,0 is identical to a read from address 0,1,1. Writing a value to address 0,0,0 performs the following operations: a) Specifies an address within the color palette RAM. b) Initializes the Color Value register. Writing a value to address 0,1,1 performs the following operations: a) Specifies an address within the color palette RAM. b) Loads the Color Value register with the contents of the location in the addressed RAM palette and then increments the Pixel Address register.
0	0	0	Pixel Address WRITE	Writing to this 8-bit register is performed prior to writing one or more color values to the color palette RAM.
0	1	1	Pixel Address READ	Writing to this 8-bit register is performed prior to reading one or more color values from the color palette RAM.
0	0	1	Color Value	The 18-bit Color Value register acts as a buffer between the microprocessor interface and the color palette. Using a three bytes transfer sequence allows a value to be read from or written to this register. When a byte is read, the color value is contained in the least significant 6 bits , D0-D5 (the most significant 2 bits are set to zero). When writing a byte, the same 6 bits are used. When reading or writing, data is transferred in the same order - the red byte first, then green, then blue. Each transfer between the Color Value register and the color palette replaces the normal pixel mapping operations of the GENDAC for a single pixel. After writing three definitions to this register, its contents are written to the location in the color palette RAM specified by the Pixel Address register, and the Pixel Address register increments. After reading three definitions from this register, the contents of the location in the color palette RAM specified by the Pixel Address registers are copied into the Color Value register, and the Pixel Address register increments.
0	1	0	Pixel Mask	The 8-bit Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P0-P7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, while a zero sets that bit to zero. The Pixel Mask register does not affect the Pixel Address generated by the microprocessor interface when the palette RAM is being accessed.

Internal Registers (continued)

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
1	0	0	PLL Address WRITE	Writing to this 8-bit register is performed prior to writing one or more PLL programming values to the PLL Parameter register.
1	1	1	PLL Address READ	Writing to this 8-bit register is performed prior to reading one or more PLL programming values from the PLL Parameter register.
1	1	0	Command	This8-bit register selects the color mode, for instance 8-bit Pseudo Color, Hi-Color , True Color, or XGA, and DAC power down. The registers are reset to pseudo color mode on power up.
1	0	1	PLL Parameter	There are sixteen parameter registers as indexed by PLL Address Write/ Readregisters. Parameter registers 00-0D and 0F are two bytes long and 0E is one byte long. This register set contains one control register. The bits of this register include clock select and enable functions, the rest contain PLL frequency parameters. After writing the start index address in the PLL address register, these registers can be accessed in successive two (or one) bytes. The address register auto increments after one or two bytes to access the entire register set.

Absolute Maximum Ratings

Power Supply Voltage	7 V
Voltage on any other pin	GND – 0.5V to V_{DD} + 0.5V
Temperature under bias	– 40° C to 85° C
Storage Temperature	– 65° C to 150° C
DC Digital Output Current	25 mA
Analog Output Current	45 mA
Reference Current	–15 mA
Power Dissipation	1.0 W

Note Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
DC CHARACTERISTICS (note: J)					
V_{DD}	Positive supply voltage		4.75	5.25	V
V_{IH}	Input logic "1" voltage		2.0	V_{DD} + 0.5	V
V_{IL}	Input logic "0" voltage		– 0.5	0.8	V
I_{REF}	Reference current		-7.0	-10	mA
V_{REF}	Reference voltage		1.10	1.35	V
I_{IN}	Digital input current	V_{DD} = max, GND ≤ V_{IN} ≤ V_{DD}		± 10	µA
I_{OZ}	Off-state digital output current	V_{DD} = max, GND ≤ V_{IN} ≤ V_{DD}		± 50	µA
I_{DD}	Average power supply current	I_O = max, Digital outputs unloaded		250	mA
I_{DACOFF}	DACs in power down mode	No palette access		50	mA
V_{OH}	Output logic "1"	I_O = -3.2mA, note K	2.4		V
V_{OL}	Output logic "0"	I_O = -3.2mA, note K		0.4	V
$ICLK_r$	Input Clock Rise Time	TTL levels		15	ns
$ICLK_f$	Input Clock Fall Time	TTL levels		15	ns
F_D	Frequency Change of CLK0 and CLK1 over supply and temperature	With respect to typical frequency		0.05	%

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Units
DAC CHARACTERISTICS (note: J)					
V_O (max)	Maximum output voltage	$I_O \le 10$ mA		1.5	V
I_O (max)	Maximum output current	$V_O \le 1$V		21	mA
	Full scale error	note A, B		± 5	%
	DAC to DAC correlation	note B		±2	%
	Integral Linearity, 6-bit	note B		±0.5	LSB
	Integral Linearity, 8-bit	note B		±1	LSB
	Full scale settling time*, 6-bit	note C		28	ns
	Full scale settling time*, 8-bit	note C		20	ns
	Rise time (10% to 90%)*	note C		6	ns
	Glitch energy*	note C		200	pVsec

* Characterized values only

Symbol	Parameter	Conditions	Min	Max	Units
PLL AC CHARACTERISTICS					
f_0	Clock 0 operating range		25	135	MHz
f_1	Clock 1 operating range		25	135	MHz
t_r	Output clocks rise time	25 pf load, TTL levels		1.5	ns
t_r	Output clocks fall time	25 pf load, TTL levels		1.5	ns
d_t	Duty Cycle		40/60	60/40	%
j_{1s}	Jitter, one sigma			130 ps	ps
j_{abs}	Jitter, absolute		-300 ps	300 ps	ps
f_{ref}	Input reference frequency	Typically 14.318 MHz	5	25	MHz

AC Electrical Characteristics (note: J)

Symbol	Parameter	Condition	80 MHz		110 MHz		135 MHz		Units
			Min	Max	Min	Max	Min	Max	
t_{CHCH}	PCLK period		12.5		9.09		7.4		ns
Δt_{CHCH}	PCLK jitter	note D		±2.5		+2.5			%
t_{CLCH}	PCLK width low		5		3.6		3		ns
t_{CHCL}	PCLK width high		5		3.6		3		ns
t_{PVCH}	Pixel word setup time	note E	3		3		2		ns
t_{CHPX}	Pixel word hold time	note E	3		2		1		ns
t_{BVCH}	BLANK* setup time	note E	3		3		2		ns
t_{CHBX}	BLANK* hold time	note E	3		2		1		ns
t_{CHAV}	PCLK to valid DAC output	note F		20		20		20	ns
Δt_{CHAV}	Differential output delay	note G		2		2		2	ns
t_{WLWH}	WR* pulse width low		50		50		50		ns
t_{RLRH}	RD* pulse width low		50		50		50		ns
t_{SVWL}	Register select setup time	Write cycle	10		10		10		ns
t_{SVRL}	Register select setup time	Read cycle	10		10		10		ns
t_{WLSX}	Register select hold time	Write cycle	10		10		10		ns
t_{RLSX}	Register select hold time	Read cycle	10		10		10		ns
t_{DVWH}	WR* data setup time		10		10		10		ns
t_{WHDX}	WR* data hold time		10		10		10		ns
t_{RLQX}	Output turn-on delay		5		5		5		ns
t_{RLQV}	RD* enable access time			40		40		40	ns
t_{RHQX}	Output hold time		5		5		5		ns
t_{RHQZ}	Output turn-off delay	note H		20		20		20	ns
t_{WHWL1}	Successive write interval	note I	4 (t_{CHCH}		4 (t_{CHCH})		4 (t_{CHCH}		cycle
t_{WHRL1}	WR* followed by read interval	note I	4 (t_{CHCH}		4 (t_{CHCH})		4 (t_{CHCH}		cycle
t_{RHRL1}	Successive read interval	note I	4 (t_{CHCH}		4 (t_{CHCH})		4 (t_{CHCH}		cycle
t_{RHWL1}	RD* followed by write interval	note I	4 (t_{CHCH}		4 (t_{CHCH})		4 (t_{CHCH}		cycle
t_{WHWL2}	WR* after color write	note I	4 (t_{CHCH}		4 (t_{CHCH})		4 (t_{CHCH}		cycle
t_{WHRL2}	RD* after color write	note I	4 (t_{CHCH}		4 (t_{CHCH})		4 (t_{CHCH}		cycle
t_{RHRL2}	RD* after color read	note I	8 (t_{CHCH}		8 (t_{CHCH})		8 (t_{CHCH}		cycle
t_{RHWL2}	WR* after color read	note I	8 (t_{CHCH}		8 (t_{CHCH})		8 (t_{CHCH}		cycle
t_{WHRL3}	RD* after read address write	note I	8 (t_{CHCH}		8 (t_{CHCH})		8 (t_{CHCH}		cycle
t_{SOD}	SENSE* output delay			1		1	1		µs

NOTES

A. Full scale error is derived from design equation $\{[(F.S.I_{OUT})\ R_L - 2.1\ (I_{REF})\ R_L]/[2.1(I_{REF})R_L]\}$ 100%

$V_{BLACK\ LEVEL}$=0V $F.S.I_{OUT}$ = Actual full scale measured output

B R= 37 5Ω, I_{REF} = – 8 88mA

C. Z_I = 37.5Ω + 30 pF, I_{REF} = – 8 88mA

D. This parameter is the allowed Pixel Clock frequency variation. It does not permit the Pixel Clock period to vary outside the minimum values for Pixel Clock (t_{CHCH}) period.

E It is required that the color palette's pixel address be a valid logic level with the appropriate setup and hold times at each rising edge of P_{CLK} (this requirement includes the blanking period).

F. The output delay is measured from the 50% point of the rising edge of CLOCK to the valid analog output. A valid analog output is defined when the analog signal is halfway between its successive values

G. This applies to different analog outputs on the same device

H Measured at ± 200 mV from steady state output voltage.

I. This parameter allows synchronization between operations on the microprocessor interface and the pixel stream being processed by the color palette.

J. The following specifications apply for V_{DD}= +5V± 0.5V, GND=0. Operating Temperature = 0°C to 70°C.

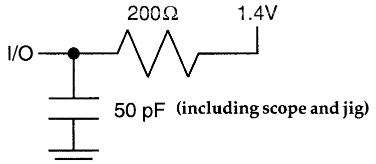
K. Except for SENSE pin.

AC Test Conditions

Input pulse levels..V_{DD} to 3V
Input rise and fall times (10% to 90%)..........................3ns
Digital input timing reference level...........................1.5V
Digital output timing reference level........0.8V and 2.4V

Capacitance

C_1 Digital input..7pF
C_0 Digital output..7pF
C_{0A} Analog output...10pF



DIGITAL OUTPUT LOAD

General Operation

The ICS5300 GENDAC is intended for use as the analog output stage of raster scan video systems. It contains a high-speed Random Access Memory of 256 x 18-bit words, three 6/8-bit high-speed DACs, a microprocessor/graphic controller interface, a pixel word mask, on-chip comparators, and two user programmable frequency generators.

An externally generated BLANK* signal can be applied to pin 39 of the ICS5300. This signal acts on all three of the analog outputs. The BLANK* signal is delayed internally so that it appears with the correct relationship to the pixel bit stream at the analog outputs.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the color palette RAM to facilitate such operations as animation and flashing objects. Operations on the contents of the mask register can also be totally asynchronous to the pixel stream.

The ICS5300 also includes dual PLL frequency generators providing a video clock (CLK0) and a memory clock (CLK1), both generated from a single 14.318 MHz crystal. There are eight selectable CLK0 frequencies of which six are programmable, and a single programmable CLK1 frequency. Default values (Table 1 and Table 2) are loaded into the appropriate registers on power up.

Video Path

The GENDAC supports four different video modes and is determined by bits 5-7 of the command register. The default mode is the 6-bit Pseudo Color mode. The other modes are the bypass 15-bit, 16-bit and 24 bit True Color.

Pseudo color

In this mode, Pixel Address and BLANK* inputs are sampled on the rising edge of the clock (PCLK) and any change appears at the analog outputs after three succeeding rising edges of the clock. The DAC outputs depends on the data in the color palette RAM.

Bypass Modes

The GENDAC supports three different bypass modes; 15-bit (5,5,5) mode, 16-bit (5,6,5) mode and the 24-bit True Color 8-bit DAC mode. In these modes, the pixel address pins P0-P7 represent the Color Data that is applied directly to the DAC. The internal RAM is bypassed. In the 15/16-bit mode two consecutive bytes contain the 15/16 bits of color data. Two consecutive rising edges of the PCLK latch the data on the P0-P7 pins into registers and the byte framing is internally synchronized with the rising edge of BLANK*. The internal pipe line delay from the "first byte" to the DAC is four PCLK rising edges. In the 24-bit True Color mode, three bytes contains the 24-bit color data. Three consecutive rising edges of the PCLK latch the data. The framing is the same as the 15/16-bit mode. The internal pipe line delay from the "first byte" to the DAC is five PCLK rising edges.

DAC Outputs

The outputs of the DACs are designed to be capable of producing 0.7 volt peak white amplitude with an I_{REF} of 8.88 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output load ($R_{EFFECTIVE}$) of 37.5Ω.

The formula for calculating I_{REF} with various peak white voltage/output loading combinations is given below:

$$I_{REF} = \frac{V_{PEAK\ WHITE}}{2.1 \times R_{EFFECTIVE}}$$

Note that for all values of I_{REF} and output loading:

$$V_{BLACK\ LEVEL} = 0$$

The reference current I_{REF} is determined by the reference voltage V_{REF} and the value of the resistor connected to R_{SET} pin. V_{REF} can be the internal band gap reference voltage or can be overridden by an external voltage. In both cases $I_{REF} = V_{REF}/R_{SET}$.

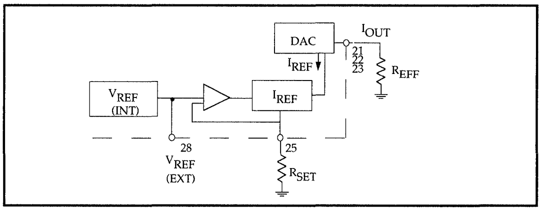


Figure 4 - DAC Set up

The BLANK* input to the GENDAC acts on all three of the DAC outputs. When the BLANK* input is low, the DACs are powered down.

The connection between the DAC outputs of the ICS5300 and the RGB inputs of the monitor should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor.

RF techniques should be observed to ensure good fidelity. The PCB trace connecting the GENDAC to the off-board connector should be sized to form a transmission line of the correct impedance. Correctly matched RF connectors should be used for connection from the PCB to the coaxial cable leading to the monitor and from the cable to the monitor.

There are two recommended methods of DAC termination: double termination and buffered signal. Each is described below with its relative merits:

Double Termination (Figure 1)
For this termination scheme, a load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line. Double termination of the DAC output allows both ends of the transmission line between the DAC outputs and the monitor inputs to be correctly matched. The result should be an ideal reflection free system. This arrangement is relatively tolerant to variations in transmission line impedance (e.g. a mismatched connector) since no reflections occur from either end of the line.

A doubly terminated DAC output will rise faster than any singly terminated output because the rise time of the DAC outputs is dependent on the RC time constant of the load.

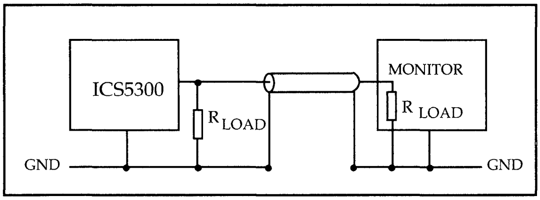


Figure 1 - Double Termination

Buffered Signal (Figure 2)
If the GENDAC drives large capacitive loads (for instance long cable runs), it may be necessary to buffer the DAC outputs. The buffer will have a relatively high input impedance. The connection between the DAC outputs and the buffer inputs should also be considered as a transmission line. The buffer output will have a relatively low impedance. It should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.

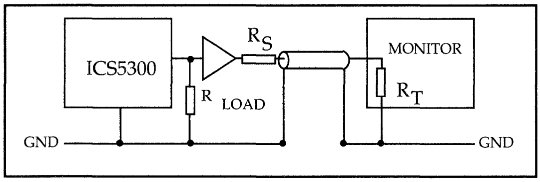


Figure 2 - Buffered Signal

SENSE Output

The GENDAC contains three comparators, one each for the DAC output (R, G and B) lines. The reference voltage to the comparators is proportional to the V_{REF} (internal or external) and is typically 0.33 for V_{REF} =1.23 Volts. When the voltage on any of these pins go higher than the reference voltage to the comparators, the SENSE* pin is driven low. This signal is used to detect the type of (or lack of) monitor connected to the system.

PLL Clock

The ICS5300 has dual PLL frequency generators for generating the video clock (CLK0) and memory clock (CLK1) needed for graphics subsystems. Both these clocks are generated from a single 14.318 MHz crystal or can be driven by an external clock source. The chip includes the capacitors for the crystal and all the components needed for the PLL loop filters, .minimizing board component count.

There are eight possible video clock, CLK0, frequencies (f0-f7) which can be selected by the external pins CS0-CS2. Pins are software selectable by setting a bit in the PLL control register. Two of these frequencies (f0-f1) are fixed and the other six (f2-f7) can be programmed for any frequency by writing appropriate parameter values to the PLL parameter registers. The default frequencies on power up are commonly used video frequencies (table 1). At power up, the frequencies can be selected by pins CS0-CS2. There is only a single programmable memory clock frequency (CLK1). On power up this frequency defaults to the frequency given in table 2. The memory clock transition between frequencies is smooth and glitch free if the transition is kept between the limits 45-65 MHz.

fn	**(MHz)**	**VLCK Comments**
f0	25.175	VGA0 (VGA Color monitor) (fixed)
f1	28.322	VGA1 (VGA Monochrome monitor) (fixed)
f2	31.500	VESA 640 x 480 @72 Hz (programmable)
f3	36.00	VESA 800 x 600 @56 Hz (programmable)
f4	40.00	VESA 800 x 600 @60 Hz (programmable)
f5	44.889	1024 x 768 @43 Hz Interlaced (programmable)
f6	65.00	1024 x 768 @ 60 Hz, 640 x 480 Hi-Color @ 72 Hz (programmable)
f7	75.00	VESA 1024 x 768 @ 70 Hz, True Color 640 x 480 (programmable)

Table 1 - Video clock (CLK0) default frequency register (with a 14.318 MHz input)

fn	MHz	Comments
fA	45.00 MHz	Memory and GUI subsystem clock

Table 2 - Memory Clock (CLK1) default frequency register

Microprocessor Interface

Below are listed the six microprocessor interface registers within the ICS5300, and the register addresses through which they can be accessed.

RS2	RS1	RS0	Register Name
0	0	0	Pixel Address (write mode)
0	1	1	Pixel Address (read mode)
0	0	1	Color Value
0	1	0	Pixel Mask
1	0	0	PLL Address (write mode)
1	0	1	PLL Parameter
1	1	0	Command
1	1	1	PLL Address (read mode)
0/HF	1	0	Command Register accessed by (hidden) flag after special sequence of events

Table 3 - Microprocessor Interface Registers

Asynchronous Access to Microprocessor Interface

Accesses to all registers may occur without reference to the high speed timing of the pixel bit stream being processed by the GENDAC. Data transfers between the color palette RAM and the Color Value register, as well as modifications to the Pixel Mask register, are synchronized to the Pixel Clock by internal logic. This is done in the period between microprocessor interface accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow the appropriate transfers or modifications to take place. Access to PLL address, PLL parameter and to the command register are asynchronous to the pixel clock.

The contents of the palette RAM can be accessed via the Color Value register and the Pixel Address registers.

Writing to the color palette RAM

To set a new color definition, a value specifying a location in the color palette RAM is first written to the Write mode Pixel Address register. The values for the red, green and blue intensities are then written in succession to the Color Value register. After the blue data is written to the Color Value register, the new color definition is transferred to the RAM, and the Pixel Address register is automatically incremented.

Writing new color definitions to a set of consecutive locations in the RAM is made easy by this auto-incrementing feature. First, the start address of the set of locations is written to the write mode Pixel Address register, followed by the color definition of that location. Since the address is incremented after each color definition is written, the color definition for the next location can be written immediately. Thus, the color definitions for consecutive locations can be written sequentially to the Color Value register without re-writing to the Pixel Address register each time.

Reading from the RAM

To read a color definition, a value specifying the location in the palette RAM to be read is written to the read mode Pixel Address register. After this value has been written, the contents of the location specified are copied to the Color Value register, and the Pixel Address register automatically increments.

The red, green and blue intensity values can be read by a sequence of three reads from the Color Value register. After the blue value has been read, the location in the RAM currently specified by the Pixel Address register is copied to the Color Value register and the Pixel Address again automatically increments. A set of color values in consecutive locations can be read simply by writing the start address of the set to the read mode Pixel Address register and then sequentially reading the color values for each location in the set. Whenever the Pixel Address register is updated, any unfinished color definition read or write is aborted and a new one may begin.

The Pixel Mask Register

The pixel address used to access the RAM through the pixel interface is the result of the bitwise ANDing of the

incoming pixel address and of the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colors without altering the video memory or the RAM contents. By partitioning the color definitions by one or more bits in the pixel address, such effects as rapid animation, overlays, and flashing objects can be produced.

The Pixel Mask register is independent of the Pixel Address and Color Value registers.

The Command Register

The Command register is used to select the various GENDAC color modes and to set the power down mode. On power up this register defaults to an 6-bit Pseudo Color mode. This register can be accessed by control pins RS2-RS0, or by a special sequence of events for graphics subsystems that do not have the control signal RS2. For graphic systems that do not have RS2, this pin is tied low and an internal flag (HF; Hidden Flag) is set when the pixel mask register is read four times consecutively. Once the flag is set, the following Read or Write to the pixel mask register is directed to the command register. The flag is reset for Read or Write to any register other than the pixel mask register. The sequence has to be repeated for any subsequent access to the command register.

The PLL Parameter Register

The CLK0 and CLK1 of the ICS5300 can be programmed for different frequencies by writing different values to the PLL parameter register bank. There are eight registers in the parameter register; seven are two bytes long and one (0E) is one byte long.

Writing to the PLL parameter register

To write the PLL parameter data, the corresponding address location is first written to the PLL address register. For software compatibility with other chips, two address registers are defined; the Write mode PLL address register and the Read mode PLL address register. They are actually a single Read/Write register in the ICS5300. The next PLL parameter write will be directed to the first byte of the address location specified by the PLL address register. The next Write to the parameter register will automatically be to the second byte of this register. At the end of the second Write the address is automatically incremented. For the one byte "0E" register the address location is incremented after the first byte Write. If this frequency is selected while programming, the output frequency will change at the end of the second Write.

Reading the PLL parameter register

To read one of the registers of the PLL parameter register the address value corresponding to the location is first written to the PLL address register. The next PLL parameter read will be directed to the first byte of the address location pointed by this index register. A next Read of the parameter register will automatically be the second byte of this register. At the end of the second Read, the address location is automatically incremented. The address register (0E) is incremented after the first byte Read.

Power Down Mode

When bit 0 in the Command register is high (set to 1), the GENDAC enters the DAC power down mode. The DACs are turned off, and the data is retained in the RAM. It is possible to access the RAM, in which case the current will temporarily increase. While the RAM is being accessed, the current consumption will be proportional to the speed of the clock. There is no effect on either clock generator while in this mode.

Power Supply

As a high speed CMOS device, the ICS5300 may draw large transient currents from the power supply, it is necessary to adopt high frequency board layout and power distribution techniques to ensure proper operation of the GENDAC. Please refer to the suggested layout on page 29.

To supply the transient currents required by the ICS5300, the impedance in the decoupling path should be kept to a minimum between the power supply pins V_{DD} and GND. It is recommended that the decoupling capacitance between V_{DD} and GND should be a 0.1μF high frequency capacitor, in parallel with a large tantalum capacitor with

a value between 22μF and 47μF. A ferrite bead may be added in series with the positive supply to form a low pass filter and further improve the power supply local to the GENDAC. It will also reduce EMI.

The combination of series impedance in the ground supply to the GENDAC, and transients in the current drawn by the device will appear as differences in the GND voltages to the GENDAC and to the digital devices driving it. To minimize this differential ground noise, the impedance in the ground supply between the GENDAC and the digital devices driving it should be minimized.

Digital Output Information

The PCB trace lines between the outputs of the TTL devices driving the GENDAC and the input to the GENDAC behave like low impedance transmission lines driven from a low impedance transmission source and terminated with a high impedance. In accordance with transmission line principles, signal transitions will be reflected from the high impedance input to the device. Similarly, signal transitions will be inverted and reflected from the low impedance TTL output. Line termination is recommended to reduce or eliminate the ringing, particularly the undershoot caused by reflections. The termination may either be series or parallel.

Series termination is the recommended technique to use. It has the advantages of drawing no DC current and of using fewer components. Series termination is accomplished by placing a resistor in series with the signal at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and ensures that any signal incident on the TTL output is not reflected.

To minimize reflections, some experimentation will have to be done to find the proper value to use for the series termination. Generally, a value around 100Ω will be required. Since each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. Therefore, the proper value of resistance should be found empirically.

Functional Description

This section describes the register address and bit definition for RAMDAC and the Frequency Synthesizer sections.

Color Palette

Command Register

(RS0-RS2 = 011)
(RS0-RS1 = 01 with hidden flag)

By setting bits in the command register the ICS5300 can be programmed for different color modes and can be powered down for low power operation.

7 6 5	4 3 2 1	0
Color Mode 2 1 0	Reserved Should all =0	Snooze

Table 3 - Command Registers

Bit 7-5 **Color Mode Select**
These three bits select the Color Mode of RAMDAC operation as shown in the following table 4 (default is 0 at power up):

Bit 4 - 1 **(Reserved)**

Bit 0 **Power Down Mode of RAMDAC**
When this bit is set to 0 (default is 0), the device operates normally. If this bit is set to 1, the power and clock to the Color Palette RAM and DACs are turned off. The data in the Color Palette RAM are still preserved. The CPU can access without loss of data by internal automatic clock start/stop control. The DAC outputs become the same as BLANK* (sync) level output during power down mode. This bit does not effect the PLL clock synthesizer function.

Color Modes

The four selectable color modes are described here.

Mode 0: 8-bit Pseudo Color (one clock per pixel). This mode is the 8-bit per pixel Pseudo Color mode. In this mode. inputs P0-P7 are the pixel address for the color palette RAM and are latched on the rising edge of every PCLK. This is the default mode on power up and it is selected by setting bits CR7-CR5 to 000 . There are three clock cycles pipe line delays from input to DAC output.

8-bit Pseudo Color mode

DATA BYTE							
7	6	5	4	3	2	1	0
PIXEL ACCESS							
7	6	5	4	3	2	1	0

CM2 (CR7)	CM1 (CR6)	CM0 (CR5)	Color Mode	Clock Cycles/ Pixel Bits
0	0	0	6-Bit Pseudo Color with Palette (Default)	1
0	0	1	15-Bit Direct Color with Bypass (Hi-Color)	2
0	1	0	24-Bit True Color with Bypass (True Color)	3
0	1	1	16-Bit Direct Color with Bypass (XGA)	2
1	0	0	15-Bit Direct Color with Bypass (Hi-Color)	2
1	0	1	15-Bit Direct Color with Bypass (Hi-Color)	2
1	1	0	16-Bit Direct Color with Bypass (XGA)	2
1	1	1	24-Bit True Color with Bypass (True Color)	3

Table 4 - Color Mode Select

Mode 1: (15-bit per color bypassHi-Color mode).
This mode is the 15-bit per pixel bypass mode. In this mode, inputs P0-P7 are the color DATA and are input directly to the DAC, bypassing the color palette. The two bytes of data is latched in two successive PCLK rising edges. ICS5300 supports only the two clock mode and does not support the mode where the data are latched on the rising and the falling edges. For compatibility, the 15/16 one clock modes are selected as two clock modes in this chip. The low-byte, high byte synchronization is internally done by the rising edge of BLANK*. Each color is 5-bit wide and is packed into two bytes as shown below. The mode is selected by setting bits CR7-CR5 to 001, 100 or 101.

15-Bit Color Mode
3LSB = set to zero

SECOND BYTE								FIRST BYTE							
P 7	P 6	P 5	P 4	P 3	P 2	P 1	P 0	P 7	P 6	P 5	P 4	P 3	P 2	P 1	P 0
X	7	6	5	4	3	7	6	5	4	3	7	6	5	4	3
	RED				GREEN						BLUE				

Mode 2: (16-bit per pixel bypass XGA mode).
This mode is the 16-bit per pixel bypass mode and the P0-P7 inputs to go to the DAC directly, bypassing the color palette. The 2 bytes data is latched on two successive rising edges and the low-byte, high-byte synchronization is internally done by the rising edge of BLANK*. In this mode, blue and red colors are 6 bits wide and green is 5 bits wide. The 2 bytes of data is packed as shown below. The mode is selected by setting bits CR7-CR5 to 011 or 110.

16-Bit color mode
2LSB = set to zero (green)
3LSB = set to zero (blue, red)

SECOND BYTE								FIRST BYTE							
P 7	P 6	P 5	P 4	P 3	P 2	P 1	P 0	P 7	P 6	P 5	P 4	P 3	P 2	P 1	P 0
7	6	5	4	3	7	6	5	4	3	2	7	6	5	4	3
RED					GREEN						BLUE				

Mode 3: (24-bit per pixel True Color Mode).
This mode is the 24-bit per pixel bypass mode. The three bytes of data are latched on three successive PCLK edges and the first byte is synchronized by the rising edge of BLANK*. In this mode, each of the colors are 8-bit wide and the DAC is an 8-bit wide DAC. The first byte is blue followed by green and red. This mode can be selected by setting bits CR7-CR5 to 010 or 111. The DAC outputs changes every three cycles and the pipeline delay from the first byte to output is five cycles.

24-bit color mode

THIRD BYTE								SECOND BYTE								FIRST BYTE							
P 7	P 6	P 5	P 4	P 3	P 2	P 1	P 0	P 7	P 6	P 5	P 4	P 3	P 2	P 1	P 0	P 7	P 6	P 5	P 4	P 3	P 2	P 1	P 0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RED								GREEN								BLUE							

Frequency Generators

The ICS5300 clock synthesizer can be reprogrammed through the microprocessor interface for any set of frequencies. This is done by writing appropriate values to the PLL Parameter Register Bank (table 5).

PLL Address Registers

The address of the parameter register is written to the PLL address registers before accessing the parameter register. This register is accessed by register select pins RS2-RS0 = 100 or 111.

7	6	5	4	3	2	1	0
PLL REGISTER ADDRESS							
7	6	5	4	3	2	1	0

PLL Parameter Register

There are sixteen registers in the PLL parameter register (table 5). Registers 00 to 07 are for the CLK0 selectable frequency list, Register 0A for CLK1 programmable frequency and register 0E is the PLL CLK0 control register.

Index	R/W	Register	
00	R/-	CLK0 f0 PLL Parameters	(2 bytes)
01	R/-	CLK0 f1 PLL Parameters	(2 bytes)
02	R/W	CLK0 f2 PLL Parameters	(2 bytes)
03	R/W	CLK0 f3 PLL Parameters	(2 bytes)
04	R/W	CLK0 f4 PLL Parameters	(2 bytes)
05	R/W	CLK0 f5 PLL Parameters	(2 bytes)
06	R/W	CLK0 f6 PLL Parameters	(2 bytes)
07	R/W	CLK0 f7 PLL Parameters	(2 bytes)
08	R/-	(Reserved) = 0	(2 bytes)
09	R/-	(Reserved) = 0	(2 bytes)
0A	R/W	CLK1fA PLL	(2 bytes)
0B	R/-	(Reserved) = 0	(2 bytes)
0C	R/-	(Reserved) = 0	(2 bytes)
0D	R/-	(Reserved) = 0	(2 bytes)
0E	R/W	PLL Control Register	(1-byte)
0F	R/-	(Reserved) = 0	(2-byte)

Table 5 - PLL Parameter Registers

PLL Control Register

Bits in this register determine internal or external CLK0 select.

7	6	5	4	3	2	1	0
(RV)	(RV)	ENBL	(RV)	(RV)	INTERNAL SELECT		
=0	=0	INCS	=0	=0	X	X	X

Bit 7 - 6 Reserved.

Bit 5 Enable Internal Clock Select (INCS) for CLK0. When this bit is set to 1, the CLK0 output frequency is selected by bit 2 - 0 in this register. External pins CS0 - CS2 are ignored.

Bit 4 - 3 (Reserved).

Bit 2 - 0 Internal Clock Select for CLK0 (INCS). These three bits selects the CLK0 output frequency if bit 5 of this register is on. They are interpreted as an octal number, n, that selects fn. Default selects f0.

PLL Data Registers

The CLK0 and CLK1 input frequency is determined by the parameter values in this register. These are two bytes registers; the first byte is the M-byte and the second is the N-byte.

M-Byte PLL Parameter Input

The M-byte has a 7-bit value (1-127) which is the feedback divider of the PLL.

7	6	5	4	3	2	1	0
Reserved	M-Divider Value						
=0	X	X	X	X	X	X	X

N-Byte PLL Parameter Input

The N-byte has two values. N1 sets a 5-bit value (1-31) for the input pre scalar and N2 is a 2-bit code for selecting 1, 2, 4, or 8 post divide clock output.

7	6	5	4	3	2	1	0
Reserved	N2-Code		N1-Divider Value				
=0	X	X	X	X	X	X	X

N2 Post Divide Code

N2 code	Divider
00	1
01	2
10	4
11	8

The block diagram of the PLL clock synthesizer is given in following figure 3.

Based on the M and N values, the output frequency of the clocks is given by the following equation:

$$F_{out} = \frac{(M+2) \times F_{ref}}{(N1+2) \times 2^{N2}}$$

M and N values should be programmed such that the frequency of the VC0 is within the optimum range for duty cycle, jitter and glitch free transition. Optimum duty cycle is achieved by programming N2 for values greater than one. See the following page for programming example.

Programming Example

Suppose an output frequency of 25.175 MHz is desired. The reference crystal is 14.318 MHz. The VCO should be targeted to run in the 100 to 180 MHz range, so choosing a post divide of 4 gives a VCO frequency of :

4 X 25.175=101.021 MHz

From the table on page 17, we find N2 = 2
Substituting $F_{ref} = 14.318$ and $2^{N2} = 4$ into the equation on page 17:

$$\left(\frac{25.175}{14.318}\right) \cdot 4 = \frac{(M+2)}{(N1+2)}$$

by trial and error:

$$\left(\frac{25.175}{14.318}\right) \cdot 4 \approx \frac{127}{18}$$

so $M + 2 = 127$ $\quad M = 125$
$N1 + 2 = 18$ $\quad N1 = 16$

so the registers are:

M = 125d = 1 1 1 1 1 0 1 b
N = 0 & N2 code & N1 = 0 & 1 0 & 1 0 0 0 0
N = 0 1 0 1 0 0 0 0 b

Additional Information on Programming the Frequency Generator section of the GENDAC

When programming the GENDAC PLL parameter registers, there are many possible combinations of parameters which will give the correct output frequency. Some combinations are better than others, however. Here is a method to determine how the registers need to be set:

The key guidelines come from the operation of the phase locked loop, which has the following restrictions:

1. $2 \text{ MHz} < f_{REF} < 32 \text{ MHz}$
   This refers to the input reference frequency. Most users simply connect a 14.318 MHz crystal to the crystal inputs, so this is not a problem.

2. $600 \text{ kHz} < \frac{f_{REF}}{(N1+2)} \leq 8 \text{ MHz}$
   This is the frequency input to the phase detector.

3. $60 \text{ MHz} \leq \frac{(M+2)}{(N1+2)} f_{REF} \leq 270 \text{ MHz}$
   This is the VCO frequency. In general, the VCO should run as fast as possible, because it has lower jitter at higher frequencies. Also, running the VCO at multiples of the desired frequency allows the use of output divides, which tends to improve the duty cycle.

4. f_{CLK0} and $f_{CLK1} \leq 135$ MHz
   This is the output frequency.

These rules lead to the following procedure for determining the PLL parameters, assuming rules 1 and 4 are satisfied.

A. Determine the value of N2 (either 1, 2, 4 or 8) by selecting the highest value of N2, which satisfies the condition
$N2^{*} f_{CLK} \leq 270$ MHz

B. Calculate $\frac{(M2+)}{(N1+2)} = \frac{2^{N2} f_{out}}{fref}$

C. Now (M+2) and (N1+2) must be found by trial and error. With a 14.318 MHz reference frequency, there will generally be a small output frequency error due to the resolution limit of (M+2) and (N1+2). For a given frequency tolerance, several different (M+2) and (N1+2) combinations can usually be found. Usually, a few minutes trying out numbers with a calculator will produce a workable combination. Multiplying possible values of (N1+2) by the desiredratio will indicate approximately the value of M. This method is shown in the example below. A program could be written to try all possible combinations of (M+2) and (N1+2) (3937 possible combinations), discard those outside error band, and select from those remaining by giving preference to ratios which use lower values of (M+2). Lower values of (M+2) and (N1+2) provide better noise rejection in the phase locked loop.

Example: Suppose we are using a 14.318 MHz reference crystal and wish to output a frequency of 66 MHz with an error of no greater than 0.5%. What are the values of the PLL data registers?

A. 66*8 = 528 > 250 VCO speed too high
66*4 = 264 > 250 VCO speed too high
66*2 = 132 < 250 VCO speed OK, N2 = 2, N2 code = 01 from table on page 17 of the data sheet.

B. 132/14.31818 = 9.219
This is the desired frequency multiplication ratio.

C. Setting (N1+2) = 3, 4,...12, 13 and performing some simple calculations yields the following table: (Note that N1 cannot be 0)

(N1+2)	(N1+2)*9.219	rounded (=M+2)	Actual Ratio	Percent Error
3	27.657	28	9.33	-1.23
4	36.876	37	9.25	-0.34
5	46.095	46	9.20	0.21
6	55.314	55	9.17	0.57
7	64.533	65	9.29	-0.72
8	73.752	74	9.25	-0.34
9	82.971	83	9.22	-0.03
10	92.19	92	9.20	0.21
11	101.409	101	9.18	0.40
12	110.628	111	9.25	-0.34
13	119.847	120	9.23	-0.13

The ratio 83/9 is closest. Thus (N2+2) = 9; N2=7. (M+2) = 83; M = 81. The M-byte PLL parameter word is simply 81 in binary, plus bit 7 (which must be set to 0), or 01010001. The N-byte PLL parameter word is N2 code (01) concatenated with 5 bits of N2 in binary (00111), or 00100111. Once again, bit 7 must be zero.

We have chosen the combination with the least frequency error, but several other combinations are within the 0.5% tolerance. Because the lowest value of (M+2) offers the best damping, the 37/4 combination will have the best power supply rejection. This results in lower jitter due to external noise.

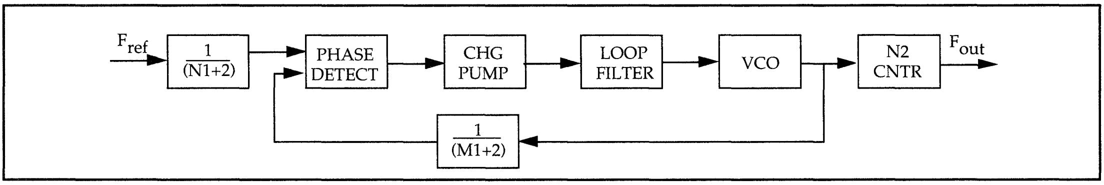
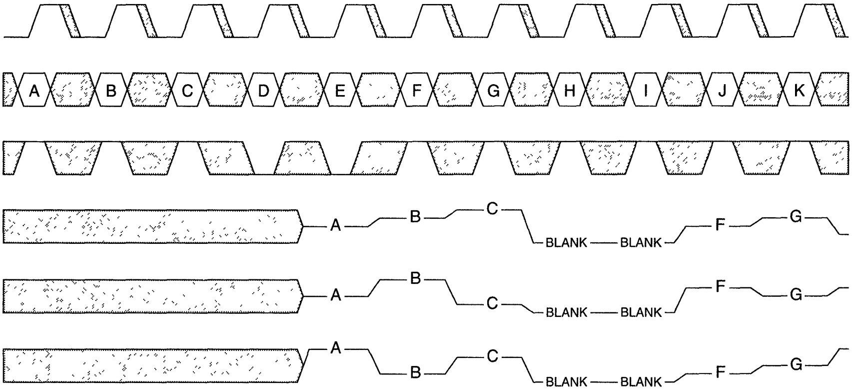


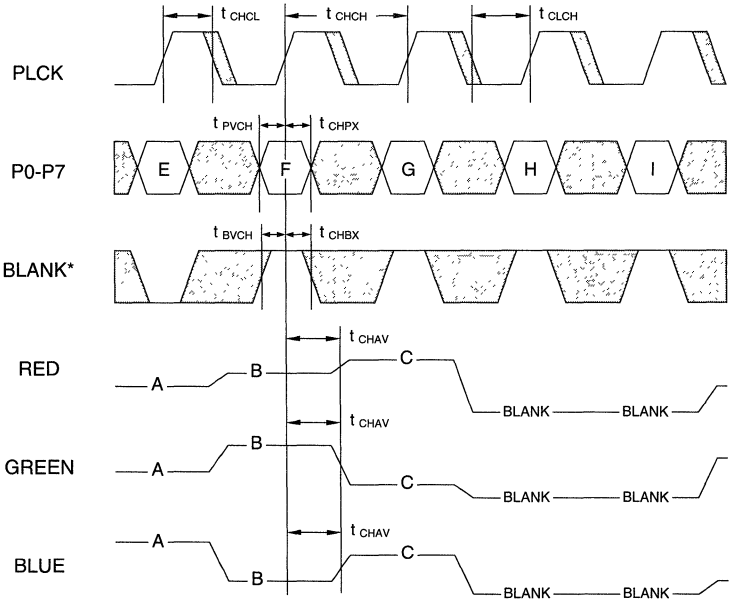
Figure 3 - PLL Clock Synthesizer Block Diagram

External Select			(Internal Select PLL Control Register)			
CS2	CS1	CS0	BIT 2	BIT 1	BIT 0	CLK 0 Frequency
0	0	0	0	0	0	f0
0	0	1	0	0	1	f1
0	1	0	0	1	0	f2
0	1	1	0	1	1	f3
1	0	0	1	0	0	f4
1	0	1	1	0	1	f5
1	1	0	1	1	0	f6
1	1	1	1	1	1	f7

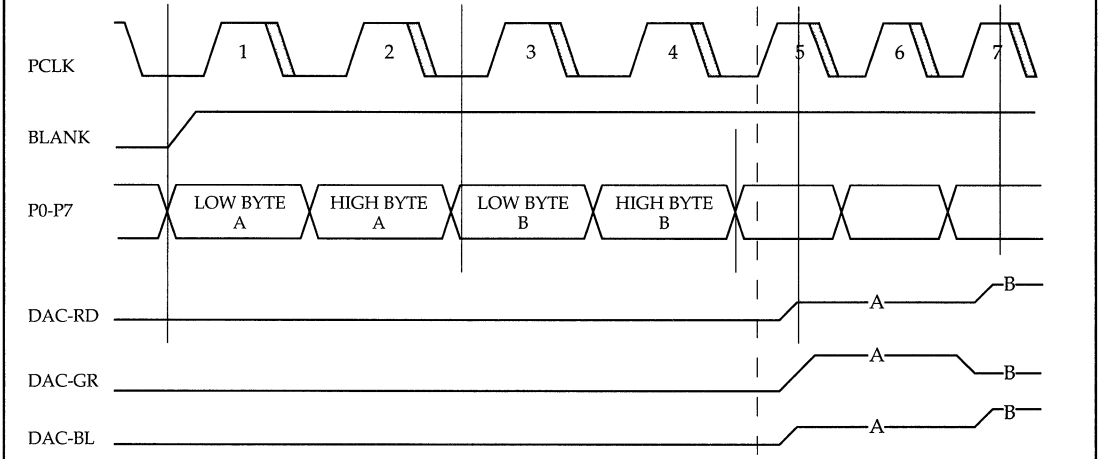
Video Clock Selection Table



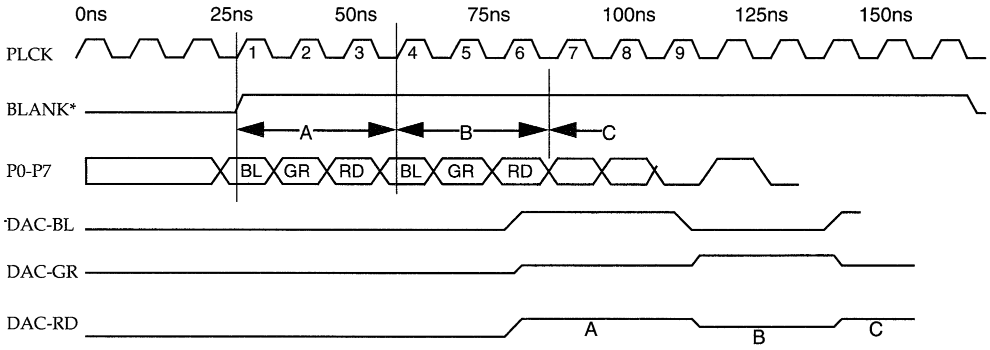
System Timing - Pseudo Color, Mode 0



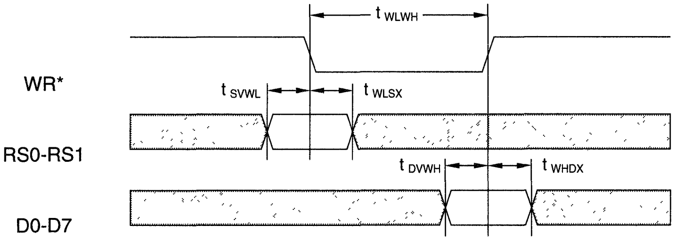
Detailed Timing Specifications - Pseudo Color, Mode 0



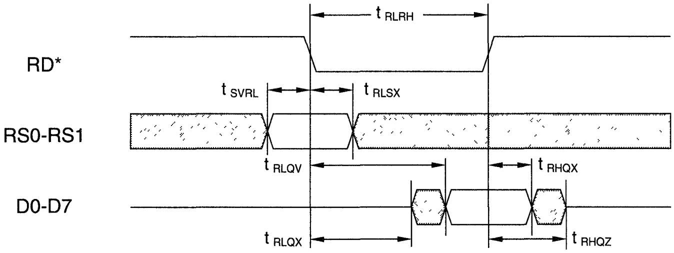
System Timing Bypass - 15 (5/5/5) and 16 (5/6/5) Modes 1, 2



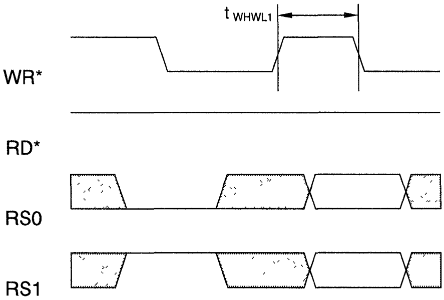
System Timing Bypass True Color 24 (8,8,8) Mode 3



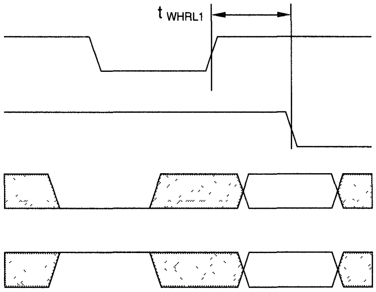
Basic Write Cycle Timing



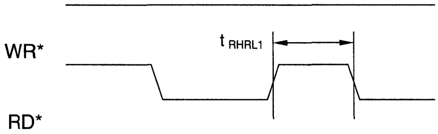
Basic Read Cycle Timing



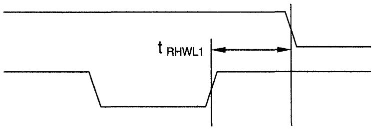
Write to Pixel Mask Register Followed by Write



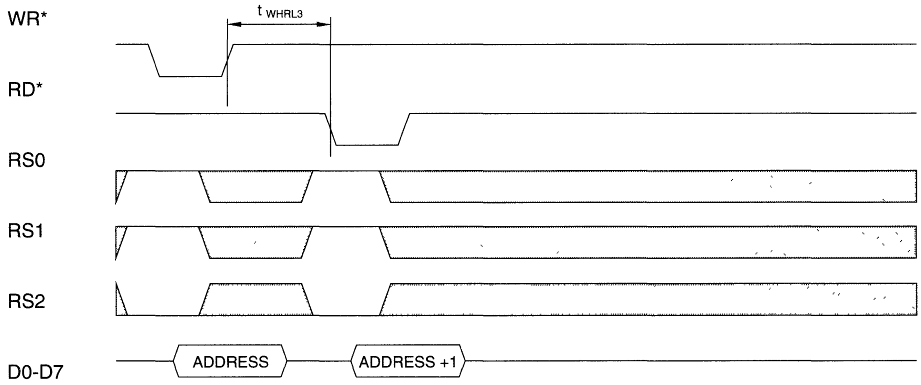
Write to Pixel Mask Register Followed by Read



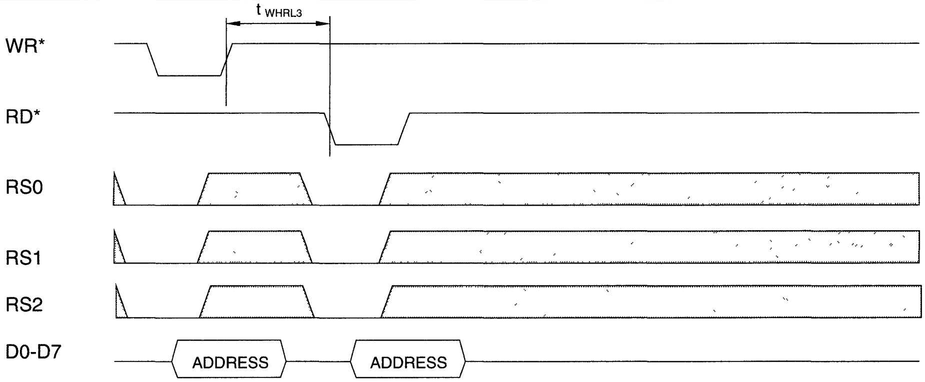
Read from Pixel or Pixel Address Register (Read or Write) followed by Read



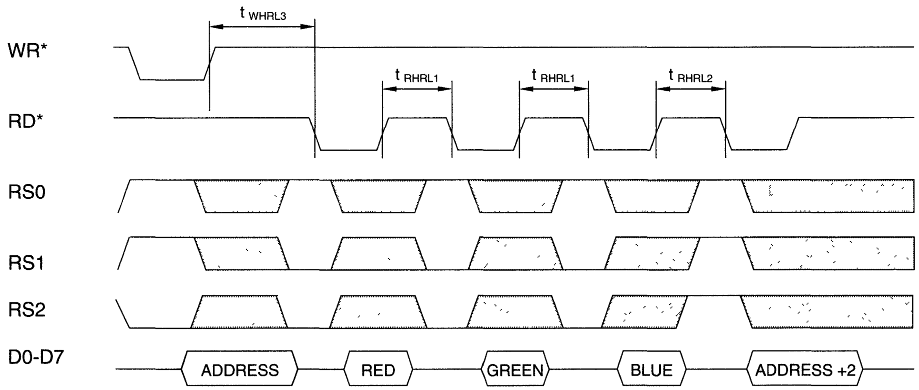
Read from Pixel or Pixel Address Register (Read or Write) followed by Write



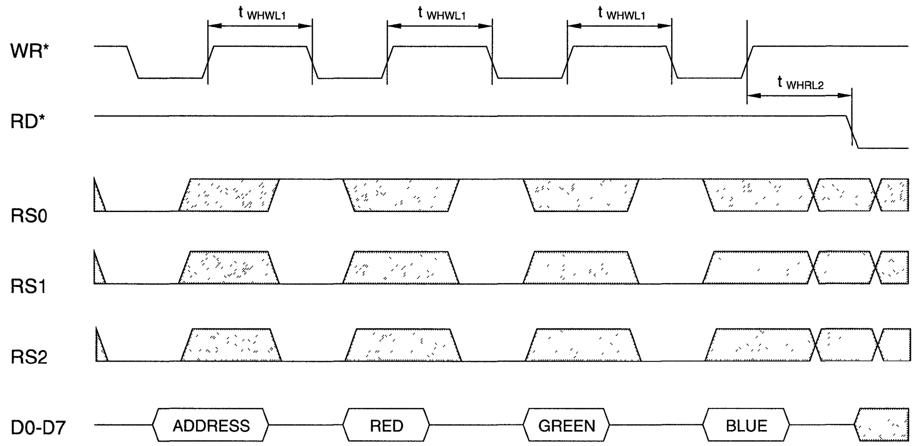
Write and Read Back Pixel Address Register (Read Mode)



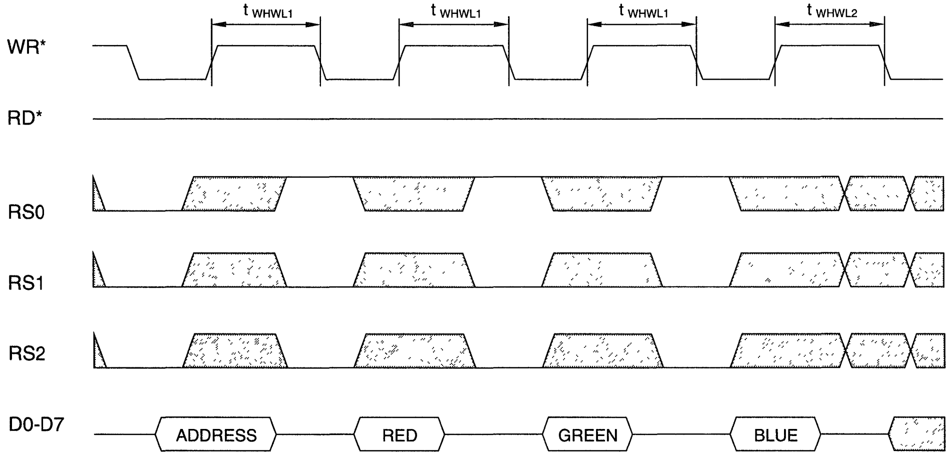
Write and Read Back Pixel Address Register (Write Mode)



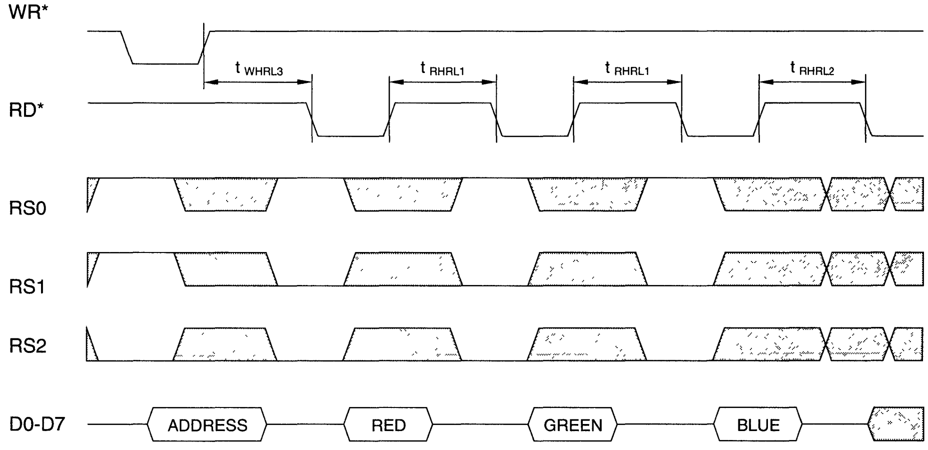
Read Color Value then Pixel Address Register (Read Mode)



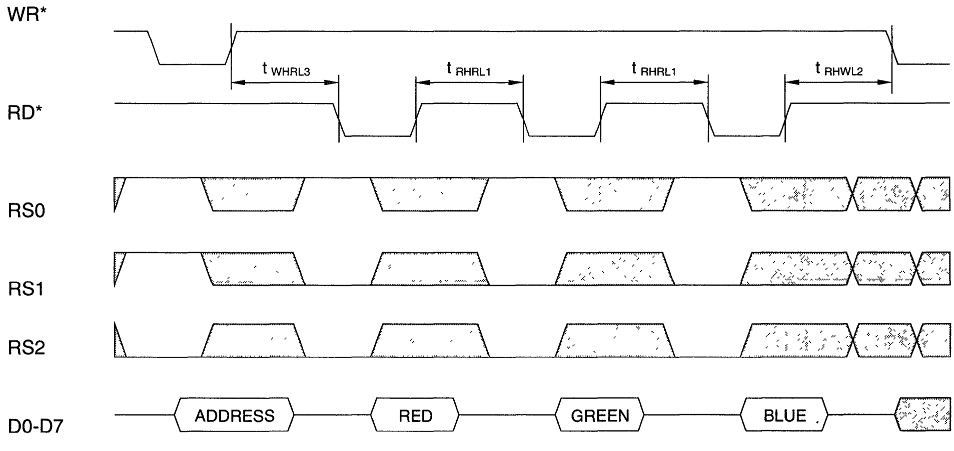
Color Value Write followed by any Read



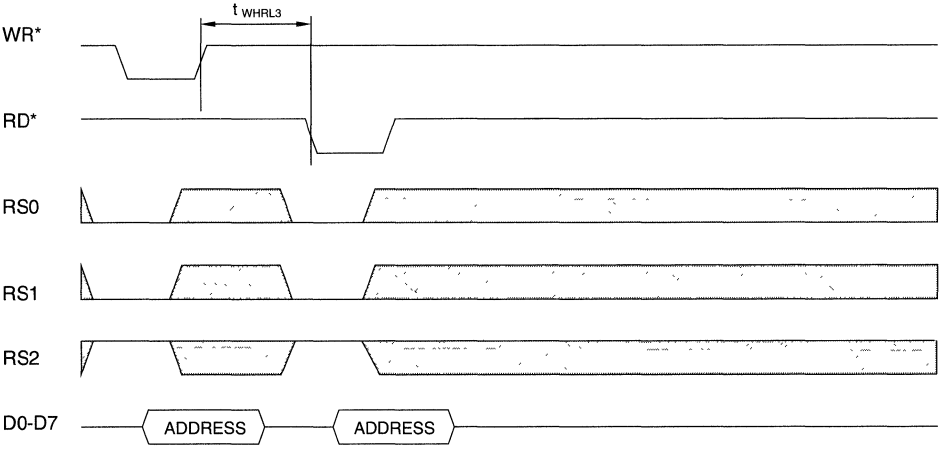
Color Value Write followed by any Write



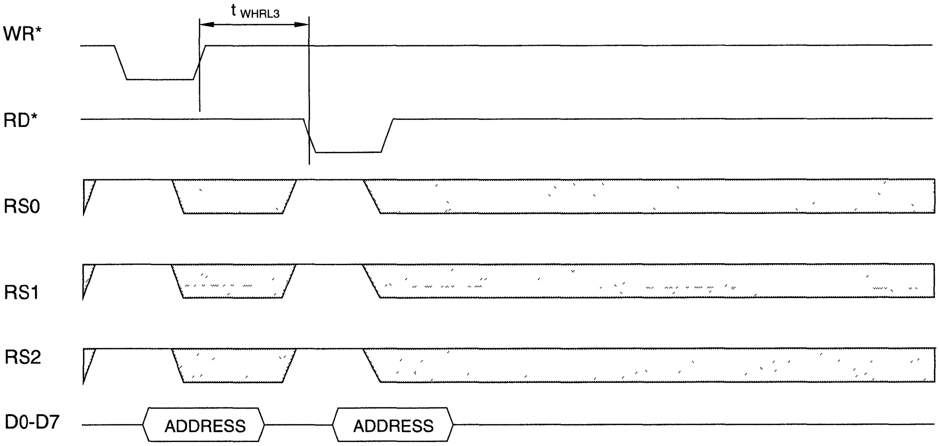
Color Value Read followed by any Read



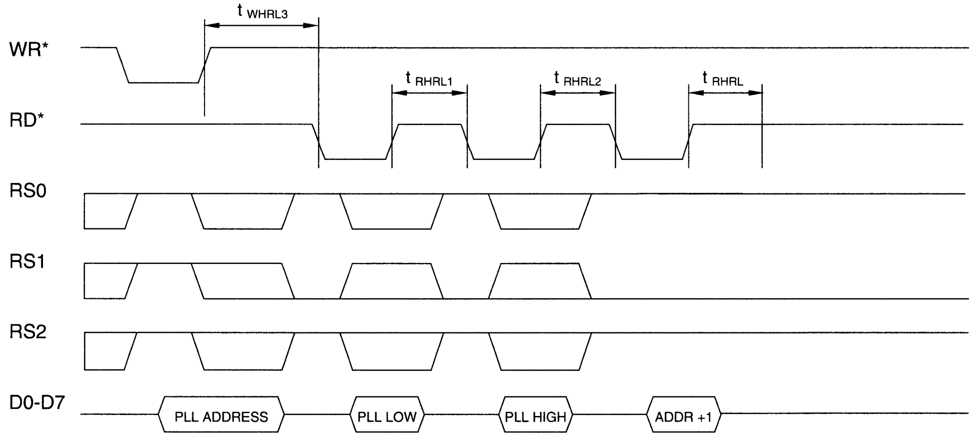
Color Value Read followed by any Write



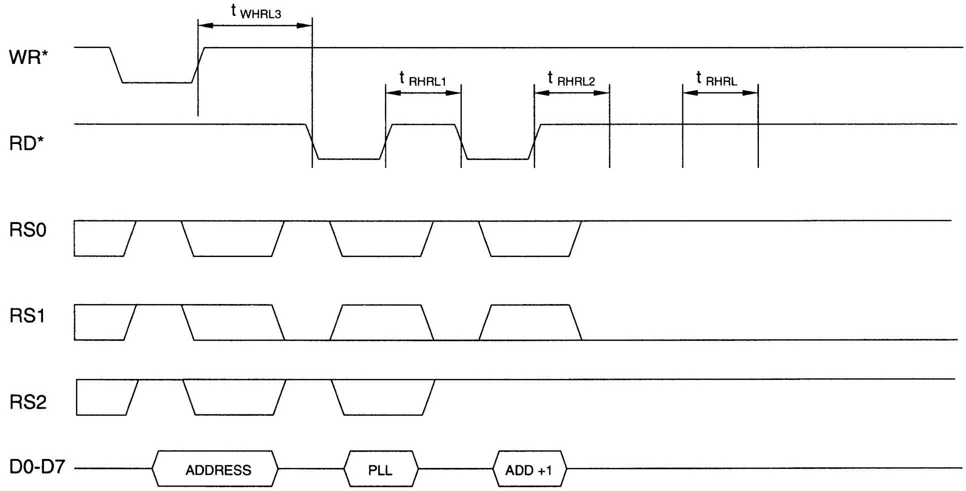
Write and Read back PLL Address Register (Write Mode)



Write and Read back PLL Address Register (Read Mode)

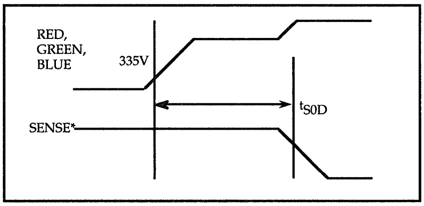


Read Two bytes PLL Register then PLL Address Register



Read One Byte PLL Register then PLL Address Register

Monitor SENSE Signal

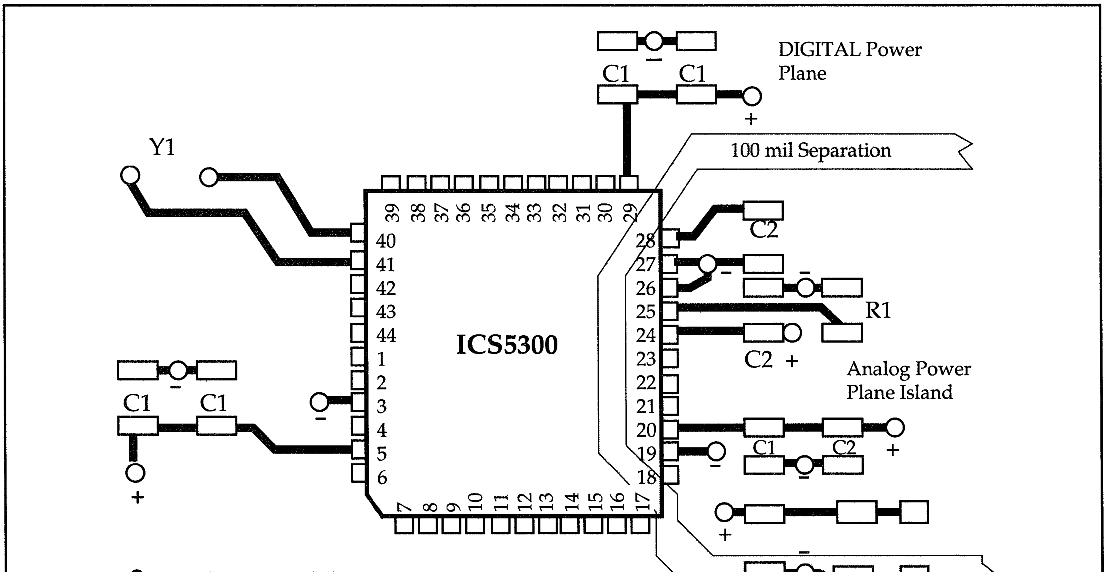


The high performance of which the ICS5300 GENDAC is capable is dependent on careful PC board layout. The use of a four layer board (internal power and ground planes, signals on the two surface layers) is recommended. The layout below shows a suggested configuration.

The ground plane is continuous, but the power plane is separated into analog and digital sections as shown. Power is supplied to the analog power plane through the ferrite bead, and bypassed at the power entry point by C3, a 10 µF tantalum capacitor. These high current connections should have multiple vias to the ground and power planes, if possible. Power connections should be connected to the analog or digital power plane, as shown in the diagram. Power pins 5 and 29 should be connected to digital power, power pins 20 and 24 to analog power. Decoupling capacitors (indicated by C1) should be placed as close to the GENDAC as possible.

The analog and digital I/O lines are not shown. Analog signals (DAC outputs, Vref, Rset) should only be routed above the analog power plane. Digital signals should only be routed above the digital power plane.

Recommended Layout



○ -	VIA to ground plane
○ +	VIA to power plane
C1	,01uf chip capacitor
C2	,1uf chip capacitor
C3	10uf tantulum capacitor
FB1	Ferrite Bead
R1	140 ohm 1% resistor
Y1	14.318 Mhz parallel resonant crysal cut for C $_L$=12

Ordering Information

ICS5300V

Example:

ICS XXXX M

Package Type
V=PLCC
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated Circuit Systems, Inc.

ICS5301
GENDAC

8-Bit Integrated Clock-LUT-DAC

General Description

The ICS5301 GENDAC is a combination of dual programmable clock generators, a 256 x 18-bit RAM, and a triple 8-bit video DAC. The GENDAC supports 8-bit pseudo color applications, as well as 15-bit, 16-bit and 24-bit True Color bypass for high speed, direct access to the DACs.

The RAM makes it possible to display 256 colors selected from a possible 262,144 colors. The dual clock generators use Phase Locked Loop (PLL) technology to provide programmable frequencies for use in the graphics subsystem. The video clock contains 8 frequencies, 6 of which are programmable by the user. The memory clock has one programmable frequency location.

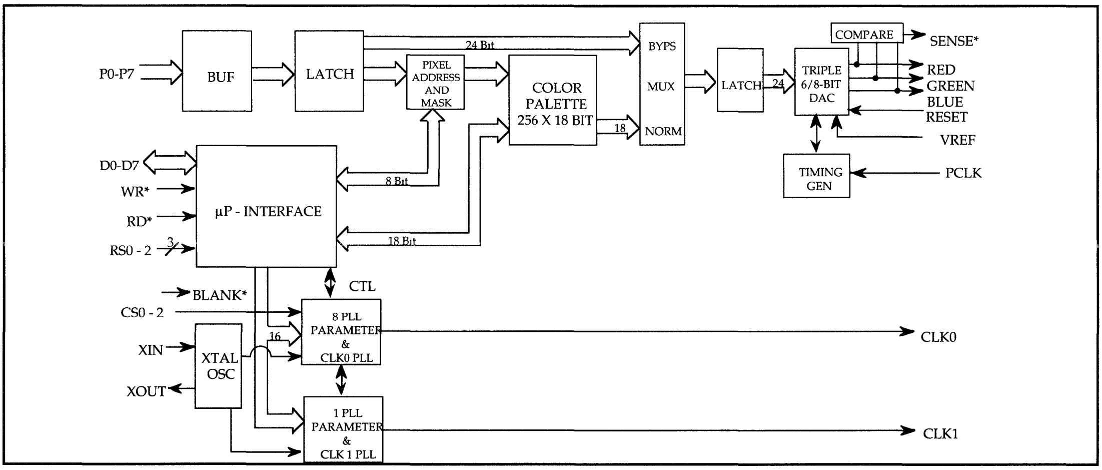
The three 8-bit DACs on the ICS5301 are capable of driving singly or doubly-terminated 75Ω loads to nominal 0 - 0.7 volts at pixel rates up to 135 MHz. Differential and integral linearity errors are less than 1 LSB over full temperature and V_{DD} ranges. Monotonicity is guaranteed by design. On-chip pixel mask register allows displayed colors to be changed in a single write cycle rather than by modifying the color palette.

ICS is the world leader in all aspects of frequency (clock) generation for graphics, using patented techniques to produce low jitter video timing.

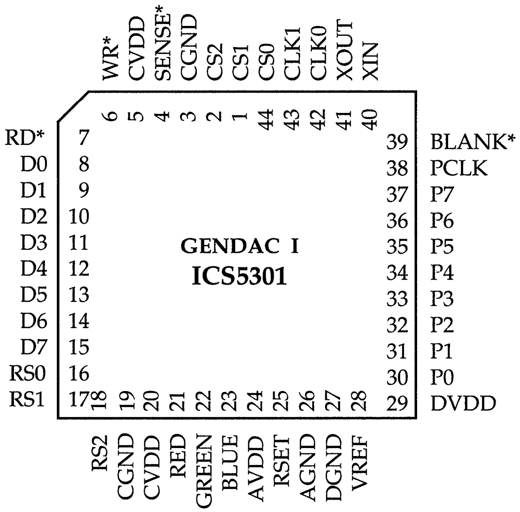
Features

- **Designed for compatibility with Tseng Labs VGA controllers**
- **Triple video DAC, dual clock generator, and a color palette**
- **24, 16, 15, or 8-bit pseudo color pixel mode supports True Color, Hi-Color, and VGA modes**
- **High speed 256 x 18 color palette (135 MHz) with bypass mode and 8-bit DACs**
- **Two fixed, six programmable video (pixel) clock frequencies (CLK0)**
- **One programmable memory (controller) clock frequency (CLK1)**
- **DAC power down in blanking mode**
- **Low power operation**
- **Anti-sparkle circuitry**
- **On-chip loop filters reduce external components**
- **Standard CPU interface**
- **Single external crystal (typically 14.318 MHz)**
- **Monitor Sense**
- **Internal voltage reference**
- **135 MHz (-3), 110 MHz (-2) & 80 MHz (-1) versions**
- **Very low clock jitter**

Block Diagram



Pin Configuration



Pin Description (68 pin PLCC) K-10

Symbol	Pin #	Type	Description
CS1	1	Input	Clock select 1. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output.
CS2	2	Input	Clock select 2. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output.
CGND	3	-	Ground for clock circuits. Connect to ground.
SENSE*	4	Output	Monitor Sense, active low. This pin is low when any of the red, green, or blue outputs have exceeded 335mV. The chip has on-board comparators and an internal 335mV voltage reference. This is used to detect monitor type.
CVDD	5	-	Clock Power Supply. Connect to DVDD
WR*	6	Input	RAM/PLL Write Enable, active low. This signal controls the timing of the write operation on the microprocessor interface inputs, D0-D7.
RD*	7	Input	RAM/PLL Read Enable, active low. This is the READ bus control signal. When active, any information present on the internal data bus is available on the Data I/O lines, D0-D7.
D0 - D7	8 - 15	I/O	System data bus I/O. These bidirectional Data I/O lines are used by the host microprocessor to write (using active low WR*) information into, and read (using active low RD*) information from the six internal registers (Pixel Address, Color Value, Pixel Mask, PLL Address, PLL Parameter, and Command). During the write cycle, the rising edge of WR* latches the data into the selected register (set by the status of the three RS pins). The rising edge of RD* determines the end of the read cycle. When RD* is a logical high, the Data I/O lines no longer contain information from the selected register and will go into a tri-state mode.

Pin Description (continued)

Symbol	Pin #	Type	Description
RS0 RS1 RS2	16 17 18	Input Input Input	Register Address Select 0. These inputs control the selection of one of the six internal registers. They are sampled on the falling edge of the active enable signal (RD* or WR*).
CGND	19	-	Ground for clock circuits. Connect to ground.
CVDD	20	-	Clock Power Supply. Connect to AVDD.
RED GREEN BLUE	21 22 23	Output Output Output	Color Signals. These three signals are the DACs' analog outputs. Each DAC is composed of several current sources. The outputs of each of the sources are added together according to the applied binary value. These outputs are typically used to drive a CRT monitor.
AVDD	24	-	Analog power supply. Connect to AVDD.
RSET	25	Input	Resistor Set. This pin is used to set the current level in the analog outputs. It is usually connected through a 140Ω, 1% resistor to ground.
AGND	26	-	Analog Ground. Connect to ground.
DGND	27	-	Digital Ground. Connect to ground.
VREF	28	Input	Internal Reference Voltage. Normally connects to a 0.1μF cap to ground. To use an external Vref, connect a 1.235V reference to this pin.
DVDD	29	-	Digital power supply.
P0 - P7	30 - 37	Input	Pixel Address Lines. This byte-wide information is latched by the rising edge of PCLK when using the Color Palette, and is masked by the Pixel Mask register. These values are used to specify the RAM word address in the default mode (accessing RAM). In the Hi-Color XGA, and True Color modes, they represent color data for the DACs. These inputs should be grounded if they are not used.
PCLK	38	Input	Pixel Clock. The rising edge of PCLK controls the latching of the Pixel Address and BLANK* inputs. This clock also controls the progress of these values through the three-stage pipeline of the Color Palette RAM, DAC, and outputs.
BLANK*	39	Input	Composite BLANK* Signal, active low. When BLANK* is asserted, the outputs of the DACs are zero and the screen becomes black. The DACs are automatically powered down to save current during blanking. The color palette may still be updated through D0-D7 during blanking.
XIN	40	Input	Crystal input. A 14.318 MHz crystal should be connected to this pin.
XOUT	41	Output	Crystal output. A 14.318 MHz crystal should be connected to this pin.
CLK0	42	Output	Video clock output. Provides a CMOS level pixel or dot clock frequency to the graphics controller. The output frequency is determined by the values of the PLL registers.
CLK1	43	Output	Memory clock output. Used to time the video memory.
CS0	44	Input	Clock select 0. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output.

Internal Registers

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
				There is a single Pixel Address register within the GENDAC. This register can be accessed through either register address 0,0,0 or register address 0,1,1. A read from address 0,0,0 is identical to a read from address 0,1,1. Writing a value to address 0,0,0 performs the following operations: a) Specifies an address within the color palette RAM. b) Initializes the Color Value register. Writing a value to address 0,1,1 performs the following operations: a) Specifies an address within the color palette RAM. b) Loads the Color Value register with the contents of the location in the addressed RAM palette and then increments the Pixel Address register.
0	0	0	Pixel Address WRITE	Writing to this 8-bit register is performed prior to writing one or more color values to the color palette RAM.
0	1	1	Pixel Address READ	Writing to this 8-bit register is performed prior to reading one or more color values from the color palette RAM.
0	0	1	Color Value	The 18-bit Color Value register acts as a buffer between the microprocessor interface and the color palette. Using a three bytes transfer sequence allows a value to be read from or written to this register. When a byte is read, the color value is contained in the least significant 6 bits, D0-D5 (the most significant 2 bits are set to zero). When writing a byte, the same 6 bits are used. When reading or writing, data is transferred in the same order - the red byte first, then green, then blue. Each transfer between the Color Value register and the color palette replaces the normal pixel mapping operations of the GENDAC for a single pixel. After writing three definitions to this register, its contents are written to the location in the color palette RAM specified by the Pixel Address register, and the Pixel Address register increments. After reading three definitions from this register, the contents of the location in the color palette RAM specified by the Pixel Address registers are copied into the Color Value register, and the Pixel Address register increments.
0	1	0	Pixel Mask	The 8-bit Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P0-P7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, while a zero sets that bit to zero. The Pixel Mask register does not affect the Pixel Address generated by the microprocessor interface when the palette RAM is being accessed.

Internal Registers (continued)

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
1	0	0	PLL Address WRITE	Writing to this 8-bit register is performed prior to writing one or more PLL programming values to the PLL Parameter register.
1	1	1	PLL Address READ	Writing to this 8-bit register is performed prior to reading one or more PLL programming values from the PLL Parameter register.
1	1	0	Command	This 8-bit register selects the color mode, for instance 8-bit Pseudo Color, Hi-Color, True Color, or XGA, and DAC power down. The registers are reset to pseudo color mode on power up.
1	0	1	PLL Parameter	There are sixteen parameter registers as indexed by PLL Address Write/ Readregisters. Parameter registers 00-0D and 0F are two bytes long and 0E is one byte long. This register set contains one control register. The bits of this register include clock select and enable functions, the rest contain PLL frequency parameters. After writing the start index address in the PLL address register, these registers can be accessed in successive two (or one) bytes. The address register auto increments after one or two bytes to access the entire register set.

Absolute Maximum Ratings

Power Supply Voltage	7 V
Voltage on any other pin	GND – 0.5V to V_{DD} + 0.5V
Temperature under bias	– 40° C to 85° C
Storage Temperature	– 65° C to 150° C
DC Digital Output Current	25 mA
Analog Output Current	45 mA
Reference Current	–15 mA
Power Dissipation	1.0 W

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
DC CHARACTERISTICS (note: J)					
V_{DD}	Positive supply voltage		4.75	5.25	V
V_{IH}	Input logic "1" voltage		2.0	V_{DD} + 0.5	V
V_{IL}	Input logic "0" voltage		- 0.5	0.8	V
I_{REF}	Reference current		–7.0	–10	mA
V_{REF}	Reference voltage		1.10	1.35	V
I_{IN}	Digital input current	V_{DD} = max, GND ≤ V_{IN} ≤ V_{DD}		± 10	µA
I_{OZ}	Off-state digital output current	V_{DD} = max, GND ≤ V_{IN} ≤ V_{DD}		± 50	µA
I_{DD}	Average power supply current	I_O = max, Digital outputs unloaded		250	mA
I_{DACOFF}	DACs in power down mode	No palette access		50	mA
V_{OH}	Output logic "1"	I_O = –3.2mA, note K	2.4		V
V_{OL}	Output logic "0"	I_O = -3.2mA, note K		0.4	V
$ICLK_r$	Input Clock Rise Time	TTL levels		15	ns
$ICLK_f$	Input Clock Fall Time	TTL levels		15	ns
F_D	Frequency Change of CLK0 and CLK1 over supply and temperature	With respect to typical frequency		0.05	%

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Units
DAC CHARACTERISTICS (note: J)					
V_O (max)	Maximum output voltage	$I_O \le 10$ mA		1.5	V
I_O (max)	Maximum output current	$V_O \le 1$V		21	mA
	Full scale error	note A, B		± 5	%
	DAC to DAC correlation	note B		±2	%
	Integral Linearity, 6-bit	note B		±0.5	LSB
	Integral Linearity, 8-bit	note B		±1	LSB
	Full scale settling time*, 6-bit	note C		28	ns
	Full scale settling time*, 8-bit	note C		20	ns
	Rise time (10% to 90%)*	note C		6	ns
	Glitch energy*	note C		200	pVsec

* Characterized values only

Symbol	Parameter	Conditions	Min	Max	Units
PLL AC CHARACTERISTICS					
f_0	Clock 0 operating range		25	135	MHz
f_1	Clock 1 operating range		25	135	MHz
t_r	Output clocks rise time	25 pf load, TTL levels		1.5	ns
t_r	Output clocks fall time	25 pf load, TTL levels		1.5	ns
d_t	Duty Cycle		40/60	60/40	%
j_{1s}	Jitter, one sigma			130 ps	ps
j_{abs}	Jitter, absolute		-300 ps	300 ps	ps
f_{ref}	Input reference frequency	Typically 14.318 MHz	5	25	MHz

AC Electrical Characteristics (note: J)

Symbol	Parameter	Condition	80 MHz		110 MHz		135 MHz		Units
			Min	Max	Min	Max	Min	Max	
t_{CHCH}	PCLK period		12.5		9.09		7.4		ns
Δt_{CHCH}	PCLK jitter	note D		±2.5		+2.5			%
t_{CLCH}	PCLK width low		5		3.6		3		ns
t_{CHCL}	PCLK width high		5		3.6		3		ns
t_{PVCH}	Pixel word setup time	note E	3		3		2		ns
t_{CHPX}	Pixel word hold time	note E	3		2		1		ns
t_{BVCH}	BLANK* setup time	note E	3		3		2		ns
t_{CHBX}	BLANK* hold time	note E	3		2		1		ns
t_{CHAV}	PCLK to valid DAC output	note F		20		20		20	ns
Δt_{CHAV}	Differential output delay	note G		2		2		2	ns
t_{WLWH}	WR* pulse width low		50		50		50		ns
t_{RLRH}	RD* pulse width low		50		50		50		ns
t_{SVWL}	Register select setup time	Write cycle	10		10		10		ns
t_{SVRL}	Register select setup time	Read cycle	10		10		10		ns
t_{WLSX}	Register select hold time	Write cycle	10		10		10		ns
t_{RLSX}	Register select hold time	Read cycle	10		10		10		ns
t_{DVWH}	WR* data setup time		10		10		10		ns
t_{WHDX}	WR* data hold time		10		10		10		ns
t_{RLQX}	Output turn-on delay		5		5		5		ns
t_{RLQV}	RD* enable access time			40		40		40	ns
t_{RHQX}	Output hold time		5		5		5		ns
t_{RHQZ}	Output turn-off delay	note H		20		20		20	ns
t_{WHWL1}	Successive write interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHRL1}	WR* followed by read interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHRL1}	Successive read interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHWL1}	RD* followed by write interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHWL2}	WR* after color write	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHRL2}	RD* after color write	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHRL2}	RD* after color read	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{RHWL2}	WR* after color read	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{WHRL3}	RD* after read address write	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{SOD}	SENSE* output delay			1		1	1		µs

NOTES:

A. Full scale error is derived from design equation $\{[(F.S.I_{OUT})\ R_L - 2\ 1\ (I_{REF})\ R_L]/[2.1(I_{REF})R_L]\}\ 100\%$

$V_{BLACK\ LEVEL}=0V$ F.S I_{OUT} = Actual full scale measured output

B. R= 37 5Ω, I_{REF} = – 8.88mA

C. Z_I = 37.5Ω + 30 pF, I_{REF} = – 8.88mA

D. This parameter is the allowed Pixel Clock frequency variation. It does not permit the Pixel Clock period to vary outside the minimum values for Pixel Clock (t_{CHCH}) period

E. It is required that the color palette's pixel address be a valid logic level with the appropriate setup and hold times at each rising edge of P_{CLK} (this requirement includes the blanking period).

F. The output delay is measured from the 50% point of the rising edge of CLOCK to the valid analog output A valid analog output is defined when the analog signal is halfway between its successive values.

G This applies to different analog outputs on the same device.

H. Measured at ± 200 mV from steady state output voltage.

I. This parameter allows synchronization between operations on the microprocessor interface and the pixel stream being processed by the color palette.

J. The following specifications apply for V_{DD}= +5V± 0.5V, GND=0. Operating Temperature = 0°C to 70°C.

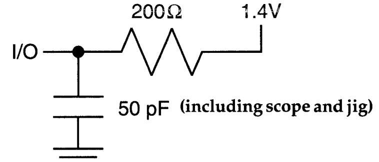
K Except for SENSE pin.

AC Test Conditions

Input pulse levels..V_{DD} to 3V
Input rise and fall times (10% to 90%)..........................3ns
Digital input timing reference level...........................1.5V
Digital output timing reference level........0.8V and 2.4V

Capacitance

C_I Digital input..7pF
C_0 Digital output...7pF
C_{0A} Analog output..10pF



DIGITAL OUTPUT LOAD

General Operation

The ICS5301 GENDAC is intended for use as the analog output stage of raster scan video systems. It contains a high-speed Random Access Memory of 256 x 18-bit words, three 6/8-bit high-speed DACs, a microprocessor/graphic controller interface, a pixel word mask, on-chip comparators, and two user programmable frequency generators.

An externally generated BLANK* signal can be applied to pin 39 of the ICS5301. This signal acts on all three of the analog outputs. The BLANK* signal is delayed internally so that it appears with the correct relationship to the pixel bit stream at the analog outputs.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the color palette RAM to facilitate such operations as animation and flashing objects. Operations on the contents of the mask register can also be totally asynchronous to the pixel stream.

The ICS5301 also includes dual PLL frequency generators providing a video clock (CLK0) and a memory clock (CLK1), both generated from a single 14.318 MHz crystal. There are eight selectable CLK0 frequencies of which six are programmable, and a single programmable CLK1 frequency. Default values (Table 1 and Table 2) are loaded into the appropriate registers on power up.

Video Path

The GENDAC supports four different video modes and is determined by bits 5-7 of the command register. The default mode is the 6-bit Pseudo Color mode. The other modes are the bypass 15-bit, 16-bit and 24 bit True Color.

Pseudo color

In this mode, Pixel Address and BLANK* inputs are sampled on the rising edge of the clock (PCLK) and any change appears at the analog outputs after three succeeding rising edges of the clock. The DAC outputs depends on the data in the color palette RAM.

Bypass Modes

The GENDAC supports three different bypass modes; 15-bit (5,5,5) mode, 16-bit (5,6,5) mode and the 24-bit True Color 8-bit DAC mode. In these modes, the pixel address pins P0-P7 represent the Color Data that is applied directly to the DAC. The internal RAM is bypassed. In the 15/16-bit mode two consecutive bytes contain the 15/16 bits of color data. Two consecutive rising edges of the PCLK latch the data on the P0-P7 pins into registers and the byte framing is internally synchronized with the rising edge of BLANK*. The internal pipe line delay from the "first byte" to the DAC is four PCLK rising edges. In the 24-bit True Color mode, three bytes contains the 24-bit color data. Three consecutive rising edges of the PCLK latch the data. The framing is the same as the 15/16-bit mode. The internal pipe line delay from the "first byte" to the DAC is five PCLK rising edges.

DAC Outputs

The outputs of the DACs are designed to be capable of producing 0.7 volt peak white amplitude with an I_{REF} of 8.88 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output load ($R_{EFFECTIVE}$) of 37.5Ω.

The formula for calculating I_{REF} with various peak white voltage/output loading combinations is given below:

$$I_{REF} = \frac{V_{PEAK\ WHITE}}{2.1 \times R_{EFFECTIVE}}$$

Note that for all values of I_{REF} and output loading:

$$V_{BLACK\ LEVEL} = 0$$

The reference current I_{REF} is determined by the reference voltage V_{REF} and the value of the resistor connected to R_{SET} pin. V_{REF} can be the internal band gap reference voltage or can be overridden by an external voltage. In both cases $I_{REF} = V_{REF}/R_{SET}$.

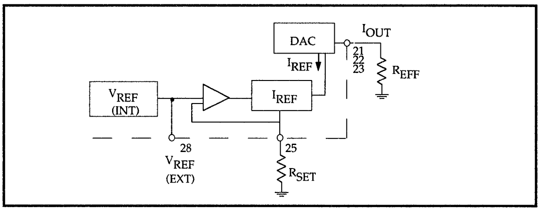


Figure 4 - DAC Set up

The BLANK* input to the GENDAC acts on all three of the DAC outputs. When the BLANK* input is low, the DACs are powered down.

The connection between the DAC outputs of the ICS5301 and the RGB inputs of the monitor should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor.

RF techniques should be observed to ensure good fidelity. The PCB trace connecting the GENDAC to the off-board connector should be sized to form a transmission line of the correct impedance. Correctly matched RF connectors should be used for connection from the PCB to the coaxial cable leading to the monitor and from the cable to the monitor.

There are two recommended methods of DAC termination: double termination and buffered signal. Each is described below with its relative merits:

Double Termination (Figure 1)
For this termination scheme, a load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line. Double termination of the DAC output allows both ends of the transmission line between the DAC outputs and the monitor inputs to be correctly matched. The result should be an ideal reflection free system. This arrangement is relatively tolerant to variations in transmission line impedance (e.g. a mismatched connector) since no reflections occur from either end of the line.

A doubly terminated DAC output will rise faster than any singly terminated output because the rise time of the DAC outputs is dependent on the RC time constant of the load.

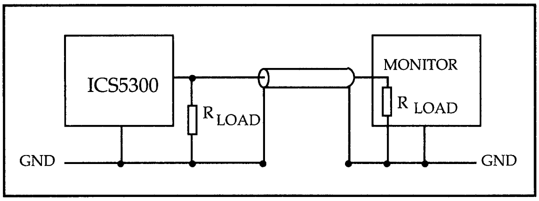


Figure 1 - Double Termination

Buffered Signal (Figure 2)
If the GENDAC drives large capacitive loads (for instance long cable runs), it may be necessary to buffer the DAC outputs. The buffer will have a relatively high input impedance. The connection between the DAC outputs and the buffer inputs should also be considered as a transmission line. The buffer output will have a relatively low impedance. It should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.

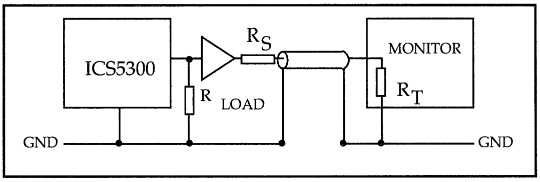


Figure 2 - Buffered Signal

SENSE Output

The GENDAC contains three comparators, one each for the DAC output (R, G and B) lines. The reference voltage to the comparators is proportional to the V_{REF} (internal or external) and is typically 0.33 for V_{REF} =1.23 Volts. When the voltage on any of these pins go higher than the reference voltage to the comparators, the SENSE* pin is driven low. This signal is used to detect the type of (or lack of) monitor connected to the system.

PLL Clock

The ICS5301 has dual PLL frequency generators for generating the video clock (CLK0) and memory clock (CLK1) needed for graphics subsystems. Both these clocks are generated from a single 14.318 MHz crystal or can be driven by an external clock source. The chip includes the capacitors for the crystal and all the components needed for the PLL loop filters, minimizing board component count.

There are eight possible video clock, CLK0, frequencies (f0-f7) which can be selected by the external pins CS0-CS2. Pins are software selectable by setting a bit in the PLL control register. Two of these frequencies (f0-f1) are fixed and the other six (f2-f7) can be programmed for any frequency by writing appropriate parameter values to the PLL parameter registers. The default frequencies on power up are commonly used video frequencies (table 1). At power up, the frequencies can be selected by pins CS0-CS2. There is only a single programmable memory clock frequency (CLK1). On power up this frequency defaults to the frequency given in table 2. The memory clock transition between frequencies is smooth and glitch free if the transition is kept between the limits 45-65 MHz.

fn	(MHz)	VLCK Comments
f0	50.350	VGA0 (VGA Color monitor) (fixed)
f1	56.644	VGA1 (VGA Monochrome monitor) (fixed)
f2	31.500	VESA 640 x 480 @72 Hz (programmable)
f3	36.00	VESA 800 x 600 @56 Hz (programmable)
f4	40.00	VESA 800 x 600 @60 Hz (programmable)
f5	44.889	1024 x 768 @43 Hz Interlaced (programmable)
f6	65.00	1024 x 768 @ 60 Hz, 640 x 480 Hi-Color @ 72 Hz (programmable)
f7	75.00	VESA 1024 x 768 @ 70 Hz, True Color 640 x 480 (programmable)

Table 1 - Video clock (CLK0) default frequency register (with a 14.318 MHz input)

MCLK (fA)	Comments
45.00 MHz	Memory and GUI subsystem clock Smooth transition between 45-65 MHz

Table 2 - Memory Clock (CLK1) Default Frequency Register

Microprocessor Interface

Below are listed the six microprocessor interface registers within the ICS5301, and the register addresses through which they can be accessed.

RS2	RS1	RS0	Register Name
0	0	0	Pixel Address (write mode)
0	1	1	Pixel Address (read mode)
0	0	1	Color Value
0	1	0	Pixel Mask
1	0	0	PLL Address (write mode)
1	0	1	PLL Parameter
1	1	0	Command
1	1	1	PLL Address (read mode)
0/HF	1	0	Command Register accessed by (hidden) flag after special sequence of events

Table 3 - Microprocessor Interface Registers

Asynchronous Access to Microprocessor Interface

Accesses to all registers may occur without reference to the high speed timing of the pixel bit stream being processed by the GENDAC. Data transfers between the color palette RAM and the Color Value register, as well as modifications to the Pixel Mask register, are synchronized to the Pixel Clock by internal logic. This is done in the period between microprocessor interface accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow the appropriate transfers or modifications to take place. Access to PLL address, PLL parameter and to the command register are asynchronous to the pixel clock.

The contents of the palette RAM can be accessed via the Color Value register and the Pixel Address registers.

Writing to the color palette RAM

To set a new color definition, a value specifying a location in the color palette RAM is first written to the Write mode Pixel Address register. The values for the red, green and blue intensities are then written in succession to the Color Value register. After the blue data is written to the Color Value register, the new color definition is transferred to the RAM, and the Pixel Address register is automatically incremented.

Writing new color definitions to a set of consecutive locations in the RAM is made easy by this auto-incrementing feature. First, the start address of the set of locations is written to the write mode Pixel Address register, followed by the color definition of that location. Since the address is incremented after each color definition is written, the color definition for the next location can be written immediately. Thus, the color definitions for consecutive locations can be written sequentially to the Color Value register without re-writing to the Pixel Address register each time.

Reading from the RAM

To read a color definition, a value specifying the location in the palette RAM to be read is written to the read mode Pixel Address register. After this value has been written, the contents of the location specified are copied to the Color Value register, and the Pixel Address register automatically increments.

The red, green and blue intensity values can be read by a sequence of three reads from the Color Value register. After the blue value has been read, the location in the RAM currently specified by the Pixel Address register is copied to the Color Value register and the Pixel Address again automatically increments. A set of color values in consecutive locations can be read simply by writing the start address of the set to the read mode Pixel Address register and then sequentially reading the color values for each location in the set. Whenever the Pixel Address register is updated, any unfinished color definition read or write is aborted and a new one may begin.

The Pixel Mask Register

The pixel address used to access the RAM through the pixel interface is the result of the bitwise ANDing of the

incoming pixel address and of the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colors without altering the video memory or the RAM contents. By partitioning the color definitions by one or more bits in the pixel address, such effects as rapid animation, overlays, and flashing objects can be produced.

The Pixel Mask register is independent of the Pixel Address and Color Value registers.

The Command Register

The Command register is used to select the various GENDAC color modes and to set the power down mode. On power up this register defaults to an 6-bit Pseudo Color mode. This register can be accessed by control pins RS2-RS0, or by a special sequence of events for graphics subsystems that do not have the control signal RS2. For graphic systems that do not have RS2, this pin is tied low and an internal flag (HF; Hidden Flag) is set when the pixel mask register is read four times consecutively. Once the flag is set, the following Read or Write to the pixel mask register is directed to the command register. The flag is reset for Read or Write to any register other than the pixel mask register. The sequence has to be repeated for any subsequent access to the command register.

The PLL Parameter Register

The CLK0 and CLK1 of the ICS5301 can be programmed for different frequencies by writing different values to the PLL parameter register bank. There are eight registers in the parameter register; seven are two bytes long and one (0E) is one byte long.

Writing to the PLL parameter register

To write the PLL parameter data, the corresponding address location is first written to the PLL address register. For software compatibility with other chips, two address registers are defined; the Write mode PLL address register and the Read mode PLL address register. They are actually a single Read/Write register in the ICS5301. The next PLL parameter write will be directed to the first byte of the address location specified by the PLL address register. The next Write to the parameter register will automatically be to the second byte of this register. At the end of the second Write the address is automatically incremented. For the one byte "0E" register the address location is incremented after the first byte Write. If this frequency is selected while programming, the output frequency will change at the end of the second Write.

Reading the PLL parameter register

To read one of the registers of the PLL parameter register the address value corresponding to the location is first written to the PLL address register. The next PLL parameter read will be directed to the first byte of the address location pointed by this index register. A next Read of the parameter register will automatically be the second byte of this register. At the end of the second Read, the address location is automatically incremented. The address register (0E) is incremented after the first byte Read.

Power Down Mode

When bit 0 in the Command register is high (set to 1), the GENDAC enters the DAC power down mode. The DACs are turned off, and the data is retained in the RAM. It is possible to access the RAM, in which case the current will temporarily increase. While the RAM is being accessed, the current consumption will be proportional to the speed of the clock. There is no effect on either clock generator while in this mode.

Power Supply

As a high speed CMOS device, the ICS5301 may draw large transient currents from the power supply, it is necessary to adopt high frequency board layout and power distribution techniques to ensure proper operation of the GENDAC. Please refer to the suggested layout on page 29.

To supply the transient currents required by the ICS5301, the impedance in the decoupling path should be kept to a minimum between the power supply pins V_{DD} and GND. It is recommended that the decoupling capacitance between V_{DD} and GND should be a $0.1\mu F$ high frequency capacitor, in parallel with a large tantalum capacitor with

a value between 22µF and 47µF. A ferrite bead may be added in series with the positive supply to form a low pass filter and further improve the power supply local to the GENDAC. It will also reduce EMI.

The combination of series impedance in the ground supply to the GENDAC, and transients in the current drawn by the device will appear as differences in the GND voltages to the GENDAC and to the digital devices driving it. To minimize this differential ground noise, the impedance in the ground supply between the GENDAC and the digital devices driving it should be minimized.

Digital Output Information

The PCB trace lines between the outputs of the TTL devices driving the GENDAC and the input to the GENDAC behave like low impedance transmission lines driven from a low impedance transmission source and terminated with a high impedance. In accordance with transmission line principles, signal transitions will be reflected from the high impedance input to the device. Similarly, signal transitions will be inverted and reflected from the low impedance TTL output. Line termination is recommended to reduce or eliminate the ringing, particularly the undershoot caused by reflections. The termination may either be series or parallel.

Series termination is the recommended technique to use. It has the advantages of drawing no DC current and of using fewer components. Series termination is accomplished by placing a resistor in series with the signal at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and ensures that any signal incident on the TTL output is not reflected.

To minimize reflections, some experimentation will have to be done to find the proper value to use for the series termination. Generally, a value around 100Ω will be required. Since each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. Therefore, the proper value of resistance should be found empirically.

Functional Description

This section describes the register address and bit definition for RAMDAC and the Frequency Synthesizer sections.

Color Palette

Command Register

(RS0-RS2 = 011)
(RS0-RS1 = 01 with hidden flag)

By setting bits in the command register the ICS5301 can be programmed for different color modes and can be powered down for low power operation.

7 6 5	4 3 2 1	0
Color Mode 2 1 0	Reserved Should all =0	Snooze

Table 3 - Command Registers

Bit 7-5 **Color Mode Select**
These three bits select the Color Mode of RAMDAC operation as shown in the following table 4 (default is 0 at power up):

Bit 4 - 1 **(Reserved)**

Bit 0 **Power Down Mode of RAMDAC**
When this bit is set to 0 (default is 0), the device operates normally. If this bit is set to 1, the power and clock to the Color Palette RAM and DACs are turned off. The data in the Color Palette RAM are still preserved. The CPU can access without loss of data by internal automatic clock start/stop control. The DAC outputs become the same as BLANK* (sync) level output during power down mode. This bit does not effect the PLL clock synthesizer function.

Color Modes

The four selectable color modes are described here.

Mode 0: 8-bit Pseudo Color (one clock per pixel). This mode is the 8-bit per pixel Pseudo Color mode. In this mode. inputs P0-P7 are the pixel address for the color palette RAM and are latched on the rising edge of every PCLK. This is the default mode on power up and it is selected by setting bits CR7-CR5 to 000 . There are three clock cycles pipe line delays from input to DAC output.

8-bit Pseudo Color mode

DATA BYTE							
7	6	5	4	3	2	1	0
PIXEL ACCESS							
7	6	5	4	3	2	1	0

CM2 (CR7)	CM1 (CR6)	CM0 (CR5)	Color Mode	Clock Cycles/ Pixel Bits
0	0	0	6-Bit Pseudo Color with Palette (Default)	1
0	0	1	15-Bit Direct Color with Bypass (Hi-Color)	2
0	1	0	24-Bit True Color with Bypass (True Color)	3
0	1	1	16-Bit Direct Color with Bypass (XGA)	2
1	0	0	15-Bit Direct Color with Bypass (Hi-Color)	2
1	0	1	15-Bit Direct Color with Bypass (Hi-Color)	2
1	1	0	16-Bit Direct Color with Bypass (XGA)	2
1	1	1	24-Bit True Color with Bypass (True Color)	3

Table 4 - Color Mode Select

Mode 1: (15-bit per color bypassHi-Color mode).
This mode is the 15-bit per pixel bypass mode. In this mode, inputs P0-P7 are the color DATA and are input directly to the DAC, bypassing the color palette. The two bytes of data is latched in two successive PCLK rising edges. ICS5301 supports only the two clock mode and does not support the mode where the data are latched on the rising and the falling edges. For compatibility, the 15/16 one clock modes are selected as two clock modes in this chip. The low-byte, high byte synchronization is internally done by the rising edge of BLANK*. Each color is 5-bit wide and is packed into two bytes as shown below. The mode is selected by setting bits CR7-CR5 to 001, 100 or 101.

15-Bit Color Mode
3LSB = set to zero

SECOND BYTE								FIRST BYTE							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
X	7	6	5	4	3	7	6	5	4	3	7	6	5	4	3
	RED				GREEN						BLUE				

Mode 2: (16-bit per pixel bypass XGA mode).
This mode is the 16-bit per pixel bypass mode and the P0-P7 inputs to go to the DAC directly, bypassing the color palette. The 2 bytes data is latched on two successive rising edges and the low-byte, high-byte synchronization is internally done by the rising edge of BLANK*. In this mode, blue and red colors are 6 bits wide and green is 5 bits wide. The 2 bytes of data is packed as shown below. The mode is selected by setting bits CR7-CR5 to 011 or 110.

16-Bit color mode
2LSB = set to zero (green)
3LSB = set to zero (blue, red)

SECOND BYTE								FIRST BYTE							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
7	6	5	4	3	7	6	5	4	3	2	7	6	5	4	3
RED					GREEN						BLUE				

Mode 3: (24-bit per pixel True Color Mode).
This mode is the 24-bit per pixel bypass mode. The three bytes of data are latched on three successive PCLK edges and the first byte is synchronized by the rising edge of BLANK*. In this mode, each of the colors are 8-bit wide and the DAC is an 8-bit wide DAC. The first byte is blue followed by green and red. This mode can be selected by setting bits CR7-CR5 to 010 or 111. The DAC outputs changes every three cycles and the pipeline delay from the first byte to output is five cycles.

24-bit color mode

THIRD BYTE								SECOND BYTE								FIRST BYTE							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RED								GREEN								BLUE							

Frequency Generators

The ICS5301 clock synthesizer can be reprogrammed through the microprocessor interface for any set of frequencies. This is done by writing appropriate values to the PLL Parameter Register Bank (table 5).

PLL Address Registers

The address of the parameter register is written to the PLL address registers before accessing the parameter register. This register is accessed by register select pins RS2-RS0 = 100 or 111.

7	6	5	4	3	2	1	0
PLL REGISTER ADDRESS							
7	6	5	4	3	2	1	0

PLL Parameter Register

There are sixteen registers in the PLL parameter register (table 5). Registers 00 to 07 are for the CLK0 selectable frequency list, Register 0A for CLK1 programmable frequency and register 0E is the PLL CLK0 control register.

Index	R/W	Register	
00	R/-	CLK0 f0 PLL Parameters	(2 bytes)
01	R/-	CLK0 f1 PLL Parameters	(2 bytes)
02	R/W	CLK0 f2 PLL Parameters	(2 bytes)
03	R/W	CLK0 f3 PLL Parameters	(2 bytes)
04	R/W	CLK0 f4 PLL Parameters	(2 bytes)
05	R/W	CLK0 f5 PLL Parameters	(2 bytes)
06	R/W	CLK0 f6 PLL Parameters	(2 bytes)
07	R/W	CLK0 f7 PLL Parameters	(2 bytes)
08	R/-	(Reserved) = 0	(2 bytes)
09	R/-	(Reserved) = 0	(2 bytes)
0A	R/W	CLK1fA PLL	(2 bytes)
0B	R/-	(Reserved) = 0	(2 bytes)
0C	R/-	(Reserved) = 0	(2 bytes)
0D	R/-	(Reserved) = 0	(2 bytes)
0E	R/W	PLL Control Register	(1-byte)
0F	R/-	(Reserved) = 0	(2-byte)

Table 5 - PLL Parameter Registers

PLL Control Register

Bits in this register determine internal or external CLK0 select.

7	6	5	4	3	2	1	0
(RV)	(RV)	ENBL	(RV)	(RV)	INTERNAL SELECT		
=0	=0	INCS	=0	=0	X	X	X

Bit 7 - 6 Reserved.

Bit 5 Enable Internal Clock Select (INCS) for CLK0. When this bit is set to 1, the CLK0 output frequency is selected by bit 2 - 0 in this register. External pins CS0 - CS2 are ignored.

Bit 4 - 3 (Reserved).

Bit 2 - 0 Internal Clock Select for CLK0 (INCS). These three bits selects the CLK0 output frequency if bit 5 of this register is on. They are interpreted as an octal number, n, that selects fn. Default selects f0.

PLL Data Registers

The CLK0 and CLK1 input frequency is determined by the parameter values in this register. These are two bytes registers; the first byte is the M-byte and the second is the N-byte.

M-Byte PLL Parameter Input
The M-byte has a 7-bit value (1-127) which is the feedback divider of the PLL.

7	6	5	4	3	2	1	0
Reserved	M-Divider Value						
=0	X	X	X	X	X	X	X

N-Byte PLL Parameter Input
The N-byte has two values. N1 sets a 5-bit value (1-31) for the input pre scalar and N2 is a 2-bit code for selecting 1, 2, 4, or 8 post divide clock output.

7	6	5	4	3	2	1	0
Reserved	N2-Code		N1-Divider Value				
=0	X	X	X	X	X	X	X

N2 Post Divide Code

N2 code	Divider
00	1
01	2
10	4
11	8

The block diagram of the PLL clock synthesizer is given in following figure 3.

Based on the M and N values, the output frequency of the clocks is given by the following equation:

$$F_{out} = \frac{(M+2) \text{ x } F_{ref}}{(N1+2) \text{ x} 2^{N2}}$$

M and N values should be programmed such that the frequency of the VC0 is within the optimum range for duty cycle, jitter and glitch free transition. Optimum duty cycle is achieved by programming N2 for values greater than one. See the following page for programming example.

Programming Example

Suppose an output frequency of 25.175 MHz is desired. The reference crystal is 14.318 MHz. The VCO should be targeted to run in the 100 to 180 MHz range, so choosing a post divide of 4 gives a VCO frequency of :

4 X 25.175=101.021 MHz

From the table on page 17, we find N2 = 2
Substituting F_{ref} = 14.318 and 2^{N2} = 4 into the equation on page 17:

$$\left(\frac{25.175}{14.318}\right)\cdot 4 = \frac{(M+2)}{(N1+2)}$$

by trial and error:

$$\left(\frac{25.175}{14.318}\right)\cdot 4 \approx \frac{127}{18}$$

so $M + 2 = 127$ $\quad M = 125$
$N1 + 2 = 18$ $\quad N1 = 16$

so the registers are:

M = 125d = 1 1 1 1 1 0 1 b
N = 0 & N2 code & N1 = 0 & 1 0 & 1 0 0 0 0
N = 0 1 0 1 0 0 0 0 b

Additional Information on Programming the Frequency Generator section of the GENDAC

When programming the GENDAC PLL parameter registers, there are many possible combinations of parameters which will give the correct output frequency. Some combinations are better than others, however. Here is a method to determine how the registers need to be set:

The key guidelines come from the operation of the phase locked loop, which has the following restrictions:

1. 2 MHz < f_{REF} < 32 MHz
This refers to the input reference frequency. Most users simply connect a 14.318 MHz crystal to the crystal inputs, so this is not a problem.

2. 600 kHz < $\frac{f_{REF}}{(N1+2)}$ ≤ 8 MHz
This is the frequency input to the phase detector.

3. 60 MHz ≤ $\frac{(M+2)}{(N1+2)} f_{REF}$ ≤ 270 MHz
This is the VCO frequency. In general, the VCO should run as fast as possible, because it has lower jitter at higher frequencies. Also, running the VCO at multiples of the desired frequency allows the use of output divides, which tends to improve the duty cycle.

4. f_{CLK0} and f_{CLK1} ≤ 135 MHz
This is the output frequency.

These rules lead to the following procedure for determining the PLL parameters, assuming rules 1 and 4 are satisfied.

A. Determine the value of N2 (either 1, 2, 4 or 8) by selecting the highest value of N2, which satisfies the condition
$N2^* f_{CLK} \leq 270$ MHz

B. Calculate $\frac{(M2+)}{(N1+2)} = \frac{2^{N2} f_{out}}{fref}$

C. Now (M+2) and (N1+2) must be found by trial and error. With a 14.318 MHz reference frequency, there will generally be a small output frequency error due to the resolution limit of (M+2) and (N1+2). For a given frequency tolerance, several different (M+2) and (N1+2) combinations can usually be found. Usually, a few minutes trying out numbers with a calculator will produce a workable combination. Multiplying possible values of (N1+2) by the desiredratio will indicate approximately the value of M. This method is shown in the example below. A program could be written to try all possible combinations of (M+2) and (N1+2) (3937 possible combinations), discard those outside error band, and select from those remaining by giving preference to ratios which use lower values of (M+2). Lower values of (M+2) and (N1+2) provide better noise rejection in the phase locked loop.

Example: Suppose we are using a 14.318 MHz reference crystal and wish to output a frequency of 66 MHz with an error of no greater than 0.5%. What are the values of the PLL data registers?

A. $66^*8 = 528 > 250$ VCO speed too high
$66^*4 = 264 > 250$ VCO speed too high
$66^*2 = 132 < 250$ VCO speed OK, N2 = 2, N2 code = 01 from table on page 17 of the data sheet.

B. 132/14.31818 = 9.219
This is the desired frequency multiplication ratio.

C. Setting (N1+2) = 3, 4,...12, 13 and performing some simple calculations yields the following table: (Note that N1 cannot be 0)

(N1+2)	(N1+2)*9.219	rounded (=M+2)	Actual Ratio	Percent Error
3	27.657	28	9.33	-1.23
4	36.876	37	9.25	-0.34
5	46.095	46	9.20	0.21
6	55.314	55	9.17	0.57
7	64.533	65	9.29	-0.72
8	73.752	74	9.25	-0.34
9	82.971	83	9.22	-0.03
10	92.19	92	9.20	0.21
11	101.409	101	9.18	0.40
12	110.628	111	9.25	-0.34
13	119.847	120	9.23	-0.13

The ratio 83/9 is closest. Thus (N2+2) = 9; N2=7. (M+2) = 83; M = 81. The M-byte PLL parameter word is simply 81 in binary, plus bit 7 (which must be set to 0), or 01010001. The N-byte PLL parameter word is N2 code (01) concatenated with 5 bits of N2 in binary (00111), or 00100111. Once again, bit 7 must be zero.

We have chosen the combination with the least frequency error, but several other combinations are within the 0.5% tolerance. Because the lowest value of (M+2) offers the best damping, the 37/4 combination will have the best power supply rejection. This results in lower jitter due to external noise.

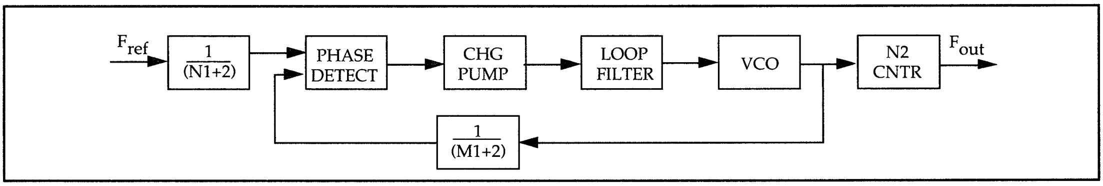
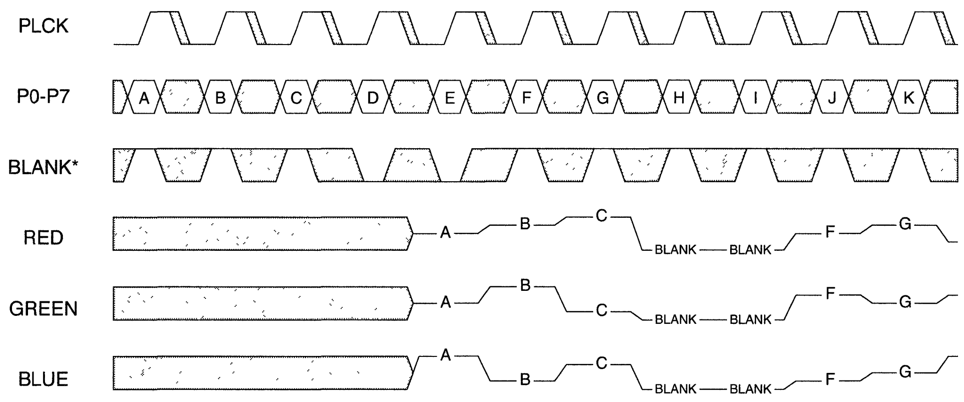


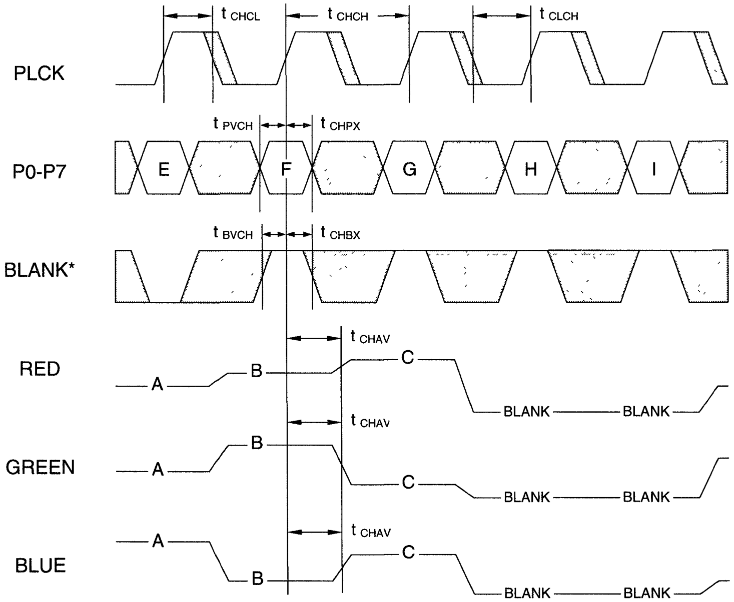
Figure 3 - PLL Clock Synthesizer Block Diagram

External Select			(Internal Select PLL Control Register)			
CS2	CS1	CS0	BIT 2	BIT 1	BIT 0	CLK 0 Frequency
0	0	0	0	0	0	f0
0	0	1	0	0	1	f1
0	1	0	0	1	0	f2
0	1	1	0	1	1	f3
1	0	0	1	0	0	f4
1	0	1	1	0	1	f5
1	1	0	1	1	0	f6
1	1	1	1	1	1	f7

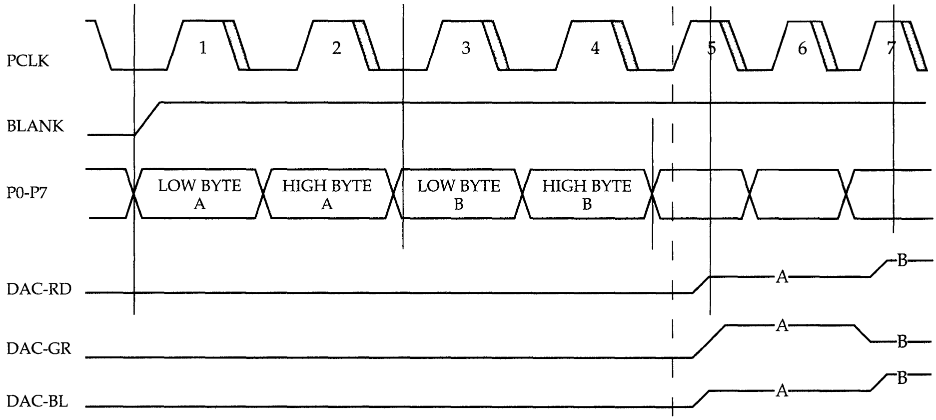
Video Clock Selection Table



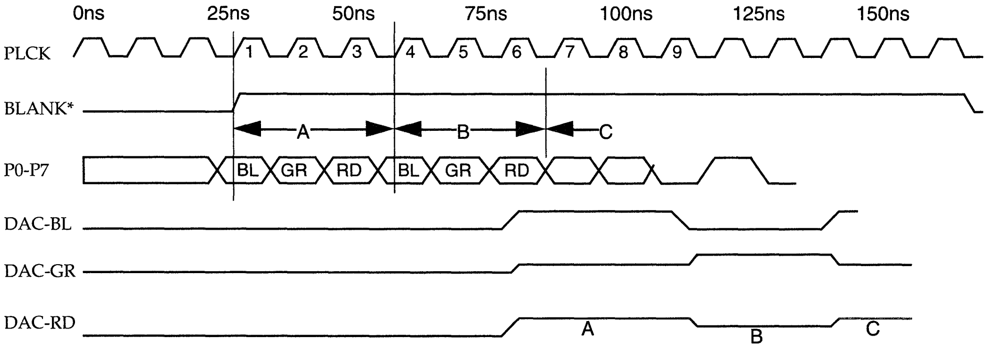
System Timing - Pseudo Color, Mode 0



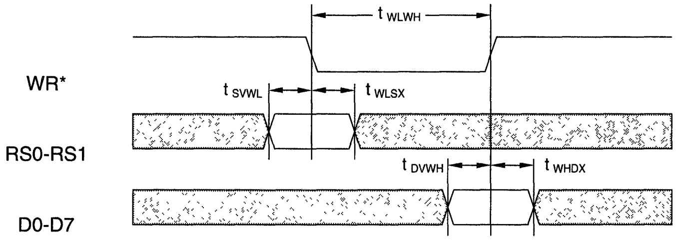
Detailed Timing Specifications - Pseudo Color, Mode 0



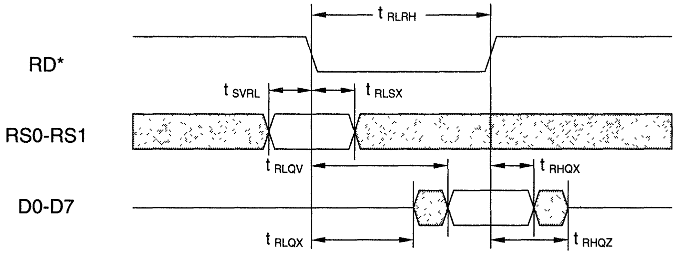
System Timing Bypass - 15 (5/5/5) and 16 (5/6/5) Modes 1, 2



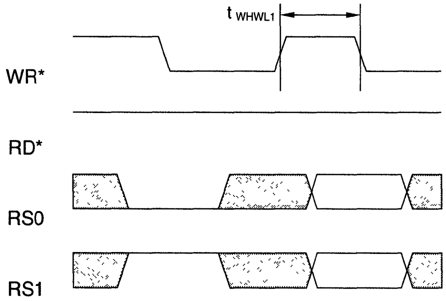
System Timing Bypass True Color 24 (8,8,8) Mode 3



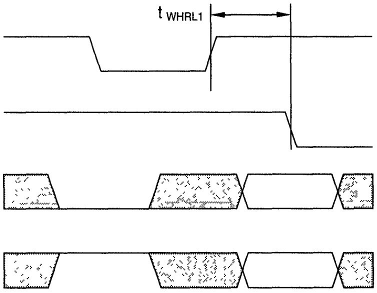
Basic Write Cycle Timing



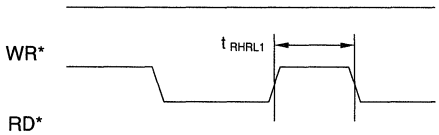
Basic Read Cycle Timing



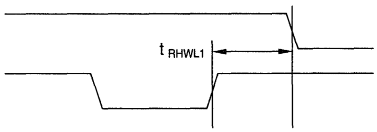
Write to Pixel Mask Register Followed by Write



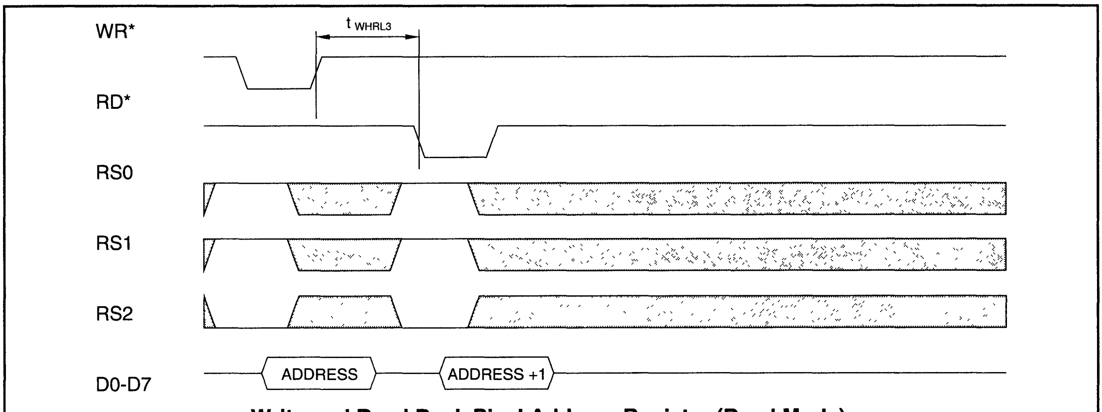
Write to Pixel Mask Register Followed by Read



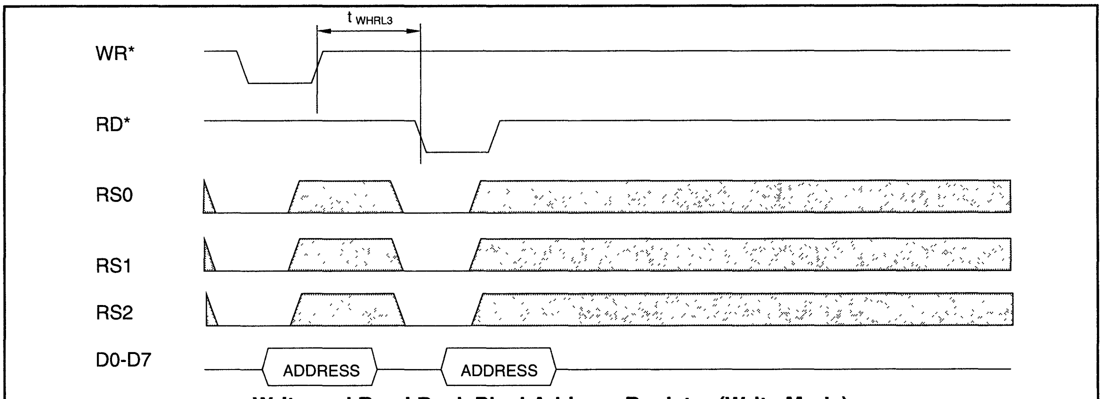
Read from Pixel or Pixel Address Register (Read or Write) followed by Read



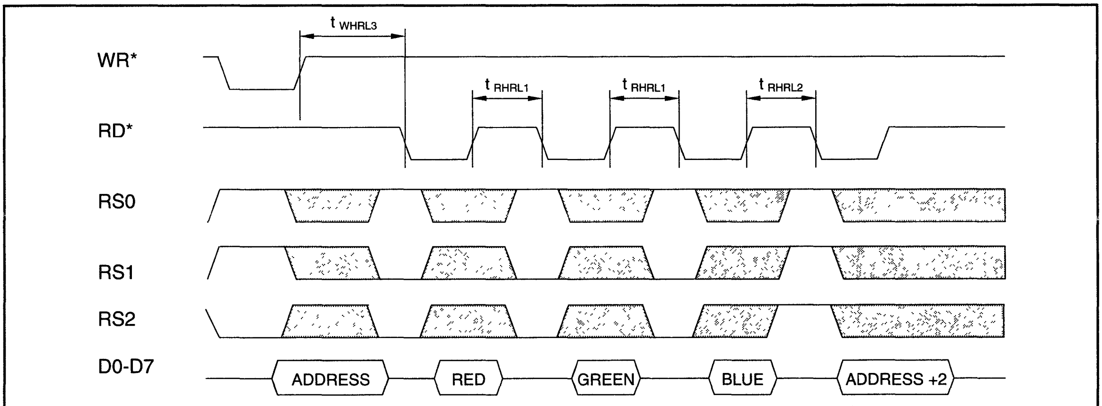
Read from Pixel or Pixel Address Register (Read or Write) followed by Write



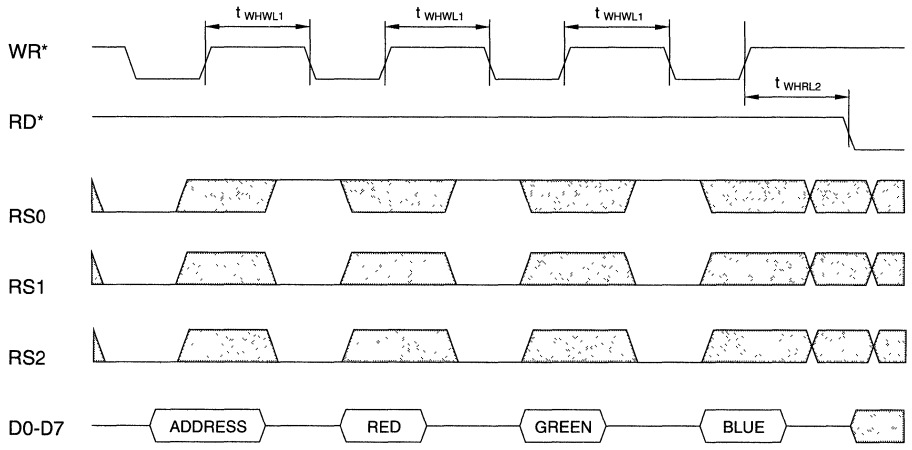
Write and Read Back Pixel Address Register (Read Mode)



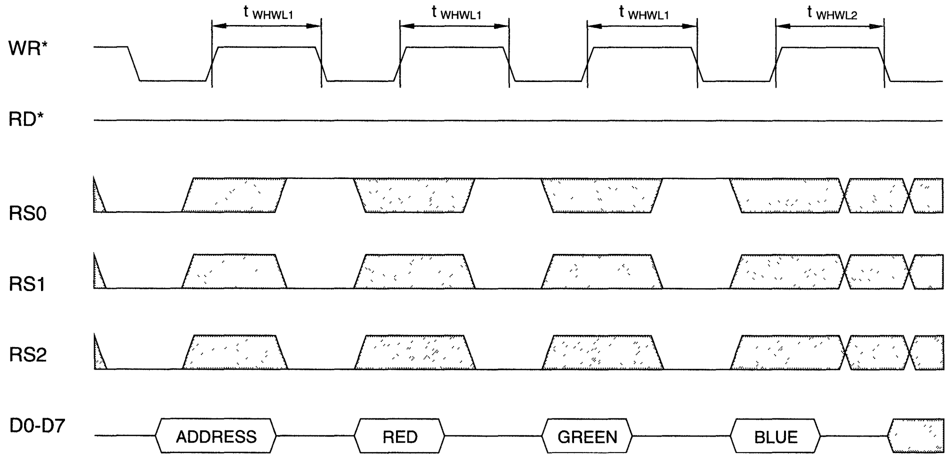
Write and Read Back Pixel Address Register (Write Mode)



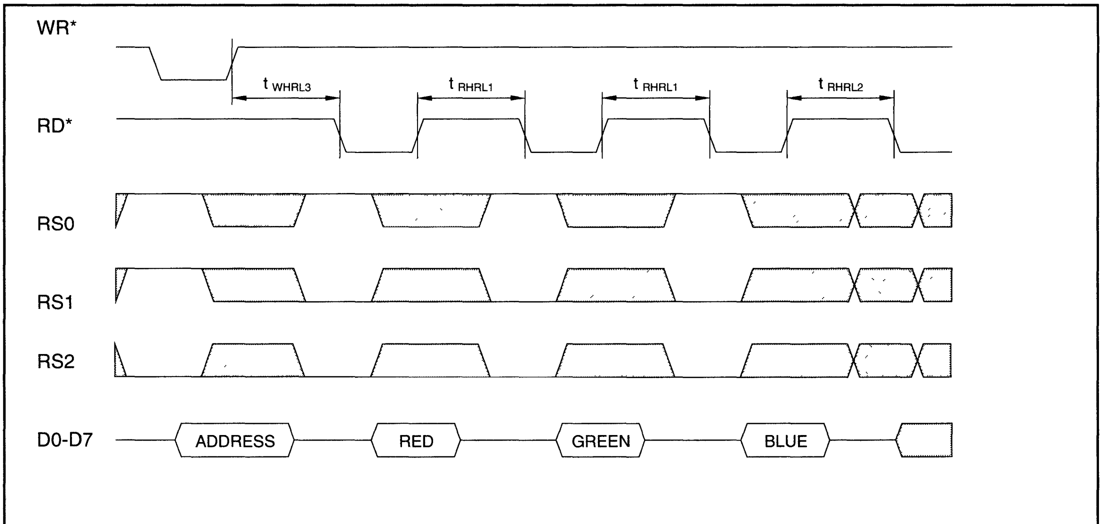
Read Color Value then Pixel Address Register (Read Mode)



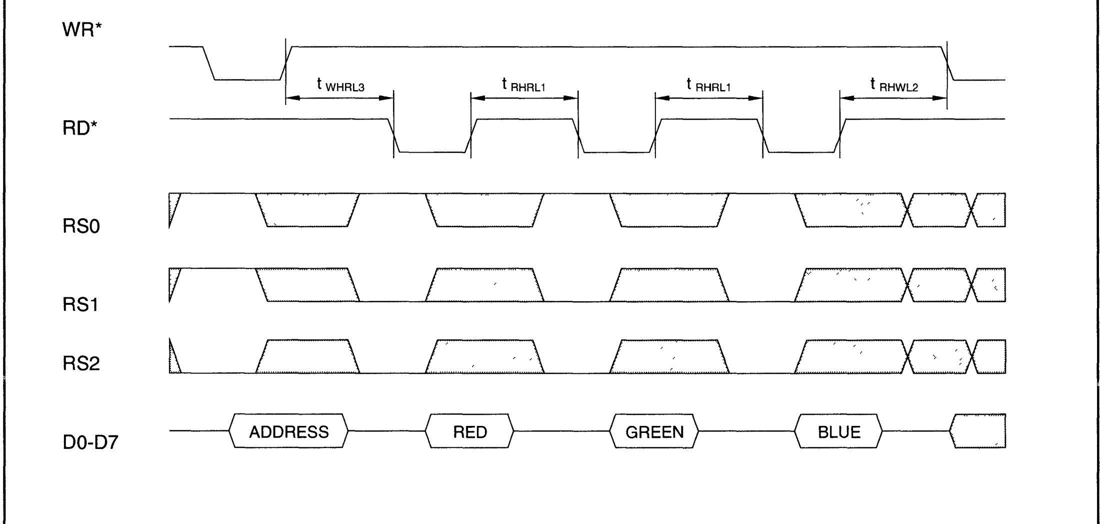
Color Value Write followed by any Read



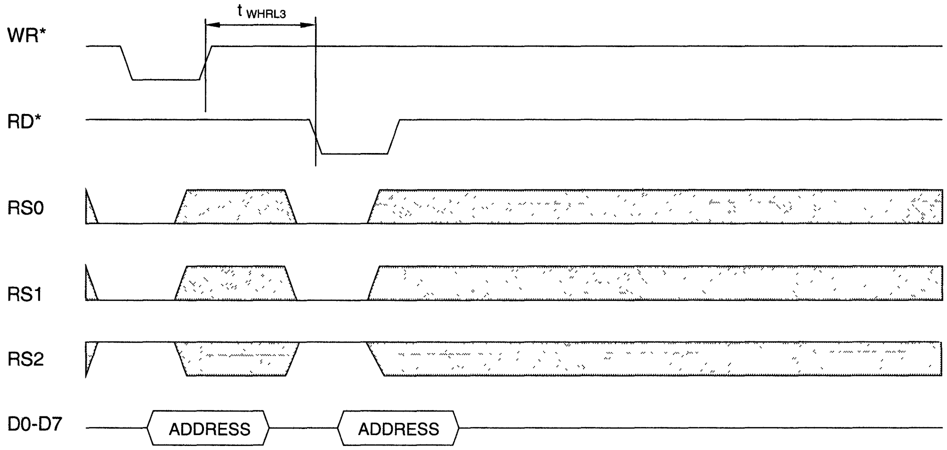
Color Value Write followed by any Write



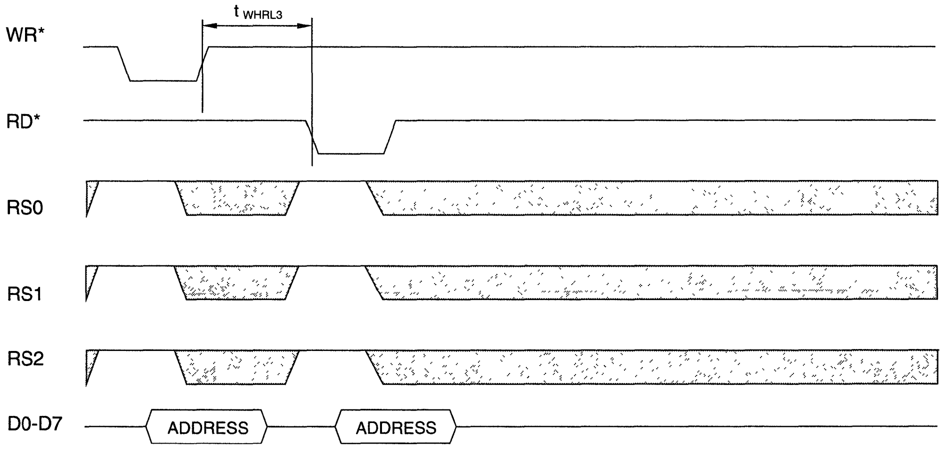
Color Value Read followed by any Read



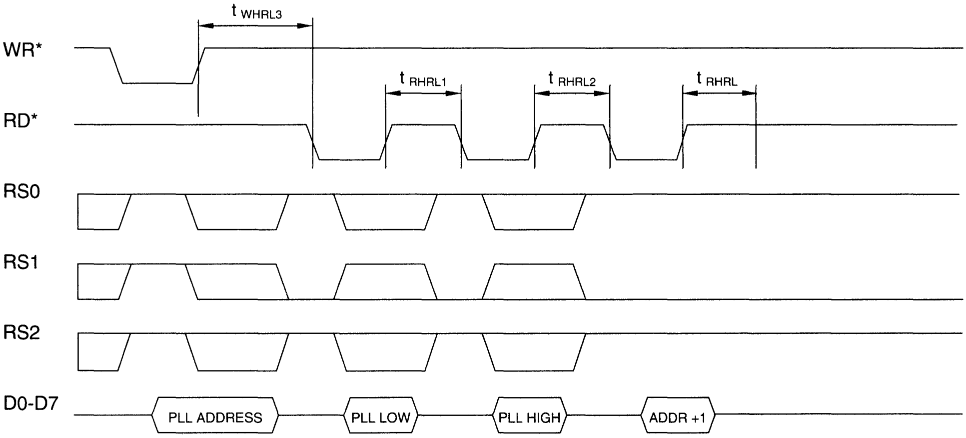
Color Value Read followed by any Write



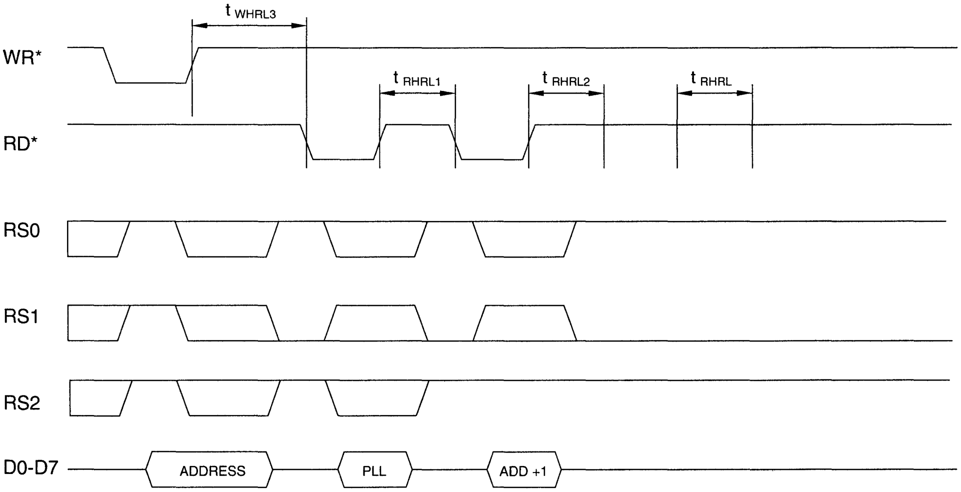
Write and Read back PLL Address Register (Write Mode)



Write and Read back PLL Address Register (Read Mode)

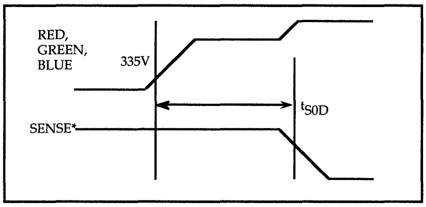


Read Two bytes PLL Register then PLL Address Register



Read One Byte PLL Register then PLL Address Register

Monitor SENSE Signal

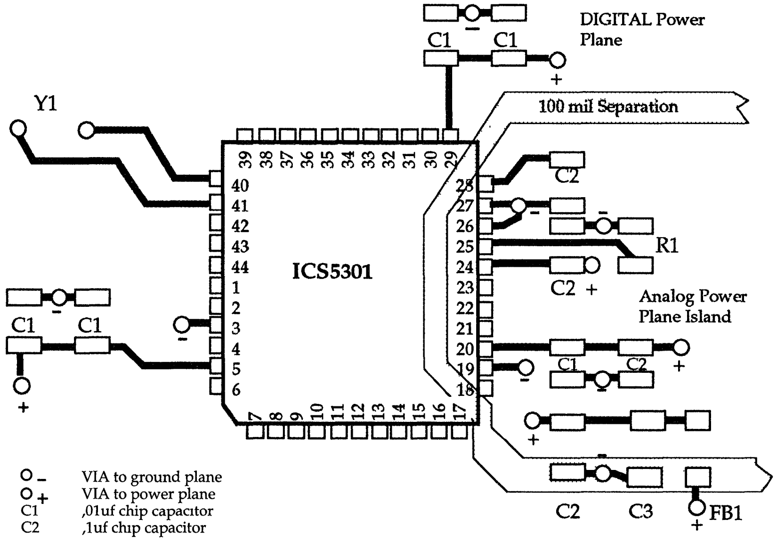


Recommended Layout

The high performance of which the ICS5301 GENDAC is capable is dependent on careful PC board layout. The use of a four layer board (internal power and ground planes, signals on the two surface layers) is recommended. The layout below shows a suggested configuration.

The ground plane is continuous, but the power plane is separated into analog and digital sections as shown. Power is supplied to the analog power plane through the ferrite bead, and bypassed at the power entry point by C3, a 10 μF tantalum capacitor. These high current connections should have multiple vias to the ground and power planes, if possible. Power connections should be connected to the analog or digital power plane, as shown in the diagram. Power pins 5 and 29 should be connected to digital power, power pins 20 and 24 to analog power. Decoupling capacitors (indicated by C1) should be placed as close to the GENDAC as possible.

The analog and digital I/O lines are not shown. Analog signals (DAC outputs, Vref, Rset) should only be routed above the analog power plane. Digital signals should only be routed above the digital power plane.



○ -	VIA to ground plane
○ +	VIA to power plane
C1	,01uf chip capacitor
C2	,1uf chip capacitor
C3	10uf tantulum capacitor
FB1	Ferrite Bead
R1	140 ohm 1% resistor
Y1	14.318 Mhz parallel resonant crysal cut for C_L=12

Ordering Information

ICS5301V

Example:

ICS XXXX M

Package Type
V=PLCC
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS5340
GENDAC

16-Bit Integrated Clock-LUT-DAC

General Description

The ICS5340 GENDAC is a combination of dual programmable clock generators, a 256 x 18-bit RAM, and a triple 8-bit video DAC. The GENDAC supports 8-bit pseudo color applications, as well as 15-bit, 16-bit and 24-bit True Color bypass for high speed, direct access to the DACs.

The RAM makes it possible to display 256 colors selected from a possible 262,144 colors. The dual clock generators use Phase Locked Loop (PLL) technology to provide programmable frequencies for use in the graphics subsystem. The video clock contains 8 frequencies, 6 of which are programmable by the user. The memory clock has two programmable frequency locations.

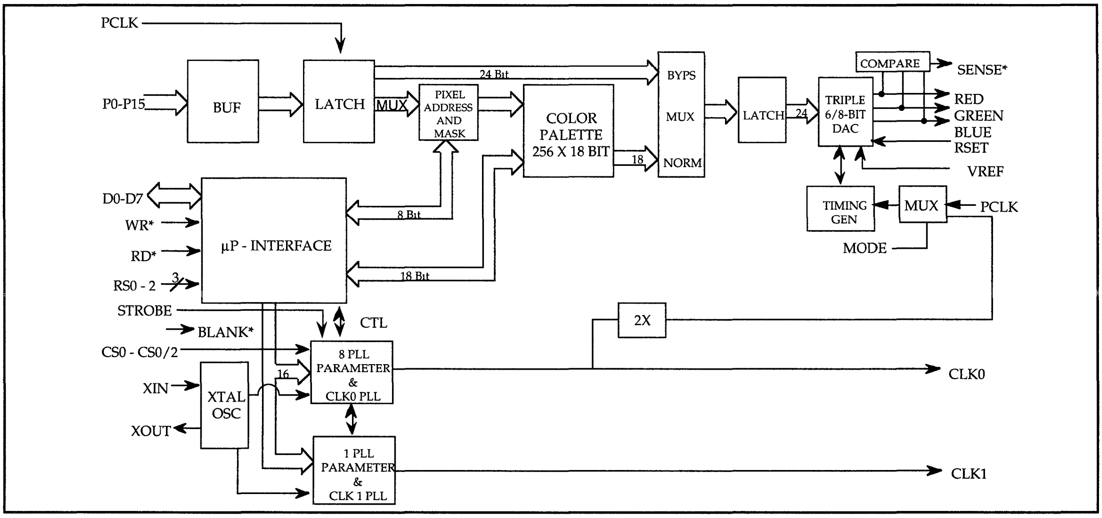
The three 8-bit DACs on the ICS5340 are capable of driving singly or doubly-terminated 75Ω loads to nominal 0 - 0.7 volts at pixel rates up to 135 MHz. Differential and integral linearity errors are less than 1 LSB over full temperature and V_{DD} ranges. Monotonicity is guaranteed by design. On-chip pixel mask register allows displayed colors to be changed in a single write cycle rather than by modifying the color palette.

ICS is the world leader in all aspects of frequency (clock) generation for graphics, using patented techniques to produce low jitter video timing.

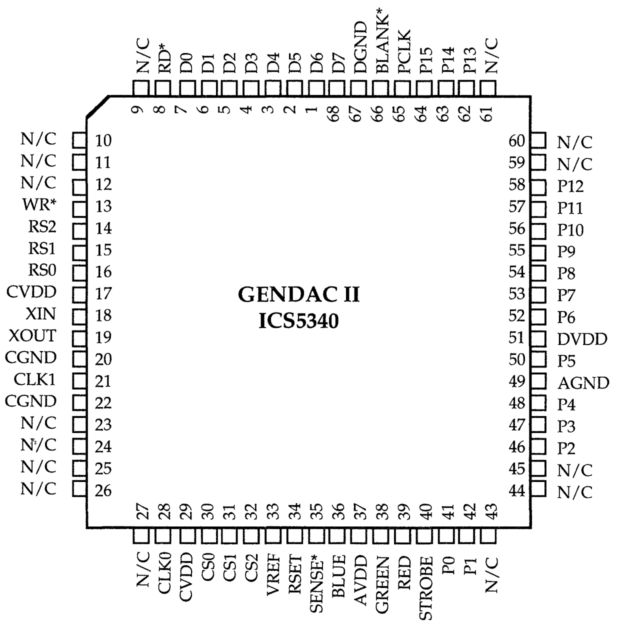
Features

- **Triple video DAC, dual clock generator, and a color palette**
- **24, 16, 15, or 8-bit pseudo color pixel mode supports True Color, Hi-Color, and VGA modes**
- **High speed 256 x 18 color palette (135 MHz) with bypass mode and 8-bit DACs**
- **Two fixed, six programmable video (pixel) clock frequencies (CLK0)**
- **Two programmable memory (controller) clock frequency (CLK1)**
- **DAC power down in blanking mode**
- **Anti-sparkle circuitry**
- **On-chip loop filters reduce external components**
- **Standard CPU interface**
- **Single external crystal (typically 14.318 MHz)**
- **Monitor Sense**
- **Internal voltage reference**
- **135 MHz (-3), 110 MHz (-2) & 80 MHz (-1) versions**
- **Very low clock jitter**
- **Latched frequency control pin**

Block Diagram



Pin Configuration



Rev 1.0

Pin Description (68 pin PLCC) K-10

Symbol	Pin #	Type	Description
D7 - D0	68, 1 - 7	I/O	System data bus I/O. These bidirectional Data I/O lines are used by the host microprocessor to write (using active low WR*) information into, and read (using active low RD*) information from the six internal registers (Pixel Address, Color Value, Pixel Mask, PLL Address, PLL Parameter, and Command). During the write cycle, the rising edge of WR* latches the data into the selected register (set by the status of the three RS pins). The rising edge of RD* determines the end of the read cycle. When RD* is a logical high, the Data I/O lines no longer contain information from the selected register and will go into a tri-state mode.
RD*	8	Input	RAM/PLL Read Enable, active low. This is the READ bus control signal. When active, any information present on the internal data bus is available on the Data I/O lines, D0-D7.
WR*	13	Input	RAM/PLL Write Enable, active low. This signal controls the timing of the write operation on the microprocessor interface inputs, D0-D7.
RS2 RS1 RS0	14 15 16	Input Input Input	Register Address Select 0. These inputs control the selection of one of the six internal registers. They are sampled on the falling edge of the active enable signal (RD* or WR*).
CVDD	17	-	Crystal oscillator and CLK0 power supply connect to AVDD.
XIN	18	Input	Crystal input. A 14.318 MHz crystal should be connected to this pin.
XOUT	19	Output	Crystal output. A 14.318 MHz crystal should be connected to this pin.
CGND	20	-	VSS for CLK0. Connect to ground.

Pin Description (continued)

Symbol	Pin #	Type	Description
CLK1	21	Output	Memory clock output. Used to time the video memory.
CGND	22	-	VSS for CLK1. Connect to ground.
CLK0 CVDD	28 29	Output -	Video clock output. Provides a CMOS level pixel or dot clock frequency to the graphics controller. The output frequency is determined by the values of the PLL registers. CLK1 Power Supply. Connect to AVDD.
CS0	30	Input	Clock select 0. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
CS1	31	Input	Clock select 1. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
CS2	32	Input	Clock select 2. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
VREF	33	I/O	Internal Reference Voltage. Normally connects to a 0.1µ cap to ground. To use an external Vref, connect a 1.235V reference to this pin.
RSET	34	Input	Resistor Set. This pin is used to set the current level in the analog outputs. It is usually connected through a 140Ω, 1% resistor to ground.
SENSE*	35	Output	Monitor Sense, active low. This pin is low when any of the red, green, or blue outputs have exceeded 335mV. The chip has on-board comparators and an internal 335mV voltage reference. This is used to detect monitor type.
AVDD	37	-	DAC power supply. Connect to AVDD.
BLUE GREEN RED	36 38 39	Output Output Output	Color Signals. These three signals are the DACs' analog outputs. Each DAC is composed of several current sources. The outputs of each of the sources are added together according to the applied binary value. These outputs are typically used to drive a CRT monitor.
STROBE	40	Input	Latches the input clock select signals CS0 - CS2.
P0 - P15	41- 42 46-48, 50	Input	Pixel Address Lines. This byte-wide information is latched by the rising edge of PCLK when using the Color Palette, and is masked by the Pixel Mask register. These values are used to specify the RAM word address in the default mode (accessing RAM). In the Hi-Color XGA, and True Color modes, they represent color data for the DACs. These inputs should be grounded if they are not used.
AGND	49	-	DAC Ground. Connect to ground.
DVDD	51	-	Digital power supply.
PCLK	65 52-58, 62-64	Input	Pixel Clock. The rising edge of PCLK controls the latching of the Pixel Address and BLANK* inputs. This clock also controls the progress of these values through the three-stage pipeline of the Color Palette RAM, DAC, and outputs.
BLANK*	66	Input	Composite BLANK* Signal, active low. When BLANK* is asserted, the outputs of the DACs are zero and the screen becomes black. The DACs are automatically powered down to save current during blanking. The color palette may still be updated through D0-D7 during blanking.
DGND	67	-	Digital Ground. Connect to ground.

Internal Registers

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
				There is a single Pixel Address register within the GENDAC. This register can be accessed through either register address 0,0,0 or register address 0,1,1. A read from address 0,0,0 is identical to a read from address 0,1,1. Writing a value to address 0,0,0 performs the following operations: a) Specifies an address within the color palette RAM. b) Initializes the Color Value register. Writing a value to address 0,1,1 performs the following operations: a) Specifies an address within the color palette RAM. b) Loads the Color Value register with the contents of the location in the addressed RAM palette and then increments the Pixel Address register.
0	0	0	Pixel Address WRITE	Writing to this 8-bit register is performed prior to writing one or more color values to the color palette RAM.
0	1	1	Pixel Address READ	Writing to this 8-bit register is performed prior to reading one or more color values from the color palette RAM.
0	0	1	Color Value	The 18-bit Color Value register acts as a buffer between the microprocessor interface and the color palette. Using a three bytes transfer sequence allows a value to be read from or written to this register. When a byte is read, the color value is contained in the least significant 6 bits , D0-D5 (the most significant 2 bits are set to zero). When writing a byte, the same 6 bits are used. When reading or writing, data is transferred in the same order - the red byte first, then green, then blue. Each transfer between the Color Value register and the color palette replaces the normal pixel mapping operations of the GENDAC for a single pixel. After writing three definitions to this register, its contents are written to the location in the color palette RAM specified by the Pixel Address register, and the Pixel Address register increments. After reading three definitions from this register, the contents of the location in the color palette RAM specified by the Pixel Address registers are copied into the Color Value register, and the Pixel Address register increments.
0	1	0	Pixel Mask	The 8-bit Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P0-P7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, while a zero sets that bit to zero. The Pixel Mask register does not affect the Pixel Address generated by the microprocessor interface when the palette RAM is being accessed.

Internal Registers (continued)

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
1	0	0	PLL Address WRITE	Writing to this 8-bit register is performed prior to writing one or more PLL programming values to the PLL Parameter register.
1	1	1	PLL Address READ	Writing to this 8-bit register is performed prior to reading one or more PLL programming values from the PLL Parameter register.
1	1	0	Command	This 8-bit register selects the color mode, for instance 8-bit Pseudo Color, Hi-Color , True Color, or XGA, and DAC power down. The registers are reset to pseudo color mode on power up.
1	0	1	PLL Parameter	There are sixteen parameter registers as indexed by PLL Address Write/ Read registers. Parameter registers 00-0D and 0F are two bytes long and 0E* is one byte long. This register set contains one control register. The bits of this register include clock select and enable functions, the rest contain PLL frequency parameters. After writing the start index address in the PLL address register, these registers can be accessed in successive two (or one) bytes. The address register auto increments after one or two bytes to access the entire register set.

Absolute Maximum Ratings

Power Supply Voltage	7 V	DC Digital Output Current	25 mA
Voltage on any other pin	GND – 0.5V to V_{DD} + 0.5V	Analog Output Current	45 mA
Temperature under bias	– 40° C to 85° C	Reference Current	–15 mA
Storage Temperature	– 65° C to 150° C	Power Dissipation	1.0 W

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
DC CHARACTERISTICS (note: J)					
V_{DD}	Positive supply voltage		4.75	5.25	V
V_{IH}	Input logic "1" voltage		2.0	V_{DD} + 0.5	V
V_{IL}	Input logic "0" voltage		– 0.5	0.8	V
I_{REF}	Reference current		–7.0	–10	mA
V_{REF}	Reference voltage		1.10	1.35	V
I_{IN}	Digital input current	V_{DD} = max, GND ≤ V_{IN} ≤ V_{DD}		± 10	µA
I_{OZ}	Off-state digital output current	V_{DD} = max, GND ≤ V_{IN} ≤ V_{DD}		± 50	µA
I_{DD}	Average power supply current	I_O = max, Digital outputs unloaded		250	mA
I_{DACOFF}	DACs in power down mode	No palette access		50	mA
V_{OHS}	Sense logic "1"	I_O = .4mA	2.4		V
V_{OLS}	Sense logic "0"	I_O = .4mA		0.4	V
V_{OHC}	Clock logic "1"	I_O = TBD	2.4		V
V_{OLC}	Clock logic "0"	I_O = TBD		0.4	V
V_{OH}	logic "1"	I_O = -3.2mA, note K	2.4		V
V_{OL}	logic "0"	I_O = 3.2mA, note K		0.4	V
$ICLK_r$*	Input Clock Rise Time	TTL levels		15	ns
$ICLK_f$*	Input Clock Fall Time	TTL levels		15	ns
F_D	Frequency Change of CLK0 and CLK1 over supply and temperature	With respect to typical frequency		0.05	%

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Units
DAC CHARACTERISTICS (note: J)					
V_O (max)	Maximum output voltage	$I_O \le 10$ mA		1.5	V
I_O (max)	Maximum output current	$V_O \le 1$V		21	mA
	Full scale error	note A, B		± 5	%
	DAC to DAC correlation	note B		±2	%
	Integral Linearity, 6-bit	note B		±0.5	LSB
	Integral Linearity, 8-bit	note B		±1	LSB
	Full scale settling time*, 6-bit	note C		28	ns
	Full scale settling time*, 8-bit	note C		20	ns
	Rise time (10% to 90%)*	note C		6	ns
	Glitch energy*	note C		200	pVsec

* Characterized values only

Symbol	Parameter	Conditions	Min	Max	Units
PLL AC CHARACTERISTICS					
f_0	Clock 0 operating range*		25	135	MHz
f_1	Clock 1 operating range*		25	135	MHz
t_r	Output clocks rise time*	25 pf load, TTL levels		3	ns
t_r	Output clocks fall time*	25 pf load, TTL levels		3	ns
d_t	Duty Cycle*		40/60	60/40	%
j_{1s}	Jitter, one sigma*			130 ps	ps
j_{abs}	Jitter, absolute*		-300 ps	300 ps	ps
f_{ref}	Input reference frequency*	Typically 14.318 MHz	5	25	MHz

AC Electrical Characteristics (note: J)

Symbol	Parameter	Condition	80 MHz		110 MHz		135 MHz		Units
			Min	Max	Min	Max	Min	Max	
t_{CHCH}	PCLK period		12.5		9.09		7.4		ns
Δt_{CHCH}^*	PCLK jitter	note D		±2.5		+2.5			%
t_{CLCH}	PCLK width low		5		3.6		3		ns
t_{CHCL}	PCLK width high		5		3.6		3		ns
t_{PVCH}	Pixel word setup time	note E	3		3		2		ns
t_{CHPX}	Pixel word hold time	note E	3		2		1		ns
t_{BVCH}	BLANK* setup time	note E	3		3		2		ns
t_{CHBX}	BLANK* hold time	note E	3		2		1		ns
t_{CHAV}^*	PCLK to valid DAC output	note F		20		20		20	ns
Δt_{CHAV}	Differential output delay	note G		2		2		2	ns
t_{WLWH}	WR* pulse width low		50		50		50		ns
t_{RLRH}	RD* pulse width low		50		50		50		ns
t_{SVWL}	Register select setup time	Write cycle	10		10		10		ns
t_{SVRL}	Register select setup time	Read cycle	10		10		10		ns
t_{WLSX}	Register select hold time	Write cycle	10		10		10		ns
t_{RLSX}	Register select hold time	Read cycle	10		10		10		ns
t_{DVWH}	WR* data setup time		10		10		10		ns
t_{WHDX}	WR* data hold time		10		10		10		ns
t_{RLQX}	Output turn-on delay		5		5		5		ns
t_{RLQV}	RD* enable access time			40		40		40	ns
t_{RHQX}	Output hold time		5		5		5		ns
t_{RHQZ}	Output turn-off delay	note H		20		20		20	ns
t_{WHWL1}	Successive write interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHRL1}	WR* followed by read interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHRL1}	Successive read interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHWL1}	RD* followed by write interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHWL2}	WR* after color write	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHRL2}	RD* after color write	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHRL2}	RD* after color read	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{RHWL2}	WR* after color read	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{WHRL3}	RD* after read address write	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{SOD}	SENSE* output delay			1		1	1		µs

NOTES:

A. Full scale error is derived from design equation $\{[(F.S.I_{OUT})\ R_L - 2.1\ (I_{REF})\ R_L]/[2.1(I_{REF})R_L]\}\ 100\%$

$V_{BLACK\ LEVEL}$=0V $F.S.I_{OUT}$ = Actual full scale measured output

B. R= 37.5Ω, $I_{REF} = -8.88$mA

C. Z_I= 37.5Ω + 30 pF, $I_{REF} = -8\ 88$mA

D. This parameter is the allowed Pixel Clock frequency variation. It does not permit the Pixel Clock period to vary outside the minimum values for Pixel Clock (t_{CHCH}) period

E. It is required that the color palette's pixel address be a valid logic level with the appropriate setup and hold times at each rising edge of P_{CLK} (this requirement includes the blanking period).

F. The output delay is measured from the 50% point of the rising edge of CLOCK to the valid analog output. A valid analog output is defined when the analog signal is halfway between its successive values.

G. This applies to different analog outputs on the same device.

H. Measured at ± 200 mV from steady state output voltage

I. This parameter allows synchronization between operations on the microprocessor interface and the pixel stream being processed by the color palette.

J. The following specifications apply for V_{DD}= +5V± 0.5V, GND=0. Operating Temperature = 0°C to 70°C.

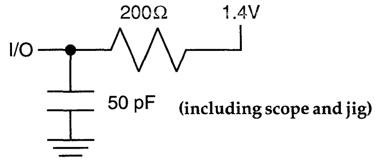
K. Except for SENSE pin.

AC Test Conditions

Input pulse levels	V_{DD} to 3V
Input rise and fall times (10% to 90%)	3ns
Digital input timing reference level	1.5V
Digital output timing reference level	0.8V and 2.4V

Capacitance

C_1 Digital input	7pF
C_0 Digital output	7pF
C_{0A} Analog output	10pF



DIGITAL OUTPUT LOAD

General Operation

The ICS5340 GENDAC is intended for use as the analog output stage of raster scan video systems. It contains a high-speed Random Access Memory of 256 x 18-bit words, three 6/8-bit high-speed DACs, a microprocessor/graphic controller interface, a pixel word mask, on-chip comparators, and two user programmable frequency generators.

An externally generated BLANK* signal can be applied to pin 66 of the ICS5340. This signal acts on all three of the analog outputs. The BLANK* signal is delayed internally so that it appears with the correct relationship to the pixel bit stream at the analog outputs.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the color palette RAM to facilitate such operations as animation and flashing objects. Operations on the contents of the mask register can also be totally asynchronous to the pixel stream.

The ICS5340 also includes dual PLL frequency generators providing a video clock (CLK0) and a memory clock (CLK1), both generated from a single 14.318 MHz crystal. There are eight selectable CLK0 frequencies. Six are programmable, and two are fixed. There are two selectable and programmable CLK1 frequencies (fA, fB). Default values (Table 1 and Table 2) are loaded into the appropriate registers on power up.

Video Path

The GENDAC supports nine different video modes and is determined by bits 4-7 of the command register. The default mode is the 8-bit Pseudo Color mode. The other modes are the bypass 15-bit, 16-bit and 24 bit True Color modes in 8-bit and 16-bit interface, and the 16-bit Pseudo Color (2:1) mode with 2X Clock.. The 16-bit True Color has sparse and packed modes.

Pseudo Color

8-bit Interface
In this mode, Pixel Address, P0-P7 and BLANK* inputs are sampled on the rising edge of the clock (PCLK) and any change appears at the analog outputs after three succeeding rising edges of the PCLK. The DAC outputs depends on the data in the color palette RAM.

16-bit Interface
In this mode, Pixel Address, P0-P15 and BLANK* inputs are sampled on the rising edge of the clock (PCLK) and any change appears at the analog outputs after three succeeding rising edges of the 2 x ICLK. The DAC outputs depends on the data in the color palette RAM.

Bypass Mode

The GENDAC supports seven different bypass modes : three for byte transfers and four for word transfers. In these modes, the address pins P0-P15 represent Color Data that is applied directly to the DAC . The internal look-up table RAM is ignored. During byte transfers, the P8-P15 inputs are Don't Care. Data is always latched on the rising edge of PCLK. Byte or Word framing is internally synchronized with the rising edge of BLANK*.

Dac Outputs

The outputs of the DACs are designed to be capable of producing 0.7 volt peak white amplitude with an I_{REF} of 8.88 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output load ($R_{EFFECTIVE}$) of 37.5Ω. The formula for calculating I_{REF} with various peak white voltage/output loading combinations is given below:

$$I_{REF} = \frac{V_{PEAK\ WHITE}}{2.1 \times R_{EFFECTIVE}}$$

Note that for all values of I_{REF} and output loading:

$$V_{BLACK\ LEVEL} = 0$$

The reference current I_{REF} is determined by the reference voltage V_{REF} and the value of the resistor connected to R_{SET} pin. V_{REF} can be the internal band gap reference voltage or can be overridden by an external voltage. In both cases $I_{REF} = V_{REF}/R_{SET}$.

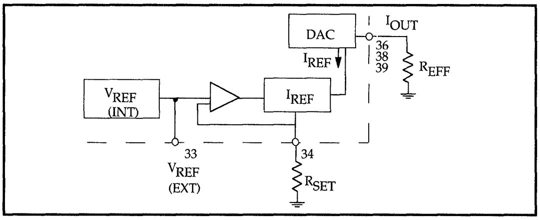


Figure 4 - DAC Set up

The BLANK* input to the GENDAC acts on all three of the DAC outputs. When the BLANK* input is low, the DACs are powered down.

The connection between the DAC outputs of the ICS5340 and the RGB inputs of the monitor should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor.

RF techniques should be observed to ensure good fidelity. The PCB trace connecting the GENDAC to the off-board connector should be sized to form a transmission line of the correct impedance. Correctly matched RF connectors should be used for connection from the PCB to the coaxial cable leading to the monitor and from the cable to the monitor.

There are two recommended methods of DAC termination: double termination and buffered signal. Each is described below with its relative merits:

Double Termination (Figure 1)
For this termination scheme, a load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line. Double termination of the DAC output allows both ends of the transmission line between the DAC

outputs and the monitor inputs to be correctly matched. The result should be an ideal reflection free system. This arrangement is relatively tolerant to variations in transmission line impedance (e.g. a mismatched connector) since no reflections occur from either end of the line.

A doubly terminated DAC output will rise faster than any singly terminated output because the rise time of the DAC outputs is dependent on the RC time constant of the load.

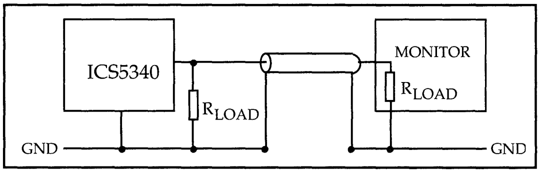


Figure 1 - Double Termination

Buffered Signal (Figure 2)

If the GENDAC drives large capacitive loads (for instance long cable runs), it may be necessary to buffer the DAC outputs. The buffer will have a relatively high input impedance. The connection between the DAC outputs and the buffer inputs should also be considered as a transmission line. The buffer output will have a relatively low impedance. It should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.

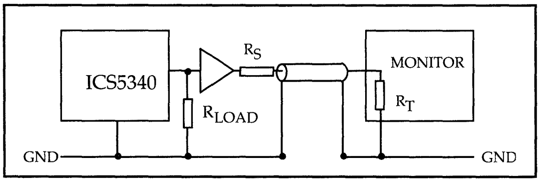


Figure 2 - Buffered Signal

SENSE Output

The GENDAC contains three comparators, one each for the DAC output (R, G and B) lines. The reference voltage to the comparators is proportional to the V_{REF} (internal or external) and is typically 0.33 for V_{REF} =1.23 Volts. When the voltage on any of these pins go higher than the reference voltage to the comparators, the SENSE* pin is driven low. This signal is used to detect the type of (or lack of) monitor connected to the system.

PLL Clock

The ICS5340 has dual PLL frequency generators for generating the video clock (CLK0) and memory clock (CLK1) needed for graphics subsystems. Both these clocks are generated from a single 14.318 MHz crystal or can be driven by an external clock source. The chip includes the capacitors for the crystal and all the components needed for the PLL loop filters, minimizing board component count.

There are eight possible video clock, CLK0, frequencies (f0-f7) which can be selected by the external pins CS0-CS2. Pins are software selectable by setting a bit in the PLL control register. Two of these frequencies (f0-f1) are fixed and the other six (f2-f7) can be programmed for any frequency by writing appropriate parameter values to the PLL parameter registers. The default frequencies on power up are commonly used video frequencies (table 1). At power up, the frequencies can be selected by pins CS0-CS2. There are two programmable memory clock frequencies (fA, fB). On power up this frequency defaults to the frequency given in table 2. The memory clock transition between frequencies is smooth and glitch free if the transition is kept between the limits 45-65 MHz.

fA	(MHz)	VLCK Comments
f0	25.175	VGA0 (VGA Graphics) (fixed)
f1	28.322	VGA1 (VGA Text) (fixed)
f2	31.500	VESA 640 x 480 @72 Hz (programmable)
f3	36.00	VESA 800 x 600 @56 Hz (programmable)
f4	40.00	VESA 800 x 600 @60 Hz (programmable)
f5	44.889	1024 x 768 @43 Hz Interlaced (programmable)
f6	65.00	1024 x 768 @ 60 Hz, 640 x 480 Hi-Color @ 72 Hz (programmable)
f7	75.00	VESA 1024 x 768 @ 70 Hz, True Color 640 x 480 (programmable)

Table 1 - Video clock (CLK0) default frequency register (with a 14.318 MHz input)

fn	MHz	Comments
fA	45.00 MHz	Memory and GUI subsystem clock
fB	55.00 MHz	Memory and GUI subsystem clock

Table 2 - Memory Clock (CLK1) default frequency register

Microprocessor Interface

Below are listed the six microprocessor interface registers within the ICS5340, and the register addresses through which they can be accessed.

RS2	RS1	RS0	Register Name
0	0	0	Pixel Address (write mode)
0	1	1	Pixel Address (read mode)
0	0	1	Color Value
0	1	0	Pixel Mask
1	0	0	PLL Address (write mode)
1	0	1	PLL Parameter
1	1	0	Command
1	1	1	PLL Address (read mode)
0/HF	1	0	Command Register accessed by (hidden) flag after special sequence of events

Table 3 - Microprocessor Interface Registers

Asynchronous Access to Microprocessor Interface

Accesses to all registers may occur without reference to the high speed timing of the pixel bit stream being processed by the GENDAC. Data transfers between the color palette RAM and the Color Value register, as well as modifications to the Pixel Mask register, are synchronized to the Pixel Clock by internal logic. This is done in the period between microprocessor interface accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow the appropriate transfers or modifications to take place. Access to PLL address, PLL parameter and to the command register are asynchronous to the pixel clock.

The contents of the palette RAM can be accessed via the Color Value register and the Pixel Address registers.

Writing to the color palette RAM

To set a new color definition, a value specifying a location in the color palette RAM is first written to the Write mode Pixel Address register. The values for the red, green and blue intensities are then written in succession to the Color Value register. After the blue data is written to the Color Value register, the new color definition is transferred to the RAM, and the Pixel Address register is automatically incremented.

Writing new color definitions to a set of consecutive locations in the RAM is made easy by this auto-incrementing feature. First, the start address of the set of locations is written to the write mode Pixel Address register, followed by the color definition of that location. Since the address is incremented after each color definition is written, the color definition for the next location can be written immediately. Thus, the color definitions for consecutive locations can be written sequentially to the Color Value register without re-writing to the Pixel Address register each time.

Reading from the RAM

To read a color definition, a value specifying the location in the palette RAM to be read is written to the read mode Pixel Address register. After this value has been written, the contents of the location specified are copied to the Color Value register, and the Pixel Address register automatically increments.

The red, green and blue intensity values can be read by a sequence of three reads from the Color Value register. After the blue value has been read, the location in the RAM currently specified by the Pixel Address register is copied to the Color Value register and the Pixel Address again automatically increments. A set of color values in consecutive locations can be read simply by writing the start address of the set to the read mode Pixel Address register and then sequentially reading the color values for each location in the set. Whenever the Pixel Address register is updated, any unfinished color definition read or write is aborted and a new one may begin.

The Pixel Mask Register

The pixel address used to access the RAM through the pixel interface is the result of the bitwise ANDing of the

incoming pixel address and of the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colors without altering the video memory or the RAM contents. By partitioning the color definitions by one or more bits in the pixel address, such effects as rapid animation, overlays, and flashing objects can be produced.

The Pixel Mask register is independent of the Pixel Address and Color Value registers.

The Command Register

The Command register is used to select the various GENDAC color modes and to set the power down mode. On power up this register defaults to an 6-bit Pseudo Color mode. This register can be accessed by control pins RS2-RS0, or by a special sequence of events for graphics subsystems that do not have the control signal RS2. For graphic systems that do not have RS2, this pin is tied low and an internal flag (HF; Hidden Flag) is set when the pixel mask register is read four times consecutively. Once the flag is set, the following Read or Write to the pixel mask register is directed to the command register. The flag is reset for Read or Write to any register other than the pixel mask register. The sequence has to be repeated for any subsequent access to the command register.

The PLL Parameter Register

The CLK0 and CLK1 of the ICS5340 can be programmed for different frequencies by writing different values to the PLL parameter register bank. There are eight registers in the parameter register; seven are two bytes long and one (0E) is one byte long.

Writing to the PLL parameter register

To write the PLL parameter data, the corresponding address location is first written to the PLL address register. For software compatibility with other chips, two address registers are defined; the Write mode PLL address register and the Read mode PLL address register. They are actually a single Read/Write register in the ICS5340. The next PLL parameter write will be directed to the first byte of the address location specified by the PLL address register. The next Write to the parameter register will automatically be to the second byte of this register. At the end of the second Write the address is automatically incremented. For the one byte "0E" register the address location is incremented after the first byte Write. If this frequency is selected while programming, the output frequency will change at the end of the second Write.

Reading the PLL parameter register

To read one of the registers of the PLL parameter register the address value corresponding to the location is first written to the PLL address register. The next PLL parameter read will be directed to the first byte of the address location pointed by this index register. A next Read of the parameter register will automatically be the second byte of this register. At the end of the second Read, the address location is automatically incremented. The address register (0E) is incremented after the first byte Read.

Power Down Mode

When bit 0 in the Command register is high (set to 1) , the GENDAC enters the DAC power down mode. The DACs are turned off, and the data is retained in the RAM. It is possible to access the RAM, in which case the current will temporarily increase. While the RAM is being accessed, the current consumption will be proportional to the speed of the clock. There is no effect on either clock generator while in this mode.

Power Supply

As a high speed CMOS device, the ICS5340 may draw large transient currents from the power supply, it is necessary to adopt high frequency board layout and power distribution techniques to ensure proper operation of the GENDAC. Please refer to the suggested layout on page 27.

To supply the transient currents required by the ICS5340, the impedance in the decoupling path should be kept to a minimum between the power supply pins V_{DD} and GND. It is recommended that the decoupling capacitance between V_{DD} and GND should be a 0.1μF high frequency capacitor, in parallel with a large tantalum capacitor with

a value between 22µF and 47µF. A ferrite bead may be added in series with the positive supply to form a low pass filter and further improve the power supply local to the GENDAC. It will also reduce EMI.

The combination of series impedance in the ground supply to the GENDAC, and transients in the current drawn by the device will appear as differences in the GND voltages to the GENDAC and to the digital devices driving it. To minimize this differential ground noise, the impedance in the ground supply between the GENDAC and the digital devices driving it should be minimized.

Digital Output Information

The PCB trace lines between the outputs of the TTL devices driving the GENDAC and the input to the GENDAC behave like low impedance transmission lines driven from a low impedance transmission source and terminated with a high impedance. In accordance with transmission line principles, signal transitions will be reflected from the high impedance input to the device. Similarly, signal transitions will be inverted and reflected from the low impedance TTL output. Line termination is recommended to reduce or eliminate the ringing, particularly the undershoot caused by reflections. The termination may either be series or parallel.

Series termination is the recommended technique to use. It has the advantages of drawing no DC current and of using fewer components. Series termination is accomplished by placing a resistor in series with the signal at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and ensures that any signal incident on the TTL output is not reflected.

To minimize reflections, some experimentation will have to be done to find the proper value to use for the series termination. Generally, a value around 100Ω will be required. Since each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. Therefore, the proper value of resistance should be found empirically.

Functional Description

This section describes the register address and bit definition for RAMDAC and the Frequency Synthesizer sections.

Color Palette Command Register

(RS0-RS2 = 011)
(RS0-RS1 = 01 with hidden flag)

By setting bits in the command register the ICS5340 can be programmed for different color modes and can be powered down for low power operation.

7	6	5	4	3	2	1	0
Color Mode				Reserved = 0			Snooze
2	1	0	3				

Table 3 - Command Registers

Bit 7-4 **Color Mode Select**
These three bits select the Color Mode of RAMDAC operation as shown in the following table 4 (default is 0 at power up):

Bit 3 - 1 **(Reserved)**

Bit 0 **Power Down Mode of RAMDAC**
When this bit is set to 0 (default is 0), the device operates normally. If this bit is set to 1, the power and clock to the Color Palette RAM and DACs are turned off. The data in the Color Palette RAM are still preserved. The CPU can access without loss of data by internal automatic clock start/stop control. The DAC outputs become the same as BLANK* (sync) level output during power down mode. This bit does not effect the PLL clock synthesizer function.

8-BIT INTERFACE

Mode Number	CM3 (CR4)	CM2 (CR7)	CM1 (CR6)	CM0 (CR5)	Color Mode	Clock Cycles/ Pixel Bits
0	0	0	0	0	8-Bit Pseudo Color with Palette (Default)	1
1	0	0	0	1	15-Bit Direct Color with Bypass (Hi-Color)	2
3	0	0	1	0	24-Bit True Color with Bypass (True Color)	3
2	0	0	1	1	16-Bit Direct Color with Bypass (XGA)	2
1	0	1	0	0	15-Bit Direct Color with Bypass (Hi-Color)	2
1	0	1	0	1	15-Bit Direct Color with Bypass (Hi-Color)	2
2	0	1	1	0	16-Bit Direct Color with Bypass (XGA)	2
3	0	1	1	1	24-Bit True Color with Bypass (True Color)	3

16-BIT INTERFACE

Mode Number	CM3 (CR4)	CM2 (CR7)	CM1 (CR6)	CM0 (CR5)	Color Mode	Clock Cycles/ Pixel Bits
4	1	0	0	0	Muxed 16-Bit Pseudo Color with Palette	1/2
5	1	0	0	1	15-Bit Direct Color with Bypass (Hi-Color)	1
6	1	0	1	0	16-Bit Direct Color with Bypass (XGA)	1
7	1	0	1	1	24-Bit Direct Color with Bypass (True-Color)	2
8	1	1	0	0	24-Bit Packed Direct Color with Bypass (True-Color)	3/2
	1	1	0	1	Reserved	
	1	1	1	0	Reserved	
	1	1	1	1	Reserved	

Table 4 - Color Mode Select

Color Modes

The nine selectable color modes are described here. Modes 0 - 3 are 8-bit interfaces with P0-P7 bits, P8-P15 are Don't Care bits.

Mode 0: 8-bit Pseudo Color (one clock per pixel). This mode is the 8-bit per pixel Pseudo Color mode. In this mode, inputs P0-P7 are the pixel address for the color palette RAM and are latched on the rising edge of every PCLK. This is the default mode on power up and it is selected by setting bits CR7-CR4 to 0000 . There are three clock cycles pipe line delays from input to DAC output.

8-bit Pseudo Color Mode

PIXEL BYTE							
P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0
PIXEL ADDRESS							

Mode 1: (15-bit per color bypassHi-Color mode).
This mode is the 15-bit per pixel bypass mode. In this mode, inputs P0-P7 are the color DATA and are input directly to the DAC, bypassing the color palette. The two bytes of data is latched in two successive PCLK rising edges. ICS5340 supports only the two clock mode and does not support the mode where the data are latched on the rising and the falling edges. For compatibility, the 15/16 one clock modes are selected as two clock modes in this chip. The low-byte, high byte synchronization is internally done by the rising edge of BLANK*. Each color is 5-bit wide and is packed into two bytes as shown below. This mode can be selected by setting bits CR7-CR4 to 0010, 1000 or 1010.

15-Bit Color Mode 1 Pixel Description

3LSB = set to zero

SECOND BYTE								FIRST BYTE							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
X	7	6	5	4	3	7	6	5	4	3	7	6	5	4	3
	RED					GREEN					BLUE				

Mode 2: (16-bit per pixel bypass XGA mode).
This mode is the 16-bit per pixel bypass mode and the P0-P7 inputs to go to the DAC directly, bypassing the color palette. The 2 bytes data is latched on two successive rising edges and the low-byte, high-byte synchronization is internally done by the rising edge of BLANK*. In this mode, blue and red colors are 5 bits wide and green is 6 bits wide. The 2 bytes of data is packed as shown below. This mode can be selected by setting bits CR7-CR4 to 0110 or 1100.

16-Bit Color Mode 2 Pixel Description

2LSB = set to zero (green)
3LSB = set to zero (blue, red)

SECOND BYTE								FIRST BYTE							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
7	6	5	4	3	7	6	5	4	3	2	7	6	5	4	3
RED					GREEN						BLUE				

Mode 3: (24-bit per pixel True Color Mode).
This mode is the 24-bit per pixel bypass mode. The three bytes of data are latched on three successive PCLK edges and the first byte is synchronized by the rising edge of BLANK*. In this mode, each of the colors are 8-bit wide and the DAC is an 8-bit wide DAC. The first byte is blue followed by green and red. This mode can be selected by setting bits CR7-CR4 to 0100 or 1110. The DAC outputs changes every three cycles and the pipeline delay from the first byte to output is five cycles.

24-bit Color Mode 3 Pixel Description

THIRD BYTE								SECOND BYTE								FIRST BYTE							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RED								GREEN								BLUE							

Modes 4 - 8 use the 16-bit pixel interface.

Mode 4: (8-bit Pseudo Color two pixels per clock) In this mode, inputs P0-P15 are latched on the rising edge of every PCLK. P0-7 and P8-P15 are used for successive addresses for the palette RAM using an internal clock that runs at twice the PCLK frequency. The DAC outputs change twice for every PCLK and the pipeline delay from the first word to output is one and a one half cycles. This mode can be selected by setting bits CR7-CR4 to 0001.

Multiplexed 8-bit Pseudo Color Word Mode 4 Pixel Description

PIXEL WORD															
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	2	0
2nd PIXEL ADDRESS								1st PIXEL ADDRESS							

Mode 5: (16-bit pixel interface, 15-bit per color bypass Hi-Color Mode) In this mode inputs P0-P15 are the color Data and are input directly to the DAC, bypassing the color palette. The Data is latched by the rising edge of PCLK and is pipelined to the DAC. The pipeline delay from input to DAC output is 3 PCLK cycles. Each color is 5-bit wide as shown below. This mode is selected by setting bits CR7-CR4 to 0011.

15-Bit Color Word Mode 5 Pixel Description

3LSB = set to zero

P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	7	6	5	4	3	7	6	5	4	3	7	6	5	4	3
	RED					GREEN					BLUE				

Mode 6: (16-bit pixel interface, 16-bit per color bypass XGA mode) In this mode input P0-P15 are the color Data and are input directly to the DAC bypassing the color Palette. The Data is latched by the rising edge of PCLK and is pipelined to the DAC. The pipeline delay, from input to DAC output, is 3 PCLK cycles. In this mode Blue and Red colors are 5 bits wide, and Green is 6 bits wide. This mode is selected by selecting bits CR7-CR4 to 0101.

16-Bit Color Word Mode 6 Pixel Description

2LSB = set to zero (GREEN)
3LSB = set to zero (BLUE, RED)

P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	7	6	5	4	3	2	7	6	5	4	3
RED					GREEN						BLUE				

Mode 7: (16-bit pixel interface, 24-bit per color bypass TRUE color mode) In this mode inputs P0-P15 are the color Data and are input directly to the DAC bypassing the color Palette. Two words are latched on two successive rising edge of PCLK to form the 24-bit DAC input. The first word and the lower byte of the second word form the 24-bit pixel input to the DAC. The higher byte of the second word is ignored. The low and high word synchronization is internally done by the rising edge of the BLANK*. The pipeline delay from latching of first word to DAC output is 4 cycles and each pixel is 2 pixel clocks wide. In this mode, each of the colors are 8-bits wide and the DAC is 8-bit wide DAC. The first byte is Blue followed by Green and Red. This mode is selected by setting bits CR7-CR4 to 0111.

24-Bit Direct Color Word Mode 7 Pixel Description

FIRST WORD															
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
GREEN								BLUE							

SECOND WORD															
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
								RED							

Mode 8: (16-bit pixel interface packed 24-bit per color bypass TRUE color mode) In this mode inputs P0-P15 are the color Data and are input directly to the DAC bypassing the color Palette. Three words are latched on three successive rising edge of PCLK to form two successive 24-bit DAC inputs. The 16-bit first word and the lower byte of the second word from the first 24-bit pixel input and the second byte of the second word with the 16 bits of the third word from the second 24-bit pixel input. This cycle repeats every 3 cycles. The three word synchronization is internally done by the rising edge of BLANK*. The pipeline delay from latching of first word to DAC output is 3 ½ cycles and each of the colors are 8-bits wide and DAC is 8-bit wide DAC. The first byte is Blue followed by Green and Red. Repeats. This mode is selected by setting bits CR7-CR4 to 1001.

Packed 24-bit Word Mode 8 Pixel Description
1st DAC Cycle

SECOND WORD								FIRST WORD															
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RED								GREEN								BLUE							

2nd DAC Cycle

THIRD WORD																SECOND WORD							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RED								GREEN								BLUE							

Frequency Generators

The ICS5340 clock synthesizer can be reprogrammed through the microprocessor interface for any set of frequencies. This is done by writing appropriate values to the PLL Parameter Register Bank (table 5).

PLL Address Registers

The address of the parameter register is written to the PLL address registers before accessing the parameter register. This register is accessed by register select pins RS2-RS0 = 100 or 111.

7	6	5	4	3	2	1	0
PLL REGISTER ADDRESS							
7	6	5	4	3	2	1	0

PLL Parameters Registers

There are sixteen registers in the PLL parameter register (table 5). Registers 00 to 07 are for the CLK0 selectable frequency list, Register 0A for CLK1 programmable frequency and register 0E is the PLL CLK0 control register.

Index	R/W	Register	
00	R/-	CLK0 f0 PLL Parameters	(2 bytes)
01	R/-	CLK0 f1 PLL Parameters	(2 bytes)
02	R/W	CLK0 f2 PLL Parameters	(2 bytes)
03	R/W	CLK0 f3 PLL Parameters	(2 bytes)
04	R/W	CLK0 f4 PLL Parameters	(2 bytes)
05	R/W	CLK0 f5 PLL Parameters	(2 bytes)
06	R/W	CLK0 f6 PLL Parameters	(2 bytes)
07	R/W	CLK0 f7 PLL Parameters	(2 bytes)
08	R/-	(Reserved) = 0	(2 bytes)
09	R/-	(Reserved) = 0	(2 bytes)
0A	R/W	CLK1 fA PLL	(2 bytes)
0B	R/W	CLK1 fB PLL	(2 bytes)
0C	R/-	(Reserved) = 0	(2 bytes)
0D	R/-	(Reserved) = 0	(2 bytes)
0E	R/W	PLL Control Register	(1-byte)
0F	R/-	(Reserved) = 0	(2-byte)

Table 5 - PLL Parameter Registers

PLL CONTROL REGISTER

Bits in this register determine internal or external CLK0 select.

7	6	5	4	3	2	1	0
(RV) =0	(RV) =0	ENBL INCS	CLK1 SEL	(RV) =0	INTERNAL SELECT		
					X	X	X

Bit 7,6, 3 Reserved.

Bit 5 Enable Internal Clock Select (INCS) for CLK0. When this bit is set to 1, the CLK0 output frequency is selected by bit 2 - 0 in this register. External pins CS0 - CS2 are ignored.

Bit 4 Clk1 Select
When this bit is set to 0, fA is selected. When it is set to 1, fB is selected. Default is 0, fA selected, at power up.

Bit 2 - 0 Internal Clock Select for CLK0 (INCS).
These three bits selects the CLK0 output frequency if bit 5 of this register is on. They are interpreted as an octal number, n, that selects fn. Default selects f0.

PLL Data Registers

The CLK0 and CLK1 input frequency is determined by the parameter values in this register. These are two bytes registers; the first byte is the M-byte and the second is the N-byte.

M-Byte PLL Parameter Input

The M-byte has a 7-bit value (1-127) which is the feedback divider of the PLL.

7	6	5	4	3	2	1	0
Reserved	M-Divider Value						
=0	X	X	X	X	X	X	X

N-Byte PLL Parameter Input

The N-byte has two values. N1 sets a 5-bit value (1-31) for the input pre scalar and N2 is a 2-bit code for selecting 1, 2, 4, or 8 post divide clock output.

7	6	5	4	3	2	1	0
Reserved	N2-Code		N1-Divider Value				
=0	X	X	X	X	X	X	X

N2 Post Divide Code

If mode 4 is set in the command register, CR7-CR4 equal 0001, N2 code must be 10.

N2 code	Divider
00	1
01	2
10	4
11	8

The block diagram of the PLL clock synthesizer is shown in figure 3.

Based on the M and N values, the output frequency of the clocks is given by the following equation:

$$F_{out} = \frac{(M+2) \text{ x } F_{ref}}{(N1+2) \text{ x} 2^{N2}}$$

M and N values should be programmed such that the frequency of the VC0 is within the optimum range for duty cycle, jitter and glitch free transition. Optimum duty cycle is achieved by programming N2 for values greater than one. See the next section for programming example.

Programming Example

Suppose an output frequency of 25.175 MHz is desired. The reference crystal is 14.318 MHz. The VCO should be targeted to run in the 100 to 180 MHz range, so choosing a post divide of 4 gives a VCO frequency of :

4 X 25.175=101.021 MHz

From the table in the previous section, we find N2 = 2 Substituting $F_{REF} = 14.318$ and $2^{N2} = 4$ into the equation on page 17:

$$\left(\frac{25.175}{14.318}\right) \cdot 4 = \frac{(M+2)}{(N1+2)}$$

by trial and error:

$$\left(\frac{25.175}{14.318}\right) \cdot 4 \approx \frac{127}{18}$$

so $M + 2 = 127$ $M = 125$

$N1 + 2 = 18$ $N1 = 16$

so the registers are:

M = 125d = 1 1 1 1 1 0 1 b

N = 0 & N2 code & N1 = 0 & 1 0 & 1 0 0 0 0

N = 0 1 0 1 0 0 0 0 b

Additional Information on Programming the Frequency Generator section of the GENDAC

When programming the GENDAC PLL parameter registers, there are many possible combinations of parameters which will give the correct output frequency. Some combinations are better than others, however. Here is a method to determine how the registers need to be set:

The key guidelines come from the operation of the phase locked loop, which has the following restrictions:

1. $2 \text{ MHz} < f_{REF} < 32 \text{ MHz}$

   This refers to the input reference frequency. Most users simply connect a 14.318 MHz crystal to the crystal inputs, so this is not a problem.

2. $600 \text{ kHz} < \frac{f_{REF}}{(N1+2)} \le 8 \text{ MHz}$

   This is the frequency input to the phase detector.

3. $60\text{ MHz} \le \frac{(M+2)}{(N1+2)} f_{ref} \le 270\text{ MHz}$

   This is the VCO frequency. In general, the VCO should run as fast as possible, because it has lower jitter at higher frequencies. Also, running the VCO at multiples of the desired frequency allows the use of output divides, which tends to improve the duty cycle.

4. f_{CLK0} and $f_{CLK1} \le 135$ MHz

   This is the output frequency.

These rules lead to the following procedure for determining the PLL parameters, assuming rules 1 and 4 are satisfied.

A. Determine the value of N2 (either 1, 2, 4 or 8) by selecting the highest value of N2, which satisfies the condition N2* $f_{CLK} \le 270$ MHz

B. Calculate $\frac{(M+2)}{(N1+2)} = \frac{2^{N2} f_{out}}{f_{ref}}$

C. Now (M+2) and (N1+2) must be found by trial and error. With a 14.318 MHz reference frequency, there will generally be a small output frequency error due to the resolution limit of (M+2) and (N1+2). For a given frequency tolerance, several different (M+2) and (N1+2) combinations can usually be found. Usually, a few minutes trying out numbers with a calculator will produce a workable combination. Multiplying possible values of (N1+2) by the desired ratio will indicate approximately the value of M. This method is shown in the example below. A program could be written to try all possible combinations of (M+2) and (N1+2) (3937 possible combinations), discard those outside error band, and select from those remaining by giving preference to ratios which use lower values of (M+2). Lower values of (M+2) and (N1+2) provide better noise rejection in the phase locked loop.

Example: Suppose we are using a 14.318 MHz reference crystal and wish to output a frequency of 66 MHz with an error of no greater than 0.5%. What are the values of the PLL data registers?

A. 66*8 = 528 > 250 VCO speed too high
66*4 = 264 > 250 VCO speed too high
66*2 = 132 < 250 VCO speed OK, N2 = 2, N2 code = 01 from table on page 17 of the data sheet.

B. 132/14.31818 = 9.219
This is the desired frequency multiplication ratio.

C. Setting (N1+2) = 3,4,...12, 13 and performing some simple calculations yields the following table: (Note that N1 cannot be 0).

(N1+2)	(N1+2)*9.219	rounded (=M+2)	Actual Ratio	Percent Error
3	27.657	28	9.33	-1.23
4	36.876	37	9.25	-0.34
5	46.095	46	9.20	0.21
6	55.314	55	9.17	0.57
7	64.533	65	9.29	-0.72
8	73.752	74	9.25	-0.34
9	82.971	83	9.22	-0.03
10	92.19	92	9.20	0.21
11	101.409	101	9.18	0.40
12	110.628	111	9.25	-0.34
13	119.847	120	9.23	-0.13

The ratio 83/9 is closest. Thus (N2+2) = 9; N2=7. (M+2) = 83; M = 81. The M-byte PLL parameter word is simply 81 in binary, plus bit 7 (which must be set to 0), or 01010001. The N-byte PLL parameter word is N2 code (01) concatenated with 5 bits of N2 in binary (00111), or 00100111. Once again, bit 7 must be zero.

We have chosen the combination with the least frequency error, but several other combinations are within the 0.5% tolerance. Because the lowest value of (M+2) offers the best damping, the 37/4 combination will have the best power supply rejection. This results in lower jitter due to external noise.

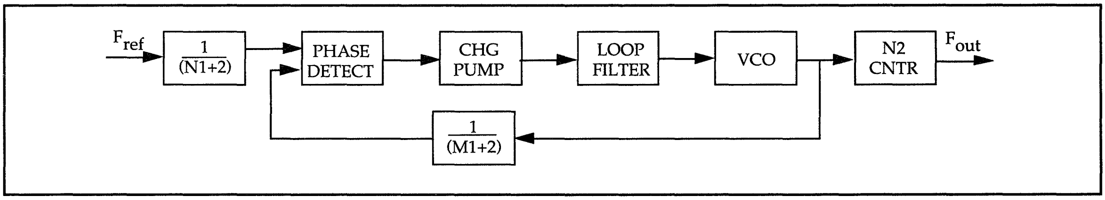
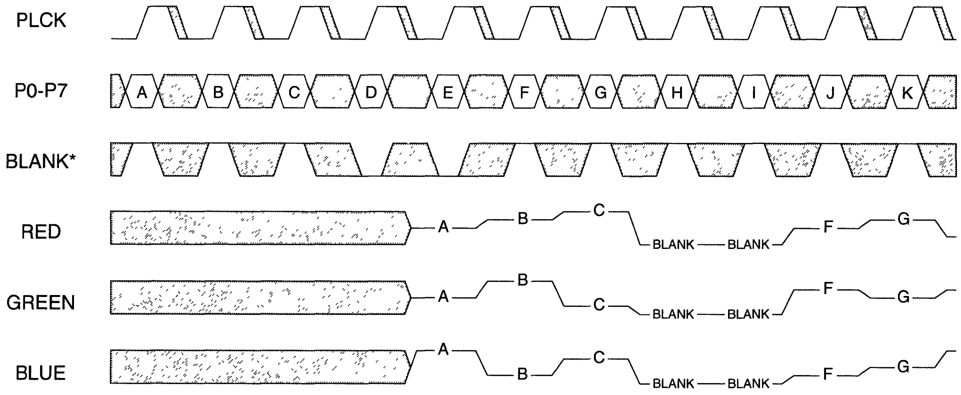


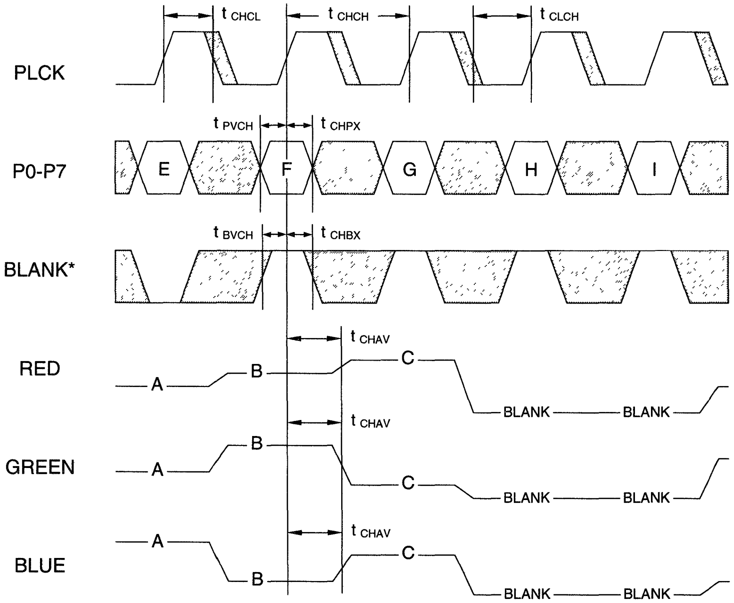
Figure 3 - PLL Clock Synthesizer Block Diagram

External Select			(Internal Select PLL Control Register)			
CS2	CS1	CS0	BIT 2	BIT 1	BIT 0	CLK 0 Frequency
0	0	0	0	0	0	f0
0	0	1	0	0	1	f1
0	1	0	0	1	0	f2
0	1	1	0	1	1	f3
1	0	0	1	0	0	f4
1	0	1	1	0	1	f5
1	1	0	1	1	0	f6
1	1	1	1	1	1	f7

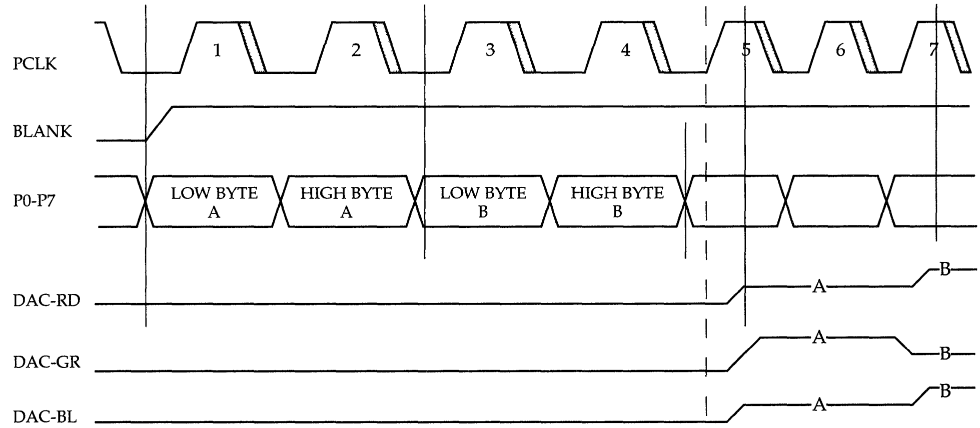
Video Clock Selection Table



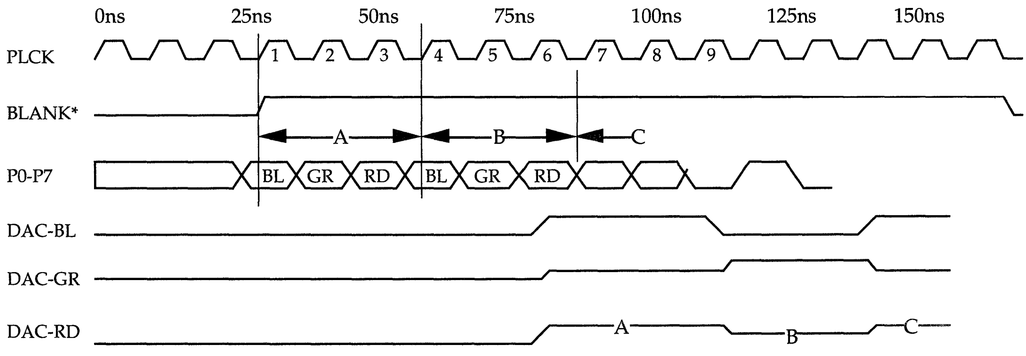
System Timing - Pseudo Color, Mode 0



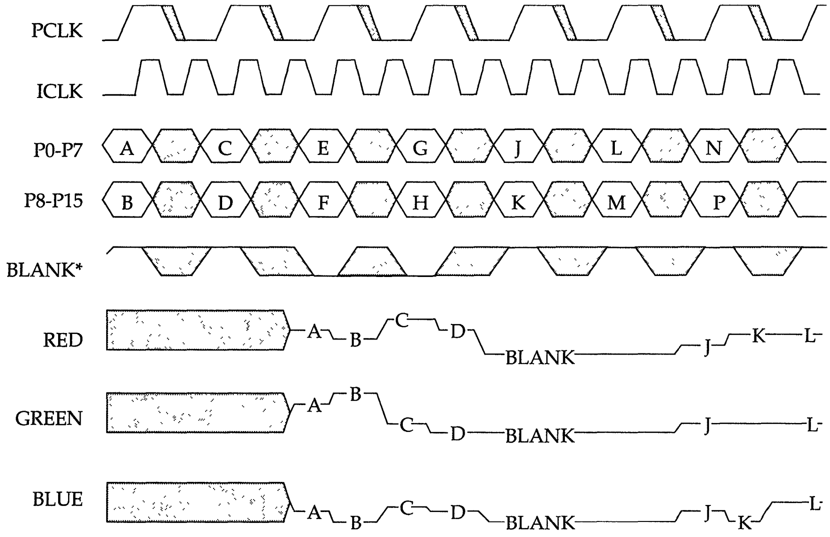
Detailed Timing Specifications - Pseudo Color, Mode 0



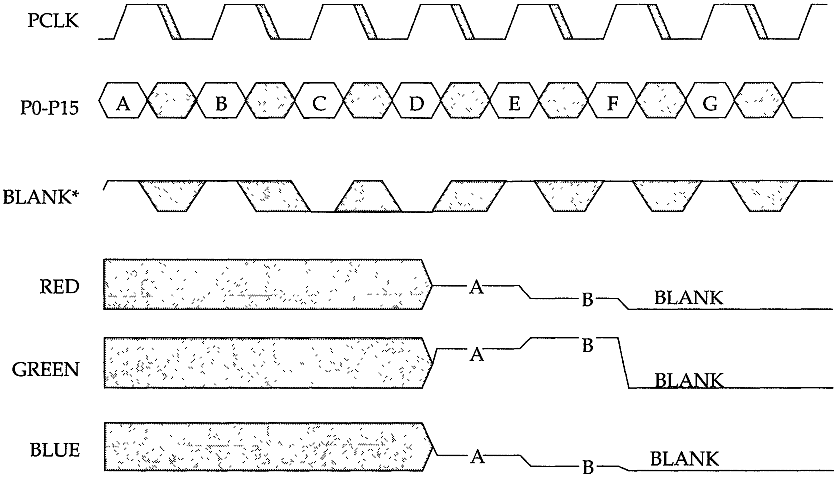
System Timing Bypass - 15 (5/5/5) and 16 (5/6/5) Modes 1, 2



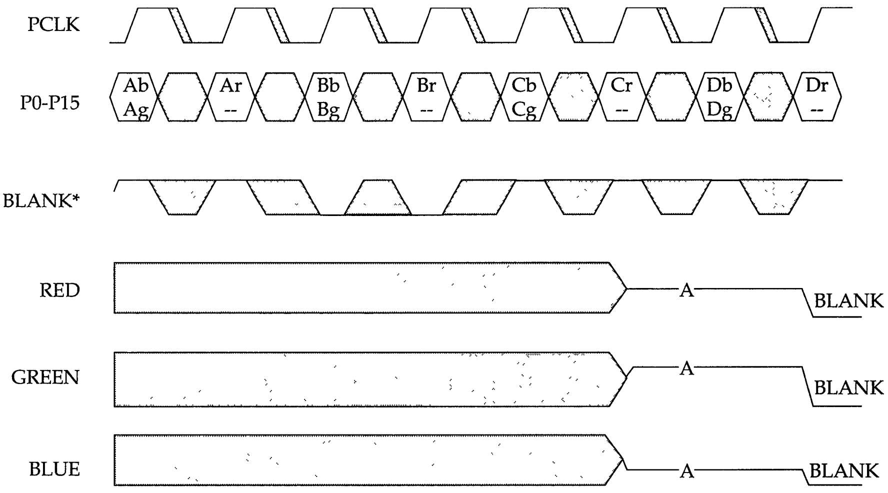
System Timing Bypass True Color 24 (8,8,8) Mode 3



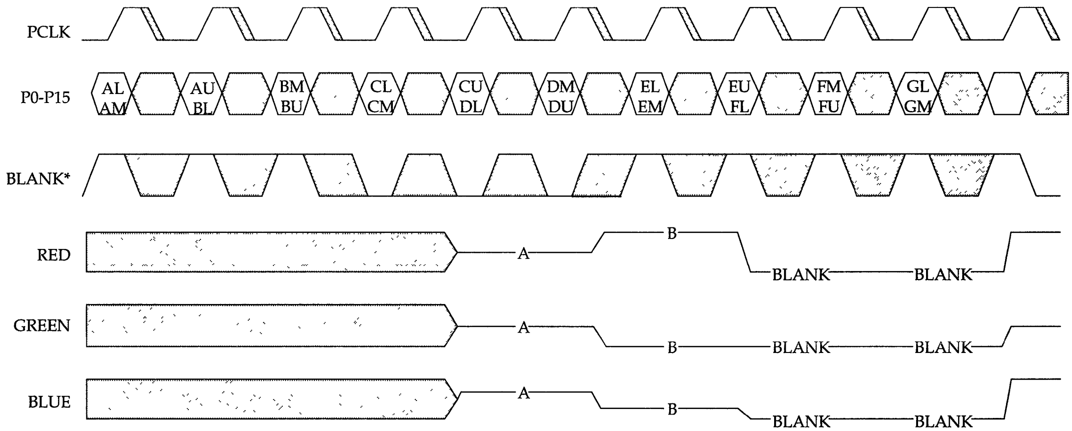
System Timing - Multiplexed 8-bit Pseudo Color, Mode 4



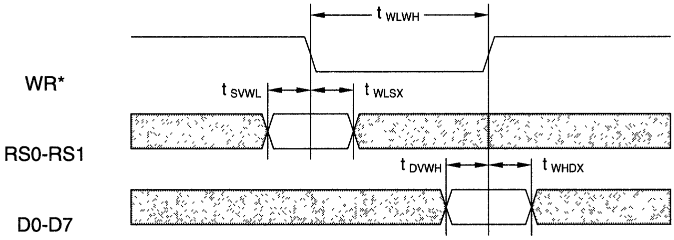
System Timing - 16-bit Color, Mode 5 (5,5,5) and 6 (5,6,5)



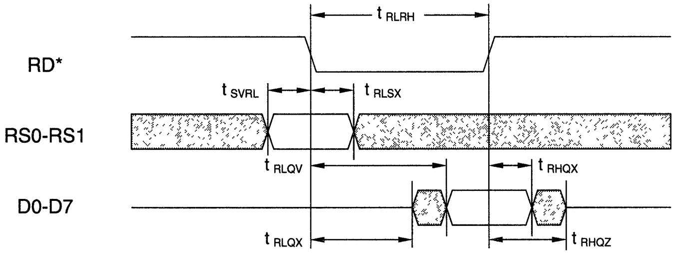
System Timing - 16-bit Direct True Color, Mode 7



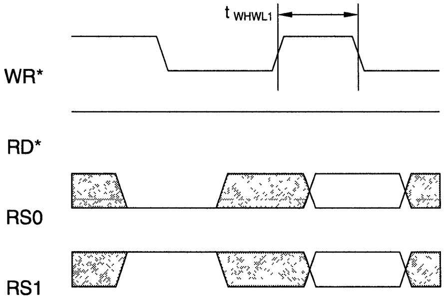
System Timing - 24-bit Packed Color, Mode 8



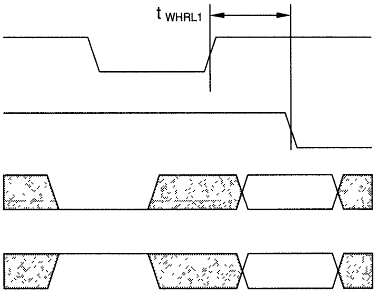
Basic Write Cycle Timing



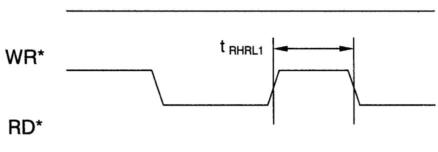
Basic Read Cycle Timing



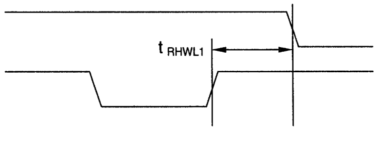
Write to Pixel Mask Register Followed by Write



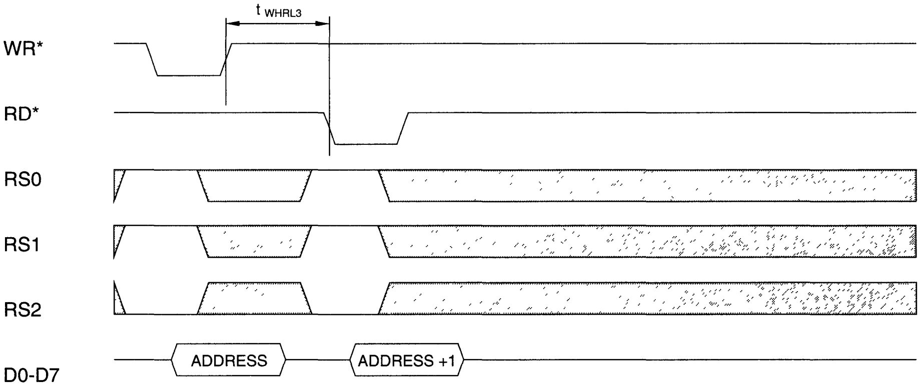
Write to Pixel Mask Register Followed by Read



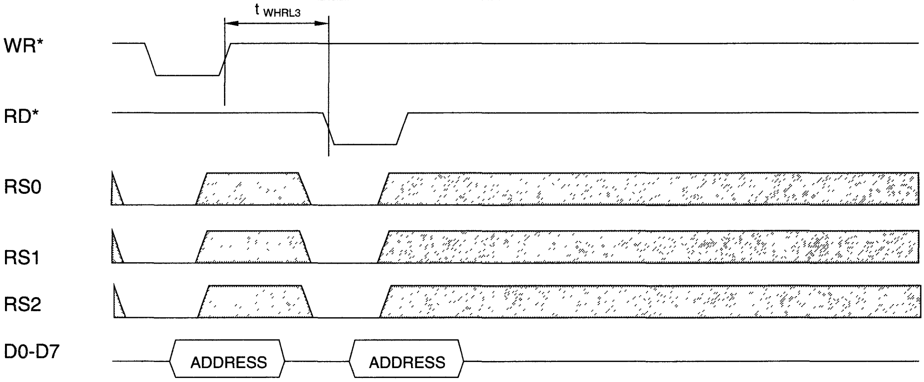
Read from Pixel or Pixel Address Register (Read or Write) followed by Read



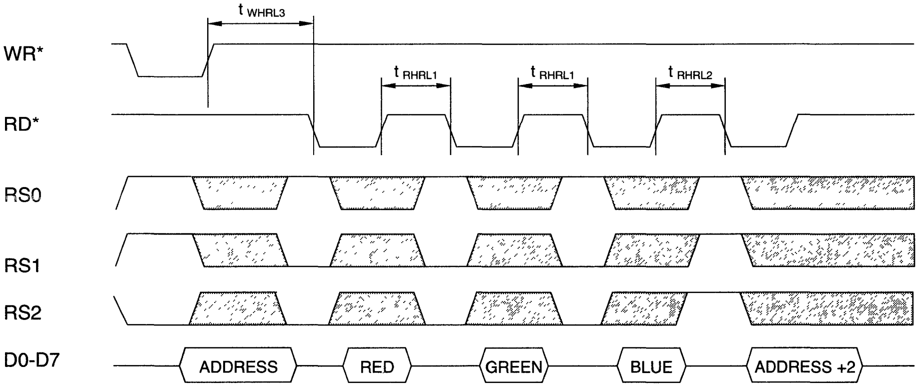
Read from Pixel or Pixel Address Register (Read or Write) followed by Write



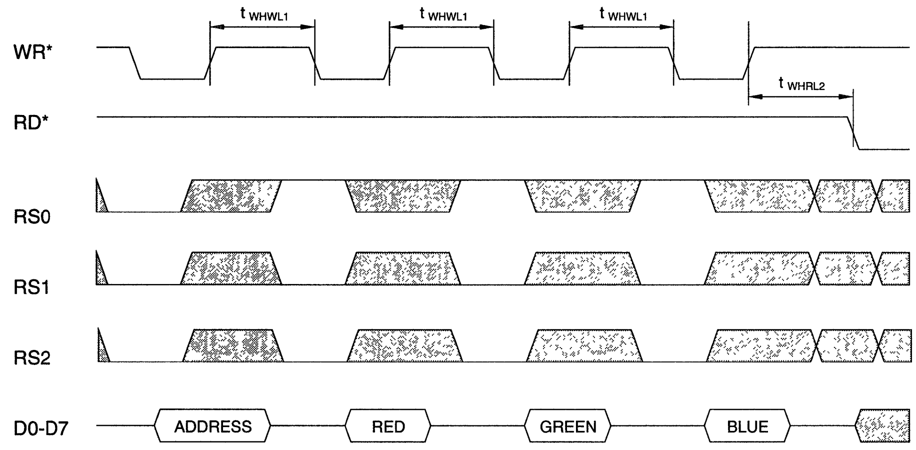
Write and Read Back Pixel Address Register (Read Mode)



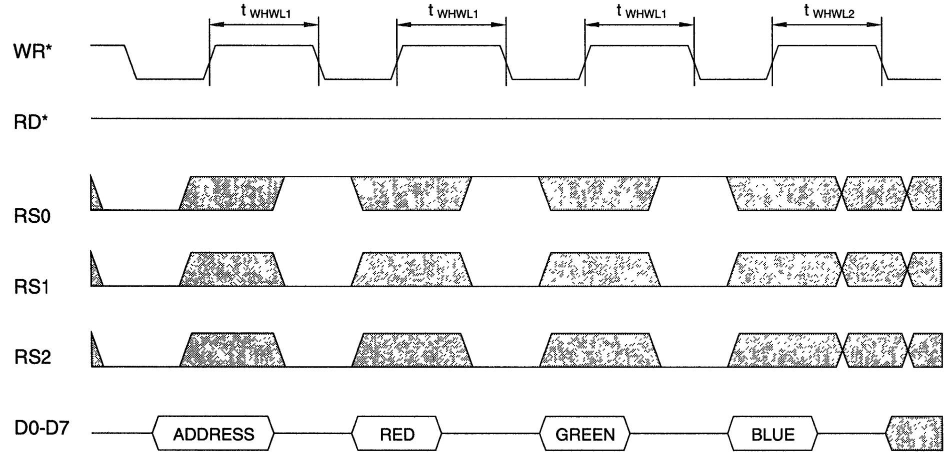
Write and Read Back Pixel Address Register (Write Mode)



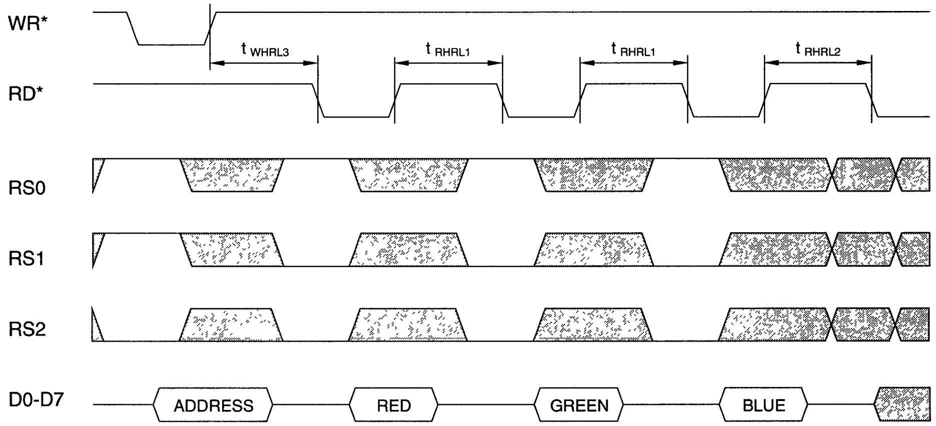
Read Color Value then Pixel Address Register (Read Mode)



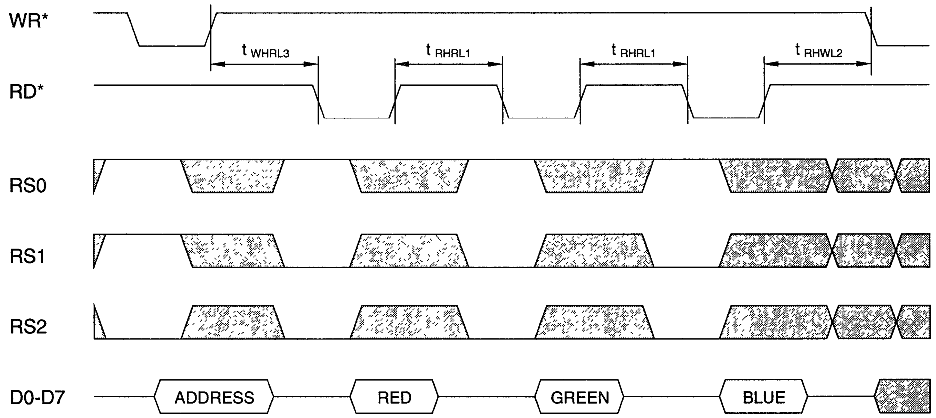
Color Value Write followed by any Read



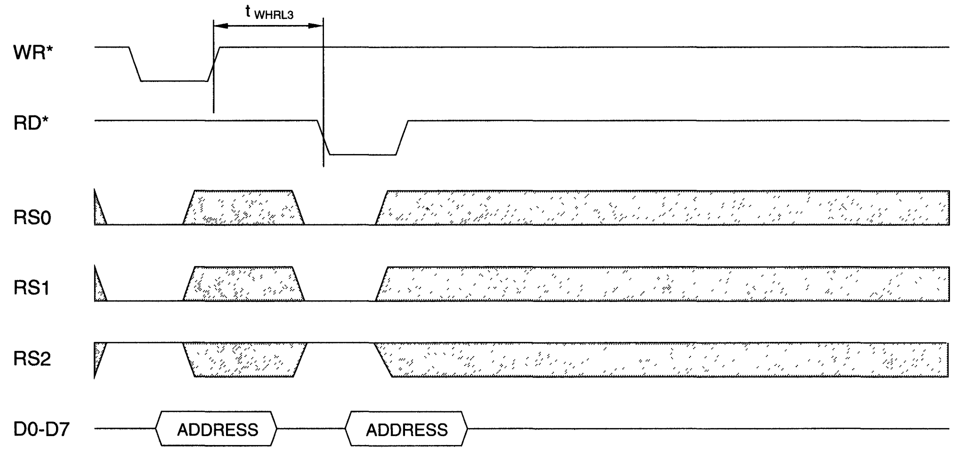
Color Value Write followed by any Write



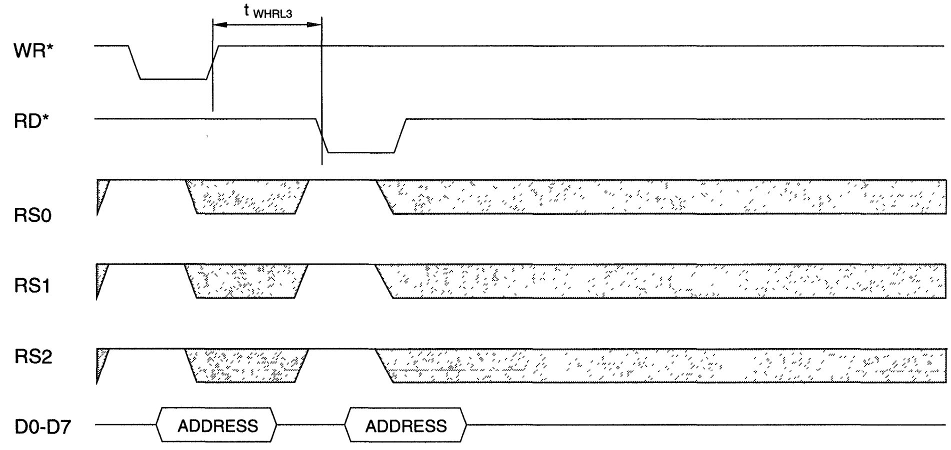
Color Value Read followed by any Read



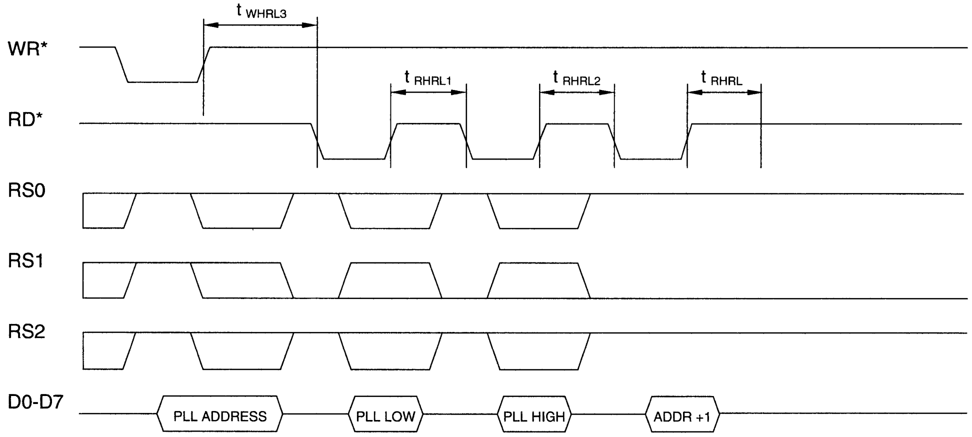
Color Value Read followed by any Write



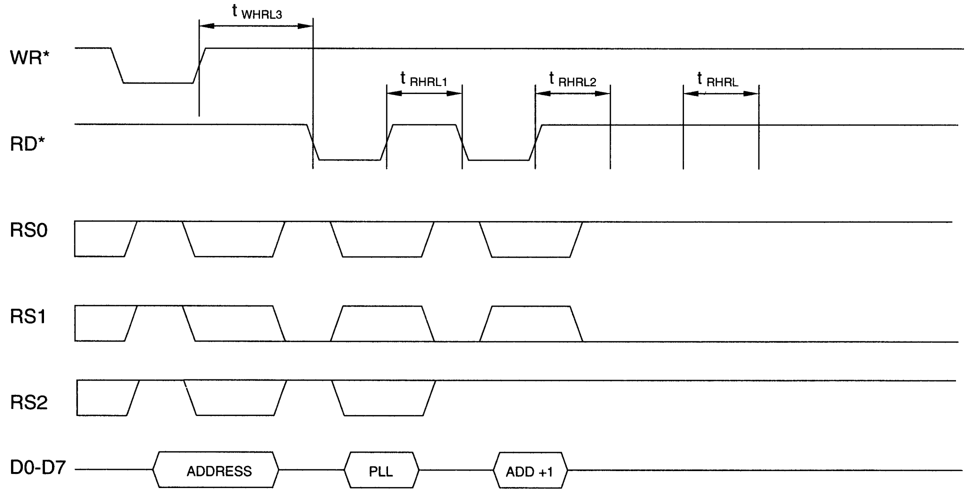
Write and Read back PLL Address Register (Write Mode)



Write and Read back PLL Address Register (Read Mode)

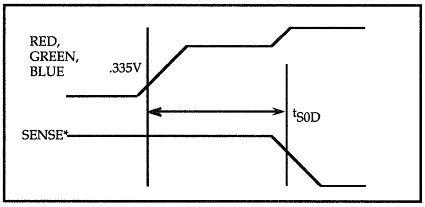


Read Two bytes PLL Register then PLL Address Register



Read One Byte PLL Register then PLL Address Register

Monitor SENSE Signal

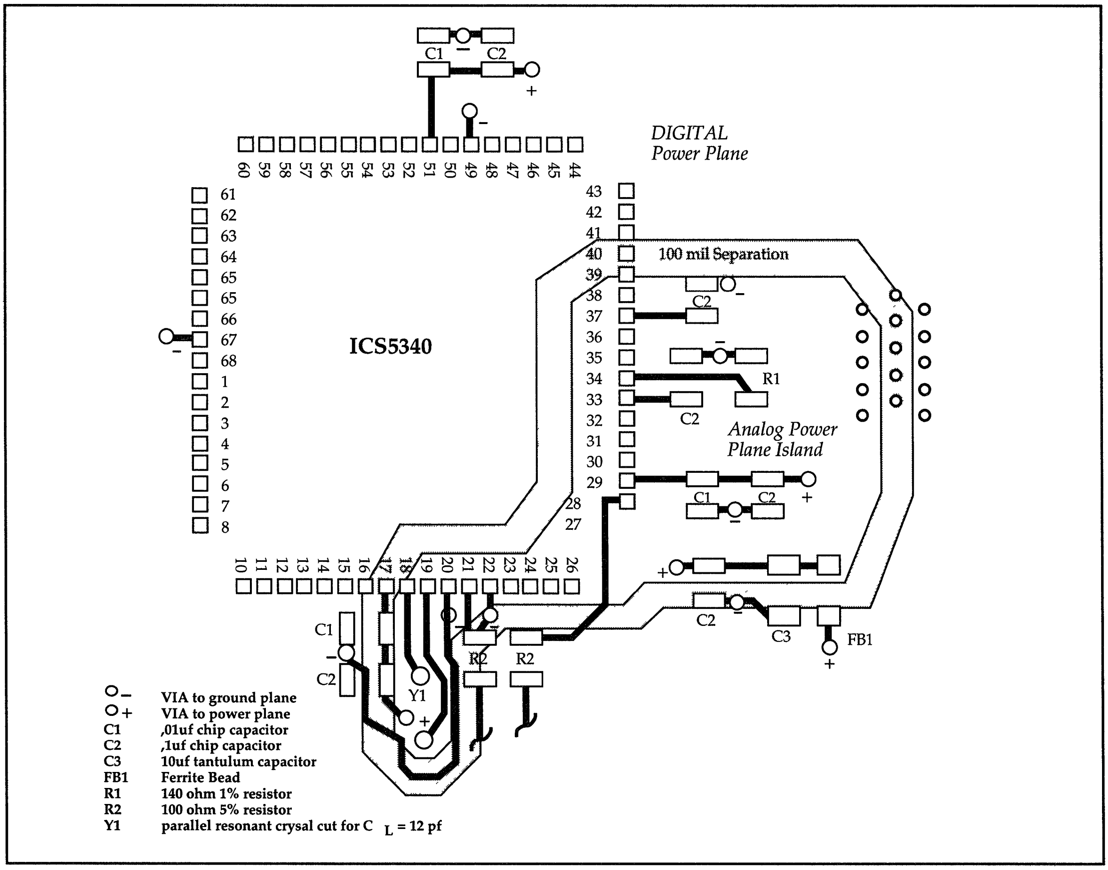


The high performance of which the ICS5340 GENDAC is capable is dependent on careful PC board layout. The use of a four layer board (internal power and ground planes, signals on the two surface layers) is recommended. The layout below shows a suggested configuration.

The ground plane is continuous, but the power plane is separated into analog and digital sections as shown Power is supplied to the analog power plane through the ferrite bead, and bypassed at the power entry point by C3, a 10 µF tantalum capacitor. These high current connections should have multiple vias to the ground and power planes, if possible. Power connections should be connected to the analog or digital power plane, as shown in the diagram. Power pins 5 and 29 should be connected to digital power, power pins 20 and 24 to analog power. Decoupling capacitors (indicated by C1 and C2) should be placed as close to the GENDAC as possible.

The analog and digital I/O lines are not shown. Analog signals (DAC outputs, Vref, Rset) should only be routed above the analog power plane. Digital signals should only be routed above the digital power plane.

Recommended Layout



Ordering Information

ICS5340V

Example:

ICS XXXX M

Package Type
V=PLCC
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Integrated
Circuit
Systems, Inc.

ICS5341
GENDAC
Advance Information

16-Bit Integrated Clock-LUT-DAC

General Description

The ICS5341 GENDAC is a combination of dual programmable clock generators, a 256 x 18-bit RAM, and a triple 8-bit video DAC. The GENDAC supports 8-bit pseudo color applications, as well as 15-bit, 16-bit and 24-bit True Color bypass for high speed, direct access to the DACs.

The RAM makes it possible to display 256 colors selected from a possible 262, 144 colors. The dual clock generators use Phase Locked Loop (PLL) technology to provide programmable frequencies for use in the graphics subsystem. The video clock contains 8 frequencies, 6 of which are programmable by the user. The memory clock has two programmable frequency locations.

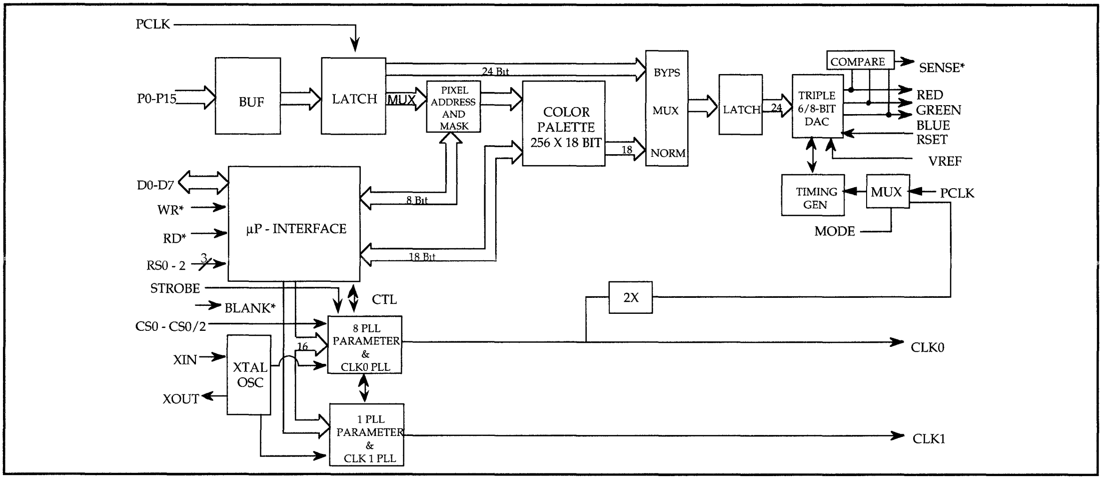
The three 8-bit DACs on the ICS5341 are capable of driving singly or doubly-terminated 75Ω loads to nominal 0 - 0.7 volts at pixel rates up to 135 MHz. Differential and integral linearity errors are less than 1 LSB over full temperature and V_{DD} ranges. Monotonicity is guaranteed by design. On-chip pixel mask register allows displayed colors to be changed in a single write cycle rather than by modifying the color palette.

ICS is the world leader in all aspects of frequency (clock) generation for graphics, using patented techniques to produce low jitter video timing.

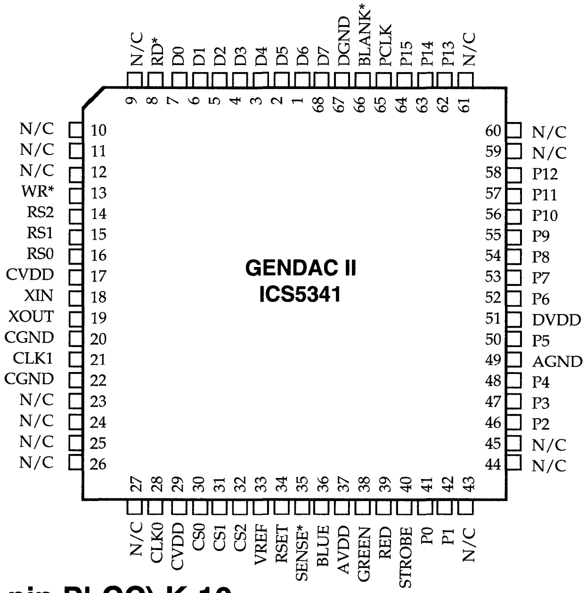
Features

- **Designed for compatibility with Tseng Labs VGA controllers**
- **Triple video DAC, dual clock generator, and a color palette**
- **24, 16, 15, or 8-bit pseudo color pixel mode supports True Color, Hi-Color, and VGA modes**
- **High speed 256 x 18 color palette (135 MHz) with bypass mode and 8-bit DACs**
- **Two fixed, six programmable video (pixel) clock frequencies (CLK0)**
- **Two programmable memory (controller) clock frequency (CLK1)**
- **DAC power down in blanking mode**
- **Anti-sparkle circuitry**
- **On-chip loop filters reduce external components**
- **Standard CPU interface**
- **Single external crystal (typically 14.318 MHz)**
- **Monitor Sense**
- **Internal voltage reference**
- **135 MHz (-3), 110 MHz (-2) & 80 MHz (-1) versions**
- **Very low clock jitter**
- **Latched frequency control pin**

Block Diagram



Pin Configuration



Rev 1.0

Pin Description (68 pin PLCC) K-10

Symbol	Pin #	Type	Description
D7 - D0	68, 1 - 7	I/O	System data bus I/O. These bidirectional Data I/O lines are used by the host microprocessor to write (using active low WR*) information into, and read (using active low RD*) information from the six internal registers (Pixel Address, Color Value, Pixel Mask, PLL Address, PLL Parameter, and Command). During the write cycle, the rising edge of WR* latches the data into the selected register (set by the status of the three RS pins). The rising edge of RD* determines the end of the read cycle. When RD* is a logical high, the Data I/O lines no longer contain information from the selected register and will go into a tri-state mode.
RD*	8	Input	RAM/PLL Read Enable, active low. This is the READ bus control signal. When active, any information present on the internal data bus is available on the Data I/O lines, D0-D7.
WR*	13	Input	RAM/PLL Write Enable, active low. This signal controls the timing of the write operation on the microprocessor interface inputs, D0-D7.
RS2 RS1 RS0	14 15 16	Input Input Input	Register Address Select 0. These inputs control the selection of one of the six internal registers. They are sampled on the falling edge of the active enable signal (RD* or WR*).
CVDD	17	-	Crystal oscillator and CLK0 power supply connect to AVDD.
XIN	18	Input	Crystal input. A 14.318 MHz crystal should be connected to this pin.
XOUT	19	Output	Crystal output. A 14.318 MHz crystal should be connected to this pin.
CGND	20	-	VSS for CLK0. Connect to ground.

Pin Description (continued)

Symbol	Pin #	Type	Description
CLK1	21	Output	Memory clock output. Used to time the video memory.
CGND	22	-	VSS for CLK1. Connect to ground.
CLK0	28	Output	Video clock output. Provides a CMOS level pixel or dot clock frequency to the graphics controller. The output frequency is determined by the values of the PLL registers.
CVDD	29	-	CLK1 Power Supply. Connect to AVDD.
CS0	30	Input	Clock select 0. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
CS1	31	Input	Clock select 1. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
CS2	32	Input	Clock select 2. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
VREF	33	I/O	Internal Reference Voltage. Normally connects to a 0.1µ cap to ground. To use an external Vref, connect a 1.235V reference to this pin.
RSET	34	Input	Resistor Set. This pin is used to set the current level in the analog outputs. It is usually connected through a 140Ω, 1% resistor to ground.
SENSE*	35	Output	Monitor Sense, active low. This pin is low when any of the red, green, or blue outputs have exceeded 335mV. The chip has on-board comparators and an internal 335mV voltage reference. This is used to detect monitor type.
AVDD	37	-	DAC power supply. Connect to AVDD.
BLUE GREEN RED	36 38 39	Output Output Output	Color Signals. These three signals are the DACs' analog outputs. Each DAC is composed of several current sources. The outputs of each of the sources are added together according to the applied binary value. These outputs are typically used to drive a CRT monitor.
STROBE	40	Input	Latches the input clock select signals CS0 - CS2.
P0 - P15	41- 42 46-48, 50	Input	Pixel Address Lines. This byte-wide information is latched by the rising edge of PCLK when using the Color Palette, and is masked by the Pixel Mask register. These values are used to specify the RAM word address in the default mode (accessing RAM). In the Hi-Color XGA, and True Color modes, they represent color data for the DACs. These inputs should be grounded if they are not used.
AGND	49	-	DAC Ground. Connect to ground.
DVDD	51	-	Digital power supply.
PCLK	65 52-58, 62-64	Input	Pixel Clock. The rising edge of PCLK controls the latching of the Pixel Address and BLANK* inputs. This clock also controls the progress of these values through the three-stage pipeline of the Color Palette RAM, DAC, and outputs.
BLANK*	66	Input	Composite BLANK* Signal, active low. When BLANK* is asserted, the outputs of the DACs are zero and the screen becomes black. The DACs are automatically powered down to save current during blanking. The color palette may still be updated through D0-D7 during blanking.
DGND	67	-	Digital Ground. Connect to ground.

Ordering Information

ICS5341V

Example:

ICS XXXX M

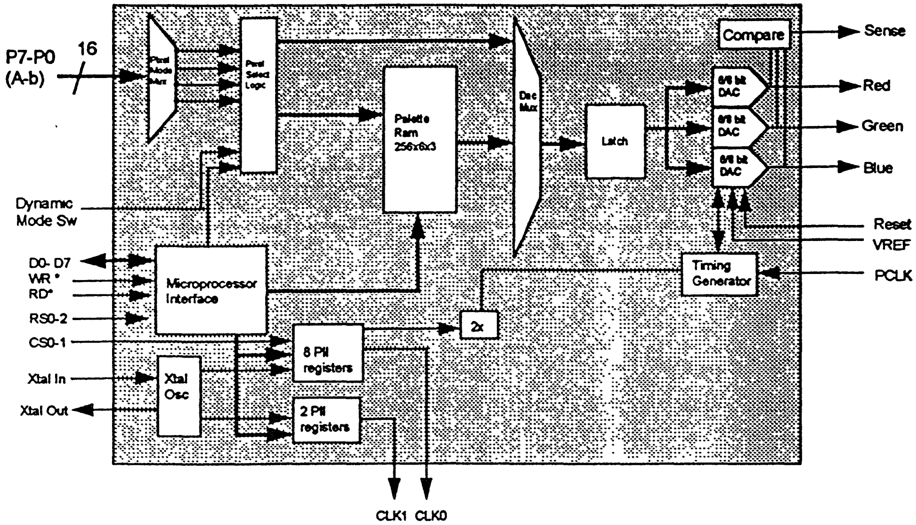
Package Type
V=PLCC
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

ICS5342

Integrated
Circuit
Systems, Inc.

Advance Information

16 bit integrated Clock, Palette Ram and DACs



Features:

- Triple 8 bit video DAC, dual clock generators, 256x6x3 palette, 16 bit pixel port
- Dynamic mode switch allows switching of color depth on a pixel by pixel basis. Ideal for multimedia video in a window applications
- Supports 8 bit pseudo, 15 bit, 16 bit hi-color and 24 bit true color (packed and sparse) modes
- On-chip loop filters reduce external components
- Eight programmable pixel clock frequency locations.
- Two programmable memory clock frequency locations
- DAC power down during blanking.
- Internal voltage reference
- Anti-sparkle circuitry
- Standard CPU interface, single external crystal (typically 14.318 MHz)
- Very low clock jitter

Color Modes:

8 bit interface

Mode number	CM3	CM2	CM1	CM0	COLOR MODE	CLOCK CYCLES/ PIXEL BITS
0	0	0	0	0	8 bit pseudo color with palette	1
1	0	0	0	1	15 bit direct color with bypass	2
3	0	0	1	0	24 bit true color with bypass	3
2	0	0	1	1	16 bit direct color with bypass	2
1	0	1	0	0	15 bit direct color with bypass	2
1	0	1	0	1	15 bit direct color with bypass	2
2	0	1	1	0	16 bit direct color with bypass	2
3	0	1	1	1	24 bit true color with bypass	3

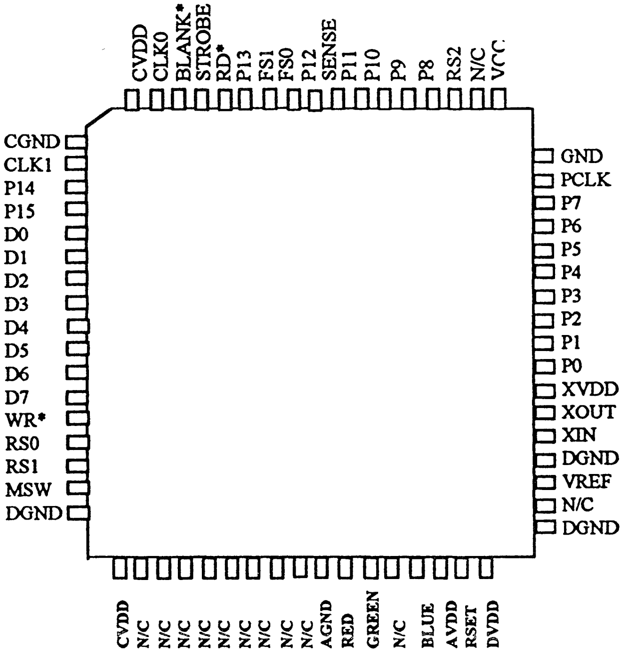
16 bit interface

Mode number	CM 3	CM 2	CM 1	CM 0	COLOR MODE	CLOCK CYCLES/ PIXEL BITS
4	1	0	0	0	Muxed 16 bit pseudo color with palette	1/2
5	1	0	0	1	15 bit direct color with bypass	1
6	1	0	1	0	16 bit direct color with bypass	1
7	1	0	1	1	24 bit true color with bypass	2
8	1	1	0	1	24 bit packed true color with bypass	3/2

Mode Select Operation:

The mode select pin MSW will toggle the chip between the primary mode and the secondary mode when "mode Enable Bit, " bit 2 of the Control Register is set. MSW will switch between two modes- 8 bit pseudo color (mode 0) and 16 bit pixel interface 16 bit direct color bypass mode (mode 6). If mode 0 is selected MSW = 0 will select the primary mode 0 and MSW =1 will select the secondary mode as mode 6 and MSW =1 will select the secondary mode as mode 0. By connecting the MSW pin to Vss the primary color mode is always selected.

Pin Configuration:



68-Pin PLCC
K-10

Pin Description (68 pin PLCC)

Symbol	Pin #	Type	Description
D7 - D0	14 - 21	I/O	Systems data bus I/O. These bi-directional Data I/O lines are used by the host microprocessor to write (using active low WR*) information into, and read (using active low RD*) information from the six internal registers (Pixel Address, Color Value, Pixel Mask, PLL Address, PLL Parameter, and Command). During the write cycle, the rising edge of WR* latches the data into the selected register (set by the status of the three RS pins). The rising edge of RD* determines the end of the read cycle. When RD* is a logical high, the Data I/O lines no longer contain information from the selected register and will go into a tri-state mode.
RD*	5	Input	RAM/PLL Read Enable, active low. This is the READ bus control signal. When active, any information present on the internal data bus is available on the Data I/O lines, D0-D7.
WR*	22	Input	RAM/PLL Write Enable, active low. This signal controls the timing of the write operation on the microprocessor interface inputs, D0-D7.
RS2 RS1 RS0	63 24 23	Input Input Input	Register Address Select 0. These inputs control the selection of one of the six internal registers. They are sampled on the falling edge of the active enable signal (RD* or WR*).
CVDD	27	-	Crystal oscillator and CLK0 power supply connect to AVDD.
XIN	48	Input	Crystal input. A 14.318 MHz crystal should be connected to this pin.
XOUT	49	Output	Crystal output. A 14.318 MHz crystal should be connected to this pin.
XVDD	50	-	Crystal oscillator power supply. Connect to AVDD.
MSW	25	Input	Mode switch. digital control for selecting primary and secondary pixel color modes. Low selects primary mode. connect to ground if not used.
CGND	26	-	VSS for CLK0. Connect to ground.
CLK1	11	Output	Memory clock output. Used to time the video memory.
CGND	10	-	VSS for CLK1. Connect to ground.
CLK0	8	Output	Video clock output. Provides a CMOS level pixel or dot clock frequency to the graphics controller. The output frequency is determined by the values of the PLL registers.
CVDD	9	-	CLK1 Power Supply. Connect to AVDD.
CS0	2	Input	Clock select 0. The status of CS0-1 determine which frequency is selected on the CLK0 (video) output.
CS1	3	Input	Clock select 1. The status of CS0-1 determine which frequency is selected on the CLK0 (video) output.
DGND	47	-	Vss for XTAL oscillator.
VREF	46	I/O	Internal Reference Voltage. Normally connects to a 0.1µ cap to ground. To use an external Vref, connect a 1.235V reference to this pin.

Pin Description (continued)

Symbol	Pin #	Type	Description
RSET	42	Input	Resistor Set. This pin is used to set the current level in the analog outputs. It is usually connected through a 140Ω, 1% resistor to ground.
SENSE*	68	Output	Monitor Sense, active low. This pin is low when any of the red, green, or blue outputs have exceeded 335mV. The chip has on-board comparators and an internal 335mV voltage reference. This is used to detect monitor type.
AVDD	41	-	DAC power supply. Connect to AVDD.
BLUE GREEN RED	40 38 37	Output Output Output	Color Signals. These three signals are the DACs' analog outputs. Each DAC is composed of several current sources. The outputs of each of the sources are added together according to the applied binary value. These outputs are typically used to drive a CRT monitor.
P0 - P15	51-58, 64067, 1-4, 12, 13	Input	Pixel Address Lines. This byte-wide information is latched by the rising edge of PCLK when using the Color Palette, and is masked by the Pixel Mask register. These values are used to specify the RAM word address in the default mode (accessing RAM). In the Hi-Color XGA, and True Color modes, they represent color data for the DACs. These inputs should be grounded if they are not used.
AGND	36	-	DAC Ground. Connect to ground.
DVDD	43	-	Digital power supply.
PCLK	59	Input	Pixel Clock. The rising edge of PCLK controls the latching of the Pixel Address and BLANK* inputs. This clock also controls the progress of these values through the three-stage pipeline of the Color Palette RAM, DAC, and outputs.
STROBE	6	Input	Latches the input clock select signals CS0-CS1.
BLANK*	7	Input	Composite BLANK* Signal, active low. When BLANK* is asserted, the outputs of the DACs are zero and the screen becomes black. The DACs are automatically powered down to save current during blanking. The color palette may still be updated through D0-D7 during blanking.
DGND	44	-	Digital Ground. Connect to ground.

Internal Registers

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
				There is a single Pixel Address register within the GENDAC. This register can be accessed through either register address 0,0,0 or register address 0,1,1. A read from address 0,0,0 is identical to a read from address 0,1,1. Writing a value to address 0,0,0 performs the following operations: a) Specifies an address within the color palette RAM. b) Initializes the Color Value register. Writing a value to address 0,1,1 performs the following operations: a) Specifies an address within the color palette RAM. b) Loads the Color Value register with the contents of the location in the addressed RAM palette and then increments the Pixel Address register.
0	0	0	Pixel Address WRITE	Writing to this 8-bit register is performed prior to writing one or mor color values to the color palette RAM.
0	1	1	Pixel Address READ	Writing to this 8-bit register is performed prior to reading one or more color values from the color palette RAM.
0	0	1	Color Value	The 18-bit Color Value register acts as a buffer between the microprocessor interface and the color palette. Using a three bytes transfer sequence allows a value to be read from or written to this register. When a byte is read, the color value is contained in the least significant 6 bits, D0-D5 (the most significant 2 bits are set to zero). When writing a byte, the same 6 bits are used. When reading or writing, data is transferred in the same order - the red byte first, then green, then blue. Each transfer between the Color Value register and the color palette replaces the normal pixel mapping operations of the GENDAC for a single pixel. After writing three definitions to this register, its contents are written tot he location in the color palette RAM specified by the Pixel Address register, and the Pixel Address register increments. After reading three definitions from this register, the contents of the location in the color palette RAM specified by the Pixel Address registers are copied into the Color Value register, and the Pixel Address register increments.

Internal Registers (continued)

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
0	1	0	Pixel Mask	The 8-bid Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P0-P7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, while a zero sets that bit to zero. The Pixel Mask register does not affect the Pixel Address generated by the microprocessor interface when the palette RAM is being accessed. The I.D. register will be read on the forth consecutive read of the mask register. I.D. for this part is 10110001.

Functional Description

This section describes the register address and bit definition for RAMDAC and the Frequency Synthesizer sections.

Color Palette

Command Register

(RS0-RS2 = 011)

(RS0-RS1 = 01 with hidden flag)

By setting bits in the command register the ICS5340 can be programmed for different color modes and can be powered down for low power operations.

7	6	5	4	3	2	1	0
Color Mode							Snooze
2	1	0	3	=0	ME	=0	

Table 3 - Command Registers

Bit 7-4 Color Mode Select

These three bits select the Color Mode of RAMDAC operation as shown in the ICS5340 data sheet (default is 0 at power up);

Bit 3,1 (Reserved)

Bit 2 Mode enable ME

When this bit is set to 0 (default is 0), mode switch is disabled. If this bit is set to 1, the MSW pin will be enabled.

Bit 0 Power Down Mode of RAMDAC

When this bit is set to 0 (default is 0), the device operates normally. If this bit is set to 1, the power and clock to the Color Palette RAM and DACs are turned off. The data in the Color Palette RAM are still preserved The CPU can access without loss of data by internal automatic clock start/stop control. The DAC outputs become the same as BLANK* (sync) level output during power down mode. This bit does not effect the PLL clock synthesizer function.

Ordering Information

ICS5342V

Example:

ICS XXXX M

Package Type
V=PLCC
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

ICS
Power Management
Products

ICS has a full line of intelligent NiCd and NiMH battery charge controllers for portable consumer electronic, power tool, audio/video and communications equipment. Each controller provides multiple charge termination methods and charge rates that provide a successful, cost effective battery charging solution.

The features available in the ICS controller line satisfy charging system requirements whether simple or complex, standard or custom. ICS has the analog and digital blocks to create custom solutions for battery gauging and monitoring, charge controllers for new or special battery chemistries, and controllers for sequential battery charging.

ICS Power Management Products

NiCd and NiMH Battery Charge Controller

Selection Guide

Charge Termination Methods	ICS Device Type	Charge Rates	Description	Package Types	Page
Voltage Slope Maximum Temperature Charge Timer	ICS1700A	Four Rates (C/2 to 4C)	Hot Battery Shutdown. Cold Battery Charge.	16-Pin DIP 20-Pin SOIC	I-3
Voltage Slope Temperature Slope Maximum Temperature Charge Timers	ICS1702	Nine Rates (C/4 to 4C)	Six Auxiliary Modes. Hot Battery Shutdown. Cold Battery Charge. Adjustable Battery Detection.	20-Pin DIP 20-Pin SOIC	I-27
Voltage Slope Temperature Slope Maximum Temperature Charge Timer	ICS1712	Four Rates (C/2 to 4C)	Hot Battery Shutdown. Cold Battery Charge.	16-Pin DIP 16-Pin SOIC	I-57
Voltage Slope Charge Timers	ICS1722	Nine Rates (C/4 to 4C)	Six Auxiliary Modes. Adjustable Battery Detection.	16-Pin DIP 16-Pin SOIC	I-79

Note: C=Ampere/hour capacity of battery.

Integrated Circuit Systems, Inc. (ICS) shall be held harmless for any misapplication of this device such as: exceeding the rated specifications of the battery manufacturer; charging batteries other than nickel-cadmium and/or nickel metal hydride type; personal or product damage caused by the charging device, circuit, or system itself; unsafe use, application, and/or manufacture of a charging system using this device.

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. ICS reserves the right to change or discontinue these products without notice.

**Integrated
Circuit
Systems, Inc.**

ICS1700A

QuickSaver® Charge Controller for Nickel-Cadmium and Nickel-Metal Hydride Batteries

General Description

The **ICS1700A** is a CMOS device designed for the intelligent charge control of either nickel-cadmium (NiCd) or nickel-metal hydride (NiMH) batteries. The controller uses a pulsed-current charging technique together with voltage slope termination. The **ICS1700A** employs a four stage charge sequence that provides a complete recharge without overcharging. The controller has four user-selectable charge rates available for customized charging systems. The **ICS1700A** is a pin-for-pin replacement for the original ICS1700 controller.

The **ICS1700A** monitors for the presence of a battery and begins charging if a battery is installed within the first 10 seconds after a reset. Voltage and temperature are measured to ensure a battery is within fast charge conditions before charge is initiated.

Applications

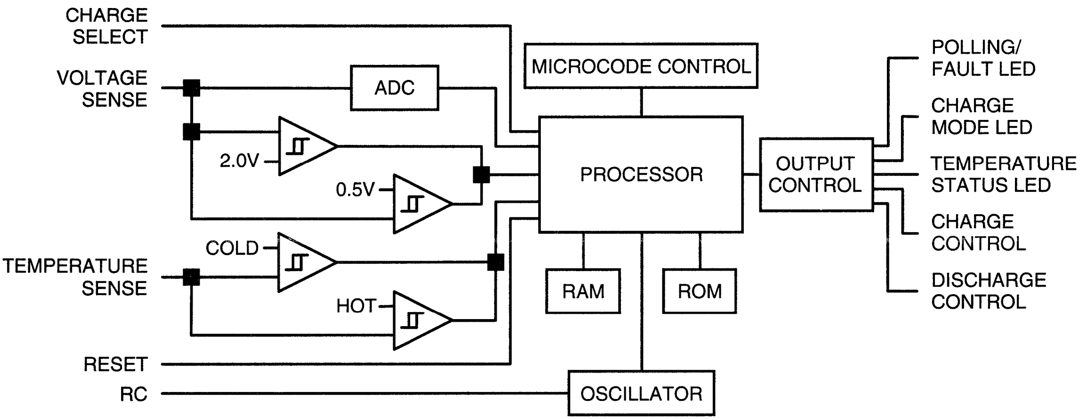
Battery charging systems for:

- Portable consumer electronics
- Power tools
- Audio/video equipment
- Communications equipment

Features

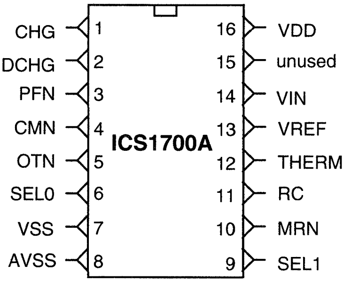
- Multiple charge termination methods include:
  - Voltage slope
  - Maximum temperature
  - Charge timer
- Four stage charge sequence:
  - Soft start charge
  - Fast charge
  - Topping charge
  - Maintenance charge
- Reverse-pulse charging available in all charge stages
- Four programmable charge rates between 15 minutes (4C) and two hours (C/2)
- Out-of-temperature range detection
  - Hot battery: charger shutdown
  - Cold battery: low current charge
- Ten second polling mode for battery detection
- Battery fault with shutdown protection

Block Diagram

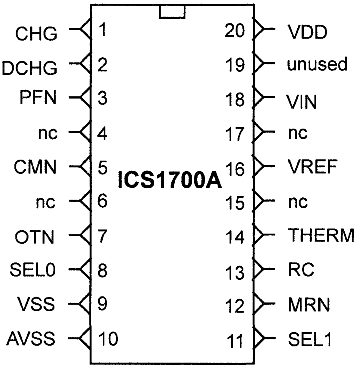


QuickSaver is a registered trademark of Integrated Circuit Systems, Inc

Pin Configuration



16-Pin DIP
K-4



20-Pin SOIC
K-7

Pin Definitions

Pin Number		Pin Name	Type	Definition
DIP	SOIC			
1	1	CHG	OUT	Active high TTL compatible signal used to turn on an external current source to provide current to charge the battery
2	2	DCHG	OUT	Active high TTL compatible signal available to turn on a discharge circuit
3	3	PFN	OUT	Polling fault indicator. An active low turns on an external indicator to show the controller is either polling for the presence of the battery or has determined the battery has been removed
4	5	CMN	OUT	Charge mode indicator A continuous low shows the controller is in a soft start or fast charge. The indicator flashes during the topping and maintenance charges.
5	7	OTN	OUT	Out-of-temperature range indicator An active low turns on an external indicator showing the battery is out of the normal fast charge temperature range
6	8	SEL0	IN	Input used with the SEL1 pin to program the device for the desired charge rate.
7	9	VSS		Ground.
8	10	AVSS		Ground.
9	11	SEL1	IN	Input used with the SEL0 pin to program the device for the desired charge rate.
10	12	MRN	IN	Master reset signal. A logic low pulse greater than 700 ms initiates a device reset
11	13	RC	IN	An external resistor and capacitor sets the frequency of the internal clock.
12	14	THERM	IN	Thermistor or thermal switch input for temperature sensing
13	16	VREF		1.26V voltage reference.
14	18	VIN	IN	Battery voltage normalized to one cell with an external resistor divider.
15	19	unused		Ground.
16	20	VDD		Device supply =+5 0 VDC

Note: (DIP/SOIC)
Pin 6/8 has an internal pull-up.
Pin 9/11 has an internal pull-up.
Pin 10/12 has an internal pull-up.
Pin 12/14 has an internal pull-up.

Controller Operation

Charging Stages

The charging sequence consists of four stages. The application of current is shown graphically in Figure 1. The soft start stage gradually increases current levels up to the user selected fast charge rate during the first two minutes. The soft start stage is followed by the fast charge stage, which continues until termination. After termination, a two hour C/10 topping charge is applied. The topping charge is followed by a C/40 maintenance charge.

Soft Start Charge

Some batteries may exhibit an unusual high impedance condition while accepting the initial charging current, as shown in Figure 2. Unless dealt with, this high impedance condition can cause a voltage peak at the beginning of the charge cycle that would be misinterpreted as a fully charged battery by the voltage termination methods.

The soft start charge eases batteries into the fast charge stage by gradually increasing the current to the selected fast charge rate. The gradual increase in current alleviates the voltage peak. During this stage, only positive current pulses are applied to the battery. The duty cycle of the applied current is increased to the selected fast charge rate, as shown in Figure 3, by extending the current pulse on every cycle until the pulse is about one second in duration. The initial current pulse is approximately 200ms. The CMN indicator is activated continuously during this stage

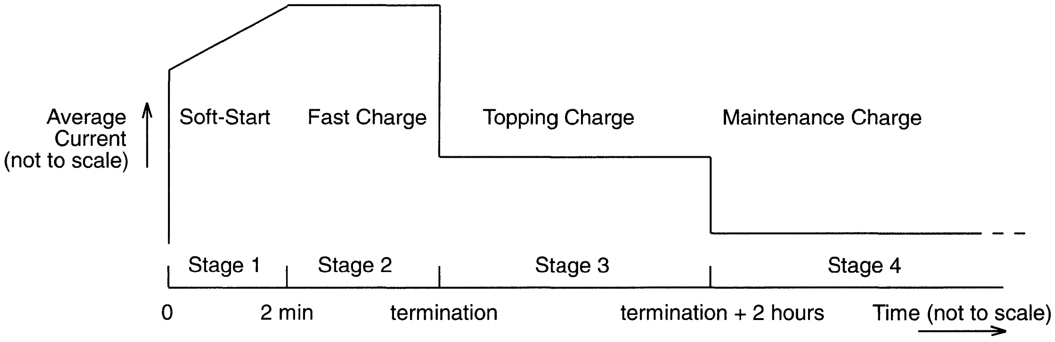


Figure 1: Graphical representation of average current levels during the four charging stages

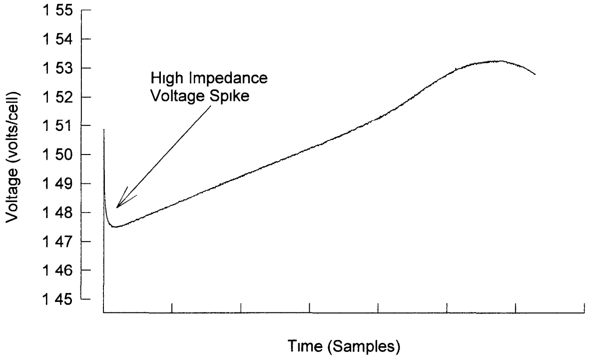


Figure 2: High impedance voltage spike at the beginning of charge

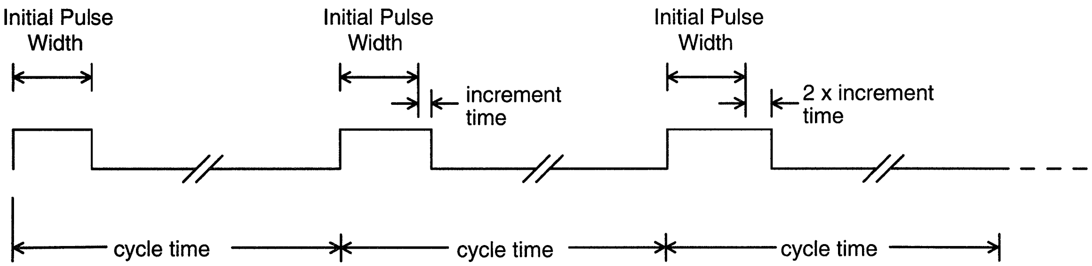


Figure 3: Cycle-to-cycle increase of the soft-start current pulse widths

Fast Charge

In the second stage, the **ICS1700A** applies the charging current in a series of charge and discharge pulses. The technique consists of a positive current charging pulse followed by a high current, short duration discharge pulse. The cycle, shown with charge, discharge, rest and data acquisition periods in Figure 4, repeats every second until the batteries are fully charged.

The amplitude of the current pulse is determined by system parameters such as the current capability of the charging system, the desired charge rate, the cell capacity and the ability of that cell to accept the charge current. The **ICS1700A** can be set for four user-selectable fast charge rates from 15 minutes (4C) to two hours (C/2). Charge pulses occur approximately every second. The CMN indicator is activated continuously during this stage.

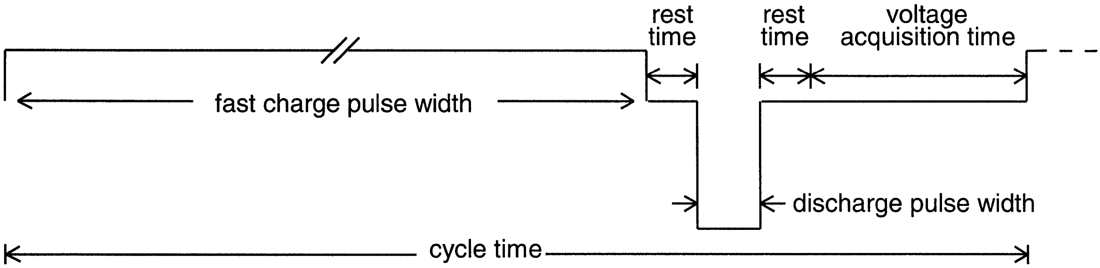


Figure 4: Charge cycle showing charge and discharge current pulses

The discharge current pulse amplitude is typically set to about 2.5 times the amplitude of the charging current based on 1.4V/cell. For example, if the charge current is 4 amps, then the discharge current is set at about 10 amps. The energy removed during the discharge pulse is a fixed ratio to the positive charge rate. The amplitude of the discharge pulse does not affect the operation of the part as described in this section.

A voltage acquisition window immediately follows a brief rest time after the discharge pulse. No charge is applied during the rest time or during the acquisition window to allow the cell chemistry to settle. Since no current is flowing, the measured cell voltage is not obscured by any internal or external IR drops or distortions caused by excess plate surface charge. The **ICS1700A** makes one continuous reading of the no-load battery voltage during the entire acquisition window. The voltage that is measured during this window contains less noise and is a more accurate representation of the true state of charge of the battery.

Topping Charge

The third stage is a topping charge that applies current at a rate low enough to prevent cell heating but high enough to ensure a full charge.

The topping charge applies a C/10 charging current for two hours. The current consists of the same pulse technique used during the fast charge stage; however, the duty cycle of the pulse sequence has been extended as shown in Figure 5. Extending the time between charge pulses allows the same charging current used in the fast charge stage so that no changes to the current source are necessary. For example, the same charge pulse that occurs every second at a 2C fast charge rate will occur every 20 seconds for a topping charge rate of C/10. The CMN indicator flashes at a one second rate during this stage.

Maintenance Charge

The maintenance charge is intended to offset the natural self-discharge of NiCd or NiMH batteries by keeping the cells primed at peak charge. After the topping charge ends, the **ICS1700A** begins this charge stage by extending the duty cycle of the applied current pulses to a C/40 rate. The maintenance charge will last for as long as the battery voltage is greater than 0.5V at the VIN pin. The CMN indicator flashes at a one second rate during this stage.

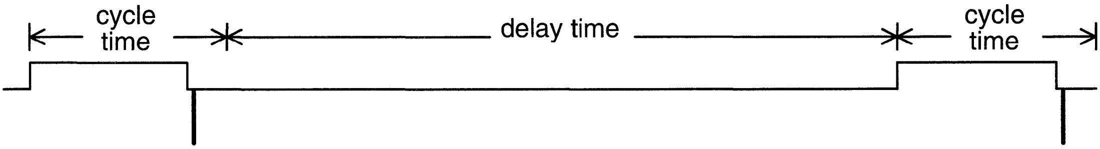


Figure 5: Representative timing diagram for topping and maintenance charge

Charge Termination Methods

Several charge termination schemes, including voltage slope, maximum temperature and a fast charge timer are available. The voltage slope method may be used with or without the maximum temperature method. Maximum temperature and the fast charge timer are available as backup methods.

Voltage Slope Termination

The most distinctive point on the voltage curve of a charging battery in response to a constant current is the voltage peak that occurs as the cell approaches full charge. By mathematically calculating the first derivative of the voltage, a second curve can be generated showing the change in voltage with respect to time as shown in Figure 6. The slope will reach a maximum just before the actual peak in the cell voltage. Using the voltage slope data, the ICS1700A calculates the point of full charge and accurately terminates the applied current as the battery reaches that point. The actual termination point depends on the charging characteristics of the particular battery.

Cells that are not thoroughly conditioned or possess an unusual cell construction may not have a normal voltage profile. The **ICS1700A** uses an alternate method of charge termination based on a slight decrease in the voltage slope to stop charge to cells whose voltage profile is very shallow. This method looks for a flattening of the voltage slope which may indicate a shallow peak in the voltage profile. The zero slope point occurs slightly beyond the peak voltage and is shown on the voltage curve graph.

Maximum Temperature Termination

Maximum temperature can be sensed using either a NTC thermistor or a thermal switch. Maximum temperature termination can also be bypassed if desired, although it is strongly recommended that some form of temperature termination be used.

If an NTC thermistor is used, an internal voltage threshold determines when the battery is too hot to charge. As temperature increases, the voltage across the thermistor will drop. This voltage is continually compared to the internal voltage threshold. If the thermistor voltage drops below the internal threshold, the OTN indicator is activated and the controller shuts down. The controller must be reset once the hot battery fault condition has cleared to restart the charge sequence.

If a thermal switch is used, a 45°C open circuit switch is recommended. When the thermal switch opens, an internal pull-up at the THERM pin results in a logic high which shuts down the controller and activates the OTN indicator. The controller must be reset once the hot battery fault condition has cleared to restart the charge sequence.

Maximum temperature termination can be disabled by grounding the THERM pin. See the section on *Temperature Sensing* for more information.

Fast Charge Timer Termination

The controller uses a timer to limit the fast charge duration. These times are pre-programmed, and are automatically adjusted in time duration according to the charge rate selected. Fast charge timer termination is best suited as a safety backup feature to limit the duration of the fast charge stage. The fast charge timer is always enabled and cannot be disabled. See Table 2 for more information.

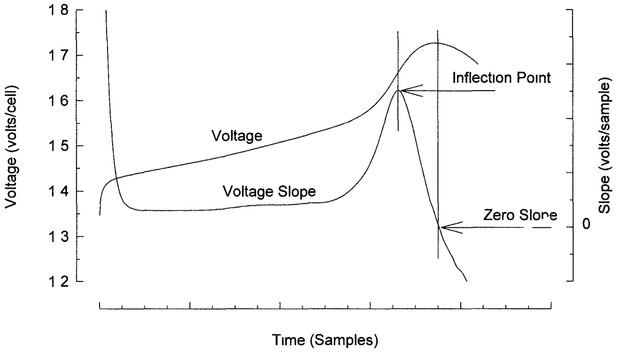


Figure 6: Voltage and slope curves showing inflection and zero slope points

Battery Polling

Upon power-up or after a reset is issued, any excess charge from filter capacitors at the charging system terminals is removed with a series of discharge pulses. After the discharge pulse series is complete, the voltage at VIN must be greater than 0.5V when a battery is present. If the voltage at VIN is less than 0.5V, the **ICS1700A** assumes no battery is attached and initiates a polling sequence.

The **ICS1700A** then applies a 100ms charge pulse. During the pulse, the **ICS1700A** monitors the VIN pin to determine if the divided down terminal voltage is greater than the internal 2.0V reference. If the battery is present, the voltage is clamped below the 2.0V reference when the current pulse is applied and the fast charge stage begins immediately. If a battery is not present, the voltage at VIN rises above the 2.0V reference and the PFN fault indicator is activated.

The charge pulses repeat for 10 seconds. If the battery is installed within 10 seconds, the **ICS1700A** will turn off the PFN fault indicator and enter the soft start stage. If the battery is not installed within 10 seconds, the PFN fault indicator remains active and the **ICS1700A** shuts down. A reset must be issued to restart the controller after installing the battery.

Battery Fault Detection

The **ICS1700A** will turn on the PFN fault indicator and shut down if the battery is removed or if an open circuit occurs in the current path anytime after fast charge has been initiated. When in the topping charge or maintenance charge stages, a charge pulse may not occur for several seconds. During the period between charge pulses, the voltage at VIN should be greater than 0.5V if a battery is attached. If the voltage at VIN is less than 0.5V, the **ICS1700A** assumes the battery has been removed, a fault condition is indicated by the PFN fault indicator, and the controller shuts down.

Cold Battery Charging

Cold battery charging is activated if a voltage at the THERM pin is in the cold battery voltage range, as shown in Figure 7. The **ICS1700A** checks for a cold battery before initiating fast charge. If a cold battery is present before fast charging begins, the **ICS1700A** begins a two hour C/10 topping charge (the pulsed duty cycle is based on the selected charge rate). If the battery is still cold after the two hour topping charge is complete, the **ICS1700A** begins a C/40 maintenance charge. The maintenance charge will continue for as long as the battery remains cold. The thermistor voltage at the THERM pin is checked every second to see if the battery has warmed up. If so, the **ICS1700A** stops the topping charge or maintenance charge and begins a fast charge at a rate selected by the SEL0 and SEL1 inputs. See the section on *Temperature Sensing* for more information.

The CMN will flash at a one second rate, and the OTN indicator will be active, indicating that a low current charge is being applied to a battery that is outside the specified temperature range for fast charging.

Pin Descriptions

The **ICS1700A** requires some external components to control the clock rate, sense temperature and provide an indicator display. The controller must be interfaced to an external power source that will provide the current required to charge a battery pack and, if desired, a circuit that will sink discharge current.

Output Logic Signals: CHG, DCHG Pins

The CHG and DCHG pins are active high, TTL compatible outputs. In addition to being TTL compatible, the CMOS outputs are capable of sourcing current which adds flexibility when interfacing to other circuitry. A logic high on the CHG pin indicates that the charging current supply should be activated. If applicable, a logic high on the DCHG pin indicates that the discharge circuit should be activated.

Care must be taken to control wiring resistance and inductance. The load resistor must be capable of handling this short duration high-amplitude pulse.

Indicators: CMN, PFN, OTN Pins

The controller has three outputs for driving external indicators. These pins are active low. The three indicator outputs have open drains and are designed to be used with LEDs. Each output can sink over 20mA which requires the use of an external current limiting resistor. The three indicator signals denote fast charge stage, topping and maintenance stages, and the polling detect or battery fault and out-of-temperature range modes as shown in Table 1.

The charge mode (CMN) indicator is activated continuously during the soft start and fast charge stages. The CMN indicator flashes at a one second rate when the **ICS1700A** is applying a topping or maintenance charge.

The polling fault (PFN) indicator is on when the **ICS1700A** polls for a battery for the first 10 seconds. The controller applies periodic charge pulses to detect the presence of a battery. The indicator is a warning that these charge pulses are appearing at the charging system terminals at regular intervals. When a battery is detected, the indicator is turned off. The indicator is also active if the battery is removed from the system, warning that a fault has occured.

The out-of-temperature range (OTN) indicator is active whenever the voltage at the temperature sense (THERM) input enters a range that indicates that the attached battery is too hot to charge. The OTN indicator is also activated with the CMN indicator if the controller is initialized with the battery in the cold battery charge region.

Table 1: Indicator Description List

PFN	CMN	OTN	Description
on			Polling mode or battery fault
	flash		Maintenance and topping charge
	on		Fast charge
		on	Hot battery shutdown
	flash	on	Cold battery charge
	on	on	see Applications Information
on	one flash		see Applications Information

Charge Rate Selection: SEL0, SEL1 Pins

The SEL0 and SEL1 inputs must be programmed by the user to inform the **ICS1700A** of the desired charge rate. When a low level is required, the pin must be grounded. When a high level is required, no connection is required since each pin has an internal 75kΩ pull-up to V_{DD}. The voltage ranges for low (L) and high (H) are listed in Table 6, *DC Characteristics*. To program the SEL0 and SEL1 inputs, refer to the *Charge Rate List* in Table 2.

The **ICS1700A** does not control the current flowing into the battery in any way other than turning it on and off. The required current for the selected charge rate must be provided by the user's power source. The external charging circuitry should provide current at the selected charge rate. For example, to charge a 1.2 ampere hour battery in 30 minutes (2C), approximately 2.4 amperes of current is required.

Table 2: Charge Rate List

SEL0	SEL1	Charge Rate	Topping Charge Pulse Rate	Maintenance Charge Pulse Rate	Fast Charge Timer Duration (after reset)
L	L	4C (15 min)	one every 40 sec	one every 160 sec	30 min
L	H	2C (30 min)	one every 20 sec	one every 80 sec	60 min
H	L	1C (60 min)	one every 10 sec	one every 40 sec	90 min
H	H	C/2 (120 min)	one every 5 sec	one every 20 sec	210 min

See the section on *Controller Operation* for additional information on the topping charge and maintenance charge. See the section on *Charge Termination Methods* for additional information on the charge timer.

Master Reset: MRN Pin

The MRN pin is provided to re-program the controller for a new charging sequence. This pin has an internal pull-up of about 75kΩ. A logic low on the MRN pin must be present for more than 700ms for a reset to occur. As long as the pin is low, the controller is held in a reset condition. A master reset is required to change charge rates or clear a temperature fault condition. Upon power-up, the controller automatically resets itself.

Clock Input: RC Pin

The RC pin is used to set the frequency of the internal clock when an external 1 MHz clock is not available. An external resistor must be connected between this pin and V_{DD}. An external capacitor must be connected between this pin and ground. The frequency of the internal clock will be about 1 MHz with a 16kΩ resistor and a 100pF capacitor. All time durations noted in this document are based on a 1 MHz clock. Operating the clock at a lower frequency will proportionally change all time durations. Operating the clock at a frequency significantly lower than 1 MHz, without adjusting the charge current accordingly, will lessen the effectiveness of the fast charge timer and lower the accuracy of the controller. Operating the clock at a frequency greater than 1 MHz will also change all time durations and, without adjusting the charge current accordingly, may cause termination to occur due to the fast charge timer expiring rather than by the battery reaching full charge.

The clock may be driven by a 1 MHz external 0 to 5V pulse provided the duty cycle is between 10% and 60%. The clock input impedance is about 1kΩ.

Temperature Sensing: THERM Pin

The THERM pin is provided for hot and cold battery detection and for maximum temperature termination of fast charge when used in conjunction with an NTC thermistor. The THERM pin also provides for hot battery and maximum temperature termination when used in conjunction with a normally closed thermal switch. Several internal voltage thresholds are used by the controller depending on whether a thermistor or a thermal switch is used. Figure 7 shows the internal thresholds over laid on a typical thermistor curve.

- Using an NTC thermistor for hot and cold battery detection:

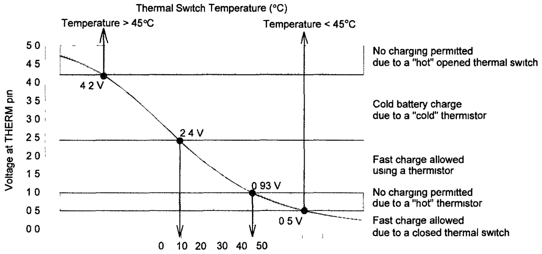


Figure 7: Voltage levels for temperature sensing with a thermistor or thermal switch

The THERM pin requires some thought if a thermistor is going to be used for hot and cold battery detection. The example below works for a typical 10kΩ @ 25°C NTC thermistor. Consider using the controller to prevent charging above 45°C and reducing the current below 10°C. At 10°C the resistance of the thermistor is 18kΩ. At 45°C, the resistance drops to 4.7kΩ. The **ICS1700A** has an internal voltage threshold at 10°C at 2.4V, and an internal voltage at 45°C at 0.93V as shown in Figure 7. At 25°C the voltage at the THERM pin is set at the midpoint of the thresholds:

$$0.93\text{V} + \frac{2.40\text{V} - 0.93\text{V}}{2} = 1.67\text{V}.$$

The THERM pin has a 75kΩ internal pull-up (R_{pu}). Using a resistor divider with 10kΩ for the thermistor (R_{th}) and a external fixed resistor (R_{fix}), the divider looks like Figure 8 at 25°C:

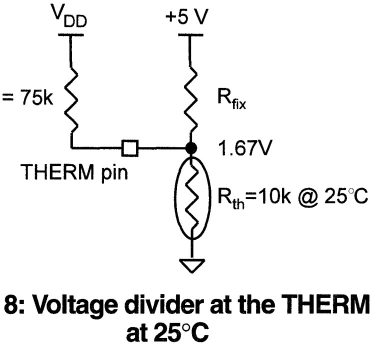


Figure 8: Voltage divider at the THERM pin at 25°C

To set the voltage at the THERM pin for 1.67V at 25°C, the equivalent divider looks like Figure 9.

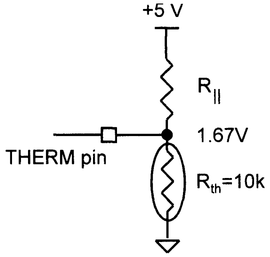


Figure 9: Equivalent voltage divider

The parallel resistance $R_{||}$ is calculated:

$$R_{||} = \frac{5.0V - 1.67V}{1.67V/10k\Omega} = 20k\Omega.$$

The internal pull-up resistance R_{pu} and the parallel resistance $R_{||}$ are known so the external fixed resistor can be calculated from:

$$R_{fix} = \frac{R_{pu}R_{||}}{R_{pu} - R_{||}}$$

Substituting in known values: $R_{fix} = 27.27k\Omega$. A $27k\Omega$ standard value is used for R_{fix}.

Since the thermistor resistance R_{th} is specified by manufacturers at a particular temperature, the voltage across the thermistor V_{th} at that temperature can be calculated from:

$$V_{th} = \frac{R_{th}}{R_{||} + R_{th}} (5V),$$

with the drop across the resistor divider equal to 5V. For this example, the calculated voltage with $R_{th}=18k\Omega$ at 10°C is 2.37V and with $R_{th}=4.7k\Omega$ at 45°C the voltage is 0.95V. Table 3 lists the internal thresholds for hot and cold battery detection. If the voltage across the thermistor (at the THERM pin) drops below 0.93V, the **ICS1700A** will shut down due to a hot battery fault condition and will not restart unless reset. If the voltage dropped across the thermistor is above 2.4V before fast charge is initiated, the **ICS1700A** will begin a reduced current charge. See the *Cold Battery Charging* section for more information.

Table 3: Thermistor Voltage Thresholds

Parameter	Voltage	Battery Temperature
Cold Battery Thermistor Voltage	>2.4	<10°C
Hot Battery Thermistor Voltage	<0.93	>45°C

- Using a thermal switch for hot battery detection:

A thermal switch that opens at about 45°C is recommended. The thermal switch must be connected between the THERM pin and ground. When the thermal switch is closed, the voltage at the THERM pin must be below 0.5V for normal operation. When the thermal switch opens (see Figure 10), the internal pull-up at the THERM pin will raise the voltage above 4.2V and the **ICS1700A** will shut down and will not restart unless reset. Table 4 contains the internal voltage thresholds used with a thermal switch.

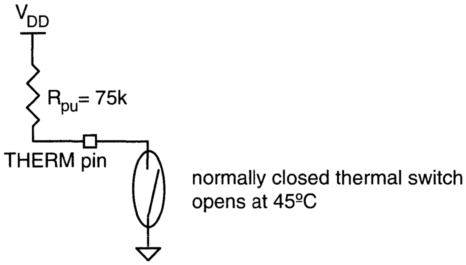


Figure 10: Thermal switch to connection to ground at the THERM pin

Table 4: Thermal Switch Voltage Thresholds

Parameter	Voltage	Battery Temperature
Opened Thermal Switch Voltage	>4.2	>45°C
Closed Thermal Switch Voltage	<0.5	<45°C

- Using no temperature sensor:

If a temperature sensor is not used, the THERM pin must be grounded.

Voltage Input: VIN Pin

The battery voltage must be normalized by an external resistor divider network to one cell. The electrochemical potential of one cell is about 1.2V. For example, if the battery consists of six cells in series, the voltage at the VIN pin must be equal to the total battery voltage divided by six. This can be accomplished with two resistors, as shown in Figure 11. To determine the correct resistor values, count the number of cells to be charged in series. Then choose either R1 or R2 and solve for the other resistor using:

$$R1 = R2 \times (\text{\# of cells -1}) \text{ or } R2 = \frac{R1}{(\text{\# of cells - 1})}$$

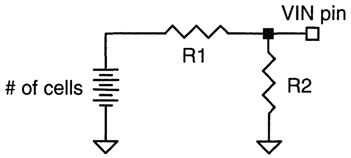


Figure 11: Resistor divider network at the VIN pin

Voltage Reference: VREF Pin

A 1.26V reference is present at this pin. The reference sets internal voltage references such as the 0.5V and 2.0V internal thresholds used by the controller for battery polling/fault detection and the analog/digital converter range.

The reference provides a fast way of checking the internal thresholds. Measuring VREF with a high input impedance volt meter (>1MΩ) is required. The reference can only be used if it is buffered with a high impedance device having an input impedance greater than 1MΩ. Buffering is essential to ensure that the internal voltage thresholds and analog/digital converter range and resolution are not altered.

The reference may be overridden by an external 1.2V to 1.3V reference.

Power: VDD Pin

The power supply for the device must be connected to the VDD pin. The voltage should be +5 VDC and should be supplied to the part through a regulator that has good noise rejection and an adequate current rating. The controller requires up to a maximum of 11mA with V_{DD}=5.00V.

Grounding: VSS, AVSS Pins

There are two ground pins. Both pins must be connected together at the device. This point must have a direct connection to a solid ground plane.

Data Tables

Table 5: Absolute Maximum Ratings

Supply Voltage	6.5	V
Logic Input Levels	-0.5 to V_{DD} + 0.5	V
Ambient Operating Temperature	0 to 70	°C
Storage Temperature	-55 to 150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at the Absolute Maximum Ratings or other conditions not consistent with the characteristics shown in this document is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 6: DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Supply Current	I_{DD}			7.3		mA
High Level Input Voltage SEL0, SEL1	V_{IH}		3.6	4.1	4.5	V
Low Level Input Voltage SEL0, SEL1	V_{IL}		0.73	0.75	0.8	V
Low Level Input Current, pull-up THERM, MRN	I_{IL}	V=0.4V		74		µA
High Level Source Current CHG, DCHG	I_{OH}	V=V_{DD}-0.4V		28		mA
Low Level Sink Current CHG, DCHG	I_{OL}	V=0.4V		25		mA
Low Level Sink Current, indicator PFN, CMN	I_{OL}	V=0.4V		40		mA
Low Level Sink Current, indicator OTN	I_{OL}	V=0.4V		28		mA
Input Impedance				1.0		MΩ
Analog/Digital Converter Range			0-2.2	0-2.7	0-2.7	V
Voltage Reference	V_{REF}		1.20	1.26	1.31	V

Table 7: DC Voltage Thresholds

T_{AMB}=25°C

PARAMETER	TYP	UNITS
Minimum Battery Voltage	0.5	V
Maximum Battery Voltage	2.0	V
Thermistor - Cold Temperature	2.4	V
Thermistor - Hot Temperature	0.93	V
Thermal Switch - Open	4.2	V
Thermal Switch - Closed	0.5	V

Table 8: Timing Characteristics

R≈16kΩ, C≈100pF

PARAMETER	SYMBOL	REFERENCE	TYP	UNITS
Clock Frequency			1.0	MHz
Reset Pulse Duration	t_{RESET}	see Figure B	700	ms
Charge Pulse Width	t_{CHG}	see Figure A	1048	ms
Discharge Pulse Width	t_{DCHG}	see Figure A	5.0	ms
Rest Time	t_R	see Figure A	4.0	ms
Data Acquisition Time	t_{DA}	see Figure A	16.4	ms
Cycle Time	t_{CYCLE}	see Figure A	1077	ms
Capacitor Discharge Pulse Width			5.0	ms
Capacitor Discharge Pulse Period			100	ms
Polling Detect Pulse Width			100	ms
Polling Detect Pulse Period			524	ms
Soft Start Initial Pulse Width			200	ms
Soft Start Incremental Pulse Width			7.0	ms
RESET to SEL Dynamic Reprogram Period	t_{RSA}	see Figure B	1160	ms

Timing Diagrams

Figure A:

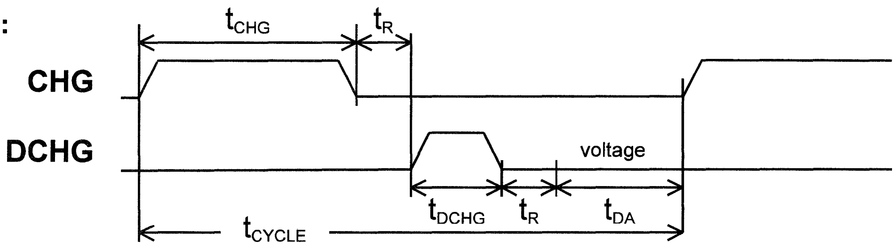
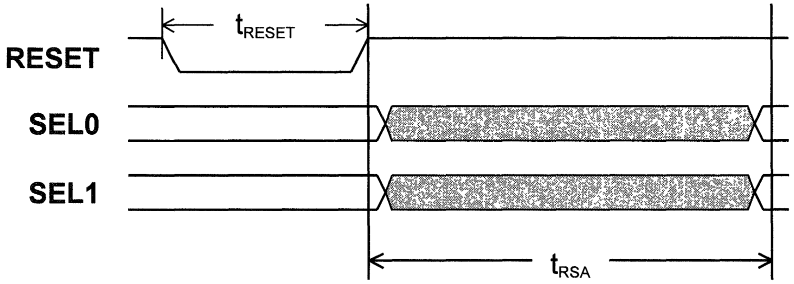


Figure B:



Applications Information

To ensure proper operation of the **ICS1700A**, external components must be properly selected. The external current source used must meet several important criteria to ensure optimal performance of the charging system.

VIN Divider Resistors

Figure 12 shows a typical application using the **ICS1700A**. R1 and R2 must be carefully selected to ensure that battery detection and voltage termination methods operate properly. R1 and R2 are selected to scale the battery voltage down to the voltage of one cell. The following table shows some typical values. Additional information is available in the *Voltage Input* section.

Cells	R1	R2
1	Short	Open
2	2.0k	2.0k
3	2.0k	1.0k
4	3.0k	1.0k
5	12k	3.0k
6	10k	2.0k
7	12k	2.0k
8	9.1k	1.3k

PC Board Design Considerations

It is very important that care be taken to minimize noise coupling and ground bounce. In addition, wires and connectors can add significant resistance and inductance to the charge and discharge circuits.

When designing the printed circuit board, make sure ground and power traces are wide and bypass capacitors are used right at the controller. Use separate grounds for the signal, charge and discharge circuits. Separate ground planes on the component side of the PC board are recommended. Be sure to connect these grounds together at the negative lead of the battery only. For the discharge circuit, keep the physical separation between power and return (ground) to a minimum to minimize field radiation effects. This precaution is also applicable to the constant current source, particularly if it is a switch mode type. Keep the **ICS1700A** and the constant current source control circuits outside the power and return loop described above. These precautions will prevent high circulating currents and coupled noise from disturbing normal operation.

Voltage Slope Termination

In general, the voltage slope termination method works best for equipment where the battery is fast charged with the equipment off or the battery is removed from the equipment for fast charge. The voltage slope termination method works best with a constant current flow into the battery during fast charge. If equipment draws a known constant current while the battery is charging, this current should be added to the fast charge current. Equipment that randomly or periodically requires current from the battery during fast charge needs evaluation to ensure it does not interfere with the proper operation of the voltage slope termination method.

Charging sources that produce decreasing current as fast charge progresses may cause a voltage inflection that may result in termination before full charge. For example, if the charge current is supplied through a resistor or if the charging source is a constant current type that has insufficient input voltage, the current will decrease and may cause a termination before full charge. Other current source characteristics that can cause a voltage inflection that is characteristic of a fully charged battery are inadequate ripple and noise attenuation capability or charge current decreasing due to thermal drift. Charging sources that have any of the above characteristics need evaluation to access their suitability for the application.

The controller soft start stage, built-in noise filtering, and fast charge timer operate optimally when the constant current source charges the battery at the rate selected. If the actual charge current is significantly less than the rate selected, the conditioning effect of the soft start stage and the controller noise immunity are lessened. Also, the fast charge timer may cause termination based on time duration rather than by the battery reaching full charge due to inadequate charge current.

Maximum Temperature Termination

Maximum temperature termination is best suited as a safety back-up feature. Maximum temperature termination requires that the thermal sensor be in intimate contact with the battery. A low thermal impedance contact area is required for accurate temperature sensing. The area and quality of the contact surface between the sensor and the battery directly affects the accuracy of temperature sensing. Thermally conductive adhesives may have to be considered in some applications to ensure good thermal transfer from the battery case to the sensor.

The thermal sensor should be placed on the largest surface of the battery for the best accuracy. The size of the battery is also a consideration when using temperature termination. The larger the battery, lower the surface area to volume ratio. Because of this, larger batteries are less capable in dissipating internal heat.

Additional considerations beyond the basics mentioned above may be involved when using maximum temperature termination where sudden changes in ambient temperature occur or where forced air cooling is used For these applications, the surface area of the thermal sensor in contact with the battery compared to the surface area of the thermal sensor in contact with the ambient air may be significant. For example, bead type thermistors are relatively small devices which have far less thermal capacity compared to most batteries. Insulating the surface of the thermistor that is in contact with the ambient air should help minimize heat loss by the thermistor and maintain accuracy.

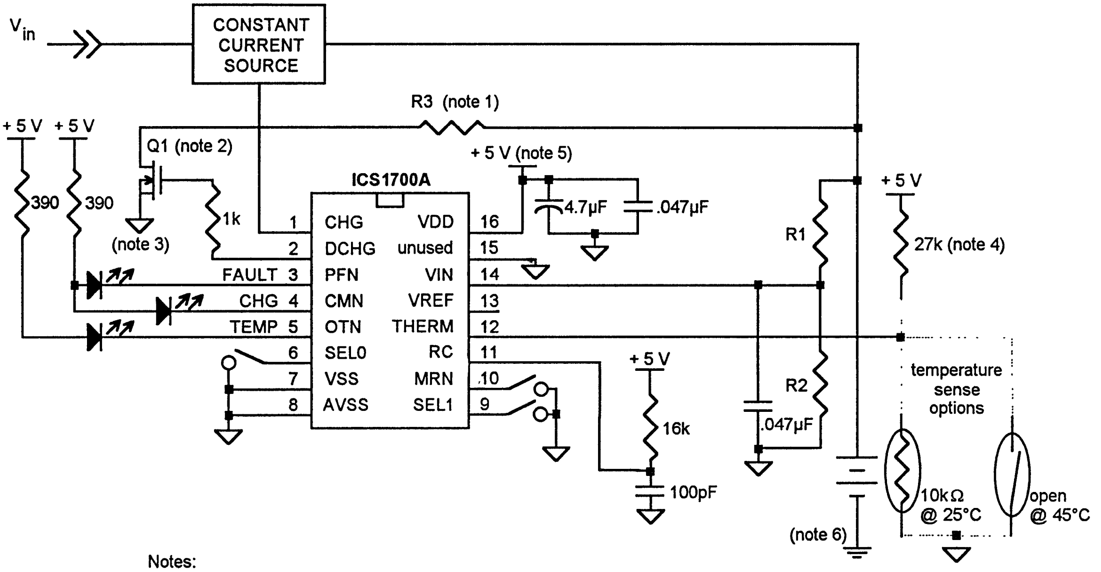
Charging System Status by Indicator

The *Indicator Description List* in Table 1 contains displays that are caused by charging system abnormalities. At power-up or after a reset is issued, one flash of the CMN indicator followed by a continuous PFN indication results from a voltage present at the battery terminals with the current source off and no battery. Check the current source and ensure that it produces no more than the equivalent of 350mV/cell when turned off with no battery. If the VIN divider resistors were not properly selected, an open circuit voltage that is actually less than the equivalent of 350mV/cell with the charger off and no battery will not divide down this open circuit voltage properly and produce a PFN fault indication. Check the VIN divider and ensure that it properly normalizes the battery voltage to the electrochemical potential of about 1.2V cell. If the PFN fault indicator is active immediately after power-up or after a reset is issued with the battery installed, then the constant current source is producing more than the equivalent of 350mV/cell when off and there is an open connection between the charger terminals and the battery. Check wires, connections, battery terminals, and the battery itself for an open circuit condition.

If the CMN and OTN indicators are active together, this is an indication that the battery temperature has dropped to below 10°C after a fast charge was initiated with the battery temperature normal. If this condition is observed and the battery temperature did not drop after fast charge was initiated, check the thermistor circuit mechanically for poor contact and electrically for excessive noise.

Enhanced Performance Characteristics

The **ICS1700A** is an enhanced performance, pin-for-pin replacement for the original ICS1700. Improved internal features provide additional capabilities. The charge sequence, voltage slope termination method, and analog-to-digital converter resolution allow the **ICS1700A** to charge either NiMH or NiCd batteries. The **ICS1700A** accepts either a thermal switch or thermistor input for temperature sensing. The polling mode for battery detection responds quickly to the removal of the battery throughout the charge sequence. The reset input debounce eliminates sensitivity to field effects and ground bounce when the PC board design recommendations cited in this document are employed. The temperature sense input debounce eliminates sensitivity to shock and vibration associated with the use of a thermal switch.



Notes:

1) Value of R3 determined by discharge current and capacity of battery pack.
2) Discharge FET is logic-level compatible in this application.
3) DC return of discharge FET must be connected close to negative battery terminal.
4) Resistor is needed only if a thermistor is used. Value may change depending on thermistor.
5) Regulated supply
6) Power ground; others are signal ground. Connect signal ground to power ground at negative battery terminal only.

Figure 12: Functional Diagram

Ordering Information

ICS1700AN, ICS1700AM, or ICS1700AMT

Example:

ICS XXXXA M

Package Type
N=DIP (Plastic)
M=SOIC
MT=SOIC Tape and Reel
Device Type (consists of 3-5 digit numbers)
Prefix
ICS=Standard Device

Integrated
Circuit
Systems, Inc.

ICS1700A

Application Note

ICS1700A Evaluation Board

General Description

The ICS1700A Evaluation Board allows quick evaluation of the ICS1700A Charge Controller for Nickel-Cadmium and Nickel-Metal Hydride Batteries. The evaluation board provides the designer an opportunity to both test the ICS1700A and a fast charge battery charger. The board is self-contained and has provisions for interfacing with an external constant current source to charge a battery.

The board includes resistors that are user-installed to customize operation for the desired charge rate, discharge pulse current, and number of cells in the battery pack. The board has a 5V regulator that provides power to the ICS1700A and the LED display. The board also has a breadboarding area consisting of a matrix of holes for user added components.

Before using the **ICS1700A Evaluation Board**, ICS recommends the user review the ICS1700A data sheet to become familiar with the operation of the controller. This data sheet should be included with the board; if not, please contact your local representative.

Customizing the Board for your Application

Refer to the evaluation board schematic diagram. The ICS1700A requires that the battery voltage is normalized to the voltage of one cell, or about 1.2V. To do this, resistors must be installed in the locations marked R6 and R8. The appropriate values can be selected from Table 1. An assortment of resistors is provided with the board.

Table 1

Cells	R6	R8
1	Open	Short
2	2.0k	2.0k
3	1.0k	2.0k
4	1.0k	3.0k
5	3.0k	12k
6	2.0k	10k
7	2.0k	12k
8	1.3k	9.1k

If the evaluation board is used with battery packs containing more than eight cells, the resistors can be determined by counting the number of cells to be charged in series. Then choose either R6 or R8 and solve for the other resistor using:

$$R8 = R6 \times (\text{\# of cells -1}) \quad \text{or} \quad R6 = \frac{R8}{(\text{\# of cells - 1})}$$

Current flow through the divider should be 0.4mA or greater for noise immunity.

The ICS1700A controller has an internal 2.0V reference used to detect the removal of the battery from the charging system. For most batteries, the maximum normalized battery voltage at the VIN pin at full charge is 1.7 to 1.8V. The voltage at VIN is compared to the 2.0V reference voltage when the current source is turned on. If the voltage at VIN is greater than the 2.0V reference, the ICS1700A assumes the battery has been removed and the ICS1700A indicates a fault condition by turning on the BF LED, and shuts down.

When power is applied to the board, the controller will start a charge sequence unless a logic low is applied to the RESET terminal. When RESET is removed by a logic high or open, a charge sequence will begin.

The board provides several low value resistors that may be used to set the amplitude of the discharge pulse. The resistors can be installed in any or all of the locations labeled R1, R2, or R3. The resistor value is calculated by setting the amplitude of the discharge pulse. The discharge pulse amplitude is typically 2.5 times the charge current based on 1.4V/cell. The resistor locations R1, R2, and R3 are connected in series. The unused locations must have a jumper to complete the circuit. Not using the discharge pulse feature will not affect the performance of the ICS1700A.

The ICS1700A is capable of operating at four different charge rates; 4C (15 minutes), 2C (30 minutes), 1C (60 minutes) and C/2 (120 minutes). The charge rate is selected by SW1 dip switch settings. Table 2 shows the proper settings to use for the desired charge rate.

Power Requirements

The evaluation board uses a regulator to provide +5 volts for the controller. The regulator allows operation from a DC supply of 8 to 32 volts when the supply is connected to the +V terminal. The board may also be operated from an external 5 volt supply by removing the regulator (VR1), wiring a jumper between regulator pins 1 and 3, and by connecting 5 volts directly to the +5V terminal.

Connections To External Circuitry

A normally closed thermal switch or a thermistor should be connected to the TS terminal. If a thermal protection device is not used, the TS terminal must be grounded.

Connect the battery between the +BAT and GND terminals. Connect the external charging current source and its return between the +CUR and GND terminals.

Two charge signals are provided to control external charging circuitry. CHARGE is high when the charging current is on. The other signal $\overline{\text{CHARGE}}$ is low when the charging current is on.

The charging circuitry should provide a current at an amplitude that is equal to the product of the battery capacity and the desired charge rate. For example, to charge a 1.2 ampere hour battery in 30 minutes, the current required would be 2.4 amps or 2C where 'C' is the battery capacity.

It is important to note that the ICS1700A does not control the current flowing into the battery in any way other than turning it on and off. The charging source should be a constant current type.

Table 2: Charge Rate List

Charge Rate	SW1-1 (S0)	SW1-2 (S1)	Topping Charge Pulse Rate	Maintenance Charge Pulse Rate	Fast Charge Timer Duration (after reset)
4C (15 min)	ON	ON	one every 40 sec	one every 160 sec	30 min
2C (30 min)	ON	OFF	one every 20 sec	one every 80 sec	60 min
1C (60 min)	OFF	ON	one every 10 sec	one every 40 sec	90 min
C/2 (120 min)	OFF	OFF	one every 5 sec	one every 20 sec	210 min

Operation

Before applying power to the board, ensure that the board is properly initialized.

- Set SW1-1 and SW1-2 for the correct charge rate.
- Check to make sure the divider resistors R6 and R8 are of the correct value to normalize the battery pack voltage to one cell.
- If applicable, choose resistors R1, R2 and R3 to obtain the required discharge current.

After applying power to the board:

- Set the external charging current source for the amplitude required by SW1 settings.

Push and hold the reset switch SW2 for at least 700ms. All LEDs should turn off while the switch is depressed. The green CM LED will light and will remain lit until full charge is detected by the ICS1700A. At that moment, the CM LED will start flashing at a 1 Hz rate, indicating that the topping charge stage has begun. The CM LED will flash until a reset is issued either by interrupting the power, removing the batteries or depressing the reset switch SW2.

Battery Polling

Upon power-up or after a reset is issued, any excess charge from filter capacitors at the +BAT and +CUR terminals is removed with a series of discharge pulses. After the discharge pulse series is complete, the voltage at VIN must be greater than 0.5V when a battery is present. If the voltage at VIN is less than 0.5V, the ICS1700A assumes no battery is attached and initiates a polling sequence.

The ICS1700A then applies a 100ms charge pulse. During the pulse, the ICS1700A monitors the VIN pin to determine if the divided down terminal voltage is greater than the internal 2.0V reference. If the battery is present, the voltage is clamped below the 2.0V reference when the current pulse is applied and the fast charge stage begins immediately. If a battery is not present, the voltage at VIN rises above the 2.0V reference and the BF LED lights immediately.

The charge pulses repeat for 10 seconds. If the battery is installed within 10 seconds, the ICS1700A will turn off the BF LED and enter the fast charge stage. If the battery is not installed within 10 seconds, the BF LED remains on and the ICS1700A shuts down. A reset must be issued to restart the controller after installing the battery.

Battery Fault Detection

The ICS1700A will turn on the BF LED and shut down if the battery is removed or if an open circuit occurs in the current path anytime after fast charge has been initiated. When in the topping charge or maintenance charge stages, a charge pulse may not occur for several seconds. During the period between charge pulses, the voltage at VIN should be greater than 0.5V if a battery is attached. If the voltage at VIN is less than 0.5V, the ICS1700A assumes the battery has been removed, a fault condition is indicated by the BF LED, and the controller shuts down.

Out-of-Temperature Range

The OT LED activates if the battery is either too hot or too cold to fast charge. If a thermistor is used, the ICS1700A employs internal voltage references to determine if a battery is hot or cold. *Note: Remove R9 and replace with a jumper when using a thermistor.* A 10kΩ @ 25°C thermistor with an external pull-up resistor is typically used. See the ICS1700A data sheet for additional information.

If a thermal switch is used, choose a switch that opens at 45°C or lower. If a thermal protection device is not used, the TS terminal must be grounded.

ICS strongly recommends the use of a thermal safety device in the battery pack. One source of thermal switches is Portage Electric Products, Inc., in North Canton, Ohio; (216) 499-2727. A source of thermistors is Semetic USA (Ishizuka Electronics Corp.), Babylon, NY; (516) 587-4086.

Application Note

ICS1700A Evaluation Board

Design Considerations

When designing external current source circuitry for use with the ICS1700A, there are several important considerations to make before starting the design and the PC board layout.

For the 2C and 4C charge rates, consideration has to be given to the use of a pulse-width modulated switch mode current source in order to reduce size and power dissipation. Switch mode current sources can provide the ability to charge battery packs that require voltages higher than the primary supply. For instance, to charge a 24 volt battery from a 12 volt vehicle battery, a switch mode boost converter could be used.

In general, linear chargers are less complex and more cost effective, but less efficient than switch mode chargers. For the 1C and C/2 charge rates, consideration should be given to using a linear charger unless the size and ability to dissipate heat are not available.

It is very important that care be taken to minimize noise coupling and ground bounce. In addition, wires and connectors can add significant resistance and inductance to the charge and discharge circuits.

When designing the printed circuit board, make sure ground and power traces are wide and bypass capacitors are used right at the controller pins. Use separate grounds for the signal, charge, and discharge circuits. Separate ground planes on the component side of the PC board are recommended. Be sure to connect these grounds together at the negative lead of the battery only.

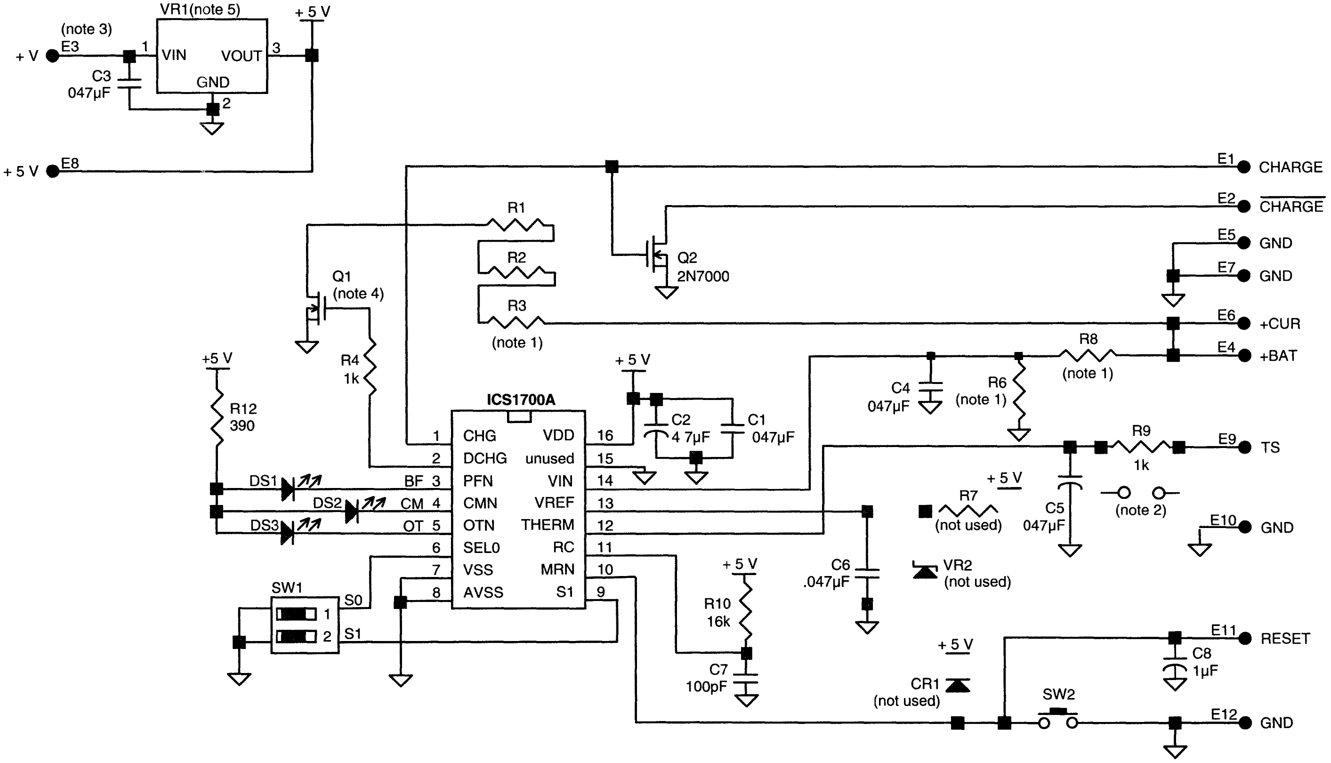
For the discharge circuit, keep the physical separation between power and return (ground) to a minimum to minimize field radiation effects. This precaution is also applicable to the constant current source, particularly if it is a switch mode type. Keep the ICS1700A and the constant current source control circuits outside the power and return loops described above. These precautions prevent high circulating currents and coupled noise from disturbing proper operation.

Integrated Circuit Systems wants to help create a successful battery charging solution using the ICS1700A. If you need technical advice or applications information, call the Power Management Products Applications department at (610) 630-5300.

Ordering Information

ICS1700AEB

Device Type
ICS1700A Evaluation Board



Notes.

1) Values are determined by number of cells and/or charge current, see text for details

2) Resistor R9 must be removed and replaced with a jumper when using a thermistor. Use of a thermistor requires an external pull-up resistor

3) 8 Vdc minimum input

4) Logic level compatible FET

5) LM340, AN7805 or equivalent

ICS1700A Evaluation Board

QuickSaver® Charge Controller for Nickel-Cadmium and Nickel-Metal Hydride Batteries

General Description

The **ICS1702** is a CMOS device designed for the intelligent charge control of either nickel-cadmium (NiCd) or nickel-metal hydride (NiMH) batteries. The controller uses a pulsed-current charging technique together with voltage slope and/or temperature slope termination. The **ICS1702** employs a four stage charge sequence that provides a complete recharge without overcharging. The controller has nine user-selectable charge rates and six user-selectable auxiliary modes available for customized charging systems.

The **ICS1702** monitors for the presence of a battery and begins charging when a battery is installed. Voltage and temperature are measured to ensure a battery is within fast charge conditions before charge is initiated.

Applications

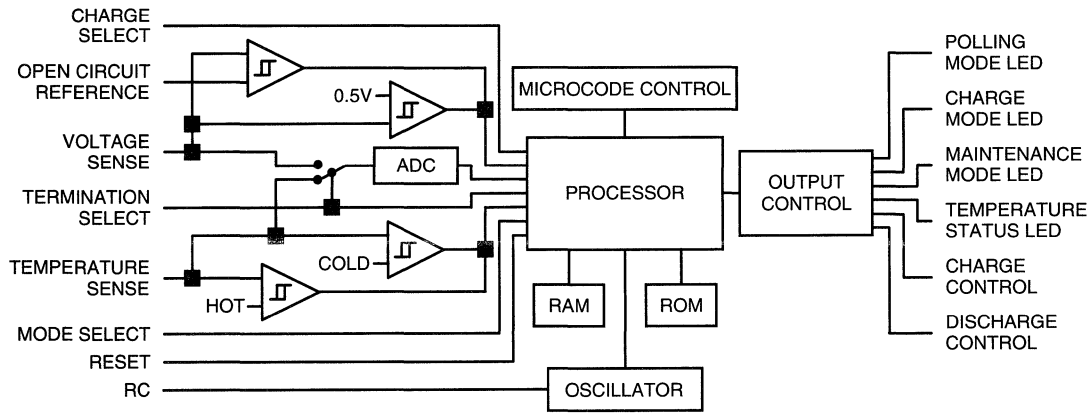
Battery charging systems for:

- Portable consumer electronics
- Power tools
- Audio/video equipment
- Communications equipment

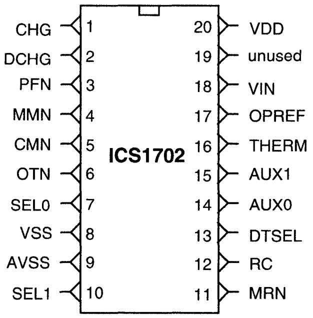
Features

- Multiple charge termination methods include:
  - Voltage slope
  - Temperature slope
  - Maximum temperature
  - Charge timer
- Four stage charge sequence:
  - Soft start charge
  - Fast charge
  - Topping charge
  - Maintenance charge
- Reverse-pulse charging available in all charge stages
- Nine programmable charge rates between 15 minutes (4C) and four hours (C/4)
- Out-of-temperature range detection
  - Hot battery: charger shutdown
  - Cold battery: low current charge
- Continuous polling mode for battery detection
- Six auxiliary modes include:
  - Discharge-before-charge
  - Ten hour C/10 conditioning charge
  - Direct to C/40 maintenance charge
  - Charging system test provided through controller
- Adjustable open circuit (no battery) voltage reference

Block Diagram



Pin Configuration



20-Pin DIP or SOIC
K-4, K-7

Pin Definitions

Pin Number	Pin Name	Type	Definition
1	CHG	OUT	Active high TTL compatible signal used to turn on an external current source to provide current to charge the battery.
2	DCHG	OUT	Active high TTL compatible signal available to turn on a discharge circuit.
3	PFN	OUT	Polling detect indicator. An active low turns on an external indicator to show the controller is polling for the presence of the battery.
4	MMN	OUT	Maintenance mode indicator. An active low turns on an external indicator showing the battery is either in the topping charge, maintenance charge or auxiliary condition mode. This signal is also applied with the out-of-temperature range indicator when the controller is in a cold battery charge mode The indicator flashes during the auxiliary discharge mode.
5	CMN	OUT	Charge mode indicator. An active low turns on an external indicator to show the controller is either in a soft start charge or fast charge.
6	OTN	OUT	Out-of-temperature range indicator. An active low turns on an external indicator showing the battery is out of the normal fast charge temperature range.
7	SEL0	IN	Tri-level input used with the SEL1 pin to program the device for the desired charge rate.
8	VSS		Ground.
9	AVSS		Ground.
10	SEL1	IN	Tri-level input used with the SEL0 pin to program the device for the desired charge rate.
11	MRN	IN	Master reset signal. A logic low pulse greater than 700 ms initiates a device reset.
12	RC	IN	An external resistor and capacitor sets the frequency of the internal clock.
13	DTSEL	IN	Selects temperature slope and/or voltage slope termination
14	AUX0	IN	Tri-level input used with the AUX1 pin to program the device for an auxiliary operating mode.
15	AUX1	IN	Tri-level input used with the AUX0 pin to program the device for an auxiliary operating mode.
16	THERM	IN	Thermistor or thermal switch input for temperature sensing.
17	OPREF	IN	Open circuit (no battery) voltage reference An external resistor divider on this pin sets the open circuit voltage reference used to detect the presence of a battery.
18	VIN	IN	Battery voltage normalized to one cell with an external resistor divider.
19	unused		Ground.
20	VDD		Device supply =+5.0 VDC

Note:
Pin 11 has an internal pull-up.
Pin 16 has an internal pull-up.
Pin 13 has an internal pull-down.
Pins 7, 10, 14, 15 float to 2.3V when unconnected.

Controller Operation

Charging Stages

The charging sequence consists of four stages. The application of current is shown graphically in Figure 1. The soft start stage gradually increases current levels up to the user selected fast charge rate during the first two minutes. The soft start stage is followed by the fast charge stage, which continues until termination. After termination, a two hour C/10 topping charge is applied. The topping charge is followed by a C/40 maintenance charge.

Soft Start Charge

Some batteries may exhibit an unusual high impedance condition while accepting the initial charging current, as shown in Figure 2. Unless dealt with, this high impedance condition can cause a voltage peak at the beginning of the charge cycle that would be misinterpreted as a fully charged battery by the voltage termination methods.

The soft start charge eases batteries into the fast charge stage by gradually increasing the current to the selected fast charge rate. The gradual increase in current alleviates the voltage peak. During this stage, only positive current pulses are applied to the battery. The duty cycle of the applied current is increased to the selected fast charge rate, as shown in Figure 3, by extending the current pulse on every cycle until the pulse is about one second in duration. The initial current pulse is approximately 200ms. The CMN indicator is activated continuously during this stage.

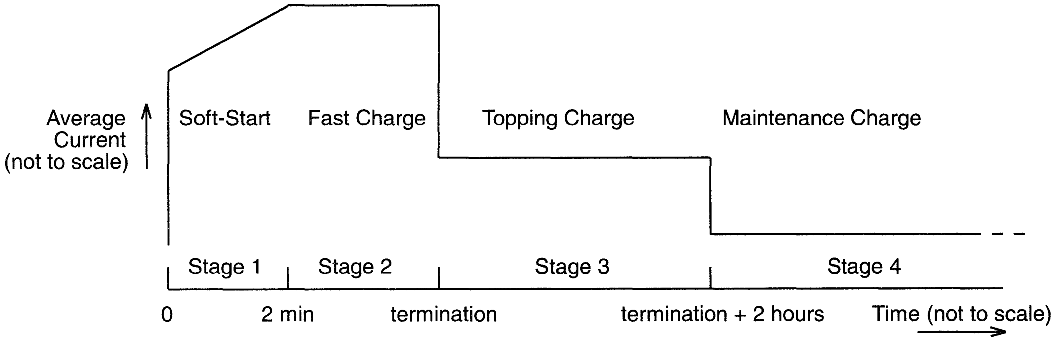


Figure 1: Graphical representation of average current levels during the four charging stages

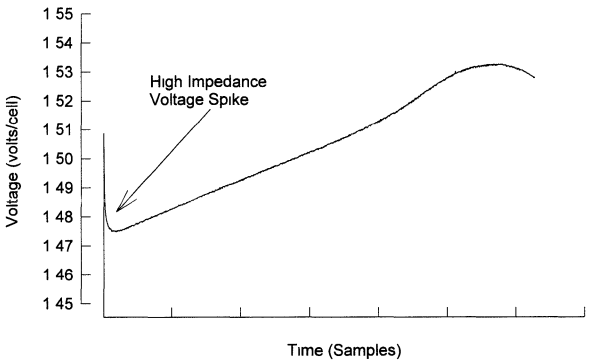


Figure 2: High impedance voltage spike at the beginning of charge

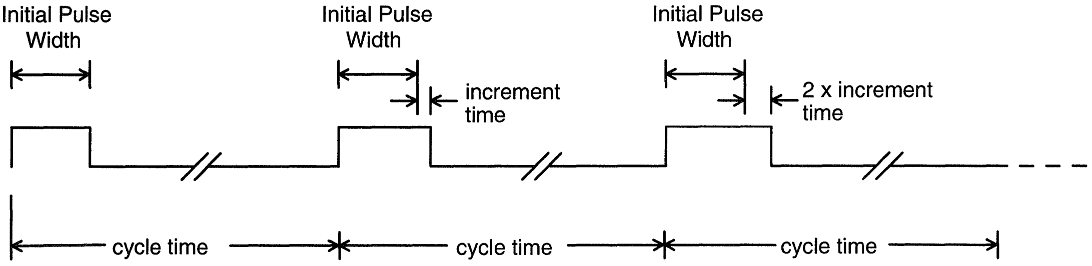


Figure 3: Cycle-to-cycle increase of the soft-start current pulse widths

Fast Charge

In the second stage, the **ICS1702** applies the charging current in a series of charge and discharge pulses. The technique consists of a positive current charging pulse followed by a high current, short duration discharge pulse. The cycle, shown with charge, discharge, rest and data acquisition periods in Figure 4, repeats every second until the batteries are fully charged.

The amplitude of the current pulse is determined by system parameters such as the current capability of the charging system, the desired charge rate, the cell capacity and the ability of that cell to accept the charge current. The **ICS1702** can be set for nine user-selectable fast charge rates from 15 minutes (4C) to four hours (C/4). Charge pulses occur approximately every second. The CMN indicator is activated continuously during this stage.

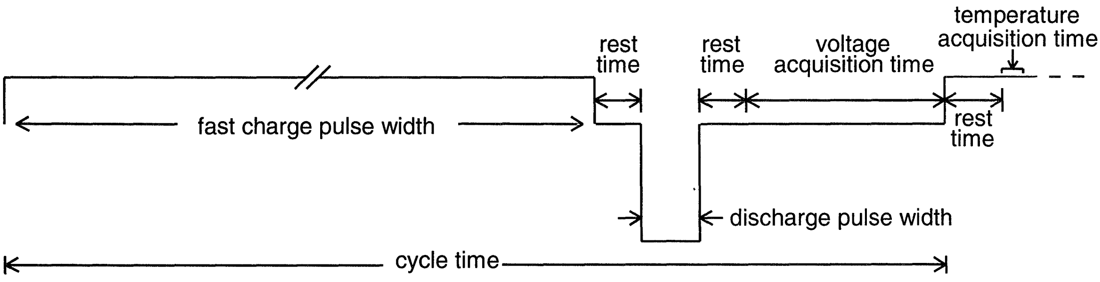


Figure 4: Charge cycle showing charge and discharge current pulses

The discharge current pulse amplitude is typically set to about 2.5 times the amplitude of the charging current based on 1.4V/cell. For example, if the charge current is 4 amps, then the discharge current is set at about 10 amps. The energy removed during the discharge pulse is a fixed ratio to the positive charge rate. The amplitude of the discharge pulse does not affect the operation of the part as described in this section.

A voltage acquisition window immediately follows a brief rest time after the discharge pulse. No charge is applied during the rest time or during the acquisition window to allow the cell chemistry to settle. Since no current is flowing, the measured cell voltage is not obscured by any internal or external IR drops or distortions caused by excess plate surface charge. The **ICS1702** makes one continuous reading of the no-load battery voltage during the entire acquisition window. The voltage that is measured during this window contains less noise and is a more accurate representation of the true state of charge of the battery. If temperature termination is selected, the thermistor voltage is sampled after a brief rest time once the current supply to the battery is turned on.

Topping Charge

The third stage is a topping charge that applies current at a rate low enough to prevent cell heating but high enough to ensure a full charge.

The topping charge applies a C/10 charging current for two hours. The current consists of the same pulse technique used during the fast charge stage; however, the duty cycle of the pulse sequence has been extended as shown in Figure 5. Extending the time between charge pulses allows the same charging current used in the fast charge stage so that no changes to the current source are necessary. For example, the same charge pulse that occurs every second at a 2C fast charge rate will occur every 20 seconds for a topping charge rate of C/10. The MMN indicator is activated continuously during this stage.

Maintenance Charge

The maintenance charge is intended to offset the natural self-discharge of NiCd or NiMH batteries by keeping the cells primed at peak charge. After the topping charge ends, the **ICS1702** begins this charge stage by extending the duty cycle of the applied current pulses to a C/40 rate. The maintenance charge will last for as long as the battery voltage is greater than 0.5V at the VIN pin, or, if the ten hour timer mode is enabled, until the timer stops the controller. The MMN indicator is activated continuously during this stage.

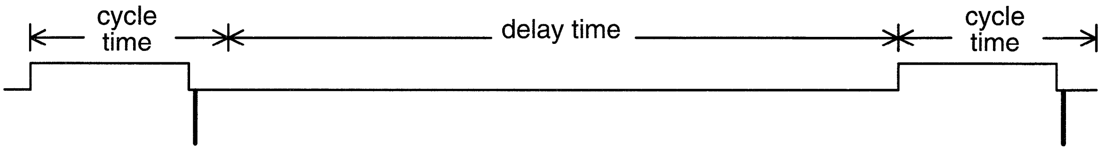


Figure 5: Representative timing diagram for topping and maintenance charge

Charge Termination Methods

Several charge termination schemes, including voltage slope, temperature slope, maximum temperature and two overall charge timers are available. The voltage slope and negative voltage slope methods may be used with or without the temperature slope and the maximum temperature method. Maximum temperature and the fast charge timer are available as backup methods.

Voltage Slope Termination

The most distinctive point on the voltage curve of a charging battery in response to a constant current is the voltage peak that occurs as the cell approaches full charge. By mathematically calculating the first derivative of the voltage, a second curve can be generated showing the change in voltage with respect to time as shown in Figure 6. The slope will reach a maximum just before the actual peak in the cell voltage. Using the voltage slope data, the **ICS1702** calculates the point of full charge and accurately terminates the applied current as the battery reaches that point. The actual termination point depends on the charging characteristics of the particular battery.

Cells that are not thoroughly conditioned or possess an unusual cell construction may not have a normal voltage profile. The **ICS1702** uses an alternate method of charge termination based on a slight decrease in the voltage slope to stop charge to cells whose voltage profile is very shallow. This method looks for a flattening of the voltage slope which may indicate a shallow peak in the voltage profile.The zero slope point occurs slightly beyond the peak voltage and is shown on the voltage curve graph.

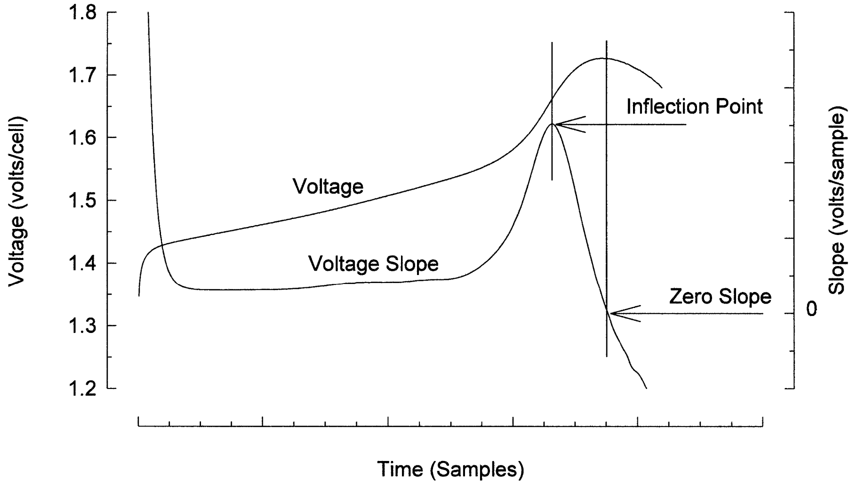


Figure 6: Voltage and slope curves showing inflection and zero slope points

Temperature Slope Termination

Temperature slope termination is based on the battery producing an accelerated rate of heating as the amount of readily chargeable material dimishes at full charge. An increase in battery (cell) heating due to the charging reaction will occur at a much faster rate than a change due to a warming ambient temperature. Note the effect of 0.5°C fluctuations in ambient temperatures resulting in slight variations in the temperature slope as shown in Figure 7. However, the increase in cell temperature near the end of charge causes a much larger change in the temperature slope that can be easily detected and used as a trigger for fast charge termination.

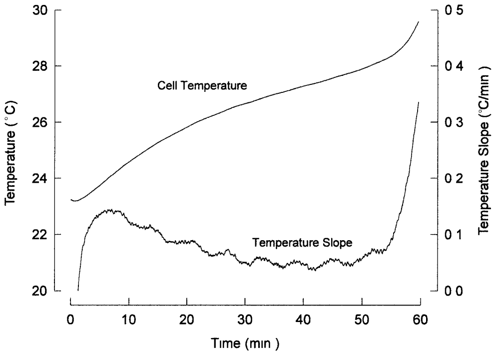


Figure 7: Cell temperature and temperature slope

The rate of change in cell temperature can be determined by measuring the change in voltage across a negative temperature coefficient thermistor as shown in Figure 8. The resistance of an NTC thermistor changes in proportion in the change in temperature of the thermistor. The **ICS1702** measures the decreasing resistance as a drop in voltage and calculates the thermistor voltage slope, shown in Figure 8. The controller terminates fast charge based on the selected charge rate and the calculated slope.

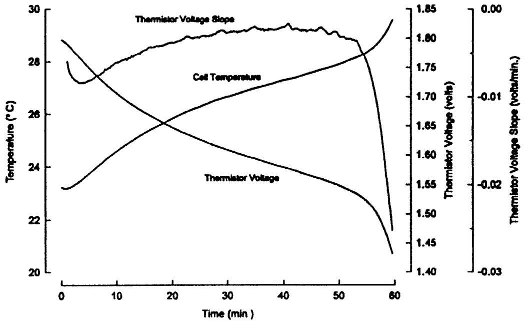


Figure 8: Cell temperature and thermistor voltage slope

Table 1 shows the decrease in thermistor voltage the last minute before full charge required by the **ICS1702** at various charge rates. The thermistor voltage slope should exceed the listed value to ensure charge termination. Note that changes in thermistor location, cell size or large ambient temperature fluctuations can affect the slope to some degree. Refer to the *Applications Information* section and *Temperature Slope and Maximum Temperature* section for more information on thermistor mounting.

Table 1: Slope vs. Charge Rate

Charge Rate	Thermistor Voltage Slope (-V/min.)
>C/2	0.040
C/2 to C/3	0.028
<C/3	0.018

To determine the required thermistor characteristics for proper temperature slope termination, the battery temperature rise must be known or determined for the last minute prior to full charge.

Maximum temperature termination is also enabled when temperature slope termination is used. Care must be taken to keep voltage levels at the THERM pin within the fast charge range (between 2.4V and 0.93V), as shown in Figure 9.

Maximum Temperature Termination

Maximum temperature can be sensed using either a NTC thermistor or a thermal switch. Maximum temperature termination can also be bypassed if desired, although it is strongly recommended that some form of temperature termination be used.

If an NTC thermistor is used, an internal voltage threshold determines when the battery is too hot to charge. As temperature increases, the voltage across the thermistor will drop. This voltage is continually compared to the internal voltage threshold. If the thermistor voltage drops below the internal threshold, the OTN indicator is activated and the controller shuts down. The controller must be reset once the hot battery fault condition has cleared to restart the charge sequence.

If a thermal switch is used, a 45°C open circuit switch is recommended. When the thermal switch opens, an internal pull-up at the THERM pin results in a logic high which shuts down the controller and activates the OTN indicator. The controller must be reset once the hot battery fault condition has cleared to restart the charge sequence.

Maximum temperature termination can be disabled by grounding the THERM pin. See the section on *Temperature Sensing* for more information.

Fast Charge Timer Termination

The controller uses a timer to limit the fast charge duration. These times are pre-programmed, and are automatically adjusted in time duration according to the charge rate selected. Fast charge timer termination is best suited as a safety backup feature to limit the duration of the fast charge stage. The fast charge timer is always enabled and cannot be disabled. See Table 4 in the section *Charge Rate Selection* for more information.

Battery Detection

Upon power-up or after a master reset, excess charge from output filter capacitors at the charging system terminals is removed with a series of discharge pulses. After the discharge pulse sequence is complete, the voltage at VIN must be greater than 0.5V when a battery is present. If the voltage at the pin is less than 0.5V, the **ICS1702** assumes no battery is present, and the polling detect mode is initiated. No indicator is active during the discharge pulses.

The **ICS1702** enters the polling detect mode and applies a 100ms charge pulse. During the pulse, the **ICS1702** monitors the VIN pin to determine if the divided down terminal voltage is above OPREF. If the battery is present, the voltage will be clamped below the reference on OPREF while the current pulse is applied. If a battery is not present, the voltage at VIN will rise above the reference at OPREF.

The charge pulse will repeat at one second intervals until the battery is reinstalled. The polling detect indicator (PFN) is the only indicator active as long as the **ICS1702** is in the polling detect mode. Once a battery is installed, the **ICS1702** will turn off the PFN indicator and enter the soft start stage. The **ICS1702** will automatically re-enter the polling detect mode if the battery is removed.

Battery Removal

During the application of a charge pulse, the voltage at the VIN pin is compared to the voltage at the OPREF pin. If the voltage at VIN is greater than the voltage at OPREF during the application of the current pulse, then the battery is assumed to have been removed and the **ICS1702** enters the polling detect mode. If the voltage at VIN is below the voltage at OPREF, the charging mode continues.

When in the topping charge or maintenance charge stages, a charge pulse may not occur for several seconds. During the period between charge pulses, the voltage at VIN must be greater than 0.5V if a battery is attached. If the voltage at VIN is less than 0.5V, the **ICS1702** assumes the battery has been removed, and the polling detect mode is initiated.

Auxiliary Modes of Operation

The **ICS1702** allows six alternate modes of operation to help customize the charging system for certain applications. The tri-level AUX0 and AUX1 pins are used to select the operating mode. The AUX0 and AUX1 pins default the **ICS1702** into fast charge operation. Except for the discharge-to-charge mode, another mode can only be selected by re-programming and resetting the controller.

Discharge-to-Charge Mode

The time required for discharge depends on the energy in the battery and the discharge rate. The discharge is not limited by a timer. This allows the user to set the discharge rate. The battery is drained to 1 volt/cell as read at the VIN pin under load and then the controller enters soft start at a charge rate set by the SEL0 and SEL1 inputs. The discharge load is activated by the DCHG pin which goes low for about 400ms every second. A resistor value selected for a 2.5C discharge based on 1.4V/cell results in about a 1C discharge rate.

The discharge-to-charge mode can be entered by placing the AUX0 pin high (H) and the AUX1 pin low (L) with the SEL0 and SEL1 inputs set for the desired fast charge rate. This setting initializes the discharge sequence. The **ICS1702** enters the discharge-to-charge mode at initial power-up or with a master reset. The discharge mode occurs first, to be followed by the selected fast charge mode. During discharge, the MMN indicator flashes at a one second rate, while during the soft start and fast charge stages the CMN indicator is activated continuously.

Four charge modes are available after the discharge portion is complete by changing the state of the AUX inputs during the discharge portion of this mode. The available charge modes are:

- Fast Charge: Leave the AUX inputs open (Z).
- Direct Maintenance Mode: Set the AUX0 low (L) and AUX1 high (H).
- Condition Mode: Set AUX0 high (H) and AUX1 open (Z).
- Ten-Hour Timer Mode: Set AUX0 high (H) and AUX1 high (H).

If the battery is removed while in the discharge-to-charge mode, the **ICS1702** will continually reset itself until the battery is reinstalled. See *Application Information* for more information.

Discharge-Only Mode

The time required for discharge depends on the energy in the battery and the discharge rate. The discharge is not limited by a timer. This allows the user to set the discharge rate. The battery is drained to 1 volt/cell as read at the VIN pin under load. The **ICS1702** shuts down after the discharge sequence is finished and a master reset must be performed to reactivate the device. The discharge load is activated by the DCHG pin which goes low for about 400ms every second. A resistor value selected for a 2.5C discharge based on 1.4V/cell results in about a 1C discharge rate. The discharge-only mode can be entered by placing the AUX0 pin open (Z) and the AUX1 pin low (L). The **ICS1702** enters this mode at initial power-up or with a master reset. During the discharge portion, the MMN indicator flashes at a one second rate.

Direct Maintenance Mode

The **ICS1702** can enter directly into the C/40 maintenance mode for cells that require a maintenance charge only. The direct maintenance mode is activated by setting the AUX0 pin low (L) and the AUX1 pin high (H), and resetting the device. The SEL0 and SEL1 pins must be set based on the charging current and the battery capacity. The formula

$$\frac{\text{Charging Current (Amps)}}{\text{Battery Capacity (Amp} \bullet \text{hr)}}$$

gives the charge rate. Use Table 4 to find the correct SEL0 and SEL1 settings. The maintenance charge is applied until the battery is removed, upon which the **ICS1702** will enter the polling detect mode. The **ICS1702** will enter the direct maintenance mode upon initial power-up or after a master reset. The MMN indicator will be active during this mode.

Conditioning Mode

The **ICS1702** can enter a conditioning mode which applies a C/10 charge for a timed 10 hour period, followed by an indefinite C/40 maintenance charge until the batteries are removed.

The conditioning mode can be entered by setting the AUX0 pin high (H) and the AUX1 pin open (Z). The SEL0 and SEL1 pins must be set based on the charging current and the battery capacity. The formula

$$\frac{\text{Charging Current (Amps)}}{\text{Battery Capacity (Amp} \bullet \text{hr)}}$$

gives the charge rate. Use Table 4 to find the correct SEL0 and SEL1 settings. The MMN indicator will be active during the 10 hour conditioning charge and the maintenance charge that follows. The **ICS1702** enters the polling detect mode if the battery is removed.

Ten Hour Timer Mode

Placing the AUX0 and AUX1 pins both high (H) enables a ten hour timer. This timer limits the total charge, including the maintenance charge, to approximately ten hours for a battery that is completely discharged before fast charge is initiated. The ten hour limit is based on the assumption that the charge terminates due to the fast charge timer as shown in Table 2.

Charging System Test

The system test mode is intended for use in applications where the charging system functionality needs to be tested. The system test sequence consists of a one second activation of the CMN, MMN and PFN indicator pins as well as the CHG and DCHG lines. The OTN indicator is not activated. The system test mode is entered by placing both the AUX0 and AUX1 pins low (L). The **ICS1702** shuts down after the test sequence is finished and a master reset must be performed to reactivate the device.

Cold Battery Charging

Cold battery charging is activated if a voltage at the THERM pin is in the cold battery voltage range, as shown in Figure 9. The **ICS1702** checks for a cold battery before initiating fast charge. If a cold battery is present before fast charge begins, the **ICS1702** begins a two hour C/10 topping charge (the pulsed duty cycle is based on the selected charge rate). If the battery is still cold after the two hour topping charge is complete, the **ICS1702** begins a C/40 maintenance charge. The maintenance charge will continue for as long as the battery remains cold unless the ten hour time mode is selected. The thermistor voltage at the THERM pin is checked every second to see if the battery has warmed up. If so, the **ICS1702** stops the topping or maintenance charge and begins a fast charge at a rate selected by the SEL0 and SEL1 inputs. A cold battery does not interfere with the condition mode, direct maintenance mode, the discharge portion of the discharge-to-charge mode, or the discharge-only mode as programmed by the AUX0 and AUX1 pins. See the section on *Temperature Sensing,* for more information.

The MMN and OTN indicators will be active, indicating that a low current charge is being applied to a battery that is outside the specified temperature range for fast charging. If the CMN and OTN indicators are active see the *Application Information* section.

Table 2: Ten Hour Timer Information

Charge Rate	Fast Charge Timer Cutoff	Maintenance Timer Cutoff (after fast charge termination)	Charge Time Limit (from reset)
4 C	0.3 hrs	9.7 hrs	10 hrs
2 C	0.6 hrs	9 4 hrs	10 hrs
1.3 C	0.9 hrs	9.1 hrs	10 hrs
1 C	1.2 hrs	8.8 hrs	10 hrs
C/1.5	1.8 hrs	8.2 hrs	10 hrs
C/2	2 4 hrs	7.6 hrs	10 hrs
C/2.5	3.5 hrs	6.5 hrs	10 hrs
C/3	4.0 hrs	6.0 hrs	10 hrs
C/4	4.6 hrs	5.4 hrs	10 hrs

Pin Descriptions

The **ICS1702** requires some external components to control the clock rate, sense temperature and provide an indicator display. The controller must be interfaced to an external power source that will provide the current required to charge a battery pack and, if desired, a circuit that will sink discharge current.

Output Logic Signals: CHG, DCHG Pins

The CHG and DCHG pins are active high, TTL compatible outputs. In addition to being TTL compatible, the CMOS outputs are capable of sourcing current which adds flexibility when interfacing to other circuitry. A logic high on the CHG pin indicates that the charging current supply should be activated. If applicable, a logic high on the DCHG pin indicates that the discharge circuit should be activated.

Care must be taken to control wiring resistance and inductance. The load resistor must be capable of handling this short duration high-amplitude pulse. If the auxiliary discharge-to-charge mode is selected, the power dissipation of the load resistor must be properly selected to accept the extended length of the discharge pulse.

Indicators: CMN, MMN, PFN, OTN Pins

The controller has four outputs for driving external indicators. These pins are active low. The four indicator outputs have open drains and are designed to be used with LEDs. Each output can sink over 20mA which requires the use of an external current limiting resistor. The four indicator signals denote fast charge stage, topping and maintenance stages, and the polling detect and out-of-temperature range modes as shown in Table 3.

The charge mode (CMN) indicator is activated continuously during the soft start and fast charge stages. When the controller enters the topping charge stage, the output goes high and the indicator turns off.

The maintenance mode (MMN) indicator is on when the **ICS1702** is either in the topping charge, maintenance charge, direct maintenance mode, or the condition mode. The MMN indicator is also lit in conjunction with the OTN indicator when cold battery charging is in progress. The maintenance mode indicator flashes at a one second rate when the **ICS1702** is controlling the discharge portion of the discharge-to-charge or the discharge-only mode.

The polling detect (PFN) indicator is on when the **ICS1702** polls for a battery. The controller applies periodic charge pulses to detect the presence of a battery. The indicator is a warning that these charge pulses are appearing at the charging system terminals at regular intervals. When a battery is detected, the indicator is turned off.

The out-of-temperature range (OTN) indicator is active whenever the voltage at the temperature sense (THERM) input enters a range that indicates that the attached battery is too hot to charge. The OTN indicator is also activated with the MMN indicator if the controller is initialized with the battery in the cold battery charge region.

Charge Rate Selection: SEL0, SEL1 Pins

The SEL0 and SEL1 inputs must be programmed by the user to inform the **ICS1702** of the desired charge rate. When left unconnected (open), these tri-level pins will float to about 2.3V. When a low level is required, the pin must be grounded. When a high level is required, the pin must be tied to V_{DD}. The voltage ranges for low (L), open (Z) and high (H) are listed in Table 10, *DC Characteristics*. To program the SEL0 and SEL1 inputs, refer to the *Charge Rate List* in Table 4.

The **ICS1702** does not control the current flowing into the battery in any way other than turning it on and off. The required current for the selected charge rate must be provided by the user's power source. The external charging circuitry should provide current at the selected charge rate. For example, to charge a 1.2 ampere hour battery in 30 minutes (2C), approximately 2.4 amperes of current is required.

Table 3: Indicator Description List

PFN	MMN	CMN	OTN	Description
on				Polling detect mode
	on			Maintenance or topping charge, direct maintenance or condition mode
		on		Fast charge
			on	Hot battery shutdown
	on		on	Cold battery charge
	flash			Discharge portion of the discharge-to-charge or discharge-only mode
		flash		see Applications Information
		on	on	see Applications Information
	flash	flash		see Applications Information
	flash		on	see Applications Information

Table 4: Charge Rate List

SEL0	SEL1	Charge Rate	Topping Charge Pulse Rate	Maintenance Charge Pulse Rate	Fast Charge Timer Duration (after reset)
L	L	4C (15 min)	one every 40 sec	one every 160 sec	21 min
L	H	2C (30 min)	one every 20 sec	one every 80 sec	39 min
L	Z	1.3C (45 min)	one every 13 sec	one every 53 sec	57 min
H	L	1C (60 min)	one every 10 sec	one every 40 sec	75 min
H	Z	C/1.5 (90 min)	one every 7 sec	one every 27 sec	110 min
H	H	C/2 (120 min)	one every 5 sec	one every 20 sec	144 min
Z	L	C/2.5 (150 min)	one every 4 sec	one every 16 sec	212 min
Z	Z	C/3 (180 min)	one every 3 sec	one every 13 sec	244 min
Z	H	C/4 (240 min)	one every 2 sec	one every 10 sec	275 min

See the section on *Controller Operation* for additional information on the topping charge and maintenance charge. See the section on *Charge Termination Methods* for additional information on the charge timer.

Mode Selection: AUX0, AUX1 Pins

The AUX0 and AUX1 inputs must be programmed by the user to inform the **ICS1702** of the desired auxiliary mode. When left unconnected (open) these tri-level pins will float to about 2.3V. When a low level is required, the pin must be grounded. When a high level is required, the pin must be tied to V_{DD}. The voltage ranges for low (L), open (Z) and high (H) are listed in Table 10, *DC Characteristics*. To program the AUX0 and AUX1 inputs, refer to the Mode Select List in Table 5. See the section on Auxiliary Modes of Operation for additional information.

Table 5: Mode Select List

AUX0	AUX1	Mode Selected	Mode Operation
L	L	Charging System Test	Charging system test for embedded applications
L	H	Direct Maintenance	Indefinite C/40 maintenance charge
Z	Z	Fast Charge	Default
Z	L	Discharge-Only	Battery discharge to 1V/cell
H	L	Discharge-to-Charge	Battery discharge to 1V/cell followed by the selected charge mode
H	Z	Condition	Timed C/10 topping charge followed by a C/40 maintenance charge
H	H	Ten Hour Timer	Limits total charge including the maintenance charge to 10 hours

Master Reset: MRN Pin

The MRN pin is provided to re-program the controller for a new mode or charging sequence. This pin has an internal pull-up of about 75kΩ. A logic low on the MRN pin must be present for more than 700ms for a reset to occur. As long as the pin is low, the controller is held in a reset condition. A master reset is required to clear a temperature fault condition, clear the charging system test, reset the ten hour timer or change charge rates or auxiliary modes. Upon power-up, the controller automatically resets itself.

Clock Input: RC Pin

The RC pin is used to set the frequency of the internal clock when an external 1 MHz clock is not available. An external resistor must be connected between this pin and V_{DD}. An external capacitor must be connected between this pin and ground. The frequency of the internal clock will be about 1 MHz with a 16kΩ resistor and a 100pF capacitor. All time durations noted in this document are based on a 1 MHz clock. Operating the clock at a lower frequency will proportionally change all time durations. Operating the clock at a frequency significantly lower than 1 MHz, without adjusting the charge current accordingly, will lessen the effectiveness of the fast charge timer and lower the accuracy of the controller. Operating the clock at a frequency greater than 1 MHz will also change all time durations and, without adjusting the charge current accordingly, may cause termination to occur due to the fast charge timer expiring rather than by the battery reaching full charge.

The clock may be driven by a 1 MHz external 0 to 5V pulse provided the duty cycle is between 10% and 60%. The clock input impedance is about 1kΩ.

Temperature Sensing: THERM Pin

The THERM pin is provided for hot and cold battery detection and for temperature slope termination of fast charge when used in conjunction with an NTC thermistor. The THERM pin also provides for hot battery and maximum temperature termination when used in conjunction with a normally closed thermal switch. Several internal voltage thresholds are used by the controller depending on whether a thermistor or a thermal switch is used. Figure 9 shows the internal thresholds over laid on a typical thermistor curve.

- Using an NTC thermistor for hot and cold battery detection:

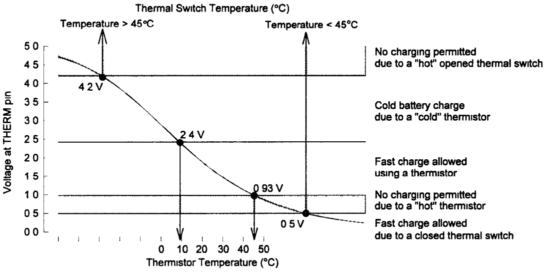


Figure 9: Voltage levels for temperature sensing with a thermistor or thermal switch

The THERM pin requires some thought if a thermistor is going to be used for hot and cold battery detection. The example below works for a typical 10kΩ @ 25°C NTC thermistor. Consider using the controller to prevent charging above 45°C and reducing the current below 10°C. At 10°C the resistance of the thermistor is 18kΩ. At 45°C, the resistance drops to 4.7kΩ. The **ICS1702** has an internal voltage threshold at 10°C at 2.4V, and an internal voltage at 45°C at 0.93V as shown in Figure 9. At 25°C the voltage at the THERM pin is set at the midpoint of the thresholds:

$$0.93\text{V} + \frac{2.40\text{V} - 0.93\text{V}}{2} = 1.67\text{V}.$$

The THERM pin has a 75kΩ internal pull-up (R_{pu}). Using a resistor divider with 10kΩ for the thermistor (R_{th}) and a external fixed resistor (R_{fix}), the divider looks like Figure 10 at 25°C:

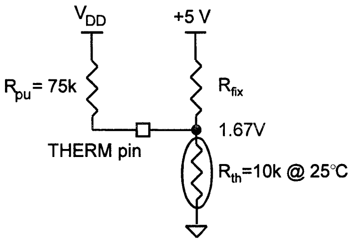


Figure 10: Voltage divider at the THERM pin at 25°C

To set the voltage at the THERM pin for 1.67V at 25°C, the equivalent divider looks like Figure 11.

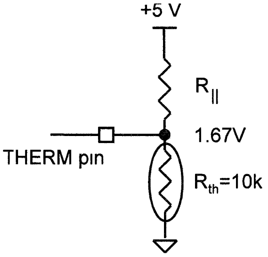


Figure 11: Equivalent voltage divider

The parallel resistance $R_{||}$ is calculated:

$$R_{||} = \frac{5V - 1.67V}{1.67V/10k\Omega} = 20k\Omega$$

The internal pull-up resistance R_{pu} and the parallel resistance $R_{||}$ are known so the external fixed resistor can be calculated from:

$$R_{fix} = \frac{R_{pu}R_{||}}{R_{pu} - R_{||}}.$$

Substituting in known values: R_{fix} = 27.27kΩ. A 27kΩ standard value is used for R_{fix}.

Since the thermistor resistance R_{th} is specified by manufacturers at a particular temperature, the voltage across the thermistor V_{th} at that temperature can be calculated from:

$$V_{th} = \frac{R_{th}}{R_{||} + R_{th}} (5V),$$

with the drop across the resistor divider equal to 5V. For this example, the calculated voltage with R_{th}=18kΩ at 10°C is 2.37V and with R_{th}=4.7kΩ at 45°C the voltage is 0.95V. Table 6 lists the internal thresholds for hot and cold battery detection. If the voltage across the thermistor (at the THERM pin) drops below 0.93V, the **ICS1702** will shut down due to a hot battery fault condition and will not restart unless reset. If the voltage dropped across the thermistor is above 2.4V before fast charge is initiated, the **ICS1702** will begin a reduced current charge. See the *Cold Battery Charging* section for more information.

Table 6: Thermistor Voltage Thresholds

Parameter	Voltage	Battery Temperature
Cold Battery Thermistor Voltage	>2.4	<10°C
Hot Battery Thermistor Voltage	<0.93	>45°C

- Using an NTC thermistor for temperature slope termination:

As a battery approaches full charge, its accelerated rate of heating can be used to terminate fast charge by detecting the large change in the temperature slope. The large change in temperature slope is proportional to the thermistor voltage change per unit of time. If the DTSEL pin is programmed for temperature slope termination, the controller will calculate the thermistor voltage slope and terminate based on internally set thresholds as listed in Table 1. The threshold is 40mV per minute for selected charge rates greater than C/2, 28mV per minute for charge rates selected at or between C/2 and C/3, and 18mV per minute for selected charge rates less than C/3. The voltage across the thermistor must change at these rates or greater to terminate the selected charge rate.

These thresholds correspond to a set change in thermistor resistance when an external pull-up to 5V is used as shown in Figure 11. Using the values calculated from the hot and cold battery detection example, the percent change in the thermistor resistance per minute for selected charge rates are provided. For selected charge rates greater than C/2, the thermistor resistance must decrease 4%/min. to terminate charge. For selected charge rates at or between C/2 and C/3, the thermistor resistance must decrease 3%/min. to terminate charge. For selected charge rates less than C/3, the thermistor must decrease 2%/min. to terminate charge.

For example, a battery was monitored as it charged at a 1C rate in 25°C ambient. In the final minute of charge, the battery temperature rose from 29.8°C to 31°C where full charge was detected. With this data, the typical 10kΩ @ 25°C thermistor used in the example above is checked to determine if its characteristics satisfy the 4% decrease in resistance required for the last minute of charge. The thermistor measures 8.37kΩ @ 29.8°C and 8.01kΩ at 31°C. For a 1C charge rate, the resistance must decrease at least 4%/min. or more between 29.8°C and 31°C. The percent decrease in resistance for the thermistor is calculated as:

$$\frac{8.37k\Omega - 8.01k\Omega}{8.37k\Omega}(100) = 4.30\%.$$

This thermistor meets the 4%/min. requirement and will result in termination at full charge at 31°C. The thermistor must be checked for a 4%/min. decrease in resistance for the last minute of charge near the hot and cold battery thresholds.

The battery in the example above was charged in a 25°C ambient with its temperature rising 31°C - 25°C or 6°C. The temperature rise was 31°C - 29.8°C or 1.2°C in the last minute before full charge occurred. This information is used to check the thermistor characteristics at the ambient extremes. If the selected 1C charge rate is initiated at 12°C, the thermistor resistance change must decrease 4%/min. between 16.8°C and 18°C. The thermistor resistance at 16.8°C is 13.68kΩ and at 18°C the thermistor resistance is 13.06kΩ.

$$\frac{13.68k\Omega - 13.06k\Omega}{13.68k\Omega}(100) = 4.53\%$$

The thermistor meets the 4%/min. requirement and will result in termination of fast charge at 18°C. If the selected 1C charge rate is initiated at 37°C, the thermistor resistance change must decrease 4%/min. between 41.8°C and 43°C. The thermistor resistance at 41.8°C is 5.48kΩ and at 43°C the thermistor resistance is 5.25kΩ.

$$\frac{5.48k\Omega - 5.25k\Omega}{5.48k\Omega}(100) = 4.19\%$$

The thermistor meets the 4%/min. requirement and will result in termination of fast charge at 43°C.

The 4%/min., 3%/min. and 2%/min. decrease in thermistor resistance for the last minute of charge for the selected charge rate are applicable for NTC thermistors other than 10kΩ @ 25°C provided that the following requirements are met:

- An external pull-up resistor to 5V is used to provide a thermistor voltage of 1.67V @ 25°C.
- The thermistor resistance at 25°C does not exceed 20kΩ so that accuracy and adequate noise immunity are maintained.
- The thermistor resistance increases by a factor of about 1.8 from 25°C to 10°C and the thermistor resistance decreases by a factor of about 2.1 from 25°C to 45°C.

• Using a thermal switch for hot battery detection:

A thermal switch that opens at about 45°C is recommended. The thermal switch must be connected between the THERM pin and ground. When the thermal switch is closed, the voltage at the THERM pin must be below 0.5V for normal operation. When the thermal switch opens (see Figure 12), the internal pull-up at the THERM pin will raise the voltage above 4.2V and the **ICS1702** will shut down and will not restart unless reset. Table 7 contains the internal voltage thresholds used with a thermal switch.

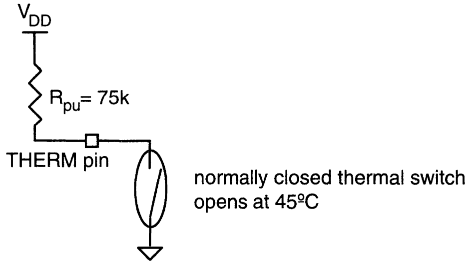


Figure 12: Thermal switch to connection to ground at the THERM pin

Table 7: Thermal Switch Voltage Thresholds

Parameter	Voltage	Battery Temperature
Opened Thermal Switch Voltage	>4.2	>45°C
Closed Thermal Switch Voltage	<0.5	<45°C

- Using no temperature sensor:

If a temperature sensor is not used, the THERM pin must be grounded.

Termination Selection: DTSEL Pin

The **ICS1702** has the capability of either temperature slope termination, voltage slope termination or both methods simultaneously. The DTSEL pin has an internal 75kΩ pull-down resistor that enables voltage slope termination as the primary method and is the default condition. Tying the pin high enables both temperature slope and voltage slope termination methods. Temperature slope termination as the primary method is enabled by tying the DTSEL pin to the CMN output (pin 5). CMN must have an external 15kΩ or lower value pull-up resistor to V_{DD} for proper activation of temperature slope termination. The **ICS1702** must be reset if a new termination method is desired. Table 8 summarizes the DTSEL pin settings. NOTE: Maximum temperature and fast charge timer termination methods are always enabled when using temperature slope termination. Refer to the sections on *Fast Charge Timer Termination* and *Maximum Temperature Termination* for more information.

Table 8: Termination Select List

Tie DTSEL Pin to ...	Result
Low (No Connect)	Voltage slope termination only
High	Voltage slope and temperature slope termination
CMN	Temperature slope termination only (CMN with external pull-up to V_{DD})

Voltage Input: VIN Pin

The battery voltage must be normalized by an external resistor divider network to one cell. The electrochemical potential of one cell is about 1.2V. For example, if the battery consists of six cells in series, the voltage at the VIN pin must be equal to the total battery voltage divided by six. This can be accomplished with two resistors, as shown in Figure 13. To determine the correct resistor values, count the number of cells to be charged in series. Then choose either R1 or R2 and solve for the other resistor using:

$$R1 = R2 \times (\#\text{ of cells} - 1) \text{ or } R2 = \frac{R1}{(\#\text{ of cells} - 1)}$$

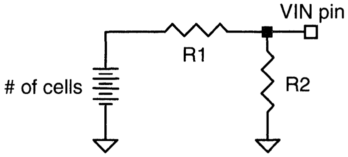


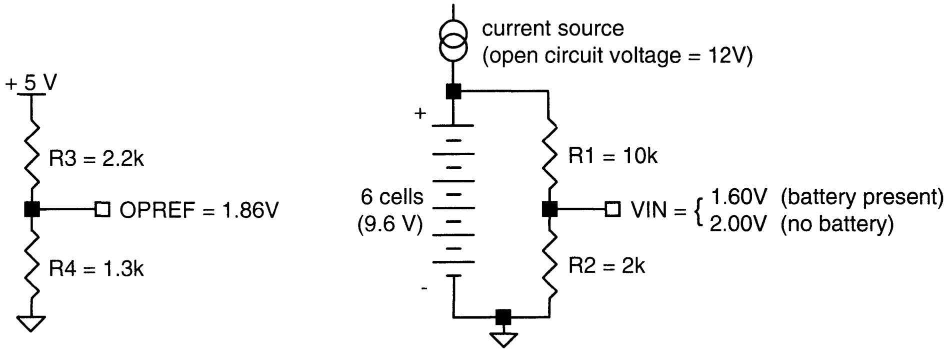
Figure 13: Resistor divider network at the VIN pin

Open Circuit Voltage Reference: OPREF Pin

The OPREF pin requires an external resistor divider to establish the open circuit (no battery) voltage reference. The purpose of this voltage reference is to detect the removal of the battery from the charging system. The voltage at this pin is compared to the voltage at the VIN pin when the current source is turned on. If the voltage at VIN is greater than the voltage at OPREF, the **ICS1702** assumes the battery has been removed and the **ICS1702** enters the polling detect mode.

For proper operation, the voltage at OPREF must be set between the (divided down) open circuit voltage produced by the current source and the maximum normalized battery voltage. An example is shown in Figure 14.

Suppose that a current source has an open circuit voltage of 12V. The maximum expected battery voltage of a six-cell pack is determined to be 9.6V. The voltage at OPREF should be set at a point between 1.6V (9.6V/6 cells=1.6V) and 2V (12V/6=2V). This is accomplished with a resistor divider network. In this example, R4 and R3 are referred to V_{DD}. Refer to the VIN and OPREF divider resistor tables in the *Applications Information* section. From the VIN table, the divider resistors are 10kΩ and 2kΩ for R1 and R2. From the OPREF table, the divider resistors are 2.2kΩ and 1.3kΩ for R3 and R4. If R3 is 2.2kΩ and R4 is 1.3kΩ, the voltage at OPREF is 1.86V.



Resistor divider at the OPREF pin

Resistor divider at the VIN pin

Figure 14: Open Circuit Reference Example

Power: VDD Pin

The power supply for the device must be connected to the VDD pin. The voltage should be +5 VDC and should be supplied to the part through a regulator that has good noise rejection and an adequate current rating. The controller requires up to a maximum of 11mA with V_{DD}=5.00V.

Grounding: VSS, AVSS Pins

There are two ground pins. Both pins must be connected together at the device. This point must have a direct connection to a solid ground plane.

Data Tables

Table 9: Absolute Maximum Ratings

Supply Voltage	6.5	V
Logic Input Levels	-0.5 to V_{DD} + 0.5	V
Ambient Operating Temperature	0 to 70	°C
Storage Temperature	-55 to 150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at the Absolute Maximum Ratings or other conditions not consistent with the characteristics shown in this document is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 10: DC Characteristics

T_{amb}=25°C. All values given are typical at specified V_{DD}.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Supply Current	I_{DD}			7.3		mA
High Level Input Voltage SEL0, SEL1, AUX0, AUX1	V_{IH}		3.6	4.1	4.5	V
Low Level Input Voltage SEL0, SEL1, AUX0, AUX1	V_{IL}		0.73	0.75	0.8	V
Open Input Voltage SEL0, SEL1, AUX0, AUX1		open		2.3		V
Low Level Input Current, pull-up THERM, MRN	I_{IL}	V=0.4V		74		µA
High Level Input Current, pull-down DTSEL	I_{IH}	V=V_{DD}-0.4V		75		µA
High Level Source Current CHG, DCHG	I_{OH}	V=V_{DD}-0.4V		28		mA
Low Level Sink Current CHG, DCHG	I_{OL}	V=0.4V		25		mA
Low Level Sink Current, indicator PFN, CMN, MMN	I_{OL}	V=0.4V		40		mA
Low Level Sink Current, indicator OTN	I_{OL}	V=0.4V		28		mA
Input Impedance				1.0		MΩ
Analog/Digital Converter Range			0-2.2	0-2.7	0-2.7	V

Table 11: DC Voltage Thresholds

T_{AMB}=25°C

PARAMETER	TYP	UNITS
Minimum Battery Voltage	0.5	V
Thermistor - Cold Temperature	2.4	V
Thermistor - Hot Temperature	0.93	V
Thermal Switch - Open	4.2	V
Thermal Switch - Closed	0.5	V

Table 12: Timing Characteristics

R≈16kΩ, C≈100pF

PARAMETER	SYMBOL	REFERENCE	TYP	UNITS
Clock Frequency			1.0	MHz
Reset Pulse Duration	t_{RESET}	see Figure B	700	ms
Charge Pulse Width	t_{CHG}	see Figure A	1048	ms
Discharge Pulse Width	t_{DCHG}	see Figure A	5.0	ms
Rest Time	t_R	see Figure A	4.0	ms
Data Acquisition Time	t_{DA}	see Figure A	16.4	ms
Cycle Time	t_{CYCLE}	see Figure A	1077	ms
Capacitor Discharge Pulse Width			5.0	ms
Capacitor Discharge Pulse Period			100	ms
Polling Detect Pulse Width			100	ms
Polling Detect Pulse Period			524	ms
Soft Start Initial Pulse Width			200	ms
Soft Start Incremental Pulse Width			7.0	ms
Discharge Mode Pulse Width			400	ms
Discharge Mode Pulse Period			1050	ms
RESET to SEL Dynamic Reprogram Period	t_{RSA}	see Figure B	1160	ms
RESET to AUX Dynamic Reprogram Period	t_{RSA}	see Figure B	1160	ms

Timing Diagrams

Figure A:

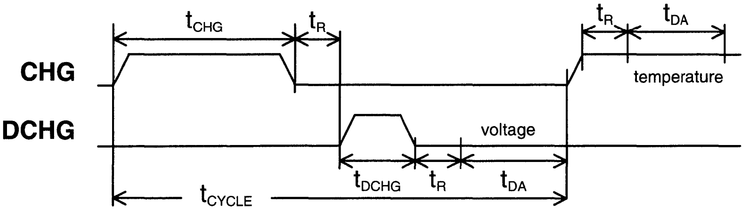
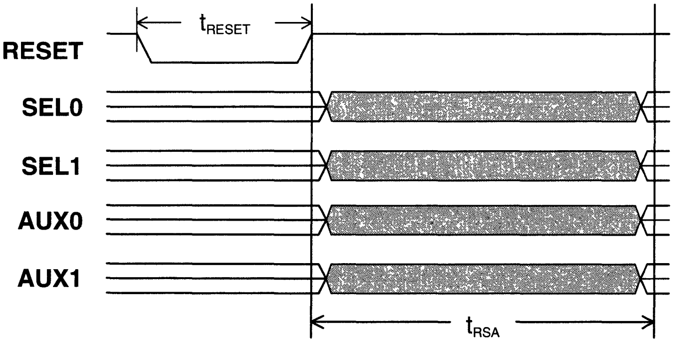


Figure B:



Applications Information

To ensure proper operation of the **ICS1702**, external components must be properly selected. The external current source used must meet several important criteria to ensure optimal performance of the charging system. The charging current should be constant when using voltage slope termination. The current may vary when using temperature slope termination.

VIN and OPREF Divider Resistors

Figure 15 shows a typical application using the **ICS1702**. R1 through R4 must be carefully selected to ensure that battery detection and voltage termination methods operate properly. R1 and R2 are selected to scale the battery voltage down to the voltage of one cell. The following table shows some typical values. Additional information is available in the *Voltage Input* section.

Cells	R1	R2
1	Short	Open
2	2.0k	2.0k
3	2.0k	1.0k
4	3.0k	1.0k
5	12k	3.0k
6	10k	2.0k
7	12k	2.0k
8	9.1k	1.3k

If using voltage slope termination, the current source should prevent ripple voltage from appearing on the battery. The effects of ripple on the battery voltage may interfere with proper operation when using the voltage slope method.

R3 and R4 are used to set the open circuit (no battery) reference voltage on the OPREF pin. The function of this pin is discussed in the *Open Circuit Reference* section.

V_{OPREF}	R3	R4
1.86 V	2.2k	1.3k
1.92 V	2.4k	1.5k
1.97 V	2.0k	1.3k
2.00 V	3.0k	2.0k
2.03 V	2.2k	1.5k
2.10 V	1.8k	1.3k
2.14 V	2.4k	1.8k
2.22 V	3.0k	2.4k

With the batteries removed, the current source must be capable of raising the voltage at the VIN pin above the voltage at the OPREF pin to ensure proper polling. With the batteries installed, the current source overshoot characteristics when turned on and off must not cause the voltage at the VIN pin to exceed the voltage at the OPREF pin. If the voltage at OPREF exceeds the voltage at VIN when a charge pulse is applied or removed, the polling feature will be activated.

PC Board Design Considerations

It is very important that care be taken to minimize noise coupling and ground bounce. In addition, wires and connectors can add significant resistance and inductance to the charge and discharge circuits.

When designing the printed circuit board, make sure ground and power traces are wide and bypass capacitors are used right at the controller. Use separate grounds for the signal, charge and discharge circuits. Separate ground planes on the component side of the PC board are recommended. Be sure to connect these grounds together at the negative lead of the battery only. For the discharge circuit, keep the physical separation between power and return (ground) to a minimum to minimize field radiation effects. This precaution is also applicable to the constant current source, particularly if it is a switch mode type. Keep the **ICS1702** and the constant current source control circuits outside the power and return loop described above. These precautions will prevent high circulating currents and coupled noise from disturbing normal operation.

Selecting the Appropriate Termination Method

In general, the voltage slope termination method works best for equipment where the battery is fast charged with the equipment off or the battery is removed from the equipment for fast charge. The temperature slope and maximum temperature termination methods are for equipment that must remain operative while the battery is fast charged.

• Voltage Slope Termination

The voltage slope termination method used by the **ICS1702** requires a nearly constant current flow into the battery during fast charge. Equipment that draws a known constant current while the battery is charging may use the voltage slope termination method. This constant current draw must be added to the fast charge current. Using the voltage slope termination method for equipment that randomly or periodically requires moderate current from the battery during fast charge needs evaluation. Equipment that randomly or periodically requires high current from the battery during fast charge may cause a voltage inflection that results in termination before full charge. A voltage inflection can occur due to the charge current decreasing or fluctuating as the load changes rather than by the battery reaching full charge. The voltage slope method will terminate charge based on voltage inflections that are characteristic of a fully charged battery.

Charging sources that produce decreasing current as fast charge progresses may also cause a voltage inflection that may result in termination before full charge. For example, if the charge current is supplied through a resistor or if the charging source is a constant current type that has insufficient input voltage, the current will decrease and may cause a termination before full charge. Other current source abnormalities that may cause a voltage inflection that is characteristic of a fully charged battery are inadequate ripple and noise attentuation capability or charge current decreasing due to thermal drift. Charging sources that have any of the above characteristics need evaluation to access their suitability for the application if the use of the voltage slope termination is desired.

When using voltage slope termination, the controller soft start stage, built-in noise filtering, and fast charge timer operate optimally when the constant current source charges the battery at the rate selected. If the actual charge current is significantly less than the rate selected, the conditioning effect of the soft start stage and the controller noise immunity are lessened. Also, the fast charge timer may cause termination based on time duration rather than by the battery reaching full charge due to inadequate charge current.

• Temperature Slope and Maximum Temperature

Temperature slope and/or maximum temperature termination may have to be used for equipment that has high dynamic current demands while operating from the battery during fast charge. Also, users who do not have a well regulated constant current source available may have to use temperature termination. In general, utilizing temperature slope as the primary termination method with maximum temperature termination as a safety back-up feature is the best approach. When using temperature slope termination, the actual current should not be appreciably lower than the selected rate in order that termination of fast charge occurs due to the battery reaching full charge rather than by the timer expiring.

Temperature termination methods require that the thermal sensor be in intimate contact with the battery. A low thermal impedance contact area is required for accurate temperature sensing. The area and quality of the contact surface between the sensor and the battery directly affects the accuracy of temperature sensing. Thermally conductive adhesives may have to be considered in some applications to ensure good thermal transfer from the battery case to the sensor.

The thermal sensor should be placed on the largest surface of the battery for the best accuracy. The size of the battery is also a consideration when using temperature termination. The larger the battery the lower the surface area to volume ratio. Because of this, larger batteries are less capable in dissipating internal heat.

Additional considerations beyond the basics mentioned above may be involved when using temperature slope termination where sudden changes in ambient temperature occur or where forced air cooling is used. For these applications, the surface area of the thermal sensor in contact with the battery compared to the surface area of the thermal sensor in contact with the ambient air may be significant. For example, bead type thermistors are relatively small devices which have far less thermal capacity compared to most batteries. Insulating the surface of the thermistor that is in contact with the ambient air should help minimize heat loss by the thermistor and maintain accuracy.

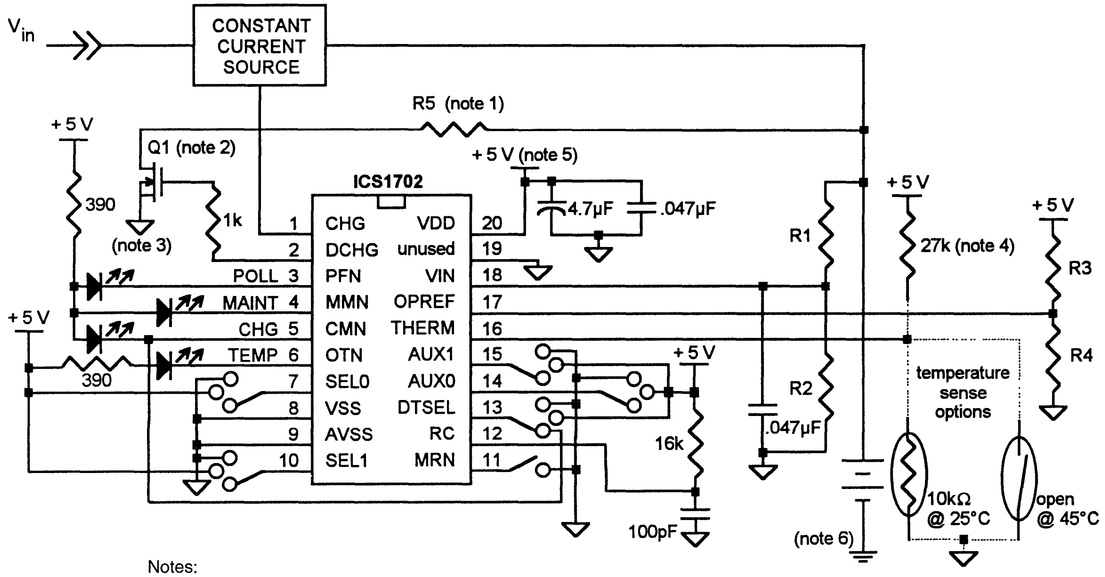
Charging System Status by Indicator

The *Indicator Description List* in Table 3 contains displays that are caused by charging system abnormalities. When the CMN indicator is flashing with no other indicator active, there is voltage present at the battery terminals with the current source off and no battery. Check the current source and ensure that it produces no more than the equivalent of 350mV/cell when turned off with no battery. If the VIN divider resistors were not properly selected, an open circuit voltage that is actually less than the equivalent of 350mV/cell with the charger off and no battery will not divide down this open circuit voltage properly and produce the CMN flash indication. Check the VIN divider and ensure that it properly normalizes the battery voltage to the electrochemical potential of about 1.2V cell. If the CMN flash indication occurs with the battery installed, then the constant current source is producing more than the equivalent of 350mV/cell when off and there is an open connection between the charger terminals and the battery. Check wires, connections, battery terminals, and the battery itself for an open circuit condition.

If the CMN and OTN indicators are active together, this is an indication that the battery temperature has dropped to below 10°C after a fast charge was initiated with the battery temperature normal. If this condition is observed and the battery temperature did not drop after high charge was initiated, check the thermistor circuit mechanically for poor contact and electrically for excessive noise.

If the MMN and CMN indicators are alternately flashing, the likely cause is no battery with the **ICS1702** programmed in the discharge-to-charge auxiliary mode. If the battery is present, check wires, connectors, battery terminals, and the battery itself for an open circuit condition.

If the MMN indicator is flashing with the OTN indicator active, this is an indication that the battery is cold while in either the discharge portion of the discharge-to-charge mode or the discharge only mode. When in the discharge-to-charge mode, if the battery does not warm-up into the normal temperature range after the discharge is complete, the **ICS1702** will enter the maintenance charge stage. When the battery warms-up, the discharge-to-charge mode will repeat.



Notes:

1) Value of R5 determined by discharge current and capacity of battery pack
2) Discharge FET is logic-level compatible in this application
3) DC return of discharge FET must be connected close to negative battery terminal.
4) Resistor is needed only if a thermistor is used Value may change depending on thermistor.
5) Regulated supply
6) Power ground; others are signal ground Connect signal ground to power ground at negative battery terminal only

Figure 15: Functional Diagram

Ordering Information

ICS1702N, ICS1702M, or ICS1702MT

Example:

ICS XXXX M

Package Type
N=DIP (Plastic)
M=SOIC
MT=SOIC Tape and Reel
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS=Standard Device

Integrated
Circuit
Systems, Inc.

ICS1702

Application Note

ICS1702 Linear Regulator Evaluation Board

General Description

The ICS1702 Linear Regulator Evaluation Board allows quick evaluation of the ICS1702 Charge Controller for Nickel-Cadmium and Nickel-Metal Hydride Batteries. The evaluation board provides the designer an opportunity to both test the ICS1702 and a fast charge battery charger. The board is self-contained and can provide a constant current to charge a battery when optional components are installed.

The board includes resistors that are user-installed to customize operation for the desired charge rate, discharge pulse current, and number of cells in the battery pack. The board has a 5V regulator that provides power to the ICS1702 and the LED display. The board also has a breadboarding area consisting of a matrix of holes for user added components.

Before using the **ICS1702 Linear Regulator Evaluation Board**, ICS recommends the user review the ICS1702 data sheet to become familiar with the operation of the controller. This data sheet should be included with the board; if not, please contact your local representative.

The **ICS1702EB** can be purchased two ways: **ICS1702EB** or **ICS1702EB/VR**. The difference between these boards is a constant current linear supply as shown in the board schematic. The **ICS1702EB** has an area on the board reserved for these components. The **ICS1702EB/VR** contains a kit which includes an LM317 and associated parts needed to build a constant current supply of up to 1.5A.

Customizing the Board for your Application

Refer to the evaluation board schematic diagram. The ICS1702 requires that the battery voltage is normalized to the voltage of one cell, or about 1.2V. To do this, resistors must be installed in the locations marked R6 and R8. The appropriate values can be selected from Table 1. An assortment of resistors is provided with the board.

Table 1

Cells	R6	R8
1	Open	Short
2	2.0k	2.0k
3	1.0k	2.0k
4	1.0k	3.0k
5	3.0k	12k
6	2.0k	10k
7	2.0k	12k
8	1.3k	9.1k

If the evaluation board is used with battery packs containing more than eight cells, the resistors can be determined by counting the number of cells to be charged in series. Then choose either R6 or R8 and solve for the other resistor using:

$$R8 = R6 \times (\text{\# of cells -1}) \quad \text{or} \quad R6 = \frac{R8}{(\text{\# of cells - 1})}$$

Current flow through the divider should be 0.4mA or greater for noise immunity.

R7 sets the open circuit (no battery) reference voltage at the OPREF pin voltage. The purpose of this voltage reference is to detect the removal of the battery from the charging system. The voltage at this pin is compared to the voltage at the VIN pin when the current source is turned on. If the voltage at VIN is greater than the voltage at OPREF, the ICS1702 assumes the battery has been removed and the ICS1702 enters the polling detect mode. For proper operation, the voltage at OPREF must be set between the (divided down) open circuit voltage produced by the current source and the maximum normalized battery. As a guide, set the voltage at OPREF (TP1) to be 200mV to 300mV higher than the maximum normalized battery voltage. For most batteries, the maximum normalized battery voltage at full charge is 1.7 to 1.8V, so OPREF (TP1) should be set at about 2V.

When power is applied to the board, the controller will start a charge sequence unless a logic low is applied to the RESET terminal. When RESET is removed by a logic high or open, a charge sequence will begin.

ICS1702 Linear Regulator Evaluation Board

The board provides several low value resistors that may be used to set the amplitude of the discharge pulse. The resistors can be installed in any or all of the locations labeled R1, R2, or R3. The resistor value is calculated by setting the amplitude of the discharge pulse. The discharge pulse amplitude is typically 2.5 times the charge current based on 1.4V/cell. The required power rating of the resistor is highest when the Discharge-to-Charge and Discharge-Only Auxiliary Modes are used. See the ICS1702 data sheet for additional information. The resistor locations R1, R2, and R3 are connected in series. The unused locations must have a jumper to complete the circuit. Not using the discharge pulse feature will not affect the performance of the ICS1702.

The ICS1702 is capable of operating at nine different charge rates between 4C (15 minutes) and C/4 (four hours). The charge rate is selected by installing jumpers in the appropriate locations. Table 2 shows the proper settings to use for the desired charge rate.

Table 2: Charge Rate List

Charge Rate	Jumper S0	Jumper S1	Topping Charge Pulse Rate	Maintenance Charge Pulse Rate	Fast Charge Timer Duration (after reset)
4C (15 min)	1 & 2	1 & 2	one every 40 sec	one every 160 sec	21 min
2C (30 min)	1 & 2	2 & 3	one every 20 sec	one every 80 sec	39 min
1.3C (45 min)	1 & 2	None	one every 13 sec	one every 53 sec	57 min
1C (60 min)	2 & 3	1 & 2	one every 10 sec	one every 40 sec	75 min
C/1.5 (90 min)	2 & 3	None	one every 7 sec	one every 27 sec	110 min
C/2 (120 min)	2 & 3	2 & 3	one every 5 sec	one every 20 sec	144 min
C/2.5 (150 min)	None	1 & 2	one every 4 sec	one every 16 sec	212 min
C/3 (180 min)	None	None	one every 3 sec	one every 13 sec	244 min
C/4 (240 min)	None	2 & 3	one every 2 sec	one every 10 sec	275 min

The **ICS1702** has several auxiliary modes available. Table 3 shows the jumper configurations for the auxiliary modes.

Table 3: Mode Select List

Auxiliary Mode	Jumper AUX0	Jumper AUX1	Mode Operation
Direct Maintenance	2 & 3	1 & 2	Indefinite C/40 maintenance mode
Charging System Test	2 & 3	2 & 3	Charging system test for embedded applications
Ten Hour Timer	1 & 2	1 & 2	Limits total charge including the maintenance charge to 10 hours
Discharge-to-Charge	1 & 2	2 & 3	Battery discharge to 1V/cell followed by the selected charge mode
Condition	1 & 2	None	Timed C/10 topping charge followed by C/40 maintenance charge
Fast Charge	None	None	Default
Discharge-Only	None	2 & 3	Battery discharge to 1V/cell

The ICS1702 has the capability to use either temperature slope termination, voltage slope termination or both methods simultaneously. Table 4 shows the termination method and the jumper settings. Refer to the ICS1702 data sheet for more information on charge termination methods.

Table 4: Termination Select List

Termination Method	Jumper DTSEL
Voltage slope termination only	None
Voltage slope and temperature slope termination	1 & 2
Temperature slope termination only	2 & 3

Power Requirements

The evaluation board uses a regulator to provide +5 volts for the controller. The regulator allows operation from a DC supply of 8 to 32 volts when the supply is connected to the +V terminal. The board may also be operated from an external 5 volt supply by removing the regulator (U2), wiring a jumper between regulator pins 1 and 3, and by connecting 5 volts directly to the +5V terminal.

Connections To External Circuitry

A normally closed thermal switch or a thermistor should be connected to the TS terminal. If a thermal protection device is not used, the TS terminal must be grounded.

Connect the battery between the +BAT and GND terminals. If using an external current source, connect the charging current source and its return between the +CUR and GND terminals. If the on board current source is used, no connection to the +CUR terminal is required.

Two charge signals are provided to control external charging circuitry. CHG is high when the charging current is on. The other signal $\overline{\text{CHG}}$ is low when the charging current is on.

The charging circuitry should provide a current at an amplitude that is equal to the product of the battery capacity and the desired charge rate. For example, to charge a 1.2 ampere hour battery in 30 minutes, the current required would be 2.4 amps or 2C where ‘C’ is the battery capacity.

It is important to note that the ICS1702 does not control the current flowing into the battery in any way other than turning it on and off. The charging current should be constant when using voltage slope termination. The current may vary when using temperature slope termination.

Current Source (VR option)

The **ICS1702EB/VR** contains an LM317 regulator. The LM317 is configured as a constant current source. The amplitude of the current is determined by the value of R15 and the setting of R16. As an example, with a 2 ohm resistor for R15, the current can be adjusted with R16 from 0.625A to 1.25A. The LM317 will regulate a voltage difference of 1.25 volts between the OUT and ADJ pins.

Operation

Before applying power to the board, ensure that the board is properly initialized.

- Set the AUX0 and AUX1 jumpers for the desired mode of operation.
- Set the S0 and S1 jumpers for the correct charge rate.
- If needed, set the DTSEL jumper for the desired termination method.
- Check to make sure the divider resistors R6 and R8 are of the correct value to normalize the battery pack voltage to one cell.
- If applicable, choose a value for R15 (see the section on Current Source).
- If applicable, choose resistors R1, R2 and R3 to obtain the required discharge current.

After applying power to the board, set the following:

- Adjust the potentiometer R7 for the desired open circuit reference voltage at the OPREF pin.
- If applicable, set the LM317 charging current by adjusting the potentiometer R16.

Push and hold the reset switch SW1 for at least 700ms. All LEDs should turn off while the switch is depressed. If fast charge is selected, the green CHG LED will light. The LED will remain lit until full charge is detected by the ICS1702. At that moment, the CHG LED will turn off and the MAINT LED will light, indicating that the topping charge stage has begun. The MAINT LED will remain on until a reset is issued either by interrupting the power, removing the batteries or depressing the reset switch SW1.

If the ten hour timer mode is selected, the LED sequence is the same as the fast charge sequence explained above. After a maximum of 10 hours has elapsed (from the time the ICS1702 was reset), the controller will shut down and the MAINT LED will turn off.

If either direct maintenance or the condition mode is selected, the MAINT LED will turn on. The LED will remain on until a reset is issued either by interrupting the power, removing the batteries or depressing the reset switch SW1.

If the discharge-only mode is selected, the MAINT LED will flash at a one second rate until the battery has been discharged. When the battery is discharged, the controller will shut down and the MAINT LED will turn off.

If the discharge-to-charge mode is selected, the MAINT LED will flash at a one second rate until the battery has been discharged. When the battery is discharged, the appropriate charge indicator will turn on. See the data sheet for more detailed information on this auxiliary mode of operation.

Polling for a Battery

Upon power-up or after a reset is issued, any excess charge from filter capacitors at the +BAT and +CUR terminals is removed with a series of discharge pulses. After the discharge pulse series is complete, the voltage at VIN must be greater than 0.5V when a battery is present. If the voltage at the pin is less than 0.5V, the ICS1702 assumes no battery is attached, and the polling detect mode is initiated.

The ICS1702 then applies a 100ms charge pulse. During the pulse, the ICS1702 monitors the VIN pin to determine if the divided down terminal voltage is above OPREF. If the battery is present, the voltage will be clamped below the reference on OPREF when the current pulse is applied. If a battery is not present, the voltage at VIN will rise above the reference at OPREF. The POLL LED lights immediately.

Charge pulses will repeat at one second intervals until the battery is reinstalled. The POLL LED is active as long as the ICS1702 is in the polling detect mode. Once a battery is installed, the ICS1702 will turn off the POLL LED and enter the soft start stage. The ICS1702 will automatically re-enter the polling detect mode if the battery is removed during the fast charge, topping charge, or maintenance charge stages. Any open circuit in the current path to the battery will initiate the polling detect mode.

When in the topping charge or maintenance charge stages, a charge pulse may not occur for several seconds. During the period between charge pulses, the voltage at VIN should be greater than 0.5V if a battery is attached. If the voltage at VIN is less than 0.5V, the ICS1702 assumes the battery has been removed, and the polling detect mode is initiated.

Out-of-Temperature Range

The TEMP LED activates if the battery is either too hot or too cold to fast charge. If a thermistor is used, the ICS1702 employs internal voltage references to determine if a battery is hot or cold. *Note: Remove R9 and replace with a jumper when using a thermistor.* A 10kΩ @ 25°C thermistor with an external pull-up resistor is typically used. See the ICS1702 data sheet for additional information.

If a thermal switch is used, choose a switch that opens at 45°C or lower. If a thermal protection device is not used, the TS terminal must be grounded.

ICS strongly recommends the use of a thermal safety device in the battery pack. One source of thermal switches is Portage Electric Products, Inc., in North Canton, Ohio; (216) 499-2727. A source of thermistors is Semetic USA (Ishizuka Electronics Corp.), Babylon, NY; (516) 587-4086.

Design Considerations

When designing external current source circuitry for use with the ICS1702, there are several important considerations to make before starting the design and the PC board layout.

For fast charge rates (1C through 4C), consideration has to be given to the use of a pulse-width modulated switch mode current source in order to reduce size and power dissipation. Switch mode current sources can provide the ability to charge battery packs that require voltages higher than the primary supply. For instance, to charge a 24 volt battery from a 12 volt vehicle battery, a switch mode boost converter could be used.

In general, linear chargers are less complex and more cost effective, but less efficient than switch mode chargers. For lower charge rates (C/1.5 through C/4), consideration should be given to using a linear charger unless the size and ability to dissipate heat are not available.

It is very important that care be taken to minimize noise coupling and ground bounce. In addition, wires and connectors can add significant resistance and inductance to the charge and discharge circuits.

When designing the printed circuit board, make sure ground and power traces are wide and bypass capacitors are used right at the controller pins. Use separate grounds for the signal, charge, and discharge circuits. Separate ground planes on the component side of the PC board are recommended. Be sure to connect these grounds together at the negative lead of the battery only.

For the discharge circuit, keep the physical separation between power and return (ground) to a minimum to minimize field radiation effects. This precaution is also applicable to the constant current source, particularly if it is a switch mode type. Keep the ICS1702 and the constant current source control circuits outside the power and return loops described above. These precautions prevent high circulating currents and coupled noise from disturbing proper operation.

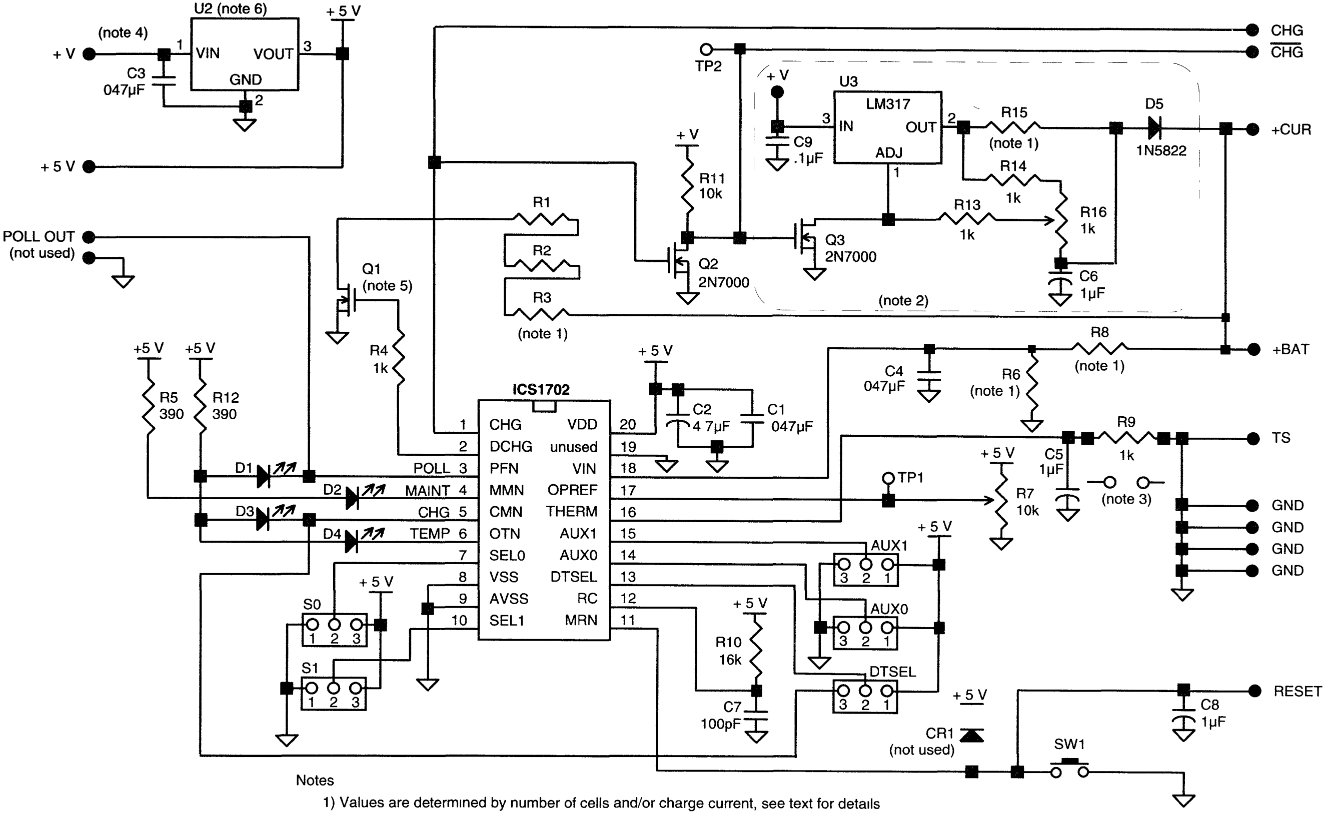
Integrated Circuit Systems wants to help create a successful battery charging solution using the ICS1702. If you need technical advice or applications information, call the Power Management Products Applications department at (610) 630-5300.

Ordering Information

ICS1702EB /VR

Ordering Option
blank=populated board
/VR=populated board with linear regulator kit

Device Type
ICS1702 Linear Regulator Evaluation Board



Notes

1) Values are determined by number of cells and/or charge current, see text for details
2) Components within dotted lines can be supplied for user-installation when ordered, see ordering information
3) Resistor R9 must be removed and replaced with a jumper when using a thermistor Use of a thermistor requires an external pull-up resistor
4) 8 Vdc minimum input
5) Logic level compatible FET
6) LM340, AN7805 or equivalent

ICS1702 Evaluation Board

QuickSaver® Charge Controller for Nickel-Cadmium and Nickel-Metal Hydride Batteries

General Description

The **ICS1712** is a CMOS device designed for the intelligent charge control of either nickel-cadmium (NiCd) or nickel-metal hydride (NiMH) batteries. The controller uses a pulsed-current charging technique together with voltage slope and/or temperature slope termination. The **ICS1712** employs a four stage charge sequence that provides a complete recharge without overcharging. The controller has four user-selectable charge rates available for customized charging systems.

The **ICS1712** monitors for the presence of a battery and begins charging if a battery is installed within the first 10 seconds after a reset. Voltage and temperature are measured to ensure a battery is within fast charge conditions before charge is initiated.

Applications

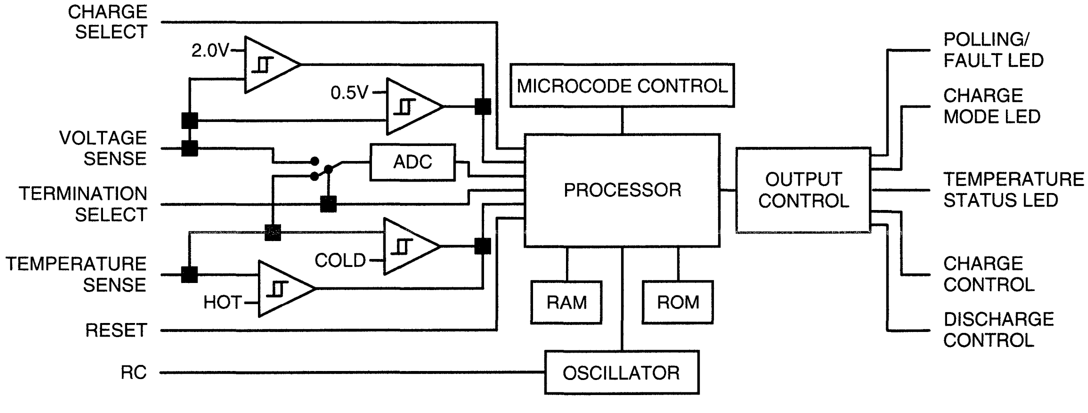
Battery charging systems for:

- Portable consumer electronics
- Power tools
- Audio/video equipment
- Communications equipment

Features

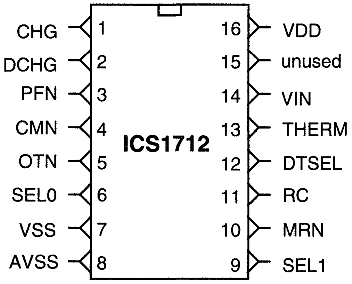
- Multiple charge termination methods include:
  - Voltage slope
  - Temperature slope
  - Maximum temperature
  - Charge timer
- Four stage charge sequence:
  - Soft start charge
  - Fast charge
  - Topping charge
  - Maintenance charge
- Reverse-pulse charging available in all charge stages
- Four programmable charge rates between 15 minutes (4C) and two hours (C/2)
- Out-of-temperature range detection
  - Hot battery: charger shutdown
  - Cold battery: low current charge
- Ten second polling mode for battery detection
- Battery fault with shutdown protection

Block Diagram



QuickSaver is a registered trademark of Integrated Circuit Systems, Inc

Pin Configuration



16-Pin DIP or SOIC
K-4, K-6

Pin Definitions

Pin Number	Pin Name	Type	Definition
1	CHG	OUT	Active high TTL compatible signal used to turn on an external current source to provide current to charge the battery.
2	DCHG	OUT	Active high TTL compatible signal available to turn on a discharge circuit.
3	PFN	OUT	Polling fault indicator. An active low turns on an external indicator to show the controller is either polling for the presence of the battery or has determined the battery has been removed.
4	CMN	OUT	Charge mode indicator. A continuous low shows the controller is in a soft start or fast charge. The indicator flashes during the topping and maintenance charges.
5	OTN	OUT	Out-of-temperature range indicator. An active low turns on an external indicator showing the battery is out of the normal fast charge temperature range.
6	SEL0	IN	Input used with the SEL1 pin to program the device for the desired charge rate.
7	VSS		Ground.
8	AVSS		Ground.
9	SEL1	IN	Input used with the SEL0 pin to program the device for the desired charge rate.
10	MRN	IN	Master reset signal. A logic low pulse greater than 700 ms initiates a device reset.
11	RC	IN	An external resistor and capacitor sets the frequency of the internal clock.
12	DTSEL	IN	Selects temperature slope and/or voltage slope termination.
13	THERM	IN	Thermistor or thermal switch input for temperature sensing.
14	VIN	IN	Battery voltage normalized to one cell with an external resistor divider.
15	unused		Ground.
16	VDD		Device supply =+5.0 VDC

Note: Pins 6, 9, 10 and 13 have an internal pull-up.
Pin 12 has an internal pull-down

Controller Operation

Charging Stages

The charging sequence consists of four stages. The application of current is shown graphically in Figure 1. The soft start stage gradually increases current levels up to the user selected fast charge rate during the first two minutes. The soft start stage is followed by the fast charge stage, which continues until termination. After termination, a two hour C/10 topping charge is applied. The topping charge is followed by a C/40 maintenance charge.

Soft Start Charge

Some batteries may exhibit an unusual high impedance condition while accepting the initial charging current, as shown in Figure 2. Unless dealt with, this high impedance condition can cause a voltage peak at the beginning of the charge cycle that would be misinterpreted as a fully charged battery by the voltage termination methods.

The soft start charge eases batteries into the fast charge stage by gradually increasing the current to the selected fast charge rate. The gradual increase in current alleviates the voltage peak. During this stage, only positive current pulses are applied to the battery. The duty cycle of the applied current is increased to the selected fast charge rate, as shown in Figure 3, by extending the current pulse on every cycle until the pulse is about one second in duration. The initial current pulse is approximately 200ms. The CMN indicator is activated continuously during this stage

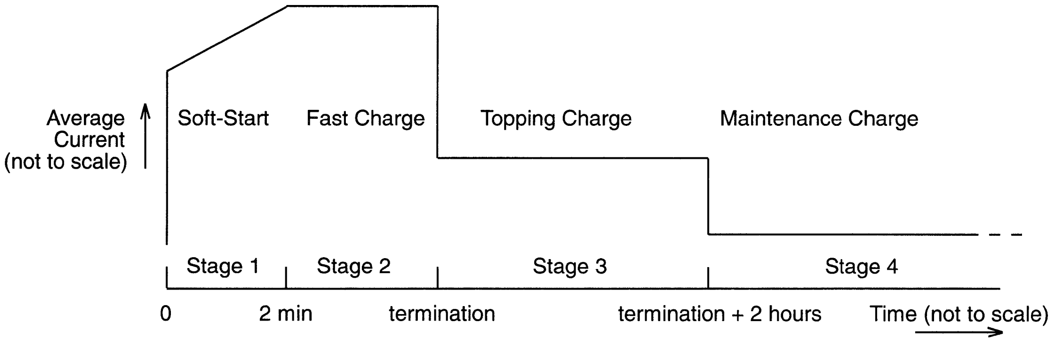


Figure 1: Graphical representation of average current levels during the four charging stages

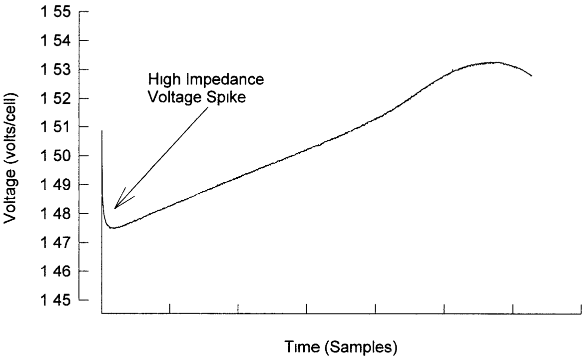


Figure 2: High impedance voltage spike at the beginning of charge

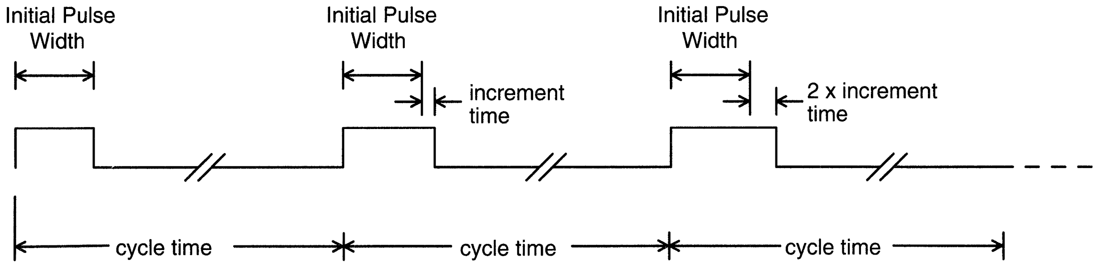


Figure 3: Cycle-to-cycle increase of the soft-start current pulse widths

Fast Charge

In the second stage, the **ICS1712** applies the charging current in a series of charge and discharge pulses. The technique consists of a positive current charging pulse followed by a high current, short duration discharge pulse. The cycle, shown with charge, discharge, rest and data acquisition periods in Figure 4, repeats every second until the batteries are fully charged.

The amplitude of the current pulse is determined by system parameters such as the current capability of the charging system, the desired charge rate, the cell capacity and the ability of that cell to accept the charge current. The **ICS1712** can be set for four user-selectable fast charge rates from 15 minutes (4C) to two hours (C/2). Charge pulses occur approximately every second. The CMN indicator is activated continuously during this stage.

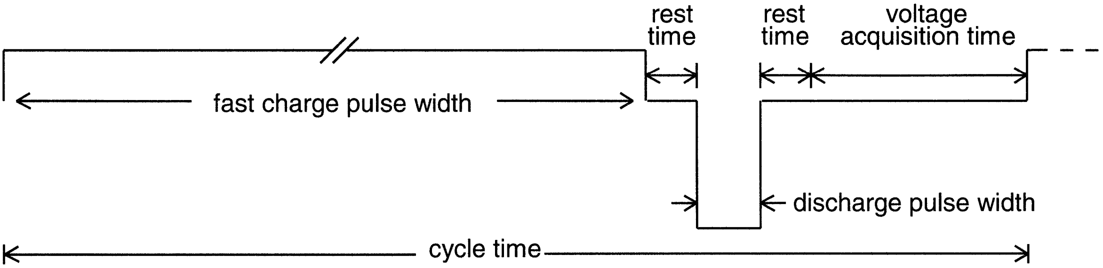


Figure 4: Charge cycle showing charge and discharge current pulses

The discharge current pulse amplitude is typically set to about 2.5 times the amplitude of the charging current based on 1.4V/cell. For example, if the charge current is 4 amps, then the discharge current is set at about 10 amps. The energy removed during the discharge pulse is a fixed ratio to the positive charge rate. The amplitude of the discharge pulse does not affect the operation of the part as described in this section.

A voltage acquisition window immediately follows a brief rest time after the discharge pulse. No charge is applied during the rest time or during the acquisition window to allow the cell chemistry to settle. Since no current is flowing, the measured cell voltage is not obscured by any internal or external IR drops or distortions caused by excess plate surface charge. The **ICS1712** makes one continuous reading of the no-load battery voltage during the entire acquisition window. The voltage that is measured during this window contains less noise and is a more accurate representation of the true state of charge of the battery.

Topping Charge

The third stage is a topping charge that applies current at a rate low enough to prevent cell heating but high enough to ensure a full charge.

The topping charge applies a C/10 charging current for two hours. The current consists of the same pulse technique used during the fast charge stage; however, the duty cycle of the pulse sequence has been extended as shown in Figure 5. Extending the time between charge pulses allows the same charging current used in the fast charge stage so that no changes to the current source are necessary. For example, the same charge pulse that occurs every second at a 2C fast charge rate will occur every 20 seconds for a topping charge rate of C/10. The CMN indicator flashes at a one second rate during this stage.

Maintenance Charge

The maintenance charge is intended to offset the natural self-discharge of NiCd or NiMH batteries by keeping the cells primed at peak charge. After the topping charge ends, the **ICS1712** begins this charge stage by extending the duty cycle of the applied current pulses to a C/40 rate. The maintenance charge will last for as long as the battery voltage is greater than 0.5V at the VIN pin. The CMN indicator flashes at a one second rate during this stage.

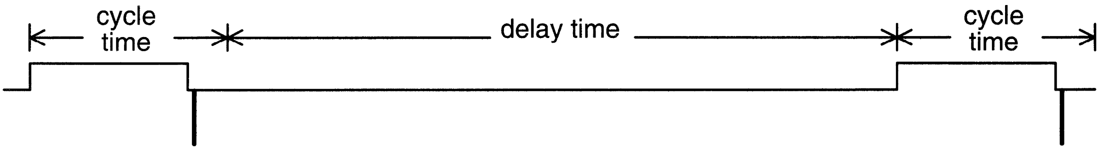


Figure 5: Representative timing diagram for topping and maintenance charge

Charge Termination Methods

Several charge termination schemes, including voltage slope, temperature slope, maximum temperature and two overall charge timers are available. The voltage slope and negative voltage slope methods may be used with or without the temperature slope and the maximum temperature method. Maximum temperature and the fast charge timer are available as backup methods.

Voltage Slope Termination

The most distinctive point on the voltage curve of a charging battery in response to a constant current is the voltage peak that occurs as the cell approaches full charge. By mathematically calculating the first derivative of the voltage, a second curve can be generated showing the change in voltage with respect to time as shown in Figure 6. The slope will reach a maximum just before the actual peak in the cell voltage. Using the voltage slope data, the **ICS1712** calculates the point of full charge and accurately terminates the applied current as the battery reaches that point. The actual termination point depends on the charging characteristics of the particular battery.

Cells that are not thoroughly conditioned or possess an unusual cell construction may not have a normal voltage profile. The **ICS1712** uses an alternate method of charge termination based on a slight decrease in the voltage slope to stop charge to cells whose voltage profile is very shallow. This method looks for a flattening of the voltage slope which may indicate a shallow peak in the voltage profile.The zero slope point occurs slightly beyond the peak voltage and is shown on the voltage curve graph.

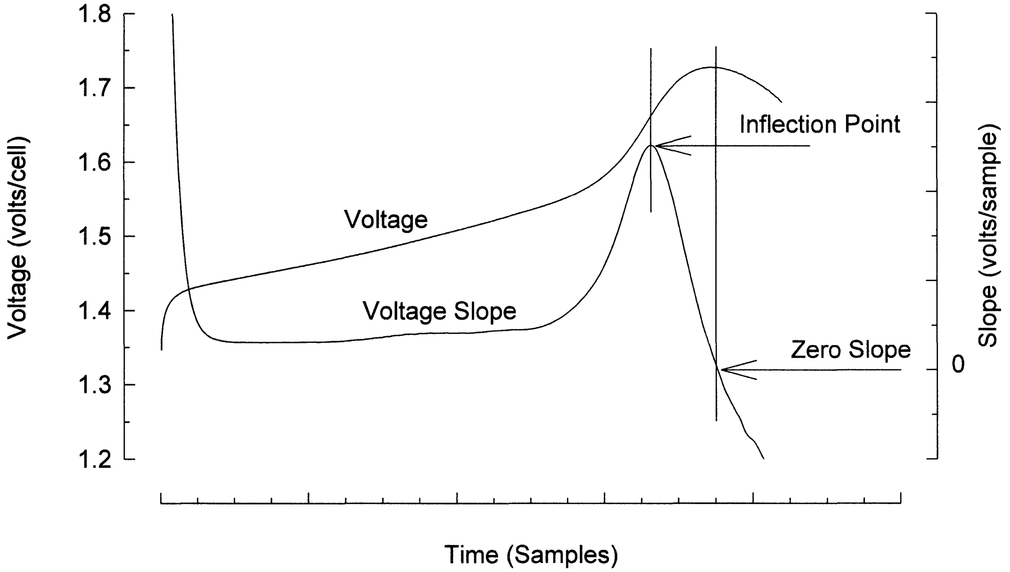


Figure 6: Voltage and slope curves showing inflection and zero slope points

Temperature Slope Termination

Temperature slope termination is based on the battery producing an accelerated rate of heating as the amount of readily chargeable material dimishes at full charge. An increase in battery (cell) heating due to the charging reaction will occur at a much faster rate than a change due to a warming ambient temperature. Note the effect of 0.5°C fluctuations in ambient temperatures resulting in slight variations in the temperature slope as shown in Figure 7. However, the increase in cell temperature near the end of charge causes a much larger change in the temperature slope that can be easily detected and used as a trigger for fast charge termination.

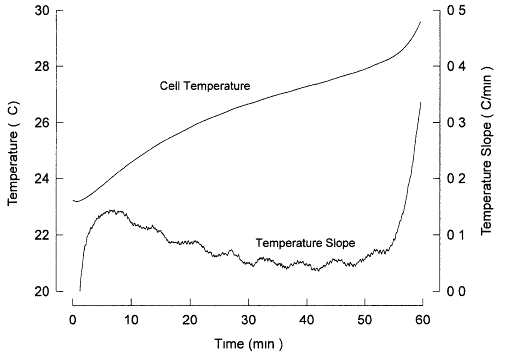


Figure 7: Cell temperature and temperature slope

The rate of change in cell temperature can be determined by measuring the change in voltage across a negative temperature coefficient thermistor as shown in Figure 8. The resistance of an NTC thermistor changes in proportion in the change in temperature of the thermistor. The **ICS1712** measures the decreasing resistance as a drop in voltage and calculates the thermistor voltage slope, shown in Figure 8. The controller terminates fast charge based on the selected charge rate and the calculated slope.

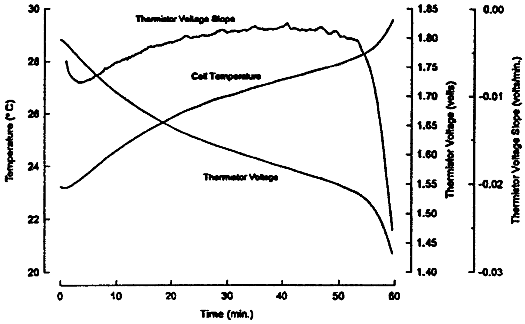


Figure 8: Cell temperature and thermistor voltage slope

Table 1 shows the decrease in thermistor voltage the last minute before full charge required by the **ICS1712** at various charge rates. The thermistor voltage slope should exceed the listed value to ensure charge termination. Note that changes in thermistor location, cell size or large ambient temperature fluctuations can affect the slope to some degree. Refer to the *Applications Information* section and *Temperature Slope and Maximum Temperature* section for more information on thermistor mounting.

Table 1: Slope vs. Charge Rate

Charge Rate	Thermistor Voltage Slope (-V/min.)
>C/2	0.040
C/2	0.028

To determine the required thermistor characteristics for proper temperature slope termination, the battery temperature rise must be known or determined for the last minute prior to full charge.

Maximum temperature termination is also enabled when temperature slope termination is used. Care must be taken to keep voltage levels at the THERM pin within the fast charge range (between 2.4V and 0.93V), as shown in Figure 9.

Maximum Temperature Termination

Maximum temperature can be sensed using either a NTC thermistor or a thermal switch. Maximum temperature termination can also be bypassed if desired, although it is strongly recommended that some form of temperature termination be used.

If an NTC thermistor is used, an internal voltage threshold determines when the battery is too hot to charge. As temperature increases, the voltage across the thermistor will drop. This voltage is continually compared to the internal voltage threshold. If the thermistor voltage drops below the internal threshold, the OTN indicator is activated and the controller shuts down. The controller must be reset once the hot battery fault condition has cleared to restart the charge sequence.

If a thermal switch is used, a 45°C open circuit switch is recommended. When the thermal switch opens, an internal pull-up at the THERM pin results in a logic high which shuts down the controller and activates the OTN indicator. The controller must be reset once the hot battery fault condition has cleared to restart the charge sequence.

Maximum temperature termination can be disabled by grounding the THERM pin. See the section on *Temperature Sensing* for more information.

Fast Charge Timer Termination

The controller uses a timer to limit the fast charge duration. These times are pre-programmed, and are automatically adjusted in time duration according to the charge rate selected. Fast charge timer termination is best suited as a safety backup feature to limit the duration of the fast charge stage. The fast charge timer is always enabled and cannot be disabled. See Table 3 in the section *Charge Rate Selection* for more information.

Battery Polling

Upon power-up or after a reset is issued, any excess charge from filter capacitors at the charging system terminals is removed with a series of discharge pulses. After the discharge pulse series is complete, the voltage at VIN must be greater than 0.5V when a battery is present. If the voltage at VIN is less than 0.5V, the **ICS1712** assumes no battery is attached and initiates a polling sequence.

The **ICS1712** then applies a 100ms charge pulse. During the pulse, the **ICS1712** monitors the VIN pin to determine if the divided down terminal voltage is greater than the internal 2.0V reference. If the battery is present, the voltage is clamped below the 2.0V reference when the current pulse is applied and the fast charge stage begins immediately. If a battery is not present, the voltage at VIN rises above the 2.0V reference and the PFN fault indicator is activated.

The charge pulses repeat for 10 seconds. If the battery is installed within 10 seconds, the **ICS1712** will turn off the PFN fault indicator and enter the soft start stage. If the battery is not installed within 10 seconds, the PFN fault indicator remains active and the **ICS1712** shuts down. A reset must be issued to restart the controller after installing the battery.

Battery Fault Detection

The **ICS1712** will turn on the PFN fault indicator and shut down if the battery is removed or if an open circuit occurs in the current path anytime after fast charge has been initiated. When in the topping charge or maintenance charge stages, a charge pulse may not occur for several seconds. During the period between charge pulses, the voltage at VIN should be greater than 0.5V if a battery is attached. If the voltage at VIN is less than 0.5V, the **ICS1712** assumes the battery has been removed, a fault condition is indicated by the PFN fault indicator, and the controller shuts down.

Cold Battery Charging

Cold battery charging is activated if a voltage at the THERM pin is in the cold battery voltage range, as shown in Figure 7. The **ICS1712** checks for a cold battery before initiating fast charge. If a cold battery is present before fast charging begins, the **ICS1712** begins a two hour C/10 topping charge (the pulsed duty cycle is based on the selected charge rate). If the battery is still cold after the two hour topping charge is complete, the **ICS1712** begins a C/40 maintenance charge. The maintenance charge will continue for as long as the battery remains cold. The thermistor voltage at the THERM pin is checked every second to see if the battery has warmed up. If so, the **ICS1712** stops the topping charge or maintenance charge and begins a fast charge at a rate selected by the SEL0 and SEL1 inputs. See the section on *Temperature Sensing* for more information.

The CMN will flash at a one second rate, and the OTN indicator will be active, indicating that a low current charge is being applied to a battery that is outside the specified temperature range for fast charging.

Pin Descriptions

The **ICS1712** requires some external components to control the clock rate, sense temperature and provide an indicator display. The controller must be interfaced to an external power source that will provide the current required to charge a battery pack and, if desired, a circuit that will sink discharge current.

Output Logic Signals: CHG, DCHG Pins

The CHG and DCHG pins are active high, TTL compatible outputs. In addition to being TTL compatible, the CMOS outputs are capable of sourcing current which adds flexibility when interfacing to other circuitry. A logic high on the CHG pin indicates that the charging current supply should be activated. If applicable, a logic high on the DCHG pin indicates that the discharge circuit should be activated.

Care must be taken to control wiring resistance and inductance. The load resistor must be capable of handling this short duration high-amplitude pulse.

Indicators: CMN, PFN, OTN Pins

The controller has three outputs for driving external indicators. These pins are active low. The three indicator outputs have open drains and are designed to be used with LEDs. Each output can sink over 20mA which requires the use of an external current limiting resistor. The three indicator signals denote fast charge stage, topping and maintenance stages, and the polling detect or battery fault and out-of-temperature range modes as shown in Table 2.

The charge mode (CMN) indicator is activated continuously during the soft start and fast charge stages. The CMN indicator flashes at a one second rate when the **ICS1712** is applying a topping or maintenance charge.

The polling fault (PFN) indicator is on when the **ICS1712** polls for a battery for the first 10 seconds. The controller applies periodic charge pulses to detect the presence of a battery. The indicator is a warning that these charge pulses are appearing at the charging system terminals at regular intervals. When a battery is detected, the indicator is turned off. The indicator is also active if the battery is removed from the system, warning that a fault has occured.

The out-of-temperature range (OTN) indicator is active whenever the voltage at the temperature sense (THERM) input enters a range that indicates that the attached battery is too hot to charge. The OTN indicator is also activated with the CMN indicator if the controller is initialized with the battery in the cold battery charge region.

Table 2: Indicator Description List

PFN	CMN	OTN	Description
on			Polling mode or battery fault
	flash		Maintenance and topping charge
	on		Fast charge
		on	Hot battery shutdown
	flash	on	Cold battery charge
	on	on	see Applications Information
on	one flash		see Applications Information

Charge Rate Selection: SEL0, SEL1 Pins

The SEL0 and SEL1 inputs must be programmed by the user to inform the **ICS1712** of the desired charge rate. When a low level is required, the pin must be grounded. When a high level is required, no connection is required since each pin has an internal 75kΩ pull-up to V_{DD}. The voltage ranges for low (L) and high (H) are listed in Table 8, *DC Characteristics*. To program the SEL0 and SEL1 inputs, refer to the *Charge Rate List* in Table 3.

The **ICS1712** does not control the current flowing into the battery in any way other than turning it on and off. The required current for the selected charge rate must be provided by the user's power source. The external charging circuitry should provide current at the selected charge rate. For example, to charge a 1.2 ampere hour battery in 30 minutes (2C), approximately 2.4 amperes of current is required.

Table 3: Charge Rate List

SEL0	SEL1	Charge Rate	Topping Charge Pulse Rate	Maintenance Charge Pulse Rate	Fast Charge Timer Duration (after reset)
L	L	4C (15 min)	one every 40 sec	one every 160 sec	30 min
L	H	2C (30 min)	one every 20 sec	one every 80 sec	60 min
H	L	1C (60 min)	one every 10 sec	one every 40 sec	90 min
H	H	C/2 (120 min)	one every 5 sec	one every 20 sec	210 min

See the section on *Controller Operation* for additional information on the topping charge and maintenance charge. See the section on *Charge Termination Methods* for additional information on the charge timer.

Master Reset: MRN Pin

The MRN pin is provided to re-program the controller for a new mode or charging sequence. This pin has an internal pull-up of about 75kΩ. A logic low on the MRN pin must be present for more than 700ms for a reset to occur. As long as the pin is low, the controller is held in a reset condition. A master reset is required to clear a temperature fault condition, clear the charging system test, reset the ten hour timer or change charge rates or auxiliary modes. Upon power-up, the controller automatically resets itself.

Clock Input: RC Pin

The RC pin is used to set the frequency of the internal clock when an external 1 MHz clock is not available. An external resistor must be connected between this pin and V_{DD}. An external capacitor must be connected between this pin and ground. The frequency of the internal clock will be about 1 MHz with a 16kΩ resistor and a 100pF capacitor. All time durations noted in this document are based on a 1 MHz clock. Operating the clock at a lower frequency will proportionally change all time durations. Operating the clock at a frequency significantly lower than 1 MHz, without adjusting the charge current accordingly, will lessen the effectiveness of the fast charge timer and lower the accuracy of the controller. Operating the clock at a frequency greater than 1 MHz will also change all time durations and, without adjusting the charge current accordingly, may cause termination to occur due to the fast charge timer expiring rather than by the battery reaching full charge.

The clock may be driven by a 1 MHz external 0 to 5V pulse provided the duty cycle is between 10% and 60%. The clock input impedance is about 1kΩ.

Temperature Sensing: THERM Pin

The THERM pin is provided for hot and cold battery detection and for temperature slope termination of fast charge when used in conjunction with an NTC thermistor. The THERM pin also provides for hot battery and maximum temperature termination when used in conjunction with a normally closed thermal switch. Several internal voltage thresholds are used by the controller depending on whether a thermistor or a thermal switch is used. Figure 9 shows the internal thresholds over laid on a typical thermistor curve.

- Using an NTC thermistor for hot and cold battery detection:

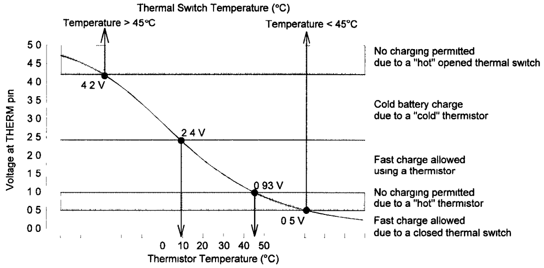


Figure 9: Voltage levels for temperature sensing with a thermistor or thermal switch

The THERM pin requires some thought if a thermistor is going to be used for hot and cold battery detection. The example below works for a typical 10kΩ @ 25°C NTC thermistor. Consider using the controller to prevent charging above 45°C and reducing the current below 10°C. At 10°C the resistance of the thermistor is 18kΩ. At 45°C, the resistance drops to 4.7kΩ. The **ICS1712** has an internal voltage threshold at 10°C at 2.4V, and an internal voltage at 45°C at 0.93V as shown in Figure 9. At 25°C the voltage at the THERM pin is set at the midpoint of the thresholds:

$$0.93\text{V} + \frac{2.40\text{V} - 0.93\text{V}}{2} = 1.67\text{V}.$$

The THERM pin has a 75kΩ internal pull-up (R_{pu}). Using a resistor divider with 10kΩ for the thermistor (R_{th}) and a external fixed resistor (R_{fix}), the divider looks like Figure 10 at 25°C:

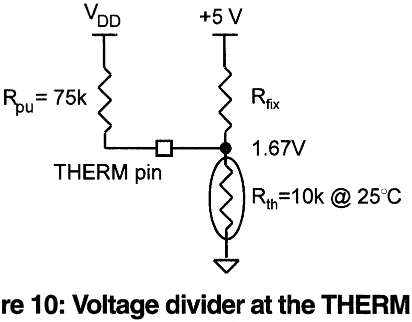


Figure 10: Voltage divider at the THERM pin at 25°C

To set the voltage at the THERM pin for 1.67V at 25°C, the equivalent divider looks like Figure 11.

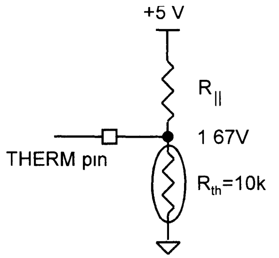


Figure 11: Equivalent voltage divider

The parallel resistance $R_{||}$ is calculated:

$$R_{||} = \frac{5V - 1.67V}{1.67V/10k\Omega} = 20k\Omega$$

The internal pull-up resistance R_{pu} and the parallel resistance $R_{||}$ are known so the external fixed resistor can be calculated from:

$$R_{fix} = \frac{R_{pu}R_{||}}{R_{pu} - R_{||}}.$$

Substituting in known values: R_{fix} = 27.27kΩ. A 27kΩ standard value is used for R_{fix}.

Since the thermistor resistance R_{th} is specified by manufacturers at a particular temperature, the voltage across the thermistor V_{th} at that temperature can be calculated from:

$$Vth = \frac{R_{th}}{R_{||} + R_{th}}(5V),$$

with the drop across the resistor divider equal to 5V. For this example, the calculated voltage with R_{th}=18kΩ at 10°C is 2.37V and with R_{th}=4.7kΩ at 45°C the voltage is 0.95V. Table 6 lists the internal thresholds for hot and cold battery detection. If the voltage across the thermistor (at the THERM pin) drops below 0.93V, the **ICS1712** will shut down due to a hot battery fault condition and will not restart unless reset. If the voltage dropped across the thermistor is above 2.4V before fast charge is initiated, the **ICS1712** will begin a reduced current charge. See the *Cold Battery Charging* section for more information.

Table 4: Thermistor Voltage Thresholds

Parameter	Voltage	Battery Temperature
Cold Battery Thermistor Voltage	>2.4	<10°C
Hot Battery Thermistor Voltage	<0.93	>45°C

- Using an NTC thermistor for temperature slope termination:

As a battery approaches full charge, its accelerated rate of heating can be used to terminate fast charge by detecting the large change in the temperature slope. The large change in temperature slope is proportional to the thermistor voltage change per unit of time. If the DTSEL pin is programmed for temperature slope termination, the controller will calculate the thermistor voltage slope and terminate based on internally set thresholds as listed in Table 1. The threshold is 40mV per minute for selected charge rates greater than C/2 and 28mV per minute for selected charge rate C/2. The voltage across the thermistor must change at these rates or greater to terminate the selected charge rate.

These thresholds correspond to a set change in thermistor resistance when an external pull-up to 5V is used as shown in Figure 11. Using the values calculated from the hot and cold battery detection example, the percent change in the thermistor resistance per minute for selected charge rates are provided. For selected charge rates greater than C/2, the thermistor resistance must decrease 4%/min. to terminate charge. For selected charge rate C/2, the thermistor resistance must decrease 3%/min. to terminate charge.

For example, a battery was monitored as it charged at a 1C rate in 25°C ambient. In the final minute of charge, the battery temperature rose from 29.8°C to 31°C where full charge was detected. With this data, the typical 10kΩ @ 25°C thermistor used in the example above is checked to determine if its characteristics satisfy the 4% decrease in resistance required for the last minute of charge. The thermistor measures 8.37kΩ @ 29.8°C and 8.01kΩ at 31°C. For a 1C charge rate, the resistance must decrease at least 4%/min. or more between 29.8°C and 31°C. The percent decrease in resistance for the thermistor is calculated as:

$$\frac{8.37\text{k}\Omega - 8.01\text{k}\Omega}{8.37\text{k}\Omega}(100) = 4.30\%.$$

This thermistor meets the 4%/min. requirement and will result in termination at full charge at 31°C. The thermistor must be checked for a 4%/min. decrease in resistance for the last minute of charge near the hot and cold battery thresholds.

The battery in the example above was charged in a 25°C ambient with its temperature rising 31°C - 25°C or 6°C. The temperature rise was 31°C - 29.8°C or 1.2°C in the last minute before full charge occurred. This information is used to check the thermistor characteristics at the ambient extremes. If the selected 1C charge rate is initiated at 12°C, the thermistor resistance change must decrease 4%/min. between 16.8°C and 18°C. The thermistor resistance at 16.8°C is 13.68kΩ and at 18°C the thermistor resistance is 13.06kΩ.

$$\frac{13.68\text{k}\Omega - 13.06\text{k}\Omega}{13.68\text{k}\Omega}(100) = 4.53\%$$

The thermistor meets the 4%/min. requirement and will result in termination of fast charge at 18°C. If the selected 1C charge rate is initiated at 37°C, the thermistor resistance change must decrease 4%/min. between 41.8°C and 43°C. The thermistor resistance at 41.8°C is 5.48kΩ and at 43°C the thermistor resistance is 5.25kΩ.

$$\frac{5.48\text{k}\Omega - 5.25\text{k}\Omega}{5.48\text{k}\Omega}(100) = 4.19\%$$

The thermistor meets the 4%/min. requirement and will result in termination of fast charge at 43°C.

The 4%/min. and 3%/min. decrease in thermistor resistance for the last minute of charge for the selected charge rate are applicable for NTC thermistors other than 10kΩ @ 25°C provided that the following requirements are met:

- An external pull-up resistor to 5V is used to provide a thermistor voltage of 1.67V @ 25°C.
- The thermistor resistance at 25°C does not exceed 20kΩ so that accuracy and adequate noise immunity are maintained.
- The thermistor resistance increases by a factor of about 1.8 from 25°C to 10°C and the thermistor resistance decreases by a factor of about 2.1 from 25°C to 45°C.

• Using a thermal switch for hot battery detection:

A thermal switch that opens at about 45°C is recommended. The thermal switch must be connected between the THERM pin and ground. When the thermal switch is closed, the voltage at the THERM pin must be below 0.5V for normal operation. When the thermal switch opens (see Figure 12), the internal pull-up at the THERM pin will raise the voltage above 4.2V and the **ICS1712** will shut down and will not restart unless reset. Table 5 contains the internal voltage thresholds used with a thermal switch.

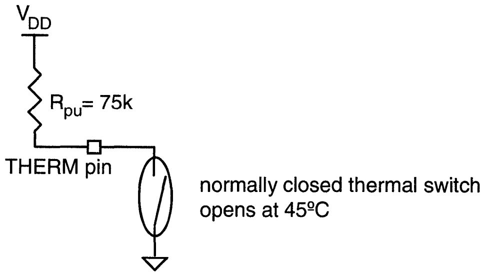


Figure 12: Thermal switch to connection to ground at the THERM pin

Table 5: Thermal Switch Voltage Thresholds

Parameter	Voltage	Battery Temperature
Opened Thermal Switch Voltage	>4.2	>45°C
Closed Thermal Switch Voltage	<0.5	<45°C

- Using no temperature sensor:

If a temperature sensor is not used, the THERM pin must be grounded.

Termination Selection: DTSEL Pin

The **ICS1712** has the capability of either temperature slope termination, voltage slope termination or both methods simultaneously. The DTSEL pin has an internal 75kΩ pull-down resistor that enables voltage slope termination as the primary method and is the default condition. Tying the pin high enables both temperature slope and voltage slope termination methods. Temperature slope termination as the primary method is enabled by tying the DTSEL pin to the CMN output (pin 4). CMN must have an external 15kΩ or lower value pull-up resistor to V_{DD} for proper activation of temperature slope termination. The **ICS1712** must be reset if a new termination method is desired. Table 6 summarizes the DTSEL pin settings. NOTE: Maximum temperature and fast charge timer termination methods are always enabled when using temperature slope termination. Refer to the sections on *Fast Charge Timer Termination* and *Maximum Temperature Termination* for more information.

Table 6: Termination Select List

Tie DTSEL Pin to ...	Result
Low (No Connect)	Voltage slope termination only
High	Voltage slope and temperature slope termination
CMN	Temperature slope termination only (CMN with external pull-up to V_{DD})

Voltage Input: VIN Pin

The battery voltage must be normalized by an external resistor divider network to one cell. The electrochemical potential of one cell is about 1.2V. For example, if the battery consists of six cells in series, the voltage at the VIN pin must be equal to the total battery voltage divided by six. This can be accomplished with two resistors, as shown in Figure 13. To determine the correct resistor values, count the number of cells to be charged in series. Then choose either R1 or R2 and solve for the other resistor using:

$$R1 = R2 \times (\text{\# of cells -1}) \text{ or } R2 = \frac{R1}{(\text{\# of cells - 1})}$$

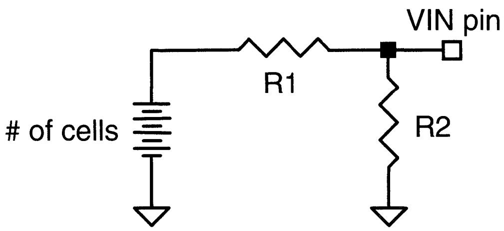


Figure 13: Resistor divider network at the VIN pin

Power: VDD Pin

The power supply for the device must be connected to the VDD pin. The voltage should be +5 VDC and should be supplied to the part through a regulator that has good noise rejection and an adequate current rating. The controller requires up to a maximum of 11mA with V_{DD}=5.00V.

Grounding: VSS, AVSS Pins

There are two ground pins. Both pins must be connected together at the device. This point must have a direct connection to a solid ground plane.

Data Tables

Table 7: Absolute Maximum Ratings

Supply Voltage	6.5	V
Logic Input Levels	-0.5 to V_{DD} + 0.5	V
Ambient Operating Temperature	0 to 70	°C
Storage Temperature	-55 to 150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at the Absolute Maximum Ratings or other conditions not consistent with the characteristics shown in this document is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 8: DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Supply Current	I_{DD}			7.3		mA
High Level Input Voltage SEL0, SEL1	V_{IH}		3.6	4.1	4.5	V
Low Level Input Voltage SEL0, SEL1	V_{IL}		0.73	0.75	0.8	V
Low Level Input Current, pull-up THERM, MRN	I_{IL}	V=0.4V		74		µA
High Level Input Current, pull-down DTSEL	I_{IH}	V=V_{DD}-0.4V		75		µA
High Level Source Current CHG, DCHG	I_{OH}	V=V_{DD}-0.4V		28		mA
Low Level Sink Current CHG, DCHG	I_{OL}	V=0.4V		25		mA
Low Level Sink Current, indicator PFN, CMN	I_{OL}	V=0.4V		40		mA
Low Level Sink Current, indicator OTN	I_{OL}	V=0.4V		28		mA
Input Impedance				1.0		MΩ
Analog/Digital Converter Range			0-2.2	0-2.7	0-2.7	V

Table 9: DC Voltage Thresholds

T_{AMB}=25°C

PARAMETER	TYP	UNITS
Minimum Battery Voltage	0.5	V
Maximum Battery Voltage	2.0	V
Thermistor - Cold Temperature	2.4	V
Thermistor - Hot Temperature	0.93	V
Thermal Switch - Open	4.2	V
Thermal Switch - Closed	0.5	V

Table 10: Timing Characteristics

R≈16kΩ, C≈100pF

PARAMETER	SYMBOL	REFERENCE	TYP	UNITS
Clock Frequency			1.0	MHz
Reset Pulse Duration	t_{RESET}	see Figure B	700	ms
Charge Pulse Width	t_{CHG}	see Figure A	1048	ms
Discharge Pulse Width	t_{DCHG}	see Figure A	5.0	ms
Rest Time	t_R	see Figure A	4.0	ms
Data Acquisition Time	t_{DA}	see Figure A	16.4	ms
Cycle Time	t_{CYCLE}	see Figure A	1077	ms
Capacitor Discharge Pulse Width			5.0	ms
Capacitor Discharge Pulse Period			100	ms
Polling Detect Pulse Width			100	ms
Polling Detect Pulse Period			624	ms
Soft Start Initial Pulse Width			200	ms
Soft Start Incremental Pulse Width			7.0	ms
RESET to SEL Dynamic Reprogram Period	t_{RSA}	see Figure B	1160	ms

Timing Diagrams

Figure A:

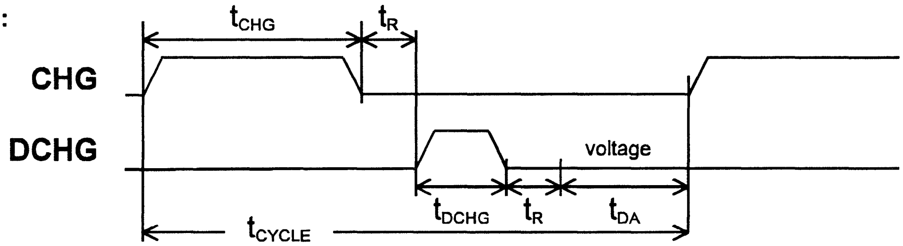
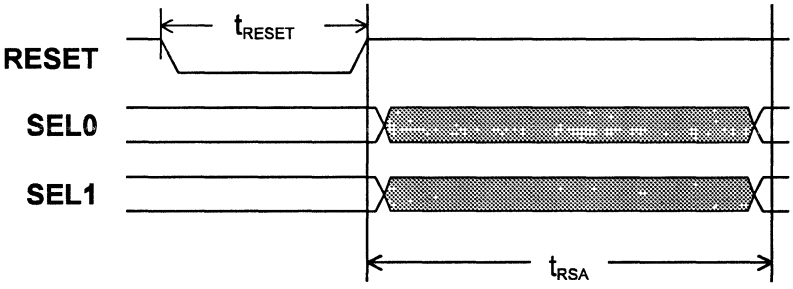


Figure B:



Applications Information

To ensure proper operation of the **ICS1712**, external components must be properly selected. The external current source used must meet several important criteria to ensure optimal performance of the charging system. The charging current should be constant when using voltage slope termination. The current may vary when using temperature slope termination.

VIN Divider Resistors

Figure 14 shows a typical application using the **ICS1712**. R1 and R2 must be carefully selected to ensure that battery detection and voltage termination methods operate properly. R1 and R2 are selected to scale the battery voltage down to the voltage of one cell. The following table shows some typical values. Additional information is available in the *Voltage Input* section.

Cells	R1	R2
1	Short	Open
2	2.0k	2.0k
3	2.0k	1.0k
4	3.0k	1.0k
5	12k	3.0k
6	10k	2.0k
7	12k	2.0k
8	9.1k	1.3k

If using voltage slope termination, the current source should prevent ripple voltage from appearing on the battery. The effects of ripple on the battery voltage may interfere with proper operation when using the voltage slope method.

PC Board Design Considerations

It is very important that care be taken to minimize noise coupling and ground bounce. In addition, wires and connectors can add significant resistance and inductance to the charge and discharge circuits.

When designing the printed circuit board, make sure ground and power traces are wide and bypass capacitors are used right at the controller. Use separate grounds for the signal, charge and discharge circuits. Separate ground planes on the component side of the PC board are recommended. Be sure to connect these grounds together at the negative lead of the battery only. For the discharge circuit, keep the physical separation between power and return (ground) to a minimum to minimize field radiation effects. This precaution is also applicable to the constant current source, particularly if it is a switch mode type. Keep the **ICS1712** and the constant current source control circuits outside the power and return loop described above. These precautions will prevent high circulating currents and coupled noise from disturbing normal operation.

Selecting the Appropriate Termination Method

In general, the voltage slope termination method works best for equipment where the battery is fast charged with the equipment off or the battery is removed from the equipment for fast charge. The temperature slope and maximum temperature termination methods are for equipment that must remain operative while the battery is fast charged.

• Voltage Slope Termination

The voltage slope termination method used by the **ICS1712** requires a nearly constant current flow into the battery during fast charge. Equipment that draws a known constant current while the battery is charging may use the voltage slope termination method. This constant current draw must be added to the fast charge current. Using the voltage slope termination method for equipment that randomly or periodically requires moderate current from the battery during fast charge needs evaluation. Equipment that randomly or periodically requires high current from the battery during fast charge may cause a voltage inflection that results in termination before full charge. A voltage inflection can occur due to the charge current decreasing or fluctuating as the load changes rather than by the battery reaching full charge. The voltage slope method will terminate charge based on voltage inflections that are characteristic of a fully charged battery.

Charging sources that produce decreasing current as fast charge progresses may also cause a voltage inflection that may result in termination before full charge. For example, if the charge current is supplied through a resistor or if the charging source is a constant current type that has insufficient input voltage, the current will decrease and may cause a termination before full charge. Other current source abnormalities that may cause a voltage inflection that is characteristic of a fully charged battery are inadequate ripple and noise attentuation capability or charge current decreasing due to thermal drift. Charging sources that have any of the above characteristics need evaluation to access their suitability for the application if the use of the voltage slope termination is desired.

When using voltage slope termination, the controller soft start stage, built-in noise filtering, and fast charge timer operate optimally when the constant current source charges the battery at the rate selected. If the actual charge current is significantly less than the rate selected, the conditioning effect of the soft start stage and the controller noise immunity are lessened. Also, the fast charge timer may cause termination based on time duration rather than by the battery reaching full charge due to inadequate charge current.

• Temperature Slope and Maximum Temperature

Temperature slope and/or maximum temperature termination may have to be used for equipment that has high dynamic current demands while operating from the battery during fast charge. Also, users who do not have a well regulated constant current source available may have to use temperature termination. In general, utilizing temperature slope as the primary termination method with maximum temperature termination as a safety back-up feature is the best approach. When using temperature slope termination, the actual current should not be appreciably lower than the selected rate in order that termination of fast charge occurs due to the battery reaching full charge rather than by the timer expiring.

Temperature termination methods require that the thermal sensor be in intimate contact with the battery. A low thermal impedance contact area is required for accurate temperature sensing. The area and quality of the contact surface between the sensor and the battery directly affects the accuracy of temperature sensing. Thermally conductive adhesives may have to be considered in some applications to ensure good thermal transfer from the battery case to the sensor.

The thermal sensor should be placed on the largest surface of the battery for the best accuracy. The size of the battery is also a consideration when using temperature termination. The larger the battery the lower the surface area to volume ratio. Because of this, larger batteries are less capable in dissipating internal heat.

Additional considerations beyond the basics mentioned above may be involved when using temperature slope termination where sudden changes in ambient temperature occur or where forced air cooling is used. For these applications, the surface area of the thermal sensor in contact with the battery compared to the surface area of the thermal sensor in contact with the ambient air may be significant. For example, bead type thermistors are relatively small devices which have far less thermal capacity compared to most batteries. Insulating the surface of the thermistor that is in contact with the ambient air should help minimize heat loss by the thermistor and maintain accuracy.

Maximum Temperature Termination

Maximum temperature termination is best suited as a safety back-up feature. Maximum temperature termination requires that the thermal sensor be in intimate contact with the battery. A low thermal impedance contact area is required for accurate temperature sensing. The area and quality of the contact surface between the sensor and the battery directly affects the accuracy of temperature sensing. Thermally conductive adhesives may have to be considered in some applications to ensure good thermal transfer from the battery case to the sensor.

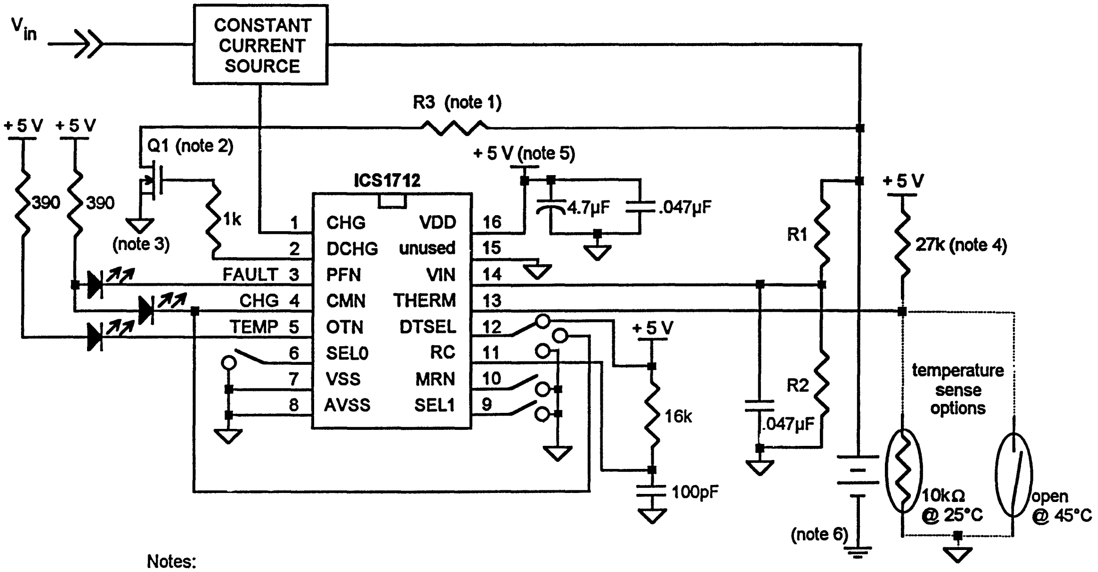
The thermal sensor should be placed on the largest surface of the battery for the best accuracy. The size of the battery is also a consideration when using temperature termination. The larger the battery, lower the surface area to volume ratio. Because of this, larger batteries are less capable in dissipating internal heat.

Additional considerations beyond the basics mentioned above may be involved when using maximum temperature termination where sudden changes in ambient temperature occur or where forced air cooling is used. For these applications, the surface area of the thermal sensor in contact with the battery compared to the surface area of the thermal sensor in contact with the ambient air may be significant. For example, bead type thermistors are relatively small devices which have far less thermal capacity compared to most batteries. Insulating the surface of the thermistor that is in contact with the ambient air should help minimize heat loss by the thermistor and maintain accuracy.

Charging System Status by Indicator

The *Indicator Description List* in Table 2 contains displays that are caused by charging system abnormalities. At power-up or after a reset is issued, one flash of the CMN indicator followed by a continuous PFN indication results from a voltage present at the battery terminals with the current source off and no battery. Check the current source and ensure that it produces no more than the equivalent of 350mV/cell when turned off with no battery. If the VIN divider resistors were not properly selected, an open circuit voltage that is actually less than the equivalent of 350mV/cell with the charger off and no battery will not divide down this open circuit voltage properly and produce a PFN fault indication. Check the VIN divider and ensure that it properly normalizes the battery voltage to the electrochemical potential of about 1.2V cell. If the PFN fault indicator is active immediately after power-up or after a reset is issued with the battery installed, then the constant current source is producing more than the equivalent of 350mV/cell when off and there is an open connection between the charger terminals and the battery. Check wires, connections, battery terminals, and the battery itself for an open circuit condition.

If the CMN and OTN indicators are active together, this is an indication that the battery temperature has dropped to below 10°C after a fast charge was initiated with the battery temperature normal. If this condition is observed and the battery temperature did not drop after fast charge was initiated, check the thermistor circuit mechanically for poor contact and electrically for excessive noise.



Notes:

1) Value of R3 determined by discharge current and capacity of battery pack.
2) Discharge FET is logic-level compatible in this application.
3) DC return of discharge FET must be connected close to negative battery terminal.
4) Resistor is needed only if a thermistor is used. Value may change depending on thermistor.
5) Regulated supply
6) Power ground; others are signal ground. Connect signal ground to power ground at negative battery terminal only.

Figure 14: Functional Diagram

Ordering Information

ICS1712N, ICS1712M, or ICS1712MT

Example:

ICS XXXX M

Package Type
N=DIP (Plastic)
M=SOIC
MT=SOIC Tape and Reel
Device Type (consists of 3-5 digit numbers)
Prefix
ICS=Standard Device

Integrated
Circuit
Systems, Inc.

ICS1722

QuickSaver® Charge Controller for Nickel-Cadmium and Nickel-Metal Hydride Batteries

General Description

The **ICS1722** is a CMOS device designed for the intelligent charge control of either nickel-cadmium (NiCd) or nickel-metal hydride (NiMH) batteries. The controller uses a pulsed-current charging technique together with voltage slope termination. The **ICS1722** employs a four stage charge sequence that provides a complete recharge without overcharging. The controller has nine user-selectable charge rates and six user-selectable auxiliary modes available for customized charging systems.

The **ICS1722** monitors for the presence of a battery and begins charging when a battery is installed. The **ICS1722** is for applications where temperature sensing is not required by the charge controller.

Applications

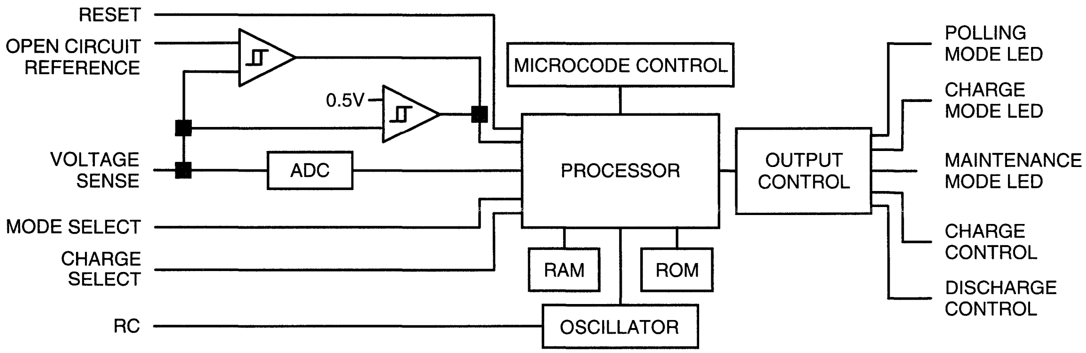
Battery charging systems for:

- Portable consumer electronics
- Power tools
- Audio/video equipment
- Communications equipment

Features

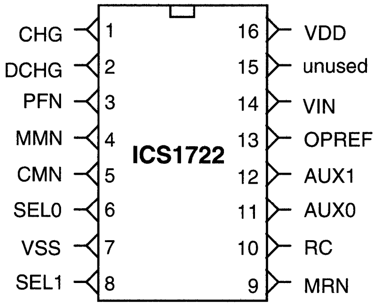
- Charge termination methods include:
  - Voltage slope
  - Charge timers
- Four stage charge sequence:
  - Soft start charge
  - Fast charge
  - Topping charge
  - Maintenance charge
- Reverse-pulse charging available in all charge stages
- Nine programmable charge rates between 15 minutes (4C) and four hours (C/4)
- Continuous polling mode for battery detection
- Six auxiliary modes include:
  - Discharge-before-charge
  - Ten hour C/10 conditioning charge
  - Direct to C/40 maintenance charge
  - Charging system test provided through controller
- Adjustable open circuit (no battery) voltage reference

Block Diagram



QuickSaver is a registered trademark of Integrated Circuit Systems, Inc

Pin Configuration



16-Pin DIP or SOIC
K-4, K-6

Pin Definitions

Pin Number	Pin Name	Type	Definition
1	CHG	OUT	Active high TTL compatible signal used to turn on an external current source to provide current to charge the battery.
2	DCHG	OUT	Active high TTL compatible signal available to turn on a discharge circuit.
3	PFN	OUT	Polling detect indicator An active low turns on an external indicator to show the controller is polling for the presence of the battery
4	MMN	OUT	Maintenance mode indicator. An active low turns on an external indicator showing the battery is either in the topping charge, maintenance charge or auxiliary condition mode The indicator flashes during the auxiliary discharge mode.
5	CMN	OUT	Charge mode indicator. An active low turns on an external indicator to show the controller is either in a soft start charge or fast charge
6	SEL0	IN	Tri-level input used with the SEL1 pin to program the device for the desired charge rate.
7	VSS		Ground.
8	SEL1	IN	Tri-level input used with the SEL0 pin to program the device for the desired charge rate
9	MRN	IN	Master reset signal. A logic low pulse greater than 700 ms initiates a device reset.
10	RC	IN	An external resistor and capacitor sets the frequency of the internal clock.
11	AUX0	IN	Tri-level input used with the AUX1 pin to program the device for an auxiliary operating mode
12	AUX1	IN	Tri-level input used with the AUX0 pin to program the device for an auxiliary operating mode.
13	OPREF	IN	Open circuit (no battery) voltage reference. An external pull-down resistor on this pin sets the open circuit voltage reference used to detect the presence of a battery.
14	VIN	IN	Battery voltage normalized to one cell with an external resistor divider.
15	unused		Ground.
16	VDD		Device supply =+5.0 VDC

Note: Pins 9 and 13 have an internal pull-up.
Pins 6, 8, 11, 12 float to 2 3V when unconnected.

Controller Operation

Charging Stages

The charging sequence consists of four stages. The application of current is shown graphically in Figure 1. The soft start stage gradually increases current levels up to the user selected fast charge rate during the first two minutes. The soft start stage is followed by the fast charge stage, which continues until termination. After termination, a two hour C/10 topping charge is applied. The topping charge is followed by a C/40 maintenance charge.

Soft Start Charge

Some batteries may exhibit an unusual high impedance condition while accepting the initial charging current, as shown in Figure 2. Unless dealt with, this high impedance condition can cause a voltage peak at the beginning of the charge cycle that would be misinterpreted as a fully charged battery by the voltage termination methods.

The soft start charge eases batteries into the fast charge stage by gradually increasing the current to the selected fast charge rate. The gradual increase in current alleviates the voltage peak. During this stage, only positive current pulses are applied to the battery. The duty cycle of the applied current is increased to the selected fast charge rate, as shown in Figure 3, by extending the current pulse on every cycle until the pulse is about one second in duration. The initial current pulse is approximately 200ms. The CMN indicator is activated continuously during this stage.

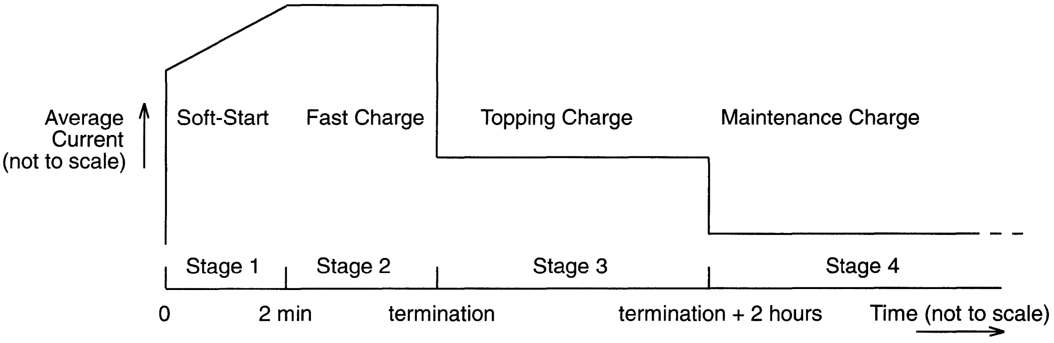


Figure 1: Graphical representation of average current levels during the four charging stages

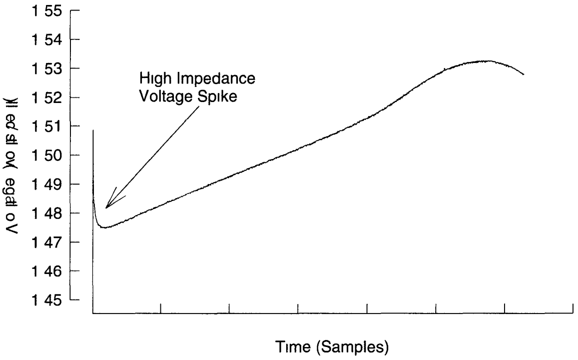


Figure 2: High impedance voltage spike at the beginning of charge

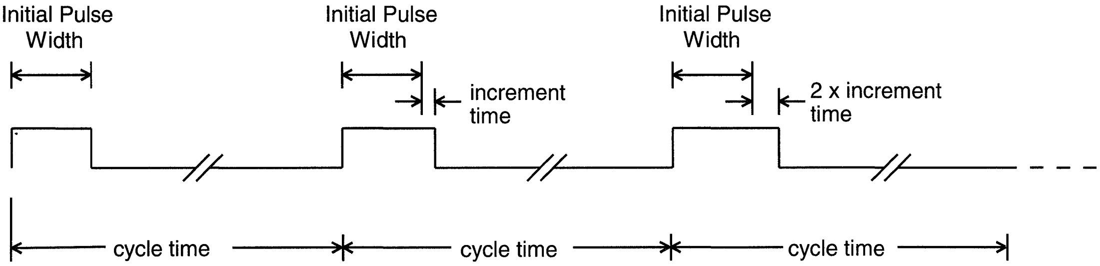


Figure 3: Cycle-to-cycle increase of the soft-start current pulse widths

Fast Charge

In the second stage, the **ICS1722** applies the charging current in a series of charge and discharge pulses. The technique consists of a positive current charging pulse followed by a high current, short duration discharge pulse. The cycle, shown with charge, discharge, rest and data acquisition periods in Figure 4, repeats every second until the batteries are fully charged.

The amplitude of the current pulse is determined by system parameters such as the current capability of the charging system, the desired charge rate, the cell capacity and the ability of that cell to accept the charge current. The **ICS1722** can be set for nine user-selectable fast charge rates from 15 minutes (4C) to four hours (C/4). Charge pulses occur approximately every second. The CMN indicator is activated continuously during this stage.

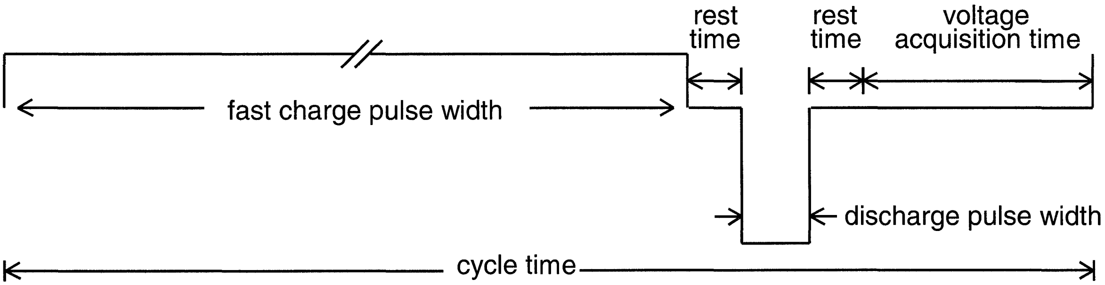


Figure 4: Charge cycle showing charge and discharge current pulses

The discharge current pulse amplitude is typically set to about 2.5 times the amplitude of the charging current based on 1.4V/cell. For example, if the charge current is 4 amps, then the discharge current is set at about 10 amps. The energy removed during the discharge pulse is a fixed ratio to the positive charge rate. The amplitude of the discharge pulse does not affect the operation of the part as described in this section.

A voltage acquisition window immediately follows a brief rest time after the discharge pulse. No charge is applied during the rest time or during the acquisition window to allow the cell chemistry to settle. Since no current is flowing, the measured cell voltage is not obscured by any internal or external IR drops or distortions caused by excess plate surface charge. The **ICS1722** makes one continuous reading of the no-load battery voltage during the entire acquisition window. The voltage that is measured during this window contains less noise and is a more accurate representation of the true state of charge of the battery.

Topping Charge

The third stage is a topping charge that applies current at a rate low enough to prevent cell heating but high enough to ensure a full charge.

The topping charge applies a C/10 charging current for two hours. The current consists of the same pulse technique used during the fast charge stage; however, the duty cycle of the pulse sequence has been extended as shown in Figure 5. Extending the time between charge pulses allows the same charging current used in the fast charge stage so that no changes to the current source are necessary. For example, the same charge pulse that occurs every second at a 2C fast charge rate will occur every 20 seconds for a topping charge rate of C/10. The MMN indicator is activated continuously during this stage.

Maintenance Charge

The maintenance charge is intended to offset the natural self-discharge of NiCd or NiMH batteries by keeping the cells primed at peak charge. After the topping charge ends, the **ICS1722** begins this charge stage by extending the duty cycle of the applied current pulses to a C/40 rate. The maintenance charge will last for as long as the battery voltage is greater than 0.5V at the VIN pin, or, if the ten hour timer mode is enabled, until the timer stops the controller. The MMN indicator is activated continuously during this stage.

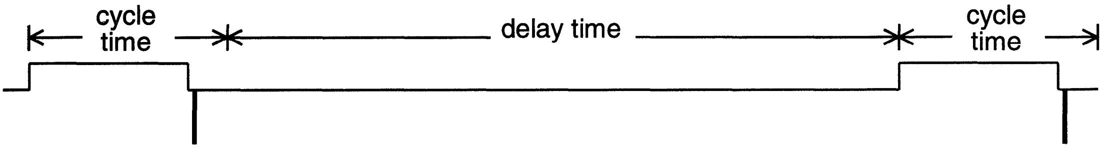


Figure 5: Representative timing diagram for topping and maintenance charge

Charge Termination Methods

Charge termination schemes include voltage slope, fast charge timer and, if desired, a ten hour timer to limit total charge time.

Voltage Slope Termination

The most distinctive point on the voltage curve of a charging battery in response to a constant current is the voltage peak that occurs as the cell approaches full charge. By mathematically calculating the first derivative of the voltage, a second curve can be generated showing the change in voltage with respect to time as shown in Figure 6. The slope will reach a maximum just before the actual peak in the cell voltage. Using the voltage slope data, the **ICS1722** calculates the point of full charge and accurately terminates the applied current as the battery reaches that point. The actual termination point depends on the charging characteristics of the particular battery.

Cells that are not thoroughly conditioned or possess an unusual cell construction may not have a normal voltage profile. The **ICS1722** uses an alternate method of charge termination based on a slight decrease in the voltage slope to stop charge to cells whose voltage profile is very shallow. This method looks for a flattening of the voltage slope which may indicate a shallow peak in the voltage profile.The zero slope point occurs slightly beyond the peak voltage and is shown on the voltage curve graph.

Charge Timer Termination

The controller uses a timer to limit the fast charge duration. These times are pre-programmed, and are automatically adjusted in time duration according to the charge rate selected. Fast charge timer termination is a safety backup feature to limit the duration of the fast charge stage. The fast charge timer is always enabled and cannot be disabled. See Table 3 in the section *Charge Rate Selection* for more information. To limit the total charge time to ten hours, refer to the section *Ten Hour Timer Mode* for more information.

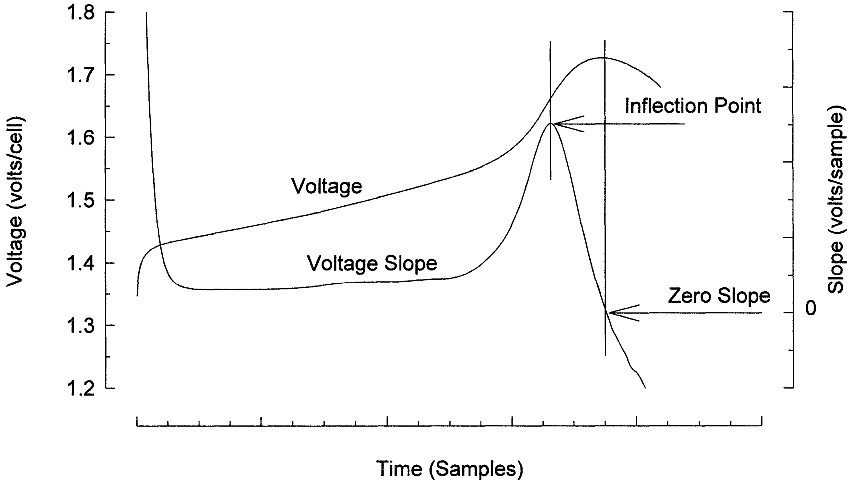


Figure 6: Voltage and slope curves showing inflection and zero slope points

Battery Detection

Upon power-up or after a master reset, excess charge from output filter capacitors at the charging system terminals is removed with a series of discharge pulses. After the discharge pulse sequence is complete, the voltage at VIN must be greater than 0.5V when a battery is present. If the voltage at the pin is less than 0.5V, the **ICS1722** assumes no battery is present, and the polling detect mode is initiated. No indicator is active during the discharge pulses.

The **ICS1722** enters the polling detect mode and applies a 100ms charge pulse. During the pulse, the **ICS1722** monitors the VIN pin to determine if the divided down terminal voltage is above OPREF. If the battery is present, the voltage will be clamped below the reference on OPREF while the current pulse is applied. If a battery is not present, the voltage at VIN will rise above the reference at OPREF.

The charge pulse will repeat at one second intervals until the battery is reinstalled. The polling detect indicator (PFN) is the only indicator active as long as the **ICS1722** is in the polling detect mode. Once a battery is installed, the **ICS1722** will turn off the PFN indicator and enter the soft start stage. The **ICS1722** will automatically re-enter the polling detect mode if the battery is removed.

Battery Removal

During the application of a charge pulse, the voltage at the VIN pin is compared to the voltage at the OPREF pin. If the voltage at VIN is greater than the voltage at OPREF during the application of the current pulse, then the battery is assumed to have been removed and the **ICS1722** enters the polling detect mode. If the voltage at VIN is below the voltage at OPREF, charging continues.

When in the topping charge or maintenance charge stages, a charge pulse may not occur for several seconds. During the period between charge pulses, the voltage at VIN must be greater than 0.5V if a battery is attached. If the voltage at VIN is less than 0.5V, the **ICS1722** assumes the battery has been removed, and the polling detect mode is initiated.

Auxiliary Modes of Operation

The **ICS1722** allows six alternate modes of operation to help customize the charging system for certain applications. The tri-level AUX0 and AUX1 pins are used to select the operating mode. The AUX0 and AUX1 pins default the **ICS1722** into fast charge operation. Except for the discharge-to-charge mode, another mode can only be selected by re-programming and resetting the controller.

Discharge-to-Charge Mode

The time required for discharge depends on the energy in the battery and the discharge rate. The discharge is not limited by a timer. This allows the user to set the discharge rate. The battery is drained to 1 volt/cell as read at the VIN pin under load and then the controller enters soft start at a charge rate set by the SEL0 and SEL1 inputs. The discharge load is activated by the DCHG pin which goes low for about 400ms every second. A resistor value selected for a 2.5C discharge based on 1.4V/cell results in about a 1C discharge rate.

The discharge-to-charge mode can be entered by placing the AUX0 pin high (H) and the AUX1 pin low (L) with the SEL0 and SEL1 inputs set for the desired fast charge rate. This setting initializes the discharge sequence. The **ICS1722** enters the discharge-to-charge mode at initial power-up or with a master reset. The discharge mode occurs first, to be followed by the selected fast charge mode. During discharge, the MMN indicator flashes at a one second rate, while during the soft start and fast charge stages the CMN indicator is activated continuously.

Four charge modes are available after the discharge portion is complete by changing the state of the AUX inputs during the discharge portion of this mode. The available charge modes are:

- Fast Charge: Leave the AUX inputs open (Z).
- Direct Maintenance Mode: Set the AUX0 low (L) and AUX1 high (H).
- Condition Mode: Set AUX0 high (H) and AUX1 open (Z).
- Ten-Hour Timer Mode: Set AUX0 high (H) and AUX1 high (H).

If the battery is removed while in the discharge-to-charge mode, the **ICS1722** will continually reset itself until the battery is reinstalled. See *Application Information* for more information.

Discharge-Only Mode

The time required for discharge depends on the energy in the battery and the discharge rate. The discharge is not limited by a timer. This allows the user to set the discharge rate. The battery is drained to 1 volt/cell as read at the VIN pin under load. The **ICS1722** shuts down after the discharge sequence is finished and a master reset must be performed to reactivate the device. The discharge load is activated by the DCHG pin which goes low for about 400ms every second. A resistor value selected for a 2.5C discharge based on 1.4V/cell results in about a 1C discharge rate. The discharge-only mode can be entered by placing the AUX0 pin open (Z) and the AUX1 pin low (L). The **ICS1722** enters this mode at initial power-up or with a master reset. During the discharge portion, the MMN indicator flashes at a one second rate.

Direct Maintenance Mode

The **ICS1722** can enter directly into the C/40 maintenance mode for cells that require a maintenance charge only. The direct maintenance mode is activated by setting the AUX0 pin low (L) and the AUX1 pin high (H), and resetting the device. The SEL0 and SEL1 pins must be set based on the charging current and the battery capacity. The formula

$$\frac{\text{Charging Current (Amps)}}{\text{Battery Capacity (Amp} \bullet \text{hr)}}$$

gives the charge rate. Use Table 3 to find the correct SEL0 and SEL1 settings. The maintenance charge is applied until the battery is removed, upon which the **ICS1722** will enter the polling detect mode. The **ICS1722** will enter the direct maintenance mode upon initial power-up or after a master reset. The MMN indicator will be active during this mode.

Conditioning Mode

The **ICS1722** can enter a conditioning mode which applies a C/10 charge for a timed 10 hour period, followed by an indefinite C/40 maintenance charge until the batteries are removed.

The conditioning mode can be entered by setting the AUX0 pin high (H) and the AUX1 pin open (Z). The SEL0 and SEL1 pins must be set based on the charging current and the battery capacity. The formula

$$\frac{\text{Charging Current (Amps)}}{\text{Battery Capacity (Amp} \bullet \text{hr)}}$$

gives the charge rate. Use Table 3 to find the correct SEL0 and SEL1 settings. The MMN indicator will be active during the 10 hour conditioning charge and the maintenance charge that follows. The **ICS1722** enters the polling detect mode if the battery is removed.

Ten Hour Timer Mode

Placing the AUX0 and AUX1 pins both high (H) enables a ten hour timer. This timer limits the total charge, including the maintenance charge, to approximately ten hours for a battery that is completely discharged before fast charge is initiated. The ten hour limit is based on the assumption that the charge terminates due to the fast charge timer as shown in Table 1.

Charging System Test

The system test mode is intended for use in applications where the charging system functionality needs to be tested. The system test sequence consists of a one second activation of the CMN, MMN and PFN indicator pins as well as the CHG and DCHG lines. The system test mode is entered by placing both the AUX0 and AUX1 pins low (L). The **ICS1722** shuts down after the test sequence is finished and a master reset must be performed to reactivate the device.

Table 1: Ten Hour Timer Information

Charge Rate	Fast Charge Timer Cutoff	Maintenance Timer Cutoff (after fast charge termination)	Charge Time Limit (from reset)
4 C	0.3 hrs	9.7 hrs	10 hrs
2 C	0.6 hrs	9.4 hrs	10 hrs
1.3 C	0.9 hrs	9.1 hrs	10 hrs
1 C	1.2 hrs	8.8 hrs	10 hrs
C/1.5	1.8 hrs	8.2 hrs	10 hrs
C/2	2.4 hrs	7.6 hrs	10 hrs
C/2.5	3.5 hrs	6.5 hrs	10 hrs
C/3	4.0 hrs	6.0 hrs	10 hrs
C/4	4.6 hrs	5.4 hrs	10 hrs

Pin Descriptions

The **ICS1722** requires some external components to control the clock rate and provide an indicator display. The controller must be interfaced to an external power source that will provide the current required to charge a battery pack and, if desired, a circuit that will sink discharge current.

Output Logic Signals: CHG, DCHG Pins

The CHG and DCHG pins are active high, TTL compatible outputs. In addition to being TTL compatible, the CMOS outputs are capable of sourcing current which adds flexibility when interfacing to other circuitry. A logic high on the CHG pin indicates that the charging current supply should be activated. If applicable, a logic high on the DCHG pin indicates that the discharge circuit should be activated.

Care must be taken to control wiring resistance and inductance. The load resistor must be capable of handling this short duration high-amplitude pulse. If the auxiliary discharge-to-charge mode is selected, the power dissipation of the load resistor must be properly selected to accept the extended length of the discharge pulse.

Indicators: CMN, MMN, PFN Pins

The controller has three outputs for driving external indicators. These pins are active low. The three indicator outputs have open drains and are designed to be used with LEDs. Each output can sink over 20mA which requires the use of an external current limiting resistor. The three indicator signals denote fast charge stage, topping and maintenance stages, and the polling detect mode as shown in Table 2.

The charge mode (CMN) indicator is activated continuously during the soft start and fast charge stages. When the controller enters the topping charge stage, the output goes high and the indicator turns off.

The maintenance mode (MMN) indicator is on when the **ICS1722** is either in the topping charge, maintenance charge, direct maintenance mode, or the condition mode. The maintenance mode indicator flashes at a one second rate when the **ICS1702** is controlling the discharge portion of the discharge-to-charge or the discharge-only mode.

The polling detect (PFN) indicator is on when the **ICS1722** polls for a battery. The controller applies periodic charge pulses to detect the presence of a battery. The indicator is a warning that these charge pulses are appearing at the charging system terminals at regular intervals. When a battery is detected, the indicator is turned off.

Charge Rate Selection: SEL0, SEL1 Pins

The SEL0 and SEL1 inputs must be programmed by the user to inform the **ICS1722** of the desired charge rate. When left unconnected (open), these tri-level pins will float to about 2.3V. When a low level is required, the pin must be grounded. When a high level is required, the pin must be tied to V_{DD}. The voltage ranges for low (L), open (Z) and high (H) are listed in Table 6, *DC Characteristics*. To program the SEL0 and SEL1 inputs, refer to the *Charge Rate List* in Table 3.

The **ICS1722** does not control the current flowing into the battery in any way other than turning it on and off. The required current for the selected charge rate must be provided by the user's power source. The external charging circuitry should provide current at the selected charge rate. For example, to charge a 1.2 ampere hour battery in 30 minutes (2C), approximately 2.4 amperes of current is required.

Table 2: Indicator Description List

PFN	MMN	CMN	Description
on			Polling detect mode
	on		Maintenance or topping charge, direct maintenance or condition mode
		on	Fast charge
	flash		Discharge portion of the discharge-to-charge or discharge-only mode
		flash	see Applications Information
	flash	flash	see Applications Information
	on		Fast charge (see Applications Information)

Table 3: Charge Rate List

SEL0	SEL1	Charge Rate	Topping Charge Pulse Rate	Maintenance Charge Pulse Rate	Fast Charge Timer Duration (after reset)
L	L	4C (15 min)	one every 40 sec	one every 160 sec	21 min
L	H	2C (30 min)	one every 20 sec	one every 80 sec	39 min
L	Z	1.3C (45 min)	one every 13 sec	one every 53 sec	57 min
H	L	1C (60 min)	one every 10 sec	one every 40 sec	75 min
H	Z	C/1.5 (90 min)	one every 7 sec	one every 27 sec	110 min
H	H	C/2 (120 min)	one every 5 sec	one every 20 sec	144 min
Z	L	C/2.5 (150 min)	one every 4 sec	one every 16 sec	212 min
Z	Z	C/3 (180 min)	one every 3 sec	one every 13 sec	244 min
Z	H	C/4 (240 min)	one every 2 sec	one every 10 sec	275 min

See the section on *Controller Operation* for additional information on the topping charge and maintenance charge. See the section on *Charge Termination Methods* for additional information on the charge timer.

Mode Selection: AUX0, AUX1 Pins

The AUX0 and AUX1 inputs must be programmed by the user to inform the **ICS1722** of the desired auxiliary mode. When left unconnected (open) these tri-level pins will float to about 2.3V. When a low level is required, the pin must be grounded. When a high level is required, the pin must be tied to V_{DD}. The voltage ranges for low (L), open (Z) and high (H) are listed in Table 6, *DC Characteristics*. To program the AUX0 and AUX1 inputs, refer to the Mode Select List in Table 4. See the section on Auxiliary Modes of Operation for additional information.

Table 4: Mode Select List

AUX0	AUX1	Mode Selected	Mode Operation
L	L	Charging System Test	Charging system test for embedded applications
L	H	Direct Maintenance	Indefinite C/40 maintenance charge
Z	Z	Fast Charge	Default
Z	L	Discharge-Only	Battery discharge to 1V/cell
H	L	Discharge-to-Charge	Battery discharge to 1V/cell followed by the selected charge mode
H	Z	Condition	Timed C/10 topping charge followed by a C/40 maintenance charge
H	H	Ten Hour Timer	Limits total charge including the maintenance charge to 10 hours

Master Reset: MRN Pin

The MRN pin is provided to re-program the controller for a new mode or charging sequence. This pin has an internal pull-up of about 75kΩ. A logic low on the MRN pin must be present for more than 700ms for a reset to occur. As long as the pin is low, the controller is held in a reset condition. A master reset is required to clear the charging system test, reset the ten hour timer, change charge rates or auxiliary modes. Upon power-up, the controller automatically resets itself.

Clock Input: RC Pin

The RC pin is used to set the frequency of the internal clock when an external 1 MHz clock is not available. An external resistor must be connected between this pin and V_{DD}. An external capacitor must be connected between this pin and ground. The frequency of the internal clock will be about 1 MHz with a 16kΩ resistor and a 100pF capacitor. All time durations noted in this document are based on a 1 MHz clock. Operating the clock at a lower frequency will proportionally change all time durations. Operating the clock at a frequency significantly lower than 1 MHz, without adjusting the charge current accordingly, will lessen the effectiveness of the fast charge timer and lower the accuracy of the controller. Operating the clock at a frequency greater than 1 MHz will also change all time durations and, without adjusting the charge current accordingly, may cause termination to occur due to the fast charge timer expiring rather than by the battery reaching full charge.

The clock may be driven by a 1 MHz external 0 to 5V pulse provided the duty cycle is between 10% and 60%. The clock input impedance is about 1kΩ.

Voltage Input: VIN Pin

The battery voltage must be normalized by an external resistor divider network to one cell. The electrochemical potential of one cell is about 1.2V. For example, if the battery consists of six cells in series, the voltage at the VIN pin must be equal to the total battery voltage divided by six. This can be accomplished with two resistors, as shown in Figure 7. To determine the correct resistor values, count the number of cells to be charged in series. Then choose either R1 or R2 and solve for the other resistor using:

$$R1 = R2 \times (\text{\# of cells -1}) \text{ or } R2 = \frac{R1}{(\text{\# of cells - 1})}$$

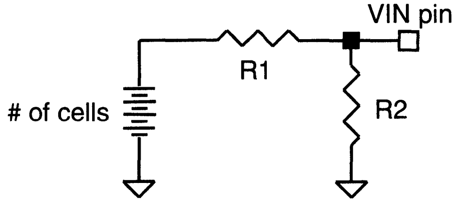


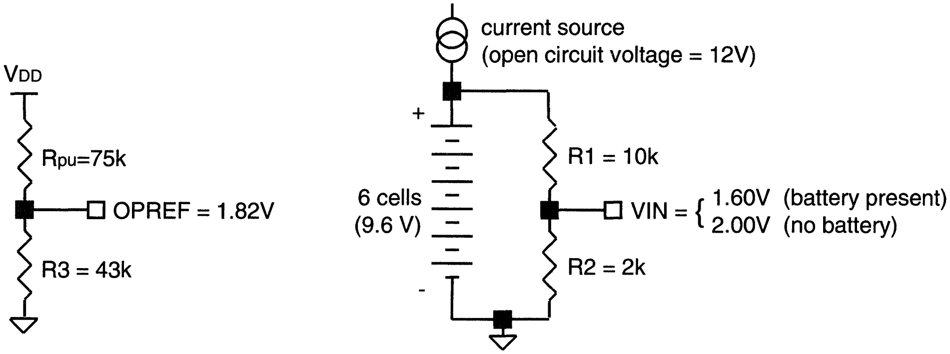
Figure 7: Resistor divider network at the VIN pin

Open Circuit Voltage Reference: OPREF Pin

The OPREF pin has an internal 75kΩ pull-up resistor to V_{DD}. OPREF requires an external pull-down resistor to establish the open circuit (no battery) voltage reference. The purpose of this voltage reference is to detect the removal of the battery from the charging system. The voltage at this pin is compared to the voltage at the VIN pin when the current source is turned on. If the voltage at VIN is greater than the voltage at OPREF, the **ICS1722** assumes the battery has been removed and the **ICS1722** enters the polling detect mode.

For proper operation, the voltage at OPREF must be set below the (divided down) open circuit voltage produced by the current source and above the maximum normalized battery voltage. The OPREF pin voltage must not exceed 2.3V or it will prevent the start of fast charge. If the voltage on OPREF exceeds 4V, the controller will shutdown and must be reset.

As an example, suppose that a current source has an open circuit voltage of 12V as shown in Figure 8. The maximum expected battery voltage of a six-cell pack is determined to be 9.6V. The voltage at OPREF should be set at a point between 1.6V (9.6V/6 cells=1.6V) and 2V (12V/6=2V). This is accomplished with a pull-down resistor. Refer to the VIN and OPREF resistor tables in the *Applications Information* section. From the VIN table, the divider resistors are 10kΩ and 2kΩ for R1 and R2. From the OPREF table, the pull-down resistor is 43kΩ for R3. If R3 is 43kΩ, the voltage at OPREF is 1.82V since the internal pull-up at the OPREF pin is 75kΩ..



Resistor divider at the OPREF pin

Resistor divider at the VIN pin

Figure 8: Open Circuit Reference Example

Power: VDD Pin

The power supply for the device must be connected to the VDD pin. The voltage should be +5 VDC and should be supplied to the part through a regulator that has good noise rejection and an adequate current rating. The controller requires up to a maximum of 11mA with V_{DD}=5.00V.

Grounding: VSS Pin

This pin must have a direct connection to a solid ground plane.

Data Tables

Table 5: Absolute Maximum Ratings

Supply Voltage	6.5	V
Logic Input Levels	-0.5 to V_{DD} + 0.5	V
Ambient Operating Temperature	0 to 70	°C
Storage Temperature	-55 to 150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at the Absolute Maximum Ratings or other conditions not consistent with the characteristics shown in this document is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 6: DC Characteristics

T_{amb}=25°C. All values given are typical at specified V_{DD}.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Supply Current	I_{DD}			7.3		mA
High Level Input Voltage SEL0, SEL1, AUX0, AUX1	V_{IH}		3.6	4.1	4.5	V
Low Level Input Voltage SEL0, SEL1, AUX0, AUX1	V_{IL}		0.73	0.75	0.8	V
Open Input Voltage SEL0, SEL1, AUX0, AUX1		open		2.3		V
Low Level Input Current, pull-up MRN, OPREF	I_{IL}	V=0.4V		74		µA
High Level Source Current CHG, DCHG	I_{OH}	V=V_{DD}-0.4V		28		mA
Low Level Sink Current CHG, DCHG	I_{OL}	V=0.4V		25		mA
Low Level Sink Current, indicator PFN, CMN, MMN	I_{OL}	V=0.4V		40		mA
Input Impedance				1.0		MΩ
Analog/Digital Converter Range			0-2.2	0-2.7	0-2.7	V
Minimum Battery Threshold				0.5		V

Table 7: Timing Characteristics

R≈16kΩ, C≈100pF

PARAMETER	SYMBOL	REFERENCE	TYP	UNITS
Clock Frequency			1.0	MHz
Reset Pulse Duration	t_{RESET}	see Figure B	700	ms
Charge Pulse Width	t_{CHG}	see Figure A	1048	ms
Discharge Pulse Width	t_{DCHG}	see Figure A	5.0	ms
Rest Time	t_R	see Figure A	4.0	ms
Data Acquisition Time	t_{DA}	see Figure A	16.4	ms
Cycle Time	t_{CYCLE}	see Figure A	1077	ms
Capacitor Discharge Pulse Width			5.0	ms
Capacitor Discharge Pulse Period			100	ms
Polling Detect Pulse Width			100	ms
Polling Detect Pulse Period			624	ms
Soft Start Initial Pulse Width			200	ms
Soft Start Incremental Pulse Width			7.0	ms
Discharge Mode Pulse Width			400	ms
Discharge Mode Pulse Period			1050	ms
RESET to SEL Dynamic Reprogram Period	t_{RSA}	see Figure B	1160	ms
RESET to AUX Dynamic Reprogram Period	t_{RSA}	see Figure B	1160	ms

Timing Diagrams

Figure A:

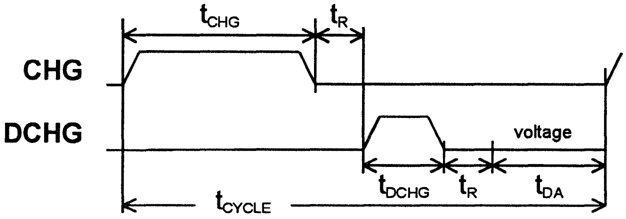
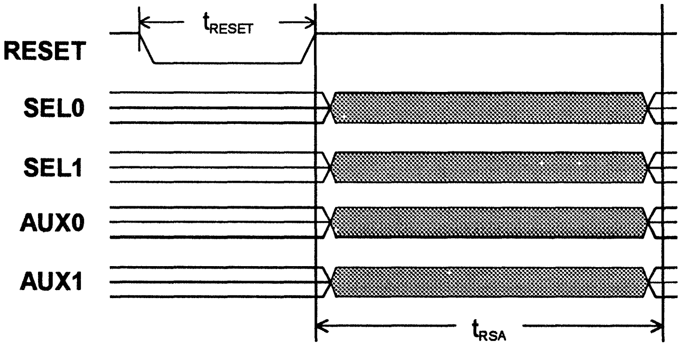


Figure B:



Applications Information

To ensure proper operation of the **ICS1722**, external components must be properly selected. The external current source used must meet several important criteria to ensure optimal performance of the charging system. The charging current should be constant when using voltage slope termination.

VIN and OPREF Divider Resistors

Figure 9 shows a typical application using the **ICS1722.** R1 through R3 must be carefully selected to ensure that battery detection and voltage termination methods operate properly. R1 and R2 are selected to scale the battery voltage down to the voltage of one cell. The following table shows some typical values. Additional information is available in the *Voltage Input* section.

Cells	R1	R2
1	Short	Open
2	2.0k	2.0k
3	2.0k	1.0k
4	3.0k	1.0k
5	12k	3.0k
6	10k	2.0k
7	12k	2.0k
8	9.1k	1.3k

The current source should prevent ripple voltage from appearing on the battery. The effects of ripple on the battery voltage may interfere with proper operation.

R3 is used to set the open circuit (no battery) reference voltage on the OPREF pin. The function of this pin is discussed in the *Open Circuit Reference* section.

VOPREF	R3
1.82 V	43k
1.93 V	47k
2.02 V	51k
2.14 V	56k

With the batteries removed, the current source must be capable of raising the voltage at the VIN pin above the voltage at the OPREF pin to ensure proper polling. With the batteries installed, the current source overshoot characteristics when turned on and off must not cause the voltage at the VIN pin to exceed the voltage at the OPREF pin. If the voltage at OPREF exceeds the voltage at VIN when a charge pulse is applied or removed, the polling feature will be activated.

PC Board Design Considerations

It is very important that care be taken to minimize noise coupling and ground bounce. In addition, wires and connectors can add significant resistance and inductance to the charge and discharge circuits.

When designing the printed circuit board, make sure ground and power traces are wide and bypass capacitors are used right at the controller. Use separate grounds for the signal, charge and discharge circuits. Separate ground planes on the component side of the PC board are recommended. Be sure to connect these grounds together at the negative lead of the battery only. For the discharge circuit, keep the physical separation between power and return (ground) to a minimum to minimize field radiation effects. This precaution is also applicable to the constant current source, particularly if it is a switch mode type. Keep the **ICS1722** and the constant current source control circuits outside the power and return loop described above. These precautions will prevent high circulating currents and coupled noise from disturbing normal operation.

Using the Voltage Slope Termination Method

In general, the voltage slope termination method works best for equipment where the battery is fast charged with the equipment off or the battery is removed from the equipment for fast charge.

The voltage slope termination method used by the **ICS1722** requires a nearly constant current flow into the battery during fast charge. Charging the battery in equipment that draws a known constant current while the battery is charging should have this current draw added to the fast charge current. Using the **ICS1722** for charging the batteries in equipment that randomly or periodically requires moderate current from the battery during fast charge needs evaluation. Equipment that randomly or periodically requires high current from the battery during fast charge may cause a voltage inflection that results in termination before full charge. A voltage inflection can occur due to the charge current decreasing or fluctuating as the load changes rather than by the battery reaching full charge. The voltage slope method will terminate charge based on voltage inflections that are characteristic of a fully charged battery. The ICS1702 and ICS1712 charge controllers have temperature termination methods for equipment that randomly or periodically draws significant current from the battery during fast charge.

Charging sources that produce decreasing current as fast charge progresses may also cause a voltage inflection that may result in termination before full charge. For example, if the charge current is supplied through a resistor or if the charging source is a constant current type that has insufficient input voltage, the current will decrease and may cause a termination before full charge. Other current source abnormalities that may cause a voltage inflection that is characteristic of a fully charged battery are inadequate ripple and noise attenuation capability or charge current decreasing due to thermal drift. Charging sources that have any of the above characteristics need evaluation to access their suitability for the application if the use of the voltage slope termination is desired.

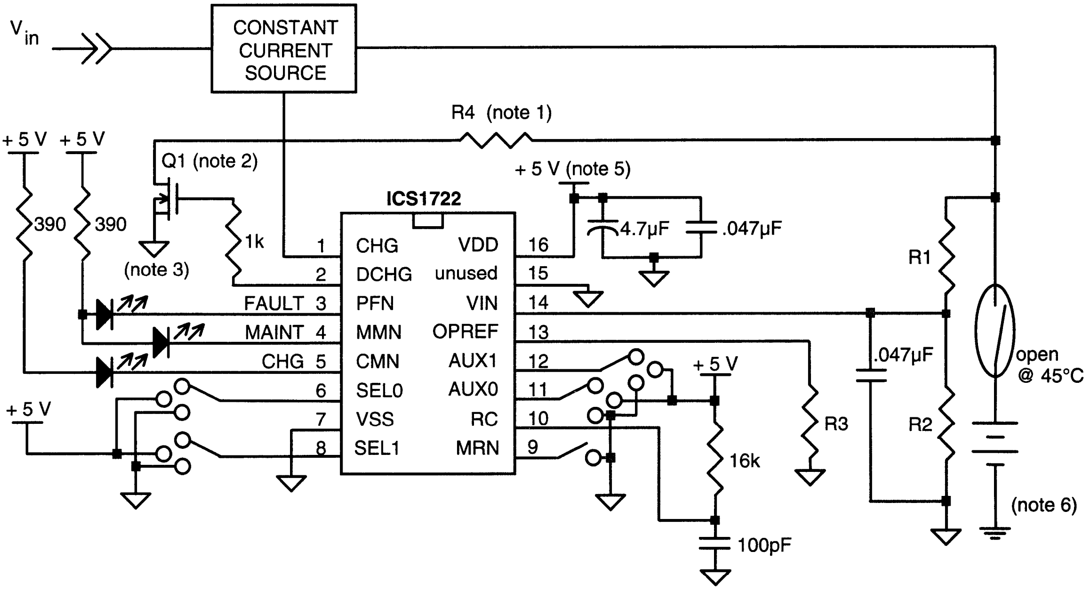
The controller soft start stage, built-in noise filtering, and fast charge timer operate optimally when the constant current source charges the battery at the rate selected. If the actual charge current is significantly less than the rate selected, the conditioning effect of the soft start stage and the controller noise immunity are lessened. Also, the fast charge timer may cause termination based on time duration rather than by the battery reaching full charge due to inadequate charge current.

Charging System Status by Indicator

The *Indicator Description List* in Table 2 contains displays that are caused by charging system abnormalities. When the CMN indicator is flashing with no other indicator active, there is voltage present at the battery terminals with the current source off and no battery. Check the current source and ensure that it produces no more than the equivalent of 350mV/cell when turned off with no battery. If the VIN divider resistors were not properly selected, an open circuit voltage that is actually less than the equivalent of 350mV/cell with the charger off and no battery will not divide down this open circuit voltage properly and produce the CMN flash indication. Check the VIN divider and ensure that it properly normalizes the battery voltage to the electrochemical potential of about 1.2V cell. If the CMN flash indication occurs with the battery installed, then the constant current source is producing more than the equivalent of 350mV/cell when off and there is an open connection between the charger terminals and the battery. Check wires, connections, battery terminals, and the battery itself for an open circuit condition.

If the MMN and CMN indicators are alternately flashing, the likely cause is no battery with the **ICS1722** programmed in the discharge-to-charge auxiliary mode. If the battery is present, check wires, connectors, battery terminals, and the battery itself for an open circuit condition.

If the MMN indicator is active at the initiation of fast charge, check the external pull-down resistor from OPREF to ground. A voltage at OPREF that exceeds 2.3V will prevent the start of fast charge.



Notes:

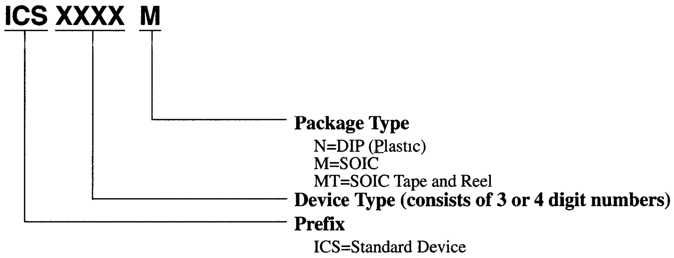
1) Value of R4 determined by discharge current and capacity of battery pack.
2) Discharge FET is logic-level compatible in this application.
3) DC return of discharge FET must be connected close to negative battery terminal.
4) Regulated supply
5) Power ground; others are signal ground. Connect signal ground to power ground at negative battery terminal only.

Figure 9: Functional Diagram

Ordering Information

ICS1722N, ICS1722M, or ICS1722MT

Example:



ICS XXXX M

Package Type
N=DIP (Plastic)
M=SOIC
MT=SOIC Tape and Reel
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS=Standard Device

ICS

ASIC Capabilities

J

Mixed Analog/Digital Technology

ICS's capability in mixed analog/digital (mixed mode) technology is a direct outgrowth of 16 years experience providing turn-key designs. We have found that few mixed-mode applications lend themselves to a high level of integration with standard cells only. Customization is critical to bridge the gap between standard cells and the application.

ICS's confidence and success in mixed-mode design is due to our custom cell approach and our focus on understanding the systems in which the IC must perform. We firmly believe the development of any mixed-signal IC can be completed quickly and accurately by our team of skilled, experienced analog designers.

At ICS we use a custom cell based design methodology for our analog designs. We have developed the tools and expertise that allow us to customize analog cells reliably and inexpensively. This approach combines the ease of design and low risk of standard cells with the flexibility of full custom.

Of course, developing a functioning analog circuit is not as easy as connecting a few cells. An analog designer must view the circuit function as a whole to ensure correct and accurate performance. Below is a representative list of analog functions which we have designed and produced.

Power Conversion/Regulation

Bandgap Voltage Reference
Linear Voltage Regulator
Charge-Pump Voltage Booster
Charge-Pump Voltage Inverter
Microprocessor Reset/Clock Supervisor
Low Battery Detect
Power Switching Circuits

Control/Actuator Drive

Stepper Motor Driver
Air-Core Meter Movement Driver
Pulse-Width Modulated Motor Driver
Solenoid Driver
SCR/Triac Drive/Phase Control
X-Y Sensor Grid Drive
4-20mA 2-Wire Current Loop
LVDT Demodulator/Driver

Miscellaneous

LED/LCD Display Drive
Crystal & Ceramic Resonator Oscillators
Timers/Oscillators
Precision Matched Current Sources
High-Frequency VCO/PLL (230 MHz)

Op-Amps

Low-Quiescent Current (uA)
Wide Input/Output Common Mode
High Speed (6 MHz)
High Output Current

A/D Converters

Successive Approximation
Dual-Slope
Sample/Track & Hold
V/F Converters

D/A Converters

R-2R
Weighted

Signal Conditioning

Active Filters
Balanced Synchronous Demodulator
Digital Sine Wave Synthesis
Fixed & Variable Gain AC Amplification

ASICS At ICS

ICS has been a leader in providing state-of-the-art mixed signal and complex digital ASIC designs since 1976. The company was founded by assembling an unequaled engineering and design team to supply the electronics industry with the best in technical solutions and customer service in the ASIC marketplace. ICS has developed over 400 circuits since its beginning, and its success in standard products can be attributed to the same attention to detail applied to ASIC contract designs. ASIC projects are an important part of our business, and we can provide our customers with the best, most cost-effective solution to their ASIC needs.

ICS has focused its resources on providing the very best technical design expertise in both analog and digital technology. The cornerstone of this expertise is a custom/cell based approach where ICS assumes responsibility for the design, simulation, layout and verification of each circuit. We use standard cell libraries together with custom cells/functions where needed, a fully integrated CAD system, and proven CMOS processes. In addition, we develop the test hardware and programs necessary for each device we design. Our goal is to supply a high quality product. We remain committed to every product through on-time delivery, inventory management and ongoing product engineering.

Our business philosophy is to form a partnership with any customer whose business and technical requirements fit our guidelines and capabilities. We provide our ASIC customers with product management, development and production sourcing capabilities, by acting as an extension of your own engineering force. Through this partnership we are able to provide the most cost-effective solution to meet your requirements. We have developed unique relationships with software design companies, silicon foundries, photomask houses, and assembly operations, both domestic and international. These relationships provide ICS with the flexibility to select from many particular methodologies, processes or techniques. Our high volume of standard product business insures competitive pricing and service that's second to none.

- **A Technical Engineering Focus** - - The ICS engineering design team assigned to your ASIC product is involved from concept through characterization. Test development is considered part of this design task, thereby assuring that all critical parameters are adequately tested. Our engineers develop a full understanding of the engineering application for each ASIC device which allows ICS to critically evaluate the planned approach.

- **Design Flexibility** - - ICS advanced design technology makes changes and modifications affordable and fast at any stage of design or production. Simple modifications can often be corrected in one or two mask levels, saving time and money when changes are needed.

- **Process Flexibility** - - To bring the very best technology to your application, our suppliers include many of the leading semiconductor foundries and packaging houses. This allows for multi-sourcing, various packaging alternatives, and optimal utilization of semiconductor process technology. The large volume of standard product business we do with our suppliers assures us of competitive pricing. This permits ICS to extend large-volume pricing advantages to our ASIC customers.

- **Complete Production Support** - - ICS's approach is to outsource mask tooling, wafer fab and assembly while maintaining in-house control over production control, testing, QC and product engineering.

ICS Application Specific Standard Product

ICS has the capability to customize any of the standard products we offer to better suit the needs of its customers. Customized Standard Products permit an OEM customer to optimize his system design and minimize the amount of "glue" logic (or "glue linear") required to implement his end product. This can result in significant size, power, and cost savings in most OEM products.

Customization of ICS standard products can entail various degrees of complexity. A simple example might be to change the sense of logic levels input or output from a standard product. Frequency Timing Generator products often require specific output frequencies, power-down capabilities, or control capabilities not available from our standard product listings. A more complex example would be the addition of latches to input or output signals. Perhaps the addition of a microphone preamplifier to one of the inputs of the ICS2101 audio mixer IC would simplify your design, packaging, and manufacturing task.

Obviously the investment in many of these alterations can be substantial in tooling and inventory costs. Therefore, the projected volume must justify the investment. In some cases ICS may be willing to share the cost if other markets can be found for the new product.

The growth of laptop and notebook personal computers in the marketplace has placed a severe demand on manufacturers in the area of packaging, power consumption, performance and cost. ASIC devices may be the only practical way to satisfy these needs.

The standard for computers since the first integrated circuits made their appearance in the marketplace has been 5 volt logic levels. Power consumption, size (due to the size of battery packs), and performance requirements are rapidly moving this standard towards 3 volt logic levels. ICS ASIC capabilities permit many standard products to be redesigned to work at 3 volt levels.

Since ICS standard products are a logical outgrowth of our ASIC experience they utilize the same wafer fabs, semiconductor processes, standard cell libraries and building blocks used in our ASIC designs. This allows ICS to use most of our standard products as super cells in ASIC designs. The inclusion of standard product designs in your large-scale ASIC design permits fully characterized building blocks to be incorporated into your ASIC with minimum risk when compared to designed-from-scratch implementations of a complex function. Design cost, risk, and time-to-market are also improved as we do not have to reinvent the wheel each time the function is needed.

Foundry Selection

The chart below shows the qualified CMOS processes used by ICS for ASIC and standard products. This chart is constantly changing, as ICS is always negotiating for the latest proven manufacturing technology. This allows us to offer the most competitive costs to our ASIC customers, while at the same time providing qualified, proven manufacturing processes. Please contact your ICS representative for the latest list of available processes applicable to your particular need.

ICS Technologies **Principal Features**

SEMICONDUCTOR TECHNOLOGY	SPEED	DENSITY	LSI CELLS	MULTI SOURCE	STD CELLS	GATE ARRAY	VOLTS	ANALOG CELLS	FULL CUSTOM
CMOS 3µ Single Metal	Medium 25 MHz	Medium	Some	YES	YES	NO	3-10	YES	YES
CMOS 3µ Double Poly	Medium	Medium	NO	YES	YES	NO	10	Switched Cap.	YES
CMOS 1.5µ Double Metal	High	OK Gates	Some	YES	YES	NO	5	YES	YES
CMOS Metal Gate	Low 10 MHz	Low	NO	YES	YES	NO	5-18	YES	YES
CMOS High Voltage	Low 10 MHz	Low	NO	NO	YES	NO	30	YES	YES
CMOS 1.0µ	High	High	Many	YES	YES	NO	5	YES	YES
CMOS .8µ	High	Very High	Many	NO	YES	NO	5	YES	YES
CMOS .6µ	High	Very High	Many	NO	YES	NO	5	YES	YES

ICS

Quality and Reliability Information

ICS: Reliability Through Design

Right from the start, we concentrate on the ultimate quality of the product. ICS product reliability is designed in to meet the necessary controls that are imposed during production and testing. All ICS designs utilize a variety of "design-process-rule checks" to insure that product performance is consistent with our quality and reliability goals. Design simulations and wafer data base file verifications play a prominent role throughout the prototype and are production stages of the design to eliminate test correlation problems after the design is completed.

In a continuing effort to improve reliability as new devices are being developed, we review the data acquired from previous device designs to determine if any changes are necessary to improve performance and/or enhance the new device's operation. We evaluate all aspects of packaging technology, including leadframe vs. die-size compatibility, packaging materials and methods. ICS develops test programs to isolate problems during wafer probe and final testing to assure the quality of our products.

An extremely important phase of the product development cycle is the characterization of devices to insure their functional performance and establish margins of performance relative to device specifications. Samples of prototype units are initially measured to ascertain their performance characteristics and to verify that the transition from design and simulation to production processes has not had any deleterious effects.

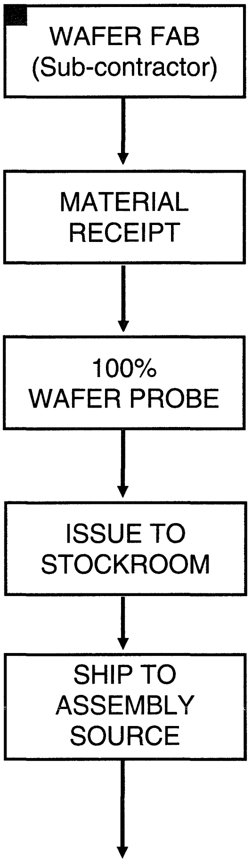
Production Flow

The production flow for ICS products is shown in the adjacent diagram, which provides some detail of the basic controls that are exercised through the various process stages. The processes of Wafer Fabrication, Assembly and Taping and Reeling are performed by outside facilities, with a process control- and electrical-data review for each lot of material before being routed for processing by these subcontractors. Wafer and package testing are performed at ICS.

A set of electrical characteristics data is provided for each wafer lot ICS receives. Every lot gets a parametric evaluation to determine the uniformity of the process and to serve as a quality control gate for wafer acceptance from manufacturing. SPC controls are maintained through the use of the accumulated profile parameters to serve as a source of electrical data feedback in support of process control and improvement programs. This data is also monitored by ICS to assess wafer fab performance and establish acceptance criteria for wafer fab lots. Environmental test monitoring including, HTOL, Temperature Cycling, Autoclave and Temperature/Humidity tests are performed to monitor the reliability of wafers produced.

The introduction of wafers into ICS from the wafer fab source initiates the traceability recording that tracks every part shipped from ICS. Wafer lot numbers assigned at the wafer fab source are recorded and are tracked through all stages of test, assembly, taping and ultimate shipment. At the ICS facility, all wafers are probed on a 100% basis before being shipped for assembly.

GENERAL PROCESS FLOW



- SPC PROCESS MONITORING
- WAFER PROBE PROCESS CONTROLS
- PROCESS RELIABILITY MONITORING

- INITIATE WAFER TRAVELER AND TRACEABILITY RECORDING

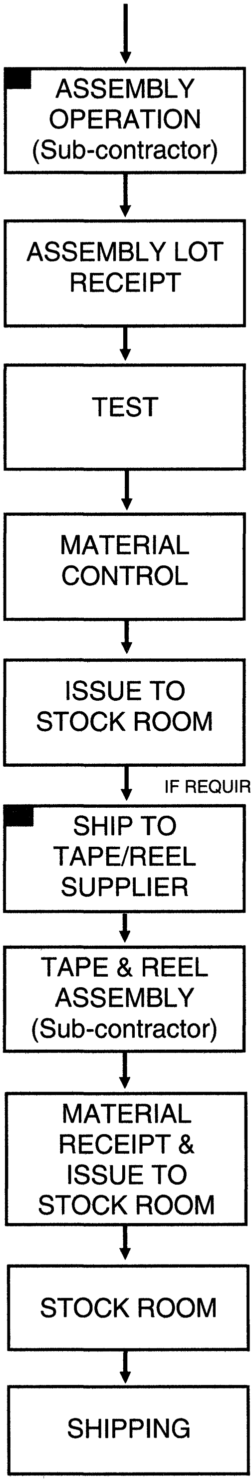
- MAINTAIN RECORDS OF EACH LOT FROM RECEIPT THROUGH PROBING, INSPECTION, STOCKING AND SHIPMENT TO ASSEMBLER

GENERAL PROCESS FLOW (continued)

Assembly suppliers are responsible to ICS for the processing of probed wafers into finished package configurations in accordance with ICS-supplied assembly specifications and bonding diagrams. Each assembly lot is supplied with a process traveler, which delineates the results of each process step and process monitor inspection. SPC data is maintained and reviewed on a periodic basis to assess such characteristics as: die shear, bond pull, solderability, marking permanence and process control elements pertinent to the assembly operations.

Processing at ICS includes incoming inspection examination of finished packages. Then we initiate test travelers to record test and inspection results and to allow for control of material into the stockroom. All parts are tested on a 100% basis in established test programs, and are checked on an AQL sampling basis for electrical and mechanical characteristics before acceptance to stock.

If customer requirements call for parts to be on tape & reel, the parts are packaged to ICS control specs for the implementation of this operation. The basic spec for this operation is per EIA Standard RS-481.



- APPROVED ASSEMBLY SOURCES WITH MONITORS OF PROCESS STEPS THROUGH ESTABLISHED SPC TRACKING AND PROCESS CONTROLS

- CONTROLLED ENVIRONMENT FOR TEMPERATURE/HUMIDITY/ ESD
- AQL SAMPLING OF ASSEMBLED PARTS AND REVIEW OF ASSEMBLY PROCESS LOT TRAVELERS
- 100% TEST OF ALL RECEIVED MATERIAL
- AQL SAMPLING FOR TEST AND AND MECHANICAL CHARACTERISTICS
- CONTROLLED STOCKROOM PENDING SHIPMENT

- TAPE & REEL OPERATIONS CONFORMING TO EIA STANDARDS RS-481

- INCOMING VISUAL EXAMINATION AND ISSUE STOCK FOR SHIPMENT

- FINAL PACKAGING AND SHIPMENT
- OUTGOING QUALITY AUDITS

Traceability

At ICS, traceability of products is a critical attribute of the entire production process. Tracking is initiated at the wafer fabrication process and is maintained through all successive processing steps through final shipment. Records of traceability are retained to allow for tracking of product delivered to a specific customer so that its source may be determined if the need arises. Records are also available for communicating with suppliers the identification and isolation of any problems.

Electrostatic Protection

The phenomenon of ESD (Electrostatic Discharge) can be a source of damage to sensitive semiconductor devices. In order to address this potential for damage a dual approach is initiated. It is first addressed in the design stage where the design guidelines provide for electrostatic protection of the input/output stages of the device. ESD susceptibility of each device is verified to ensure the design is robust enough to be handled in the customers' environment using normal handling precautions. A minimum level of 2kV is the standard for design; however, product currently under test is equal to or exceeds 4kV susceptibility levels. Tests are performed in accordance with MIL STD 883 method 3015.7.

Second, we protect against damage throughout the inspection, test and subsequent handling of parts. All personnel are aware of the effects of ESD and are trained in proper handling techniques. Work stations are ESD controlled with ground straps, ESD dissipative table tops and floor mats and air ionizers. Work in process is transported in conductive tubs and discharged before handling on the dissipative work tables. Parts are shipped in ESD protective tubes or reels which are further protected by electrostatic protective bags.

Product Qualification and Monitoring

The Quality Assurance Department is responsible for the qualification and monitoring of all devices manufactured by ICS. This activity is designed to evaluate all wafer processes and package configurations and to maintain a proactive corrective program to prevent the shipment of unreliable product.

In the qualification process, we apply the following tests and stresses:

High Temperature Operating Life

High temperature operating life (HTOL or HTOB) testing is performed to accelerate failure mechanisms which are thermally activated through the application of extreme temperatures and the use of biased operating conditions. The temperature and voltage conditions used in the stress will vary with the product being tested. However, the typical stress ambient is 125°C with the bias applied equal to or greater than the data sheet nominal value. All devices used in the HTOL test are sampled directly after final electrical test with no prior burn-in or other prescreening unless called out in the normal production flow. Testing can either be performed with dynamic signals applied to the device or in static bias configuration for a typical test duration of 1000 hours.

Temperature Humidity Bias

Temperature humidity bias (THB) is an environmental test performed at a temperature of 85°C and a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metalization. Most groups are tested to 1000 hours.

Autoclave

Autoclave is an environmental test which measures device resistance to moisture penetration and the resultant effects of galvanic corrosion. Autoclave is a highly accelerated and destructive test. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Groups of parts are normally tested for a 96 hour duration.

High Temperature Storage

High temperature storage is performed to measure the stability of semiconductor devices during storage at elevated temperatures with no electrical stress applied. The devices are typically exposed to an ambient of 150°C. An acceleration of charge loss from the storage cell or threshold changes are the expected results. All groups are typically tested to 1000 hours.

Temperature Cycle

Temperature cycle testing accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed per MIL STD 883 or MIL STD 750 with the minimum and maximum temperatures being -65°C and +150°C. During temperature cycle testing, devices are inserted into a cycling system and held at the cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minute minimum time period. The system employs a circulating air environment to assure rapid stabilization at the specified temperature. The dwell at each extreme, plus the two transition times of five minutes each (one up to the hot dwell temperature, another down to the cold dwell temperature), constitute one cycle. Test duration for this test will vary with the device and packaging system employed. A typical test consists of 300 cycles, however some tests are extended to look for longer term effects.

Thermal Shock

The objective of thermal shock testing is the same as that for temperature cycle testing - to emphasize differences in expansion coefficients for components of the packaging system. However, thermal shock provides the additional stress of sudden temperature change. This sudden change is due to the shorter transfer time, 10 seconds maximum, and the increased thermal conductivity of a liquid ambient. This test is typically performed per MIL STD 883 or MIL STD 750 with minimum and maximum temperatures being -65°C to +150°C. Devices are placed in a fluorocarbon bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes minimum, the devices are transferred to an adjacent chamber filled with fluorocarbon at the maximum specified temperature for an equivalent time. Two five-minute dwells plus two ten-second transitions constitute one cycle.

Reliability Data Analysis

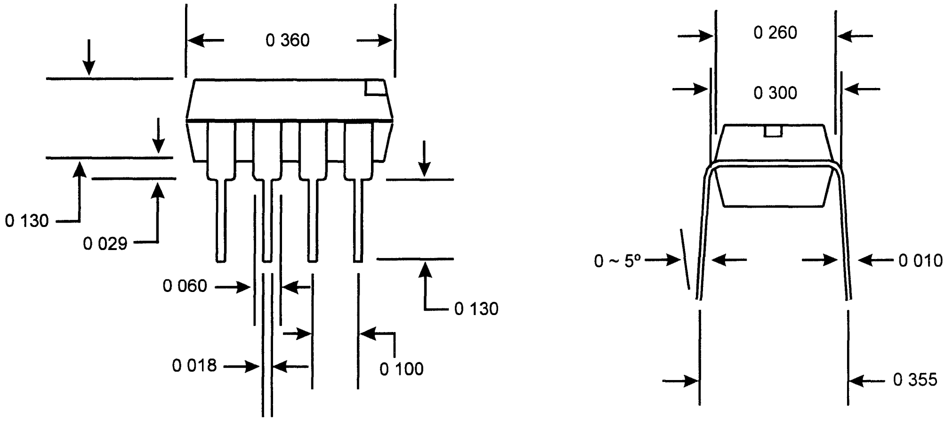
Reliability is the probability that a semiconductor device will perform its specified function in a given environment for a specified period of time. The most frequently used reliability measure is the device failure rate. The failure rate is obtained by dividing the number of failures observed by the product of the number of total device on test and the test time interval. This is normally expressed in failures per billion device hours (FITS), which is a point estimate because it is obtained from observations on a portion, or sample, of the population of devices.

To project the failure rate of devices being tested to a total population, chi-square distribution statistics are applied at established confidence intervals. These are nominally calculated at 60% and 90% confidence levels to express a level of confidence that the sample failure rate approximates that of the entire population. In addition, since the failure rate of semiconductor devices is inherently low, the application of acceleration factors is applied to the data. Commonly used Arrhenius equations are applied which provide relationships between test stress levels and normal use operation. In applying this assessment tool an activation energy (Ea) of 0.7Ea is normally used to determine the Acceleration factor. This Ea level is chosen in lieu of establishing individual Ea values for each of the failure mechanisms applicable to the technology and circuit under evaluation, particularly since the failure mechanism database is so limited.

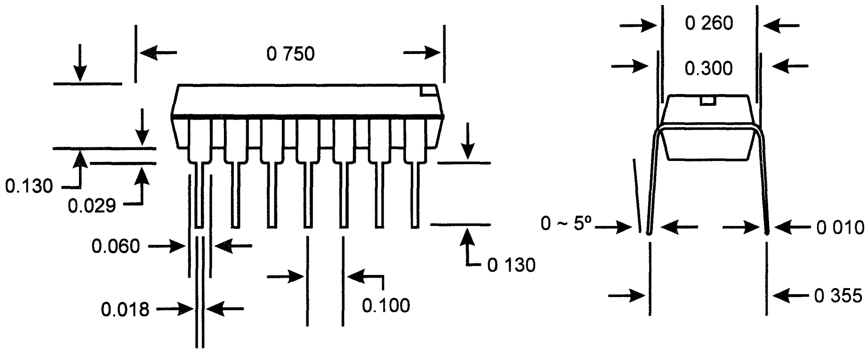
To determine the failure rate of ICS products, the HTOL data for individual as well as families of devices is utilized. HTOL testing provides an adequate thermal stress with the devices being biased at greater than nominal value and operated in a dynamic mode in this environment. Utilization of these techniques will provide a realistic, conservative estimation of the product failure rate.

ICS
Standard
Package Dimensions

DIP Packages



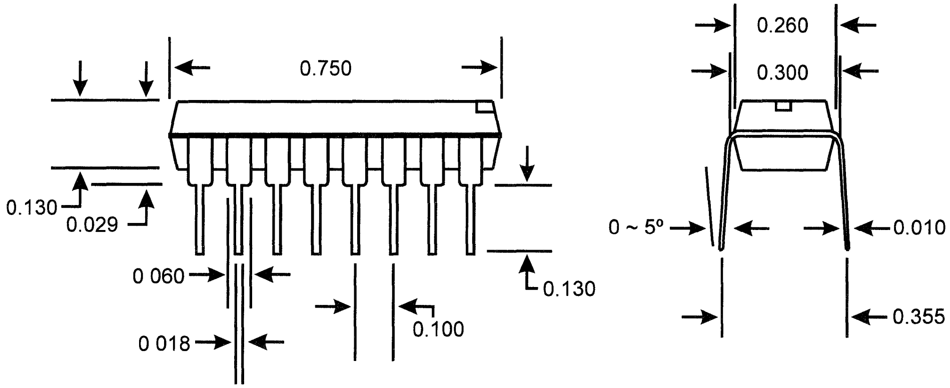
8-Pin DIP Package



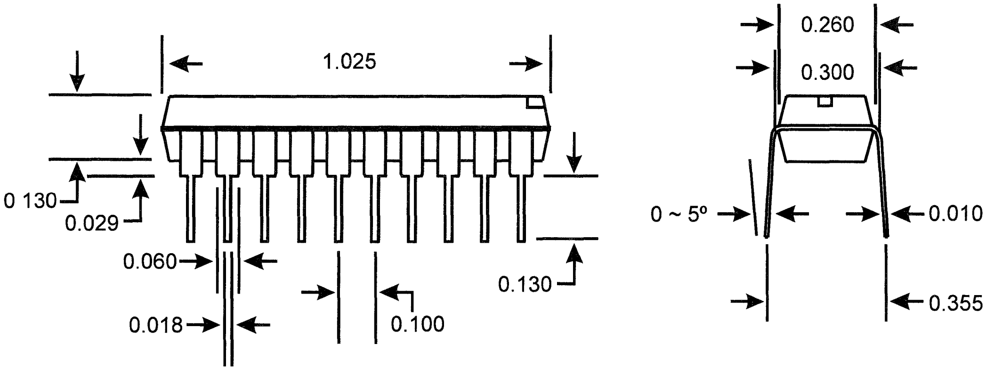
14-Pin DIP Package

See individual data sheets for more specific ordering information.

DIP Packages



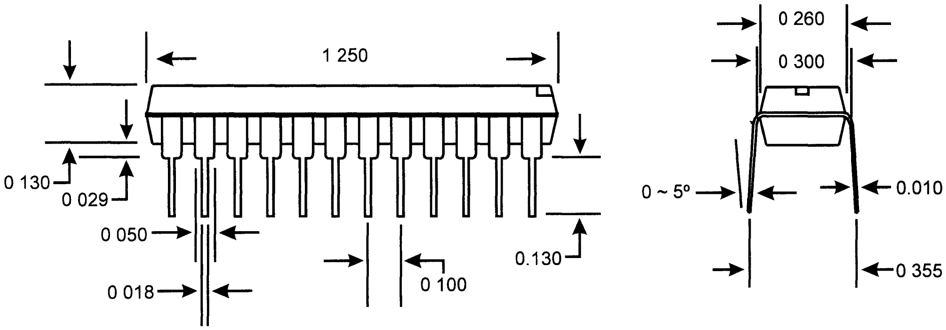
16-Pin DIP Package



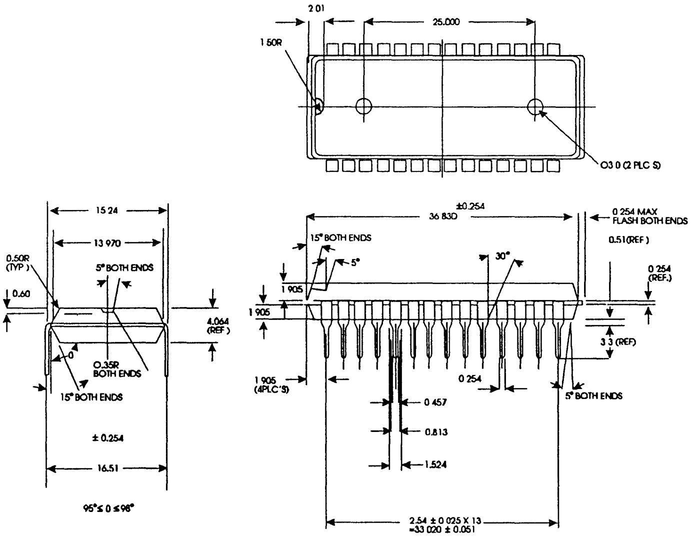
20-Pin DIP Package

See individual data sheets for more specific ordering information.

DIP Packages



24-Pin DIP Package

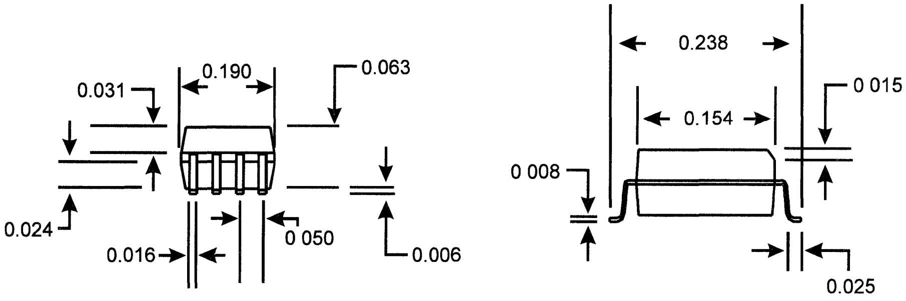


Dimensions in millimeters

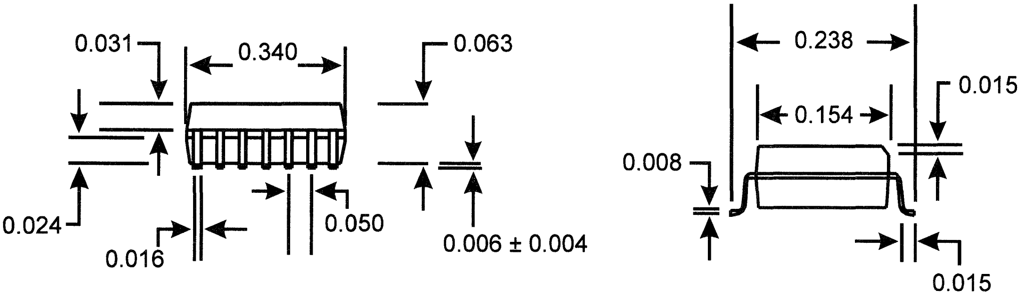
28-Pin DIP Package

See individual data sheets for more specific ordering information.

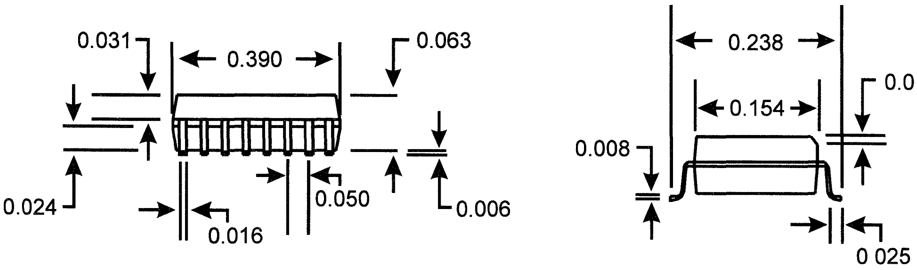
SOIC Packages



8-Pin SOIC Package



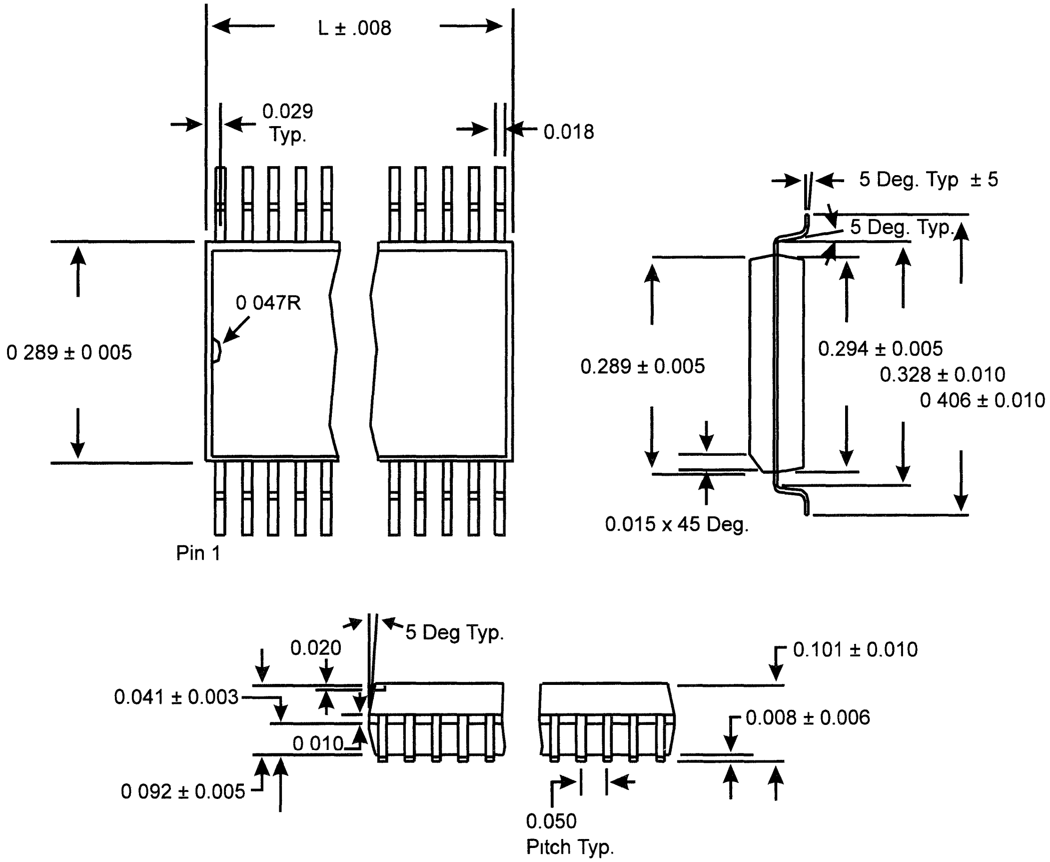
14-Pin SOIC Package



16-Pin SOIC Package

See individual data sheets for more specific ordering information.

SOIC Packages

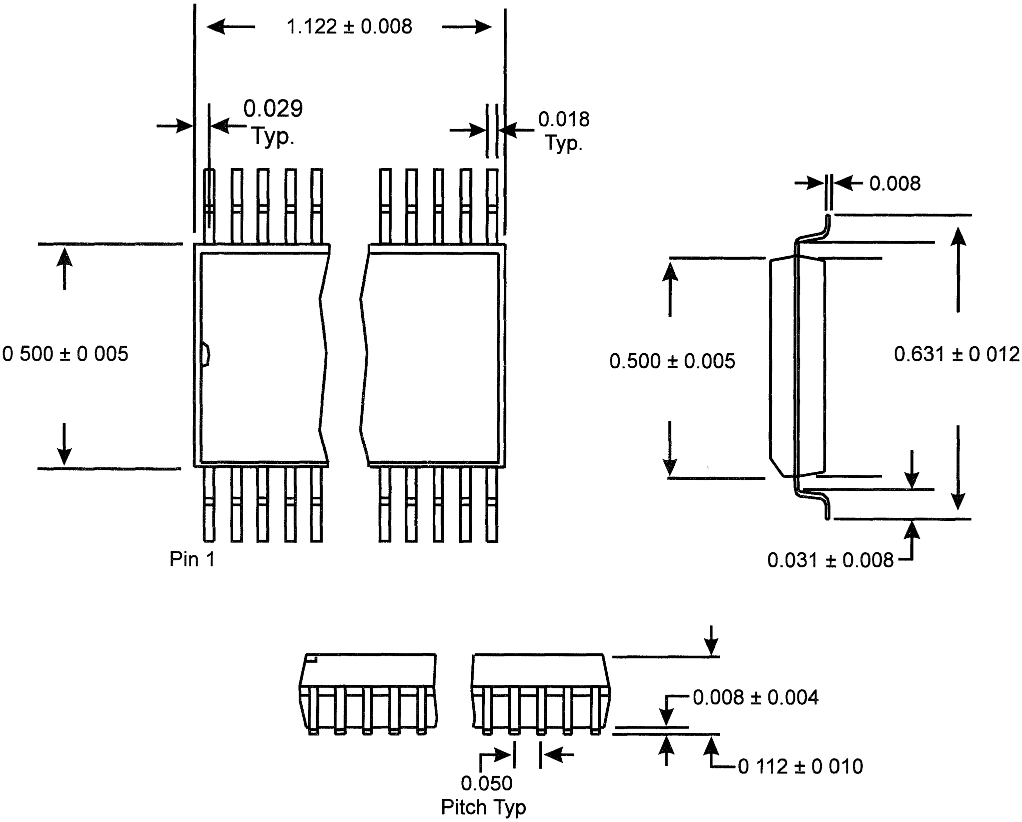


SOIC Package (wide body)

LEAD COUNT	14L	16L	18L	20L	24L	28L	32L
DIMENSION L	0.354	0.404	0.454	0.504	0.604	0.704	0.804

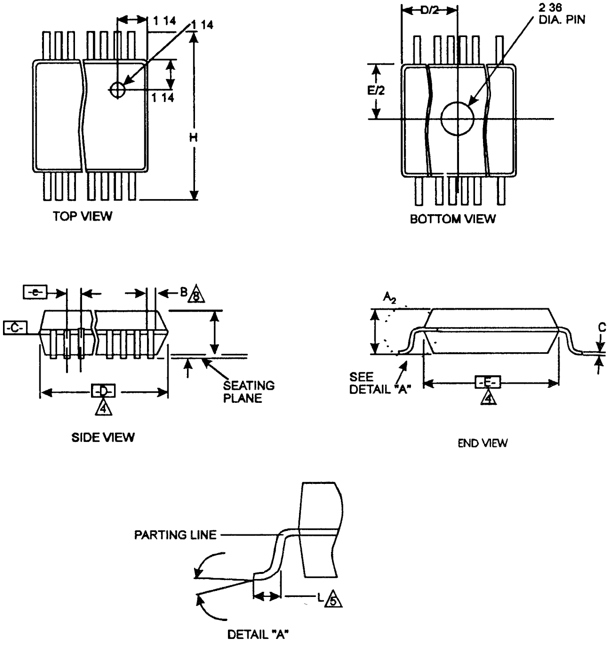
See individual data sheets for more specific ordering information.

SOP Package



SOP Package

See individual data sheets for more specific ordering information.



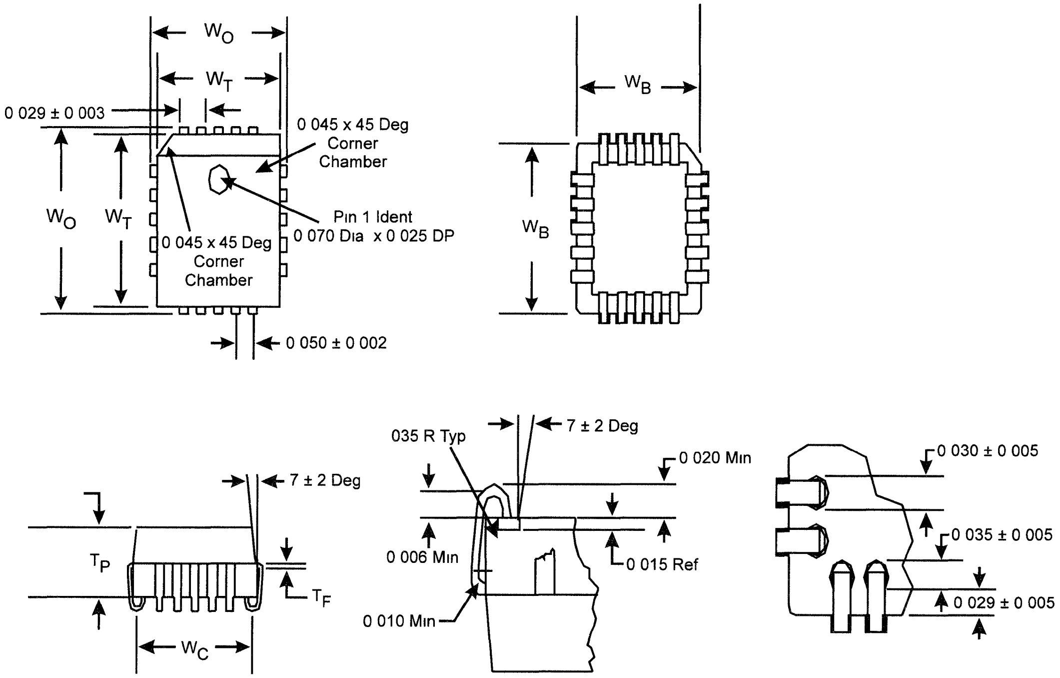
SSOP Package

SYMBOL	COMMON DIMENSIONS				NOTE	4			6
						D			N
	MIN.	NOM.	MAX.	NOTE	VARIATIONS	MIN.	NOM.	MAX.	
A	0.68	0.73	0.78		AA	0.239	0.244	0.249	14
A1	0.002	0.005	0.008		AB	0.239	0.244	0.249	16
A2	0.066	0.068	0.070		AC	0.278	0.284	0.289	20
B	0.010	0.012	0.015		AD	0.318	0.323	0.328	24
C	0.005	0.006	0.008		AE	0.397	0.402	0.407	28
D	See Variations			4	AF	0.397	0.402	0.407	30
E	0.205	0.209	0.212	4					
e		0.026 BSC							
H	0.301	0.307	0.311						
L	0.022	0.030	0.037	5					
N	See Variations			6					
∝	0°	4°	8°						

This table in inches.

See individual data sheets for more specific ordering information.

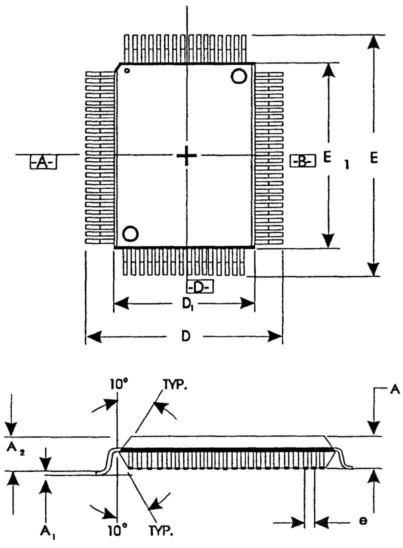
PLCC Packages

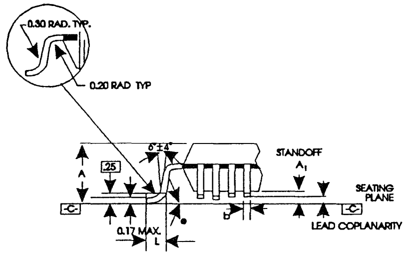


PLCC Package

LEAD COUNT	FRAME THICKNESS T_F ±.0003	PKG. THICKNESS T_P ±.004	PKG. WIDTH TOP W_T ±.004	PKG. WIDTH BOTTOM W_B ±.066	OVERALL PKG. WIDTH W_O ±-.005	CONTACT WIDTH W_O ±.010/-.030
20L	0.010	0.152	0.350	0.323	0.390	0.320
28L	0.010	0.152	0.450	0.423	0.490	0.420
44L	0.010	0.152	0.650	0.623	0.690	0.620
52L	0.010	0.152	0.750	0.723	0.790	0.720
68L	0.008	0.150	0.950	0.923	0.990	0.920
84L	0.008	0.150	1.160	1.123	1.190	1.120

See individual data sheets for more specific ordering information.



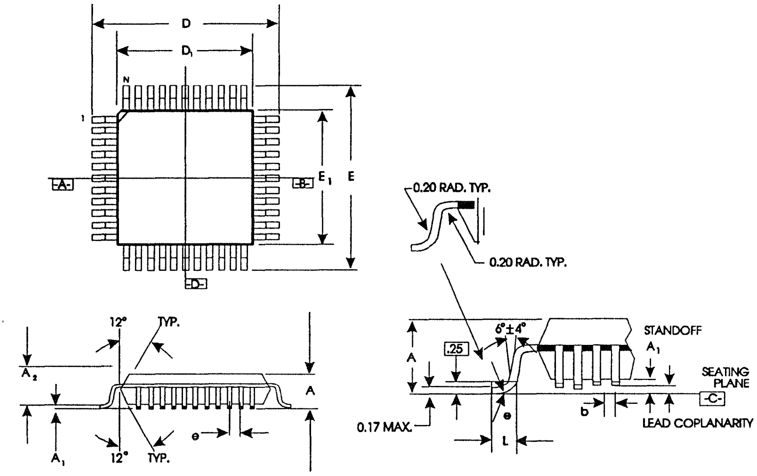


QFP Package

LEAD COUNT		44L	64L	80L	100L	64L	80L	100L
BODY THICKNESS		2.0				2.70		
FOOTPRINT (BODY+)		3.20						
DIMENSIONS	TOLERANCE							
A	MAX.	2.35	2.45			3.40		
A_1		0.25 MAX.				0.25 MIN.		
A_2	±0.10	2.0				2.70		
D	±0.25	13.20	17.20					
D_1	±0.10	10.0	14.00					
E	±0.25	13.20	23.20					
E_1	±0.10	10.0	20.00					
L	±0.15/0.10	0.70	0.88					
e	BASIC	0.80	1.00	0.80	0.65	1.00	0.80	0.65
b	+0.05	0.35			0.30	0.35		0.30
ccc	MAX.	0.10						
ddd		0.20 NOM.			0.12 NOM.	0.20 NOM.		0.12 NOM.
0		0° - 7°						

See individual data sheets for more specific ordering information.

TQFP Packages



TQFP Package

LEAD COUNT		32L	
BODY THICKNESS		1.00	1.40
FOOTPRINT (BODY+)		2.00	
DIMENSIONS	TOLERANCE		
A	MAX.	1.20	1.60
A1		0.05 MIN./0.10 MAX.	
A2	±0.5	1.00	1.40
D	±0.25	9.00	
D1	±0.10	7.00	
E	±0.25	9.00	
E1	±0.10	7.00	
L	±0.15/-0.10	0.60	
e	BASIC	0.80	0.50
b	+0.05	0.35	0.22
ccc	MAX.	0.10	0.08
ddd		0.20 MAX.	0.08 MAX.
0		0° - 7°	

See individual data sheets for more specific ordering information.

ICS
Sales Offices
and
Sales Representatives

Integrated Circuit Systems, Inc.

SINCE 1976

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(Please call ICS headquarters for rep in this area.)

Washington
Advance Technical
Marketing, Inc.
8521 154th Avenue N.E.
Redmond, WA 98052
Phone: (206) 869-7636
Fax: (206) 869-9841

Wisconsin
KMA Sales
Suite 202
2433 North Mayfair Road
Milwaukee, WI 53226-1406
Phone: (414) 259-1771
Fax: (414) 259-0246

Wyoming
Waugaman Associates, Inc.
Suite 101
11445 W. I-70 Frontage Rd. North
Wheat Ridge, CO 80033-2101
Phone: (303) 423-1020
Fax: (303) 467-3095

Integrated Circuit Systems, Inc.

ICS Sales Offices

Eastern & Central Area
Headquarters
Integrated Circuit Systems, Inc.
2435 Boulevard of the Generals, P.O. Box 968
Valley Forge, PA 19482-0968
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Fax: (610) 630-5399
Toll-Free: 1-800-220-3366

Northern Area
Integrated Circuit Systems, Inc.
Suite 30
8330 Madison Street
Burr Ridge, IL 60521
Phone: (708) 323-1397
Fax: (708) 323-0741

Western Area
Integrated Circuit Systems, Inc.
1271 Parkmoor Avenue
San Jose, CA 95126
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Fax: (408) 925-9460

International ICS Sales Representatives

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(Please call ICS Headquarters for the rep in this area.)

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ACAL Auriema
Lozenberg 4
B-1932 Zaventem
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Fax: (32) 2 725 10 14

Canada
(Alberta and British Columbia only)
Advance Technical
Marketing, Inc.
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Redmond, WA 98052
Phone: (206) 869-7636
Fax: (206) 869-9841

(Eastern)
Dynasty Components
#110-1140 Morrison Dr.
Ottawa, Ontario K2H 8S9
Phone: (613) 596-9800
Fax: (613) 596-9886

Denmark
E.V. Johanssen Elektronik A/S
Titangade 15
DK-2200 Copenhagen N
Phone: (45) 31 83 90 22
Fax: (45) 31 83 92 22

Send Components only
ACTE Lagerhotel
Vallensbækvej 41
DK-2605 Broendby
Denmark

Finland
IE Oy AB
Turkhaudantie 1
SF-00700 Helsinki
Phone: (358) 0-351 3133
Fax: (358) 0-351 3134

France
Tekelec Airtronic
5, Rue Carle Vernet
92315 Sevres Cedex
Phone: (33) 1 46 23 24 25
Fax: (33) 1 45 07 21 91

Germany
Scantec GmbH
Behringstrasse 10
D-82152 Planegg
Phone: (49) 89 8 99 14 30
Fax: (49) 89 8 57 65 74

Scantec GmbH
Armbruststrasse 26
73230 Kirchheim/Teck
Phone: (49) 7021 979321
Fax: (49) 7021 979262

Germany *(continued)*
Topas Electronic GmbH
Striehlstrasse 18
30159 Hannover
Phone: (49) 51 1 13 12 17
Fax: (49) 51 1 13 12 16

Topas Electronic GmbH
Max-Weber Strasse 16
25451 Quickborn
Phone: (49) 41 06 73097
Fax: (49) 41 06 73378

Hong Kong
RTI Industries Co., Ltd.
Room 402
Nan Fung Commercial Centre
No. 19, Lam Lok Street
Kowloon Bay, Kowloon,
Hong Kong
Phone: (852) 2795-7421
Fax: (852) 2795-7839

Electrocon Products Ltd.
8/F, Blk. B,
Prosperity Centre
77 Container Port Road
Kwai Chung, N.T.,
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Phone: (852) 2481-6022
Fax: (852) 2480-3967

Israel
ELDIS Technologies Ltd.
4 Hess Street
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Fax: (972) 9 562642

Italy
Sitel S.P.A.
Via Po, 37
20031 Cesano Maderno
Milan
Phone: (39) 362 524941
Fax: (39) 362 501516

Comprel S.P.A.
Via Po, 37
20031 Cesano Maderno
Milan
Phone: (39) 362 553 991
Fax: (39) 362 553 967
(Distribution Office)

Japan
Micro Summit K.K.
Premier Ki Building, 4F
1, Kanda Mikura-cho
Chiyoda-ku, Tokyo 101
Phone: (81) 3 3258-5531
Fax: (81) 3 3258-0433

Nichimen Elect.Comp. Corp.
Yokobori Kurisu Bldg. 2F,
8-5, Koraibashi 4-Chome,
Chuo-ku, Osaka 541
Phone: (81) 6 226-0015
Fax: (81) 6 226-0016

Rymex
Suite 201
1333 Lawrence Expressway
Santa Clara, CA 95051
Phone: (408) 296-6626
Fax: (408) 296-2063

Korea
Acetronix
Parklim Bldg., #402
Seobingko-Dong 95
Yongsan-Ku, Seoul
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Fax: (47) 63 87 90 00

Puerto Rico
Semtronic Associates
Suite 816
Mercantil Plaza Building
Hato Rey, Puerto Rico 00918
Phone: (809) 766-0700
Fax: (809) 763-8071

Singapore
Scan Technology Pte. Ltd.
50 Kallang Bahru
#04-01/03
Kallang Industrial Estate
Singapore 1233
Phone: (65) 294-2112
Fax: (65) 296-1685

Scan Components (M)SDN BHD
761-B Jalan Sultan Azlan Shah
Sungai Nibong, 11900 Penang
Malaysia
Phone: (60) 4-6435136
Fax: (60) 4-6436320

Sweden
IE Komponenter AB
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S-16111 Bromma
Phone: (468) 80 46 85
Fax: (468) 26 22 86

Taiwan
Maxtek Technology Co. Ltd.
3F, No. 197
Section 4, Nanking E. Road
Taipei, Taiwan ROC
Phone: (886) 2 713-0209
Fax: (886) 2 712-6780

Princeton Technology Corp.
2F, No. 233-1
Bao Chiao Road
Hsin Tien, Taipei Hsien
Taiwan, ROC
Phone: (886) 2 917-8856
Fax: (886) 2 917-3836

United Kingdom
Amega Technology
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Roentgen Road,
Daneshill East,
Basingstoke,
Hants, RG24 ONG
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** Country & city codes listed apply to U.S. residents only. International calls placed outside of the U.S. should check with local telephone service for correct codes.

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Fax: (716) 292-0750

Alabama
Nu Horizons
Suite 11
4801 University Square
Huntsville, AL 35816
Phone: (205) 722-9330
Fax: (205) 722-9348

California
Nu Horizons
2070 Ringwood Avenue
San Jose, CA 95131
Phone: (408) 434-0800
Fax: (408) 434-0935

Nu Horizons
Suite 123
13700 Alton Parkway
Irvine, CA 92718
Phone: (714) 470-1011
Fax: (714) 470-1104

Florida
(North)
Nu Horizons
Suite 270
600 S. North Lake Blvd.
Altamonte Springs, FL 32701
Phone: (407) 831-8008
Fax: (407) 831-8862

Nu Horizons
3421 N.W. 55th Street
Ft. Lauderdale, FL 33309
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Fax: (305) 735-2880

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Nu Horizons
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Norcross, GA 30093
Phone: (404) 416-8666
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Columbia, MD 21046
Phone: (410) 995-6330
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Nu Horizons
19 Corporate Place, Bldg. 1
107 Audubon Road
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Phone: (617) 246-4442
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Nu Horizons
6955 Washington Ave., South
Edina, MN 55439
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Pine Brook, NJ 07058
Phone: (201) 882-8300
Fax: (201) 882-8398

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Nu Horizons
Suite A-15
6200 SOM Center Road
Solon, OH 44139
Phone: (216) 349-2008
Fax: (216) 349-2080

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18000 Horizon Way
Mt. Laurel, NJ 08054
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Phone: (609) 231-0900 (NJ)
Fax: (609) 231-9510

Texas
Nu Horizons
2081 Hutton Dr., Suite 119
Carrollton, TX 75006
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Revised: 05/01/95

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