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M48-013
UNIVERSAL LOGIC INTERFACE
INSTRUCTION MANUAL

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M48-013
UNIVERSAL LOGIC INTERFACE INFORMATION SPECIFICATION

1. INTRODUCTION

This manual describes the installation, maintenance, programming and application information for the 02-304 Universal Logic Interface. The Universal Logic Interface provides the customer with the ability to interface a custom device into an INTERDATA system. The Universal Logic Interface (ULI) consists of two sections. One half of the ULI is a general purpose interface to the INTERDATA Multiplexor Bus or Selector Channel I/O Bus. The general purpose interface allows data transfer in the byte or halfword modes. The remaining half of the ULI allows the customer to build a custom device controller via wire wrapped Integrated Circuit (I.C.) and component connections.

2. PHYSICAL DESCRIPTIONS

The Universal Logic Interface (ULI) requires one circuit board slot position in an INTERDATA 15 inch chassis. The board measures 15 inches square and is composed of two sections. One half of the board is a general purpose interface to the INTERDATA Multiplexor Bus or Selector Channel I/O Bus. The other half of the board is a general purpose wire wrap component section. This section of the board contains 77 fields. Each field may contain one Integrated Circuit Module or up to eight axial lead discrete components (resistors, capacitors, and diodes).

Either 14 or 16 pin Dual In Line Packaged (DIP) I.C.s can be accomodated. The I.C.s are usually soldered directly into their designated field locations. If removable or interchangable I.C.s are desired, commercially available I.C. Sockets, with 300 mil. mounting centers can be soldered into the I.C. field positions by the user.

The circuit board contains 25 mil. square wire wrap posts which correspond directly to the I.C. pins, discrete component leads, and cable connections. All interconnections between components and the connectors are made by wire wrapping to the 25 mil. square wire wrap posts. See Figure 1.

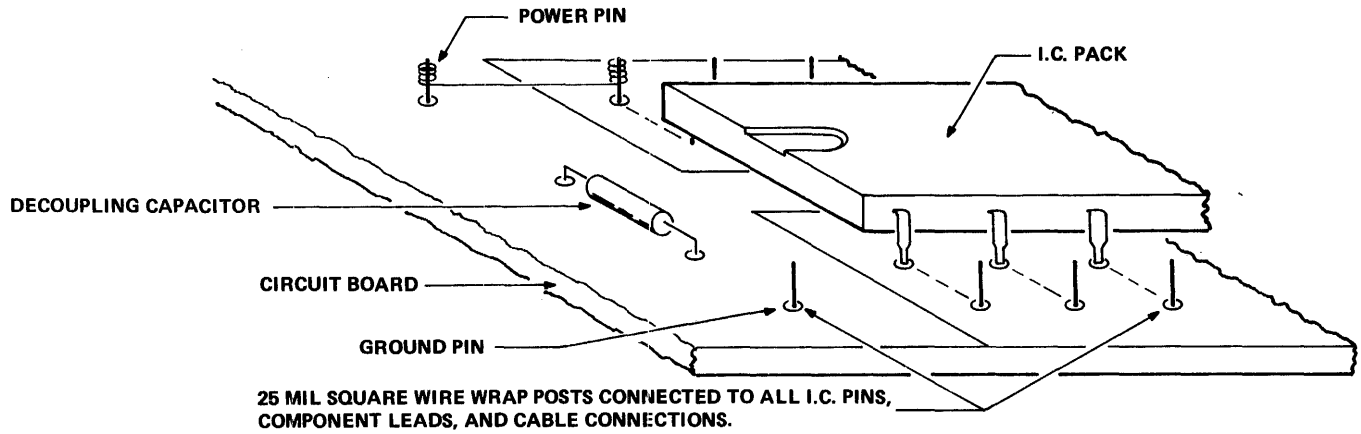


Figure 1. Wire Wrap Pins/IC or Components Leads Connection

3. DEVICE CONTROLLER LOGIC DESIGN

This section describes the procedures to follow in designing device controllers which connect to the Multiplexor Bus or Selector Channel I/O Bus. While it is impossible to describe all possible controllers, this section explains representative circuits in sufficient detail to permit design of most controllers.

NOTE:

Figures 2 through 5 are example logic. These figures are not the actual logic of the ULI.

3.1 Multiplexor Bus

The Multiplexor Bus or Selector Channel I/O Bus is a byte or halfword oriented I/O system which communicates with up to 255 peripheral devices. The Multiplexor Bus consists of 30 lines; 16 bi-directional Data Lines, 8 Control Lines, 5 Test Lines, and an Initialize Line.

All busses are false type, i.e. low level is active, high level is inactive. The device controller circuits used to communicate with the Multiplexor Bus are shown in Figure 2.

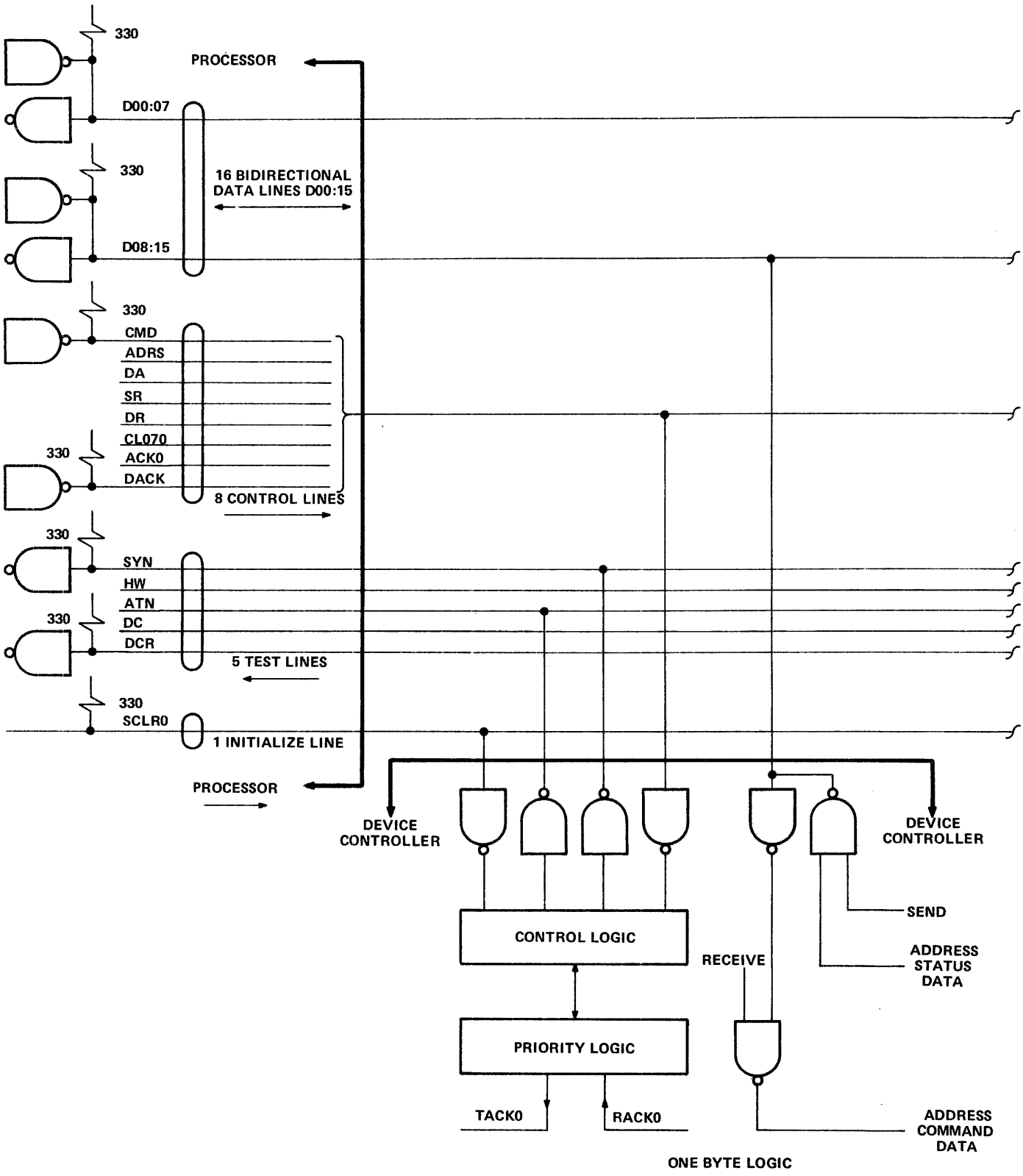


Figure 2. Processor/Device Controller Logic Interface (Sheet 1 of 2)

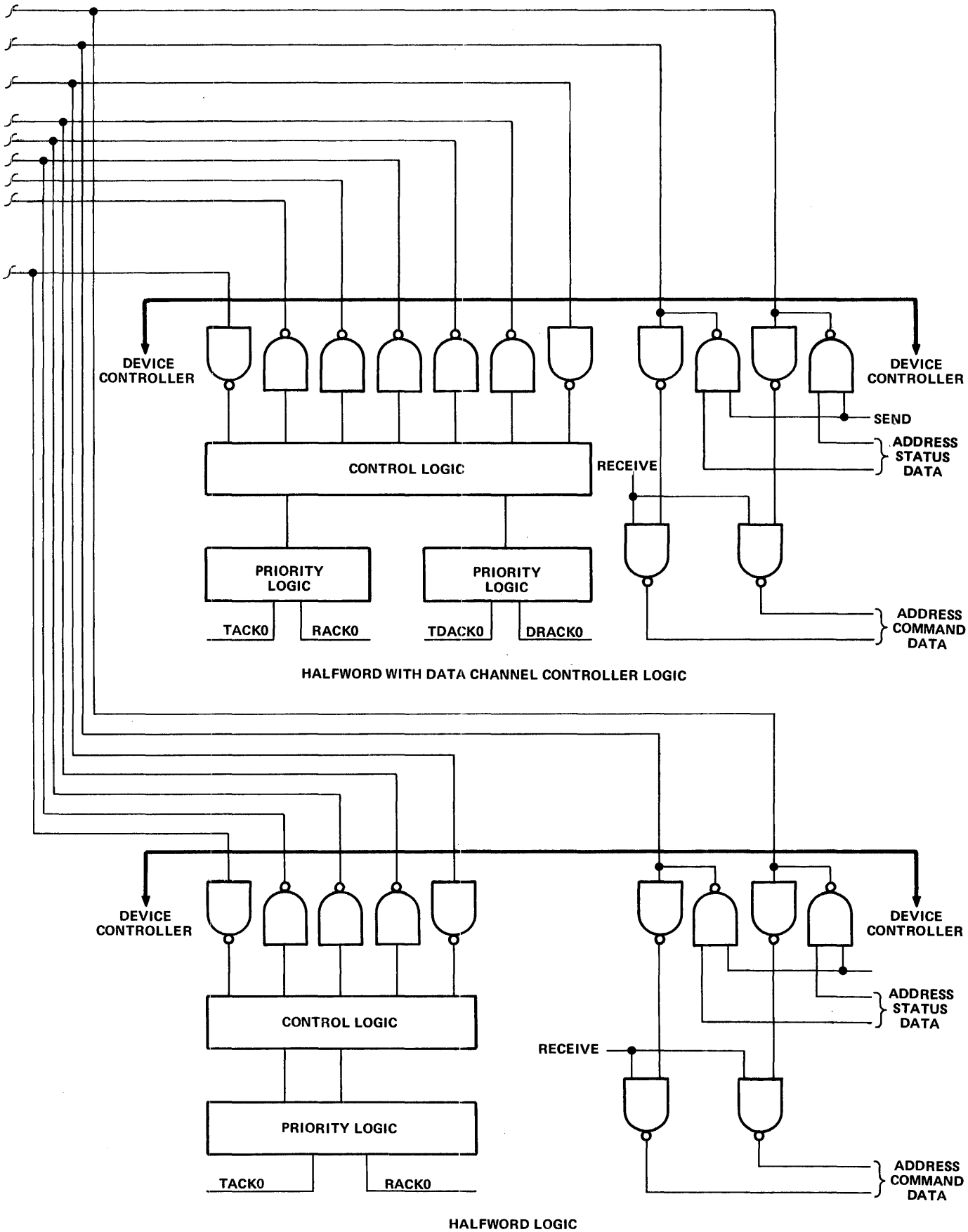


Figure 2. Processor/Device Controller Logic Interface (Sheet 2 of 2)

In a typical case, a device controller will receive an 8-bit Address Byte, an 8-bit Command Byte, and either an 8-bit data byte or a 16-bit data halfword from the Processor over the 16 bi-directional Data Lines (D00:15). Likewise, a device controller will send an 8-bit Address Byte, an 8-bit Status Byte, and either an 8-bit data byte or a 16-bit data halfword to the Processor over the 16 bi-directional Data Lines (D00:15). When only a byte of data is transferred, that byte is passed over the lower eight Data Lines (D08:15).

3.2 Device Controller Addressing

Refer to Figure 3. during the following description. The dotted lines around the groups of logic functions represent INTERDATA standard logic. When a device controller is addressed, the 8-bit address code is placed on the Data Lines (D080 through D150). The two buffers provide the true and false data lines. The Address Decoder circuit is hard-wired on each controller with its assigned address code, and the eight coded outputs are applied to an eight input gate. Thus, the Decoded Device output (DD1) goes true. The Address control line (ADRS1) then strobes the DD1 line into the ADRS flip-flop.

The Synchronize (SYN) signal is returned to the Processor, during the presence of ADRS1, via the Address Sync line, (ADSY0). Notice that an OR gate is used here for returning the other device Command Sync lines. The set output from the Address flip-flop, called Device Enable (DENB1), is used to gate all other I/O control lines to the device controller. When another device is addressed, the Decoded Device line (DD1) is low, causing the ADRS1 strobe line to reset the Address flip-flop, disabling the controller. Thus, only one device controller may be addressed at any time. During the address cycle, only the device that was addressed returns a SYN.

3.3 Data and Status Input

3.3.1 Data. Figure 4 shows how a byte or halfword of data may be read into the Processor. When an 8-bit byte oriented device controller is addressed, DENB1 is high, enabling the Data Request (DR) control line from the Processor. The DR enables the data byte onto the eight bottom Data Lines (D080 through D150). If a 16-bit halfword oriented device controller is addressed, one data byte is enabled as described above, and a second data byte is enabled onto the eight top Data Lines (D000 through D070) by an active Halfword (HW) signal.

3.3.2 Status. Figure 3 shows how a byte of status may be read into the Processor. When the byte or halfword oriented device controller is addressed, DENB1 is high, enabling the Status Request (SR) control line from the Processor. Open collector gates are used for OR tying multiple data and status sources onto the eight Data Lines (D080 through D150).

The device controller logic should place a high on BSY1 until the data is ready. The Processor may now be synchronized to the device data rate by testing the device status until the Busy bit is low. Then, when the Busy bit is low, the program may transfer data. Device synchronization can also be achieved by generating an interrupt when the data is ready and BSY1 has reset.

The End of Medium (EOM) bit is normally placed high at the termination of the device medium, such as End of Card. The Device Unavailable (DU) bit typically signifies that device power is not turned on.

The Examine Status (EX) bit is used to signify other appropriate device conditions. In this case, the user assigns S01 through S31 to appropriate conditions, such as Parity Error, etc.

It is appropriate to note here that the Busy Status is unconditionally defined such that data cannot be transferred unless Busy is false. The remaining status bits are defined as required by the device controller. Not all device controllers require all eight status bits.

Device controllers are designed such that the Processor or the Selector Channel maintains the Status Request line once the current status of the device is presented. Specifically, if the status changes while the Status Request line is true, the status byte returned to the Processor or Selector Channel should also change.

3.4 Data and Command Output

3.4.1 Data. Figure 5 shows how a data byte may be output from the Processor. The buffered true and false Data Lines (D081 through D151 and D080 through D150) from Figure 3 connect to the set and reset inputs of the Data Register.

When the device is addressed, DENB1 is high, enabling the control line DAG1 to strobe the data condition into the J-K flip-flop Data Register. The DASY0 line also returns the SYN signal to the Processor.

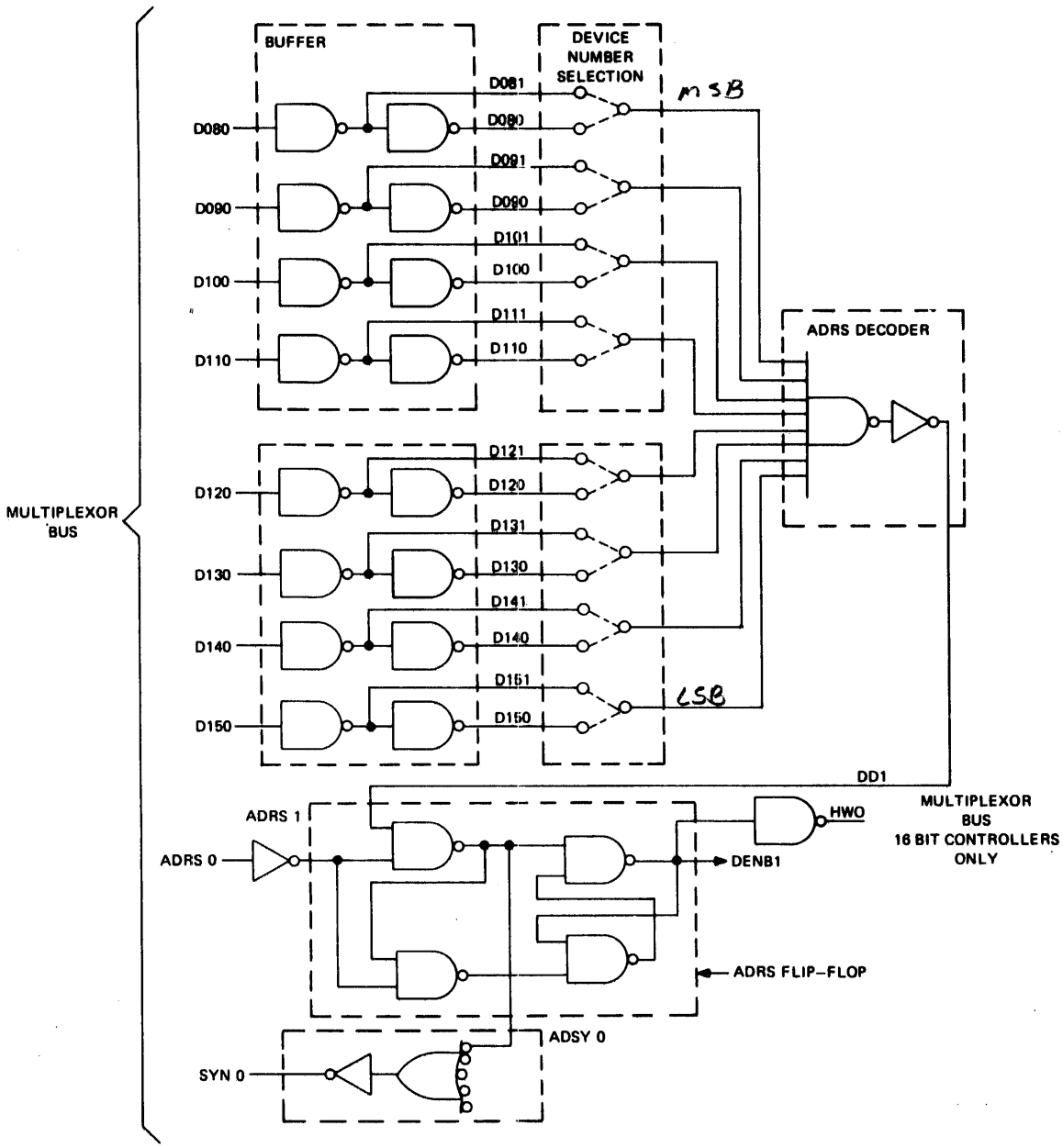


Figure 3. Device Addressing, Logic Diagram

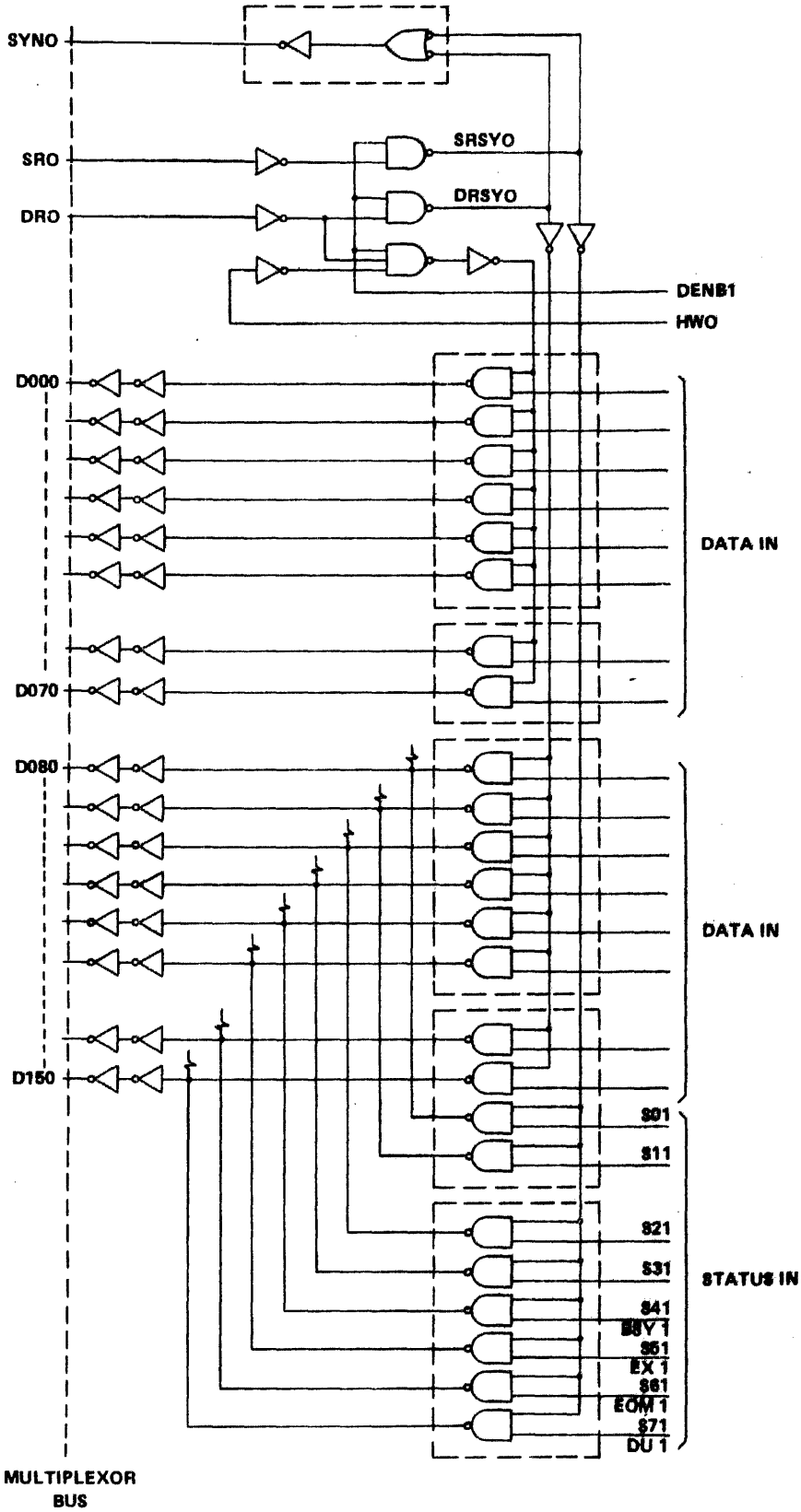


Figure 4. Data and Status Input Logic Diagram

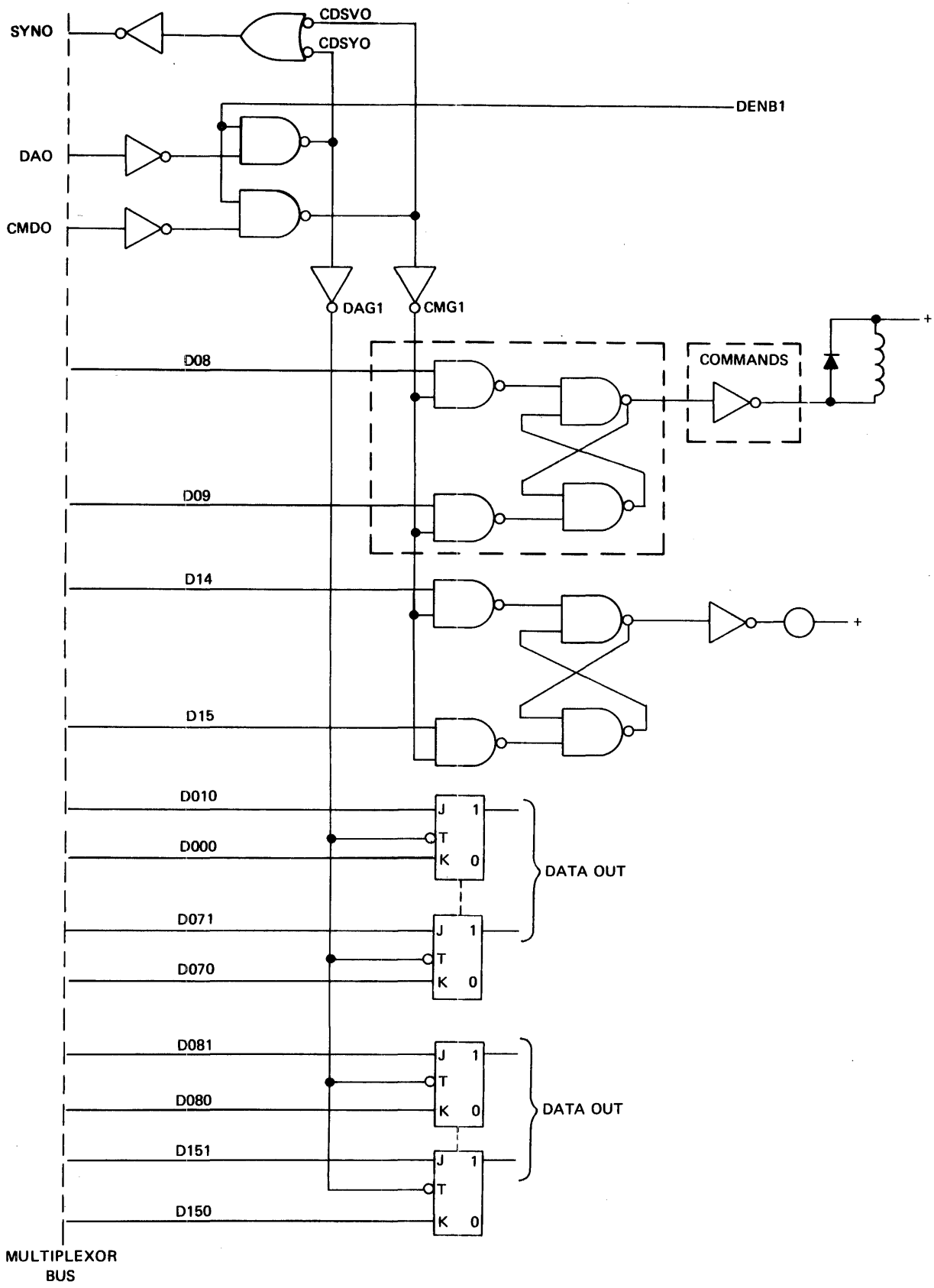


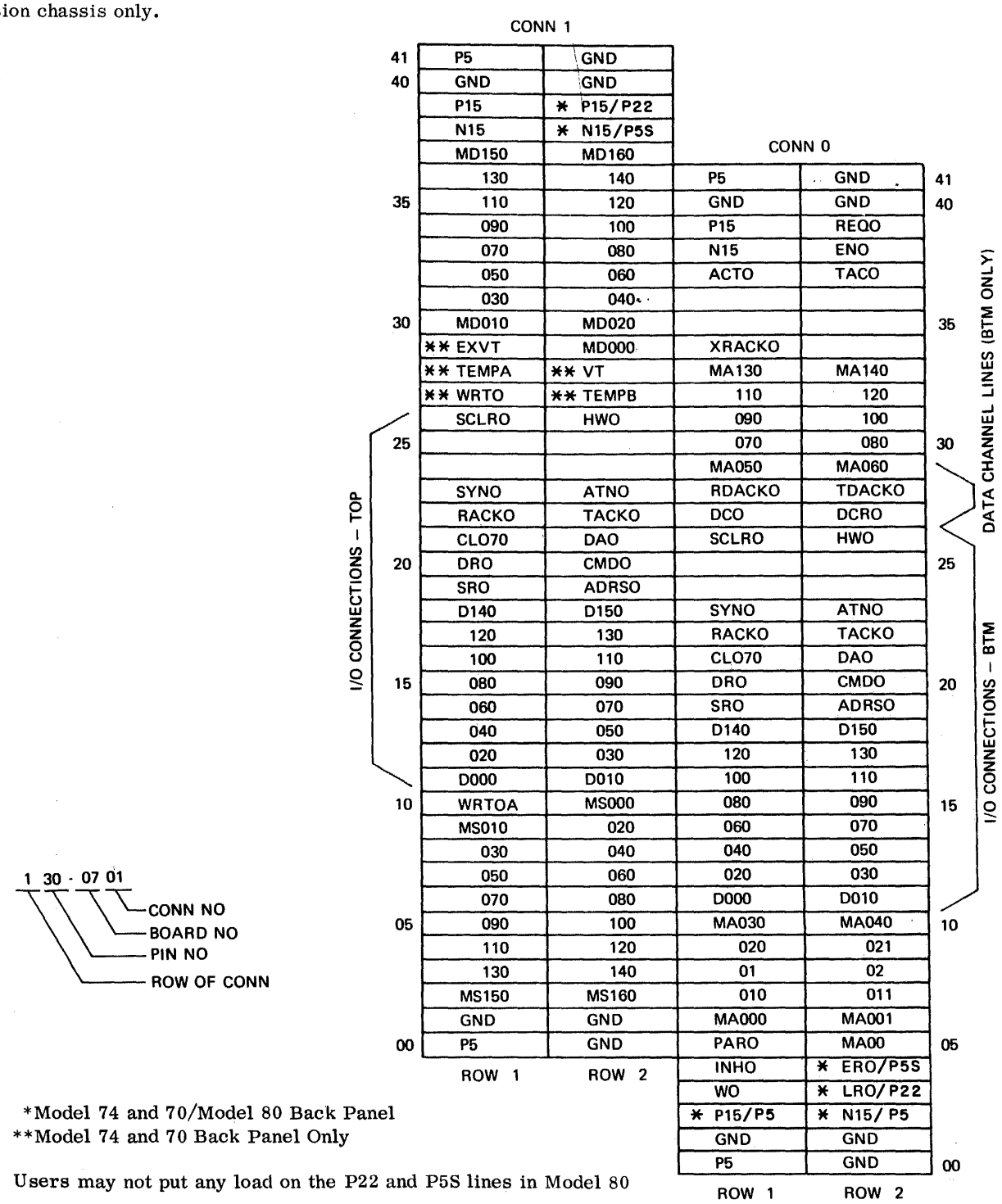
Figure 5. Data and Comrnand Output, Logic Diagram

3.4.2 Command. The command lines are shown on Figure 5 as being used in the toggle mode. For example, a high on Bit 8 (D081) sets a control relay when CMG1 goes high. A high on Bit 9 (D091) resets the relay. Bits 14 and 15 are shown operating an indicator. Other pairs of bits may be used to enable/disable interrupts, etc.

Again, note that definition of the command bits is a function of the device controller only. Not all device controllers require eight separate commands.

3.5 Multiplexor Bus Wiring

Wiring for the Multiplexor Bus and for the Selector Channel Bus is identical in the Processor and expansion chassis. Each card position contains two connectors with the Multiplexor and Memory Busses wired to each at pin positions indicated in Figure 6. The Memory Bus may be accessed at the back panels of the Processor chassis and the first expansion chassis only.



	CONN 1 ROW 1	CONN 1 ROW 2	CONN 0 ROW 1	CONN 0 ROW 2	
41	P5	GND	P5	GND	41
40	GND	GND	GND	GND	40
	P15	* P15/P22	P15	REQO	
	N15	* N15/P5S	N15	ENO	
	MD150	MD160	ACTO	TACO	
	130	140			
35	110	120			35
	090	100	XRACKO		
	070	080	MA130	MA140	
	050	060	110	120	
	030	040	090	100	
30	MD010	MD020	070	080	30
	** EXVT	MD000	MA050	MA060	
	** TEMPA	** VT	RDACKO	TDACKO	
	** WRTO	** TEMPB	DCO	DCRO	
	SCLRO	HWO	SCLRO	HWO	
25					25
	SYNO	ATNO	SYNO	ATNO	
	RACKO	TACKO	RACKO	TACKO	
	CLO70	DAO	CLO70	DAO	
20	DRO	CMDO	DRO	CMDO	20
	SRO	ADRSO	SRO	ADRSO	
	D140	D150	D140	D150	
	120	130	120	130	
	100	110	100	110	
15	080	090	080	090	15
	060	070	060	070	
	040	050	040	050	
	020	030	020	030	
	D000	D010	D000	D010	
10	WRTOA	MS000	MA030	MA040	10
	MS010	020	020	021	
	030	040	01	02	
	050	060	010	011	
	070	080	MA000	MA001	
05	090	100	PARO	MA00	05
	110	120	INHO	* ERO/P5S	
	130	140	WO	* LRO/P22	
	MS150	MS160	* P15/P5	* N15/P5	
	GND	GND	GND	GND	
00	P5	GND	P5	GND	00

*Model 74 and 70/Model 80 Back Panel
**Model 74 and 70 Back Panel Only

Users may not put any load on the P22 and P5S lines in Model 80

Figure 6. Typical Universal Expansion Slot Wiring

3.6 Multiplexor Channel Timing

Both the Input and Output operations on the Multiplexor Channel make use of request/response signaling. This allows the system to run at its maximum speed whenever possible, but permits a graceful slowdown if the characteristics of a particular device controller require signals of longer duration. Device controller designs should keep Multiplexor Channel usage as fast as possible, consistent with practical circuit margins. Doing this assures the fastest computer input/output operation when a system is configured with a number of peripheral devices.

Timing for typical Input/Output operations is shown in Figure 7. On the Output operation, the Processor places a signal on the data lines followed by an appropriate control line signal. This stagger (T1) will vary, but it is guaranteed to be at least 100 nanoseconds. When the device controller has received the Output Byte, the SYN signal is returned to the Processor, which terminates the control line signal. Realizing that T5 is a 100 nanosecond minimum, the SYN delay T2 should be only long enough to guarantee proper reception of the Output Byte. The control line/data line removal time (T3) is important where single-rail to double-rail operation is used; e.g., the ADRS flip-flop on Figure 2. A minimum of 100 nanoseconds is guaranteed for T3. For SYN generation as per Figure 3 the control line signal is DC coupled through the gates to form the SYN signal.

It should be emphasized that the times shown on Figure 7 are defined for signals on the Multiplexor Channel. Within a given controller, one signal may flow through more gates than another signal and these delays must be considered.

For the Input operation, the Processor places a signal on a control line. The currently addressed device controller should gate signals to the data lines as soon as possible to keep T1 at a minimum. The SYN delay (T2) must guarantee that the Input Byte is on the data lines considering the slowest data gates and the fastest SYN gates. The Processor will remove the control line signal when SYN is received with a minimum delay (T4) of 100 nanoseconds. With SYN and the byte gate DC coupled to the control line, the removal delay (T3) will be the sum of the corresponding gate delays. The Processor considers the operation complete when SYN falls.

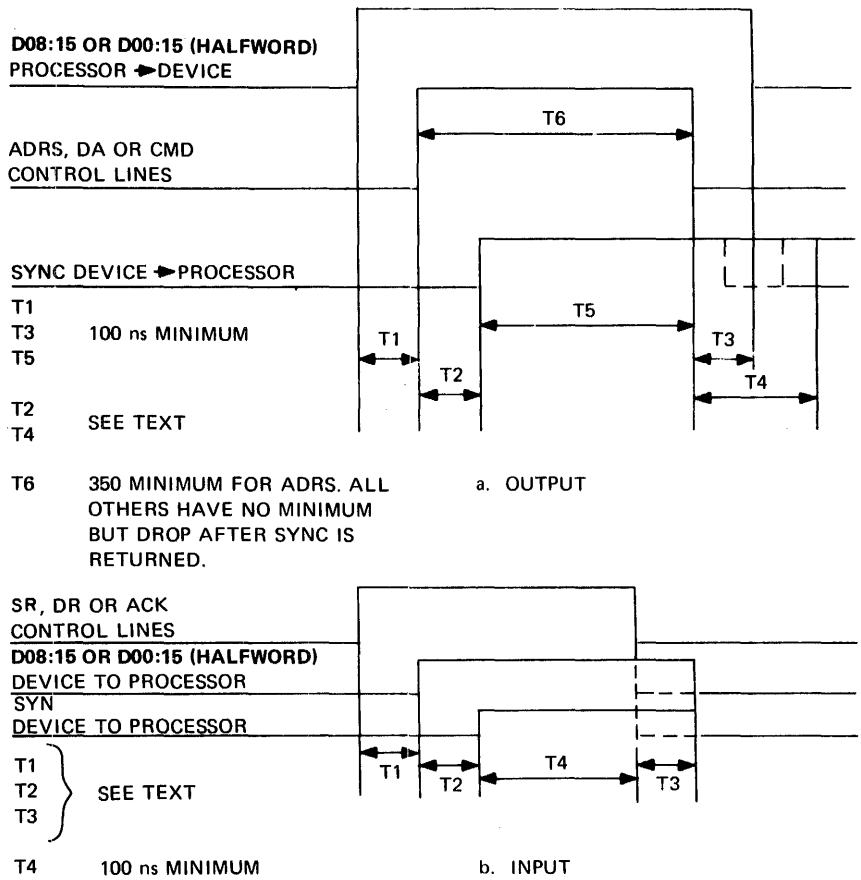


Figure 7. Multiplexor Channel Timing

4. INTERDATA NUMBERING SYSTEM FOR WIRE WRAP SECTION OF BOARD

This system is offered only as a suggested method of numbering; the user can invent his own system.

4.1 Component Field Numbering

The wire wrap section of the board is divided into 77 fields. Each field can accomodate one IC (fixed or socket) or eight discrete components. Refer to Figure 8 for IC field numbers.

Use Field 142 as an example (refer to Figure 9). The component designation takes the form A142-01R, and A142-16R where A142 is the field, 16 indicates the top pin of the component, 01 designates the bottom pin of the component, and R indicates a resistor. The IC pack pin orientation in field 133 is bottom left to right, Pins 1-8; top right to left, Pins 9-16.

An example of a power gate mounted directly on a circuit board is shown in Figure 10. Note that the pin numbers correspond directly with the actual IC pin number. Note further that the IC is located in Field A133 and the diode is in a component position of the field.

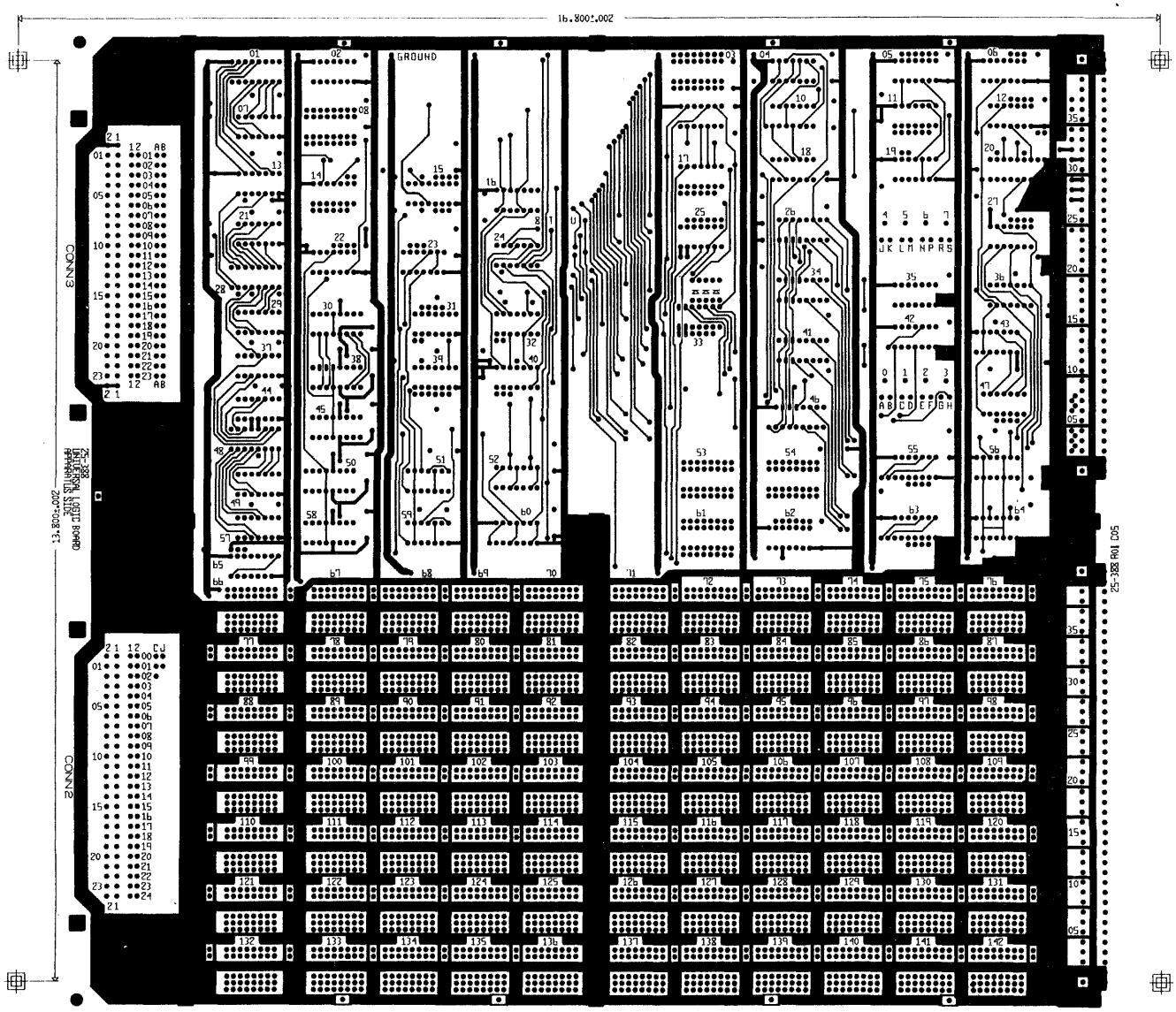


Figure 8. Universal Logic Interface

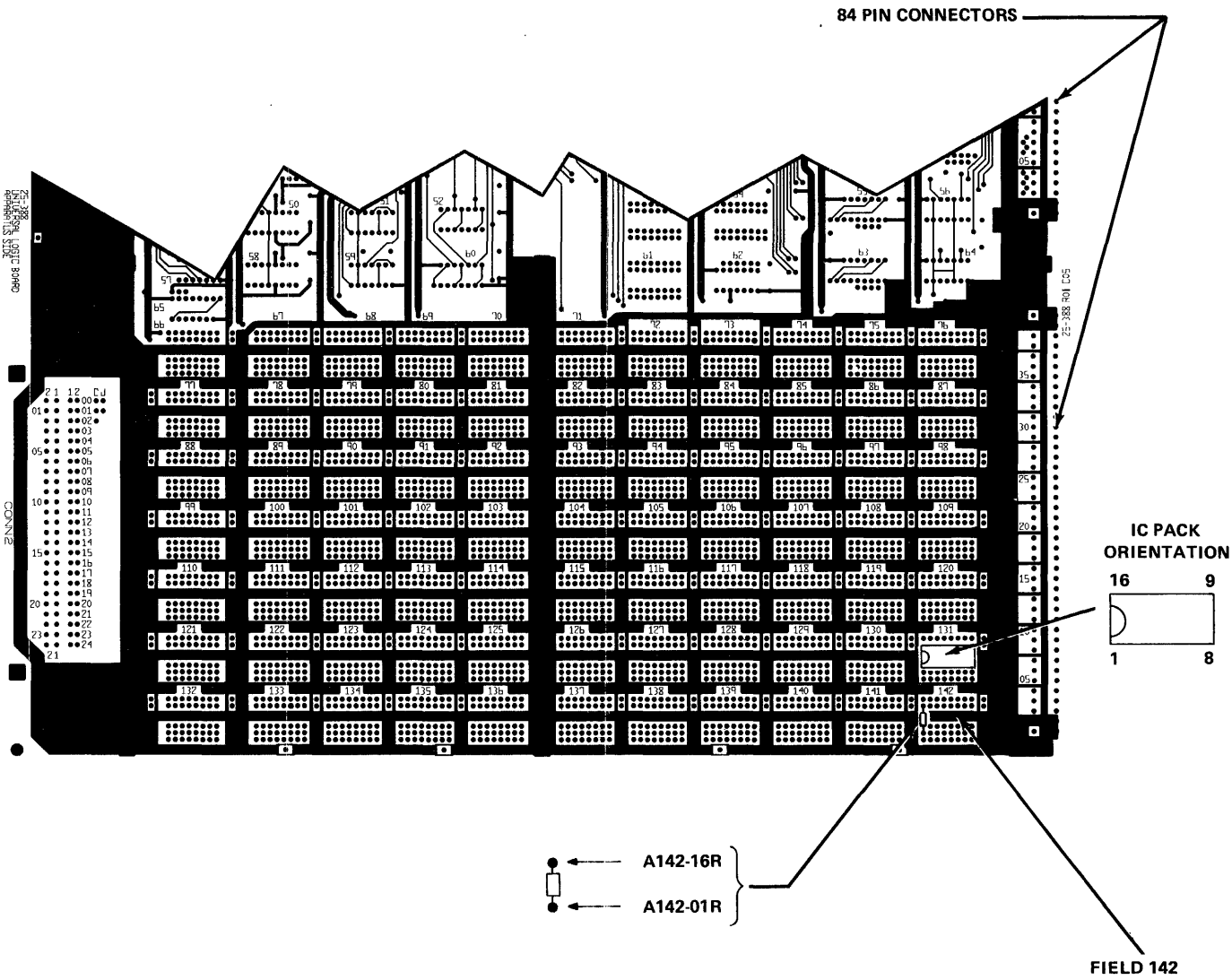


Figure 9. IC Circuit Board Numbering System

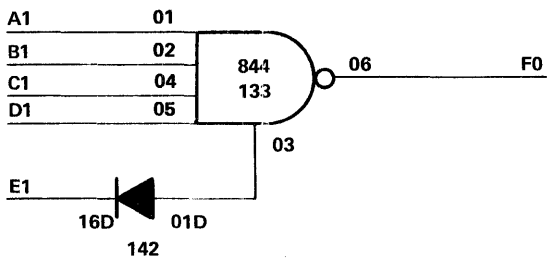


Figure 10. Example of a Power Gate

4.2 Connector Layout

Figure 11 shows the pin numbering system for the two standard 84 pin backpanel connectors, and the two standard 50 pin connectors. The fourth and fifth digits indicate the board number, 00-07. The sixth and seventh digits specify the connector field 00 (zero), or 01 (one). INTERDATA uses the symbol indicated below for a back panel connection for schematic drawings. During this description refer to Figure 12.

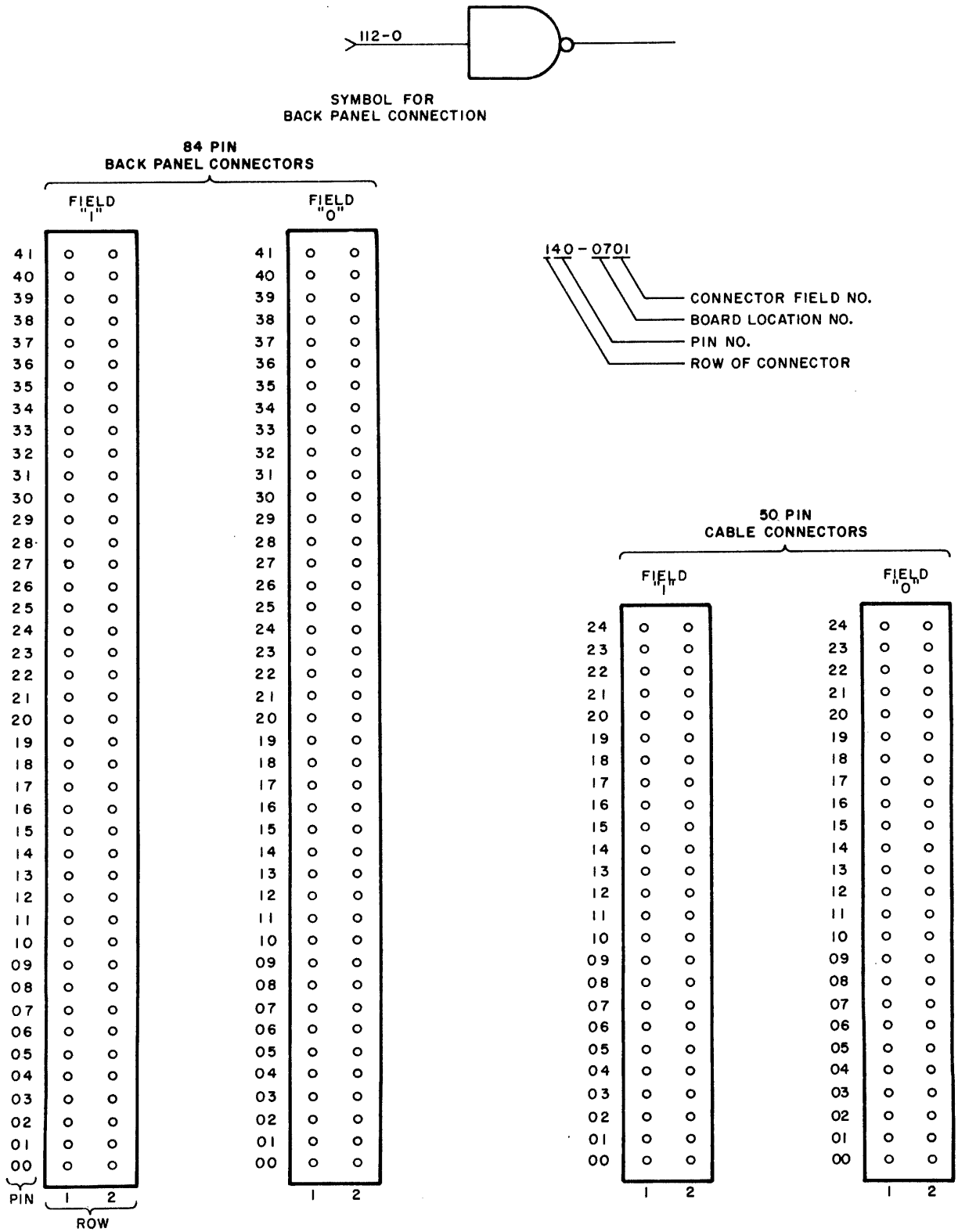


Figure 11. General Purpose Wire Wrap Board Connector Layout.

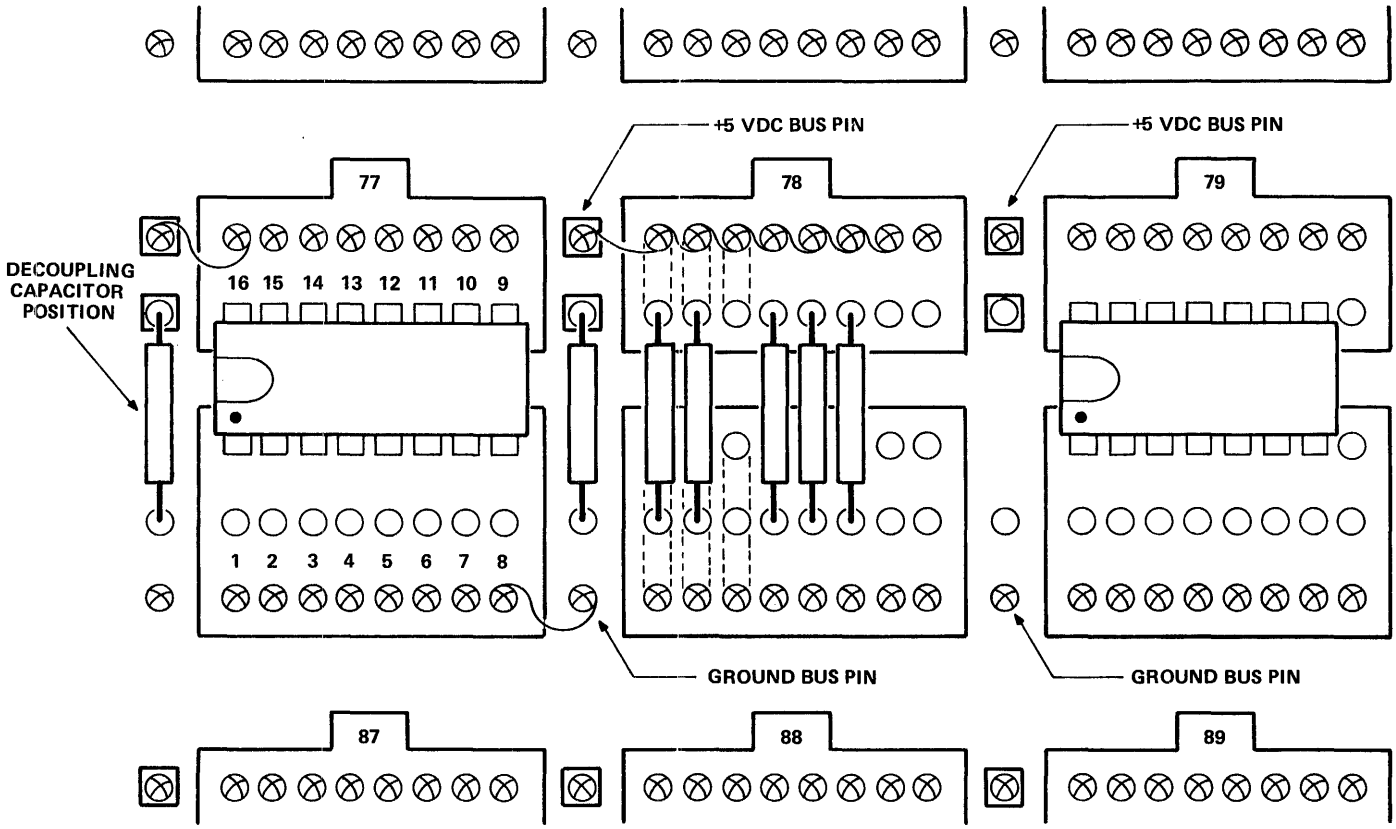


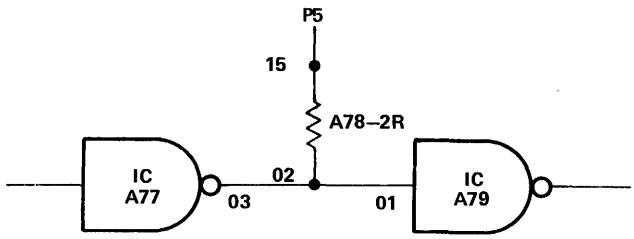
Figure 12. Example of General Purpose Wire Wrap Section

Field 77 shows a 16 pin IC installed with power and ground wired. To the left of the 16 pin IC is a decoupling capacitor. Power and ground are applied to the decoupling capacitor via the printed circuits.

Wire wrap pins may be numbered corresponding to the IC pin number. Pin one of the IC becomes wire wrap pin one.

The following is an example wire run list to wire power and ground to the 16 pin IC in field 77.

FROM	TO	NAME
A77-16	A77–PWR	+5VDC
A77–08	A77–GND	GROUND
A77–03	A78–02R	GATE 'A'
A78–02	A79–01	GATE 'A'



Field 78 shows components inserted into a field instead of an IC. When only components are in a field, all of them may be machine mounted. All decoupling capacitors may be machine mounted. The wire wrap pin notations may remain the same as for ICs.

4.3 Available Cables

The Universal Logic Interface 02-304 is supplied with a 17-185 cable assembly and a 17-200 test cable assembly. Other cables suitable for use with the ULI are:

1. Cable 17-179, a 10 foot, open ended cable with 25 twisted pair, 28 ga. stranded, and is useful for connecting to user circuits.

2. Cable 17-178, a 3 1/2 foot, 25 twisted pair, 28 ga. stranded cable, suitable for interconnecting more than one ULI.

These cables are purchased separately from the 02-304 Universal Logic Interface. The mating connector required for the two 50 pin cables is AMP 1-85972-9, or equivalent.

M48-013
UNIVERSAL LOGIC INTERFACE
INSTALLATION SPECIFICATION

1. INTRODUCTION

The Universal Logic Interface (Part Number 02-304) consists of the 35-479 Universal Logic Interface, one 17-185 cable, and a 17 - 200 test cable.

The Universal Logic Interface provides the general purpose logic necessary to interface into the I/O system of an INTERDATA Processor. The general purpose interfacing logic may be used to connect a device to either the Multiplexor or Selector Channel I/O Bus. One half of the Universal Logic Interface contains the general purpose logic and the other half may be used to build a controller for a device.

2. UNPACKING

When the Universal Logic Interface is shipped with a system, it is installed at the factory so there is no special unpacking procedure. If the module assembly is purchased separately, it should be inspected for damage prior to installation.

3. LOCATION

The 15 inch 35-479 Universal Logic Interface may be installed in any available I/O slot of a standard 15 inch chassis.

4. BACK PANEL WIRING

Remove the RACK0/TACK0 jumper from the slot occupied by the Universal Logic Interface. The jumper is located between Terminals 122 and 222 of Connector 1 of the selected slot.

5. CABLE CONNECTIONS

5.1 Internal

The 50 pin connector of the 17-185 cable is connected to Connector 3 of the 35-479 ULI. The other end of the cable is divided into two 25 wire cables which terminate in the following connectors.

One 26-035, 25 pin, J2 female Cinch connector.
One 26-036, 25 pin, P1 male Cinch connector.

The J2 and P1 connectors are mounted on the convenience panel in the system cabinet. See Figure 1. The 17-200 ULI Test Cable is connected to Connector 3 of the 35-479 ULI. Refer to the 06-129R03 or higher ULI Test Program for further information on the 17-200 ULI Test Cable.

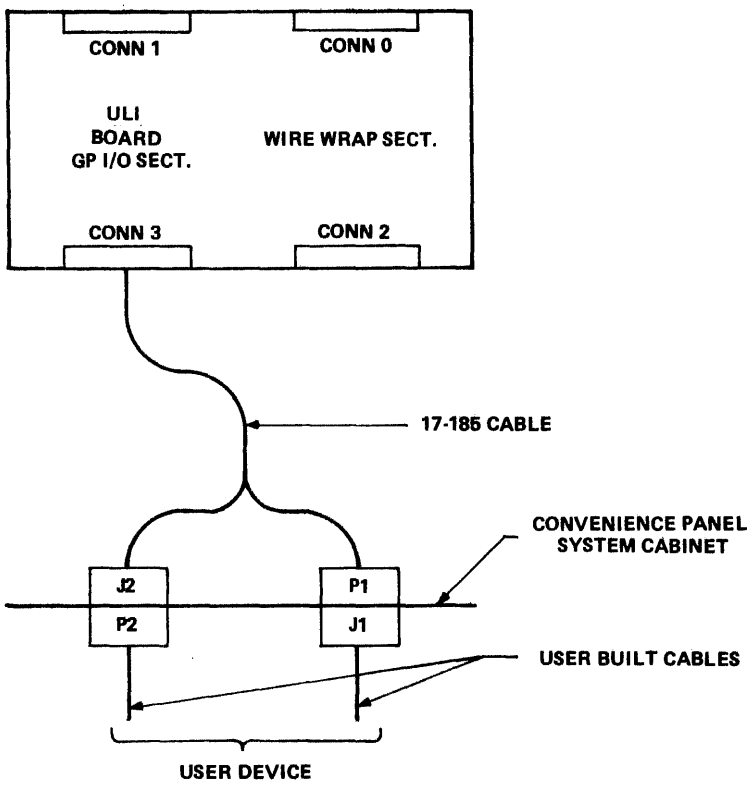


Figure 1. Cable Connection

5.2 External

The user is provided with one 26-035, 25 pin, J1 female Cinch connector, and one 26-036, 25 pin, P2 male Cinch connector to mate with the J2 and P1 connectors on the convenience panel. That is, J1 to P1 and P2 to J2. The user builds cables as required to interface peripheral equipment into the system. Refer to the pin map and connector pin location in Figures 2 and 3. The pin map lists the ULI Input/Output lines available to the user at the convenience panel's J2 and P1 connectors. The user's P2 and J1 connectors are wired such that the desired signal transfers are obtained between the ULI and the user's equipment. For example, to connect to Data Input line DIN000, the user connects to Pin 01, P2 connector, which mates with Pin (socket) 01, J2 connector on the convenience panel.

6. STRAP OPTIONS

6.1 Address Strapping

The preferred address of the Universal Logic Interface is X'8B'. The ULI is strapped for this address at the factory. To change the address, refer to Functional Schematic 02-304D08, Sheet 2.

6.2 External Lines

All signals that are shown in Figure 2, Pin Map, with the exception of grounds, may be changed at option. Refer to Functional Schematic 02-304D08, Sheets 3 and 4.

6.3 Byte to Halfword Mode

The Universal Logic Interface is normally strapped for Halfword to Halfword or Byte to Byte date transfer mediums. By changing a strap option on the ULI, a Byte to Halfword data transfer may be obtained. Refer to Functional Schematic 02-304D08, Sheet 3. The ULI Programming Specification (02-304A22) describes this mode of operation.

Strap 8 to T for Byte to Halfword.

Strap 8 to U for Byte to Byte or Halfword to Halfword.

PIN MAP		
CONNECTOR 3		
ROW 1	ROW 2	PIN NO.
GND	GND	00
SIN060	SIN070	01
SIN040	SIN050	02
SIN020	SIN030	03
SIN000	SIN010	04
DIN140	DIN150	05
DIN120	DIN130	06
DIN100	DIN110	07
DIN080	DIN090	08
DIN060	DIN070	09
DIN040	DIN050	10
DIN020	DIN030	11
DIN000	DIN010	12
SATN0	SCLROB	13
COT070	COT060	14
COT050	COT040	15
DOT150	DOT140	16
DOT130	DOT120	17
DOT110	DOT100	18
DOT090	DOT080	19
DOT070	DOT060	20
DOT050	DOT040	21
DOT030	DOT020	22
DOT010	DOT000	23
GND	GND	24

PIN MAP		
CONNECTOR 2		
ROW 1	ROW 2	PIN NO.
		00
		01
		02
		03
		04
		05
		06
		07
		08
		09
		10
		11
		12
		13
		14
		15
		16
		17
		18
		19
		20
		21
		22
		23
		24

This pin map shows what signals are present on the connectors of the ULI as wired at the factory. These signals may be changed by changing the wire wrap straps (refer to Functional Schematic 02-304D08, Sheets 3 and 4).

Figure 2. Pin Map

PIN MAP*		
CONNECTORS		
J2	P1	PIN NO.
DIN000	GND	01
INT0	GND	02
SCLR0B	SIN070	03
COT070	SIN060	04
COT060	SIN050	05
COT050	SIN040	06
COT040	SIN030	07
DOT150	SIN020	08
DOT140	SIN010	09
DOT130	SIN000	10
DOT120	DIN150	11
DOT110	DIN140	12
DOT100	DIN130	13
DOT090	DIN120	14
DOT080	DIN110	15
DOT070	DIN100	16
DOT060	DIN090	17
DOT050	DIN080	18
DOT040	DIN070	19
DOT030	DIN060	20
DOT020	DIN050	21
DOT010	DIN040	22
DOT000	DIN030	23
GND	DIN020	24
GND	DIN010	25

*Pin Map for J2 and P1 connectors when the 17-185 cable is connected to Conn 3 of the ULI and mounted on the convenience panel in the system cabinet.

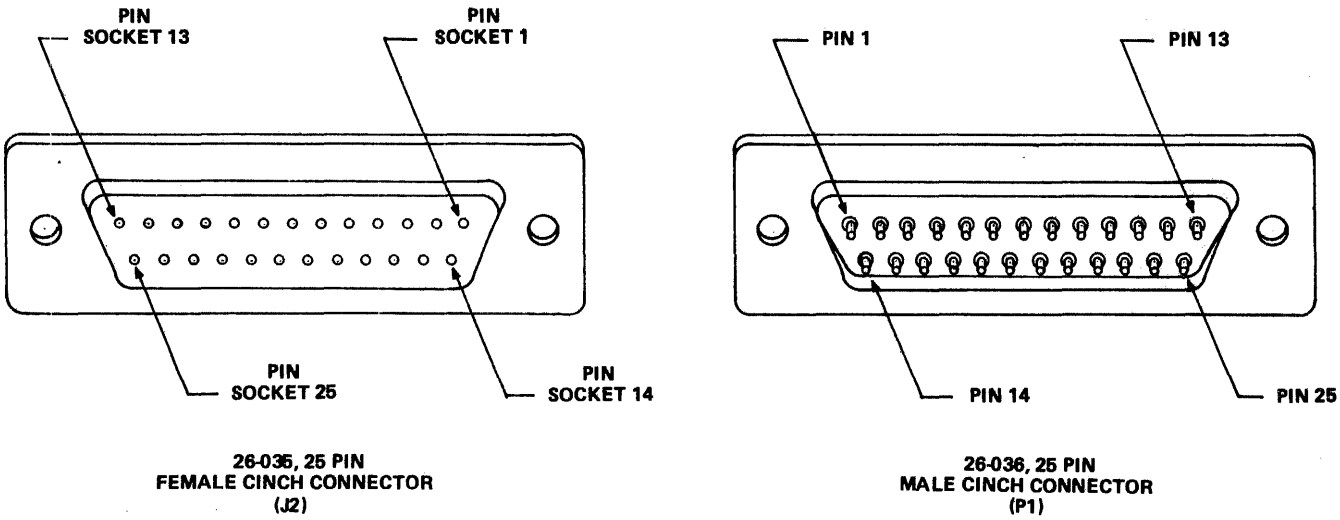


Figure 3. Pin Map and Connector Pin Location for 17-185 Cable

7. INSTALLATION CHECKS

To insure proper operation of the Universal Logic Interface, Test Program 06-129R03 or higher should be executed in accordance with its test program description.

8. DEFINITION INPUTS AND OUTPUTS

8.1 Inputs

The 16 Data Input lines DIN000:150, 8 Status Input lines SIN080:150, and 1 interrupt line (SATN0), are terminated on the 15 inch module board as shown in Figure 4. The G gate is a standard DTL type 846 or equivalent.

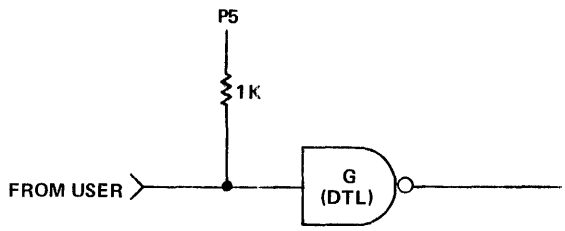


Figure 4. Module Input Termination

8.2 Outputs

The 16 Data Output lines DOT000:150, 4 Command Output lines COT040:070, and 1 initialize line (SCLR) from the module, are driven as shown in Figure 5. The P gate is a standard DTL open collector type 858 or equivalent.

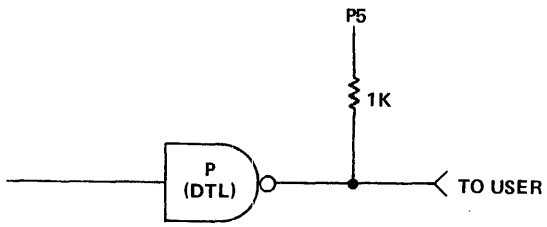


Figure 5. Module Output Logic

9. TIMING

There is no special timing in this module.

10. OPTIONS

The module operates with a byte oriented device or a halfword oriented device and may be operated in an 8-bit Byte Mode or in a true 16-bit parallel Halfword Mode.

M48-013
UNIVERSAL LOGIC INTERFACE MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-304 Universal Logic Interface (ULI) is an interface device designed to provide a convenient byte or halfword interface between user designed circuits and the INTERDATA Multiplexor or Selector Channel I/O Bus. This module contains the following functions.

1. Sixteen Data Output lines (DOT)
2. Sixteen Data Input lines (DIN)
3. Four Command Output lines (COT)
4. Eight Status Input lines (SIN)
5. One Interrupt line (SATN0)
6. One Initialize line (SCLR)
7. Five I/O Service lines

Data can be transferred between the ULI and the Multiplexor Bus (MPX) in an eight-bit Byte Mode or in a true sixteen-bit parallel Halfword Mode. The data transfer mode is set up under program control and strap option. The interrupt line can be disabled, enabled, or disarmed within the ULI by program control.

2. SCOPE

This specification describes the functional operation of the Universal Logic Interface and its relationship with the user's device and the Processor. This specification contains a block diagram analysis, a functional diagram analysis, and a mnemonic list for the ULI.

3. BLOCK DIAGRAM ANALYSIS

The ULI is a communication link between the Processor I/O Multiplexor Bus (MPX) or the Selector Channel I/O Bus and a byte oriented or halfword oriented device. Refer to the ULI block diagram in Figure 1 and to Functional Schematic 02-304D08.

The functions that are integrated in the operation of the module are: Status, Command, Data Output, and Data Input.

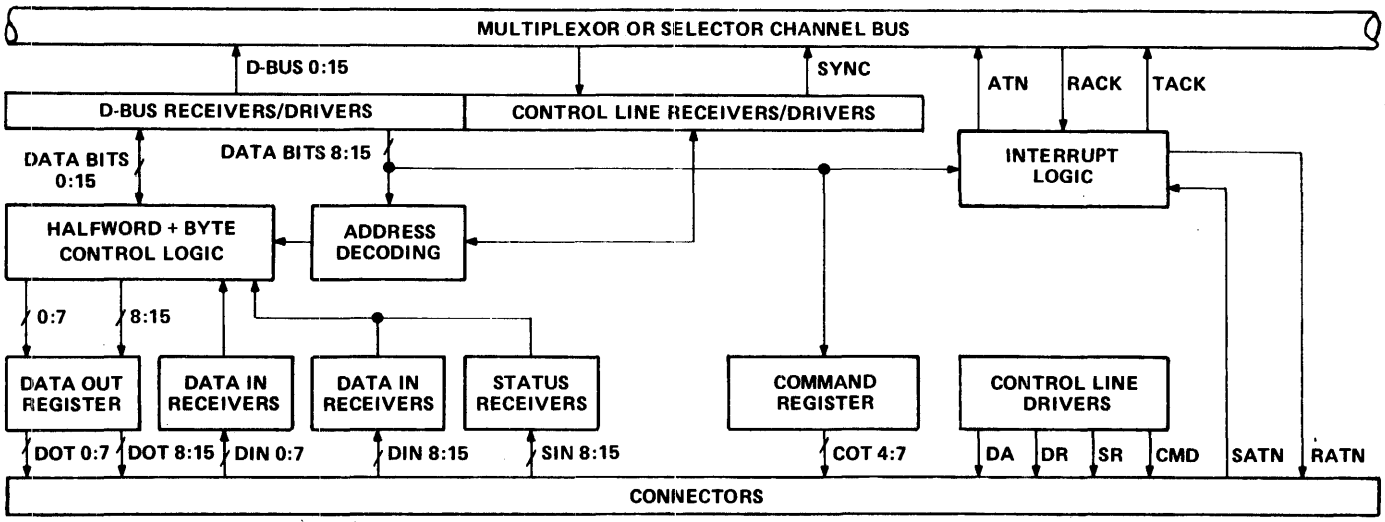


Figure 1. Universal Logic Interface Block Diagram

3.1 Status

Eight Status Input lines (SIN000:070) are available to the user. The user connects the desired sense lines to eight status input lines. To read in status on the eight status lines, the program executes a Sense Status instruction which causes the Processor to generate a Status Request pulse (SR0). The SR0 pulse enables the transfer of status from the eight Status Input lines SIN000:070 onto Data Lines D080:150.

3.2 Command

The Command control lines combined with the Command instructions on Data Lines D080:150, are used and/or steered as follows:

The two most significant bits of the command byte (Bits 8 and 9) and the Command control line, disable, enable, or disarm the interrupt logic.

The third bit of the command byte (Bit-10) and the Command control line determines the data transfer medium between the ULI and the Processor or SELCH.

The fourth command bit is not used.

The four least significant bits of the command byte (Bits 12:15) on Data Lines D120:150 are loaded onto Command Output lines COT040:070 by the Command control line.

3.3 Data Output

Sixteen Data Output lines (DOT000:150) are available to the user and may be used in three modes of operation.

3.3.1 Byte Mode. In the eight-bit Byte Mode, all data is transferred over Bits 0:7 between the ULI and the byte oriented device.

When the Data Available Line (DA0) is pulsed and if the ULI is addressed, signal LHDT1 becomes active causing the Data Output register to copy the data on the I/O Bus (D080:D150) and place that data on the Data Output lines (DOT000: DOT070).

3.3.2 Halfword Mode. In the Halfword Mode, two parallel eight-bit bytes are transferred at the same time between the ULI and the Processor or Selector Channel. All data is also transferred between the ULI and the device as a 16 bit halfword. Either a byte or halfword oriented device may be used in this mode. Read Halfword and Write Halfword instructions must be used. If the device is byte oriented, ignore either the least or most significant byte of data.

When the Data Available line is pulsed and if the ULI is addressed, signals LLDT1 and LHDT1 become active causing the Data Output register to copy the data on the I/O Bus (D000:D150) and place that data on the Data Output lines (DOT000: DOT150).

3.3.3 Byte to Halfword Mode (Strap Option). The Byte to Halfword Mode may be obtained by changing a strap option in the ULI. Refer to Functional Schematic 02-304D08, Sheet 3. In this mode of operation, data is transferred between the ULI and the Processor or Selector Channel as eight-bit bytes which are assembled by the ULI into halfwords for a halfword oriented device. In the Byte to Halfword Mode, the first Data Available pulse (DA0) loads an eight-bit byte from the I/O Bus Bits 8:15 (D080:D150) into the Data Output register Bits 0 through 7 (DOT000:DOT070). The second Data Available pulse loads an eight-bit byte into the Data Output register Bits 8:15 (DOT080:DOT150).

3.4 Data Input

Sixteen Data Input lines (DIN000:DIN000:150) are available to the user and may be used in three modes of operation.

3.4.1 Byte Mode. In the eight-bit Byte Mode, when the Data Request lines are pulsed and if the ULI is addressed, Data In lines 0 through 7 (DIN000:DIN070) are gated into the Processor or Selector Channel I/O Bus Bits 8 through 15 (D080:D150).

3.4.2 Halfword Mode. In the Halfword Mode, when the Data Request line (DR0) is pulsed and if the ULI is addressed, Data In lines 0 through 15 (DIN000:DIN150) are gated into the Processor or Selector Channel I/O Bus Bits 8 through 15 (D00:D150).

3.4.3 Byte to Halfword Mode (Strap Option). Refer to 3.3.3 Byte to Halfword Mode. Data Input lines 0 through 7 (DIN000:DIN070) are gated to the Processor or Selector Channel I/O Bus, Bits 8 through 15 (D080:D150) on the first Data Request. The second Data Request gates Data Input lines 8 through 15 (DIN080:DIN150) into the I/O Bus of the Processor or Selector Channel Bits 8 through 15 (D080:D150).

4. FUNCTIONAL DIAGRAM ANALYSIS

4.1 Introduction

To understand INTERDATA functional schematics, it must be noted that the last character in the mnemonic symbol designates the logic level when the signal is active. For example; D080 is Data Line Number 8 and the last character 0 means that when D080 is active, the line is at a logical Zero level.

4.2 Addressing

To communicate with the ULI, it must first be addressed. The ULI Address (X'8B' preferred) is placed on Data Lines D080:150 (Sheet 2) and the Address control line is activated (ADRS0) (2G2). The appropriate data lines are inverted by eight NAND gates. The gated outputs are strapped to present all highs at the inputs to the NAND gate at 2F1. The non-inverted output from this gate SAD0 is applied to the Direct Set input of the Address flip-flop (2K2) enabling SYNC (SYN0) to the Processor.

4.3 Command

An active Command control line (CMD0) (3A2) is ANDed with FAD1 enabling SYN0 to the Processor. CMD0 also generates CMG1 (4R4) which loads command information from Data Lines D120:150 onto the four Command Output lines COT 040:070. The trailing edge of CMD1 toggles the DISARM (2H7) and DISABLE (2H6) flip-flops to disable, enable, or disarm the interrupt logic. Refer to Programming Specification 02-304A22.

The Command control line (CMD0) and Data Bit 10 (D100) determine the data transfer mode of operation. To establish the Halfword Mode, the Command Control Line and Data Bit 10 must be active. The trailing edge of the CMD0 pulse sets the Halfword flip-flop (3E2). The set output of the Halfword flip-flop (FEHW0) causes the halfword line (HW0) (3K1) to the Processor or Selector Channel to become active indicating to the Processor or Selector Channel that the ULI expects the halfword data transfers.

If the Byte to Halfword option is installed, the set output of the Halfword flip-flop (FEHW0) (3E2), when set, holds the Byte Steering flip-flops clear (3E3). When the system is Initialized or Powered-Up (SCLR0) (2G3), the Halfword flip-flop is set and the Byte Steering flip-flop is held cleared.

In the Byte Mode (CMD0 active and Data Bit 10 (D100) inactive), the Halfword flip-flop is reset on the trailing edge of the CMD0 pulse. The halfword line (HW0) (3K1) to the Processor or Selector Channel becomes inactive indicating that the ULI expects data a byte at a time.

4.4 Status Request (Sense Status Instruction)

An active Status Request control line (SR0) causes both 3D6 (1L9) and ED1B1 (3D5) to go low. SR0 is ANDed with FAD1, activating EDI0 (3G5) which enables SYN0 to the Processor (3K5). The low ED1A1, ED1B1, and EDI0 signals are input to the four Four-to-One multiplexors (Sheet 2) to load status information on Status Input lines SIN000:070 onto Data Lines D080:150.

4.5 Data Available (Write Data Instruction)

In the eight bit Byte Mode (Halfword flip-flop reset) when a Write Data instruction is executed, a Data Available pulse (DA0) is sent from the Processor or Selector Channel. The DA0 pulse is ANDed with FAD1 and causes a SYNC pulse (SYN0) to be sent to the Processor or Selector Channel. The DA0 pulse also causes Load High Data (LHDT1) (3K3) to go active. LHDT1 active and FEHW0 high loads the data being sent from the Processor or Selector Channel on data lines D080:D150 into the Data Output register. The Data Output lines DOT000:DOT070 indicate the byte of data loaded into the Data Output Register. Successive DA0 pulses will perform the same operation.

If the Byte to Halfword option is installed and the Halfword and Byte Steering flip-flops are reset, when two consecutive Write Data (WD) instructions are executed and two Data Available pulses (DA0) are sent from the Processor, the first DA0 pulse is ANDed with FAD1. The output enables SYN0 to the Processor, applies DA0 to the gate at 3H5, and is ANDed with DR1 which applies a high to the toggle input of the Byte Steering flip-flop (3E3). With the Byte Steering flip-flop reset, Load High Data is active (LHDT1) (3K3). LHDT1 active and FEHW0 high (4A4) loads the first data byte from Data Lines D080:150 onto Data Output lines DOT000:070. The Byte Steering flip-flop sets on the trailing edge of the first DA0 pulse. The second DA0 pulse enables SYN0 to the Processor. With the Counter flip-flop set, Load Low Data is active (LLDT1) (3K2) and LHDT1 is inactive. LLDT1 loads the second data byte from Data Lines D080:150 onto Data Output lines DOT080:150. The Byte Steering flip-flop resets on the trailing edge of the second DA0 pulse.

In the Halfword Mode, the Halfword flip-flop (3E2) is set by CMD0 control line, Data Bit-10 (D100). HW0 and SYN0 are enabled to the Processor, and the Byte Steering is reset by FEHW0. The reset output from the Byte Steering flip-flop (FEHB1), an active FEHW0, and the DA0 pulse enables both LLDT1 and LHDT1. LLDT1 loads the data byte from Data Lines D080:150 onto Data Output lines DOT080:150. FEHW1 high (3M1) is ANDed with the data byte from Data lines D000:070. The outputs are loaded onto Data Output lines DOT000:070 by LHDT1.

4.6 Data Request (Read Data Instruction)

In the eight bit Byte Mode (Halfword flip-flop reset) when a Read Data instruction is executed, a Data Request pulse (DR0) is sent from the Processor or Selector Channel. The DR0 pulse is ANDed with FAD1 at 3C3, activating ED10 which enables SYNC (SYN0) to the Processor or Selector Channel. DR0 also causes ED1B1 to go active, enabling Data In Lines DIN000 through DIN070 to be gated to the Processor or Selector Channel data lines (D080:D150). Successive DR0s will perform the same operation.

If the Byte to Halfword option is installed and the Halfword and Byte Steering flip-flops are reset, when two consecutive Read Data (RD) instructions are executed and two Data Request pulses (DR0) are sent from the Processor, the first DR0 pulse is ANDed with FAD1 at 3C3, activating ED10 which enables SYN0 to the Processor, and is applied to one input of the gates 3C6 and 3C2 which control the EDIA1 and EDIB1 signals. DR0 is also ANDed with FAD1 at 3D3. The output from this gate is ANDed with DA1 which applies a high to the toggle input of the Byte Steering flip-flop. With the Byte Steering flip-flop reset, EDIA1 is low, EDIB1 is high, and EDI0 is low. These signals are input to the four four-to-one multiplexors (Sheet 2) to load the data byte from Data Input lines DIN000:070 onto Data Lines D080:150. The Byte Steering flip-flop sets on the trailing edge of the first Data Request pulse. The second DR0 pulse also enables SYN0 to the Processor. With the Counter flip-flop set, EDIA1 is high, EDIB1 is low, and EDI0 is low. These signals are input to the four-to-one multiplexors (Sheet 2) to load the second data byte from Data Input lines DIN080:150 onto Data Lines D080:150. The Byte Steering flip-flop sets on the trailing edge of the second DR0 pulse.

In the Halfword Mode, the Halfword flip-flop (3E2) is set by CMD0 control line, DATA Bit 10 (D100) active. HW0 and SYN0 are enabled to the Processor. GHD1 loads the data byte from Data Input lines DIN000:070 onto Data Lines D000:070. EDIA1 is high, EDIB1 is low, and ED10 is low. These signals are input to the four four-to-one multiplexors (Sheet 2) to load the data byte from Data Input lines DIN080:150 onto Data Lines D080:150.

4.7 Interrupt

When an interrupt is generated, the Attention flip-flop is direct set via a differentiated negative going pulse, Set Attention (SATN0). The output from the Attention flip-flop generates an Attention signal (ATN0) to the Processor. Command Bits 8 and 9 provide control over the Attention flip-flop and the ANT0 line to the Processor. With Bit 8 true and Bit 9 (Data) false, the Attention flip-flop is disabled. That is, the flip-flop may be set, but the output is held low. With Bit 8 false and Bit 9 true, the ATN0 signal to the Processor is active which allows new interrupts or a queued interrupt to be recognized. With Bits 8 and 9 both true, the low from the Disarm flip-flop 2M7 direct clears the Attention flip-flop. The flip-flop is now in a disarm state and cannot be set by the interrupt line. The disarm state is cleared whenever an enable or disable command is received. Initialize (SCLR0) also disarms the Attention flip-flop.

ATN0 is connected to the interrupt line in the Processor. The program responds with an Acknowledge Interrupt signal which is received by the controller as Receive Acknowledge (RACK0). Since the Attention flip-flop (2M3) was set prior to RACK0, ATN0A holds the RACK0/TACK0 latch set (2C4), and the Transmit Acknowledge (TACK0) to other devices is held high. The RACK0 signal generates Reset Attention RATN0A enabling SYN0 to the Processor, and RATN0 (2S4) which enables the device number, wired in by the address strapping (Sheet 2), to be input to the four four-to-one multiplexors. The decoded device number is loaded onto Data Lines D080:250. Upon receiving SYN0, the Processor removes RACK0 causing the Attention flip-flop to reset.

4.8 Initializing

When the system is initialized (SCLR0 active), the Attention, Address, Disable, and Disarm flip-flops are reset, and the Halfword flip-flop is set. SCLR0B is sent to the user.

5. MNEMONICS

The following list provides a brief description of each mnemonic found in the Universal Logic Interface. The source of each signal on Schematic Drawing 02-304D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
ADRS0	Address control signal from the Processor.	2G2
ADR0:7	Address lines in the ULB which return the module address to the Processor via Data Lines D080:150.	Sheet 2
ATN0	Attention signal to the Processor - Generated by active user interrupt signal.	2N5

MNEMONIC	MEANING	SCHEMATIC LOCATION
CMD0	Command signal from the Processor.	2A2
CMG0	Command gating signal.	3A1
COT040:070	Command Output Lines - Processor control lines to the user.	Sheet 4
DA0	Data Available pulse from the Processor.	3A4
DIN000:150	Data Input lines from the user to the ULI.	Sheet 3
DOT000:150	Data Output lines from the ULI to the user.	Sheet 4
DR0	Data Request from the Processor.	3A3
D000:150	16 bi-directional data lines between the ULI and the Processor.	Sheet 2
ED10A ED1A1 ED1B1	Enable Data Input - Enables status input (SR), low data byte input (DR), and SYN0 to the Processor (SR and DR).	3G5
FAD1	Address Flip-Flop set output.	2K2
FDSARM0	DISARM Flip-Flop 1 side - Command byte Bit-9 active.	2M7
FDSABL1	Disable Flip-Flop 0 Output - Command byte Bit-8 active.	2M6
FEHB1	Enable High Byte to the Processor - Write Data and Read Data byte and Halfword mode.	3F3
FEHW0	Enable Halfword Mode - Command byte Bit-10 active, Counter Flip-Flop 0 side.	3F2
GHD1	Gate High Data Byte to the Processor - Read Data, Halfword Mode.	3J3
HW0	Halfword active to the Processor.	3J1
INTR0	Interrupt-output of one shot which is started by the pulsing of SATN0.	2M8
LHDT1	Load High Data Byte (0:7) - Write Data, Byte and Halfword Mode.	3J3
LLDT1	Load Low Data Byte (8:15) - Write Data, Byte and Halfword Mode.	3J2
RACK0	Receive Acknowledge from the Processor via daisy chain priority system.	2J4
RATN0	Reset Attention - Enables decoding of the device address.	2S4
RATN0A	Reset Attention - Enables SYN0 to the Processor.	2S4
SAD0	Decoded device address output.	2M1
SATN0	Interrupt signal from the user.	2J9

MNEMONIC	MEANING	SCHEMATIC LOCATION
SCLR0	System clear - Initialize signal from the Processor.	2G3
SCLR0B	System clear - to the user.	4R7
SIN000:070	Status Input lines to the Processor.	Sheet 3
SR0	Status Request signal from the Processor.	3A5
SYN0	Synchronization pulse to the Processor.	3J5
TACK0	Transmit Acknowledge to the next device on the daisy chain priority system.	2R5

M48-013
UNIVERSAL LOGIC INTERFACE
PROGRAMMING SPECIFICATION

1. INTRODUCTION

The 02-304 Universal Logic Interface (ULI) provides a fully buffered, byte or halfword oriented interface module for data transfer between the Processor and byte or halfword oriented equipment provided by the user. The ULI is a transparent interface in that the function of any I/O instruction issued to the module depends upon the user's equipment. Data transfer rates can approach 1.9 million bytes per second (1.9 MBS) using the ULI, although this is highly dependent on the user's equipment and the related INTERDATA Processor.

2. CONFIGURATION

Not applicable to the 02-304 Universal Logic Interface.

3. OPERATING PROCEDURES

Not applicable to the 02-304 Universal Logic Interface.

4. DATA FORMAT

As shown in Figure 1, the ULI may be interfaced with either a byte or a halfword oriented device. The major functions available to the user equipment from the ULI are:

1. Sixteen Data Output lines (DOT000:150), each with a storage flip-flop which may be updated by executing a Write Halfword instruction.

2. Sixteen Data Input lines (DIN000:150) which may be read by executing a Read Halfword instruction.

3. Four Command Output lines (COT040:070), each with a storage flip-flop which may be updated by executing an Output Command instruction on Data Lines D120:150. These may be used as Read Commands, Write Commands, or for any other purpose determined by the user.

4. Eight Status Input lines (SIN000:070) which may be read by executing a Sense Status instruction. The definition of the status lines is determined by the user.

5. One priority interrupt line that may be queued and enabled by an output command. When acknowledge by an Acknowledge Interrupt instruction, the device number of the module is automatically transferred to the Processor along with the Eight Status Input lines.

6. One Initialize line that also clears any pending interrupt and Disarms the interrupt logic within the ULI.

7. Five I/O control lines:

   a. DAG1B — Indicates data is being sent from Processor or SELCH to the ULI.
   b. DRG1B — Indicates data is being read from the ULI by the Processor or SELCH.
   c. SRG1B — Indicates that the status bits of the ULI are being read by the Processor or SELCH.
   d. CMG1B — Indicates that a Command Byte is being sent to the ULI from the Processor.
   e. RATN1B — Indicates that an interrupt that was queued in the ULI was acknowledged by the Processor.

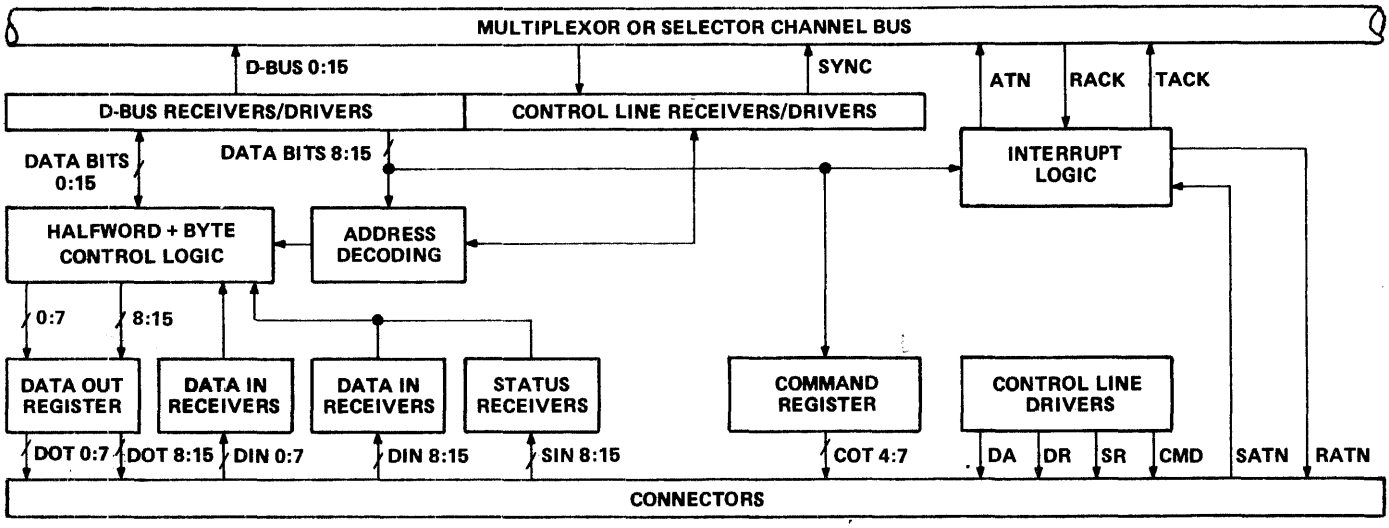


Figure 1. Universal Logic Interface Block Diagram

5. PROGRAMMING INSTRUCTIONS

Data transfer mode is selected by an output command to the module. Table 1 lists the output command bit assignments.

TABLE 1. UNIVERSAL LOGIC INTERFACE BYTE AND STATUS DATA

BITS	8	9	10	11	12	13	14	15
COMMAND	DISABLE	ENABLE	HW	X	COMMAND OUTPUT LINES (COT040:070)			
STATUS	← SIN000:070 →							

DISABLE — Disable Interrupt: Setting this bit with the ENABLE Bit reset prevents the device from interrupting the Processor, but allows an interrupt from the user's equipment to be queued.

ENABLE — Enable Interrupt: Setting this bit, with DISABLE Bit reset, allows the ULI to interrupt the Processor when an interrupt occurs from the user's equipment.

DISABLE-ENABLE — Setting both the DISABLE and ENABLE Bits places the interrupt logic in the DISARM state. The ULI is prevented from interrupting the Processor or queuing interrupts from the user's equipment, and any queued interrupt in the ULI is cleared. If both the ENABLE and DISABLE Bits are reset the prior interrupt state will be unchanged.

HW (HALFWORD) — Setting this bit places the ULI into the halfword mode and indicates to the Processor or Selector Channel that the ULI is a halfword interface. This mode may be used for parallel halfword data transfer with the Processor. This mode when used on a Selector Channel will cause all data to be transferred as halfwords.

X — This bit is undefined and has no effect on the ULI.

COT040:070 — The four least significant command bits (12:15) are available to the user and can be defined by the user as his equipment requires. Typically, these lines are used as Read or Write, or for other control purposes such as halt, run, etc.

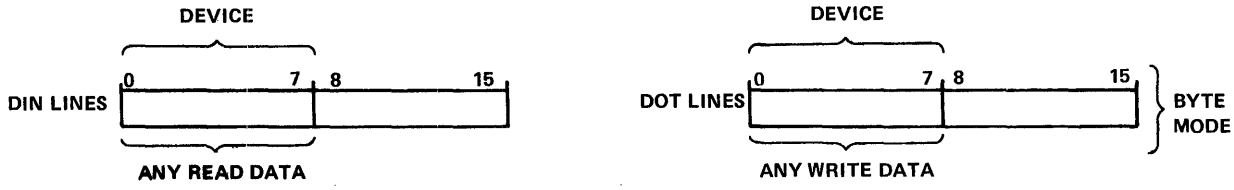
STATUS BYTE — These bits are defined by the user according to the requirements of his equipment. Typically, these lines are used to indicate equipment ready, equipment busy, equipment trouble, and a variety of other equipment status conditions.

6. PROGRAMMING SEQUENCES

The Universal Logic Interface is structured such that it may be either byte or halfword oriented depending upon whether it is in the byte or halfword mode. When the ULI is in the halfword mode, only Read and Write halfword instructions may be used.

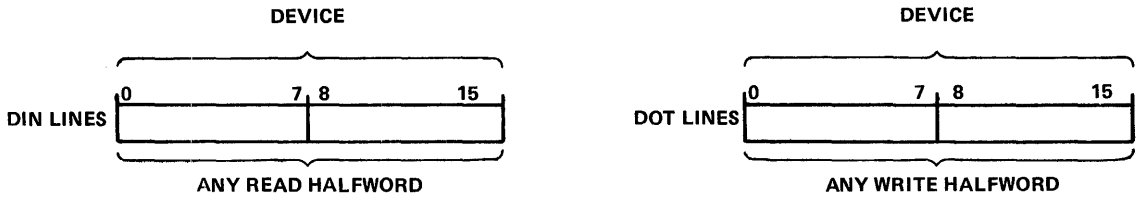
6.1 Byte Mode

When the ULI is in the byte mode, all data is transferred a byte at a time over Bits 8 through 15, between the ULI and the Processor or Selector Channel. Data is transferred between the ULI and the device, a byte at a time over Bits 0 through 7.



6.2 Halfword Mode

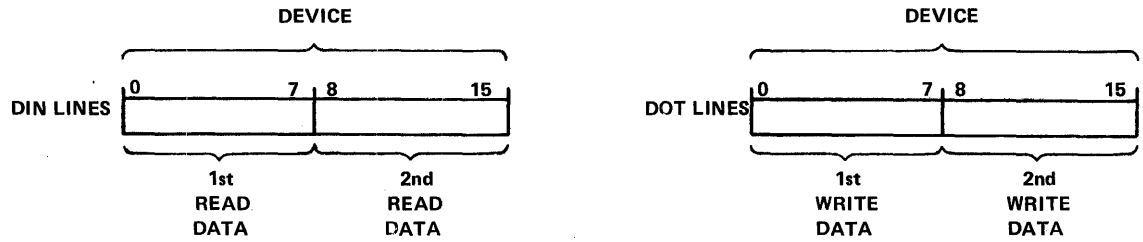
When the ULI is in the Halfword mode and Halfword instructions are used, two parallel bytes of data are transferred at the same time over Bits 0 through 15 between the ULI and the Processor or Selector Channel. Data is transferred between the ULI and the device as a halfword over Bits 0 through 15.



6.3 Byte to Halfword Mode (Strap Option)

When operating with a byte oriented device, the ULI can be operated in the Halfword Mode using Read Halfword and Write Halfword instructions and ignoring the least or most significant byte of data.

The Byte to Halfword mode option provides the ability to read or write halfwords of data between the ULI and the Processor or Selector Channel a byte at a time. Refer to Functional Schematic 02-304D08, Sheet 3, for strap option information.



Note that data is transferred between the ULI and the device as a halfword.

7. INTERRUPTS

The interrupt queuing capability of the ULI may be altered by program control. Three different states may be obtained by manipulation of Command Bits 8 and 9. Refer to Figure 2.

COMMAND BIT	8	9
ENABLE	0	1
DISABLE	1	0
DISARM	1	1
NO CHANGE	0	0

Figure 2. Interrupt Command Structure

When the ULI interrupt logic is Enabled, an interrupt may be queued in the ULI and signaled to the Processor.

When the ULI interrupt logic is Disabled, an interrupt may be queued in the ULI but the interrupt will not be signaled to the Processor until Enabled.

When the ULI interrupt logic is Disarmed, an interrupt may not be queued or signaled to the Processor. Any queued interrupt will become reset.

8. INITIALIZATION

The ULI is initialized when the Processor is powered-up or when manually initialized by the INIT switch on the Processor console. The initialized state of the ULI is when the interrupt logic is in the DISARM state and the Halfword Mode is set and the ULI is not addressed.

9. DEVICE NUMBER

The Universal Logic Interface is normally assigned Device Number X'8B', but this may be changed by a minor wiring alteration to the ULI. Refer to Functional Schematic 02-304D08, Sheet 2.

10. SAMPLE PROGRAM(S)

Not applicable to the 02-304 Universal Logic Interface.

11. APPENDICES

Not applicable to the 02-304 Universal Logic Interface.

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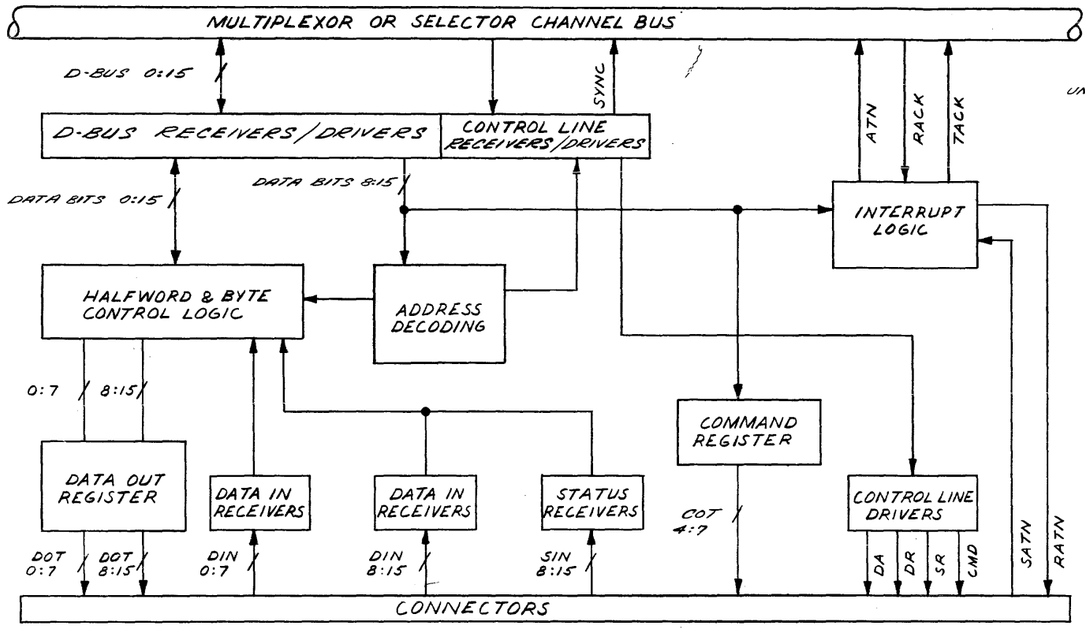
REVISIONS

UNIVERSAL LOGIC INTERFACE MODULE WITH 17-185 CABLE



UNIVERSAL LOGIC INTERFACE BLOCK DIAGRAM

UNIVERSAL LOGIC INTERFACE CONN3 — TYP 25 PLACES — P1

200	WHT	GND	01
100	BLK	GND	02
201		SIN070	03
101		SIN060	04
202		SIN050	05
102		SIN040	06
203		SIN030	07
103		SIN020	08
204		SIN010	09
104		SIN000	10
205		DIN150	11
105		DIN140	12
206		DIN130	13
106		DIN120	14
207		DIN110	15
107		DIN100	16
208		DIN090	17
108		DIN080	18
209		DIN070	19
109		DIN060	20
210		DIN050	21
110		DIN040	22
211		DIN030	23
111		DIN020	24
212		DIN010	25

UNIVERSAL LOGIC INTERFACE CONN3 — J2

112	DIN000	01
213	SCLR0B	03
113	SATN0	02
214	COT060	05
114	COT070	04
215	COT040	07
115	COT050	06
216	DOT140	09
116	DOT150	08
217	DOT120	11
117	DOT130	10
218	DOT100	13
118	DOT110	12
219	DOT080	15
119	DOT090	14
220	DOT060	17
120	DOT070	16
221	DOT040	19
121	DOT050	18
222	DOT020	21
122	DOT030	20
223	DOT000	23
123	DOT010	22
224	GND	25
124	GND	24

BACK PANEL MAP

ROW 1	ROW 2	TERM. NO.	CONN
P5	GND	41	0
GND	GND	40	
GND	GND	01	
P5	GND	00	

BACK PANEL MAP

ROW 1	ROW 2	TERM. NO.	CONN
P5	GND	41	1
GND	GND	40	
SCLR0	HWO	26	
		25	
		24	
SYNO	ATNO	23	
RACKO	TACKO	22	
	DAO	21	
DRO	CMDO	20	
SRO	ADR5O	19	
D140	D15O	18	
D120	D130	17	
D100	D110	16	
D080	D090	15	
D060	D050	14	
D040	D040	13	
D020	D030	12	
D000	D010	11	
GND	GND	01	
P5	GND	00	

FRONT EDGE CONNECTOR

ROW 2	ROW 1	TERM. NO.	CONN
		00	2
		01	
		02	
		22	
		23	
		24	

FRONT EDGE CONNECTOR

ROW 2	ROW 1	TERM. NO.	CONN
GND	GND	24	3
DOT000	DOT010	23	
DOT020	DOT030	22	
DOT040	DOT050	21	
DOT060	DOT070	20	
DOT080	DOT090	19	
DOT100	DOT110	18	
DOT120	DOT130	17	
DOT140	DOT150	16	
COT040	COT050	15	
COT060	COT070	14	
SCLR0B	SATN0	13	
DIN010	DIN000	12	
DIN030	DIN020	11	
DIN050	DIN040	10	
DIN070	DIN060	09	
DIN090	DIN080	08	
DIN110	DIN100	07	
DIN130	DIN120	06	
DIN150	DIN140	05	
SIN010	SIN000	04	
SIN030	SIN020	03	
SIN050	SIN040	02	
SIN070	SIN060	01	
GND	GND	00	

BUS 1 / 0

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REV LEVEL

UNIV LOGIC INTERFACE	35-479 R00

NOTE: THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

SHEET INDEX	REV LEVEL / SHEET NO.	1	2	3	4

NOTES

NAME	TITLE	DATE
B. GRAY	DRAFT	5-14-73
R. CERO	CHK	6-12-73
G. JOYCE	ENGR	6-5-73
H. ROSS	QC	6-1-73
R. E. JONES	DIR ENG	6-12-73

TITLE: FUNCTIONAL SCHEMATIC UNIVERSAL LOGIC INTERFACE

TASK NO. 03045 — SHEET OF 1-4

DWG NO. 02-304 D08

BRUNING 44-231 16042

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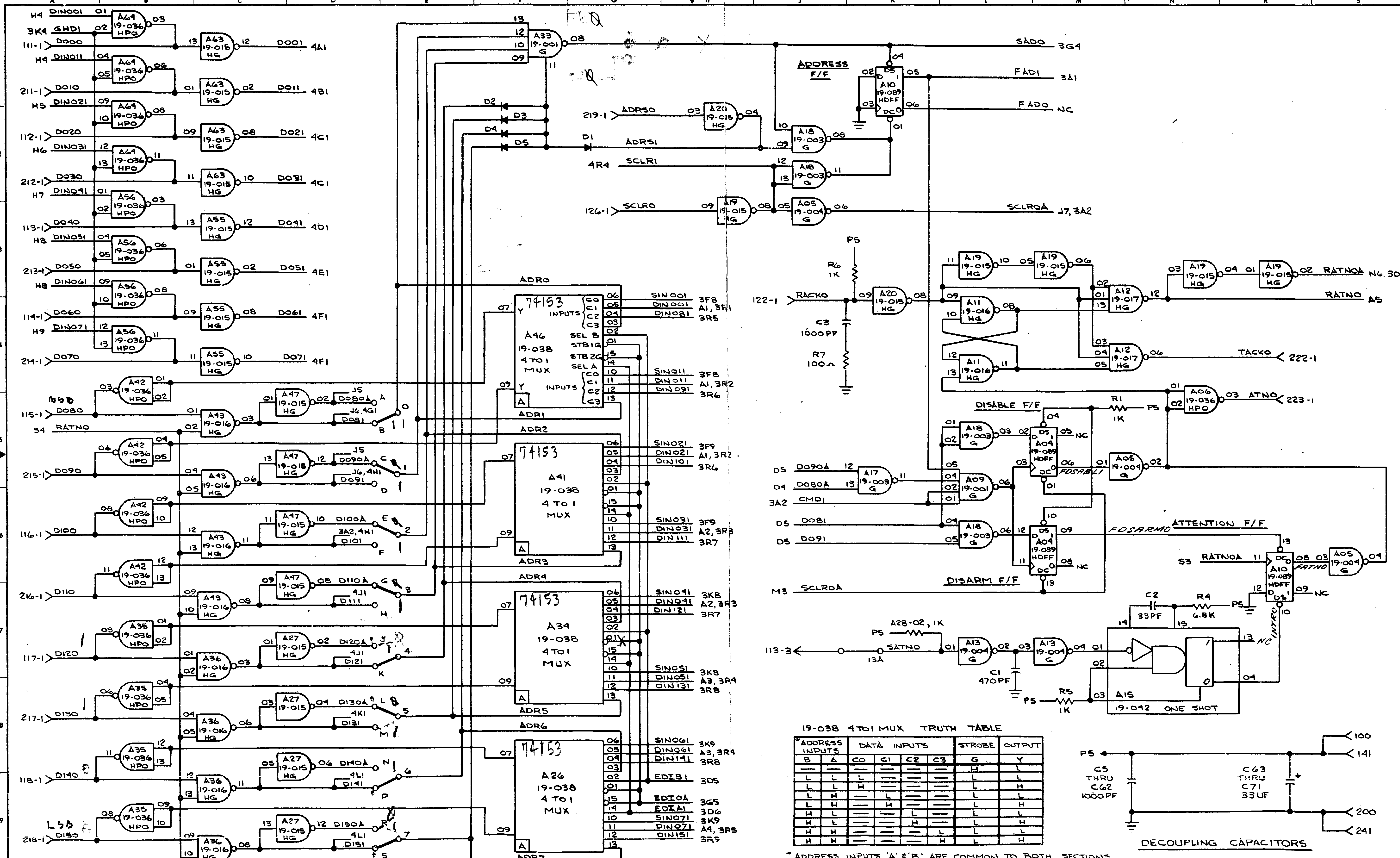
Computer Systems Division
Oceanport, N.J. 07757



19-038 4TO1 MUX TRUTH TABLE

*ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
—	—	—	—	—	—	H	L
L	L	L	—	—	—	L	L
L	L	H	—	—	—	L	H
L	H	—	L	—	—	L	L
L	H	—	H	—	—	L	H
H	L	—	—	L	—	L	L
H	L	—	—	H	—	L	H
H	H	—	—	—	L	L	L
H	H	—	—	—	H	L	H

*ADDRESS INPUTS 'A' & 'B' ARE COMMON TO BOTH SECTIONS

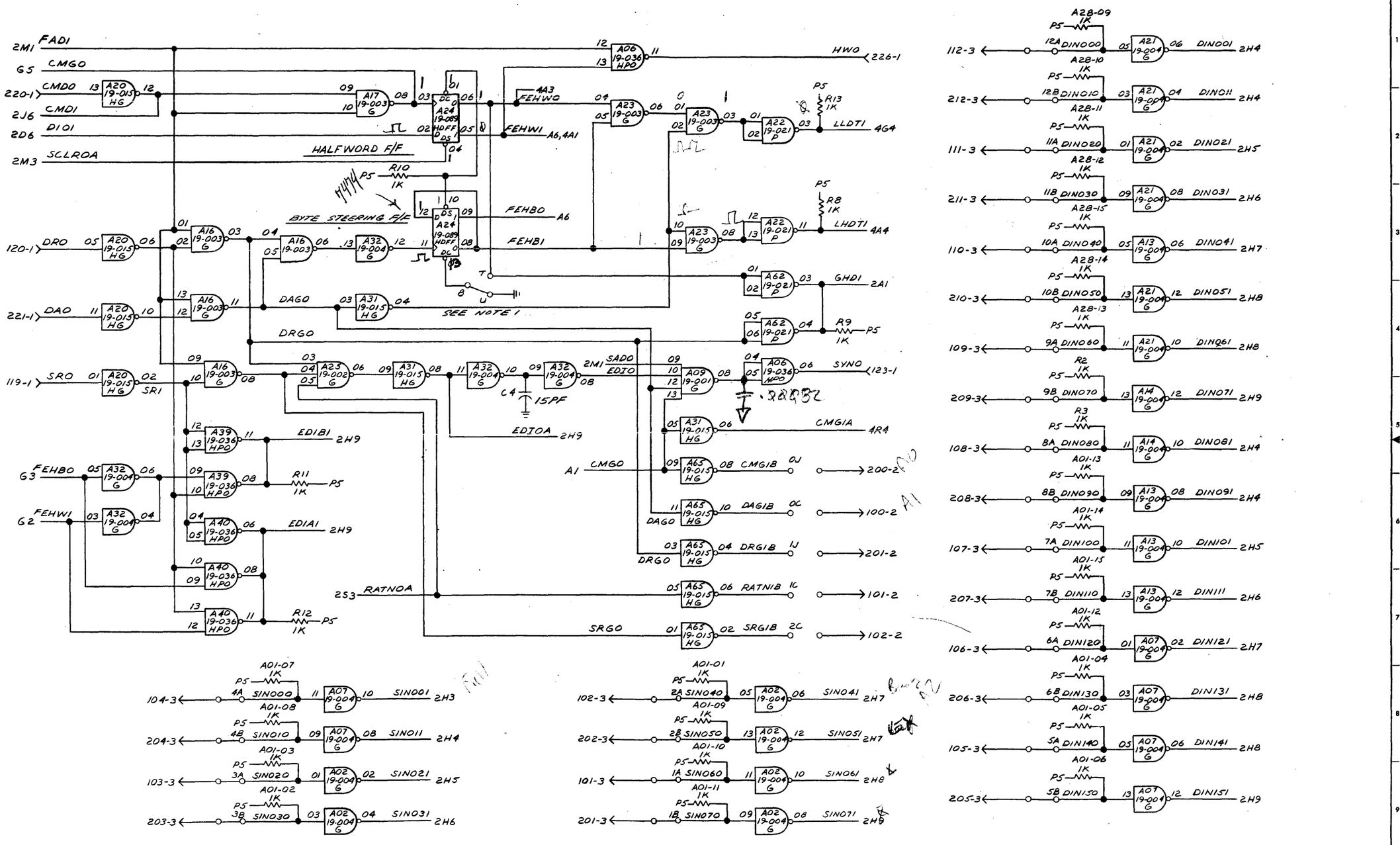
NOTES
1. PREFERRED DEVICE ADDRESS IS X'88'.
2. ALL DIODES ARE 23-001.

NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	4 MAY 73
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
UNIVERSAL LOGIC INTERFACE
TASK NO. 03095
DWG NO. 02-304 D08
SHEET 2-4

X'88' 1000 1011

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757



NOTES
1. FOR BYTE TO HALFWORD OPTION STRAP "8" TO "T".
HALFWORD ONLY "8" TO "U"

NAME	TITLE	DATE
B GRAY	DRAFT	5-9-73
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
UNIVERSAL LOGIC INTERFACE
TASK NO. 03045
DWG NO. 02-304 D08
SHEET OF 3-4

BRUNING 44-231 16042

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DATA OUTPUT REGISTER

NOTES

NAME	TITLE	DATE	TITLE FUNCTIONAL SCHEMATIC
CHRIS JENSEN	DRAFT	2 MAY 73	UNIVERSAL LOGIC INTERFACE
	CHK		
	ENGR		
	DIR ENG		TASK NO. 03095 SHEET OF
			DWG NO. 02-304 D08 4-4

BRUNING 44-231 16042

REVISIONS	
RELEASED FOR PRODUCTION	
MFG ENG:	DATE 6/11

15.380 REF

35,11 INSTALL APPARATUS SIDE

33 (5 PLACES)

SEE NOTE 1

GROUND

CONN3

CONN2

14.880 REF.

JUMPER TIP. CHL 23 ROWS

MOUNT ON SOLDER SIDE (4 PLACES)

SEE NOTE 1

BEND PINS CLOSEST TO EDGE OF BOARD INWARD PRIOR TO SOLDERING.

.530 MAX

.062 REF.

.125 MAX.

PARTIAL VIEW A-A

NOTE:
1. STIFFENER BAR (ITEM 3) SHALL BE SOLDERED TO GND BUS AT 2 END POINTS AND CENTER POINT.

INSTALL ITEM 35 APPARATUS SIDE AS SHOWN. TYPICAL MOUNTING FOR SPARE POSITIONS 66 THRU 102.

MASK DASHED AREA BEFORE WAVE SOLDERING OPERATION. (TYPICAL 7 ROWS)

COMPONENT	REF DESIGNATION
CAPACITORS	C1 THRU C71.
RESISTORS	R1 THRU R13.
DIODES	D1 THRU D5.
ICS	A01, 02, 04 THRU 07, 09 THRU 32, 55 THRU 60, 62 63 & 69.

NAME	TITLE	DATE
E. CERO	DRAFTING	6-11-73
E.F. CERO	CHECK	6-11-73
G. JOSCE	ENGR	6-11-73
H. ROSS	ECI	6-11-73
R.E. JONES	MFG ENG	6-21-73

TITLE: ASSEMBLY UNIVERSAL LOGIC INTF. MMS

03095 SHT 1 OF 1

35-979 E03

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