

DIGITAL INPUT/OUTPUT CONTROLLER

PROGRAMMING MANUAL

PERKIN-ELMER

Computer Systems Division
2 Crescent Place
Oceanport, New Jersey 07757
(201) 229-6800

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DIGITAL INPUT/OUTPUT CONTROLLER (DIO) PROGRAMMING MANUAL

INTRODUCTION

This document provides programming information for the INTERDATA Digital I/O Controller. It assumes that the reader is familiar with the I/O programming structure of INTERDATA Processors.

For information about INTERDATA programming, refer to the following:

INTERDATA 32-Bit Series Reference Manual, Publication Number 29-365
Model 7/32 Reference Manual, Publication Number 29-399
Model 8/32 Processor User's Manual, Publication Number 29-428
16-Bit Series Reference Manual, Publication Number 29-398

This manual describes the Digital Input/Output Controller and summarizes all of the information necessary to program the system. The Digital I/O (DIO) controller provides a standard interface between the Multiplexor Bus and the external peripheral device.

CONFIGURATION

The DIO Controller may be used with any Model 7/16, Model 7/32 or equivalent Processor.

DATA FORMAT

The DIO system is a halfword-oriented device. It consists of a 16-Bit output register and 16 input data lines. The 16 controller input bits represent external inputs to the system. The 16 bits of digital output data represent outputs from the processor. Since the DIO Controller includes two independent data paths, a bi-directional flow of information is possible between the processor and the peripheral device. Input operations command the external device to acquire and transfer 16 bits of information to the computer. Output operations enable the computer to output 16 bits of data to the external device (see Section entitled Device Numbers).

PROGRAMMING INSTRUCTIONS

Processor Instructions

The following Processor I/O Instructions are used to control and communicate with the Digital I/O Controller:

Sense Status (SS or SSR)

The Sense-Status instruction is used to determine whether the peripheral device is ready for data transfer operations.

Output Command (OC or OCR)

The Output Command instruction is used to enable, disable or disarm DIO Controller interrupts.

Write Halfword (WH or WHR)

The Write Halfword instruction is used to output 16 bits of data to the controller output register.

Read Halfword (RH or RHR)

The Read Halfword instruction is used to read 16 bits of data from the controller input data lines.

Acknowledge Interrupt (AI, AIR, ACK, and ACKR)

The Acknowledge Interrupt instruction (applicable to INTERDATA 16-Bit Processors only) is used to service interrupts. Execution of this instruction returns the address and status of the interrupting device.

Read Data/Write Data (RD,RDR,WD,WDR)

Since the DIO Controller is a halfword oriented device, the use of these instructions is not recommended. However, if used, the low order byte of data will be transferred to the device as a halfword with the 8 high order bits *undefined*.

STATUS AND COMMAND BYTES

Table 1 summarizes the DIO status and command byte data formats.

TABLE 1. DIO STATUS AND COMMAND BYTE FORMATS

Bit Number	0	1	2	3	4	5	6	7
Status Byte					BUSY			
Command Byte	Disable	Enable						

DISARM

*BUSY

The resetting of this bit, signals the computer that a halfword of data is available in the controller. If enabled, an interrupt is generated. The program can then read a halfword of data. When the read operation is complete, BUSY sets.

OUTPUT OPERATION:

The resetting of this bit signals the computer that the interface output register is ready to receive a halfword of data from the computer. If enabled, an interrupt is generated. The program must then write a halfword of data. At the completion of the Write operation, BUSY sets.

COMMAND

ENABLE

When this bit is set and DISABLE is reset, interrupts are passed to the Processor as they occur.

DISABLE

When this bit is set and ENABLE is reset, interrupts are not passed to the Processor as they occur but are queued by the interface.

DISARM

When both ENABLE and DISABLE are set, interrupts are not passed to the Processor as they occur, and are not queued by the interface. All pending interrupts are cleared.

NOTES

1. A Controller option enables the user to unconditionally inhibit the setting of the BUSY bit.
2. When the INIT switch is depressed on the Processor console, BUSY is set. Furthermore, when power is turned on, BUSY is set.
3. There is no Controller Output command to set or reset the BUSY status. In order to set the BUSY bit under program control, a "dummy" Read and Write operation must be performed (see section entitled "PROGRAMMING SEQUENCES").

PROGRAMMING SEQUENCES

Asynchronous Data Transfers (Appendices 2 and 3)

Data may be transferred to or from the device asynchronously by issuing a Write Halfword to the output address (N), or a Read Halfword instruction from the input address (N+1). The first programming example in Appendices 2 and 3 illustrates the use of a simple subroutine designed to transfer data in this manner. Interrupts from the controller should be disarmed and the BUSY status is not used to signal the processor when data transfers should be initiated.

Sense-Status Operation (Appendices 2 and 3)

Appendices 2 and 3 illustrate a subroutine to transfer data by sensing BUSY status. In addition, to initiate an input operation:

1. Disarm the controller interrupt system (see section entitled INTERRUPTS).
2. The BUSY status bit must be set to initiate the operation. If the state of the BUSY bit is unknown, a "dummy" Read Halfword instruction must be issued to set the BUSY bit. This signals the controller to initiate an input operation. The data read from the input data register by this "dummy" read, is undefined.
3. A Sense-Status instruction is used to sense the controller status. When BUSY resets, the program can read one halfword of data.

To initiate an output operation:

1. Disarm the Controller interrupts (see section entitled INTERRUPTS).
2. The BUSY status bit must be set to initiate the operation. If the state of the BUSY bit is unknown, a "dummy" Write Halfword instruction must be issued to set the BUSY bit. This signals the Controller to initiate an output operation.
3. A Sense-Status instruction is used to sense the status. When BUSY resets, the program can write one halfword of data.

Interrupt Driver Operation

Appendix 2 outlines a program to execute interrupt driven data transfers. To initiate an input operation:

1. Output a command to the input address assigned to the interface to enable interrupts.
2. Repeat Step 2 of Sense-Status Operation.*
3. When BUSY resets, the Controller generates an interrupt indicating that the input data is available in the DIO Controller. The program can then read 1 halfword of data.

To initiate an output operation:

1. Output a command to the output address assigned to the interface to enable interrupts.
2. Repeat Step 2 of the Sense-Status operation.**
3. When BUSY resets, the Controller generates an interrupt indicating that the computer should send data to the device by issuing a Write-Halfword to the output address.

Auto Drive Channel Operation

Appendix 3 illustrates an example of using the Series 32 Processor Auto-Drive channel to execute DIO data transfers. For further information concerning Auto-Driver Channel programming, refer to the *32 Bit Series Reference Manual*, Publication Number 29-365.

*If the Controller is wired to inhibit the setting of the BUSY status bit, this step should be ignored. An external interrupt occurs when data is available in the Controller.

**If the Controller is wired to inhibit the setting of the BUSY status bit, this step should be ignored. An external interrupt occurs when the device is ready to receive data.

INTERRUPTS

If enabled, an interrupt is generated by the DIO Controller when data is available in the interface, or when the output data register is requesting a halfword of data from the computer. This interrupt occurs if the BUSY bit is operational or not.

INITIALIZATION

Initialization disarms all system interrupts, clears the digital input and output registers and sets the BUSY status (bit 4), if operational.

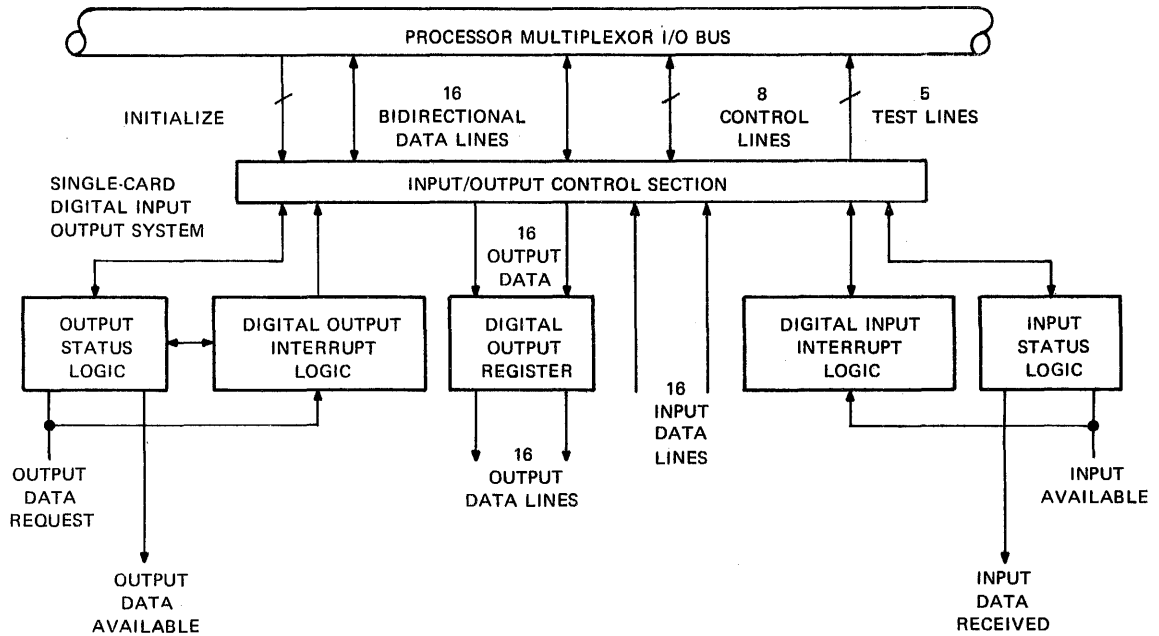
DEVICE NUMBERS

The Digital I/O Controller communicates with the processor via two device numbers. I/O instructions used in output operations must address a device number N as selected by two hexadecimal switches located on the controller board. This setting must be even, i.e., the least significant switch setting must be 0, 2, 4, 6, 8, A, C, or E. I/O instructions used in input operations must address an odd device number equal to $N + 1$.

SAMPLE PROGRAMS

Appendices 2 and 3 contain sample programs illustrating various methods of DIO data transfer.

APPENDIX 1
DIGITAL INPUT/OUTPUT (DIO) SYSTEM
BLOCK DIAGRAM



INTERFACING SIGNALS (REQUEST/RESPONSE)

SIGNAL	DESCRIPTION	FUNCTION	INTERRUPT	STATUS
OUTPUT DATA REQUEST	1 μSEC PULSE	PERIPHERAL DEVICE REQUESTING DATA	GENERATE PROCESSOR INTERRUPT	RESET BUSY=0
OUTPUT DATA AVAILABLE	1 μSEC PULSE	PROCESSOR DATA SETTLED ON LINES AND READY FOR PERIPHERAL	NO INTERRUPT GENERATED	SET BUSY=1
INPUT AVAILABLE	1 μSEC PULSE	PERIPHERAL DEVICE REQUESTING TO INPUT DATA TO PROCESSOR	GENERATE PROCESSOR INTERRUPT	RESET BUSY=0
INPUT DATA RECEIVED	1 μSEC PULSE	PROCESSOR ACKNOWLEDGES DATA ACCEPTED	NO INTERRUPT GENERATED	SET BUSY=1

PROG= *NONE* ASSEMBLED BY CAL 03-066R04-01 (32-BIT)

		1	SCRAT		D1000000
		2	TARGT 32		AOC00010
0000R		3	NLSTC		D1000020
		4	NORX3		D1000030
0000R		5	SGCHK		D1000031
0000R		6	IFZ ADC-2		D1000040
		9	ENDC		D1000080
		10	WIDTH 120		D1000090
0000R		11	SQUEZ		D1000100
		12	CROSS		D1000110
		13	* COPYRIGHT INTERDATA MAY 1975		D1000120
		14	*		D1000130
		15	* THE PROGRAMMING SEQUENCES THAT FOLLOW DEMONSTRATE THE VARIOUS METHODS		D1000140
		16	* OF DATA TRANSFER USING THE DIGITAL I/O CONTROLLER, THE FLOW-		D1000150
		17	* CHARTS IN APPENDIX 2 OUTLINE THE METHODS IMPLEMENTED BELOW. IN THE		D1000160
		18	* FIRST EXAMPLE, DATA IS TRANSFERRED TO AND FROM THE SYSTEM WITHOUT THE		D1000170
		19	* USE OF HANDSHAKING OR INTERRUPT LOGIC. STATUS FROM THE INPUT AND		D1000180
		20	* OUTPUT SUBSYSTEMS IS IGNORED AND SYSTEM INTERRUPTS ARE DISARMED, THE		D1000190
		21	* SUBROUTINE DIGITIO IS CALLED TO EXECUTE DATA TRANSFERS, THE CALLING		D1000200
		22	* ARGUMENTS INCLUDE AN INPUT/OUTPUT OPERATION IDENTIFIER AND A POINTER		D1000210
		23	* TO MEMORY SPECIFYING WHERE DATA IS TO BE RETRIEVED OR STORED.		D1000220
		24	* ALL PROGRAMMING EXAMPLES RUN WITH THE TEST CABLE REFERENCED IN		D1000230
		25	* APPENDIX 6 OF DOCUMENT 06-188A15.		D1000240
		26	* ALL PROGRAMMING EXAMPLES ARE WRITTEN IN CAL COMMON CODE.		D1000250
		27	*		D1000260
		28	* EQUATES AND REGISTER ALLOCATIONS		D1000270
0000 000D		29	STAT EQU 13	STATUS REGISTER	D1000280
0000 0004		30	OUTDEV EQU 4	OUTPUT DEVICE ADDRESS	D1000290
0000 0005		31	INDEV EQU 5	INPUT DEVICE ADDRESS	D1000300
0000 0006		32	IOIND EQU 6	INPUT-OUTPUT IDENTIFIER	D1000310
0000 0007		33	DTAPTR EQU 7	POINTER TO INPUT/OUTPUT BUFFER	D1000320
0000 0008		34	BSY EQU 8	BUSY STATUS FROM DIO CONTROLLER	D1000330
0000 000C		35	DTAPTR1 EQU 12	INPUT BUFFER POINTER FOR INTERRUPTS	D1000340
0000 0008		36	IONTCMP EQU 8	I/O NOT COMPLETE FLAG	D1000350
0000 0009		37	WK1 EQU 9	WORK REGISTER- GENERAL PURPOSE	D1000360
0000 000A		38	RETRY EQU 10	ADDRESS FOR ERROR RETRY	D1000370
0000 000B		39	INTDEV EQU 11	INTERRUPTING DEVICE ADDRESS	D1000380
0000 000F		40	RETN EQU 15	SUBROUTINE RETURN ADDRESS	D1000390
0000 0040		41	OLDPSWST EQU X'40'	OLD PSW SAVE AREA 16 BIT ONLY	D1000400
0000 0044		42	NEWPSWST EQU X'44'	NEW PSW STAT ON EXT INT 16 BIT ONLY	D1000410
0000 0046		43	NEWPSWLC EQU X'46'	NEW PSW LOC EXT INT 16 BIT ONLY	D1000420
0000 0003		44	RST03 EQU 3	EXECUTIVE REGISTER SET 0 R3	D1000430
0000 0002		45	RST02 EQU 2	EXECUTIVE REGISTER SET 0 R2	D1000440
0000 0001		46	RST01 EQU 1	EXECUTIVE REGISTER SET 0 R1	D1000450
0000 0000		47	RST00 EQU 0	EXECUTIVE REGISTER SET 0 R0	D1000460
0000 0000		48	RSTF0 EQU 0	REGISTER SET F-REGISTER SET 0	D1000470
0000 0007		49	DTAPTR0 EQU 7	OUTPUT BUFFER POINTER -REGISTER SET 0	D1000480
0000 0004		50	OUTDEV0 EQU 4	OUTPUT DEVICE ADDRESS- REG. SET 0	D1000490
0000 0005		51	INDEV0 EQU 5	REGISTER SET 0 INPUT DEVICE ADDR	D1000500
0000 000C		52	DTAPTR10 EQU 12	REGISTER SET 0 INPUT BUFFER POINTER	D1000510
0000 000E		53	WK2 EQU 14	WORK REGISTER 2	D1000520
0000 0002		54	BUFFLMST EQU 2	BUFFER LIMIT STATUS	D1000530
0000R C890 00F0		55	DIOINTR LDAI WK1,X'F0'	SELECT REGISTER SET X'F'	D1000540
0000R 95A9		56	FPSH RETRY,WK1	EXCHANGE PROGRAM STATUS	D1000541

0006R	4840	010AR	57	LH	OUTDEV,DEVADR1	GET THE OUTPUT DEVICE ADDRESS	D1000542	
000AR	DE40	0112R	58	OC	OUTDEV,DISARM	DISARM OUTPUT DEVICE LOGIC.	D1000550	
000ER	4850	010CR	59	LH	INDEV,DEVAUR2	GET THE INPUT DEVICE ADDRESS	D1000560	
0012R	DE50	0112R	60	OC	INDEV,DISARM	DISARM INPUT DEVICE INTERRUPTS	D1000580	
0016R	2461		61	LIS	IOIND,1	SET THE I/O INDICATOR FOR DIO OUTPUT	D1000590	
0018R	C870	010ER	62	LDAI	DTAPTR,OUTBUFFER	GET THE POINTER TO THE OUTPUT DATA	D1000600	
001CR	41F0	002ER	63	BAL	RETN,DIGITIO	CALL THE SUBROUTINE TO WRITE DATA.	D1000610	
0020R	0766		64	XAR	IOIND,IOIND	RESET THE IO INDICATOR FOR INPUT OP	D1000620	
0022R	C870	0110R	65	LDAI	DTAPTR,INBUFFER	GET POINTER FOR INPUT DATA	D1000630	
0026R	41F0	002ER	66	BAL	RETN,DIGITIO	GO READ THE INPUT DATA	D1000640	
002AR	C200	0120R	67	LPSW	WAIT	HALT THE MACHINE	D1000650	
			68	*			D1000660	
			69	*	SUBROUTINE DIGITIO TRANSFERS 16 BITS OF PARALLEL BINARY DATA EITHER		D1000670	
			70	*	TO THE DIGITAL I/O SYSTEM OR FROM THE DIGITAL I/O SYSTEM. STATUS LOG-		D1000680	
			71	*	IC FROM THE CONTROLLER IS IGNORED. AMONG THE CALLING ARGUMENTS ARE AN		D1000690	
			72	*	INPUT/OUTPUT INDICATOR FLAG,PHYSICAL DEVICE ADDRESS AND A POINTER TO		D1000700	
			73	*	THE RESPECTIVE INPUT OR OUTPUT DATA BUFFER.		D1000710	
			74	*			D1000720	
			75	*	CALLING SEQUENCE: BAL RETN,DIGITIO		D1000730	
			76	*	INPUT REGISTERS: OUTDEV= OUTPUT DEVICE ADDRESS(EVEN DEVICE ADDR.)		D1000740	
			77	*	INDEV= INPUT DEVICE ADDRESS (ODD DEVICE ADDRESS)		D1000750	
			78	*	IOIND= INPUT OUTPUT IDENTIFIER		D1000760	
			79	*	DTAPTR= POINTER TO INPUT OR OUTPUT BUFFER		D1000770	
			80	*	REGISTERS DESTROYED:NONE		D1000780	
			81	*	SUBROUTINE OUTPUT DATA STORED IN MEMORY LOCATION SPECIFIED BY POINTER		D1000790	
			82	*	DTAPTR,IF IOIND=0 OPERATION IS A READ OTHERWISE IT IS A WRITE		D1000800	
			83	*			D1000810	
002ER	0866		84	DIGITIO	LDAI	IOIND,IOIND	CHECK THE I/O INDICATOR FLAG	D1000820
* 0030R	2334		85		BZ	READIN	BRANCH TO READ OPERATION	D1000830
0032R	D847	0000	86		WH	OUTDEV,0(DTAPTR)	WRITE A HALFWORD FROM OUTBUFFER	D1000840
* 0036R	2303		87		R	RETURN		D1000850
0038R	D957	0000	88	READIN	RH	INDEV,0(DTAPTR)	READ A HALFWORD INTO INPUT BUFFER	D1000860
003CR	030F		89	RETURN	BR	RETN	RETURN TO THE USER.	D1000870
			90	*				D1000880

SENSE-STATUS PROGRAMMING EXAMPLES

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92 * IN THIS EXAMPLE THE DATA TRANSFERS ARE SYNCHRONIZED WITH THE CONTROL-
93 * LER THROUGH THE USE OF HANDSHAKING SIGNALS ASSOCIATED WITH THE DEVICE
94 * A COMPLETE DESCRIPTION OF THE BUSY STATUS IS INCLUDED IN SECTION 4
95 *
96 *
003ER C890 00F0 97 DIOENTR1 LDAI WK1,X*F0* SELECT REGISTER SET X*F*
0042R 95A9 98 EPSK RETRY,WK1 EXCHANGE PROGRAM STATUS
0044R 4840 010AR 99 LH OUTDEV,DEVADR1 GET THE OUTPUT DEVICE ADDRESS
0048R DE40 0112K 100 OC OUTDEV,DISARM DISARM SYSTEM INTERRUPTS
004CR 4850 010CR 101 LH INDEV,DEVADR2 GET THE INPUT SYSTEM DEVICE ADDRESS
0050R DE50 0112K 102 OC INDEV,DISARM DISARM INPUT DEVICE INTERRUPTS
0054R 2461 103 LIS IOIND,1 SET THE I/O IND FOR OUTPUT OP
0056R 9959 104 RHR INDEV,WK1 EXECUTE A READ OPERATION TO INITIA-
105 * LIZE THE DIGITAL I/O STATUS
0058R C870 010ER 106 CONT LDAI DTAPTR,OUTBUFFER GET THE DATA POINTER TO OUTPUT BUFFER
005CR 41F0 0070R 107 BAL RETN,DIGIT101 GO TO DIGITAL I/O ROUTINE FOR OUTPUT
0060R C8A0 0058R 108 LDAI RETRY,CONT GO CHECK IF OP WAS COMPLETED
0064R 41F0 00A0R 109 BAL RETN,CHECK GO TO DIGITAL I/O ROUTINE FOR INPUT
0068R 41F0 0070R 110 BAL RETN,DIGIT101 HALT THE PROCESSOR
006CR C200 0120R 111 LPSW WAIT
112 * SUBROUTINE DIGIT101 FIRST CHECKS TO INSURE THAT BUSY STATUS FROM THE
113 * DESIRED SUBSYSTEM IS ZERO. IF IT IS NOT, THEN THE PERIPHERAL DEVICE
114 * IS NOT READY FOR DATA TRANSFER AND THE SUBROUTINE RETURNS TO THE USER
115 * WITH THE IONTCMP FLAG SET=1. OTHERWISE, THE SUBROUTINE WILL EXECUTE THE
116 * APPROPRIATE READ OR WRITE OPERATION AND INSURE THAT THE BUSY STATUS
117 * WAS SET=1 FOLLOWING THE I/O OPERATION.
118 *
119 * CALLING SEQUENCE: BAL RETN,DIGIT101
120 * INPUT REGISTERS:
121 * OUTDEV=OUTPUT DEVICE ADDRESS(EVEN DEVICE ADDRESS)
122 * INDEV=INPUT DEVICE ADDRESS (ODD DEVICE ADDRESS)
123 * IOIND= INPUT/OUTPUT IDENTIFIER
124 * DTAPTR= POINTER TO INPUT OR OUTPUT BUFFER
125 * REGISTERS DESTROYED: R8=IONTCMP,WK1=R9
126 *
127 *
0070R 0866 128 DIGIT101 LDAR IOIND,IOIND GET THE INPUT/OUTPUT OP IDENTIFIER
* 0072R 2130 129 BNZ WRITEOP IF ITS SET, ITS A WRITE OPERATION.
0074R 4850 010CR 130 LH INDEV,DEVADR2 OTHERWISE,GET THE INPUT DEV.ADDRESS
0078R 9D5D 131 SSR INDEV,STAT GET THE STATUS OF THE DEVICE
* 007AR 2383 132 BFC BSY,CONT1 IF ITS ZERO,DO THE READ OPERATION
007CR 4300 009CR 133 B EXITINCP OTHERWISE, SET THE I/O NOT COMPLETE
134 * FLAG AND RETURN TO THE USER
0080R D957 0000 135 CONT1 RH INDEV,0(DTAPTR) READ A HALFWORD OF DIGITAL DATA AND
0084R 9D5D 136 SSR INDEV,STAT CHECK INPUT STATUS BUSY SHOULD SET.
0086R 4380 0106R 137 BFC BSY,ERROR IF IT DIDN'T,THE DEVICE IS IN ERROR.
* 008AR 230A 138 B RETURN1 RETURN TO THE USER.
008CR 9D4D 139 WRITEOP SSR OUTDEV,STAT SENSE DEVICE STATUS.
* 008ER 2187 140 RTC BSY,EXITINCP IF THE BUSY BIT IS SET,SET I/O NOT
141 * COMPLETE AND RETURN.
0090R L847 0000 142 CONT2 WH OUTDEV,0(DTAPTR) DO THE WRITE OPERATION.
0094R 9D4D 143 SSR OUTDEV,STAT SENSE DEVICE STATUS
0096R 4380 0106R 144 BFC BSY,ERROR BUSY BIT SHOULD BE SET
* 009AR 2302 145 B RETURN1 RETURN TO THE USER

```

APPENDIX 2 (Continued)

SENSE-STATUS PROGRAMMING EXAMPLES

009CR	2481	146	EXITINCP LIS	IONTCMP,1	SET THE I/O INCOMPLETE FLAG	OIO01440
009ER	030F	147	RETURN1 BR	RETN		OIO01450
		148	*			OIO01460
		149	*			OIO01470
		150	*			OIO01480
		151	*			OIO01490
		152	* SUBROUTINE CHECK INSURES THAT THE I/O OPERATION WAS COMPLETED			OIO01500
		153	* SUCCESSFULLY, IF IT WAS NOT IT WILL RESET THE IONTCMP FLAG AND RETRY			OIO01510
		154	* THE OPERATION. IF IT WAS A SUCCESSFUL OPERATION, THE SUBROUTINE WILL			OIO01520
		155	* INITIALIZE ALL PARAMETERS FOR SUBSEQUENT OPERATIONS			OIO01530
		156	*			OIO01540
		157	* CALLING SEQUENCE: BAL RETN,CHECK			OIO01550
		158	* INPUT REGISTERS: IONTCMP=IONTCMPLETD INDICATOR			OIO01560
		159	*	IOIND=I/O INDICATOR FLAG		OIO01570
		160	*	DTAPTR=DATA POINTER TO INPUT OR OUTPUT BUFFER		OIO01580
		161	*	RETRY= RETRY ADDRESS		OIO01590
		162	*			OIO01600
		163	* REGISTERS DESTROYED:			OIO01610
		164	* IONTCMP= I/O OPERATION NOT COMPLETED FLAG			OIO01620
		165	* DTAPTR= POINTER TO MEMORY BUFFER			OIO01630
		166	* IOIND= I/O INDICATOR			OIO01640
00A0R	0888	167	CHECK	LDAR IONTCMP,IONTCMP	TEST THE IO NOT COMPLETED FLAG	OIO01650
00A2R	2333	168		BZ REINIT	IF IT ZERO,THE PREVIOUS OPERATION	OIO01660
00A4R	0788	169		XAR IONTCMP,IONTCMP	WAS SUCCESSFUL, OTHERWISE RESET THE	OIO01670
00A6R	030A	170		BR RETRY	COMPLETED FLAG TRY AGAIN.	OIO01680
00A8R	C870 0110R	171	REINIT	LDAI DTAPTR,INBUFR	REINITIALIZE THE OUTPUT DATA POINTER	OIO01690
00ACR	0766	172		XAR IOIND,IOIND	RESET I/O FLAG FOR A READ OPERATION	OIO01700
00AER	0788	173		XAR IONTCMP,IONTCMP	RESET I/O NOT COMPLETE FLAG	OIO01710
00B0R	030F	174		BR RETN		OIO01720
00B2R		175		IFZ ADC-2		OIO01730

INTEKRUPT DRIVEN OPERATION-16 BIT PROCESSORS

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177 * THE FOLLOWING EXAMPLE DEMONSTRATES THE USE OF INTERRUPTS IN SYNCHRON-
178 * IZING DATA TRANSFERS.WHEN THE PERIPHERAL DEVICE REQUIRES SERVICING
179 * AN EXTERNAL INTERRUPT IS GENERATED.INTERRUPTS GENERATED BY THE COMMON
180 * DIGITAL I/O CONTROLLER CAN BE ENABLED/DISABLED OR DISARMED,THIS PROC-
181 * ESS IS DESCRIBED IN DETAIL IN SECTION 4 OF THIS DOCUMENT
182 *
183 *
184 *
185 DIOENTR2 LH OUTDEV,DEVADR1 GET THE OUTPUT DEVICE ADDRESS
186          LH INDEV,DEVADR2 GET THE INPUT DEVICE ADDRESS
187          AIS INDEV,1 ADD 1 TO MAKE IT AN ODD ADDRESS
188          XAR WK1,WK1 SET UP LOCORE TO PROCESS
189          STH WK1,NEWPSWST EXTERNAL INTERRUPTS
190          LDAI WK1,EXTINT
191          STH WK1,NEWPSWLC
192          OC OUTDEV,ENABLE ENABLE OUTPUT AND INPUT EXTERNAL
193          OC INDEV,ENABLE DEVICE INTERRUPTS
194          LDAI DTAPTR,OUTBUFFER LOAD THE MEMORY BUFFER POINTERS
195          LDAI DTAPTR1,INBUFFER
196          WH OUTDEV,0(DTAPTR) ONCE THE WRITE HALFWORD IS EXECUTED
197 * A READ SERVICE INTERRUPT IS GENERATED AND THE PROGRAM WILL
198 * CONTINUE PROCESSING INTERRUPTS UNTIL MANUALLY HALTED
199          LPSW WAIT EXECUTED A WRITE SERVICE INTERRUPT
200 * EXTERNAL INTERRUPTS ENTER HERE- WHEN THE PERIPHERAL DEVICE REQUESTS
201 * DATA FROM THE PROCESSOR,THE INTERRUPT IS VECTORED TO WRITEINT, WHEN
202 * THE PERIPHERAL DEVICE IS READY TO SEND DATA TO THE PROCESSOR THE
203 * INTERRUPT IS VECTORED TO READINT WHICH EXECUTES A READ HALFWORD
204 * OPERATION FROM THE DIO INPUT SUBSYSTEM
205 *
206 EXTINT ACKR WK1,STAT ACKNOWLEDGE THE INTERRUPT
207          CLHR WK1,INDEV INPUT DEVICE REQUESTING SERVICE?
208          BE READINT IF YES GO SERVICE IT WITH A READ INT
209          CLHR WK1,OUTDEV IS THE OUTPUT DEVICE REQUESTING SERV
210          BE WRITEINT YES GO SERVICE IT WITH A WRITE
211          B ERROR OTHERWISE ERROR
212 *
213 * REQUESTS TO WRITE TO DIGITAL I/O CONTROLLER ENTER HERE
214 WRITEINT LOAR STAT,STAT TEST THE RETURNED STATUS
215          BNZ ERROR BUSY STATUS NON-ZERO SIGNIFIES ERROR.
216          WH OUTDEV,0(DTAPTR) WRITE DATA TO THE DIO OUTPUT SUBSYS
217          LPSW OLDPSWST RETURN TO THE USING PROGRAM
218 * REQUESTS TO READ DATA FROM THE PERIPHERAL DEVICE ENTER HERE
219 READINT LOAR STAT,STAT IF THE STATUS IS
220          BNZ ERROR NON-ZERO THATS AN ERROR CONDITION
221          RH INDEV,0(DTAPTR1) READ DATA INTO INPUT BUFFER
222          LPSW OLDPSWST
223          ENDC

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INTERRUPT DRIVEN OPERATION-16 BIT PROCESSORS

		267	* ERRORS CAUSE THE MACHINE TO HALT IN THE WAIT STATE WITH	01002660
		268	* INTERRUPTS DISABLED	01002670
0106K	C200 0118R	269	ERROR LPSW ERR ON AN ERROR HALT THE MACHINE WITH LOC	01002680
		270	* POINTING TO ERR	01002690
		327	ELSE	01003300
010AR		328	ENDC	01003310
		329	* MEMORY CONSTANTS, BUFFER AREAS AND COMMANDS	01003320
010AR	0000	330	DEVAUR1 DC X'0'	01003330
010CR	0000	331	DEVAUR2 DC X'0'	01003340
010ER	0000	332	OUTBUFFER DC X'0'	01003350
0110K	0000	333	INBUFFER DC X'0'	01003360
0112K	C040	334	DISARM DC X'C040'	01003370
	0000 0113R	335	ENABLE EQU *-1	01003380
0118R		336	ALIGN 8	01003390
	0000 0118R	337	ERR EQU *	01003400
0118R		338	IFZ ADC-2	01003410
0118R	8000	339	DC X'A000'	01003420
011AR	0118R	340	DC A(ERR)	01003430
		344	ENDC	01003470
0120R		345	ALIGN 8	01003480
	0000 0120R	346	WAIT EQU *	01003490
0120R		347	IFZ ADC-2	01003500
0120R	C000	348	DC X'C000'	01003510
0122R	0120R	349	DC A(WAIT)	01003520
		353	ENDC	01003560
0124R		354	ALIGN 4	01003570
		387	ELSE	01003900
0124R		388	ENDC	01003910
0124R		389	END	01003920

INTERRUPT DRIVEN OPERATION-16 BIT PROCESSORS

NO ERRORS 3 SQUEZ PASSES

CAL 04-01

ARSTOP	0000																				
ADC	0002	6	175	271	338	347	355														
BSY	0008	132	137	140	144																
BUFFLMST	0002																				
CHECK	00A0R	109																			
CONT	0058R	108																			
CONT1	0080R	132																			
CONT2	0090R																				
DEVADR1	010AR	57	99	185																	
DEVADR2	010CR	59	101	130	186																
DIGITIO1	0070R	107	110																		
DIGITIO	002ER	63	66																		
DIOENTR	0000R																				
DIOENTR1	003ER																				
DIOENTR2	00B2R																				
DISARM	0112R	58	60	100	102																
DTAPTR	0007	62	65	86	88	106	135	142	171	194	196	216									
DTAPTR0	0007																				
DTAPTR1	000C	195	221																		
DTAPTR10	000C																				
ENABLE	0113R	192	193																		
ERR	0118R	269	340																		
ERROR	0106R	137	144	211	215	220															
EXITINCP	009CR	133	140																		
EXTINT	00E2R	190																			
IMPTOP	0124R																				
INBUFFR	0110R	65	171	195																	
INDEV	0005	59	60	88	101	102	104	130	131	135	136	186	187	193							
		207	221																		
INDEV0	0005																				
INTDEV	000B																				
IOIND	0006	61	64	64	84	84	103	128	128	172	172										
IONTCMP	0006	146	167	167	169	169	173	173													
LAUC	0001																				
NEWPSWLC	0046	191																			
NEWPSWST	0044	189																			
OLDPSWST	0040	217	222																		
OUTBUFFR	010ER	62	106	194																	
OUTDEV	0004	57	58	86	99	100	139	142	143	185	192	196	209	216							
OUTDEV0	0004																				
PURETOP	0000R																				
READIN	0038R	85																			
READINT	00FAR	208																			
REINIT	00A8R	168																			
RETN	000F	63	66	89	107	109	110	147	174												
RETRY	000A	56	98	108	170																
RETURN	003CR	87																			
RETURN1	009ER	138	145																		
RST00	0000																				
RST01	0001																				

APPENDIX 2 (Continued)

INTERRUPT DRIVEN OPERATION-16 BIT PROCESSORS

RST02	0002													
RST03	0003													
RSTF0	0000													
STAT	000D	131	136	139	143	206	214	214	219	219				
WAIT	0120R	67	111	199	349									
WK1	0009	55	56	97	98	104	188	188	189	190	191	206	207	209
WK2	000E													
WRITEINT	00EER	210												
WRITEUP	008CR	129												

PRG= *NONE* ASSEMBLED BY CAL 03-066R04-01 (32-BIT)

		1	SCRAT			D1000000
		2	TARGT 32			AOC00010
0000001		3	NLSTC			D1000020
		4	NORX3			D1000030
0000001		5	SQCHK			D1000031
		8	ELSE			D1000060
0000001		9	ENDC			D1000080
		10	WIDTH 120			D1000090
0000001		11	SQUEZ			D1000100
		12	CROSS			D1000110
		13	* COPYRIGHT INTERDATA MAY 1975			D1000120
		14	*			D1000130
		15	* THE PROGRAMMING SEQUENCES THAT FOLLOW DEMONSTRATE THE VARIOUS METHODS			D1000140
		16	* OF DATA TRANSFER USING THE DIGITAL I/O CONTROLLER. THE FLOW-			D1000150
		17	* CHARTS IN APPENDIX 2 OUTLINE THE METHODS IMPLEMENTED BELOW. IN THE			D1000160
		18	* FIRST EXAMPLE, DATA IS TRANSFERRED TO AND FROM THE SYSTEM WITHOUT THE			D1000170
		19	* USE OF HANDSHAKING OR INTERRUPT LOGIC. STATUS FROM THE INPUT AND			D1000180
		20	* OUTPUT SUBSYSTEMS IS IGNORED AND SYSTEM INTERRUPTS ARE DISARMED. THE			D1000190
		21	* SUBROUTINE DIGITIO IS CALLED TO EXECUTE DATA TRANSFERS. THE CALLING			D1000200
		22	* ARGUMENTS INCLUDE AN INPUT/OUTPUT OPERATION IDENTIFIER AND A POINTER			D1000210
		23	* TO MEMORY SPECIFYING WHERE DATA IS TO BE RETRIEVED OR STORED.			D1000220
		24	* ALL PROGRAMMING EXAMPLES RUN WITH THE TEST CABLE REFERENCED IN			D1000230
		25	* APPENDIX 6 OF DOCUMENT 06-188A15.			D1000240
		26	* ALL PROGRAMMING EXAMPLES ARE WRITTEN IN CAL COMMON CODE.			D1000250
		27	*			D1000260
		28	* EQUATES AND REGISTER ALLOCATIONS			D1000270
	0000 000D	29	STAT EQU 13	STATUS REGISTER		D1000280
	0000 0004	30	OUTDEV EQU 4	OUTPUT DEVICE ADDRESS		D1000290
	0000 0005	31	INDEV EQU 5	INPUT DEVICE ADDRESS		D1000300
	0000 0006	32	IOIND EQU 6	INPUT-OUTPUT IDENTIFIER		D1000310
	0000 0007	33	DTAPTR EQU 7	POINTER TO INPUT/OUTPUT BUFFER		D1000320
	0000 0008	34	BSY EQU 8	BUSY STATUS FROM DIO CONTROLLER		D1000330
	0000 000C	35	DTAPTR1 EQU 12	INPUT BUFFER POINTER FOR INTERRUPTS		D1000340
	0000 0008	36	IONTCMP EQU 8	I/O NOT COMPLETE FLAG		D1000350
	0000 0009	37	WK1 EQU 9	WORK REGISTER- GENERAL PURPOSE		D1000360
	0000 000A	38	RETRY EQU 10	ADDRESS FOR ERROR RETRY		D1000370
	0000 000B	39	INTDEV EQU 11	INTERRUPTING DEVICE ADDRESS		D1000380
	0000 000F	40	RETN EQU 15	SUBROUTINE RETURN ADDRESS		D1000390
	0000 0040	41	OLDPSWST EQU X'40'	OLD PSW SAVE AREA 16 BIT ONLY		D1000400
	0000 0044	42	NEWPSWST EQU X'44'	NEW PSW STAT ON EXT INT 16 BIT ONLY		D1000410
	0000 0046	43	NEWPSWLC EQU X'46'	NEW PSW LOC EXT INT 16 BIT ONLY		D1000420
	0000 0003	44	RST03 EQU 3	EXECUTIVE REGISTER SET 0 R3		D1000430
	0000 0002	45	RST02 EQU 2	EXECUTIVE REGISTER SET 0 R2		D1000440
	0000 0001	46	RST01 EQU 1	EXECUTIVE REGISTER SET 0 R1		D1000450
	0000 0000	47	RST00 EQU 0	EXECUTIVE REGISTER SET 0 R0		D1000460
	0000 0000	48	RSTF0 EQU 0	REGISTER SET F-REGISTER SET 0		D1000470
	0000 0007	49	DTAPTR0 EQU 7	OUTPUT BUFFER POINTER -REGISTER SET 0		D1000480
	0000 0004	50	OUTDEV0 EQU 4	OUTPUT DEVICE ADDRESS. REG. SET 0		D1000490
	0000 0005	51	INDEV0 EQU 5	REGISTER SET 0 INPUT DEVICE ADDR		D1000500
	0000 000C	52	DTAPTR10 EQU 12	REGISTER SET 0 INPUT BUFFER POINTER		D1000510
	0000 000E	53	WK2 EQU 14	WORK REGISTER 2		D1000520
	0000 0002	54	BUFFLMST EQU 2	BUFFER LIMIT STATUS		D1000530
0000001	E690 00F0	55	DIOENTR LDAI WK1,X'F0'	SELECT REGISTER SET X'F'		D1000540
0000041	95A9	56	EPSR RETRY,WK1	EXCHANGE PROGRAM STATUS		D1000541

000006I	4840	8198	57	LH	OUTDEV,DEVAOR1	GET THE OUTPUT DEVICE ADDRESS	01000542
00000AI	DE40	819C	58	OC	OUTDEV,DISARM	DISARM OUTPUT DEVICE LOGIC.	01000550
00000EI	4850	8192	59	LH	INDEV,DEVAOR2	GET THE INPUT DEVICE ADDRESS	01000560
000012I	DE50	8194	60	OC	INDEV,DISARM	DISARM INPUT DEVICE INTERRUPTS	01000580
000016I	2461		61	LIS	IOIND,1	SET THE I/O INDICATOR FOR DIO OUTPUT	01000590
000018I	E670	818A	62	LDAI	DTAPTR,OUTBUFFER	GET THE POINTER TO THE OUTPUT DATA	01000600
00001CI	41F0	800E	63	BAL	RETN,DIGITIO	CALL THE SUBROUTINE TO WRITE DATA.	01000610
000020I	0766		64	XAR	IOIND,IOIND	RESET THE IO INDICATOR FOR INPUT OP	01000620
000022I	E670	8182	65	LDAI	DTAPTR,INBUFFER	GET POINTER FOR INPUT DATA	01000630
000026I	41F0	8004	66	BAL	RETN,DIGITIO	GO READ THE INPUT DATA	01000640
00002AI	C200	818A	67	LPSW	WAIT	HALT THE MACHINE	01000650
			68	*			01000660
			69	*	SUBROUTINE DIGITIO TRANSFERS 16 BITS OF PARALLEL BINARY DATA EITHER		01000670
			70	*	TO THE DIGITAL I/O SYSTEM OR FROM THE DIGITAL I/O SYSTEM. STATUS LOG-		01000680
			71	*	IC FROM THE CONTROLLER IS IGNORED. AMONG THE CALLING ARGUMENTS ARE AN		01000690
			72	*	INPUT/OUTPUT INDICATOR FLAG,PHYSICAL DEVICE ADDRESS AND A POINTER TO		01000700
			73	*	THE RESPECTIVE INPUT OR OUTPUT DATA BUFFER.		01000710
			74	*			01000720
			75	*	CALLING SEQUENCE: BAL RETN,DIGITIO		01000730
			76	*	INPUT REGISTERS: OUTDEV= OUTPUT DEVICE ADDRESS(EVEN DEVICE ADDR.)		01000740
			77	*	INDEV= INPUT DEVICE ADDRESS (ODD DEVICE ADDRESS)		01000750
			78	*	IOIND= INPUT OUTPUT IDENTIFIER		01000760
			79	*	DTAPTR= POINTER TO INPUT OR OUTPUT BUFFER		01000770
			80	*	REGISTERS DESTROYED:NONE		01000780
			81	*	SUBROUTINE OUTPUT DATA STORED IN MEMORY LOCATION SPECIFIED BY POINTER		01000790
			82	*	DTAPTR,IF IOIND=0 OPERATION IS A READ OTHERWISE IT IS A WRITE		01000800
			83	*			01000810
00002EI	0866		84	DIGITIO	LDAR IOIND,IOIND	CHECK THE I/O INDICATOR FLAG	01000820
*000030I	2334		85	RZ	READIN	BRANCH TO READ OPERATION	01000830
000032I	D847	0000	86	WH	OUTDEV,0(DTAPTR)	WRITE A HALFWORD FROM OUTBUFFER	01000840
*000036I	2303		87	B	RETURN		01000850
000038I	D957	0000	88	READIN	RH INDEV,0(DTAPTR)	READ A HALFWORD INTO INPUT BUFFER	01000860
00003CI	030F		89	RETURN	BR RETN	RETURN TO THE USER.	01000870
			90	*			01000880

SENSE-STATUS PROGRAMMING EXAMPLES

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92 * IN THIS EXAMPLE THE DATA TRANSFERS ARE SYNCHRONIZED WITH THE CONTROL- D1000900
93 * LER THROUGH THE USE OF HANDSHAKING SIGNALS ASSOCIATED WITH THE DEVICE D1000910
94 * A COMPLETE DESCRIPTION OF THE BUSY STATUS IS INCLUDED IN SECTION 4 D1000920
95 * D1000930
96 * D1000940
00003E1 E690 00F0 97 DIOENTR1 LDAI WK1,X*F0 SELECT REGISTER SET X*F, D1000950
000042I 95A9 98 EPSR RETRY,WK1 EXCHANGE PROGRAM STATUS D1000951
000044I 4840 815A 99 LH OUTDEV,DEVADR1 GET THE OUTPUT DEVICE ADDRESS D1000952
000048I DE40 815E 100 OC OUTDEV,DISARM DISARM SYSTEM INTERRUPTS D1000960
00004CI 4850 8154 101 LH INDEV,DEVADR2 GET THE INPUT SYSTEM DEVICE ADDRESS D1000970
000050I DE50 8156 102 OC INDEV,DISARM DISARM INPUT DEVICE INTERRUPTS D1000990
000054I 2461 103 LIS IOIND,1 SET THE I/O IND FOR OUTPUT OP D1001000
000056I 9959 104 RHR INDEV,WK1 EXECUTE A READ OPERATION TO INITIA- D1001010
105 * LIZE THE DIGITAL I/O STATUS D1001020
000058I E670 814A 106 CONT LDAI DTAPTR,OUTBUFFER GET THE DATA POINTER TO OUTPUT BUFFER D1001030
00005CI 41F0 8010 107 BAL RETN,DIGIT101 GO TO DIGITAL I/O ROUTINE FOR OUTPUT D1001040
000060I E6A0 FFF4 108 LDAI RETRY,CONT GO TO CHECK IF OP WAS COMPLETED D1001050
000064I 41F0 8038 109 BAL RETN,CHECK GO TO DIGITAL I/O ROUTINE FOR INPUT D1001060
000068I 41F0 8004 110 BAL RETN,DIGIT101 HALT THE PROCESSOR D1001070
00006CI C200 8148 111 LPSW WAIT D1001080
112 * SUBROUTINE DIGIT101 FIRST CHECKS TO INSURE THAT BUSY STATUS FROM THE D1001090
113 * DESIRED SUBSYSTEM IS ZERO. IF IT IS NOT, THEN THE PERIPHERAL DEVICE D1001100
114 * IS NOT READY FOR DATA TRANSFER AND THE SUBROUTINE RETURNS TO THE USER D1001110
115 * WITH THE IONTCMP FLAG SET=1, OTHERWISE, THE SUBROUTINE WILL EXECUTE THE D1001120
116 * APPROPRIATE READ OR WRITE OPERATION AND INSURE THAT THE BUSY STATUS D1001130
117 * WAS SET=1 FOLLOWING THE I/O OPERATION. D1001140
118 * D1001150
119 * CALLING SEQUENCE: BAL RETN,DIGIT101 D1001160
120 * INPUT REGISTERS: D1001170
121 * OUTDEV=OUTPUT DEVICE ADDRESS (EVEN DEVICE ADDRESS) D1001180
122 * INDEV=INPUT DEVICE ADDRESS (ODD DEVICE ADDRESS) D1001190
123 * IOIND= INPUT/OUTPUT IDENTIFIER D1001200
124 * DTAPTR= POINTER TO INPUT OR OUTPUT BUFFER D1001210
125 * REGISTERS DESTROYED: R8=IONTCMP,WK1=R9 D1001220
126 * D1001230
127 * D1001240
000070I 0866 128 DIGIT101 LDAR IOIND,IOIND GET THE INPUT/OUTPUT OP IDENTIFIER D1001250
*000072I 213D 129 BNZ WRITEOP IF ITS SET, ITS A WRITE OPERATION. D1001260
000074I 4850 812C 130 LH INDEV,DEVADR2 OTHERWISE, GET THE INPUT DEV. ADDRESS D1001270
000078I 905D 131 INDEV,STAT GET THE STATUS OF THE DEVICE D1001290
*00007AI 2383 132 BFC BSY,CONT1 IF ITS ZERO, DO THE READ OPERATION D1001300
00007CI 4300 801C 133 B EXITINCP OTHERWISE, SET THE I/O NOT COMPLETE D1001310
134 * FLAG AND RETURN TO THE USER D1001320
000080I D957 0000 135 CONT1 RH INDEV,0(DTAPTR) READ A HALFWORD OF DIGITAL DATA AND D1001330
000084I 905D 136 SSR INDEV,STAT CHECK INPUT STATUS BUSY SHOULD SET. D1001340
000086I 4380 8086 137 BFC BSY,ERROR IF IT DIDN'T, THE DEVICE IS IN ERROR. D1001350
*00008AI 230A 138 B RETURN1 RETURN TO THE USER. D1001360
00008CI 9D4D 139 WRITEOP SSR OUTDEV,STAT SENSE DEVICE STATUS. D1001370
*00008EI 2187 140 BTC BSY,EXITINCP IF THE BUSY BIT IS SET, SET I/O NOT D1001380
141 * COMPLETE AND RETURN. D1001390
000090I D847 0000 142 CONT2 WH OUTDEV,0(DTAPTR) DO THE WRITE OPERATION. D1001400
000094I 904D 143 SSR OUTDEV,STAT SENSE DEVICE STATUS D1001410
000096I 4380 8076 144 BFC BSY,ERROR BUSY BIT SHOULD BE SET D1001420
*00009AI 2302 145 B RETURN1 RETURN TO THE USER D1001430

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INTERRUPT DRIVEN OPERATION-32 BIT PROCESSORS

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225 *
226 * THE FOLLOWING EXAMPLE DEMONSTRATES THE USE OF INTERRUPTS IN SYNCHRON-
227 * IZING DATA TRANSFERS, USING THE INTERRUPT STRUCTURE OF THE SERIES 32
228 * PROCESSORS. WHEN THE PERIPHERAL DEVICE REQUIRES SERVICING, AN EXTERNAL
229 * INTERRUPT IS GENERATED. THE INTERRUPT IS GENERATED BY THE DIO CONTROLLER
230 * CAN BE DISABLED/ENABLED OR DISARMED BY THE APPROPRIATE PROCESSOR
231 * OUTPUT COMMAND. THIS PROCESS IS DESCRIBED IN DETAIL
232 * IN THE SECTION ENTITLED COMMAND AND STATUS BYTES.
233 *
234 * DIOENTR2 LDAI WK1,X'F0' SELECT REGISTER SET X'F'
235 EPSR RETRY,WK1 EXCHANGE PROGRAM STATUS
236 LH OUTDEV,DEVADR1 GET THE OUTPUT DEVICE ADDRESS
237 LH INDEV,DEVADR2 GET THE INPUT DEVICE ADDRESS
238 LDAR WK1,OUTDEV GET THE OUTPUT DEVICE ADDRESS
239 SLLS WK1,1 MULTIPLY IT BY 2 FOR INDEXING INTO
240 LDAI WK2,WRITEINT LOCORE,GET INT. SERVICE ROUTINE ADDR
241 STH WK2,X'D0'(WK1) STORE INTERRUPT HANDLER ADDRESS
242 LDAR WK1,INDEV GET INPUT DEVICE ADDRESS
243 SLLS WK1,1 MULTIPLY IT BY TWO FOR INDEXING
244 LDAI WK2,READINT IN LOCORE, AFTER STORING THE ADDRESS
245 STH WK2,X'D0'(WK1) OF THE INTERRUPT HANDLER ENABLE DIO
246 OC OUTDEV,ENABLE INPUT AND OUTPUT INTERRUPTS
247 OC INDEV,ENABLE
248 LDAR DTAPTR,OUTBUFFER INITIALIZE THE POINTERS TO THE
249 LDAR DTAPTR1,INBUFFER INPUT AND OUTPUT DATA BUFFERS.
250 STM OUTDEV,RSAVE STUKE REG. SET X'F'
251 WH OUTDEV,0(DTAPTR)
252 LPSW WAIT WAIT WITH INTERRUPTS ENABLED
253 * WRITE SERVICE REQUESTS ENTER HERE:
254 WRITEINT LDAR RST03,RST03 TEST THE INTERRUPTING STATUS
255 BNZ ERROR A NON-ZERO STATUS IS AN ERROR COND.
256 WH OUTDEV,0(DTAPTR0) WRITE DATA TO THE DIO CONTROLLER
257 LM OUTDEV,RSAVE LOAD REG. SET 0: REG.4-REG X'F'
258 LPSWR RST00 RETURN TO USER
259 * READ SERVICE INTERRUPTS ENTER HERE:
260 READINT LDAR RST03,RST03 TEST THE INTERRUPTING STATUS
261 BNZ ERROR A NON-ZERO STATUS IS AN ERROR COND.
262 RH INDEV,0(DTAPTR10) READ DATA FROM THE DIO CONTROLLER
263 LM OUTDEV,RSAVE LOAD REG. SET 0: REG.4-REG X'F'
264 LPSWR RST00 RETURN TO USER
265 ENOC

```

```

0000B2I E690 00F0
0000B6I 95A9
0000B8I 4840 80E6
0000BCI 4850 80E4
0000C0I 0894
0000C2I 1191
0000C4I E6E0 802C
0000C8I 40E9 00D0
0000CCI 0895
0000CEI 1191
0000D0I E6E0 802E
0000D4I 40E9 00D0
0000D8I DE40 80CF
0000DCI DE50 80CB
0000E0I E670 80C2
0000E4I E6C0 80C0
0000E8I D040 8144
0000ECI D847 0000
0000F0I C200 80C4

0000F4I 0833
*0000F6I 213D
0000F8I D847 0000
0000FCI D140 8130
000100I 1800

000102I 0833
*000104I 2136
000106I D95C 0000
00010AI D140 8122
00010EI 1800
000110I

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D1002230
D1002240
D1002250
D1002260
D1002270
D1002280
D1002290
D1002300
D1002310
D1002320
D1002321
D1002322
D1002330
D1002350
D1002360
D1002370
D1002380
D1002390
D1002400
D1002410
D1002420
D1002430
D1002440
D1002450
D1002460
D1002470
D1002520
D1002530
D1002540
D1002550
D1002560
D1002570
D1002571
D1002580
D1002590
D1002600
D1002610
D1002620
D1002621
D1002630
D1002640

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INTERRUPT DRIVEN OPERATION-32 BIT PROCESSORS

		267	* ERRORS CAUSE THE MACHINE TO HALT IN THE WAIT STATE WITH	D1002660
		268	* INTERRUPTS DISABLED	D1002670
000110I	C200 809C	269	ERROR LPSW ERR ON AN ERROR HALT THE MACHINE WITH LOC	D1002680
		270	* POINTING TO ERR	D1002690
000114I		271	IFNZ ADC-2	D1002700

SERIES 32 AUTO-DRIVER CHANNEL-DIGITAL I/O OPERATION

		273	*			DIO02720
		274	*	THE FOLLOWING EXAMPLE DEMONSTRATES THE USE OF THE SERIES 32 AUTO-DRIVER CHANNEL IN EXECUTING DIGITAL INPUT-OUTPUT SYSTEM DATA TRANSFERS.		DIO02730
		275	*	TWO CHANNEL COMMAND BLOCKS ARE ESTABLISHED TO CONTROL WRITE OPERATION AND READ OPERATION RESPECTIVELY. THE LOW CORE INTERRUPT SERVICE POINT		DIO02740
		276	*	ER TABLE IS SET UP WITH THE ADDRESS OF THE CHANNEL CONTROL BLOCKS+1		DIO02750
		277	*	CHANNEL CONTROL BLOCKS ARE SET UP PRIOR TO AUTO-DRIVER SERVICING.		DIO02760
000114I	E690 00F0	280	DIOENTR3	LDAI WK1,X'F0'	SELECT REG. SET X'F'	DIO02770
000118I	95A9	281		EPSR RETRY,WK1	EXCHANGE PROGRAM STATUS	DIO02780
00011AI	4840 8084	282		LH OUTDEV,DEVADR1	GET THE OUTPUT DEVICE ADDRESS	DIO02790
00011EI	4850 8082	283		LH INDEV,DEVADR2	GET THE INPUT DEVICE ADDRESS	DIO02792
000122I	0894	284		LDAR WK1,OUTDEV	GET THE OUTPUT DEVICE ADDRESS	DIO02800
000124I	1191	285		SLLS WK1,1	MULTIPLY IT BY TWO FOR INDEXING	DIO02820
000126I	E6E0 8096	286		LDAI WK2,CCB1	GET THE WRITE CHANNEL CONTROL BLOCK	DIO02830
00012AI	26E1	287		AIS WK2,1	MAKE IT ODD	DIO02840
00012CI	40E9 00D0	288		STH WK2,X'D0'(WK1)	STORE IT IN THE INTERRUPT SERVICE	DIO02850
		289	*		TABLE	DIO02860
000130I	0895	290		LDAR WK1,INDEV	SIMILIARLY SET UP LOW CORE TO	DIO02870
000132I	1191	291		SLLS WK1,1	SERVICE READ OR INPUT SERVICE INTRPT	DIO02880
000134I	E6E0 80A0	292		LDAI WK2,CCB2	GET THE WRITE CHANNEL CONTROL BLOCK	DIO02890
000138I	26E1	293		AIS WK2,1	MAKE IT ODD	DIO02900
00013AI	40E9 00D0	294		STH WK2,X'D0'(WK1)	AND STORE IT IN LOW CORE	DIO02910
		295	*			DIO02920
00013EI	E690 8054	296		LDAI WK1,WRITERM	LOAD ADDRESS OF WRITE TERMINAL	DIO02930
000142I	4090 808E	297		STH WK1,SUBADR	SUBROUTINE IN THE WRITE CHANNEL	DIO02940
000146I	E690 40D0 FF85	298		LDAI WK1,X'FF85'	CONTROL BLOCK- STORE WRITE CHANNEL	DIO02950
00014CI	4090 8070	299		STH WK1,CCB1	COMMAND WORD IN THE WRITE CHANNEL	DIO02960
000150I	E690 809C	300		LDAI WK1,OTBFFRS	CONTROL BLOCK.	DIO02970
000154I	E6E0 80B7	301		LDAI WK2,OTBFFRE	GET THE OUTPUT BUFFER END ADDRESS	DIO02980
000158I	50E0 8068	302		ST WK2,BUFEND	STORE IT IN THE WRITE CONTROL BLOCK	DIO02990
00015CI	089E	303		SR WK1,WK2	CALCULATE THE BUFFER BYTE COUNT	DIO03000
00015EI	4090 8060	304		STH WK1,BUFCOUNT	STORE RESULT IN THE CONTROL BLOCK.	DIO03010
000162I	E690 8036	305		LDAI WK1,READTERM	LOAD ADDRESS OF THE READ TERMINAL	DIO03020
000166I	4090 8082	306		STH WK1,SUBADR1	SUBROUTINE AND STORE IT IN THE READ	DIO03030
		307	*		CONTROL BLOCK.	DIO03040
00016AI	E690 40D0 FF81	308		LDAI WK1,X'FF81'	LOAD THE CHANNEL COMMAND WORD.	DIO03050
000170I	4090 8064	309		STH WK1,CCB2	STORE IT IN THE READ CONTROL BLOCK.	DIO03060
000174I	E690 8098	310		LDAI WK1,INBUFFRS	GET THE INPUT BUFFER START ADDRESS	DIO03070
000178I	E6E0 80B3	311		LDAI WK2,INBUFFRE	GET THE INPUT BUFFER END ADDRESS.	DIO03080
00017CI	50E0 805C	312		ST WK2,BUFEND1	STORE IT IN THE CONTROL BLOCK	DIO03090
000180I	089E	313		SR WK1,WK2	CALCULATE THE BYTE COUNT	DIO03100
000182I	4090 8054	314		STH WK1,BUFCONT1	STORE IT IN THE CONTROL BLOCK.	DIO03110
000186I	DE40 8021	315		OC OUTDEV,ENABLE	ENABLE OUTPUT INTERRUPTS	DIO03120
00018AI	DE50 801D	316		OC INDEV,ENABLE	ENABLE INPUT INTERRUPTS	DIO03130
00018EI	095C 00D0	317		RH INDEV,0(DTAPTR1)	PERFORM READ OP TO GEN FIRST INTRPT	DIO03140
000192I	C200 8022	318		LPSW WAIT	WAIT WITH INTERRUPTS ENABLED	DIO03200
		319	*	WRITE TERMINAL SUBROUTINE ADDRESS		DIO03210
		320	*		SENSE STATUS ON OUTPUT DEVICE	DIO03220
000196I	4320 FF76	321		WRITERM RFC BUFLMST,ERROR	IF NOT BUFF LIMIT STATUS ERROR	DIO03230
00019AI	1800	322		LPSWR RST00	RETURN TO THE USER	DIO03240
		323	*	READ TERMINAL SUBROUTINE		DIO03250
		324	*			DIO03260
00019CI	4320 FF70	325		READTERM BFC BUFLMST,ERROR	IF NOT BUFFER LIMIT STATUS	DIO03270
0001A0I	1800	326		LPSWR RST00	ITS IN ERROR	DIO03280
						DIO03290

SERIES 32 AUTO-DRIVER CHANNEL-DIGITAL I/O OPERATION

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		328	ENDC		D1003310
		329	* MEMORY CONSTANTS, BUFFER AREAS AND COMMANDS		D1003320
0001A2I	0000	330	DEVADR1 DC X'0'	OUTPUT DEVICE ADDRESS	D1003330
0001A4I	0000	331	DEVADR2 DC X'0'	INPUT DEVICE ADDRESS	D1003340
0001A6I	0000	332	OUTBUFFER DC X'0'	OUTPUT BUFFER	D1003350
0001A8I	0000	333	INBUFFER DC X'0'	INPUT BUFFER	D1003360
0001AAI	C040	334	DISARM DC X'C040'	DISARM INTERRUPTS (DIO CONTROLLER)	D1003370
	0000 01ABI	335	ENABLE EQU *-1	ENABLE DIO INTERRUPTS	D1003380
0001B0I		336	ALIGN 8		D1003390
	0000 01B0I	337	ERR EQU *		D1003400
		341	ELSE		D1003440
0001B0I	0000 80F0	342	DC Y'80F0'	32 BIT PSW STATUS WAIT STATE	D1003450
0001B4I	0000 01B0I	343	DC A(ERR)	32 BIT PSW LOC ON ERROR HALT	D1003460
0001B8I		344	ENDC		D1003470
0001B8I		345	ALIGN 8		D1003480
	0000 01B8I	346	WAIT EQU *		D1003490
		350	ELSE		D1003530
0001B8I	0000 C0F0	351	DC Y'C0F0'	32 BIT PSW STATUS WAIT STATE	D1003540
0001BCI	0000 01B8I	352	DC A(WAIT)	INTERRUPTS ENABLED LOC=WAIT	D1003550
0001C0I		353	ENDC		D1003560
0001C0I		354	ALIGN 4		D1003570
0001C0I		355	IFNZ ADC-2		D1003580
		356	* THE FOLLOWING CHANNEL COMMAND BLOCKS CONTROL THE DIO INPUT OR OUTPUT		D1003590
		357	* REQUESTS AND PROVIDE THE USER WITH AN EXAMPLE OF ESTABLISHING THE		D1003600
		358	* CONTROL PARAMETERS		D1003610
0001C0I	0000	359	CCB1 DC H'0'	CCW WORD- WRITE IN THE FAST MODE	D1003620
0001C2I	0000	360	BUFCOUNT DC H'0'	WRITE OUTPUT BUFFER COUNT	D1003630
0001C4I	0000 0000	361	BUFEND DC F'0'	END ADDRESS OF BUFFER	D1003640
0001C8I	0000	362	CHECK1 DC H'0'	CHECK BYTE	D1003650
0001CAI	0000	363	BUF1CNT DC H'0'	BUFFER 1 COUNT	D1003660
0001CCI	0000 0000	364	BUF1END DC F'0'	BUFFER 1 END ADDRESS	D1003670
0001D0I	0000 0000	365	TABLE DC F'0'	ADDRESS OF TRANSLATION TABLE	D1003680
0001D4I	0000	366	SUBADR DC H'0'	ADDRESS OF TERMINATION SUBROUTINE	D1003690
		367	*		D1003700
		368	*		D1003710
		369	*		D1003720
		370	ALIGN 4		D1003730
0001D8I		371	CCB2 DC H'0'	CCW WORD- READ IN THE FAST MODE	D1003740
0001DAI	0000	372	BUFCONT1 DC H'0'	READ INPUT BUFFER COUNT	D1003750
0001DCI	0000 0000	373	RUFEND1 DC F'0'	END ADDRESS OF READ BUFFER	D1003760
0001E0I	0000	374	CHECK2 DC H'0'	CHECK BYTE	D1003770
0001E2I	0000	375	BUF1CNT1 DC H'0'	BUFFER1 COUNT	D1003780
0001E4I	0000 0000	376	BUF1END1 DC F'0'	BUFFER1 END ADDRESS	D1003790
0001E8I	0000 0000	377	TABLE1 DC F'0'	ADDRESS OF TRANSLATION TABLE	D1003800
0001ECI	0000	378	SUBADR1 DC H'0'	ADDRESS OF TERMINATION SUBROUTINE	D1003810
0001F0I		379	ALIGN 4		D1003820
0001F0I		380	OTBFFRS DSH 16	16 HALFWORDS OF DIGITAL OUTPUT DATA	D1003830
	0000 020FI	381	OTBFFRE EQU *-1	BUFFER END ADDRESS	D1003840
000210I		382	INBUFFRS DSH 16	16 HALFWORDS OF DIGITAL INPUT DATA	D1003850
	0000 022FI	383	INBUFFRE EQU *-1	BUFFER END ADDRESS	D1003860
000230I		384	ALIGN 4		D1003870
000230I		385	RSAVE DSH 16	REGISTER SAVE AREA FOR INTERRUPT	D1003880
		386	* SUBROUTINE AND AUTO-DRIVER CHANNEL SUBROUTINE		D1003890
		388	ENDC		D1003910

APPENDIX 3 (Continued)

APPENDIX 3 32 BIT DIGITAL I/O PROGRAMMING EXAMPLES

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SERIES 32 AUTO-DRIVER CHANNEL-DIGITAL I/O OPERATION

0002701

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END

DI003920

APPENDIX 3 (Continued)

SERIES 52 AUTO-DRIVER CHANNEL-DIGITAL I/O OPERATION

NO ERRORS 3 SQUEZ PASSES

CAL 04-01

ABSTOP	0000	0000																		
ADC	0000	0004	6	175	271	338	347	355												
BSY	0000	0006	132	137	140	144														
BUF1CNT	0000	01CAI																		
BUF1CNT1	0000	01E2I																		
BUF1END	0000	01CCI																		
BUF1END1	0000	01E4I																		
BUFCNT1	0000	01DAI	314																	
BUFCOUNT	0000	01C2I	304																	
BUFEND	0000	01C4I	302																	
BUFEND1	0000	01DCI	312																	
BUFLMST	0000	0002	321	325																
CCB1	0000	01C0I	286	299																
CCB2	0000	01D8I	292	309																
CHECK	0000	00A0I	109																	
CHECK1	0000	01C8I																		
CHECK2	0000	01E0I																		
CONT	0000	0058I	108																	
CONT1	0000	0080I	132																	
CONT2	0000	0090I																		
DEVADR1	0000	01A2I	57	99	236	282														
DEVADR2	0000	01A4I	59	101	130	237	283													
DIGIT101	0000	0070I	107	110																
DIGIT10	0000	002EI	63	66																
DIOENTR	0000	0000I																		
DIOENTR1	0000	003EI																		
DIOENTR2	0000	00B2I																		
DIOENTR3	0000	0114I																		
DISARM	0000	01AAI	58	60	100	102														
DTAPTR	0000	0007	62	65	86	88	106	135	142	171	248	251								
DTAPTR0	0000	0007	256																	
DTAPTR1	0000	000C	249	317																
DTAPTR10	0000	000C	262																	
ENABLE	0000	01ABI	246	247	315	316														
ERR	0000	01B0I	269	343																
ERROR	0000	0110I	137	144	255	261	321	325												
EXITINCP	0000	009CI	133	140																
IMPTOP	0000	0270I																		
INBUFFER	0000	01A8I	65	171	249															
INBUFFRE	0000	022FI	311																	
INBUFFRS	0000	0210I	310																	
INDEV	0000	0005	59	60	88	101	102	104	130	131	135	136	237	242	247					
			283	290	316	317														
INDEV0	0000	0005	262																	
INTDEV	0000	000B																		
IOIND	0000	0006	61	64	64	84	84	103	128	128	172	172								
IONTCMP	0000	000b	146	167	167	169	169	173	173											
LAUC	0000	0002																		
NEWSWLC	0000	0046																		
NEWSWS1	0000	0044																		

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APPENDIX 3 (Continued)

SERIES 32 AUTO-DRIVER CHANNEL-DIGITAL I/O OPERATION

OLUPSWST	0000	0040																
OTBFRE	0000	020FI	301															
OTBFERS	0000	01F0I	300															
OUTBUFFER	0000	01A6I	62	106	248													
OUTDEV	0000	0004	57	58	86	99	100	139	142	143	236	238	246	250	251			
			257	263	282	284	315											
OUTDEV0	0000	0004	256															
PURETOP	0000	0000P																
READIN	0000	0038I	85															
READINT	0000	0102I	244															
READTERM	0000	019CI	305															
REINIT	0000	00A8I	168															
RETN	0000	000F	63	66	89	107	109	110	147	174								
RETRY	0000	000A	56	98	108	170	235	281										
RETURN	0000	003CI	87															
RETURN1	0000	009EI	138	145														
RSAVE	0000	0230I	250	257	263													
RST00	0000	0000	258	264	322	326												
RST01	0000	0001																
RST02	0000	0002																
RST03	0000	0003	254	254	260	260												
RSTF0	0000	0000																
STAT	0000	0000	131	136	139	143												
SUBADR	0000	01D4I	297															
SUBADR1	0000	01ECI	306															
TABLE	0000	01D0I																
TABLE1	0000	01E6I																
WAIT	0000	0188I	67	111	252	318	352											
WK1	0000	0009	55	56	97	98	104	234	235	238	239	241	242	243	245			
			280	281	284	285	288	290	291	294	296	297	298	299	300			
			303	304	305	306	308	309	310	313	314							
WK2	0000	000E	240	241	244	245	286	287	288	292	293	294	301	302	303			
			311	312	313													
WRITEINT	0000	00F4I	240															
WRITEOP	0000	008CI	129															
WRITERM	0000	0196I	296															

APPENDIX 3 (Continued)

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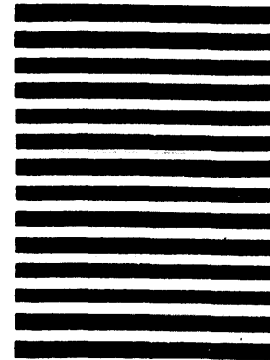
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