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M48·050
BUFFERED SELECTOR CHANNEL
(BSELCH)
MAINTENANCE MANUAL

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FOREWORD

This manual covers the installation and maintenance of the M48-050 Buffered Selector Channel (BSELCH). Chapter 1, Installation, covers the physical characteristics, installation wiring and cabling, and strap options. Chapter 2, Maintenance, contains block diagrams and functional schematic analysis, timing information, installation checks, and a mnemonics list.

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CHAPTER 1
INSTALLATION

1.1 INTRODUCTION

This Chapter provides the necessary information for the installation of the 02-456 Buffered Selector Channel (BSELCH) in a Model 7/32 or 8/32 Processor System. The Buffered Selector Channel is complete on one 35-635 printed circuit board.

1.2 PHYSICAL CHARACTERISTICS

1.2.1 Dimensions

15 3/8" x 14 7/8"

1.2.2 Weight

2½ pounds maximum

1.2.3 Power

6.0 ADC max at 5.0 VDC

1.3 INSTALLATION

The BSELCH may be installed in any even numbered chassis slot (i.e., 0, 2, 4, or 6) of the Extended Direct Memory Access (EDMA) Bus. In a 7/32 Processor, the EDMA Bus starts at either Slot 3 or Slot 7 of the Expansion back panel of the twin chassis. See 02-348A20, 7/32 Memory Access Controller (MAC) Installation Specification for details. For an 8/32 Processor, the EDMA Bus starts at Slot 7 of the I/O Expansion Chassis. The EDMA Bus can be extended to other Expansion chassis through cables but the bus length is limited to eight feet. Seven DMA devices may be installed on the EDMA Bus. The seven devices may all be BSELCHs with no extended memory interfaces or custom DMA devices.

1.3.1 Back Panel Wiring

At installation, it is necessary to cut the Multiplexor Bus wiring between the even numbered slot accepting the BSELCH and the next higher numbered slot on the one (1) connector only. The Receive Acknowledge/Transmit Acknowledge (RACK0/TACK0) "daisy chain" wiring on the back panel is rerouted according to Figure 1-1A. The lower numbered card slots in the chassis become part of the private BSELCH Bus on the one (1) connector only.

To install a BSELCH in Slot 4:

1. Remove all wires from Connector One (1), between Slots 4 and 5, on Pins 11 through 26, Rows 1 and 2 (see back panel map on Functional Schematic 02-456D08, Sheet 1).

2. Remove the wire between 222-0001 and 122-0700.

3. Remove the RACK0/TACK0 jumper between Pins 122 and 222 on both the zero (0) and one (1) connectors and RPC0/TPC0 jumper between Pins 137 and 237 on zero (0) connector of Slot 4.

4. Connect 122-0700 to 222-0501.

5. Install the BSELCH into Slot 4 of the chassis. The private BSELCH Bus now appears on the Connector One (1) side of Slots 4, 3, 2, 1 and 0. All slots on the Connector Zero (0) side and Slots 7, 6, and 5 on Connector One (1) side remain as standard Multiplexor Bus slots.

To install a BSELCH in any other even numbered slot of a universal expansion chassis, a similar procedure is followed. Refer to Figure 1-1 (B, C, D,).

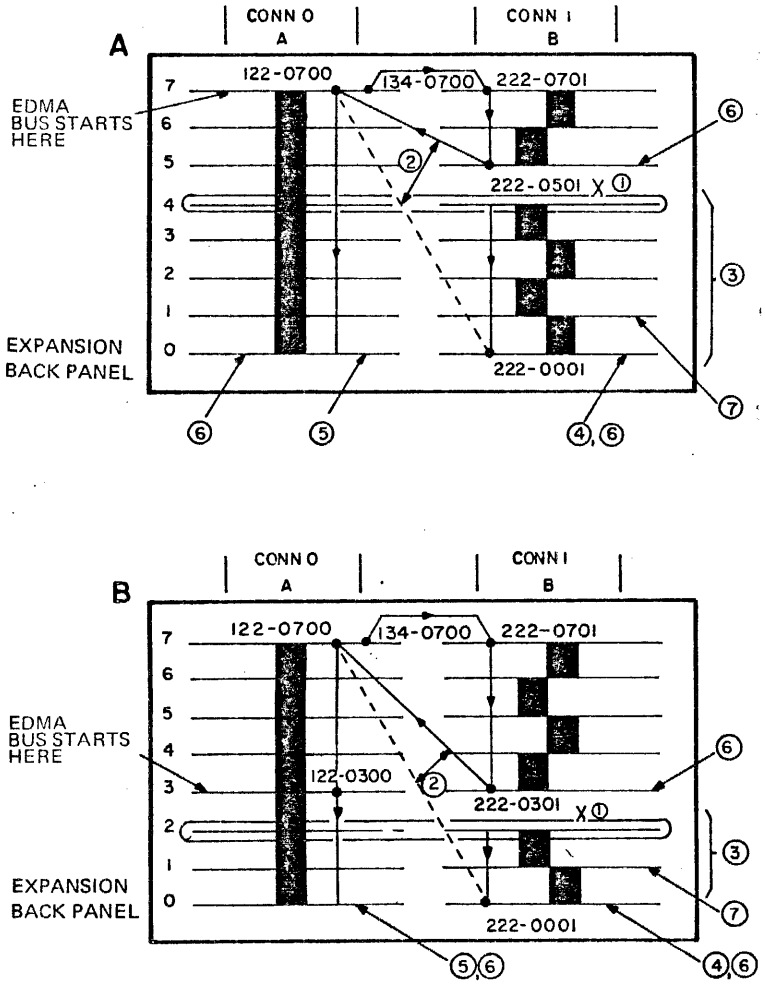
1.3.2 Cabling

The cabling necessary for the BSELCH depends on the systems physical configuration. When the BSELCH Bus does not extend outside the chassis, no cabling is required. When the BSELCH Bus must be extended to another chassis, a number of cable configurations can be used, see Figure 1-2. Care should be taken to minimize bus lengths and not exceed 30 inches (three expansion chassis).

On 7/32 systems, the termination of the 17-312 cable, at Slot 7 or Slot 3, on the Expansion back panel designates the start of the EDMA Bus. Refer to Figure 1-3. If any slot (on the one side) is to be used for a BSELCH, add contiguous wire straps as follows:

Slot 7		Slot 3	
From	129-0701	From	129-0301
To	129-0601	To	129-0201
To	129-0501	To	129-0101
To	129-0401	To	129-0001
To	129-0301		
To	129-0201		
To	129-0101		
To	129-0001		

through the appropriate chassis.



NOTE: THE CIRCLED NUMBERS ON ILLUSTRATIONS A, B, C, D, E, AND F REFER TO THE CORRESPONDING NUMBERS IN THE FOLLOWING INSTALLATION PROCEDURES.

TO INSTALL A SELECTOR CHANNEL IN SLOT 4 OF THE 7/32 EXPANSION BACK PANEL OF THE TWIN CHASSIS OR IN AN 8/32 I/O EXPANSION CHASSIS.

① CUT THE MULTIPLEXOR BUS.

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPER.

③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN 1) SIDE ONLY ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE AND SLOTS 7, 6 AND 5 ON THE CONNECTOR ONE SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑥ INSTALL I/O TERMINATORS 35-433R01 HERE.

⑦ INSTALL EDMA BUS TERMINATOR 35-548 HERE.

TO INSTALL A SELECTOR CHANNEL IN SLOT 2 OF THE 7/32 EXPANSION BACK PANEL OF THE TWIN CHASSIS OR IN AN 8/32 I/O EXPANSION CHASSIS.

① CUT THE MULTIPLEXOR BUS

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPER.

③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

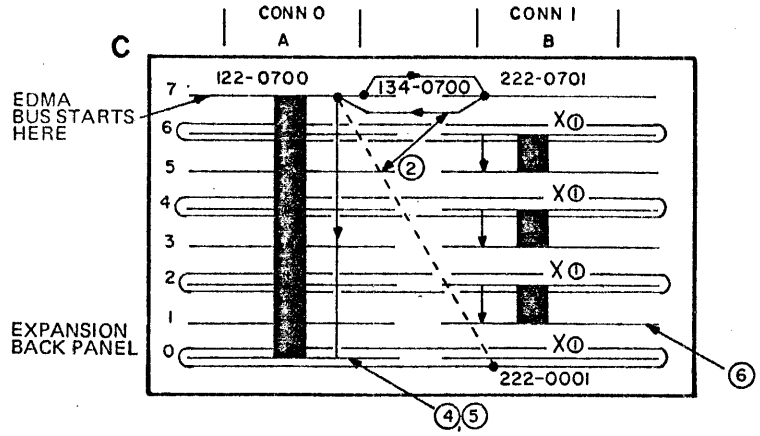
④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑥ INSTALL I/O TERMINATORS 35-433R01 HERE.

⑦ INSTALL EDMA BUS TERMINATOR 35-548 HERE.

Figure 1-1 Backpanel Modifications



TO INSTALL 4 SELECTOR CHANNELS (IN SLOTS 6, 4, 2, AND 0) OF THE 7/32 EXPANSION BACK PANEL OF THE TWIN CHASSIS OR AN 8/32 I/O EXPANSION CHASSIS.

① CUT THE MULTIPLEXOR BUS IN FOUR PLACES.

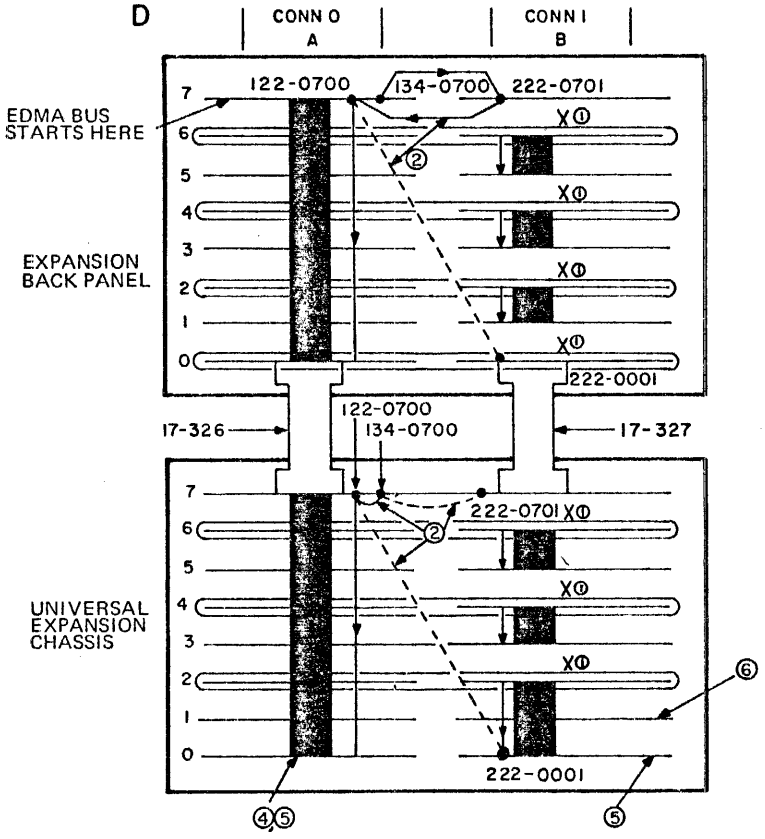
② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPER.

③ EACH SELCH EXCEPT THE ONE IN SLOT 0 HAS ONE SLOT AVAILABLE ON IT'S PRIVATE BUS. THE PRIVATE BUSSES CAN BE EXTENDED TO OTHER CHASSIS BY INSTALLING CABLES IN SLOT POSITIONS 0, 1, 3, AND 5 ON CONNECTOR ONE (CONN1) SIDE.

④ ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE REMAIN AS THE STANDARD MULTIPLEXOR BUS. THIS BUS CAN BE EXTENDED BY INSTALLING A CABLE HERE.

⑤ INSTALL I/O TERMINATOR 35-433R01 HERE.

⑥ INSTALL EDMA BUS TERMINATOR 35-548 HERE.



TO INSTALL 7 SELECTOR CHANNELS IN SLOTS 6, 4, 2 AND 0 OF 7/32 EXPANSION BACK PANEL OF THE TWIN CHASSIS OR AN 8/32 I/O EXPANSION CHASSIS, AND 2, 4, 6 OF EXPANSION CHASSIS.

① CUT THE MULTIPLEXOR BUS IN 7 PLACES.

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPER.

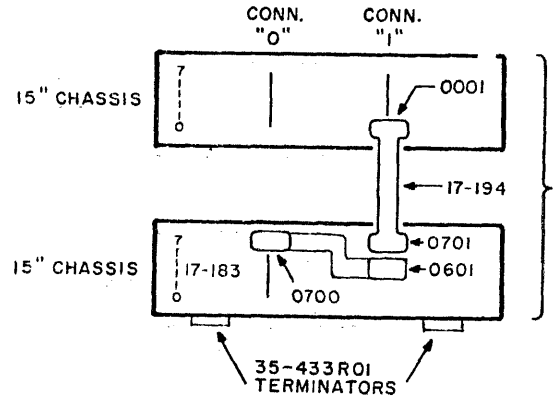
③ EACH SELCH EXCEPT THE ONE IN SLOT 2 OF UNIVERSAL EXPANSION CHASSIS HAS ONE SLOT AVAILABLE ON IT'S PRIVATE BUS. THE PRIVATE BUSSES CAN BE EXTENDED TO OTHER CHASSIS BY INSTALLING CABLES IN SLOT POSITIONS 1, 3, AND 5 OF JUMBO CHASSIS AND 0, 3, 5 OF EXPANSION CHASSIS ON CONNECTOR ONE (CONN 1) SIDE.

④ ALL SLOTS ON THE CONNECTOR ZERO (CONN 0) SIDE REMAIN AS THE STANDARD MULTIPLEXOR BUS. THIS BUS CAN BE EXTENDED BY INSTALLING A CABLE HERE.

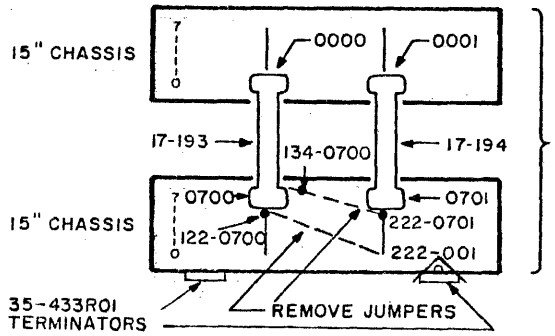
⑤ INSTALL I/O TERMINATORS 35-433R01 HERE.

⑥ INSTALL EDMA BUS TERMINATOR 35-548 HERE.

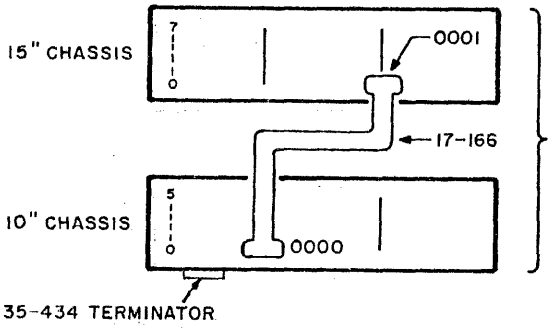
Figure 1-1 Backpanel Modificiations (Continued)



(A) CONNECTS TWO ADJACENT 15" CHASSIS. THE PRIVATE SELCH BUS APPEARS AT BOTH CONNECTORS 0 AND 1 OF THE LOWER CHASSIS. NOTE THE DATA CHANNEL DOES NOT APPEAR IN THE LOWER CHASSIS.



(B) USED TO CONNECT TWO ADJACENT 15" CHASSIS. THE MULTIPLEXOR BUS APPEARS AT CONNECTOR 0, AND THE SELCH BUS APPEARS AT CONNECTOR 1. WHEN USING THIS CONFIGURATION, THE FOLLOWING WIRING CHANGES TO THE RACK0/TACK0 DAISY CHAIN MUST BE MADE TO THE LOWER CHASSIS: REMOVE 134-0700 TO 122-0701 AND 222-0001 TO 122-0700 AND ADD 134-0700 TO 122-0700.



(C) CONNECTS THE PRIVATE SELCH BUS TO A 10" CHASSIS ONE OR TWO CHASSIS AWAY.

Figure 1-2 Cabling

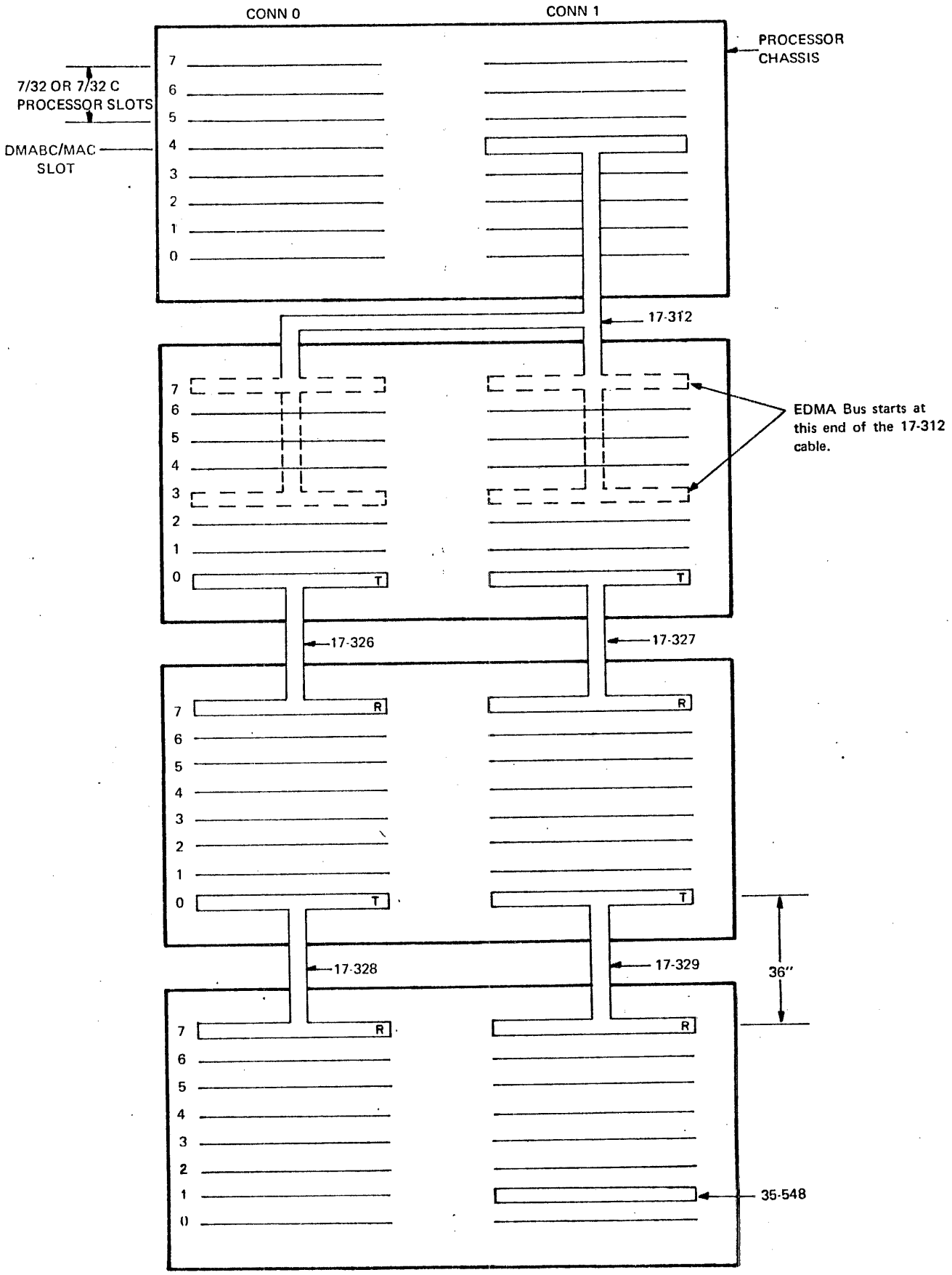


Figure 1-3 DMABC And MAC Back Connections

1.4 BSELCH STRAP OPTIONS

1.4.1 Address Straps

The preferred address of the BSELCH is X'0F0' (10 bit address). The stakes for address strapping are located on Connector 3, at the front of the board (see Figure 1-4). The inner row of pins are marked either 0 or 1. The outer row of pins are marked 06 through 15, corresponding to the 10 bits of address. Strap each address bit to the adjacent 0 or 1 as desired to form the BSELCH address.

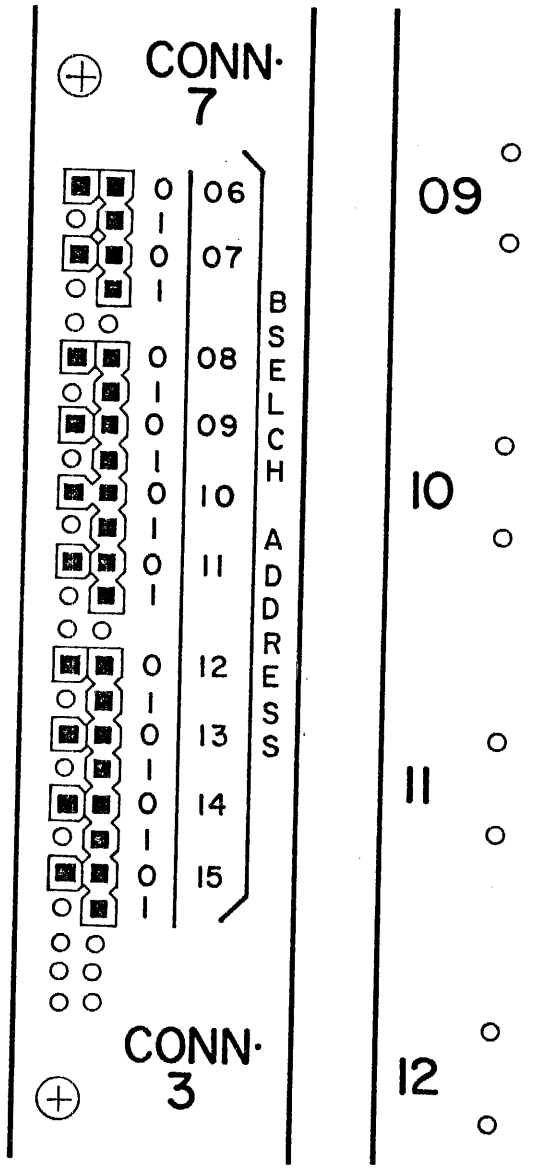


Figure 1-4 Address Strapping

1.4.2 Address Space Allocation

Address space allocation for each of the four memory systems is determined from strap options on the BSELCH. Each memory system's address space must be zero or a multiple of 64K bytes up to a maximum of 1024K bytes for an 8/32 Processor or a maximum of 256K bytes for a 7/32 Processor. Address assignment must be contiguous and the four memory systems are assigned address space in ascending order.

There are two 19-136 decoders on the BSELCH which decode the four most significant address bits. Each output of the decoder allocates 64K bytes of memory. The sixteen outputs (of 64K bytes each) with wire wrap stakes are marked 00 through 15. The five stakes adjacent to them are marked M00, M10, M20, M30 (for the four memory systems) and NON (for all non-existant memory). The address space allocation should be strapped according to system configuration. See Figure 1-5, Address Allocation.

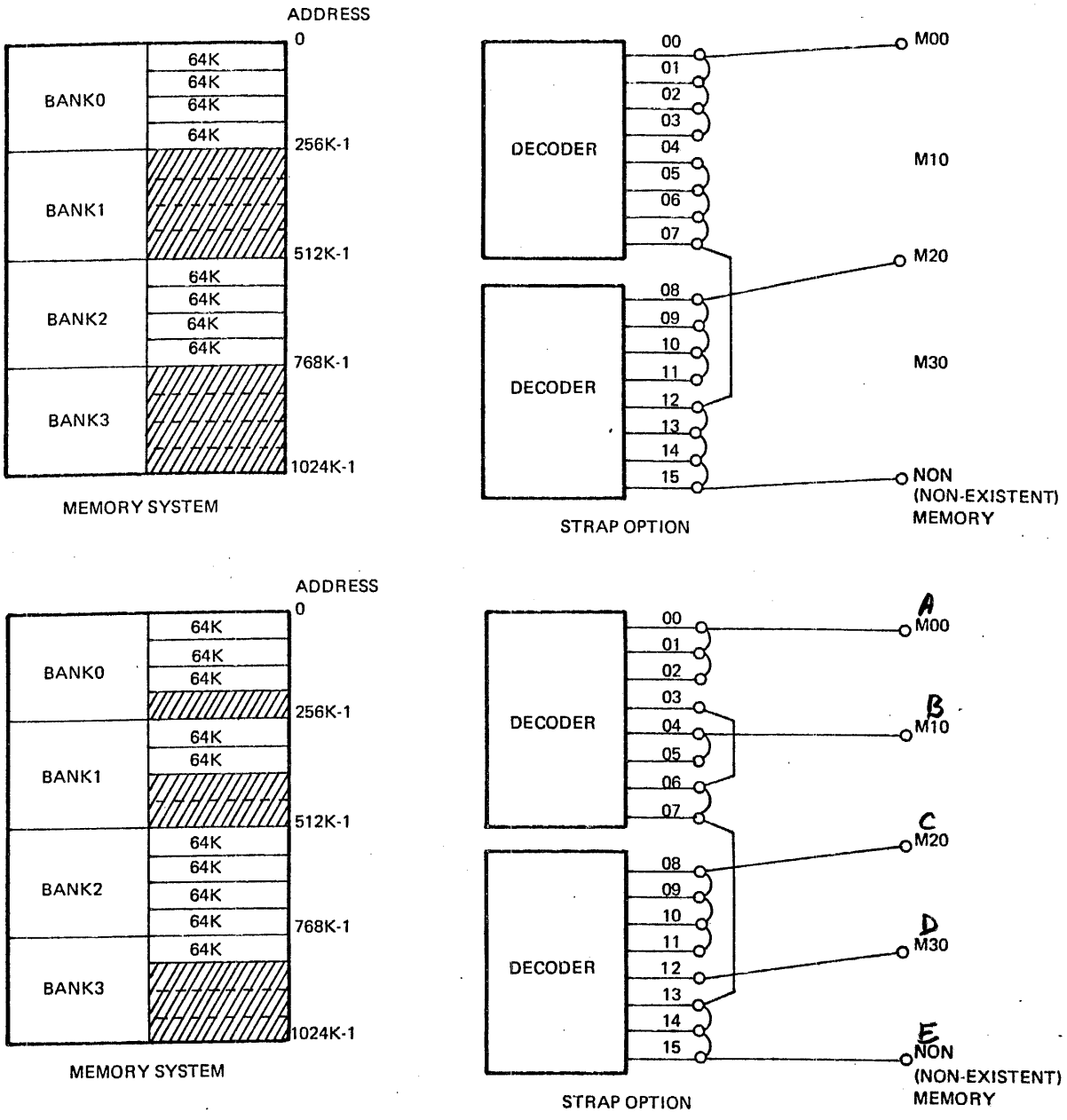


Figure 1-5 Address Allocation

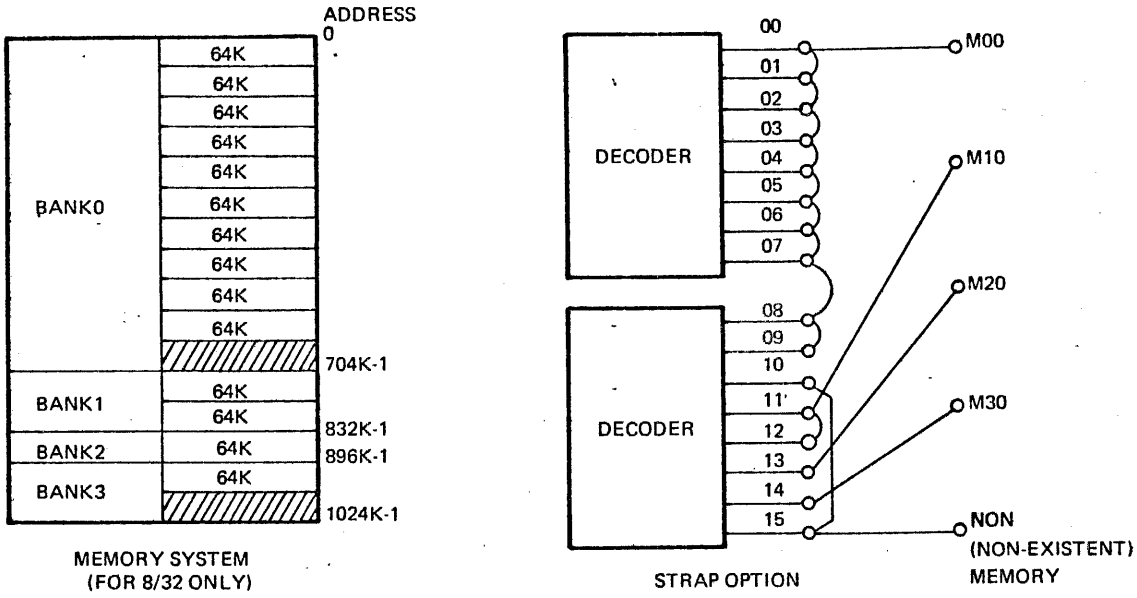


Figure 1-5 Address Allocation (Continued)

1.4.3 Memory Busy Strapping

The three wire wrap stakes marked 7/32, 8/32, and M should be strapped according to processor. Strap 7/32 to M for the Model 7/32 Processor, or strap 8/32 to M for the Model 8/32 Processor.

1.4.4 Burst Size/Mode of Operation Straps

There are six wire wrap stakes on the front of the board marked 0, 1, MODE, and BSTSZ. For a Model 7/32 Processor, the BSELCH *must* operate in the halfword mode. The Model 8/32 may operate in Halfword or Burst mode. Table 1-1 summarizes the strapping for Halfword mode and Burst mode with all possible burst sizes. Burst sizes are given in 1 through 7 fullwords. When strapped for the Halfword Mode, it is imperative that BSTSZ 0, 1, and 2 be strapped to 0.

TABLE 1-1 BURST SIZE/MODE OF OPERATION STRAPS

MODE	BURST SIZE	STRAP 0 TO	STRAP 1 TO
HALFWORD		BSTSZ 0, 1, AND 2	MODE
BURST	1	BSTSZ 0, 1 AND MODE	BSTSZ 2
BURST	2	BSTSZ 0, 2 AND MODE	BSTSZ 1
BURST	3	BSTSZ 0 AND MODE	BSTSZ 1 AND 2
BURST	4*	BSTSZ 1, 2 AND MODE	BSTSZ 0
BURST	5	BSTSZ 1 AND MODE	BSTSZ 0 AND 2
BURST	6	BSTSZ 2 AND MODE	BSTSZ 0 AND 1
BURST	7	MODE	BSTSZ 0, 1 AND 2

*DEFAULT STRAPPING

The burst size is strapped at the factory to suit the system configuration. Parameters such as system throughput requirements and number of contending devices (for the memory) are taken into consideration. The nominal setting of the burst size option is four fullwords. This burst size will accommodate the majority of systems requirements and is the default setting of the option. Should it become necessary to modify the burst size strap option, the following parameters should be considered:

(a) EDMA bus throughput required
(b) Memory system throughput
(c) Number of contending EDMA devices
(d) Device throughput
(e) Device priority

Refer to Figures 2-9 and 2-10, timing diagrams for Burst Mode transfers, in Chapter 2 of this manual. If the burst size is increased, the period of time the BSELCH is transferring data on the EDMA bus is increased. The effect on lower priority devices is to increase the chance of overflow since the lower priority device must wait a longer period of time before its request for memory is acknowledged. Conversely, if the burst size is decreased, the frequency of requests is increased and high speed, high priority devices may dominate the EDMA bus, "locking out" the lower priority device.

1.4.5 Test Straps

The following strap options are available for test purposes. All of these options should be configured "NORMAL" when installing a BSELCH.

TEST FUNCTION	NORMAL STRAP	TEST STRAP
1) DISABLE FIFO	211-5 TO 212-5	210-5 TO 212-5
2) INJECT CLOCK	00D01 TO 00D02	00D02 TO 00D03
3) ADJUST CLOCK	05E34 TO 05E35	05E34 TO 05E36

CHAPTER 2
MAINTENANCE

2.1 INTRODUCTION

The 02-456 Buffered Selector Channel (BSELCH) is a Direct Memory Access (DMA) interface between I/O device controllers and processor memory systems. Once initiated, the BSELCH performs data transfers to or from the memory and the I/O device, independent of processor control. To start the data transfer, the processor sets up the I/O device controller, loads the BSELCH with the starting and final addresses of the data buffer, specifies the type of transfer (Read or Write), and issues a GO command. The BSELCH then performs the data transfer without further direction from the processor. When the transfer is completed, the processor is notified by an interrupt from the BSELCH.

The BSELCH is complete on one 15 inch printed circuit board and occupies one slot in a system chassis. The BSELCH provides the drivers, receivers, and terminators for the private BSELCH bus. The private bus originates at Connector 1 of the BSELCH slot and extends to each slot below it in the systems chassis. The private bus may be extended to other chassis as required.

2.2 Scope

This chapter describes the BSELCH in its various modes: Setup, Memory Read, Memory Write, and Termination. The Multiplexor channel Bus and the Extended Direct Memory Address Bus are referenced. These busses are described in detail in the following Architectural and Product Line standards:

43-009	I/O Interface Design Standards
43-005	Direct Memory Access Bus, Extended Series

2.3 Block Diagram Analysis

Refer to the BSELCH block diagram on Sheet 1 of Functional Schematic 02-456D08. The BSELCH contains a 16 halfword First In First Out memory stack. In the Read mode (Memory Write), data is read from the device and loaded into the FIFO stack. When enough data has been written into the stack to initiate a burst transfer to the memory, the BSELCH requests the memory and writes the data into the block of memory as defined by the address register. In the Write Mode (Memory Read), a request is made to memory for data any time there is room in the stack for the data. When the data has fallen through the stack and appears at the stack outputs, the stack is considered valid and data transfers to the device commence. Transfers to/from memory and transfers to/from the device operate totally independently of each other as long as the stack contains valid data. It is only when the stack is empty or full that one of these operations is inhibited.

Prior to initiation of data transfers via the BSELCH, both the device controller and the BSELCH must be set up. The set up procedure is implemented by the processor via the Multiplexor (MPX) Bus. Refer to the appropriate programming manual for each device controller.

When in the Idle (initialized) state, the MPX bus is tied to the BSELCH private bus and the processor can communicate directly with any device on the private bus. To prepare the BSELCH for data transfers, the starting and final addresses of the memory block must be loaded into the BSELCH address registers. These registers are loaded from the eight least significant Data Lines, D080:150 by four or six consecutive Data Availables (DA0) from the processor. If the memory block to be accessed is within the first 64KB of address, then four bytes may be used to load the address registers. If the memory block is beyond the first 64KB of address, then six bytes must be used to load the address registers. The first two (or three) bytes load the starting address and the last two (or three) bytes load the final address. Data transfers begin when a GO command is issued to the BSELCH by the processor. The GO command begins the data transfers between the active device and memory independent of the processor and inhibits any communication between the processor and the device until termination of the transfers.

Upon termination of the data transfers, the processor is notified by an interrupt and by the inactive state of the BSELCH Busy bit of the status byte. BSELCH status and command byte data are shown in Table 2-1. A description of each bit follows.

TABLE 2-1. BSELCH STATUS AND COMMAND BYTE DATA

BIT NUMBER	8	9	10	11	12	13	14	15
STATUS BYTE			MEMORY MAL-FUNCTION	MEMORY PARITY FAIL	BUSY			
COMMAND BYTE		EXTENDED ADDRESS READ	READ	GO	STOP	SELCH STATUS		

BUSY — This bit is set by command GO. It remains set while the BSELCH is in the process of transferring data. It is cleared by Initialize, Command STOP, normal termination, and error abortion. When this bit is cleared, an interrupt is generated.

MEMORY MALFUNCTION — This bit is set when the memory interface recognizes a malfunction. It is stored in the BSELCH for subsequent evaluation by the processor, however, the transfer is not interrupted. It is cleared by Initialize or Command GO.

MEMORY PARITY FAIL — This bit is set when the memory interface recognizes a parity failure. It is stored in the BSELCH for subsequent evaluation by the processor, however, the transfer is not interrupted. It is cleared by Initialize or Command GO.

READ — This command changes the mode of the BSELCH from Write to Read. In Read mode, data is transmitted from the active device on the BSELCH and written into memory. Whenever a data transmission has been completed, the BSELCH is placed in the Write mode. Each time a Read operation is required, a Read command must be issued.

GO — This command initiates a data transmission. This command can be issued at the same time the Read/Write mode is established.

STOP — This command halts any data transmission in progress, and initializes the BSELCH for starting a new operation. It must be given when the BSELCH terminates.

SELCH STATUS — When this bit is set, the BSELCH status is returned every time on an SR or SS instruction to the BSELCH. When reset, the current SELCH definition applies (i.e., when the BSELCH is idle, the device status is returned with the BUSY bit forced to a zero. When the BSELCH is transferring data, only the BUSY bit is returned. The BSELCH becomes idle only after Initialize or any I/O instruction to the BSELCH is executed).

EXTENDED ADDRESS READ — When this bit is set, the BSELCH returns a three byte final address to the processor if RD or RDR followed by RH or RHR instructions are executed. The most significant byte is returned first. When this bit is reset, the BSELCH returns a two byte final address to the Processor if two successive RD or RDR instructions are executed. The most significant byte is returned first. Before issuing RD or RH instructions to read the final address, a Command STOP must be issued to insure that the BSELCH is in the initialized state.

2.4 Functional Schematic Diagram Analysis

2.4.1 Introduction

This section relates to Functional Schematic 02-456D08, sheets 2 through 15. Note that in INTERDATA functional schematics, the last character in the mnemonic symbol denotes the logic level when the signal is active. For example, D150 is Data Line 15 (D15). The last character (0) indicates that D15 is active at a logical zero level.

With the aid of the schematics and timing diagrams, the following sections describe the circuit operation of the BSELCH when Idle and when Busy.

2.4.2 Idle BSELCH

The BSELCH is in the Idle mode after initialization, or after any I/O instruction to the BSELCH is executed while not busy. The Idle mode is characterized by the state of the following control flip flops.

1. The BSELCH Address (AD1) flip-flop is reset (5J2).
2. The Busy (BSY1) flip-flop is reset (7N7).
3. The Multiplexor-SELCH (MSC1) flip-flop is set (7N8).

The processor MPX bus is tied directly to the BSELCH private bus, allowing the processor to communicate with any device on the BSELCH private bus. This is accomplished by the Idle mode control flip-flops. Control Line Gate (CLG1 = MSC1 · AD0) (6N8), when active, gates the control line multiplexor (6D6) and selects control signals issued by the processor. When inactive, the control signals generated by the BSELCH are selected. Similarly, CLG1 selects Processor Data Lines (D001:071) when active and when inactive selects the outputs of the FIFO stack. These multiplexors (5K5:K8) gate data to the Private Data Lines (PD000:070). BSY1 controls the selection of data for PD080:150. When inactive D081:151 are selected and when active, data from the stack is selected.

When data is being transmitted from the processor to the device, ENBD0 (6L3) is inactive (high), and the bus drivers of the transceivers which gate data onto the MPX bus are disabled. Because ENBD0 is high, when the BSELCH is not busy, ENBPD0 (6M4) is active low. Therefore, data is received at the MPX bus transceivers (6C1:C5) and gated onto the private data lines through the PD transceivers (6L1:L6). Conversely, when data is to be sent from the device to the processor, ENDB0 is low, disabling ENBPD0. The data is received at the PD transceivers and gated onto the MPX bus by the MPX bus transceivers. The select lines of the 8:1 multiplexors (Sheet 8) are inactive, selecting PDR081:151 to be returned to MPX bus.

To communicate with the BSELCH, it must first be addressed. The BSELCH address ('0F0' preferred) is placed on D060:150 and the address control line ADRS0 (6A4) is activated. The data lines are compared to the address for which the BSELCH is strapped (SAD061:151) (5A2:A6) and if there is a match, SADR0 (6F2) is active. The leading edge of ADRS1 sets the BSELCH address flip-flop (AD1) (6J2). When AD1 is active, it prevents processor control signals from passing onto the private bus by holding CLG1 inactive. SADR0 (6A5) also inhibits ADRS0 from passing onto the private bus as PADRS0. This permits the BSELCH to be addressed without resetting the address flip-flop of the active device on the private bus.

2.4.2.1 Address Registers

The starting and final addresses of the memory block must be loaded into the BSELCH before starting a data transfer. Three address registers are used on the BSELCH. The Final Address Register (FAR001:191) (Sheet 9) is loaded with the address of the last location of memory to be accessed. The Memory Address Register (MAR001:181) (Sheet 10) is loaded with the address of the first memory location to be accessed. The MAR is incremented with each memory access and is compared to the FAR. When an address match occurs, the memory transfers are terminated. The Auxiliary Address Register (AAR001:191) (Sheet 11) also is loaded with the address of the first memory location to be accessed. The AAR is incremented with each byte of data transferred to/from the active device and is compared to the FAR. When an address match occurs, transfers to/from the device are terminated.

Figure 2-1 is a block diagram of the data path when loading the address registers. Note that each byte received from the processor is loaded into FAR121:191. With each successive byte received from the processor, the contents of FAR121:191 is loaded into FAR041:111 and FAR041:111 is loaded into AAR121:191 and so on.

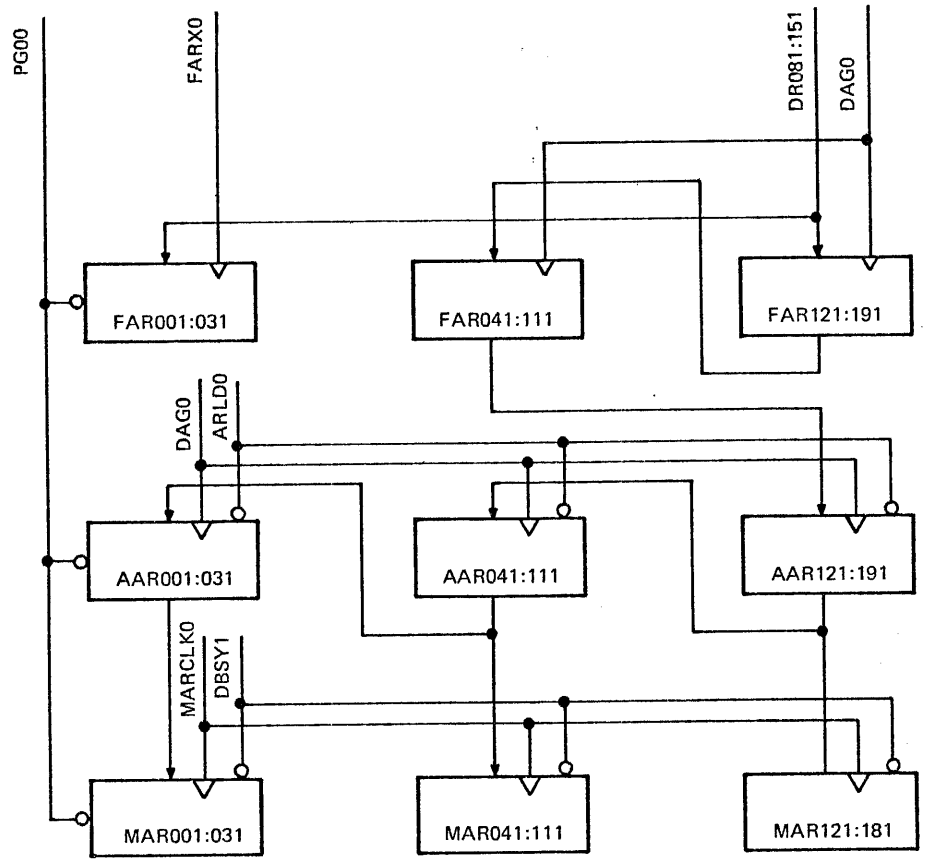


Figure 2-1 Block Diagram Of Data Paths When Loading Address Registers

Table 2-2 summarizes the sequential loading of the address registers when six bytes are used. A 19-035, 4 bit counter (11J5) is used to control the loading and unloading sequence. The counter is preset to a count of '3', and is incremented with each DAG0. The signal LFARX0 (11N4) is active when the fourth byte is written to the BSELCH for loading FAR001:031. ARLD0 (11N4) is active for the first five bytes written to the BSELCH for the purpose of enabling the load input to AAR001:191. If four bytes are used to load the starting and final addresses, PG00 (11N5) becomes active when the processor issues a GO command. PG00 then zeros the most significant four bits of the FAR, AAR and MAR. The MAR is loaded by a direct transfer of AAR001:181 to MAR001:181 when the processor issues a GO command. Figure 2-2 is a timing diagram of the loading sequences for four and six bytes.

TABLE 2-2 FLOW OF DATA THROUGH ADDRESS REGISTERS WHEN LOADING

BYTE	AAR001:031	AAR041:111	AAR121:191	FAR001:031	FAR041:111	FAR121:191
1	X	X	X	X	X	1
2	X	X	X	X	1	2
3	X	X	1	X	2	3
4	X	1	2	4	3	4
5	1	2	3	4	4	5
6	1	2	3	4	5	6

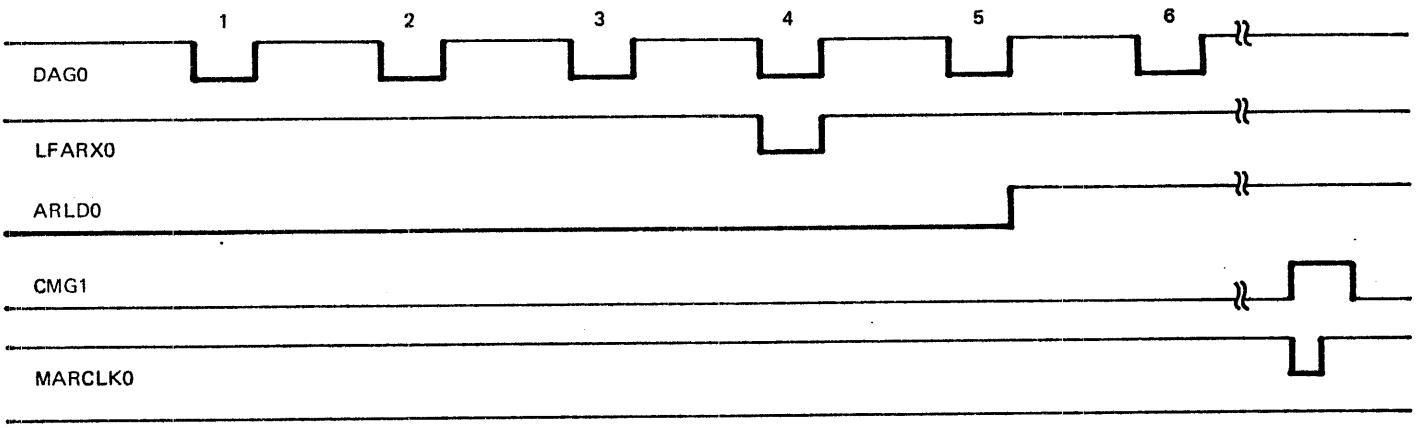


Figure 2-2A Timing Diagram (6 Bytes)

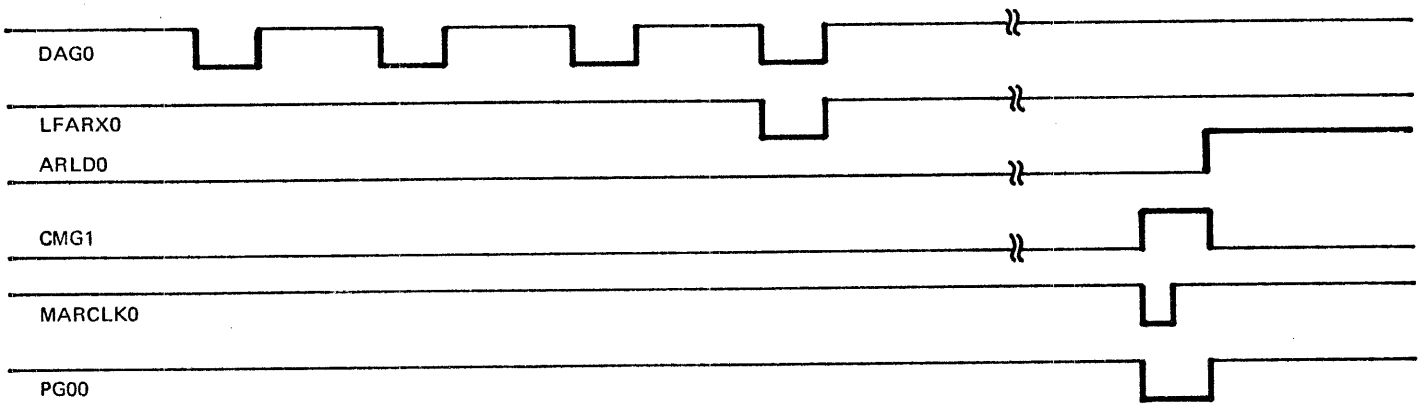


Figure 2-2B Timing Diagram (4 Bytes)

Figure 2-2 Timing Diagram For Loading 4 or 6 Bytes

When the BSELCH terminates, the loader/unloader counter is again preset to a count of '3' and the AAR may be read by the processor. If six bytes were used to load the address registers, the Extended Read (EXRD) bit of the command byte should be set when reading the AAR. The 19-136, 1/10 decoder (11J2) gates the appropriate control to the 8/1 multiplexors (8D6) for reading back the AAR. The AAR is returned to the processor with each successive Data Request, beginning with the most significant byte and ending with the least significant byte. With each DRG0 the counter is incremented and the unload control is changed. Table 2-3 summarizes this operation for reading two and three bytes.

TABLE 2-3 UNLOAD SEQUENCE

BYTE NO.	CNT	EXRD	UNLOAD CONTROL	BYTE RETURNED
1	'3'	0	UAARH0	AAR041:111
2	'4'	0	UAARL0	AAR121:191
1	'3'	1	UAARX0	AAR001:031
2	'4'	1	UAARH0	AAR041:111
3	'5'	1	UAARL0	AAR121:191

2.4.3 Device Data Transfers

2.4.3.1 Data Paths

When the processor issues a GO command to the BSELCH, the trailing edge of Command Gate (CMG1) (6L1) fires a 19-042 one shot resulting in a Command GO pulse (CMDGO1) (7F6). This pulse sets the Busy bit, prevents the processor from communicating with the active device on the private bus, and starts the transfers to the device and to the memory.

In the Read Mode (MWRT1), the Device Data is received at the PD transceivers (Sheets 4 and 5) and is then loaded into an input buffer (3C4:M4). The input buffer is comprised of four 19-187s. These devices are 2:1 multiplexors with storage and are used for temporary storage prior to loading into the 19-200 FIFO stack (3C7:M7). The data is transferred to the stack immediately after loading the input buffer.

In the Write Mode, data is read from the stack and transferred to the device. The stack data (STK001:151) is gated onto the Private Bus at the PD transceivers after passing through the multiplexors. After a halfword has been transferred to the device, STKCLK0 (3A8) updates the stack and the next halfword to be transferred to the device appears at the stack outputs.

2.4.3.2 Control Circuits

When the BSELCH is given an output Command GO, it immediately assumes control of the active device on the private bus and begins data transfers. Each data transfer cycle consists of a Sense Status and a Data Read/Data Write. Device data transfers operate independently of memory transfers, governed only by the status of the FIFO stack. That is, before a write to the device can be done, the stack must be valid, and before a read from the device can be done, the stack must not be full.

2.4.3.2.1 Read Mode

Refer to Figure 2-3, Timing Diagram-Private Bus Control, Read from Device. When the BSELCH is controlling transfers to/from the device, it continuously alternates a status transfer with a data transfer until all data has been transferred to/from the device. When the processor issues a command to GO, CMDGO0 activates the Set Status Transfer (SSX0) (14K4) signal which sets the Status Transfer (SX1) flip-flop (8S8). This activates the Private Status Request (PSR0) control line on the Private Bus. When the device returns the SYNC signal (PSYN0), the BSELCH examines the four least significant bits of the status byte as follows. PSYN1 (8A8) is delayed approximately 50ns to allow the data to settle. The leading edge of Delayed Private SYNC (DPS1) (8F8) is gated with the status returned by the device. If all four bits are reset, meaning the device is not busy and there are no error conditions, the Data Transfer flip-flop (DX1) (8S6) is set and PSR0 is made inactive. When the device releases PSYN0, DPS0 goes high and the Private Data Request (PDR1) (8S6) control line becomes active if the stack is not full. PDR1 also resets the SX1 flip-flop. When the device responds to PDR0 with PSYN0, DPS1 resets the DX1 flip-flop and PDR1 is made inactive, and the device releases PSYN0. The trailing edge of DPS0 fires the End of Data Transfer (EDX1) (15D5) one shot, which in turn activates SSX0 and another cycle is initiated. This process continues until a match (IOMCH1) between the AAR and FAR is detected. IOMCH1 (9J2) inhibits further data transfers by preventing SSX0 from being activated.

The data to be read from the device is received at the PD transceivers and loaded into the input buffer. If the active device performs halfword transfers, then the clock pulses to both halves (high byte and low byte) of the input buffer are made active with the leading edge of DPS1. The least significant bit of the AAR (AAR191) is used for byte steering if the active device is byte oriented. When loading the AAR, it is necessary that AAR191 be zero if the data is to be properly aligned in memory. When AAR191=0, the byte read from the device is loaded into the most significant portion of the input buffer by LDBH0 (15H1). When AAR191=1, the byte read from the device is loaded into the least significant portion of the input buffer by LDBL0 (15H2). Each time LDBL0 is made active, the contents of the input buffer are transferred into the stack by the signal LDSTK1 (15N1). LDSTK1 is a 50ns pulse derived from LDBL0. It is delayed approximately 40ns after the leading edge LDBL0 to allow the data to settle at the stack inputs.

The AAR is incremented with each byte that is transferred. If the active device is byte oriented, the AAR is incremented by the trailing edge of EDX0 (11L5). If the device performs halfword transfers, the AAR is incremented twice within each data tranfer cycle; once by EDX0 and once by the gate (15M6) whose logic is PHW1 · PDAR1 · PSYN0A. Note that when a match is detected, IOMCH0 (11G9) prevents the AAR from changing value by disabling the 19-070 counters.

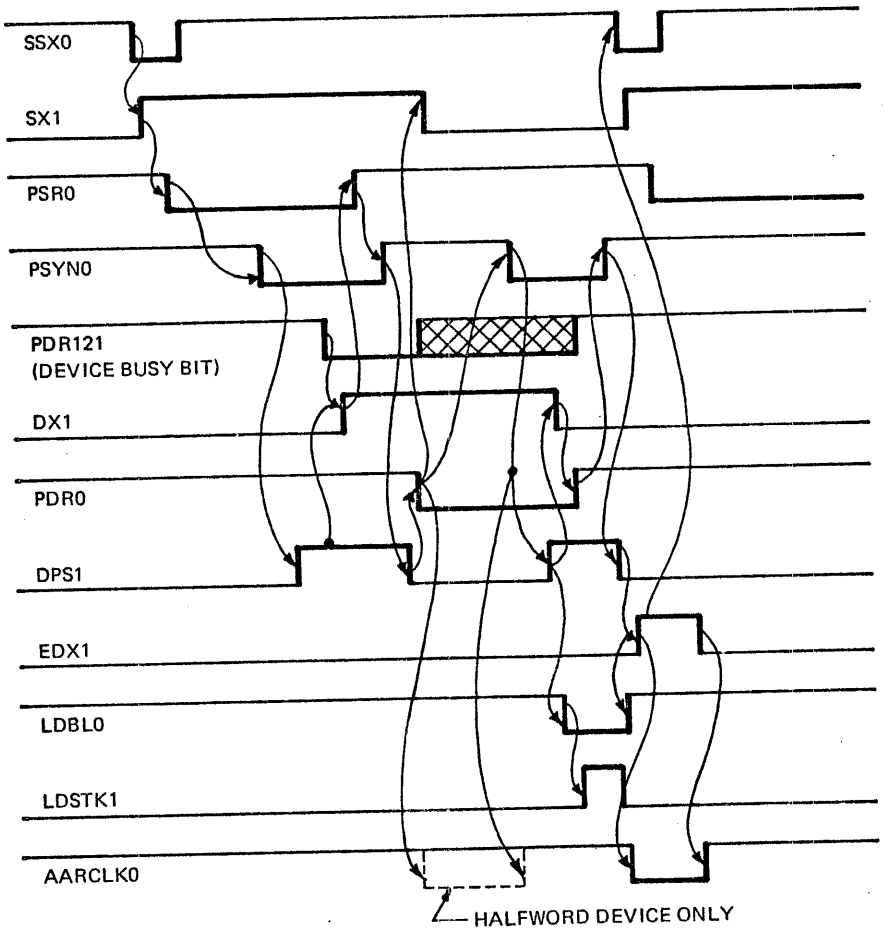


Figure 2-3 Timing Diagram – Private Bus Control
Read From Device

2.4.2.2 Write Mode

Refer to Figure 2-4, Timing Diagram Private Bus Control, Write to Device. The BSELCH Private Bus control circuit operates similar to Read Mode. The differences are described in the following paragraphs. At the end of a status transfer, DPS0 sets the GPD1 (8J9) flip-flop which enables the private data bus transceivers (ENBPD0) (6K4). GPD1 is delayed to permit settling of the data, and then enables the Private Data Available (PDA1) (8S9) control line. When the device returns SYNC, DPS1 resets the DX1 flip-flop, disabling the PDA1 control line. When the device releases the PSYN0 control line, DPS0 fires the EDX1 one shot beginning a new cycle.

Data at the outputs of the stack is changed by the trailing edge of STKCLK0 (15H2). If the active device performs halfword transfers, STKCLK0 is active in every data transfer cycle. If the device is byte oriented, AAR191 is used for byte steering, and the stack outputs are changed after two bytes have been transferred. In either case, STKCLK0 is formed directly from the DPS1 signal.

The AAR is incremented exactly as discussed in the previous section, READ mode.

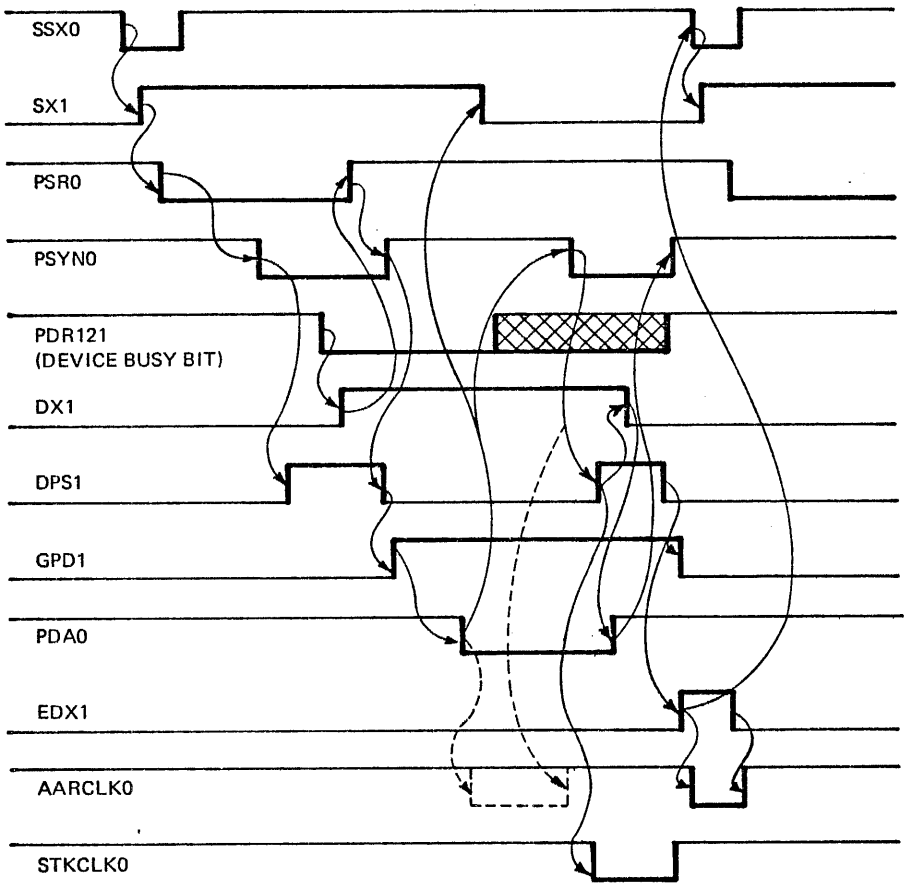


Figure 2-4 Timing Diagram – Private Bus Control
Write To Device

2.4.4 EDMA Bus Transfers

2.4.4.1 Data Paths

In the Write Mode (Memory Read), when the processor issues an Output Command Go, the BSELCH immediately requests access to the memory and proceeds to fill the stack. As data is written to the device and space becomes available in the stack for additional data, the BSELCH again requests the memory to refill the stack. This procedure continues until the MAR matches the FAR (HWMCH0) (10L5) and EDMA transfers terminate. The data read from the memory is received at the EDMA bus transceivers (2G1:G9) and loaded into the input buffer for transfer to the stack.

In the Read mode (Memory Write), data is read from the device and loaded into the stack. When the data has fallen through the stack, the stack is considered valid and data transfers to the memory may begin. The stack outputs are loaded into a high speed data buffer (2B1:B9) which is gated onto the EDMA bus through the transceivers at the appropriate time. When the MAR matches the FAR, the BSELCH terminates.

2.4.4.2 EDMA Bus Control Circuits

The BSELCH performs EDMA bus transfers in either the Halfword Mode or Burst Mode. Mode of operation and Burst Size are strap options. Model 7/32 Processors must operate in the Halfword mode and Model 8/32 Processors may operate in either Halfword or Burst Mode. Refer to Chapter 1, Installation, for strapping instructions.

2.4.4.2.1 Bus Acquisition

When the BSELCH has determined that it is necessary to transfer data to/from memory, the DMARQ1 (14R8) flip-flop is set. This begins a handshake sequence with the processor to acquire the bus for data transfer. This sequence is identical for Burst Mode and Halfword Mode transfers.

Figure 2-5 is a timing diagram of the bus acquisition sequence. The sequence is initiated when the BSELCH activates XREQO (12L6). Before XREQO can be made active, two conditions must be met:

1. The memory system to which a request has been made must not be busy, and
2. The BSELCH must not be selected for transfer.

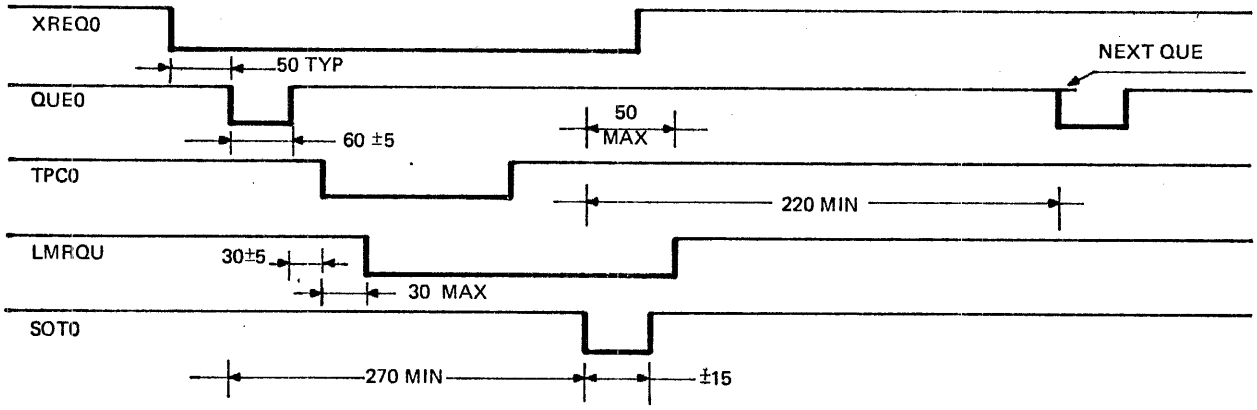


Figure 2-5 Timing Diagram, EDMA Bus Acquisition Sequence

Two 19-136, 1/10 decoders (12C1:C4) monitor the four most significant bits of the MAR. The outputs of these decoders are strapped to define each memory system boundary (M0, M1, M2, and M3) in blocks of 64KB, and all non-existant memory. Refer to Chapter 1, Installation, for strapping instructions. The four bits designating the memory system are encoded to PAGE01 and PAGE11 (12M4). The 19-069 multiplexor (12M2) examines each memory busy signal and PAGE01 and PAGE11 select the appropriate memory busy signal at its output. Therefore, MBZ1 (12N2) always notifies the BSELCH if the memory system to which it is about to transfer is busy. If the BSELCH is not transferring data, the Select flip-flop (SEL1) (12M8) is reset. These conditions, plus the presence of DMARQ1, make the DREQ1 (12L5) gate high and XREQ0 active.

When the processor receives XREQO, it sends a Queue Pulse (QUEO) (12C8) to freeze the request status of all EDMA bus devices. The leading edge of QUEO loads DREQ1 into the first contention flip-flop (12F8) and the trailing edge of QUEO loads the request into the second contention flip-flop. All requesting devices would now have these flip-flops set, and all devices not having a request on the bus would have these flip-flops reset. Next, the processor transmits a Priority Chain Pulse (RPCO) (12C9). The highest priority device which has been queued captures the RPCO pulse and sets the third stage request flip-flop. If the BSELCH has not been queued, RPCO is transmitted to the next device as TPCO (12J9). If the BSELCH is transferring to local memory, M01 (12H2) is high and LMRQO (12K6) (Local Memory Request) is active. Contention being resolved, if the memory is not busy, the processor sends a Start of Transmit (SOT0) (12J9) pulse. SOT0 sets the Select flip-flop and the BSELCH begins transmission.

2.4.4.2.2 Data Transfers

When the BSELCH is selected for data transfer, the internal clock (DMACLK1) (15N8) is activated, starting the control sequences for the data transfer. The control required to implement the data transfer is programmed in two of the 19-199 Programmable Logic Arrays (PLA) and with each DMACLK1 pulse, the PLA outputs are latched (14G1:G8) and the internal program is advanced to the next control state. Figure 2-6 is a Control State Diagram of BSELCH data transfers. There are eight control states used to implement the four types of data transfers. A brief description of each type of transfer follows.

Memory Read, Halfword mode. Refer to Figure 2-7, Timing Diagram, Memory Read, Halfword Mode. The leading edge of SOT0 sets the Select (SEL1) flip-flop, and since the BSELCH is in the idle Control State Zero (CS01), the gate at (15F7) starts DMACLK1. The first transition of DMACLK1 places the BSELCH in Control State One (CS1) where the following control signals become active.

The GADRO (2C2) signal selects the MAR on the multiplexors to the EDMA bus. The ENBDMAO signal (2R1) enables the EDMA bus transceivers. During CS1, the MAR is gated to the EDMA bus. On the next DMACLK1, the BSELCH is placed in CS2 where the MAR is still gated to the bus and two control signals, LOAD0 (2R9) and EOT0 (13R8) are transmitted. Since this is the extent of BSELCH transmission, the next DMACLK1 returns the BSELCH to the idle (CS01) state.

The BSELCH is now waiting for the requested data from the memory. The data is gated to the EDMA bus by the processor and an Answer SYNC pulse (ANS0) is transmitted with the data. To insure that the data is intended for BSELCH, the ANS0 is decoded as follows. When the BSELCH becomes selected, the leading of SEL1 loads the encoded PAGE01 and PAGE11 into a register (13C8) for temporary storage. When the data read from the memory is gated to the EDMA bus, DMX140 and DMX150 are encoded to reflect the memory system from which the data has been sent. These are compared to the stored PAGE01 and PAGE11, and if they are the same, the input to the flip-flop at (13K7) is high. When the answer pulse is received, the leading edge of ANSR1 (13K7) loads this flip-flop and the decoded answer is formed from the RANS0 (13R7) gate.

To insure that the BSELCH does not decode answers intended for other devices, a Wait for Answer (W4ANS1) flip-flop (13R5) is set during Control State One. The W4ANS1 flip-flop is a double rank flip-flop designed to permit two ANS0 signals to be decoded (for Burst mode) prior to resetting the W4ANS1 flip-flop. On the transition to Control State Zero, the Reset Wait for Answer (RW4ANS0) signal (13L6) becomes active. The leading edge of the decoded RANS1 resets the first flip-flop and the trailing edge of RANS0 resets the W4ANS1 flip-flop. When W4ANS1 is low, the Answer SYNC decoding flip-flop is held low, and received answers cannot be decoded.

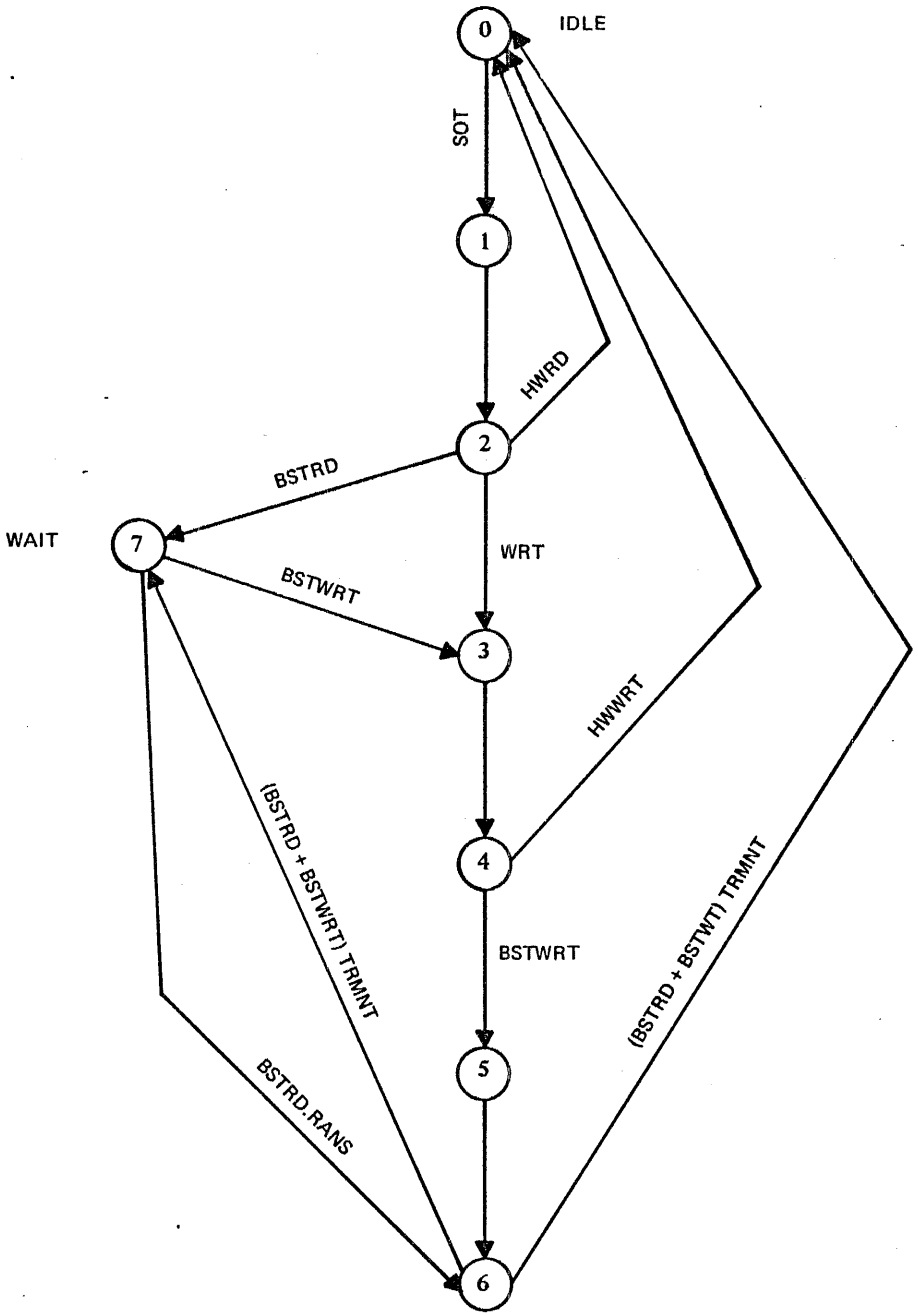


Figure 2-6 Control State Diagram – EDMA Transfers

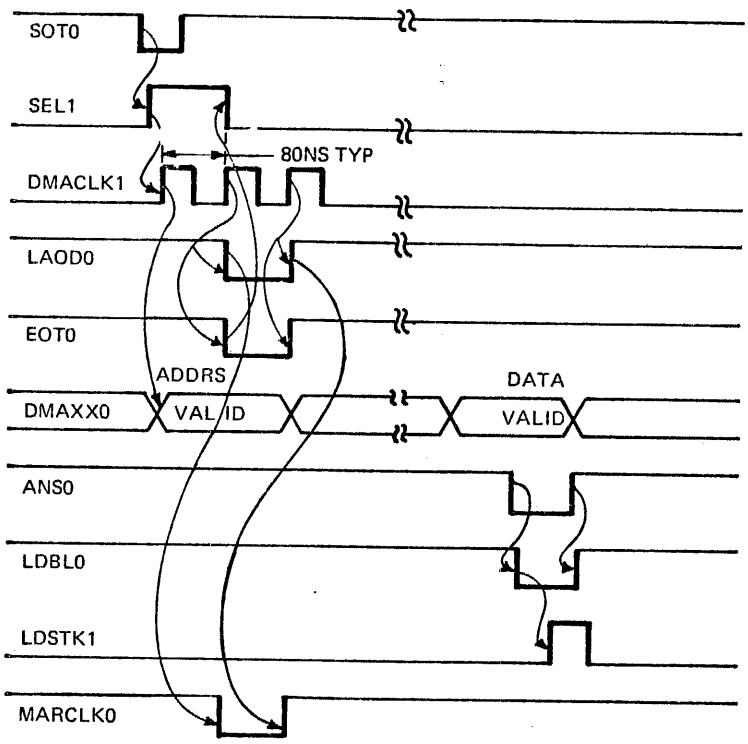


Figure 2-7 EDMA Transfer, Memory Read, Halfword Mode

Memory Write, Halfword Mode. Refer to Figure 2-8, the timing diagram for Memory Write, Halfword Mode. The DMACLK1 is started as previously discussed and the MAR is transmitted in Control States One and Two. On the transition from Control State Two to Control State Three, the contents of the FIF0 stack are loaded into EDMA bus data register (2B1:B9). During Control States Three and Four, GADR0 becomes inactive and the EDMA bus multiplexors gate the data register to the transceivers and onto the EDMA bus. In Control State Two, a LOAD0 is sent with the address and in Control State Four, LOAD0 is sent with the data. Also, during Control State Four, an EOT0 is sent, signaling the End of Transmission. From Control State Four, the BSELCH returns to the Idle Control State Zero.

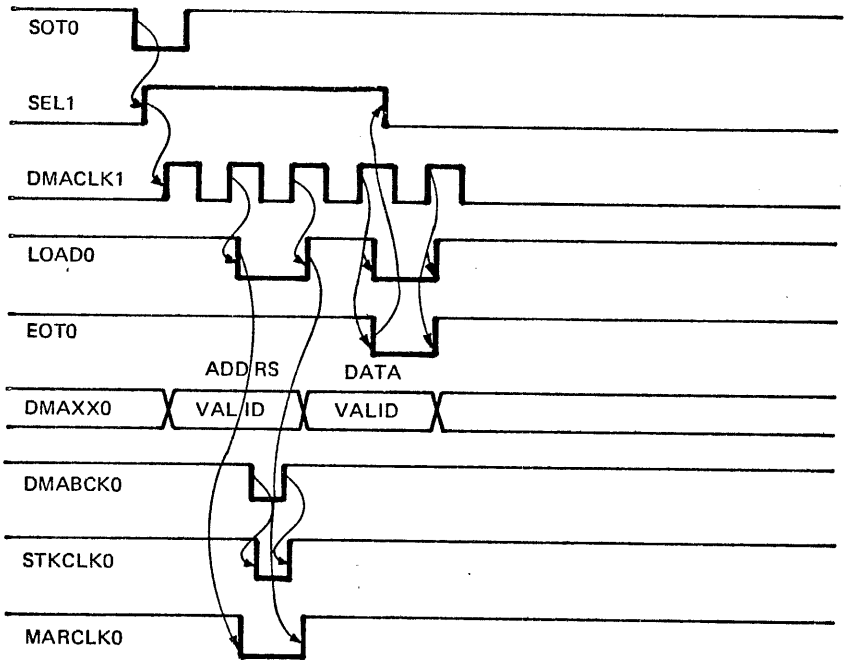


Figure 2-8 EDMA Transfer, Memory Write, Halfword Mode

Memory Read, Burst Mode. Refer to Figure 2-9, Timing Diagram for Memory Read, Burst Mode. The MAR is gated to the EDMA bus in Control States One and Two. In Control State Two, LOAD0 and EOT0 are sent. The W4ANS1 flip-flop has been set, and from Control State Two, the BSELCH proceeds to Control State Seven, a Burst Mode wait state. On the transition to Control State Seven, DINH1 (15E8) becomes active and DMACLK1 is inhibited by the gate at (15F8) until the first ANS0 is received. The leading edge of RANS0 starts DMACLK1, resulting in two clock pulses. The first pulse sends the BSELCH to Control State Six where either a LOAD0 or an EOT0 is transmitted to the processor. In this case, the signal sent is used to notify the processor if additional data is required. If another fullword of data is desired, LOAD0 is sent. If no additional data is desired, EOT0 is sent. If another fullword is requested, the next clock pulse returns the BSELCH to Control State Seven to wait for another pair of ANS0 signals. If the EOT0 is sent, the next clock sends the BSELCH to Control State Zero, terminating the burst transfer. The second ANS0 received would then reset the W4ANS1 flip-flop.

Memory Write, Burst Mode. Refer to Figure 2-10 Timing Diagram for Memory Write, Burst Mode. The address is sent to the processor during Control States One and Two and a LOAD0 is sent with the address in Control State Two. On the transition from Control State Two to Three, the data register is loaded from the stack with the first halfword of the burst transfer. This is gated to the EDMA bus during Control States Three and Four and a LOAD0 is sent during Control State Four. On the transition from Control State Four to Five, the data register is loaded with the second halfword of the burst. This is gated to the bus during Control States Five and Six and a LOAD0 is sent during Control State Six. If this burst transfer is to be terminated, an EOT0 is also sent during Control State Six and the BSELCH returns to the idle state, Control State Zero. If additional data is to be sent, the BSELCH proceeds to Control State Seven, the wait state. The W4ANS1 flip-flop is set and DINH1 inhibits DMACLK1. When the processor sends an ANS0 indicating it is ready to accept additional data, the leading edge of RANS0 starts the clock and the BSELCH proceeds from Control State Seven to Control State Three. During Control States Three, Four, Five, and Six, the next two halfwords are read from the stack, loaded into the data register, and sent to the memory. This procedure continues until the burst is terminated with an EOT0 in Control State Six and the BSELCH returns to Control State Zero.

Termination of a burst transfer (Read and Write) can result from any of the following:

1. End of Burst (EOBST1). The appropriate number of fullwords, as defined by the burst size strap option, have been transferred.

2. Crossing Memory System Boundary (XBNDRY1). The next fullword to be transferred would necessitate crossing a memory system boundary. The BSELCH terminates the transfer and requests access to the memory system into which it has crossed.

3. Address Match (FWMCH0, HWMCH0). The address contained in the MAR matches the final address contained in the FAR. This condition signals an end to all memory transfers.

4. Unusual Conditions (TERM1). There are four other conditions not normally encountered which would force termination of a burst and all other activity (BSELCH returns to Idle Mode).

    (a) Initialize (CLO71).

    (b) STOP Command.

    (c) ACRY0. The AAR has incremented to the largest possible value. This prevents wrap around in memory transfers.

    (d) . NOMEM0. The MAR is pointing to an address of non-existant memory.

The PLA programs are presented in Tables 2-4 and 2-5. Refer to Sheet 14 of the schematics to obtain correlation of the truth table to BSELCH signals. The tables specify the outputs of the PLA with respect to their inputs.

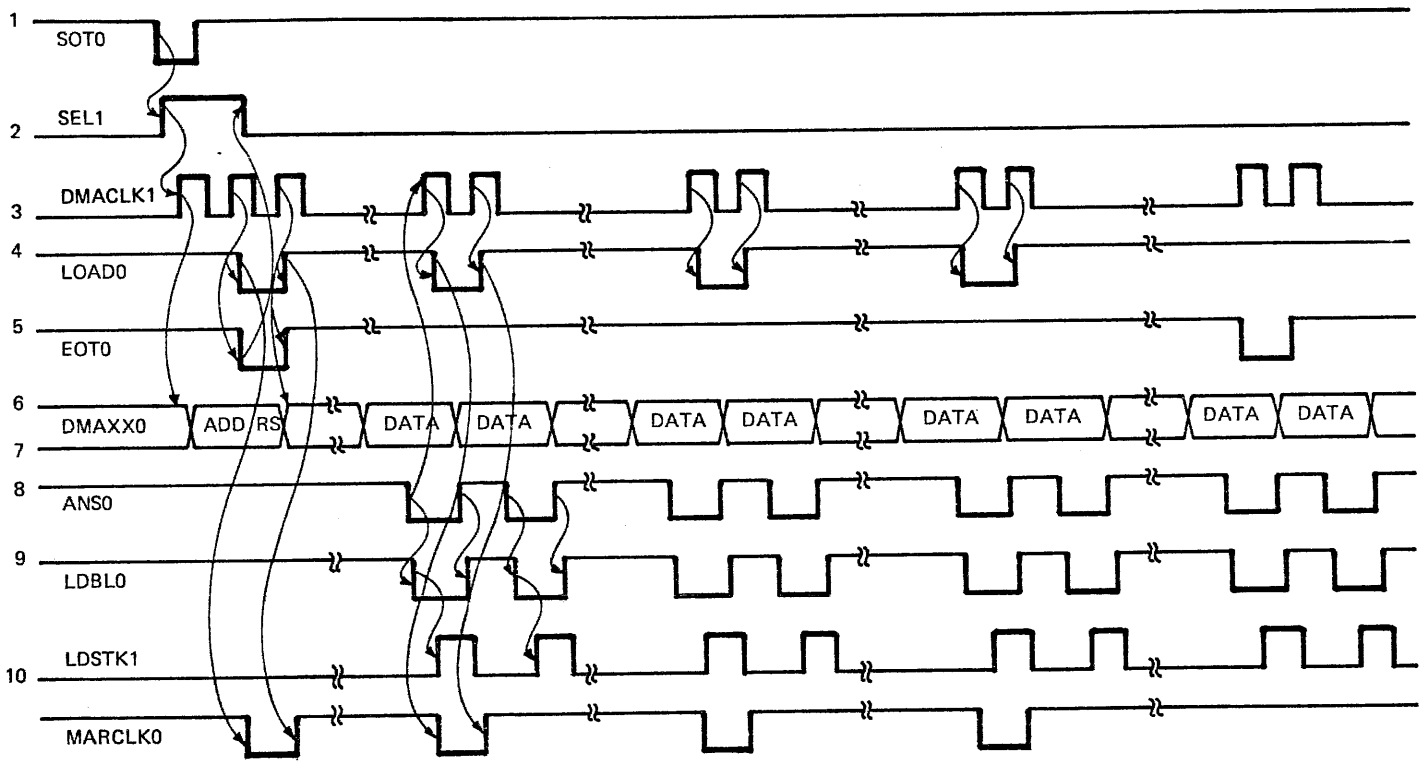
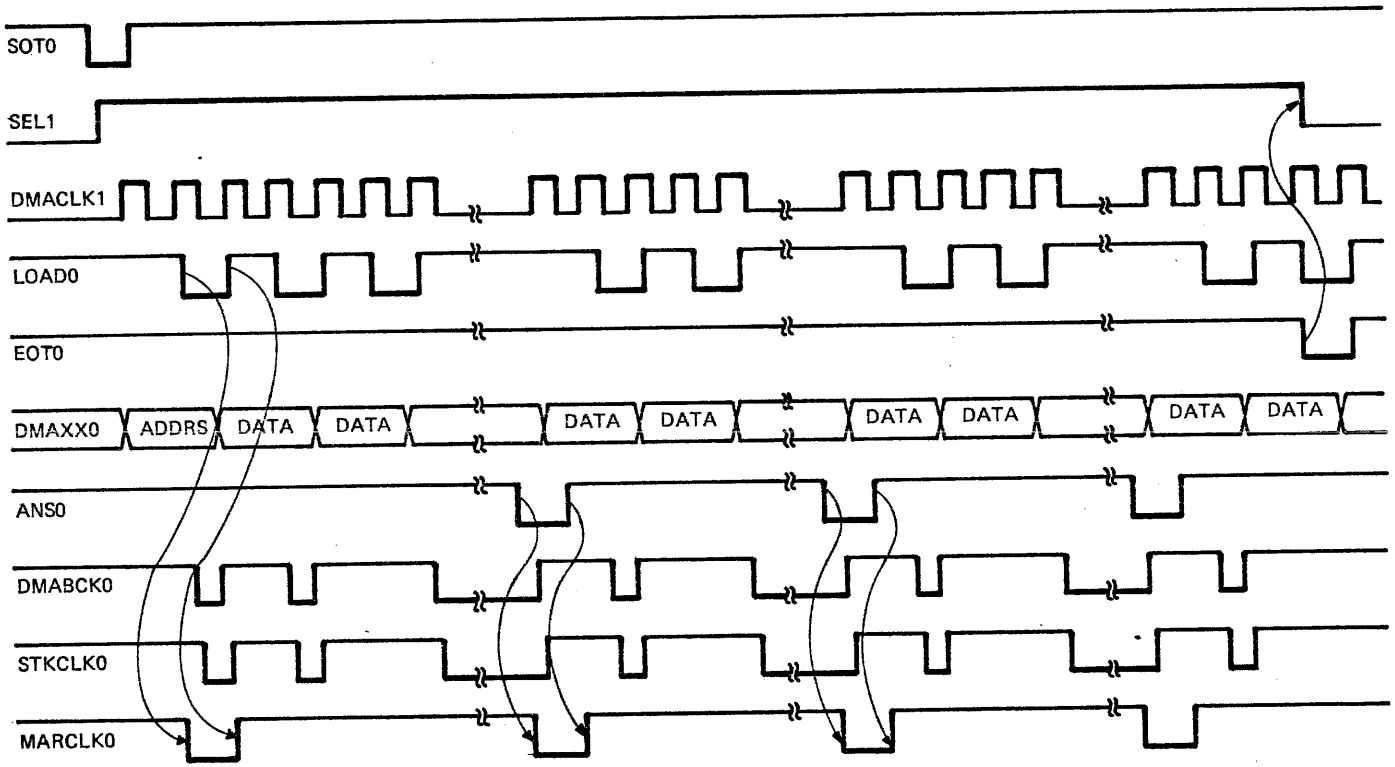


Figure 2-9 EDMA Transfer, Memory Read, Burst Mode



TIMING SHOWN FOR A BURST OF 4 FULLWORDS

Figure 2-10 EDMA Transfer, Memory Write, Burst Mode

TABLE 2-4 PLA PROGRAM TABLE (19-199F01)

PROGRAM TABLE ENTRIES

INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
I_M	I_M	DON'T CARE	PROD TERM PRESENT IN F_P	PROD TERM NOT PRESENT IN F_P	ACTIVE HIGH	ACTIVE LOW
H	L		A		H	L
NOTE: ALL UNUSED INPUTS MUST BE PROGRAMMED AS DON'T CARE			NOTE: OUTPUT FUNCTION ENTRIES ARE INDEPENDENT OF PROGRAMMED OUTPUT PRIORITY		NOTE: OUTPUT PRIORITY PROGRAMMED ONCE ONLY	

PRODUCT TERM																		ACTIVE LEVEL							
	INPUT VARIABLE (1_m)																	H	H	H	H	H	H		
																		OUTPUT FUNCTION							
NO.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	L	L				•	•	•	•	A	A
1	–	–	–	–	–	–	–	–	–	–	–	–	H	–	H	L				•	•	•	•	A	•
2	–	–	–	–	–	–	–	–	–	–	–	L	H	–	L	H				•	•	•	•	A	•
3	–	–	–	–	–	–	–	–	–	–	–	–	H	H	H	H				•	•	•	•	A	•
4	–	–	–	–	–	–	–	–	–	–	–	–	L	H	L	L				•	•	•	A	•	•
5	–	–	–	–	–	–	–	–	–	–	–	L	H	H	L	L				•	•	•	A	•	•
6	–	–	–	–	–	–	–	–	H	L	–	–	–	L	H	H				•	•	A	•	•	•
7	–	–	–	–	–	–	–	L	–	–	–	H	H	L	L	H				•	•	A	•	•	•
8	–	–	–	–	–	–	–	L	–	–	–	H	L	L	L	L				•	A	•	•	•	•
9	–	–	–	–	–	–	–	L	L	–	–	–	L	H	H	H				•	A	•	•	•	•
10	–	–	–	–	–	–	H	L	–	–	–	H	H	L	L	L				•	A	•	•	•	•
11	–	–	–	–	L	H	L	–	–	–	–	H	H	L	L	H				•	A	•	•	•	•
12	–	–	–	–	–	–	H	L	L	–	–	–	H	L	H	H				•	A	•	•	•	•
13	–	–	–	–	L	H	L	–	–	–	–	–	H	L	H	H				•	A	•	•	•	•
14	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–				•	A	•	•	•	•
15	L	–	H	H	–	L	–	–	–	–	L	–	L	–	–	–				A	•	•	•	•	•
16	L	H	–	L	–	L	–	–	–	–	L	–	L	–	–	–				A	•	•	•	•	•
17	L	–	H	L	–	L	–	–	–	–	L	–	L	–	–	–				A	•	•	•	•	•
18	L	–	–	–	H	–	–	–	–	–	L	H	H	–	–	–				A	•	•	•	•	•
19	L	H	–	L	–	–	–	–	–	–	L	L	H	–	–	–				A	•	•	•	•	•
20	L	–	H	L	–	–	–	–	–	–	L	L	H	–	–	–				A	•	•	•	•	•
21	L	L	L	L	H	H	H	–	–	–	L	L	H	–	–	–				A	•	•	•	•	•
22																									
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TABLE 2-5 PLA PROGRAM TABLE (19-199F02)

PROGRAM TABLE ENTRIES					
INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
I_M	I_M	DON'T CARE	PROD TERM PRESENT IN F_P	PROD TERM NOT PRESENT IN F_P	ACTIVE HIGH	ACTIVE LOW
H	L		A		H	L
NOTE: ALL UNUSED INPUTS MUST BE PROGRAMMED AS DON'T CARE			NOTE: OUTPUT FUNCTION ENTRIES ARE INDEPENDENT OF PROGRAMMED OUTPUT PRIORITY		NOTE: OUTPUT PRIORITY PROGRAMMED ONCE ONLY	

PRODUCT TERM																		ACTIVE LEVEL							
	INPUT VARIABLE (1_m)																	H	H	H	H	H	H	H	H
																		OUTPUT FUNCTION							
NO.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
0	–	–	–	–	–	–	–	–	–	–	–	L	L	L	H	L		•	•	•	•	•	A	A	A
1	–	–	–	–	–	–	–	–	–	–	–	L	H	L	L	H		•	•	•	•	•	A	•	A
2	–	–	–	–	–	L	L	–	–	H	L	–	–	L	H	H		•	A	•	•	•	A	A	A
3	–	–	–	–	–	L	L	H	L	L	L	–	–	L	H	H		•	A	•	•	•	A	A	A
4	–	–	–	–	–	–	–	–	–	–	–	–	H	H	H	L		•	•	•	A	•	•	•	A
5	–	–	–	–	–	–	–	–	–	–	–	–	H	H	L	H		•	•	•	A	•	•	A	A
6	–	–	–	–	–	–	–	–	–	–	–	–	L	H	H	H		•	•	•	•	•	•	A	A
7	–	–	–	–	–	–	–	–	–	–	–	–	H	L	H	L		•	•	•	•	•	A	A	•
8	–	–	–	–	–	–	–	–	–	–	–	–	H	H	H	H		•	•	•	•	•	A	A	•
9	–	–	–	–	–	–	–	–	–	–	–	–	–	H	L	L		•	•	•	A	•	•	A	•
10	–	–	–	–	–	–	–	–	–	–	–	–	–	L	L	L		•	•	•	•	•	A	•	•
11	–	–	–	–	–	–	–	–	–	–	–	–	L	H	L	L		•	•	•	•	A	•	•	•
12	–	–	–	–	–	–	–	–	–	–	–	H	H	H	H	L		•	•	•	•	A	•	•	•
13	–	–	–	–	–	–	H	–	–	–	–	–	H	H	L	H		•	•	•	•	A	•	•	•
14	–	–	–	–	–	H	–	–	–	–	–	–	H	H	L	H		•	•	•	•	A	•	•	•
15	–	–	–	–	–	–	–	–	–	–	H	–	H	H	L	H		•	•	•	•	A	•	•	•
16	–	–	–	–	–	–	–	–	H	L	–	–	H	H	L	H		•	•	•	•	A	•	•	•
17	–	–	–	–	–	–	–	L	L	L	–	–	H	H	L	H		•	•	•	•	A	•	•	•
18	–	–	–	–	–	–	H	–	–	–	–	–	L	H	H	H		•	•	•	•	A	•	•	•
19	–	–	–	–	–	H	–	–	–	–	–	–	L	H	H	H		•	•	•	•	A	•	•	•
20	–	–	–	–	–	–	–	–	–	–	H	–	L	H	H	H		•	•	•	•	A	•	•	•
21	–	–	–	–	–	–	–	–	H	L	–	–	L	H	H	H		•	•	•	•	A	•	•	•
22	–	–	–	–	–	–	–	L	L	L	–	–	L	H	H	H		•	•	•	•	A	•	•	•
23	–	–	–	–	–	L	L	–	–	H	L	–	L	H	H	H		•	•	•	A	•	•	•	•
24	–	–	–	–	–	L	L	H	L	L	L	–	L	H	H	H		•	•	•	A	•	•	•	•
25	–	–	–	–	–	L	L	–	–	H	L	–	H	L	H	H		•	•	A	•	•	•	•	•
26	–	–	–	–	–	L	L	H	L	L	L	–	H	L	H	H		•	•	A	•	•	•	•	•
27	–	–	–	–	–	–	–	–	–	–	–	–	H	H	L	L		•	•	A	•	•	•	•	•
28	–	–	–	–	–	–	–	–	–	–	–	L	H	H	H	L		•	•	A	•	•	•	•	•
29	–	–	–	–	–	–	–	–	–	–	–	L	L	L	H	L		•	A	•	•	•	•	•	•
30	–	–	–	–	–	–	–	–	–	–	–	H	L	L	H	L		A	•	•	•	•	•	•	•
31	–	–	–	–	–	–	H	–	–	–	–	–	L	–	H	H		A	•	•	•	•	•	•	•
32	–	–	–	–	–	H	–	–	–	–	–	–	L	–	H	H		A	•	•	•	•	•	•	•
33	–	–	–	–	–	–	–	–	–	–	H	–	L	–	H	H		A	•	•	•	•	•	•	•
34	–	–	–	–	–	–	–	–	H	L	–	–	L	–	H	H		A	•	•	•	•	•	•	•
35	–	–	–	–	–	–	–	L	L	L	–	–	L	–	H	H		A	•	•	•	•	•	•	•
36																									
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2.4.4.2.3 EDMA Request Logic

The logic for making requests to the memory is programmed into the 19-199F01 PLA and is derived from the status of the FIFO stack. As data is loaded into and/or removed from the stack, the MAR and the AAR are incremented to reflect completion of the data transfer. The 19-133 four bit adder (13E4) performs a subtraction between the four least significant bits of the MAR and the AAR (AAR - MAR = S). The result, S, is interpreted as follows.

1. In the Memory Read mode, data is loaded into the stack from the memory and subsequently transferrred to the active device. The MAR is always larger than or equal to the AAR until a match occurs. Therefore, S always reflects (in number of halfwords) the available, or empty, stack locations.

2. In the Memory Write Mode, the converse is true. The AAR is always larger than or equal to the MAR and S reflects the number of halfwords present in the stack.

The resultant sum, S, is compared to the Burst size strap option and the mode of operation strap option. Three signals are generated from the comparison (13K4):

(1) SGTRB1 – when active means S is greater than the burst size.

(2) SEQB1 – when active means S is equal to the burst size.

(3) SLTB1 – when active means S is less than the burst size.

A request is made whenever S is greater than or equal to the burst size. This insures that in Memory Read mode there are enough stack locations available for a burst transfer, and in Memory Write Mode enough data has been written into the stack for the burst transfer.

2.4.5 Termination

When the BSELCH has completed its data transfers, the Delayed Busy (DBSY1) (7N2) signal becomes inactive and fires the Set Attention (SETATN0) (7K4) one shot. The SELCH Attention (SATN1) flip-flop is set and an interrupt is sent to the processor.

Normal termination occurs when the BSELCH has successfully transferred all of its data. In the Memory Read mode, this occurs when the last byte of data has been transferred to the device. When transferring the last byte of data, IOMCH1 is active and when the EDX1 one shot is fired, the Halt I/O (HLTIO1) flip-flop (15N5) is set. This signal resets the BSY1 flip-flop (7N7) and DBSY1 becomes inactive, firing the SETATN0 one shot. In the Memory Write mode, the HLTIO1 flip-flop is set prior to completion of the memory transfers. BSY1 is reset by HLTIO0 but DBSY1 is prevented from becoming inactive by the MWTHLT0 gate being active. When the memory transfers are completed (the stack emptied), the DMA Finish (DMAFIN1) flip-flop (14H7) is set and it resets the HLTIO1 flip-flop. MWTHLT0 then becomes inactive and DBSY1 fires the SETATN0 one shot.

Abnormal termination can occur from two sources. TERM1 (7N2) resets BSY1, and if there is no DMA activity (DMACT0) (7G3), DBSY1 is reset. The other means of termination result from bad status received from the active device when the BSELCH is in the midst of a status transfer. Bad Status (BADST0) (15K7) sets the HLTI01 flip-flop and prevents the DX1 flip-flop from being set. HLTIO0 clears BSY1 and, if in Memory Read Mode, it clears DBSY1. If in the Memory Write Mode, the valid data in the stack must be transferred to the memory. When this has been done, DMFIN1 is set, HLTIO1 is reset, and then DBSY1 is reset.

2.5 Installation Checks

Refer to Chapter 1, Installation, to insure that all backpanel modifications and BSELCH strap options have been properly made. The DMACLK1 oscillator is adjusted at the factory with precision test equipment. If necessary, adjust the clock as follows:

(1) remove the wire-wrap strap between 05E34 and 05E35.

(2) install wire wrap strap between 05E35 and 05E36.

(3) DMACLK0 may be observed from the stake in 00D01. Adjust for a period of 80ns ± 10%.

Return the strap at 05E to the normal configuration after adjustment.

2.6 MNEMONICS

The following is a list of mnemonics found in the BSELCH. A brief description and the 02-456D08 schematic location of each signal are provided.

AAR001:191	Auxiliary Address Register	11E1:11E8,11L1
ACRY0	Carry Out from AAR	11E2
AD1	Address flip-flop – active when BSELCH is addressed	5J2
ADRS0	Address control line from MPX bus	6A4
ANS0	Answer Control line – signals that data from memory is available	2N9
ARLD0	When active permits loading of the AAR	11N4
ATN0	Attention to Processor	6A5
ATSYN0	Attention Sync – generated by Acknowledge Attention from the Processor	6N5
BADST0	Bad Status returned from the device while transferring	15J7
BSTSZ01:21	Burst Size – number of fullwords to be transferred in each memory access	13F6
BSY1	Busy – indicates BSELCH is transferring data	7N7
CLG1	Control Line Gate – gates MPX bus control lines to Private Bus	6N8
CLRS0	Clear SELCH – initializes BSELCH	7N1
CLO70	Power Failure Clear	6A4
CMD0	Command control line from MPX bus	6A2
CMDG01	Command GO initiates the transfer	7F6
CMG0	Command control gated with AD1	6L2
CSO1	Control State Zero of an EDMA data transfer	14N3
D000:150	Data lines from MPX bus	4A2,4A5 5F6,5F9
DA0	Data Available control line from MPX bus	6A3
DAG0	Data Available control line gated with AD1 and BSY1	6L2
DBSY1	Delayed Busy – delays interrupt to Processor until memory accesses are complete	7N2
DINH1	Inhibits clock during wait state of memory transfers	14H4
DMA000:170	EDMA bus data lines	2H1:2H9 2N9
DMACLK1	Clock for memory transfers	Sheet 15
DMACT0	Indicates EDMA activity	14R9

DMARQ1	EDMA bus request flip-flop	14R8
DMFIN1	Indicates EDMA transfers are completed	14H8
DMX120:150	EDMA bus extended data lines	2N2:2N3
DPS1	Private Sync control line delayed	8F8
DR0	Data Request control line from MPX bus	6A2
DREQ1	Indicates BSELCH is requesting the memory	12L5
DRG0	Data Request control line gated with AD1 and BSY1	6L2
DT081:151	Data lines returned to Processor	8C1,N1 C4,N4 8S6
DX1	Data Transfer flip-flop	
EDX0	End of Data Transfer one shot	15E5
EOBST1	End of Burst – indicates appropriate number of Fullwords have been transferred to the memory	13K2
EOT0	End of Transmission signal for EDMA transfers	13R8
ENBD0	Enables MPX bus data line drivers	6L3
ENBPD0	Enables Private bus data line drivers	6M4
EXRD1	Extended Read – set in command byte when three bytes are required to read the Final Address	7E1
FAR001:191	Final Address Register – address of last location in memory to be accessed	9D1:9D7 9K4:9K7
FWMCH0	Fullword Match – memory address matches the FAR on a fullword boundary	10L2
GPD1	Gate Private Data – enables Private bus data line drivers during writes to device	8S9
HLTIO1	Halt I/O flip-flop	15N5
HW0	Halfword Control line sent to Processor MPX bus	6N8
HWFF1	Halfword Flip-Flop – set when BSELCH is to perform a halfword EDMA bus transfer	14R7
HWMCH0	Halfword Match – the necessary address matches the FAR on a halfword boundary	10L3
HWMD1	Halfword Mode	13F5
IOMCH1	I/O Match – indicates the AAR matches the FAR	9J9
LDBH0	Load Data Buffer High	15H1
LDBL0	Load Data Buffer Low	15H2
LDSTK1	Load Stack	15N1
LFARX0	Loads FAR001:031	11N4
LMRQ0	Local Memory Request Queued	12L6
LOAD0	Load signal on EDMA bus transfer	2N9

M00:M30	Memory Banks 0:3	12F1,64
M0BZ0:M3BZ0 s	Memory Busy	12H3
MAR001:181	Memory Address Register	Sheet 10
MARCLK0	Memory Address Register Clock	13DF2
MMF1	Memory Malfunction status bit	13R1
MRD1	Memory Read command bit	7F5
MWRT1	Memory Write command bit	7F4
MSC1	Multiplexor-SELCH control flip-flop	7N8
NOMEM0	No Memory – indicates MAR is pointing to non existant memory	12G4
PADRS0	Private Address control to BSELCH private bus	6F5
PATN0	Private Attention from device	6A9
PCL070	Private Power Fail control line	6F8
PCMD0	Private Command control line	6F6
PD000:150	Private Data Lines	4N2,4N7 5N6,5N9
PDA0	Private Data Availablescontrol line	6F6
PDR0	Private Data Request control line	6F7
PF1	Memory Parity Failure status bit	13R1
PHW0	Private Halfword control line	6J8
PSR0	Private Status Request control line	6F7
PSYN0	Private Sync from device	6A9
PTACK0	Private Transmit Acknowledge to private bus	6N6
QUE0	Queue – to resolve contention for EDMA bus	12C8
RACK0	Receive Acknowledge from MPX bus	6G5
RPC0	Receive Priority Chain pulse from EDMA bus	12C9
SAD081:151	BSELCH ten bit address	5A2:5A6
SCLR0	Systems Clear	7J2
SEL1	Select flip flop - when active, BSELCH selected for EDMA transfer	12MA
SELSTS1	SELCH Status command bit	7E2
SOT0	Start of Transmission pulse from EDMA bus	12J9
SR0	Status Request control line	6L1
SRG0	Status Request control line gated with AD1	6A2

STK001:151	FIFO Stack data outputs	3A9:3L9
STKCLK0	FIFO Stack clock – removes data from the stack	15H2
STKFL0	Stack Full signal	3K1
STKVLD1	Stack Valid signal	3N1
SYN0	Sync to MPX bus	6A5
SX1	Status Transfer flip-flop	8S8
TACK0	Transmit Acknowledge to MPX bus	6N7
TERM1	Terminate the transfer	7N2
TPC0	Transmit Priority Chain pulse to EDMA bus	12J9
UAARH0	Unload AAR041:111	11M1
UAARL0	Unload AAR121:191	11M1
UAARX0	Unload AAR001:031	11M2
W4ANS1	Wait for Answer	13R5
XBNDRY1	Indicates BSELCH is about to cross a memory system boundary	13J9
XREQ0	Request EDMA bus for service	12L6

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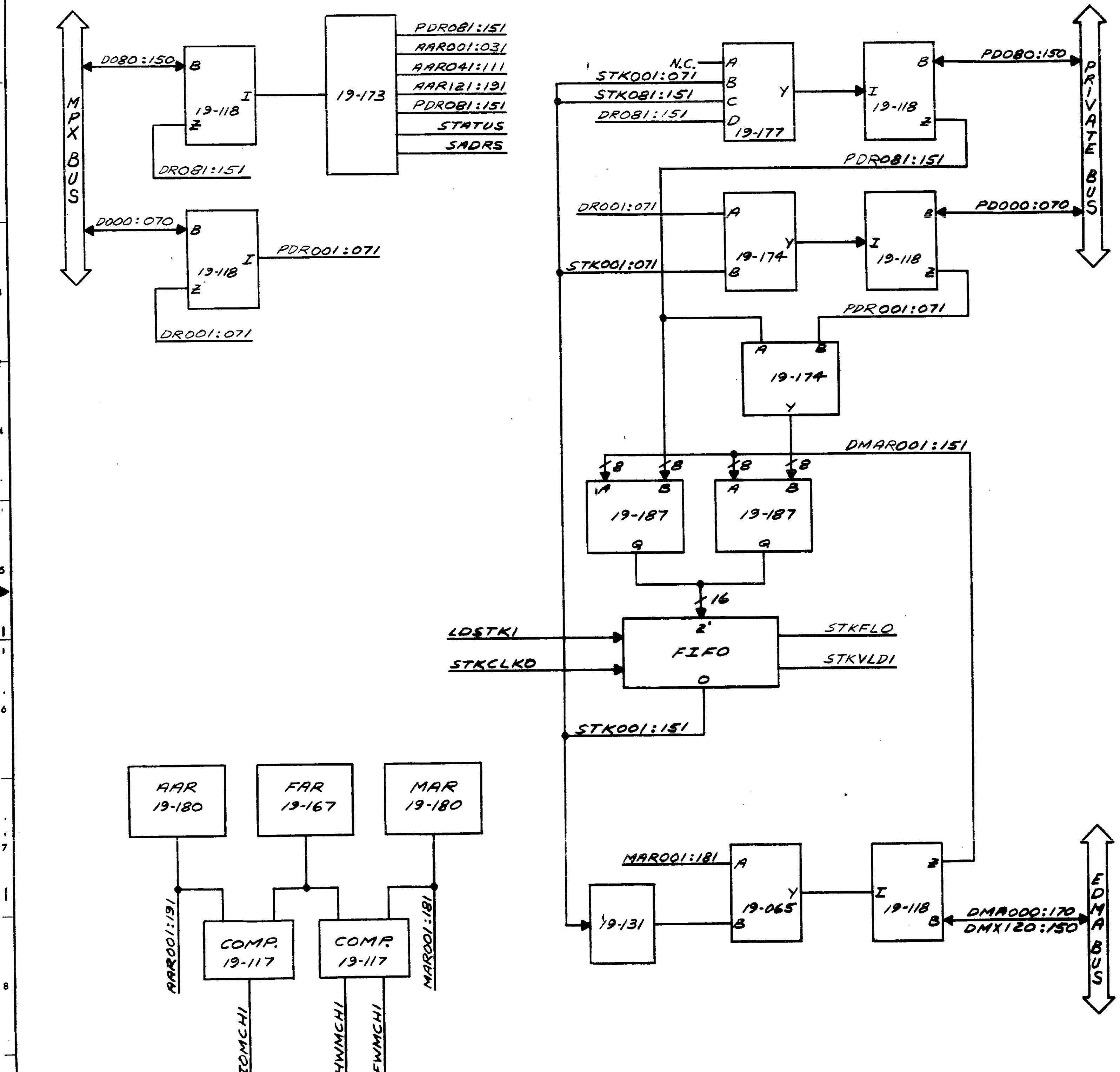
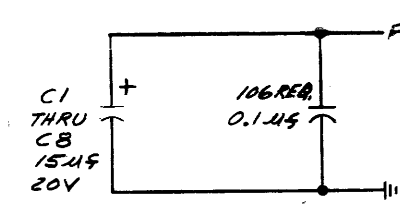


BACK PANEL MAP

BSELCH			
ROW 1	TERM. NO.	ROW 2	
P5	41	GND	1
GND	40	GND	
	39		
	38		
DMA170	37	DGND	
DMA150	36	DMA160	
DMA130	35	DMA140	
DGND	34	DMA120	
DMA110	33	DMA100	
DMA090	32	DMA080	
DMA070	31	DMA060	
DMA050	30	DGND	
DMA030	29	DMA040	
DMA010	28	DMA020	
DGND	27	DMA000	
SCLRO	26	PHWO	
	25		
	24	XBSYO	
PSYNO	23	PATNO	
	22	PTACKO	
PCLO70	21	PDAO	
PDRO	20	PCMDO	
PSRO	19	PADRSO	
PDI40	18	PDI50	
PDI20	17	PDI30	
PDI00	16	PDI10	
PD080	15	PD090	
PD060	14	PD070	
PD040	13	PD050	
PD020	12	PD030	
PD000	11	PD010	
	10	DMX140	
DMX150	09	DMX120	
DMX130	08	DGND	
M3B20	07	M2B20	
M1B20	06	M0B20	
LOADO	05	ANSO	
LMRQO	04	DGND	
SOTO	03	EOTO	
XREQO	02	QUEO	
GND	01	GND	
P5	00	GND	
ROW 1	TERM. NO.	ROW 2	
P5	41	GND	0
GND	40	GND	
	39		
	38		
RPCO	37	TPCO	
DGND	36		
	35		
	34		
	33		
	32		
	31		
	30		
	29		
	28		
	27		
SCLRO	26	HWO	
	25		
	24		
SYNO	23	ATNO	
RACKO	22	TACKO	
CLO70	21	DAO	
DRO	20	CMDO	
SRO	19	ADRSO	
DI40	18	DI50	
DI20	17	DI30	
DI00	16	DI10	
D080	15	D090	
D060	14	D070	
D040	13	D050	
D020	12	D030	
D000	11	D010	
	10		
	09		
	08		
	07		
	06		
	05		
	04		
	03		
	02		
GND	01	GND	
P5	00	GND	
ROW 1	TERM. NO.	ROW 2	

TEST POINTS

DESIG.	MNEMONIC	SHT. LOC.
A	ADO	5J2
B	DXI	8S6
C	MSCO	7N9
D	BSYI	7N7
E	SELI	12M7
F	MWRTI	7F4
G	SXI	8S8
TP1	STKFLO	3K2
TP2	STKVLDI	3N2



PRINTED CIRCUIT BOARD AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

BSELCH	35-635	R07

NOTE: THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

REVISIONS

PRE PRODUCTION APPROVAL — INIT / DATE — DEV 11/2/76 — PROD

ADD DGND TO BACK PANEL MAP PINS 136-0, 204-1, 208-1, 127-1, 230-1, 134-1 & 237-1. REVISED SHEETS 8 & 15						
	HM	03870-1	—	12/8/76		R01
REVISED SHTS 10, 11, 12						
		3870-02	—	12-13-76		R02
REVISED SHTS 2, 10, 13-15 35-635 WAS R02						
		3870-03	—	12/22/76		R03
RELEASED FOR PRODUCTION ENG. DATE 12/22/76						
REVISED SHTS 6, 7 & 11. 35-635 WAS R03.						
GS		3323		8-12-77		R04
REVISED SHTS 2, 5, 6, 7, 8, 10 & 12. 35-635 WAS R04.						
GS		3180		10-7-77		R05
REVISED SHTS 6, 13 & 14. 35-635 WAS R06.						
GS		3333		12-16-77		R06

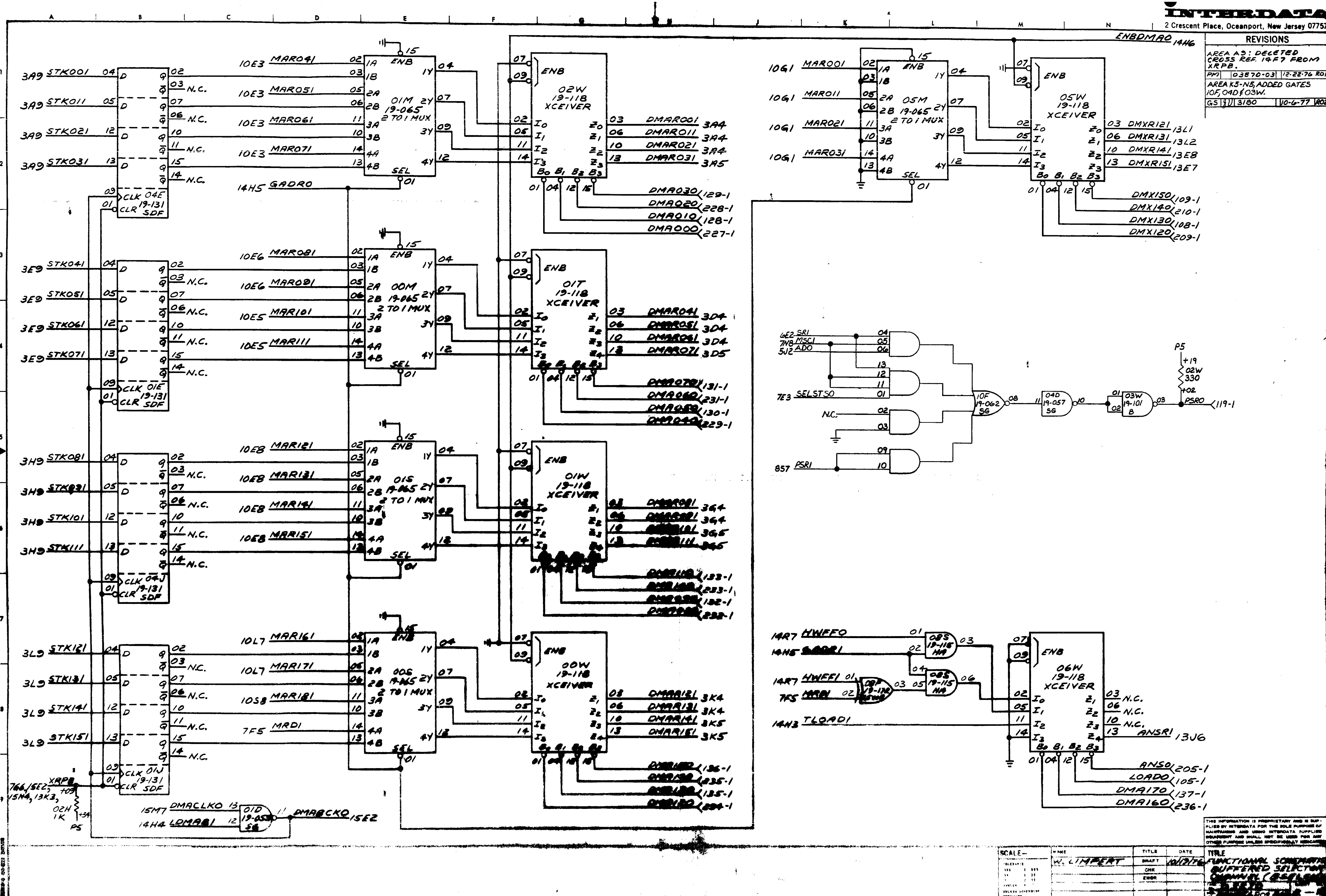
NOTES:
1. UNLESS OTHERWISE SPECIFIED; ALL RESISTORS ARE 1/4 W ±5%.

SHEET INDEX																
REV.		2	–	–	1	3	2	2	–	3	2	2	2	2	2	
SHT.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

SCALE–
TOLERANCE: .XXX ± .005; .XX ± .02; .X ± .03; ANGLES ± 1°; UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
W. LIMPERT	DRAFT	10/25/76
H. MATTER	CHK	10/25/76
E. D'ANGELO	ENGR	
R.A. BARKER	Q.C.	
S. MESSINA	MGR.	

TITLE: FUNCTIONAL SCHEMATIC BUFFERED SELECTOR CHANNEL (BSELCH)
TASK NO. 03870
R06
SHEET 1



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2 Crescent Place, Oceanport, New Jersey 07757
REVISIONS
AREA A3: DELETED CROSS REF. 14F7 FROM XRPB.
03870-03 12-22-76 R01
AREA K5-N5, ADDED GATES 10F, 04D & 03W.
3180 10-6-77 R02
STK001 STK011 STK021 STK031
04E 19-131 SDF
MAR041 MAR051 MAR061 MAR071
01M 19-065 2 TO 1 MUX
02W 19-118 XCEIVER
DMAR001 DMAR011 DMAR021 DMAR031
DMA030 DMA020 DMA010 DMA000
STK041 STK051 STK061 STK071
01E 19-131 SDF
MAR081 MAR091 MAR101 MAR111
00M 19-065 2 TO 1 MUX
01T 19-118 XCEIVER
DMAR041 DMAR051 DMAR061 DMAR071
STK081 STK091 STK101 STK111
04J 19-131 SDF
MAR121 MAR131 MAR141 MAR151
01S 19-065 2 TO 1 MUX
01W 19-118 XCEIVER
STK121 STK131 STK141 STK151
01J 19-131 SDF
MAR161 MAR171 MAR181 MRD1
00S 19-065 2 TO 1 MUX
00W 19-118 XCEIVER
DMAR121 DMAR131 DMAR141 DMAR151
GADR0
ENBDMAR0 14H6
MAR001 MAR011 MAR021 MAR031
05M 19-065 2 TO 1 MUX
05W 19-118 XCEIVER
DMXR121 DMXR131 DMXR141 DMXR151
DMX150 DMX140 DMX130 DMX120
SR1 MSC1 ADO SELSTS0 PSR1
10F 19-062 SG
04D 19-057 SG
03W 19-101 B
PSR0
HWFF0 GADR1 HWFF1 MRD1 TLOAD1
08S 19-115 HA
06W 19-118 XCEIVER
ANSR1 ANS0 LOAD0 DMA170 DMA160
XRPB
DMACLK0 LDMAB1
01D 19-053 SG
DMABCK0
SCALE-
W. LIMPERT
10/13/76
FUNCTIONAL SCHEMATIC
BUFFERED SELECTOR

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

NOTES;
1. NORMALLY STRAPPED AS SHOWN STRAP TO XRPE FOR TEST ONLY.

SCALE—

NAME	TITLE	DATE
W. LIMPERT	DRAFT	10/27/76
	CHK	
	ENGR	

TITLE FUNCTIONAL SCHEMATIC BUFFERED SELECTOR CHANNEL (BSELCH)

TAB NO. 03870 SHEET 3

DWG NO. 42-455

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

6L3 ENBDO

13T 19-118 XCEIVER
8C1 DT081
8C4 DT091
8G1 DT101
8G4 DT111
115-0 D080
215-0 D090
116-0 D100
216-0 D110
DR081 F1, 5C2, 9H4
DR091 F3, 5C3, 7B1, 9H4
DR101 F3, 5C3, 7B4, 9H5
DR111 F5, 5C3, 7B5, 9H5
11LS, 13A2

12T 19-118 XCEIVER
8K1 DT121
8K4 DT131
8N1 DT141
8N4 DT151
117-0 D120
217-0 D130
118-0 D140
218-0 D150
DR121 F6, 5C5, 7B3, 9A1, 9H6
DR131 F7, 5C5, 9A2, 9H6
DR141 F8, 5C5, 9A2, 9H7
DR151 F9, 5C5, 9A2, 9H7

7N9 MSCO
6N5 ATSYNO
6L1 SRGO
12C 19-059 SA

6N7 PHWOA
11L7 AARI90
07A 19-153 LSG
08D 19-154 LSA
06C 19-153 LSG
06C 19-153 LSG
06D 19-160 LSA
7N7 BSYI
7F4 MWRTI
5H7 BSYWTI

3A9 STK001
3H9 STK081
D2 DR081
STB1
SEL B 06H 19-177
SEL A
STB 2
3A9 STK011
3H9 STK091
D2 DR091
4 TO 1 MUX

3A9 STK021
3H9 STK101
D2 DR101
STB1
SEL B 06U 19-177
SEL A
STB2
3A9 STK031
3H9 STK111
D2 DR111
4 TO 1 MUX

3E9 STK041
3L9 STK121
D4 DR121
STB1
SEL B 03J 19-177
SEL A
STB2
3E9 STK051
3L9 STK131
D4 DR131
4 TO 1 MUX

3E9 STK061
3L9 STK141
D5 DR141
STB1
SEL B 03K 19-177
SEL A
STB2
3E9 STK071
3L9 STK151
D5 DR151
4 TO 1 MUX

03T 19-118 XCEIVER
PDR081 3A1, 8A1
PDR091 3A1, 8A3
PDR101 3A2, 8D1
PDR111 3A2, 8D3
PD110 216-1
PD100 116-1
PD090 215-1
PD080 115-1
+08 02H 330 +35
+07 02H 330 +36
+06 02H 330 +37
+05 02H 330 +38 P5

6M4 ENBPDO

02T 19-118 XCEIVER
PDR121 3D1, 8H1, 8H6
PDR131 3D1, 8H3, 15E7
PDR141 3D2, 8L1, 15E7
PDR151 3D2, 8L3, 15E7
PD150 218-1
PD140 118-1
PD130 217-1
PD120 117-1
+01 02S 330 +10
+02 02S 330 +09
+04 02S 330 +07
+03 02S 330 +08 P5

SCALE–
TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
W. LIMPERT	DRAFT	10/19/76
	CHK	
	ENGR	

TITLE
FUNCTIONAL SCHEMATIC
BUFFERED SELECTOR
CHANNEL (8SSLCH)

TASK NO. 03870
SYS NO. 02-456
SHEET 9F
PAGE 4-15

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

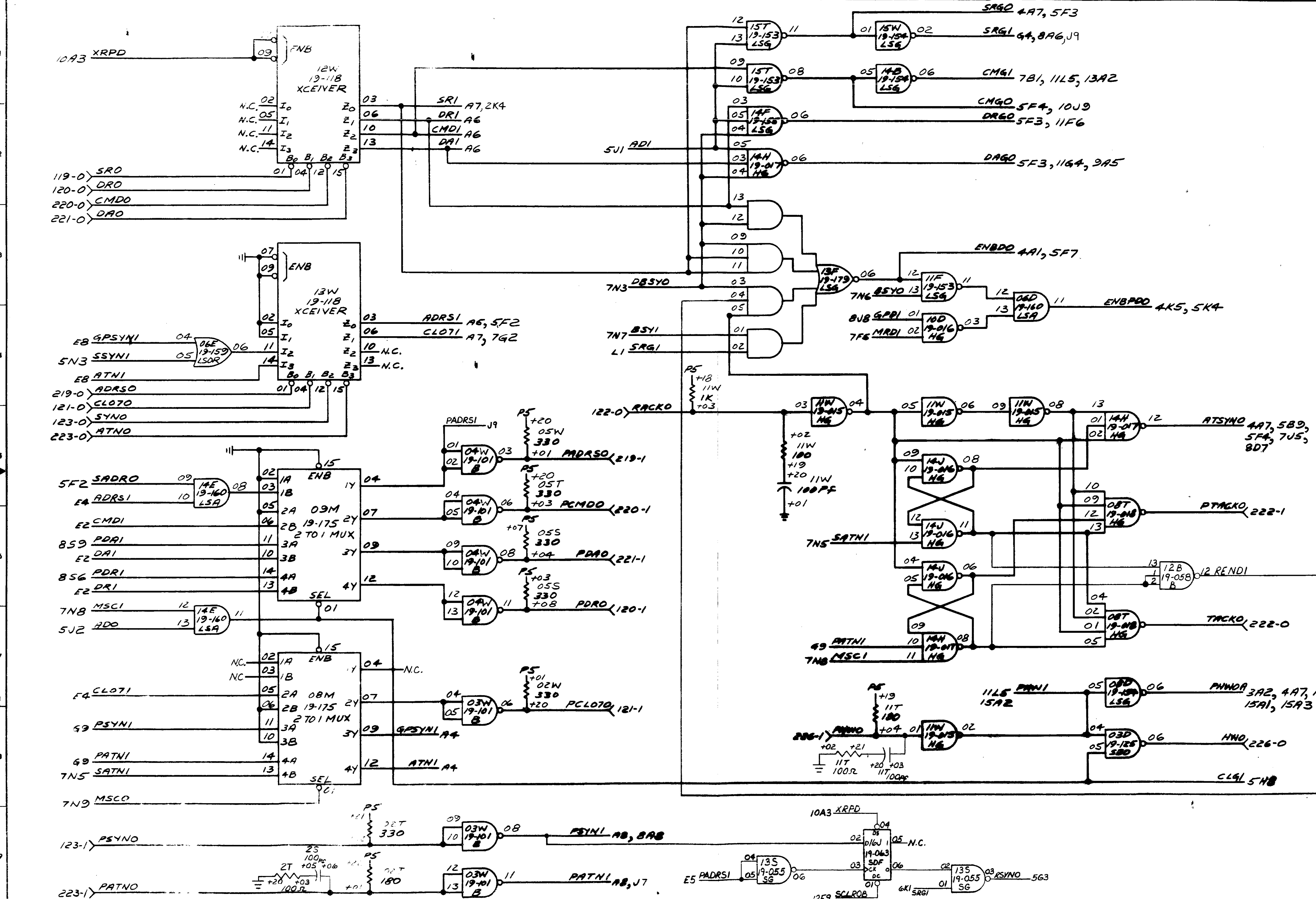
REVISIONS
AREA G3, ADDED SHT LOC, & MNEMONIC TO PINS 01 & 02 OF GATE 16T. PINS 01 & 02 OF 16T WERE CONNECTED TO PIN 03 OF GATE 15T. AREA J2, ADDED 2J4 TO ADO, 16T-04 WAS SRGO GLI
GS | AV | 3180 | 10-7-77 | R01

NOTES:
1. BSELCH PREFERRED ADDRESS = '0 F 0'

SCALE—	NAME	TITLE	DATE
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	W. LIMPERT	DRAFT	10/20/76
		CHK	
		ENGR	

TITLE: FUNCTIONAL SCHEMATIC BUFFERED SELECTOR CHANNEL (BSELCH)
TASK NO: 03870 SHEET OF 5—15
DWG NO: 02-456R01 DOC

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757



10A3 XRPD
12W 19-118 XCEIVER
13W 19-118 XCEIVER
SR1 A7, 2K4
DR1 A6
CMD1 A6
DA1 A6
119-0 SR0
120-0 DR0
220-0 CMD0
221-0 DA0
5U1 AD1
SRG0 4A7, 5F3
SRG1 G4, 8A6, J9
CMG1 7B1, 11L5, 13A2
CMG0 5F4, 10U9
DRG0 5F3, 11F6
DAG0 5F3, 11G4, 9A5
ENBD0 4A1, 5F7
7N3 DBSY0
7N6 BSY0
8J8 GPB1
7F6 MRD1
ENBPD0 4K5, 5K4
7N7 BSY1
L1 SRG1
ADRS1 A6, 5F2
CL071 A7, 7G2
E8 GPSYN1
5N3 SSYN1
E8 ATN1
219-0 ADRS0
121-0 CL070
123-0 SYN0
223-0 ATN0
122-0 RACK0
ATSYN0 4A7, 5B9, 5F4, 7U5, 8D7
PTACK0 222-1
12B 19-058 B
RENDI
TACK0 222-0
PADRS1 J9
PADRS0 219-1
PCMD0 220-1
PDA0 221-1
PDR0 120-1
5F2 SADR0
E4 ADRS1
E2 CMD1
8S9 PDA1
E2 DA1
8S6 PDR1
E2 DR1
09M 19-175 2 TO 1 MUX
08M 19-175 2 TO 1 MUX
7N8 MSC1
5J2 AD0
7N5 SATN1
G9 PATN1
7N8 MSC1
E4 CL071
G9 PSYN1
G9 PATN1
7N5 SATN1
7N9 MSC0
PCL070 121-1
GPSYN1 A4
ATN1 A4
11L6 15A2 PAWI
PHWOA 3A2, 4A7, 15K6, 15A1, 15A3
286-1 PHWO
HWO 226-0
CLG1 5H8
123-1 PSYN0
PSYN1 A8, 8A8
223-1 PATN0
PATN1 A8, J7
E5 PADRS1
10A3 XRPD
19-063 SDF
12F9 SCLR0B
6K1 SRG1
RSYN0 5G3

REVISIONS

EXTENSIVE CHANGES WERE MADE FOR PREVIOUS REV LEVELS SEE VOID COPY IN FILES (R01)

GS		3180	10-6-77	R02

AREA C9-D9 CAP. TO RESISTOR TO GND. ON "PATNO" WAS NOT SPEC'D. AREA U8 CAP. TO RESISTOR TO GND. ON "PHWO" WAS NOT SPEC'D.

GS		3333	12-16-77	R03

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SCALE–	NAME	TITLE	DATE
	W. LIMPERT	DRAFT	10/20/76
		CHK	
		ENGR	

TITLE: FUNCTIONAL SCHEMATIC BUFFERED SELECTOR CHANNEL (BSELCH)

TASK NO. 03870

DWG NO. 02 456 R03 | SHEET 6 OF 15

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
AREA G2, 11S6 ACRYO WAS 11E2 ACRYO.			
GS	01	3323	8-11-77 R01
AREA N8 ADDED "2J4" TO MSC1. AREA E3 ADDED "2J5" TO "SELST3SO".			
GS	01	3180	10-7-77 R02

SETATNO

SR2 XRPC
4D2 DR091
6L1 CMG1
N2 SCLR0A
4D5 DR131
4D4 DR121
4D2 DR101
N8 MSC1
11G4 DARG0
4D2 DR111
10MB SETG01
15ES EDX1
EXRD1 11G1
N.C.
SELSTS1 8A6
SELSTS0 8A7, 2J5
STOP0
MWRT1 3A5, 4A9, 8M6, 13A1, 13K8, 14A2, 15G5
MRD1 2D8, 2K8, 6U4, 8H8, 13A1, 13L1, 14K8, 15E3
CMDG01 14K8
XRPB 2A9
WXFR1
F 102-7
+01 14S +10 P5 6.8K
N.C. EXC EXR 13C 19-042
15K
+04 14C P5 6.8K +07
N.C. EXC EXR 13C 19-042
SR2 XRPC
6N5 ATSYN0
N3 MSC0
CLR0A 10S9, 14F3
CLR0 11G5, 13L4, 14R8, 15K5
SCLR0A B2, J8, 5F2, 11A7, 12C9, 13L3
DBSY1 3A8, 8H2, 10A2, 14F8
TERM1 14A2
DBSY0 6G3
MWTHLT0 14K3
SATN1 6A8, 6U6
N.C.
126-1 SCLR0
126-0
6E4 CL071
12G3 NOMEMO
11S6 ACRYO
N6 BSY0
14R9 DMACT0
14H8 SDRQ0
15N5 HLTI01
15NS HLTI00
BSY0 4J3, J8, 6G4
BSY1 4A8, 6G4, 8A9
MSC1 8A4, 6A7, 6U7, 8A6, 2J4
MSC0 H6, 4A7, 6A8, 8A7
CMDG00 13L3, 15G4
5U2 SGADD
N6 BSY0
N2 SELR0A
XBSY0 224-1
+08 02E NOTE; FOR FUTURE SYSTEMS +07
+05 02C 1K +06 P5
D 104-7
C 105-7

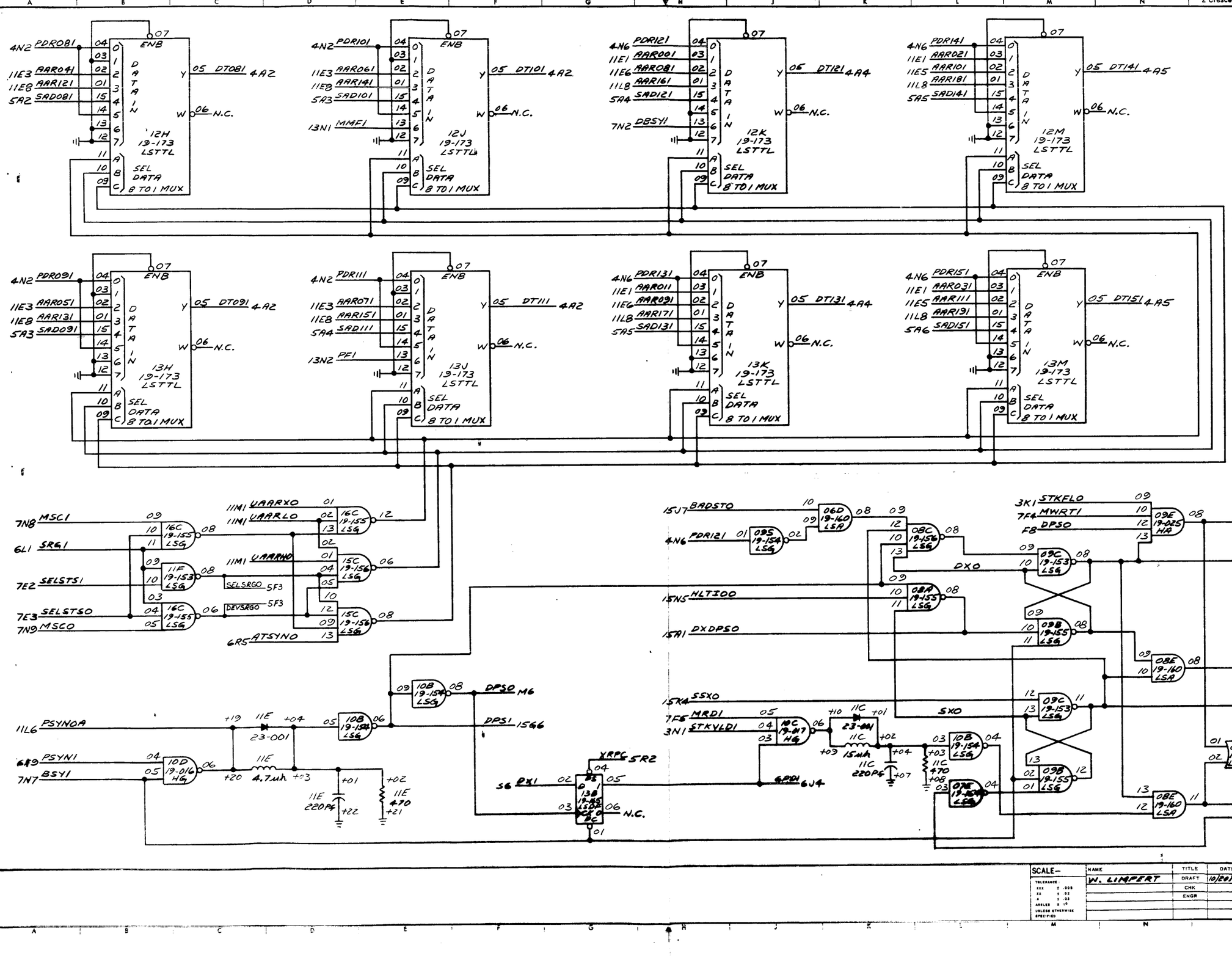
SCALE–	NAME	TITLE	DATE
TOLERANCE: XXX ± .005, XX ± .02, X ± .05, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	W. LIMPERT	DRAFT	11/20/76
		CHK	
		ENGR	

TITLE FUNCTIONAL SCHEMATIC BUFFERED SELECTOR CHANNEL (BSELCH)

TASK NO. 03870
DWG NO. 02-456 R02
SHEET OF 7—A

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS				
ADDED 15G6 TO PSR1 IN ZONE S7. ZONE S8 SX1 WAS GOING TO 15G6.				
KK	HM	03870-1	-	12/8/76 R01
AREA D7, ADDED MNEMONIC "SELSRGO" & SHT REF "5F3" TO PIN 08 OF GATE 11F. ADDED MNEMONIC "DEVSRGO" & SHT REF "5F3" TO PIN 06 OF GATE 16C. AREA S7, ADDED 2J5 TO PSR1."				
GS	RJ	3180	10-7-77	R02



SCALE—	NAME	TITLE	DATE
TOLERANCE: XXX ± .000, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	W. LIMPERT	DRAFT	10/20/76
		CHK	
		ENGR	

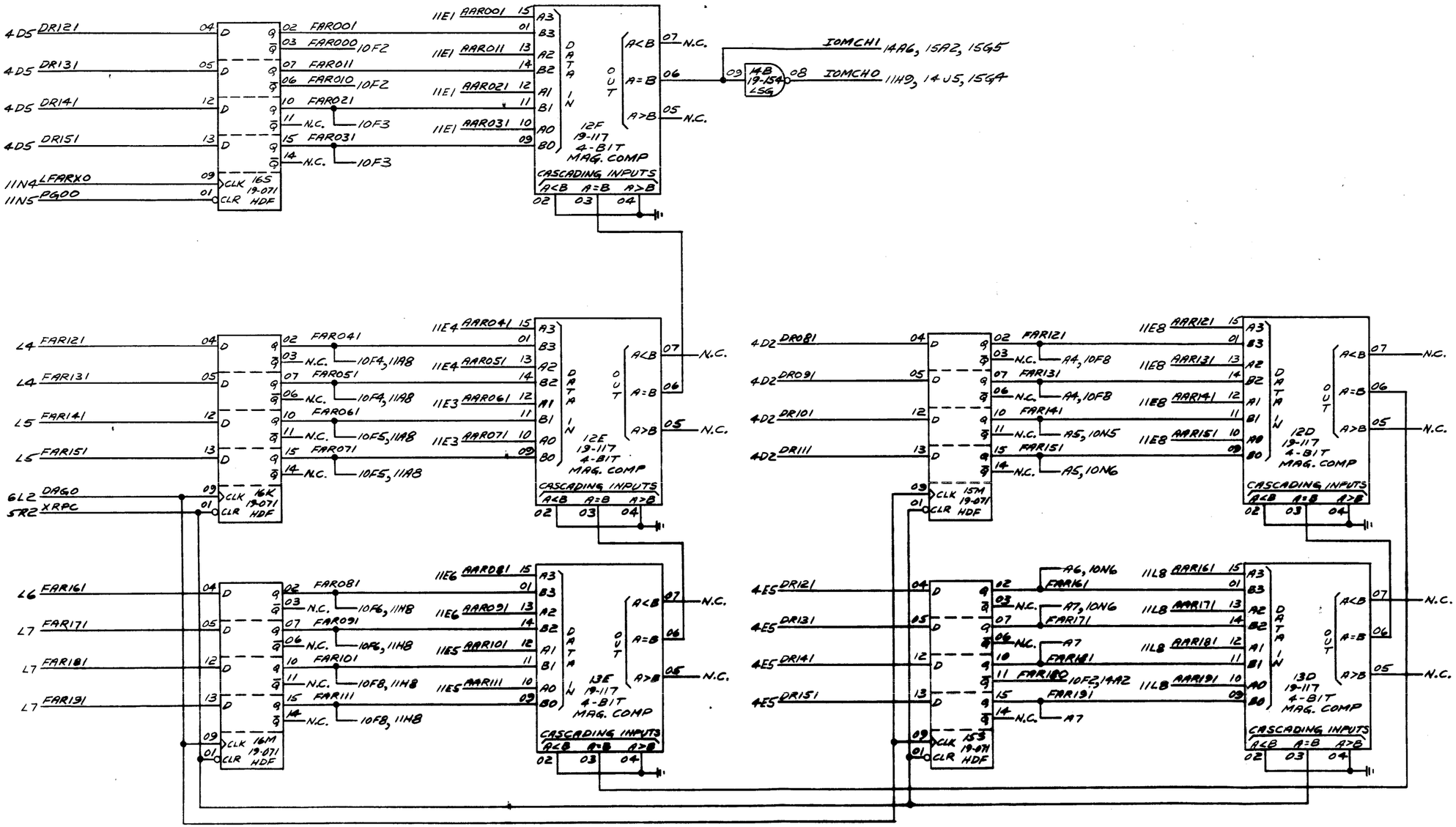
TITLE FUNCTIONAL SCHEMATIC BUFFERED SELECT CHANNEL (BSELCH)

TASK 03870 SHEET 8

DWG 02-456 R02 PAGE

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

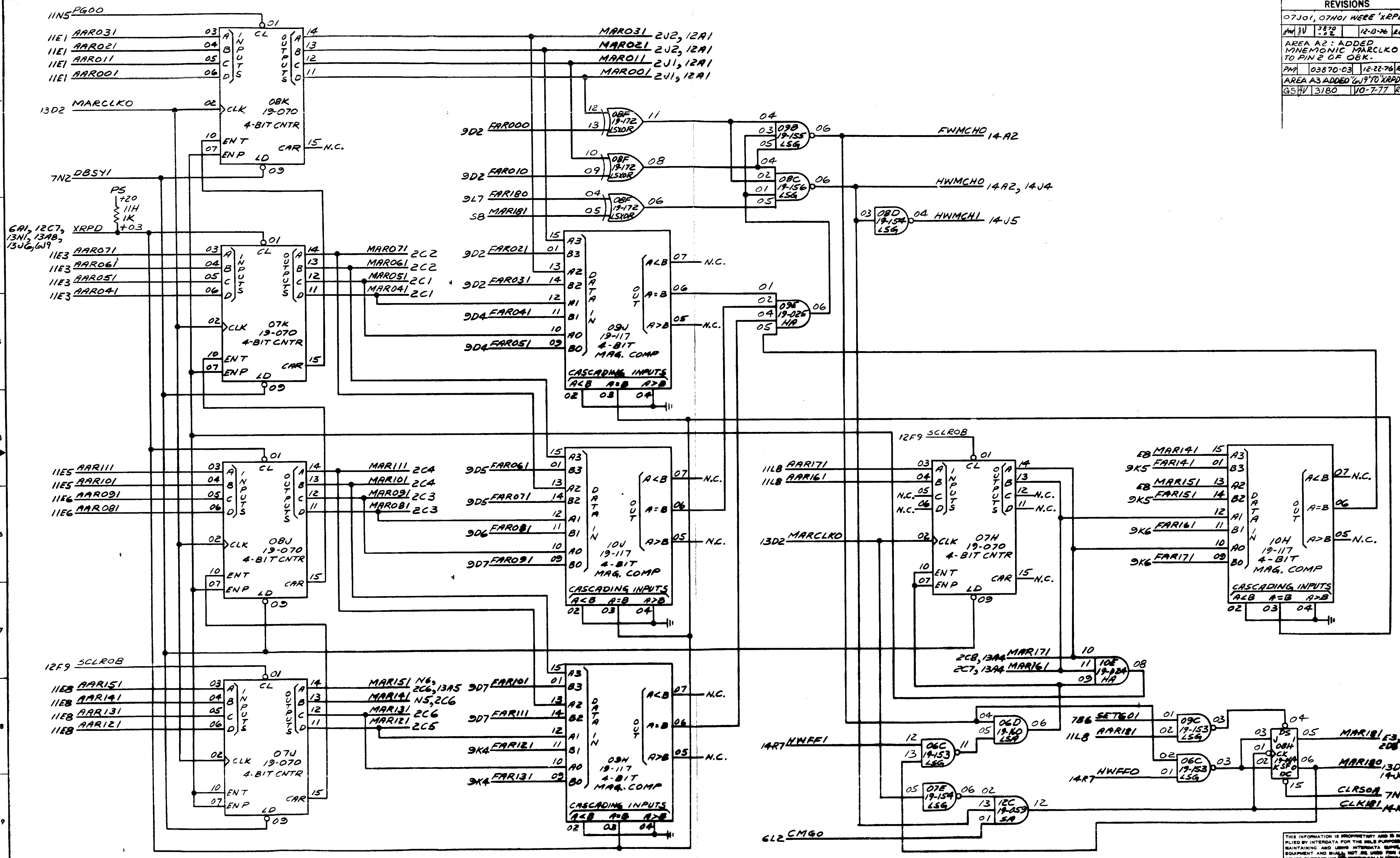


SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .08, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	W. LIMPERT	DRAFT	10/21/76
		CHK	
		ENGR	

TITLE: FUNCTIONAL SCHEMATIC BUFFERED SELECTOR CHANNEL (BSELCH)

TASK NO. 03870 DWG NO. 02456 SHEET 9 REV

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757



11N5 PG00
11E1 AAR031
11E1 AAR021
11E1 AAR011
11E1 AAR001
13D2 MARCLKO
08K 19-070 4-BIT CNTR
MAR031 2J2, 12A1
MAR021 2J2, 12A1
MAR011 2J1, 12A1
MAR001 2J1, 12A1
9D2 FAR000
9D2 FAR010
9L7 FAR180
S8 MAR181
08F 19-172 LSXOR
09B 19-155 LSG
08C 19-156 LSG
08D 19-154 LSG
FWMCH0 14A2
HWMCH0 14A2, 14J4
HWMCH1 14J5
7N2 DBSY1
PS +20 11H 1K +03
6A1, 12C7, 13N1, 13A8, 13J6, 6J9 XRPD
11E3 AAR071
11E3 AAR061
11E3 AAR051
11E3 AAR041
07K 19-070 4-BIT CNTR
MAR071 2C2
MAR061 2C2
MAR051 2C1
MAR041 2C1
9D2 FAR021
9D2 FAR031
9D4 FAR041
9D4 FAR051
09J 19-117 4-BIT MAG. COMP
CASCADING INPUTS
09E 19-026 HA
11E5 AAR111
11E5 AAR101
11E6 AAR091
11E6 AAR081
08J 19-070 4-BIT CNTR
MAR111 2C4
MAR101 2C4
MAR091 2C3
MAR081 2C3
9D5 FAR061
9D5 FAR071
9D6 FAR081
9D7 FAR091
10J 19-117 4-BIT MAG. COMP
12F9 SCLR0B
11L8 AAR171
11L8 AAR161
13D2 MARCLKO
07H 19-070 4-BIT CNTR
E8 MAR141
9K5 FAR141
E8 MAR151
9K5 FAR151
9K6 FAR161
9K6 FAR171
10H 19-117 4-BIT MAG. COMP
2C8, 13A4 MAR171
2C7, 13A4 MAR161
10E 19-024 HA
12F9 SCLR0B
11E8 AAR151
11E8 AAR141
11E8 AAR131
11E8 AAR121
07J 19-070 4-BIT CNTR
MAR151 N6, 2C6, 13A5
MAR141 N5, 2C6
MAR131 2C6
MAR121 2C5
9D7 FAR101
9D7 FAR111
9K4 FAR121
9K4 FAR131
09H 19-117 4-BIT MAG. COMP
14R7 HWFF1
06C 19-153 LSG
06D 19-160 LSG
07E 19-154 LSG
12C 19-059 SA
7B6 SETG01
11L8 AAR181
14R7 HWFF0
09C 19-153 LSG
06C 19-153 LSG
08H 19-144 K-S F/F
MAR181 E3, 2D8
MAR180 13D4, 14J4
CLRS0A 7N1
CLK181 14K7
6L2 CMG0
N.C.

REVISIONS

07J01, 07H01 WERE 'XRPD'			
JV	3870-02	12-13-76	R01
AREA A2: ADDED MNEMONIC MARCLKO TO PIN 2 OF 08K.			
PM	03870-03	12-22-76	R02
AREA A3 ADDED "6J9" TO "XRPD"			
GS JV	3180	10-7-77	R03

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SCALE—

NAME: W. LIMPERT — DRAFT — 10/21/76

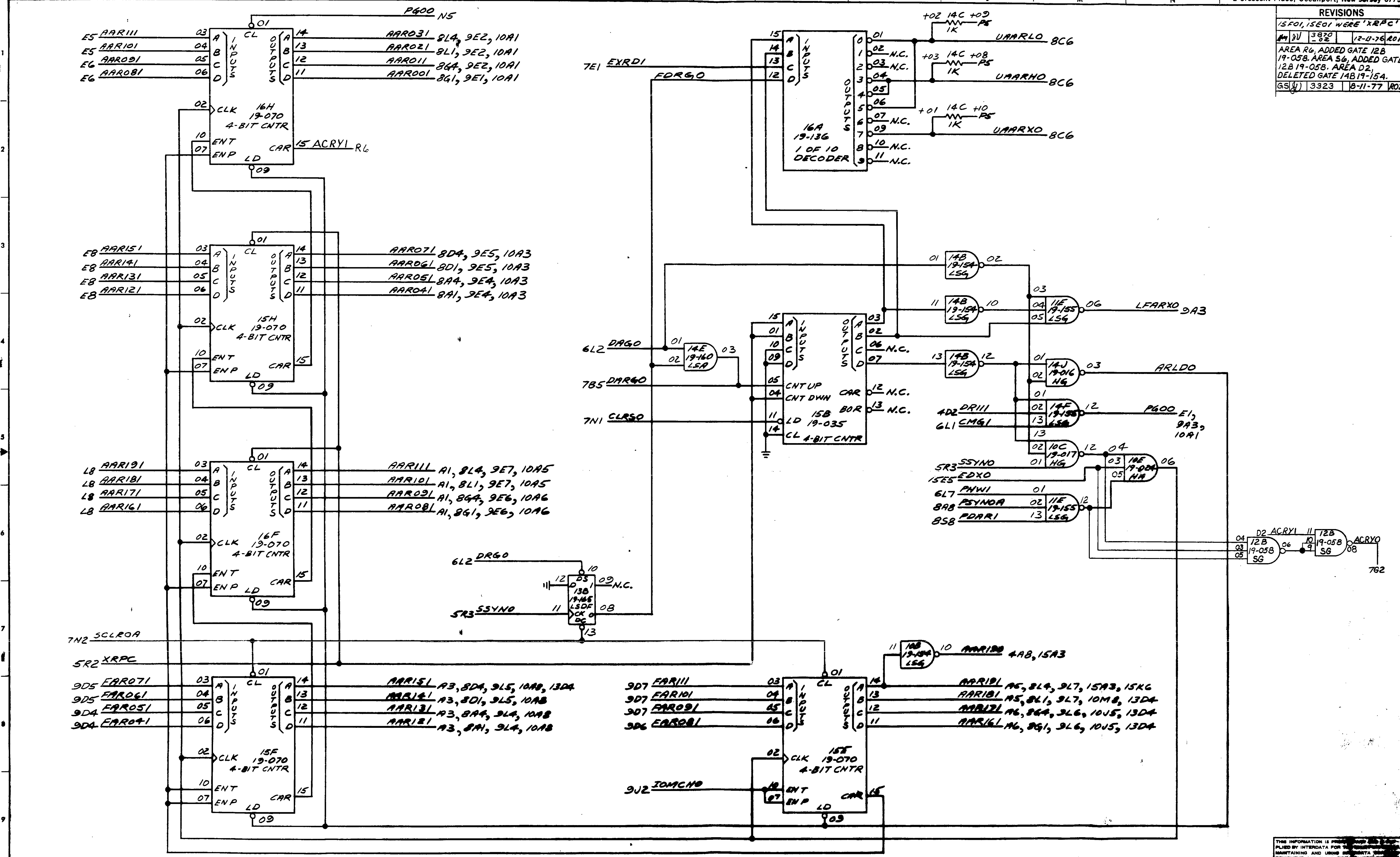
TITLE: FUNCTIONAL SCHEMATIC BUFFERED SELECTOR CHANNEL (BSELCH)

63870

02-456

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
15F01, 15E01 WERE 'XRPC'			
	3870 02	12-13-76	R01
AREA R6, ADDED GATE 12B 19-058. AREA S6, ADDED GATE 12B 19-058. AREA D2, DELETED GATE 14B 19-154.			
GS	3323	8-11-77	R02



SCALE—	NAME	TITLE	DATE	TITLE
	W. LIMPERT	DRAFT	10/22/76	FUNCTIONAL SCHEMATIC BUFFERED SELECTOR CHANNEL
		CHK		03870
		ENGR		02-456 R0

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS				
AREA F9: ADDED 'SCLR08' TO 11T03				
MM	PJ	3037 -28	12-13-76	R01
AREA F9 ADDED 07W 19-170 "SCLR08"				
GS	JJ	3180	10-7-77	R02

07M 19-136 1 OF 10 DECORER

06M 19-136 1 OF 10 DECODER

11M

11S

07T 19-069 8 TO 1 MUX

05T 19-118 XCEIVER

MBE1

09T 30-018 100NS DELAY LINE

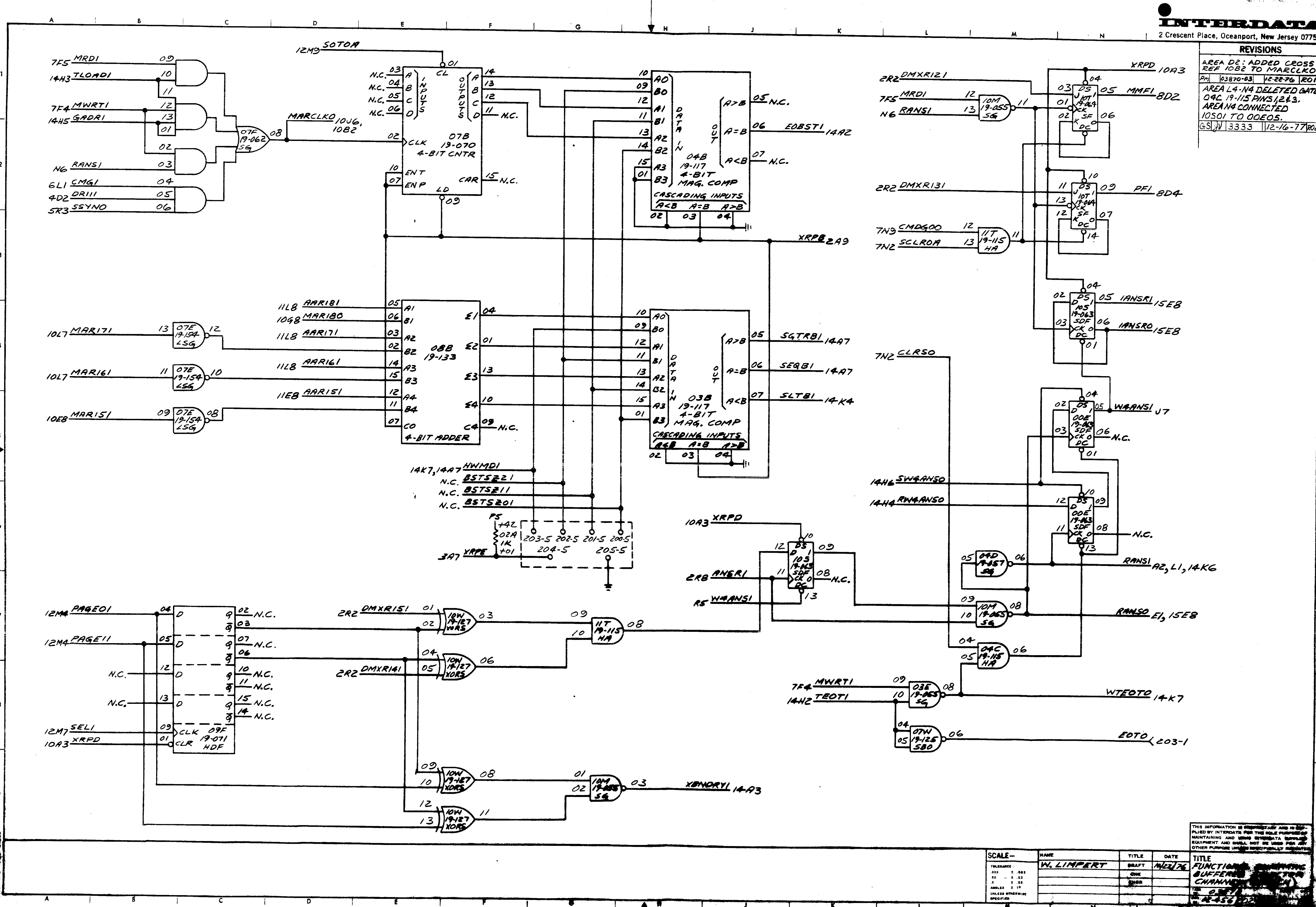
SCLR08

SCALE—

NAME	TITLE	DATE
W. LIMPERT	DRAFT	10/22/76
	CHK	
	ENGR	

TITLE
FUNCTIONAL SCHEMATIC BUFFERED SELECTOR CHANNEL (BSELCH)

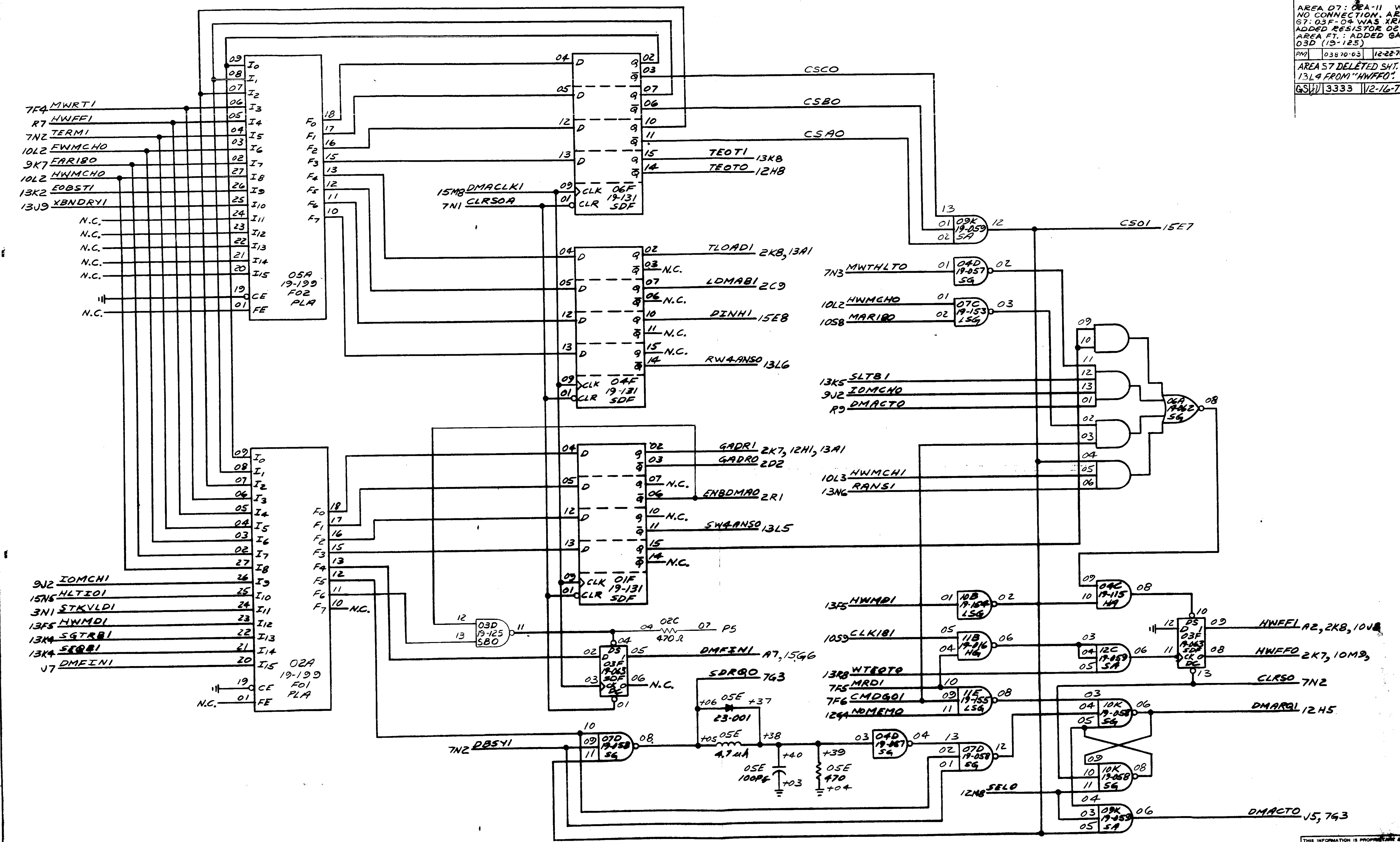
DWG NO. 03870
REV NO. 02-456 R02


INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757
REVISIONS
AREA D2: ADDED CROSS REF 10B2 TO MARCLKO
03870-03 10-22-76 R01
AREA L4-N4 DELETED GATE 04C 19-115 PINS 1,2 & 3. AREA N4 CONNECTED 10S01 TO 00E05.
3333 12-16-77 R02
MRDI
TLOADI
MWRTI
GADRI
RANSI
CMGI
DRIII
SSYNO
07F 19-062 SG
MARCLKO 10J6, 10B2
SOTOA
07B 19-070 4-BIT CNTR
INPUTS
OUTPUTS
N.C.
CLK
ENT
ENP
CAR
LD
04B 19-117 4-BIT MAG. COMP
DATA IN
OUT
CASCADING INPUTS
A>B
A=B
A<B
E0BSTI 14A2
XRPB 2A9
AARI8I
MARI80
AARI7I
AARI6I
AARI5I
MARI7I
MARI6I
MARI5I
07E 19-154 LSG
08B 19-133
4-BIT ADDER
03B 19-117 4-BIT MAG. COMP
SGTRBI 14A7
SEQBI 14A7
SLTBI 14K4
HWMDI
BSTSZ2I
BSTSZ1I
BSTSZ0I
F5 +42 02A 1K +01
XRPE
203-5 202-5 201-5 200-5
204-5 205-5
PAGE0I
PAGE1I
SELI
XRPD
09F 19-071 HDF
CLK
CLR
DMXR15I
DMXR14I
10W 19-127 XORS
11T 19-115 HA
10M 19-055 SG
XBNORYI 14-A3
DMXR12I
XRPD 10A3
10T 19-064 SF
MMFI 8D2
DMXR13I
PFI 8D4
CMDG00
SCLROA
10S 19-063 SDF
IANSRI 15E8
IANSRO 15E8
CLRSO
00E 19-143 SDF
W4ANSI J7
SW4ANSO
RW4ANSO
ANSRI
W4ANSI
04D 19-057 SG
RANSI A2, L1, 14K6
RANSO E1, 15E8
04C 19-115 HA
MWRTI
TEOTI
03E 19-055 SG
WTEOTO 14-K7
07W 19-125 SBO
EOTO 203-1
SCALE
NAME
W. LIMPERT
TITLE
DATE
DRAFT
10/22/76
CHK
TITLE
FUNCTIONAL
BUFFERED
CHANNEL

REVISIONS

AREA D7: 02A-11 WAS NO CONNECTION. AREA G7: 03F-04 WAS XRPB. ADDED RESISTOR 02C. AREA F7: ADDED GATE 03D (19-125)
PM 03870-03 12-22-76 R01

AREA S7 DELETED SHT. REF. 13L4 FROM "HWFFO".
GS 3333 12-16-77 R02



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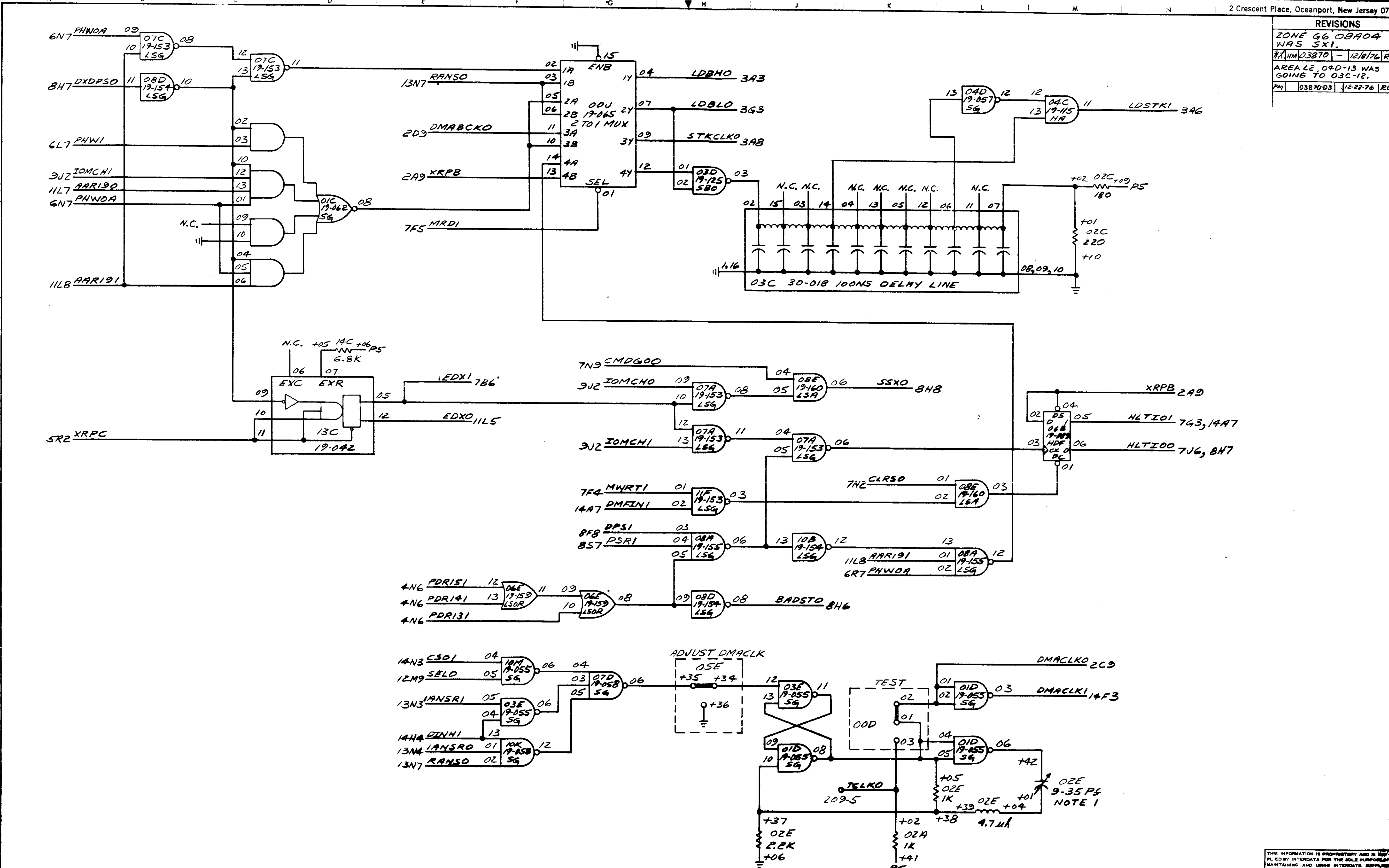
SCALE–	NAME	TITLE	DATE	TITLE
TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	W. LIMPERT	DRAFT	10/25/76	FUNCTIONAL BUFFERED CHANNEL
		CHK		03870
		ENGR		02-456 R02

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

ZONE G6 08A04 WAS SX1.			
IIM 03870	–	12/8/76	R01
AREA L2 04D-13 WAS GOING TO 03C-12.			
PM	03870-03	12-22-76	R02

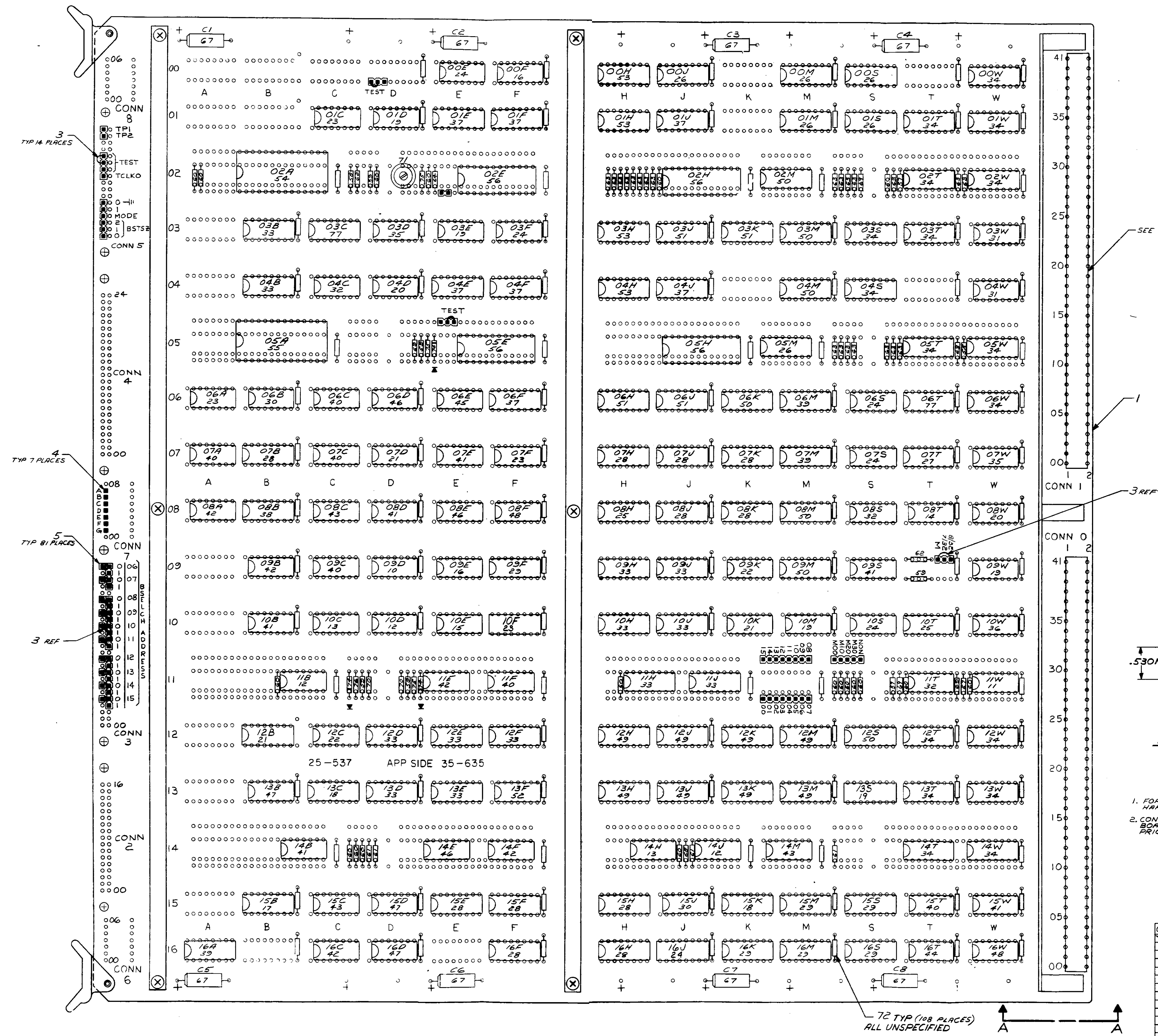


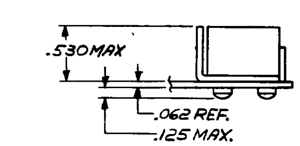
NOTES:
1. ADJUST DMACLK1 FOR A PERIOD OF 80NS ±10%.

SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ±.005 XX ±.02 X ±.03 ANGLES ±1° UNLESS OTHERWISE SPECIFIED	W. LIMPERT	DRAFT	10/25/76
		CHK	
		ENGR	

TITLE: FUNCTIONAL SCHEMATIC BUFFERED SELECTOR CHANNEL (BENCH)

03870 — 02-456 R02 — SHEET 15





PARTIAL VIEW A-A
TYP 3 PLACES

1. FOR MOUNTING OF STANDARD HARDWARE SEE 16-642 D12.
2. CONTACTS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

REVISIONS

Description				
LOC 02C: ADDED RESISTOR (ITEM 53) BETWEEN PINS 4 & 7				
PM	03870-02			R01
RELEASED FOR PRODUCTION MFG. ENG. DATE				
LOC. 12B, ADDED IC (ITEM 21).				
GS	AV	3323	8-12-77	R02
LOC 16J: ADDED IC (ITEM 28). LOC 10F: ADDED IC (ITEM 23). LOC 13S: ADDED IC (ITEM 19).				
GS	AV	3180	10-7-77	R03
LOC. 11T: ADDED RESISTOR (ITEM 57) BETWEEN PINS 32 & 21. ADDED CAP. (ITEM 69) BETWEEN PINS 33 & 20. RES. BETWEEN PINS 34 & 19 WAS SPEC'D ITEM 62. LOC 02S: ADDED CAP. (ITEM 69). LOC. 02T ADDED RES. (ITEM 57) BETWEEN PINS 33 & 20.				
GS	AV	3333	12-16-77	R04

COMPONENT	REF DESIGNATION

NAME	TITLE	DATE
W. LIMPERT	DRAFT	10/4/76
H. MATTER	CHK	10/4/76
E. D'ANGELO	ENGR	
R. BARKER	Q.C.	
S. MESSINA	MGR.	

TITLE: ASSEMBLY BUFFERED SELECTOR CHANNEL (BSELCH

03870

NO. 35-635 R04 E03 — SHEET 1 OF 1

INDEX

B SELCH

PERKIN-ELMER

CUSTOMER SERVICE DIVISION

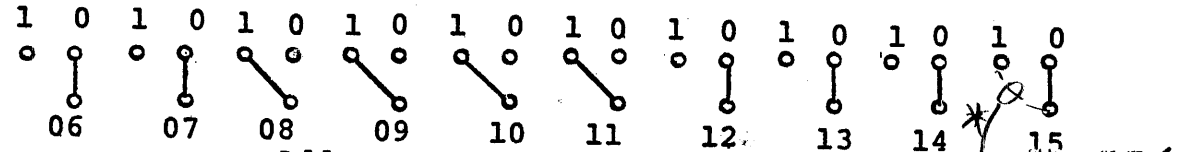
MODULE REPLACEMENT CHECKLIST

PRODUCT NUMBER: 35-635M01	PRODUCT DESCRIPTION: B Selch (New Protocol)

SERIAL NUMBER _____ REVISION LEVEL _____ DATE _____

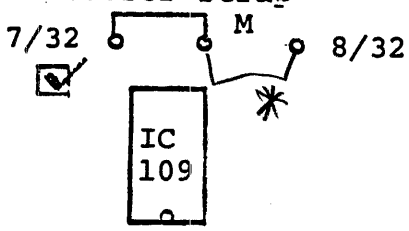
ASSOCIATED DOCUMENTS:

B Selch Maintenance Manual 29-590
700/800 Business Systems Installation Manual 29-645



Address Strapping - Standard Address = XFØ ☑

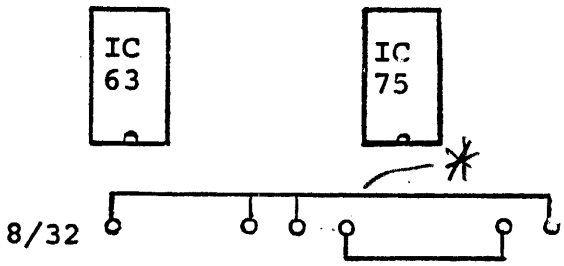
Processor Strap



☑ E5

E4 — A 147

Add Strap E4-E5 to Enable New Protocol

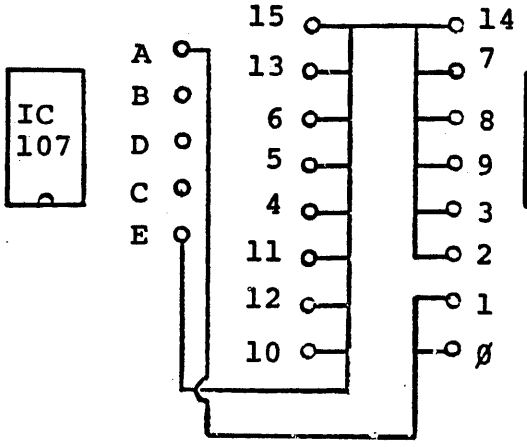


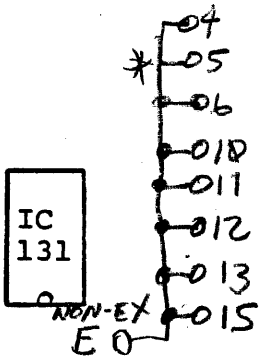
8/32 'F1' Selch setup = *

☑ 7/32

MEMORY BANK STRAPPING

☑ 128KB





MINIMUM OPERATIONAL VERIFICATION:

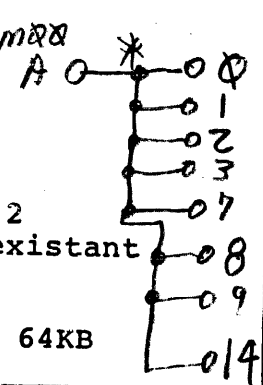
06-161 Selch Test
06-159 Systems Ex.
Customer Software for 30 Min.

NOTES:

1-B Selch in 7/32 does not utilize burst mode.
2-Move Buffers in Selch Test (06-161).
3- Strapping E4-E5 Changes Function Level to F01

A = Bank Ø
B = Bank 1
D = Bank 3
C = Bank 2
E = Non-existant

Each Stake = 64KB



A1933-1

OPTION STRAPPING	C/E INDICATE CHANGES ✓ = As checked on strapping guide. X = Indicates change in option.
1. Address Strapping	✓
2. Processor Strap	✓
3. Burst Size	✓
4. New Protocol	✓
5. Memory Bank Allocation	✓
C E Initial Change	
Date	

C E Information