EAGLE on SGI
837+5/20/44(512) 1lv=1
gap1=20
gap2=30

SMD 2190

High-performance Multibus® Storage Module Device (SMD) Disk Controller

User's Guide

SMD 2190
DISK CONTROLLER
USER'S GUIDE

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PREFACE

This User's Guide is intended to be a reference document for users who already have a general understanding of the function of disk controllers, a general knowledge of Multibus system needs, and a familiarity with disk drives. It does not intend to provide information that should already be available to the user, instead it provides detailed descriptions of features over which the user has parametric control. The following information is provided:

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SECTION 1

INTRODUCTION TO THE SMD 2190

OVERVIEW

The SMD 2190 is an intelligent Controller/formatter for Storage Module Device (SMD) standard disk drives. Devices on the Multibus may command the SMD 2190 to perform a disk function, such as READ or WRITE a sector (or more) of data into or out of System Memory. All such functions have an extended list of the parameters to define the exact function to be performed. This list is called the IOPB (Input/Output Parameter Block) and is found in common memory, that is, memory accessible to both the requesting device, such as a CPU, and the SMD 2190. In order to cause a disk function to be performed, the IOPB is built in memory, a pointer to the IOPB is written into the Address Registers, and a "GO" is issued to the Command Register. The function is automatically completed by the SMD 2190. Both an "Operation Done" interrupt and "Done Status" are provided.

The SMD 2190 supports a wide variety of system configurations including 8- and 16-bit (or mixed) systems, single or multiple CPUs and other bus masters, serial and parallel bus priority, single user or multiuser/multitask environments, absolute or relative addressing modes, operation in Buffered Mode, Cached Mode or Direct Mode, as well as other features.

Multiple disk drives and types with varying speeds and capacities can be controlled simultaneously. The Interleave Factor, which is software programmable, can be optimized for optimum system-wide performance based on a wide number of factors. An optional on-board cache with an intelligent prefetch caching algorithm provides very high performance in systems that tend to make sequential disk sector accesses in separate sequential operating system transactions.

A programmable Spiral Formatting skew factor allows multitrack transactions to not cost ar extra disk revolution due to head-to-head select times or track-to-track seek time:. Finally, a number of initialization parameters control a wide number of operating parameters such as whether or not to correct errors with ECC, whether or not to move known bad (uncorrectable) data, the number of sectors per track, heads per unit, bytes per sector, and gap sizes in the disk formatting.

This document is a basic User's Guide for the most fundamental of operations, and makes no attempt to discuss File Management Systems, Disk Operating Systems and other such elaborate program structures.

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SECTION 2

MODES OF OPERATION

BUFFERED MODE

The SMD 2190 has three basic modes of operation: the Buffered Mode, the Cache Mode, and the Direct Mode. In the Buffered Mode, all data to or from the disk is buffered on a sector basis in an on-board non-Multibus-accessible buffer memory. Sector sizes are programmable but are limited to a maximum of 3512 or 7608 bytes with normal or extended size buffers respectively. All recovery from data errors is done in the local buffer with no bus activity until data (on a READ) is ready to be DMAed in its final form into Multibus memory. The lowest Interleave Factor usable in the Buffered Mode is 2 (2 to 1) which will typically use about 30% of the bus bandwidth of a typically configured system during a large multisector transaction. This allows for a high throughput rate while still leaving enough of the bus for all of the other bus transactions typically needed for normal simultaneous operation. For comparison, the Cache Mode allows a 1 to 1 interleave but still only uses the same 30 percent of the bus bandwidth.

DIRECT MODE

The Direct Mode operates differently. Data does not go through the on-board sector buffer, but instead goes directly to and from Multibus-accessible memory. If error correction is necessary (on a READ), all bit manipulations must take place over the bus, which is, of course, slower than manipulation in the local buffer. If uncorrectable data errors exist, erroneous data will then exist in Multibus memory. Of course, the user is made aware of this fact with the Error and Status bytes of the IOPB.

Operation in the Direct Mode allows sector sizes to be up to a full track long (one sector per track) with one stipulation. The error detection span of the ECC codes allows detection of errors in a full track sector, but the maximum span of the correction algorithm is 4096 bytes. This means that the limit of sector size in the Direct Mode is 4096 if you need error correction, and is a full track if you do not. Retries will still be done (unless disabled in the UIB) if an error is detected. Also, due to timing constraints, most drives must be run at sector sizes greater than 256 bytes if direct mode is to be used.

In the Direct Mode, the Interleave Factor can be 1, that is, contiguous physical and logical sectors. The primary disadvantage of using the Direct Mode is that while the sector of interest is under the Read/Write head of the disk, the SMD 2190 requires unrestricted access to the Multibus and its memory. The bus is released only between sectors of a multisector transaction, and the controller must be able to re-acquire the bus before the next sector comes around, otherwise it will have to wait a full disk revolution to pick up the next sector. This allows high priority events to interrupt the disk activity if necessary, but with a relatively high price in terms of data throughput. The bus is available for about 70 microseconds between sectors for uninterrupted operation in a Direct Mode multisector READ (READ DIRECT). If used in a system using Common Bus Request, the SMD 2190 will operate totally according to Multibus specifications, but the same high price can be incurred if another device locks out the disk from the bus during attempted disk transactions. One additional requirement is that the *memory access time must be less than or equal to 480 nanoseconds for every transfer.* This requirement causes some dynamic memory boards to be incompatible due to refresh requirements.

These restrictions on bus usage during Direct Mode READS and WRITES are perfectly acceptable to a number of applications using a classic Multibus environment and cause no hardships in some specialized Multibus environments. Whether or not the bus latencies and overall bus bandwidth characteristics of Direct Mode operation are acceptable to your application must be considered carefully.

BUFFERED MODE/DIRECT MODE INTERACTION

Data written in either mode can be read in either mode. Multiple sectors of data written in Direct Mode with an Interleave of 1 will, however, be read back slowly (one sector per revolution) if read in the Buffered Mode. Also consider that it makes no sense to use the Direct Mode unless you are using an Interleave Factor of one and are using multisector transactions, or unless you need very large sectors. If you wish to mix Direct Mode transactions and Buffered Mode transactions on one

disk unit, you should format part of the disk with an Interleave of one and part with an Interleave factor of two or more. The Interleave Factor that you use is specified while formatting the disk unit. The READ (81H) or READ DIRECT (91H) and WRITE (82H) or WRITE DIRECT (92H) commands specify whether Direct Mode or Buffered Mode is used. The VERIFY command can operate with any Interleave Factor format since there is no bus activity required.

CACHE MODE

In addition to the Buffered Mode and Direct Mode, the SMD 2190 offers a mode of operation called the Cache Mode. This mode does two things: it allows physically contiguous sectors (Interleave of 1) to be accessed in one revolution of the disk without demanding excessive bus bandwidth, and it does a prefetch and caching of subsequent sectors on the same track in anticipation of a request for that data.

Many operating systems, particularly the UNIX and UNIX-like operating systems, commonly break file accesses into multiple accesses with atomic sizes from one to three sectors each. This is true even though the file may be many sectors long and may be written on the disk in logically consecutive sectors. Since there is necessarily an operating system interaction between these accesses, there is a delay between accesses that will always be long enough such that, if the disk is formatted 1 to 1 (Interleave = 1), the next sector of interest will have already traversed beneath the read head when the access is requested. The result is, naturally, that only one sector (or other atomic size) access can be made per revolution.

Many operating systems have lessened this problem by adding a "software interleave" to the disk hardware interleave, but this reduces the average throughput to something equivalent to a four or five to one interleave (or worse) for accesses of this type. Although the nature of disk activity in a real system is multifaceted and highly variable based on many factors, file activity of this type is almost always a majority of the activity. The only exception to this is in systems in which the files have become extremely scattered or where the memory available is much too small.

The SMD 2190 Cache Mode operation is such that the average access to the first sector (or atomic unit) of a group of contiguous sectors accessed by separate disk transactions, is ruled primarily by the seek time and rotational latency of the drive as always. All subsequent accesses to the trailing sectors are made directly from the cache buffer without regard to the current location of the disk, other bus activity, or how much overhead exists between accesses. Since data is read on a 1 to 1 basis into the cache buffer, data is read at the maximum rate specified by the disk , and there is no possibility of data overrun or underruns. Since no "software interleave" is necessary, the final result is a significantly better throughput rate than with other approaches, for a majority of the disk transactions seen in most systems of this type.

Although Cache Mode operation can be used with the normal size SMD 2190 buffer which can cache up to six sectors of 512 bytes each, most users who wish to use Cache Mode will choose to use the optional extended size buffer. With the extended buffer, the cache size is up to 23 sectors of 512 bytes each. (With differing sector sizes, a different number of sectors can be cached.) The cache size is programmable and can be any nonzero number of sectors that will fit in the buffer. Most users are expected to set the cache size to be one half of a track of data. Therefore, if a track of data has 32 sectors, most users will opt for a cache size of 16 sectors.

FINE TUNING YOUR SYSTEM

One could ask why not always set the cache size to the maximum size of 23, which is perfectly acceptable. The decision is multifaceted and can be influenced by any natural tendency your operating system may have towards grouping of allocated sectors. The SMD 2190 will complete its caching function once it is started, and will incur some overhead before being able to start a new access. Therefore, there is a trade off between incurring too much overhead by bringing unnecessary sectors into the cache, and incurring the possibility of a wasted disk revolution by bringing in too few sectors.

Since many operating systems have a tendency to group sectors during the resources allocation function, the SMD 2190 caching algorithm allows a further refinement called "Grouping." This allows a track to be broken into groups of a size that makes sense for your application. If your system tends to group sectors into, for example, eight-sector units, you may choose to set your group size to either eight sectors, or, if there is some reasonable probability of two consecutive units of sectors being accessed sequentially, 16 sectors. If the cache size (or Group Size)

is 16, then two sets of eight sectors will be brought into the cache if a READ is made to the first sector or group of sectors, in anticipation of subsequent READs.

If a track is broken into two groups of one-half track each, then the track is formatted 1 to 1 all the way around the disk. If the track is broken into more than two groups, it is further possible to interleave the groups. For example, a 32-sector track could be broken into four groups of eight sectors each with groups interleaved 3 to 1. This would allow multiple, consecutive, eight-sector groups to be accessed in one revolution, without either group incurring extra overhead. The compromise however would be that it would take three revolutions of the disk to read all the data on the track. That would, however, be irrelevant if full track transfers are uncommon in the system.

EXAMPLE CACHE MODE CONFIGURATION

All of the above may sound very complicated or confusing, but it merely demonstrates the extreme flexibility of the Cache Mode in allowing optimization for your system. Unless you have reason to do otherwise, use a one-half track cache/group size. Referring to the UIB format in Figure 5, and assuming your disk has 32 sectors per track, initialize the drive with the GRP (Group Enable) and CE (Cache Enable) bits and the LSB of the Interleave Factor byte (byte 6) set to 1, and the Group Size (Byte 15) set to 16 (decimal). When you Format the track, it will be formatted with a 1 to 1 sector interleave (contiguous sectors). Since the CE bit is ON, caching is enabled. When you read any sector or number of sectors, the SMD 2190 will automatically read the subsequent sectors up to the end of the caching group. Subsequent reads to data in cache will be completed with zero latency.

If you subsequently reinitialize with the CE bit OFF (GRP bit still ON), multisector reads are still done on a 1 to 1 basis into the buffer but no caching to the end of the caching group is done. If, for some reason, you want caching to be disabled on a selective basis, such as operating system accesses for which subsequent sequential sectors may never be relevant, leave the CE bit ON and use the READ NONCACHED (94H) command. It operates the same as the above but does not require re-initialization. If the GRP bit is 0, then the CE bit is ignored.

Although the intelligent caching algorithms are operating as long as the GRP and CE bits are ON, the user need never be aware of their actions. Operation is totally automatic and transparent to the user.

Multisector transfers of any size can be made disregarding starting sector, sector groupings, track changes, or other factors. Since the caching group size is programmable, it is possible that the number of caching groups is a noninteger. The SMD 2190 allows fragmented caching groups at the end of a track. No data is automatically cached across track boundaries.

SECTION 3

CONTROLLING THE SMD 2190

I/O REGISTERS

The four input registers and one output register of the SMD 2190 allow the user to point the SMD 2190 to an IOPB in memory and initiate a command. They are shown in Figure 1 on the following page. The registers are referred to as R0, R1, R2, and R3 and are accessed via the IN and OUT (or equivalent) instructions. The 8- or 16-bit absolute I/O address can be selected via the SW1 and SW2 Dip Switches. The least significant two bits of the address select one of the four registers.

The IOPB address pointer registers, R1, R2, and R3, must be loaded with a 24-bit memory pointer to the first byte of the IOPB. They are write-only registers.

R0 is both Read and Write (Status and Command, respectively). The Command Register (R0) format is shown in Figure 2 on the following page. Four functions are performed: Hardware Reset, Select Bus Width, Clear Interrupt, and Go.

Bit 7 of the Command Register causes an actual hardware reset to the controlling microprocessor (8085), which forces the microcode to restart at 0. This does exactly the same thing as asserting the INIT/line on the bus. To use this function, set the bit to '1' and then set it to '0' at least two microseconds later. To verify completion of the hardware reset function after the above sequence, observe the hardware BUSY bit. It will go to a '1' and then go to a '0', at which time reset is complete.

Bit 5 of the Command Register (R0) selects an 8- or 16-bit data bus. Bit 1 is used to clear a pending interrupt and turn off the Operation Done status bit. This is accomplished by writing 02 (or 22) to R0.

Bit 0 is used to start a new function specified in the IOPB (pointed to by R1, R2, and R3). This is done by issuing a GO (01 or 21) to R0. The user may also write a CLEAR INT and GO (03 or 23) to R0, if desired. The SMD 2190 will first clear the interrupt (and status bit), then proceed to execute the command and finally, set the new interrupt (and status bit).

	WRITE	READ	ADDR1	ADDR0
RO	COMMAND	STATUS	0	0
R1	XMB IOPB MEM.	---	0	1
R2	MSB ADDRESS	---	1	0
R3	LSB REGISTERS	---	1	1

I/O address bits ADR2-ADRF of RØ are defined by dip switches SW1 and SW2.

Figure 1. SMD 2190 I/O Registers

COMMAND (R0)

7	6	5	4	3	2	1	0
RESET	0	BUS	DSBL INTR	0	0	CLR INT	GO

STATUS (R0)

7	6	5	4	3	2	1	0
R3	R2	R1	R0	0	STAT CHNG INT	OP DONE INT	BUSY

Figure 2. R0 Command/Status Bytes

The Status Register (R0) has three operation status bits and four drive status bits. The BUSY bit indicates when the SMD 2190 is busy performing an operation. The Operation Done Interrupt bit indicates when a disk operation has been completed. The Status Change Interrupt indicates a change in disk status (if enabled in the UIB as explained later). A visual indicator (LED 1) also indicates a pending interrupt. Further information is also found in the IOPB.

An interrupt-driven system will typically check the status bit to verify that the disk was the source of an interrupt. More information regarding interrupts is provided in the interrupt-driven systems section. For those applications not requiring the Operation Done Interrupt, bit 4 of the Command Register (R0) may be set. When this bit is '0', the SMD 2190 will generate interrupts on whatever level is selected by the straps on the board (one of eight levels).

A system that does not use interrupts (status-driven) will typically have no need for the Status Register and will use the Status Code byte in the IOPB. The clear interrupt command need not be issued under these conditions.

The four MSBs of the Status Register (RO) indicate the Ready Status of each of up to four separate SMD drives and can be observed at any time. If initialized to do so, an interrupt is generated when the Ready Status of any drive changes. This is most useful when overlapped seeks are used. In that case, a Normal Operation Complete Interrupt indicates acceptance of the SEEK command by the drive; then, a subsequent Status Change Interrupt is generated when the drive has completed the seek operation. This is described in more detail in later sections.

INPUT/OUTPUT PARAMETER BLOCK

The Input/Output Parameter Block (IOPB) directs the operation of the SMD 2190. The format of the IOPB is shown in Figure 3. Although some commands do not need certain parameters, the format of the IOPB remains consistent.

Since the Status Code and Error Code bytes of the IOPB are updated by the controller, the IOPB must reside in RAM, although the operating program may reside in PROM.

A description of each IOPB element follows the figure.

0	COMMAND	
1	COMMAND OPTIONS	
2	STATUS	
3	ERROR	
4	UNIT SELECT	
5	HEAD SELECT	
6 7	CYLINDER SELECT	MSB LSB
8 9	STARTING	MSB LSB
10 11	SECTOR COUNT	MSB LSB
12	DMA COUNT	
13 14 15	BUFFER ADDRESS	XMB MSB LSB
16 17	I/O ADDRESS	LSB MSB
18 19	RELATIVE ADDRESS	MSB LSB
20	RESERVED	
21 22 23	LINKED IOPB ADDRESS	XMB MSB LSB

Figure 3. IOPB Format

COMMAND CODES

This byte identifies the nature of the operation to be performed. A list of Command Codes is found in Table 1, and a detailed description of each code is provided in Appendix A.

Table 1: Command Codes

81	READ	8A	SEEK
82	WRITE	8F	RESET
83	VERIFY	90	READ RAW DATA
84	FORMAT TRACK	91	DIRECT READ
85	MAP	92	DIRECT WRITE
86	REPORT CONFIGURATION	93	READ ABSOLUTE
87	INITIALIZATION	94	READ NONCACHED
89	RESTORE		

COMMAND OPTIONS

This byte controls data bus width for the data buffer transfer and for independently controlling linked IOPBs. It also sets the addressing mode for these two functions independently. Although four addressing modes can be defined, only two are supported.

STATUS CODE

Once a disk command is accepted, operation status is provided. The three possible status indicators are listed below.

80H = Operation Successful, ready for next command
81H = Operation in progress, busy
82H = Error on last command

The user generally initializes the IOPB with a 00 in the Status Byte to indicate that the operation has not yet been acknowledged. It is not necessary to observe the BUSY (81H) indication before looking for successful (80H) or unsuccessful (82H) completion. In fact, operations that can show immediate (or very fast) completion may never report the BUSY condition.

ERROR CODES

If the Status Code = 82H after an operation, this byte provides an error code. A complete list of error codes can be found in Appendix B. If the Status = 80H, this byte provides the number of automatic error recovery procedures required before successful completion of the operation. The upper four bits indicate whether Error Correction has been applied, whether Bad Data has been transferred (only possible if enabled), and whether a RESTORE and RESEEK was done. The lower four bits represent the number of retries required.

7	6	5	4	3 2 1 0
EC	BD	0	RS	NUMBER OF ROTATIONAL RETRIES

Figure 4. Error Codes for Sucessfully Completed Operations

UNIT SELECT

This byte is used for the binary selection of a disk unit from zero to three.

HEAD SELECT

This byte is used to Select the head to be used. The head address is determined by the type of SMD drive being used.

CYLINDER SELECT

This 16-bit word selects the disk cylinder.

STARTING SECTOR

This word is used for the 16-bit number (0-N) of the starting sector of the operation. The sector and cylinder numbers start from 00.

SECTOR COUNT

This word specifies the 16-bit number of sequentially numbered sectors to transfer. implied seeks are automatic when crossing a cylinder or head boundary.

DMA COUNT

This byte sets the maximum number of bus transactions (bytes or words) to allow in one burst (bus acquisition). The minimum DMA count is three. If the DMA COUNT byte is set to zero, then a full sector is transferred.

BUFFER ADDRESS

This three-byte (24-bit) value points to the beginning of the system memory data buffer. Its effective value is based on the addressing mode (either Absolute or Memory Sector Relative).

I/O ADDRESS

This 16-bit value specifies where the SMD 2190 Input/Output Registers are located within the Multibus I/O space. It must be set to the starting I/O Address of the I/O Write and Read Register (R0).

RELATIVE ADDRESS

This 16-bit value is the Addressing offset or Memory Sector address and is used only if Relative addressing is used. Future relative addressing modes (1,0 and 1,1) will use this value in different ways.

RESERVED

Byte 20 in the IOPB is not used at this time. In order to insure compatibility with future firmware versions install a '0' in this location.

LINKED IOPB ADDRESS

This three-byte (24-bit) value must point to the address of the linked IOPB if the Link Bit of the Command Options byte is set. All addressing modes apply to this value and the mode may be different from the data buffer addressing mode. In most cases, the Absolute Addressing mode will be used for all IOPBs.

COMMAND OPTIONS BYTE

The Command Options byte of the IOPB provides for several bit mapped options. Each bit of this byte is discussed below.

Bit 7 Link Bit

The Link bit, if set, says to automatically link to the next IOPB as a part of this transaction. Bytes 21, 22, 23 point to the next IOPB. No Done Interrupt is generated until the last linked IOPB in a sequence has been completed, however, the Status and Error bytes of the completed parts of the linked transactions are updated as the individual IOPBs are satisfied. The Linked IOPBs section more completely describes linked transactions.

Bit 6 REL1 IOPB &
Bit 5 REL0 IOPB

If the Link bit is set, these bits identify the addressing mode of the pointer to the next IOPB (bytes 21, 22, 27). If the bits are 00, the Absolute Address in the pointer is used. If the bits are 01, the Memory Sector Relative Mode as described below, is used to calculate the effective address. If the Link bit is '0', these bits are ignored. Other bit combinations are reserved for future addressing modes.

Bit 4 Bus IOPB

If this bit is '0', the linked IOPB is addressed in Byte (8-bit) mode. If this bit is '1', the linked IOPB is addressed in Word (16-bit) mode. If the Link bit is '0', this bit is ignored.

Bit 3 RSRV

If this bit is a '1', the drive will remain Reserved after completion of this IOPB for dual ported drives that have been initialized as such by the UIB. If this bit is a '0', the drive is released after this operation. If the drive is not initialized for dual porting, this bit is ignored. (See also Dual Porting Section.)

Bit 2 REL1 Buffer
Bit 1 REL0 Buffer

These bits define the method of calculating the effective Buffer Address. If the bits are '00', the effective address is the absolute number found in bytes 13, 14, 15. If the bits are '01', the Memory Sector Relative Mode, is used to calculate the effective address. Other bit combinations are reserved for future addressing modes.

Bit 0 Bus Buffer

If this bit is '0', the data DMA is done in Byte (8-bit) mode. If this bit is '1', the data DMA is done in Word (16-bit) mode. Commands that do not move any data over the Multibus ignore this bit.

ADDRESSING MODES

The SMD 2190 currently supports two addressing modes; Absolute and Memory Sector Relative. These two modes are used to calculate effective addresses for both Buffer pointers and Linked IOPB pointers and are shown in Figure 4.

In the Absolute Mode, the pointers are literals. In the Memory Sector Relative Mode, pointers are calculated by taking the Relative Address word (bytes 18, 19) of

the IOPB shifted left four places into a 24-bit field of zeros and adding that to the 24-bit values in the Buffer Address or Linked IOPB Address as appropriate. This is primarily useful to support the Memory Sector Relative addressing scheme of the 8086. Future address modes may be added as customer inputs are received.

DUAL PORTING

If the SMD 2190 is to be used in conjunction with a drive implementing the Dual Port Option, then the Dual Port Drive bit in the UIB must be set to a '1' for the Initialize command. When the SMD 2190 attempts to select a drive that is reserved by the other channel, it will wait 500 milliseconds for the drive to go "not busy" before reporting the error back to the operating system. If the RSRV bit in the Command Option byte of the IOPB is set to '0', then the channel will be released on completion of that operation. If the RSRV bit is set to '1', then the channel will remain reserved at the completion of that operation (this feature should be used for overlapped seeks, read after writes, and other back-to-back operations).

Most dual ported drives have a protection timeout that will release a channel after a specified length of time (typically 500 milliseconds) if the drive has been deselected but not released on that channel. If so desired, this timeout can be disabled by a switch in the drive.

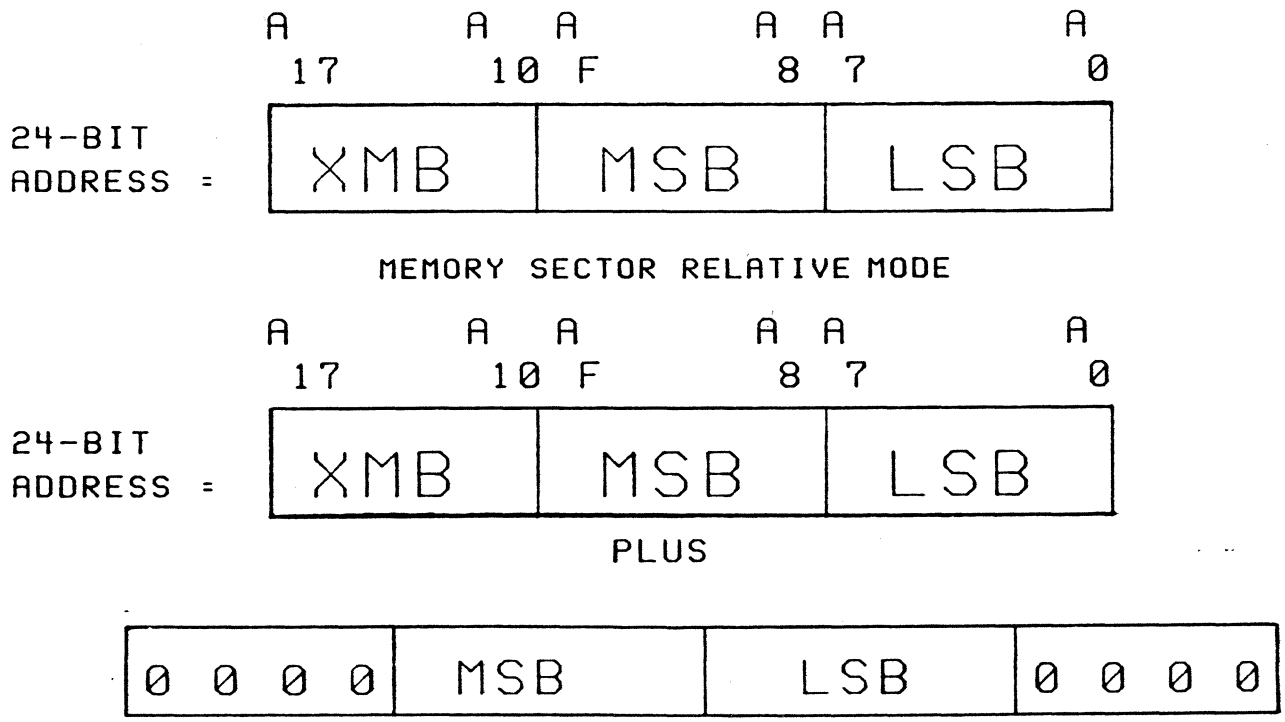

Figure 5. Addressing Modes

USE OF THE STATUS AND ERROR BYTES

The Status and Error bytes of the IOPB are normally initialized by the user to 00 before the transaction is started. When the GO bit is set in R0 (hardware register), the SMD 2190 automatically fetches the IOPB starting at the address pointed to in R1, R2, and R3 as described earlier, and updates the Status byte to a 81H to indicate that the operation is in progress (BUSY). The SMD 2190 then does all the work necessary to complete the transaction. If the transaction has been successfully completed, the Status byte is then set to 80H to indicate it is a successful completion and is ready for the next transaction. An interrupt is also generated if enabled.

If an unrecoverable error condition is encountered, the Status byte is set to 82H and an Error Code is written into the Error byte. An interrupt is also generated, if enabled. The Error Codes are are described in Appendix B. A "most primitive error" reporting approach reports the lowest level causative factor which allows for a quick determination of the true source of the error. This avoids the common problem of higher level errors masking lower level problems, typical of the diagnostic reporting techniques of many competitive units.

If the Status byte indicates a successful completion, the Error byte takes on a new meaning which can be useful in predicting future problems in a slowly degrading system. The lowest four bits indicate the number of retries required to complete the transaction. Bit 7 indicates if Error Correction has been applied. Bit 4 indicates if a Restore and Reseek sequence was required. Bit 6 is set if known bad data (uncorrectable) has been moved into system memory. This is only possible if the SMD 2190 has been initialized in its UIB to move bad data.

It should be understood that with any error correction technique there is a minute possibility of miscorrected data. The ECC technique used by the SMD 2190 is the highest reliability technique used by any known competitive unit and is less susceptible to miscorrected errors than most competitive units.

The SMD 2190 first retries data reads found to be in error and only after an error is deemed to be a "hard error" is error correction attempted using ECC algorithms. The confidence in data received without error on a Retry should be considered just

as high as that received without error on the first try, but a large number of retries over a period of time may indicate a gradual degradation of the system or the stored data on disk. This may be due to media contamination, degraded heads, or other factors. The intention is to allow preventive action before the disk degrades beyond its useful limits or before uncorrectable hard errors appear. System performance will, of course, degrade if a large number of retries or error corrections become necessary.

The Initialization section describes the large number of system operating options available with regard to error recovery.

SECTION 4

SOFTWARE INTERFACE CONSIDERATIONS

INTRODUCTION

The SMD 2190 is exceptionally simple to use. It is essentially automatic in nature, including error recovery and executes macro-level (operation oriented) commands. The software operating environment may be characteristically one of two types, Interrupt driven or Status driven.

STATUS DRIVEN SYSTEMS

Single user/Single task systems are typically Status driven; that is, once a command is issued, the program waits for completion of the command, as indicated by observing Status, before proceeding to the next operation. This arrangement is perfectly suitable for many systems and is the easiest to implement. For such systems, all interrupts are disabled by removing W17 as described later in Section 7, Option Switches and Straps.

Status driven systems have no need for the Status hardware register (R0), unless Drive Ready Status is of interest, and operate by observing the Status Code byte of the IOPB. When the IOPB is originally written in system memory, the Status Code and Error Code bytes should be initialized to '0'. When the SMD 2190 recognizes the GO command (01 or 21 output to R0) it puts operation status in the Status Code byte. An 81H indicates Busy (operation in progress), 80H indicates Ready For Next Command (operation successfully completed) , and a 82H indicates Error on Last Command. If an error is indicated, the Error Code byte indicates the nature of the error as defined in Appendix B.

The only routine precaution that should normally be taken in a Status-driven system is a timeout to protect against system hang-ups. The SMD 2190 has internal timeouts to protect against disk drive oriented hang-ups and Multibus access timeouts, once the command is accepted (typically 30 microseconds after issuing the command).

The following flowchart indicates operation of the SMD 2190 in a status driven system. The timeout is optional and its implementation is determined by system hardware, which normally includes a realtime clock (which may run on an interrupt level even though the system is status driven) or a hardware interval timer. If used as shown in the flowchart, the timeout duration should take into consideration the normal time to complete the given operation, including retries.

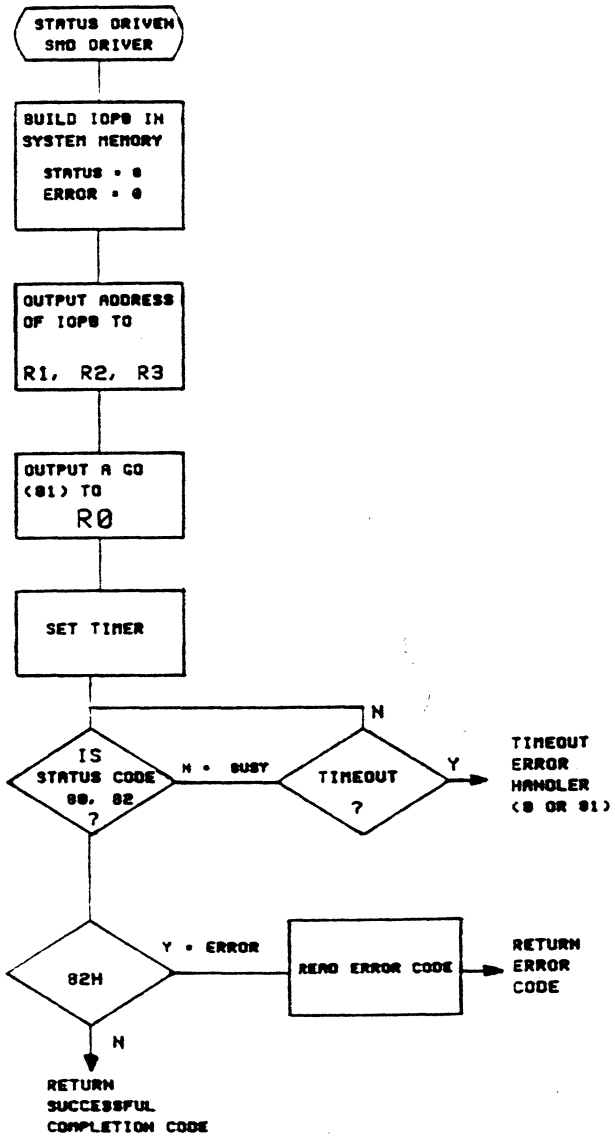

Figure 6. Typical Status Driven SMD Handler

Many systems use a fixed location to hold the IOPB to be used by the SMD 2190. In such systems, it is not necessary to rewrite R1, R2 and R3 for each transaction. Except in systems that may routinely have one or more disk drives turned off, or where an operator is required to change a removable cartridge, the Drive Ready Status bits of R0 are seldom observed after initial power ON. Should a drive not be Ready at the time of an attempted operation, a specific error code is returned.

INTERRUPT DRIVEN SYSTEMS

Multiuser/Multitask and some realtime systems are typically interrupt driven; that is, once the command is given, the other programs in the system proceed to run and the CPU is notified of completion (successful or not) of the disk function via an interrupt. There must obviously be an interrupt handler program, and the disk task is generally one of a number of tasks scheduled by a Realtime Operating System of some type. The interrupt can be verified (in a polled-interrupt environment) by reading the hardware Status Register (R0), and can be reset by outputting a Clear Interrupt (02 or 22) to R0, or, if more work is to be done immediately, by writing a Clear Interrupt and a Go (03 or 23) to R0. The interrupt level is selectable via Strap W17.

The hardware interrupt condition is cleared instantaneously upon receipt of any I/O write to the command register (R0), or to any of the address registers (R1, R2, or R3), but the Operation Done or Disk Status Change bits in the Status Register (R0) are cleared only upon receipt of the Clear Interrupt bit. It is also important to understand that the function of clearing the interrupt is controlled by firmware, includes several housekeeping tasks, and takes from 20 to 70 microseconds to complete based on the uncertainty of certain events. If it is necessary for the software to issue separate Clear Interrupt and GO commands, one must be aware that a GO command issued during the up to 70 microsecond uncertainty period can be missed, or can overwrite the Clear Interrupt command. In order to avoid this situation one can either:

1. Insure that at least 70 microseconds elapses after issuing the CLEAR INTERRUPT before the GO is issued. The Address Register can be written to during this period without any problems.

2. Observe that the hardware Operation Done (or Disk Status Change) bit (collectively referred to as the Interrupt Pending bit) is cleared before issuing the next GO command. The SMD 2190 clears the bit as the last item of the Clear Interrupt function, and is the true indicator of completion of the task.

If it is possible to issue a combined Clear Interrupt and Go, it is best to do so since there is no possibility of missing the command and no time is wasted waiting for availability of the hardware register. This is generally feasible if disk commands have been queued up by the operating system. Recall that the hardware interrupt condition can be cleared without issuing the Clear Interrupt command, as mentioned above.

The program must still check the Status Code of the IOPB to determine success of the operation. All Error Codes retain the same meanings as in a Status-driven system. If multiple tasks, or even multiple CPUs in a multiprocessor system, are to have access to the disk it is most common to have a single task, or the Operating System itself, handle intimate scheduling of disk activities.

In addition to the Operation Done and Disk Status Change interrupt-status bits of register R0, a Busy status bit of R0 is provided. It indicates that the SMD 2190 is currently busy doing some operation, and is not available for starting a new command. R0-R3 are, of course, available to any Bus Master (CPU or otherwise) on the BUS. If more than one CPU in a multiprocessor system is to have direct access to the SMD 2190, some contention resolution mechanism should be employed, other than simply observing the Busy bit. Recall that it takes about 30 microseconds from the time that the SMD 2190 recognizes a Go command until the Busy bit goes true.

Care should be taken to not re-enable interrupts in the interrupt handler until after clearing the interrupt. The interrupt handler must normally reset the source of interrupt while interrupts are still disabled. The user may either simply set or pulse the CLR INT bit. If pulsed, the bit must stay on for at least ten microseconds.

Status driven systems (interrupt disabled) do not require resetting of the interrupt. If the user wishes to observe the operation complete LED, which would otherwise stay permanently on, a combination of CLR INT and GO (03 or 23) may be issued. The interrupt bit (and LED 1) is cleared first. This combination command may also be used by an interrupt handler if it wishes to start the next command immediately.

On boards with firmware revisions of 4.10 and greater, if the status change interrupt is enabled in the UIB, the hardware status byte is updated in the following manner. When the board is not busy and no interrupts are pending the disk drives are checked approximately every 16 milliseconds for a change in status. If a change is detected bits R0 through R3 are updated and the Status Change Interrupt is set. The values in R0 through R3 are not updated until the status change interrupt has been cleared. These ready status values and the status change interrupt status are also frozen when an operation done interrupt is pending. When the interrupt or interrupts are cleared, any and all ready status changes since the last update are reported. If the status change interrupt is not set in the UIB then the ready status values are updated without regard to interrupt pending conditions.

USE OF LINKED IOPBS

Single or multisectored transactions may be automatically linked by setting the Link bit to a '1' and providing a pointer to the next IOPB as described earlier.

Set up and start the transaction as always. Only the pointer to the first IOPB is written into the address registers. As soon as the first IOPB is accepted, the Status Code byte in that IOPB is set to Busy (81H). At the end of the transaction of the first IOPB, its Status byte is set to 80H (or 82H, if in error) in the IOPB, but no interrupt is generated unless there is an error (R0 will continue to indicate Busy). If the Link is set, the next IOPB is fetched and its Status Code byte is set to Busy. At the completion of that transaction, the Status Code byte indicates 80H (or 82H, if in error), and so on until the Link bit is not set OR any unrecoverable error is seen in any transaction. In either case, the interrupt is generated to indicate completion, successful or not.

In the case of a successfully completed transaction, all Status Code bytes in all linked IOPBs will be set to 80H (ready for next command -- no error). Only the last IOPB need be checked because any unrecoverable condition in the chained transaction will abort the transaction.

In the case of any unrecoverable condition, the user may see where the transaction was aborted by observing the Status Code byte in the sequential IOPBs. If an 80H is seen, there was no error.

If an 82H is seen, this is where the chain was broken. All subsequent IOPBs will still show '0' for Status to indicate they have not been acknowledged. If the user is interrupted and R0 shows Operation Complete, the last IOPB will indicate either success or abortion (or Error, if encountered in the last IOPB transaction). Typically, the user will remember only the first and last IOPBs. The last to indicate success, and the first to allow tracking down the problem, if an error occurs. A status driven system user may either set a long timeout and observe only the last IOPB, or choose to follow completion of each IOPB in succession.

If a linked transaction needs to be aborted before completion, write a '0' to R0. The current IOPB will be completed, but the link will be broken.

SECTION 5

INITIALIZATION

INTRODUCTION

The SMD 2190 can handle up to four SMD disk drives with differing capacities, data bit capacities, bit rates, number of heads or cylinders and even differing optimum intersegment gap sizes. Varying data rates can also affect the optimum Interleave Factor and there can even be a mixture of optimum Interleave Factors in a mixed system. For example, the SMD 2190 can simultaneously control a Lark (8 MBytes fixed/8 MBytes removable) operating with 256 byte sectors at 9.6 Mbits/sec and a Fujitsu Eagle (474 MBytes Fixed) with 512 byte sectors and running at 15 Mbits/sec.

The SMD 2190's vast flexibility is attribuatable to the Initialize command (87H) which allows all the variables of both the disk drive and the system environment to be set, and therefore optimized for the given application.

UNIT INITIALIZATION BLOCK

Upon power up, Multibus Reset, issuance of the RST bit, or after issue of the Reset (8FH) command at any time, each of the ports in use (from 1 to 4) must be initialized. A sequence of Initialize commands may be linked if desired. In order to Initialize a disk drive unit, simply issue an Initialize command with the proper unit selected and the Buffer Address pointing to the appropriate Unit Initialization Block (UIB) which may be any place in system accessible memory (either RAM or PROM). The format of the UIB is shown in Figure 5.

Interphase will help you configure your system and will send you a UIB Format to meet your needs. For assistance, please call: Applications Engineering Department, (214) 350-9000. In the U.K., please call: (0296) 435661

0	NUMBER OF HEADS		
1	SECTORS/TRACK		
2	BYTES/SECTOR (LOW BYTE)		
3	BYTES/SECTOR (HIGH BYTE)		
4	BYTES IN GAP 1		
5	BYTES IN GAP 2		
6	GRP	CE	INTERLEAVE FACTOR
7	RETRY COUNT		
8	ERROR CORRECTION ENABLE (0 OR 1)		
9	RESEEK ENABLE (0 OR 1)		
10	MOVE BAD DATA ENABLE (0 OR 1)		
11	INCREMENT BY HEAD ENABLE (0 OR 1)		
12	DUAL PORT DRIVE (0 OR 1)		
13	INTERRUPT ON STATUS CHANGE (0 OR 1)		
14	SPIRAL SKEW FACTOR		
15	GROUP SIZE (SECTORS)		
16	RESERVED (0)		
17	RESERVED (0)		
18	RESERVED (0)		

Figure 7. Unit Initialization Block

NUMBER OF HEADS

The number of heads is the number of addressable data heads of your disk unit. This does not include servo heads. In addition, some disk drives have tandem multiple heads on the same disk surface to decrease seek times. These tandem heads are actually accessed by cylinder selection, not head selection. In that case, those multiple heads count as one.

SECTORS/TRACK

The number of sectors you can fit on a track is a function of the size of the track (physical bytes per track) and the size of the sector. Each sector has about 70 bytes of overhead in addition to the number of data bytes, regardless of the data field size. This is split between the header and the two gaps (Gap1 and Gap2).

Other factors include the end of the track gap, whether or not the drive has an embedded servo, and sometimes, the Interleave Factor and operating mode. A set of tables for common drives and configurations is found later in this section. If your drive is not mentioned in the tables, you may choose to call Interphase for advice. The table shows conservative gap sizes and sectors/track that will work for all operating modes: Buffered, Direct, and Cache. In some cases, Buffered mode operation will allow more sectors/track by varying other parameters. For more in-depth information, contact the Interphase Application Engineering Department.

In addition to the obvious function, this parameter is also used to determine that an entire track has been searched for a given sector. The SMD 2190 will allow two revolutions of the disk (2 x this parameter) before reporting "sector not found" if the sector of interest does not exist or has errors in its header.

Your disk drive has sets of switches or straps that must be set to select the number of sector pulses it is to generate per revolution. Consult your disk drive manuals for that information. Setting their switches is commonly an activity that causes problems since an incorrect setting can appear to work but cause the controller to appear to malfunction only on some sectors.

BYTES/SECTOR (LOW BYTE)
BYTES/SECTOR (HIGH BYTE)

The number of data bytes per sector. Normally determined by the software operating system being used. It can be any even number from 2 (4 with ECC) to 3512 (7608 if extended buffer) in the Buffered Mode and any even number up to 65536 in the Direct Mode (maximum of 4096 if Error Correction is required).

BYTES IN GAP 1

The Gap between the Sector/Index and the Start of Header. Determined primarily by the drive being used. Table 2 in this section shows gap sizes for most drives.

BYTES IN GAP 2

The Gap between the End of Header and the Start of Data Field. Determined primarily by the drive being used. Table 2 in this section shows Gap2 sizes for most drives.

INTERLEAVE FACTOR/GRP/CE

The sector interleave factor to be used during Formatting is fully programmable. When the GRP and CE bits (bit 7 and 6 respectively) are '0', a normal formatting mode is used and the lower 6 bits of the byte are a binary sector interleave factor to be used during formatting. The valid range is from 1 to 63, although a reasonable number when using the standard Buffered Mode is usually low (2, 3, 4, etc.) and should never be more than the number of sectors on a track. The optimum interleaving factor is largely determined by the numerous system loading and bus bandwidth variables. A track intended to be used in Direct Mode will generally use an interleave of 1, physically consecutive sector numbering. So long as GRP and CE are '0', this parameter has no operational effect except during the formatting function. A sector or group of sectors written with one interleave factor can be read with any other interleave factor set.

When GRP and CE bits are set to '1' and a track is formatted, group formatting as described in the Cache Mode section is used, with byte 15 setting the size of the group and the low six bits of byte 6 setting the Group Interleave. For use during formatting, both GRP and CE should be either '0' or '1'. During Operation if the GRP Bit is set to '0', then CE is ignored.

Anytime after formatting with GRP and CE set to '1', the CE (Cache Enable) bit may be left ON '1' to enable caching or OFF '0' to disable caching. Caching can also be enabled after normal Buffer Mode formatting, but that seldom makes any sense. Use of the GRP and CE bits are more completely explained in the Cache Mode section.

A table in this section shows minimum suggested interleave factors for normal buffer mode operation. You may always choose a larger interleave factor that may be found to be optimum if your system is heavily loaded and has a lot of interrupt activity that requires heavy bus bandwidth. If you are using Cache Mode operation refer to the Cache Mode section.

RETRY COUNT

The number of rotational retries (0-15) to perform (if a data error is detected) before error correction is attempted. Most users select a Retry Count of three.

ECC ENABLE

If this byte is a '1', Error Correction is enabled. If it is a '0', Error Correction is disabled.

RESEEK ENABLE

If this byte is a '1', a Reseek operation is performed after rotational retries or Error Correction fail to yield positive results. If it is a '0', no Reseek is performed. Note that since this operation includes a seek to track zero (Recalibrate) then back, it can take a long time to complete.

MOVE BAD DATA ENABLE

If this bit is a '1', uncorrectable data, if encountered, is moved into system memory on a Read operation. In this case the Error byte of the IOPB indicates an uncorrectable error as described earlier.

INCREMENT BY HEAD ENABLE

When a multisector operation traverses a track boundary, the controller automatically addresses the next track. If this parameter is a '0', the next cylinder (same head) is accessed, forcing an implied seek. If this parameter is set to '1', the head number is incremented first, accessing the rest of the tracks in this cylinder before a seek to the next cylinder is performed.

DUAL PORT DRIVE

If the byte is a '1', this UIB is for a dual ported drive. The Command Options byte of the IOPB controls reserving and releasing the device. If this byte is '0', this UIB is not for a dual ported drive.

INTERRUPT ON STATUS CHANGE

When overlapped seeks are used, this option allows the system to be interrupted when the disk drive reaches its final destination in addition to the normal interrupt. (The SEEK (8AH) command is complete when the drive accepts the command and starts the head motion). If this byte is a '1' an interrupt is generated any time a disk drive changes its Ready to Read, Write, or Seek status (except as part of an implied seek). If a drive asynchronously changes status, such as with a drive failure or operator intervention, an interrupt is also generated. A bit in the hardware status register (R0), as described earlier, indicates that this is the source of interrupt. If this byte is a '0', no Status Change interrupts are generated.

SPIRAL SKEW FACTOR

This byte controls the track-to-track skewing during formatting to implement the Spiral Formatting feature. The SMD 2190 formats adjacent tracks on a disk such that a sector zero on one is slightly skewed from the next. This is done so that the head select times do not cause the waste of a disk revolution in multisector transactions that overlap track boundaries. The Skew Factor is, therefore, primarily a function of the head switch time, the sector size, and the spin rate. Spiral skew is only applicable when the increment by head option is selected (which is the recommended mode of operation).

For Buffered and Direct Mode operation, it is usually best to set the Skew Factor to the Interleave plus two. For Cache Mode operation, it is usually best to set it to the group size.

GROUP SIZE

When the GRP bit in Byte 6 is a '1', this byte sets the size of the group, as defined in the Cache Mode section. When the sector size is 512 bytes per sector, the maximum is six sectors when used with a normal buffer size and 23 when used with a board with the extended buffer installed.

BYTES 16, 17, 18

Reserved for Future Use. Set them to a '0' to insure compatibility with future options.

SUGGESTED (UIB) PARAMETERS

The following Table and Disk Drive Notes contain a summary of suggested UIB parameter values and relevant disk drive information for existing disk drives and common systems configurations. This set of guidelines will be updated as more disk drive models become available.

Many parameters, such as Interleave Factor, Retry Count, etc., will, of course, operate reliably over a wide range of values with greater or lesser system throughput. The optimum values may be determined heuristically or theoretically during the system development cycle if desired. If your disk drive is not listed in the Table or your system configuration is unusual, you may choose to contact Interphase Corporation for suggested UIB parameters.

The Interleave Factor and Spiral Skew Factor are used only by the FORMAT command. If you are experimenting with different Interleave Factors, you will, of course, have to Reformat your media to see any effect. The SMD 2190 will be able to Read and Write on to a unit reliably even if it has been initialized with a different Interleave Factor than the one it was formatted with. This means you can use older units even if you have later optimized your system for higher performance.

Also, the Gap1 and Gap2 bytes allow optimization for highest reliability based on the actual type of drive being used. The PLO lock time varies significantly from drive type to drive type while still being SMD compatible. Programmability in these parameters insures the ability to operate all current and future SMD drives. Gap1 programmability is particularly powerful in the embedded servo-type drives available from some manufacturers.

Finally, some users have cleverly allowed multiple types of drives to be installed in their systems and determine the system configuration by reading the first sector on one of the drives. They then initialize each drive based on this information. This is very simple to do with the SMD 2190. The only parameter that needs to be correct to read one, or a few, sectors is the number of bytes per sector which is generally consistent from drive to drive in real systems. Simply set the number of sectors/track to be very large during a dummy initialize, read the sector(s) of interest (not crossing a track boundary), and then reinitialize all the ports with correct parameters. Certain parameters, such as Heads/Unit, Interleave Factor, etc., are checked for valid ranges, but the dummy parameters need not be correct for the particular drive in use during this procedure.

Table 2 - Example UIB

UIB BYTE	CONTENTS	HEX VALUE
0	NUMBER OF HEADS	07
1	SECTORS/TRACK	20
2	BYTES/SECTOR (LOW)	00
3	BYTES/SECTOR (HIGH)	02
4	GAP1	14
5	GAP2	1E
6	GRP/CE/INTERLEAVE	C1
7	RETRY COUNT	03
8	ECC ENABLE (0 OR 1)	01
9	RESEEK ENABLE (0 OR 1)	00
10	MOVE BAD DATA ENABLE (0 OR 1)	00
11	INCREMENT BY HEAD (0 OR 1)	01
12	DUAL PORT DRIVE (0 OR 1)	00
13	STATUS CHANGE INT. (0 OR 1)	00
14	SPIRAL SKEW FACTOR	10
15	GROUP SIZE (SECTORS)	10
16	RESERVED	00
17	RESERVED	00
18	RESERVED	00

DRIVE MODEL: FUJITSU 2312K
84 MByte

SET DRIVE SWITCHES
S2=11111111
S3=00100000

CONFIGURATION: 512 Byte Sectors (32 Sectors/Track)
Cache Mode On
16 Sector Cache Groups
Error Correction On
Increment By Head On

As a free service Interphase will provide a UIB per your configuration
Call the Applications Engineering Department:
(214)350-9000

In the U.K., please call:
(0296) 435661

Table 3 - UIB PARAMETER TABLE
(Values are in Decimal Notation)

DRIVE TYPE & MODEL	SECTORS/TRACK 256	512	1024	GAP SIZE 256/512/1024 G1	G2	BUFFERED MODE INTERLEAVE 256	512	1024	DISK DRIVE NOTES
AMPEX									
DM940, DM980	64	32	16	18/20/20	20/30/30	3	2	2	1
9160, 9300	64	32	16	18/20/20	20/30/30	3	2	2	1
DFR SERIES	64	32	16	18/20/20	20/30/30	3	2	2	1
9100, 9200	44	22	12	18/20/20	20/30/30	3	2	2	1
CAPRICORN	64	32	16	18/20/20	20/30/30	3	2	2	1
CDC									
9400, 9700	64	32	16	18/20/20	20/30/30	3	2	2	1,2
LARK 9455	64	32	XX	18/20/20	20/30/30	3	2	X	1,3
LARK 9457	XX	32	XX	18/20/20	20/30/30	X	2	X	1,3
CDC FSD	64	32	16	18/20/20	20/30/30	3	2	2	1
CDC 9771XMD	160	80	40	18/20/20	20/30/30	4	3	3	
CENTURY DATA									
T80, T3000	64	32	16	18/20/20	20/30/30	3	2	2	1
T20, T25,T50	44	22	12	18/20/20	20/30/30	3	2	2	1
M20,M40,M80	64	32	16	18/20/20	20/30/30	3	2	2	1
AMS190	75	40	20	18/20/20	20/30/30	3	2	2	1
M160, AMS380	80	50	25	18/20/20	20/30/30	3	2	2	1
C2075, C8048	64	32	XX	18/20/20	20/30/30	3	2	X	1
DISK TEK ONE									
ALL MODELS	64	32	16	18/20/20	20/30/30	3	2	2	1
FUJITSU									
2311, 2312	64	32	16	18/20/20	20/30/30	3	2	2	1,5
M2284	64	32	16	18/20/20	20/30/30	3	2	2	1
M2351/EAGLE	80	44	24	18/20/20	20/30/30	4	3	3	4
KENNEDY/BASF									
6170	32	22	11	18/20/20	20/30/30	3	2	2	1
MICROPOLIS									
1400 SERIES	64	32	16	18/20/20	20/30/30	3	2	2	1
NEC CORP.									
D2200 SERIES	64	32	16	18/20/20	20/30/30	3	2	2	1

Table 3 - UIB Parameter Table (cont.)
(Values are In Decimal Notation)

DRIVE TYPE & MODEL	SECTORS/TRACK 256	512	1024	GAP SIZE 256/512/1024 G1	G2	BUFFERED MODE INTERLEAVE 256	512	1024	DISK DRIVE NOTES
PRIAM									
3350, 6650	64	32	16	18/20/20	20/30/30	3	2	2	1
3450, 7050	32	21	12	18/20/20	20/30/30	3	2	2	1
15450, 803	64	32	16	18/20/20	20/30/30	3	2	2	1
SLI									
CHEYENNE	32	22	11	18/20/20	20/30/30	3	2	2	1
TECSTOR									
	64	32	16	18/20/20	20/30/30	3	2	2	1

SMD 2190 DISK DRIVE INTERFACING NOTES

NOTE 1:
For information on 2048 byte sectors and larger please contact Interphase Corporation.

NOTE 2:
Certain CDC 9400 series drives cannot run with 1024 byte sectors. This is a drive limitation not a controller limitation. Please contact the Interphase Application Engineering Dept. for assistance in using 1024 sector sizes for these drives.

NOTE 3:
This drive has embedded servo and has only two fixed sector size options, 32 or 64 sectors per track. Special note for CDC 9457: due to the design of the index pulse spacing, the SMD 2190 cannot run 256 sector sizes on the CDC 9457 (Lark II).

NOTE 4:
Early manuals on the EAGLE drives have errors in the tables that show the switch setting vs. sector per track. The switch settings should be verified using the formula given in the disk drive manual.

NOTE 5:
Drive switch settings for the Fujitsu 2312 and 2311 for 2048 sector sizes are:

S-2	S-3
1 2 3 4 5 6 7	1 2 3 4 5 6 7
C C 0 C 0 C C	0 0 0 0 C 0 0

FOR ASSISTANCE IN USING THE SMD 2190
PLEASE CALL THE
INTERPHASE APPLICATIONS ENGINEERING DEPARTMENT

(214) 350-9000

IN THE U.K., PLEASE CALL (0296) 435661

SECTION 6

FORMATTING

INTRODUCTION

Before data can be written to or read from any disk, that disk must be formatted. That means that all the "header" information for each sector on a track is recorded along with a dummy data field which can later be overwritten and read. The header tells the SMD 2190 where the Read/Write head is positioned and the SMD 2190 first verifies that it is where it thinks it is before writing or reading.

A disk drive unit is typically made up of a number of disk platters with two sides (surfaces) each. Each surface contains a number of concentric tracks each of which is broken into a number of sectors. The term cylinder refers to the three-dimensional visualization of the same track (radially coincident) on a stack of platters and is sometimes used interchangeably with the term track. A track, however, is really specified by a combination cylinder number and head number.

The SMD 2190 automatically formats one track of a disk when it receives the FORMAT command. To format an entire unit the user should write a simple iterative program loop with each iteration specifying a different cylinder/head (in the IOPB) until all tracks have been formatted. The Initialize process must, of course, precede the Format operation since certain parameters of formatting are defined at that point.

Each sector on a track contains a software selectable (via Initialize) size, or number of bytes for the data field. The data field can vary from two to 3,512 bytes long when operating in the Buffered Mode with the normal buffer size and up to 7608 with the optional extended buffer. The sector size can be even larger in the Direct Mode. The data byte replicated in the data field is specified in byte 15 of the IOPB. This byte is referred to as the data fill character.

INTERLEAVE FACTOR AND ITS EFFECTS

The sectors are numbered from zero to N on a track, but are not necessarily numbered physically sequentially. A term called "Interleave Factor" controls the number sequence. On a disk with an Interleave of 2, logical sectors one and two are actually one physical sector apart. For an Interleave of 3, logically consecutive sectors are physically two sectors apart. For an Interleave of 1, logically consecutive sectors are also physically consecutive. Once formatted, the user need not be concerned with this logical-to-physical mapping since it is automatically handled by the SMD 2190.

BUFFERED MODE

In the Buffered Mode, an entire sector of data is fetched from the disk (on a READ) and verified for accuracy (using the ECC) before sending the data on to system memory across the Multibus. The purpose of Interleaving is to give the SMD 2190 time to send the data across the bus, while having to contend with all the other system facilities for bus bandwidth, in time to access the next logical sector in case the transaction is a multisector transaction. For such multisector transactions it is critical that the controller is ready for the next logical sector when it comes under the Read/Write head, otherwise it is necessary to wait an entire disk revolution to access that sector, with a radical decrease in overall throughput.

CACHE MODE

In the Cache Mode (with the GRP bit = 1), the SMD 2190 formats the disk using a 1 to 1 interleave (Interleave Factor = 1) within the limits of the cache group. If the cache group size is set to be one-half of the track size, then the track is formatted 1 to 1 all the way around the track. The group size can also be set to be other than one-half track, and then the groups can be interleaved individually, if desired, using the Interleave Factor.

GENERAL

The SMD 2190 is capable of approximately two million 8-bit or 16-bit bus transactions per second if it has unrestricted access to the bus, but in most real Multibus systems, no bus master has unrestricted access to the bus. The SMD 2190 is highly programmable so that it can be optimized for maximum system throughput,

which is a function of many factors outside control of the disk controller. It should be understood that no simplistic statement such as "an Interleave of 2 is faster than an Interleave of 3" can be made without regard for overall system configuration, CPU speed, memory speed, acceptable bus latency, interrupt activity, and characteristics of other resident bus masters. What is important is that the system is optimum, not that any one element of the system operates at its maximum.

It should also be understood that your system will work over a wide range of Interleave Factors, and optimization should be done only after the overall system works so that no systematic problems are confused with variations in Interleave. And don't be surprised if overall system performance is not dramatically affected by simply changing the Interleave Factor from three to two, for example. If your Operating System makes access to only one sector at a time and consecutive sectors are commonly needed in succession it is probable that Cache Mode operation will show the greatest average data throughput.

This is also true if consecutive multisector groups are commonly requested in consecutive transactions. An environment that is particularly receptive to Cache Mode is UNIX or UNIX-like operating systems. In many cases, Cache Mode operations under UNIX will considerably outperform the more simplistic 1-to-1 interleave approaches. It uses a 1-to-1 interleave, but adds an intelligent prefetch caching scheme to insure no lost revolutions of the disk.

Refer to the UIB Parameter Table for guidelines in UIB parameters for various configurations and drive types. When you get ready to fine tune your system for optimum performance, feel free to contact Interphase Corporation for further advice if desired.

SPIRAL FORMATTING

Most disk controllers format all disk tracks such that sector zero on track one is directly in line with sector zero on track two. On multisector transactions that overlap track boundaries it is common practice to incur a one disk revolution time penalty because of the inherent delay for head-to-head selection. (The SMD 2190 allows automatic incrementing of head number or cylinder number, by UIB option, on transactions that overlap track boundaries.)

The SMD 2190 uses a feature called "Spiral Formatting" which skews sector 0 on adjacent tracks such that even after the head select time, sector zero of the next track will not have already gone past the head. A UIB parameter called Skew Factor specifies how much skew is to be employed. It is suggested that the increment by head scheme be used so that spiral skewing can be used.

FORMATTING FAULTY MEDIA

It is not uncommon for a disk drive or disk cartridge to have imperfect media. This shows up as bad tracks which have hard errors on them. Sometimes the disk manufacturer provides a list of the bad tracks, and it is assumed that the user will somehow map out the bad tracks to an area reserved for spare tracks and avoid the bad tracks. In addition to bad areas of new disks, it is possible for a track to go bad after some amount of use. One must also avoid these areas.

After Formatting a disk unit, it is good practice to Verify all of the tracks. If a track fails to Verify successfully, you should then use the MAP command to map that track to one of the alternate tracks. To do this, simply build an IOPB with the form of Figure 9 on the following page and execute a GO.

The SMD 2190 will automatically write a repetitive pattern on the old track (the entire track will not be bad, only a section of it) vectoring it to the specified alternate physical track. In addition, the alternate track will be automatically formatted to appear to be the old track. When subsequent accesses to the old logical track are made, the SMD 2190 will go to the old track, read the vector information, and automatically go to the alternate track. Spare tracks may be allocated anywhere on the disk, i.e., any head, any cylinder. Improved average performance may be realized by positioning the spare tracks somewhere close to the middle of the drive so that average seek times to these spares will be low.

0	85	
1	COMMAND OPTIONS	
2	STATUS	
3	ERROR	
4	UNIT SELECT	
5	CURRENT HEAD SELECT	
6 7	CURRENT CYLINDER SELECT	MSB LSB
8	00	
9	TARGET HEAD SELECT	
10 11	TARGET CYLINDER SELECT	MSB LSB
12	00	
13 14 15	00 00 00	
16 17	I/O ADDRESS	LSB MSB
18 19 20	00 00 00	
21 22 23	LINKED IOPB ADDRESS	XMB MSB LSB

FIGURE 8: SMD 2190 ALTERNATE TRACK FORMAT

SECTION 7

OPTION SWITCHES AND STRAPS

INTRODUCTION

The SMD 2190 can operate in a wide variety of modes and system environments. Many of those are configurable under software control, primarily by the UIB. Other factors are typically defined by the nature of the system and are not dynamic. They are selected by a number of on-board straps and by two DIP switches (S1 and S2), each with 10 switches that can be either ON (Closed) or OFF (Open).

SWITCHES

The two switches are shown in Figure 9 and select the I/O port addresses of the GO Register (R0). S1 is the Least Significant byte of the I/O address. If 16-bit addressing is used, poles 3-10 of S2 select the Most Significant byte of the I/O address. If 8-bit addressing is selected, those poles are ignored. Four switch poles (two poles on each switch) are reserved for future use.

The I/O address of R1, R2, and R3 (the IOPB pointer) is always that of R0 plus 1, 2, and 3 respectively. The two least significant bits of the I/O address of R0 are always 00.

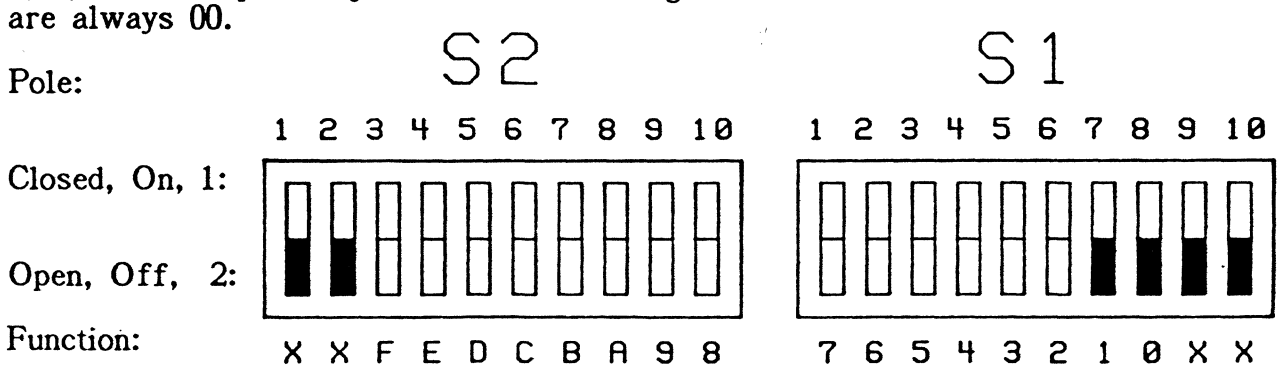

Figure 9. Switch Settings

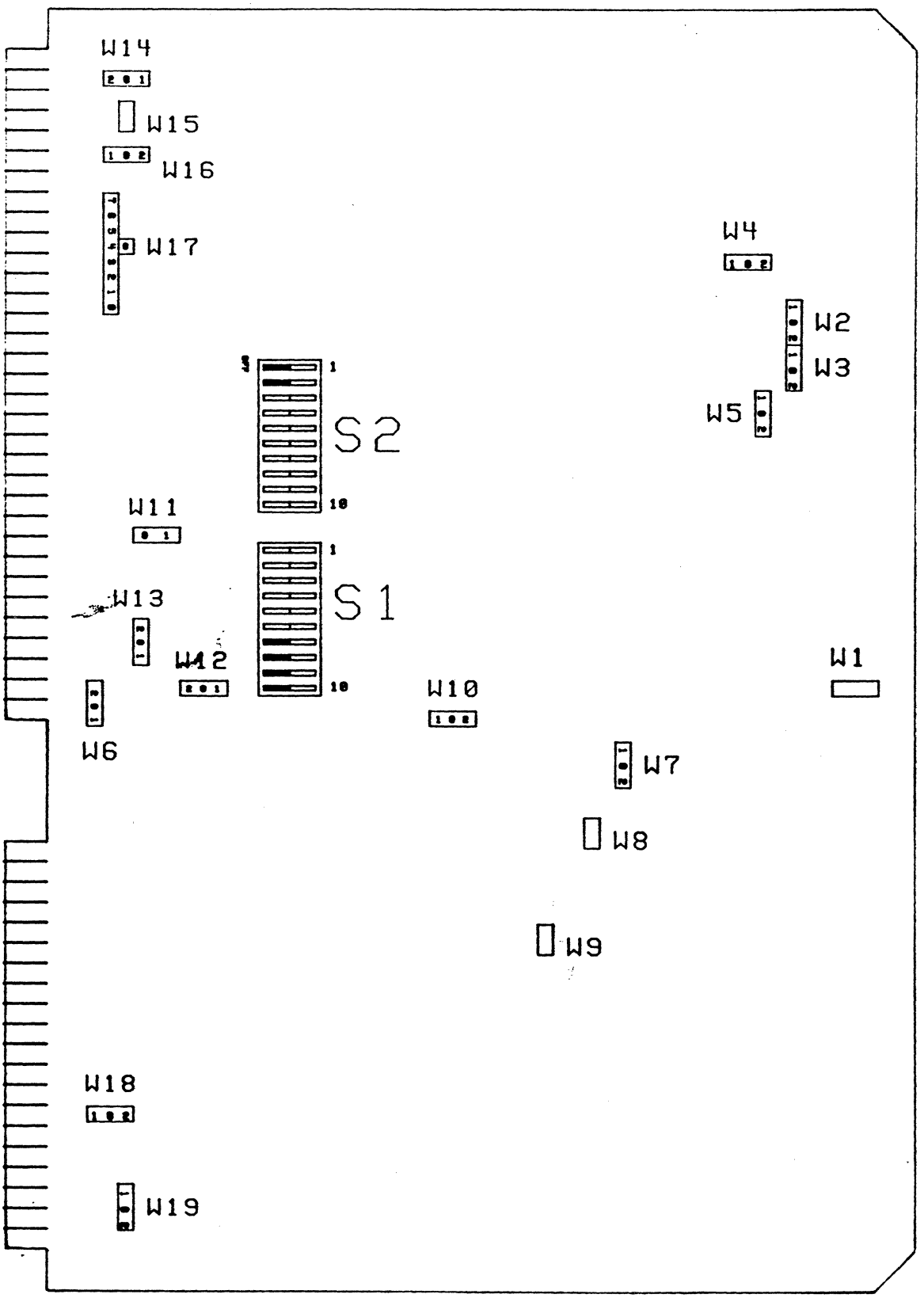

Figure 10. Jumper and Switch Positions

OPTION STRAPS

There are 19 straps on the SMD 2190 labeled W1 through W19. Most have a common node (PAD "C") which must be connected to one of the choices (PAD "1", etc.). A few strap options are selected by their connection, or lack thereof, and have pads labeled "1" and "2." Some options that are very seldom different from one application to another have been connected in etch on the board to reduce the number of unnecessary option plugs. If one of these options requires a change, the etch has been made very accessible and can be easily cut. A few options are not self-explanatory and are discussed below.

W1 - CBRQ ENABLE

With W1 connected, the SMD 2190 does not monitor the Common Bus Request Line. With no connection, the SMD 2190 can both monitor and assert the CBRQ line exactly as specified in IEEE 796.

W2 and W3 - UNIT GROUP SELECTION

The ANSI SMD specification allows up to 16 units to be selected. The unit number is generally set on the disk drive by a switch or strap selection. The SMD 2190 can control up to four disk units, W2 and W3 select which group of four drives can be controlled.

W4 and W5 - SECTOR DETECT

The SMD 2190 can operate on disk drives using either sector pulses (hard sectoring) or drives using Address Marks as the effective sector pulse (soft sectoring); however, current firmware only supports the sector pulse option.

W6 and W18 - -5 VOLT SOURCE

The SMD 2190 requires a -5 volt supply in order to be SMD compatible. This can be accomplished in a variety of ways. If your system supplies at least .6 amps of -5 through P1-9 and 10, connect W18 as C-1. If not, connect W18 as C-2, then the on-board -5 volt regulator can generate -5 from either the -12 volt supply on P1-79 and 80 (connect W6 as C-2) or from a -10 volt supply on P1-77 and 78 (connect W6 as C-2).

W14 - BPRO (BUS PRIORITY OUT)

In a serial bus priority scheme, the Multibus signal BPRO/ is defined by the Multibus specification to be active low. Unfortunately, some CPUs, even those made by Intel, violate the usage of this signal with respect to connecting it to the BPRN/. To use the SMD 2190 with an SBC 80/10, SBC 80/11, or SBC 80/14 the normally supplied signal must be inverted (connect W14 as C-2). Most other CPUs require W14 to be connected as C-1.

Application Note #3 further elaborates on use of the SMD 2190 with SBC 80/10 type CPUs.

When using a parallel bus resolution scheme, the BPRO/ must be disconnected altogether, neither C to 1 or C to 2. If left connected, it may cause unusual problems with some backplanes.

W15 - BCLK/

The SMD 2190, and all other Bus Masters, requires a synchronizing clock called BCLK/. The SMD 2190 can either supply BCLK/ (connect W15) or run off an otherwise supplied BCLK. (Do not connect W15.) It is not recommended that the SMD 2190 supply BCLK due to the fact that it runs at 12 MHz instead of the standard 10 MHz. See Application Note #4 for a warning regarding BCLK/.

W16 - BPRN/ (BUS PRIORITY IN)

The BPRN/ option allows for various Bus Master Priority arrangements, including both serial and parallel bus priority resolution schemes. When using the serial scheme, the backplane should be strapped as shown below. Intel warns that no more than three (3) Bus Masters be daisy-chained in the serial approach (based on use of the SBC 86/12 CPU).

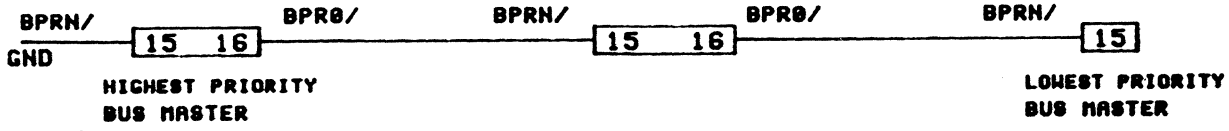

Figure 11. Backplane Straps for Serial Connection

OPTION STRAPS

There are 19 straps on the SMD 2190 labeled W1 through W19. Most have a common node (PAD "C") which must be connected to one of the choices (PAD "1", etc.). A few strap options are selected by their connection, or lack thereof, and have pads labeled "1" and "2." Some options that are very seldom different from one application to another have been connected in etch on the board to reduce the number of unnecessary option plugs. If one of these options requires a change, the etch has been made very accessible and can be easily cut. A few options are not self-explanatory and are discussed below.

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When using a parallel bus resolution scheme, the BPRO/ must be disconnected altogether, neither C to 1 or C to 2. If left connected, it may cause unusual problems with some backplanes.

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The SMD 2190, and all other Bus Masters, requires a synchronizing clock called BCLK/. The SMD 2190 can either supply BCLK/ (connect W15) or run off an otherwise supplied BCLK. (Do not connect W15.) It is not recommended that the SMD 2190 supply BCLK due to the fact that it runs at 12 MHz instead of the standard 10 MHz. See Application Note #4 for a warning regarding BCLK/.

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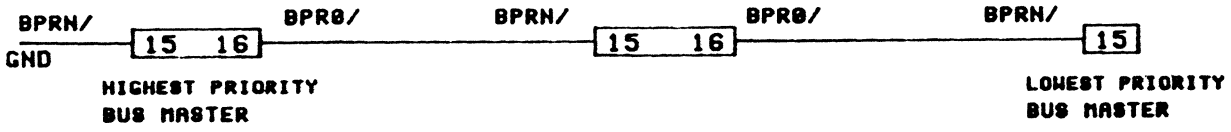

Figure 11. Backplane Straps for Serial Connection

When using external parallel Bus priority resolution, any number of Masters can be employed. The SMD 2190 provides all bus signals necessary for use in such a scheme, and is used exactly like any other bus master.

If a parallel priority system is used or if the disk is not the highest priority in a serial system connect W16 as C-1. If the disk is the highest priority in a serial bus priority system connect W16 as C-2.

W17 - INTERRUPT LEVEL

The SMD 2190 can generate interrupts on any one (or none) of the eight bus interrupt lines. W17 selects which one.

W19 - OPCDET (OPEN CABLE DETECT)

The controller normally supplies a voltage to the disk drive which is used by the Open Cable Detect circuitry of the drive to signify that the "A" cable is disconnected or that the controller has lost power. If controller power is lost, this voltage causes the controller commands to the drive to terminate. This protection has been extended to permit a voltage from a Multibus device to also cause the controller top issue this signal. For example, loss of CPU power.

Multibus pin 52 of P2 is the input to the controller for this feature. Jumper W19 on the controller board will implement the function when installed in the C2 position. In the C1 position, the feature is disabled.

OTHER STRAPS

All other Straps are factory configured straps and should not be changed for normal operation. If information concerning these straps is desired, please contact Interphase.

SECTION 8

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

Power:	+5 VDC = ±5% @3.75 Amps
	-5 VDC = ±5% @ .60 Amps
Or:	-10 VDC
Or:	-12 VDC

PHYSICAL SPECIFICATIONS

Height:	6.75"
Width:	12.00"
Thickness:	.50"
Weight:	14.00 Oz.

CONNECTORS

Bus:	Card Edge, 86 Pins On .156" Center
SMD:	"A" Cable - 60 Pins
	"B" Cable - 26 Pins
Maximum Cable Length:	50 Feet

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature:	32-131 deg F. (0-55 deg. C)
Max. Relative Humidity:	10-90% noncondensing

The -5 volt supply in some systems may not supply sufficient current for SMD drivers and receivers. If the -5 drops below -4.5 V when the SMD disk controlle is installed, the -5 V is not sufficient. In addition, some systems may not supply -5 volt at all. In either case, an on-board regulator can be attached to either -10 volts or -12 volts. Refer to the option straps section for further information.

APPENDIX A

APPENDIX A

COMMANDS

The SMD 2190 automatically completes macro-level commands after it is initiated with the GO bit. The first byte of the IOPB specifies such things as Read data from the disk directly into system memory. The user simply specifies the Disk Unit/Head/Cylinder, the starting sector number, number of sectors, and where to put the data into system memory. The SMD 2190 does any necessary Seeking, handles any error corrections, does the DMA, and interrupts the CPU when done. Commands can also be Linked, or chained together, as described earlier.

All command codes are listed in hexadecimal format.

81 **READ:** Read one or more logically sequential disk sectors from the specifed (starting) location on the specified disk unit and put the data into system memory starting at the Buffer Address (or the effective address if relative addressing is used). The data first goes into the on-board sector buffer, is checked for errors using the ECC code and is corrected, if necessary, while still in the buffer. The data is then put directly into system memory by the SMD 2190 which becomes a Bus Master. It acquires the bus and transfers up to the DMA COUNT (IOPB) of bytes or words of data before releasing the bus. Multiple bus acquisitions are generally required. Upon completion, the SMD 2190 updates the Status and Error bytes of the IOPB and interrupts the CPU.

82 **WRITE:** Write the specifed data stored in Multibus memory into one or more logically sequential disk sectors. The direct inverse of the READ command. A 32-bit Error Correction Code (ECC) is automatically appended to the sector so that errors can be detected and corrected upon subsequent READ operations. Up to 65535 sectors can be Written and Read. When track boundaries are overlapped, the SMD 2190 automatically seeks to the next cylinder or selects the next head based on initialization parameters.

83 **VERIFY:** One or more logically sequential sectors of previously written data can be verified for lack of ECC errors, by reading them from the disk but not transferring the data to the bus.

84 **FORMAT TRACK:** Before any disk surface may be used to Read or Write a sector of data, the surface must be formatted. The formatting operation stores record header information to allow verification of head position before a Read or Write to the disk. This instruction automatically formats a single track, according to initialization parameters. During the format operation, a physical-to-logical sector number translation is performed based on the Interleave Factor, Group Enable, and Spiral Skew.

To format a surface of a disk platter, one must write a simple iterative program loop, which increments the cylinder select byte of the IOPB and issues a Format Command. Maximum cylinder number varies from drive to drive.

85 **MAP:** The MAP command allows the user to map a bad track on any surface to a specifiable spare track on any surface. It can be invoked by the user upon detection of the failure to properly format a track during the formatting or verify cycle. When the MAP command is invoked, a special IOPB must be built to specify the track that is bad and the spare track that is to be substituted for it. The special IOPB specifes the current track and the target track.

0	85
1	COMMAND OPTIONS
2	STATUS
3	ERROR
4	UNIT SELECT
5	CURRENT HEAD SELECT
6 7	CURRENT CYLINDER SELECT MSB LSB
8	00
9	TARGET HEAD SELECT
10 11	TARGET CYLINDER SELECT MSB LSB
12	00
13	00
14	00
15	00
16 17	I/O ADDRESS MSB LSB
18	00
19	00
20	00
21 22 23	LINKED IOPB ADDRESS XMB MSB LSB

NOTE: CURRENT REFERS TO BAD TRACK
TARGET REFERS TO SPARE TRACK

The SMD 2190 upon detection of this command, will first format the bad track with a special format that indicates that it is a bad track. It also specifies which track is to be substituted for the bad track. Then the controller will seek to the target track and format it to be the logical replacement of the bad track. All of the appropriate seeks to perform this operation are implied and are handled by the SMD 2190.

In subsequent normal operation, whenever the logical track that was referenced as bad, the controller will first seek to the bad track, will discover by reading of the special header that it was bad and then will perform another seek to the track that was substituted for the bad one. All of this is totaly transparent to the user, except for the additional seek times required to perform the operation.

86 **REPORT CONFIGURATION:** This command reads certain information stored in the PROM and reports it to the user by writing it into the IOPB. The information includes the controller type and firmware revision level. After successfully receiving an 86H command, the SMD 2190 will respond with the following bytes in the IOPB:

IOPB BYTE		CONTENTS
2 (STATUS)	=	80H (Normal completion)
3 (ERROR)	=	First two digits of firmware revision level in BCD format
4 (UNIT)	=	Pre-release extension in ASCII or a 0 if official production release.
5 (HEAD)	=	39, product code for SMD2190

If unsuccessful, normal error reporting is generated. If the 86H command is issued to a SMD 2181 (as opposed to the SMD 2190) only bytes 2 and 3 are reported and bytes 4-5 remain unchanged from those set up when issuing the command.

87 **INITIALIZE:** Upon power-up, the SMD 2190 must be initialized with a number of parameters that identify the type of disk drive attached to it, the preferred interleave factor for formatting, and a number of operating options. Since any mix of disk drive types can be attached to the four ports, each disk unit must be initialized individually before use. The INITIALIZE Command can also be invoked at any time to change operating characteristics.

89 **RESTORE:** This command causes the selected disk drive unit to seek to cylinder zero and clear a fault by issuing a Restore or Recalibrate command and Clear Fault to the unit. This command takes up to several seconds on some SMD disk drives and is generally seldom used except on power-up and to clear disk drive faults.

8A **SEEK:** The selected disk unit is commanded to move its read/write head to the specified cylinder and select the specified head. Since most commands have automatically implied seeks it is not necessary to use this command at all unless you use overlapped seeks.

The SEEK command generates a Command Complete Interrupt as soon as the seek is started by the disk drive, so that another command can be started on another unit while the head on the first unit is in motion. If so initialized, the SMD 2190 will also generate a Disk Status Change Interrupt when the first unit completes its seek.

8F **RESET:** This command reports completion status in the IOPB. It is often used after power-up in order to verify that the SMD 2190 exists and can obtain access to the bus. Use of the command is entirely optional. After RESET the SMD 2190 must be Initialized, whether or not on power-up. Asserting INIT/ on the Multibus or issuing a hardware reset with bit 7 of the Command Register also causes a RESET; therefore, the host CPU should do an Initialize for each drive connected after every RESET.

91 **DIRECT READ:** Does the same thing as READ except in the Direct Mode (see Direct Mode section). The on-board buffer is not used. Error correction works but runs slower since it must manipulate system memory instead of the faster sector buffer memory. Certain systematic limitations apply in the Direct Mode which should be understood before using this command. Refer to the Direct Mode Usage section. This command is normally used only where the disk is formatted with consecutive physical sectors and the transaction is a multiple sector command unless the sector size is too large for the physical buffer.

90 **READ RAW DATA:** This command is implemented for those who wish to Read (without error correction and detection) the data that immediately follows an index pulse. This data may be a manufactures media defect list or simply a sector including header information for diagnostic purposes. The following information is provided as an aid in using this command:

1. The command causes the number of bytes specified in the Bytes/Sector (Bytes 2 and 3) portion of the UIB to be Read (uncorrected) beginning at the index pulse. The sector count contained in the IOPB is ignored.

2. The data is Read in LSB-MSB order, and any translation that is required, must be performed by the host.

3. If the first bit read is not a logical '1', a bit shift on the data field will be necessary.

92 **DIRECT WRITE:** Inverse of the DIRECT READ with the same restrictions.

93 **READ ABSOLUTE:** This read command functions the same as an ordinary read (81H) except that if an error is detected in the data field, no retries or error recovery mechanisms are employed. Functionally, this command is equivalent to having the Move Bad Data bit set in the UIB when the drive was initialized. This command allows absolute reading of data on a per IOPB basis which may be useful in certain applications where occasional bit errors can be tolerated more easily than delays in data caused by retries or error correction.

94 **READ NONCACHED:** This command is the same as a READ (81H) except that if the cache is enabled, via the UIB, it reads only the sector(s) of interest and defeats automatic caching. This allows for a more efficient transaction if it is known that no later reference to trailing sector(s) will be made.

APPENDIX B

APPENDIX B - ERROR CODES

NOTE: ALL CODES ARE HEXADECIMAL.

10 DISK NOT READY

The disk's ready signal output is tested at the beginning of any command requiring a head movement, i.e., all commands except Reset. Error "10" is posted if the disk is not ready. Note that error "1B" is issued if the drive is not powered up.

11 INVALID DISK ADDRESS

The unit selects bits in the IOPB and are examined for the presence of a valid unit selection (0-3). Checked on all commands except Reset.

12 SEEK ERROR

If the 2190 cannot find the sector of interest in two revolutions, it tries to verify that it is on the right track by reading several sectors. If either the Head number or Cylinder number in the Header is incorect, then error 12 is issued. If the Head number and Cylinder number are correct, error 29 is issued.

13 ECC CODE ERROR-DATA FIELD

The computed ECC code on the data did not agree with the ECC code appended to the data on the disk, and no error correction was attempted. (NOTE: See also Error 23.)

14 INVALID COMMAND CODE

The command code, byte 0 in the IOPB was not valid.

15 NOT USED

16 INVALID SECTOR IN COMMAND

The target sector in the IOPB, byte 8 and 9 in the IOPB, was greater than the capacity of the drive as specified in byte 1 of that drive's UIB. This check is performed after the Seek has been done.

17 NOT USED

18 BUS TIMEOUT

Bus acquisition was not made within three milliseconds of a request, or XACK was not received within three milliseconds of a MRDC/, MWTC/ or IOWTC/.

19 NOT USED

1A DISK WRITE PROTECTED

Posted when attempts are made to write to a disk that is write protected.

1B UNIT NOT SELECTED

A unit select was made and the unit failed to respond with "Unit Selected." This error is returned when the drive unit number is misselected, the drive is not powered up, or the cable is not connected.

1C NO ADDRESS MARK - HEADER FIELD

This error is posted if no sync information is found in the header of the target sector. Error correction will not be attempted on the header field.

1D NOT USED

1E DRIVE FAULTED

A Fault condition exists in a selected unit. The Fault should be cleared by a Restore Command.

1F NOT USED

20 NOT USED

21 NOT USED

22 NOT USED

23 UNCORRECTABLE ERROR

Error correction was attempted on the data field and the error was found to be uncorrectable.

24 NOT USED

25 NOT USED

26 NO SECTOR PULSE

The sector pulse is missing from a selected unit.

27 DATA OVERRUN

A data field timeout error generally caused by missing TX or RX clock.

28 NO INDEX PULSE ON WRITE FORMAT

During a Write Format operation the SMD 2190 looks for the index pulse from the disk. If not found within 65 milliseconds, the error is posted. No retries.

29 SECTOR NOT FOUND

If at any point during a Read- or Write-type operation the target sector cannot be found, this error is posted. This error will also be posted if an attempt is made to directly access a target sector which lies within one of the spare tracks which had been previously mapped.

2A ID FIELD ERROR-WRONG HEAD

The head number read from the disk in the header field was wrong.

2B INVALID SYNC IN DATA FIELD

The first byte read from the data field was not a valid sync character.

2D SEEK TIMEOUT

A seek was made and a normal complete response did not occur within 500 milliseconds.

2E BUSY TIMEOUT

On a dual ported drive, BUSY has been active for more than 500 milliseconds.

2F NOT ON CYLINDER

The drive must be "on cylinder" within three seconds of being selected.

30 RTZ TIMEOUT

A Restore command was executed and a normal completion did not occur within three seconds.

31 WRITE UNDERRUN

There was a data underrun condition during a direct write. The write should be performed again.

40 UNIT NOT INITIALIZED

A command was attempted on a unit that has not been initialized.

42 GAP SPECIFICATION

The value for either GAP1 or GAP2 in the UIB is too small.

4B SEEK ERROR

A seek error was reported by the disk drive.

4C MAPPED HEADER ERROR

No sector pulse found on track to be mapped.

50 SECTOR PER TRACK

The sector/track in the UIB is set to zero.

51 BYTES/SECTOR

The bytes/sector in the UIB, bytes 2 and 3, exceed the capacity of the buffer.

52 INTERLEAVE FACTOR

The interleave factor in the UIB, byte 6, is either zero or greater than the number of sectors per track.

53 INVALID HEAD ADDRESS

The target head in the IOPB, byte 5, was greater than the capacity of the drive as specified in byte 1 of that drive's UIB.

5D INVALID DMA BURST COUNT

The specified DMA burst count causes the controller to attempt to transfer an odd number of bytes.

5F INVALID GROUP SIZE

This code indicates that an invalid value for group size has been placed in byte 15 of the UIB. The total number of bytes int he group must not exceed the capacity of the buffer which is 4K for normal buffer and 12K for the extended buffer. An error will be posted if an Initialize command is attempted when this condition exists and if the GRP bit of Byte 6 in the UIB is set to '1'. Also, if the group size is set to zero and caching is enabled, a 5F will be reported.

APPENDIX C

APPENDIX C

SMD 2190 AUXILIARY PORT

INTRODUCTION

The SMD 2190 Auxiliary Port is a parallel port that supports high-speed bidirictional data transfers between the SMD 2190 and a system memory board. DMA transfers, controlled by the SMD 2190, are initiated by an auxiliary port READ or WRITE command from the host CPU. Data is transferred 16 bits at a time (word wide), which allows a maximum data rate of four megabytes per second.

One of the control lines on the auxiliary port can be used by the SMD 2190 to load a 24-bit address (found in the IOPB for the current command) into an address register on the memory board. This increases flexibility of the port and allows error correction in Direct Mode (if required).

SIGNAL DESCRIPTION

Note: Signal Type - OUT - Output from SMD 2190
IN - Input to SMD 2190
BI - Bidirectional

Pin Number	Signal	Type	Description
1-8	ADBL0-ADBL7	BI	Least significant 8 bits of data
17-24	ADBH0-ADBH7	BI	Most significant 8 bits of data
13	IOPBEN		IOPB Enable
10	AUXCLK	OUT	12 MHz system clock
15	ADDRLD	OUT	Address Load Enable - Active High: When active, this signal indicates that 3 bytes of address are to be loaded into address registers on the memory board. ADDRLD must be inactive during data transfers.

Pin Number	Signal	Type	Description
9	XVRRD	OUT	Transceiver Read -Active low: When active, this signal indicates that the direction of data transfer is from the memory board and to the SMD 2190. XVRRD could be used as a direction control for bidirectional buffers on the memory board data bus.
12	AUXACK	IN	Auxiliary Transfer Acknowledge - Active low: When active, this signal indicates to the SMD 2190 that the Read/Write operation has been completed on the memory board.
16	MWTC	OUT	Memory Write Command - Active high: When active, this signal indicates that valid data has been placed on the Auxiliary Port data bus by the SMD 2190. MWTC specifies that the data is to be written into the currently addressed memory location on the memory board.
11	MRDC	OUT	Memory Read Command - Active high: When active, this signal indicates that the contents of the currently addressed memory location on the memory board are to be placed on the Auxiliary Port data bus and read by the SMD 2190.

THEORY OF OPERATION

The host CPU initiates an Auxiliary Port transaction by setting bits one and two in the command options byte of the IOPB for the current READ or WRITE command. The SMD 2190 then activates signals ADDRLD and AUXSLT and loads a three-byte (24-bit) address into the address registers that reside on the system memory board.

This three-byte value is passed in three word-wide transfers under DMA control and points to the beginning of the system memory data buffer. Since the minimum DMA count is three due to SMD 2190 hardware restrictions, three transfers are required. The order of address words written is as follows:

	Upper Byte	Lower Byte
Word 1	Don't Care	Don't Care
Word 2	XMB	Don't Care
Word 3	LSB	MSB

Note: This 24-bit address is low true.

Once the address registers have been initialized (and signal ADDRLD is deactivated), data transfer (disk-to-memory or memory-to-disk) may be accomplished in the exact same way as between the SMD 2190 and Multibus, including status and error reporting upon command completion. Buffer Mode, Cache Mode, and Direct Mode are all supported as well as error correction.

NOTES

APPLICATION NOTES

From time to time Interphase is made aware of isolated or common systematic problems and confusing phenomena. This section attempts to make you aware of these factors and will ocasionally be updated.

APPLICATION NOTE 1

20- AND 24-BIT ADDRESS: Some Multibus backplanes do not include the necessary 2.2K pull up resistors ADDR 10-13 (HEX) or ADDR 10-17, the upper bits of a 20-bit or a 24-bit address. Attempting to use 20-bit or 24-bit addressing can cause strange problems on these units. To insure these lines are pulled up, remove all cards in system and THEN check backplane pins on these lines for +5V.

APPLICATION NOTE 2

IN-CIRCUIT EMULATION: The SMD 2190 will work under in-circuit emulation. One must, however, be aware of certain peculiarities of ICE 80, ICE 85, ICE 86 and others when used with a CPU in a target system which includes any other Bus Master, including the SMD 2190. While it is emulating, the ICE presents a true representation of a processor to the target system. While it is not emulating, however, the representation may not be valid, and since the processor commonly controls the bus indirectly via HLDA and other signals, the Bus may lock up. As a result, the ICE in some cases cannot be single-stepped or break-pointed while the SMD 2190 (or any other Bus Master) is in the middle of an operation on the BUS, i.e., after issuing a GO command, but before sensing completion.

APPLICATION NOTE 3

USE OF SBC 80/10 CPU: The SMD 2190 will operate with all Multibus CPUs. Some peculiarities of CPUs, however, restrict the system configuration. The SBC 80/10, 80/11, 80/12, and 80/14 all require the polarity of BPRO/ to be switched to BPRO in a serial priority system.

This is accommodated on the SMD 2190 by strap W14. In addition, if a SBC 80/10 is used in a Serial Priority System, it MUST be the lowest priority and the SMD 2190 must be the next highest priority. Only two masters should be used in that case.

Also see Application Note: 4.

APPLICATION NOTE 4

BCLK/WARNING: Some Intel supplied card cage/backplanes use pull-up/pull-down terminating resistors on both BCLK/ and CCLK/ (Multibus pins 13 and 31 respectively). Intel's SBC 80/10 CU cannot drive these signals since the default strap (as it comes from the factory) ties both signals, and, therefore, their terminators in parallel. All Bus Masters (including the SMD 2190) require BCLK/ to operate. One must either remove the terminating resistor from one or both signals OR remove the strap tying the signals together on the board. The latter suggestion is the easiest, but will not work if anything requires CCLK/. Interphase suggests removing both sets of terminators unless the bus is expanded beyond eight card slots. The problem is less serious for SBC 80/20, SBC 80/30 and SBC 86/12, since a heavier driver is used on these boards, although a heavily loaded system may still overload the signal.

APPLICATION NOTE 5

WORD-WIDE IOPB & UIB: Users of 16-bit CPUs may find the following figures useful. The IOPB and UIB formts are shown on a word basis for both LSByte first machines and MSByte first machines.

IOPB, LSB FIRST MACHINES (INTEL CPU):

WORD	ODD BYTE	EVEN BYTE
0	COMMAND OPTIONS	COMMAND
2	ERROR	STATUS
4	HEAD SELECT	UNIT SELECT
6	CYLINDER SELECT (LSB)	CYLINDER SELECT (MSB)
8	STARTING SECTOR (LSB)	STARTING SECTOR (MSB)
10	SECTOR COUNT (LSB)	SECTOR COUNT (MSB)
12	BUFFER ADDRESS (XMB)	DMA COUNT +
14	BUFFER ADDRESS (LSB)	BUFFER ADDRESS (MSB)
16	I/O ADDRESS (LSB)	I/O ADDRESS (MSB)
18	RELATIVE ADDRESS (LSB)	RELATIVE ADDRESS (MSB)
20	LINKED IOPB ADDR (XMB)	RESERVED
22	LINKED IOPB ADDR (LSB)	LINKD IOPB ADDR (MSB)

UIB, LSB FIRST MACHINES (INTEL CPU):

WORD	ODD BYTE	EVEN BYTE
0	SECTORS/TRACK	NUMBER OF HEADS
2	BYTES/SECTOR (MSB)	BYTES/SECTOR (LSB)
4	BYTES IN GAP 2	BYTES IN GAP 1
6	RETRY COUNT	GRP, CE, INTERLEAVE FACTOR
8	RESEEK ENABLE	ERROR CORRECTION ENABLE
10	INCREMENT BY HAD ENABLE	MOVE BAD DATA ENABLE
12	STATUS CHANGE INT.	DUAL PORT DRIVE
14	GROUP SIZE (SECTORS)	SPIRAL SKEW FACTOR
16	RESERVED	RESERVED
18	NOT USED	RESERVED

IOPB, MSB FIRST MACHINES (68000 CPU):

WORD	ODD BYTE	EVEN BYTE
0	COMMAND	COMMAND OPTIONS
2	STATUS	ERROR
4	UNIT SELECT	HEAD SELECT
6	CYLINDER SELECT (MSB)	CYLINDER SELCT (LSB)
8	STARTING SECTOR (MSB)	STARTING SECTOR (LSB)
10	SECTOR COUNT (MSB)	SECTOR COUNT (LSB)
12	DMA COUNT	BUFFER ADDRESS (XMB)
14	BUFFER ADDRESS (MSB)	BUFFER ADDRESS (LSB)
16	I/O ADDRESS (MSB)	I/O ADDRESS (LSB)
18	RELATIVE ADDRESS (MSB)	RELATIVE ADDRESS (LSB)
20	RESERVED	LINKED IOPB ADDR (XMB)
22	LINKED IOPB ADDR (MSB)	LINKED IOPB ADDR (LSB)

UIB, MSB FIRST MACHINES (68000 CPU):

WORD	ODD BYTE	EVEN BYTE
0	NUMBER OF HEADS	SECTORS/TRACK
2	BYTES/SECTOR (LSB)	BYTES/SECTOR (MSB)
4	BYTES IN GAP 1	BYTES IN GAP 2
6	GRP, CE, INT. FACTOR	RETRY COUNT
8	ECC ENABLE	RESEEK ENABLE
10	MOVE BAD DATA ENABLE	INCREMENT BY HEAD ENABLE
12	DUAL PORT DRIVE	INTERRUPT ON STATUS CHANGE
14	SPIRAL SKEW FACTOR	GROUP SIZE (SECTORS)
16	RESERVED	RESERVED
18	RESERVED	NOT USED

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