```
PAL16R4                                 PAL DESIGN SPECIFICATION
PAT000                                  3/4/86
Monochrome Workstation Card vertical sync PAL
Integrated Solutions, Incorporated
CK137 V2 V0 V7 V6 V5 V11 V9 V4 GND /OE
V8 V10 NC /VSYNC /VBLNK /VLAST V1 V3 VCC

VSYNC     =:    V11 *  V10 *  V9 *  V8 *  V7 *  V6
                    * /V5 *  V4 * /V3 * /V2 *  V1 * /V0        ;On at 4050
              + /V5 *  VSYNC                                   ;Hold to 4064
              + /V1 *  VSYNC                                   ;Hold to 4065

VBLNK     =:    V11 *  V10 *  V9 *  V8 *  V7 *  V6
                    * /V5 *  V4 * /V3 * /V2 *  V1 * /V0        ;On at 4050
              +  V10 *  VBLNK                                  ;Hold to 4095

VLAST     =:    V11 *  V10 *  V9 *  V8 *  V7 *  V6
                    * /V5 *  V4 * /V3 * /V2 * /V1 *  V0        ;On at 4049

FUNCTION TABLE

CK137 V11 V10 V9 V8 V7 V6 V5 V4 V3 V2 V1 V0 /VSYNC /VBLNK /VLAST
;                                       /  /  /
;C                                      V  V  V
;K                                      S  B  L
;1  V  V                                Y  L  A
;3  1  1  V  V  V  V  V  V  V  V  V  V  N  N  S
;7  1  0  9  8  7  6  5  4  3  2  1  0  C  K  T
-------------------------------------------------
;Two cycles to reset
 C  X  X  X  X  X  X  H  X  X  X  H  X  H  X  X
 C  X  L  X  X  X  X  X  X  X  X  X  X  H  H  X
;End of frame sequence
 C  H  H  H  H  H  H  L  H  L  L  L  L  H  H  H     ;4048
 C  H  H  H  H  H  H  L  H  L  L  L  H  H  H  L     ;4049
 C  H  H  H  H  H  H  L  H  L  L  H  L  L  L  H     ;4050
 C  H  H  H  H  H  H  L  H  L  L  H  H  L  L  H     ;4051
 C  H  H  H  H  H  H  L  H  L  H  L  L  L  L  H     ;4052
 C  H  H  H  H  H  H  L  H  L  H  L  H  L  L  H     ;4053
 C  H  H  H  H  H  H  L  H  L  H  H  L  L  L  H     ;4054
;Cycles omitted
 C  H  H  H  H  H  H  L  H  H  H  H  L  L  L  H     ;4062
 C  H  H  H  H  H  H  L  H  H  H  H  H  L  L  H     ;4063
 C  H  H  H  H  H  H  H  L  L  L  L  L  L  L  H     ;4064
 C  H  H  H  H  H  H  H  H  L  L  L  H  L  L  H     ;4065
 C  H  H  H  H  H  H  H  H  L  L  L  H  L  H  L  H  ;4066
;Cycles omitted
 C  H  H  H  H  H  H  H  H  H  H  H  L  H  H  L  H  ;4093
 C  H  H  H  H  H  H  H  H  H  H  H  H  L  H  L  H  ;4094
 C  H  H  H  H  H  H  H  H  H  H  H  H  H  H  L  H  ;4095
 C  H  L  H  H  H  H  L  H  L  L  H  L  H  H  H     ;3026
 C  H  L  H  H  H  H  L  H  L  L  H  H  H  H  H     ;3027
-------------------------------------------------
```

DESCRIPTION

This PAL provides the vertical sync and blank signals and a signal which comes on during the last line on the screen.

Vn	The vertical counter Vn cycles from 3026 to 4095 over and over.

cc: CASEY COX
ROB BRIODY
DOUG SWARTZ
KAOEH MOAZAMI
CHRIS HORNE

LOW END MONO GRAPHICS REVIEW
E/NET REVIEW
NEXT ~~FRIDAY~~ MONDAY 7/~~31~~ @ 1:00 P.M.
MAIN CONFERENCE ROOM

```
PAL16L8                                 PAL DESIGN SPECIFICATION
PAT000                                  6/26/86
Monochrome Workstation Card latch output enable PAL
Integrated Solutions, Incorporated
/LWORD A1 /CTLSEL /VSELX /WRITE D8 /SELREG DT /REFRESH GND
/VRESET /OEBAX /OEABL /OEBAL /OEABH /OEBAH RIEN DA18 /RRD VCC

IF (VCC) OEBAX     =  /LWORD * /A1 * /CTLSEL * VSELX *  WRITE

IF (VCC) OEABH     =   LWORD * /A1 * /CTLSEL * VSELX * /WRITE

IF (VCC) OEBAH     =   LWORD * /A1 * /CTLSEL * VSELX *  WRITE

IF (VCC) OEBAL     =  /LWORD *  A1 * /CTLSEL * VSELX *  WRITE
                     +  LWORD * /A1 * /CTLSEL * VSELX *  WRITE

IF (VCC) OEABL     =  /LWORD *  A1 * /CTLSEL * VSELX * /WRITE
                     +  LWORD * /A1 * /CTLSEL * VSELX * /WRITE

IF (VCC) /RIEN     =   VRESET
                     +  LWORD  * /RIEN
                     + /SELREG * /RIEN
                     +  A1     * /RIEN
                     + /D8     * /RIEN
                     + /LWORD  * SELREG * /A1 * /D8

IF (VCC) /DA18     =  /VRESET *  LWORD  * /DA18
                     + /VRESET * /SELREG * /DA18
                     + /VRESET * /A1     * /DA18
                     + /VRESET * /D8     * /DA18
                     + /VRESET * /LWORD  * SELREG *  A1 * /D8

IF (VCC) RRD       =  /WRITE * /DT * /REFRESH

FUNCTION TABLE

/LWORD A1 /CTLSEL /VSELX /WRITE D8 /SELREG DT /REFRESH
/OEBAX /OEABL /OEBAL /OEABH /OEBAH RIEN DA18 /RRD /VRESET
;                          /
;      /           /       R                          /
;/     C  /  /     S       E  /  /  /  /  /           V
;L     T  V  W     E       F  O  O  O  O  O           R
;W     L  S  R     L       R  E  E  E  E  E  R  D  /  E
;O     S  E  I     R       E  B  A  B  A  B  I  A  R  S
;R  A  E  L  T  D  E  D  S  A  B  A  B  A  E  1  R  E
;D  1  L  X  E  8  G  T  H  X  L  L  H  H  N  8  D  T
-----------------------------------------------------
;Write DA18
 H  X  X  X  X  X  H  X  X  X  X  X  X  X  X  H  X  L
 H  H  X  X  X  L  H  X  X  X  X  X  X  X  X  H  X  H
 H  H  X  X  X  L  L  X  X  X  X  X  X  X  X  L  X  H
 H  H  X  X  X  L  H  X  X  X  X  X  X  X  X  L  X  H
 H  H  X  X  X  H  H  X  X  X  X  X  X  X  X  L  X  H
 H  H  X  X  X  H  L  X  X  X  X  X  X  X  X  H  X  H
 H  H  X  X  X  H  H  X  X  X  X  X  X  X  X  H  X  H
;Write RIEN
 H  X  X  X  X  X  H  X  X  X  X  X  X  X  L  X  X  L
 H  L  X  X  X  H  H  X  X  X  X  X  X  X  L  X  X  H
 H  L  X  X  X  H  L  X  X  X  X  X  X  X  H  X  X  H
 H  L  X  X  X  H  H  X  X  X  X  X  X  X  H  X  X  H
 H  L  X  X  X  L  H  X  X  X  X  X  X  X  H  X  X  H
 H  L  X  X  X  L  L  X  X  X  X  X  X  X  L  X  X  H
 H  L  X  X  X  L  H  X  X  X  X  X  X  X  L  X  X  H
;Longword RAM access
 L  L  H  L  H  X  X  X  X  H  L  H  L  H  X  X  X  X
 L  L  H  L  L  X  X  X  X  H  H  L  H  L  X  X  X  X
;Access odd RAM address
 H  H  H  L  H  X  X  X  X  H  L  H  H  H  X  X  X  X
 H  H  H  L  L  X  X  X  X  H  H  L  H  H  X  X  X  X
;Access even RAM address
 H  L  H  L  H  X  X  X  X  H  H  H  H  H  X  X  X  X
 H  L  H  L  L  X  X  X  X  L  H  H  H  H  X  X  X  X
;RAM read
 X  X  X  X  H  X  X  L  H  X  X  X  X  X  X  X  L  X
-----------------------------------------------------
```

DESCRIPTION

This PAL generates output enables for the RAM latches on the Monochrome Workstation Board.

A1, /WRITE /LWORD	These signals are positive true latched copies of the corresponding VME signals.
/VSELX	This signal indicates that the board is being selected from the VME interface.
/CTLSEL	This signal goes active when the UART or register is being accessed. It is generated from the VME address lines.
/SELREG	This is a signal from the arbiter state machine which indicates that the on-board register is being selected.
DT	This signal indicates that a data transfer cycle is taking place.
/REFRESH	This signal indicates that a refresh cycle is taking place.
/OExxx	These signals are the output enables for the RAM latches. Look at the schematic to see how they work.
/RRD	This signal is active during RAM reads.
RIEN	This signal is a set-reset flip-flop which enables retrace interrupts when true. It is bit 8 in CR00;
DA18	This signal is a set-reset flip-flop which selects the memory plane to be displayed. It is bit 8 in CR01.

```
PAL20L8                                 PAL DESIGN SPECIFICATION
PAT000                                  6/20/86
Monochrome Workstation Card interrupt/select PAL
Integrated Solutions, Incorporated
DLDLDS IPENDLT /IACKLT /VIACKIN /VIACK IACK3 IACK2 IACK1 /VJMPH
/SDTACK VA3B GND VA2B VA1B /IACK /XDTACK /IACKEN VIAKOUT VAM5B
VAM4 VAM3 /VSEL /VJMPL VCC

IF (VCC) IACK      =   VIACK * /VA3B * /VA2B *  VA1B
                           * /IACK3 * /IACK2 *  IACK1
                     + VIACK * /VA3B *  VA2B * /VA1B
                           * /IACK3 *  IACK2 * /IACK1
                     + VIACK * /VA3B *  VA2B *  VA1B
                           * /IACK3 *  IACK2 *  IACK1
                     + VIACK *  VA3B * /VA2B * /VA1B
                           *  IACK3 * /IACK2 * /IACK1
                     + VIACK *  VA3B * /VA2B *  VA1B
                           *  IACK3 * /IACK2 *  IACK1
                     + VIACK *  VA3B *  VA2B * /VA1B
                           *  IACK3 *  IACK2 * /IACK1
                     + VIACK *  VA3B *  VA2B *  VA1B
                           *  IACK3 *  IACK2 *  IACK1

IF (VCC) VSEL      =   VJMPL *          VAM5B *  VAM4 *  VAM3 * /VIACK
                     + VJMPL * VJMPH * /VAM5B * /VAM4 *  VAM3 * /VIACK

IF (VCC) XDTACK    =   SDTACK
                     + IACKLT * IPENDLT * VIACKIN * VIACK * DLDLDS

IF (VCC) IACKEN    =   IACKLT * VIACKIN * IPENDLT

IF (VCC) /VIAKOUT  =  /VIACKIN + /DLDLDS + IPENDLT * IACKLT

FUNCTION TABLE

DLDLDS IPENDLT /IACKLT /VIACKIN /VIACK IACK3 IACK2 IACK1 VA3B VA2B
VA1B VIAKOUT /IACKEN /IACK /SDTACK /XDTACK /VJMPH /VJMPL VAM5B VAM4
VAM3 /VSEL
;         /
;   I  /  V                       V  /     /  /
;D  P  I  I  /                    I  I     S  X  /  /                 /
;L  E  A  A  V  I  I  I           A  A  /  D  D  V  V  V        /
;D  N  C  C  I  A  A  A  V  V  V  K  C  I  T  T  J  J  A  V  V  V
;L  D  K  K  A  C  C  C  A  A  A  O  K  A  A  A  M  M  M  A  A  S
;D  L  L  I  C  K  K  K  3  2  1  U  E  C  C  C  P  P  5  M  M  E
;S  T  T  N  K  3  2  1  B  B  B  T  N  K  K  K  H  L  B  4  3  L
-------------------------------------------------------------------
;Pass through interrupt
 H  L  X  L  L  X  X  X  X  X  X  H  H  X  H  H  X  X  X  X  X  X
 H  X  H  L  L  X  X  X  X  X  X  H  H  X  H  H  X  X  X  X  X  X
;Acknowledge interrupt
 L  H  L  L  L  X  X  X  X  X  X  L  L  X  H  H  X  X  X  X  X  X
 H  H  L  L  L  X  X  X  X  X  X  L  L  X  H  L  X  X  X  X  X  X
;Recognize jumpered interrupt level
 X  X  X  X  L  L  L  H  L  L  H  X  X  L  X  X  X  X  X  X  X  X
 X  X  X  X  L  L  H  L  L  H  L  X  X  L  X  X  X  X  X  X  X  X
 X  X  X  X  L  L  H  H  L  H  H  X  X  L  X  X  X  X  X  X  X  X
 X  X  X  X  L  H  L  L  H  L  L  X  X  L  X  X  X  X  X  X  X  X
 X  X  X  X  L  H  L  H  H  L  H  X  X  L  X  X  X  X  X  X  X  X
 X  X  X  X  L  H  H  L  H  H  L  X  X  L  X  X  X  X  X  X  X  X
 X  X  X  X  L  H  H  H  H  H  H  X  X  L  X  X  X  X  X  X  X  X
;SDTACK from arbiter state machine
 X  X  X  H  X  X  X  X  X  X  X  L  H  H  L  L  X  X  X  X  X  X
;16-bit select
 X  X  X  X  H  X  X  X  X  X  X  X  X  X  X  X  X  L  H  H  H  L
;32-bit select
 X  X  X  X  H  X  X  X  X  X  X  X  X  X  X  X  X  L  L  L  L  H  L
-------------------------------------------------------------------
```

DESCRIPTION

This PAL handles interrupt acknowledge cycles and board selects.

DLDLAS — This signal is a version of the VME data strobes delayed by about 400 nanoseconds. It is used to generate a DTACK for interrupt acknowledge sequences.

IPENDLT — This signal is used in deciding whether to pass an interrupt acknowledge down the daisy chain or to acknowledge an interrupt. Look at the schematic to see how it works.

/IACKLT — This signal indicates an interrupt acknowledge to the network card's interrupt level is taking place. It changes state 140 nanoseconds or so after the VME data strobe(s).

/VIACKIN, /VIACK — These are connected to the corresponding VME signals.

IACKn — These signals are connected to jumpers which determine the card's interrupt level.

/VJMPH — This signal indicates a decode of the VA24-VA31 values jumpered for the board. It is used in decoding 32-bit addresses.

/SDTACK — This signal is an acknowledge from the arbiter state machine to the VME bus. It occurs during register and UART accesses.

VAnB — These are buffered copies of the corresponding VME address lines.

VAM5B — This is a buffered copy of the VME signal AM5.

VAMn — These pins are connected directly to the corresponding VME signals.

/VJMPL — This signal indicates a decode of the VA23-VA18 and VAM2-VAM3 values jumpered for the board. It is used in decoding 16- and 32-bit addresses.

/IACK — This signal becomes active during a VME interrupt acknowledge sequence for the interrupt level present on jumpers IACK1-IACK3.

/VSEL — This signal indicates that the VME bus is accessing the card, and triggers an arbitration sequence.

/XDTACK — This signal provides VME DTACK* for interrupt acknowledges and accesses acknowledged by the arbiter state machine.

/IACKEN — This signal enables the interrupt vector onto the VME bus during a VME interrupt acknowledge.

VIAKOUT — This signal is connected through an inverting buffer to the VME signal VIACKOUT*.

```
PAL16R4                                 PAL DESIGN SPECIFICATION
PAT000                                  3/4/86
Monochrome Workstation Card horizontal sync PAL
Integrated Solutions, Incorporated
CK137 H7 H6 H5 H4 /VSYNC /VBLNK /VLAST H3 GND
/OE H2 H1 /HSYNC /BLANK /COUNT /DAINIT H0 NC VCC

HSYNC     =:   H7 *  H6 *  H5 *  H4 *  H3 *  H2 *  H1          ;On 254-255
             +  H7 * /H6 * /H5 *  H4 * /H3                     ;On 148-151
             +  H7 * /H6 * /H5 *  H4 *  H3 * /H2 * /H1         ;On 152-153

BLANK     =:   H7 *  H6 *  H5 *  H4 * /H3 *  H2 *  H1 *  H0    ;On 247
             +  H7 *  H6 *  H5 *  H4 *  H3                     ;On 248-255
             +  H7 * /H6 * /H5 *  H4                           ;On 148-159
             +  H7 * /H6 *  H5 * /H4 * /H3 * /H2               ;On 160-163
             +  H7 * /H6 *  H5 * /H4 * /H3 *  H2 * /H1         ;On 164-165
             +  H7 * /H6 *  H5 * /H4 * /H3 *  H2 *  H1 * /H0   ;On 166
             +  VBLNK

COUNT     =:  /BLANK

DAINIT    =:   H7 *  H6 *  H5 *  H4 * /H3 * /H2 * /H1          ;On 240-241
               * VLAST

FUNCTION TABLE

CK137 H7 H6 H5 H4 H3 H2 H1 H0 /VSYNC /VBLNK /VLAST
/HSYNC /BLANK /COUNT /DAINIT
;                                                /
;                                 /  /  /  /  /  /  D
;C                                V  V  V  H  B  C  A
;K                                S  B  L  S  L  O  I
;1                                Y  L  A  Y  A  U  N
;3  H  H  H  H  H  H  H  H  N  N  S  N  N  N  I
;7  7  6  5  4  3  2  1  0  C  K  T  C  K  T  T
-------------------------------------------------
;Two cycles to reset
 C  H  L  H  L  L  H  H  H  X  H  H  H  H  X  H    ;167
 C  H  L  H  L  H  L  L  L  X  H  H  H  H  L  H    ;168
;Last line timing without VBLNK
 C  H  H  H  L  H  H  H  H  X  H  L  H  H  L  H    ;239
 C  H  H  H  H  L  L  L  L  X  H  L  H  H  L  L    ;240
 C  H  H  H  H  L  L  L  H  X  H  L  H  H  L  L    ;241
 C  H  H  H  H  L  L  H  L  X  H  L  H  H  L  H    ;242
 C  H  H  H  H  L  L  H  H  X  H  L  H  H  L  H    ;243
 C  H  H  H  H  L  H  L  L  X  H  L  H  H  L  H    ;244
 C  H  H  H  H  L  H  L  H  X  H  L  H  H  L  H    ;245
 C  H  H  H  H  L  H  H  L  X  H  L  H  H  L  H    ;246
 C  H  H  H  H  L  H  H  H  X  H  L  H  L  L  H    ;247
 C  H  H  H  H  H  L  L  L  X  H  L  H  L  H  H    ;248
 C  H  H  H  H  H  L  L  H  X  H  L  H  L  H  H    ;249
 C  H  H  H  H  H  L  H  L  X  H  L  H  L  H  H    ;250
 C  H  H  H  H  H  L  H  H  X  H  L  H  L  H  H    ;251
 C  H  H  H  H  H  H  L  L  X  H  L  H  L  H  H    ;252
 C  H  H  H  H  H  H  L  H  X  H  L  H  L  H  H    ;253
 C  H  H  H  H  H  H  H  H  L  X  H  L  L  L  H  H    ;254
 C  H  H  H  H  H  H  H  H  H  X  H  L  L  L  H  H    ;255
 C  H  L  L  H  L  H  L  L  X  H  L  L  L  H  H    ;148
 C  H  L  L  H  L  H  L  H  X  H  L  L  L  H  H    ;149
 C  H  L  L  H  L  H  H  L  X  H  L  L  L  H  H    ;150
 C  H  L  L  H  L  H  H  H  X  H  L  L  L  H  H    ;151
 C  H  L  L  H  H  L  L  L  X  H  L  L  L  H  H    ;152
 C  H  L  L  H  H  L  L  H  X  H  L  L  L  H  H    ;153
 C  H  L  L  H  H  L  H  L  X  H  L  H  L  H  H    ;154
 C  H  L  L  H  H  L  H  H  X  H  L  H  L  H  H    ;155
 C  H  L  L  H  H  H  L  L  X  H  L  H  L  H  H    ;156
 C  H  L  L  H  H  H  L  H  X  H  L  H  L  H  H    ;157
 C  H  L  L  H  H  H  H  L  X  H  L  H  L  H  H    ;158
 C  H  L  L  H  H  H  H  H  X  H  L  H  L  H  H    ;159
 C  H  L  H  L  L  L  L  L  X  H  L  H  L  H  H    ;160
 C  H  L  H  L  L  L  L  H  X  H  L  H  L  H  H    ;161
 C  H  L  H  L  L  L  H  L  X  H  L  H  L  H  H    ;162
 C  H  L  H  L  L  L  H  H  X  H  L  H  L  H  H    ;163
 C  H  L  H  L  L  H  L  L  X  H  L  H  L  H  H    ;164
 C  H  L  H  L  L  H  L  H  X  H  L  H  L  H  H    ;165
 C  H  L  H  L  L  H  H  L  X  H  L  H  L  H  H    ;166
 C  H  L  H  L  L  H  H  H  X  H  L  H  H  H  H    ;167
 C  H  L  H  L  H  L  L  L  X  H  L  H  H  L  H    ;168
 C  H  L  H  L  H  L  L  H  X  H  L  H  L  L  H    ;169
;VBLNK pass-through
 C  X  X  X  X  X  X  X  X  X  L  X  X  L  X  X
-------------------------------------------------
```

DESCRIPTION

This PAL provides the horizontal sync and blank signals, a signal which enables the display address counter, and a signal which initializes the display address counter at the end of the screen.

Hn	The horizontal counter Hn cycles from 148 to 256 over and over.
/VSYNC	This signal is the vertical sync signal. It is not used in this implementation, but is connected to allow composite sync generation with the installation of a new hsync PAL.
/VBLNK	This is the vertical blanking signal.
/VLAST	This signal comes on during the last line of a frame.

```
PAL16L8                                 PAL DESIGN SPECIFICATION
PAT000                                  6/25/86
Monochrome Workstation Card enable PAL
Integrated Solutions, Incorporated
DS0 DS1 A1 NC /LWORD /WRITE /VSELX LT /CTLSEL GND
/LTD WE0 WE1 WE2 WE3 /EN16H /EN16L /OEABX DIR VCC

IF (VCC) /WE0      =   /LT
                     + /DS0
                     + /LWORD * /A1
                     +  LWORD *  A1
                     +  LWORD * /DS1
                     + /DS1   * /A1

;        WE0       =    LT * /A1 * DS0 * DS1 *  LWORD
;                     +  LT *  A1 * DS0       * /LWORD

IF (VCC) /WE1      =   /LT
                     + /DS1
                     + /LWORD * /A1
                     +  LWORD *  A1
                     +  LWORD * /DS0
                     + /DS0   * /A1

;        WE1       =    LT * /A1 * DS0 * DS1 *  LWORD
;                     +  LT *  A1       * DS1 * /LWORD

IF (VCC) /WE2      =   /LT
                     + /DS0
                     +  A1
                     +  LWORD * /DS1

;        WE2       =    LT * /A1 * DS0 * DS1 *  LWORD
;                     +  LT * /A1 * DS0       * /LWORD

IF (VCC) /WE3      =   /LT
                     + /DS1
                     +  A1
                     +  LWORD * /DS0

;        WE3       =    LT * /A1 * DS0 * DS1 *  LWORD
;                     +  LT * /A1       * DS1 * /LWORD

IF (VCC) EN16H     =    LWORD * /A1 * DS0 * DS1 *  LT
                     +  LWORD * /A1 * DS0 * DS1 * /LT
                              * VSELX * /WRITE

IF (VCC) EN16L     =    LT
                     +  VSELX

IF (VCC) OEABX     =   /LWORD * /A1 * /CTLSEL * VSELX * /WRITE

IF (VCC) /DIR      =    LT
                     +  LTD
                     + /VSELX
                     +  WRITE

FUNCTION TABLE

DS0 DS1 A1 NC /LWORD /WRITE /VSELX LT /CTLSEL
/LTD WE0 WE1 WE2 WE3 /EN16H /EN16L /OEABX DIR
;
;                     /
;          /  /  /    C               /  /  /
```

```
;           L  W  V     T                    E  E  O
;           W  R  S     L  /                 N  N  E
;D  D        O  I  E     S  L  W  W  W  W  1  1  A  D
;S  S  A  N  R  T  L  L  E  T  E  E  E  E  6  6  B  I
;0  1  1  C  D  E  X  T  L  D  0  1  2  3  H  L  X  R
-------------------------------------------------------
;Writes to RAM
 H  H  L  X  L  L  X  H  H  L  H  H  H  H  L  L  H  L   ;Long word
 H  H  L  X  H  L  X  H  H  L  L  L  H  H  H  L  H  L   ;Even word
 H  H  H  X  H  L  X  H  H  L  H  H  L  L  H  L  H  L   ;Odd word
 L  H  L  X  H  L  X  H  H  L  L  L  L  H  H  L  H  L   ;Even byte, even word
 H  L  L  X  H  L  X  H  H  L  L  L  H  L  H  L  H  L   ;Odd byte, even word
 L  H  H  X  H  L  X  H  H  L  L  H  L  L  H  L  H  L   ;Even byte, odd word
 H  L  H  X  H  L  X  H  H  L  H  L  L  L  H  L  H  L   ;Odd byte, odd word
;Reads from RAM
 H  H  L  X  L  H  L  L  H  H  L  L  L  L  L  L  H  H   ;Long word
 X  X  L  X  H  H  L  L  H  H  L  L  L  L  H  L  L  H   ;Even word
 X  X  H  X  H  H  L  L  H  H  L  L  L  L  H  L  H  H   ;Odd word
;UART, register read
 X  X  X  X  H  H  L  L  L  H  L  L  L  L  H  L  H  H
;UART, register write
 X  X  X  X  H  L  L  L  L  H  L  L  L  L  H  L  H  L
-------------------------------------------------------
```

DESCRIPTION

This PAL generates miscellaneous enables for the Monochrome Workstation Board.

DS0, DS1, A1 /LWORD, /WRITE	These signals are positive true latched copies of the corresponding VME signals.
/VSELX	This signal indicates that the board is being selected from the VME interface.
LT	This signal indicates that data and address have been latched for a pipelined write to RAM.
/CTLSEL	This signal goes active when the UART or register is being accessed. It is generated from the VME address lines.
/LTD	This signal is a delayed copy of the signal LT. It is used during a pipelined RAM write to prevent the VME bus drivers from momentarily driving the VME data lines at the end of a RAM write.
WEn	These signals enable the four write enables on each of the four bytes of the dynamic RAM.
/EN16H	This signal enables the VME bus transceiver for the upper 16 data bits during a longword access.
/EN16L	This signal enables the VME bus transceiver for the lower 16 data bits.
/OEABX	This signal enables the latched upper data bits onto the lower data bits during non-longword reads of even addresses.

```
PAL16R8                                 PAL DESIGN SPECIFICATION
PAT000                                  7/1/86
Monochrome Workstation Card bus arbiter / refresh PAL
Integrated Solutions, Incorporated
CK69 RWPSYN /VRESET /VSELSYN /WRITE /CTLSEL /DTSTART RFPEND /LOCK GND
/OE /SELREG /SELJMP /MEMCY /DT /REFRESH /DONE STC0 STC1 VCC

/STC0     =:   /VRESET *  STC1 *  STC0 * /MEMCY * /LOCK          ;MA0
               *  RWPSYN
               * /DTSTART * /RFPEND
          + /VRESET *  STC1 *  STC0 * /MEMCY * /LOCK          ;MA0
               *  VSELSYN * /CTLSEL * /WRITE
               * /DTSTART * /RFPEND * /RWPSYN
          + /VRESET *  STC1 *  STC0 * /MEMCY * /LOCK          ;M0
               *  RFPEND * /DTSTART
          + /VRESET *  STC1 *  STC0 * DTSTART * /MEMCY        ;M0
          + /VRESET *  STC1 *  STC0 * /LOCK                   ;J0
               *  VSELSYN *  CTLSEL * /WRITE
               * /DTSTART * /RFPEND * /RWPSYN
          + /VRESET *  STC1 * /STC0                           ;M1,MA1,J1

/STC1     =:   /VRESET * /STC0                          ;M1,MA1,J1,M2,MA2,J2
          + /VRESET * /STC1 *  STC0 * /MEMCY        ;Stay in J2,R0
               *  VSELSYN
          + /VRESET * /STC1 *  STC0 *  MEMCY        ;Stay in MA2
               * /DT * /REFRESH * VSELSYN * /DONE
          + /VRESET *  STC1 *  STC0 * /LOCK         ;R0
               *  VSELSYN *  CTLSEL *  WRITE
               * /DTSTART * /RFPEND * /RWPSYN

DT        =:   /VRESET *  STC1 *  STC0 *  DTSTART * /MEMCY
          + /VRESET * /STC1 *  STC0 *  DT
          + /VRESET * /STC0 *  DT

REFRESH   =:   /VRESET *  STC1 *  STC0 * /LOCK
               * /MEMCY * /DTSTART *  RFPEND
          + /VRESET * /STC1 *  STC0 *  REFRESH
          + /VRESET * /STC0 *  REFRESH

MEMCY     =:   /VRESET *  STC1 *  STC0 * /MEMCY
               *  DTSTART
          + /VRESET *  STC1 *  STC0 * /MEMCY
               *  RFPEND
          + /VRESET *  STC1 *  STC0 * /MEMCY
               *  VSELSYN * /CTLSEL * /WRITE
          + /VRESET *  STC1 *  STC0 * /MEMCY
               *  RWPSYN
          + /VRESET * /STC1 *  STC0 *  MEMCY
          + /VRESET * /STC0 *  MEMCY

DONE      =:   /VRESET * /STC1 * /STC0
               *  MEMCY * /DT * /REFRESH *  RWPSYN
          + /VRESET * /STC1 * /STC0 *  SELJMP
          + /VRESET *  STC1 *  STC0
               *  VSELSYN *  CTLSEL *  WRITE
               * /DTSTART * /RFPEND * /LOCK * /RWPSYN

SELREG    =:   /VRESET *  STC1 *  STC0
               *  VSELSYN *  CTLSEL *  WRITE
               * /LOCK * /DTSTART * /RFPEND * /RWPSYN

SELJMP    =:   /VRESET *  STC1 *  STC0
               *  VSELSYN *  CTLSEL * /WRITE
               * /LOCK * /DTSTART * /RFPEND * /RWPSYN
          + /VRESET * /STC1 *  STC0 *  SELJMP       ;Stay in J2
               * VSELSYN
          + /VRESET * /STC0 *  SELJMP
```

FUNCTION TABLE

```
CK69 RWPSYN /VRESET /VSELSYN /WRITE /CTLSEL /LOCK /DTSTART
RFPEND STC1 STC0 /SELREG /SELJMP /MEMCY /DT /REFRESH /DONE
;         /           /                          /
;      /  V     /     D           /  /        R
;   R  V  S  /  C     T  R        S  S  /     E
;   W  R  E  W  T  /  S  F        E  E  M     F  /
;C  P  E  L  R  L  L  T  P  S  S  L  L  E     R  D
;K  S  S  S  I  S  O  A  E  T  T  R  J  M  /  E  O
;6  Y  E  Y  T  E  C  R  N  C  C  E  M  C  D  S  N
;9  N  T  N  E  L  K  T  D  1  0  G  P  Y  T  H  E
-----------------------------------------------------
;Reset
 C  L  L  H  X  X  H  H  L  H  H  H  H  H  H  H  H  ;01
;DT Cycle
 C  X  H  X  X  X  L  H  X  H  H  H  H  H  H  H  H  ;02
 C  X  H  X  X  X  L  L  X  H  L  H  H  L  L  H  H  ;03
 C  X  H  X  X  X  X  X  X  L  L  H  H  L  L  H  H  ;04
 C  X  H  X  X  X  X  X  X  L  H  H  H  L  L  H  H  ;05
 C  X  H  X  X  X  X  X  X  H  H  H  H  L  L  H  H  ;06
 C  X  H  X  X  H  X  X  X  H  H  H  H  H  H  H  H  ;07
;RAM Refresh Cycle
 C  X  H  X  X  X  H  H  H  H  L  H  H  L  H  L  H  ;08
 C  X  H  X  X  X  X  X  X  L  L  H  H  L  H  L  H  ;09
 C  X  H  X  X  X  X  X  X  L  H  H  H  L  H  L  H  ;10
 C  X  H  X  X  X  X  X  X  H  H  H  H  L  H  L  H  ;11
;Register Write
 C  L  H  L  L  L  H  H  L  L  H  L  H  H  H  H  L  ;12
 C  L  H  L  X  X  X  X  X  L  H  H  H  H  H  H  H  ;13
 C  L  H  H  X  X  H  H  L  H  H  H  H  H  H  H  H  ;14
;RAM Write
 C  H  H  X  X  X  H  H  L  H  L  H  H  L  H  H  H  ;15
 C  H  H  X  X  X  X  X  X  L  L  H  H  L  H  H  H  ;16
 C  H  H  X  X  X  X  X  X  L  H  H  H  L  H  H  L  ;17
 C  X  H  X  X  X  X  X  X  H  H  H  H  L  H  H  H  ;18
 C  L  H  H  X  X  H  H  L  H  H  H  H  H  H  H  H  ;19
;Jumper Read
 C  L  H  L  H  L  H  H  L  H  L  H  L  H  H  H  H  ;20
 C  X  H  X  X  X  X  X  X  L  L  H  L  H  H  H  H  ;21
 C  X  H  X  X  X  X  X  X  L  H  H  L  H  H  H  L  ;22
 C  X  H  L  X  X  X  X  X  L  H  H  L  H  H  H  H  ;23
 C  L  H  H  X  X  H  H  L  H  H  H  H  H  H  H  H  ;24
;RAM Read
 C  L  H  L  H  H  H  H  L  H  L  H  H  L  H  H  H  ;25
 C  X  H  X  X  X  X  X  X  L  L  H  H  L  H  H  H  ;26
 C  X  H  X  X  X  X  X  X  L  H  H  H  L  H  H  H  ;27
 C  X  H  L  X  X  X  X  X  L  H  H  H  L  H  H  H  ;28
 C  X  H  L  X  X  X  X  X  L  H  H  H  L  H  H  H  ;29
 C  X  H  H  X  X  X  X  X  H  H  H  H  L  H  H  H  ;30
 C  L  H  H  X  X  H  H  L  H  H  H  H  H  H  H  H  ;31
-----------------------------------------------------
```

DESCRIPTION

This PAL arbitrates the use of the local bus between data transfer cycles, refresh cycles, register accesses, RAM reads, and RAM writes from the pipeline. Its state sequence (a hand-drawn diagram included in the design review packet) is such that the RAM cycle time is 5 69-nanosecond clocks or 345 nanoseconds.

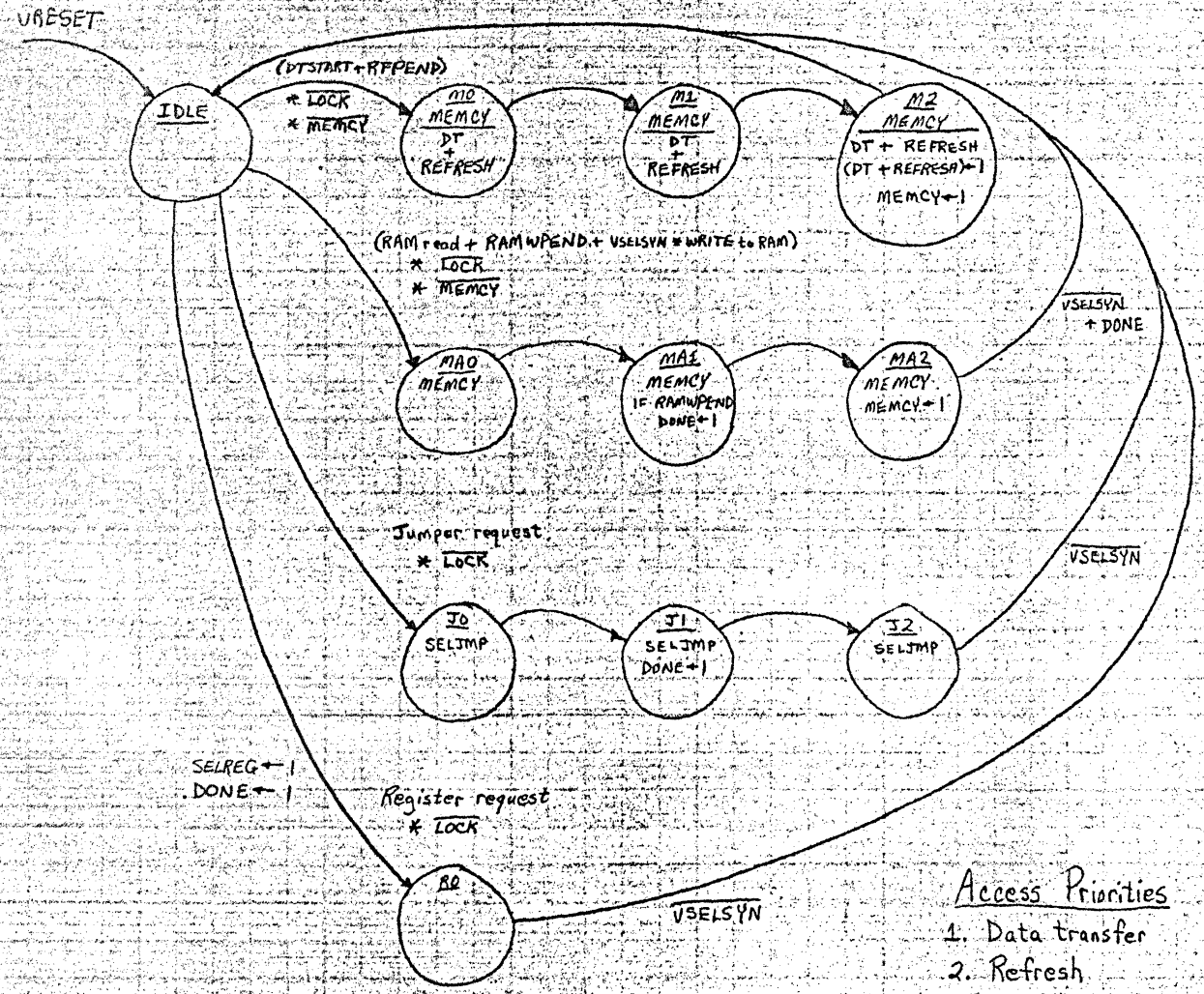
/VRESET	This is a synchronized version of the VME reset signal.
RWPSYN	This signal indicates that address and data have been latched in the write pipeline, and a RAM write should occur.
/VSELSYN	This signal indicates that the board is being selected from the VME interface. It will come on momentarily during a VME write memory transaction, so the state machine will not respond to memory writes until it sees the RAMWPEND signal.
/WRITE	This is a copy of the VME signal with the same name. While RAMWPEND is true, it is latched true.
/CTLSEL	This signal is active when the VME is requesting access to the register or the jumpers.
DTSTART	This signal tells the state machine to begin a DT cycle.
RFPEND	This signal indicates that a refresh must occur.
LOCK	This signal causes the state machine to stay in the idle state after the current transaction is completed. It goes active just before DTSTART goes active. It is used to keep any transactions from interfering with DT cycles.
/SELREG	This signal indicates that the register is currently being written to.
/SELJMP	This signal indicates that the jumpers are currently being read.
/DONE	During RAM writes, the falling edge of this signal resets RAMWPEND. During register accesses, and RAM reads, the falling edge of this signal generates a VME DTACK.
STCn	These signals comprise a state counter.
/MEMCY	This signal causes a memory cycle. It remains active for four clock cycles, and has a maximum cycle time of five clock cycles or 345 nanoseconds.
/DT	When true during MEMCY, this signal causes a data transfer cycle.
/REFRESH	When true during MEMCY, this signal causes a refresh cycle.
CK69	This is the 69-nanosecond state machine clock.

MWS TTL Useage

7-2-86

F04	9 ~~10~~ ~~11~~ 9 10
F14	~~4~~ 6 5
F11	~~1~~ ~~2~~ 3
F10	~~4~~ 3
F32	7
F38	4
F240	~~7~~ 6 ~~4~~ ~~2~~ 6 5
S51	4
F74	21
F174	5
F00	8
F08	~~1~~ 0

Synchronous Arbiter State Diagram $t_{cy} = 69ns$ Monochrome Workstation Board 6-26-86



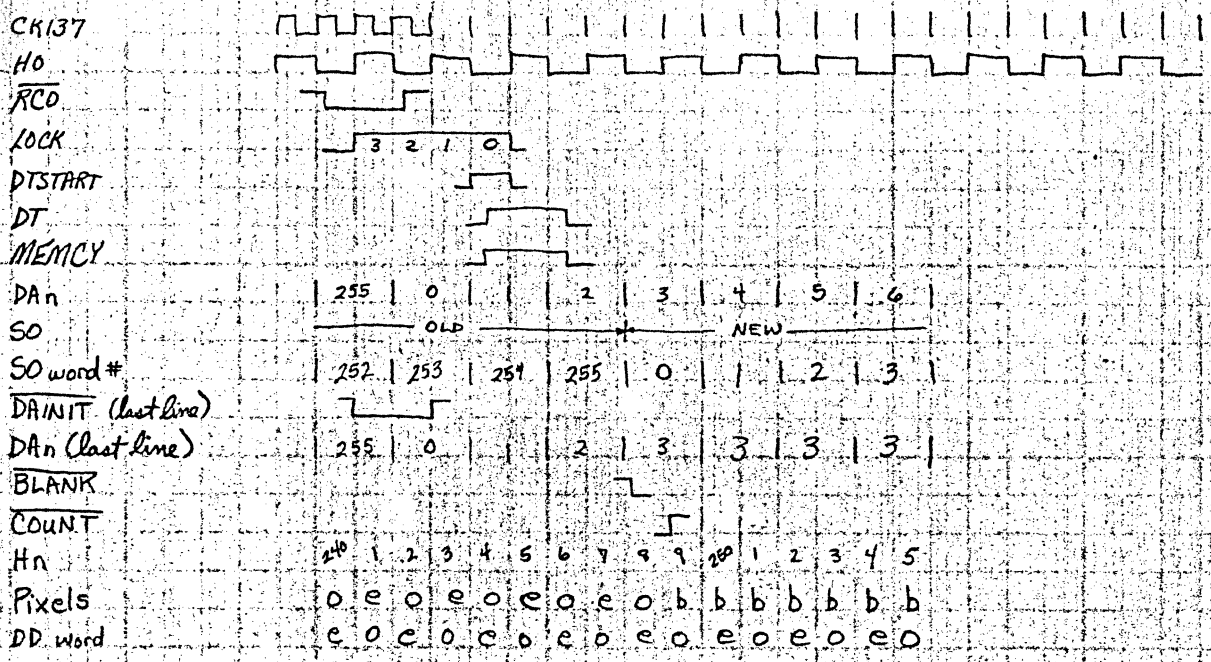
State	Mnemonics
00	M1, MA1, J1
01	M2, MA2, J2, R0
10	M0, MA0, J0
11	IDLE

Access Priorities

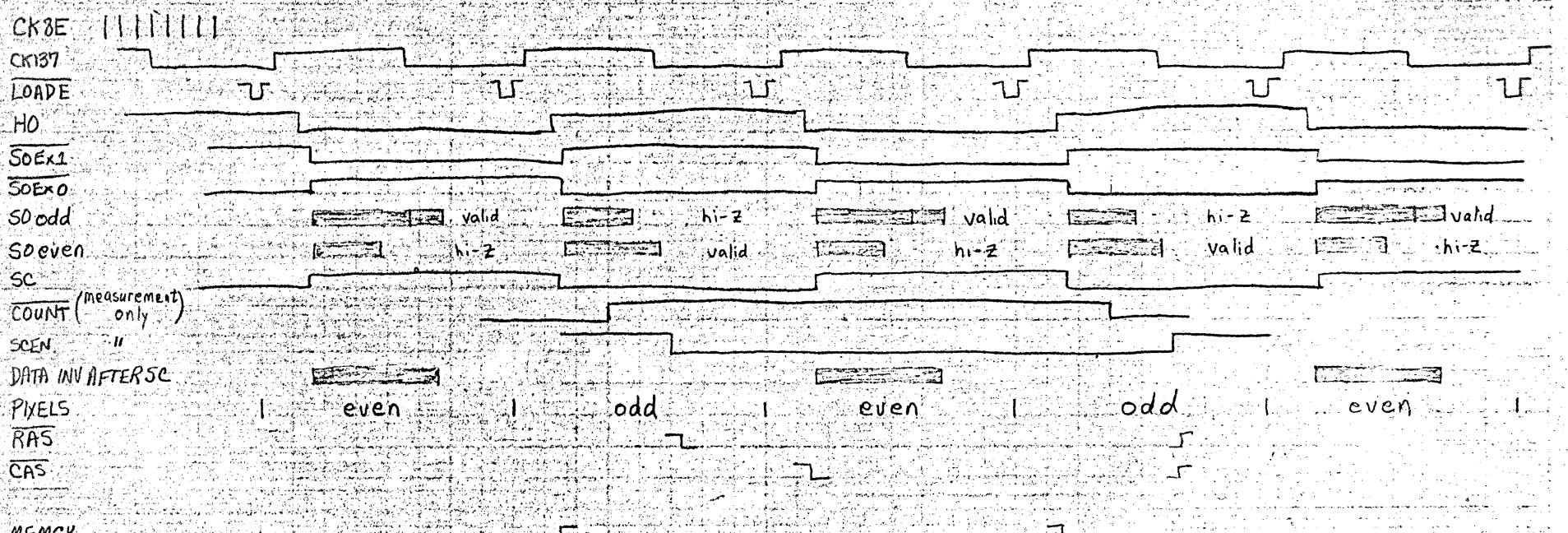
1. Data transfer
2. Refresh
3. RAM Write
4. VME cycles

Data Transfer Timing

7-1-86



32-Bit Shift Cycle 16 ns/div "even" => low-order data bits
"odd" => high-order data bits 2-5-86



Is RAM data always clocked into 8177?

$137.3 - (10136_{CK-Q} + 10125 + F163_{CK-Q} + \max(F32 + t_{SOA}, S51 + t_{SCA}) + t_{SDD}) \overset{?}{\geq} 0$

$137.3 - (5 + 6 + 11 + \max(6.6 + 50, 6 + 60) + 10) \overset{?}{\geq} 0$

$137.3 - 98 \overset{?}{\geq} 0$

$39.3 > 0$ Yes.

8177 LOAD setup w/10KH

$3.5 + 1.7 + 1.5 = 6.7$ ns much better

Is LOADE truncated by BLANK?

No: $t_{CK8E-CK137E} \ll t_{CK8E-BLANKE}$

Is 8177 DD hold time satisfied?

$10136_{CK-A\ min} + 10125_{min} + F163_{CK-A\ min} + F00_{min} + t_{SOZ\ min} > (t_{HDD} = 5ns)$ Yes.

8177 LOAD setup

$10136_{CK-Q\ max} + 10109_{max} - 10104_{min} + t_{SLOAD} \overset{?}{\leq} 8.58$ ns

$5.0 + 3.3 - 1 + 1.5 \overset{?}{\leq} 8.58$

$8.8 \not\leq 8.58$ Won't work at 80°C

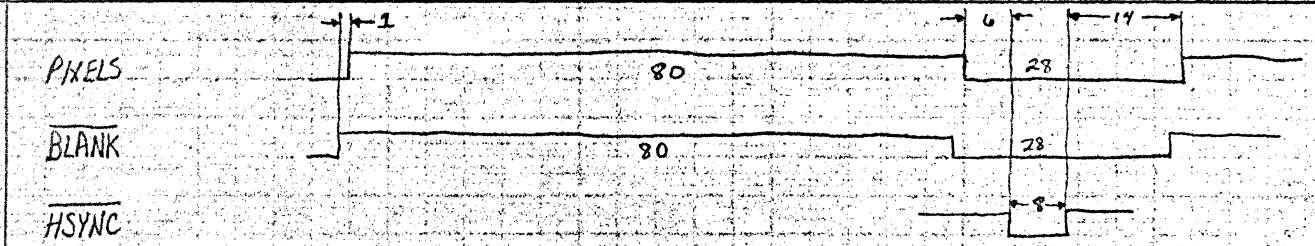
$4.4 + 2.9 - 1 + 1.5 \overset{?}{\leq} 8.58$

$7.8 \overset{?}{\leq} 8.58$ Barely Works at 25°C

USE 10KH

Horizontal Timing 5 words/div

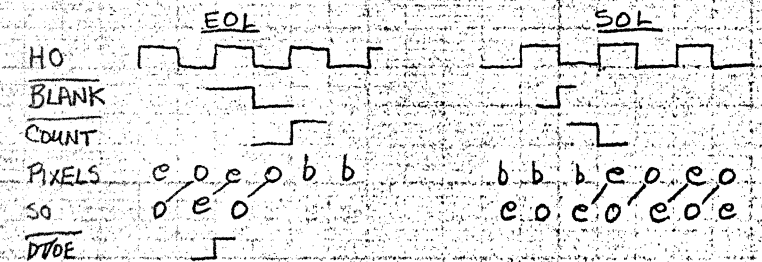
2-19-86



Increment DA once for each SC cycle.

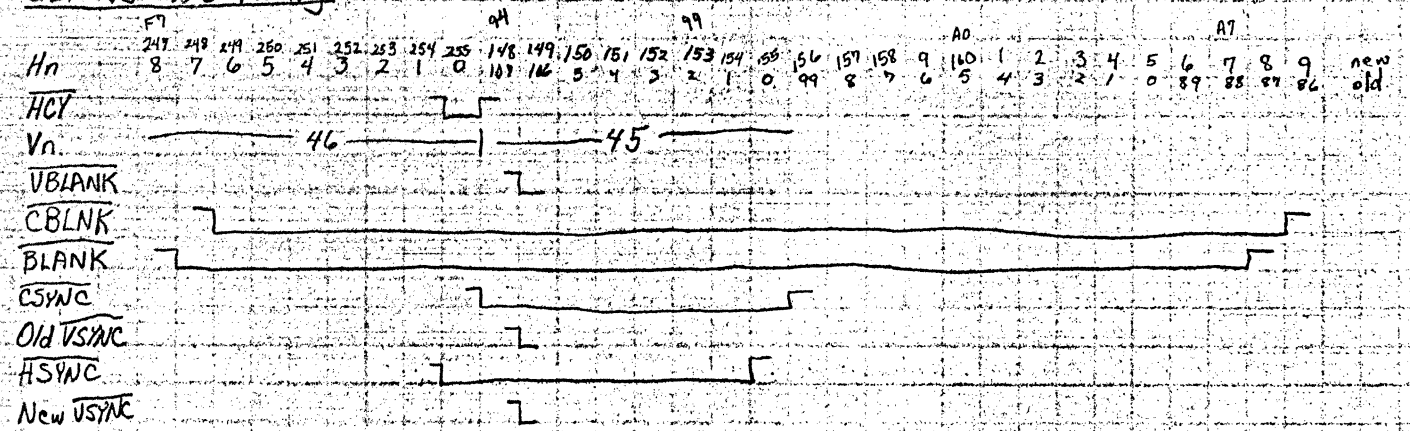
At the end of the first scan line, during blanking, DA should equal 40+3 = 43.

COUNT vs. BLANK



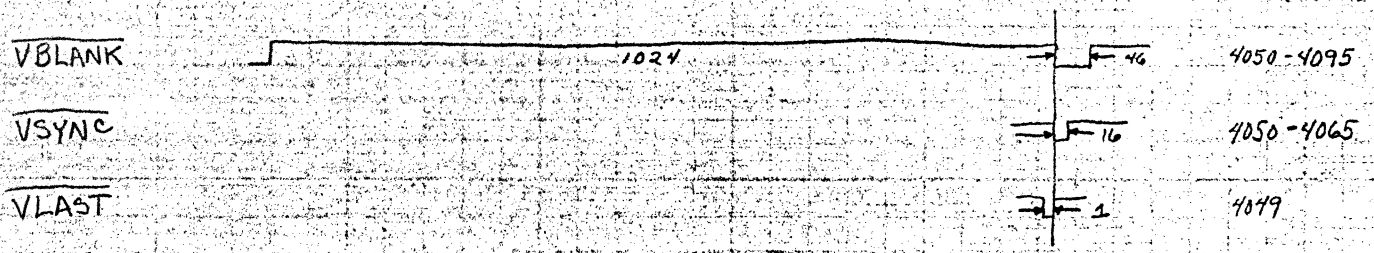
COUNT := BLANK

GIP vs. WS Timing



Vertical Timing 50 lines/div

2-19-86



1-17-86

How many lwords per refresh?

$\frac{1024 * 1280}{32} = 40960$ lwords/scan (16.667 - 0.6823) ms/scan 12.89 μs/refresh

$\frac{0.01289 \text{ ms/refresh} * 40960 \text{ lwords/scan}}{(16.667 - 0.6823) \text{ ms/scan}} = 33.03$ lwords/refresh

Choose 32. Request a refresh on DA6 falling edges & use DA7-DA14 for row address.

What is the actual refresh period?

$64 * \frac{16.667 - 0.6823}{81920} = 12.488$ μs/refresh. Uses $\frac{0.300}{12.488} = 2.4\%$ of bandwidth.

How many longwords per data transfer?

256

How many data transfers per screen?

$\frac{1024 \times 1280}{32 \times 256} = 160 = 0xA0$ (minimum BW consumption) Correction: $\frac{1024}{4} = 256$

How many lines per data transfer?

$\frac{1024}{160} = 6.4$

What is DT bandwidth consumption?

$\frac{160 \times 0.345}{16667} = 0.33\%$

What is total bandwidth inefficiency due to synchronism constraint on refresh?

refresh inefficiency = $2.4 - 1.92 = 0.48\%$

What bandwidth is consumed by DT + refresh?

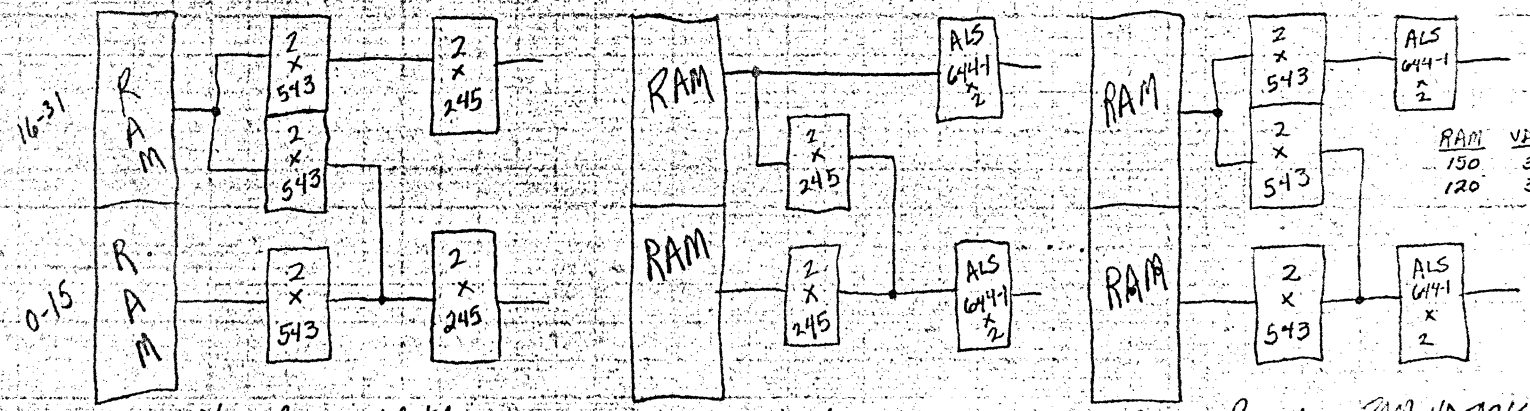
$2.4 + 0.33 = 2.73\%$

How many seconds / longword?

$8.58 * 32 = 274.56$ ns (two clocks at 7.284 MHz)

How to bus?

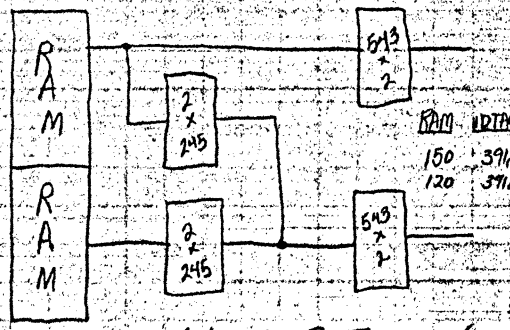
3-6-85



won't work — must latch ..., VME
10 chips

cycle won't fit into 250 ns
8 chips

Yuck. But allows RAM VDTACK at 225ns.
10 chips



Int vector chip must be right on the bus to permit intacks during pipelined writes.

AS646's cannot be doubled up on the bus.

fastest + smallest soln, BUT F543's violate VME drive/rcv spec AND int vec ALS646-1 must be thrown out
8 chips

Monochrome Workstation Loading Analysis

3-5-86

Is VAn OK?

max (F373, S244, F521) ? < 600/50
max (600/20, 400/50, 600/20) < 600/50 Yes.

Is VDn load OK?

2 × ALS646-1 ? < 600/50
400/40 < 600/50 Yes.

Is VDn drive OK?

48/15 = ALS646-1 ? > 48K/3K Yes.

Is D_n^{0-15} OK?

LS174 + F245 + ALS646-1 ? < 2681
650/90 = 400/20 + 50/50 + 200/20 ? < 2400/400 Yes.

RAMWPEND

$F174_{CLR}$ + 2 × ($ALS646_{SBA}$ + $ALS646\text{-}1_{CBA}$) + $F74_{CL}$ + $F74_{CK}$? < F14
600/20 + 400/80 + 1800/20 + 600/20 < 20K/1K
3400/140 < 20K/1K Yes.

RAMWPEND

4 × $F245_{DIR}$ + 1648 + $F74_{CL}$ + 3 × $F373_{LEN}$? < F14
2400/80 + 250/20 + 1800/20 + 1800/60 < 20K/1K
6250/180 < 20K/1K Yes.

RDS

5 × $F74_{CL}$? < F04
9000/100 < 20K/1K Yes.

T50

4 × $F153_{SO}$ + 2 × $F74_{CL}$? < DL
2400/80 + 3600/40 < 32K/400 Yes.

Is D16-31 OK?

41264 ? > F245 + ALS646-1 + 41264
4200/2K ? > 600/50 + 200/20 + 10/10
4200/2K > 810/80 Yes.

RDYACK

$F74_Q$? > 6 × $F543_{LEAB}$
20K/1K > 3600/120 Yes.

VSELX

$F74_Q$? > F08 + 2 × $F74_R$ + F10
20K/1K > 600/20 + 3600/10 + 600/20 Yes.

Monochrome Workstation Loading

3-9-86

T75

$DL \overset{?}{\geq} 3 \times F74_{CK} + 6F$

$32K/400 > 1800/60 + 3600/120$

yes.

3-7-86

Monochrome Workstation Timing

Does REND go away before VSELX goes away?

$$F74_{CLR\text{-}Q_{max}} \overset{?}{<} F00_{min} + F74_{CLR\text{-}Q_{min}} + F32_{min} + F04_{min}$$

$$10.5 \overset{?}{<} 2 + 3.2 + 3 + 1.5$$

$10.5 \nless 9.7$ Yes. Reset SYEND+REND w/VSELX. OK now.

What is t_{RAH} minimum?

$25 - F00_{max} + \min_{S-3,2}(F51, F153) = 25 - 6 + 3.2 = 22.2$ (need 20) Marginal. Put in an F32 in T50.

$25 - F00_{max} + \min_{S-3,2}(F151, F153) + F32_{min} = 25 - 6 + 3.2 + 3 = 25.2$ Better.

What is the possible range of $t_{SC\uparrow - DT\downarrow}$?

$$min = -69 + 20R8A_{min} + 175 + F74_{CKQ_{min}} + S51_{min} - S51_{max} - F163_{CK\text{-}Q_{max}}$$

$$= -69 + 0 + 175 + 3 + 0 - 6 - 11 = 92\ ns$$ Fine.

$$max = -69 + 20R8A_{max} + 175 + F74_{CK\text{-}Q_{max}} + S51_{max} - S51_{min} - F163_{CK\text{-}Q_{min}}$$

$$= -69 + 15 + 175 + 10 + 6 - 0 - 3 = 134\ ns$$ Fine.

RAM timing looks OK... checked parameter by parameter.

Is select ckt ok?

$$max(S244, F521) + 20L8A + F74_{su} \overset{?}{<} F14_{min} + F32_{min} + 40$$

$$max(9, 11) + 25 + 3 \overset{?}{<} 2.5 + 3 + 40$$

$39 < 45.5$; 6.5 ns margin Yes.

Is WRITE pipeline select OK?

$$F74_{CKQ_{min}} + F10_{min} + F04_{min} + 40 + F32_{min} + F14_{min} - F373_{max} - S133_{max} - F04_{max} - F32_{max} - F74_{su} > 0$$

$$3.8 + 2 + 1.5 + 40 + 3 + 2.5 - 8 - 7 - 6 - 6.6 - 3 \overset{?}{>} 0$$

$22.2 > 0$ Yes.

MWS

6-22-86

Can delay line connected to RAMWPEND be taken out?

$$F74_{CKOmin} + F14_{min} + F10_{min} + F04_{min} \overset{?}{\geq} F74_{CPWmin}$$

$$3.8 + 2.5 + 2.0 + 1.5 \overset{?}{\geq} 5.0$$

$$9.8 \geq 5.0$$

$$F74_{S-Qmax} + F74_{trec} \overset{?}{\leq} F14_{min} + F10_{min} + F04_{min}$$

$$10.5 + 2.0 \overset{?}{\leq} 2.5 + 2.0 + 1.5$$

$$12.5 \not\leq 6.0$$

NO

What is DSn* to DTACK delay for RAM writes?

$$50 + F74_{CKO} + F10 + F04 + F74_{CKO} + 20 + F04 + F74_{CKO} + F10 + F38$$

$$50 + 9.2 + 6.0 + 6.0 + 9.2 + 20 + 6.0 + 9.2 + 6.0 + 6$$

127.6 ns worst case

$$5.5 + 4.2 + 40 + 6.2 + 3.7 + 3.7 + 6.2 + 20 + 3.7 + 6.2 + 3.7 + 6$$

109.1 ns typical

Put in F11 and trigger RAM WR DTACK before delay line.

$$F74_{CKOmin} + F74_{CKOmin} + F10_{min} + F38_{min} + F14_{min} + F32_{min} + F08_{min} + F74_{SAmin} + F11_{min} \overset{?}{\geq} F74_{CPWmin}$$

$$3.8 + 3.8 + 2.0 + 0 + 2.5 + 3.0 + 2.5 \quad \therefore \quad >> 5.0$$

What is delay now?

$$50 + F74_{CKO} + F11 + F74_{CKO} + F74_{CKO} + F10 + F38$$

$$50 + 9.2 + 6.6 + 9.2 + 9.2 + 6.0 + 6 = 96.2 \text{ ns worst case}$$

$$5.5 + 4.2 + 40 + 6.2 + 4.2 + 6.2 + 6.2 + 3.7 + 6 = 82.2 \text{ ns typical}$$

MWS

7-1-86

Is screen timing carry path OK?

$$LS169_{LD\,setup} + F169_{CK\text{-}TC} + (F169_{PT\text{-}TC} \times 2) + LS169_{PT\text{-}TC} \leq 137$$

$$35 + 17 + 18 + 25 \leq 137$$

$$95 < 137$$

What is the maximum time between full IDLE states? (RAM read)

$$16R8A_{CKO} + F04 + F32 + 150 + F74_{CKO} + F32 + F04 + F11 + S51 + 69\,sync + 69\,response$$

$$16 + 6 + 6.6 + 150 + 9.2 + 6.6 + 6 + 6.6 + 6 + 69 + 69 = 350\,ns$$

$\frac{350}{69} = 5.07$ ∴ Lock must be on 6 clock cycle

What is t_{ASC}?

$25 - F151_{S\text{-}Y} + F10_{min} = 25 - 8 + 2 = 19\,ns$ min = 0

$t_{WCS} \leq 25 - F74_{CKO} - F00 + F10_{min} = 25 - 9.2 - 6.0 + 2 = 11.8\,ns$ min = 0

$t_{DLS} \leq 25 - S51 - 16R8A\,skew - F04 + F00_{min} = 25 - 6 - 6 + 2 - skew = 15 - PAL\,skew$ min = 0

$t_{DTR} \leq 25 - S51 + F74_{CKO} + F74_{CKOmin} + F00_{min} = 25 - 6 - 9.2 + 3.8 + 2 = 15.6\,ns$ min = 10

Monitor Notes

7-2-86

Monitorm, Dick Isenhart (612) 935-4151 ISI uses VR1000 L20 P104 1E
5740 Green Circle Dr., Minnetonka MI 55343
Ikegami, Jim Dempsey (415) 449-1794 " " DM2050
HQ (201) 368-9171
Mr. Kazuma (213) 534-0050

Monitor Practical Limits - Dick Isenhart

HR = 3 μs (maybe 2.8) VR = 600 μs HF = 95 KHz (landscape)

HF (15" short axis) = 100 KHz HF (20" landscape) = 89 KHz

Std. sizes - displayable area

15" - 7.56" x 10.14"; 17" - 9.10" x 12.15"; 20" - 10.50" x 13.50"

Fast phosphor flicker - - seen by what % of population

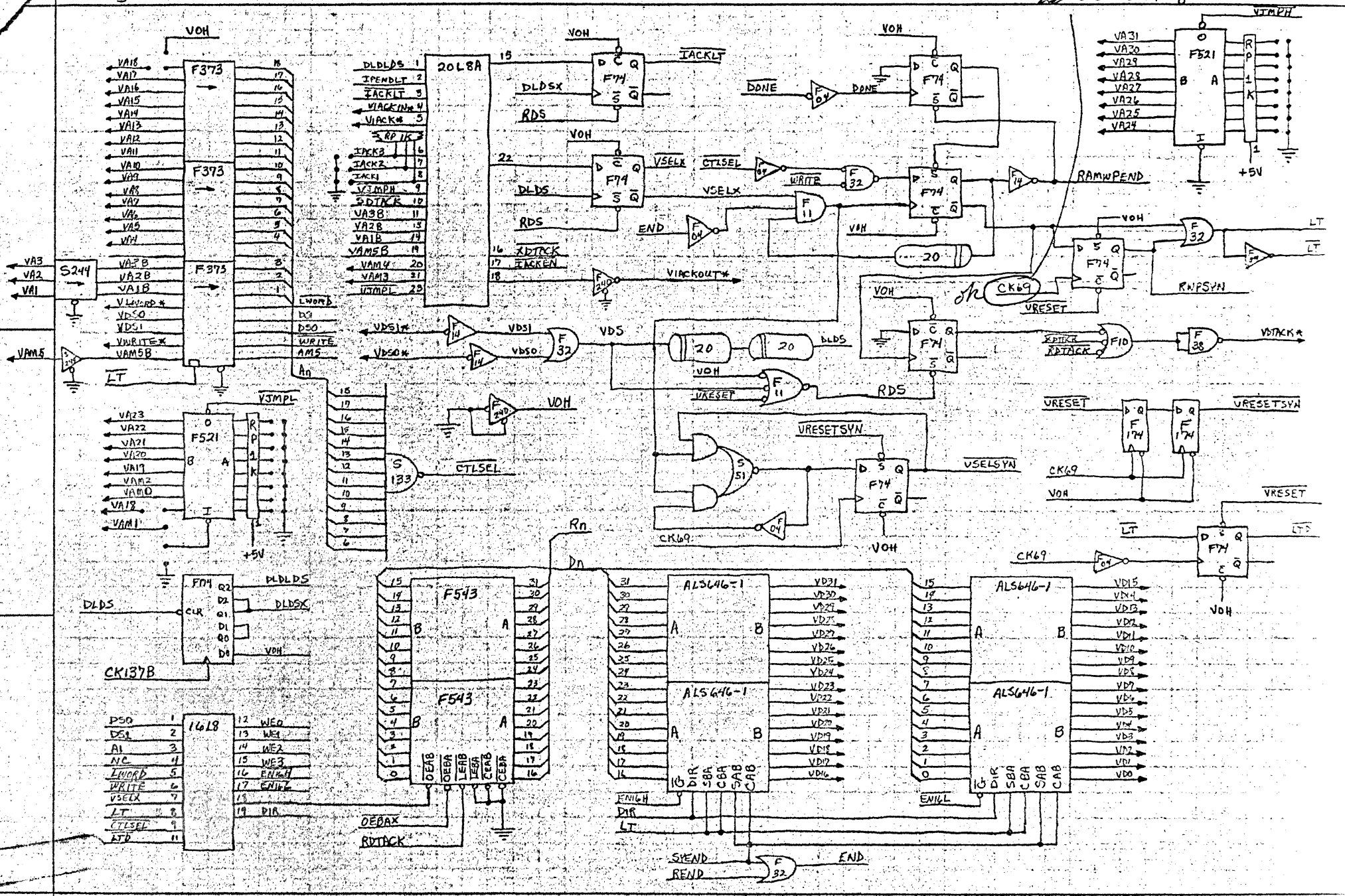
66 Hz - 95% see none; 60 Hz 80% see none; 50 Hz - seen by large % age

Monitors w/ high persistance phosphor can be used at 50 Hz.

Sun has 63 or 64 Hz VF. Majority has 60 Hz.

ADDRESS MODIFIERS ACCEPTED / Monochrome Workstation Board

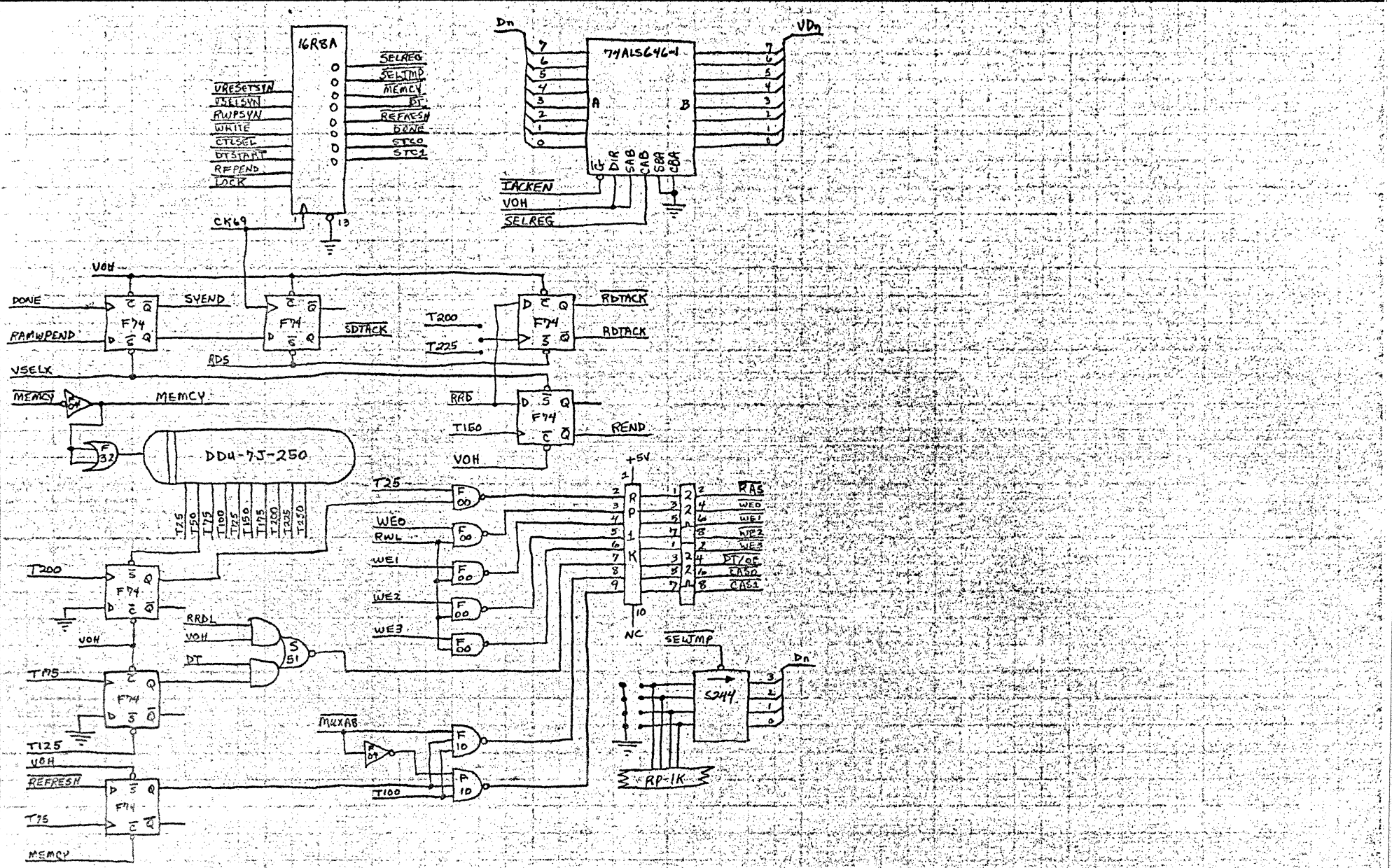
1-28-86



Why 2 sets of latches
F543 + ALS646

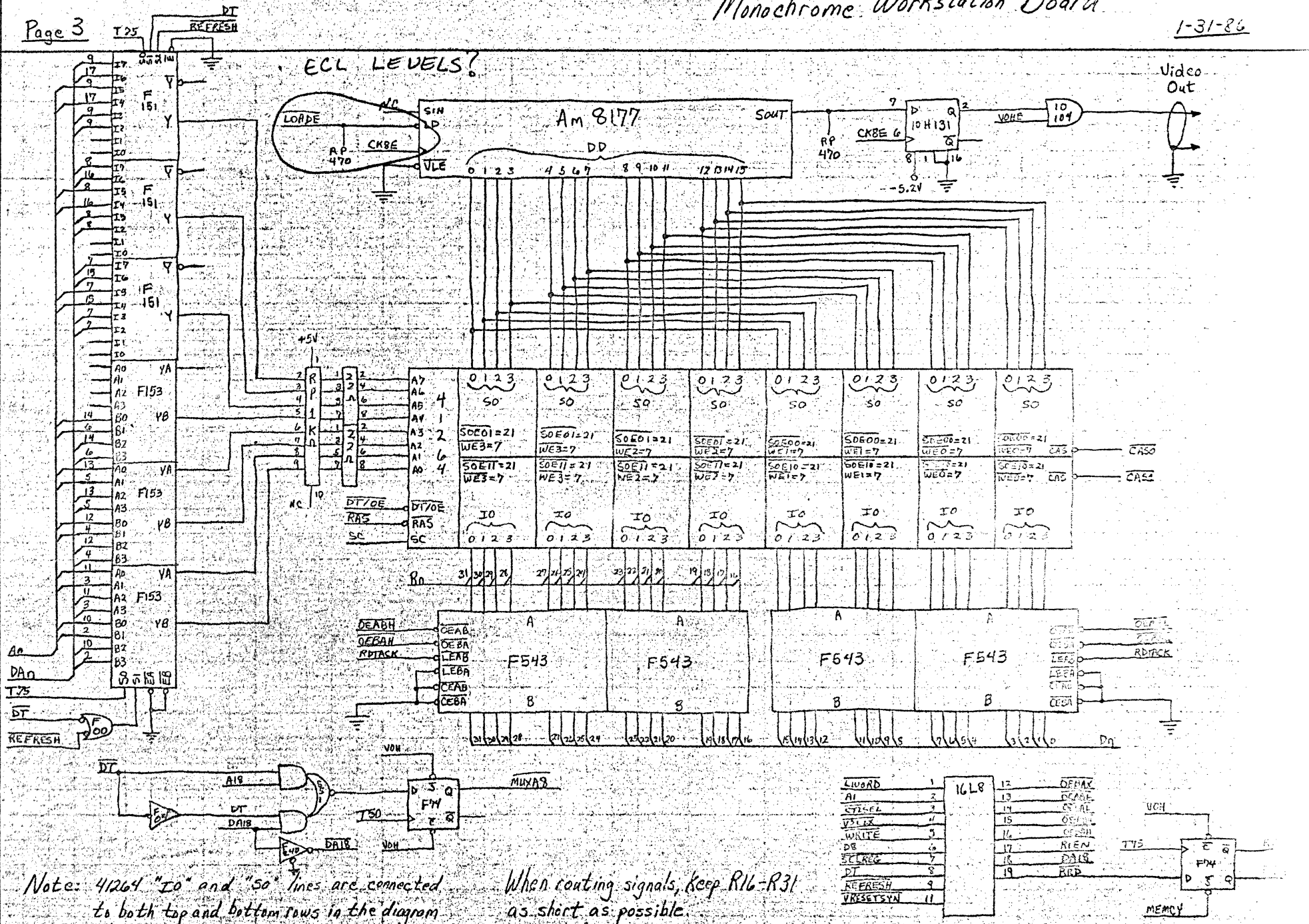
Monochrome Workstation Board

6-24-86



Monochrome Workstation Board

1-31-86

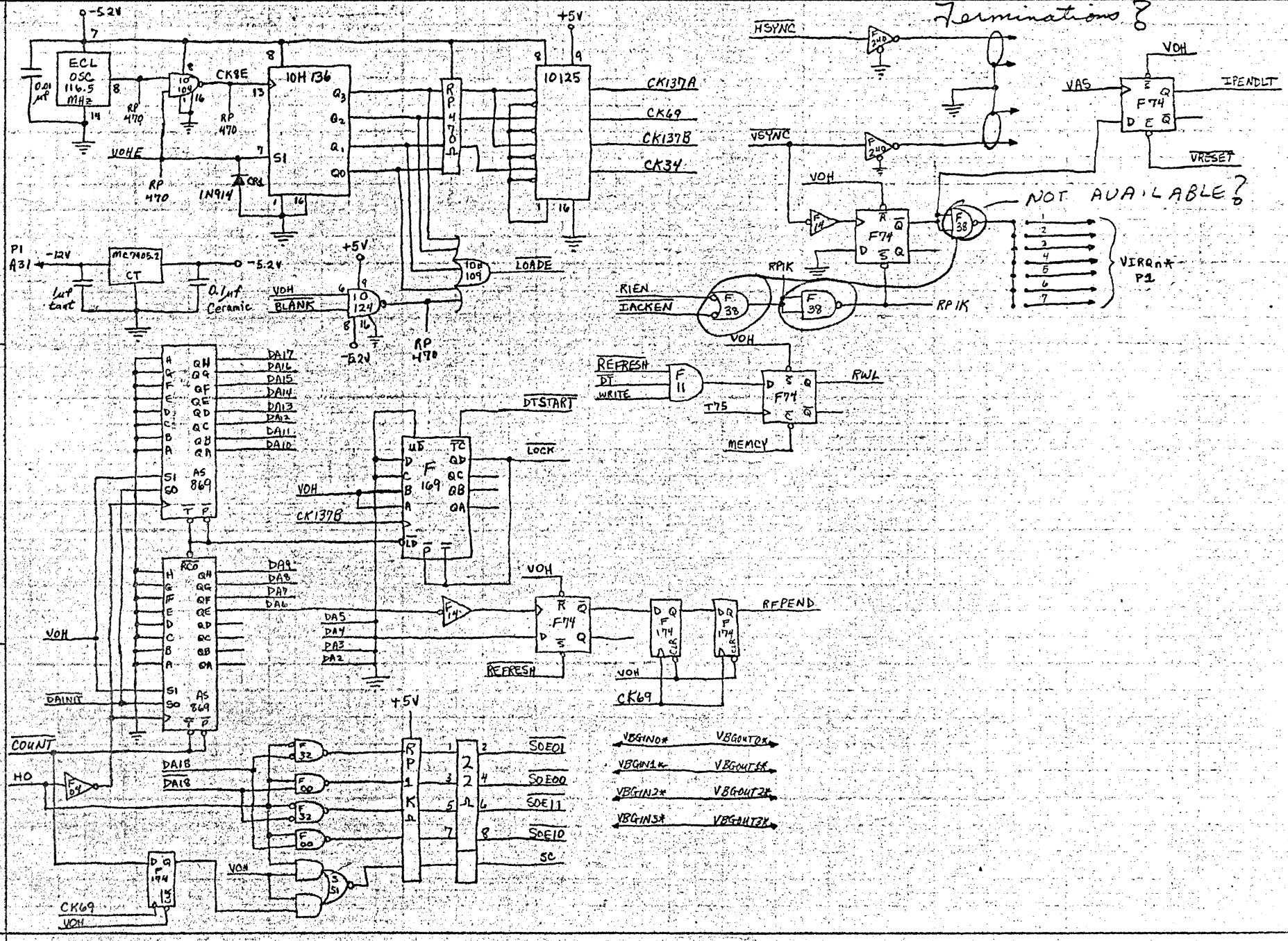


Note: 4164 "IO" and "SO" lines are connected to both top and bottom rows in the diagram above.

When routing signals, keep R16-R31 as short as possible.

Monochrome Workstation Board

2-3-86



Monochrome Workstation Board