N O T I C E :

The STEP button was changed to the HALT button on the operator console after the printing of this manual. The change is only in the name of this button -- its function has in no way been altered. Therefore, all information concerning the STEP button now applies to the HALT button.

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

TABLE OF CONTENTS (continued)

T A B L E O F C O N T E N T S (continued)

TABLE OF CONTENTS (continued)

TABLE OF CONTENTS (continued)

L I S T O F I L L U S T R A T I O N S

L I S T O F I L L U S T R A T I O N S (continued)

LIST OF ILLUSTRATIONS (continued)

LIST OF ILLUSTRATIONS (continued)

LIST OF ILLUSTRATIONS (continued)

L I S T O F T A B L E S

INTRODUCTION

INTRODUCTION

Litton Electronic Business System's 1600 series central processor is a compact, stored-program computer. The basic storage medium is a magnetic drum, and a variety of logic circuits and flipflop registers are used to record, playback, and interpret the information recorded on the drum. Almost all of the logic circuitry is made-up from integrated-circuit packages, mounted on printed circuit boards inside the processor. The remaining circuitry utilizes discrete components. Information flow within the processor is bit-by-bit, in a serial shift manner. Information flow between the processor and its peripheral equipment is in 8-bit bytes, in a parallel manner. The processor can operate with a variety of available peripheral equipment via the 1966 Standard 27 Wire Interface. This includes the Model 11 or 13 Alpha-Numeric Keyboard, Model 30 Printer, and the Model 60/70 Reader and Punch.

The basic operation of the different models of the 1600 series central processor is the same. The storage area on the drum, however, is different for each model. Presently, there are only 2 models in production; an EBS 1601 Central Processor and an EBS 1602 Central Processor. The storage capacity of the EBS 1601 is 4096 words whereas the capacity of the EBS 1602 is 2048 words, or half that of the EBS 1601.

The 1600 processors are housed in small desk-shaped cabinets, 28 inches high x 28 inches long x 21.5 inches wide. In addition, an operator console is mounted to the top of the cabinet, making the overall height 35.5 inches. Basic construction of the cabinet is of vinyl enamel painted steel except for the top made of Formica. Access to the electronic circuits and drum is gained through removable side panels and the top.

Power consumption of the 1600 processor is approximately 500 watts. The processor is available in two versions; one for use in the U.S.A. which is wired for use with 115-volt, 60-cycle power; one for use in Europe which is wired to use 230-volt, 50-cycle power. Processors used in France are field modified to use 115-volt, 50-cycle power.

CHAPTER 1

GENERAL DESCRIPTION

CHAPTER 1. GENERAL DESCRIPTION

1.1 CAPABILITIES AND LIMITATIONS

1.1.1 GENERAL INFORMATION

The EBS 1601 is a binary, serial, 40-bit word processor with drum memory. Each of these terms is discussed briefly to indicate its bearing on the operational characteristics of the processor as a whole. Since the primary application of this processor is in the field of accounting, special attention is given in this section to the areas of input, output, and the arithmetic functions that must be performed by accounting processors.

The term binary refers to the fact that all arithmetic within the processor is performed with the numbers expressed in base 2 notation. The binary number system offers 2 distinct advantages in the simplicity of design of the arithmetic circuits and increased efficiency in the utilization of storage. Binary arithmetic units typically contain only 1/3 to 1/2 of the components required in a unit that operates in base 10 or other notational system. The binary unit normally operates at a higher speed when performing arithmetic since there is no necessity for the correction cycles required in other systems. Storage of information in binary format permits an increase in memory capacity of from 20% to 100% over present day decimal or character oriented systems.

The denotation of the EBS 1601 as a serial processor stems from the method in which information is processed within the system. Information is entered into the system in a parallel fashion, one 8-bit byte at a time. As the information enters the processor it is converted to the serial form and all internal operations are then carried out by examining one bit of information at a time. This type of organization provides for the least amount of hardware within the processor.

To simplify the handling of data within a serial system some provision is normally made to group a series of bits into a larger unit of information called a word. In the general case, this grouping is accomplished by dividing the memory of the processor into word units that contain an equal number of bits. This type of memory organization is known as fixed-length word memory and is the type employed in the EBS 1601. The length of the word in the EBS 1601 is 40 bits and there are 4096 such words in the processor's memory.

The 40-bit word of the EBS 1601 is capable of storing an 11 decimal digit number plus sign. If all of the bits are considered as numeric values,

the capacity would be slightly greater than 12 digits; but it is necessary to utilize 1 or 2 of the bits for representation of the sign of the number and to control arithmetic overflow. The 40-bit word of the processor is ample for most business applications.

The word size also has a bearing on the capability of the system when processing alphabetic data. In the case of the EBS 1601, it is possible to pack 5 or 6 alphabetic characters in each word. Messages of longer length require multiple words and the linking together of these words during input or output must be accomplished by programming. This has a definite effect on the speed of alphabetic transmission since a separate memory access must be made for every 5 or 6 character portions of a message.

1.1.2 COMMANDS AND INSTRUCTION WORDS

The command repertoire of the EBS 1601 contains about 44 primitive commands. Within a 40-bit instruction word several of these commands can be grouped together since an EBS 1601 command is either 8 or 16 bits long. In order to perform useful arithmetic operations, several commands must be grouped together and arranged in some order within the instruction word. For example, to add 2 numbers together and store the result requires the execution of 4 commands. The basic sequence is: 1, bring the first number from memory to the arithmetic unit; 2, add the second number to the first; and 3, store the result back into memory. Only 2 of the above commands can be stored in one 40-bit word in memory, consequently a fourth command must be inserted in the sequence that brings the second required instruction word from memory to the control section of the processor. Access time to instruction words and data words must be computed to determine the time that is required to complete the operation described above. If it is possible to arrange all of the memory words in the best possible manner the time would be .00064 seconds. However, it is reasonable to assume that this ideal can not always be achieved. The worst-case time for the above sequence is .02 seconds if it is necessary to allow maximum access to each word. The average of these 2 times results in a figure of .01032 seconds. It should be noted that if the result is to be stored into the same location as one of the original numbers the minimum time for the sequence would be increased to .005 seconds by the memory cycle time (i.e., time required for repetitive reference to a given memory location). This increases the average to .0125 seconds. This example was chosen since it represents the type of calculation that is prevalent in accounting processors.

A program for the EBS 1601 consists of 2 types of instruction sequences. The first of these is the control program that fully defines and controls the application that is to be performed by the system. The second type of sequence is called a subroutine and consists of the instructions necessary to perform functions that occur frequently in the course of

executing the control program. Examples of functions performed by subroutines are data input, data output, multiplication, and division. These functions are required in practically any application and are normally written in a standard form compatible with general programming techniques. Special situations sometimes arise that do not lend themselves to the use of general purpose subroutines. This is particularly true in dealing with applications that have fixed requirements on data format during input and output; or when the magnitude of the numeric fields that are encountered can be predetermined.

1.1.3 EXECUTION TIMES

Several general purpose routines have been written for the EBS 1601 to determine the execution times for multiplication, division, and output of numeric data. The routine for input of numeric data is written for a system that is assumed to have input via a keyboard or paper tape reader that transmits in USASCII code. In the following description of these routines, it should be understood that they are written solely for the purpose of investigation and not to the specifications of any specific application.

The multiplication routine is designed to form an 80-bit product as the result of multiplying two 40-bit operands. The sign of the product is computed by the routine, and the result is scaled decimally to any range specified. The routine occupies about 40 words of storage and requires a fixed time of .055 seconds to complete the multiplication and scaling. To calculate the total time required for multiplying 2 numbers and storing the result, access time for the various operands and instructions must be included. The sequence is as follows:

Instruction word 1 -	a.	Bring first number from memory
	b.	Store number as multiplicand
Instruction word 2 -	a.	Bring second number from memory
	b.	Store as multiplier
Instruction word 3 -	a.	Execute the Multiply subroutine
	b.	Store product in memory

The best case time for executing the above sequence is .0013 seconds, while the worst case is .040 seconds for an average of .02 approximately. Adding the fixed time of .055 seconds for the routine gives a total of .075 seconds. This implies that about 13 multiplications can be performed per second.

The division routine is designed to divide one 40-bit word by another and produce a signed quotient within the range of accuracy specified. The routine occupies about 44 words of memory and requires a fixed time of .075 seconds to complete the division process. The sequence of in-

structions that must be processed to set-up the dividend and divisor and store the product is similar to those for the multiply routine. The total time for division and storage of the result is about .095 seconds, indicating slightly more than 10 divisions per second.

The output routine is designed to convert a 40-bit binary number into decimal digits under the control of another 40-bit word that specifies the format of the output message. This format, or edit word, specifies the number of digits to be output, which of the digits are significant, the location of commas or decimal points within the field, and whether or not a sign is to be output. The edit word also allows the programmer to insert slashes or spaces between characters and provides filler characters for protection of amounts when required. The actual characters that are transmitted to the output device are retrieved from a table that is part of the routine. Changing the contents of the registers in this table changes the code to whatever form is required by the device without any changes in the routine.

The output routine occupies about 45 words of memory and produces one character every drum revolution, or approximately 200 characters per second after initial set-up. The time involved in set-up is similar to the time required for entry to a multiply or divide routine since 2 words must be retrieved from memory. To this .02 seconds must be added an additional .015 seconds since the routine requires this much time to prepare the number for conversion and return to the main control routine when output is complete. The set-up and recovery time for the routine is therefore equal to .035 seconds or the time that is required to output a 7-digit message. This indicates that the effective rate for output of successive 7-digit fields is 1/2 of the rate of the routine, or 100 characters per second.

A final important factor to consider in the processing time of the output routine is the fact that the starting point of the sequence of instructions that produces the output characters occurs only once per drum revolution. If the output device is not ready to accept the character that the processor attempts to transmit, a delay of one entire drum revolution must occur before the sequence of conversion instructions may be entered again. This means that a device that takes longer than one drum revolution to process a character received from the processor reduces the speed of the routine from 200 characters per second to 100 characters per second or lower. To ensure the 200-character per second rate would require a device that can accept characters at a rate of 210 to 220 per second. Alphabetic data that has been stored in the memory of the processor in a code compatible with the output device may be output at much higher rates since no conversion is necessary.

1.2 BLOCK DIAGRAM ANALYSIS

In order to think of the EBS 1601 in terms of a complete system, it is advantageous to use a block diagram. Figure 1.1 is a block diagram of the EBS 1601. It shows the processor in terms of four basic units; memory, control, arithmetic, and input-output (I/O). The memory unit represents the processor's drum memory. Associated with memory are all the record and playback amplifiers, retiming flipflops, and control gates. The control unit represents the registers which control the operation of the processor by executing its stored program. Also associated with the control unit are the operator's console, timing circuits, and control flipflops. The arithmetic unit represents a 2-input adder/subtractor and the accumulator register. The I/O unit represents the buffer register and its associated gates. This unit serves as the connection link between the peripheral equipment and processor.

Information from a peripheral device enters the processor via the buffer register of the I/O unit. This information may either be in the form of characters with or without a parity bit, or in the form of status data which concerns the operation of a selected peripheral device. From the buffer register the information goes directly into the accumulator register of the arithmetic unit via the "accumulator input character, status" path. At this point, the program in execution can cause the control unit, via the "general control" path, to do one of 3 things with the information in the accumulator. It can allow the information to remain in the accumulator for later use, transfer the information via the "storage record" path into the memory unit for storage, or transfer the information back into the buffer register with or without the addition of a parity bit (parity may be either even or odd, as determined by the programmer).

The control paths show that the control unit controls each of the other major units. The memory unit can be instructed by the control unit, via the "storage control" path, to record and playback storage information to and from the memory and arithmetic units. This is done by the "storage record" and "storage playback" paths. The arithmetic unit or some part of it is used in about 65 of the processor's commands under the control of the control unit via the "general control" path. This path is, therefore, the most used path in the processor. The I/O unit is controlled by the "I/O control" path.

The control paths also show that the control unit can receive, under special conditions, control information from the arithmetic and I/O units. Control information from the arithmetic unit consists of whether or not a conditional command is to be executed. This form of feedback from the arithmetic unit to the control unit is essential to any processor. Control information from the I/O unit is in the form of a Busy signal which if present during input and certain output operations prevents the execution of the command which initiated the input or output

operation, and advances the program to the next command of the instruction word.

The information paths show that the path from the memory unit to the control unit is used only for jump commands. These commands are the means by which a new storage word can be brought into the control unit from the memory unit to replace an existing word in the control unit. The information path from the control unit to the arithmetic unit is used only for the Jump Mark command. This command, in addition to transferring a storage word from memory to the control unit, transfers the existing word in the control unit to the accumulator. The "jump to accumulator" path is used only for the command of this name which transfers the 1-word contents of the accumulator into the control unit, replacing the existing word in the control unit. The control paths also show that output information can enter the I/O unit from either the arithmetic unit or can come directly from the control unit in the form of immediate output.

Output information to the I/O unit may either be in the form of a character or a device select code. The device select code is the means by which peripheral devices are selected for communication with the processor. This is discussed in more detail in paragraph 3.6.

1.3 MEMORY

The basic storage medium of the EBS 1601 is a magnetic drum. The drum can be divided into 4 areas of storage; (1) general storage tracks, (2) scratchpad loop, (3) block interchange loop, and (4) master timing tracks. Each of these areas is discussed in the following text.

1.3.1 GENERAL STORAGE

The general storage area of the drum consists of 32 separate tracks, each having sectors numbered 0-127 around the drum. A single head is used for both recording and playing back information or to and off of each track. Tracks 31 and 32 are special tracks in that they cannot be recorded upon without first performing a service adjustment. In normal processor operation tracks 31 and 32 are playback-only, or as they may otherwise be called "sealed" tracks. A special program, OPUS, is recorded on these two tracks prior to their being sealed. The OPUS program is used to aid in program debugging and loading. For more information about OPUS, refer to the 1600 Programming Manual.

Each of the 32 general storage tracks contain 5120 bits, or 128 words (1 word = 40 bits). The 128 words per track are recorded so that they are aligned across the drum. This means the words on each track all begin and end at the same place across the drum. The space occupied by

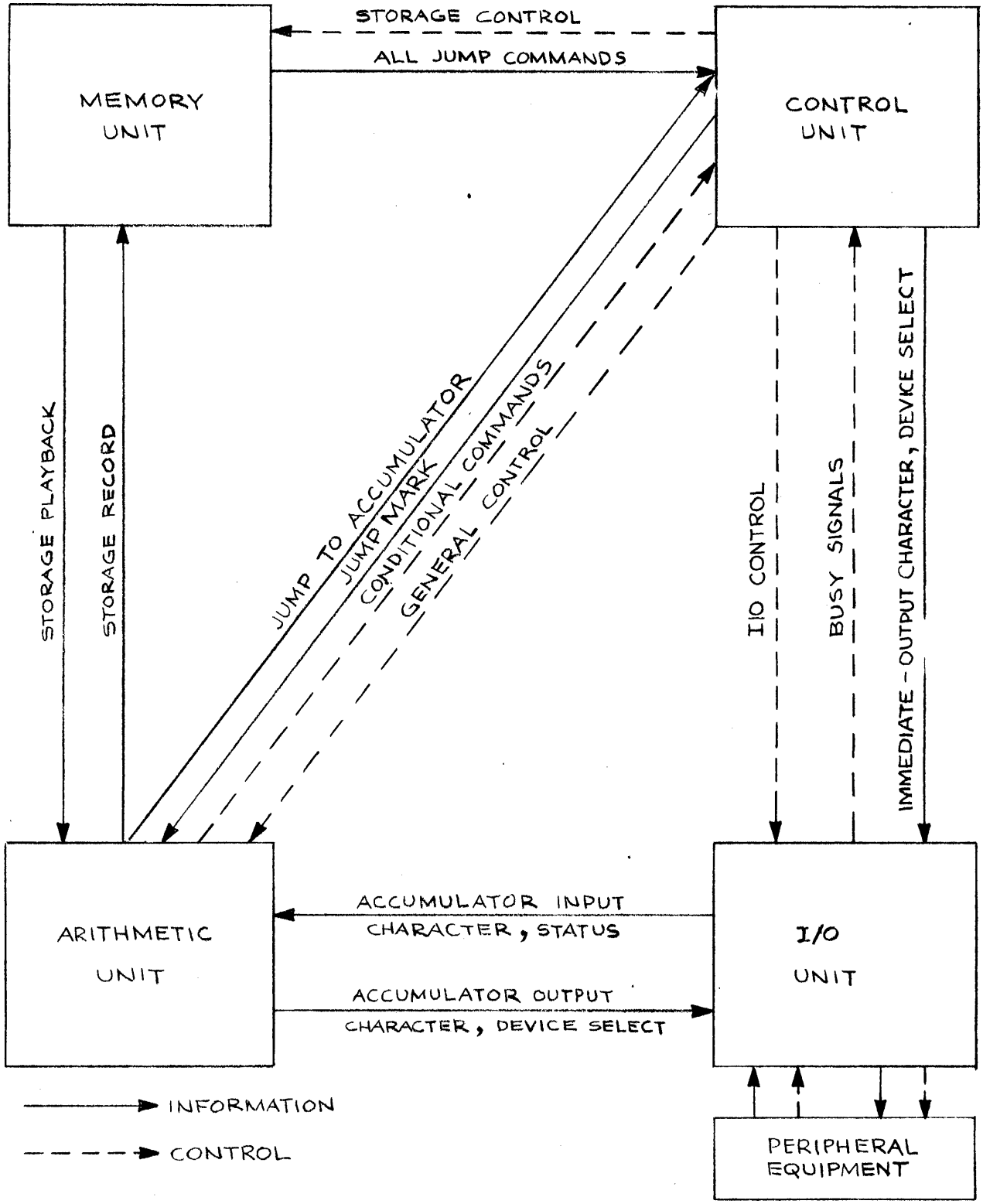


Figure 1.1 EBS 1601, Block Diagram

each of the 128 words per track is referred to as a sector of that track. Thus, there are 128 sectors, numbered 0 through 127 in ascending order around the drum, per track of general storage. The location of each of 4096 general storage sectors is defined by a distinct 3-digit binary-coded hexadecimal address. However, only 4088 of the total 4096 general storage sectors are useable because the addresses (000 through 007) of the first 8 sectors of general storage track 0 are decoded by the processor to specify instead, sectors 0 through 7 of the scratchpad track. Thus, sectors 0 through 7 on general storage track 0 are not useable by the processor. Starting, then, with sector 8 on general storage track 0, the binary-coded hexadecimal track-sector addresses for general storage are 008 through FFF.

In order to convert a binary-coded hexadecimal track-sector address, such as FFF, to a decimal track and sector location, use table 1.1 in the following manner:

DECIMAL-BINARY-HEX CONVERSION TABLE

Decimal	Binary	Hex	Decimal	Binary	Hex
0	0000	0	8	1000	8
1	0001	1	9	1001	9
2	0010	2	10	1010	A
3	0011	3	11	1011	B
4	0100	4	12	1100	C
5	0101	5	13	1101	D
6	0110	6	14	1110	E
7	0111	7	15	1111	F

Table 1.1 Decimal to Binary to Hexadecimal Conversion Table

Each of the 3 hexadecimal address digits is converted to its binary equivalent (FFF = 1111 1111 1111). The 5 high-order bits of the binary equivalent are grouped together to form a single binary number (11111). The decimal equivalent of this number is the general storage track number (11111 = 31, note that general storage track 31 is the last, or 32nd, general storage track since the tracks are numbered 0 through 31). The 7 low-order bits are grouped together to form a second number, the sector location number (1111111 = 127, note that since the first sector of a track is sector zero, the 128th sector of a track is sector 127). The sector addressed by FFF is the last sector on the last track of general storage.

The selection of any one of the 32 general storage tracks is virtually instantaneous, but a specific sector on a track is available only once per drum revolution. Since it takes 5.12 milliseconds per drum revolution (at a nominal drum speed of 11,900 RPM), the average access time to a sector is 2.56 milliseconds.

At 5.12 milliseconds per drum revolution, each word is 40 microseconds long. This time is called a word-time. Similarly, the time of each bit, 1 microsecond, is called a bit-time.

1.3.2 SCRATCHPAD LOOP

The scratchpad storage area (also known as "fast access area") of the drum consists of a single track, or loop around the drum. Unlike general storage, which uses one combination record/playback head per track, the scratchpad track has 2 separate heads, one for record and one for playback. The scratchpad heads are spaced around the track so that 319 bits can be stored on the track area between the two heads, going in the direction of record to playback. In addition to the 319 bits on the track, the scratchpad playback circuit contains a 1-bit delay flipflop which extends the scratchpad into a 320-bit or 8-sector recirculating loop. Under certain conditions, however, the 1-bit delay flipflop can be bypassed to allow a 1-bit early playback of scratchpad information.

Since the scratchpad requires the use of about 1/16 of its track at any given time, access to any one of its 8 sector takes an average of only 0.16 milliseconds, compared to an average general storage sector access time of 2.56 milliseconds. As discussed in paragraph 1.3.1, addresses of the 8 scratchpad sectors run from 000 to 007. The timing relationship between the scratchpad and general storage is designed so that a scratchpad sector is available for use whenever a general storage sector having the same 3 low-order binary address bits is present. For instance, scratchpad sector 007 (binary 0000 0000 0111) is available for use whenever general storage sectors 00F (binary 0000 0000 1111), 017 (binary 0000 0001 0111), 01F (binary 0000 0001 1111), 027 (binary 0000 0010 0111), ..., FFF (binary 1111 1111 1111) are available.

1.3.3 BLOCK INTERCHANGE LOOP

The block interchange loop consists of a single track around the drum and uses separate heads for record/playback operations, similar to the scratchpad. The block interchange loop combined with its playback flipflop contains 320 bits or 8 words. Unlike the scratchpad, the 8 words of the block interchange loop are not contained in individually addressable sectors. They can only be used, via the Block Interchange command, as a single block of information to be interchanged with the entire 8-sector contents of the scratchpad.

1.3.4 MASTER TIMING TRACKS

The master timing track section of the drum contains 3 tracks. They are the Z1 master clock track, Z2 sector index clock track, and Z3 sec-

tor address track. The information on each of the master tracks is factory recorded. The tracks are, of course, playback-only.

The Z1 master clock track is used to produce the basic bit timing pulse of the processor. This timing pulse is used to sequence information through the processor, and defines a 1-microsecond bit-time. The sector index clock track is used to produce 3 timing pulse signals. One signal is used to define the end of a sector and the beginning of the next sector. The other 2 signals are used to define various parts of a sector. The sector address track contains the 7-bit address of each sector (0 through 127) on the drum. By comparing this address to the storage address being located, it can be determined if the next sector available for use on the drum is the desired location. The sector address track is also used to produce an index pulse which defines the first word of the scratchpad and block interchange loops.

1.4 SPARE TRACKS

Within each of the 4 storage areas on the drum there are spare record-playback heads and tracks. The spare heads and tracks are provided for use in the event of a head or track failure. Of special importance are the spare master tracks which contain factory recorded duplications of the original master tracks. The use of spare heads and tracks is discussed in Chapter 5.

1.5 REGISTERS, 8- AND 16-BIT COMMANDS

In addition to the drum storage mentioned in the above paragraph, the EBS 1601 contains 6 special flipflop registers. Each is listed below along with the number of bits contained in the register. The abbreviation used in this manual for each register is enclosed by parentheses.

Command Register	- 8 Bits (CR)
Instruction Register	- 40 Bits (I)
Accumulator Register	- 40 Bits (A)
Buffer Register	- 8 Bits (B)
Carry Register	- 1 Bit (K)
Parity Failure Register	- 1 Bit (P)

1.5.1 COMMAND REGISTER

The 8-bit command register (CR) is made up of flipflops F8 through F1. The arrangement of the 8 bits from left to right, high to low order, is as follows:

F8 F7 F6 F5 F4 F3 F2 F1

The CR is divided into 2 binary tetrads, F8F7F6F5 and F4F3F2F1, the contents, or numeric value, of each can also be expressed hexadecimally. For example, if the binary contents of the command register is 0111 1100, the CR is said to contain hex 7C, see table 1.1.

As mentioned in paragraph 1.1.2 the commands of the 1601 may be either 8 or 16 bits. When the CR contains an 8-bit command, the high-order tetrad always contains the basic operation code. The low-order tetrad contains a modifier to the basic operation code, as in the case of the Test for Zero command (binary 0001 0001, hex 11), Jump to A command (binary 0000 1101, hex 0D), etc. The low-order 3 bits of the low-order tetrad, F3F2F1, may contain as a modifier the address of a scratchpad sector, as in the case of the Test Equal command (binary 0011 0sss where s = sector address bits, hex 30+S where S = scratchpad sector address).

The Halt command (binary 0000 0XXX, hex 00+X) is a unique 8-bit command since the state of the 3 low-order bits (X) has no affect on the command. These bits are used only to identify the various Halt commands of a given program on the REGISTER DISPLAY indicator lights.

When a 16-bit command is to be executed, the CR contains only the 2 high-order tetrads of the command. The low-order 2 tetrads are contained in the high-order 8 bits of the I. The high-order tetrad of the CR contains the basic operation code of the commands. The low-order tetrad of the CR contains a modifier to the basic operation code. The 2 tetrads in the high-order 8 bits of the I also contain modifiers. An example of this is the Read Status command (binary 0101 0000 in the CR and binary 1000 0000 in the high-order 8 bits of the I, expressed hexadecimally as 5080). The low-order tetrad of the CR may contain as a modifier the high-order 4 bits of a 5-bit storage track address. The low-order track address bit is contained in the high-order bit of the I. The remaining 7 bits of the high-order 8 I bits contain the address of a sector on the track addressed by the other bits. An example of this is the Add command where the CR and 2 high-order tetrads of the I are as follows:

```
1001 tttt tsss ssss
  CR    High-Order 2 Tetrads of the I

          s = sector address bits
          t = track address bits
```

If the Add command is addressed to use the contents of sector 24 on track 19, for example, then the command would appear in binary as:

```
    CR       High-Order 2 Tetrads of the I
1001 1001  1001  1000

                    Sector 24 Address

                    Track 19 Address
```

Hexadecimally, the Add command is expressed as 9000+M, where M equals the 3 digit hexadecimal track-sector storage address. In the case of the Add command using the contents of sector 24 on track 19, M would equal 998 (the conversion of the binary track-sector address to hexadecimal is described in paragraph 1.3.1) and the Add command would be expressed as 9998, since 9000+998 = 9998.

Shift commands, both binary and decimal, fall into a special category in that they contain modifiers which specify the number of shifts to be performed by the command. All shift commands are 16-bit commands. They are used to shift data, within the accumulator or scratchpad, to the right or left a specified number of digits. The number of digits shifted is called the shift count. This is specified in the command by a number N which is one less than the shift count. For example, to shift 8 digits, N must equal 7. N cannot equal a number less than zero. Therefore, a shift of zero digits is not allowed since when N equals zero (the smallest number it can equal) a shift of 1 digit takes place. The largest number N can be is 127, which means the largest shift that can take place is 128 digits. Using the Binary Left Single Shift command as an example, the CR and 2 high-order tetrads of the I are as follows:

```
0100 0000  ONNN NNNN
   CR      High-Order 2 Tetrads of the I
```

If, for example, a shift count of 33 is called for, N would equal 32 (which equals binary 0100000) and the command would appear as:

```
0100 0000  0010 0000
   CR      High-Order 2 Tetrads of the I
```

The process of shifting is performed by successive 1-digit shifts. After each 1-digit shift is performed, N is reduced by 1 until N equals zero at which time one more 1-digit shift is performed to complete the execution of the command. After this shift is performed, the high-order 2 tetrads of the I are filled with 1's. The following is an example of a Binary Left Single Shift command with a shift count of 6. (The Binary Left Single Shift command shifts the contents of the A left the number of times specified by the shift count.)

CR High-Order 2 I Tetrads	A
	Initial state prior to execution of command (N=5)
0100 0000 0000 0101	00000000000000000000000000000000000000000001
	After first 1-digit shift is performed (N=4)
0100 0000 0000 0100	00000000000000000000000000000000000000000010
	After second 1-digit shift is performed (N=3)
0100 0000 0000 0011	00000000000000000000000000000000000000000100
	After third 1-digit shift is performed (N=2)
0100 0000 0000 0010	00000000000000000000000000000000000000001000
	After fourth 1-digit shift is performed (N-1)
0100 0000 0000 0001	00000000000000000000000000000000000000010000
	After fifth 1-digit shift is performed (N=0)
0100 0000 0000 0000	00000000000000000000000000000000000000100000
	After sixth 1-digit shift is performed (execution of command completed)
0100 0000 1111 1111	00000000000000000000000000000000000001000000

Hexadecimally, the Binary Left Single Shift command is expressed as 4000+N, where N equals a 2-digit hexadecimal number which equals the shift count minus one. For example, if the shift count is to be 40, hexadecimal N equals 28 (decimal to hexadecimal conversion is shown in the appendix at the end of this manual) and the command would appear as 4028, since 4000+28 = 4028.

During a binary shift, the data specified in the command is shifted, according to the shift count, 1 bit at a time in the direction specified. Following a binary shift, the K contains the last bit shifted out of the affected register. During a decimal shift, the specified data is shifted decimally as directed. This is equivalent to multiplying (left shifts) or dividing (right shifts) by 10, depending on shift direction. For decimal right shifts, K will be reset to 0. K is reset to 0 for decimal left shifts if:

$(R)10^c < 2^b$ Where:

- b = Bit size of register or block of information shifted (either 40 or 80)
- c = Shift count
- R = Contents of register or block of information prior to execution of command.

At all other times, K is unpredictable. A decimal left shift should not be attempted if: $(R)10^{c} \geq 2^{b}$.

1.5.2 INSTRUCTION REGISTER

The instruction register I is a 40-bit (10 tetrad) register. Each of the 40 bits is assigned a position number, 39 through 0. Left to right the bits descend from high to low order. The I is used collectively with the CR to form a 48-bit control loop which processes, one at a time, the instruction words of the stored program. Basically, the control loop functions as follows: An instruction word is transferred from storage into the I under the control of a jump command contained in the CR. The I is then used to supply the CR with the 8- and 16-bit commands contained in the instruction word. The 2 low-order tetrads of a 16-bit command are left in the high-order 2 tetrads of the I when a 16-bit command is executed since the CR can only contain 8-bits. After the commands of an instruction word are used up, another instruction word is transferred into the I from storage under the control of a jump command. Thus, the control loop processes, one at a time, all the instruction words of the stored program. (This operation is discussed in greater detail in Chapter 3.)

1.5.3 ACCUMULATOR REGISTER

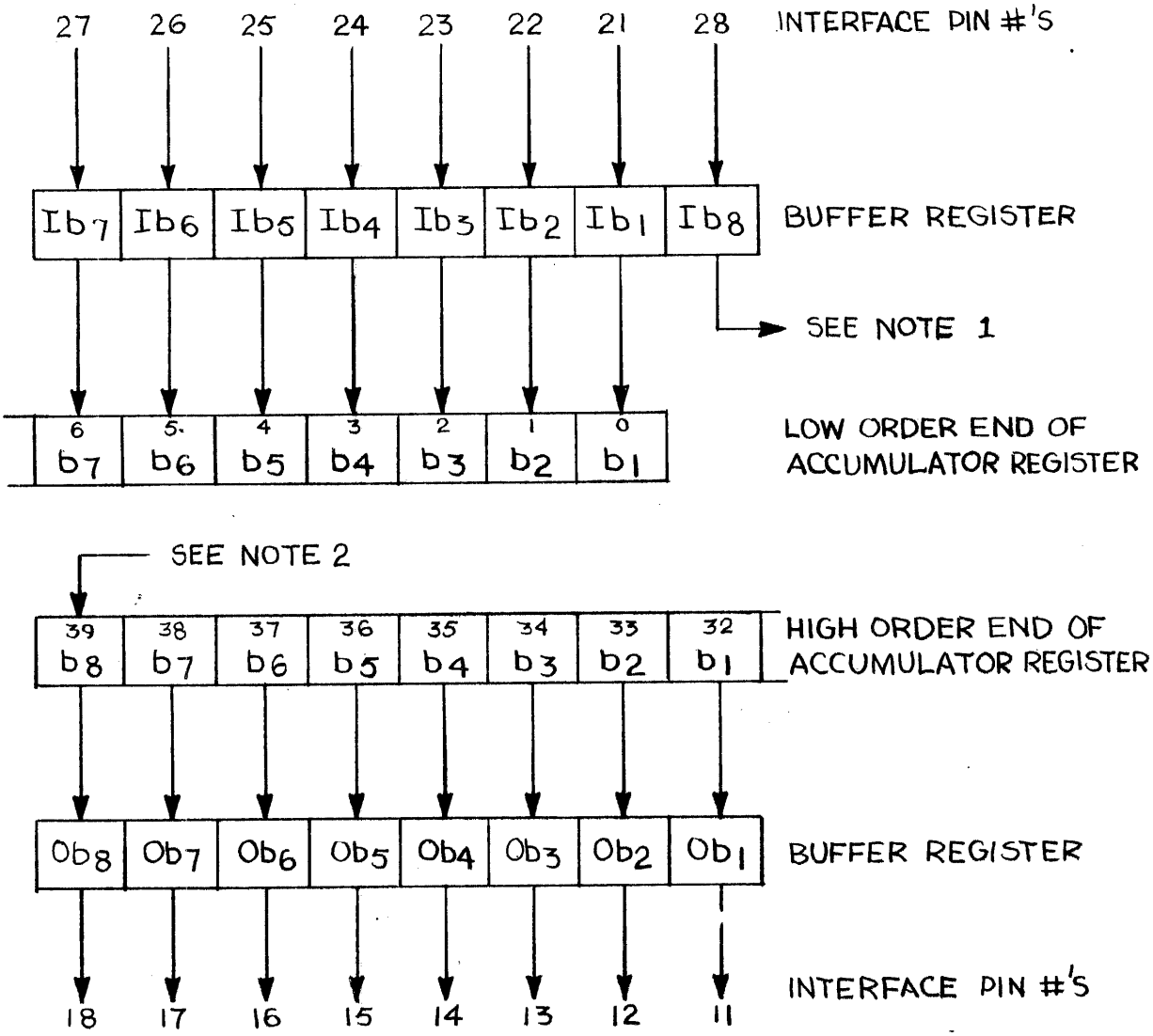
The accumulator register A is a 40-bit (10 tetrad) register used to hold operands or data, as well as to maintain arithmetic results. Like the I, the 40 bits of the A are assigned position numbers 39 through 0, high to low order. The A is available for use every word-time, and about 2/3 of the processor's commands involve the use of it. The low-order bit position of A, bit position 0, is bypassed during the execution of some commands to allow a 1-bit early playback of the A.

1.5.4 BUFFER REGISTER

The buffer register B is an 8-bit (2 tetrad) register used for storing I/O and other data in transit. It serves all standard 8-bit I/O devices via the 1966 Standard 27 Wire Interface.

Loading and unloading the B with information from and to the I/O devices is done all at once in a parallel-shift manner. Loading the B from the A and I (the only two registers in the processor which can do so) is done bit-by-bit in a serial-shift manner. Unloading the B to the A (the only register in the processor which can directly receive the contents of the B) is also done in a serial-shift manner.

The 8 input bits are denoted Ib1 through Ib8. In order of most to least significant, the bits are Ib7, Ib6, Ib5, Ib4, Ib3, Ib2, Ib1, Ib8. The 8 output bits are denoted Ob8 through Ob1, in order of the most to least significant bit. The labels b8 through b1, in both cases, correspond to USASCII bit designations. The 8 input bits may represent an 8-bit character, status data, or a 7-bit character plus parity bit. What the bits represent is determined by the type of input command being executed. Similarly, the 8 output bits may represent an 8-bit character, a device select code, or a 7-bit character plus parity bit, depending upon the type of output command being executed. When a parity bit is called for, it always appears in Ib8 for input and Ob8 for output. The remaining 7 character bits are Ib7 through Ib1 and Ob7 through Ob1, respectively, in descending order of significance. Figure 1.2 shows the flow of a 7-bit character plus parity bit from the interface through the B to the A, and from the A through the B to the interface. Note the orientation of the I/O bits. It should be remembered that Ib8 is the least significant input bit, whereas Ob8 is the most significant output bit. The figure is not intended to show the actual parallel and serial shifting of bits that occurs in the processor.



NOTES:

1) Ib8 used only for parity checking purposes; afterwhich it is discarded.
2) Processor-generated parity bit.

Figure 1.2 7-Bit Input-Output Character Plus Parity Bit Flow Diagram.

Figure 1.3 shows the flow of an 8-bit input character or input status data from the interface through the B to the A, and flow of an 8-bit output character or device select code from the A through the B to the interface.

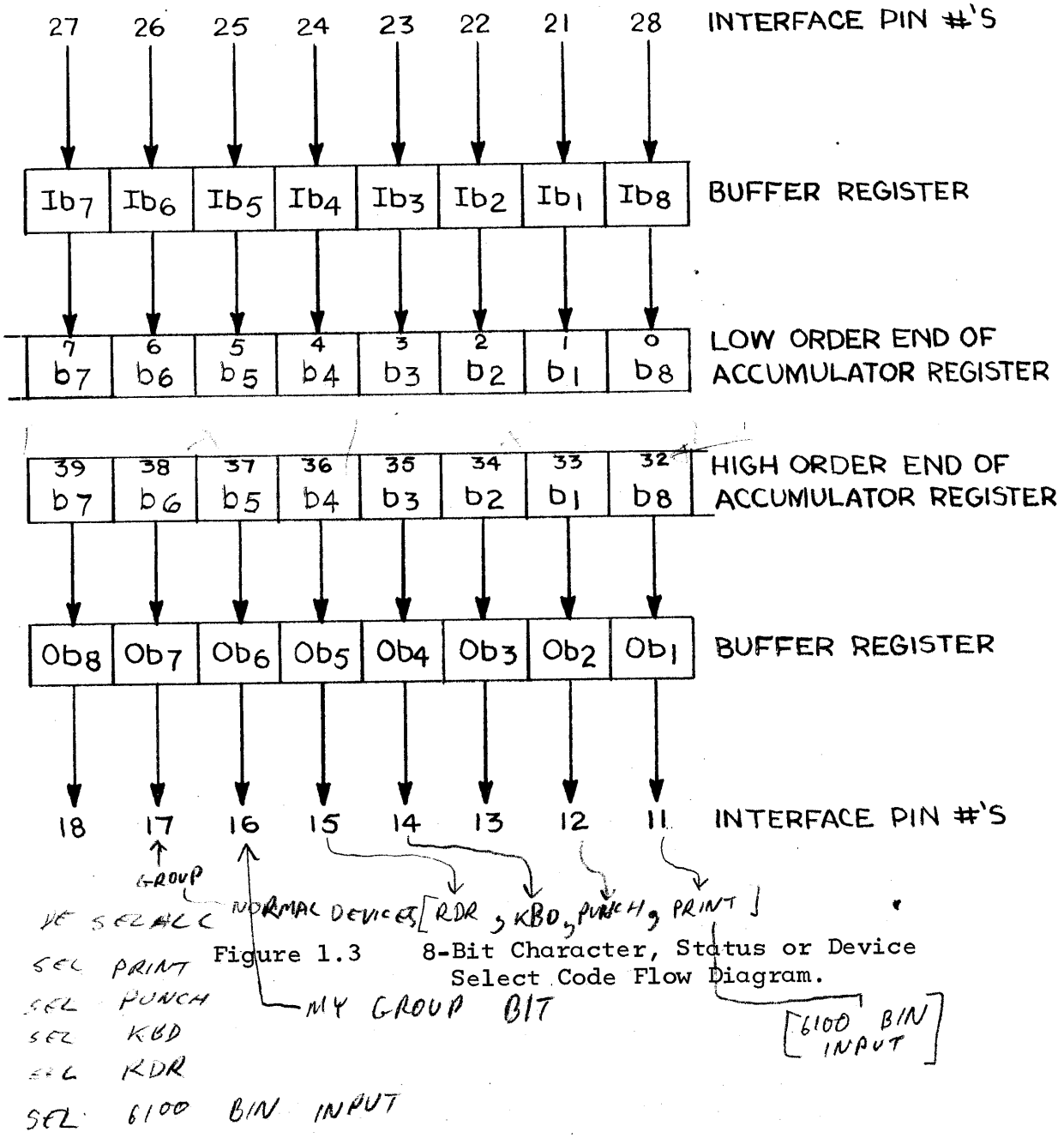


Figure 1.3 8-Bit Character, Status or Device Select Code Flow Diagram.

Rev. 1MAY69

1.5.5 CARRY REGISTER

The carry register K is a 1-bit register made up of flipflop F14. The K has 2 functions; it performs the carry and borrow operation for the adder/subtractor, and is used at other times as a control register in that it stores the fact of whether or not certain commands are to be executed or not executed (aborted). In this case when K = 1 the command is executed, when K = 0 the command is aborted. The following is a list of those commands which affect the content of the K.

All Add Commands
All Select Commands
Block Interchange Command
All Binary Left Shift Commands
All Binary Right Shift Commands
All Clear, Input Commands
Complement Command
All Decimal Left Shift Commands
All Decimal Right Shift Commands
Logical And Command
All Output Commands
Reset K to 0 Command
Read Status Command
Shift Input Command
Set K to 1 Command
All Test Commands

Listed below are those commands that do not affect the content of the K.

Clear and Add Command
Clear A Command
Halt Command
All Jump Commands
No-Operation Command
Store Command
Exchange Command
Extract Command

1.5.6 PARITY FAILURE REGISTER

The parity failure register P is a 1-bit register made up of flipflop F12. The P stores the fact of whether or not a parity error (failure) has occurred during the execution of any of the following commands:

Clear, Input, Check Even Parity command (5840)
Clear, Input, Check Even Parity Into A command (5C40)
Clear, Input, Check Odd Parity command (5800)
Clear, Input, Check Odd Parity Into A command (5C00)

If a parity error is detected during the execution of any of the above commands, P is set to 1. Once the P has been set, it can only be reset to zero by the execution of a Test Parity Failure command (14) which records the state of the P into the high-order A bit, 39, and then resets the P to zero.

NOTE

The P may be set to 1 during the execution of a Shift Input command (5000) depending upon the input data and the contents of the A.

1.6 SIGNAL CONVENTIONS

The following signal conventions are used repeatedly in the following chapters of this manual. Since common words like these are frequently subject to different interpretations, they are hereby firmly defined.

Logical "1"	Approximately equal to +5 volts (Chapter 4 contains exact values) for all signals except those connected directly to and from the 1966 27 Wire Standard Interface; approximately ground potential for all signals connected directly to and from the 1966 27 Wire Standard Interface.
Logical "0"	Approximately equal to ground potential (Chapter 4 contains exact values) for all signals except those connected directly to and from the 1966 27 Wire Standard Interface; approximately -10 volts for all signals connected directly to and from the 1966 27 Wire Standard Interface.
Logical OR Function	The logical OR function is denoted by the letter "v" between 2 signals, e.g., F13 v D19.
Logical AND Function	The logical AND function is denoted by a space between 2 signals, e.g., F19 D19.
SET	Either the state of a logical "1" signal or a true condition, or the action of making it so.
RESET	Either the state of a logical "0" signal or a false condition, or the act of making it so.

REAL Signal	The signal which is a logical "1" when the basic defining action or state is true. When the real signal is a logical "1", the prime signal is a logical "0" and vice versa. The real signal is indicated by the absence of a null bar over a signal, e.g., F13.
PRIME Signal	The signal which is a logical "0" when the basic defining action or state is false. A prime signal may electronically exist without a real signal, and vice versa. The prime signal is represented by the presence of a null bar over a signal, e.g., $\overline{F13}$.

1.7 LOGIC DIAGRAM CONVENTIONS

The symbols used in the numerous logic diagrams which appear in this manual are in accordance with the ABS Logic Symbol Guide. For reference purposes, figure 1.4 shows the logic symbols used in this manual. The logical equation and/or other pertinent data for these symbols is given below. For additional information, refer to Chapter 4, Circuits.

AND Gate	$D = A\ B\ C$
NAND Gate	$C = \overline{A} \vee \overline{B}$
NOR Gate	$D = \overline{A}\ \overline{B}\ \overline{C}$
Expanded NOR Gate	$F = \overline{A}\ \overline{B}\ (\overline{C} \vee \overline{D}) = \overline{A}\ \overline{B}\ \overline{E}$
Amplifier, Inverting and Non-Inverting	Whenever a signal is amplified and not inverted its designation, if one is used, is increased by 100, e.g., F13 amplified becomes F113. Whenever a signal is amplified and inverted its designation, if one is used, has a null bar over it if the input signal does not, otherwise vice versa. The output designation is increased by 100 if it has already been used elsewhere, otherwise it is not. For example, F13 amplified and inverted becomes F13 if the designation "F13" is not used elsewhere, otherwise it becomes $\overline{F113}$.

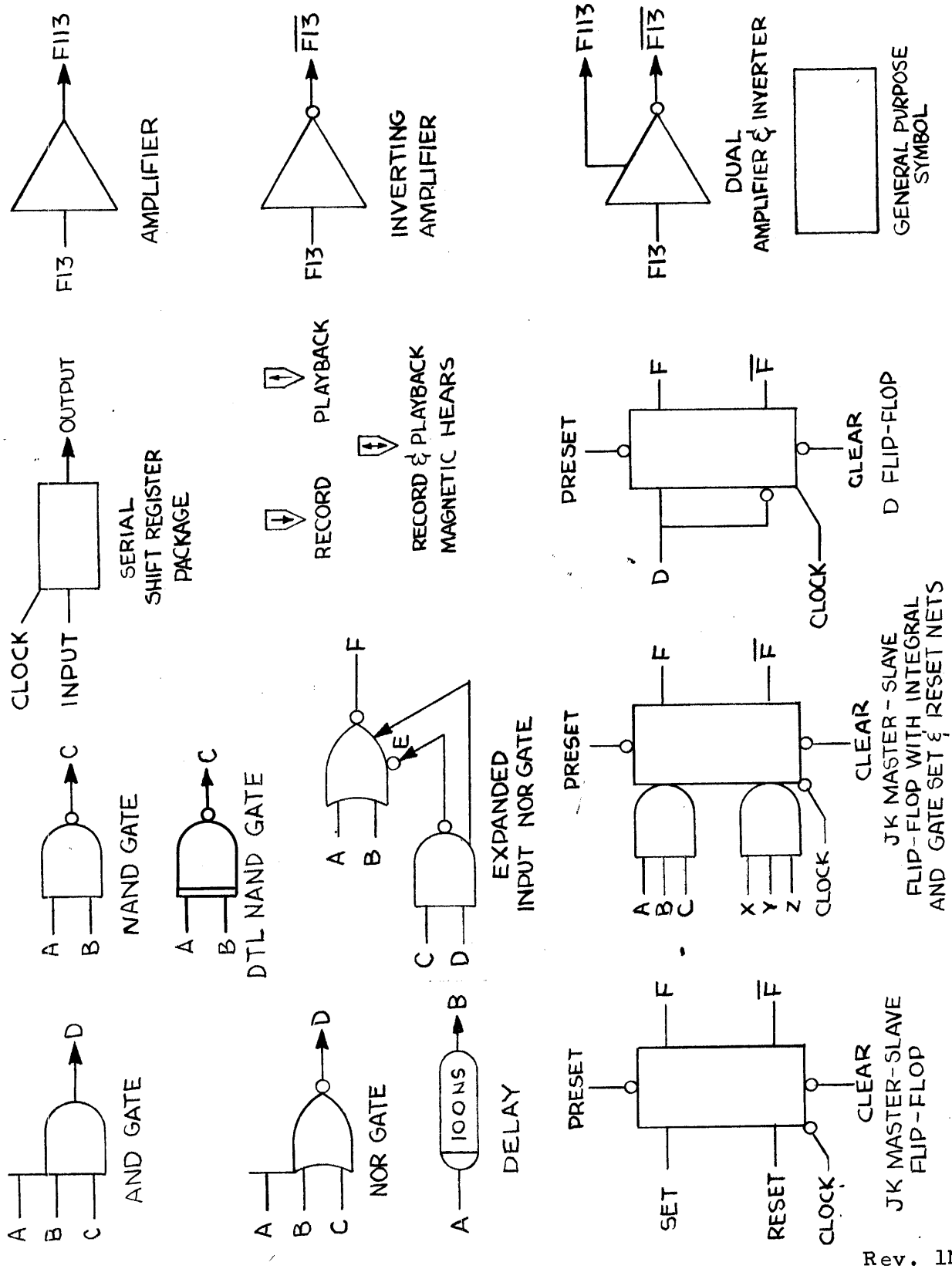


Figure 1.4 Logic Diagram Symbols.

Serial Shift Register Package

All serial shift register packages are the same type. They store a maximum of 8 bits. The register shifts 1 bit per clock pulse.

Magnetic Heads

The arrow inside the magnetic head symbol indicates the type of head; i.e., record, playback, or record-playback.

JK Master-Slave Flipflop

This type of flipflop works on the master-slave principle, described in the 4 steps below. Entry into the master section from the set and reset inputs is controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master (lower positive edge of clock pulse).
2. Enter information from inputs to master (upper positive edge of clock pulse).
3. Disable inputs (upper negative edge of clock pulse).
4. Transfer information from master to slave (lower negative edge of clock pulse).

Preset and clear are independent of clock; both operation on a logical 0.

JK Master-Slave Flipflop with Integral AND Gate Set and Reset Nets

This type of flipflop is identical to the one mentioned above except that it has 3 input AND gates in place of the single inputs, set and reset. All inputs to the AND gate must be active (logical 1) for the flipflop to change state.

D Flipflop

This type of flipflop is edge-triggered. Input is via a single input, and input information is transferred to the outputs on the positive edge of the clock pulse. Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; afterwhich the input is locked out. Preset and clear are independent of clock; both operate on a logical 0.

General Purpose Logic Symbol	This symbol is used whenever a circuit cannot be represented by any of the other logic symbols. The function of a general purpose logic symbol is written inside the symbol.

Each of the printed circuit boards of the processor is assigned a letter designation. The components on each printed circuit board are divided into row and columns on any one board. In cases where a board is small and division impractical, the board is not divided.

Within most of the logic symbols there are 2 identification designations. Such symbols represent IC packages. The lowermost designation is in the form of a single number followed by a single letter. The letter indicates on which of the printed circuit boards the IC package is located, while the number indicates either the row or column of the printed circuit board in which the IC package is to be found. The uppermost designation within the logic symbol is the IC package designation. It serves 2 purposes. First, since it is printed on the component side of the printed circuit board, next to its associated IC package, it can be used to find a given IC package along the row or column specified by the lowermost logic symbol designation. Second, the IC package designations are referenced in Chapter 4 to the circuits which they represent.

1.8 FLOW CHART CONVENTIONS

Included as part of the Chapter 3 explanation of each processor command is a flow chart. The symbols used in these flow charts are shown in figure 1.5. They consist of 3 basic types; a circle, square, and a rectangle. Circles have either a dot or a "v" in their center. The dot indicates the circle is performing the logical AND function; the "v" indicates the circle is performing the logical OR function. Squares represent flipflops. Flipflops are drawn with only one input and one output which represent the input and output of interest at that particular time. Rectangles are used to represent all other functions. Symbols are connected together by either solid or broken lines. The solid line is used to indicate information flow and a setting action to a flipflop or gate. The broken line is used only to indicate a resetting action to a flipflop. Direction of travel along lines is indicated by arrow heads. Different cycles of the processor's operation are separated from one another by solid vertical lines. Time in each cycle progresses from left to right (i.e., the leftmost part of a cy is the beginning, the rightmost part the end). A signal produced in one cycle can be used in another cycle without having its signal line pass from one cycle to the other. A signal must be generated to advance the processor from its present cycle of operation to its next cycle of operation. This signal is given the name of the next cycle of operation and its line usually passes from the present to the next cycle of operation. Unless otherwise specified on the individual flow charts, all cycles shown are within the processor's two active modes of operation -- M2 and M3.

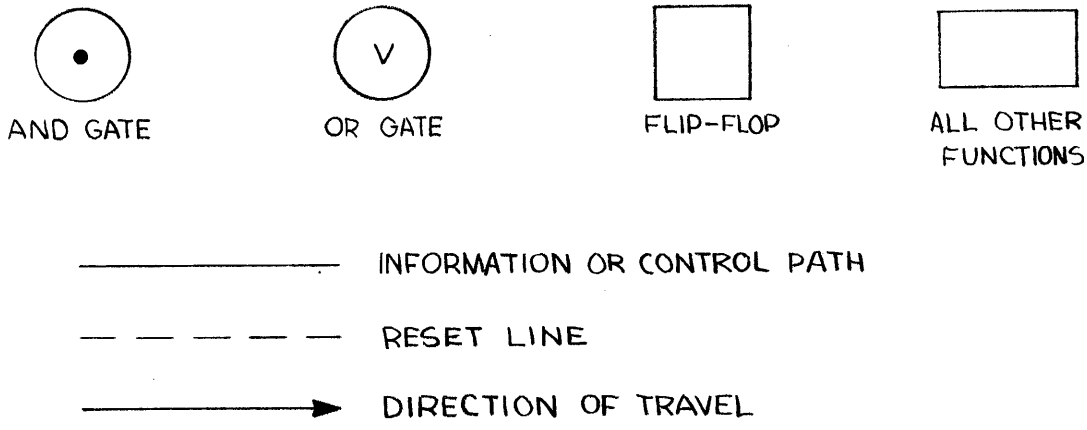


Figure 1.5 Flow Chart Symbols.

CHAPTER 2

OPERATING CONTROLS & INDICATORS

CHAPTER 2. OPERATING CONTROLS AND INDICATORS

2.1 INTRODUCTION

The EBS 1601 has 16 operator controls and 16 indicator lights, located on the EBS 1601 operator console. Figure 2.1 shows the EBS 1601 operator console. Below is a list of the controls and indicators.

1. POWER On-Off Indicator Light
2. POWER On-Off Button
3. READY Indicator Light
4. READY Button
5. RUN Indicator Light
6. RUN Button
7. HALT Indicator Light
8. HALT Button
9. Reset (R) Carry Flipflop Button
10. Carry Flipflop (K) Indicator Light
11. Set (S) Carry Flipflop Button
12. TRACK Flipflop F9 Indicator Light

13 through 28. REGISTER DISPLAY Controls and Indicator Lights from right to left are as follows:

13. Command Register Bit 0 Indicator Light
14. Set Command Register Bit 0 Button
15. Command Register Bit 1 Indicator Light
16. Set Command Register Bit 1 Button
17. Command Register Bit 2 Indicator Light
18. Set Command Register Bit 2 Button
19. Command Register Bit 3 Indicator Light
20. Set Command Register Bit 3 Button
21. Command Register Bit 4 Indicator Light
22. Set Command Register Bit 4 Button
23. Command Register Bit 5 Indicator Light
24. Set Command Register Bit 5 Button
25. Command Register Bit 6 Indicator Light
26. Set Command Register Bit 6 Button
27. Command Register Bit 7 Indicator Light
28. Set Command Register Bit 7 Button

29. Reset (R) Command Register Bits 0 through 7 Button
30. REGISTER SELECT Switch
31. ACCUMULATOR Register Half of REGISTER SELECT Switch Indicator Light
32. INSTRUCTION Register Half of REGISTER SELECT Switch Indicator Light

2.2 POWER BUTTON AND INDICATOR LIGHT

The POWER button, when depressed, causes its indicator light and the STEP indicator light to light. All power to the processor is turned on, and a short warm-up period follows. During the warm-up, an Inhibit signal is from the processor, via the interface, to the peripheral devices to block their operation during the processor warm-up. At the end of the warm-up period, a Jump Conditional command to address FFF is forced into the control loop and the K is set. Following the depression of either the RUN or HALT button, the jump to FFF is performed and control is transferred to the last sector of the last general storage track, which normally contains the start of the OPUS program (described in the 1600 Programming Manual).

When power is on, the POWER button may be used to turn off the power to the processor. All indicators are turned off, and the processor is shut down.

2.3 READY BUTTON AND INDICATOR LIGHT

The READY indicator light lights when the processor is ready to operate, and remains lit during all modes of operation. However, if there is a power failure or a loss of the processor's bit timing clock, the READY indicator light goes out. If the failure was caused by a loss of the bit timing clock or a power failure less than 15 seconds, the READY indicator light remains out after the clock or power is returned to normal (indicated by a lit HALT indicator light). The READY button must then be pressed to return the processor to its ready-to-operate status. It also forces a Jump Conditional command to address FFF and sets K. If the power failure is longer than 15 seconds, the READY indicator light will light upon the return of power after the processor goes through the warm-up period described in paragraph 2.2.

Pressing the READY button when its indicator light is lit, in the automatic mode, has no effect on the processor. If, on the other hand, the processor is in the idle mode (indicated by a lit HALT indicator light), the READY button forces a Jump Conditional in the control loop and sets K.

2.4 RUN BUTTON AND INDICATOR LIGHT

The RUN button is operative only when the READY indicator light is lit and the REGISTER SELECT switch is in a CONTROL position. It initiates automatic processing of the stored-program with the command in the CR. The RUN indicator light is lit when the processor is in the automatic

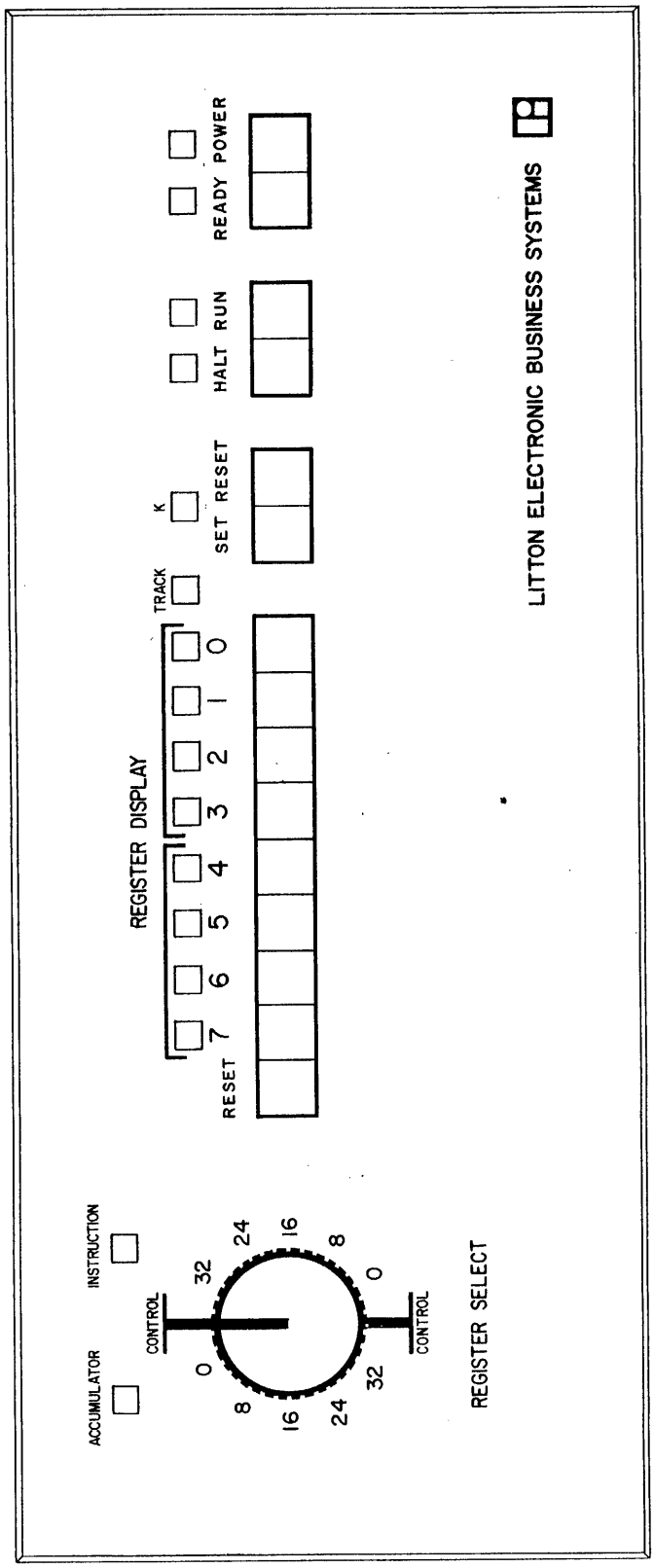


Figure 2.1 EBS 1601 Operator Console.

mode of instruction processing. If the command in the CR when the RUN button is depressed is a Halt command, it is treated by the processor as a No-Operation command so that the next command of the instruction word is executed. Pressing the RUN button when the RUN indicator light is lit has no affect on the processor's operation.

2.5 HALT BUTTON AND INDICATOR LIGHT

The HALT button is only operative when the READY indicator light is lit and the REGISTER SELECT switch is in a CONTROL position. If the HALT button is then pressed while its indicator light is unlit and the RUN indicator light is lit, processor in the automatic mode, causes the automatic processing to halt after executing the command contained in the CR. The HALT indicator light then lights; the RUN indicator light extinguishes. At this point the processor is in the idle mode. Each subsequent depression of the HALT button, while the processor is in the idle mode, causes one command to be executed from the CR. No-Operation commands are skipped.

2.6 CARRY REGISTER (K) CONTROLS AND INDICATOR LIGHT

The K indicator light indicates the content of the K. When lit, K is in the set state (contains a logical 1). When unlit, the carry is in the reset state. The operator can change the state of the K by depressing the set (S) button to force the K to 1, or by depressing the reset (R) button to force the K to 0. These controls are operative only when the processor is in the idle mode (STEP indicator light lit) while the READY indicator light is lit.

2.7 TRACK FLIPFLOP INDICATOR LIGHT

The TRACK indicator light indicates the state of flipflop F9 which is used to store the low order bit of the 5-bit track address. Flipflop F9 is also used, at other times, to store a modifying bit for commands that require it. When the TRACK indicator light is lit, F9 is in the set state; when unlit F9 is in the reset state.

2.8 COMMAND REGISTER CONTROLS AND INDICATOR LIGHTS

There are 8 command REGISTER DISPLAY indicator lights which display the contents of the 8-bit CR. The lights are labeled 0 through 7 to correspond to the order of the CR bits. A lit light indicates the presence

of a logical 1; an unlit light indicates the presence of a logical 0. Directly below each indicator light is a set button which when pressed forces a logical 1 into its bit position. A single reset (R) button is used to force all 8 bits of the CR to logical 0. These controls are operative only when the processor is in the idle mode (HALT indicator light lit) while the READY indicator light is lit.

2.9 REGISTER SELECT SWITCH

The REGISTER SELECT switch is a 12-position clockwise rotary switch. It is used to display the contents of the I and A on the REGISTER DISPLAY indicator lights. In either of the 2 CONTROL positions of the switch, the contents of the CR are displayed on the REGISTER DISPLAY indicator lights and the operator can alter the contents of the CR via the set and reset buttons as described in paragraph 2.8. When the switch is in either CONTROL position both the ACCUMULATOR and INSTRUCTION register indicator lights are unlit. The first 5 positions of the switch, going clockwise from the upper CONTROL position, display successive 8-bit portions of the I, starting from the low-order end and going toward the high-order end. The 5 positions from the lower to the upper CONTROL positions, display successive high- to low-order 8-bit portions of the A. When the I is being displayed the INSTRUCTION register indicator light is lit. When the A is being displayed, the ACCUMULATOR register indicator light is lit. The contents of the I and A can be altered 8 bits at a time when displayed. The REGISTER SELECT switch is operative only when the processor is in the idle mode (HALT indicator light lit) while the READY indicator light is lit. The HALT and RUN buttons are not operative when the REGISTER SELECT switch is not in a CONTROL position.

If the processor goes into the idle mode from the automatic mode while the REGISTER SELECT switch is not in a CONTROL position (only way is via a Halt command) an unwanted command is precessed into the CR when the switch is returned to a CONTROL position. This situation requires the contents of the control loop and possibly the A to be altered by REGISTER DISPLAY buttons in conjunction with the use of the REGISTER SELECT switch to correct this condition. Otherwise, it is necessary to restart the program over again from the beginning.

CHAPTER 3

THEORY OF OPERATION

CHAPTER 3. THEORY OF OPERATION

3.1 MODES AND CYCLES OF OPERATION

3.1.1 GENERAL ANALYSIS

The EBS 1601 has 4 modes of operation defined by the 4 states of mode flipflops M5 and M6 listed below.

$\overline{M5}\ \overline{M6}$ = M0, Stop Mode
$M5\ \overline{M6}$ = M1, Idle Mode
$\overline{M5}\ M6$ = M2, Step Mode
$M5\ M6$ = M3, Automatic Mode

In the automatic mode of operation, instruction words of the stored program are processed one at a time in the control loop under the control of the stored program. In the step mode, instruction words of the stored program are processed one at a time under the control of the operator. The stop mode is the mode through which the processor goes before going into the idle mode. Nothing else is done in the stop mode; all information remains the same. The idle mode is the mode in which there is no program processing. All information within the processor regenerates while it is in the idle mode.

Within each of the 4 modes of operation there are 4 cycles of operation that the processor may go through. Each cycle is defined by one of the 4 states of cycle flipflops C1 and C2 listed below.

$C1\ \overline{C2}$ = C10, 8-Bit Precession Cycle
$C1\ \overline{C2}$ = C20, 8-Bit Precession Cycle
$\overline{C1}\ \overline{C2}$ = C30, Search Cycle
$\overline{C1}\ C2$ = C40, Execute Cycle

Cycles C10 and C20 are 8-bit precession cycles which are used to shift the individual commands of the instruction word held in the I into the CR (precession is discussed in paragraph 3.1.3). All 16-bit commands are followed by both precession cycles, and all 8-bit commands are followed by C20 only, in order to correctly load the CR. The search cycle sets up the conditions necessary to execute the command, locates storage information, and determines if the command is to be executed in certain cases. In the execute cycle, C40, the individual commands of the stored program are carried out.

3.1.2 DETAILED ANALYSIS OF MODES AND CYCLES OF OPERATION

Each of the processor's mode-cycle combinations, shown in figure 3.1, is discussed in the following paragraphs. During this discussion, the REGISTER SELECT switch is assumed to be in a CONTROL position unless otherwise mentioned. Note that there are 3 mode-cycle combinations which are not used by the processor. They are C10M0 (read cycle C10 of mode M0), C10M1, and C40M0. Although it is not labeled, C20M1 is the starting position.

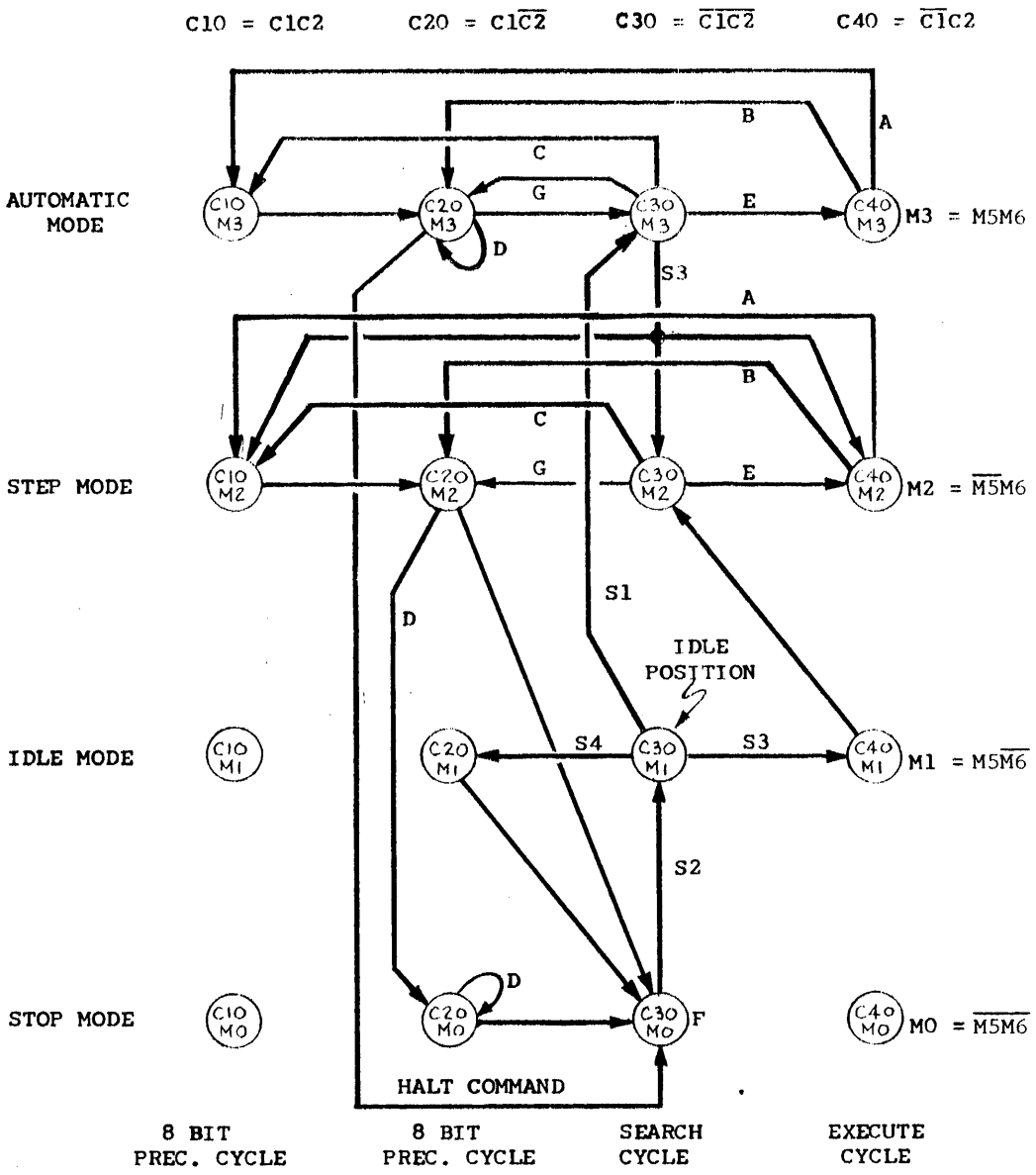
3.1.2.1 Warm-Up

During the warm-up period, the processor is kept in the C20M1 position. After the warm-up period and at the beginning of the next word-time, the processor goes into C30M0. It stays in C30M0 for only one bit-time, after which it is forced into the idle position, C30M1, provided that neither the RUN or STEP button is being pressed. If either button is being pressed, the processor remains in C30M0 until the pressed button is released. The processor then remains in the idle position until either the RUN or STEP button is depressed.

3.1.2.2 Automatic Instruction Processing

In order to start automatic processing of the instructions, the processor must be brought out of the idle position and into the M3 mode. This is done by depressing the RUN button. The processor then goes from the idle position into C30M3 which is the search cycle of the automatic mode. Once in C30M3, automatic instruction processing begins. If all the prerequisites to execution of the command that is in the CR at this time have been met, the processor automatically goes into C40M3, where the command is executed. If a prerequisite to execution is that a storage address be located, the processor stays in the search cycle, C30M3, until this is done. However, when the prerequisite requires that a Busy signal not be present, and a Busy signal is present, the processor is forced into C10M3 for all commands except the Block Interchange command (BI). In case of the BI command, the processor is forced into C20M3. Forcing the processor into C10M3 or C20M3, as the case may be, aborts the command since it is precessed out of the CR before it can be executed in C40M3.

The reason the abort path for the BI command goes to C20M3, instead of C10M3, is that the BI command is only 8 bits long thereby requiring only one 8-bit precession cycle for clearance of the CR. All other commands which can be aborted are 16 bits long and require two 8-bit precession cycles to be cleared from the CR. Hence, they use the abort path to C10M3.



NOTES:
A = 16-bit precession loop; B = 8-bit precession loop; C = abort path; D = no-operation path; E = C30 successful; F = usually in this position for first bit-time of a word; S1, S2, S3, S4 see Signal Glossary, paragraph 3.8; G = abort path for BI command.

Figure 3.1 Modes and Cycles of Operation.

After execution of a command in the M3 mode the processor automatically goes into C10M3 if the command is 16 bits, or into C20M3 if 8 bits. After going through one word 8-bit precession cycle C10M3, the processor always goes through one word 8-bit precession cycle C20M3. At the end of C20M3 the processor automatically goes into search cycle C30M3, unless a Halt or No-Operation command has been precessed into the CR. The presence of either command is detected in the last bit-time of C20M3. A halt command forces the processor into C30M0, where it usually stays for one bit-time before going into idle position C30M1. If either the RUN or STEP button is depressed while the REGISTER SELECT switch is in a CONTROL position, the processor remains in C30M0 until the button is released or the REGISTER SELECT switch rotated out of the CONTROL position. The processor then goes into C30M1. If a No-Operation command is detected instead of a Halt command, the processor recycles through C20M3 until another command is brought into the CR. The processor then goes into C30M1.

3.1.2.3 Modes and Cycles Used for Step (Non-Automatic) Instruction Processing.

There are two paths that bring the processor into the step mode, in which instructions are processed on at a time (non-automatic). One path is from the automatic mode, C30M3, the other is from the idle position, C30M1. If the STEP button is depressed while automatic instruction processing is taking place, the processor goes to one of 3 step mode positions at the end of the first word-time in C30M3. The 3 position are C10M2, C30M2, and C40M2. The processor goes into C10M2 if at the end of C30M3 a 16-bit command is to be aborted. The 8-bit BI command abort path is to C20M2. The processor goes into C30M2 if the first word-time in C30M3 specified a storage address that is not located. The processor goes into C40M2 if after the first word-time in C30M3 a specified storage address is located, or if the command requires only one word-time in C30 and is not to be aborted.

The path taken in going from the idle position to the step mode is via C40M1 to C30M2. The processor stays in C40M1 for one word-time during which nothing happens in way of instruction processing and all information regenerates. Whatever command happens to be in the CR when the processor goes into C30M2 is treated in the same manner as if it were in C30M3 which was described in paragraph 3.1.2.2. In fact the operation of all the other cycles of M2 are the same as the ones described for M3 except for what occurs at the end of the first word-time in C20M2. Whereas C20M3 automatically goes into C30M3, assuming that a Halt or No-Operation command is not decoded; C20M2 automatically goes into C30M0 for one bit-time and then into the idle position for all commands except the No-Operation command. It remains there until either the STEP or RUN button is pressed.

If a No-Operation command is decoded at the end of C20M2, the processor goes into C20MO and recycles through C20MO until another command is brought into the CR. The processor then goes into C30MO for one bit-time before finally going into the idle position.

3.1.2.4 Modes and Cycles Used for Register Display

In order to display the contents of either the I or A without actually executing any of the commands being displayed, it is necessary to stay within the 2 non-active modes of the processor, M1 and MO. Each time the REGISTER SELECT switch is rotated one notch, the processor goes into C20M2 for one word-time and precesses the high order 8 bits of either the I or A, depending upon which half of the switch is being used, into the CR. The REGISTER DISPLAY indicator lights indicate the contents of the CR, thus the necessity of precessing the information to be displayed into the CR. After the information has been precessed into the CR, the precessor goes into C30MO for one bit-time before finally going back to the idle position.

3.1.3 ORDERS PRECESSION

One of the most important aspects of the processor's operation is the means by which commands are precessed, or shifted, into and through the CR from the I. In order to understand this action, it is necessary to first understand the structure of an instruction word, which is held in the I.

Instruction words are the remembered data by which the processor performs a sequential chain of actions in order to carry out the program. Therefore, a stored program must then contain an ordered sequence of instruction words. The 40 bits of each instruction word are divided into two groups; one group of 8 bits and one group of 32 bits. The 8-bit group is a partial address of the next instruction word to be used by the processor. The 32-bit group contains various 8- and/or 16-bit commands. Figure 3.2 shows the different configurations of the instruction word that can be made by using various combinations of 8- and 16-bit commands.

The following paragraphs explain the operation of orders precession. The binary tetrads in the CR and I are represented hexadecimally (hex) in the following text. The individual commands in the I are separated by spaces.

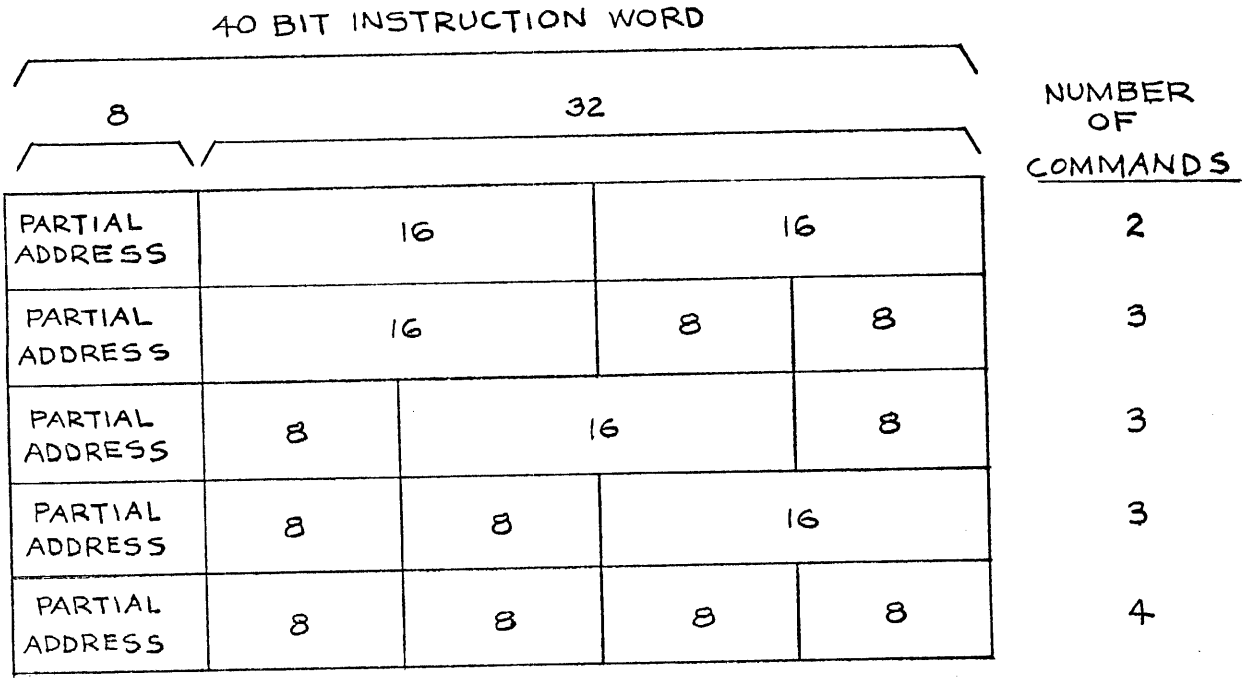


Figure 3.2 Instruction Word Configurations.

An instruction word can only be brought into the I from storage under the control of a jump command in the CR and high-order 8 bits of the I. It should be remembered from paragraphs 2.2 and 2.3 that whenever the processor's power is turned on or the READY button operated, a Jump Conditional command to address FFF is forced into the control loop and K is set. This jump is the starting point of the instruction word processing. The state of the CR and I, prior to execution of the Jump Conditional command, (JU), is shown in figure 3.3.1.

CR	I
EF	FF --------

The dash (-) indicates hex digits of no pertinence.

Figure 3.3.1 Orders Precession

After the execution of the JU command, the CR and I would be as shown in figure 3.3.2, assuming the contents of storage address FFF to be: 01 5840 14 13

CR	I
EF	01 5840 14 13

Figure 3.3.2 Orders Precession

The CR and I are electronically connected together to form a single 48-bit loop. Remember that each hex digit represents 4 binary bits. The information in the loop is shifted one bit right for each bit-time of a word-time. Bits shifted out of the low-order end of the I are shifted into the high-order bit position of the CR, as shown in figure 3.3.3. This results in the information shifting right

CR	I
EF	01 5840 14 13

Figure 3.3.3 Orders Precession

40 bits (10 hex digits). Since the loop contains 48 bits, a shift right of 40 bits does not return the bits to their original position. Instead, they are displaced 8 bits (2 hex digits) to the left of their original position, as shown in figure 3.3.4. It is this process, of shifting the information,

CR	I
Before 40-bit right shift.	
EF	01 5840 14 13
After 40-bit right shift.	
01	5840 14 13 EF

Figure 3.3.4 Orders Precession

which is called "orders precession", or just simply "precession".

Note that at this point the CR contains hex 01, which is a new partial address for the jump command. In order to clear the CR of this information and bring in the next command of the instruction word from the I, a second 8-bit precession cycle must be executed. The CR and I then are as shown in figure 3.3.5.

CR	I
58	40 14 13 EF01

Figure 3.3.5 Orders Precession

The 5840 command is executed, after which it is followed by two 8-bit precession cycles to bring the 8-bit 14 command into the CR. After the 14 command is executed, one 8-bit precession cycle is executed to bring the 13 command into the CR. After the 13 command is executed, one 8-bit precession cycle is executed to bring the EF01 into the CR. At this point all the commands in the instruction word have been executed and the original jump command is back in the CR. This jump command is now referred to as an automatic jump.

Any jump command that is executed and then precessed through the instruction register back into the command register becomes an automatic jump. All automatic jumps are Jump Unconditional commands since Jump Mark commands and Jump Conditional commands are converted, after they are executed, into Jump Unconditional commands.

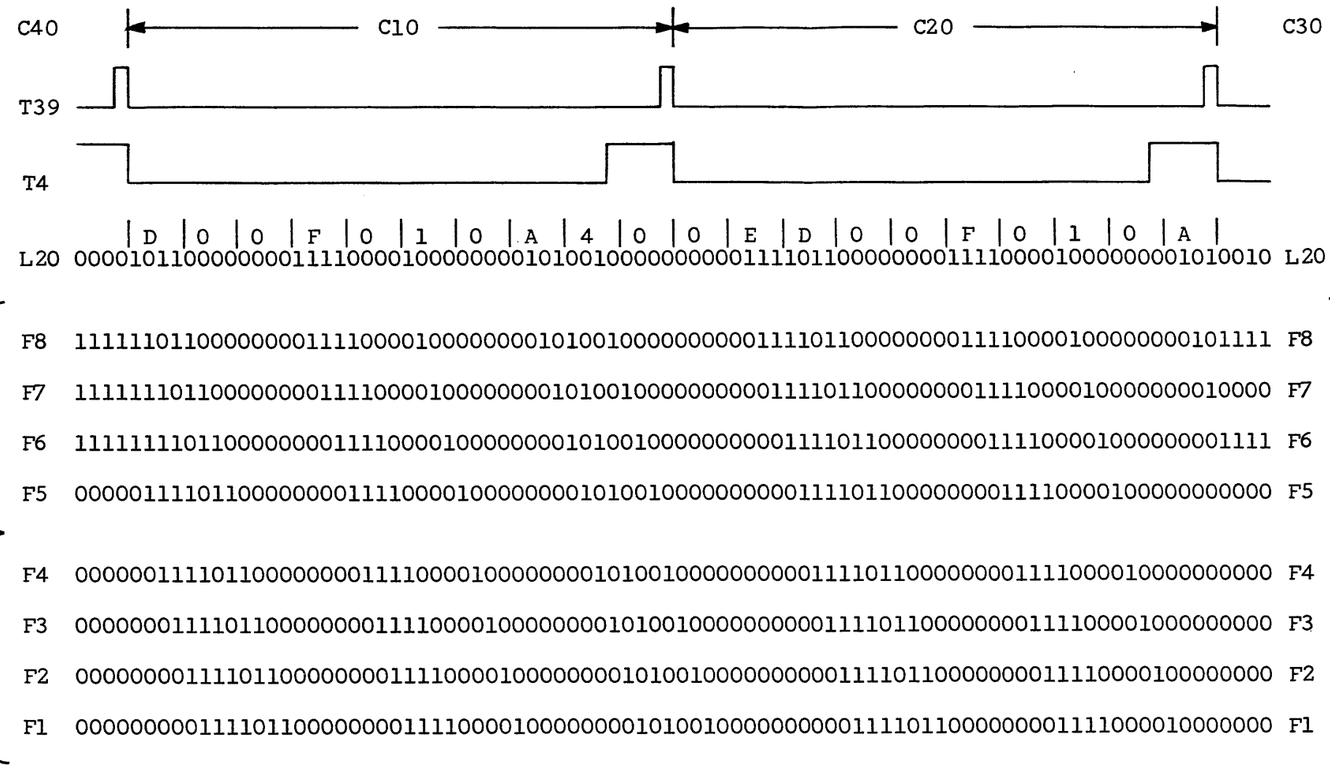
Every instruction word carries with it the 8-bit partial address of the next instruction word to be used. The 8-bit partial address is tagged on to the 4-bit address contained in the automatic jump command. Since the 4-bit address is part of the automatic jump, it is not replaced when the automatic jump command is executed. Therefore, unless a branch occurs in the program, the automatic jump has a choice of only 256 registers since the 8-bit partial address can specify any sector on the track specified by the 4-bit address, or any sector on the next higher track than the track specified by the 4-bit address. If a jump to any sector outside of 256 sector range of the automatic jump is required, a complete 16-bit jump command must be placed in the instruction word. This jump command would then become the new automatic jump if it is processed through the I and back into the CR after being executed, and the same 256 sector restriction would apply to it.

The last paragraph can be summarized by saying that every instruction word carries with it the partial address of the next instruction word. Therefore, the automatic sequencing of the commands within an instruction word can only take place over an area of 256 registers. Finally,

TYPICAL 16-BIT PRECESSION
(8-BIT PRECESSION REQUIRED C20 ONLY)

CR = hex E0 (last command performed)

I = hex 04A010F00D (04 last address used)


C40
C10
C20
C30
T39
T4
| D | 0 | 0 | F | 0 | 1 | 0 | A | 4 | 0 | 0 | E | D | 0 | 0 | F | 0 | 1 | 0 | A |
L20 00001011000000001111000010000000010100100000000001111011000000001111000010000000001010010 L20
E
F8 11111101100000000111100001000000001010010000000000111101100000000011110000100000000101111 F8
F7 11111110110000000011110000100000000101001000000000011110110000000001111000010000000010000 F7
F6 11111111011000000001111000010000000010100100000000000111101100000000011110000100000000001111 F6
F5 00000111101100000000011110000100000000101001000000000011110110000000001111000010000000000000 F5
F4 00000011110110000000001111000010000000010100100000000000111101100000000011110000100000000000 F4
F3 00000001111011000000000111100001000000001010010000000000011110110000000001111000010000000000 F3
F2 00000000111101100000000011110000100000000101001000000000001111011000000000111100001000000000 F2
F1 00000000011110110000000001111000010000000010100100000000000011110110000000001111000010000000 F1
A
0
0
| 0 | E | D | 0 | 0 | F | 0 | 1 | 0 | A | 4 | 0 | 0 | E | D | 0 | 0 | F | 0 | 1 |
L21 00000000011110110000000001111000010000000010100100000000000111101100000000011110000100000000 L21
F9 00000000001111011000000000111100001000000001010010000000000011111011000000000111100001000000 F9
F10 00000000000000000000000000000000000000000000000011000000000000000000000000000000000000001111111 F10

Where:

F8 - F1	=	High- to low-order 8 bits of CR	L20	=	I playback
F9	=	Follows high-order bit of I	L21	=	I record
F10	=	Senses high-order 5 bits of I, if any of these bits = 1, F10 is set.			

Figure 3.3.6 Orders Precession

since the partial address within the instruction word contains the entire sector address, the program can be minimum access coded with only a small effort.

As another aid to understanding orders precession, figure 3.3.6 illustrates the flow of bits through the CR for a typical 16-bit precession of the control loop.

3.2 CLOCK AND TIMING PULSES

3.2.1 INTRODUCTION

All the clock and timing pulses used in the processor are either directly or indirectly derived from the playback of three master clock tracks. Figure 3.4 shows the clock and timing pulses used in the processor.

3.2.2 Z1 CLOCK

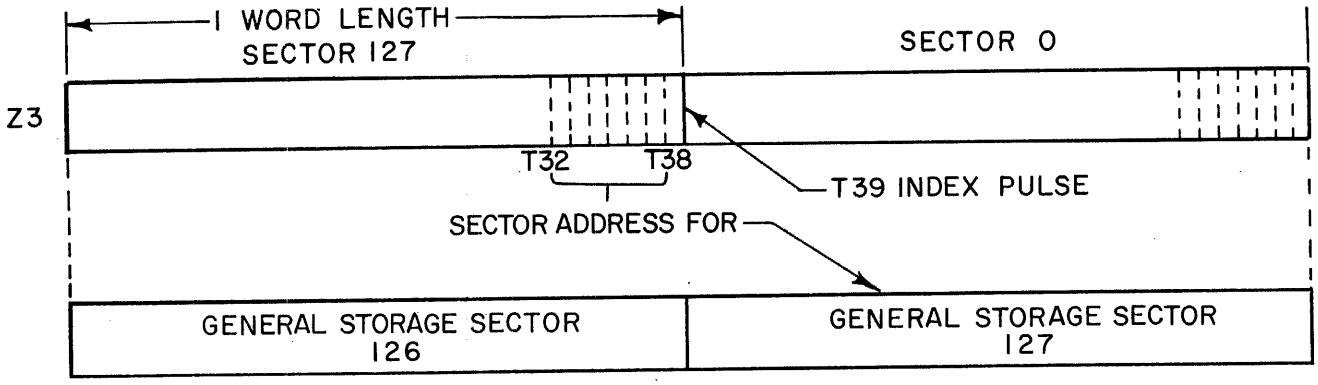
The Z1 clock is the basic timing clock of the processor. It is directly derived from the playback of the first master track. The Z1 clock is a continuously running pulse train, producing 5120 evenly spaced pulses per drum revolution. The time between the falling edge of one pulse and the next is defined as a bit-time (1 microsecond at a nominal drum speed of 11,900 RPM), and there are 40 bit-times, (0 through 39), per fixed length word or sector of the EBS 1601. The 40 bit-times of every word-time are denoted 0 through 39. The same is true of the 40 Z1 pulses per every word-time.

3.2.3 Z2 CLOCK

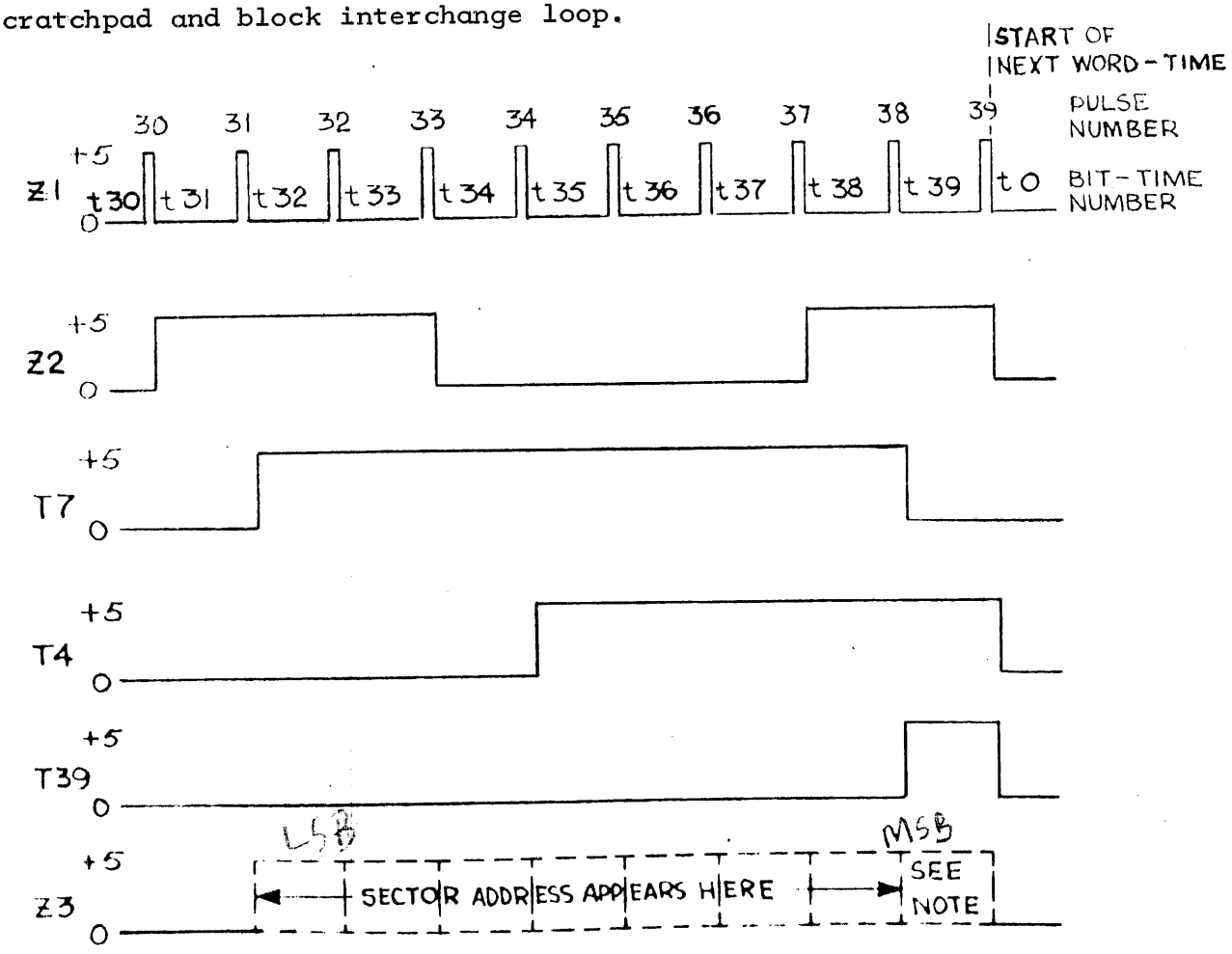
The playback from the second master track produces the sector index clock, Z2. The Z2 clock pulse is high during bit-times 31, 32, 33, and 38, 39. The Z2 clock is used to produce 3 other timing pulses: T4, T7, and T39. These timing pulses and the Z2 clock pulse are used to index, by being high, the various bit-times shown in figure 3.4.

3.2.4 Z3 CLOCK

The third master clock track produces sector address clock, Z3, during the T7 time. The seven high-order bits, T32 through T38, of each 40-bit word length in the Z3 clock track contains the sector address of the next available general storage track.



As shown in the illustration above, the sector address on the Z3 clock track is recorded one 40-bit word length ahead of the corresponding general storage track so that a full 40-bit length of recording space is available if comparison establishes that the Z3 clock track contains a word length with an address for the following general storage sector. The T39 index pulse, produced at every eighth sector from 7 through 127, in combination with that sector address selects the first sector of the scratchpad and block interchange loop.



+5v = Logical 1 0v = Logical 0

Rev. 1MAY69 Figure 3.4.1 Overall Timing Diagram.

3.3 SECTOR COMPARISON

3.3.1 INTRODUCTION

Sector comparison is the means by which the processor determines when the storage sector addressed by a command is available for use. Of those commands which can access storage, the 8-bit commands may only access scratchpad storage sectors, whereas the 16-bit commands may access both general storage and scratchpad storage sectors. The process of sector comparison performed for 8-bit commands differs from the process performed for 16-bit commands. Each process is discussed in the following text.

3.3.2 SECTOR COMPARISON FOR 8-BIT COMMANDS

The 3-bit scratchpad sector address for 8-bit commands which can access the scratchpad are contained in the low-order 3 bits of the CR. These 3 address bits are contained in flipflops F3, F2, and F1 of the CR as shown below:

F8	F7	F6	F5	F4	F3	F2	F1	8-Bit CR.
-	-	-	-	-	s	s	s	Contents of CR; dash equals bits of command other than address bits, "s" equals scratchpad address bits.

Using a Logical And command (LA) addressed to use scratchpad sector 5 as an example, the CR appears as shown below:

F8	F7	F6	F5	F4	F3	F2	F1
0	0	0	1	1	1	0	1

During time $\overline{T4}$ T7 (bit-times 32, 33, and 34), shown in figure 3.4, the sector address clock, Z3, produces the low-order 3 bits of the 7-bit sector address that specifies which one of the 128 general storage sectors is up-coming for use during the next word-time. It should be recalled from paragraph 1.3.2 that the low-order 3 bits of the general storage sector address specify the scratchpad sector which will be available for use during the next up-coming word-time. The processor must, therefore, determine if the scratchpad address contained in the command agrees (successful sector comparison) or disagrees (unsuccessful sector comparison) with the scratchpad address of the Z3 clock. The comparison is made bit-by-bit during bit-times 32, 33, and 34 ($\overline{T4}$ T7 time) of the search cycle, C30 (the only cycle which allows sector comparison), as follows:

a. During bit-time 32 of the first cycle through C30 for the command, the state of F1 is compared to the state of the Z3 clock. If they are unequal, F11 which was reset earlier in the word-time is set. If they are equal, F11 is left in the reset state.

b. During bit-time 33 of the first cycle through C30 for the command, the state of F2 is shifted into F1 while F1 is shifted into F3, and F3 shifted into F2. F1 (which now contains the original state of F2) is compared to Z3. If they are unequal, F11 is set. If they are equal, F11 is left reset.

c. During bit-time 34 of the first cycle through C30 for the command, The F3 to F2 to F1 to F3 loop is shifted one bit, as described in step b, so that F1 contains the original state of F3. F1 is then compared to Z3. If they are unequal, F11 is set. If they are equal, F11 is left reset.

The sector comparison is now complete and F11 stores the fact of whether the sector comparison was successful (F11 left in the reset state) or unsuccessful (F11 set). During bit-time 35 of the first cycle through C30 for the command, the F3 to F2 to F1 to F3 loop is shifted one more bit so that F3, F2, and F1 contain their original contents. If the sector comparison was successful, at the end of the first cycle through C30 the processor goes into C40 and executes the command. If the sector comparison was unsuccessful, at the end of the first cycle through C30 the processor is forced to recycle through C30 and make another sector comparison. This time the comparison is made to the next sector address of the Z3 clock. The processor is forced to recycle through C30 for as many times as is necessary to find a successful comparison (the maximum number of cycles through C30 is 8, since by this time all 8 scratchpad address are compared to the scratchpad sector address contained in the command). At the end of the C30 cycle in which a successful comparison is made, the processor goes into C40 and executes the command.

3.3.3 SECTOR COMPARISON FOR 16-BIT COMMANDS

The order of bits for 16-bit commands which access storage are, as should be recalled from paragraph 1.5.1, given below.

8 Bits of CR								High-Order 8 Bits of I							
F8	F7	F6	F5	F4	F3	F2	F1	39	38	37	36	35	34	33	32
-	-	-	-	t	t	t	t	t	s	s	s	s	s	s	s

Where:

s = sector address bits
t = track address bits

The first operation performed of the sector comparison process determines if the command's address specifies a scratchpad or a general storage sector. If the address specifies a general storage sector, then one or more of bits F4, F3, F2, F1, and 39 must be high. If all these bits are low, then the address specifies a scratchpad sector. This operation is performed as follows:

a. During T4 time (bit-times 35, 36, 37, 38, and 39) of precession cycle C20, which may or may not have been used with precession cycle C10 to shift the 16-bit command into the CR and high-order 8 bits of the I, the state of F1 is sensed by flipflop F10. During this time the high-order 5 bits of the I are processed through F1, as shown in figure 3.3.6. If any of these 5 bits (39, 38, 37, 36, and 35) are high, F1 will be high and F10, which was initially reset during the beginning of C20, is set.

b. During the first bit-time of C30, following C20, the states of F4, F3, F2, and F1 are sensed by F10. If any of these bits are high, F10 is set if it hasn't already been set in step a.

If, at this point, F10 is in the reset state, a scratchpad sector is specified by the command and the processor continues the sector comparison using the Scratchpad Sector Comparison Process given below. If F10 is in the set state, a general storage sector is specified by the command and the processor continues the sector comparison using the General Storage Sector Comparison Process given below.

Scratchpad Sector Comparison Process:

c. During bit-time 32 of the first cycle through C30 for the command, the state of the I playback, L20, is compared to the state of Z3. (The low-order sector address bit contained in I bit 32 is compared to the low-order sector address bit of the Z3 clock.) If they are unequal, F11 which was reset at beginning of C30 is set. If they are equal, F11 is left reset.

d. During bit-time 33 of the first cycle through C30 for the command, L20 (equal to I bit 33) is compared to Z3. If they are unequal, F11 is set. If they are equal, F11 is left reset.

e. During bit-time 34 of the first cycle through C30 for the command, L20 (equal to I bit 34) is compared to Z3. If they are unequal, F11 is set. If they are equal, F11 is left reset.

The scratchpad sector comparison is now complete and F11 stores the fact of whether the comparison was successful (F11 left in the reset state) or unsuccessful (F11 set). If the comparison was successful, at the end of the first cycle through C30 the processor goes into C40 and executes the command. If the comparison was unsuccessful, at the end of the first cycle through C30 the processor is forced to recycle through C30 and make another comparison. This time the comparison is made to the next sector address of the Z3 clock. The processor is forced to recycle through C30 for as many times as is necessary to find a successful comparison (the maximum number of cycles through C30 is 8, since by this time all 8 scratchpad addresses are compared to the scratchpad sector address contained in the command). At the end of the C30 cycle in which a successful comparison is made, the processor goes into C40 and executes the command.

General Storage Sector Comparison Process:

f. Steps c, d, and e of the Scratchpad Sector Comparison Process are performed.

g. During bit-time 35 of the first cycle through C30 for the command, L20 (equal to I bit 35) is compared to Z3. If they are unequal, F11 is set. If they are equal, F11 is left reset.

h. During bit-time 36 of the first cycle through C30 for the command, L20 (equal to I bit 36) is compared to Z3. If they are unequal, F11 is set. If they are equal, F11 is left reset.

i. During bit-time 37 of the first cycle through C30 for the command, L20 (equal to I bit 37) is compared to Z3. If they are unequal, F11 is set. If they are equal, F11 is left reset.

j. During bit-time 38 of the first cycle through C30 for the command, L20 (equal to I bit 38, the high-order sector address bit) is compared to Z3. If they are unequal, F11 is set. If they are equal, F11 is left reset.

The general storage sector comparison is now complete and F11 stores the fact of whether the comparison was successful (F11 left in the reset state) or unsuccessful (F11 set). If the comparison was successful, at the end of the first cycle through C30 the processor goes into C40 and executes the command. If the comparison was unsuccessful, the processor is forced to recycle through C30 and make another comparison. This time the comparison is made to the next sector address of the Z3 clock. The processor is forced to recycle through C30 for as many times

as is necessary to find a successful comparison. The maximum number of cycles through C30 is 128, since by this time all 128 general storage sectors on the track specified by the "t" bits (the process of track selection is discussed in Chapter 4) in the command are compared to the general storage sector address contained in the command. At the end of the C30 cycle in which a successful comparison is made, the processor goes into C40 and executes the command. Figure 3.4.2 illustrates an example of sector comparison and shows the waveshapes involved.

3.4 PLAYBACK AND RETIMING

3.4.1 GENERAL STORAGE

Since general storage uses the same head for record and playback operations (unlike the other loops on the drum that have two separate heads), the various time delays in recording and playing back information cannot be cancelled by positioning the playback head early on the drum (as in the case of the other loops). However, the processor is designed so that these delays add up to one bit-time. Thus, by recording information one bit-time early into general storage (from T39 of C30 to T38 of C40, instead of from T0 of C40 to T39 of C40) general storage playback is on time. Note that the playback flipflop, M149, shown in figure 3.88, is clocked with $\overline{Z1}$. Since this flipflop triggers on the positive-going edge of the clock, which is the trailing edge of the $\overline{Z1}$ clock pulse, L40 is guaranteed to be stable on the positive-going leading edge of Z1, used to clock the flipflops that have L40 as an input.

3.4.2 SCRATCHPAD AND BLOCK INTERCHANGE LOOPS

Both of these two loops have separate record and playback heads. This allows positioning of the playback head on drum to cancel the record and playback time delays. The playback flipflops, M147, shown in figures 3.86 and 3.91 are clocked with $\overline{Z1}$ for the same reason as M149, discussed in paragraph 3.4.1.

3.4.3 INSTRUCTION REGISTER

The I, shown in figure 3.84, consists of 5 8-bit serial shift register packages and a single flipflop, all connected to form a single serial shift register. The 5 packages, M155 through M159, are clocked with Z1 while the single flipflop, M149, is clocked with $\overline{Z1}$. As a result, the total delay of the I is 40 bits since the last bit of package M155 and the bit of flipflop M149 are clocked with the leading and trailing edge, respectively, of the same clock pulse. This is also done with the general storage, scratchpad, block interchange, Z2 and Z3 loops on the drum. The reason for clocking M149 with $\overline{Z1}$ is the same as M149, discussed in paragraph 3.4.1.

3.4.4 ACCUMULATOR REGISTER, MASTER TIMING TRACK PLAYBACKS

The A, Z2, and Z3 playbacks work on the same Z1 - $\overline{Z1}$ timing principle that the I works on, discussed in paragraph 3.4.3. Since the Z1 master track produces the Z1 clock pulse to which all timing in the processor is referenced, it does not have the timing problem that the other loops and registers discussed in this section have.

3.4.5 COMMAND REGISTER

The 8-bit CR is a serial shift register made up of separate master-slave flipflops. As a result of using master-slave flipflops the problem of output information being stable on the leading edge of the Z1 clock pulse is not present.

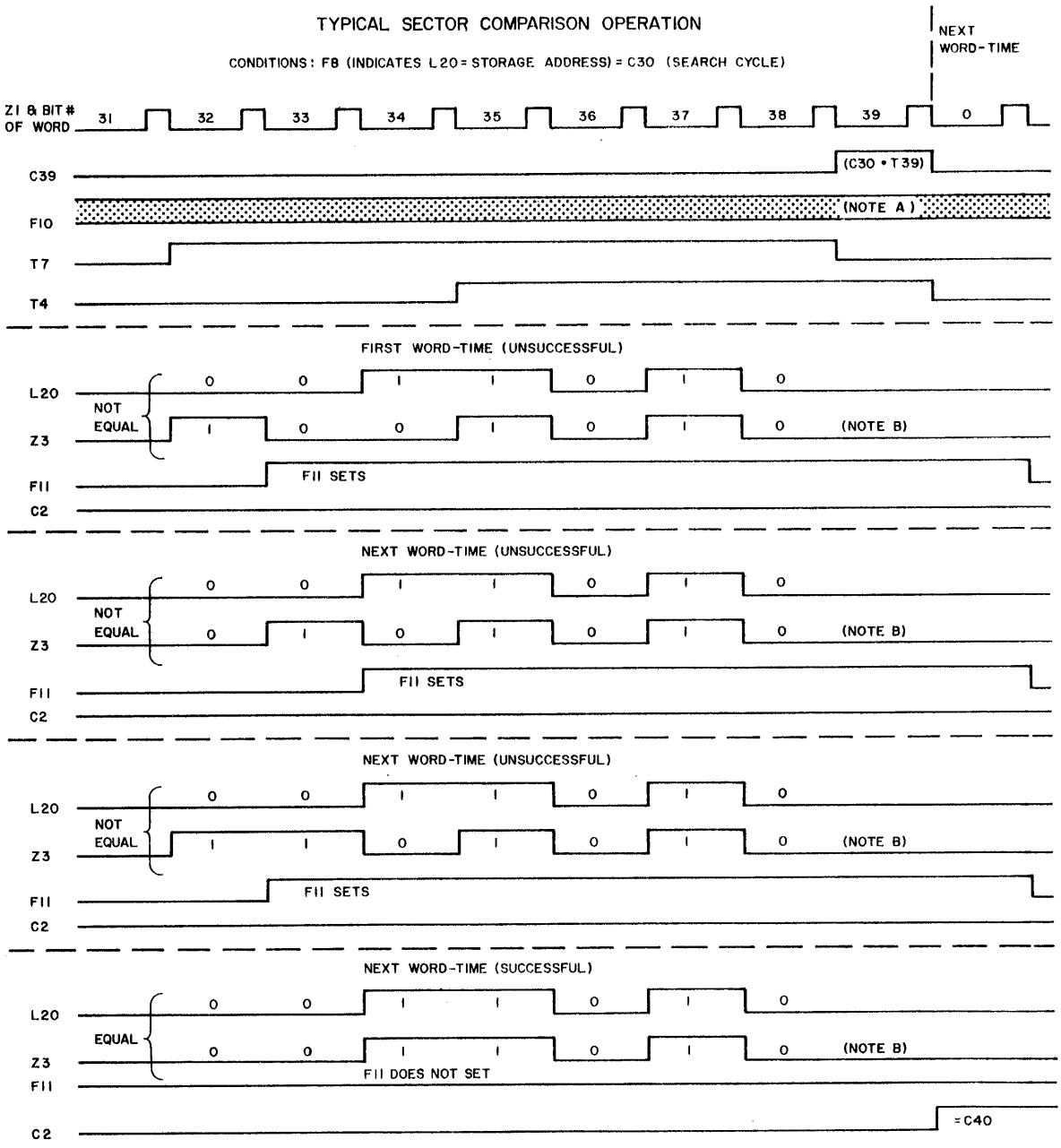
3.4.6 BUFFER REGISTER

The B, shown in figures 3.70 and 3.71, is clocked with a logically gated derivative of the Z1 clock pulse, named Z4. The waveshape of the Z4 pulse is identical to that of the Z1 pulse, though Z4 is only present at times controlled by the logic. Since Z4 is a logically gated derivative of Z1, it is slightly delayed with respect to Z1. Information entering the buffer register is timed with Z1. Since Z4 lags Z1, the bit of information to be entered into the B may no longer be present or stable by the time Z4 arrives. This problem (technically known as "clock skew") is solved in the following manner. Information is entered into M131-2 with the leading edge of the Z1 clock. It is then transferred into M131-12 on the trailing edge of the $\overline{Z4}$ clock. All this occurs within slightly more than one clock-pulse time so that the total delay of the 2 flipflops is only one bit-time. The information at F28 is stable at Z4 time. The rest of the B is clocked with Z4. Since Z4 lags Z1, B output is stable at Z1 time, therefore, no problem exists in going from Z4 timing back to Z1 timing.

3.5 FLIPFLOP FUNCTIONS

The EBS 1601 contains a total of 37 flipflops. Each is listed below (in the form of output signal suffixed to package number) and followed by the function it performs in the processor.

FLIPFLOP	FUNCTION
M131-F20	Buffer Register Z1 to Z4 Retiming
M131-F28	Buffer Register Z1 to Z4 Retiming and Bit B8
M127-F27	Buffer Register Bit F27
M130-F26	" " " F26



NOTES:

A) If F10 is set, comparison occurs from bits 32-38. If F10 is reset, occurs only during bits 32, 33, and 34. State of F10 is determined during T4 time of last precession cycle.

B) Address in Z3 identifies next sector under head.

Figure 3.4.2 Sector Comparison Process

FLIPFLOP	FUNCTION
M130-F25	Buffer Register Bit F25
M129-F24	" " " F24
M129-F23	" " " F23
M128-F22	" " " F22
M128-F21	" " " F21
M14-C1	Cycle Control
M13-C2	Cycle Control
M64-F1	Command Register Bit F1
M63-F2	" " " F2
M61-F3	" " " F3
M62-F4	" " " F4
M61-F5	" " " F5
M60-F6	" " " F6
M59-F7	" " " F7
M58-F8	" " " F8
M97-F9	Control
M97-F10	"
M112-F11	"
M126-F15	"
M105-F12	Parity Failure Register (P)
M112-F14	Carry Register (K) and Control
M45-L10	Retiming, Accumulator Register
M149-L20	" Instruction Register
M147-L39	Retiming and One Bit-Time Early Playback, Fast Access Loop
M146-L30	Playback on Time, Fast Access Loop
M149-L40	Retiming, General Storage
M147-L90	" Block Interchange Loop
M148-Z2	Timing, Master Track Z2
M148-Z3	" Master Track Z3
M11-M5	Mode Control
M12-M6	Mode Control
M10-T4	Timing
M9-T7	Timing

The B, CR, K, and P are discussed in paragraph 1.5. Playback and retiming flipflops are discussed in paragraph 3.4. Mode-cycle flipflops are discussed in paragraph 3.1. Timing signals produced by the timing flipflops are discussed in paragraph 3.2.

Flipflops classified as control flipflops perform a variety of functions which are discussed in the "sequence of events" description of those commands which make use of them. Most of these functions are also listed in the Signal Glossary, paragraph 3.8.1, under their corresponding output signal.

3.6 INTERFACE AND INPUT-OUTPUT DEVICE SELECTION

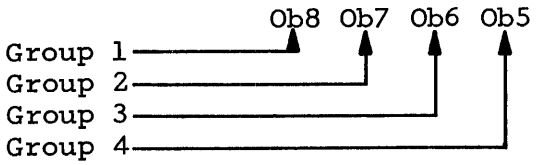
Connection between the processor and its peripheral I/O devices is made via the 1966 Standard 27 Wire Interface. As many as 8 input and 8 output devices can be attached to interface at one time. These devices are connected one to another in chain fashion along the interface from the processor. Listed below are the connector pin-signal assignments for the interface.

PIN	SIGNAL
1	Frame Ground
2	Circuit Ground
3	+18 volts
4	dc Return
5	K150 Clear
6	K83 Input/Status Control (K83 = Status data, $\overline{K83}$ = Character
7	Input Busy K75
8	W110 Inhibit
9	K82 Device Select Common
10	K80 Output Common DATA COMMON
11	Ob1
12	Ob2
13	Ob3
14	Ob4
15	Ob5
16	Ob6
17	Ob7
18	Ob8
19	K76 Output Busy
20	spare
21	Ib1
22	Ib2
23	Ib3
24	Ib4
25	Ib5
26	Ib6
27	Ib7
28	Ib8
29	spare
30	spare
31	spare
32	spare
Shell	Shield

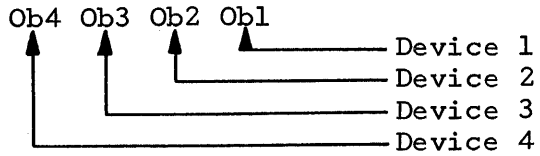
The EBS 1601 is capable of supporting 16 I/O devices, conveniently arranged in 4 groups of 4 devices per group. To execute a transfer of data to or from a device, it must be selected. I/O devices are selected and/or unselected via any of the following 4 device select commands:

Accumulator Select	(7600)
Accumulator Select on Test	(7400)
Immediate Select	(7E00+D)
Immediate Select on Test	(7C00+D)

The above commands output an 8-bit device select code over output lines Ob8 through Ob1. The 8-bit device select code is divided into 2 tetrads: Ob8 Ob7 Ob6 Ob5 Ob4 Ob3 Ob2 Ob1. A "1" in any of the high-order tetrad bits specifies a group or groups of devices as follows:



A "1" in any of the low-order tetrad bits specifies a device or devices of the group(s) specified by the high-order tetrad as follows:



The bits of the high-order tetrad are called Group Bits; the bits of the low-order tetrad are called Select Bits. Each device along the interface is jumpered to its appropriate Group and Select Bits. Each device has a special jumper board for this purpose. In order to select and/or unselect one or more of the devices, it is necessary that the processor execute one of the 4 device select commands. The execution of such a command forces the Device Select Common signal high. This signal is sent to all the devices connected along the interface and forces them to scan their Group Bit and Select Bit inputs. Listed below are the different logic level combinations of the 3 signals and their results upon the selection-unselection of the devices.

DEVICE SELECT SIGNAL	GROUP BIT	SELECT BIT	RESULTS
High	High	High	Device Selected
High	High	Low	Device Unselected
High	Low	High	No Effect
High	Low	Low	" "
Low	Any Combination		" "

NOTE: All signals must be simultaneously present in order to effect selection-unselection of a device(s).

3.7 COMMANDS

3.7.1 INTRODUCTION

On the following pages, each of the 44 commands, and their variations, used by the processor is described in detail and accompanied by a flow chart showing its sequence of events. The commands are arranged in alpha-numeric order based on their hexadecimal code. To facilitate the location of each command, and index, listing each command by its mnemonic and giving the page it is to be found on, follows this introduction. The index also gives the hexadecimal coding of each command and its timing. Following the descriptions of the commands are the logic diagrams of the EBS 1601. At the end of this chapter (following the logic diagrams) are signal and abbreviation glossaries.

The logic names of the commands, given with the description of each command, are derived from the basic logic signal that each command uses. For example, all the K0 commands (K0A through K0F) use the K0 logic signal, both the K1A and the K1B commands use the K1 signal. There are cases, such as K8, the Jump command, for which there is no corresponding logic signal, such as a K8 logic signal, and vice versa. In these cases, the logic name of the command was arbitrarily chosen.

INDEX OF COMMANDS

Mnemonic	Hex. Code	Name	Timing	Page
AC	D000+M	Add Conditional	4+ma (3)	3.150
AD	9000+M	Add	4+ma	3.144
AK	08	Add K	3	3.32
AS	76C0	Accumulator Select	4	3.134
AST	74C0	Accumulator Select on Test	4 (3)	3.132
BI	0F	Block Interchange	10+za (2)	3.42
BLD	4200+N	Binary Left Double shift	8n-3+za	3.71
BLDK	4280+N	Binary Left Double shift, including K	8n-3+za	3.71
BLDS	4300	Binary Left Double shift, on Scratchpad	5	3.74
BLDSK	4380	Binary Left Double shift on Scratchpad, including K	5	3.74
BLS	4000+N	Binary Left Single shift	3+n	3.65

INDEX OF COMMANDS (CONT'D)

INDEX OF COMMANDS (CONT'D)

INDEX OF COMMANDS (CONT'D)

NOTE:

A = Accumulator Register
I = Instruction Register
K = K (Carry Flipflop F14) Bit
ma = Memory Access Time
n = Shift Count
sa = Scratchpad Access Time
za = Scratchpad Address 000 Access Time
M = Storage Address 000-FFF
S = Scratchpad Sector Address 000-007
N = Shift Count - 1
D = Device Select Code (8-Bit Maximum)
C = Character (8 Bits)

All timing is given in word-times, timing figure in parenthesis is for aborted command (condition failure).

3.7.2 HALT COMMAND (HH)

Hex code:	00+X	Logic Name:	K0A
Binary Code:	0000 0XXX	Timing:	

Description

This command, decoded one bit-time before C30, forces the processor into the idle mode. In this mode all information within the processor remains unchanged. The processor remains in this mode until either the RUN or STEP button is pressed. The state of the X bits do not affect the operation of the command. They are used to identify various Halt commands of the program in execution, on the REGISTER DISPLAY indicator lights. Figure 3.5 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C20:
   1) Set M0 at T39 via gates M31 and M24-12, figure 3.92. Note that at T39 of C20 the Halt command is being decoded one bit early so that the state of the command register is 000X XXX- and $\overline{L20}$=1.
   2) Set C30 at T39 via gate M22, figure 3.54.

B) Set C30M1 via gate M11-9, figure 3.92, on next clock pulse after establishment of C30M0 if S2.

C) Remain in C30M1 until RUN or STEP button is pressed, or the REGISTER SELECT switch is rotated out of a CONTROL position.

Decoded Signals

3.46
3.49 A5 = $\overline{F8}\ \overline{F7}\ M6$
3.51 A12 = $C20\ K0\ \overline{L20}$
3.73 K0 = $A5\ \overline{F5}\ \overline{F6}$
3.96 S2 = Positions 0, 8, 16, 24, and 32 of REGISTER SELECT switch or RUN and STEP buttons not depressed while REGISTER SELECT switch is in a CONTROL position.

IF PROC WAS RUNNING, DISPLAY HALT INSTRUCTION

DURING S/S, DONT XQT THE HALT IN DISPLAY.

(NOR ALL OTHER INSTRUCTIONS, THE DISPLAYED INSTRUCTION IS XQTED)

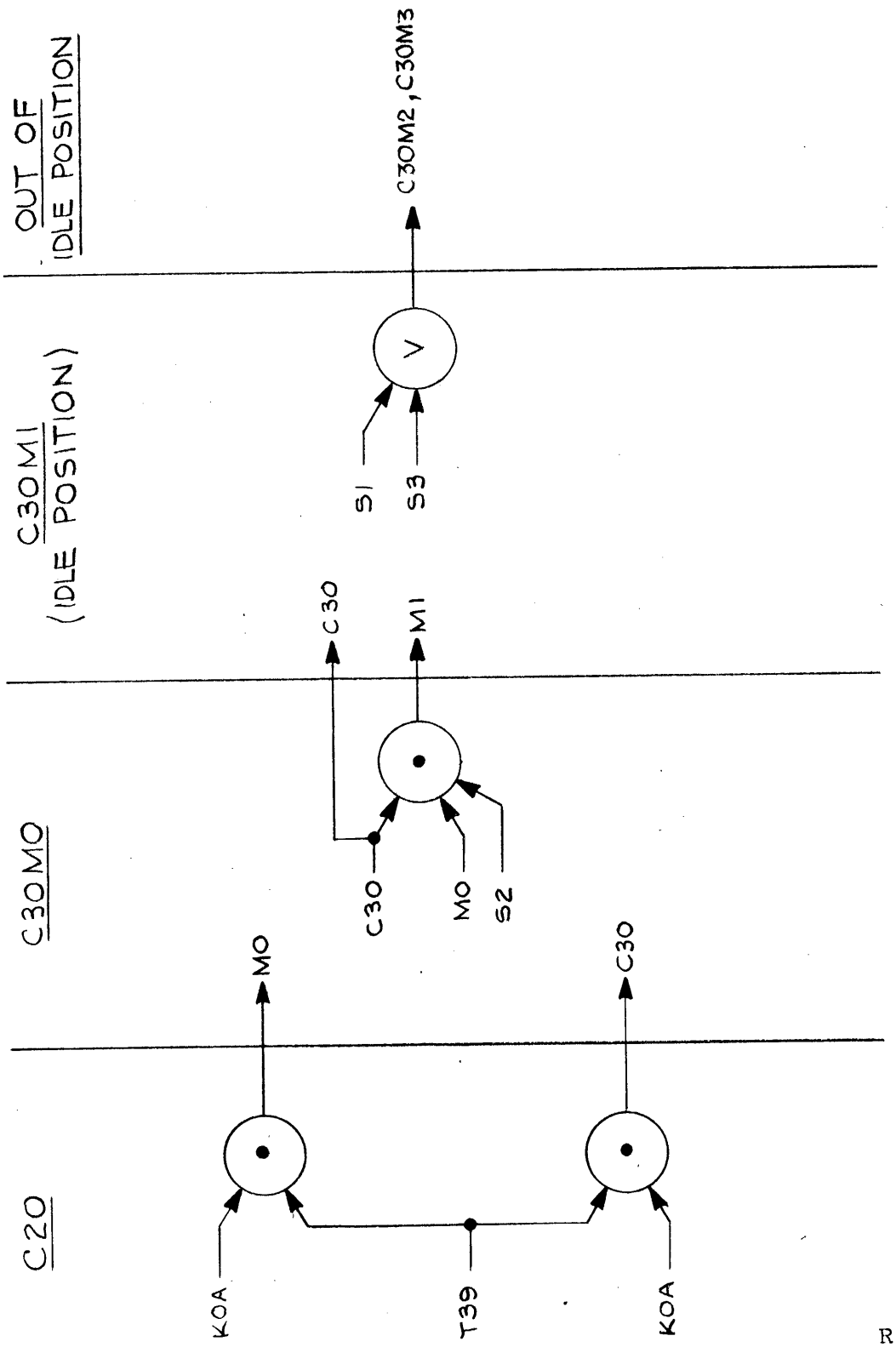


Figure 3.5 Halt Command, Flow Chart

3.7.3 ADD K COMMAND (AK)

Hex Code:	08	Logic Name:	K0F
Binary Code:	0000 1000	Timing:	3

Description

This command causes the content of K (F14) to be added to the low-order A bit. The results are stored in A. If A overflows, K is set; otherwise K is reset. Figure 3.6 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30 at T39 set C40 via gate M33-6, figure 3.55.

B) During C40:
   1) Reset L50 for duration of C40 via gates M88-3 and M88-4, figure 3.89.
   2) Establish L51 equal to A playback (L10) via gate M67-1, figure 3.90.
   3) Add K (F14) to contents of A via adder/subtractor, figure 3.90, and record results (L53) back into A via gate M36-9, figure 3.81.
   4) Leave K (F14) set if A overflows via gate M103-5, figure 3.67.
   5) Set C20 at T39 via gates M25-8, figure 3.54, and M13-9, figure 3.55.

Decoded Signals

A18 = $\overline{F8}$ F7

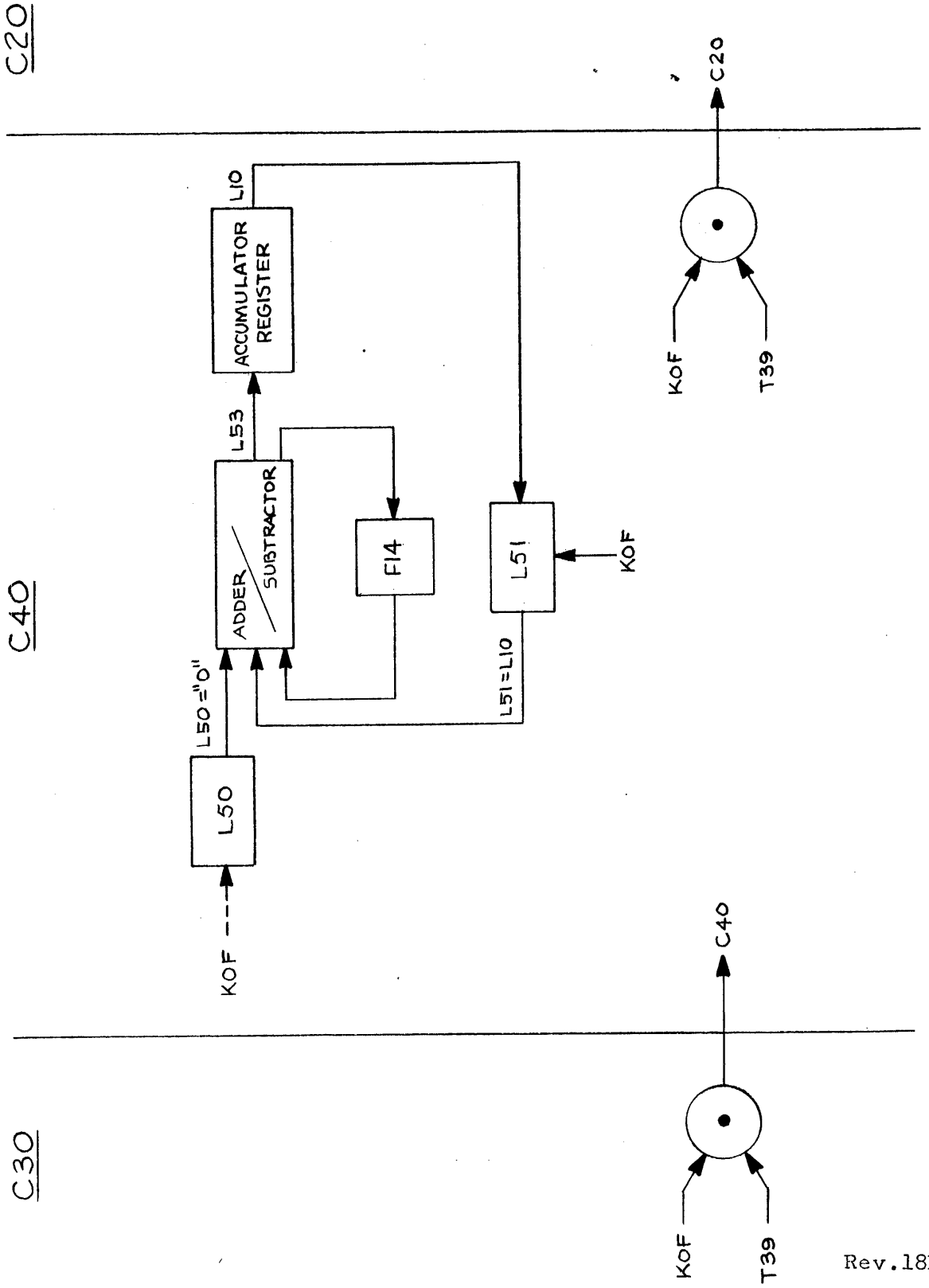


Figure 3.6 Add K Command, Flow Chart.

Rev.18NOV68

3.7.4 CLEAR A COMMAND (CL)

Hex Code:	09	Logic Name:	K0C
Binary Code:	0000 1001	Timing:	3

Description

This command loads the A with 0's, thereby clearing it. Figure 3.7 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30 set C40 at T39 via gate M33-6, figure 3.55.

B) During C40:
   1) Do not enable any input to gate M47-6, figure 3.83, via keeping L11 low.
   2) Set C20 at T39 via gates M25-8, figure 3.54, and M13-9, figure 3.55.

Decoded Signals

A18 = $\overline{F8}$ F7

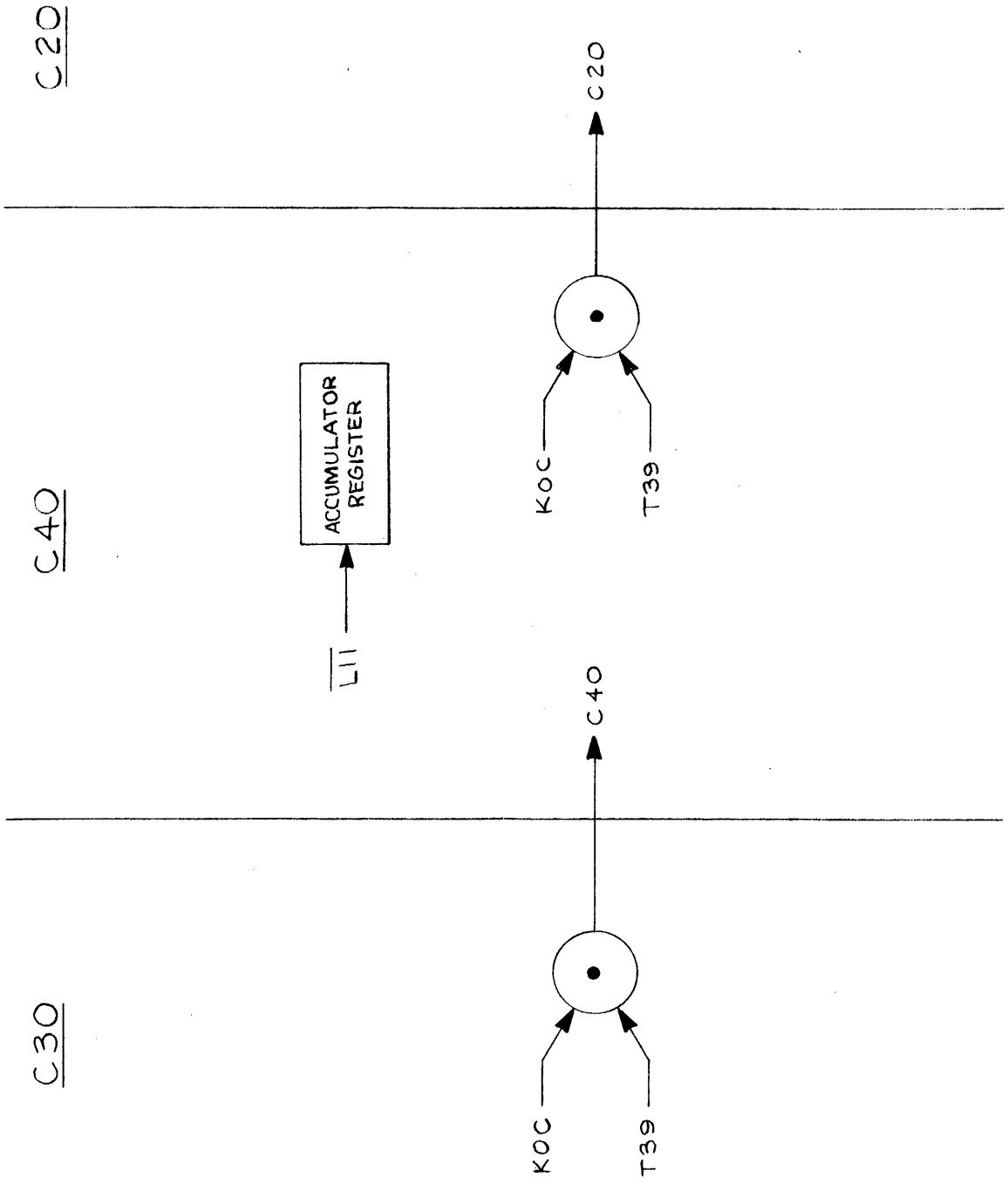


Figure 3.7 Clear A Command, Flow Chart.

3.7.5 NO-OPERATION COMMAND (NN)

Hex Code:	0A	Logic Name:	K0B
Binary Code:	0000 1010	Timing:	1

Description

This command causes the processor to recycle through C20, precessing the next high-order 8 I bits into the CR. If these bits contain another No-Operation command the processor remains in C20 until the next high-order 8 bits of the I are precessed into the CR. The processor recycles through C20 for as many times as this command is decoded. When this command is no longer decoded, the processor is allowed to advance into C30. Figure 3.8 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

During C20:

1) Set M0 at T39 if M2 via gate M12-11, figure 3.92.
2) Remain in C20 (don't advance into C30 at T39) via gate M14-9, figure 3.54. Note that at T39 of C20 the No-Operation command is being decoded one bit early so that the state of the CR is 0001 010- and $\overline{L20}$ = 1.
3) Advance into C30 at T39 if No-Operation command is not decoded via gate M14-9, figure 3.54.

Decoded Signals

A38 = F5 $\overline{F6}$

IF CR (8 BITS) + I (40 BITS) ONLY CONTAINS 0A INSTRUCTIONS, THE MACHINE WILL STAY IN C20 TILL POWER DOWN!

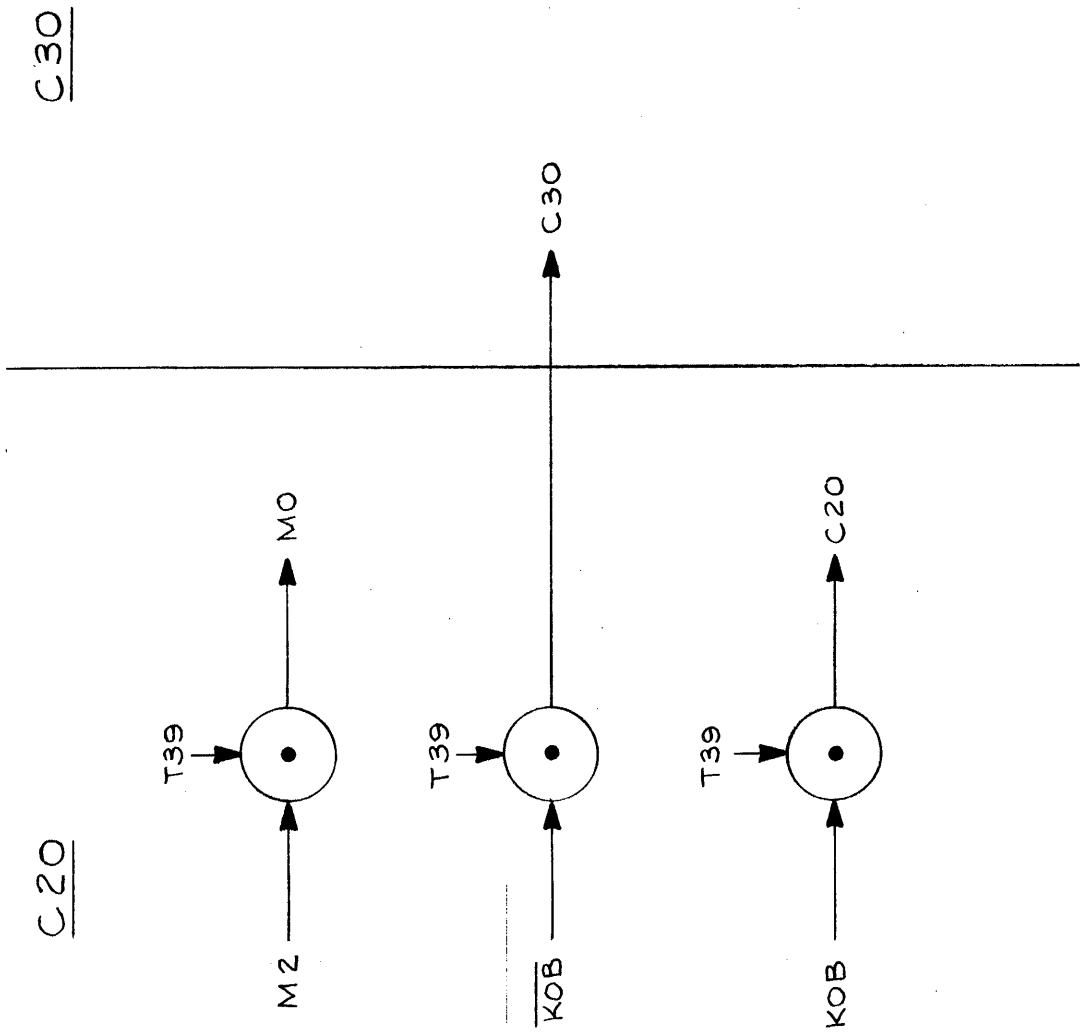


Figure 3.8 No-Operation Command, Flow Chart.

3.7.6 COMPLEMENT (CM)

Hex Code:	OB	Logic Name:	KOD
Binary Code:	0000 1011	Timing:	3

Description

This command causes the processor to take the 2's complement of the contents of the A. The results are stored in the A. K (F14) is set if the contents of the A is not equal to zero; otherwise K is reset. The logic of the adder/subtractor used in this operation is based upon the signal notation given below. Figure 3.9 is a flow chart showing the sequence of events that occur for this command.

L50 - Minuend
L51 = Subtrahend
F14 = Borrow
L53 = Difference

Equating the basic formula for a full-subtractor in terms of the above signals results in the following equation: L53 = L50 L51 F14 v L50 $\overline{L51}$ $\overline{F14}$ v $\overline{L50}$ L51 $\overline{F14}$ v $\overline{L50}$ $\overline{L51}$ F14. Since the minuend is kept equal to zero in taking the 2's complement, L53 = $\overline{L50}$ L51 $\overline{F14}$ v $\overline{L50}$ $\overline{L51}$ F14. As long as the A input (subtrahend) to the adder/subtractor is zero, the borrow remains reset ($\overline{F14}$) because 0 - 0 = 0 with no borrow. However, the first time the subtrahend equals 1 the borrow is set and remains so for the duration of the complementation process because 0 - 1 = 1 with a borrow. Since all the minuends are zero the borrow is required for all the remaining subtractions.

Sequence of Events

A) During C30:
   1) Reset F14 at T39 via gate M95-4, figure 3.67.
   2) Set C40 at T39 via gate M33-6, figure 3.55.

B) During C40:
   1) Reset L50 for duration of C40 via gates M88-2 and M88-4, figure 3.89.
   2) Establish L51 equal to A playback (L10) via gate M67-1, figure 3.90.
   3) Subtract L51 from L50 via adder/subtractor, figure 3.90, and record difference (L53) in A via gate M36-9, figure 3.81.
   4) Set F14 if L10 via L51 with gate M108-8, figure 3.68.
   5) Set C20 at T39 via gates M25-8, figure 3.54, and M13-9, figure 3.55.

Decoded Signals

A18 = $\overline{F8}$ F7
K28 = K0 F2 F4

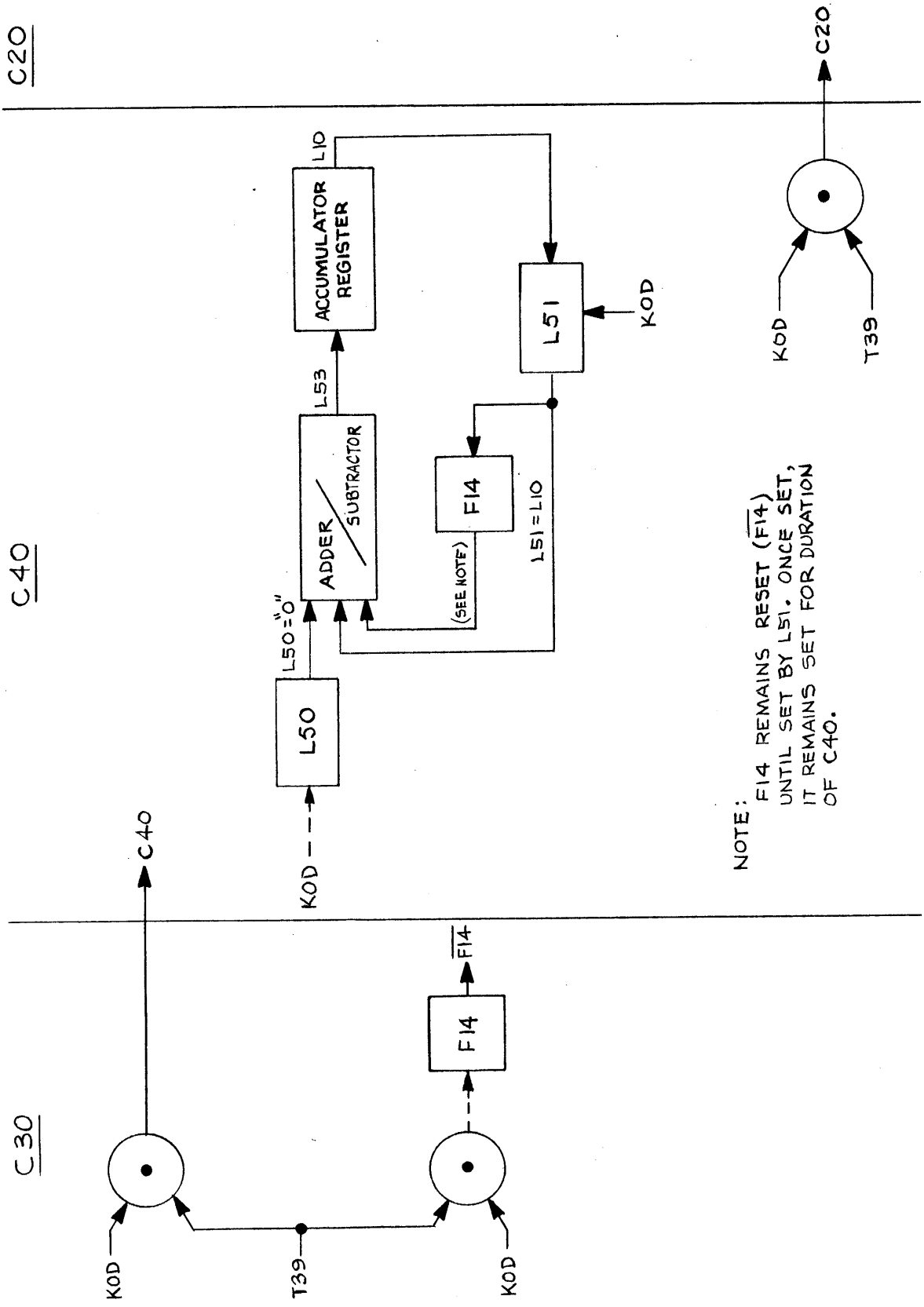


Figure 3.9 Complement Command, Flow Chart.

3.7.7 JUMP TO A COMMAND (JA)

Hex Code:	0D	Logic Name:	K0E
Binary Code:	0000 1101	Timing:	3

Description

This command causes the contents of the A to be shifted into the I, while the contents of the A is regenerated. Figure 3.10 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30 at T39 set C40 via gate M13-9, figure 3.55.

B) During C40:
   1) Shift contents of A into I via gate M1-1, figure 3.85, while regenerating A via gate M35-13, figure 3.82.
   2) Set C20 at T39 via gates M25-8, figure 3.54, and M13-9, figure 3.55.

Decoded Signals

A5 = $\overline{F8}\ \overline{F7}$ M6
K0 = A5 $\overline{F5}\ \overline{F6}$
K27 = K0 $\overline{F2}$ F3 F4

IF A = 01 02 03 04 05
AND CR = 0D AND I = EEFF0ADA0A (ORIGINAL INSTRUCTION WAS FF0A0A0A0D)
THEN AFTER C40, A = OLD A (LAST 2 TRACKS)
AND CR = 01 AND I = 02030405 0D
AND NEXT INSTRUCTION IS THE '01'

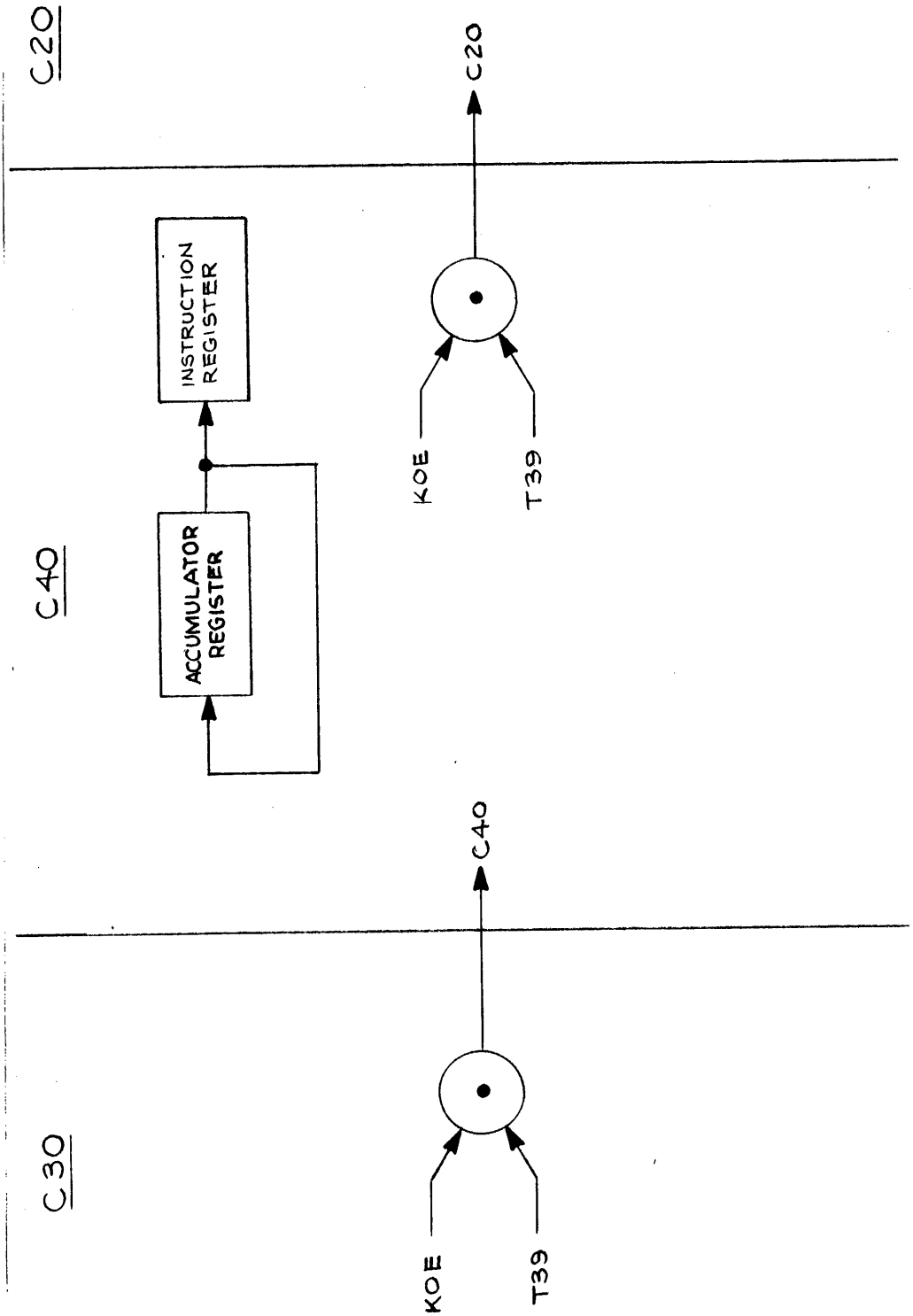


Figure 3.10 Jump to A Command, Flow Chart.

Rev.18NOV68

3.7.8 BLOCK INTERCHANGE COMMAND (BI)

Hex Code:	OF	Logic Name:	KOG
Binary Code:	0000 1111	Timing:	10+za (2)

Description

This command causes the contents of the block interchange loop to be interchanged with the contents of the scratchpad loop, and vice versa. K (F14) is set. If an external block interchange device is used with the processor, this command will only be executed when the busy signal line from the device is low during T7 of C30. If high at that time, the command is aborted and K reset. If an external block interchange device is not used with the processor, the busy signal line is wired in the processor to a constant low so that the command is always executed. Figure 3.11 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30:
   1) Set F14 via gate M111-9, figure 3.68.
   2) Reset F14 at T7 if external block interchange device is busy (K92 = 1) via gate M107-5, figure 3.66. If external block interchange device is not plugged into the processor, this step is not performed and F14 is left set.
   3) Set C40 at T39 if $\overline{F14}$ and Z3 via gate M34-3B-6, figure 3.55.
   4) Set C20 at T39 if $\overline{F14}$ via gate M25-6, figure 3.54.

B) During C40:
   1) Record contents of scratchpad loop into block interchange loop via gates M57-8 and M49-8, figure 3.91.
   2) Record contents of block interchange loop into scratchpad loop via gates M50-8 and M49-11, figure 3.87.
   3) Set C20 at T39 if Z3 via gates M25-6, figure 3.54 and M13-9, figure 3.55.

Decoded Signals

$A5 = \overline{F8}\ \overline{F7}\ M6$
$A13 = \overline{C49}\ \overline{K9}\ \overline{Z3}$
$A14 = \overline{C39}\ v\ F14\ v\ (\overline{A11}\ \overline{K9})$
$K0 = A5\ \overline{F5}\ \overline{F6}$
$K9 = K28\ F1\ F3$
$K28 = K0\ F2\ F4$
$K90 = K9\ C40$

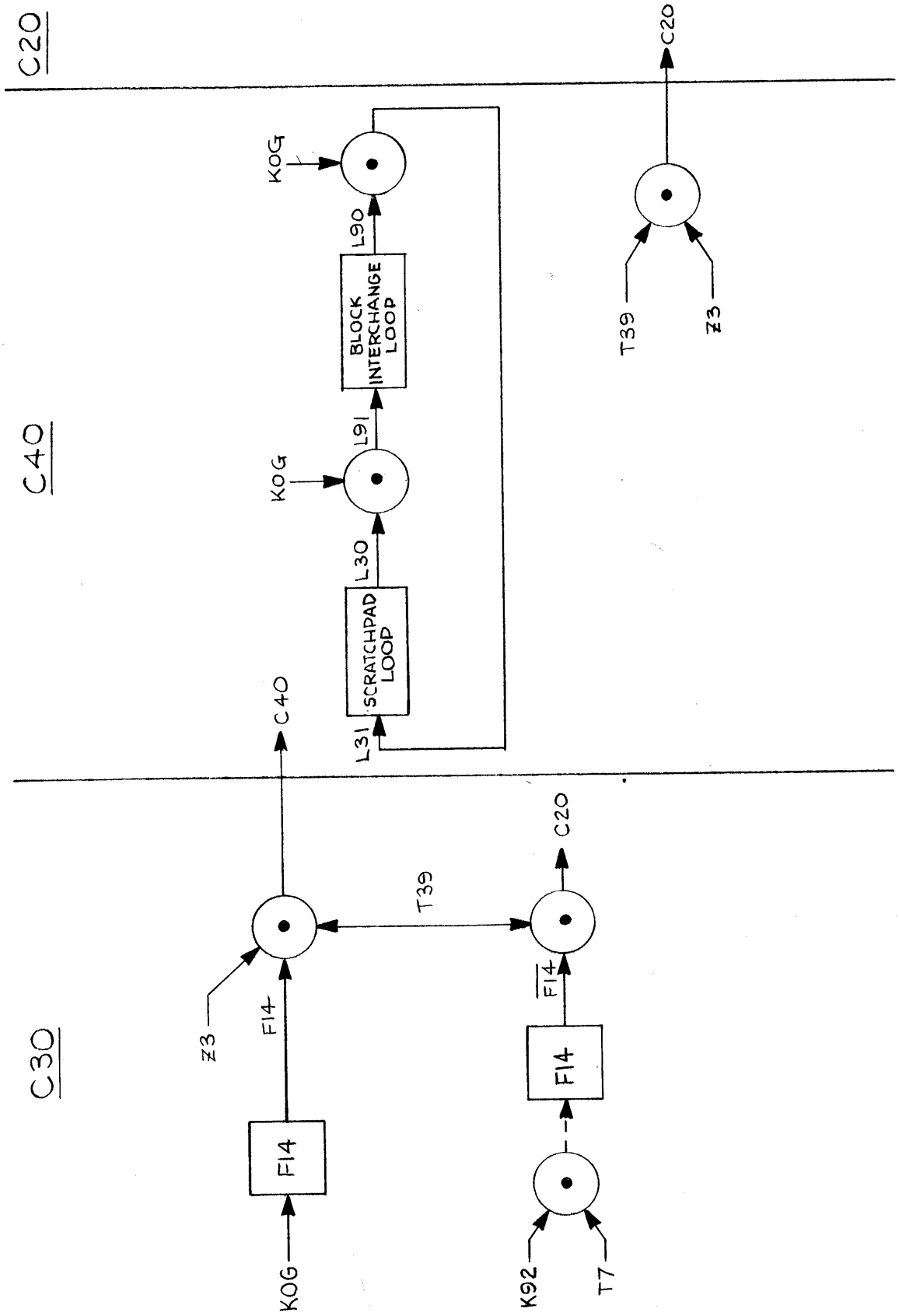


Figure 3.11 Block Interchange Command, Flow Chart.

3.7.9 SET K TO 1 COMMAND (SK)

Hex Code:	10	Logic Name:	K7D
Binary Code:	0001 0000	Timing:	3

Description

This command forces K (F14) to set, regardless of its prior state. Figure 3.12 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30:
   1) Set F14 via M108-12, figure 3.68.
   2) Set C40 at T39 via gate M33-6, figure 3.55.

B) During C40 at T39 set C20 via gates M25-8, figure 3.54 and M13-9, figure 3.55.

Decoded Signals

$A5 = \overline{F8}\ \overline{F7}\ M6$
$K0 = A5\ \overline{F5}\ \overline{F6}$
$K9 = K28\ F1\ F3$
$K28 = K0\ F2\ F4$

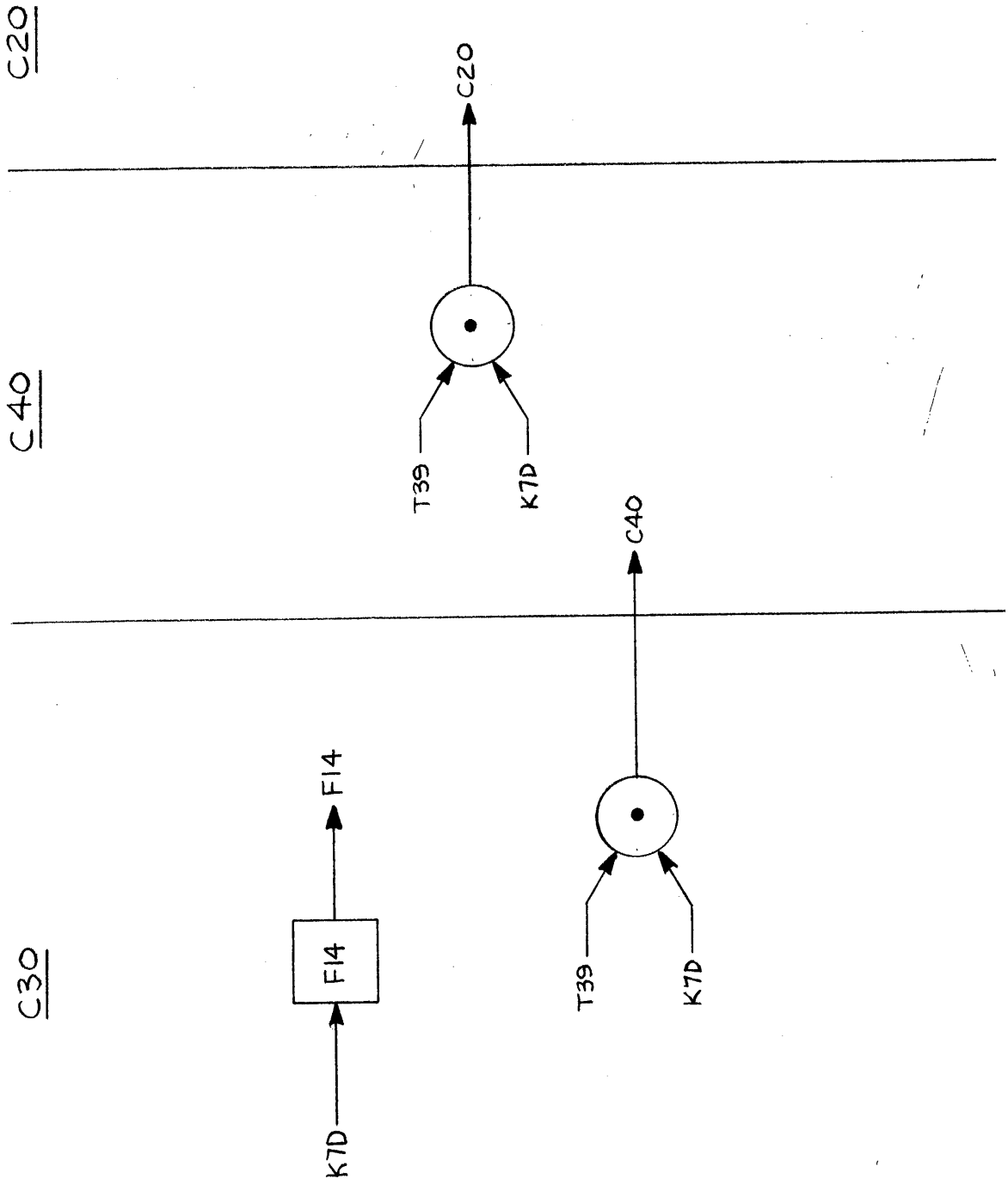


Figure 3.12 Set K to 1 Command, Flow Chart.

3.7.10 TEST FOR ZERO (TZ)

Hex Code:	11	Logic Name:	K7A
Binary Code:	0001 0001	Timing:	3

Description

This command forces K (F14) to set if the A contains all 0's, otherwise K is reset. Figure 3.13 is flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30:
   1) Set F14 via gate M109-6, figure 3.68.
   2) Set C40 at T39 via gate M33-6, figure 3.55.

B) During C40:
   1) Reset F14 if L10 via gate M94-13, figure 3.66.
   2) Set C20 at T39 via gates M25-8, figure 3.54 and M13-9, figure 3.55.

Decoded Signals

$A5 = \overline{F8}\ \overline{F7}\ M6$
$A14 = \overline{C39}\ v\ F14\ v\ (\overline{A11}\ \overline{K9})$
$A38 = F5\ \overline{F6}$
$K7 = A5\ A38\ C40$

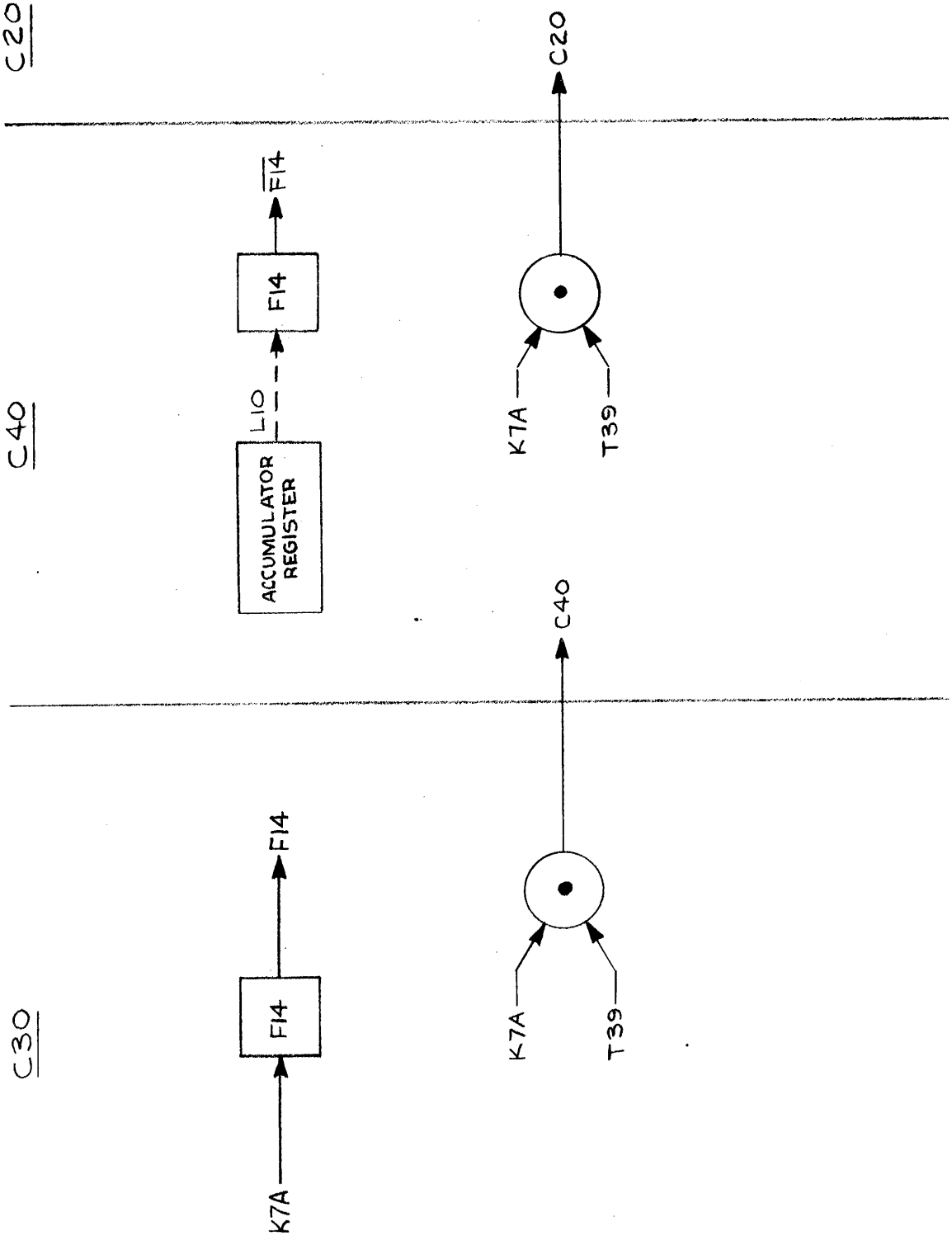


Figure 3.13 Test for Zero Command, Flow Chart.

3.7.11 TEST HIGH ORDER A BIT COMMAND (TH)*

* This command is also called Test for Negative (TN).

Hex Code:	12	Logic Name:	K7B
Binary Code:	0001 0010	Timing:	3

Description

This command forces K (F14) to set if the high-order A bit equals 1, otherwise K is reset. Figure 3.14 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30:
   1) Set F14 via gate M109-6, figure 3.68.
   2) Set C40 at T39 via gate M33-6, figure 3.55.

B) During C40:
   1) Reset F14 if $\overline{L10}$ at T39 via gate M86-9, figure 3.66.
   2) Set C20 at T39 via gates M25-8, figure 3.54, and M13-9, figure 3.55.

Decoded Signals

$A5 = \overline{F8}\ \overline{F7}\ M6$
$A38 = F5\ \overline{F6}$
$K7 = A5\ A38\ C40$

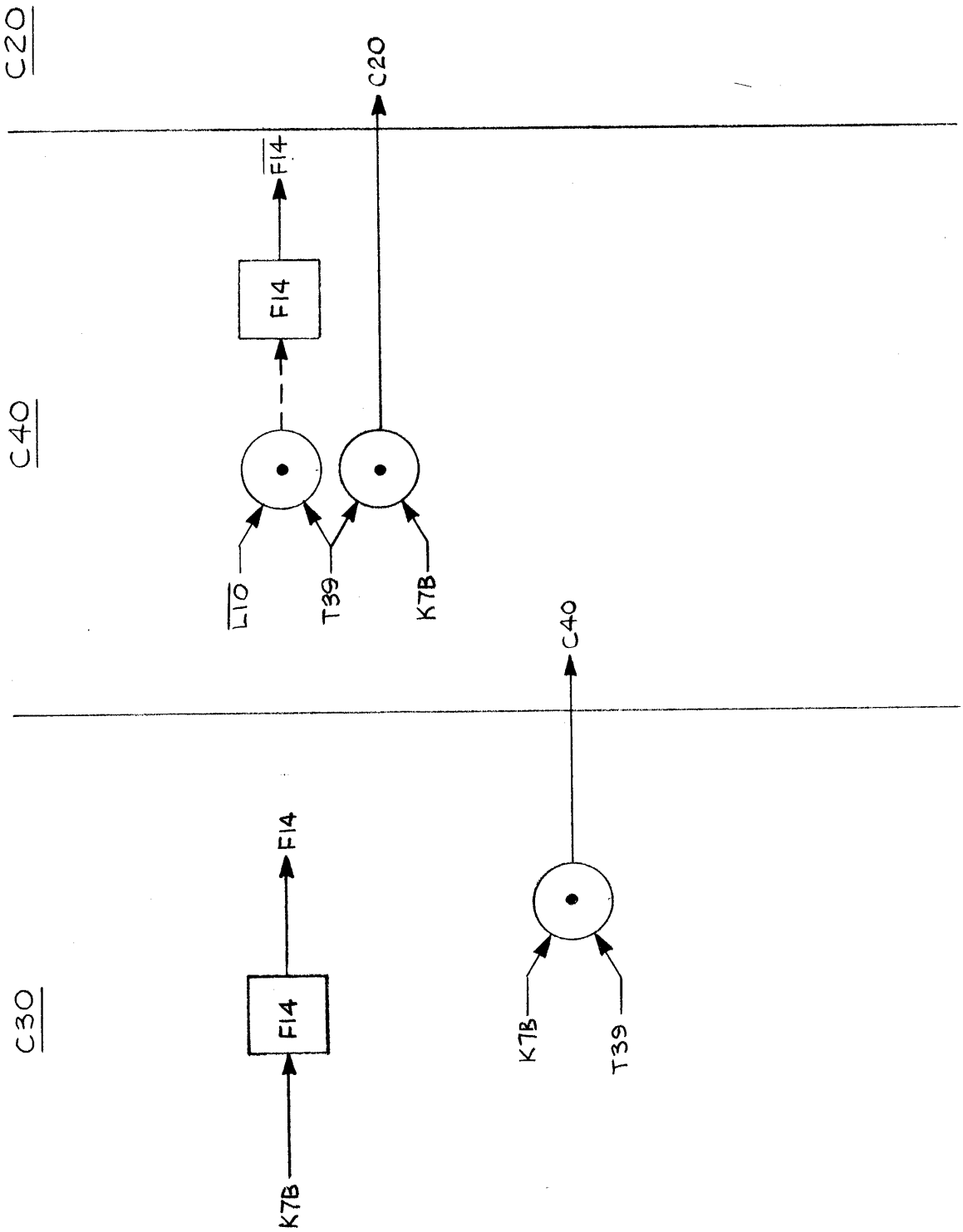


Figure 3.14 Test High Order A Bit Command and Test for Negative Command, Flow Chart.

3.7.12 RESET K TO O COMMAND (RK)

Hex Code:	13	Logic Name:	K7E
Binary Code:	0001 0011	Timing:	3

Description

This command forces K (F14) to reset, regardless of its prior state. Figure 3.15 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30:
   1) Set F14 via gate M109-6, figure 3.68.
   2) Set C40 at T39 via gate M33-6, figure 3.55.

B) During C40:
   1) Reset F14 via gate M94-6, figure 3.66.
   2) Set C20 at T39 via gates M25-8, figure 3.54, and M13-9, figure 3.55.

Decoded Signals

A11 = F5 $\overline{F7}$ M6
A18 = F7 $\overline{F8}$
K5 = A11 A18 $\overline{F6}$

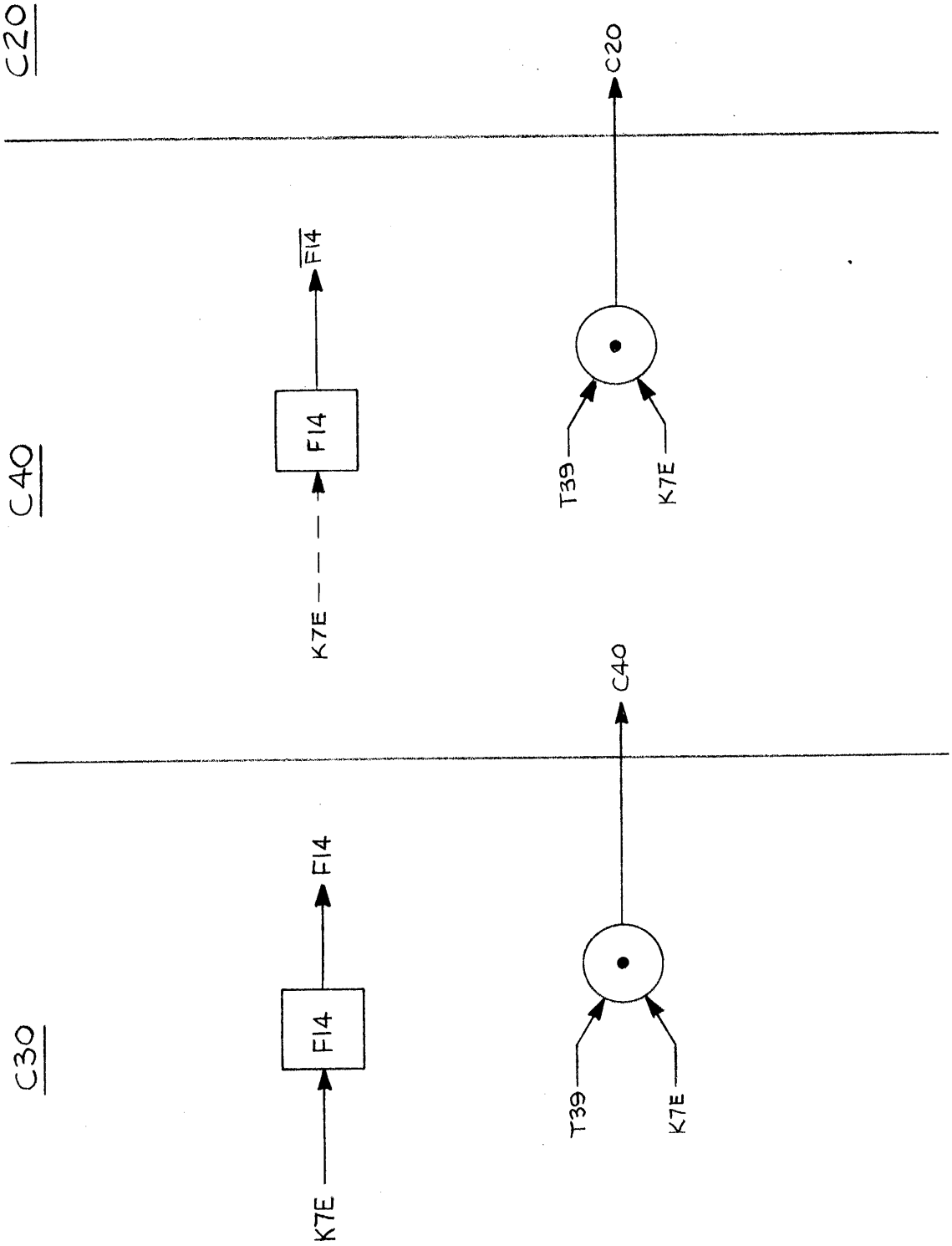


Figure 3.15 Reset K to 0 Command, Flow Chart.

3.7.13 TEST PARITY FAILURE COMMAND (TP)

Hex Code:	14	Logic Name:	K7F
Binary Code:	0001 0100	Timing:	3

Description

This command forces K (F14) to set if P (F12) is set. P is set by a parity failure or, depending upon the input data and the contents of the A, execution of the Shift Input Command. Upon completion of this command, P is reset. Figure 3.16 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30:
   1) Set F14 via M109-6, figure 3.68.
   2) Set C40 at T39 via gate M33-6, figure 3.55.

B) During C40:
   1) Reset F14 if $\overline{F12}$ via gate M94-9, figure 3.66.
   2) Reset F12 at T39 via gate M105-9, figure 3.65.
   3) Set C20 at T39 via gates M25-8, figure 3.54, and M13-9, figure 3.55.

Decoded Signals

A5 = $\overline{F8}$ $\overline{F7}$ M6
A19 = C49 $\overline{F3}$
A38 = F5 $\overline{F6}$
K7 = A5 A38 C40

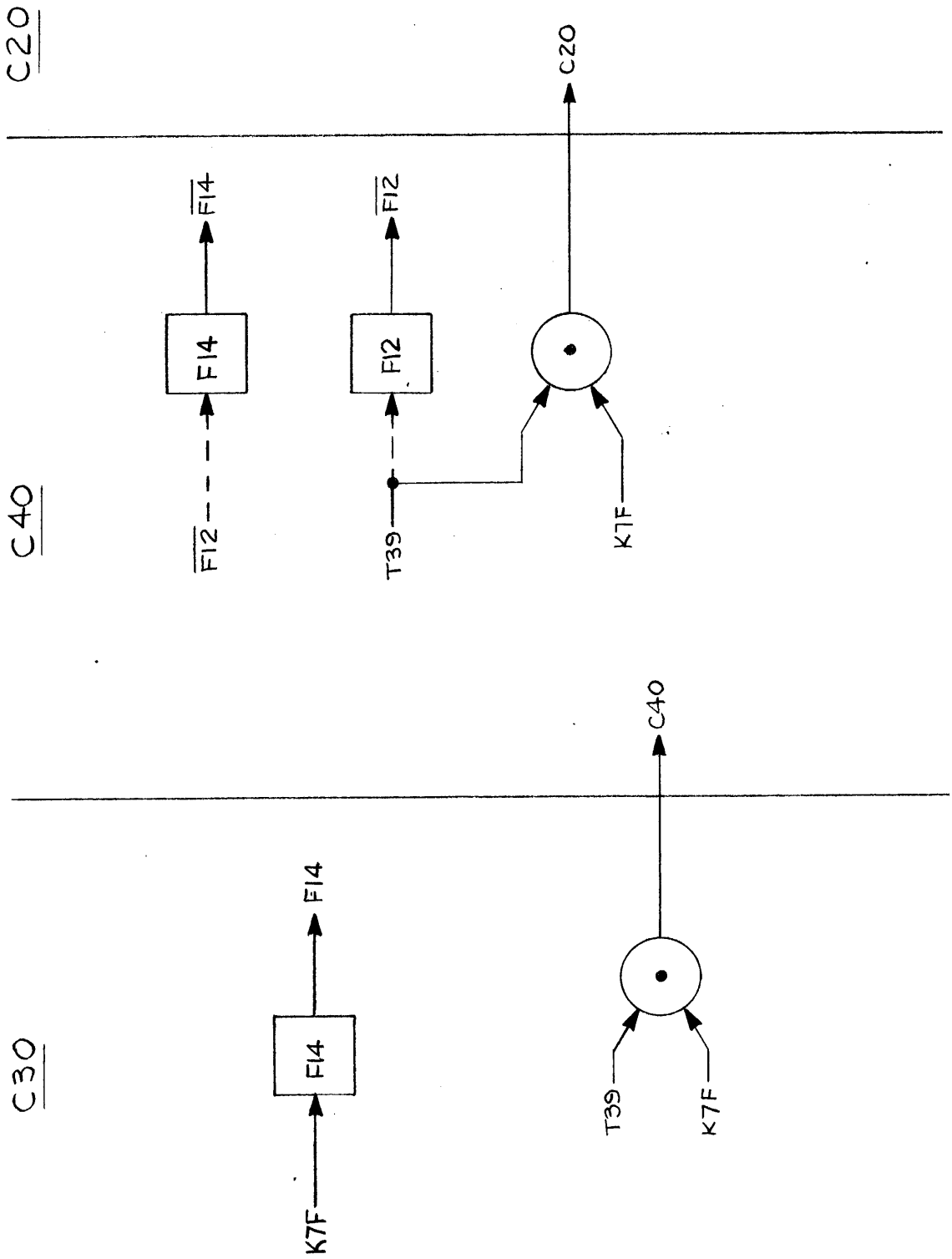


Figure 3.16 Test Parity Failure Command, Flow Chart.

3.7.14 LOGICAL AND COMMAND (LA)

Hex Code:	18+S	Logic Name:	K7C
Binary Code:	0001 1SSS	Timing:	3+sa

Description

This command causes the contents of the S to be "anded" together with the contents of the A. The results are recorded back into the A. If at any time during this operation the result equals 1, K (F14) is reset; otherwise K is set. Figure 3.17 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30:
   1) Set F14 via gate M109-6, figure 3.68.
   2) Reset F11 at $\overline{T4}$ $\overline{T7}$ via gate M70, figure 3.65.
   3) Shift during $\overline{T4}$ T7 time F3 to F2, F2 to F1, F1 to F3, ... until F3 is shifted back into F3 via gates M2, M75-8, M64-3, M64-9 in figure 3.58, and M73-8, M73-6 in figure 3.59.
   4) Set F11 if F1 $\neq$ Z3 during $\overline{T4}$ T7 via gates M69-2 and M69-4, figure 3.64.
   5) Set C40 at T39 if $\overline{F11}$ via gate M32-6, figure 3.55.

B) During C40:
   1) Record L10 L30 into A via gates M30-6 and M35-13, figure 3.82.
   2) Reset F14 if L10 L30 via gate M104-6, figure 3.66.
   3) Set C20 at T39 via gates M25-8, figure 3.54, and M33-13, figure 3.55.

Decoded Signals

A4 = $\overline{K22}$ v C1
A5 = $\overline{F8}$ $\overline{F7}$ M6
A14 = $\overline{C39}$ v F14 v (A11 K9)
A38 = F5 $\overline{F6}$
K7 = A5 A38 $\overline{C40}$
K22 = A5 C37 $\overline{T4}$ ($\overline{F6}$ v F4 F5)

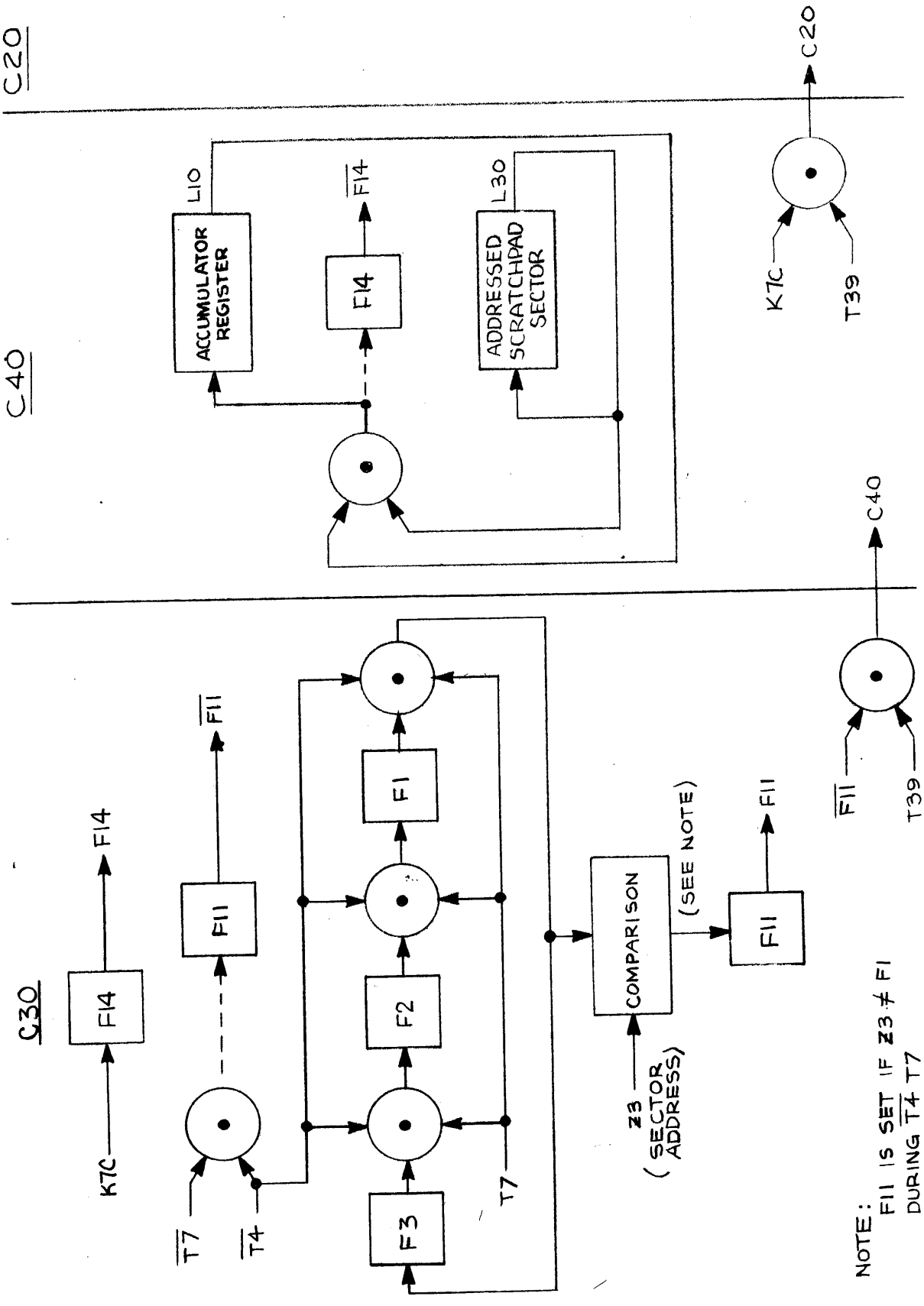


Figure 3.17 Logical And Command, Flow Chart.

3.7.15 EXCHANGE COMMAND (XC)

Hex Code:	20+S	Logic Name:	K1A
Binary Code:	0010 OSSS	Timing:	3+sa

Description

This command causes the contents of the S to be interchanged with the contents of the A. Figure 3.18 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30:
   1) Reset F11 at $\overline{T4}$ $\overline{T7}$ via gate M70, figure 3.65.
   2) Shift during $\overline{T4}$ T7 time F3 to F2, F2 to F1, F1 to F3, ... until F3 is shifted back into F3 via gates M72, M75-8, M64-3, M64-9 in figure 3.58, and M73-8, M73-6 in figure 3.59.
   3) Set F11 if F1 $\neq$ Z3 during $\overline{T4}$ T7 via gates M69-2 and M69-4, figure 3.64.
   4) Set C40 at T39 if $\overline{F11}$ via gate M32-6, figure 3.55.

B) During C40:
   1) Record L10 into S via gate M37-2, figure 3.87.
   2) Record L30 into A via gate M29, figure 3.82.
   3) Set C20 at T39 via gates M25-8, figure 3.54, and M13-9, figure 3.55.

Decoded Signals

A4 = K22 v C1
A5 = $\overline{F8}$ $\overline{F7}$ M6
A38 = F5 $\overline{F6}$
K1 = A5 $\overline{F5}$ F6 C40
K7 = A5 A38 C40
K22 = A5 C37 $\overline{T4}$ ($\overline{F6}$ v F4 F5)

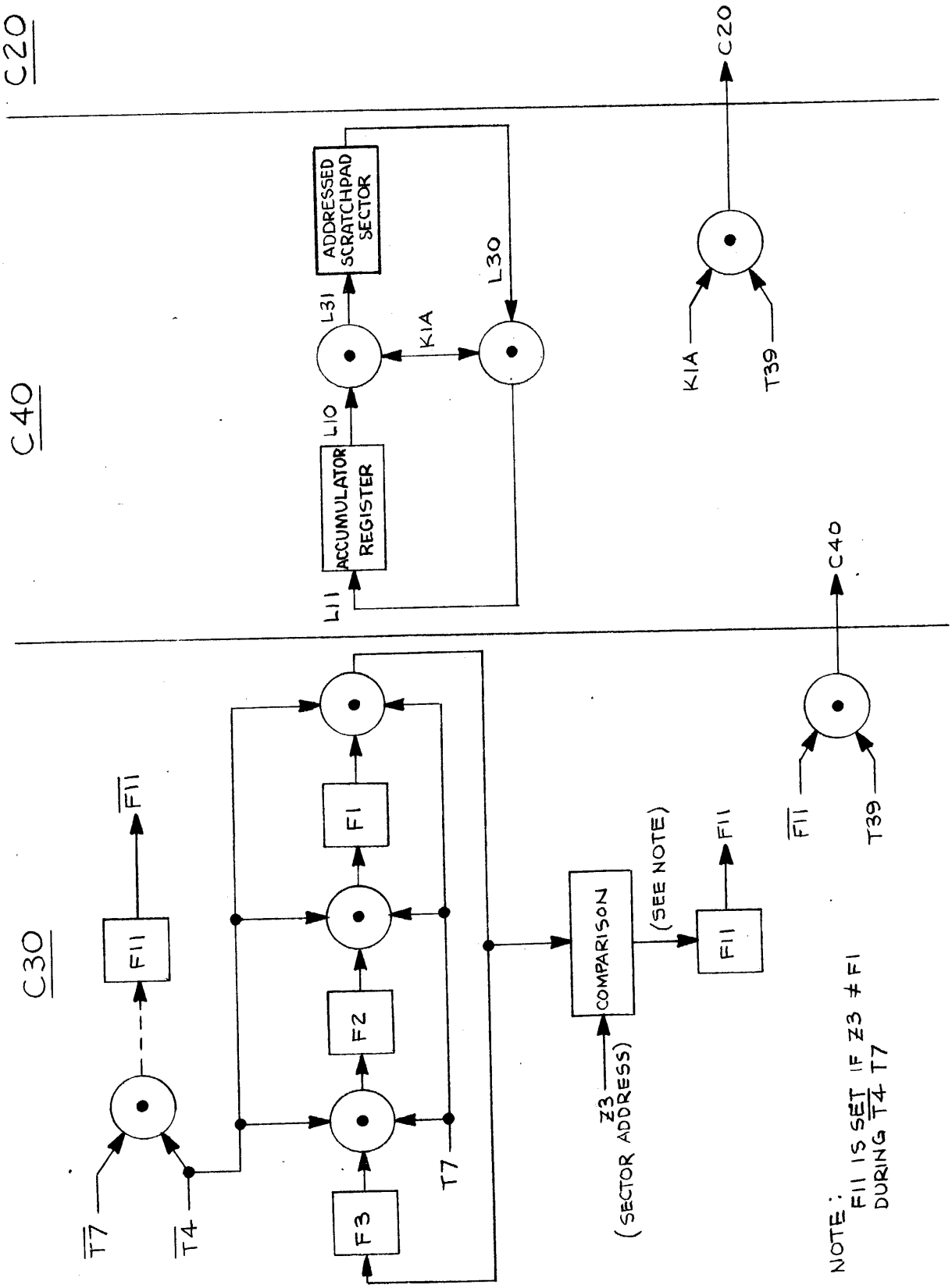


Figure 3.18 Exchange Command, Flow Chart.

3.7.16 EXTRACT COMMAND (XT)

Hex Code:	28+S	Logic Name:	K1B
Binary Code:	0010 1SSS	Timing:	3+sa

Description

This command causes the contents of the S to be "anded" together with the contents of the A, the results of which are recorded back into the A. Simultaneously, the contents of the S are "anded" together with the inverted contents of the A, the results of which are recorded back into the S. Figure 3.19 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30 see C30 of Exchange Command, steps 1 through 4, paragraph 3.7.15.

B) During C40:
   1) Record L10 and L30 into A via gates M30-6 and M35-13, figure 3.82.
   2) Record $\overline{L10}$ and L30 into S via gate M49-3, figure 3.87.
   3) Set C20 at T39 via gates M25-8, figure 3.54, and M13-9, figure 3.55.

Decoded Signals

A4 = K22 v C1
A5 = $\overline{F8}$ $\overline{F7}$ M6
A38 = F5 $\overline{F6}$
K1 = A5 $\overline{F5}$ F6 C40
K7 = A5 A38 C40
K22 = A5 C37 $\overline{T4}$ ($\overline{F6}$ v F4 F5)

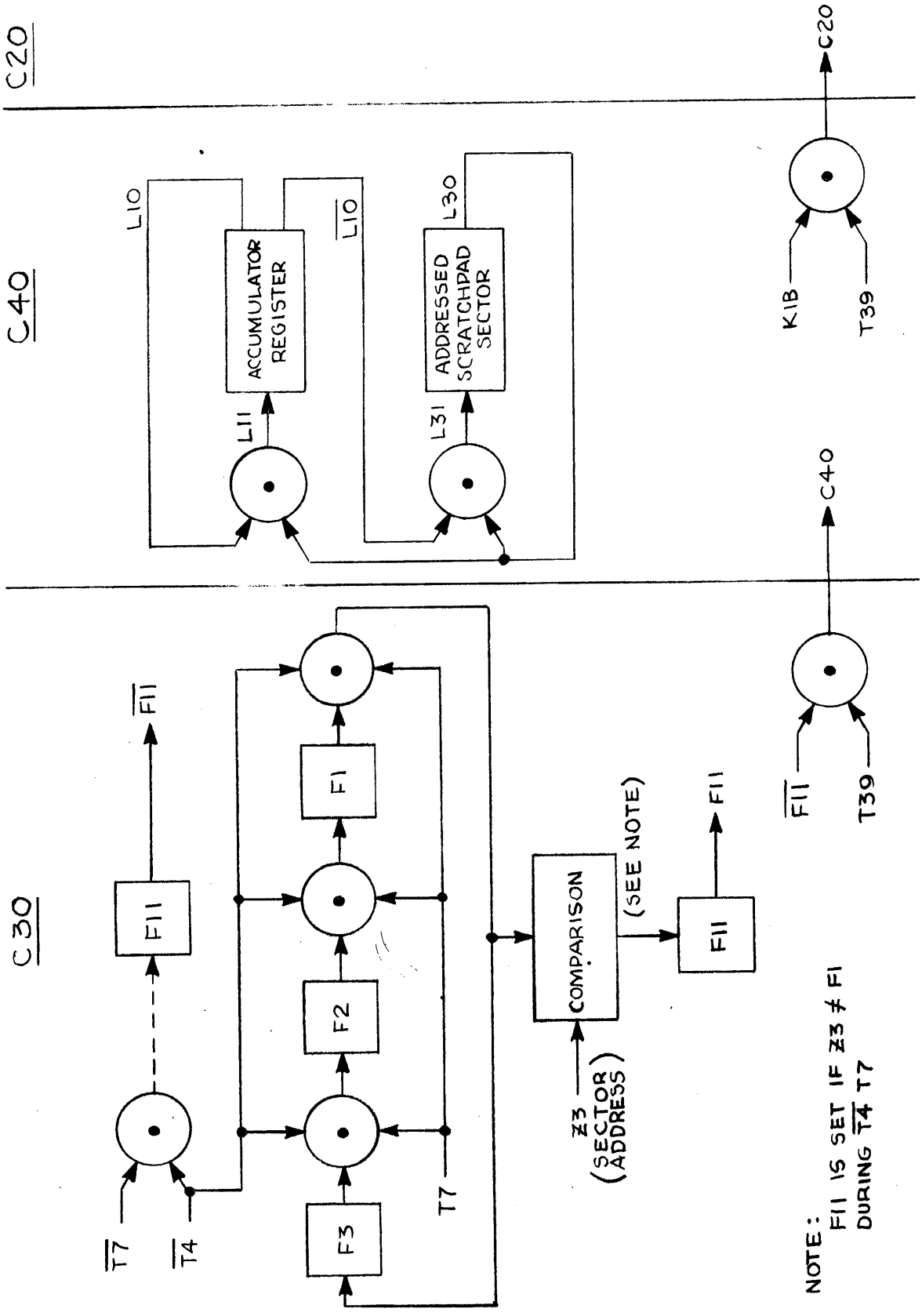


Figure 3.19 Extract Command, Flow Chart.

3.7.17 TEST EQUAL COMMAND (TE)

Hex Code:	30+S	Logic Name:	K2A
Binary Code:	0011 0SSS	Timing:	3+sa

Description

This command forces K (F14) to set if the contents of the S equals the contents of the A. If they are unequal, K is reset. Figure 3.20 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30:
   1) See C30 of Logical And Command, steps 1 through 5, paragraph 3.7.14.
   2) Reset F10 via gate M78-9, figure 3.63.

B) During C40:
   1) Establish L50 = L30 via gates M56-9, figure 3.91, and M88-4, figure 3.89.
   2) Establish L51 = L10 via gate M67-1, figure 3.90.
   3) Set L53 if L50 = L51 via gates M87-2 and M67-3, figure 3.90.
   4) Reset F14 if $\overline{L53}$ via gate M95-13, figure 3.67.
   5) Set C20 at T39 via gates M25-8, figure 3.54, and M13-9, figure 3.55.

Decoded Signals

A5 = $\overline{F8}$ $\overline{F7}$ M6
A11 = $\overline{F5}$ F7 M6
A18 = $\overline{F8}$ F7
K2 = A5 F5 F6 C40

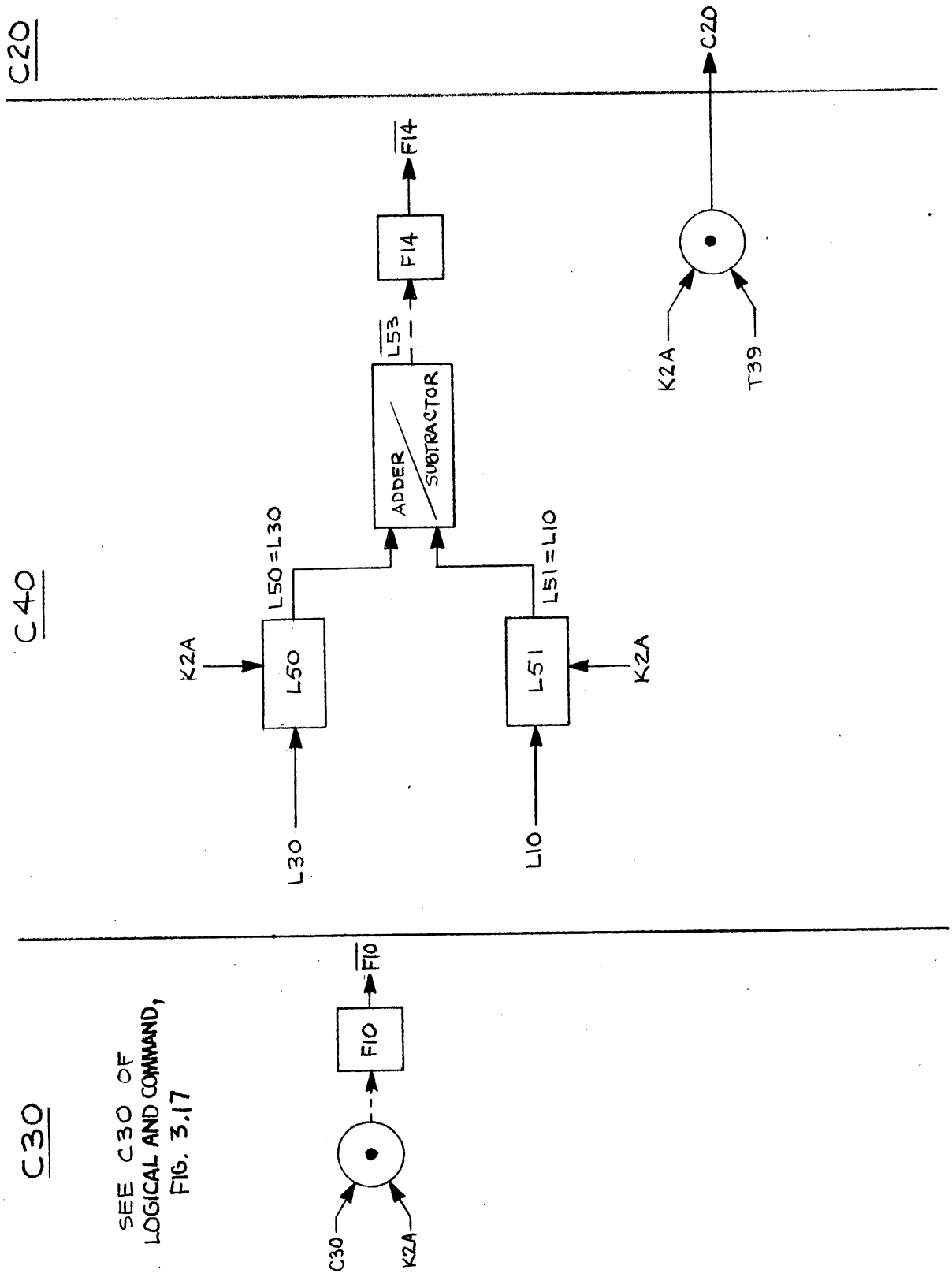


Figure 3.20 Test Equal Command, Flow Chart.

3.7.18 TEST EQUAL OR GREATER COMMAND (TG)

Hex Code:	38+S	Logic Name:	K2B
Binary Code:	0011 1SSS	Timing:	3+sa

Description

This command forces K (F14) to set if the contents of the A are equal to or greater than the contents of S. Otherwise, K is reset. Figure 3.21 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30 see C30 of Test Equal Command, steps 1 and 2, paragraph 3.7.17.

B) During C40:
   1) Establish L50 = L30 via gates M56-9, figure 3.91, and M88-4, figure 3.89.
   2) Establish L51 = $\overline{L10}$ via gate M67-1, figure 3.90.
   3) Reset F14 if L50 $\overline{L51}$ via gates M102-8 and M103-4, figure 3.67.
   4) Set C20 at T39 via gates M25-8, figure 3.54, and M13-9, figure 3.55.

Decoded Signals

A5 = $\overline{F8}$ $\overline{F7}$ M6
A11 = $\overline{F5}$ F7 M6
A18 = $\overline{F8}$ F7
K2 = A5 F5 F6 C40

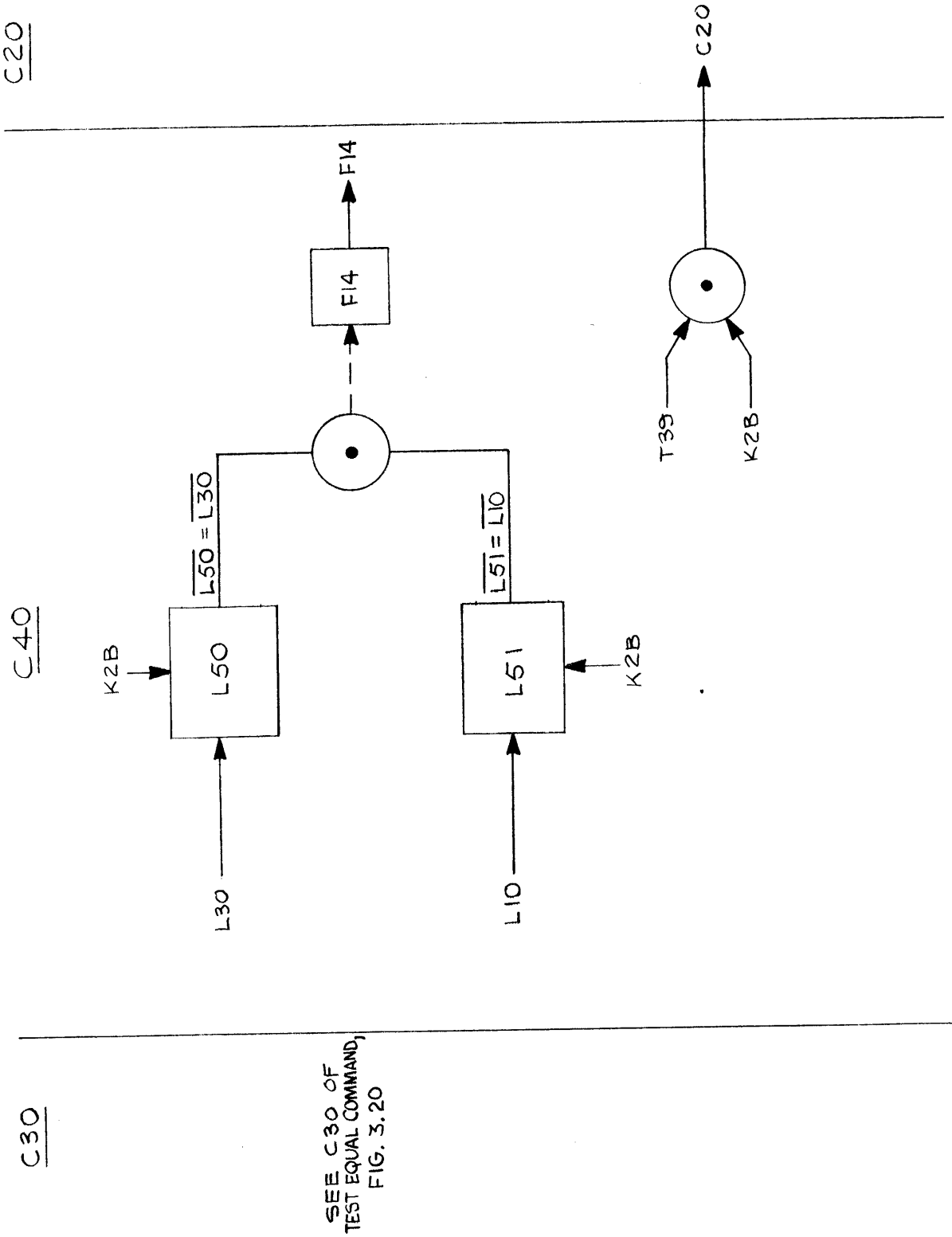


Figure 3.21 Test Equal or Greater Command, Flow Chart.

3.7.19 BINARY LEFT SINGLE SHIFT COMMAND (BLS) AND BINARY LEFT SINGLE SHIFT INCLUDING K COMMAND (BLSK)

Hex Code: 4000+N (BLS)
4080+N (BLSK)

Logic Name: K3B1 (BLS & BLSK)

Binary Code:
0100 0000 0NNN NNNN (BLS)
0100 0000 1NNN NNNN (BLSK)

Timing: 3+n (BLS & BLSK)

Description

Both commands shifts the contents of A left, the number of times specified by the shift count. N equals the shift count minus one. The last high-order bit (overflow bit) shifted out of the A is stored in K (F14). The BLSK command performs an additional operation, it forces the initial state of K into the emptied low-order A bit. Figure 3.22 is a flow chart showing the sequence of events that occur for these commands.

Sequence of Events

A) During C30:
1) Reset F14 at T39 via gate M103-9, figure 3.67.
2) Reset F9 if $\overline{F14}$ via gate M77, figure 3.62. Note that F9 is set at T39 of C20 via gate M89-8, figure 3.62, for the BLSK command.
3) Set C40 at T39 via gate M24, figure 3.55.

B) During C40:
1) Establish L53 = L10 via gates M111-5, figure 3.89, and M87-4, figure 3.90.
2) Delay L53 one bit-time by gating it through F9 via gates M89-6 and M80-11, figure 3.62.
3) Record F9 (initial state equal to 0 or F14, thereafter equal to L53 delayed one bit-time) into A via gate M35-10, figure 3.81.
4) Set F3 at time $\overline{T4}$ $\overline{T7}$ Z2 via gate M81, figure 3.59.
5) Record $\overline{L20}$ with F3 via gate M1-2, figure 3.85, into I.
6) Reset F3 if L20 during T7 via gate M73-6, figure 3.59.
7) Record L20 with $\overline{F3}$ via gate M1-4, figure 3.85, into I.
8) Store last overflow bit in F14 with F3 at T39 via gate M110-8, figure 3.68.
9) Reset F9 at T39 via gate M68-9, figure 3.62.
10) Set C10 at T39 if F3 via gate M25-8, figure 3.54.

Decoded Signals

A2 = C1 A3
A3 = $\overline{M1}$ v $\overline{S6}$ v W2
A6 = T39 $\overline{F2}$
A7 = F1 L30 v $\overline{F1}$ L10
A8 = $\overline{A2}$ $\overline{F1}$
A15 = $\overline{K40}$ $\overline{A6}$
A18 = $\overline{F8}$ F7
A39 = $\overline{F1}$ F2
K34 = K35 C40 $\overline{A39}$
K35 = A18 $\overline{F5}$ M6
K42 = K34 $\overline{F4}$
K43 = F4 K34 ($\overline{F6}$ $\overline{F9}$)

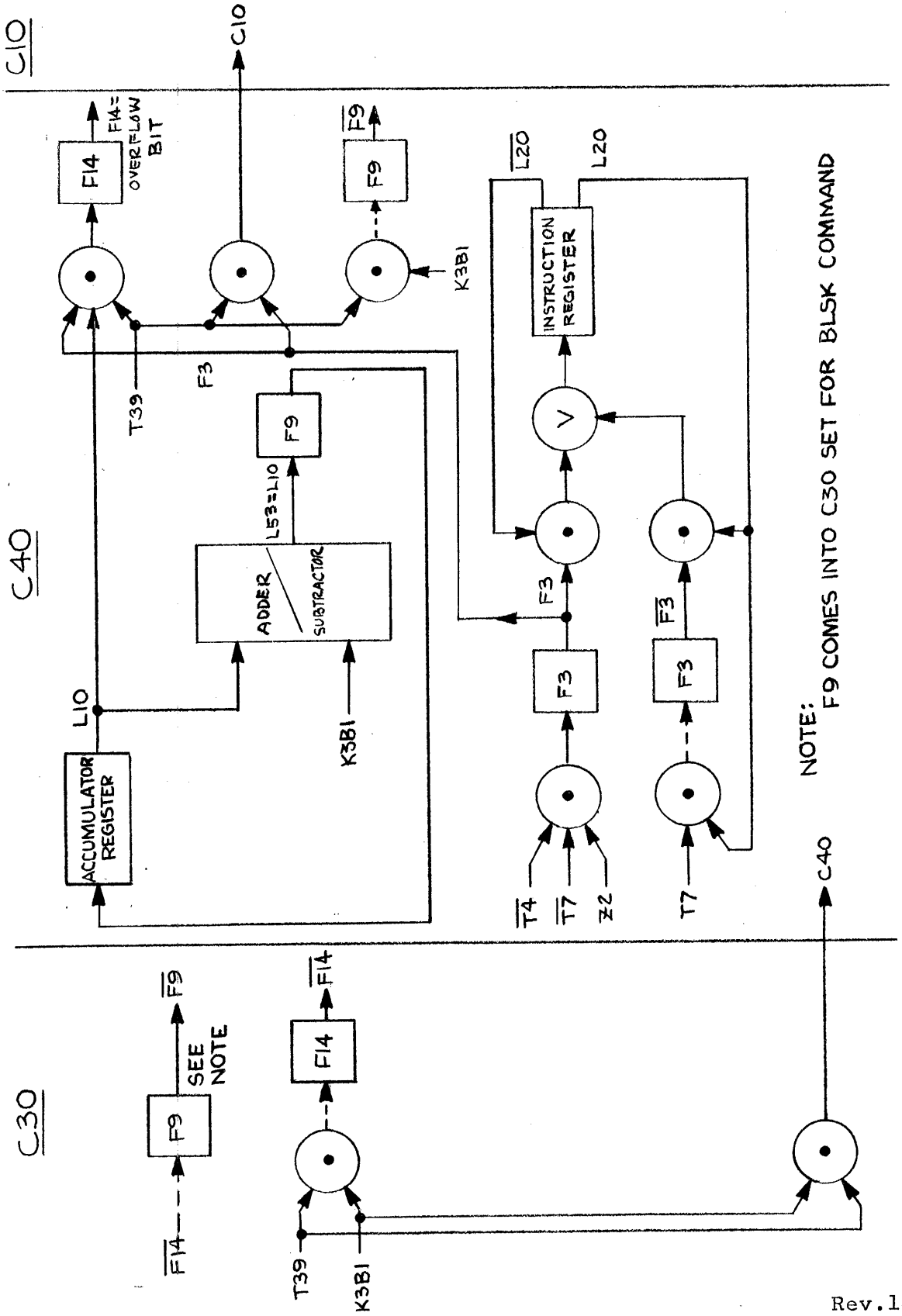


Figure 3.22 Binary Left Single Shift Command and Binary Left Single Shift Including K Command, Flow Chart.

Rev.18NOV68

ONE BIT SHIFT ONLY

3.7.20 BINARY LEFT SINGLE SHIFT ON SCRATCHPAD COMMAND (BLSS) AND BINARY LEFT SINGLE SHIFT ON SCRATCHPAD INCLUDING K COMMAND (BLSSK)

Hex Code: 4100 (BLSS)
4180 (BLSSK)

Logic Name: K3B4 (BLSS & BLSSK)

Binary Code:
0100 0001 0000 0000 (BLSS)
0100 0001 1000 0000 (BLSSK)

Timing: 4 (BLSS & BLSSK)

Description

Both commands cause the contents of whichever S happens to be available for use to shift left one bit. The high-order bit (overflow bit) shifted out of the S is stored in K (F14). The BLSSK command performs an additional operation, it forces the initial state of K into the emptied low-order S bit. Figure 3.23 is a flow chart showing the sequence of events that occur for these commands.

Sequence of Events

A) During C30 see C30 of BLS-BLSK commands, steps 1 through 3, paragraph 3.7.19.

B) During C40:
1) Establish L53 = L30 via gates M111-5, figure 3.89, and M67-6, figure 3.90.
2) Delay L53 one bit-time by gating it through F9 via gates M89-6 and M80-11, figure 3.60.
3) Record F9 (initial state equal to 0 or F14, thereafter equal to L53 delayed one bit-time) into S via gate M50-13, figure 3.87.
4) Set F3 at time $\overline{T4}$ $\overline{T7}$ Z2 via gate M81, figure 3.59.
5) Store overflow bit in F14 at T39 via gate M110-8, figure 3.68.
6) Set C10 at T39 with F3 via gate M25-8, figure 3.54.

Decoded Signals

See Decoded Signals of BLS-BLSK commands, paragraph 3.7.19.

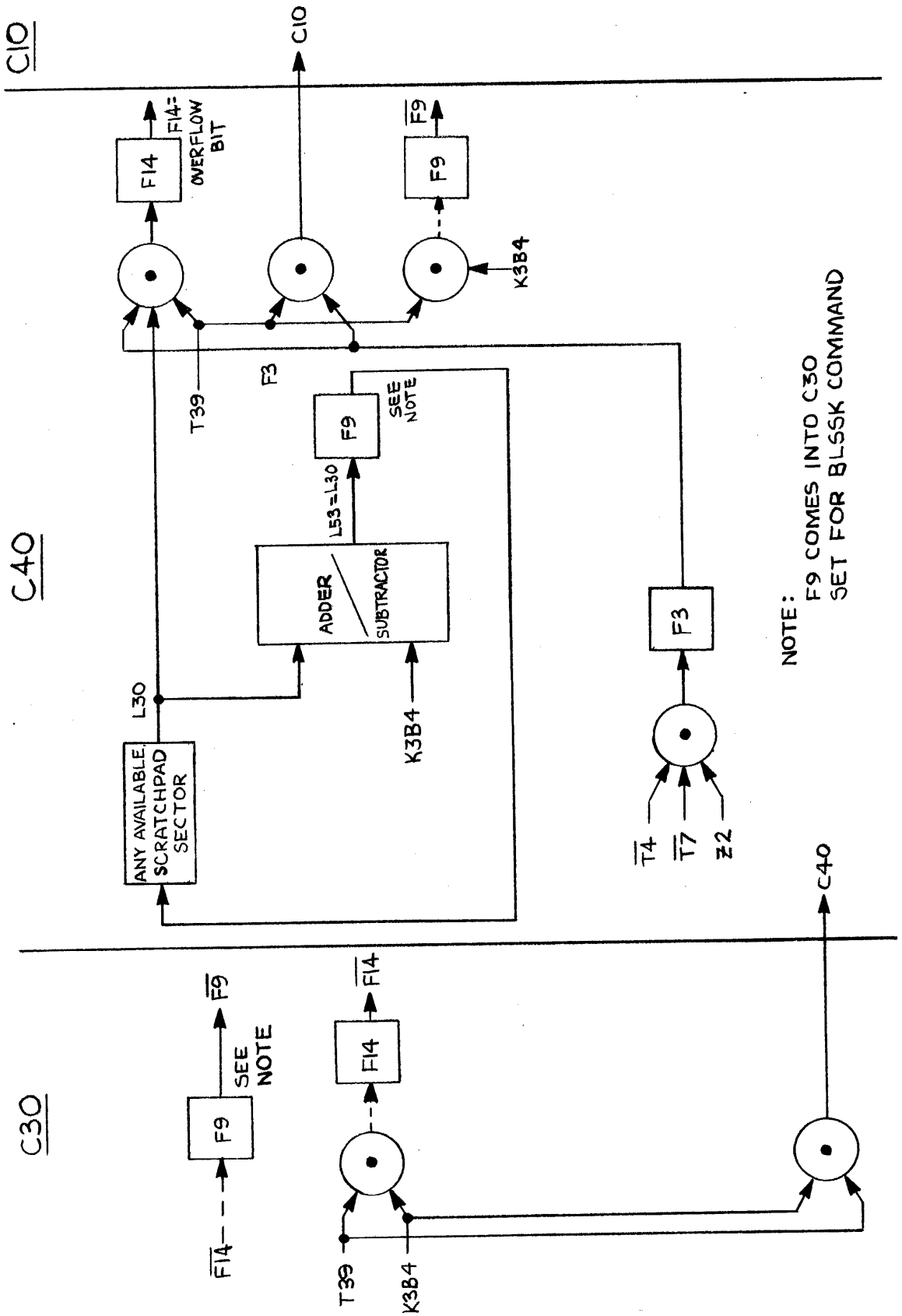


Figure 3.23 Binary Left Single Shift on Scratchpad Command and Binary Left Single Shift on Scratchpad Including K Command, Flow Chart.

3.7.21 BINARY LEFT DOUBLE SHIFT COMMAND (BLD) AND BINARY LEFT DOUBLE SHIFT INCLUDING K COMMAND (BLDK)

Hex Code: 4200+N
4280+N

Logic Name: K3B2 (BLD & BLDK)

Binary Code:
0100 0010 0NNN NNNN (BLD)
0100 0010 1NNN NNNN+N (BLDK)

Timing: 8n-3+za (BLD & BLDK)

Description

These commands causes the combined contents of scratchpad sectors 0 and 1 to shift left, as a single 80-bit block, the number of times specified by the shift count. N equals the shift count minus one. The last high-order bit (overflow bit) shifted out of the block is stored in K (F14). The BLDK command performs an additional operation, it forces the initial state of K into the emptied low-order bit of the block. Figure 3.24 is a flow chart showing the sequence of events that occur for these commands.

Sequence of Events

A) During C30:
1) Reset F9 if $\overline{F14}$ via gate M77, figure 3.62. Note that F9 is set at T39 of C20 via gate M89-8, figure 3.62, for the BLDK command.
2) Reset F14 at T39 via gate M103-9, figure 3.67.
3) Set F1 if Z3 at T39 via gate M65, figure 3.58.
4) Set C40 at T39 via gate M24, figure 3.55.

B) During C40:
1) Set F1 if Z3 at T39 via gate M65, figure 3.58.
2) Establish L53 = L30 via gates M111-5, figure 3.89, and M67-6, figure 3.90.
3) Delay L53 one bit-time by gating it through F9 via gates M89-6 and M80-11, figure 3.62.
4) Record F9 (initial state equal to 0 or F14, thereafter equal to L53 delayed one bit-time) into S if F1 via gate M50-13, figure 3.87.
5) Reset F2 if F1 $\overline{F2}$ at T39 via gate M75-8, figure 3.58.
6) Set F3 if $\overline{F2}$ at $\overline{T4}$ $\overline{T7}$ Z2 via gate M81, figure 3.59.
7) Record $\overline{L20}$ with F3 via gate M1-2, figure 3.85, into I.
8) Reset F3 if L20 during T7 via gate M73-6, figure 3.59.
9) Record L20 with $\overline{F3}$ via gate M1-4, figure 3.85, into I.

10) Store last overflow bit in F14 with F3 at T39 via gate M110-8, figure 3.68.
11) Reset F9 at T39 if $\overline{F2}$ via gate M68-9, figure 3.62.
12) Set F2 if F1 $\overline{F2}$ at T39 via gate M72, figure 3.58.
13) Reset F1 if $\overline{F2}$ at T39 via gate M64-9, figure 3.58.
14) Set C10 at T39 if F3 via gate M25-6, figure 3.54.

Decoded Signals

See Decoded Signals of BLS-BLSK commands, paragraph 3.7.19.

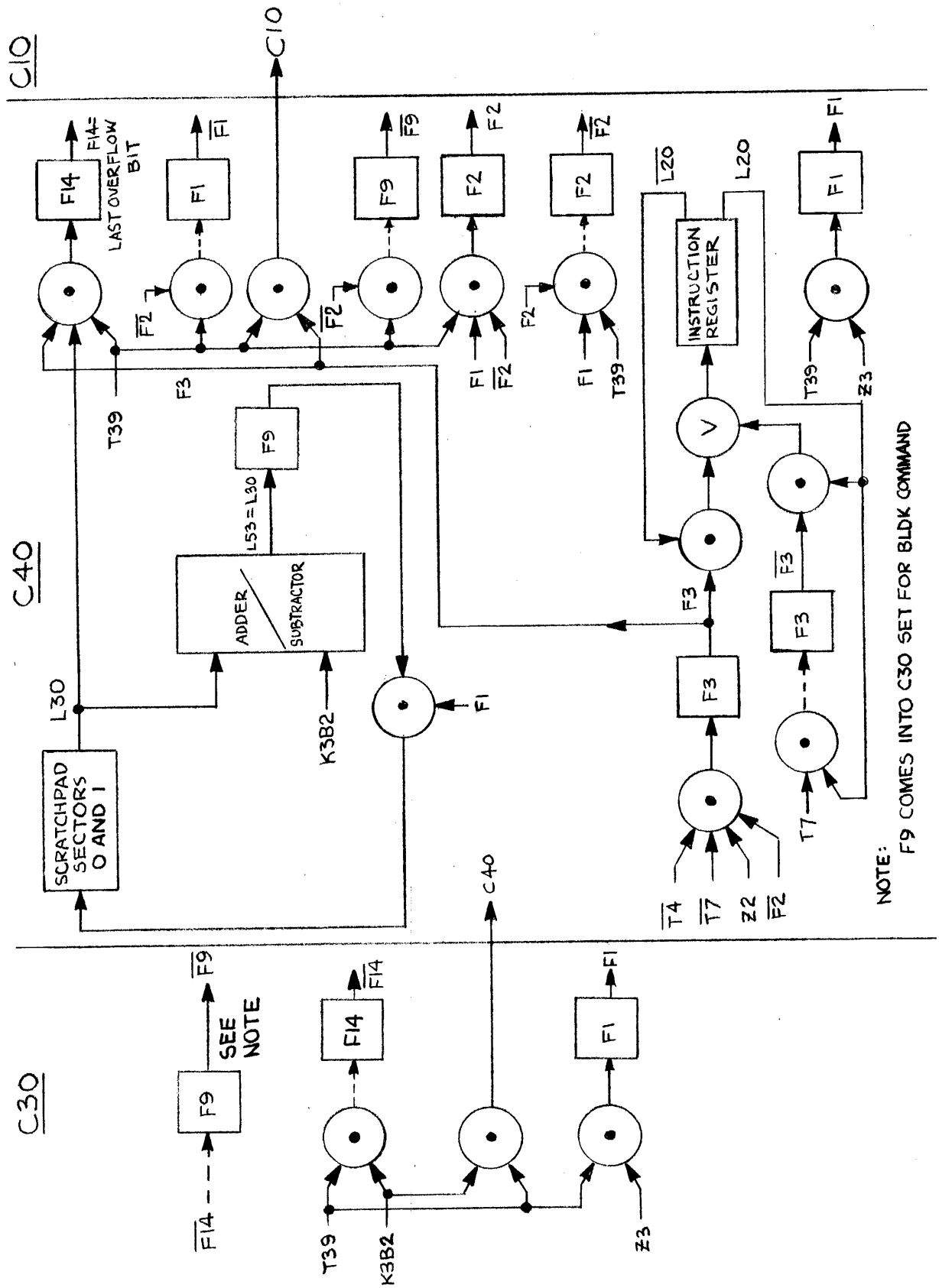


Figure 3.24 Binary Left Double Shift Command and Binary Left Double Shift Including K Command, Flow Chart

3.7.22 BINARY LEFT DOUBLE SHIFT ON SCRATCHPAD COMMAND (BLDS) AND BINARY LEFT DOUBLE SHIFT ON SCRATCHPAD INCLUDING K COMMAND (BLDSK)

Hex Code: 4300 (BLDS) Logic Name: K3B3 (BLDS & BLDSK)
4380 (BLDSK)

Binary Code:
0100 0011 0000 0000 (BLDS) Timing: 5 (BLDS & BLDSK)
0100 0011 1000 0000 (BLDSK)

Description

These commands cause the combined contents of whichever 2 scratchpad sectors happen to be available for use to shift left one bit as a single 80-bit block of information. The high-order bit (overflow bit) shifted out of the block is stored in K (F14). The BLDSK command performs an additional operation, it forces the initial state of K into the emptied low-order bit of the block. Figure 3.25 is a flow chart showing the sequence of events that occur for these commands.

Sequence of Events

A) During C30 see C30 of BLD-BLDK commands, steps 1, 2 and 4, paragraph 3.7.21.

B) During C40 see C40 of BLD-BLDK commands, steps 2 through 6, 8, 10, 11 and 14, paragraph 3.7.21.

Decoded Signals

See Decoded Signals of BLS-BLSK commands, paragraph 3.7.19.

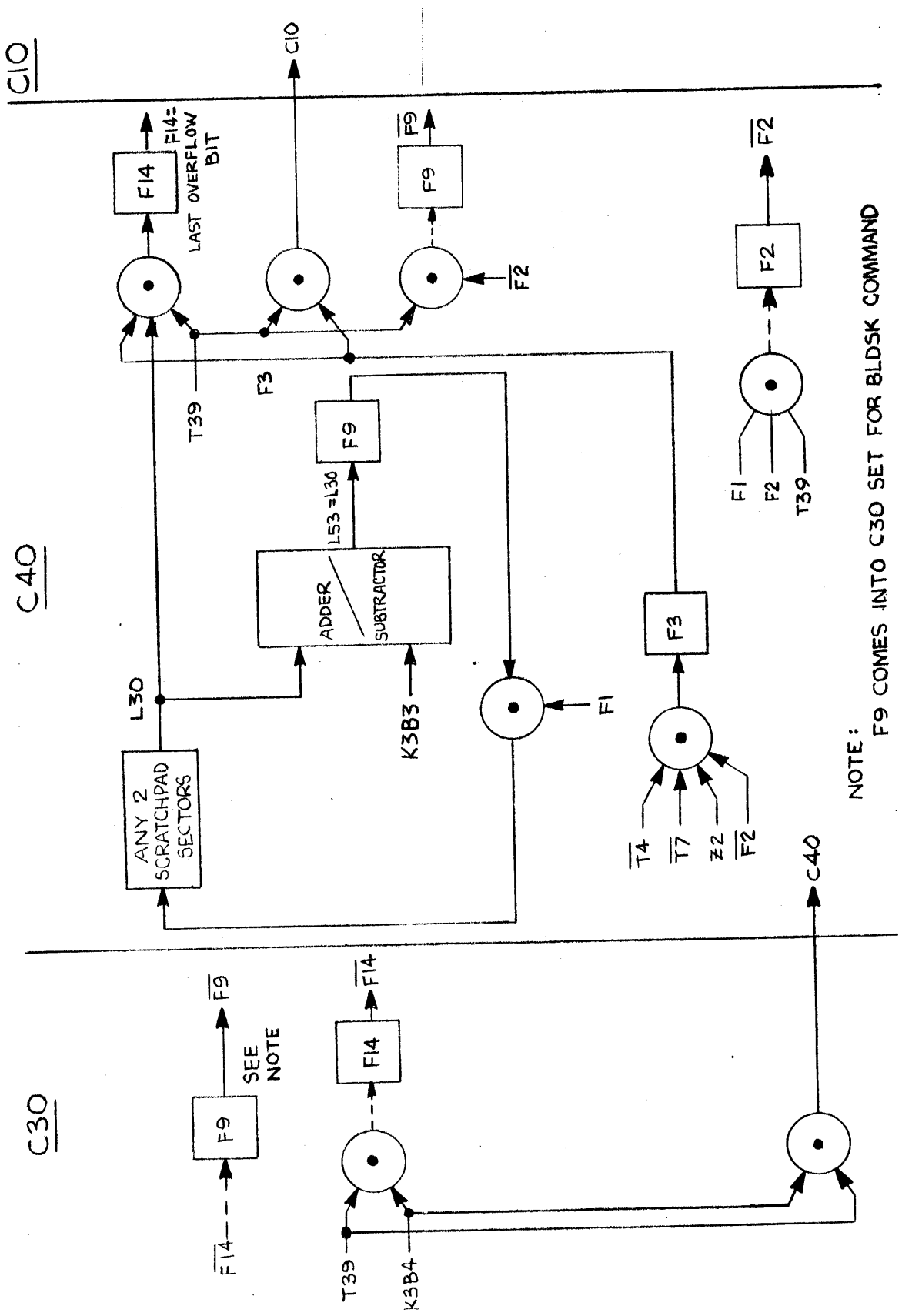


Figure 3.25 Binary Left Double Shift on Scratchpad Command and Binary Left Double Shift on Scratchpad Including K Command, Flow Chart.

3.7.23 BINARY RIGHT SINGLE SHIFT COMMAND (BRS) AND BINARY RIGHT SINGLE SHIFT INCLUDING K COMMAND (BRSK)

Hex Code: 4800+N (BRS) Logic Name: K3A1 (BRS & BRSK)
4880+N (BRSK)

Binary Code:
0100 1000 0NNN NNNN (BRS) Timing: 3+n (BRS & BRSK)
0100 1000 1NNN NNNN (BRSK)

Description

These commands shift the contents of the A right, the number of times specified by the shift count. N equals the shift count minus one. The last low-order bit (overflow bit) shifted out of the A is stored in K (F14). The BRSK command performs an additional operation, it forces the initial state of K into the emptied high-order A bits. Figure 3.26 is a flow chart showing the sequence of events that occur for these commands.

Sequence of Events

A) During C30 see C30 of BLS-BLSK commands, steps 1 through 3, paragraph 3.7.19.

B) During C40:
1) Establish $\overline{L50}$ equal to L19 $\overline{T39}$ via gates M82-3 and M75, figure 3.89.
2) Record $\overline{L50}$ v F9 T39 into A via gate M35-10, figure 3.81.
3) Don't shift L10 (low order A bit) if $\overline{T39}$ via gate M141-8, figure 3.80.
4) Set F3 at time $\overline{T4}$ $\overline{T7}$ Z2 via gate M81, figure 3.59.
5) Record $\overline{L20}$ with F3 via gate M1-2, figure 3.85, into I.
6) Reset F3 if L20 during T7 via gate M73-6, figure 3.59.
7) Record L20 with $\overline{F3}$ via gate M1-4, figure 3.85, into I.
8) Store last underflow bit in F14 with F3 at T39 via gate M110-8, figure 3.68.
9) Set C10 at T39 if F3 via gate M25-8, figure 3.54.

Decoded Signals

See Decoded Signals of BLS-BLSK commands, paragraph 3.7.19.

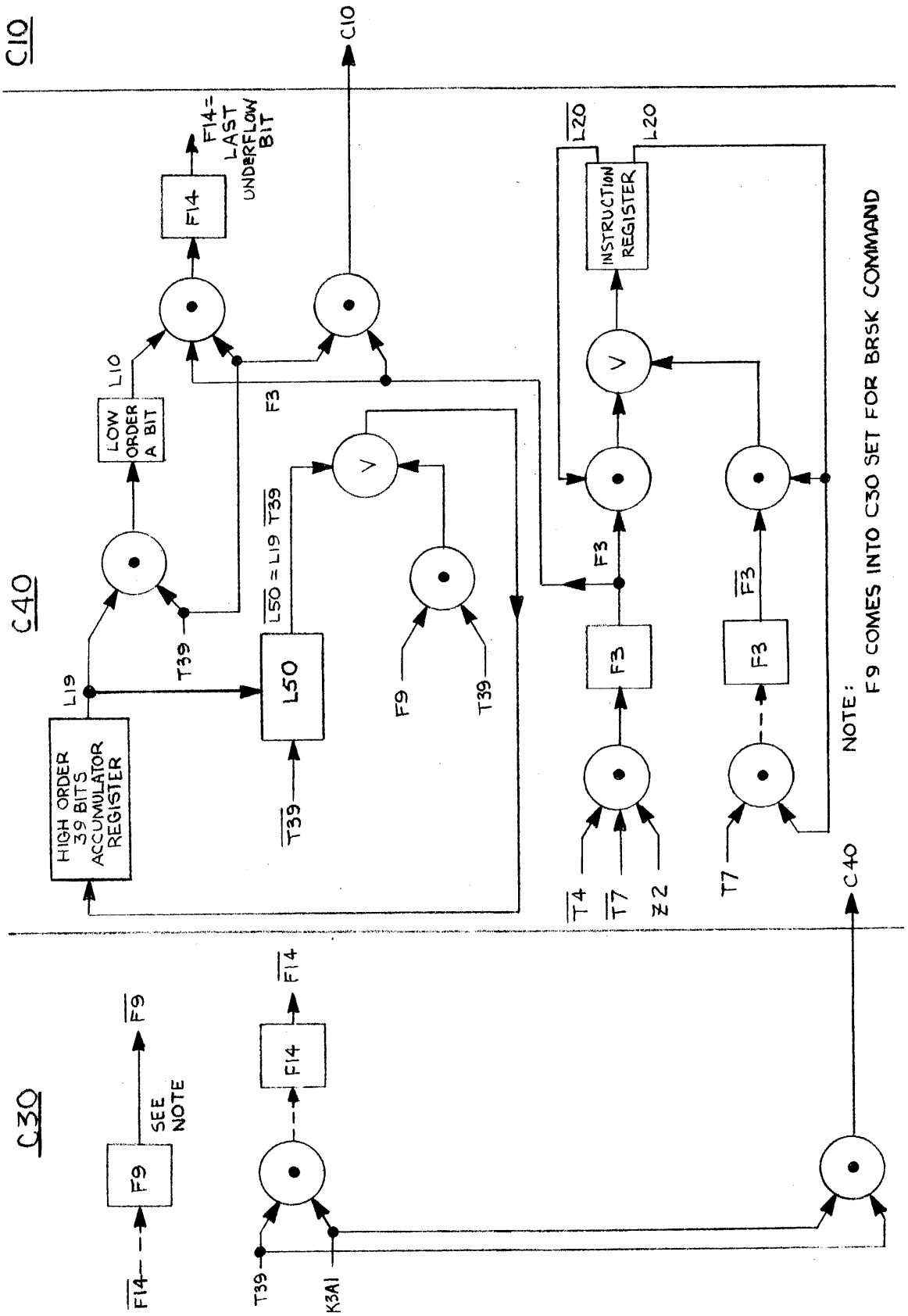


Figure 3.26 Binary Right Single Shift Command and Binary Right Single Shift Including K Command, Flow Chart.

3.7.24 BINARY RIGHT SINGLE SHIFT ON SCRATCHPAD COMMAND (BRSS) AND BINARY RIGHT SINGLE SHIFT ON SCRATCHPAD INCLUDING K COMMAND (BRSSK)

Hex Code: 4900 (BRSS) Logic Name: K3A4 (BRSS & BRSSK)
4980 (BRSSK)

Binary Code:
0100 1001 0000 0000 (BRSS) Timing: 4 (BRSS & BRSSK)
0100 1001 1000 0000 (BRSSK)

Description

These commands cause the contents of whichever S that happens to be available for use, to shift right one bit. The low-order bit (underflow bit) shifted out of the S is stored in K (F14). The BRSSK command performs an additional operation, it forces the initial state of K into the emptied high-order S bit. Figure 3.27 is a flow chart showing the sequence of events that occur for these commands.

Sequence of Events

A) During C30 see C30 of BLS-BLSK commands, steps 1 through 3, paragraph 3.7.19.

B) During C40:
1) Establish $\overline{L50}$ equal to L39 $\overline{T39}$ via gates M82-5 and M75, figure 3.89.
2) Record $\overline{L50}$ v F9 T39 into S via gate M50-13, figure 3.87.
3) Don't shift L30 if $\overline{T39}$ via gate M141-6, figure 3.86.
4) Set F3 at time $\overline{T4}$ $\overline{T7}$ Z2 via gate M81, figure 3.59.
5) Store underflow bit in F14 with F3 at T39 via gate M110-8, figure 3.68.
6) Set C10 at T39 with F3 via gate M25-8, figure 3.54.

Decoded Signals

See Decoded Signals of BLS-BLSK commands, paragraph 3.7.19.

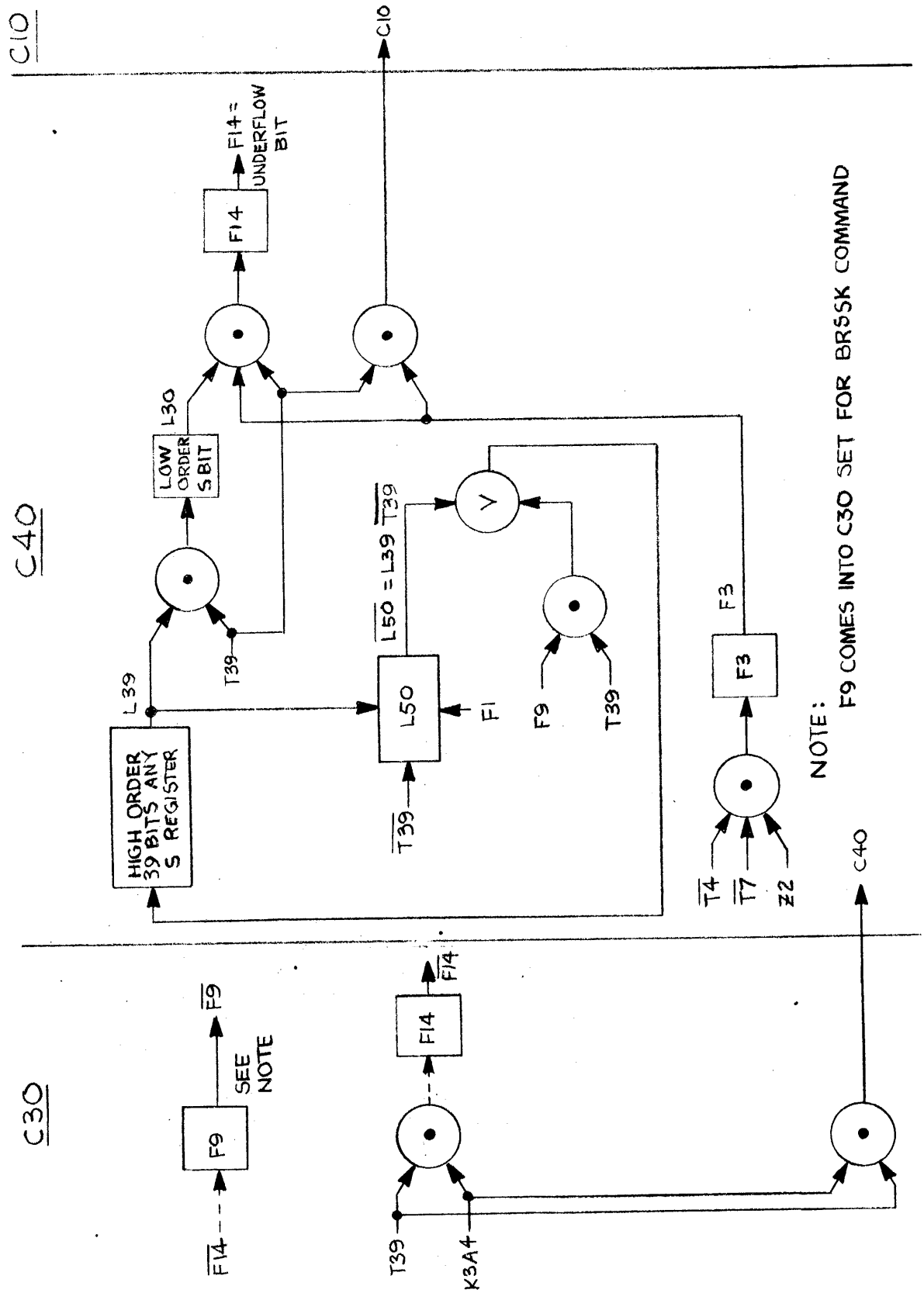


Figure 3.27 Binary Right Shift on Scratchpad Command and Binary Right Shift on Scratchpad Including K Command, Flow Chart.

3.7.25 BINARY RIGHT DOUBLE SHIFT COMMAND (BRD) AND BINARY RIGHT DOUBLE SHIFT INCLUDING K COMMAND (BRDK)

Hex Code: 4A00+N (BRD) Logic Name: K3A2
4A80+N (BRDK)

Binary Code:
0100 1010 0NNN NNNN (BRD) Timing: 8n-3+za (BRD & BRDK)
0100 1010 1NNN NNNN (BRDK)

Description

These commands cause the combined contents of scratchpad sectors 0 and 1 to shift right, as a single 80-bit block, the number of times specified shift count. N equals the shift count minus one. The low-order bit (underflow bit) shifted out of the block is stored in K (F14). The BRDK command performs an additional operation, it forces the initial state of K into the emptied high-order bits of the block. Figure 3.28 is a flow chart showing the sequence of events that occur for these commands.

Sequence of Events

A) During C30 see C30 of BLD-BLDK commands, steps 1 through 4, paragraph 3.7.21.

B) During C40:
1) Set F1 if Z3 at T39 via gate M65, figure 3.58.
2) Establish $\overline{L50}$ equal to L39 ($\overline{T39}$ v F2) if F1 via gates M82-5 and M75, figure 3.89.
3) Record $\overline{L50}$ v F9 $\overline{F2}$ T39 into S if F1 via gate M50-13, figure 3.87.
4) Don't shift L30 if F1 (F2 v $\overline{T39}$) via gate M141-6, figure 3.86.
5) Reset F2 if F1 F2 at T39 via gate M75-8, figure 3.58.
6) Set F3 if $\overline{F2}$ at time $\overline{T4}$ $\overline{T7}$ Z2 via gate M81, figure 3.59.
7) Record $\overline{L20}$ with F3 via gate M1-2, figure 3.85, into I.
8) Reset F3 if L20 during T7 via gate M73-6, figure 3.59.
9) Record L20 with $\overline{F3}$ via gate M1-4, figure 3.85, into I.
10) Store last underflow bit in F14 with F3 at T39 via gate M110-8, figure 3.68.
11) Set F2 if F1 $\overline{F2}$ at T39 via gate M72-12, figure 3.58.
12) Reset F1 if $\overline{F2}$ at T39 via gate M64-9, figure 3.58.
13) Set C10 at T39 if F3 via gate M25-6, figure 3.54.

Decoded Signals

See Decoded Signals of BLS-BLSK commands, paragraph 3.7.19.

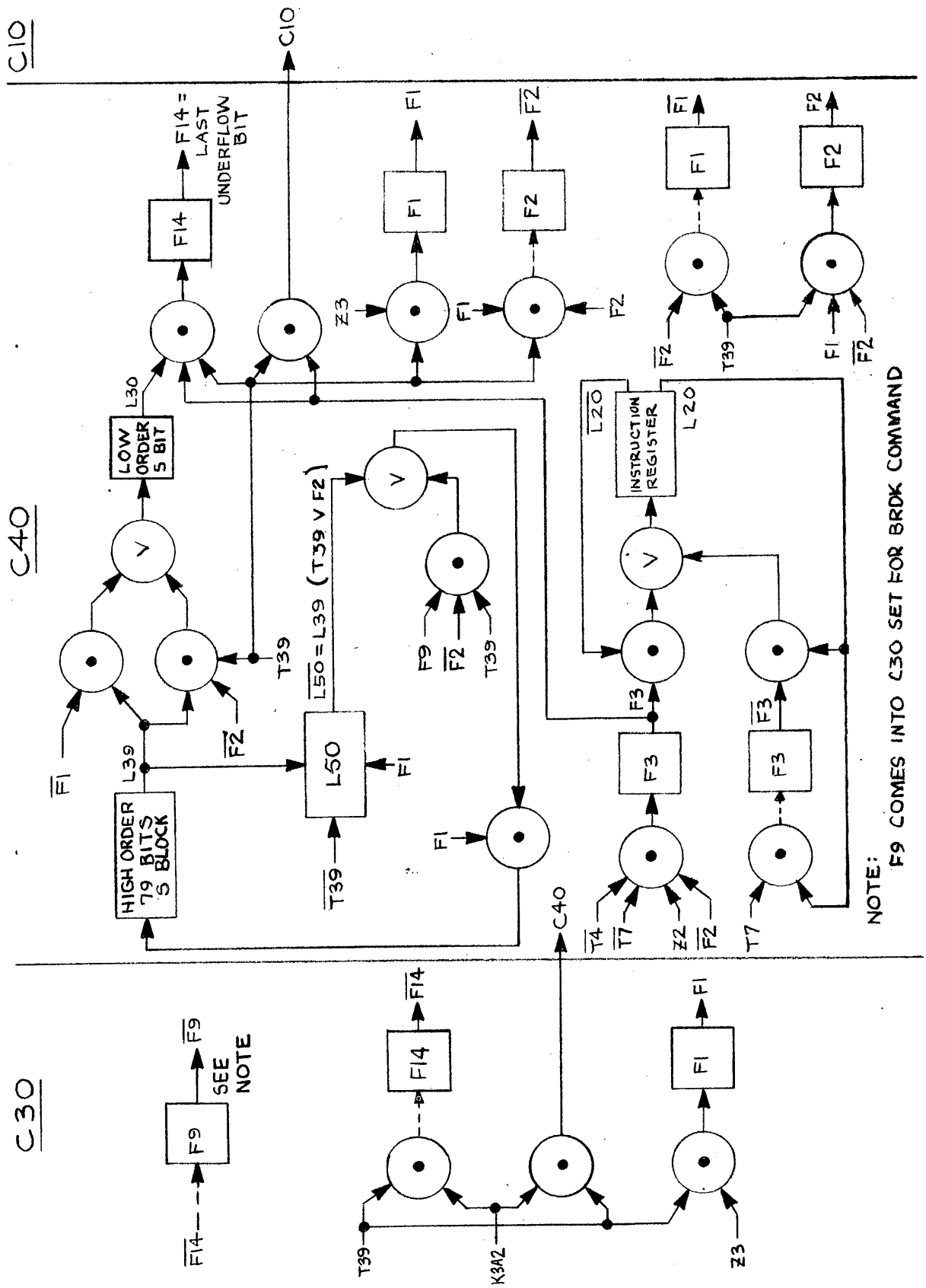


Figure 3.28 Binary Right Double Shift Command and Binary Right Double Shift Including K Command, Flow Chart.

3.7.26 BINARY RIGHT DOUBLE SHIFT ON SCRATCHPAD COMMAND (BRDS) AND BINARY RIGHT DOUBLE SHIFT ON SCRATCHPAD INCLUDING K COMMAND (BRDSK)

Hex Code: 4B00 (BRDS) 4B80 (BRDSK)

Logic Name: K3A3 (BRDS & BRDSK)

Binary Code:
0100 1011 0000 0000 (BRDS)
0100 1011 1000 0000 (BRDSK)

Timing: 5 (BRDS & BRDSK)

Description

These commands cause the combined contents of whichever 2 scratchpad sectors happen to be available for use to shift right one bit as a single 80-bit block of information. The low-order bit (underflow bit) shifted out of the block is stored in K (F14). The BRDSK command performs an additional operation, it forces the initial state of K into the emptied high-order bit of the block. Figure 3.29 is a flow chart showing the sequence of events that occur for these commands.

Sequence of Events

A) During C30 see C30 BLS-BLSSK commands, steps 1 through 3, paragraph 3.7.19.

B) During C40 see C40 of BRD-BRDK commands, steps 2 through 6, 10, and 13, paragraph 3.7.25.

Decoded Signals

See Decoded Signals of BLS-BLSK commands, paragraph 3.7.19.

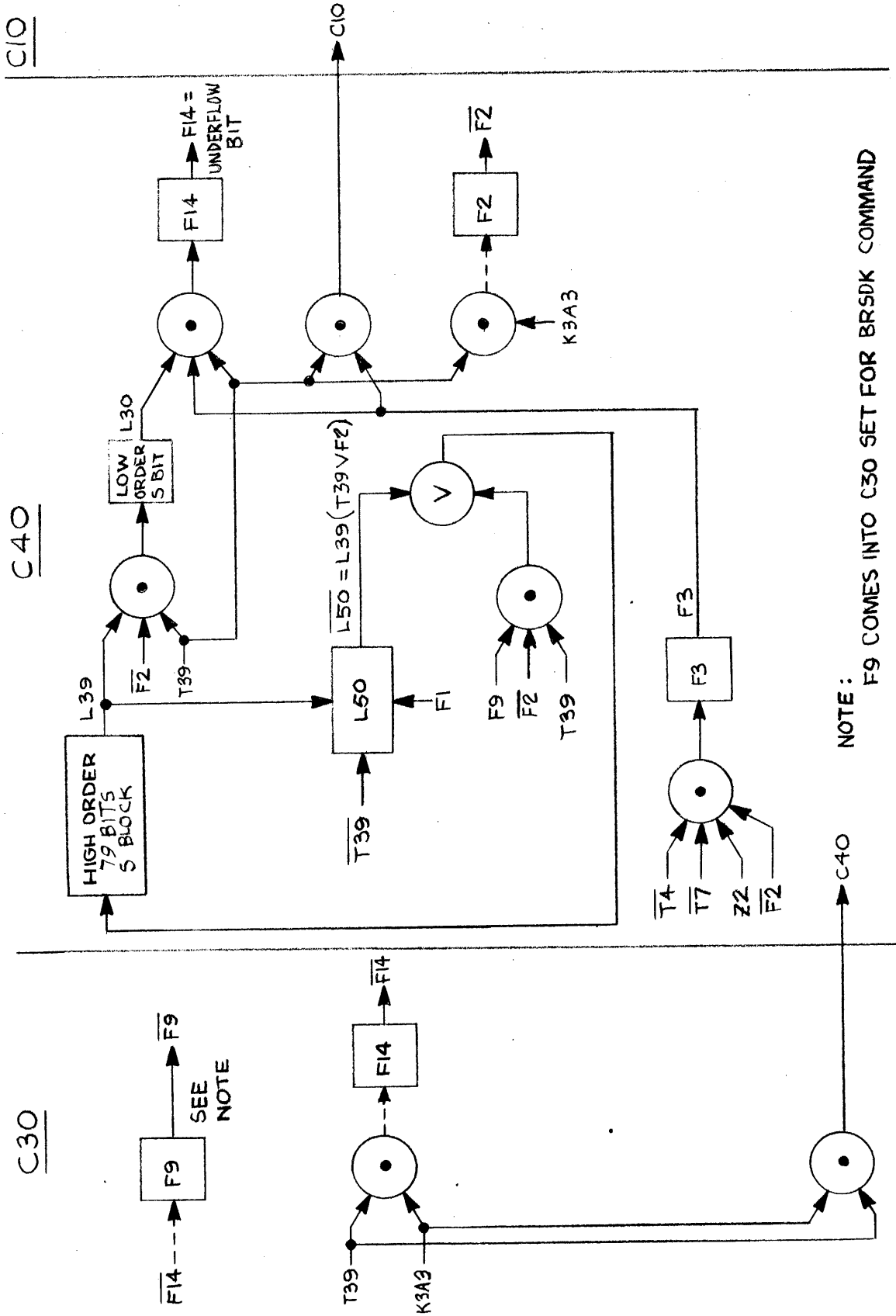


Figure 3.29 Binary Right Double Shift on Scratchpad Command and Binary Right Double Shift on Scratchpad Including K Command, Flow Chart.

3.7.27 SHIFT INPUT COMMAND (SI)

Hex Code:	5000	Logic Name:	K5A
Binary Code:	0101 0000 0000 0000	Timing:	4 (3)

Description

This command causes K (F14) to set if a selected input device does not present a Busy signal during T7 of C30. The B is then parallel-loaded with an 8-bit input character from the selected device. The input character is then serially shifted out of the B into the low-order 8 A bits, 0-7. Simultaneously, the high-order 8 A bits are shifted into the B. Note that, depending upon the input data and the contents of the A, the execution of this command may set P (F12). If a Busy signal had been present during T7 of C30, this command is aborted and K reset. Figure 3.30 is a flow chart showing the sequence of events that occur for this command. Figure 1.3 shows the orientation of the input bits to the B and A.

Sequence of Events

A) During C20:
   1) Reset F9 with A2, $\overline{\text{F101}}$ via M68-1, figure 3.62.
   2) Set C30 at T39 via gate M14-9, figure 3.54.

B) During C30:
   1) Reset F11 via gate M70, figure 3.65.
   2) Ask selected input device for character by generating $\overline{\text{K83}}$ via gate M116-8, figure 3.78.
   3) Set F14 at $\overline{\text{T7}}$ via gate M111-9, figure 3.68.
   4) Reset F14 at T7 if K75, Busy signal, via gate M107-9, figure 3.66.
   5) Parallel-load B at T39 if F14 via gates M117-3, 6, 8, 11, and M115-3, 6, 8, 11, figure 3.70 and 3.71.
   6) Set C40 at T39 if F14 via gate M33-6, figure 3.55.
   7) Set C10 at T39 if $\overline{\text{F14}}$ via gates M25-6, figure 3.54, and M33-6, figure 3.55.

C) During C40:
   1) Precess contents of B to low-order A via gate M46-1, figure 3.81, while precessing high-order 8 bits of A into B via gate M125-4, figure 3.70.
   2) Send Clear signal (K150) via gate M116-6, figure 3.79, to selected input device.
   3) Set C10 at T39 via gate M25-6, figure 3.54.

K=1 ⇒ EXECUTED OK
K=0 = ABORTED

Rev.18NOV68

Decoded Signals

A6 = T39 $\overline{\overline{F2}}$
A11 = F5 F7 M6
A14 = $\overline{\overline{C39}}$ v F14 ($\overline{\overline{A11}}$ K9)
A18 = $\overline{\overline{F8}}$ F7
K5 = A18 A11 $\overline{\overline{F6}}$
K50 = K5 C40
K51 = K5 C39 F14

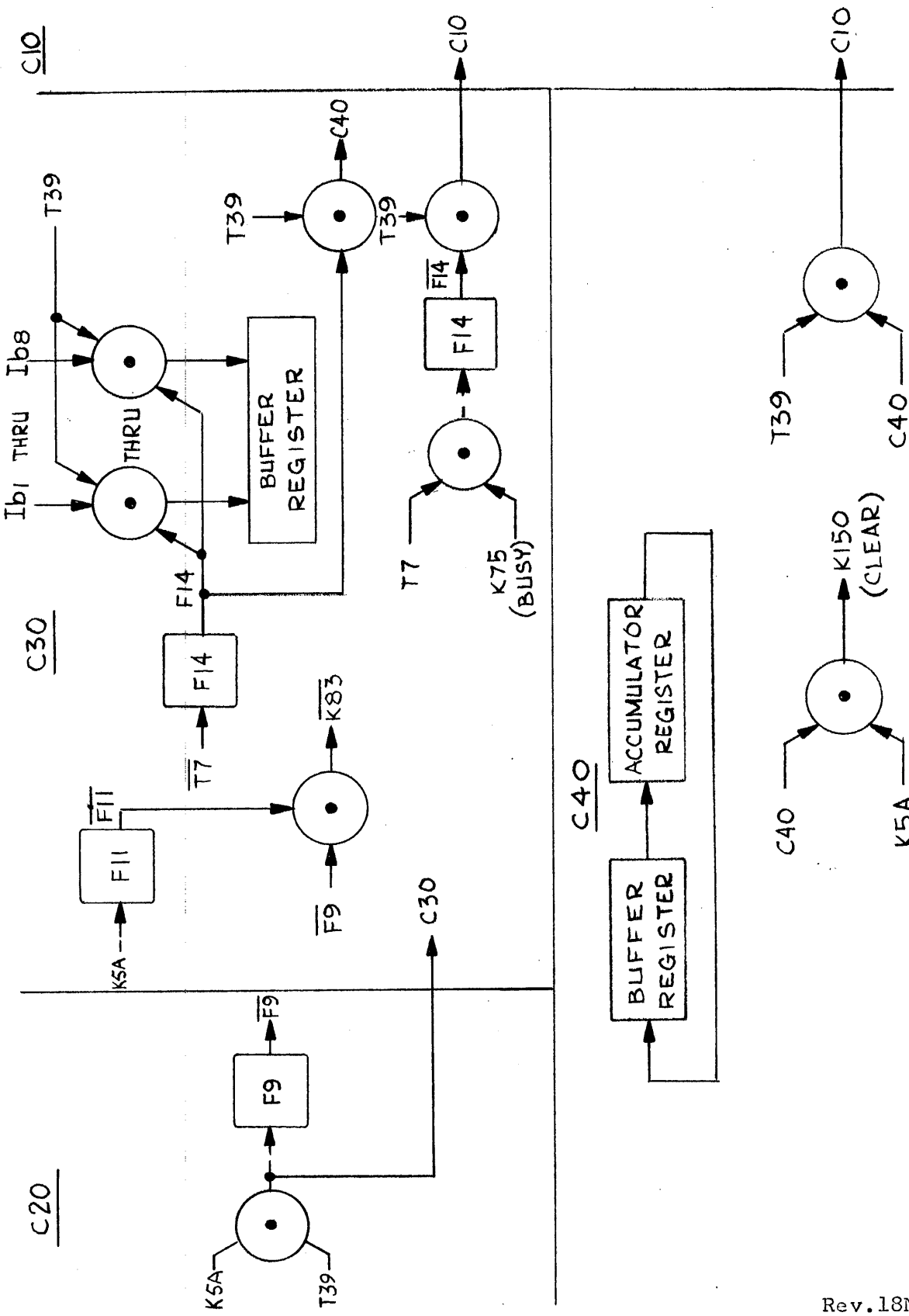


Figure 3.30 Shift Input Command, Flow Chart.

Rev.18NOV68

3.7.28 READ STATUS COMMAND (RS)

Hex Code:	5080	Logic Name:	K5B
Binary Code:	0101 0000 1000 0000	Timing:	4 (3)

Description

This command causes K (F14) to set if an "in process" signal from a selected input device is not present during T7 of C30. The B is then parallel-loaded with 8 bits of status data. The status bits contain special information concerning the operation or condition of an input device. The status bits are serially shifted from the B into the low-order A bits, 0-7. Simultaneously, the high-order 8 A bits are shifted into the B. If an "in process" signal had been present during T7 of C30, this command is aborted and K reset. Figure 3.31 is a flow chart showing the sequence of events that occur for this command. Figure 1.3 shows the orientation of the status bits to the B and A.

Sequence of Events

A) During C20:
   1) Set F9 with A8 at T39 via gate M89-8, figure 3.62.
   2) Set C30 at T39 via gate M14-9, figure 3.54.

B) During C30:
   1) Reset F11 at T31 time via M70-1C-6.
   2) Ask selected input device for status data by generating K83 via gate M116-8, figure 3.78.
   3) Set F14 at $\overline{T7}$ via gate M111-9, figure 3.68.
   4) Reset F14 at T7 if K73, "in process" signal, via gate M107-13, figure 3.66.
   5) Parallel-load B at T39 if F14 via gates M117-3, 6, 8, 11, and M115-3, 6, 8, 11, figures 3.70 and 3.71.
   6) Set C40 at T39 if $\overline{F14}$ via gate M33-6, figure 3.55.
   7) Set C10 at T39 if $\overline{F14}$ via gates M25-6, figure 3.54, and M33-6, figure 3.55.

C) During C40:
   1) Set F11 via gate M89, figure 3.64.
   2) Also see C40 of SI command, steps 1 through 3, paragraph 3.7.27.

Decoded Signals

See Decoded Signals of SI command, paragraph 3.7.27.

Rev.18NOV68

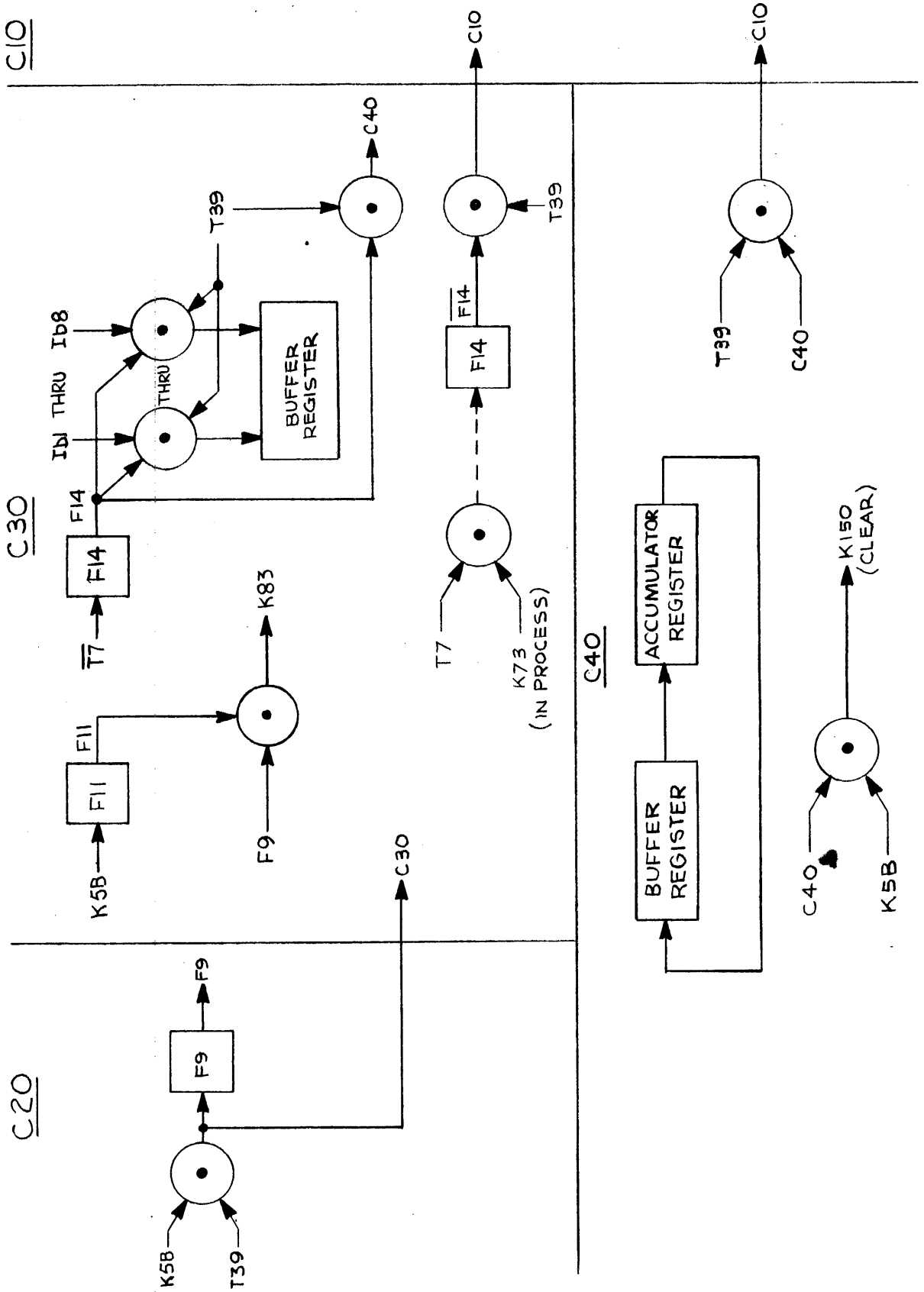


Figure 3.31 Read Status Command, Flow Chart.

3.7.29 CLEAR, INPUT, CHECK ODD PARITY COMMAND (CIO)

Hex Code:	5800	Logic Name:	K5A
Binary Code:	0101 1000 0000 0000	Timing:	4 (3)

Description

This command causes K (F14) to set if a selected input device does not present a Busy signal during T7 of C30. The B is then parallel-loaded with an 8-bit input character. The 7 high-order B bits are serially shifted into the low-order 7 A bits, 0-6. During the shift, 0's are precessed behind the 7 bits filling the remaining 33 A bits and the entire B with 0's. The low-order B bit, F21, is used only as a parity bit in the odd parity check performed during the B to A shift. If a parity error is detected, P (F12) is set. If a Busy signal had been detected during T7 of C30, this command is aborted and K reset. Figure 3.32 is a flow chart showing the sequence of events that occur for this command. Figure 1.2 shows the orientation of the input bits to the B and A.

Sequence of Events

A) During C20:
   1) Reset F10 at $\overline{T4}$ via gate M78-12, figure 3.63.
   2) See C20 of SI command, steps 1 and 2, paragraph 3.7.27.

B) During C30 see C30 of SI command, steps 1 through 7, paragraph 3.7.27.

C) During C40:
   1) Send Clear signal (K150) via gate M116-6, figure 3.79, to selected input device.
   2) Precess high-order 7 bits of B into low-order A via gate M46-9, figure 3.81.
   3) Precess 0's behind high-order 7 bits of B via gate M125-9, figure 3.70.
   4) Center-trip F10 for every F21 with A16 via gates M96-6 and 8, figure 3.63, while shifting contents of B through F21.
   5) Set F12 if $\overline{F10}$ at T39 (parity error) via gate M105-3, figure 3.65.
   6) Set C10 at T39 via gate M25-6, figure 3.54.

Decoded Signals

A2 = C1 A3
A3 = M1 v $\overline{S6}$ v W2
A10 = $\overline{F9}$ $\overline{F10}$
A16 = $\overline{K50}$ v $\overline{F21}$

In addition, see Decoded Signals of SI command, paragraph 3.7.27.

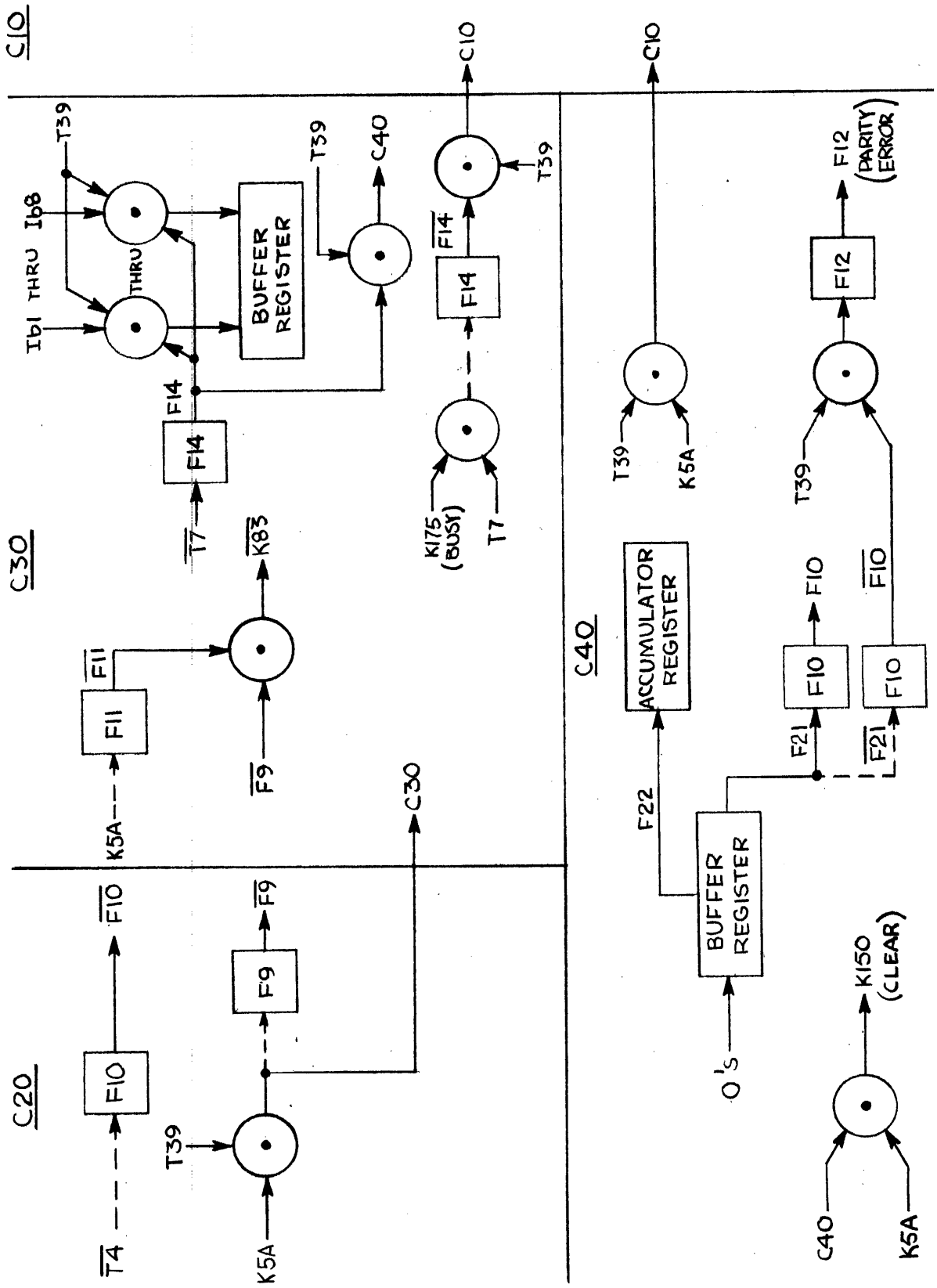


Figure 3.32 Clear, Input, Check Odd Parity Command, Flow Chart.

3.7.30 CLEAR, INPUT, CHECK EVEN PARITY COMMAND (CIE)

Hex Code:	5840	Logic Name:	K5A
Binary Code:	0101 1000 0100 0000	Timing:	4 (3)

Description

This command performs the same operations as the CIO command, paragraph 3.7.29, with one exception. Instead of checking for odd parity, an even parity check is made. Figure 3.33 is a flow chart showing the sequence of events that occur for this command. Figure 1.2 shows the orientation of the input bits to the B and A.

Sequence of Events

A) During C20:
   1) Set F10 during T4 via gate M79-12, figure 3.63.
   2) See C20 of SI command, steps 1 and 2, paragraph 3.7.27.

B) During C30 see C30 of SI command, steps 1 through 7, paragraph 3.7.27.

C) During C40 see C40 of CIO command, steps 1 through 6, paragraph 3.7.29.

Decoded Signals

See Decoded Signals of CIO command, paragraph 3.7.29.

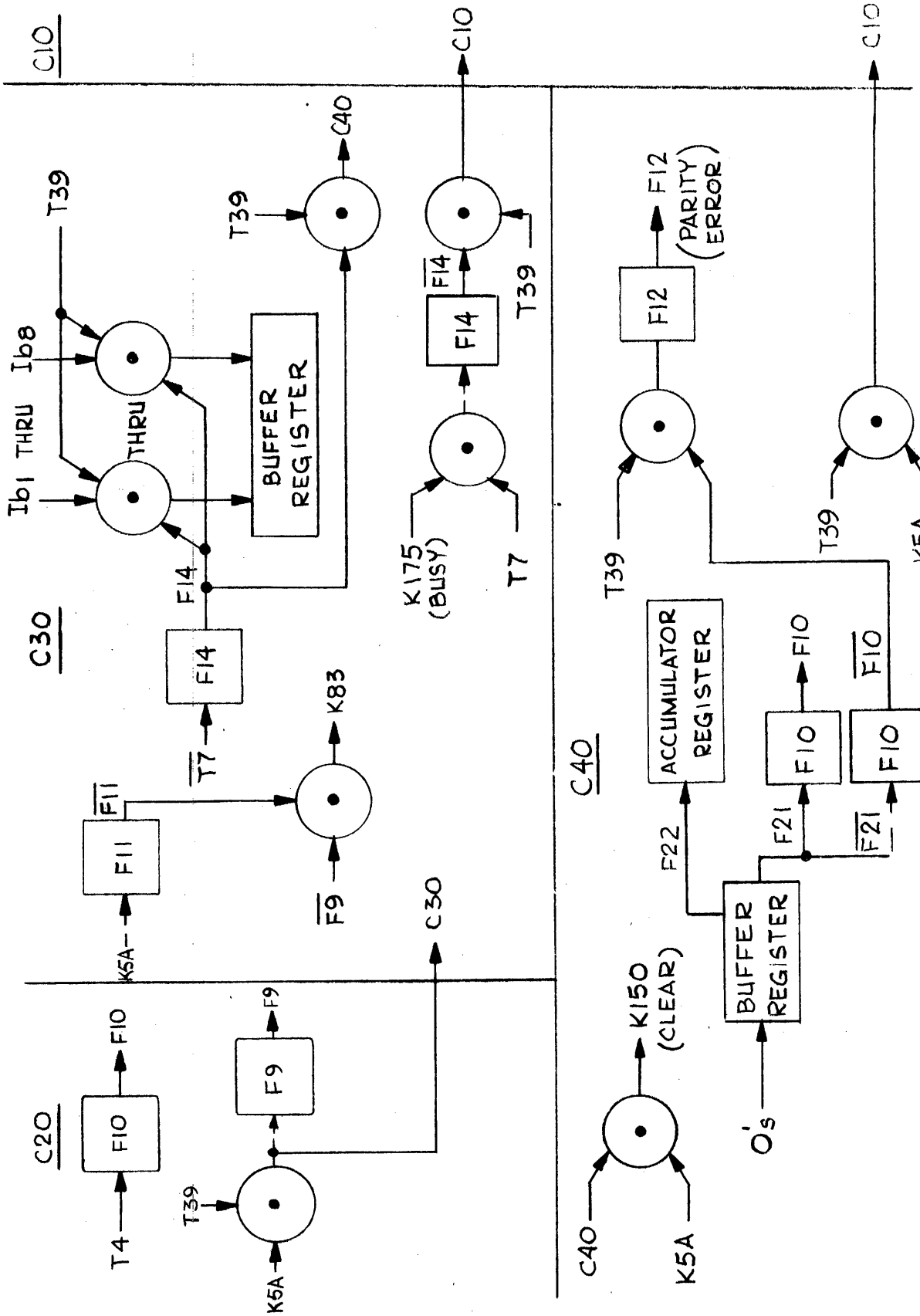


Figure 3.33 Clear, Input, Check Even Parity Command, Flow Chart.

3.7.31 CLEAR, INPUT, CHECK ODD PARITY INTO A COMMAND (CIOP)

Hex Code:	5C00	Logic Name:	K5A
Binary Code:	0101 1100 0000 0000	Timing:	4 (3)

Description

This command performs all the operations of the CIO command, paragraph 3.7.29, plus one additional operation. The state of P (F12) is recorded into the high-order A bit. Figure 3.34 is a flow chart showing the sequence of events that occur for this command. Figure 1.2 shows the orientation of the input bits to the B and A.

Sequence of Events

A) During C20 see C20 of CIO command, steps 1 and 2, paragraph 3.7.29.

B) During C30 see C30 of SI command, steps 1 through 7, paragraph 3.7.27.

C) During C40:
   1) See C40 of CIO command, steps 1 through 6, paragraph 3.7.29.
   2) Record $\overline{F10}$ at T39 into A via gate M27-13, figure 3.83.

Decoded Signals

See Decoded Signals of CIO command, paragraph 3.7.29.

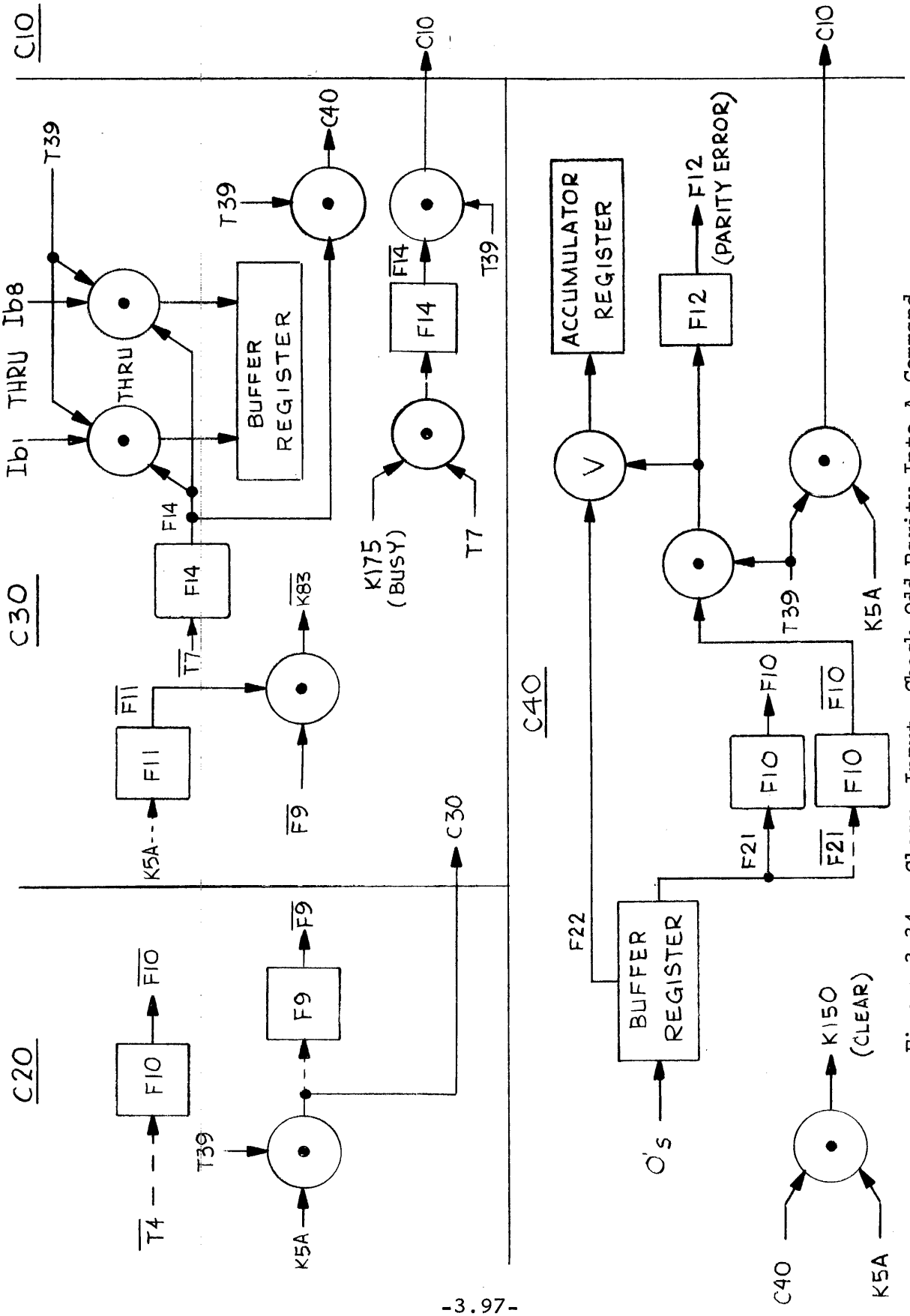


Figure 3.34 Clear, Input, Check Odd Parity Into A Command, Flow Chart.

3.7.32 CLEAR, INPUT, CHECK EVEN PARITY INTO A COMMAND (CIEP)

Hex Code:	5C40	Logic Name:	K5A
Binary Code:	0101 1100 0100 0000	Timing:	4 (3)

Description

This command performs all the operations of the CIE command, paragraph 3.7.30, plus one additional operation. The state of P (F12) is recorded into the high-order A bit. Figure 3.35 is a flow chart showing the sequence of events that occur for this command. Figure 1.2 shows the orientation of the input bits to the B and A.

Sequence of Events

A) During C20 see C20 of CIE command, steps 1 and 2, paragraph 3.7.30.

B) During C30 see C30 of SI command, steps 1 through 7, paragraph 3.7.27.

C) During C40:
   1) See C40 of C10 command, steps 1 through 6, paragraph 3.7.29.
   2) Record $\overline{F10}$ at T39 into A via gate M27-13, figure 3.83.

Decoded Signals

See Decoded Signals of CIO command, paragraph 3.7.29.

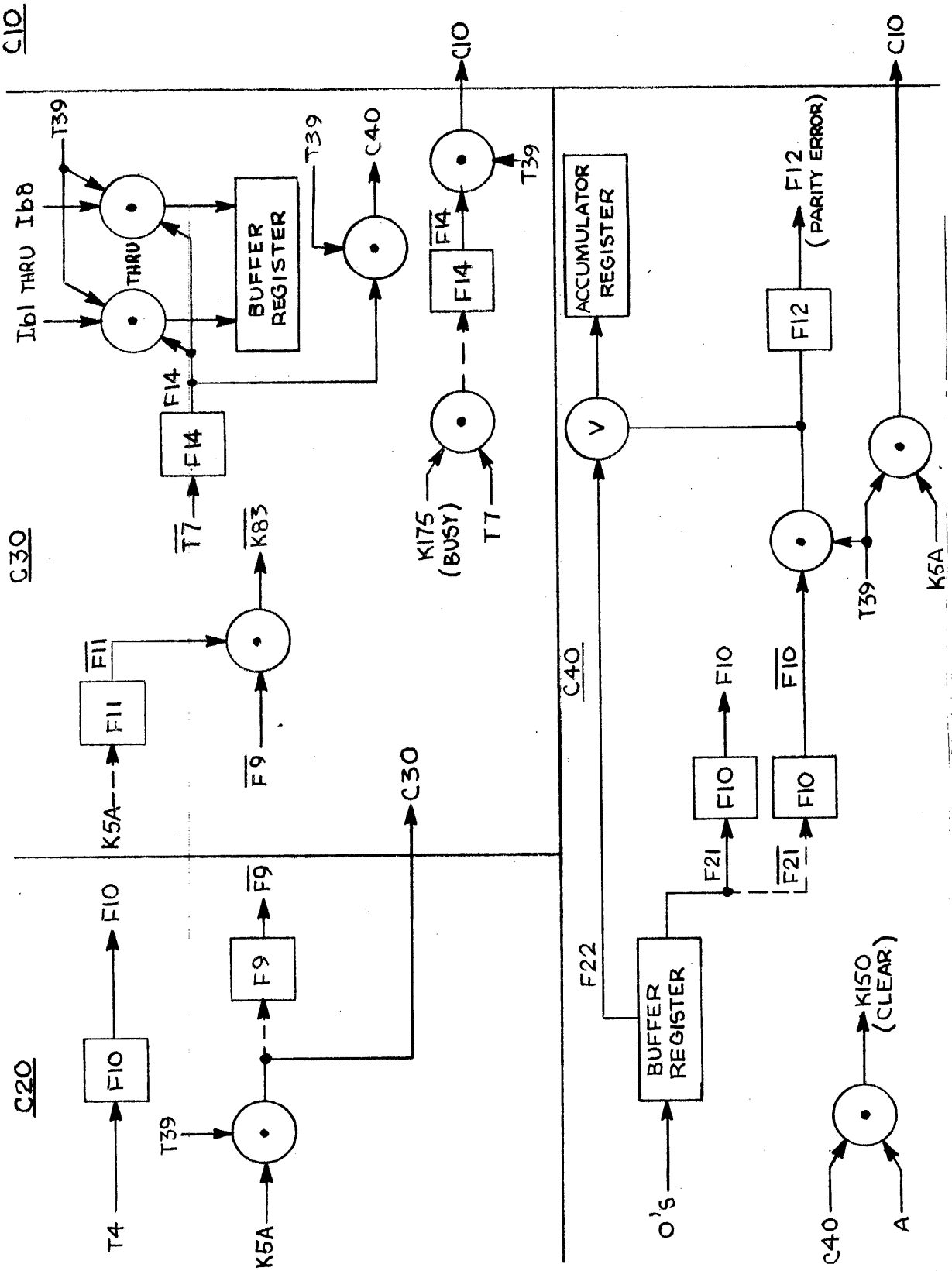


Figure 3.35 Clear, Input, Check Even Parity Into A Command, Flow Chart.

3.7.33 DECIMAL LEFT SINGLE SHIFT COMMAND (DLS)

Hex Code:	6000+N	Logic Name:	K4B1
Binary Code:	0110 0000 0NNN NNNN	Timing:	3+n

Description

This command causes the contents of the A to be multiplied by 10, the number of times specified by the shift count. N equals the shift count minus one. The state of K (F14) is destroyed. The shift is performed by delaying the A 2 bit-times, equivalent to multiplying A by 4, and simultaneously adding the results of this operation to A (A x 5). The A is then delayed one bit-time (A x 10). The results are now equal to 10 times the original of the A: 2 (4A + A) = 10A. Figure 3.36 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30:
   1) Reset F10 via gate M78-9, figure 3.63.
   2) Reset F11 via gate M70, figure 3.65.
   3) Reset F14 via gate M103-9, figure 3.67.
   4) Set C40 at T39 via gate M24, figure 3.55.
   5) Reset F9 via $\overline{\text{F101}}$ at T39, M68-13.

B) During C40:
   1) Establish L50 = L10 via gate M111-5, figure 3.89.
   2) Delay L50 2 bit-times by gating it through F10 and then through F11 via gates M88-13 and M87-1, figure 3.63; M69-13, figure 3.64; and M104, figure 3.65.
   3) Establish L51 = F11 via gate M76-8, figure 3.90.
   4) Add L51 (equal to zero for the first 2 bit-times of the first cycle through C40, thereafter equal to L50 delayed 2 bit-times) to L50 in the adder/subtractor, figure 3.90. (Note, F14 is set by L50 L51 via gate M108-8, figure 3.68, and is reset by $\overline{\text{L50 L51}}$ via gate M103-4, figure 3.67.)
   5) Delay L53 one bit-time by gating it through F9 via gates M89-6 and M80-11, figure 3.62.
   6) Record F9 (initially = 0) into A via gate M35-10, figure 3.81.
   7) See C40 of BLS-BLSK commands, steps 4 through 7, 9, and 10, paragraph 3.7.19.

Decoded Signals

A6 = T39 F2
A7 = F1 L30 v $\overline{\text{F1}}$ L10
A11 = F5 $\overline{\text{F7}}$ M6
A18 = F7 $\overline{\text{F8}}$
A35 = K41 v $\overline{\text{K13}}$ v $\overline{\text{A36}}$
A39 = $\overline{\text{F1}}$ F2
K34 = K35 C40 $\overline{\text{A39}}$
K35 = A18 $\overline{\text{F5}}$ M6
K41 = K42 $\overline{\text{F6}}$
K42 = K34 $\overline{\text{F4}}$

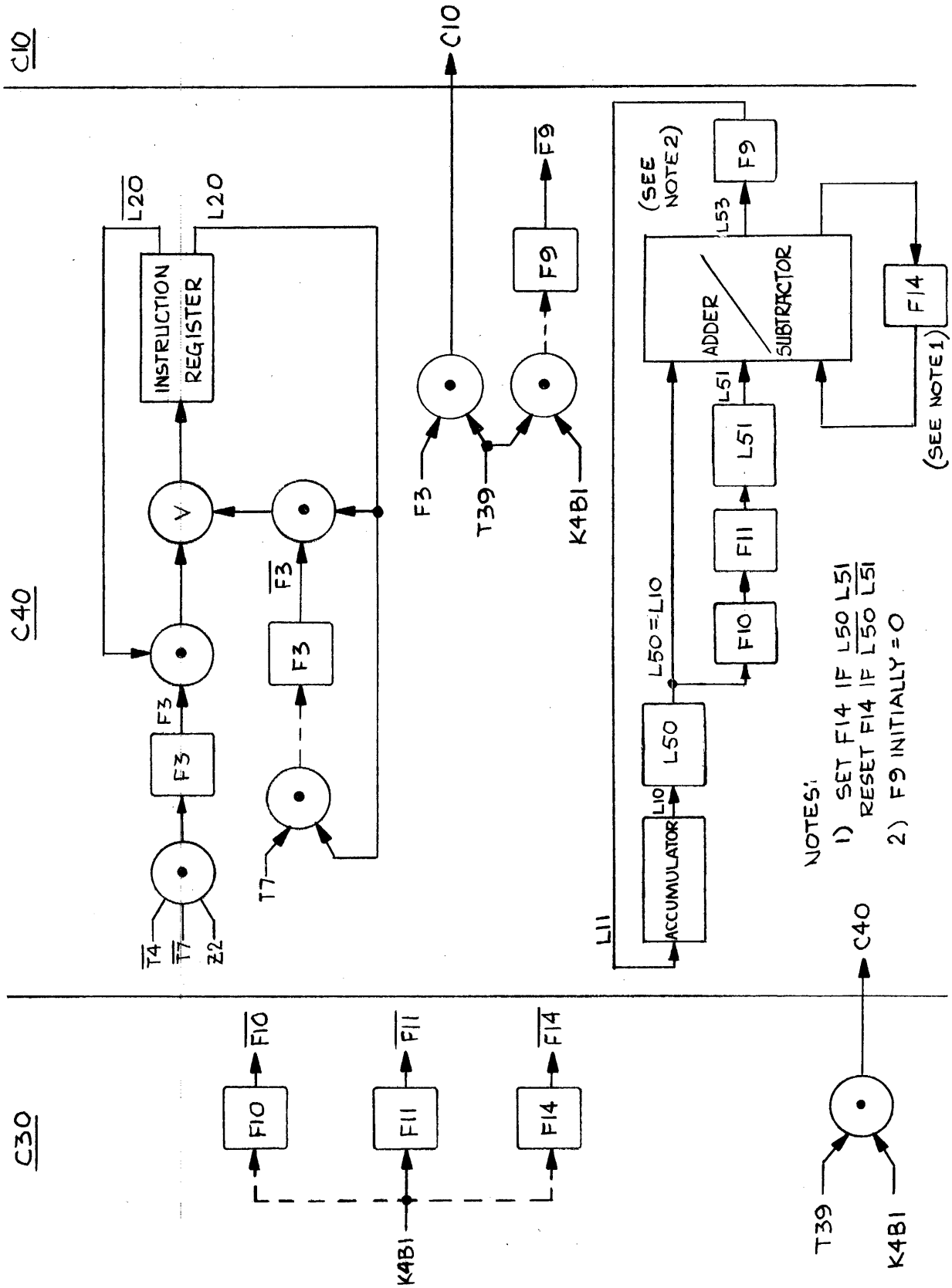


Figure 3.36 Decimal Left Single Shift Command, Flow Chart.

3.7.34 DECIMAL LEFT SINGLE SHIFT, PLUS CONSTANT COMMAND (DLSC)

Hex Code:	6080+N	Logic Name:	K4B1
Binary Code:	0110 0000 1NNN NNNN	Timing:	3+n

Description

This command performs the same operations of the DLS command, paragraph 3.7.33, with one additional operation. At the beginning of the first shift, the low-order A bit is set to 1. Figure 3.37 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C20, set F9 via A8, M89-3C-9.

B) During C30, see C30 of DLS command, steps 1 through 4, paragraph 3.7.33.

C) During C40:
   1) See C40 of DLS command, steps 1 through 5, paragraph 3.7.33.
   2) Record F9 (initially = 1) into A via gate M35-10, figure 3.81.
   3) See C40 of BLS-BLSK commands, steps 4 through 7, 9, and 10, paragraph 3.7.19.

Decoded Signals

See Decoded Signals of DLS command, paragraph 3.7.33.

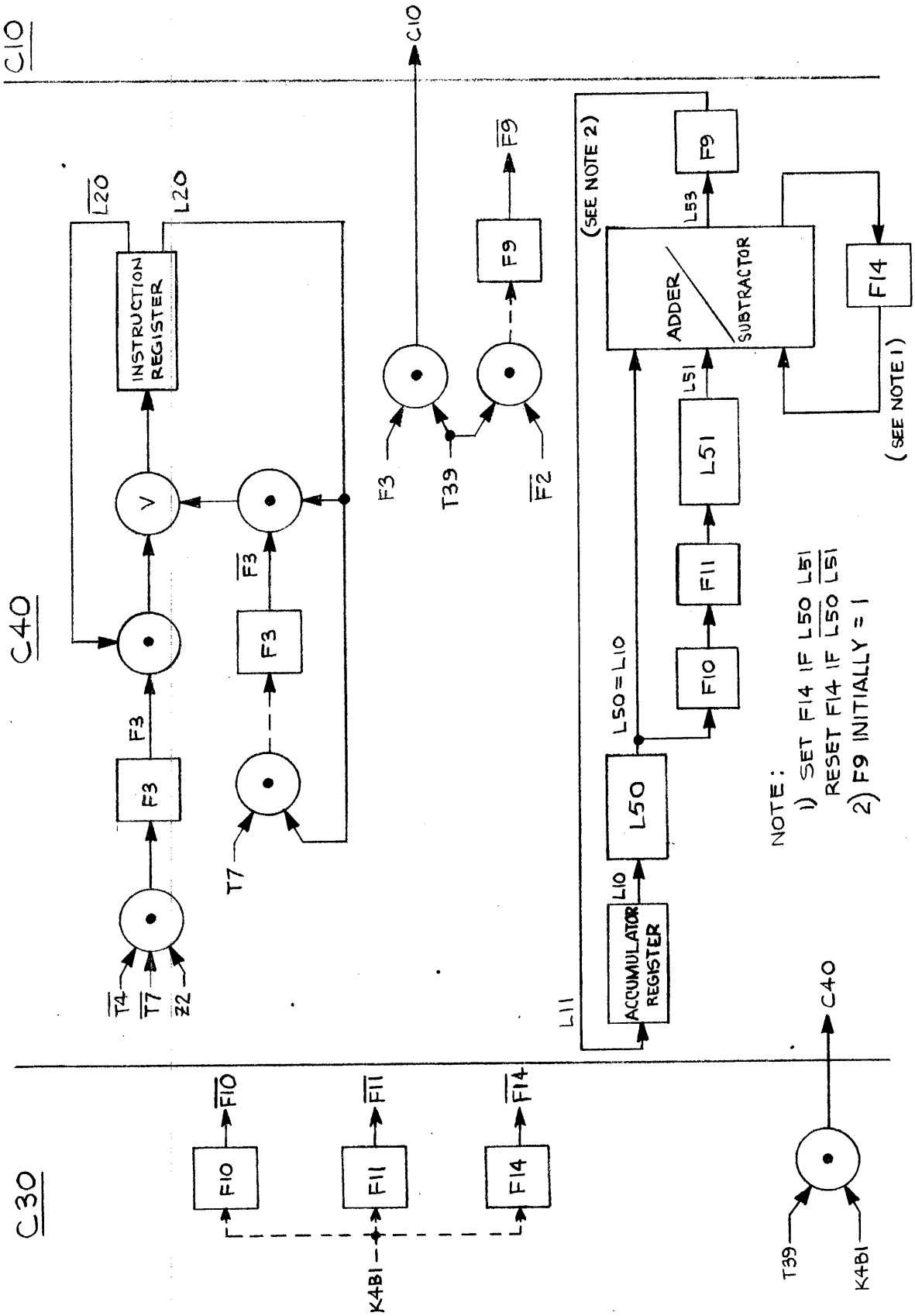


Figure 3.37 Decimal Left Single Shift, Plus Constant Command, Flow Chart.

3.7.35 DECIMAL LEFT SINGLE SHIFT ON SCRATCHPAD COMMAND (DLSS)

Hex Code:	6100	Logic Name:	K4B4
Binary Code:	0110 0001 0000 0000	Timing:	4

Description

This command performs the same operations on whichever S happens to be available for use, that the DLS command, paragraph 3.7.33, performs on the A. The DLSS command, however, allows only one shift to be performed since N is fixed at zero. Figure 3.38 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30 see C30 of DLS command, steps 1 through 4, paragraph 3.7.33.

B) During C40:
   1) Establish L50 = L30 via gate M111-5, figure 3.89.
   2) See C40 of DLS command, steps 2 through 5, paragraph 3.7.33.
   3) Record F9 (initially = 0) into S via gate M50-13, figure 3.87.
   4) Set F3 at $\overline{T4}$ $\overline{T7}$ Z2 via gate M81-8, figure 3.59.
   5) Set C10 at T39 via gate M25-6, figure 3.54.

Decoded Signals

See Decoded Signals of DLS command, paragraph 3.7.33.

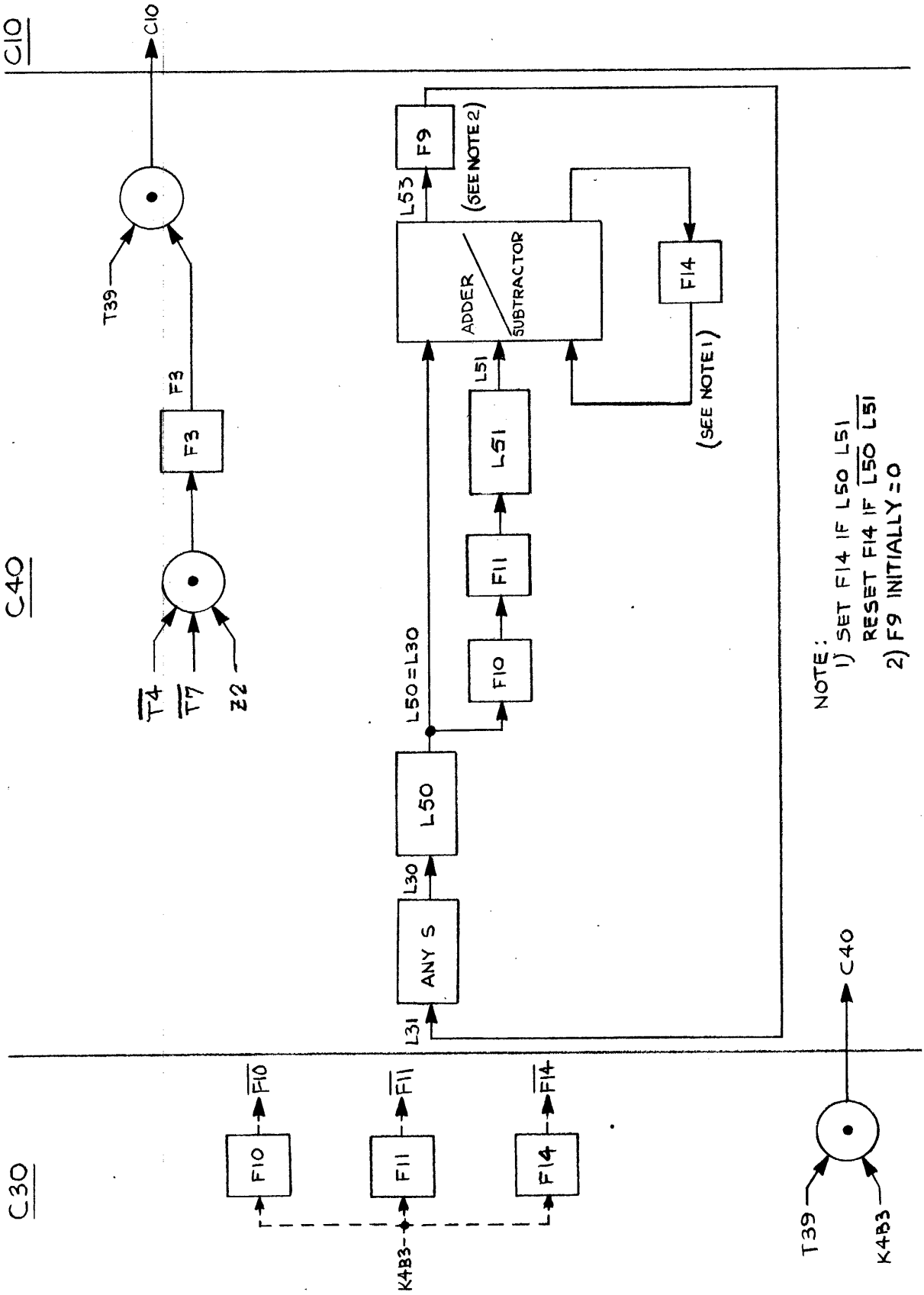


Figure 3.38 Decimal Left Single Shift on Scratchpad Command, Flow Chart.

3.7.36 DECIMAL LEFT SINGLE SHIFT ON SCRATCHPAD, PLUS CONSTANT COMMAND (DLSSC)

Hex Code:	6180	Logic Name:	K4B4
Binary Code:	0110 0001 1000 0000	Timing:	4

Description

This command performs the same operations on whichever S happens to be available for use, that the DLSC command, paragraph 3.7.34, performs on the A. The DLSSC command, however, allows only one shift to be performed since N is fixed at zero. Figure 3.39 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30 see C30 of DLS command, steps 1 through 4, paragraph 3.7.33.

B) During C40:
   1) Establish L50 = L30 via gate M111-5, figure 3.89.
   2) See C40 of DLS command, steps 2 through 5, paragraph 3.7.33.
   3) Record F9 (initially = 1) into S via gate M50-13, figure 3.87.
   4) Set F3 at $\overline{T4}$ $\overline{T7}$ Z2 via gate M81, figure 3.59.
   5) Set C10 at T39 via gate M25-6, figure 3.54.

Decoded Signals

See Decoded Signals of DLS command, paragraph 3.7.33.

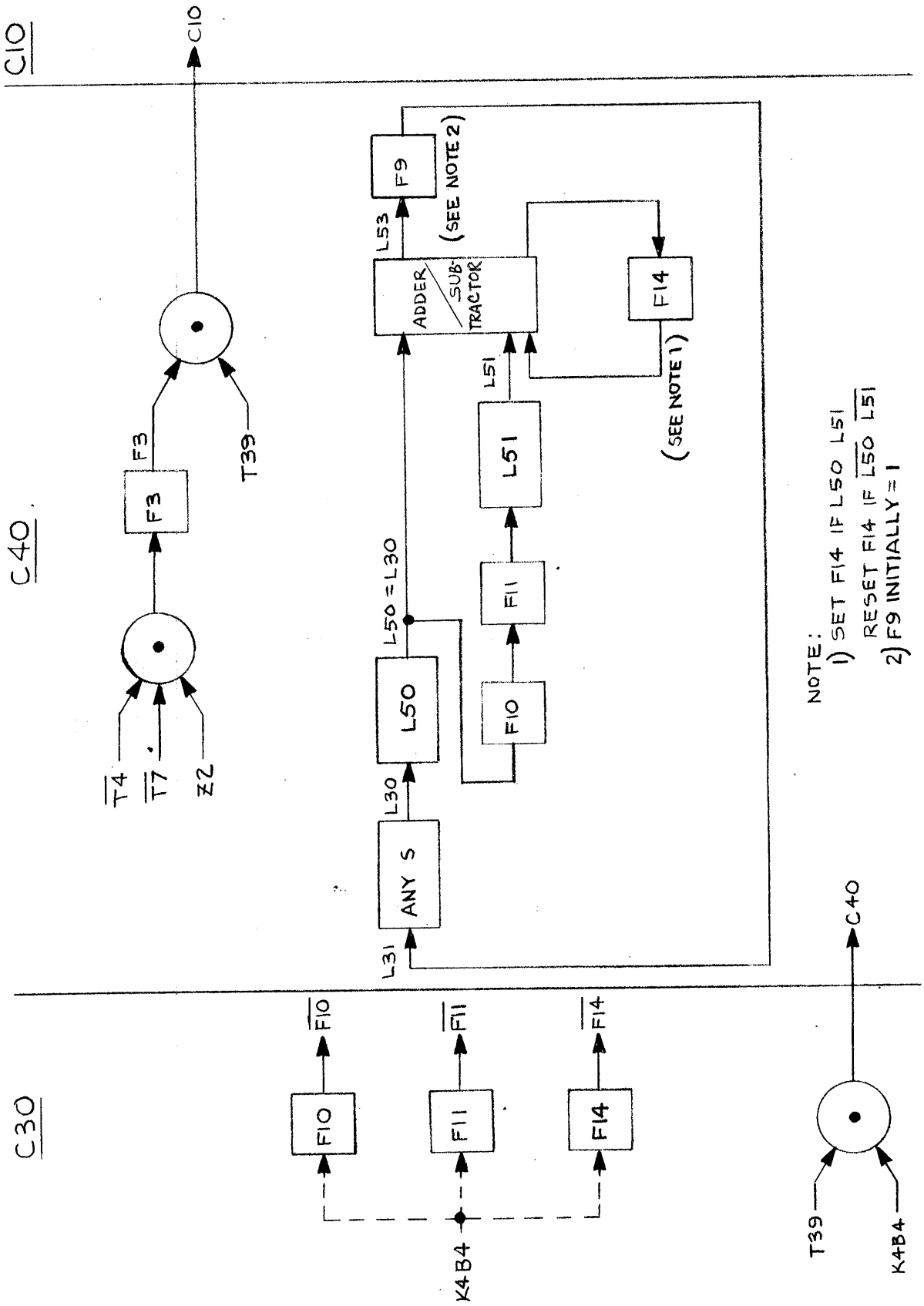


Figure 3.39 Decimal Left Single Shift on Scratchpad, Plus Constant Command, Flow Chart.

3.7.37 DECIMAL LEFT DOUBLE SHIFT COMMAND (DLD)

Hex Code:	6200+N	Logic Name:	K4B2
Binary Code:	0110 0010 0NNN NNNN	Timing:	8n-3+za

Description

This command performs the same operations on scratchpad sectors 0 and 1, combined as a single 80-bit block of information, that the DLS command, paragraph 3.7.33, performs on the A. Figure 3.40 is a flow chart showing the sequence of events that occurs for this command.

Sequence of Events

A) During C30:
   1) See C30 of DLS command, steps 1 through 4, paragraph 3.7.33.
   2) Set F1 if Z3 at T39 via gate M65, figure 3.58.

B) During C40:
   1) Set F1 if Z3 at T39 via gate M65, figure 3.58.
   2) Establish L50 = L30 via gate M111-5, figure 3.89.
   3) See C40 of DLS command, steps 2 through 5, paragraph 3.7.33.
   4) Record F9 (initially = 0) into S if F1 via gate M50-13, figure 3.87.
   5) See C40 of BLD-BLDK commands, steps 5 through 9 and 11 through 14, paragraph 3.7.21.

Decoded Signals

See Decoded Signals of DLS command, paragraph 3.7.33.

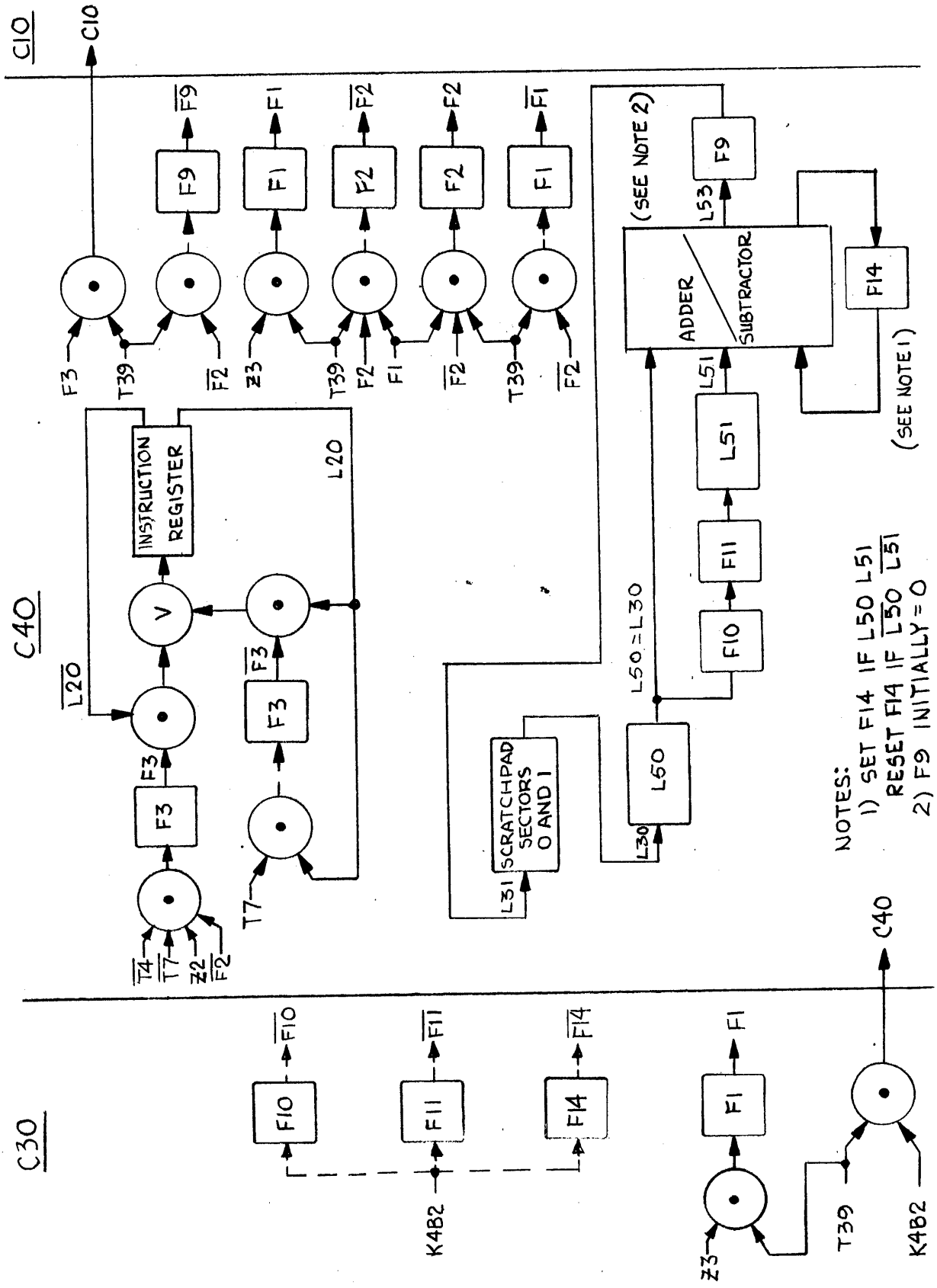


Figure 3.40 Decimal Left Double Shift Command, Flow Chart.

3.7.38 DECIMAL LEFT DOUBLE SHIFT, PLUS CONSTANT COMMAND (DLDC)

Hex Code:	6280+N	Logic Name:	K4B2
Binary Code:	0110 0010 1NNN NNNN	Timing:	8n-3+za

Description

This command performs the same operations on scratchpad sectors 0 and 1, combined as a single 80-bit block of information, that the DLSC command, paragraph 3.7.34, performs on the A. Figure 3.41 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30:
   1) See C30 of DLS command, steps 1 through 4, paragraph 3.7.33.
   2) Set F1 if Z3 at T39 via gate M65, figure 3.58.

B) During C40:
   1) Set F1 if Z3 at T39 via gate M65, figure 3.58.
   2) Establish L50 = L30 via gate M111-5, figure 3.89.
   3) See C40 of DLS command, steps 2 through 5, paragraph 3.7.33.
   4) Record F9 (initially = 1) into S if F1 via gate M50-13, figure 3.87.
   5) See C40 of BLD-BLDK commands, steps 5 through 9 and 11 through 14, paragraph 3.7.21.

Decoded Signals

See Decoded Signals of DLS command, paragraph 3.7.33.

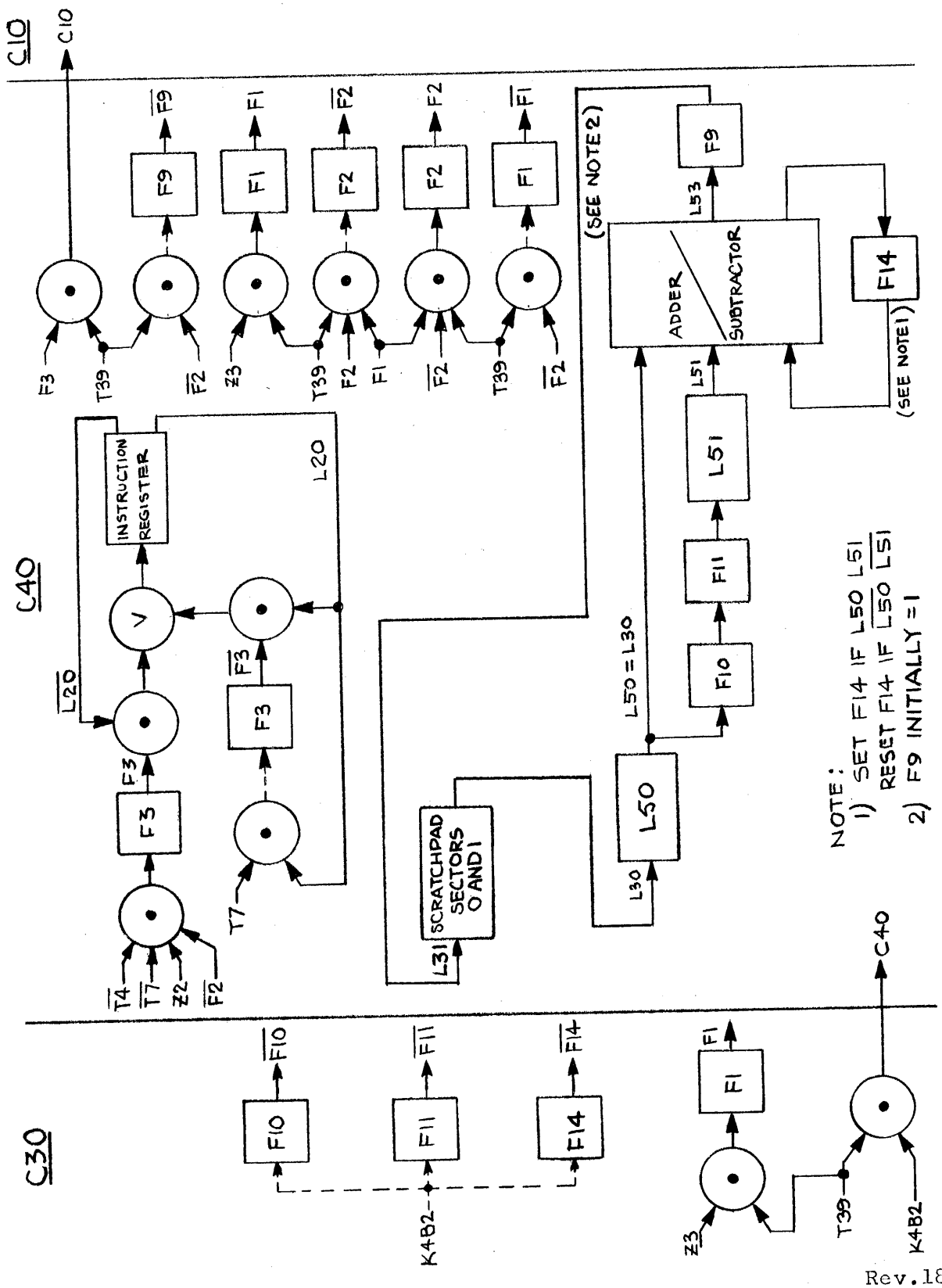


Figure 3.41 Decimal Left Double Shift, Plus Constant Command, Flow Chart.

Rev.18NOV68

3.7.39 DECIMAL LEFT DOUBLE SHIFT ON SCRATCHPAD COMMAND (DLDS)

Hex Code:	6300	Logic Name:	K4B3
Binary Code:	0110 0011 0000 0000	Timing:	5

Description

This command performs the same operations on whichever 2 scratchpad sectors that happen to be available for use, as a single 80-bit block of information, that the DLS command performs on the A. Figure 3.42 is a flow chart showing the sequence of events that occurs for this command.

Sequence of Events

A) During C30 see C30 of DLS command, steps 1 through 4, paragraph 3.7.33.

B) During C40:
   1) Establish L50 = L30 via gate M111-5, figure 3.89.
   2) See C40 of DLS command, steps 2 through 5, paragraph 3.7.33.
   3) Record F9 (initially = 0) into S via gate M50-13, figure 3.87.
   4) See C40 of BLD-BLDK commands, steps 5, 6, and 14, paragraph 3.7.21.

Decoded Signals

See Decoded Signals of DLS command, paragraph 3.7.33.

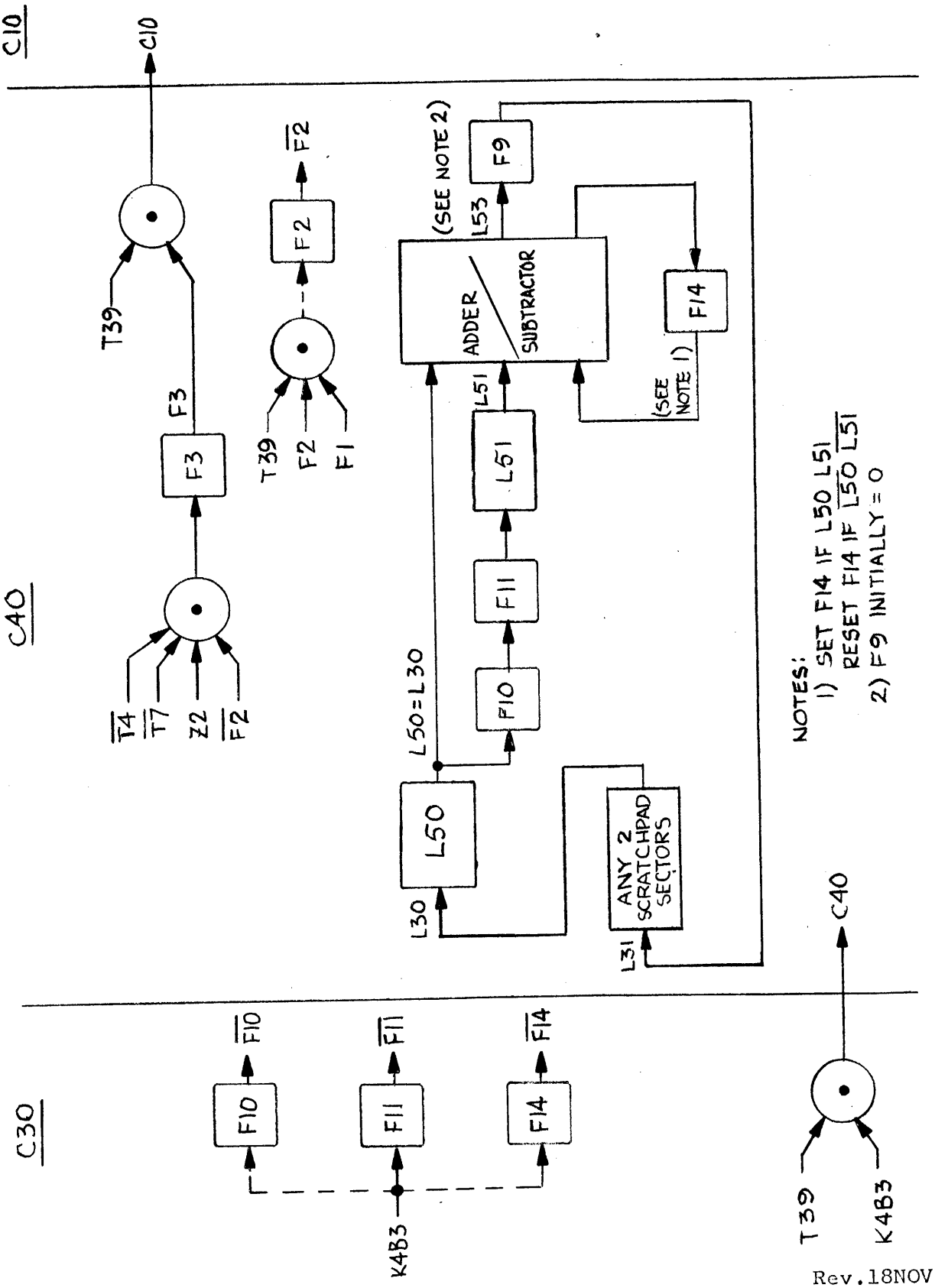


Figure 3.42 Decimal Left Double Shift on Scratchpad Command, Flow Chart.

Rev.18NOV68

3.7.40 DECIMAL LEFT DOUBLE SHIFT ON SCRATCHPAD PLUS CONSTANT COMMAND (DLDSC)

Hex Code:	6380	Logic Name:	K4B3
Binary Code:	0110 0011 1000 0000	Timing:	5

Description

This command performs the same operations on whichever 2 scratchpad sectors that happen to be available for use, as a single 80-bit block of information, that the DLSC command, paragraph 3.7.34, performs on the A. Figure 3.43 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30 see C30 of DLS command, steps 1 through 4, paragraph 3.7.33.

B) During C40:
   1) Establish L50 = L30 via gate M111-5, figure 3.89.
   2) See C40 of DLS command, steps 2 through 5, paragraph 3.7.33.
   3) Record F9 (initially = 1) into S via gate M50-13, figure 3.87.
   4) See C40 of BLD-BLDK commands, steps 5, 6, and 14, paragraph 3.7.21.

Decoded Signals

See Decoded Signals of DLS command, paragraph 3.7.33.

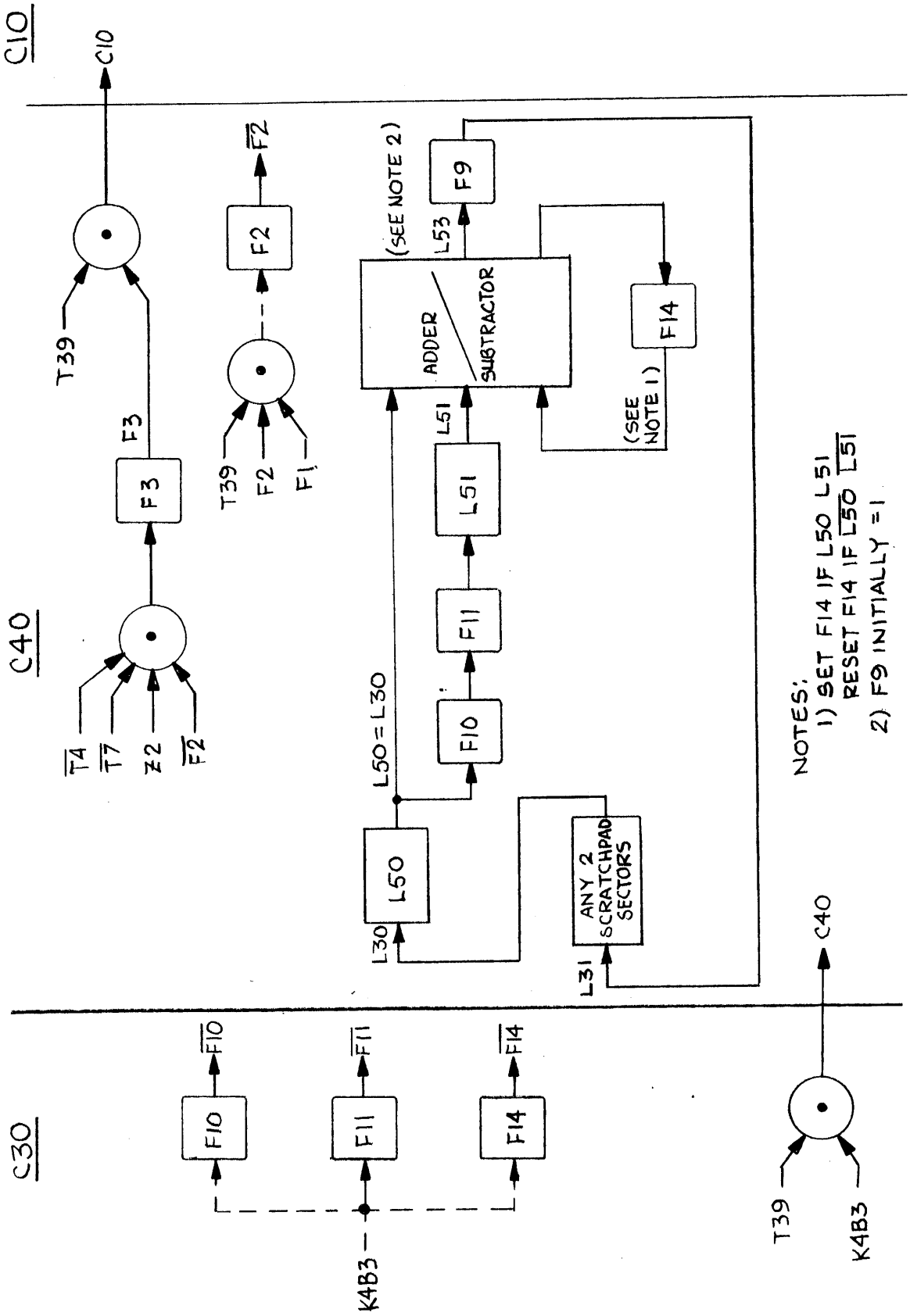


Figure 3.43 Decimal Left Double Shift on Scratchpad, Plus Constant Command, Flow Chart.

3.7.41 DECIMAL RIGHT SINGLE SHIFT COMMAND (DRS)

Hex Code:	6800+N	Logic Name:	K4A1
Binary Code:	0110 1000 0NNN NNNN	Timing:	2+2n

Description

This command causes the contents of the A to be divided by 10, the number of times specified by the shift count. N equals the shift count minus one. This operation is performed by a 2 word-time algorithm that divides by 5. Simultaneously, during the first word-time of the algorithm the contents of the A are shifted right one bit (equivalent to dividing by 2) resulting in a total division of 10.

The algorithm uses a basic subtraction process where the minuend is the number to be divided by 5, the remainder is the result, and the subtrahend is developed from the remainder. Let us examine a simple example. The number to be divided by 5 is 10 and we have an 8-bit word. The number is shown in binary with the 2 low-order bits of the subtrahend equal to zero:

```
00001010                after subtracting:   00001010
-     00                                     -     00
-------                                      --------
                                                  10
```

The 2 low-order bits of the remainder are now used as the next 2 bits of the subtrahend, and after subtracting.

```
00001010
-   1000
--------
    0010
```

Continuing this process to the end of the word we have:

```
 00001010          number (-10) N
-00001000                      - S
---------          ------------
 00000010          result (-2)  R
```

Another way of looking at this is with some simple algebra. The subtrahend (S) is subtracted from the number (N) to give the result (R), N - S = R. But the subtrahend is observed to be nothing more than the result shifted 2 places to the left which is the equivalent of multiplying by 4. Therefore:

$$S = 4R$$
$$N - 4R = R$$
$$N = R + 4R$$
$$N = 5R$$
$$R = \frac{N}{5}$$

Here again the result is equal to 1/5 of the original number. However, there is one limitation to this process. This subtraction process gives the correct result only when the number is exactly divisible by 5 which can be readily verified by the reader. To overcome this difficulty, the process is repeated for 2 consecutive word-times with any borrow carried across the word-time. The following is a 6-bit word example where the number is equal to 19.

```
0 1 0 0 1 1     0 1 0 0 1 1
0 0 1 1 1 1     0 1 1 1 0 0
-----------     -----------
0 0 0 0 1 1     1 1 0 1 1 1
```

second word time | first word time

The correct result (3) appears as the remainder of the second word-time. The algorithm as it now stands will correctly divide any number by 5.

It turns out that since the computer has a 40-bit word which is an even number of pairs of bits (20) the minuend during the first word time must be the 1's complement of the number. Therefore, a better example is one with an 8-bit word:

```
0 0 0 1 0 0 1 1     1 1 1 0 1 1 0 0
0 0 0 0 1 1 1 1     1 1 1 1 0 0 0 0
---------------     ---------------
0 0 0 0 0 0 1 1     1 1 1 1 1 1 0 0
```

The above example shows the divide by 5 algorithm as it is implemented in the computer. In order to divide by 10, the above algorithm must be combined with a divide by 2, or right shift, as previously mentioned. This is done during the first word-time of the algorithm. Figure 3.44 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30:
   1) Reset F10 via gate M78-9, figure 3.63.
   2) Reset F11 via gate M70, figure 3.65.
   3) Reset F14 via gate M103-9, figure 3.67.
   4) Set C40 at T39 via gate M24, figure 3.55.

Rev.18NOV68

B) During C40:

1) Establish $\overline{L50}$ = L19 if $\overline{F9}$ $\overline{T39}$ via gate M111-2, figure 3.89. (Note, F9 is initially reset during C20 via gate M68-13, figure 3.62.)
2) Record $\overline{L50}$ $\overline{T39}$ if $\overline{F9}$ into A via gate M35-10, figure 3.81.
3) Delay L53 2 bit-times by gating it through F10 and F11 via gates M87-9 and M88-9, figure 3.63; M69-13, figure 3.64; and M104, figure 3.65.
4) Establish L51 = F11 via gate M76-8, figure 3.90.
5) Subtract L51 (equal to zero for the first 2 bit-times of the first cycle through C40, thereafter equal to L53 delayed 2 bit-times) from L50 (1's complement of A one bit-time early if $\overline{F9}$) via adder/subtractor, figure 3.90. (Note, F14 is set if $\overline{L50}$ L51 via gate M108-8, figure 3.68, and F14 is reset if L50 $\overline{L51}$ via gate M103-4, figure 3.67.)
6) Reverse state of F9 at T39 via gates M80-6 and M89-8, figure 3.62. (Since A15 is low both the set and reset inputs of F9 are high. F9 being a JK type flipflop reverses its state. Thus, during the first cycle through C40, F9 is reset; during the second F9 is set; during the third reset; etc.
7) Establish L50 = L10 if F9 via gate M111-5, figure 3.89.
8) Record L53 if F9 into A via gate M35-10, figure 3.81.
9) Set F3 at $\overline{T4}$ $\overline{T7}$ Z2 via gate M81, figure 3.59.
10) Record $\overline{L20}$ with F3 via gate M1-2, figure 3.85, into I.
11) Record F3 if L20 during T7 via gate M73-6, figure 3.59.
12) Record L20 with $\overline{F3}$ via gate M1-4, figure 3.85, into I.
13) Set C10 at T39 if F3 via gate M25-6, figure 3.54.

Decoded Signals

A6 = T39 $\overline{F2}$
A7 = F1 L30 v $\overline{F1}$ L10
A11 = F5 F7 M6
A15 = $\overline{K40}$ v $\overline{A6}$
A18 = $\overline{F8}$ F7
A35 = K41 v $\overline{K13}$ v $\overline{A36}$
A39 = $\overline{F1}$ F2
K34 = K35 C40 $\overline{A39}$
K35 = A18 $\overline{F5}$ M6
K40 = K34 F6 F4
K41 = K42 $\overline{F6}$
K42 = K34 $\overline{F4}$
K43 = F4 K34 ($\overline{F6}$ $\overline{F9}$)

Rev.18NOV68

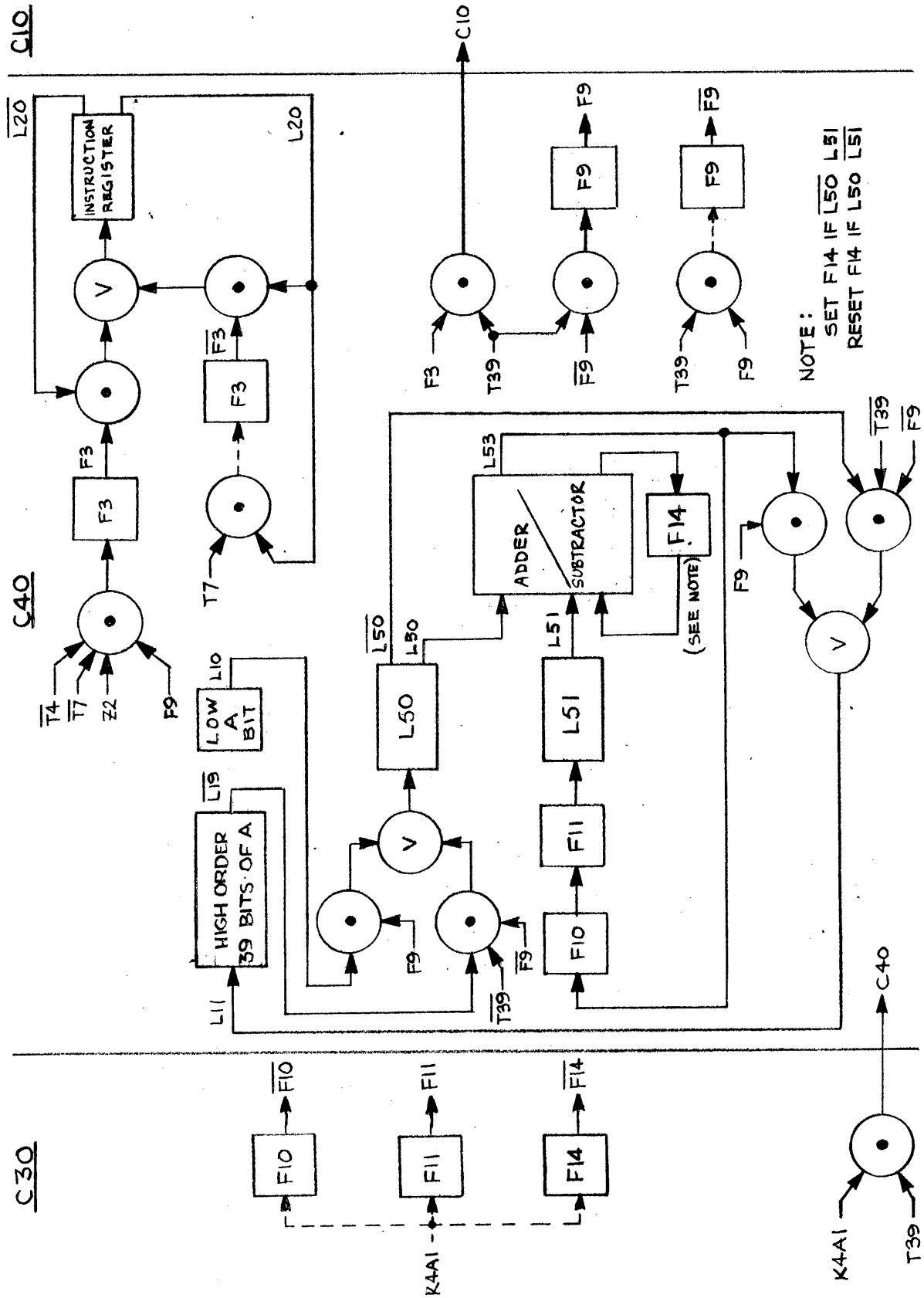


Figure 3.44 Decimal Right Single Shift Command, Flow Chart.

3.7.42 DECIMAL RIGHT DOUBLE SHIFT COMMAND (DRD)

Hex Code:	6A00+N	Logic Name:	K4A2
Binary Code:	0110 1010 0NNN NNNN	Timing:	16n-3+za

Description

This command performs the same operations on scratchpad sectors 0 and 1 that the DRS command, paragraph 3.7.41, performs on the A. Figure 3.45 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30:
   1) See C30 of DRS command, steps 1 through 4, paragraph 3.7.41.
   2) Set F1 if Z3 at T39 via gate M65, figure 3.58.

B) During C40:
   1) Set F1 if Z3 at T39 via gate M65, figure 3.58.
   2) Establish $\overline{L50}$ = L39 if $\overline{F9}$ $\overline{T39}$ via gate M82-5, figure 3.89. (Note, F9 is initially reset during C20 via gate M68-13, figure 3.62.)
   3) Record $\overline{L50}$ $\overline{T39}$ if F1 $\overline{F9}$ into S via gate M50-13, figure 3.87.
   4) Delay L53 2 bit-times by gating it through F10 and F11 via gates M87-9 and M88-9, figure 3.63; M69-13, figure 3.64; and M104, figure 3.65.
   5) Establish L51 = F11 via gate M76-8, figure 3.90.
   6) Subtract L51 (equal to zero for the first 2 bit-times of the first cycle through C40, thereafter equal to L53 delayed 2 bit-times) from L50 (1's-complement of S one bit-time early if $\overline{F9}$) via adder/subtractor, figure 3.90. (Note, F14 is set if $\overline{L50}$ L51 via gate M108-8, figure 3.68, and F14 is reset if L50 $\overline{L51}$ via gate M103-4, figure 3.67.)
   7) Reverse state of F2 at T39 if F1 via gates M72 and M75-8, figure 3.58. (Note, since F2 is a JK type flipflop when both set and reset inputs are high the flipflop reverses state. During the first cycle through C40 with F1, F2 is set; during the second, reset; during the third, set; etc.
   8) Reverse state of F9 at T39 if $\overline{F2}$ via gates M80-6 and M89-8, figure 3.62.

9) Reset F1 if $\overline{F2}$ at T39 via gate M64-9, figure 3.58.
10) Set F1 if Z3 at T39 via gate M65, figure 3.58.
11) Establish L50 = L30 if F9 via gate M111-5, figure 3.89.
12) Record L53 if F1 F9 into S via gate M50-13, figure 3.87.
13) Set F3 if $\overline{F2}$ F9 at $\overline{T4}$ $\overline{T7}$ Z2 via gate M81, figure 3.59.
14) See C40 of DRS command, steps 10 through 13, paragraph 3.7.41.

Decoded Signals

$K37 = \overline{K35} \vee \overline{C49} \vee \overline{F1}$

See Decoded Signals of DRS command, paragraph 3.7.41.

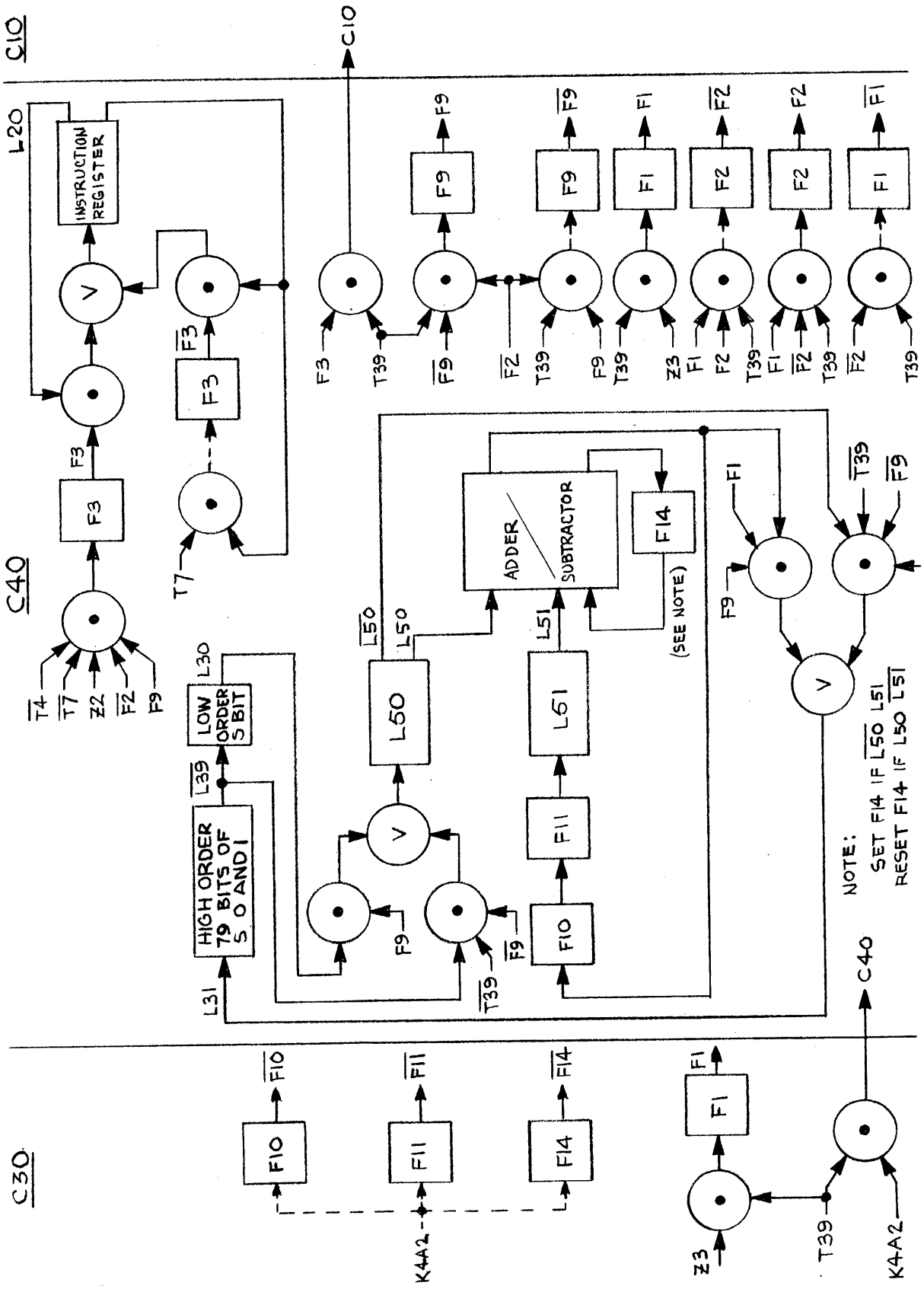


Figure 3.45 Decimal Right Double Shift Command, Flow Chart

3.7.43 OUTPUT ACCUMULATOR WITH ODD PARITY COMMAND (OAO)

Hex Code:	7000	Logic Name:	K6C
Binary Code:	0111 0000 0000 0000	Timing:	4 (3)

Description

If a Busy signal from a selected output device is not present during T7 of C30, K (F14) is set. An odd parity bit is generated and recorded into the high-order A bit, 39. The high-order 8 A bits, 32 through 39, are precessed into the B. An Output Common signal is generated and sent via the interface to the selected output device(s) forcing the device(s) to simultaneously sense all 8 bits of the B. If a Busy signal had been present during T7 of C30, this command is aborted and K reset. Figure 3.46 is a flow chart showing the sequence of events that occur for this command. Figure 1.2 shows the orientation of the output bits to the B and A.

Sequence of Events

A) During C30:
   1) Reset F11 via gate M70, figure 3.65.
   2) Set F14 via gate M111-9, figure 3.68.
   3) Reset F14 at T7 if K176, Busy signal, via gate M106, figure 3.66.
   4) Toggle F10 for every 1's bit of L10 during T7 via gates M96-6 and M96-8, figure 3.63. (Note, F10 is initially reset during C20.)
   5) Record state of $\overline{F10}$ in high-order A bit at T39 if F14 via gate M27-13, figure 3.83. (Note, high-order A bit must equal zero otherwise it would regenerate itself via gate M27-10, figure 3.83, preventing $\overline{F10}$ from being recorded.)
   6) Set "C10 after C30" at T39 if $\overline{F14}$ via gates M25-6, figure 3.54, and M24, figure 3.55.
   7) Set C40 at T39 if F14 via gate M24, figure 3.55.

B) During "C10 after C30" precess next command of instruction word into CR and work from there.

C) During C40:
   1) Precess high-order 8 bits of A into B via gate M125-4, figure 3.70, while contents of B (all 0's due to clearance during C20) are precessed into low-order 8 bits of A via gate M46-2, figure 3.81.

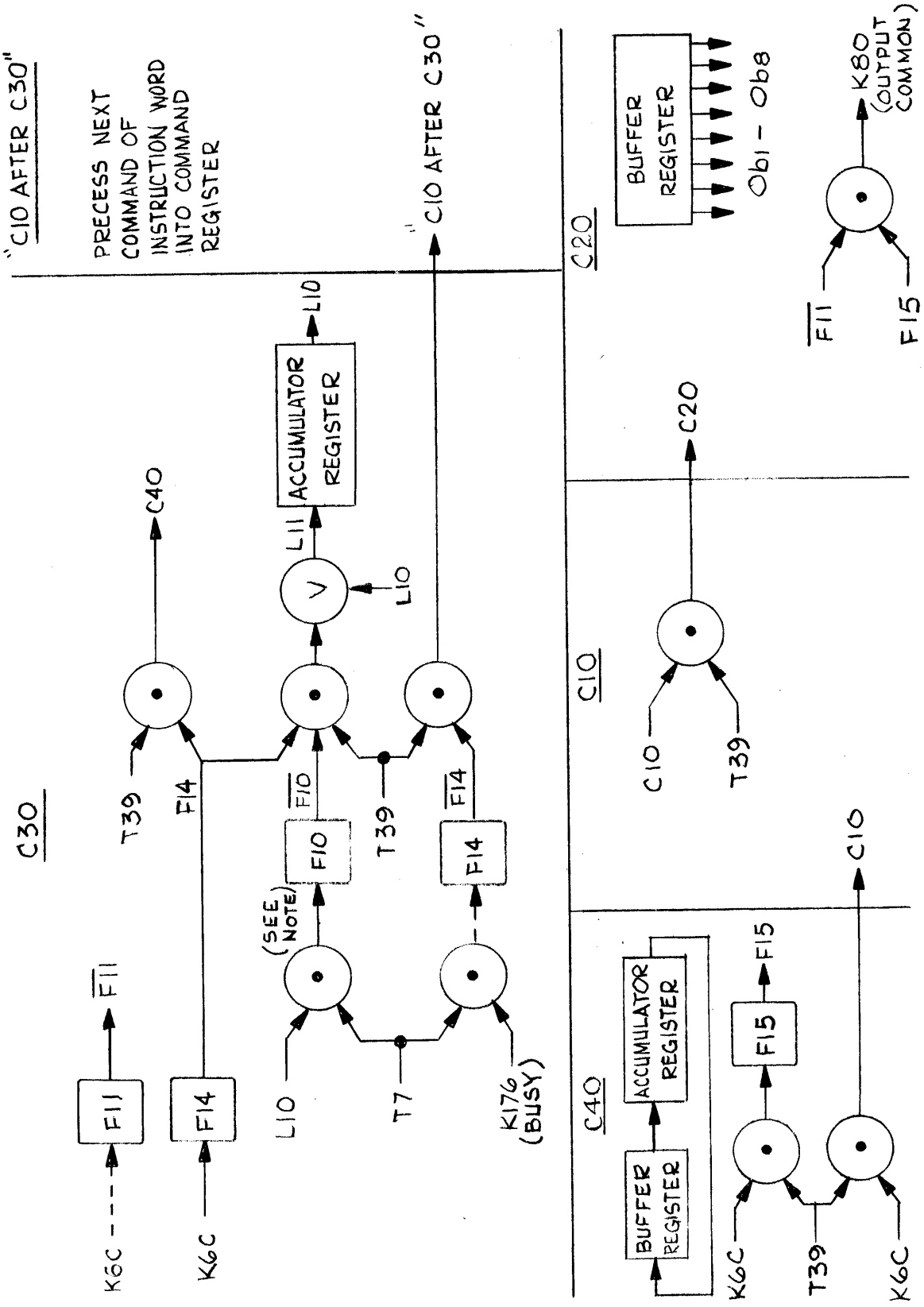
2) Set F15 at T39 via gate M126-3, figure 3.69.
3) Set C10 at T39 via gates M25-6, figure 3.54, and M24, figure 3.55.

D) During C10 set C20 at T39 via gate M13-9, figure 3.55.

E) During C20 generate K80, Output Common signal, via gate M120-12, figure 3.78.

Decoded Signals

$A10 = \overline{F9}\ F10$
$A11 = \overline{F5}\ F7\ M6$
$A14 = \overline{C39} \vee \overline{F14} \vee \overline{(\overline{A11}\ \overline{K9})}$
$A17 = \overline{K6} \vee \overline{C37} \vee \overline{L10}$
$A18 = \overline{F8}\ F7$
$K6 = A18\ A11\ F6$



NOTE: F10 INITIALLY = 0, F10 TOGGLED BY L10 = 1

Figure 3.46 Output Accumulator with Odd Parity Command, Flow Chart.

3.7.44 OUTPUT ACCUMULATOR WITH EVEN PARITY COMMAND (OAE)

Hex Code:	7040	Logic Name:	K6C
Binary Code:	0111 0000 0100 0000	Timing:	4 (3)

Description

This command performs the same operations of the OAO command, paragraph 3.7.43, with one exception. An even parity bit is generated instead of an odd parity bit. Figure 3.47 is a flow chart showing the sequence of events that occur for this command. Figure 1.2 shows the orientation of the output bits to the B and A.

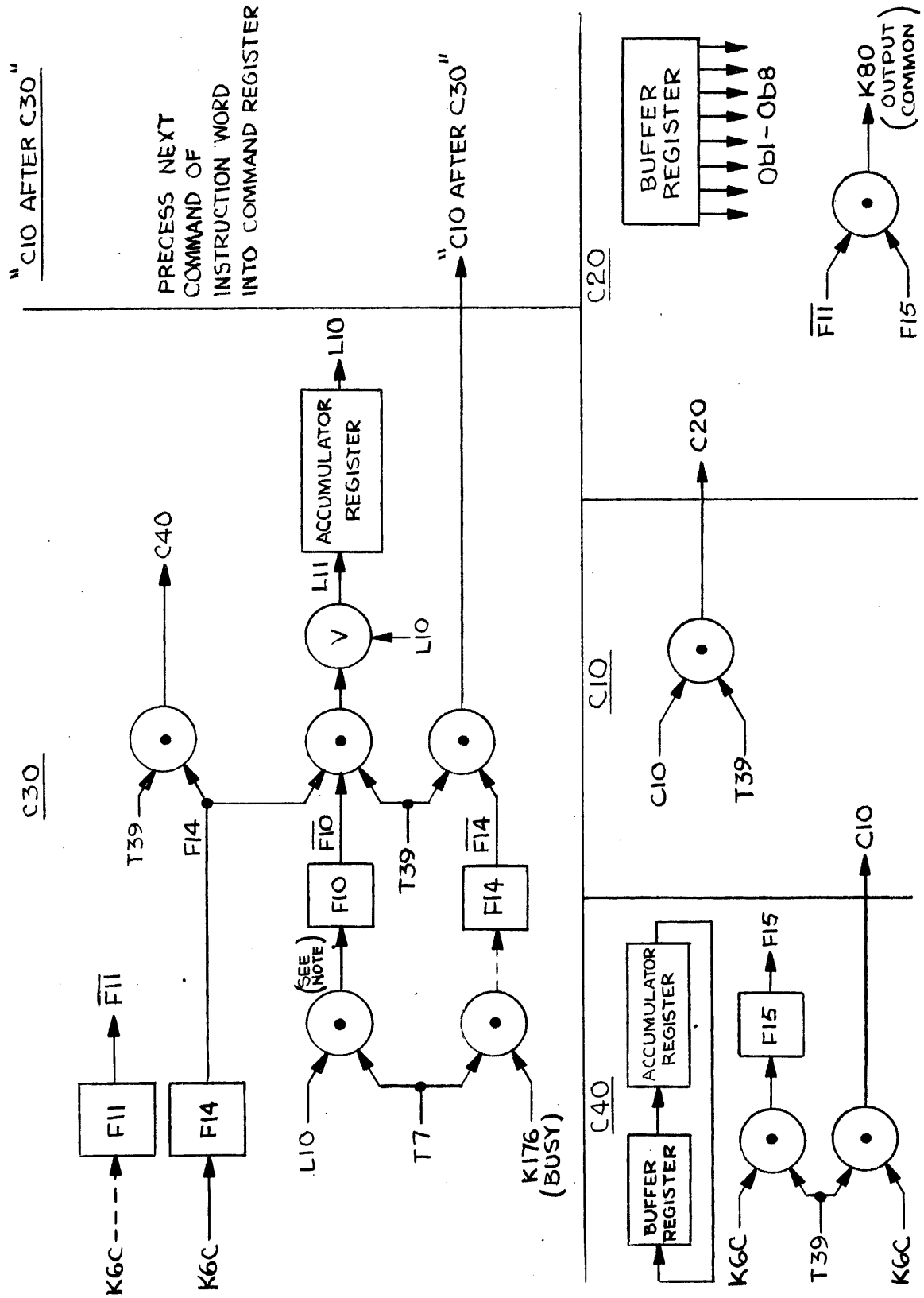
Sequence of Events

A) During C30:
   1) See C30 of OAO command, steps 1 through 3 and 5 through 7, paragraph 3.7.43.
   2) Toggle F10 for every 1's bit of L10 during T7 via gates M96-6 and M96-8, figure 3.63. (Note, F10 is initially set during C20.)

B) See OAO command, B through E, paragraph 3.7.43.

Decoded Signals

See Decoded Signals of OAO command, paragraph 3.7.43.



NOTE: F10 INITIALLY=1, F10 TOGGLED BY L10=1.

Figure 3.47 Output Accumulator with Even Parity Command, Flow Chart.

3.7.45 OUTPUT ACCUMULATOR COMMAND (OA)

Hex Code:	70C0	Logic Name:	K6C
Binary Code:	0111 0000 1100 0000	Timing:	4 (3)

Description

This command performs the same operation of the OAO command, paragraph 3.7.43, except that a parity bit is not generated. Figure 3.48.1 is a flow chart showing the sequence of events that occur for this command. Figure 1.3 shows the orientation of the output bits to B and A.

Sequence of Events

A) During C30 see C30 of OAO command, steps 1, 2, 3, 6, and 7, paragraph 3.7.43.

B) See B through E of OAO command, paragraph 3.7.43.

Decoded Signals

See Decoded Signals of OAO command, paragraph 3.7.43.

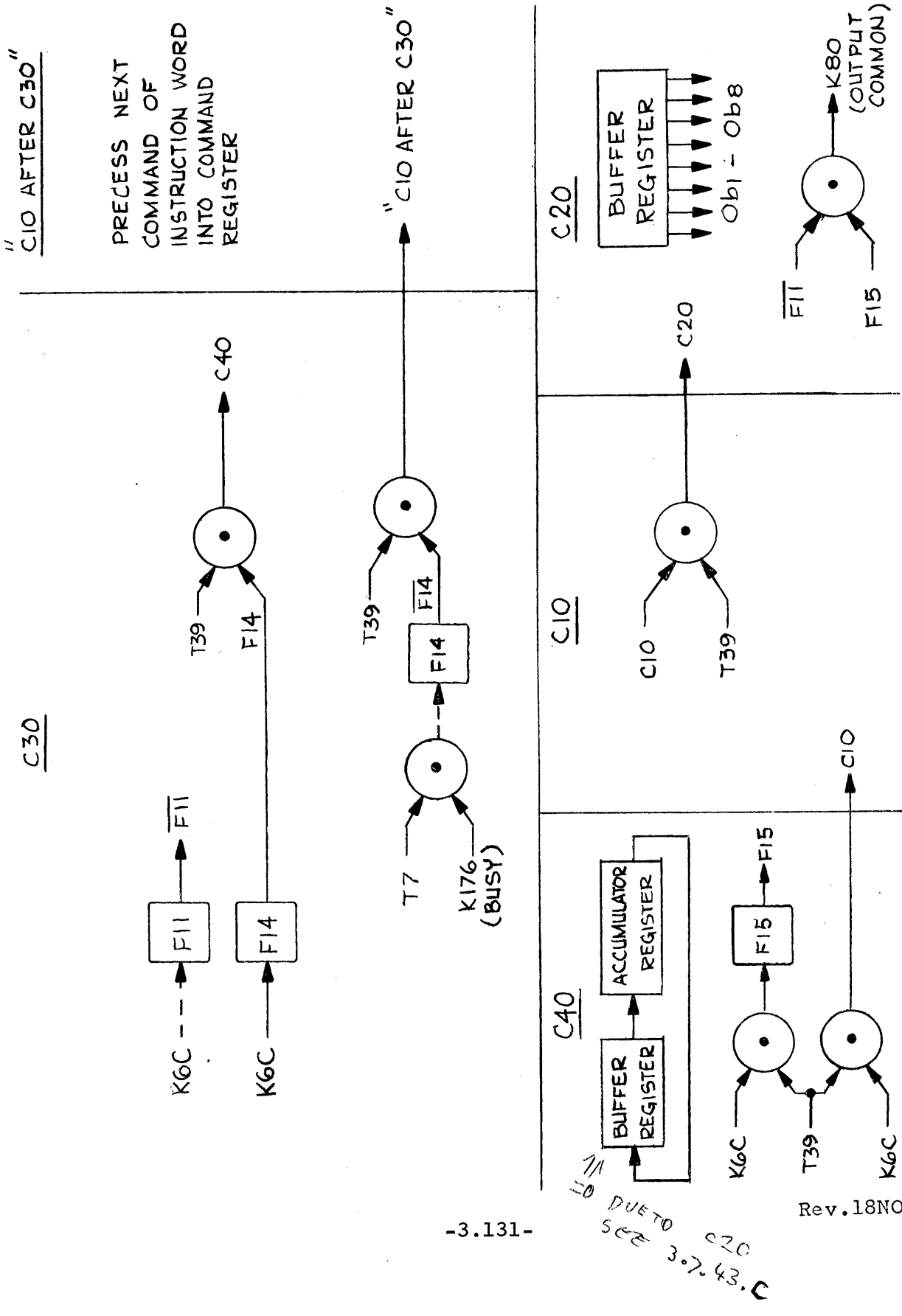


Figure 3.48.1 Output Accumulator Command, Flow Chart.

3.7.46 ACCUMULATOR SELECT ON TEST COMMAND (AST)

Hex Code:	74C0	Logic Name:	K6D
Binary Code:	0111 0100 1100 0000	Timing:	4 (3)

Description

This command causes K (F14) to set if a Busy signal is not present from any output device during T7 of C30. The high-order 8 bits of the A, 32 through 39, are precessed into the B to form the 2 device select code tetrads discussed in paragraph 3.6. A Device Select Common signal is generated and sent via the interface to all I/O devices forcing them to scan their Select and Group Bit inputs, as discussed in paragraph 3.6. If a Busy signal had been present during T7 of C30, this command is aborted and K reset. Figure 3.48.2 is a flow chart showing the sequence of events that would occur for this command. Figure 1.3 shows the orientation of the output bits to the B and A.

Sequence of Events

A) During C30 see C30 of OA0 command, steps 2, 3, 6, and 7, paragraph 3.7.43.

B) During "C10 after C30" precess next command of instruction word into CR and work from there.

C) During C40:
   1) Precess high-order 8 bits of A into B via gate M125-4, figure 3.70, while contents of B (all 0's due to clearance during C20) are precessed into low-order 8 bits of A via gate M46-2, figure 3.81.
   2) Set F11 via gate M71-12, figure 3.64.
   3) Set F15 at T39 via gate M126-3, figure 3.69.
   4) Set C10 at T39 via gates M25-6, figure 3.54.

D) During C10 set C20 at T39 via gate M13-9, figure 3.55.

E) During C20 set K82, Device Select Common signal, via gate M120-6, figure 3.78.

Decoded Signals

See Decoded Signals of OA0 command, paragraph 3.7.43.

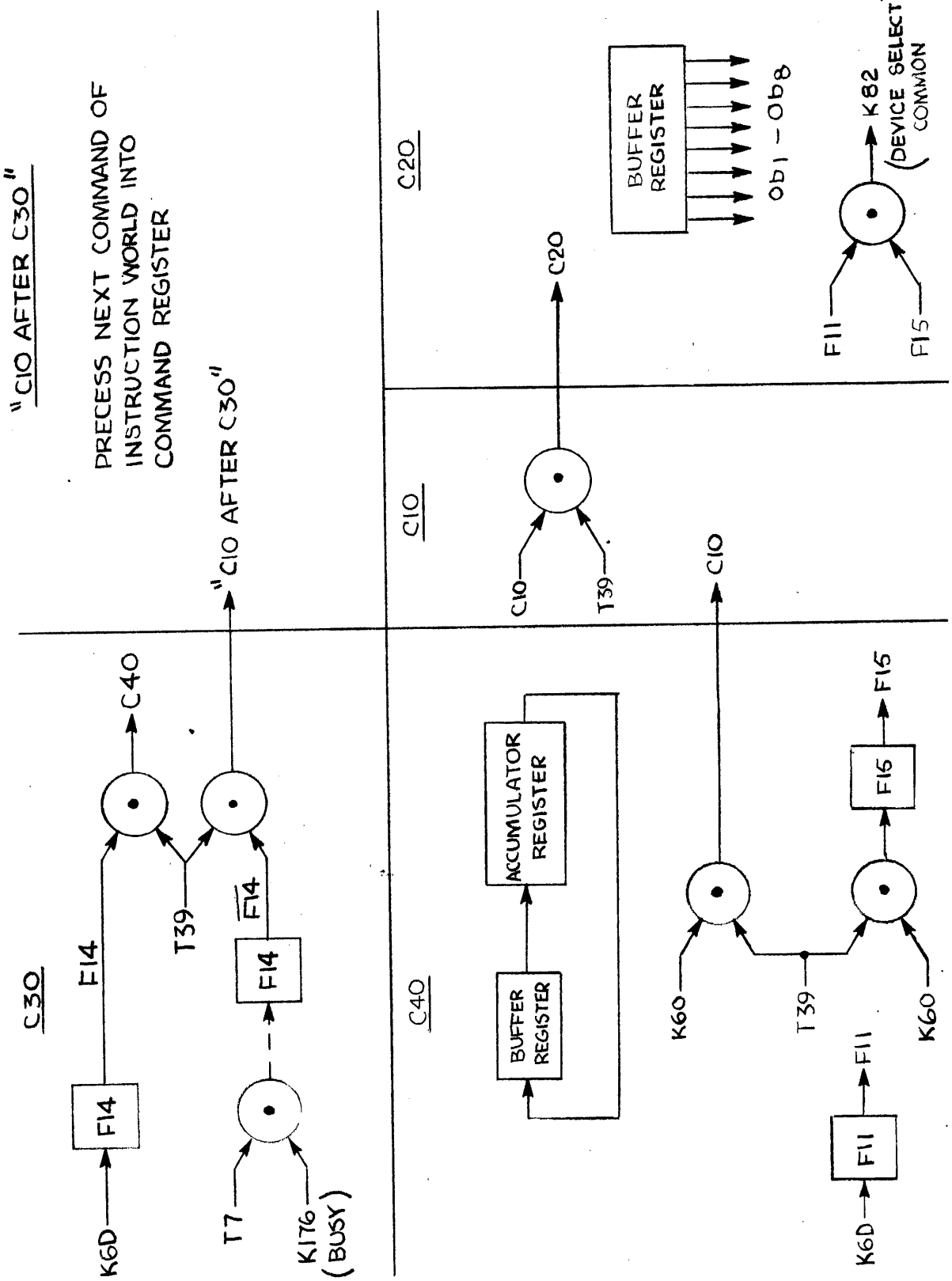


Figure 3.48.2 Accumulator Select on Test Command, Flow Chart.

3.7.47 ACCUMULATOR SELECT COMMAND (AS)

Hex Code:	76C0	Logic Name:	K6D
Binary Code:	0111 0110 1100 0000	Timing:	4

Description

This command causes K (F14) to set. The high-order 8 bits of A, 32 through 39, are then precessed into B to form the 2 tetrads of the device select code discussed in paragraph 3.6. A Device Select Common signal is generated and sent via the interface to all I/O devices forcing them to scan their Select and Group Bit inputs, as discussed in paragraph 3.6. Figure 3.48.3 is a flow chart showing the sequence of events that occur for this command. Figure 1.3 shows the orientation of the output bits to the B and A.

Sequence of Events

A) During C30:
   1) Set F14 via gate M111-9, figure 3.68.
   2) Set C40 at T39 via gate M24, figure 3.55.

B) See AST command, C through E, paragraph 3.7.46.

Decoded Signals

See Decoded Signals of OAO command, paragraph 3.7.43.

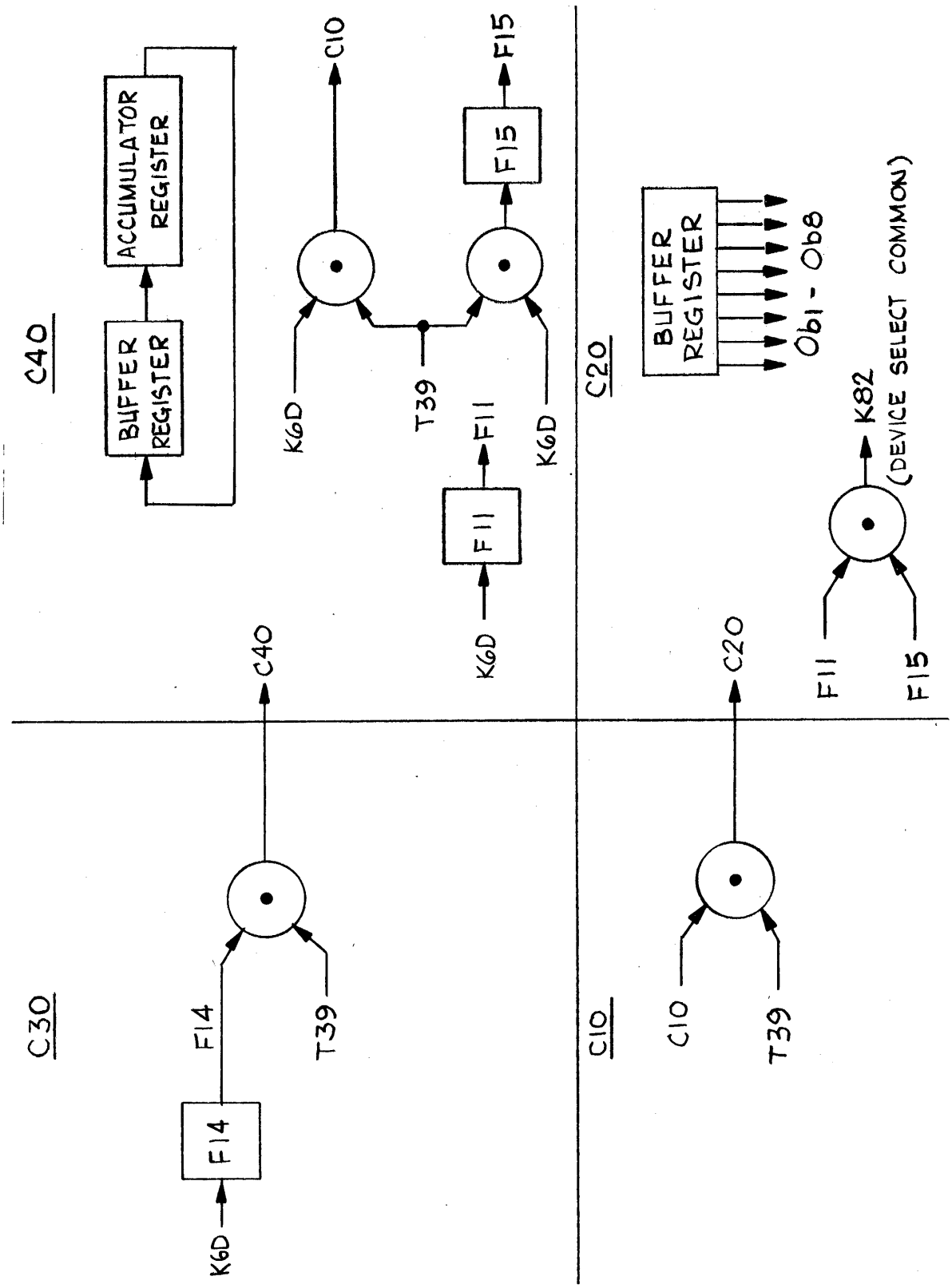


Figure 3.48.3 Accumulator Select Command, Flow Chart.

Rev.18NOV68

3.7.48 OUTPUT IMMEDIATE COMMAND (OI)

Hex Code:	7800+C	Logic Name:	K6A
Binary Code:	0111 1000 CCCC CCCC	Timing:	4 (3)

Description

This command causes the K (F14) to set if a Busy signal from a selected output device is not present during T7 of C30. The high-order 8 bits (C) of the I, 32 through 39, are then precessed into the B while the I regenerates itself. An Output Common signal is generated and sent via the interface to the output devices forcing the selected output devices to sense the 8 bits of the B output. If a Busy signal had been present during T7 of C30, this command is aborted and the K reset. Figure 3.48.4 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30 see C30 of OAO command, steps 1, 2, 3, 6, and 7, paragraph 3.7.43.

B) During "C10 after C30" precess next command of instruction word into CR and work from there.

C) During C40:
   1) Precess high-order 8 bits of I into B via gate M118, figure 3.70.
   2) Regenerate I via gate M16, figure 3.85.
   3) Set F15 at T39 via M126-3, figure 3.69.
   4) Set C10 at T39 via gates M25-6, figure 3.54.

D) During C10 set C20 at T39 via gate M13-9, figure 3.55.

E) During C20 set K80, Output Common signal, via gate M120-12, figure 3.78.

Decoded Signals

See Decoded Signals of OAO command, paragraph 3.7.43.

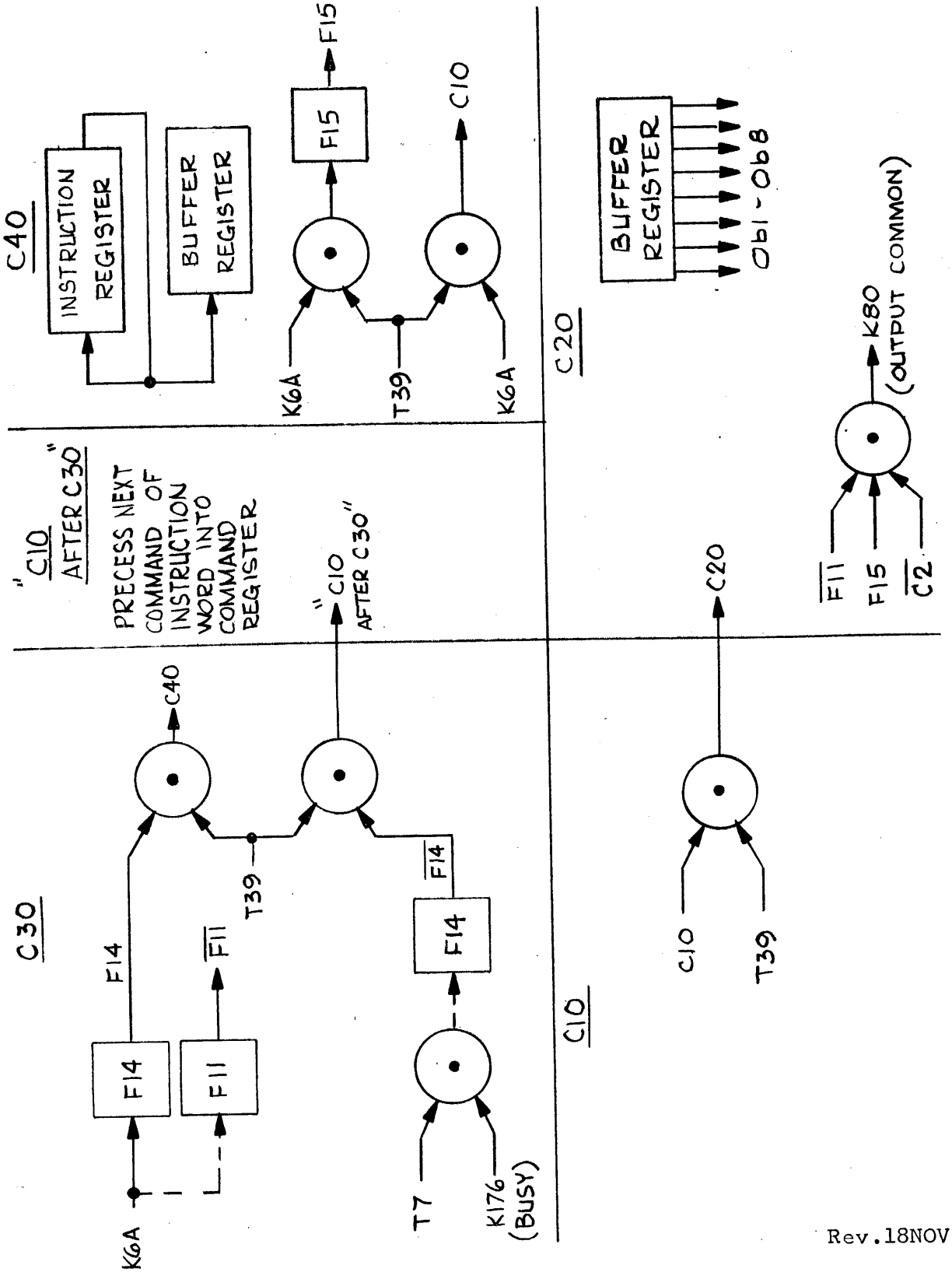


Figure 3.48.4 Output Immediate Command, Flow Chart.

Rev.18NOV68

3.7.49 IMMEDIATE SELECT ON TEST COMMAND (IST)

Hex Code:	7C00+D	Logic Name:	K6B
Binary Code:	0111 1100 DDDD DDDD	Timing:	4 (3)

Description

This command causes K (F14) to set if a Busy signal is not present from any output device during T7 of C30. The high-order 8 bits of I, 32 through 39, are then precessed into the B while I regenerates itself. The 8 bits contained in B form the 2 device select code tetrads discussed in paragraph 3.6. A Device Select Common signal is generated and sent via the interface to all I/O devices forcing them to scan their Select and Group Bit inputs, as discussed in paragraph 3.6. If a Busy signal had been present during T7 of C30, this command is aborted and K reset. Figure 3.48.5 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30 see C30 of OAO command, steps 2, 3, 6, and 7, paragraph 3.7.43.

B) During "C10 after C30" precess next command of instruction word into CR and work from there.

C) During C40:
   1) Precess high-order 8 bits of I into B via gate M118, figure 3.70.
   2) Regenerate I via gate M16, figure 3.85.
   3) Set F11 via gate M71-12, figure 3.64.
   4) Set F15 at T39 via gate M126-3, figure 3.69.
   5) Set C10 at T39 via gates M25-6, figure 3.54.

D) During C10 set C20 at T39 via gate M13-9, figure 3.55.

E) During C20 set K82, Device Select Common signal, via gate M120-6, figure 3.78.

Decoded Signals

See Decoded Signals of OAO command, paragraph 3.7.43.

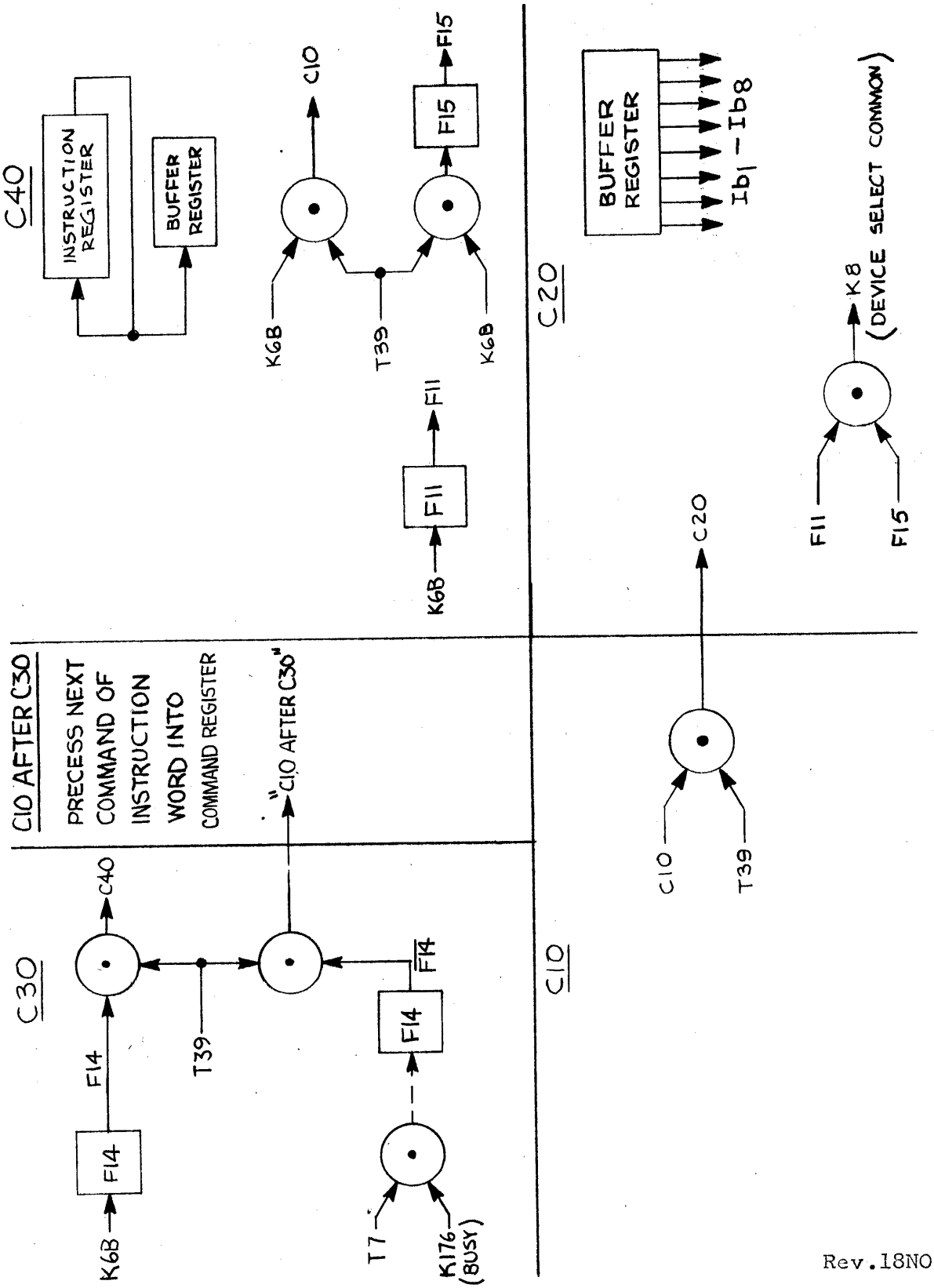


Figure 3.48.5 Immediate Select on Test Command, Flow Chart.

Rev.18NOV68

3.7.50 IMMEDIATE SELECT COMMAND (IS)

Hex Code:	7E00+D	Logic Name:	K6B
Binary Code:	0111 1110 DDDD DDDD	Timing:	4

Description

This command causes K (F14) to set. The high-order 8 I bits, 32 through 39, are then precessed into the B while the I regenerates itself. The 8 bits of the B form the 2 device select code tetrads discussed in paragraph 3.6. A Device Select Common signal is generated and sent via the interface to all I/O devices forcing them to scan their Select and Group Bit inputs, as discussed in paragraph 3.6. Figure 3.48.6 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C30:
   1) Set F14 via gate M111-9, figure 3.68.
   2) Set C40 at T39 via gate M24, figure 3.55.

B) See IST command, C through E, paragraph 3.7.49.

Decoded Signals

See Decoded Signals of OAO command, paragraph 3.7.43.

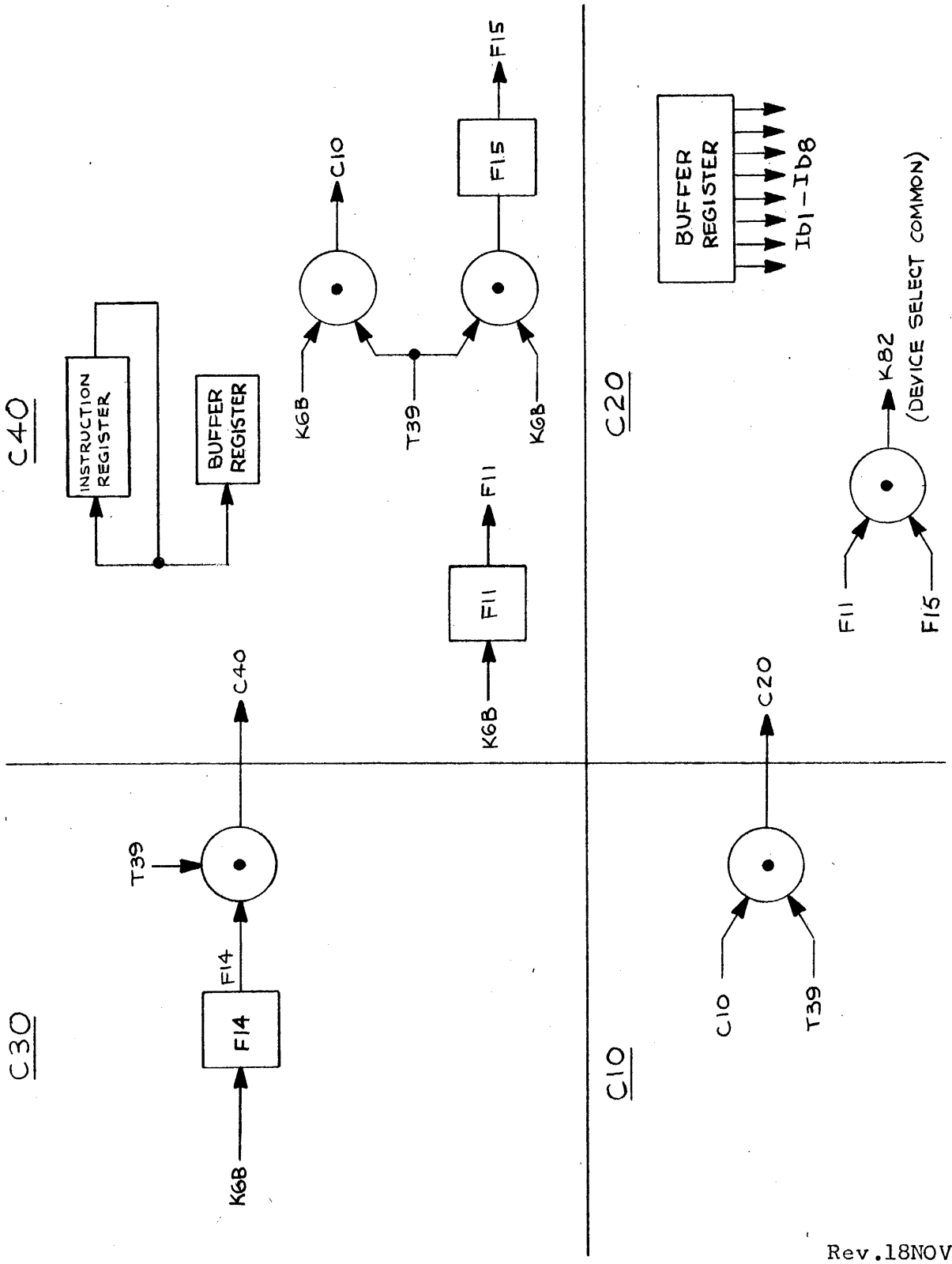


Figure 3.48.6 Immediate Select Command, Flow Chart.

Rev.18NOV68

3.7.51 CLEAR AND ADD COMMAND (CA)

Hex Code:	8000+M	Logic Name:	K14
Binary Code:	1000 tttt tsss ssss	Timing:	4+ma

Description

This command causes the contents of M to be transferred to the A. Figure 3.48.7 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C20:
   1) Reset F10 via gate M78-12, figure 3.63.
   2) Set F10 if F1 during T4 via gate M79-12, figure 3.63. (Note, high-order 5 bits of I are sensed as a result.)
   3) Set C30 at T39 via gate M14-9, figure 3.54.

B) During C30:
   1) Set F10 if F1 $\cdot$ $\overline{F2}$ v F3 v F4 via gate M79-9, figure 3.63.
   2) Reset F11 at $\overline{T4}$ $\overline{T7}$ via gate M70, figure 3.65.
   3) Set F11 if Z3 $\neq$ L20 during T7 if F10 via gate M77, figure 3.64.
   4) Set F11 if Z3 $\neq$ L20 during $\overline{T4}$ T7 if $\overline{F10}$ via gate M77, figure 3.64.
   5) Set C40 at T39 if $\overline{F11}$ via gate M33-6, figure 3.55.

C) During C40:
   1) Transfer contents of M into A via gates M56-8, figure 3.91, and M36-12, figure 3.81.
   2) Set C10 at T39 via gate M25-8, figure 3.54.

Decoded Signals

A2 = $\overline{C1}$ A3
A3 = $\overline{M1}$ v $\overline{S6}$ v W2
A9 = F8 M6
A18 = $\overline{F8}$ $\overline{F7}$
A37 = $\overline{F1}$ $\overline{F2}$

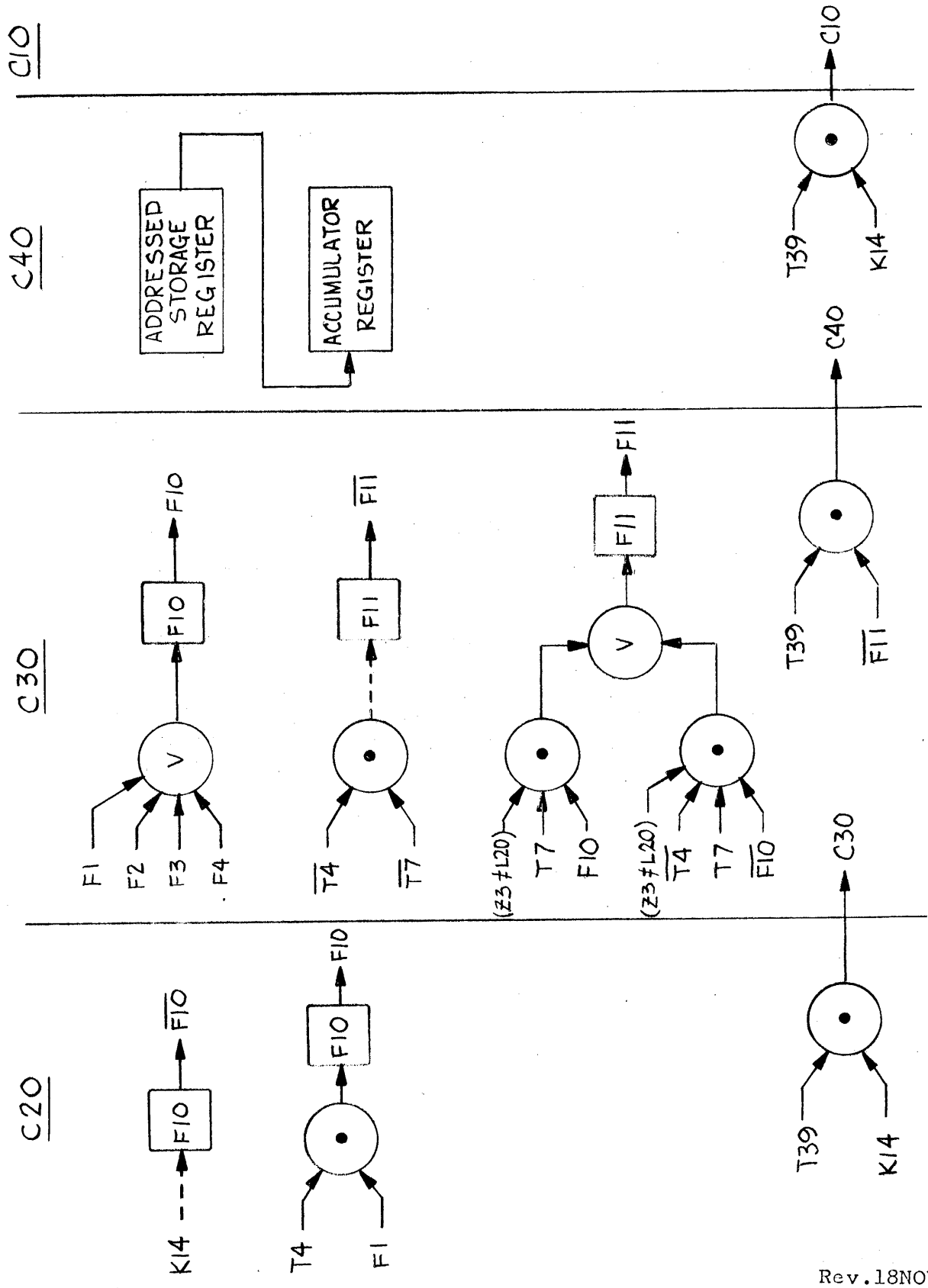


Figure 3.48.7 Clear and Add Command, Flow Chart.

Rev.18NOV68

3.7.52 ADD COMMAND (AD)

Hex Code:	9000+M	Logic Name:	K16
Binary Code:	1001 tttt tsss ssss	Timing:	4+ma

Description

This command causes the contents of M to be added to the contents of the A. K (F14) stores the carry bit. Figure 3.48.8 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C20 see C20 of CA command, steps 1 through 3, paragraph 3.7.51.

B) During C30:
   1) See C30 of CA command, steps 1 through 5, paragraph 3.7.51.
   2) Reset F14 at T39 if $\overline{F11}$ via gate M95, figure 3.67.

C) During C40:
   1) Establish L50 equal to M playback via gates M56-8, figure 3.91, and M88-5, figure 3.89.
   2) Establish L51 = L10 via gate M67-1, figure 3.90.
   3) Add L50 to L51 in adder/subtractor, figure 3.90, and record the sum, L53, into A via gate M36-9, figure 3.81. (Note, F14 is set if L50 L51; reset if $\overline{L50}$ $\overline{L51}$.)
   4) Set C10 at T39 via gate M25-8, figure 3.54.

Decoded Signals

$A2 = C1\ \overline{A3}$
$A3 = \overline{M1} \vee \overline{S6} \vee W2$
$A9 = F8\ M6$
$A18 = \overline{F8}\ F7$
$A37 = \overline{F1}\ \overline{F2}$
$A38 = F5\ \overline{F6}$
$K13 = \overline{A9} \vee \overline{A38}$

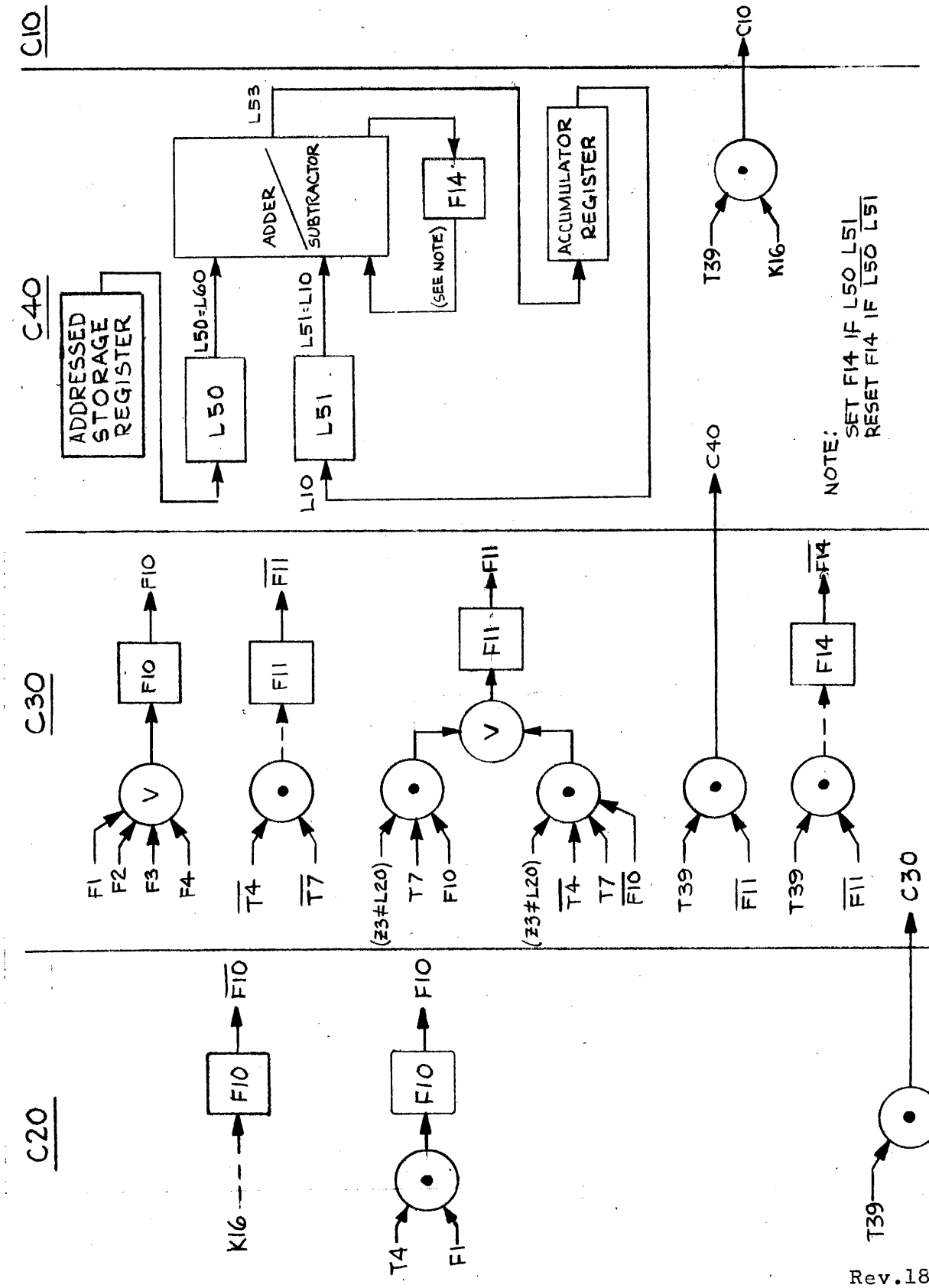


Figure 3.48.8 Add Command, Flow Chart.

Rev.18NOV68

3.7.53 STORE COMMAND (ST)

Hex Code:	B000+M	Logic Name:	K15
Binary Code:	1011 tttt tsss ssss	Timing:	4+ma

Description

This command causes the contents of the A to be transferred into the M. In cases where M specifies a general storage location, it should be remembered from paragraph 3.4.1 that information to be recorded into general storage must be recorded one bit-time early to compensate for various record-playback time delays. Figure 3.48.9 is a flow chart showing the sequence of events that occurs for this command.

Sequence of Events

A) During C20 see C20 of CA command, steps 1 through 3, paragraph 3.7.51.

B) During C30:
   1) See C30 of CA command, steps 1 through 5, paragraph 3.7.51.
   2) Enable general storage record, L41, if F10 $\overline{\text{F11}}$ at T39 via gate M52-8, figure 3.88, and record L19 into general storage via gates M143-6 and M143-8, figure 3.88.

C) During C40:
   1) Enable general storage record, L41, if F10 $\overline{\text{F11}}$ $\overline{\text{T39}}$ via gate M52, figure 3.88, and record L19 into general storage via gates M43-6 and M43-8, figure 3.88.
   2) Record L10 into S if $\overline{\text{F10}}$ via gate M51, figure 3.87.
   3) Set C10 at T39 via gate M25-8, figure 3.54.

Decoded Signals

K46 = A9 F5 F6 $\overline{\text{F7}}$
See Decoded Signals of CA command, paragraph 3.7.51.

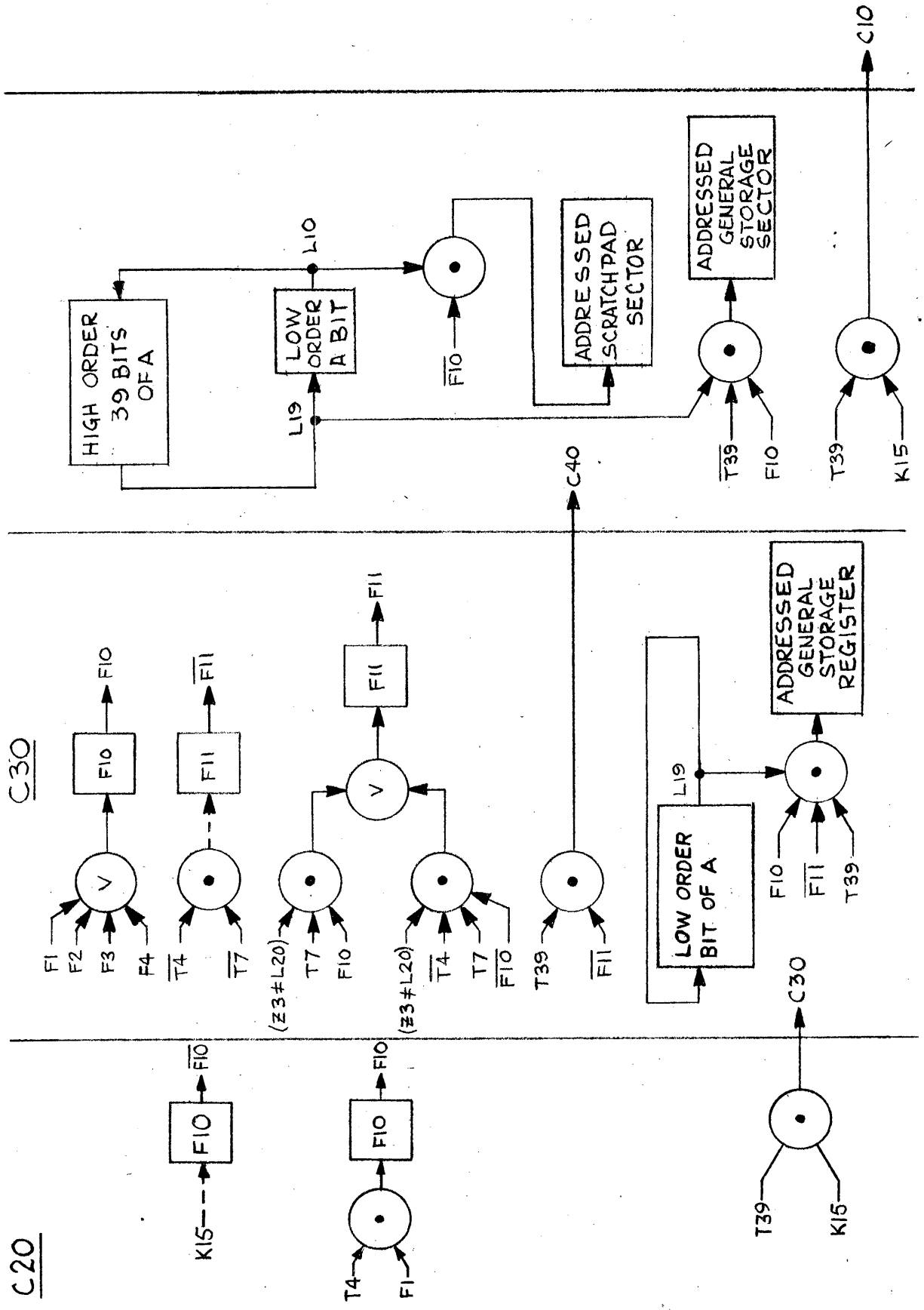


Figure 3.48.9 Store Command, Flow Chart.

3.7.54 JUMP MARK COMMAND (JM)

Hex Code:	C000+M	Logic Name:	K10
Binary Code:	1100 tttt tsss ssss	Timing:	4+ma

Description

This command causes the contents of M to be transferred into the I while the contents of the I are transferred into the A. Upon completion of execution, this command is converted into a JU command and is precessed back into the I as such. Figure 3.48.10 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C20 see C20 of CA command, steps 1 through 3, paragraph 3.7.51.

B) During C30 see C30 of CA command, steps 1 through 5, paragraph 3.7.51.

C) During C40:
   1) Record L20 into A via gate M27-2, figure 3.81.
   2) Record L30 into I if F10 via gates M56-9, figure 3.91, and M1-9, figure 3.85.
   3) Record L40 into I if F10 via gates M56-13, figure 3.91, and M1-9, figure 3.85.
   4) Set C10 at T39 via gate M25-8, figure 3.54.

Decoded Signals

K14 = A9 A38 F7
See Decoded Signals of AD command, paragraph 3.7.52.

IFM = 300, 300: 01 02 03 04 05, A = XXXX XXXX XX

CRH = C300 06 07 E340, (ie: INSTRUCTION CAME FROM AREA 3, AND WAS 40 C300 0607)

THEN

CR+I = 02 03 04 0C E3 01 (IE. JUMP U TO 300, AND TREAT TOP BYTE (01) AS A PARTIAL ADDRESS. THIS IS NORMAL FOR JU)

OLD A IS LOST

A = 00 06 07 E3 40

TO RETURN FROM A SUBROUTINE, EITHER STORE A IN A MEMORY LOCATION AND JUMP TO IT, OR DO A BLS 8 ⇒ 4007 AND THEN DO A 'JA' ⇒ OD. BOTH METHODS WILL GIVE CONTINUATION, WITH 06 07 E340 XX. THE 5TH TETRAD WILL ALWAYS BE E (JU) SO THE XX DOESN'T MATTER

(IF NOT SCRATCHPAD, IT WILL TAKE A FULL REV!) AT ~128 TIME IS 348

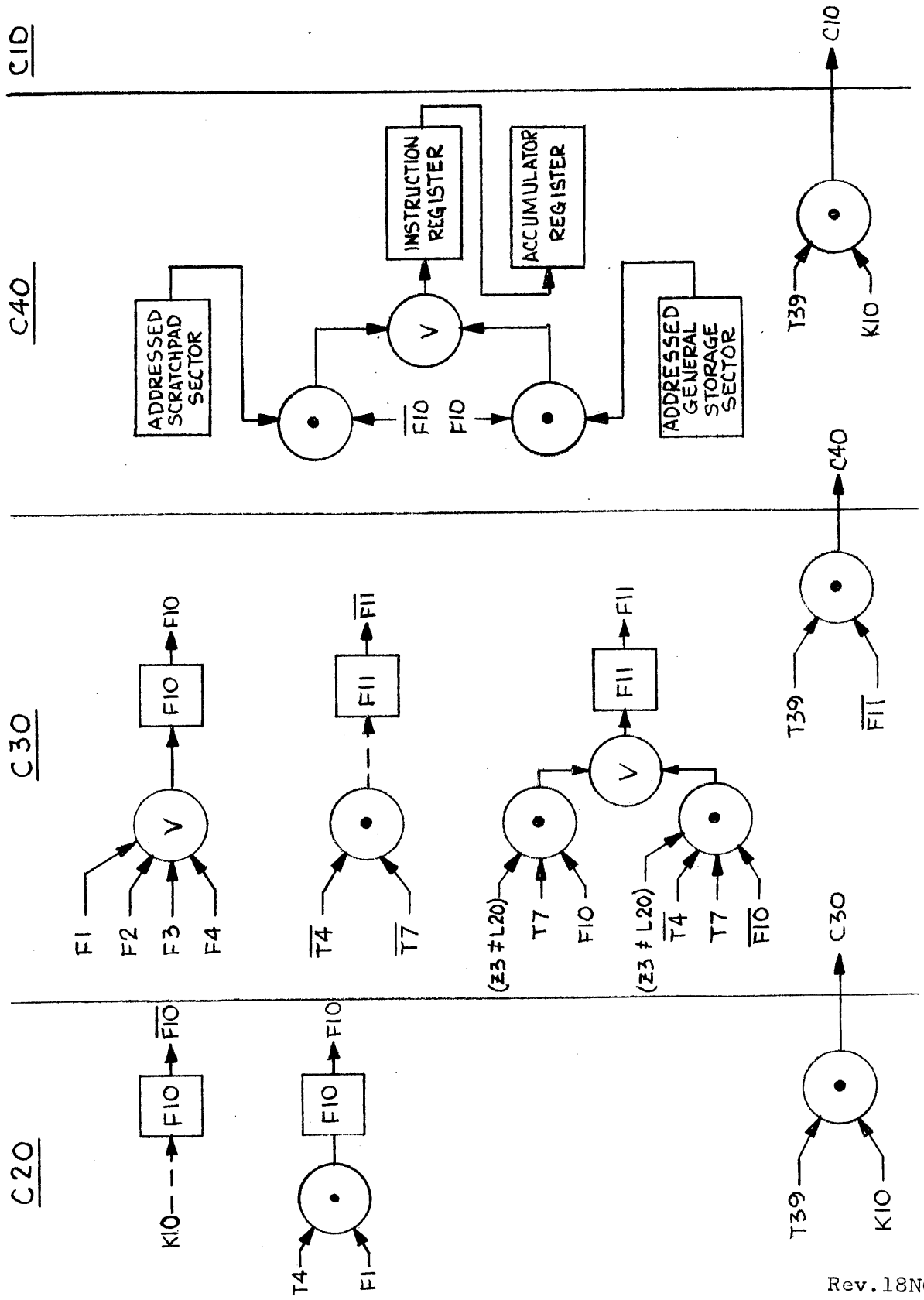


Figure 3.48.10 Jump Mark Command, Flow Chart.

Rev.18NOV68

3.7.55 ADD CONDITIONAL COMMAND (AC)

Hex Code:	D000+M	Logic Name:	K12
Binary Code:	1101 tttt tsss ssss	Timing:	4+ma (3)

Description

If K (F14) is in the set state at the start of this command's execution, this command performs the same operations that the AD command, paragraph 3.7.52, performs. If, however, K is in the reset state, this command is aborted and the next command of the instruction word is precessed into the CR. Figure 3.48.11 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C20 see C20 of CA command, steps 1 through 3, paragraph 3.7.51.

B) During C30:
   1) See C30 of CA command, steps 1 through 4, paragraph 3.7.51.
   2) Reset F14 at T39 if $\overline{F11}$ via gate M95-4, figure 3.67.
   3) Set C40 at T39 if F14 $\overline{F11}$ via gate M33-6, figure 3.55.
   4) Set C10 at T39 if $\overline{F14}$ via gate M25-6, figure 3.54.

C) During C40 see C40 of AD command, steps 1 through 4, paragraph 3.7.52.

Decoded Signals

A14 = $\overline{C39}$ v F14 v ($\overline{A11}$ $\overline{K9}$)
See Decoded Signals of AD command, paragraph 3.7.52.

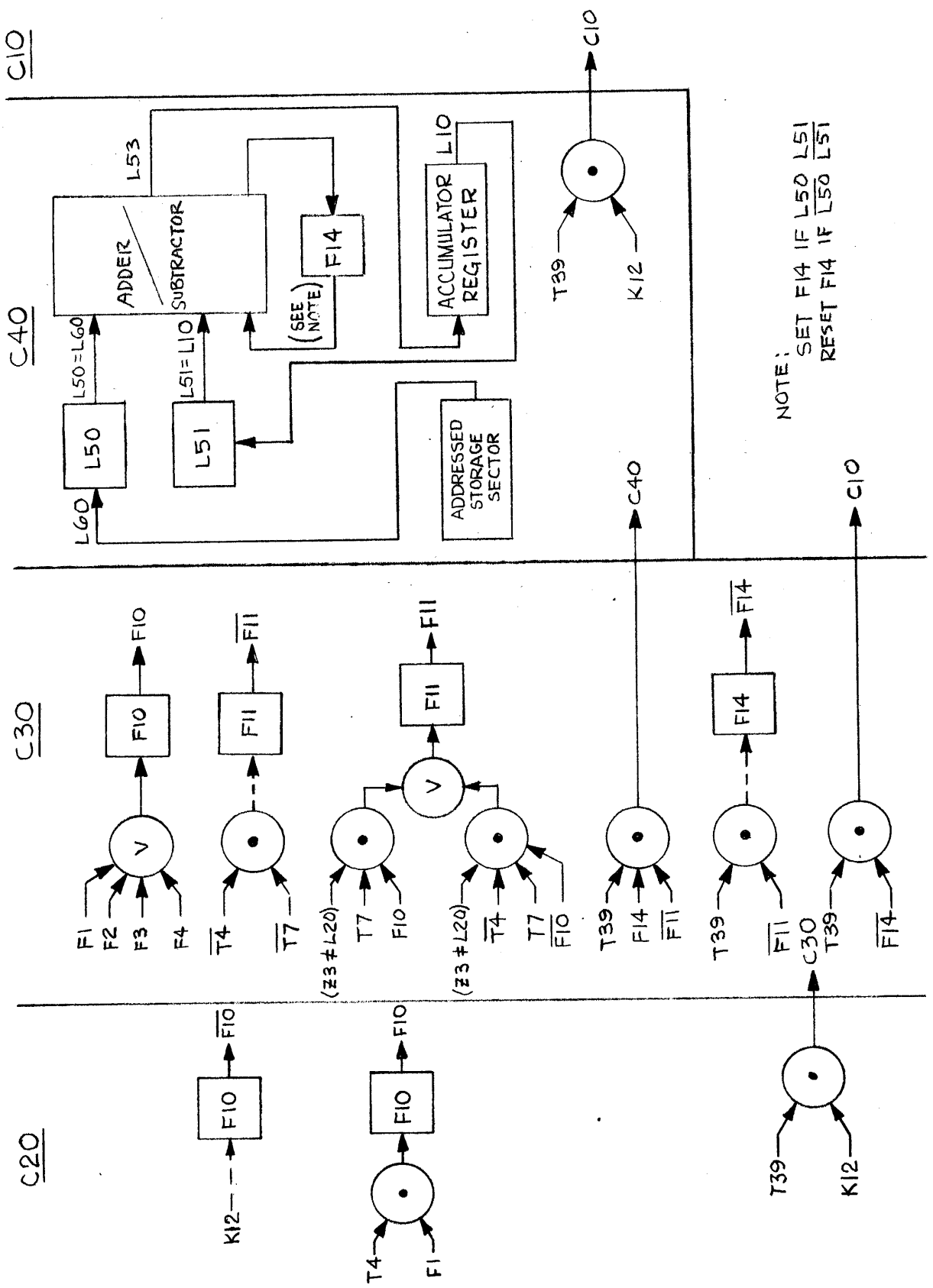


Figure 3.48.11 Add Conditional Command, Flow Chart.

3.7.56 JUMP UNCONDITIONAL COMMAND (JU)

Hex Code:	E000+M	Logic Name:	K8
Binary Code:	1110 tttt tsss ssss	Timing:	4+ma

Description

This command causes the contents of M to be transferred into the I. The original contents of the I are destroyed. Figure 3.48.12 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C20 see C20 of CA command, steps 1 through 3, paragraph 3.7.51.

B) During C30 see C30 of CA command, steps 1 through 5, paragraph 3.7.51.

C) During C40 see C40 of JM command, steps 2 through 4, paragraph 3.7.54.

Decoded Signals

See Decoded Signals of AD command, paragraph 3.7.52.

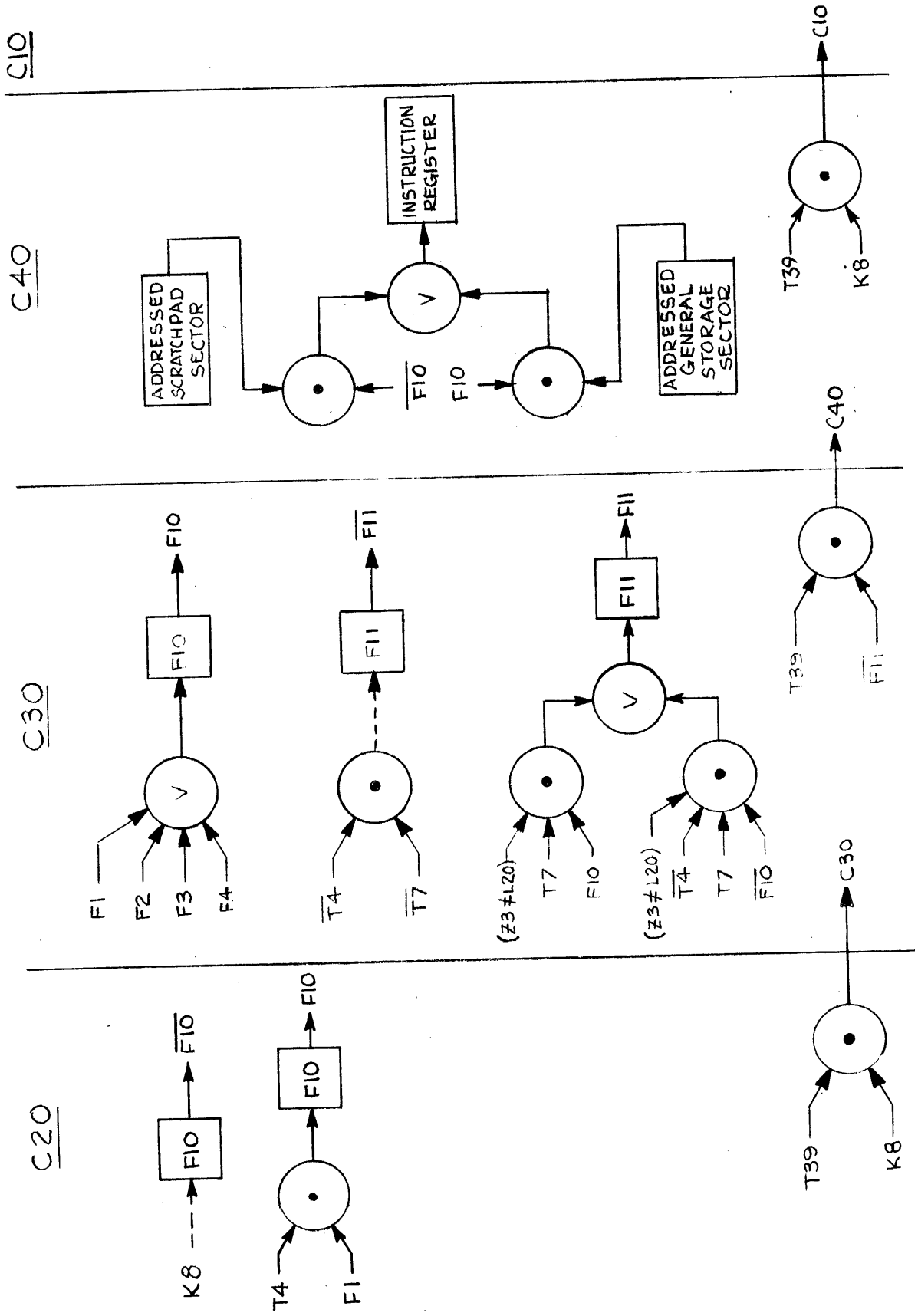


Figure 3.48.12 Jump Unconditional Command, Flow Chart.

3.7.57 JUMP CONDITIONAL COMMAND (JC)

Hex Code:	F000+M	Logic Name:	K11
Binary Code:	1111 tttt tsss ssss	Timing:	4+ma (3)

Description

This command causes the contents of M to be transferred into the I if K (F14) is in the set state before the start of this command's execution. The original contents of the I are destroyed when the contents of the M are transferred into it. Upon completion of execution, this command is converted into a JU command and is precessed back into the I as such. If K had been in the reset state at the start of this command, this command is aborted and the next command of the instruction word is precessed into the CR. Figure 3.48.13 is a flow chart showing the sequence of events that occur for this command.

Sequence of Events

A) During C20 see C20 of CA command, steps 1 through 3, paragraph 3.7.51.

B) During C30:
   1) See C30 of CA command, steps 1 through 4, paragraph 3.7.51.
   2) Set C40 at T39 if $\underline{F14}\ \overline{F11}$ via gate M33-6, figure 3.55.
   3) Set C10 at T39 if $\overline{F14}$ via gate M25-6, figure 3.54.

C) During C40 see C40 of JM command, steps 2 through 4, paragraph 3.7.54.

Decoded Signals

See Decoded Signals of AD command, paragraph 3.7.52.

JUMP IF K=1

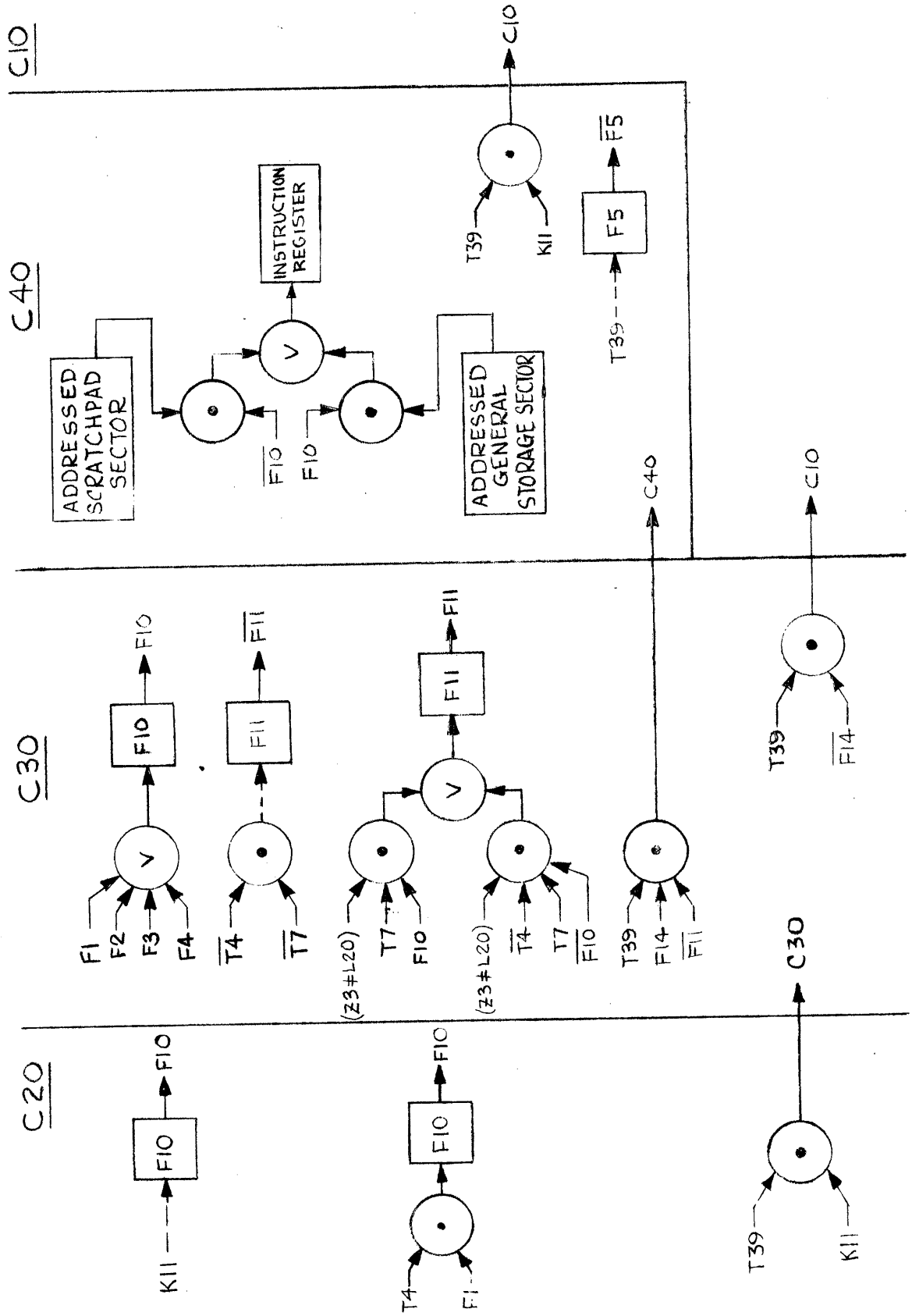


Figure 3.48.13 Jump Conditional Command, Flow Chart.

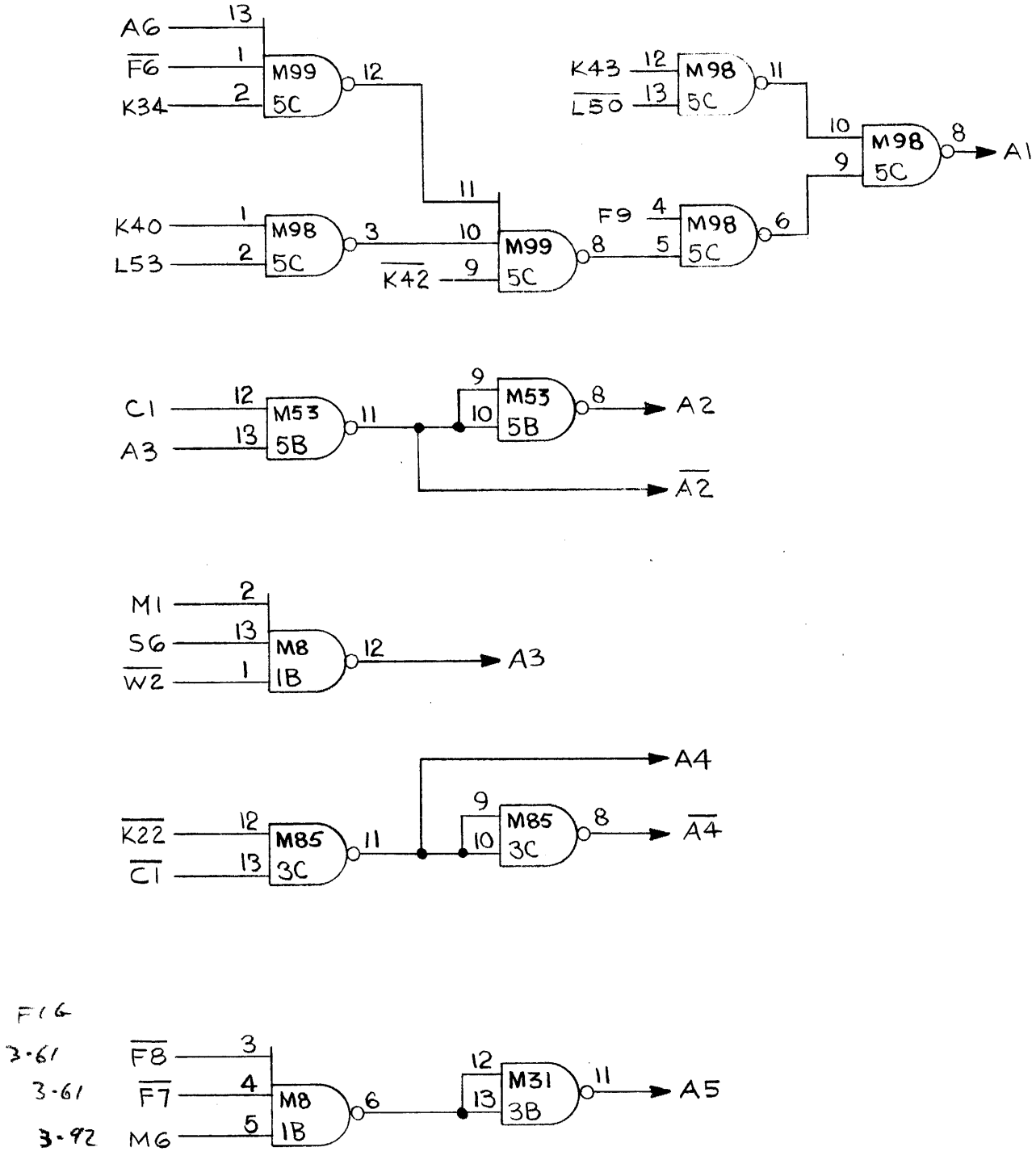


FIG
3-61
3-61
3-92

Figure 3.49 Logic Diagram.

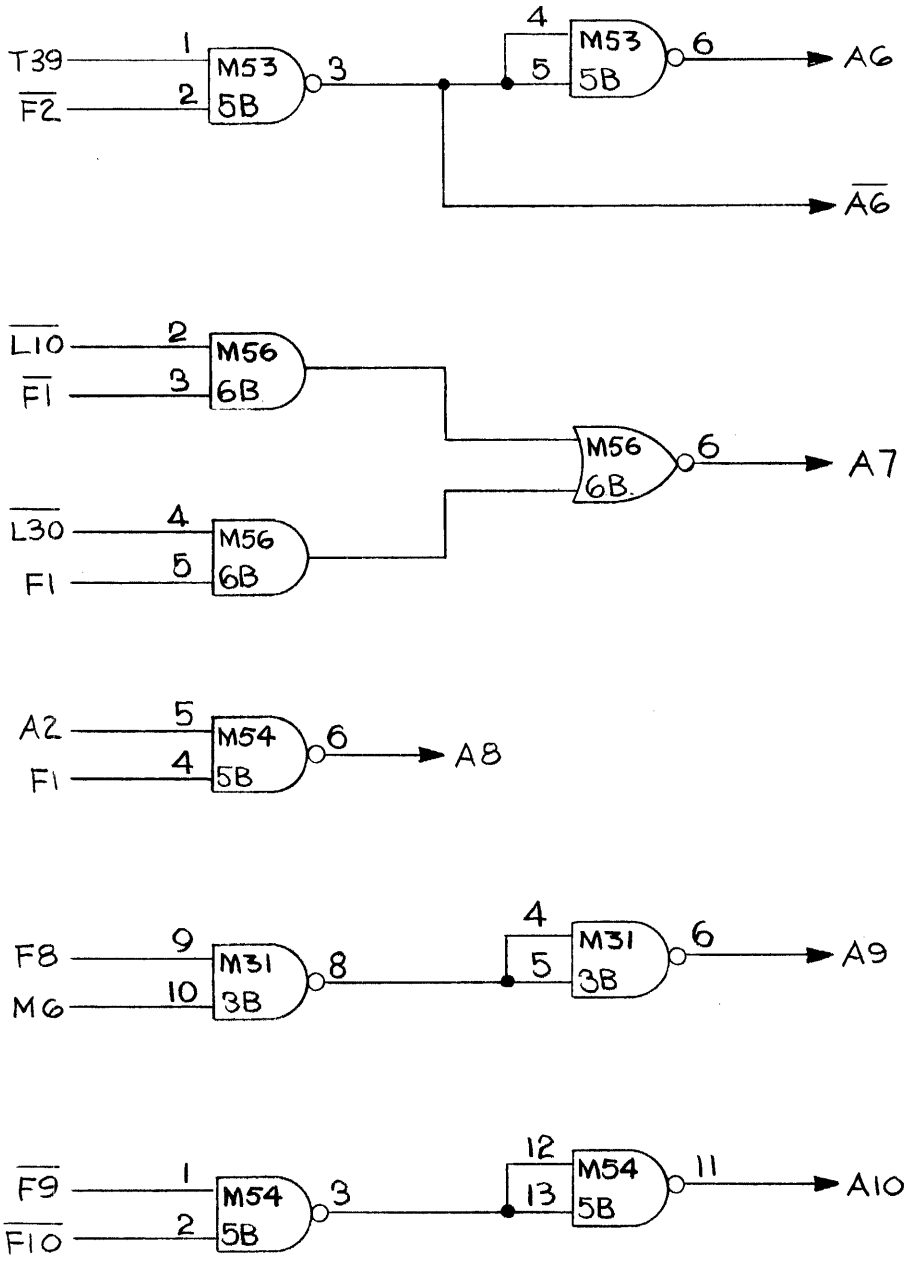


Figure 3.50 Logic Diagram.

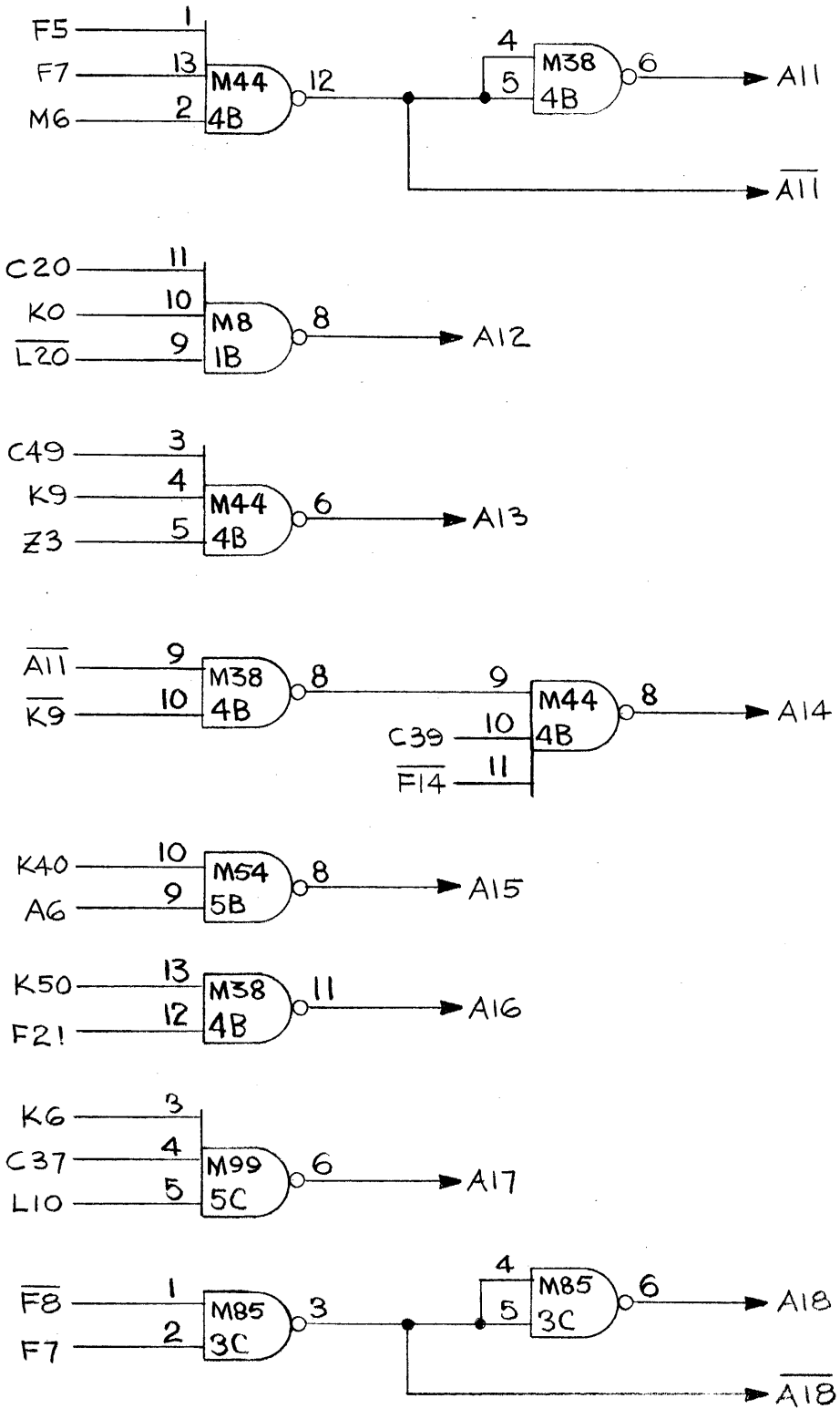


Figure 3.51 Logic Diagram.

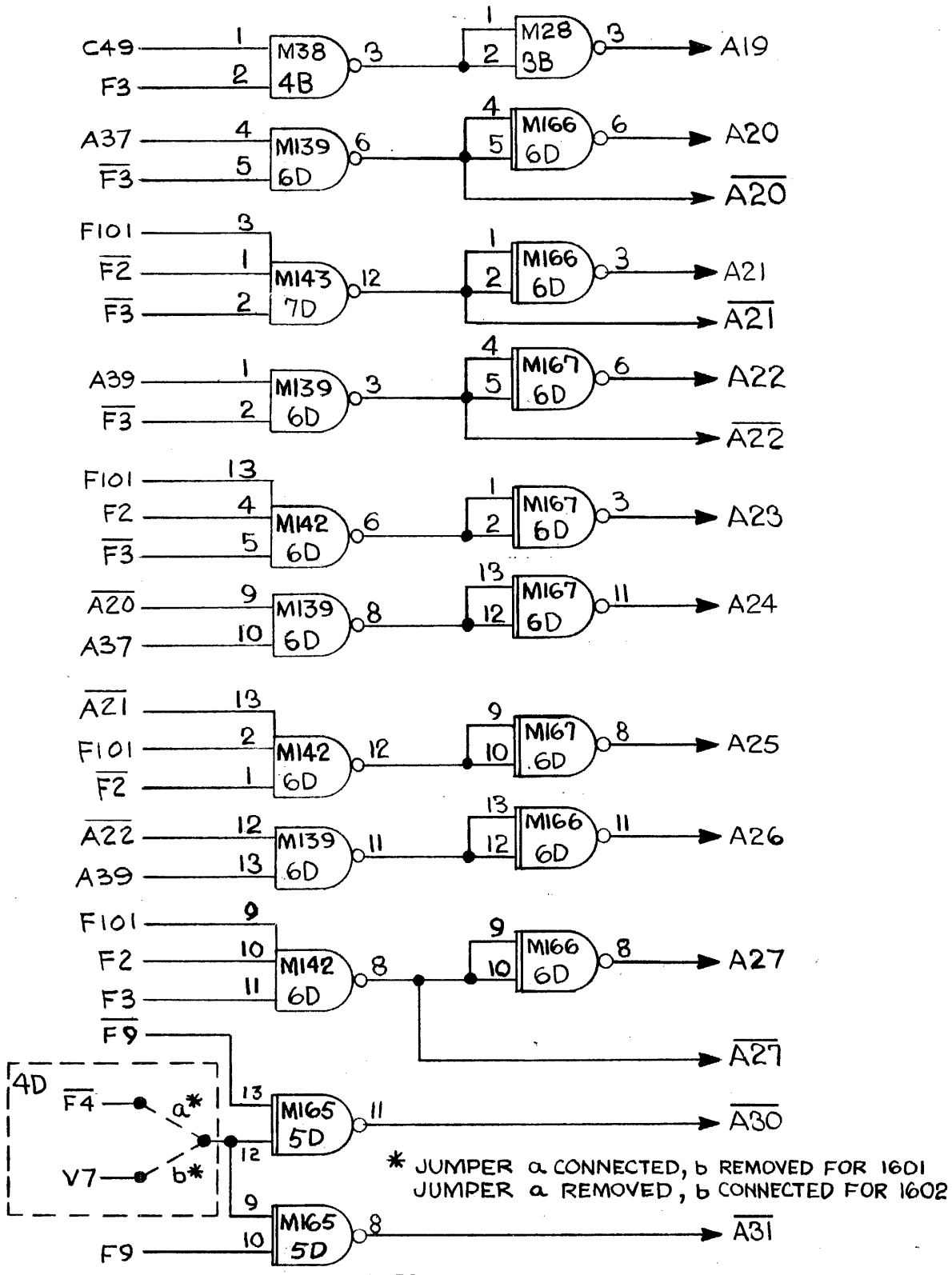


Figure 3.52 Logic Diagram.

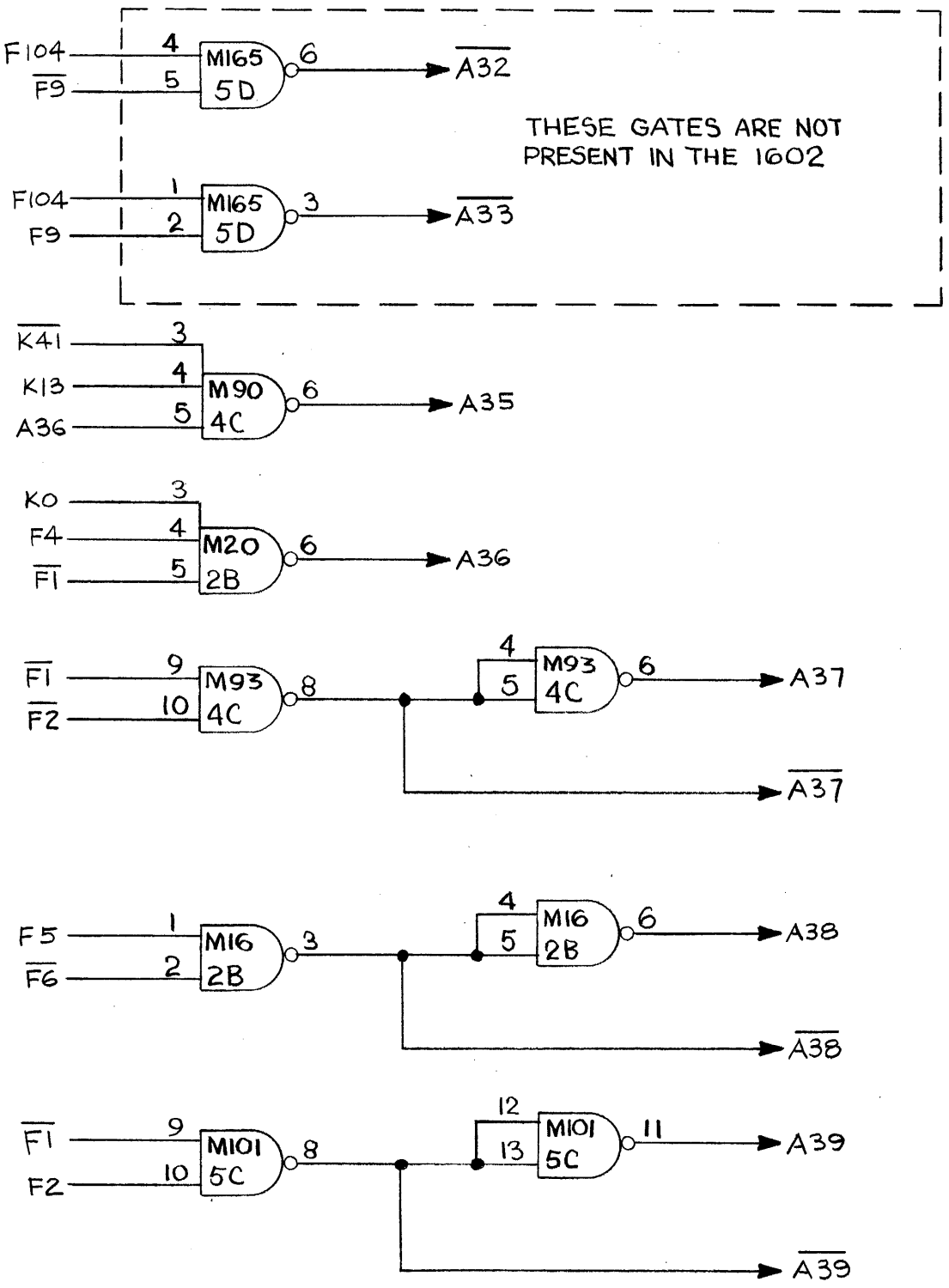


Figure 3.53 Logic Diagram.

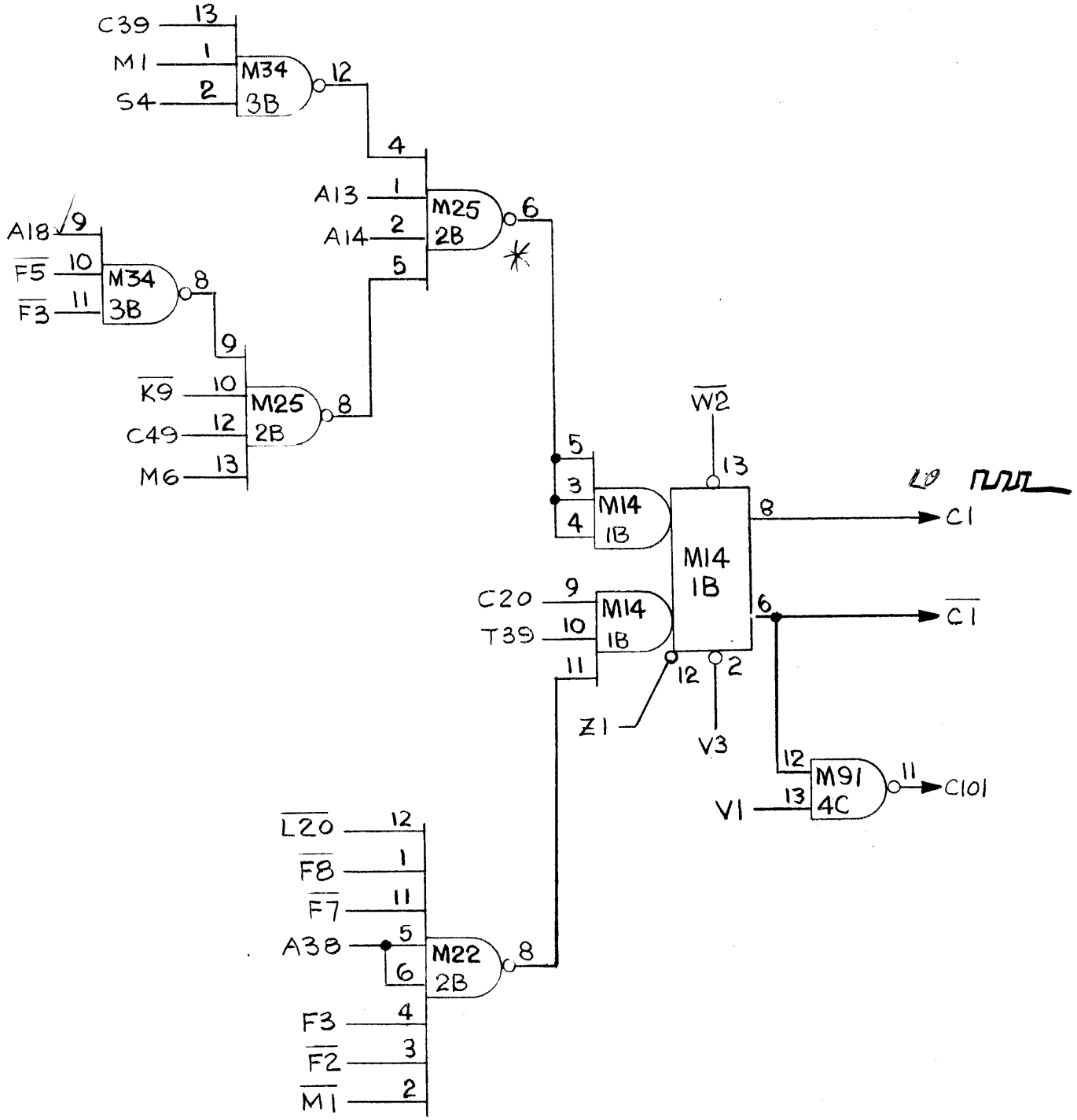


Figure 3.54 Logic Diagram.

HALT BLUE.
RUN

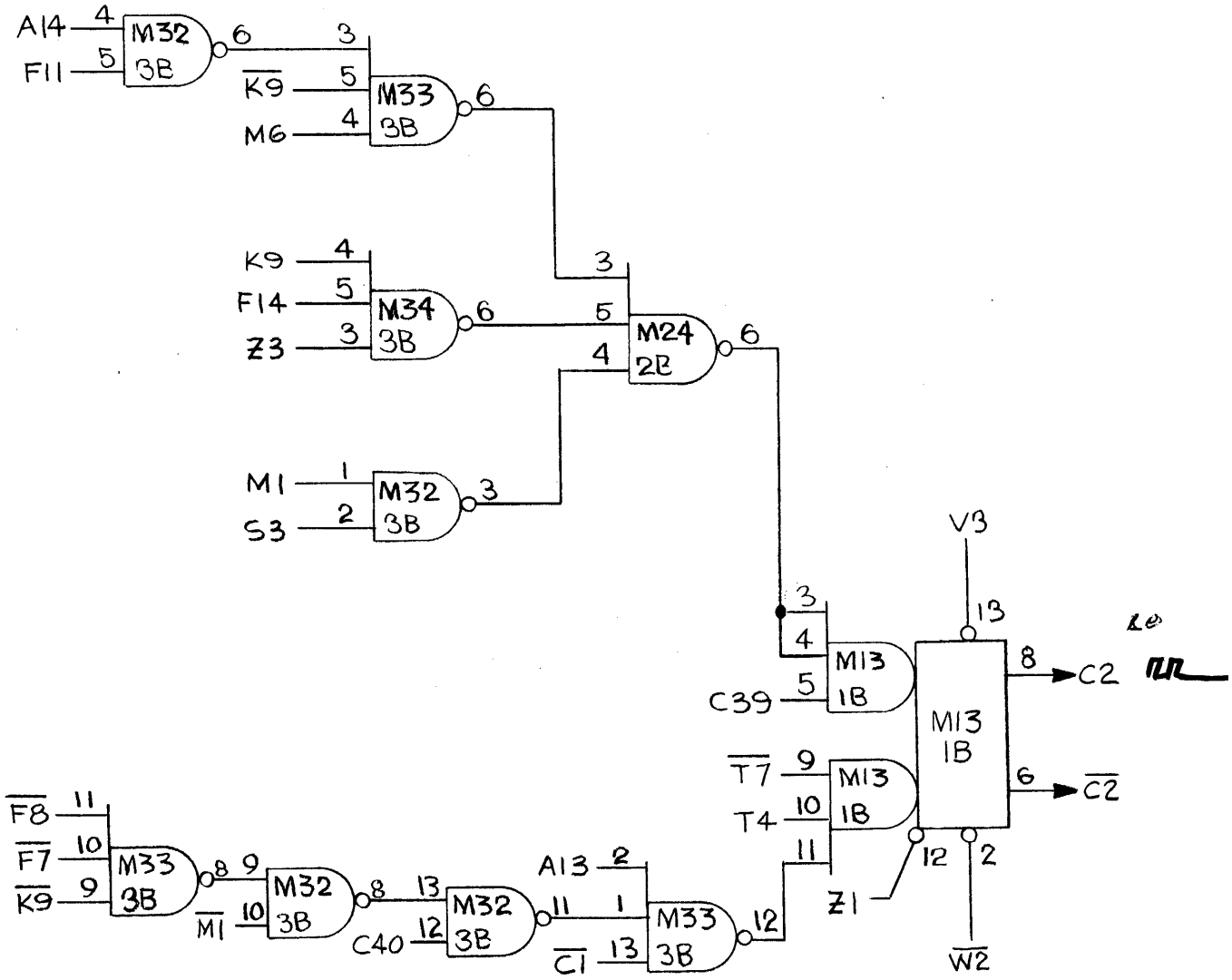


Figure 3.55 Logic Diagram.

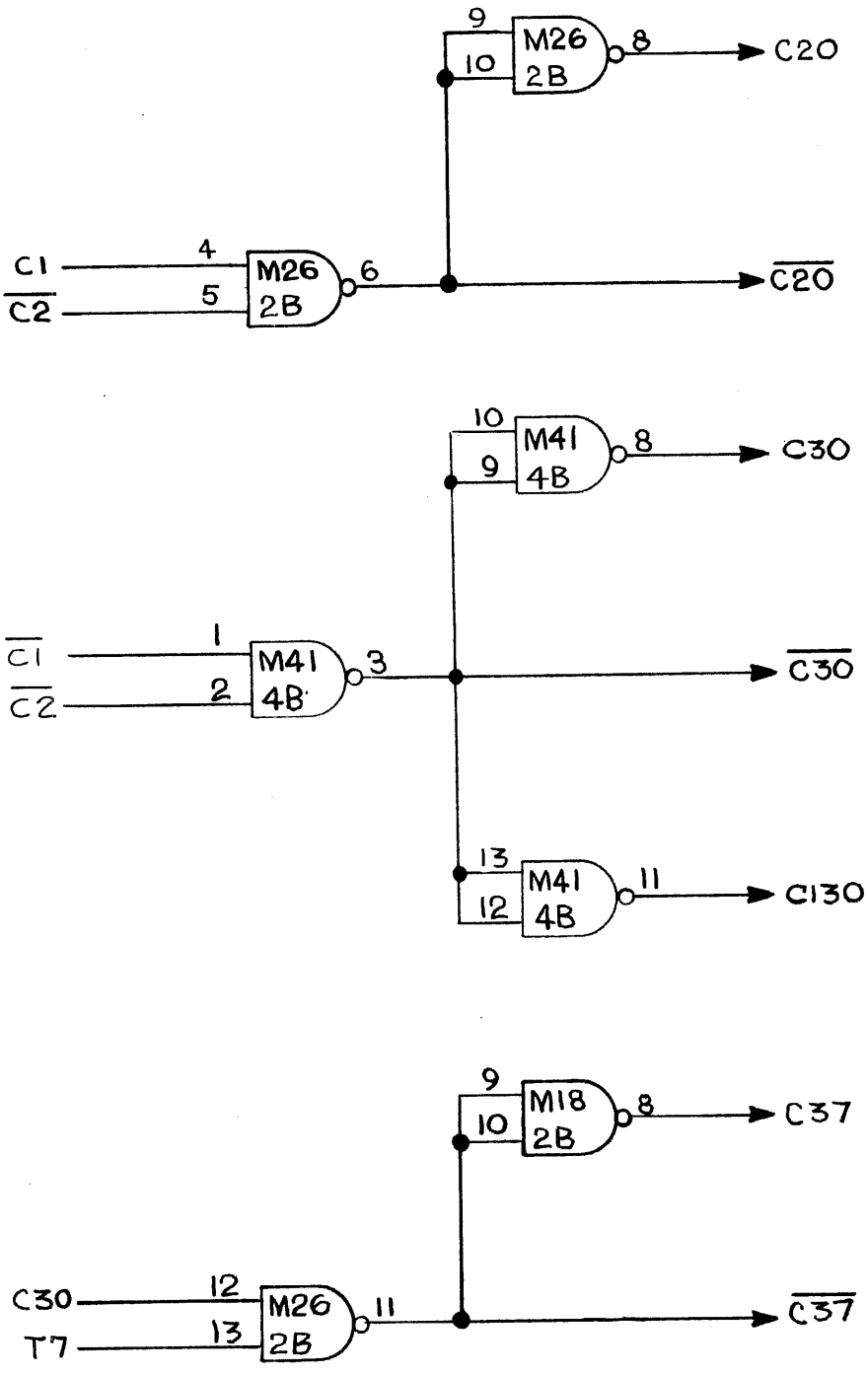


Figure 3.56 Logic Diagram.

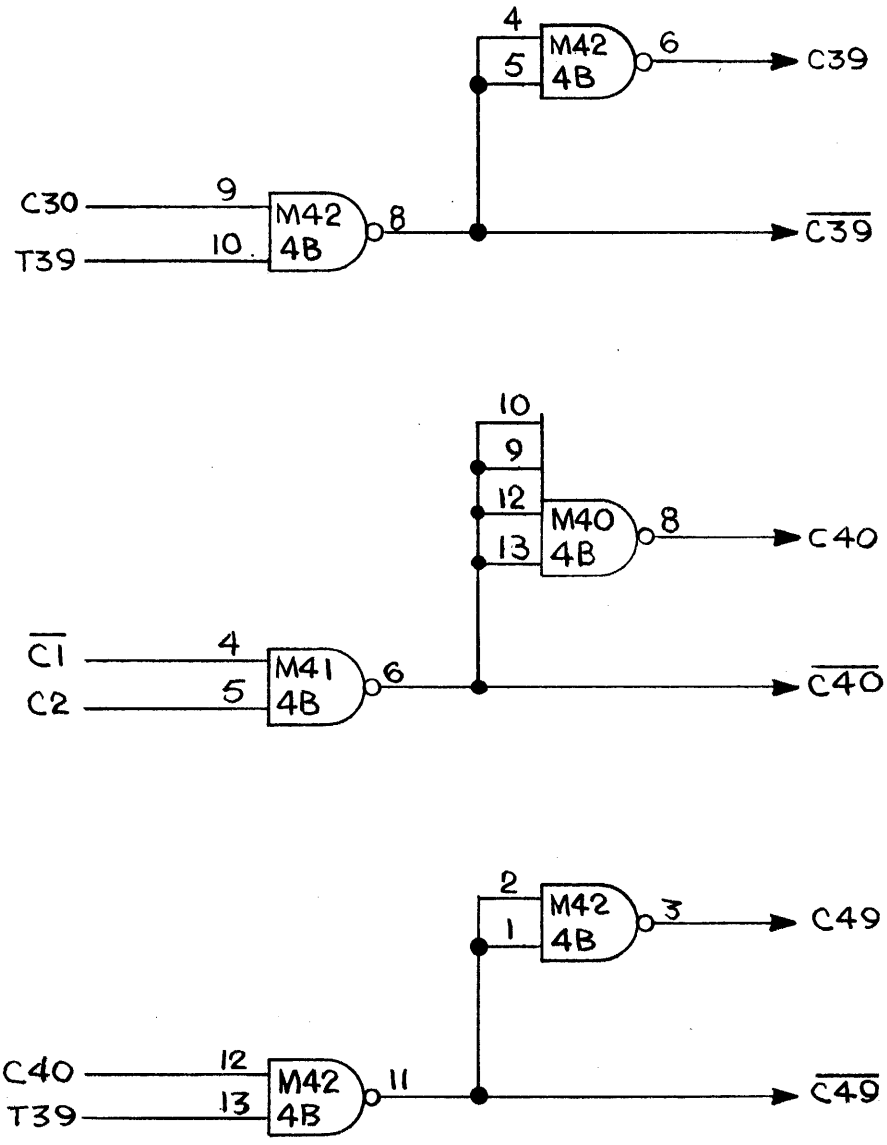
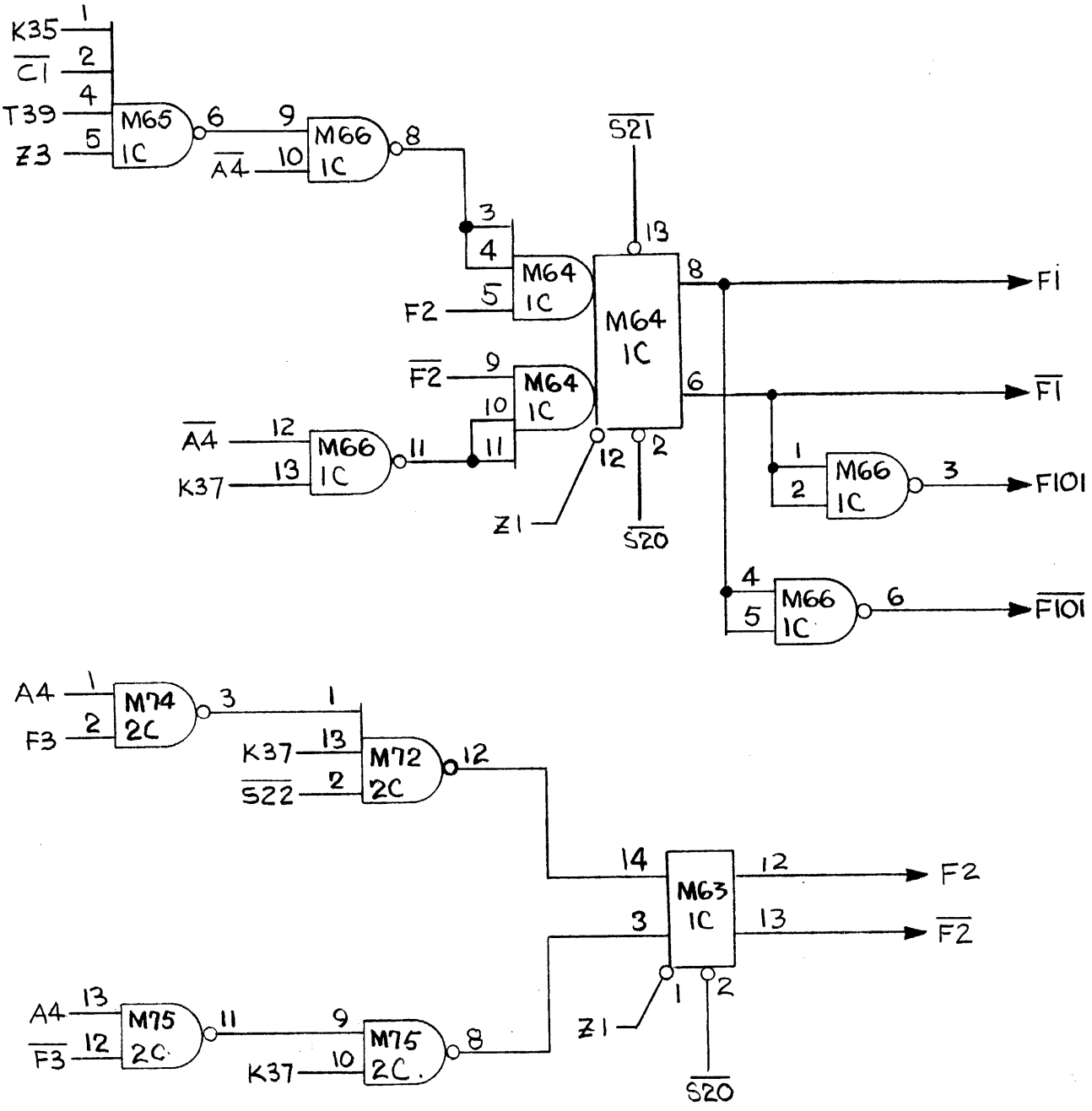


Figure 3.57 Logic Diagram.



PART OF COMMAND REGISTER

Figure 3.58 Logic Diagram.

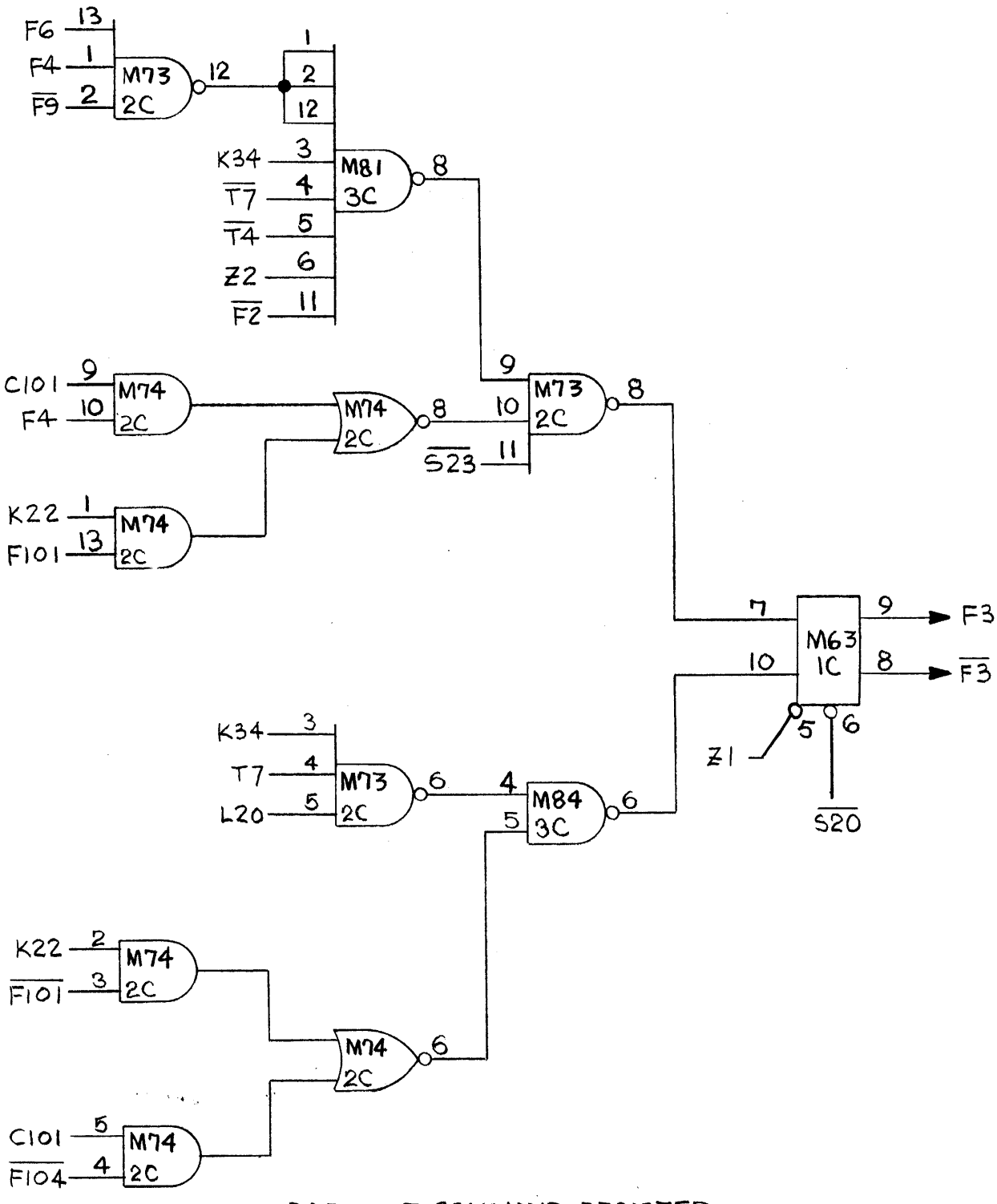
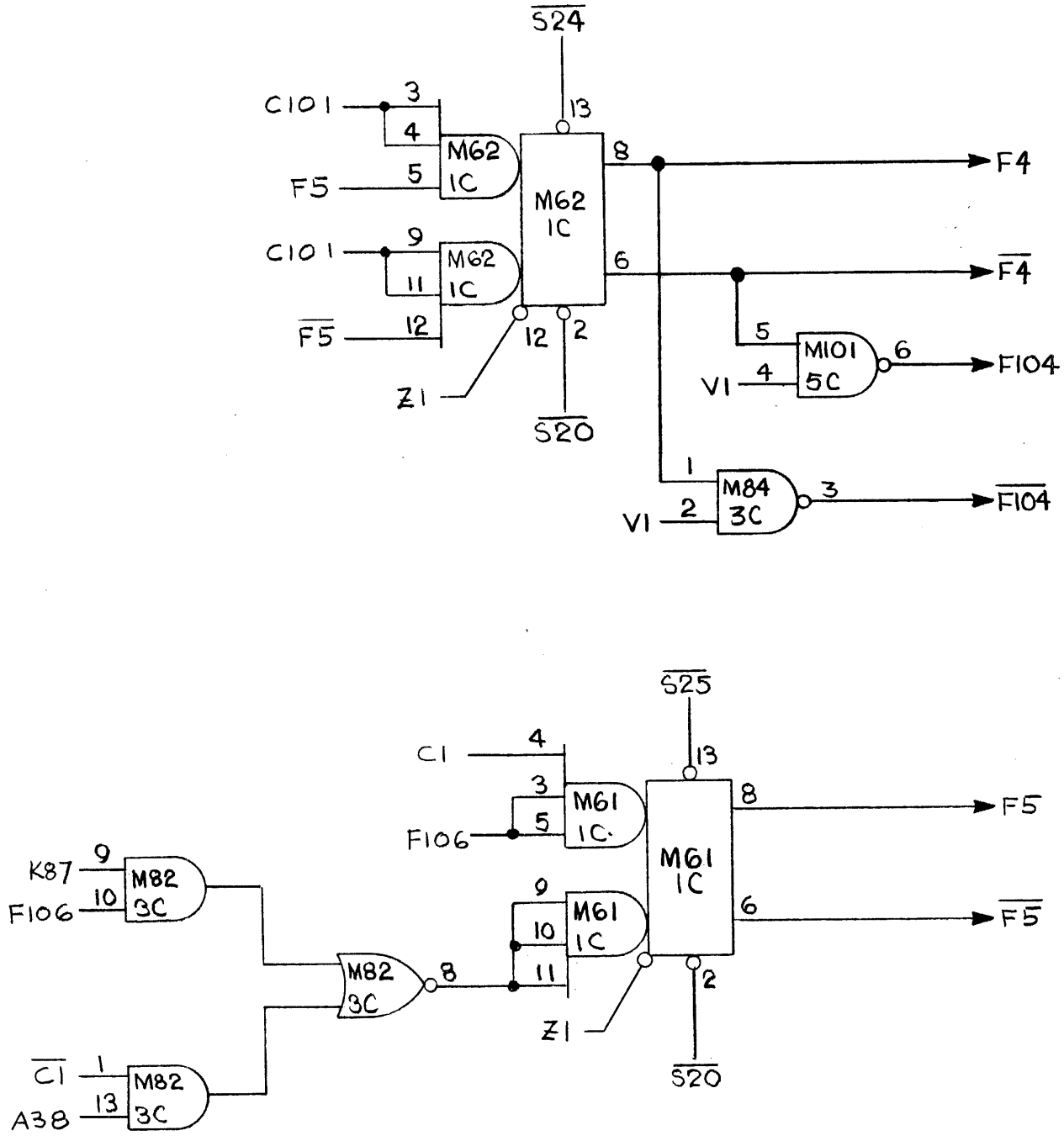
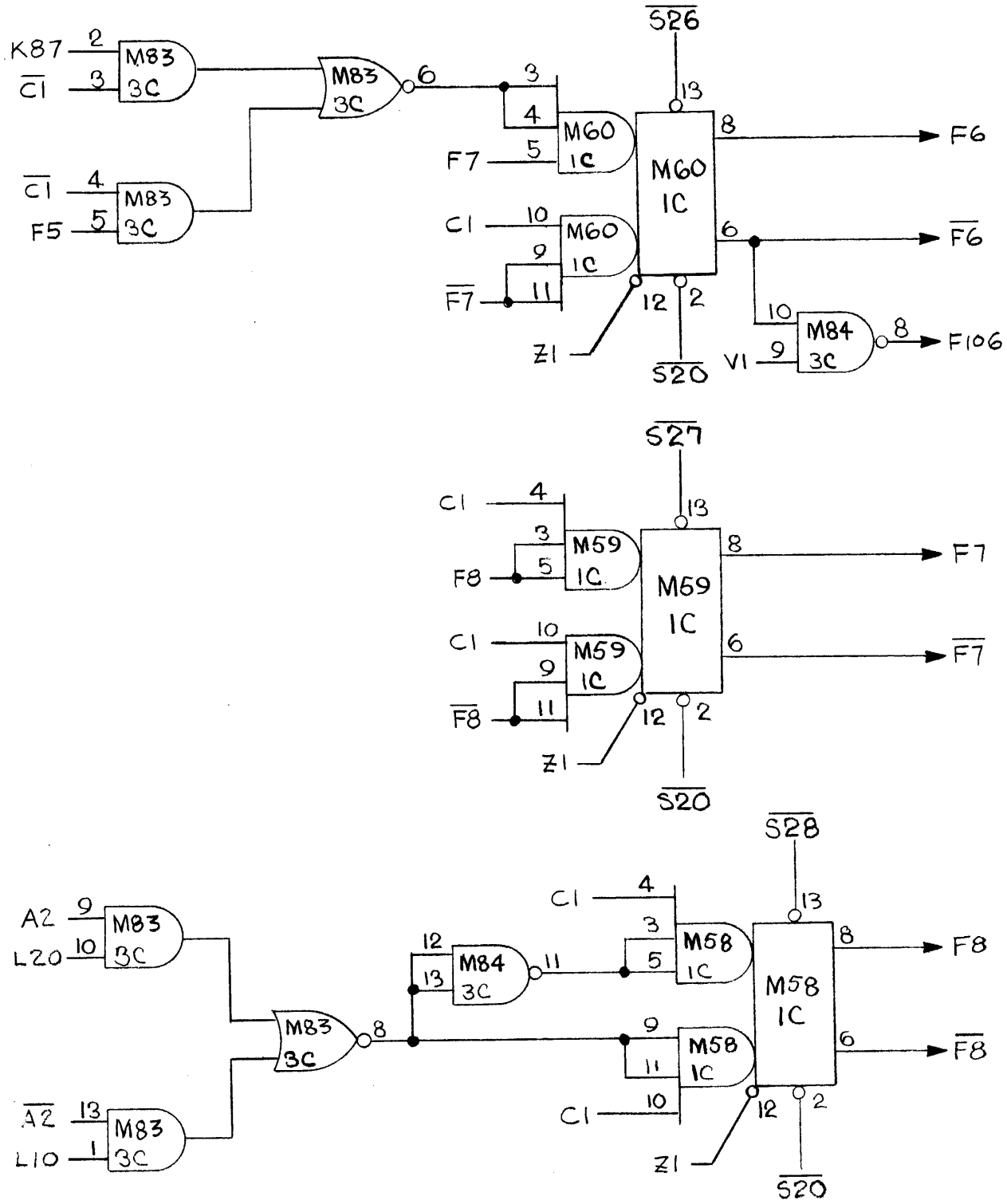


Figure 3.59 Logic Diagram.



PART OF COMMAND REGISTER

Figure 3.60 Logic Diagram.



PART OF COMMAND REGISTER

Figure 3.61 Logic Diagram.

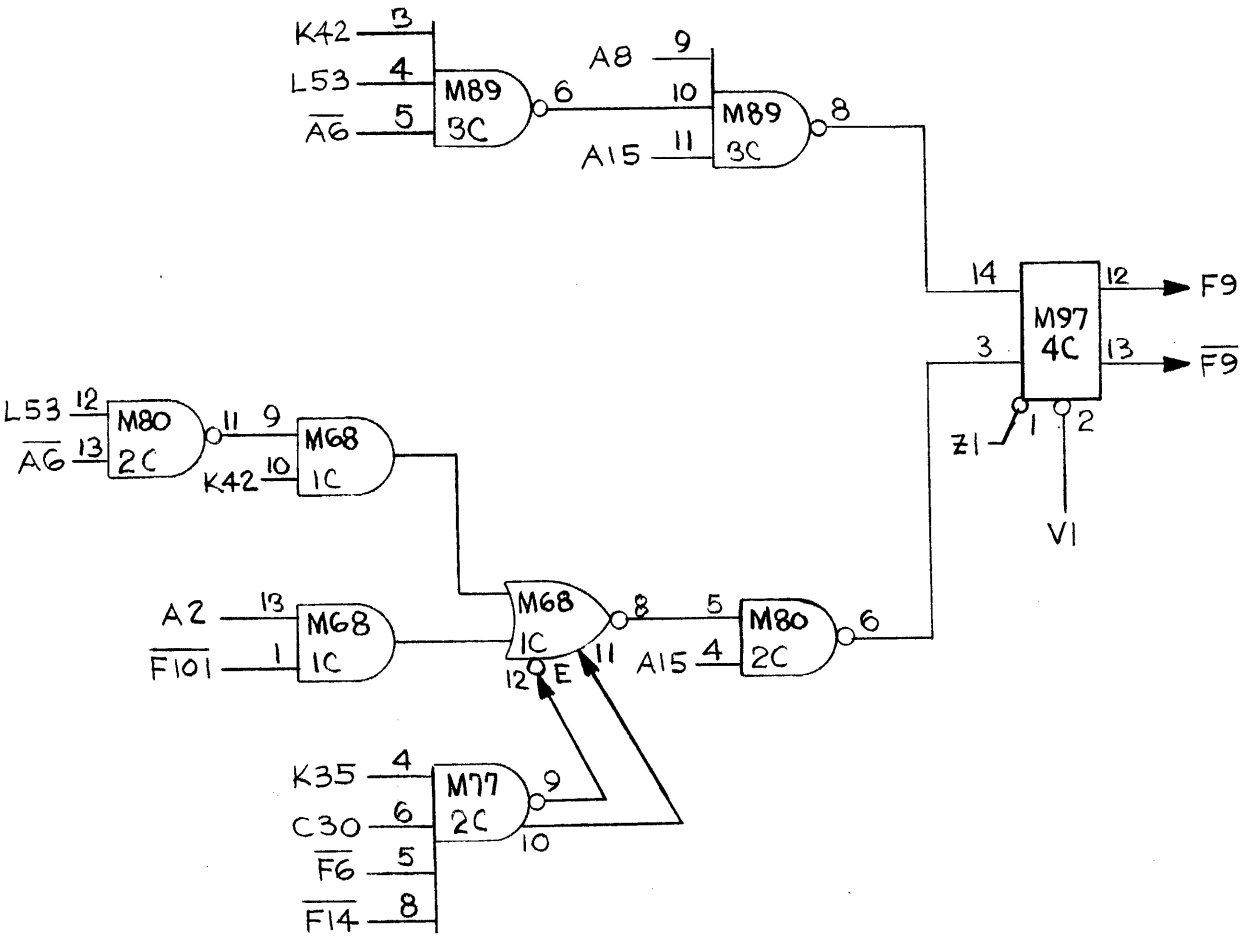


Figure 3.62 Logic Diagram.

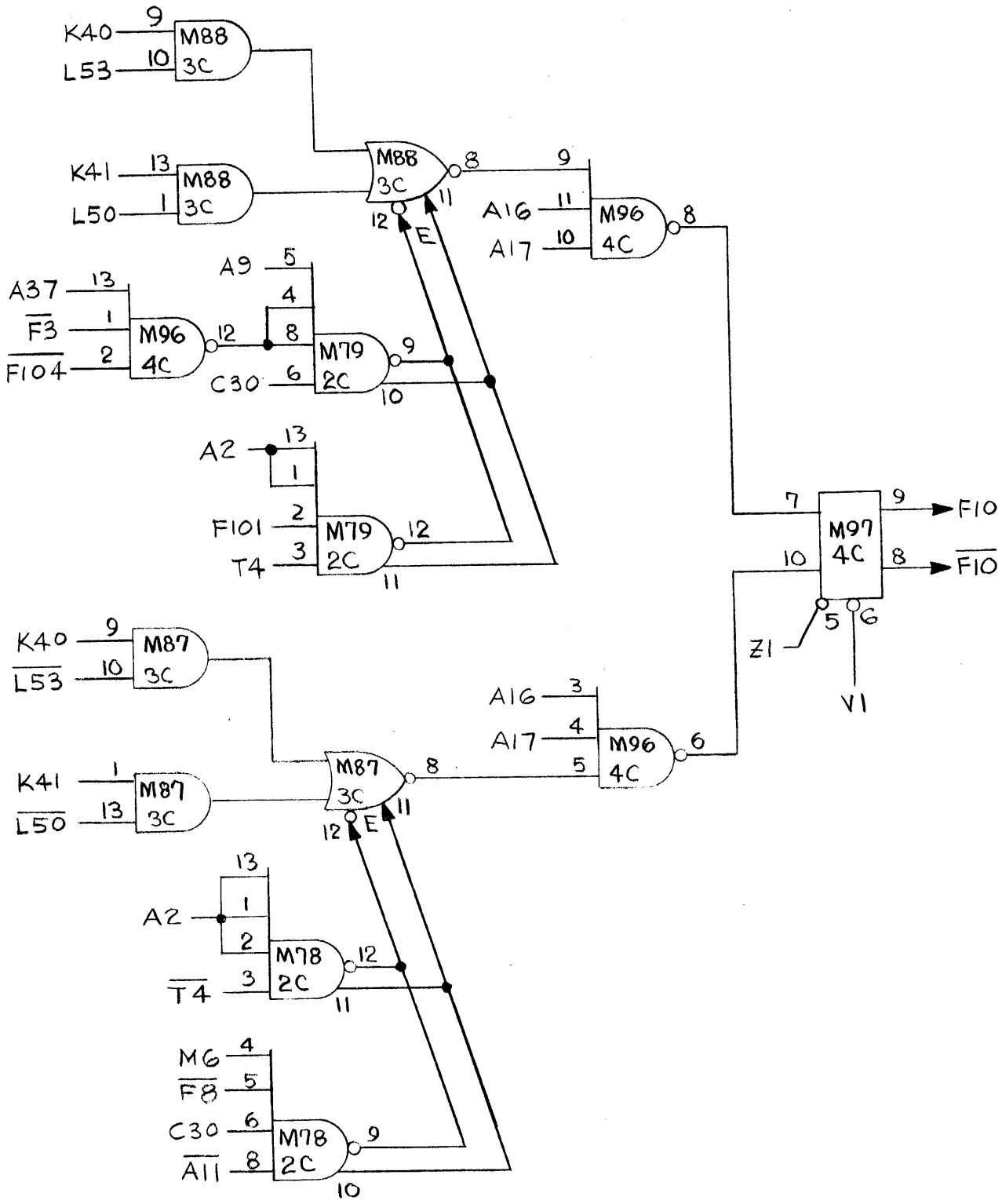
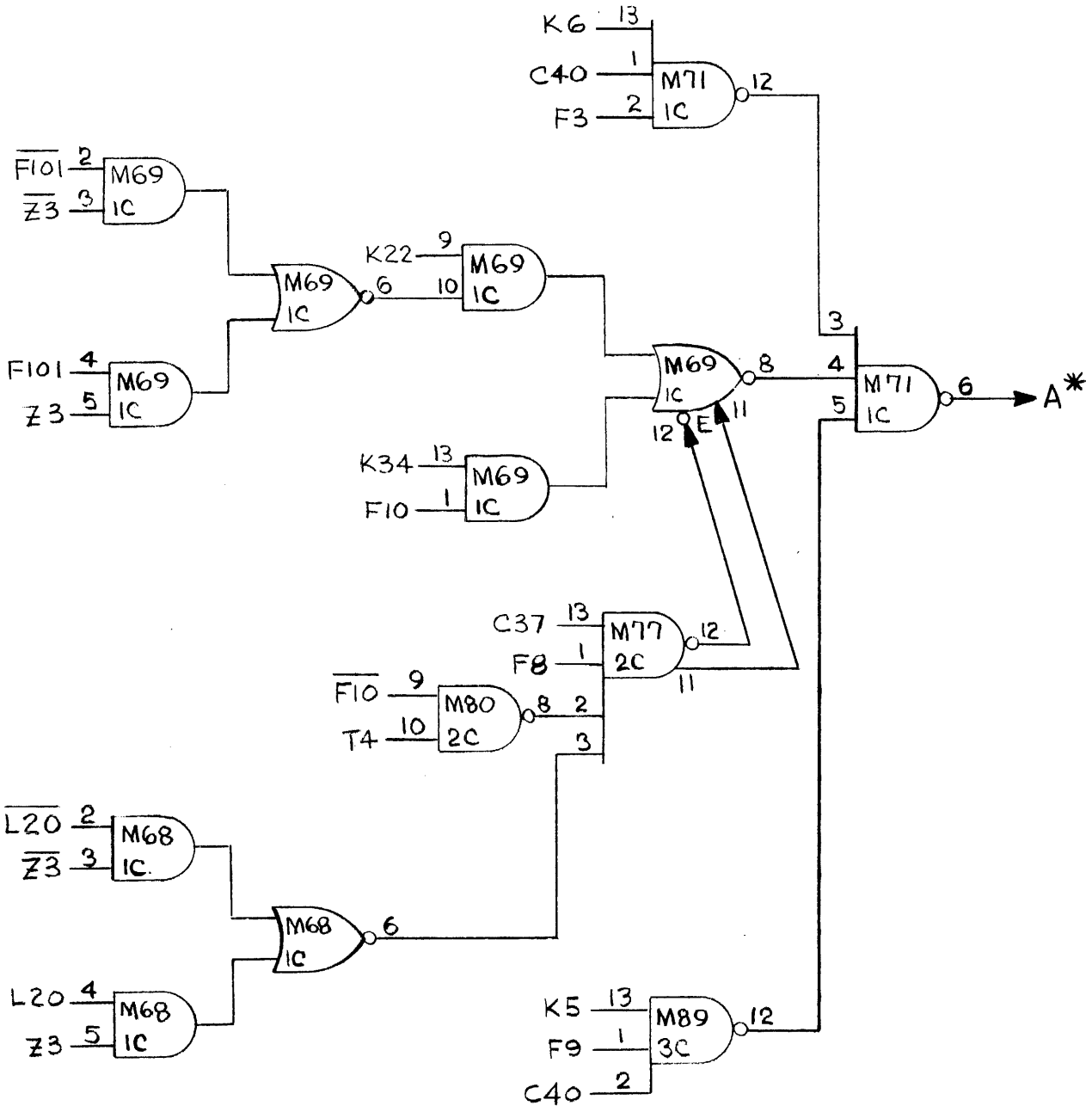
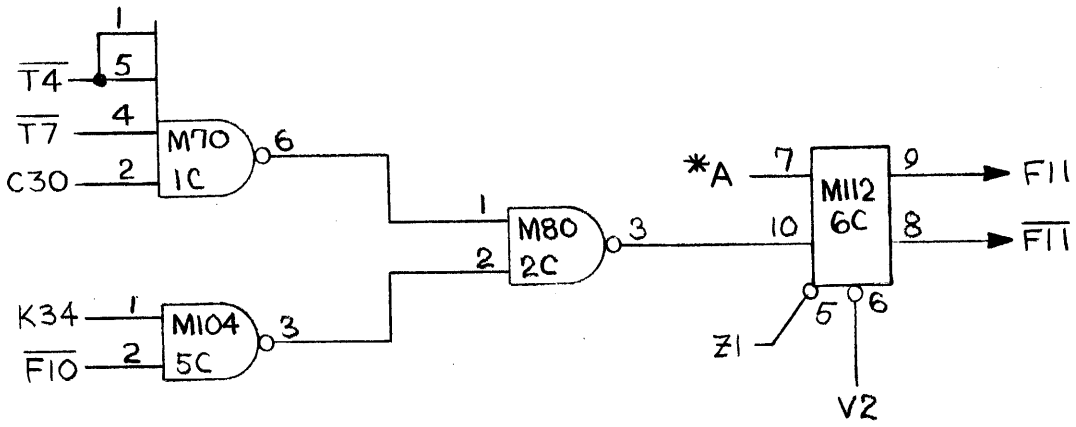


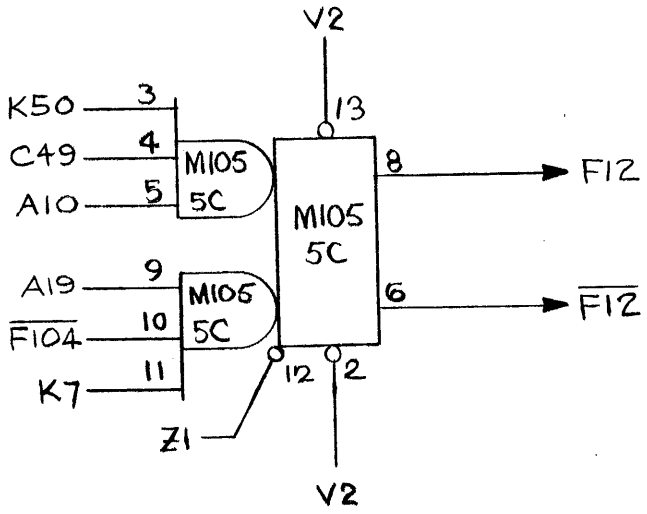
Figure 3.63 Logic Diagram.



* A TO FIGURE 3.65, M112-7

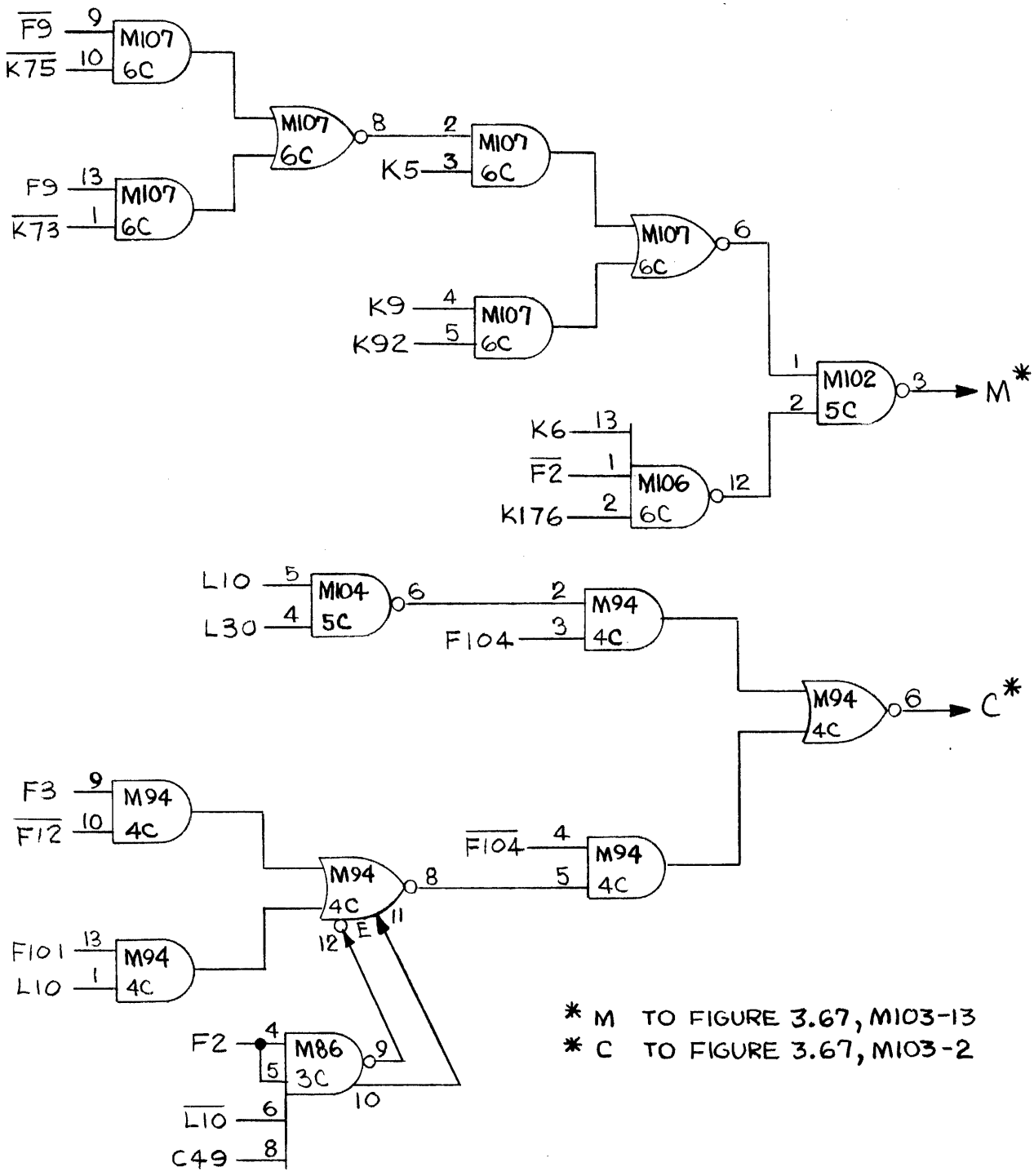
Figure 3.64 Logic Diagram.





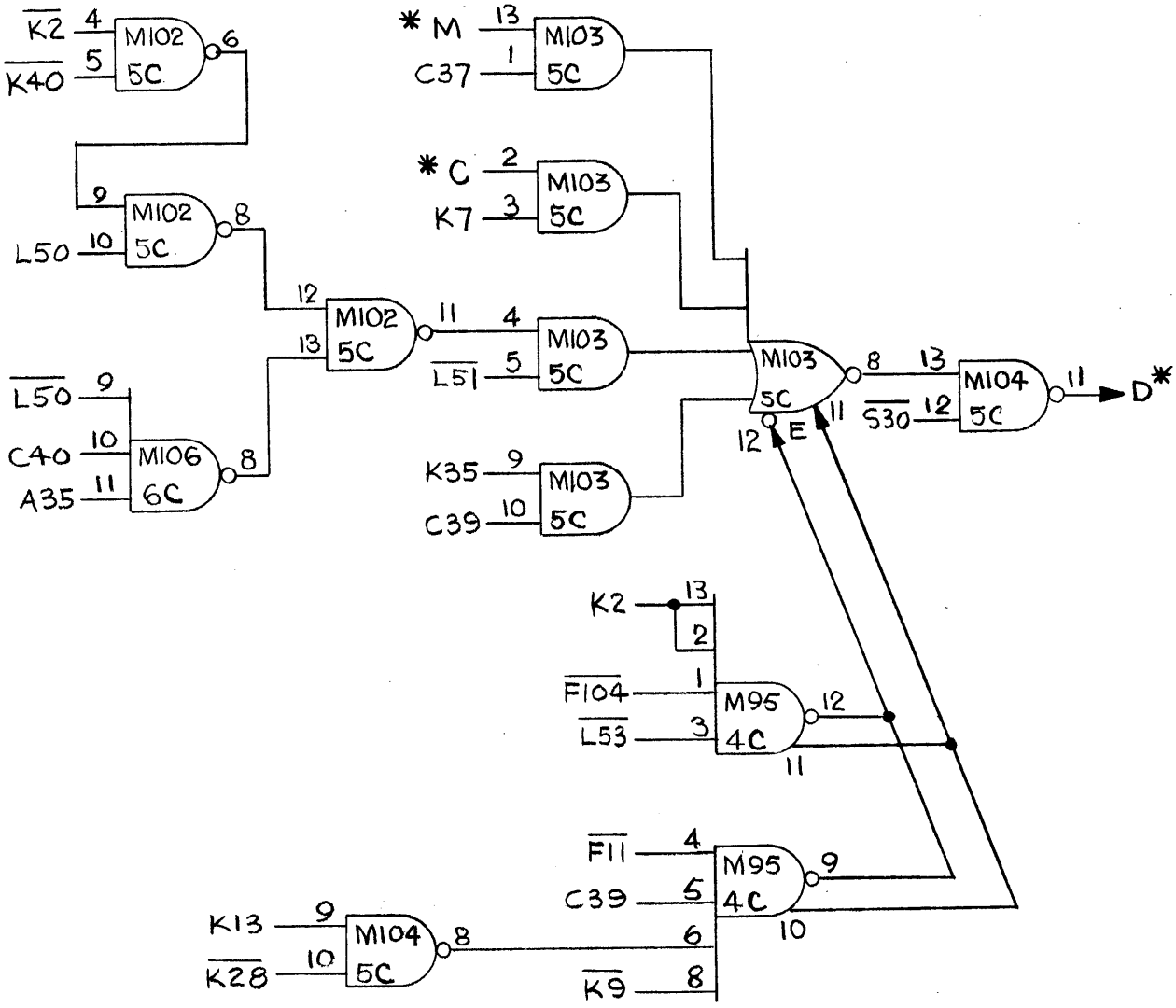
*A FROM FIGURE 3.64, M71-6

Figure 3.65 Logic Diagram.



PART OF F14 RESET NET

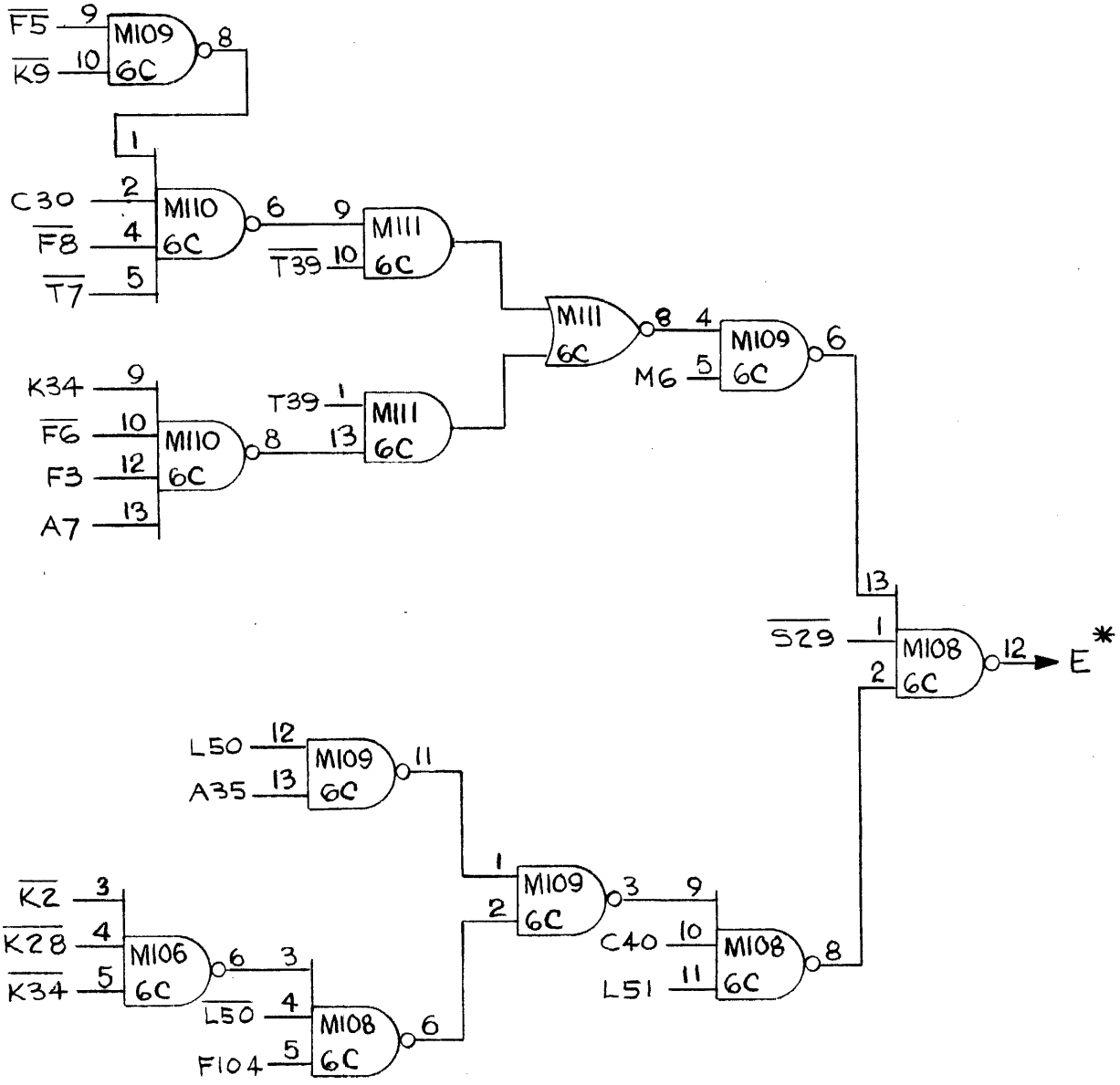
Figure 3.66 Logic Diagram.



* M FROM FIGURE 3.66, M102-3
* C FROM FIGURE 3.66, M94-6
* D TO FIGURE 3.69 M112-14

PART OF F14 RESET NET

Figure 3.67 Logic Diagram.

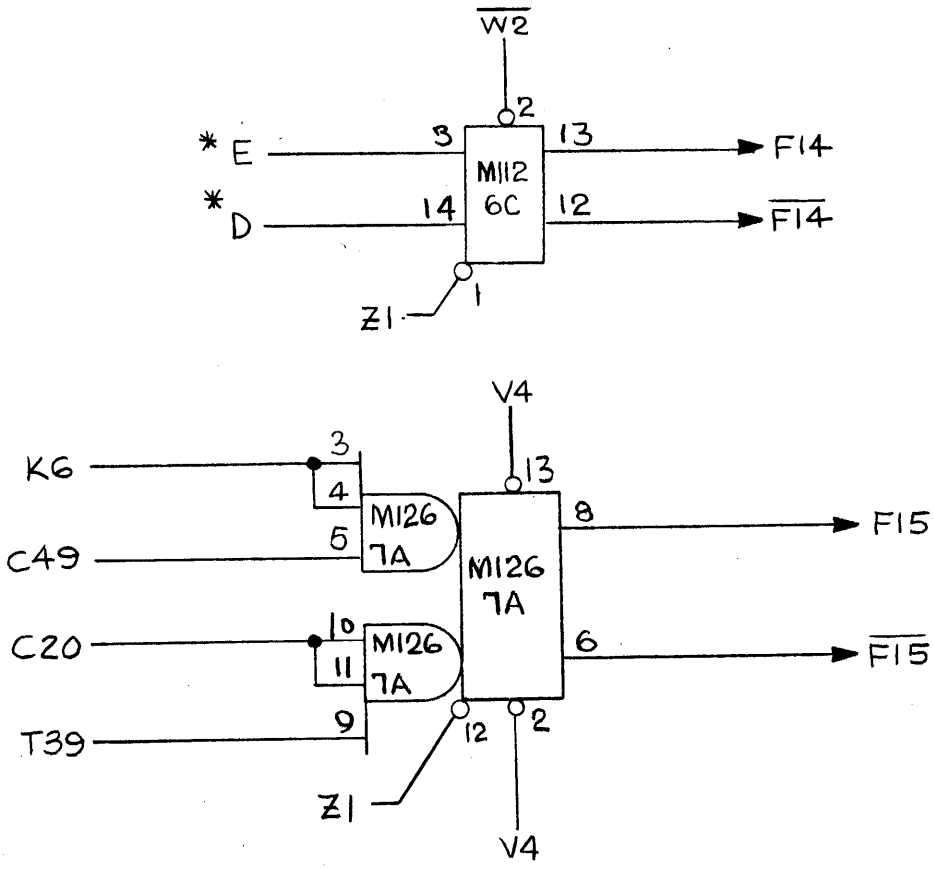


* E TO FIGURE 3.69, M112-3

F14 SET NET

Figure 3.68 Logic Diagram.

HALT



*D FROM FIGURE 3.67, M104-11
*E FROM FIGURE 3.68, M108-12

Figure 3.69 Logic Diagram.

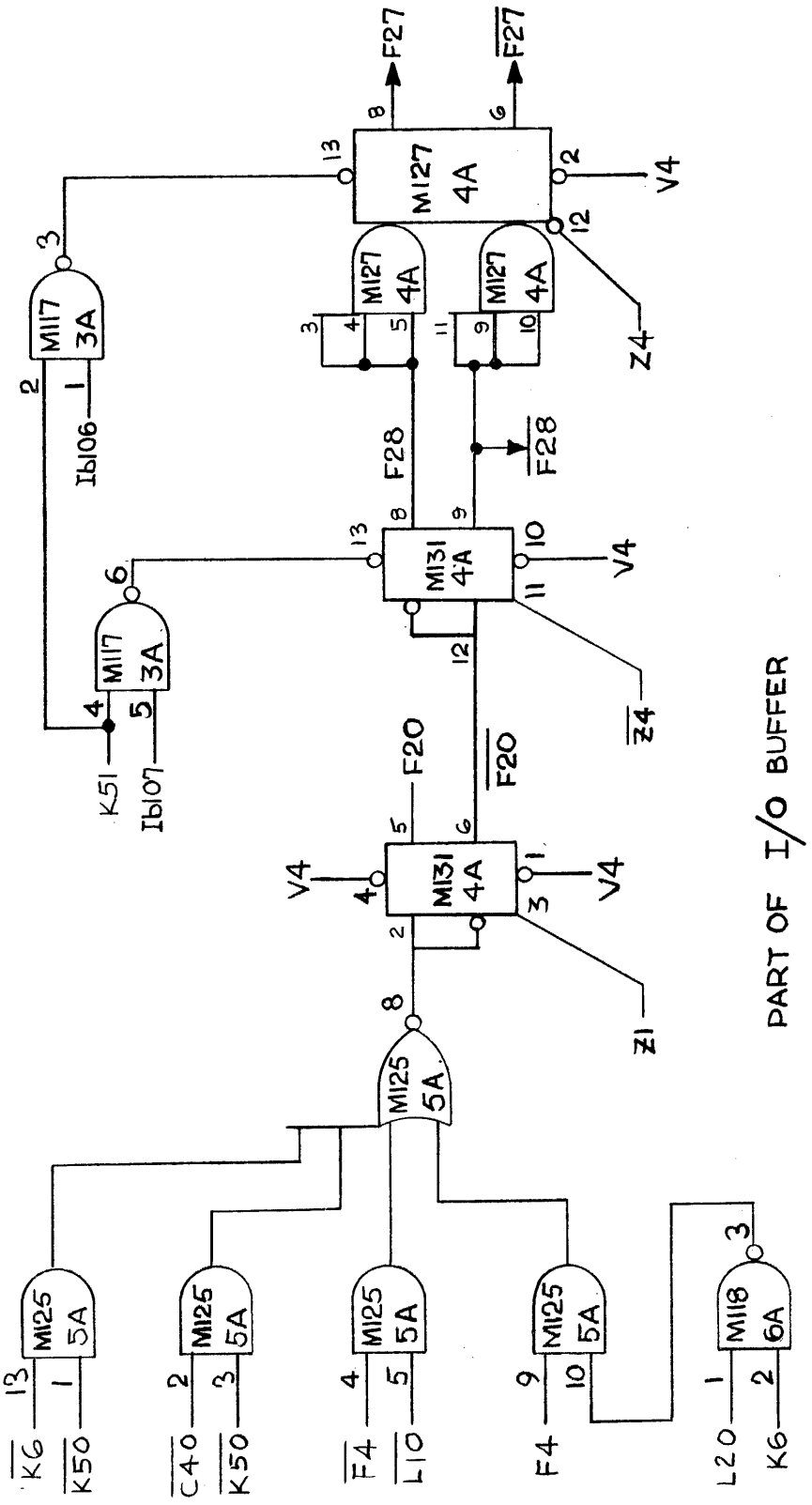


Figure 3.70 Logic Diagram.

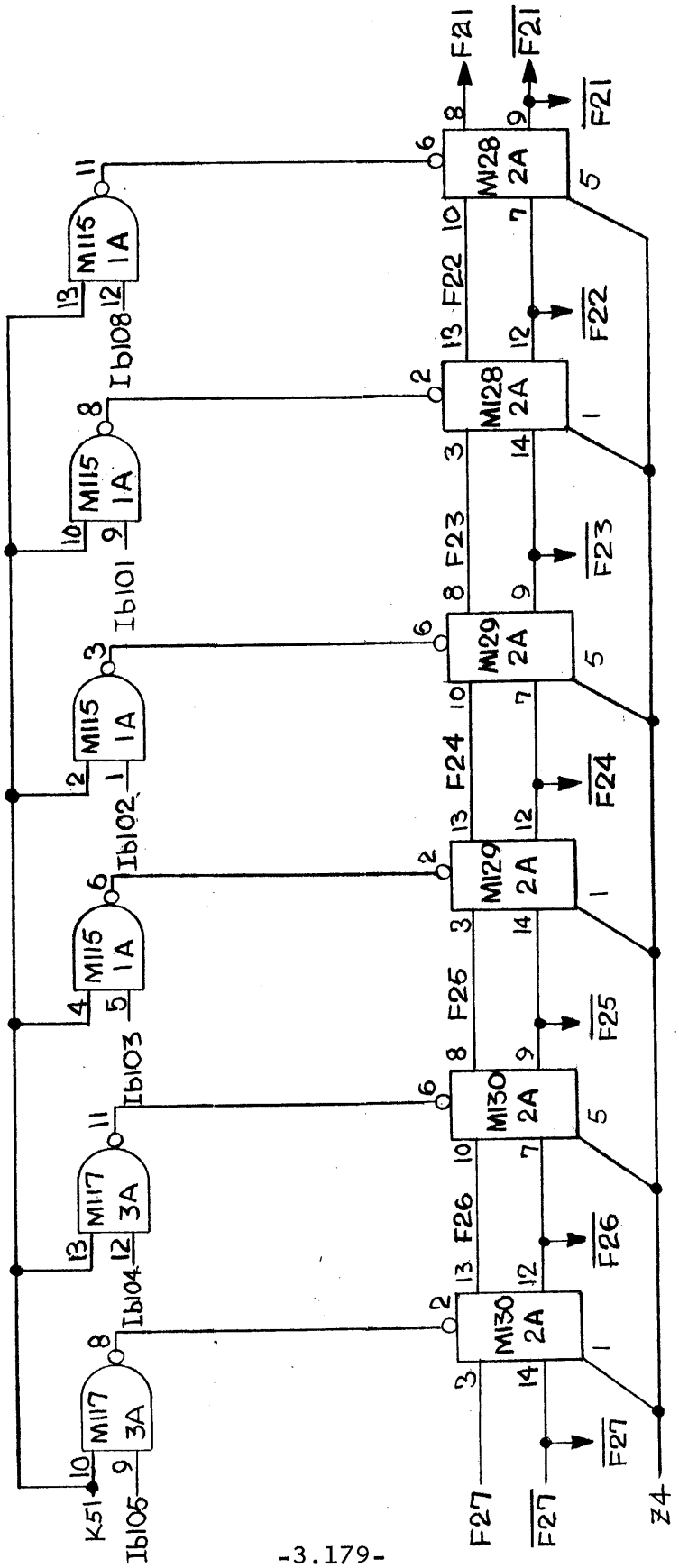


Figure 3.71 Logic Diagram.

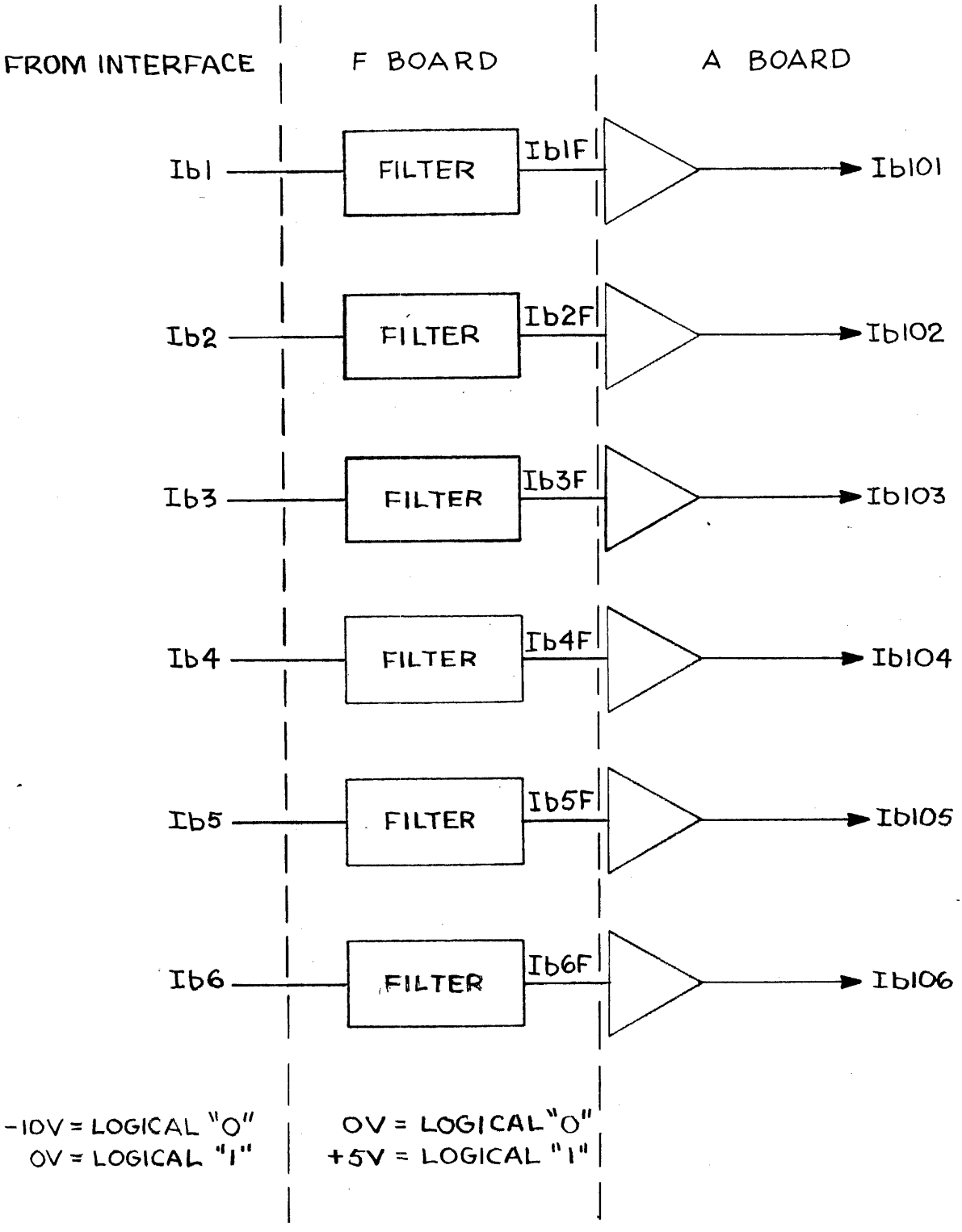


Figure 3.72 Logic Diagram.

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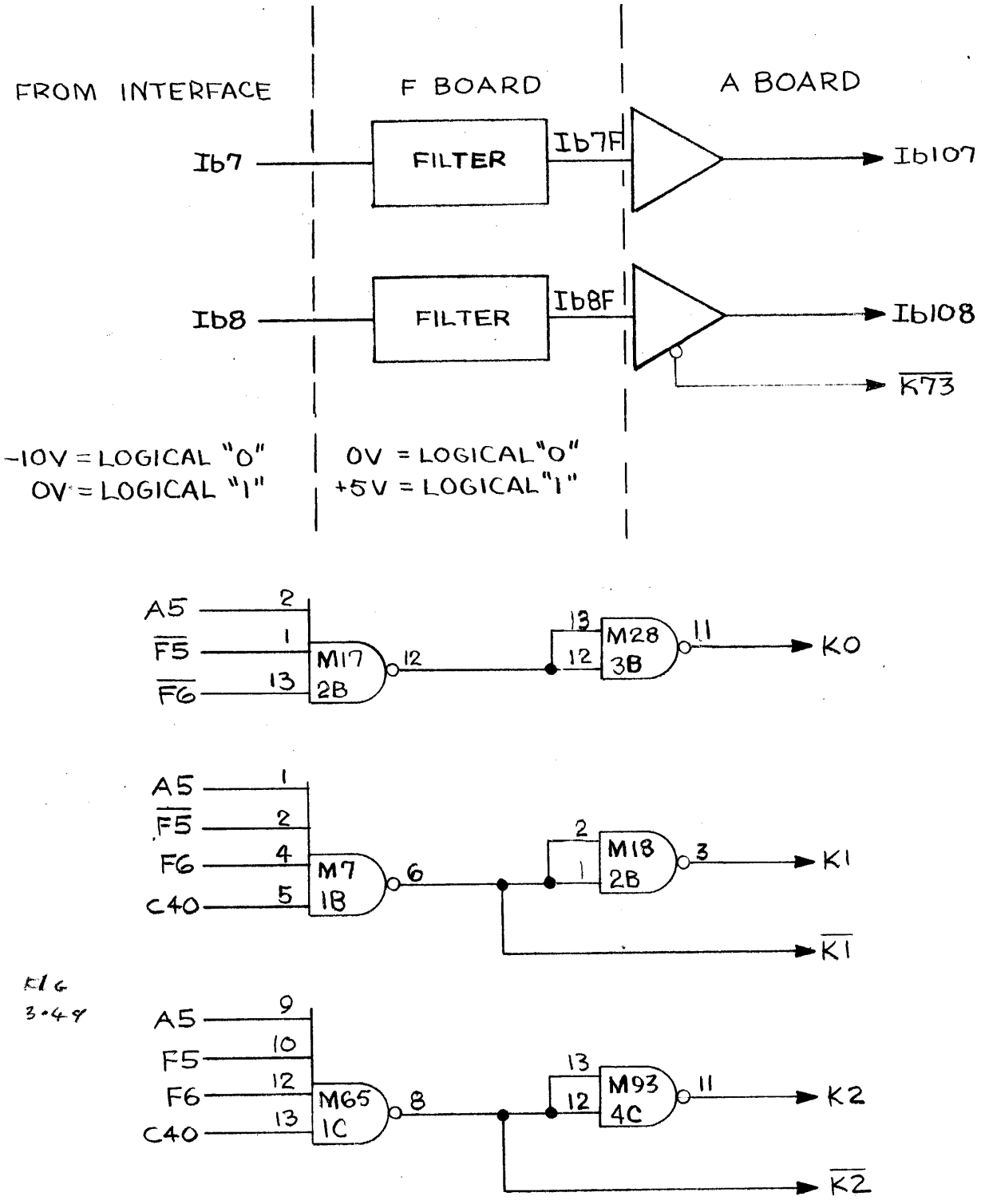
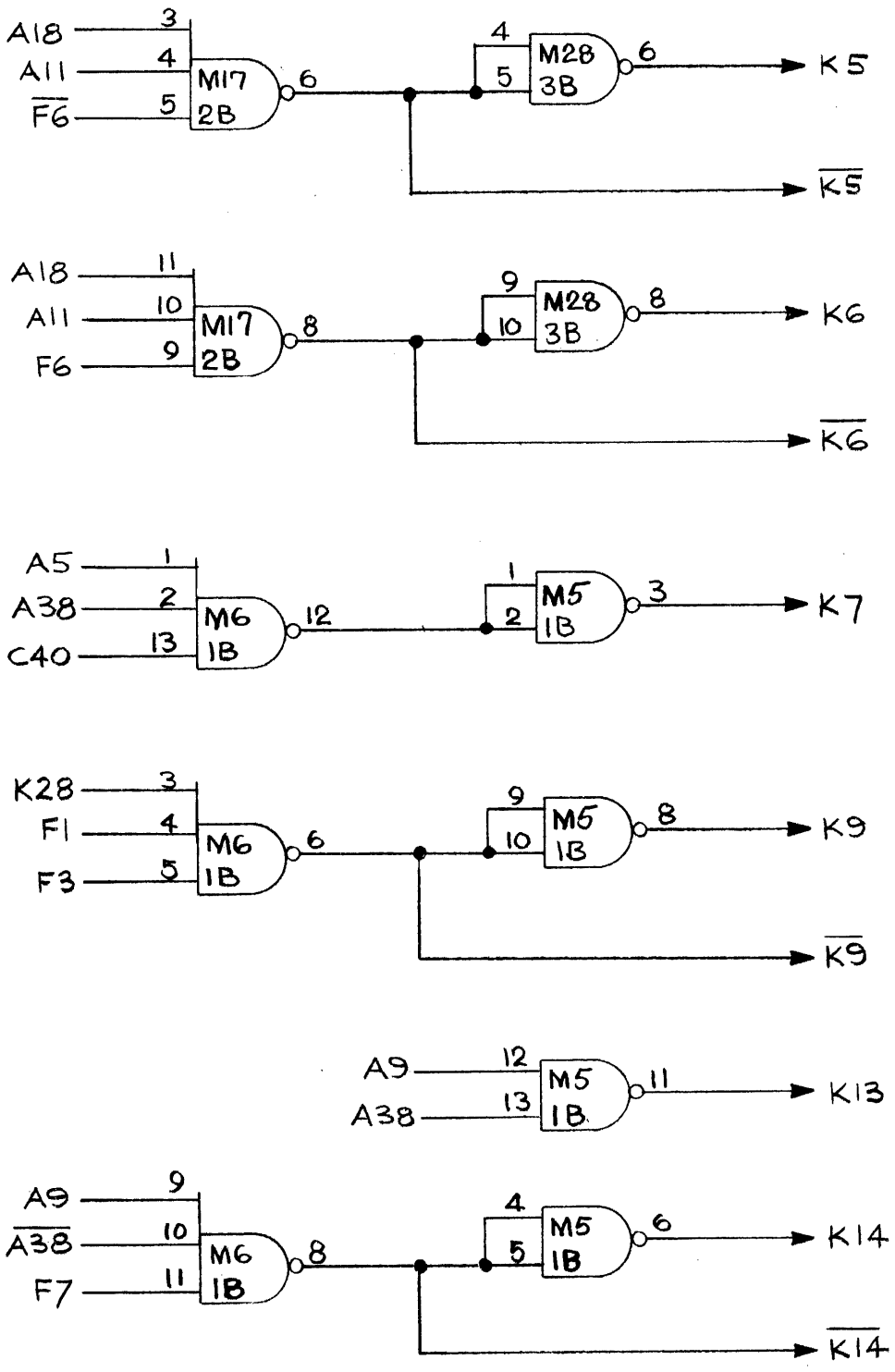


FIG 3-49

Figure 3.73 Logic Diagram.

Rev. 1MAY69



Rev.18NOV68

Figure 3.74 Logic Diagram.

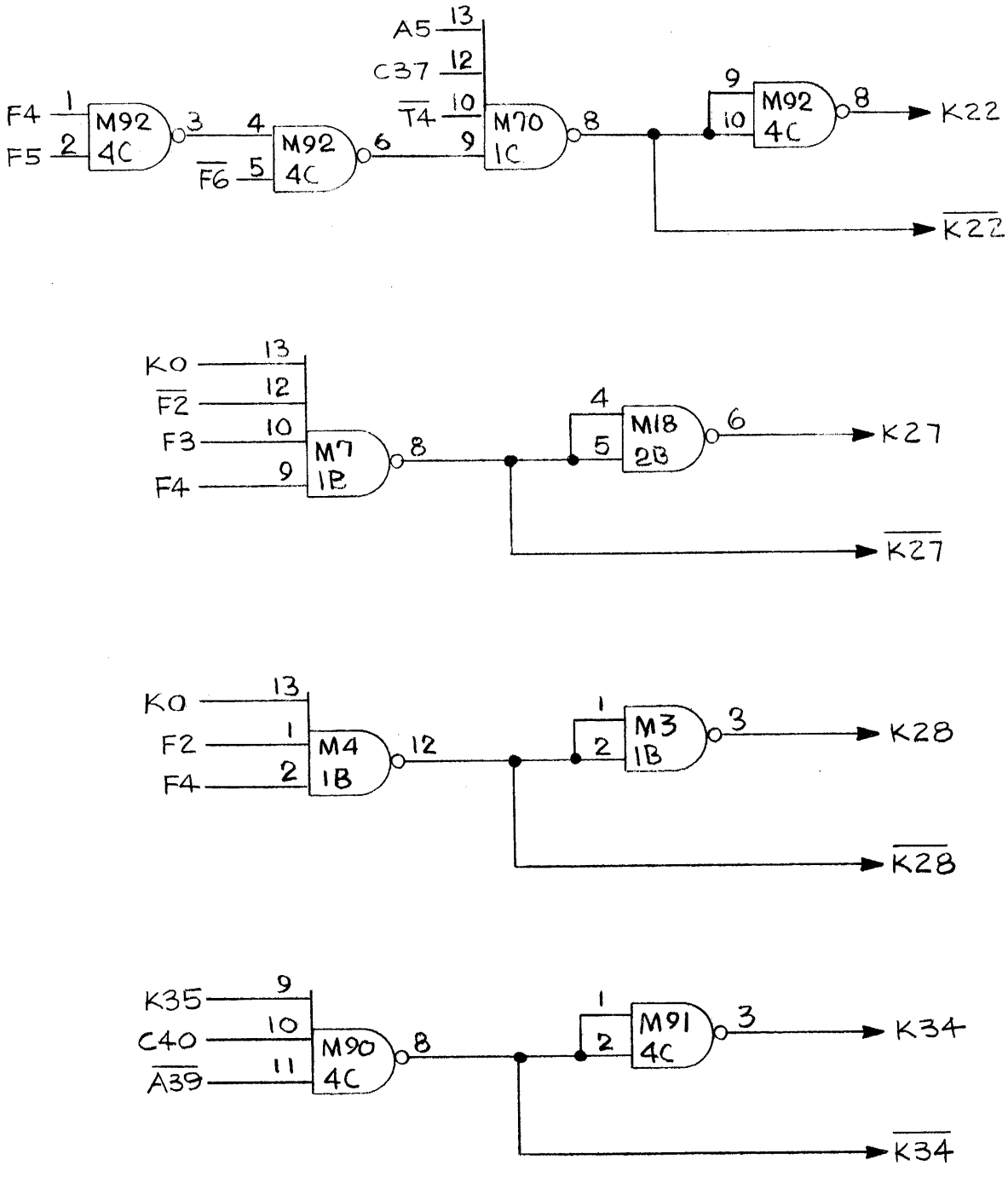


Figure 3.75 Logic Diagram.

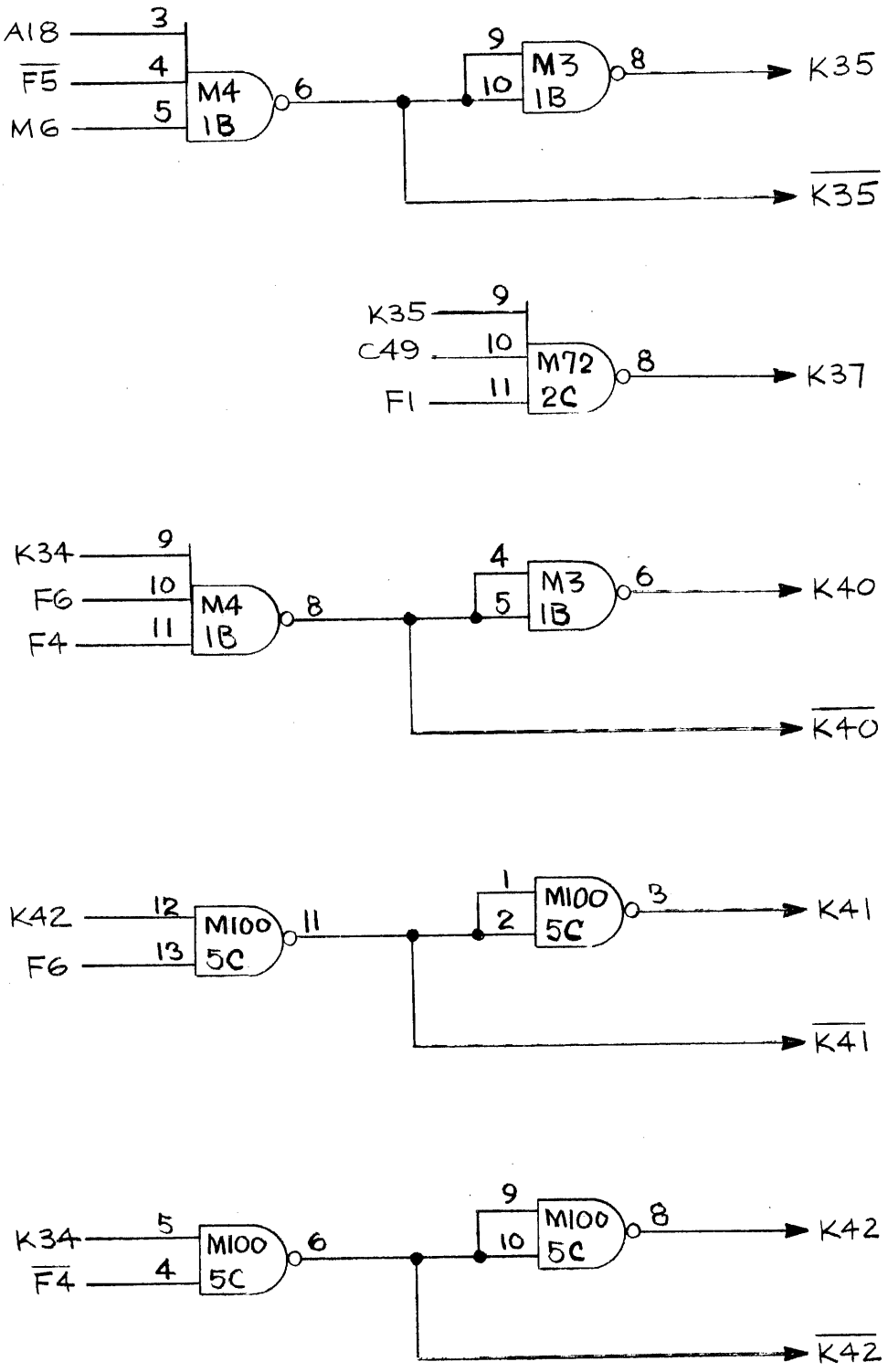


Figure 3.76 Logic Diagram.

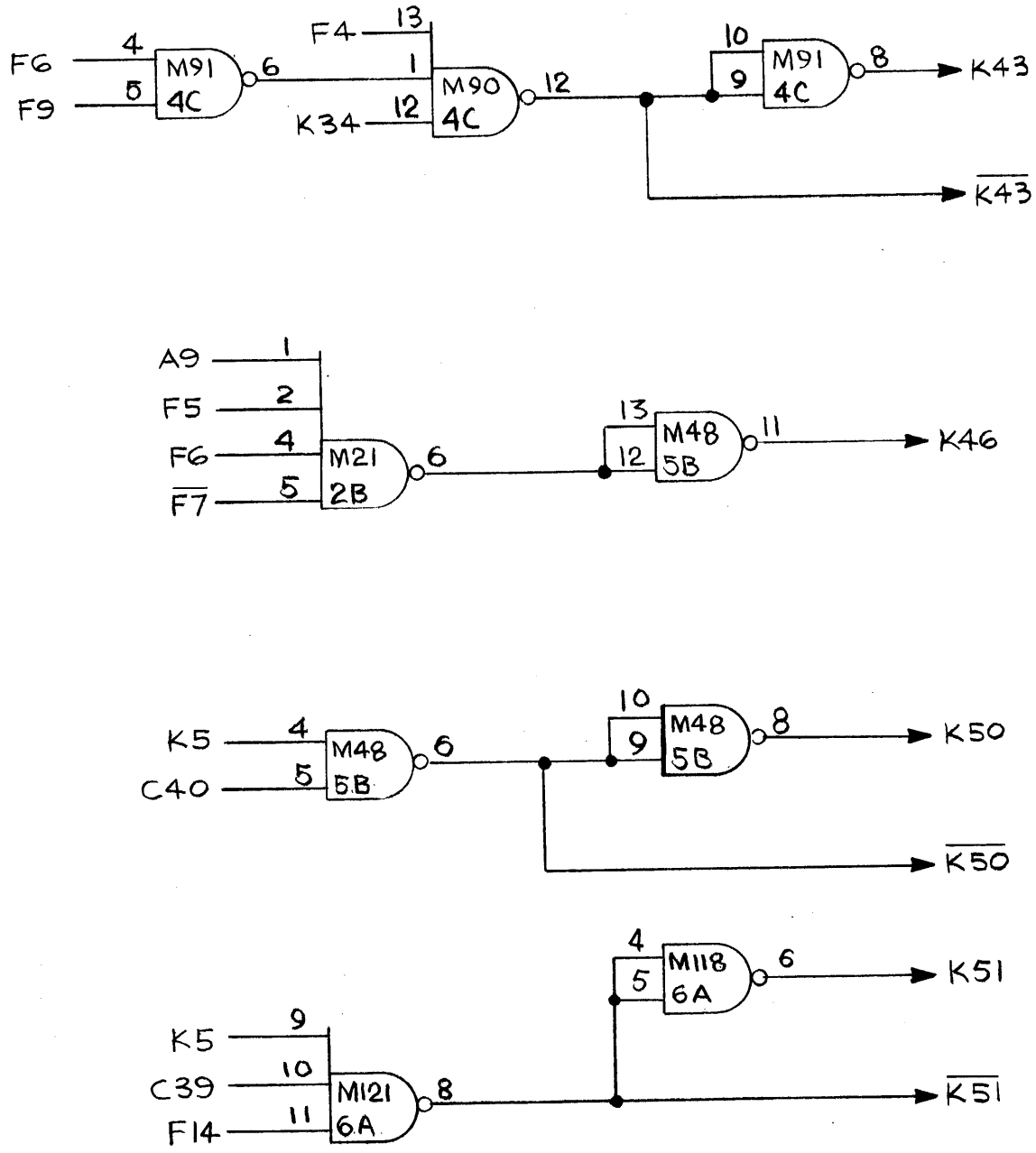


Figure 3.77 Logic Diagram. Rev.18NOV68

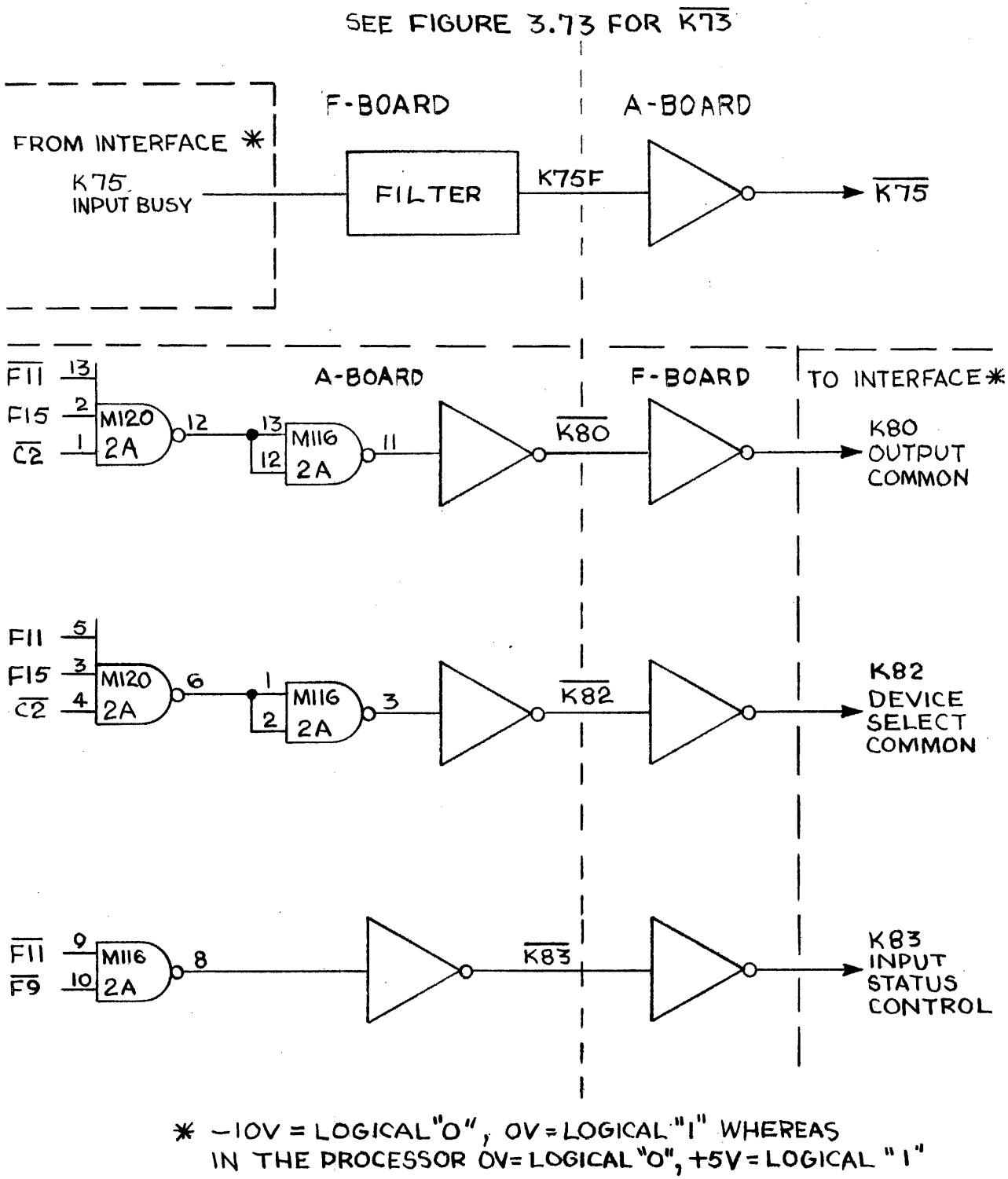


Figure 3.78 Logic Diagram.

Rev. 1MAY69

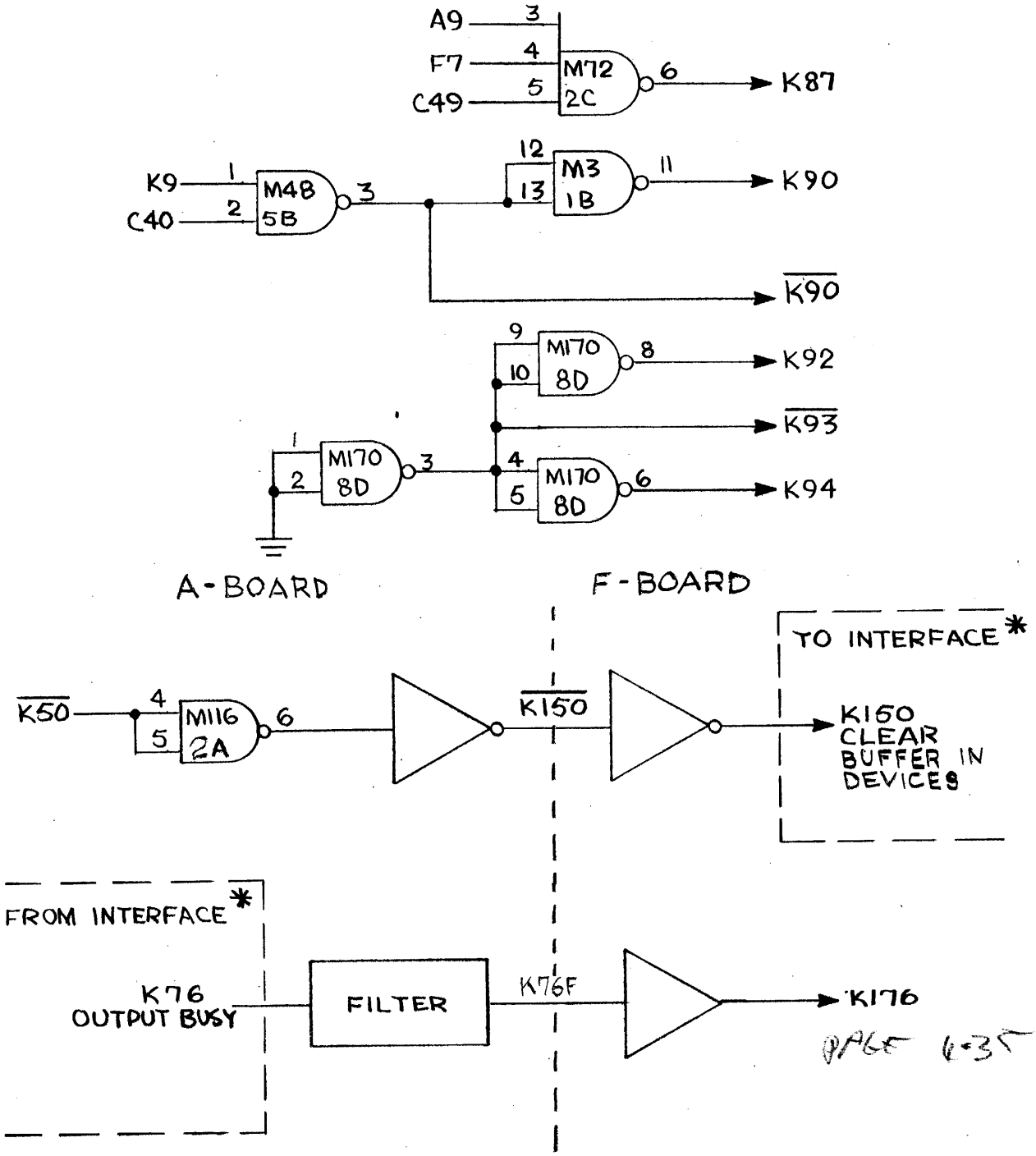
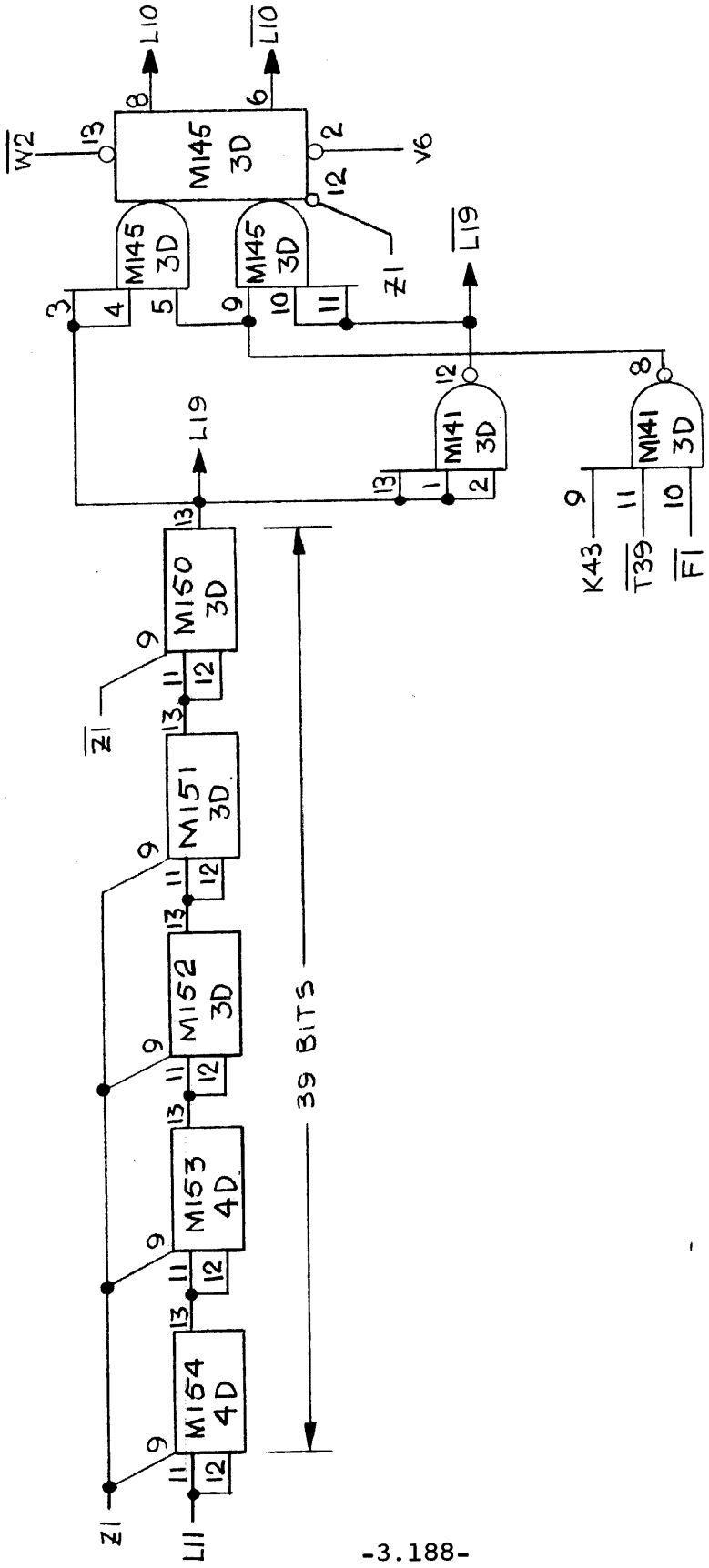
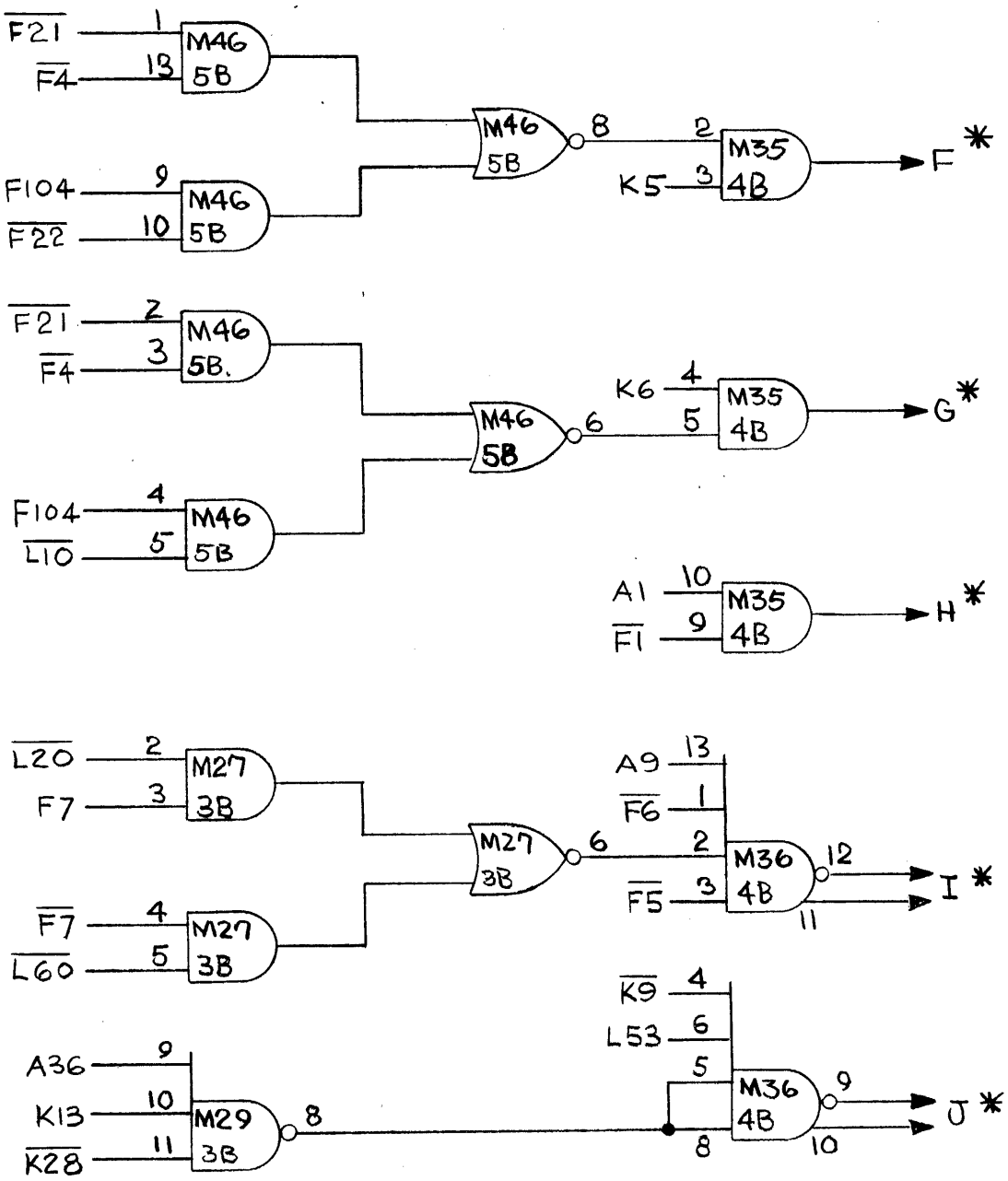


Figure 3.79 Logic Diagram. Rev. 1MAY69



ACCUMULATOR
40 BITS

Figure 3.80 Logic Diagram.

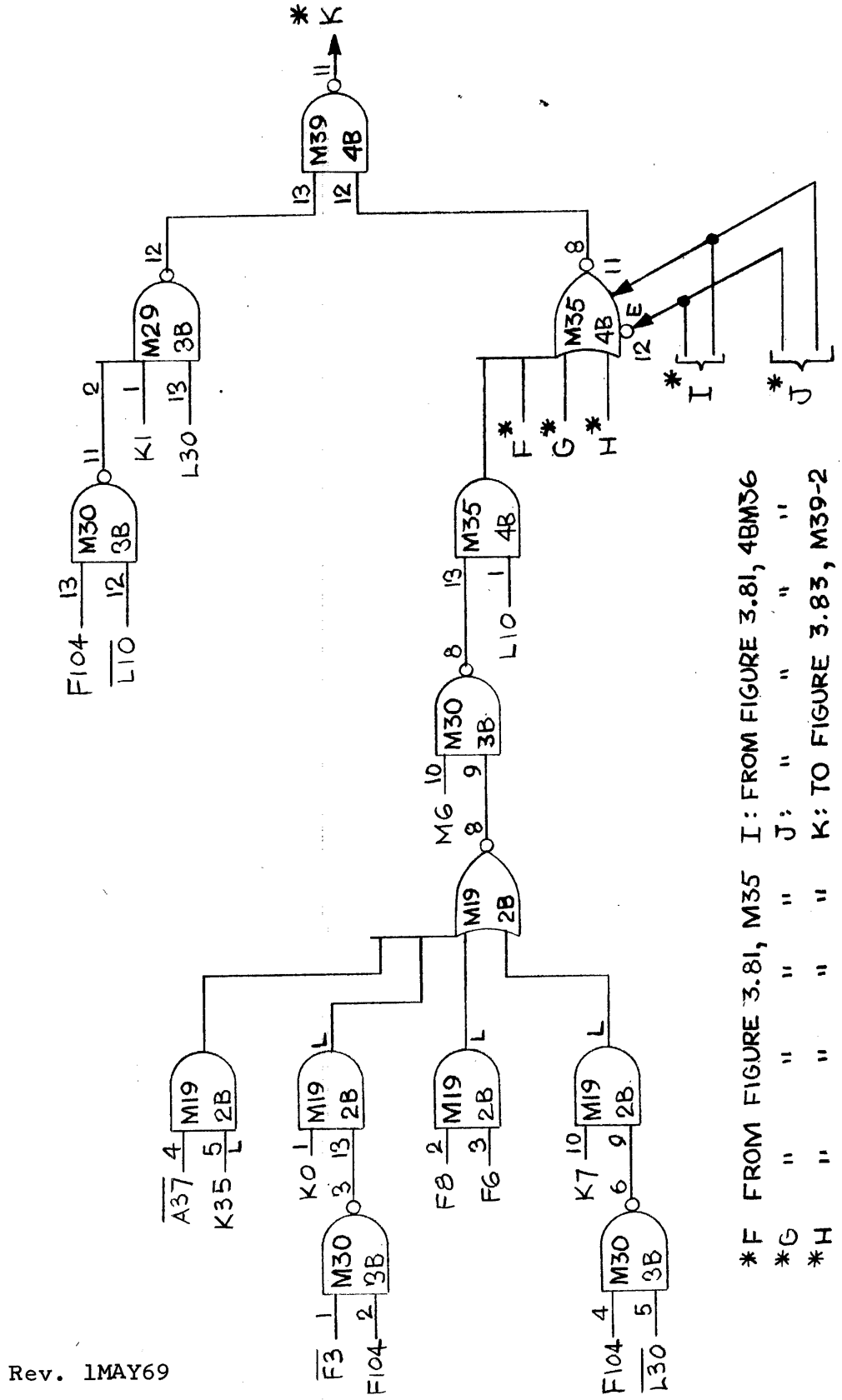


*F TO FIGURE 3.82, M35 I: TO FIGURE 3.82, M35
*G " " " " J: " " " "
*H " " " "

PART OF ACCUMULATOR RECORD NET

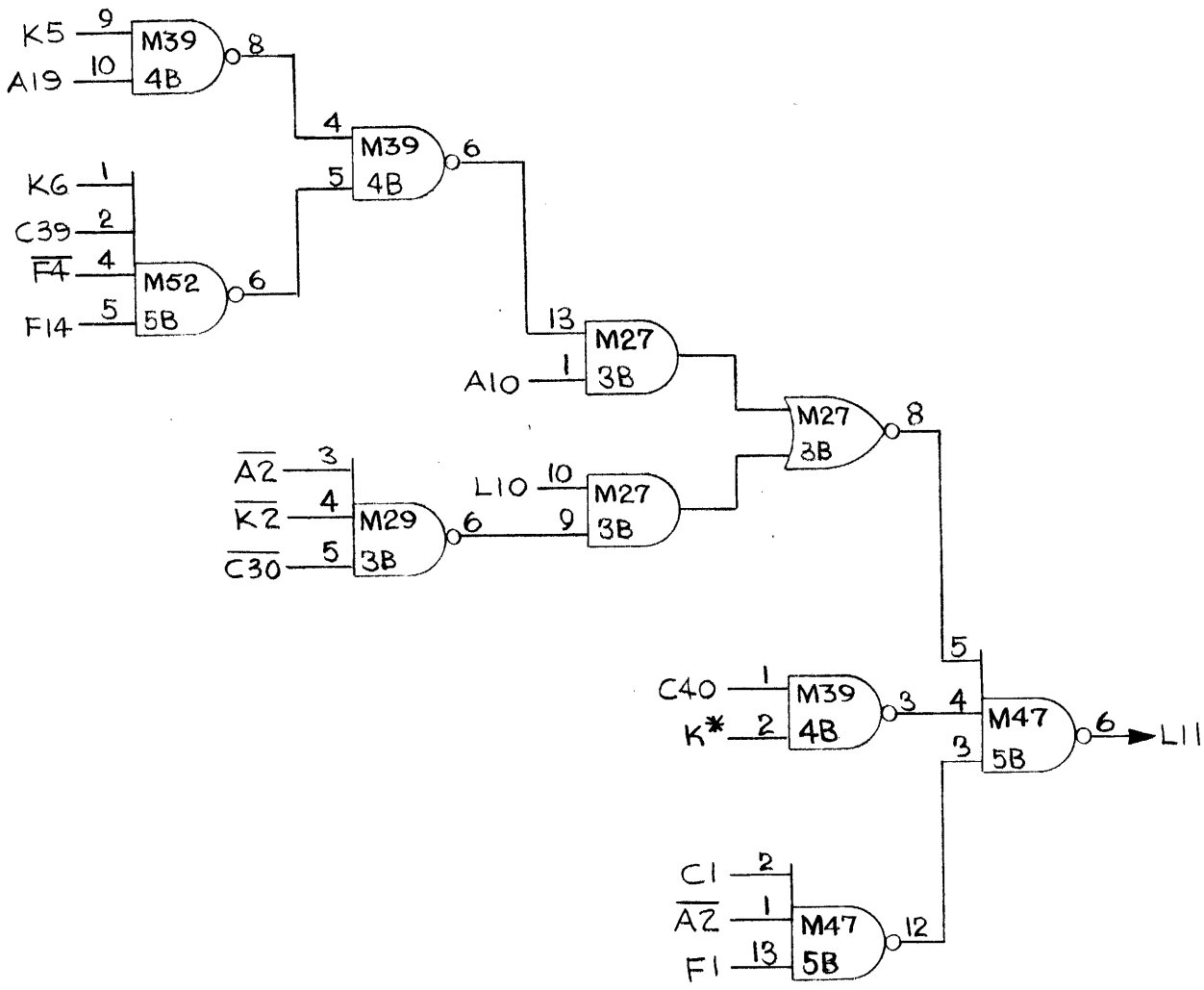
Figure 3.81 Logic Diagram.

Rev.18NOV68



PART OF ACCUMULATOR RECORD NET

Figure 3.82 Logic Diagram.



* K FROM FIGURE 3.82, M39-11

PART OF ACCUMULATOR RECORD NET

Figure 3.83 Logic Diagram.

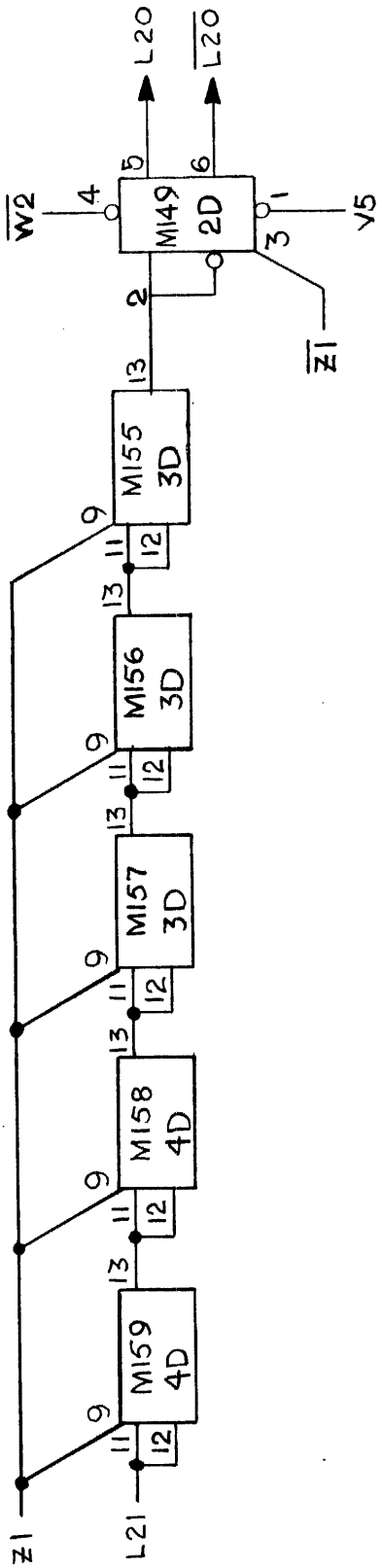
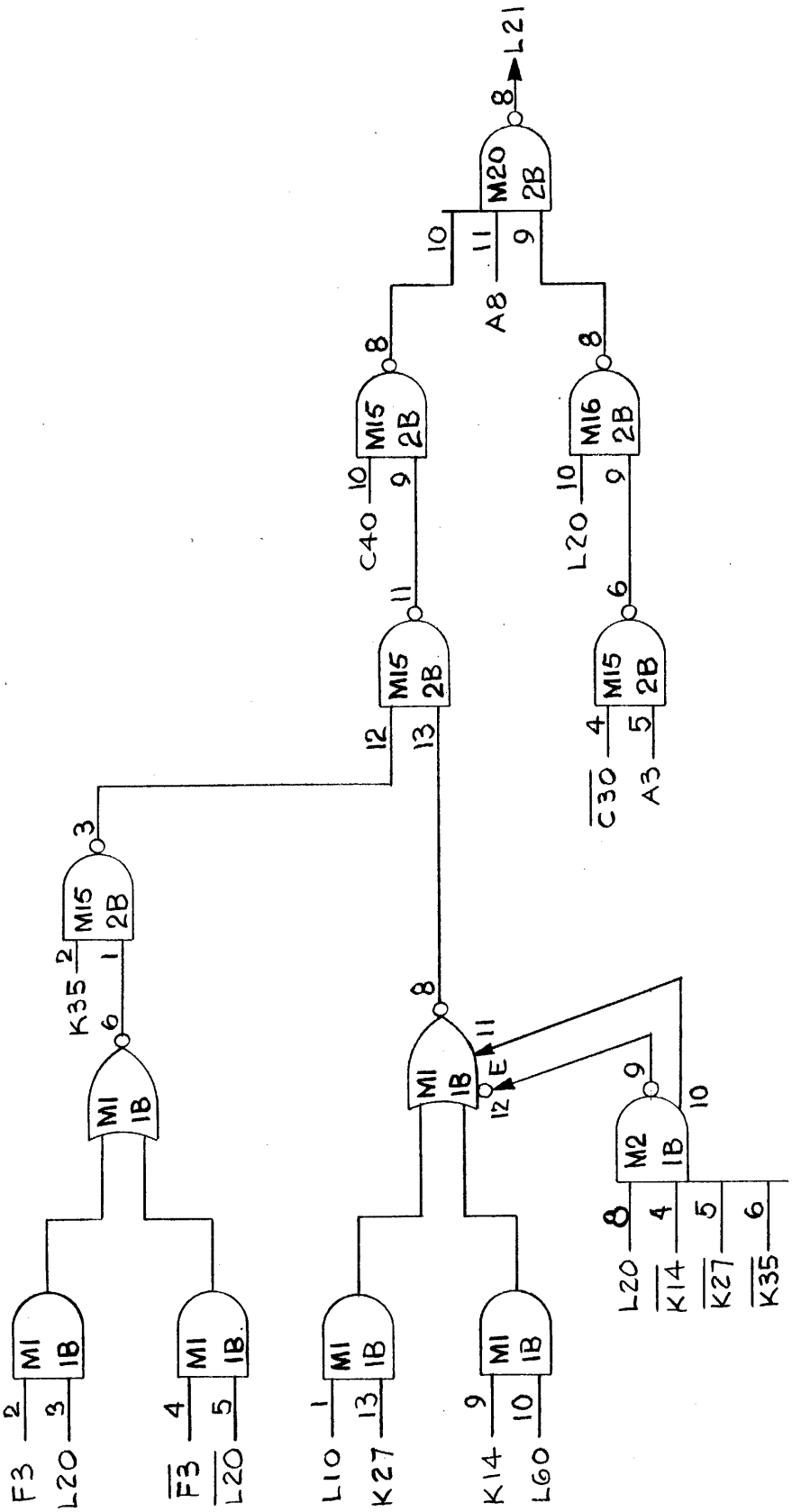


Figure 3.84 Logic Diagram.



INSTRUCTION REGISTER RECORD NET

Figure 3.85 Logic Diagram.

Rev.18NOV68

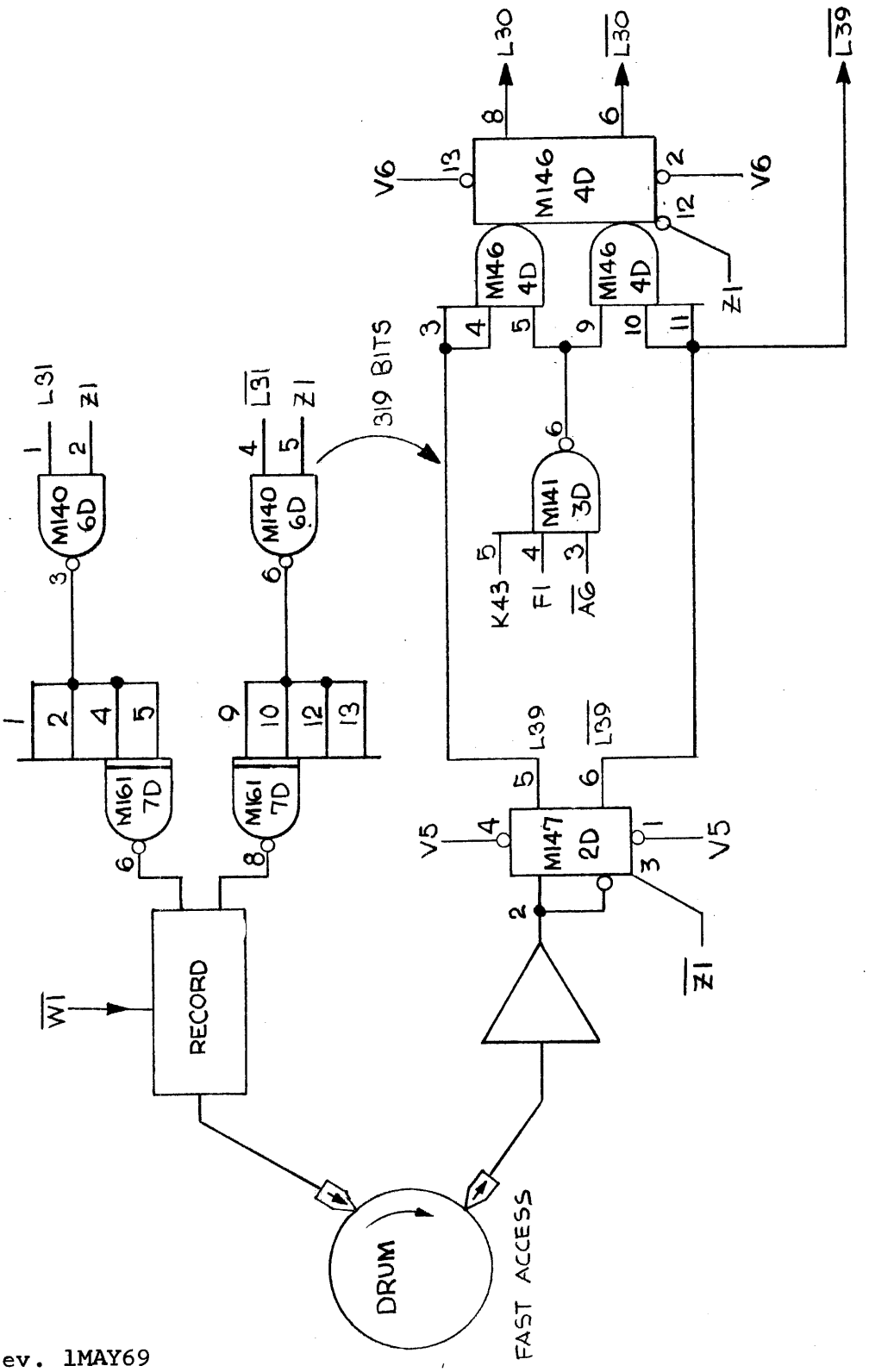
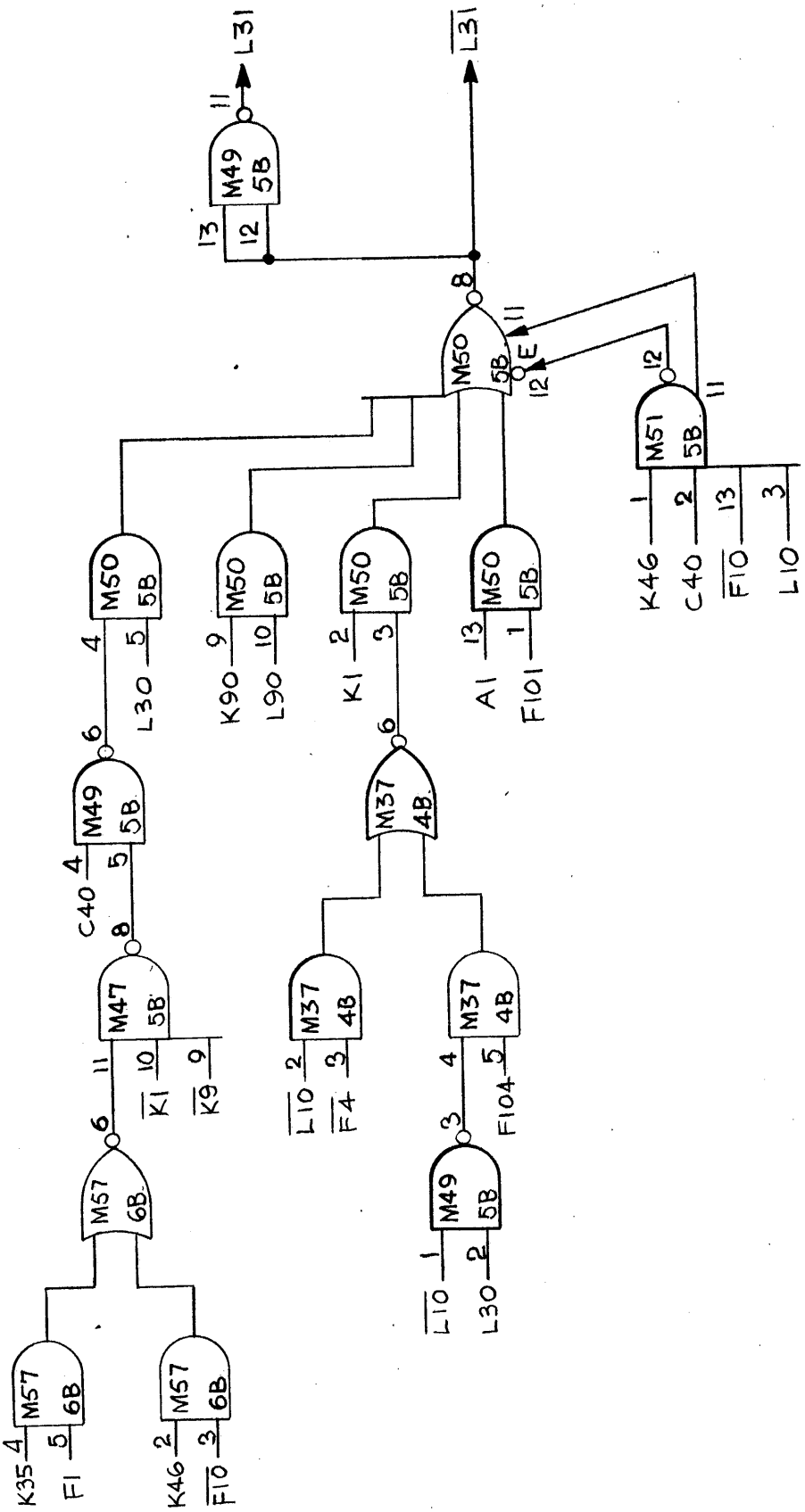


Figure 3.86 Logic Diagram.



FAST ACCESS RECORD NET

Figure 3.87 Logic Diagram.

Rev.18NOV68

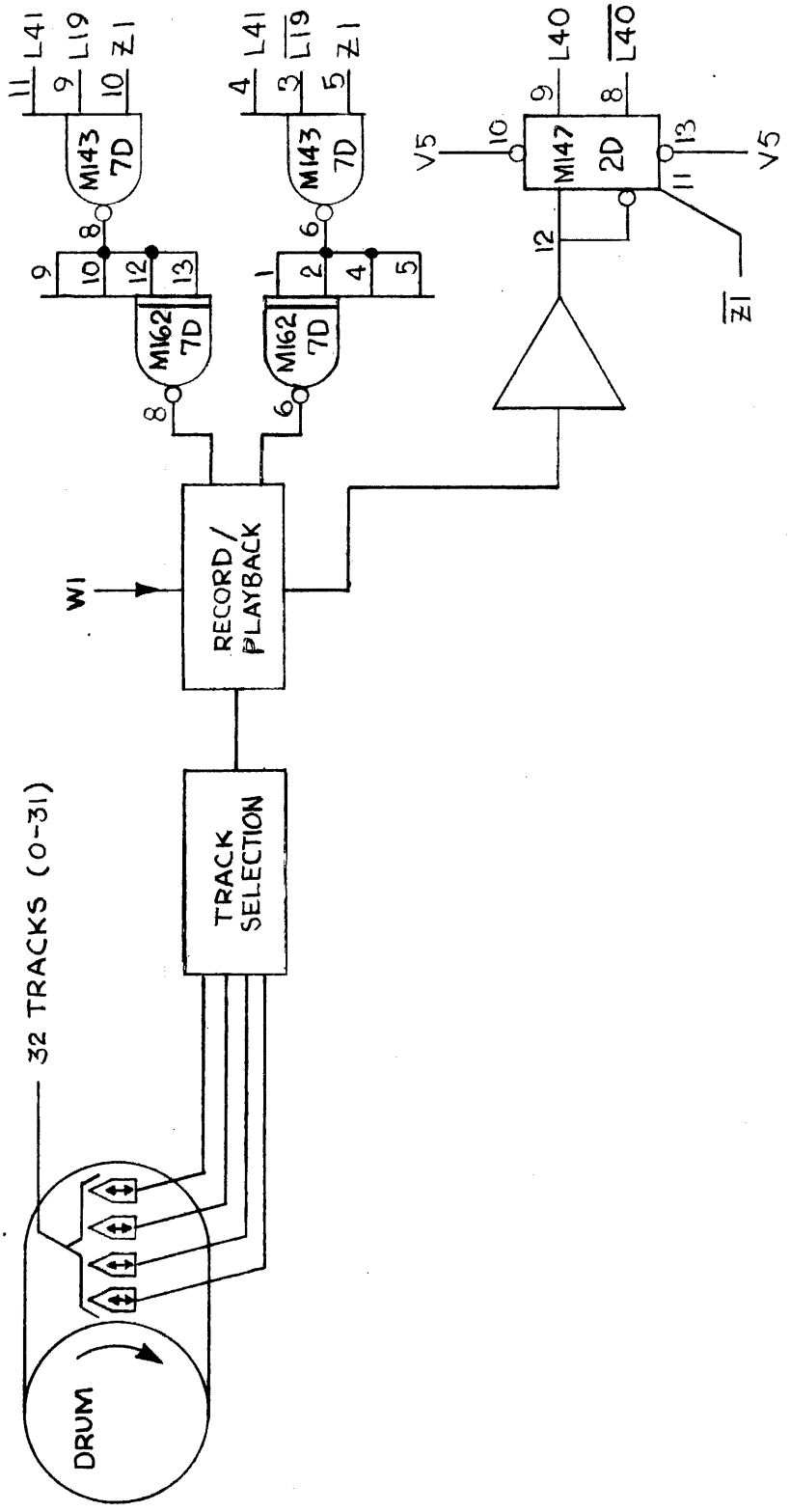
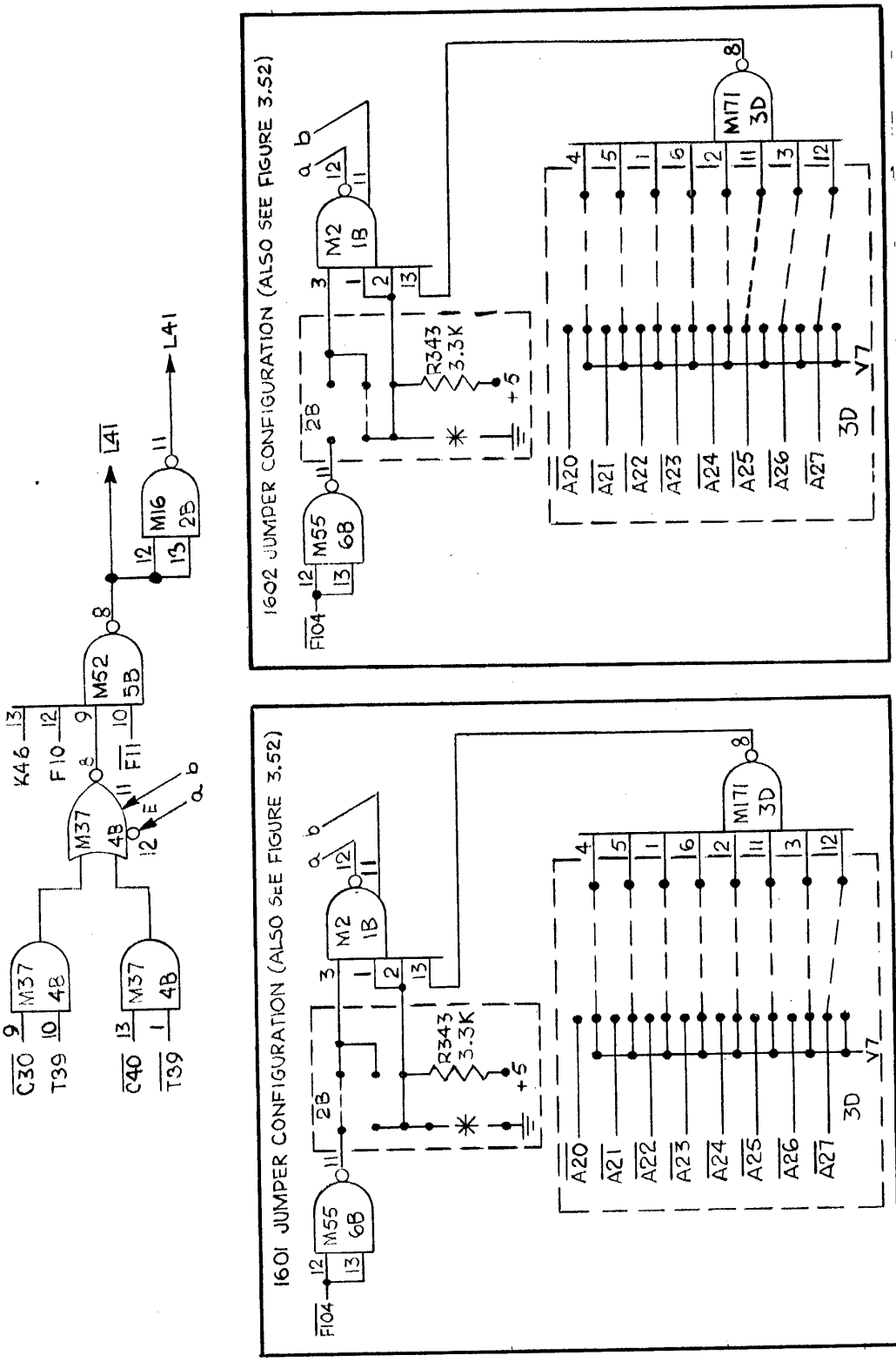


Figure 3.88.1 Logic Diagram.



* IF JUMPER IS CONNECTED, TRACKS 30 AND 31 OF THE 1601 OR TRACKS 10, 11, 12, 13, 14, AND 15 OF THE 1602 ARE UNSEALED (FOR SERVICE USE ONLY). IF JUMPER IS REMOVED, THESE TRACKS ARE SEALED (NORMAL USE).

Figure 3.88.2 Logic Diagram.

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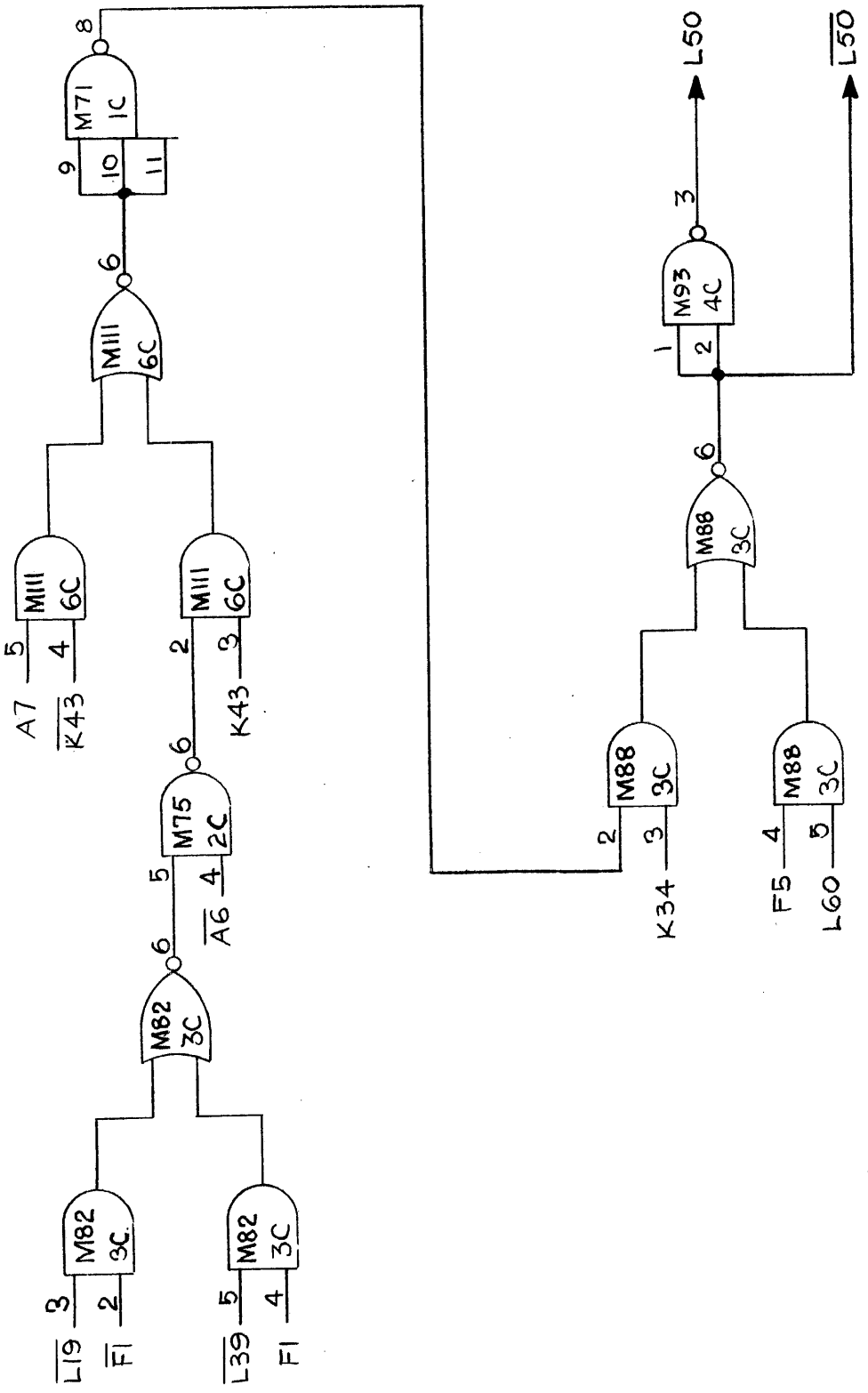


Figure 3.89 Logic Diagram.

Rev.18NOV68

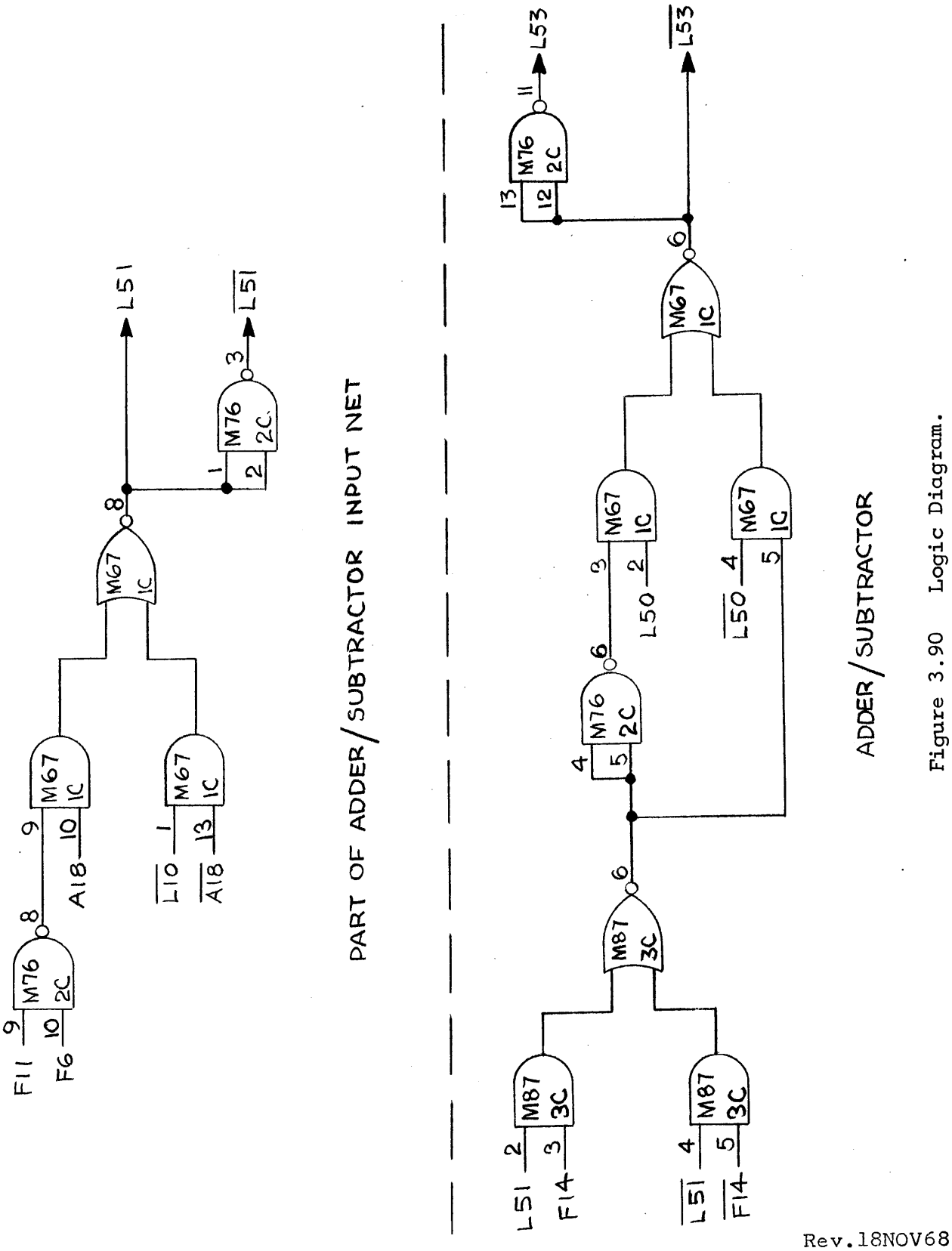


Figure 3.90 Logic Diagram.

Rev.18NOV68

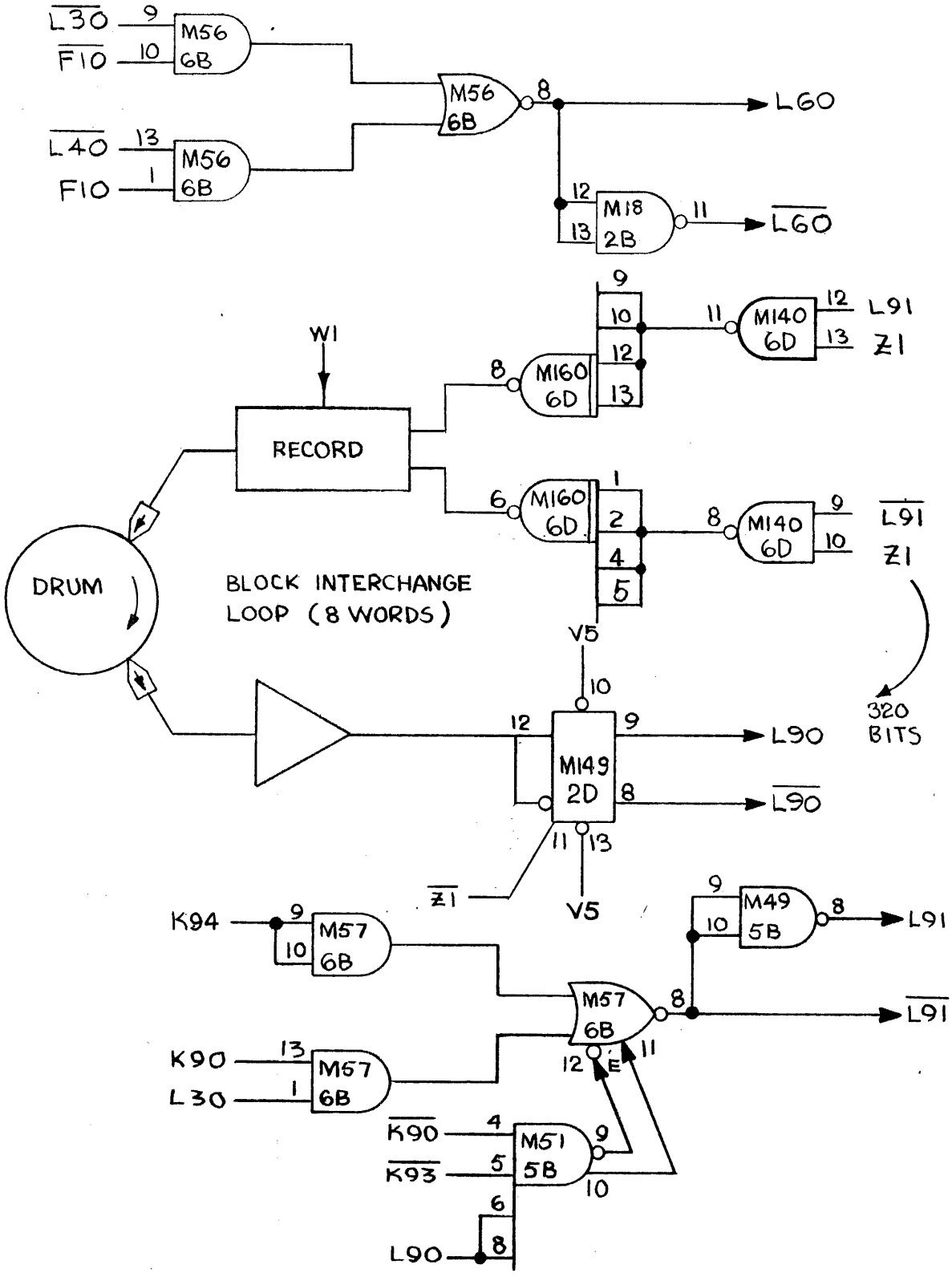


Figure 3.91 Logic Diagram.

HALT - BLUE. PEN

RUN - RED.

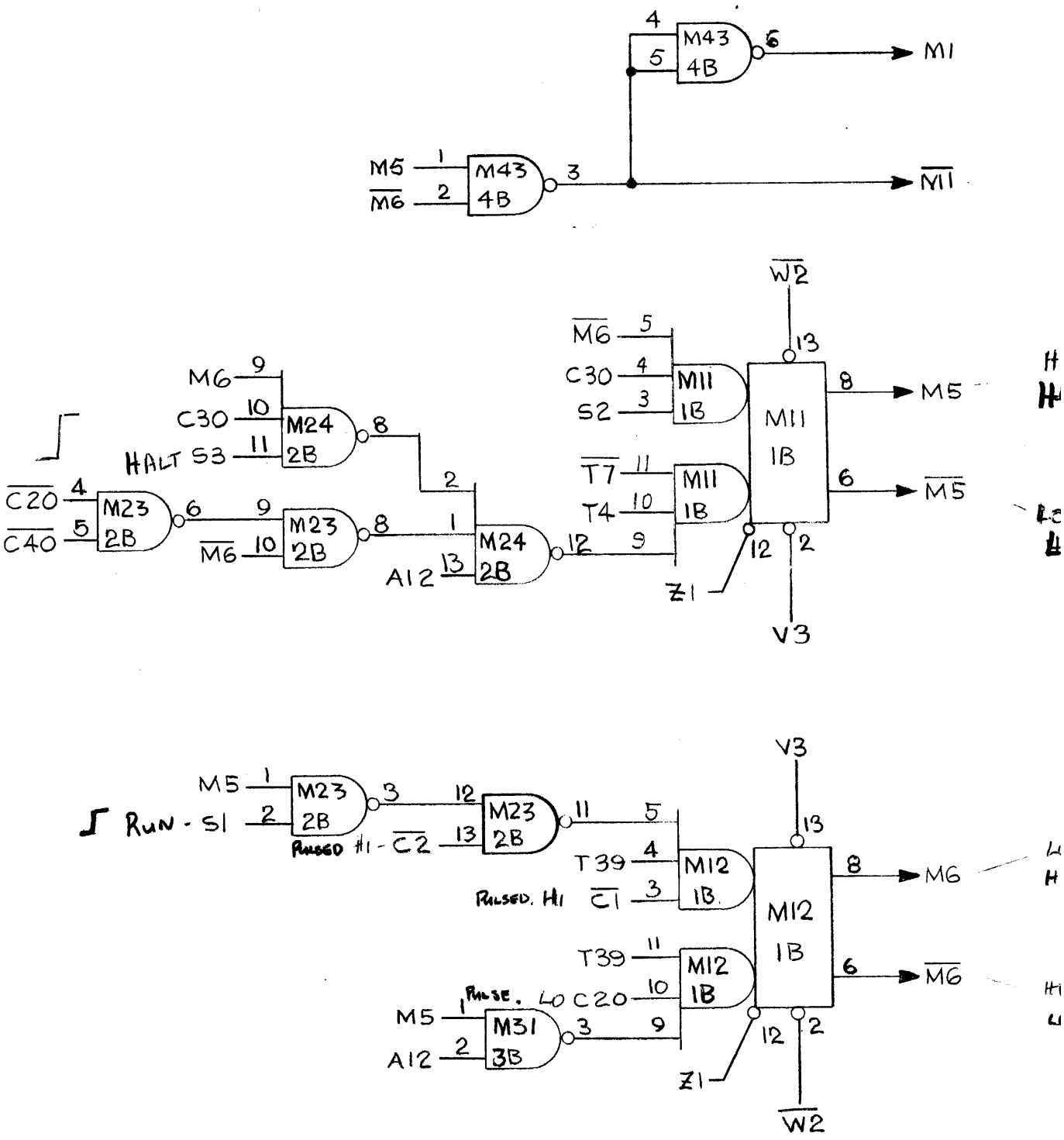
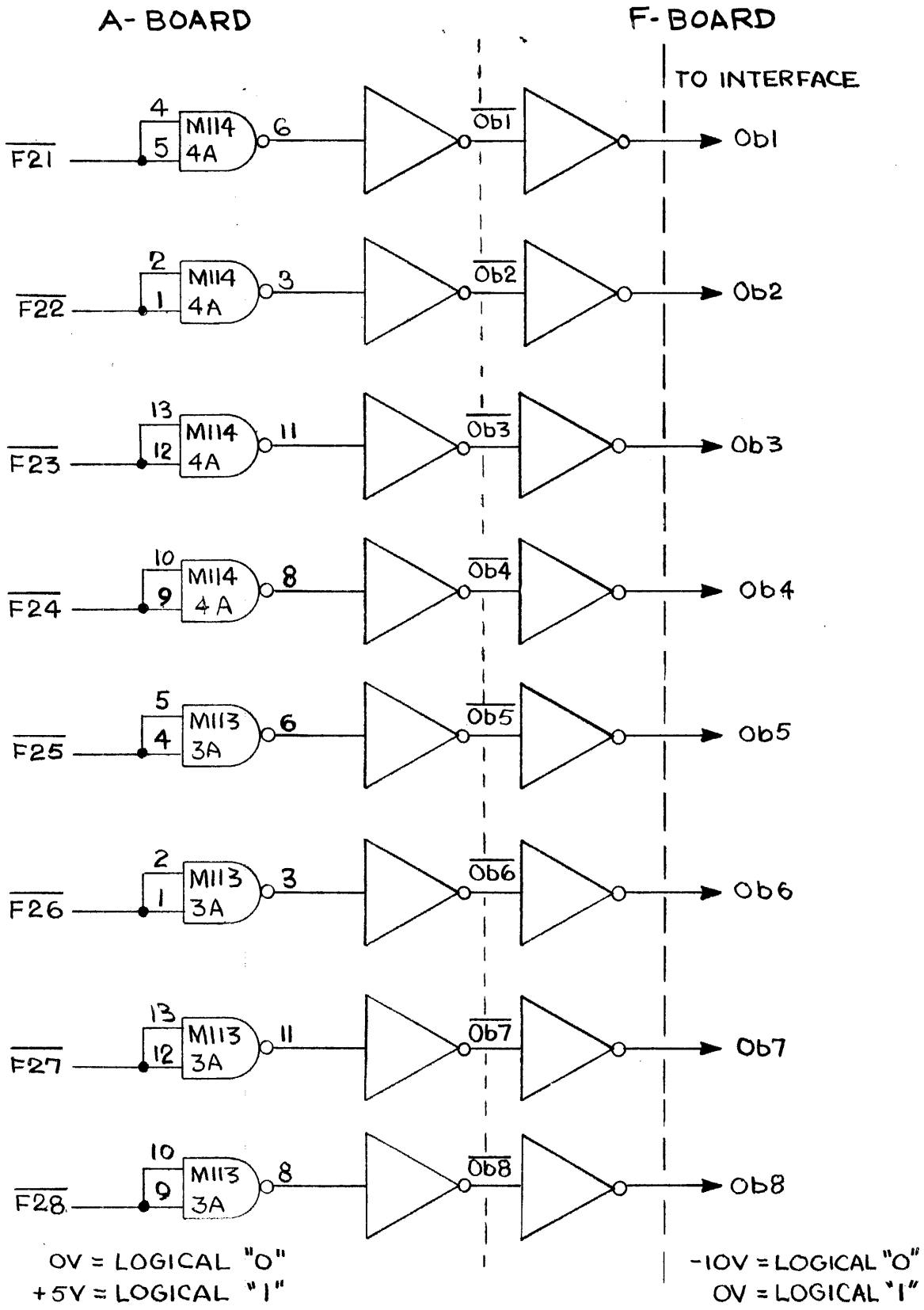


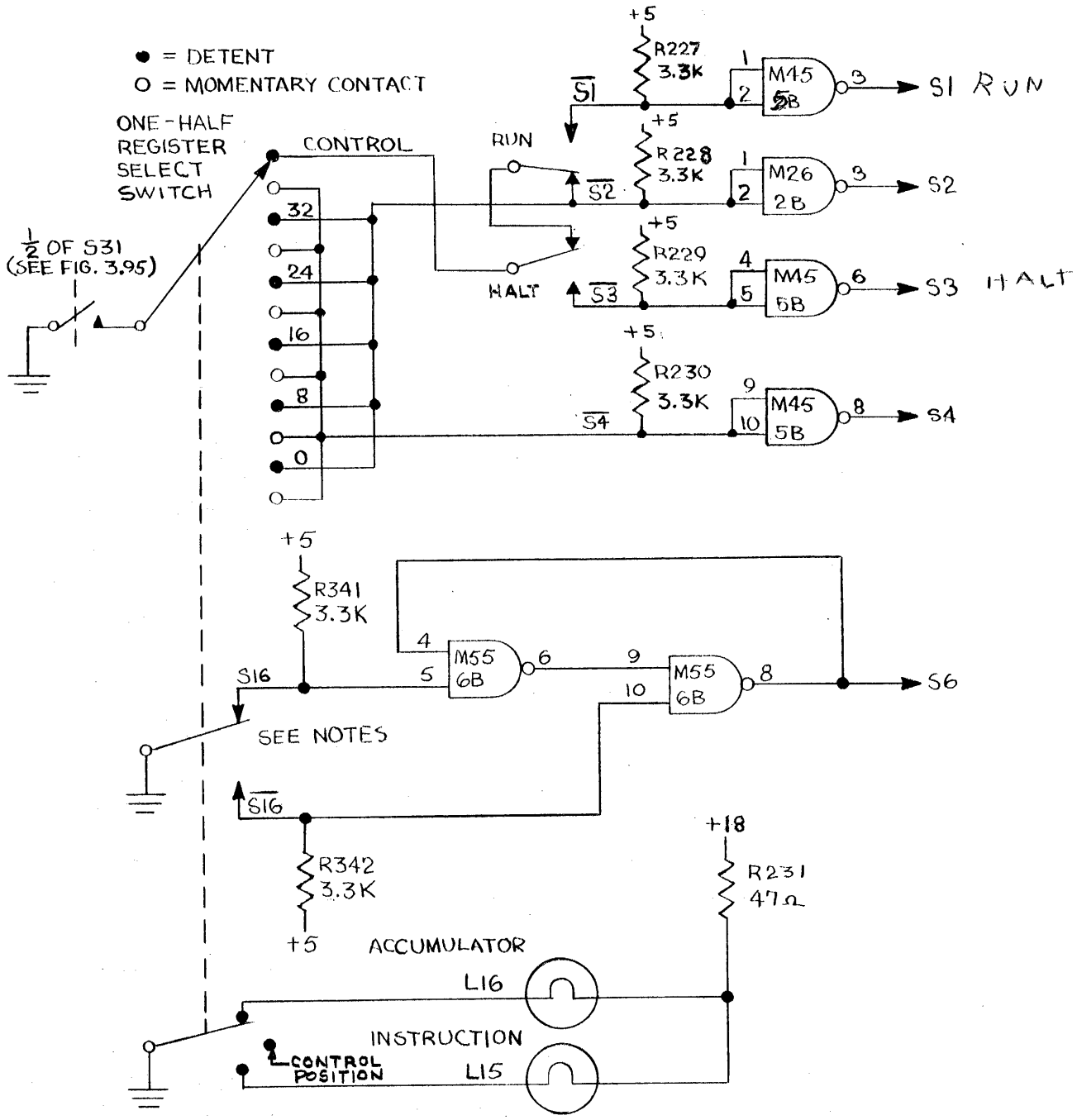
Figure 3.92 Logic Diagram.

Rev. 1MAY69



Rev. 1MAY69

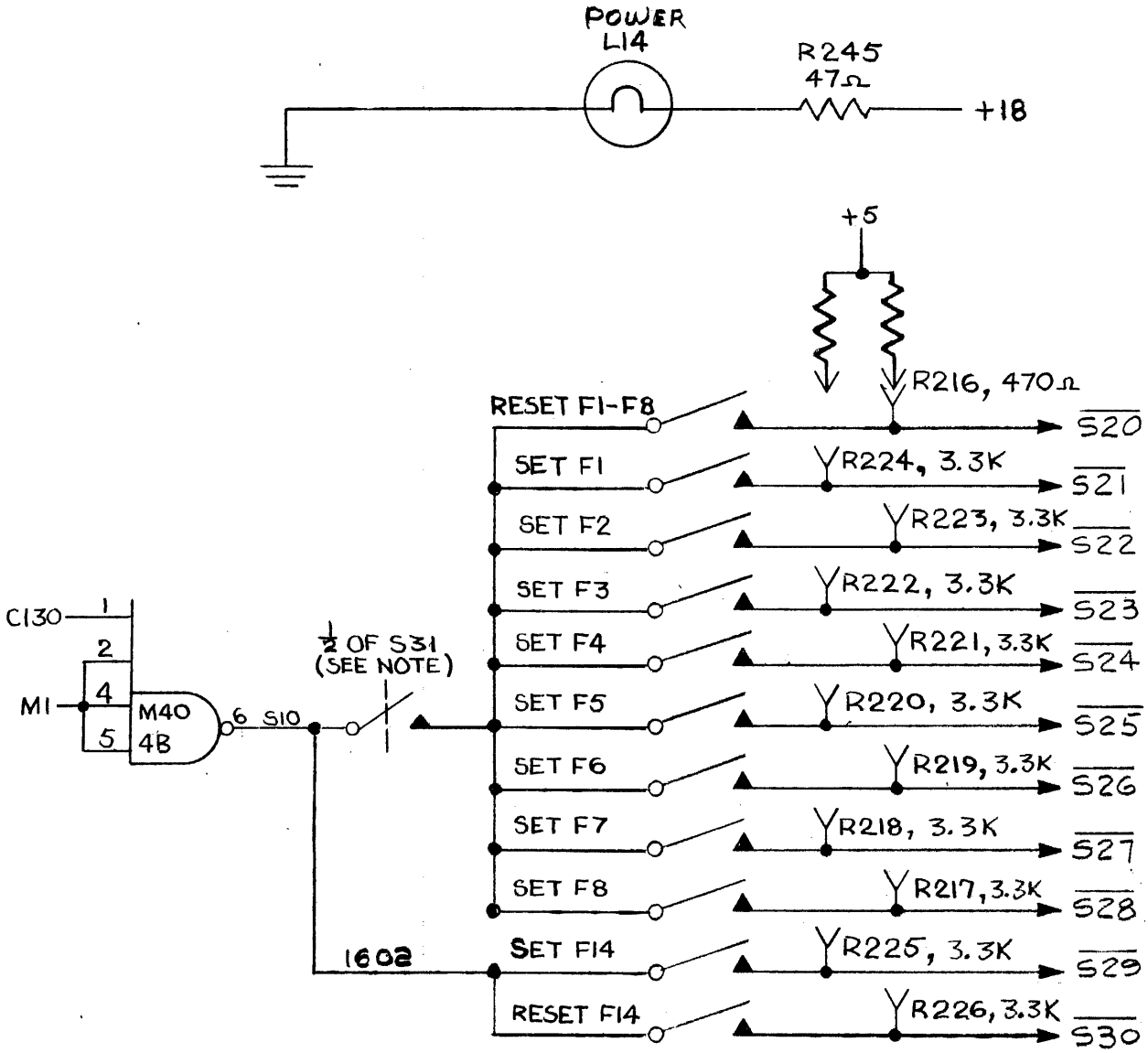
Figure 3.93 Logic Diagram.



NOTES: S16 = OV FOR UPPER CONTROL AND ALL I POSITIONS, $\overline{S16}$ = OV FOR LOWER CONTROL AND ALL A POSITIONS OF REGISTER SELECT SWITCH. L16 LIT FOR ALL A POSITIONS, L15 LIT FOR ALL I POSITIONS, L16 AND L15 UNLIT FOR BOTH CONTROL POSITIONS.

WITH THE EXCEPTION OF S31, ALL SWITCHES, RESISTORS, AND LAMPS ARE LOCATED ON BOARD G.

Figure 3.94 Logic Diagram. Rev. 1MAY69



NOTE: S31, LOCATED ON CONTROL PANEL HOUSING AND SHOWN IN FIGURES 3.94 AND 3.95, IS ALWAYS CLOSED FOR THE 1601. FOR THE 1602, IT IS OPEN WHEN THE BACK PANEL OF THE PROCESSOR IS CLOSED, AND CLOSED WHEN THE BACK PANEL IS OPEN.

WITH THE EXCEPTION OF S31, ALL SWITCHES, RESISTORS, AND THE LAMP ARE LOCATED ON BOARD G.

Rev. 1MAY69

Figure 3.95 Logic Diagram.

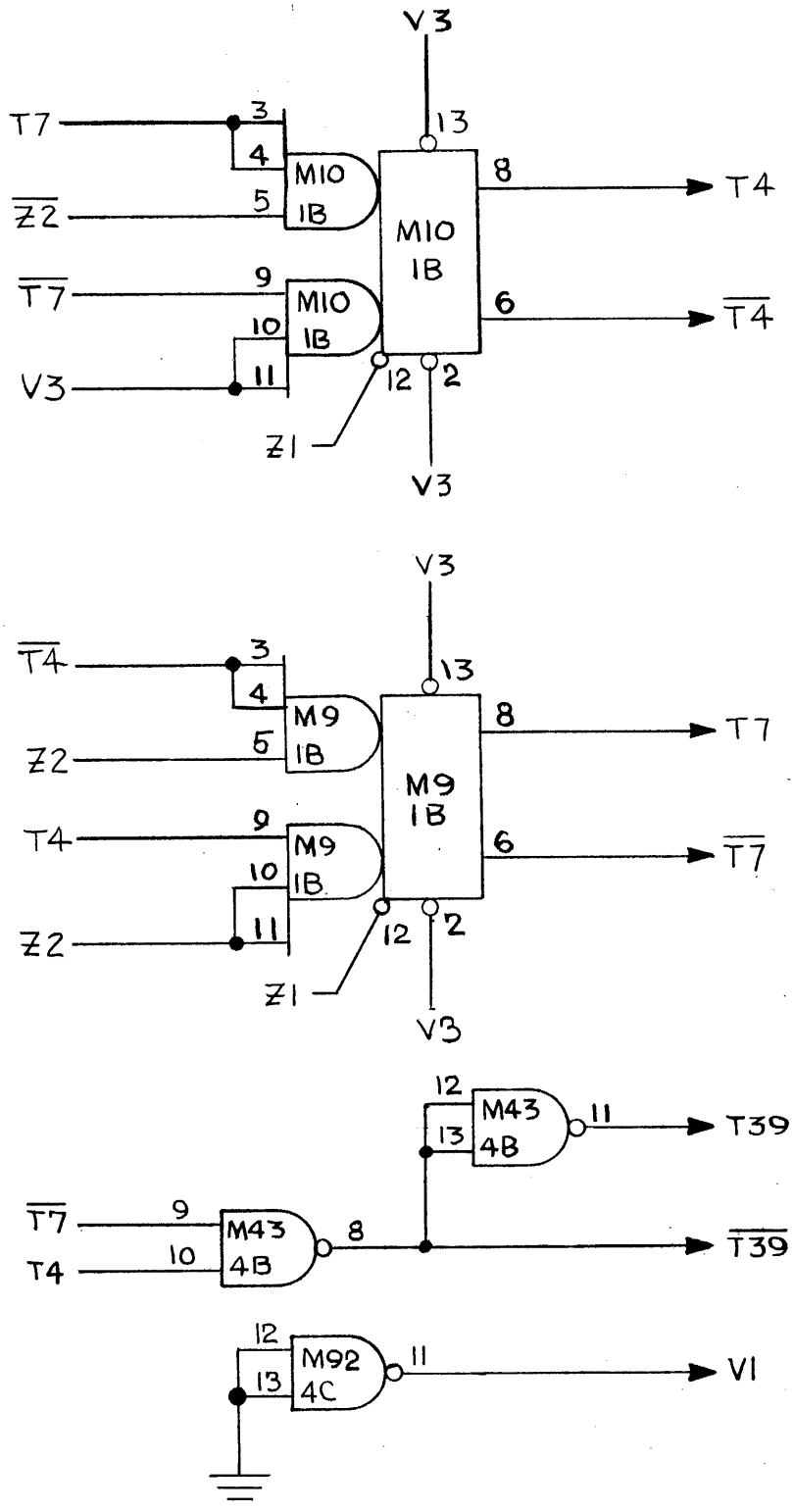


Figure 3.96 Logic Diagram.

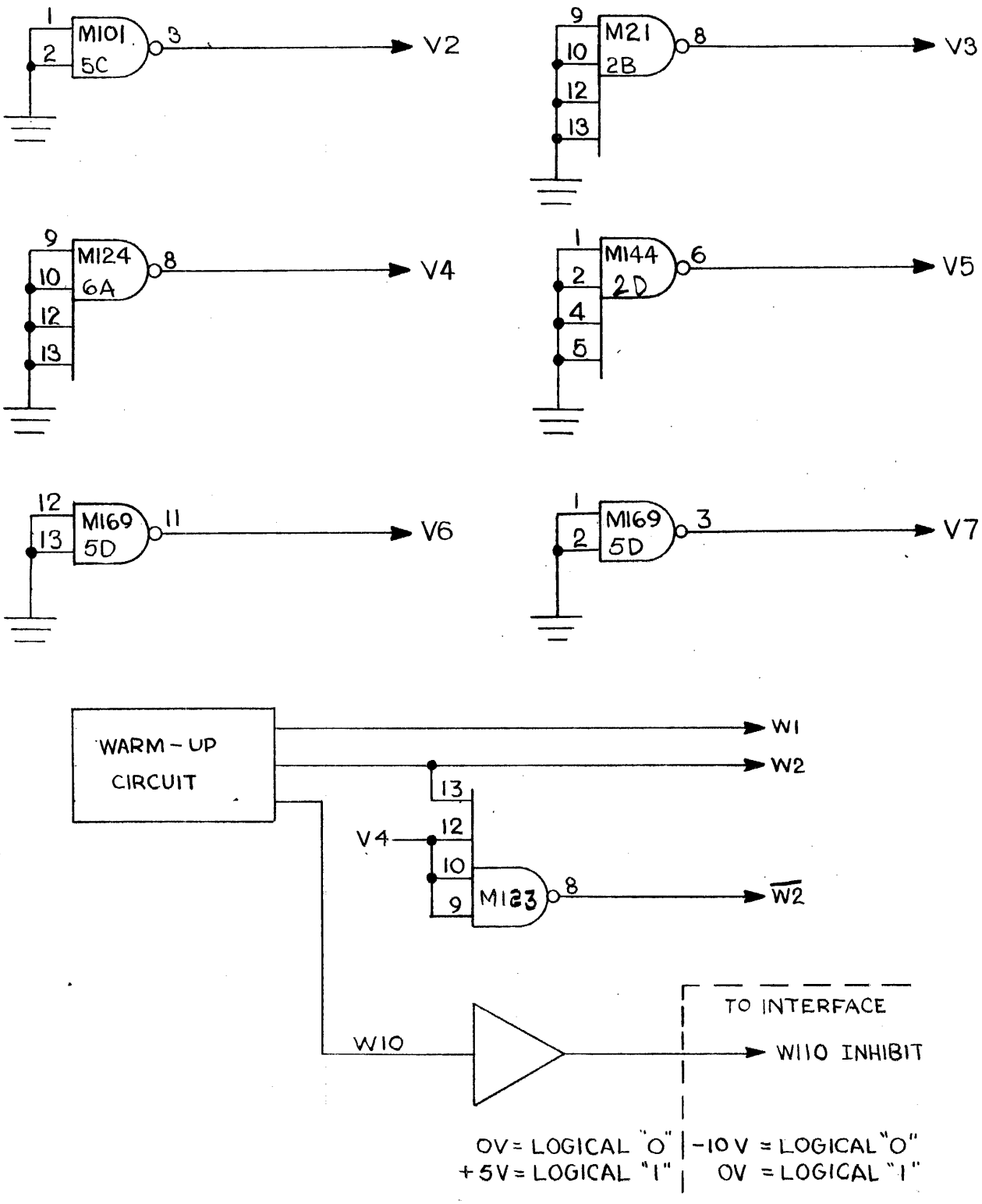


Figure 3.97 Logic Diagram.

Rev. 1MAY69

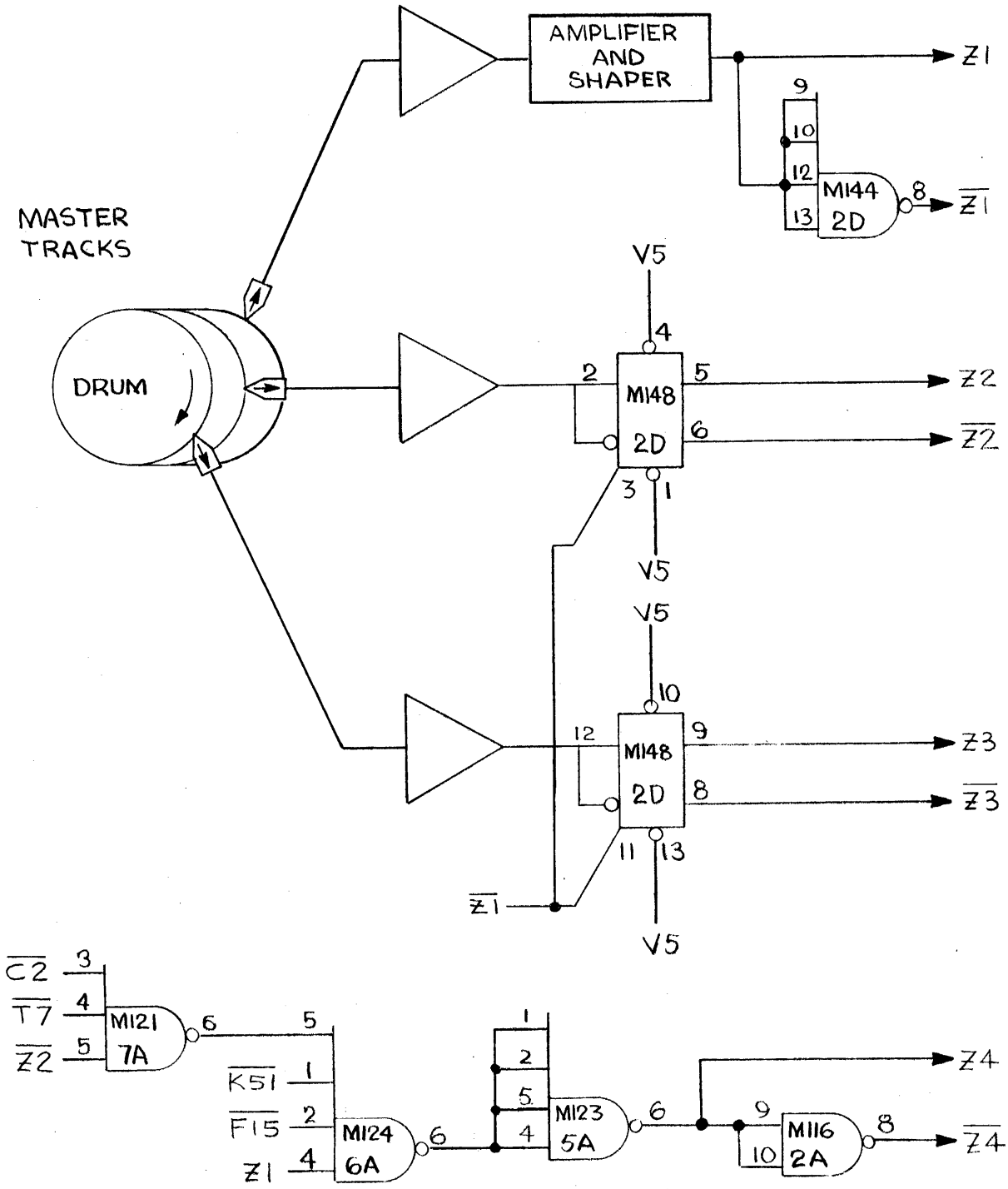
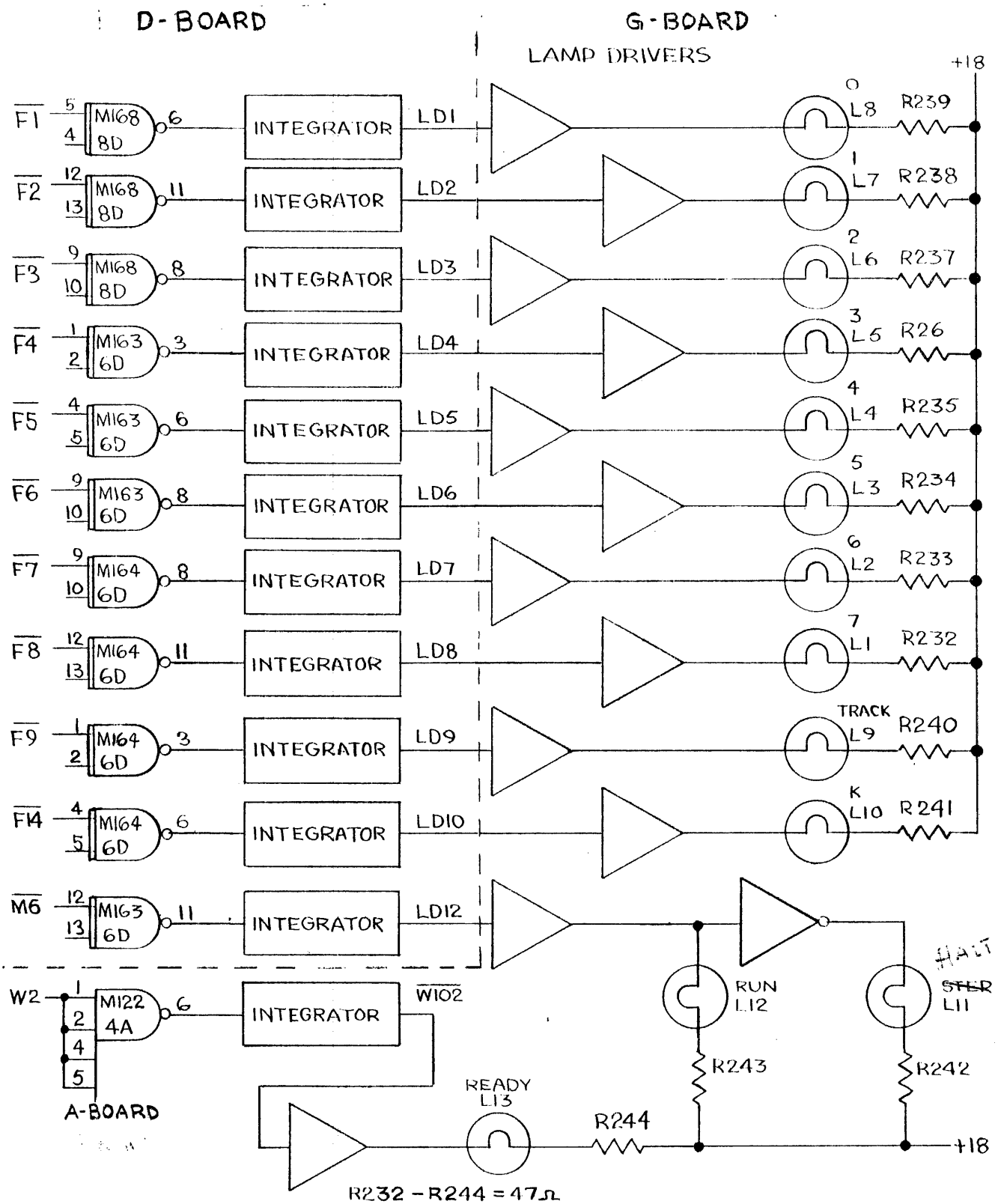


Figure 3.98 Logic Diagram.



Rev. 1MAY69

Figure 3.99 Logic Diagram.

3.8 SIGNAL GLOSSARY

The following signal glossary lists all the logic signals used in the processor with the following exceptions. Suppose signal A35 goes through an amplifier, it would then become signal A135 since any time a signal is amplified and not inverted its number is increased by 100. Only signal A35 would be listed in the glossary unless signal A135 performs a unique function, in which case A135 would be listed and A35 would probably not be listed.

Signal	Description or Function	Logic Figure No.
A1	Record Gate	3.49
A2	$\overline{C1}$ A3	3.49
A3	$\overline{M1}$ v $\overline{S6}$ v W2	3.49
A4	$\overline{K22}$ v C1	3.49
A5	$\overline{F8}$ $\overline{F7}$ M6	3.49
A6	T39 $\overline{F2}$	3.50
A7	$\overline{F1}$ L30 v $\overline{F1}$ L10	3.50
A8	$\overline{A2}$ v $\overline{F1}$	3.50
A9	$\overline{F8}$ $\overline{M6}$	3.50
A10	$\overline{F9}$ $\overline{F10}$	3.50
A11	$\overline{F5}$ F7 $\overline{M6}$	3.51
A12	$\overline{C20}$ v $\overline{K0}$ v $\overline{L20}$	3.51
A13	$\overline{C49}$ v $\overline{K9}$ v $\overline{Z3}$	3.51
A14	$\overline{(A11}$ $\overline{K9)}$ v $\overline{C39}$ v F14	3.51
A15	$\overline{K40}$ v $\overline{A6}$	3.51
A16	$\overline{K50}$ v $\overline{F21}$	3.51
A17	$\overline{K6}$ v $\overline{C37}$ v $\overline{L10}$	3.51
A18	$\overline{F8}$ F7	3.51
A19	C49 F3	3.52
A20	Select Track o v 1 v 16 v 17 (Matrix Column 1)	3.52
A21	Select Track 2 v 3 v 18 v 19 (Matrix Column 2)	3.52
A22	Select Track 4 v 5 v 20 v 21 (Matrix Column 3)	3.52
A23	Select Track 6 v 7 v 22 v 23 (Matrix Column 4)	3.52
A24	Select Track 8 v 9 v 24 v 25 (Matrix Column 5)	3.52
A25	Select Track 10 v 11 v 26 v 27 (Matrix Column 6)	3.52
A26	Select Track 12 v 13 v 28 v 29 (Matrix Column 7)	3.52
A27	Select Track 14 v 15 v 30 v 31 (Matrix Column 8)	3.52
A30	Select Track 0 v 2 v 4 v 6 v 8 v 10 v 12 v 14 (Matrix Row 1)	3.52
A31	Select Track 1 v 3 v 5 v 7 v 9 v 11 v 13 v 15 (Matrix Row 2)	3.52
A32	Select Track 16 v 18 v 20 v 22 v 24 v 26 v 28 v 30 (Matrix Row 3)	3.53
A33	Select Track 17 v 19 v 21 v 23 v 25 v 27 v 29 v 31 (Matrix Row 4)	3.53

Signal	Description or Function	Logic Figure No.
A35	K41 v $\overline{K13}$ v $\overline{A36}$	3.53
A36	$\overline{K0}$ v $\overline{F4}$ v F1	3.53
A37	$\overline{F1}$ $\overline{F2}$	3.53
A38	F5 $\overline{F6}$	3.53
A39	$\overline{F1}$ F2	3.53
C1	C10 v C20, Cycle Flipflop	3.54
C2	C10 v C40, Cycle Flipflop	3.55
C20	C1 $\overline{C2}$	3.56
C30	$\overline{C1}$ $\overline{C2}$	3.56
C37	C30 T7	3.56
C39	C30 T39	3.57
C40	$\overline{C1}$ C2	3.57
C49	C40 T39	3.57
F1	Command Register Bit	3.58
F2	Command Register Bit	3.58
F3	Command Register Bit	3.59
F4	Command Register Bit	3.60
F5	Command Register Bit	3.60
F6	Command Register Bit	3.61
F7	Command Register Bit	3.61
F8	Command Register Bit	3.61
F9	High-Order Instruction Register Bit Senser, Two Word-Time Counter, One Bit Delay, or Control Flipflop.	3.62
F10	Parity Control, High-Order 5 Bit Instruction Register Senser, Select General Storage, One Bit Delay, or Control Flipflop.	3.63
F11	Device Select Common, Sector Location, or One Bit Delay Flipflop.	3.65
F12	Parity Failure Flipflop	3.65
F14	Carry or Control Flipflop	3.69
F15	Output Common or Device Select Common Flipflop	3.69
F20	Buffer Register Timing Flipflop	3.70
F21	Buffer Register Bit	3.71
F22	Buffer Register Bit	3.71
F23	Buffer Register Bit	3.71
F24	Buffer Register Bit	3.71
F25	Buffer Register Bit	3.71
F26	Buffer Register Bit	3.71
F27	Buffer Register Bit	3.70
F28	Buffer Register Bit	3.70

Signal	Description or Function	Logic Figure No.
Ib1	Input Bit 1	3.72
Ib2	Input Bit 2	3.72
Ib3	Input Bit 3	3.72
Ib4	Input Bit 4	3.72
Ib5	Input Bit 5	3.72
Ib6	Input Bit 6	3.72
Ib7	Input Bit 7	3.73
Ib8	Input Bit 8	3.73
K0	A5 $\overline{F5}$ $\overline{F6}$	3.73
K1	A5 $\overline{F5}$ F6 C40	3.73
K2	A5 F5 F6 C40	3.73
K5	A18 A11 $\overline{F6}$	3.74
K6	A18 A11 F6	3.74
K7	A5 A38 C40	3.74
K9	K28 F1 F3	3.74
K13	$\overline{A9}$ v $\overline{A38}$	3.74
K14	A9 A38 $\overline{F7}$	3.74
K22	A5 C37 $\overline{T4}$ ((F4 F5) v F6)	3.75
K27	K0 $\overline{F2}$ F3 F4	3.75
K28	K0 F2 F4	3.75
K34	K35 C40 $\overline{A39}$	3.75
K35	A18 $\overline{F5}$ M6	3.76
K37	$\overline{K35}$ v $\overline{F1}$ v $\overline{C49}$	3.76
K40	K34 F6 F4	3.76
K41	K42 $\overline{F6}$	3.76
K42	K34 $\overline{F4}$	3.76
K43	F4 ($\overline{F6}$ v $\overline{F9}$) K34	3.77
K46	A9 F5 F6 $\overline{F7}$	3.77
K50	K5 C40	3.77
K51	K5 C39 F14	3.77
K73	$\overline{Ib8}$ ("In Process" Signal)	3.73
K75	Input Busy Signal	3.78
K80	Output Common Signal	3.78
K82	Device Select Common	3.78
K83	Input/Status Control Signal	3.78
K87	$\overline{A9}$ v $\overline{F7}$ v $\overline{C49}$	3.79
K90	K9 C40	3.79
K93	Regenerate Block Interchange Loop Signal	3.91
K94	Block Interchange Device Input	3.91
K150	Clear Signal	3.79
K176	Output Busy Signal PAGE 4.35	3.79

Rev.18NOV68

Signal	Description or Function	Logic Figure No.
L10	Accumulator Register Playback	3.80
L11	Accumulator Register Record	3.83
L19	Accumulator Register Playback One Bit-Time Early	3.80
L20	Instruction Register Playback	3.84
L21	Instruction Register Record	3.85
L30	Fast Access Loop Playback	3.86
L31	Fast Access Loop Record	3.87
L39	Fast Access Loop Playback One Bit-Time Early	3.86
L40	General Storage Playback	3.88
L41	General Storage Record Enable	3.88
L50	Part of Adder/Subtractor Input Net	3.89
L51	Part of Adder/Subtractor Input Net	3.90
L53	Adder/Subtractor Output	3.90
L60	F10 L40 v $\overline{\text{F10}}$ L30	3.91
L90	Block Interchange Loop Playback	3.91
L91	Block Interchange Loop Record	3.91
M1	Idle Mode	3.92
M5	M1 or M3, Mode Flipflop	3.92
M6	M2 or M3, Mode Flipflop	3.92
Ob1	Output Bit 1	3.93
Ob2	Output Bit 2	3.93
Ob3	Output Bit 3	3.93
Ob4	Output Bit 4	3.93
Ob5	Output Bit 5	3.93
Ob6	Output Bit 6	3.93
Ob7	Output Bit 7	3.93
Ob8	Output Bit 8	3.93
S1	RUN Button Depressed, STEP Button Not Depressed, and REGISTER SELECT Switch in CONTROL Position.	3.94
S2	Positions 0, 8, 16, 24, and 32 of REGISTER SELECT Switch or RUN and STEP Buttons Not Depressed while REGISTER SELECT Switch in CONTROL Position.	3.94
S3	STEP Button Depressed and REGISTER SELECT Switch in CONTROL Position.	3.94
S4	Momentary Contact Position of REGISTER SELECT Switch	3.94
S6, S16	Accumulator Register Positions of REGISTER SELECT Switch	3.94
S20	Reset F1 through F8	3.95
S21	Set F1	3.95
S22	Set F2	3.95
S23	Set F3	3.95
S24	Set F4	3.95
S25	Set F5	3.95

Signal	Description or Function	Logic Figure No.
S26	Set F6	3.95
S27	Set F7	3.95
S28	Set F8	3.95
S29	Set F14	3.95
S30	Reset F14	3.95
T4	5-Bit Duration Timing Pulse	3.96
T7	7-Bit Duration Timing Pulse	3.96
T39	$\overline{T7}$ T4	3.96
V1	Constant +5v	3.96
V2	Constant +5v	3.97
V3	Constant +5v	3.97
V4	Constant +5v	3.97
V5	Constant +5v	3.97
V6	Constant +5v	3.97
W2	Warm-Up Signal	3.97
W110	Inhibit Signal	3.97
Z1	Bit-Time Timing Clock	3.98
Z2	Sector Index Clock	3.98
Z3	Sector Address Clock	3.98
Z4	Buffer Register Timing Gate	3.98

CHAPTER 4. CIRCUITS

4.1 INTEGRATED CIRCUIT PACKAGES (IC'S)

The integrated circuitry of the processor uses a variety of IC package types. Each IC package is related in the following list to the IC package designation that appears in the logic symbols used through this manual.

Logic Symbol Designation	IC Package Part Number
M1	585012
M2	585016
M3	585007
M4	585008
M5	585007
M6	585008
M7	585009
M8	585008
M9	585017
M10	585017
M11	585017
M12	585017
M13	585017
M14	585017
M15	585007
M16	585007
M17	585008

Logic Symbol Designation	IC Package Part Number
M18	585007
M19	585015
M20	585008
M21	585011
M22	585010
M23	585007
M24	585008
M25	585009
M26	585007
M27	585013
M28	585007
M29	585008
M30	585007
M31	585007
M32	585007
M33	585008
M34	585008
M35	585014
M36	585016
M37	585012
M38	585007
M39	585007
M40	585009
M41	585007

Logic Symbol Designation	IC Package Part Number
M42	585007
M43	585007
M44	585008
M45	585007
M46	585013
M47	585008
M48	585007
M49	585007
M50	585014
M51	585016
M52	585009
M53	585007
M54	585007
M55	585007
M56	585013
M57	585012
M58	585017
M59	585017
M60	585017
M61	585017
M62	585017
M63	585018
M64	585017
M65	585009

Logic Symbol Designation	IC Package Part Number
M66	585007
M67	585013
M68	585012
M69	585012
M70	585009
M71	585008
M72	585008
M73	585008
M74	585013
M75	585007
M76	585007
M77	585016
M78	585016
M79	585016
M80	585007
M81	585010
M82	585013
M83	585013
M84	585007
M85	585007
M86	585016
M87	585012
M88	585012
M89	585008

Logic Symbol Designation	IC Package Part Number
M90	585008
M91	585007
M92	585007
M93	585007
M94	585012
M95	585016
M96	585008
M97	585018
M98	585007
M99	585008
M100	585007
M101	585007
M102	585007
M103	585014
M104	585007
M105	585017
M106	585008
M107	585013
M108	585008
M109	585007
M110	585009
M111	585013
M112	585018
M113	585007

Logic Symbol Designation	IC Package Part Number
M114	585007
M115	585007
M116	585007
M117	585007
M118	585007
M119	585007
M120	585008
M121	585008
M122	585022**
M123	585011
M124	585011
M125	585015
M126	585017
M127	585017
M128	585018
M129	585018
M130	585018
M131	585019
M132	585007
M133	585023
M134	585023
M135	585023
M136	585023
M137	585023

Logic Symbol Designation	IC Package Part Number
M138	585023
M139	585007
M140	585007
M141	585008
M142	585008
M143	585008
M144	585011
M145	585017
M146	585017
M147	585019
M148	585019
M149	585019
M150	585020
M151	585020
M152	585020
M153	585020
M154	585020
M155	585020
M156	585020
M157	585020
M158	585020
M159	585020
M160	585022**
M161	585022**

Logic Symbol Designation	IC Package Part Number
M162	585022**
M163	585021*
M164	585021*
M165	585021*
M166	585021*
M167	585021*
M168	585021*
M169	585007
M170	585007
M171	585010
M172	585009
M173	585008
M174	585010

The following voltage specifications apply to those packages part numbers which are not denoted with an asterisk (with the exception of 585023 which is a differential comparator).

Logical 0 Output $\leq$ 0.4 volts Logical 0 Input $\leq$ 0.8 volts

Logical 1 Output $\geq$ 2.4 volts Logical 1 Input $\geq$ 2.0 volts

4.75 volts $\leq$ Vcc $\leq$ 5.25 volts

* The following voltage specifications apply to those packages part numbers denoted with a single asterisk.

Logical 0 Output $\leq$ 0.5 volts Logical 0 Input $\leq$ 0.95 volts

Logical 1 Output $\geq$ 2.5 volts Logical 1 Input $\geq$ 2.0 volts

4.75 volts $\leq$ Vcc $\leq$ 5.25 volts

** The following voltage specifications apply to those packages part numbers denoted with a double asterisk.

Logical 0 Output $\leq$ 0.5 volts Logical 0 Input $\leq$ 0.95 volts

Logical 1 Output $\geq$ 1.0 volts Logical 1 Input $\geq$ 2.0 volts

4.75 volts $\leq$ Vcc $\leq$ 5.25 volts

4.1.1 585007, QUADRUPLE 2-INPUT NAND GATE PACKAGE

Figure 4.1 shows the pin arrangement, logic, and a representative circuit schematic of this package.

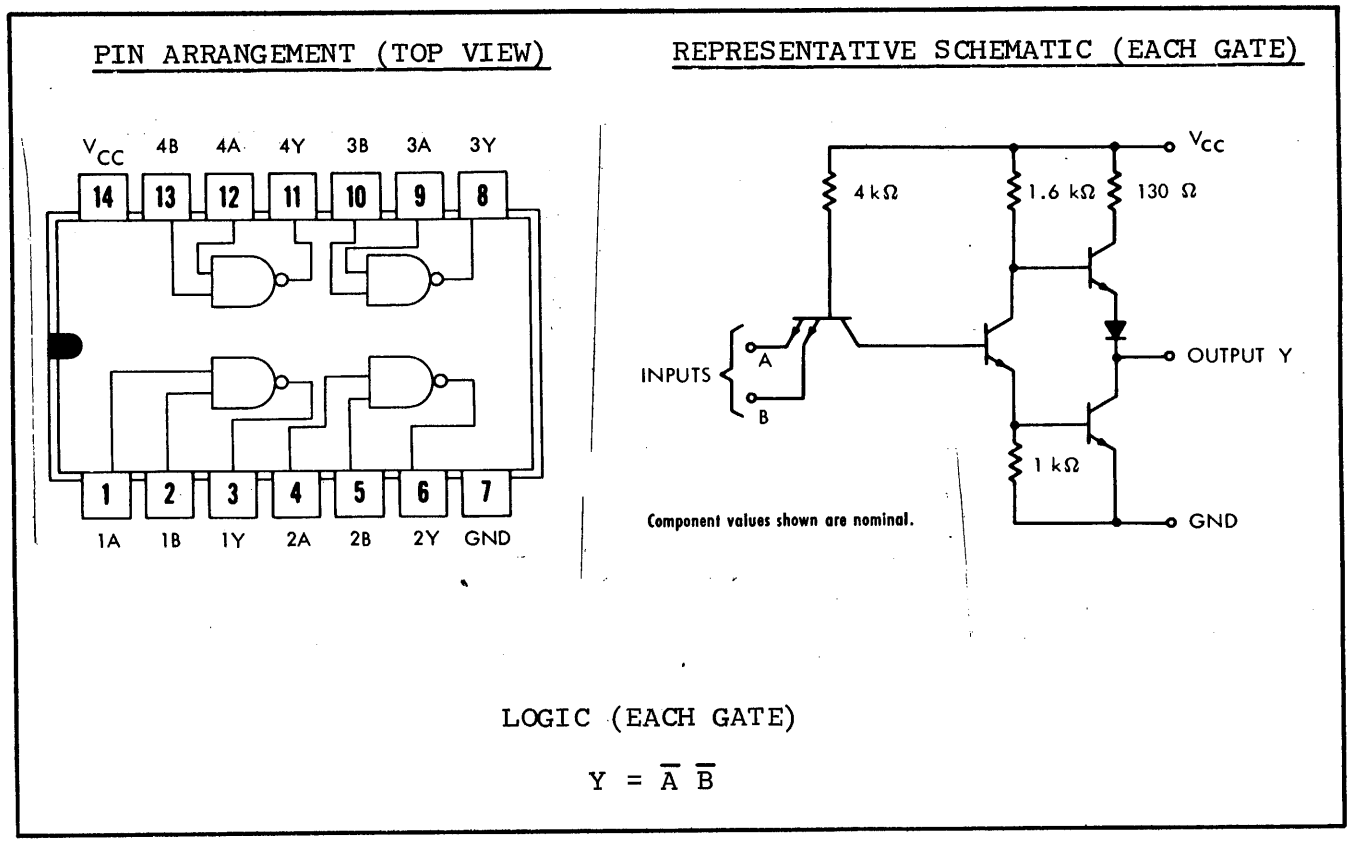
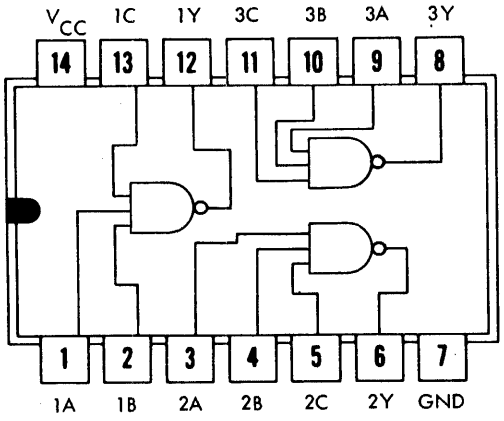


Figure 4.1 585007, Quadruple 2-Input Positive NAND Gate Package.

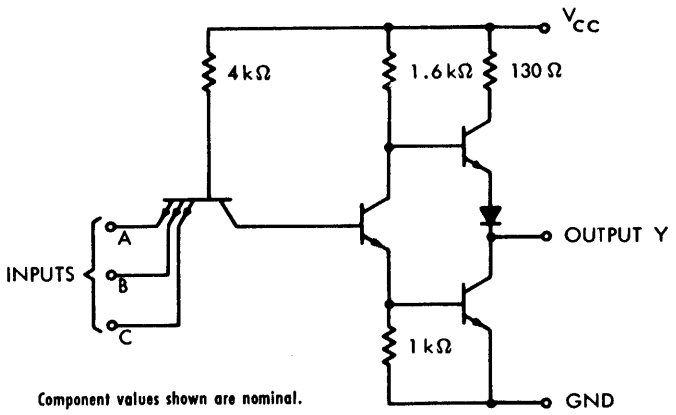
4.1.2 585008, TRIPLE 3-INPUT NAND GATE PACKAGE

Figure 4.2 shows the pin arrangement, logic, and a representative circuit schematic of this package.

PIN ARRANGEMENT (TOP VIEW)



REPRESENTATIVE SCHEMATIC (EACH GATE)



LOGIC (EACH GATE)

$$Y = \overline{A\ B\ C}$$

Figure 4.2 585008, Triple 3-Input NAND Gate Package.

4.1.3 585009, DUAL 4-INPUT NAND GATE PACKAGE

Figure 4.3 shows the pin arrangement, logic, and a representative circuit schematic of this package.

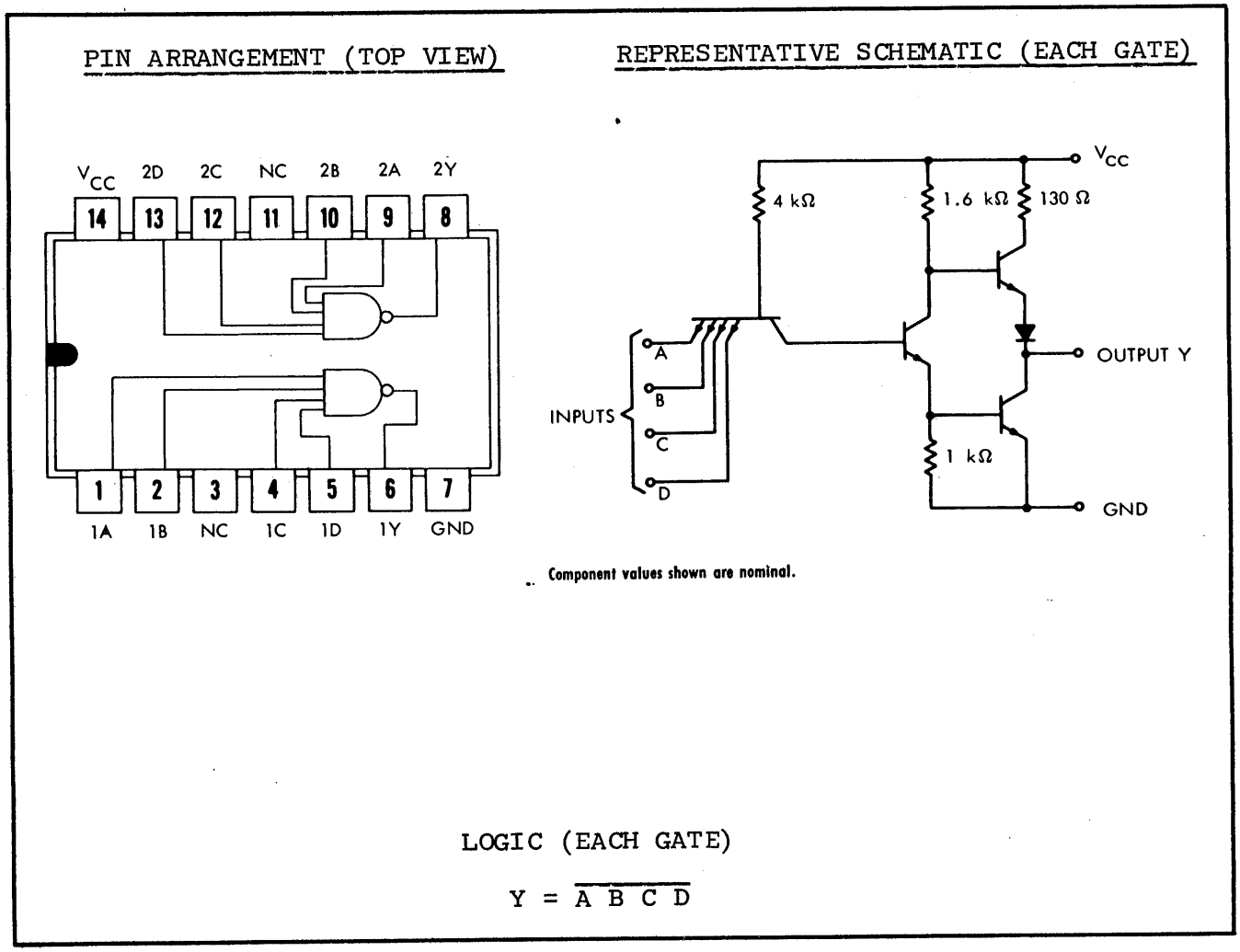


Figure 4.3 585009, Dual 4-Input NAND Gate Package.

4.1.4 585010, SINGLE 8-INPUT NAND GATE PACKAGE

Figure 4.4 shows the pin arrangement, logic, and a representative circuit schematic of this package.

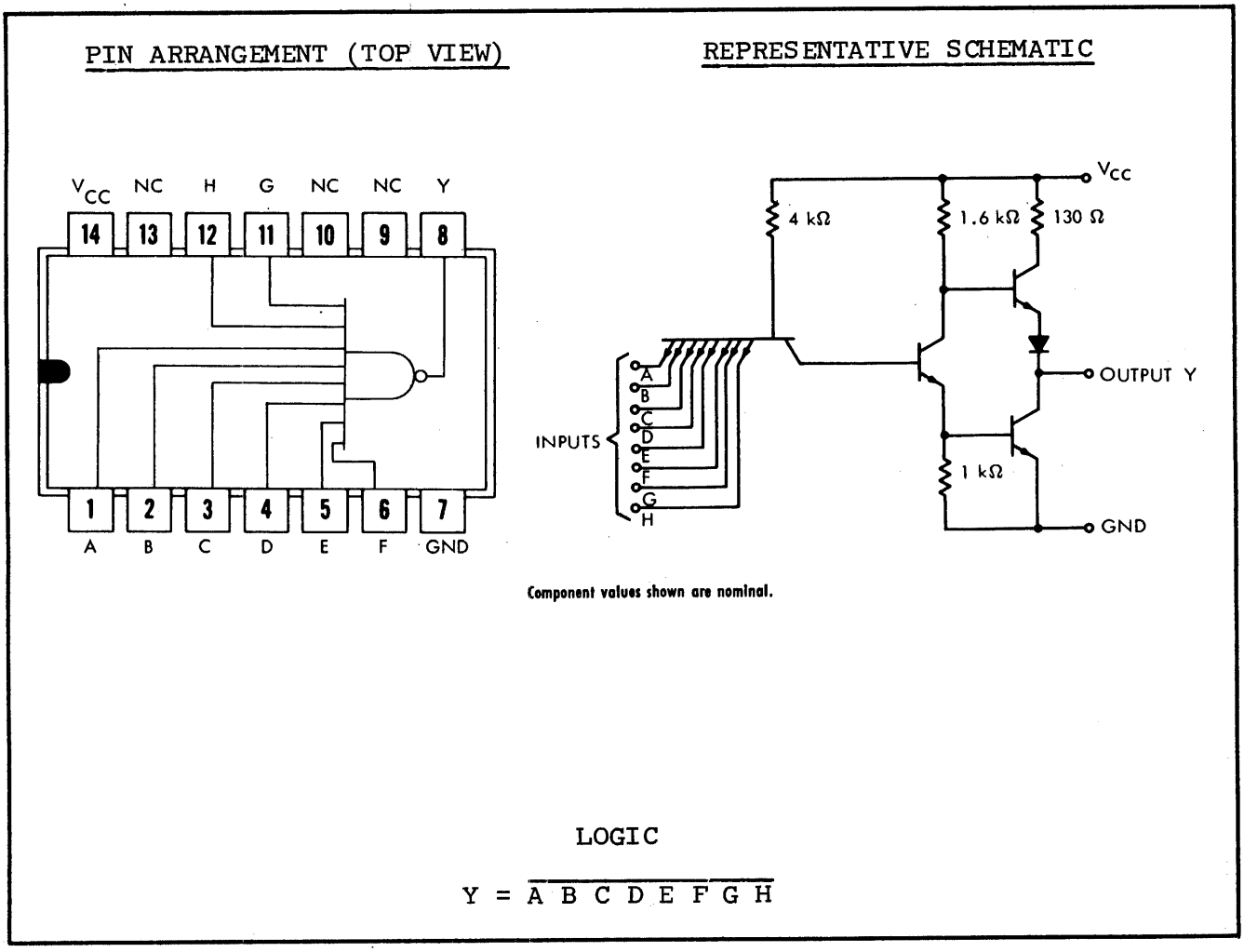


Figure 4.4 585010, Single 8-Input NAND Gate Package.

4.1.5 585011, DUAL 4-INPUT NAND BUFFER PACKAGE

Figure 4.5 shows the pin arrangement, logic, and a representative circuit schematic of this package. The reason for calling the individual gates of this package "buffers" is to indicate that they have a greater power output than those gates not so designated.

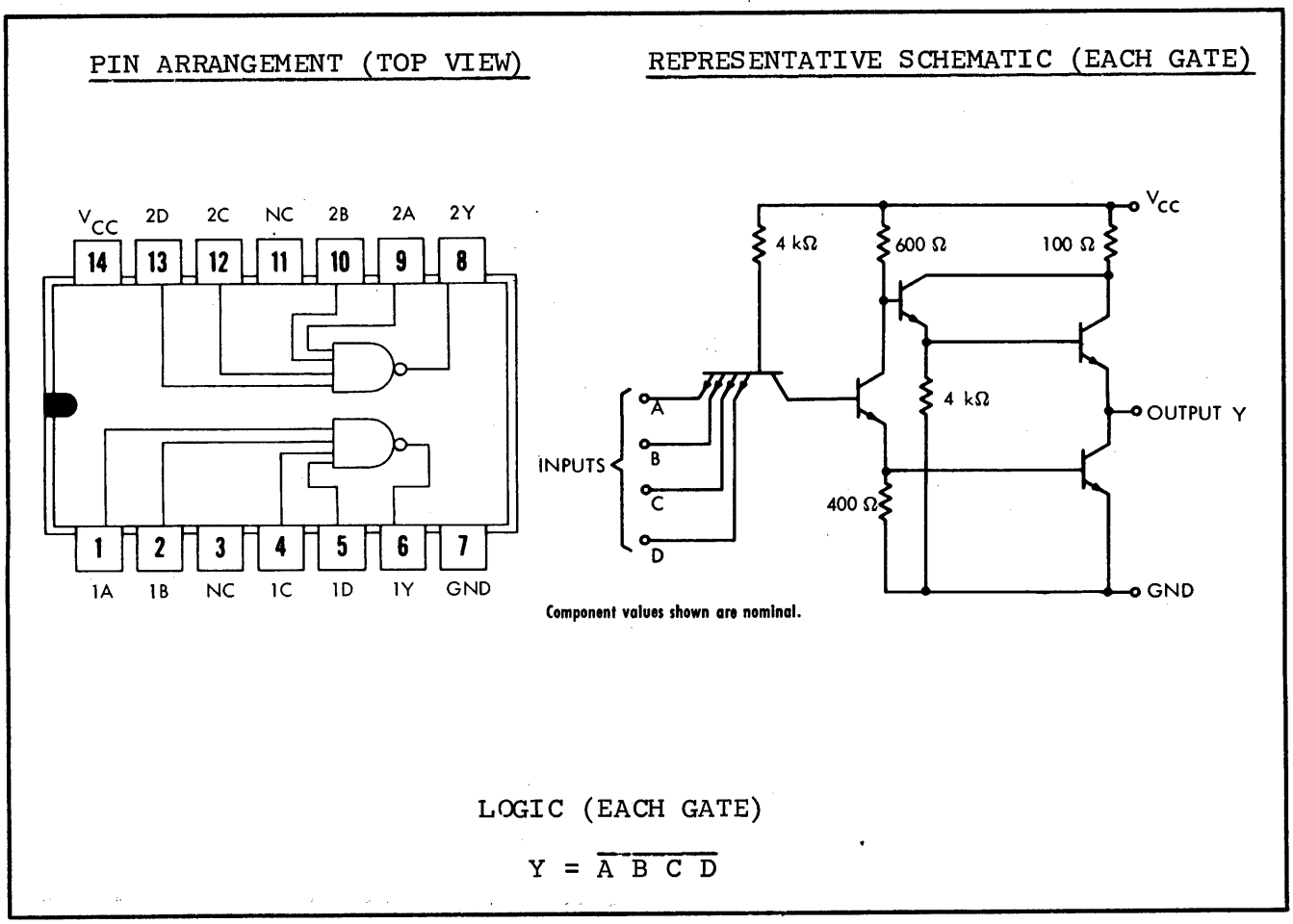
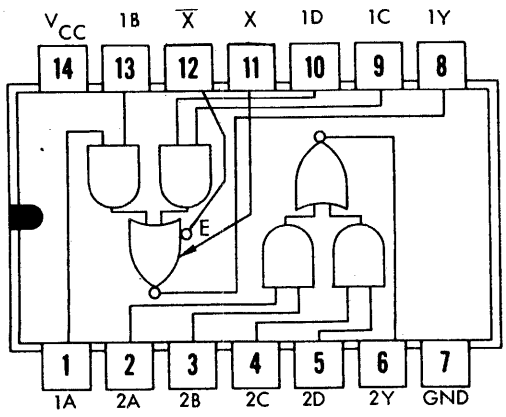


Figure 4.5 585011, Dual 4-Input NAND Buffer Package.

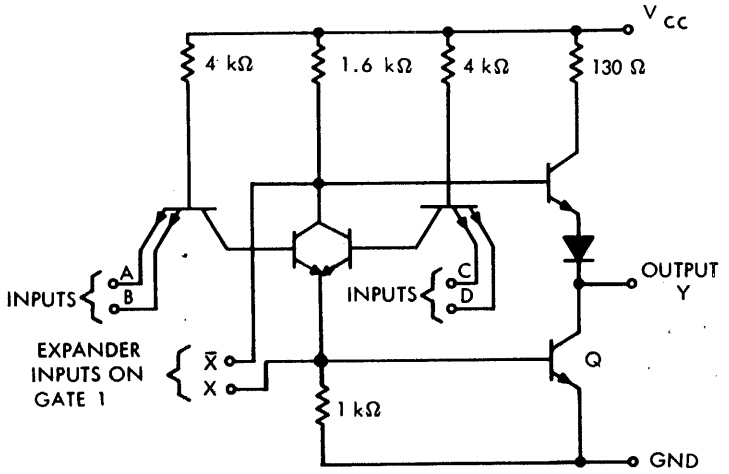
4.1.6 585012, DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE PACKAGE

Figure 4.6 shows the pin arrangement, logic, and a representative circuit schematic of this package.

PIN ARRANGEMENT (TOP VIEW)



REPRESENTATIVE SCHEMATIC (EACH GATE)



Component values shown are nominal.

LOGIC (EACH GATE)

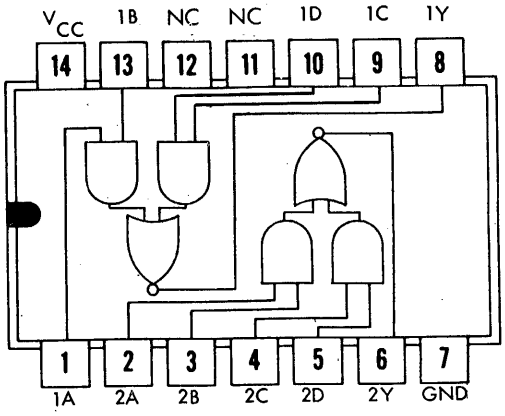
$$Y = \overline{(A\ B)\ v\ (C\ D)\ v\ X}$$

Figure 4.6 585012, Dual 2-Wide 2-Input AND-OR-Invert Gate Package.

4.1.7 585013, DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE PACKAGE

Figure 4.7 shows the pin arrangement, logic, and a representative circuit schematic of this package.

PIN ARRANGEMENT (TOP VIEW)



LOGIC (EACH GATE)

$$Y = \overline{(A\ B)\ v\ (C\ D)}$$

REPRESENTATIVE SCHEMATIC (EACH GATE)

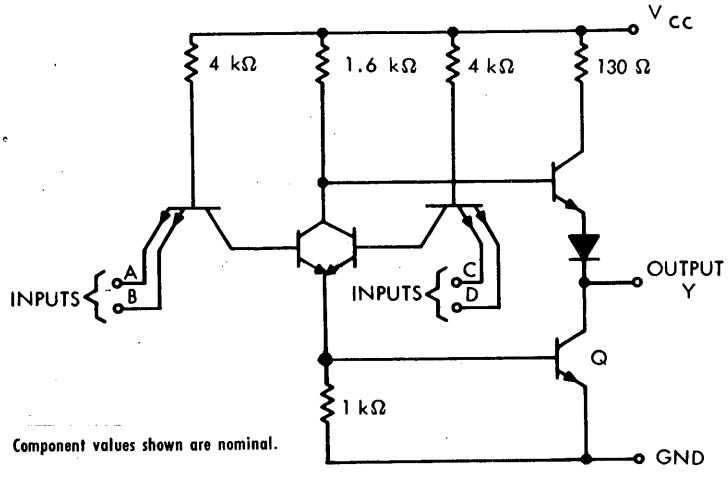


Figure 4.7 585013, Dual 2-Wide 2-Input AND-OR-Invert Gate Package.

4.1.8 585014, 4-WIDE 2-INPUT AND-OR-INVERT GATE PACKAGE

Figure 4.8 shows the pin arrangement, logic, and a representative circuit schematic of this package.

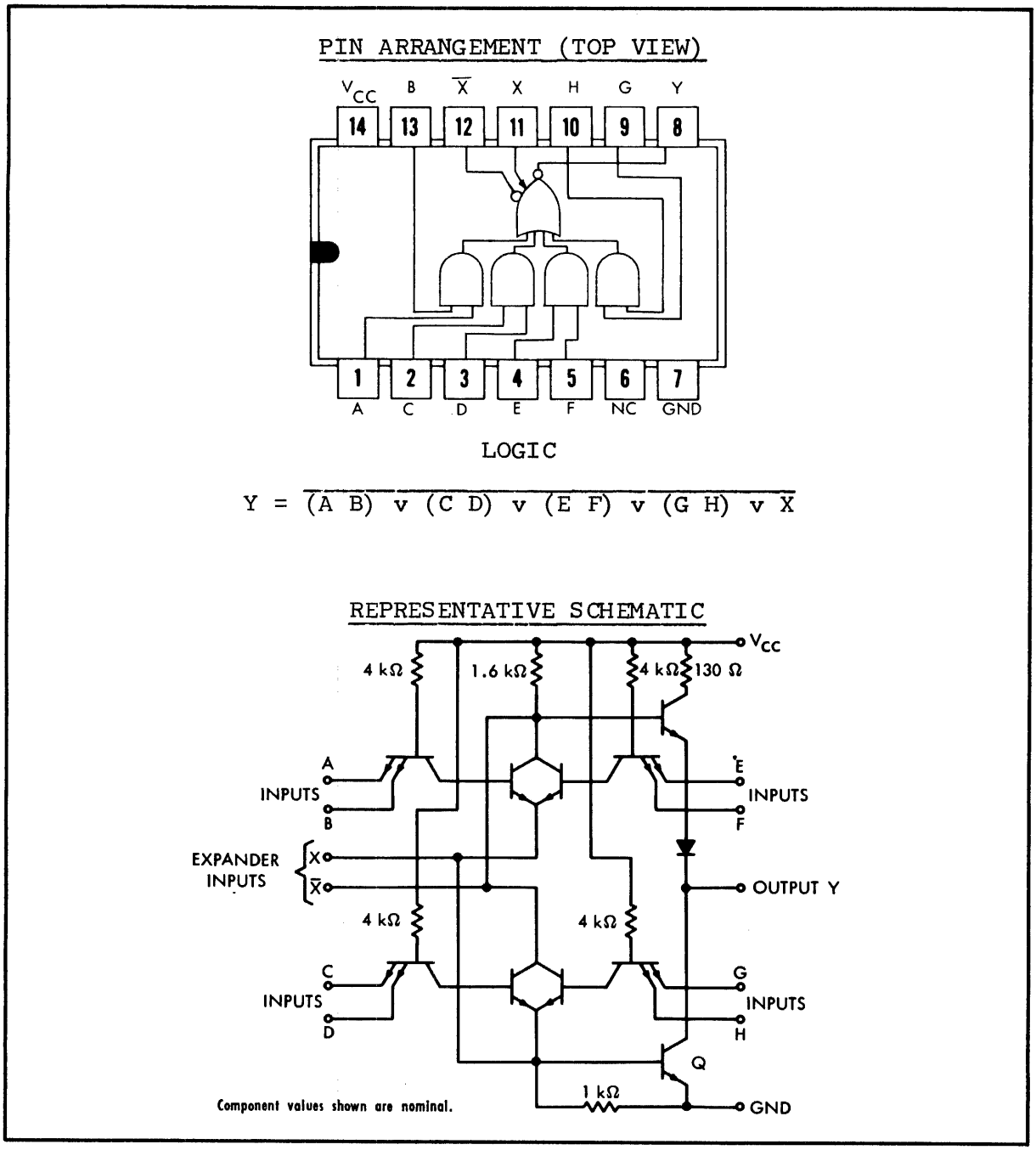


Figure 4.8 585014, 4-Wide 2-Input AND-OR-Invert Gate Package.

4.1.9 585015, 4-WIDE 2-INPUT AND-OR-INVERT GATE PACKAGE.

Figure 4.9 shows the pin arrangement, logic, and a representative circuit schematic of this package.

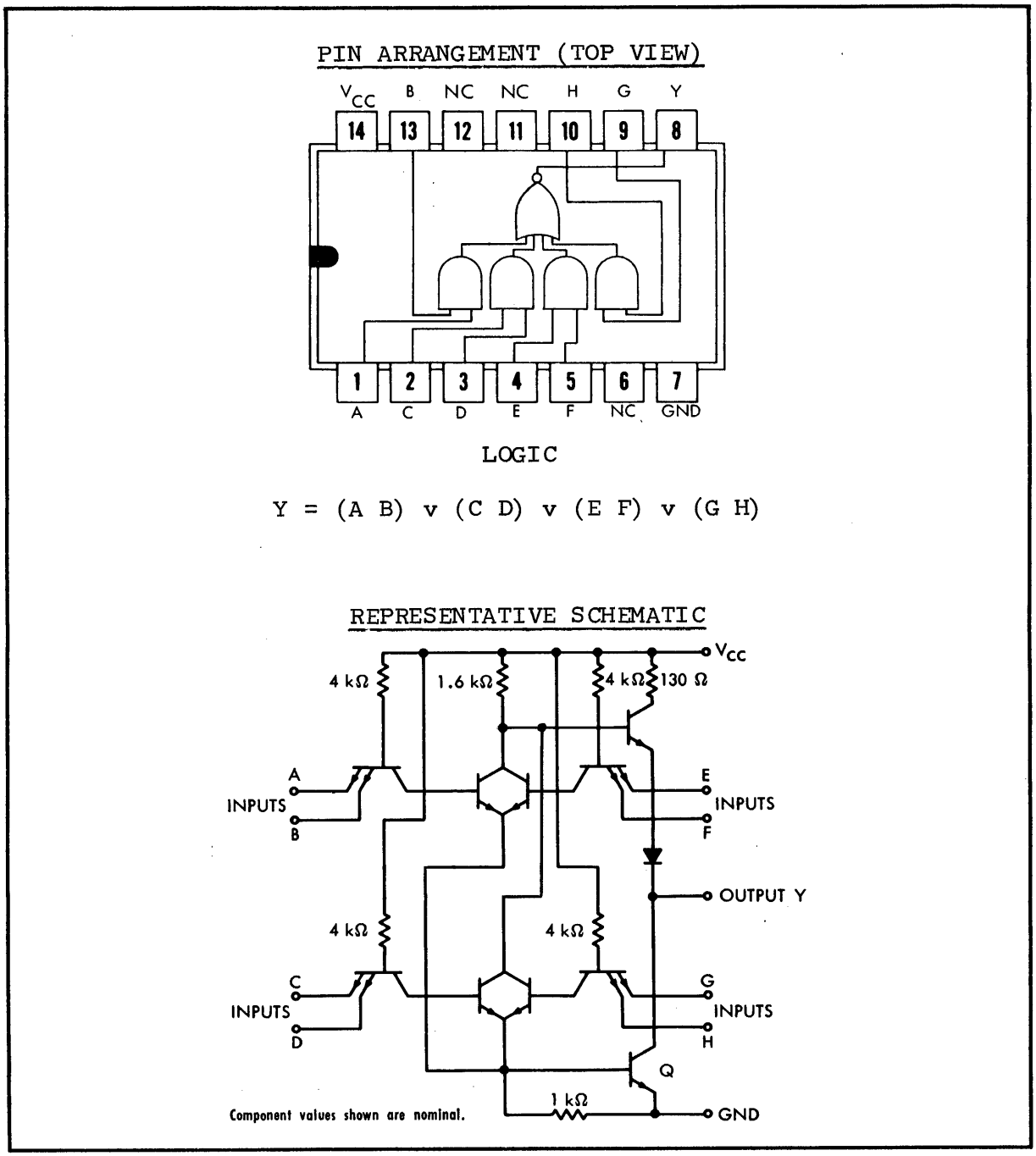


Figure 4.9 585015, 4-Wide 2-Input AND-OR-Invert Gate Package.

4.1.10 585016, DUAL 4-INPUT EXPANDER PACKAGE

Figure 4.10 shows the pin arrangement, logic, and a representative circuit schematic of this package.

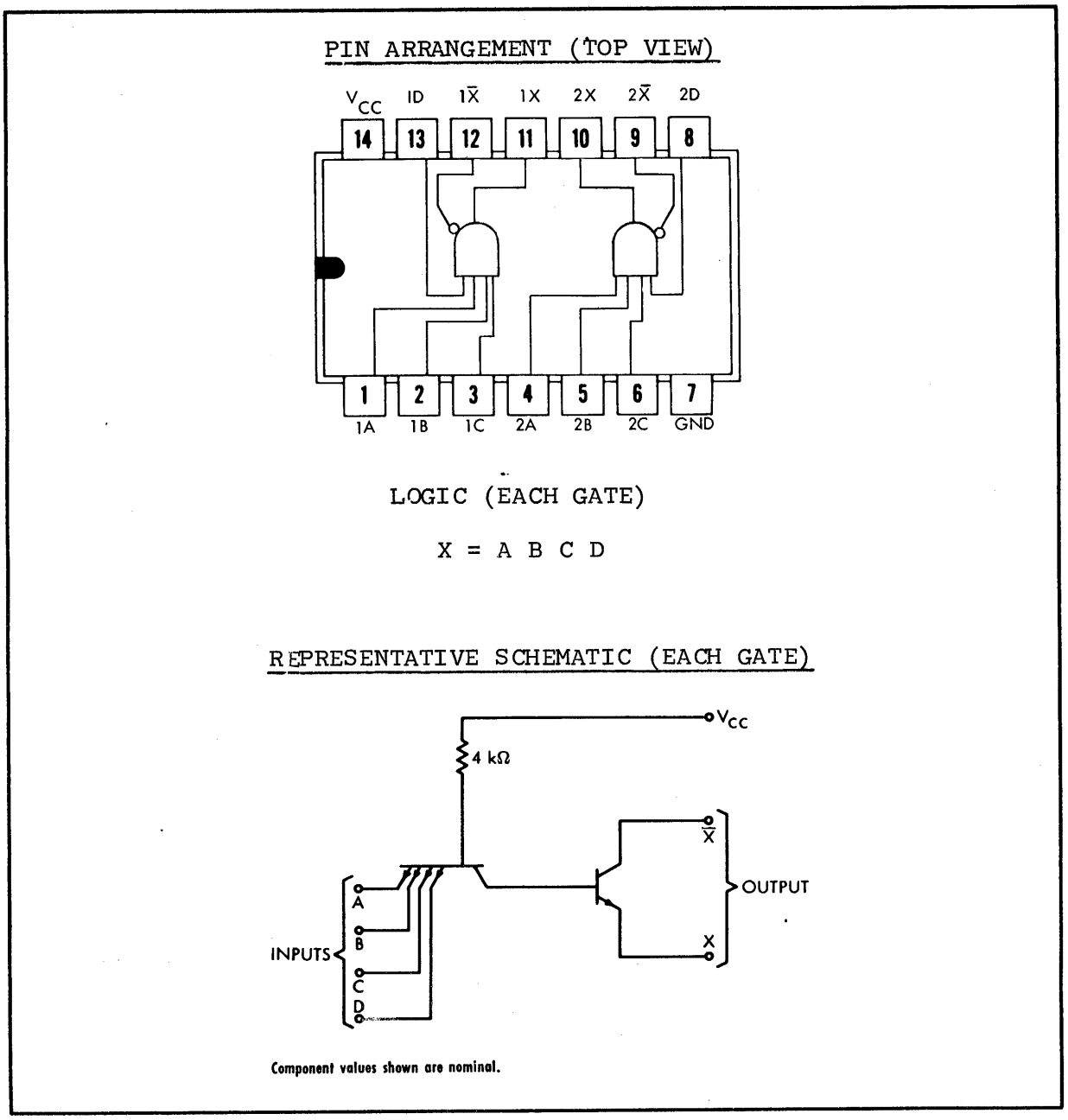


Figure 4.10 585016, Dual 4-Input Expander Package.

4.1.11 585017, JK MASTER-SLAVE FLIPFLOP PACKAGE

Figure 4.11 shows the pin arrangement, truth table, and clock waveform of this package. Figure 4.12 shows a functional block diagram and a representative circuit schematic.

NOTE: In Order to facilitate drawing of the pin arrangement shown in figure 4.11, the clock input is not drawn in its standard position.

This JK flipflop is based on the master-slave principle, discussed below, and has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. Both the clear and preset inputs are independent of the clock and override the JK inputs. The master-slave principle considers the single flipflop to theoretically contain 2 flipflops, a master flipflop and a slave flipflop, which are coupled together. The operations of these 2 flipflops is as follows (keyed to the clock waveform of figure 4.11):

1. Isolate slave from master.
2. Enter information from AND gate inputs to master.
3. Disable AND gate inputs.
4. Transfer information from master to slave *information then appears on outputs).

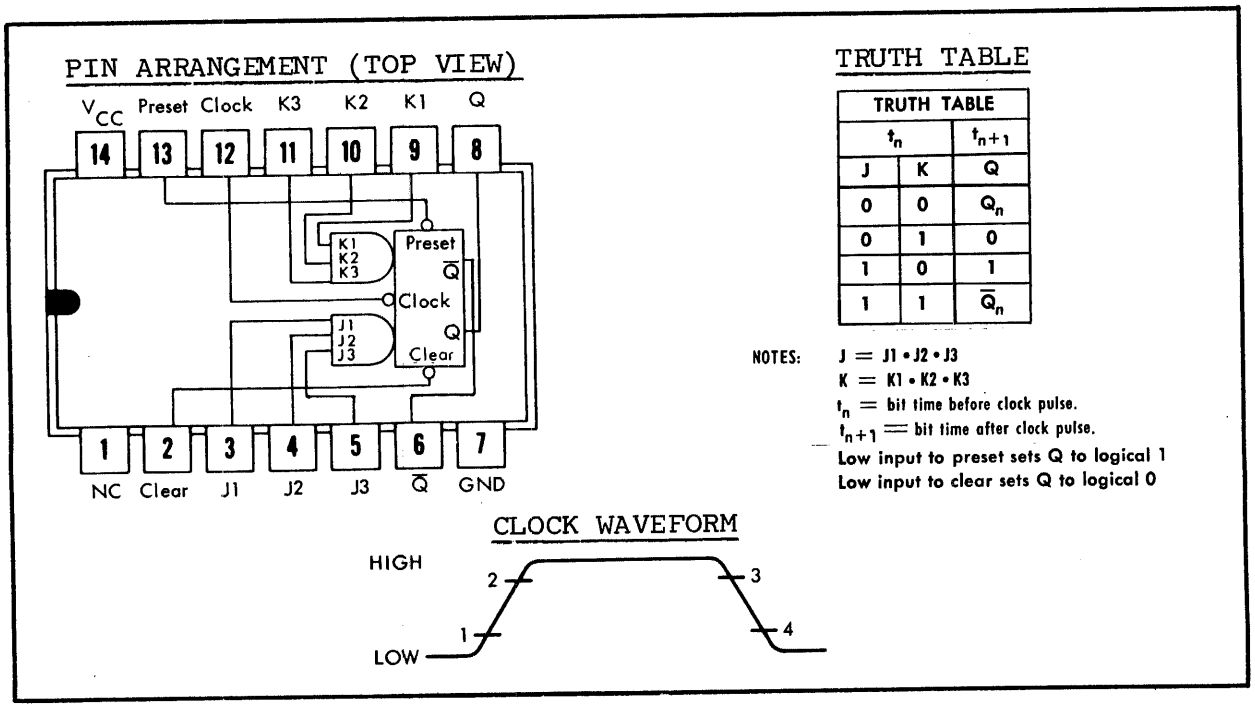


Figure 4.11 585017, JK Master-Slave Flipflop Package.

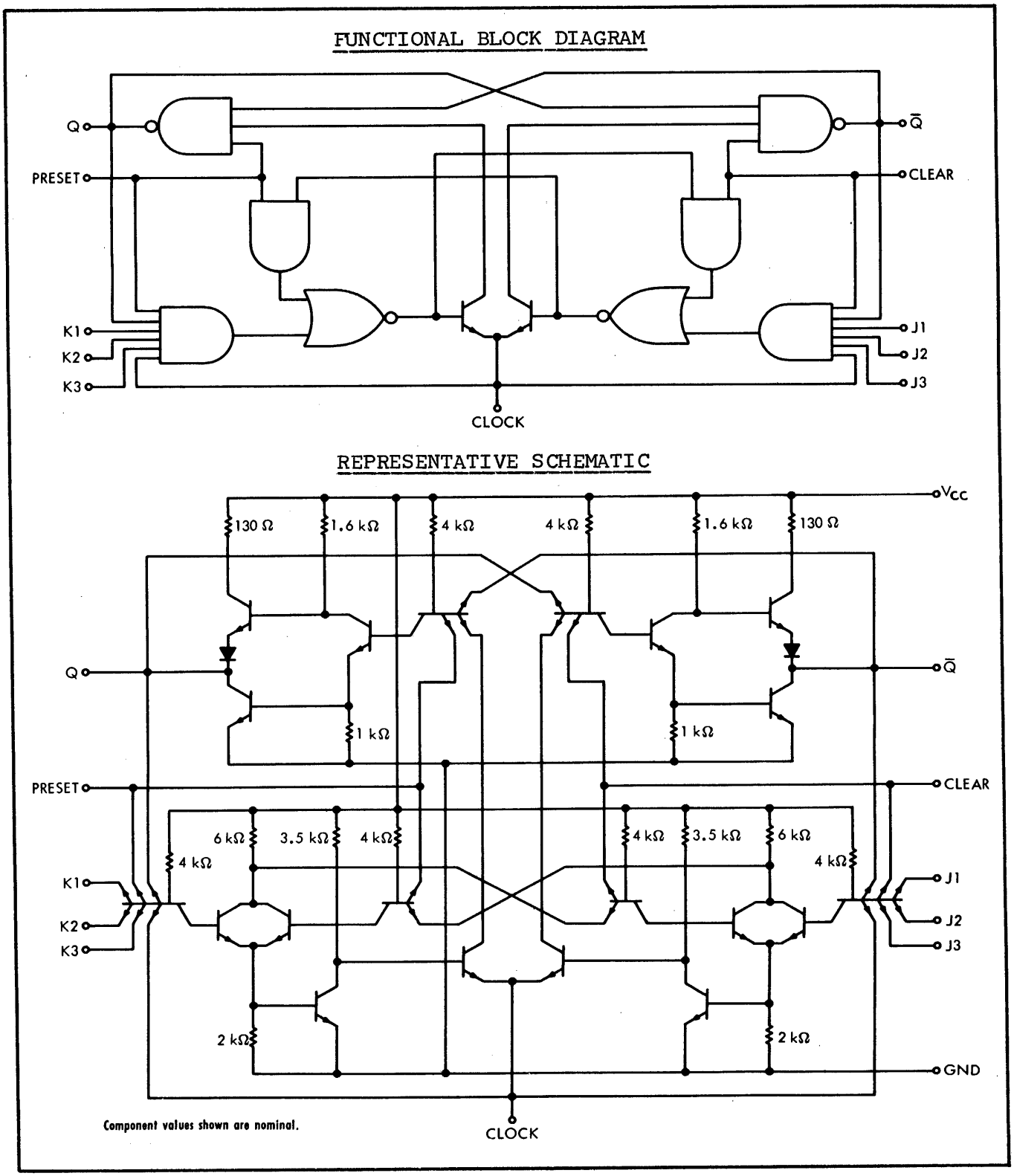
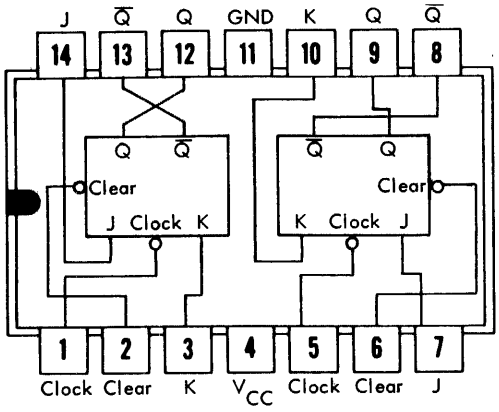


Figure 4.12 585017, JK Master-Slave Flipflop Package.

4.1.12 585018 DUAL JK MASTER-SLAVE FLIPFLOP PACKAGE

Figure 4.13 shows the pin arrangement and truth table for this package. Figure 4.14 shows a functional block diagram and a representative circuit schematic. The flipflops of this package function as described in paragraph 4.1.11.

PIN ARRANGEMENT (TOP VIEW)



TRUTH TABLE (EACH FLIPFLOP)

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.
Low input to clear sets Q to logical 0 regardless of clock state.

Figure 4.13 585018, Dual JK Master-Slave Flipflop Package.

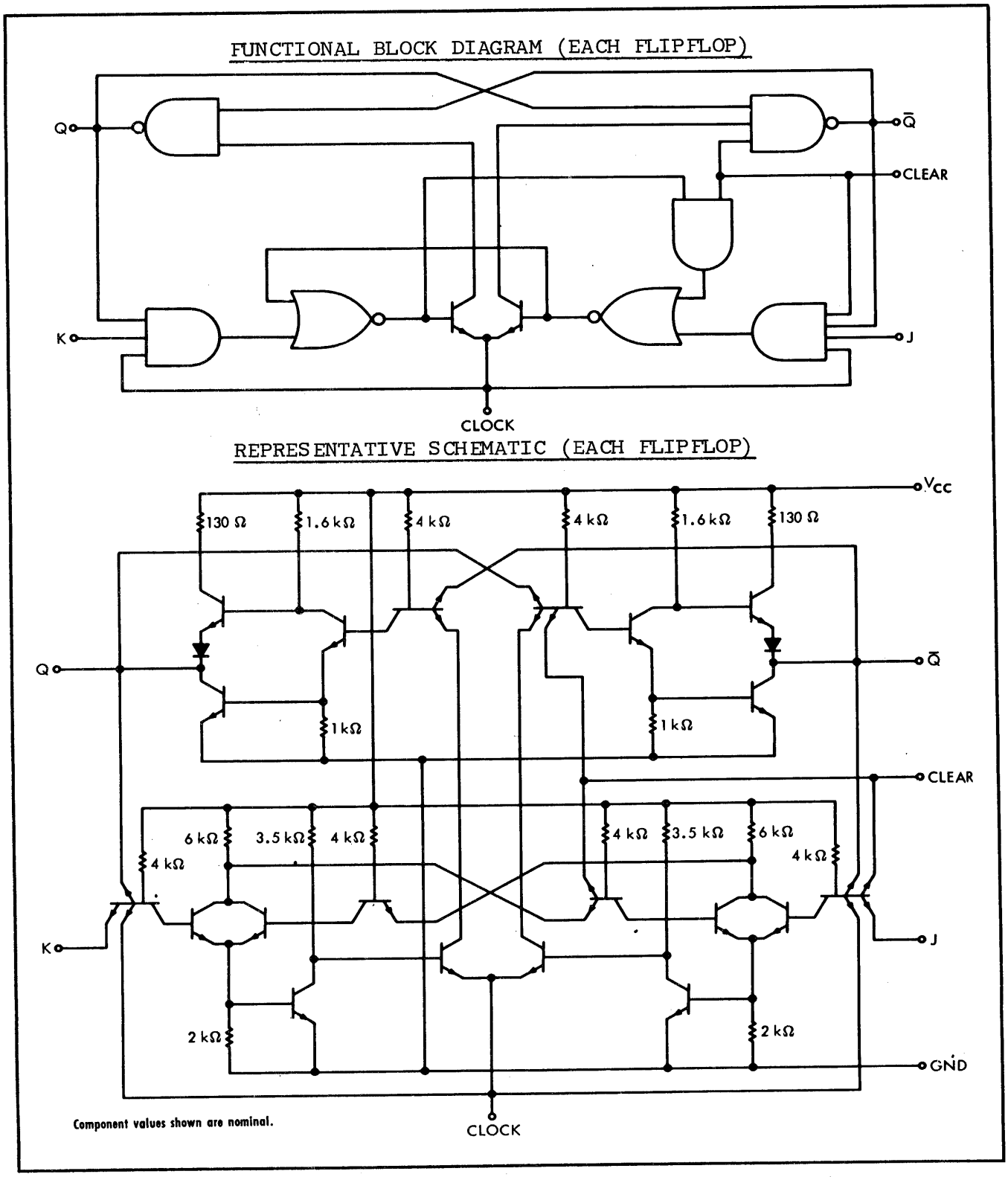


Figure 4.14 585018, Dual JK Master-Slave Flipflop Package.

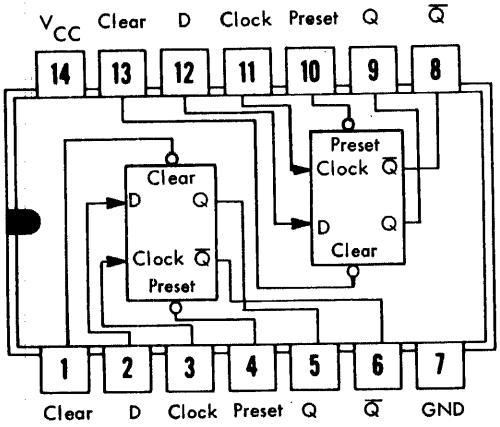
4.1.13 585019, DUAL D-TYPE EDGE-TRIGGERED FLIPFLOP PACKAGE

Figure 4.15 shows the pin arrangement and truth table for this package. Figure 4.16 shows a functional block diagram and a representative circuit schematic.

NOTE: In order to facilitate drawing of the pin arrangement shown in figure 4.15, the clock input is not drawn in its standard position.

Input information is transferred to the Q and $\overline{Q}$ outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the clock input threshold voltage has been passed the data input (D) is locked out. Both the clear and preset inputs are independent of the clock and override the D input.

PIN ARRANGEMENT (TOP VIEW)



TRUTH TABLE (EACH FLIPFLOP)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
0	0	1
1	1	0

NOTES: t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.
Low input to clear sets Q to logical 0.
Low input to preset sets Q to logical 1.

Figure 4.15 585019, Dual D-Type Edge-Triggered Flipflop Package.

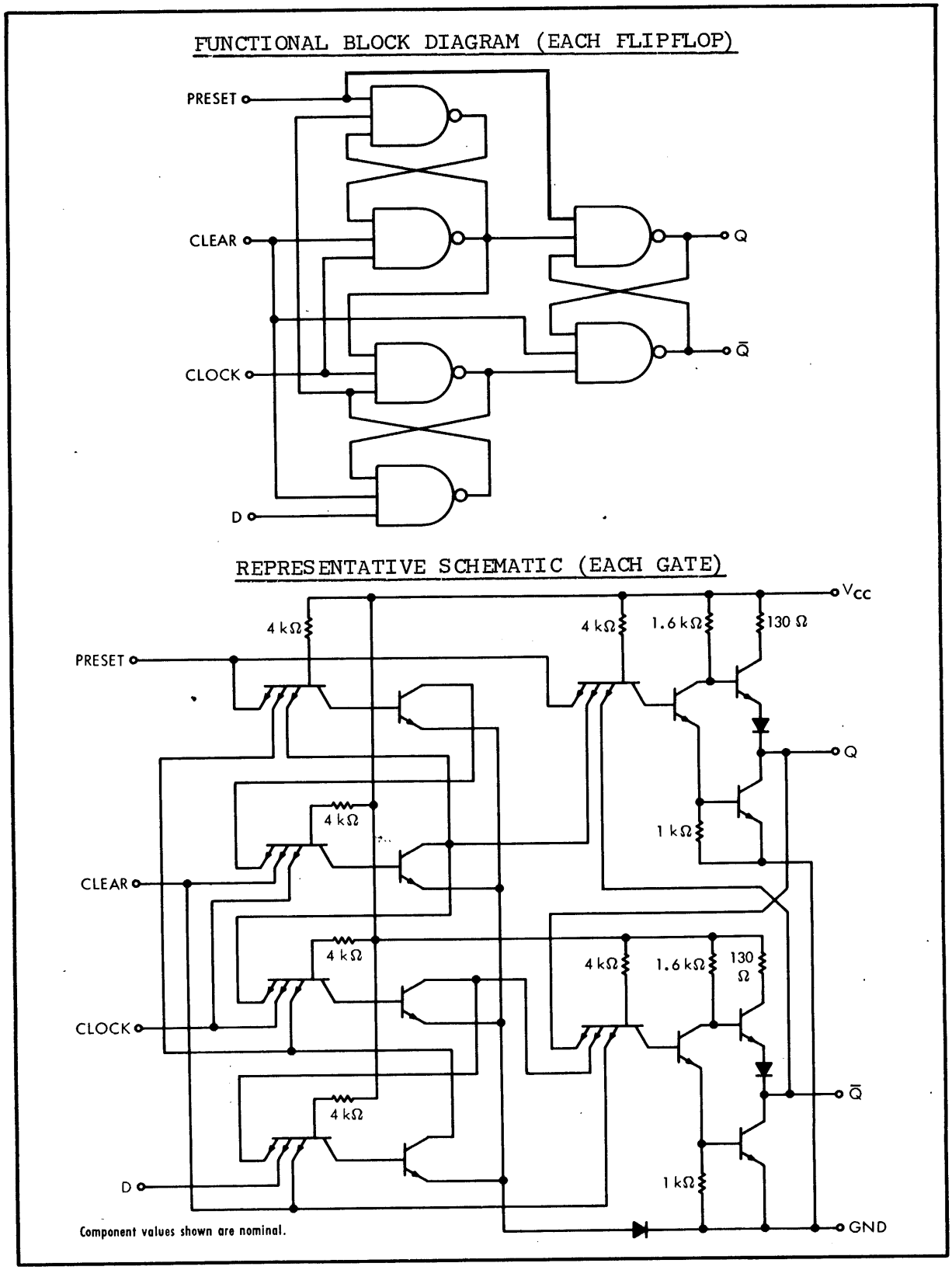


Figure 4.16 585019, Dual D-Type Edge-Triggered Flipflop Package.

4.1.14 585020, 8-BIT SHIFT REGISTER PACKAGE

Figure 4.17 shows the pin arrangement, truth table, and typical input/output waveforms of this package.

NOTE: In order to facilitate drawing of the pin arrangement shown in figure 4.17, the clock input is not drawn in its standard position.

The shift register is a serial-in, serial-out, 8-bit shift register composed of 8 RS master-slave flipflops (master-slave flipflops are discussed in paragraph 4.1.11). Though the register has a 2-input AND gate input, the 2 inputs are externally connected together in the processor so that only the first and last conditions of the truth table pertain to the use of this register.

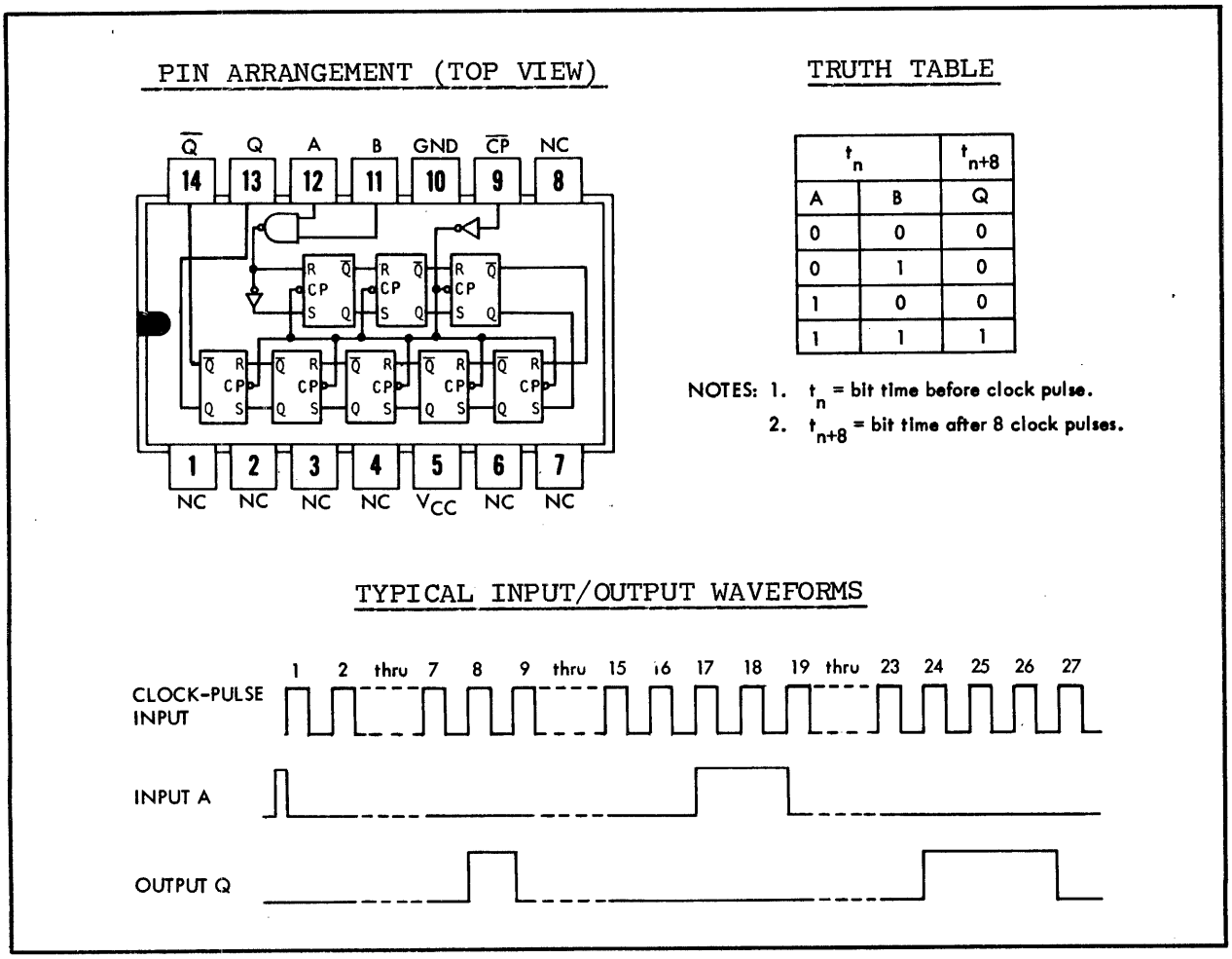
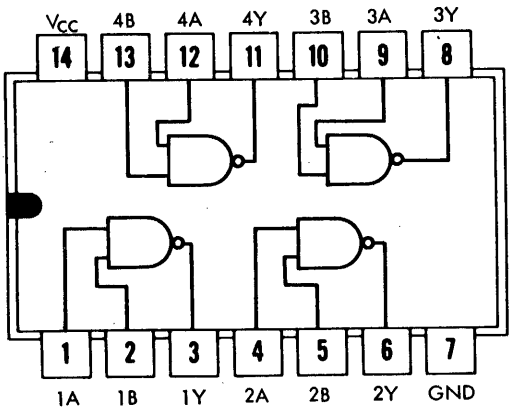


Figure 4.17 585020, 8-Bit Shift Register Package.

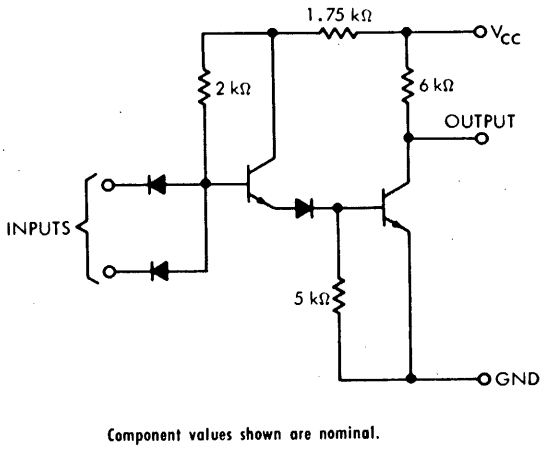
4.1.15 585021, QUADRUPLE 2-INPUT NAND GATE PACKAGE

Figure 4.18 shows the pin arrangement, logic, and a representative circuit schematic of this package.

PIN ARRANGEMENT (TOP VIEW)



REPRESENTATIVE SCHEMATIC



Component values shown are nominal.

LOGIC

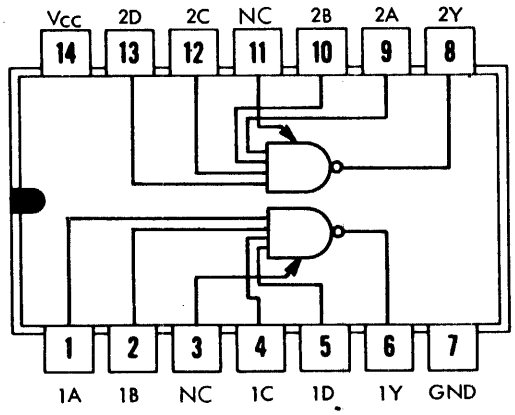
$$Y = \overline{A\ B}$$

Figure 4.18 585021, Quadruple 2-Input NAND Gate Package.

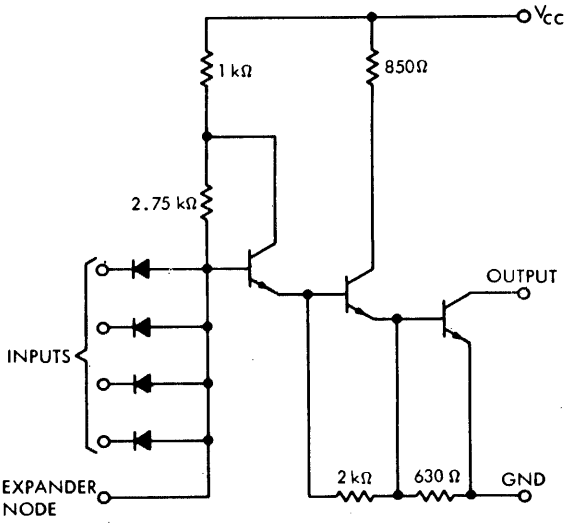
4.1.16 585022, DUAL 4-INPUT NAND GATE PACKAGE

Figure 4.19 shows the pin arrangement, logic, and a representative circuit schematic of this package.

PIN ARRANGEMENT (TOP VIEW)



REPRESENTATIVE SCHEMATIC



Component values shown are nominal.

LOGIC

$$Y = \overline{A\ B\ C\ D}$$

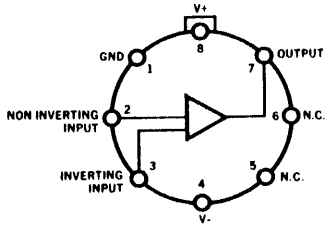
Figure 4.19 585022, Dual 4-Input NAND Gate Package.

4.1.17 585023, DIFFERENTIAL COMPARATOR PACKAGE

Figure 4.20 shows the pin arrangement and a representative circuit schematic of this package. This package is used in the processor's playback amplifiers as a high-noise immunity memory sense amplifier. It's operation is discussed as part of the playback amplifier discussion.

PIN ARRANGEMENT (TOP VIEW)

TO-5 CONNECTION DIAGRAM
(TOP VIEW)



Note: Pin 4 connected to case

REPRESENTATIVE SCHEMATIC

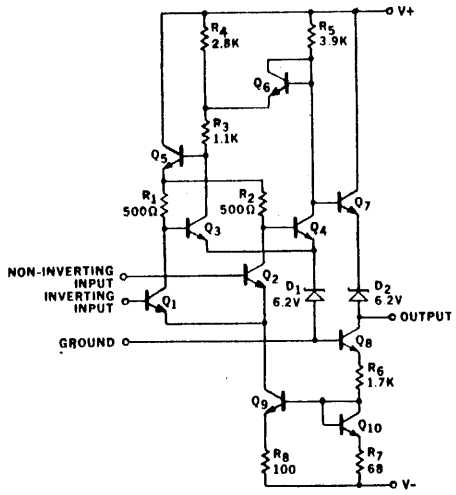


Figure 4.20 585023, Differential Comparator Package.

4.2 DISCRETE CIRCUITS

Each of the processor's discrete component circuits is discussed in this section. Each circuit discussion is accompanied by a schematic diagram of the circuit. Multiple circuits which are identical are portrayed by one schematic diagram which contains special component and connector designations. These designations are used to determine, from a table accompanying the schematic, the actual component designations and connectors for each of the multiple circuits. The location code of each component is prefixed to the component designation given in the table. The use of the location code prefix is discussed in paragraph 1.7. The table also gives the location code of each test point in the circuit.

Unless otherwise specified, all voltage and current values given in the text of this chapter are approximations. All voltages are with respect to signal ground, unless otherwise mentioned. Input and output levels are expressed as no-load voltages.

4.2.1 I/O CIRCUITS

The 2 voltage divider circuits shown in figure 4.21 supply the I/O circuits with a Zener-regulated -6 volts and a non-regulated -12 volts bias.

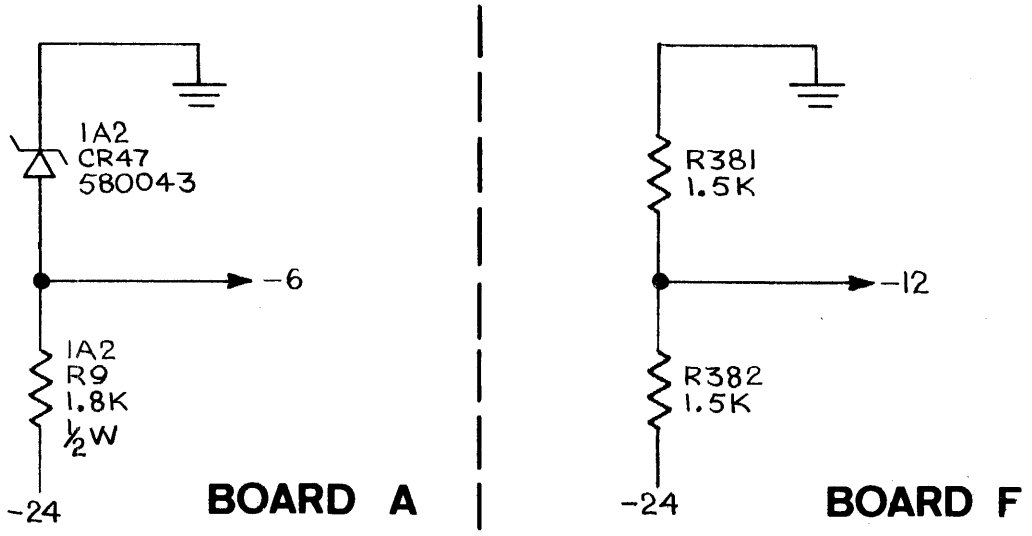


Figure 4.21 Voltage Dividers, I/O Circuits.

4.2.1.1 Input Circuits IB101 - Ib107

The Ib101 - Ib107 circuits, see figure 4.22 and table 4.1, perform 3 functions. They filter, power amplify, and level shift input signals Ib1 - Ib7 from their interface logic level (-10 volts nominally equals logical 0, 0 volts nominally equals logical 1) to the processor logic

level (0 volts nominally equals logical 0, +5 volts nominally equals logical 1) of signals Ib101 - Ib107.

The junction of Ra and Rc is pulled to -12 volt (logical 0) when the data source does not supply input drive. Rb, Ca, and Rd form a high-frequency filter to reduce noise at the base of Qa. The base-emitter junction of Qb is normally forward biased, placing the Qa-Qb emitter junction at -6.6 volts. Since the Ra, Rc junction is at -12 volts, the base-emitter junction of Qa is reverse biased. Qb remains forward biased and its collector tries to go negative. CRa, however, becomes forward biased and clamps the appropriate signal (Ib101 - Ib107) to ground (logical 0).

When the data source drives the Ra, Rc junction to ground (logical 1), Qa is turned on and the Qa, Qb emitter junction is forced positive with respect to the base of Qb. Qb is turned off and the appropriate output signal is pulled to +5 volts (logical 1) through Rf. CRa is reverse biased.

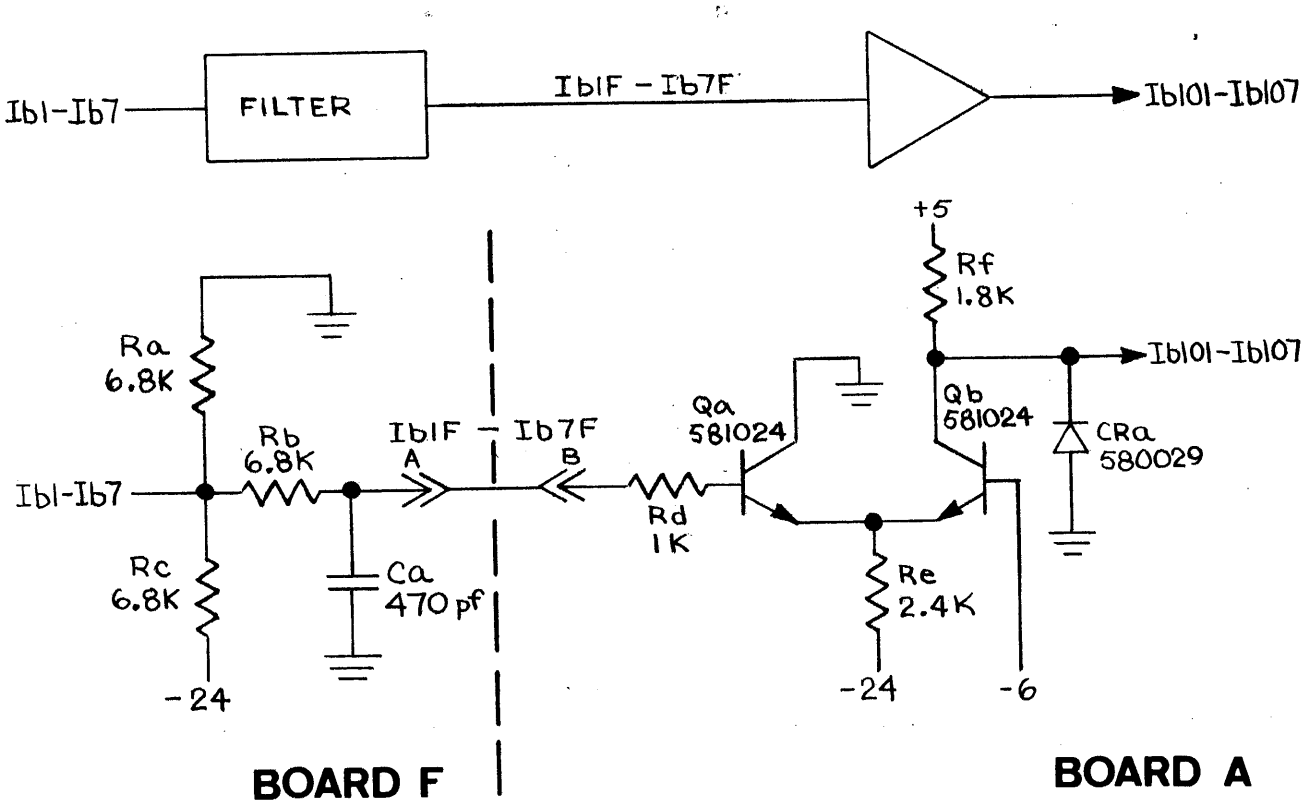


Figure 4.22 Input Circuits Ib101 - Ib107.

4.2.1.2 Input Circuit Ib108 and $\overline{K73}$

The operation of this circuit, shown in figure 4.23, for Ib108 is identical to the operation of circuits Ib101 - Ib107, discussed in the previous paragraph. The operation of $\overline{K73}$ is similar to the operation of Ib108 except that $\overline{K73}$ is the inverse of Ib108. This is because when Ib8 is at -12 volts (logical 0), the base-emitter junction of Q27 is reverse biased, Q27 is turned off, and $\overline{K73}$ is pulled to +5 volts (logical 1) through R54. CR14 is reversed biased in this case. When $\overline{Ib8}$ is driven to ground (logical 1), Q27 is turned on and CR14 clamps $\overline{K73}$ to ground (logical 0). CR13 prevents the base of Q27 from going above ground.

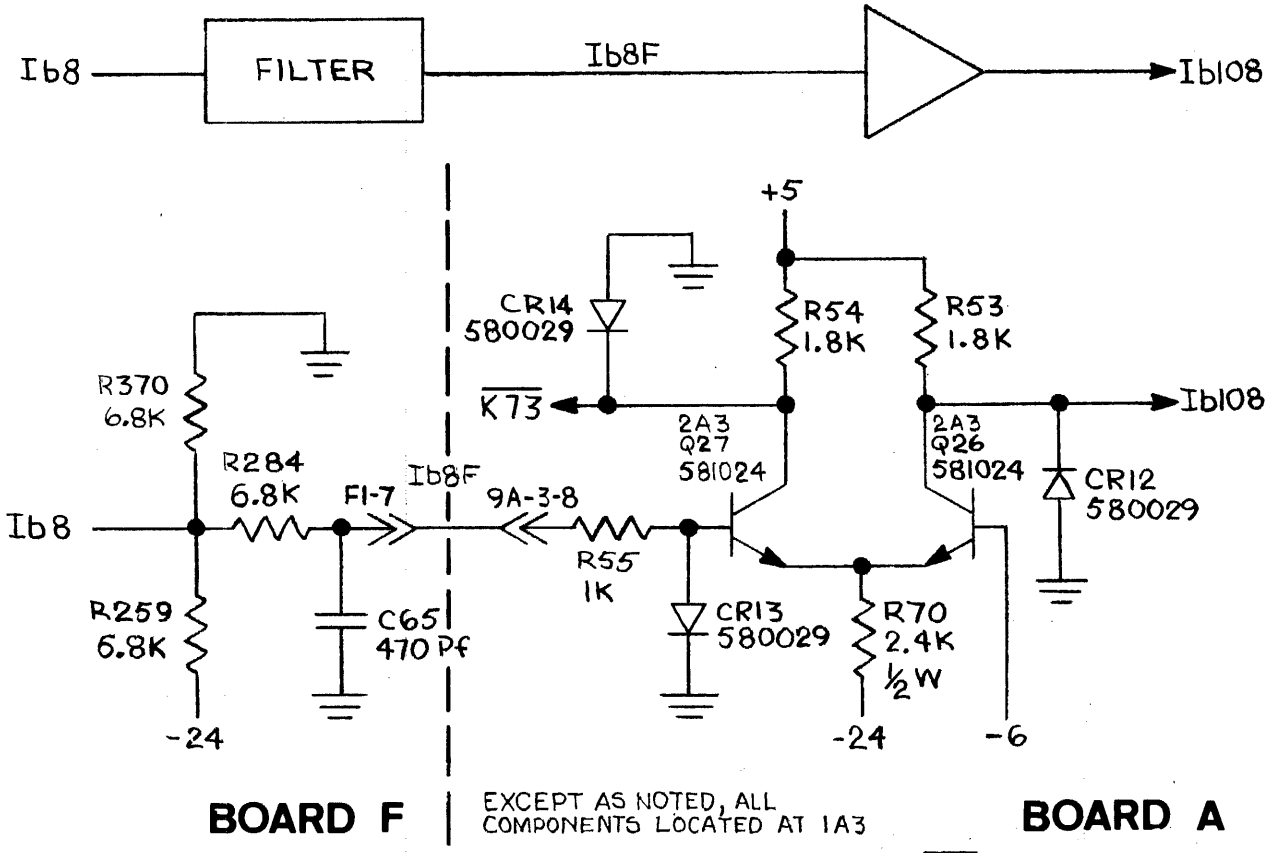


Figure 4.23 Input Circuits Ib108 and $\overline{K73}$.

4.2.1.3 Input Circuit $\overline{K75}$

This circuit, shown in figure 4.24, serves as a filter, power amplifier/inverter, and shifts the interface logic level (nominally -14 volts = logical 0, 0 volts = logical 1) to the processor logic level (0 volts = logical 0, +5 volts = logical 1) of the K75, Input Busy, signal. It also performs the additional function of forcing $\overline{K75}$ low (selected input device is busy) whenever there are no input devices attached to the processor so that the processor can recognize this condition.

	SCHEMATIC LABEL	INDIVIDUAL CIRCUITS						
		Ib101	Ib102	Ib103	Ib104	Ib105	Ib106	Ib107
COMPONENT	Ca	C66	C67	C68	C69	C70	C71	C72
	CRa	2A3CR11	3A3CR10	4A3CR9	4A3CR8	5A3CR7	5A3CR6	6A3CR5
	Qa	2A3Q28	3A3Q29	3A3Q30	4A3Q31	5A3Q32	5A3Q33	6A3Q34
	Qb	2A3Q25	3A3Q24	3A3Q23	4A3Q22	5A3Q21	5A3Q20	6A3Q19
	Ra	R371	R372	R373	R374	R375	R376	R377
	Rb	R285	R286	R287	R288	R289	R290	R291
	Rc	R260	R261	R262	R263	R264	R265	R266
	Rd	2A3R56	3A3R57	4A3R58	4A3R59	5A3R60	5A3R61	6A3R62
	Re	2A3R69	3A3R68	4A3R67	4A3R66	5A3R65	5A3R64	6A3R63
	Rf	2A3R52	3A3R51	4A3R50	4A3R49	5A3R48	5A3R47	6A3R46
CONNECTOR	A	F1-3	F1-9	F1-10	F1-11	F1-12	F1-13	F1-14
	B	9A-3-1	9A-3-2	9A-3-3	9A-3-4	9A-3-5	9A-3-6	9A-3-1

Table 4.1 Input Circuits Ib101 - Ib107.

Rev.18NOV68

R283, C74, and R5 form a high-frequency filter to reduce noise at the base of Q17. CR88 prevents the junction of itself and R283 from going more negative than -12 volts. CR4 prevents the base of Q17 from going positive. When the selected input device(s) is not busy the base-emitter junction of Q15 is forward biased, placing emitter of Q17 at -6 volts. K75 is at -10 volts (logical 0). The base-emitter junction of Q17 is reverse biased, keeping it off. $\overline{K75}$ is pulled to +5 volts (logical 1) through R4. CR2 is reverse biased. When either no input devices are attached to the processor (no data source) or when a selected input device is busy, K75 is pulled positive by the +18 volt supply through R268. The base-emitter junction of Q17 is forward biased, turning Q17 on and Q15 off. CR2 clamps $\overline{K75}$ to ground (logical 0).

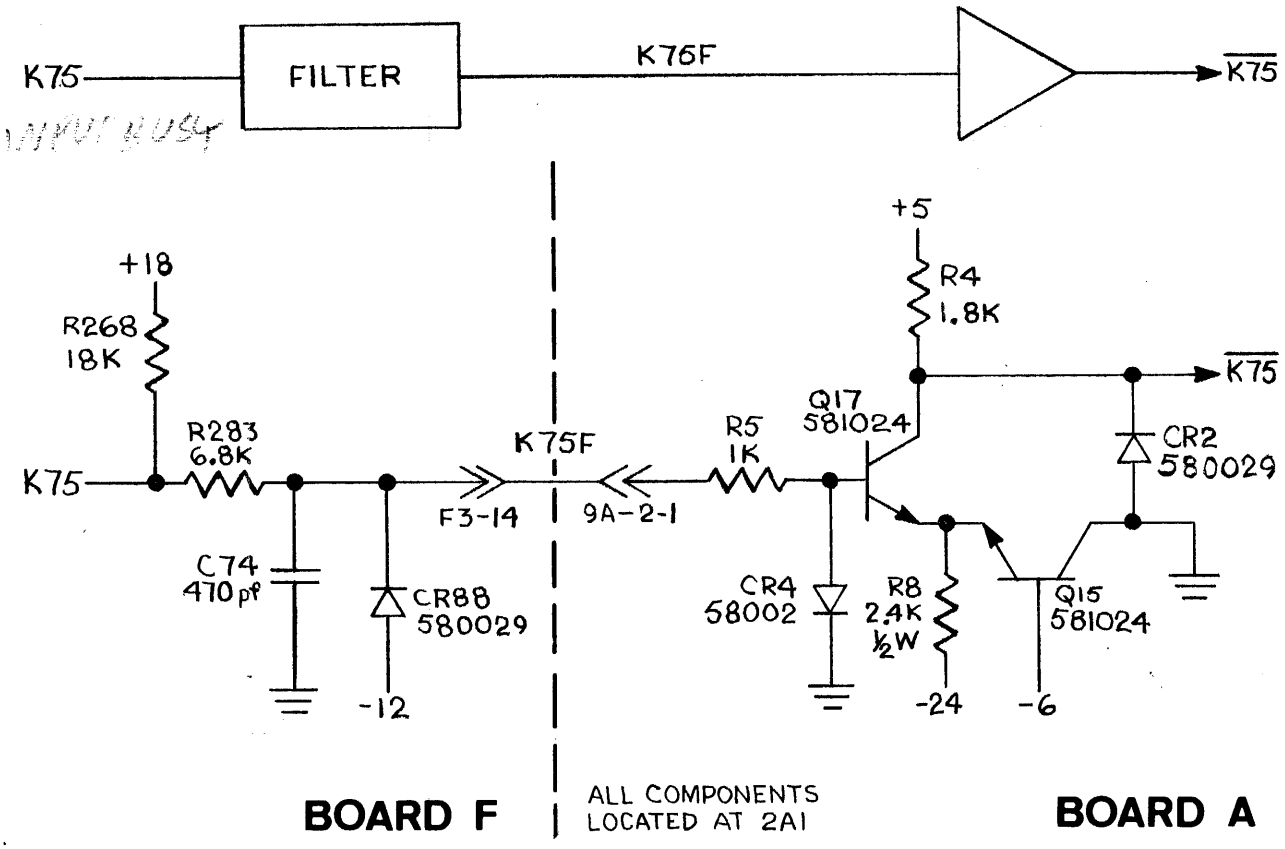


Figure 4.24 Input Circuit $\overline{K75}$.

4.2.1.4 Output Circuit K176

The operation of the K176, Output Busy, circuit, shown in figure 4.25, is similar to the operation of the $\overline{K75}$ circuit, discussed in the previous paragraph, except that this circuit does perform an inversion. R282, C73, and R6 form a high-frequency filter to reduce noise at the base of Q16. CR89 prevents the junction of itself and R282 from going

more negative than -12 volts. CR3 prevents the collector of Q18 and K176 from going below ground. When all the selected output devices are not busy, the base-emitter junction of Q18 is forward biased, placing the emitter of Q16 at -6 volts. K76 is at -14 volts nominally (logical 0). Q16 is forced off and Q18 remains on. With Q18 conducting, K176 is clamped at ground (logical 0) by CR3. When no output devices are attached to the processor or when a selected output device is busy, K76 is pulled positive by the +18 volt supply through R267. Q16 is forced on, forcing Q18 off. With Q18 off, K176 is pulled to +5 volts (logical 1) through R3.

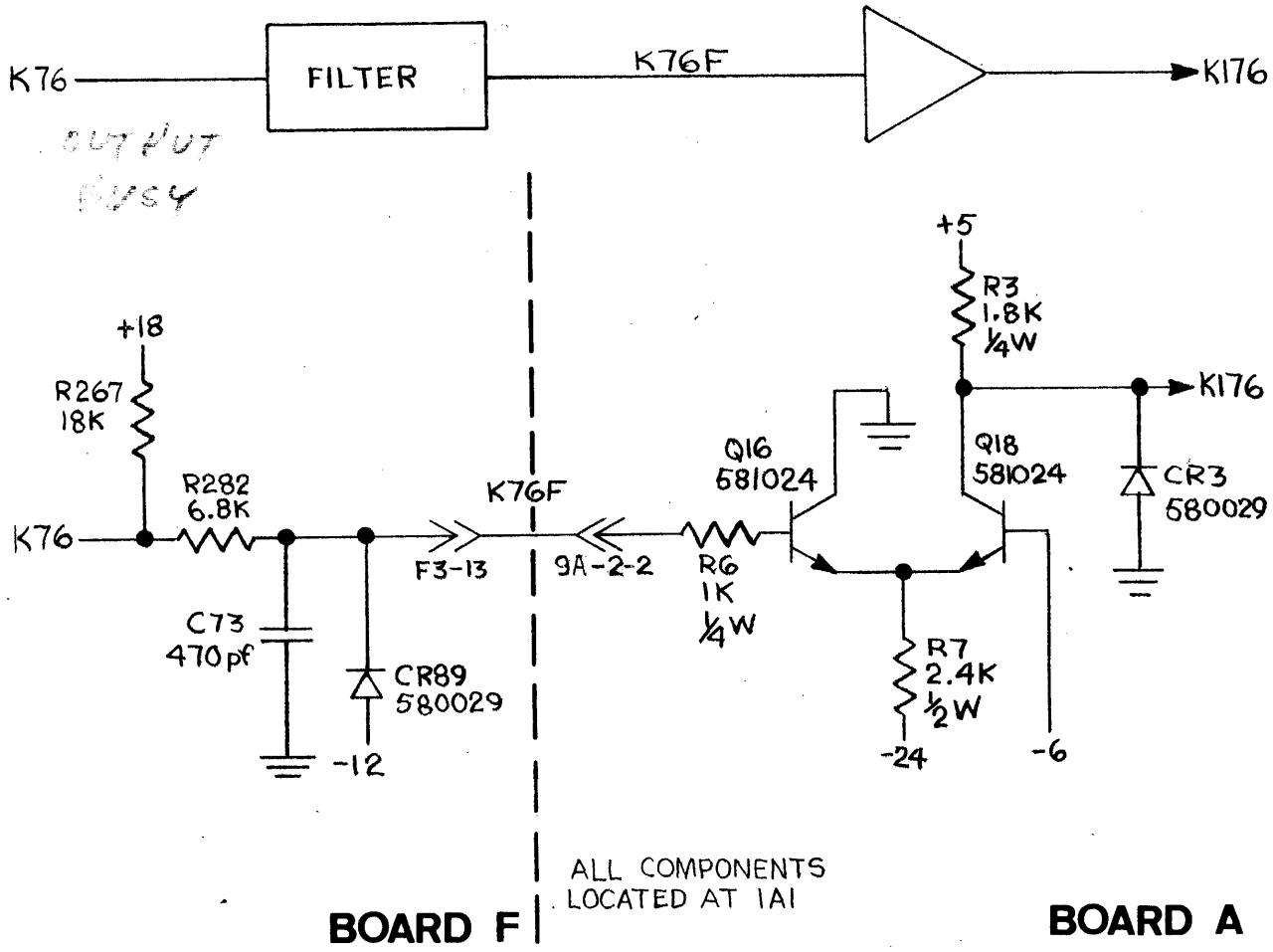


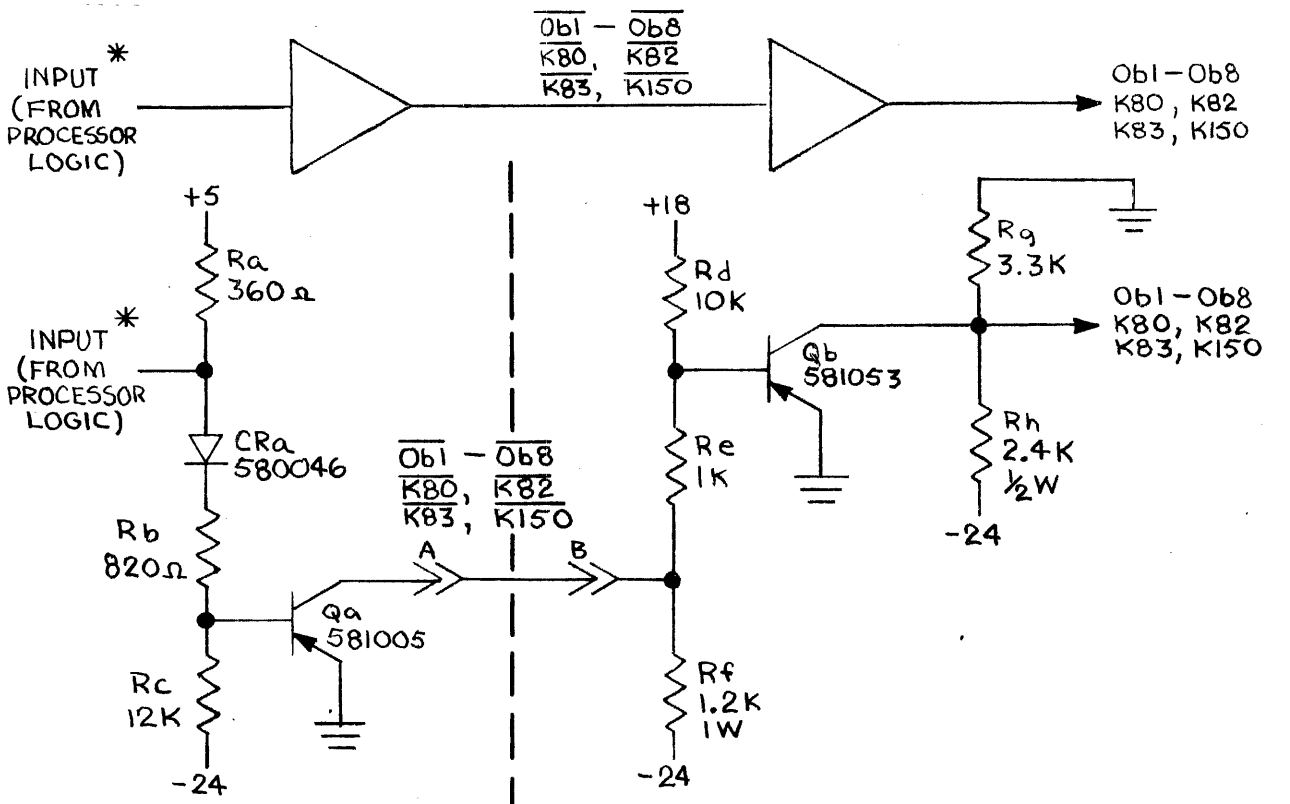
Figure 4.25 Output Circuit K176.

4.2.1.5 Output Circuits Ob1 - Ob8, K80, K82, K83, and K150

These circuits, see figure 4.26 and table 4.2, perform 2 functions. They drive their respective lines on the interface and shift the signals from

Rev.18NOV68

the processor logic level (0 volts = logical 0, +5 volts = logical 1) to the nominal interface level (nominally -14 volts = logical 0, 0 volts = logical 1). When the input drives the junction of Ra and CRa to ground (logical 0), CRa is forward biased and the base-emitter junction of Qa is forward biased, turning it on. This causes the base of Qb to go positive, turning it off. The junction of Rg and Rh drops to -14 volts (logical 0). When the logic of the processor does not drive the junction of Ra and CRa to ground, the +5 volt supply pulls the input line toward +5 volts (logical 1). CRa is forward biased and the base of Qa goes positive, turning it off. This allows the base of Qb to go negative, turning it on. With Qb on, the junction of Rg and Rh is pulled to ground (logical 1). The purpose of CRa is to provide a negative voltage (its diode drop) to offset the input voltage when the input is at its upper logical 0 margin of +0.4 volts. This insures that Qa is turned on under this condition.



Output of Gate	M114-6,	figure 3.93	Output of Gate	M113-11,	figure 3.93
	M114-3	" "		M113-8	" "
	M114-11	" "		M120-12	" 3.78
	M114-8	" "		M120-6	" "
	M113-6	" "		M120-8	" "
	M113-3	" "		M116-6	" 3.79

Figure 4.26 Output Circuits Ob1 - Ob8, K80, K82, K83, and K150.

	SCHEMATIC LABEL	INDIVIDUAL CIRCUITS					
		Ob~~1~~8	Ob~~2~~7	Ob~~3~~6	Ob~~4~~5	Ob~~5~~4	Ob~~6~~3
COMPONENT	CRa	6A2CR31	5A2CR32	5A2CR33	5A2CR34	4A2CR35	4A2CR36
	Qa	6A2Q1	5A2Q2	5A2Q3	5A2Q4	4A2Q5	4A2Q6
	Qb	Q103	Q104	Q105	Q106	Q107	Q108
	Ra	6A2R21	5A2R20	5A2R19	5A2R18	4A2R17	4A2R16
	Rb	6A2R22	5A2R23	5A2R24	5A2R25	4A2R26	4A2R27
	Rc	6A2R45	5A2R44	5A2R43	5A2R42	4A2R41	4A2R40
	Rd	R304	R305	R306	R307	R308	R309
	Re	R292	R293	R294	R295	R296	R297
	Rf	R317	R318	R319	R320	R321	R322
	Rg	R270	R271	R272	R273	R274	R275
	Rh	R247	R248	R249	R250	R251	R252
CONNECTOR	A	F3-8	R3-7	R3-6	R3-5	R3-4	R3-3
	B	9A-2-7	9A-2-8	9A-2-9	9A-2-10	9A-2-11	9A-2-12

	SCHEMATIC LABEL	INDIVIDUAL CIRCUITS					
		Ob~~7~~2	Ob~~8~~1	K8~~0~~3	K82	K8~~3~~150	K15~~0~~80
COMPONENT	CRa	3A2CR37	3A2CR38	2A2CR39	2A2CR40	1A2CR41	1A2CR42
	Qa	3A2Q7	3A2Q8	2A2Q9	2A2Q10	1A2Q11	1A2Q12
	Qb	Q109	Q110	Q111	Q112	Q113	Q114
	Ra	3A2R15	3A2R14	2A2R13	2A2R12	1A2R11	1A2R10
	Rb	3A2R28	3A2R29	2A2R30	2A2R31	1A2R32	1A2R33
	Rc	3A2R39	3A2R38	2A2R37	2A2R36	1A2R35	1A2R34
	Rd	R310	R311	R312	R313	R314	R315
	Re	R298	R299	R300	R301	R302	R303
	Rf	R323	R324	R325	R326	R327	R328
	Rg	R276	R277	R278	R279	R280	R281
	Rh	R253	R254	R255	R256	R257	R258
CONNECTOR	A	F3-2	F3-1	F3-12	F3-10	F3-9	F3-11
	B	9A-2-13	9A-2-14	9A-2-3	9A-2-5	9A-2-6	9A-2-4

Table 4.2 Output Circuits Ob1 - Ob8, K80, K82, K83, and K150.

4.2.1.6 Output Circuit W110

This circuit, shown in figure 4.27, drives the Inhibit line on the interface and shifts the signal levels of W10 to the nominal interface levels (-15 volts = logical 0, 0 volts = logical 1). The warm-up circuit does not supply drive to W10 (logical 0) after the processor has warmed up. As a result, CR58 clamps the base of Q102 at -15 volts. Q102 is turned off and W110 is pulled to -15 volts (logical 0). During warm-up, the warm-up circuit supplies drive to W10 (logical 1), by trying to force it toward +18 volts, Q102 is forward biased into saturation, placing its emitter and W110 at ground (logical 1).

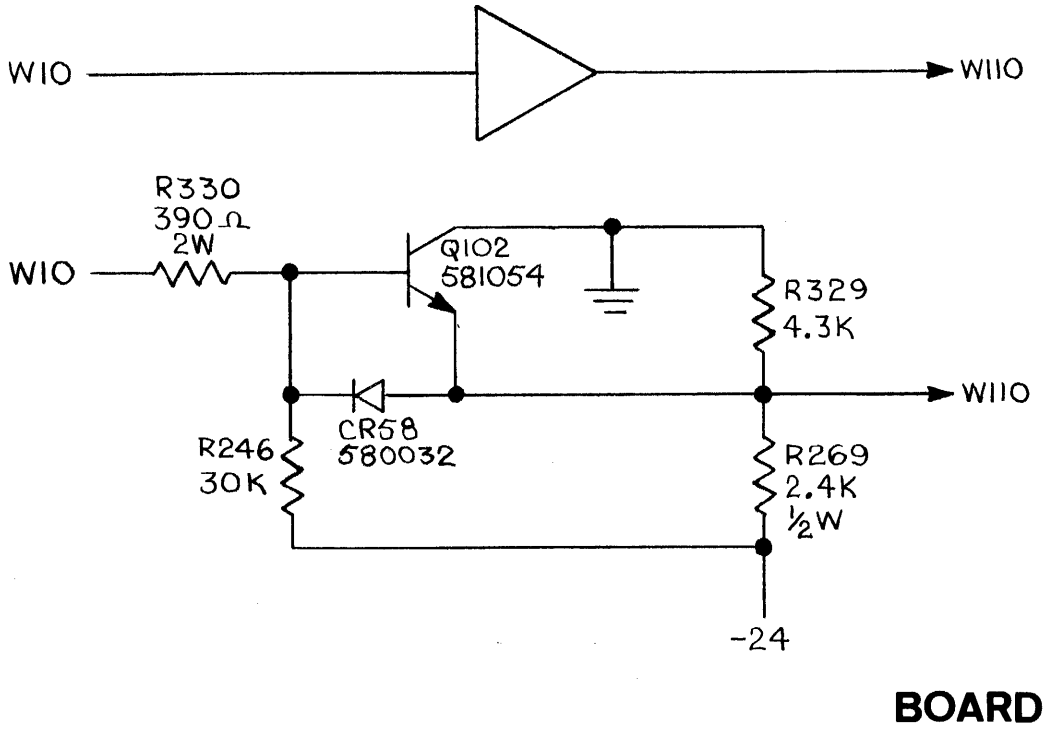


Figure 4.27 Output Circuit W110.

4.2.2 LAMP DRIVER CIRCUITS

4.2.2.1 Lamp Driver Circuits 0 - 7, TRACK, K, and READY

These circuits, see figure 4.28 and table 4.3, act to switch their respective indicator lights, located on the operator console, on and off in response to the input from the processor logic. Ra, Rb, Ca, and Rc form an RC integrator which reduces the switching current, and subsequently the magnetic radiation, between the input and Qa. Qa is used to switch lamp La on and off. Re serves as a "keep-alive" for La, i.e., it allows enough filament current to flow to keep it warm, though not

lit, and prolong its life. Assuming the input drives the Ra, Rb junction to ground (logical 0), Qa is turned off and La unlit. (Note that CR54, which references the Qa emitter at +.6 volts, is common to all lamp driver circuits.) When the input does not supply drive to the Ra, Rb junction, Ca charges toward +5 volts through Ra and Rb. As soon as Ca is charged to about +1.5 volts, the base-emitter junction of Qa is forward biased. Qa is turned on, current flows through La, and La lights. Due to the presence of Rc, Ca is charged a few tenths of a volt above the turn on threshold of Qa. Thus, when the input reverses state, and drives the Ra, Rb junction to ground, Ca must discharge a few tenths of a volt through Rb and Rc before Qa turns off and La goes out.

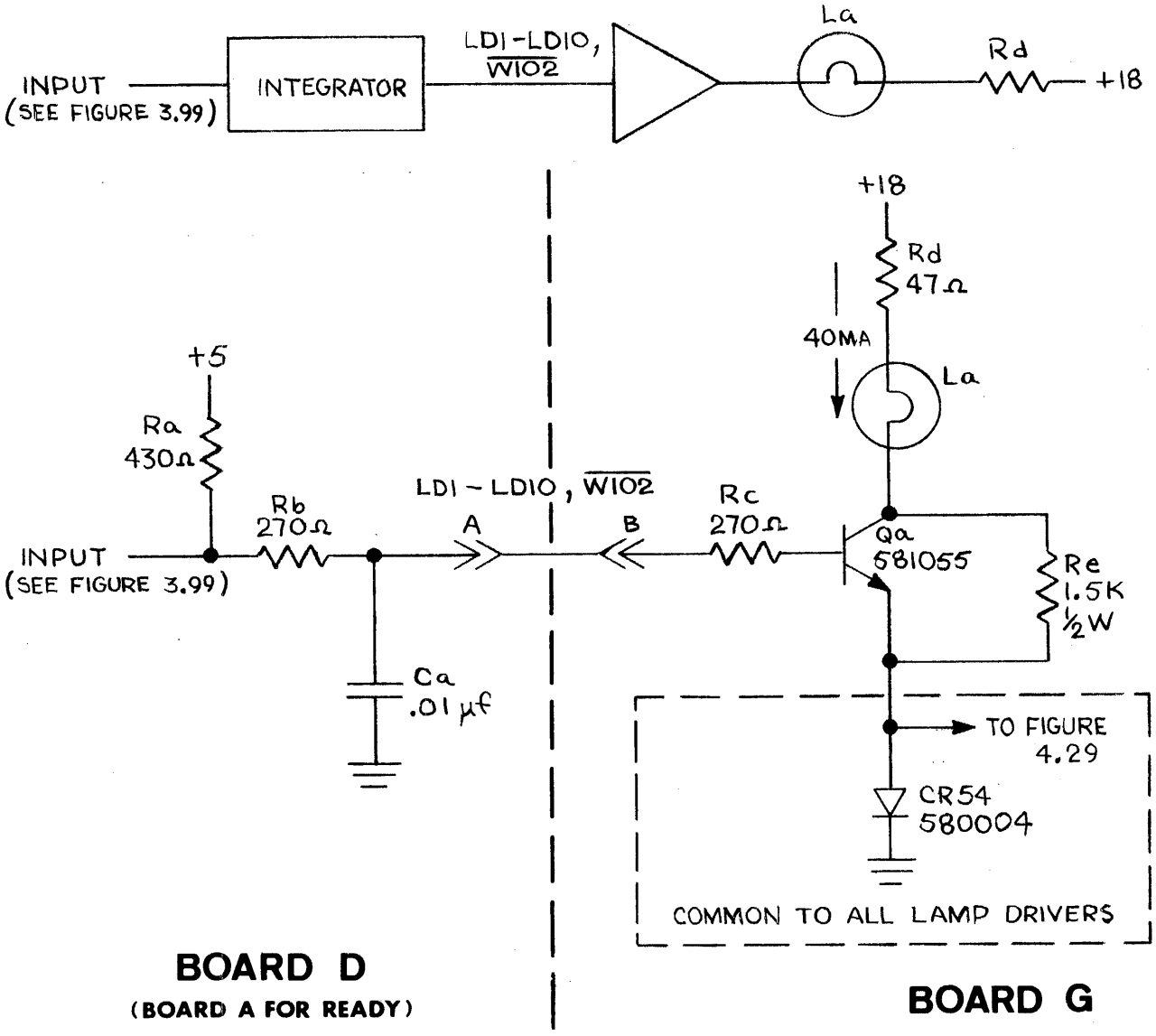


Figure 4.28 Lamp Driver Circuits 0-7, TRACK, K, and READY.

Rev. 1MAY69

	SCHEMATIC LABEL	INDIVIDUAL CIRCUIT				
		6	7	TRACK	K	READY
COMPONENT	Ca	7D2C239	7D1C240	7D1C241	7D1C242	8A1C202
	La	L2	L1	L9	L10	L13
	Qa	Q86	Q85	Q93	Q94	Q44
	Ra	6D2R142	6D1R141	6D1R140	6D1R139	8A1R71
	Rb	6D2R135	6D1R136	6D1R137	6D1R138	8A1R72
	Rc	R367	R368	R360	R359	R357
	Rd	R233	R237	R240	R241	R244
	Re	R355	R356	R348	R347	R344
CONNECTOR	A	G1-12	G1-13	G1-5	G1-4	G2-5
	B	9D-1-8	9D-1-9	9D-1-10	9D-1-11	9A-1-10

	SCHEMATIC LABEL	INDIVIDUAL CIRCUIT					
		0	1	2	3	4	5
COMPONENT	Ca	7D3C233	7D2C234	7D2C235	7D2C236	7D2C237	7D2C238
	La	L8	L7	L6	L5	L4	L3
	Qa	Q92	Q91	Q80	Q89	Q88	Q87
	Ra	6D3A148	602R147	6D2R146	6D2R145	6D2R144	6D2R143
	Rb	6D3R129	602R130	6D2R131	6D2R132	6D2R133	6D2R134
	Rc	R361	R362	R363	R364	R365	R366
	Rd	R239	R238	R237	R236	R235	R234
	Re	R349	R350	R351	R352	R353	R354
CONNECTOR	A	G1-6	G1-7	G1-8	G1-9	G1-10	G1-11
	B	9D-1-2	9D-1-3	9D-1-4	9D-1-5	9D-1-6	9D-1-7

Table 4.3 Lamp Driver Circuits 0-7, TRACK, K, and READY.

4.2.2.2 Lamp Driver Circuit HALT and RUN

This circuit, shown in figure 4.29, turns the HALT indicator light on and the RUN indicator light off (both lights are located on the operator console), and vice versa under the control of the input from the processor's logic. The operation of this circuit is similar to the lamp drivers discussed in the previous paragraph. R149, R128, C232, and R358 form the integrator used to reduce magnetic radiation. When Q96 is on (no input drive - logical 1 - C32 charged to about +1.5 volts), L12 is lit. The base-emitter junction of Q95 is reverse biased and L11 is unlit. When Q96 is off (input drive - logical 0 - C32 discharged), L12 is unlit. The base-emitter junction of Q95 is forward biased, Q95 is conducting, and L11 is lit.

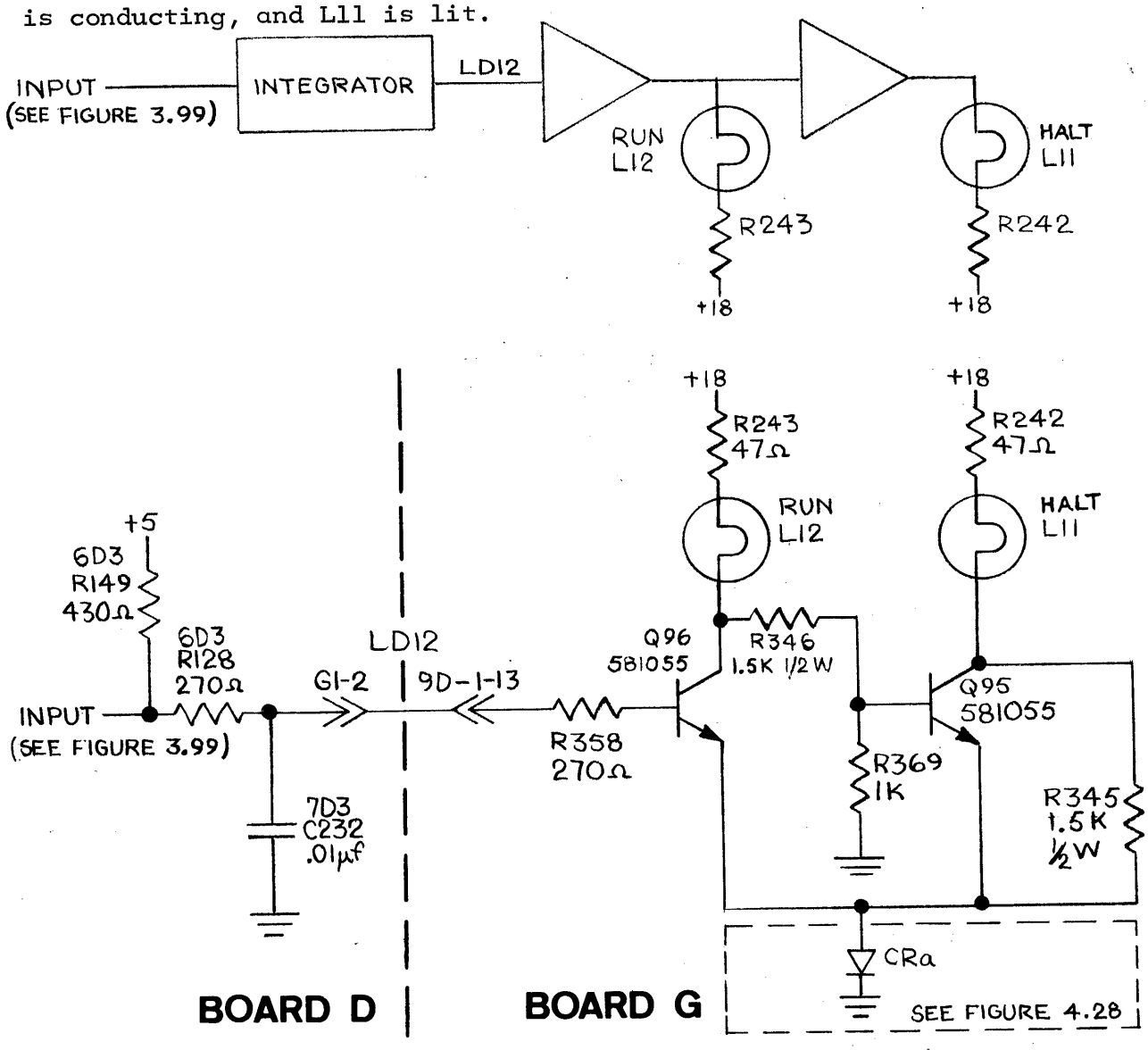


Figure 4.29 Lamp Driver Circuit, HALT and RUN.

Rev. 1MAY69

4.2.3 RECORD CIRCUITS

4.2.3.1 Record Circuits, Scratchpad and Block Interchange Loops

These circuits, see figure 4.30 and table 4.4, are used to record information on their respective tracks around the drum. Each circuit has 2 logically opposed inputs - labeled on the schematic as input and input. In order to record a logical 1, the input must go to logical 1 while the input is at logical 0. In order to record a logical 0, the input must be at logical 0 while the input goes to logical 1. When both inputs go to or are at logical 0, nothing happens. The processor logic prevents both inputs from going to logical 1. During warm-up of the processor, W1 is at ground. Since W1 serves as the pull-up supply for the inputs, they cannot rise above ground. During normal operation of the processor, W1 is at +7 volts. If both inputs are pulling current from W1, the bases of Qa and Qb are at ground (logical 0). Since CRc and Rc reference the emitters of Qa and Qb at +.6 volts, both transistors are off and current does not flow through the record head. Subsequently, nothing is recorded. However, if the input should stop pulling current from W1, the base of Qa (input) goes positive and Qa turns on. Current then flows from the +35 volt supply through Rd, the 1 half of the record head, Re, Qa, and CRc. Qb remains off. Subsequently, a 1 is recorded on the drum. If instead of input going positive, the input when positive, Qb would have turned on. Current then flows from the +35 volt supply through Rd, the 0 half of the record head, Rf, Qb, and CRc. Qa remains off and no current flows through the 1 side of the record head. Subsequently, a 0 is recorded on the drum. When current flows in either half of the record head, a voltage is induced across the other half. If voltage is induced across the 1 half, normally reversed biased CRa becomes forward biased, clamping the collector of Qa at +35 volts to prevent Qa from breaking down. If the voltage is induced across the 0 half, CRb becomes forward biased to protect Qb. Ca serves as high-frequency noise filter on the +35 volt line. Cb reduces the voltage transient across CRc when Qa or Qb turns on.

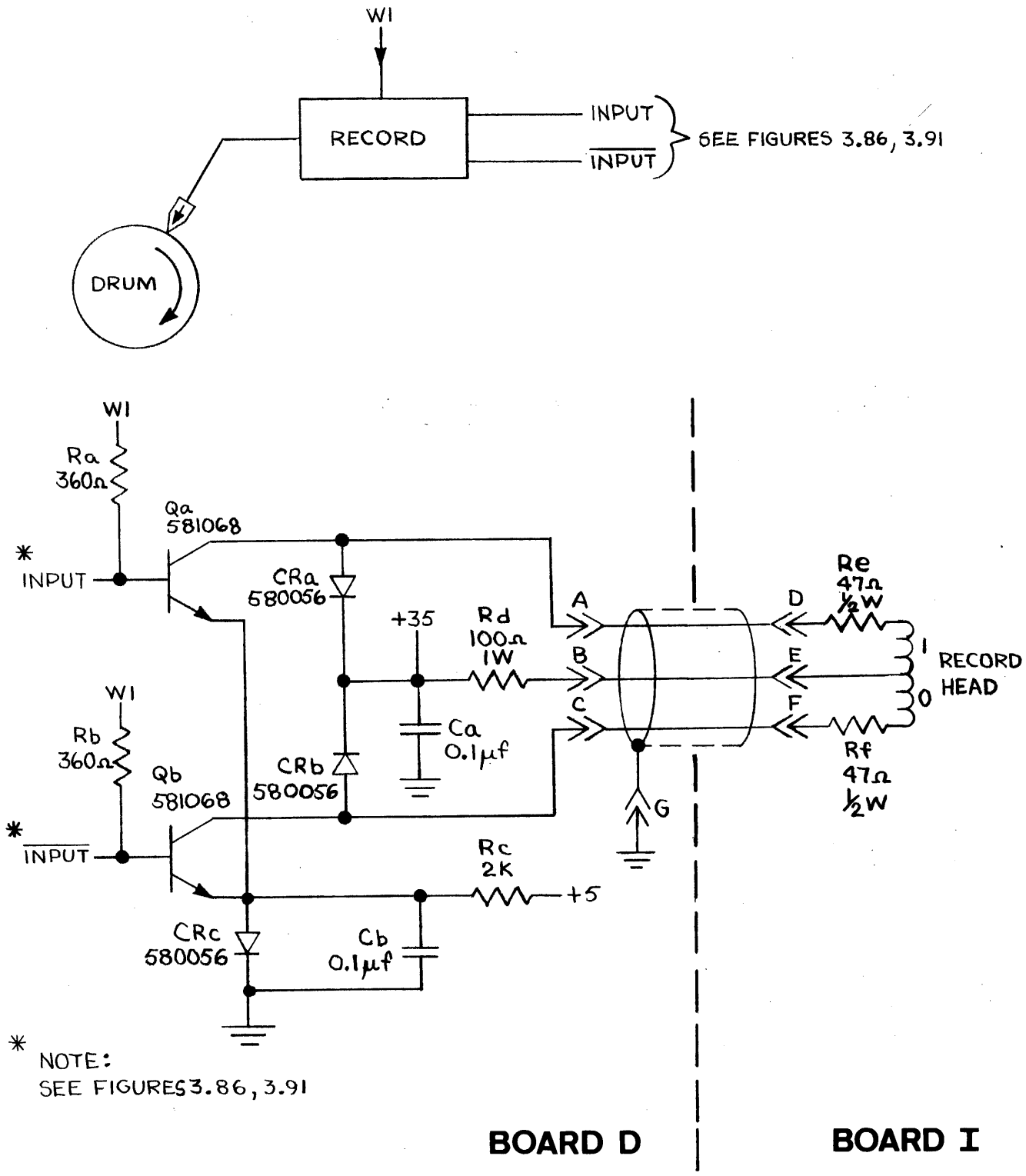


Figure 4.30 Record Circuits, Scratchpad and Block Interchange Loops.

	SCHEMATIC LABEL	INDIVIDUAL CIRCUITS	
		S	BI
COMPONENT	Ca	7D9C79	5D9C80
	Cb	7D9C179	6D9C178
	CRa	7D9CR73	6D9CR75
	CRb	7D9CR74	6D9CR76
	CRc	7D9CR78	6D9CR77
	Qa	7D9Q54	6D9Q56
	Qb	7D9Q55	6D9Q57
	Ra	7D9R336	6D9R334
	Rb	7D9R335	6D9R333
	Rc	8D9R340	6D9R378
	Rd	7D9R331	6D9R214
	Re	*	*
	Rf	*	*
CONNECTOR	A	7D9-B	6D9-B
	B	7D9-C	6D9-C
	C	7D9-A	6D9-A
	D	*	*
	E	I-17	I-11
	F	*	*
	G	7D9-D	6D9-E

* Determined as discussed in paragraph 5.5.2.1.

Table 4.4 Record Circuits, Scratchpad and Block Interchange Loops.

4.2.3.2 Track Selection and Record Circuits, General Storage

Before recording can begin in a specified track-sector address of general storage, the addressed track must be selected for use and the addressed sector must be found. The process of finding a specified sector, termed "sector comparison", is discussed in paragraph 3.3. The process of selecting a track is performed by the track selection circuits of the processor.

Whenever the processor decodes a track-sector address, one of the 4 row signals is forced low, turning on its associated row driver. Simultaneously, one of the 8 column signals are forced high, turning on its associated column driver. All other row and column drivers are off. Each record/playback head of general storage is connected, via diodes, to one row and one column driver in such a way that no two heads connect to the same row/column combination. Depending upon which row/column driver combination is turned on, all the diodes of only one head are forward biased, and the track associated with this head is selected. The remaining 31 heads and the tracks associated with these heads are unselected. The track selection matrix table in figure 4.31 lists which track is selected by each row/column combination. For example, if the processor decodes track address 9, row driver 2 and column driver 5 are turned on, resulting in the selection of the head for track 9.

Each row driver, see figure 4.32 and table 4.5, consists of 2 transistors, Qa and Qb. When Qa is on, Qb is off, and vice versa. When Qb is on the row driver is in the on state; when Qb is off the row driver is in the off state. A row driver is forced off when its input (A30-A33) does not supply drive (logical 1), and on when its input supplies drive (logical 0). All 4 Qb emitters are tied together and connected to a common bias circuit consisting of CR56, CR57, and R186. While the processor is on there is always one row driver which is on. Since Qb of such a driver will be on, the emitters of all the Qb's are held at about +3.5 volts. When one row driver is turned off another is turned on so that the Qb emitters remain essentially at +3.5 volts.

As mentioned above, without input drive the row driver is off. The Qa base is pulled toward +5 volts through Ra. The Qa base-emitter junction is forward biased, turning Qa on. The Qa collector is almost at ground potential. Since the Qb emitter is at +3.5 volts, the Qb base-emitter junction is reverse biased, and Qb is off. The collector of Qb is at +35 volts.

In order for a row driver to be turned on, its input must drive current through Ra to the point when the voltage at the Qa base drops below the emitter reference voltage (+.6 volts) provided by CR70. When this is done, the Qa base-emitter junction is reverse biased, turning Qa off. Since current is no longer pulled through Rb by Qa, the base of Qb goes positive to point where it forward biases the base-emitter junction of Qb. Qb turns on and saturates. Its collector goes to +4 volts.

Each column driver consists of 2 transistors, Qc and Qd. When Qc is on, Qd is on. When Qc is off, Qd is off. When Qd is on, the column driver is in the on state; when Qd is off the column driver is in the off state. In order for a column driver to be off, its input must drive current through Rd to the point where the voltage at the Qc base drops to nearly ground, reverse biasing the Qc base-emitter junction. Qc is off and its collector goes to +35 volts. Since the emitter of Qd is connected to +5 volts, the Qd base-emitter junction is reverse biased. Qd is off and its collector is at -24 volts. In order for a column driver to be turned on its input must not apply drive through Rd. The +35 volt supply can then pull the Qc base positive to point where its base-emitter junction is forward biased. Qc turns on and saturates. Its collector drops toward ground potential until the Qd base-emitter junction is forward biased. Qd turns on and saturates. Its collector goes to about +4.5 volts.

The track selection circuit is designed so that with any row/column driver combination turned on, the diodes of only one of the 32 heads have their anodes connected through the head to the collector of the Qd which is on (collector at +4.5 volts) while having their cathodes connected through the selection transformer (T2) to the collector the Qb which is on (collector at +4 volts). All the diodes of this head are thereby forward biased, and the head is selected.

A current path exists between the row driver which is on and the column driver which is on. Current flows from the +5 volt supply through Qd into the center tap of the head. Half of the current goes through the 1 half of the head; the other half goes through the 0 half of the head.

Since the current flow through each half of the head is in opposite directions, a magnetic field is not produced (due to various factors the current flow through each half may not be equal. This imbalance is not enough to produce a field strong enough to adversely affect the drum). From the end windings of the head, current flows through the forward biased diodes into the end windings of the respective T2 secondary winding. Current flow through each half of the T2 secondary is in opposite directions, preventing a field from being produced. At the center tap of T2 the current flow comes together and flows through Qb, R186, and into the -24 volt supply.

With a general storage record/playback head selected, the processor may begin recording on an addressed sector of the track associated with the selected head once the sector is located, as described in paragraph 3.3. With one minor exception, the operation of the general storage record circuit, shown in figure 4.33, is identical to the record circuit discussed in paragraph 4.2.3.1. The exception being that the general storage record circuit drives a transformer, T2, instead of a record head.

When record current flows through the 1 or 0 half of the T2 primary, a 34 volt record pulse is induced across the T2 secondaries. The ±17 volt pulse induced across the halves of the T2 secondary associated with the selected head drives current through one half of the selected head while reverse biasing the diodes of the other half and disabling it. A record pulse generated to record a 1's bit will drive current through the 1's bit half of the selected head while disabling the 0's bit half. The opposite is true of a 0's bit record pulse. The path for the current induced by the record pulse is from the T2 center tap through Qb and CR56 into the +5 volt supply. From the +5 volt supply current flows through Qd, the proper side of the record head, through the forward biased diode to the end tap of the T2 secondary. Note that the record pulse raises the Qb emitter voltage from +4 to the point where CR56 turns on, clamping the Qb emitter at +5.6 volts for the duration of the record pulse. CR57 is a protection diode which prevents the input line from being pulled negative in case a selected head is burnt out (open).

The record pulse generated across the T2 secondaries does not have sufficient amplitude to forward bias any of the reverse biased diodes of the unselected heads. Thus, the record pulse has no effect on the unselected heads.

TRACK SELECTION MATRIX TABLE

ROWS	COLUMNS 1	2	3	4	5	6	7	8
	A20	A21	A22	A23	A24	A25	A26	A27
1 $\overline{A30}$	0	2	4	6	8	10	12	14
2 $\overline{A31}$	1	3	5	7	9	11	13	15
3 $\overline{A32}$	16	18	20	22	24	26	28	30
4 $\overline{A33}$	17	19	21	23	25	27	29	31

NOTES:
HEADS 16 THROUGH 32 ARE REMOVED FOR THE 1602
ALL DIODES 580056
* TRACK

COL. = COLUMN DRIVERS 1-8 (SEE FIGURE 4.32)

ROW = ROW DRIVERS 1-4 (SEE FIGURE 4.32)

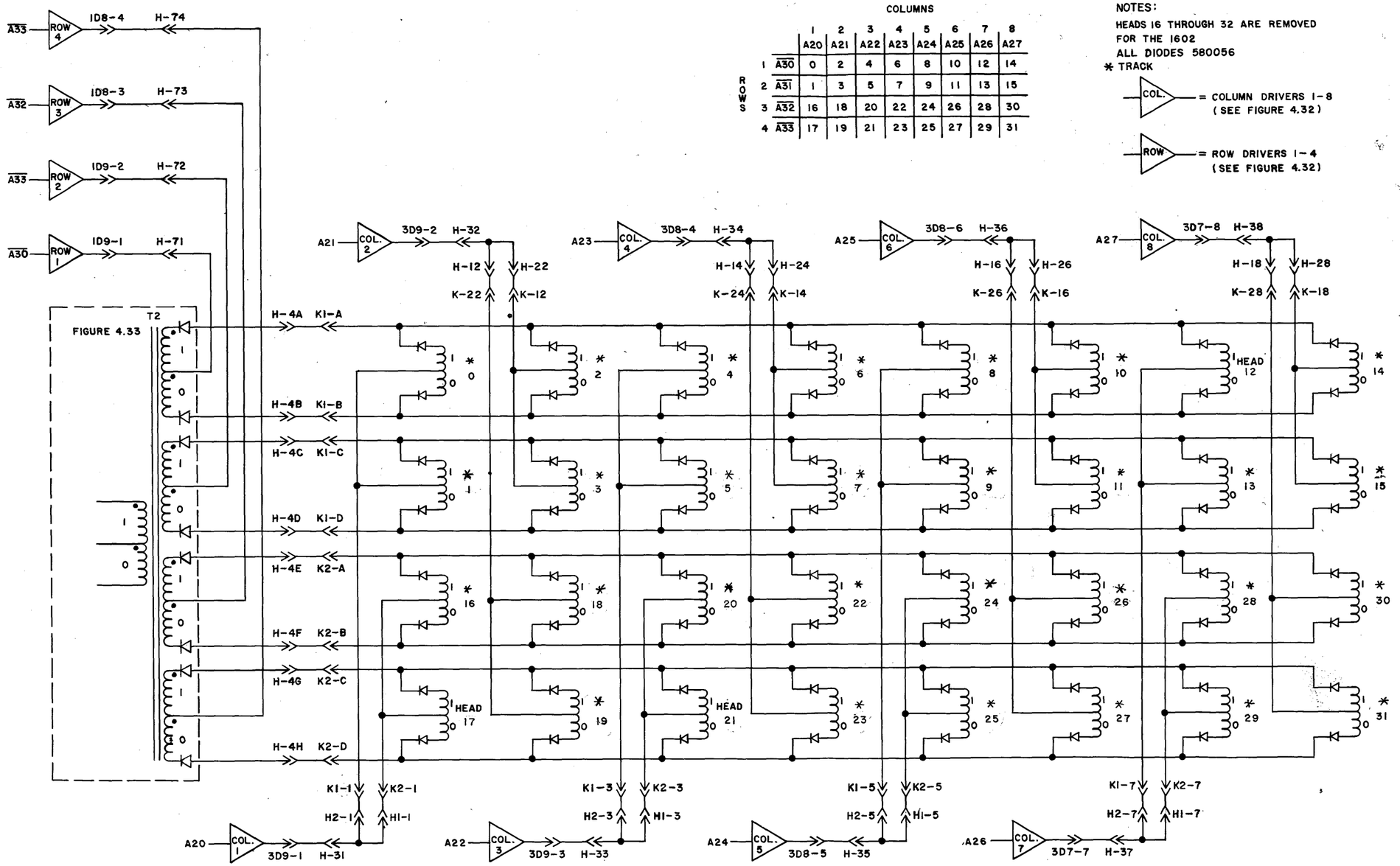


Figure 4.31 Track Selection Circuits.

Rev. 1MAY69

COMPONENT	SCHEMATIC LABEL	INDIVIDUAL CIRCUIT					
		Row 1	Row 2	Row 3	Row 4	Col. 1	Col. 2
	Qa	2D9Q66	2D9Q67	2D8Q68 *	2D8Q69 *	------	------
	Qb	1D9Q79	1D9Q80	1D8Q81 *	1D8Q82 *	------	------
	Qc	------	------	------	------	4D9Q58	4D9Q59
	Qd	------	------	------	------	3D9Q71	3D9Q72
	Ra	2D9R181	2D9R180	2D8R179	2D8R178	------	------
	Rb	2D9R185	2D9R184	2D8R183	2D8R182	------	------
	Rc	1D9R177	1D9R176	1D8R175	1D8R174	------	------
	Rd	------	------	------	------	4D9R202	4D9R201
	Re	------	------	------	------	4D9R210	4D9R209
	Rf	------	------	------	------	3D9R194	3D8R193

COMPONENT	SCHEMATIC LABEL	INDIVIDUAL CIRCUIT					
		Col. 3	Col. 4	Col. 5	Col. 6	Col. 7	Col. 8
	Qa	------	------	------	------	------	------
	Qb	------	------	------	------	------	------
	Qc	4D9Q60	4D8Q61	4D8Q62	4D8Q63	4D8Q64	4D7Q65
	Qd	3D9Q73	3D8Q74	3D8Q75	3D8Q76	3D7Q77	3D7Q78
	Ra	------	------	------	------	------	------
	Rb	------	------	------	------	------	------
	Rc	------	------	------	------	------	------
	Rd	4D9R200	4D8R199	4D8R198	4D8R197	4D7R196	4D7R195
	Re	4D9R208	4D8R207	4D8R206	4D8R205	4D8R204	4D7R203
	Rf	3D9R192	3D8R191	3D8R190	3D8R189	3D7R188	3D7R187

* THESE PARTS FOR MODEL 1601 ONLY.

Table 4.5 Row and Column Drivers.

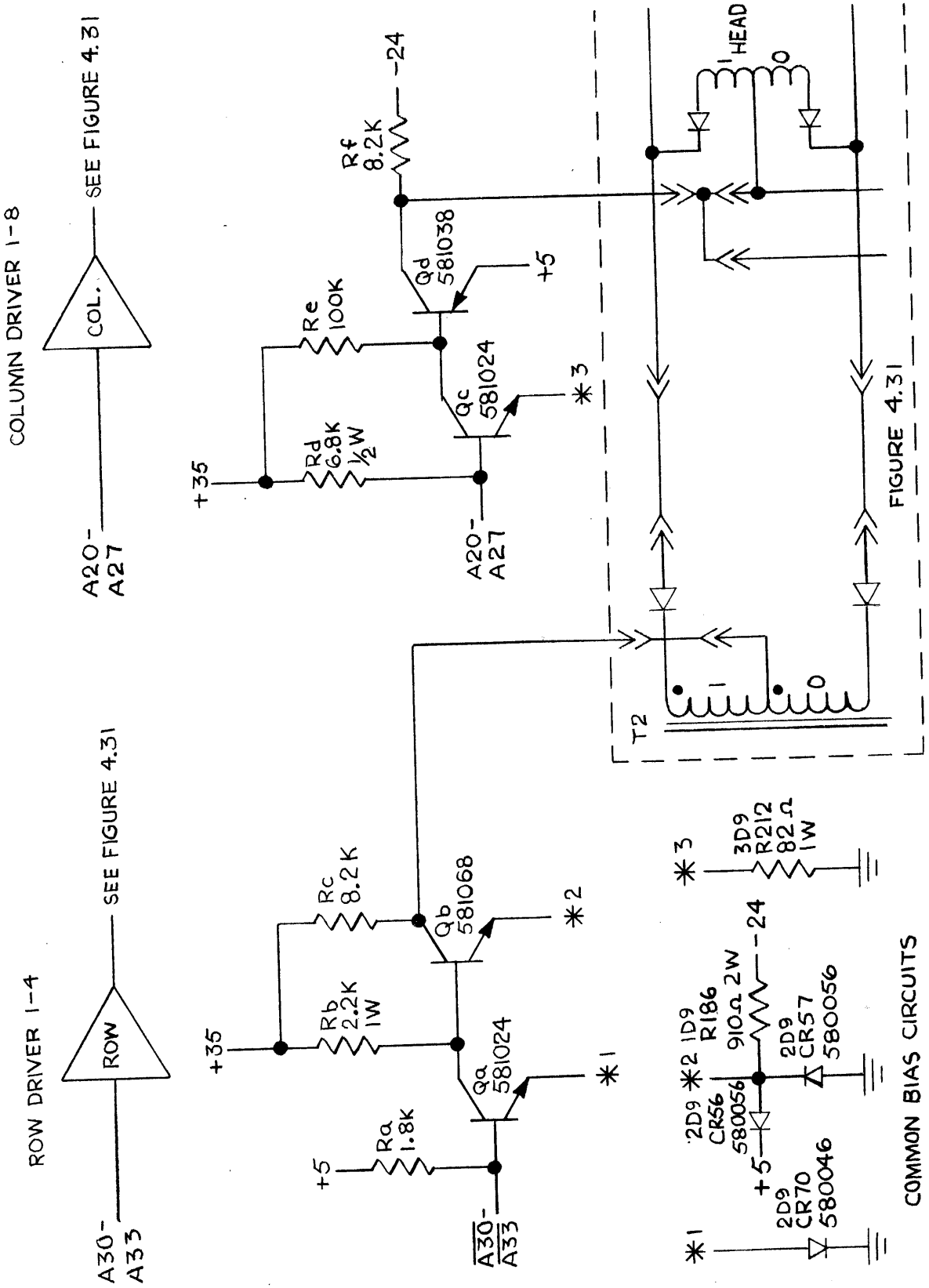


Figure 4.32 Row and Column Drivers

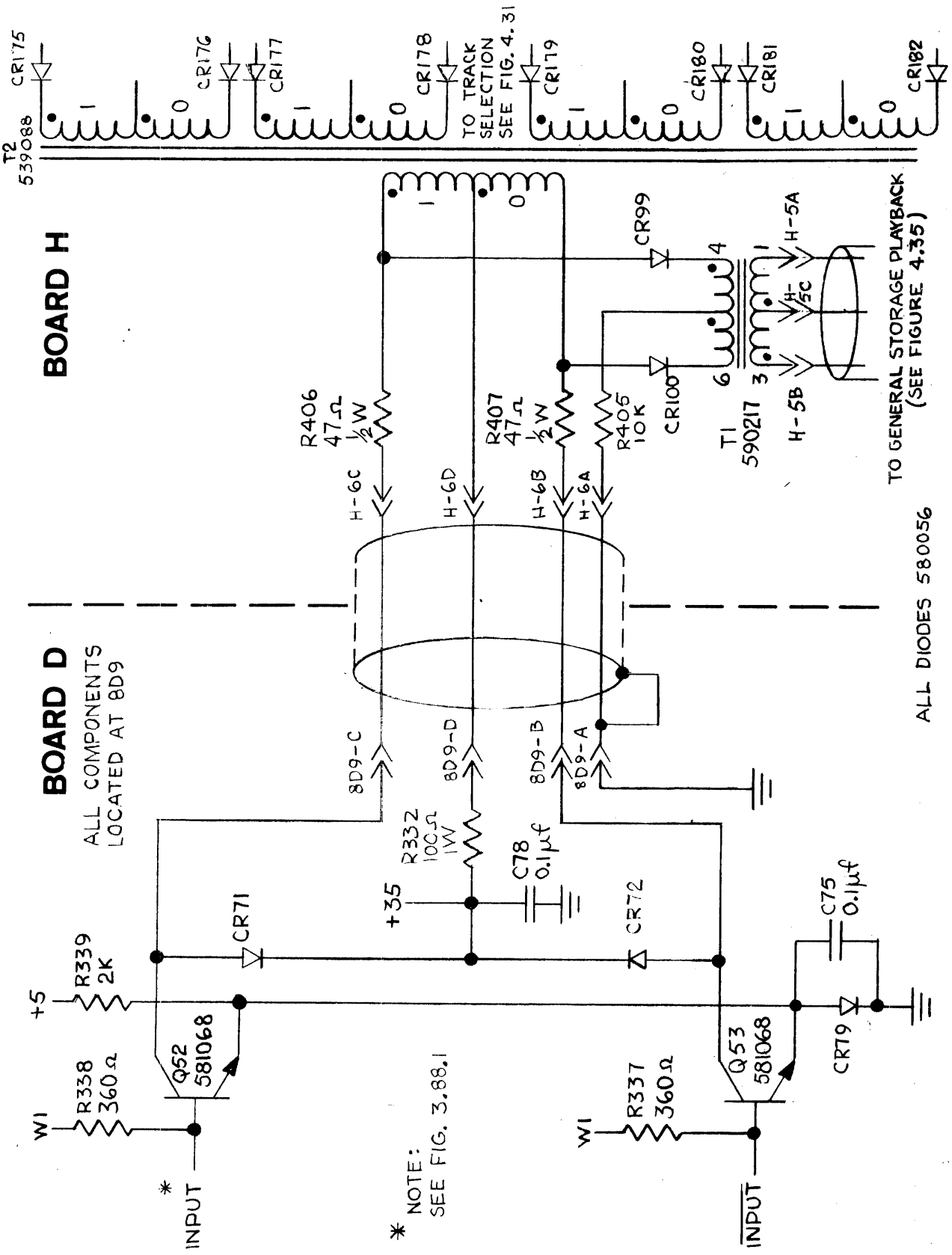


Figure 4.33 Record Circuit, General Storage.

4.2.4 PLAYBACK CIRCUITS

4.2.4.1 -6 and +12 Volt Regulators

The playback circuits receive -6 and +12 volt power from the 2 power regulators shown in figure 4.34. These circuits supply only the playback circuits. The -6 volt regulator consists simply of Zener diode CR81, and R170. The +12 volt regulator is a series regulator. Q98 is the control transistor; Q90 the sensing transistor. In normal operation both Q98 and Q90 are forward biased and are not saturated. The Q98 base voltage is controlled by Q90 so that current flow from the +18 volt supply through Q98 and the output load results in a 6 volt drop across Q98. This places the output, Q98 emitter, at +12 volts. If the output load increases, the output voltage tries to decrease. This decrease is felt at the Q90 base since its base voltage is scaled down from the output voltage via R168 and R169. A decrease in Q90 base voltage results in less current flow through R171, R172, and itself. Less voltage is dropped across R171, and the Q98 base goes positive. This forces Q98 to conduct harder to compensate, by maintaining its 6 volt drop, for the increased output load. If the load decreases, instead of increases, Q90 conducts harder, the Q98 base goes negative and Q98 conductor less to keep its 6 volt drop and thus compensate for the decreased output load. Note that the emitter of Q90 is Zener referenced to -6.2 volt by CR80 and R173. This prevents fluctuations in the +35 volt supply from affecting the Q98 base voltage.

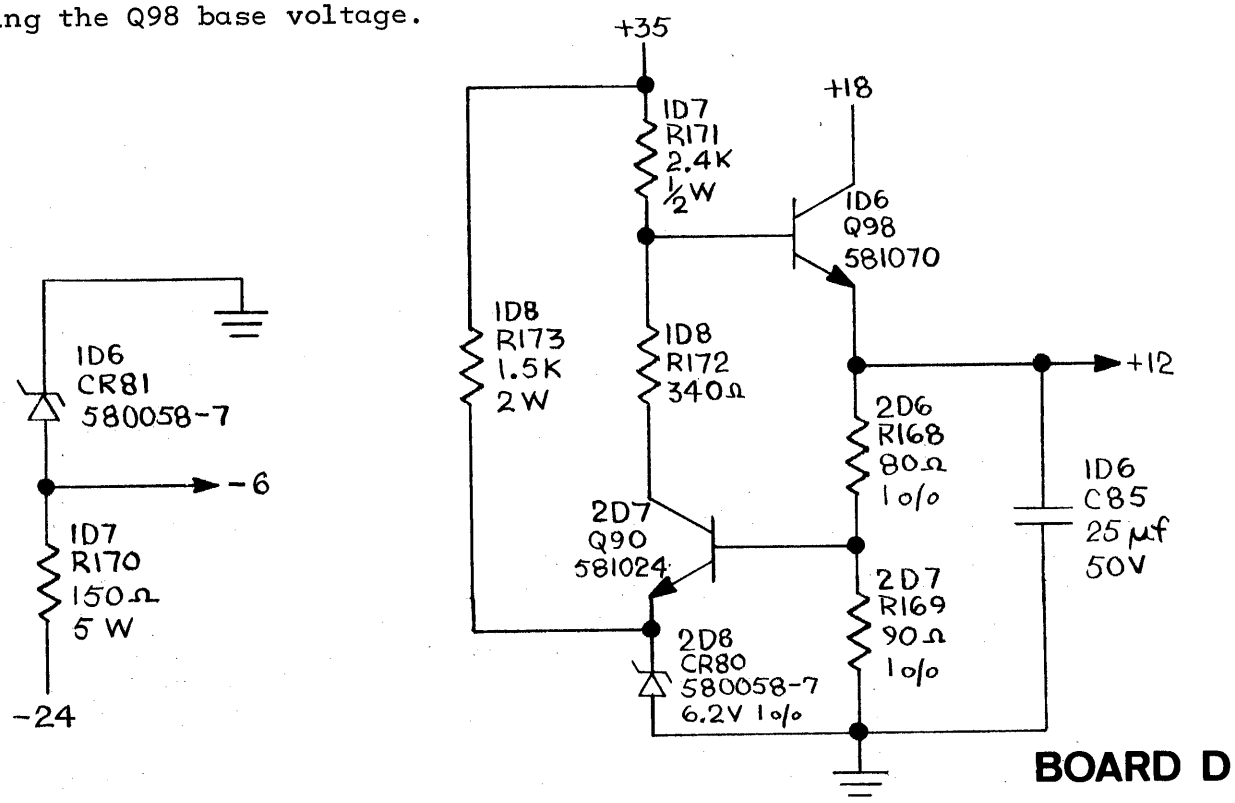


Figure 4.34 -6 and +12 Volt Regulators for Playback Circuits.

4.2.4.2 Playback Circuit, General Storage

Before information can be played back from a general storage track-sector address, the addressed track must be selected for use and the addressed sector must be found. The process of finding a specified sector, termed "sector comparison", is discussed in paragraph 3.3. The process of selecting a track is performed by the track selection circuits as described in paragraph 4.2.3.2.

Whenever information is not being recorded, the magnetic bits recorded on the drum induce a voltage across the selected head, see figure 4.32. The induced voltage is not sufficient to reverse bias the forward biased diodes of the selected head. The voltage induced across the head causes current to flow through the secondary winding of T2 associated with the selected head. As a result, playback voltage is induced in the primary of T2, see figure 4.33. Since recording is not taking place, the record circuit transistors, Q52 and Q53, are off. CR99 and CR100 are forward biased by the DC current path from the +35 volt supply through the T2 primary, the 2 primary winding halves of T1, and R405 to ground. The playback voltage induced across T2 causes current to flow through CR99 and CR100, (the playback voltage is not sufficient to reverse bias either diode) and through the T1 primary. Playback voltage is then induced in the T1 secondary, shown in figure 4.35. The voltage across the secondary of T1 is supplied, via a transmission line terminated by R150, as input to IC package M137, which is a differential comparitor or amplifier.

The voltage waveform induced across the head is shown in figure 4.35. The only difference between the waveform produced for a 1's bits and a 0's bit is in their phase. During the first 180 degrees of the 1's bit playback, a positive voltage is induced at the 1 side of the head and input pin 3 of M137. Simultaneously, the voltage induced at the 0 side of the head and input pin 2 of M137 is negative. The opposite is true during the first 180 degrees of the 0's bit playback. The voltage across pins 3 and 2 of M137 during the first 180 degrees of the 1's bit playback turns M137 off. Its output, at pin 7, is at ground. During the next 180 degrees of the 1's bit playback, the voltage across pins 3 and 2 drive M137 high. It's output goes toward +5 volts. A 100 nanoseconds delay is imposed by D1 so that the Q119 base is pulled to ground by R430 100 nanoseconds after the M137 output goes to ground. Similarly, 100 nanoseconds after the M137 output goes toward +5 volts, CR174 is reverse biased and the Q119 base driven positive. Q119 is turned off when its base is at ground, and on when its base is driven positive. CR173 clamps the Q119 collector at +5 volts when Q119 is off. When Q119 conducts, it pulls the collector to ground. Midway during the time that Q119 is off, the trailing (positive-going) edge of $\overline{Z1}$ clocks flipflop M149. Since Q119 is providing a +5 volt (logical 1) input to the flipflop at this time, the flipflop is set and forces L40 high. The

flipflop remains set until the next positive-going edge of $\overline{Z1}$ occurs, which is during the first 180 degrees of the next bit's playback. If this bit is another 1's bit, the flipflop remains set. If, however, this bit is a 0's bit, the M137 output during the first and last 180 degrees is the opposite of the 1's bit output. As a result, Q119 is supplying a ground (logical 0) input to the flipflop when the positive-going edge of $\overline{Z1}$ occurs, causing the flipflop to reset. L40 is forced low when the flipflop is reset.

Noise induced along the lines from the T1 secondary to pins 2 and 3 of M137 does not affect the output of M137, and subsequently L40. This is because the polarity of the noise voltage is the same at pins 2 and 3 of M137. Since M137 is sensitive only to a differential voltage across its inputs, it does not respond to the noise normally found in the processor.

Since the playback circuit shares part of the record circuit, various isolation techniques are used to prevent the record circuit from damaging the playback circuit and to prevent the playback circuit from sinking record current. CR99 and CR100, shown in figure 4.33, prevent record current flowing from the positive end tap of T2 through the entire primary of T1 to the other end tap of T2. Due to the capacitance of CR99 and CR100, a small current does manage to flow despite their presence. Current also flows from the positive end winding of T2 through one side of T1, via CR99 or CR100, through R405 to current. R405, however, keeps the current to a minimum.

The total current flow through the T1 primary during recording is not enough to affect the recording process, but it is sufficient to induce a voltage across the T2 secondary which exceeds the maximum input levels of M137. CR83-CR86 prevent the voltage induced across the T1 secondary from reaching levels dangerous to M137. Since the voltage is limited and not removed during recording, the output of M137 and subsequently the state of L40 is forced to logical 1 on the positive-going edge of $\overline{Z1}$ when a 1's bit is being recorded. Similarly, L40 is forced to logical 0 when a 0's bit is being recorded. This is of no consequence since the processor's logic does not "look" at L40 during general storage recording.

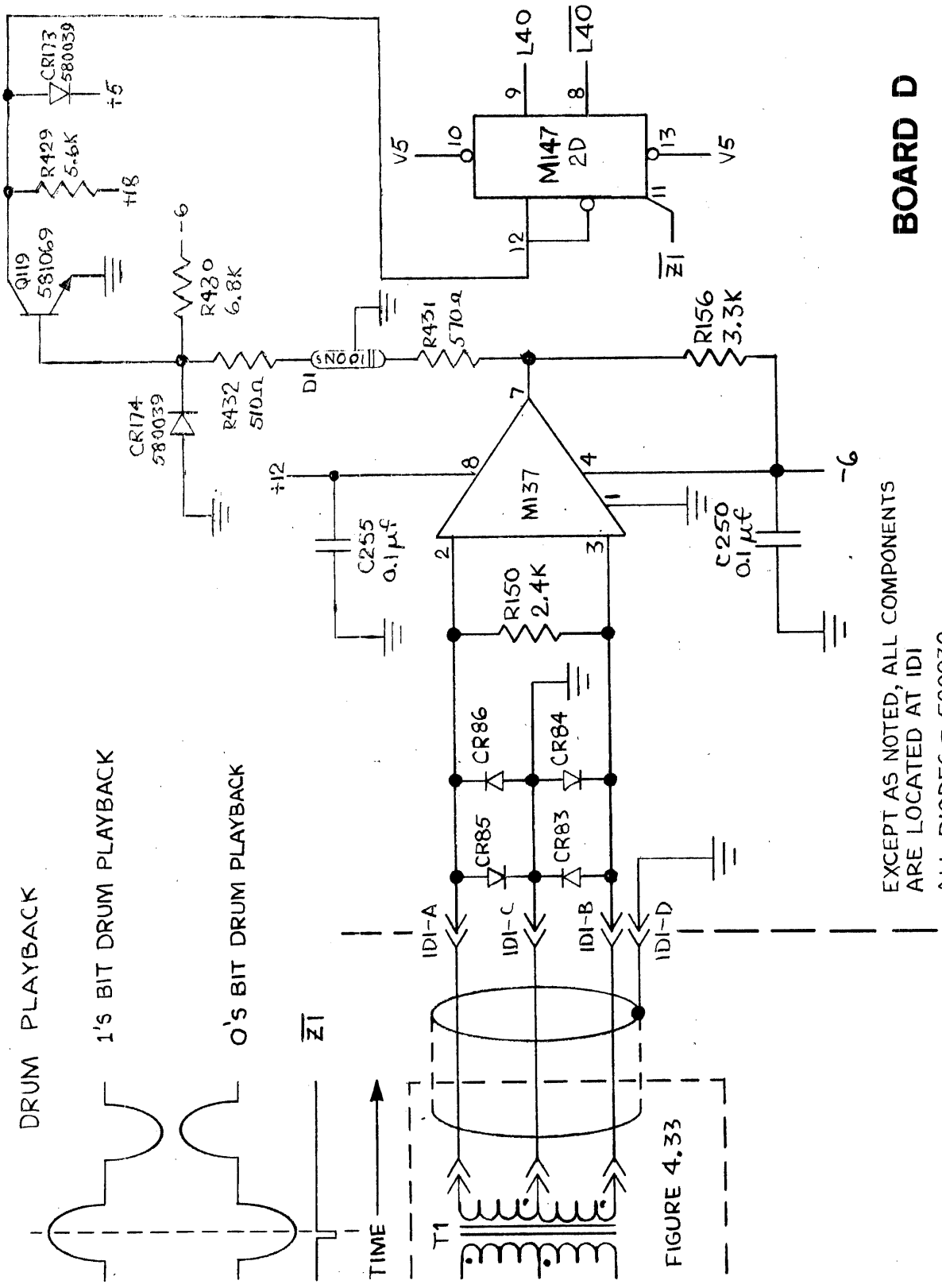


Figure 4.35 Playback Circuit, General Storage.

4.2.4.3 Playback Circuits L39, L90, Z2, and Z3

With one minor exception, operation of these circuits, see figure 4.36 and table 4.6, are identical to the playback circuit of general storage shown in figure 4.35 and discussed in paragraph 4.2.4.2. The exception being that the pins 2 and 3 of Ma connect directly to the playback head whereas pins 2 and 3 of M137 connect to the T1 secondary.

	SCHEMATIC LABEL	INDIVIDUAL CIRCUITS			
		L39	L90	Z2	Z3
COMPONENT	Ca	1D2C251	1D5C254	1D4C253	1D3C252
	Cb	1D2C256	1D5C259	1D4C258	1D3C257
	Ra	1D2R151	1D4R154	1D3R153	1D3R152
	Rb	1D2R157	1D5R160	1D4R159	1D3R158
	Ma	1D2M134	1D5M133	1D4M136	1D3M135
	Mb	4D2M146-8	2D2M147-9	2D3M148-5	2D3M148-9
CONNECTOR	A	*	*	*	*
	B	J-11	J-17	I-1	I-2
	C	*	*	*	*
	D	ID2-B	ID4-B	ID3-F	ID3-B
	E	ID2-C	ID4-C	ID3-G	ID3-C
	F	ID2-A	ID4-A	ID3-E	ID3-A
	G	ID2-D	ID4-D	ID3-H	ID3-D

* Determined as discussed in paragraph 5.5.2.1.

Table 4.6 Playback Circuits L39, L90, Z2, and Z3.

Rev.18NOV68

4.2.4.4 Playback Circuit Z1

Unlike the playback of other tracks, the Z1 playback consists entirely of 1's bits. There are 5120 factory recorded 1's bits around the Z1 track. These bits induce a continuous voltage waveform across the Z1 playback head, 2 bit-times of this waveform are shown in figure 4.37. During the first 180 degrees of playback, the voltage at pin 2 of M138, shown in figure 4.38, goes positive with respect to pin 3. As a result, M138, a differential comparitor (amplifier), is turned on and driven high. (The operation of M138 is identical to the operation of M137 shown in figure 3.35 and discussed in paragraph 4.2.4.2.)

Its output, at pin 7, during this time is +2.5 volts or greater. As soon as the input at pin 2 is not positive with respect to pin 3, M138 turns off and its output drops to ground.

Assuming the M138 output, at pin 7, has been at ground for some time, then Q83 is off, CR82 is forward biased, Q84 is on, the voltage across C86 is negligible, Q97 is on, and Z1 is at +0.4 volts. When the M138 output goes to +2.5 volts, the base-emitter junction of Q83 is forward biased and Q83 turns on. Its collector voltage drops to +0.6 volts. CR82 remains forward biased. Due to its drop, the Q84 base drops to ground, reverse biasing its base-emitter junction. Q84 turns off. Instantaneously, current flows from +5 through R166, C86, and into the base of Q97, keeping it on. C86 charges to 4.4 volts (Q84 collector side of C86 is the positive-going side). Q97 remains on and the circuit remains in this condition until the M138 output drops from +2.5 to 0 volts. The base-emitter junction of Q83 is reverse biased, and Q83 turns off. Its collector goes positive to the point where current flows through CR82 into the base of Q84, turning on. As soon as Q84 is turned on, its collector drops to +0.6 volts. Since C86 has been charged to 4.4 volts, the voltage at the Q97 base jumps to -3.8 volts which immediately turns Q97 off. The Q97 collector, Z1 output, is pulled to +4 volts via the 91 and 300 ohm divider. Meanwhile, CR86 starts charging in the opposite direction through Q84, R379 in parallel with R164, and R165 toward 4.5 volts (Q97 base side of C86 is the positive-going side). As soon as C86 charges to the point where the Q97 base reaches +0.6 volts, Q97 turns back on and pulls Z1 back to +0.4 volts. R379 is adjusted, as described in paragraph 5.5.2.2, so that the +4 volt duration of Z1 is 200 + 20 - 0 nanoseconds. Since C86 uses the +5 volt supply as the current source when it charges in either direction, variations in the +5 volts do not affect the Z1 duration time.

Since the pulse repetition rate of Z1 is nominally 1 MHz, it requires a transmission line means of distribution. This is accomplished by physically keeping the Z1 printed circuit line between the +5 and ground printed circuit lines at all times except where Z1 goes directly into a gate (not shown on the schematic). The transmission line starts at the collector of Q97 and divides into 2 paths. One path remains on the D board. The

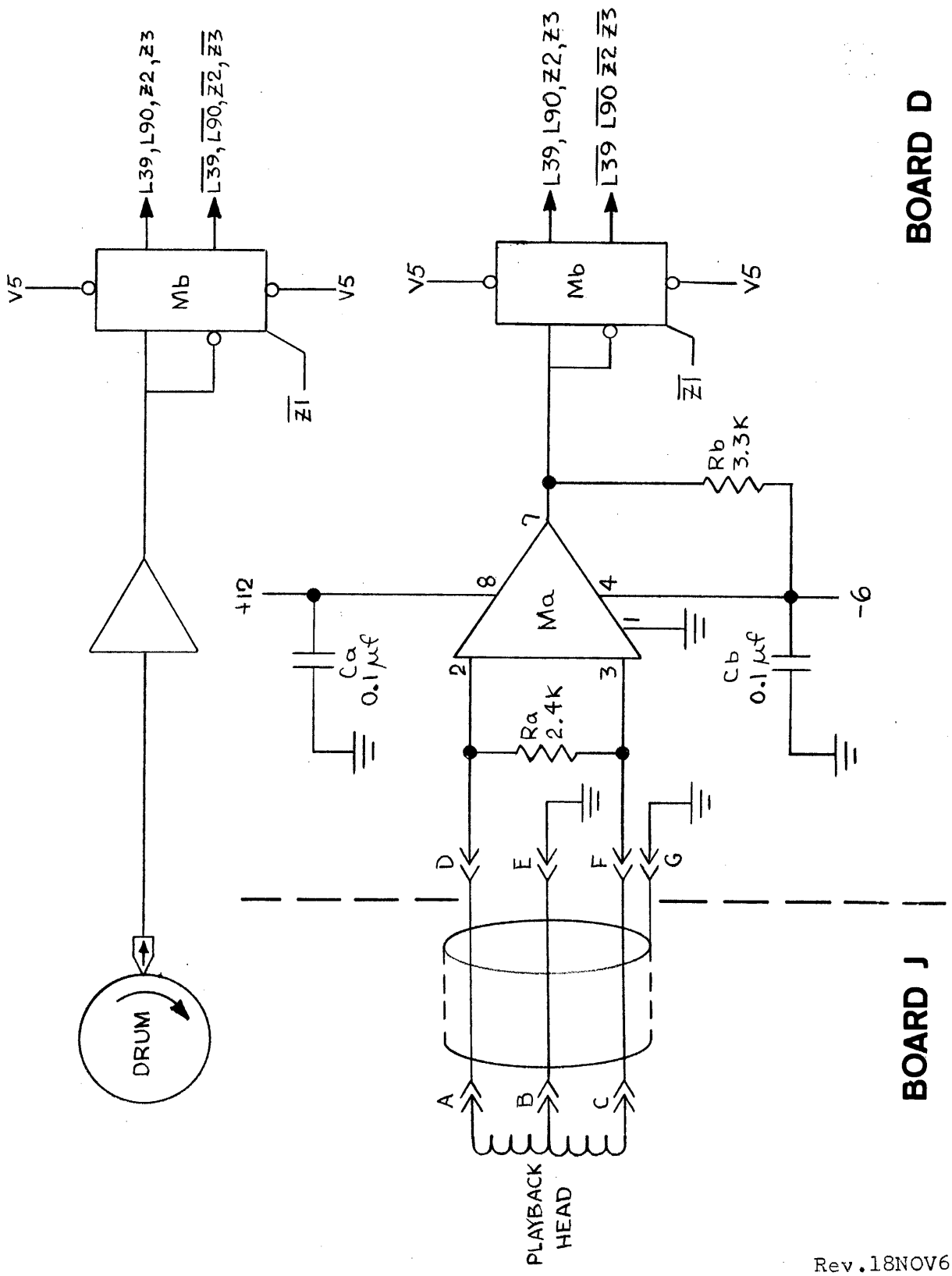


Figure 4.36 Playback Circuits L39, L90, Z2, Z3.

Rev.18NOV68

other path goes out, via a strip connector, to board C. Note that in the strip connector Z1 is still between +5 and ground. From board C the transmission line goes to board B, via a strip connector, and from board B it goes to A, via a strip connector. On board A the transmission line is terminated by a 300 ohm resistor to the ground line, and a 91 ohm resistor to the +5 line. A 0.1 mfd capacitor is across the +5 and ground line, thus AC tying the +5 and ground lines together. All other resistors and capacitors attached to the Z1 transmission line are to keep the shape of Z1 correct.

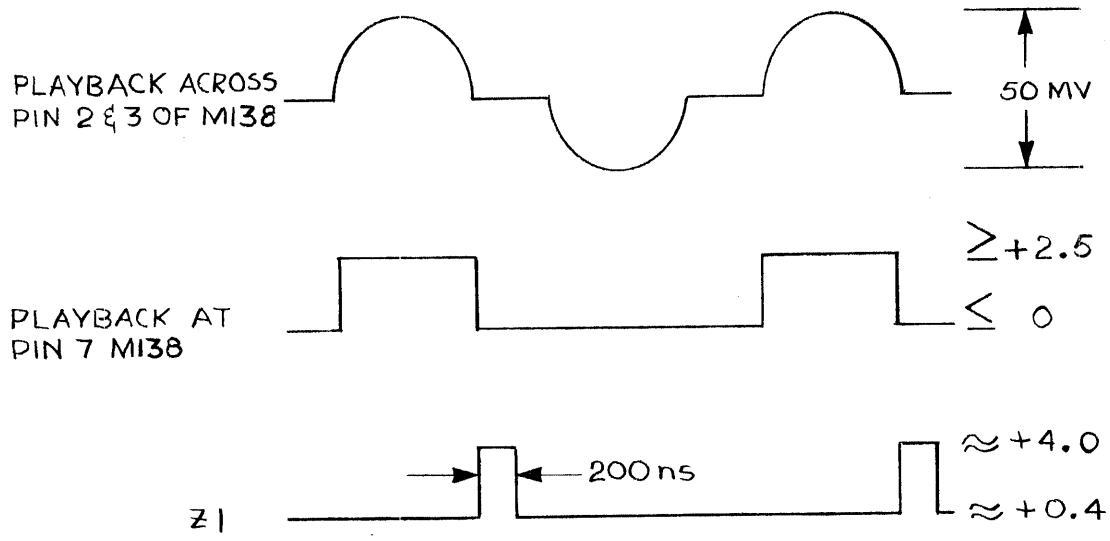
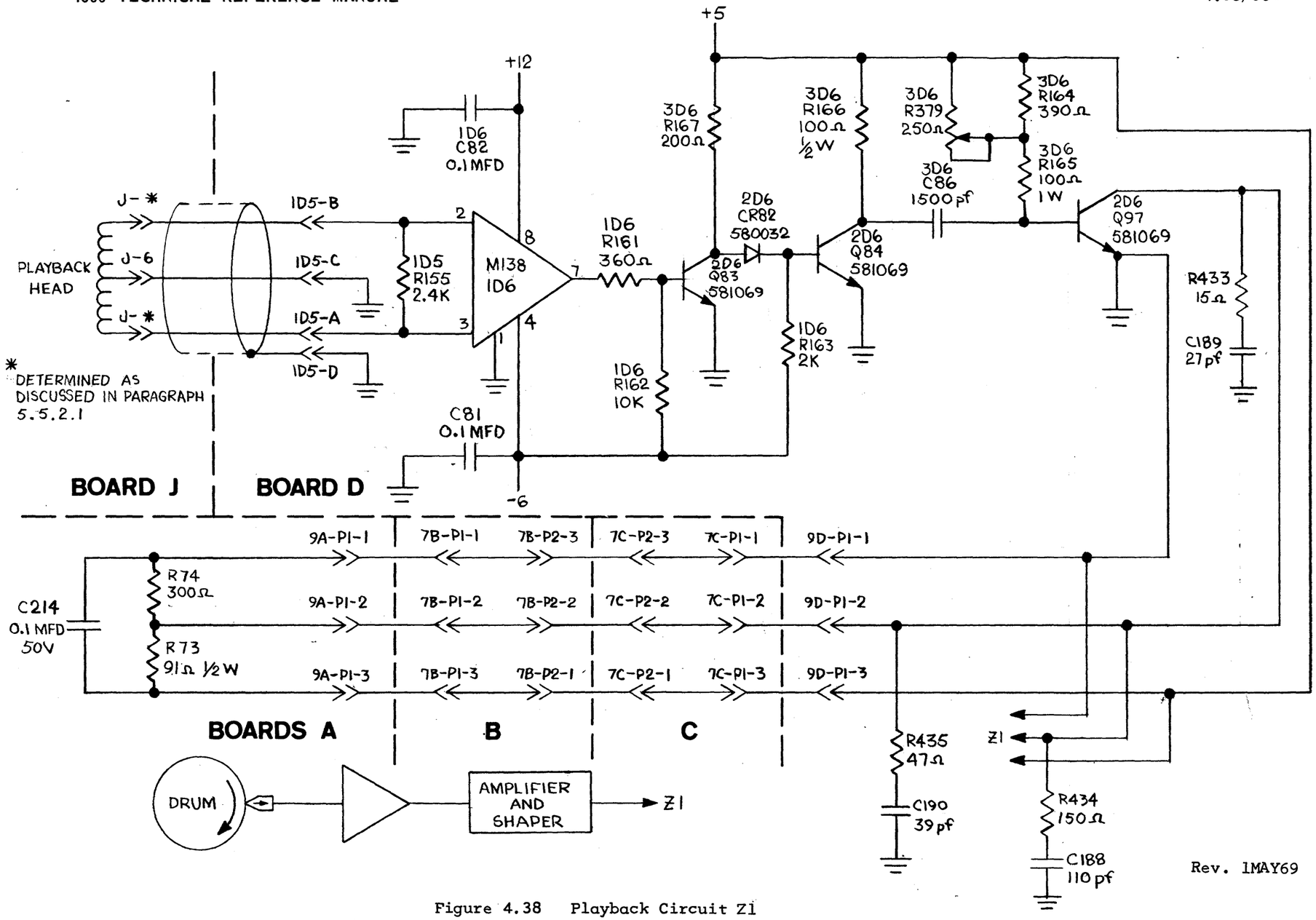


Figure 4.37 Playback Circuit Z1, Waveforms.



Rev. 1MAY69

Figure 4.38 Playback Circuit Z1

4.2.5 WARM-UP CIRCUIT

The warm-up circuit, shown logically in figure 3.97, has a twofold purpose. First, it controls a warm-up period for the processor whenever the processor is turned on. Second, while the processor is on, it maintains a constant check on the critical areas of AC/DC power, Z1 clock and drum speed. In the event that the check locates a failure in one of these areas, it forces the processor back into the warm-up state. When the processor is in the warm-up state, signal W1 is low (logical 0) while signals W2 and W10 are high (logical 1). W1 low prevents operation of the record circuits. W2 high forces a Jump Conditional command to the last memory address into the command register, and sets the K. W2 high also turns off the READY indicator light, via the logic circuits shown in figure 3.99. W10 high drives the W11O interface signal high (the W11O output circuit is discussed in paragraph 4.2.1.6). This, in turn, inhibits the operation of all I/O devices connected to the interface. When the processor is not in the warm-up state, W1 is high while W2 and W10 are low, allowing normal processor operation.

Figure 4.39 is a block diagram of the warm-up circuit. Each of the 9 blocks is referenced to a figure containing a schematic of the circuit represented by the block. As indicated by the block diagram, the warm-up circuit centers around the failure latch. This latch has two states; on (set) and off (reset). When set, W1 is low while W2 and W10 are high; when reset they are inverted. The state of the latch is controlled by 2 groups of circuits, the check circuits and the reset circuits. The check circuits act to set the latch when they locate a failure condition. Once the latch is set, the reset circuits are the only means by which it can be reset.

The +5 volt check circuit monitors the +5 volt supply. If it should drop below +4.7 volts, the +5 volt check circuit immediately sets the latch. (The need for this close tolerance is a result of the -0.5 volt tolerance on the +5 volt Vcc for the IC packages.) The Z1 clock check circuit immediately sets the latch in the event that the clock frequency drops below a failure threshold (somewhere between 850-925 KHz). Since the Z1 frequency is dependent upon the drum speed, the Z1 clock check circuit is indirectly checking drum speed. In the event that the AC line voltage should drop below 95 volts, the AC line check circuit sets the latch. In this case, the latch setting is delayed by the timing circuit until the end of the present word-time. This allows any recording operations to be finished out. The POWER button check circuit, via the timing circuit, sets the latch at the end of the word-time during which its pressed. This allows the word to be finished out -- the turn-off sequence when the POWER button is pressed to its off position allows this and also allows the latch to set at end of the word-time. The +35, +18, and -24 volt check circuit immediately sets the latch if these voltages drops below +32, +14, and -18 volts, respectively.

When the processor is initially turned on, the DC voltages are low and +5 volt and/or +35, +18, -24 volt check circuits immediately set the latch. The processor is designed so that the +5 volt failure condition ceases before the last of the other failure conditions. When the last of these other failure conditions cease, the initial start-up circuit is energized. About one second after being energized, it generates a latch reset pulse. Since the +5 volt failure condition should cease before the initial start-up circuit is energized, the reset pulse is free to reset the latch. If something goes wrong and the +5 volt failure condition does not cease before the generation of the latch reset pulse, the latch set signal generated by the +5 volt check circuit overrides the latch reset pulse. Thus the latch remains set and the processor remains in the warm-up state. If any of the other failure conditions should appear during the time that the initial start-up circuit is energized but before it generates the reset pulse, the initial start-up circuit is deenergized until the failure condition ceases, at which time it would energize and one second later generate a reset pulse. If the initial start-up circuit is prevented from resetting the initially set latch by a +5 volt failure, or if after it has reset the latch a failure condition sets the latch, then the only means for resetting the latch is by the READY button circuit -- after the failure condition ceases.

The READY button circuit generates a latch reset pulse whenever the READY button on the operator console is pressed. If a failure condition exists (latch set signal present) the reset pulse cannot override it. Hence, the processor remains in the warm-up state. When the button is pressed after the failure condition ceases (latch set signal not present) the reset pulse generated is free to reset the latch and take the processor out of the warm-up state. The operation of the READY button and its associated indicator light are discussed in greater detail in paragraph 2.3.

4.2.5.1 +5 Volt Check Circuit

This circuit, shown in figure 4.40, is basically a differential amplifier. When the +5 volts is not in a failure condition, the Q45-1 base is at +5 volts and the Q45-2 base is Zener referenced by CR49 to +4.7 volts. The Q45-1 base-emitter junction is forward biased, allowing current to flow from the +18 volt supply through R78, Q45-1, and R86. This places the Q45-2 emitter at +4.4 volts, turning it off. As a result, the Q40 base is at +18 volts while its emitter is at the Q45-1 collector level (+5 volts). Q40 is, therefore, turned off, placing the Q46 base at ground. With this base voltage, Q46 is unable to drive the line A positive, indicating a no-failure condition. If the +5 volt supply should drop below the +4.7 failure threshold voltage, Q45-2 turns on and holds the Q45-1 emitter at +4.1 volts. Since the +5 supply is

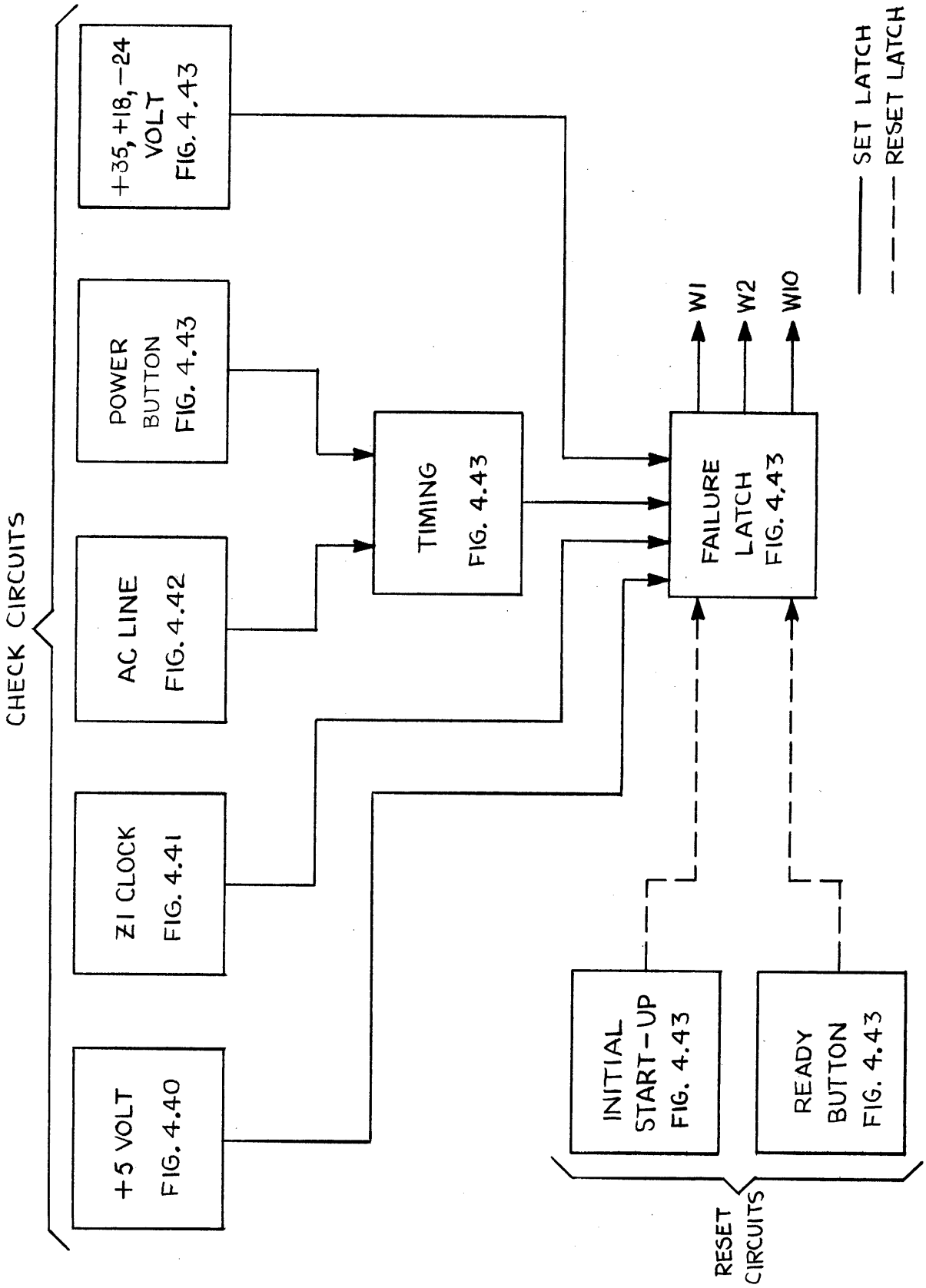


Figure 4.39 Block Diagram, Warm-Up Circuit.

below +4.7 volts, Q45-1 is off. The base of Q40 is at +4.7 volts due to the Q45-2 conduction. Since Q45-1 is off, the +18 volt supply pulls the Q40 emitter positive to the point where Q40 turns on. This raises the Q46 base voltage to +4.7 volts, turning it on and driving the A line positive (indicating a +5 volt failure condition).

Note that during normal operation CR30 is reverse biased. CR29 is forward biased and supplies current for Zener diode CR49. If a +35 volt failure occurs and the +35 volt supply drops below +18 volts, CR30 becomes forward biased and maintains current through CR49, thereby keeping the +4.7 volts Q45-2 base reference. In this case, the +18 volt supply maintains the entire +5 volt check circuit. This is required because, if the +35 volts disappears entirely, the +5 volt supply would also be lost since the +5 volts supply uses power from the +35 volt supply. Since the +35 volt check circuit uses IC logic, which requires the +5 volts, the +35 volt check circuit may not detect the total loss of the +35 volts. If this should happen, the +5 volt check circuit, being maintained by the +18 volt supply, detects the subsequent loss of the +5 volts, and generates a +5 volt failure signal (A line is driven positive).

4.2.5.2 Z1 Clock Check Circuit

This circuit, shown in figure 4.41, consists of a sawtooth generator, rectifier, and DC level detector. The sawtooth generator consists of the circuitry to the left of the CR22 anode shown in the figure. The rectifier consists of CR22, R106, and C226. The DC level detector consists of the remaining circuitry.

The sawtooth generator starts producing a voltage ramp on the trailing edge of the Z1 pulse. On the leading edge of the next Z1 pulse, the ramp is rapidly forced down to its initial starting level. The lower the Z1 frequency, the more time between trailing edge of one Z1 pulse and the leading edge of the next, and the greater the peak ramp voltage. The sawtooth waveform produced by the ramps between Z1 pulses is rectified. Since there is little loading on the rectifier, its DC output equals the peak ramp voltage. When the frequency of Z1 goes below the failure threshold, which is anywhere from 850-925 KHz, the rectified peak ramp voltage is great enough to turn on the DC level detector. This, in turn, drives line B to ground, indicating a Z1 failure condition.

Due to interal hysteresis of the DC level detector, its turn on level is at a higher voltage than its turn off level. This is necessary for 2 reasons. First, when the DC level detector turns on it increases the load on the rectifier, tending to decrease its output. Second, by having the turn on and turn off levels different, the DC level detector does not oscillate on and off if the Z1 frequency sits just at the failure threshold level.

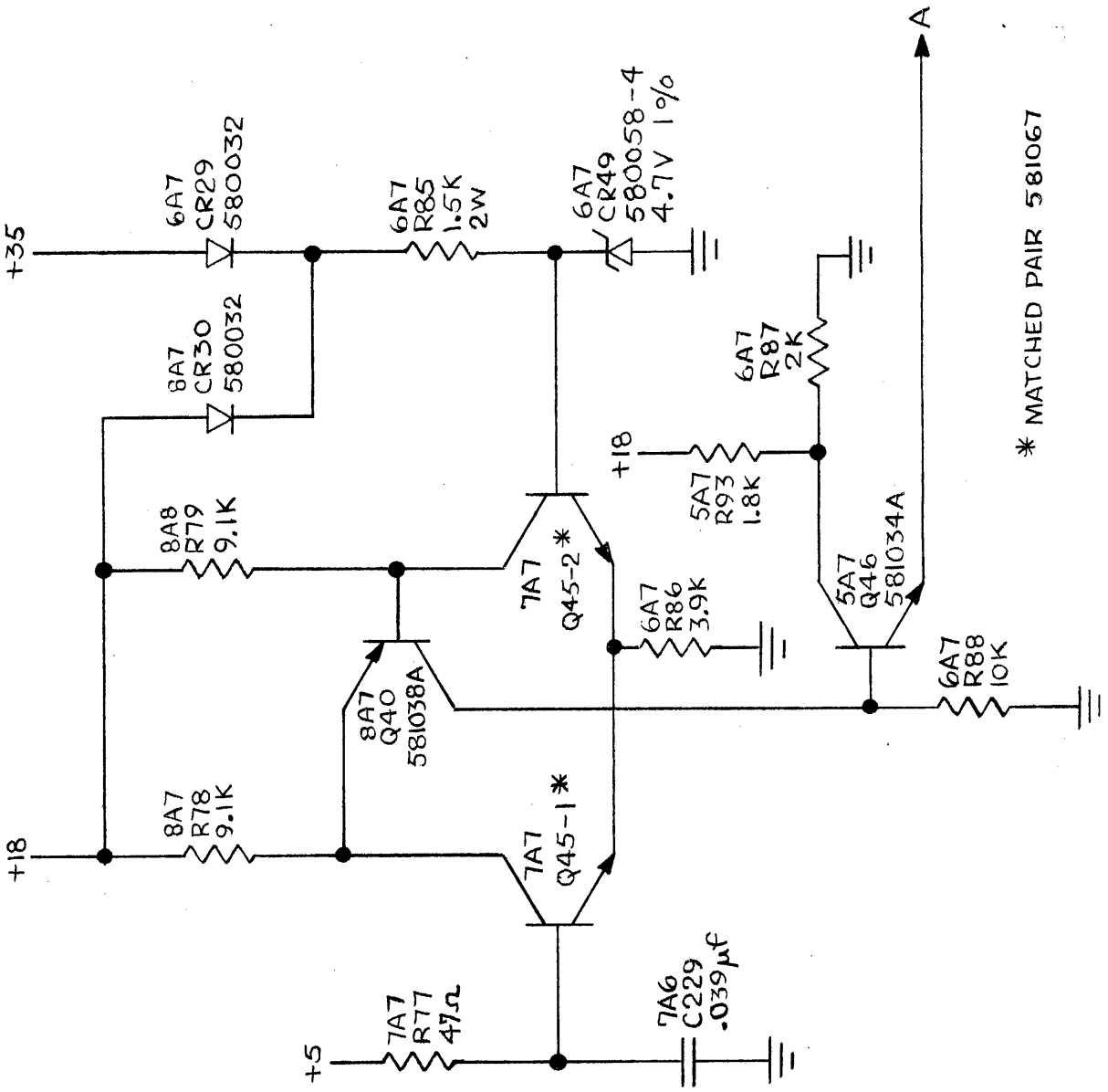


Figure 4.40 +5 Volt Check Circuit.

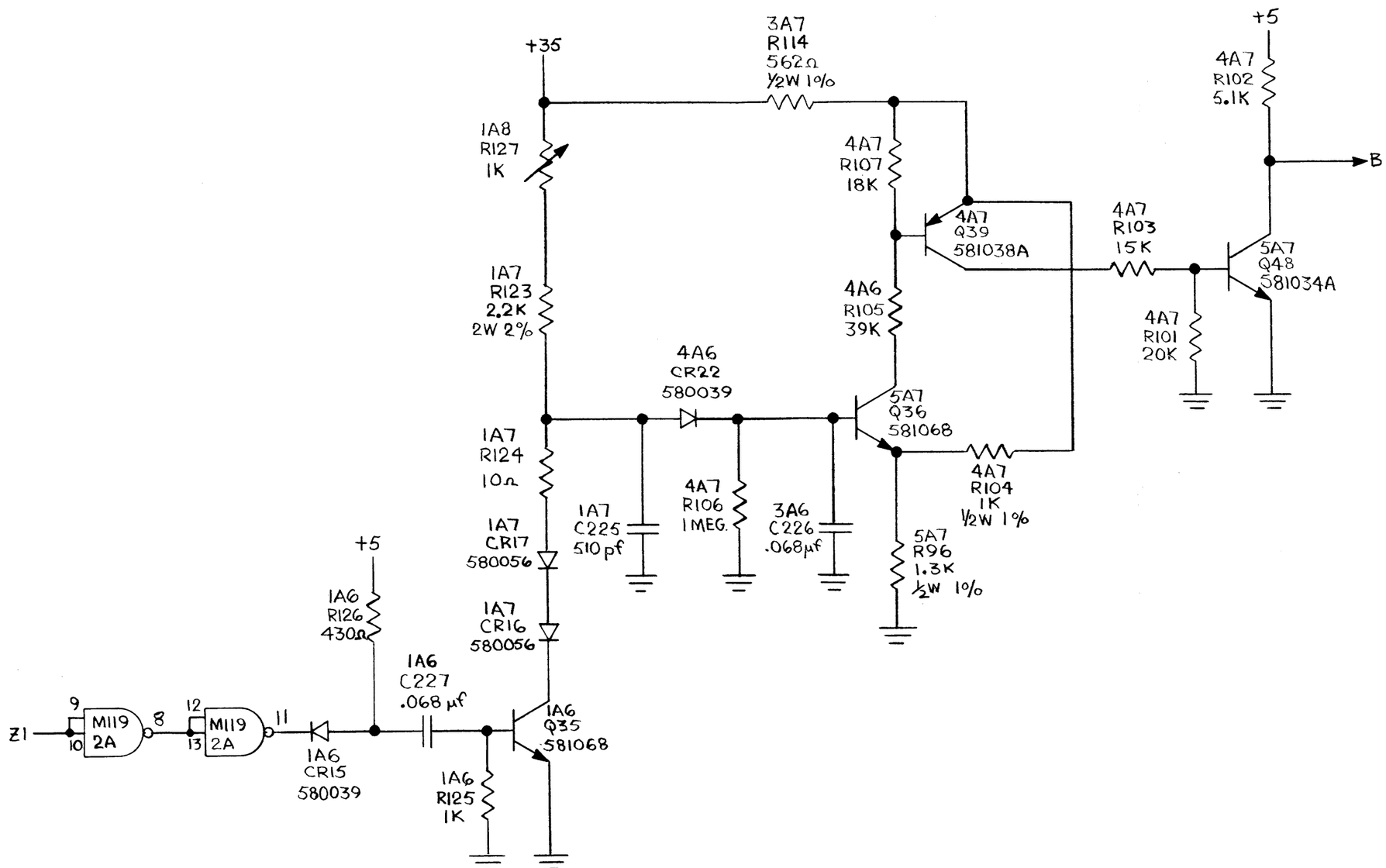
The Z1 pulse is double inverted by M119-8 and M119-11. Therefore, the output at M119-11 equals Z1. When the 200 nanosecond Z1 pulse is not present, the output at M119-11 is at ground and CR15 is forward biased. Both the Q35 base and emitter are at ground, holding Q35 off. When the 200 nanosecond Z1 pulse arrives, M119-11 goes toward +5 volts and CR15 is reverse biased. Instantaneously, current flows from the +5 volt supply through R126, C227 and into the base of Q35, turning it on. Due to the relatively long time-constant of R126 and C227 compared to the duration of the Z1 pulse, Q35 is kept on for the entire duration of the Z1 pulse. During this time the R123-R124 junction is pulled to +1.8 volts by the conduction of Q35. When Q35 turns back off on the trailing edge of the Z1 pulse, C225 starts charging toward +35 volts through R127 and R123. The amount of time C225 is allowed to charge depends upon how long Q35 is off (which depends upon the Z1 frequency). When the leading edge of the next Z1 pulse turns Q35 on, C225 is rapidly discharged down to +1.8 volts through the low resistance path of R124, CR17, CR16, and Q35. Assuming C226 is discharged, then when Q35 turns off, current will flow through CR22 and charge C226 in parallel with C225. When Q35 turns on and discharges C225, CR22 prevents C226 from also being discharged. The next time Q35 turns off, CR22 is forward biased when the charge across C225 reaches the charge across C226. C226 then increases its charge in parallel with C225. During a no-failure condition, the charge across is not positive enough to forward bias the base-emitter junction of Q36, thus, the only load across C226 is R106. R106 cannot discharge C226 to any great extent during the on time of Q35. Thus, the DC level at the C226-Q36 base junction rises to the peak level of the voltage ramp. With Q36 off, Q39 has no base drive and is turned off. With Q35 off, Q48 has no base drive and is turned off. Line B is pulled to +5 volts indicating a no-failure condition. The voltage at the Q36 emitter is +16 volts.

If a Z1 failure occurs, the ramp across C225 goes more positive, C226 charges more positive and exceeds the Q36 turn on threshold. With Q36 on, the Q39 base is pulled to the point when it turns on. Q39 on drives the Q48 base positive, turning it on. Q48 on drives the B line to ground, indicating a Z1 clock failure.

The Z1 clock circuit is adjusted by R127 so that if the Z1 frequency drops below a failure threshold, which can be anywhere from 850-925 KHz, the B line is pulled to ground. Before R127 can be correctly adjusted, the Z1 circuit must be properly adjusted, as described in paragraph 4.2.4.4, and the drum must be at its normal operating speed. The adjustment procedure is then as follows:

a. Adjust R127 for 0 volts at the Q48 collector.

b. Monitor the voltage across C226 and turn R127 slowly clockwise until the Q48 collector goes to +5 volts. At this point, note the voltage across C226.



BOARD A

Figure 4.41 Z1 Clock Check Circuit.

c. Continue turning R127 clockwise until the voltage across C26 is 1.25 volts lower than the reading noted in step b. The R127 adjustment is now complete.

4.2.5.3 AC Line Check Circuit

The AC line check circuit, shown in figure 4.42, is a single transistor circuit. During a no-failure condition, the AC check input from the processor's power supply is -24 volts. This reverse biases the Q115 base-emitter junction, keeping it off. Line C is unaffected. When the voltage across the primary of the power supply transformer goes below 95 VAC, the -24 volt AC check signal deteriorates toward ground and forces Q115 to turn on. Line C is pulled to ground, via R94 shown in figure 4.43, and indicates an AC line failure condition.

The AC line check circuit has one adjustment, R384. R384 is adjusted so that line C goes to ground when the voltage across the power supply transformer primary goes below 95 VAC.

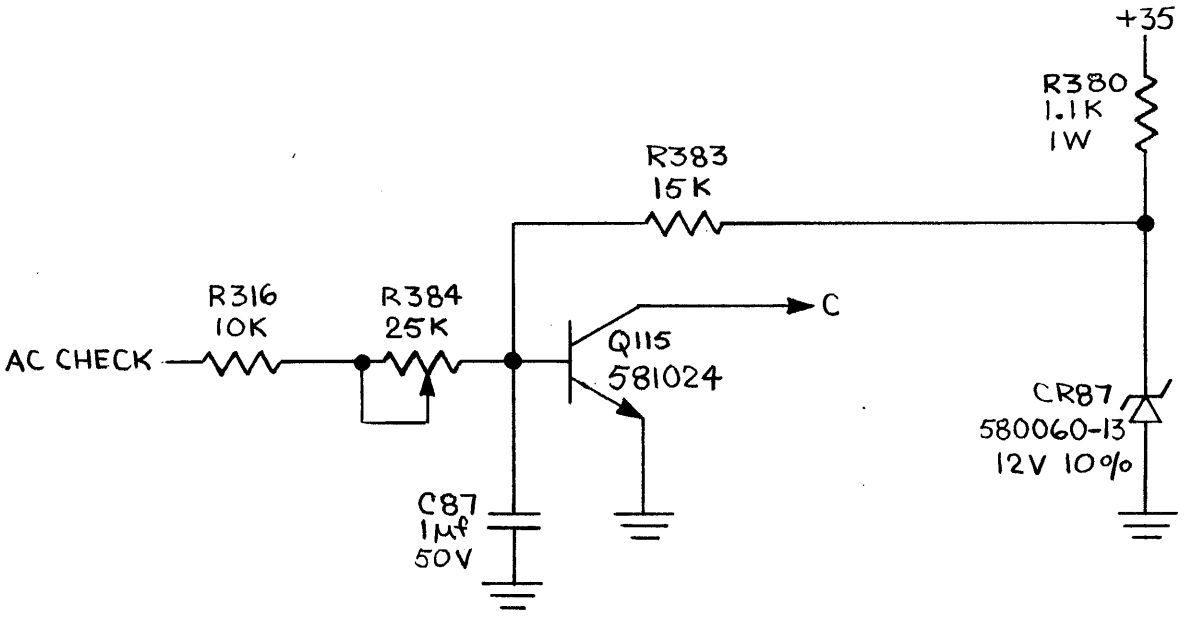


Figure 4.42 AC Line Fail Check Circuit.

4.2.5.4 +35, +18, and -24 Volt Check Circuits

The +35, +18 volt check circuit consists basically of Q13, Q14, and M119-3 shown in figure 4.43. Under a no-failure condition, the voltage at the Q14 base is +7.4 volts and the voltage at the Q13 base is +8 volts. Since emitters of Q14 and Q13 are tied to the +5 volt supply, both transistors are off and their collectors are at ground. The output of M119 is at +5 volts, indicating a no-failure condition. If the +35 volt supply drops below +32 volts, or if the +18 volt supply drops below +14 volts, the voltage at the Q14 base or Q13 base, respectively, drop to the point where the transistor turns on. This places the Q14-Q13 collector junction at +4.4 volts, which forces the output of M119-3 to ground, indicating a failure condition. CR18 and CR21 are protection diodes. They prevent the +35 and +18 volts lines, in the event of a failure, from pulling excessive emitter-base current through Q14 and Q13. CR53 and CR52 are used to drop 10 volts from the +35 and +18 volt inputs, respectively. C186 and C185 are noise filters.

The -24 volt check circuit consists basically of Q47, shown in figure 4.43. Under a no-failure condition, CR50 and CR51 drop the -24 volts to -4 volts at the Q47 base. Q47 is reverse biased and line B is unaffected. If a -24 volt failure occurs (-24 supply drops below -18 volts), the Q47 base voltage goes positive, turning Q47 on. Q47 then pulls line B to ground, indicating the failure condition. C187 is a noise filter.

4.2.5.5 POWER Button Check Circuit

The POWER button check circuit consists of S7-B and R94, shown in figure 4.43. While the processor is on, S7-B is open and does not affect line C. When the POWER button is pressed to its off position (considered as a failure condition), the contacts of S7-B make before the contacts of S7-A, which control the processors power supply, break and turn off the power. As a result, line C is pulled to ground before the processor's power is turned off and decays. The capacitor across the S7-B contacts is used to reduce contact bounce noise.

4.2.5.6 Failure Latch Circuit

The failure latch circuit consists primarily of Q37 and Q41, shown in figure 4.43. Since the conduction of one transistor forces the conduction of other, both transistors are either on (latch set) or off (latch reset). During a no-failure condition, line A and the Q37 base are at -0.6 volts. Q37 is therefore reverse biased and off. Its collector is at +19.2 volts, keeping Q41 off. With the latch in the reset state, CR28 is reverse biased and the Q43 base is held positive with respect to its emitter by the +11.8 volts at the anode of Zener diode CR48. Q43 is on and pulls current through CR44, forward biasing it. Current is also pulled through the base-emitter junction of Q42 by Q43. Q42

is turned on and supplies 90 ma to W1, allowing operation of the record circuits. As a result of Q41 being off, W10 is at -15 volts and does not inhibit the operation of any of the I/O devices. Q50 is off and, providing that the reset button is not being depressed (input R to M172-6 at ground), both inputs to M132-11 are at +5 volts. W2 is at ground and does not affect the processor's operation. During a failure condition line A is pulled positive by one or more of the check circuits. The Q37 base-emitter junction is forward biased. Q37 turns on and forward biases the Q41 base-emitter junction. Q41 is turned on and, in turn, maintains the Q37 base positive even after the actual failure has been cleared up. With Q37 on, current is pulled through CR48, R83, and CR28, thereby removing the base drive of Q43, forcing it off. With Q43 off, CR44 is reverse biased, the Q42 base is at +18 volts, and Q42 is off. This removes the W1 drive to the record circuits and prevents their operation. Since Q41 is on at this time, W10 is pulled to +17.4 volts, inhibiting all the processor's I/O devices. CR23 is forward biased, the Q50 base-emitter is forward biased, and the Q50 collector pulled to ground. This forces W2 (regardless of the M172-6 output) to +5 volts which forces a Jump Conditional command to the last memory address into the control loop, and set the K.

Due to the collector-base feedback of Q41 to Q37, and vice versa, once the latch is set by one of the check circuits it maintains line A positive regardless of whether or not any of the check circuits continue to supply drive. In order for the latch to be reset, the CR26 anode must be driven to ground by the reset circuits to reverse bias it and open the Q41 collector to Q37 base feedback path. If one of the check circuits is driving line A positive, Q37 remains on and keeps Q41 on despite the loss of Q41 to Q37 feedback. If line A is not being driven positive, the Q37 base is pulled negative by the -24 volt supply, forcing Q37 off. Its collector goes positive and forces Q41 off, resetting the latch.

4.2.5.7 Failure Latch, Untimed and Timed Set Circuits

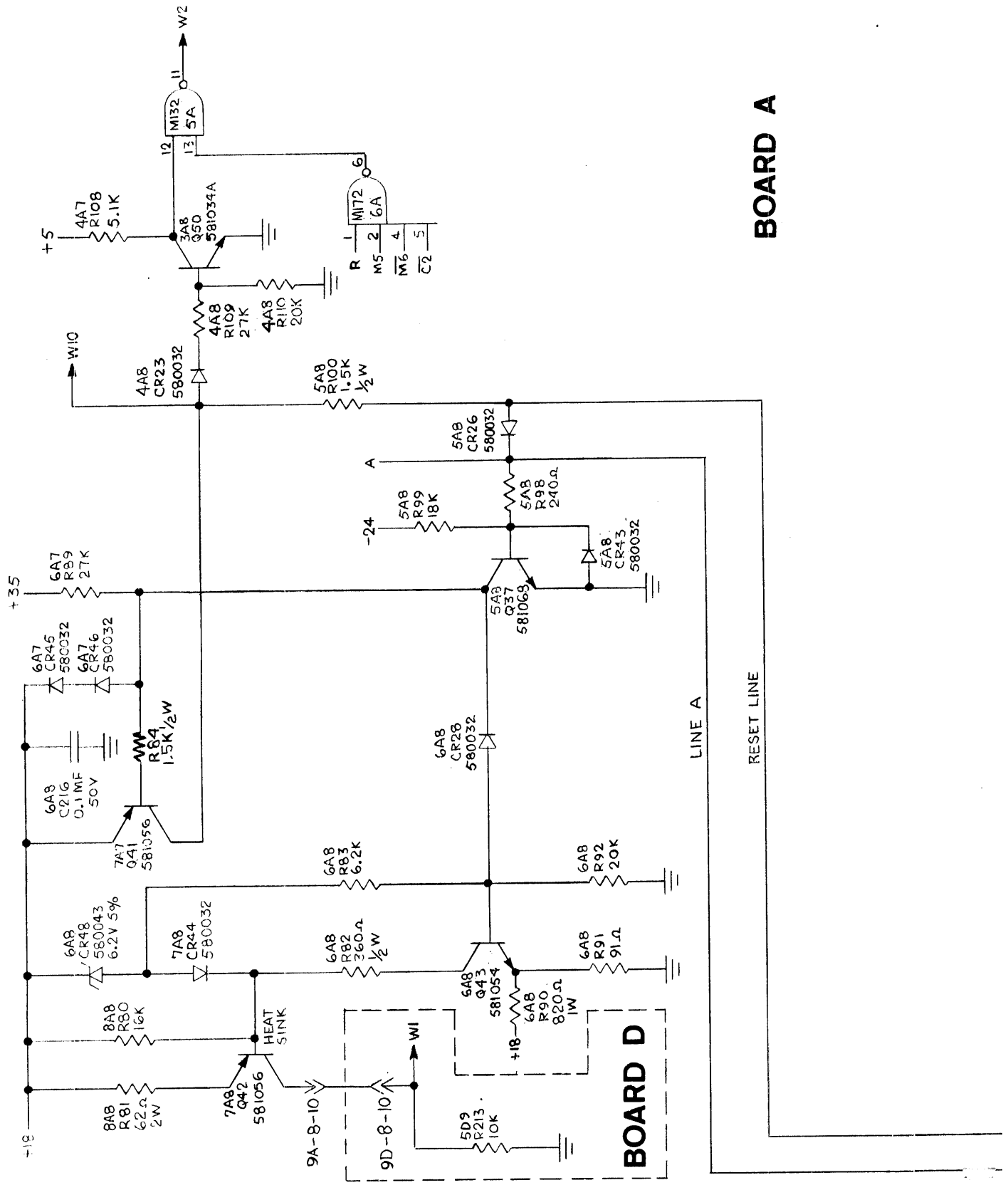
In the event of a +35 volt, +18 volt, Z1 clock, -24 volt, or +5 volt failure, the failure latch is immediately set. A +35 or +18 volt failure forces the output of M119-3, shown in figure 4.43, to ground. This ground forces the output of M122-8 to +5 volts. CR27 is forward biased and the failure latch set. The ground at the output of M119-3 also forces the output of M173-12 to +5 volts, which results in the output of M173-8 and M132-3 being forced to +5, preventing a reset signal from being generated. A Z1 clock failure or a -24 volt failure forces pin 9 of M122-8 to ground, which forces its output to +5 volts, and thus sets the failure latch. The M173-12 output is also forced to +5 volts, which again prevents a reset signal from being generated. A +5 volt failure causes Q46 to drive line A positive, thereby setting the failure latch. If a reset signal is present (output of M132-3 or M173-8 at ground) CR26 is reverse biased, preventing its interference with the setting of the latch. In addition, if the output of M122-8 is at ground, CR27 is reverse biased to prevent its interference with the setting of the latch.

In the event of an AC power failure or when the POWER button is turned off, the setting of the latch is delayed until the end of the present word-time if general storage recording is taking place. When either condition occurs, pin 1 of M173-12 is forced to ground, forcing pin 13 of M172-8 to +5 volts. When signals $\overline{T4}$, $\overline{L41}$, and $\overline{T7}$ are all at +5 volts (end of present word-time if recording is taking place), the output of M172-8 is forced to ground. This forces the output of M122-8 to +5 volts, and thus sets the failure latch. The +5 output of M173-12 forces the M132-3 output to +5 volts, preventing a reset signal from being generated.

4.2.5.8 Failure Latch, Reset Circuits

When the processor is initially turned on, the failure latch is set by the low DC voltages. During this time, the output of M122-8 is positive so that the Q51 base-emitter junction is forward biased, via line E. Q51 is on, its collector is at +0.6 volts and C230 is discharged. The Q49 base-emitter junction is forward biased, and Q49 is on. Its collector voltage is at ground, resulting in the M132-3 output being at +5 volts, which has no affect on the latch. As the processor warms up, the various failure conditions cease. As soon as the +35 volt, +18 volt, Z1 clock, and -24 volt failure conditions cease, all the inputs to M173-12 go to +5 volts, forcing its output to ground. The same is true of the M122-8 output. The ground at the M122-8 output turns Q51 off. C230 starts charging via R122. As it charges, the Q51 collector goes positive, CR20 is reverse biased and unilateral switch Q38 is open. When C230 charges to the point where the Q51 collector is +8 volts, Q38 closes and the Q51 collector voltage drops to +1.2 volts. This negative-going shift passes through CR20 and C228, momentarily turning Q49 off. The Q49 collector goes to +5 volts. Since the output of M173-12 is ground, both inputs to M132-3 are now at +5 volts, forcing its output to ground. If the +5 volt supply is operating normally, it will by this time be up to its no-failure level and not driving line A positive. The ground at the M132-3 output forward biases CR24 and pulls the anode of CR26 to ground, reverse biasing it and breaking the latch feedback path. The latch resets. If the +5 volt supply had failed, then line A would be positive and maintain the latch set. Note that once Q38 closes, it remains so until the processor is turned off. Thus, this circuit generates only an initial reset pulse even if failures occur.

If the failure latch is set after this initial pulse is generated, or if the initial reset pulse is prevented by a +5 volt failure from resetting the latch, then the READY button must be used to reset the latch after the failure condition has ceased. Assuming the failure condition has ceased and the READY button is pressed, pin 5 of M132-6 is momentarily forced to ground. Its output pulls line R to +5 volts. This, in turn, places pin 9 of M173-8 at +5 volts. Since pin 11 of M173-8 is at +5 volts (due to the assumption that the failure has ceased) and pin 10 is at +5 volts during the time the READY button is held down, the output of M173-8 is forced to ground. This, in turn, keeps the


BOARD A
BOARD D
W2
M132 5A
M172 6A
+5
4A7 R108 5.1K
3A8 Q50 581034A
4A8 R109 27K
4A8 R110 20K
W10
4A8 CR23 580032
5A8 R100 1.5K ½W
5A8 CR26 580032
A
5A8 R99 18K
5A8 R98 240Ω
-24
5A8 CR43 580032
5A8 Q37 581069
+35
6A7 R89 27K
6A7 CR45 580032
6A7 CR46 580032
6A8 C216 0.1 MF 50V
R64 1.5K ½W
7A7 Q41 581056
6A8 CR28 580032
LINE A
RESET LINE
6A8 R83 6.2K
6A8 R92 20K
6A8 CR48 580043 6.2V 5%
7A8 CR44 580032
6A8 R82 360Ω ½W
6A8 Q43 581054
6A8 R91 91Ω
8A8 R80 16K
HEAT SINK
6A8 R90 820Ω 1W
+18
W1
8A8 R81 62Ω 2W
7A8 Q42 581056
9A-8-10
9D-8-10
5D9 R213 10K
+19

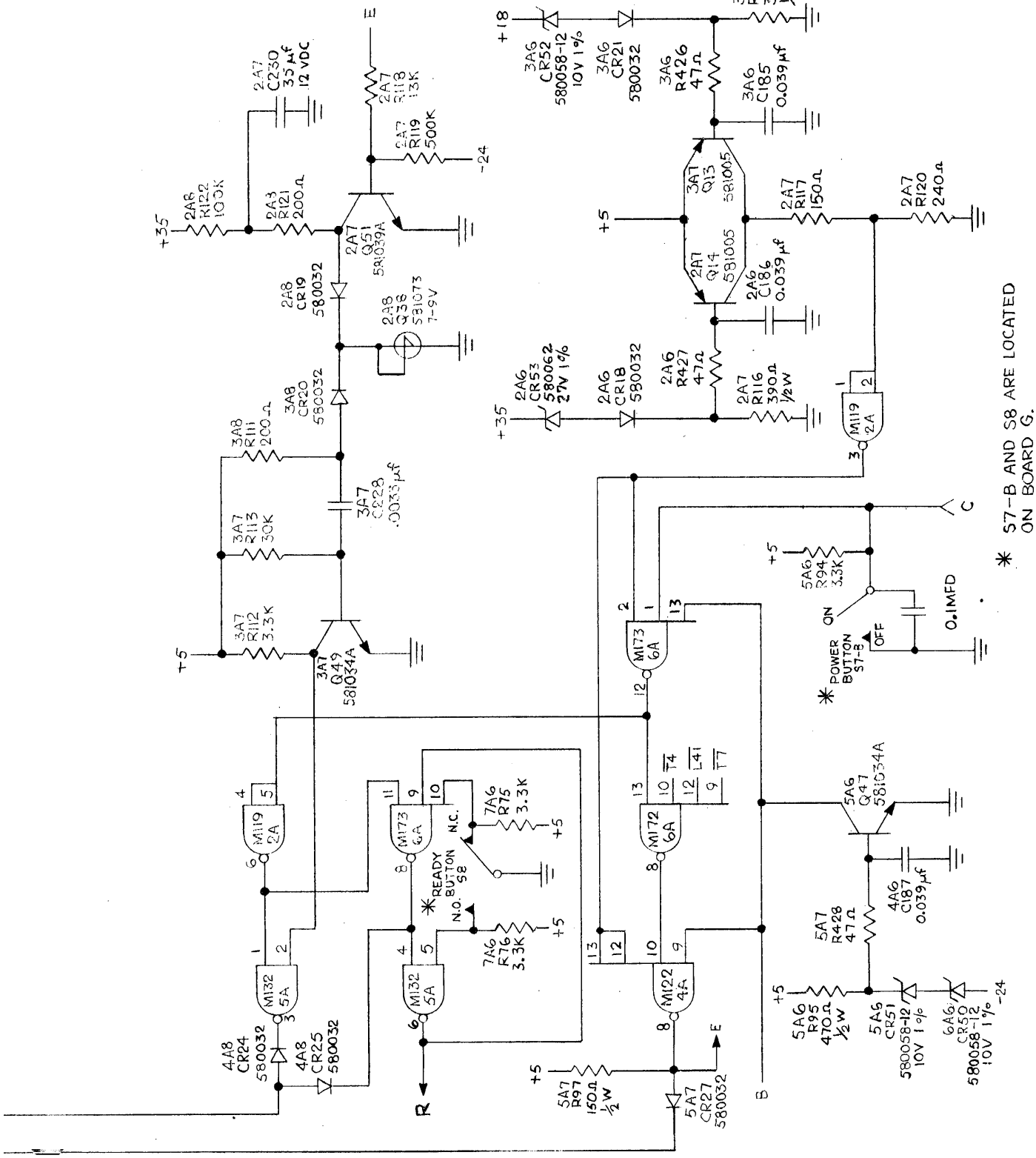


Figure 4.43 Warm-Up Circuits.

M132-6 output at +5 volts from the time that the READY button contact grounds pin 5 of M132-6 until the time it returns back to its normally closed position, grounding pin 10 of M173-8. This guarantees line D to be at +5 volts for at least one word-time. During this time, the ground output of M173-8 forward biases CR25 and reverse biases CR26, resetting the latch. Since D is at +5 volts, the output of M172-6 is forced to ground if M5, $\overline{M6}$, and $\overline{C2}$ are high (processor in idle mode). A ground at the M172-6 output forces W2 high for at least one word-time. If the READY button is pressed and a +5 volt failure condition is present, the operation of M132-6 and M173-8 remains the same. Since the W2 is high during a failure, D does not affect it. Since line A during a +5 volt failure is positive, the M173-8 ground output cannot reset the latch. If the READY button is pressed and any failure except +5 volts exists, the output of M119-6 is at ground. The M173-8 output is forced to +5 volts regardless of position of the READY button. Thus, a reset signal is not produced -- both CR24 and CR25 are reverse biased. The momentary +5 volt output of M132-6, when pin 5 is grounded, has no affect on W2, which is at +5 volts. (Note that purpose of M172-6 is to force W2 to +5 volts whenever the READY button is pressed while the processor is in the idle mode during a no-failure condition.)

4.2.6 AC/DC POWER

4.2.6.1 AC Power

The processor is available in 2 versions; an American version which uses 115-volt, 60 cycle power, and an European version which uses 230-volt, 50-cycle power. Though the AC wiring, shown in figure 4.44, of both versions is the same, each version has its own type of drum motor, fan motor, power relay, and fuses. In addition, the wiring of the power supply transformer primary differs for each version as shown in figure 4.45.

When the POWER button, shown in figure 4.44, is pressed to its on position, power relay K1 is energized and applies power to power supply transformer T3, the drum motor, and fan motor. Thus, the processor is turned on. When the POWER switch is turned off, K1 is deenergized and power is removed from the power supply, drum motor, and fan motor, turning off the processor.

4.2.6.2 DC Power Supply

The DC power supply, shown in figure 4.45, supplies the processor with all of its DC power. It consists of a constant voltage transformer, T3, and 5 full-wave bridge rectifiers. The constant voltage transformer consists of completely isolated primary and secondary windings, with a magnetic shunt added to the core. The magnetic shunt is controlled by

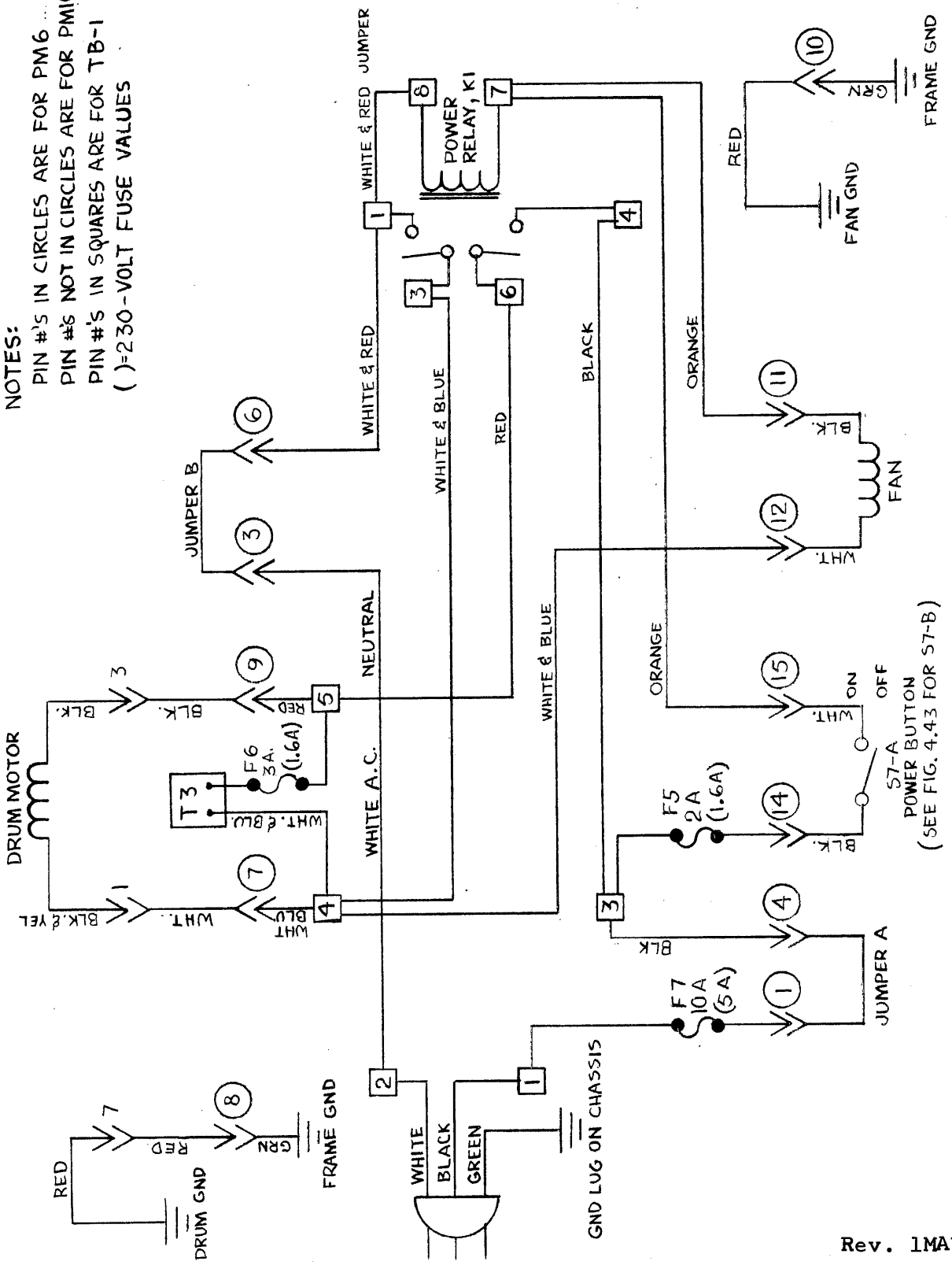


Figure 4.44 AC Wiring.

Rev. 1MAY69

C105 so that the operating point is placed above the knee of the primary voltage-versus-flux curve, which produces a greatly reduced change in flux density for any change in primary voltage. Consequently, the secondary is much less affected by any change in primary current, increasing stability for normal operation.

On the secondary side of T3 are 4 windings which feed the rectifiers of the +35, +18, and +13 volt supplies. The output of each rectifier is RC filtered and fused. The +13 volt supply is used only to provide power to the +5 volt regulator. The tolerance specified on the schematic for the output of each supply takes into account a ±20 volt tolerance on the 115 VAC input to T3 (±40 volts for 230 VAC input to T3). With the input to T3 exactly 115 VAC and all loads nominal, the output of these supplies is within ±3% of their nominal values. The worst case ripple is 2%, based on the peak to peak value, with the exception of the +13 volt supply which is 5%, based on the RMS value. Because of the constant voltage characteristics of the transformer, difficulties may be encountered in the field when attempting to vary the line voltage in order to obtain marginal test conditions. To solve this problem, phono jacks have been added to the circuits for +35, +18, and -24 volt supplies. Insertion of a standard phono jack with connections to a suitable Variac permits the output voltage of these supplies to be varied while temporarily cutting them off from the constant voltage transformer.

On the primary side of T3 is a winding used by the CR91-CR94 rectifier. The RC filtered output (-24 volts) of this rectifier is used by the warm-up circuit as a line voltage monitor. It has no other use. Since the winding for the rectifier of this circuit is on the primary side of T3, it does not have the constant voltage characteristics of the other windings. Thus, the output of this circuit is sensitive to variations in the line voltage, and for this reason serves as a line voltage monitor to the warm-up circuit.

4.2.6.3 +5 Volt Regulator

The +5 volt regulator circuit, shown in figure 4.46, is a series type regulator with remote sensing. Q100-1 and Q100-2 form a differential amplifier which compares the remotely sensed voltage to an exact +5 reference voltage. The output of the differential amplifier is proportional to the amount of error between the two. This output (error signal) is amplified by Q101 and Q118, and is applied to the Q99 base. Q99 controls the current flow through the load which is in series with it. The error signal at the Q99 base causes Q99 to either increase or decrease the current flow through the load in order to keep the remotely sensed voltage at +5 volts.

The +5 volt regulator has 2 protection circuits. One circuit, consisting of CR67, CR68, Q116, and Q117 protects the processor in the event that something fails and the +5 volt output of the regulator goes above

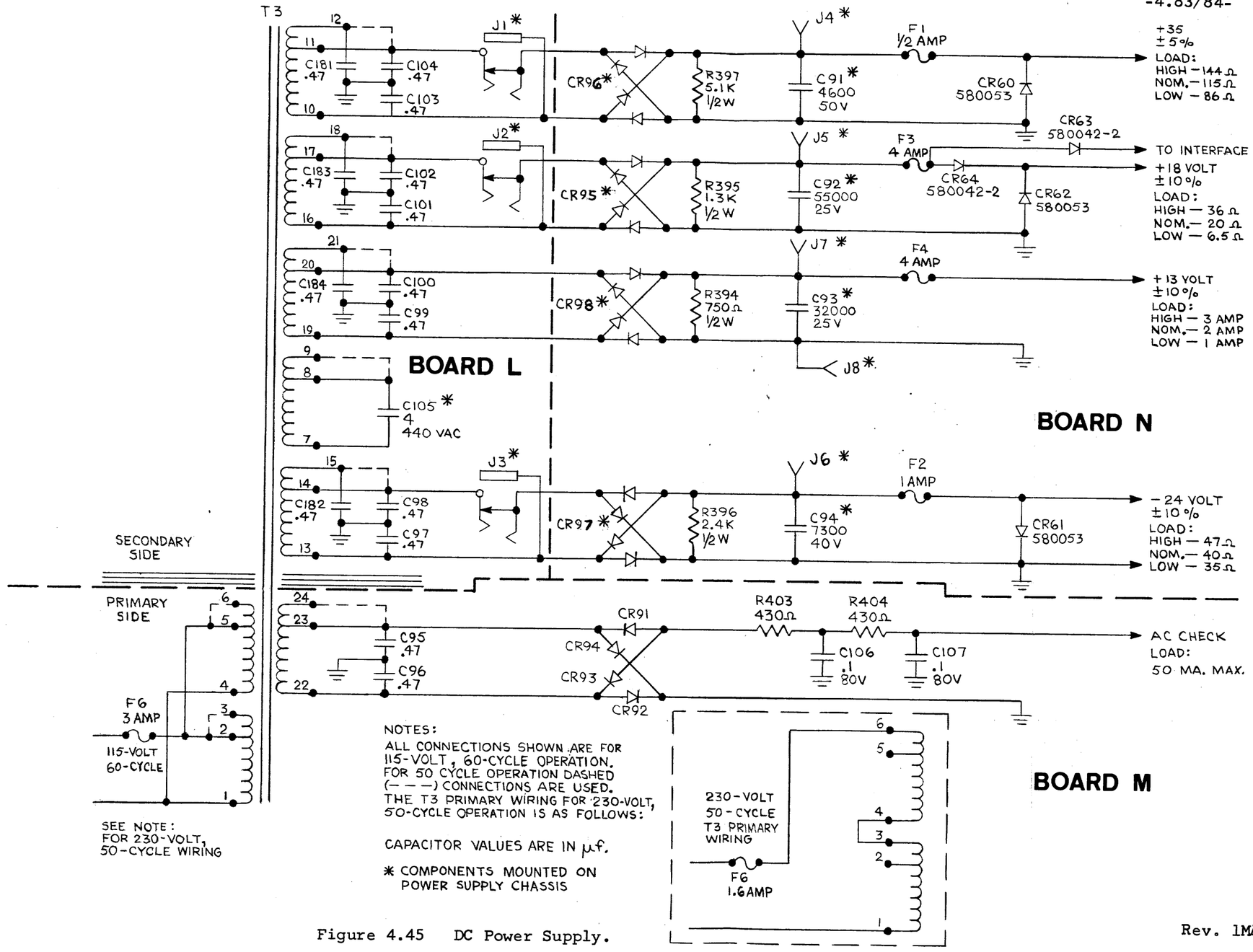


Figure 4.45 DC Power Supply.

+5.6 volts. The other protection circuit consists simply of CR69 which prevents the +5 volt output from dropping below ground.

The +5 reference voltage for Q100-1 and Q100-2 is supplied by CR66, CR65, and the resistive divider at the Q100-1 base. CR66 produces a regulated +12 volts. This is further regulated by CR65 which produces +6.2 volts. R385, R402, and R390 divide the +6.2 volts so that the Q100-1 base is at +5 volts. If the remotely sensed voltage is also +5 volts, the base-emitter junctions of Q100-1 and Q100-2 are equally forward biased and both transistors conduct equally. If the remotely sensed voltage goes above +5 volts, Q100-2 conducts harder, Q100-1 conducts less, and the Q100-2 collector voltage drops. The reverse is true if the remotely sensed voltage goes below +5 volts. Under normal operating condition, the remotely sensed voltage does not vary enough to turn either Q100-1 or Q100-2 off. C90 and R391 are used to reduce the response time of Q100-1 and Q100-2, thereby preventing oscillation.

The Q100-2 collector voltage controls the Q101 conduction. If this voltage goes positive, Q101 conducts less, and its emitter goes positive. The reverse is true if the Q101 base goes negative. The Q101 emitter voltage controls the conduction of Q118. The more positive the Q101 emitter, the more base current flows into Q118, and vice versa. Since Q118 is used as an emitter-follower, a small change in its base current produces a large change in its emitter current. This current change is further amplified by emitter-follower Q99, which controls the current flow through the load. Thus, if the remotely sensed voltage tries to go below +5 volts, the Q101 emitter goes positive, and the current flow through Q118, Q99 and the load increases and prevents the remotely sensed voltage from going below +5 volts. The reverse occurs if the remotely sensed voltage tries to go above +5 volts.

In the event that something fails, and the regulator output tries to go above +5.6 volts, the Q116 base-emitter junction, which is referenced by CR67, is forward biased, turning Q116 on. The R398 and R401 junction goes positive and causes Q117, an SCR, to turn on. As a result, the Q118 base is pulled low in an attempt to reduce the Q99 current flow and the output voltage. If something is wrong with either Q118 or Q99, and the output does not drop, CR68 which would normally be reverse biased by the 2 diode drops across Q118 and Q99, becomes forward biased. In this case, the SCR sinks all the output current until the fuse in the power source opens.

In the event that something fails and the regulator output tries to go below ground, CR69 becomes forward biased and clamps the output to ground.

R402 is adjusted so that the voltage across the sense inputs is 5 volts ±30 millivolts. If any one of the regulator components requires replace-

ment, the entire N board must be removed and a factory replacement installed. R402 is adjusted at the factory, it should at no time be tampered with.

When the processor is undergoing margin testing, the jumpers connected between pins 1 and 3, 7 and 9 of PM5 are removed. A variable resistor is connected between pins 1 and 7, allowing the +5 volt output to be varied as required by the test.

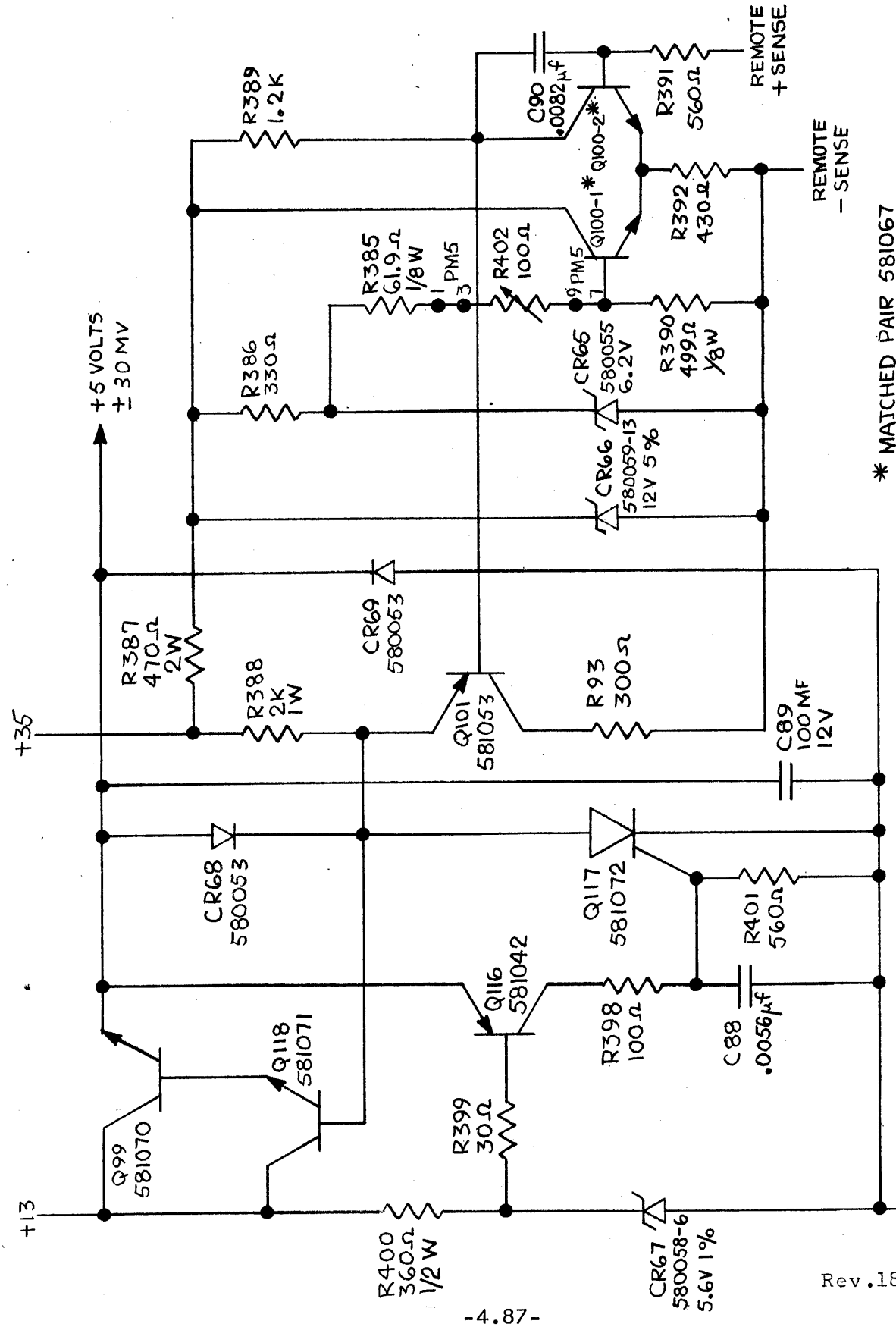


Figure 4.46 +5 Volt Regulator.

CHAPTER 5

MECHANICAL ASSEMBLIES

CHAPTER 5. MECHANICAL ASSEMBLIES.

5.1 HOUSING

The processor housing consists of a welded steel frame - the main chassis - with front, center and rear supports, base, tie plate and table top. The base supports the main chassis and the outside housing which is formed by removable side plates. The chassis also supports the power supply, drum assembly, printed circuit boards with tilt-out frames, the cooling fan and the operator console, which sits above a cutout in the table top.

Base and tie plate are mechanically isolated from the main chassis by Neoprene grommets that are pressed into holes in the main chassis. Steel sleeves within the grommets fit over studs welded onto the base plate, or they allow screws to pass through from the main chassis to the table top to secure it as shown in figure 5.1.

The outside housing consists of the two side and the front and rear covers, all of which are fastened to the base and the tie plate. The rear cover provides the only direct mechanical and electrical contact between the outside housing and the main chassis by having the rear cover of the power supply fastened directly to the rear cover of the processor housing. In this way, the housing is grounded at one point only to eliminate spurious ground current flow, which results in more effective shielding of the main chassis and its components. Good electrical contact between the base and cover is established by tabs on each cover. These tabs fit into slots in the base containing phosphor-bronze contact clips as shown in figure 5.2. Side covers are fastened to the tie plate at the top with captive retaining screws, while the front and rear covers are secured with removable screws at the top and at the base. The front cover is recessed for the air intake panel and filter.

A detent plate is mounted to the top of the tie plate, held in place with two mounting screws. The plate has two die-punched tabs at the end facing the air intake panel, and the plate is mounted in such a position that these tabs line up with dimples in the upper edge of the air intake panel. Hence, no mounting screws are required to hold the panel in place; the force exerted by the detent plate is sufficient to keep the panel secured. The filter is held to the inside of the air intake panel by a filter locking wire.

The rear cover has a face plate with a through-hole for the 32-pin Cannon connector of the standard interface. This connector is mounted to the

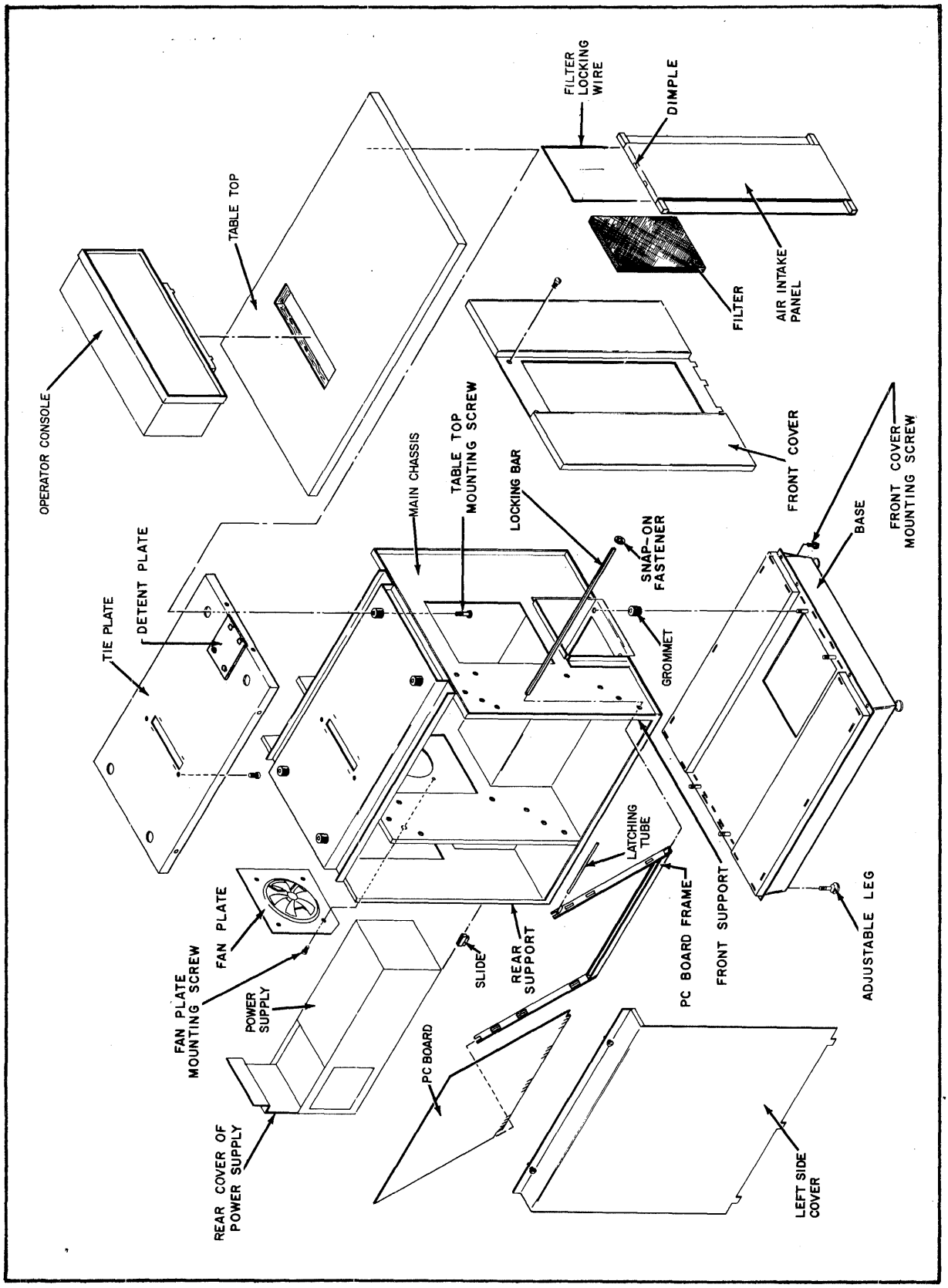


Figure 5.1 Housing.

rear cover of the power supply and it projects through the hole in the rear cover face plate. A cutout at the bottom of the plate allows the power line cord to pass through, see figure 5.3. The panel is held in place with two screws each at the top and bottom after the power supply is in place. The power supply rests on polypropylene slides that clip into the bottom of the main chassis, and its rear panel is fastened to the rear cover with two screws at the top.

Printed circuit boards A, B, C and D and their frames are suspended between two of the three vertical supports of the main chassis. The concavities of the two outer supports, as well as the underside of the tie plate, are lined with a styrofoam-type resilient material for noise absorption and to prevent inadvertent electrical shorting of leads against the chassis. The printed circuit board frames are supported at the bottom by locking bars that fit through holes in the front and center support. The ends of the locking bars are prevented from sliding sideways by snap-on fasteners at each end.

The four holes in each panel are staggered so that board frames can be folded out of the main chassis, after removal of the left side cover, without danger of having components contact each other when boards overlay. The side of each frame rests on the adjoining one with sufficient spacing between the side and each board to prevent components from touching ground or other components on adjacent boards.

The drum assembly is fastened to a base plate that sits above the center section of the main chassis. Four cutouts in the base plate allow it to be slipped over bolts inserted in the front and center supports of the main chassis. Bolts must be tightened after the drum base is in place to secure and to retain it.

The center support has a cutout similar to that of the other two supports; however, a fan mounting plate has been welded over this cutout. The fan mounting plate has an opening corresponding to the actual blade diameter of the fan and four mounting holes for attaching the fan plate. The fan is supported by four legs that are fastened with hollow rivets to the fan plate, and mounting screws pass through these rivets into the fan mounting plate. During operation, the fan draws air through the filter and through the cutouts in the front and center supports and that in the front cover. It then pushes the air over and around power supply components to eject it through the cutouts in the main chassis and base plate.

Access to the fan, drum assembly, printed circuit boards and/or power supply is obtained by removing the respective outer panels of the housing. The recommended procedure is listed under Disassembly. The housing must be firmly supported on a good surface, and the table top should be level and flush with those of other components of the data processing system. Therefore, the four adjustable legs, one of which is inserted at each

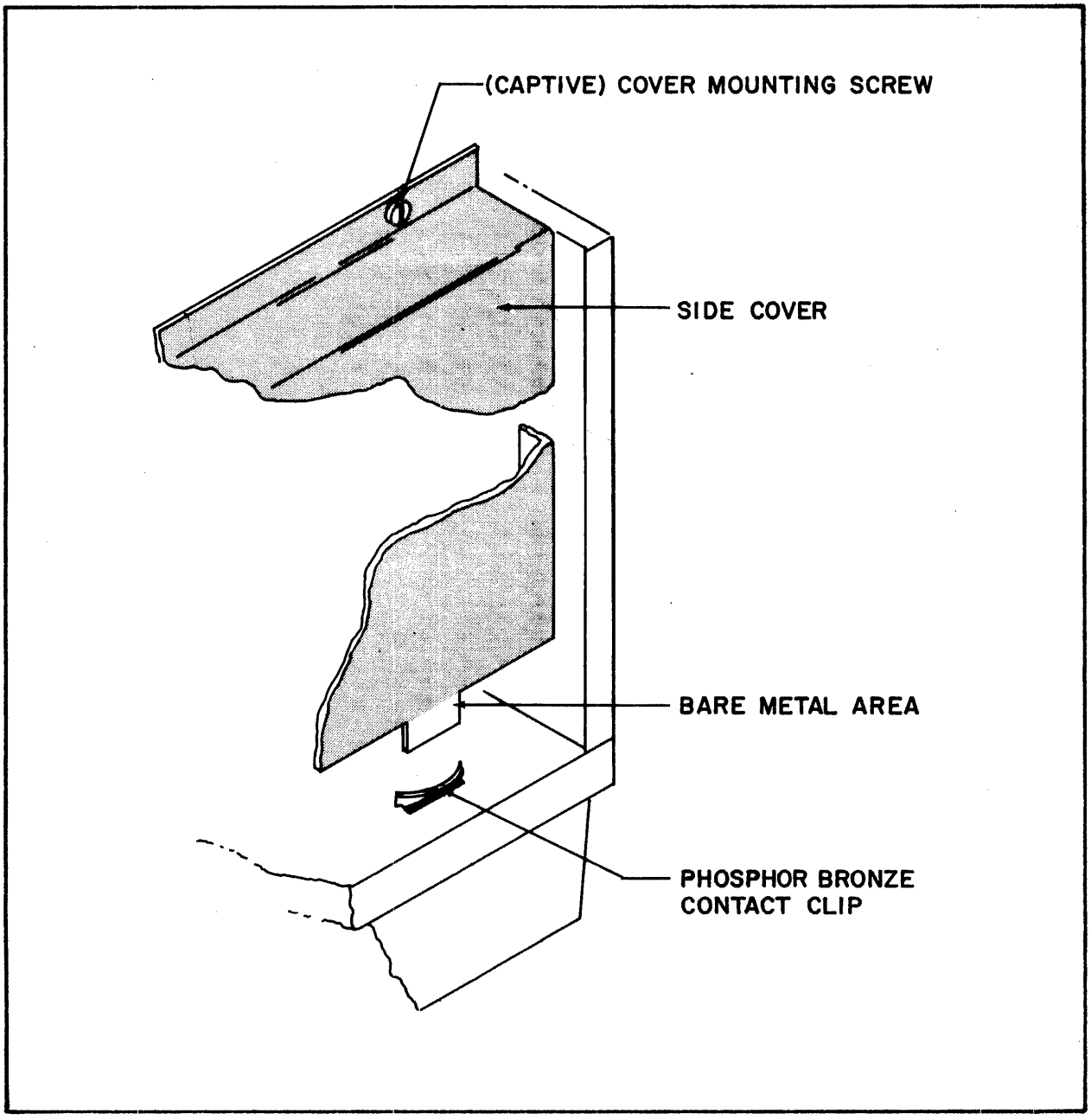


Figure 5.2 Cover Contact Arrangement.

corner of the base, should be set up at installation so that all four rest firmly on the floor, and so that the table top is level. The legs provide sufficient height adjustment to bring the table top in line with those of other system components.

5.1.1 DISASSEMBLY

Access to components within the processor housing is gained in the following manner:

To Printed Circuit Boards

1. Remove the left side cover by loosening the two captive screws at the top.

2. Pull the cover away from the housing and lift it to clear tab slots in the base.

3. Push the two latching tubes on board A out of the holes in the front and center support. Push tubes toward the middle of the board and move the board down and forward. Repeat this process with the other three boards.

4. Pull up the latching tube on board F to lift its lower end out of the bracket on the rear support. Then swing board F outward.

To Front of Power Supply

1. Insert a screwdriver tip between the upper edge of the air intake panel and the lower edge of the detent plate. Lift the plate and pull the air intake panel away from the processor housing.

2. Test jacks are now accessible for margin testing of circuits. Refer to figure for jack identification.

To Fuses in Power Supply

1. Remove the left side cover as outlined previously.

2. Fuses are located on the left side of the power supply, to the right of the center support.

To Rear of Power Supply for Removal

1. Turn power OFF. Remove the power line cord from the wall receptacle.

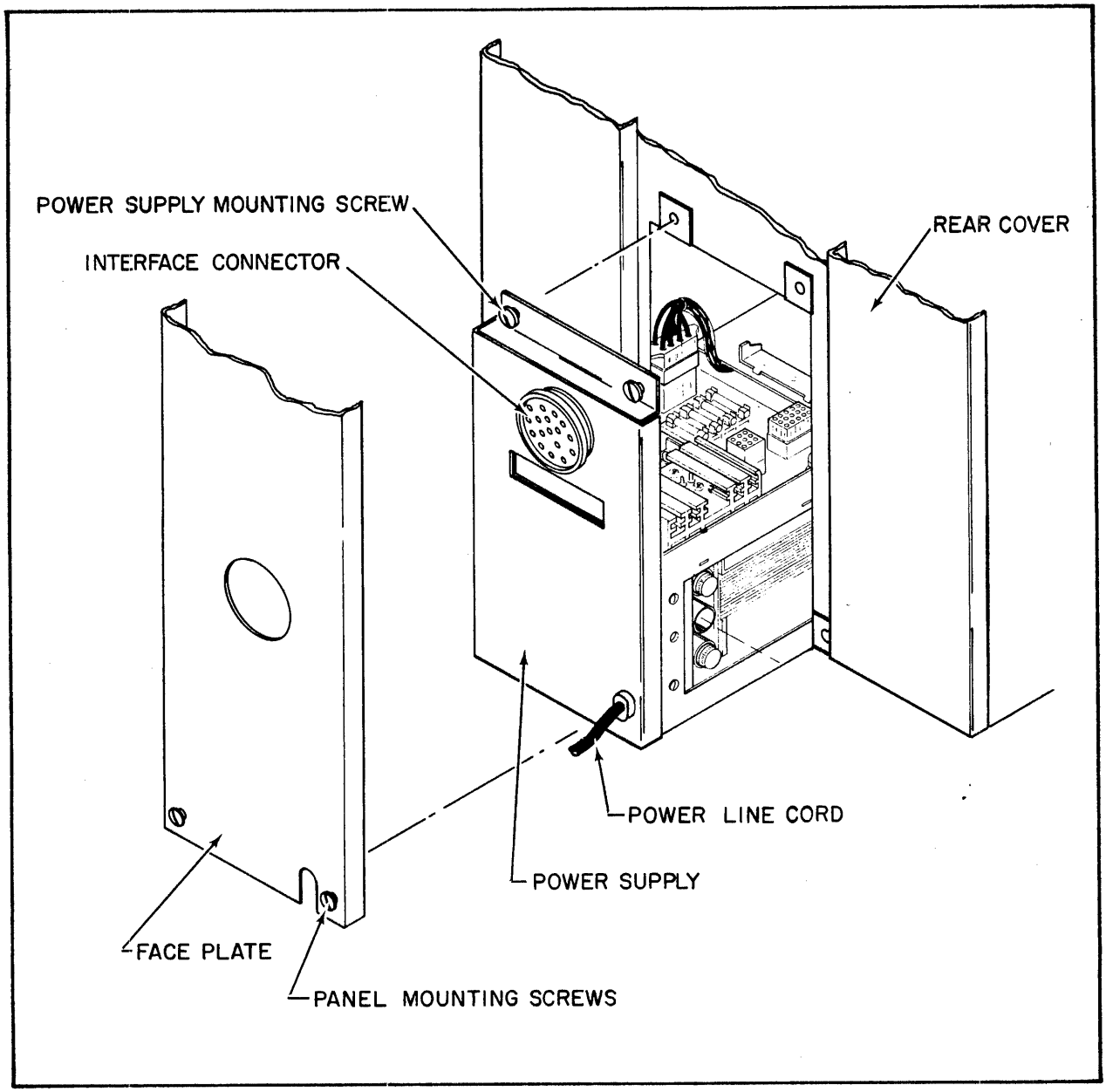


Figure 5.3 Rear Panel.

2. Remove the face plate from the rear cover by loosening the four captive screws.

3. Remove the rear cover in a manner identical to that described for the front cover.

4. Remove the four screws and nuts from the front and back of the interface connector. Nuts can be reached through the cutout in the rear support. Push the connector free of its hole. Remove the ground lug from the terminal next to the interface connector.

5. Remove the four connectors from the top and the one from the right side of the power supply. Remove the four ground lugs next to P6, see figure 5.12.

6. Remove the two screws from the top of the power supply rear cover. Pull the power supply out of the main chassis. Make sure that the interface connector clears all power supply projections during removal.

To Cooling Fan

1. Access to the fan can be gained by removing either the right or left side cover. If more than access is required, i.e., if the fan needs to be replaced, follow steps outlined in the following paragraphs.

2. Turn power OFF. Remove the power line cord from the wall receptacle.

3. Remove the face plate from the rear cover. Remove the rear cover.

4. Remove the four fan mounting screws from the fan mounting plate.

5. Disconnect fan motor leads. Replace the fan.

To Drum Assembly

1. Turn power OFF. Remove the power line plug from the wall receptacle.

2. Remove right and left side covers as outlined previously.

3. For drum assembly removal refer to paragraph 5.3.1.

5.2 OPERATOR CONSOLE

The operator console consists of a rectangular housing that supports the U-channel to which the switch assembly, the REGISTER SELECT switch, printed circuit board G with indicating lights, and associated components are mounted as shown in figure 5.4. The channel is fastened to the inside of the console housing. A cable harness interconnects the switches and printed circuit board. Flexible conductor cables carry signals and supply voltages between the circuit board and required connecting points on other boards or on the power supply.

An interlock switch at the rear of the U-channel senses the presence of the back panel. The switch is inoperative on 1601 processors; but, on 1602 models, it deactivates all other switches except K SET and RESET, STEP, RUN, READY and POWER when the panel is in place. The switch allows all console switches to operate normally while the back panel has been removed.

The REGISTER SELECT switch and its integral circuit board section fasten to the U-channel by locking the threaded portion of the switch against the channel. The shaft then projects through holes in the printed circuit board and front panel to support the SELECT knob.

The multiple switch assembly is held to the U-channel with several mounting screws. Knobs are pressed onto the ends of switch actuating rods. Program indicating lights project through holes in the printed circuit board. The two leads of each light are soldered at the rear to points on the circuit board. At the front, a lens holder is cemented to the rear of the front panel, and a lens is snapped into place at each indicating light position.

Edge-tab connectors provide electrical contact between printed circuit boards, the circuit board of the REGISTER SELECT switch and the cable harness. Connectors on the harness fit over the tab sections on the circuit boards. Connection to the main chassis is made via the flexible cable in the contact clamp. The clamp is suspended by the locking handle, which fits into cutouts in the contact clamp holder. The holder is mounted on two of the frame mounting screws and secured by tightening the two nuts.

Front panel switch and indicating light markings are shown in figure 2.1. The front panel fits into a groove in the four-piece frame as shown in figure 5.4, and this frame mounts to the console with screws from the front and nuts from within the console housing. Normally, neither panel nor frame require removal.

The base of the console sits on the tie plate to which it is fastened with two screws. The cutout in the table top allows the base to pass

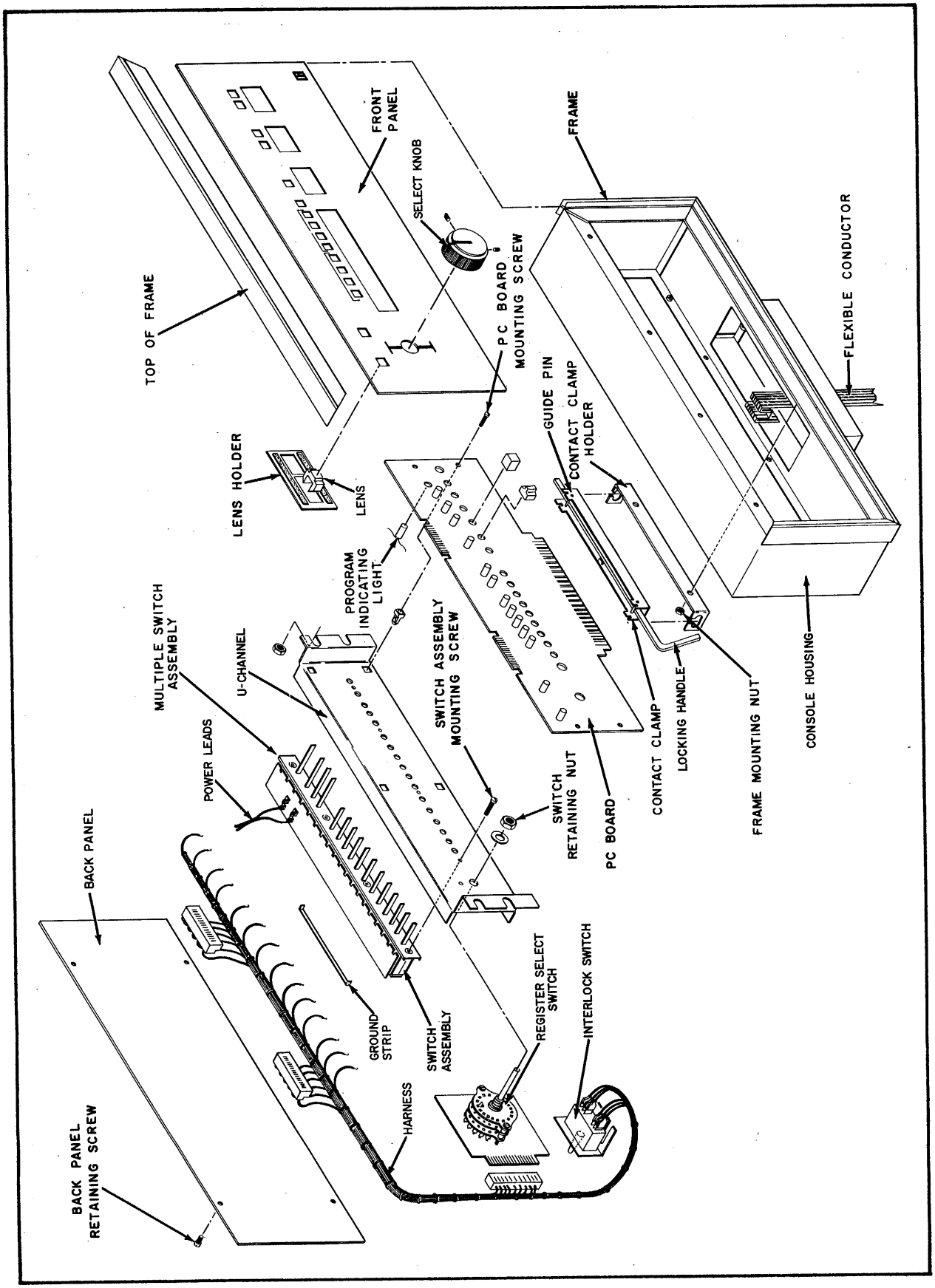


Figure 5.4 Operator Console.

through and a cutout in the console housing, as well as a slot in the tie plate, provide a passageway for the flexible conductors to the main chassis.

5.2.1 REPLACEMENT - INDICATING LIGHTS

1. Turn power OFF and remove the plug of the power line cord from the wall outlet. Remove the back panel retaining screws and remove the panel.

2. Loosen the two set screws in the SELECT knob and remove the knob. Remove the four U-channel mounting nuts from inside the console. Push the locking handle of the contact clamp holder upward to remove the printed circuit board from the flexible conductor clamp. Pull the U-channel out of the console.

3. Pull all switch knobs off their switch actuating shafts by gripping each knob with a pair of pliers. Remove the five board mounting screws and, if necessary, the connectors from the top of the board. Pull the board forward so that it clears the shaft of the REGISTER SELECT switch. Unsolder the leads of the defective indicating light and remove the light by pushing it out of its hole. Scrape away traces of cement from inside the mounting hole.

4. Insert a new light and adjust it so that it projects the same distance as other lights, then cement it in place. Solder its leads to the points from which the two previous light leads were removed.

5. Replace console parts by reversing the sequence of disassembly.

5.2.2 REPLACEMENT - MULTIPLE SWITCH ASSEMBLY

1. Perform steps 1 through 3 outlined in paragraph 5.2.1 except that indicating light leads are not to be unsoldered. Instead, unsolder the two line cord leads from the outside switch terminals.

2. First mark and then unsolder harness leads from switch terminals. Remove the three switch assembly mounting screws. Remove the switch assembly and install a replacement. Fasten it and resolder harness leads to corresponding switch terminals. Replace the circuit board.

3. Replace console parts by reversing the sequence of disassembly.

5.2.3 REPLACEMENT - REGISTER SELECT SWITCH

1. Perform steps 1 through 3 outlined in paragraph 5.2.1 except that indicating light leads are not to be unsoldered.

2. Remove the edge-tab connector from the board on the switch. Loosen and remove the switch retaining nut. Pull the switch out from the rear of the channel.

3. Install a new switch and position it so that its guide pin fits into the locating hole in the U-channel. Tighten the retaining nut. Replace the connector and all parts of the console by reversing the sequence of disassembly. Replace the line cord plug in the wall receptacle and check operation of the processor and its associated equipment.

5.3 DRUM ASSEMBLY

The drum and its drive motor are supported by the drum mount shown in figure 5.5. The drum is a sealed assembly that cannot be adjusted or repaired. The motor is designed for single phase, capacitor-start, a.c. operation, with thermal overload protection. The motor or its starting capacitors may be replaced, if necessary.

The drum mount sits on four shock and vibration isolators that are fastened to the base. Mounting screws pass through clearance holes in the base to tighten mount and isolators. Cutouts in the base and its two vertical side tabs allow heads of mounting bolts to pass through during installation on the main chassis of the processor; see paragraph 5.1. The bottom of the base is protected by an insulating plate that is held in place by the bent-down tabs on the base.

A damping plate connects the tops of drum and motor housings to reduce total vibration of both units during operation. Printed circuit board H is mounted to this damping plate with four rubber standoffs to reduce vibration transmission to the board. The circuit board and plate must be removed if the motor is to be replaced. Drum head circuit boards I, J, K1 and K2 are mounted to the drum housing, and these boards must not be removed from the drum. The boards contain the magnetic heads and associated circuits, and they may be rewired in the field to substitute a replacement head, if necessary.

5.3.1 DRUM ASSEMBLY REMOVAL AND REPLACEMENT

1. Turn power OFF and remove the line cord plug from the wall receptacle. Remove the right and left side covers from the processor housing, see paragraph 5.1.

2. Remove connector P10 from the center support of the main chassis.

3. Loosen the four drum base retaining bolts in the front and center supports, and lift the base off the bolt heads. Remove the entire drum assembly less insulating plate through the left side of the housing. The insulating plate remains on the main chassis.

CAUTION: Make sure that the assembly rests sideways on a solid surface. Support it only on the side opposite to that of the drum head circuit boards. The assembly must NOT lie on the side on which boards mount to the drum. If the drum assembly cannot be placed as specified without disconnecting jumpers to drum head circuit boards first, complete steps #4 and #5 before step #3.

4. Mark the location and color coding of jumper wires to boards I, J, K1 and K2. Remove the jumper wires from these boards.

5. Remove board mounting screws and the rubber standoffs from board H. Move the board aside to clear the damping plate. Do NOT remove jumper wires from board H.

6. Replace the drum assembly entirely, including the base. Install its replacement and reassemble all parts by reversing the sequence of disassembly.

5.3.2 DRUM MOTOR REMOVAL AND SERVICE

The drum motor is permanently lubricated; therefore, it does not require periodic inspection or maintenance. The motor is protected against overheating by a thermal overload relay which automatically disconnects windings from the power line if the temperature within the motor housing rises above maximum permissible limits. The relay cuts the motor back in after the temperature drops sufficiently to permit safe operation.

Observe the following steps for motor replacement:

1. Turn power OFF. Remove the power line plug from the wall receptacle.

2. Remove the drum assembly from the main chassis as outlined in steps #2 and #3 of paragraph 5.3.1. Remove the board mounting screws and the rubber standoffs from board H. Do NOT remove jumpers from this board. If the board cannot be moved sideways to clear the damping plate without removing jumpers from any of the other drum head circuit boards, mark the position and color coding of jumpers on these boards and remove them.

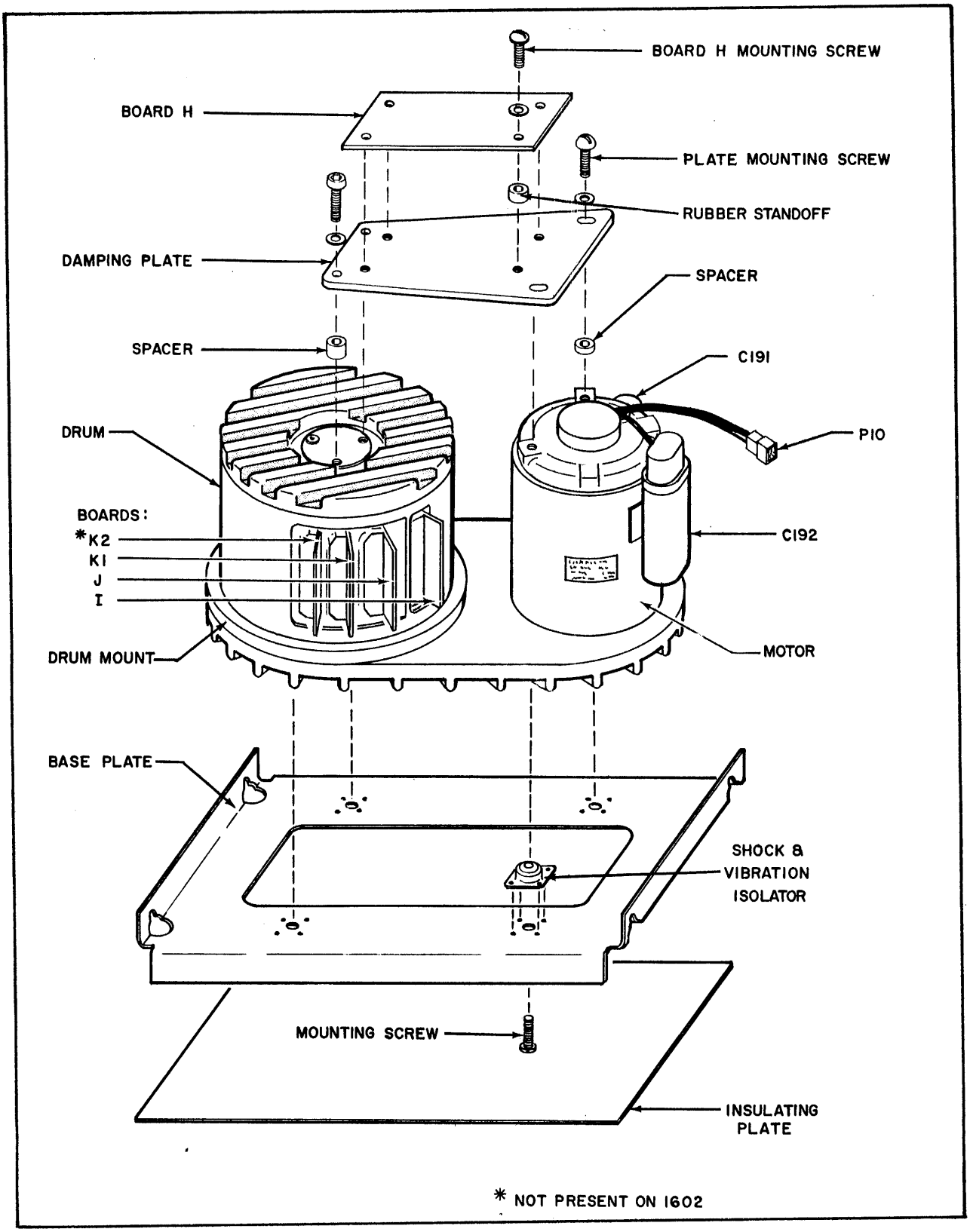


Figure 5.5 Drum Assembly.

3. Remove the damping plate by removing the four mounting screws. Note the thickness of spacers between plate and motor, and plate and drum. Spacer thickness differs, but must be correct at installation of the new motor.

4. Loosen the four motor mounting screws from the underside of the drum mount. These screws are socket head cap screws, and two can be reached only by inserting the socket wrench between belt and pulley. To make removal easier, the rim of the pulley is notched at opposite ends, and notches should be aligned with screw heads before removal.

5. Slide the motor toward the drum and remove the belt. Loosen the set screw in the motor pulley hub and remove the pulley. Then remove the mounting screws and the motor from the drum mount. Install the replacement motor.

6. Loosely fasten the motor mounting screws. Place the pulley on the motor shaft and tighten the set screw loosely against the flat of the shaft. Then adjust the belt as outlined in paragraph 5.3.3. Fully tighten the motor mounting screws and reassemble the remaining components by reversing the sequence of disassembly. Turn power ON and check drum operation.

Proceed as follows to replace starting capacitors C191 or C192:

1. Turn power OFF. Remove the power line plug from the wall receptacle.

2. Pry off the cap from the top of the defective capacitor. Unsolder the black lead from one, and the blue and white leads from the other capacitor terminal. Remove the mounting screw for C192, or push C191 out of its clamp.

3. Install a replacement capacitor and tighten its mounting screw or clamp.

4. Solder the black lead to one terminal, and the blue and white leads to the other. Replace the cap to protect the leads and terminals. Put the processor back into operation.

5.3.3 PULLEY ALIGNMENT AND BELT TENSION ADJUSTMENT

The drum assembly must be removed from the main chassis of the processor for this adjustment. It is assumed that steps #1 through #3 of paragraph 5.3.1 have been completed and that the drum assembly is lying sideways with the drum head circuit boards facing up. The two damping plate mounting screws at the motor top must have been removed. Proceed as follows:

1. If the motor was replaced so that the pulley had to be loosened, check pulley alignment. The outer faces of both pulleys must be within 0.010 inch of each other. Place a straight-edge on the face of the drum pulley and raise or lower the motor pulley until both are in line. Then tighten the set screw in the motor pulley hub on the flat of the motor shaft.

2. Check belt tension by placing a tension scale, tool kit #243-A, on one side of the belt centered between the two pulley shafts. Apply a force of 1 lb. at the point of scale contact. Belt deflection should not exceed 3/8 inch maximum. Slide the motor away from or toward the drum to obtain a belt tension within the specified range. Then tighten the four motor mounting screws. See Figure 5.6.

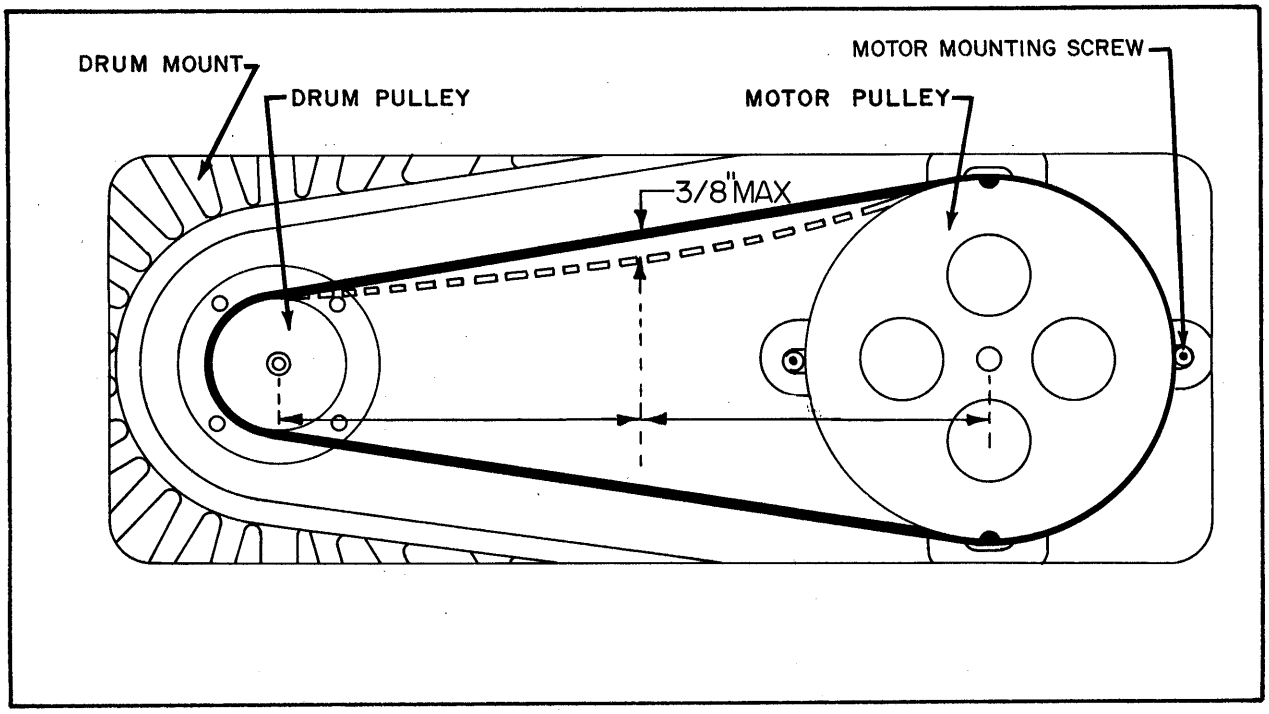


Figure 5.6 Belt Tension Adjustment.

NOTE: If the motor pulley should require replacement, both motor and drum pulleys must be replaced as a matched set.

3. Reassemble all drum components by reversing the sequence of disassembly.

5.4 FLEXIBLE CONDUCTORS AND LOCK

The power supply and all printed circuit boards interconnect with flat, flexible, transparent Polyimide tapes with embedded copper leads. The tapes are pre-cut and pre-shaped to produce desired conductor configurations of specific lengths. Connecting leads between any two points, therefore, can only be replaced by substituting an entire conductor of proper length and shape.

Table 5.1 lists conductor sources and destinations. The letter P in the Cable Position column identifies power-carrying conductors. Figure 5.7 shows how conductors are clamped against printed circuit boards to provide good electrical contact. A portion of the U-shaped frame for the larger boards is shown in the right-hand view, while the bottom channel, shown in both views, is typical of the locking arrangement for all boards.

Conductors are assembled into the spring steel clamp of the lower frame. They are then cemented in place on the outside. Replacement of a conductor, therefore, requires that hold-down strips of double-faced adhesive tape be replaced at the same time.

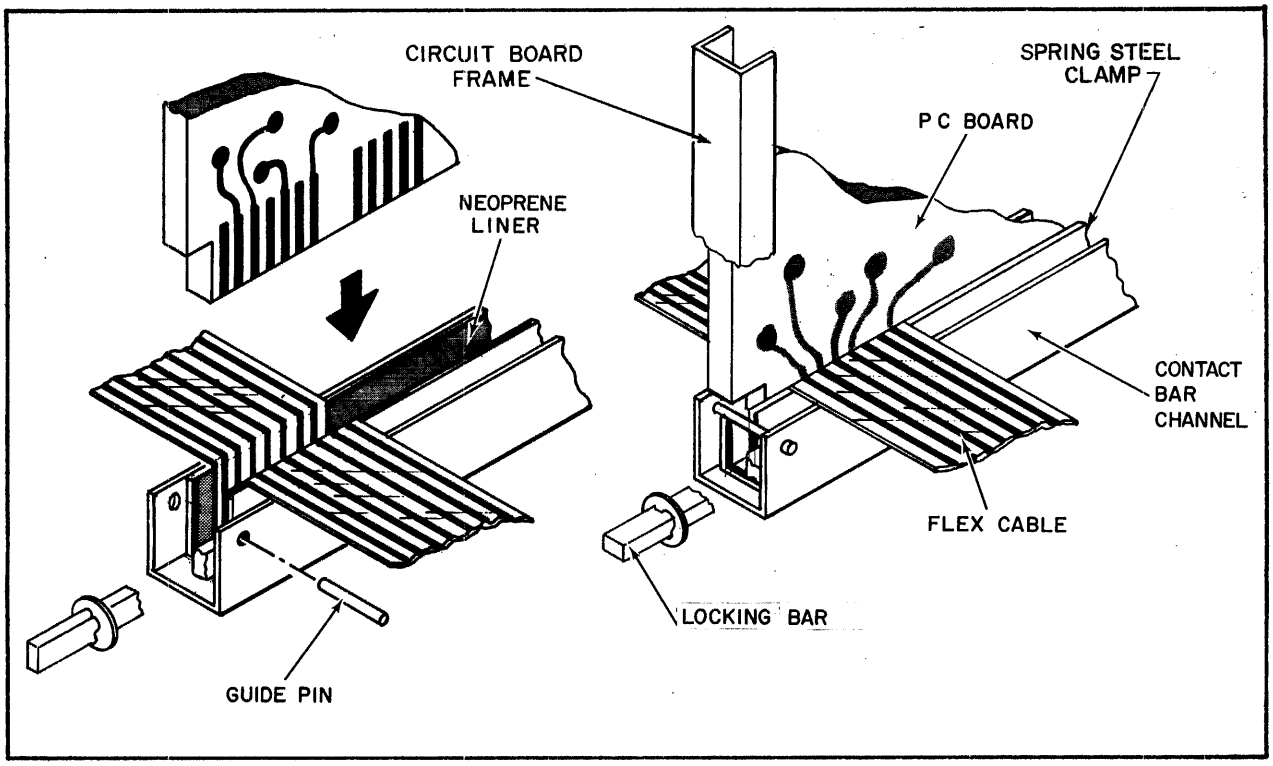
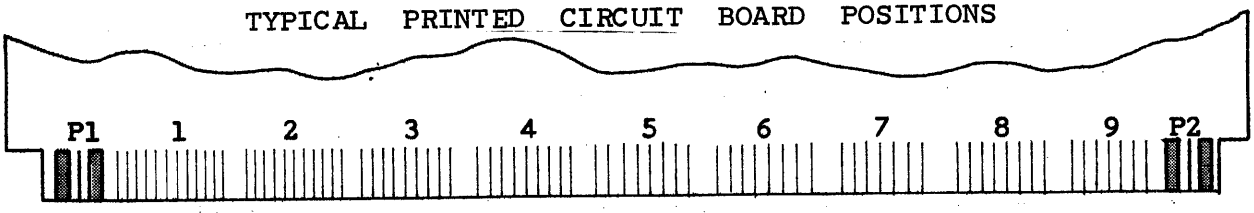


Figure 5.7 Flexible Conductor Lock.

TYPICAL PRINTED CIRCUIT BOARD POSITIONS



SOURCE		INTERMEDIATE BOARDS						DESTINATION	
BOARD	POS.	BOARD	POS.	BOARD	POS.	BOARD	POS.	BOARD	POS.
A	P1	B	P1	E	P1	C	P1	D	P1
	P2	E	7	-	-	-	-	D	P2
	1	B	1	-	-	-	-	G	2
	2	-	-	-	-	-	-	F	3
	3	-	-	-	-	-	-	F	1
	4	B	4	C	4	-	-	D	4
	5	B	5	C	5	-	-	D	5
	6	B	6	C	6	-	-	D	6
	7	B	7	C	7	-	-	D	7
	8	B	8	C	8	-	-	D	8
	9	B	9	C	9	-	-	D	9
B	2	C	2	-	-	-	-	D	2
	3	C	3	-	-	-	-	D	3
C	1	-	-	-	-	-	-	G	4
	2	B	P2	-	-	-	-	E	8
D	1	-	-	-	-	-	-	G	1
E	2	-	-	-	-	-	-	G	P2

Table 5.1: Flexible Conductor List.

Steel spring clamps are notched at the ends to fit between and under guide pins. This prevents side movement of boards, and it also prevents clamps from being lifted out of frame bottoms when a board is pulled upward.

A Neoprene liner within the clamp prevents slippage of the conductors, and it also makes for better contacts by increasing the gripping action of the clamp when locked. Guide pins at bottom frame ends help to locate circuit boards during insertion, so that contacts on the boards line up with the correct leads in appropriate conductors. Contact areas on the conductors are cleared of all insulating material in the region where contact is to be made at board surfaces.

The ends of locking bars fit into holes in the main chassis supports, where each end is secured with a snap-on clip. Boards can be released by removing the right and/or left side cover from the processor housing. A locking bar is turned approximately 90 degrees to release the board. The board can then be pulled upward and out along slides placed in the sides of the frame. The ends of locking bars act as pivots to allow boards to be swung away from the main chassis after release of the two latching tubes at the top of each board. Board G in the operator console differs only in that the channel is fastened to the console, thereby not being free to pivot about its locking bar.

5.5 PRINTED CIRCUIT BOARDS AND DRUM HEAD CIRCUITS

5.5.1 PRINTED CIRCUIT BOARDS

The main chassis of the processor supports the four large printed circuit boards shown folded down in figure 5.8. Boards are labeled: A, B, C and D, with the A board mounted closest to the outside of the housing. The boards are inserted in frames, shown in figure 5.1, to pivot about the ends of their locking bars. To fasten boards in an upright position, the two latching tubes at the top of each board are pushed outward into holes located in the front and center supports.

The frame of the F board is supported in similar manner by a bracket on the fan mounting plate which is spotwelded to the center support. The frame pivots in the same way as the larger boards except that its pivot bar is on the right side, therefore, the board swings outward in a counterclockwise direction when it is unlatched. It latches on the left with a bracket mounted below the board to the center support.

The E board is fastened securely to the left side of the main chassis enclosure that houses the power supply. The board is the conversion point between flexible conductors, described in paragraph 5.4, and the normal cable wiring originating at the power supply.

The G board contains indicating lights and other circuit components for display and program select or operating functions. The board is mounted firmly to the U-channel in the operator console as shown in figure 5.4.

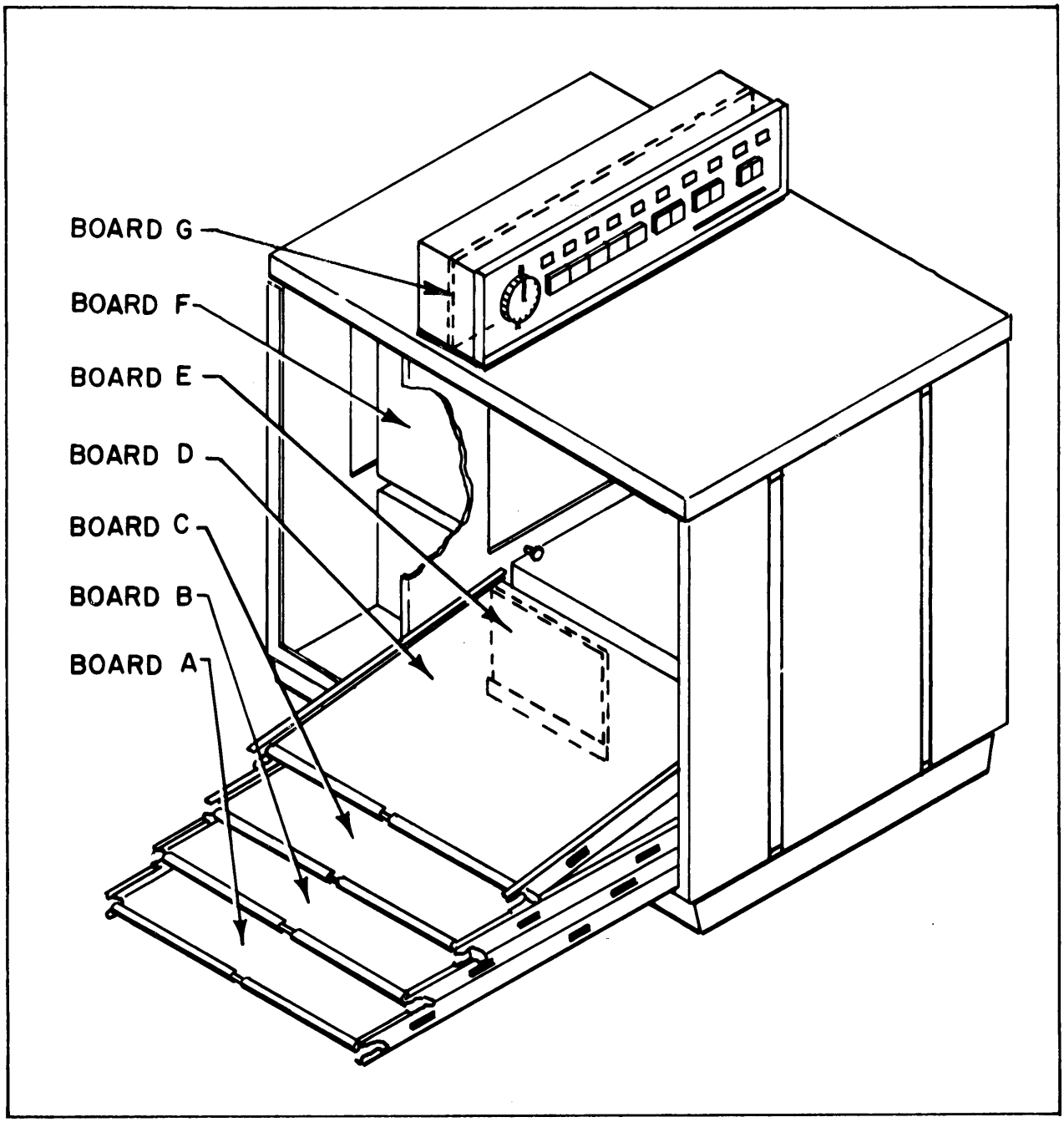


Figure 5.8 Printed Circuit Board Location.

The A and D boards are marked with grid lines to form 64 rectangles on the A board and 72 rectangles on the D board for easier component location. Parts mounted to these boards, therefore, carry board and grid location to their designations, prefixes such as 1A1..., 2D9..., 8A8.... All other boards are not gridded, and part designations are either marked on the board, or parts are identified by reference to marked components, pin numbers, etc.

5.5.2 DRUM HEAD CIRCUIT BOARDS

Four printed circuit boards are mounted to one side of the drum on the Model 1601 processor, whereas only three boards are mounted to the drum of the Model 1602. All boards carry magnetic head assemblies for record and/or playback of drum track information. Circuits associated with each head are contained on the same board as the head.

Boards are labeled I, J, K1 and K2. The latter board is left out on Model 1602. Boards are shown assembled to the drum in figure 5.5, with individual boards and their applicable circuit configuration shown in figures 5.9 through 5.11. Boards are mounted and adjusted for correct tracking at the factory. At no time should the serviceman attempt to remove or loosen a head circuit board. If a board requires replacement, the entire drum assembly must be turned in for replacement. Spare heads are provided on each board and are used as replacements of defective heads as outlined in paragraph 5.5.2.1. When all the spare heads on a particular board are used, the entire drum assembly must be replaced.

Board I holds one active head (the head in use is termed "active") each for BI and S record, and for Z2 and Z3 playback. It also holds an equivalent number of spares. Heads are inserted in the board in such a manner that they protrude slightly beyond the board mounting surface. Three leads connect each head with its circuit components as shown in figure 5.9. The heavier lead connects to the center tap of the head, while the two thinner leads connect to opposite outer leads. Outer leads of different heads do not necessarily correspond; therefore, jumper wires to the board are arranged to phase each head correctly. Gray shaded lines and blank broken lines on the schematic depict printed circuit interconnections on both sides of the board. Magnetic heads are checked out at the factory, and it is possible that, in some cases, boards are released with active and spare heads interchanged.

The J board is arranged similarly, containing the BI, S, and Z1 playback heads. K board layout is also similar to that described previously, except that each board carries 18 dual-function record/playback heads. Two of these heads are spares, the other 16 are active. The spare heads are located at the top and bottom of the assembly. The K1 and K2 boards are identical in component arrangement, with the label for general storage tracks and diodes listed in Table 5.2.

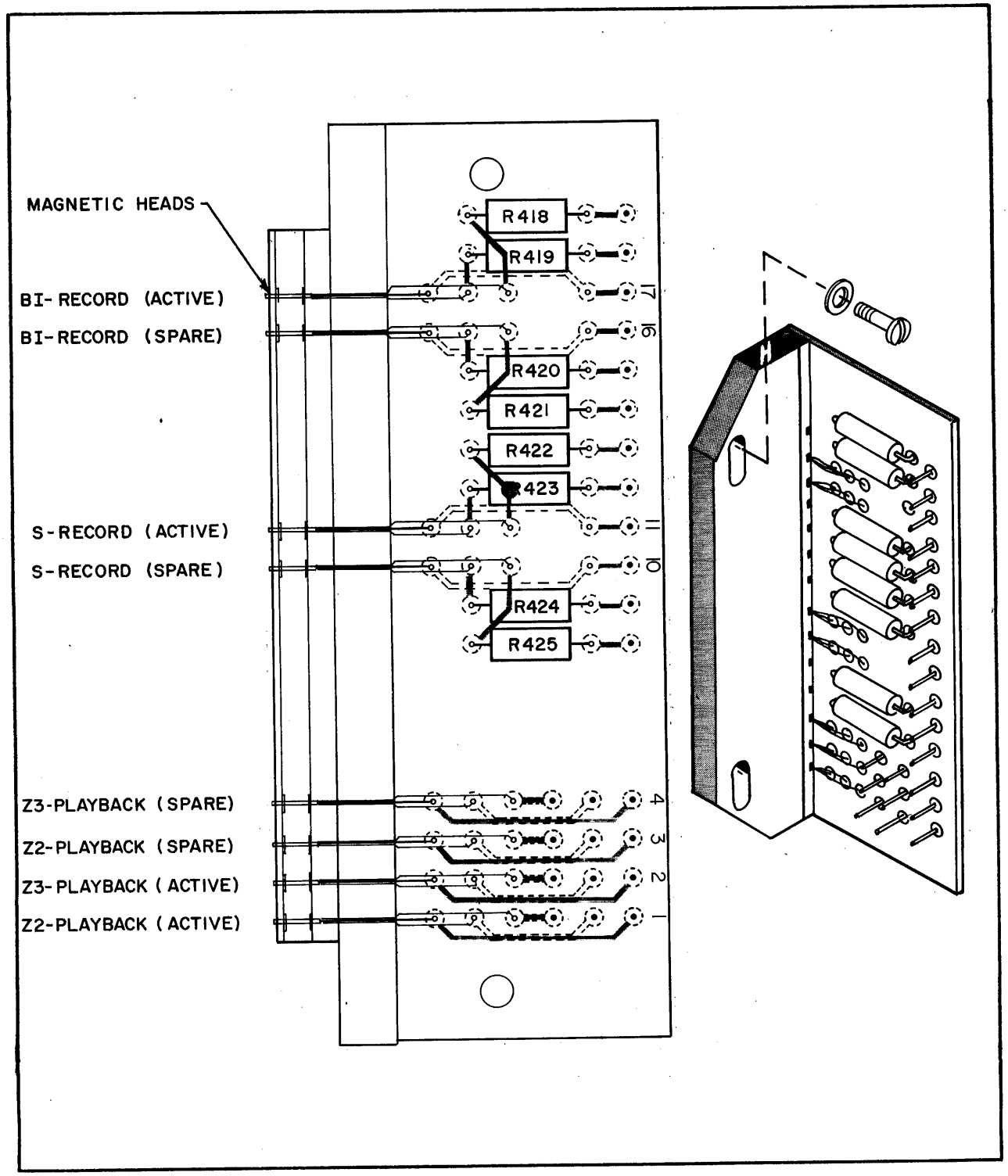


Figure 5.9 Head Circuit Board I.

HEAD NO.	BOARD K1		BOARD K2	
	TRACK	DIODES NO.	TRACK	DIODES NO.
18	Spare	CR101 & CR102	Spare	CR137 & CR138
17	15	CR103 & CR104	31	CR139 & CR140
16	14	CR105 & CR106	30	CR141 & CR142
15	13	CR107 & CR108	29	CR143 & CR144
14	12	CR109 & CR110	28	CR145 & CR146
13	11	CR111 & CR112	27	CR147 & CR148
12	10	CR113 & CR114	26	CR149 & CR150
11	9	CR115 & CR116	25	CR151 & CR152
10	8	CR117 & CR118	24	CR153 & CR154
9	7	CR119 & CR120	23	CR155 & CR156
8	6	CR121 & CR122	22	CR157 & CR158
7	5	CR123 & CR124	21	CR159 & CR160
6	4	CR125 & CR126	20	CR161 & CR162
5	3	CR127 & CR128	19	CR163 & CR164
4	2	CR129 & CR130	18	CR165 & CR166
3	1	CR131 & CR132	17	CR167 & CR168
2	0	CR133 & CR134	16	CR169 & CR170
1	Spare	CR135 & CR136	Spare	CR171 & CR172

Table 5.2: K Board Track & Diode Identification.

5.5.2.1 Spare Head Replacement

If a spare head on either boards I or J has to be substituted for a defective one, the 3 jumper wires connected to the 3 pins associated with the defective head must be removed and connected to the corresponding pins of the spare head. (Note that the numbered pin identifies the center tap of each head.)

For instance, to interchange BI record heads on board I, remove the jumper from pin #17 and connect it to pin #16. Remove the jumper to the pin closest to R419 and connect it to the pin closest to R420. Likewise, remove the jumper from the R418 pin and connect it to the R421 pin. This substitutes the spare head for the presently active head. Consequently, R418 and R419 will be replaced by R421 and R420, respectively.

When a BI or S record head is replaced on board I, the corresponding playback head on board J must also be interchanged. In other words, if the upper magnetic head on board I is used for BI record, the upper head

on board J must then be used for BI playback. Z1, Z2 and Z3 tracks are playback-only tracks. Therefore, they have no record heads, but they do have spare playback heads. Jumper wires for these tracks are moved up or down as a group; i.e., to interchange the Z3 heads, remove the jumpers from the row of three pins marked #2 and move them, without mixing them up, to the three pins marked #4.

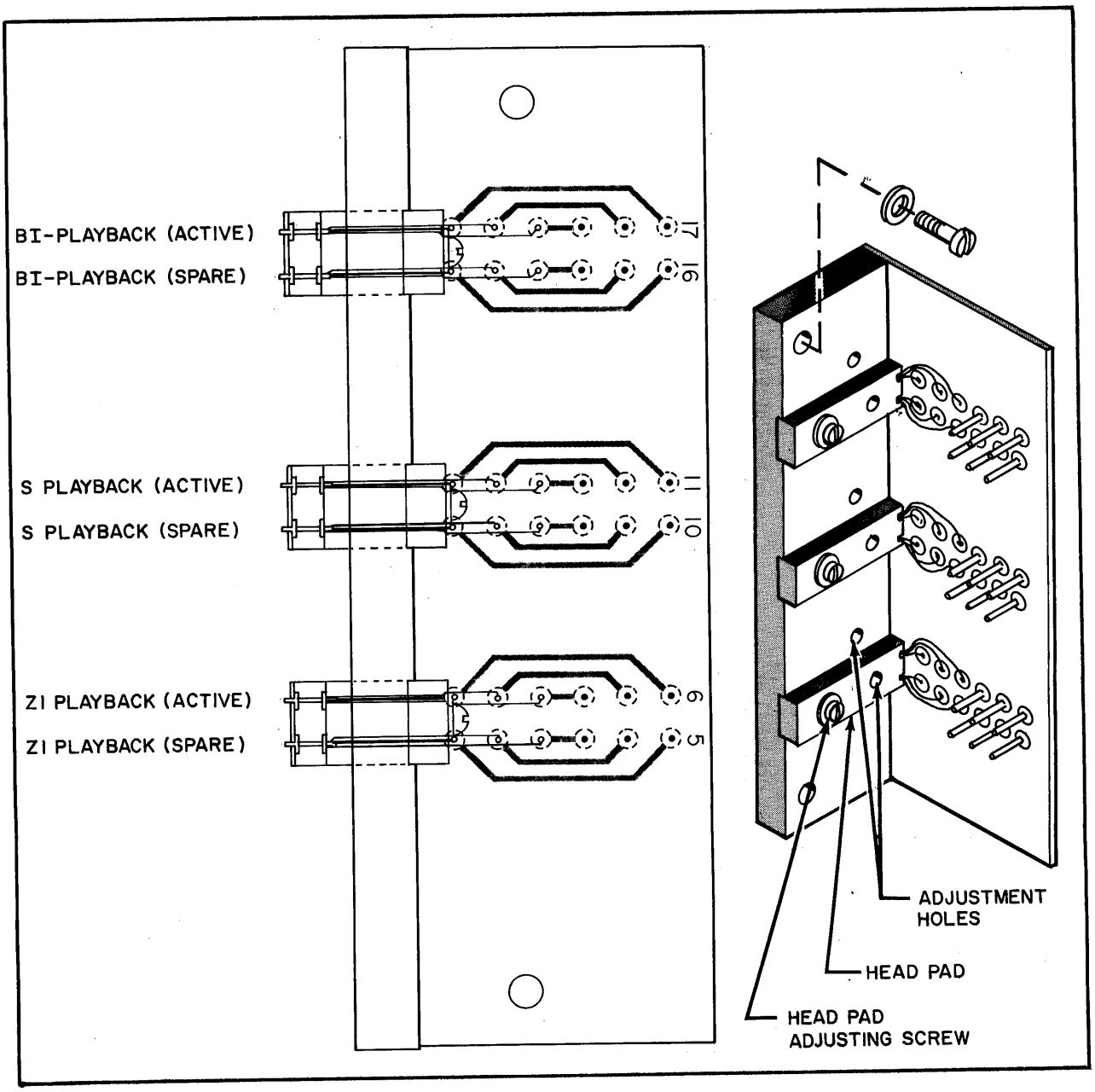


Figure 5.10 Head Circuit Board J.

An operational check to determine correct phasing of the heads must be performed after each head interchange.

1. Generate a test pulse and store it on the track affected by the head interchange.

2. Play back this test pulse through the correct playback head.

3. A HIGH or LOW recorded previously must be reproduced as such; if it is not, interchange the two jumpers to the unnumbered pins.

4. With the phasing correct, it is then necessary to check the playback sensing, as outlined in paragraph 5.5.2.2.

If a spare head on the K1 or K2 board has to be substituted for a defective one, proceed as follows:

1. Select the spare closest to the head to be replaced.

2. Cut out the two diodes from the outer leads of the defective head. Then trace circuit connections from the defective head with the schematic of figure 5.11 to the numbered or labeled jumper wire pins. Do NOT remove the jumpers.

3. Instead, solder a wire to each diode connection for the spare head, and a third to the common center connection.

4. Solder the other ends of these leads to the numbered or labeled jumper pin connections to which wires of the defective heads have been traced.

5. Record a test pulse and then play it back to make sure that head phasing is correct. If a HIGH is recorded, but a LOW is played back, reverse the wires going to the solder joints with leads from the outside connections of the spare head.

5.5.2.2 Playback Sensing

Whenever a spare Z1, Z2, Z3, BI, or S head is used to replace a defective active head, playback sensing must be checked for that track only. The procedures are outlined for each individual track.

Z1 Track

1. At pin Z1, located within 2D6, check polarity of Z1. If the polarity is not as shown in view 1 of figure 5.12, interchange the jumper wires connected to the two unnumbered pins of the Z1 head in use on board I.

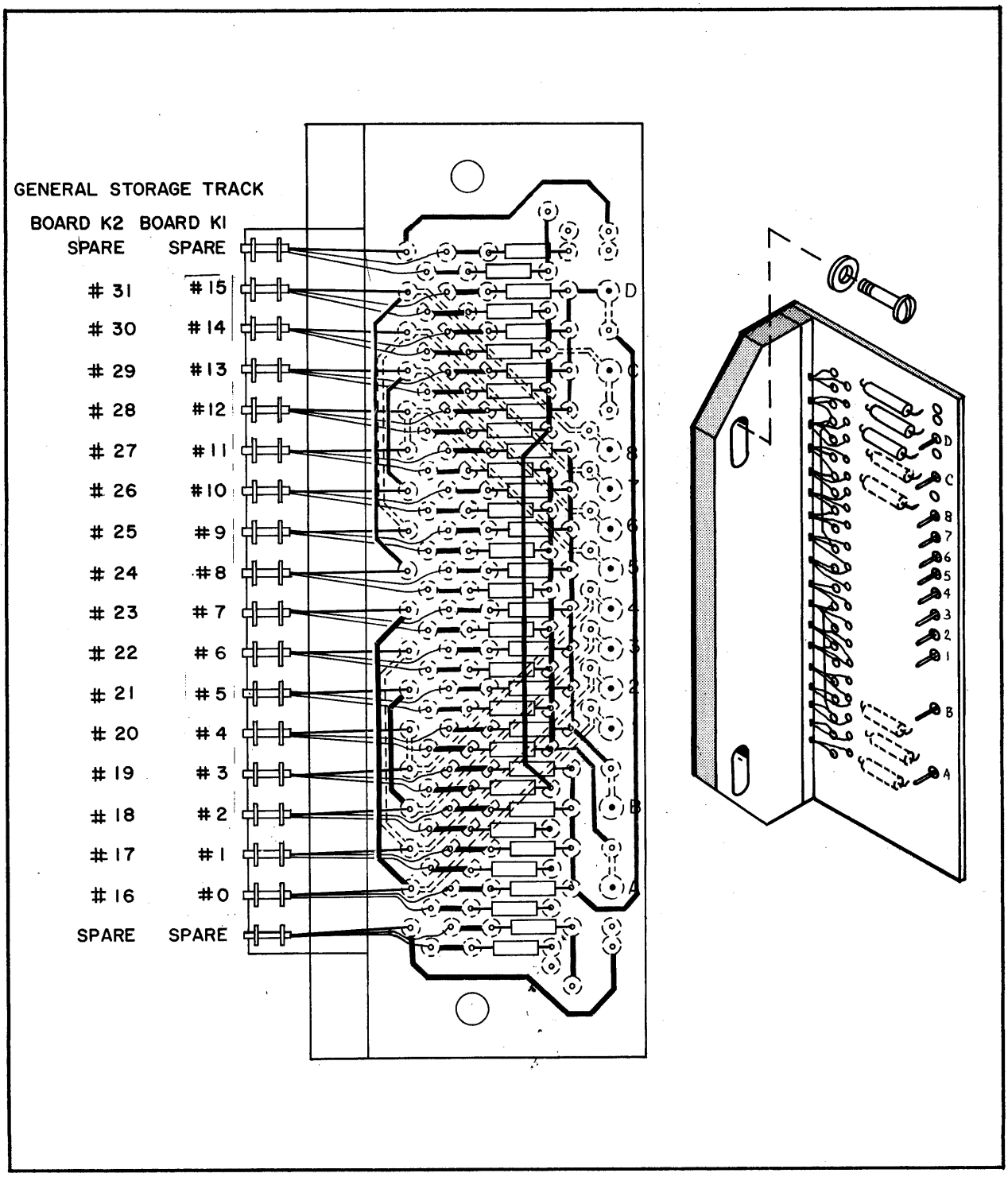


Figure 5.11 Head Circuit Boards K1 and K2.

2. The Z1 pulse width, at the Z1 pin, should be 200 ± 20-0 nanoseconds. If the width is not as noted, adjust R379, located within 3D6, for the correct width.

   NOTE: If R379 requires adjustment, storage must be erased as outlined in the storage erase procedure.

3. With a dual-trace scope, check that the trailing edges of the $\overline{Z1}$ pulse, at pin $\overline{Z1}$ within 2D5, occur about midway between consecutive output pulses of the Z2 comparator, at pin Z2 within 1D4, as shown in view 2 of figure 5.12. If they do, Z1 playback sensing is correct. If they do not, proceed with the following steps.

4. Slightly loosen the head pad adjusting screw for the Z1 heads, see figure 5.10. Insert the two prongs of kit tool #..... into the head pad adjusting holes and very slowly pivot the head pad to bring the trailing edges of $\overline{Z1}$ midway between consecutive Z2 comparator output pulses. Keep the head pad in this position and tighten the adjusting screw to secure the pad. Check that tightening of the screw does not upset the adjustment.

5. Check processor operation by placing it into the idle mode and check for the presence of timing signals at the following location:

   T4 at pin M10-8, within 1B
   T7 at pin M9-8, within 1B
   T39 at pin M43-11, within 4B

Storage Erase Procedure

All of the processor's storage EXCEPT master timing tracks Z1, Z2, and Z3 must be erased whenever R379 (Z1 pulse width) is adjusted. Use the Erase Box, kit tool #393, and perform the following steps:

1. Turn the processor OFF and remove power supply fuse F6, (see paragraph 5.6), and also remove harness from headboard. Turn the processor ON. Because the fuse has been removed, only AC power is present in the processor and all DC is disabled. The drum can now be erased without danger of DC shorting.

2. Turn the erase box OFF by rotating its control knob fully counterclockwise. Then plug the power cord of the box into

a wall outlet. Connect the black and white leads of the erase box to the two unnumbered pins of the active B1 playback head on board I. Turn the erase box control slowly to its maximum clockwise position and then slowly back to its OFF position. Remove the two leads and repeat this operation for the active S playback.

3. Turn the erase box OFF. Connect its black and white leads to pins A and B on board K1. Connect its red lead to pin 1. Turn the control slowly from the OFF position to the maximum clockwise position and then back to its OFF position. Remove the red lead, connect it to pin 2, and repeat the procedure.

4. Repeat the operation of step 3 for pins 3 through 8, then remove the black and white leads from pins A and B and connect them to pins C and D. Connect the red lead as outlined previously and repeat step #3.

5. Repeat steps 3 and 4 for board K2.

6. Turn the processor OFF and replace the power supply fuse and harnesses removed in step 1.

7. Turn the processor ON and check for normal operation.

Z2 Track

1. Perform the check specified in step 3 of the playback sensing procedure for track Z1. If the trailing edges of $\overline{Z1}$ occur about midway between consecutive output pulses of the Z2 comparator, playback sensing for the Z2 track is correct and no further adjustment is required. If they do not, note the amount of displacement and proceed with the following steps.

2. Measure the amount of displacement between the trailing edges of $\overline{Z1}$, as measured with a dual-trace scope at pin $\overline{Z1}$ within 2D5, and the midpoint of consecutive Z3 comparator output pulses at pin Z3 within 1D3. If the trailing edge displacement equals - both in magnitude and direction - the Z2 replacement of $\overline{Z1}$ to Z2, proceed with step 3. If the displacements are not equal, replace the active Z3 head with its spare. The head replacement should cause the $\overline{Z1}$ to Z3 displacement to equal the $\overline{Z1}$ to Z2 displacement. If it does not, or if a spare Z3 head is not available for replacement purposes, then the entire drum assembly has to be returned for replacement.

3. Perform steps 4 and 5 of the playback sensing procedure for track Z1.

NOTE: If timing signals T4, T7, and T39 are not present or correct, interchange the jumper wires connected to the two unnumbered pins of the Z2 head in use on board I.

Z3 Track

1. Check whether the trailing edges of the $\overline{Z1}$ pulse, as measured with a dual-trace scope at pin $\overline{Z1}$ within 2D5, fall about midway between consecutive Z3 comparator output pulses, measured at pin Z3 within 1D3. If they do, playback sensing for the Z3 track is correct and no further adjustment is required. If they do not, note the amount of displacement and proceed with the following steps.

2. Measure the amount of displacement between the trailing edges of $\overline{Z1}$, as measured with a dual-trace scope at pin $\overline{Z1}$ within 2D5, and the midpoint of consecutive Z2 comparator output pulses at pin Z2 within 1D4. If the trailing edge displacement equals - both in magnitude and direction - the $\overline{Z1}$ to Z3. pulse displacement, proceed with step 3. If the displacements are not equal, replace the active Z2 head with its spare. The head replacement should cause the $\overline{Z1}$ to Z2 displacement to equal the $\overline{Z1}$ to Z3 displacement. If it does not, or if a spare Z2 head is not available for replacement purposes, then the entire drum assembly has to be returned for replacement.

3. Perform steps 4 and 5 of the playback sensing procedure for track Z1.

NOTE: If timing signals T4, T7, and T39 are not present or correct, interchange the jumper wires connected to the two unnumbered pins of the Z3 head in use on board I.

BI Track

1. Turn the processor OFF. Unsolder the end closest to the top of the board of jumper L90, located within 7D3. Connect a wire from this end of the jumper (input to BI record circuit) to the T39 signal at pin M43-11, located within 4B. Also connect one lead of a dual-trace scope to this point. Connect the other scope lead to M146-8.

2. Turn the processor ON. After it warms-up, view the two scope traces. If the T39 BI playback is inverted, with respect to

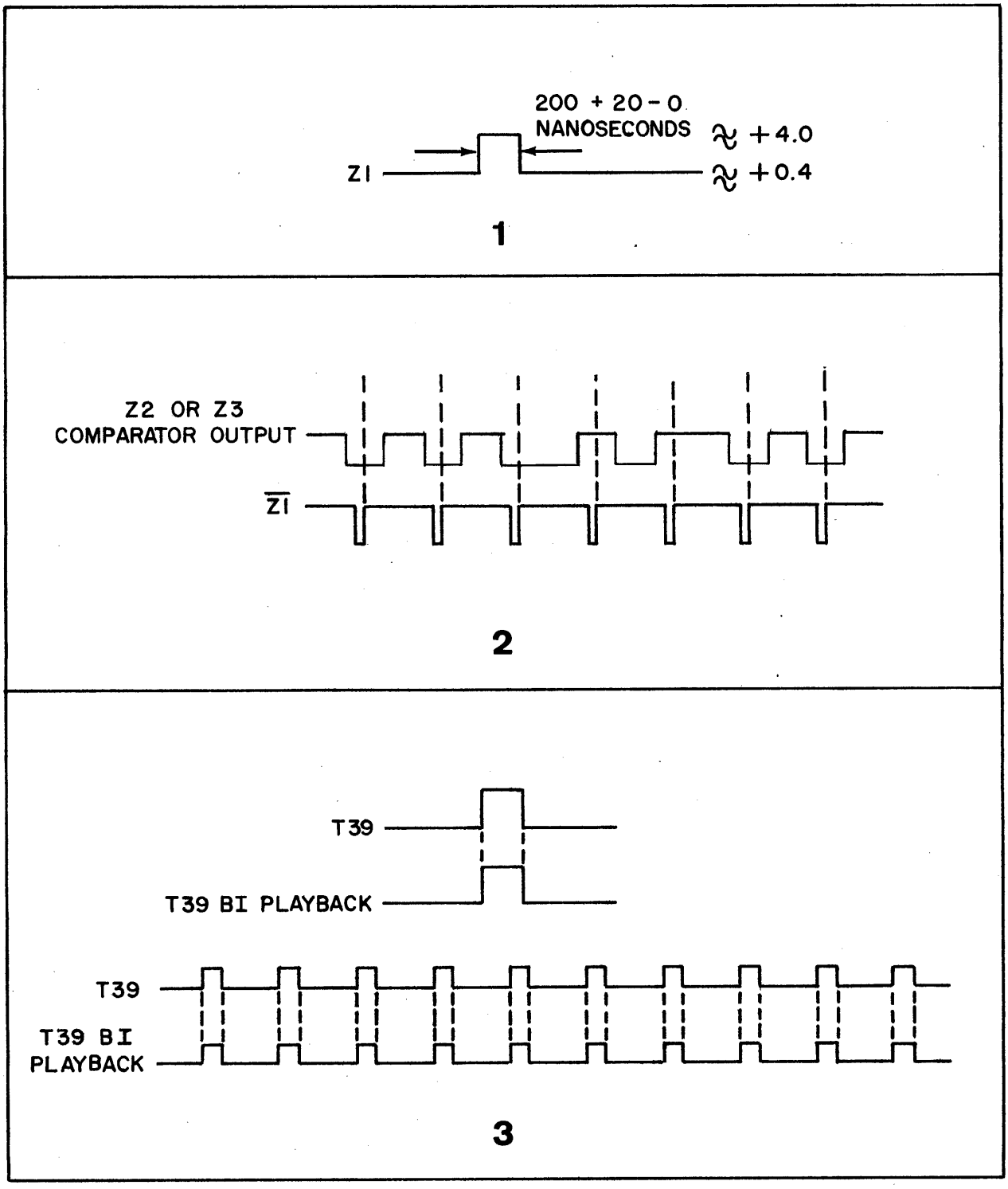


Figure 5.12 Playback Sensing.

Rev. 1MAY69

the T39 BI input, interchange the jumper wires connected to the two unnumbered pins of the BI playback head in use on board J.

3. Observe one T39 pulse, see view 3 of figure 5.12. If the T39 BI playback pulse does not line up horizontally with the T39 pulse, slightly loosen the BI head pad adjusting screw, see figure 5.10. Insert the two prongs of kit tool #..... into the head pad adjusting holes and very slowly pivot the head pad until the two scope traces line up horizontally.

4. Observe at least eight T39 pulses. If all the T39 BI playback pulses do not line up horizontally with the T39 pulses, pivot the BI head pad until they do, and also check step 3 again.

5. Secure the head pad by tightening its adjusting screw. Check that in tightening the screw, the adjustments of steps 3 and 4 are not disturbed.

6. Turn the processor OFF. Remove the scope leads, disconnect the wire from T39 to the jumper, and solder the L90 jumper back to the printed circuit board.

7. Turn the processor ON and check for normal operation.

S Track

Perform the playback sensing procedure for track BI, but substitute jumper L30, located within 7D3, for jumper L90. In addition, make adjustments and references to the S head instead of the BI head and other scope lead to M149-9.

5.6 POWER SUPPLY

Power supply components are contained in a drawer-like chassis that is inserted into the main chassis from the rear of the processor housing. The power supply is fastened to the main chassis with two captive screws.

The line voltage transformer, filter capacitors, rectifiers and components of voltage and current regulating circuits are fastened to various internal surfaces of the power supply chassis. Circuit connections are made as shown on the schematics of figures 4.44 through 4.46. Fuse holders for Buss-type fuses, F1 through F4, are mounted to the upper section of the supply, therefore they are accessible for replacement from the top. Three additional fuse holders for F5 through F7 are mounted to the right side of the supply. These fuses can be replaced

only with correct current values, and replacement of a defective fuse requires changing both the fuse and its integral cap.

Circuit boards L, M and N are mounted to brackets fastened to the transformer. Interconnections to external circuit sections are made by way of connectors P2 through P5 at the top of the supply, and with connector PM6 on the lefthand side. All connectors differ in size and pin arrangements so that accidental interchange is impossible.

Test jacks at the rear of the supply permit margin testing of different circuit parameters. These jacks are accessible by removal of the front cover of the processor housing, as outlined in paragraph 5.1. Their identification is shown in figure 5.13. The power supply chassis has two side cutouts, one at the top and one at the bottom, so that cooling air drawn in by the fan through the filter in the front cover can be spilled from the bottom of the processor.

The power supply can be wired for operation from 115 or 230 vac lines with frequencies of 50 or 60 Hz. The line voltage transformer is of the constant-current type, thereby maintaining regulated output voltages of 5, 18, 35 and -24 volts. A differentiating amplifier is used in the supply to hold the 5 volt output voltage within specified limits under varying load conditions.

Test jacks J1 through J3 at the rear of the supply permit margin testing of different circuit parameters. Jacks are accessible when the front cover of the processor housing is removed as outlined in paragraph 5.1. They are identified in figure 5.14. Other jacks, labeled J4 through J8, are voltage test points for performance checkout of power supply operation.

The power supply can be removed from the main chassis as noted in paragraph 5.1. The power supply chassis has two side cutouts, one additional cutout at the top and one at the bottom, so that cooling air drawn in by the fan through the filter in the front cover can be expelled from the bottom of the processor housing after it passes over the various components of the power supply.

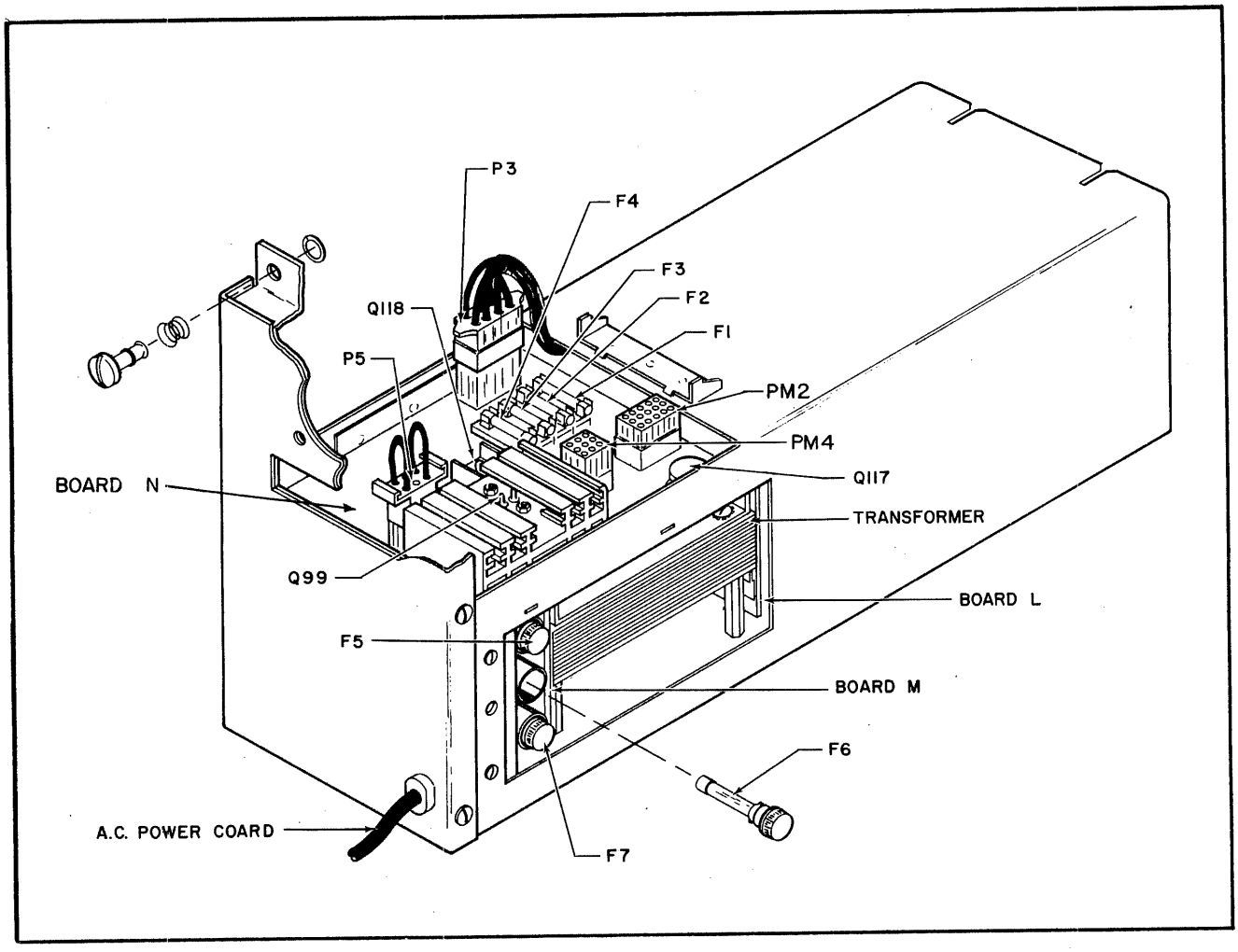


Figure 5.13 Power Supply, Top and Right Side View.

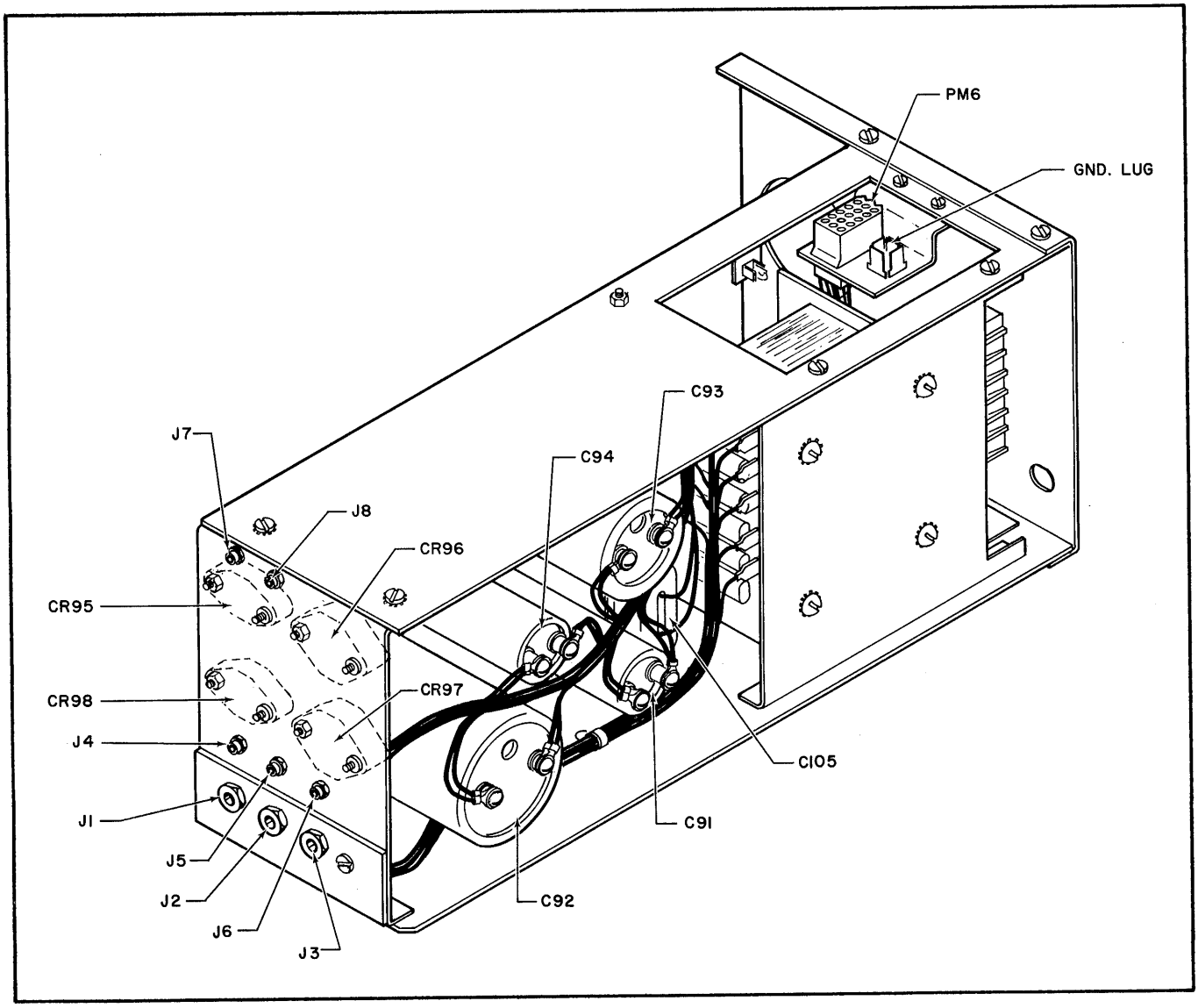


Figure 5.14 Power Supply, Bottom View.

CHAPTER 6

RUNNING SHEETS

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
A1	C5-1	8	M98	$\overline{F1}$	L11	B4-1	10
				F101	L31	B5-6	13
					EXIT	B2-8	
					EXIT	C2-8	
A2	B5-9	8	M53	L20	F8	C3-3	9
				$\overline{F101}$	$\overline{F9}$	C1-11	13
				F101 T4	F10	C2-8	13,1
				$\overline{T4}$	$\overline{F10}$	C2-7	13,1,2
				F1	A8	B5-10	5
				+VCC	F10		
				+VCC	$\overline{F10}$		
					EXIT	B2-12	
					EXIT	C2-12	
$\overline{A2}$	B5-9	11	M53	INPUT	A2	B5-9	9,10
				L10	F8	C3-3	13
				C1 F1	L11	B5-3	1
				$\overline{K2}$ $\overline{C30}$	L11	B3-3	3
				+VCC	A2		
					EXIT	B2-11	
					EXIT	C2-11	
A3	B1-8	12	M8	$\overline{C30}$	L21	B2-1	5
				C1	$\overline{A2}$	B5-9	13
A4	C3-5	11	M85	INPUT	A4	C3-5	9,10
				F3	F2	C2-4	1

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
				F3	F2	C2-4	13
				+VCC	A4		
A4	C3-5	8	M85	G	F1	C1-9	10
				K37	F1	C1-9	12
A5	B3-5	11	M31	F5 F6	K0	B2-3	2
				F5 F6 C40	K2	C1-8	9
				A38 C40	K7	B1-6	1
				F5 F6 C40	K1	B1-7	1
				C37 T4 G	K22	C1-13	13
					EXIT	B5-7	
					EXIT	C5-7	
A6	B5-9	6	M53	F6 K34	A1	C5-2	13
				K40	A15	B5-10	9
					EXIT	B9-2	
					EXIT	C9-2	
A6	B5-9	3	M53	G	L50	C2-4	4
				INPUT	A6	B5-9	5,4,3
				K42 K53	F9	C3-9	5
				L53	F9	C2-9	13
				K43 F1	L30	M141-3D	3
					EXIT	B6-14	
					EXIT	C6-14	
					EXIT	D6-14	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
A7	B6-2	6	M56	$\overline{K43}$	$\overline{L50}$	C6-6	5
				K34 $\overline{F6}$ F3	F14	C6-5	13
					EXIT	B6-4	
					EXIT	C6-4	
A8	B5-10	6	M54	A15 G	F9	C3-9	9
				G G	L21	B2-6	11
					EXIT	B9-11	
					EXIT	C9-11	
A9	B3-5	6	M31	C30 G	F10	C2-8	5
				$\overline{F6}$ $\overline{F5}$ G	L11	B4-2	13
				A38	K13	B1-5	12
				$\overline{A38}$ F7	K14	B1-6	9
				F5 F6 F7	K46	B2-7	1
				F7 C49	K87	C2-1	3
					EXIT	B2-4	
					EXIT	C2-4	
A10	B5-10	11	M54	G			
				G	L11	B3-1	1
					F12	C5-8	5
					EXIT	B9-13	
						C9-13	
A11	B4-4	6	M38	A18 F6	K5	B2-3	4
				A18 F6	K6	B2-3	10

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
$\overline{A11}$	B4-10	12	M44	INPUT	A11	B4-4	4,5
				$\overline{K9}$	A14	B4-4	9
				C30 $\overline{F8}$ M6	$\overline{F10}$	C2-7	8
				+VCC	A11	B4-4	4,5
					EXIT	B6-8	
					EXIT	C6-8	
A12	B1-8	8	M8	G G	$\overline{M5}$	B2-10	13
				M5	$\overline{M6}$	B3-5	2
A13	B4-10	6	M44	A14 G G	C1	B2-11	1
				$\overline{C1}$ G	$\overline{C2}$	B3-7	2
A14	B4-10	8	M44	A13 G G	C1	B2-11	2
				F11	C2	B3-6	4
A15	B5-10	8	M54	G	$\overline{F9}$	C2-9	4
				A8 G	F9	C3 9	11
					EXIT	B9-10	
					EXIT	C9-10	
A16	B4-4	11	M38	A17 G	F10	C4-7	11
				A17 G	F10	C4-7	3
					EXIT	B9-5	
					EXIT	C9-5	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
A17	C5-2	6	M99	A16 G	F10	C4-7	10
				A16 G	$\overline{F10}$	C4-7	4
A18	C3-5	6	M85	G			
				G	L51	C1-10	10
				$\overline{F5}$ $\overline{F3}$	C1	B3-8	9
				A11 $\overline{F6}$	$\overline{K5}$	B2-3	3
				A11 F6	$\overline{K6}$	B2-3	11
				$\overline{F5}$ M6	K35	B1-4	3
					EXIT	B5-13	
					EXIT	C5-13	
$\overline{A18}$	C3-5	3	M85	$\overline{L10}$	L51	C1-10	13
A19	B3-2	3	M28	K5	L11	B4-5	10
				$\overline{F4}$ K7	$\overline{F12}$	C5-8	9
					EXIT	B9-12	
					EXIT	C9-12	
A20	D6	6	M166	COL SEL			
$\overline{A20}$	D6	6	M139	A37	A24	M139-6D	9
				V7	L41	M171-3D	4*

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
A21	D6	3	M166	COL SEL			
$\overline{A21}$	D7	12	M143	F101 $\overline{F2}$	$\overline{A25}$	M142-6D	13
				V7	L41	M171-3D	5*
A22	D6	6	M167	COL SEL			
$\overline{A22}$	D6	3	M139	A39	$\overline{A26}$	M139-6D	12
				V7	L41	M171-3D	1*
A23	D6	3	M167	COL SEL			
$\overline{A23}$	D6		M167	V7	L41	M171-3D	6*
A24	D6	11	M167	COL SEL			
$\overline{A24}$	D6		M167	V7	L41	M171-3D	2*

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
A25	D6	8	M167	COL SEL			
$\overline{A25}$	D6		M167	V7	L41	M171-3D	11*
A26	D6	11	M166	COL SEL			
$\overline{A26}$	D6		M166	V7	L41	M171-3D	3*
A27	D6	8	M166	COL SEL			
$\overline{A27}$	D6	8	M142	V7	L41	M171-3D	12*
* = When connected to M171 for memory seal							
$\overline{A30}$		11	M165	ROW SEL			
$\overline{A31}$		8	M165	ROW SEL			

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
$\overline{A32}$		6	M165	ROW SEL			
$\overline{A33}$		3	M165	ROW SEL			
A35	C4-1	6	M90	L50	F14	C6-4	13
				$\overline{L50}$ C40	$\overline{F14}$	C6-1	11
A36	B2-6	6	M20	K13 $\overline{K28}$	L11	B3-3	9
				K13 $\overline{K41}$	A35	C4-1	5
					EXIT	B2-6	
					EXIT	C2-6	
*A37	C4-4	6	M93	$\overline{F3}$	$\overline{A20}$	D M139	4
*				$\overline{A20}$	$\overline{A24}$	D M139	10
				F3 $\overline{F104}$	F10	C4-7	13
					EXIT	C4-5	
*					EXIT	D4-5	
$\overline{A37}$	C4-4	8	M93	INPUT	A37	C4-4	4,5
				K35	L11	B2-5	4
				+VCC	A37	C4-4	5
					EXIT	B5-12	
					EXIT	C5-12	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
A38	B2-2	6	M16	L20 $\overline{F8}$	$\overline{C1}$	B2-8	5,6
				$\overline{F7}$ F3			
				$\overline{F2}$ $\overline{M1}$			
				$\overline{C1}$	$\overline{F5}$	C3-2	13
				A5 C40	K7	B1-6	2
				A9	K13	B1-5	13
				VCC	$\overline{C1}$	B2-8	
					EXIT	B2-7	
					EXIT	C2-7	
$\overline{A38}$	B2-2	3	M16	INPUT	A38	B2-2	4,5
				F7 A9	K14	B1-6	10
				+VCC	A38		
*A39	C5-4	11	M101	$\overline{F3}$	$\overline{A22}$	M139	1
				$\overline{A22}$	$\overline{A26}$	M139	13
					EXIT	C4-6	
					EXIT	D4-6	
$\overline{A39}$	C5-4	8	M101	INPUT	A39	C5-4	12,13
				K35 C40	$\overline{K34}$	C4-1	11
				+VCC	A39		
C1	B1-14	8	M14	$\overline{A2}$ F1	L11	B5-3	2
				C2	C20	B2-12	4
				G-INPUT	F8	C1-1	4
				G-INPUT	F8	C1-1	10
				G-INPUT	F7	C1-2	4

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
				G-INPUT	F7	C1-2	10
				F7-INPUT	F6	C1-3	10
				F106-INPUT	F5	C1-4	4
				A3	A2	B5-9	12
					EXIT	B5-5	
					EXIT	C5-5	
C101	C4-2	11	M91	F4	F3	C2-3	9
				F104	F3	C2-3	5
				F5	F4	C1-5	3,4
				F5	F4	C1-5	9,11
				+VCC	F4	C1-5	
C1	B1-14	6	M14	K87	F6	C3-3	3
				F5	F6	C3-3	4
				A38	F5	C3-2	1
				K35 T39 Z3	F1	C1-8	2
				T39 G	M6	B1-12	3
				C2	C30	B4-7	1
				C2	C40	B4-7	4
				INPUT, V1	C101	C4-2	12
				A13 G	C2	B3-7	13
				K22	A4	C3-5	13
					EXIT	B5-4	
					EXIT	C5-4	
C2	B1-13	8	M13	C1	C40	B4-7	5

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
$\overline{C2}$	B1-13	6	M13	G	M6	B2-9	13
				$\overline{C1}$	$\overline{C30}$	B4-7	2
				C1	$\overline{C20}$	B2-12	5
				$\overline{T7}$ $\overline{Z2}$	Z4	M121-7A	3
				$\overline{F11}$ $\overline{F15}$	$\overline{K80}$	M120-2A	1
				F11 F15	$\overline{K82}$	M120-2A	4
					WARM UP	M172-6A	5
					EXIT	B4-5	
					EXIT	A4-5	
C20	B2-12	8	M26	KO-$\overline{L20}$	A12	B1-8	11
				T39 G	$\overline{M6}$	B1-12	10
				T39 G	$\overline{C1}$	B1-14	9
				T39	$\overline{F15}$	M126-7A	10,11
				+VCC	$\overline{F15}$		
					EXIT	A4-7	
					EXIT	B4-7	
$\overline{C20}$	B2-12	6	M26	$\overline{C40}$	$\overline{M5}$	B2-9	4
				INPUT	C20	B2-12	9,10
				VCC	C20		
C30	B4-7	8	M41	$\overline{M6}$ $\overline{S2}$	M5	B1-11	10
				M6 S3	M5	B2-10	10
				T7	C37	B2-12	12
				T39	$\overline{C39}$	B4-8	9
				K35 $\overline{F6}$ $\overline{F14}$	F9	C2-6	6
				A9 G	F10	C2-8	6
				M6 $\overline{F8}$ $\overline{A11}$	F10	C2-7	6
				$\overline{T7}$ F8 G	F14	C6-5	2
				T7 T4	F11	C1-13	2

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
					EXIT	B9-7	
					EXIT	C9-7	
$\overline{C30}$	B4-7	3	M41	+VCC	C30		
				+VCC	C130		
				INPUT	C30	B4-7	9,10
				INPUT	C130	B4-7	12,13
				$\overline{A2}$ $\overline{K2}$	L11	B3-3	5
				A3	L21	B2-1	4
				T39	$\overline{L41}$	B4-3	9
C130	B4-7	11	M41	M1	S10	B4-6	1
					EXIT	B4-3	
					EXIT	A4-3	
C37	B2-4	8	M18	F8 G G	F11	C2-6	13
				G	$\overline{F14}$	C5-6	1
				L10 K6	A17	C5-2	4
				A5 $\overline{T4}$ G	$\overline{K22}$	C1-13	12
					EXIT	B6-10	
					EXIT	C6-10	
$\overline{C37}$	B2-12	11	M26	INPUT	C37	B2-4	9,10

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
C39	B4-8	6	M42	M1 S4	C1	B3-8	13
				G	C2	B1-13	5
				K35	$\overline{F14}$	C4-6	5
				$\overline{F11}$ $\overline{K9}$ G	$\overline{F14}$	C5-6	10
				K6 $\overline{F4}$ F14	L11	B5-8	2
				$\overline{F14}$ G	A14	B4-10	10
				K5 F14	$\overline{K51}$	M121-6A	10
					EXIT	A9-3	
					EXIT	B9-3	
					EXIT	C9-3	
$\overline{C39}$	B4-8	8	M42	INPUT	C39	B4-8	4,5
C40	B4-6	8	M40	G	$\overline{C2}$	B3-6	12
				T39	$\overline{C49}$	B4-8	12
				$\overline{L50}$ A35	$\overline{F14}$	C6-1	10
				L51 G	F14	C6-3	10
				G	L11	B4-5	1
				K46 F10 L10	$\overline{L31}$	B5-5	4
				G	$\overline{L31}$	B5-7	2
				G	L21	B2-1	10
				K6 F3	F11	C1-14	1
				A5 $\overline{F5}$ F6	$\overline{K1}$	B1-7	5
				A5 F5 F6	$\overline{K2}$	C1-8	13
				K35 $\overline{A39}$	$\overline{K34}$	C4-1	10
				K5	$\overline{K50}$	B5-4	5
				K9	$\overline{K90}$	B5-4	2
				A5 A38	K7	B1-6	13
				K5 F9	F11	C3-9	2
					EXIT	B2-5	
					EXIT	C2-5	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
$\overline{C40}$	B4-7	6	M41	INPUT	C40	B4-6	9,10,12,13
				$\overline{K50}$	F20	M125-5A	2
				$\overline{T39}$	$\overline{L41}$	B4-3	13
				$\overline{C20}$	$\overline{M5}$	B2-9	5
				+VCC	C40		
				+VCC	C40		
				+VCC	C40		
					EXIT	B4-4	
					EXIT	A4-4	
C49	B4-8	3	M42	M6 $\overline{K9}$ G	C1	B2-11	12
				A10 K50	F12	C5-8	4
				K6	F15	M126-7A	5
				K9 Z3	A13	B4-10	3
				F3	A19	B4-4	1
				K35 F1	K37	C2-1	10
				A9 F7	K87	C2-1	5
				F2 $\overline{L10}$	$\overline{F14}$	C3-6	8
					EXIT	A6-1	
					EXIT	B6-1	
					EXIT	C6-1	
$\overline{C49}$	B4-8	11	M42	INPUT	C49	B4-8	1,2
F1	C1-7	8	M64	K43 $\overline{A6}$	L30	M141-3D	4
				INPUT	$\overline{F101}$	C1-9	4,5
				$\overline{L39}$	$\overline{L50}$	C3-2	4
				K35	$\overline{L31}$	B6-3	5
				C1 A2	L11	B5-3	13
				$\overline{L30}$	A7	B6-2	5

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
				A2	A8	B5-10	4
				K28 F3	$\overline{K9}$	B1-6	4
				K35 C49	K37	C2-1	11
					EXIT	B3-6	
					EXIT	C3-6	
					EXIT	D3-6	
F101	C1-9	3	M66	$\overline{F2}$ $\overline{F3}$	$\overline{A21}$	M143-7D	3
				F2 $\overline{F3}$	$\overline{A23}$	M142-6D	13
				$\overline{A21}$ $\overline{F2}$	$\overline{A25}$	M142-6D	2
				F2 F3	$\overline{A27}$	M142-6D	9
				L10	$\overline{F14}$	C4-5	13
				Z3	F11	C1-12	4
				A2 T4	F10	C2-8	2
				K22	F3	C2-3	13
				A1	$\overline{L31}$	B5-6	1
					EXIT	B8-9	
					EXIT	C8-9	
					EXIT	D8-9	
$\overline{F1}$	C1-7	6	M64	INPUT	F101	C1-9	1,2
				K43 $\overline{T39}$	L10	M141-3D	10
				INPUT	LD 1	M168-8D	5
				A1	L11	B4-1	9
				K0 F4	A36	B2-6	5
				F2	$\overline{A39}$	C5-4	9
				$\overline{F2}$	$\overline{A37}$	C4-4	9
				$\overline{L10}$	A7	B6-2	3
				$\overline{L19}$	$\overline{L50}$	C3-2	2
					EXIT	B3-7	
					EXIT	C3-7	
					EXIT	D3-7	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
$\overline{F101}$	C1-9	6	M66	$\overline{Z3}$	F11	C1-12	2
				A2	$\overline{F9}$	C1-11	1
				K22	$\overline{F3}$	C2-3	3
F2	C1-6	12	M63	G	F1	C1-7	5
				$\overline{L10}$ C49	$\overline{F14}$	C3-6	4,5
				F101 $\overline{F3}$	$\overline{A23}$	M142-6D	4
				F101 F3	$\overline{A27}$	M142-6D	10
				K0 F4	$\overline{K28}$	B1-4	1
				$\overline{F1}$	$\overline{A39}$	C5-4	10
					EXIT	B3-13	
					EXIT	C3-13	
					EXIT	D3-13	
$\overline{F2}$	C1-6	13	M63	T39	$\overline{A6}$	B5-9	2
				$\overline{F1}$	$\overline{A37}$	C4-4	10
				F101 F3	$\overline{A21}$	M143-7D	1
				$\overline{A21}$ F101	$\overline{A25}$	M142-6D	1
				INPUT	LD-2	M168-8D	12
				K0 F3 F4	$\overline{K27}$	B1-7	12
				$\overline{L20}$ $\overline{F8}$			
				$\overline{F7}$ A38	$\overline{C1}$	B2-8	3
				F3 $\overline{M1}$			
				G	$\overline{F1}$	C1-7	9
				G K34 $\overline{T7}$	F3	C3-1	11
				T4 Z2			
				K6 K76	$\overline{F14}$	C6-1	1
					EXIT	B3-8	
					EXIT	C3-8	
					EXIT	D3-8	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
F3	C1-6	9	M63	A7 $\overline{F6}$ K34	F14	C6-5	12
				$\overline{F12}$	$\overline{F14}$	C4-5	9
				$\overline{L20}$ $\overline{F8}$ $\overline{F7}$	$\overline{C1}$	B2-8	4
				A38 $\overline{F2}$ $\overline{M1}$			
				A4	F2	C2-4	2
				K6 C46 G	F11	C1-14	2
				L20	L21	B1-1	2
				F101 F2	$\overline{A27}$	M142-6D	11
				C49	A19	B4-4	2
				K28 F1	$\overline{K9}$	B1-6	5
				K0 $\overline{F2}$ F4	$\overline{K27}$	B1-7	10
					EXIT	B3-11	
					EXIT	C3-11	
					EXIT	D3-11	
$\overline{F3}$	C1-6	8	M63	A18 $\overline{F5}$	C1	B3-8	11
				A4	$\overline{F2}$	C2-4	12
				A37 $\overline{F104}$	F10	C4-7	1
				F104	L11	B3-4	1
				$\overline{L20}$	L21	B1-1	4
				INPUT	LD-3	M168-8D	9
				A37	$\overline{A20}$	M139-6D	5
				F101 F2	$\overline{A21}$	M143-7D	2
				A39	$\overline{A22}$	M139-6D	2
				F101 F2	$\overline{A23}$	M142-6D	5
					EXIT	B3-9	
					EXIT	C3-9	
					EXIT	D3-9	
F4	C1-5	8	M62	F6 $\overline{F9}$	F3	C2-2	1
				C101	F3	C2-3	10
				F5	$\overline{K22}$	C4-3	1

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
				KO F2	$\overline{K28}$	B1-4	2
				K34 F6	$\overline{K40}$	B1-4	11
				KO F2 F3	K27	B1-7	9
				K34 G	K43	C4-1	13
				INPUT, V1	$\overline{F104}$	C3-4	2
				KO $\overline{F1}$	A36	B2-6	4
				G	F20	M125-5A	9
				EXIT	A5-2		
				EXIT	B5-2		
				EXIT	C5-2		
F104	C5-4	6	M101	$\overline{L50}$ G	F14	C6-3	5
				G	$\overline{F14}$	C4-5	3
				$\overline{F3}$	L11	B3-4	2
				$\overline{L30}$	L11	B3-4	4
				$\overline{B2}$	L11	B5-2	9
				$\overline{L10}$	L11	B3-4	13
				$\overline{L10}$	L11	B5-2	4
				G	L31	B4-3	5
				$\overline{F9}$	$\overline{A32}$	M165-5D	4
				F9	$\overline{A33}$	M165-5D	1
					EXIT	B6-3	
					EXIT	C6-3	
					EXIT	D6-3	
$\overline{F4}$	C1-5	6	M62	$\overline{F9}$	$\overline{A31}$	M165-5D	9
				F9	$\overline{A30}$	M165-5D	12
				INPUT, V1	F104	C5-4	5
				K34	$\overline{K42}$	C5-3	4
				$\overline{L10}$	F20	M125-5A	4
				$\overline{L10}$	L31	B4-3	3
				$\overline{F21}$	L11	B5-2	3
				$\overline{F21}$	L11	B5-2	13
				K6 C39 F14	L11	B5-8	4

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
				INPUT	LD4 (LAMP)	M163-6D	1
					EXIT	B5-1	
					EXIT	A5-1	
					EXIT	C5-1	
					EXIT	D5-1	
$\overline{F104}$	C3-4	3	M84	A37 $\overline{F3}$	F10	C4-7	2
				C101	$\overline{F3}$	C2-3	4
				K2 L53	$\overline{F14}$	C4-6	1
				G	$\overline{F14}$	C4-5	4
				A19 K7	F12	C5-8	10
						B6-1	12,13
					EXIT	B3-14	
					EXIT	C3-14	
F5	C1-4	8	M61	$\overline{F6}$	$\overline{A38}$	B2-2	1
				F7 M6	$\overline{A11}$	B4-10	1
				F4	$\overline{K22}$	C4-3	2
				A9 F6 $\overline{F7}$	K46	B2-7	2
				A5 F6 C40	$\overline{K2}$	C1-8	10
				L60	$\overline{L50}$	C3-8	4
				C101	F4	C1-5	5
				$\overline{C1}$	F6	C3-3	5
					EXIT	B5-9	
					EXIT	C5-9	
$\overline{F5}$	C1-4	6	M61	INPUT	LD-5	M163-6D	4
				A18 $\overline{F3}$	C1	B3-5	10
				C101	$\overline{F4}$	C1-5	10
				A9 $\overline{F6}$ G	L11	B4-2	3
				A5 $\overline{F6}$	K0	B2-3	1

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
				A5 F6 C40	$\overline{K1}$	B1-7	2
				A18 M6	$\overline{K35}$	B1-4	4
				$\overline{K9}$	F14	C6-4	9
					EXIT	B3-4	
					EXIT	C3-4	
					EXIT	D3-4	
F6	C1-3	8	M60	F9	$\overline{K43}$	C4-2	4
				A9 F5 $\overline{F7}$	K46	B2-7	4
				K34 F4	$\overline{K40}$	B1-4	10
				K42	$\overline{K41}$	C5-3	13
				A18 A11	$\overline{K6}$	B2-3	9
				A5 $\overline{F5}$ C40	$\overline{K2}$	C1-8	12
				A5 $\overline{F5}$ C40	$\overline{K1}$	B1-7	4
				F8	L11	B2-5	3
				F11	L51	C2-5	10
				F4 $\overline{F9}$	F3	C2-2	13
					EXIT	B5-10	
					EXIT	C5-10	
F106	C3-4	8	M84	K87	$\overline{F5}$	C3-2	10
				C1	F5	C1-4	3,5
$\overline{F6}$	C1-3	6	M60	INPUT	LD-6	M163-6D	9
				INPUT, V1	F106	C3-4	10
				K35 C30 $\overline{A4}$	$\overline{F9}$	C2-6	5
				K34 F3 A7	F14	C6-5	10
				A9 $\overline{F5}$ G	L11	B4-2	1
				A6 K34	A1	C5-2	1
				A5 $\overline{F5}$	K0	B2-3	13
				A18 A11	$\overline{K5}$	B2-3	5

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
				G	$\overline{K22}$	C4-3	5
				F5	$\overline{A38}$	B2-2	2
					EXIT	B3-5	
					EXIT	C3-5	
					EXIT	D3-5	
F7	C1-2	8	M59	F5 M6	$\overline{A11}$	B4-10	13
				$\overline{F8}$	$\overline{A18}$	C3-5	2
				A9 $\overline{A38}$	$\overline{K14}$	B1-6	11
				A9 C49	L87	C2-1	4
				$\overline{L20}$	L11	B3-1	3
				G	F6	C1-3	5
					EXIT	B2-1	
					EXIT	C2-1	
$\overline{F7}$	C1-2	6	M59	C1	$\overline{F6}$	C1-3	9,11
				$\overline{L20}$ $\overline{F8}$ A38	$\overline{C1}$	B2-8	11
				F3 $\overline{F2}$ $\overline{M1}$			
				$\overline{F8}$ $\overline{K9}$	$\overline{C2}$	B3-7	10
				INPUT	LD-7	M164-6D	9
				$\overline{L60}$	L11	B3-1	4
				$\overline{F8}$ M6	A5	B1-8	4
				A9 F5 F6	K46	B2-7	5
					EXIT	B3-1	
					EXIT	C3-1	
					EXIT	D3-1	
F8	C1-1	8	M58	M6	A9	B3-5	9
				F6	L11	B2-5	2
				C37 G-G	F11	C2-6	1
				C1	F7	C1-2	3,5

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
					EXIT	B2-2	
					EXIT	C2-2	
$\overline{F8}$	C1-1	6	M58	INPUT	LD-8	M164-6D	12
				C1	$\overline{F7}$	C1-2	9,11
				$\overline{T7}$ C30 G	F14	C6-5	4
				M6 C30 $\overline{A11}$	$\overline{F10}$	C2-7	5
				$\overline{L20}$ $\overline{F7}$ A38	$\overline{C1}$	B2-8	1
				F3 $\overline{F2}$ $\overline{M1}$			
				$\overline{F7}$ $\overline{K9}$	$\overline{C2}$	B3-7	11
				$\overline{F7}$ M6	A5	B1-8	3
				F7	$\overline{A18}$	C3-5	1
					EXIT	B6-7	
					EXIT	C6-7	
					EXIT	C6-7	
F9	C4-8	13	M97	G	A1	C5-1	4
				F104	$\overline{A33}$	M165-5D	2
				$\overline{K73}$	$\overline{F14}$	C6-2	13
				$\overline{F4}$ or V7	$\overline{A31}$	M165-5D	10
					EXIT	C4-2	
					EXIT	D4-2	
				INPUT	LD-9	M164-6D	1
				$\overline{K75}$	$\overline{F14}$	C6-2	9
				F6 F4	F3	C2-2	2
				$\overline{F104}$	$\overline{A30}$	M165-5D	13
				F104	A32	D5-2	5
				F10	A10	B5-10	1
					EXIT	B3-3	
					EXIT	C3-3	
					EXIT	D3-3	
					EXIT	D5-8	
					EXIT	A5-8	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
F10	C4-8	9	M97	$\overline{L40}$	L60	B6-2	1
				K46 $\overline{F11}$ G	$\overline{L41}$	B5-8	12
				K34	F11	C1-12	1
					EXIT	B9-4	
					EXIT	C9-4	
$\overline{F10}$	C4-8	8	M97	$\overline{L30}$	L60	B6-2	10
				T4	F11	C2-9	9
				K34	$\overline{F11}$	C5-7	2
				K46	$\overline{L31}$	B6-3	3
				K46 C40 L10	$\overline{L31}$	B5-7	13
				$\overline{F9}$	A10	B5-10	2
					EXIT	B9-9	
					EXIT	C9-9	
F11	C6-7	9	M112	F15 $\overline{C2}$	$\overline{K82}$	M120-2A	5
				F6	L51	C2-5	9
				A14	C2	B3-6	5
					EXIT	A8-4	
					EXIT	B8-4	
					EXIT	C8-4	
$\overline{F11}$	C6-7	8	M112	C39 $\overline{K9}$ G	$\overline{F14}$	C4-6	4
				F10 K46 G	$\overline{L41}$	B5-8	10
				F15 $\overline{C2}$	$\overline{K80}$	M120-2A	13
					EXIT	A8-3	
					EXIT	B8-3	
					EXIT	C8-3	
F12	C5-8	8	M105				
$\overline{F12}$		6	M105	F3	$\overline{F14}$	C4-5	10

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
F14	C6-7	13	M112	K9 Z3	C2	B3-8	5
				L51	$\overline{L53}$	C3-7	3
				K6 C39 $\overline{F4}$	L11	B5-8	5
				K5 C39	$\overline{K51}$	M121-6A	11
					EXIT	A8-1	
					EXIT	B8-1	
					EXIT	C8-1	
$\overline{F14}$	C6-7	12	M112	INPUT	LD-10	M164-6D	4
				C39 G	A14	B4-10	11
				$\overline{L51}$	$\overline{L53}$	C3-7	5
				K35 C30 F6	$\overline{F9}$	C2-6	8
					EXIT	B8-2	
					EXIT	C8-2	
					EXIT	D8-2	
F15	Bd A	8	M126	$\overline{F11}$ $\overline{C2}$	$\overline{K80}$	M120-2A	2
				F11 C2	$\overline{K82}$	M120-2A	3
$\overline{F15}$	Bd A	6	M126	Z1, K51, G	Z4	M124-6A	2
F20	Bd A	5	M131-4A				
F20	Bd A	6	M131-4A		F28 SET	M131-4A	12

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
F21	Bd A	8	M128-2A	K50	A16	B4-4	12
					EXIT	A1-13	
					EXIT	B1-13	
$\overline{F21}$	Bd A	9	M128-2A	$\overline{F4}$	L11	B5-2	1
				$\overline{F4}$	L11	B5-2	2
					OB1	M114-4A	4,5
					EXIT	B1-11	
					EXIT	A1-11	
F22	Bd A	13	M128-2A		F21 SET	M128-2A	10
$\overline{F22}$	Bd A	12	M128-2A	F104	L11	B5-2	10
					062	M114-4A	1,2
					F21 Reset	M128-2A	7
F23	Bd A	8	M129-2A		F22 SET	M128-2A	3
$\overline{F23}$	Bd A	9	M129-2A		F22 RESET	M128-2A	14
					OB3	M114-4A	12,13
F24	Bd A	13	M129-2A		F23 SET	M129-2A	10

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
$\overline{F24}$	Bd A	12	M129-2A		F23 RESET	M129-2A	7
					OB4	M114-4A	9,10
F25	Bd A	8	M130-2A		F24 SET	M129-2A	3
$\overline{F25}$	Bd A	9	M130-2A		F24 RESET	M129-2A	14
					OB5	M113-3A	4,5
F26	Bd A	13	M130-2A		F25 SET	M130-2A	10
$\overline{F26}$	Bd A	12	M130-2A		F25 RESET	M130-2A	7
F27	Bd A	8	M127-4A		F26 SET	M130-2A	3
F27	Bd A	6	M127-4A		F26 RESET	M130-2A	14
					OB7	M113-3A	12,13

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
F28	Bd A	8	M131-4A		F27 SET	M127-4A	3,4,5
$\overline{F28}$	Bd A	6	M131-4A		F27 RESET	M127-4A	3,4,5
					0B8	M113-3A	9,10
K0	B3-2	11	M28	C20 $\overline{L20}$	A12	B1-8	10
				F4 $\overline{F1}$	A36	B2-6	3
				$\overline{F2}$ F3 F4	$\overline{K27}$	B1-7	13
				F2 F4	$\overline{K28}$	B1-4	13
				G	L11	B2-5	1
K1	B2-4	3	M18	L30 G	L11	B3-3	1
				G	L31	B5-6	2
$\overline{K1}$	B1-7	6	M7	$\overline{K9}$ G	L31	B5-3	10
				INPUT	K1	B2-4	1,2
K2	C4-4	11	M93	$\overline{F4}$ $\overline{L53}$	$\overline{F14}$	C4-6	13,2
$\overline{K2}$	C1-8	8	M65	$\overline{K40}$	F14	C5-5	4
				$\overline{K28}$ $\overline{K34}$	F14	C6-1	3
				$\overline{A2}$ $\overline{C30}$	L11	B3-3	4
				INPUT	K2	C4-4	13,12
					EXIT	B5-6	
					EXIT	C5-6	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
K5	B3-2	6	M28	G	L11	B4-1	3
				A19	L11	B4-5	9
				G	$\overline{F14}$	C6-2	3
				C39 F14	$\overline{K51}$	M121-6A	9
				C4	$\overline{K50}$	B5-4	4
				F9 C30	F11	C3-9	13
					EXIT	A8-8	
					EXIT	B8-8	
					EXIT	C8-8	
$\overline{K5}$	B2-3	6	M17	INPUT	K5	B3-2	4,5
K6	B3-2	8	M28	$\overline{F2}$ K76	$\overline{F14}$	C6-1	13
				C49	F15	M126-7A	3,4
				C40 F3	F11	C1-14	13
				G	L11	B4-1	4
				C39 $\overline{F4}$ F14	L11	B5-8	1
				L20	F20	M118-6A	2
				C37 L10	A17	C5-2	3
					EXIT	A8-7	
					EXIT	B8-7	
					EXIT	C8-7	
$\overline{K6}$	B2-3	8	M17	$\overline{K50}$	F20	M125-5A	13
				INPUT	K6	B3-2	9,10
					EXIT	A4-2	
					EXIT	B4-2	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
K7	B1-5	3	M5	G	L11	B2-5	10
				G	$\overline{F14}$	C5-6	3
				A19 $\overline{F4}$	$\overline{F12}$	C5-8	11
					EXIT	B5-3	
					EXIT	C5-3	
K9	B1-5	8	M5	K92	$\overline{F14}$	C6-2	4
				F14 Z3	C2	B3-8	4
				C49 Z3	A13	B4-10	4
				C40	$\overline{K90}$	B5-4	1
					EXIT	B2-13	
					EXIT	C2-13	
$\overline{K9}$	B1-6	6	M6	INPUT	K9	B1-5	9,10
				$\overline{A11}$	A14	B4-4	10
				K1 G	$\overline{L31}$	B5-3	9
				L53 G	L11	B4-2	4
				C39 $\overline{F11}$ G	$\overline{F14}$	C4-6	8
				$\overline{K5}$	F14	C6-4	10
				C49 M6 G	C1	B2-11	10
				M6 G	C2	B3-7	5
				$\overline{F7}$ $\overline{F8}$	$\overline{C2}$	B3-7	9
					EXIT	B2-14	
					EXIT	C2-14	
K13	B1-5	11	M5	K28	F14	C5-7	9
				A36 K28	L11	B3-3	10
				K41 A36	A35	C4-1	4
					EXIT	B9-6	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
					EXIT	C9-6	
K14	B1-5	6	M5	L60	L21	B1-1	9
$\overline{K14}$	B1-6	8	M6	L20 $\overline{K27}$ $\overline{K35}$	L21	B1-2	4
				INPUT	K14	B1-5	4,5
K22	C4-3	8	M92	G	F11	C1-12	9
				F101	F3	C2-3	1
				F1	F3	C2-3	2
$\overline{K22}$	C1-13	8	M70	INPUT	K22	C4-3	9,10
				$\overline{C1}$	A4	C3-5	12
K27	B2-4	6	M18	L10	L21	B1-1	13
$\overline{K27}$	B1-7	8	M7	INPUT	K27	B2-4	4,5
				L20 K14 K35	L21	B1-2	5

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
K28	B1-3	3	M3	F1 F3	$\overline{K9}$	B1-6	3
$\overline{K28}$	B1-4	12	M4	INPUT	K28	B1-3	1,2
				$\overline{K2}$ $\overline{K34}$	F14	C6-1	4
				K13	$\overline{F14}$	C5-7	10
				A36 K13	L11	B3-3	11
					EXIT	B9-1	
					EXIT	C9-1	
K34	C4-2	3	M91	F10	F11	C1-12	13
				$\overline{F10}$	$\overline{F11}$	C5-7	1
				$\overline{T7}$ $\overline{T4}$	F3	C3-1	3
				$\overline{Z2}$ $\overline{F2}$ G			
				T7 L20	$\overline{F3}$	C2-2	3
				$\overline{F6}$ F3 A7	F14	C6-5	9
				G	$\overline{L50}$	C3-8	3
				A6 $\overline{F6}$	A1	C5-2	2
				F6 F4	$\overline{K40}$	B1-4	9
				$\overline{F4}$	$\overline{K42}$	C5-3	5
				F4 G	$\overline{K43}$	C4-1	2
					EXIT	B3-2	
					EXIT	C3-2	
$\overline{K34}$	C4-1	8	M90	INPUT	K34	C4-2	1,2
				$\overline{K2}$ K28	F14	C6-1	5
K35	B1-3	8	M3	C1 T39 Z3	F1	C1-8	1
				C30 F6 F14	F9	C2-6	4

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
				C39	$\overline{F14}$	C5-6	9
				$\overline{A37}$	L11	B2-5	2
				G	L21	B2-1	2
				F1	$\overline{L31}$	B6-3	4
				C40 $\overline{A39}$	$\overline{K34}$	C4-1	9
				C49 F1	K37	C2-1	9
					EXIT	B2-3	
					EXIT	C2-3	
$\overline{K35}$	B1-4	6	M4	INPUT	K35	B1-3	9,10
				L20 $\overline{K14}$ $\overline{K27}$	L21	B1-2	6
K37	C2-1	8	M72	$\overline{A4}$	$\overline{F1}$	C1-9	13
				S22 G	F2	C2-1	13
				G	$\overline{F2}$	C2-4	10
K40	B1-3	6	M3	L53	F10	C3-8	9
				$\overline{L53}$	$\overline{F10}$	C3-7	9
				L53	A1	C5-1	1
				A6	A15	B5-10	10
					EXIT	B2-9	
					EXIT	C2-9	
$\overline{K40}$	B1-4	8	M4	INPUT	K40	B1-3	4,5
				$\overline{K2}$	$\overline{F14}$	C5-5	5
					EXIT	B5-14	
					EXIT	C5-14	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
K41	C5-3	3	M100	L50	F10	C3-8	13
				$\overline{\text{L50}}$	$\overline{\text{F10}}$	C3-7	1
$\overline{\text{K41}}$	C5-3	11	M100	INPUT	K41	C5-3	1,2
				K13 A36	A35	C4-1	3
K42	C5-3	8	M100	F6	$\overline{\text{K41}}$	C5-3	12
				L53 $\overline{\text{A6}}$	F9	C3-9	3
				G	$\overline{\text{F9}}$	C1-11	10
$\overline{\text{K42}}$	C5-3	6	M100	INPUT	K42	C5-3	9,10
				G - G	A1	C5-2	9
K43	C4-2	8	M91	$\overline{\text{L50}}$	A1	C5-1	12
				G	$\overline{\text{L50}}$	C6-6	3
				$\overline{\text{T39}}$ $\overline{\text{F1}}$	L10	D3-1	9
				F1 A6	L30	D3-1	5
					EXIT	C4-1	
					EXIT	D4-1	
$\overline{\text{K43}}$	C4-1	12	M90	INPUT	K43	C4-2	9,10
				A7	L50	C6-6	4

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
K46	B5-4	11	M48	F10 $\overline{F11}$ G	$\overline{L41}$	B5-8	13
				C40 $\overline{F10}$ L10	$\overline{L31}$	B5-7	1
				$\overline{F10}$	$\overline{L31}$	B6-3	2
K50	B5-4	8	M48	C49 A10	F12	C5-8	3
				F21	A16	B4-4	12
					EXIT	B9-14	
					EXIT	C9-14	
K50	B5-4	6	M48	INPUT	K50	B5-4	9,10
				CLEAR	$\overline{K150}$	M116-2A	4,5
				$\overline{K6}$	F20	M125-5A	1
				$\overline{C40}$	F20	M125-5A	3
				EXIT	A4-1		
				EXIT	B4-1		
K51	'A' BOARD	6	M118	I6107	PRESET F28	M117-3A	4
				I6106	F27	M117-3A	2
				I6105	F26	M117-3A	10
				I6104	F25	M117-3A	13
				I6103	F24	M115-1A	4
				I6102	F23	M115-1A	2
				I6101	F22	M115-1A	10
				I6108	F21	M115-1A	13

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
$\overline{K51}$	'A' Bd	8	M121	INPUT	K51	M118-6A	4,5
				$\overline{F15}$ Z1 G	Z4	M124-6A	1
$\overline{K73}$	'A' Bd			F9	F14	C6-2	1
					EXIT	A4-13	
					EXIT	C4-13	
$\overline{K75}$	'A' Bd			INPUT	$\overline{K175}$		
				EXIT	A2-1		
				EXIT	F3-14		
$\overline{K175}$	'A' Bd			$\overline{F9}$	$\overline{F14}$	C6-2	10
					EXIT	A4-12	
					EXIT	C4-12	
$\overline{K76}$	'A' Bd			INPUT	K176		
					EXIT	A2-2	
					EXIT	F3-13	
K176	'A' Bd			K6 F2	F14	C6-1	2
					EXIT	C4-11	
					EXIT	A4-11	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
K82	'A' Bd				EXIT	A2-5	
					EXIT	F3-10	
K87	C2-1	6	M72	$\overline{C1}$	F6	C3-3	2
				F106	$\overline{F5}$	C3-2	9
K90	B1-3	11	M3	L30	$\overline{L91}$	B6-3	13
				L90	L31	B5-6	9
$\overline{K90}$	B5-4	3	M48	INPUT	K90	B1-3	12,13
				$\overline{K93}$ L90	$\overline{L91}$	B5-7	4
K92	MAG CARD BD	8	M170	K9	$\overline{F14}$	C6-2	5
					EXIT	C4-7	
					EXIT	B4-7	
$\overline{K93}$	MAG CD BD	3	M170	$\overline{K90}$ L90	$\overline{L91}$	B5-7	5
					EXIT	B7-13	
					EXIT	D7-13	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
K94	MAG CD BD	6	M170		$\overline{L91}$	B6-3	9,10
					EXIT	B7-14	
					EXIT	D7-14	
K80	'A' Bd				EXIT	A2-3	
						F3-12	
K150	'A' Bd				EXIT	A2-4	
					EXIT	F3-11	
L10	'D' Bd	8	M145	K27	L21	B1-1	1
				$\overline{F10}$ C4 K46	$\overline{L31}$	B5-7	3
				G	L11	B3-1	10
				G	L11	B4-1	1
				F101	$\overline{F14}$	C4-5	1
				L30	$\overline{F14}$	C5-7	5
				$\overline{A2}$	F8	C3-3	13
				K6 C37	A17	C5-2	5
					EXIT	B3-10	
					EXIT	C3-10	
					EXIT	D3-10	
$\overline{L10}$	'D' Bd	6	M145	$\overline{A18}$	L51	C1-10	1
				F2 C49	$\overline{F14}$	C3-6	6
				F104	L11	B3-4	12
				F104	L11	B5-2	5
				$\overline{F4}$	$\overline{L31}$	B4-3	2
				L30	$\overline{L31}$	B5-5	1
				$\overline{F4}$	F20	M125	5

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
				$\overline{F1}$	A7	B6-2	2
					EXIT	D6-2	
					EXIT	C6-2	
					EXIT	B6-2	
					EXIT	A6-2	
L11	B5-3	6	M47	ACCUM		M154-4D	11,12
				INPUT			
					EXIT	B7-1	
					EXIT	D7-1	
L19	'D' Bd	13	M150	G INPUT	L10	M145-3D	3,4
				L41 Z1	GS RECORD	M143-7D	9
				+VCC	$\overline{L19}$	M141-3D	1,2,13
$\overline{L19}$	'D' Bd	12	M141	G INPUT	$\overline{L10}$	M145-3D	10,11
				L41 Z1	GS RECORD	M143-7D	3
				$\overline{F1}$	$\overline{L50}$	C3-2	3
				+VCC			
					EXIT	C4-4	
					EXIT	D4-4	
L20	'D' Bd	5	M149	A2	F8	C3-3	10
				Z3	F11	C1-11	4
				F3	L21	B1-1	3
				K14 K27 K35	L21	B1-2	8
				G	L21	B2-2	10
				K6	F20	M118-6A	1

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
				K34 T7	F3	C2-2	5
						A4-9	
					EXIT	B4-9	
					EXIT	C4-9	
					EXIT	D4-9	
$\overline{L20}$	D1	6	M149	$\overline{F8}$ $\overline{F7}$ A38	$\overline{C1}$	B2-8	12
				$\overline{F3}$ $\overline{F2}$ $\overline{M1}$			
				Z3	F11	C1-11	2
				F7	L11	B3-1	2
				F3	L21	B1-1	5
				C20 K0	A12	B1-8	9
					EXIT	B6-13	
					EXIT	C6-13	
					EXIT	D6-13	
L21	B2-6	8	M20	INST REG		M159-4D	11,12
				INPUT			
					EXIT	B7-2	
					EXIT	D7-2	
L30	D4	8	M146	$\overline{L10}$	$\overline{L31}$	B5-5	2
				G	$\overline{L31}$	B5-6	5
				K90	L91	B6-3	1
				K1 G	L11	B3-3	13
				L10	F14	C5-7	4
					EXIT	B8-5	
					EXIT	C8-5	
					EXIT	D8-5	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
L30	D4	6	M146	F104	L11	B3-4	5
				$\overline{F10}$	L60	B6-2	9
				F1	A7	B6-2	4
					EXIT	B7-4	
					EXIT	D7-4	
L31	B5-5	11	M49	FA "A" RD		M140-6D	1
					EXIT	B4-14	
					EXIT	D4-14	
$\overline{L31}$	B5-6	8	M50	FA "A" RECORD		M140-6D	4
				INPUT	L31	B5-5	12,13
					EXIT	B7-3	
					EXIT	D7-3	
L39	M147-2D	5	M147	INPUT	L30		
				+VCC			
$\overline{L39}$	M147-2D	6	M147	INPUT	$\overline{L30}$		
				F1	$\overline{L50}$	C3-2	5
				+VCC			
					EXIT	C4-3	
					EXIT	D4-3	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
L40	D Bd	9	M147				
$\overline{L40}$	D Bd	8	M147	F10	L60	B6-2	13
					EXIT	B7-7	
					EXIT	D7-7	
L41	B2-2	11	M16	G5 RECORD		M143	4,11
$\overline{L41}$	B5-8	8	M52	INPUT	L41	B2-2	12,13
				WARM UP CKT		M172-6A	12
					EXIT	A4-8	
					EXIT	B4-8	
L50	C4-4	3	M93	K41	F10	C3-8	1
				G	$\overline{L53}$	C1-10	2
				G	$\overline{F14}$	C5-5	10
				A35	F14	C6-4	12
$\overline{L50}$	C3-8	6	M88	K41	$\overline{F10}$	C3-7	13
				G	$\overline{L53}$	C1-10	4
				F104 G	F14	C6-3	4
				C40 A35	F14	C6-1	9
				INPUT	L50	C4-4	1,2
				K43	A1	C5-1	13

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
L51	C1-10	8	M67	INPUT	$\overline{L51}$	C2-5	1,2
				F14	$\overline{L53}$	C3-7	2
				C40 G	F14	C6-3	11
$\overline{L51}$	C2-5	3	M76	G	$\overline{F14}$	C5-6	5
				$\overline{F14}$	L53	C3-7	4
L53	C2-5	11	M76	$\overline{K9}$ G	L11	B4-2	6
				K40	A1	C5-1	2
				$\overline{A6}$	$\overline{F9}$	C2-9	12
				K42 $\overline{A6}$	F9	C3-9	4
				K40	F10	C3-8	10
$\overline{L53}$	C1-10	6	M67	INPUT	L53	C2-5	12,13
				K40	$\overline{F10}$	C3-7	10
				K2 $\overline{F104}$	$\overline{F14}$	C4-6	3
L60	B6-2	8	M56	INPUT	$\overline{L60}$	B2-4	12
				F5	$\overline{L50}$	C3-8	5
				F14	L21	B1-1	10
					EXIT	B6-11	
					EXIT	C6-11	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
$\overline{L60}$	B2-4	11	M18	$\overline{F7}$	L11	B3-1	5
L90	M149-2D	9	M149	K90	$\overline{L31}$	B5-6	10
				$\overline{K40}$ $\overline{K90}$	$\overline{L91}$	B5-7	6,8
					EXIT	B7-6	
					EXIT	D7-6	
$\overline{L90}$	M149-2D	8	M149				
L91	B5-5	8	M49	$\overline{Z1}$	FA-B RECORD	M140-6D	12
					EXIT	B7-8	
					EXIT	D7-8	
$\overline{L91}$	B6-3	8	M57	$\overline{Z1}$	FA-B RECORD	M140-6D	9
				INPUT	L91	B5-5	9,10
					EXIT	B7-5	
					EXIT	D7-5	
LD-1	D BD				EXIT	D1-9	
					EXIT	G1-6	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
LD-2	D BD				EXIT	D1-8	
					EXIT	G1-7	
LD-3	D BD				EXIT	D1-7	
					EXIT	G1-8	
LD-4	D BD				EXIT	D1-6	
					EXIT	G1-9	
LD-5	D BD				EXIT	D1-5	
					EXIT	G1-10	
LD-6	D BD				EXIT	D1-4	
					EXIT	G1-11	
LD-7	D BD				EXIT	D1-3	
					EXIT	G1-12	
LD-8	D BD				EXIT	D1-2	
					EXIT	G1-13	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
LD-9	D BD				EXIT	D1-10	
					EXIT	G1-5	
LD-10	D BD				EXIT	D1-11	
					EXIT	G1-4	
LD-11	D BD				EXIT	D1-12	
					EXIT	G1-3	
LD-12	D BD				EXIT	D1-13	
						G1-2	
LD-13	(W $\overline{102}$)				EXIT	A1-10	
	A BD				EXIT	G2-5	
M1	B4-9	6	M43	C39 S4	C1	B3-8	1
				S3	C2	B3-6	1
				C30	S10	B4-6	2,4,5
				S6 $\overline{W2}$	A3	B1-8	12

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
M1	B4-9	3	M43	INPUT	M1	B4-9	3,4,5
				M2 F2 F3	C1	B2-8	2
				F138 F7			
				F8 L20			
				G	C2	B3-6	10
M5	B1-11	8	M11	S2	M6	B2-9	1
				A12	M6	B3-5	1
				M6	M1	B4-9	1
				WARM UP		M172-6A	2
					EXIT	A4-6	
						B4-6	
M5	B1-11	6	M11				
M6	B1-12	8	M12	C30 S3	M5	B2-10	9
				C49 K9 G	C1	B2-11	13
				K9 G	C2	B3-7	4
				F8 C30 A11	F10	C2-7	4
				G	F14	C6-4	5
				G	L11	B3-4	10
				F8 F7	A5	B1-8	5
				F8	A9	B3-5	10
				F5 F7	A11	B4-10	2
				A18 F5	K35	B1-4	5
					EXIT	B6-9	
					EXIT	C6-9	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
M6	B1-12	6	M12	INPUT	LD-11	M163-6D	12
				INPUT	Warm-Up	M172-6A	4
				M5	$\overline{M1}$	B4-9	2
				C30 $\overline{S2}$	M5	B1-11	9
				G	$\overline{M5}$	B2-9	10
					EXIT	A8-14	
					EXIT	B8-14	
					EXIT	C8-14	
S1	B5-1	3	M45	M5	M6	B2-9	2
$\overline{S1}$	Req Sel SW				S1	B5-1	1,2
					EXIT	B1-1	
					EXIT	G2-14	
S2	B2-12	3	M26	$\overline{M6}$ C30	M5	B1-11	11
$\overline{S2}$	RUN SW				S2	B2-12	1,2
					EXIT	B1-2	
					EXIT	G-2-13	
					EXIT	G-7-11	
S3	B5-1	6	M45	M6 C30	$\overline{M5}$	B2-10	11
				M1	C2	B3-6	2

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
$\overline{S3}$	HALT SW				S3	B5-1	4,5
					EXIT	B1-3	
					EXIT	G2-12	
					EXIT	G7-10	
S4	B5-1	8	M45	C39 M1	C1	B3-8	2
$\overline{S4}$	MOMENTARY CONTACT				S4	B5-1	9,10
	POSITIONS OF REG.				EXIT	B1-7	
	SEL. SW				EXIT	G2-8	
					EXIT	G7-6	
S6	B6-1	8	M55	M1 $\overline{W2}$	A3	B1-8	13
$\overline{S6}$	B6-1	6	M55	$\overline{S16}$	S6	B6-1	9
S7-B	POWER BUTTON			INPUT	WARM-UP	M173-6A	1
					EXIT	A1-5	
					EXIT	G2-10	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
S8	READY BUTTON			INPUT			
					WARM-UP NORM CLOSED	M173-6A	10
					NORM OPEN	M132-5A	5
					EXIT	A1-4	
					EXIT	G2-11	
S10	B4-6	6	M40	S31	$\overline{S20}$-$\overline{S30}$	BRD G	
					EXIT	B1-9	
					EXIT	G6-13	
S16	REG. SEL. SW				$\overline{S6}$	B6-1	5
					EXIT	A1-14	
					EXIT	B1-14	
					EXIT	G2-1	
$\overline{S16}$	REG. SEL. SW			$\overline{S6}$	S6	B6-1	10
					EXIT	B1-8	
						G2-7	
$\overline{S20}$	DISPL. BD.				F8	C1-1	2
					F7	C1-2	2
					F6	C1-3	2
					F5	C1-4	2
					F4	C1-5	2
					F3	C1-6	6
					F2	C1-6	2
					F1	C1-7	2

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
					EXIT	C1-2	
					EXIT	G4-13	
$\overline{S21}$	DISPL BD			PRESET	F1	C1-7	13
					EXIT	C1-10	
						G4-5	
$\overline{S22}$	DISPL BD			K37 G	F2	C2-1	2
					EXIT	C1-9	
						G4-6	
$\overline{S23}$	DISPL BD			G G	F3	C2-2	11
					EXIT	C1-8	
					EXIT	G4-7	
$\overline{S24}$	DISPL BD			PRESET	F4	C1-5	13
					EXIT	C1-7	
						G4-8	
$\overline{S25}$	DISPL BD			PRESET	F5	C1-4	13
					EXIT	C1-6	
					EXIT	G4-9	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
$\overline{S26}$	DISPL BD			PRESET	P6	C1-3	13
					EXIT	C1-5	
					EXIT	G4-10	
$\overline{S27}$	DISPL BD			PRESET	F7	C1-2	13
					EXIT	C1-4	
					EXIT	G4-11	
$\overline{S28}$	DISPL BD			PRESET	F8	C1-1	13
					EXIT	C1-3	
					EXIT	G4-12	
$\overline{S29}$	DISPL BD			G - G SET	F14	C6-3	1
					EXIT	C1-11	
						G4-4	
$\overline{S30}$	DISPL BD			G	$\overline{F14}$	C5-7	12
					EXIT	C1-12	
					EXIT	G4-3	
T4	B1-10			Z2	$\overline{T7}$	B1-9	9
				$\overline{T7}$ G	$\overline{C2}$	B1-13	10
				$\overline{T7}$	T39	B4-9	10
				$\overline{T7}$ G	M5	B1-11	4

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
				F101 A2	F10	C2-8	3
				$\overline{F10}$	F11	C2-9	10
					EXIT	B9-8	
					EXIT	C9-8	
$\overline{T4}$	B1-10	6	M10	Z2	T7	B1-9	3,4
				K34 $\overline{T7}$ Z2	F3	C3-1	5
				$\overline{F2}$ G			
				WARM UP		M172-6A	10
				A2	$\overline{F10}$	C2-7	3
				$\overline{T7}$ C30	$\overline{F11}$	C1-13	5
				A5 C37 G	$\overline{K22}$	C1-13	10
						A6-5	
					EXIT	B6-5	
					EXIT	C6-5	
T7	B1-9	8	M9	Z2	T4	B1-10	3,4
				K34 L20	$\overline{F3}$	C2-2	4
				C30	$\overline{C37}$	B2-12	13
					EXIT	B2-10	
						C2-10	
$\overline{T7}$	B1-9	6	M9	INPUT	$\overline{T4}$	B1-10	9
				T4 G	$\overline{C2}$	B1-13	9
				WARM UP		M172-6A	9
				T4 G	$\overline{M5}$	B1-11	3
				T4	$\overline{T39}$	B4-9	9
				K34 T4	F3	C3-1	4
				Z2 F2 G			
				C30 $\overline{T4}$	$\overline{F11}$	C1-13	4
				F8 C30 G	F14	C6-5	5

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
				C2 Z2	Z4	M121-7A	4
					EXIT	A6-6	
					EXIT	B6-6	
					EXIT	C6-6	
T39	B4-9	11	M43	C20 G	$\overline{C1}$	B1-14	10
				C30	$\overline{C39}$	B4-8	10
				C40	$\overline{C49}$	B4-8	13
				$\overline{C1}$ G	M6	B1-12	4
				C20 G	$\overline{M6}$	B1-12	11
				K35 C1 Z3	F1	C1-8	4
				G	F14	C6-6	1
				C20	$\overline{F15}$	M126-7A	9
				C20	$\overline{L41}$	B4-3	10
				$\overline{F2}$	$\overline{A6}$	B5-9	1
					EXIT	B8-6	
					EXIT	C8-6	
					EXIT	A8-6	
$\overline{T39}$	B4-9	8	M43	K43 $\overline{F1}$	L10	D3	11
				G	F14	C6-6	10
				$\overline{C40}$	$\overline{L41}$	B4-3	1
				INPUT	T39	B4-9	12,13
					EXIT	B6-12	
					EXIT	C6-12	
					*EXIT	D6-12	
V1	C4-3	11	M92	$\overline{F6}$	F106	C3-4	0
				F4	$\overline{F104}$	C3-4	1
				F4	F104	C5-4	4
				CLEAR	F9	C4-8	2

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
				CLEAR	F10	C4-8	6
				C1	C101	C4-2	13
V2	C5-4	3	M101	CLEAR	$\overline{F11}$	C6-7	6
				PRESET	F12	C5-8	13
				CLEAR	$\overline{F12}$	C5-8	2
V3	B2-7	8	M21	PRESET/CLEAR	T7	B1-9	2,13
				PRESET/CLEAR	T4	B1-10	2,13
				CLEAR	$\overline{M5}$	B1-11	2
				PRESET	M6	B1-12	13
				PRESET	C2	B1-13	13
				CLEAR	$\overline{C1}$	B1-14	2
V4	A6	8	M124		$\overline{W2}$	M123	9,10,12
	A BD	8	M124	PRESET	F20	M131-4A	4
				CLEAR	$\overline{F20}$	M131-4A	1
				CLEAR	$\overline{F15}$	M126-7A	2
				CLEAR	$\overline{F28}$	M131-4A	10
				CLEAR	$\overline{F27}$	M127-4A	2
V5	D BD	6	M144	PRESET	Z2	M148-2D	4
				CLEAR	$\overline{Z2}$	M148-2D	1
				PRESET	Z3	M148-2D	10
				CLEAR	$\overline{Z3}$	M148-2D	13
				PRESET	L90	M149-2D	10
				CLEAR	L90	M149-2D	13
				PRESET	L40	M147-2D	10

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
				CLEAR	$\overline{L40}$	M147-2D	13
				PRESET	L39	M147-2D	4
				CLEAR	$\overline{L39}$	M147-2D	1
				CLEAR	$\overline{L20}$	M149-2D	1
V6	D BD	11	M169	PRESET	L30	M146-4D	13
				CLEAR	$\overline{L30}$	M146-4D	2
				CLEAR	$\overline{L10}$	M145-3D	2
V7	D BD	3	M169	MEMORY UNSEAL *	L41	M171-3D	4,5,1,6,2,
							11,3,12
			* JUMPER CONNECTED TO V7 TO UNSEAL PAIR OF TRACKS				
			1602	$\overline{F9}$	$\overline{A30}$	M165-5D	12
			ONLY	F9	$\overline{A31}$	M165-5D	9
W1	'A' BD			FA-A, FA-B	EXIT	A8-10	
	WARM UP			G.S. RECORD		D8-10	
	CIRCUIT			INHIBIT			
W2	'A' BD						
$\overline{W2}$	'A' BD			PRESET	M5	B1-11	13
				"	$\overline{M6}$	B1-12	2
				"	C1	B1-14	13

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
				"	C2	B1-13	2
				"	F14	C6-7	2
				INPUT	LD	M122-4A	1,2,4,5
				M1 & S6	A3	B1-8	1
				PRESET	L10	M145-3D	13
				"	L20	M149-2D	4
					EXIT	A8-12	
					EXIT	B8-12	
					EXIT	C8-12	
					EXIT	D8-12	
W110	'A' BD			INHIBIT DEVICES	EXIT	A3-9	
				DURING WARM UP	EXIT	F1-6	
$\overline{Z1}$	'D' BD	8	M144	L39		M147-2D	3
				L40		M147-2D	11
				L90		M149-2D	11
				L10		M145-3D	12
				L20		M149-2D	3
				Z2		M148-2D	3
				Z3		M148-2D	11
Z2	'D' BD	5	M148		T7	B1-9	5
					T7	B1-9	10,11
					F3	C3-1	6
					EXIT	B4-10	
					EXIT	C4-10	
					EXIT	D4-10	

SIGNAL	GENERATED		PKG.NO.	USED WITH	ON NET	LOCATION	PIN
	LOCATION	PIN					
$\overline{Z2}$	'D' BD	6	M148		T4	B1-10	5
					Z4	M121-7A	5
					EXIT	A8-13	
					EXIT	B8-13	
					EXIT	D8-13	
Z3	'D' BD	9	M148	F14, K9	C2	B3-8	3
				K35, $\overline{C1}$, T39	F1	C1-8	5
				F101	F11	C1-12	5
Z4	A Bd	6	M123	ENABLE	F27	M127-4A	12
				BUFFER	F26	M130-2A	1
				REGISTER	F25	M130-2A	5
					F24	M129-2A	1
					F23	M129-2A	5
					F22	M128-2A	1
					F21	M128-2A	5
				INPUT	Z4	M116-2A	9,10
$\overline{Z4}$	A BD	8	M116-2A		F28	M131-4A	11

INTERFACE SIGNAL GLOSSARY

PIN	NAME	DESCRIPTION
3	+18 volts DC	Signal to control application of AC power to the motors and power supplies in a peripheral device. This line will go high when power is applied to the processor and will remain high until power is removed from the processor.
5	CLEAR	This signal will go high whenever the processor has accepted a byte of data from a peripheral device. The duration of this signal will be 40 microseconds. The type of information that was accepted, data or status, will be indicated to the device by the condition of the Status Control line.
6	STATUS CONTROL	This line will be high when the processor attempts to sample the status indicators in a peripheral device and will be low when data is to be read. The high or low condition of this line will be stable for 40 microseconds before the processor strobes the input busses, and will remain stable for 40 microseconds after the strobe. The period after the strobe will be defined by the CLEAR signal described above. This signal is used for other purposes within the system and may be expected to vary in a random fashion except at the intervals described above.
7	INPUT BUSY	This signal will be high whenever there is no data ready for delivery to the processor from an input device. The processor normally holds this bus high through a resistor to +18 volts to ensure a busy condition if no devices are connected or if none of the connected devices are selected. When a device is selected, it <u>will pull the signal low</u> when a character is ready to be delivered to the processor and return the signal to its high condition within 40 microseconds of the rise of the CLEAR signal associated with the reading of the character. This signal will not be changed by the reading of status information.

INTERFACE SIGNAL GLOSSARY (CONTINUED)

PIN	NAME	DESCRIPTION
8	INHIBIT	This signal is generated when power is present at the processor, but the processor is not in the READY state. This condition will exist during the initial application of AC power to the processor or whenever a line fluctuation occurs that forces the processor out of the READY state. The signal should be used by the peripheral devices to establish initial conditions of their control circuits.
9	SELECT COMMON	This signal will go high for 40 microseconds whenever the processor wishes to change the settings of the Select Flipflops in the peripheral devices. The data that controls the setting of these flipflops will be placed on the output busses 40 microseconds before the rise of this signal and will remain there during the 40 microsecond Common signal and for 40 microseconds thereafter.
10	DATA COMMON	This signal will go high whenever the processor is transferring data to a peripheral device. The duration of the signal will be 40 microseconds. The data to be transferred will be placed on the output busses 40 microseconds prior to the rise of this signal and will remain there for the duration of the Common signal and for 40 microseconds thereafter.
11 T H R U 18	Ob1 T H R U Ob8	These eight signals represent the eight output busses used to transfer data from the processor to a peripheral device. The type of data is determined by the Select Common or Data Common signal that will accompany the data.

INTERFACE SIGNAL GLOSSARY (CONTINUED)

PIN	NAME	DESCRIPTION
19	OUTPUT BUSY	This signal will be high whenever a selected peripheral device is not ready to accept a transfer of data from the processor. The processor normally holds this signal high through a resistor +18 to ensure a busy condition if no devices are connected or if connected devices are not selected. When a device is selected, it will pull the signal low whenever it is ready to accept a character from the processor and will return the signal to its high condition within 40 microseconds after the rise of the DATA COMMON signal.
21 T H R U 28	Ib1 T H R U Ib8	These eight signals represent the eight input busses used to transfer information from a peripheral device to the processor. A selected device will place either data information or status information on these lines as determined by the STATUS CONTROL signal. When data, as opposed to status, information is placed on these lines, it must be stable for at least 25 microseconds prior to pulling the INPUT BUSY signal to the low condition that will permit the processor to read the information.