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PADLA™

Programmable Asynchronous Dual Line Adapter

CONTAINS:

- INSTALLATION SPECIFICATION
- PROGRAMMING SPECIFICATION
- MAINTENANCE SPECIFICATION
- SCHEMATICS

PADLA INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification covers installation of the 200520 Programmable Asynchronous Dual Line Adapter (PADLA). The assembly consists of a standard half-board and cable assembly. The half-board must be strapped to a blank half-board of an active half-board to be installed in a chassis designed for full boards. The PADLA may be used in either right or left half positions as required.

2. INSTALLATION

2.1 Unpacking

The module assembly should be unpacked carefully and inspected for damage prior to installation.

2.2 Location

The PADLA, strapped to a blank or active half-board may be installed in any I/O slot. After installing the module, remove the RACKO/TACKO strap located on the back panel between terminals 222 and 122 of the selected slot.

2.3 Cables

The supplied cable is connected between the cable connector at the edge of the PADLA and the cable entry panel. Note that the flat wire connector is polarized. The two DA-15-P connectors are marked 1 and 2 to indicate each channel.

3. ADJUSTMENTS

Baud rates for Clock Select 1 and 0 are selected with the indicated hexadecimal switches. The Clock 1 Switch will select the baud rate for DOS and OS/MT. Clock rates are as follows:

3. ADJUSTMENTS (cont'd.)

POSITION	BAUD
0	OFF
1	19200
2	50
3	75
4	134.5
5	200
6	600
7	2400
8	9600
9	4800
A	1800
B	1200
C	2400
D	300
E	150
F	110

4. DEVICE ADDRESS

The addresses of each channel is set with the indicated hexadecimal switches. Addresses can only be set to an even boundary, e.g. a setting of X'11' will respond to address X'10 for Receive and X'11' for Transmit. Two switches are associated with each address.

Channels must not have the same address or the address of any device on the multiplexer bus.

5. OPTIONS

The following options for each of the channels are selected per the following:

Position		Function When On
1	:	Full Duplex Operation Channel 1

5. OPTIONS (cont'd.)

Position		Function When On
2	:	Disable CL2S Status Channel 1
3	:	Disable DSRDY Status Channel 1
4	:	Disable CARR Status Channel 1
5	:	Disable CL2S Status Channel 2
6	:	Disable DSRDY Status Channel 2
7	:	Disable CARR Status Channel 2
8	:	Full Duplex Operation Channel 2

When the switch is on (rocker down, red dot next to OFF), the above function(s) will be selected.

Care should be exercised to insure that the hexadecimal rotary switches are properly centered in their detent. If difficulties are encountered during installation, these switches should be carefully reset at the proper detent by rocking the selector slightly about the desired position.

PADLA PROGRAMMING SPECIFICATION

1. INTRODUCTION

The PADLA provides two independant interfaces between the Multiplexer or Selector Channel Bus of an Interdata Processor. These RS-232-C compatible channels will connect a wide variety of Modems or Data Terminals in either half-duplex or full-duplex mode.

Each of the two channels has two consecutive addresses: even for Receive and HDX Transmit, and odd for FDX Transmit. Interrupts are generated for Receive and Transmit of each channel. The PADLA is fully software-compatible with the Single Line Adapter (PASLA) from Interdata.

Each of the two channels are fully independant. Commands are separate for each channel as are status bits. Both channels, however, must be set to half of full duplex.

2. PROGRAMMING INSTRUCTIONS

Standard Processor byte I/O instructions are used to communicate with the PADLA.

2.1 I/O Instructions

2.1.1 Sense Status This instruction is used to detect if data transfers are complete and correct, and to detect the status of the data set. The mode and function of the PADLA modify the Status Register. Tables 1 and 2 should be consulted for proper definition.

2.1.2 Output Command This instruction is used to change the PADLA mode from Receive to Transmit, to select data format, select interrupts and to service the Data Set. Two command bytes are required for each channel.

2.1.3 Write Data This instruction is used to load the PADLA Output Register with a byte of data.

2.1.4 Read Data This instruction will read an assembled byte into the Processor.

2.1.5 Acknowledge Interrupt This instruction is used to service PADLA interrupts. Status will be returned per Tables 1 & 2.

2.2 Status and Command Bytes

		0	1	2	3	4	5	6	7
RCV Status		OV	PF	FR	RCR	RBSY	$\overline{\text{DSRDY}}$+OV +PF+FR	CARR OFF	RING
WRT HDX Status		0	$\overline{\text{CL2S}}$	0	RCR	TBSY	$\overline{\text{DSRDY}}$	0	RING
WRT FDX Status		0	$\overline{\text{CL2S}}$	0	0	TBSY	0	0	0
CMD 1	RCV	DIS	EN	DTR	ECHO PLEX	RCT/ DTB	TRANS LB	WRT	1
	WRT	DIS	EN						
CMD 2		X	CLK	BIT SEL		STOP BIT	PARITY		0

TABLE 1. PADLA STATUS & COMMAND DATA

PADLA MODE	STATUS MODE
RCV - HDX - EVEN ADDR	RCV
RCV - HDX - ODD ADDR	RCV
RCV - FDX - EVEN ADDR	RCV
RCV - FDX - ODD ADDR	WRT FDX
WRT - HDX - EVEN ADDR	WRT HDX
WRT - HDX - ODD ADDR	WRT HDX
WRT - FDX - EVEN ADDR	RCV
WRT - FDX - ODD ADDR	WRT FDX

TABLE 2. STATUS MODES

STATUS

OV — This bit is set if the current received character overwrites an unread character. The error condition is reset by reading the current character.

PF — This bit is set if the parity of the received character is not equal to the protrammed parity. This bit will be inactive if no parity is selected, and will be reset at the end of the next character without error.

FR — This bit is set to indicate that the current received character has no stop bit(s). An all-zero character with this bit set may indicate a line break. This bit will be reset at the end of the next valid transition.

RCR — Reverse Channel Receive (SB). This bit will be active to indicate a line space condition of the half-duplex data set. If the data set is not equipped with the Reverse Channel Option, or the Hardware Supress Option is selected, this bit will be inactive.

RBSY — When this bit is low, the Adapter is ready to transfer data to the processor. If an OV condition occurs, a Read Data instruction must be issued to set the RBSY bit to a high state. This bit is set if Data Set Ready (CC) is off.

EX — OV + PF + FR + $\overline{\text{DATA SET READY}}$. This bit is set if one or more of the previous conditions occur.

CARR OFF — This bit will indicate the state of the CF signal from the data set. When this bit is set, the incoming data is not valid.

RING This bit will indicate the state of the CE signal from the Data Set.

$\overline{\text{CL2S}}$ This bit is set to indicate the state of the CB signal from the Data Set. When this bit is set, the modem can no longer transmit data.

TBSY When this bit is low, the Adapter is ready to transfer Data from the processor. If Clear to Send (CB) is off, or Data Set Ready (CC) is off, or the adapter character is full, this bit will be set.

2.3 PADLA Commands

Command 1. This command is selected by setting bit 7. Two PADLA commands are required to select the desired operating mode of each channel.

DIS/EN DIS/EN bits are separate for the Receive and Transmit side. To change DIS/EN on the Receive side, issue a command with WRT:0, and the desired DIS/EN function. To change DIS/EN on the Transmit side, issue a WRT:1 command with the desired DIS/EN function. Because the WRT bit is gated to the Data Set as Request to Set, it is essential that a WRT:0 command be followed by a WRT:1 command when in FDX operation. In HDX operation, the odd address has interrupts disabled.

DISABLE	ENABLE	
0	0	No change
0	1	Enable
1	0	Disable (Interrupt Queued)
1	1	Complement (Change State)

DTR — When this bit is active, the Data Terminal Ready (CD) signal from the PADLA to the Data Set is activated. When on, it allows automatic answering of incoming calls, and allows the Data Set to remain in the Data mode. If this bit is held off, it does not allow automatic answering of calls and causes an existing connection to be disconnected.

ECHO PLEX — When set, the data received from the Data Set on the BB line is transmitted back to the Data Set on the BA line. The PADLA will also analyze the character. This bit must not be set while transmitting a character.

RCT/DTB — Reverse Channel Transmit (SA) or Data Terminal Busy for 202C or 103 type Data Sets. This bit should be set to one to satisfy the RS-232-C requirements: When set, a Mark state will be transmitted on the reverse channel, when reset a space will be transmitted on the reverse channel. With Data Sets equipped with the DTB option, the inactive condition of this bit will cause the terminal to be busy and not allow a call to be answered.

TRANS LB — When set, a continuous space will be transmitted to the Data Set. This bit will override the ECHO-PLEX mode, and will cause transmitted data to be garbled.

WRT — When this bit is set, Request to Send (CA) is gated to the Data Set if Data Set Ready (CC) is active. When this bit is reset, Request to Send (CA) will deactivate after the last data transfer has been completed. Busy will be forced active during this mode change and will be active until a character is recieved.

Command 2. This command is selected by resetting bit 7.

CLK — This bit selects one of two available baud rates for the PADLA. If this bit is set, the rate selected by Clock 1

switch is selected. If this bit is reset, the rate selected by Clock 0 switch is selected. These clock rates are fully independant (e.g. 110 baud and 9600 baud may be selected).

BIT SEL — These bits select the number of data bits/character

2	3	Number of Data Bits
0	0	5
0	1	6
1	0	7
1	1	8

If less than eight bits are selected, the data must be right-justified before a Write Data is issued. In the Read mode, the data returned to the Processor with the Read Data command will be right-justified, with unused bits in a Zero state.

STOP BIT

0 = 1 STOP BIT
1 = 2 STOP BITS

The receiver only samples the first Stop Bit.

PARITY

5	6	PARITY
1	0	ODD
1	1	EVEN
0	X	NONE

If Parity is selected, the transmitter will append a parity bit after the last data bit, and the receiver will examin this bit position for parity agreement. PF status will be set if received parity is not the selected parity. If parity is disabled, a stop bit will reappend after the last data bit, and receiver parity is disabled.

2.4 Interrupts

A list of interrupting conditions is shown in the following table:

STATUS BIT	HDX		FDX	
	RCV	WRT	RCV	WRT
RING → 1	X	X	X	
CARR OFF → 1	X		X	
CARR OFF → 0	X		X	
RCR → 1	X	X	X	
RCR → 0	X	X	X	
DSRDY → 0	X	X	X	
BUSY → 0	X	X	X	X
$\overline{\text{CL2S}}$ → 1	X	X		X

PADLA MAINTENANCE SPECIFICATION

1. INTRODUCTION

The Programmable Asynchronous Dual Line Adapter (PADLA) provides two independant interfaces between an Interdata multiplexer bus and half or full duplex asynchronous data sets and/or local terminals. RS-232-C interface specifications, with the exception of the interface connector, are observed.

Data are transferred by bytes between the CPU and interface. Data are transferred bit serial to the Data Set/Terminal. The Adapter contains the hardware necessary to control the data communication network.

The 7"X15" PADLA will replace two Interdata PASLA units while maintaining full software compatibility and hardware compatibility.

2. SCOPE

This specification covers the operation and maintenance of the PADLA.

3. FUNCTIONAL DESCRIPTION

The entire circuitry of the PADLA is contained on one four-layer circuit board. The two internal layers are used for power and ground distribution. Extensive use of Low-power Schotkey TTL and CMOS integrated circuits insures maximum reliability.

3.1 Address Decoding

The address and data section of the multiplexer bus is shown on sheet 1 of the schematics. The seven most significant bits of the bus are decoded by the address logic, U25 (CH1) and U34 (CH2). The eighth bit (LSB) is used to set the odd FF, U32-5. NAND gate U6-6 is active when data bits 6 and 7 are low to accomodate the 10-bit addressing requirements of 32-bit processors.

Multiplexers U27, 26, 35, 36 select the decoded address of the interrupting channel during an interrupt service. The multiplexers also select the status of the read or write side of each channel. The three-state output of the multiplexers is bussed with the data output of the UARTs.

3.2 Control/Command Logic

Control logic is shown on sheet 3.

Data requests or status requests (U4-6) and channel select (U3-11) or ATSYNO (U12-6) will cause the 7438 buss drivers to be gated 'ON' (U13-6 and U12-11). Additionally, a SYNC response will be sent (U20-8). Data requests are decoded into channel 1 or 2 by U2-3 and U2-6. Status multiplexers U70, 71, 72 will default to address 1 (1ADR1).

'Data Available' commands are qualified by U2-11 and U2-8, directly driving the individual channel UARTs.

Commands are qualified both by address decode and data bit 15 for command 1 or 2. Command 2 drives the UARTs and baud select flip-flops U59 (sheet 4).

3.3 Interrupts

Each of the seven interrupt-generating signals are monitored by the edge-detecting logic on sheet 5. These leading and trailing edge-detectors rely upon the intrinsic delay of the 74C14 invertor (approx. 100 nS). These signals are combined in HDX mode and split if FDX by U91. The individual interrupts are used to set the 'D' flip-flops on sheet 6 (U74 and 73). The J-K flip-flops, (U57 and 58), arm or disarm the interrupts. The priority encoder, U46, is used to insure that Receive Channel 1 has priority over Transmit Channel 1. These events have priority over Channel 2 Receive, with Channel 2 Transmit having lowest priority. Decoder U64 is used to reset each interrupt flip-flop as it is serviced.

Latch, U55, insures that an interrupt occurring during a service period will not cause the priority to shift and thereby erroneously reset a pending interrupt. U37-11 is used to delay interrupt servicing until SYN1 to allow the logic to stabilize. U19-12 inhibits the ATNO output after each service until the logic can clear itself.

3.4 RS-232-C Logic

3.4.1 Receive The 1489A RS-232-C receivers (sheet 2) are Slew-rate limited to reduce the effects of cross-talk. Three of the signals may be disabled by using the attribute switch on the front edge of the PADLA. These inputs are compatible with a ± 15V swing.

3.4.2 Transmit The 1488 RS-232-C transmitters are powered by ± 9V to allow an output swing of ± 6V. These drivers are shown on sheet 5.

3.5 Local Clock

3.5.1 Baud Rate U78 is used to generate the independant baud rates for each channel. The Q_0 output (pin 1) selects, via U79, switch 6 or 5. U68-3 and U68-8 select the positive or negative phase of Q_0 to clock flip-flops U60.

3.5.2 Power Supply U78-3 output is further divided by U87 to produce a 19,200 Hz signal to drive U40-3+6. This signal is amplified by the Quad PNP array (U48) and drives transformer, T1. The ± 9V output drives the RS-232-C drivers, U98 and U99.

4. TESTING

The PADLA may be tested using the Interdata PALS off-line test and the test connector described in the Appendix.

APPENDIX I

CONNECTOR ASSIGNMENTS

DA-15-P Channel Connectors

PIN	NAME	
1	AB	Signal Ground
2	CD	Data Terminal Ready
3	CB	Clear To Send
4	CF	Received Line Signal Detector
5	GROUND	
6	SBA	Secondary Transmitted Data
7	AA	Protective Ground
8	SBB	Secondary Receive Data
9	CE	Ring Indicator
10	GROUND	
11	BB	Received Data
12	CC	Data Set Ready
13	CA	Request To Send
14	BA	Transmitted Data
15	GROUND	

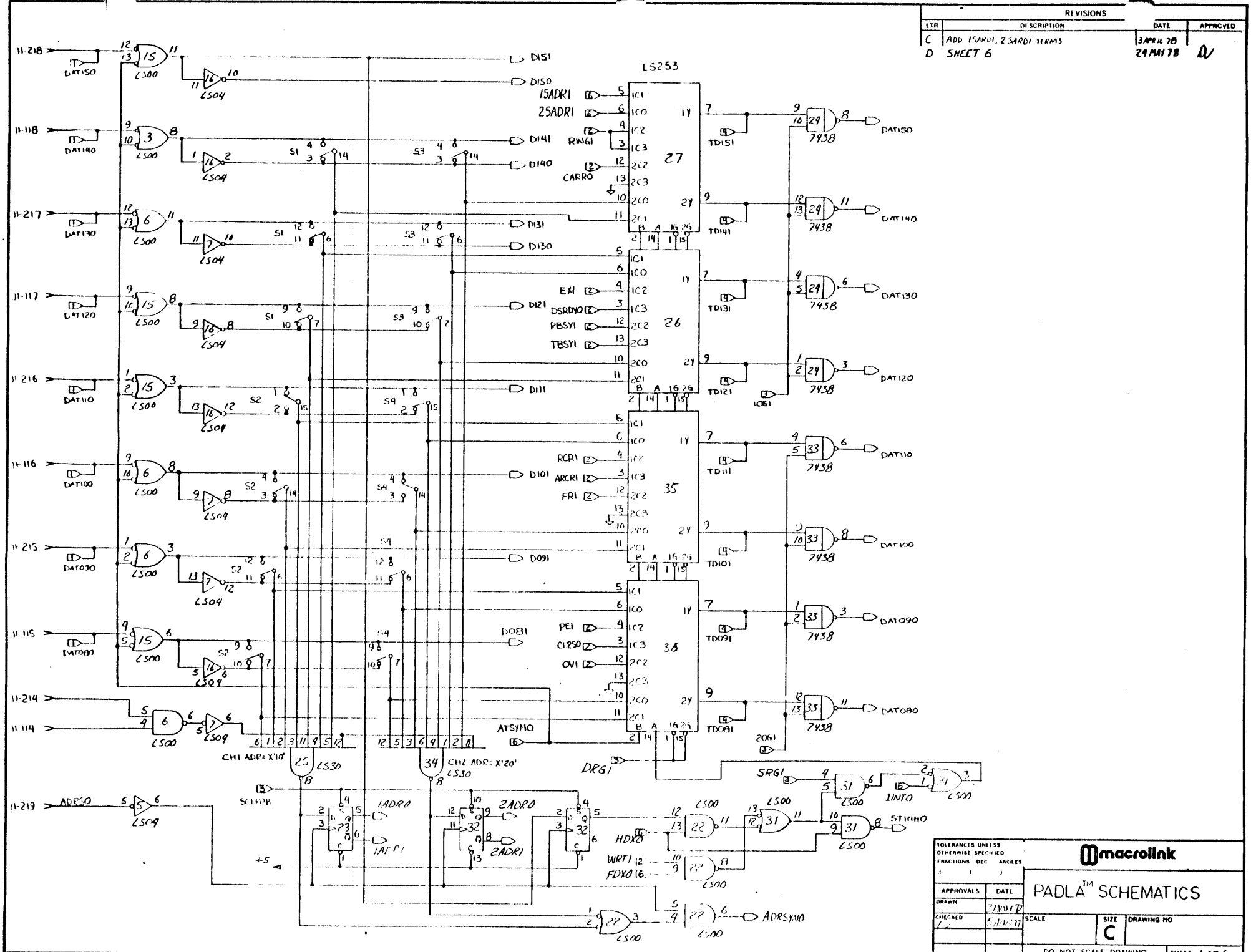
RECOMMEND PADLA TO CRT CABLE

PATLA DA-15-S		CRT DB-25-S	
2	DS RUN	6	Cable assemblies should be made
11	TDATA	2	with twisted pair. Terminate
12	DTR	20	the ground side of each pair to
14	RDATA	3	Pin 15 of the PATLA connector;
15	GND	1,7	Pin 1 and 7 or the CRT connector.

APPENDIX II

TEST CONNECTOR FOR PALS TEST

J1 DA-15-S		J2 DA-15-S
2	.....	4, 12
3	.....	13
4, 12	.....	2
6	.....	9, 8
8, 9	.....	6
11	.....	14
13	.....	3
14	.....	11


REVISIONS
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C ADD 1SADRI, 2SADRI TERMS 3APRIL 78
D SHEET 6 24MAY78
LS253
DAT15O
DAT14O
DAT13O
DAT12O
DAT11O
DAT1OO
DAT09O
DAT08O
DI51
DI50
DI41
DI40
DI31
DI30
DI21
DI11
DI01
DO91
DO81
1SADRI
2SADRI
RNGI
CARRO
EXI
DSRDYO
PBSYI
TBSYI
RCRI
ARCRI
FRI
PEI
CLRSO
OVI
ATSYNO
TDI51
TDI41
TDI31
TDI21
TDI11
TDI01
TDO91
TDO81
1O61
2O61
DAT15O
DAT14O
DAT13O
DAT12O
DAT11O
DAT1OO
DAT09O
DAT08O
DRGI
SRGI
1INTO
STSYNO
HDXO
WRTI
FDXO
ADRSYNO
CH1 ADR= X'10'
CH2 ADR= X'20'
SCLKOO
1ADRO
1ADRI
2ADRO
2ADRI
ADRSO
+5
LS00
LS04
LS09
LS30
7438
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
APPROVALS DATE
DRAWN
CHECKED
macrolink
PADLA™ SCHEMATICS
SCALE
SIZE C
DRAWING NO
DO NOT SCALE DRAWING
SHEET 1 OF 6

REVISIONS			
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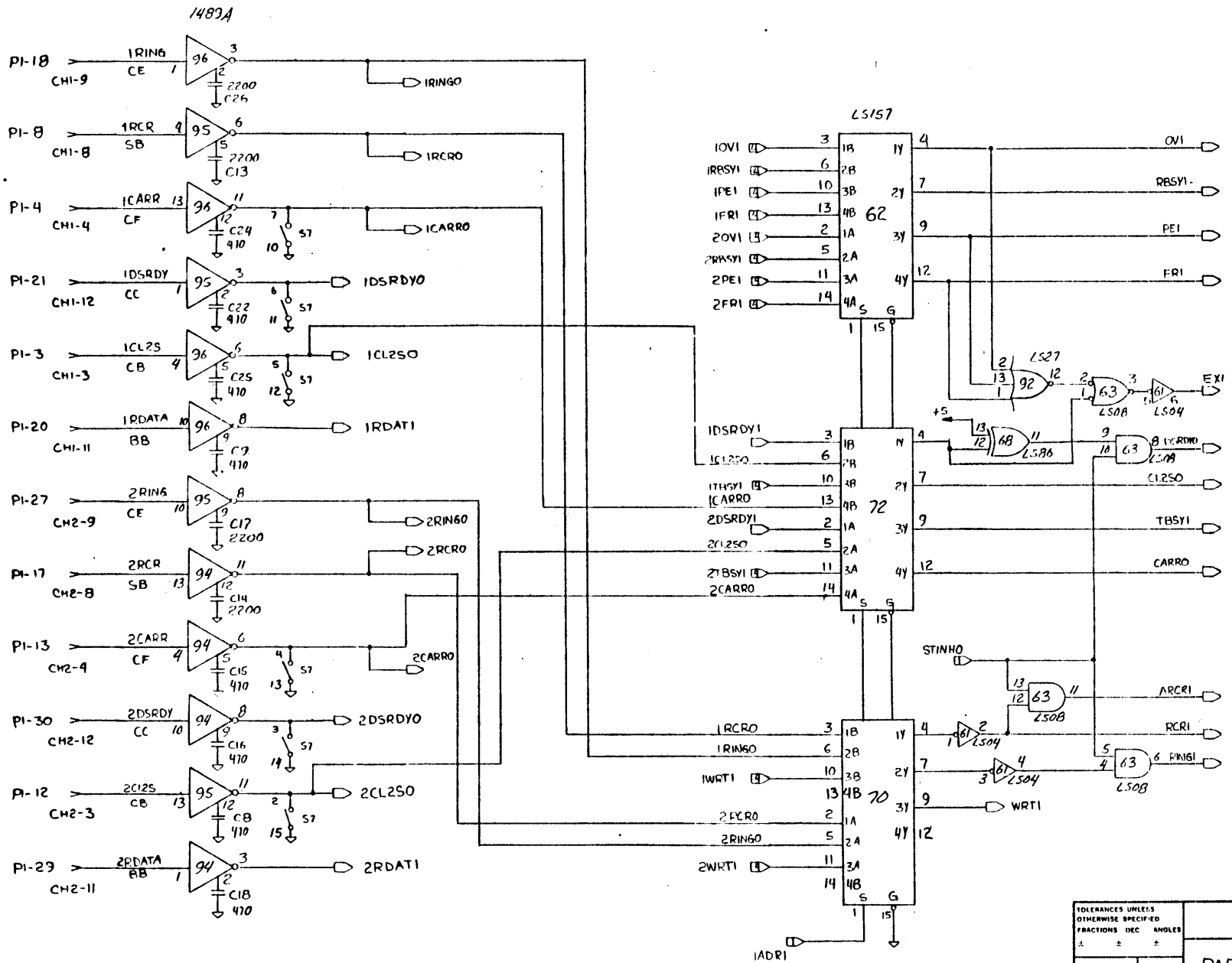

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN	27 MAR 77
CHECKED	6 APR 77

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SCALE	SIZE	DRAWING NO.
	C	

DO NOT SCALE DRAWING | SHEET 2 OF 6

REVISIONS			
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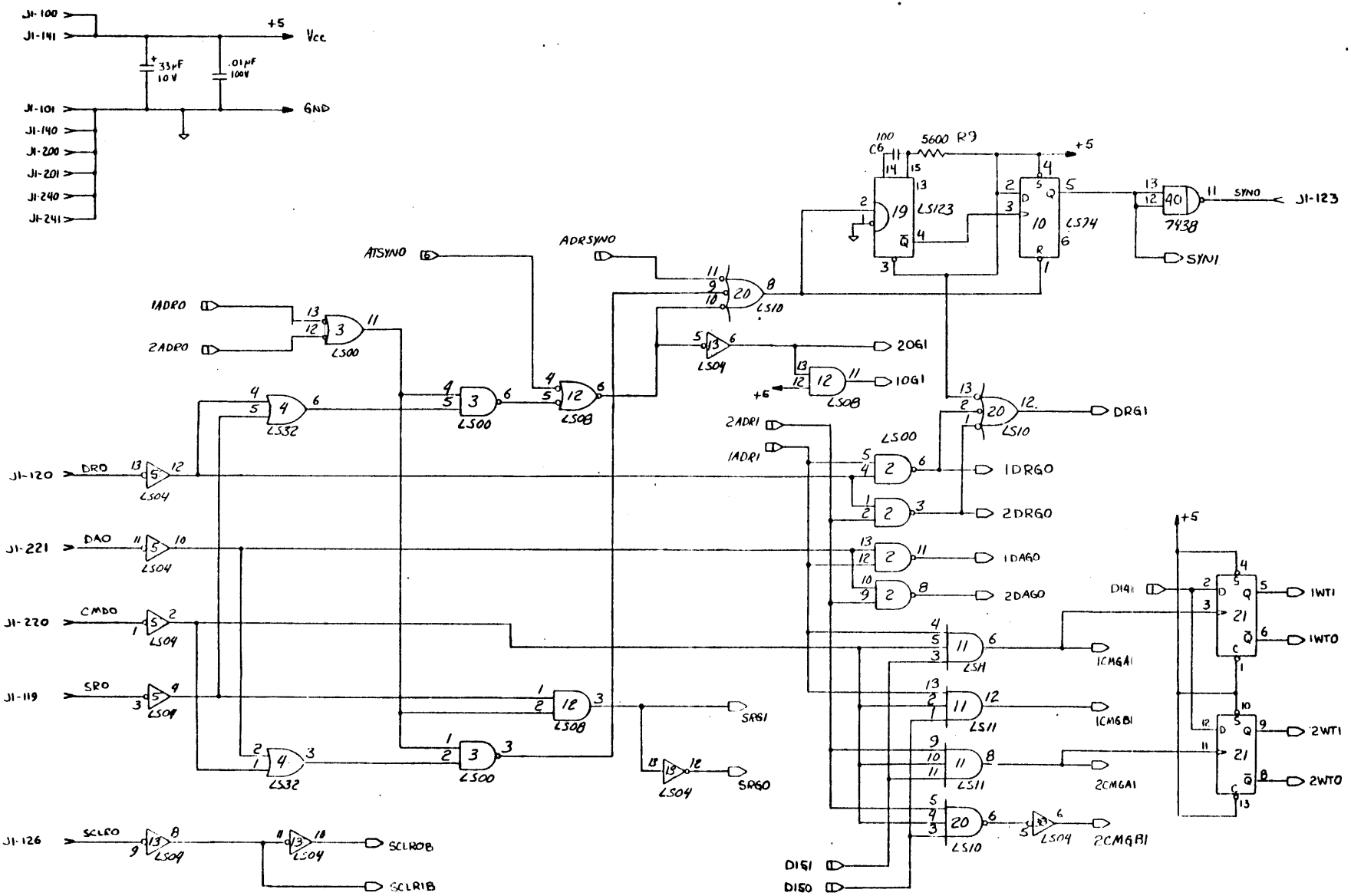
C	R9 IS 560Ω, REMOVE PSINHO		



TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN	11 AUG 77
CHECKED	5 AUG

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SCALE	SIZE	DRAWING NO.
	C	

DO NOT SCALE DRAWING — SHEET 3 OF 6

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
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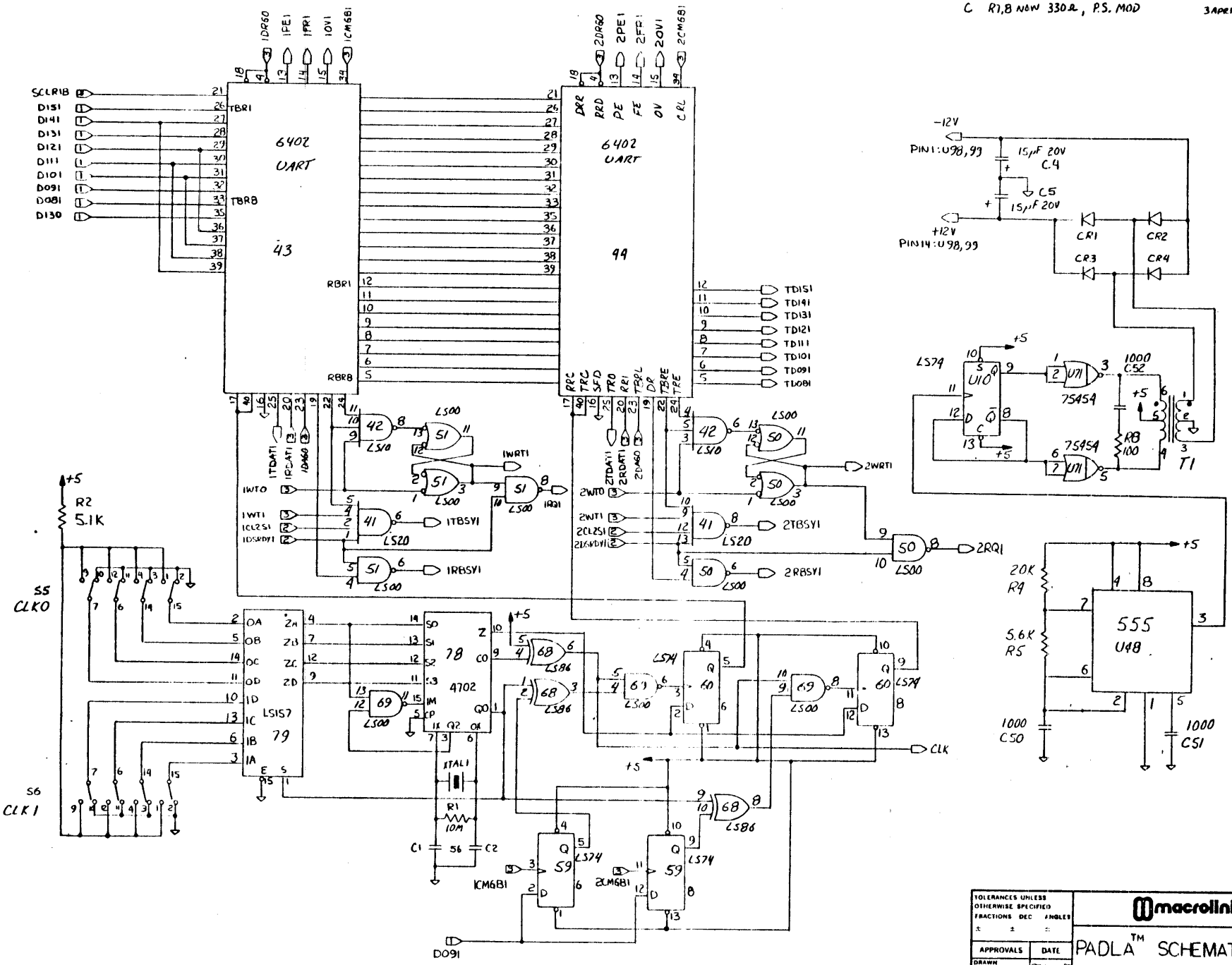
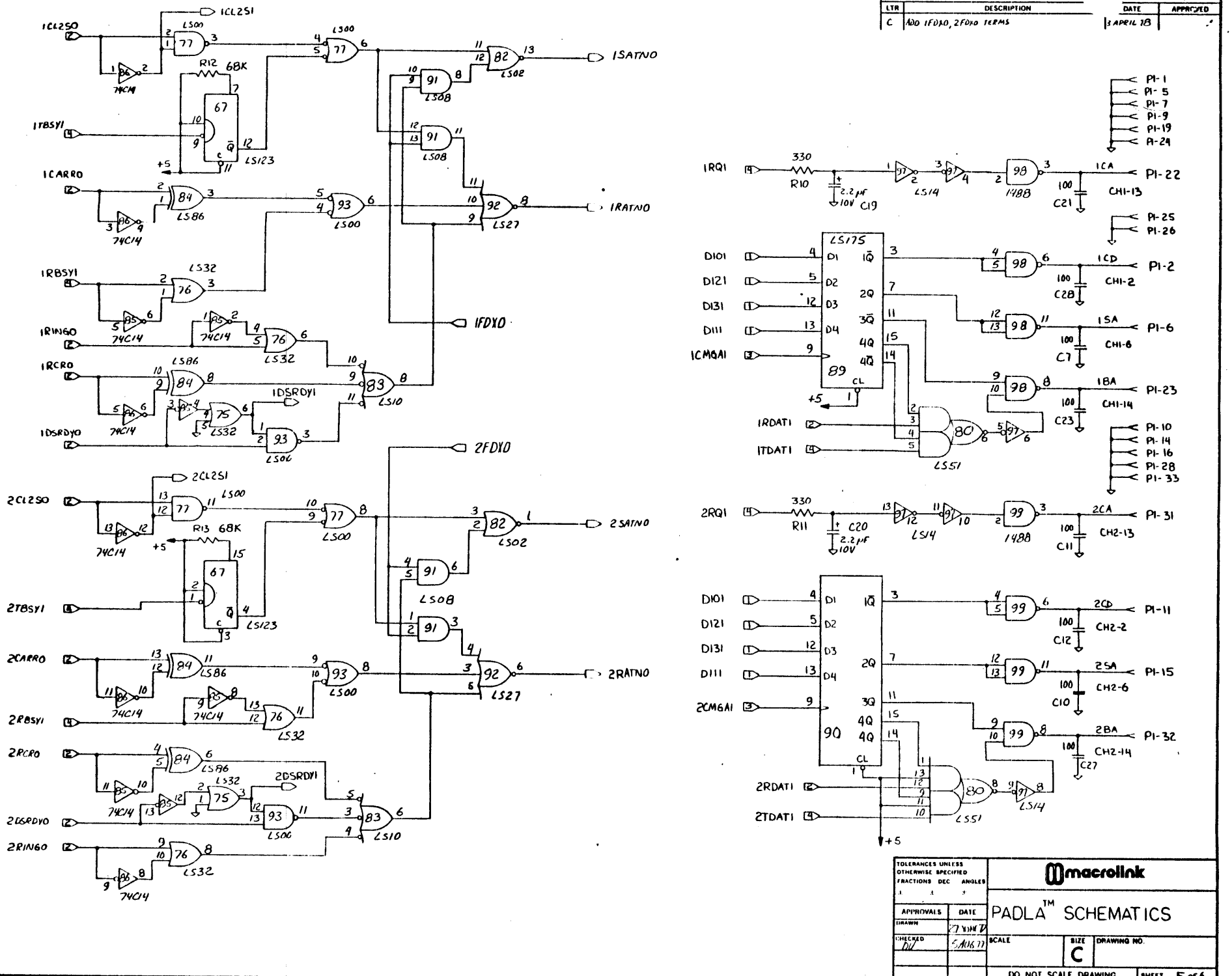
C	R7,8 NOW 330Ω, P.S. MOD	3 APRIL 78	



TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		macrolink	
APPROVALS	DATE	PADLA™ SCHEMATICS	
DRAWN	27 JULY 77		
CHECKED DV	5 AUG	SCALE	SIZE C — DRAWING NO.
		DO NOT SCALE DRAWING	SHEET 4 OF 6



TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES

APPROVALS	DATE
DRAWN	27 MAR 77
CHECKED DW	5 AUG 77

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SCALE | SIZE C | DRAWING NO.

DO NOT SCALE DRAWING | SHEET 5 OF 6

REVISIONS			
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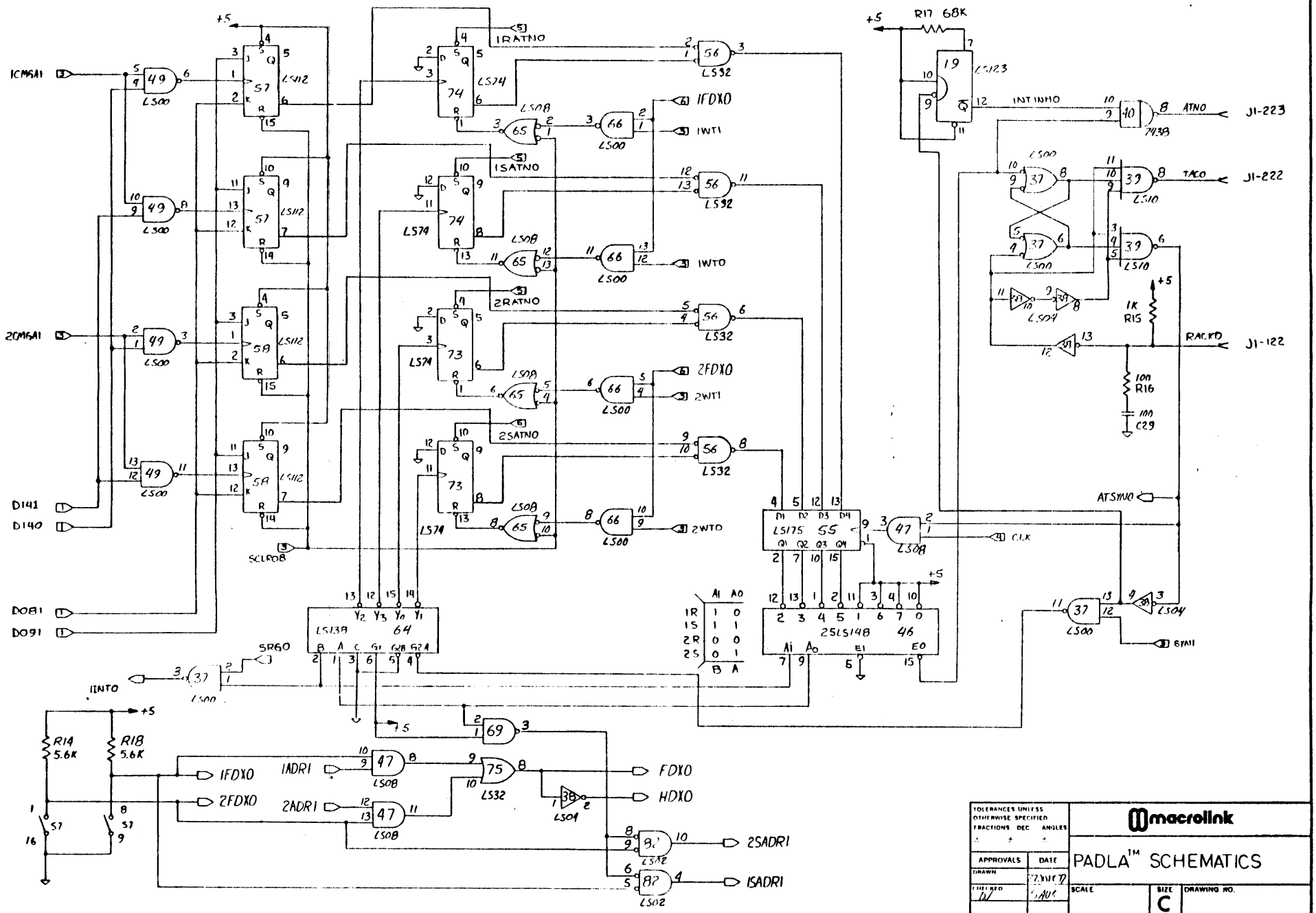

TOLERANCES UNLESS OTHERWISE SPECIFIED	
FRACTIONS DEC ANGLES	
± ± ±	
APPROVALS	DATE
DRAWN	
CHECKED	

macrolink

PADLA™ SCHEMATICS

SCALE | SIZE C | DRAWING NO.

DO NOT SCALE DRAWING | SHEET 6 OF 6