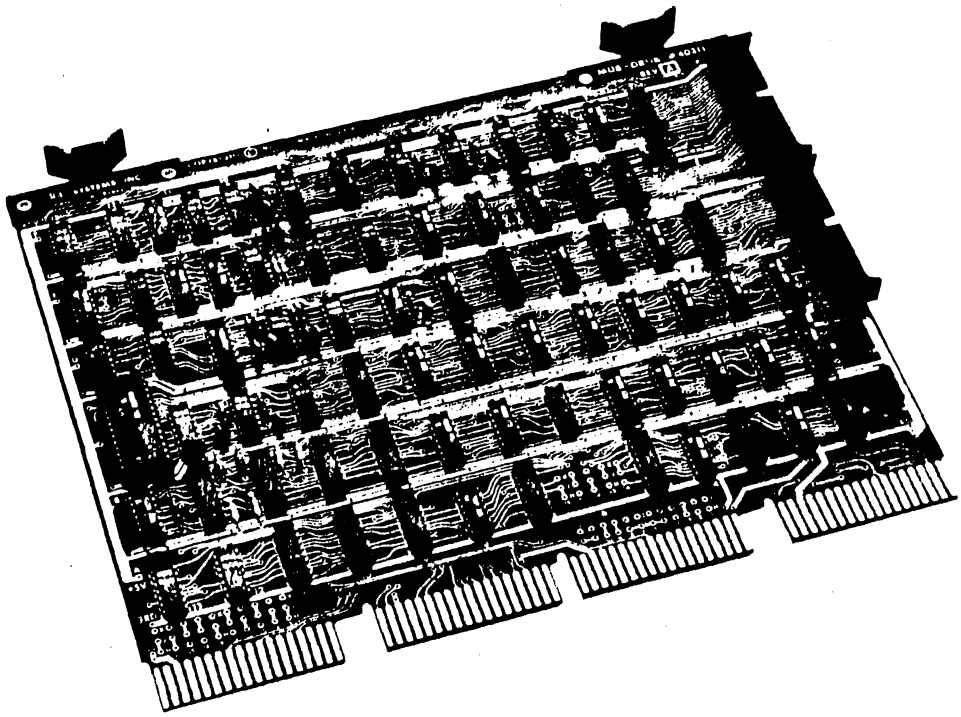
MDB

DR11B DIRECT MEMORY ACCESS MODULE for use with PDP*-11 Computers



MDB Direct Memory Access Module for PDP*-11 Computers

- Bi-directional exchange of 16-bit data from PDP-11 and external device
- Interrupt request and bus master control
- Control and status register
- Address selection
- Output buffer register and input buffer gates
- TTL input and output signals
- Compatible with DEC DR11B operating and diagnostic software
- Electrically plug-compatible with the DEC DR11B

The MDB DR11B direct memory access module controls data transfer between the DEC PDP-11 Unibus* and user peripheral devices.

The DR11B module contains all necessary hardware for control and status register assignments. The DR11B module is connected by two 40-pin Berg connectors to a peripheral unit. The DR11B module with appropriate software will control the 16-bit data exchange between the Unibus and various peripheral equipment on a direct memory access basis.

Interrupt request, bus master control logic, address selection, and device interface logic comprise the main functional sections of the MDB DR11B.

Four registers consisting of an input and output buffer (16-bit read/write), control/status (16-bit read/write), word count (16-bit read/write), and bus address (18-bit read/write) form the interface logic circuits of the DR11B module. Additional logic allows user selectable addressing across 32K boundaries without an ERROR condition. (Overflow to zero will cause ERROR).

Convenient data exchange between two PDP-11 computers can be achieved by cabling two DR11B modules together using an MDB-M91WW dual wire-

MDB SYSTEMS INC.
1995 N. Batavia Street
Orange, California 92665
714-998-6900
TWX:910-593-1339

Printed in USA
P/DRB/10M/8-79

*TM Digital Equipment Corp.

wrap module to perform similar to the DEC DA11B. Using this method a continuous and dependable exchange of data is accomplished and each module maintains transparency to its host computer.

ELECTRICAL REQUIREMENTS:

- +5V at 2.4A

ACCESSORIES:

- Optional general purpose cables available
- Dual wire-wrap module MDB-M91WW for custom applications and inter-processor communications.

PHYSICAL:

- Occupies 1 quad slot of standard system unit

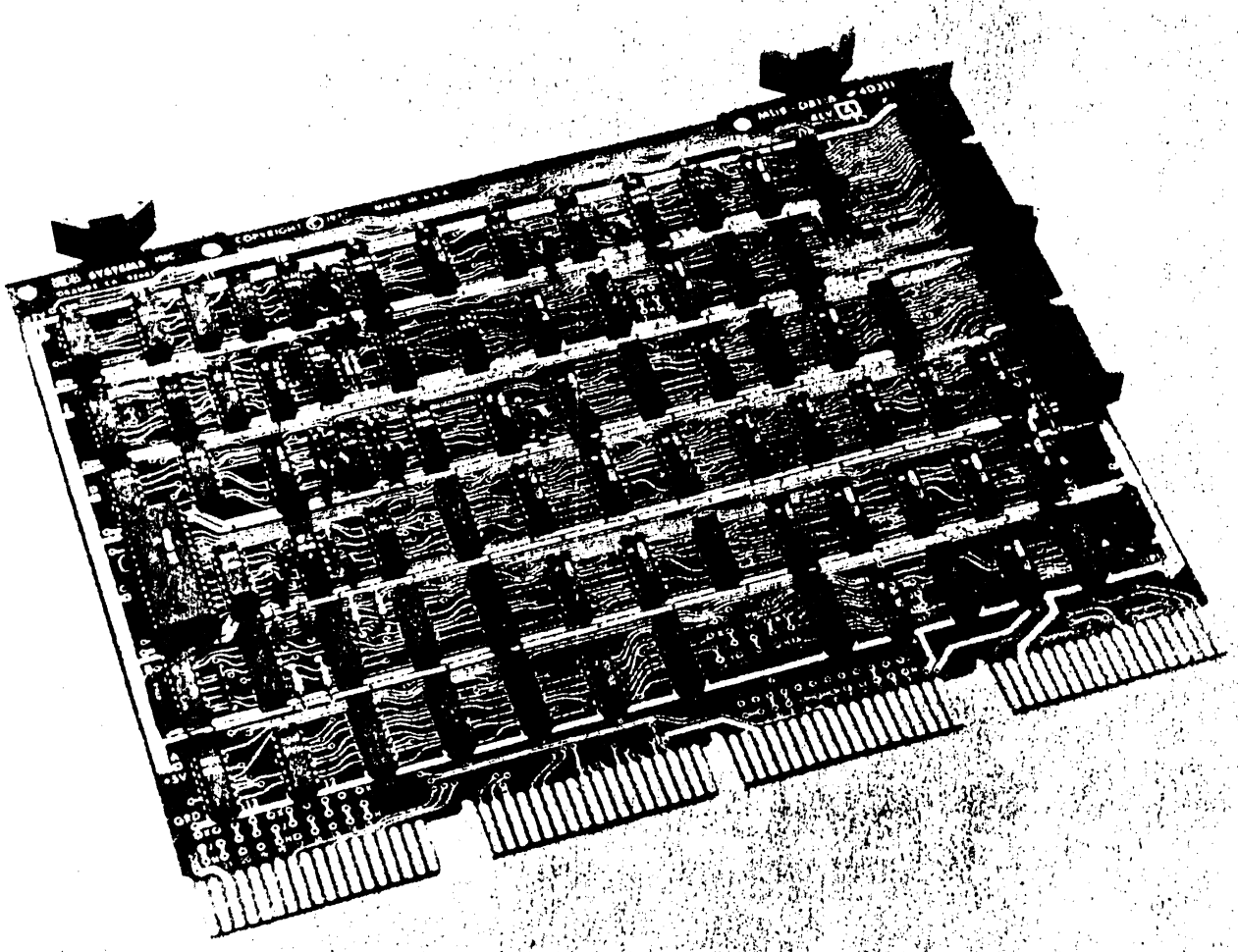
DR11B Cable Connector Pin Assignments

Connector P1		Connector P2	
Pin	Signal	Pin	Signal
1	DATI15	1	ODAT15
2	DATI00	2	ODAT00
3	DATI14	3	ODAT14
4	DATI01	4	ODAT01
5	DATI13	5	ODAT13
6	DATI02	6	ODAT02
7	DATI12	7	ODAT12
8	DATI03	8	ODAT03
9	DATI11	9	ODAT11
10	DATI04	10	ODAT04
11	DATI10	11	ODAT10
12	DATI05	12	ODAT05
13	DATI09	13	ODAT09
14	DATI06	14	ODAT06
15	DATI10	15	ODAT10
16	DATI07	16	ODAT07
17	C0 CONTROL IN	17	GND
18	A00IN	18	GND
19	ATTN	19	INIT0
20	GND	20	GND
21	BA INC ENB	21	WC INC ENB
22	GND	22	GND
23	no connection	23	READY0
24	GND	24	GND
25	BUSY0	25	470 OHMS TO +5V DC
26	GND	26	GND
27	C1 CONTROL IN	27	FNCT10
28	GND	28	NO LOCK
29	DSTATC	29	FNCT10
30	GND	30	GND
31	DSTATB	31	FNCT20
32	GND	32	GND
33	SINGLE CYCLE	33	FNCT30
34	GND	34	GND
35	DSTATA	35	FNCT30
36	GND	36	GND
37	GO0	37	CYCLE REQ B
38	GND	38	GND
39	CYCLE REQ A	39	END CYCLE 0
40	GND	40	GND

MDB DR11B

DIRECT MEMORY ACCESS MODULE

INSTRUCTION MANUAL



PRICE 10 00

TABLE OF CONTENTS

	Page
INTRODUCTION	1
PHYSICAL DESCRIPTION	2
INSTALLATION	
Installing Module	2
Cabling	2
Jumper Connections	6
Device Address	6
Vector Address	6
Bus Master Control Level	7
Bus Address Overflow Control	7
Non-Processor Request Control	7
REGISTERS	
Data Register	7
Word Count Register	8
Bus Address Register	8
Command, Status Register	8
UNIBUS INTERFACE	11
USER DEVICE INTERFACE	14
LOGIC ORGANIZATION	
Slave Mode Operation	16
Bus Master Mode Operation	18
Interrupt Operation	18
Data Transfer Operation	18
MAINTENANCE	
Maintenance Mode Operation	18
Troubleshooting and Repair	19
DRAWINGS	19

MDB SYSTEMS INC.
1995 N. Batavia Street
Orange, California 92665
714-998-6900
TWX:910-593-1339

MDB-DR11B
DIRECT MEMORY ACCESS MODULE

INTRODUCTION

The MDB-DR11B Direct Memory Access Module is an interface for the direct-memory-access transfer of data between a Digital Equipment Corporation (DEC) PDP-11 computer memory, and the user's peripheral device (figure 1).

The MDB-DR11B consists of a single quad module. The module fits into only one SPC slot of a DD11-A, B, or C assembly, unlike the DEC DR11B which occupies four slots. The MDB module works with all standard DEC software for the DR11B and performs all DEC DR11B functions.

Logic on the module includes the following facilities:

a. bus drivers and receivers;

b. four registers, as follows:
   Data Register
   Word Count Register
   Address Register
   Command Status Register;

c. a multiplexer to select the bus address, word count, input data, or command status information onto the Unibus;

d. logic to decode the received device address; and

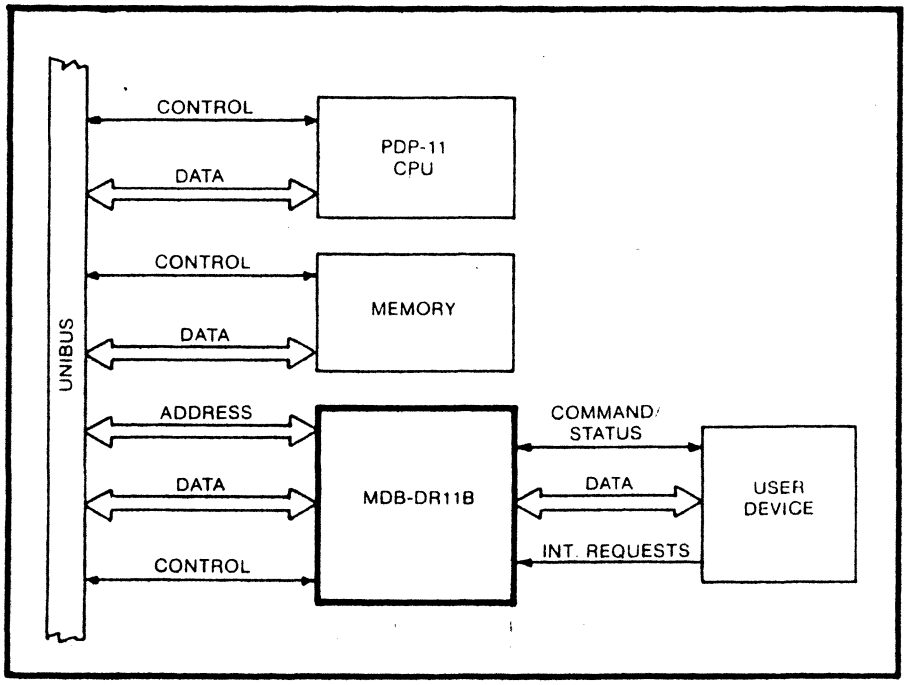


Figure 1. System Block Diagram

c. interrupt and bus master control logic.

Operation is always begun under program control which does the following:

a. loads the required word count into the Word Count Register;

b. specifies the starting memory address or bus address at which the block transfer is to begin; and

c. loads function bits into the Command/Status Register.

The user device responds to the function bits by setting-up controls to the DR11B. If the user device is to receive data, the DR11B performs a DATI operation, loading its data register with information at the specified bus address. Outputs of the Data Register are presented to the user device.

If the user device is to send data to the memory, the DR11B performs a DATO operation, transferring data words from the user device to the specified bus address. Note that input data is not buffered and must be retained for the entire Unibus transfer.

Data and control signals at the MDB-DR11B user interface are at standard TTL levels.

PHYSICIAL DESCRIPTION

The MDB-DR11B module is a quad module fitting into one slot in the systems assembly. The interface to the Unibus is through the assembly backplane. The module is connected to the user device through two 40-pin Berg connectors, J1 and J2. User logic may be built on an MDB-M957 wire-wrap board, connected to the MDB-DR11B through short ribbon jumpers.

The MDB-DR11B is powered by the +5V dc supply at the systems assembly, and requires 2.4 amperes from that supply.

INSTALLATION

The following paragraphs contain instructions and information for installing the MDB-DR11B module, and for installing or removing jumpers that configure the module for its application.

INSTALLING MODULE

Plug the module into any available small peripheral slot in the PDP-11 processor, or into one of the four slots in a DD11 Peripheral Mounting Panel (figure 2). Figure 2 shows the backplane wiring that may be required to maintain the non-processor grant (NPG) chain. Note that in some newer processors and DD11 system units a wire jumper is installed between CA1 and CB1. In these cases, it is only necessary to remove that wire jumper in the slot in which the MDB-DR11B is to be installed.

CABLING

The module has two Berg connectors for the user device interface. Cables from the device may be brought directly to these connectors, or to an MDB-M91WW wirewrap board

(figure 3) used in custom applications. Table 1 lists pin connections for J1 and J2 on the module.

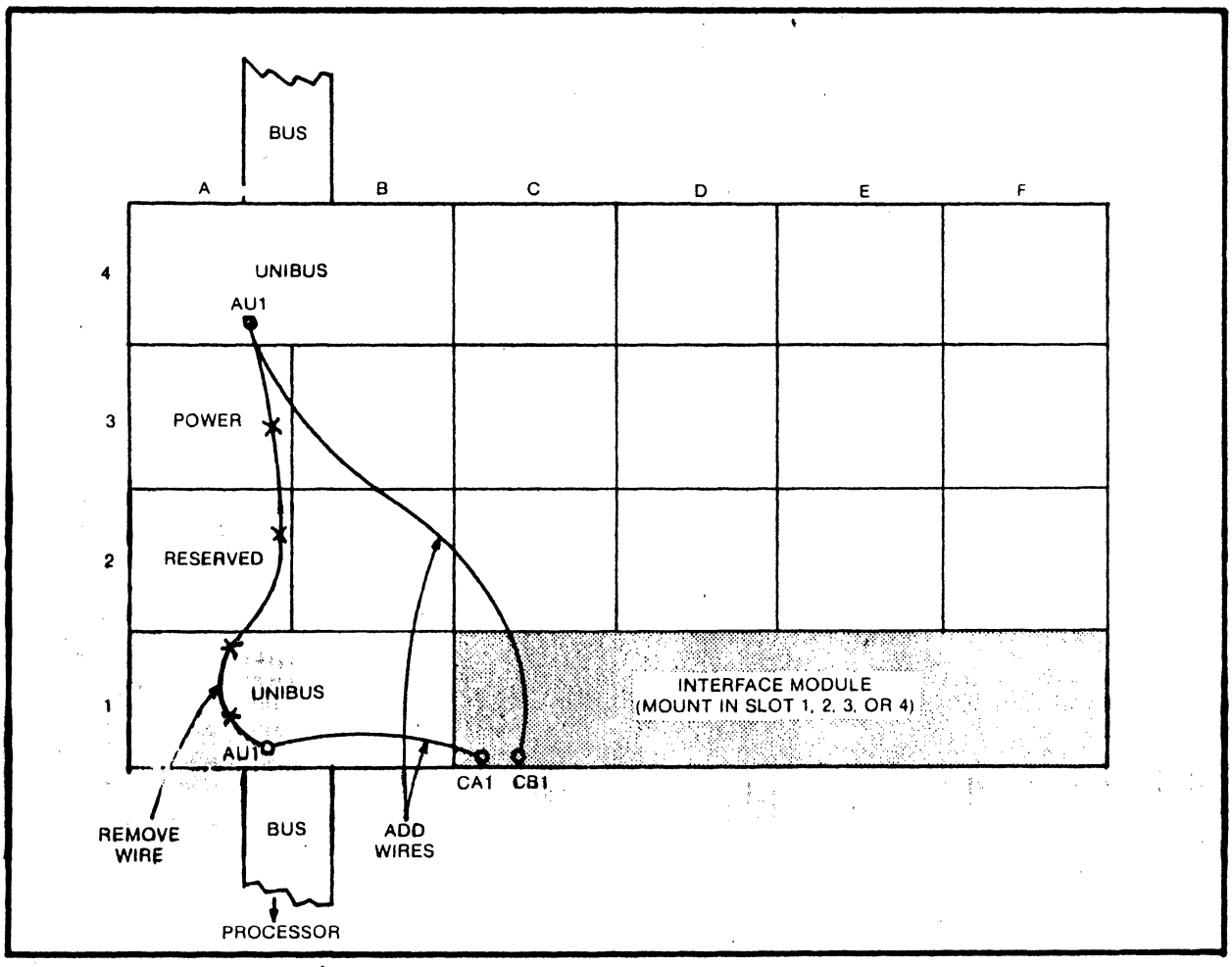


Figure 2. Typical Interface Location and Jumper Modification for NPR Chain

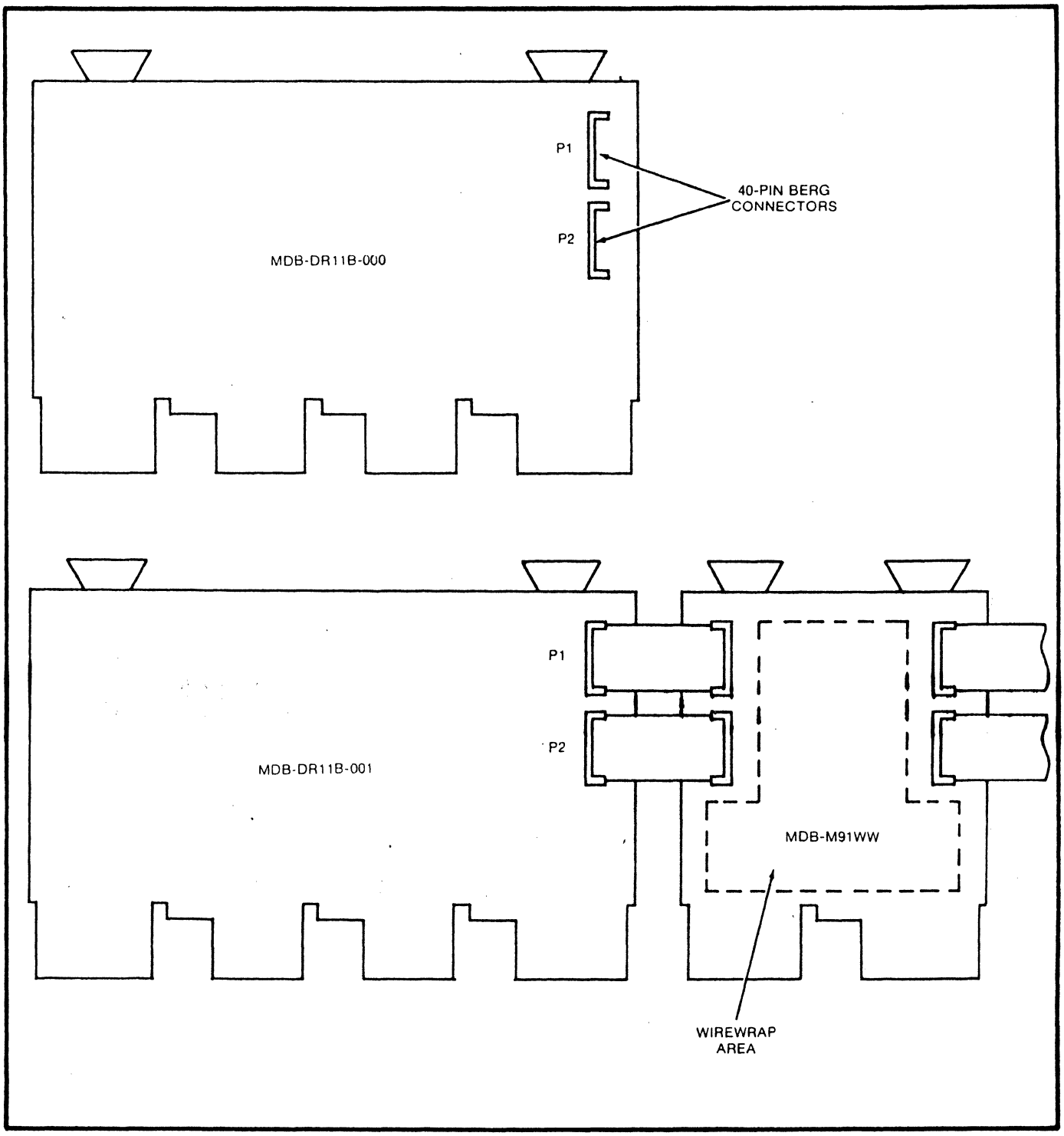


Figure 3. Using MDB-M91WW Wirewrap Board

Table 1. Interface Cable Connectors, Pin Assignments

Connector P1		Connector P2	
Pin	Signal	Pin	Signal
1	DATI15	1	ODAT15
2	DATI00	2	ODAT00
3	DATI14	3	ODAT14
4	DATI01	4	ODAT01
5	DATI13	5	ODAT13
6	DATI02	6	ODAT02
7	DATI12	7	ODAT12
8	DATI03	8	ODAT03
9	DATI11	9	ODAT11
10	DATI04	10	ODAT04
11	DATI10	11	ODAT10
12	DATI05	12	ODAT05
13	DATI09	13	ODAT09
14	DATI06	14	ODAT06
15	DATI10	15	ODAT10
16	DATI07	16	ODAT07
17	CO CONTROL IN	17	GND
18	A00IN	18	GND
19	ATTN	19	INIT0
20	GND	20	GND
21	BA INC ENB	21	WC INC ENB
22	GND	22	GND
23	no connection	23	READY0
24	GND	24	GND
25	BUSY0	25	470 OHMS TO +5V DC
26	GND	26	GND
27	C1 CONTROL IN	27	FNCT10
28	GND	28	NO LOCK
29	DSTATC	29	FNCT10
30	GND	30	GND
31	DSTATB	31	FNCT20
32	GND	32	GND
33	SINGLE CYCLE	33	FNCT30
34	GND	34	GND
35	DSTATA	35	FNCT30
36	GND	36	GND
37	GO0	37	CYCLE REQ B
38	GND	38	GND
39	CYCLE REQ A	39	END CYCLE 0
40	GND	40	GND

MDR-DR11B MANUAL CHANGE 1-80
CHANGE: PIN 15 DATI10 PIN 15 ODAT10
TO: PIN 15 DATI08 PIN 15 ODAT08
PG. 5

JUMPER CONNECTIONS

Certain jumper connections may be prepared on the module in order to configure the module for its application. The module is furnished with certain preferred configurations strapped by printed circuit etch. To change configurations, cut etch and/or install wire jumpers as required.

Device Address

Ten bits of the device address are strapped at jumpers numbered 13 through 22 (zone 13A on the module). The module is furnished strapped for address 772410.

A connection from pad J to pad K selects a logic "1", and a connection from pad J to pad H selects a logic "0". Jumpers are related to address bits as follows:

Bit	Jumper
A03	15
A04	14
A05	22
A06	13
A07	16
A08	19
A09	21
A10	20
A11	18
A12	17

Address assignments determined by standard DEC software are as follows:

No. of DR11B Module	Register Address
First	772410 - 772416
Second	772430 - 772436
Third	772450 - 772456
Fourth	772470 - 772476

Vector Address

The 6-bit vector address is strapped at jumper locations 23 through 28 (zones 6A and 5A). The module is furnished strapped for vector address 124. Where more than one module is used, the user must assign a different address to each module, with 124 assigned to the first module.

A connection from pad J to pad H selects a logic "1", and a connection from pad J to pad K selects a logic "0". Jumpers are related to data bus bits as follows:

Bit	Jumper
DATA02	28
DATA03	27
DATA04	26
DATA05	24
DATA06	23
DATA07	25

Bus Master Control Level

The module is furnished with etched connections to select level 5. That is, BR5I, BG5INH, and BG5OUTH are connected to driver receiver circuits. Inputs for BG4INH, BG6INH, and BG7INH are etch-jumpered to corresponding BG4OUTH, BG6OUTH, and BG7OUTH lines.

To select a level other than level 5, cut the etch for level 5, and connect wire jumpers for the selected level, as follows (be sure to remove any etched or wire jumpers not listed for the selected level):

Level 4	Level 5	Level 6	Level 7
4/H-J	3/H-J	2/H-J	1/H-J
11/H-J	9/H-J	7/H-J	5/H-J
12/H-J	10/H-J	8/H-J	6/H-J
9/H-10/H	11/H-12/H	11/H-12/H	11/H-12/H
7/H-8/H	7/H-8/H	9/H-10/H	9/H-10/H
5/H-6/H	5/H-6/H	5/H-6/H	7/H-8/H

Bus Address Overflow Control

The module is furnished with etched jumpers that cause the logic to set READY and ERROR if the bus address overflows the 32K boundary set by some DEC software. These jumpers are 29/H-J and 30/H-J.

If your application permits disregarding the 32K boundary, jumpers may be reconfigured so that each 32K overflow simply increments the Extended Bus Address count, and sets READY and ERROR only when the address has overflowed the limit of system addressing. To select this mode of operation, cut etch jumpers 29/H-J and 30/H-J, and connect wire jumpers at 29/H-K and 30/H-K.

Non-Processor Request Control

The module is furnished to permit an interrupt cycle to be performed without interruption by an NPR request from some other device. That is, there is an etch connection at 31/H-J.

If an NPR request is to be permitted to take control during an interrupt latency period (between the interrupt request and the bus grant), cut the etch at 31/H-J and connect a wire jumper at 31/H-K.

REGISTERS

There are four registers available to the Unibus. Each register is described in the following paragraphs.

DATA REGISTER

The 16-bit Data Register is used both to read, and write, data as follows:

a. **Write Data.** The register stores the output data word for presentation to the user device. The register is loaded under program control.

b. **Read Data.** A data word from the user device is transferred to the Unibus without buffering. That is, the user device must hold data on the lines until it is read under program control or transferred directly to memory.

The preferred Data Register address is 772416.

WORD COUNT REGISTER

The Word Count Register is a 16-bit read/write register. It is loaded from the Unibus, under program control, with the 2's-complement of the number of words to be transferred, and normally is incremented one count towards zero as each word is transferred. Incrementing may be inhibited by a WC INC ENB signal from the user device.

When the word count reaches zero, the READY bit is set in the command/status word to stop the bus cycle.

The preferred Word Count Register address is 772410.

BUS ADDRESS REGISTER

The Bus Address Register is a 15-bit register, as bit 0 is furnished by the user device. The contents of the register are used, along with bits XBA16 and XBA17 (in the Command Status Register) to specify the bus address.

The Bus Address Register is normally incremented after each word to transferred, advancing the address to the next word location. The user device may inhibit incrementing by asserting BA INC ENB.

The ERROR bit is set in the Command/Status Register if the address overflows (changes from all-"1's to all-"0's"). The error (BAOF) is cleared either by INIT or by loading a new number into the Bus Address Register.

The preferred Bus Address Register address is 772412.

COMMAND/STATUS REGISTER

The contents of the Command Status Register are commands to control the user device, and bits giving user device status to the Unibus. Table 2 lists and defines bits in the Command Status Register.

The preferred Command Status Register address is 772414. Figure 3 shows the contents of the Command Status Register.

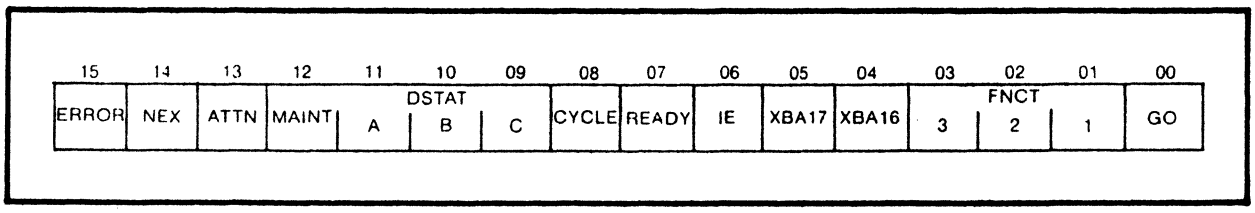


Figure 3. Contents of Command/Status Register

Table 2. Command/Status Bits

Bit	Name	Description and Effect
15	ERROR (read only)	a. Indicates error as follows: 1. NEX (bit 14), or 2. ATTN (bit 13), or 3. Interlock error (module connector discontinuity), or 4. Bus address overflow (BAOF) as bus address changes from all-"1's" to all-"0's". b. Sets READY (bit 7) and causes interrupt if IE (bit 6) has been set. c. ERROR is cleared by clearing all error conditions, as follows: 1. Module is seated in connector. 2. Bus address is cleared or reloaded. 3. Bit 14 is loaded with a "0". 4. Bit 13 is cleared by the user device.
14	NEX (read/write)	a. **Non-existent Memory.** Indicates that the module, acting as bus master, failed to receive a SSYN response within 20 microseconds after asserting MSYN. b. NEX sets ERROR bit. c. Cleared by INIT or by loading "0".
13	ATTN (read only)	a. **Attention.** Shows state of user device ATTN signal. b. Sets ERROR for device-initiated interrupt. c. Set and cleared only by user device.
12	MAINT (read/write)	a. **Maintenance.** Used to enable execution of diagnostic programs. b. Cleared by INIT.

Table 2. Command/Status Bits (cont'd)

Bit	Name	Description and Effect
11 10 09	DSTATA DSTATB DSTATC (read only)	a. **Device Status.** Indicate state of user-designated DSTATA, DSTATB, and DSTATC signals. b. Set and cleared only by user device.
08	CYCLE (read write)	a. If set when GO is issued, enables an immediate bus cycle. b. Cleared by INITI, or start of bus cycle.
07	READY (read only)	a. Indicates the MDB-DR11B is able to accept a new command. b. Set by INIT or ERROR, or by word count overflow. c. Cleared by GO. d. If bit 6 is set, READY causes an interrupt, forcing module to release the Unibus.
06	IE (read write)	a. **Interrupt Enable.** Enables either ERROR or READY to set an interrupt. b. Cleared by INIT.
05 04	XBA17 XBA16 (read write)	a. **Extended Bus Address.** Along with contents of Bus Address Register, specify address for **indirect** memory transfers. b. Cleared by INIT. c. Bits XBA17 and XBA16 are **not** incremented when Bus Address Register overflows, but ERROR is set.
03 02 01	FNCT3 FNCT2 FNCT1 (read write)	a. **Function.** Bits available to user device for assignment by user. b. Cleared by INIT.
00	GO (write only)	a. Causes MDB-DR11B to signal user device that a command has been issued. b. Clears READY.

UNIBUS INTERFACE

Table 3 lists and defines signals at the Unibus MDB-DR11B interface. Refer to appropriate DEC PDP-11 documents for detailed timing information and software considerations.

Table 3. Backplane Interface Terms

Pin	Signal	Description
	D00L-015L	Unibus bidirectional data lines. Low (ground) level is true, +3V is false.
CS2	D00L	Data bit 0 (LSB)
CR2	D01L	Data bit 1
CU2	D02L	Data bit 2
CT2	D03L	Data bit 3
CN2	D04L	Data bit 4
CP2	D05L	Data bit 5
CV2	D06L	Data bit 6
CM2	D07L	Data bit 7
CL2	D08L	Data bit 8
CK2	D09L	Data bit 9
CJ2	D10L	Data bit 10
CH1	D11L	Data bit 11
CH2	D12L	Data bit 12
CF2	D13L	Data bit 13
CE2	D14L	Data bit 14
CD2	D15L	Data bit 15
	A00L-A17L	Device and function address from master device. Low level is true. Bits A01L, A02L, and A03L, and control line C1L encode one of 16 addresses. Bits A04L through A17L are used to enable the decoder.
EH2	A00L	Address bit 0 (LSB)
EH1	A01L	Address bit 1
EF1	A02L	Address bit 2
EV2	A03L	Address bit 3
EU2	A04L	Address bit 4
EV1	A05L	Address bit 5
EU1	A06L	Address bit 6
EP2	A07L	Address bit 7
EN2	A08L	Address bit 8
ER1	A09L	Address bit 9
EP1	A10L	Address bit 10
EL1	A11L	Address bit 11
EC1	A12L	Address bit 12
EK2	A13L	Address bit 13
EK1	A14L	Address bit 14
ED2	A15L	Address bit 15
EE2	A16L	Address bit 16
ED1	A17L	Address bit 17

Table 3. Backplane Interface Terms (cont'd)

Pin	Signal	Description
DL1	INITL	Low-level true or negative-going transition received from master device when a programmed RESET instruction is issued, the console START switch is pressed, or a power-up or power-down condition occurs.
EF2	C1L	Control line, low level true. With C0L, specifies the type of cycle to be performed.
EJ2	C0L	Control line, low level true. With C1L, specifies type of cycle to be performed, as follows: **C1L** **C0L** **Cycle** 0 0 DATI 0 1 DATIP 1 0 DATO 1 1 DATOB
EE1	MSYNL	Timing pulse from master device. Negative transition initiates internal timing sequence enabled by address decoding.
EJ1	SSYNL	Negative-going pulse (approx. 200 nsec) sent by module to master device. Follows (by approx. 100 nsec) the negative-going transition of MSYNL when device address has been decoded.
FD1	BBSYL	Busy signal (low level true) sent to master device by interrupt logic on the module. Level falls on receipt of bus grant input, and rises as vector address is transferred onto Unibus.
FT2	SACKL	Control level (low level true) sent to master device by interrupt logic to acknowledge receipt of bus grant input. Reset when vector address has been transferred onto Unibus.
FJ1	NPRL	Bus-master request (low level true) sent by user device to master device.
FM1	INTRL	Control level (low level true) sent to master device by interrupt logic as vector address is transferred onto Unibus.
DH2	BR4L	One of four possible bus request levels sent to master device in response to request by user device. Level is selected by means of wire jumper. Negative level is true.
DF2	BR5L	Bus request level 5 (see BR4L).

Table 3. Backplane Interface Terms (cont'd)

Pin	Signal	Description
DE2	BR6L	Bus request level 6 (see BR4L).
DD2	BR7L	Bus request level 7 (see BR4L).
DS2	BG4INH	One of four possible bus grant input levels sent by master device in response to bus request. Level is selected by means of wire jumper. High level is true.
DP2	BG5INH	Bus grant level 5 (see BG4INH).
DM2	BG6INH	Bus grant level 6 (see BG4INH).
DK2	BG7INH	Bus grant level 7 (see BG4INH).
DT2	BG4OUTH	One of four possible bus grant output levels selected by wire jumper and sent to another controller to extend a serial interrupt priority link. High level is true.
DR2	BG5OUTH	Bus grant output level 5 (see BG4OUTH).
DN2	BG6OUTH	Bus grant output level 6 (see BG4OUTH).
DL2	BG7OUTH	Bus grant output level 7 (see BG4OUTH).
CA1	NPRGINH	Bus-master bus grant signal sent by master device to user device in response to NPRL. High level is true.
CB1	NPRGOUTH	Bus-master bus grant output level to another controller to extend serial priority bus-master control. High level is true.

USER DEVICE INTERFACE

Signals at the user device interface are at standard TTL levels. Output drivers are 74367 bus drivers with "enable" inputs strapped to ground. Table 4 lists and defines signals at the user device interface. Unless otherwise stated, logic is asserted at the high level.

Table 4. User Device Interface Terms

Signal	Description
Inputs to MDB-DR11B from User Device	
DAT100-DAT115	Sixteen data lines. Data must be held until transferred to memory in a DATO cycle.
C1 CONTROL IN C0 CONTROL IN	Two signals specify type of Unibus cycle to be performed, and have the same meanings (but opposite logic levels) as Unibus signals C1 and C0 (refer to table 1).
CYCLE REQ A, CYCLE REQ B	Either signal sets CYCLE bit to initiate bus request and subsequent Unibus cycle. Must be pulsed positive for at least 100 nanoseconds (negative-going transition is active).
WC INC ENB	**Word Count Increment Enable.** To permit counting each bus cycle, this line must be held high. For certain operations, however, such as a read-modify-write sequence, the line may be brought low for the DATIP cycle and raised for the following DATO cycle.
BA INC ENB	**Bus Address Increment Enable.** To permit the Bus Address Register to increment following each bus cycle, this line must be held high. For certain operations, however, such as a read-modify-write sequence, the line may be brought low for the DATIP cycle and raised for the following DATO cycle.
A00IN	**Bus Address Bit 00.** Used as bit 0 of the Bus Address Register. For sequential word addressing A00 is held low. The line may be controlled to permit byte addressing.
DSTATA, DSTATB, DSTATC	**Device Status Bits.** User-assigned status signals. Levels on these lines appear as bits 09, 10, and 11 in the Command Status Register.
ATTN	**Attention.** The signal level on this line becomes bit 13 in the Command Status Register. ATTN causes an error condition and prevents further bus cycles. If the IE bit is set, ATTN causes an interrupt. If not used, ATTN must be held low.

Table 4. User Device Interface Terms (cont'd)

Signal	Description
SINGLE CYCLE	When held high, SINGLE CYCLE causes MDB-DR11B to release bus after each cycle, permitting Unibus to interleave MDB-DR11B cycles with cycles of other devices. In this case, MDB-DR11B requests bus master for each cycle. For burst-mode or read-modify-write operations, SINGLE CYCLE is held low, causing MDB-DR11B to control the bus until SINGLE CYCLE goes high, or until READY is set. Bus cycle does not begin until CYCLE is set.
Outputs from MDB-DR11B to User Device.	
ODAT00-ODAT15	Data to user device. Data is buffered in Output Data Register, which is loaded under program control, or by an MDB-DR11 DATI cycle. INIT clears all lines to "0".
INITO	**Initialize.** Goes high when Unibus is initialized.
FNCT1, FNCT2, FNCT3	**Function.** Bits 01, 02, and 03 in Command Status Register, output through drivers. Defined by user to control device operation. Cleared by INIT.
READYO	Bit 07 in Command Status Register. Set high by INIT. Goes low as GO bit is loaded to indicate that a command has been received. Set high again by word count overflow or error.
BUSYO	High level while bus cycle is in progress. Set high as CYCLE is set, and goes low when cycle is complete. When CYCLE is controlled by program, BUSYO follows CYCLE.
END CYCLE O	Positive-going pulse (approx. 100 nsec) output as bus cycle is ended.
GOO	Positive-going pulse (approx. 200 nsec) output as GO is set in Command Status Register. Indicates start of new operation.

The sequence of operation at the MDB-DR11B user device interface is, generally, as follows:

a. The GO bit is set, and READY goes low, indicating that a cycle is to begin. FNCT bits may define the command.

b. The user device then provides the following signals: DATI00-DATI15, C1 CONTROL, C0 CONTROL, WC INC ENB, and A00IN. These signals must be held on the lines throughout the bus cycle.

c. At least 100 nsec after the data appears on the lines, the trailing edge of CYCLE REQ A or B sets BUSY.

d. At the end of the bus cycle, the MDB-DR11B sends END CYCLE, and BUSY goes low. A new cycle request wil not be serviced while BUSY is set.

The BA INC ENB signal need not be set until BUSY is set. However, BA INC ENB must be held until the end of END CYCLE.

The program may load the CYCLE bit into the Command/Status Register. This raises BUSY, so that a bus cycle is begun when GO is set. Consequently, the MDB-DR11B is set-up so that the first bus cycle may be begun without a CYCLE REQ (A or B) signal from the user device.

LOGIC ORGANIZATION.

Figure 5 shows the general organization of logic in the MDB-DR11B. Refer also to the schematic diagrams (Dwg. 40311) in this manual.

The four registers in the MDB-DR11B are controlled either under program control (slave mode), or with the MDB-DR11B acting as bus master, controlling the Unibus.

SLAVE MODE OPERATION

When operating as a slave under program control, information is loaded into one of four registers selected by address bits A01 and A02. Bits A13 through A17 are hardwired "1's", and bits A04 through A12 must match the code jumpered on the module in order for the MDB-DR11B to respond to the program.

After the address has settled, the Unibus asserts MSYN. The module acknowledges by returning SSYN.

The bus signals C0 and C1, and A00IN (from the user device) are decoded to define the type of operation to be performed. Note that only the Command/Status Register may be loaded by either the high-order or low-order byte, selectively. Other registers handle only a 16-bit word.

Output data is loaded, or input data is selected to the bus, by bits A01, A02, and A03, which select one of the following:

- Data Register ($A01 \cdot A02$)
- Word Count Register ($\overline{A01} \cdot \overline{A02} \cdot A03$)
- Bus Address Register ($A01 \cdot \overline{A02} \cdot A03$)
- Command Status Register ($\overline{A01} \cdot A02$).

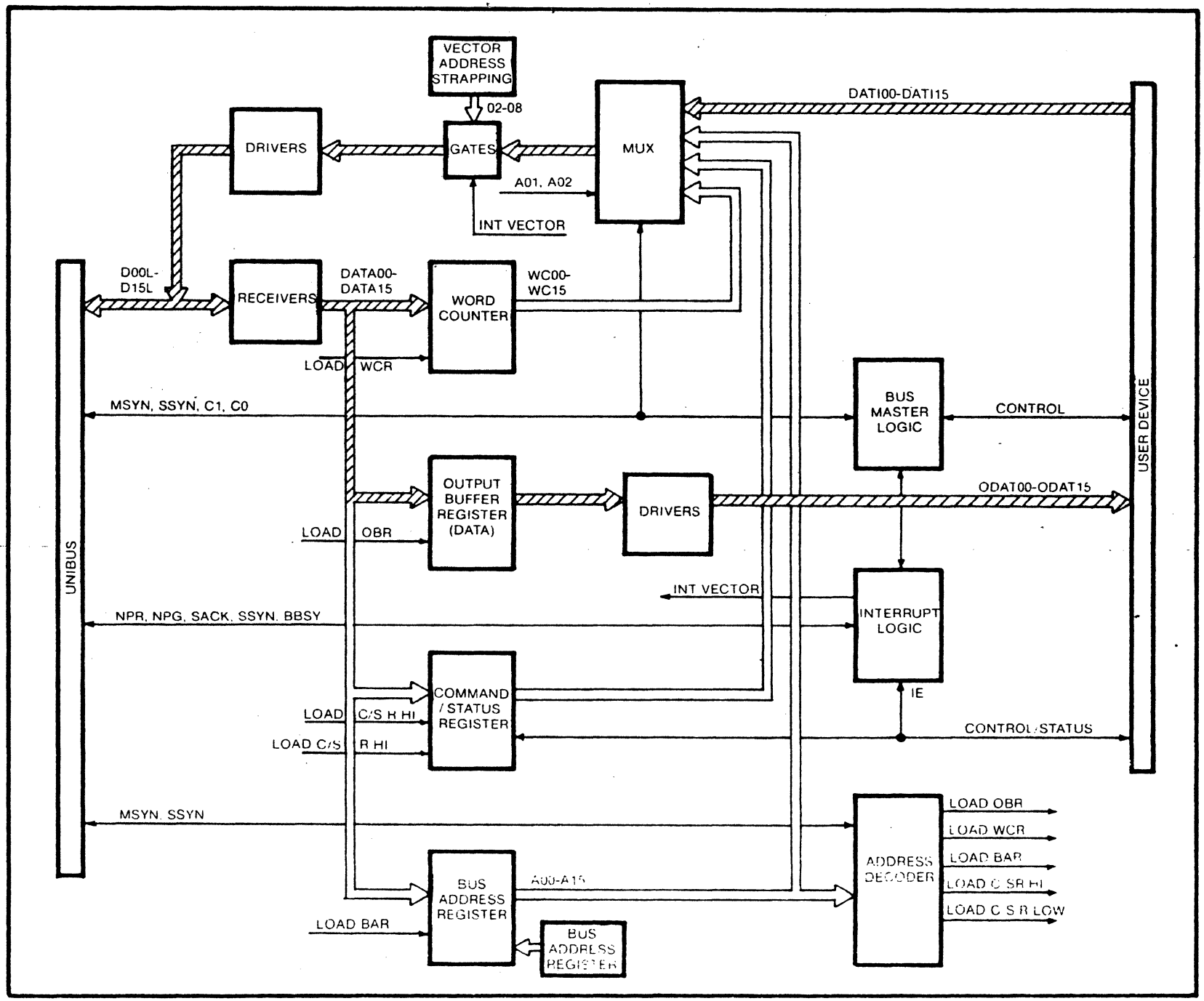


Figure 5. MDB-DR11B, Logic Organization

BUS MASTER MODE

In the Bus Master mode of operation, the user device causes the MDB-DR11B to take control of the bus and perform either an interrupt operation, or a data transfer operation.

Interrupt Operation
The MDB-DR11B can initiate an interrupt cycle if both bit 06 (Interrupt Enable) and bit 07 (READY) are set in the Command/Status Register. The resulting bus request (BRnL) requests control of the bus.

The master device then sends the bus grant signal (BGnINH) which the module acknowledges by returning SACKL. When the bus is free, the module puts the vector address on the bus, along with the signal INTRL. This directs the program to the subroutine that controls the user device.

Data Transfer Operation
The module will perform DATI, DATIP, DATO, and DATOB operations.

The program first loads Bus Address and Word Counter Registers, and then loads bit 0 (GO) into the Command/Status Register to clear READY. A CYCLE REQUEST (A or B) from the user device initiates transfer by setting CYCLE, and consequently, BUSY. A bus request is then sent to the master device which responds with the bus grant signal, permitting the module to become bus master.

The module makes its request on the NPR line and, when the NPR bus grant is received, becomes bus master, asserting BUS BBSY. The address is then put on the bus. C0 CONTROL and C1 CONTROL lines from the user device determine subsequent operation.

MAINTENANCE

MAINTENANCE MODE OPERATION

The MAINT bit (bit 12) in the Command Status Register enables the MDB-DR11B to operate with existing DEC software for DR11-B diagnostics. To configure the MDB-DR11B for diagnostic operation (with outputs looped to inputs), connect jumper cable (supplied) between connectors J1 and J2 (refer to table 1 for pin connections).

The MAINT bit causes the FNCT bits to act as an octal counter which counts bus cycles. Note that with FNCT1 connected to the C1 CONTROL line, the MDB-DR11B performs alternating DATI and DATO cycles. If J1 and J2 are jumpered together but the MAINT bit is not set, either all DATI cycles, or all DATO cycles, will be performed.

Because FNCT3 is looped to the SINGLE CYCLE line, the MAINT bit causes a burst mode sequence of four cycles, followed by four single cycles.

Refer to appropriate DEC documentation for details of diagnostics.

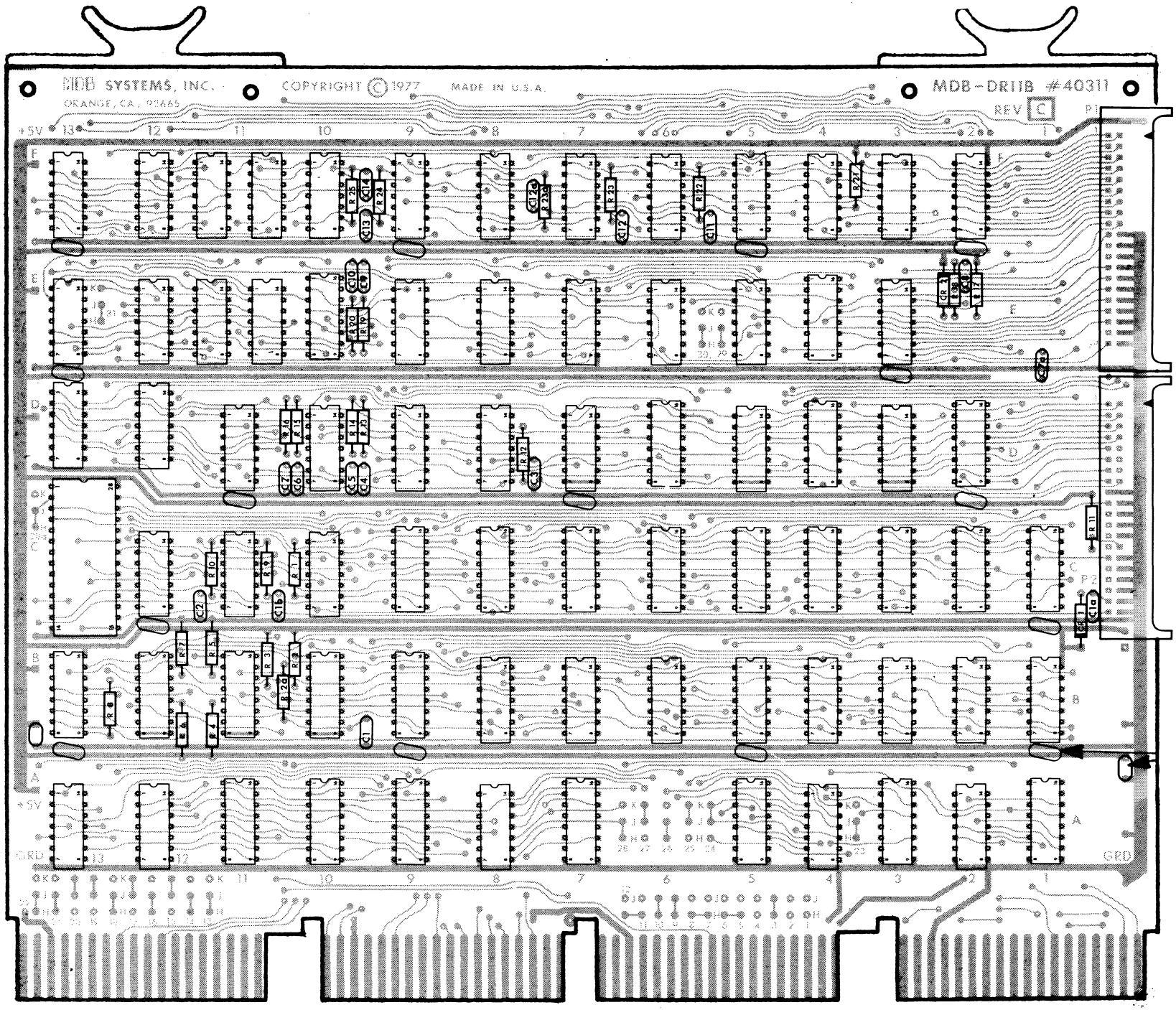
TROUBLESHOOTING AND REPAIR

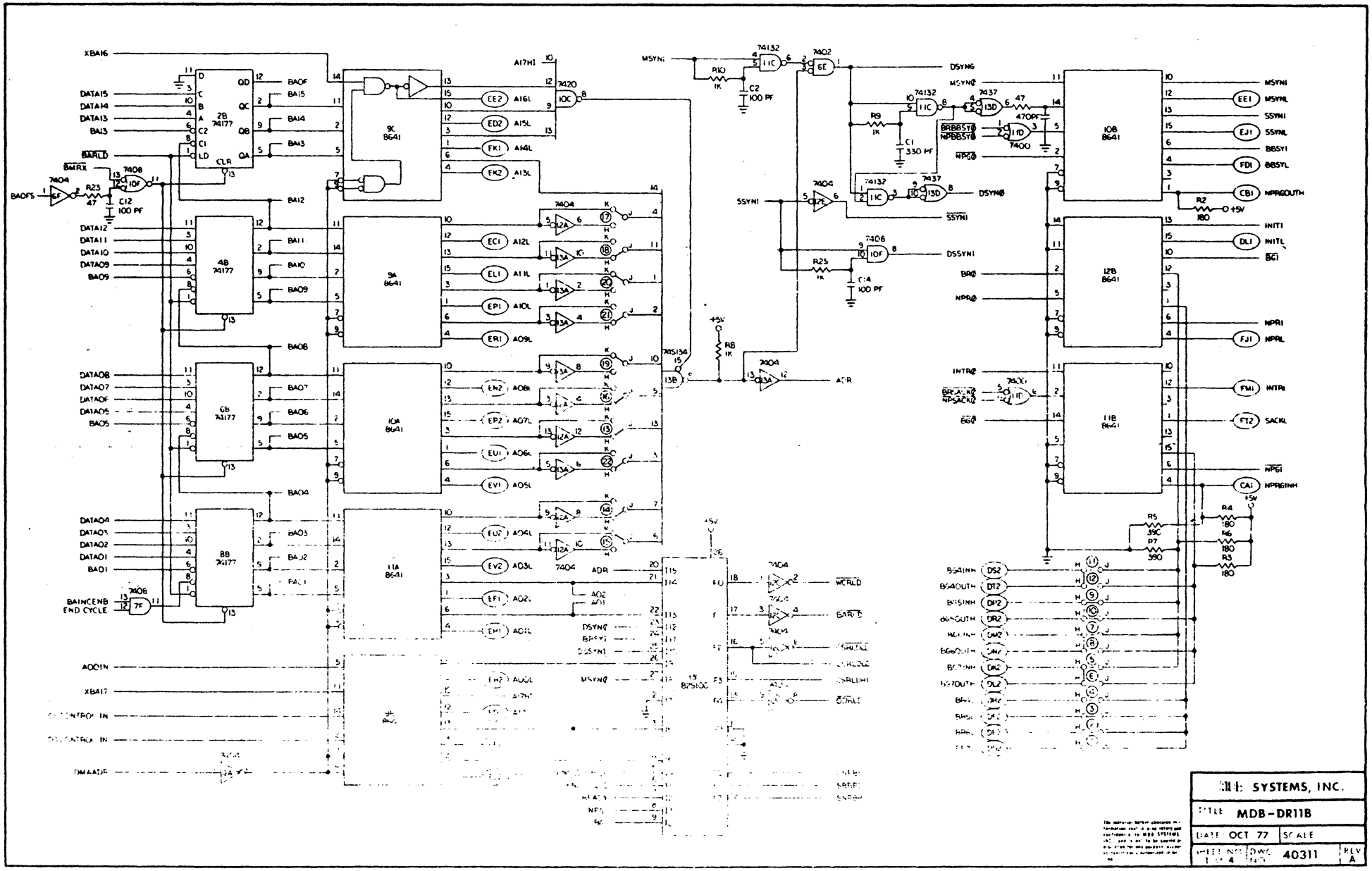
Troubleshooting will generally be based on existing DEC diagnostic software for the DR11-B.

Repair the module using appropriate skills, techniques, and materials. If you wish MDB Systems to repair the module, first notify MDB System's Customer Service, then pack the module carefully, along with your best evaluation of trouble symptoms, and ship it, prepaid, to MDB Systems.

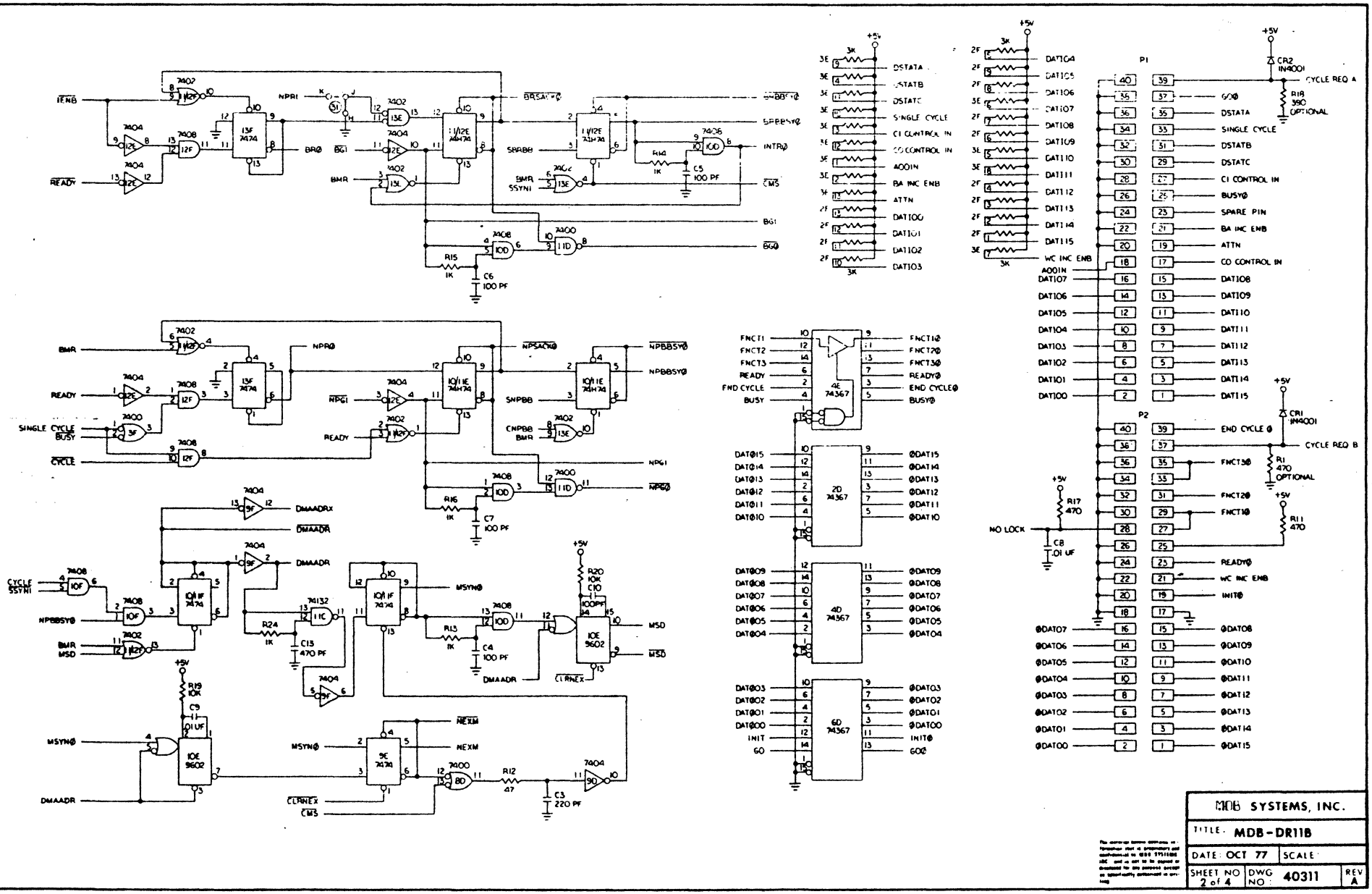
DRAWINGS

The following pages contain logic diagrams and assembly drawings useful in maintaining and repairing the module.

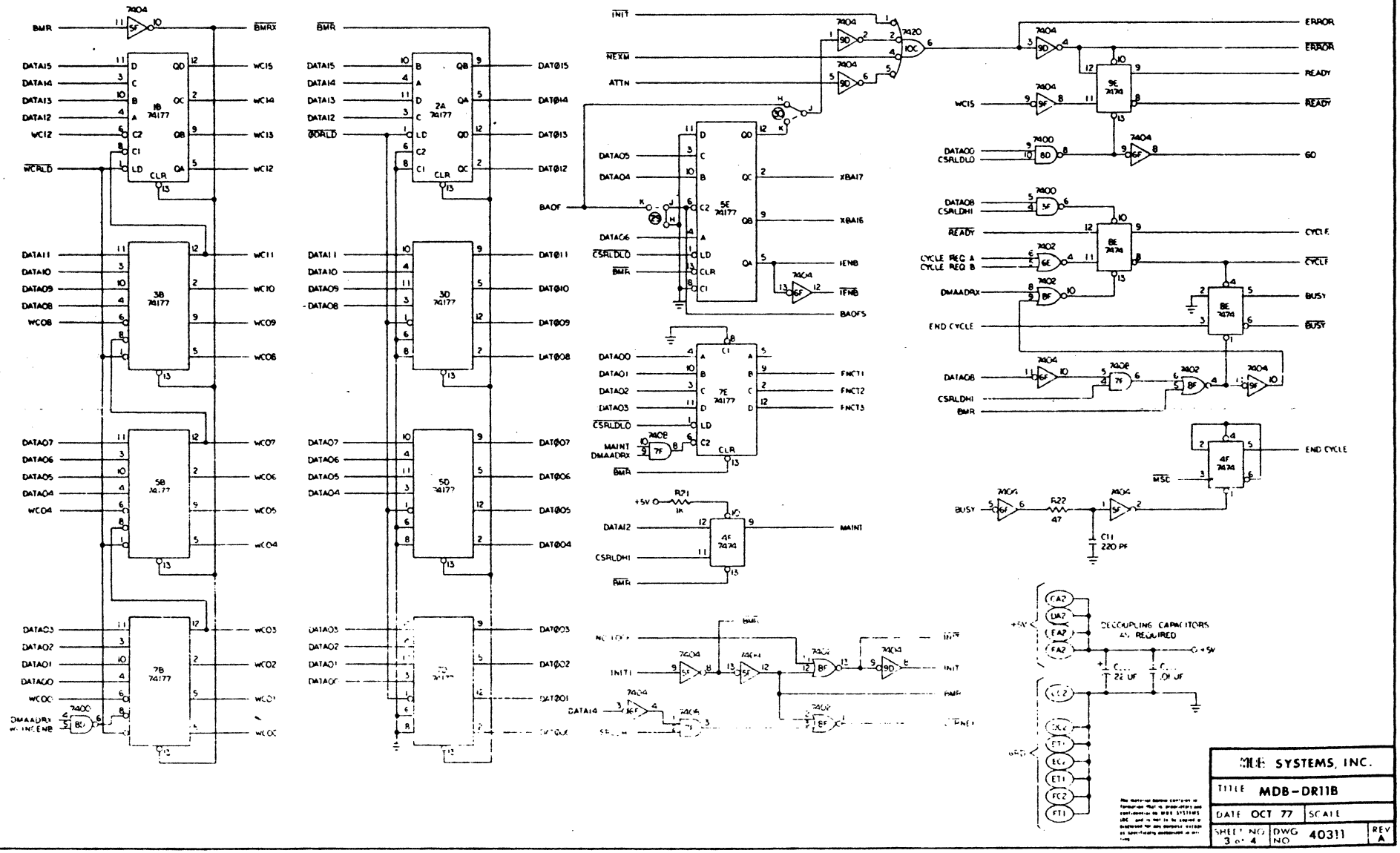

MDB SYSTEMS, INC.
ORANGE, CA. 92665
COPYRIGHT © 1977
MADE IN U.S.A.
MDB-DR11B #40311
REV C
+5V
GRD
P1
P2

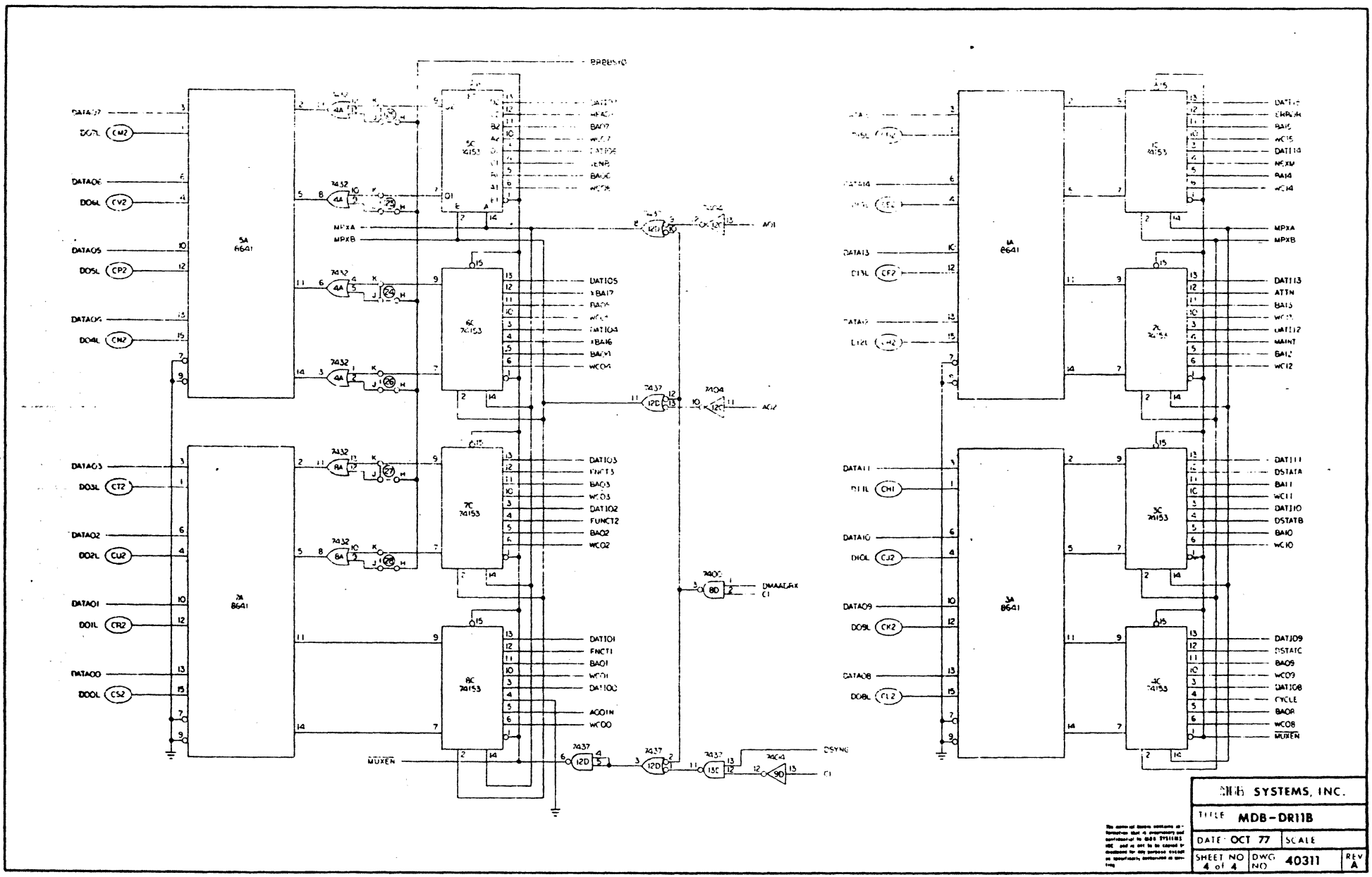


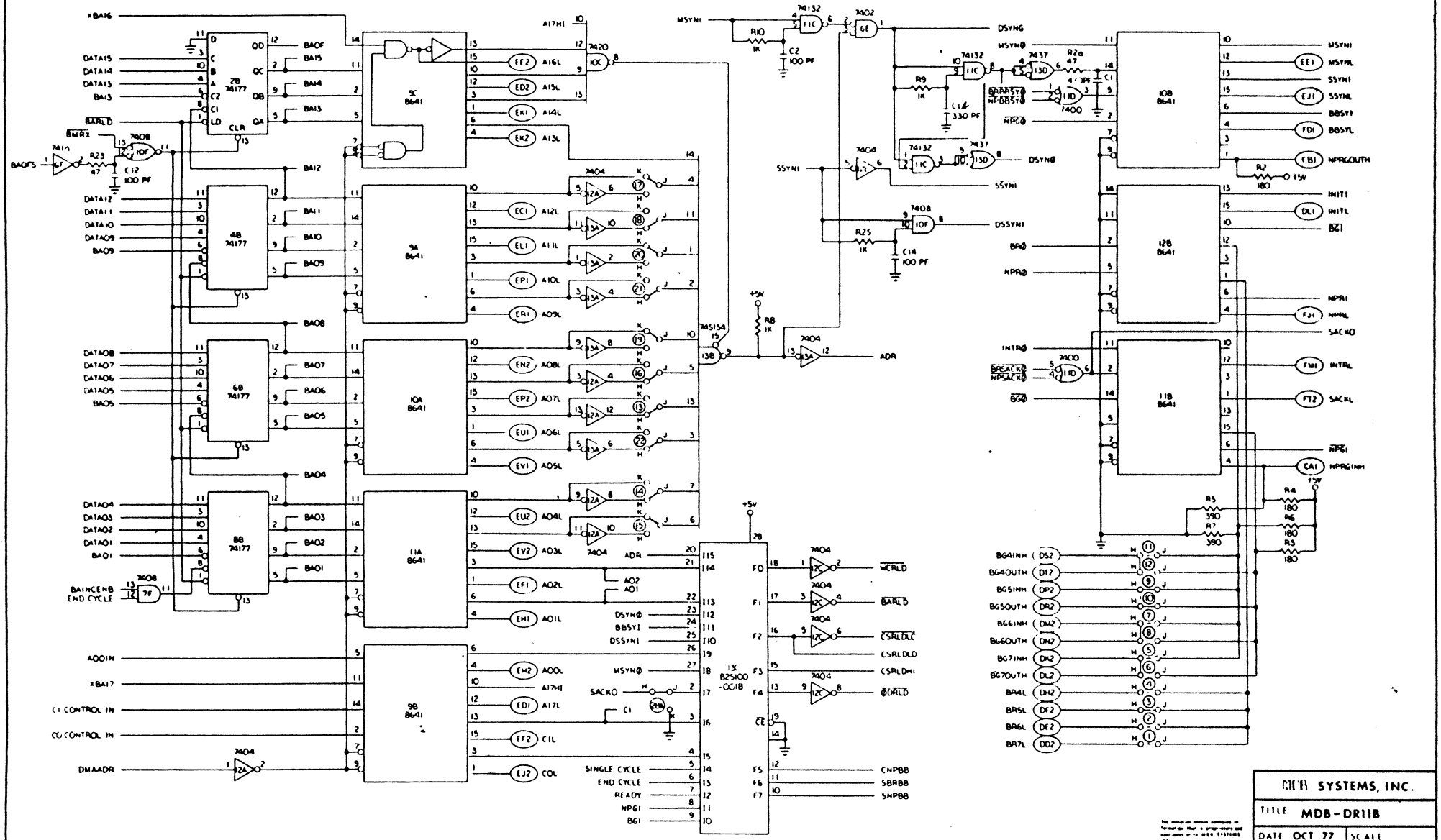
SYSTEMS, INC.	
TITLE MDB-DR11B	
DATE OCT 77	SCALE
SHEET NO. 1 OF 4	DWG 40311 REV A

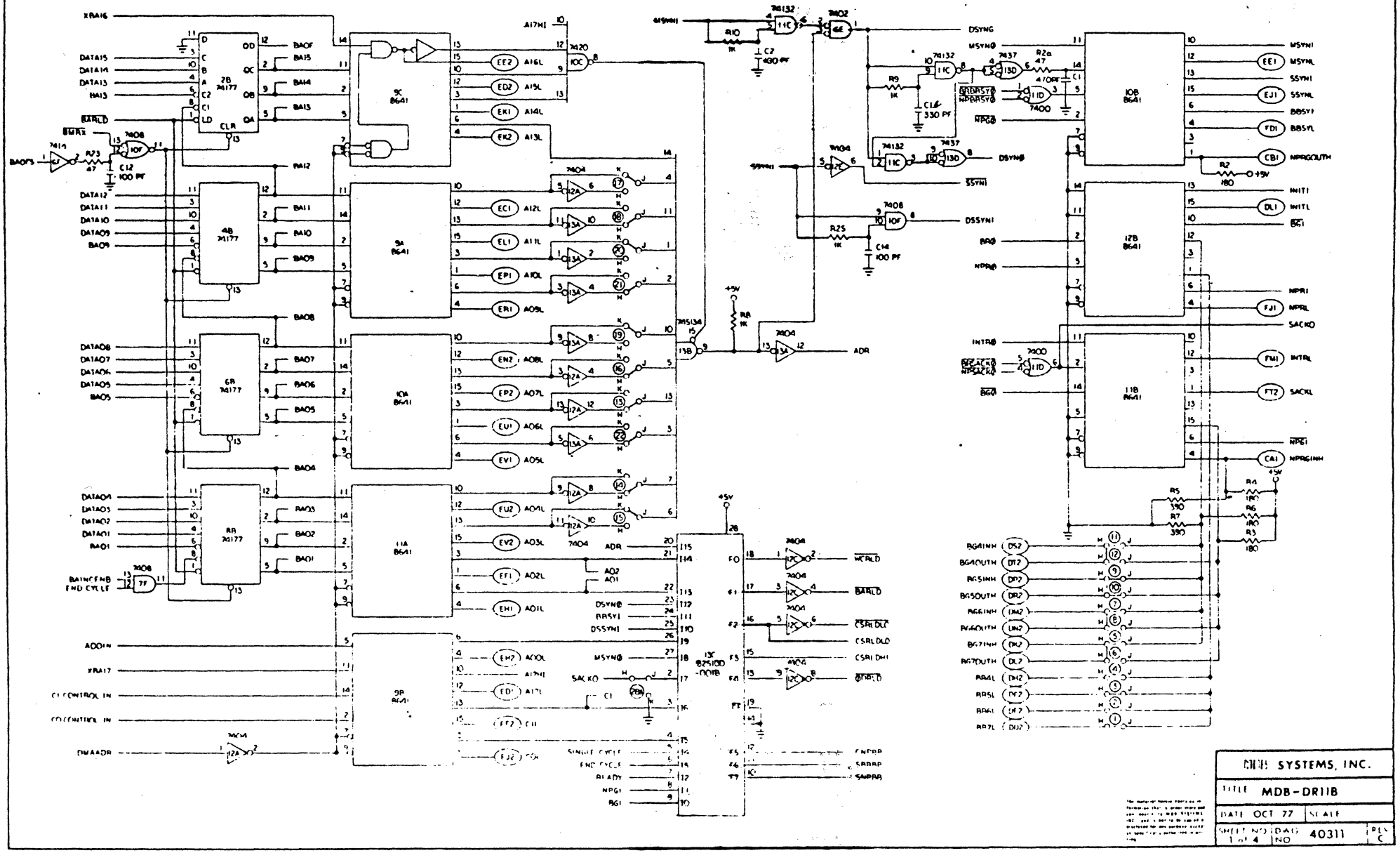


MDB SYSTEMS, INC.		
TITLE: MDB-DR11B		
DATE: OCT 77	SCALE:	
SHEET NO 2 of 4	DWG NO: 40311	REV A


BMR
BMRX
DATAI5
DATAI4
DATAI3
DATAI2
WC12
WCRLD
WC15
WC14
WC13
WC12
DATAI1
DATAI0
DATAO9
DATAO8
WCO8
WC11
WC10
WC09
WCO8
DATAO7
DATAO6
DATAO5
DATAO4
WCO4
WCO7
WCO6
WCO5
WCO4
DATAO3
DATAO2
DATAO1
DATAOO
WCOC
WCO3
WCO2
WCO1
WCOO
DMAADRX W. INH. ENB
7400
8B
1B 74177
2B 74177
3B 74177
5B 74177
7B 74177
BMR
DATAI5
DATAI4
DATAI3
DATAI2
ØDRLD
DATAI1
DATAI0
DATAO9
DATAO8
DATAO7
DATAO6
DATAO5
DATAO4
DATAO3
DATAO2
DATAO1
DATAOO
DAT15
DAT14
DAT13
DAT12
DAT11
DAT10
DAT09
DAT08
DAT07
DAT06
DAT05
DAT04
DAT03
DAT02
DAT01
DAT00
1A 74177
2A 74177
3D 74177
4D 74177
5D 74177
7D 74177
INIT
NEXM
ATTN
7404
7420
10C
DATAO5
DATAO4
DATAO6
CSRLDLO
BMR
BAOF
5E 74177
XBAI7
XBAI6
IENB
IENB
BAOFS
DATAOO
DATAO1
DATAO2
DATAO3
CSRLDLO
MAINT
DMAADRX
BMR
7E 74177
FNCT1
FNCT2
FNCT3
7408
7F
+5V
R21
1K
DATAI2
CSRLDHI
BMR
4F 7474
MAINT
INIT1
DATAI4
INIT
BMR
ERROR
ERROR
READY
READY
WCI5
9E 7474
GO
DATAOO
CSRLDLO
7400
8D
6F
DATAO8
CSRLDHI
7400
5F
READY
CYCLE
CYCLE REQ A
CYCLE REQ B
7402
6E
CYCLF
DMAADRX
7402
8F
BE 7474
BUSY
BUSY
END CYCLE
DATAO8
CSRLDHI
BMR
7404
6F
7408
7F
7402
8F
7404
9F
END CYCLE
MSC
4F 7474
BUSY
7404
6F
R22
47
7404
5F
C11
220 PF
DECOUPLING CAPACITORS AS REQUIRED
+5V
GND
C1
22 UF
C2
.01 UF
CA2
DA2
EA2
FA2
CC2
ET1
EC2
ET1
FC2
FT1
MDB SYSTEMS, INC.
TITLE MDB-DR11B
DATE OCT 77
SCALE
SHEET NO 3 OF 4
DWG NO 40311
REV A

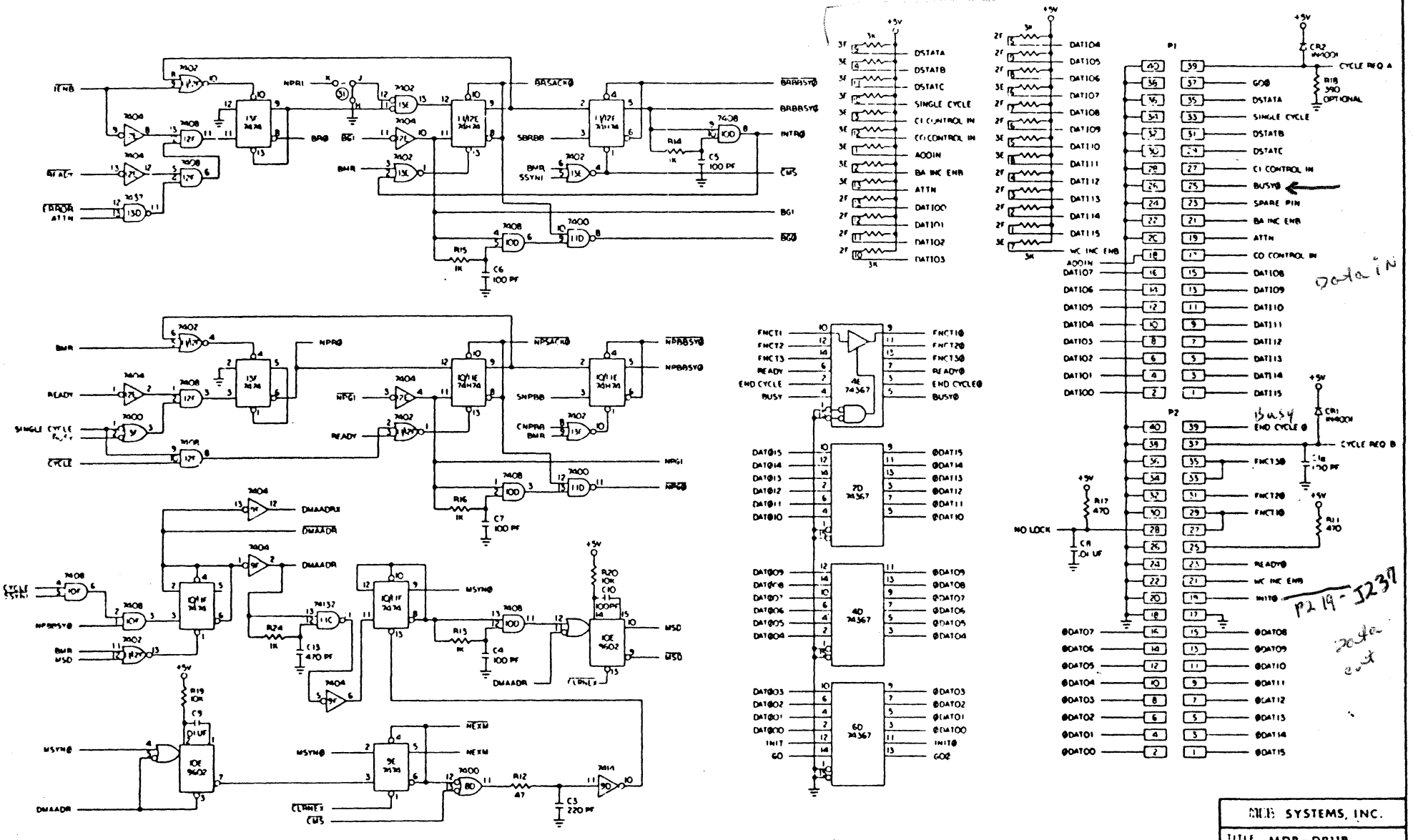

MDB SYSTEMS, INC.
TITLE MDB-DR11B
DATE OCT 77
SCALE
SHEET NO 4 of 4
DWG NO 40311
REV A

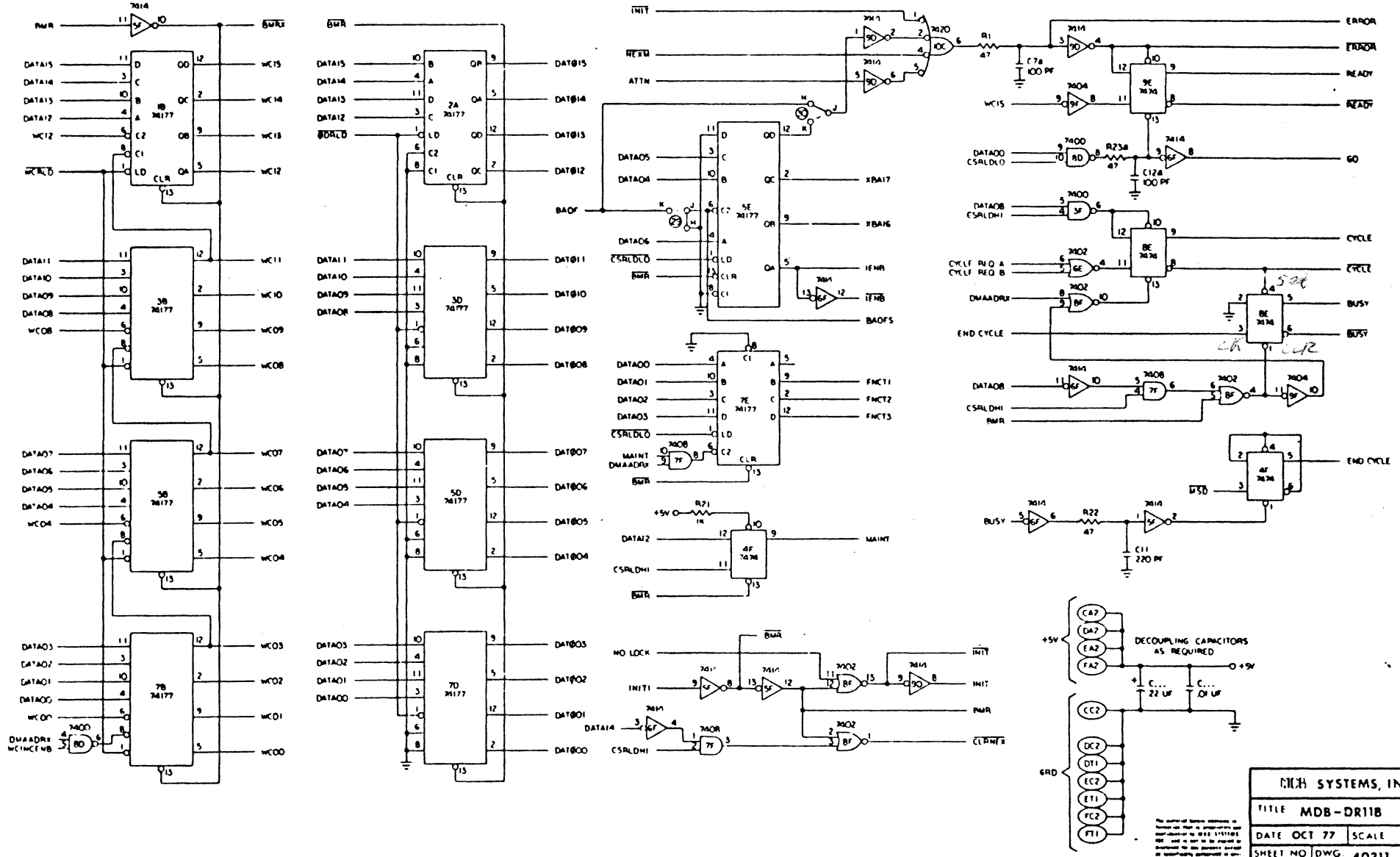

MDB SYSTEMS, INC.
TITLE MDB-DR11B
DATE OCT 77
SCALE
SHEET NO 1 of 4
DWG NO 40311
REV C



NOTE: CR1 & CR2 have been replaced with 3.3K 1/4 W resistors.

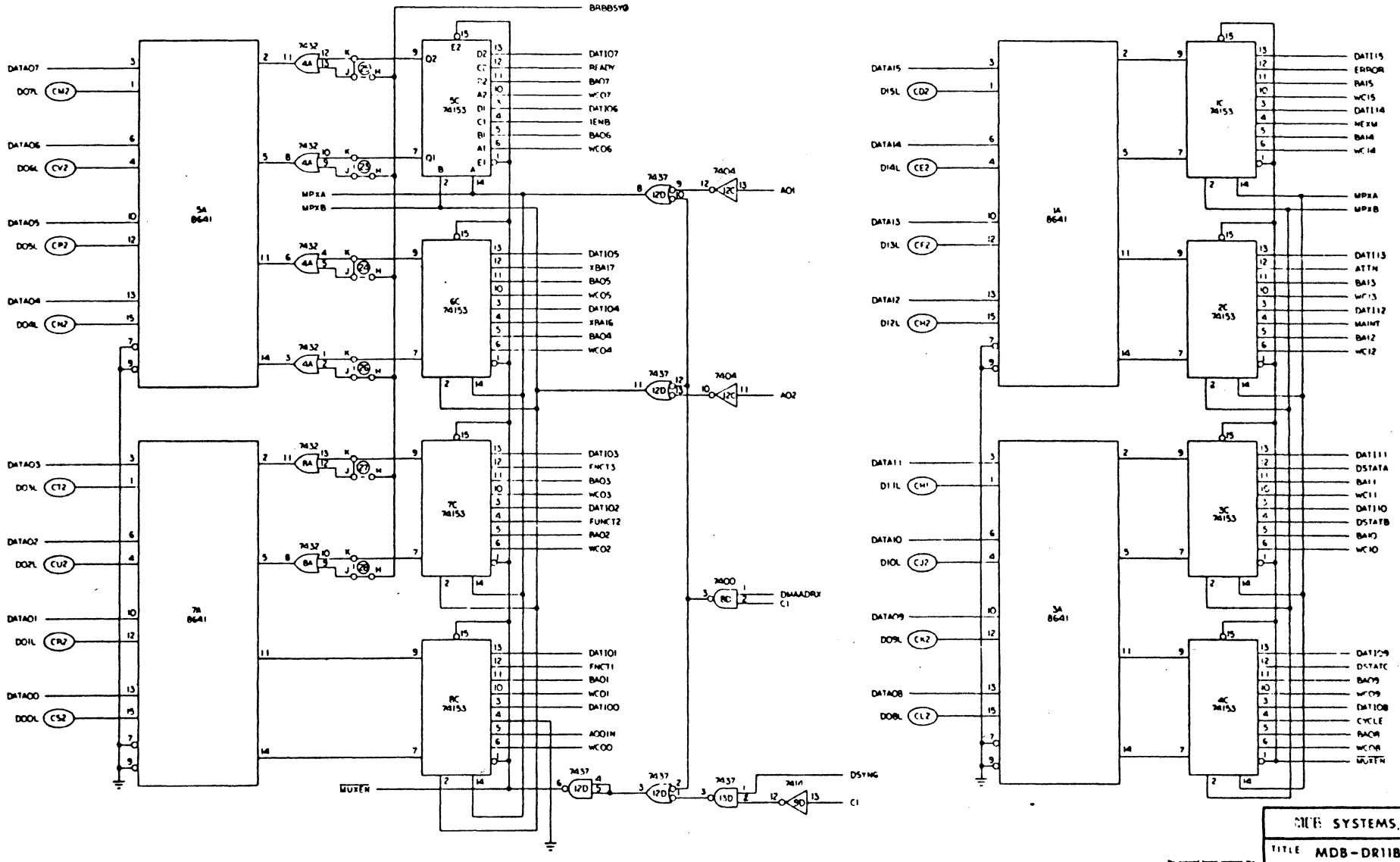
40311 REV. C1


IENB
NPR1
BRSACK@
BRBBSY@
BR@
BG1
SBRBB
INTR@
BMR
SSYNI
CWS
READY
ERROR
ATTN
BG1
BG@
RI15 1K
C6 100 PF
BMR
READY
SINGLE CYCLE
CYCLE
NPR@
NPRSACK@
NPRBBSY@
NPG1
SNPRB
CNPRA
BMR
NPG1
NPG@
RI16 1K
C7 100 PF
DMAADR1
DMAADR
DMAADR
CYCLE SYNC
NPRBBSY@
BMR
MSD
MSD
MSYN@
DMAADR
RI24 1K
C13 470 PF
MSYN@
C4 100 PF
DMAADR
CLRNEX
RI20 10K
C10 100 PF
RI19 10K
C9 .01 UF
MSYN@
DMAADR
NEXM
MSYN@
NEXM
CLRNEX
CWS
RI12 47
C3 220 PF
DSTATA
DSTATB
DSTATC
SINGLE CYCLE
C1 CONTROL IN
C0 CONTROL IN
ADDIN
BA INC ENB
ATTN
DATI00
DATI01
DATI02
DATI03
DATI04
DATI05
DATI06
DATI07
DATI08
DATI09
DATI10
DATI11
DATI12
DATI13
DATI14
DATI15
WC INC ENB
P1
P2
CYCLE REQ A
GO@
DSTATA
SINGLE CYCLE
DSTATB
DSTATC
C1 CONTROL IN
BUSY@
SPARE PIN
BA INC ENB
ATTN
C0 CONTROL IN
ADDIN
DATI07
DATI06
DATI05
DATI04
DATI03
DATI02
DATI01
DATI00
DATI08
DATI09
DATI10
DATI11
DATI12
DATI13
DATI14
DATI15
BUSY
END CYCLE @
CYCLE REQ B
FNCT3@
FNCT2@
FNCT1@
READY@
WC INC ENB
INIT@
@DATO7
@DATO6
@DATO5
@DATO4
@DATO3
@DATO2
@DATO1
@DATO0
@DATI8
@DATI9
@DATI0
@DATI1
@DATI2
@DATI5
@DATI4
@DATI5
CR2 1N4001
RI18 390 OPTIONAL
CR1 1N4001
C18 470 PF
RI7 470
RI1 470
NO LOCK
CR .01 UF
FNCT1
FNCT2
FNCT3
READY
END CYCLE
BUSY
FNCT1@
FNCT2@
FNCT3@
READY@
END CYCLE@
BUSY@
DATO15
DATO14
DATO13
DATO12
DATO11
DATO10
DATO09
DATO08
DATO07
DATO06
DATO05
DATO04
DATO03
DATO02
DATO01
DATO00
INIT
GO
@DATO15
@DATO14
@DATO13
@DATO12
@DATO11
@DATO10
@DATO09
@DATO08
@DATO07
@DATO6
@DATO5
@DATO4
@DATO3
@DATO2
@DATO1
@DATO0
INIT@
GO@
4K 74367
7D 74367
4D 74367
6D 74367
P219-J239
Data IN
busy
MDB SYSTEMS, INC.
TITLE MDB-DR11B
DATE OCT 77
SCALE
SHEET NO 2 of 4
DWG NO 40311
REV C



MDB SYSTEMS, INC.

TITLE	MDB-DR11B	
DATE	OCT 77	SCALE
SHEET NO	DWG NO	REV
3 of 4	40311	C



NCR SYSTEMS, INC.	
TITLE MDB-DR11B	
DATE OCT 77	SCALE
SHEET NO 4 of 4	DWG NO 40311 REV C

MDB SYSTEMS

ERRATA: MDB DR11B INSTRUCTION MANUAL

MDB Systems regrets the errors which appear in this manual. Rather than delay the information, please make the following corrections:

Page 7, Bus Address Overflow Control

The last line of the second paragraph reads:

"29/H-K and 30/H-K."

It should be corrected to read:

"29/J-K and 30/J-K."

Page 7, Non-Processor Request Control

The last line of the second paragraph reads:

"wire jumper at 31/H-K."

It should be corrected to read:

"wire jumper at 31/J-K."

May 31, 1979
DR11B Manual

MDB SYSTEMS INC.
1995 N Batavia Street
Orange, California 92665
714-998-6900
TWX 910-593-1339