This package has all the documentation to build, repair, and test omega 300s and omega 400s.

The differences are as follows

1) the omega 300 and the omega 420 are identical, except the front panels. The 300 has omega 300 and the 420 has omega 420 on the front panel. Both of these are 4 bit plane units (only half of the rams get stuffed).

Omega 300 - 4 bit plane and will operate as follows
1024 X 768 at 33hz refresh
736 X 552 at 60hz refresh
640 X 480 at RS170
Omega 305 - 4 bit plane and will operate as follows
1024 X 768 at 33hz refresh
736 X 552 at 60hz refresh
640 X 480 at RS170
1024 X 1024
Omega 420 - 4 bit plane and will operate as follows
1024 X 768 at 33hz refresh
736 X 552 at 60hz refresh
640 X 480 at RS170
Omega 425 - 4 bit plane and will operate as follows
1024 X 768 at 33hz refresh
736 X 552 at 60hz refresh
640 X 480 at RS170
1024 X 1024
Omega 440 - 8 bit plane and will operate as follows
1024 X 768 at 33hz refresh
736 X 552 at 60hz refresh
640 X 480 at RS170
Omega 445 - 8 bit plane and will operate as follows
1024 X 768 at 33hz refresh
736 X 552 at 60hz refresh
640 X 480 at RS170
1024 X 1024

All the Omega series have built in self tests which is described in this document. Once units pass self test, there is a program on the VAX, manuf. LAMDA, and eng. LAMDA called ctest8 which will test most functions of the omega products.

NAME

ctest - perform crc tests on the Omega display controllers.

SYNOPSIS

ctest [-option...] ... loop_count

DESCRIPTION

Ctest draws various patterns on the screen and then reads back the CRC and compares it against a previously stored value. If the two do not agree, ctest prints out a message logging the error. The loop_count determines how many times ctest repeats the test. If the loop_count is specified as 0, ctest goes into 'learn' mode and tries to create the CRC definition file.

The default parameters are: -33 and loop_count = 1.

The following options are interpreted:

-h Halt if a CRC error is detected.

-33 Take the stored CRCs from the file crc33 in the current directory.

-66 Take the stored CRCs from the file crc66 in the current directory.

-c file_name
Use the specified file_name as the source for the stored CRCs.

-p file_name
Use the specified file for additional program names for generating patterns. The program names in the file are one name per line.

FILES

/usr1/john/red/test/ctest
/usr1/john/red/test/ctest.doc

SEE ALSO

BUGS

HISTORY

Written by John Providenza 7-5-82

METHEUS OMEGA 400 SERVICE MANUAL

CONTENTS:

**********INTRODUCTION**********

The Omega 400 is a high performance display controller based on 64K RAM and Bit Slice technology. Aside from interface options, 2 models are available: Omega 420, with 4 planes of 1024 X1024 pixels, and the Omega 440 with 8 planes.

The controller has no adjustments, and installation consists of simply unpacking, connecting power and RGB coax to the monitor, and the appropriate cable to the host computer. Extensive self-test capability is built into all models, and the Ready light on the front panel gives a high reliability indication that these self tests have been passed.

The user need only be concerned with one stap option: monitor refresh at 33 Hz interlaced or 60 Hz non-interlaced as described in the Operator's Manual.

**********SPECIFICATIONS**********

ENVIRONMENTAL:

Temperature: -40C to +75C non-operating

	0C to +55C operating
Humidity:	+65C @ 95% non-condensing non-operating +40C @ 95% non-condensing operating
Vibration: (non-operating)	5 to 7.5Hz 0.5 in displacement 7.5 to 200Hz @ 1.5 G 7.5 to 5 Hz 0.5 in displacement 12 min/cycle, 84 min/axis
Shock: (non-operating)	Magnitude: 30 G Duration: 11 msec # of shocks: 3/surface on 6 surfaces Waveform: Half sine Bench drop: 4 in tilt
Altitude:	25,000 ft. non-operating 15,000 ft. operating
Drop Test: (non-operating, packaged)	30 in. each face and corner
EMI:	VDE Class B
SAFETY:	UL114 (Office Machines) UL478 (EDP) CSA154 (EDP) IEC380 (Equivalent to VDE 0806) IEC435 (EDP 1982)

ELECTRICAL:

Rated Line Voltage:	Low Range 90 to 132 V AC High Range 180 to 264 V AC
Frequency Range:	47 to 63 Hz
Supply Regulation:	< .2%
Ripple:	< 1 mV
Power Dissipated:	<100 W; 85 W typical
Supply Ratings:	+5 V @ 20 A -5V @ 12 A
Fuse:	4 A Low Voltage Range fast blow 2 A High Voltage Range fast blow
Clocks:	72.440 Mhz crystal controlled and binary subdivisions
Video:	RS-343 Compatible. 1V p-p with sync on ~~each of Red~~, Green ~~and Blue~~. .7V video, .3V sync within 5%.

FUNCTIONAL:

Resolution:	1024 X 768 @33 Hz interlaced 736 X 552 @60 Hz non-interlaced Other options are soft programmable, such as 640 X 480 30 Hz RS-170.
Host Interfaces:	HPIB

GPIO
DEC Parallel
RS-232 asynchronous

Tablet Interfaces: HP 9111A
SummaGraphics Bit Pad
GTCO Digipad

Self Test: >90% of IC failures caught
Data Bus counter check
Bit slice register increment check
Loop counter check
I/O loop back check
scratchpad RAM check...load with addr
Memory test: write all 1s, 0s, 1s, 0s; readback
Write Mask Write Data check with readback
Vector drawing test followed by signature read

Reset: Power Up causes full self test
Host reset only initializes I/O interface

Op Codes: Unless otherwise specified, all writes to pixel memory observe the Write Data, Write Mask and present Area Pattern. That is, a write in plane k occurs only if bit k of the Write Data Register and Write Mask Register are = 1 AND the present Area Pattern function A(x,y) = 1.

Byte arguments are indicated by lower case, word arguments by upper case. Word arguments are read in the order LO BYTE, HI BYTE.

STATE VARIABLES:

P1 (pointer 1)
P2 (pointer 2)
WRITE DATA (also called "current color")
WRITE MASK (determines planes written)
PATTERN REGISTER (incl. line and area patterns)
READ MASK (planes viewed)
BLANK
BLINK
CMAP (contents of 256 locations)
CONFIGURATION (33/60 Hz, #planes, tablet present)
SETCORN, SETCSZ, FSIZE, CSPACE (character info)
SZCUR (cursor size)
CURRENT POLYGON STRUCTURE (vertex list)

MNEUMONIC	HEX	DESCRIPTION
AFILL1	68	Read Pixel @ P1 Do While Neighbor Color=P1 Pixel Color Write Neighbor with Write Data End P1 and P2 unmodified.
AFILL2 <f>	69	Read Pixel @ P1 Do Until Neighbor Color= f Write Neighbor with Write Data

End
P1 and P2 unmodified.

ARC <L>	62	Draw arc of length L using Write Data and center of curvature P1. Begin at P2. P2 left at end of arc upon completion.
BLANK <b>	4B	b is LSB of argument byte. IF b=1 then blank screen and give processor access. IF b=0 then return to screen-priority mode.
BLINK <b>	4D	b is LSB of argument byte. IF b=1 then toggle plane 7 at 2Hz. using Read Mask. IF b=0 then restore steady plane 7.
CHAR <c1,c2...,cN>	6B	Draw text starting with P1 pointing to the lower left corner of the 16 X 8 character cell. c1,c2 etc. are ASCII codes 0-127. cN is the ESC charcter (#27) and terminates text mode. See also SETCSZ,FSIZE and CSPACE.

Control Characters Decoded:

CR	Return to left margin
LF	Move pointer down one line
BS	Move pointer back one space
ESC	Exit text mode

Font Graphics are shown in Appendix B.

CLEAR	60	Fill screen with Write Data.
CMAP <a,r,g,b>	51	Load color map location a with values r,g and b.
COMPDR	72	Draw a vector between P1 and P2 complementing present pixel values. Leave P1 at P2 after.
CRTWR <r,d>	46	Write the 6845-1 CRT Controller Register r with d.
CSPACE <DX,DY>	48	Auto increment between successive characters. Apply increment DX,DY from lower left corner of cell, then apply transformation specified by SETCORN.
CURS	71	Draw cursor at P1. Drawn in complement mode, with crosshair width and height as set by SZCUR. Automatically removed upon receipt of next op code. Write Mask and Area Pattern ignored.
DRAW	61	Draw vector from P1 to P2. Leave P1 at P2 after.
FFILL	65	Fill rectangle dfined by diagonal P1,P2. Approx. 16 times faster than RECT2; no patterns allowed.
FSIZE <dx,dy>	49	Font size. 0<dx<7 , 0<dy<15 . These define a window on the 16 X 8 character cell.
GRAFIN <a>	4A	Set Graphic Input (from Tablet). The argument may be one of the following:

0 Init scale factors and delimiter(hex 80).

1 Set cursor tracking. Cursor appears at a screen position determined by taking the tablet x and y, and adding the Offset

specified as a Scale Factor (see 3 below). The position of P1 is set by the product of the previous sum and the current x and y coefficients, also a part of Scale Factor. The present screen coordinates are sent automatically when the tablet stylus of cursor button is depressed. This may be programmed to occur on a leading edge, both leading and trailing edge, or on button level. The latter is the default state. Refer to entry 7 below for details.

The format of the message sent to the host is as follows:

	BIT							
BYTE	7	6	5	4	3	2	1	0
1	0	1	pb8	pb4	pb2	pb1	0	0
2	0	0	x5	x4	x3	x2	x1	x0
3	0	0	0	0	x9	x8	x7	x6
4	0	0	y5	y4	y3	y2	y1	y0
5	0	0	0	0	y9	y8	y7	y6

Exit of cursor tracking mode occurs automatically upon receipt of a new op code.

2 Set Transparent Mode. Enable full-duplex communication between tablet and host. Useful for programming tablet. Exit occurs upon receipt of Delimiter from host.

3 Set Scale Factors. The Omega will expect eight bytes to follow, that specify the offset and multiplication to be done on tablet data in producing a cursor position.

BYTE	VALUE
1	X Offset Low Byte
2	X Offset High Byte
3	X Multiplier Fraction
4	X Multiplier Integer
5	Y Offset Low Byte
6	Y Offset High Byte
7	Y Multiplier Low Byte
8	Y Multiplier High Byte

4 Define Delimiter. Receipt of Delimiter from host while in Transparent Mode causes exit of Graphin. The default delimiter is hex 80.

5 Sample Position in Screen Coordinates. Sends the previously described 5 byte message to the host in screen coordinates.

6 Sample Position in Tablet Coordinates. The result is one tablet coordinate sample, in the format of the tablet used.

7 Modify Mode Register. A Grafin Mode Register has the following bit functions defined:

BIT	IF=0(default)	IF=1
0	Wrap around if scaled tab x,y exceeds screen.	Hold cursor at screen edge if tab x,y exceeds screen.
1	Send during button push if coordinates diff. (level mode)	Send only one value, upon button change. (edge mode)
2	Button press causes transmit.	Button press ignored.
3	If Edge Mode, use leading only.	If Edge Mode, use both leading & trailing edges.

The Mode Register is written either as a whole, if bit 7=1, or individual bits may be written to the value of bit 3, and the particular bit addressed by bits (2,1,0). Individual bit set requires that bit 7=0.

INIT 5E Soft Init. Receipt of this code causes the following:

- Write Mask set to FF
- Write Data set to 0
- Set solid pattern
- Set No Zoom & Pan
- Turn on Read Mask for all planes
- Load Character Gen with ESC
- Clear line pattern counter
- Clear Scratchpad RAM
- Set default parameters in Scratchpad:
  - Font Width = 8
  - Font Height =16
  - Auto Increment dx=8
  - Auto Increment dy=0
- Initialize tablet, delimiter etc.
- Load Color LUT with default values

The default Color LUT values are most easily specified in terms of pixel value (address) for a given ratio of red,green and blue:

pixel value=224*R+28*G+3*B where R and G are chosen from the set (0,1/7,2/7,...,7/7) and B is chosen from (0,1/3,2/3,3/3).

MOVP1 <X,Y> 52 Move P1 to X,Y.

MOVP2 <X,Y> 53 Move P2 to X,Y.

PATTERN <p> 50 Set pattern as specified in p. Refer to figure __ for a graphic description of the available line and area patterns. Area patterns remain in effect through all drawing operations except cursor and flash fill; in these instances drawing is in solid mode i.e. line pattern 0.

BIT

7 6 5 4 3 2 1 0

```
 |   |   |   |   |   |   |   |
--mode-----  invert line  --pattern--
```

Bit 3 selects line pattern if a 1, area if a 0.
Bit 4 selects normal mode if 0, or swaps the foreground with background if = 1.

Mode: The pattern is considered a binary function of run length (line pattern) or x,y (area pattern). If the function =1, then this is defined as Foreground (FG). Similarly a value of 0 is defined as Background (BG). These definitions can be interchanged via bit 4 in the Pattern argument byte.

Abbreviate the Write Data register byte as WD, and the Write Mask register byte as WM. Then the pattern mode options and mode bit values are:

OPTION	BIT VALUE	MEANING
FG <-- WD	BIT 6=0	write all
FG <-- WD*WM	BIT 6=1	write selected
BG <-- BG*WM'	BIT 7=1	zero selected
BG <-- 0	BIT 7=0 and BIT5=0	zero all
BG <-- BG	BIT 7=0 and BIT5=1	no change

PIXBLT<DX,DY,d> 70

Copy a rectangle of pixels of width DX and height DY relative to P1 to a rectangle of identical size relative to P2. The direction byte is used to prevent problems with overlapped regions; one must avoid writing a pixel before it is read.

DIRECTION BIT	IF=0	IF=1
0	normal	swap x,y axies on destination.
1	increment destination y	decrement destination y
2	increment destination x	decrement destination y
3	increment source y	decrement source y
4	increment source x	decrement source x

POLYC 45

Sub polygon delimiter command; used for concatenated polygons, holes etc. Inserted after POLYS, POLYV<X0,Y0>, POLYV<X1,Y1>, ... POLYV<Xk,Yk> to define a k+1 vertex figure. The following POLYV<Xk+1,Yk+1>, POLYV<Xk+2,Yk+2>, ... POLYV<Xn,Yn>, POLYC will define another sub polygon of n-k vertices. This process may continue up to the stack limit (900 vertices).

A subsequent POLYO will cause outline drawing of the various sub polygons, without drawing any ties. A POLYF will perform a parity fill on the sub polygons (see POLYF below).

POLYF	67	Polygon Fill. The current list of sub polygons in the stack will be scan converted and filled inclusive of edges. A parity fill occurs, meaning that only those regions are filled which are reached from the screen boundary via an odd number of edge crossings.
POLYM <X,Y>	44	Polygon Move. The polygon edge from the previous point to X,Y is flagged so as not to be drawn during POLYO. It is in other respects treated as a normal polygon edge.
POLYO	66	Polygon Outline. Outline the individual sub polygons, except where POLYM occurs.
POLYS	56	Polygon Start. Clears polygon working area.
POLYV <X,Y>	57	Polygon Vertex. Adds vertex X,Y to the present sub polygon.
PPAN	5B	Set origin of display to P1. Confined to 16 pixel increments in X when no zoom.
RDCONF	5D	Read Configuration. Upon receipt, the Omega returns two bytes. The first has bits 0 through 4 defined:

BIT	IF=0	IF=1
0	33HZ	60HZ

These bits encode one of 8 configurations:

0=Omega 420
1=Omega 440
2 through 7 reserved for future use.

4	No Grafin	Grafin Installed

The second byte specifies the microcode release level as two hex numbers. For example, the byte 33 hex means version 3.3 microcode is installed.

RDMSK <m>	4C	Read Mask. The byte m specifies which planes are to be viewed, and has no effect on readback functions such as RDR, RPIXEL, AFILL, COMPDR or XDRAW. Overridden by blink function.
RDR	6E	Read Rectangle. The Omega returns a stream of pixel values from the rectangle defined by P1,P2 beginning at the upper left corner and progressing left to right within top to bottom. Read is exclusive of right and bottom edges, so that the total number of pixels transferred is

ABS(P1X-P2X)*ABS(P1Y-P2Y)

P1 and P2 are not modified.

RECT1	63	Outline the rectangle defined by P1,P2 diagonal. P1 and P2 are left unmodified.
RECT2	64	Fill rectangle defined by P1,P2 diagonal, inclusive of edge. P1 and P2 are left unmodified.

RLFILL <DX> 6A
Run Length Fill. Write DX successive pixels from P1, including P1, and leave P1 one pixel past the sequence.

RMOVP1 <DX,DY> 54
Relative move of P1. Argument is 2s compliment.

RMOVP2 <DX,DY> 55
Relative move of P2. Argument is 2s compliment.

RPIXEL 6C
Read pixel at P1. A single byte is returned.

SETCOLOR <c> 4E
Set Color, or Write Data Register.

SETCORN <d> 59
Set Character Orientation. The direction byte assigns meaning to the lower three bits; these indicate character rotation and mirror inversion. Assume a relative 360 degree axis with ccw angle:

d	ROTATION	INVERSION
0	0	no
1	-90	yes
2	180	yes
3	-90	no
4	0	yes
5	90	no
6	180	no
7	90	yes

Transformations applied by CSPACE happen after this one.

SETCSZ <x,y> 58
Set Character Size. In text mode, characters are drawn within the constraints of FSIZE, CSPACE, and SETCORN and this parameter. Its effect is to zoom characters via pixel replication, and the bytes x and y specify the replication number in the X and Y directions PRIOR TO ROTATION.

SIGRD 5C
Read signature. A CRC polynomial is returned as two sorted bytes. In non interlaced mode the two bytes are identical; in interlace mode they are odd and even field signatures.

SYNC <f> 5F
Wait until f fields have occured before accepting further commands. Useful for animation.

SZCUR <dx,dy> 47
Set Cursor Size. The cursor is displayed either in response to the CURS command, or during GRAFIN cursor tracking mode. It is a complementing crosshair with dimensions set by dx and dy of this command. The cursor dimensions will be twice these values.

WPIXEL 6D
Write pixel at P1 using current color.

WRMSK <m> 4F
Set Write Mask to byte value m; this determines the particular planes written for most drawing operations. It is ignored in cursor drawing and under certain pattern conditions.

WRR <b1,b2..bn> 6F
Write Rectangle defined by P1 and P2, beginning in the upper left and proceeding left to right within top to bottom. Fill is exclusive of the bottom and right edges, and the number of pixels expected is the same as for RDR. P1,P2 unmodified.

XDRAW	43	Exclusive OR vector draw from P1 to P2. The pixel written is the EXOR of the previous value and the Write Data register. P1 is left at P2 afterwards.
ZOOM <z>	5A	Zoom screen via pixel replication by a count of z. The position of the origin remains unchanged. P1,P2 unmodified.

**********THEORY OF OPERATION**********

*INTRODUCTION

The Metheus Omega 400 is a high performance raster graphics display controller constructed from a mixture of MOS and bipolar technology. The architectural components include:

- A Bit-slice processor with 64 bit microword
- Megabyte of DRAM, organized as 8 megabit planes 1024X1024
- Integrated signature analyzer
- Hardware pan and zoom
- Line and area pattern generators
- EPROM based character generator
- 36 MHz pixel clock

Communications with the host computer occur over the Omega I/O interface. Present options include 16 bit parallel, 8 bit IEEE-488, and asynchronous serial RS-232.

A graphic tablet interface option is supported, allowing a local cursor to track the tablet stylus. Both RS-232 and IEEE-488 tablet interfaces are available.

A fully configured system is shown in figure 1:

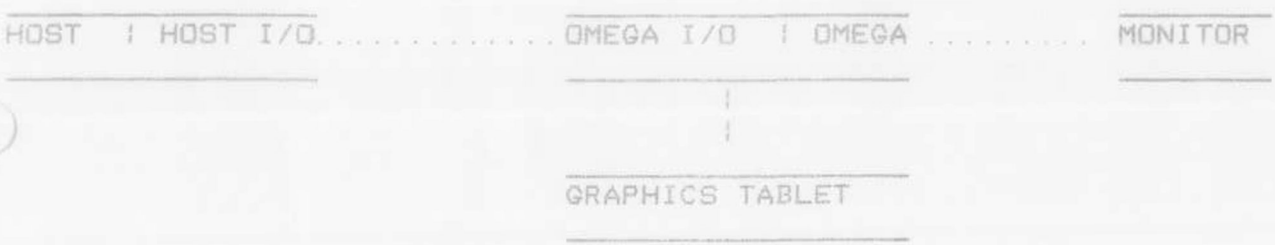

Fig. 1

The link between host and Omega is bidirectional. The host sends opcodes

and arguments in the Omega syntax, and thus builds a picture in display memory. The host may also read display memory or Omega status.

The link to the graphics tablet is also bidirectional, although the tablet functions primarily as a "talker". Thus software configurable tablets can be set under host control.

The link between Omega and monitor is actually three coaxial cables carrying composite video conforming to the RS-343 standard for RGB transmission.

*THE OMEGA 400: THEORY OF OPERATION

**Functional Overview

A preliminary partition of the Omega hardware appears in figure 2. At the heart of the device is the dynamic ram bit-map, access to which is arbitrated between processor and screen refresh.

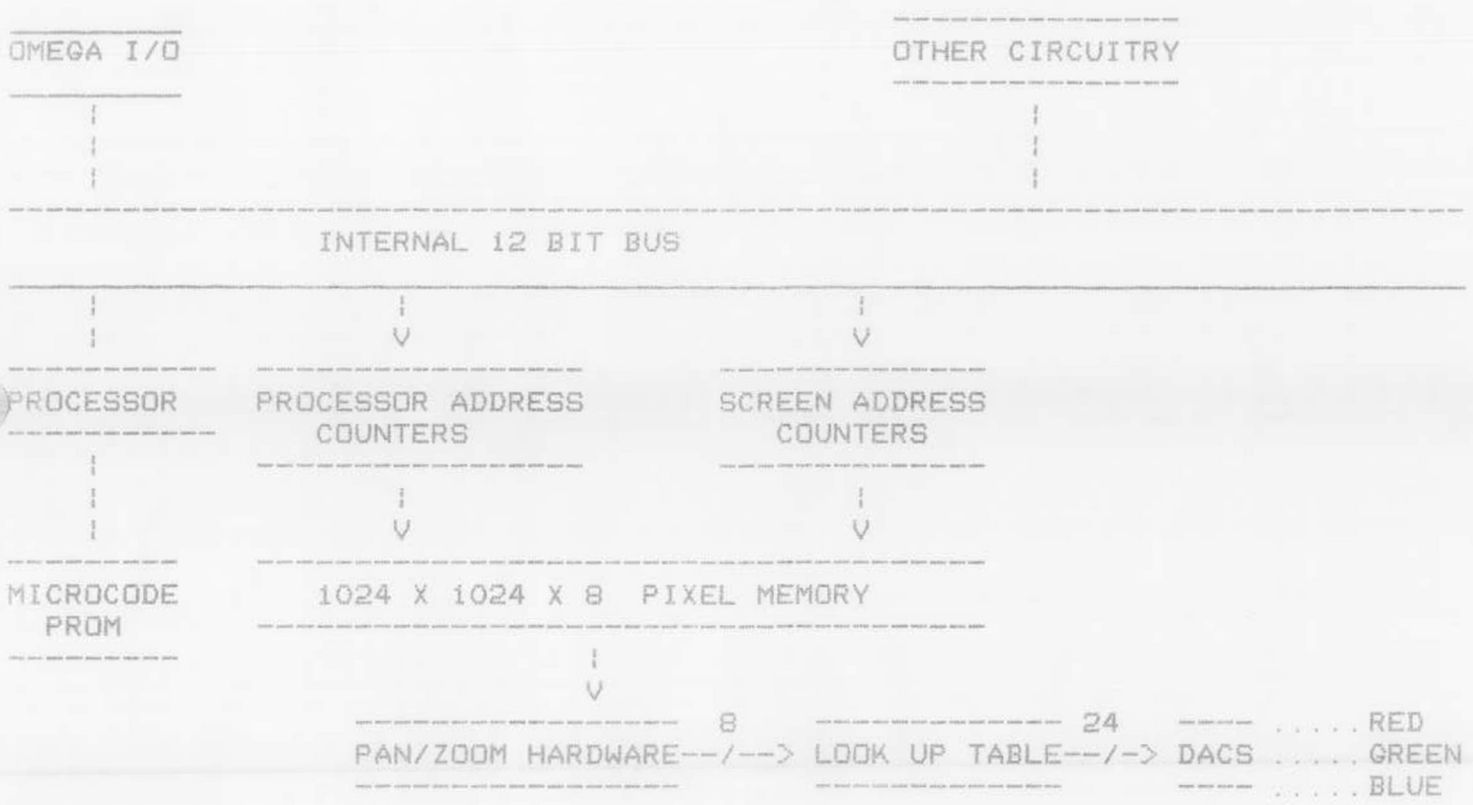

Fig. 2. Main components of the Omega 400.

The functions of these blocks are as follows:

OMEGA I/O. The host port. Omega processor communicates with a "2-wire" handshake, ready and strobe.

PROCESSOR. 12 bit, composed of 3 2901B bit slices, running at a 220 ns. cycle time.

MICROCODE. A 64 bit wide PROM array controlling processor alu, source and destinations for data transfers, load of the processor counters and all important Omega functions. Only the high speed functions such as memory cycle timing are performed independently, in state machines or random logic.

PROCESSOR ADDRESS COUNTERS 12 bit counters which respond to the commands Load, Up/Down, and Count. One for each of X and Y.

SCREEN ADDRESS COUNTERS	A 6 bit counter for X and a 10 bit counter for Y. These only count up, but may be loaded with a start count other than zero to achieve the Pan function. Automatically loaded on each vertical retrace. Counting can be pre-scaled by a modulo Zoom value.
PIXEL MEMORY	128 DRAMS, 16 chips of 64K bits per plane. Organized such that blocks of 16 adjacent pixels on a raster line are each contributed by a different DRAM output. Memory operates at a 220 ns write cycle and a 440 ns read cycle. The 8 planes are individually addressable through the Write Mask, Write Data, and Read Mask. These are each 8 bit registers with a flip flop for each of the 8 planes. As illustrated in figure 3, only when the Write mask is set for a particular plane is its write enable line allowed to pulse. When written, the value of the particular Write Data flip flop determines whether a 1 or a 0 is written. The Read Mask affects the planes read out, and has no effect on data read by the Processor.
PAN/ZOOM	This circuitry contains modulo counters which essentially mirror the function of the Screen Address Counters. Zoom is achieved by slowing down the entire pipeline from DRAM to the output DACS, causing pixel replication. Pan is achieved primarily by the Screen Address Counters, but these only address contiguous 16 pixel blocks. To obtain a finer offset, a circular buffer is used as a programmable delay line.
LOOK UP TABLE	The 8 bit path through Pan/Zoom continues to the Look Up Table, a 256 X 24 RAM that allows the user to work with 256 colors simultaneously from a palette of 16.7 million.
DACS	The 24 bits from the Look Up Table (LUT) are broken into 3 groups, and routed to 3 eight bit Digital to Analog Converters: Red, Green and Blue. Composite sync is added to the Green output to create a 1V p-p signal.

PLANE	WRITE MASK	WRITE DATA	READ MASK
0	0	1	0
1	1	1	1
2	0	1	1
3	1	0	1
4	1	1	0
5	0	0	1
6	1	0	1
7	1	1	0

Fig.3. In this example, plane 0 is neither read nor written. Plane 1 is written with a 1, and is viewed. Plane 2 is written, but not viewed. Plane 3 is written with a 0, and viewed. Plane 4 is written with a 1 and viewed, etc.

**Microcode Word Definition-Overview

The 64 bit microcode word resides in eight 16K PROMs, allowing 2048 steps of control memory. These PROMs are addressed by a 12 bit sequencer comprising two 2911As and a 2909A. The sequencer in turn is

driven by microcode control bits and branching conditions from various sections of the hardware. The next section will explain these conditions in more detail.

The microcode word is subdivided into five major groups, called fields:

1) Control field. 13 bits of control lines to regulate the processor address counters, the write enable generator for pixel memory, and other functions described below.

2) Data Bus Source and Destination Control. Every instruction must specify a driver and also a receiver for the internal data bus; this occurs even if no actual data transfer is required, in which case the destination is a dummy location. The sub-fields are:

Data Source	3 bits
Data Destination	5 bits

3) Conditional Branch Control. These 11 bits directly control the activity of the microcode sequencer, which in turn selects the next microcode word decoded. There are three sub-fields:

Branch Type	3 bits
Condition Code	8 bits

4) Bit Slice ALU Controls. 20 bits that specify internal action of the three 2901B bit slice parts. There are 5 subfields:

External Carry/Borrow	3 bits
ALU Destination	3 bits
ALU Function	3 bits
ALU Source	3 bits
Register Address	8 bits

5) Data Field. The microcode often must drive the data bus, either to load the ALU with a constant operand, preset data bus destinations to some value, specify a branch locatioon to the sequencer, or other operation. This is a single 12 bit field.

**Microcode Word Definition-Detail

1) Control Field.

BIT	SIGNAL	FUNCTION
63	BPTO-H	Stops the processor clock. Used for development only.
62	SPARE	Not used.
61	RLD-L	Specifies that the internal R Register of the sequencer is to be loaded with the contents of the data bus.
60	RSRO-H	Controls shifting of the Readback Shift Register (RSR). This register can be loaded with a contiguous 16 pixel group as pointed to by the processor address counters. This line works in conjunction with RSR1-H (bit 58) to command the following functions:

RSR1-H	RSR0-H	FUNCTION
0	0	Hold
0	1	Shift Right
1	0	Shift Left
1	1	Load

59	CGCNT-L	Enables the counter dedicated to addressing the EPROM containing alphanumerics, and also the PROM holding line pattern information. The counter is loaded as a Data Bus Derstination.
58	RSR1-H	See RSR0-H, bit 60.
57	PYCNT-L	Enables the Processor Y Address Counter to increment or decrement, as specified by the PYUP-H control (bit 56).
56	PYUP-H	Controls direction of processor Y count.
55	PXCNT-L	Enables the Processor X Address Counter to increment or decrement, as specified by the PXUP-H control (bit 54).
54	PXUP-H	Controls direction of processor X count.
53	LPEN-L	Enables the Loop Counter, which feeds its most significant bit to the conditional branch circuitry.
52	WALL-H	Commands the circuitry driving the write enable of pixel memory to write 16 consecutive pixels. Used in "Flash Fill".
51	PWR-L	Commands a write of a single pixel at address specified by processor X,Y counters.

2)Data Bus Source and Destinations.

50	DEST4-H	
49	DEST3-H	
48	DEST2-H	These 5 bits specify one of the following
47	DEST1-H	data bus destinations:
46	DEST0-H	

DEST#	DESTINATION
0	No destination (dummy location)
1	Loop Counter
2	Write Data Register
3	Pattern Register
4	Processor X Counter
5	Processor Y Counter
6	Screen X Counter Start Register
7	Zoom Register
8	Screen Y Counter Start Register
9	CRT Controller Read*
10	Reset to I/O board
11	Strobe to I/O board
12	Character Register
13	CRT Controller Write
14	Color Look Up Table Data
15	Diagnostic LEDs
16	Scratchpad RAM Address

	17	Scratchpad RAM Data
	18	Write Mask
	19	Signature Read*
	20	Soft Power Up
	21	Read Mask
	22	Tablet Interface Write
	23	Tablet Interface Read*

*These destination addresses are actually sources. They must be used in conjunction with a dummy source address EXTSRC.

45	SRC2-H	
44	SRC1-H	
43	SRC0-H	These 3 bits specify one of the following data bus sources:

SRC#	SOURCE
0	Not Used.
1	ALU. The 2901 is the source.
2	Ucode. Lower 12 bits of microPROM.
3	Scratchpad RAM
4	Readback Even (8 even numbered pixels)
5	EXTSRC. Dummy source for Read DEST.
6	I/O interface
7	Readback Odd (8 odd numbered pixels)

3) Conditional Branch Control.

42	BR2-H	
41	BR1-H	These 3 bits select the type of branch to
40	BR0-H	occur. R means the contents of the sequencer R Register, D means the contents of the Data Bus. CC2 and CC1 are condition codes explained later. In all cases 2-7 the sequencer simply increments if CC1=0.

BR#	BRANCH TYPE
0	GOTO R+2*CC2+CC1
1	GOTO D+2*CC2+CC1
2	GOTO R if CC1=1
3	GOTO D if CC1=1
4	GOSUB R if CC1=1
5	GOSUB D if CC1=1
6	Not used.
7	RETURN if CC1=1

39	CC22-H	
38	CC21-H	
37	CC20-H	These 3 bits specify CC2 in the above branch type table:

CC2#	CONDITION
0	Loop Counter MSB=1
1	Loop Counter MSB=0
2	Data Bus LSB=0
3	Data Bus LSB=1
4	ALU Carry=1
5	ALU Carry=0

		6	RRC=1. Refer to 2901 manual for details.
		7	RRC=0. " " "
36	CC14-H		If =1, then CC1=1 if the condition selected by
35	CC13-H		CC13, C12, CC11 and CC10 is true. Otherwise,
34	CC12-H		CC1=1 if the condition is false.
33	CC11-H		
32	CC10-H		These 4 bits specify CC1 in the above branch type table:

CC1#	CONDITION
0	Never (used for uncond. branch/rtn)
1	ALU MSB=1 (minus)
2	ALU Carry
3	ALU Overflow
4	ALU Zero
5	Loop Counter MSB=1
6	RRC=1
7	QRC=1
8	LRC=1
9	Data Bus LSB=1
10	DSL=1 (a loopback test line)
11	NCY=1 (nibble carry)
12	Option strap set to 33 Hz.
13	Vertical Blanking
14	I/O Data Accepted
15	Input Data Ready

4) Bit Slice ALU Controls.

31	SH1-H	
30	SH0-H	These two bits specify the value fed to the 2901 during an internal shift of the ALU output prior to register load:

SH#	SHIFT TYPE
0	Shift in 0
1	Shift in 1
2	Rotate end-around
3	Arithmetic shift (preserve sign)

29	I8-H	
28	I7-H	These 3 bits define the ALU Destination
27	I6-H	as described fully in the 2901 manual and abbreviated here:

I#	ALU DESTINATION
0	QREG (Q, Y <-- F)
1	NOP (Y <-- F)
2	RAMA (B <-- F , Y <-- A)
3	RAMF (B, Y <-- F)
4	RAMQD (B <-- F/2, Q <-- Q/2, Y <-- F)
5	RAMD (B <-- F/2, Y <-- F)
6	RAMQU (B <-- 2F, Q <--2Q, Y <-- F)
7	RAMU (B <-- 2F, Y <-- F)

26	I5-H	
25	I4-H	
24	I3-H	These 3 bits specify the ALU operation:

I#	ALU OPERATION

		0	ADD (F <-- R+S)
		1	SUBR (F <-- S-R)
		2	SUBS (F <-- R-S)
		3	OR (F <-- R V S)
		4	AND (F <-- RS)
		5	NOTRS (F <--R'S)
		6	EXOR (F <--R'S V RS')
		7	EXNOR (F <--R'S' V RS)

23	CY-H	Carry in to the ALU. Used for add with increment, subtract with decrement.
22	I2-H	
21	I1-H	
20	I0-H	These bits conrol R and S of the above table:

I#	R	S
0	A	Q
1	A	B
2	0	Q
3	0	B
4	0	A
5	D	A
6	D	Q
7	D	0

19	A3-H	
18	A2-H	
17	A1-H	
16	A0-H	Four bits to select A register
15	B3-H	
14	B2-H	
13	B1-H	
12	B0-H	Four bits to select B register
11	Di1-H	
10	Di0-H	
:	:	
0	D0-H	Twelve bits of microcode constant

**Other Programmed Parts

Ther are 7 other programmed parts in the Omega. In this section, each is functionally described:

1) Character EPROM.
U150
2K X 8

This is a 2716 used to hold the 128 characters each defined within a 16X8 pixel cell. Eight high order bits of address are driven by the Character Register (destination 12). The remaining 4 row bits are driven by the Character Row Counter, which is preset when the Character Register is loaded.

2) Line Pattern
PROM
U149
32 X 8

Contains 8 line patterns, as serial streams on each output. The desired pattern stream is selected by mux and fed to the pixel write circuitry. Addressed by the Character Row Counter, which is shared with Character EPROM.

3) Area Pattern

Contains 8 area stipple patterns, as serial

PROM
U148
512 X 8

streams on each output. The desired output is selected by the same mux (U147) as Line Pattern. Addressed by the Processor Address Counters, using the lower 4 bits of X and Y to yield a 16 X 16 cell for pattern replication.

4) State Machine
PROM
U237
512 X 8

Encoded with 16 states and a state transition algorithm. Inputs and Outputs are:

INPUT	MEANING
PWRUP-L	Power up reset; initializes state machine.
RRASO-L	Force a refresh cyle. Active during certain zoom factors and in Blank mode.
RCYL-H	Full RAS-CAS cycle, caused when DRAM page boundary exceeded. Default is CAS only page mode.
BL-L	Blank. All DRAM cycles given to processor; none to screen.
HSYNC-H	Active during horizontal sync. Used to position RRASO cycles.

OUTPUT	MEANING
A-H B-H	A and B are decoded into one of four conditions:

B	A	Condition
0	0	Refresh Address enable
0	1	Refresh Address enable/count
1	0	Processor Address enable
1	1	Screen Address enable

C-H
D-H

D	C	Present Cycle	Next Cycle
0	0	RAS	CAS
0	1	CAS	CAS
1	0	RAS or CAS	WAIT
1	1	WAIT	RAS or CAS

5) Memory Cycle 1
PAL

This PAL replaces random logic, and has the following inputs and outputs:

INPUTS	MEANING
CLK	18 MHz pixel clock/2
C, D	Next state info (see above)
QC, QD	Present state info (C, D above)
QA, QB	Subcycle time slot counter
DWZ-H	Modulo carry on X zoom counter
WEPP-L	Write pulse command

OUTPUTS	MEANING
RASP-L	RAS pulse to DRAM
ROWEN-L	Enable Row Address to DRAM
CASP-L	CAS pulse to DRAM
COLEN-L	Enable Column Address to DRAM
WEP-H	Qualified write pulse
WEPO-L	Write enable decoder polarity. Used for Write All (WALL).
VSRSO-H	Video Shift Register Control. 1=Load 0=Shift Left or Hold

6) Memory Cycle 2 PAL

This device also replaces random logic.

INPUTS	MEANING
QD-H	Indicates RAS cycle. Used to disable PRCLK during RAS.
QB-H	Source for PRCLK
RSRLD-H	Load of Readback SR; stops PRCLK if attempted during screen cyc.
CMAPLD-L	Color LUT load; stops PRCLK if attempted during screen cycle.
WALL-H	Write All (Flash-fill). Generates the appropriate WEPP-L & WEEN-L.
PRWR-L	Processor Write, from microcode PROM.
BR-L	Breakpoint. Halts PRCLK
CLIP-H	Inhibits write when Pr. Addr. overflow

OUTPUTS	MEANING
WEPP-L	Active during all writes of DRAM.
WEEN-L	Active during single pixel writes. Inactive during WALL cycles.
PRCLKA, B	Processor clocks, parallel drivers
CASMSK-L	Enables write mask for memory write.

7) Branch Control PAL

This device replaces random logic, receiving as inputs the condition code information from microcode and the actual conditions, and generating actual control lines to condition code muxer, the stack control on the 2911/2909, and the OR inputs on the same, used in the 4 Way Branch.

**********TROUBLESHOOTING GUIDE**********

Preliminary Test Procedure:

1. Test equipment required
   - 1.1 Oscilloscope H-P model 1740A or equivalent
   - 1.2 Logic probe H-P model 545A or equivalent
   - 1.3 Multimeter Fluke model 8024B or equivalent
   - 1.4 Freq. countr H-P model 5315A or equivalent(optional)
   - 1.5 Monitor color graghic Hitachi model HM3619AC-XX-X
   - 1.6 Terminal CIT model 101 or equivalent

1.7 DC power supply assembly
1.8 Video cable assembly

2. Visual inspection (pre-test)
   2.1 Visually examine the controller board for obvious solder bridges, component placement, correct mods, latest revision level microcode, pals and character generator.
   2.2 Verify that the D.C. power busses are not shorted by measuring the following points with the multimeter:
      2.2.1 +5VDC TO GROUND 310 OHMS +/-10%.
      2.2.2 -5VDC TO GROUND 1.0 OHMS +/-10%.
      2.2.3 +5VDC TO -5VDC 310 OHMS +/-10%.

3. Functional test procedure
   3.1 Connect the test station D.C. power supplies to the graphics controller.
   3.2 Connect the test station monitor to the graphics controller via the video cable fixture.
   3.3 Inatall an RS232 serial interface to the graphics controller.
   3.4 Turn power on and determine that the controller is passing through the power up dianostic routine by observing the diagnostic leds on the controller board and observing the monitor.
   NOTE: The monitor will be blank(black) while running the power up diagnostic routine(8 to 10 seconds). At the end of diagnostic test the star pattern will appear.
   3.5 When the controller has successfully completed the power up diagnostic routine verify that the following signals are present and are correct.
      3.5.1 36MHZ at U336-14 with a voltage level of 1.5VDC.
      3.5.2 Horizontal sync test point time is 35us.
      3.5.3 Vertical sync test point time is 15ms.
      3.5.4 Composite sync at U239-15 is OVDC to -.8VDC
      3.5.5 Video analog signal at U239-14, U264-15 and U265-15 is OVDC to 1.5VDC.
   3.6 After paragraphs 3.1 through 3.4 have been successfully completed run a minimum of 20 passes of the ctest program from the vax computer.
   3.7 After paragraphs 3.1 through 3.4 have been completed mount the graphics controller to the main structural assembly and begin 100 hour burn-in.

Diagnostic LED Failure Indications:

D5	D6	D7	D8	D9	D10	D11	D12	D13	PROBLEM
							PROCLK		
								HWCLK	
						X			NOT SEQUENCING
					X				2901 PROBLEMS

			X	X	DATA BUS BAD
		X			LOOP CNTR BAD
		X		X	I/O ERROR
		X	X		SCRATCH PAD BAD
		X	X	X	CRT CONTROLLER BAD
	X				WR/RD BACK BAD
	X			X	SIGNATURE BAD
X				X	RAM ERROR ROW 1
X			X		RAM ERROR ROW 2
X			X	X	RAM ERROR ROW 3
X	X	X	X		RAM ERROR ROW E
X	X	X	X	X	RAM ERROR ROW F

D7 indicates ram error and D8 thru D11 indicate which row the failure is on. Furtheremore to find out which page the error is on look at the scratch pad address lines. A0 high indicates page 0 is bad. A1 high indicates page 1 is bad,ect,ect. A7 high indicates page 7 is bad.

D13 should always be on indicating that HWCLK is running.

D12 should always be on indicating that PROCLK is running.

1) OMEGA 420 4 BIT PLANE

2) OMEGA 440 8 BIT PLANE

The basic difference between the 420 and the 440 is on the 420, rams (U125 TO U140, U157 TO U172, U177 TO U192, U209 TO U224) are not stuffed. Blink is then tied to U91 and U109. On the 420 sixteen colors can be put on the screen at one time. The 440 can put up 256 colors at one time.

The built in self test starts on power up for the 420 and the 440. The leds get you started in the right direction. D12 is HWCLK and D13 is PROCCLK. If these leds are off the the problem is in the clock circuit. However, if the -5 volts is not present these leds will be off also.

If the unit runs self test properly all the leds will activate including the ready led on the front panel. The self test checks the signature on the star pattern, which is stored in the proms, if the same signature turns on the ready led. If different will not turn on the ready led, however programs can

still be executed.

DATA LINE PROBLEMS

The self test counts up the data bus. If two data lines are shorted together, or shorted to ground or +5 volts, or two devices driving the data bus at the same time leds D10 and D11 will be set on.

LOOP CNTR BAD

Self test counts down loop counter and checks the signal LPCNTCRYH. possible cause U114,U115,U116. Led D9 will be turned on.

I/O ERROR

An i/o board has to be connected to the omega board to run through self test and to even come up. On parallel board units the host computer has to be on and connected to the parallel board with ribbon cable connected properly. The micro code will loop sending 0,1's to the i/o board and then read them back. Signals involved are ODATHLDENL, ODATACCH, IDATSTBH, CLIDRDYH, IDRDYH, IDATACCH, ODATSTBH, ODATRDYH, SODRDYH, IDATHRDENL. Most likely cause would be i/o board. Check that ODATSTBH and IDATSTBH pulse during i/o self test. Leds D9 and D11 will be on. MAKE SURE ALL SWITCHES (IF ANY) ARE SET CORRECTLY.

SCRATCH PAD BAD

Scratch pad test loops passing address to data and then writes. Then address 1 contains data 1, add. 2 con. data 2 ect,ect. It then reads back. If an error omega hangs. If passes, the data is complemented, written, and then checked. Scratch pad rams are U342, U341, U340. Signals involved are SPRAMDATL , SPRAMRDL , address and data lines. Leds D9 and D10 will be on.

CRT CONTROLLER BAD

Self test for crt controller is obsolete. Horiz. sync is 35u sec. and is on U318 pin 39, U319 pin 7, and U292 pins 10 and 11. Vert. sync is 15m sec. and is on U318 pin 40, U319 pin 4, U292 pins 13 and 12. Chips involved are U291, U318, and U319.

WR/RD BACK ERROR

Here you are writing to memory and then reading it back, through the read back shift registors (not signature) If they dont match you get and error. Possible cause of this error is output of two rams shorted together, WE shorted together, RAS or CAS bad, shift registor bad. Led D8 will be on. A good place to start looking is on the read back shift registors.

SIGNATURE BAD

This part of self test puts up the star pattern and checks

the signature. If it does not match the sig. in prom (known good sig.) leds D8 and D11 will be on. Possible problem bad ram or whole bank of rams, signature hardware bad, color map bad, pan and zoom possibly bad. Most of the time you will see something wrong on the screen.

RAM ERROR

If led D7 lights up there is a ram error. The combination of leds (D8 thru D11) indicate the row in which the error occured. Furthermore the address lines on the scratch pad rams indicate which back of rams is failing. Here is a chart to go by.

LEDS

D7	D8	D9	D10	D11		RAMS INVOLVED IN BAD ROW
X					ROW 0	U18, 49, 77, 108, 140, 172, 192, 224
X				X	ROW 1	U17, 48, 76, 107, 139, 171, 191, 223
X			X		ROW 2	U16, 47, 75, 106, 138, 170, 190, 222
X			X	X	ROW 3	U15, 46, 74, 105, 137, 169, 189, 221
X		X			ROW 4	U14, 45, 73, 104, 136, 168, 188, 220
X		X		X	ROW 5	U13, 44, 72, 103, 135, 167, 187, 219
X		X	X		ROW 6	U12, 43, 71, 102, 134, 166, 186, 218
X		X	X	X	ROW 7	U11, 42, 70, 101, 133, 165, 185, 217
X	X				ROW 8	U10, 41, 69, 100, 132, 164, 184, 216
X	X			X	ROW 9	U9 , 40, 68, 99 , 131, 163, 183, 215
X	X		X		ROW 10	U8 , 39, 67, 98 , 130, 162, 182, 214
X	X		X	X	ROW 11	U7 , 38, 66, 97 , 129, 161, 181, 213
X	X	X			ROW 12	U6 , 37, 65, 96 , 128, 160, 180, 212
X	X	X		X	ROW 13	U5 , 36, 64, 95 , 127, 159, 179, 211
X	X	X	X		ROW 14	U4 , 35, 63, 94 , 126, 158, 178, 210
X	X	X	X	X	ROW 15	U3 , 34, 62, 93 , 125, 157, 177, 209

SCRATCH PAD ADD.

A0 U341PIN5 HIGH INDICATES BAD RAM (U3 THRU U18)
A1 U341PIN6 HIGH INDICATES BAD RAM (U34 THRU U49)
A2 U341PIN7 HIGH INDICATES BAD RAM (U62 THRU U77)
A3 U341PIN4 HIGH INDICATES BAD RAM (U93 THRU U108)
A4 U341PIN3 HIGH INDICATES BAD RAM (U125 THRU U140)
A5 U341PIN2 HIGH INDICATES BAD RAM (U157 THRU U172)
A6 U341PIN1 HIGH INDICATES BAD RAM (U177 THRU U192)
A7 U341PIN17HIGH INDICATES BAD RAM (U209 THRU U224)

With this matrix you can find which ram is bad. If more then one scratch pad address is high the possible problem is in the control lines, such as address lines, write, enable, ras, and cas.

FIELD SERVICE TROUBLE-SHOOTING GUIDE

RS232 INTERFACE:

With a RS232 interface the display controller should go through it's self test and come up with the readu

led on, with no computer line hooked up.

If leds indicate i/o problem (D9 and D11 on and all others off except clock leds D12 PROCLK & D13 HWCLK)
POSSIBLE PROBLEMS:
1)Check that RS232 board is plugged in all the way.
2)Most likely cause would be RS232 board.
3)The least likely would be the omega board.

Swap RS232 board out to determine which board is bad. If the RS232 is bad check,
1)Clocks to Z80 (U10 pin 6)
2)PROCLK (U13 pin 3)
3)Data bus for shorts

During self test the 2901 writes a byte (O'S) out to the RS232 board and then reads it back. If the data read back is different, Z80 is not running, or hand-shake is bad the omega will hang at an i/o error.

On the next page is a timing diagram for the omega i/o (RS232) self test.

If the omega goes through its self test but does not receive date then check
1) Baud rate switches (for the correct position)
2) Check RS232 cable to host (correctly installed)
3) Check input receiver U5 (26LS33)

FIELD SERVICE TROUBLE-SHOOTING GUIDE

PARALLEL INTERFACE

Parallel interface units need a host computer hooked up in order to go through self test. The cables have to be hooked up properly also. If the cables are not hooked up, the omega board will hang at an i/o error.

On the parallel board, J1 is the 16 bit parallel into omega, J2 is the 16 bit parallel out to the host.

J3 is the 16 bit DMA into omega, and J4 is the 16 bit DMA out to the host.

If leds on the omega indicate i/o problem (D9 and D11 on), and all others off except clock leds (D12 PROCLK & D13 HWCLK), then check for these possible problems.

1) Parallel board not plugged in all the way
2) Host cables not correctly installed to omega
3) Parallel board itself
4) omega board

The reason the omega board will not come up with host cables not installed is J3 pin 1 will be floating causing U10 to be disabled. Furthermore J1 pin 40 (NEWDATARDY) and J2 pin 3 (DATATRANS) will be floating causing U2 pin 12 (IDATSTBH) to be low and U4 pin 11 (ODATSTBH) to be low which are the hand shake signals.

During self test the 2901 writes a byte of (0's) and then a byte of (1's) out to the parallel board, then reads them back. If the hand-shake or data read back is bad, the omega will hang at i/o error.

On the next page is a timing diagram for the parallel board read and write.

If the omega passes self test, but the opcodes operate wrong the possible problem would be the input section from the host. U11, U12, U13, U14, U15, and U16 would be the suspect components.

**********PARTS LIST**********

Bill of material graphic controller omega 440 10 june, 1982

revision #__8 11 nov., 1982

Part no.	Description	use	pull
86-00005-00	printed circuict board, graphics controller	1	
49-00341-00	choke, .33uh, dale type ir2	1	
33-00148-00	connector, molex #09-18-5094	1	
33-00159-00	connector, berg header, #65499-136	35	
33-00136-00	connector, sealectro #51-051-0000	3	
33-00138-00	connector, viking #1mr01vh18e01	1	
32-00114-00	connector, 16 pin dip, augat #c7216-59	1	
32-00119-00	connector, 20 pin dip, augat #c7220-59	5	
32-00121-00	connector, 24 pin dip, augat #c7224-59	9	
26-00414-00	led type t1 3/4, dialight #521-9246(red)	1	
26-00415-00	led, , dialight #550-0204 (green)	1	
26-00416-00	led, , dialight #550-0404 (red)	8	
26-00422-00	diode, type in914	3	
22-00425-00	voltage regulator, type lm336bz-2.5	1	
28-00426-00	transistor, type 2n3904	1	
28-00427-00	transistor, type 2n3906	3	
20-00295-00	integrated circuict, type 74s04	1	
20-00281-00	" " " 74s157	2	
20-00279-00	" " " 74s163	1	
20-00278-00	" " " 74s182	1	
20-00272-00	" " " 74s251	3	
20-00269-00	" " " 74s374	3	
22-00763-00	" " " 74f151	1	
22-00519-00	" " " 74f158	3	
19-00268-00	" " " 74ls00	2	
19-00267-00	" " " 74ls02	3	
19-00266-00	" " " 74ls04	4	
19-00265-00	" " " 74ls08	3	
19-00259-00	" " " 74ls27	1	
19-00257-00	" " " 74ls32	1	
19-00255-00	" " " 74ls40	1	
19-00253-00	" " " 74ls74	5	
19-00251-00	" " " 74ls123	1	
19-00248-00	" " " 74ls138	4	

19-00247-00	"	"	74ls139	1
19-00239-00	"	"	74ls669	7
19-00238-00	"	"	74ls240	1
19-00237-00	"	"	74ls241	1
19-00236-00	"	"	74ls244	4
19-00235-00	"	"	74ls245	3
19-00234-00	"	"	74ls253	2
19-00229-00	"	"	74ls299	33
19-00228-00	"	"	74ls374	2
19-00227-00	"	"	74ls377	17
19-00226-00	"	"	74ls393	2
22-00224-00	"	"	10102	5
22-00222-00	"	"	10104	4
22-00221-00	"	"	10113	4
22-00220-00	"	"	10124	12
22-00219-00	"	"	10125	3
22-00218-00	"	"	10131	2
22-00217-00	"	"	10133	2
22-00216-00	"	"	10136	4
22-00215-00	"	"	10141	4
22-00214-00	"	(FAIRCHILD)	10145a	2
22-00213-00	"	"	10153	4
22-00839-00	"	"	10h158	1
22-00211-00	"	"	10176	9
22-00210-00	"	"	10188	1
22-00209-00	"	"	10318	3
22-00208-00	"	"	10422	6
22-00207-00	"	"	am2901b	3
22-00206-00	"	"	am2909a	1
22-00205-00	"	"	am2911a	2
22-00203-00	"	"	am2966	3
22-00186-00	"	"	am9114c	3
22-00199-00	"	"	hd46505sp-1	1
22-00197-00	"	"	hd4864-2	128
19-00196-00	"	"	am25ls2538	2
19-00195-00	"	"	am25ls2569	10
19-00184-00	"	"	am25ls2520	1
17-00391-00	capacitor, 15pf, mono, #sga-q15			1
17-00388-00	capacitor, 270pf, mono, #dd271			2
17-00383-00	capacitor, .1uf, mono, #2c52u104x9100c4			3
17-00380-00	capacitor, .1uf, dip, avx #md015c104kaa			252
17-00381-00	capacitor, .01uf, mon, #1c25u103x9100c4			3
17-00378-00	capacitor, .001uf, mono, type 5ga-d10			1
17-00374-00	capacitor, 100uf, elect, #503d107f016nb			2
10-00474-00	resistor, 100ohm, 1/4w, 5%, composition			1
10-00472-00	resistor, 1k ohm, 1/w, 5%, composition			35
10-00470-00	resistor, 150 ohm, 1/4w, 5%, composition			2
10-00469-00	resistor, 1.5kohm, 1/4w, 5%, composition			6
10-00467-00	resistor, 22 ohm. 1/4w, 5%, composition			3
10-00464-00	resistor, 240 ohm, 1/4w, 5%, composition			1
10-00460-00	resistor, 390 ohm, 1/4w, 5%, composition			1
10-00459-00	resistor, 470 ohm, 1/4w, 5%, composition			3
10-00458-00	resistor, 4.7kohm, 1/4w, 5%, composition			2
09-00456-00	resistor, 75 ohm, 1/4w, 1%, metal film			3
08-00441-00	resistor, sip, 75ohm, msp08c05-r121/195			43
08-00435-00	resistor, sip, 33ohm, msp08a03-330g			4
08-00434-00	resistor, sip, 330ohm, #msp10a01-331g			1
08-00431-00	resistor, sip, 4.7k , #msp10a01-472g			1
27-00413-00	crystal, 72.44mhz, type hc18/u			1
01-00794-00	double faced foam tape, .3" wide			a/r

1. revision 1 adds one 158-0101-00 i.c. 10101 quant from 1 to 2.
2. revision 2 changes 33 ohm resistor pack from msp08a01 to msp08a03

3. revision 3 deletes 200 ohm resistor, adds 2-4.7k resistors and changes quantity of 1k resistor from 37 to 35.
4. revision 4 changes the burg header count from 29 to 33, changes .1uf capacitor from monolythic to avx type and changes count from 256 to 255, deletes one 100uf from three to two, adds one 240 ohm resistor and deletes one 470 ohm resistor.
5. revision 5 changes quantity of .1uf cap #281-0001-01 from 1 to 3.
6. revision 6 changes 10158 to 10h158.
7. revision 7 changes 74s158 to 74f158 and 74s157 to 74f157.
8. revision 8 deletes remaining 100uf cap and 220 ohm resistor