REV	EO	DESCRIPTION	DWN	CHKD	APPD	DATE
A	4513	NEW RELEASE	J.C.C.	RH	[illegible]	2/16/76

CURRENT REV.	A	A	A	A	A	A	A		
SHEET NO.	19	20	21	22	23	24	25		
CURRENT REV.	A	A	A	A	A	A	A	A	A
SHEET NO.	10	11	12	13	14	15	16	17	18
CURRENT REV.	A	A	A	A	A	A	A	A	A
SHEET NO.	1	2	3	4	5	6	7	8	9

UNINCORPORATED ENGINEERING ORDERS	

	DATE
PREPARED J.H.Hookum	5/5/75
CHECKER [illegible]	2/6/76
ENGINEER [illegible]	2/12/76
APPD D Savitt	2/13/76
APPD [illegible]	2-12-76
APPD L. Brook	2/16/76
RECORDS M. Riddell	2/17/76

TITLE

3200 MAGNETIC TAPE CONTROLLER

Microdata
IRVINE, CALIFORNIA

A	FS2000320	A
IDENT CODE 52936	DWG SIZE	SHEET 1 OF 25 REV

Form 3-132-1

TABLE OF CONTENTS

Table of Contents (cont'd)

FIGURES

1.0 GENERAL DESCRIPTION

1.1 Peripheral Device

The 3200 Magnetic Tape Controller is designed to interface the Microdata Series 6000 and 7000 tape transports, using Model 6923 NRZI, or Model 6922 Phase-Encoded (PE) Formatters. Up to two formatters, each controlling up to four tape transports, may be connected to the controller.

1.2 Type of I/O

The magnetic tape controller accepts orders and sends status information to the 3200 computer through the various fields of the Device Register Block (DRB). All data transfer is performed by Direct Memory Access (DMA).

1.3 System Characteristics

The 3200 Magnetic Tape Controller is designed to support up to eight tape transports allowing precise control of tape motion while requiring no program intervention for data transfer. All error generation and checking is accomplished with hardware, and detailed status information on each transport is available.

On a read operation, if the record is longer than the byte count, only the number of bytes specified is transferred to memory. Error checking is still carried out as usual, and a 'read data too long' flag is set.

The ending of a transfer between tape drive and memory is reported by either checking status, or if enabled by the program, an interrupt occurs. Although the controller can support only one data transfer operation at a time, any number of drives may be rewinding simultaneously.

The controller permits response to a special "Initial Program Load" (IPL) command which initiates "Cold Start" program loading. Thus, with the IPL command, the first record of tape unit 0, formatter 0 will be automatically read into memory starting at address 0 and continuing until the complete record is loaded. The IPL command is initiated by the LOAD switch on the system front panel and is routed to the Magnetic Tape Controller via the CPU logic.

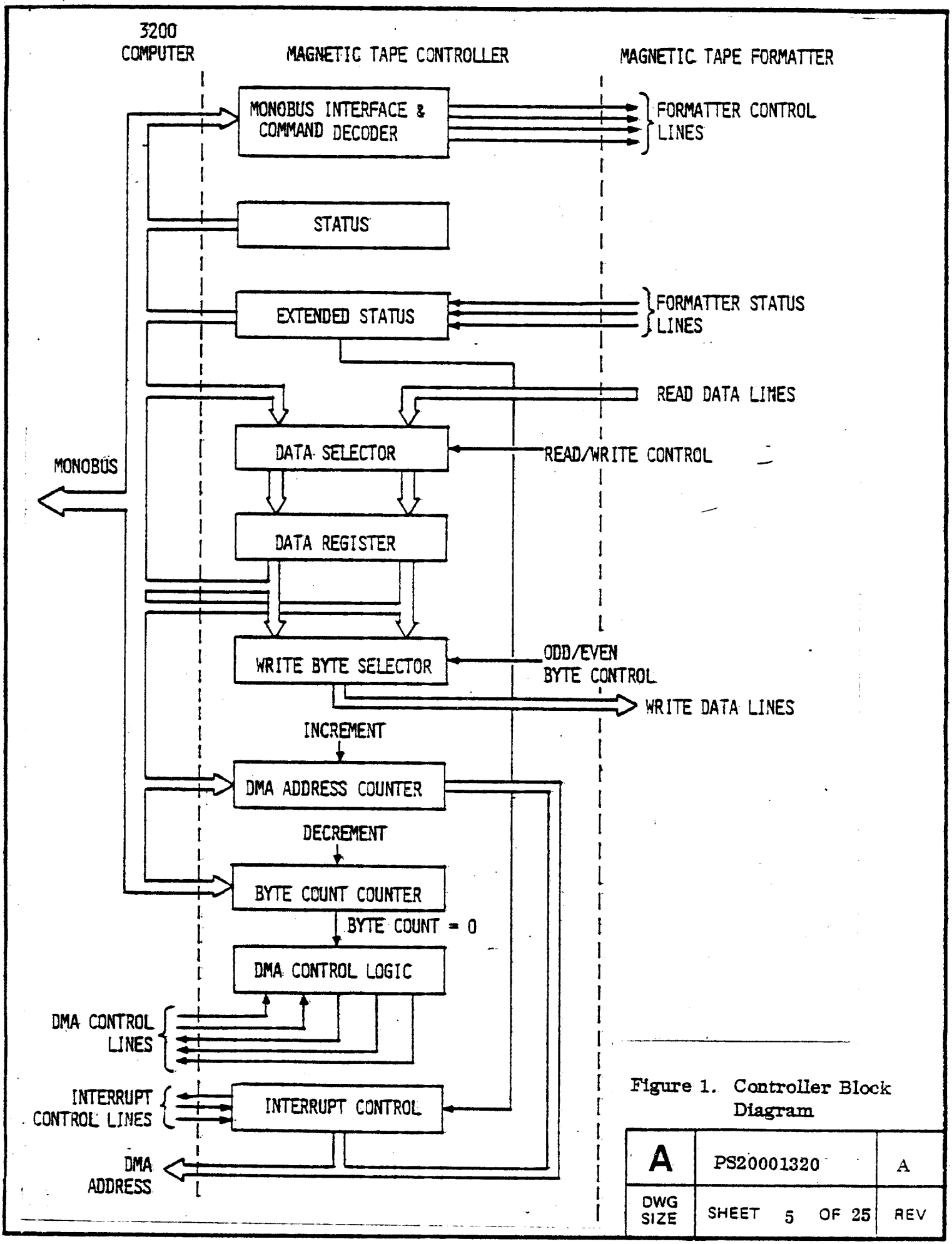


Figure 1. Controller Block Diagram

A	PS20001320	A
DWG SIZE	SHEET 5 OF 25	REV

Form 3-132-2

2.0 FUNCTIONAL DESCRIPTION

2.1 Functional Block Diagram

Figure 1 is a functional block diagram of the magnetic tape controller. The function of each section is briefly described below.

2.1.1 Monobus Interface and Command Decode Section

This section decodes the particular DRB word being accessed by the computer. If it is a storing operation, the decoding generates control signals to appropriate elements of the controller and the information contained in the data lines is stored in registers. If it is a read operation, the controller will place the selected DRB word on the Monobus data lines.

2.1.2 Status and Extended Status

These sections contain the status of both the controller and magnetic tape system at all times.

2.1.3 Data Selector

Selects the data to be routed to the Data Register during data transfer operations. For tape write operations, the information on the Monobus data lines is routed to the Data Register. During tape read operations the read data lines from the formatter are routed to the Data Register.

2.1.4 Data Register

This is a 16-bit register which contains the data being transferred to or from the magnetic tape system. During tape write operation this data is routed to the Write Byte Selector whose function is described below. During tape read operations the information on the 8 Read Data lines from the formatter is stored in the Data Register. The controller packs two 8-bit bytes into the Data Register before it makes a DMA input request. At that time the information contained in the Data Register is placed on the Monobus data lines.

2.1.5 Write Byte Selector

This section is active only during tape unit operations and selects the appropriate half of the Data Register to be placed on the Write Data lines. The most significant half (bits 15-8 of the Data Register) is selected first and the least significant half (bits 7-0) selected second.

2.1.6 DMA Address Counter

This counter contains the address of the next 16-bit data word to be transferred to or from the computer. This counter is loaded by the program prior to data transfer initiation. Once the data transfer commences, the counter is automatically incremented by the controller with each byte transferred.

2.1.7 Byte Count Counter

This counter is loaded by the program prior to data transfer initiation and controls the size of the data record. The counter is decremented with each byte transferred. Data transfer stops when the byte count reaches zero or when the inter-record gap is detected by the formatter during a tape read operation.

2.1.8 DMA Control Logic

This section controls the generation of Monobus requests, data routing and address enabling for transfer of data to and from the computer.

2.1.9 Interrupt Control

This section controls the generation of three types of interrupts, provided the interrupts are enabled. The Special Interrupt is generated as a response to a Set Special Interrupt order. The Status Change interrupt occurs when the status of a tape unit changes from On-line to Off-line, Off-line to On-line, or rewinding to not rewinding. The Termination Interrupt occurs at the end of any tape operation or after a stop controller order is issued by the program.

2.2 Interface Specifications

2.2.1 Interface Drivers/Receivers

All interface signals are low true. The approximate logic levels are:

+3V = False
0V = True

The controller uses 7416 and 7438 drivers for generating the signals to the controller. Each line from the formatter is terminated at the controller end with a 220-330$_\Omega$ resistor network.

Figure 2 shows the typical connection of interface lines.

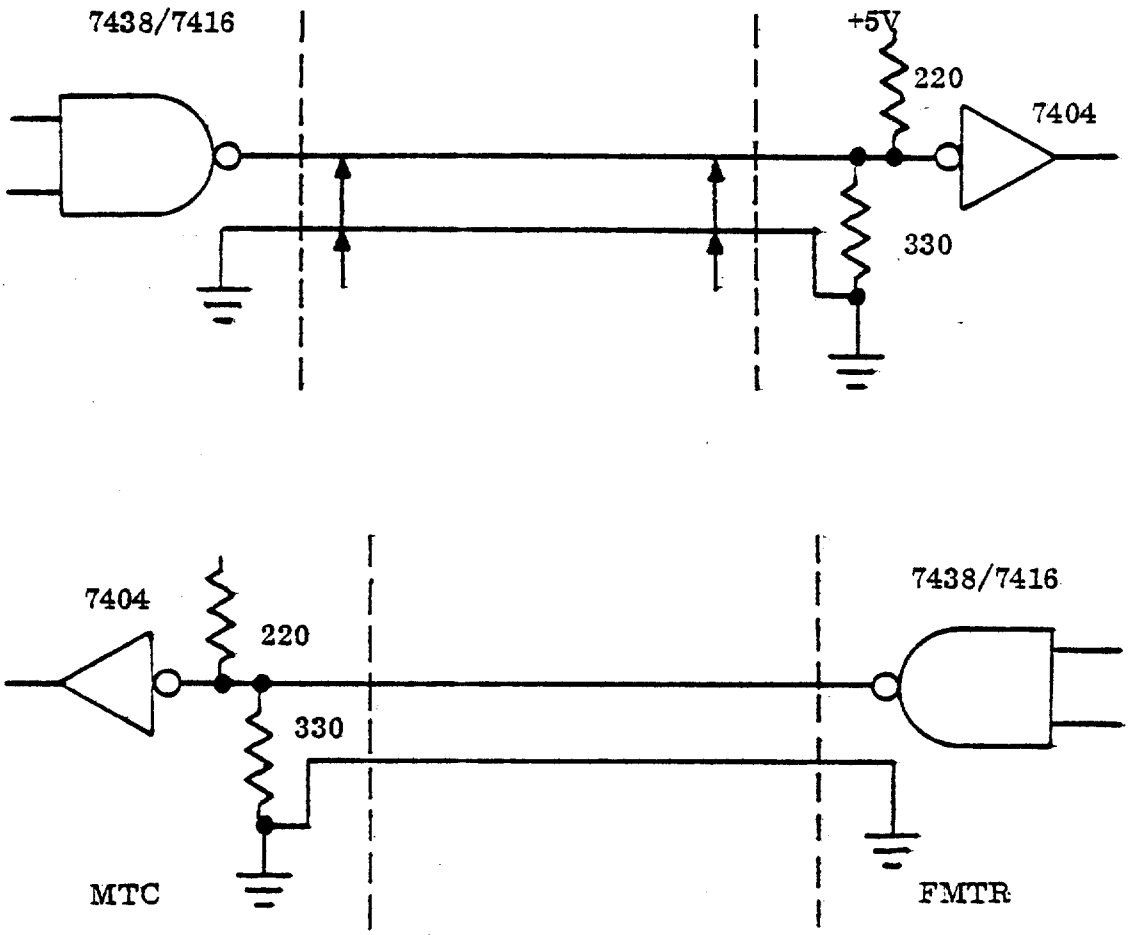


Figure 2. Typical Controller-Formatter Interface Electronics

2.2.2 Controller-Formatter Interface Lines

Controller Interface Connector J1 Pin No.	Signal Name	Formatter Interface Connector J105* Pin No.
1	Formatter Address	B1
2	Transport Address 0	A1
3	Transport Address 1	B3
4	Initiate Command	A3
6	Write/Read	A4
7	Reverse/Forward	B4
8	Edit	A6
9	Write File Mark	B6
11	Erase	B7
12	Off Line	A12
13	Parity	B10
14	Formatter Enable	A13
15	Rewind	B12
17	Last Byte	B13
18	Write Data 1	A16
19	Write Data 0	B16
20	Write Data 3	A18
21	Write Data 2	B18
22	Write Data 5	A19
23	Write Data 4	B19
24	Write Data 7	A21
25	Write Data 6	B21
27	Formatter Busy	B22
28	Hard Error/NRZI Read Error	A24
29	PE ID Burst/Gap Detected	B24
30	File Mark	A25
31	Soft Error	B25
32	On Line	A27
34	File Protect	A28
35	Rewinding	B28
36	End of Tape	A30
37	Load Point	B30
38	NRZI Out	A31
39	7-Track	B33
40	Write Strobe	A34
41	Read Strobe	B36
43	Read 0	B37
44	Read 1	A37
45	Read 2	B39
46	Read 3	A39
47	Read 4	B40
48	Read 5	A40
49	Read 6	B42
50	Read 7	A42

*Consult Formatter Product Specification for capability/functions, i.e., Edit, Erase, Read Backward, etc.

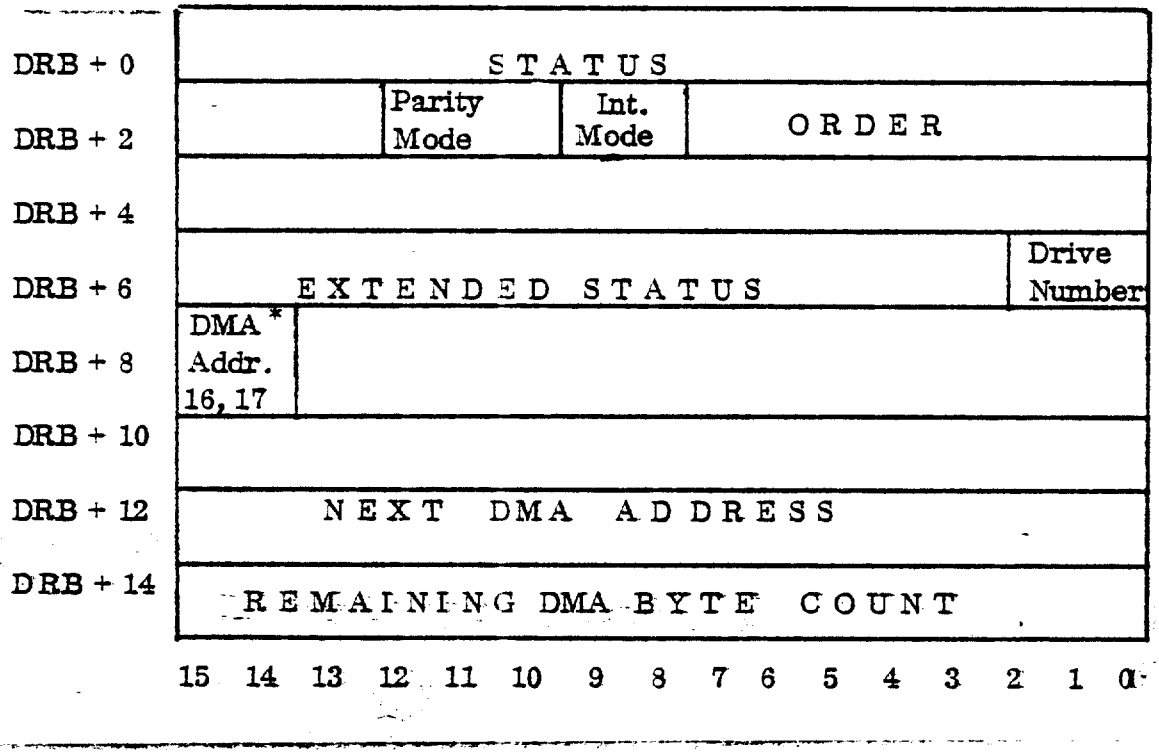
3.0 PROGRAMMING AND USE

The operation of the tape controller requires that certain information be stored in controller registers to enable DMA operation to proceed without program intervention.

3.1 Device Register Block (DRB)

The DRB consists of a group of registers physically located in the tape controller which is accessible by the programmer for the purpose of transferring control information to the tape controller and sampling status from it. Data transfer to or from tape drive is accomplished by Direct Memory Access (DMA).

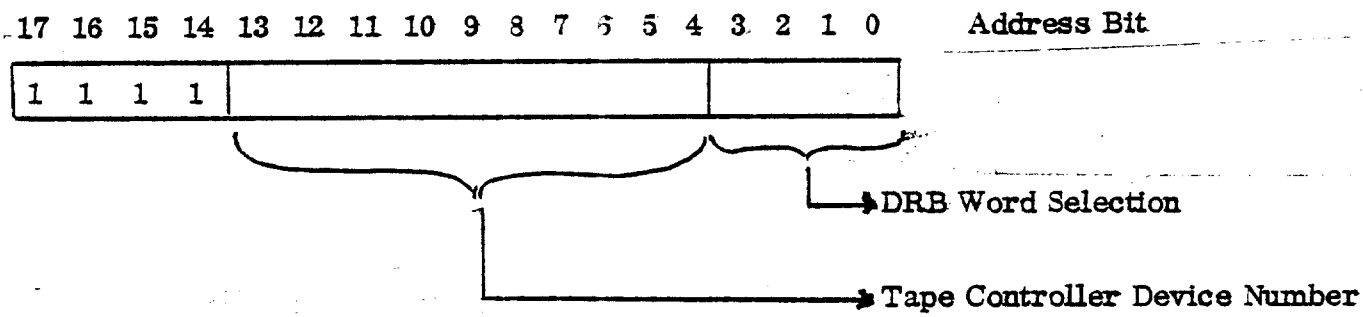
The DRB for the tape controller is shown in Figure 3.



*Address Bits 16 and 17 are set to zero only during IPL action.

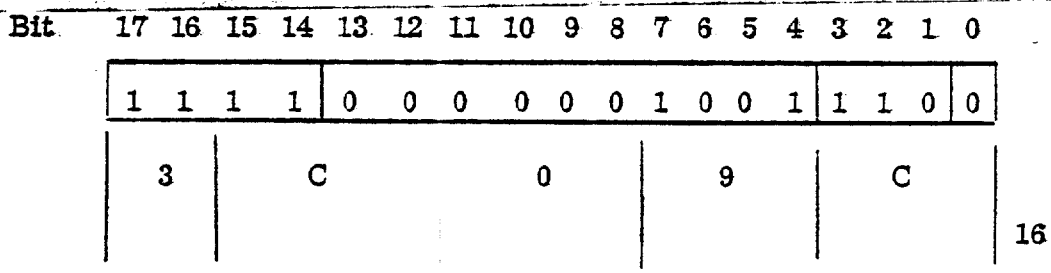
Figure 3. DRB for Tape Controller

Each register is accessed by a Monobus address which is formed by the DRB base address plus a displacement. The DRB base address is formed as follows:



Example:

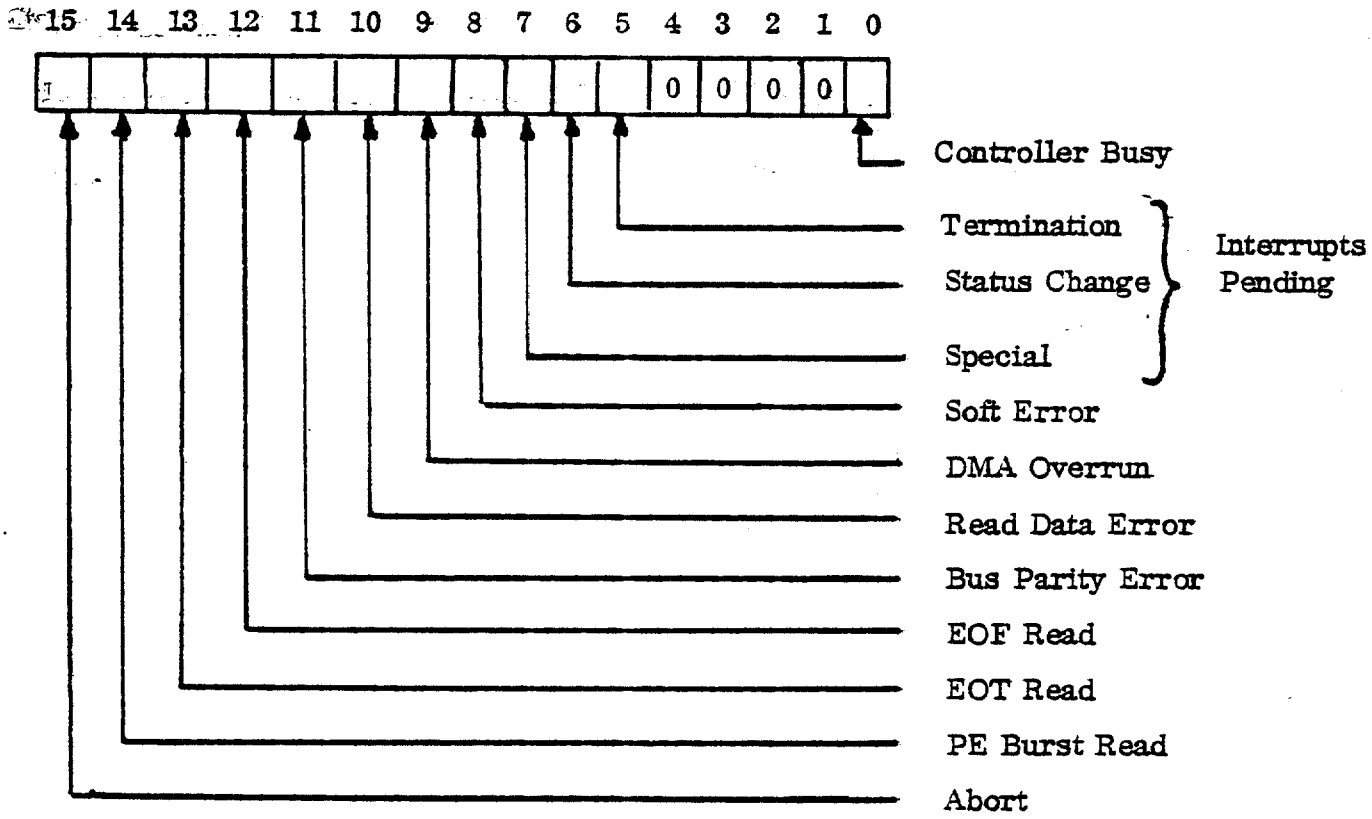
If the tape controller device address is set to 9, the Monobus address would show "Next DMA Address" as:



A	PS20001320	A
DWG SIZE	SHEET 11 OF 25	REV

FORM 3-132-2

3.1.1 Status Field (DRB + 0) - All status bits are set to zero by the action of System Reset DRB+0 and DRB+6.



1: True Condition
0: False Condition

Bit 0: Controller Busy

1: Indicates that the controller is performing a "Select Order" (refer to Order Field DRB+2) or is doing an IPL. The controller does not remain busy during rewind.

0: Indicates that the controller is in its REST state and is ready to accept orders. In the REST state the controller is continuously scanning all units for status changes.

The controller enters the REST state when one of these conditions occurs:

a. The controller has completed the specified operation.

b. An abort condition is present (see bit 15).

c. A "Stop Controller" order has been executed.

Bit 5: Termination

1: Indicates that the controller has gone from the BUSY state to the REST state (see bit 0). If interrupts are enabled by the program an interrupt will occur.

0: The termination bit is reset by sending an "Acknowledge Interrupt" order (refer to Order Field DRB+2) with bit 5 ON to the controller.

Bit 6: Status Change

1: This bit is set when a transport goes from online to offline, from offline to online, or from rewinding to not rewinding. If interrupts are enabled, this condition will cause an interrupt and the drive number will be displayed in DRB+6. Changes are not detected when the controller is busy or waiting for interrupt acknowledge.

0: This bit is reset by sending an "Acknowledge Interrupt" order with bit 6 ON to the controller.

Bit 7: Special

1: This bit is set by sending a "Set Special Interrupt" order (refer to Order Field DRB+2) to the controller. If interrupts are enabled, this condition will cause an interrupt.

0: This bit is reset by sending an "Acknowledge Interrupt" order with bit 7 ON to the controller.

Bit 8: Soft Error

1: The Phase Encoded Formatter has attempted to correct a one bit error on the tape.

0: This bit is reset by any order that sets Controller Busy (bit 0).

Bit 9: DMA Overrun

1: The controller has not been able to access memory in time to service the tape unit.

0: Reset by any order that sets Controller Busy.

Bit 10: Read Data Error

1: An uncorrectable check code error has occurred while reading or writing tape.

0: Reset by any order that sets Controller Busy.

Bit 11: Bus Parity Error

1: A parity error has occurred on the Monobus while reading data from main memory.

0: Reset by any order that sets Controller Busy.

Bit 12: EOF Read

1: The last operation resulted in reading a Filemark on tape.

0: Reset by any order that sets Controller Busy.

Bit 13: EOT Read

1: The last operation resulted in detection of the EOT (End of Tape).

0: Reset by any order that sets Controller Busy.

Bit 14: PE Burst Read

1: The first read operation on a Phase-Encoded Tape resulted in passing over the special PE identification burst.

0: Reset by any order that sets Controller Busy.

Bit 15: Abort

1: The last attempted operation was terminated by one of the following conditions:

a. Device not Online.

b. Device rewinding.

c. Online status lost during operation.

d. Write operation tried on File Protected device.

e. Backspace or Read Backward reached Load Point.

f. "Sense" select order on File Protected device. The sense is still completed.

g. Forward command at EOT.

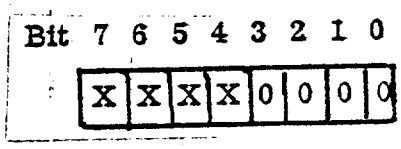
0: Reset by any order that sets Controller Busy.

3.1.2 Order Field (DRB+2, bits 7-0)

This field is used to activate the controller. The program writes information into this field which is decoded by the tape controller and causes it to perform various activities.

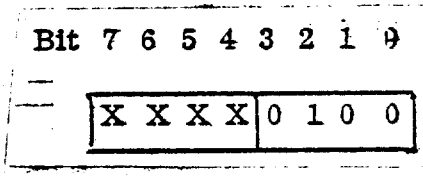
If bit 0 is set, it is a "select" order, bits 3-1 name the unit, and bits 7-4 define the function to be performed. If bit 0 is not set, it is a "controller" order and bits 3-1 define the order. Bits 7-4 are used in the "Acknowledge Interrupts" order. (NOTE: X is a 0 or 1.)

3.1.2.1 No Operation



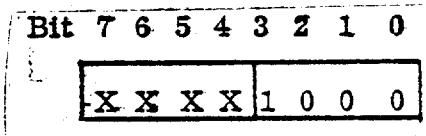
This order has no effect on the operation of the tape controller.

3.1.2.2 Stop Controller



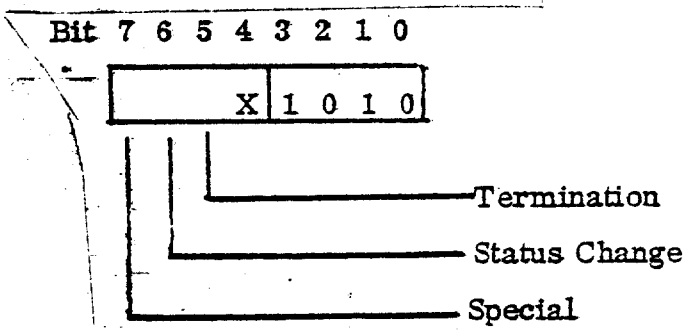
This order causes the controller to return to its REST state.

3.1.2.3 Set Special Interrupt



This order turns ON bit 7 of the status field, and IF interrupts are enabled, it will cause an interrupt.

3.1.2.4 Acknowledge Interrupts



This order causes the removal of the interrupt conditions.

Bit 5:

1: Resets termination bit (bit 5, Status Field)

0: No change.

Bit 6:

1: Resets Status Change bit (bit 6, Status Field)

0: No change.

Bit 7:

1: Resets Special bit (bit 7, Status Field)

0: No change.

3.1.2.5 Initial Program Load

Bit	7	6	5	4	3	2	1	0
	X	X	X	X	1	1	0	0

This order instructs the controller to read the first record of unit 0, formatter 0 into memory starting at address 0.

3.1.2.6 Select Orders

The functions described below may be modified by the capabilities of the formatter used with this controller.

Select Unit 0	X	X	X	X	0	0	0	1
1	X	X	X	X	0	0	1	1
2	X	X	X	X	0	1	0	1
3	X	X	X	X	0	1	1	1
4	X	X	X	X	1	0	0	1
5	X	X	X	X	1	0	1	1
6	X	X	X	X	1	1	0	1
7	X	X	X	X	1	1	1	1

3.1.2.6.1 Read

0 0 0 0	1

Read a record on the selected unit.

3.1.2.6.2 Sense

0 0 0 1	1

Display the extended status of the selected unit in DRB+6.

3.1.2.6.3 Read Backward

0 0 1 0	1

Read a record in reverse direction.

3.1.2.6.4 Backspace/Edit

0 0 1 1	1

3.1.2.6.5 Backspace Record

0 1 0 0	1

3.1.2.6.6 Backspace File

0 1 0 1	1

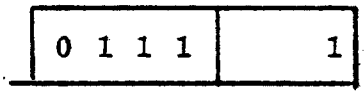
Backspace until a File mark is read.

3.1.2.6.7 Forward Space Record

0 1 1 0	1

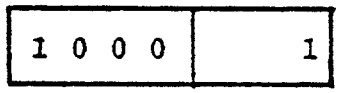
Forward space one record.

3.1.2.6.8 Forward Space File



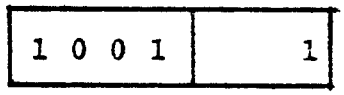
Forward space until a File mark is read.

3.1.2.6.9 Write



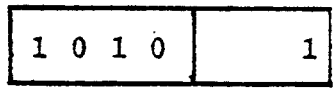
Write a record from memory to tape.

3.1.2.6.10 Erase



Erase three inches of tape.

3.1.2.6.11 Write EOF

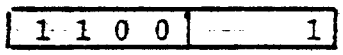


Write a File mark.

3.1.2.6.12 Write/Edit

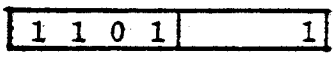
Used in conjunction with Backspace/Edit in overwriting a record.

3.1.2.6.13 Rewind



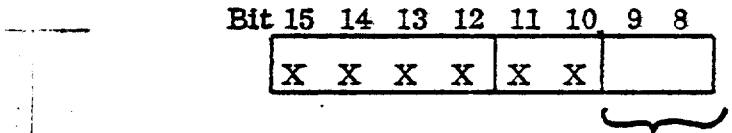
Do high speed rewind to load point.
The controller goes not busy immediately after the rewind is started.

3.1.2.6.14 Rewind and Disconnect



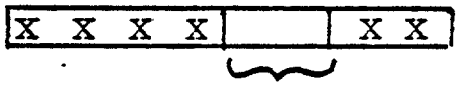
Do high speed rewind and place unit off-line.

3.1.3 Interrupt Mode Field (DRB + 2, Bits 9-8)



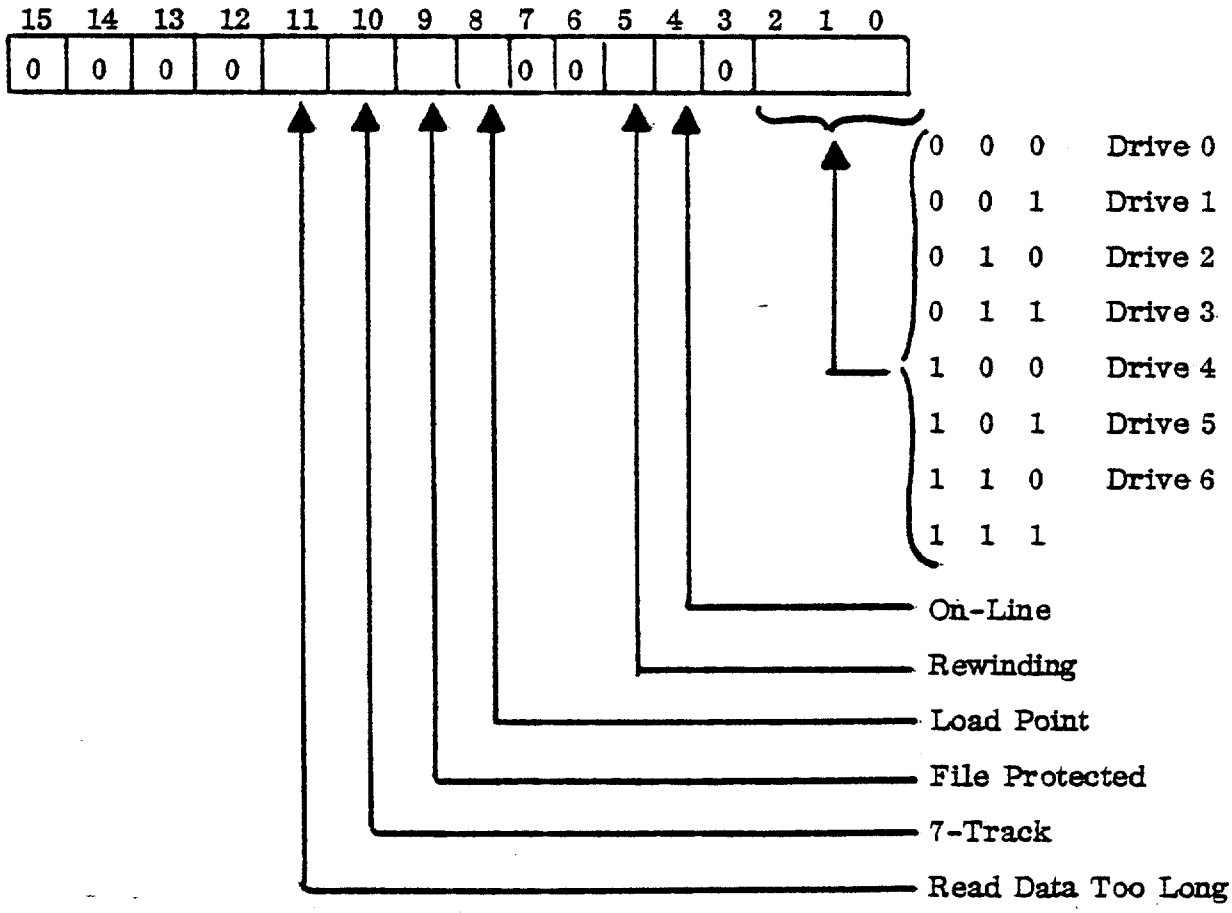
Do not change mode	0 0
Enable Interrupts	0 1
Disable Interrupts	1 0
Not used	1 1

3.1.4 Parity Mode Field (DRB + 2, Bits 9-8)



Do not change mode	0 0
Generate/check odd parity	0 1
Generate/check even parity	1 0
Not used.	1 1

3.1.5 Extended Status Field (DRB + 6)



3.1.5.1 Bits 2-0: Drive Number

These bits identify the drive with which the controller is communicating while a select order is being performed, or the drive that is causing an interrupt, if interrupts are enabled. Also, the "Sense" select order will set this number. The status bits in DRB + 6 reflect the status of the drive whose number is in this field.

3.1.5.2 Bit 4: On-Line

The selected unit is on-line.

3.1.5.3 Bit 5: Rewinding

The selected unit is performing a high-speed rewind.

3.1.5.4 Bit 8: Load Point

The selected unit is at Load Point.

3.1.5.5 Bit 9: File Protected

The selected unit does not have a write ring, and writing shall be inhibited.

3.1.5.6 Bit 10: 7-Track

The selected unit is a 7-track unit.

3.1.5.7 Bit 11: Read Data Too Long

The record just read contains more bytes than was initially specified in DRB+14, remaining byte count.

3.1.6 Next Address MSB's (DRB+8, Bits 15-14)

This field specifies the two most significant Monobus address bits for data transfer. It is writable and readable. Its initial state is not defined, hence the programmer must remember to initialize it. The bits are set to zero during a tape IPL. The next DMA address does not carry into this field so data transfers cannot cross 64K boundaries. Attempting to cross a 64K boundary will result in a "wraparound."

3.1.7 Next DMA Address (DRB+12)

This word always contains the address of the next memory location to be read or written into. It is initially loaded by the programmer with the memory buffer address. This register is writable and readable.

3.1.8 Remaining DMA Byte Count (DRB + 14)

This register is loaded with the number of bytes to be transferred. This register is write only and may not be read by the programmer.

4.0 PROGRAMMING

4.1 Typical Programming Flow Chart (without Interrupts)

The Figure 4 flow chart illustrates the sequence of events that must take place in order to initiate a data transfer.

4.2 Programming with Interrupts

The Figure 5 flow chart illustrates the sequence of events that must take place in order to initiate a data transfer from an interrupt mode.

4.3 Cold Start

The Cold Start function is generated when a "Start in IPL Mode" order is issued. The controller will automatically read the first record of unit number 0. The controller will store this data in memory starting at address 0.

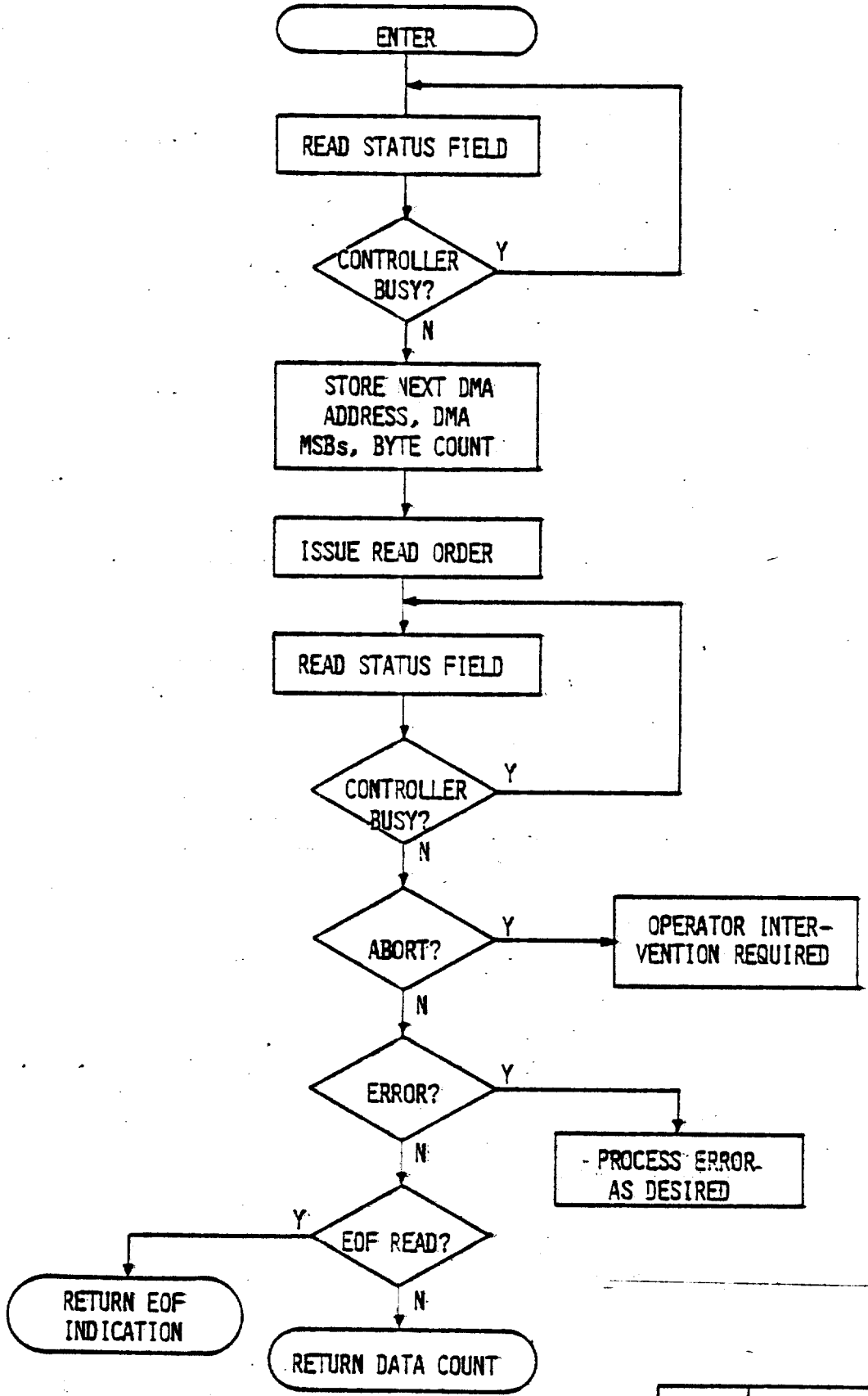


Figure 4. Flow Chart for Non-Interrupt Programming of a Read Operation

A	PS20001320	A
DWG SIZE	SHEET 24 OF 25	REV

Form 3-132-2