MICROPOLIS
MODEL 1115
OEM FLEXIBLE DISK DRIVES

MAINTENANCE MANUAL

MICROPOLIS™

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MAINTENANCE MANUAL

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A	Jan 1983		Initial Release
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SECTION I

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides operation and maintenance information for the Model 1115-Series of 5 1/4-inch Flexible Disk Drives, manufactured by Micropolis Corporation, Chatsworth, California. This manual provides data to aid in installing and maintaining the equipment.

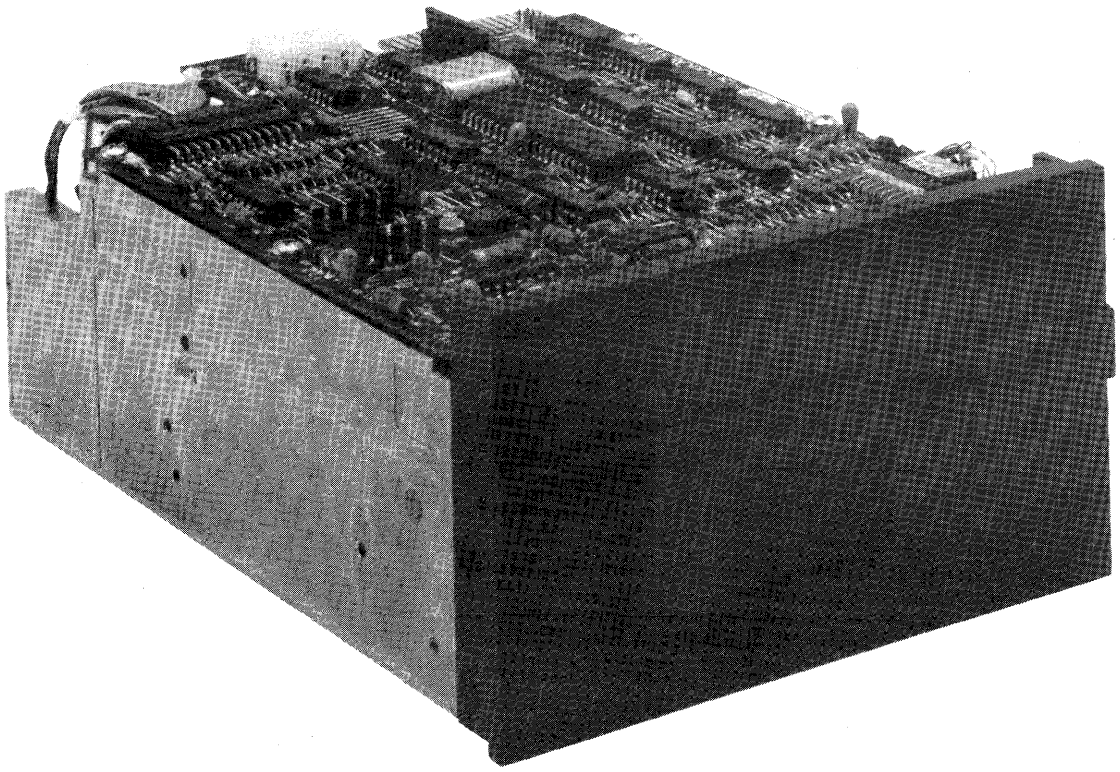

Figure 1-1. Micropolis 1115 OEM Flexible Disk Drive (Typical)

1.2 SCOPE OF MANUAL

This manual is primarily directed to service personnel, either field service engineers or repair technicians in an OEM repair facility. The manual consists of the following eight sections:

a. Section I, General Information, provides introductory data of a general nature. This includes a description and specification summary for the drives, maintenance philosophy, a list of maintenance equipment required, brief preventive and corrective maintenance information, and a description of Micropolis services (including spare parts ordering instructions).

b. Section II, Installation, provides procedures for unpacking the drive, installing the drive, configuring multi-drive systems, and supplying power.

c. Section III, Theory of Operation, provides a detailed description of the disk drive, covering the drive mechanism, the interface, and the drive electronics board.

d. Section IV, Tests and Adjustments, provides procedures to test and adjust critical parameters of the disk drive.

e. Section V, Troubleshooting, provides information to assist in the isolation of a fault to the replaceable component or subassembly in a logical manner.

f. Section VI, Removal and Replacement Procedures, provides step-by-step instructions for the replacement of assemblies, subassemblies, or components of the disk drive.

g. Section VII, Parts Lists, provides a set of parts lists for the disk drive.

h. Section VIII, Assembly Drawings and Schematic Diagram, provides the assembly drawings for the drive, and the assembly drawing and schematic diagram for the Drive Electronics board used in the 1115 Series Flexible Disk Drive.

1.3 DESCRIPTION OF DRIVES

The Disk Drive (see Figure 1-1) consists of a Drive Electronics board and a Drive Mechanism. Since the drives are intended to be mounted within an OEM system and receive regulated DC power from that system, neither enclosure nor regulated power supply is included.

Throughout this manual, the term "1115 drive" refers to any member of the entire series of Model 1115, 5 1/4-inch OEM Flexible Disk Drives.

The specific 1115-series drives described in this manual are:

- Model 1115-2 (Single head, 100 TPI)
- Model 1115-4 (Dual head, 100 TPI)
- Model 1115-5 (Single head, 96 TPI)
- Model 1115-6 (Dual head, 96 TPI)

Model 1115-2 and 1115-4 drives have a track density of 100 tracks per inch (TPI), with 77 total tracks. Model 1115-5 and 1115-6 drives have a track density of 96 TPI, with 80 total tracks. The difference in track density and total number of tracks results from using a different lead screw in the positioner assembly.

Table 1-1 summarizes the specifications of the 1115 drives.

TABLE 1-1. SPECIFICATIONS

Physical	
Height (overall)	3.25 inches (8.26 cm)
Width (overall)	5.75 inches (14.61 cm)
Depth (overall)	8.00 inches (20.32 cm)
Weight	3.60 pounds (1.63 kg)
Environmental	
Ambient temperature:	50°-113°F (10°-45°C)
Relative Humidity:	20%-80% (without condensation)
Shock (Non-Operating)	
In Shipping Container	25.0 G's maximum in any axis
Directly to Drive	15.0 G's maximum in any axis
Vibration	
Non-Operating	3.0 G's maximum (25-2000 Hz) in any axis
Operating	1.0 G's maximum (25-300 Hz) in any axis
Power Dissipation	
Standby	5.3 watts max
Operating	16 watts nominal
Head Load Solenoid (option)	3 watts
Door Lock Solenoid (option)	0.7 watts

TABLE 1-1. SPECIFICATIONS (continued)

Reliability/Maintainability

MTBF (25% spindle motor duty cycle)	8500 hours
MTTR	0.5 hours
Media life	
Passes/Track	3×10^6
Disk Insertions	3×10^4
Error Rate	
Soft error rate	1 in 10^9
Hard error rate	1 in 10^{12}
Seek error rate	1 in 10^6

	Model Number			
Parameter	1115-5	1115-6	1115-2	1115-4
Heads/Drive	1	2	1	2
Tracks/Surface	80	80	77	77
Track Density (TPI)	96	96	100	100
At Speed After MOTOR ON (ms)	200	200	200	200
Spindle Speed (RPM)	300	300	300	300
Speed Variation (%)	±1.5	±1.5	±1.5	±1.5
MFM Data Density (BPI)	5577	5921	5248	5552
MFM Flux Density (FRPI)	5577	5921	5248	5552
MFM Flux Rate (kHz)	250	250	250	250
Encoding Method	MFM	MFM	MFM	MFM
Sectoring Method	Hard/Soft	Hard/Soft	Hard/Soft	Hard/Soft
Unformatted Capacity				
KBytes/Track	6.250	6.250	6.250	6.250
KBytes/Surface	500	500	480	480
KBytes/Diskette	500	1000	480	960
MFM Transfer Rate (Kbits/sec)	250	250	250	250
Average Latency (ms)	100	100	100	100
Head Load Time (ms) (NOTE 1)	75	N/A	75	N/A
Access Time (ms)				
Track to Track	6	6	6	6
Settling	15	15	15	15
Average (NOTE 2)	173	173	167	167

NOTE 1: Timing when head load option is employed
NOTE 2: ([(Tracks per Side - 1)/3] x 6ms) + 15ms

1.4 MAINTENANCE PHILOSOPHY

Micropolis Flexible Disk Drives are designed for trouble-free operation. Maintenance operations require a high degree of technical sophistication, the proper training, and the proper equipment. Non-technical end users should NOT attempt to perform corrective maintenance.

1.5 MAINTENANCE EQUIPMENT REQUIRED

The following tools, test equipment, and special items are required for maintaining and/or servicing Micropolis 1115-Series OEM Flexible Disk Drives. Where a manufacturers part number is given, equivalent equipment may be used.

a. Tools: Screwdriver, Phillips #1.
3/32-inch hex Allen wrench, two-inch shank.
Tweezers.
Cotton swabs.

b. Test Equipment: Oscilloscope - Tektronix 465.
Digital multimeter - Simpson 461.
Frequency counter, 0 to 10 MHz (optional).
Micropolis Flexible Disk Exerciser, Model 1099 (optional).

c. Special Items: DuPont Freon TF or isopropyl alcohol.
Alignment Diskette (see Paragraph 1.5.1).
Cleaning Diskette.

1.5.1 Alignment Diskette

Specific alignment diskettes are used with each configuration of the drive. These are:

100 TPI - Single head - Micropolis Model No. 1081-03 (Dymek)
Dual head - Micropolis Model No. 1081-06 (Dymek)

96 TPI - Single head - Micropolis Model No. 1081-04 (Dymek)
Dual Head - Micropolis Model No. 1081-07 (Dymek)

The proper tracks on the alignment diskette must be used, as follows:

	100 TPI Drives	96 TPI Drives
Radial Alignment Track	36	32
Index Track	5	2
Azimuth Track	76	68

CAUTION

Care should be exercised not to erase the prerecorded alignment tracks. Do not defeat or override the write protect feature of the drive or diskette. Do not install an alignment disk in a drive with a suspected write logic or write protect logic failure. NEVER unplug the drive's head connector or remove power with any diskette installed.

1.6 PREVENTIVE MAINTENANCE

Micropolis Flexible Disk Drives do not require preventive maintenance. However, to ensure trouble-free operation over a wide variety of operating conditions, the preventive maintenance operations specified in Table 1-2 should be performed.

TABLE 1-2. PREVENTIVE MAINTENANCE SCHEDULE

Operation	Frequency	Time Required (Hours)	Manual Paragraph Reference
Replace Head Load Pad	2000 hours of diskette access	0.1	6.5.1
Clean Head	2000 hours of diskette access	0.1	1.6.1

1.6.1 Cleaning the Head

Use an approved cleaning diskette per the manufacturer's instructions. If additional information is required, contact Micropolis Technical Support.

1.7 CORRECTIVE MAINTENANCE

Corrective maintenance consists of isolating a fault to a defective or misadjusted assembly or component, replacing or adjusting the assembly or component, and verifying that the repair has eliminated the fault.

The following suggested sequence will help to make the most effective and efficient use of this manual:

a. Isolate the malfunction to the faulty assembly, subassembly, or component; see the Troubleshooting Chart in Section V.

b. If a more thorough understanding of the operation of a circuit or a mechanical or electrical component is desired; see the Theory of Operation in Section III. The circuit descriptions reference the Assembly Drawings and Schematic Diagram in Section VIII.

c. If necessary, test the suspected circuit or mechanical assembly; see Section IV, Tests and Adjustments. Also using Section IV, it may be possible to perform an adjustment to eliminate the fault.

d. Order the replacement component, subassembly, or assembly; see Section VII, Parts Lists.

e. Replace the component, subassembly, or assembly; see Section VI, Removal and Replacement Procedures.

f. Adjust and/or test the circuit or mechanism after replacing the part; see Section IV, Tests and Adjustments.

1.8 MICROPOLIS SERVICES

a. Training

Formal training courses are conducted by Micropolis at various locations around the world. These courses cover the theory of operation and the maintenance of Micropolis Flexible Disk Drives. Further information on these training courses can be obtained from Micropolis Technical Support.

b. Micropolis Repair Depots

Micropolis maintains fully equipped depots which provide warranty and non-warranty repairs and emergency spares support. Further information on repairs and spare parts availability can be obtained from Micropolis Marketing/Sales Administration, Order Entry Group.

Before returning any item for repair or refurbishment, contact Micropolis Customer Service for a Return Goods Authorization (RGA). Ensure the equipment is properly packed for shipment, following the guidelines given in Paragraph 2.8.

c. Spare Parts

Section VII, Parts Lists, provides part numbers of the replaceable parts for the Model 1115 Drives. Micropolis Technical Support has information on recommended spares levels for field engineers and for repair depots.

Orders for spare parts should be placed through Micropolis Order Entry.

An identification label is attached to the drive. It shows the model number, part number, and serial number of the drive. These numbers should be quoted in all correspondence.

SECTION II

INSTALLATION

2.1 INTRODUCTION

This section provides information necessary for installing the Model 1115 Drive. Included are instructions for unpacking and visually inspecting the drive, installing the drive, providing the proper power and the interface signals, configuring multiple-drive systems and addressing each drive, and re-packing the drive for shipment.

2.2 UNPACKING THE DRIVE

The drive is packed to minimize the possibility of damage during shipment. Carefully follow the procedure to unpack the drive, and SAVE ALL PACKING MATERIAL in case it is necessary to re-pack the drive for shipping.

a. Place the shipping carton on a flat work surface.

b. Cut the sealing tape on the carton top, and open the top flaps.

c. Remove and save the foam that covers the inner carton.

CAUTION

Use extreme care when handling the inner carton; the drive (inside it) is subject to damage if dropped.

d. Carefully remove the inner carton containing the drive, and place it on the work surface.

CAUTION

When the carton is removed, the drive mechanism and circuit board will be exposed. Handle VERY carefully.

e. Remove the top and bottom sections of the inner carton from the drive.

f. Save both halves of the inner carton and the foam covers.

g. Visually inspect the drive for damage. If shipping damage of any kind is evident, notify the carrier at once. Do not return a damaged drive until the shipping company inspector has reviewed the damage, since an insurance claim may be involved.

Verify that the model number on the identification label is as ordered and agrees with the shipping paperwork. Immediately bring any discrepancy to the attention of the supplier.

2.3 DRIVE CONFIGURATIONS

The specific configuration of the drive is established by the installation or omission of jumpers on the Drive Electronics board. These jumper options are used to vary the interface pin assignments of certain signals as well as specify or change many of the functional parameters of the drive. Section 3.3 of this manual provides a detailed description of all of the interface signals and the various options available.

2.4 INSTALLING THE DRIVE

2.4.1 General Guidelines

The following general guidelines should be adhered to when planning the installation:

a. Ambient temperature must be in the range of 50^{o}-113^{o} F(10^{o}-45^{o} C).

b. Avoid dirty, dusty, or smoky areas.

c. Avoid static discharging to any part of the system (use anti-static spray on carpets).

d. Ensure that adequate regulated DC power is available (as specified in Paragraph 2.5).

2.4.2 Specific Mounting Requirements

Refer to Figure 2-1 for details, and ensure that the following mounting requirements are met:

a. The drive may be mounted in any orientation except upside down.

b. The drive will normally be inserted through the panel opening from the front.

c. The mounting scheme must NOT rely on the bezel for support.

d. There are several mounting options (see Figure 2-1):

   1) Use the four #6-32 holes in the bottom of the chassis.

   2) Use the four #6-32 holes (two each side) spaced 4.00 inches apart.

   3) Use the four #6-32 holes (two each side) spaced 3.12 inches apart.

e. For any of the options specified in the preceding steps, mounting screws must not extend more than 0.2 inches into the drive mechanism.

f. Allow for convection cooling of the drive, especially the circuit board area.

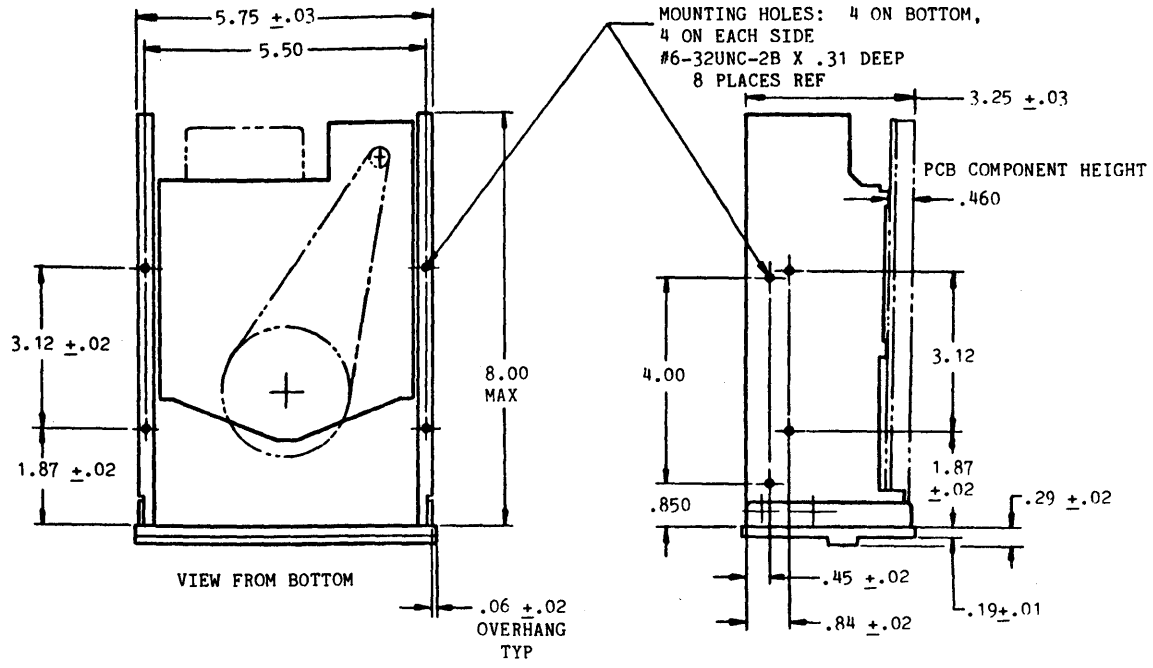

Figure 2-1. Drive Mounting Details

2.5 POWER REQUIREMENTS/CONNECTIONS

a. 1115-Series drives require user-supplied DC power. Regulated 5V and 12V DC power is supplied to the drive via one of three possible connectors on the Drive Electronics board. (Since each "dash-number" version of the board comes with a specific power connector, this is determined when the drive is ordered; J8A is considered to be the "standard" power connector, J7 or J8B are options.)

Connector J8A

The "standard" power connector is J8A, a 4-pin AMP Mate-n-Lok connector (Micropolis P/N 680-0405-0, AMP P/N 641737-1), on the Drive PCBA. The mating connector is AMP P/N 1-480424-0, utilizing AMP P/N 60617-1 pins. For connector J8A, pin assignments are:

J8A Pin	Connection
1	+12V regulated
2	+12V ground return
3	+5V ground return
4	+5V regulated

Connector J7 (optional)

Alternate power connector J7 is a 7-pin Molex connector (Microplois P/N 680-0701-2, Molex P/N 22-05-2071). The mating connector is Molex P/N 22-01-2071, utilizing Molex P/N 08-50-0114 pins. J7 pin assignments are:

J7 Pin	Connection
1	not used
2	insertion key
3	+12V ground return
4	+12V regulated
5	not used
6	+5V ground return
7	+5V regulated

Connector J8B (optional)

Alternate power connector J8B is a 4-pin AMP Mate-n-Lok connector (Micropolis P/N 680-0401-9, AMP P/N 350211-1). The mating connector for J8B is AMP P/N 1-480424-0, utilizing Amp P/N 60617-1 pins. J8B pin assignments are:

J8B Pin	Connection
1	+12V regulated
2	+12V ground return
3	+5V ground return
4	+5V regulated

b. Current requirements (regardless of which power connector is used) are as follows:

Voltage	Ripple Voltage	Standby (Door Open)	Operating	
			Average	Peak
+12V ±5%	100mv	0.1A	1.10A	1.70A
+5V ±5%	50mv	0.70A	0.70A	0.70A

c. The Drive Electronics board's signal ground is connected to the drive chassis via jumper W26 on the board. The drive chassis may be mounted so that it is either isolated or directly connected to the main chassis ground of the host unit.

Additionally, there is a "quick connect" male lug attached to the chassis which may be used to connect the user's earth ground to the drive's chassis. The female mating connector is AMP P/N 60972-1 or equivalent. Careful consideration should be given to the use of this connection: If the signal ground jumper mentioned above is in place, and if the "quick connect" lug is used to connect the drive to the earth ground, then the drive board's signal ground will be connected directly to earth ground. It is recommended that the chassis not be used as a current carrying conductor.

The drive chassis must be connected to the computer chassis or directly to earth ground.

2.6 SIGNAL PIN ASSIGNMENTS

Signal Connector J1 is located on the Drive Electronics board. J1 provides the interface connection between the disk drive and the host controller. Table 2-1 briefly lists the signals at J1; more detailed information on each of the signals, the options available (through the addition or removal of jumpers), and specific timing requirements are given following Table 3-1 of this manual.

TABLE 2-1. CONNECTOR J1 SIGNAL ASSIGNMENTS

Connector Pin Signal	Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
2	1	HDLD/	Head Load	I	W19	W20,W24
(NOTE 3)		DRLK/	Door Lock	I	W10	W12,W14,W29
4	3	INUSE/	In Use	I*	W7	W9
6	5	RDY/	Ready	O	W17	W6,W35
(NOTE 3)		DS4/	Drive Select 4	I*	W4,W6	W5,W8 W17,W35
	DOOR CLOSED/		Door Closed	O	W35	W30,W17
	DRIVE STATUS/		Drive Status	O	W35,W30	W17
8	7	SECP/	Sector/Index Pulse	O*		
10	9	DS1/	Drive Select 1	I*	W1	W2,W3, W4,W5
12	11	DS2/	Drive Select 2	I*	W2	W1,W3, W4,W5
14	13	DS3/	Drive Select 3	I*	W3	W1,W2 W4,W5
16	15	MTRN/	Drive Motor On	I*		
18	17	DIRN/	Step Direction	I*		
20	19	STEP/	Step Command	I*		
22	21	WDA/	Write Data	I*		
24	23	WRT/	Write Gate	I*		
26	25	TRKØ/	Track Ø	O*		
28	27	WPT/	Write Protect	O*		
30	29	RDA/	Read Data	O*		
32	31	HSLT/	Head Select	I*	W27	W28
34	33	DS4/	Drive Select 4	I	W4,W8	W1,W2,W3, W5,W6,W9,
(NOTE 3)		INUSE/	In Use	I	W9	W7,W8,W16
	DOOR CLOSED/		Door Closed	O	W16	W30
	DRIVE STATUS/		Drive Status	O	W16,W30	
		RDY/	Ready	O	W34	W6,W16

* Industry standard interface lines.

Note 1: The mating connector is Scotchflex P/N # 3463-0001 or equivalent.

Note 2: All interface lines are low = true.

Note 3: The specific I/O signal on these lines is selectable by proper jumper placement. See Table 3-1 of this manual.

2.7 MULTI-DRIVE DISK SYSTEMS

Micropolis 1115 Series drives can be configured into multi-drive systems; the drive's interface circuitry provides for up to four drives being connected to a host controller. This section provides the information necessary to implement a multi-drive system.

2.7.1 Daisy-Chaining Drives

A multi-drive system consists of two, three, or four drives, connected to the host controller with a "Daisy-Chain" interface cable.

A typical multiple drive system is shown in Figure 2-2.

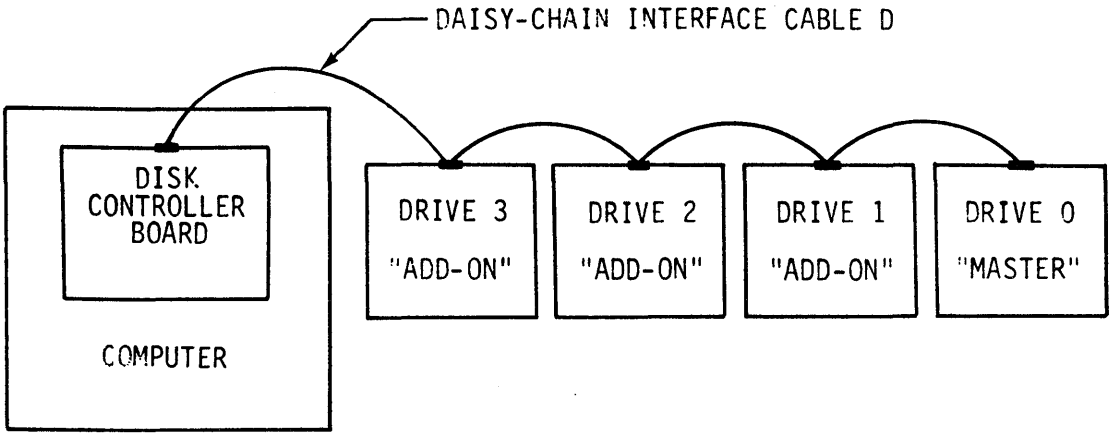

Figure 2-2. Typical Multiple Drive System

The Daisy-Chain interface cables listed below are available from Micropolis:

Name	Model No.	Usage
Interface Cable B	1083-02	Two drives
Interface Cable C	1083-03	Three drives
Interface Cable D	1083-04	Four drives

The Daisy-Chain interface cable is connected in place of the standard Interface Cable A. The Master drive (the one with the terminators) must be connected to the last connector on the cable (i.e., the one farthest from the controller) to provide the proper termination.

2.7.2 Drive Addressing

The interface cable includes four disk select lines in addition to the other input/output lines. All the lines are supplied to all the drives. Address comparison logic in the drive enables the drive to respond to one and only one disk select line. A single drive may be set to respond to address 0, 1, 2, or 3 (normally, if there is only one drive it will be set for address 0). In a multi-drive system, no two drives may be set to respond to the same disk select line.

To establish or change the address of a drive, configure the address comparison logic as follows:

a. Determine which of jumpers W1 through W5 on the Drive Electronics board (see Figure 2-3) are installed. These jumpers specify the drive's address. Only ONE of the jumpers W1 through W4 may be installed on a drive (note that jumper W5, which can be installed in a single-drive system to have the drive always selected, cannot be used in a multi-drive system).

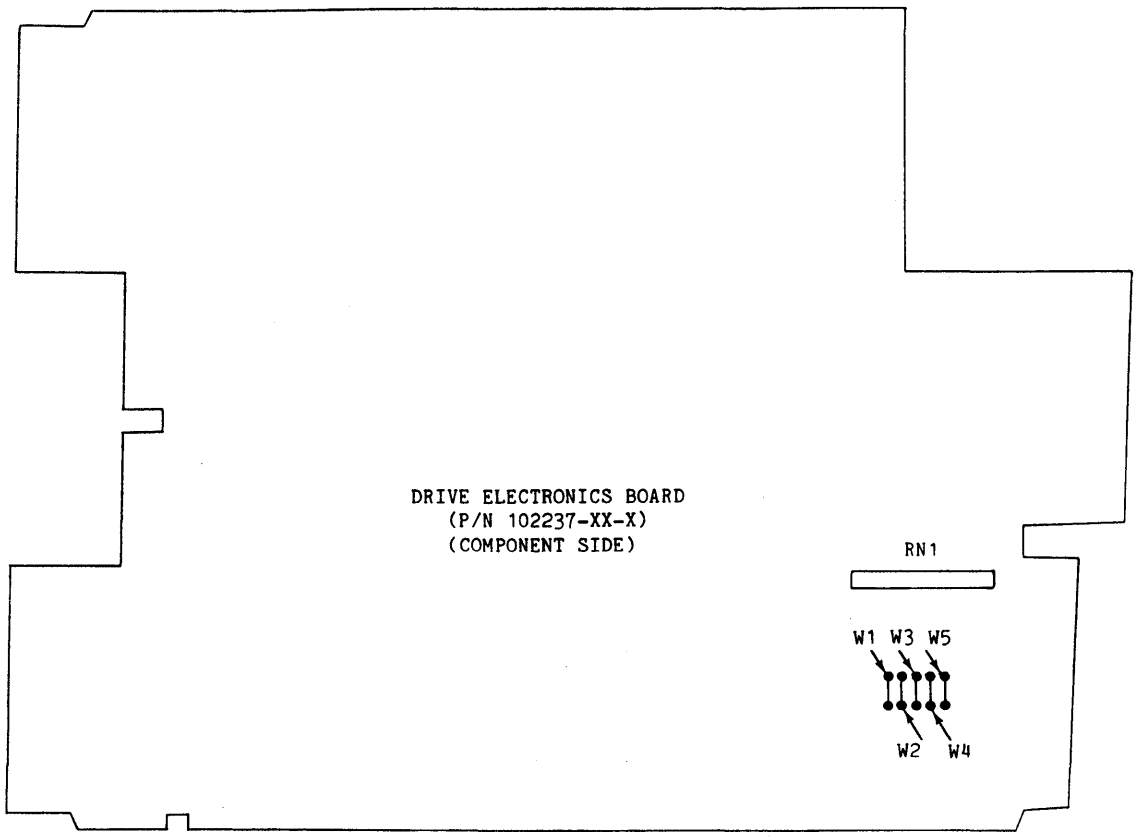

Figure 2-3. Drive Electronics Board Address Jumpers and Terminators

b. To change the drive's address, remove the jumper from the socket and replace it in the socket for the desired address, as follows:

Drive Address	Install Jumper	No Jumper
0	W1	W2,W3,W4,W5
1	W2	W1,W3,W4,W5
2	W3	W1,W2,W4,W5
3	W4	W1,W2,W3,W5

2.7.3 Master to Add-On Conversion

In a multi-drive system a distinction is made between the "master" drive and the "add-on" drives. The master drive includes a resistor network for terminating the interface lines (the network is RN1, Micropolis P/N 116-0011-1). An add-on unit does not include the termination network. The master/add-on distinction does not effect the address selection; any drive may have any address.

To convert a master drive to an add-on, remove the terminator as follows:

a. Locate the terminator resistor pack (RN1, see Figure 2-3).

b. With a small flat-blade screwdriver, carefully loosen the resistor pack and remove it from socket J3. The termination network should be saved in case it is desired to convert the drive back in the future.

2.8 RE-PACKING THE DRIVE FOR SHIPMENT

If it is necessary to re-pack the drive for shipment, the following procedure must be used.

CAUTION

Do not attempt to ship the drive except in the original packing.

a. Put the drive in the bottom half of the inner carton, fold the sides of the carton carefully, and hold them in place.

b. Put the top of the inner carton on the drive, thus securing the sides of the bottom carton in place.

c. Place the bottom foam in the shipping carton.

d. Place the drive in the bottom foam.

e. Put the top foam on top of the drive.

f. Close the outer carton flaps and seal securely with tape.

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

This section describes the theory of operation of the Model 1115, 5 1/4-inch Flexible Disk Drive. The drive consists of the mechanical and electrical components necessary to record data on, and retrieve data from, a magnetic disk. The overall organization of the drive is shown in Figure 3-1.

The theory of operation is presented in the following order:

a. Electromechanical Description (Section 3.2)

   An overall description of the drive's mechanical and electrical components is presented in this section.

b. Drive Interface (Section 3.3)

   All the interface signals used for communication with the host controller are described in this section.

c. Functional Theory of Operation (Section 3.4)

   This section examines the operational interactions between the various functional elements of the Drive Electronics board and the mechanical components.

d. Circuit Theory of Operation (Section 3.5)

   A detailed analysis of the circuitry on the Drive Electronics board is presented in this section.

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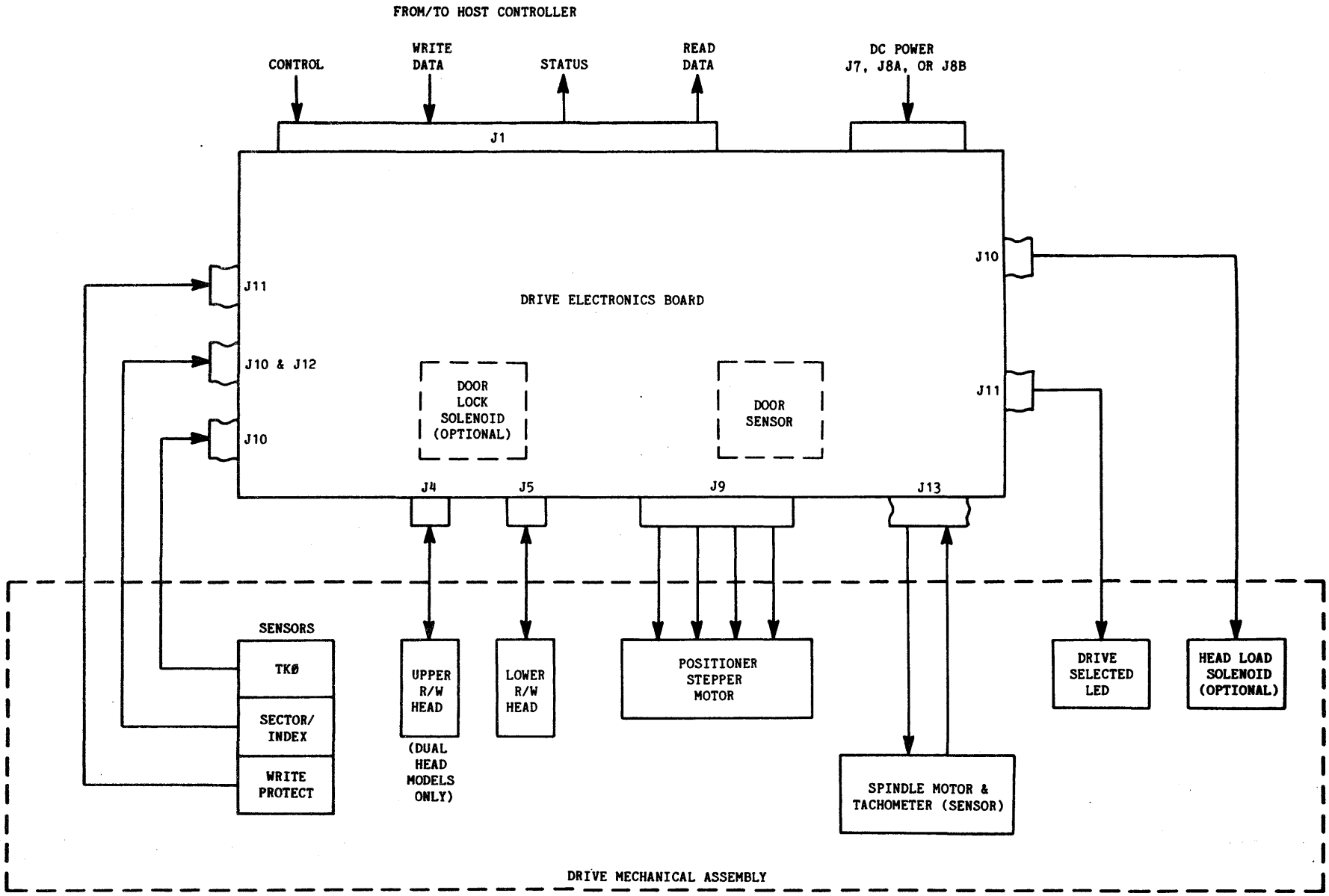

Figure 3-1. 1115-Series Drive Organization

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3.2 ELECTROMECHANICAL DESCRIPTION

The Model 1115 Flexible Disk Drive consists of a drive mechanics assembly and a drive electronics board. Together, the mechanics assembly and the electronics board perform the following functions under control of the host system:

a. Clamp and rotate the diskette.

b. Interpret and generate control signals.

c. Position the read/write head on the desired track.

d. Read and write data.

Figure 3-2 shows the interaction of the drive's mechanical components.

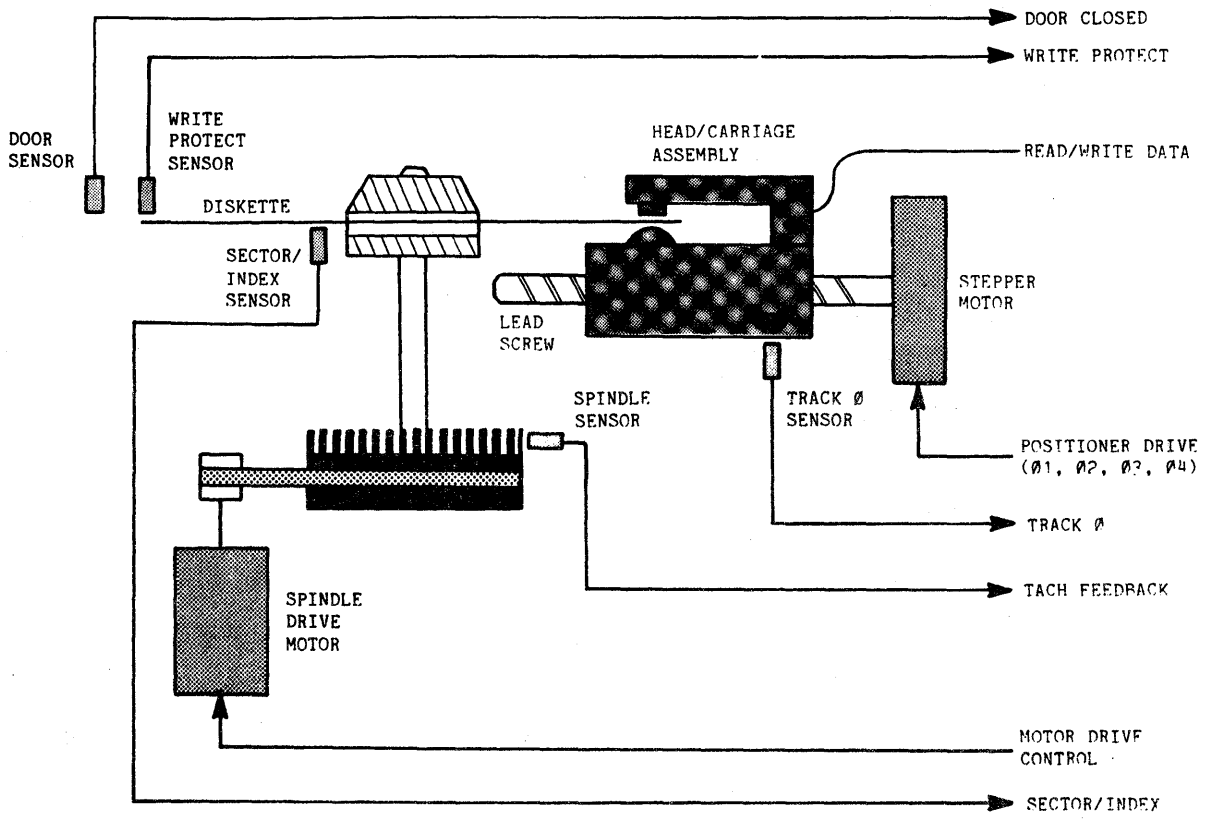


Figure 3-2. Drive Mechanical Elements

3.2.1 Drive Mechanics Assembly

The drive mechanics consists of the following sub-assemblies:

a. Chassis and Sub-chassis

The sub-chassis is comprised of a die cast inner structure that contains virtually all of the drive's mechanical components; it pivots within a die cast outer frame (the chassis). The outer frame isolates the inner structure from mounting related stress and distortion, and provides enhanced EMI shielding for the read/write head(s).

b. Diskette Clamping Mechanism

The diskette is inserted through the disk access door onto a registration hub, which centers the diskette on the spindle shaft. As the door is closed, the diskette is rotated and clamped to the spindle motor hub. Note that when the diskette is inserted and the door is closed, the spindle motor is automatically energized. This action (independent of the interface signals) centers and seats the diskette on the spindle for accurate registration. A sensor detects when the door begins to close.

c. Spindle Drive Motor

The spindle is driven by a DC motor. The motor-to-spindle pulley size ratio provides the proper speed reduction. An LED/photo-sensor pair senses "flags" on the spindle pulley; the resulting sensor pulses are applied to the drive's Microcomputer, which generates a control signal to slow down or speed up the spindle motor, thereby the correct speed. Generating the feedback signal at the spindle pulley eliminates any effects of pulley or belt wear. This gives the drive a very closely regulated spindle speed of 300 RPM, enhancing data reliability and diskette interchange-ability.

d. Head/Carriage Assembly

Each head consists of a ferrite read/write element and two tunnel erase elements mounted in a ceramic slider. The head(s) are designed to provide maximum signal transfer to and from the diskette with a minimum of wear. During write operations, tunnel erase gaps trim the written data to produce a clean erased area between adjacent tracks. This erased area provides a guard band, which allows reasonable mechanical tolerances to be used without affecting the interchangeability of diskettes between drives. This also increases data reliability.

The read/write head is mounted in a carriage assembly, which is supported and driven by a lead screw; see Section 3.2.1f. Double-sided models use two heads; one on each side of the diskette.

e. Head Lift Mechanism

The read/write head is loaded against the diskette via a load arm operated by either the door latch assembly or the optional head load solenoid (for single-head drives only). A cushion on the load arm assures that the diskette jacket is loaded against the platen surface to maintain correct head-to-diskette contact.

1) Drives using the door-operated load arm cause the head(s) to load whenever the door is closed; opening the door unloads the head(s).

2) The single head drives that include the optional head load solenoid load the head upon activation of the solenoid; de-activating the solenoid unloads the head. Solenoid control is asserted either by the host controller or by the drive's Microcomputer.

Dual head drives have an "interposer" feature to prevent the heads from loading if a diskette is not present. This protects the polished head surfaces (by preventing them from contacting each other).

f. Head Positioner

The head/carriage assembly (see Section 3.2.1d) is positioned by a four-phase, permanent magnet stepper motor, a jeweled follower, and stainless steel lead screw.

The stepper motor and lead screw combination positions the head to the desired track. The head/carriage assembly moves (via the follower) along a radial line with respect to the diskette when the lead screw is rotated. For each Step Command pulse received from the host controller, the head moves one track position in or out as specified by a direction signal.

The positioner lead screw is preloaded in tension against a bearing in the sub-chassis, directly adjacent to the spindle. This referencing technique removes the sub-chassis from the thermal expansion loop, giving repeatable and exact track positioning that is independent of temperature.

g. Sensor Assemblies

There are five sensor assemblies in the drive. Each of the sensor assemblies consists of a LED/photosensor pair. These utilize non-contact sensing for high reliability and long life.

1) Sector/Index Sensor

A photosensor circuit is used to detect the occurrence of the diskette's index mark (and sector marks, if present). These are holes in the diskette that are used by the host controller for formatting purposes.

Soft-sectored diskettes do not have pre-assigned sectoring, and thus do not have sector marks, only a single index mark. Hard sectored diskettes have sector holes that divide the diskette surface into equal angular segments. The index hole is located midway between the holes identifying the last sector and sector Ø. Because the Sector/Index photosensor circuit generates a signal for each hole, the host controller must be able to differentiate the index hole from the sector holes.

2) Track Ø Sensor

The Track Ø Sensor circuit provides an input signal to the drive's Microcomputer when the read/write head is positioned at Track Ø. The interface Track Ø signal is a microcomputer-generated signal that is set true when the head is positioned at Track Ø and the stepper motor is placed in the hold mode.

If, during normal operation, the host controller suspects a positioning error, it should step the drive out until Track Ø is reached and the interface Track Ø output goes true.

3) Write Protect Sensor

CAUTION

> Two write protect conventions are explained in the following paragraphs. Ensure that the appropriate write protect option is installed in your system.

The diskette's write protect status is determined by a cutout along one edge of its jacket. The presence of that cutout is detected by a sensor assembly mounted in the drive mechanism. If the cutout is covered, the write circuits are disabled and the diskette cannot be overwritten. However, if the cutout is uncovered, writing is permitted. The write protect status is sent to the host system via an interface line.

A jumper-option is available that reverses the above-described logic. If this option is implemented, when the cutout is covered, the write circuits are enabled; and the diskette can be overwritten. If the cutout is uncovered, the diskette is write protected.

4) Spindle Feedback Tachometer

An optical sensor assembly and a spindle pulley with integral flags form the spindle tachometer. The sensor (tachometer) output signal is sent to the drive's Microcomputer as spindle speed feedback. The Microcomputer then processes this data and generates a control signal to appropriately slow down or speed up the motor.

5) Door Sensor

The Door Sensor is composed of a flag and an LED/photosensor pair, which provides an input to the drive's electronics that indicates the start of closure of the disk access door. This signal automatically starts the spindle motor. This provides smooth and accurate diskette clamping, since the spindle will be turning when the diskette is clamped. The signal stays asserted as long as the door is closed. This signal is also gated with the various door lock options and ensures that the door lock solenoid cannot be activated when the door is open.

h. Indicator

An LED indicator in the front bezel is used to indicate when the drive has been selected by the host system.

3.2.2 Drive Electronics Board

The Drive Electronics board contains the interface circuitry, the Microcomputer-based control logic, and the read/write circuitry for the drive. It includes the following elements:

a. Drive Select Logic

This circuitry uses a jumper to define the drive's address. The drive then responds to the corresponding one of four Drive Select lines. When the appropriate Drive Select line is true, the drive responds to signals on the interface input lines. When the drive is selected, the interface output lines are enabled.

b. Drive Ready Logic

The optional Ready (RDY/) signal is an interface status signal that provides an indication to the host interface that:

- The drive is powered.
- The diskette is inserted.
- The disk access door is closed.
- The drive is selected.
- The spindle motor is up to speed.

If the Ready option is used, it is recommended that the controller test the RDY/ state before initiating a read/write operation.

c. Positioning Control Logic and Power Drivers

The drive's Microcomputer implements the logical functions for the positioner by generating appropriate motion and direction signals. The power drivers amplify the drive signals to the stepper motor.

d. Write/Erase Circuits

These circuits accept the encoded write data from the interface and generate the signals to the write head. The erase circuits control the turn-on/turn-off time delay for the trailing erase heads. These delays ensure appropriate registration between written data and the erase bands.

e. Read Circuits

These circuits amplify, filter, differentiate, zero-crossing detect, and digitize the read signal. Additional circuits de-glitch and wave shape the data for transmission to the host.

f. Interface Drivers and Receivers

The Drivers provide the appropriate signal levels at the drive interface to transmit data and status to the host.

The Receivers provide proper termination for data and control signal lines from the host.

g. Spindle Speed Control

The Microcomputer controls the spindle speed via direct feedback from the optically servoed drive system. This direct feedback control provides precise speed regulation, and eliminates the need for speed adjustment.

3.3 DRIVE INTERFACE

3.3.1 Drive Interface Connection

Interface Connector J1 provides signal interconnection between the disk drive and the host controller. J1 is a 34-pin edge connector which is physically part of the Drive Electronics printed circuit board. The interface is pin and plug compatible with what is accepted as the "industry standard" configuration. Additional control and status interface lines are also present; their use is optional.

Either flat cable or twisted pairs may be used, with a maximum cable length of twenty feet. The recommended mating connector is Scotchflex 3464-0001. Care should be taken to avoid contamination of the gold contact fingers. If necessary, the connector may be cleaned using a cotton swab and DuPont Freon TF or isopropyl alcohol.

3.3.2 Drive Interface Signals

The signal assignments and jumper options at each pin of Interface Connector J1 are listed in Table 3-1; the table and the following paragraphs provide a detailed description of each signal (and jumper-selectable option) and show the required timing relationships between them. The jumpers are located on the Drive Electronics board; their locations are shown in Figure 3-3.

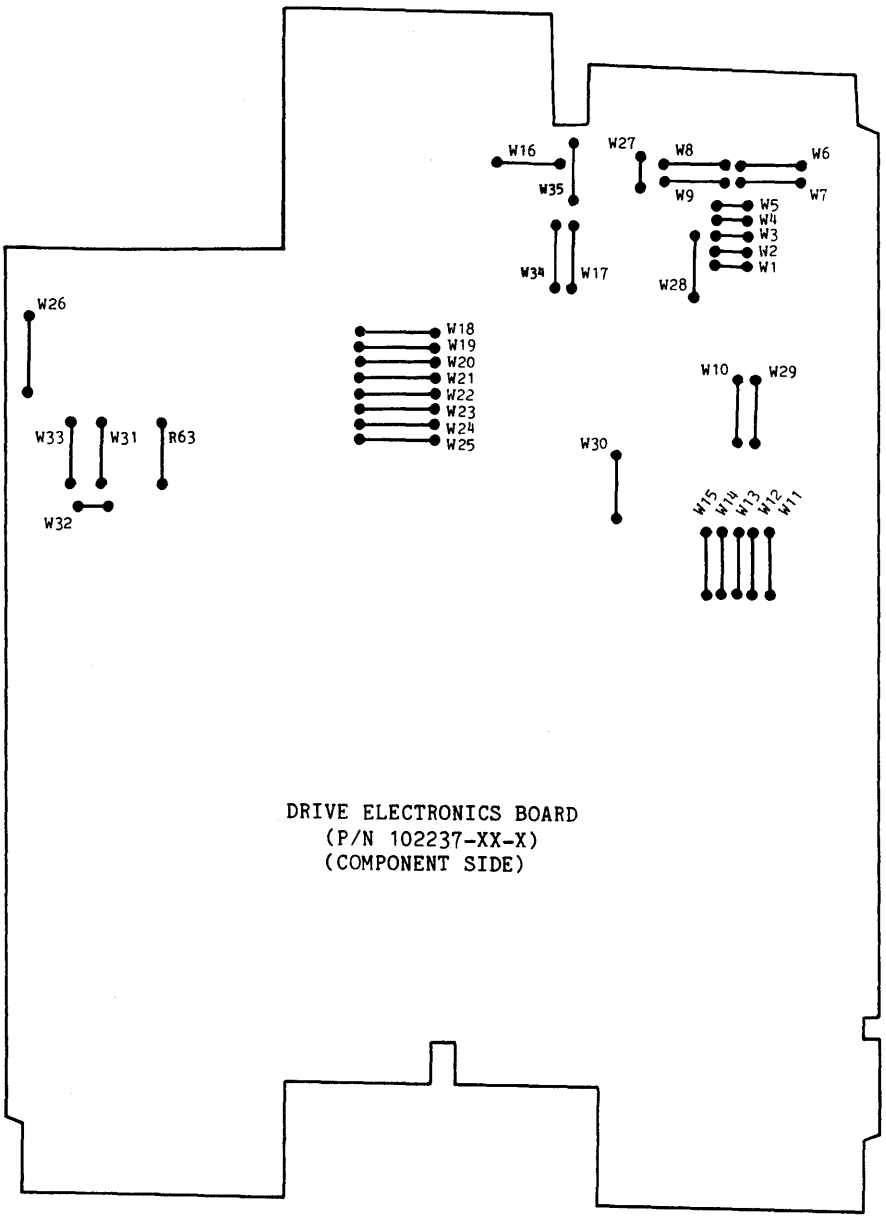


Figure 3-3. Drive Electronics Board Jumper Locations

TABLE 3-1. INTERFACE SIGNAL DETAILS

Connector Pin Signal	Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
2	1	One of:				
		HDLD/	Head Load	I	(see below)	
		DRLK/	Door Lock	I	(see below)	

If HDLD/ is on J1-2, then DRLK/ is not available and vice versa. The use of either of these signals requires a corresponding optional solenoid.

Head Load Options:

If W19 is installed (W20 and W24 omitted), the head will load when the MTRN/ interface signal is asserted (which turns on the drive motor) and either the HDLD/ interface signal is asserted or the drive is selected.

In addition to head load operation via the interface HDLD/ signal, the following head load jumper options are available:

a. If W20 is installed (W19 and W24 omitted), the head loads when both MTRN/ is asserted and the drive is selected.

b. If W24 is installed (W19 and W20 omitted), the head loads when either MTRN/ is asserted or the drive is selected.

Door Lock Options:

If W10 is installed (W12, W14, and W29 omitted), asserting the DRLK/ signal (when the diskette access door is closed) will activate the Door Lock Solenoid, thereby locking the door.

In addition to door lock solenoid operation via the interface DRLK/ signal, the following door lock jumper options are available:

a. W12 Option (W10, W14, and W29 omitted): If the INUSE/ signal is true when the drive is selected, the Door Lock Solenoid activates, locking the door of the selected drive. When INUSE/ goes false and the drive is selected again, the door unlocks.

b. W14 Option (W10, W12, and W29 omitted): If INUSE/ is true, the Door Lock Solenoid activates, locking the door.

c. W29 Option (W10, W12, and W14 omitted): The Door Lock Solenoid activates when the drive is selected.

TABLE 3-1. INTERFACE SIGNAL DETAILS (continued)

Connector Pin Signal	Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
4	3	INUSE/	In Use	I*	W7	W9

For an alternative interface INUSE/ option, see J1-34.

If the INUSE/ signal is on J1-4, then J1-34 can be used (with appropriate jumpering) for the DS4/ input, the DOOR CLOSED/ output, or the DRIVE STATUS/ output.

The INUSE/ interface signal, in conjunction with the four jumper options listed below, allows the host controller to operate the Door Lock Solenoid or the Front Panel LED.

INUSE/ Interface Signal Options:

Option a or b may be selected in conjunction with option c or d. Note that door lock solenoid options require inclusion of the optional door lock solenoid.

a. W12 Option (W10, W14, and W29 omitted): If the INUSE/ signal is true when the drive is selected, the Door Lock Solenoid activates, locking the disk access door of the selected drive. When INUSE/ goes false and the drive is selected again, the door unlocks.

b. W14 Option (W10, W12, and W29 omitted): Assertion of the INUSE/ signal (regardless of the Selected status), activates the Door Lock Solenoid, locking the door.

c. W13 Option (W11 and W15 omitted): If the INUSE/ signal is asserted when the drive is selected, the Front Panel LED lights. When the INUSE/ signal goes false and the drive is selected again, the LED goes off.

d. W15 Option (W11 and W13 omitted): Assertion of INUSE/ (regardless of the Selected status) lights the Front Panel LED.

* Industry standard interface line.

TABLE 3-1. INTERFACE SIGNAL DETAILS (continued)

Connector Pin Signal	Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
6	5	One of:				
		RDY/	Ready Status	O	W17	W6
		DS4/	Drive Select 4	I*	W4,W6	W1,W2,W3, W5,W8,W17
		DOOR CLOSED/	Door Closed	O	W35	W30,W16, W17
		DRIVE STATUS/	Drive Status	O	W35,W30	W16,W17

If DS4/ is on J1-6, the RDY/ status signal is not available and vice versa.

RDY/ Interface Signal Options:

a. W18 Omitted: This option places the RDY/ signal on the interface at J1-6. The RDY/ signal is true when the power supplies are up to voltage, the disk access door is closed, the spindle has been rotated for proper seating of the diskette, the drive is selected, the drive motor is at speed, and at least one index pulse has been detected by the drive's Microcomputer, verifying the presence of a diskette.

b. W18 Installed: When a seek operation is initiated, RDY/ will be set false; upon seek completion, RDY/ will be set true, indicating to the host controller that the drive is ready to accept further commands.

DS4/ Interface Signal Option:

For an alternative interface DS4/ input option, see J1-34.

For a detailed explanation of the Drive Selection process, refer to Section 3.3.2.2.

DOOR CLOSED/ Interface Signal Option:

For an alternative interface DOOR CLOSED/ input option, see J1-34.

DRIVE STATUS/ Interface Signal Option:

For an alternative interface DRIVE STATUS/ input option, see J1-34.

* Industry standard interface line.

TABLE 3-1. INTERFACE SIGNAL DETAILS (continued)

Connector Pin Signal	Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
8	7	SECP/	Sector/Index Pulse	O*	---	---

The SECP/ signal goes true when a sector hole or index hole is detected as the diskette rotates. The sector/index determination is handled by the host controller. For information on Sector/Index Pulse timing, to Section 3.3.2.3.

Connector Pin Signal	Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
10	9	DS1/	Drive Select 1	I*	W1	W2,W3, W4,W5

Refer to Section 3.3.2.2 for a complete explanation of the Drive Selection process.

Connector Pin Signal	Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
12	11	DS2/	Drive Select 2	I*	W2	W1,W3, W4,W5

Refer to Section 3.3.2.2 for a complete explanation of the Drive Selection process.

Connector Pin Signal	Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
14	13	DS3/	Drive Select 3	I*	W3	W1,W2, W4,W5

Refer to Section 3.3.2.2 for a complete explanation of the Drive Selection process.

Connector Pin Signal	Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
16	15	MTRN/	Drive Motor On	I*	(see below)	

The MTRN/ line allows the host controller to enable and disable the spindle motors of each disk drive or all of the drives in the system simultaneously.

* Industry standard interface lines.

TABLE 3-1. INTERFACE SIGNAL DETAILS (continued)

MTRN/ Interface Signal Options:

a. With both W21 and W22 omitted, the motor will turn on whenever MTRN/ is true.

b. With W21 installed (W22 omitted), the motor will turn on when MTRN/ is true and the drive is already selected.

c. With W22 installed (W21 omitted), the motor will turn on if MTRN/ is true or the drive is selected.

Connector Pin Signal	Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
18	17	DIRN/	Step Direction	I*	(see below)	

The DIRN/ signal controls the direction of motion of the head(s) when a Step Command (in the form of one or more pulses on the STEP/ interface line) is received. If DIRN/ is low when a Step Command is received, the head(s) will move toward the center of the diskette (higher track number). Motion away from the center (lower track number) of the diskette occurs when a Step Command is applied to the interface line while DIRN/ is high.

Head Selection Option:

For dual-head drives only, if W28 is installed (and W27 is omitted), the interface DIRN/ line also performs the head selection function. A true (low) level selects the upper head; a false (high) level selects the lower head. (Note that head selection is not valid while the drive is stepping; J1-32 would then not be used for head selection).

When a Step Command pulse is received, this line's level determines the step direction in the same manner as described above.

Connector Pin Signal	Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
20	19	STEP/	Step Command	I*	---	---

The drive will step one track from the current track per Step Command pulse, in the direction specified by the DIRN/ line (see J1-18). For information on Step Command timing, refer to Section 3.3.2.4.

* Industry standard interface lines.

TABLE 3-1. INTERFACE SIGNAL DETAILS (continued)

Connector Pin Signal Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
22 21	WDA/	Write Data	I*	---	---

Write Data is the encoded data from the host to be written on the diskette. For information on Write Data timing, refer to Section 3.3.2.5.

Connector Pin Signal Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
24 23	WRT/	Write Gate	I*	---	---

Read/write control for the selected drive is exercised via the WRT/ input signal. When WRT/ is true (low), the drive's write circuits are enabled provided the diskette is not write protected (see J1-28 for write protect options) and a step operation is not in progress. Write Data (at J1-22) is written on the diskette. When the WRT/ signal is false (high), data is read from the diskette and is output to the interface as RDA/ (at J1-30). For information on Write Gate timing, refer to Section 3.3.2.6.

Connector Pin Signal Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
26 25	TRKØ/	Track Ø	O*	---	---

The TRKØ/ signal is controlled by the drive's Microcomputer, and is set true when the read/write head is positioned at Track Ø and the Microcomputer has placed the stepper motor in the hold mode. This signal indicates to the host that the head is at Track Ø; the host uses this information to establish a reference point to continually compute the current track position.

Connector Pin Signal Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
28 27	WPT/	Write Protect	O*	(see below)	

The Write Protect status is sent to the host system and indicates the write protected status of the diskette.

WPT/ Interface Signal Options:

a. "Standard" write protect convention with W32 and W33 installed (etched conductors), W31 omitted, and R63 = 100K ohms:

   The diskette is write protected when the diskette notch is covered by a write protect tab (this disables the drive's write circuitry; the interface WPT/ signal conveys this status to the controller). With the notch uncovered, the drive's write circuitry is enabled.

* Industry standard interface lines.

TABLE 3-1. INTERFACE SIGNAL DETAILS (continued)

b. With W31 installed, W32 omitted and W33 = 100K ohms (this requires cutting the etched jumpers at W32 and W33 and installing a 100K ohm resistor for W33), and R63 = Ø ohms:

The diskette is write protected when the notch in the diskette is uncovered (this disables the drive's write circuitry; the interface WPT/ signal conveys this status to the controller). Covering the notch enables the drive's write circuitry.

Connector Pin Signal	Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
30	29	RDA/	Read Data	O*	---	---

The Read Data, read from the diskette, is then decoded by the host. For information on Read Data timing, refer to Section 3.3.2.7.

Connector Pin Signal	Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
32	31	HSLT/	Head Select	I*	W27	W28

See J1-18 for an alternative head selection option.

For dual-head drives only, a true (low) level selects the upper head; a false (high) level selects the lower head. For information on Head Select timing, refer to Section 3.3.2.8.

Connector Pin Signal	Ground	Signal Name	Description	In/Out	Jumpers In	Jumpers Out
34	33	One of:				
		DS4/	Drive Select 4	I	W4,W8	W1,W2,W3, W5,W6,W9, W16
		INUSE/	Inuse	I	W9	W7,W8,W16
		DOOR CLOSED/	Door Closed	O	W16	W30
		DRIVF STATUS/		O	W16,W30	
		RDY/	Ready Status	O	W34	W6,W16,W17

* Industry standard interface lines.

TABLE 3-1. INTERFACE SIGNAL DETAILS (continued)

DS4/ Interface Signal Option:

This is an alternative to using J1-6 for the DS4/ signal. For an explanation of the Drive Selection process, see to Section 3.3.2.2

INUSE/ Interface Signal Option:

This is an alternative to using J1-4 for the INUSE/ signal.

The INUSE/ interface signal (in conjunction with four jumper options) allows the host controller to operate the Door Lock Solenoid or the Front Panel LED; see the explanation for J1-4.

DOOR CLOSED/ Interface Signal Options:

a. W23 Installed: J1-34 is low (true) when the disk access door is closed and is high (false) when the door is open.

b. W23 Omitted: This enables a latch function that monitors and stores any door open event. When the door is opened, J1-34 will remain high (false) until the drive is deselected; then the output will reflect the current door status (low when the door is closed and high when the door is opened).

DRIVE STATUS/ Interface Signal Options:

a. If W23 is installed, DRIVE STATUS/ will be true (low) when the following three conditions are met:

   - The drive is selected.
   - The disk access door is closed.
   - The drive is Ready (a diskette has been inserted, indicated by a Sector Pulse having occurred; and the spindle is at speed).

b. If W23 is omitted, the DRIVE STATUS/ signal will be true (low) when the following three conditions are met:

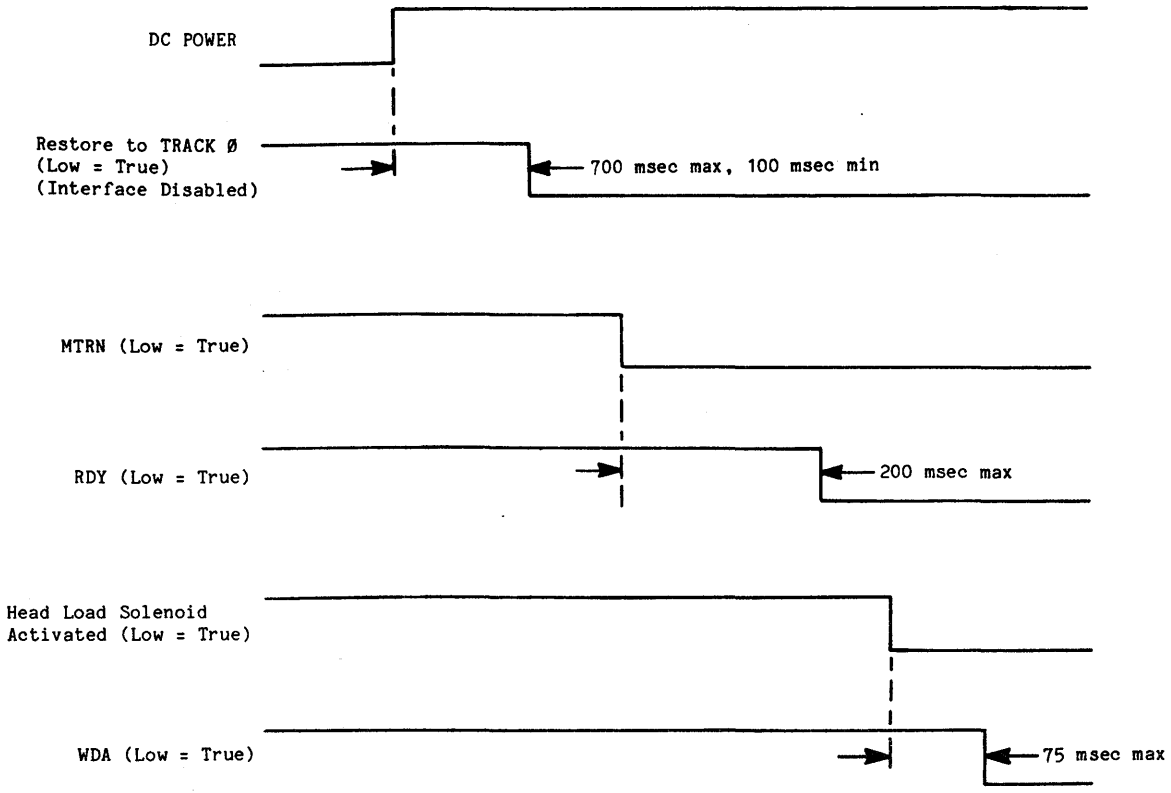
   - The drive is selected.
   - The disk access door has not been opened since the drive was last deselected.
   - The drive is Ready (a diskette has been inserted, indicated by a Sector Pulse having occurred; and the spindle is at speed).

RDY/ Interface Signal Option:

This is an alternative to using J1-6 for the RDY/ signal.

3.3.2.1 Drive Interface General Timing

General timing requirements are specified in Figure 3-4. Specific timing requirements are given with the particular signals.



Drive functions are unavailable to the user until the initialization is complete; i.e., TRKØ/ is true.

NOTE: The head load solenoid is optional.

Figure 3-4. General Timing

3.3.2.2 Drive Selection

The Drive Select lines DS1/, DS2/, and DS3/ (J1-10, J12, and J1-14 respectively) have fixed I/O connector pin assignments; the DS4/ line, if used, has two input pin options:

a. J1 pin 6: The DS4/ signal appears on J1-6 when W6 is installed and W8 is removed.

b. J1 pin 34: When W8 is installed and W6 is removed, the DS4/ signal appears on J1-34.

Assertion of one of the four Drive Select lines (to a drive that has the corresponding jumper W1 through W4 installed), selects that drive for operation by the host controller. In a multiple drive system, each drive must have a unique jumper address (assigned by the use of one of the jumpers W1, W2, W3, or W4) and is selected by a different Drive Select line. When selected, the drive responds to control and data signals on the input lines and provides status and data signals on the output lines.

If jumper W5 is installed (with W1 through W4 removed), the drive is always Selected. This alternative should only be used on single-drive systems.

Two other jumper options are:

a. If W11 is installed (W13 and W15 omitted), the Front Panel LED illuminates when the drive is Selected.

b. If W12 is installed (W10 and W14 omitted) and the INUSE/ signal is true, the door will be locked when the drive is Selected. To deselect the drive, switch INUSE/ false; and re-assert the Drive Select line.

3.3.2.3 Sector/Index Pulse Timing

This signal goes true for 4 (±1) milliseconds each time an index hole (and the sector holes, if present) in the diskette passes the Sector/Index sensor in the selected drive. The leading edge of the signal should be used by the host as the time reference.

The SECP/ output signal is not valid until the diskette has reached operating speed. Figure 3-5, Sector/Index Timing (16 Sectors), shows the timing for a sixteen sector diskette rotating at 300 RPM. The optional interface Ready (RDY/) line may be used to indicate when the motor is up to speed.

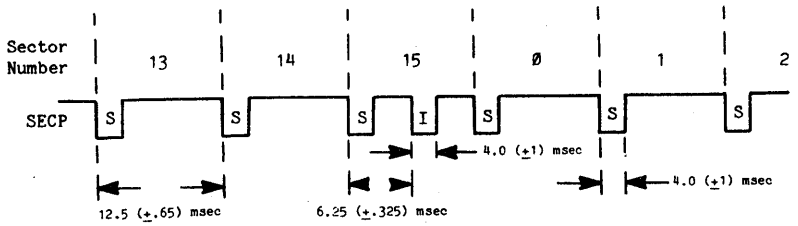


Figure 3-5. Sector/Index Timing (16 Sectors)

3.3.2.4 Step Command Timing

The host controller needs to provide only one STEP/ pulse on the interface to move the positioner one track position in accordance with the direction specified by the DIRN/ interface signal.

Stepping can be performed either in "Conventional" or "Burst" mode. Mode selection is made automatically by the drive's Microcomputer, based on the pulse rate of the incoming Step pulses. Step pulses with a period equal to or greater than six milliseconds force the logic into Conventional mode; pulses with a period of from three to five milliseconds force the logic into Burst mode. Step pulses with periods between five and six milliseconds are not valid.

The interface Ready line (with jumper W18 installed) may be used as a Seek Complete line, which indicates to the host computer that the head is in position and reading or writing may occur. If this option is used, add twelve milliseconds to the positioning timing before reading or writing.

The Ready line option may be used in either Conventional or Burst mode; it is particularly useful in Burst mode, in that it eliminates the requirement for the host controller to calculate and implement the time delay TTP1 (which is described below in the description of the Burst Mode). Instead, the host controller only has to check the interface Ready line and ensure that RDY/ is true prior to a read/ write operation.

a. Conventional Mode: Conventional Mode is used for pulse rates greater than or equal to six milliseconds. Minimum time between consecutive Step pulses is six milliseconds when moving in the same direction or 21 milliseconds when changing the direction of motion. A 21-millisecond (minimum) period must elapse after the last Step pulse is received and a read or a write operation begins; see Figure 3-6 for Conventional Mode Stepper Timing.

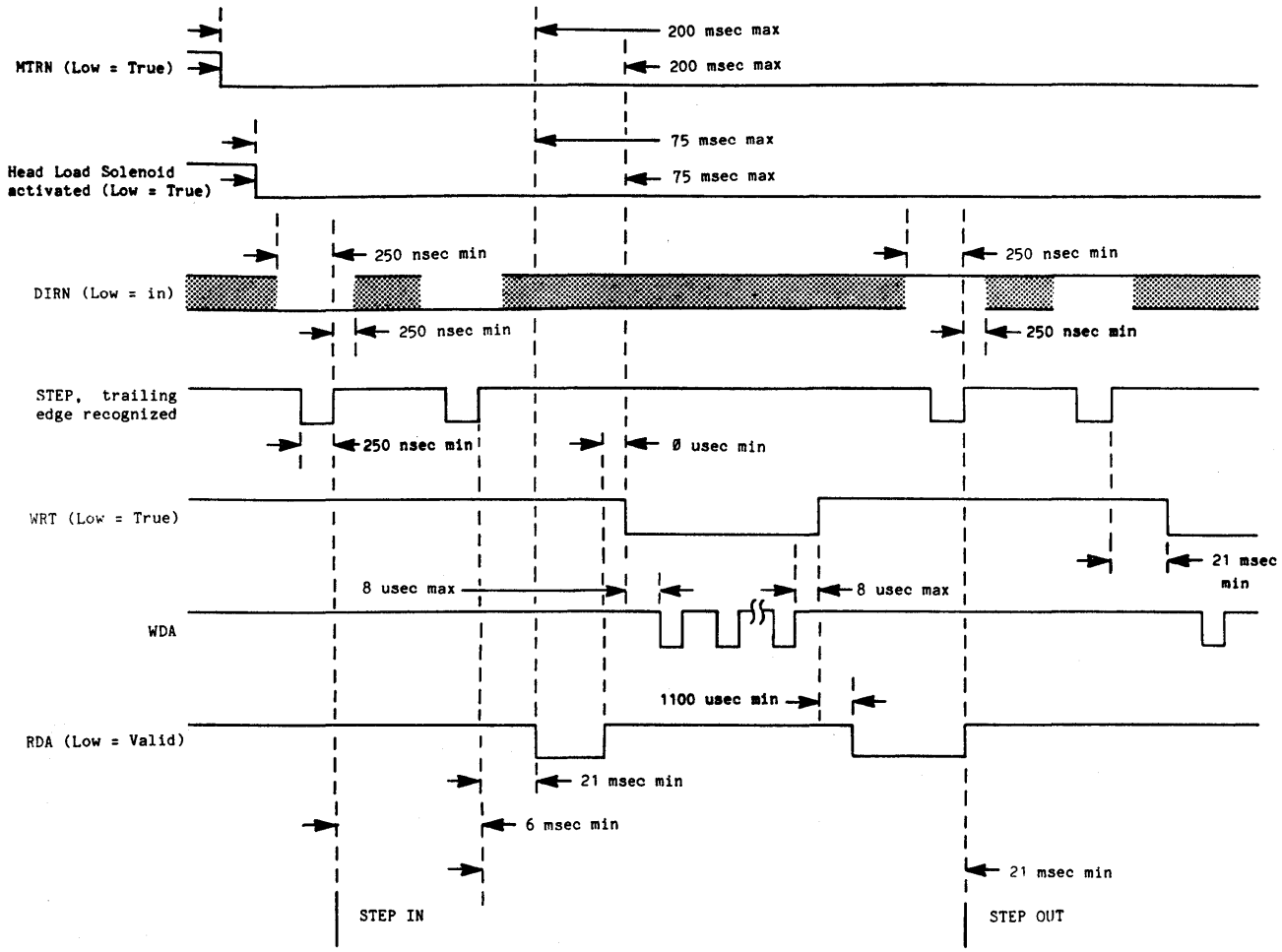
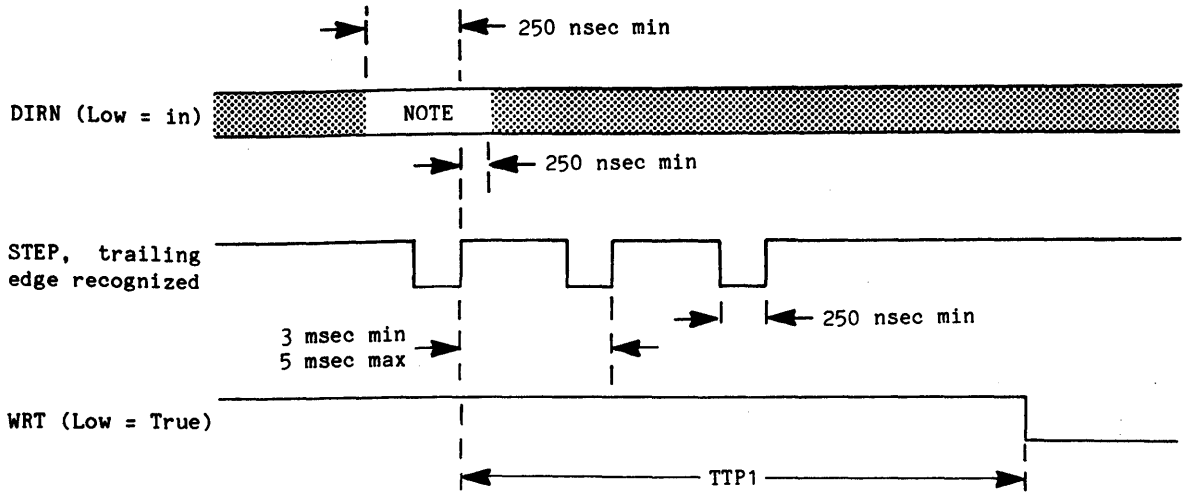


Figure 3-6. Conventional Mode Stepper Timing

b. Burst Mode: The Burst Mode is for pulse rates of from three to five milliseconds, see Figure 3-7. Burst mode is advantageous for executing overlapped seeks in multi-drive systems.



NOTE: The direction of movement is specified by the state of the interface DIRN/ line upon receipt of the first Step pulse.

Figure 3-7. Burst Mode Stepper Timing

Although pulses may be sent to the drive at rates between three and five milliseconds, the host must allow Time-To-Position (TTP1) the head prior to any read/write operation, where:

$$TTP1 = \begin{pmatrix}\text{number of Step} \\ \text{pulses in burst}\end{pmatrix} \times (6 \text{ ms/track}) + 15 \text{ ms}$$

There may theoretically be up to 256 pulses in a burst. As a general rule, though, the controller will normally issue no more pulses than there are tracks (i.e., the maximum number of pulses equals the number of remaining tracks from the current track to the last available track).

After the last step pulse in a burst, no further pulses are allowed until the TTP1 has elapsed. During TTP1, the stepper motor positions the read/write head in accordance with the number of step pulses received and in the direction specified. At the end of TTP1, the read/write head is in position; and the drive is available for reading, writing, or further positioning.

DIRN/ should be allowed to settle for 250 nanoseconds prior to the first Step pulse, and it must not change for 250 nanoseconds after the trailing edge of the last pulse in the burst.

3.3.2.5 Head Select

This interface input signal selects the lower head when at a high logic level and the upper head when at a low level. The timing restrictions placed on the switching of the interface HSLT/ signal are shown in Figure 3-10.

Head Select (HSLT/) should not change sooner than 250 nanoseconds before the Write Gate (WRT/) signal is asserted and no later than 250 nanoseconds after Write Gate is terminated.

3.3.2.6 Write Gate

Read/write control for the selected drive is exercised via the WRT/ input signal. Read Channel circuitry is disabled and Step Commands are ignored while WRT/ is true and during trim erase periods.

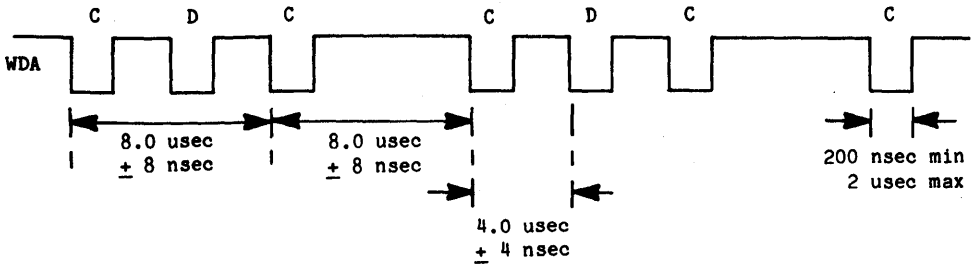
WRT/ should not be asserted less than 250 nanoseconds after HSLT/ changes state. Trim erase is energized approximately 425 microseconds after the leading edge of the WRT/ signal and de-energized approximately 950 microseconds after the trailing edge of WRT/. Thus, the tunnel erase gaps provide a guard band, which allows for moderate, mechanical tolerances to be used without affecting the interchangeability of diskettes between drives. Data reliability is enhanced.

3.3.2.7 Write Data Timing

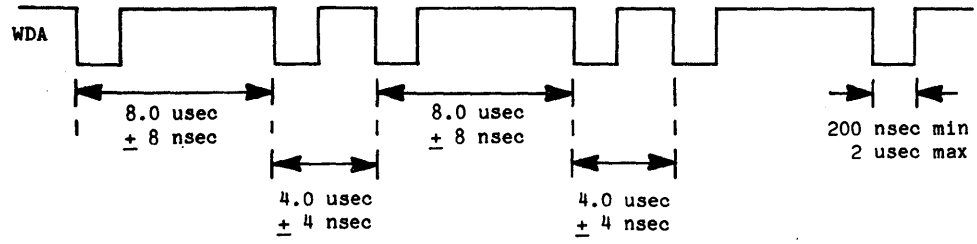
The interface WDA/ line passes the encoded Write Data to be recorded on the diskette. The negative-going edge of each WDA/ pulse causes a reversal of the current flowing through the write head, thereby recording a flux transition on the diskette.

Write data pulse widths must be in the range of 200 nanoseconds to two microseconds. Write Data is enabled when the interface Write Gate signal (WRT/) is true, provided a Step operation is not in progress or the diskette is not write protected. The leading edge of each pulse must be within 0.1% of the data cell time as shown in Figure 3-8, Write Data Timing.

Write Data (WDA/) must be available no later than eight microseconds after WRT/ is asserted, and WRT/ must be terminated no longer than eight microseconds after the last state change of WDA/. Trim erase of Write Data begins approximately 425 microseconds after WRT/ is asserted. Trim erase continues for approximately 950 microseconds WRT/ is terminated; see Figure 3-10.



Write Data Timing for FM @ 125 Kbits/sec



Write Data Timing for MFM @ 250 Kbits/sec

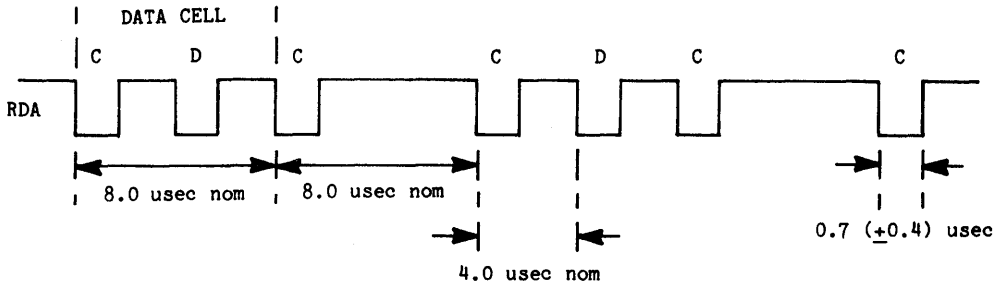
Figure 3-8. Write Data Timing

If write precompensation is included in the host controller, a reduction in peak shift and a corresponding increase in decoding margins can be expected. Precompensation should be in the range of from 8% to 10% of a data cell and should be used on the inner tracks only (track numbers greater than 44).

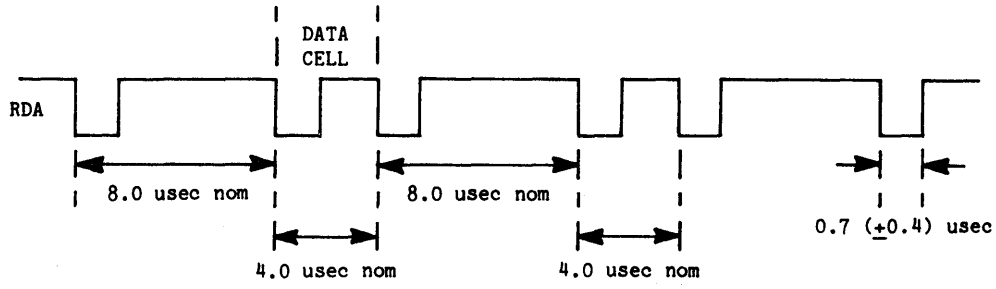
3.3.2.8 Read Data Timing

The Read Data (RDA/) line transmits composite data from the selected drive to the host controller. The data consists of a series of low-true pulses, one pulse for each flux transition recorded on the diskette. The width of each data pulse is 0.7 (±0.4) microseconds. The leading edge of the pulse represents the true position of the flux transitions on the diskette surface and should always be used as the time reference. Read data peak shift is dependent on the data pattern, encoding method, and data transfer rate. Worst case peak shift conditions using MFM encoding are shown in Figure 3-9.

Read Data (RDA/) is valid 1100 microseconds after WRT/ is terminated or 250 nanoseconds after HSLT/ changes state if WRT/ has been terminated for at least 1100 microseconds; see Figure 3-10.



Read Data Timing for FM @ 125 Kbits/sec



Read Data Timing for MFM @ 250 Kbits/sec

Figure 3-9. Read Data Timing

The Read Data output signal is inhibited during a write operation and also during the trailing trim erase delay and read amplifier recovery time. A total of 1100 microseconds is required before the output data is valid. The timing constraints on RDA are shown in Figure 3-6, Conventional Mode Stepper Timing.

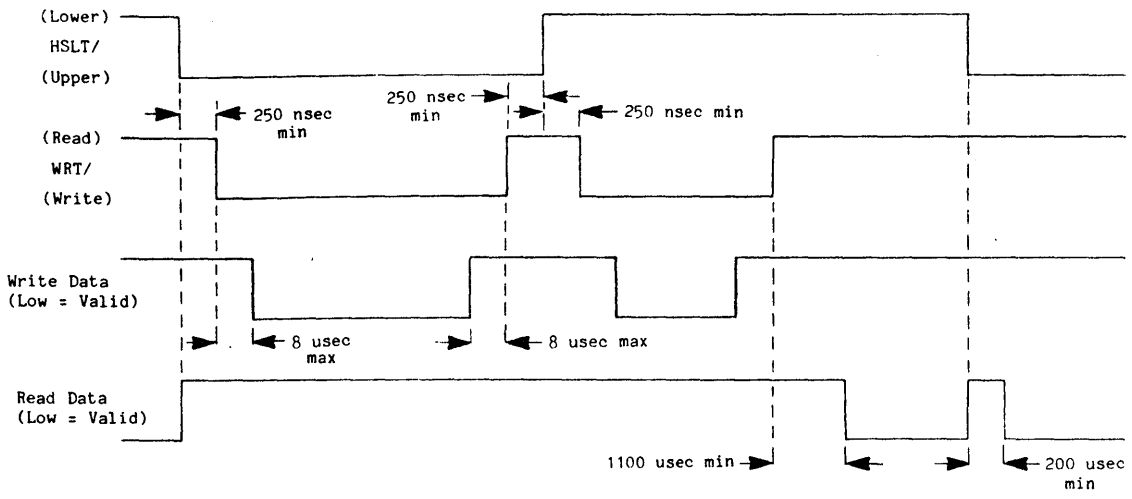


Figure 3-10. Head Select and Read/Write Control Timing

3.4 FUNCTIONAL THEORY OF OPERATION

This section describes the operation of the 1115-Series Flexible Disk Drive from a functional viewpoint. The circuits referenced in this section are described in detail in Section 3.5.

The major Drive Functional Elements of the drive are shown in Figure 3-11.

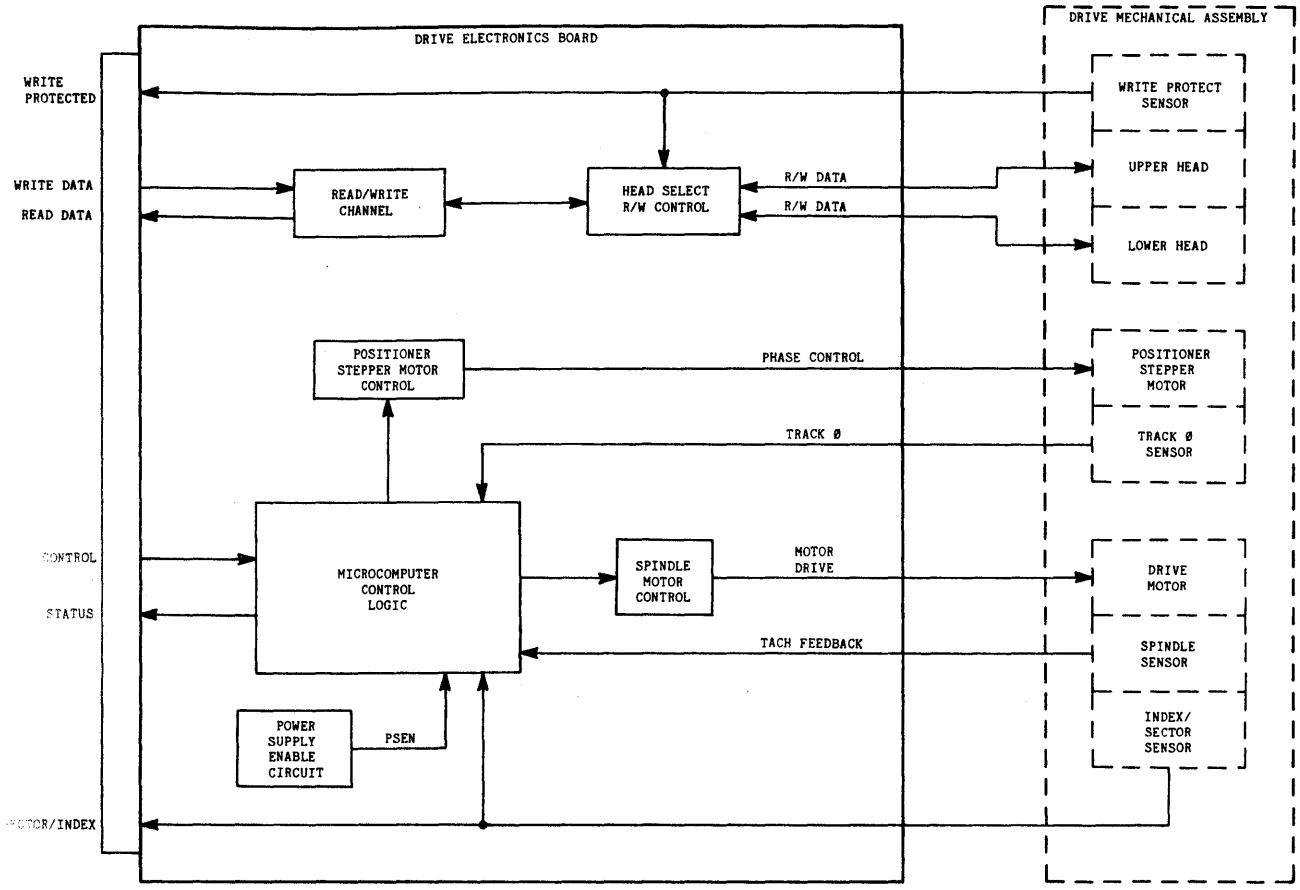


Figure 3-11. Drive Functional Elements

3.4.1 Functional Overview

When power is applied to the drive, a power-on reset signal initializes the drive's Microcomputer and clears selected control logic circuits. Next, the Microcomputer performs a Restore operation, which positions the read/write head at Track Ø. The restore operation is done whether a diskette is inserted in the drive or not.

When a diskette is inserted into the drive and the access door is closed, the diskette is rotated (for centering purposes) and clamped to the spindle. When the controller asserts the interface Motor On signal (MTRN/), the spindle motor accelerates the diskette to its nominal speed of 300 RPM, and maintains that speed. At this point the drive can be selected by the controller. Spindle motor speed is maintained until the Motor On signal is dropped, the disk access door is opened, or power is removed.

The drive is selected by the host controller asserting the appropriate Drive Select signal (there are various jumper options available for this function). From this "selected" state, the controller can then direct the drive into seek mode, read or write mode, or de-select the drive.

The drive goes into seek mode upon receipt of one or more Step pulses from the host controller. The positioner moves the head one track per Step pulse, in the direction (from Track Ø initially or from the previous track) specified by a Direction signal. At the conclusion of the seek, the drive returns to its "selected" state, as above.

If the host controller asserts the Write Gate signal (assuming that the drive is not seeking and that no write unsafe condition exists), the drive will go into write mode. Write data from the controller (in the form of a coded stream of pulses) is received by the drive. The leading edge of each pulse reverses the direction of current flowing in the head windings, recording a flux reversal on the diskette (on the track under the head) for each input data pulse. When the Write Gate signal is dropped, the drive returns to the "selected" state.

If Write Gate is not asserted and the drive is not seeking, it will automatically be in read mode. The drive's read electronics senses the flux reversals on the track under the head. That read signal is amplified, peak detected, digitized, and then output to the controller as a stream of read data pulses, nominally identical in timing to the original write data pulses. All data encoding and decoding is performed by the controller.

The Microcomputer in the drive's control logic constantly monitors the drive's status. Various possible fault conditions are detected, the drive's status is indicated to the controller, and any operation that could jeopardize data is prevented.

3.4.2 Detailed Functional Theory

3.4.2.1 Control Logic (Microcomputer)

a. Initial Sequencing

When power is applied to the drive, the Microcomputer and its associated control logic are reset. Next, the Microcomputer automatically steps the read/write head outward until the Track Ø sensor output goes true. If the head is already positioned at (or behind) Track Ø, the head is stepped in until the sensor is no longer seen and then restored to Track Ø. Positioning the head to Track Ø occurs whether a diskette is inserted in the drive or not. Thus, upon power-up, the host controller does not need to position the read/write head but simply waits for the interface Track Ø signal to go true. The time (maximum) for this process is 700 milliseconds.

When the head is positioned at Track Ø, the drive's Microcomputer asserts drive control signal OUTPUT ENABLE/. Until this occurs, the user's input commands are ignored; and the drive's output signals are disabled.

When a diskette is inserted in the drive, the access door is closed, and the diskette is rotated for proper seating, the diskette is considered Ready. Then, if the drive is selected, the drive motor is up to speed, and at least one index pulse has been detected, the drive is Ready. At this time, the drive is prepared to accept read, write, and step commands from the host controller.

b. Positioner and Control

In response to an interface Step Command (STEP/), the drive's Microcomputer generates four sequential signals, identified as Phase 1, Phase 2, Phase 3, and Phase 4, which are applied to the stepper motor to cause the track-to-track positioning of the read/write head(s).

1) Positioner: The positioning mechanism uses multiple steps per track, and employs a precision lead screw and a low friction, long life, jeweled follower.

   A temperature compensating, single-point head reference system further increases accuracy.

2) Control: The positioner is activated by the four-phase stepper motor such that each Step Command causes the stepper motor to move/turn two incremental steps, corresponding to one track movement. The track-to-track access time is six milliseconds.

3) Special Considerations: If more Step pulses are issued than there are available tracks, the following can occur:

- If stepping is toward the inner/higher tracks and the head moves beyond the last allowable track, eventually the head will reach a mechanical lift ramp and then a mechanical stop. The stepper motor will continue to rotate until all the Step pulses are issued. The host controller (or host software) would then issue a seek to Track Ø to restore the head to a known track location. The jeweled follower drops into the groove in the lead screw, and the head is restored to Track Ø. Normal read/write and seek operations would be resumed.

- If the step direction is toward Track Ø and the number of Step pulses issued attempts to move the head beyond Track Ø, the drive will stop on Track Ø and ignore the extra pulses.

- If a step out command is issued when the head is at Track Ø, the positioner will remain at Track Ø.

If, during normal operation, the host controller suspects a possible positioning error has occurred, the controller should step the drive out until the interface Track Ø signal goes true.

c. Spindle Drive and Control

The spindle is driven by a DC drive motor via a belt and pulley. The speed reduction from motor to spindle is 8-to-1. A closed loop servo regulates the drive motor speed.

The drive motor is controlled by the interface Motor On (MTRN/) signal from the host controller. A drive with power on, a diskette inserted, and the access door closed is accellerated to operating speed when the Motor On signal is true.

Spindle speed is monitored at the spindle pulley by an LED/photosensor pair, which is interupted by flags integral to the spindle pulley. The sensor output is digitized and sent to the drive's Microcomputer, which utilizes an algorithm to regulate the spindle speed. The Microcomputer then generates a digital (pulse-width modulated) speed control signal, which is applied to an operational amplifier and filter network. The linear output of the op-amp drives a power amplifier, which in turn powers the DC drive motor.

3.4.2.2 Read/Write Data

a. Media

A diskette is comprised of a recording medium held inside a protective jacket. The recording medium typically consists of a polyester disk coated with a formulation of oxides and polymers. The diskette surface has low abrasivity to reduce head wear. The jacket provides an environment that prevents damage from normal handling, and eliminates the buildup of static charges. The jacket lining is a wiping fabric bonded to the inside of the jacket. This wiping material continually wipes dust and other contaminants from the recording surface.

b. Heads

A center-tapped coil wound around the ferrite element provides the write excitation and the read pick-off.

The equivalent magnetic circuit of the read/write head is a slotted-ring magnet structure with a center-tapped coil, as shown in Figure 3-12.

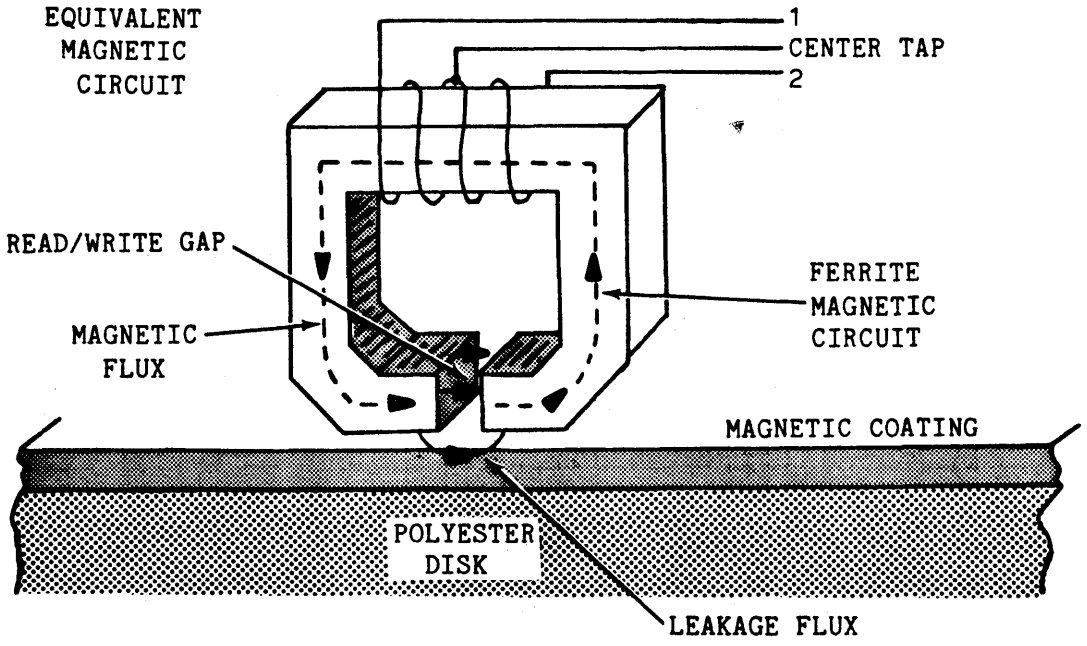


Figure 3-12. Magnetic Head and Media

c. Data Recording

The Magnetic Recording Process is shown in Figure 3-13.

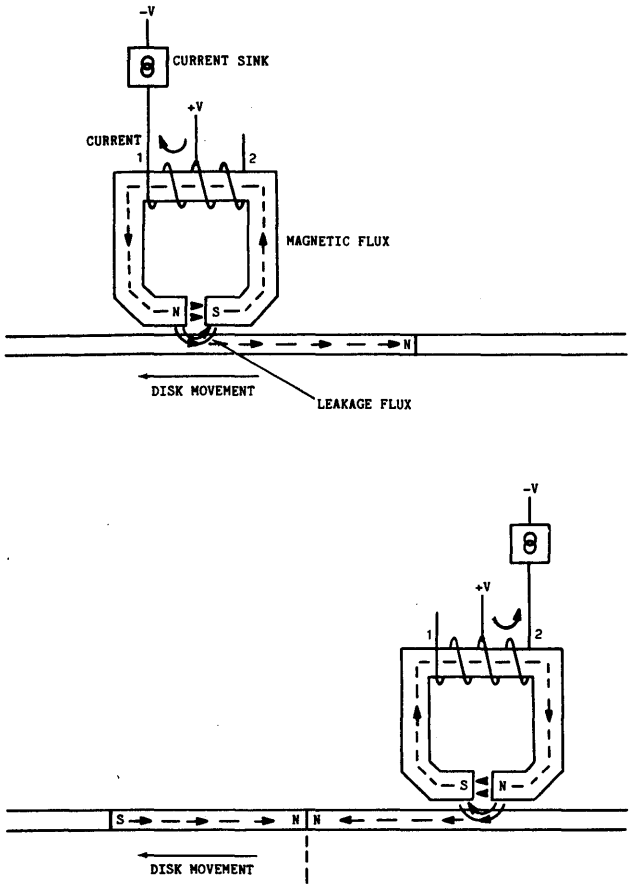


Figure 3-13. The Magnetic Recording Process

When current is passed through half of the head winding, a magnetic induction field is created in the head. At the point where the head gap breaks the magnetic circuit, some of the flux leaks out around the gap, through the magnetic coating on the diskette. When the diskette is moved relative to the head, the area of the diskette surface passing under the head is left magnetized in the same direction as the leakage flux.

When the current is passed through the other half of the head winding, the magnetic flux flows through the head, across the gap, and through the media in the other direction. As may be seen in Figure 3-13, each time the current is switched between the two windings, the magnetic field reverses and a magnetic dipole is recorded in the magnetic coating of the diskette.

The recording process is shown in greater detail in Figure 3-14.

Write data is presented to the drive as a stream of pulses. For each pulse, a flux reversal is to be recorded on the diskette. The pulses are applied to a write flip-flop which changes state on each pulse. The write flip-flop switches the head current, thereby recording magnetic dipoles in the magnetic disk coating.

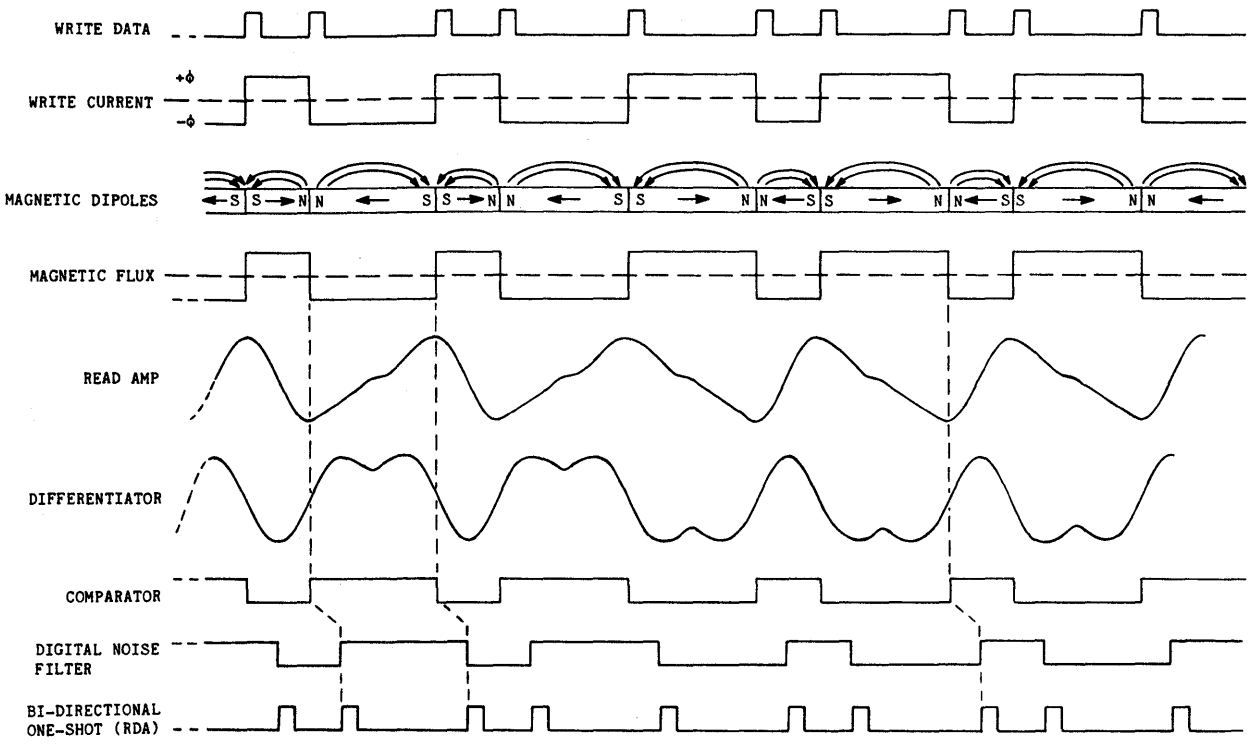


Figure 3-14. Recording Process - Detailed

Each magnetic dipole creates a magnetic field that is external to the magnetic coating itself. The flux of this magnetic field alternates in sign at each switch point as shown. In practice, the changeover is not instantaneous. Rather, finite switching times and finite magnetic transition widths cause the flux reversals to be less well defined.

In the read-back process, the magnetized diskette surface is passed under the head. The head acts as a collector of magnetic flux. As the diskette passes under the head, the alternate-direction fields in the magnetic dipoles produce a changing magnetic flux in the head itself. The head functions as a differentiator (i.e., a voltage is induced across the head windings, which is proportional to the rate of change of flux in the head). The derivative of the actual flux, $d\Phi/dt$ as shown, represents the output. The read signal is developed across both halves of the head and applied via switching diodes to the Read Amplifier.

c. Read/Write

1) Read Channel:

The drive electronics Read Channel processes the head output to produce a stream of read pulses nominally identical in timing to the original write data stream.

Signal Path

The read signal from the data head passes through an Input Clamp, which prevents any transients generated by the write circuit from propagating through the read circuit. The read signal is applied to an Amplifier circuit. The amplified read signal is then processed through a Filter circuit to eliminate noise and to minimize distortion.

Next, the amplified and filtered read signal is applied to a Differentiator circuit. The Differentiator (in conjunction with the Comparator circuit) functions as a peak detector. As a peak detector, the Differentiator identifies each read signal peak with a corresponding "zero-crossing."

The differentiated read signal is filtered, digitized by a Comparator, and then applied to the Digital Noise Filter, which eliminates short-duration, pulse-type noise. The final stage in the Read Channel is a Bidirectional One-Shot, which generates the Read Data signal. The Read Data signal is then output to the host controller.

Read Data consists of a series of low true pulses; one for each flux transition recorded on the media. The pulse width is 0.7 microseconds (plus or minus 0.4 microseconds).

2) Write Channel

Signal Path

Assertion of the interface Write Gate line puts the drive logic into write mode. In write mode, the data received on the interface Write Data line is recorded on the diskette.

The Write Data enters the drive as a stream of pulses. The received pulses are applied to the write flip-flop, which changes state on the leading edge of of each pulse. Each time the flip-flop changes state, the write drivers switch the head current, thereby recording a flux reversal on the diskette for each Write Data pulse.

Writing is permitted only if it is safe to do so. Write control logic enables the write circuits only if:

- Voltage monitor PSEN indicates the regulated +5V and +12V supply voltages are present, and within tolerance.
- The drive is Ready (i.e., a diskette is inserted, the access door is closed and the diskette is clamped, the drive is selected, and the spindle motor is up to speed).
- The drive is not performing a positioning/step operation.
- The diskette is not write protected.

If these conditions are not met, the write control logic disables the write circuits.

3.5 CIRCUIT THEORY OF OPERATION

This section presents a detailed theory of operation of the circuitry in the 1115-Series of 5 1/4-inch Flexible Disk Drives. These circuits are located on the Drive Electronics board.

The circuit descriptions follow a functional approach and are presented in the following order:

Section 3.5.1 Interface, Control, and Status

Section 3.5.2 Sensors

Section 3.5.3 Spindle Motor Control

Section 3.5.4 Positioner Control

Section 3.5.5 Write Channel

Section 3.5.6 Read Channel

Section 3.5.7 Microcomputer-Based Control Logic

Specific sheets of the circuit board schematic diagram are referenced as required; the Schematic Diagram is located in Section VIII of this manual.

The level of circuit analysis is specifically geared to service personnel who will be field-repairing the drive and/or repairing the circuit boards in a central depot. Since service personnel for this sophisiicated level of equipment must already possess a thorough understanding and have experience in both analog and digital circuit theory, relatively trivial circuits are not described in detail. For more detailed information on the integrated circuits used, refer to the appropriate manufacturer's literature.

3.5.1 Interface, Control, and Status

3.5.1.1 Interface Connection

Interface connector J1 provides signal interconnection between the disk drive and the host controller; see Table 3-1 in Section 3.3.2. All interface lines are low true with the following logic levels:

True = Logic Ø = 0.0V to 0.4V

False = Logic 1 = +2.5V to +5.25V

3.5.1.2 Interface Signal Processing

There are a total of seventeen TTL-compatible interface lines on connector J1.

a. Inputs: Up to thirteen signals (two are jumper-selectable) are terminated by 220/330 ohm terminator network RN1. Network RN1 provides the proper input signal termination. Systems having more than one drive on a daisy-chain interface cable must have RN1 installed in the last drive on the cable; RN1 is removed from the other drives. All the terminated signals are received by inverting Schmitt trigger gates U1 and U5. Schmitt triggers are used on the input lines to provide noise immunity.

b. Outputs: Up to six signals (two are jumper-selectable) can be used as outputs and are passed to the interface via tri-state buffer inverter U10. Gate U10 is used as a control gate, which is enabled when the drive is Selected and the microcomputer-generated OUTPUT ENABLE/ signal is true.

3.5.1.3 Input Signals (Sheet 3)

The input lines at connector J1 provide the host system with direct control over the drive.

MTRN/ (Motor On)

When the interface MTRN/ signal is low (true), that low is inverted by U5 to MTRN. The high MTRN signal is applied to Microcomputer U11 (Sheet 8) input pin 6. Microcomputer control logic accelerates the spindle motor and then maintains it at operating speed as long as MTRN/ is true.

The jumper-selectable options available for the Motor On signal were described in Table 3-1 and will not be repeated here.

3.5.1.3 Input Signals (continued)

DS1/ through DS4/ (Drive Select)

The jumper-selectable options available for the Drive Select signals were described in Table 3-1 and will not be repeated here.

When any one of the four DS (Drive Select) lines is asserted and the associated select jumper is installed (or if W5 is installed in a drive in a single-drive system), the resulting low level is passed to input pin 3 of inverting Schmitt trigger gate U1. The inverted output (U1 pin 4) becomes the SEL (Selected) signal and is:

a. Sent to Microcomputer U11 (Sheet 8), pin 8.

b. Applied to the D-input of Step flip-flop U13 (Sheet 8).

Two jumper-selectable options are available for the SEL signal:

a. If W11 (Sheet 5) is installed (W13 and W15 omitted), the SEL signal is applied to inverter U7 pin 5. The inverted output signal controls the Front Panel LED, which will light when the drive is Selected.

b. If W12 (Sheet 5) is installed (W10 and W14 omitted), and the interface INUSE/ signal is true, the disk access door will be locked when the drive is Selected.

   When the drive is Selected, the positive-going edge of the SEL signal clocks flip-flop U3, thereby loading the logic level of the INUSE signal into U3. Output pin 9 (gated by U19 with the DOOR signal) controls the Door Lock Solenoid.

The SEL signal is inverted to SEL/ by inverter U1 pin 2.

a. The SEL/ signal goes to input pin 5 of inverter U2 (Sheet 6). The output at pin 6 is a function of WRT, WPT, SEL/, and SBSY, and functions as a Write Enable signal. This signal controls head-select inverters U6, write current driver U3, erase current drivers U9, and Write Busy (WBSY) generator Q3.

b. The SEL/ signal is also applied to pin 15 (the output-enable pin) of gate U10 (Sheet 3). Gate U10 is a tri-state device, which is enabled only when the OUTPUT ENABLE/ signal is true and the drive is Selected; i.e., when SEL/ is low (true).

   During initial power-up, the OUTPUT ENABLE/ signal is false, disabling the drive's output signals. At the completion of the sequence (when Track Ø is reached), the OUTPUT ENABLE/ signal goes true, and the drive is made available to the user.

3.5.1.3 Input Signals (continued)

HSLT/ (Head Select)

The Head Select signal is used for dual head drives only. The HSLT/ signal from the host controller is received on the interface at J1 pin 32 as a signal level. A high level selects the lower head and vice versa. Head Select operation is explained in detail in Section 3.5.5.2, Head Select Circuit.

HDLD/ (Head Load)

NOTE

Enclosed within the dotted lines on schematic Sheet 5 are the components only installed on versions of the board that use the Head Load Solenoid and Door Lock options.

The HDLD/ signal on J1 pin 2 is applied to pin 5 of inverter U1. The output, HDLD, is applied to Microcomputer U11 (Sheet 8) input pin 9 via jumper-option W19 (W20 and W24 removed). Microcomputer control logic asserts the HEAD LOAD SOL signal at pin 29 when MTRN is true and either HDLD is true or the drive is Selected. The HEAD LOAD SOL signal is gated with the the normally high PWR ON RESET/ signal by U19. Output pin 3 controls the Head Load Solenoid.

The Head Load function has two selectable options, which are not controlled by the interface Head Load signal.

a. If jumper W20 (Sheet 8) is installed with W19 and W24 removed, Microcomputer control logic ensures that the head will load when MTRN is true and the drive is Selected.

b. If jumper W24 (Sheet 8) is installed with W19 and W20 removed, Microcomputer control logic ensures that the head will load when either MTRN is true or the drive is Selected.

STEP/ (Step Command)

The interface STEP/ signal is inverted twice by U5. The resultant signal, also identified as STEP/, is applied to clock input pin 11 of Step flip-flop U13 (Sheet 8). If the drive is Selected, then the D-input of U13 is high. That high is clocked into the flip-flop by the Step pulse, and output pin 9 goes high. When pin 9 goes high, the positive-going edge clocks DIRN (Step Direction) into U12. Both the Step and the Step Direction outputs are applied to Microcomputer U11 (Sheet 8) at input pins 3 and 2 respectively. Before the next Step pulse is received, the Microcomputer asserts a reset pulse at output port PC6 (pin 14), which resets Step flip-flop U13.

3.5.1.3 Input Signals (continued)

DIRN/ (Step Direction)

The interface DIRN/ signal is inverted to DIRN by U5 and is passed to the D-input of Direction flip-flop U12 (Sheet 8). When a Step Command is received and the drive is Selected, Step flip-flop U13 sets. When U13 sets, the positive-going edge at output pin 9 clocks DIRN (Step Direction) into U12. Thus, the direction of motion of the heads is latched into U12 at pin 5 and is independent of any further changes on the Direction line until another Step pulse is received. The output of the flip-flop is applied to Microcomputer U11 (Sheet 8) input pin 2.

One jumper option is available on the DIRN/ line:

If W28 (Sheet 3) is installed with W27 removed, the appropriate head is selected via the interface DIRN/ line; see Section 3.5.5.2, Head Select Circuit.

INUSE/ (In Use)

The options available for the INUSE/ signal were described in Table 3-1, and will not be repeated here.

The INUSE/ signal is applied to pin 11 of inverter U1 (Sheet 3). The output, INUSE, can have one of three destinations:

a. If W14 is installed, then INUSE is applied to pin 6 of U19 and is gated with the DOOR (high when closed) signal. Output pin 5 activates the Door Lock Solenoid.

b. If W15 is installed, then INUSE is applied to inverter U7 pin 5. U7 pin 6 controls the Front Panel LED. When INUSE/ is true, the Front Panel LED illuminates.

c. If neither W14 nor W15 are installed, then INUSE is applied to the D-input of flip-flop U3. The D-input is clocked into U3 by the positive-going edge of the SEL signal; i.e., when the drive is Selected. If W12 is installed, the output of U3 at pin 9 is applied to U19 pin 6 and is gated with the DOOR signal (which is high when closed) signal. The resultant output at U19 pin 5 activates the Door Lock Solenoid.

   If W13 is installed, the output of U3 at pin 9 is applied to inverter U7 pin 5 via jumper W13. The inverted output at pin 6 controls the Front Panel LED (thus INUSE/ will light the LED on a selected drive).

3.5.1.3 Input Signals (continued)

DRLK/ (Door Lock)

NOTE

Enclosed within the dotted lines on schematic Sheet 5 are the components only installed on versions of the board that use the Door Lock and Head Load Solenoid options.

a. Door Lock Options:

NOTE

In the signal description below, the apparent inconsistency of the mnemonics is due to the multiple uses of various signals; specific usage is determined by jumper selection.

The DRLK/ signal is applied to pin 5 of inverter U1. Output HDLD at U5 pin 6 is applied to pin 6 of gate U19 (Sheet 5) via jumper-option W10 (W12 and W14 removed). The HDLD signal is then gated with the DOOR (high when closed) signal by U19. The output at pin 5 controls the Door Lock Solenoid.

The Door Lock function has three jumper-selectable options; these options are not controlled by the interface DRLK/ signal.

1) W12 Option (Sheet 5) with W10, W14, and W29 removed: If the INUSE/ signal is true and the drive is Selected, the Door Lock Solenoid is activated.

   When the drive is Selected, the positive-going edge of the SEL signal clocks Door Lock flip-flop U3, thereby loading the logic state of the INUSE signal into the flip-flop. The output, at pin 9, is gated by U19 (via W12) with the DOOR (high when closed) signal. Output pin 5 controls the Door Lock Solenoid.

2) W14 Option (Sheet 5) with W10, W12, and W29 removed: If the INUSE/ signal is true, the Door Lock Solenoid is activated.

   The IN USE signal is gated by U19 (via W14) with the DOOR (high when closed) signal. The output at pin 5 controls the Door Lock Solenoid.

3) W29 Option (Sheet 5) with W10, W12, and W14 removed: If the drive is Selected and the disk access door is closed, the Door Lock Solenoid is activated.

3.5.1.3 Input Signals (continued)

b. Door Lock Solenoid Driver:

The door lock solenoid driver circuit (comprised of a transistor and its associated bias and timing components) generates a high current pulse to energize the solenoid and then provides a low holding current to maintain the solenoid in the energized state.

1) In the unlocked condition, output pin 5 of U19 is high; and transistor Q10 is off. No current flows in the circuit.

2) If the disk access door is closed (U19 pin 7 is high) and U19 pin 6 goes high, output pin 5 goes low. Capacitor C53 discharges immediately and then charges again via resistors R103 and R104. While C53 is charging, Q10 is turned on; and approximately +11.5V energizes the solenoid. After the RC network times out, Q10 shuts off, thereby switching off the high current. In this way, an approximately ten-millisecond, high current pulse is generated to energize the Door Lock Solenoid.

As long as the door is closed, U19 pin 5 stays at a logic low. That low forward biases diode CR39 (via the solenoid and resistor R102) and keeps the solenoid energized with a low, holding current.

WDA/ (Write Data)

Write Data from the host controller is received on the interface at J1 pin 22 as a stream of digital pulses. For each digital pulse, a flux reversal is written on the diskette. Write Channel operation is explained in detail in Section 3.5.5.

WRT/ (Write Gate)

The WRT/ signal is applied to pin 11 of inverter U5 to become the WRT signal. The WRT signal is passed to pin 9 of open-collector buffer U6 (Sheet 6). The output at pin 6 is a function of WRT, WPT, SEL/, and SBSY and is called the Write Enable signal. Write Enable controls the operation of head-select inverters U6, write current driver U3, erase current drivers U9, and Write Busy (WBSY) generator Q3. Operation of the Write Channel is explained in detail in Section 3.5.5.

3.5.1.4 Output Signals

The six output lines appearing at connector J1 provide the host controller with continuous status and data signals when the drive is Selected.

All six output signals are passed to the interface via gate U10.

Gate U10 is a tri-state buffer inverter, which is enabled only when the microcomputer-controlled OUTPUT ENABLE/ signal is true and the drive is Selected. When the drive is not Selected, U10 is not enabled and the high impedance output state of the gate effectively removes the outputs from the Bus.

During the initial power-up sequence, The OUTPUT ENABLE/ signal is false, thus disabling the drive's output signals. At the completion of the sequence (when Track Ø is reached), the OUTPUT ENABLE/ signal goes true, thereby making the drive available to the user.

RDY (Ready)

The Ready signal is a signal generated by the drive's Microcomputer that is asserted when the power supplies are within tolerance, the door is closed, the spindle has been rotated for proper diskette centering, the drive is Selected, and the motor is up to speed.

If jumper W18 is installed, the above conditions apply and SBSY (Step Busy) must be false; i.e., the drive must not be performing a step operation for the drive to be Ready.

RDA/ (Read Data)

The RDA/ line at J1 pin 30 transmits Read Data from the selected drive to the host controller. The data consists of a series of low-true pulses, one pulse for each flux transition recorded on the diskette. The host controller then decodes this pulse stream into the actual data. Operation of the Read Channel is covered in detail in Section 3.5.6.

SECP/ (Sector/Index Pulse)

The SECP/ signal goes low (true) at interface connector J1 pin 8 each time a sector hole or index hole is detected as the diskette rotates. The leading edge of the signal should be used as the time reference by the host controller.

TRKØ/ (Track Zero)

This signal at J1 pin 26 is controlled by the drive's Microcomputer; it is set true when the read/write head is positioned at Track Ø and the drive's Microcomputer has placed the stepper motor in the hold mode.

WPT/ (Write Protect)

The two write protect conventions were described in Table 3-1, and will not be repeated here.

DOOR CLOSED/ (Door Closed)

This interface option (jumper W16 installed, jumper W30 removed) places the DOOR CLOSED/ status signal on J1 pin 34.

If W16 and W17 are removed and W35 is installed, the DOOR CLOSED/ status signal appears on J1 pin 6.

Jumper W23 controls the microcomputer-generated Door signal (PC4).

a. Installed: Microcomputer output port PC4 goes low whenever the disk access door is closed. That output is inverted by U8 to become the DOOR CLOSED signal.

b. Removed: A latch circuit, internal to the Microcomputer, is enabled. This circuit monitors and stores/latches any door open event while the drive is deselected. If this occurs, Microcomputer output port PC4 goes high and stays high until the drive is deselected. That output at PC4 is inverted by U8 to become the DOOR CLOSED signal.

DRIVE STATUS (Drive Status)

This optional (jumpers W16 and W30 installed) interface signal on J1 pin 34, indicates the disk access door is closed and the drive is Ready.

If W16 and W17 are removed and W30 and W35 are installed, the DRIVE STATUS/ signal appears on J1 pin 6.

3.5.2 Sensors (Sheet 4)

3.5.2.1 Door Open Sensor

The circuit consists of an LED/Photosensor pair and an inverter.

a. When the disk access door is open, the light emitted by DOOR LED CR25 is blocked by a mechanical flag. Door Sensor Q6 is turned off; and the output voltage, measured at the collector, is high (+5V). That high at the output is inverted by U4 to a logic low at pin 8. This low DOOR signal indicates the door is open.

b. When the disk access door in closed, the mechanical flag is removed. The light emitted by the DOOR LED is detected by Door Sensor Q6, causing it to conduct. The output of Q6, at the collector, approaches ØV. That low at the output of the sensor is inverted by U4 to a logic high at pin 8. This high DOOR signal indicates the door is closed.

The DOOR signal at U4 pin 8 is passed to Microcomputer U11 (Sheet 8) input pin 4 and to Door Lock Solenoid gate U19 (Sheet 5) pin 7.

3.5.2.2 Track Ø Sensor

The circuit consists of an LED/Photosensor pair, a precision voltage comparator, and a stabilizing capacitor.

a. When the read/write head is at Track Ø, the light emitted by the TRKØ LED is blocked by a mechanical flag. The TRKØ Sensor is turned off; the sensor output at the emitter is low; and that low is applied to comparator U20, non-inverting input pin 7. Since the input is negative with respect to the +2.5V reference on comparator pin 6, output TRKØIN/ goes low (true), indicating the read/write head is positioned at Track Ø.

b. When the head is NOT at Track Ø, the mechanical flag is removed. The light, emitted by the TRKØ LED, is detected by the TRKØ Sensor, causing it to conduct. The output of the sensor at the emitter is high, approximately +4.5V. That high at the output is applied to comparator U20, non-inverting input pin 7 and can be measured at TP8-3. Since the input level is positive with respect to the +2.5V reference on comparator pin 6, output TRKØIN/ goes high (false), which indicates the head is NOT at Track Ø.

c. Capacitor C35, in U20's feedback loop, is used to suppress oscillations that occur as the comparator changes state.

The TKØIN/ circuit output appears at U20 pin 1 and is passed to Microprocessor U11 (Sheet 8) input pin 7.

3.5.2.3 Write Protect Sensor

The Write Protect sensor circuit consists of an LED/Photosensor pair and a precision voltage comparator.

a. Write Protected with a tab: Jumpers 32 and W33 installed, W31 omitted, and a 100K-ohm resistor at R63. (This is the "standard" write protect convention.)

   1) When the diskette is write protected, a tab is placed over the cutout along the edge of the diskette jacket. The light emitted by WPT LED CR37 is blocked by the tab, the WPT Sensor is turned off, and its collector output is high, +5V.

      The high level at the output of the sensor is applied (via W32) to comparator U20, input pin 5. Since the input to the comparator is positive with respect to the +2.5V reference on pin 4, output WPT goes high, indicating that the diskette is write protected.

   2) When the diskette is NOT write protected (i.e., when the tab is removed), operation of the circuit is the inverse of that described in preceding paragraph a-1.

b. Write Protected without a tab: Install jumper W31, omit jumper W32, first cut the etched jumper and then install a 100K-ohm resistor for W33, and install a zero-ohm resistor for R63.

   1) When the diskette is to be write protected, the tab covering the cutout along the edge of the diskette jacket is removed. The light emitted by the WPT LED is detected by the WPT Sensor, causing it to conduct. The output of the sensor at the emitter is high, approximately +4.5V.

      That high at the output is applied (via W31) to comparator U20, input pin 5. Since the input to the comparator is positive with respect to the +2.5V reference on pin 4, output WPT goes high, which indicates that the diskette is write protected.

   2) When the diskette is NOT write protected (i.e., when the tab is placed over the cutout), operation of the circuit is the inverse of that described in preceding paragraph b-1.

Write Protect Sensor Circuit output WPT (Write Protect) appears at U20 pin 2. The WPT signal is sent to U2 pin 9 (Sheet 6) as a write control signal and to interface output control gate U10 (Sheet 3).

3.5.2.4 Spindle Tachometer Feedback Sensor

The circuit consists of an LED/Photosensor pair, a precision voltage comparator, a differentiator circuit, and an inverter.

a. Spindle speed is sensed by an optical tachometer that utilizes an LED and Photosensor. As the light from the Spindle LED is interrupted by flags on the spindle pulley, the Spindle Sensor is alternately turned off and on, causing its collector to alternately switch from +5V to 0V. Comparator input pin 9 then alternately switches from positive to negative with respect to the +2.5V reference on pin 8. The resulting comparator output is a pulse train, switching from +5V to 0V. Feedback resistor R84 provides circuit hysteresis.

b. The comparator output is passed through a differentiator circuit consisting of capacitor C37 and resistor R81. This network "shapes" the signal. Only the positive-going pulses of the differentiated signal are passed on to U4. The negative-going spikes of the differentiated signal forward bias diode CR35.

c. The positive-going pulses, applied to inverter U4 pin 11, appear as the MOT TACH/ signal at pin 10.

The MOT TACH/ signal is passed to the drive's Microcomputer, input pin 37, and to Motor Control flip-flop U13, reset pin 1 (both on Sheet 8).

3.5.2.5 Sector/Index Sensor

The circuit consists of an LED/Photosensor pair, an RC network, and two inverters.

a. The Index Sensor detects the light (emitted by the Index LED) passing through the index hole and sector holes in the diskette, as the diskette rotates. The Index Sensor assembly output is a negative-going pulse for each hole sensed.

b. These pulses are applied to input pin 3 of inverter U4.

c. Positive feedback, which produces hysteresis, is achieved via resistor R3. Hysteresis prevents the circuit from responding to small discontinuities in the input signal.

The circuit output at U4 pin 4 is the signal SECP (Sector/Index Pulse). The SECP signal is passed to Microprocessor U11 (Sheet 8) input pin 4 and to interface output control gate U10 (Sheet 3).

3.5.3 Spindle Motor Control (Sheet 5)

The Spindle Motor Control circuit is comprised of an LED/photosensor pair, a microcomputer-generated control signal, and a spindle motor drive circuit. Spindle speed is maintained at 300 RPM.

3.5.3.1 Sensor Assembly and Control Logic

The MOT TACH/ signal (refer to Section 3.5.2.4, Spindle Tachometer Feedback Sensor) is sent to Microcomputer U11 (Sheet 8), input Port PA1 (pin 37). The Microcomputer applies the input pulse rate to the algorithm which regulates the spindle motor speed. The Spindle Motor Control signal appears at output Port PB7 (pin 22) and is applied to the spindle drive circuit.

3.5.3.2 Spindle Motor Drive Circuit

The spindle motor drive circuitry consists of a flip-flop, an inverter, a comparator operating as a filter and amplifier, and a power amplifier (with a control gate).

a. The motor control signal is applied to the D-input (pin 2) of motor control flip-flop U13 and is clocked into the flip-flop by the inverted CNTR signal. The flip-flop is reset by the MOT TACH/ pulse.

b. The output of flip-flop U13 at pin 6 is inverted by buffer U7.

c. Comparator U20 operates as a two-pole, low-pass filter and as an amplifier.

   The input to the comparator circuit is a square wave; however, the output at pin 13 is a linear signal that drives power amplifier Q9 (a Darlington pair transistor). This conversion from a pulse-width modulated digital signal to an analog signal reduces the noise that would normally be generated by a digital motor-control signal.

d. The power amplifier consists of Darlington pair transistor Q9 with associated bias and filter components.

   Resistor R87 is a convenient point to monitor the spindle motor current. Diode CR36 protects Q9 from the inductive kick-back caused by commutation.

The power amplifier circuit is controlled by the MOT/ signal. When MOT/ is low, power amplifier Q9 is enabled.

The Spindle Motor Control signal regulates the spindle drive circuit by slowing down or speeding up the spindle motor.

a. If the spindle speed is too slow:

   Output Port PB7 (pin 22) goes high. That high, applied to the D-input of motor control flip-flop U13, sets the flip-flop when clocked by the inverted CNTR signal. Output pin 6 goes low and stays low until the next MOT TACH/ pulse resets the flip-flop. The low output at pin 6 is inverted to a high by inverter buffer U7. The high, applied to the non-inverting input of U20, causes output pin 13 to go high. That high turns on Darlington pair Q9, and the spindle motor starts to accelerate.

b. If the spindle speed is too fast:

   Output Port PB7 switches low. That low level is applied to the D-input (pin 2) of flip-flop U13, which switches the output at pin 6 to a high when clocked by the inverted CNTR signal. The high output at pin 6 is inverted to a low by inverter buffer U7. The low applied to the non-inverting input of U20 causes output pin 13 to go low. The low turns off Darlington pair Q9 and the spindle motor starts to decelerate.

3.5.4 Positioner Control (Sheet 5)

The Positioner Control circuit performs the stepping function and consists of Step and Direction logic, microcomputer-generated control logic, power drivers, and a holding circuit.

3.5.4.1 Step and Direction Logic

a. Step Logic: The interface STEP/ signal (Sheet 3) is inverted twice by U5. The resultant signal (U5 pin 8) is then applied to clock input pin 11 of Step flip-flop U13 (Sheet 8). If the drive is Selected, the D-input of U13 is high. That high is clocked into the flip-flop by the Step pulse, and the output at pin 9 goes high. When pin 9 goes high, the positive-going edge clocks Direction flip-flop U12. Before the next Step pulse is received, U13 is reset by the Microcomputer U11 (Sheet 8) output signal at pin 14 applied to flip-flop reset pin 13.

b. Direction Logic: The DIRN/ signal (Sheet 3) is inverted to DIRN by U5 and is passed to the D-input of Direction flip-flop U12 (Sheet 8). When the Step flip-flop output at pin 9 switches high, the positive-going edge clocks DIRN into flip-flop U12. In this way, the intended direction of motion of the heads is latched into U12 at pin 5. Any changes on the Direction line are ignored until another Step pulse is received.

3.5.4.2 Positioner Control Logic

The latched Step output (U13 pin 9) and the latched Step Direction output (U12 pin 9) are applied to Microcomputer U11 at input pins 3 and 2 respectively. Given the Step Command and the Direction, the drive's Microcomputer controls the balance of the step operation.

There are two modes of stepping (conventional and burst). Selection of the appropriate step mode is made by the Microcomputer. Mode determination is based on the Step pulse rate and does not affect the circuit descriptions.

The drive's Microcomputer asserts the necessary phase, logic, and hold outputs via Port B to position the head at the desired track.

a. Phase Control: The on-board Microcomputer generates four phase-control signals. These signals appear at output ports PB1 through PB4 and are applied directly to the D-inputs of Step register U14. The D-inputs are transferred to the Q-outputs on the positive-going edge of the inverted CNTR pulse applied to CK input pin 9.

   Gate U8 ensures that Phase 2 is asserted during the time that the Power-On Reset signal is true.

b. Logic Control: The Step Busy signal at Port PB6, like the phase-control signals, is also clocked into Step register U14 by the inverted CNTR signal. The output, SBSY, appears at pin 12 of U14.

   The SBSY signal is applied to write control inverter buffer U7 pin 9 (Sheet 6). The output at pin 8 is a function of WRT, WPT, SEL/, and SBSY, and is identified as the Write Enable signal. Write Enable controls the operation of head-select inverters U6, write current driver U3, erase current drivers U9, and Write Busy (WBSY) generator Q3. The SBSY signal ensures that a write operation is not attempted while the drive is stepping. The Write Channel is explained in detail in Section 3.5.5.

c. Holding Control: If, after a specified delay, no further Step Commands are received, output port PB5 (the HOLD signal) is asserted; and the holding phase is entered.

d. Timing Control: The circuit clock pulse for the control logic timing is generated by Microcomputer U11 at CNTR output pin 21 and is inverted by U1 before clocking Step register U14.

3.5.4.3 Power Drivers

The power drivers amplify the drive signals to the stepper motor.

a. Power driver U18 (Sheet 5) is always enabled since the +5V regulated supply voltage is applied to enable input pin 14. The power driver passes the four phase-control signals from Step register U14 to the outputs. Those four open-collector outputs drive the stepper motor.

b. Internal to the chip are four output diode clamps. These diodes are connected (via pins 2 and 7) to the cathode of 20V-Zener CR33. Since the anode of CR33 is tied to the +12V motor supply voltage, the turn-off transient is limited to about +32V.

3.5.4.4 Positioner Holding Circuit

A reduced hold current is supplied to the stepper motor when the HOLD signal is asserted.

a. When stepping the HOLD signal is low (false). That low is applied to open-collector buffer U6. The low output at pin 12 turns on Darlington pair transistor Q8 to saturation, thereby providing +12V from the power supply to the center-taps of the stepper-motor windings. Diode CR32, in the holding circuit, is reverse biased.

b. When the drive is in the holding mode, the HOLD signal is high (true). That high, applied to buffer U6, allows output pin 12 to go high, turning Q8 off completely. Diode CR32 is forward biased, which places +5V, via resistor R65, on the center-taps of the stepper-motor windings. This is done to reduce power consumption in the stand-by mode.

3.5.5 Write Channel (Sheet 6)

Write Data from the host interface is received by the Write Channel as a stream of pulses. Each pulse causes the current flowing through the write head to be reversed. As a result, for each Write Data pulse received on the interface, a flux reversal is recorded on the diskette.

NOTE

The format and encoding schemes are determined by, and actually performed in, the host controller. The Write Channel records one flux reversal for each (encoded) pulse.

Figure 3-15 is a block diagram of the Write Channel. The Write Channel consists of a power supply enable circuit, a read/write switch, a head select circuit, write control logic, write current driver, and erase current drivers.

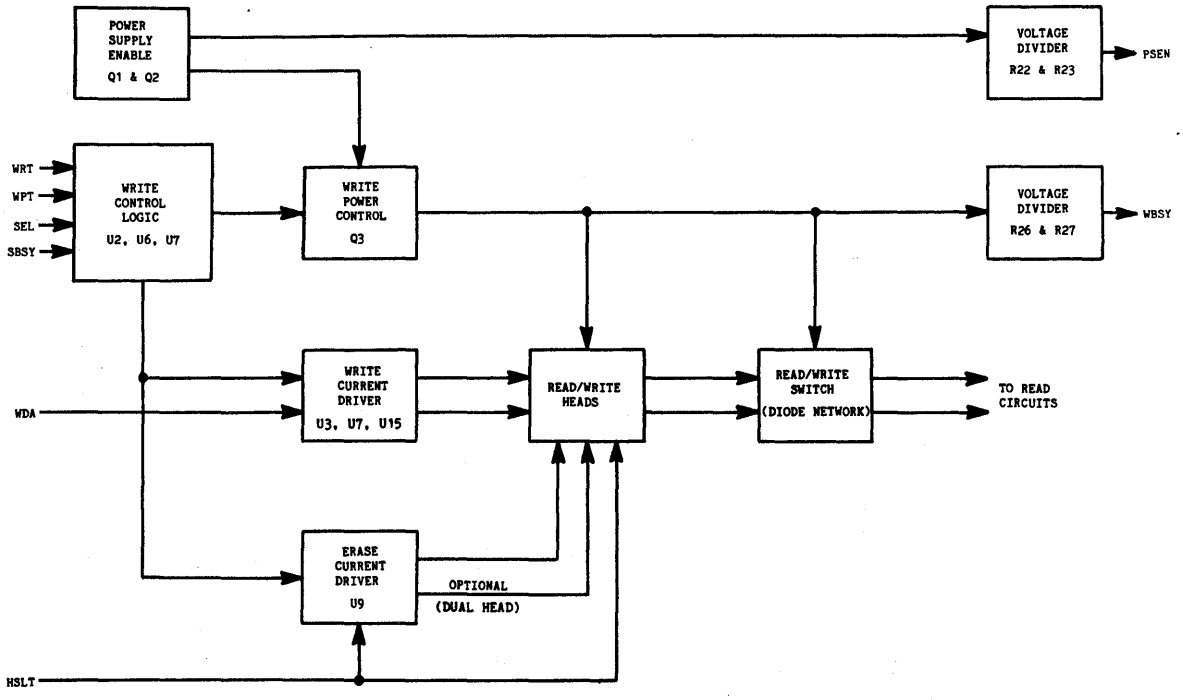


Figure 3-15. Write Channel Block Diagram

3.5.5.1 Power Supply Enable Circuit

The Power Supply Enable circuit consists of transistors Q1 and Q2 and associated biasing components.

When power is applied to the drive, the regulated +5V power supply voltage rises to its operational level. Transistor Q2 conducts as soon as its base voltage exceeds +3.4V (i.e., the 2.7V Zener voltage of CR5 plus Q2's 0.7V base-emitter drop). When the collector current of Q2 drops 0.7V across resistor R18, transistor Q1 conducts, thereby providing +12V (if the +12V is present) to the remaining circuit elements. The +12V (supplied by Q1) is applied to the voltage divider consisting of resistors R22 and R23. This voltage divider develops a PSEN level of approximately +2.8V.

The PSEN signal is applied directly to the Power-On Reset circuit (Sheet 8); see Section 3.5.7.2b., Support Circuitry.

3.5.5.2 Read/Write Switch

The read/write switch consists of diodes CR11, CR12, CR13, and CR15 through CR21, and resistors R38, R44, R45, and R46.

a. During a write operation, transistor Q3 conducts. The anodes of diodes CR19 and CR20 go to approximately +11.5V, which forward biases both diodes. The voltage at the cathodes of the two diodes is about +10.8V. Since the anodes of diodes CR18 and CR21 cannot rise above the V2 clamp voltage in the read circuits (Sheet 7), both CR18 and CR21 are reverse biased. Reverse biasing CR18 and CR21 effectively isolates the read circuits from the read/write head.

   With transistor Q3 turned on, approximately +10V is applied (via diode CR6 and either head-select transistor Q4 or Q5) to the center-tap of the selected read/write head, thus providing the correct write current to the head.

b. When the read mode is selected, transistor Q3 is turned off; the circuit stabilizes with diodes CR19 and CR20 cut off and all the diodes in the bridge (formed by CR11, CR15, CR18, and CR21) conducting. With the four diodes in the bridge each conducting approximately 0.25 milliamps, the diode bridge provides a low impedance path (for the read signal) to differentiator U17 in the Read Channel (Sheet 7).

   With transistor Q3 turned off, +12V is divided by resistors R41, R42, and R43. This divider produces about 6.7V, which is used in the Read Channel Input Clamp (see Section 3.5.6.1). At the same time, approximately +6V is applied to the center-tap of the selected read/write head via head-select transistor Q4 or Q5, thus providing the correct bias for U17 in the Read Channel.

3.5.5.3 Head Select Circuit

NOTE

The same Drive Electronics board is used for both single and dual head drives. Enclosed within the dotted lines on schematic Sheet 6 are the components not installed on versions of the board used with single head drives.

For dual head drives (1115-4 and 1115-6 models), the interface HSLT/ signal selects the desired head (upper or lower).

a. When the interface HSLT/ signal (Sheet 3) is high, the high is inverted by U1 to HSLT. The low HSLT signal is applied to input pin 1 of open-collector buffer U6 (Sheet 6), which turns on head-select transistor Q4. Transistor Q4 couples write current (from transistor Q3) or read bias (from voltage divider R49, R50, and R51) to lower head J4.

   Head-select transistor Q5, in turn, is shut off via the high signal from open-collector inverter buffer U2 pin 10. With Q5 off, upper head J5 is disabled.

b. When the HSLT/ signal is low, that low is inverted by U1 to HSLT. The high HSLT signal is inverted again by inverter U2 (Sheet 6). The low output at U2 pin 10 turns on head-select transistor Q5. Transistor Q5 couples either the write current or the read bias, depending on the mode, to upper head J5.

   Head-select transistor Q4 is shut off via open-collector buffer U6. With Q4 off, lower head J4 is disabled.

c. The Head Select function has one jumper-selectable option; this option, however, is not controlled by the interface Head Select signal.

   If W28 (Sheet 3) is installed with W27 removed, the appropriate head is selected via the interface DIRN/ line. After the DIRN/ signal is inverted by U1 to HSLT, the head selection circuit description is exactly the same as the HSLT/ explanation.

3.5.5.4 Write Control Logic

a. The logic signals WRT, WPT, SEL/, and SBSY are gated to form a Write Enable signal that controls the write circuits. To write:

- The drive must be in Write Mode (WRT is high at U6 pin 9).
- The diskette must not be Write Protected (WPT is low at U2 pin 9).
- The drive must be Selected (SEL/ is low at U2 pin 5).
- The drive must not be Stepping (SBSY is low at U7 pin 9).

b. If the above four conditions are met, the Write Enable signal is high and:

1) Write current driver U3 is enabled. The high releases the clear and preset inputs (pins 1 and 4 respectively), which enables U3 to respond to Write Data at input pin 3. When pins 1 and 4 are held low, outputs 5 and 6 are both high.

2) The selected erase current driver is enabled via buffer U6, pins 6 or 10. Erase current driver selection depends upon the condition of the HSLT signal.

3) WBSY is generated. The high write enable signal is applied to pin 3 of inverter buffer U2. The low output, coupled to the base of transistor Q3, turns on the transistor. WBSY is generated by the voltage divider formed by R26 and R27. The WBSY signal ensures that no stepping occurs while writing.

3.5.5.5 Write Current Driver

The write current driver circuit consists of a flip-flop, two gates, two power drivers, two diodes, and two resistors.

a. When the Write Enable goes high, the preset and clear inputs to write flip-flop U3 are released; and the flip-flop toggles on each WDA pulse. The complementary outputs of U3 are inverted by exclusive-OR gates U15. The outputs at pins 6 and 8 then are applied to power inverters U7. Thus, as write flip-flop U3 toggles, the outputs (at U7 pins 2 and 12) alternately drive current through the two halves of the read/write head.

b. Resistors R4 and R5 ensure that diodes CR10 and CR14 are reverse biased when the write operation is completed, thus isolating the write circuits from the read/write head during read operations.

3.5.5.6 Erase Current Driver

The erase current driver circuit for single-head drives consists of a delay generator circuit (capable of generating two different delays) and a driver circuit.

a. Resistors R12 and R13, capacitor C5, and diode CR3 comprise a delay network that generates the two delays.

   1) When a write operation is initiated, U6 pin 6 goes high. Capacitor C5 charges via resistor R12 and forward-biased diode CR3. The C5 charge-time via R12 is approximately 400 microseconds. After that delay, the voltage at capacitor C5 (applied to the trigger and the threshold inputs at pins 6 and 2 respectively) turns on timer U9.

   2) At the conclusion of the write operation, U6 pin 6 goes low. Capacitor C5 discharges through resistor R13; diode CR3 is reverse biased and does not offer an alternate discharge path. The discharge time via R13 is approximately 800 microseconds. At the end of that delay, the voltage at capacitor C5 is removed from the trigger and threshold inputs, which turns off timer U9.

b. Timer U9 and various filter and biasing components comprise the driver circuit.

   1) When a write operation is initiated and U6 pin 6 goes high, the output of timer U9 does not follow the change of state until the 400 microsecond delay circuit times out. At this time, U9 senses the the high state of U6 pin 6; and U9 pin 5 goes low. This condition causes the erase current to flow through the erase winding and diode CR8. The amount of erase current is determined by the value of resistors R36 and R15.

   2) At the conclusion of the write operation, U6 pin 6 goes low. However, the output of timer U9 does not follow that change of state until the 800 microsecond delay circuit times out. At the end of that time delay, U9 pin 5 goes high; and the erase current stops flowing. When the head winding current stops, diode CR4 absorbs the inductive EMF.

For dual head drives, the description of the erase current driver circuitry (within the dotted lines on Sheet 6 of the schematic) is identical to that explained in previous paragraphs a and b.

3.5.6 Read Channel (Sheet 7)

After passing through the Input Clamp, the read signal is Amplified and then Filtered. Next, the signal is differentiated, filtered, and then digitized by the Comparator. The digitized read signal is then applied to the Digital Noise Filter. The final stage of the Read Channel is the Bidirectional One-Shot, which generates the read data signal, RDA. The RDA signal is then passed to the host controller via the interface. Figure 3-16 is a block diagram of the read circuitry.

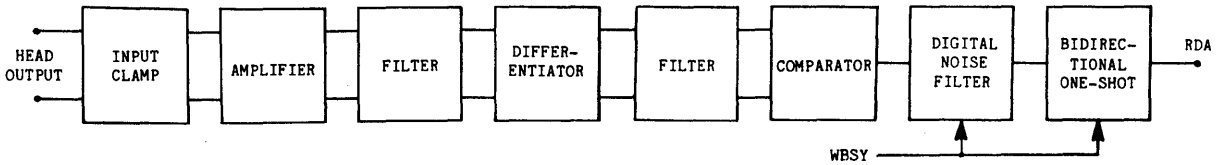


Figure 3-16. Read Channel Block Diagram

The regulated +12V supplied to the elements of this circuit is filtered by inductor L5 to provide noise isolation. Voltage divider R92 and R93, and filter capacitor C44, develop reference voltage V1, which is approximately +6V.

3.5.6.1 Input Clamp

The low-level read signal (approximately 2 to 3.5 millivolts) from the head first passes through the Input Clamp, which consists of two diodes and a reference voltage.

a. When in the write mode, the junction of CR22 and CR23 is set at approximately +10.6V (V2 reference voltage), thereby reverse biasing diodes CR18 and CR21 (Sheet 6). Diodes CR22 and CR23 then constitute a clamp circuit that blocks the input to the Read Channel and prevents large transients, generated by the write circuit, from propagating through the read circuits.

b. When reading, the junction of diodes CR22 and CR23 switches to approximately +6.7V (V2 reference voltage), forward biasing diodes CR18 and CR21 and thus providing a low impedance path for the read signal. The V2 reference voltage is set by the voltage divider formed by resistors R49, R50, and R51; see Paragraph 3.5.5.2b, Read/Write Switch.

The read signal is fed to the Amplifier circuit via zero-ohm resistors R39 and R40.

3.5.6.2 Amplifier

The Amplifier circuit consists of amplifier U17 with capacitor C23 connected to pins 3 and 12. The gain of the amplifier is approximately 100 and cannot be adjusted. The balanced, differential output is applied directly to the Filter.

3.5.6.3 Filter

The Filter circuit is a differential LCR network.

Inductors L2 and L4, capacitors C45 and C47, and resistor R91 form one leg of the filter; inductors L1 and L3, capacitors C45 and C43, and resistor R90 form the other leg of the filter. Note that capacitor C45 is common to both legs of the filter.

Resistors R90 and R91, along with reference voltage V1, maintain the read signal at the center of differentiator U21's linear range.

3.5.6.4 Differentiator

The Differentiator consists of an amplifier chip and its associated gain select components. This Differentiator circuit (in conjunction with the Comparator circuit) functions as a peak detector.

U21 is a differential output, wideband amplifier. Capacitor C54 provides the 6db per octave rising characteristic of a differentiator, while resistor R88 terminates this characteristic at 250 kHz. Inductor L6 rolls off noise at frequencies greater than 250 kHz.

For test purposes, a jumper can be connected across TP7-1 and TP7-2. This jumper by-passes differentiator component C54 in the gain select network, thereby enabling U21 to operate as an amplifier only. This test is performed in order to check circuit resolution and adjust CE.

The output of the differentiator is AC coupled to the Comparator by capacitors C48 and C46 and resistors R94 and R97, while resistors R95 and R96 center the output at the V1 reference potential.

The outputs of the Differentiator at U21 pins 7 and 8, shown in Figure 3-14, cross the zero baseline each time a peak is detected on the input signal. This output is first filtered and then passed to the Comparator.

3.5.6.5 Filter

The filter consists of an RC network.

The output of the Differentiator is processed by the filter network formed by R94, R97, and C50. This filter provides additional noise rejection before the read signal is applied to the Comparator.

The differentiated, amplified, and filtered read signal is made available for measurement at TP11-5 and TP11-6 and is passed on to the Comparator.

3.5.6.6 Comparator

Voltage comparator U22 detects the zero-crossings of the differentiated read signal and changes state at each zero-crossing. This has the effect of digitizing the read signal.

3.5.6.7 Digital Noise Filter

The digital noise filter consists of an edge detector, a delay, and a flip-flop. Signal timing through the digital noise filter is shown in Figure 3-17.

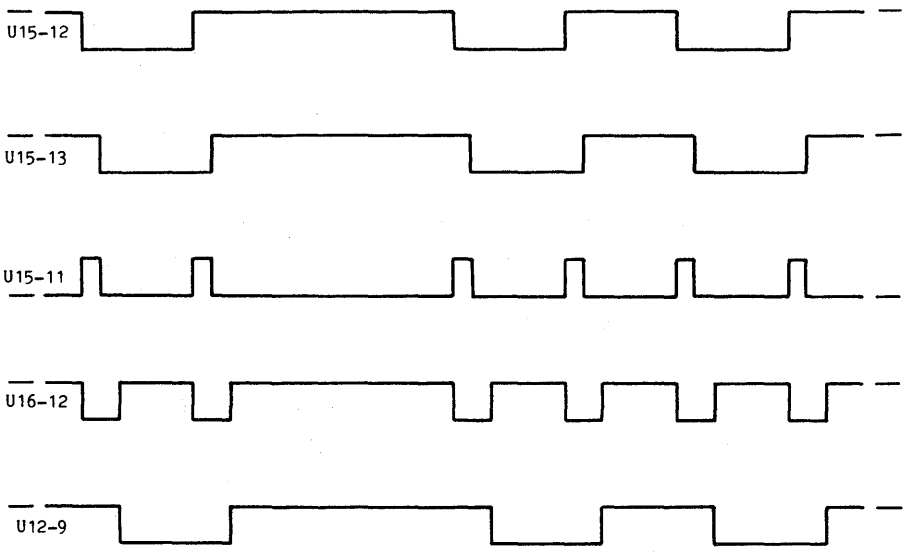


Figure 3-17. Digital Noise Filter Timing Diagram

a. The digitized read signal from the Comparator is applied to an edge detector circuit.

The Comparator output is applied directly to exclusive-OR gate U15 input pin 12. The Comparator signal is also delayed (by RC network R55/C18) and applied to U15 input pin 13.

The output at U15 pin 11 is a narrow, positive-going pulse, which is generated for every change in state of the Comparator output.

b. The edge detector clock pulses are delayed by one-shot U16.

The RC time constant set by C20 and R54 determines the pulse width of one-shot U16. The normally high output at U16 pin 12 goes low with each pulse generated by the edge detector. The one-shot output at pin 12 will stay low for the duration of the delay and will then return to its normally high logic state. The positive-going edge of the one-shot output clocks flip-flop U12 pin 9 (Sheet 7).

The Write Busy signal (WBSY) from the Write Channel (Sheet 6) disables delay one-shot U16 whenever the drive is in the write mode. This prevents noise from being passed through the Read Channel to the interface.

The delay circuit shifts the clock timing away from the read data signal transitions. This is done to eliminate any short-duration noise spikes from being clocked through the Digital Noise Filter. The output of this delay circuit is used to clock the Digital Noise Filter flip-flop.

c. U12 pin 9 is a D-type flip-flop and is positive edge triggered.

The positive-going edge of the delayed pulse from the delay circuit clocks the flip-flop.

1) If <u>read data</u> initiates the delayed clock pulse, then data appears at the D-input of flip-flop U12, and the flip-flop will change state. In other words, the change in logic state that fired the one-shot will be clocked into the flip-flop, and the output at pin 9 will assume that state.

2) If <u>noise</u> initiates the delayed clock pulse, U12 will not change state. By the time the delayed clock edge is applied to the flip-flop, the noise pulse at the D-input of the flip-flop will have passed.

3.5.6.8 Bidirectional One-Shot

The Bidirectional One-Shot consists of an edge detector and a one-shot. Figure 3-18 shows the timing.

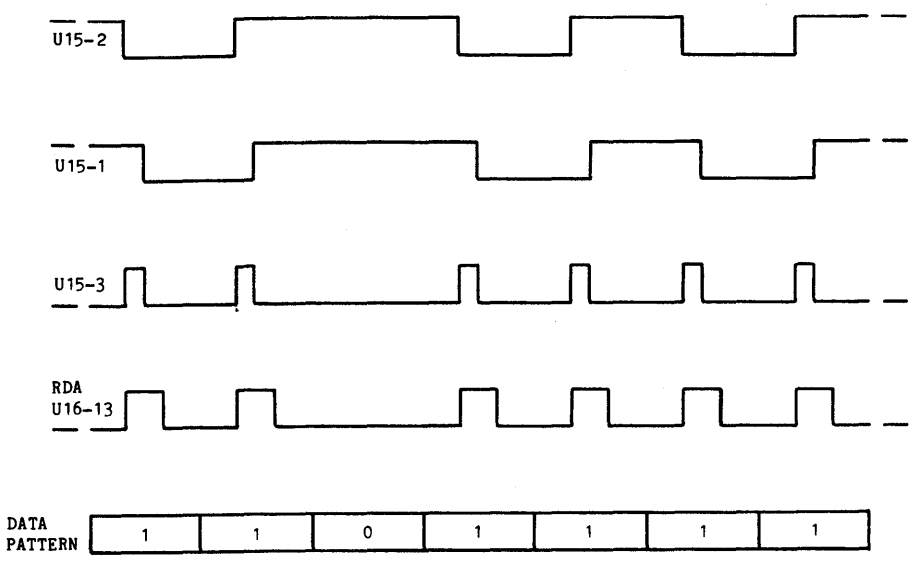


Figure 3-18. Bidirectional One-Shot Timing Diagram

a. Edge Detector: The read signal from flip-flop U12 pin 9 is applied directly to exclusive-OR gate U15 pin 2. The read signal is also delayed (by RC network R52/C19) and applied to U15 pin 1.

   The output at U15 pin 3 is a narrow, positive-going pulse, which is generated for each read data pulse transition or edge. The width of each output pulse is determined by the RC delay.

b. One-shot: U16 pin 13 is a re-triggerable, monostable multivibrator with associated timing components.

   The clock pulses, generated by the edge detector, fire one-shot U16. The RC time constant determined by capacitor C30 and resistor R72 establishes a 0.7 ($\pm$0.4) microsecond one-shot pulse width.

   The WBSY (Write Busy) signal from the Write Channel (Sheet 6) disables delay one-shot U16 when writing. Disabling U16 prevents noise from being passed to the interface.

The RDA signal is passed to the interface via interface output control gate U10 (Sheet 3).

3.5.7 Microcomputer-Based Control Logic (Sheet 8)

The microcomputer-based control logic supervises, controls, and monitors all the operations of the drive. The control logic consists of a 6500 Single-Chip Microcomputer System (U11) and associated support circuitry.

3.5.7.1 Microcomputer

The 6500 Microcomputer is a complete 8-bit computer with 2048 bytes of Read Only Memory (ROM) and 64 bytes of Random Access Memory (RAM) fabricated on a single chip.

Thirty-two signal lines (four eight-bit ports) are available for input and output functions. Input/Output applications for Microcomputer U11 are as follows:

a. Ports A and D:

   Although these eight-bit ports can be used for either inputs or outputs, both ports are used as <u>input</u> ports ONLY.

b. Ports B and C:

   These two eight-bit ports, like Ports A and D, can be used for either inputs or outputs; both ports are used as <u>output</u> ports ONLY.

3.5.7.2 Support Circuitry (Sheet 8)

a. Clock Oscillator:

The Clock Oscillator provides the basic timing signals used by the 6500 Microcomputer. The reference frequency is provided by an external 2.000 MHz crystal connected to the Microcomputer's XTAL input pins 10 and 11.

b. Power-On Reset Circuit:

The Reset input (RES) to the drive's Microcomputer is a power-on reset signal that initializes the Microcomputer when power is applied to the drive.

The reset circuit consists of an RC network, a diode, a logic gate (connected as an inverter), and two Schmitt trigger inverters.

When power is turned on, the PSEN signal goes high and capacitor C3 charges, via resistor R9, to about +2.8V. As C3 charges, the positive-going voltage passes the threshold of gate U4; and output pin 2 switches to 0V.

1) The low on output pin 2 is inverted to a high at U8 pin 11. That reset signal is applied directly to reset pin 39 (RES) of Microcomputer U11 (Sheet 8)

2) The low on output pin 2 is inverted to a high at U4 pin 12.

   The reset signal at U4 pin 12, identified as PWR ON RESET/, is applied to:

   - Reset pin 1 (MR) of Phase latch U14 (Sheet 8)
   - Input pin 4 of gate U8 (Sheet 8)
   - Reset pin 13 (R) of In Use latch U3 (Sheet 5)
   - Input pin 2 of Head Load Solenoid gate U19 (Sheet 5)

The RC time-constant of R9 and C3 holds the signal, applied to Microcomputer input RES, low for at least eight clock cycles after the supply voltage is within tolerance. That reset time guarantees that all Microcomputer circuitry and associated control logic is reset.

3.5.7.3 Microprocessor I/O Signals

The chart that follows summarizes all of the I/O signals into and out of Microcomputer U11.

PORT A (Input)

Microcomputer Identifier	Drive Logic Signal Name	Function
PAØ	-	Inverted CNTR signal (from Microcomputer output pin 21).
PA1	MOT TACH/	Spindle speed sensor output, used by the Microcomputer for spindle motor speed regulation.
PA2 (NOTE)	W21, jumper option (W22 removed)	The spindle motor comes on when MTRN is true and the drive is selected.
PA3 (NOTE)	W22, jumper option (W21 removed)	Spindle motor comes on if either MTRN is true or the drive is selected.
PA4	W23, jumper option	Controls the microcomputer-generated Door signal (PC4). Installed: Microcomputer output port PC4 goes high when the disk access door is opened. Removed: Enables a latch circuit which monitors and stores any door open event while the drive is deselected. If this occurs, Microcomputer output port PC4 goes high. The latch is cleared when the drive is deselected.
PA5	W24, jumper option (W19, W20 removed)	The head will load when the drive is selected or MTRN is true.
PA6	W25, jumper option	Not used.
PA7	WBSY	Write Busy (WBSY) indicates that a write operation is being performed.

NOTE: If both jumpers W21 and W22 are removed, the motor will come on when MTRN is true.

PORT B (Output)

Microcomputer Identifier	Drive Logic Signal Name	Function
PBØ	HEAD LOAD SOL	Loads the head when asserted.
PB1	φ1	Phase 1 of four signals applied (via latch U14) to the stepper motor drive circuits to cause track-to-track positioning.
PB2	φ2	Phase 2 of four signals applied (via latch U14) to the stepper motor drive circuits to cause track-to-track positioning.
PB3	φ3	Phase 3 of four signals applied (via latch U14) to the stepper motor drive circuits to cause track-to-track positioning.
PB4	φ4	Phase 4 of four signals applied (via latch U14) to the stepper motor drive circuits to cause track-to-track positioning.
PB5	HOLD	Asserted at the end of a step operation. Holds the positioner in place in a low power, stand-by mode.
PB6	SBSY	Asserted during a step operation and applied to the write control logic (via latch U14). Ensures that writing does not occur while the drive is stepping.
PB7	-	Applied directly to the D-input of Motor Control flip-flop U13, which controls the spindle motor circuit.

3.5.7.3 Microprocessor I/O Signals (continued)

PORT C (Output)

Microcomputer Identifier	Drive Logic Signal Name	Function
PCØ	OUTPUT ENABLE/	Gated with the SEL/ signal to enable interface output control gate U10.
PC1	READY	Indicates the operational status of the selected drive.
PC2	-	Not used.
PC3	TKØOUT	Asserted when the read/write head is positioned at Track Ø and the stepper motor is in the hold mode.
PC4	-	Indicates the open/closed condition of the disk access door.
PC5	-	Not used.
PC6	-	Resets Step flip-flop U13 before the occurrence of the next pulse in a series of step pulses.
PC7	MOT/	Enables the spindle motor circuit.

PORT D (Inputs)

Microcomputer Identifier	Drive Logic Signal Name	Function
PDØ	HDLD	Controls (along with jumper-options W19, W20, and W24) the HEAD LOAD SOL signal (PBØ).
PD1	SEL	Indicates the drive has been selected by the host controller.
PD2	TKØIN	Indicates when the read/write head is positioned at Track Ø.
PD3	MTRN	Controls the on/off condition of the spindle motor.
PD4	SECP	Indicates the occurrence of an index hole or sector holes as the diskette rotates.
PD5	DOOR	Indicates the condition of the disk access door (i.e., open or closed).
PD6	-	Indicates the presence of an interface step command.
PD7	-	Indicates the step direction.

SECTION IV

TESTS AND ADJUSTMENTS

4.1 INTRODUCTION

This section provides information on testing a drive and (if necessary) adjusting the appropriate electrical and/or mechanical parameters. The tests and adjustments should be done in an order dictated by the operating condition of the drive; this may or may not be the order in which they are presented in this section. In general, the test requirements for different drive configurations are the same. When test requirements differ, relevant paragraphs specify those differences. Figure 4-1 shows the location of the PCBA-mounted components referenced in this section. Tools and test equipment required are listed in Section 1.5 of this manual.

4.2 TEST AND ADJUSTMENT PHILOSOPHY

Acceptable limits are specified in each functional test and adjustment procedure, taking into account the assumed accuracy of the test equipment specified. If the measured value of any parameter is within the acceptable limits, NO ADJUSTMENT should be made. If the measured value is outside the acceptable limits, the accompanying adjustment (if present) should be made; otherwise, troubleshoot to the defective component.

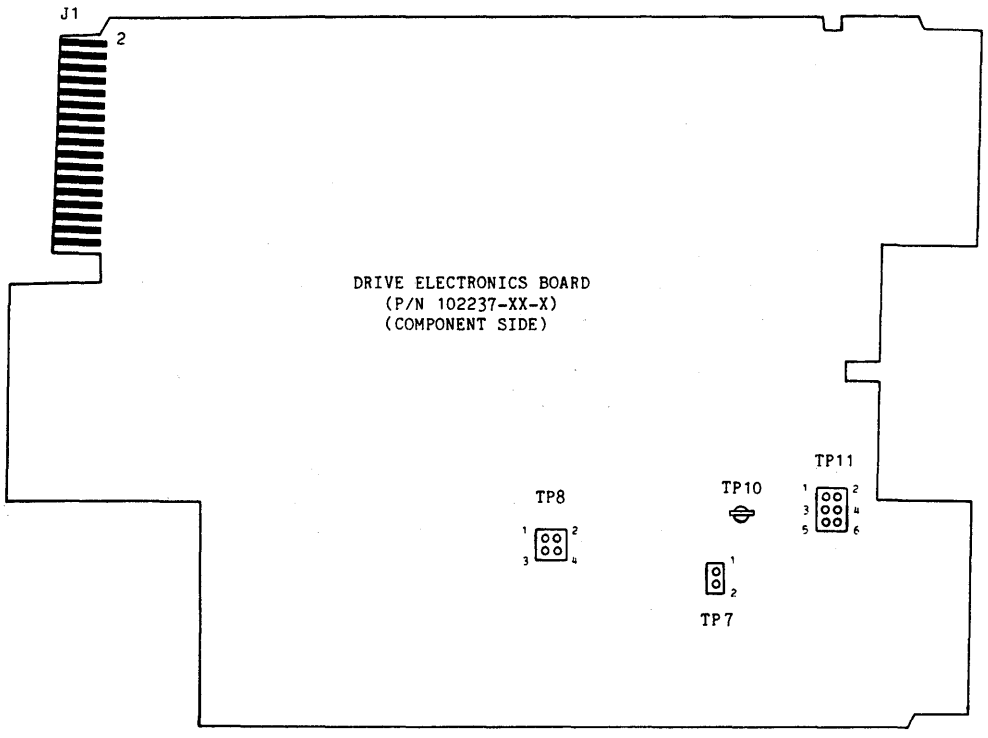


Figure 4-1. PCBA-Mounted Components

4.3 FUNCTIONAL TESTS

NOTE

There are no adjustments for the functional tests; if the measured value is outside the acceptable limits, troubleshoot to the defective component.

4.3.1 Drive Motor Speed

a. Drive motor speed should be checked whenever:

1) The drive motor is replaced.

2) The PCBA is replaced.

3) Any drive motor circuit components are replaced.

4) Diskette compatibility problems are encountered.

b. A strobe disk is fixed to the large spindle pulley and is visible when the drive is set on its side. The strobe disk is used to check the drive motor speed.

1) Apply power to the drive.

2) Apply a low signal to interface line MTRN/ (J1, pin 16).

3) Insert a work diskette into the drive, and load it.

4) Apply interface signals that cause the drive to be selected and the head to be positioned at Track Ø. (The head should be loaded at this time.)

5) Turn the drive on its side, and illuminate the strobe disk with a fluorescent lamp.

6) Observe the outer strobe pattern for 60Hz lamp power (or the inner strobe pattern for 50Hz), and time the pattern rotation speed. The pattern should be stationary. A maximum pattern drift of five revolutions per minute, clockwise or counter-clockwise, is acceptable.

4.3.2 Instantaneous Speed Variation

Instantaneous speed variation (ISV) is the change of rotational speed over a short period of time. The period used in this test is one and one-half revolutions of the large pulley.

a. ISV should be checked whenever:

1) The drive motor is replaced.

2) The PCBA is replaced.

3) PCBA components in the drive motor circuit are replaced.

4) Diskette compatibility problems are encountered.

b. Measure the ISV as follows:

1) Apply power to the drive.

2) Apply a low signal to interface line MTRN/ (J1, pin 16).

3) Insert a work diskette into the drive and load it.

4) Select the drive, and write an all ones pattern on Track Ø of the diskette.

5) Connect the Channel 1 oscilloscope probe to Read Amp TP11-6 and the ground to GND TP10.

Set the vertical scale to 0.2V/cm, and set the time base to 0.5 usec/cm. Uncalibrate the time-base so that one cycle of the waveform fills the calibrated part of the screen.

6) ISV appears as the width of the scope trace, as shown in Figure 4-2. The maximum allowable range of ISV is 6% of the overall width of one cycle of the waveform.

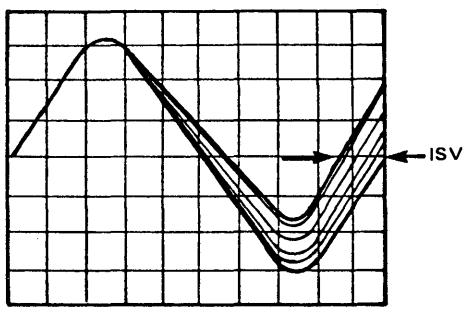


Figure 4-2. ISV Waveform

7) If ISV exceeds 6%, troubleshoot to the defective component; there is no ISV adjustment.

4.3.3 Read Amplifier Output

The read amplifier signal level is measured at the output of the amplifier chain.

a. The read amplifier output should be checked whenever:

1) The head is replaced.

2) The PCBA is replaced.

3) PCBA components in the Read Channel (differentiator, read amplifier, etc.) are replaced.

b. Check the read amplifier output as follows:

1) Apply power to the drive.

2) Apply a low signal to interface line MTRN/ (J1, pin 16).

3) Insert a work diskette in the drive, and load it.

4) For single head drives: Select the drive and write an all ones pattern on Track Ø of the diskette.

For dual head drives: Select the upper head and write an all ones pattern on Track Ø of the diskette.

NOTE

This test MUST be performed at Track Ø. Signal amplitude decreases as the head moves toward the center of the diskette.

5) Connect the Channel 1 oscilloscope probe to Read Amp TP11-6 and Ground TP10.

Set the vertical scale to 0.5V/cm, and set the time base to 10 us/cm. Trigger internally.

6) The amplitude of the read signal should be within the nominal range of 1.0V to 2.0V peak-to-peak.

7) If the read amplifier output is not within the specified range, troubleshoot to the defective component; there is no read amplifier output adjustment.

4.3.4 Door Open Sensor

The door open sensor is positioned to be activated when the door has been moved a minimum amount from its full open position; the sensor is deactivated when the door is fully open.

Activation of the sensor will rotate the spindle to allow for proper and accurate centering of the diskette.

a. The door open sensor operation should be checked whenever:

   1) The Jaw Lifter Assembly has been replaced.

   2) PCBA components in the door open sensor circuit have been replaced.

   3) There is evidence of diskette misclamping.

b. Check the operation of the door open sensor as follows:

   1) Apply power to the drive.

   2) Apply a low signal to interface line MTRN/ (J1, pin 16).

   3) Verify that when the door is open the drive motor does not turn; with the door closed the motor turns. If this criterion is not met, troubleshoot to the defective component; there is no door open sensor adjustment.

4.3.5 Write Protect Sensor

The write protect sensor is mounted on the outer structure; its associated LED is mounted on the Drive Electronics board. The write protect sensor assembly detects the presence of a slot or no slot (covered by a tab) on the diskette.

a. The write protect sensor should be checked whenever:

   1) The sensor assembly is replaced.

   2) A false indication of a write protected or a write enabled condition occurs.

b. Check the operation of the write protect sensor as follows:

   1) Operational Check:

      a) Attempt to write on a write protected diskette. A write protect error should result.

      b) Write on a diskette that is NOT write protected. No error should occur.

   2) Static Check:

      NOTE

      This check assumes the "standard" write protect convention, in which the diskette notch is covered for write protection and uncovered to enable writing. If the drive is configured for the reverse, the results will be opposite those shown.

      a) Insert a diskette that is NOT write protected (i.e., notch uncovered) into the drive. With an oscilloscope, verify that the signal level at TP8-1 (WPT) is at a TTL low.

      b) Insert a write protected diskette (i.e., notch covered) into the drive. Verify that TP8-1 (WPT) is now a TTL high level.

   3) If the drive fails either test in Step 2, troubleshoot to the defective component; there is no adjustment for the write protect sensor.

4.4 ADJUSTMENTS

If the measured value of any adjustable parameter is within the acceptable limits, NO ADJUSTMENT should be made. If the measured value is outside of the acceptable limits, the accompanying adjustment should be made.

4.4.1 Index Alignment

a. The index alignment test checks that:

1) The relationship between the head and the index/sector photosensor is correct.

2) The head moves along a line which passes through the center of the diskette (i.e., a radius).

b. The index alignment should be checked whenever:

1) The head is replaced.

2) The positioner subassembly is replaced.

3) The index photosensor is replaced.

4) The index LED assembly or the LED is replaced.

5) Diskette compatibility problems are encountered.

c. Check the index as follows:

1) Apply power to the drive.

2) Apply a low signal to interface line MTRN/ (J1, pin 16).

3) Use an appropriate alignment diskette (see Paragraph 1.5.1).

4) Insert the diskette into the drive, and load it.

5) Connect and preset the oscilloscope as follows:

a) Connect the Channel 1 test probe to TP11-6 (Read Amp) and TP10 (GND).

Set the vertical scale to 0.5V/cm, set the time-base to 50 usec/cm, and set the coupling to AC.

b) Connect the trigger probe to TP8-2 (Index/Sector Pulse).

Trigger: CH1, DC, NORMal , and + (positive).

6) Select the drive, then position the head at Track 5 for a 100TPI (MOD II or MOD IV) drive or at Track 2 for a 96TPI (MOD V or MOD VI) drive.

7) Measure the time between the leading edge of the index pulse and the first peak of the index alignment burst (see Figure 4-3). The time should be between 100 and 300 microseconds. If the time is not in that range, adjust the index alignment (see Paragraph d). Note the measured value, and then proceed to Paragraph e.

NOTE

If the burst cannot be obtained, the Radial Alignment (Paragraph 4.4.2) or Track Zero Adjustment (Paragraph 4.4.3) may be incorrect.

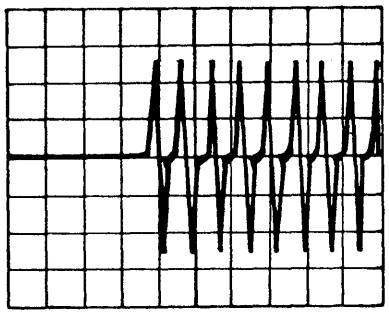


Figure 4-3. Index/Azimuth Alignment Waveform

d. Adjust the index alignment as follows:

1) Turn the adjustment screw (see Figure 4-4) to set the index-to-data time to its nominal value of 200 microseconds (18 degrees = 25 microseconds).

2) Repeat Paragraph c, Step 7 to recheck the index alignment.

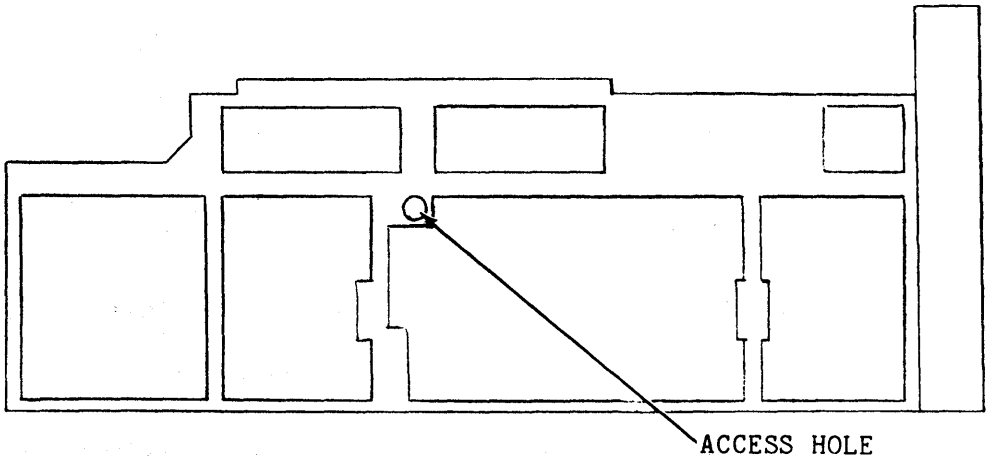


Figure 4-4. Index Adjustment Access

e. Check the azimuth as follows:

1) Select the drive, then position the head at Track 76 for a 100TPI (MOD II or MOD IV) drive or at Track 68 for a 96TPI (MOD V or MOD VI) drive.

2) Leave the oscilloscope connected as specified in Paragraph c; i.e., to TP11-6 (Read Amp) and TP10 (GND).

3) Measure the time between the leading edge of the index pulse and the first peak of the index alignment burst. Note the value and proceed to Paragraph f.

For dual head models, select the upper head; and repeat the procedure starting with Paragraph c, Step 5.

NOTE

If the burst cannot be obtained, the Radial Alignment (Paragraph 4.4.2) or Track Zero Adjustment (Paragraph 4.4.3) may be incorrect.

f. The index/azimuth alignment standard is as follows:

1) The INDEX time and the AZIMUTH time (as noted in Paragraph c, Step 7 and Paragraph e, Step 3) should differ by no more than 100 microseconds.

If the index/azimuth difference exceeds the 100-microsecond standard, troubleshoot to the defective component; there is no index/azimuth adjustment.

2) For dual head models, the readings must be balanced so that both heads (upper and lower) meet the specification.

4.4.2 Radial Track Alignment

Radial track alignment ensures that the head is operating at the required radius for the particular track.

The alignment utilizes a "Cat's Eye" pattern (usually called the CE pattern) on the alignment diskette. The CE pattern is centered on Track 36 for 100TPI (MOD II or MOD IV) drives or Track 32 for 96TPI (MOD V or MOD VI) drives. The Radial Track Alignment should only be performed when the temperature is $70^{\circ}F \pm 5^{\circ}$ and the relative humidity is 50% ±5%.

a. Radial alignment should be checked whenever:

   1) The head has been changed.

   2) The positioner assembly has been replaced.

   3) Diskette compatibility problems are encountered.

b. Check the radial alignment as follows:

   1) Apply power to the drive.

   2) Apply a low signal to interface line MTRN/ (J1, pin 16).

   3) Obtain the appropriate alignment diskette (see Section I, Paragraph 1.5.1).

   4) Insert the diskette into the drive, and load it.

   5) Connect and preset the oscilloscope as follows:

      a) Connect the Channel 1 test probe to TP11-6 (Read Amp) and TP10 (GND).

         Set the vertical scale to 10 mv/cm, set the time-base to 200 msec/cm, and set the coupling to AC.

      b) Connect the trigger probe to TP8-2 (Index/Sector Pulse).

         Trigger: EXTernal, DC, NORMal, and + (positive).

   6) Select the drive, then position the head at Track 36 for a 100TPI (MOD II or MOD IV) drive or at Track 32 for a 96TPI (MOD V or MOD VI) drive.

7) Observe the CE ("Cat's Eye") pattern (see Figure 4-5). Place a jumper across TP7-1 and TP7-2. Uncalibrate the vertical scale of the scope, and adjust the peak-to-peak amplitude of the larger lobe to eight major divisions/centimeters.

   Note the amplitude of the smaller lobe.

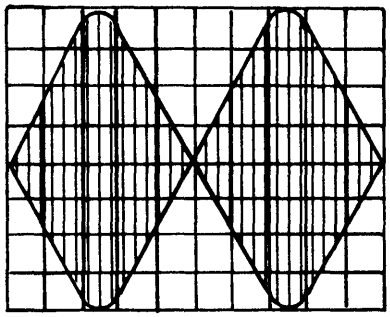


Figure 4-5. Cat's Eye Pattern for Radial Alignment

8) Apply interface signals that cause the positioner to move off two tracks and then return to the track used in Step 6.

   Set the larger lobe to eight centimeters and note the amplitude of the smaller lobe.

9) Apply interface signals that cause the positioner to move off track in the opposite direction and return.

   Again, set the larger lobe to eight centimeters and note the amplitude of the smaller lobe.

10) Track alignment is acceptable if the three measurements of the peak-to-peak amplitudes of the two lobes (i.e., from Steps 7, 8, and 9) are within two major divisions/centimeters of being equal, when the larger lobe is set to eight major divisions. If the track alignment is not acceptable, perform the necessary adjustment specified in Paragraph c.

c. Adjust the radial alignment as follows:

1) Loosen the two clamp screws that hold the stepper motor to the sub-chassis (see Figure 4-6, Stepper Motor Adjustment).

2) Rotate the stepper motor body as required to equalize the two lobes. Rotate the motor clockwise if the first lobe is greater than the second, or counter-clockwise if the second lobe is greater than the first.

NOTE

If the adjustment range is inadequate to equalize the lobes, the track zero sensor must be moved two full tracks; see Paragraph 4.4.3, Track Zero.

3) Tighten the clamp screws (see Figure 4-6) snugly so the stepper motor cannot turn (be careful to not bend the stepper motor flange), and reverify the alignment.

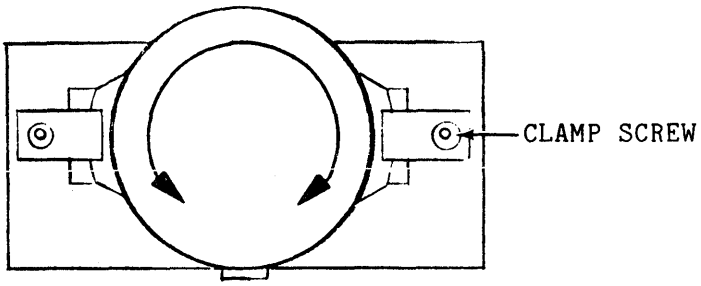


Figure 4-6. Stepper Motor Adjustment

4) Alternately check and adjust the radial alignment (refer to Paragraph b, Steps 7, 8, and 9 for the check and Paragraph c, Steps 1 through 3 for the adjustment), until equal amplitudes are obtained.

For dual head models, apply interface signals to select the upper head; repeat the procedure starting with Paragraph b, Step 5. The readings must be balanced so that both heads (upper and lower) meet the specification.

4.4.3 Track Zero Adjustment

The track zero sensor indicates to the host system that the head is at Track Ø.

a. The track zero sensor should be checked whenever:

   1) The positioner has been replaced.

   2) The head has been replaced.

   3) The track zero sensor assembly has been replaced.

   4) Radial alignment has been performed.

   5) Radial alignment has been unsuccessfully attempted.

b. Check the track zero sensor as follows:

   1) Apply power to the drive.

   2) Apply a low signal level to interface line MTRN/ (J1, pin 16).

   3) Insert a work diskette into the drive, and load it.

   4) Select the drive, and position the head to Track 1.

   5) Connect and preset the oscilloscope as follows:

      a) Connect the Channel 1 test probe to (TP8-3) and the Ground to TP10.

         Set the VOLTS/DIV to 1, set the time-base to 200 msec/cm, and set the coupling to DC.

      b) Trigger free running (i.e., AUTO).

   6) Observe the DC level on the scope. The track zero sensor setting is acceptable if the DC voltage is between +1.5 and +2.75 volts.

c. Adjust the track zero sensor as follows:

1) Observe the DC level specified in Paragraph b, Step 6.

2) Turn the track zero adjustment screw (see Figure 4-7) to set the DC level to its nominal value of +2.0 volts.

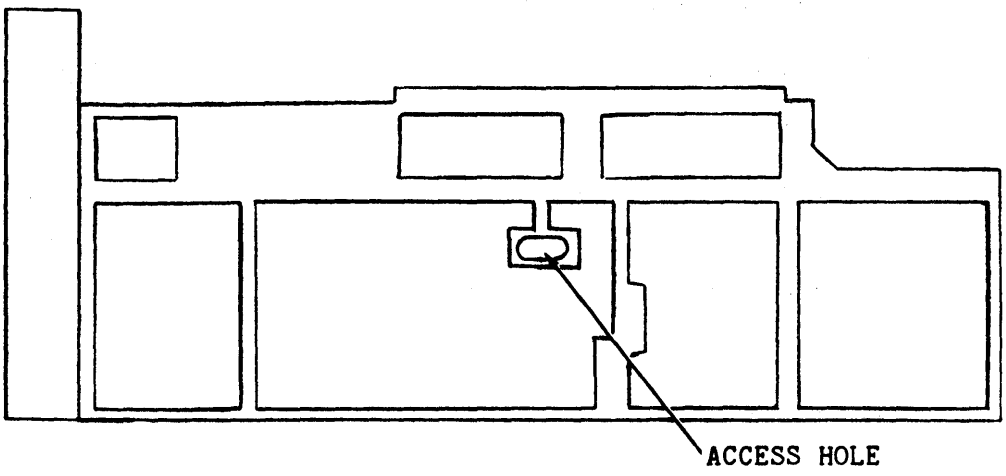


Figure 4-7. Track Zero Adjustment Access

SECTION V

TROUBLESHOOTING

5.1 INTRODUCTION

This section provides a troubleshooting chart to aid in isolating a fault symptom to a specific circuit, component, or sub-assembly. In most cases, there is a paragraph reference for more information or a detailed procedure.

TABLE 5-1 TROUBLESHOOTING CHART

Symptom	Possible Cause	Action	Reference
Select indicator is always lit.	Interface cable is reversed at one end.	Reverse the cable.	2.6, 3.3
Drive motor does not rotate when the diskette is inserted and is clamped. (MTRN, J1-16 is low.)	Controller is not connected to drive.	Check the interface cable.	2.6, 3.3
	No power to drive.	Check for +5V and +12V at proper pins of power connector (see Para 2.5 for pin assignments).	2.5
	Drive motor is defective.	a. Check motor.	3.5.3.2
		b. Replace the motor if defective.	6.4
	Drive motor circuit on PCBA defective.	a. Troubleshoot circuit.	3.5.3
		b. Replace PCBA.	6.3
	Door open sensor defective.	Check sensor assembly for proper operation; if defective, replace.	4.3.4, 3.5.2.2
	Failure in the door open sensor circuit on PCBA.	a. Troubleshoot circuit.	3.5.2.2
		b. Replace PCBA.	6.3

TABLE 5-1 TROUBLESHOOTING CHART (continued)

Symptom	Possible Cause	Action	Reference
Drive motor rotates much more rapidly than 300 RPM and cannot be adjusted.	Intermittent connector on drive motor.	Repair/replace connector.	-
	Defective tachometer sensor assembly.	Check sensor assembly for proper operation; if defective, replace.	3.5.2.4 6.5.6
	Failure in the servo circuit on PCBA.	a. Troubleshoot circuit. b. Replace PCBA.	3.5.3 6.3
Head will not load. (Drives with head load solenoid option only.)	Head load solenoid open.	Replace solenoid.	6.5.4
	Failure in head load solenoid circuit or head load logic on the PCBA.	a. Troubleshoot circuit. b. Replace PCBA.	3.5.1.3 6.3
Head will not unload. (Drives with head load solenoid option only.)	Head load solenoid driver is shorted on the PCBA.	a. Troubleshoot circuit. b. Replace PCBA.	3.5.1.3 6.3
	Solenoid binding.	Remove obstruction to free movement.	-
Positioner misteps, head ends up at wrong track.	Stepper motor defecective.	Replace positioner.	6.5.3
	Component failure in positioner circuit on the PCBA.	a. Troubleshoot circuit. b. Replace PCBA.	3.5.4 6.3
Diskette jams or miscenters.	Clamp miscentered.	Reset E-ring.	6.6.1
	Contamination on the clamp or spindle.	Clean with alcohol.	-
	Clamp defective.	Replace clamp.	6.6.1
Door cannot latch or unlatch.	Defective jaw lifter.	Replace jaw lifter.	6.6.2

TABLE 5-1 TROUBLESHOOTING CHART (continued)

Symptom	Possible Cause	Action	Reference
Soft read errors. (Non-permanent.)	Degraded surface on diskette.	Change diskette.	-
	Head dirty or contaminated with oxide.	Clean head.	1.6.1
	Head load pad dirty or contaminated with oxide (single head models only).	Replace head load pad.	6.5.1
	Excessive instantaneous speed variation (ISV).	a. Check ISV.	4.3.2
		b. Check/replace drive motor.	6.4
	Excessive pulse-type noise in read signal (appears as spikes on the read amplifier waveform).	Isolate source and repair/replace. May be internal (bad PCBA, faulty drive motor, etc.) or external (bus noise, noisy cabling, radiating CRT, poor electrical ground, etc.).	-
	Marginal/intermittent component in the read circuit on PCBA.	a. Troubleshoot circuit.	3.5.6
		b. Replace PCBA.	6.3
Hard (permanent) read errors.	Degraded surface on diskette.	Change diskette.	-
	Component failure in read circuit on the PCBA.	a. Troubleshoot circuit.	3.5.6
		b. Replace PCBA.	6.3

TABLE 5-1 TROUBLESHOOTING CHART (continued)

Symptom	Possible Cause	Action	Reference
Write errors.	Head is dirty or contaminated with oxide.	Clean head.	1.6.1
	Head load pad dirty or contaminated with oxide (single head models only).	Replace head load pad.	6.5.1
	Write protect sensor intermittent.	Check sensor assembly for proper operation; if defective, replace.	4.3.5, 3.5.2.3, 6.6.4
	Intermittent write protect circuit on the PCBA.	a. Troubleshoot circuit. b. Replace PCBA.	3.5.2.3 6.3
	Intermittent diodes in read/write head switch circuit.	a. Troubleshoot circuit. b. Replace PCBA.	3.5.5.2 6.3
	Erase current driver in write circuit has incorrect delays.	a. Troubleshoot circuit. b. Replace PCBA.	3.5.5.6 6.3
	Component failure in write circuitry on the PCBA.	a. Troubleshoot circuit. b. Replace PCBA.	3.5.5 6.3
	Defective head.	If replacing the PCBA does not correct the problem, replace head.	6.5.2
Drive is always or never write protected.	Write protect sensor failure.	Check sensor assembly for proper operation; if defective, replace.	4.3.5, 3.5.2.3, 6.6.4
	Component failure in write protect circuit on the PCBA.	a. Troubleshoot circuit. b. Replace PCBA.	3.5.2.3 6.3

TABLE 5-1 TROUBLESHOOTING CHART (continued)

Symptom	Possible Cause	Action	Reference
Diskette incompatibility between drives.	Drive motor speed incorrect.	Check motor speed.	4.3.1
	Excessive instantaneous speed variation (ISV).	a. Check ISV.	4.3.2
		b. Check/replace drive motor.	6.4
	Index alignment out of adjustment.	Check/adjust the index alignment.	4.4.1
	Radial alignment out of adjustment.	Check/adjust the radial alignment.	4.4.2
	Marginal read/write circuit on the PCBA.	a. Troubleshoot circuit.	3.5.5, 3.5.6
		b. Replace PCBA.	6.3
	Defective head.	If replacing the PCBA does not correct the problem, replace head.	6.5.2

SECTION VI

REMOVAL AND REPLACEMENT PROCEDURES

6.1 INTRODUCTION

This section provides detailed procedures for replacing sub-assemblies and parts of the drive. Components are replaced at their spared level; i.e., a sub-assembly is replaced as a unit. Tests and adjustments in Section IV are referenced as applicable for each replacement procedure. Tools required for these procedures are listed in Section I, General Information.

6.2 DISK DRIVE REPLACEMENT

Use this procedure to replace the entire disk drive, consisting of the drive mechanism and the Drive Electronics PCBA (alternatively, follow the System manufacturer's procedure).

a. Disconnect the DC power (at J8A, J7, or J8B - see Paragraph 2.5a), and remove the interface cable to the controller at J1 on the PCBA.

b. Note the type and location of the screws used to attach the disk drive to the base chassis or brackets, since the replacement drive will be mounted using them. Remove the mounting screws, then remove the disk drive through the panel opening.

c. Insert the replacement drive through the panel opening from the front.

d. Reattach the drive to the base chassis or mounting brackets. (See Section 2.4 for more information, if needed.)

e. Reconnect the interface cable at J1; reconnect the DC power.

6.3 DRIVE ELECTRONICS PCBA

The Drive Electronics PCBA is mounted on top of the drive mechanism.

a. Note the location and orientation of drive-to-PCBA connectors J9 through J13 (the proper orientation at these connectors is shown in Figure 6-2), then disconnect those connectors.

CAUTION

For the following steps, handle the head cable and cable connector very carefully because they are fragile and irreparable.

b. Disconnect the head cable at PCBA connector J4/J5 (single-head drives use J4; dual-head drives use both J4 and J5).

c. Remove the four screws that attach the PCBA to the chassis (see Figure 6-1), and lift the PCBA off the drive mechanism.

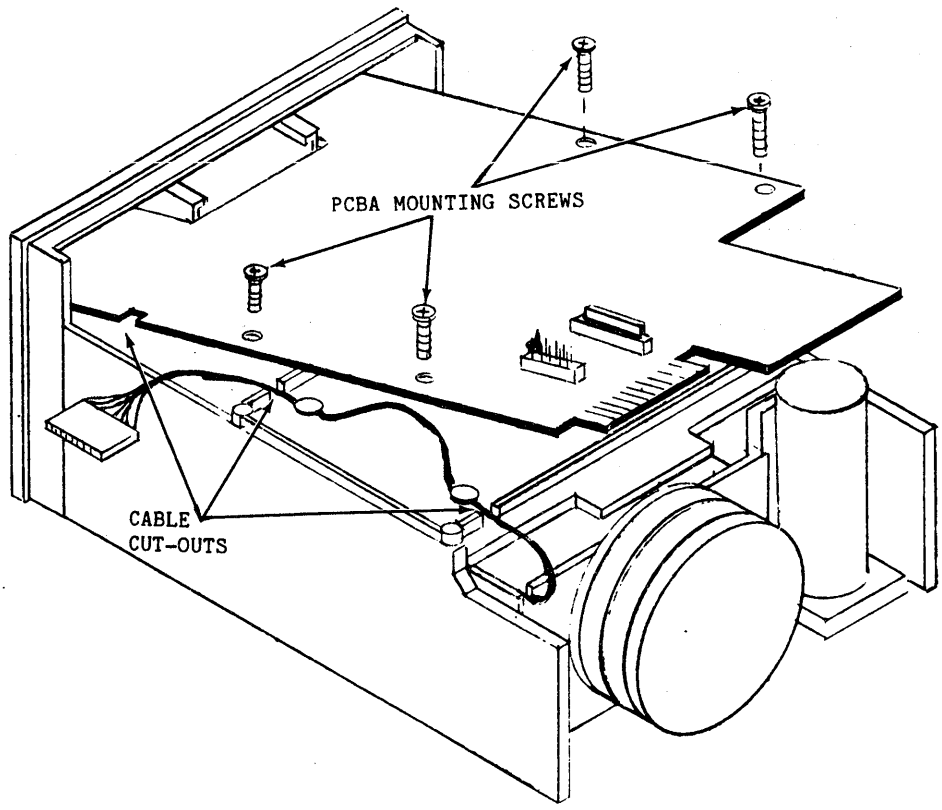


Figure 6-1. PCBA Mounting Details

d. Configure the replacement PCBA as required (i.e., check for appropriate drive select jumper placement and use of the terminator resistor pack). Refer to Section 2.7.

e. Take the replacement PCBA, and tilt the front slightly downward. Slide the PCBA into the slot in the casting, located just behind the bezel. Position the PCBA so that it is supported by the bezel fingers/guides.

f. Ensure the head cable runs freely under the PCBA, through the cable cut-outs in the casting, and through the cut-out adjacent to connector J4/J5 on the PCBA.

g. Install the four PCBA mounting screws removed in Step c.

h. Verify that the Door sensor and Door LED (located on the PCBA on each side of the door "flag") are vertical. If they are not, then gently reposition them.

i. Mate the keyed, head cable connector with J4/J5 (see Step b above); the label on the connector must be facing up.

j. Mate the drive-to-PCBA connectors (J9 through J13) with the PCBA, orienting them as noted in Step a (see Figure 6-2).

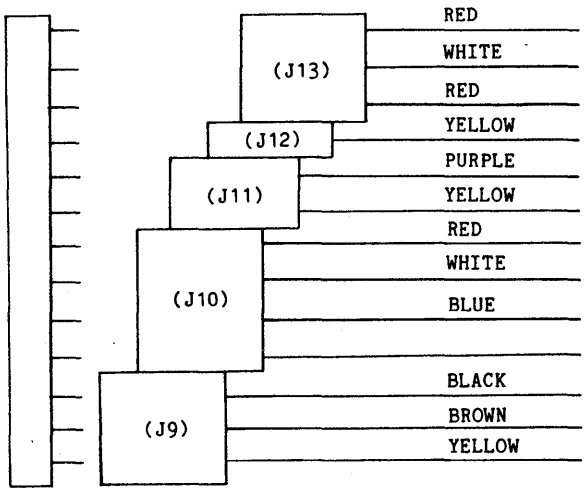


Figure 6-2. J9-J13 Orientation

k. Check for proper PCBA installation and operation by performing the following tests in the order listed:

Procedure	Paragraph
Drive Motor Speed	4.3.1
Instantaneous Speed Variation	4.3.2
Read Amplifier Output	4.3.3

6.4 SPINDLE DRIVE MOTOR

Depending on how the disk drive is mounted, the Spindle Drive Motor and/or Drive Belt may be accessible without first removing the drive. If it is necessary to remove the drive, use the procedure given in Section 6.2.

CAUTION

If the drive belt is to be reused, do not stretch or kink it during removal. If stretching or kinking occurs, the drive belt must be replaced.

a. Note that the shiny side of the drive belt is in contact with the pulleys. Slip the drive belt off the large pulley, and then remove it from the small pulley on the drive motor. Retain the belt if it is acceptable for reuse. If the belt is to be replaced and the existing drive motor is acceptable, proceed directly to Step h.

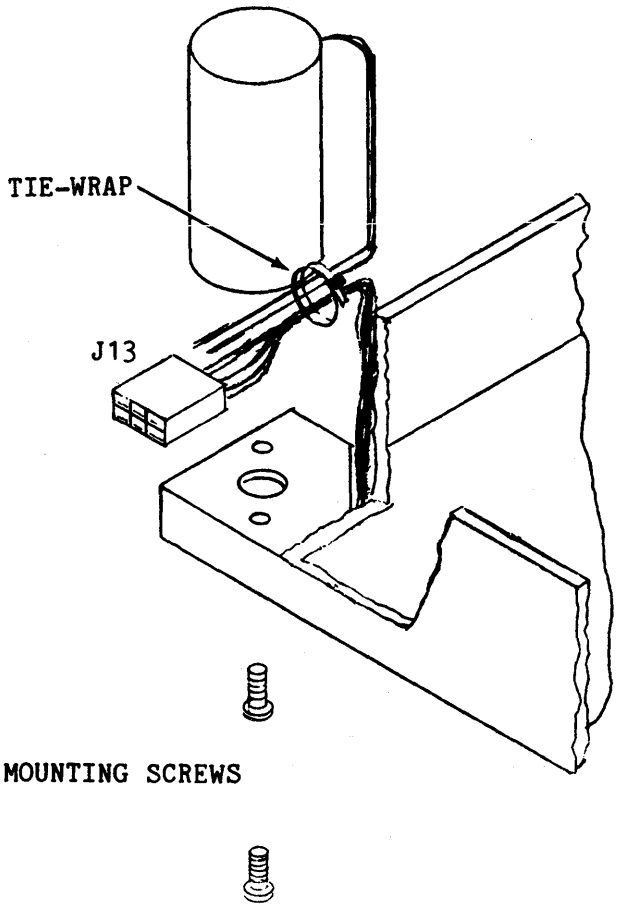


Figure 6-3. Spindle Drive Motor

NOTE

The replacement assembly includes the connector that mates to the Drive Electronics Board. Since the same connector is used for several functions, if the original connector is not damaged it may be easier to use the original connector. To do this, at the suitable time in the following procedure, remove the original assembly's wires at the connector, detach the new assembly's wires from the (new) connector and insert them at the appropriate locations in the original connector.

b. Disconnect the cable connector at J13 on the PCBA, and cut the tie-wrap on the cable.

c. Extract the blue motor wire and the red motor wire (pins 1 and 2 respectively) from the cable connector.

d. While holding the drive motor, remove the drive motor mounting screws. Lift the drive motor from the chassis.

e. Align the replacement drive motor with the sub-chassis mounting holes. Ensure that the motor wires face the interior of the sub-chassis. Secure the drive motor to the sub-chassis using the same two motor mounting screws removed in Step d.

f. Insert the blue wire (pin 1) and the red wire (pin 2) into the J13 cable connector. The contacts are internally barbed so the wires will not pull out.

g. Attach the cable connector to J13 on the PCBA, and then tie-wrap the cable as indicated in Figure 6-3.

NOTE

In the next step, ensure that the shiny surface of the belt is in contact with the pulleys.

h. Place the original or replacement drive belt over the small drive motor pulley, and rotate the large pulley while slipping the belt over it.

i. Check for proper motor and/or belt installation and operation by performing the Drive Motor Speed test (Paragraph 4.3.1) and the Instantaneous Speed Variation test (Paragraph 4.3.2).

6.5 SUB-CHASSIS

The Sub-Chassis consists of a die cast frame, which pivots within an outer die cast structure. Removal of the sub-chassis is necessary for access to the sub-assemblies housed in either the sub-chassis or the outer structure.

a. To remove the sub-chassis:

1) Remove the Drive Electronics PCBA; see Section 6.3.

2) Loosen the pivot pin set screws (3/32-inch hex).

3) Open the door of the drive. With one hand, hold the Jaw Lifter in the open position (i.e., press down on the ends of the torsion bars, where the lift links are attached, as shown by the arrows in Figure 6-4).

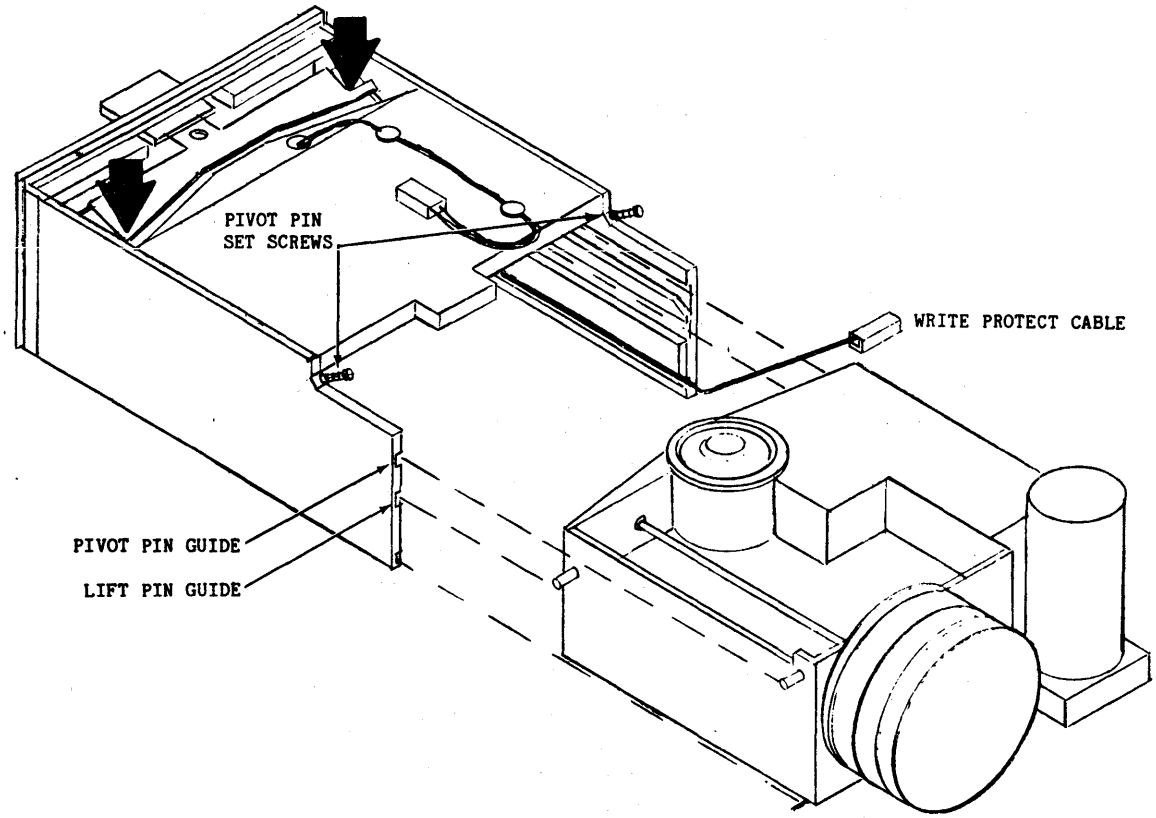


Figure 6-4. Sub-Chassis Installation

4) With the other hand, grasp the sub-chassis and pivot the front of the sub-chassis up until the lift pins are freed from the lift links.

5) Pull the sub-chassis to the rear, sliding it out via the guide slots.

6) Perform whatever repair or maintenance is required on the sub-assemblies housed in the sub-chassis or the outer structure.

b. To reinstall the sub-chassis:

1) With the outer structure placed right-side up and flat on a table, ensure that all the sensor harness wires (on the outer structure) are positioned out of the way of the incoming sub-chassis. Position the Write Protect Cable in the slot indicated in Figure 6-4.

2) Open the door of the drive.

3) Install the sub-chassis by sliding it into the guide slots. The lower slots are for the lift pins, and the upper slots are for the pivot pins (as shown in Figure 6-4).

4) Hold the Jaw Lifter in the open position (press down on the ends of the torsion bars where the lift links are attached - see Figure 6-4), and push the sub-chassis forward until the lift pins connect with the lift links and the pivot pins seat in the outer structure.

5) Ensure the door of the drive is still open.

6) While holding the sub-chassis pressed forward, tighten the pivot pin set screws (see Figure 6-4).

7) Check for proper installation and operation by opening and closing the drive's door and checking for smooth action of the sub-chassis.

8) Install the PCBA; see Section 6.3.

6.5.1 Head Load Pad (Single Head Models only)

The Head Load Arm and Head Load Pad are accessible when the sub-chassis is removed from the outer structure; see Section 6.5.

a. Using a spring hook or tweezers, remove the spring holding the head load arm in place (see Figure 6-5); and lift the load arm from its pivot block.

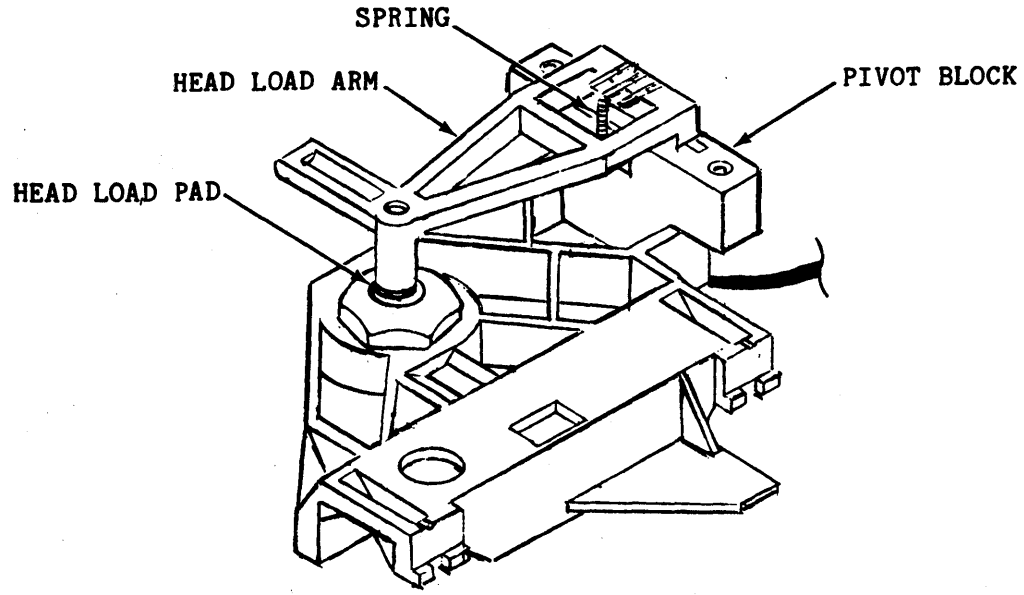


Figure 6-5. Head Load Arm and Pad

b. Using tweezers, carefully remove the old head load pad from the head load arm. Adhesive will usually remain stuck in the recess in the load arm. Carefully remove all bits of residual adhesive.

c. While being careful not to touch the adhesive surface, peel the protective strip from the back of the replacement head load pad.

CAUTION

During the next step, ensure that the head load pad is flat; an off-center and/or off-level head load pad will cause data errors.

d. Position the head load pad in the head load arm recess, then use a flat tool to press it into place.

e. Place the head load arm back on its pivot block. Reconnect the spring, hooking one spring loop over the lower spring pin first and then slippping the other spring loop over the center spring pin on the load arm.

f. Perform the Read Amplifier Output test (Paragraph 4.3.3).

6.5.2 Head-Carriage

The Head-Carriage assembly is supported and driven by the positioner lead screw. The head carriage is accessible when the sub-chassis is removed from the outer structure (see Section 6.5).

CAUTION

For dual head drives, the upper and lower heads must not come into direct contact with each other. During removal and replacement, an interposer (an integral part of the head carriage assembly) separates the two heads thus preventing possible head damage.

a. Cut the tie-wrap securing the head cable(s) to the casting. Note the cable routing and the tie point on the casting.

b. By manually rotating the lead screw, position the carriage midway between the stepper motor and the end of the lead screw (i.e., centered on the lead screw).

c. Hold the head carriage firmly with one hand. Using tweezers, remove (pull up and then away from the lead screw) both the front and the rear carriage springs shown in Figure 6-6.

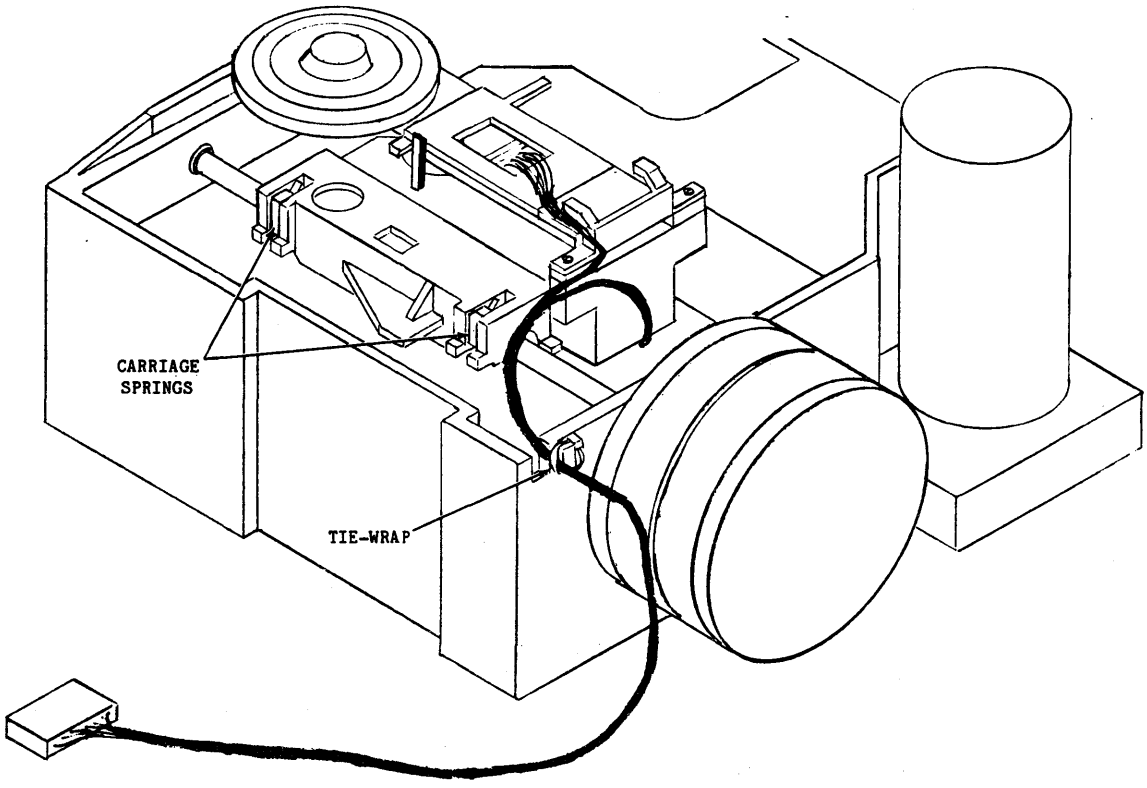


Figure 6-6. Head Carriage Assembly

d. Lift the head carriage assembly out of the sub-chassis.

e. Set the replacement head carriage on the lead screw (towards the front), sliding the platen spring of the carriage under the platen on the sub-chassis. Ensure that the lead screw channel on the carriage is seated on the lead screw (see Figure 6-7).

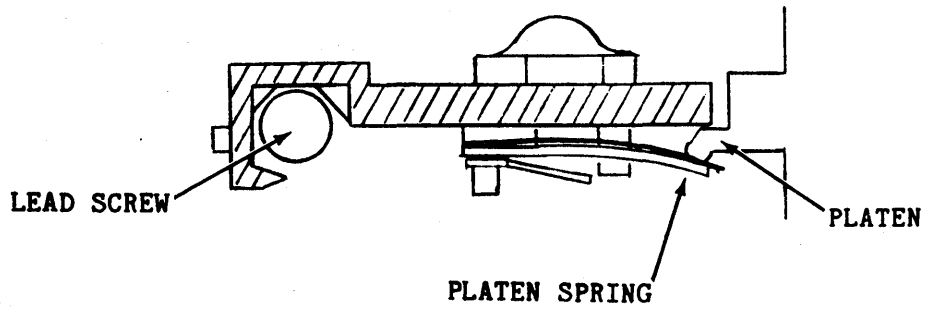
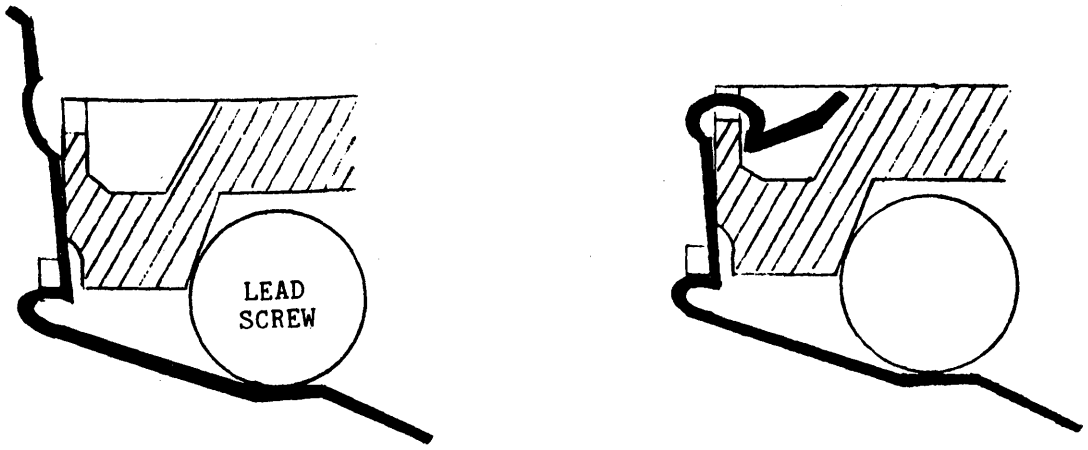


Figure 6-7. Properly Seated Carriage

f. Hold the head carriage firmly with one hand. Grasp the "front" carriage spring (see Figure 6-8) with tweezers.

Figure 6-8. Carriage Spring Identification

g. Position the carriage spring below the spring channel near the front of the carriage. With the spring clipped over the lead screw, pull the spring up through the groove of the channel (see Figure 6-9a). Then, slide the spring over the lip of the carriage, locking it in place (see Figure 6-9b).



A. POSITIONED

B. LOCKED

Figure 6-9. Carriage Spring Placement

g. Grasp the "back" carriage spring (see Figure 6-8) with tweezers and position it below the spring channel near the rear of the carriage. With the spring clipped over the lead screw, pull the spring up through the groove of the channel (see Figure 6-9a). Then, slide the spring over the lip of the carriage, locking it in place (see Figure 6-9b).

h. Route and tie-wrap the head cable(s) as noted in Step a. Ensure that the tie-wraps do not stress the upper head arm.

i. Reassemble the drive; see Section 6.5.

j. Check for proper installation and operation of the Head Carriage by performing the following tests in the order listed:

Procedure	Paragraph
Read Amplifier Output	4.3.3
Index Alignment	4.4.1
Radial Track Alignment	4.4.2
Track Zero Alignment	4.4.3

6.5.3 Stepper Motor Assembly

The Stepper Motor Assembly (also identified as the Positioner Assembly), consisting of a stepper motor and a lead screw, is replaced as a unit. The step motor assembly is accessible when the sub-chassis is removed from the outer structure (see Section 6.5) and the head carriage assembly is removed from the lead screw (see Section 6.5.2).

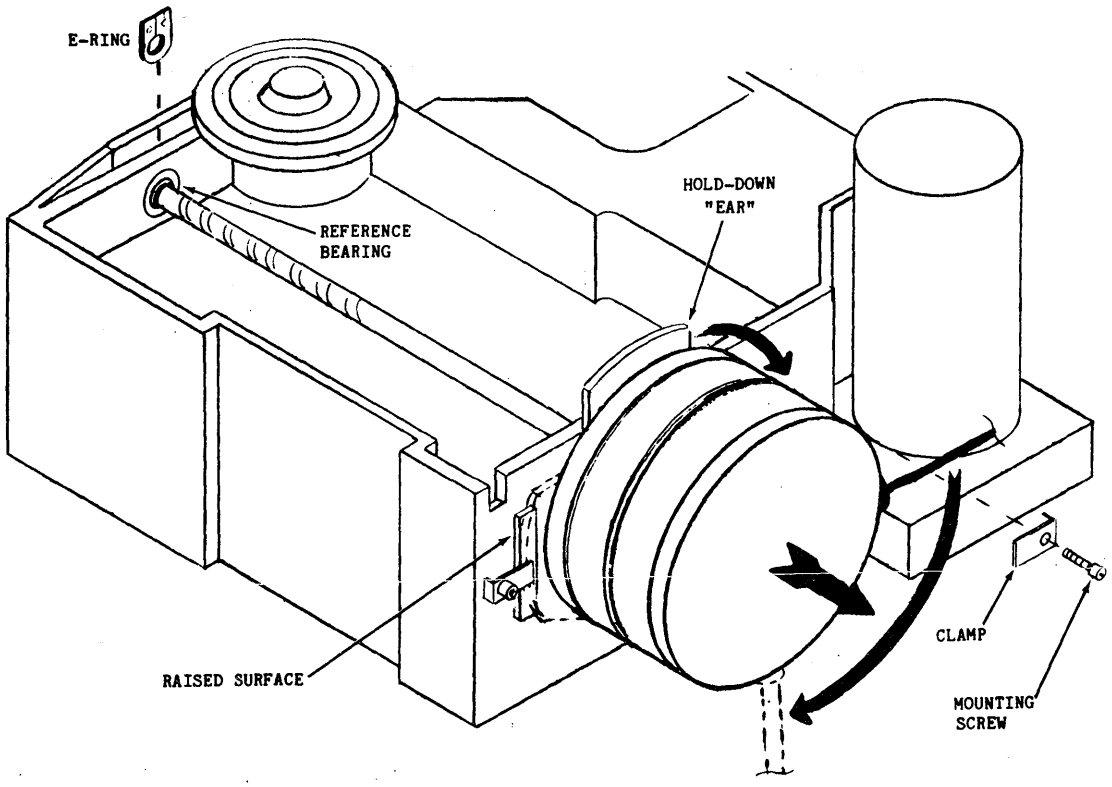


Figure 6-10. Step Motor Assembly

a. Disconnect the cable connector at J9 on the PCBA, and clip the tie-wrap holding the cable. Note the position of the tie-wrap.

b. Loosen the two positioner mounting screws thereby freeing the clamps that hold the positioner to the sub-chassis.

c. Rotate the positioner counter-clockwise until the "ears" of the motor are vertical and the motor is flat against the the rear of the sub-chassis.

d. Unclip the E-ring from around the lead screw shaft (located in front of the reference bearing, next to the spindle). This releases the lead screw.

e. Slide the lead screw shaft out of the sub-chassis, and remove the positioner assembly.

f. Insert the replacement stepper motor lead screw shaft into the sub-chassis through the hole located in the rear wall. Ensure that the wires of the stepper motor are positioned at the bottom of the drive and that the front of the shaft enters the reference bearing located next to the spindle.

g. Make sure that the visible bearing on the front of the stepper motor is seated in the hole in the back wall of the casting and that the left and right "ears" of the stepper motor are flush to the mounting flanges of the casting.

h. Rotate the positioner counter-clockwise until the "ears" of the motor are vertical and the motor is flat against the the rear of the sub-chassis.

i. Install the E-ring (removed in Step d) around the shaft, in front of the reference bearing.

j. Hold the sub-chassis firmly with one hand. With the other hand, grasp the stepper motor and pull it to the rear (until a slight movement is detected). Then rotate the motor clockwise until the motor wires exit the bottom and the ears are on the raised surfaces of the casting. Release the stepper motor; lead screw pre-load will hold the positioner assembly securely in place.

k. Apply a light coat of grease (Magnalube) to the lead screw from approximately 0.25 inches behind the front reference bearing to approximately 0.25 inches from the rear wall of the casting.

l. Mount the stepper motor (at each of the hold-down ears) to the sub-chassis using the same hex cap screws and hold-down clamps loosened in Step c. Tighten the screws just enough to keep the motor from turning, since the lead screw pre-load holds the positioner in place.

m. Tie-wrap the cable (as noted in Step a), and attach the cable connector to J9 on the PCBA.

n. Reassemble the drive; see Section 6.5.2 and Section 6.5.

o. Perform the following tests and adjustments in the order listed:

Procedure	Paragraph
Radial Alignment	4.4.2
Index Alignment	4.4.1
Track Zero Alignment	4.4.3
Radial Alignment (second time)	4.4.2

6.5.4 Head Load Solenoid (Optional - Single Head Models Only)

The Head Load Solenoid is accessible when the sub-chassis is removed from the outer structure; see Section 6.5.

NOTE

The replacement assembly includes the connector that mates to the Drive Electronics board. Since the same connector is used for several functions, if the original connector is not damaged it may be easier to use the original connector. To do this, at the suitable time in the following procedure, remove the original assembly's wires at the connector, detach the new assembly's wires from the (new) connector and insert them at the appropriate locations in the original connector.

a. Remove the drive motor belt, disconnect drive-to-PCBA connector J10, and cut the cable tie-wraps.

b. Extract the brown wire (pin 1) and the yellow wire (pin 2) from cable connector J10.

c. Remove the two head load solenoid mounting screws, and then lift the head load solenoid out of the drive mechanism (note the routing of the wires).

d. Route the solenoid wires through the hole in the casting as noted in Step b.

e. Set the replacement head load solenoid into its mounting cavity and gently position it until it seats on the two mounting holes. While holding the solenoid in place with one hand, secure it to the chassis using the same mounting screws removed in Step b.

f. Ensure the solenoid plunger moves freely.

g. Insert the brown wire (pin 1) and the yellow wire (pin 2) into cable connector J10.

h. Attach the solenoid connector to J10 on the PCBA, tie-wrap the cable, and install the drive motor belt (see Section 6.4).

i. Reassemble the drive; see Section 6.5.

j. Verify proper head load solenoid installation and operation by writing data and then reading the data written.

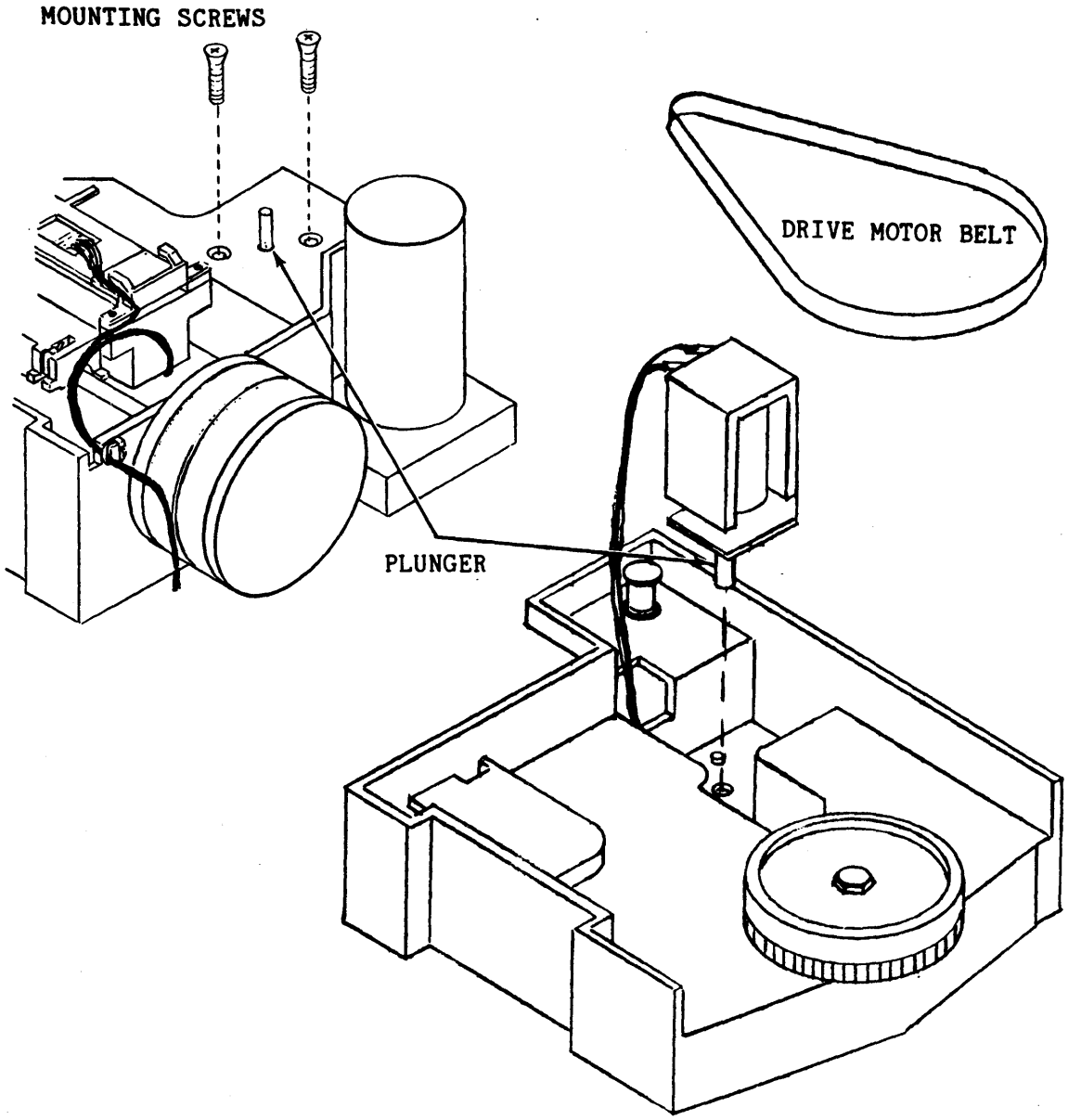


Figure 6-11. Head Load Solenoid

6.5.5 Track Zero Sensor

The Track Zero Sensor is accessible when the sub-chassis is removed from the outer structure; see Section 6.5.

NOTE

The replacement assembly includes the connector that mates to the Drive Electronics Board. Since the same connector is used for several functions, if the original connector is not damaged it may be easier to use the original connector. To do this, at the suitable time in the following procedure, remove the original assembly's wires at the connector, detach the new assembly's wires from the (new) connector and insert them at the appropriate locations in the original connector.

a. Disconnect the drive-to-cable connector at J10 on the PCBA, and cut the tie-wraps on the cable from the connector to the Track Zero Assembly.

b. Extract the green wire (pin 5), the white wire (pin 6), the black wire (pin 7), and the red wire (pin 8) from cable connector J10.

c. In order to make the Track Zero Sensor accessible, free the Track Zero Assembly as follows (refer to Figure 6-12):

   1) First remove the E-Clip from the adjustment screw.

   2) Then remove the two hex cap screws holding the assembly in place.

   3) Carefully unscrew the adjustment screw to release the Track Zero Assembly. Slide the assembly off the screw, and lift the assembly from the chassis (note the cable routing).

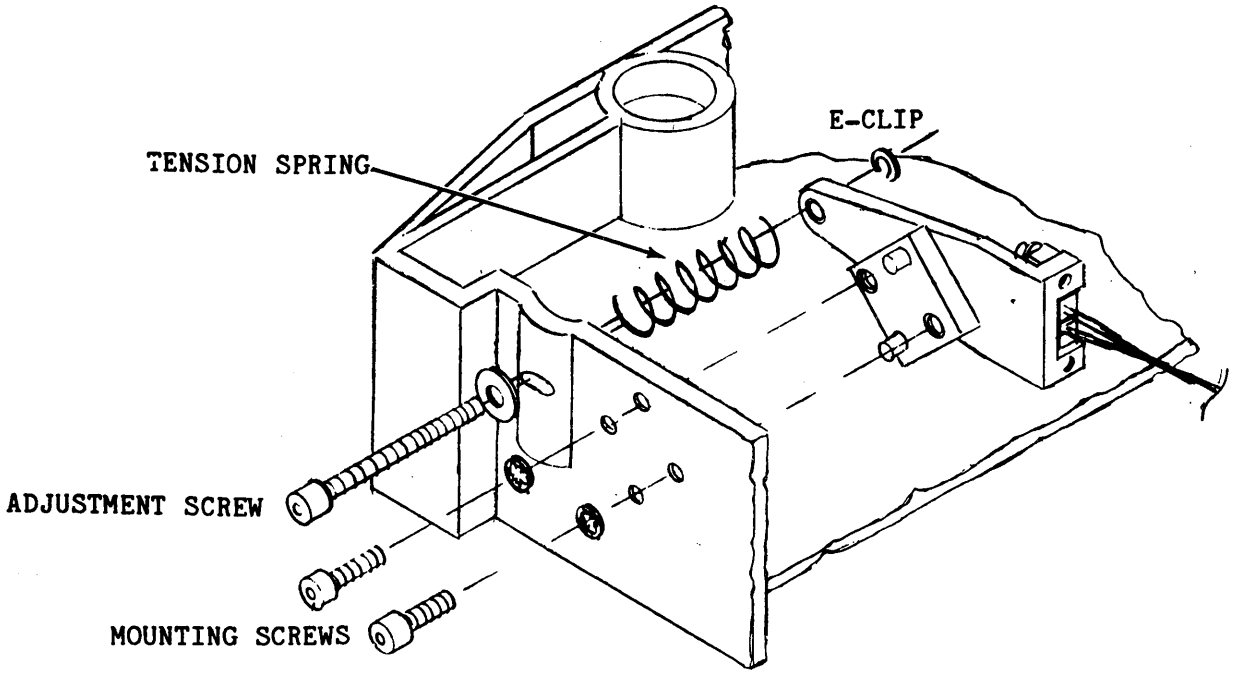


Figure 6-12. Track Zero Assembly

d. Remove the two screws and washers holding the Sensor Assembly to the Track Zero Mount; see Figure 6-13.

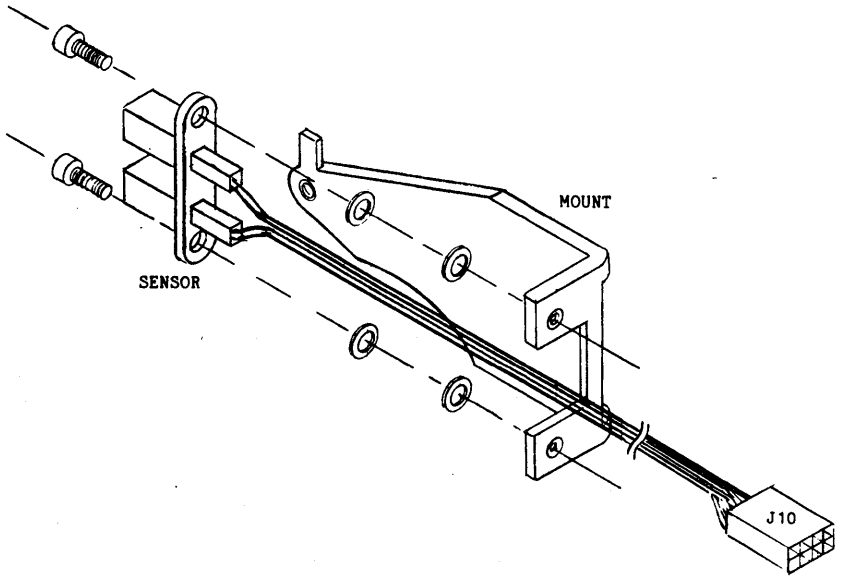


Figure 6-13. Track Zero Sensor

e. Screw the replacement Track Zero Sensor to the Track Zero Mount. Use the same hardware removed in Step d, placing two flat washers on each screw between the sensor and the mount.

f. Route the sensor wires through the hole in the bottom of the sub-chassis immediately behind the mounting position of the sensor.

g. Position the Track Zero Assembly on the side wall, placing the two locator pins in the appropriate holes. While holding the assembly in place, secure it with the two hex cap screws removed in Step c.

h. Ensure that the adjustment screw, with the washer on it, is inserted through the adjustment hole in the casting and that the tension spring is added to the screw. Thread the screw through the brass insert in the plastic mount. The screw should extend 0.25 ($\pm$0.125) inch beyond the other side. Place the E-Ring on the end of the screw (refer to Figure 6-12).

i. Turn the sub-chassis over and finish routing the wires as noted in Step c. Ensure slack exists in the wires between the hole and the Track Zero Assembly for adjustment purposes.

j. Insert the green wire (pin 5), the white wire (pin 6), the black wire (pin 7), and the red wire (pin 8) into cable connector J10. The contacts are internally barbed so the wires will not pull out. Tie-wrap the cable.

k. Reassemble the drive; see Section 6.5.

l. Check for proper Track Zero Sensor and Assembly installation by performing Step b of Section 4.4.3; adjust as required.

6.5.6 Tach Sensor Assembly

The Tach Sensor Assembly is part of the sub-chassis assembly and is accessible when the sub-chassis is removed from the outer structure; see Section 6.5.

NOTE

The replacement assembly includes the connector that mates to the Drive Electronics Board. Since the same connector is used for several functions, if the original connector is not damaged it may be easier to use the original connector. To do this, at the suitable time in the following procedure, remove the original assembly's wires at the connector, detach the new assembly's wires from the (new) connector and insert them at the appropriate locations in the original connector.

a. Disconnect the cable connector at J13 on the PCBA, and cut the tie-wraps on the cable.

b. Extract the green wire (pin 3), the white wire (pin 4), the black wire (pin 5), and the red wire (pin 6) from cable connector J13.

c. Remove the single hex cap screw and the flat washer that holds the Tach Sensor Assembly to the sub-chassis, and lift the Tach Sensor Assembly from the chassis (note the cable routing).

d. Align the replacement Tach Sensor Assembly with the mounting hole. The red and the black wires at the top of the sensor should be closest to the spindle.

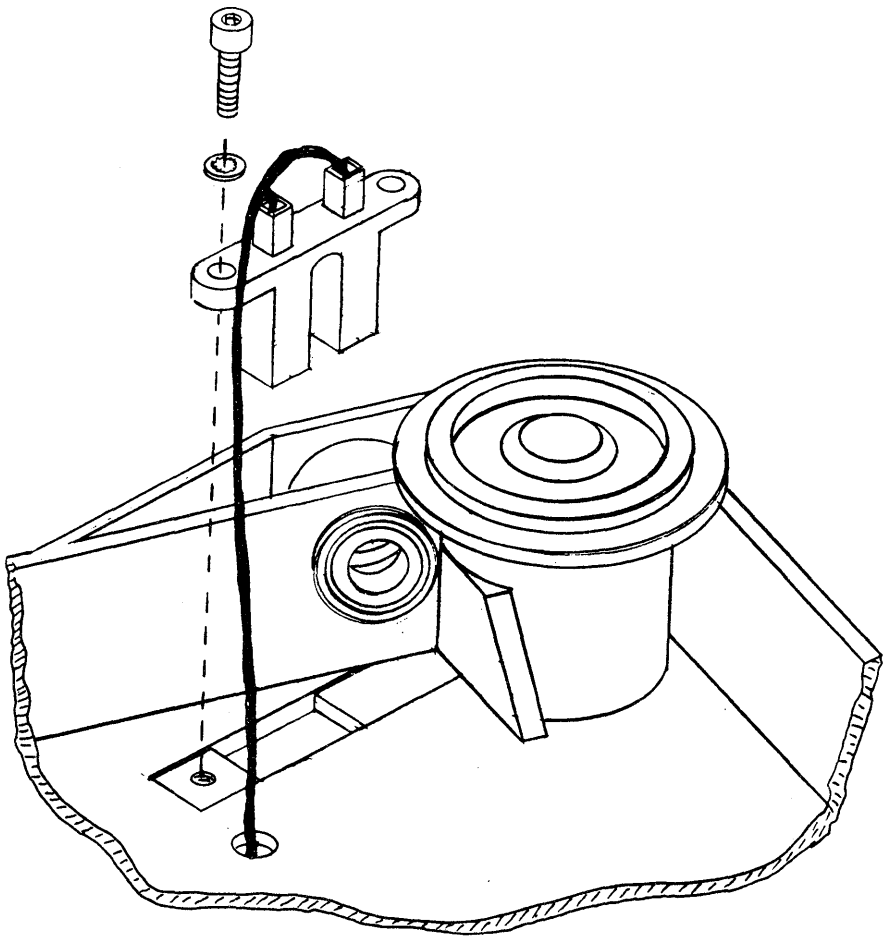


Figure 6-14. Tach Sensor Placement

e. Ensure that the pulley's fingers do not interfere with the Tach Sensor Assembly (rotate the pulley by hand one or two revolutions for verification); see Figure 6-15.

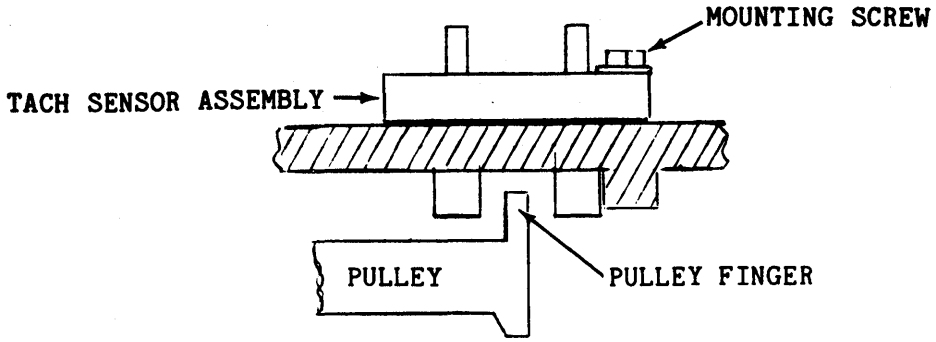


Figure 6-15. Sensor Alignment

f. Secure the assembly to the chassis using the same hex cap screw and flat washer removed in Step a.

g. Route the four-wire sensor cable to the connector (following the same path as noted in Step c).

h. Insert the green wire (pin 3), the white wire (pin 4), the black wire (pin 5), and the red wire (pin 6) into cable connector J13. The contacts are internally barbed so the wires will not pull out.

i. Attach the cable connector to J13 on the PCBA, and then tie-wrap the cable approximately two inches from the connector.

j. Reassemble the drive; see Section 6.5.

k. Check for proper Tach Sensor Assembly installation and operation by performing the Drive Motor Speed test (Section 4.3.1).

6.5.7 Index Sensor Harness Assembly

The Index Sensor Harness Assembly is part of the sub-chassis assembly and is accessible when the sub-chassis is removed from the outer structure; see Section 6.5.

NOTE

The replacement assembly includes the connector that mates to the Drive Electronics Board. Since the same connector is used for several functions, if the original connector is not damaged it may be easier to use the original connector. To do this, at the suitable time in the following procedure, remove the original assembly's wires at the connector, detach the new assembly's wires from the (new) connector and insert them at the appropriate locations in the original connector.

a. Disconnect the cable connector at J10 on the PCBA, and cut the tie-wrap on the cable.

b. Extract the blue wire (pin 3) and the orange wire (pin 4) from the cable connector (note the pin locations).

c. Pull the wires through the hole at the rear of the sub-chassis, and then free those wires up to the hole next to the Index Sensor Assembly (note the routing of the wires).

d. Remove the index spring using a flat blade screwdriver, and slide the entire assembly off its mounting post (see Figure 6-16, Detail B).

e. Slip the nut of the adjustment screw out of the slot in the casting; it may be necessary to unscrew the adjustment screw to release the nut (see Figure 6-16, Detail A).

f. Remove the assembly, pulling the wires through the routing hole. Set the assembly aside.

g. Route the wires of the replacement sub-assembly through the hole in the sub-chassis, immediately below the mounting position.

h. Place the replacement sub-assembly in its approximate mounting position; and slide the nut of the adjustment screw into the slot in the casting, ensuring that the washer is between the casting wall and the tension spring (see Figure 6-16, Detail A). Turn the adjustment screw clockwise several times to lock the nut in place.

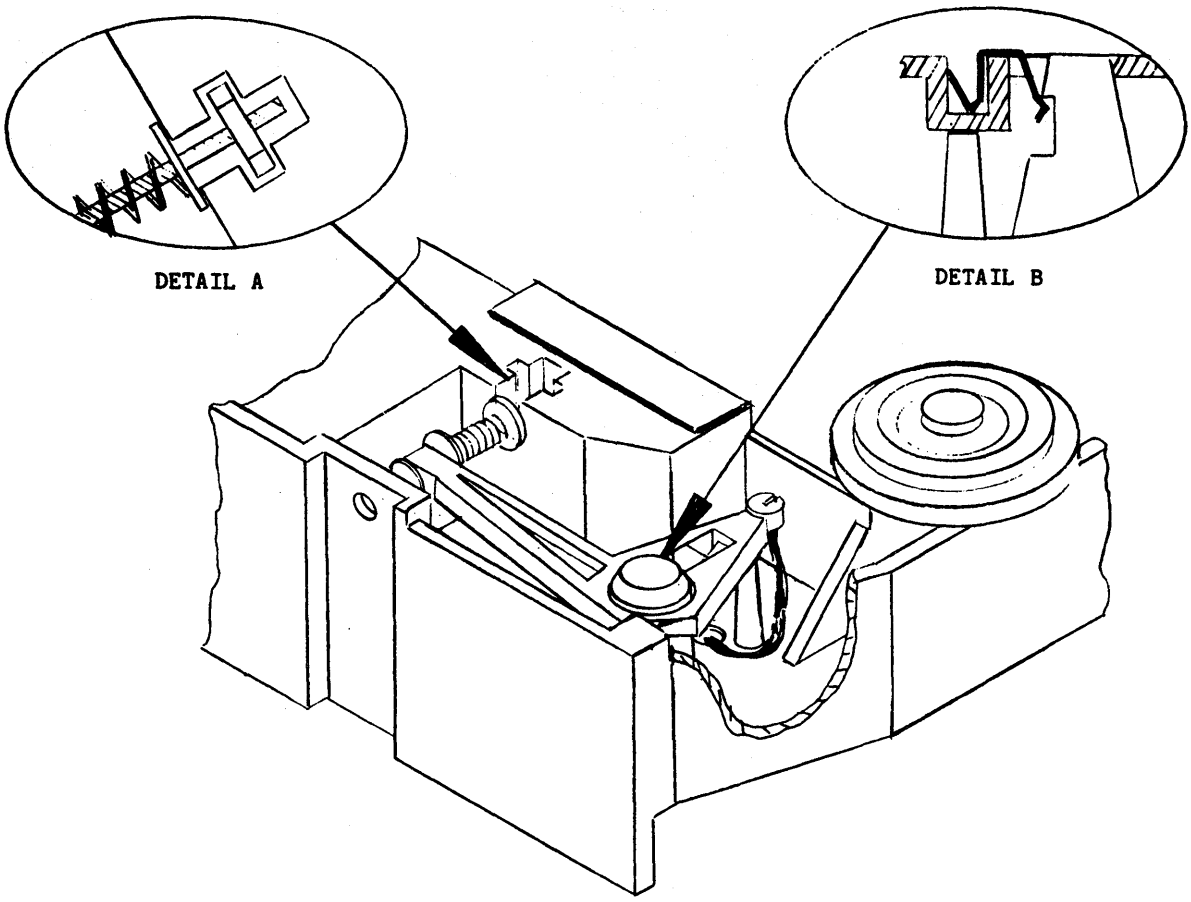


Figure 6-16. Index Sensor Assembly Placement

i. Slide the sub-assembly onto the mounting post and into position (see Figure 6-16, Detail B).

j. Push the index spring into place using a flat blade screwdriver.

k. Turn the drive over and finish routing the harness wires. Follow the same path, through the hole at the rear of the sub-chassis, as noted in Step c.

l. Insert the blue wire (pin 3) and the orange wire (pin 4) into connector J10, as noted in Step b. The contacts are internally barbed so the wires will not pull out.

m. Attach the cable connector to J10 on the PCBA, and then tie-wrap the cable approximately two inches from the connector.

n. Reassemble the drive; see Section 6.5.

o. Check for proper Index Sensor Assembly installation and operation by performing the Index Alignment test (Section 4.4.1).

6.6 OUTER STRUCTURE

The outer structure is a die cast frame supporting an internal sub-chassis. Removal of the sub-chassis is necessary for access to the assemblies and sub-assemblies housed in the outer structure.

6.6.1 Disk Clamp Assembly

The Disk Clamp Assembly consists of a clamp, a clamp spring, two thrust washers, a needle thrust bearing, and an E-Ring. The assembly is part of the outer structure and is accessible when the sub-chassis is removed; see Section 6.5.

a. While holding the disk clamp assembly , take off the E-Ring that holds the assembly to the outer structure (see Figure 6-17). Then remove the assembly.

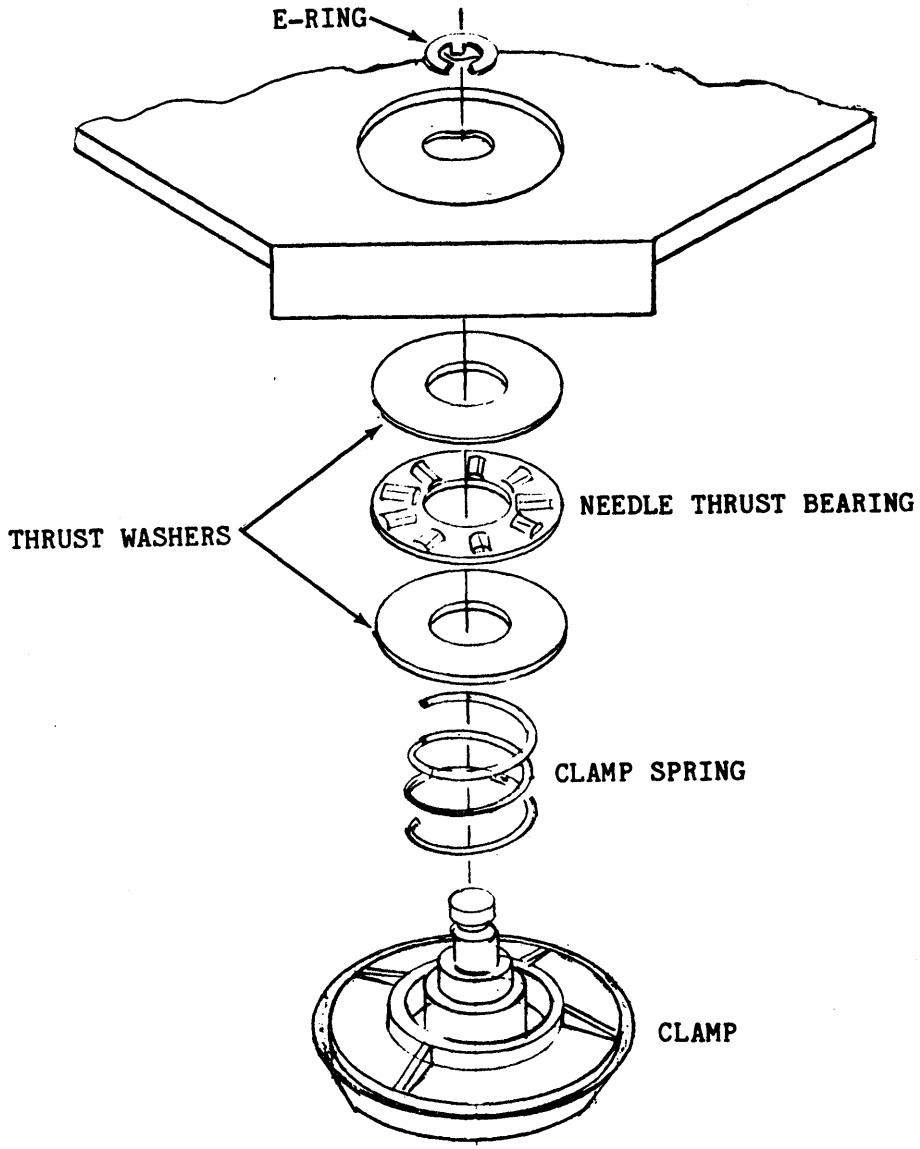


Figure 6-17. Disk Clamp Assembly

b. Slide the thrust washer, the needle thrust bearing, the other thrust washer, and the clamp spring off the clamp shaft.

c. Replace the defective part/component.

d. With the outer structure turned up-side down, place a thrust washer over the mounting hole.

e. Apply a light coat of grease (ANDOK B) to both sides of the needle thrust bearing, position it on the thrust washer, and place the other thrust washer on top of the bearing.

f. Set the spring on top of the thrust washer.

g. Take the disk clamp, and press the shaft down through the spring, slipping it through the washer-bearing combination.

h. Hold the Disk Clamp Assembly in place, turn the outer structure over (i.e., right-side up), and clip the E-Ring in place.

i. Reassemble the drive; see Section 6.5.

6.6.2 Jaw Lifter Assembly

The Jaw Lifter Assembly is accessible when the sub-chassis is removed from the outer structure; see Section 6.5.

a. Disconnect the connector to the bezel LED (note the orientation of the connector wires), and then remove the four screws holding the bezel to the outer structure. Set the bezel aside.

b. Rotate the Jaw Lifter Assembly to the vertical position.

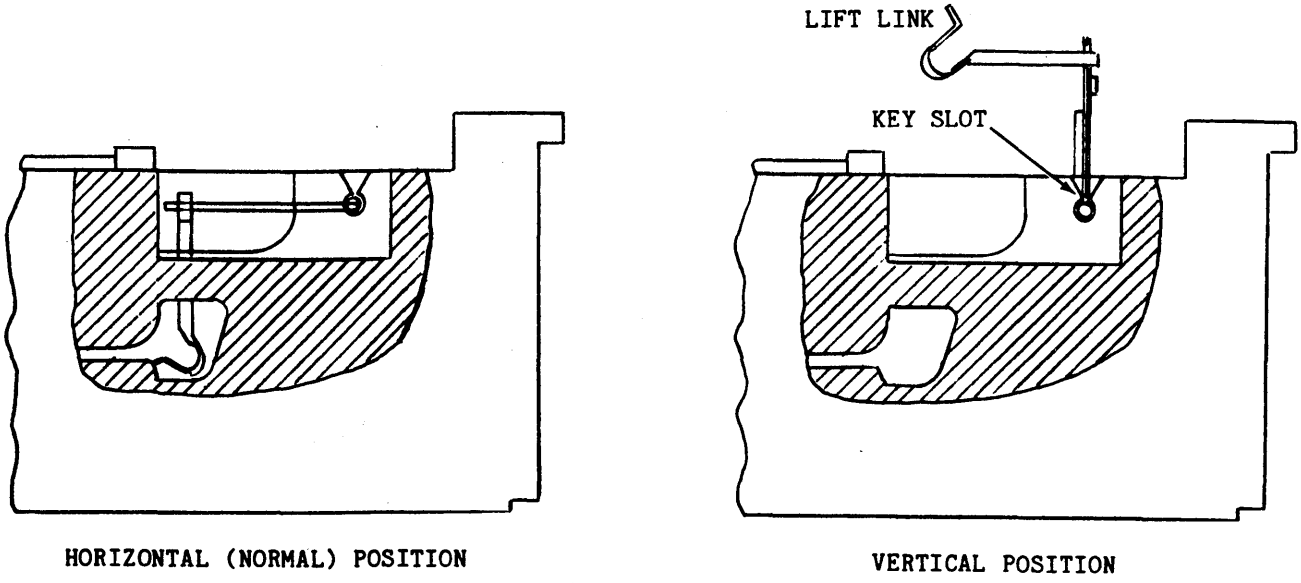


Figure 6-18. Jaw Lifter - Detailed

c. Pull the assembly torsion springs up and out of the key slots.

d. Insert the torsion springs of the replacement Jaw Lifter Assembly into the casting key slots of the outer structure. Press down until the the assembly "clicks" into place.

e. Rotate the assembly to the horizontal position, ensuring that each link is properly guided into the holes provided.

f. Attach the bezel to the outer structure using the same four mounting screws removed in Step a.

g. Close the door of the drive; and if the door is not flush to the front of the bezel, loosen the two screws in back of the door. Adjust the door so that it is flush, and retighten the screws.

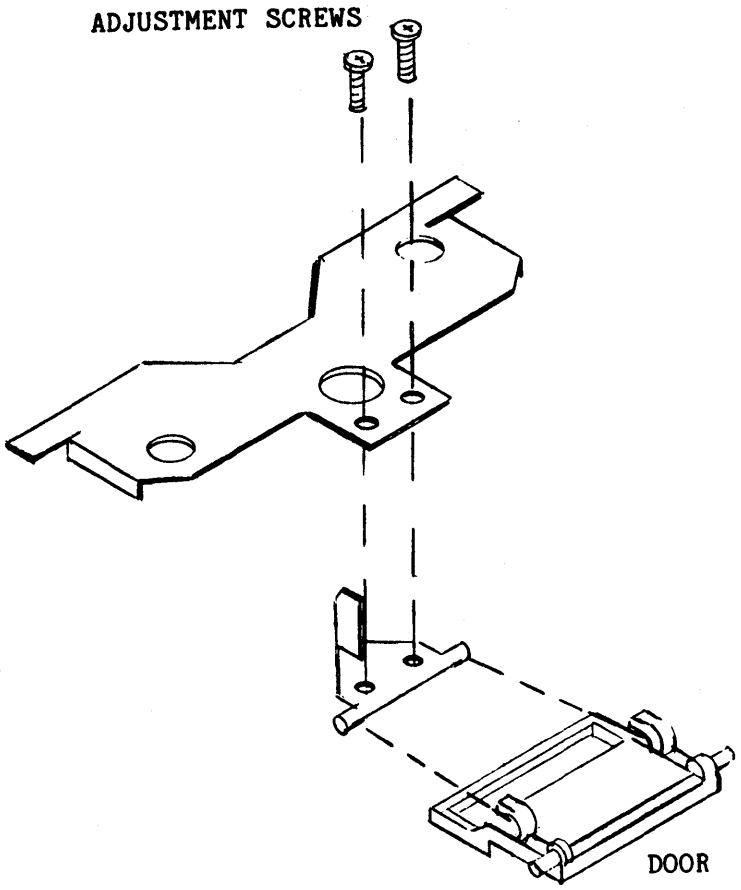


Figure 6-19. Door Alignment

h. Reconnect the harness connector to the bezel LED, orienting the connector as noted in Step a.

i. Reassemble the drive; see Section 6.5.

j. Check for proper Jaw Lifter Assembly installation and operation by inserting a disk in the drive and observing the clamping action as the door is alternately opened and closed.

6.6.3 Index LED Harness Assembly

The Index LED Harness Assembly is accessible when the sub-chassis is removed from the outer structure; see Section 6.5.

a. Disconnect J12, and free the harness up to the LED (note the routing of the cable wires).

NOTE

In the next step, the bushing is destroyed upon removal. The replacement assembly comes with another bushing.

b. Turn the outer structure up-side down. Using diagonal cutters, cut the flange holding the bushing (and LED) in place.

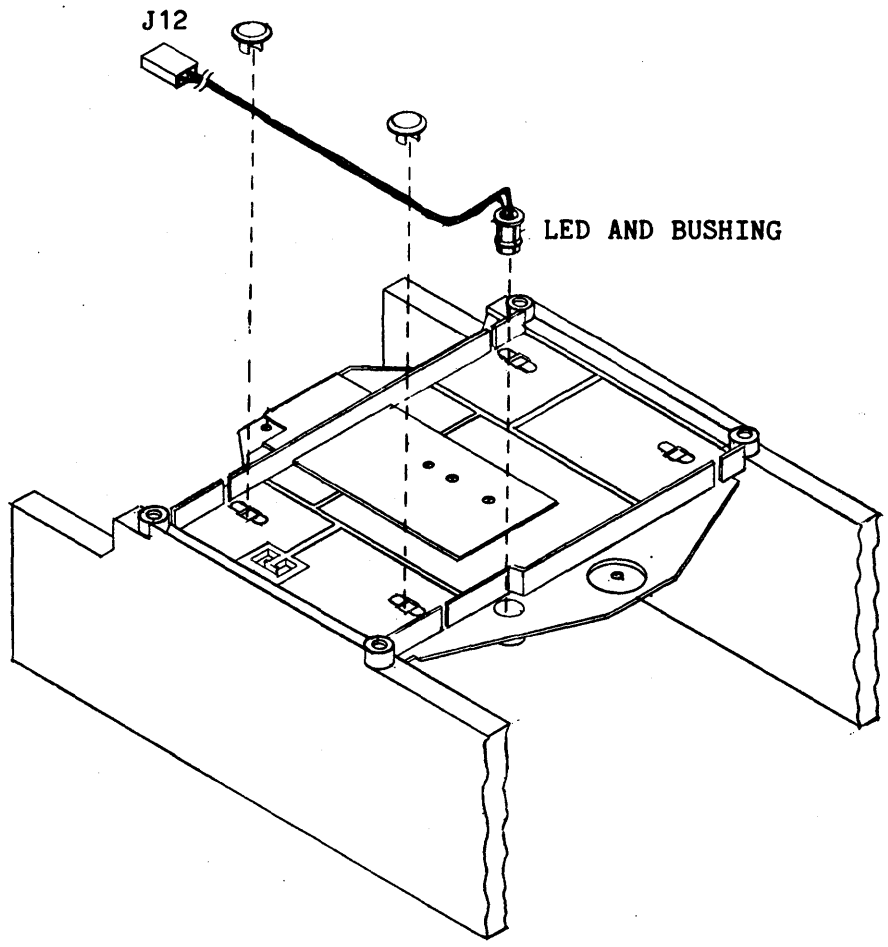


Figure 6-20. Index LED Assembly

c. With the structure up-side down, carefully push the bushing and LED out of the mounting hole with a screwdriver or small diameter nut-driver.

d. Turn the structure over (i.e., right-side up), and install the replacement assembly by first inserting the 2-pin connector and wires through the slot next to the Index LED mounting hole.

CAUTION

In the next step, a support block is used to prevent the top plate of the outer structure from bending.

e. Insert the Index LED sub-assembly (with the plastic bushing already on it) into the top plate of the outer structure. Set a support block beneath the mounting hole, and press the sub-assembly into place. Ensure that the plastic bushing fingers have captured the casting ridge uniformly.

f. Route the harness as noted in Step a.

g. Attach the cable connector to J12 on the PCBA.

h. Reassemble the drive; see Section 6.5.

i. Check for the proper Index LED Harness Assembly installation and operation by performing the Index Alignment test; see Section 4.4.1.

6.6.4 Write Protect Sensor

Access to the Write Protect Sensor is possible when the sub-chassis is removed from the outer structure; see Section 6.5.

a. Disconnect the 2-wire connector from the leads of the sensor.

NOTE

In the next step, the bushing is destroyed upon removal. The replacement assembly comes with another bushing.

b. Using diagonal cutters, cut the flange holding the bushing (and sensor) in place.

c. Leaving the structure up-side down, carefully push the bushing and sensor out of the mounting hole with a screwdriver.

d. Turn the structure right-side up, and insert the replacement sensor (with the plastic bushing already on it) into the mounting hole. Using a blunt instrument, press the assembly in place, ensuring the plastic bushing is uniformly and properly seated.

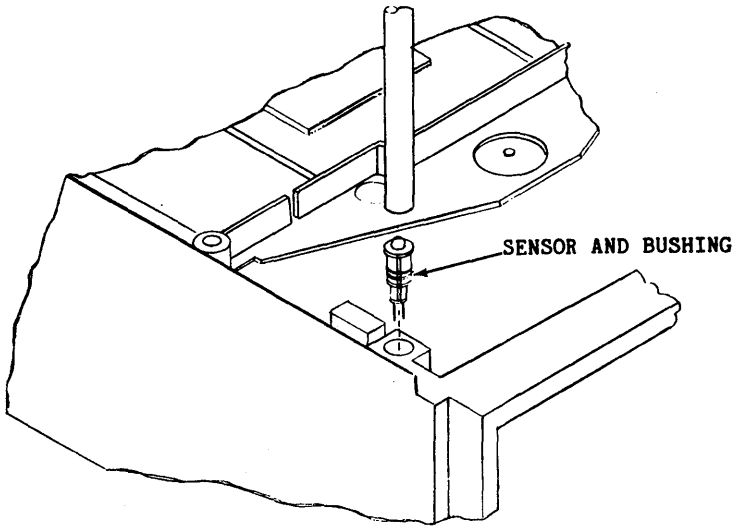


Figure 6-21. Write Protect Sensor Assembly

e. Attach the 2-pin cable connector to the sensor leads. Ensure the gray cable wire goes to the emitter (the Micropolis-marked red lead) of the sensor.

f. Reassemble the drive; see Section 6.5.

g. Check for proper Write Protect Sensor installation and operation by performing the Write Protect Sensor test; see Section 4.3.5.

6.6.5 In-Use LED

The In-Use LED assembly is accessible when the sub-chassis is removed from the outer structure; see Section 6.5.

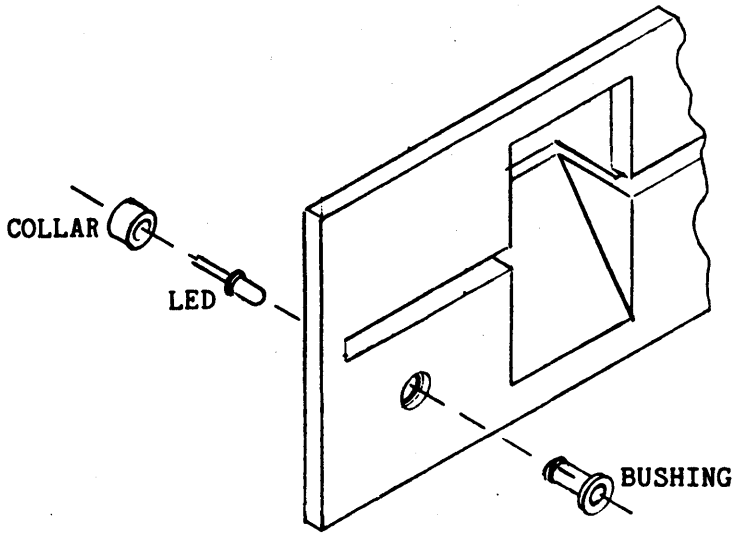


Figure 6-22. In-Use LED Assembly

a. Disconnect the 2-wire connector from the leads of the LED.

b. Remove the collar holding the bushing and the LED in place.

c. Remove the defective LED from the rear of the bezel, and insert (from the rear) the replacement LED into the bushing.

d. While holding the LED and the bushing from the front of the bezel, install the bushing collar (from the rear, over the bushing), thereby locking the LED and the bushing in place. Make sure the collar is flush to the rear of the bezel.

e. Attach the 2-pin cable connector to the leads of the LED. Ensure that the yellow cable wire goes to the anode (the Micropolis-marked red lead) of the sensor.

f. Reassemble the drive; see Section 6.5.

g. Check for the proper installation and operation of the In-Use LED by observing the LED when the drive is alternately selected and deselected.

SECTION VII

PARTS LISTS

7.1 INTRODUCTION

This section provides a set of parts lists for the 1115-Series Flexible Disk Drive. Item numbers are keyed to the drawings in Section 8 of this manual.

TABLE 7-1. TOP ASSEMBLY

(See Figure 8-1)

Item	Qty	Micropolis Part Number	Description
Ref			Top Assembly
		901001	1115-II, Single sided, 100 TPI, No options
		901002	1115-II, Single sided, 100 TPI, with Head Load Solenoid option
		901003	1115-IV, Double sided, 100 TPI, No options
		901004	1115-V, Single sided, 96 TPI, No options
		901005	1115-V, Single sided, 96 TPI, with Head Load Solenoid option
		901006	1115-VI, Double sided, 96 TPI, No Options
		901007	1106-II, Single sided, 100 TPI, Without Index Sensor or Track Ø Sensor, Subchassis only
		901008	1106-IV, Double sided, 100 TPI, Without Index Sensor or Track Ø Sensor, Subchassis only
		901009	1115-V, Single sided, 96 TPI, with Door Lock Solenoid option
		901010	1115-VI, Double sided, 96 TPI, with Door Lock Solenoid option

TABLE 7-1. TOP ASSEMBLY (continued)

Item	Qty	Micropolis Part Number	Description
3	1		Printed Circuit Board Assembly (See Table 7-2)
		102237-51-8	MFM, Single Head, No Options (Used on 901001 and 901004)
		102237-52-6	MFM, Double Head, No Options (Used on 901003 and 901006)
		102237-53-4	MFM, Single Head, Head Load option (Used on 901002 or 901005)
		102237-54-2	MFM, Single Head, Door Lock option (Used on 901009)
		102237-55-9	MFM, Double Head, Door Lock option (Used on 901010)
6	4	700-0604-4	#6-32 x 1/4 Pan Head Phillips Screw
7	1	102252-01-2	Product Label (Used on all drives and subchassis units)
9	1	102267-01-0	Door Lock Interposer Spring (901009 and 901010 only)
10	1	102291-01-0	Outer Structure Assembly (See Table 7-3) (Used on all complete drives)
11	1		Subchassis Assembly (See Table 7-9)
		102292-01-8	(Used on 901001)
		102292-02-6	(Used on 901002)
		102292-03-4	(Used on 901003)
		102292-04-2	(Used on 901004 and 901009)
		102292-05-0	(Used on 901005)
		102292-06-7	(Used on 901006 and 901010)
		102292-07-5	(Used on 901007 and 901008)
14	1	116-0011-1	Resistor Network — Termination Network (Only used on the last drive on the interface cable.)
15	1	680-0204-7	Address Jumper — W1, W2, W3, W4, or W5 (See Table 2-1 or Section 3.3.2.1 for address selection information.)

TABLE 7-2. DRIVE ELECTRONICS PCBA

PART NUMBER (see below)

Item	Qty	Micropolis Part Number	Description	Remarks
Ref		102237-XX-X	Drive Electronics PCBA	
		-51-8	96/100 TPI, MFM, Single Head, No Options	
		-52-6	96/100 TPI, MFM, Dual Head, No Options	
		-53-4	96/100 TPI, MFM, Single Head, Head Load Solenoid	
		-54-2	96/100 TPI, MFM, Single Head, Door Lock Solenoid	
		-55-9	96/100 TPI, MFM, Dual Head, Door Lock Solenoid	
3	1	0102236	Process Board	
7	1	0102258	Door Lock Solenoid	(Option)
8	35	100-0000-8	Resistor, 0 ohm, 5%, 1/4W	R6 THRU 35,R39,R40
9	5	100-1000-7	Resistor, 100 ohm, 5%, 1/4W	R23,R57,R58,R64,R98
10	9	100-1001-5	Resistor, 1K, 5%, 1/4W	R17,R25,R27,R28,R29,R80, R82,R83,R86
11	3	100-1003-1	Resistor, 100K, 5%, 1/4W	R59,R63,R84
12	1	100-1200-3	Resistor, 120 ohm, 5%, 1/4W	R100
13	1	100-1201-1	Resistor, 1.2K, 5%, 1/4W	R81
14	8	100-1202-9	Resistor, 12K, 5%, 1/4W	R14,R33,R38,R42,R43, R44,R56,R70
15	4	100-1500-6	Resistor, 150 ohm, 5%, 1/4W	R1,R62,R90,R91
16	3	100-1501-4	Resistor, 1.5K, 5%, 1/4W	R20,R21,R24
17	3	100-1800-0	Resistor, 180 ohm, 5%, 1/4W	R18,R61,R68
18	3	100-2200-2	Resistor, 220 ohm, 5%, 1/4W	R89,R92,R93
19	10	100-2201-0	Resistor, 2.2K, 5%, 1/4W	R2,R7,R8,R31,R49,R67, R76,R77,R95,R96

TABLE 7-2. DRIVE ELECTRONICS PCBA (continued)

Item	Qty	Micropolis Part Number	Description	Remarks
20	4	100-2202-8	Resistor, 22K, 5%, 1/4W	R4,R5,R41,R79
21	4	100-2702-7	Resistor, 27K, 5%, 1/4W	R45,R46,R66,R99
22	6	100-3300-9	Resistor, 330 ohm, 5%, 1/4W	R19,R22,R26,R52,R55,R103
23	4	100-4700-9	Resistor, 470 ohm, 5%, 1/4W	R53,R88,R94,R97
24	4	100-4702-5	Resistor, 47K, 5%, 1/4W	R3,R9,R85,R104
25	1	100-5600-0	Resistor, 560 ohm, 5%, 1/4W	R50
26	1	101-0010-5	Resistor, 1 ohm, 5%, 1/2W	R87
27	1	101-2200-0	Resistor, 220 ohm, 5%, 1/2W	R65
28	2	101-3900-4	Resistor, 390 ohm, 5%, 1/2W	R36,R37
29	3	105-1003-0	Resistor, 100K, 1%, 1/4W	R69,R71,R75
30	2	105-1962-7	Resistor, 19.6K, 1%, 1/4W	R10,R13
31	3	105-2742-2	Resistor, 27.4K, 1%, 1/4W	R60,R72,R73
32	2	105-3651-4	Resistor, 3.65K, 1%, 1/4W	R6,R32
33	1	105-5901-1	Resistor, 5.9K, 1%, 1/4W	R54
34	2	105-6191-8	Resistor, 6.19K, 1%, 1/4W	R11,R12
35	1	116-0011-1	Resistor Network, 220/330 ohm, SIP	RN1

TABLE 7-2. DRIVE ELECTRONICS PCBA (continued)

Item	Qty	Micropolis Part Number	Description	Remarks
36	7	163-3304-9	Capacitor, Tantalum 3.3uF,25V	C3,C17,C26,C28,C42,C44,C51
37	1	163-3306-4	Capacitor, Tantalum, 33uF, 16V	C53
38	2	163-4703-1	Capacitor, Tantalum, .47uF, 25V	C43,C47
39	17	169-1002-8	Capacitor, Ceramic, .01uF, 50V	C4,C8,C11,C12,C13,C14 C15,C16,C21,C24,C25,C27, C30,C33,C38,C49,C52
40	2	170-1000-0	Capacitor, Monolithic, 330pF, 50V	C7,C22
41	1	170-3300-2	Capacitor, Monolithic, 4700uF, 50V	C50
42	2	170-4700-2	Capacitor, Monolithic, 470pF, 50V	C20,C31
43	2	170-7500-3	Capacitor, Monolithic, 750pF, 50V	C18,C19
44	1	171-1501-5	Capacitor, Monolithic, 1500pF, 50V	C45
45	5	171-2202-9	Capacitor, Monolithic, .022uF, 50V	C37,C39,C40,C46,C48
46	2	171-4701-8	Capacitor, Monolithic, 4700pF, 50V	C23,C35
47	4	171-4702-6	Capacitor, Monolithic, .047uF, 50V	C5,C10,C34,C41
48	3	172-4703-2	Capacitor, Monolithic .47uF, 50V	C29,C32,C36
49	2	190-0240-1	Inductor, 24uH	L3,L4
50	3	190-1000-8	Inductor, 100uH	L1,L2,L5
51	25	200-446-76	Diode, Switch	CR1,CR2,CR3,CR4,CR6 THRU CR23,CR35,CR39,CR40
52	1	210-5223-8	Zener Diode, 2.7V, 500mW	CR5

TABLE 7-2. DRIVE ELECTRONICS PCBA (continued)

Item	Qty	Micropolis Part Number	Description	Remarks
53	1	210-5228-7	Zener Diode, 3.9V, 500mW	CR34
54	1	210-5250-1	Zener Diode, 20V, 500mW	CR33
55	8	220-4002-6	Diode, Semipower	CR26,CR27,CR28,CR29,CR30, CR32,CR36,CR38
56	1	240-0060-6	Diode, IR	CR37 (Write Protect)
57	1	240-0094-5	Diode, IR	CR25 (Door Switch)
58	1	250-0005-0	Supressor	CR24
59	2	300-4400-2	Transistor, 2N4440	Q2,Q7
60	5	300-4402-8	Transistor, 2N4402	Q1,Q2,Q4,Q5,Q10
61	1	330-0014-2	Photo-Transistor	Q6 (Door Switch)
62	1	340-0110-7	Power Driver Transistor, TIP110	Q9
63	1	340-0125-5	Power Driver Transistor, TIP125	Q8
64	3	400-0014-3	IC, 74LS14	U1,U4,U5
65	1	400-0026-7	IC, 74LS26	U8
66	3	400-0074-7	IC, 74LS74	U3,U12,U13
67	1	400-0086-1	IC, 74LS86	U15
68	1	400-0174-5	IC, 74LS174	U14
69	2	401-0016-6	IC, 7416	U2,U7
70	1	401-0017-4	IC, 7417	U6
71	1	406-0437-3	IC, Stepper Driver	U18
72	1	406-0452-2	IC, Driver, 75452	U19
73	1	407-0004-9	IC, 74LS123	U16
74	1	408-0008-8	IC, 8T96	U10

TABLE 7-2. DRIVE ELECTRONICS PCBA (continued)

Item	Qty	Micropolis Part Number	Description	Remarks
75	1	410-0311-2	IC, Comparator LM311	U22
76	1	410-0339-3	IC, LM339	U20
77	1	410-0556-2	IC, Dual Timer	U9
78	2	410-0592-7	IC, Video Amplifier, NE 592	U17,U21
79	1	430-0007-4	Microprocessor, 6500/1	U11
80	1	500-2000-7	Crystal, 2MHz	Y1
81	A/R	650-0003-6	Thermal Compound	
82	2	650-0005-1	Heat Sink	
83	1	680-0204-7	2-Pin Jumper	J0
84	1	680-0206-2	1X2 Male Header	TP7
86	1	680-0405-0	1X4 Power Connector	J8A
87	2	680-0406-8	2X2 Male Header	TP8,TP11
88	1	680-0701-2	1X7 Power Connector	J7
89	1	680-0702-0	1X7 Right-Angle Header	J5
90	1	680-0703-8	1X7 Right-Angle Header	J4
91	1	680-1008-1	10-Pin SIP Socket	J3
92	1	680-1009-9	2X5 Pin Header	J2
93	1	680-2801-8	2X13 Right-Angle Header	J9
95	2	700-0605-1	#6-32 x 5/16 Pan Head Phillips Screw	
96	2	710-0602-7	#6-32 Hex Nut with Lock Washer	

TABLE 7-3. OUTER STRUCTURE ASSEMBLY

(See Figure 8-2)

PART NUMBER 102291-01-0

Item	Qty	Micropolis Part Number	Description	Remarks
2	1	102218-01-3	Machined Outer Structure	
3	1	102219-01-1	Disk Clamp Spring	
5	1	102222-01-5	Index LED Harness Assembly	(See Table 7-4)
6	1	102224-01-1	File Protect Sensor and In-Use LED Harness Assembly	(See Table 7-5)
8	1	102281-01-1	Head Lifter Assy	
9	1	102282-01-9	File Protect Transistor Assy	
12	1	102297-01-6	Disk Clamp Assembly	(See Table 7-6)
13	1	102298-01-4	Jaw Lifter Assembly	(See Table 7-7)
17	2	704-0409-0	#4-40 x 9/16" Socket Head Screw	
18	1	707-1101-5	.110" Dia. External E-Ring	Disk Clamp Shaft
19	2	712-2502-3	Thrust Washer	Disk Clamp Thrust Bearing
20	1	715-2005-1	Extension Spring	Head Lifter
22	1	716-2504-0	Needle Thrust Bearing	Disk Clamp Assembly
23	A/R	732-0003-2	Grease - ANDOK B	Disk Clamp Thrust Bearing
25	1	102275-01-3	Bezel Assembly	(See Table 7-8)
29	4	702-0606-5	#6-32 x 3/8 Black Screw	Bezel
31	1	683-1801-3	3/16 Fast-On Male Tab	Ground Terminal
32	1	703-0604-8	#6-32 x 1/4 Hex Head Screw	Ground Terminal

TABLE 7-4. INDEX LED HARNESS ASSEMBLY

PART NUMBER 102222-01-5

Item	Qty	Micropolis Part Number	Description	Remarks
5	1	102268-03-4	Yellow Wire	
6	1	102268-04-2	Green Wire	
8	A/R	670-0002-6	1/8" Heat-Shrinkable Tubing	
10	1	680-0203-9	2-Pin Housing	J 12
12	4	683-1106-7	Contact Pin	
14	1	240-0031-7	I.R. Emitting LED	Index Emitter
16	1	102233-01-2	Index LED Bushing	

TABLE 7-5. FILE PROTECT SENSOR AND IN-USE LED HARNESS ASSEMBLY

PART NUMBER 102224-01-1

Item	Qty	Micropolis Part Number	Description	Remarks
3	1	102268-05-4	Yellow Wire	
4	1	102268-06-7	Brown Wire	
5	1	102268-01-8	Purple Wire	
6	1	102268-02-6	Gray Wire	
8	2	680-0203-9	2-Pin Housing	
9	1	680-0407-6	2x2 Pin Housing	J11
10	8	681-1106-7	Contact Pin	

TABLE 7-6. DISK CLAMP ASSEMBLY

PART NUMBER 102297-01-6

Item	Qty	Micropolis Part Number	Description	Remarks
7	1	100027-01-0	Clamp	
10	1	102220-01-9	Disk Shaft Clamp	

TABLE 7-7. JAW LIFTER ASSEMBLY

PART NUMBER 102298-01-4

Item	Qty	Micropolis Part Number	Description	Remarks
3	1	102201-01-9	Latch	Hinge
4	1	102202-01-7	Latch Hinge	
7	1	102240-01-7	Crossmember	
8	1	102241-01-5	R.H. Torsion Spring	
9	1	102242-01-3	L.H. Torsion Spring	
10	1	102243-01-1	Torsion Spring Spacer	
11	2	102244-01-9	Link	Torsion Spring
14	2	706-0402-0	Latch Screw	

TABLE 7-8. BEZEL ASSEMBLY

PART NUMBER 102275-01-3

Item	Qty	Micropolis Part Number	Description	Remarks
3	1	102200-01-1	Bezel	
5	1	622-0006-8	Visible Red LED	In-Use LED, including bushing and collar

TABLE 7-9. SUBCHASSIS ASSEMBLY

(See Figure 8-3)

PART NUMBER (See Below)

Item	Qty	Micropolis Part Number	Description	Remarks
Ref		102292-	Subchassis Assembly	
		-01-8		Used on 901001
		-02-6		Used on 901002
		-03-4		Used on 901003
		-04-2		Used on 901004 and 901009
		-05-0		Used on 901005
		-06-7		Used on 901006 and 901010
		-07-5		Used on 901007 and 901008
3	1	102203-01-5	Hub and Shaft	
4	1	102208-01-4	Carriage Load Spring	Carriage Front Leg
5	1	102208-02-2	Carriage Load Spring	Carriage Rear Leg
6	1	102211-01-8	Machined Subchassis	
8	2	102228-01-2	Stepper Motor Clamp	
9	1		Head Assembly	(See Table 7-11)
		102274-01-6	Single Sided	(Used on -01, -02, -04, -05, -06, -07)
		102274-02-4	Double Sided	(Used on -03, -08)
10	1	102280-01-3	Spindle Pulley Assembly	
11	1	102248-01-0	Track Zero Adjustment Screw	(Not used on -07 or -08)
13	2	102251-01-4	Dowel Pin	Subchassis Pivot
14	2	102251-02-2	Dowel Pin	Subchassis Lift Link
15	1	102253-01-0	Subchassis Label	
18	1	102257-01-1	Head Load Solenoid Assembly	(Used on -02, -05, -06); (See Table 7-13)
19	1		Step Motor Assembly	(See Table 7-14)
		102293-01-6	96 TPI	(Used on -04, -05, -06)
		102293-02-4	100 TPI	(Used on -01, -02, -03, -07, -08)

TABLE 7-9. SUBCHASSIS ASSEMBLY (continued)

Item	Qty	Micropolis Part Number	Description	Remarks
20	1	102294-01-4	Tach Sensor Assembly	(See Table 7-15)
21	1	102295-01-0	Index Assembly	(Not used on -07 or -08); (See Table 7-16)
22	1	102296-01-8	Track Zero Assembly	(Not used on -07 or -08); (See Table 7-17)
23	1	102299-01-2	Spindle Motor Assembly	(See Table 7-18)
26	5	669-1001-9	4" Tie Wrap	
28	1	701-0605-9	#6-32 x 5/16 Hex Head Screw	Spindle Pulley
28a	2	702-2405-0	#4-40 x 5/16 Flat Head Screw	Head Load Solenoid Assy (Used on -02, -05, -06)
29	2	703-0606-3	#6-32 x 3/8 Taptite Screw	Spindle Motor Assembly
30	5	704-0404-1	#4-40 x 1/4 Socket Head Screw	Track Zero Assembly, Stepper Motor, Tach Mount
32	1	707-2501-5	.25" Dia. Retaining Ring	Step Motor Reference
33	2	707-1251-4	.094" Dia. Grip Ring	Subchassis Pivot Pins
36	1	711-0401-2	#4 Flat Washer, .016" Thick	Track Ø Adjustment
37	4	711-0405-3	#4 Internal Lock Washer	Stepper Motor, Track Zero Assembly
38	3	711-0603-3	#6 External Lock Washer	Spindle Motor, Spindle Pulley
39	1	707-0941-5	3/32 E-Ring	Track Ø Stop
41	1	715-1006-9	Compression Spring	Track Ø Adjustment
44	1	716-2505-7	Bearing, .25" ID ANDOK B	Step Motor Reference
45	2	716-3701-1	Bearing, .375" ID	Spindle
47	1	102245-01-6	Jaw Open Spring	(Not used on -07 or -08)
49	1	102266-01-2	Platen Shim	

TABLE 7-10. INDEX SENSOR HARNESS ASSEMBLY

PART NUMBER 102222-01-5

Item	Qty	Micropolis Part Number	Description	Remarks
5	1	102268-03-4	Yellow Wire	
6	1	102268-04-2	Green Wire	
8	A/R	670-0002-6	1/8" Heat-Shrinkable Tubing	
10	1	680-0203-9	2 Pin Housing	J12
12	4	683-1106-7	Contact Pin	
14	1	240-0031-7	IR Emitting LED	Index Emitter
15	1	102233-01-2	Index LED Bushing	

TABLE 7-11. HEAD ASSEMBLY

PART NUMBER (see below)

Item	Qty	Micropolis Part Number	Description	Remarks
REF			Head Assembly	
		102274-01-6	Single Sided, MFM	
		102274-02-4	Double Sided, MFM, Aligned	
3	1		Head Carriage Assy	(See Table 7-12)
		102230-01-8	Single Sided	
		102231-01-6	Double Sided	
5	1	102213-01-4	Platen Load Spring	
6	1	102214-01-2	Platen Load Clamp	
7	1	704-0406-4	#4-40 x 3/8 Socket Head Screw	Platen Load Clamp
8	1	711-0400-5	#4 Internal Lock Washer	Platen Load Clamp

TABLE 7-12. HEAD CARRIAGE ASSEMBLY

PART NUMBER (See Below)

Item	Qty	Micropolis Part Number	Description	Remarks
Ref			Head Carriage Assy	
		102230-01-8		Single Sided
		102231-01-6		Double Sided
1	1	100074-01-2	Head Load Pad	Upper Arm (Single Sided only)
2	A/R	100412	5-Conductor Cable	
3	1	102206-01-8	Carriage	
4	1	102207-01-6	Index	
5	1	102209-01-2	Upper Arm	(Single Sided only)
6	1	102213-01-4	Platen Load Spring	
7	1	102214-01-2	Platen Load Clamp	
10	1			
		680-0704-6	7-Pin Housing	J4 (Single Sided)
		680-1405-0	7x2 Pin Housing	J4, J5 (Double Sided)
11		681-1108-3	Contact Pin	
	6			(Single Sided)
	12			(Double Sided)
12	1	671-0007-3	Strain Relief Pin	Head Connector
13	1	704-0406-4	#4-40 x 3/8 Socket Head Screw	Platen Load Clamp
15	1	711-0405-3	#4 Internal Lock Washer	Platen Load Clamp

TABLE 7-13. HEAD LOAD SOLENOID ASSEMBLY

PART NUMBER 102257-01-1

Item	Qty	Micropolis Part Number	Description	Remarks
6	1	102257-01-1	Head Load Solenoid	
7	A/R	660-2404-3	Yellow Wire	
8	A/R	660-2401-9	Brown Wire	
9	A/R	670-0002-6	1/8" Heat-Shrinkable Tubing	
10	2	683-1106-7	Contact Pin	

TABLE 7-14. STEP MOTOR ASSEMBLY

PART NUMBER (See Below)

Item	Qty	Micropolis Part Number	Description	Remarks
Ref			Step Motor Assembly	
		102293-01-6	96 TPI	
		102293-02-4	100 TPI	
6	1		Step Motor - B	
		102212-01-6	96 TPI	
		102212-02-4	100 TPI	
10	1	680-0605-5	2x3 Pin Housing	J9
12	6	683-1106-7	Contact Pin	

TABLE 7-15. TACH SENSOR ASSEMBLY

PART NUMBER 102294-01-4

Item	Qty	Micropolis Part Number	Description	Remarks
6	1	240-0824-5	Sensor Assembly	Spindle Tach Transducer
10	1	680-0605-5	2x3 Pin Housing	J12
12	4	683-1106-7	Contact Pin	

TABLE 7-16. INDEX ASSEMBLY

PART NUMBER 102295-01-0

Item	Qty	Micropolis Part Number	Description	Remarks
1	1	102223-01-3	Index Harness Assembly	
4	1	102205-01-0	Index Housing	
5	1	1-2249-01-8	Index Housing Spring	
10	1	704-0418-1	#4-40 x 1 1/8 Socket Head Screw	Adjustment Screw
12	1	710-0401-4	#4 Hex Nut	
14	3	711-0401-2	#4 Flat Washer, .016 Thick	
17	1	715-1005-1	Compression Spring	

TABLE 7-17. TRACK ZERO ASSEMBLY

PART NUMBER 102296-01-8

Item	Qty	Micropolis Part Number	Description	Remarks
2	1	102204-01-3	Track Ø Mount	
5	1	240-0824-5	Sensor Assembly	Track Ø Transducer
7	1	680-0809-3	2x4 Pin Housing	J10
9	4	683-1106-7	Crimp-On Pin	Sensor Assembly
12	2	704-0406-4	#4-40 x 3/8 Socket Head Screw	Sensor Assembly
15	4	711-0401-2	#4 Flat Washer, .016 Thick	Sensor Assembly

TABLE 7-18. SPINDLE DRIVE MOTOR ASSEMBLY

PART NUMBER 102299-01-2

Item	Qty	Micropolis Part Number	Description	Remarks
6	1	600-0008-0	Spindle Motor	Without Tach
9	2	683-1106-7	Contact Pin	

SECTION VIII

ASSEMBLY DRAWINGS AND SCHEMATIC DIAGRAM

8.1 INTRODUCTION

This section presents mechanical assembly drawings and the circuit board assembly drawing and schematic diagram for the 1115-Series of 5 1/4-inch Flexible Disk Drives. These figures are given in the following order:

Figure 8-1. Top Assembly

Figure 8-2. Outer Structure Assembly

Figure 8-3. Subchassis Assembly

Printed Circuit Board Assembly, dwg 102237

Printed Circuit Board Schematic Diagram, dwg 102238 (9 sheets)

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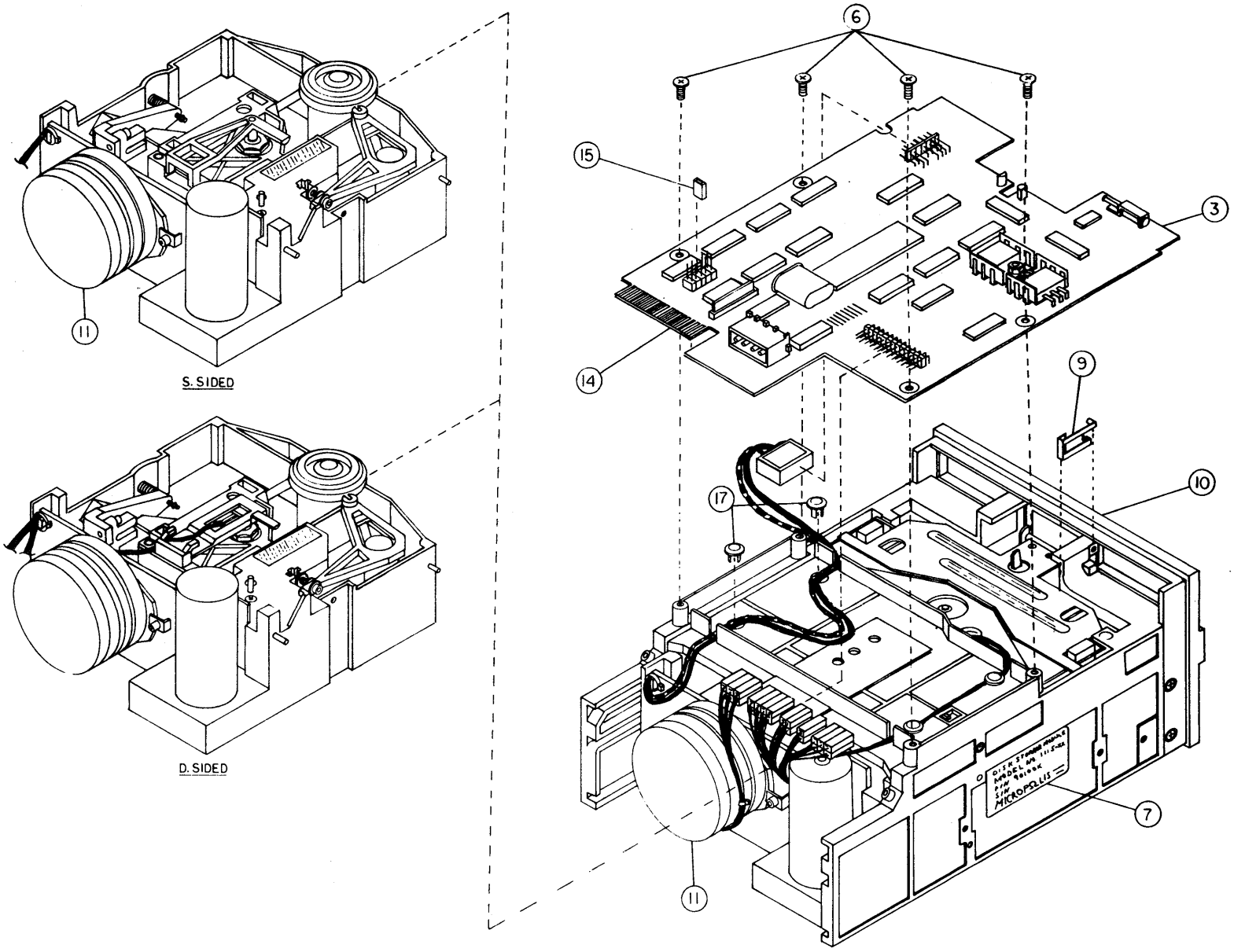

Figure 8-1. Top Assembly

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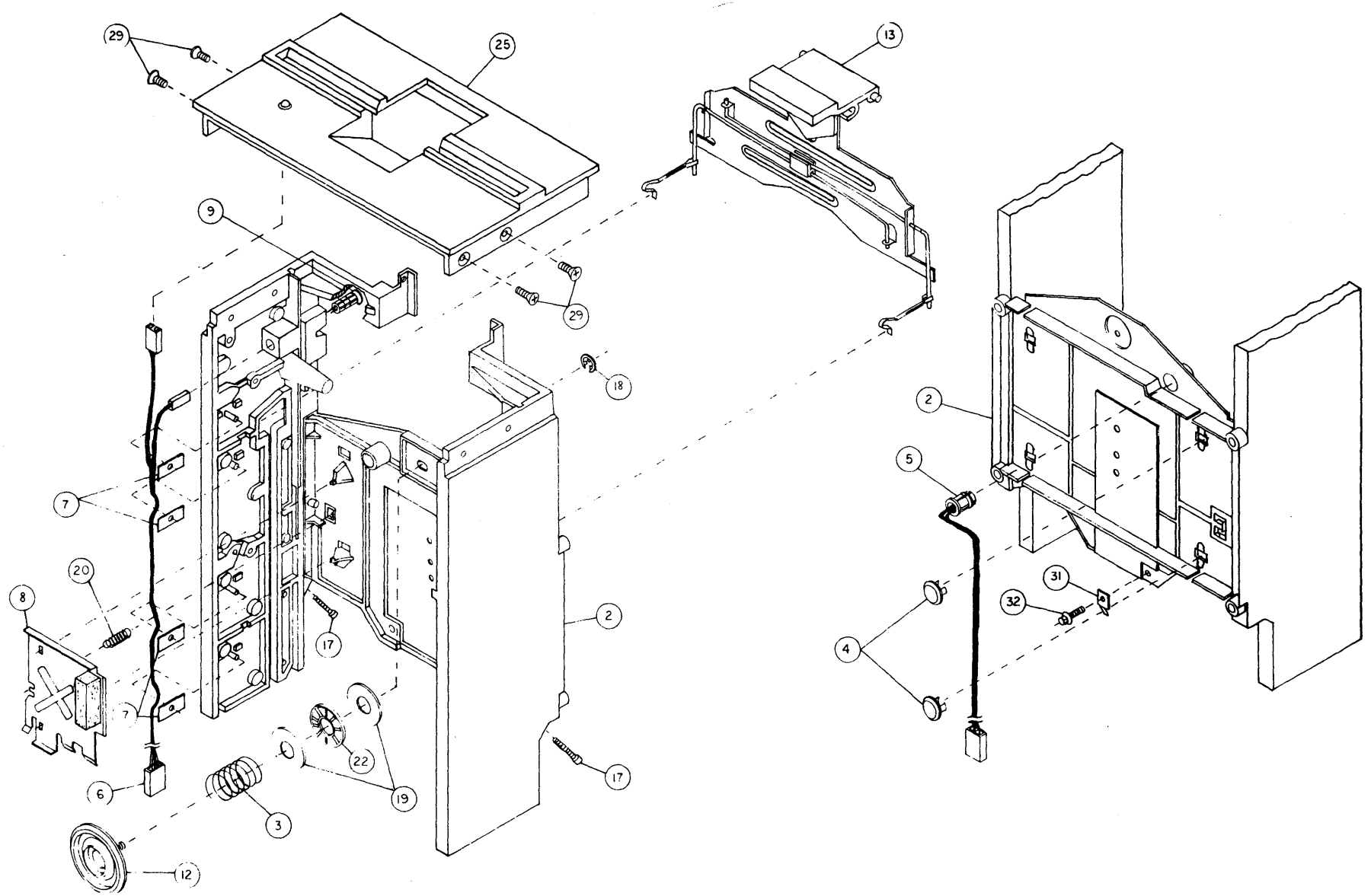

Figure 8-2. Outer Structure Assembly

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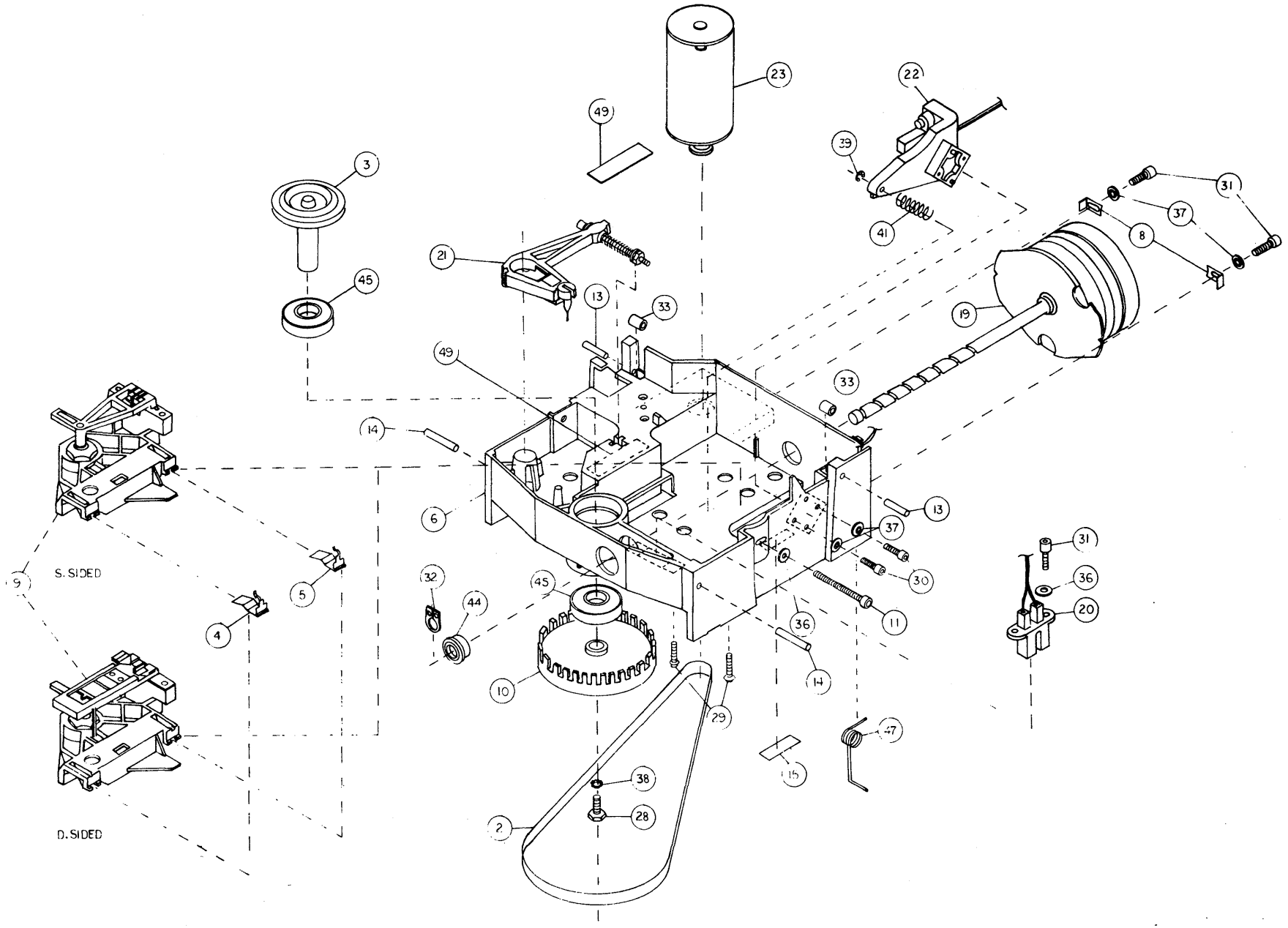

Figure 8-3. Subchassis Assembly

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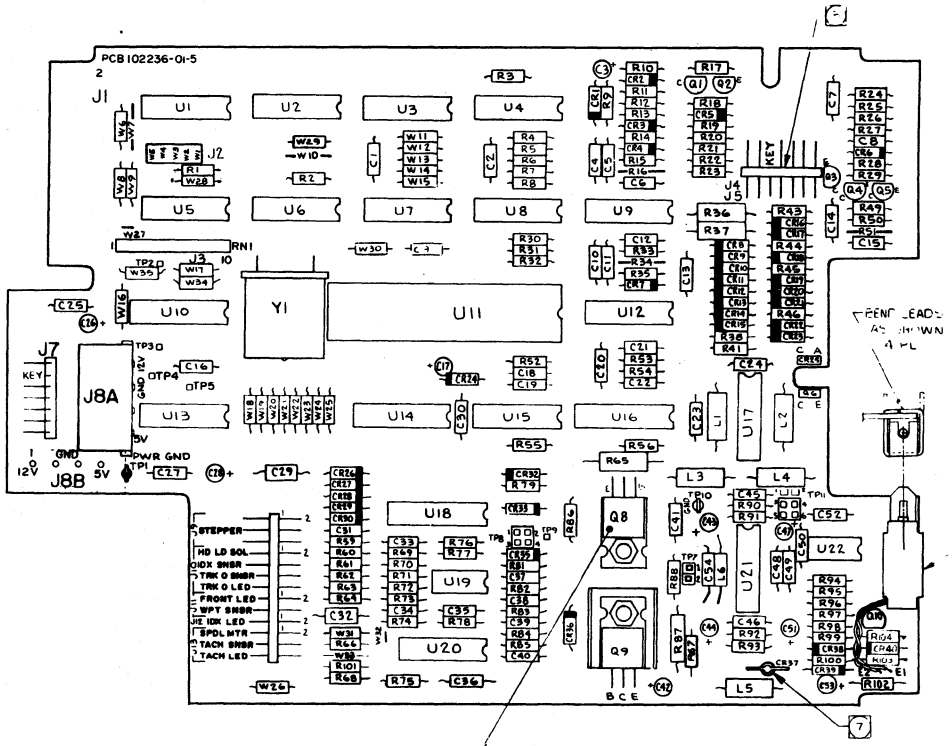
	DESCRIPTION	DATE	APPROVED
B3	PRE-PRODUCTION RELEASE PER ERN 2207	6/3/82	
C1	NOT USED, PROTO ONLY	8/13/82	
D1	REVISED PER EN 2344	8/19/82	
D2	REVISED PER ECN 2396	9/9/82	
D3	ECN 2509	11/7/82	
D4	ECN 2579	12/1/82	
E1	ECN 2584	12/22/82	



9. LEAD LENGTH ON CIRCUIT SIDE SHALL BE .090 MAX.

8. REMOVE PIN 3 ON J4 AND J6.

7. CR37 MAY NOT BE FLOW SOLDERED.

6. TORQUE HEX NUT TO 6 INCH POUNDS.

5. ITEM NUMBERS ON DRAWING DO NOT RELATE TO LIST OF MATERIALS.

4. THE FOLLOWING REFERENCE DESIGNATORS ARE ETCHED CONDUCTORS WHICH MAY BE CUT AND SUBSTITUTED WITH COMPONENTS AS REQUIRED: W7, R16, R34, R39, R40 AND R51.

3. ▭ BAND INDICATES CATHODE END OF DIODE.

2. INTEGRAL PARTS LIST IS FOR REFERENCE ONLY.

1. FOR LIST OF MATERIALS SEE LM102237.

ITEM NO	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	ZONE
15						
14			650-0003-6	THERMAL COMPOUND		
13			340-0125-5	TRANSISTOR	Q8	
12			340-0110-7	TRANSISTOR	Q9	
11			650-0005-1	HEATSINK		
10			102258	DOOR LOCK SOLENOID		
9			710-0602-7	NUT, HEX		
8			700-0605-1	SCREW		
7			680-0702-0	CONNECTOR	J5	
6			680-0703-8	CONNECTOR	J4	
5			680-2801-8	CONNECTOR	J9, J10, J11, J12, J13	
4			680-0701-2	CONNECTOR	J7	
3			680-0401-9	CONNECTOR	J8B	
2			680-0405-0	CONNECTOR	J8A	
1			102236	PROCESS BOARD		

REF PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ±	CONTRACT NO
MATERIAL SEE NOTES	DR BY AVAGE 11/5/82
FINISH	CHK BY ERIC HEGTEL 11/15/82
	APPROVED BY

MICROPOLIS

PCB ASSEMBLY, 1115

D F/D 102237 E1

SIZE 2/1

102290-01-2 1100

102237 E1

TABLE I

PART NO.	REF DESIGNATION
100-0000-8	W6,8,9,10,11,12,13,14,15, 16,17,18,19,20,21,22,23, 24,25,26,28,29,30,31
100-0750-8	R98
100-1000-7	R64
100-1001-5	R17,25,27,28,29,82 83,86,101
100-1003-1	R59,63,84
100-1200-3	R100
100-1201-1	R81
100-1202-9	R14,33,38,42,43,44, 56,70
100-1500-6	R1,15,35,62,90,91
100-1501-4	R20,21,22,24
100-1800-0	R18,61,68
100-2200-2	R92,R93
100-2201-0	R2,7,8,9,30,31,49, 67,76,77,95,96
100-2202-8	R4,5,41,79
100-2702-7	R45,46,66,99
100-3300-9	R19,26,52,55,103
100-6800-5	R88
100-4700-9	R23,53,94,97
100-4702-5	R3,85,104
100-5600-0	R50
101-0010-5	R87
101-0180-6	R102
101-0330-7	R65
101-2200-0	R36,37
105-1003-0	R69,71,75
105-1962-7	R10,13
105-2742-2	R60,72,73
105-3651-4	R6, R32
105-6191-8	R11,R12
163-3304-9	C17,26,28,42,44,51

TABLE I (CONT)

PART NO.	REF DESIGNATION
163-3305-6	C3
177-0003-0	C53
163-4703-1	C43,47
169-2705-5	C23
169-1002-8	C1,4,8,11,12,14,15,16, 21,24,25,27,30,33,38, 49,52
170-1000-0	C7,22
170-3300-2	C50
170-4700-2	C20,C31
170-8200-9	C54
170-7500-3	C18,C19
171-1501-5	C45
171-2202-9	C37,39,40,46,48
171-4701-8	C35
171-4702-6	C5,6,10,13,34,41
171-4703-2	C29,32,36
190-0240-1	L3,4
190-1000-8	L1,2,5
190-4700-0	L6
200-4446-7	CR1,2,3,4,6,7,8,9,10, 11,12,13,14,15,16,17,18, 19,20,21,22,23,35 39,40
210-5223-8	CR5
210-5250-1	CR33
220-4002-6	CR26,27,28,29,30,32, 36,38
240-0060-6	CR37
240-0071-3	CR25
250-0005-0	CR24
300-4400-2	Q2
300-4402-8	Q1,3,4,5,10
330-0701-4	Q6
340-0110-7	Q9
340-0125-5	Q8
400-0014-3	U1,4,5
400-0026-7	U8
400-0074-7	U3,12,13
400-0086-1	U15

TABLE I (CONT)

PART NO.	REF DESIGNATION
400-0174-5	U14
401-0016-6	U2,7
401-0017-4	U6
406-0437-3	U18
406-0452-2	U19
407-0004-9	U16
408-0008-8	U10
410-0311-2	U22
410-0339-3	U20
410-0556-2	U9
410-0592-7	U17,21
430-0007-4	U11
500-2000-7	Y1
680-0206-2	TP7
680-0401-9	J8B
680-0405-0	J8A
680-0406-8	TP8,11
680-0701-2	J7
680-0702-0	J5
680-0703-8	J4
680-1008-1	J3
680-1009-9	J2
680-2601-2	J9
684-0008-4	TP1,10
102258	DOOR LOCK ASSY.

TABLE II

LAST USED	NOT USED	DELETED
C54		
CR39	CR31,34 32	
J13	J6	
L6		
Q10	Q7	
R104	R47,48,30, 58,57,89,80	
TP11		
U22		
W35		
Y1		
RN1		

REFERENCE DOCUMENTS

MASTER LAYOUT 102235
PROCESS BOARD 102236
P.C.B. ASSEMBLY 102237

SEE SHEET 2 FOR NOTES.

NOTE UNLESS OTHERWISE SPECIFIED

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B3	PRE-PRODUCTION RELEASE PER ERN 2207	6/1/82	
	C1	NOT USED	8/5/82	
	D1	~~PRE PRODUCTION RELEASE~~ PER EN 2344	8/19/82	
	D2	REVISE PER EN# 2396 EK	9/9/82	
	D3	ECN #2509	11/17/82	
	D4	ECN #2579 JS	12/17/82	
	E1	ECN #2584 JS	12/22/82	

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION			ZONE
PARTS LIST						

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± .XX ± .XXX ± DECIMALS ± .X ± .XX ± ANGLES ±

CONTRACT NO.

DR BY John Savage 5/10/82
CHK BY [illegible] 5/10/82
APPROVED BY

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

MICROPOLIS

SCHEMATIC, 1115

SIZE	PROD CODE	DWG NO.	REV.
D	F/D	102238	E1

SCALE

SHEET 1 OF 9

102238 E1

TABLE III

ASSEMBLY 102237 VERSION	VERSION CHARACTERISTIC	C10, C11, J5, Q5, CR2, CR7, CR9, CR12, CR17 R11, R20, R29, R33, R37, R43	CR 30	U19			JUMPER CONFIGURATION	J7 J8A OR J8B	CR38,39,40 R67,102,103,104 Q10, C53	R88	C54	L6	R54	
-51-8	96/100 TPI, MFM SINGLE HD, NO OPTIONS						W6, W11, W16, W26	J 8A		680	820PF	470 UH	11K	
-52-6	96/100 TPI, MFM DUAL HD, NO OPTIONS	IN					W6, W11, W16, W26	J8A		680	820 PF	470UH	11K	
-53-4	96/100 TPI, MFM SINGLE HD, HD SOL		IN	IN			W6, W11, W16, W26	J8 A		680	820 PF	470 UH	11K	
-54-2	96/100 TPI, MFM SINGLE HD, D. LOCK			IN			W6, W10, W11, W16, W26	J8A	IN	680	820PF	470 UH	11K	
-55-9	96/100 TPI, MFM DUAL HD, D LOCK	IN		IN			W6, W10, W11, W16, W26	J8A	IN	680	820PF	470 UH	11K	

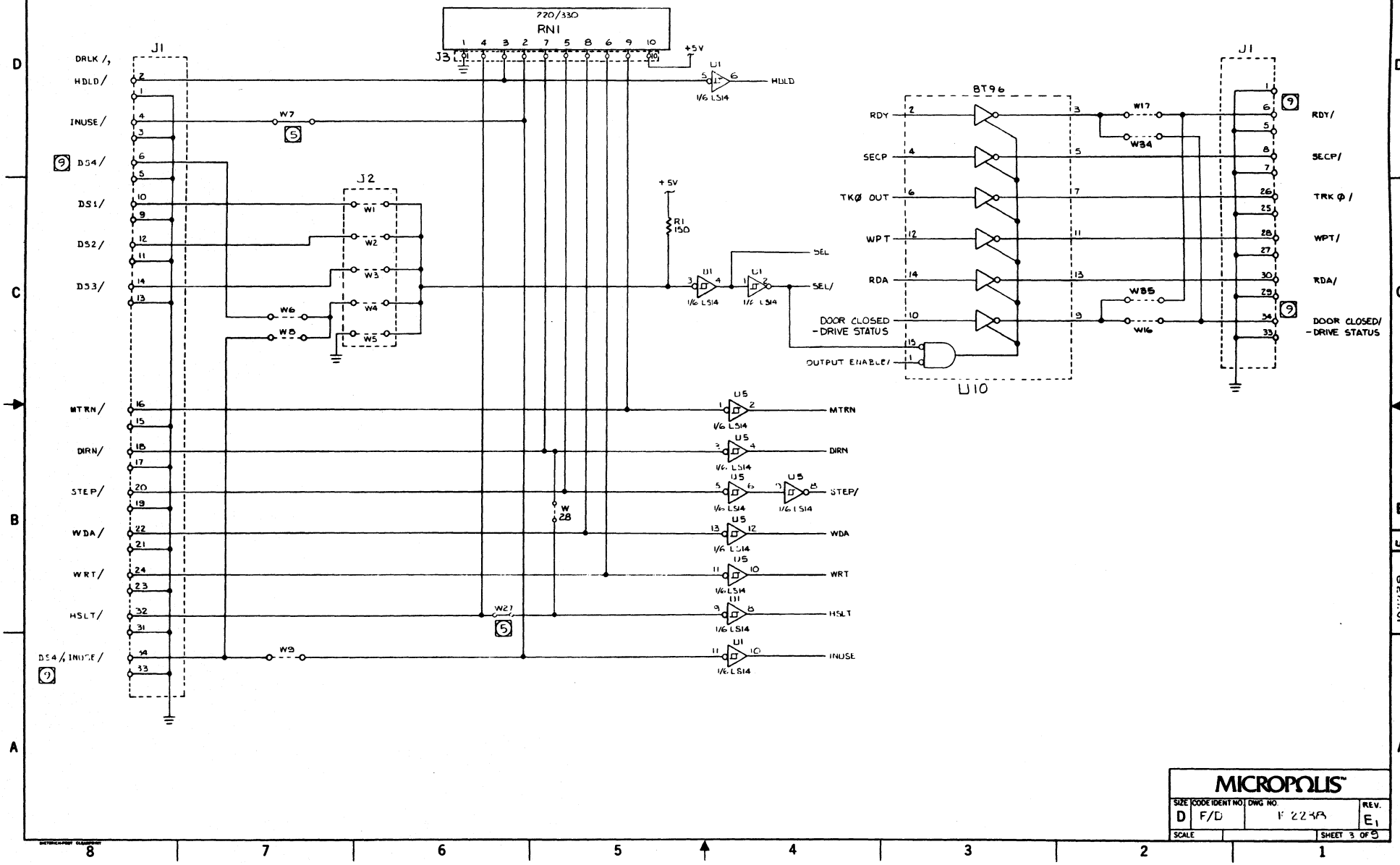
9. CONNECTORS MAY BE USED FOR INPUT OR OUTPUT.
8. FOR LAST USED, NOT USED OR DELETED, SEE TABLE II.
7. FOR LIST OF PART NUMBERS, SEE TABLE I.
6. FOR COMPONENTS AFFECTED BY VERSION, SEE TABLE III.
5. NOTED COMPONENTS ARE ETCHED CONDUCTORS WHICH MAY BE REPLACED AS REQUIRED.
4. NOTED COMPONENTS ARE NOT USED IN STANDARD VERSIONS.
3. ALL DIODES ARE PART NUMBER 200-4446-7.
2. CAPACITOR VALUES ARE IN MICROFARADS.
1. RESISTOR VALUES ARE IN OHMS AND WITHIN ±5%.

NOTES: UNLESS OTHERWISE SPECIFIED.

MICROPOLIS

SIZE	PROD. CODE	DWG NO.	REV
D	F/D	102238	E1
SCALE			SHEET 2 OF 9

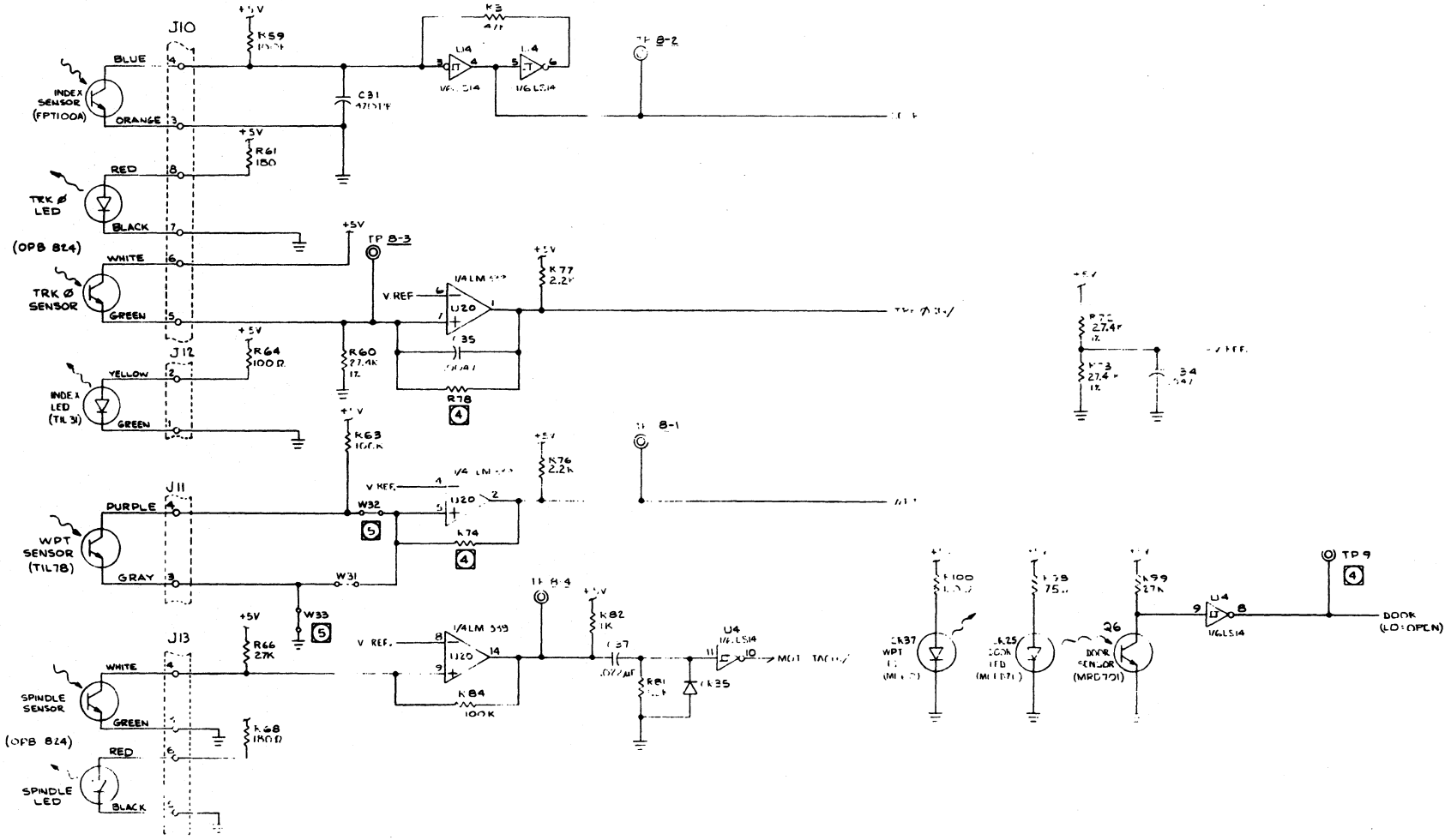
102238 E1



MICROPOLIS

SIZE	CODE IDENT NO.	DWG NO.	REV.
D	F/D	1122XA	E1
SCALE			SHEET 3 OF 9

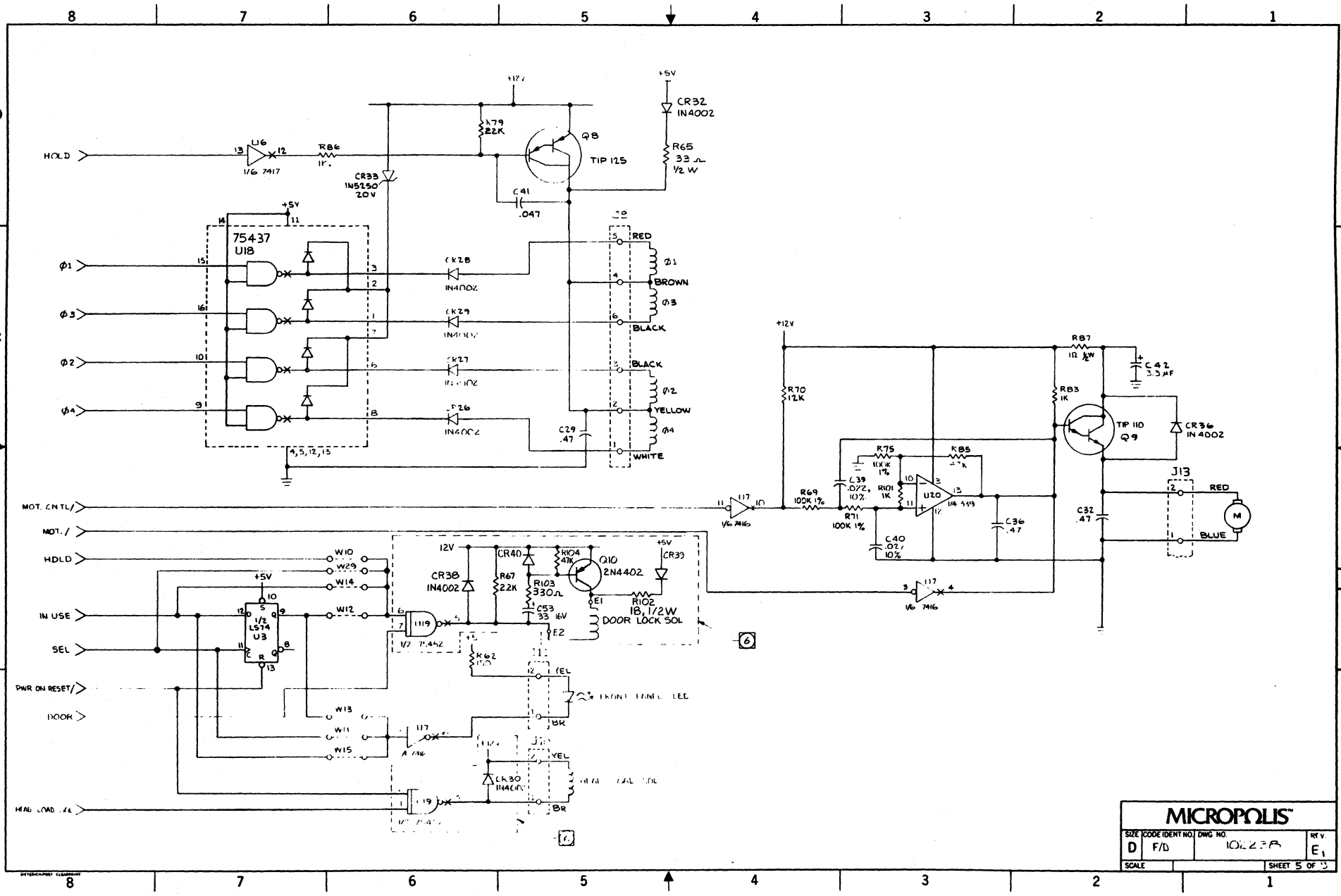
1122XA E1



MICROPOLIS

SIZE	PROD. CODE	DWG NO.	REV
D	[illegible]	102238	E1
SCALE			SHEET 1 OF 2

102238 E1

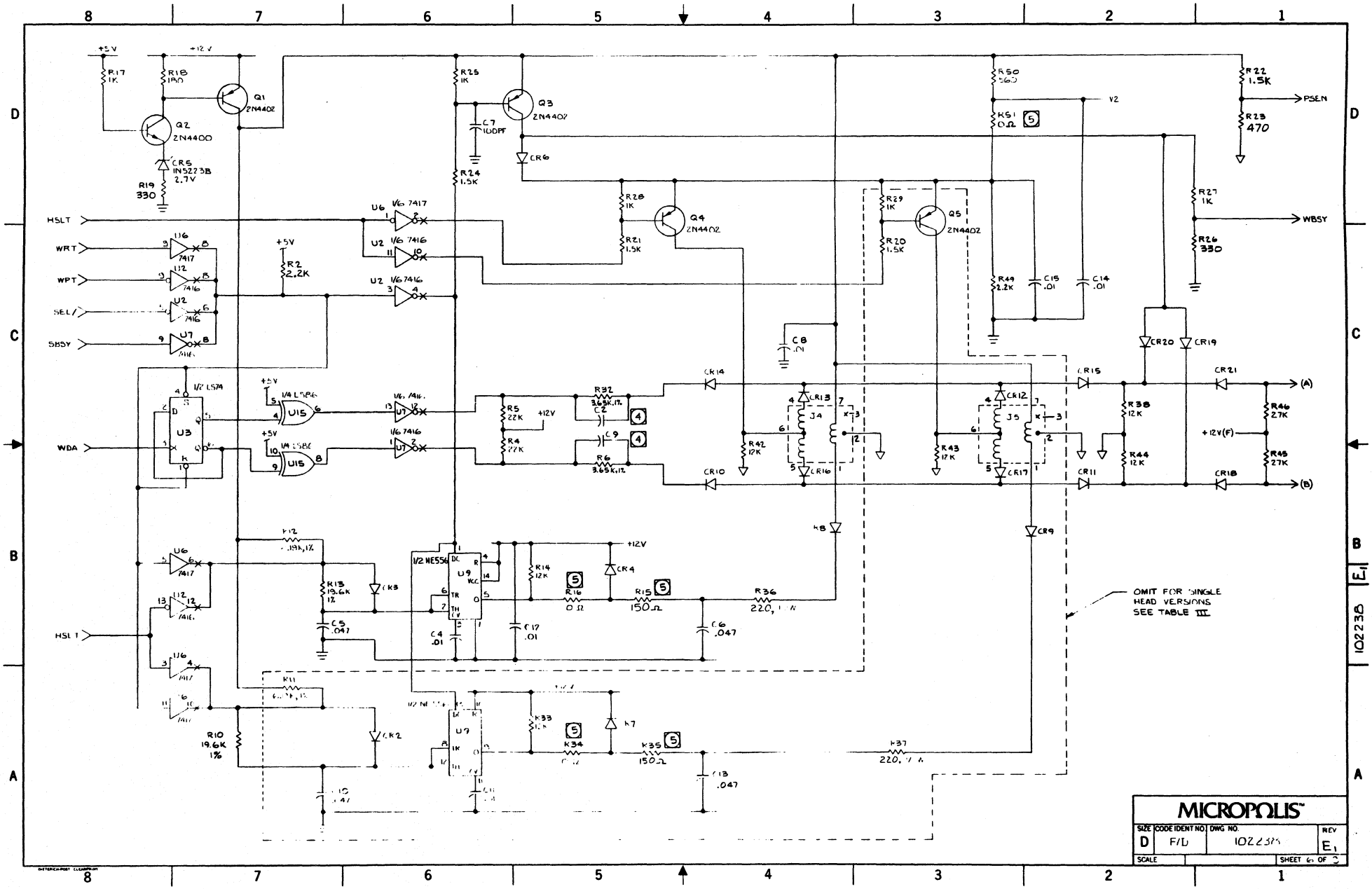


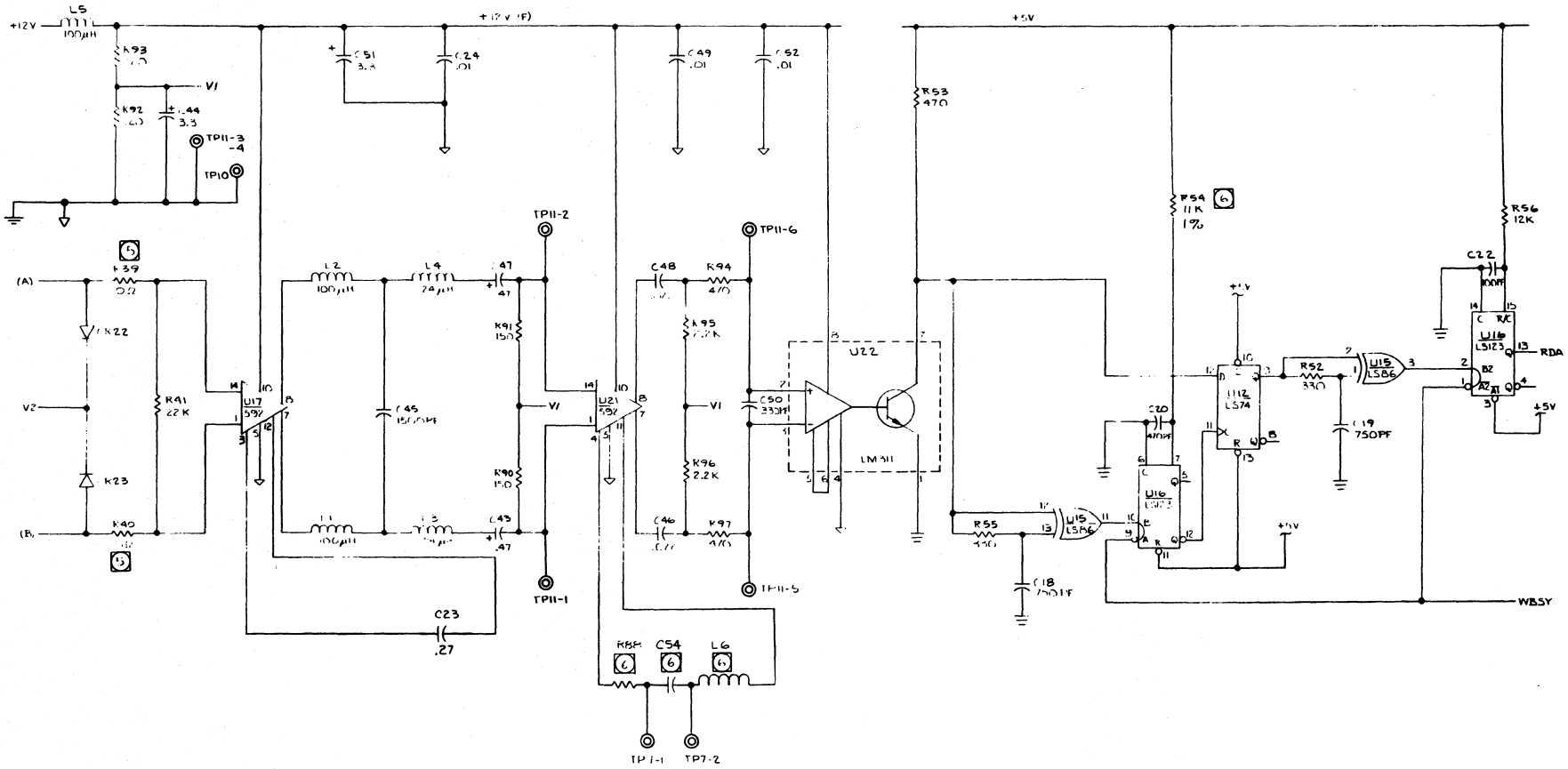
MICROPOLIS

SIZE	CODE IDENT NO.	DWG NO.	REV.
D	F/D	102238	E1

SCALE

SHEET 5 OF 13


+5V
+12V
R17 1K
R18 180
Q1 2N4402
Q2 2N4400
CR5 IN5223B 2.7V
R19 330
R25 1K
Q3 2N4402
C7 100PF
CR6
R24 1.5K
R28 1K
Q4 2N4402
R21 1.5K
R29 1K
Q5 2N4402
R20 1.5K
R50 56Ω
KS1 0Ω
V2
R22 1.5K
PSEN
R23 470
R27 1K
WBSY
R26 330
R49 2.2K
C15 .01
C14 .01
HSLT
WRT
WPT
SEL/
SBSY
U6 1/6 7417
U2 1/6 7416
R2 2.2K
C8 .01
CR20
CR19
CR14
CR15
CR21
(A)
WDA
U3
U15
R5 22K
R4 22K
R32 3.65K,1%
C2
C9
R6 3.65K,1%
CR13
CR16
CR12
CR17
R42 12K
R43 12K
R38 12K
R44 12K
R46 2.7K
R45 2.7K
+12V(F)
CR10
CR11
CR18
(B)
CR8
CR9
R12 19.1K,1%
R13 19.6K 1%
CR3
U9 1/2 NE556
R14 12K
R16 0Ω
CR4
R15 150Ω
R36 220Ω, 1 W
C5 .047
C4 .01
C17 .01
C6 .047
OMIT FOR SINGLE HEAD VERSIONS SEE TABLE III
R10 19.6K 1%
CR2
R33 1K
CR7
R34
R35 150Ω
R37 220Ω, 1 W
C13 .047
MICROPOLIS
SIZE D
CODE IDENT NO. F/D
DWG NO. 102238
REV E1
SCALE
SHEET 6 OF 7
102238 E1

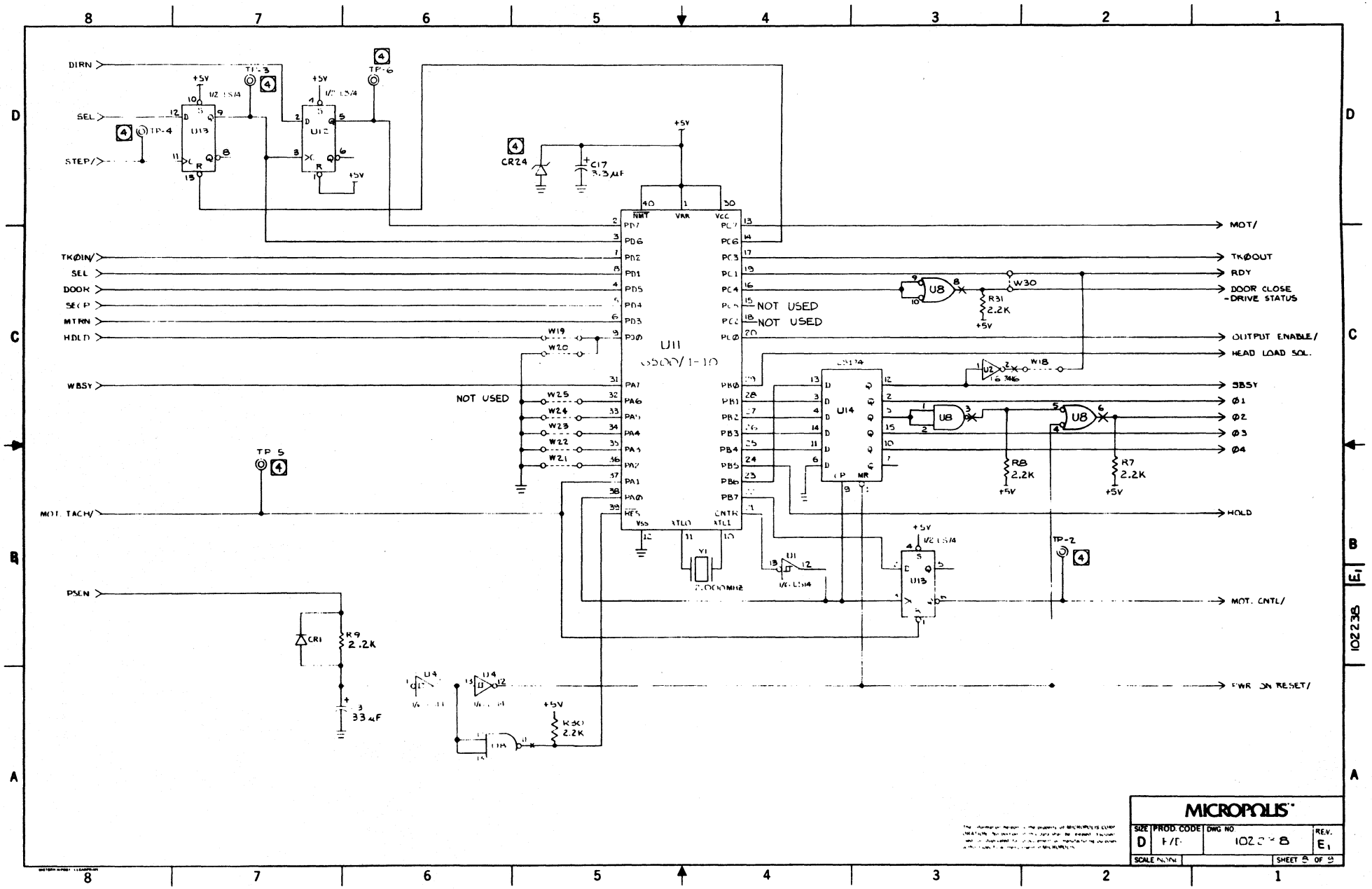


MICROPOLIS

SIZE	PROD. CODE	DWG NO.	REV
D	F/L	102238	E1

SCALE N. N.L. SHEET 1 OF 2

102238 E1



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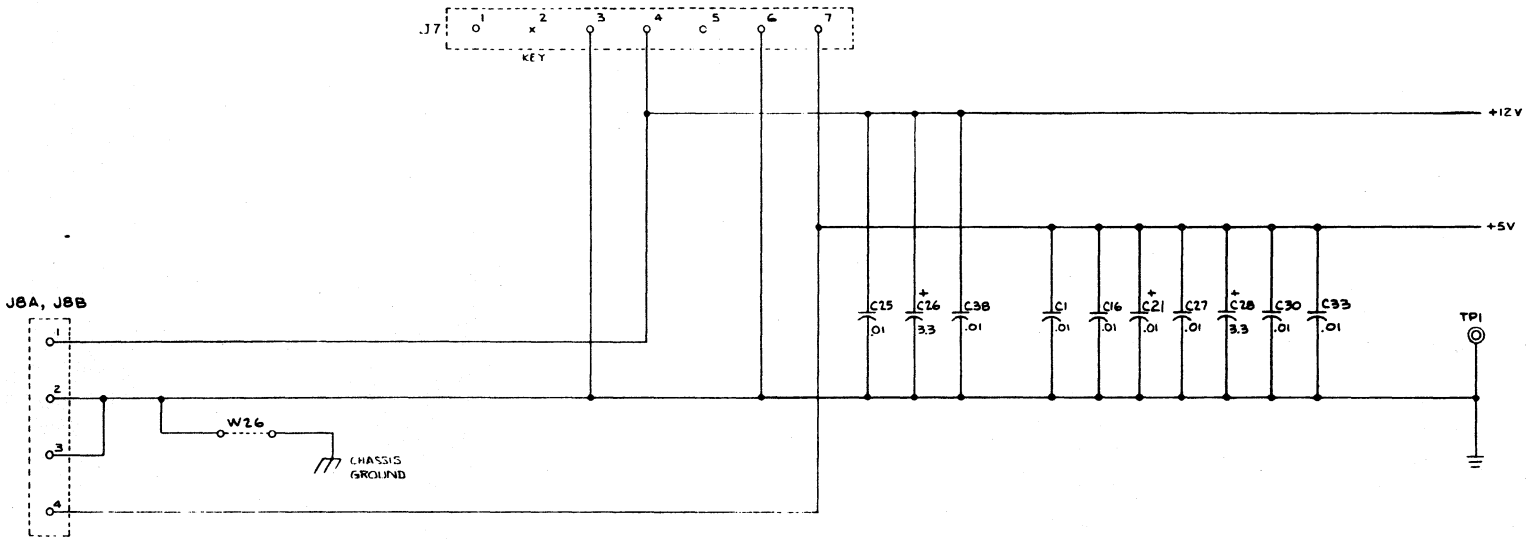
SIZE	PROD. CODE	DWG NO	REV.
D	1/1-	102238	E1

SCALE NONE | SHEET 5 OF 9

102238 E1



MICROPOLIS

SIZE	PROD. CODE	DWG NO.	REV.
D	F/D	102238	E1

SCALE N. T. S. | SHEET 3 OF 5

102238 E1

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