PRODUCT DESCRIPTION

Micropolis 1550 Series

5 1/4-Inch Rigid Disk Drive

MICROPOLIS

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DOCUMENT No. 104004 REV A

PREFACE

This Product Description, intended for use by engineers, designers, and planners, describes the typical characteristics of the Micropolis 1550 Series of 5 1/4-inch Disk Drives. The information contained in this Product Description reflects current Micropolis design and experience, and is subject to change without notice.

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SECTION 1. DESCRIPTION

Micropolis 1550 Series high-performance, 5 1/4-inch Winchester Disk Drives provide OEMs with high-speed, high-capacity, random-access storage. They are fully compatible with the Serial mode of the Enhanced Small Device Interface (ESDI) standard and are designed to meet the needs of diverse applications environments. The 1550 Series is available in the following standard configurations:

Model Number	Data Heads per Drive	Capacity in MBytes * (Unformatted)
1558-15	15	382.3
1558-14	14	356.8
1557-13	13	331.3
1557-12	12	305.8
1556-11	11	280.3
1556-10	10	254.9
1555-09	9	229.4
1555-08	8	203.9
1554-07	7	178.4

* 1 MByte = 1,000,000 bytes

1.1 FEATURES OF THE 1550 SERIES

- High-performance positioner delivers 18-millisecond average seek time for fast data access and high system throughput.
- Up to 382.5 MBytes (unformatted) per drive, and up to 2.68 GBytes per controller.
- MTBF 30,000 hours.
- Hard or soft sectoring permits use with all ESDI controllers.
- Industry-standard 5 1/4-inch form-factor and mounting provisions ensure easy incorporation into current system packages.
- Rugged dual-chassis construction suspends the Head/Disk Assembly (HDA) on shock/vibration isolators to provide exceptional protection during transportation, installation, and operation.
- Balanced rotary positioner provides immunity to shock and vibration, and permits the drive to be mounted in any orientation.
- Positive media protection upon spin down is provided by retracting and locking the positioner in a data-free landing zone. A dynamic brake stops the motor quickly.
- Board-swap design results in an MTTR of less than 15 minutes.
- Microprocessor-based, adaptive electronics eliminates adjustment or periodic maintenance and improves overall reliability.

1.2 CHARACTERISTICS

General Performance Specifications

Seek Time (including settling time)

Track-to-Track	4 msec
Average	18 msec
One-Third Stroke (maximum)	19 msec
Maximum	40 msec

Rotational Latency

Average	8.33 msec
Nominal Maximum	16.67 msec

Start Time (to Drive Ready)	12 seconds typical 20 seconds maximum
Stop Time	20 seconds maximum

General Functional Specifications

Cylinders	1224
Interface encoding method	NRZ
Internal encoding method	2,7 RLL
Spindle speed (rpm)	3600
Speed variation (%)	±0.5
Transfer rate (MBits/sec)	10.00

General Physical Specifications

Drive:	Height	3.25 in	(82.6 mm)
	Width	5.75 in	(146 mm)
	Depth	8.00 in	(203 mm)
Bezel:	Height	3.38 in	(85.7 mm)
	Width	5.88 in	(149 mm)
	Depth	0.185 in	(4.7 mm)
Drive Weight (1558-15, typical)		7.5 lbs	(3.4 kg) nominal

Capacity

Unformatted

	Model Number								
	1554-07	1555-08	1555-09	1556-10	1556-11	1557-12	1557-13	1558-14	1558-15
MBytes/Unit	178.4	203.9	229.4	254.9	280.3	305.8	331.3	356.8	382.3
Data Heads	7	8	9	10	11	12	13	14	15
Cylinders	1224								
Bytes/Track	20,832								
MBytes/Surface	25.49								

Formatted (1024-Byte Format) *

	Model Number								
	1554-07	1555-08	1555-09	1556-10	1556-11	1557-12	1557-13	1558-14	1558-15
MBytes/Unit	166.6	190.4	214.2	238.1	261.9	285.7	309.5	333.3	357.1
Sectors/Track	19								
Bytes/Track	19,456								
MBytes/Surface	23.81								

Formatted (512-byte format) *

	Model Number								
	1554-07	1555-08	1555-09	1556-10	1556-11	1557-12	1557-13	1558-14	1558-15
MBytes/Unit	157.9	180.4	203.0	225.6	248.1	270.7	293.2	315.8	338.4
Sectors/Track	36								
Bytes/Track	18,432								
MBytes/Surface	22.56								

* See Section 5 for format parameters.

Vibration

Operating (the drive can be operated and subjected to vibration up to the following levels, and will meet error specifications shown on page 1-5)

5 - 40 Hz	0.006 inches, peak-peak
40-300 Hz	0.5 G peak

Non-Operating (the drive will sustain no damage if subjected to vibration up to the following levels)

Packaged (in original Micropolis shipping container)

5 - 10 Hz	0.2 inches, peak-peak
10 - 44 Hz	1 G peak
44 - 98 Hz	0.01 inches, peak-peak
98-300 Hz	5 G peak

Unpackaged

5 - 31 Hz	0.02 inches, peak-peak
31 - 69 Hz	1 G peak
69 - 98 Hz	0.004 inches, peak-peak
98-300 Hz	2 G peak

Shock

Operating (the drive can be operated and subjected to shock up to the following levels, and will meet error specifications shown on page 1-5)

1/2 Sinusoidal	5 msec, 3 G peak
	11 msec, 2 G peak
	20 msec, 1 G peak

Non-Operating (the drive will sustain no damage if subjected to shock up to the following levels)

Packaged (in original Micropolis shipping container)

Free-fall drop	36 inches
1/2 Sinusoidal	20 msec, 50 G max

Unpackaged

Free-fall drop	0.75 inches
Topple test	1.5 inches
1/2 Sinusoidal	5 msec, 40 G max
	11 msec, 20 G max
	20 msec, 15 G max
	50 msec, 15 G max
	100 msec, 20 G max

Environmental Requirements

	Operating	Storage
Ambient Temperature	10°C to 50°C (50°F to 122°F)	-40°C to 65°C (-40°F to 149°F)
Relative Humidity	10% to 90% non-condensing	10% to 90% non-condensing
	26.7°C (80°F) maximum wet bulb non-condensing	26.7°C (80°F) maximum wet bulb non-condensing
Altitude	-200 ft to 10,000 ft	-1000 ft to 50,000 ft
Thermal Shock	2.0°C/5 Minutes (3.6°F/5 Minutes)	24.0°C/Hour * (43.2°F/Hour)

* This gradient should not be exceeded when moving the drive from storage to operation.

Power Dissipation (typical drive, nominal voltage)

Stand-by	29 Watts; 98.9 BTU/hr
Positioning **	35 Watts; 119.4 BTU/hr

** This value is for 1/3-stroke seeks with an 8-millisecond idle period between seeks to simulate a typical system environment.

Acoustic Noise

Less than 51 dBA (sound pressure)

Reliability

Soft Read Errors	$\leq$ 10 in 10^{11} bits read
Hard Read Errors	$\leq$ 10 in 10^{13} bits read
Seek Errors	$\leq$ 10 in 10^{7} seeks
Unit MTBF	30,000 Power-On Hours

Maintainability (HDA not included)

MTTR	Less than 15 minutes

1.3 MAJOR COMPONENTS

The disk drive consists of a mechanical assembly and an electronics package. For a detailed functional theory of operation, see the 1550 Series Technical Manual, Micropolis No. 104789.

1.3.1 Mechanical Assembly

The mechanical assembly consists of a sealed Head/Disk Assembly (HDA) and an outer Frame.

a. Head/Disk Assembly

The Head/Disk Assembly (HDA) consists of a die-cast structure that contains virtually all of the drive's mechanical components. Two die-cast members create a sealed clean area. Components included in the clean area are the read/write heads, the magnetic disks, the head preamplifier, and the rotary positioner. Electrical connection between the mechanics in the clean area and the electronic circuit boards is made with flexible circuits.

Air circulates through the clean area by disk rotation-induced flow. The air is filtered by a 0.3-micron absolute filter. The sealed area breathes to the outside via a similar filter.

- Disk/Spindle Assembly

The magnetic disks are mounted on the spindle assembly, which incorporates a three-phase brushless DC motor, commutated by Hall-effect devices. Each end of the spindle assembly is supported by the casting.

- Head Assembly

The drives have one servo head and up to 15 data heads. The head assembly flies over the disk surface on an "air bearing" created by the rotation of the disk. The heads rest on the disk surface (i.e., the landing zone) when the disk is not rotating.

- Positioner Assembly

The positioner is a balanced rotary motor mechanism. Each end of the positioner shaft is supported by the casting. The servo head and data heads are attached to the head-arm assemblies mounted to the pivot housing. The motor torque rotates the positioner about its axis of rotation. Rotation is constrained to keep the heads over the safe operating area of the disk by means of limit stops.

Position reference is made to tracks recorded on the disk surface nearest the baseplate. Position information is recorded on these tracks in a "Modified Dibit" format.

An area of the disk (not used for data storage) is reserved for landing the heads. When power is removed from the drive, the positioner assembly is automatically retracted to that landing zone, and a latch is activated to prevent the positioner from leaving the landing zone. Thus, no operator intervention is necessary when shipping a drive or when shipping the equipment in which a drive is installed.

- Recording Media

  The recording media is a 130-millimeter (5 1/4-inch) diameter aluminum disk substrate covered with a thin coating of magnetic media. The disk surface permits head-to-disk contact without damage.

- Braking

  The heads contact the disk surface when the disks are not spinning and during start and stop cycles. To minimize head and disk wear, dynamic braking is used to bring the spindle to a quick stop.

b. Frame (Outer Chassis)

The HDA is suspended on shock mounts within an outer frame mounts. This method of suspension isolates the HDA from mounting-related distortion or stress, or shock and vibration.

1.3.2 Electronic Components

The electronic components for the 1550 Series are mounted on three printed circuit boards:

a. Device Electronics board.

b. Hybrid Electronics board (plugs into the Device Electronics board).

c. Preamplifier board (inside the HDA).

The electronic circuitry provides overall control and data functions for the drive. The microprocessor-based logic controls power-up and power-down sequencing and velocity profile generation. The servo circuits ensure positioner speed and accuracy. Interface drivers and receivers provide for transmission and reception of signals across the interface, while the data read/write circuits provide for data flow onto and off the disks.

SECTION 2. INTERFACE

2.1 INTERFACE AND POWER CONNECTOR PIN ASSIGNMENTS

The 1550 Series is pin- and function-compatible with the Serial mode of the Enhanced Small Device Interface (ESDI) for 5 1/4-inch Winchester disk drives. In the Serial mode, interface signals (control, data, and status) are transmitted serially via handshaking request/acknowledge signals.

Electrical interface between the drive and the host system is accomplished via five connectors: Control Signal Connector J1 (see Table 2-1) and Data Transfer Connector J2 (see Table 2-2), Power Connector J3 (see Table 2-3), and optional Ground Connectors J4 and J5. Refer to Figure 3-1 for the locations of the five connectors.

TABLE 2-1. CONTROL SIGNAL CONNECTOR J1 PIN ASSIGNMENTS

J1 Connector Pin Signal	Ground	Signal Name	Source
2	1	-HEAD SELECT 2^3	Controller
4	3	-HEAD SELECT 2^2	Controller
6	5	-WRITE GATE	Controller
8	7	-CONFIGURATION/STATUS DATA	Drive
10	9	-TRANSFER ACKNOWLEDGE	Drive
12	11	-ATTENTION	Drive
14	13	-HEAD SELECT 2^0	Controller
16	15	{ -SECTOR -ADDRESS MARK FOUND }	Drive
18	17	-HEAD SELECT 2^1	Controller
20	19	-INDEX	Drive
22	21	-READY	Drive
24	23	-TRANSFER REQUEST	Controller
26	25	-DRIVE SELECT 1	Controller
28	27	-DRIVE SELECT 2	Controller
30	29	-DRIVE SELECT 3	Controller
32	31	-READ GATE	Controller
34	33	-COMMAND DATA	Controller

Recommended Cable: 3M Scotchflex 3365/34

Mating Connector: AMP 88373-3 (key slot between pins 4 and 6)

TABLE 2-2. DATA TRANSFER CONNECTOR J2 PIN ASSIGNMENTS

J2 Connector Pin Signal	Ground	Signal Name	Source
1	-	-DRIVE SELECTED	Drive
2	-	{ -SECTOR / -ADDRESS MARK FOUND }	Drive
3	-	-COMMAND COMPLETE	Drive
4	-	-ADDRESS MARK ENABLE	Controller
5	6	(Reserved)	Drive
7	-	+WRITE CLOCK	Controller
8	-	-WRITE CLOCK	
9	-	(Reserved)	Drive
10	12	+READ/REFERENCE CLOCK	Drive
11		-READ/REFERENCE CLOCK	
13	15	+NRZ WRITE DATA	Controller
14	16	-NRZ WRITE DATA	
17	19	+NRZ READ DATA	Drive
18		-NRZ READ DATA	
20	-	-INDEX	Drive

Recommended Cable: 3M Scotchflex 3365/20

Mating Connector: AMP 88373-6 (key slot between pins 4 and 6)

Power is supplied to the drive via AMP MATE-N-LOK Connector J3; refer to Section 4 for power requirements. Voltages in Table 2-3 are ±5%, measured at the drive's power connector. Suggested wire size is 18 AWG (minimum) for all pins. Recommended mating connector is AMP 1-480424-0; recommended pins are AMP 350078-4.

TABLE 2-3. DC POWER CONNECTOR J3 PIN ASSIGNMENTS

Pin	Voltage
1	+12 VDC
2	+12 Return
3	+ 5 Return
4	+ 5 VDC

2.2 INTERFACE ELECTRICAL CHARACTERISTICS

Figure 2-1 summarizes the electrical characteristics of the signals at Control Signal Connector J1. These signals control the drive and transfer drive status to the host controller. The signals are low-true at the interface, high-true into drivers and out of receivers, and have the following logic levels:

True = 0.0 VDC to 0.4 VDC @ I = -48 milliamps (maximum)
False = 2.5 VDC to 5.25 VDC @ I = +250 microamps (open collector)

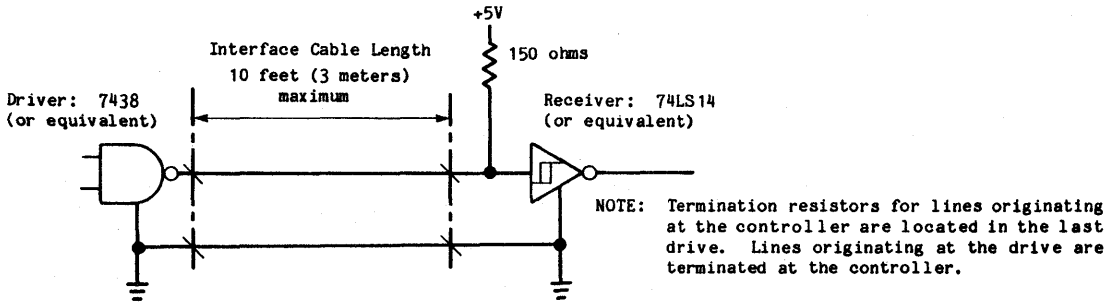


Figure 2-1. Control Signal Driver/Receiver Combination

All interface data transfer signals are differential in nature. Figure 2-2 summarizes the electrical characteristics of those differential signals at Data Transfer Connector J2 (one TTL control signal and four TTL status signals are also provided at Connector J2). The signals are high true into drivers and out of receivers and have the following levels (EIA RS-422):

High = +2V
Low = +0.5V

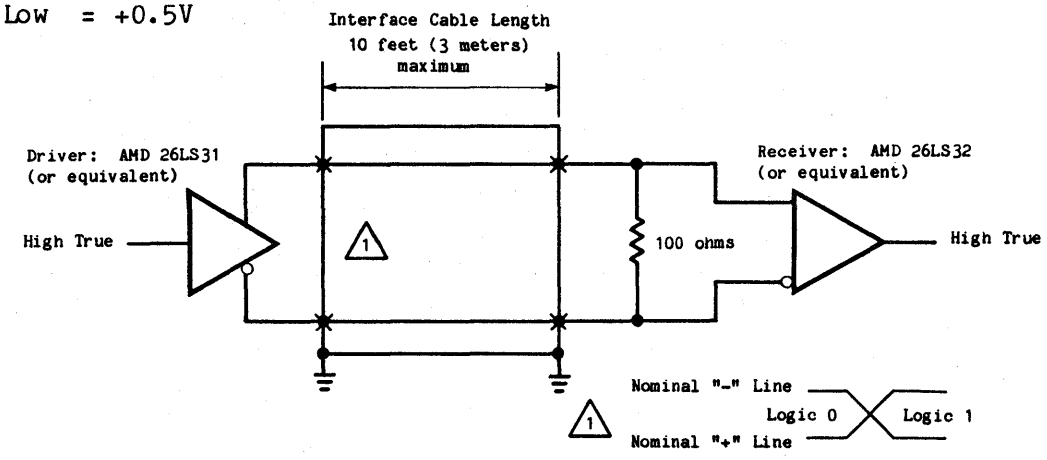


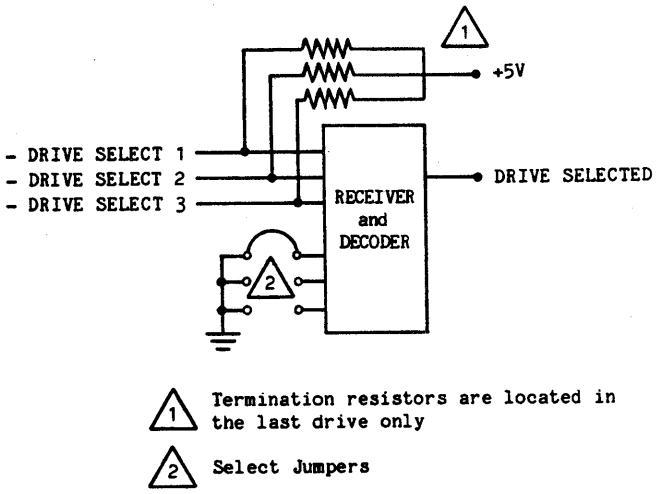
Figure 2-2. Data Line Driver/Receiver Combination

2.3 INTERFACE SIGNAL DESCRIPTIONS

2.3.1 Control Input Signals

DRIVE SELECT 1 through DRIVE SELECT 3 (J1, Pins 26, 28, and 30)

Up to seven drives can be connected to one host controller/formatter. Drive Select 1, Drive Select 2, and Drive Select 3 carry the binary-coded address of the drive to be selected. The address of the drive is set with drive-selection jumpers DA1, DA2, and DA3 as a binary combination. When the address is decoded and the decoded value matches the value specified by the three drive-selection jumpers, that drive is enabled to receive commands and transmit status. Drive Select 1 is the least significant bit.



Drive Address	Interface Signals DRIVE SELECT 3 (DA3)	DRIVE SELECT 2 (DA2)	DRIVE SELECT 1 (DA1)
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

1 = true, 0 = false

"Drive Address 0" is used as a "deselect" (i.e., no drive is selected).

Figure 2-3. Drive Select Termination and Matrix

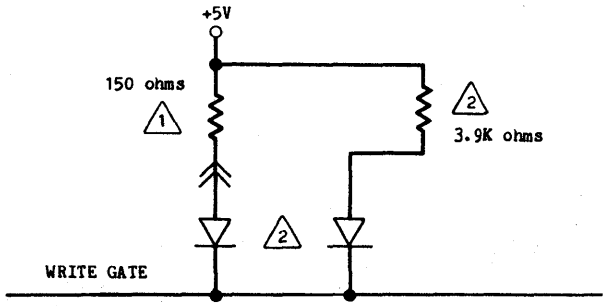
2.3.1 Control Input Signals (continued)

HEAD SELECT 2^0 through HEAD SELECT 2^3 (J1, Pins 14, 18, 4, and 2)

These four head-select lines furnish a binary-coded address which, when decoded, selects the corresponding data head. The four lines provide for the selection of up to sixteen data heads (addressed 0 through 15). A 150-ohm resistor pack allows for line termination. For 1550-series drives, the maximum number of data heads is fifteen. The heads are addressed Ø through 14 (depending on the model) in a binary-coded sequence where Head Select 2^0 is the least significant bit. If all four Head Select lines are inactive, Head Ø is selected. An attempt to write to a head with an address greater than any contained in the drive will result in a write fault.

WRITE GATE (J1, Pin 6)

When the Write Gate signal is active, (i.e., low) data may be written to the disk. The high-to-low transition of this signal creates a write splice and initiates the writing of the Data PLO Sync field by the drive; refer to Section 5. When formatting, the Write Gate signal should be deactivated for two bit times minimum between the address area and the data area to identify to the drive the beginning of the Data PLO Sync field. This line is protected from terminator power loss by implementation of the circuit as shown in Figure 2-4.



1 Part of the termination resistor pack in the last drive of the daisy chain.

2 Permanently located in the drive.

Figure 2-4. Write Gate Termination

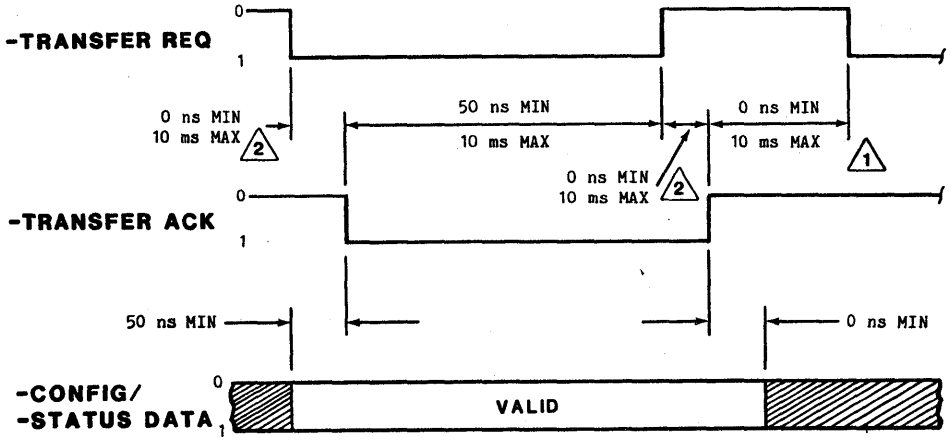
READ GATE (J1, Pin 32)

When the Read Gate signal is active (i.e., low), data may be read from the disk. This signal should be activated only during a PLO Sync field and at least the number of bytes defined by the drive prior to the ID or Data Sync bytes. The length of the PLO Sync field is determined by the response to the Request PLO Sync Field Length command. Read Gate must be dropped before a splice area and raised again after going through the splice area. A 150-ohm resistor pack allows for line termination.

2.3.1 Control Input Signals (continued)

TRANSFER REQUEST (J1, Pin 24)

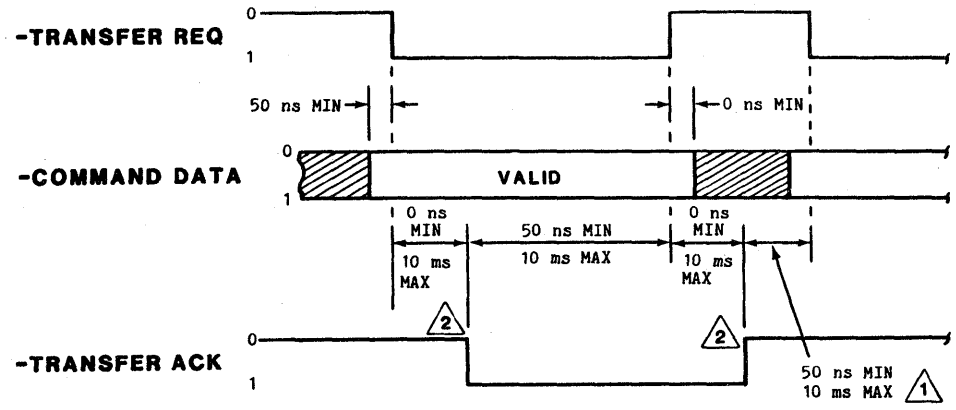
The Transfer Request signal is a "handshake" signal used in conjunction with the Transfer Acknowledge signal during Command and Configuration/ Status transfers; see Figures 2-5 and 2-6 for timing. Typical timing for the complete 17-bit transfer is less than 200 microseconds.



1 Except on the last bit.

2 Typical timing is less than 10 microseconds.

Figure 2-5. One Bit Transfer Timing - From Drive



1 Except on the last bit.

2 Typical timing is less than 10 microseconds.

Figure 2-6. One Bit Transfer Timing - To Drive

2.3.1 Control Input Signals (continued)

ADDRESS MARK ENABLE (J2, Pin 4)

The Address Mark Enable signal is a control input in the radial (J2) cable. It is not multiplexed. This signal line is permanently terminated in the drive as shown in Figure 2-1.

a. For Soft Sector Configuration

The Address Mark Enable signal, when active with the Write Gate signal, causes an Address Mark to be written. The Address Mark Enable signal must be held active for 24 bit times; see Figure 2-7 for timing.

The low-to-high transition (or de-assertion) of the Address Mark Enable signal, while Write Gate is active, causes the drive to begin writing the ID PLO Sync field; refer to Figure 5-4.

If both the Write Gate and Read Gate signals are false, the active state of the Address Mark Enable signal causes a search for Address Marks.

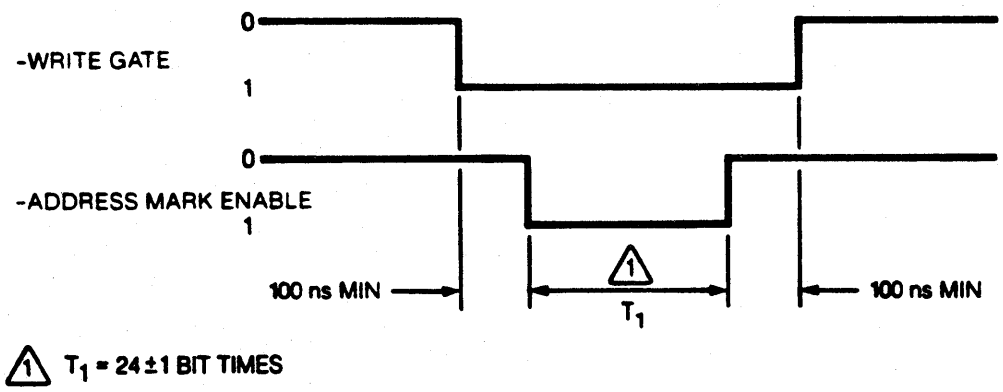


Figure 2-7. Write Address Mark Timing

b. For Fixed Sector Configuration

Assertion of the Address Mark Enable signal does not cause an Address Mark to be written. The trailing edge of the signal with the Write Gate signal true initiates the writing of the header PLO Sync field; refer to Figure 5-2.

2.3.1 Control Input Signals (continued)

COMMAND DATA (J1, Pin 34)

When a command is sent to the drive, sixteen bits of serial data, plus parity, are presented on this line. Figure 2-8 shows the structure for the command data word.

Parity utilized in all commands is odd. The parity bit is a "1" when the number of 1 bits in a sixteen-bit command is even. As a result, the total number of 1 bits in a command, including parity, is always odd.

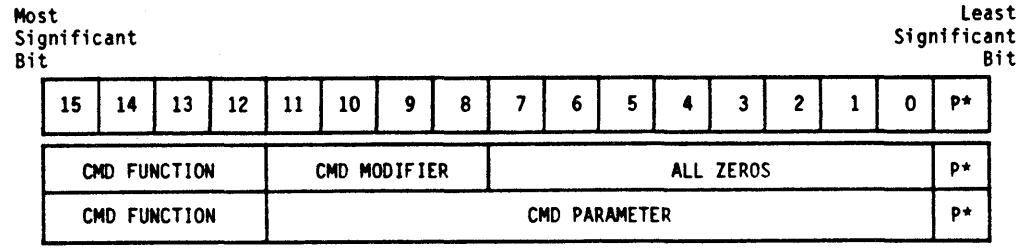


Figure 2-8. Command Data Word Structure

Command Data is controlled by "handshake" protocol with the Transfer Request and Transfer Acknowledge signals; Figure 2-6 specifies the timing. Upon receipt of the serial data, the drive performs the function specified by the bit configuration. The most significant bit (MSB) is transmitted first. No communications should be attempted unless the Command Complete line is true. Command definitions associated with the various bit configurations are shown in Table 2-4.

Note that the Command Data line must be at a logic zero when not in use.

Command Codes (Table 2-4)

0000 - Seek

The Seek command causes the drive to seek to the cylinder indicated by bits 0 - 11. A Seek command restores track and data strobe offsets to zero.

0001 - Recalibrate

The Recalibrate command returns the data heads to Cylinder Ø. This command also restores track and data strobe offsets to zero.

COMMAND DATA (continued)

TABLE 2-4. COMMAND DATA DEFINITION

CMD FUNCTION BITS 15	14	13	12	CMD FUNCTION DEFINITION	CMD MODIFIER APPLICABLE (Bits 11-8)	CMD PARAMETER APPLICABLE (Bits 11-0)	STATUS/CONFIGURATION DATA RETURNED TO CONTROLLER
0	0	0	0	SEEK	NO	YES	NO
0	0	0	1	RECALIBRATE	NO	NO	NO
0	0	1	0	REQUEST STATUS	YES	NO	YES
0	0	1	1	REQUEST CONFIGURATION	YES	NO	YES
0	1	0	0	SELECT HEAD GROUP (not implemented)	NO	YES	NO
0	1	0	1	CONTROL	YES	NO	NO
0	1	1	0	DATA STROBE OFFSET	YES	NO	NO
0	1	1	1	TRACK OFFSET	YES	NO	NO
1	0	0	0	INITIATE DIAGNOSTICS	NO	NO	NO
1	0	0	1	SET BYTES PER SECTOR	NO	YES	NO
1	0	1	0	- RESERVED	-	-	-
1	0	1	1	- RESERVED	-	-	-
1	1	0	0	- RESERVED	-	-	-
1	1	0	1	- RESERVED	-	-	-
1	1	1	0	- SET CONFIGURATION (not implemented)	NO	YES	NO
1	1	1	1	- RESERVED	-	-	-

NOTES:

1. All unused or not applicable lower-order bits must be zero.
2. Any reserved or unimplemented command or function is treated as an invalid command.
3. Simultaneous data strobe and track offsets are allowed by multiple commands.

0010 - Request Status

The Request Status command causes the drive to send 16 bits of status information to the host controller as determined by the command modifier bits. Parity is odd for all responses.

Request Standard Status

When command modifier bits 11 - 8 of the Request Status command are 0000, the drive responds with 16 bits of standard status information; refer to Table 2-11, Status Response Bits.

- Bits 15 - 12 of this status are defined as status bits, which do not cause the Attention signal to be asserted.

- Bits 11 - 0 of this status are fault or status change bits that cause the Attention signal to be asserted each time one is set.

COMMAND DATA (continued)

Request Vendor Unique Status (command modifier 0001)

Vendor Unique Status consists of one word of status and is only valid if bit 2 of the Standard Status is a one. This status is only intended to be utilized by trained field maintenance personnel and is not intended to be interpreted by disk controllers or operating systems. If this bit is detected, the controller should attempt to reset Standard Status and reattempt the original function a minimum of three times prior to defining the drive as inoperative. After the last attempt, the Vendor Unique Status word should be read by the controller and sent back to the system for a print out of these codes which may then be utilized by the field maintenance personnel. Command modifiers 1010 thru 1111 are not implemented.

0011 - Request Configuration

The Request Configuration command causes the drive to send 16 bits of configuration data to the host controller. The parity utilized in all configuration responses is odd. The specific drive configuration is specified by bits 11 - 8 of the command; see Table 2-5.

TABLE 2-5. REQUEST CONFIGURATION MODIFIER BITS

COMMAND MODIFIER BITS 11	10	9	8	FUNCTION
0	0	0	0	GENERAL CONFIGURATION OF DRIVE AND FORMAT
0	0	0	1	NUMBER OF CYLINDERS, Fixed
0	0	1	0	NUMBER OF CYLINDERS, Removable
0	0	1	1	NUMBER OF HEADS
0	1	0	0	MINIMUM UNFORMATTED BYTES PER TRACK
0	1	0	1	UNFORMATTED BYTES PER SECTOR (hard sector only)
0	1	1	0	SECTORS PER TRACK (hard sector only)
0	1	1	1	MINIMUM BYTES IN ISG FIELD
1	0	0	0	MINIMUM BYTES PER PLO SYNC FIELD
1	0	0	1	NUMBER OF WORDS OF VENDOR-UNIQUE STATUS AVAILABLE
1	0	1	0	RESERVED
1	0	1	1	RESERVED
1	1	0	0	RESERVED
1	1	0	1	RESERVED
1	1	1	0	RESERVED
1	1	1	1	VENDOR IDENTIFICATION (not implemented)

0100 - Select Head Group

Not implemented in the 1550 Series at this time. Execution will result in an Unimplemented Command fault.

2.3.1 Control Input Signals (continued)

COMMAND DATA (continued)

0101 - Control

The Control command causes operations specified by bits 11 - 8 to be performed as shown in Table 2-6.

TABLE 2-6. CONTROL COMMAND MODIFIER BITS

COMMAND MODIFIER BITS 11	10	9	8	FUNCTION
0	0	0	0	RESET INTERFACE ATTENTION AND STANDARD STATUS (Bits 0-11)
0	0	0	1	- RESERVED
0	0	1	0	- RESERVED
0	0	1	1	START SPINDLE MOTOR *
0	1	0	0	- RESERVED
0	1	0	1	- RESERVED
0	1	1	0	- RESERVED
0	1	1	1	- RESERVED
1	X	X	X	- RESERVED

* This command is effective only when the spindle control option jumper is installed; see Figure 3-2.

0110 - Data Strobe Offset

The Data Strobe Offset command causes the drive to offset the data strobe in the direction specified by bits 11 - 8; see Table 2-7. The 1550 Series implements only one value of Data Strobe Offset. The drives respond to all offset commands as legal functions by offsetting the one value in the specified direction. Seek or Recalibrate commands restore offsets to zero. Simultaneous Track and Data Strobe offsets are allowed by using multiple commands.

TABLE 2-7. DATA STROBE COMMAND MODIFIER BITS

COMMAND MODIFIER BITS 11	10	9	8	FUNCTION
0	0	0	0	RESTORE OFFSET TO Ø
0	0	0	1	RESTORE OFFSET TO Ø
0	0	1	0	EARLY OFFSET 1
0	0	1	1	LATE OFFSET 1
0	1	0	0	EARLY OFFSET 2
0	1	0	1	LATE OFFSET 2
0	1	1	0	EARLY OFFSET 3
0	1	1	1	LATE OFFSET 3
1	X	X	X	- RESERVED

2.3.1 Control Input Signals (continued)

COMMAND DATA (continued)

0111 - Track Offset

The Track Offset command causes the drive to perform a track offset in the direction specified by bits 11 - 8; refer to Table 2-8. The 1550 Series implements only one value of Track Offset. The drives respond to all offset commands as legal functions by offsetting the one value in the specified direction. Seek and Recalibrate commands restore the offsets to zero. Simultaneous Track and Data Strobe offsets are allowed by the use of multiple commands.

TABLE 2-8. TRACK OFFSET COMMAND MODIFIER BITS

COMMAND MODIFIER BITS 11	10	9	8	FUNCTION
0	0	0	0	RESTORE OFFSET TO Ø
0	0	0	1	RESTORE OFFSET TO Ø
0	0	1	0	POSITIVE OFFSET 1
0	0	1	1	NEGATIVE OFFSET 1
0	1	0	0	POSITIVE OFFSET 2
0	1	0	1	NEGATIVE OFFSET 2
0	1	1	0	POSITIVE OFFSET 3
0	1	1	1	NEGATIVE OFFSET 3
1	X	X	X	- RESERVED

1000 - Initiate Diagnostics

The Initiate Diagnostics command causes the drive to perform internal diagnostics. The Command Complete signal indicates the completion of the diagnostics. The Attention signal, along with the Command Complete signal, indicates that a fault was encountered and that status should be requested to determine a proper course of action. Extended fault information is made available in one word of Vendor Unique Status; see COMMAND DATA (Request Status, 0010).

1001 - Set Unformatted Bytes Per Sector

Note that this command is valid only if the drive is configured to be in the drive hard sector mode.

The Set Unformatted Bytes Per Sector command causes the drive to set the number of bytes per sector indicated by bits 11 - 0. Sector size may be selected in one-byte increments, with a minimum of 82 bytes/sector. If this command is not implemented by the host controller, default sector sizes may be jumper selected by default sector option jumpers; see Section 3.3.2.

2.3.1 Control Input Signals (continued)

COMMAND DATA (continued)

1110 - Set Configuration

Not implemented in the 1550 Series at this time. Execution will result in an Unimplemented Command fault.

2.3.2 Control Output Signals

The output signals transfer drive status to the host controller. All J1 output signals are enabled/gated by their respective Drive Select line decode; J2 output control signals are ungated. Figure 2-1 shows the driver/receiver combination used in 1550-series drives for control output signals.

DRIVE SELECTED (J2, Pin 1)

Drive Selected is the status line that informs the host system of the selection status of the drive. This signal goes active when the drive is programmed as drive n (where n = 1, 2, 3, 4, 5, 6, or 7) and the Drive Select lines at J1 are activated by the host system to produce a binary code equal to n.

READY (J1, Pin 22)

When true, together with the Command Complete signal, the Ready signal indicates that the drive is conditioned to read, write, or seek. When this line is false, seeking or writing is inhibited.

CONFIGURATION/STATUS DATA (J1, Pin 8)

The drive presents serial configuration or status data on this line upon request from the host controller. The serial data is made available at the interface using Transfer Request and Transfer Acknowledge signals for the "handshake" protocol; see Figure 2-5. The parity used is odd. Once initiated, 16 bits plus parity are transmitted, MSB first. Refer to Figure 2-9 for the data word structure.

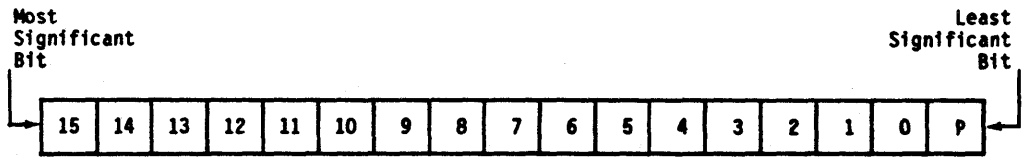


Figure 2-9. Configuration/Status Data Word Structure

2.3.2 Control Output Signals (continued)

CONFIGURATION/STATUS DATA (continued)

Figure 2-10 shows a typical serial operation.

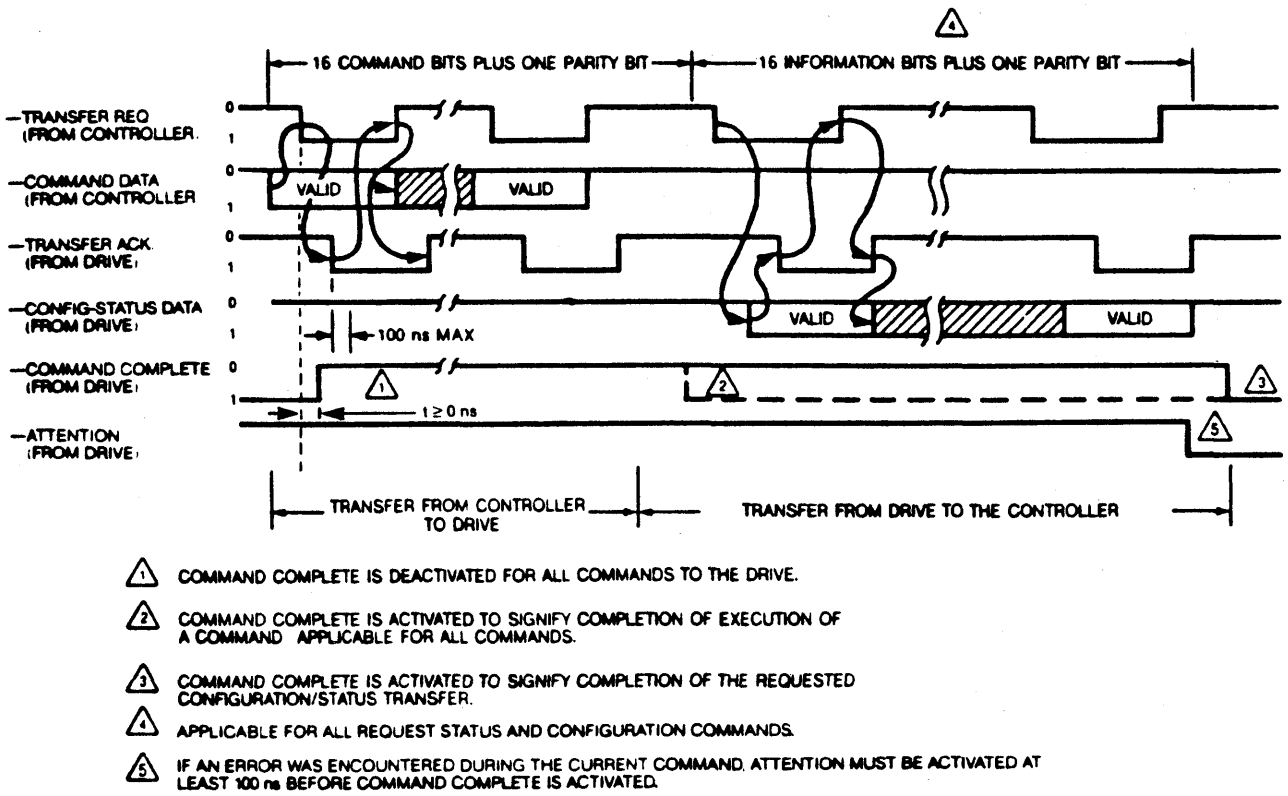


Figure 2-10. Typical Serial Operation(s)

1) Configuration Response Bits

In response to the Request Configuration (0011) command, 16 bits of configuration information are returned to the host controller.

- If the command modifier bits (11 - 8) are 0000, the general configuration status information shown in Table 2-9 is returned.

- If command modifier bits (11 - 8) other than 0000 are used, the specific configuration data shown in Table 2-10 is returned for each Request Configuration command with those modifiers.

CONFIGURATION/STATUS DATA (continued)

TABLE 2-9. GENERAL CONFIGURATION RESPONSE BITS

BIT POSITION	FUNCTION	VALUE
15	TAPE DRIVE	0
14	FORMAT SPEED TOLERANCE GAP REQUIRED	0
13	TRACK OFFSET OPTION AVAILABLE	1
12	DATA STROBE OFFSET OPTION AVAILABLE	1
11	ROTATIONAL SPEED TOLERANCE > 0.5%	0
10	TRANSFER RATE > 10 MHz	0
9	TRANSFER RATE > 5 MHz ≤ 10 MHz	1
8	TRANSFER RATE ≤ 5 MHz	0
7	REMOVABLE CARTRIDGE DRIVE	0
6	FIXED DRIVE	1
5	SPINDLE MOTOR CONTROL OPTION IMPLEMENTED	X Selectable
4	HEAD SWITCH TIME > 15 usec	0
3	RLL ENCODED (not MFM)	1
2	CONTROLLER SOFT SECTORED (ADR Mark)	X] Selectable
1	DRIVE HARD SECTORED (Sector Pulses)	X
0	CONTROLLER HARD SECTORED (Byte Clock)	0

TABLE 2-10. SPECIFIC CONFIGURATION RESPONSE BITS

COMMAND MODIFIER BITS 11	10	9	8	CONFIGURATION RESPONSE
0	0	0	1	NUMBER OF CYLINDERS, Fixed
0	0	1	0	NUMBER OF CYLINDERS, Removable Media (zero)
0	0	1	1	NUMBER OF HEADS BITS 15-8: Removable drive heads BITS 7-0: Fixed heads
0	1	0	0	MINIMUM UNFORMATTED BYTES PER TRACK
0	1	0	1	MINIMUM UNFORMATTED BYTES PER SECTOR (hard sector only)
0	1	1	0	NUMBER OF SECTORS PER TRACK (drive hard sector only) BITS 15-8: Reserved BITS 7-0: Sectors per track
0	1	1	1	MINIMUM BYTES IN ISG FIELD BITS 15-8: ISG Bytes after Index/Sector Pulse BITS 7-0: Bytes per ISG
1	0	0	0	MINIMUM BYTES PER PLO SYNC FIELD BITS 15-8: Reserved BITS 7-0: Bytes per PLO Sync Field required when READ GATE is asserted
1	0	0	1	NUMBER OF WORDS OF VENDOR-UNIQUE STATUS AVAILABLE BITS 15-4: Reserved BITS 3-0: Number of vendor-unique status words
1	0	1	0	RESERVED
1	1	1	0	
1	1	1	1	VENDOR IDENTIFICATION (not implemented)

2.3.2 Control Output Signals (continued)

CONFIGURATION/STATUS DATA (continued)

2) Status Response Bits

In response to the Request Status (0010) command, 16 bits of status information are sent to the host controller; see Table 2-11.

a. Bits 15 - 12 are defined as state bits which do not cause the Attention signal to be asserted.

b. Bits 11 - 0 are fault or status-change bits which cause the Attention signal to be asserted.

TABLE 2-11. STATUS RESPONSE BITS

BIT POSITION	FUNCTION
15	- RESERVED
14	REMOVABLE MEDIA NOT PRESENT
13	WRITE PROTECTED, Removable Media
12	WRITE PROTECTED, Fixed Media
11	- RESERVED
10	- RESERVED
9	SPINDLE MOTOR STOPPED (1)
8	POWER-ON RESET CONDITIONS EXIST (2)
7	COMMAND DATA PARITY FAULT
6	INTERFACE FAULT
5	INVALID OR UNIMPLEMENTED COMMAND FAULT (3)
4	SEEK FAULT
3	WRITE GATE WITH TRACK OFFSET FAULT
2	VENDOR UNIQUE STATUS AVAILABLE
1	WRITE FAULT (4)
0	REMOVABLE MEDIA CHANGED

(1) Spindle Motor stopped due to previous command to stop, or drive is in Power-On Reset condition.

(2) Reconfiguration or Start Spindle Motor command may be required.

(3) This status is issued when a command is received which is invalid or has not been implemented.

(4) Conditions that can cause a Write Fault are:

a. Write current in a head without WRITE GATE active, or no write current with WRITE GATE active and the drive selected.

b. Multiple heads selected, no head selected, or improperly selected with WRITE GATE active.

c. WRITE GATE active to a write-protected drive.

d. Simultaneous activation of READ GATE and WRITE GATE.

e. DC voltages grossly out of tolerance.

2.3.2 Control Output Signals (continued)

TRANSFER ACKNOWLEDGE (J1, Pin 10)

The Transfer Acknowledge signal functions as a "handshake" signal with the Transfer Request signal during Command and Configuration/Status transfers; refer to Figures 2-5 and 2-6.

ATTENTION (J1, Pin 12)

The Attention signal is asserted when the drive wants the host controller to request Standard Status. Generally, this is a result of a fault condition or a change of status. Writing is inhibited when Attention is asserted. The Attention signal is deactivated by Reset Interface Attention; see Section 2.3.1, COMMAND DATA (Control, 0101).

INDEX (J1, Pin 20; and J2, Pin 20)

An Index pulse is generated once per disk revolution (nominally every 16.7 milliseconds) to indicate the beginning of a track. This signal is normally high and makes the transition to logical true to indicate Index; see Figure 2-11. Only the transition from high to low (the leading edge) is valid. This signal is available on J1 (gated) and on J2 (ungated).

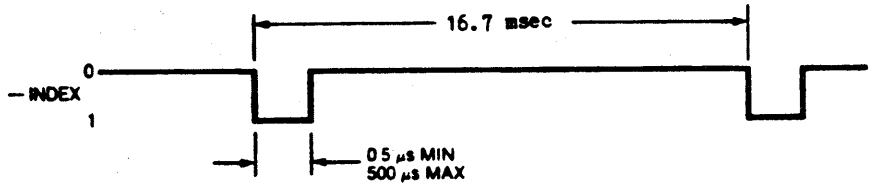


Figure 2-11. Index Pulse Timing

SECTOR or ADDRESS MARK FOUND (J1, Pin 16; and J2, Pin 2)

The Sector and Address Mark Found signals are mutually exclusive and thus share the same line. The signal used is determined by the option configuration and is user-selectable by means of a jumper; refer to Section 3.3.2. These signals are available on J1 (gated) and J2 (ungated).

1) Sector (Drive Hard Sector)

This optional interface signal indicates the start of a sector. No short sectors are generated. The leading edge of the sector pulses is the only edge that is accurately controlled.

2.3.2 Control Output Signals (continued)

Note that the Index pulse indicates sector zero; see Figure 2-12.

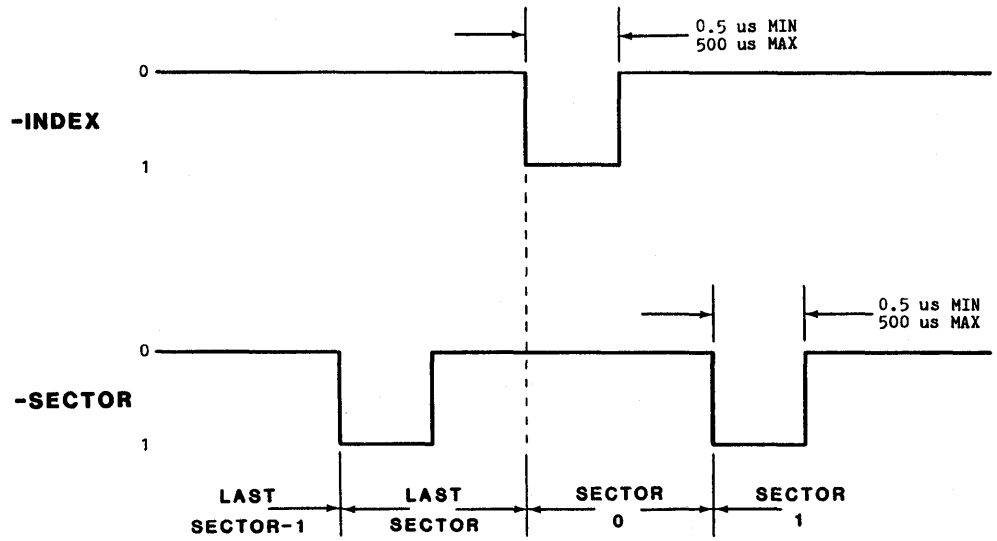
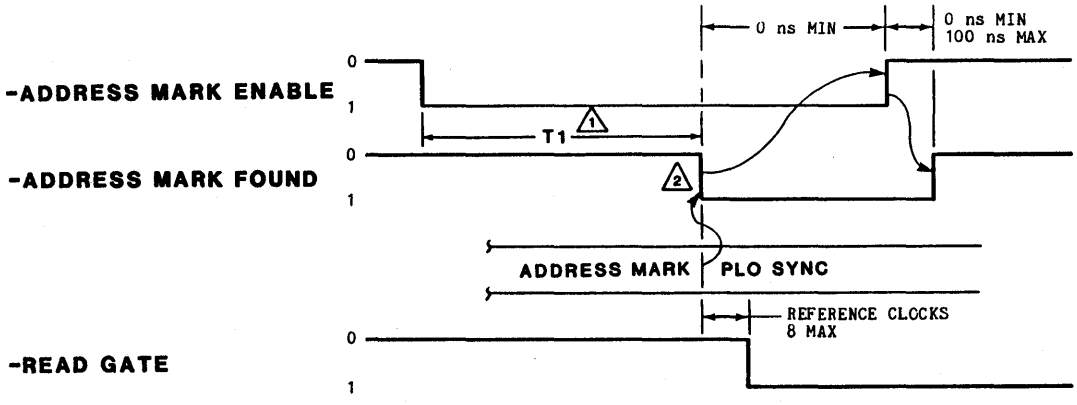


Figure 2-12. Sector Pulse Timing

2) Address Mark Found (Controller Soft Sector)

This signal indicates the detection of the end of an Address Mark; see Figure 2-13 for timing.



1 T1 = 24 bit times minimum.

2 Leading edge indicates the location of the end of an address mark.

Figure 2-13. Read Address Mark Timing

2.3.2 Control Output Signals (continued)

COMMAND COMPLETE (J2, Pin 3)

The Command Complete status line permits the host controller to monitor the drive's activity, without selecting the drive.

The Command Complete signal goes false for the following reasons:

- A recalibration sequence is initiated (by drive logic) at power-on, if the read/write heads are not positioned over Track Ø.
- Upon receipt of the first Command Data bit.

The Command Complete signal remains false during the entire command sequence.

2.3.3 Data Transfer Signals

All data-transfer lines between the drive and the host system are differential in nature and may not be multiplexed. Four pairs of balanced signals are used to transfer data: NRZ Write Data, NRZ Read Data, Write Clock, and Read/Reference Clock. Figure 2-2 shows the driver/receiver combination used for data-transfer signals.

NRZ WRITE DATA (J2, Pins 13 and 14)

The NRZ Write Data pair of signals defines the data to be written on the disk. The data is clocked by Write Clock; see Figure 2-14 for timing.

NRZ READ DATA (J2, Pins 17 and 18)

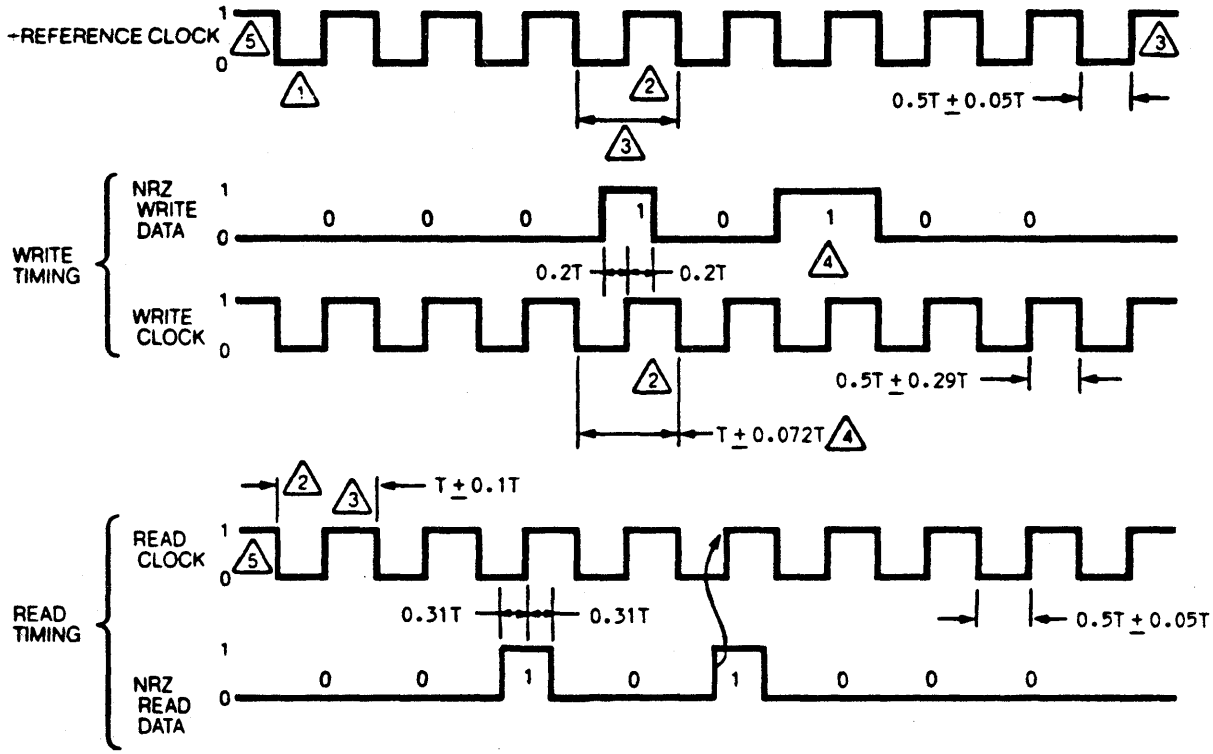
Read Data is transmitted to the host system via the NRZ Read Data signal pair. The data is clocked by the Read/Reference Clock signal; see Figure 2-14 for timing. These lines are held at a zero level until PLO sync has been obtained and the data is valid.

WRITE CLOCK (J2, Pins 7 and 8)

The Write Clock pair of signals is provided by the host controller, at the bit data rate. This clock frequency is dictated by the Read/Reference Clock during the write operation; see Figure 2-14 for timing. Write Clock need not be supplied to the drive continuously, but it should be supplied prior to a write operation and should last for the duration of the operation.

READ/REFERENCE CLOCK (J2, Pins 10 and 11)

The timing diagram shown in Figure 2-14 illustrates the sequence of events (with associated timing restrictions) for proper read/write operation of the 1550-series drives. The Read/Reference Clock signal from the drive determines the data-transfer rate. The transition from Read Clock to Reference Clock is performed without "glitches," but up to two clock cycles may be missing. Read/Reference Clock is synchronized to spindle rotation.



NOTES

1. ALL TIMES IN ns MEASURED AT I/O CONNECTOR OF THE DRIVE. T IS THE PERIOD OF THE CLOCK SIGNALS AND IS THE INVERSE OF THE REFERENCE OR READ CLOCK FREQUENCY.
2. SIMILAR PERIOD SYMMETRY SHALL BE IN ± 4ns BETWEEN ANY TWO ADJACENT CYCLES DURING READING OR WRITING.
3. EXCEPT DURING A HEAD CHANGE OR PLO SYNCHRONIZATION THE CLOCK VARIANCES FOR SPINDLE SPEED AND CIRCUIT TOLERANCES SHALL NOT VARY MORE THAN -5.5% to +5.0%. PHASE RELATIONSHIP BETWEEN REFERENCE CLOCK AND NRZ WRITE DATA OR WRITE CLOCK IS NOT DEFINED.
4. THE WRITE CLOCK MUST BE THE SAME FREQUENCY AS THE DRIVE SUPPLIED REFERENCE CLOCK. (i.e. THE WRITE CLOCK IS THE CONTROLLER RECEIVED AND RETRANSMITTED DRIVE REFERENCE CLOCK)
5. REFERENCE CLOCK IS VALID WHEN READ GATE IS INACTIVE. READ CLOCK IS VALID WHEN READ GATE IS ACTIVE AND PLO SYNCHRONIZATION HAS BEEN ESTABLISHED.
6. SEE FIGURE 2-2 FOR DEFINITION OF Ø AND 1 ON THESE DIFFERENTIAL SIGNAL LINES.

Figure 2-14. NRZ Read/Write Data Timings

2.4 READ, WRITE, AND FORMAT PARAMETERS

2.4.1 General Summary of Critical Read-Function Timing Parameters

Controller variations of the read timing are allowed if the following drive-dependent parameters are met:

- Read Initialization Time

  A read operation may not be initiated until 15 microseconds following a head change.

- Read-Gate Timing

  The Read Gate signal may not be enabled or true during a write-splice area. The Read Gate signal must be deactivated one bit time minimum before a write-splice area and may be enabled one bit time minimum after a write-splice area.

- Read Propagation Delay

  Data read at the interface is delayed by up to nine bit times from the data recorded on the disk.

- Read Clock Timing

  Read Clock and Read Data are valid within the number of PLO Sync field bytes specified by the drive configuration after Read Enable and a PLO Sync field is encountered. The Interface Read/Reference Clock line may contain no transitions for up to two Reference Clock periods for transitions between reference and read clocks. The transition period will also be one-half of a Reference Clock period minimum with no shortened pulse widths.

2.4.2 General Summary of Critical Write-Function Parameters

Controller timing variations in the record-update function are allowed if the following drive-dependent write (and interrelated read) timing parameters are met:

- Read-to-Write Recovery Time

  Assuming head selection is stabilized, the time lapse from deactivating READ GATE to activating WRITE GATE shall be five Reference Clock periods minimum.

- Write Clock-to-Write Gate Timing

  Write Clock must precede Write Gate by a minimum of two and a half Reference Clock periods.

- Write-Driver Plus Data-Encoder Turn-On from Write Gate

  The write-driver plus data-encoder turn-on time (write-splice width) is between three and seven Reference Clock periods.

- Write-Driver Turn-Off from Write Gate

  To account for data-encoding delays, the Write Gate signal must be held on for at least two byte times after the last bit of the information to be recorded.

- Write-to-Read Recovery Time

  The time lapse before Read Gate or Address Mark Enable signals can be activated after deactivating the Write Gate signal is ten microseconds.

- Head-Switching Time

  The Write Gate signal must be deactivated at least one microsecond before a head change. Write Gate may not be activated until 15 microseconds after a head change or after the Command Complete signal is true.

- Reference Clocks Valid Time

  The Read/Reference Clock lines will contain valid Reference Clocks within two Reference Clock periods after deactivation of the Read Gate signal. Pulse widths will not be shortened during the transition time, but clock transitions may not occur for up to two Reference Clock periods.

- Read Clocks Valid Time

  The Read/Reference Clock line will contain valid Read clocks within two Clock periods after PLO synchronization is established. Pulse widths will not be shortened during the Reference Clock to Read Clock transition time, but missing clocks may occur for up to two clock periods.

- Write Propagation Delay

  Write data received at the I/O connector will be delayed by the Write Data encoder by up to eight bit times maximum prior to being recorded on the disk.

SECTION 3. INSTALLATION

3.1 PHYSICAL INTERFACE

The electrical interface between the 1550-series drive and the host system is accomplished via five connectors: J1, J2, J3, J4, and J5. The connectors and their recommended mating connectors are described below.

3.2 POWER AND INTERFACE CABLES AND CONNECTORS

Figure 3-1 shows the locations of the power and interface connectors. Pin assignments for J1, J2, and J3 are listed in Section 2.1.

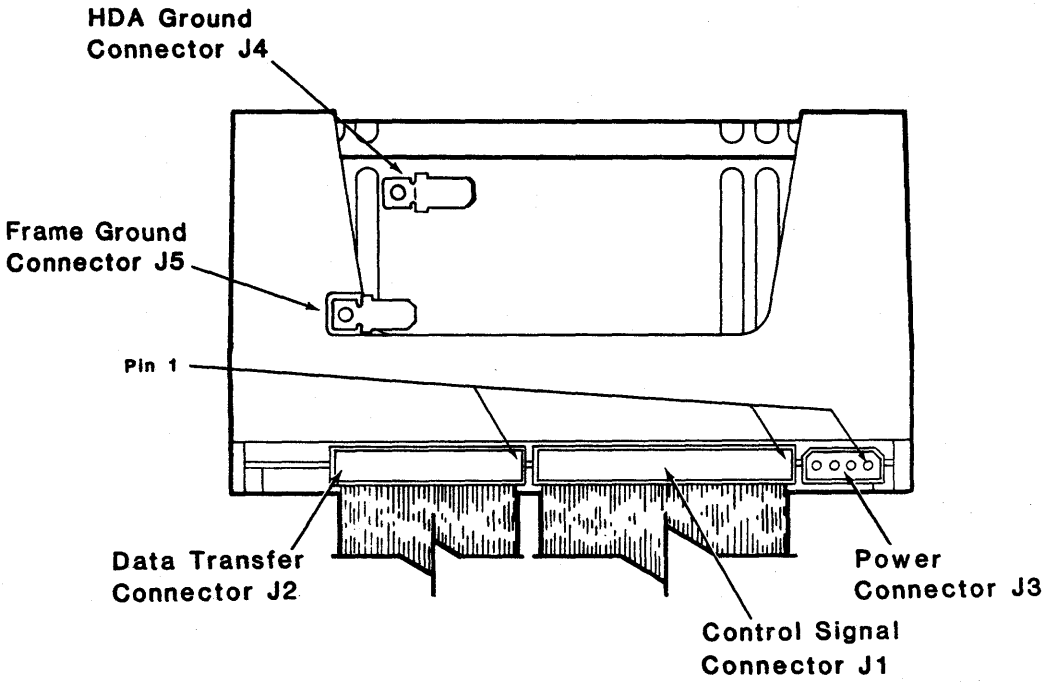


Figure 3-1. Power and Interface Connections

The signal interface connection is made through connectors J1 and J2 on the Device Electronics board. The control cable interconnects the host controller and J1; the data cable interconnects the controller and J2.

- Control Signal Connector J1

  J1 is a 34-pin board-edge connector. The signals on this connector control the drive and transfer drive status to the host controller.

  Recommended Cable: 3M Scotchflex 3365/34
  Mating Connector: AMP 88373-3 (key slot between pins 4 and 6)

- Data Transfer Connector J2

  J2 is a 20-pin board-edge connector. The signals on this connector contain read or write data.

  Recommended Cable: 3M Scotchflex 3365/20
  Mating Connector: AMP 88373-6 (key slot between pins 4 and 6)

- DC Power Connector J3

  J3 is a 4-pin, keyed AMP MATE-N-LOCK connector. This connector supplies DC power (+5V and +12V) to the drive.

  Mating Connector: AMP 1-480424-0
  Pins: AMP 350078-4

  Suggested Wire Size: 18 AWG

- Ground Connectors J4 and J5

  1/4-inch spade lugs J4 and J5 are provided for grounding; system characteristics determine the proper ground connection. J4 is located on the HDA, and J5 is located on the outer Frame.

  Mating Connector: AMP 62187-1 or equivalent

3.3 DRIVE OPTION SELECTION

3.3.1 Drive Addressing and Interface Termination

Figure 3-2 shows the locations of the three Drive Address jumpers (DA1, DA2, and DA3) for Drive Address selection (Drive Addresses 1 through 7) and Interface Terminator Pack RN1 on the Device Electronics board. The drive is configured for Drive Address 1 at the factory. Drive Address 0 is used as a "deselect" (i.e., no drive is selected).

TABLE 3-1. DRIVE SELECT MATRIX

Drive Address	Select Jumpers DA3	DA2	DA1
1	out	out	in
2	out	in	out
3	out	in	in
4	in	out	out
5	in	out	in
6	in	in	out
7	in	in	in

The three Drive Select interface lines are decoded to select the correspondingly addressed drive to the host controller/formatter. In multiple-drive systems, each drive must have its own unique address.

Terminator Pack RN1 provides proper termination for the interface lines. When daisy-chaining multiple 1550 drives, the terminator is installed only in the last drive on the daisy chain.

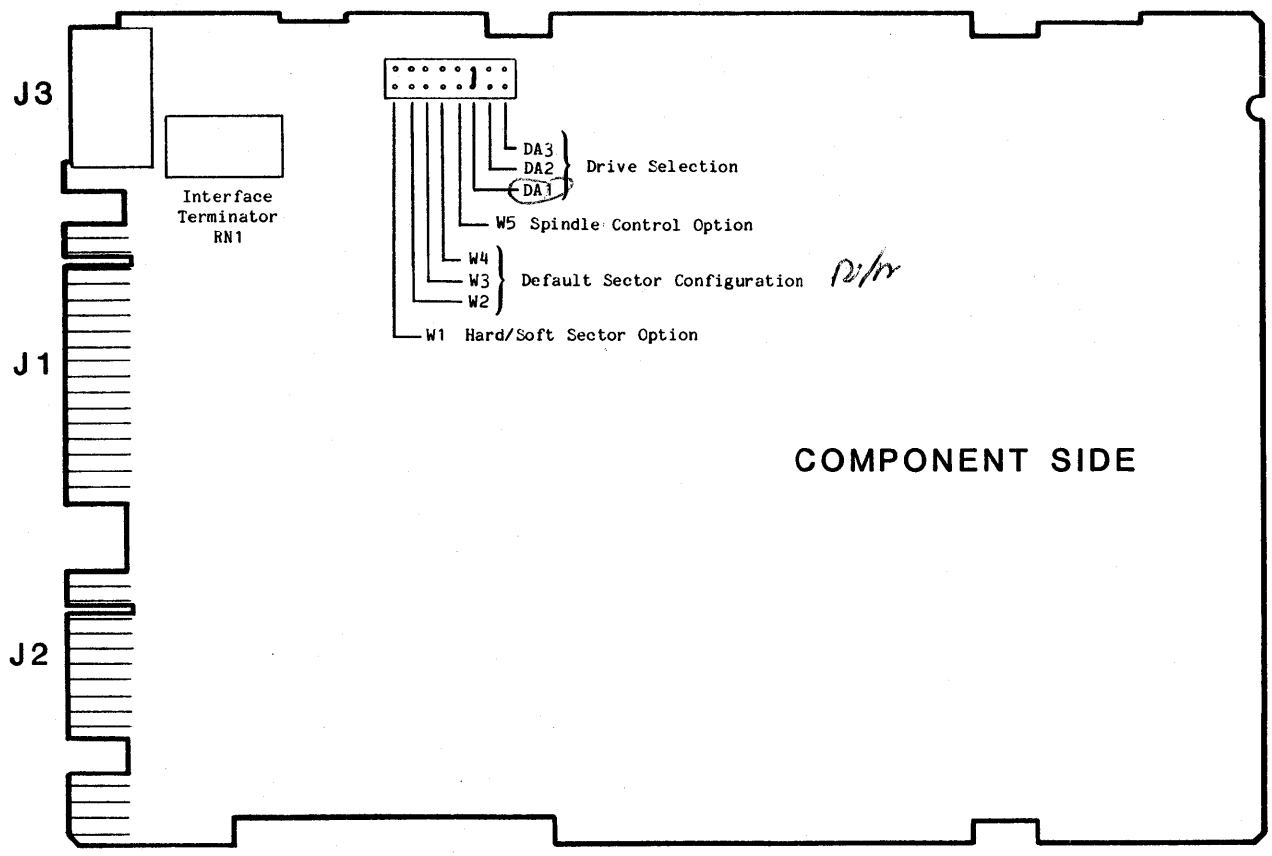


Figure 3-2. Option Jumpers and Interface Terminator

3.3.2 Spindle Control Option

Jumper W5 selects the spindle control option.

- When W5 is installed, the drive must wait for a Start Spindle command to start the spindle motor.
- When W5 is not installed (the factory default configuration), the drive automatically starts the spindle motor at power-on.

3.3.3 Sectoring Options

Figure 3-2 shows the locations of the four jumpers (W1, W2, W3, and W4) associated with sector configuration options.

Jumper W1 selects hard- or soft-sectored mode.

- When W1 is installed, the drive is configured to operate in the soft sector mode. Address mark generation and detection are enabled, and the Sector/Address Mark Found interface signal is used to report address mark found. Sector size is selected by the host controller.

- When W1 is not installed (the factory default configuration), the drive is configured to operate in the hard sector mode. The Sector/Address Mark Found interface signal is used to transmit sector pulses to the host controller.

  Sector pulses are derived from the servo disk. The number of sector pulses generated is equal to:

$$\text{INT}\left[\frac{20{,}832}{n}\right]$$

  Where 20,832 = byte clock derived from servo disk

  INT = integer part of

  n = the number of bytes/sector (82 minimum)

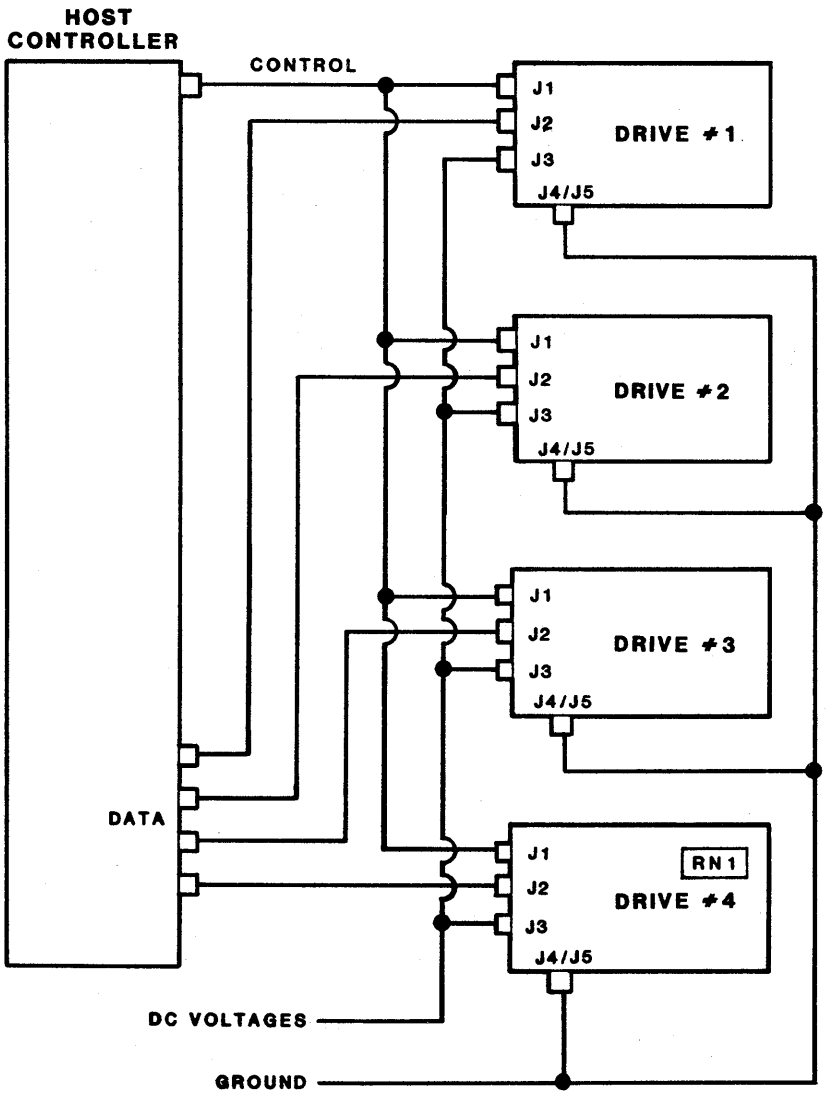
The number of bytes/sector may be specified using the Set Bytes Per Sector command or by selecting a default sector configuration with option jumpers W2, W3, and W4. Sector configurations may be selected as shown in Table 3-2. Other combinations of sector numbers and bytes per sector are available; contact Micropolis Product Support for details.

TABLE 3-2. DEFAULT HARD SECTOR CONFIGURATION WITH JUMPER OPTIONS

SECTORS	BYTES/SECTOR		JUMPERS		
	Formatted	Unformatted	W4	W3	W2
35	512	595	out	out	out
36	512	578	out	out	in
19	1024	1096	out	in	out
9	2048	2314	out	in	in
5	4096	4166	in	out	out
32	512	651	in	out	in
64	256	325	in	in	out
1	20832	20832	in	in	in

3.4 DAISY-CHAINING THE 1550 DRIVE

Up to seven 1550-series drives may be connected to a single host controller/ formatter. Control signals at J1 are transmitted via standard, daisy-chain interconnection. Data signals at J2 are transmitted via radially connected data-transfer lines. Figure 3-3 shows the connections for a system configuration using four drives.



NOTES: 1) Interface Terminators RN1 is installed only in the last physical drive in the control chain.

2) Connectors J4 and J5 are provided for grounding; system characteristics determine the proper ground connection.

Figure 3-3. 1550 Daisy-Chain Configuration

3.5 DIMENSIONS AND MOUNTING

The 1550 Series uses industry-standard mounting for 5 1/4-inch Winchester disk drives (the same as for 5 1/4-inch flexible disk drives). Figure 3-4 shows the mounting hole locations. The length of the mounting screws must be such that the screws do not penetrate the side mounting holes by more than 0.14 inch or the bottom mounting holes by more than 0.20 inch. Maximum torque applied to the screws must not exceed 10 in-lbs.

Recommended orientation is vertical on either side, or horizontal with the Device Electronics board down; other mounting orientations may be used provided the ambient air temperature around the drive is kept at or below 50°C (122°F).

Inasmuch as the drive frame acts as a heat sink to dissipate heat from the unit, the enclosure and mounting structure should be designed to allow natural convection of heat around the HDA and outer frame. If the enclosure is small or if natural convection is restricted, a fan may be required.

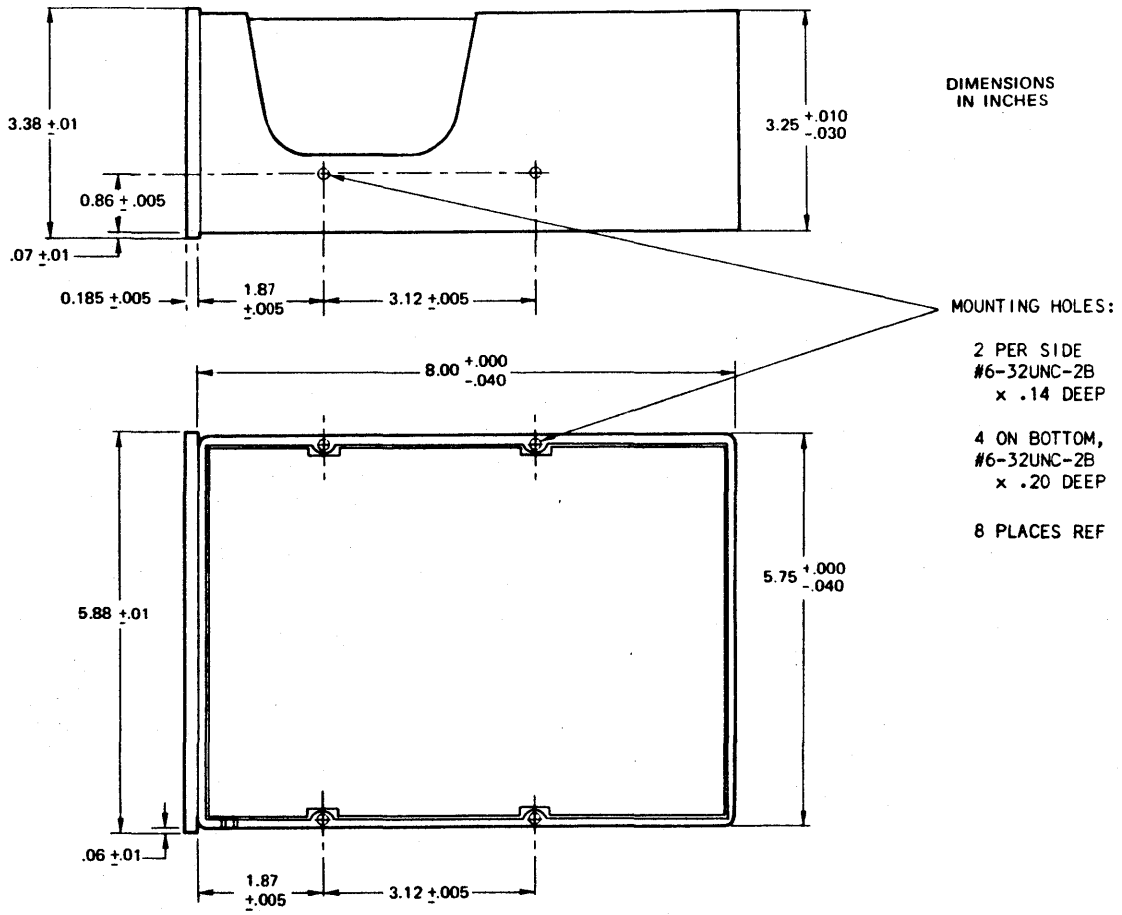


Figure 3-4. Dimensions and Mounting

SECTION 4. POWER REQUIREMENTS

4.1 POWER SUPPLY REQUIREMENTS

DC voltage and current requirements for the 1550 Series are shown below. Voltages may be applied to the drive in any sequence during power-up. Voltage verification must be performed at the drive connector. The rise time of the +5V must be less than one second for proper operation of the power-on reset circuits. Figure 4-1 shows the current profile for the +12V.

TABLE 4-1. DC POWER REQUIREMENTS

Voltage	Start-up Avg.	Start-up Peak	Idle Avg.	Idle Peak	Seeking (1) Avg.	Seeking (1) Peak	Ripple (maximum)
+5V ±5% maximum: (2)	2.0A	2.0A	2.0A	2.0A	2.0A	2.0A	2%
+12V ±5% (3) typical: (4)	4.25A	4.25A	1.80A	1.90A	2.25A	3.10A	2%
maximum: (2)	4.35A	4.35A	2.00A	2.10A	2.45A	3.30A	

(1) These values are for 1/3-stroke seeks with an 8-millisecond idle period between seeks to simulate a typical system environment.

(2) Maximum values to be considered for power supply design and system integration.

(3) +5%, -10% tolerance during start-up.

(4) Typically measured values.

DC POWER PIN ASSIGNMENTS (Connector J3)

Pin	Voltage	Pin	Voltage
1	+12 VDC	3	+5 RETURN
2	+12 RETURN	4	+5 VDC

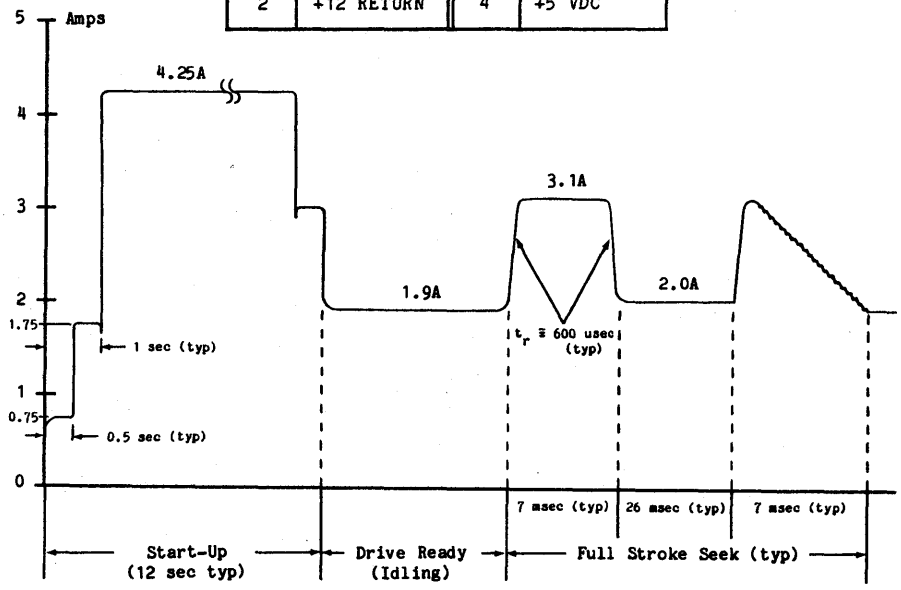


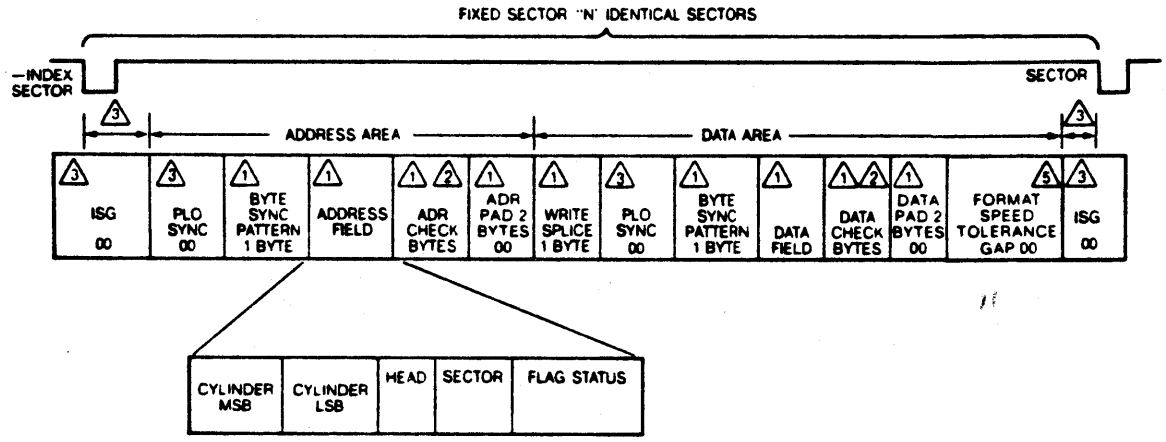
Figure 4-1. 12V Peak Current Profile (typical, 1558-15)

SECTION 5. DATA ORGANIZATION

5.1 TRACK FORMAT

5.1.1 Fixed Sector Format

The record format on the disk is under control of the host controller. The Index and Sector pulses are available for use by the controller to indicate the beginning of a track and allow the controller to define the beginning of a sector. A suggested format for fixed data records is shown in Figure 5-1.



(1) THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

(2) THE NUMBER OF CHECK BYTES IS USER DEFINED.

(3) PLO SYNC FIELD AND ISG ARE REPORTED IN RESPONSE TO THE REQUEST CONFIGURATION COMMANDS:
- ISG IS 16 BYTES MINIMUM (12 BYTES AFTER INDEX, 4 BYTES BEFORE INDEX).
- PLO SYNC IS 16 BYTES MINIMUM.

(4) ALL BYTE NUMBERS INDICATED ARE MINIMUMS EXCEPT ADDRESS FIELD LENGTH.

(5) NOT REQUIRED ON THE 1550 SERIES; SEE PAGE 5-4.

Figure 5-1. Fixed Sector Format

The format presented in Figure 5-1 consists of three functional areas:

- Intersector Gap
- Address Area
- Data Area

The Data Area is used to record the system's data files. The Address Area is used to locate and verify the track and sector location on the disk where the Data Areas are to be recorded.

5.1.1 Fixed Sector Format (continued)

Intersector Gap

The Intersector (ISG) Gap provides a separation between each sector. The minimum number of bytes in the Intersector Gap field is 16 (4 bytes before Index and 12 bytes after Index). The Intersector Gap size is chosen to provide for:

- Drive-required, write-to-read recovery time (minimum time between deassertion of Write Gate and assertion of Read Gate).
- Drive-required head-switching time.
- Host controller decision-making time between sectors.
- Other drive-required ISG times.
- Variations in detecting Index.

Address Area

The Address Area provides a positive indication of the track and sector locations. The Address Area is normally read by the host controller, and the address bytes verified prior to a Data Area read or write. The Address Area is normally only written by the controller during a format function, and thereafter only read to provide a positive indication of the sector location and establish the boundaries of the Data Area. The Address Area consists of the following bytes:

a. PLO Sync Field (11 bytes minimum)

PLO Sync Field bytes are required by the drive to allow the drive's read-data, phase-locked oscillator to become phase- and frequency-synchronized with the data bits recorded on the media. The host controller should send ØØs during this time. The number of bytes required may be determined by the Request Configuration command; see Section 2.3.1. The minimum number of bytes in the field is 11.

b. Byte Sync Pattern (one byte minimum)

This byte establishes byte synchronization (i.e., the ability to partition the ensuing serial bit stream into meaningful information groupings, such as bytes) and indicates to the host controller the beginning of the address field information. It is recommended that the Byte Sync Pattern contain the hexadecimal pattern FE.

c. Address Field

The Address Field bytes are user-defined and interpreted by the host controller. A suggested format consists of five bytes, which allows two bytes to define the cylinder address, one byte to define the head address, one byte to define the sector address, and one byte to define flag status.

5.1.1 Fixed Sector Format (continued)

d. ADR Check Bytes (Address Field Check Codes)

An appropriate error-detection mechanism is generated by the host controller and applied to the address for file-integrity purposes. These codes are written on the media during formatting. Data integrity is maintained by the controller recalculating and verifying the address-field check codes when the address field is read.

ADR Check Bytes are user defined.

e. ADR Pad (two bytes minimum) - (Address Field Pad)

The Address Field Pad bytes must be written by the host controller and are required by the drive to ensure proper recording and recovery of the last bits of the address-field check codes. These pad bytes should be ØØs.

Data Area

The Data Area is used to record data fields. The contents of the data fields within the Data Area are specified by the host system. The remaining parts of the Data Area are specified and interpreted by the host controller to recover the data fields and ensure their integrity. The Data Area consists of:

a. Write Splice (one byte minimum)

This byte area is required by the drive to allow time for the write drivers to turn on and reach recording amplitude sufficient to ensure data recovery. Allowance should be made for this byte in the format, and the controller should send ØØs during this time.

b. PLO Sync Bytes (11 bytes minimum)

These bytes are required when reading to allow the drive's phase-locked oscillator (PLO) to become phase- and frequency-synchronized with the data bits recorded on the media. The host controller should send ØØs during these byte times. The number of bytes required may be determined by the Request Configuration command; see Section 2.3.1. The minimum number of bytes in the field is 11.

c. Byte Sync Pattern (one byte minimum)

The Byte Sync Pattern establishes byte synchronization and indicates the beginning of the data field to the host controller. It is recommended that the Byte Sync Pattern contain the hexadecimal pattern FE.

5.1.1 Fixed Sector Format (continued)

d. Data Field

The Data Field contains the host system's data files.

e. Data Check Bytes (Data Field Check Codes)

The Data Check bytes are generated by the host controller and are written on the media at the end of the Data Field. Data integrity is maintained by the controller recalculating and verifying the Data Field Check Codes or applying error correction algorithms, if applicable, when the Data Field is read.

The Data Check Field is user defined.

f. Data Pad (two bytes minimum) - (Data Field Pad)

The Data Field Pad bytes must be issued by the host controller. The pad is required by the drive to ensure proper recording and recovery of the last bits of the Data Field Check Codes. The controller should send ØØs during these byte times.

g. Format Speed Tolerance Gap

The Format Speed Tolerance Gap is not required. This is due to the fact that the Read/Reference clock is synchronized to the rotation of the disk by the servo phase-locked loop. The number of clocks between sector or index pulses is fixed and independent of spindle speed variation.

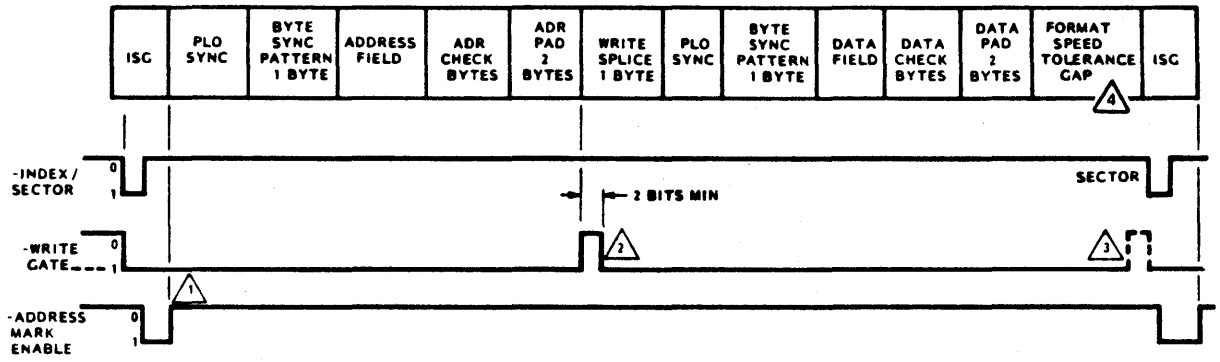
Fixed Sector Address Mark, Write Gate, and PLO Sync Format Timing

This timing is required to support all drives that utilize unique encoding for PLO Sync fields (i.e., if Bit 3 in General Configuration Response is set to 1).

NOTE

The beginning of each PLO Sync field must be specified by the host controller.

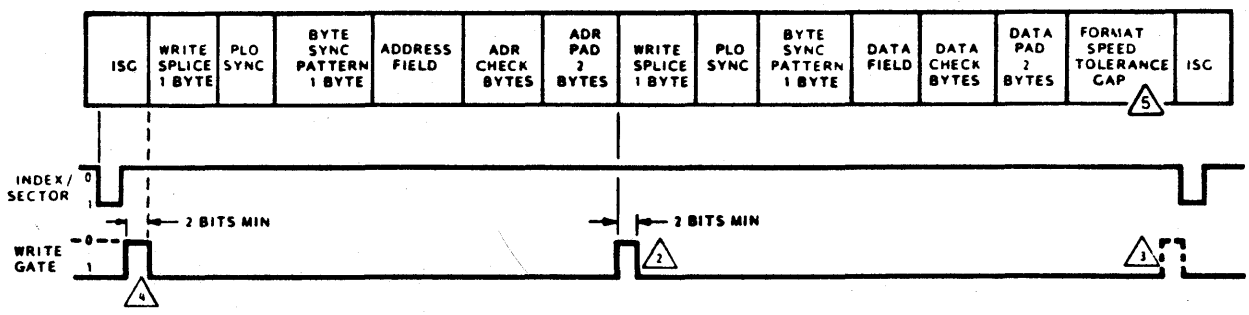
For compatibility with the host controller's soft sector mode of operation, the beginning of the Header PLO Sync field will be specified by the trailing edge of the Address Mark Enable signal when the Write Gate signal is true; see Figure 5-2.



1. TRAILING EDGE OF ADDRESS MARK ENABLE SIGNIFIES THE START OF HEADER PLO SYNC FIELD. DRIVE WILL NOT WRITE AN ADDRESS MARK ON THE DISK MEDIA.
2. TRANSITION REQUIRED ONLY IF THE DISK IS READ AFTER A FORMAT AND PRIOR TO A DATA FIELD WRITE UPDATE.
3. CONTROLLER MUST REINITIALIZE TIMING WITH EACH SECTOR PULSE (NEED NOT DEACTIVATE WRITE GATE).
4. NOT REQUIRED ON THE 1550 SERIES; SEE PAGE 5-4.

Figure 5-2. Fixed Sector Address Mark, Write Gate, and PLO Sync Format Timing

An alternative method that may be used to define the beginning of the Header PLO Sync field is to negate and then assert WRITE GATE immediately prior to the start of the Header PLO Sync field; see Figure 5-3.

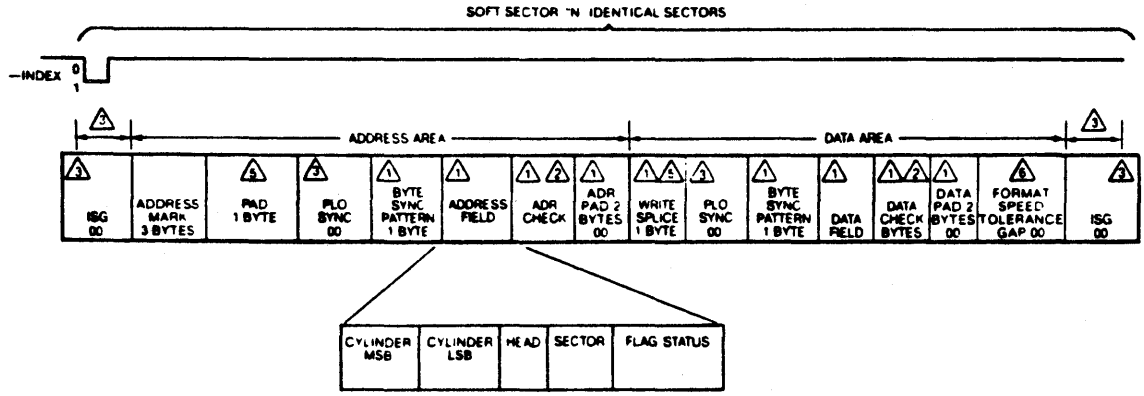


1. TRAILING EDGE OF ADDRESS MARK ENABLE SIGNIFIES THE START OF HEADER PLO SYNC FIELD. DRIVE WILL NOT WRITE AN ADDRESS MARK ON THE DISK MEDIA.
2. TRANSITION REQUIRED ONLY IF THE DISK IS READ AFTER A FORMAT AND PRIOR TO A DATA FIELD WRITE UPDATE.
3. CONTROLLER MUST REINITIALIZE TIMING WITH EACH SECTOR PULSE (NEED NOT DEACTIVATE WRITE GATE).
4. LEADING EDGE OF WRITE GATE (0 TO 1) DEFINES A WRITE SPLICE AND THE START OF THE HEADER PLO SYNC FIELD.
5. NOT REQUIRED ON THE 1550 SERIES; SEE PAGE 5-4.

Figure 5-3. Fixed Sector Address Mark, Write Gate, and PLO Sync Format Timing (alternative method)

5.1.2 Soft Sector Format

The format shown in Figure 5-4 is similar to the format commonly used for hard sector disk drives and indicates minimum requirements.



1. THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.
2. THE NUMBER OF CHECK BYTES IS USER DEFINED.
3. PLO SYNC FIELD AND ISG ARE AS REPORTED IN RESPONSE TO THE REQUEST CONFIGURATION COMMANDS.
4. ALL BYTE NUMBERS INDICATED ARE MINIMUMS EXCEPT ADDRESS FIELD LENGTH.
5. THIS AREA IS PART OF THE PLO SYNC FIELD TO ALLOW FOR READ GATE ACTIVATION DELAYS. CONTROLLER SHOULD TREAT THIS AS AN ADDITIONAL BYTE IN THE PLO SYNC FIELD.
6. NOT REQUIRED ON THE 1550 SERIES; SEE PAGE 5-4.

Figure 5-4. Soft Sector Format

Intersector Gap

The description of the Intersector Gap is the same as the description given in Section 5.1.1, Hard Sector Format.

Address Area

The descriptions of the functional areas in the Address Area are the same as the descriptions given in Section 5.1.1, Hard Sector Format. There are two additional fields in this format, Address Mark and Address Mark Pad.

a. Address Mark

The Address Mark is a three-byte field which precedes the Address Mark Pad and the PLO Sync. The contents of this field are drive-dependent and are written by the drive when the Write Gate and the Address Mark Enable signals are active simultaneously. Detection of an Address Mark indicates the beginning of a sector.

5.1.2 Soft Sector Format (continued)

b. Address Mark Pad

The Address Mark Pad is a one-byte field and is considered part of the PLO Sync field. Its purpose is to allow for Read Gate activation delays after detecting the Address Mark Found signal.

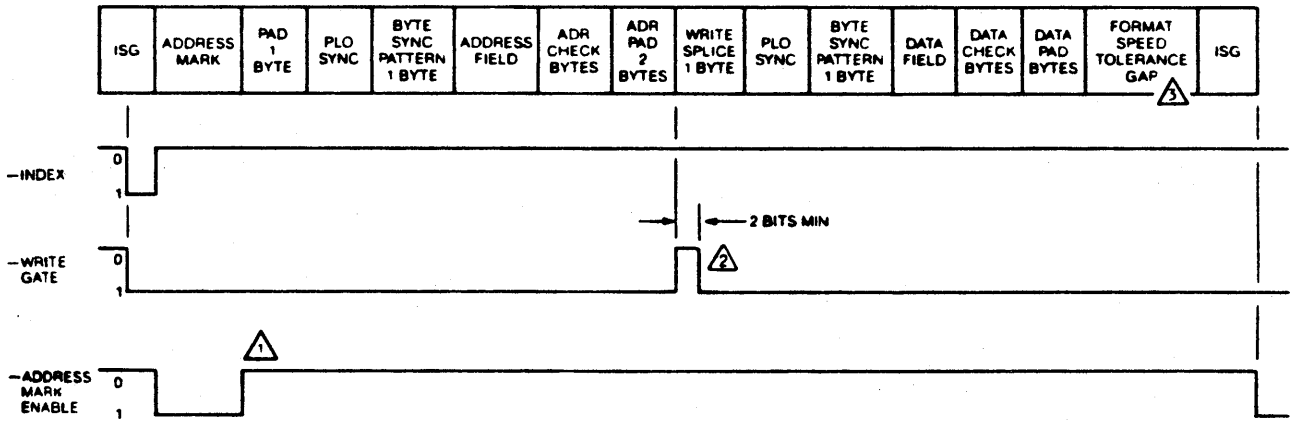
Data Area

The descriptions of the functional areas in the Data Area are the same as the descriptions given in Section 5.1.1, Hard Sector Format.

Soft Sector Address Mark, Write Gate, and PLO Sync Format Timing

This timing is used to support drives that utilize unique encoding for PLO Sync fields.

- The beginning of each PLO Sync field must be specified by the host controller.
- The beginning of the header PLO Sync field will be specified by the trailing edge of the Address Mark Enable signal when the Write Gate signal is true; see Figure 5-5.



1 TRAILING EDGE OF ADDRESS MARK ENABLE SIGNIFIES THE START OF HEADER PLO SYNC FIELD.

2 TRANSITION REQUIRED ONLY IF THE DISK IS READ AFTER A FORMAT AND PRIOR TO A DATA FIELD WRITE UPDATE.

3 NOT REQUIRED ON THE 1550 SERIES; SEE PAGE 5-4.

Figure 5-5. Soft Sector Address Mark, Write Gate, and PLO Sync Format Timing

5.2 ERROR RATES

An error may be defined as a discrepancy between recovered and recorded data. For example, bits may be missing, bits may have shifted, or there may be extra bits. Additionally, a Ø may appear as a 1, a 1 as a Ø, etc.

Errors are classified as soft or hard.

- A soft error is defined as being recoverable within six retries, excluding error correction and all known media defects. It shall occur no more than 10 in 10^{11} bits read.

- A hard error is defined as being unrecoverable after six retries. It shall occur no more than 10 in 10^{13} bits read. Seek errors shall not exceed 10 in 10^{7}.

It is common practice in many systems environments to minimize the effects of hard errors by following a write operation with a read-after-write verification. This ensures that data is written safely in a defect-free area. The failing sector is then mapped out of use by the system.

5.3 MEDIA DEFECTS

Micropolis specifies that all 1550-series disk drives will meet or surpass the following criteria:

> All drives shall have no more than one defect per megabyte of unformatted capacity. Additionally, Cylinder Ø shall be defect-free at the time of shipment.

Media defects are physical characteristics of the media which result in repetitive read errors when a functional drive is operated within specified operating conditions.

At the time of manufacture, a media test system evaluates every drive and identifies the location of each media defect. The defects are logged on a label affixed to the drive. Defective areas are identified by cylinder, head address, and number of bytes from Index. A printout (listing) of the defects is also shipped with each drive. In addition to listing the defects on the label and the printout, the defects are also mapped on the drive in the format shown in Figure 5-6.

A defect list is written for each surface. The list is written on the corresponding surface in Sector Ø of cylinder 1223 (the maximum cylinder) and is repeated on cylinder 1215 (the maximum cylinder minus eight). This redundancy is provided in case a defect occurs on the maximum cylinder.

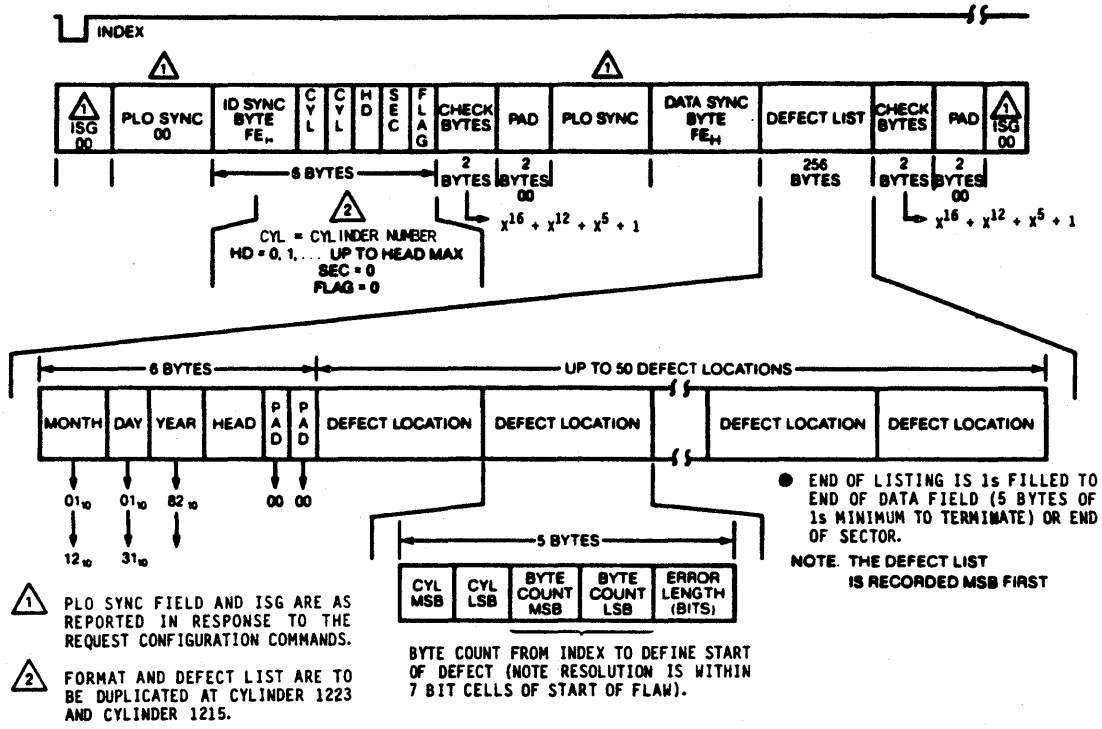


Figure 5-6. Defect List Format

The format for the data field portion (see Figure 4-20) of this sector is 256 bytes with two bytes of CRC:

a. Each defect entry uses five bytes.

b. The Byte Count is the number of bytes from Index.

c. The start of the actual defect may be off by up to seven bits because of the one-byte resolution.

d. The end of the defect list for each surface is indicated by five bytes of ones in the defect location field or at the end of the sector.

e. CRC check bytes should be used if that capability exists but may be ignored if multiple reads are a more desirable approach.

CRC is specified as follows:

- CRC is performed on non-inverted data.
- CRC is applied to the 256 bytes of data plus the sync byte.
- The CRC seed is two bytes long and is all zeros.
- The CRC formula is $X^{16} + X^{12} + X^5 + 1$.

SECTION 6. SERVICEABILITY AND TECHNICAL SUPPORT

6.1 ADJUSTMENTS AND MAINTENANCE

The 1550 Series of drives requires no adjustments or periodic maintenance. Additionally, no mechanical adjustments are required to prepare the drives for handling or shipment.

6.2 FIELD-REPLACEABLE COMPONENTS

The concept of repair by replacement of complete functional components is utilized in the 1550 Series, resulting in an MTTR of less than 15 minutes.

6.3 SERVICE DATA

See Micropolis Manual No. 104189 for complete maintenance and service data.

6.4 TECHNICAL SUPPORT

For assistance regarding spares, technical training, system integration, applications, etc., contact:

Micropolis Corporation
21123 Nordhoff Street
Chatsworth, CA 91311

Attn: Product Support

(818) 709-3300

- or -

Micropolis Corporation
European Operations
210 Elgar Road
Reading, Berkshire, RG2 OPJ
England

(734) 751315

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