

FDP-1 COMPUTER
ELECTRICAL ENGINEERING DEPARTMENT
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FDP-35-3

INSTRUCTION MANUAL

PART 3 -- I/O AND MASS MEMORY DEVICES

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Most I/O devices must be assigned before they are used. This avoids conflicts since only the program which has a given I/O unit assigned can use that unit.

Many I/O devices are operated with the ivk (op code 740000) instruction. All such devices used by a program are accessed through a program-selectable number called a "C-list index". The low 6 bits of the ivk instruction are the C-list index of the device to be operated. There are a few conventions regarding the indices assigned to certain types of devices. For example, the paper tape reader is typically operated as device number 10, and the punch as device 11. They could be assigned as other numbers, however. All devices operated by ivk's (except the typewriter) are assigned with "mta" instructions, usually mta 306. The low 6 bits of the AC give the required C-list index and the rest of the AC determines which I/O device is desired. Thus, the reader is typically assigned with AC = 30010 and is operated with ivk 10. Indices must be between 0 and 17 for most programs. It is possible to increase the upper limit to 77 by running the program in "PRL" mode.

Devices cannot be assigned unless the specified C-list index is free, i.e. no device of any kind already occupies that index. Hence, if the reader is already assigned at index 10, a subsequent attempt to assign it at index 10 would fail, not only because index 10 is occupied, but because the reader is "busy". (The fact that the present owner of the reader is the same program as the one trying to assign it again makes no difference.)

The mta instruction that assigns such a device will skip if the assignment is successful, i.e. the requested C-list index was free and the device was available (not assigned to the same or another console.)

All devices operated by the ivk instruction are dismissed with the mta 204 (770274) instruction with the C-list index in the low 6 bits of the AC.

The console typewriter is the one exception to the rule that all devices operated by ivk instructions must be assigned by a mta instruction. When a user logs in, the typewriter for that console is automatically assigned at index zero.

The W Register

Many IO devices that are interpreted by the supervisor require that more information be supplied than will fit in the AC and IO. Therefore, there is another register, called the "W" register, which exists inside the supervisor. A program can read and write its W register with the following instructions.

mta 0	Copy A into W
mta 1	Copy I into W
mta 2	Copy W into A
mta 3	Copy W into I

If an I/O device operation requires information in all three of A, I, and W, the program will typically load the data for W into the AC, transmit it to W with a mta, load the data for the AC and IO, and then execute the 1vk.

Typewriters

The instructions for operating the typewriters are

Instruction	Action
ivk 100	Type out 6-bit character in A(12-17).
ivk 200	Type in 6-bit character to A(12-17), clearing A(0-11).
ivk 300	Type out 6-bit character in I(12-17).
ivk 400	Type in 6-bit character to I(12-17), clearing I(0-11).
ivk 1300	Type out 7-bit character in A(11-17).
ivk 1400	Type in 7-bit character to A(11-17), clearing A(0-10).
ivk 1500	Type out 7-bit character in I(11-17).
ivk 1600	Type in 7-bit character to I(11-17), clearing I(0-10).

On typeout, bits other than the ones noted are ignored.

6-bit characters are the ones used by the actual typewriters. Programs operating typewriters in 6-bit mode must explicitly handle upshift (7^u) and downshift (7^d) characters.

In 7-bit mode, the timesharing supervisor handles case shifts automatically. The "100" bit (bit 11) of a character is on if the character is in upper case.

See the appendix to the assembler memo (PDP-45) for a list of character codes.

All type-out instructions wait until the typewriter is ready to accept them, i.e. the supervisor handles the necessary synchronization. Type-in instructions wait until a key is struck.

There are some other typewriter operations, used only in multiple sphere applications, which are described in part 5 of the instruction manual.

Paper Tape Reader

The FDP-1 has a photoelectric paper tape reader capable of reading 320 or 640 lines per second, as selected by a toggle switch on the left side of the reader rack (bay 11). Eight-hole tape is normally used, although five and seven hole tape may also be read.

The reader operates in one of two modes, alpha and binary. The mode is decided at the time the reader is assigned and cannot be changed except by dismissing and assigning it again.

The reader is assigned with the instruction mta 306 (770376) with AC = 300NN for alpha mode and 301NN for binary mode. This instruction will skip if the assignment is successful. In either mode the reader is operated with the instruction ivk NN (7400NN). NN is often chosen as 10.

Alpha mode

One line of tape is read and placed in the AC. Channel 1 (the end channel on the edge of the tape closer to the feedholes) is read into bit 17, channel 2 into bit 16, etc. for the number of channels on the tape. A(0-9) is cleared. If the reader is out of tape, the ivk does not skip. Otherwise the ivk will skip after the data has been read.

Binary mode

Three lines of tape are read. Channel 8 must always appear punched; if not, the line is ignored. Channel 7 is always ignored. Channels six through one of the first line are placed in A(0-5). A(6-11) is filled from the second line of tape, and A(12-17) from the third. If the reader is out of tape, the ivk does not skip. Otherwise the ivk will skip after the data has been read.

The system will do a certain amount of buffering of the input. Thus, if a program reads one line of tape, the supervisor will read many additional lines, which it will transmit to the program when subsequent ivk's are executed. If the tape is removed from the reader and replaced by another tape, the result may not be what is desired. The supervisor's buffer can be cleared by releasing the reader and re-assigning it.

Paper Tape Punch

The PDP-1 paper tape punch punches standard eight-hole tape at a speed of 63 lines per second.

The punch is assigned with the instruction mta 306 with AC = 400NN, and operated with the instruction ivk NN. NN is often chosen as 11.

The punch ivk causes one line of tape to be punched. Tape channels eight through one come from A(10-17) respectively. The rest of the AC is ignored. The feedhole is always punched.

CRT Display

The display is intended to be used as an on-line output device for the PDP-1. It is useful for high speed presentation of graphs, diagrams, drawings, and alphanumeric information. The unit uses solid-state circuits and has magnetic deflection and focus. The cathode ray tube has a P7 phosphor, allowing either a blue or yellow filter to be used to select the short or long persistence for photography purposes. Some characteristics of the display are --

- 1024 by 1024 addressable locations
- Plots 20,000 points per second
- Random point plotting
- Accuracy of point is 3 percent of raster size
- Raster size is 9.25 by 9.25 inches
- Origin may be at one of four points under control of each display instruction
- Brightness may be controlled to one of 8 levels under control of each display instruction

To the unaided eye, approximately 512 points are resolvable on each axis. Five of the eight brightness levels are considered visible. A photomultiplier tube may see all brightness levels.

Note that this device is not operated with the `ivk` instruction. The display does not need to be assigned. It can be operated from any console at any time.

The `dpy` instruction (73cb07) causes one point to be displayed on the scope. `A(0-9)` specifies the X coordinate and `I(0-9)` gives the Y coordinate. `A` and `I` remain unchanged after the `dpy` instruction. The three "b" bits control the brightness -- the order is 4, 5, 6, 7, 0, 1, 2, 3 where 4 is visible to photomultiplier tubes, 7 is barely visible, 0 is normal, and 3 is the brightest. The "c" bits control the centering. 0 makes the origin in the center of the scope, 1 puts it at the center of the bottom edge, 2 makes the origin be half way up the left edge, while 3 puts it at the lower left corner.

A `dpy` (that is, with the `i`-bit on) takes 40 microseconds to complete. `dpy-1` (lot 7) does not wait for the scope to complete. Since it is impossible to activate the scope too fast, one normally executes lot 7 instructions. This allows the program to continue while the scope is running.

Subroutines for plotting points and lines exist in the relocatable subroutine library.

Light Pen

The light pen is designed to be used with the CRT display. A program utilizing the light pen can give the user the ability to make choices by pointing at the display. For example, a CRT editor program could let the user point the light pen at the displayed text to specify the character or line to be edited.

About 39 microseconds after the last dpy (or dpy-1) instruction has occurred, a scope completion pulse interrogates the light pen. If it is seeing light at that time, program flag 3 is set. By clearing flag 3, displaying a point, waiting the requisite 40 microseconds and then checking flag 3, a program can determine whether the light pen saw light. Note that the light does not have to come from the scope face. A threshold control for the light pen sensitivity is located on the bottom of the scope tube cabinet.

If a program uses dpy instructions (that is, the iot instruction with the 1-bit on), flag 3 will be set, if it is going to be, when the dpy completes. If a program uses dpy-1 instructions, there must be at least 40 microseconds between the dpy-1 and the time that flag 3 is checked.

Subroutines for tracking the light pen can be found on the "filecase" tape.

Color Display

The color scope is used as an on-line output device for the PDP-1. The cathode ray tube has only a short persistence phosphor. Some characteristics of the display are ---

- 512 by 512 addressable locations
- Plots up to 10,000 points per second
- Random point plotting
- Origin may be at one of four points under control of each display instruction
- Brightness of each color may be independently controlled to one of 16 levels

The color scope is not operated with the `lvk` instruction. The display does not need to be assigned, and can be operated from any console at any time.

The color scope is normally left off when not in use. The scope should be turned on several minutes prior to using it by pushing the ON switch. When finished using the scope, depress the OFF switch and hold it down for a few seconds until the click of the hardware powering off is heard.

There are two instructions that operate the scope. The first is `lot 16` (`720016`) which sets the color register from `A(3-17)`. `A(3-5)` are respectively the red, green and blue enable bits. If the bit is zero, the beam is off regardless of the intensity specified elsewhere. If one, the beam will be on. `A(6-9)` is the red intensity, where intensity 0 is dimmest and 17 is brightest. `A(10-13)` is green intensity, and `A(14-17)` is blue intensity.

Setting of the color may be done at any time, even while the scope is displaying a point. If the color is changed while a point is being displayed, the display will be affected.

A point is displayed by an `lot cw17` (`72cw17`) instruction. `A(0-8)` indicates the horizontal or X coordinate and `I(0-8)` gives the vertical or Y coordinate. `A` and `I` remain unchanged after the `lot` instruction. The low two bits of "c", instruction bits 7-8, determine the centering of the display and are interpreted the same as for the non-color scope.

The high order bit of "c", instruction bit 6, determines the length of time the scope will take to display the point. If the bit is zero it will take 100 microseconds, and if the bit is one it will take 250 microseconds. A problem in using the faster `lot` is that widely separated points displayed sequentially may show noticeable distortion in position.

No `lot` to the color scope waits. An `lot` to display a point will be ignored if the scope is not finished with the previous display. If "w", instruction bit 11, is one, the `lot` instruction will skip only if the scope was indeed ready to display a point, and will not skip if the scope was busy. Thus a common programming sequence is `lot 117, jmp, =1` which will effectively wait until the point is accepted before continuing. If bit 11 is zero, the instruction will never skip.

Buttons and Switches

Four consoles of nine buttons and nine switches each can be connected to the PDP-1 to facilitate communications between users and the machine. Two standard panels are currently available, each of which has a set of buttons and switches on it. Either or both of these may quickly be replaced by inputs from user I/O equipment. However, the two panels (0 and 1) are the usual configuration.

The button and switch states are read into I by the instruction, rbt ("read buttons" = iot #237). This will set a bit in I for each button or switch which is on. Buttons go into I(0-8), and switches into I(9-17). The x field of the instruction determines which of the four panels is being read.

```
panel 0 = rbt
panel 1 = rbt 400
panel 2 = rbt 1000
panel 3 = rbt 1400
```

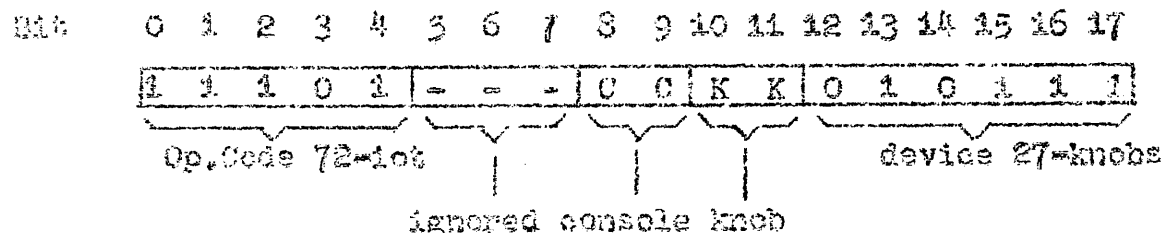
There is also a way to make the timesharing system signal a program when any button or switch changes. See part 5 of this Instruction Manual.

Knobs

Four consoles of four analog devices each can be connected to the computer. Two consoles with four knobs each are currently connected.

These may be replaced by inputs from external equipment by simply changing plugs. In the cable is a reference voltage which is nominally -10 volts. When triggered by a ckn instruction, the digital to analog converter measures the ratio of input voltage to reference voltage and puts this fraction in I[10-17]. In the case of the knobs, a reading of zero means the knob is fully counter-clockwise, while 377 means that it is fully clockwise.

The ckn instruction ("check knobs", = iot 27) has the following format —



Plotter

The Calcomp plotter features:

- 0.005 inch (0.127 mm) step size
- 300 steps/sec maximum speed
- 30 inch by 120 feet maximum paper size
- An adapter for 12 inch wide paper rolls
- Both liquid ink and ball-point pen

Liquid ink and ink pen points suitable for the plotter are made by Staedtler under the trademark "Kars". Standard Rapidograph points also work. Pen points and inks are available in a variety of widths and colors, respectively. Ball-point pens are more convenient to use than liquid ink, but produce lower quality drawings. Ball-point pens are available from Calcomp. In addition, there are some available with the plotter, for experimental use. Before using the plotter, have someone instruct you on procedures for setting up and putting away the plotter.

The plotter must be operated in "PRL" mode. A program enters this mode by executing the mta 403 instruction, and leaves it by executing mta 402. While in PRL mode, references to locations 0 through 77 of core module 0 are illegal. While in PRL mode, capability indices may be any number between 0 and 77. (The upper limit is 17 otherwise.)

The plotter is assigned with mta 306 with AC = 0727NN, and operated with ivk NN. NN is often chosen as 27. The plotter is operated with an ivk with data in the AC. The AC may contain three six-bit fields which are processed in the order A(12-17), A(6-11), then A(0-5) until either all three fields have been used or a field which is zero is encountered. Each six-bit field has the following format:

0	1	2	3	4	5	A(0-5)
6	7	8	9	10	11	A(6-11)
12	13	14	15	16	17	A(12-17)
up	down	+x	-x	+y	-y	

Up and down refer to the pen position. Moving in the +x direction causes paper to be rolled off the supply reel onto the floor. The coordinate system is right handed, and the maximum "y" travel is 30 inches.

It is not permissible to specify +x and -x, +y and -y, or "up" and "down" in the same command field. It is permissible to specify any other combination of x, y, and pen motion desired.

This instruction will complete when the plotter is ready to accept another command. The buffering is sufficient to keep the plotter running at full speed if no more than 3.5 milliseconds elapses from the time the plotter becomes ready. Subroutines for drawing lines and characters exist in the Relocatable Subroutine Library.

Clocks

The PDP-1 is equipped with numerous clock devices, but perhaps the most useful for ordinary purposes are the temporary clocks and the real-time clock. The temporary clocks can be used to cause a process to wait a specified time, and the real time clock provides high-resolution timing information.

The temporary clock ticks 1760 times per minute, or slightly less than 30 ticks per second. The clock is assigned with mta 305 with AC = 200NN, and used with an ivk NN. Unlike many other devices, the temporary clock is not limited to one copy, that is, any program can be sure of assigning its own clock whenever it wishes.

In order to wait for n ticks of the clock a program should load the AC with $-(n+1)$ and execute a clock ivk. At the end of the delay, the program will resume, with AC = 0. If the initial AC is ≥ -1 , the instruction will complete immediately with the AC unchanged. The following sequence would cause a 1/5 second delay in program execution (providing the clock be assigned on index 6):

```
lan 7   /load AC with  $-(5+1)$ 
ivir 6
```

The real time clock is usually read by the mta 103 instruction, which reads the high 18 bits of the time register into the AC and the low 18 bits into the IO. Any program may read the clock in this manner at any time. This clock ticks once every 100 microseconds, but the 36-bit counter takes 79 days to overflow. Thus, it provides an accurate time base for almost any program application.

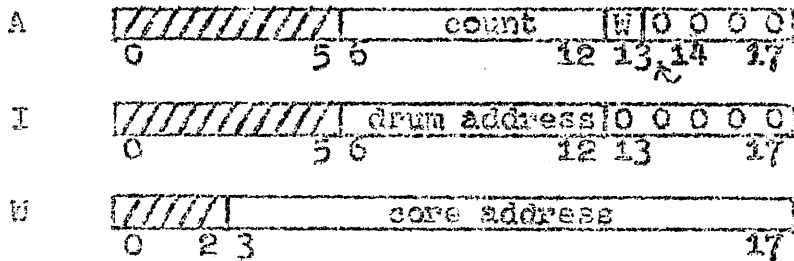
There is a program "time" on public tape 0 which reads the clock and displays the date and time on the CRT.

Drum Fields

A drum field is a 10000 (octal) word block of medium speed memory. Transfers take place between the drum and core memory.

Drum field assignment and operation is similar to that for I/O devices. Fields are assigned with mta 300 with AC = NN. The field is then read or written with ivk NN.

The contents of the AC, IO, and W registers required for a transfer is as follows:



The core address for the transfer is specified in W(3-17), the drum address in I(6-17), and the word count (plus 20 if writing) in A(6-17). Note that the drum address and word count must be multiples of 40 octal words and hence will always leave I(13-17) zero. If A(13) is zero, data will be read from the drum into core; if one, data will be written onto the drum. A(14-17) is ignored.

The count will always be interpreted as a multiple of 40 words, and, if zero, all 4K words will be transferred. Transfers are performed mod 10000 octal, so that if a transfer attempts to reference data beyond the end of the field, the references will "wrap around" to the beginning of the same field. A transfer may not cross a core boundary however. The core address need not be a multiple of 40 words. The instruction will skip if the transfer was successful. The contents of the registers are never changed.

WARNING - ET's text buffer is kept on drum fields on C-list index 2 and following (as many as necessary, but many texts need only field 2). Writing on these fields can destroy the text. Fields used for temporary storage by programs are often given numbers around 13 to 15.

Microtapes

The PDP-1 has four microtape (DECtape) transports.

WARNING - Most microtape operations are executed by the Microtape File System (see memo FDP-42), and most tapes have data stored on them in a format known to the File System. Programmers that use microtapes directly should be exceedingly careful, since writing on tapes can destroy files or even the tape directory. Scratch tapes exist, have appropriate labels affixed, and are provided for those who would like to test their tape programs.

People wishing their own microtapes for use on the PDP-1 should purchase them UNFORMATTED from DEC or another vendor. A special tape marking program is used to format the tape into 1102 (octal) blocks numbered 0 through 1101, each of which contains 400 (octal) 18.-bit words. These tape markings are compatible with the DEC standard markings for the PDP-1, 4, 6, 7, 9, 10 and 15.

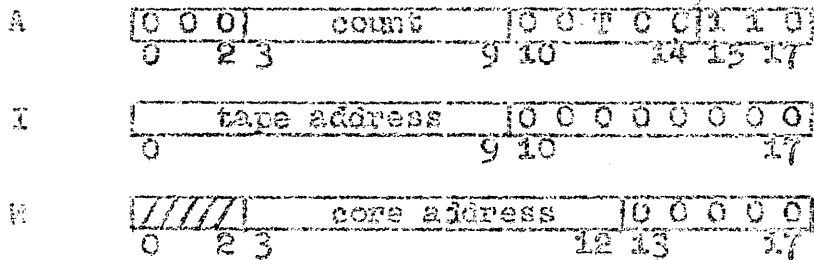
Mechanical operation of the tape drives

There are four major states of a tape drive. The first state is OFF. When a tape is in this state, the motors are not operating and tapes may be mounted or dismounted. State two is manual mode. In this mode the drive is under external control and tape may be wound forward or in reverse by the "fwd" or "rev" buttons respectively. The third state is automatic mode, which will light the light above the auto/run switch. In this state the tape is not moving but may at any time begin moving by command from the CPU. Write permit may be turned on by pushing the write/stop switch to write position for a moment, which will cause the light above the switch to turn on. If write permit is not on, the hardware will not allow the tape to be written on, but will allow read operations to occur. State four is when the computer is actively spinning the tape, during which time none of the front panel controls will have any effect.

Program operation of microtapes

Tape units are assigned with the instruction `ata 306`, with the AC containing `000NN`, and are operated with the instruction `ivk NN`. `T` specifies the transport number (0 to 3). `NN` is often chosen as 16.

The `ivk NN` instruction will rewind the tape or transfer data between core and the tape as specified by `A`, `I` and `W`, whose format is illustrated below:



The core address for the transfer is specified by `W(3-17)` and must be a multiple of 40 words, hence `W(13-17)` will be zero. The `I` register contains the starting tape address which is the initial block number multiplied by 400. If one thinks of the tape as containing `1102x400` words, the tape address is equal to the desired initial word, which must be a multiple of 400. The AC contains the number of words to be transferred, which must be a multiple of 400, plus other control information. (A word count of zero will be interpreted as 400, however.) The control information is as follows:

00 = 00	read from tape into core
10	write from core onto tape
01	rewind tape to beginning;
	program will wait until beginning reached.
11	rewind tape to beginning but don't
	wait for beginning to be reached. Any
	subsequent tape instruction will override
	this command and commence immediately.

For example -

- AC = 406 will read one block
- AC = 426 will write one block.
- AC = 16 will rewind and wait.
- AC = 36 will rewind and proceed.

Consecutive tape blocks are transferred between consecutive areas of core. All 400 words of each tape block must be transferred to or from a single core module. If more than one block is transferred, different blocks may be in different core modules. For example, starting a two block tape copy at core address `07400` is acceptable, but starting at core address `07500` is not, as it would require the last 100 words be written across a core boundary.

In all cases where the tape is to be used only on the PDP-1, the T bit, A(12), should be zero. If tapes from other computer installations are used on the PDP-1, see below for a description of translation. If all data was successfully transferred, the instruction will skip, A(0-11) will be zero, and A(12-17) will be unchanged. W will contain one plus the highest core address transferred. The IO will contain one plus the last tape address transferred.

If the transfer was not successful, A(0-11) will be the number of words remaining to be transferred, including the block which was in error. The IO will contain the tape address of the block in error. The W will have an error code which is one of the following:

- 0 tape unit is not in automatic status
- 1 block cannot be found (probably bad tape)
- 2 illegal core address specified
- 3 checksum error (data transfer took place anyway)
- 4 mark track error (probably bad tape)
- 5 data channel error (serious hardware malfunction)
- 6 write permit not on.

Only error 0 can occur for rewind operations.

Translation.

Microtapes are marked with block 0 at the beginning of the tape and block 1101 at the end. In order to perform multiple block transfers without stopping the tape unnecessarily and without burdening the user, the system translates the block numbers given by the program so that blocks that are consecutively numbered (as seen by the program) are two blocks apart on the actual tape. The actual renumbering is shown below.

logical/	0	1	...	437	440	441	442	...	1101
physical/	1	3	...	1077	1101	1100	1076	...	0

Setting the T bit to one will disable translation. Multiple block transfers will transfer consecutive physical tape blocks as expected.

External register and external levels

The instruction mta 500 (770570) is used to assign and deassign external levels and the External Register. The action of the mta 500 is determined by the contents of the AC as follows. Note that the external register and levels are not operated with ivk instructions, and hence the previous considerations regarding C-list indices do not apply.

A[0-5] Operation

- C0 Assign external levels. For all i , $1 \leq i \leq 7$, external level i is assigned if $A[i+40] = i$. For example, to assign external level 2, A should contain 40. The mta 500 will skip if the assignment is successful, i.e. no one else has the level(s) assigned.
- C1 Deassign external levels as above. No skip.
- C2 Assign External Register, shared. Skip if successful, i.e. no one else has it assigned as private.
- C3 Assign External Register, private. Skip if successful, i.e. no one else has it assigned.
- C4 Deassign External Register. No skip.

External Levels

- 3 Used for temporary hardware connections
- 4 External clock
- 6 Used for temporary hardware connections
- 7 Radio Astronomy antenna

The PDP-1 External Register is an 18-bit register which can be loaded and read by the PDP-1 and by I/O devices. The music hardware and the 8-bit D-A converter use the External Register. The External Register must be assigned before it can be used.

Instruction	Action
lei (724577)	Load External Register from I.
lea (724677)	Load External Register from A.
rer (724777)	Read External Register into I.

Music Hardware

The music hardware consists of six identical channels, one per voice. Each channel has a flip-flop which can be loaded from the accumulator sign bit (A(0)) by the appropriate lct instruction. The rate at which this flip-flop is turned on and off determines the pitch of the note played by that voice. The volume level for a given channel is controlled by three bits of the External Register. Zero in these bits is the softest, seven the loudest.

voice	loudness controlled by ext. reg. bits
0	6-8
1	9-11
2	12-14
3	15-17
4	0-2
5	3-5

Instruction	Function
72nn14	A(0) to voice n flip-flop, n=0,1,2,3,4,5 A(6-8) is ignored

A switch associated with each of channels 0-3 determines whether the output of that channel is connected to the left or right inputs of the stereo power amplifier. Voices 4 and 5 are connected to the right side. Four degrees of treble roll-off can be applied to the left and right sides independently. This is controlled by four toggle switches, two per side.

See the Music Programs memo, FDP-43, for information on the music compiler and the music player.

8-bit D-to-A Converter

The input to the 8-bit digital to analog converter is bits 10-17 of the External Register. The output will be -10 volts times the fraction in ER(10-17). The output appears on a BNC connector inside bay 10.