Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: TOGGLE SWITCH STORAGE SYSTEM TX-2

To: Group 63 Staff

From: Leopold Neumann L. Neumann

Date: April 21, 1958

Approved: B. M. G.

Abstract: The TX-2 toggle switch storage system is a bank of twenty-four, 37 bit registers, sixteen of which are completely variable by toggle switches on the main T.S.S. panel.

Three special plug-in units are used in the T.S.S. system: A T.S.S. Resistor Driver PIU which contains 2 separate 4 transistor amplifiers, each putting out a -25v, 125ma signal; A T.S.S. digit detector PIU which contains 6 separate inverters, each having an input diode; A T.S.S. -25v power unit which supplies -25 volts, referenced to the TX-2 -30v supply voltage, for use in the T.S.S. Resistor Driver.

LN:med

Distribution:

Baker, R.H. (Group 24)
Barck, P.E.
Best, R.L.
Bradspies, S.
Burke, R.L.
Clark, W.A.
Corderman, C.L.
Eckl, D.J.
Ellis, D.H.
Fadiman, J.R.
Farley, B.G.
Fergus, P.A.
Forgie, J.W.
Frankovich, J.M.
Gilmore, J.T.
Gerelds, G.W.
Gould, R.H.
Gurley, B.M.
Harwood, E.
Herndon, T.O.
Hudson, R.W.
Johnston, R.C.
Konkle, K.H.
Lin, C.S.
Mitchell, J.L.
Molnar, C.E.
Neumann, L. (10)
Norman, C.A.
Papian, W.N.
Peterson, H.P.
Raffel, J.I.
Savell, R.E.
Stockebrand, T.C.
Vecchia, F.M.
Zieman, H.E.

REMAINDER OF GROUP 63 STAFF TO RECEIVE ABSTRACT ONLY.

2. The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19 (122)-458.

This M-note will give a description of the TX-2 toggle switch storage system and the plug-in units used in this system.

(1) General

The TX-2 toggle switch storage is a bank of twenty-four 37 bit registers. Sixteen of these registers are completely variable by means of toggle switches on the main T.S.S. panel. The other eight registers are partially fixed but have some variable digits on a separate auxiliary T.S.S. panel.

The sixteen completely accessible registers are used in the computer operation for holding parameters, constants, and instructions that the programmer may wish to vary as the program is running. The eight partially variable registers will be used for starting routines that are fixed except perhaps for an address that would vary with individual programs.

(2) Basic Operation (ref. SD-67720)

The basic mechanism of the T.S.S. is a resistor-switch matrix. 888 7.5 K resistors and 888 switches (or fixed connections for non-variable digits) form this matrix. The matrix is arranged in 24 rows and 37 columns (see SD-67720). Each resistor has one end tied to a digit line (24 resistors/digit line) and the other end tied to the common terminal of a switch. One side of each switch, the zero position, (N.C.) is tied to ground. The other side, the ONE position, (N.O.) is tied to a resistor driver (37 resistors/driver). One resistor from each digit line goes to each resistor driver.

The resistor driver of the register to be observed is selected by a -3 volt level on one of three lines and a ground level on one of eight lines. These levels are obtained via cascodes from the central computer. The output of the selected resistor driver swings from ground to -25 volts. All unselected resistor drivers are held at ground.

Those resistors that are tied to switches set in the ONE position are connected to resistor drivers. They drive their digit lines to -1 volt. Hence, a -1 volt signal on a digit line means that the appropriate digit of the selected register is a ONE.

The digit line signal is detected, amplified to a standard level, and inverted in a digit detector unit. The digit detector in turn drives a cable driver that transfers the information to the central computer, where it is strobed and used.

(3) Resistor Driver (see figure 1, also ref. to D-82581)

The T.S.S. resistor driver is a 4 transistor amplifier. It is driven by a -3 volt level at the base and a ground level at the emitter of its input transistor (Q_1).

In this condition Q_1 will be on, Q_2 and Q_3 off, and the -150 volt supply will drive the emitter follower Q_4 through an external 9K resistor. The amplifier in this state will put out a -25 volt level capable of driving the 125 ma. (worst case) drawn by the resistor matrix.

The -25 volt output level was chosen because of the 2N123 breakdown voltage. When Q_3 is off, its collector is clamped to the Q_4 collector supply voltage by the collector diode of Q_4. Since the base of Q_3 is at -5 volts, and its collector-to-base breakdown is 20 volts, the Q_4 supply is restricted to -25 volts.

When Q_1 is not turned on by the -3 and ground input levels, Q_2 and Q_3 are on, putting the base of Q_4 at a nominal ground (-0.2 to -0.4 due to transistor drop). Hence, the output will be at a nominal ground (-0.0 to -0.3 approximately). In this state the amplifier can drive a 6 ma. load, sufficient to meet worst case conditions and pull up the output of Q_4.

The bases of Q_1 and Q_2 are returned through resistors

to a nominal +10 volt marginal checking bias voltage. Increasing this voltage tends to supply a greater turnoff current to both Q_1 and Q_2. When Q_1 is turned on this bias increase acts to reduce the effective gain of Q_1. This effect is partially compensated for by the simultaneous increase in Q_2 turnoff current. However, a low gain transistor in the Q_1 position would be detected. When Q_1 is turned off, increasing the marginal checking bias voltage will show up weaknesses in the rest of the circuit (Q_2, Q_3, Q_4). Decreasing the M.C. bias voltage will show up excessive leakage currents and excessive hole storage time delays which may cause timing problems.

Q_4 may also be marginal checked by varying the -150 supply voltage. Decreasing this voltage decreases the turn-on current of this transistor and will show up a low Beta WA-52830..

Marginal checking of the T.S.S. resistor drivers indicate that the nominal 10 volt bias may be increased to above +40 volts without harmful effects on operation. The bias may also be decreased to +3 volts before the unit rise time increases to 1.5 μsec.

The maximum normal (M.C. voltage = +10) transition time of the resistor driver is 1 μsec.

There are two T.S.S. resistor driver circuits in the T.S.S. resistor driver P.I.U. However, an external 9K (two 18K, 2W resistors in parallel) resistor going from the base of Q_4 to an external -150 volt supply must be used in conjunction with the package. This resistor could not be included in the package because of its high heat dissipation (2w).

(4) Digit Detector (see figure 2, also ref. to D-82557)

When connected in the T.S.S. system the input of the digit detector is tied to 24 resistors, as shown in Fig. 3a. Twenty-three of these resistors are always tied to ground, either directly to a ground bus or to the ground held by an unselected resistor driver. The 24th

resistor is returned to the -25 volt output of the selected resistor driver when the digit under consideration of the selected register is a ONE.

The Thevenin equivalent of the digit detector input network is a -1.04 volt signal through a 312 ohm resistor as shown in Fig. 3b.

The T.S.S. digit detector is a single L-5122 inverter. The input signal of the detector is D.C. coupled to the inverter base through a germanium stabistor voltage-dropping diode (Transitron TS320G). This diode has a 0.3 volt drop across it. The function of the diode is to prevent a group of resistor drivers, each a few tenths of a volt negative (as described in (3)), from causing a false "ONE" indication.

The D.C. gain characteristic of the T.S.S. digit detector is shown in Fig. 4. It should be noticed that, as desired, it has no response to a small negative signal (below 0.4 volt) and will saturate at -0.8 volt.

The base of the L-5122 is returned to a nominal +10 marginal checking bias voltage. As this voltage is decreased, less turnoff current is supplied to the L-5122 base. This increases the turnoff time of the transistor.

To marginal check the L-5122 gain, it was felt desirable to decrease the -30 volt supply rather than to increase the +10 volt supply, as is usually done. This is due to the input network of the L-5122. When the TS-320-G drop is exceeded, the bias supply tends to drive the low impedance looking back into the resistor matrix, rather than providing turnoff current for the L-5122.

When the T.S.S. -30 volt supply is decreased, the nominal -25 volt resistor driver supply derived from it is proportionately decreased. This decreases the matrix drive and hence the input signal to the digit detectors.

Marginal checking of the T.S.S. digit detectors indicates that decreasing the M.C. bias from +10 volts to 0 volt increases the fall time to about 1.5 μsec (it may initially be as high as 0.5 μsec). This seemingly long fall time is partially compensated for by the digit output cable drivers. Their output rises to full value before the digit detectors have completed their slow fall. In a typical case the 1.5 μsec delay is reduced to 0.8 μsec at the cable driver output. Marginal checking by reducing the -30 volt supply indicates that it may be reduced to -23 volts, in the worst case, before any appreciable degeneration of the digit detector ground level occurs.

Six digit detector circuits are included in each T.S.S. digit detector P.I.U.

(5) -25 Volt Power Unit (ref. to D-82691)

As shown in (3) a maximum value for the resistor driver output supply voltage is -25 volts. A voltage near or at this maximum is needed to supply sufficient drive to the T.S.S. resistor matrix. Since there is no such standard TX-2 voltage, it is necessary to generate a -25 volt supply voltage.

The -25 volt power unit contains a resistor-divider across the TX-2 -30 volt supply, which puts -25 volts into an H6 emitter-follower having a -30 volt collector supply. Hence, a -25 volt supply referenced to the TX-2 -30 volt supply is produced.

(6) Construction (See Figures 5 and 6)

The TX-2 main toggle switch board contains sixteen toggle switch registers arranged in horizontal columns in groups of four. The registers are numbered in the octal number system from 0 through 17. The registers consist of 37 digits (vertical columns) broken into groups of 3, 9, and 18 with the leftmost bit (marker bit) separated from the other 36 bits. The digits are numbered 1.1 - 1.9, 2.1 - 2.9, 3.1 - 3.9, 4.1 - 4.10.

Each bit position is a toggle switch. A modified Minneapolis-Honeywell Microswitch Division 6AT1 switch is used (#6AT56-T2). This switch differs from the 6AT1 in that it has turret lug connections and gold plated contacts.

The N.O. and the N.C. connections of each register (row of switches) are each tied together forming two busses per register. The N.C. bus lines are tied to ground and the N.O. bus lines are tied to a resistor driver.

The common connection of each switch is tied to a 7.5K resistor. Resistors common to each digit (column of switches) are tied together with a bus wire supported by terminal blocks at the top and bottom of the toggle switch board. Each of these thirty-seven busses (digit lines) are tied to a digit detector.

The resistor drivers, digit detectors, power unit, cascodes, and input-output plugs for the T.S.S. are mounted on a hinged panel on the back of the toggle switch board. Thus, the wiring of the panel is accessible when the hinged panel is opened.

Attachments:

Figure 1, Dwg. No. A-86703
Figure 2, Dwg. No. A-86704
Figure 3, Dwg. No. A-86645
Figure 4, Dwg. No. A-86517
Figure 5, Dwg. No. A-86646
Figure 6, Dwg. No. A-86647

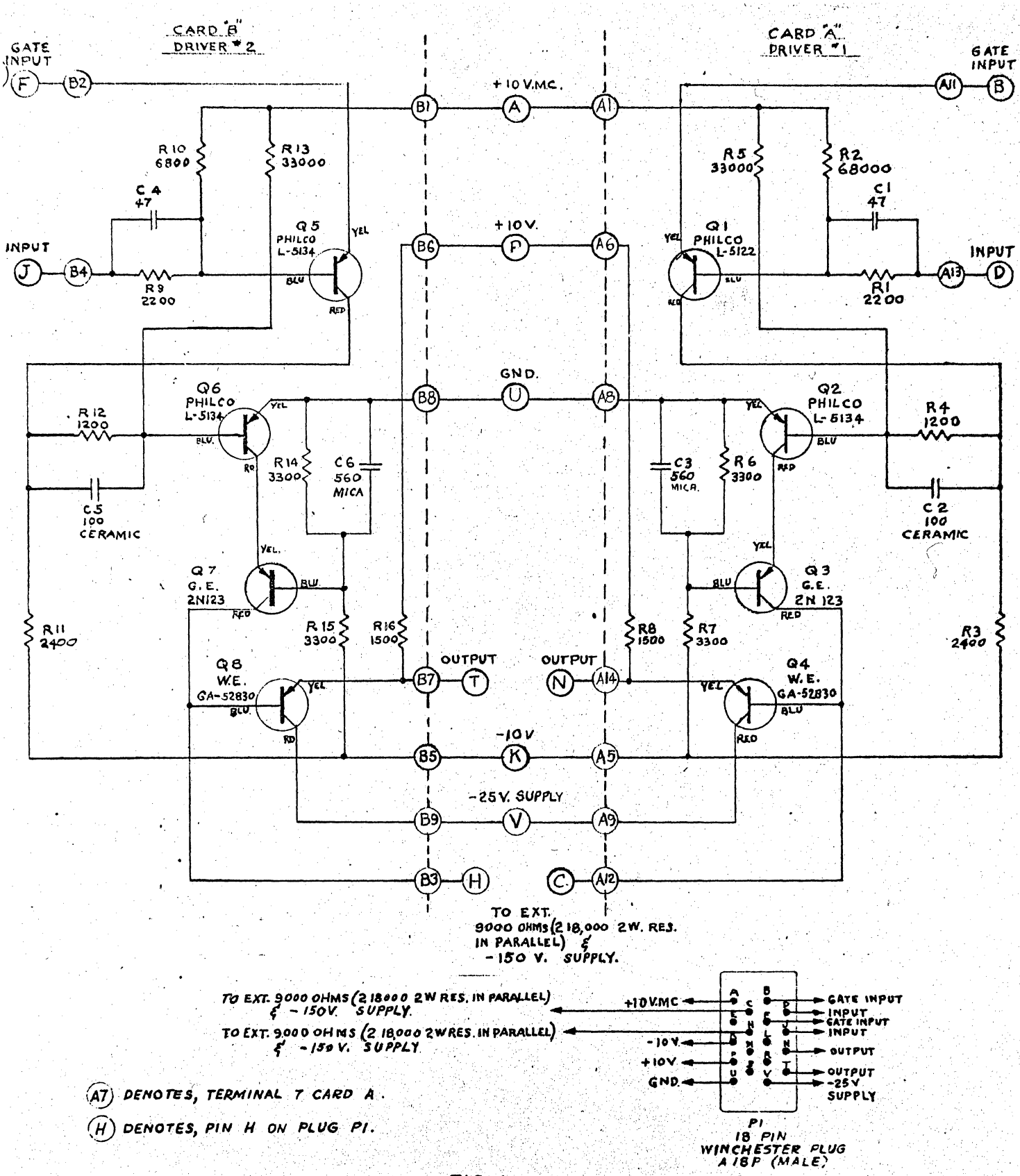
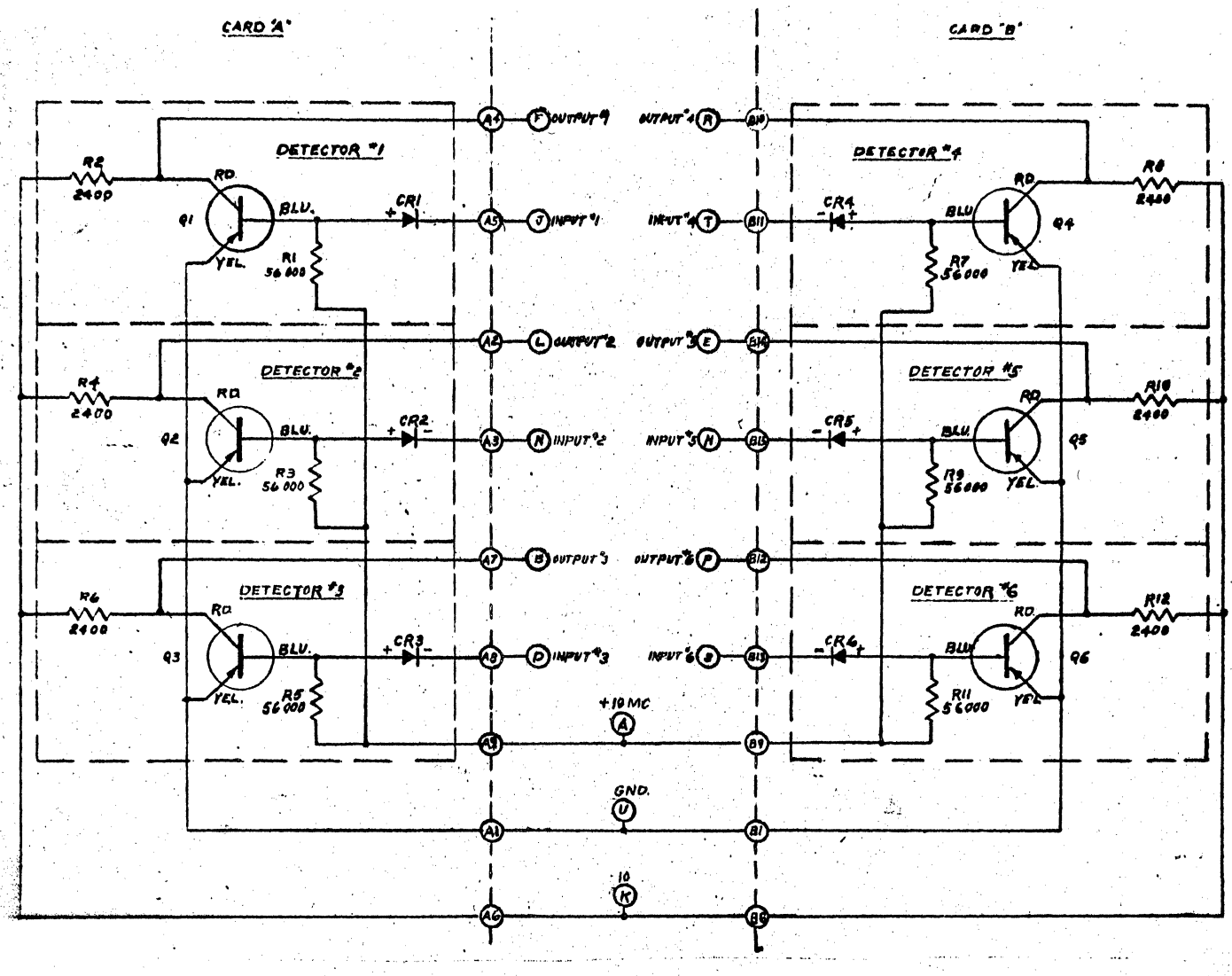
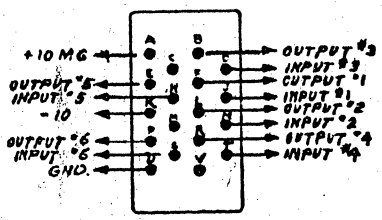


FIG. 1

CIRCUIT SCHEMATIC, P. I. U. TOGGLE SWITCH STORAGE RESISTOR DRIVER, TX-2

A-6805





P1
18 PIN
WINCHESTER PLUG
A 18 P (MALE)

(A7) DENOTES, TERMINAL 7 CARD A.

(H) DENOTES, PIN H ON PLUG P1.

FIG. 2

CIRCUIT SCHEMATIC, P.I.U. TOGGLE SWITCH STORAGE DIGIT DETECTOR, TX-2

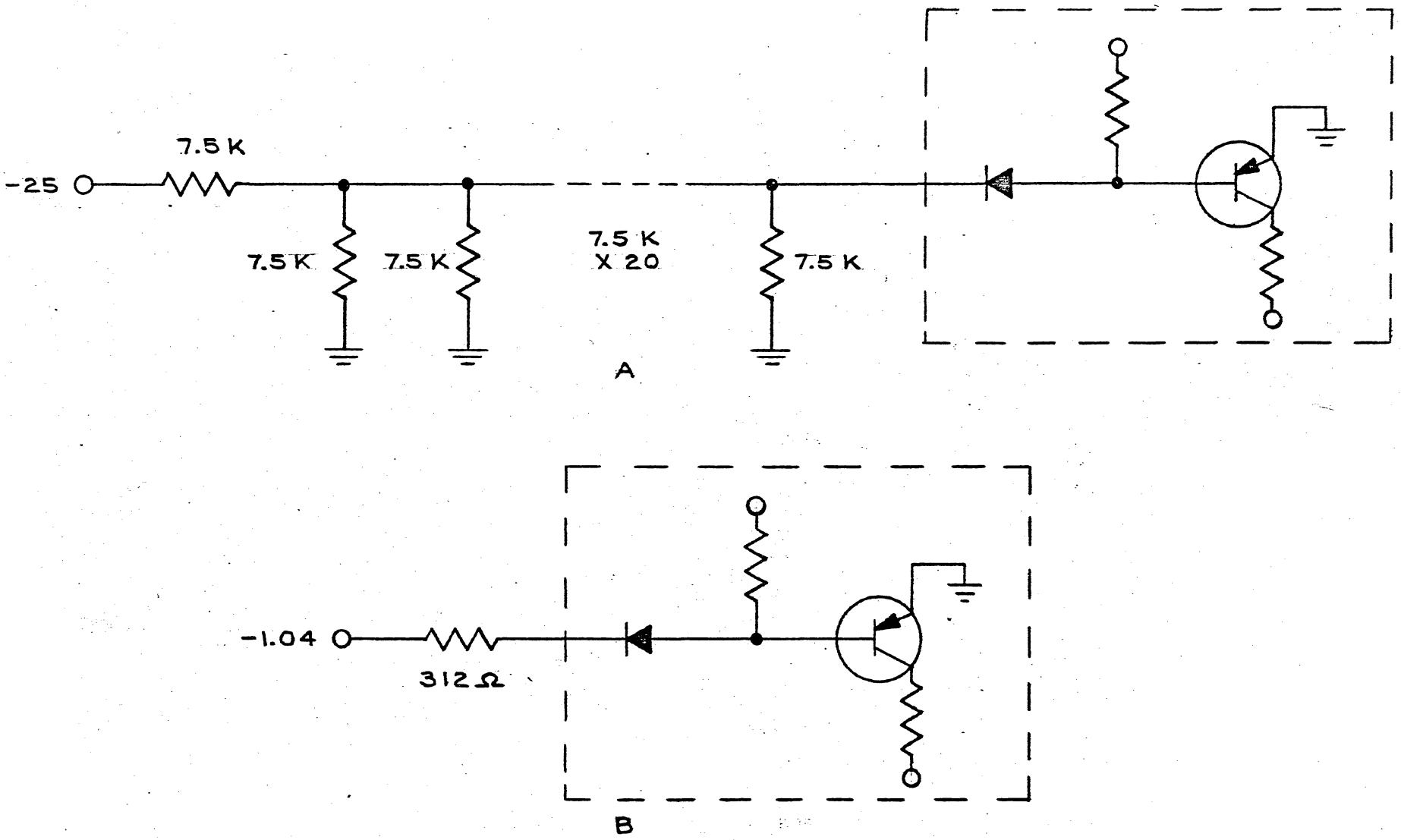


FIG. 3

EQUIVALENT INPUT NETWORK - T.S.S. DIGIT DETECTOR

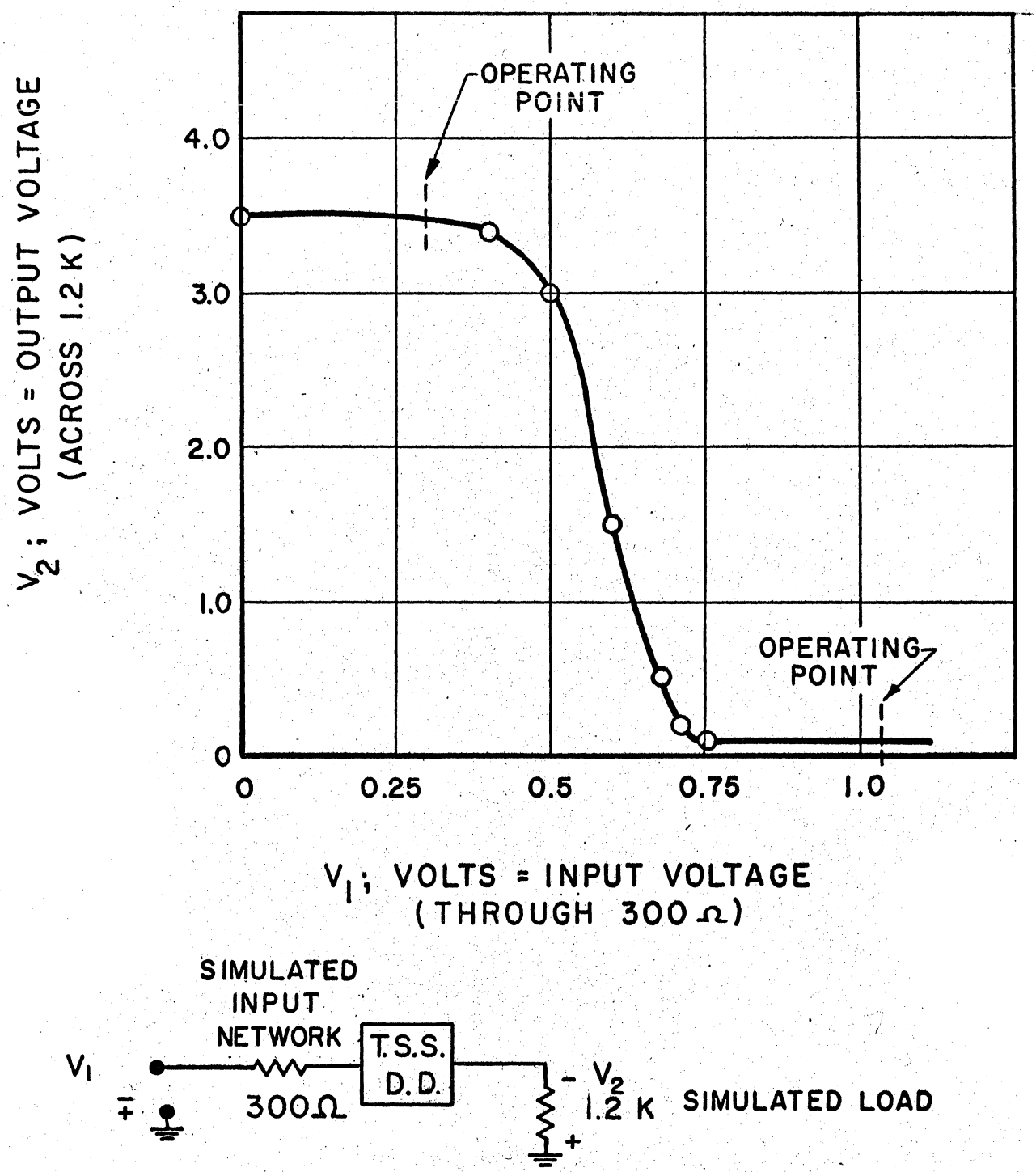


FIG. 4

T.S.S. DIGIT DETECTOR;
D.C. GAIN CHARACTERISTIC

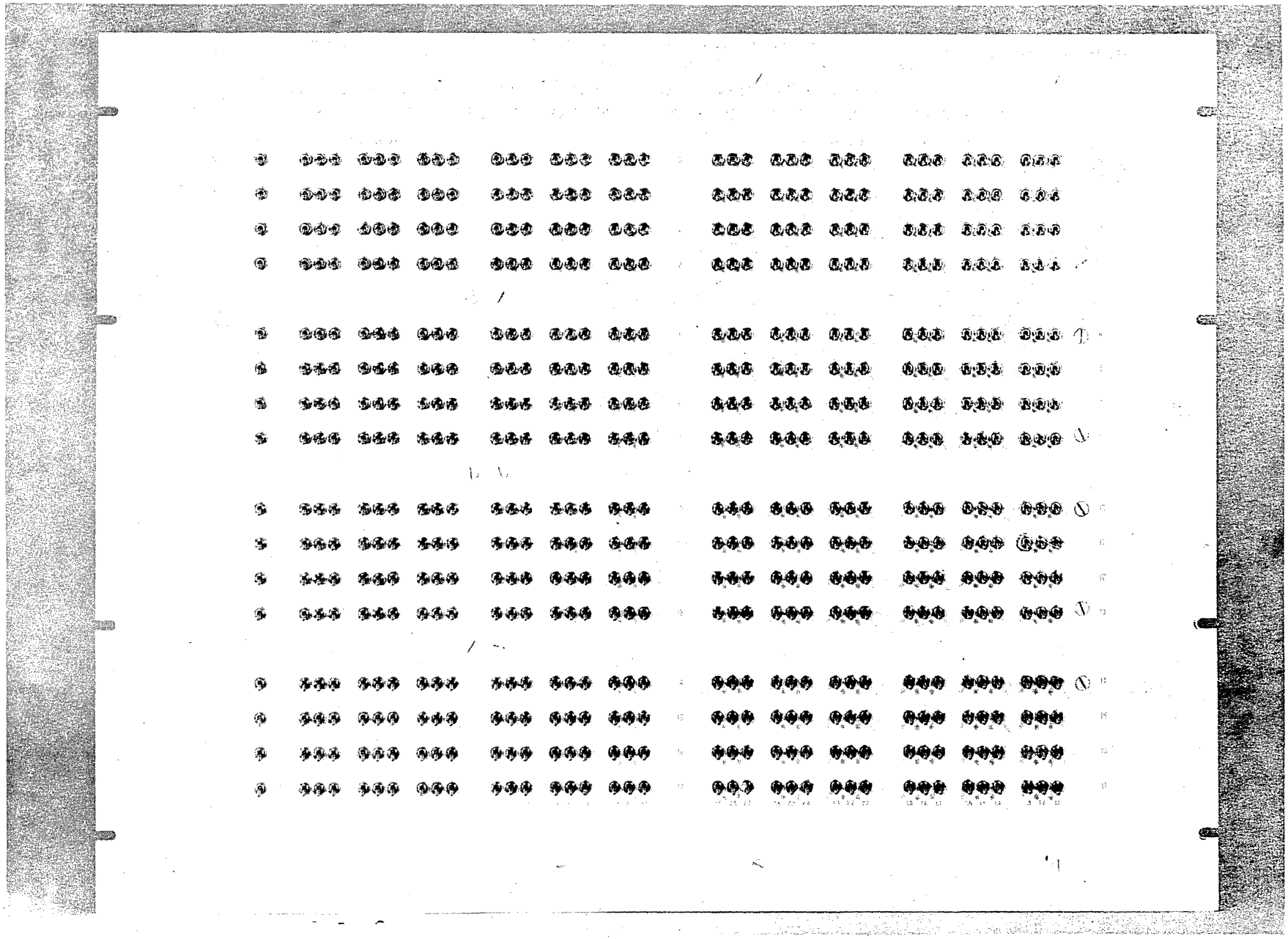


FIG. 5

TOGGLE SWITCH STORAGE SYSTEM, MAIN PANEL FRONT VIEW

A-86647

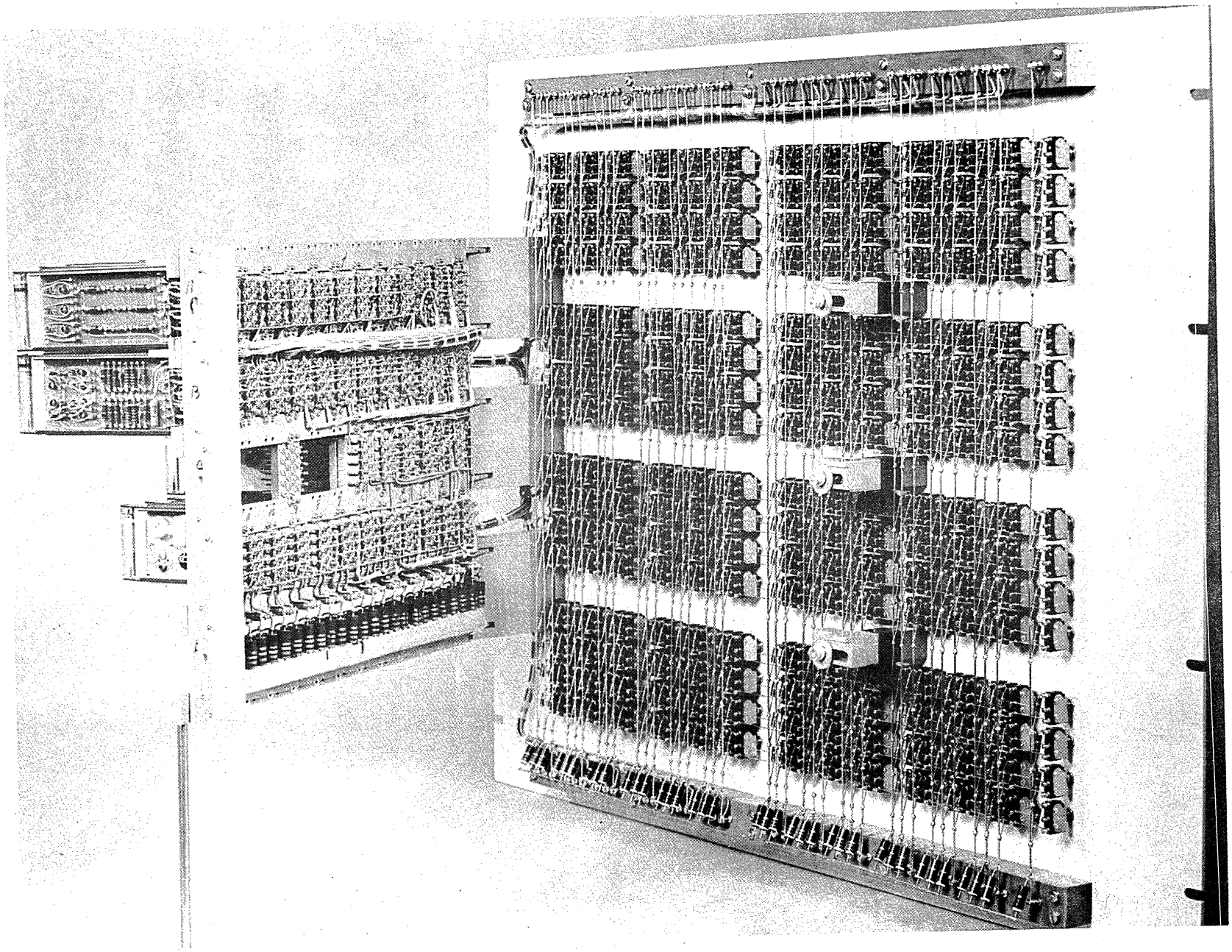


FIG. 6 TOGGLE SWITCH STORAGE SYSTEM, MAIN PANEL BACK VIEW. HINGED BACK IS SHOWN OPEN EXPOSING WIRING. (NOTE TEMPORARY RESISTORS ON THE BOTTOM OF THE T.S.S. PANEL. THEY SIMULATE THE 8 SEMI-FIXED REGISTERS THAT ARE NOT INCLUDED ON THE MAIN PANEL.)