technical manual
PERIPHERAL CONTROLLERS
volume I

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PERIPHERAL CONTROLLERS

TECHNICAL MANUAL

VOLUME I

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I. GENERAL I/O SYSTEM DESCRIPTION

INTRODUCTION

MODCOMP computer systems are designed to be very flexible in input/output and peripheral device configurations. The basic computer enclosure contains the register I/O subsystem and I/O cable driver/receiver module capable of driving up to 100 feet of I/O cable in the MODCOMP II and III, and up to 50 feet in the MODCOMP I. The I/O cable may be connected to up to eight other cable driver/receiver loads. The Direct Memory Processor (DMP), and the controllers for the console TTY and high-speed paper tape reader are also contained in the basic computer enclosure when those options are included in the system.

Input/Output options not contained within the computer enclosure and representative peripheral devices and controllers are shown in Figure 1-1, the Peripheral Device Configurator. As can be seen by the configurator, several I/O schemes are possible using the Modular approach. A brief description follows:

TTY & CHALCO

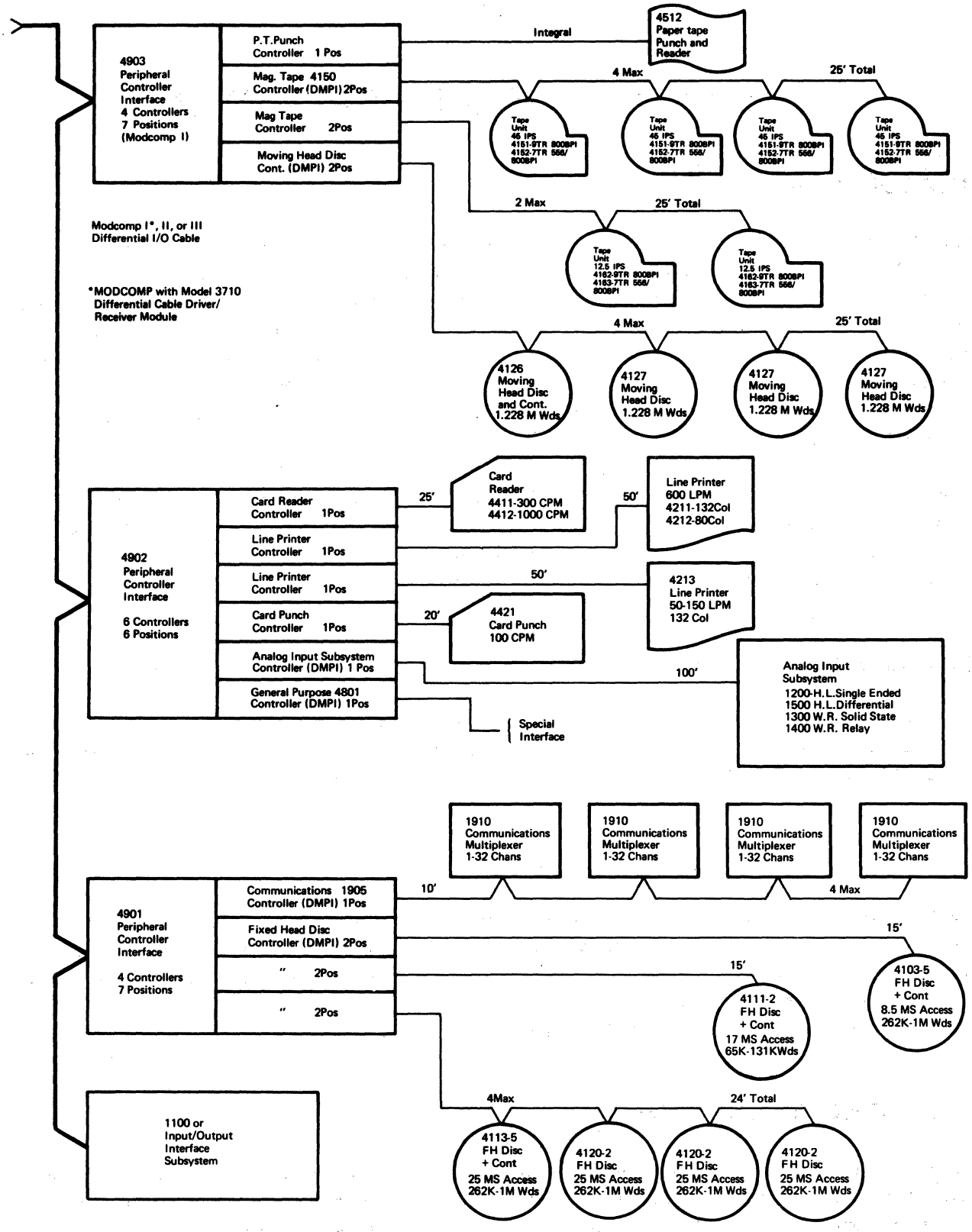
The console teletypewriter and high-speed paper tape reader share a controller located and directly connected within the computer enclosure. This optional controller is in addition to the eight driver/receiver loads mentioned above.

AIS

The Modular Analog Input Subsystems are specifically designed for use in computer based measurement and control applications. They provide the capability for highly flexible analog input signal multiplexing when used with the MODCOMP computer family. The four basic subsystems are High-Level, High-Level Differential and two Wide-Range versions. Each AIS requires a half plane, or one controller position in the PCI.

DIRECT MEMORY PROCESSOR

The DMP option is mounted on Plane 4 of the computer when it is included in the system. Peripheral device controllers which have high transfer rates may be connected to the optional DMP to reduce the amount of program involvement in I/O transfers. A DMP interface is included in the controllers for discs, magnetic tape units, solid-state analog input subsystems, and many communication and custom interface units. No special placement or cabling is required for controllers connected to the DMP.



Peripheral Device Configurator

PERIPHERAL CONTROLLER INTERFACE

The optional Peripheral Controller Interface (PCI) is a separate enclosure which provides a convenient means to interface the single I/O bus cable from the CPU with up to eight additional device controllers through a Driver/Receiver module(s).

Peripherals, except for the directly connected console TTY and high-speed paper tape reader are connected to the computer by means of individual controllers packaged in the PCI enclosure. The PCI contains I/O bus and DMP interfaces plus the power supplies required by the controllers. Multiple PCI enclosures may be connected to one computer, enabling many combinations of peripherals to be used in a system. The controllers which may be housed in the PCI enclosure are:

Card Reader
Paper Tape Punch
Line Printer
Fixed Head Disc
Moving Head Disc
General Purpose Controller
Magnetic Tape
Analog Input Subsystem(s)

PERIPHERAL DEVICE CABLES

Most of the peripheral devices are directly connected to individual controllers located in the Peripheral Controller Interface enclosure by peripheral device cables. Some of the peripherals, however, share a device controller. Others contain their own device controller and connect directly to the I/O cable.

Magnetic Tape Units, up to a total of four, are "daisy-chained" to a magnetic tape controller.

The standard maximum length of each peripheral device cable is shown in the configurator, Figure 1-1.

SUMMARY

An overview of possible I/O configuration has been given. The remainder of this manual deals with the Peripheral Controller Interface and associated controllers discussed earlier, with the exception of the Analog Input Subsystems which are described in separate manuals.

II. PERIPHERAL CONTROLLER INTERFACE UNIT

PHYSICAL DESCRIPTION

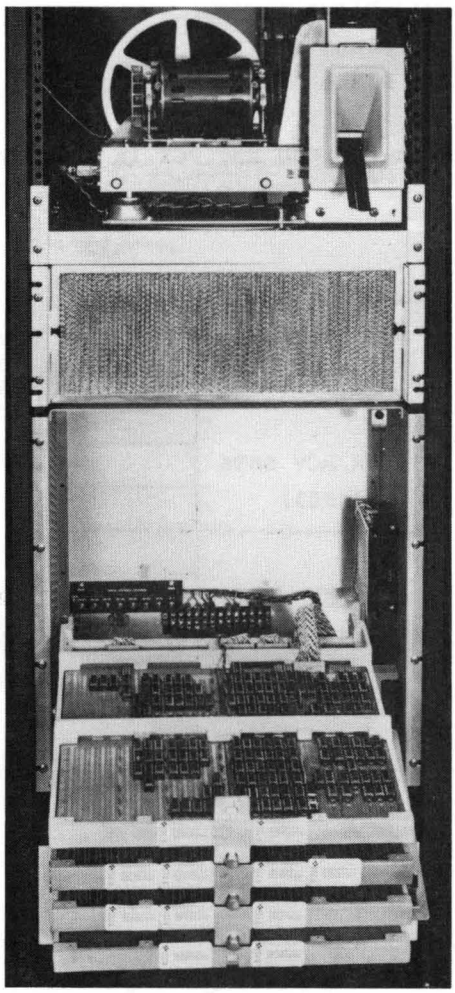


FIGURE 2-7

The Peripheral Controller Interface enclosure is shown here mounted in a cabinet below the standard power supply enclosure (covered by air filter) provided with the PCI. At the top of the cabinet is the highspeed paper tape punch mechanism. All planes in the PCI are hinged to provide convenient access to logic components and I/O cable connectors. The disc write lockout switches, a terminal block and cooling fan can be seen within the PCI enclosure.

The Peripheral Controller Interface (PCI) is a rack mountable enclosure with the same physical dimensions as the MODCOMP III computer enclosure. Depending on the system configuration, it may be mounted in the same rack with the computer enclosure or in a separate standard 19 inch cabinet (MCS Model No. 0001). Four hinged planes may be mounted within the enclosure. Each controller is mounted on one-half of one of the planes, except for the magnetic tape and the disc controllers, which require a full plane each. A driver/receiver module capable of connecting four controllers to the I/O cable occupies one-half of plane 1 in the Model 4901 PCI. A second driver/receiver module occupies the other half of plane 1 in the Model 4902 PCI.

A separate enclosure with space for up to three power supplies is also provided with the PCI enclosure. One logic supply (±5V) is included as standard.

Figure 2-1 is a front view of a Peripheral Controller Interface (Model 4902) enclosure with all four planes tilted out.

The PCI has the capability to interface the CPU with the following controllers:

General Purpose Controller	1/2 Plane
Paper Tape Punch Controller	1/2 Plane
Card Reader Controller	1/2 Plane
Line Printer Controller	1/2 Plane
Fixed Head Disc Controller	Full Plane
Moving Head Disc Controller	Full Plane
Magnetic Tape Controller	Full Plane
High Level Analog Input System Controller	1/2 Plane
Wide Range Analog Input System Controller	1/2 Plane

A functional block diagram of the interface between the CPU and PCI is illustrated in Figure 2-2.

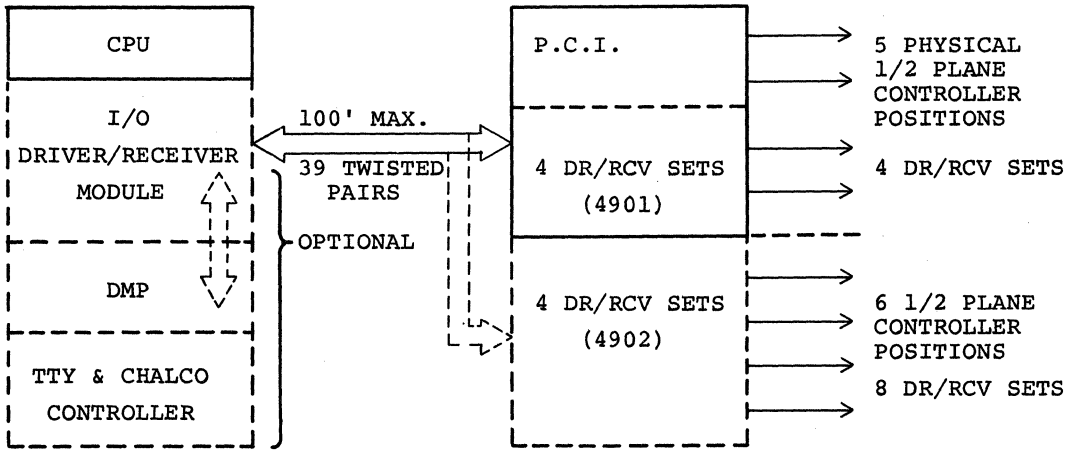


FIGURE 2-2 PCI/CPU INTERFACE
FUNCTIONAL BLOCK DIAGRAM

Standard plane numbering and coordinates, including the 26 pin 3M I/O connector locations are illustrated in Figure 2-3.

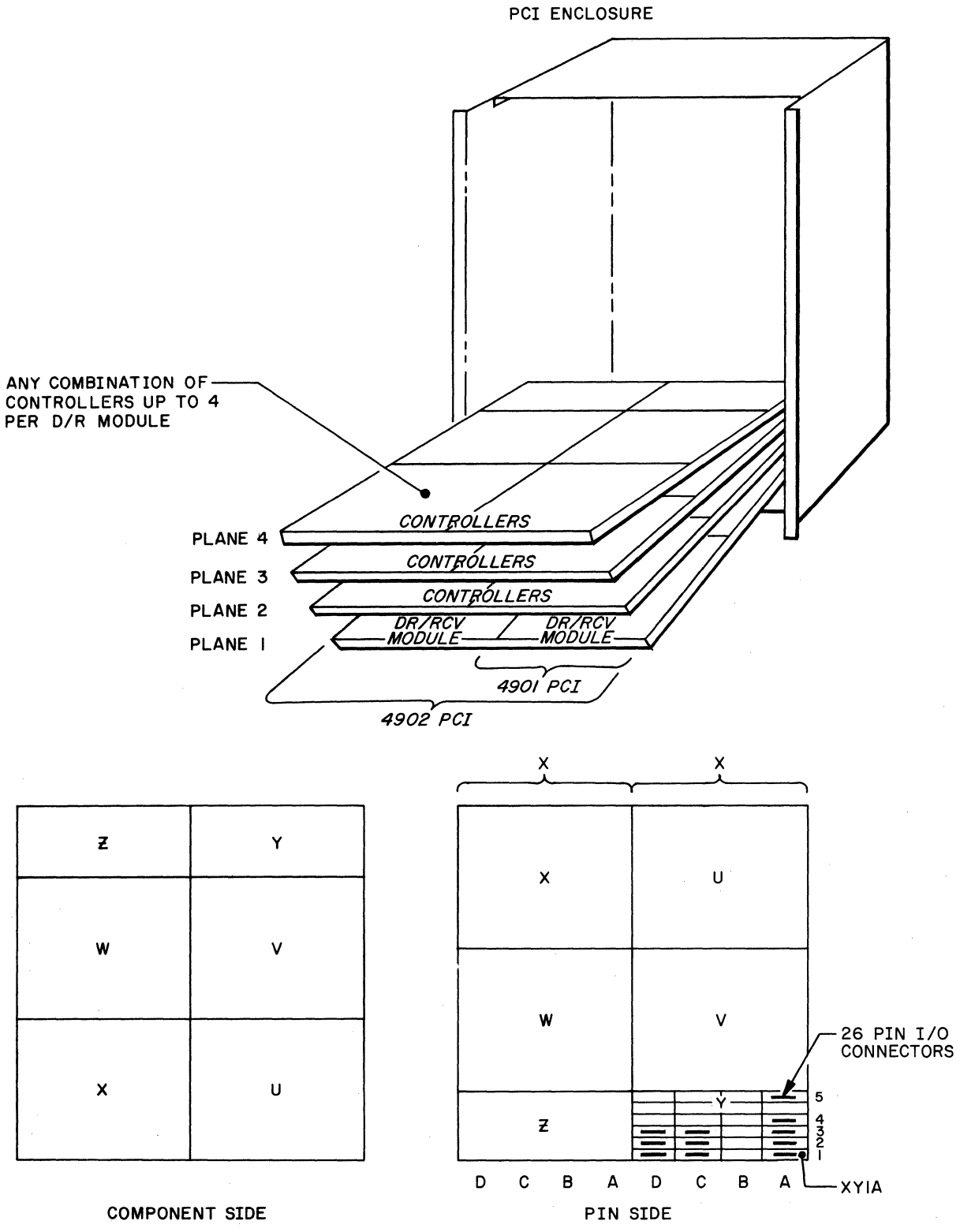
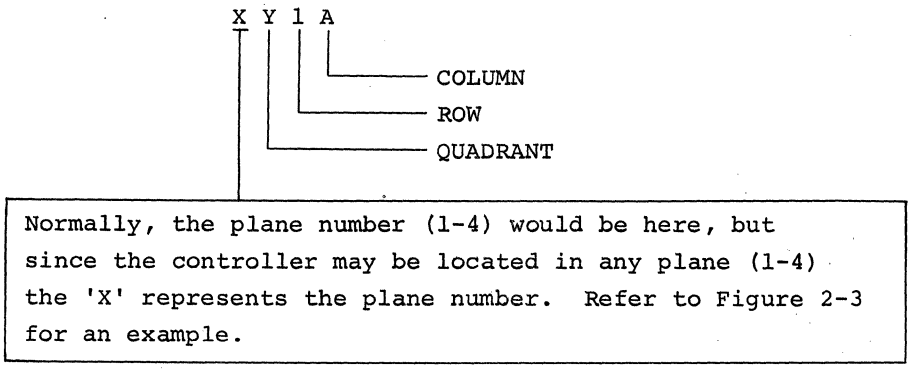


FIGURE 2-3 PLANE NUMBERING AND COORDINATES

It should be noted that half plane controllers use "U", V" and "Y" signal designations even though the controller could be on either half of the plane. This was done for uniformity of logical signal designations. Full plane controllers (discs, mag tape) use U, V, Y and X, W, Z designations.

It should also be noted that an 'X' prefix to signals is used which is not to be confused with sector 'X' of the full plane. For example:



Although the Driver/Receiver module(s) always occupy Plane 1, the above signal designations apply.

The following figure illustrates all possible combinations of half and full plane controllers for both the 4901 and 4902 Peripheral Controller Interface units.

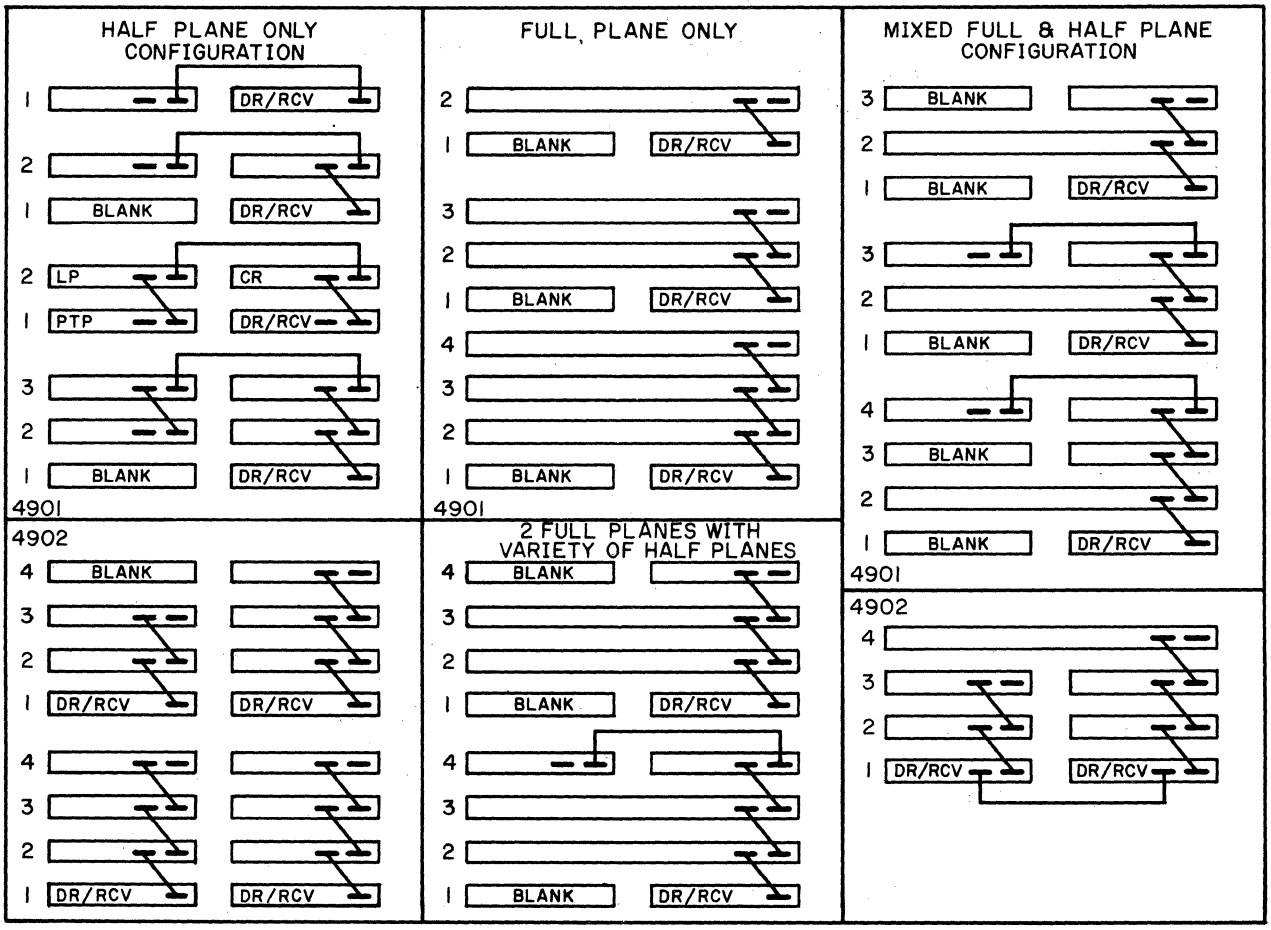


FIGURE 2-4 PERIPHERAL CONTROLLER CONFIGURATOR

I/O CABLE CONNECTIONS

The following illustrations describe the I/O Connector Panel layout and a functional diagram of the I/O bus interconnection from the CPU to the PCI.

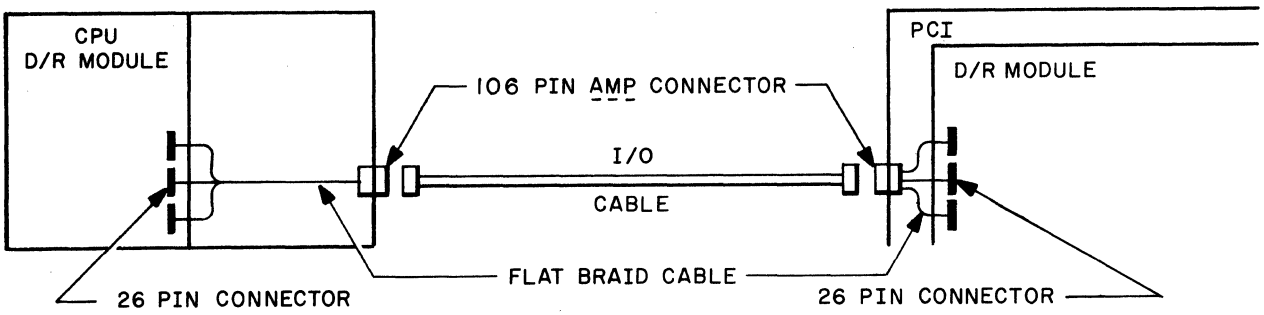


FIGURE 2-5 I/O BUS INTERCONNECTION DIAGRAM

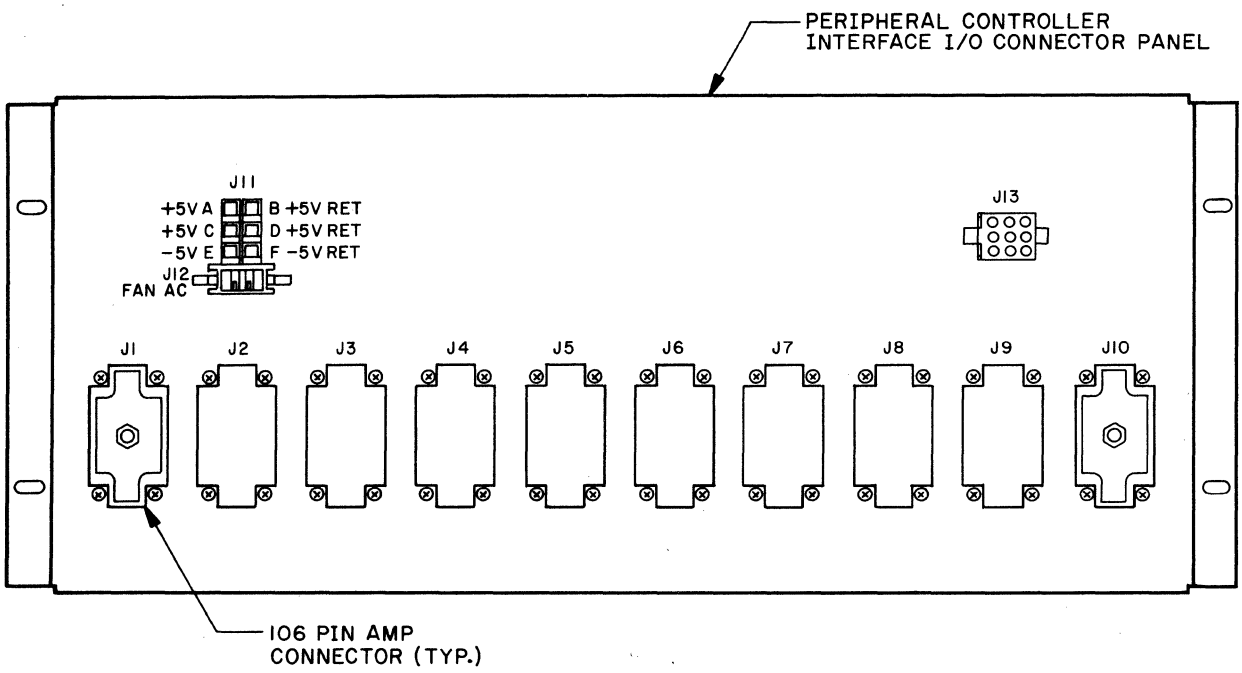


FIGURE 2-6 PCI I/O CONNECTOR PANEL

POWER SUPPLY

The standard ±5 volt power supply provided with the PCI is described below.

The +5 and -5 volt regulators are located on schematic and wiring drawings 526-100000 and 525-100000, respectively. Transformer T1 supplies the high current a.c. for the +5 volt and -5 volt regulators. Its center-tapped secondary is full wave rectified both positively and negatively, and both rectifiers are capacitively filtered. Refer to Figure 2-7.

+5 Volt Regulator - The +5 volt regulator consists of parallel NPN series pass transistors, Q3-Q9, an emitter follower driver, Q2, and a monolithic voltage regulator, IC2. +Vcc for IC2 is generated by a voltage doubler consisting of diodes, CR4-CR7, and capacitors, C4-C6. The +5 volt output is sensed at pin 4, the inverting input of the error amplifier,and compared with a reference voltage established at pin 5, the non-inverting input. The error amplifier output is amplified by Q2 to provide sufficient current to drive the pass transistors. The current foldback knee is adjustable with R19, which is nominally set for a maximum of 35 amperes at 5 volts. Folded back short-circuit current is approximately 23 amperes. Over-voltage protection is provided by a "crowbar" circuit consisting of Q3, CR8, and CR3. CR8 establishes a reference voltage of 5.6 volts on the base of Q3. Should the output voltage ever exceed 6 volts, Q3 will turn on CR3, instantaneously dropping the output to zero and opening fuse, F1.

-5 Volt Regulator - The -5 volt regulator consists of a PNP series pass transistor, an emitter follower driver and monolithic voltage regulator, IC1. -5 volt sensing is accomplished by means of a balanced bridge which quiescently maintains a zero volt differential between pins 5 and 4, the inverting and non-inverting inputs, respectively, of the error amplifier. Any change in the -5 volt output unbalances the bridge, producing an error output signal at pin 10. This error signal is amplified by an emitter follower to provide sufficient current to drive the pass transistor. An over-current condition is sensed between the emitter and base of Q2, causing the current to fold back to approximately 3.7 amperes when the output is directly shorted.

Voltage Adjustments

+5 Volts - This voltage should be set to +5.0 volts ±.05 volts by means of trimpot R13 in the power supply.

-5 Volts - This voltage should be set to -5.0±.05 volts by means of trimpot R9 in the power supply.

CAUTION

1. ±5 volt supply - if uncabled from system, external sensing pins must be jumpered to maintain regulation. Refer to drawings 525-100000 and 550-100000.
   Jumpers are: J1-7 to J3-1 (-5 Volts)
   J1-9 to J3-3 (+5 Volts)
2. All input fuses are high-speed fuses. SLO-BLOW fuses will cause damage to the power supply or PCI logic in the event of crowbar shutdown.
3. Use a 1% meter for adjusting voltages.
4. Over-current adjustments are factory set and should not be tampered with.

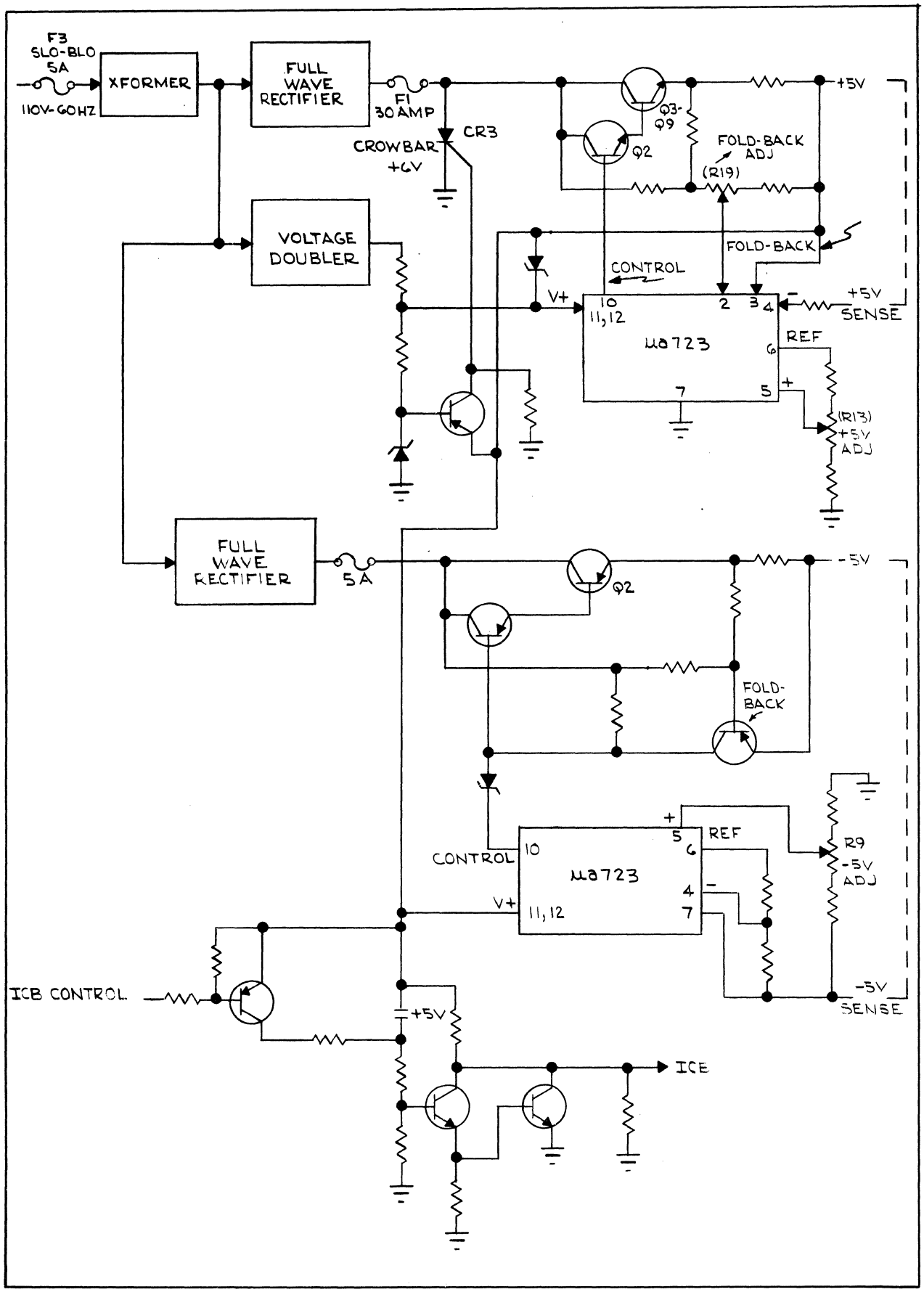


FIGURE 2-7 ±5V POWER SUPPLY FUNCTIONAL DIAGRAM

DRIVER/RECEIVER MODULE

The driver/receiver module occupies one half of plane one in the Model 4901 PCI and a second driver/receiver module occupies the other half of plane one in the Model 4902 PCI. Figure 2-8 is an illustration of the standard half plane driver/receiver module. Refer to Logic Drawings 516-100018 and 515-100018(1-3) for details of the DR/RCV module.

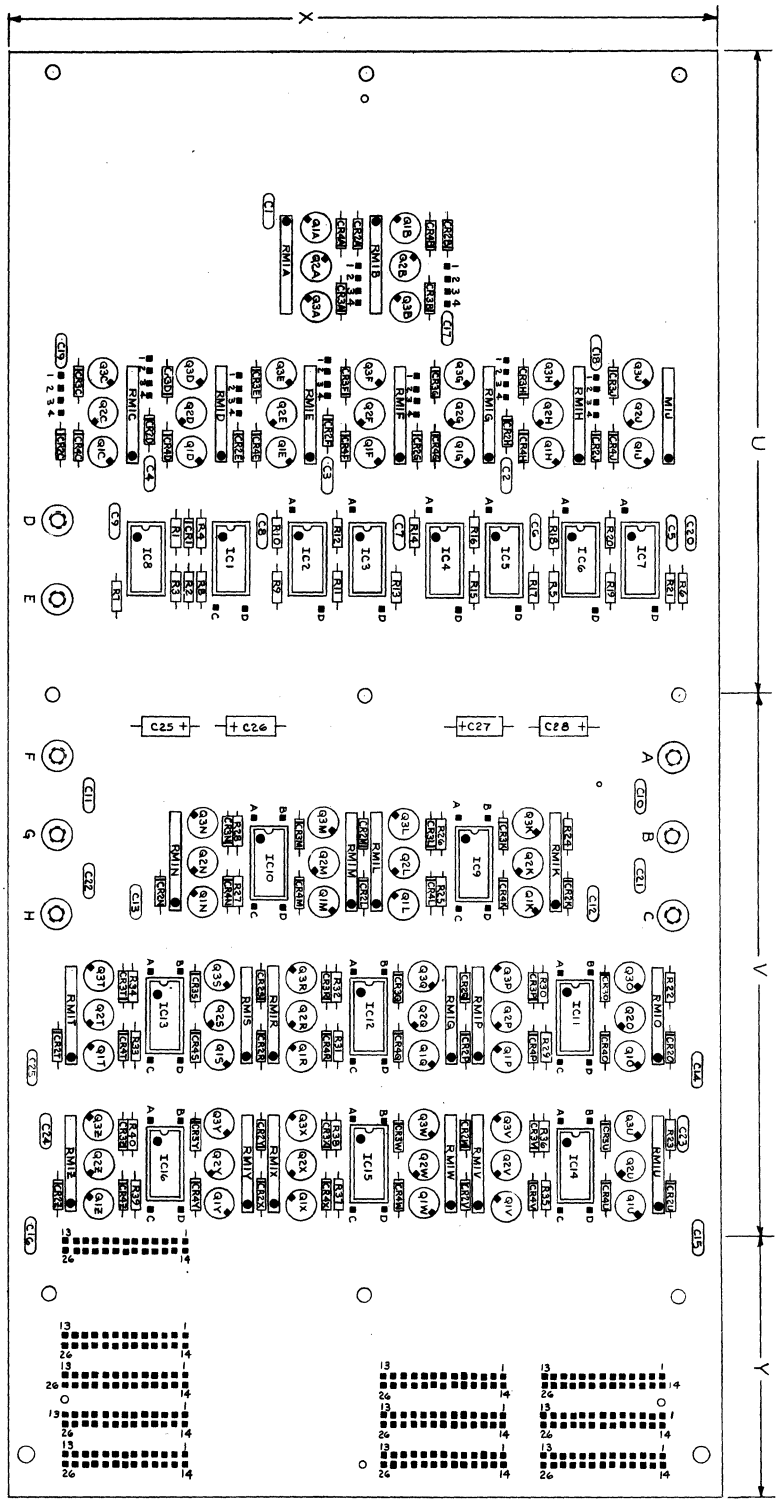


FIGURE 2-8 DRIVER/RECEIVER MODULE

CABLE DRIVER

General

The cable drivers, -001 and -002, are intended to drive twisted pair cables which are terminated at both extremities in their characteristic impedance. In addition to driving the line differentially, the driver may be paralleled or "OR'ED" at any location on the cable. In this configuration, common mode noise between these distributed locations of up to ±3 volts peak will not interfere with signal transmission on the cable.

Functional Description

Speed: 5 MHz, Max.

Function Input Requirements:

Amplitude: Logic "1": 0.4V, Max.

Logic "0": 3.0V, Min.

Input Load Current: Ein = 0.4V; $Iin_{(1)}$ = 18 Ma.

Ein = 3.0V; $Iin_{(0)}$ = 7.5 Ma.

Ein = 5.0V; $Iin_{(0)}$ = ±0.8 Ma.

Input Rise and Fall Times: Tr = Tf = 5 ns for output specifications stated

Output Specifications (Terminated Per Figure 2-6)

Amplitude Ein = 0.4V; Output = +12 ± 2 Ma.

$\overline{\text{Output}}$ = 12 ± 2 Ma.

Ein = 3.0V; Output = +10 ua, Max.

$\overline{\text{Output}}$ = 10 ua, Max.

Risetime: 7 ns, Min., 20 ns, Max.

Falltime (Either Output): 7 ns, Min., 25 ns, Max.

Propagation Delay (Either Output): Logic "1": 5 ns, Min., 10 ns, Max.

Logic "0": 5 ns, Min., 10 ns, Max.

Voltage Compliance: -001: ±3.75 VDC or Peak AC, Max.
(Either Output To GND) -002: ±3.0 VDC or Peak AC, Max.

Environmental Conditions:

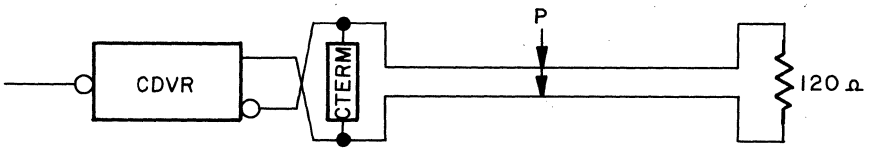
Operating Temperature Range: 0°C to 70°C

Power Requirements: +5V ±5%, 28 Ma, Max.

-5V ±5%, 26 Ma, Max.

Theory of Operation

In operation, signals applied to the line are received by MCS Part Number 640-100020 differential line receivers. Thresholds for this receiver are +25 MV and -25 MV for logic 1 and logic 0 outputs respectively. To provide bias in excess of threshold when the drivers are in "0" state (zero output current) the line termination network shown below is employed (See Next section, Receivers).



Refer to Figure 2-10 The impedance seen by the line at the driven end is $R_2 + R_3$ in parallel with $R_1 + R_4$, which is equal to R_0. R_0 is equal to Z_0, the characteristic impedance of the cable. The current through the total network (with zero driver current) is normally 6 ma., providing a balanced (with respect to driver signal common) bias across the line. A logic "1" input to the driver causes the outputs to deliver a nominal 12 ma. current opposing the bias. This results in a reversal of the voltage across the line equal in magnitude to the original bias and balanced with respect to driver signal common.

When the driver input is positive, transistor Q_2 emitter voltage is slightly below +Vcc in level. The resulting voltages across R_2 and R_4 are insufficient in magnitude to overcome the base-emitter voltage thresholds of Q_1 and Q_3 respectively. Q_1 and Q_3 are therefore in cutoff and no collector currents flow. When the input voltage goes negative (0 to +0.4V), Q_2 emitter is pulled down to a level near zero volts with respect to signal common. The resulting voltage across R_2 exceeds Q_1 base-emitter threshold, and the remainder across R_5 generates an emitter current of 12 ma., nominally. Since the common base current gain (h_{FB}) of Q_2 is nearly unity, the collector current of Q_2 (h_{FB})is nearly unity, Q_1 collector current is very nearly equal to its emitter current. The resulting voltage levels across R_4 and R6 respectively are nearly equal to those across R_2 and R_5 respectively. h_{FB} of Q_3 is nearly unity so that approximately -12 ma of collector current will flow, regardless of collector voltage (within limits specified).

The 002 version of the circuit includes a pair of diodes (CR3, CR4) connected in series with the outputs. This circuit is used when several drivers are connected to the same cable. The diodes decouple the driver from the cable when its power is removed.

SYMBOL:

-001 -002

FIGURE 2-9 CDVR SYMBOLS

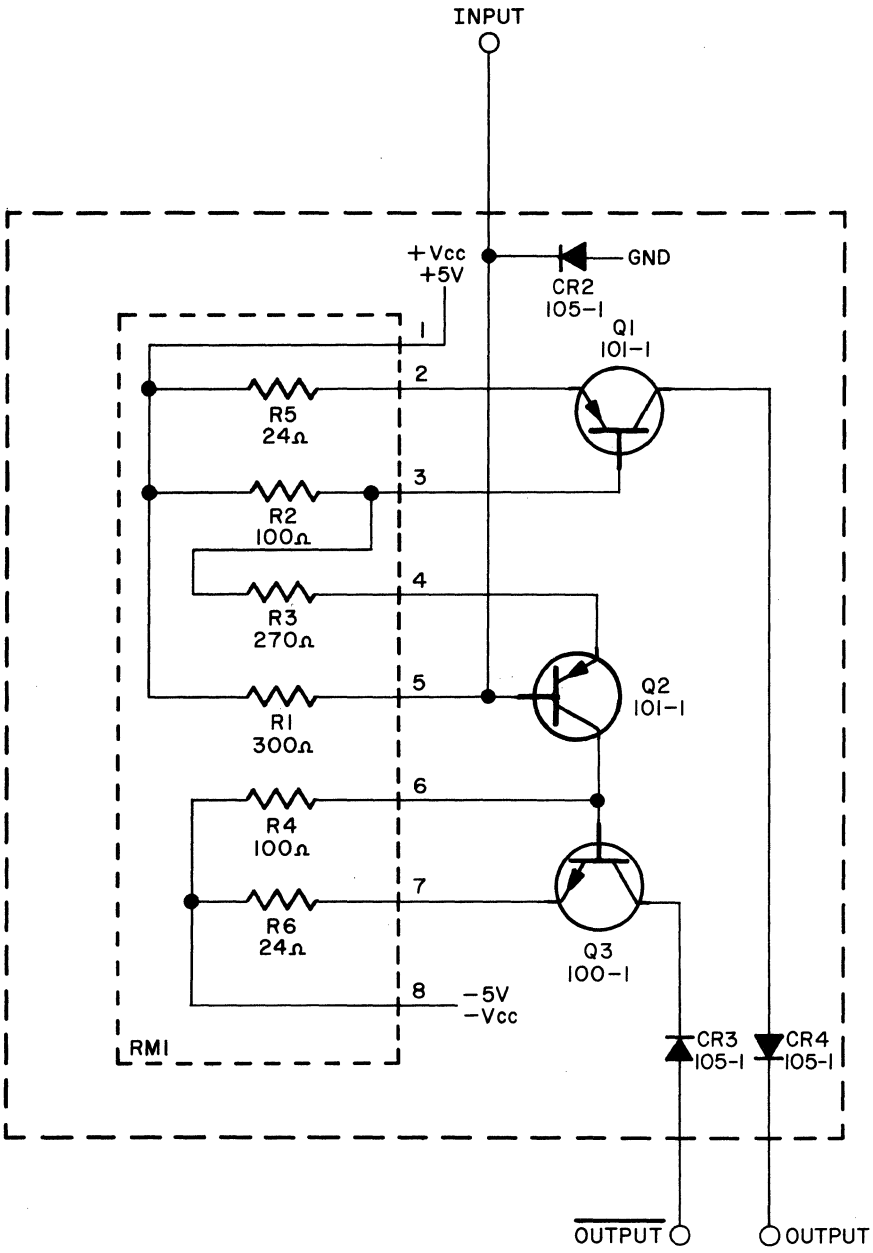


FIGURE 2-10 CABLE DRIVER SCHEMATIC

DESIGNATION	DESCRIPTION	MCS PART NUMBER
Q_1, Q_2	Transistor, PNP	653-100001-001
Q_3	Transistor, NPN	653-100000-001
R_1 - R_6	Module, Resistor	650-600000-001
CR_1 - CR_3	Diode, Switching	653-100005-001

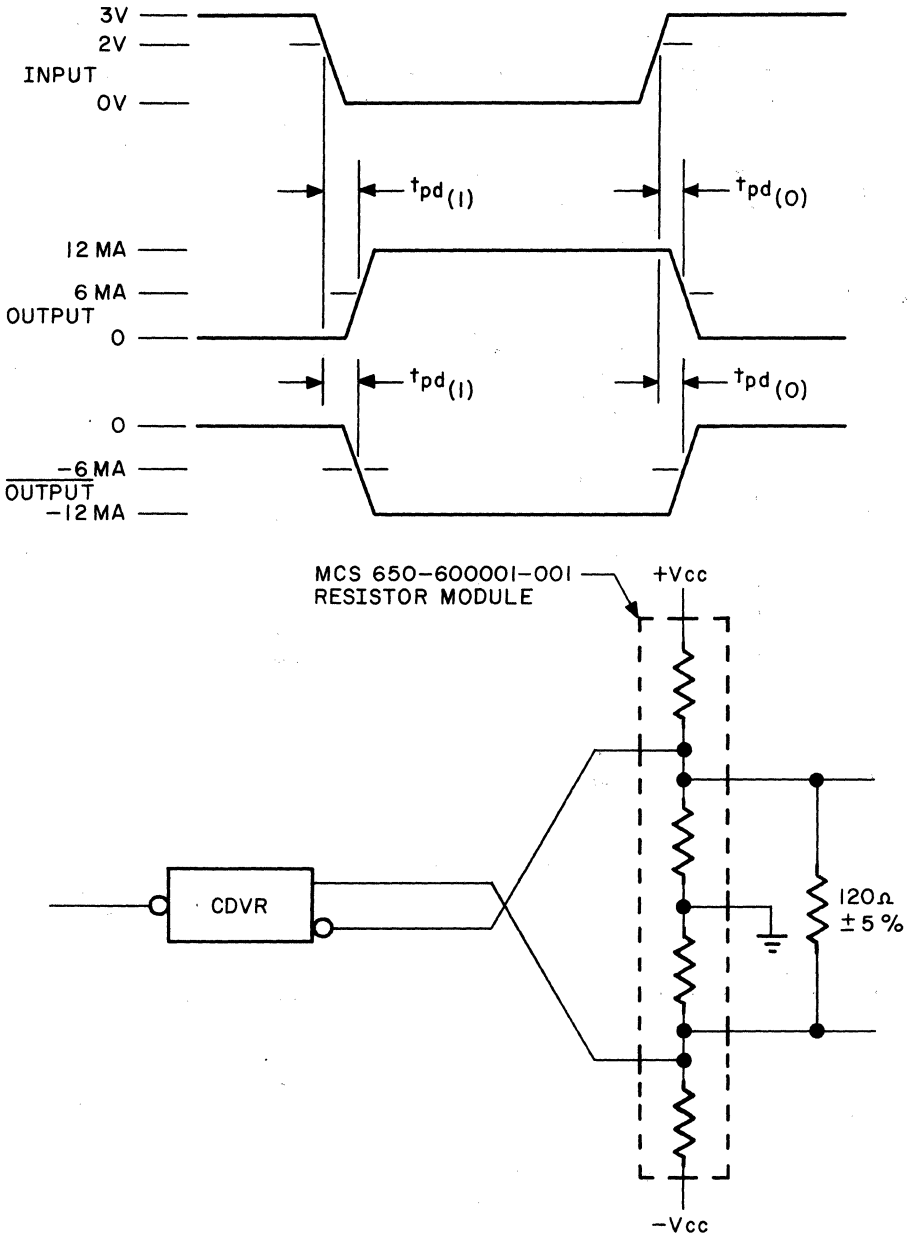


FIGURE 2-11 WAVE FORMS AND TERMINATION NETWORK

CABLE RECEIVERS

General

The cable termination modules, -001 and -002 are used in conjunction with cable drivers 60001 and 60002 (MCS Circuit Registration - 600000) and MCS Part Number 640-100020 line receivers in twisted pair transmission line applications. They are used to terminate lines in their characteristic impedance while providing a differential bias voltage.

Functional Description:

Impedance: (Small Signal)
Either Teminal to Signal Common:
-001, 002 60 Ohms ±3%
-003 6800 Ohms ±5%
Terminal To Terminal:
-001, -002 120 Ohms ±3%
-003 960 Ohms ±5%

Output Level:
-001, -002; Terminals Shunted by 120 Ohms ±5%; -003 Open Circuit
Positive Terminal: 0.18V ±10%
Negative Terminal: -0.18V ±10%

Environmental Conditions:

Operating Temperature Range: 0°C To 70°C

Power Requirements:
-001, +5V. ±5%, 7 Ma, Max.
-002 -5V. ±5%, 7 Ma, Max.
-003, +5V. ±5%, 0.21 Ma, Max.
-5V. ±5% 0.21 Ma, Max.

Theory of Operation

The -001 module is employed at lines where only one driver at a time is operating. Refer to Figure 2-12.

The -002 module is used where several drivers may be operating simultaneously. Diode CR1 limits the differential voltage to about .65 volts when two or more drivers are applying current to the line.

When a single driver is working into several receivers distributed down a line, the state of the line becomes indeterminate when power to the driver is removed. When this situation is intolerable, the driver termination is omitted, and the -003 termination circuit is employed at each receiver.

Up to 8 -003 circuits may be cascaded onto a single driver. The circuit must be used with a 60002 driver, and must be limited to level type signals, since the line will be improperly terminated, and signal edges will result in line reflections requiring considerable settling time.

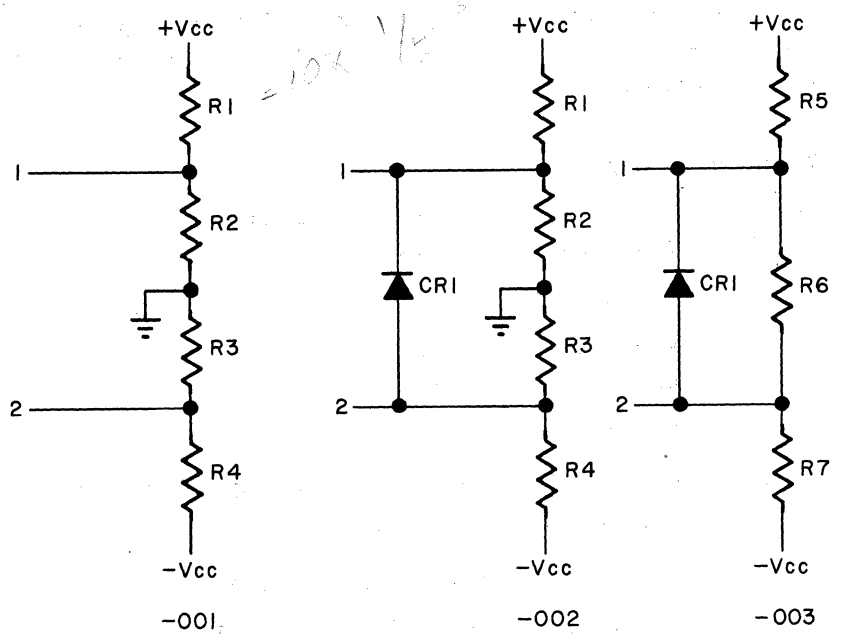


FIGURE 2-12 CABLE RECEIVER SCHEMATIC

DESIGNATION	DESCRIPTION	MCS PART NUMBER
R_1 - R_4	Module Resistor	650-600001-001
R_5 - R_7	Resistor, 13K ± 5%, 1/4W	650-100000-100
R_6	Resistor, 1K ±5%, 1/4W	650-100000-073
CR_1	Diode Switching	653-100005-001

TABLE 2-1

DRIVER/RECEIVER MODULE TO I/O PANEL CABLING

SIGNAL NAME	3M CONNECTOR	AMP BLOCK	WIRE COLOR
	XY1C		
IOD00	1	13A	Brown
IOD00N	14	14A	White
IOD01	2	13B	Red
IOD01N	15	14B	White
IOD02	3	11A	Orange
IOD02N	16	12A	White
IOD03	4	11B	Yellow
IOD03N	17	12B	White
IOD04	5	11C	Green
IOD04N	18	12C	White
IOD05	6	9A	Blue
IOD05N	19	10A	White
IOD06	7	9B	Biolet
IOD06N	20	10B	White
IOD07	8	9C	Gray
IOD07N	21	10C	White
IOD08	9	7A	Black
IOD08N	22	8A	White
IOD09	10	7B	Brown
IOD09N	23	8B	Gray
IOD10	11	7C	Red
IOD10N	24	8C	Gray
IOD11	12	5A	Orange
IOD11N	25	6A	Gray
IOD12	13	5B	Yellow
IOD12N	26	6B	Gray
	XY2C		
IODA5	1	13H	Green
IODA5N	14	14H	Gray
IODA4	2	13J	Blue
IODA4N	15	14J	Gray
IODA3	3	11G	Violet
IODA3N	16	12G	Gray
IODA2	4	11H	Brown
IODA2N	17	12H	Black
IODA1	5	11J	Red
IODA1N	18	12J	Black
IODA0	6	9G	Orange
IODA0N	19	10G	Black
IODMU	7	9H	Yellow
IODMUN	20	10H	Black

TABLE 2-1

DRIVER/RECEIVER MODULE TO I/O PANEL CABLING (CONT'D)

SIGNAL NAME	3M CONNECTOR	AMP BLOCK	WIRE COLOR
	XY2C		
IODSIU UDSIQN	8	9J	Green
IODSIUN	21	10J	Black
IODIU UDIQN	9	7G	Blue
IODIUN	22	8G	Black
IOCDF DACSN	10	7H	Brown
IOCDFN	23	8H	Violet
IOCLK IOCLN	11	7J	Red
IOCLKN	24	8J	Violet
IOIOS [illegible]	12	5H	Orange
IOIOSN	25	6H	Violet
IOIOF DAIQN	13	5J	Yellow
IOIOFN	26	6J	Violet
	XY3C		
IOID0 SIDQN	1	17D	Green
IOID0N	14	18D	Violet
IOID1	2	17E	Blue
IOID1N	15	18E	Violet
IOID2	3	17F	Brown
IOID2N	16	18F	Yellow
IOID3	4	15D	Red
IOID3N	17	16D	Yellow
IOID4	5	15E	Green
IOID4N	18	16E	Yellow
IOID5	6	15F	Blue
IOID5N	19	16F	Yellow
IODIR DIRQN	7	13C	Brown
IODIRN	20	14C	Orange
IOSIR [illegible]	8	13D	Red
IOSIRN	21	14D	Orange
IODMR DMRQN	9	13E	Green
IODMRN	22	14E	Orange
IOICB IOICB	10	13F*	Blue
IOICBN	23	14F*	Orange
IOD13	11	13G	Brown
IOD13N	24	14G	Green
IOD14	12	11D	Red
IOD14N	25	12D	Green
IOD15	13	11F	Blue
IOD15N	26	12F	Green
Shield		12E	

*No terminating resistors.

I/O BUS TERMINATOR

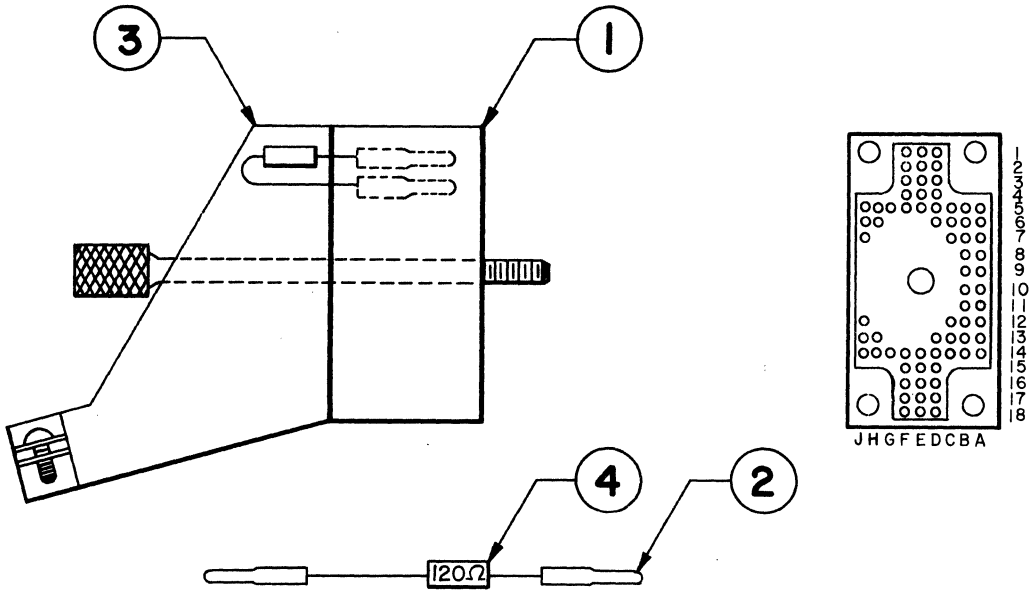


FIGURE 2-13 I/O TERMINATOR

I/O TERMINATOR LIST OF MATERIALS

ITEM	MCS NUMBER	DESCRIPTION	QUANTITY
1	667-200000-001	Recpt.	1
2	667-200000-201	Pins	78
3	667-200000-601	Shield Assy.	1
4	650-100000-051	120Ω 1/4w 5%	39

The I/O Terminator illustrated in Figure 2-13, is used at the last point in the chain in the last PCI in the system. Each controller has bus "in" and bus "out" connectors (26 pin 3M) which are internally jumpered within each controller, and cabled from each controller's bus "out" to the next controller's bus "in". The last controller in the system has a bus "out" which would be floating, causing improper balance and line reflection on the I/O bus. To avoid this, the last controller position bus "out" is cabled to the PCI I/O connector panel where the Terminator is then plugged in.

III. INPUT/OUTPUT OPERATION

INTRODUCTION

The Register I/O and the Direct Memory Processor use the party line I/O bus for data transfers. Data that is transferred over the I/O cable is transmitted by differential drivers and received by differential receivers. This reduces common mode noise induced by capacitive coupling between twisted pairs and also permits the electronic cabinets to be at different ground potentials. All signals on the I/O cable can be transmitted a maximum of 100 feet.

The I/O cable contains three separate busses (Figure 3-1). The first bus is a 16 bit, bi-directional data bus used for transferring data to and from the computer. During update periods, the data bus is also used to establish priority for the data interrupts, service interrupts and the direct memory processor operations. The second bus is an 8 bit device address bus containing a 6 bit field that can select 1 of 64 controllers and a 2 bit field used to determine the direction and type of I/O transfer. The third bus is the source ID bus used normally to identify the communicating controller; or, as in the case of the DMP, it is used to encode ROM entry addresses. In addition to the 3 major busses, the I/O cable also carries several control signals such as master clear (ICB), clock (5MHZ), 3 request lines from the controllers, 3 update lines that are used to establish priority and a sync line used to control the timing of transfers.

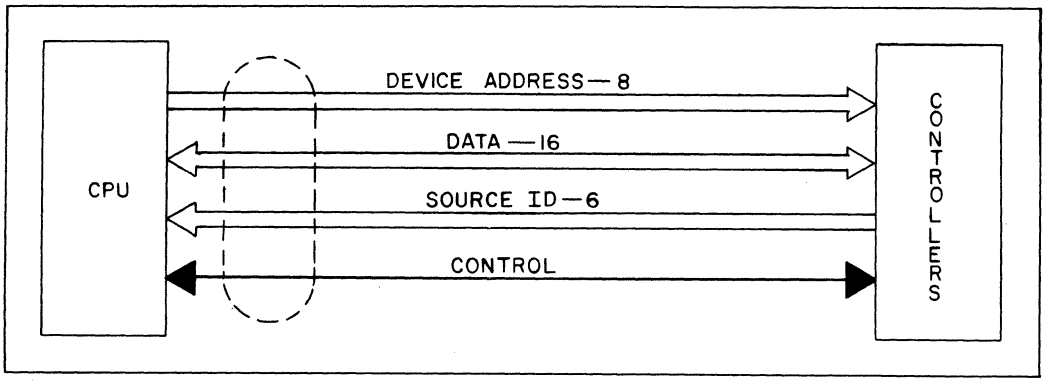


FIGURE 3-1 I/O CABLE

Device Addressing And I/O Instruction Decoding

Refer to Figure 3-2. The device address is used to select a controller on the I/O cable during register I/O operations. The 6 device address signals (DA0-DA5) are transmitted from the instruction register during each I/O instruction or from an 8 bit function register during DMP operations. Each controller has been jumpered to decode a unique device address. The controller that is selected will respond with an internal signal called This Unit Is Selected (TUISEL) which will enable the I/O instruction Logic to decode the two remaining device command signals (IOF, CDF). The I/O instruction decoder will develop one of four unique signals labeled command, input

status, input data or output data. A sync pulse (IOS) is transmitted to the I/O Instr tion decoder during a timing window in which the device address and IOF, CDF signals are guaranteed valid. The outputs of the I/O instruction decoder will correspond to the width of the sync pulse. The width of the sync pulse will vary with the I/O mode of operation. For DMP operations, an Enable Zero F/F (ENZERO) will allow the controll transferring data to respond to a device address of zero. (This permits the 6 device address bits within the I/O function register to be used for custom I/O macros).

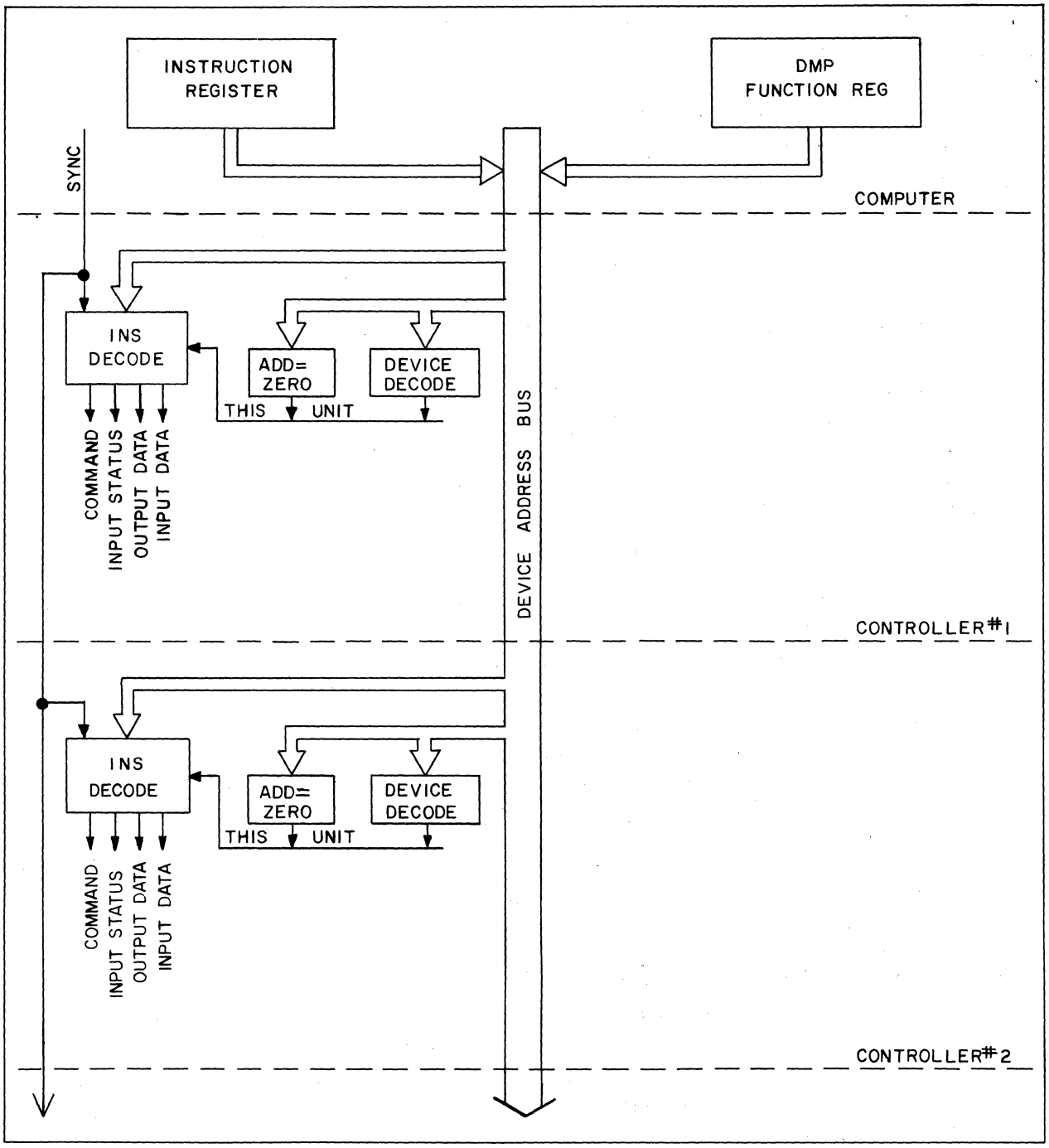


FIGURE 3-2 DEVICE ADDRESS AND INSTRUCTION DECODE

Output Data

Data from the computer's I/O register is transferred to the controller's data register with an output data command. The DMP I/O macro programs will generate this command for DMP output transfers. The data is guaranteed to be valid during the output data pulse (OUDCM) decoded in the I/O instruction decoder. Either edge of this pulse may also be used to strobe the data. Figure 3-3 is a functional block diagram of output data.

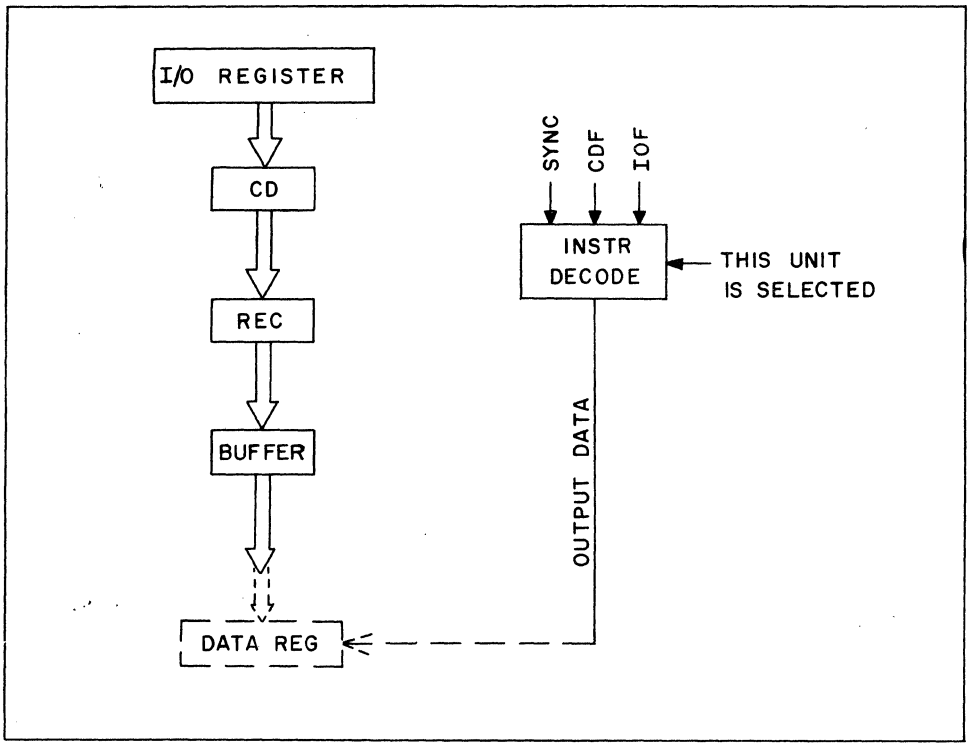


FIGURE 3-3 OUTPUT DATA

Input Data

When an input data command is executed, the input data signal (ENID) will open the input data transfer gates and place the data word onto the I/O data bus. The duration of the data pulses are controlled by the gating signal which is in turn controlled by the width of the sync pulse. The sync pulse will have a minimum width of 1 μs to guarantee valid data in the I/O input buffer for 100 feet of I/O cable. See Figure 3-4.

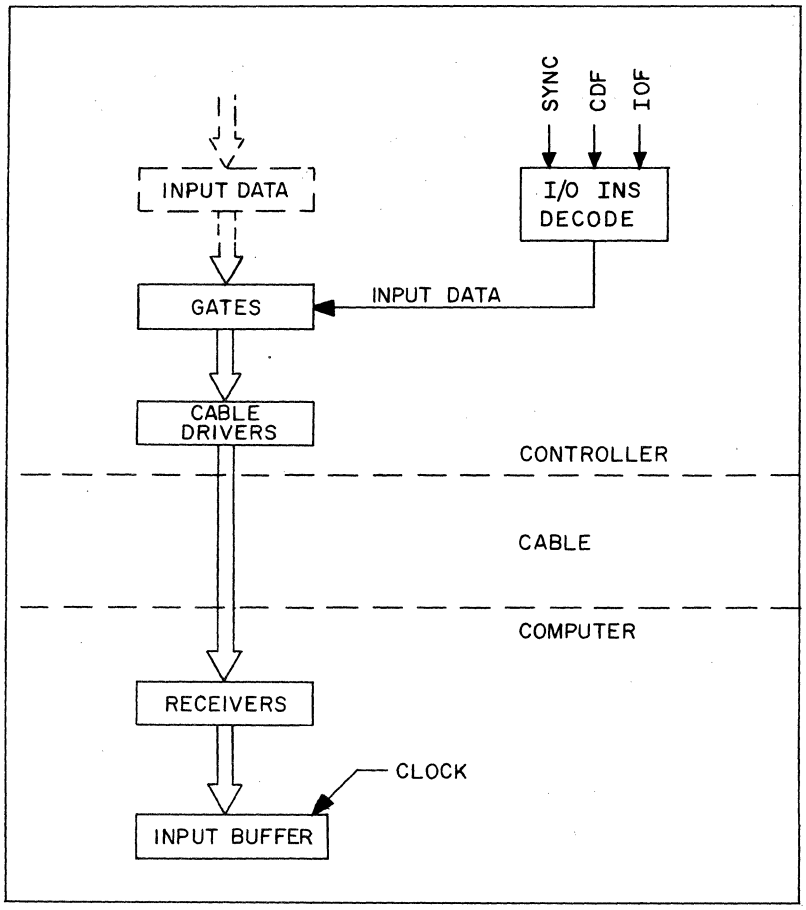


FIGURE 3-4 INPUT DATA

Input Status

Input status commands cause the input status pulse (ENIS) to open the status transfer gates and place a status word on the I/O data bus. Reference Figure 3-5. The duration of the data pulses are controlled by the gating pulse which in turn is controlled by the width of the sync pulse. The sync pulse will have a minimum width of 1 μs to guarantee valid data into the I/O input buffer register for 100 feet of I/O cable. Bit 0 of the data will be equal to a one for any error condition. Errors are indicated by status bits 1-6. Bits 1-6 are'OR'ed'to form bit 0. Bit 1 is used for synchronous devices to indicate a data word lost condition. An overflow is a word lost on an input transfer. An underflow is a word lost on an output transfer. Bit 2 is used to indicate a device parity error or checksum condition. Bit 3 is used to indicate an inoperable condition in the device such as off line or power removed. Bit 4 is used by the DMP when a memory parity error occurs on a data transfer.

The DMP will issue a terminate command with bit 7 = 1 if it detects a memory parity error on a data transfer. Bits 7-15 is the event field of which bit 7 indicates device busy, bit 8 indicates data ready and bits 9-15 contain optional event information.

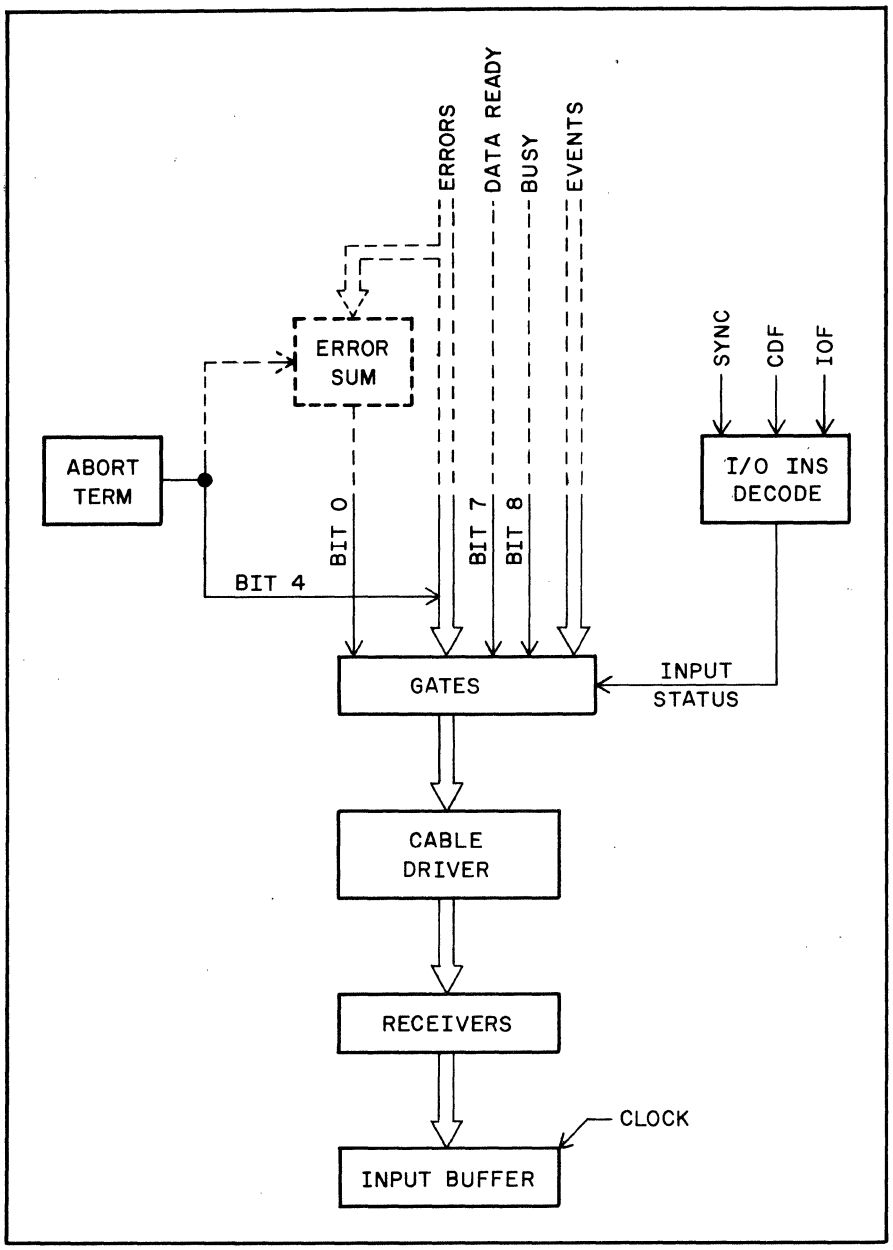


FIGURE 3-5 INPUT STATUS

Outputs to Command Registers

The output command can be used to load one of three command registers; enable and disable the interrupts within the controller; force either a data or service interrupt; select either the register or DMP I/O mode and start or stop a device. When the output command is issued, bits 0 and 1 of the data will be used to select one of the three basic type of commands.

See Figure 3-6. The first command, the select command, is developed by having both bits 0 and 1 equal to zero. This command causes select command register to be loaded with bits 2-15 of the data word. The controller will not accept a select command if it is busy. This command is normally used for device selection before a transfer initiate command is issued. However, it can be used as an extension of the control command field which is discussed next.

The second command is the control command. The control command will load the control command register with bits 7-15 of the data word if the device is not busy. The control command is selected by having bits 0, 4 and 5 equal to zero and bits 1 and 6 equal to one.

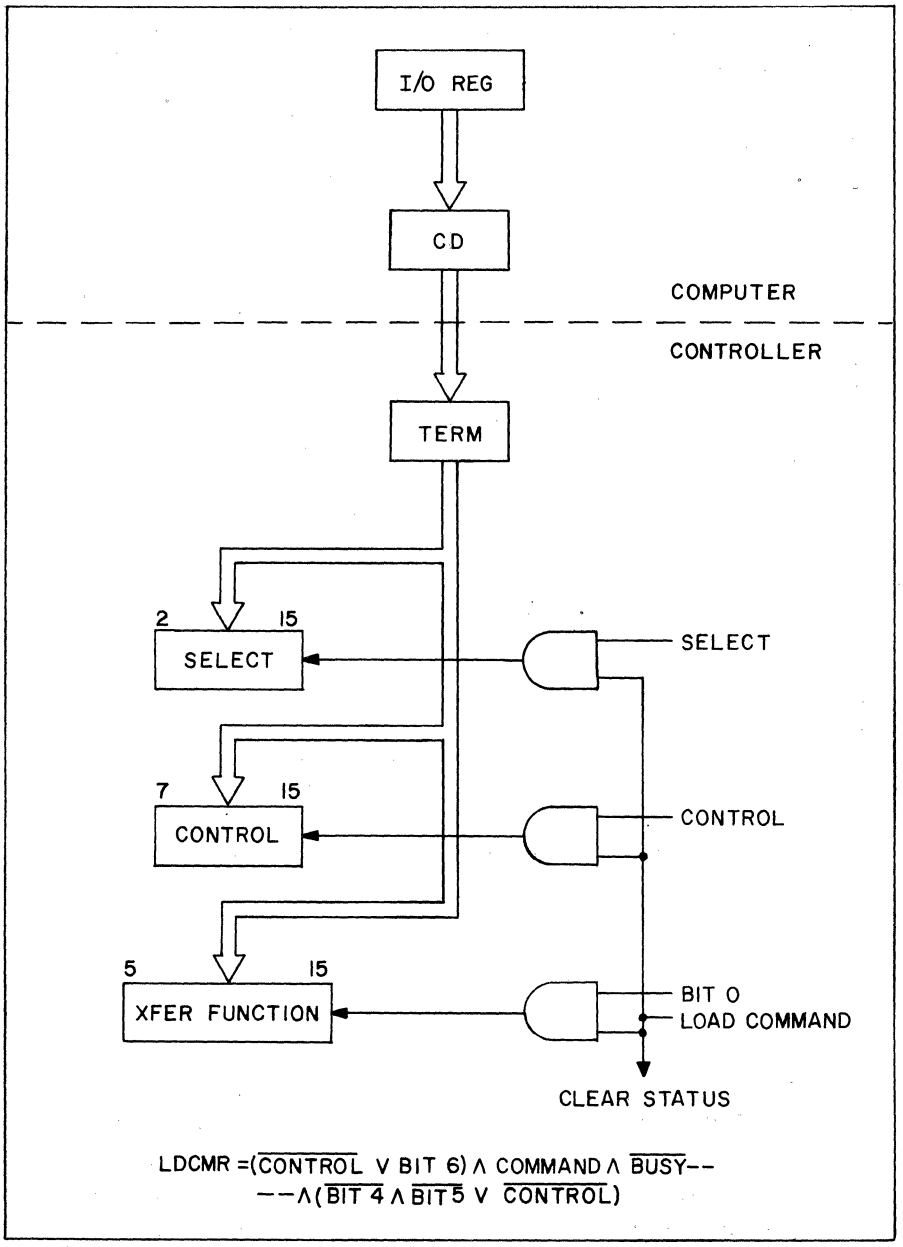


FIGURE 3-6 OUTPUT TO COMMAND REGISTER

The third command, transfer initiate command, is used to start a device and will cause the load command pulse to load the transfer initiate command register with data bits 5-15. The controller must not be busy to accept this command. It should be noted that a clear status pulse (CLSTA) will be generated anytime the load command pulse is developed and will be used to reset any resettable status.

Output Command

In addition to loading command register, output command can be used for standard control functions. If bits 4, 5 and 6 of a control command are equal to zero the command becomes a no-op command. The no-op command will not load the control command register. The no-op command is used for two basic functions. It allows bits 2 and 3 to enable and disable the interrupts at any time and it can be used to generate a clear status signal (CLSTA) if the controller is not busy. The clear status pulse is used to reset any resettable status. If bit 4 of the control command is equal to a one, then an end of block (EOB) pulse will cause a data interrupt request. This feature is used by the DMP to force a data interrupt request at the end of each block of chained data. If bit 5 of the control command is equal to one, a terminate command is issued to stop a device or force a service interrupt request if the controller is not busy. If the controller is busy the service interrupt request will occur when the busy signal is turned off by the device. If bits 4 and 5 are both equal to one, then both of the above functions will occur with the data interrupt request being serviced first because of its higher priority in the computer. Any transfer initiate command in addition to loading a transfer initiate command register will turn on the busy signal and start a device. Bit 1 of this command is used to select the I/O mode. Bit 2 and 3 of the initiate command are used to enable and disable the data and service interrupts (Bit 03 = SI if "1"; Bit 02 = DI if "1"). Bit 4 is stored in the input/output F/F so that the controller will be able to properly steer the data ready F/F and be able to modify the source ID bits for DMP data transfers.

Busy

The busy signal is used to indicate to the computer that the controller is either performing a device dependent function or a data transfer function. When the busy signal goes true, it will inhibit the load command pulse and therefore prevent changes within the three command registers and status indicators. The busy signal is generated at two basic times. It is always turned on with any transfer initiate command and will remain on until an error condition occurs, a terminate command is received and a data transfer function is complete, or it will be reset immediately by an abort terminate command. The busy signal is also turned on for device dependent control command and will be reset automatically when the function is completed. A service interrupt request will be generated when the busy signal is turned off, if the interrupt is connected. For DMP register file operations a terminate sequence is started when the busy signal is turned off.

Data Ready

The data ready signal is used to indicate that a data word is ready for transfer. In the input mode, it is turned on when the input buffer is filled by the device and is turned off when an input data transfer instruction or a terminate command is executed. In the output data mode the data ready signal is turned on with the transfer initiate command or when the output buffer is emptied by the device and is turned off when the cutput data instruction is executed. The data ready signal is used to generate the data interrupt request for register I/O operations or it is used to generate the DMP data transfer request for DMP operations.

Interrupt System

The data interrupt, service interrupt and DMP sections of the controller all use a similar technique for communicating to the computer. Each section operates independently of the others, except for their data busy priority system. However, similar sections in other controllers will share the same resources within the computer. All operations are initiated within the controllers. Each section within the controller has a request line to the computer. When one of the request lines to the computer is turned on, the computer will respond with an update pulse to the requesting sections and to all similar sections within the other controllers. Because several controllers could be requesting at the same time, the update pulse is used to open a timing window in which the controllers use the data bus to establish priority. Each controller on the I/O cable is assigned a unique bit on the I/O data bus. All requesting controllers will turn on their bit when the update pulse is true. Connected to the I/O bus within each controller is a jumpered priority detector. It consists of a large OR gate to which the data bits for all higher level controllers are connected. When the update pulse is received, each requesting controller will place a source ID word onto the source ID bus. If the priority detector within the controller detects a higher priority, then that controller will remove its source ID. Within a very short time only one source ID will remain on the source ID bus. The correct source ID is guaranteed to be valid at the computer at the end of the update pulse. At this point, the computer will sample the source ID word and place that word into the source ID register. For interrupts, the source ID is the same as the device address code for the controller. For DMP request, the source ID selects the DMP channel and the functions to be performed. The computer does not need to know which controller is requesting a DMP operation since the controller which is transferring data will respond to a device address of zero. Two bits of the source ID from the DMP section are used to select custom I/O macros; the remaining four bits of the source ID will become the 4 most significant bits in a 7 bit address field used for custom I/O macro ROM entries. Figure 3-7 illustrates the Interrupt System.

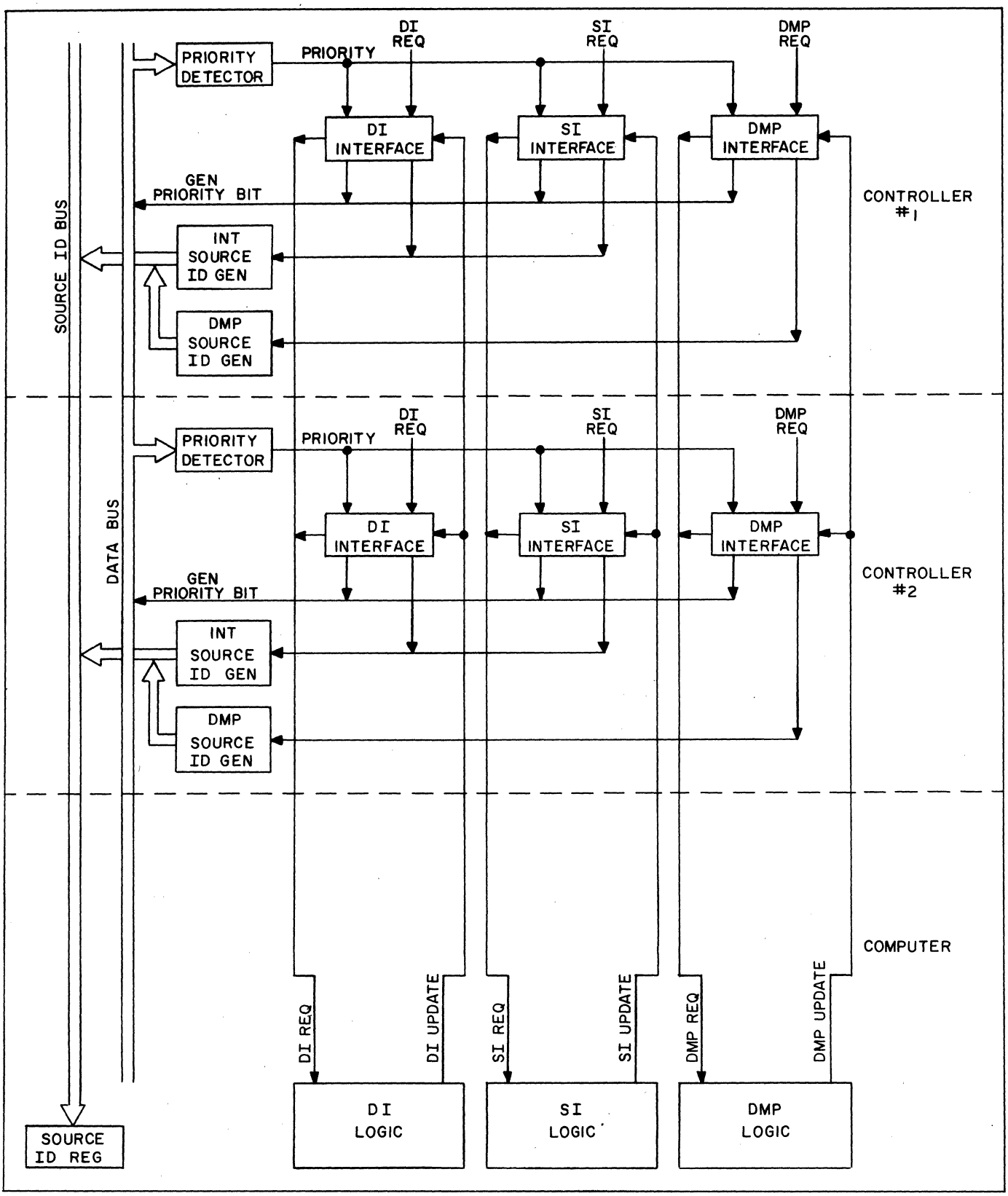


FIGURE 3-7 INTERRUPT SYSTEM

Data Interrupt

The data interrupt must be enabled within the controller by an output command before any interrupt request can be transmitted to the computer. Refer to Figure 3-8. An interrupt strobe pulse (INTSTB), which loads data bit 2 into the enable F/F, is generated for each transfer initiate or functional control command if the controller is not busy or for any no-op command. For the register I/O mode the data ready signal going on will set the data interrupt set request F/F. For DMP operations the set request F/F can be set with an EOB command from the computer. Provided the interrupt is enabled and interrupt system is not being updated, then the set request F/F will cause the data interrupt request F/F to set. At this time the request line to the computer is turned on and the interrupt sequence is started. On the next clock pulse after the request F/F is set, a reset F/F is set and a reset sequence is started which will first reset the set request F/F. For the controller which has the highest priority the request F/F will go reset on the trailing edge of the update pulse. For the other controllers requesting, their request F/F's will stay set for the next interrupt sequence. The request F/F in any controller can also be turned off by reseting the enable F/F with a no-op or an initiate command or directly turned off by a terminate command without the EOB bit set.

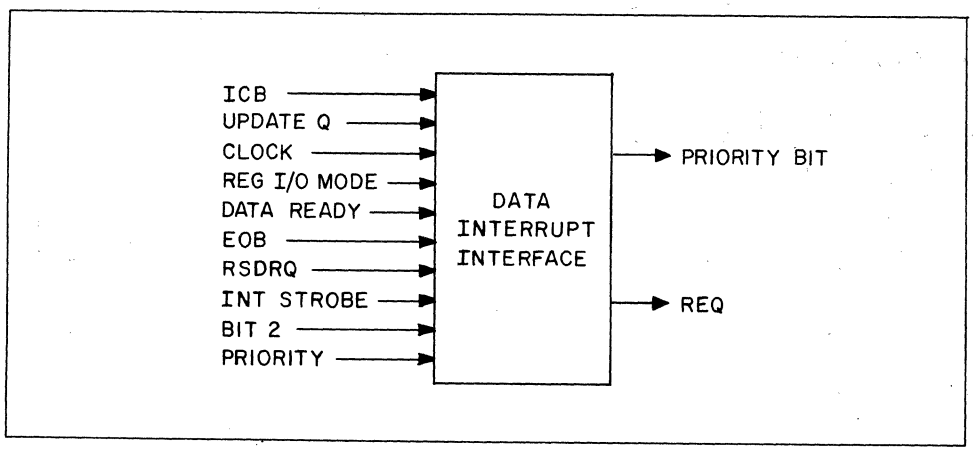


FIGURE 3-8 DATA INTERRUPT

Service Interrupt

The service interrupt is very similar to that of the data interrupt. The enable F/F is loaded by the interrupt strobe pulse which is now using bit 3 as the select bit. The set SI request signal (STSIRQ) will set the request F/F provided the interrupt is enabled and the interrupt system is not being updated. The set SI request signal is turned on when the busy signal is turned off or when a terminate command is executed if the controller is not busy. Once the request F/F is set, the interrupt request signal is sent to the computer and the interrupt sequence is started. At the same time a reset pulse (SIRST) is generated which is used to reset the set SI request signal. If the controller has highest priority, the request F/F will go reset on the

trailing edge of the update pulse. The request F/F can also be reset when the enable F/F is turned off with a command.

DMP Interface

The DMP interface logic is used to perform four basic functions: Initialize, transfer data, terminate and is used for starting custom I/O macros. The initialize and terminate functions are used only for DMP register file operations. The initialize function is used to transfer the contents of dedicated memory locations into the DMP register file. The terminate function is used to transfer the contents of the transfer address register into the appropriate dedicated memory location. The DMP source ID bits are jumpered to unique configurations as follows:

DMP SOURCE ID FUNCTIONS

BITS							FUNCTION
0	1	2	3	4	5		
0	0	Channel Select					Memory File In
0	1						Memory File Out
1	0	0	0	FILE SELECT			Register File In
1	0	0	1				Register File Out
1	0	1	0				Register File Initialize
1	0	1	1				Register File Terminate
1	1	ROM Entry					Custom I/O Macro's

The initialize sequence is started with a transfer initiate command with data bit 1 equal to a one. This causes a set initialize request F/F to be set. The request F/F will set once the initialize request signal is on and the request in progress signal and the update signals are off. The request F/F turns on the DMP request line (DRDMRN) to the computer and enables the priority bit (DMPRQN) to be placed onto the data bus when the update signal is true. The request F/F also starts a transfer sequence that will transfer the contents of the set initialize F/F into a holding F/F used for source ID generation. The source ID bits (0-5) will be encoded with a code of 1010XX where the least significant two bits are jumpered to select one of the four register files. The three DMP functions: initialize, transfer data and terminate all operate in a similar manner with the initialize function having the highest priority followed by the terminate function, with the data transfer function being the lowest. There are two additional operations performed during data transfer. The input/output signal is encoded into the source ID and the device address zero decoder is enabled so that the controller will be able to respond to any command with a device address of zero if it had highest priority at the trailing edge of the DMP update signal.

IV. INPUT/OUTPUT INSTRUCTIONS

Two input instructions are provided to enable a data or status word to be transferred from any peripheral device to any general register. Two output instructions are provided to enable a data or command word to be transferred from any general register to any peripheral device.

Up to 64 peripheral devices, consisting of four groups of 16 each, are addressable by each instruction. The group address is obtained from the two least significant bits of the operation code field. Therefore four operation codes and mnemonics are assigned to each instruction.

I/O GROUP A	Consists of Device Addresses 00-0F
I/O GROUP B	Consists of Device Addresses 10-1F
I/O GROUP C	Consists of Device Addresses 20-2F
I/O GROUP D	Consists of Device Addresses 30-3F

All instructions are executed in the fixed length of time contained in each instruction description.

OUTPUT COMMAND

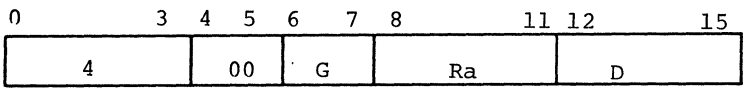
OCA OCA (40) Output Command To I/O Group A

OCB OCB (41) Output Command To I/O Group B

OCC OCC (42) Output Command To I/O Group C

OCD OCD (43) Output Command To I/O Group D

1.07 μs



G, D → I/O Address Lines
(R_a) → I/O Data Lines

The group (G) and device (D) numbers contained in the instruction word are placed on the I/O bus address lines.

The 16 bit output command stored in register Ra is then transferred to the I/O register and placed on the I/O bus data lines.

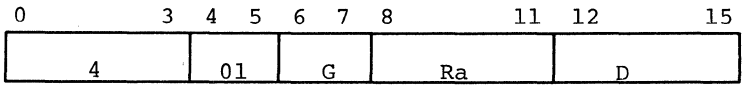
OUTPUT DATA

ODA ODA (44) Output Data To I/O Group A

ODB ODB (45) Output Data To I/O Group B

ODC ODC (46) Output Data To I/O Group C

ODD ODD (47) Output Data To I/O Group D



1.07 µs

G, D → I/O Address Lines
(R_a) → I/O Data Lines

The group (G) and device (D) numbers contained in the instruction word are placed on the I/O bus address lines.

The 16 bit data word stored in register Ra is then transferred to the I/O register and placed on the I/O bus data lines.

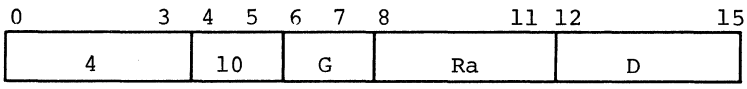
INPUT STATUS

ISA ISA (48) Input Status From I/O Group A

ISB ISB (49) Input Status From I/O Group B

ISC ISC (4A) Input Status From I/O Group C

ISD ISD (4B) Input Status From I/O Group D



1.6 µs

G, D → I/O Address Lines
Device Status → Ra

The group (G) and device (D) numbers contained in the instruction word are placed on the I/O bus address lines.

NOTE: I/O interrupt processing routines use a unique ISA or IDA instruction format:

ISA,R,0 which is an ISA instruction with a device address of 0 causes the routine to interrogate the Service Interrupt sub-levels.

IDA,R,0 which is an IDA instruction with a device address of 0 causes the routine to interrogate the Data Interrupt sub-levels.

Up to 16 bits of status are then transferred from the addressed device over the I/O bus to replace the contents of register Ra.
Affected: Ra

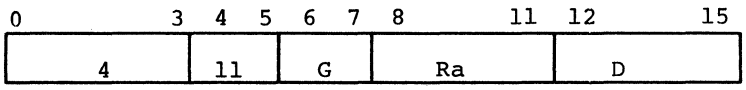
INPUT DATA

IDA IDA (4C) Input Data From I/O Group A

IDB IDB (4D) Input Data From I/O Group B

IDC IDC (4E) Input Data From I/O Group C

IDD IDD (4F) Input Data From I/O Group D



1.6 µs

G, D → I/O Address Lines
Device Data → Ra

The group (G) and device (D) numbers contained in the instruction word are placed on the I/O bus address lines.

Up to 16 bits of data are then transferred from the addressed device over the I/O bus to replace the contents of register Ra.
Affected: Ra

V. GENERAL PURPOSE CONTROLLER

INTRODUCTION

The general purpose controller provides all the interfacing logic, including data buffer amplifiers, required to connect an I/O device to the I/O cable. The general purpose controller also contains a work area where data buffer registers, setup registers, input status logic and special control logic can be implemented. The logic for two I/O interrupts and the DMP channel interface are also included. The general purpose controller will generate the timing pulses for transferring data, commands and status into and out of the work area.

Internal jumpers must be connected to satisfy variable I/O functions, such as device address and device priority. If the DMP interface is used, some jumpers must be connected to select the type of DMP (Memory or register file), and channel. If custom I/O macros are used, the ROM entry address of the firm-wired program must be jumpered to the source I/D lines.

Data transfers are controlled by two signals from the general purpose controller. One signal, output data command, is a strobe pulse used to output a data word to a buffer register in the work area. A second signal, input data command, is a gating pulse used to gate data in from a buffer register in the work area. These are the only two signals required for data transfers.

For inputting a status word a gating signal (enable input status) is provided. This signal is used just like the input data command signal.

An additional feature of the general purpose controller is that it contains interlocking logic for device dependent functions. A busy signal from the work area is required to enable and disable the interlocking function. The interlocking function is used to prevent a device from receiving a motion command, caused by a program error, during a period in which the device is performing a previous motion command.

For setup operations, the command instruction will cause a gating signal, load command register, to be generated only if the busy signal is false. This pulse (LDCMR) is used to strobe data into a command register in the work area. For more complex setup operations, several sub-functions of the commands are available.

The interrupt logic and its enabling and disabling logic is contained in the general purpose controller. There are two I/O interrupts available in the controller. These interrupts can be used for any function, but the DI is normally used for data transfers and the SI is normally used to indicate that a controller is not busy. The two interrupts are requested by signals from the work area. The set service interrupt request

signal is normally reset when the interrupt has been accepted by a reset service interrupt request pulse from the controller. The data interrupt is normally reset by an output data command, input data command or a terminate command.

The interfacing logic required by the DMP is contained in the general purpose controller. The data request signal must be connected from the work area. Each time the data request signal is true, a transfer sequence will be started.

A 5 MHz square wave and a master clear pulse are also available to the work area from the general purpose controller.

GENERAL DESCRIPTION

The general-purpose controller provides the means for custom installation of a standard interface between the cable driver/receiver set and special device controllers.

Logic diagrams and physical layout drawings are provided in Volume II as a guide to implementing all of the logic functions common to most bi-directional devices. 54 integrated circuit connectors with wire-wrap pins are provided for the implementation of this logic together with the integrated circuits required. In addition, a total of 89 unassigned dual-in-line integrated circuit connectors are provided on the same printed circuit card. These may be used for the custom logic required for each controller, in addition to that portion of the general purpose logic implemented.

The general-purpose controller is packaged on a 7" x 14-1/2" printed circuit card. It contains dual-in-line integrated circuit connectors for all logic circuits. Power and ground are distributed by printed wiring. The number of connectors available for custom wiring is described in Table 5-1.

PINS	CONNECTORS	POWER AND GROUND CONNECTED
14	64	Yes
16	25	No
24	4	No
26	18	No

TABLE 5-1 CUSTOM WIRING CONNECTIONS

The power connections are +5V (pin 14) and GROUND (pin 7). The 26-pin connectors are at the front edge of the card and are available for connecting twisted pair cables between the controller and eight 106-pin I/O cable connectors mounted in the back of the enclosure. These eight connectors and standard I/O cable are used for connecting peripheral devices to the controller. The 16 pin connectors without power connections are used for cable terminating resistors.

The 7" x 14-1/2" printed circuit card is mountable in one-half of a Peripheral Controlle Interface enclosure plane. It is cabled directly to a cable driver/receiver set in the enclosure, which can be connected to a total of four controllers.

LOGIC SIGNALS

The following logic signals are provided at the interface of the general purpose controller logic and the custom logic. The general purpose controller logic is wired as indicated by the logic drawings in Volume II. However, not all of these signals will be required by every device. The unused signals and inputs should be examined for termination requirements.

Device Address From Buffers (DAFBX) 520-100106 SHT. 1

Six device address lines with inverted outputs can be provided. They are defined as:

High True
DAFB0 - DAFB5 (LSB)

Low True
(DAFB0N - DAFB5N (LSB)

It is generally not necessary to interrogate these signals since gating is provided for unit selection.

This Unit Is Selected Line (TUISEL) (106-1)

The desired combination of device address lines are wired into specified gates, thus generating this unit is selected line. TUISEL is high true when the unit is selected either by programmed I/O or DMP mode. This signal is generally not necessary for custom interfaces.

This Unit Has Highest Priority (TUHPRI) (106-1)

All higher priority data bits (DFBOON - DFBXXN) are wired into specified gates, thus generating the TUHPRI line. TUHPRI is high true when the selected unit has the highest I/O priority. This signal is generally not necessary for a custom interface.

Interrupt Level

The interrupt (low true) is custom wired from the output of a generating gate to the desired input data bit (DTDXXN). This signal is generally not necessary for custom interfaces.

Output Data Command (OUDCMN) (106-3)

The OUDCMN signal is a gated pulse which is active (low true) for the duration of the I/O sync (approximately 200 ns). OUDCMN is gated with TUISEL. OUDCMN is not gated with controller busy.

Input data Command (INDCMN) (106-3)

The INDCMN signal is a gated pulse which is active (low true) for the duration of the I/O sync (approximately 1.1 µs). INDCMN is gated with TUISEL. INDCMN is not gated with controller busy.

Enable Input Data (ENID01 - ENID02) (106-3)

ENID01 and ENID02 are provided as the inversion of INDCMN.

Enable Input Status (ENIS01 - ENIS02) (106-3)

The ENIS0X signals are gated pulses which are active (high true) for the duration of the I/O sync (approximately 1.1 µs). ENIS0X is gated with TUISEL. ENIS0X is not gated with controller busy.

Clock From Buffer (CLKFB)

CLKFB is provided as the I/O clock to the device. The same phase relationship is maintained as is present on the differential I/O bus.

Terminate Command (TERMN) (106-3)

TERMN is a gated pulse which is active (low true) for the duration of I/O sync and this unit selected. TERMN is not gated with busy. TERMN should reset all data requests in the custom interface. TERM is provided as the inversion of TERMN. TERMN occurs when the I/O terminate command is performed.

Control Command (CTLCMD) (106-3)

CTLCMD is a high true pulse for the duration of the I/O sync. It is generated when the I/O control command is programmed.

Select Command (SELCTN) (106-3)

Select Command is provided as a low true signal for the duration of valid data bits on the I/O bus. If it is necessary for the custom logic to use this signal, then it must be gated with the I/O sync pulse.

End of Block Command (EOBLKN) (106-3)

EOBLKN maintains the same characteristics as TERMN except that it occurs when the I/O end of block is performed. This signal is generally not necessary for custom interfaces.

Load Command Register (LDCMRN) (106-3)

LDCMRN is a gated pulse occurring during an I/O output command for the duration of the I/O sync (low true). LDCMRN is inhibited by controller busy no operation, TERMN and EOBLKN. LDCMRN should be used to load the command register of the custom interface.

Clear Status Register (CLSTAN) (106-3)

CLSTAN is generated by the same conditions as LDCMRN. However, it is not inhibited by the no operation command. CLSTAN is low true when active and should be used to reset status bits as required in the custom interface.

Set Service Interrupt Request (STSIRQ) (106-1)

STSIRQ must be supplied by the custom logic as a high true signal. It must remain high until the service interrupt reset pulse (SIRSTN) is generated. If STSIRQ is not reset by SIRSTN, unwanted interrupts may occur.

Reset Service Interrupt Line (SIRSTN) (106-1)

SIRSTN is provided as low and high true. It becomes active approximately 100 ns after the trailing edge of service interrupt signal if the SI is connected and STSIRQ is active. SIRSTN remains active until the selected unit is the highest priority plus approximately 100 ns after the SI queue trailing edge. SIRSTN must be used to reset the custom logic STSIRQ signal.

Data Request (DATARS) (106-2)

DATARS must be supplied by the custom logic as high true. It is used to set either the data interrupt or the DMP data request. It must be reset by OUDCMN, INDCMN and Terminate in the custom logic.

Initial Condition Bus (ICBFB) 520-100106 - SHT. 1

ICBFB is provided to the custom logic as both high and low true. It is generated by computer console master clear or power turn-on.

Source ID (DRIDON - DRIDRN) (106-2)

The desired source ID lines are wired from the outputs of supplied gates to pre-set pins on the I/O connector. Only those bits which are "ONES" are wired in. This wiring may also include DMP source ID.

Output Data From Buffer (DFB00 - DFB15) (106-4)

The 16 DFBXX lines provide high true data signals for the duration of the active "ONE" on the I/O bus. DFBXXN are provided as the 16 inverted lines of DFBXX. All the above lines are free of gating.

Data To Logic Module (DTLM00 - DTLM15) (106-5)

DTLMXX are 16 logic signals which are supplied by the custom logic as high signals. Only those data bits which are desired to be sent to the computer need be connected. These lines must be stable during an input data command for the duration of the I/O sync pulse.

Status To Logic Module (ISLM00 - ISLM15) (106-5)

ISLMXX are 16 custom logic supplied signals which are high true. Only those status bits which are desired to be sent to the computer need be connected. These lines must be stable during an input status command for the duration of the I/O sync pulse.

Receiver Data Module to Driver (DTD00N - DTD15N) (106-5)

These 16 lines which are the low true outputs of the respective DTLMXX and ISLMXX supplied gates must be custom wired to pre-set pins on the I/O connector. Only those bits which are used should be wired in.

DMP Store SID Request Strobe (DMPSRS) (106-7)

DMPSRS is a custom supplied high true pulse which is used to generate the store DMP source identification code. Generally the STSIRQ may be used as the DMPSRS signal. DMPSRS may be reset by the LDCMRN signal or SIRSTN. All the DMP source ID generation is contained in the general purpose controller DMP logic.

DETAILED THEORY

The general purpose controller is a standard front end common to all controllers. The logic description which follows explains how this common front end functions as a separate unit, but being common to all controllers, the logic description applies to them as well.

NOTE: The prefix DR before a mnemonic indicates that the signal comes from or goes to the driver/receiver module before going to or coming from the CPU. The driver/receiver module is a level converter from the differential bus to the high (+5V) and low (ground) logic levels used by the controllers. The controller portion of the interface generates some signals and will be termed the user in this description. Circuit and gate designations in this description are referenced by the output pin of that circuit or gate. Table 5-2, at the end of this section, contains a signal mnemonic list with definitions.

Priority decode, service interrupt control and device address decode are located on logic drawing 520-100106, sheet one.

Priority Decode 520-100106-1

The I/O priority is decoded by gates XV5D08 and XV5C08. These two gates look at the data bits from the bus (DFBXX) from sheet four. The data bits that must be connected are only those which have a higher I/O priority than this controller. I/O priorities are described in Appendix A, Peripheral Device Assignments. Figure 5-1 illustrates the logic for priority decode. One line from each higher priority device is connected to the 'OR' gates. Unused inputs are tied to +5V to disable them. Figure 5-1 assumes, for the purpose of illustration, that this device is a card reader, (rather than the general purpose controller) with I/O priority eight (8) from Appendix A. The output of XU2F01 will be high if this controller is the highest priority, and the signal TUHPRI will be generated.

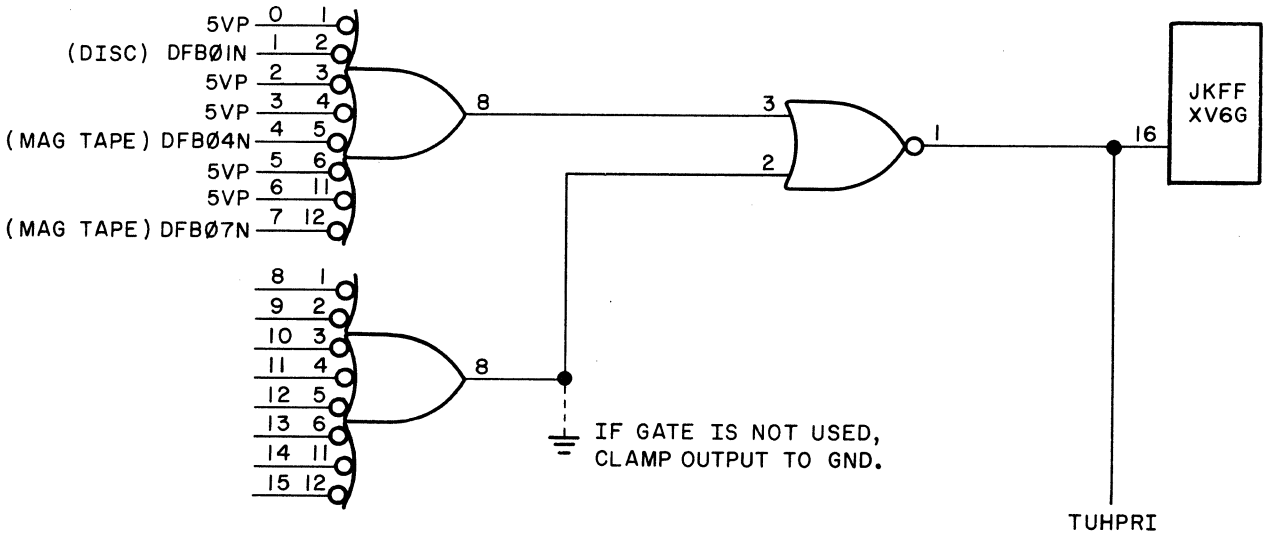


FIGURE 5-1 PRIORITY DECODE

Service Interrupt 520-100106-1

The SI connect F/F XU1F05 will be set or reset by the pulse INTSTB (interrupt strobe). The state of DFB03 will determine the state of SI connect F/F XU1F05.

SI request F/F XV6G15 will be set by gate XU1E12 going low if the SI has been connected, there is no update queue (DRSIUN) on the line, and the signal STSRIQ (set SI request) is detected from the user. The output of XV6G15 is inverted by XV4E02 and sent to the CPU via the driver/receiver module as signal DRSIRN. The CPU will respond to the SI request by sending the signal DRSIUN (SI update queue) back to the controller when the SI request can be serviced. The SI request F/F will be reset on the trailing edge of update queue if this unit is the highest priority requestor. The priority of this unit is put on the data bus during the update queue. This is accomplished from the output of XU1C03 which is one of three 'OR' conditions on gate XU1E06. The output of XU1E06 is inverted by XV4E04 and put on the data bus as this units priority. To connect the priority level to the bus, the signal DTDXXN goes to sheet five where it is'wire-ored' directly to the corresponding bit on the output bus. The priority level is 'turned around' at the driver/receiver module, coming in at sheet four and back to the priority decode logic on sheet one. The priority level is then connected to all controllers having lower priority than this one.

The priority level is also put on the bus if there is a DIREQN (data interrupt request) or DMPRQN (DMP request) satisfying one of the other two 'OR' conditions on gate XU1E06. Pin five of XU1E05 is tied to 5VPD if the DMP option is not included in the system.

The first clock after SI request F/F goes set will cause the F/F XU1F08 (in reset state) to go set, generating SIRSTN (service interrupt reset).

SIRSTN is used to reset the source that provided the initial STSIRQ.

Device Address 520-100106-1

The device address is determined by the output of the six inverters XV2A and the six inverters XV5B. The device address for each peripheral can be found in Appendix A, Peripheral Device Assignments. The correct address for this device is wired into gates XU1D06 and XU1D12 as shown in Figure 5-2. The outputs of the two gates are AND'ed by gate XU1C06 which is one of two OR conditions on gate XU1C08. The resulting signal is TUISEL (this unit is selected).

The signal ADDZEN (address zero) is connected to XU1C10 if the controller has the DMP option. If no DMP, XU1C10 is connected to 5VPD.

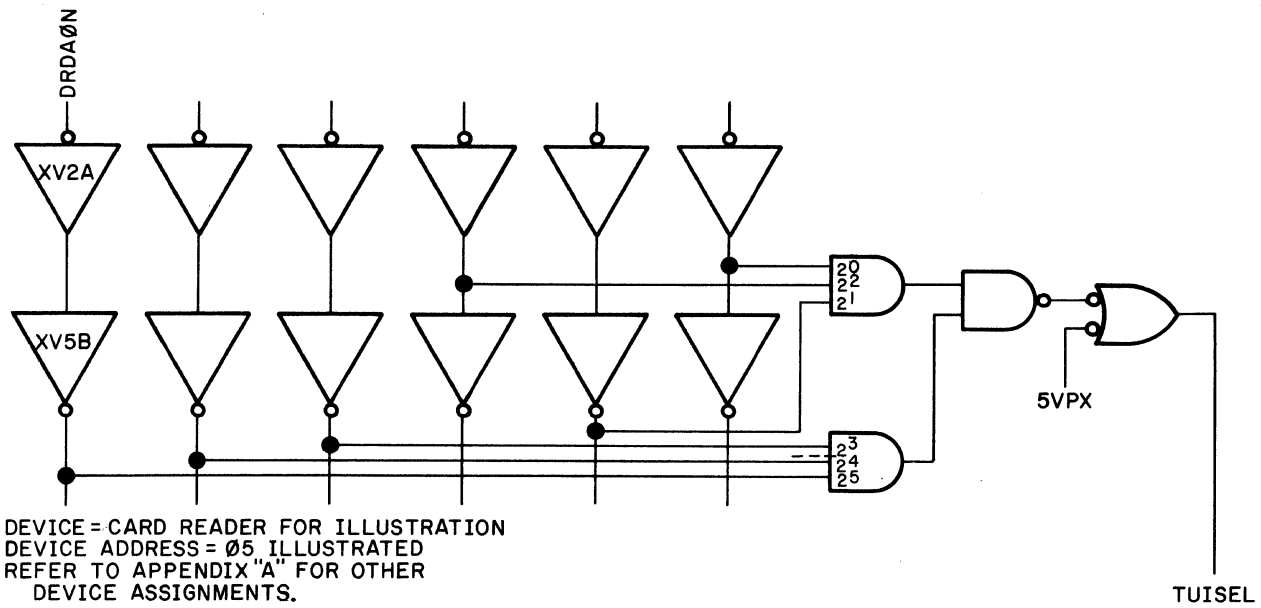


FIGURE 5-2 DEVICE ADDRESS

Data interrupt control and source ID control are located on 520-100106 sheet two.

Data Interrupt Control 520-100106-2

The DI connect F/F XU2E05 is set or reset by the pulse, INTSTB. The state of DFB02 will determine the state of XU2E05.

DI set request F/F XU1B can be set in one of the following two ways. Either the signal EOBLKN (end of block) is detected or the pulse DATARS (data request) from the user is detected. The inhibit signal RGIOMD (XU1B02) is present if the controller has DMP and the DMP mode is selected. If there is no DMP, XU1B02 is connected to 5VPD. The DI request F/F XV6G11 is set by AND gate XU1E08 being satisfied as a result of: DI connect F/F XU2E05 set, DRDIUN (data interrupt update queue) not present and DI set request F/F XU1B set. The output of XV6G11 is inverted by XV4E06 and sent to the CPU via driver/receiver module as signal DRDIRN (DI request). The CPU will respond by sending DRDIUN (data interrupt update queue) to the controller when DRDIRN is detected and can be serviced. When DRDIUN is received at the controller, it will be AND'ed with DI request F/F on gate XU1C11. The signal generated (DIREQN) goes back to sheet one providing one of the 'OR' conditions on XU1E04 to put the priority level on the data bus.

The first clock, after DI request F/F is set, causes the DI reset F/F (XU1B08) to go set, which in turn allows the DI set request F/F to go reset. The next clock resets the DI reset F/F XU1B.

The DI request F/F will be reset on the trailing edge of the update queue if this device is highest priority. In the case of both DI and SI request, if the device is not the

highest priority requestor, the request F/F's are inhibited from resetting by keeping the K input at ground. This results in leaving the request on line (pending) until the device becomes the highest priority requestor.

If a terminate is detected, the signal RSDRQN (reset data request) is generated on sheet three and is received on gate XV6C (sheet two), resetting any outstanding DI request on the line.

Source ID

When a DI or SI update pulse is received, each controller puts its unique source ID on the source ID bus through inverters XV4D. Only the inverters needed for the ID code are connected. The source ID code is the same as the device address code for the controller.

The signals SIREQN and DIREQN are OR'ed by gate XU2D03 to prime AND gate XU1D.

The second input to XU1D is TUHPRI. If the priority detector within the controller detects a higher priority, TUHPRI goes false, disabling gate XU1D which removes the source ID of each lower priority controller. The source ID of the highest priority requestor is valid at the CPU by the end of the update pulse.

Gate XU2F04 is used to reset status gates in the controller. The output, RSTSTN (reset status) is an OR condition of ICB and MDESEL (mode select) which is a result of a command issued and detected on sheet three.

Command Decode

The I/O command decode logic is found on sheet three. Four types of commands are decoded. They are:

Output Command	(OCA)
Input data command	(IDA)
Output data command	(ODA)
Input status	(ISA)

These command codes are decoded by gates on the right hand side of the page.

Three other signals are also necessary to enable the command decode. They are:

DRIOFN - input/output function
DRCDFN - command/data function
DRIOSN - I/O sync

Data flow is determined by DRIOFN. If the signal DRIOFN is true (low), data is input to the CPU. IF DRIOFN is false (high), data is output from the CPU to the controller.

DRCDFN determines whether the instruction is a command or data. If DRCDFN is true (low), the instruction is data. If DRCDFN is false (high), the instruction is a command.

These lines are interrogated at I/O sync time, DRIOSN.

	DRCDFN	$\overline{\text{DRCDFN}}$
DRIOFN	INPUT DATA - IDA -	INPUT STATUS - ISA -
$\overline{\text{DRIOFN}}$	OUTPUT DATA - ODA -	OUTPUT COMMAND - OCA -

Output data command (OUDCMN) - gate XV6E06 will be made by ANDing TUISEL, DRIOSN, DRCDFN and $\overline{\text{DRIOFN}}$.

Input data command (INDCMN) - gate XV6F06 will be made by ANDing TUISEL, DRIOSN, DRCDFN and DRIOFN. The input data signal is inverted by two individual inverters which provide enable signals for the data gates on sheet five. The signals are ENID01 and ENID02 (enable input data one and two). The data is interrogated by the CPU on the trailing edge of INDCMN.

Input status command - gate XV6E08 is made by AND'ing TUISEL, DRIOSN, $\overline{\text{DRCDFN}}$ and DRIOFN. The output is inverted by two individual inverters which provide enables for the status gates on sheet five. The output of the inverters are ENIS01 and ENIS02 (enable input status one and two).

Output command - gate XU1A06 will be made by AND'ing TUISEL, DRIOSN, $\overline{\text{DRCDFN}}$ and $\overline{\text{DRIOFN}}$. There are three types of output commands:

Select
Control
Transfer Initiate

Select instruction - gate XV6D03 will be satisfied if data bits DFB00N and DFB01N are false, producing SELCTN.

Transfer initiate - gate XU2C12 will be made if DFB01N is false, DFB00 is true and MDESEL is true, producing RIOTIS (register I/O transfer initiate command).

Control instruction - gate XV6C03 is made by DFB00N false and DFB01 true.

Control command - gate XV6C06 is made by XU1A06 true (command) and CONT true.

End-of-block - gate XV6D08 is made if DFB04 is true and CTLCMD is true.

Terminate command - TERMN is generated from gate XV6D11 if DFB05 and CTLCMD are both true.

Reset data request - RSDRQN is generated from gate XU2A06 if DFB05 (terminate bit) is true, CTLCMD is true and DFB04N (EOB bit) is false.

Set service interrupt - SETSIN is generated by gate XU2A12 if DFB05 is true, CTLCMD is true and BUSY F/F XU2E08 is reset.

Interrupt strobe - INTSTB is generated from gate XU1A08 if SELCTN is false, XU1A06 (command) is true, XU2B06 is false (no EOB or terminate bit set, a result of OR gate XU2B03) and XU2D08 true. XU2D08 is true if device not busy or XV6D06 is true, which indicates a CTLCMD was issued and DFB06N was false. (Gate XV6D06 true and XV2B06 false indicates a NO-OP command was issued).

Mode select - MDESEL is generated by gate XU2C06 if XU1A06 is true (command), BUSY F/F XU2E08 is reset, and XU2B06 is false (no EOB or terminate bit set).

Clear status registers - CLSTAN is a result of inverting MDESEL through XU3D10.

Load command register - LDCMRN is generated by gate XU2D11 if XU2C06 is true and gate XV6D06 is false.

Busy - if the controller goes busy (the signal ISLM07 being provided by the user) and I/O sync is not present, BUSY F/F XU2E will be set by gate XU2D06. If the controller goes busy during I/O sync time, the BUSY F/F will be set on the trailing edge of command (XU1A06). This F/F inhibits any commands getting through while the controller is busy.

Output data buffers - Sheet four contains the output data buffers. The input to the inverters are from the driver/receiver module and are signals DFD00N through DFD15N. The output of these inverters are DFB00 through DFB15 (data from buffer). The signals are inverted one time, producing signals DFB00N through DFB15N. This allows the user to wire in the correct polarity for custom I/O interfaces.

Input data buffers - Sheet five contains the input data buffers. This produces a wire OR'ed bus for data or status. The correct gates are enabled by signals ENIS01 and ENIS02 for input status and ENID01 and ENID02 for input data.

Twisted pair connections - Sheet six contains the twisted pair connections for the I/O interface from the controller to the 3M connectors to be interfaced to the driver/ receiver module.

DIRECT MEMORY PROCESSOR

Logic for the DMP option is contained on sheet seven. There are two modes of DMP; Register file and Memory file.

A DMP command is detected by gate XU5A12. If DFB00, DFB01 and MDESEL are true, XU5A12 will go high, setting mode latch XU5E. The output of XU5E04 being low (RGIOMD), inhibits DI request from being generated by DATARS on Sheet 2. This allows the signal DATARS to generate a DMP request. If the Register I/O mode is selected, the mode latch is reset by signal RIOTIS. This insures that there will be no DMP request made and the signal RGIOMD will enable DI request to be generated on Sheet 2.

There are three ways to generate a DMP request (DRDMRN) in the Register file mode. The first request is generated when gate XU5A12 goes high (this is the same gate that sets the mode latch). The output of XU5A12 sets F/F XU5C05 through pin 3. In the register file mode, pin 2 of XU5C and pin 2 of XU4D are connected to 5VPK. If the memory file mode is used, these two pins are tied to GND, and these two methods of generating DMP request are inhibited. The output of XU5C06 goes to F/F XU4C09 and insures this F/F is reset at the initialization of DMP. The output also goes to one of the three OR conditions on gate XU2A08. The output goes to gate XU2C08, and if F/F XU4A05 is not set (indicates no DMP request in process), then gate XU2C08 is enabled. The output of XU2C08 goes to one input of NAND gate XU5F06 and if there is no DMP update queue present, gate XU5F06 will set DMP request F/F XU4G15. The output of DMP request F/F is used several places as an enable. Gate XV4C03 is enabled and the signal DRDMRN (DMP Request) is sent to the CPU via driver/receiver module. When the request can be serviced, the signal DRDMUN (DMP update queue) is sent to the controller. During this signal, gate XU4B03 will be enabled and signal DMPRQN (DMP Request) goes to sheet 1 to enable this controller's priority to be put on the bus. If this unit is highest priority, gate XU5B06 will be enabled, allowing the source ID to be put on the ID bus. The source ID tells the CPU what type of request is being made. Bits 0 and 1 indicate whether the DMP is Register file or Memory file. This is determined by the type of controller and whether the inputs to these two gates (XU4C06 and XV4C08) are tied to GND or 5VPG. Bits 2 and 3 are used to indicate one of four modes if you are in the Register file mode: 1 Input 2 Output 3 Initialize 4 Store transfer address. Also in this mode, bits 4 and 5 indicate which set of registers to be used from 20-27. In the memory file mode, bits 2-5 are used to generate 1 of 16 dedicated address. Pairs for transfer address and count.

When DMP request F/F is set, the output goes to the D input of F/F XU4A05. The first clock after Request is set, F/F XU4A05 will be set. The output of XU4A05 goes to the A/C trigger of three F/F's. This will transfer the information from the first F/F into the second rank. Since F/F XU5C05 was set by the DMP initialize, XU5C09 will be set by the pulse from XU4A05. The $\overline{Q}$ output goes to gate XU5E13. Since F/F XU4A05 was set, these two signals are AND'ed together and the output of XU5E13 resets F/F XU5C05 through OR gate XU5E10. $\overline{Q}$ output of F/F XU5C08 also goes to OR gate XU4B11 to provide the correct ID for initialize. If this unit is highest priority, DMP Request F/F is reset on the trailing edge of Update Queue. If this unit does become highest priority after Request F/F is reset, the first clock will reset F/F XU4A05.

F/F XU5C09 will stay set until the next DMP Request is made and F/F XU5C05 is not set.

The second way a DMP Request is generated is by signal DATARS (Data Request). This signal sets F/F XU4C05. Output of XU4C06 goes to one of the three inputs on OR gate XU2A08. If F/F XU4A06 is not set and there is presently not a DMP Update Queue on the line, DMP Request F/F XU4G15 will be set. DMP Request is sent to the CPU, and F/F XU4A05 will be set on the first clock following the set of the request F/F. This transfers the data request into F/F XU4C09 and resets F/F XU4C05 through AND gate XU5F11 and OR gate XU5B12. When the Update Queue is received, signal DMPRQN is sent to sheet 1 to put the priority bit on the bus. If this unit is highest priority, the Source ID bus is enabled. The direction of data flow, whether input or output, is determined by gate XU4B06. Pin 5 of XU4B is tied to a signal that indicates output. If XU4B06 is low, this will put Source ID on bus for output. If XU4B06 is high, this will put the Source ID on the bus for input.

If this unit is highest priority, and data request F/F XU4C06 is set, the D input of F/F XU4A09 will be enabled so that on the trailing edge of Update Queue F/F XU4A09 will be set providing the signal ENZERO which goes to gate XU4E08 as an enable. Also, on the trailing edge of Update Queue if this unit is highest priority, DMP Request F/F will be reset. If this unit is not highest priority, DMP Request will remain set until this unit is highest priority. F/F XU4C09 will remain set until there is a request and a Data Request is not made or an initialize DMP occurs. F/F XU4A09 will remain set until a DMP Request occurs without a data request. A terminate will occur automatically when the word count reaches zero. A terminate will be generated with an address of zero. This allows any Data Request or DMP Request in progress to be reset. This is accomplished through gate XU4E08, which is address zero, and ENZERO F/F is set. This produces signal ADDZEN (Address Zero) which goes to sheet 1,(OR gate XU1C08) to produce signal TUISEL. Output XU4E08 is inverted by XU4F04 which goes to gate XU5F03 to be AND'ed with signal TERM. The output of XU5F03 goes to OR gate XU5A08. The output of XU5A08 goes to F/F XU4C05 as a reset and also goes to DMP Request F/F XU4615 as a reset.

The third way to generate a DMP Request is by signal DMPSRS which occurs at the same time as the SI request. This request is used to store transfer address. F/F XU4D05 is set by DMPSRS, and output XU4D06 goes to OR gate XU2A08. If there is no DMP in progress (output of XU4A05) and there is presently not a DMP Update Queue on line, then DMP Request F/F XU4G15 is set. The first clock after request F/F is set causes F/F XU4A05 to be set. The output of XU4A05 transfers the store transfer address to F/F XU4D09, and also, through gate XU5F08 and OR gate XU5A06 F/F, causes XU4D05 to be reset.

When Update Queue is received, signal DMPRQN is generated and sent to sheet 1 to allow the priority bit to be put on the bus. If this unit is highest priority, the Source ID is enabled to be put on the bus by gate XU5B06. The correct ID is provided by output of F/F XU4D08. The output goes to two OR gates, XU4B08 and XU4B11. On the trailing edge of Update Queue and this unit is highest priority, DMP Request F/F will be reset. If this unit is not highest priority, DMP Request will stay set until this

unit becomes highest priority. The first clock after DMP Request is reset causes F/F XU4A05 to be reset. F/F XU4D09 (Store transfer address) will be reset when the next request is made and F/F XU4D05 is not set.

Memory parity error F/F is also contained on sheet 7. If a parity error is detected during a DMP data transfer, bit 7 (DFB07) is included in the terminate command. F/F XU4G11 is set by the leading edge of terminate command. The output (XU4G11) goes to the status gates on sheet 5 (ISLM04). The $\overline{Q}$ output goes to logic in the controller as signal MPEN and is used as an indicator that there was an error causing status bit 00 to become a zero.

TABLE 5-2

MNEMONIC LIST FOR STANDARD I/O
(GENERAL PURPOSE CONTROLLER)

MNEMONIC	DESCRIPTION	LOGIC DRAWING: 520-100106 Sheet#
CLKFB	MASTER CLOCK FROM BUFFER	3
CLKFBN	MASTER CLOCK FROM BUFFER (LOW TRUE)	3
CLSTAN	CLEAR STATUS REGISTERS	3
CTLCMD	CONTROL COMMAND	3
CONT	CONTROL INSTRUCTION DECODED	3
DAFB0N TO DAFB5N	DEVICE ADDRESS FROM BUFFER	1
DFB00 TO DFB15	OUTPUT DATA FROM BUFFER	4
DFB00N TO DFB15N	OUTPUT DATA FROM BUFFER (LOW TRUE	4
DFD00N TO DFD15N	OUTPUT DATA FROM DRIVER RECEIVER MODULE	4
DIREQN	DATA INTERRUPT REQUEST	2
DISET	DATA INTERRUPT SET	2
DISETN	DATA INTERRUPT SET (LOW TRUE)	2
DRCDFN	COMMAND/DATA FUNCTION FROM DRIVER RECEIVER MODULE	3
DRCLKN	MASTER CLOCK FROM DRIVER RECEIVER MODULE	3
DRDA0N TO DRDA5N	DEVICE ADDRESS FROM DRIVER RECEIVER MODULE	1
DRDIRN	DATA INTERRUPT REQUEST TO DRIVER RECEIVER MODULE	2
DRDIUN	DATA INTERRUPT UPDATE QUEUE FROM DRIVER RECEIVER MODULE	2
DRICBN	INITIAL CONDITION BUS FROM DRIVER RECEIVER MODULE	2
DRID0N TO DRID5N	SOURCE ID TO DRIVER RECEIVER MODULE	2
DRI0FN	INPUT/OUTPUT FUNCTION FROM DRIVER RECEIVER MODULE	3
DRI0SN	I/O SYNC FROM DRIVER RECEIVER MODULE	3
DRSIRN	SERVICE INTERRUPT REQUEST TO DRIVER RECEIVER MODULE	1
DRSIUN	SERVICE UPDATE QUEUE FROM DRIVER RECEIVER MODULE	1
DTD00N TO DTD15N	INPUT DATA TO DRIVER RECEIVER MODULE	5
ENID01 & ENID02	ENABLE DATA TO DRIVER RECEIVER MODULE	3
ENIS01 & ENIS02	ENABLE STATUS GATES TO DRIVER RECEIVER MODULE	3
IOBFB	INITIAL CONDITION BUS FROM BUFFER	2
IOBFBN	INITIAL CONDITION BUS FROM BUFFER (LOW TRUE)	2
INDCMN	INPUT DATA COMMAND	3
INTSTB	INTERRUPT STROBE	3
LDCMRN	LOAD COMMAND REGISTERS	3
MDESEL	MODE SELECT	3
OUDCMN	OUTPUT DATA COMMAND	3
RIOTIS	REGISTER I/O TRANSFER INITIATE COMMAND	3
RSDRQN	RESET DATA REQUEST	3
RSTSTN	ICB OR INSTRUCTION RESET (LOW TRUE)	2
SELCTN	SELECT INSTRUCTION DECODED (LOW TRUE)	3
SETSIN	TERMINATE COMMAND AND NOT BUSY SET SI	3
SISICNT	SERVICE INTERRUPT CONNECTED	1
SICNTN	SERVICE INTERRUPT CONNECTED (LOW TRUE)	1
SIRON	SERVICE INTERRUPT REQUEST	1

TABLE 5-2 (CONT'D)

MNEMONIC LIST FOR STANDARD I/O
(GENERAL PURPOSE CONTROLLER)

MNEMONIC	DESCRIPTION	LOGIC DRAWING: 520-100106 Sheet#
SIRQST	SERVICE INTERRUPT REQUEST SET	1
SIRSTN	SERVICE INTERRUPT RESET	1
TERM	TERMINATE COMMAND	3
TERMN	TERMINATE COMMAND (LOW TRUE)	3
TUHPRI	THIS UNIT HAS PRIORITY	1
TUISEL	THIS UNIT IS SELECTED	1
5VPA TO 5VPG	PULL UP VOLTAGE	1

MNEMONIC LIST FOR DMP

ADDZEN	DEVICE ADDRESS EQUALS ZERO	7
DMPRQN	DMP REQUEST (LOW TRUE)	7
DRDMRN	DMP REQUEST TO DRIVER RECEIVER MODULE	7
DRDMUN	DMP UPDATE QUEUE FROM DRIVER RECEIVER MODULE	7
ISLM04	STATUS BIT 04 (MEMORY PARITY ERROR)	7
MPEN	MEMORY PARITY ERROR (LOW TRUE)	7
RGIOMD	REGISTER I/O MODE	7
5VPH TO 5VPP	PULL UP VOLTAGE	7

VI. CARD READER CONTROLLER

INTRODUCTION

The card reader controller, which occupies a half plane in the Peripheral Controller Interface unit, is compatible with either the medium speed or the high speed card reader.

Medium Speed Card Reader

The Model 4411 Card Reader is a compact unit which reads standard 80 column punched cards photo-electrically at speeds of up to 300 cards per minute. It employs a vacuum picker mechanism to help reduce card wear and to facilitate the picking of worn cards. The Model 4411 provides a convenient means for rapidly loading programs and input data for batch processing and real-time system applications.

The card reader incorporates extensive self check and error check features for dependable operation over a wide range of environmental conditions. The reader may be operated up to fifteen feet away from the controller which is located in the PCI.

High Speed Card Reader

The Model 4412 is a heavy duty card reader which contains all of the features of the Model 4411 described previously, but reads cards at speeds up to 1000 cards per minute.

Specifications - Model 4411 Card Reader

Reading Rate - 300 cards per minute
Card Type - 80 column cards (EIA Standard RS-292, January 1964)
Coding - 12 bit or 8 bit transitional code upon command
Hopper Capacity - 600 cards
Stacker Capacity - 600 cards
Card Feeding Mechanism - Vacuum picker
Cable Length - 15 feet
Reader Dimensions - 11 inches high, 19-1/4 inches wide, 14 inches deep
Weight - 68 pounds
Environmental Conditions
    Operating Temperature - 32° to 125°F
    Relative Humidity - 30% to 90%
Power Requirements - 115 VAC($\pm$10VAC), 60 Hz $\pm$3 Hz Single Phase
    Starting Current - 9.5 amps
    Run Current - 4.0 amps

Specifications - Model 4412 Card Reader

Reading Rate - 1000 cards per minute
Card Type - 80 column cards (EIA Standard RS-292, January 1964)
Coding - 12 bit or 8 bit transitional code upon command
Hopper Capacity - 1000 cards
Stacker Capacity - 1000 cards
Card Feeding Mechanism - Vacuum picker
Cable Length - 15 feet
Reader Dimensions - 13 1/2 inches high, 23 inches wide, 18 inches deep
Weight - 86 pounds
Environmental Conditions
    Operating Temperature - 32° to 125°F
    Relative Humidity - 30% to 90%
Power Requirements - 115 VAC(±10 VAC), 60 Hz ±3 Hz Single Phase
    Starting Current - 10 amps
    Run Current - 4.5 amps

FUNCTIONAL DESCRIPTION

General

The card reader controller functions in the register I/O mode. In the register I/O mode, the data is transferred to the register by program control. The normal process of transferring data is by the use of data interrupts at the rate of one per column. If interrupts are not used, Data Ready can be monitored by testing bit eight of the status word.

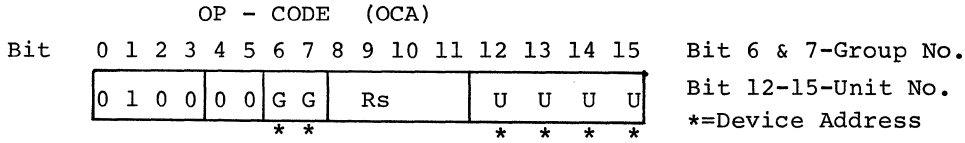
If connected, there will be a service interrupt generated by end of card or a malfunction in the device.

The data is transferred to the CPU in two modes. One mode is the binary mode. In this mode the data is an exact image of data on the card. The second mode is the translate mode, where data is converted from a twelve bit code to a modified eight bit code.

The following information describes the instructions that are used with this controller. Also provided in this description is a section on programming sequence, standard assignments and physical characteristics.

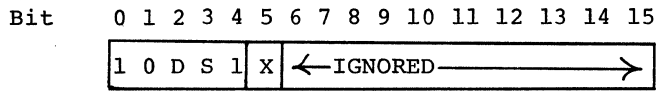
INSTRUCTIONS

Output Command



The following are contents of Rs as specified by the output command.

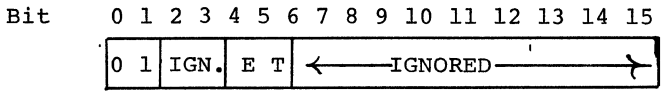
Read A Card (Transfer Initiate Format)



Bit 2 = 0 - Disconnect data interrupt and reset any stored request.
= 1 - Connect data interrupt to I/O interrupt level.
Bit 3 = 0 - Disconnect service interrupt to I/O interrupt level.
= 1 - Connect service interrupt to I/O interrupt level.
Bit 5 = 0 - Data will be transferred in the translate mode.
= 1 - Data will be transferred in the binary mode.

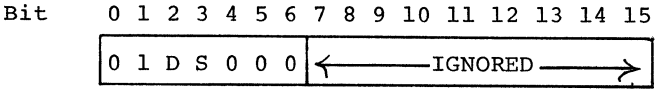
This command initiates card motion and conditions the controller for input of data in the mode specified by bit 5. If connected, a data interrupt will be generated for each of the 80 data columns. If connected, a service interrupt will be generated at end of card or as a result of an abnormal condition in the card reader.

Terminate And End Of Block



Bit 4 = 0 - No effect.
= 1 - Can be used with terminate command. If connected, a data interrupt will be generated by the EOB command. For maintenance purposes only.
Bit 5 = 0 - No effect.
= 1 - Specifies terminate command. This command will stop the transfer of data and reset any outstanding data request.

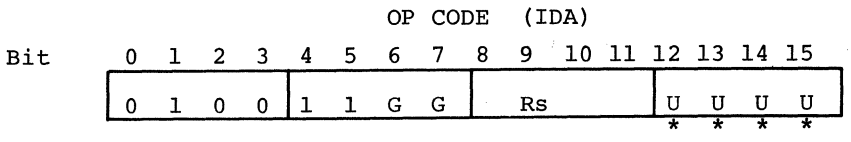
NO OP



This command is used to reset all status bits in the controller.

Bit 2 = 0 - Disconnect data interrupt and reset any stored request.
= 1 - Connect data interrupt to I/O interrupt level.
Bit 3 = 0 - Disconnect service interrupt and reset any stored request.
= 1 - Connect service interrupt to I/O interrupt level.

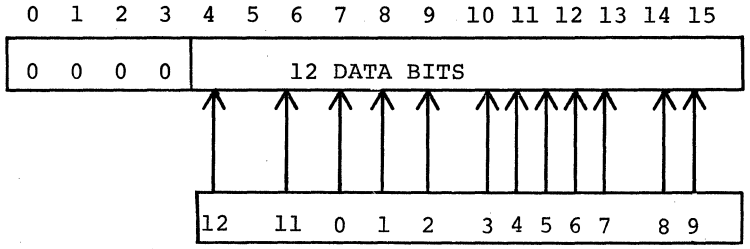
Data In



Bit 6 & 7-Group No.
Bit 12-15-Unit No.
*=Device Address

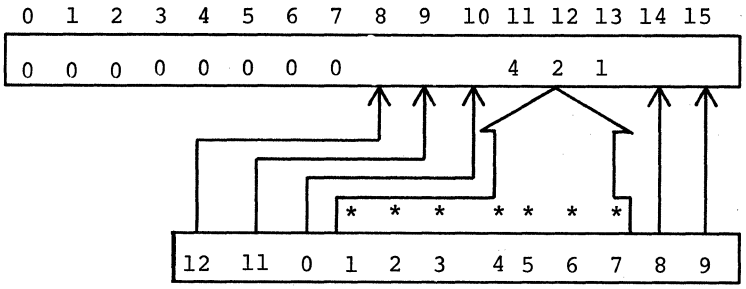
This command conditions the controller to enable data to be transferred to the register specified by Rs. The format for data is shown below:

This represents the contents of Rs in the binary mode.



Corresponding column of card data

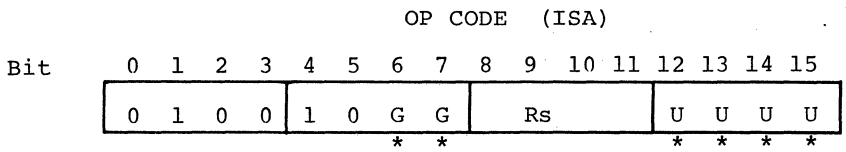
This represents the contents of Rs in the translate mode.



Column Data

*These seven bits are binary decode into the three bit positions of 11, 12 and 13.

Input Status



Bit 6 & 7-Group No.
Bit 12-15-Unit No.
*=Device Address

This command enables the controller to transfer its status to the register specified by Rs.

The status indicators are listed below:

Bit 0 = 0 - This indicates one of the following error bits is set - Bit 1,2,3.
= 1 - No errors
1 = 0 - No effect
= 1 - Overflow
2 = 0 - No effect
= 1 - light/dark check or card motion error
3 = 0 - No effect
= 1 - Inoperable — Which is a result of one or all of the following conditions:
a) Power Off
b) Pickfail
c) Hopper empty/stacker full
d) Light current or dark current or card motion error

Bit 4,5,6 - Not Used
7 = 0 - No effect
= 1 - Controller busy-indicates the controller/device are busy performing a read a card command.
8 = 0 - Data Ready-indicates data is available in the input buffer.
= 1 - No effect
9 = 0 - No effect
= 1 - Hopper empty/stacker full
10,11 - Not Used
12 = 0 - No effect
= 1 - Hold Condition — This is a condition of card reader operable and the stop button being depressed. If a command is issued it will be stored and acted on when the reset button is depressed.

13 = 0 - No effect
= 1 - Pickfail
14 = 15- Not Used

Interrupts

There are two standard interrupts provided - data and service interrupt. If connected, a data interrupt will be generated for each buffer ready (full) in the register I/O mode. The service interrupt, if connected, will be generated at the end of card or if there is some malfunction in the device.

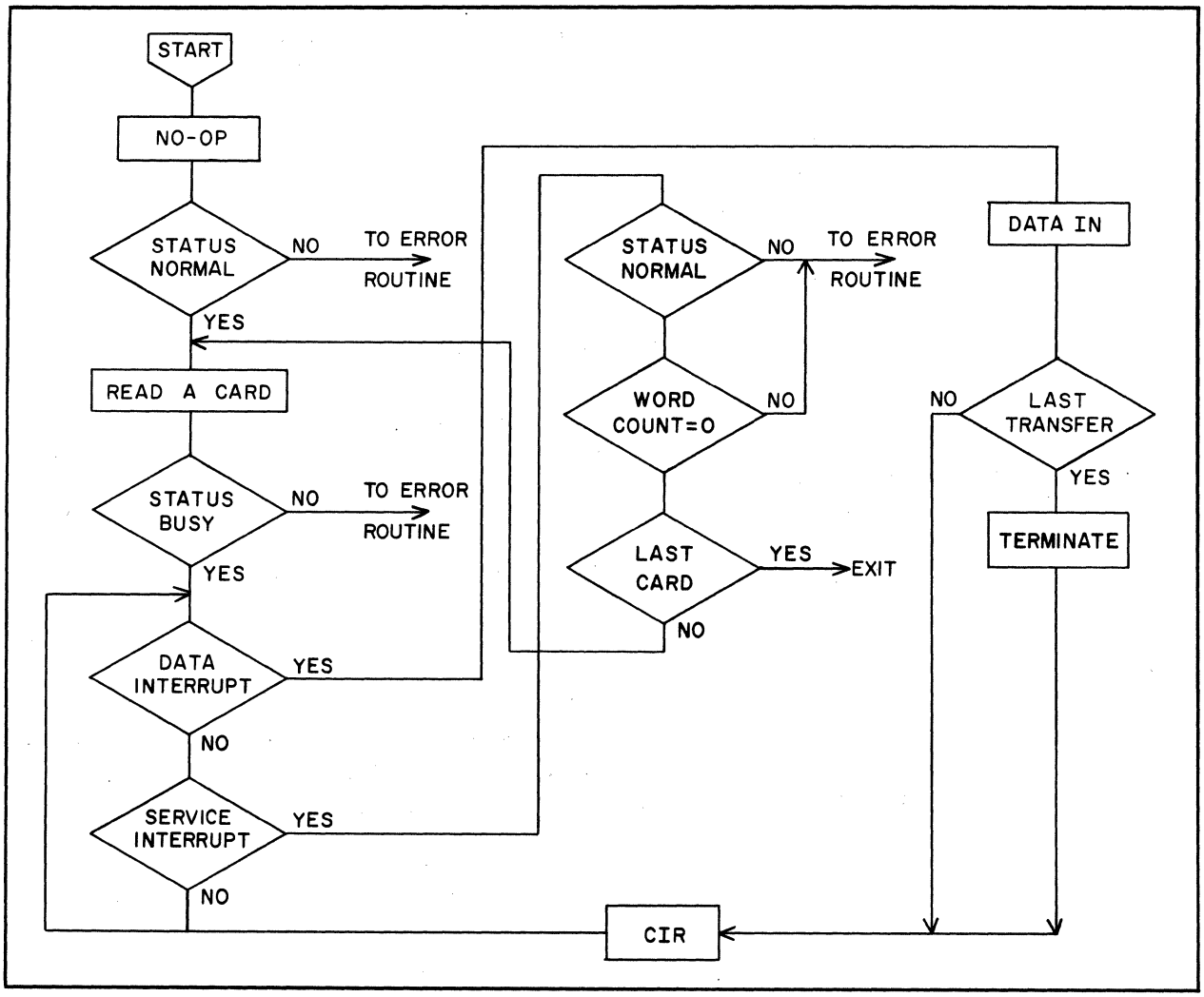
Standard Assignments

Device Address		I/O Priority	I/O Interrupt Location (Hex)	
Group	Unit		Data	Service
0	5	8	85	C5

Operator Controls

Stop Reset	Switches	Power Stop Reset	Switches
Power Read Check Pick Check Stack Check Hopper Check Stop Reset	Indicators	Power Read Check Pick Check Stack Check Hopper Check Stop Reset	Indicators

Programming Sequence Register I/O, Using Interrupts



THEORY OF OPERATION

Introduction

The card reader controller front end logic is very similar to the general purpose controller logic previously discussed. The logic drawings are located on drawing number 520-100101, sheets 1-10, in Volume II.

The process of reading information from a punched card and putting it on an I/O bus to a computer in an acceptable format is similar, regardless of the card reader model being used. Both models of the card reader feature the same operational characteristics. The following descriptions apply to both models unless otherwise noted.

Basic Functions

Basically, the following events occur in the process of retrieving data from punched cards.

1. The CPU issues a Pick Command, which initiates card motion if/when the reader is Ready.
2. The first card is picked from the input hopper. The card reader generates a clock pulse (data strobe) in sync with each punched column as it passes through the read station.
3. The CPU can expect 12 bits of parallel binary data (8 bits in translate mode) on the data bus output lines, in sync with the clock (data strobe) pulse.
4. Error lines, at the interface, signal the controller of malfunctions or possible data errors.
5. Status lines are also available at the interface for such signals as busy, ready, hopper empty/stacker full or motion check.

A logic description and timing diagram of the above functions will be illustrated in the following text.

Front End

The standard controller front end logic has been adequately described in the previous section under General Purpose Controller. The technician should refer back to it for standard signal description and operation. The first six pages of the card reader controller logic contain the standard front end. Refer to Table 6-1 at the end of this section for mnemonic signal names and descriptions.

Timing

The interface between the card reader and its controller is separated into three distinct categories. First are the card processing control/status signals. Second are the actual data bits with a clock or data strobe pulse. Third are the various error signals. Figure 6-1 is a timing diagram which should be referred to in conjunction with the following text.

Card Feed

The card read cycle is initiated by a Pick Command. The READY line (logic sheet eight) from the reader must be true before the pick command is accepted, although the command may be present at any time. READY indicates that the device is cleared of errors and ready to receive a Pick Command. READY is true when the following conditions are met.

1. Power on and run-up complete (3 seconds).
2. Input hopper loaded.
3. RESET pushbutton switch has been depressed.

Pick Command - Sheet seven

A transfer initiate command from the CPU will be decoded in the standard front end, generating the pulse RIOTIS (Register I/O Transfer Initiate) if device READY is true. The output of gate XV5M08 (RIOTIS) will set three F/F's.

F/F XV5L05	Transfer Enable
F/F XV4F09	Busy (Controller)
F/F XV4K05	Pick Command

Pick Command is inverted by gate XV2N02 and sent to the device as signal PCN (pick command), which generates the PICK pulse to the picker solenoid. After a delay (see Figure 6-1), the leading edge of the card reaches the read station, generating BSYN (true) in the device. BSYN enters the controller as CRNRDR (card in reader) and resets the Pick Command F/F XV4K05.

Pick Command and Ready must be present concurrently for at least 1 micro-second to initiate the card pick cycle. Once the cycle is initiated, Pick Command line is ignored until the BSYN signal (in device) goes false, indicating the end of the read cycle.

Busy

The output of F/F XV4K09 (Controller busy) goes to the input status gates on sheet five as signal ISLM07. Busy F/F stays set until the trailing edge of signal CRNRDR (BSYN from device) is detected through gate XV4L02. Busy (XV4K09) also goes to OR gate XV5M12 which is inverted by gate XV5J06. This ensures that Data Ready F/F is reset and stays reset while the controller is not busy.

Data Transfer

The read cycle begins when the leading edge of the card enters the read station generating BSYN in the device (CRNRDR in controller). Eighty equally spaced index marks (one per column) of six μsec duration are generated in the device while CRNRDR is present. These index marks enter the controller as signal DATSTB (Data Strobe).

The output of Transfer Enable F/F XV5L05 goes to the D input of Data Ready F/F XV4J05.

Transfer Enable F/F will stay set until a Terminate command is received or by SI request F/F XV5L09 through OR gate XV4M03 and inverter XV5J04. Transfer Enable being reset ensures that no data request will be generated if less than 80 columns of data are to be transferred.

Data requests are controlled by F/F XV4J05 (data ready). The data ready F/F is enabled by transfer enable F/F XV5L05. Data ready F/F will be set on the trailing edge of DATSTB from the device through inverter XV5J08. The $\overline{Q}$ output goes to the status gates on sheet five as signal ISLM08, low true indicating Data Ready. The $\overline{Q}$ output also goes to OR gate XV4N11 as an enable for Overflow check. The Q output goes to AND gate XV5K08, and if transfer enable is set and there is no overflow condition, signal DATARS is generated and sent to sheet 2. If Data Interrupt is connected, there will be an interrupt generated for each column of data. The data ready F/F will stay set until the signal INDCMN (Input data command) is received from the CPU. If this signal is not received before the leading edge of the next data strobe, overflow F/F XV4J09 will be set through OR gate XV5M06. The other input to OR gate XV5M06 ensures that there is an overflow check made after the 80th column of data, by using the CRNRDR signal. Gate XV4N11 ensures that the overflow F/F will stay set until the command is generated. The output of overflow F/F goes to the status gates on sheet five as signal ISLM01 (overflow). The Q output also goes to OR gate XV5N01 to indicate that there is an error by sending a low signal from XV5N01 to the status gates as signal ISLM00. The $\overline{Q}$ output goes to gate XV5K08 to inhibit any further data request.

The DATSTB pulse after being inverted by gate XV5J08 goes to gate XV4N08 to be buffered and given the drive capability to load a data buffer. Data from the device is loaded into the buffer on the trailing edge of signal LDBUF which is the output of XV4N08.

Data can be transferred in two different modes which is determined by the state of mode latch XV4N. The latch is normally in the translate mode, being cleared initially by ICB. If bit 5 is set in the transfer initiate command, the mode latch will be set by gate XV4M08. The latch will remain in this mode until the trailing edge of card, when the SI is generated and resets the latch through OR gate XV4M03 and inverter XV5J04.

Service Interrupt

A service interrupt can be generated in one of three ways.

1. The normal occurrence is at the trailing edge of CRNRDR. This is accomplished through inverter XV4L02 and pin 11 of Service Interrupt Request F/F XV5L09.
2. A SI will be generated if the device is inoperable and a command was issued. This happens through AND gate XV4M06. The output is inverted by XV4L06 and goes to OR gate XV5N04. The output DC sets Request F/F XV5L09.

3. The third way is if a terminate command was issued to the controller and the controller was not busy. This is decoded in the standard front end as signal SETSIN. This signal is inverted by gate XV4L08 and goes to the other input of OR gate XV5N04. The output of XV5N04 DC sets Request F/F XV5L09. The output of request F/F XV5L09 goes to sheet one. If the SI is connected, a service interrupt is sent to the CPU. The $\overline{Q}$ output of request F/F goes to OR gate XV4M03. The output of XV4M03 is inverted by gate XV5J04 and is used to ensure that the mode latch is reset, and that the three control F/F's transfer enable, busy and pick command are reset.

Gate XV5K06 (HOLD) is an indicator that goes to the status gates on sheet five. This gate will be true if power is on, the device is not ready and there is no read error. HOLD also results from not pushing the reset button, or by pushing the stop button, or as a result of pick fail or hopper empty/stacker full. These conditions will cause the controller to accept a command and hold it, but not act on it until the Hold condition is cleared by pushing the reset button or other operator intervention, as in the case with pick fail, or hopper empty/stacker full.

Status

Sheet 8 contains the status logic. These are the external lines from the device, interrogated by the controller.

BSYN: This signal indicates that a card has reached the read station. It will remain true until the card has advanced past the read station. It is used in the controller as signal CRNRDR (card in reader).

IMN: This signal is used to indicate data on the line and is referred to as index mark. This signal is a pulse approximately 2μs in duration. It occurs once for each of the eighty columns of data. The rate of this pulse depends on the speed of the card reader. It is used in the controller as signal DATSTB and LDBUF.

RDYN: This signal indicates that the device is ready to receive a command. RDYN signal will be true if the reset button has been depressed and there are no malfunctions such as; hopper empty/stacker full, pick fail.

MOCKN: This signal is used to indicate a motion check, which is a result of pick fail or a card hung up in the read station.

HEN: This signal indicates a hopper empty/stacker full condition.

ERRORN: This signal indicates a dark or light check error, which is a result of a faulty diode or a read check.

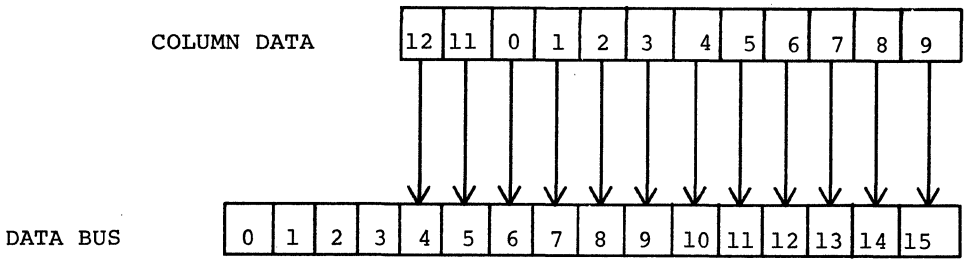
IPROFN: This signal indicates that power is on in the device.

Gate XV4M11 is an OR condition of read trouble or power off. If either of these conditions exist, the output of XV4M11 goes to the status gates on sheet five and to sheet seven as ISLM03 (device inoperable).

Sheet nine contains the data buffer and the data decode for binary or translate mode.

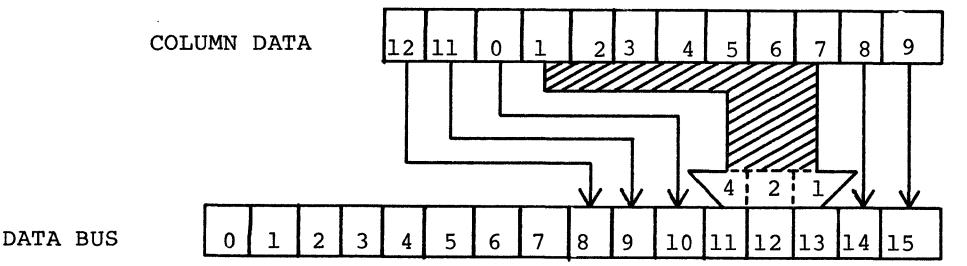
Data is loaded into the buffer by signal LDBUF which is a result of index mark from the device.

In the binary mode, the correct gates are selected by signal BINRY. In this mode, data is a direct image of data on the card in all 12 columns.

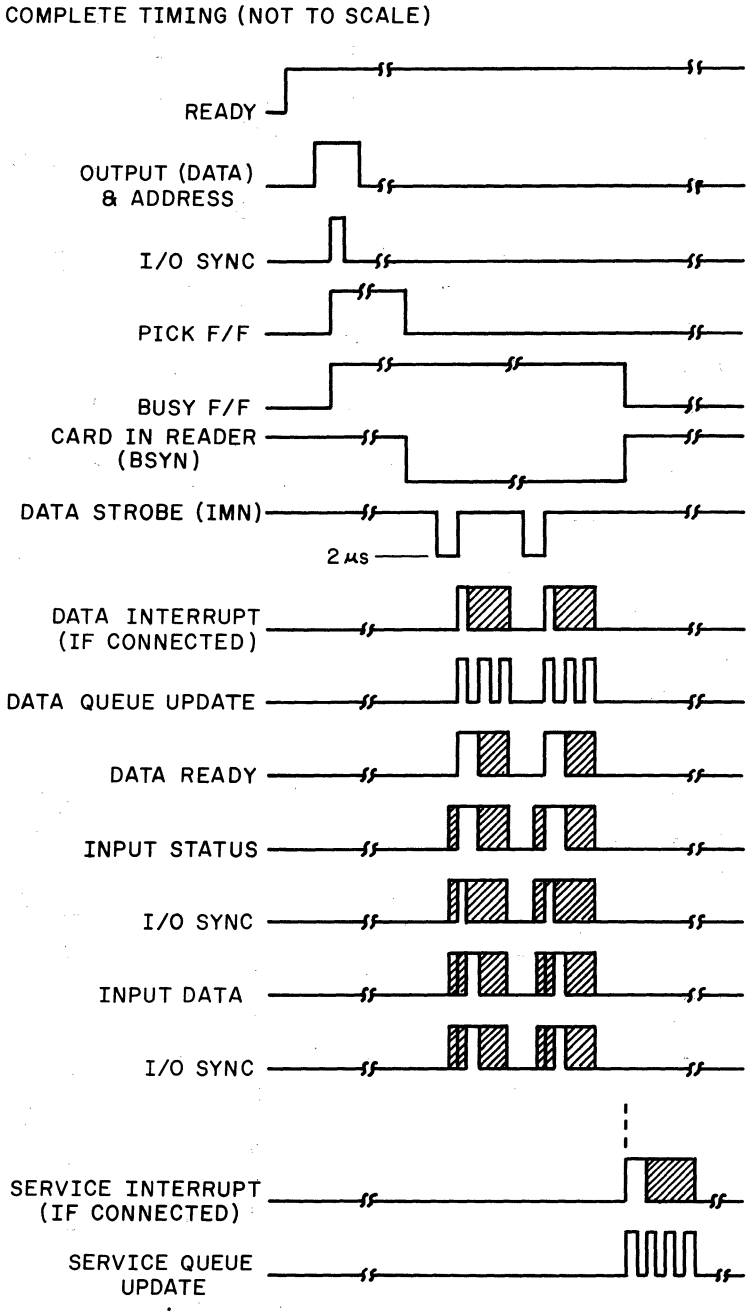


In the translate mode, the correct gates are selected by signal TRANS. In this mode of operation, data is changed from a 12 bit code to a modified 8 bit code.

Only one punch will appear in rows one through seven using 029 card code. Bits 11, 12, 13 of the buffer will contain the binary (octal) code of the punched row. For example, a punch in row one would appear as 001. A punch in row five would appear as 101.



Sheet ten contains the twisted pair connections from the controller to the 26 pin 3M connectors, for connections to the device.



Load buffer at this time.

If highest priority, interrupt will be reset. If not, interrupt will remain true until controller is highest priority.

On trailing edge, Source ID is put on bus when highest priority.

Bit eight of status word.

If interrupts are not used, this method is used to transfer data.

Data is interrogated by the mainframe I/O at the last 200 ns of I/O Sync.

If highest priority, interrupt will be reset. If not, interrupt will remain high until controller is highest priority.

Source ID is put on the bus at the trailing edge when highest priority.

FIGURE 6-1 CARD READER TIMING CHART

TABLE 6-1

MNEMONIC LIST FOR CARD READER

MNEMONIC	DESCRIPTION	LOGIC DRAWING #520-100101 Sheet#
BINRY	BINARY MODE	7
BSYN	DEVICE BUSY (CARD IN READ STATION-LOW TRUE	8
CLKFR	MASTER CLOCK FROM BUFFER	3
CLKFBN	MASTER CLOCK FROM BUFFER (LOW TRUE)	3
CLSTAN	CLEAR STATUS REGISTERS (LOW TRUE)	3
CONT	CONTROL INSTRUCTION DECODED	3
CRNRDR	CARD IN READER	8
CTLCMD	CONTROL COMMAND	3
DAFB0N TO DAFB5N	DEVICE ADDRESS FROM BUFFER	1
DATARS	DATA REQUEST	7
DATSTB	DATA STROBE	8
DFB00 TO DFB15	OUTPUT DATA FROM BUFFER	4
DFB00N TO DFB15N	OUTPUT DATA FROM BUFFER (LOW TRUE)	4
DFD00N TO DFD15N	OUTPUT DATA FROM DRIVER RECEIVER MODULE	4
DIREQN	DATA INTERRUPT REQUEST	2
DISET	DATA INTERRUPT SET	2
DISETN	DATA INTERRUPT SET (LOW TRUE)	2
DRCDFN	COMMAND/DATA FUNCTION FROM DRIVER RECEIVER MODULE	3
DRCLKN	MASTER CLOCK FROM DRIVER RECEIVER MODULE	3
DRDA0N TO DRDA5N	DEVICE ADDRESS FROM DRIVER RECEIVER MODULE	1
DRDIRN	DATA INTERRUPT REQUEST TO DRIVER RECEIVER MODULE	2
DRDIUN	DATA INTERRUPT UPDATE QUEUE FROM DRIVER RECEIVER MODULE	2
DRICBN	INITIAL CONDITION BUS FROM DRIVER RECEIVER MODULE	2
DRID0N TO DRID5N	SOURCE ID TO DRIVER RECEIVER MODULE	2
DRI0FN	INPUT/OUTPUT FUNCTION FROM DRIVER RECEIVER MODULE	3
DRI0SN	I/O SYNC FROM DRIVER RECEIVER MODULE	3
DRSIRN	SERVICE INTERRUPT REQUEST TO DRIVER RECEIVER MODULE	1
DRSIUN	SERVICE UPDATE QUEUE FROM DRIVER RECEIVER MODULE	1
DTD00N TO DTD15N	INPUT DATA TO DRIVER RECEIVER MODULE	5
DTLM04 TO DTLM15	DATA TO LOGIC MODULE	9
D01N TO D12N	COLUMN DATA FROM READER (LOW TRUE)	9
ENID01 & ENID02	ENABLE DATA TO DRIVER RECEIVER MODULE	3
ENIS01 & ENIS02	ENABLE STATUS GATES TO DRIVER RECEIVER MODULE	3
E0BLKN	END OF BLOCK COMMAND	3
ERRORN	LIGHT OR DARK CHECK FROM READER (LOW TRUE)	8
HEN	HOPPER EMPTY/STACKER FULL FROM READER (LOW TRUE)	8
ICBFB	INITIAL CONDITION BUS FROM BUFFER	2
ICBFBN	INITIAL CONDITION BUS FROM BUFFER (LOW TRUE)	2
IMN	INDEX MARK FROM READER (DATA STROBE-LOW TRUE)	8
INDCMN	INPUT DATA COMMAND	3
INTSTB	INTERRUPT STROBE	3
IPROFN	INTERFACE POWER OFF	8

TABLE 6-1

MNEMONIC LIST FOR CARD READER (CONT'D)

MNEMONIC	DESCRIPTION	LOGIC DRAWING #520-100101 Sheet#
ISLM00	STATUS BIT 00 (ERROR BIT)	7
ISLM01	STATUS BIT 01 (OVERFLOW)	7
ISLM02	STATUS BIT 02 (READ TROUBLE)	8
ISLM03	STATUS BIT 03 (INOPERABLE)	8
ISLM07	STATUS BIT 07 (BUSY)	7
ISLM08	STATUS BIT 08 (DATA READY, LOW TRUE)	7
ISLM09	STATUS BIT 09 (HOPPER EMPTY/STACKER FULL)	8
ISLM12	STATUS BIT 12 (HOLD CONDITION)	7
ISLM13	STATUS BIT 13 (PICK FAIL)	8
LDBUF	LOAD DATA BUFFER	7
LDCMRN	LOAD COMMAND REGISTERS	3
MDESEL	MODE SELECT	3
MOCKN	MOTION CHECK FROM READER (LOW TRUE)	8
OUDCMN	OUTPUT DATA COMMAND	3
PCN	PICK COMMAND TO READER (LOW TRUE)	7
PWROFN	POWER OFF	8
RDTBLN	READ TROUBLE	8
RDYN	CARD READER READY FROM READER (LOW TRUE)	8
READYN	CARD READER READY	8
RIOTIS	REGISTER I/O TRANSFER INITIATE COMMAND	3
RSDRQN	RESET DATA REQUEST	3
RSTSTN	ICB OR INSTRUCTION RESET (LOW TRUE)	2
SELCTN	SELECT INSTRUCTION DECODED (LOW TRUE)	3
SETSIN	TERMINATE COMMAND AND NOT BUSY SET SI	3
SICNT	SERVICE INTERRUPT CONNECTED	1
SICNTN	SERVICE INTERRUPT CONNECTED (LOW TRUE)	1
SIREQN	SERVICE INTERRUPT REQUEST	1
SIRQST	SERVICE INTERRUPT REQUEST SET	1
SIRSTN	SERVICE INTERRUPT RESET	1
STSIRQ	SET SI REQUEST	7
TERM	TERMINATE COMMAND	3
TERMN	TERMINATE COMMAND (LOW TRUE)	3
TRANS	TRANSLATE MODE	7
TUHPRI	THIS UNIT HAS PRIORITY	1
TUISEL	THIS UNIT IS SELECTED	1
5VPA TO 5VPG	PULL UP VOLTAGE	1

DEVICE CABLING

The following Figure 6-2 and Table 6-2 illustrates I/O cabling between the device and the controller.

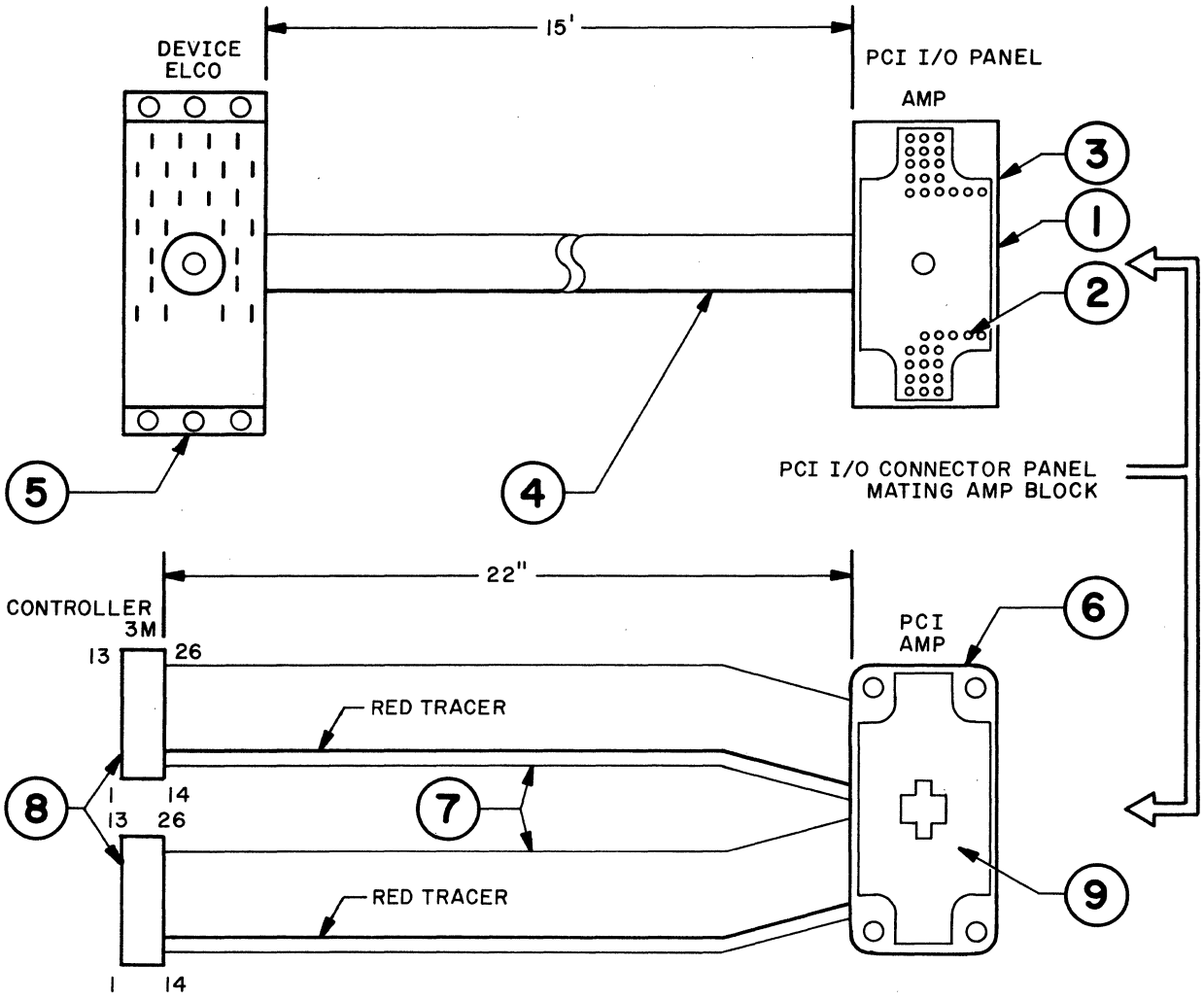


FIGURE 6-2 CARD READER I/O CABLING

LIST OF MATERIALS (CARD READER I/O CABLING)

ITEM	DESCRIPTION	QUANTITY
1	Recpt. (Amp)	1
2	Pins	39
3	Shield Assg.	1
4	Cable	15 feet
5	ELCO	1
6	Plug (Amp)	1
7	Ribbon Cable	44"
8	3M Connectors	2
9	Sockets	52

TABLE 6-2

CARD READER DEVICE CABLE

SIGNAL NAME	DEVICE ELCO CONN.	WIRE COLOR	AMP BLOCK	CONTROLLER 3M CONN. XY1C
ICL12N	A	Brown	13A	1
Ret.	F	White	14A	14
ICL11N	B	Red	13B	2
Ret.	F	White	14B	15
ICL10N	C	Orange	11A	3
Ret.	H	White	12A	16
ICL01N	D	Yellow	11B	4
Ret.	J	White	12B	17
+5V	E	Orange	9H	See Note*
ICL02N	K	Green	11C	5
Ret.	P	White	12C	18
ICL03N	L	Blue	9A	6
Ret.	R	White	10A	19
ICL04N	M	Black	9B	7
Ret.	S	White	10B	20
ICL05N	N	Brown	9C	8
Ret.	T	Blue	10C	21
ICL06N	U	Red	7A	9
Ret.	W	Blue	8A	22
ICL07N	V	Orange	7B	10
Ret.	X	Blue	8B	23
ICL08N	Y	Yellow	7C	11
Ret.	CC	Blue	8C	24
ICL09N	Z	Green	5A	12
Ret.	DD	Blue	6A	25
SPARE			5B	13
Ret.			6B	26
				XY1D
IDSN	AA	Red	13J	2
Ret.	EE	Green	14J	15
IRDYN	BB	Orange	11G	3
Ret.	FF	Green	12G	16
ITRN	HH	Brown	9G	6
Ret.	NN	Red	10G	19

*Pin "E" in ELCO Connector has orange wire connected from pair orange/red. The other end goes to 9H in the Amp Block.

TABLE 6-2

CARD READER DEVICE CABLE (CONT'D)

SIGNAL NAME	DEVICE ELCO CONN.	WIRE COLOR	AMP BLOCK	CONTROLLER 3M CONN. XY1D
IHESFN	JJ	Black	11J	5
Ret.	PP	Green	12J	18
IPFN	KK	Yellow	11H	4
Ret.	RR	Green	12H	17
IRCN	LL	Yellow	9J	8
Ret.	SS	Red	10J	21
ICIRN	MM	Brown	13H	1
Ret.	TT	Green	14H	14
SPARE			5J	13
Ret.			6J	26
IPROFN			9H	7
Ret.			10H	20
N/C			7G	9
Ret.			8G	22
SPARE			7H	10
Ret.			8H	23
SPARE			7J	11
Ret.			8J	24
SPARE			5H	12
Ret.			6H	25

VII. LINE PRINTER CONTROLLER

INTRODUCTION

The line printer controller occupies a half plane in the Peripheral Controller Interface Unit and is compatible with two line printer models. The Model 4211 and 4212 Line Printers provide high speed printing capability for listings and document preparation. Both of these fully buffered printers operate at a printing speed of 600 lines per minute with up to six-part forms.

A tape controlled vertical format unit is standard on both units and provides flexibility in form control and in data formatting. The printer enclosure provides a number of standard convenience features like paper storage and printout stacking and provides easy access for maintenance and repair. These printers contain standard self-test systems which provide the capability for off-line adjustment and maintenance of the printers without interferring with the rest of the computer system.

SPECIFICATIONS

Printing Speed - 600 lines per minute
Line Spacing - 6 lines/inch
Character Spacing - 10 characters/inch
Number of columns - Model 4211 - 132 columns/line
Model 4212 - 80 columns/line
Vertical Format Unit - 8 channel
Form Width - Model 4211 - 3-1/2 to 19-1/2 inches
Model 4212 - 8-1/2 inches
Dimensions and Weights
Model 4211 - 44 in. high, 36 in. wide, 34 in. deep, 600 lbs.
Model 4212 - 44 in. high, 26 in. wide, 30 in. deep, 450 lbs.
Environmental Requirements
Operating temperature - 0° to 55°C
Relative Humidity - 10% to 90%
Power - 117 VAC $\pm$10%, 60 Hz $\pm$1 HZ Single Phase, 7 Amps

FUNCTIONAL DESCRIPTION

General

The line printer controller functions in only the Register I/O mode. In the Register I/O mode, data is transferred to the controller under program control. The normal operation uses the data interrupt for buffer ready indication. If interrupts are not used, buffer ready can be tested by testing bit 8 in the status word.

If connected, a service interrupt is generated at the end of printing, device inoperable or at the end of paper movement.

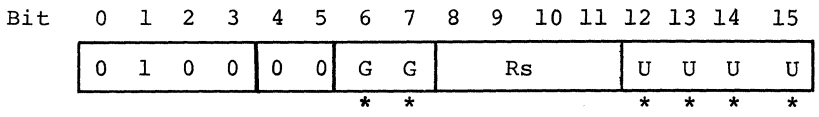
In the transfer initiate command, the printer will first move paper the number of lines decoded in the initiate command. Upon completion of paper movement, the controller is conditioned to transfer data until a terminate command is received or all 80/132 columns have been transferred. Upon completion of data transfer, a print command to the device will be generated. When printing is finished, an SI will be generated.

Paper movement can be accomplished without printing by using the output control format.

Since the line printer is buffered, there is no minimum transfer rate. The maximum transfer rate will be 20 KHz.

INSTRUCTIONS

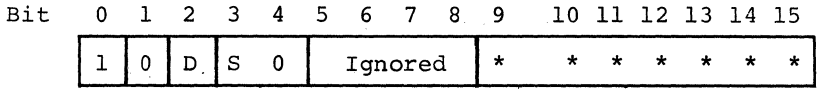
Output Command - (OCA)



*Device Address
Bits 6 & 7 = Group No.
Bits 12-15 = Unit No.

The following are contents of Rs specified in the output command.

Transfer Initiate Format (advance, transfer and print)



Bit 2 = 0 - Disconnects data interrupt and resets any active interrupt.
= 1 - Connects data interrupt to I/O interrupt level.

Bit 3 = 0 - Disconnects service interrupt and resets any active interrupt.
= 1 - Connects Service interrupt to I/O interrupt level.

Bit 4 = 0 - Output

Bits 9-15 = - These bits specify number of line feeds to be performed. The following are the formats to be used.

Bit	9	10	11	12	13	14	15	
	0	0	0	0	0	0	0	No Line Feed
	0	0	0	0	0	0	1	Skip One Line
				Thru				
	0	1	1	1	1	1	1	Skip 63 Lines
	1	0	0	0	0	0	0	Skip to Channel 1
	1	0	0	0	0	1	0	Skip to Channel 2
				Thru				
	1	0	0	1	0	0	0	Skip to Channel 8

If connected, a service interrupt will be generated upon the completion of the print cycle.

Control Format

Paper Advance

Bit	0	1	2	3	4	5	6	7 8	9	10	11	12	13	14	15
	0	1	D	S	0	0	1	Ignored	*	*	*	*	*	*	*

Bit 2 = 0 - Disconnects data interrupt and resets any active interrupt.
= 1 - Connects data interrupt to I/O interrupt level.

Bit 3 = 0 - Disconnects service interrupt and resets any active interrupt.
= 1 - Connects service interrupt to I/O interrupt level.

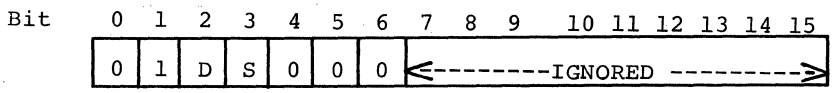
Bit 6 = 1 - Move paper per bits 9-15.

*Bits 9-15 = - These bits specify number of line feeds to be performed. The following are the formats to be used.

Bit	9	10	11	12	13	14	15	
	0	0	0	0	0	0	0	No Line Feed
	0	0	0	0	0	0	1	Skip 1 Line
				Thru				
	0	1	1	1	1	1	1	Skip 63 Lines
	1	0	0	0	0	0	0	Skip to Channel 1
	1	0	0	0	0	1	0	Skip to Channel 2
				Thru				
	1	0	0	1	0	0	0	Skip to Channel 8

If connected, a service interrupt will be generated upon the completion of the paper advance.

NO OP

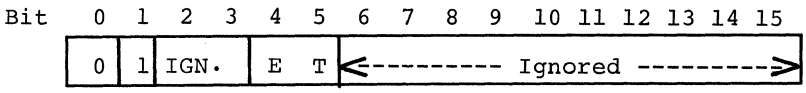


Bit 2 = 0 - Disconnects data interrupt and resets any active interrupt.
= 1 - Connects data interrupt to I/O interrupt level.

Bit 3 = 0 - Disconnects service interrupt and resets any active interrupt.
= 1 - Connects service interrupt to I/O interrupt level.

This command is used to reset all status bits in the controller.

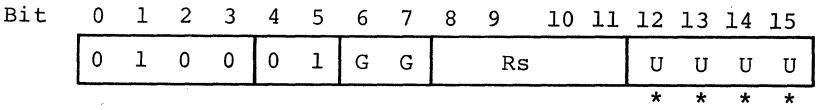
Terminate and End of Block



Bit 4 = 0 - No Effect.
= 1 - Specifies end of block. Can be used with terminate command. Normally, this command is generated by the Direct Memory Processor hardware. If connected, a data interrupt will be generated by the EOB command.

Bit 5 = 0 - No Effect.
= 1 - Specifies terminate command. This command will stop the transfer of data and reset any outstanding data request. If the controller is not busy, an SI will be generated.

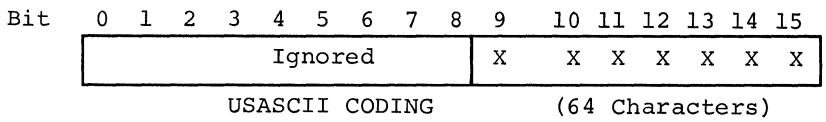
Data Out (ODA)



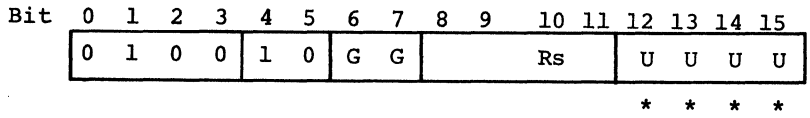
*Dev. Address
Bit 6 & 7 = Group No.
Bits 12-15 = Unit No.

This command conditions the controller to enable data to be transferred from the register specified by Rs in the DATA OUT COMMAND to the controller. The data bits that are received by the controller are shown below, and are represented by X's.

This represents contents of Rs:



Input Status (ISA)



*Dev. Address
Bit 6 & 7 = Group No.
Bits 12-15 = Unit No.

This command enables the controller to transfer its status to the register specified by Rs. The status indicators are listed below:

Bit 0 = 0 - This indicates bit 3 is set.
= 1 - No errors.

Bits 1 & 2 = Not used

Bit 3 = 0 - No effect
= 1 - Inoperable (Inoperable = Power Off)

Bit 4,5,& 6 = Not used.

Bit 7 = 0 - No effect.
= 1 - Controller busy - indicates the controller/device are busy performing a print/advance or paper advance command.

Bit 8 = 0 - Data ready, indicates buffer is empty and ready to accept data.
1 - Buffer busy.

Bit 9 = 0 - No effect.
= 1 - Paper low.

Bit 10 = 0 - No effect.
= 1 - Bottom of form.

Bit 11 = Not used.

Bit 12 = 0 - No effect.
= 1 - Hold Condition. This condition exists when power is on and the stop button on the printer has been depressed. This condition will exist until the Run button on the printer has been depressed. While in the hold contition, a command will be accepted and stored; the command will be acted on when the RUN button is depressed.

Bits 13,14, & 15 = Not used.

Interrupt

There are two standard interrupts provided - data and service interrupt. If connected, a data interrupt will be generated for each buffer ready (Empty) in the register I/O mode. Issuance of an EOB command, whether the controller is busy or not, will also generate a data interrupt.

The service interrupt, if connected, will be generated at the end of (advance, transfer, and print) command, end of paper command, or if there is some malfunction in the device during the execution of either of the above commands. Issuance of a terminate command while the controller is not busy will also cause the immediate generation of an SI.

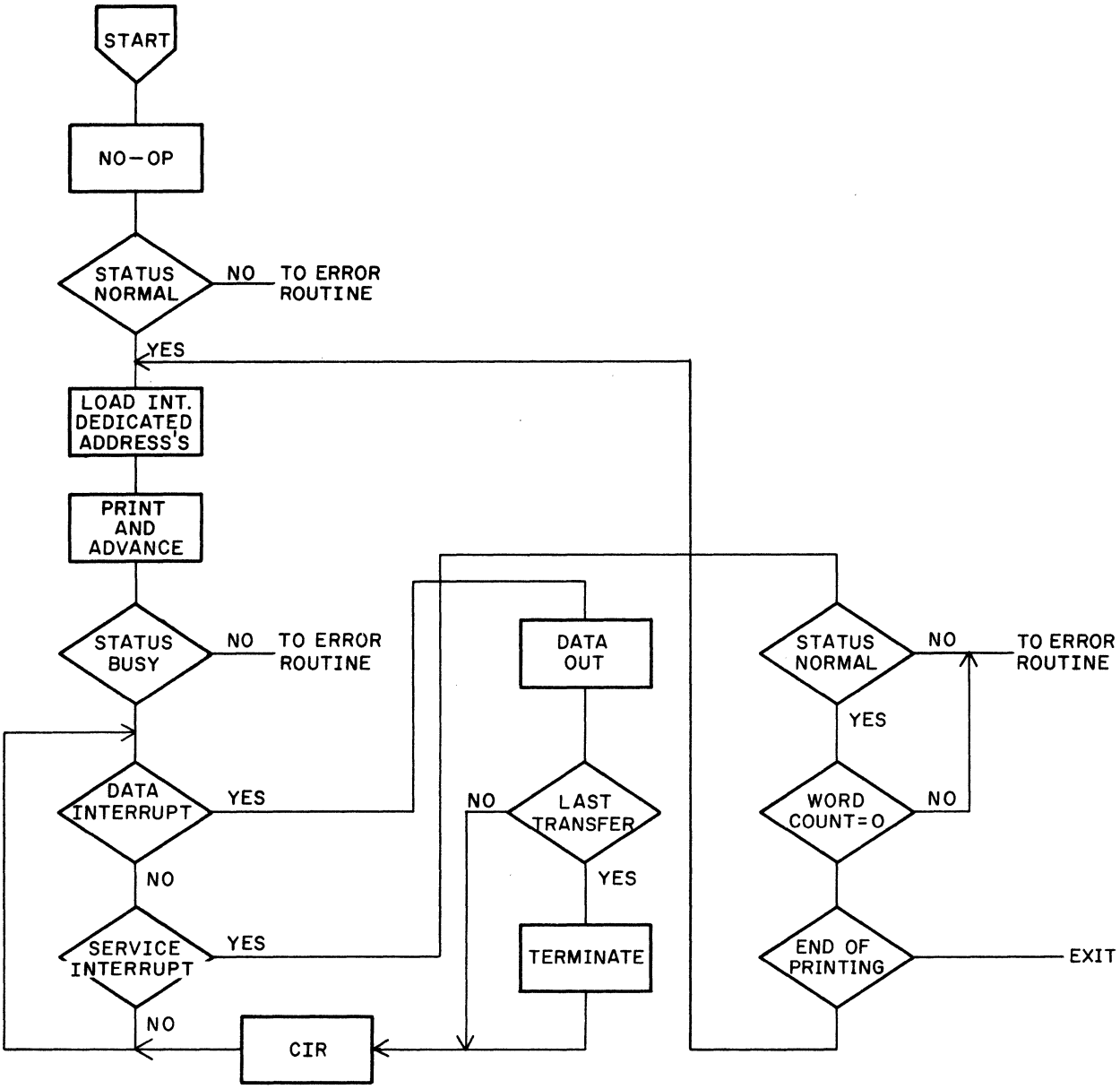
Standard Assignments

Device Group	Address Level	I/O Priority	I/O Interrupt Location (Hex) Data	Service
0	7	11	87	C7

Operator Controls

Switches	Indicators
On	On
Off	Off
Run	Run
Stop	Stop
Home	Alarm
1 Line	

PROGRAMMING SEQUENCE



THEORY OF OPERATION

INTRODUCTION

The line printer controller front end logic is very similar to the general purpose controller logic previously discussed. The logic drawings for the line printer are located on drawing number 520-100103, sheets 1-11 in Volume II.

Both models of the line printer feature the same operational characteristics. The following description applies to both models unless otherwise noted.

Basic Functions

The operation of the line printer consists of four basic cycles. These are:

1. Paper feed command
2. Paper feed
3. Load data command
4. Print

Timing

Figure 7-1 is a timing diagram of the line printer basic cycles. Following the print cycle, which is completely under control of the device electronics, a paper feed command can be sent from the controller and be accepted by the printer. During the time required for the printer hammers to recover from the previous print cycle, paper feed and paper settling is completed and a new line of data is loaded into the printer buffer.

Motion Commands

Paper feed is accomplished in one of two ways. One is a Control command for paper movement only and the second is as part of the Transfer Initiate command. The number of lines for paper to be moved is contained in bits 9 through 15 of either command. (If bit 9=1, skip to channel N under control of the vertical format unit).

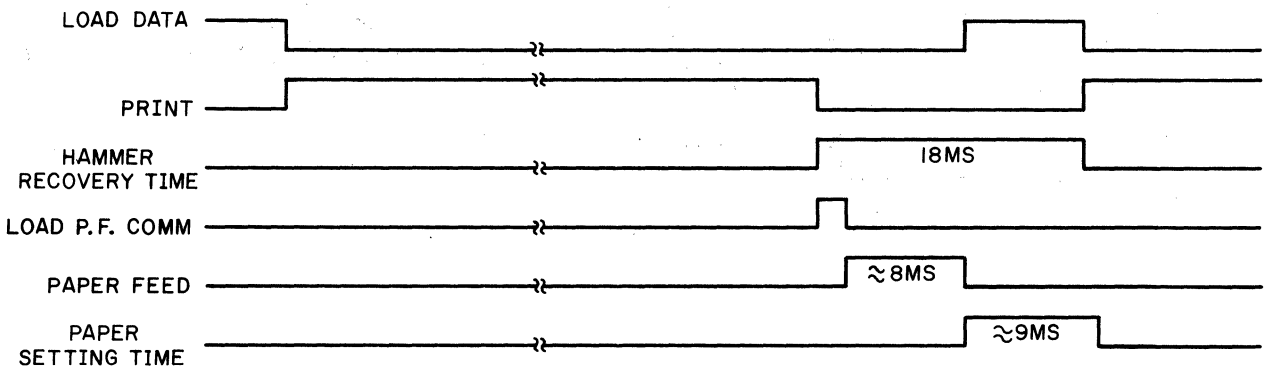


FIGURE 7-1 BASIC TIMING

Logic drawing 520-100103 sheet 7 contains the control logic for paper feed, transfer initiate and service interrupt.

Control Command - Paper feed F/F XV6L05 is set by the 'AND' condition of OPERABLE, and pulse LDCMRN (load command register) on gate XV5L03. BUSY latch, XV6K03 is also set by the output of gate XV5L03. The paper feed F/F will remain set until the trailing edge of SEND DATA (SNDATN) from the line printer. The output of paper feed F/F XV6L06 is inverted by gate XV2P03 and sent to the line printer as a paper feed command (PFDCMD). If the paper feed is a control command, there will be a pulse generated out of gate XV5M12, which goes to gate XV5N08 as one of two 'OR' conditions. The output of XV5N08 sets F/F XV5K05 through the DC set. This F/F conditions the SI F/F so that when the line printer goes ready after the paper feed is complete, the SI F/F will be set through the AC trigger. SI being set indicates that the line printer is ready to accept another command.

Busy - Busy is reset by the output of XV2K11 which is a condition of RDYSS (ready single shot) and the output of F/F XV5K05, which preconditioned the SI flip-flop. Output of XV2K11 goes to gate XV3J11 as one of two OR conditions. The output of XV3J11 is inverted by gate XV2P11 and is used as the BUSY reset.

Transfer Initiate - In a transfer initiate command, the paper feed F/F and Busy are set in the same manner as in the control command. The advance initialize command latch is set by XV6K11 which is Operable and the pulse RIOTIS (register I/O transfer initiate.) The output of latch XV5L11 conditions the D input of XV5K02. When the printer has completed the paper feed, the SI pre-condition F/F XV5K05 is set by the output of gate XV3P06 which is RDYSS and the controller not in the hold condition, through XV5K03. This conditions the SI F/F so that when the printer goes ready after the print cycle is complete, the SI F/F will be set by gate XV3P06 through XV5K11. Busy will be reset as described in the control command.

After the paper feed cycle is complete, the print command F/F is set and signal FSTRQN (first data request) is developed through gate XV5L06. This gate is made as a result of command latch and the inverted output of gate XV3P06 which is a result of the printer going ready after the paper feed command has been completed. The output of XV6L08 is buffered through gate XV2P06 and goes to the printer as signal PNTCMD (Print Command). The print F/F will remain set until the buffer in the printer is full and SEND DATA goes away, resetting the F/F through pin 11 of XV6L. If there is less data transferred than the maximum buffer size in the printer, the Print F/F is reset through pin 13 by signal RESETN. This is a result of F/F XV5J being set by TERMN (terminate command). If there are no data strobes in progress, gate XV5N06 goes high, is inverted, then OR'ed through gate XV5N01 resulting in signal RESETN. The print F/F being reset is the go ahead to the printer to print the information stored in its buffer.

Service Interrupt - The SI flip flop being set as described above also sets through the OR condition of gate XV5N11. Signal SETSIN is the result of a terminate command being issued while the controller was not busy. The other set is through gate XV6K08, which is device inoperable and a command issued to the controller.

The hold F/F is set by gate XV3P03, which says hold (ISLM12) and a command issued. The hold F/F is used so that any of the gates that use RDYSS will not be erroneously set or reset when going from the hold condition to the non-hold condition when the printer goes ready. Hold will be explained later in this description.

Data Transfer - Sheet 8 contains the control logic for making Data Request and developing the Data Strobe pulse to the printer.

Data Request F/F XV4K is set by FSTRQN through pin 10. This is First Data Request. If connected, a data interrupt is generated by DATARS. If not connected, Data Ready can be tested by status bit 8 (ISLM08).

In response to the data request, an OUDCMN (output data command) is generated by the CPU. This signal resets Data Request F/F and sets counter enable F/F XV4K through pin 4. If Print Command is set and Send Data is enabled from the printer, gate XV5M08 will go low enabling the counter to begin counting. The counter is incremented by CLKFB (Clock From Buffer). OUDCMN also insures DATA STROBE ENABLE F/F is in the set condition through gate XV3K12. When the counter reaches count four, a data strobe pulse is generated through gate XV3P08, buffered by gate XV2P08 and sent to the printer as DATSTB. This allows the line printer to strobe in the data that was stored in our buffer as part of the OUDCMN. When the count reaches count 8, the data strobe enable F/F is set by this count going high on pin 11 of XV4L. This insures that as the counter continues, no other data strobe will be generated until another output data is issued. The data request is mad at two different rates, according to whether the data interrupt is connected or not. If the interrupt is not connected, XV4M08 will go low when the counter reaches count 8. If the interrupt is connected, XV4M08 will go low at count 128. This signal resets the counter enable F/F and makes a data request if the print F/F is still set by trigger on Pin 11 of XV4K. This operation will continue until the buffer is full or a terminate is received.

When the paper feed command is set, PPRCMD and Send Data from the printer allows the counter to begin to count. When the counter reaches count 4 a data strobe is sent to the printer and the number of lines to be fed which was contained in the least significant 7 bits and stored in our buffer will be stored in the printer buffer and acted on. PPRCMD and send data will go away after the printer detects the data strobe, thus resetting and stopping the counter. The data strobe enable F/F XV41 is insured to be in the reset condition by the signal LDCMRN.

Data Buffer - Sheet 9 contains the data buffer. When a control command is detected by signal LDCMRN, the data contained in the least significant 7 bits, which is the number of line feeds to be performed, is strobed into the buffer on the trailing edge and remains in the buffer until a new control command or OUDCMN is detected. When an output data command is detected, the data contained in the least significant seven bits, which is the data to be printed, is strobed into the buffer on the trailing edge. The output of the storage buffer is buffered through gates and sent to the printer as BUS1 through BUS 7. The line printer looks at this BUS during the Data Strobe.

Status Logic - Sheet 10 contains the status logic from the printer. Bottom of form

F/F XV5J05 is set when CHL08N (Channel 8 VFU) is detected through gate XV3L11 which is channel 8 and 6LNSBN (6 lines per inch strobe) from the printer through pin 3 of XV5J. The output goes to the status gates on sheet 5. When paper is advanced past CHL08N, the F/F is reset by gate XV3J03 through an OR condition and inverted. XV3J03 is a result of CHL08N not present and a 6LNSBN from the printer.

RUNLPN & RUNLP - is the output of the Run button on the control panel of the line printer. When the condition exists that the printer is in the stop mode and power is on, the gate XV3L08 will be satisfied giving a HOLD condition. In this state the controller will accept a command, store it, and act on it when the RUN button is depressed. If power is off, gate XV3J08 will be satisfied having a low output. This indicates that the printer is inoperable. Output of inverter XV2J goes to the status gates on sheet 5 and gates on sheet 7. When power is on, the output of gate XV3J will be high, whether in the run or stop mode. This indicates that power is on and the printer is operable. Operable goes to the status gates as ISLM00 and to sheet 7, gate XV5L03.

PRTRDY - is an indication from the printer that it is ready to accept a paper feed or a print command. When one of these two functions is in progress, PRTRDY will be low. When the printer goes ready (SSXV3N) is enabled as long as the RUN switch is depressed and XV3L06 is high into XV3N05. The output of the SS is an approximate 200NS pulse used on sheet 7.

SENDAT - is an indication from the printer that it is ready to accept data in either a paper feed or data format.

PPRLOW - is a signal to indicate paper in the printer is low and should be acted on by the operator. The output goes to the status gates on sheet 5 as ISLM09.

Twisted Pair List - Sheet 11 contains the twisted pair list from the controller to the device.

TABLE 7-1

MNEMONIC LIST FOR LINE PRINTER

MNEMONIC	DESCRIPTION	SHT#
BUS1 TO BUS2	DATA BUS TO PRINTER	9
CHL08N	VERTICAL FORMAT CHANNEL 08 (BOTTOM OF FORM)	10
CLKFB	MASTER CLOCK FROM BUFFER	3
CLKFBN	MASTER CLOCK FROM BUFFER (LOW TRUE)	3
CLSTAN	CLEAR STATUS REGISTERS	3
CONT	CONTROL INSTRUCTION DECODED	3
CTLCMD	CONTROL COMMAND	3
DAFBON TO DAFB5N	DEVICE ADDRESS FROM BUFFER	1
DATARS	DATA REQUEST	8
DATSTB	DATA STROBE TO PRINTER	8
DFB00 TO DFB15	OUTPUT DATA FROM BUFFER	4
DFB00n TO DFB15N	OUTPUT DATA FROM BUFFER (LOW TRUE)	4
DFD00N TO DFD15N	OUTPUT DATA FROM DRIVER RECEIVER MODULE	4
DIREQN	DATA INTERRUPT REQUEST	2
DISET	DATA INTERRUPT SET	2
DISETN	DATA INTERRUPT SET (LOW TRUE)	2
DRCDFN	COMMAND/DATA FUNCTION FROM DRIVER RECEIVER MODULE	3
DRCLKN	MASTER CLOCK FROM DRIVER RECEIVER MODULE	3
DRDA0N TO DRDA5N	DEVICE ADDRESS FROM DRIVER RECEIVER MODULE	1
DRDIRN	DATA INTERRUPT REQUEST TO DRIVER RECEIVER MODULE	2
DRDIUN	DATA INTERRUPT UPDATE QUEUE FROM DRIVER RECEIVER MODULE	2
DRICBN	INITIAL CONDITION BUSS FROM DRIVER RECEIVER MODULE	2
DRID0N TO DRID5N	SOURCE ID TO DRIVER RECEIVER MODULE	2
DRIOFN	INPUT/OUTPUT FUNCTION FROM DRIVER RECEIVER MODULE	3
DRIOSN	I/O SYNC FROM DRIVER RECEIVER MODULE	3
DRSIRN	SERVICE INTERRUPT REQUEST TO DRIVER RECEIVER MODULE	1
DRSIUN	SERVICE UPDATE QUEUE FROM DRIVER RECEIVER MODULE	1
DSBNPN	DATA STROBE IN PROCESS	8
DTD00N TO DTD15N	INPUT DATA TO DRIVER RECEIVER MODULE	5
ENID01 & ENID02	ENABLE DATA TO DRIVER RECEIVER MODULE	3
ENIS01 & ENIS02	ENABLE STATUS GATES TO DRIVER RECEIVER MODULE	3
EOBLKN	END OF BLOCK COMMAND	3
FSTRQN	FIRST DATA REQUEST	7
ICBFB	INITIAL CONDITION BUSS FROM BUFFER	2
ICBFBN	INITIAL CONDITION BUSS FROM BUFFER (LOW TRUE)	2
INDCMN	INPUT DATA COMMAND	3
INTSTB	INTERRUPT STROBE	3
ISLM00	STATUS BIT 00 (ERROR BIT SET-LOW TRUE-)	10
ISLM03	STATUS BIT 03 (INOPERABLE)	10
ISLM07	STATUS BIT 07 (BUSY)	7
ISLM08	STATUS BIT 08 (DATA READY-LOW TRUE-)	8

TABLE 7-1

MNEMONIC LIST FOR LINE PRINTER (CONT'D)

MNEMONIC	DESCRIPTION	SHT#
ISLM09	STATUS BIT 09 (PAPER LOW)	10
ISLM10	STATUS BIT 10 (BOTTON OF FORM)	10
ISLM12	STATUS BIT 12 (HOLD CONDITION)	10
LDCMRN	LOAD COMMAND REGISTERS	3
MDESEL	MODE SELECT	3
OUDCMN	OUTPUT DATA COMMAND	3
PFDCMD	PAPER FEED COMMAND TO PRINTER	7
PNTCMD	PRINT COMMAND TO PRINTER	7
PPRCMD	PAPER ADVANCE COMMAND	7
PPRLOW	PAPER LOW FROM PRINTER	10
PRTCMD	PRINT COMMAND	7
PRTRDY	PRINTER READY FROM PRINTER	10
RDYSS	READY SINGLE SHOT	10
RDYSSN	READY SINGLE SHOT (LOW TRUE)	10
RESETN	TERMINATE/SI/ICB	7
R10TIS	REGISTER I/O TRANSFER INITIATE COMMAND	3
RSDRQN	RESET DATA REQUEST	3
RSTSTN	ICB OR INSTRUCTION RESET (LOW TRUE)	2
RUNLP	RUN BUTTON DEPRESSED	10
RUNLPN	RUN BUTTON DEPRESSED (LOW TRUE)	10
SELCTN	SELECT INSTRUCTION DECODED (LOW TRUE)	3
SENDAT	SEND DATA FROM PRINTER	10
SETSIN	TERMINATE COMMAND AND NOT BUSY,SET SI	3
SICNT	SERVICE INTERRUPT CONNECTED	1
SICNTN	SERVICE INTERRUPT CONNECTED (LOW TRUE)	1
SIREQN	SERVICE INTERRUPT REQUEST	1
SIRQST	SERVICE INTERRUPT REQUEST SET	1
SIRSTN	SERVICE INTERRUPT RESET	1
SNDAT	SEND DATA	10
SNDATN	SEND DATA (LOW TRUE)	10
STSIRQ	SET SI REQUEST	7
TERM	TERMINATE COMMAND	3
TERMN	TERMINATE COMMAND (LOW TRUE)	3
TUHPRI	THIS UNIT HAS PRIORITY	1
TUISEL	THIS UNIT IS SELECTED	1
5VPA TO 5VPG	PULL UP VOLTAGE	1
6LNSBN	SIX LINE PER INCH STROBE	10

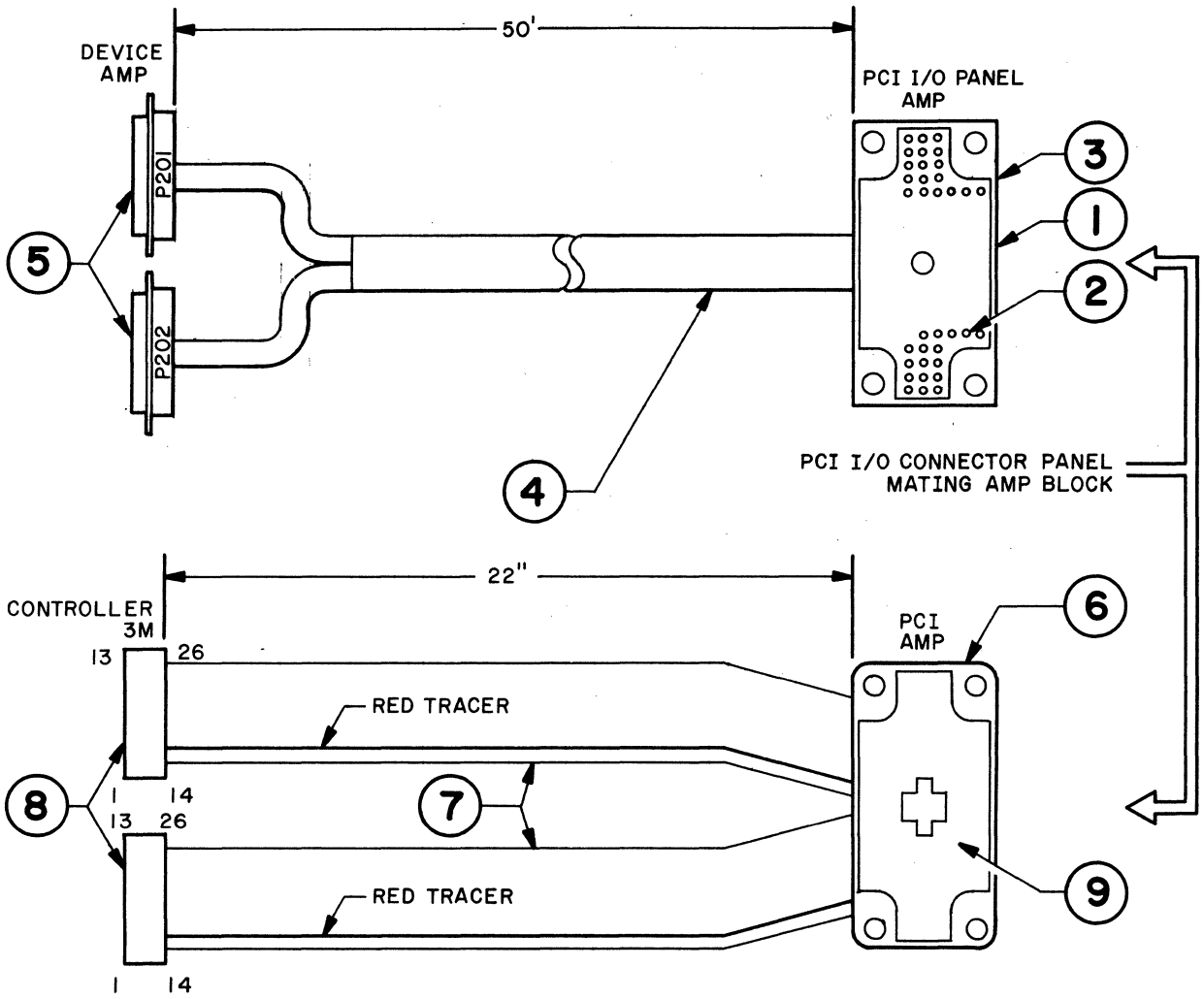


FIGURE 7-2 Line Printer Device Cabling to PCI

LIST OF MATERIALS

ITEM	MCS NUMBER	DESCRIPTION	QUANTITY
1	667-200000-001	Receptacle (AMP)	1
2	667-200000-201	Pins	36
3	667-200000-601	Shield Assy.	1
4	668-600001-001	Cable	50 ft.
5	667-200009-001	Amphenol Connector	2
6	667-200000-101	Plug (AMP)	1
7	668-600000-001	Ribbon Cable	44"
8	667-200003-001	3M Connector	2
9	667-200000-301	Socket	52

TABLE 7-2

LINE PRINTER CABLING

SIGNAL NAME	DEVICE AMP CONN. P201	WIRE COLOR	AMP BLOCK	CONTROLLER 3M CONN. XY1C
RUN	1	Brown	13A	1
Ret.	14	White	14A	14
PRTRDY	2	Red	13B	2
Ret.	15	White	14B	15
SPARE			11A	3
Ret.			12A	16
SENDAT	4	Yellow	11B	4
Ret.	17	White	12B	17
RUNN	5	Green	11C	5
Ret.	18	White	12C	18
SPARE			9A	6
Ret.			10A	19
6LNSBN	20	Black	9B	7
Ret.	7	White	10B	20
SPARE			9C	8
Ret.			10C	21
SPARE			7A	9
Ret.			8A	22
CHL08N	23	Orange	7B	10
Ret.	10	Blue	8B	23
SPARE			7C	11
Ret.			8C	24
PPRLOW	12	Green	5A	12
Ret.	25	Blue	6A	25
SPARE			5B	13
Ret.			6B	26
	P202			XY1D
AUTOLF	1	Brown	13H	1
Ret.	14	Green	14H	14
SPARE			13J	2
Ret.			14J	15
PFDCMD	3	Orange	11G	3
Ret.	16	Green	12G	16
PNTCMD	4	Yellow	11H	4
Ret.	17	Green	12H	17
DATSTB	5	Black	11J	5
Ret.	18	Green	12J	18
BUS 1	6	Brown	9G	6
Ret.	19	Red	10G	19

TABLE 7-2

LINE PRINTER CABLING (Cont'd)

SIGNAL NAME	DEVICE AMP CONN. P202	WIRE COLOR	AMP BLOCK	CONTROLLER 3M CONN. XY1D
BUS 2	7	Orange	9H	7
Ret.	20	Red	10H	20
BUS 3	8	Yellow	9J	8
Ret.	21	Red	10J	21
BUS 4	9	Black	7G	9
Ret.	22	Red	8G	22
BUS 5	10	Brown	7H	10
Ret.	23	Black	8H	23
BUS 6	11	Brown	7J	11
Ret.	24	Blue	8J	24
BUS 7			5H	12
Ret.			6H	25
SPARE			5J	13
Ret.			6J	26

VIII. MAGNETIC TAPE CONTROLLER

INTRODUCTION

Models

The Model 4151 and 4152 Magnetic Tape Units provide IBM compatible 7 and 9 track magnetic tape systems for data storage and program entry. The 4151 and 4152 Magnetic Tape Units operate with the Model 4150 Controller. Up to four magnetic tape units can share a single controller and they are interconnected by a total of up to 25 feet of device cable. The four magnetic tape units can be any combination of 7 and 9 track units. These high performance magnetic tape systems feature a tape speed of 45 IPS with a density of 800 BPI. The tape units handle 10 1/2 inch reels, feature a single capstan drive with a velocity servo system, and are furnished in a rack mountable enclosure.

Both models offer the dual gap head read after write feature. These models conform to the NRZI format and except for minimum block length they are ANSI and IBM compatible.

Specifications

MODEL	TRACKS	DENSITY	TRANSFER RATE CHAR/SEC
4151	9	800	36 KHZ
4152	7	556, 800	25.02 KHZ, 36 KHZ

Tape Velocity - 45 IPS
Recording Mode - NRZ1 IBM compatible
Tape - Computer grade 0.5 inch wide, 1.5 mil thick
Rewind Speed - 150 IPS
Reel Size - 10 1/2 inch
Dimensions - 24 inches high, 19 inches wide, 11 inches deep
Weight - 100 pounds
Environmental Requirements
- Operating Temperature - 40° to 90°F
- Non-operating Temperature - 30° to 140°F
- Relative Humidity - 15% to 95% noncondensing
- Altitude - 0-20,000 feet

Power - 117 VAC ± 10%, 60 HZ ± 2 HZ single phase, 500 watts

FUNCTIONAL DESCRIPTION

General

The mag tape controller allows a maximum of four independently addressable tape transports of the same speed (45 IPS) to be attached by a simple "daisy-chain" connection

to a common interface. These can be of the same type, or a mixture of 7 and 9 channel.

GENERAL DESCRIPTION

Mag tape transfer rates normally require the controller to operate with a Memory File DMP channel. Also, a Memory File DMP channel is required when mag tapes are interfaced to standard MAX software operating systems. However, the controller may also operate in the programmed I/O mode.

Dynamic gapping in lieu of start/stop operation is maintained if the software responds to a service interrupt within a specified period of time. The new command must be of the same type, same device, and direction as the previous one or the active transport will come to a complete stop before starting the new operation.

The controller features rewind complete detection logic thereby maintaining maximum efficiency on multi-unit systems.

Four words of buffering are provided by the controller to compensate for possible I/O latency conditions.

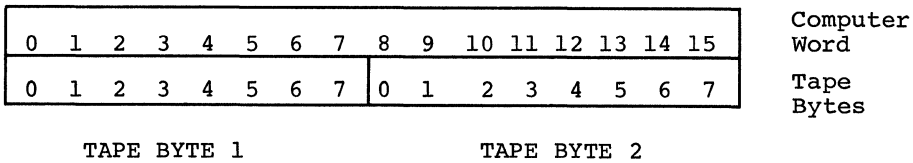
The controller occupies two standard half pages in a hardware logic frame.

DATA FORMATS

Two modes of word assembly/disassembly are provided for tape byte/character packing. These modes are binary and interchange. Binary is the most efficient mode and provides normal transfer for internally generated tapes. Interchange is not as efficient, but it provides input transfer for externally generated 7 track tape, and output for tapes to be read by external 7 track machines.

Binary Mode

9 TRACK WRITE

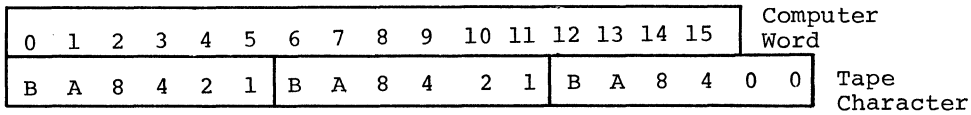


When writing on 9 track drives, transfer is implemented by writing the most significant byte as the first tape byte and the least significant byte as the second tape byte.

Since the mag tape controller operates in a word transfer mode only, this implies that only an even number of tape bytes may be written in a block.

If the selected unit is 9 track then the binary mode is automatically selected.

7 TRACK WRITE

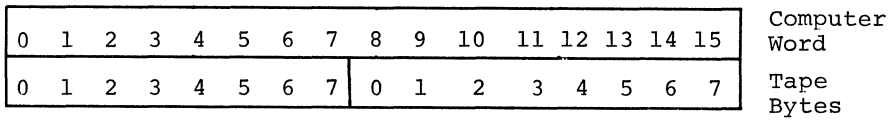


When writing on 7 track drives, transfer is implemented by writing the 6 upper order bits as the first tape character, the next 6 bits as the second tape character, and 4 low order bits as third tape character. Track 1 and 2 of the third character are written as zeros.

Since the mag tape controller operates in a word transfer mode only, this implies that only a multiple of three tape characters may be written in a block while in the binary mode.

If even parity is selected while writing to a 7 track transport and one of the tape characters to be written is 000000 then it is translated and written as 001010. Reverse translation does not occur in read.

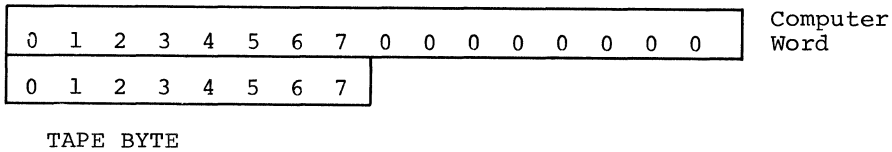
9 TRACK READ
2X Tape Bytes



When reading from 9 track drives, transfer is implemented by storing the first tape byte encountered as the most significant byte in a memory word and the second as the least significant byte.

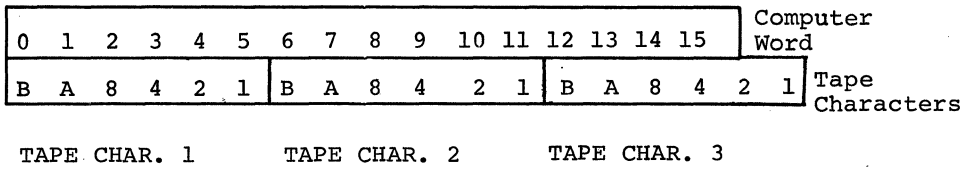
If an odd number of tape bytes are read, the last tape byte is positioned as the most significant byte and the least significant byte is set to zero of the last word. The last word appears as follows:

LAST WORD
9 TRACK READ
2X + 1 TAPE BYTES



The partial word transferred status (bit 13) is set to 1.

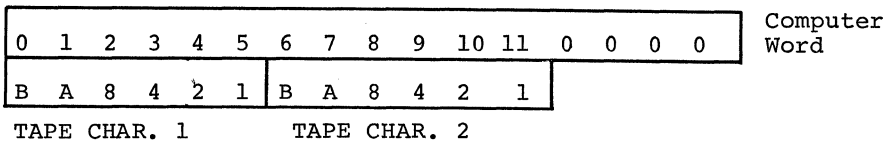
7 TRACK READ
3X TAPE CHARACTERS



When reading from 7 track drives, transfer is implemented by positioning the first tape character encountered as the 6 upper order bits, the second tape character as the next 6 bits, and the third tape character as the 4 low order bits of the computer word. Tracks 1 and 2 of every third tape character are ignored and thereby lost.

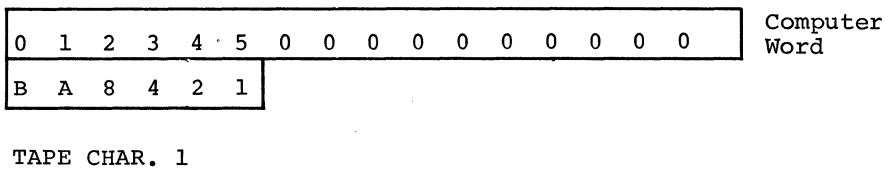
If a multiple of three plus 2 tape characters are read, the last two tape characters are positioned as the upper order 6 and next 6 bits of the last word. The 4 low order bits are set to zero as shown below. The partial word transferred status (bit 13) is set to one.

LAST WORD
7 TRACK READ
3X + 2 TAPE CHARACTERS



If a multiple of three plus 1 tape characters are read, the last tape character is positioned as the upper order 6 bits and bits 6 thru 15 of the last word are set to zero as shown below.

LAST WORD
7 TRACK READ
3X + 1 TAPE CHARACTERS



The partial word transferred status (bit 13) is set to one.

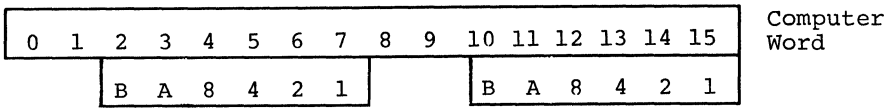
Binary mode is selected when bit 5 = 0 (read command) so that the fill operation may be performed from either a 7 or 9 track tape transport.

Binary mode is automatically selected if the selected unit is 9 track even though interchange mode may have been programmed.

Interchange Mode

Interchange mode applies only to 7 track tape transports.

7TRACK WRITE

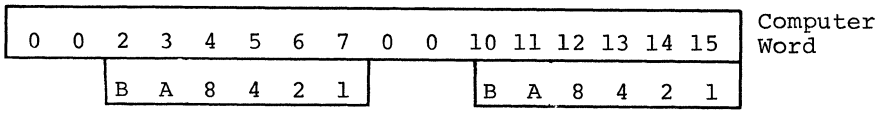


When writing on 7 track drives, transfer is implemented by writing bits 2-7 as the first tape character and bits 10-15 as the second tape character. Bits 0,1,8 and 9 of each word are ignored and thereby lost.

Since the mage tape controller operates in a word transfer mode only, this implies that only an even number of tape characters may be written in a block while in the Interchange Mode.

If even parity is selected while writing to a 7 track transport and one of the tape characters to be written is 000000 then it is translated and written as 001010. Reverse translation does not occur in read.

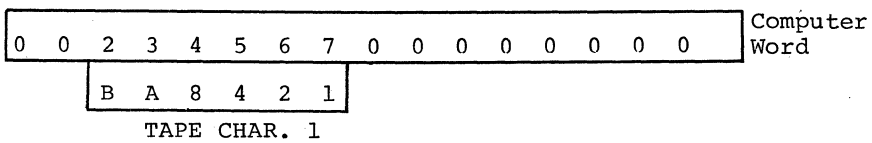
7 TRACK READ
2X TAPE CHARACTERS



When reading from 7 track drives, transfer is implemented by positioning the first tape character encountered as bits 2-7 and the second tape character as bits 10-15 of the computer word. Bits 0,1,8 and 9 are set to zero in each word.

If an odd number of tape characters are read, the last tape character is positioned as bits 2-7 and bits 0,1, and 8-15 are set to zero as shown below:

LAST WORD
7 TRACK READ
2X +1 TAPE CHARACTERS



The partial word transferred status bit 13 is set to one.

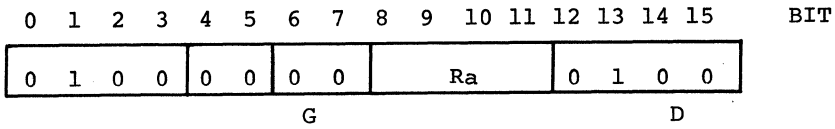
INSTRUCTIONS

The mag tape controller responds to the basic I/O Instructions - Input Data, Input Status, Output Data, Output Command.

Output Command Instruction (OCA)

This instruction causes the contents of the register specified by Ra to be transferred to the controller as a command.

COMMAND CODE



Bit one of the transfer initiate write and read commands defines the I/O transfer mode. See figure 1. Bit one = 0 specifies programmed I/O mode. Bit one = 1 specifies memory file DMP transfer mode.

Transport Select

The issuance of this command causes the controller to store the specified unit number (bits 14 and 15) in the unit register which in turn selects the transport. The transport unit bits are binarily coded as transport 0 thru 3.

This command does not cause the controller to go busy, or cause an SI under any condition. Transport select resets all resettable status.

Transport select may be issued during the dynamic window, but transport selection change does not occur until the termination of the window. Transport select does not inhibit or enable dynamic mode. An ISA may be given at any time to determine the number of the transport presently selected.

Continuous Scan

The Continuous Scan command is issued in the transport select (bit 7 = one) and it provides the method of detecting the completion of a previously initiated rewind operation. Continuous Scan causes the controller to go busy and sequentially interrogate the rewind complete status of each transport. The controller remains busy scanning transports until the occurrance of one of the following, at which time busy is reset.

1. Master Clear is issued.
2. Terminate is issued.
3. Rewind complete is true on a transport that was previously commanded to rewind. At this time the unit bits of the first transport encountered sequentially are presented in the status word. It should be noted that other transports may be in the rewind complete state after a rewind command, however, this is unknown since the scanning operation ceases after the first rewind complete is encountered. The rewind complete condition of the remaining transports may be determined by either issuing a transport select command or scan operation, followed by ISA.

If the SI is connected in the continuous scan command, in addition to going not busy, an SI is generated by the issuance of a terminate or rewind complete.

A word of caution is given regarding continuous scan. If at any time after the issuance of a rewind command, an SI disconnect is given, then the fact (storage element) that the rewinding transport was told to rewind is reset, therefore, non-busy or SI cannot occur for that transport or any others during a continuous scan.

Also, it is important to note that due to the asynchronous nature of the scan with respect to the issuance of a terminate, any SI generated after the terminate command is a result of the terminate and not a rewind complete. However, if a rewind complete did occur at approximately the same time as the terminate, it would be lost and it would be detected during the next scan operation.

Write Command

If the selected transport is operable, not rewinding and write ring engaged, the write command causes write and erase head currents to be "turned on" and forward tape motion occurs.

The unit bits (14,15), transfer mode (5), parity (8), SCS (7), and density (9) bits must be programmed in each write command if the device to be selected is a 7 track transport. Transfer mode, parity and density need not be programmed if the unit to be selected is a 9 track transport since they are overridden and set to binary, odd, and 800 CPI.

Write command with long gap selected (bit six = 1) causes an additionally longer inter-record gap of approximately five inches to be generated before writing the first tape byte/character. This allows erasing over bad areas of tape before writing. See Input Status bit 6. The first four data requests occur while the transport is in motion generating the IRG. Once the gap is generated, data requests occur at a multiple of the tape transfer rate. Data transfer continues until an underflow occurs or a terminate command is received. The DMP automatically generates a terminate command when TC=0, or after detecting a memory parity error. After the last byte/character is written, the appropriate check character(s) (CRC, LRC) are written, depending on the configuration of the selected transport (7 or 9 tracks). The CRC character (9 track only) is based on a modified cyclic code and provides a more rigorous method of error detection than using the VRC or LRC checks only.

An SI is generated (if connected) after the write command is initiated as a result of one of the following conditions:

1. The device is inoperable, or rewinding. The SI occurs immediately and the command is not attempted.
2. The SCS bit was set in the command word and a rewind complete had previously occurred. The SI occurs at the time of detection. The command is aborted and aborting unit bits and BOT are presented as status.

3. An attempt is made to write on a transport which is write protected (no write ring). The SI occurs immediately and file protect violation is set in the status word.
4. An underflow or MPE error is detected. Data transfer is terminated and the SI occurs in the normal manner after the check characters are read. The dynamic window commences with SI
5. Completion of the write operation (TC goes to zero). The SI occurs in the normal manner after the check characters are read. The dynamic window commences with SI.

The controller goes busy at the initiation of the write command and remains busy until the read logic reads the check character(s) and performs the necessary error checks. The DMP automatically generates a terminate command when TC=0 or after detecting a MPE.

When writing the first record from BOT, the first tape character of the record is written approximately 3.5 inches past the trailing edge of the BOT tab.

Read Command

If the selected transport is operable and not rewinding, the read command causes forward tape motion and write current "turn off" to occur.

The unit (14,15), transfer mode (5), parity (8), SCS (7), and density (9) bits must be programmed in each read command if the device to be selected is a 7 track transport. Transfer mode, parity and density need not be programmed if the unit to be selected is a 9 track transport since they are overridden and set to binary, odd and 800 CPI.

Tape data is assembled into words as it is encountered for subsequent transfer to the computer. The first data request occurs after the first word is assembled and thereafter data requests occur at a multiple of the tape transfer rate. Transfer continues until an overflow occurs, a terminate command is received or end of block is detected, whichever occurs first. The DMP automatically generates a terminate command when TC=0, or after detecting a memory parity error.

An SI is generated (if connected) after the read command is initiated as a result of one of the following conditions:

1. The drive is inoperable, or rewinding. The SI occurs immediately and the command is not attempted.
2. The SCS bit was set in the command word and a rewind complete had previously occurred. The SI occurs at the time of detection. The command is aborted, and aborting unit bits and BOT are presented as status.
3. An end of record is detected. The SI occurs after the read logic detects the IRG and performs error checks. A status check determines

if any of the following occurred during the block.

A) Overflow
B) Block was greater than TC
C) Parity Error
D) End of Tape
E) A partial word was transferred.
F) The block was an EOF.

The TC will not be 0 if the transfer count was greater than the block.

The controller goes not busy and stops in the IRG only after the check character(s) are read, followed by the error checks. If data transfer is terminated prior to the end of the block, data checks continue until gap detection. For 9 track transports the CRC character is utilized for error detection and not for error correction.

If the block read in response to a read command is an EOF mark, then no data requests are generated and the EOF status bit is set. The controller goes not busy and generates the SI at gap detection.

When reading the first record from BOT, the controller can detect records written with an initial minimum gap of 0.75 inches from the trailing edge of BOT.

Write EOF

If the selected transport is operable, not rewinding and write ring engaged, the write EOF command causes write and erase head currents to be "turned on" and commencement of forward tape motion to occur. If any of the above stated write operation prerequisites are not true, then the operation is inhibited and an SI is immediately generated. An SI may occur as a result of a rewind complete (see Single Cycle Scan).

Approximately 5 inches of tape are erased and then an EOF block is written. The 9 track block consists of a single data character (000010011) followed by eight character spaces with an identical LRC. There is no intervening CRC character. The 7 track block consists of a single data character (0001111) followed by four character spaces with an identical LRC. Data requests are not generated in response to a write EOF command. The unit device (14,15), SCS (7) and density (9) bits must be programmed in each WRITE EOF command if the device to be selected is a 7 track transport. Density need not be programmed if the unit to be selected is a 9 track transport since it is overridden and set to 800 CPI.

The controller goes not busy and generates the SI only after the read logic has read the LRC check character and performed the error check. At SI generation the dynamic gap window time-out commences allowing new command(s) to be accepted.

The EOF status bit is set after the read logic detects the EOF block. If a full EOF (both characters = EOF) is not detected then parity error is set.

Space Record Forward

If the selected Transport is operable and not rewinding, the space record forward command causes forward tape motion and write current "turn off" to occur. If either of the above stated prerequisites is not true, then the operation is inhibited and an SI is immediately generated. An SI may occur as a result of a rewind complete (see Since Cycle Scan).

The unit (14, 15), SCS (7) and density (9) bits must be programmed in each space record forward command if the device to be selected is a 7 track transport. Density need not be programmed if the unit to be selected is a 9 track transport since it is overridden and set to 800 CPI. The 7 track transport density must be correct to insure the reliable operation of EOF and gap detection.

Forward motion continues without making any data error checks until the next IRG is encountered. The controller goes not busy and stops in the IRG, only after the controller read logic senses the check character(s). When the controller goes not busy, the SI is generated and the dynamic gap window time-out commences allowing new command(s) to be accepted.

Data requests are not made during a space record forward. However, if the block read is an EOF tape mark, the EOF status bit is set. When spacing forward and no IRG (no more blocks on the tape) is detected, the transport moves tape forward until the physical end is reached and then goes inoperable. An SI is generated and the inoperable status bit is set.

Space Record Backward

This command operates similarly to and requires the same prerequisites and program considerations as Space Record Forward with the following exceptions.

1. Motion occurs in the reverse direction.
2. The controller goes not busy and stops in the next IRG after the read logic senses the first (detects gap) character of the respective block.
3. If no IRG (no more blocks on tape to load point) is detected, the transport moves tape backwards until the BOT tab is reached and then stops at load point. The controller goes not bysy generating an SI allowing new command(s) to be accepted. BOT and EOF status bits are set.
4. If the tape is positioned at the BOT tab when the command is given, the operation is inhibited and an SI is immediately generated. BOT and EOF status bits remain set.

Space To EOF Forward

This command operates similarly to and requires the same prerequisites and program

considerations as Space Record Forward with the following exception:

1. Blocks are spaced over without stopping until the read logic detects the EOF tape mark block, and the stops. EOF status is set.

Space To EOF Backward

This command operates similarly to and requires the same prerequisites and program consideration as Space Record Backward with the following exception:

1. Blocks are spaced over without stopping until the read logic detects the EOF tape mark block, and then stops. EOF status is set.

Single Cycle Scan

The single cycle scan mode is implemented in a write, read, write EOF, or space command by setting bit 7 equal to one. SCS is similar to continuous scan, except that only one cycle of interrogation is attempted per command. If desired, SCS must be selected with each command.

With SCS selected, the controller goes busy as though a normal operation was in process. However, before the operation is attempted, a one cycle interrogation of the rewind complete status of all four transports is initiated. If none of the four transports has a true rewind complete status (as a result of a previous rewind command), then the desired operation is initiated. If a rewind complete is established at any drive in the sequential cycle, continuance of the cycle is curtailed. In addition, the operation is aborted, and the aborting unit bits and BOT are presented in the status word. The SI occurs at the detection of the rewind complete. The controller also goes not busy at this time.

The single cycle scan occurs only if the dynamic window is made. This means that if the dynamic mode is not met, then either a continuous scan or transport select must be issued, followed by ISA to determine the rewind complete status of a transport. See Dynamic Mode for further explanation.

Rewind Command

If the selected transport is operable, the rewind command causes the unit to go into the high speed rewind mode. If the transport is inoperable or already rewinding, an SI is generated immediately. AN SI is generated after the rewind operation is initiated, which may be immediate, or occur up to 14.5 MS after the command is issued.

Selected transport rewinding sets status bit 12 true and the transport rejects commands until BOT is reached. Another unit may be selected and operated while any number of tape units are rewinding.

Rewind With Lockout

This command is similar to the rewind command except that the transport goes off-line

when the rewind is initiated. After the SI for this command is generated, device status bits 3 and 12 are set true. Operator intervention is required to return the transport to operable status.

Terminate/EOB/MPE

The issuance of a terminate while the controller is busy causes the immediate termination of data transfer. The controller remains busy, however, until the read logic detects (in normal manner) the end of the current block. Any data check errors detected (also applies to portion of block not transferred to computer in read mode) are indicated in the status word after the SI generation. A terminate issued while controller not busy will cause the immediate generation of an SI. Bit 7 of the terminate command, when set, specifies that a memory parity error has been detected during a DMP transfer. The condition may be checked with an ISA instruction because bit 4 of the status word is set by MPE in the terminate. A terminate of this type is normally hardware generated.

An EOB command, issued in conjunction or independently of Terminate, causes the immediate generation of a DI.

NO-OP

The NO-OP command is accepted by the controller regardless of controller busy status and causes the connection or disconnection of the data or service interrupt levels as specified by bits 2 and 3. See Table 8-1. If the controller is not busy, NO-OP resets all resettable controller status indicators.

Dynamic Mode

Non-stop operation in the same direction, for the same type command (excluding rewind) may be achieved by issuing a new command to the same transport within a specified time after the last service interrupt. If the dynamic window is missed, the tape will come to a complete stop before it is restarted again. No indication is given to the program that the window was missed, since the desired instruction is performed normally.

Transport select does not inhibit or enable dynamic mode. If a transport select command is issued during the window to a different transport, the selection is stored, but unit status is that of the original device. The stored unit bits are transferred to the decode register at the termination of the window, thereby selecting the desired transport.

The variable period of time for the dynamic window is specified as follows:

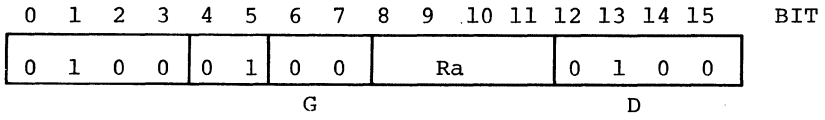
Type of Operation	No. of Tracks	Duration of Window
Write Forward	7,9	2 MS
Non-Write Forward	7,9	1 MS
Non-Write Backward	7	4.5 MS
Non-Write Backward	9	1 MS

The length of the IRG written is specified as follows:

	7 Track		9 Track	
	Min.	Nominal	Min.	Nominal
Start/Stop	.6	.78	.5	.62
Dynamic	.6	.74	.5	.59

Output Data Instruction (ODA)

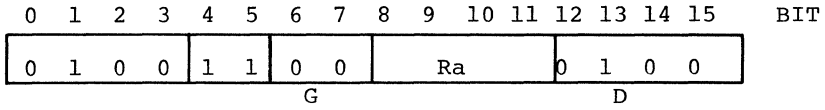
FORMAT:



This instruction causes the contents of the register specified by Ra to be transferred to the controller as data.* This instruction is used only for programmed I/O operations, since DMP handles data transfers automatically.

Input Data Instruction (IDA)

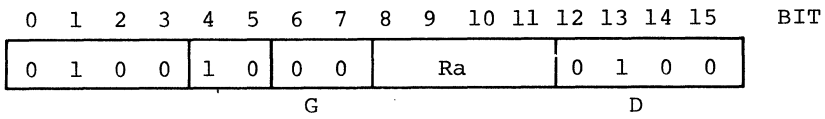
FORMAT:



This instruction causes the controller to transfer data to the register specified by Ra.* It is used only for programmed I/O operations, since DMP handles Data Transfers automatically.

Input Status (ISA)

This instruction enables the controller to transfer status to the register specified by Ra. All status bits except bits 3,7,11,12,13 are reset by a new command. The status word bit format is shown in Table 8-1.



Ra Contents

Bit 0 - Error - This bit reset (0) indicates that one or more of bits 1 through 6 are set. (See bits 1 and 5 for exceptions).

*See Data Formats for particular operations.

Bit 1 - Underflow/Overflow or Block > TC - This bit set (1) with bit 0 reset (0) indicates that data was not transferred by the CPU at a sufficient rate during write (underflow) or read (overflow). Data transfer is terminated at detection of this error. This bit set (1) with bit zero set (1) indicates that during a read data transfer was terminated prior to the end of the physical record.

Bit 2 - Device Parity Error - This bit set (1) indicates that a vertical, longitudinal or cyclical redundancy (9 track only) error was detected during a read or write (due to read after write) or write EOF operations. It is also set if a full EOF is not detected during write EOF. This error is never set during spacing operations or if EOF is detected while reading.

Bit 3 - Inoperable - This bit set (1) indicates that the selected unit has power off, an opened interlock, is off-line or is initiating the initial load sequence. Selected transport rewinding does not set inoperable unless the rewind with lockout command was issued. If the transport goes inoperable during a command, an SI is generated.

Bit 4 - Memory Parity Error - Indicates when set to 1 that the last read or write operation was terminated due to a memory parity error being detected (DMP operations only).

Bit 5 - File Protect - This bit set to one indicates that the selected transport does not contain an enable write ring. A write attempt to a file protected transport is inhibited and SI is generated. Status bit 0 is reset to 0.

Bit 6 - Tape Defect - This bit set to 1 indicates that readback data was detected while erasing during any write operation. This is not a recoverable error and normally means that the tape should be discarded.

Bit 7 - Controller Busy - Indicates when set to 1 that the controller is busy reading, writing, spacing, or initiating a rewind command. The controller does not go busy due to a transport select command. SI is generated when the controller goes not busy.

Bit 8 - Data Ready - Indicates when reset (0) that a data buffer is ready to send or receive data. This bit would only be used for programmed I/O transfers.

Bit 9 - End of Tape (EOT) - This bit is set to 1 whenever the end of tape marker is detected during a read, write or space operation. It is not set during a rewind. It is possible for EOT to occur for two consecutive records.

Bit 10 - End of File (EOF) - This bit is set to 1 whenever an EOF record is detected during a read or space, or read while writing EOF operation. This bit is also set whenever BOT (Bit 11) is true.

Bit 11 - Beginning of Tape - This bit is true (1) whenever the selected transport is positioned at the BOT Marker. Rewind and backspace issued to a transport at BOT will cause no motion, however, an SI will be generated. BOT will not be indicated after termination of a forward motion command from BOT. Bit 10 (EOF) is always set when bit 11 is set.

Bit 12 - Device Rewinding or Offline - This bit is true (1) whenever the selected transport is rewinding and online, or offline. If the transport is offline (including rewinding offline) bit 3, (inoperable) is set and bit 0 is reset.

Bit 13 - Partial Word - For 9 track or 7 track interchange mode read, this bit set to 1 indicates that a modulo number of frames was not read from the tape. This means that in the last word transferred the more significant bits compose a valid character and the less significant bits are padded to zero. It indicates that the last word transferred to the CPU contained only one or two valid characters. (See Data Formats.)

Bits 14 & 15 - Unit Number - These bits indicate the binary address of the transport presently selected by the controller.

STANDARD ASSIGNMENTS

Device Address	I/O Priority	Interrupt Locations		DMP Locations	
		SI	SI	TC	TA
Group 0, Unit 04	7	84	C4	64	74

OPERATOR CONTROL PANEL

POWER — This is a combination pushbutton switch and indicator. The indicator is on when regulated power has been supplied to the drive. For the convenience of the maintenance or customer engineer, a power switch is provided on the power supply chassis at the rear of the machine. It is accessible only when the tape unit is swung open for service.

LOAD — After threading the tape, press this combination pushbutton switch and indicator to complete the tape loading operation. Tape is automatically advanced to the load point, or beginning-of-tape marker, and then the tape system goes on line. LOAD and ON LINE will be lit when the action is completed. The LOAD light will go out when the tape is advanced from the load point or rewound. The LOAD light will be lit any time that the tape is positioned at the load point.

ON LINE — This is a combination pushbutton switch and indicator. As previously mentioned, it is lit when the system is under control of the computer or data system. If the system is off line and if control is to be turned over the computer, press the ON-LINE pushbutton.

FILE PROTECT — This is an indicator that is lit when a write enable ring is not installed on the file reel. When a file or supply reel is put on the machine with the write enable ring in place in the slot at the back of the reel, the FILE PROTECT light will be off. This indicates that data may be written

FILE PROTECT (Cont'd) on the tape. With the ring, protective circuits in the tape system prevent data from being written, which would in turn erase data previously written on the tape.

REWIND — Pressing this pushbutton switch will result in rewind of the tape, with high-speed reverse operation. The operator can stop this reverse motion by pressing the RESET pushbutton. If RESET is not pressed, the tape will go beyond the beginning-of-tape marker, stop, and then automatically return to the load point. If the REWIND pushbutton is then again pressed, the tape will be drawn out of the tape path and the unload sequence will be completed. If the tape system is under computer control, the REWIND pushbutton will not function. This safety feature prevents accidental tape damage.

FORWARD — This is a combination pushbutton switch and indicator. The pushbutton will function only when the machine is off line. If the ON-LINE indicator is on, pressing the FORWARD pushbutton will have no effect. If the ON-LINE indicator is off and the FORWARD pushbutton is pressed, the indicator will light up and the tape unit will move tape in the forward direction at the normal tape speed. To stop the machine, when it is running in this mode, press the RESET pushbutton.

REVERSE — If the ON-LINE indicator is on, pressing the REVERSE pushbutton will not affect the operation of the machine. If the tape unit is off line, pressing this combination pushbutton switch and indicator will light the light and move the tape in reverse at the normal tape speed. To stop the machine, when it is running in this mode, press the RESET pushbutton.

RESET — All tape motion, except UNLOAD, will stop when the RESET pushbutton is pressed. Pressing RESET also removes the tape unit from on-line operation with the computer or data system and turns off the ON-LINE indicator.

The table (8-1) on the following page is a summary of the Magnetic Tape Unit Control and Status indicators.

The Magnetic Tape Controller logic is located on drawing 520-100107 Sheets 1-26. The following mnemonic list (Table 8-2) gives signal names and the logic sheet number where the signal can be found. Additionally, Table 8-3 gives wiring between the controller and the device.

MAGNETIC TAPE CONTROL & STATUS

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
WRITE	1	M	D	S	Ø	Ø= BINARY 1 = INTER-CHANGE	Ø= N-GAP 1= L-GAP	1 = SINGLE CYCLE SCAN	Ø= ODD 1 = EVEN	Ø= 8ØØ CPI 1 = 556 CPI	Ø	Ø	Ø	Ø	U	U	XFER INIT
READ	1	M	D	S	1	Ø= BINARY 1 = INTER-CHANGE	Ø	1=SCS	Ø= ODD 1 = EVEN	Ø= 8ØØ CPI 1 = 556 CPI	Ø	Ø	Ø	Ø	U	U	XFER INIT
WRITE EOF	Ø	1	D	S	Ø	Ø	1	1=SCS	Ø	Ø= 8ØØ CPI 1= 556 CPI	WRITE EOF 1	Ø	Ø	Ø	U	U	CONT
SPACE	Ø	1	D	S	Ø	Ø	1	1=SCS	Ø	Ø= 8ØØ CPI 1= 556 CPI	Ø	SPACE 1	Ø= FORWARD 1= REVERSE	Ø= BLOCK 1= FILE	U	U	CONT
REWIND	Ø	1	D	S	Ø	Ø	1	1= LOCK OUT	REWIND 1				Ø		U	U	CONT
TERM EOB	Ø	1	IGNORED	IGNORED	1=EOB	1=TERM	IGNORED	1=MPE	IGNORED								CONT
NO-OP	Ø	1	D	S	Ø	Ø	Ø	IGNORED									CONT
TRANSPORT SELECT	Ø	1	D	S	Ø	Ø	1	1= CON-TINUOUS SCAN	Ø		Ø	Ø			U	U	CONT
STATUS	Ø= ERROR	1= OVER/ UNDER-FLOW OR B > C	1= DEVICE PARITY ERROR	1= INOP	1= MEMORY PARITY ERROR	1= FILE PROTECT	1= TAPE DEFECT	1= CON-TROLLER BUSY	Ø= DATA READY	1 =EOT	1 =EOF	1 =BOT	1= DEVICE OFF LINE OR REWINDING	1 = PARTIAL WORD	U	U	STATUS

COMMANDS

TABLE 8-1

INPUT CONTROL FUNCTIONS

The following on-line input signals control operation of the magnetic tape transport only after power is on, the on-line mode has been initiated, ready status has been established, and the unit has been selected. (Table 8-3 shows the pin connections required to achieve correct interface with the tape controller).

Input Functions	
Input Control Lines	Input Data Lines
Select (1 line)	Write Data (7 or 9 lines)
Forward/Stop (1 line)	Write Data Strobe (1 line)
Reverse/Stop (1 line)	Write Reset (1 line)
Rewind (1 line)	
Off-Line (1 line)	
Write Enable (1 line)	
Density Select (1 line)	

Select (1 Line). When this becomes TRUE, it enables all the write and read circuitry, the on-line transport control commands, and the status output lines if the ready status line is TRUE and if the unit is in the on-line mode. When the level goes FALSE, the above transport functions are disabled.

Forward/Stop (1 Line). When TRUE, this level causes tape to move forward. When the level goes FALSE, tape motion ceases.

Reverse/Stop (1 Line). When TRUE, this level causes tape to move in the reverse direction. When the level goes FALSE, tape motion ceases.

Rewind (1 Line). A 2 μsec minimum pulse on this line causes the tape transport to drive tape at 150 ips in the reverse direction and stop at the load point. The transport initiates a load sequence, illumination the LOAD indicator, and remains in the on-line mode. If already at load point when the rewind command is given, the command is ignored. All other motion commands are inhibited until the rewinding sequence is complete.

Off-Line (1 Line). This is a level or a 2 μsec minimum pulse that resets the on-line flip-flop to the ZERO state, placing the transport under manual control. It is gated only by Select in the transport logic, allowing an off-line command to be given while a rewind is in progress.

Write Enable (1 Line). This is a pulse whose leading edge must be prior to or coincident with the leading edge of the forward or reverse motion command and the level must remain TRUE at least 20 μsec after the initiation of the motion command in order to set the tape transport in the write mode. It is not required to pulse this line if consecutive records are to be written, but merely to hold this line TRUE until the write operation is terminated.

If the read mode of operation is required, keep this line FALSE for at least 20 μsec starting from the leading edge of the motion command. In a seven-track system this pulse occurs four character times after the last write data strobe of every block of data.

In a nine-track system this pulse occurs eight character times after the last write data strobe of every block of data.

This will reset the read/write flip-flop and place the transport in the read mode. The write mode can also be disabled by the following conditions:

a) a rewind command
b) an off-line command
c) loss of interlocks
d) manually switching to the off-line mode (by RESET action at the operator's control panel).

Density Select (1 Line). This line is used only with seven-channel tape transports. It is permanently tied TRUE on nine-channel tape transports. When this line is TRUE, it selects the high data packing density and also causes the high-density status to go TRUE.

INPUT DATA FUNCTIONS

Write Data (9 or 7 Lines). One line is required for each bit in a character. The write data lines establish the controlling condition for the NRZI write register. When TRUE, the state of the corresponding flip-flop will be changed at the time of the write data strobe. This will change the direction of the current through the write head and establish a flux reversal (ONE) on the tape. When FALSE, the state of the flip-flop will not be changed at the time of the write data strobe. This will result in no change in the direction of write head current, hence no flux reversal (ZERO) will be on tape. These data lines must be held steady through the time interval from 0.5 μsec before to 0.5 μsec after the write data strobe. A minimum of one data line must be TRUE for every strobe.

Write Data Strobe (1 Line). A 2 μsec pulse on this line causes a change in the state of any NRZI write register cell for which the corresponding write data line is TRUE. One pulse is required for each character to be recorded. The recording density is determined by the tape speed and the frequency of the pulses.

Write Reset (1 Line). A 2 μsec pulse on this line resets the NRZI write register. This pulse is used to write the longitudinal parity check (LPC) character at the end of each block of data, creating an even number of flux reversals (ONE's) in each track of the block.

OUTPUT CONTROL FUNCTIONS

The following on-line output signals provide the data and control status functions when the unit is ready and selected. (Refer to Table 8-3 for pin connections.)

Output Current Level

Output Functions

Output Control Status Lines		Output Data Lines	
Ready Status	(1 line)	Read Data	(7 or 9 lines)
On-Line Status	(1 line)	Read strobe	(1 line)
Rewind Status	(1 line)		
EOT Status	(1 line)		
BOT Status	(1 line)		
File Protect Status	(1 line)		
High-Density Status	(1 line)		

Ready Status (1 Line). This line is TRUE when the transport interlocks are made, the unit is on line and not rewinding, and the initial load sequence is complete.

On-Line Status (1 Line). When TRUE, this line indicates that the on-line flip-flop is set and the transport is under remote control.

Rewind Status (1 Line). When TRUE, this line indicates that the tape transport is rewinding. The rewinding function is completed when the tape stops at the load point.

EOT (1 Line). When TRUE, this line indicates that the tape transport is sensing the EOT reflective marker.

BOT (1 Line). When TRUE, this line indicates that the tape transport is sensing the BOT reflective marker.

File Protect (1 Line). A TRUE level on this line indicates that no write enable ring has been installed on the supply reel.

High-Density Status (1 Line). When this line is TRUE, the transport has been set for high-density operation, and the read circuitry has been conditioned accordingly. This line is used only for seven-channel systems and is tied permanently TRUE for nine-channel systems.

OUTPUT DATA FUNCTIONS

Read Data (7 or 9 Lines). One line is required for each bit in a character. Each output is at a level that changes to its appropriate state prior to the trailing edge of the read strobe pulse and remains in that state until 0.5 μsec after the trailing edge of the read strobe pulse.

Read Strobe (1 Line). The read strobe line provides a pulse of 2 μsec for each data character read from tape. The trailing edge of this pulse is used to sample the read data lines.

TABLE 8-2

45 IPS MAG TAPE CONTROLLER

MNEMONIC	DESCRIPTION	SHT#
BTINHN	BEGINNING OF TAPE DALAY COUNTER INHIBIT	9
BUFEQ	DATA BUFFER ADDRESS EQUALITY	13
BUFLDN	DATA BUFFER LOAD PULSE (LT)	13
BUSY	BUSY	23
BUSYN	BUSY (LT)	23
CLKFB	MASTER CLOCK FROM BUFFER	3
CLKFBN	MASTER CLOCK FROM BUFFER (LOW TRUE)	3
CLK1	CLOCK #1	10
CLK2	CLOCK #2	10
CLSTAN	CLEAR STATUS REGISTERS	3
CONT	CONTROL INSTRUCTION DECODED	3
CONTS	CONTINUOUS SCAN SELECTED	10
CTLCMD	CONTROL COMMAND	3
DAFB0N TO DAFB5N	DEVICE ADDRESS FROM BUFFER	1
DFB00 TO DFB15	OUTPUT DATA FROM BUFFER	4
DATARS	DATA REQUEST STROBE	13
DCRU	DELAY COUNTER RUN FLOP	12
DCRUN	DELAY COUNTER RUN FLOP (LT)	12
DCSTR	DELAY COUNTER START MODE LATCH	12
DCSTRN	DELAY COUNTER START MODE LATCH (LT)	12
DCS01	DELAY COUNTER STAGE 1	12
DCS02	DELAY COUNTER STAGE 2	12
DCS03	DELAY COUNTER STAGE 3	12
DCS04	DELAY COUNTER STAGE 4	12
DCS05	DELAY COUNTER STAGE 5	12
DCS05N	DELAY COUNTER STAGE 5 (LT)	12
DCS06	DELAY COUNTER STAGE 6	12
DCS08	DELAY COUNTER STAGE 8	12
DCS10	DELAY COUNTER STAGE 10	12
DCS11	DELAY COUNTER STAGE 11	12
DCS12	DELAY COUNTER STAGE 12	12
DCS13	DELAY COUNTER STAGE 13	12
DCS14	DELAY COUNTER STAGE 14	12
DCS15	DELAY COUNTER STAGE 15	12
DCS17	DELAY COUNTER STAGE 17	12
DCS19	DELAY COUNTER STAGE 19	12
DFB00N TO DFB15N	OUTPUT DATA FROM BUFFER (LOW TRUE)	4
DFD00N TO DFD15N	OUTPUT DATA FROM DRIVER RECEIVER MODULE	4
DFMTP	DATA FROM MAG TAPE TRANSPORT PARITY BIT	25
DFMT0-DFMT7	DATA FROM MAG TAPE TRANSPORT BITS 0-7	25
DIREQN	DATA INTERRUPT REQUEST	2
DISET	DATA INTERRUPT SET	2

TABLE 8-2

45 IPS MAG TAPE CONTROLLER (CONT'D)

MNEMONIC	DESCRIPTION	SHT#
DISETN	DATA INTERRUPT SET (LOW TRUE)	2
DRCDFN	COMMAND/DATA FUNCTION FROM DRIVER RECEIVER MODULE	3
DRCLKN	MASTER CLOCK FROM DRIVER RECEIVER MODULE	3
DRDA0N TO DRDA5N	DEVICE ADDRESS FROM DRIVER RECEIVER MODULE	1
DRDIRN	DATA INTERRUPT REQUEST TO DRIVER RECEIVER MODULE	2
DRDIUN	DATA INTERRUPT UPDATE QUEUE FROM DRIVER RECEIVER MODULE	2
DRICBN	INITIAL CONDITION BUSS FROM DRIVER RECEIVER MODULE	2
DRID0N TO DRID5N	SOURCE ID TO DRIVER RECEIVER MODULE	2
DRIOFN	INPUT/OUTPUT FUNCTION FROM DRIVER RECEIVER MODULE	3
DRIOSN	I/O SYNC FROM DRIVER RECEIVER MODULE	3
DRSIRN	SERVICE INTERRUPT REQUEST TO DRIVER RECEIVER MODULE	1
DRSIUN	SERVICE UPDATE QUEUE FROM DRIVER RECEIVER MODULE	1
DTD00N TO DTD15N	INPUT DATA TO DRIVER RECEIVER MODULE	5
DTLM00-DTLM15	DATA BUFFER OUTPUT BITS 0-15	14
DTMTP	DATA TO MAG TAPE TRANSPORT, PARITY BIT	17
DTMT0-DTMT7	DATA TO MAG TAPE TRANSPORT, BITS 0-7	17
DYNGO	DYNAMIC GAP ACHIEVED	9
DYNGON	DYNAMIC GAP ACHIEVED (LT)	9
ENID01 & ENID02	ENABLE DATA TO DRIVER RECEIVER MODULE	3
ENIS01 & ENIS02	ENABLE STATUS GATES TO DRIVER RECEIVER MODULE	3
ENRDST	ENABLE READ STROBE	11
ENRDSN	ENABLE READ STROBE (LT)	11
ENSTA	ENABLE TRANSPORT STATUS	23
ENSTP	ENABLE STOP	20
ENWRCL	ENABLE WRITE CLOCK	11
EOBLKN	END OF BLOCK COMMAND	3
EOFDT	EOF DETECT	21
EOFDTN	EOF DETECT (LT)	21
ERQSTB	ENABLE WRITE REQUEST STROBE	16
FORWD	FORWARD MODE SELECTED	8
FORWDN	FORWARD MODE SELECTED (LT)	8
GAP7N	GAP TIME 7 LATCH (LT)	20
GATEI	GATE INHIBIT	11
GATEIN	GATE INHIBIT (LT)	11
GA310	GAP COUNTER TIME 3 TO 10	20
GA411	GAP COUNTER TIME 4 TO 11	20
GA411N	GAP COUNTER TIME 4 TO 11 (LT)	20
GCSTB	GAP COUNTER STROBE	19
IBAD1	INPUT BUFFER ADDRESS 1	13
IBAD2	INPUT BUFFER ADDRESS 2	13
ICBFB	INITIAL CONDITION BUSS FROM BUFFER	2
ICBFBN	INITIAL CONDITION BUSS FROM BUFFER (LOW TRUE)	2

TABLE 8-2

45 IPS MAG TAPE CONTROLLER (CONT'D)

MNEMONIC	DESCRIPTION	SHT#
ICBN	INITIAL CONDITION BUS (LT)	10
INDCMN	INPUT DATA COMMAND	3
INEARN	INHIBIT EARLY LOAD OF UNIT BITS (LT)	11
INTER	INTERCHANGE MODE SELECTED	8
INTERN	INTERCHANGE MODE SELECTED (LT)	8
INTSTB	INTERRUPT STROBE	3
ISLM00	STATUS BIT 0 (ERROR POINTER)	25
ISLM01	STATUS BIT 1 (OVER/UNDERFLOW OR BLOCK > COUNT)	25
ISLM02	STATUS BIT 2 (PARITY ERROR)	22
ISLM03	STATUS BIT 3 (INOPERABLE)	25
ISLM05	STATUS BIT 5 (FILE PROTECT)	25
ISLM06	STATUS BIT 6 (TAPE DEFECT)	16
ISLM07	STATUS BIT 7 (BUSY)	23
ISLM08	STATUS BIT 8 (DATA READY)	13
ISLM09	STATUS BIT 9 (EOT)	25
ISLM10	STATUS BIT 10 (EOF)	25
ISLM11	STATUS BIT 11 (BOT)	25
ISLM12	STATUS BIT 12 (DEVICE OFF LINE OR REWINDING)	25
ISLM13	STATUS BIT 13 (PARTIAL WORD)	19
ISLM14	STATUS BIT 14 (UNITS MSB)	8
ISLM15	STATUS BIT L% (UNITS LSB)	8
LDCMRN	LOAD COMMAND REGISTERS	3
LDCR1	LOAD COMMAND REGISTER #1	9
LDCR2	LOAD COMMAND REGISTER #2	9
LDUB	LOAD UNIT BITS	10
LGGAP	LONG GAP SELECTED	8
LGGAPN	LONG GAP SELECTED (LT)	8
LOCKO	REWIND LOCKOUT SELECTED	8
LRCST	LRC CHECK STROBE	20
LRCSTN	LRC CHECK STROBE (LT)	20
MDESEL	MODE SELECT	3
MOCMDN	MOTION COMMAND SELECTED (LT)	9
MT0SL	MAG TAPE TRANSPORT 0 SELECTED	8
MT1SL	MAG TAPE TRANSPORT 1 SELECTED	8
MT2SL	MAG TAPE TRANSPORT 2 SELECTED	8
MT3SL	MAG TAPE TRANSPORT 3 SELECTED	8
OBAD1	OUTPUT BUFFER ADDRESS 1	13
OBAD2	OUTPUT BUFFER ADDRESS 2	13
ODD	ODD PARITY SELECTED	8
ODDN	ODD PARITY SELECTED (LT)	8
OUDCMN	OUTPUT DATA COMMAND	3
PARERN	PARITY ERROR LATCH (LT)	22

TABLE 8-2

45 IPS MAG TAPE CONTROLLER (CONT'D)

MNEMONIC	DESCRIPTION	SHT#
PARIN	PARITY GENERATION INHIBIT	15
PCRCR	CRC REGISTER PARITY BIT	18
PGCSAN	PROGRAMMED CONTINUOUS SCAN PULSE (LT)	10
RAWOR	READ AFTER WRITE OR READ MODE SELECTED	8
RDBLPN	READ BUFFER LOAD PULSE (LT)	19
RDCRU	RESET DELAY COUNTER RUN FLOP	11
RDCTE	READ CONTROL ENABLE	19
RDCTEN	READ CONTROL ENABLE (LT)	19
RDSTBN	READ STROBE FROM TRANSPORT (LT)	25
RDSTB1	READ STROBE 1	25
RDSTB2	READ STROBE 2	25
READ	READ RECORD SELECTED	8
READY	READY FROM TRANSPORT	25
RESTEN	RESET PARITY ERROR (LT)	21
REWD2	REWIND SELECTED	8
REWNDN	REWIND MODE SELECTED (LT)	8
RFPH8	READ CHARACTER TIME COUNTER PHASE 8	19
RIOTIS	REGISTER I/O TRANSFER INITIATE COMMAND	3
RPSS	READ PARITY SHIFT STROBE	19
RRDCTN	RESET READ CONTROL ENABLE (LT)	20
RSDRQN	RESET DATA REQUEST	3
RSF01	READ SERIAL SHIFT STROBE PHASE 1	19
RSF02	READ SERIAL SHIFT STROBE PHASE 2	19
RSSC1N	RESET SCAN MODE 1 (LT)	23
RSTSTN	ICB OR INSTRUCTION RESET (LOW TRUE)	2
RUNMT	RUN MAG TAPE (GO)	10
RWSTN	SELECTED TRANSPORT REWINDING (LT)	25
SCANE	SCAN MODE ENABLED	10
SCANEN	SCAN MODE ENABLED (LT)	10
SCSCA	SINGLE CYCLE SCAN ENABLE PULSE	12
SCSCAN	SINGLE CYCLE SCAN ENABLE PULSE (LT)	12
SCSHD	SINGLE CYCLE SCAN HOLD	10
SELCTN	SELECT INSTRUCTION DECODED (LOW TRUE)	3
SERRD	SERIAL READ DATA	22
SETBYN	SET BUSY PULSE (LT)	10
SETDYN	SET DYNAMIC MODE (LT)	20
WECRL	WRITE ENABLE CRC REG DATA LOAD INTO MT OUTPUT REG	16
WECRLN	WRITE ENABLE CRC REG DATA LOAD INTO MT OUTPUT REG (LT)	16
WEOFDN	WRITE EOF DATA (LT)	15
WEOFEN	SET PARITY ERROR DURING WRITE EOF (LT)	21
WPH5	WRITE PHASE 5 MS COUNTER	15
WPH15	WRITE PHASE 1 MS COUNTER & PHASE 5 LS COUNTER	15

TABLE 8-2

45 IPS MAG TAPE CONTROLLER (CONT'D)

MNEMONIC	DESCRIPTION	SHT#
SETERN	SET PARITY ERROR (LT)	20
SETEVN	SET EVEN PARITY MODE (LT)	19
SETRU	SET RUN LATCH	10
SETSIN	TERMINATE COMMAND AND NOT BUSY SET SISE	3
SETTIN	SET TRANSFER INITIATE PULSE (LT)	10
SHEOF	SEARCH EOF SELECTED	8
SICNT	SERVICE INTERRUPT CONNECTED	1
SICNTN	SERVICE INTERRUPT CONNECTED (LOW TRUE)	1
SILUPN	SI LOCK UP (LT)	23
SIREQN	SERVICE INTERRUPT REQUEST	1
SIRQST	SERVICE INTERRUPT REQUEST SET	1
SIRSTN	SERVICE INTERRUPT RESET	1
SISTPN	SET SI ON STOP (LT)	20
SPACE	SPACE RECORD SELECTED	8
SRSPIN	START OR STOP INITIATE (LT)	12
STARI	START INITIATE (DELAY COUNTER)	9
STARIN	START INITIATE (DELAY COUNTER) (LT)	9
STBGCN	STROBE BLOCK GREATER THAN COUNT (LT)	20
STBMCT	STROBE WRITE CHARACTERS/WORD MODE CONTROL	15
STBRC	STROBE READ CONTROL	20
STBRSS	STROBE READ MS COUNTER (SECOND SECTION)	19
STBSCN	STROBE SCAN INITIATE CONTROL (LT)	11
STBUB	STROBE UNIT BITS	10
STBUBN	STROBE UNIT BITS (LT)	10
STDYG	DELAY COUNTER START OR STOP/DYNAMIC MODE	11
STOPI	STOP INITIATE	20
STOPIN	STOP INITIATE (LT)	20
STRMC	STROBE READ CHARACTERS/WORD MODE CONTROL	19
STRMCN	STROBE READ CHARACTERS/WORD MODE CONTROL (LT)	19
STSCS	STROBE SCAN CONTROL	12
STSIRQ	STROBE SI REQUEST	23
STWRQN	STROBE FIRST WRITE REQUEST OF BLOCK (LT)	16
TDEFTN	TAPE DEFECT ERROR LATCH (LT)	16
TERM	TERMINATE COMMAND	3
TERMN	TERMINATE COMMAND (LOW TRUE)	3
TUHPRI	THIS UNIT HAS PRIORITY	1
TUISEL	THIS UNIT IS SELECTED	1
UFOFN	UNDERFLOW/OVERFLOW (LT)	13
UNITEQ	UNITS SELECTED EQUAL TO PREVIOUS SELECTION	8
WCRCLD	WRITE REQUEST STROBE DERIVATION	15
WDSTB	WRITE STROBE DERIVATION	15
WDSTBN	WRITE STROBE DERIVATION (LT)	15

TABLE 8-2

45 IPS MAG TAPE CONTROLLER (CONT'D)

MNEMONIC	DESCRIPTION	SHT#
WPH15N	WRITE PHASE 1 MS COUNTER & PHASE 5 LS COUNTER (LT)	15
WRAMZ	WRITE AMPLIFIER RESET	16
WRCLZN	WRITE CLOCK RESET	15
WRCTE	WRITE CONTROL ENABLE	15
WREOF	WRITE EOF SELECTED	8
WREOFN	WRITE EOF SELECTED (LT)	8
WRFPEN	WRITE FILE PROTECT ERROR (LT)	23
WRFREQ	WRITE/READ FORWARD/REVERSE EQUAL TO PREVIOUS SELECT	8
WRITE	WRITE MODE SELECTED	8
WRITEN	WRITE MODE SELECTED (LT)	8
WRRCD	WRITE RECORD SELECTED	8
WRSFT	WRITE SERIAL SHIFT CLOCK	15
WRSFTN	WRITE SERIAL SHIFT CLOCK (LT)	15
WRSLCN	WRITE SERIAL LOAD CONTROL (LT)	15
WRSTB	WRITE STROBE	
WRSTR	WRITE START	16
XFERI	TRANSFER INITIATE LATCH	23
XFERIN	TRANSFER INITIATE LATCH (LT)	23
ZRFSN	RESET FIRST SECTION READ CHARACTER TIME COUNTER (LT)	20
ZRSSN	RESET SECOND SECTION READ CHARACTER TIME COUNTER (LT)	20
ZSTATN	RESET CONTROLLER STATUS (LT)	25
ZWCLEN	RESET WRITE CONTROL ENABLE (LT)	16
0CRCR-7CRCR	CRC REGISTER BITS 0-7	18
1P6US	ONE PULSE OCCURRING 1.6US AFTER DELAY COUNTER STARTS	9
1P6USN	ONE PULSE OCCURRING 1.6US AFTER DELAY COUNTER STARTS (LT)	9
1245MS	1,2 OR 4.5 MS AFTER DELAY COUNTER STARTS IN STOP MODE	11
5VPA TO 5VPG	PULL UP VOLTAGE	1
7TRRVN	SEVEN TRACK REVERSE MODE SELECTED (LT)	8
800CP	800 CHARACTERS/INCH SELECTED	8
800CPN	800 CHARACTERS/INCH SELECTED (LT)	8
9TRAK	SELECTED TRANSPORT IS 9TRACK	25
9TRAKN	SELECTED TRANSPORT IS 9TRACK (LT)	25

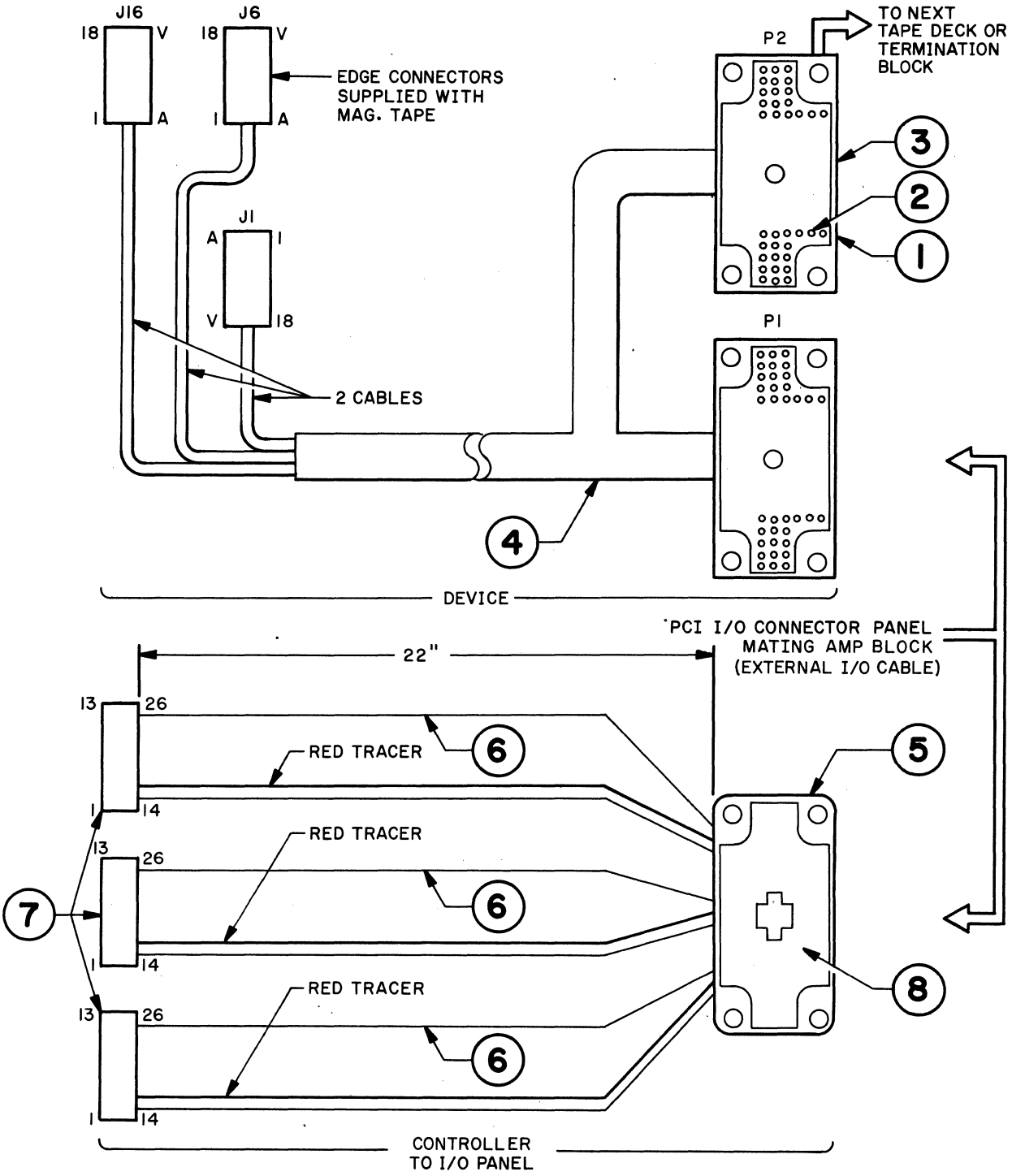


FIGURE 8-1 DEVICE CABLING

List of Materials

Item	MCS Number	Description	Quantity	Item	MCS Number	Description	Quantity
1	667-200000-001	Recpt.	2	5	667-200000-101	Plug	1
2	667-200000-201	Shield Assy.	2	6	668-600000-001	Ribbon Cable	66"
3	667-200000-601	Pins	152	7	667-200003-001	3M Connectors	3
4	668-600002-001	Cable 43 Pair Note		8	667-200000-301	Sockets	78

TABLE 8-3

MAGNETIC TAPE DEVICE CABLING

SIGNAL NAME	CONTROLLER 3M CONN.	WIRE COLOR	AMP CONNECTOR I/O PANEL & DEVICE-IN (P1)	DEVICE EDGE CONN.	DEVICE AMP-OUT (P2)
	XZ3B			J6	
	1	Brown	1D		1D
	14	White	1F		1F
DFMT7N	2	Red	2D	18	2D
Ret.	15	White	2F	V	2F
DFMT6N	3	Orange	3D	17	3D
Ret.	16	White	3F	U	3F
DPMT5N	4	Yellow	4D	15	4D
Ret.	17	White	4F	S	4F
DFMT4N	5	Green	5D	14	5D
Ret	18	White	5F	R	5F
DFMT3N	6	Blue	5C	9	5C
Ret.	19	White	5G	K	5G
DFMT2N	7	Violet	5B	8	5B
Ret.	20	White	5H	J	5H
DFMT1n	8	Gray	5A	4	5A
Ret.	21	White	5J	D	5J
DFMT0N	9	Black	6D	3	6D
Ret.	22	White	6F	C	6F
DFMTPN	10	Brown	6C	1	6C
Ret.	23	Gray	6G	A	6G
RSFMTN	11	Red	6B	2	6B
Ret.	24	Gray	6H	B	6H
HDNSTN	12	Orange	6A	E	6A
Ret.	25	Gray	6J	6	6J
ONLSTN	13	Yellow	7D	M	7D
Ret.	26	Gray	7F	11	7F
	XZ4C			J16	
MT2SLN	1	Green	7C		14D
Ret.	14	Gray	7G		14F
MT3SLN	2	Blue	7B		7C
Ret.	15	Gray	7H		7G
DNSELN	3	Violet	7A	D	7A
Ret.	16	Gray	7J	4	7J
WRTEBN	4	Brown	8D	K	8D
Ret.	17	Black	8F	9	8F
OFFLIN	5	Red	8C	L	8C
Ret.	18	Black	8G	10	8G
REWINDN	6	Orange	8B	H	8B
Ret.	19	Black	8H	7	8H
REVSPN	7	Yellow	8A	E	8A
Ret.	20	Black	8J	5	8J

TABLE 8-3

MAGNETIC TAPE DEVICE CABLING (CONT'D)

SIGNAL NAME	CONTROLLER 3M CONN. XZ4C	WIRE COLOR	AMP CONNECTOR I/O PANEL & DEVICE-IN(P1)	DEVICE EDGE CONN. J16	DEVICE AMP-OUT (P2)
FORSPN	8	Green	9C	C	9C
Ret.	21	Black	9G	3	9G
REWSTN	9	Blue	9B	N	9B
Ret.	22	Black	9H	12	9H
FIPSTN	10	Brown	9A	P	9A
Ret.	23	Violet	9J	13	9J
RDYSTN	11	Red	10C	T	10C
Ret.	24	Violet	10G	16	10G
BOTSTN	12	Orange	10B	R	10B
Ret.	25	Violet	10H	14	10H
EOTSTN	13	Yellow	10A	U	10A
Ret.	26	Violet	10J	17	10J
	XZ3D			J1	
DTMT7N	1	Green	11D	V	11D
Ret.	14	Violet	11F	18	11F
DTMT6N	2	Blue	11C	U	11C
Ret.	15	Violet	11G	17	11G
DTMT5N	3	Brown	11B	T	11B
Ret.	16	Yellow	11H	16	11H
DTMT4N	4	Red	11A	S	11A
Ret.	17	Yellow	11J	15	11J
DTMT3N	5	Green	12D	R	12D
Ret.	18	Yellow	12F	14	12F
DTMT2N	6	Blue	12C	P	12C
Ret.	19	Yellow	12G	13	12G
DTMT1N	7	Brown	12B	N	12B
Ret.	20	Orange	12H	12	12H
DTMT0N	8	Red	12A	M	12A
Ret.	21	Orange	12J	11	12J
DTMTPN	9	Green	13D	L	13D
Ret.	22	Orange	13F	10	13F
WRAMZN	10	Blue	13C	C	13C
Ret.	23	Orange	13G	3	13G
WRSTBN	11	Brown	13B	A	13B
Ret.	24	Green	13H	1	13H
MT0SLN	12	Red	13A	J - J16	
Ret.	25	Green	13J	8 - J16	
MT1SLN	13	Blue	14D		13A
Ret.	26	Green	14F		13J
+5		Brown	17D	S - J16	17D
+5		Blue	18D	S - J16	18D

The figure below illustrates the "daisy chain" interconnection of four magnetic tape units. The Unit Select 0-3 signals are named MT0-3SLN and can be found in Table 8-3 along with corresponding pin numbers. It can be seen from the figure that the first magnetic tape device connected to the controller is Unit 0, the next device in the chain is Unit 1 and so on up to Unit 3 (4 mag tape units). The terminator is illustrated on the next page and is plugged into P2 of the last mag tape unit in the chain.

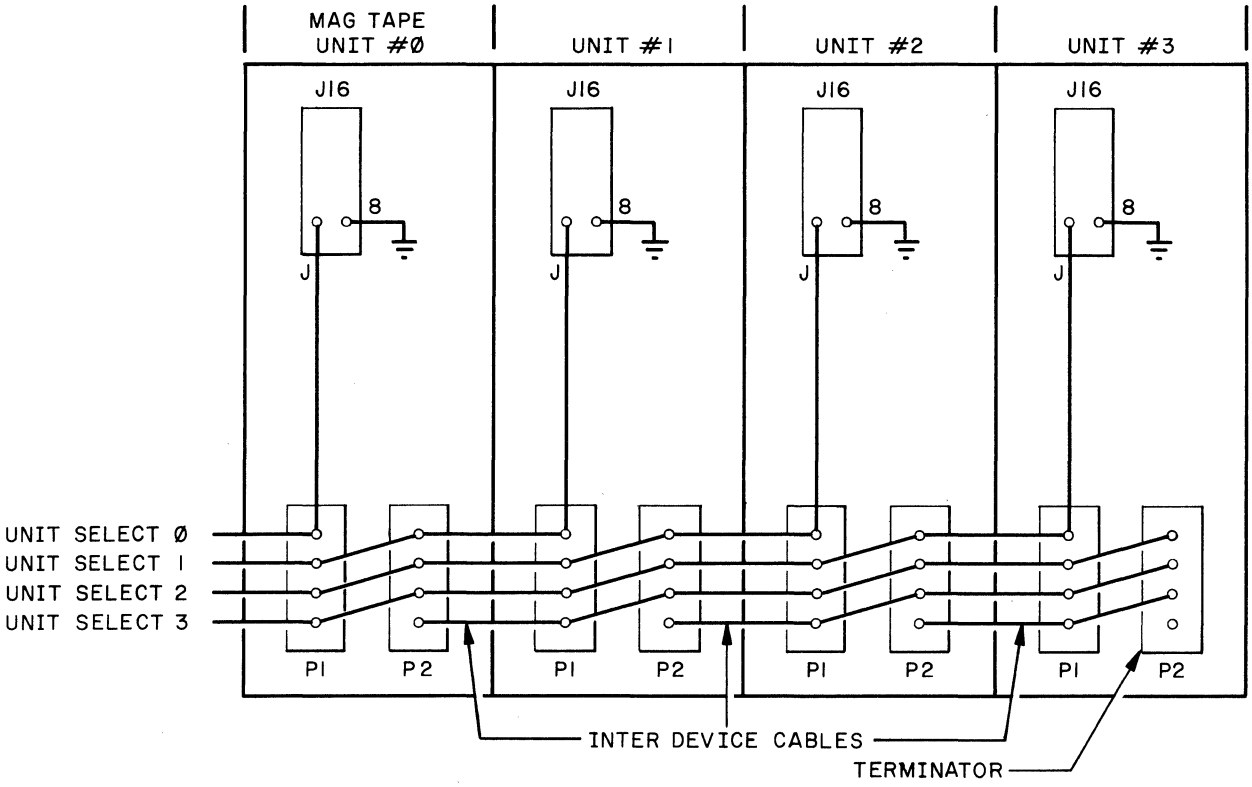


FIGURE 8-2 MAG TAPE "DAISY-CHAIN"

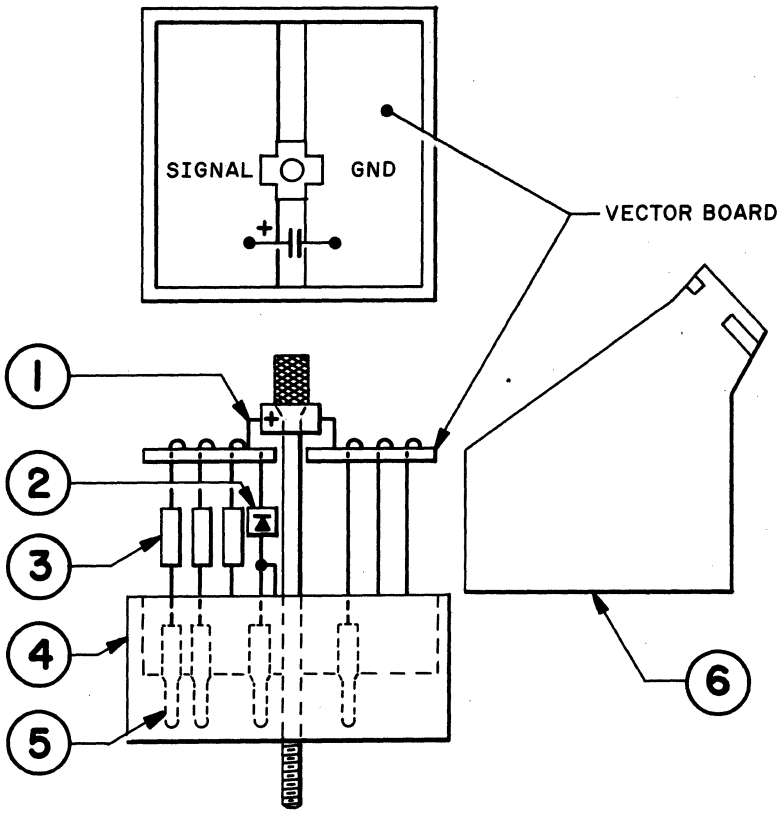


FIGURE 8-3 MAG TAPE TERMINATOR

List of Materials

Item	MCS Number	Description	Quantity
1	651-600001-014	33 µf 10V Cap.	1
2	653-200006-001	1N4002	1
3	650-100000-051	120Ω1/4W	38
4	667-200000-001	Recpt.	1
5	667-200000-202	Pins	76
6	667-200000-601	Shield Assy.	1

IX. FIXED HEAD DISC CONTROLLER

INTRODUCTION

The fixed head disc controller is capable of interfacing to up to four discs whose characteristics are listed below:

Model No.	No. TR's	No. Sectors	Average Acc. Time (MS)	Capacity Words	Transfer Rate Words/Sec.
4111	32	16	17.6	65,536	68K
4112	64	16	17.6	131,072	68K
4113	64	32	25	262,144	94K
4114	128	32	25	524,288	94K
4115	256	32	25	1,048,576	94K

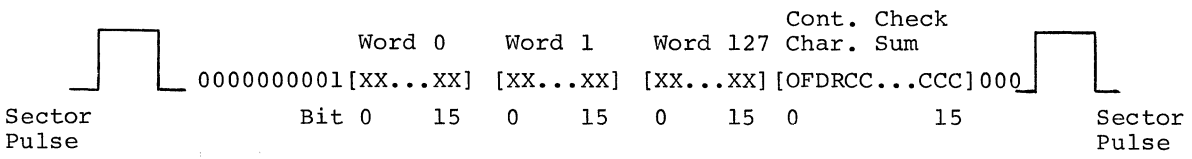
Sector size for all discs is 128 words. A logical record may be a portion of a sector or may consist of any number of sectors up to the capacity limit of the memory. Record size is controlled by word count while writing. End of Record, End of Device and End of File indicators are provided to aid in file organization.

Disc transfer rate normally requires the controller to operate in the Register File Direct Memory Processor mode. The controller is wired to operate under programmed I/O, however.

FUNCTIONAL DESCRIPTION

TRACK FORMAT

Data is recorded in with a format as shown in the following diagram:



SECTOR GAP TIMING

A time period of 200 µs exists between the end of one sector (when the SI is generated) and the beginning of the following sector. A new read or write instruction must be issued within that period to guarantee that the next sequential sector is operated on without losing a revolution. If head switching is to be done between sectors, the head select command must precede the next sector by a minimum of 30 µs or else an additional revolution will be required to complete a subsequent R/W operation.

WRITE LOCK OUT

A track protection feature is provided via a panel of eight manual switches. Write is inhibited in groups of eight physical tracks. Should an attempt to write to a protected track occur, an SI is generated and appropriate status indicated.

Model 4111 disc has four effective switches that lock out 16K words per switch. Model 4112 uses all eight switches, locking out 16K per switch; for Models 4113, 4114, 4115, each of the eight switches protect 32K words. Hence, for Models 4114 and 4115, only the lower 256K words can be protected. Write lockout applies to only the first unit of a multi unit system.

INSTRUCTIONS

OUTPUT COMMAND INSTRUCTION (OCA)

This instruction causes the contents of the register specified by Ra to be transferred to the controller as a command.

Command Code:

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	0	1	0	0	0	0	0	0	Ra				0	0	1	0
								G							D	

Ra Contents

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Write*	1	1	D	S	0	E_{O_D}	E_{O_F}	Ignored				S	S	S	S	S	Transfer Initiate
Read*	1	1	D	S	1	Ignored						S	S	S	S	S	
Head-Select	0	1	D	S	0	0	1	I_{G_N}	H	H	H	H	H	H	H	H	Control
Term/EOB	0	1	I_{G_N}		E_{O_B}	T_{R_M}	I_{G_N}	M_{P_E}	Ignored								
NOOP	0	1	D	S	0	0	0	Ignored									
Unit Select	0	0													U	U	Select

*If Bit 1 = 0 Programmed I/O is Selected Rather Than DMP.

WRITE COMMAND

The issuance of this command causes the controller to count to the specified sector, write a preamble, followed by data, followed by a control character and check sum character on a previously selected track. If the word count is greater than 128, the controller continues to write in subsequent sectors until the word count is exhausted. If the word count is not a multiple of 128 words, the controller fills the remainder of the last sector with zeroes. Should track index be encountered during this process, the head address will be automatically incremented and writing continued. When the word count does go to zero, an end of record bit is written in the control character. If the end of file bit and/or end of device bit was set to one during command initiation, these bits are also written in the control character.

The controller goes busy at the initiation of this command and remains busy until the check sum (CS) character is written at the end of the last sector, after which an SI is generated. While busy, the controller will accept only terminate, EOB and NO-OP commands. Command acceptance resets previous controller status indicators.

READ COMMAND

This command, when issued, causes the controller to count to the specified sector, synchronize on the preamble, and transfer the following data to memory from a previously selected track. Data transfer continues until the word count goes to zero. If TC $\leq$ 128, the control character and CS are read and the command terminated. If TC > 128, subsequent sectors are read until the word count is exhausted. The head register will be automatically incremented when necessary to complete the read. CS is checked for each sector read and data transfer terminated on the sector where an error is detected. Data transfer is also terminated on a sector when EOR is detected. A status test, after the read operation is complete, will indicate whether EOR, EOD and/or EOF bits were set in the control word.

The controller goes busy at the initiation of this command and remains busy until the CS is checked at the end of the last sector, at which time an SI is generated. Command acceptance resets previous controlled status indicators.

HEAD SELECT

The issuance of this command causes the controller to store the specified address (Bits 8 through 15) in the head register which, in turn, selects a head within the device. This command does not cause the controller to go busy or generate an SI, (unless the unit is inoperable). It will reset controller status indicators. Head select recovery time is 30 μs. Master clear sets head address to zero.

TERMINATE/EOB

The issuance of a terminate while the controller is busy will cause the immediate termination of data transfer. The controller will remain busy, however, until the end of the current sector. A terminate issued while not busy will cause the immediate generation of an SI. If bit 7 of the command is set, bit 4 of the status indicator will also be set. A terminate of this type is normally hardware generated to indicate a memory parity error. An EOB command, issued in conjunction or independently of terminate, will cause the immediate generation of a DI.

NO-OP

The NO-OP command will be accepted by a controller regardless of busy status and will cause the connection or disconnection of the data and service interrupt levels as specified by bits 2 and 3. If the control is not busy, it will also reset controller status indicators.

UNIT SELECT

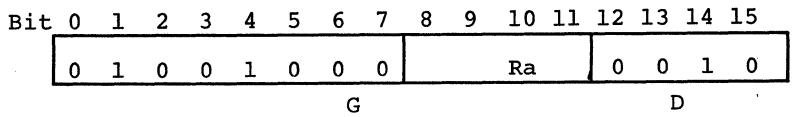
The issuance of this command causes the controller to store the specified unit number (bits 14 and 15) in the unit register; which , in turn, selects the unit. Whenever

a unit select command is issued to a different device, sector coincidence is inhibited until the sector counter is synchronized with the new device. This command does not cause the controller to go busy nor to generate an SI. It does not reset controller status indicators. Master clear selects unit zero.

INPUT STATUS INSTRUCTION (ISA)

This instruction enables the controller to transfer its status to the register specified by Ra.

Command:



Ra Contents:

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	E R R O R	0/F U/F	C H E C K S U M	I N P	M P E	W R T E L / O		B U S Y	D A T A R E A D Y	E D	E O F	E O R				

Bit

0 - Error - This bit reset (0) indicates that one or more of bits 1 through 4 are set.

1 - Underflow/Overflow - This bit set (1) indicates that data was not transferred by the CPU at a sufficient rate during write (underflow) or read (overflow). Data transfer is terminated at detection of this error. For writes, the remainder of the sector is filled with zeroes.

2 - CS Error - This bit set (1) indicates that a check sum check error was detected upon reading a sector. During multisector (sequential) reads, data transfer terminates at the detection of the error.

3 - Inoperable - This bit being set (1) indicates that device power is off.

4 - Memory Parity Error - Indicates when set (1) that the last read or write operation was terminated due to a memory parity error being detected.

5 - Write Lockout Violation - This bit set to 1 indicates that the selected track is protected. If bit zero is also Reset (zero), an attempt was made to write to a protected group of 8 heads.

6 - Not used.

7 - Busy - Indicates when set to 1 that the controller is busy performing a data transfer command. The controller does not go busy due to the head selection command.

Bit

8 - Data Ready - Indicates when reset (0) that a data buffer is ready to send or receive data. This bit would be used for programmed I/O.

9 - End of Device - Indicates when set to 1 that the last record read (single or multiple sector) was written as an End of Device Record. This bit is also true after writing an EOD record.

10 - End of File - Indicates when set (1) that the last record read (single or multiple sector) was written as an End of File Record. This bit is also true after writing an EOF record.

11 - End of Record - Indicates when set to 1 that the last sector read was either a single sector logical record or the last sector of a multi-sector logical record. This bit is always true after writing a record.

12-15 - Not used.

STANDARD ASSIGNMENTS

DEVICE ADDRESS	I/O PRIORITY	INTERRUPT LOCATIONS		DMP LOCATIONS	
		DI	SI	TC	TA
02	1	82	C2	62	72

PHYSICAL CHARACTERISTICS

Models 4111, 4112:

Size: Standard Retma/EIA
Rack Mounted on Slides
19" wide, 12.25" high, 24" deep

Weight: 65 pounds

Power: 115 volts AC ± 10% 60 HZ ± 1% 1 phase
Starting: 3.5 amps
Running: 1.5 amps

Models 4113, 4114, 4115

Size: Free Standing Cabinet on casters 22" wide, 48" deep, 51" high.

Weight: 270 Pounds

Power: 115 VAC ± 10%, 60 Hz ± 1%, Single Phase
Starting: 32 AMPS
Running: 7 AMPS

Environmental Conditions, All Models

Operating: Temp. Range 50°F to + 150°F
Humidity 10% to 90% RH, Non-condensating

Non-Operating: Temp. Range 40°F to + 160°F
Humidity 10% to 95% RH, Non-condensating

TABLE 9-1

MNEMONIC LIST FOR FHD

MNEMONIC	DESCRIPTION	SHT#
ADDZEN	DEVICE ADDRESS EQUALS ZERO	7
BCTEQ	BUFFER COUNT EQUAL	10
BTCLK	BIT CLOCK (WRITE CLOCK)	19
BTCLKN	BIT CLOCK (WRITE CLOCK) LOW TRUE	19
BTCLKI	BIT CLOCK (WRITE CLOCK) INTERFACE FROM DEVICE	19
BTCT1 TO BTCT8	BIT COUNTS	13
BTCT1N TO BTCT8N	BIT COUNTS (LOW TRUE)	13
CKSERN	CHECK SUM ERROR	16
CKSM00 TO CKSM11	CHECK SUM BITS	16
CLICR	CLEAR/ICB	11
CLKFB	MASTER CLOCK FROM BUFFER	3
CLKFBN	MASTER CLOCK FROM BUFFER (LOW TRUE)	3
CLSTAN	CLEAR STATUS REGISTERS	3
CONT	CONTROL INSTRUCTION DECODED	3
CTLCMD	CONTROL COMMAND	3
CT1248	OUTPUT OF BIT COUNTER. TRUE WHEN ALL COUNTS ARE HIGH	8
DAFB0N TO DAFB5N	DEVICE ADDRESS FROM BUFFER	1
DATARS	DATA REQUEST	10
DFB00 TO DFB15	OUTPUT DATA FROM BUFFER	4
DFB00N TO DFB15N	OUTPUT DATA FROM BUFFER (LOW TRUE)	4
DFD00N TO DFD15N	OUTPUT DATA FROM DRIVER RECEIVER MODULE	4
DIREQN	DATA INTERRUPT REQUEST	2
DISET	DATA INTERRUPT SET	2
DISETN	DATA INTERRUPT SET (LOW TRUE)	2
DMPRQN	DMP REQUEST (LOW TRUE)	7
DMPSRS	DMP STORE TRANSFER ADDRESS REQUEST SET	11
DRCDFN	COMMAND/DATA FUNCTION FROM DRIVER RECEIVER MODULE	3
DRCLKN	MASTER CLOCK FROM DRIVER RECEIVER MODULE	3
DRDA0N TO DRDA5N	DEVICE ADDRESS FROM DRIVER RECEIVER MODULE	1
DRDIRN	DATA INTERRUPT REQUEST TO DRIVER RECEIVER MODULE	2
DRDIUN	DATA INTERRUPT UPDATA QUEUE FROM DRIVER RECEIVER MODULE	2
DRDMRN	DMP REQUEST TO DRIVER RECEIVER MODULE	7
DRDMUN	DMP UPDATE QUEUE FROM DRIVER RECEIVER MODULE	7
DRICBN	INITIAL CONDITION BUSS FROM DRIVER RECEIVER MODULE	2
DRID0N TO DRID5N	SOURCE ID TO DRIVER RECEIVER MODULE	2
DRIOFN	INPUT/OUTPUT FUNCTION FROM DRIVER RECEIVER MODULE	3
DRIOSN	I/O SYNC FROM DRIVER RECEIVER MODULE	3
DRSIRN	SERVICE INTERRUPT REQUEST TO DRIVER RECEIVER MODULE	1
DRSIUN	SERVICE UPDATE QUEUE FROM DRIVER RECEIVER MODULE	1
DTD00N TO DTD15N	INPUT DATA TO DRIVER RECEIVER MODULE	5
DTLM00 TO DTLM15	DATA TO LOGIC MODULE	14
ENID01 & ENID02	ENABLE DATA TO DRIVER RECEIVER MODULE	3

TABLE 9-1

MNEMONIC LIST FOR FHD (Cont'd)

MNEMONIC	DESCRIPTION	SHT#
ENIS01 & ENIS02	ENABLE STATUS GATES TO DRIVER RECEIVER MODULE	3
EOBLKN	END OF BLOCK COMMAND	3
HA1I TO HA128I	HEAD ADDRESS INTERFACE TO DEVICE	19
HA1N TO HA128N	HEAD ADDRESS (LOW TRUE)	17
IBAD1	INPUT BUFFER ADDRESS 1	10
IBAD2	INPUT BUFFER ADDRESS 2	10
ICBFB	INITIAL CONDITION BUSS FROM BUFFER	2
ICBFBN	INITIAL CONDITION BUSS FROM BUFFER (LOW TRUE)	2
INCWDN	INCREMENT WORD COUNTER	9
INDCMN	INPUT DATA COMMAND	3
INOPN	INOPERABLE (LOW TRUE)	12
INTSTB	INTERRUPT STROBE	3
ISLM00	STATUS BIT 00 (ERROR DETECTED IN BITS 1 THROUGH 4)	16
ISLM01	STATUS BIT 01 (UNDERFLOW/OVERFLOW)	10
ISLM02	STATUS BIT 02 (CRC ERROR)	16
ISLM03	STATUS BIT 03 (INOPERABLE)	12
ISLM04	STATUS BIT 04 (MEMORY PARITY ERROR)	7
ISLM05	STATUS BIT 05 (WRITE LOCKOUT VIOLATION)	18
ISLM07	STATUS BIT 07 (BUSY)	9
ISLM08	STATUS BIT 08 (DATA READY-LOW TRUE)	10
ISLM09	STATUS BIT 09 (END OF DEVICE)	11
ISLM10	STATUS BIT 10 (END OF FILE)	11
ISLM11	STATUS BIT 11 (END OF RECORD)	11
LDBUFN	LOAD DATA BUFFER	10
LDCMRN	LOAD COMMAND REGISTERS	3
LDHDRN	LOAD HEAD REGISTER (LOW TRUE)	17
LOSIN	WRITE LOCKOUT SI (LOW TRUE)	18
MDESEL	MODE SELECT	3
MPEN	MEMORY PARITY ERROR (LOW TRUE)	7
OBAD1	OUTPUT BUFFER ADDRESS 1	10
OBAD2	OUTPUT BUFFER ADDRESS 2	10
OUDCMN	OUTPUT DATA COMMAND	3
PSRSCN	PARALLEA SERIAL REGISTER SHIFT CONTROL (LOW TRUE)	11
RDBCA	READ BIT COUNT ENABLE	9
RDBLPN	READ BUFFER LOAD PULSE (LOW TRUE)	9
RDBSY	READ BUSY	9
RDBSYN	READ BUSY (LOW TRUE)	9
RDBTCL	READ/BIT CLOCK	15
RDCKA	READ CHECK SUM ENABLE	9
RDCLK	READ CLOCK	19
RDCLKN	READ CLOCK (LOW TRUE)	19
RDCLKI	READ CLOCK INTERFACE FROM DEVICE	19

TABLE 9-1

MNEMONIC LIST FOR FHD (Cont'd)

MNEMONIC	DESCRIPTION	SHT#
RDDATA	READ DATA	19
RDDATI	READ DATA INTERFACE FROM DEVICE	19
RDENA	READ ENABLE	9
RDENAN	READ ENABLE (LOW TRUE)	9
RDENBI	READ ENABLE INTERFACE TO DEVICE	19
RDEND	END SECTOR READ	9
RDENDN	END SECTOR READ (LOW TRUE)	9
RDSFA	READ SHIFT ENABLE	9
RDSFAN	READ SHIFT ENABLE (LOW TRUE)	9
REICN	READ END/ICB (LOW TRUE)	9
RGIOMD	REGISTER I/O MODE	7
RIOTIS	REGISTER I/O TRANSFER INITIATE COMMAND	3
RSDRQN	RESET DATA REQUEST	3
RSTSTN	ICB OR INSTRUCTION RESET (LOW TRUE)	2
SECND	SECTOR COINCIDENCE	12
SECT	SECTOR PULSE	19
SECTN	SECTOR PULSE (LOW TRUE)	19
SECTI	SECTOR PULSE INTERFACE FROM DEVICE	19
SELCTN	SELECT INSTRUCTION DECODED (LOW TRUE)	3
SETSIN	TERMINATE COMMAND AND NOT BUSY SET SI	3
SICNT	SERVICE INTERRUPT CONNECTED	1
SICNTN	SERVICE INTERRUPT CONNECTED (LOW TRUE)	1
SIILON	TERMINATE NOT BUSY SI/INITIAL LOCKOUT SI	18
SIREQN	SERVICE INTERRUPT REQUEST	1
SIRQST	SERVICE INTERRUPT REQUEST SET	1
SIRSTN	SERVICE INTERRUPT RESET	1
SPBT00 TO SPBT15	SERIAL/PARALLEL DATA BITS	15
STSIRQ	SET SI REQUEST	11
TACH	BEGINNING OF DISC	19
TACHN	BEGINNING OF DISC (LOW TRUE)	19
TACHF	BEGINNING OF DISC FLIP FLOP	17
TACHT	BEGINNING OF DISC INTERFACE FROM DEVICE	19
TERM	TERMINATE COMMAND	3
TERMN	TERMINATE COMMAND (LOW TRUE)	3
TERMF	TERMINATE F/F	11
TERMFN	TERMINATE F/F (LOW TRUE)	11
TICMD	TRANSFER INITIATE COMMAND	8
TICMDN	TRANSFER INITIATE COMMAND (LOW TRUE)	11
TUHPRI	THIS UNIT HAS PRIORITY	1
TUISFL	THIS UNIT IS SELECTED	1
UFOFN	UNDERFLOW/OVERFLOW (LOW TRUE)	10
UNBT1 TO UNBT2	UNIT SELECT BITS	17

TABLE 9-1

MNEMONIC LIST FOR FHD (Cont'd)

MNEMONIC	DESCRIPTION	SHT#
UNIT0I TO UNIT3I	UNIT NUMBER INTERFACE TO DEVICE	19
UNIT0N TO UNIT3N	DEVICE UNIT NUMBER	17
UNSELN	UNIT SELECT (LOW TRUE)	17
WDCTE	WORD COUNT END	13
WDCTEN	WORD COUNT END (LOW TRUE)	13
WDCT01 TO WDCT64	WORD COUNTS	13
WRBSY	WRITE BUSY	8
WRBSYN	WRITE BUSY (LOW TRUE)	8
SRCCDE	WRITE CONTROL CHARACTER DATA ENABLE	8
WRCSD	WRITE AND CHECK SUM DATA	19
WRCSF	WRITE CHECK SUM ENABLE	8
WRCSEN	WRITE CHECK SUM ENABLE	8
WRDATI	WRITE DATA INTERFACE TO DEVICE	19
WRDCS	WRITE DATA AND CHECK SUM ENABLE	11
WRENA	WRITE ENABLE	8
WRENAN	WRITE ENABLE (LOW TRUE)	8
WRENDI	WRITE ENABLE INTERFACE TO DEVICE	19
WREND	END SECTOR WRITE	8
WRENDN	END SECTOR WRITE (LOW TRUE)	8
WRGAPN	WRITE GAP (LOW TRUE)	8
WRINTN	WRITE INITIALIZE (LOW TRUE)	10
WRLCSN	WRITE LOAD CHECK SUM (LOW TRUE)	8
WRLDCN	LOAD WRITE DATA CLOCK	8
WRLERN	WRITE LOCKOUT ERROR (LOW TRUE)	18
WRLS07 TO WRLS63	WRITE LOCKOUT SWITCHES (GROUP OF 8)	18
WROK	WRITE OK	8
WRONFN	WRITE ONE 1 (LOW TRUE)	8
WRSDF	WRITE SERIAL DATA ENABLE	8
WRSDEN	WRITE SERIAL DATA ENABLE (LOW TRUE)	8
WRSIHN	WRITE SHIFT INHIBIT (LOW TRUE)	8
WRSLC	WRITE SERIAL LOAD CONTROL	8
WRSLCN	WRITE SERIAL LOAD CONTROL (LOW TRUE)	8
WRTRM	WRITE TERMINATE	11
WRTRMN	WRITE TERMINATE (LOW TRUE)	11
5VPA TO 5VPG	PULL UP VOLTAGE	1
5VPH TO 5VPP	PULL UP VOLTAGE	7
5VPQ TO 5VPW	PULL UP VOLTAGE	10
5VP1 TO 5VP7	PULL UP VOLTAGE	11

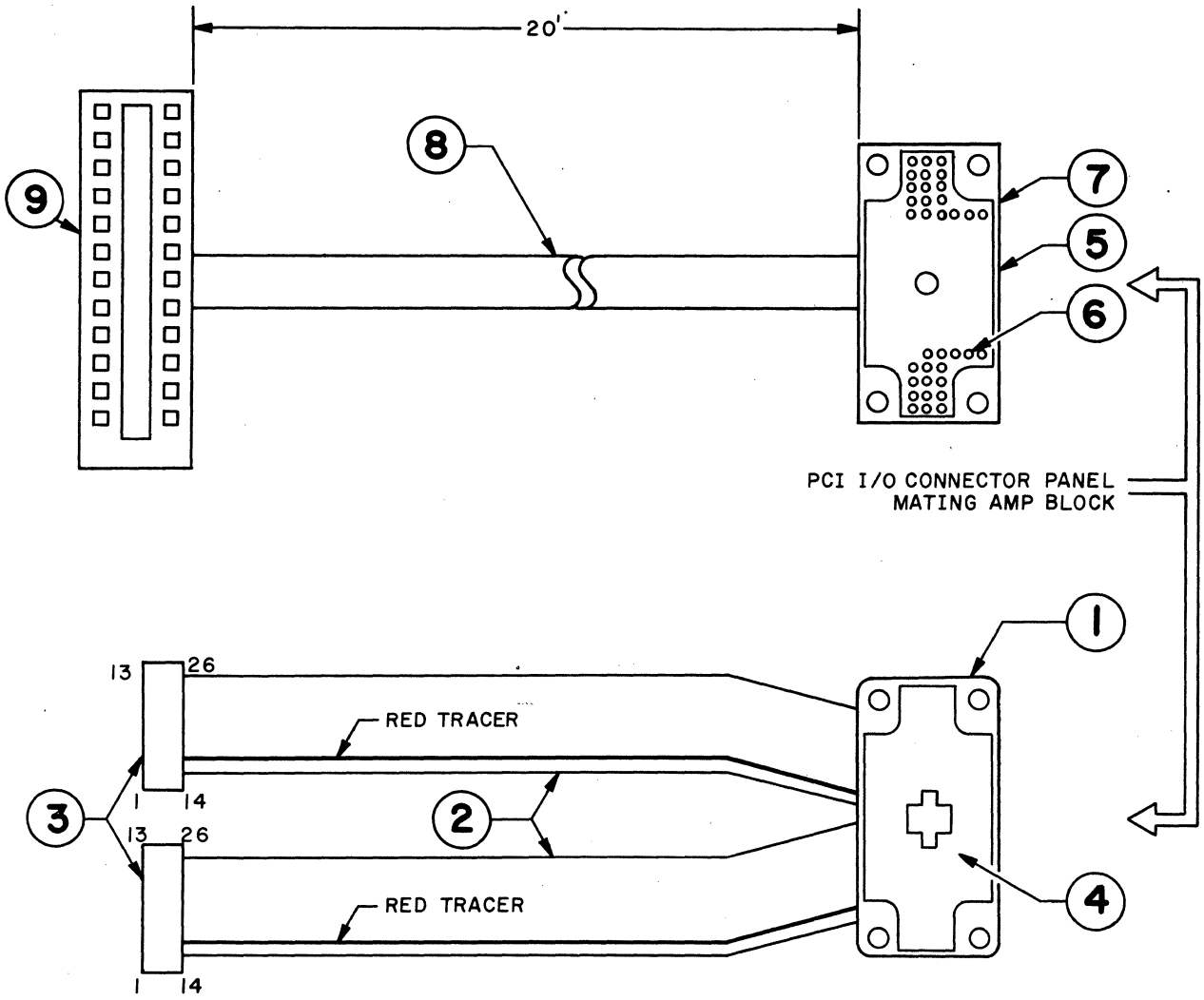


FIGURE 9-1 DEVICE CABLING

List of Materials (Fixed Head Disc)

Item	MCS Number	Description	Quantity
1	667-200000-101	Plug	1
2	668-600000-001	Ribbon Cable	44"
3	667-200003-001	3M Connector	2
4	667-200000-301	Socket	52
5	667-200000-001	Receptacle	1
6	667-200000-201	Pins	40
7	667-200000-601	Shield Assy.	1
8	668-600001-001	Cable	20 ft.
9		Amphenol Connector	1

TABLE 9-2

FIXED HEAD DISC

SIGNAL NAME	DEVICE CONN.	WIRE COLOR	AMP BLOCK	CONTROLLER 3M CONN. XY2C
HA128I	16	Brown	13A	1
Ret.	18	White	14A	14
HA64I	17	Red	13B	2
Ret.	18	White	14B	15
HA32I	12	Orange	11A	3
Ret.	18	White	12A	16
HA16I	20	Yellow	11B	4
Ret.	18	White	12B	17
HA08I	21	Green	11C	5
Ret.	18	White	12C	18
HA04I	22	Blue	9A	6
Ret.	18	White	10A	19
HA02I	23	Black	9B	7
Ret.	18	White	10B	20
HA01I	24	Brown	9C	8
Ret.	18	Blue	10C	21
UNT0	19	Red	7A	9
Ret.	18	Blue	8A	22
UNT1	9	Orange	7B	10
Ret.	18	Blue	8B	23
UNT2	10	Yellow	7C	11
Ret.	18	Blue	8C	24
UNT3	11	Green	5A	12
Ret.	18	Blue	6A	25
SPARE			5B	13
Ret.			6B	26
				XY2D
RDENBI	4	Brown	13H	1
Ret.	18	Green	14H	14
WRENBI	8	Red	13J	2
Ret.	18	Green	14J	15
WRDATI	7	Orange	11G	3
Ret.	18	Green	12G	16
RDDATI	6	Yellow	11H	4
Ret.	18	Green	12H	17
SECTI	2	Black	11J	5
Ret.	14	Green	12J	18
TACHI	1	Brown	9G	6
Ret.	13	Red	10G	19
BTCLKI	3	Orange	9H	7
Ret.	15	Red	10H	20

TABLE 9-2

FIXED HEAD DISC

SIGNAL NAME	DEVICE CONN.	WIRE COLOR	AMP BLOCK	CONTROLLER 3M CONN. XY2D
RDCLKI	5	Yellow	9J	8
Ret.	18	Red	10J	21
SPARE			7G	9
Ret.			8G	22
SPARE			7H	10
Ret.			8H	23
SPARE			7J	11
Ret.			8J	24
SPARE			5H	12
Ret.			6H	25
SPARE			5J	13
Ret.			6J	26

X. HIGH SPEED PAPER TAPE PUNCH CONTROLLER

GENERAL

The High Speed Paper Tape Punch (BRPE) Controller is mounted on a standard logic page to be located in the Peripheral Controller Interface unit which may mount in the same rack as the mainframe or in a separate rack, depending on the system configuration.

The punch power supply and solenoid driver card are located in a standard MCS rack mountable power supply enclosure.

The punch configuration will not be capable of handling fanfold paper.

Power - BRPE and power supply electronics require 115 VAC.

The BRPE controller receives 1.2 amps at 5 volts from a 5 volt power supply located in the cabinet.

Punch Speed - 110 CPS

I/O INSTRUCTION FORMAT

Four types of I/O instructions exist as defined by bits 4 and 5 of the I/O instruction. These instruction types are Command, Data In/Out and Status. The high speed punch does not respond to the Input Data instruction.

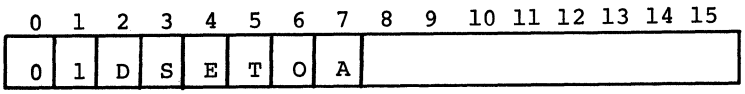
The output register instruction (a programmed I/O instruction) presents the contents of the specified register on the 16 I/O data lines. In addition, bits 4 through 7 and bits 12 through 15 of the instruction register are presented on the function and address lines. The function lines define to the I/O device the type of I/O instruction in progress. The address lines define the device which is to receive the instruction. The input register instruction places the contents of the 16 data lines into the specified register. In addition, bit 4 through 7, and 12 through 15 of the instruction register are presented on the function and address lines. Terminate and status commands are the only instructions that will be accepted by the controller when it is busy.

Program Commands

The high speed punch Controller responds to the control and transfer initiate command formats. The control format is used in the minimal standard configuration, as shown below. It should be noted that a no-operation may be obtained with bits 4, 5 and 6

of the control format equal to zero. Bits 2 and 3 may be "zero or "one" depending on programming constraints. All commands except terminate will reset any stored status.

Control



BITS	FUNCTION
0	Must be "zero." This bit in conjunction with bit 1 specifies the control format.
1	Must be "one". This bit in conjunction with bit 0 specifies the control format.
2	Specifies the state of the data interrupt. Ignored during terminate. Zero - disconnects and resets the request if it was active. One - connects the interrupt, thus allowing it to become active each time the punch controller is capable of receiving data.
3	Specifies the status of the service interrupt. Ignored during terminate. Zero - disconnects and resets the request if it was active. The service interrupt becomes active after a terminate command is issued if the interrupt had previously been connected. This may occur immediately if the high speed punch is ready to respond a new command i.e. not busy.
4	Specifies EOB when equal to "one". No effect when equal to "zero". The EOB sets the DI if it was previously connected. EOB may be issued in conjunction with terminate or independently.
5	Specifies terminate command when equal to "one". No effect when equal to "zero". A terminate command will be accepted when the controller is busy. The terminate command stops data transfer to the controller and resets any nonactive data interrupt. The terminate command will also condition the controller to generate the service interrupt when it is ready to respond to another transfer initiate command. This occurs at the next sprocket hole time if the controller is ready and the SI had been previously connected.

If another transfer initiate does not occur within 10 sec the punch motor will be turned off. The controller ignores all bits except 0, 1, 4, 5 and 7 during a terminate. Once a terminate has been programmed, a transfer initiate must be programmed to start data transfer again. A terminate does not reset status.

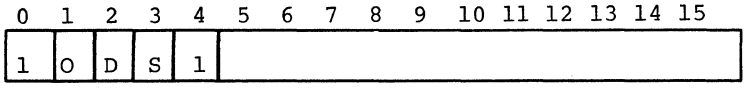
6 — Specifies the no-op command when equal to "zero" in concurrence with 4 and 5 equal to "zero".

7 — Specifies abort terminate command when equal to "one". No effect when equal to "zero". The abort terminate must be issued in the terminate command to be active. Abort terminate causes the controller to unconditionally go not busy at the time of receipt.

8 - 15 — Ignored by controller.

Transfer Initiate

A transfer initiate command places the controller in the active state and starts the process of transferring data.



0 — Must be "one". This bit specifies the transfer initiate format.

1 — Ignored by the controller.

2, 3 — Same as bits 2 and 3 of the control format.

4 — When equal to one no effect.

Zero - Output. This command turns power on to the BRPE motor and conditions the controller to accept output data. The first data interrupt occurs 1 sec after the output command is received if the motor was not previously turned on. However, the data interrupt will occur immediately after the output command if the motor was previously turned on.

The motor will be turned off 10 sec after a terminate command if an output command is not received during this interval. If a terminate command is not given, the punch controller will maintain the data interrupt active if connected and leave the motor on.

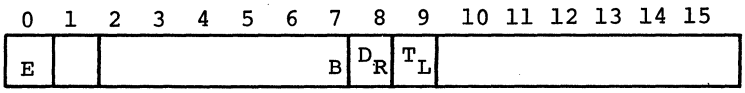
5 - 15 — Ignored by controller.

INPUT STATUS FORMAT

If bits 4 and 5 of the I/O command equal 10, an input status instruction is specified. This instruction causes the contents of the 16 I/O data lines to be placed into the specified register.

The status format is so defined that a status word of all zeros is invalid, indicating a malfunctioning or non-existent controller.

STATUS WORD



BIT	INDICATION
0	Error Pointer Bit For the high speed punch controller this bit is always equal to one.
1 - 6	Presented as zeros by the controller.
7	Busy Status of Controller. Zero - controller is not busy. This means that it is not receiving data, and it has received a terminate command, or master clear. One - controller is busy. The controller goes busy immediately upon receiving a transfer initiate command and remains so until a terminate command is issued and the controller has finished transfer of the operating character. When the controller goes not busy, it is prepared to accept another transfer initiate command.
8	Data Ready This status bit is used primarily in the non-interrupt transfer mode. It is activated (zero) whenever the controller wishes to receive a data word. It is essentially generated in the same manner as the data interrupt. Terminate will reset it, in addition to a data out instruction or not busy. It is only enabled when the controller is busy. One - Device controller is not ready to receive a data word. Zero - Device controller is ready to receive a data word.

9	Tape Low Zero - Tape supply reel does not need to be replaced. One - Tape supply reel is low and must be replaced. Commands will not reset this bit. It will reset when Tape is no longer low.
10 - 15	Presented as zeros by controller.

DATA OUT/IN

When bits 4 and 5 of the I/O instruction specify a data transfer out, the content of the specified register are placed on the 16 data lines along with an I/O sync strobe and device address.

When outputting to the punch the maimum rate of transfer is 110 characters per second. The controller sends a data interrupt at 9.09 ms intervals. The DI occurs each time the controller is ready to receive a character. Data is presented to the controller from the 8 least significant bits.

A terminate will be effective once the transmitting character has been completed.

STANDARD ASSIGNMENTS

DEVICE ADDRESS	I/O PRIORITY	INTERRUPT LOCATIONS	
		DI	SI
09	13	89	C9

PROGRAMMING SEQUENCE

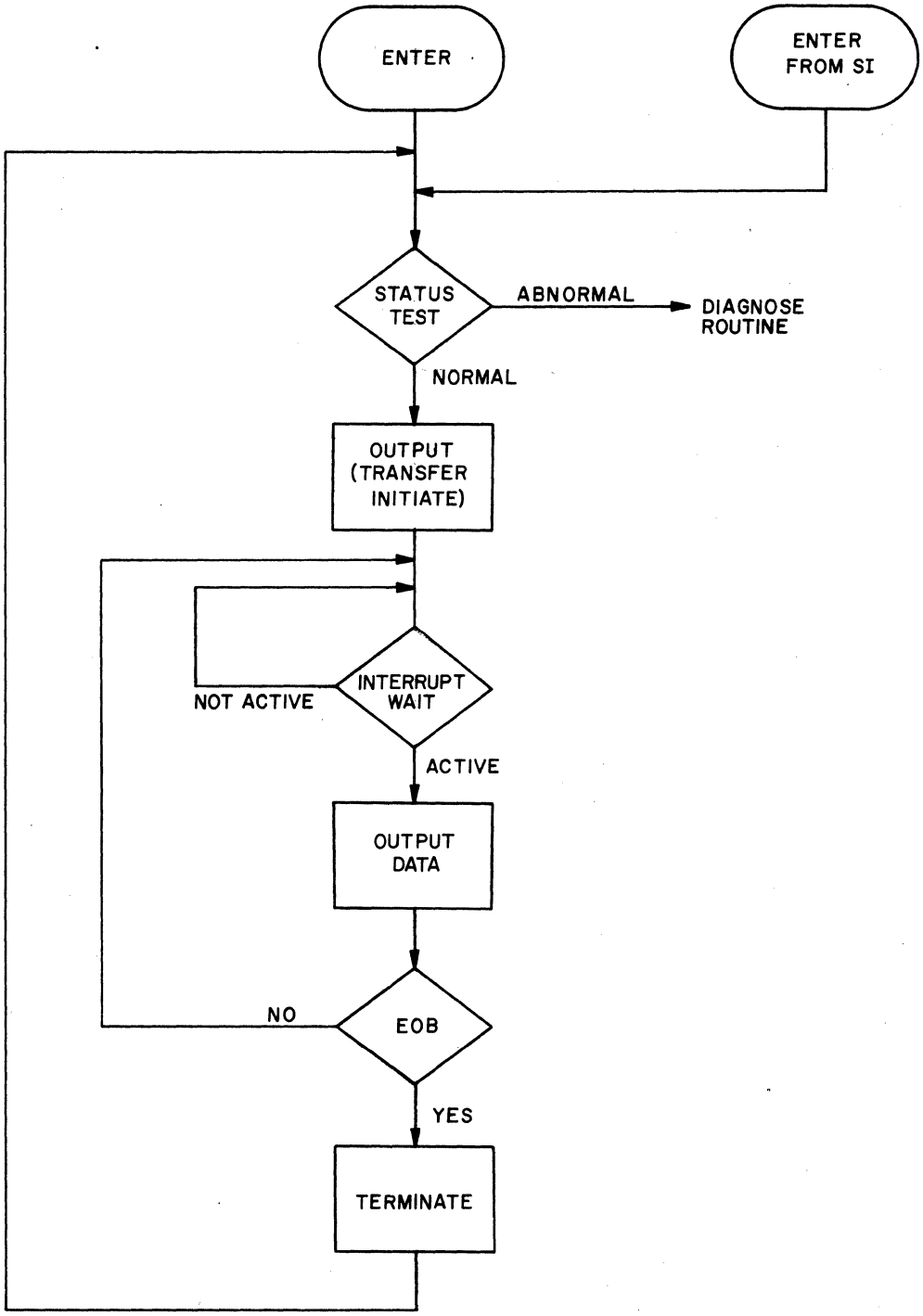


TABLE 10-1

MNEMONIC LIST FOR PAPER TAPE PUNCH

MNEMONIC	DESCRIPTION	SHT#
CLKFB	MASTER CLOCK FROM BUFFER	3
CLKFBN	MASTER CLOCK FROM BUFFER (LOW TRUE)	3
CLSTAN	CLEAR STATUS REGISTERS	3
CONT	CONTROL INSTRUCTION DECODED	3
CTLCMD	CONTROL COMMAND	3
DAFB0N TO DAFB5N	DEVICE ADDRESS FROM BUFFER	1
DATARS	DATA REQUEST STROBE	8
DFB00 TO DFB15	OUTPUT DATA FROM BUFFER	4
DFB00N TO DFB15N	OUTPUT DATA FROM BUFFER (LOW TRUE)	4
DFD00N TO DFD15N	OUTPUT DATA FROM DRIVER RECEIVER MODULE	4
DIREQN	DATA INTERRUPT REQUEST	2
DISET	DATA INTERRUPT SET	2
DISETN	DATA INTERRUPT SET (LOW TRUE)	2
DRCDFN	COMMAND/DATA FUNCTION FROM DRIVER RECEIVER MODULE	3
DRCLKN	MASTER CLOCK FROM DRIVER RECEIVER MODULE	3
DRDA0N TO DRDA5N	DEVICE ADDRESS FROM DRIVER RECEIVER MODULE	1
DRDIRN	DATA INTERRUPT REQUEST TO DRIVER RECEIVER MODULE	2
DRDIUN	DATA INTERRUPT UPDATE QUEUE FROM DRIVER RECEIVER MODULE	2
DRICBN	INITIAL CONDITION BUSS FROM DRIVER RECEIVER MODULE	2
DRID0N TO DRID5N	SOURCE ID TO DRIVER RECEIVER MODULE	2
DRIOFN	INPUT/OUTPUT FUNCTION FROM DRIVER RECEIVER MODULE	3
DRIOSN	I/O SYNC FROM DRIVER RECEIVER MODULE	3
DRSIRN	SERVICE INTERRUPT REQUEST TO DRIVER RECEIVER MODULE	1
DRSIUN	SERVICE UPDATE QUEUE FROM DRIVER RECEIVER MODULE	1
DTD00N TO DTD15N	INPUT DATA TO DRIVER RECEIVER MODULE	5
DTRD0N TO DTRD7N	DATA TO RELAY DRIVER (LOW TRUE)	8
ENID01 & ENID02	ENABLE DATA TO DRIVER RECEIVER MODULE	3
ENIS01 & ENIS02	ENABLE STATUS GATES TO DRIVER RECEIVER MODULE	3
ENOUT	ENABLE OUTPUT DATA TO RELAY DRIVERS	7
ENOUTN	ENABLE OUTPUT DATA TO RELAY DRIVERS (LOW TRUE)	7
FETRDN	FEED TO RELAY DRIVER (LOW TRUE)	8
ICBFB	INITIAL CONDITION BUSS FROM BUFFER	2
ICBFBN	INITIAL CONDITION BUSS FROM BUFFER (LOW TRUE)	2
ICBPN	INITIAL CONDITION BUSS PUNCH (LOW TRUE)	8
INDCMN	INPUT DATA COMMAND	3
INTSTB	INTERRUPT STROBE	3
ISLM07	STATUS BIT 07 (BUSY)	8
ISLM08	STATUS BIT 08 (DATA READY, LOW TRUE)	8
ISLM09	STATUS BIT 09 (TAPE LOW)	8
LDCMRN	LOAD COMMAND REGISTERS	3
MDESEL	MODE SELECT	3
OUDCMN	OUTPUT DATA COMMAND	3

TABLE 10-1

MNEMONIC LIST FOR PAPER TAPE PUNCH

MNEMONIC	DESCRIPTION	SHT#
PICKUP	MAGNETIC PICKUP FROM PUNCH	7
POWER	PUNCH POWER IS ON	7
POWERN	PUNCH POWER IS ON (LOW TRUE)	7
POWOSD	POWER ON START DELAY	7
POWTD	POWER ON TO RELAY DRIVER	7
RIOTIS	REGISTER I/O TRANSFER INITIATE COMMAND	3
RSDRQN	RESET DATA REQUEST	3
RSTSTN	ICB OR INSTRUCTION RESET (LOW TRUE)	2
SELCTN	SELECT INSTRUCTION DECODED (LOW TRUE)	3
SETSIN	TERMINATE COMMAND AND NOT BUSY SET SI	3
SICNT	SERVICE INTERRUPT CONNECTED	1
SICNTN	SERVICE INTERRUPT CONNECTED (LOW TRUE)	1
SIREQN	SERVICE INTERRUPT REQUEST	1
SIRQST	SERVICE INTERRUPT REQUEST SET	1
SIRSTN	SERVICE INTERRUPT RESET	1
STSIRQ	SET SI REQUEST	8
TAPELN	TAPE LOW FROM PUNCH (LOW TRUE)	8
TERLA	TERMINATION LATCH	8
TERM	TERMINATE COMMAND	3
TERMN	TERMINATE COMMAND (LOW TRUE)	3
TUHPRI	THIS UNIT HAS PRIORITY	1
TUISEL	THIS UNIT IS SELECTED	1
5VPA TO 5VPG	PULL UP VOLTAGE	1

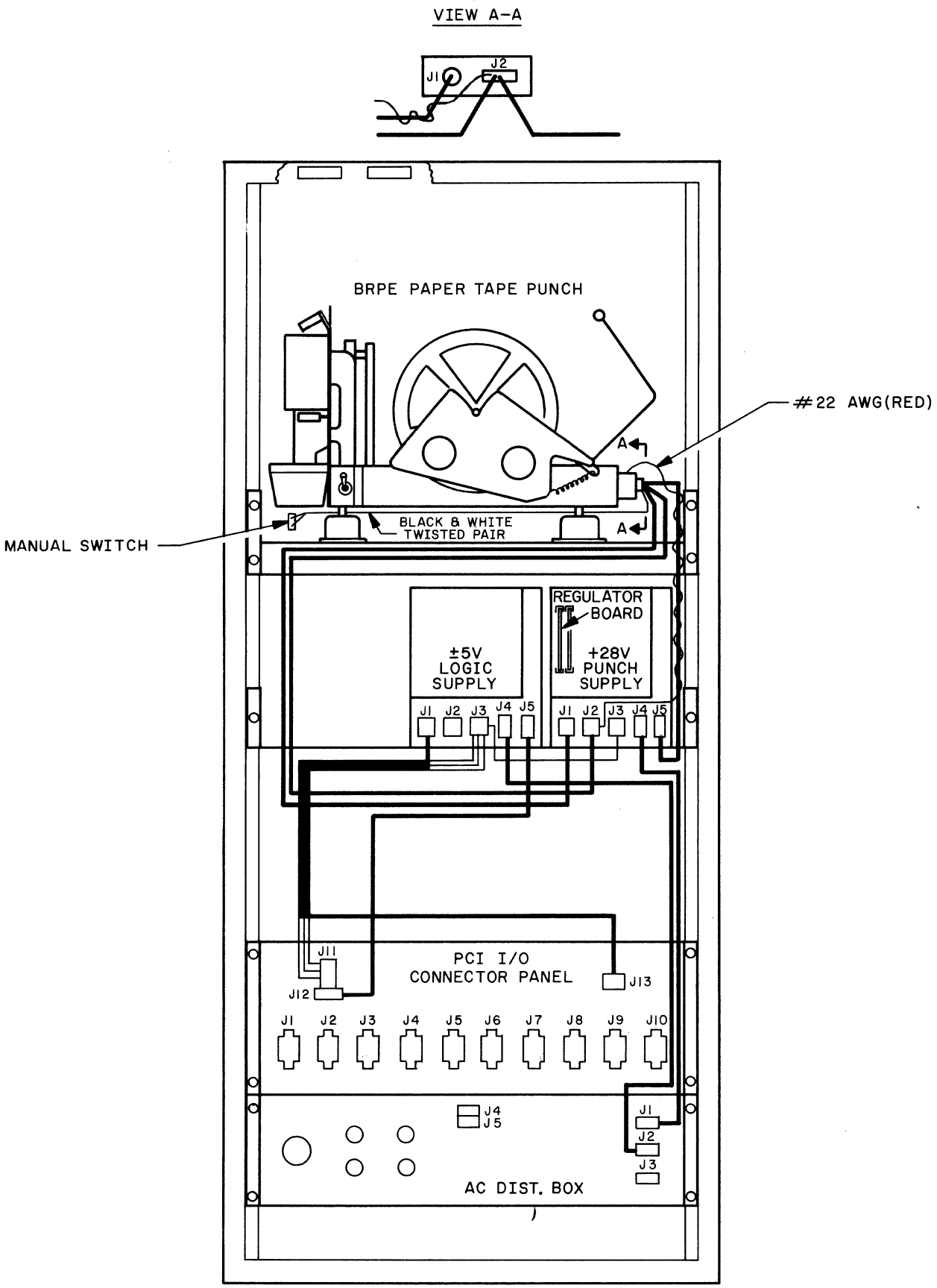


FIGURE 10-1 BRPE RACK CABLING

CABLE SUMMARY

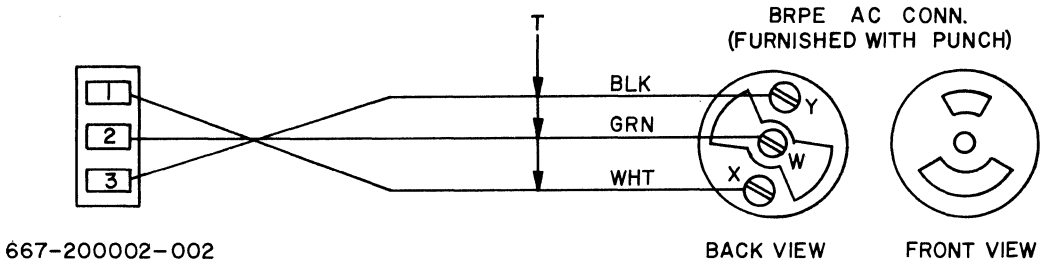
Logic Supply	to	Controller Box
J1		J13
J3		J11
Logic Supply	to	+28V Supply
J3		J3
Logic Supply	to	AC Dist. Box
J4		J2
Logic Supply	to	Controller Box
J5		J12
+28V Supply	to	BRPE Connector
J1		J2
J2		
+28V Supply	to	AC Dist. Box
J4		J1
+28V Supply	to	BRPE Power Connector
J5		J1

PUNCH POWER HARNESS

WIRE NO.	FROM	TO	COLOR
1	P11-A I/O	P3-5L	Red
2	P11-B I/O	P3-6L	Black
3	P11-E I/O	P3-1L	Green
4	P11-F I/O	P3-2L	Black
5	P11-C I/O	P3-3L	Red
6	P11-D I/O	P3-4L	Black
7	P3-1P	P3-3L	Red
8	P3-2P	P3-4L	Black
9	P13-4 I/O	P1-4L	White
10	P13-5 I/O	P1-5L	Black
11	P13-7 I/O	P1-7L	Green
12	P13-8 I/O	P1-8L	Black
13	P13-9 I/O	P1-9L	Red
14	Logic Breaker Com.	P1-1L	Red
15	Logic Breaker N. C.	P1-2L	White

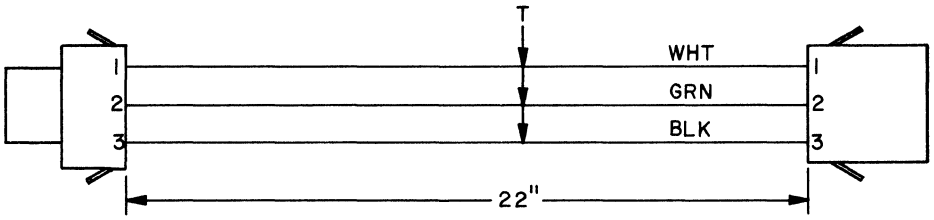
NOTE: L is Logic Supply - P is Punch Supply - I/O is I/O Panel Conn.

AC CABLE J5 PUNCH P.S. TO BRPE AC CONN. J1
16 AWG IPVC TWISTED 40" LONG



667-200002-002 BACK VIEW FRONT VIEW

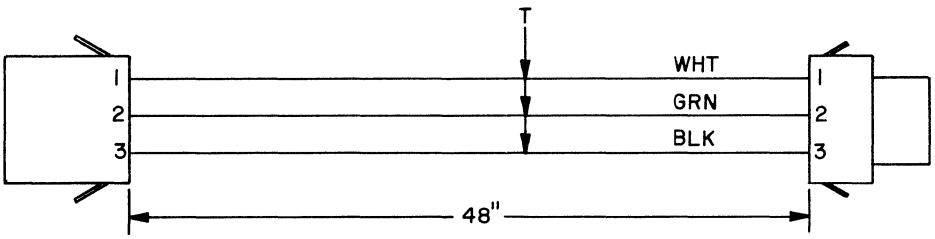
AC CABLE J4 PUNCH P.S. TO AC PANEL J1



667-200002-001 16 AWG IPVC TWISTED 667-200002-002

AC CABLE J4 LOGIC P.S. TO AC PANEL J2
SAME AS ABOVE EXCEPT 42" LONG

AC CABLE J5 LOGIC P.S. TO CONTROLLER J12



667-200002-002 16 AWG IPVC TWISTED 667-200002-001

FIGURE 10-2 A/C Cabling

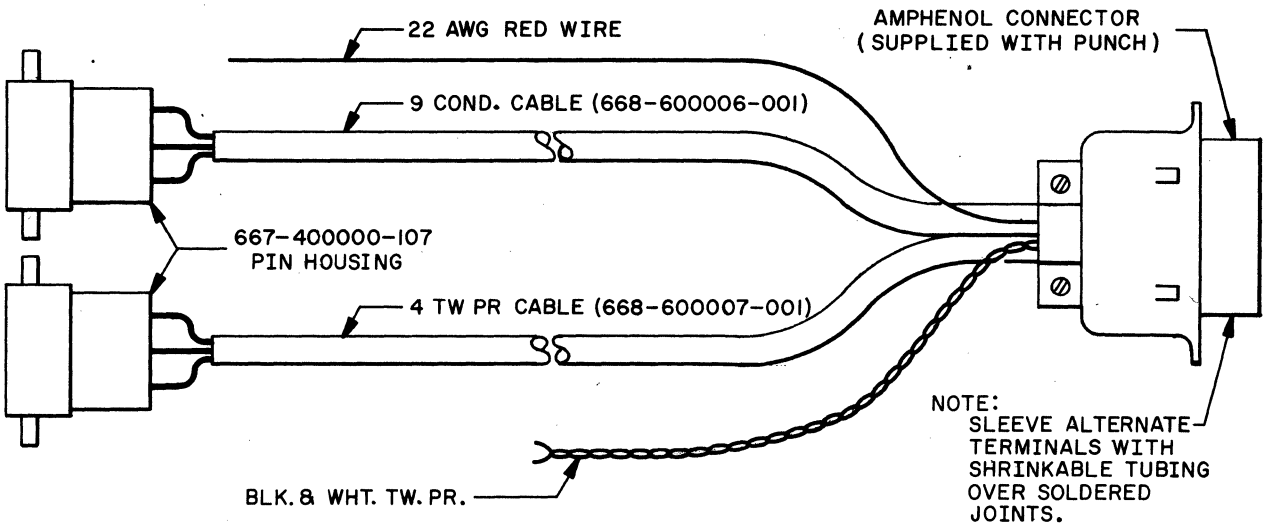


FIGURE 10-3 CONTROL CABLE

PAPER TAPE PUNCH CONTROL CABLE

WIRE NO.	FROM	TO	COLOR
1	J1-1PS	J2-8P	Black
2	J1-2PS	J2-1P	Red
3	J1-3PS	J2-2P	White
4	J1-4PS	J2-3P	Green
5	J1-5PS	J2-4P	Orange
6	J1-6PS	J2-5P	Black
7	J1-7PS	J2-6P	Brown
8	J1-8PS	J2-7P	Yellow
9	J1-9PS	J2-9P	Violet
10	J2-2PS	J2-24P	Black
11	J2-3PS	J2-12P	Red
12	J2-4PS	S1-N.O.	White
13	J2-5PS	S1-Com.	Black
14	J2-6PS	J2-21P	Black
15	J2-9PS	J2-20P	Blue
16	J2-7PS	J2-18P	Green
17	J2-8PS	J2-18P	Black
18	J2-1PS	J2-13P	Red

NOTE: PS is Punch Power Supply - P is Amphenol Connector on Punch.

TABLE 10-2

BRPE CABLE CONNECTION

SIGNAL NAME	3M CONNECTOR & PUNCH SUPPLY DRIVER BOARD XY3D	AMP CONNECTOR
N/C	1	13A
N/C	14	14A
POWTD	2	13B
Ret.	15	14B
TAPELN	3	11A
Ret.	16	12A
PICK-UP	4	11B
Ret.	17	12B
FETRDN	5	11C
Ret.	18	12C
DTRD7N	6	9A
Ret.	19	10A
DTRD6N	7	9B
Ret.	20	10B
DTRD5N	8	9C
Ret.	21	10C
DTRD4N	9	7A
Ret.	22	8A
DTRD3N	10	7B
Ret.	23	8B
DTRD2N	11	7C
Ret.	24	8C
DTRD1N	12	5A
Ret.	25	6A
DTRD0N	13	5B
Ret.	26	6B
Used only when punch and controller are in separate cabinets.	+5	16D, 17D, 18D
	Ret.	16F, 17F, 18F

XI. 2315 COMPATIBLE CARTRIDGE

MOVING HEAD DISC CONTROLLER

GENERAL

The moving head disc controller allows a maximum of four independently addressable disc drives of the same bit density to be attached by a simple "daisy-chain" connection to a common interface. Specifications are as follows:

Model No.	4126
Bit Density	2200 BPI
Tracks per Cartridge	406
Tracks per Cylinder	2
Cylinders per Cartridge	203
Sectors per Track	32
16 Bit Words per Sector	100
Word Transfer Rate	97.625 KHz
Words per Cartridge	1,299,200
Medium	IBM 2315 Type Cartridge with double density surfaces.
Average Rotational Latency	20 MSEC.
Maximum Head Positioning Times	
. Single Cylinder	15 MSEC.
. Average	70 MSEC.
. 200 Cylinders	135 MSEC.

The controller features overlapping seeks and automatic sector, head, and cylinder switching. A logical record may be a portion of a sector or may consist of any number of contiguous sectors up to the capacity limit of the cartridge. Record size is controlled by the word count. End of Record, End of Device and End of File indicators are provided to aid in file organization. Four words of buffering are provided by the controller to compensate for possible I/O Latency conditions.

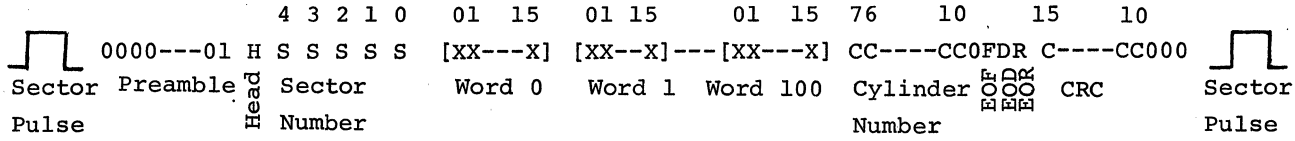
CMHD transfer rates normally require the controller to operate with a Register File DMP; however the controller may also operate in the programmed I/O mode when the device can be insured of dedicated machine access (e.g. FILL operation). A Register File DMP channel is required, however, when CMHD's are interfaced to standard MAX software operating systems. Hardware automatic cylinder position verification is maintained in the controller by initially preparing the cartridge surface with sector/head/cylinder number and thereafter writing or reading only when a sector/head/cylinder comparison exists.

Automatic restore to cylinder zero/head zero of drive 0 occurs upon the detection of master clear, thereby accomodating the FILL macro.

No hardware is provided for the indication of defective tracks and/or assignment of alternate tracks. Hence, either perfect cartridges are utilized or a software system for alternate track assignment is used.

TRACK FORMAT

Data is recorded serially bit by bit in the following format:



WRITE LOCK OUT

A cylinder protection feature is provided via a panel of eight manual switches. Write is inhibited in groups of eight physical cylinders. Should an attempt to write on a protected track occur, an SI is generated and appropriate status indicated. Write lock out applies only to the low order cylinders of drive 0. A maximum of 409,600 words may be locked out when all eight switches are active.

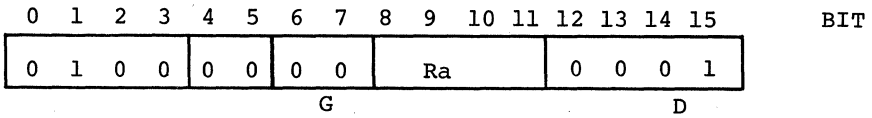
INSTRUCTIONS

The CMHD controller responds to the basic I/O instructions - Input Data, Input Status, Output Data, Output Command.

OUTPUT COMMAND INSTRUCTION (OCA)

This instruction causes the contents of the register specified by Ra to be transferred to the controller as a command.

COMMAND CODE



Bit one of the transfer initiate write and read commands defines the I/O transfer mode. See Figure 11-1. Bit one = 0 specifies programmed I/O mode. Bit one = 1 specifies Register file DMP transfer mode.

HEAD/DRIVE SELECT

The issuance of this command causes the controller to store the specified unit number (bits 14 and 15) in the unit register; which, in turn selects the drive. The drive unit bits are binarily coded as drive 0 through 3. This command also causes the selection of one of the two heads in a cylinder via bit 7.

This command does not cause the controller to go busy.

Head/drive select resets all resettable status. Master Clear selects drive 0, cylinder 0 and head 0. Head/drive select does not cause an SI under any condition.

Physical drive identification is independent of actual position in the daisy chain arrangement. Drive identification is maintained via a jumper on the mother board in each drive.

DISC PREPARATION

Each disc pack (cartridge) must initially be prepared with the correct sector, head, and cylinder numbers. The disc prep mode is established for writing by the issuance of a head/drive select command with bit 13 set to a one. The mode is maintained until a new head/drive select is issued resetting prep mode.

Disc prep mode is different from normal write in that cylinder, sector and head numbers are written without first obtaining read compares. The cylinder is assumed to be correct if the drive does not respond with a seek error. The head is assumed to be correct. The correct sector is established by counting sector pulses from the beginning of the track (index pulse).

The sector is written upon receipt of a programmed write command in the normal manner. The data written may be of any pattern.

The entire disc (203 cylinders) must be prepared and checked either sequentially or randomly.

Before a normal read or write may be attempted, the track to be operated on must be prepped in its entirety (32 sectors).

The setting of disc prep mode does not cause the controller to go busy or generate an SI.

CONTINUOUS SCAN

The Continuous Scan command is issued in the select format (bit 8 = one) and it provides the method of detecting seek complete used in overlapping seeks. It takes precedence over all other functions in the select format such as Head/Drive Select.

Continuous Scan causes the controller to go busy and sequentially interrogate the seek complete status of each CMHD. The controller remains busy scanning drives until the occurrence of one of the following, at which time busy is reset.

1. Master clear is issued.
2. Terminate is issued.
3. Seek complete is true on a drive that was previously commanded to seek. At this time the unit bits of the first drive encountered sequentially are presented in the status word. It should be noted that other drives may be in the seek complete state after a seek command. This is unknown since the scanning operation ceases after the first seek complete is encountered. The seek complete condition of the remaining drives may be determined by either issuing a head/drive select command or scan operation, followed by ISA.

If the SI is connected with a NO-OP, cylinder select or R/W command prior to the seek and continuous scan commands, in addition to going not busy, an SI is generated by the issuance of a terminate or seek complete.

A word of caution is given on continuous scan. If at any time after the issuance of a cylinder select command an SI disconnect is given via a NO-OP command, then the fact (storage element) that the seeking drive was told to seek is reset. Therefore, non-busy or SI cannot occur for that drive or any others during a continuous scan, as a result of seek complete.

Also it is important to note that due to the asynchronous nature of the scan with respect to the issuance of a terminate, any SI generated after the terminate command is a result of the terminate and not a seek complete. However, if a seek complete did occur at approximately the same time as the terminate, it would not be lost and it would be detected during the next scan operation.

TERMINATE/EOB/MPE

The issuance of a terminate while the controller is busy causes the immediate termination of data transfer. The controller remains busy, however, until the read/write logic detects the end of the current sector. Any data check errors detected (also applies to the portion of the sector not transferred to the computer in read mode) are indicated in the status word after the SI generation. A terminate issued while controller not busy will cause the immediate generation of an SI. Bit 7 of the terminate command when set specifies that a memory parity error has been detected during a DMP transfer. The condition may be checked with an ISA instruction because bit 4 of the status word is set by MPE in terminate. A terminate of this type is normally hardware generated.

An EOB command, issued in conjunction or independently of Terminate, causes the immediate generation of a DI.

NO-OP

The NO-OP command is accepted by the controller regardless of controller busy status and causes the connection or disconnection of the data or service interrupt levels as specified by bits 2 and 3. See Figure 11-1. If the controller is not busy, NO-OP resets all resettable controller status indicators.

CYLINDER SELECT

The issuance of this command causes the controller to compare the contents of the selected drive cylinder register and bits 8 through 15 of the command. If the present address and desired address are equal, the controller takes no further action and does not go busy. If they are unequal, the controller goes busy and initiates a seek operation to the drive. A status test of controller busy immediately following this command will indicate whether a seek was initiated or not. If initiated, the controller will remain busy for 25 µs to 55 µs, at the end of which time an SI will be generated, if connected. If an invalid cylinder address (greater than 202 but not a restore) is used, seek error status will be indicated at this time. Another SI is generated if connected during a scan operation as a result of seek complete.

If the drive is inoperable, or seeking, an SI occurs immediately (if connected) and the cylinder select is not attempted.

RESTORE

If a cylinder select is issued with an address of FF hexadecimal, a restore command will be issued to the selected drive. The controller will go busy for 25 µs to 55 µs, at the end of which time an SI will be generated, if connected. The drive will continue busy seeking until the head positioner returns to home position and is then located over track 0. This command is used to recover from seek error conditions. A restore will automatically be issued to disc drive 0 when a master clear occurs. This feature allows a console generated bootstrap fill starting at cylinder zero.

Disc drives are automatically restored when their power is turned on, hence no software initialization is required.

If the drive is inoperable, or seeking, an SI occurs immediately (if connected) and the restore is not attempted.

WRITE COMMAND

If the selected drive is operable, the write command causes the controller to read the selected track, searching for head, cylinder and sector comparison, synchronizing on each sector prior to the one desired to be written, and the write current is switched "on" during the inter-sector gap.

A preamble is written, followed by head/sector number, data, cylinder number, control bits and CRC.

If the word count is greater than 100 the controller continues writing, automatically incrementing sector, head, and cylinder until the word count is exhausted. Cylinder advance is treated as a normal cylinder seek followed by a write since a complete compare is made before writing is resumed.

If the word count is not a multiple of 100 words, (or an underflow occurs) the controller fills the remainder of the last sector with zeros.

When the word count does go to zero, an end of record bit is written in the control character. If the end of file bit and/or end of device bit was set to "one" during command initiation, these bits are also written in the control character.

An SI is generated (if connected) after the write command is initiated as a result of one of the following conditions:

1. The device is inoperable, or seeking. The SI occurs immediately and the command is not attempted.
2. The SCS bit was set in the command word and a seek complete has previously occurred. The SI occurs at the time of detection. The command is aborted and aborting unit bits and SKC are presented as status.
3. A head, cylinder or sector comparison does not occur after one complete revolution. The SI occurs after one revolution or sooner and seek error is set.
4. An attempt is made to write on a cylinder which is write protected. The SI occurs immediately and write lock out violation is set in the status word.
5. An underflow or MPE error is detected. The SI occurs after the last CRC is written on the sector where the underflow occurred, and overflow error is set.
6. Completion of the write operation. The SI occurs after the last CRC is written on the sector where TC went to zero.
7. An attempt is made to increment into a write protected cylinder 203. The SI occurs after the last CRC is written on the sector prior to the occurrence of the violation. Status is indicated accordingly.

The controller goes busy at the initiation of the write command (if operable) and remains busy until the CRC character is written at the end of the last sector, after which an SI is generated. While busy, the controller will accept only terminate, EOB and NO-OP commands. Command acceptance resets previous controller resettable status indicators. The DMP automatically generates a terminate when TC=0 or after detecting a MPE.

READ COMMAND

If the selected drive is operable, the read command causes the controller to read the selected track, searching for head, cylinder and sector comparison. Comparison occurs at the sector desired to be read.

When comparison occurs, the controller commences to send data to the computer, automatically incrementing sector, head, and cylinder (if necessary) until the word count goes to zero or an EOR, compare, CRC or overflow error is detected.

Cylinder advance is treated as a normal cylinder seek followed by read in that a complete compare is made before reading is resumed.

CRC is checked for each sector read and data transfer terminated on the sector where an error is detected. Data transfer is also terminated on a sector when EOR, O/F is detected. A status test, after the read operation is complete, will indicate whether EOR, EOD, and/or EOF bits were set in the control word when written.

An SI is generated (if connected) after the read command is initiated as a result of one of the following conditions:

1. The drive is inoperable, or seeking. The SI occurs immediately and the command is not attempted.
2. The SCS bit was set in the command word and a seek complete had previously occurred. The SI occurs at the time of detection. The command is aborted, and aborting unit bits and SKC are presented as status.
3. A head, cylinder or sector comparison does not occur after one complete revolution. SI occurs after one revolution, or sooner and seek error is set.
4. A CRC error is detected. The SI occurs on the sector where the error is detected and CRC error is set.
5. An EOR bit is detected. The SI occurs on the sector where the EOR is detected. EOR bit is set in the status word.
6. An overflow error is detected for multisector records. The SI occurs at the end of the sector during which the overflow occurred, and overflow error is set.
7. Completion of the Read operation (word count goes to zero). The SI occurs at the end of the sector on which the terminate is received.

The controller goes busy at initiation of the read command and remains busy until the SI is generated. Command acceptance resets previous controller resettable status indicators. The DMP automatically generates a terminate command when TC=0 or after detecting a MPE.

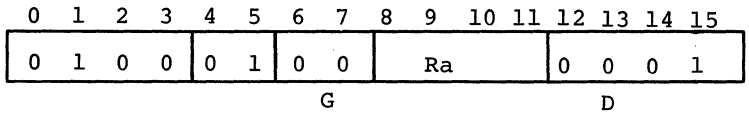
SINGLE CYCLE SCAN

The single cycle scan mode is implemented in a read or write command by setting bit 8 equal to one. SCS is similar to continuous scan except that only one cycle of interrogation is attempted per R/W command. If desired, SCS must be selected with each R/W command.

With SCS selected, the controller goes busy as though a normal R/W operation was in process. However, before read or write is attempted, a one cycle interrogation of the seek complete status of all four drives is initiated. If none of the four drives has a true seek complete status (as a result of a previous seek command) then the desired R/W operation is initiated. If a seek complete is established at any drive in the sequential cycle, continuance of the cycle is curtailed. In addition, the R/W operation is aborted, and the aborting unit bits are presented in the status word, as well as seek complete status at the detection of the seek complete. The controller also goes not busy generating an SI (if connected) at this time.

OUTPUT DATA INSTRUCTION

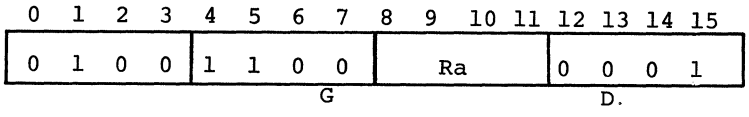
FORMAT:



This instruction causes the contents of the register specified by Ra to be transferred to the controller as data. This insturction is only used for programmed I/O operations, since DMP handles data transfers automatically.

INPUT DATA INSTRUCTION

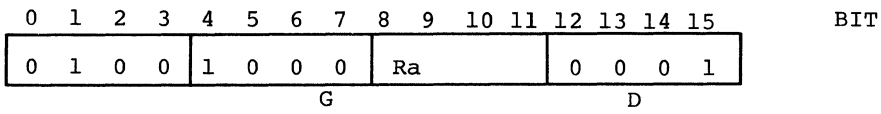
FORMAT:



This instruction causes the controller to transfer data to the register specified by Ra. It is used only for programmed I/O operations, since DMP handles data transfers automatically.

INPUT STATUS (ISA)

This instruction enables the controller to transfer status to the register specified by Ra. All status bits except bits 3,5,6,7,12,14 and 15 are reset by a new command. The status word bit format is shown in Figure 11-1.



Ra Contents

Bit 0 - Error - This bit being reset (0) indicates that one or more of bits one through six are set. See Bit 5 for an exception.

Bit 1 - Underflow/Overflow - This bit set (1) indicates that data was not transferred by the CPU at a sufficient rate during write (underflow) or read (overflow). Data transfer is terminated at detection of this error. For writes, the remainder of the sector is filled with zeroes.

Bit 2 - CRC Error - This bit set (1) indicates that a CRC error was detected upon reading a sector. During multisector (sequential) reads, data transfer terminates at the detection of the error.

Bit 3 - Inoperable - This bit set (1) indicates that the selected drive is in one of the following conditions:

1. Power Off
2. Disc Cartridge not loaded
3. Door Open
4. Load/Run switch in load position
5. Disc is not up to speed
6. Heads not loaded
7. Write Circuit Malfunction

Selected drive seeking does not set inoperable. If the unit goes inoperable during a command, an SI is generated.

Bit 4 - Memory Parity Error - Indicates when set to 1 that the last read or write operation was terminated due to the detection of a memory parity error (DMP operations only).

Bit 5 - Write Lock Out Violation - This bit set to 1 indicates that the selected cylinder group is protected. If bit zero is also reset (0), an attempt was made to write to a protected group of 8 cylinders.

Bit 6 - Seek Error - This bit set to 1 indicates that the selected unit is not positioned to the desired cylinder. This error may occur upon initiation of a seek, due to addressing of a cylinder greater than 202, or when a seek completes, due to a device malfunction. The error may also be set during a read/write operation if the cylinder and head number written on the track do not match the expected values. Data transfer does not occur and write is not enabled if a seek error is detected. To

recover from this error, a restore command must be issued to the drive. If the error was caused by a drive malfunction, the only means of resetting the status bit is by the restore operation.

Bit 7 - Controller Busy - Indicates when set to 1 that the controller is busy reading, writing, initiating a cylinder select or scanning for a seek complete. The controller does not go busy due to a head/drive select command. An SI is generated when the controller goes not busy.

Bit 8 - Data Ready - Indicates when reset (0) that a data buffer is ready to send or receive data. This status bit would only be useful for programmed I/O transfers.

Bit 9 - End of Device - Indicates when set to 1 that the last record read (single or multiple sector) was written as an End of Device record.

Bit 10 - End of File - Indicates when set to 1 that the last record read (single or multiple sector) was written as an End of File record.

Bit 11 - End of Record - Indicates when set to 1 that the last sector read was either a single sector logical record or the last sector of a multi-sector logical record. Detection of an End of Record will terminate data transfer during read operations whether or not transfer count has gone to zero.

Bit 12 - Device Busy Seeking - This bit is true (1) if the selected drive is busy seeking to a new cylinder.

Bit 13 - Seek Complete - This bit true (1) indicates that an SI occurred as a result of a seek complete scan operation. It will not become active if an SI disconnect is given via a NO-OP command after the issuance of a cylinder select.

Bits 14 & 15 - Unit Number - These bits indicate the binary address of the drive presently selected by the controller.

STANDARD ASSIGNMENTS

DEVICE ADDRESS	I/O PRIORITY	INTERRUPT LOCATIONS		DMP LOCATIONS	
		DI	SI	TC	TA
01	0	81	C1	61	71

PHYSICAL CHARACTERISTICS

DISC DRIVE

Rack Mountable with slides.

Width 17 1/2"

Depth	22 7/8"
Height	6 1/2"
Weight	43 pounds
Power	+15V ± 5%, 7 Amp DC
	-15V ± 5%, 7 Amp DC
Rotation	1,500 rpm ± 1%
Average Latency Time	20 msec (half rotation)
Head Positioning	15 msec - Track to Track
	70 msec - average
	135 msec - 200 Track movement
Bit Density	2200 BPI
Track Density	100 TPI
Bit Transfer	1562 KHz
Tracks per cylinder	2
Cylinders per cartridge	203
Medium	IBM 2315 Type cartridge with double density surfaces 15" diameter 16 sectors.
Cable Length	20 feet including daisy chain up to four drives.

POWER SUPPLY

The power supply has the capacity to control two drives with the following specifications. It mounts in hardware adaptable for one or two supplies.

Width	8"
Depth	17"
Height	3.3"
Weight	30 pounds
Output Power	+15V ± 5% 14.4 Amp DC
	-15V ± 5% 11.8 Amp DC
Input Power	120 VAC, 4 Amp

ENVIRONMENTAL CONDITIONS

Temperature	60° to 90°F ambient, to assure cartridge interchange ability
Relative Humidity	20% to 80%

TABLE 11-1

COMPATIBLE CARTRIDGE MOVING HEAD DISC CONTROLLER

MNEMONIC	DESCRIPTION	SHT#
AA	ADDRESS ACKNOWLEDGE	25
AALAI	ADDRESS ACKNOWLEDGE OR LOGICAL ADDRESS INTERLOCK	25
AALAIN	ADDRESS ACKNOWLEDGE OR LOGICAL ADDRESS INTERLOCK (LT)	25
ADDZEN	DEVICE ADDRESS EQUALS ZERO	7
ALLRW	ALLOW READ OR WRITE	10
BCS	BIT COUNTER STROBE	18
BCSG2N	BIT COUNTER STAGE 2 (LT)	9
BCSG3	BIT COUNTER STAGE 3	9
BCSN	BIT COUNTER STROBE (LT)	18
BCSG3N	BIT COUNTER STAGE 3 (LT)	9
BCSG4	BIT COUNTER STAGE 4	9
BCTRZN	BIT COUNTER RESET	9
BUFEQ	DATA BUFFER ADDRESS EQUALITY	22
BUFLDN	DATA BUFFER LOAD PULSE (LT)	22
BUSY1	BUSY 1	16
BUSY2	BUSY 2	16
CLKFB	MASTER CLOCK FROM BUFFER	3
CLKFBN	MASTER CLOCK FROM BUFFER (LOW TRUE)	3
CLKSCN	CLOCK SECTOR COUNTER	18
CLOCKN	CLOCK FROM DRIVE (LT)	25
CLSTAN	CLEAR STATUS REGISTERS	3
CNTS	CONTINUOUS SCAN SET	11
CONTSN	CONTINUOUS SCAN STROBE (LT)	16
CONT	CONTROL INSTRUCTION DECODED	3
CR001	UNIT CYLINDER REGISTER BIT 1	13
CR002	UNIT CYLINDER REGISTER BIT 2	13
CR004	UNIT CYLINDER REGISTER BIT 4	13
CR008	UNIT CYLINDER REGISTER BIT 6	13
CR016	UNIT CYLINDER REGISTER BIT 16	13
CR032	UNIT CYLINDER REGISTER BIT 32	13
CR064	UNIT CYLINDER REGISTER BIT 64	13
CR128	UNIT CYLINDER REGISTER BIT 128	13
CTLCMD	CONTROL COMMAND	3
CYLCEN	CYLINDER COMPARE ERROR	14
CYLEQN	CYLINDER SELECTED EQUAL TO PREVIOUS SELECTION (LT)	13
CYLSE	CYLINDER SELECT STROBE	10
CYLSEN	CYLINDER SELECT STROBE (LT)	10
CY001	INCREMENTING CYLINDER REGISTER BIT 1	14
CY002	INCREMENTING CYLINDER REGISTER BIT 2	14
CY004	INCREMENTING CYLINDER REGISTER BIT 4	14
CY008	INCREMENTING CYLINDER REGISTER BIT 16	14
CY016	INCREMENTING CYLINDER REGISTER BIT 32	14

TABLE 11-1

COMPATIBLE CARTRIDGE MOVING HEAD DISC CONTROLLER (CONT'D)

MNEMONIC	DESCRIPTION	SHT#
CY032	INCREMENTING CYLINDER REGISTER BIT 32	14
CY064	INCREMENTING CYLINDER REGISTER BIT 64	14
CY128	INCREMENTING CYLINDER REGISTER BIT 128	14
DAFB0N TO DAFB5N	DEVICE ADDRESS FROM BUFFER	1
DATARS	DATA REQUEST STROBE	22
DD0SL	DISC DRIVE 0 SELECTED	11
SS1SL	DISC DRIVE 1 SELECTED	11
DD2SL	DISC DRIVE 2 SELECTED	11
DD3SL	DISC DRIVE 3 SELECTED	11
DFB00 TO DFB15	OUTPUT DATA FROM BUFFER	4
DFB00N TO DFB15N	OUTPUT DATA FROM BUFFER (LOW TRUE)	4
DFD00N TO DFD15N	OUTPUT DATA FROM DRIVER RECEIVER MODULE	4
DIREQN	DATA INTERRUPT REQUEST	2
DISET	DATA INTERRUPT SET	2
DISETN	DATA INTERRUPT SET (LOW TRUE)	2
DMPRQN	DMP REQUEST (LOW TRUE)	7
DRDMRN	DMP REQUEST TO DRIVER RECEIVER MODULE	7
DRDMUN	DMP UPDATE QUEUE FROM DRIVER RECEIVER MODULE	7
DMPSRS	DMP SI STROBE	15
DPINCN	DISC PREP INCREMENT SECTOR CTR ONCE	18
DPSCP	DISC PREP SECTOR COMPARE	21
DPSCPN	DISC PREP SECTOR COMPARE (LT)	21
DRCDFN	COMMAND/DATA FUNCTION FROM DRIVER RECEIVER MODULE	3
DRCLKN	MASTER CLOCK FROM DRIVER RECEIVER MODULE	3
DRDA0N TO DRDA5N	DEVICE ADDRESS FROM DRIVER RECEIVER MODULE	1
DRDIRN	DATA INTERRUPT REQUEST TO DRIVER RECEIVER MODULE	2
DRDIUN	DATA INTERRUPT UPDATE QUEUE FROM DRIVER RECEIVER MODULE	2
DRICBN	INITIAL CONDITION BUSS FROM DRIVER RECEIVER MODULE	2
DRID0N TO DRID5N	SOURCE ID TO DRIVER RECEIVER MODULE	2
DRIOFN	INPUT/OUTPUT FUNCTION FROM DRIVER RECEIVER MODULE	3
DRIOSN	I/O SYNC FROM DRIVER RECEIVER MODULE	3
DRSIRN	SERVICE INTERRUPT REQUEST TO DRIVER RECEIVER MODULE	1
DRSIUN	SERVICE UPDATE QUEUE FROM DRIVER RECEIVER MODULE	1
DTD00N TO DTD15N	INPUT DATA TO DRIVER RECEIVER MODULE	5
DTLM00 TO DTLM15	DATA BUFFER OUTPUT BITS 0-15	23
EBCTR	ENABLE BIT COUNTER	18
EBCTRN	ENABLE BIT COUNTER (LT)	18
EFLD34	ENABLE FIELD 3 AND 4	18
ENF3B	ENABLE FIELD 3B	15
ENF3BN	ENABLE FIELD 3B (LT)	15
ENID01 & ENID02	ENABLE DATA TO DRIVER RECEIVER MODULE	3
ENIS01 & ENIS02	ENABLE STATUS GATES TO DRIVER RECEIVER MODULE	3

TABLE 11-1

COMPATIBLE CARTRIDGE MOVING HEAD DISC CONTROLLER (CONT'D)

MNEMONIC	DESCRIPTION	SHT#
ENSCA	ENABLE SCAN	10
ENSCAN	ENABLE SCAN (LT)	10
FOBLKN	END OF BLOCK COMMAND	3
FIRDY	FILE READY	25
FIRDYN	FILE READY	25
FLD1	FIELD 1	9
FLD1D	FIELD 1 DATA	19
FLD2	FIELD 2	9
FLD2D	FIELD 2 DATA	20
FLD2N	FIELD 2 (LT)	9
FLD3	FIELD 3	9
FLD3A	FIELD 3A	14
FLD3AD	FIELD 3A DATA	14
FLD3B	FIELD 3B	14
FLD3BD	FIELD 3B DATA	14
FLD4	FIELD 4	9
FLD4D	FIELD 4 DATA	20
FLD5	FIELD 5	9
FLD56	FIELD 5 OR 6	15
FLD6	FIELD 6	9
GENST	GENERATED SECTOR STROBE	8
GENSTN	GENERATED SECTOR STROBE (LT)	8
HDEQN	HEAD SELECTED EQUAL TO PREVIOUS SELECTION	19
HDDYC	HEAD SWITCHING DELAY COMPLETE	17
HEAD0	HEAD 0	19
HEAD0N	HEAD 0 (LT)	19
IBAD1	INPUT BUFFER ADDRESS 1	22
IBAD2	INPUT BUFFER ADDRESS 2	22
ICBFB	INITIAL CONDITION BUSS FROM BUFFER	2
ICBFBN	INITIAL CONDITION BUSS FROM BUFFER (LOW TRUE)	2
ICBN	INITIAL CONDITION BUS (LT)	12
INCYF	INCREMENT CYLINDER FLOP	15
INCYFN	INCREMENT CYLINDER FLOP (LT)	15
INCYLN	INCREMENT CYLINDER (LT)	15
INDCMN	INPUT DATA COMMAND	3
INDEX	INDEX	25
INEARN	INITIATE EARLY TERMINATE, CRC ERROR (LT)	20
INHD	INCREMENT HEAD	15
INHDN	INCREMENT HEAD (LT)	15
INRYS	INTERROGATE SEEK COMPLETE (READY) STATUS	11
INSETN	INCREMENT SECTOR (LT)	15
INSRP	INCREMENT SECTOR CTR ONCE IN READ OR PREP MODE	10

TABLE 11-1

COMPATIBLE CARTRIDGE MOVING HEAD DISC CONTROLLER (CONT'D)

MNEMONIC	DESCRIPTION	SHT#
INTSTB	INTERRUPT STROBE	3
ISLM00	STATUS BIT 0 (ERROR POINTER)	17
ISLM01	STATUS BIT 1 (UNDER/OVERFLOW)	22
ISLM02	STATUS BIT 2 (CRC ERROR)	20
ISLM03	STATUS BIT 3 (INOPERABLE)	16
ISLM04	STATUS BIT 4 (MEMORY PARITY ERROR)	7
ISLM05	STATUS BIT 5 (WRITE LOCK OUT)	24
ISLM06	STATUS BIT 6 (SEEK ERROR)	17
ISLM07	STATUS BIT 7 (BUSY)	16
ISLM08	STATUS BIT 8 (DATA READY)	22
ISLM09	STATUS BIT 9 (EOD)	24
ISLM10	STATUS BIT 10 (EOF)	24
ISLM11	STATUS BIT 11 (EOR)	24
ISLM12	STATUS BIT 12 (DISC SEEKING)	16
ISLM13	STATUS BIT 13 (SEEK COMPLETE)	12
ISLM14	STATUS BIT 14 (UNITS MSB)	11
ISLM15	STATUS BIT 15 (UNITS LSB)	11
IUICN	INHIBIT UNIT INCREMENT (LT)	12
LAIN	LOGICAL ADDRESS INTERLOCK (LT)	25
LDCMRN	LOAD COMMAND REGISTERS	3
LDCYLR	LOAD UNIT CYLINDER REGISTER	15
LDICRN	LOAD INCREMENTING CYLINDER REGISTER (LT)	10
LDSCF	LOAD SCAN FLOPS	10
LDUCR	LOAD UNIT CYLINDER REGISTER	10
LDUCRN	LOAD UNIT CYLINDER REGISTER (LT)	10
MDESEL	MODE SELECT	3
MPEN	MEMORY PARITY ERROR (LOW TRUE)	7
NSCFF	NORMAL SECTOR COMPARE FLIP-FLOP	21
OBAD1	OUTPUT BUFFER ADDRESS 1	22
OBAD2	OUTPUT BUFFER ADDRESS 2	22
OUDCMN	OUTPUT DATA COMMAND	3
PREDO	PREAMBLE DONE	8
PREP	PREP MODE SET	18
PREPN	PREP MODE SET (LT)	18
PSECEQ	PREP MODE SECTORS EQUAL	19
PSEUSN	PSEUDO SECTOR MARK	8
PSGS8	PSEUDO SECTOR GENERATOR STAGE 8	8
PSGS9	PSEUNDO SECTOR GENERATOR STAGE 9	8
RDBLPN	READ BUFFER LOAD PULSE (LT)	21
RDCLK	READ CLOCK	25
RDDAT	READ DATA	25
RDYST	READY STROBE	10

TABLE 11-1

COMPATIBLE CARTRIDGE MOVING HEAD DISC CONTROLLER (CONT'D)

MNEMONIC	DESCRIPTION	SHT#
RESTR	RESTORE	10
RDSYC	READ SYNC ON SECTOR	18
RDSYCN	READ SYNC ON SECTOR (LT)	18
RDYSTN	READY STROBE (LT)	10
RESTRN	RESTORE (LT)	10
RGIOMD	REGISTER I/O MODE	7
RGSTB	READ GATE STROBE	8
RGSTBN	READ GATE STROBE (LT)	8
RIOTIS	REGISTER I/O TRANSFER INITIATE COMMAND	3
RSDRQN	RESET DATA REQUEST	3
RSRW	READY TO SEEK/READ/WRITE	25
RSRWN	READY TO SEEK/READ/WRITE (LT)	25
RSTDSN	RESET DATA SEQUENCER (LT)	15
RSTSTN	ICB OR INSTRUCTION RESET (LOW TRUE)	2
SECCP	SECTOR COMPARE NON-PREP	21
SECCPN	SECTOR COMPARE NON-PREP (LT)	21
SECTM	SECTOR MARK	25
SECTMN	SECTOR MARK (LT)	25
SEC01	SECTOR COUNTER BIT 1	19
SEC02	SECTOR COUNTER BIT 2	19
SEC04	SECTOR COUNTER BIT 4	19
SEC08	SECTOR COUNTER BIT 8	19
SEC16	SECTOR COUNTER BIT 16	19
SEEKI	SEEK INCOMPLETE	25
SEEKIN	SEEK INCOMPLETE (LT)	25
SELCTN	SELECT INSTRUCTION DECODED (LOW TRUE)	3
SELST	SELECT STROBE	11
SELSTN	SELECT STROBE (LT)	11
SETSIN	TERMINATE COMMAND AND NOT BUSY SET SI	3
SFCTR	SHIFT FIELD COUNTER	9
SICNT	SERVICE INTERRUPT CONNECTED	1
SICNTN	SERVICE INTERRUPT CONNECTED (LOW TRUE)	1
SIREQN	SERVICE INTERRUPT REQUEST	1
SIRQST	SERVICE INTERRUPT REQUEST SET	1
SIRSTN	SERVICE INTERRUPT RESET	1
SKERN	SEEK ERROR LATCH	17
SMSYF	SECTOR MARK SYNC FLOP	8
SPCTR	STROBE PARTS COUNTER	9
SNSETN	SCAN SET (LT)	11
STBSR	STROBE SECTOR SHIFT REGISTER	19
STBCSN	SET BUSY FOR CYLINDER SELECT	10
STROB	INTERFACE STROBE	10

TABLE 11-1

COMPATIBLE CARTRIDGE MOVING HEAD DISC CONTROLLER (CONT'D)

MNEMONIC	DESCRIPTION	SHT#
STSIRQ	STROBE SI REQUEST	16
STWPT	STROBE WRITE PROTECT STATUS	10
STWPTN	STROBE WRITE PROTECT STATUS (LT)	10
STWRON	SET FIRST WRITE DATA REQUEST	21
SXFRI	TRANSFER INITIATE STROBE	18
SXFRIN	TRANSFER INITIATE STROBE (LT)	18
TERM	TERMINATE COMMAND	3
TERMN	TERMINATE COMMAND (LOW TRUE)	3
TUHPRI	THIS UNIT HAS PRIORITY	1
TUISEL	THIS UNIT IS SELECTED	1
UFOFN	UNDERFLOW/OVERFLOW (LT)	22
UNDlFN	UNITS DIFFERENT FLOP (LT)	17
UFQ	UNITS SELECTED EQUAL TO PREVIOUS SELECTION	11
WDACK	WRITE DATA AND CLOCK TO INTERFACE DRIVER	21
WLOEN	WRITE LOCK OUT ERROR (LT)	16
WLOL	WRITE LOCK OUT LATCH	24
WLOLN	WRITE LOCK OUT LATCH (LT)	24
WLOSN	WRITE LOCK OUT STATE	24
WRDAT	WRITE DATA TO CRC REGISTER	21
WRGT	WRITE GATE SET	18
WRGTN	WRITE GATE SET (LT)	18
WRITE	WRITE MODE SET	18
WRITEN	WRITE MODE SET (LT)	18
WRSLCN	WRITE SERIAL LOAD CONTROL (LT)	21
WRXFI	WRITE OR READ TRANSFER INITIATE	15
XFERI	TRANSFER INITIATE LATCH	15
XFERIN	TRANSFER INITIATE LATCH (LT)	15
ZBCYSN	RESET BUSY CYLINDER SELECT (LT)	10
ZBSCN	RESET BUSY SEEK COMPLETE (LT)	12
ZBUSYN	RESET BUSY (LT)	16
ZSCN	RESET SECTOR CTR WITH INDEX WHEN IN PREP MODE	21
ZSTATN	RESET RESETABLE STATUS (LT)	17
01	CLOCK PHASE 1	8
01N	CLOCK PHASE 1 (LT)	8
02	CLOCK PHASE 2	8
02N	CLOCK PHASE 2 (LT)	8
03	CLOCK PHASE 3	8
03N	CLOCK PHASE 3 (LT)	8
04	CLOCK PHASE 4	8
04N	CLOCK PHASE 4 (LT)	8
5VPA TO 5VPG	PULL UP VOLTAGE	1
5VPH TO 5VPP	PULL UP VOLTAGE	7

TABLE 11-2

CONTROL AND STATUS INDICATORS

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
WRITE	1	M	D	S	Ø	EOD	EOF	IGN	SCS	IGNORED		S	S	S	S	S	XFER INIT
READ	1	M	D	S	1	IGNORED		IGN	SCS	IGNORED		S	S	S	S	S	XFER INIT
CYLINDER SELECT	Ø	1	D	S	Ø	Ø	1	IGN	C	C	C	C	C	C	C	C	CONT
TERM EOB	Ø	1	IGNORED		E	T	IGN	MPE	IGNORED								CONT
NO—OP	Ø	1	D	S	Ø	Ø	Ø	IGNORED									CONT
HEAD/ DRIVE SELECT	Ø	Ø	IGNORED					H	CS	IGNORED				P	U	U	SELECT

STATUS	E	O/F U/F	CRC	INOP	MPE	WLO	SE	BUSY	DR	EOD	EOF	EOR	DS	SKC	U	U	STATUS

XII. CENTRONICS PRINTER CONTROLLER

GENERAL

The Centronics printer functions in the register I/O mode only. Data that is transferred to the controller is done so under program control. The normal operation uses the data interrupt for buffer ready indication. If interrupts are not used, buffer ready can be determined by testing bit 8 in the status word.

If connected, a service interrupt is generated at the end of printing, device inoperable or at end of paper movement.

In the transfer initiate command, the controller is conditioned to transfer data until a terminate command is received or all 132 columns have been transferred. Upon completion of data transfer, the printer will automatically go into a print cycle. When the print cycle is complete a line feed will occur. When the line feed is completed an SI will be generated.

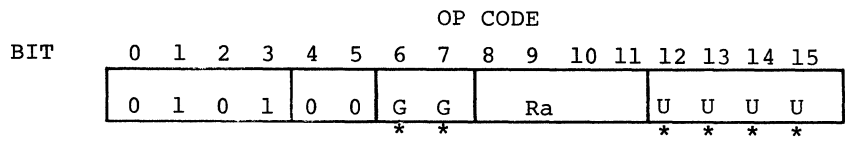
Paper movement can be accomplished without printing by using the output control format.

Since the Centronics printer is buffered, there is no minimum transfer rate. The max transfer rate will be 20 KHZ.

The following information describes the command and data formats; also provided is a program sequence, standard assignments and device characteristics.

INSTRUCTIONS

OUTPUT COMMAND

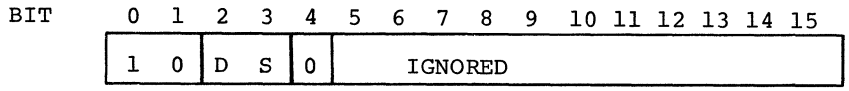


* Device Address

BITS 6 & 7 = Group No.
BITS 12 - 15 = Unit No.

The following are contents of Ra specified in the Output Command.

TRANSFER INITIATE FORMAT (Transfer, Print & Adv.)



BIT 2 = 0 - Disconnects data interrupt & resets any actice interrupt.
= 1 - Connects data interrupt to I/O interrupt level.
BIT 3 = 0 - Disconnects service interrupt & resets any active interrupt.
= 1 - Connects service interrupt to I/O interrupt level.
If connected a service interrupt will be generated upon the completion of the line feed cycle.

CONTROL FORMAT

PAPER ADVANCE

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	0	1	D	S	0	0	1	IGN		X	X	X	X	X	X	X

BIT 2 = 0 - Disconnects data interrupt and resets any active interrupt.
= 1 - Connects data interrupt to I/O interrupt level.
BIT 3 = 0 - Disconnects service interrupt & resets any active interrupt.
= 1 - Connects service interrupt to I/O interrupt level.
BITS 9-15 These bits specify number of line feeds to be performed. The following are the formats used.

BIT	9	10	11	12	13	14	15	
	0	0	0	1	0	1	0	Feed 1 Line
	0	0	0	1	1	0	0	Top of Form

If connected on service interrupt will be generated at completion of the feed.

NO-OP

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	0	1	D	S	0	0	0	IGNORED								

BIT 2 = 0 - Disconnects data interrupt and resets any active interrupt.
= 1 - Connects data interrupt to I/O interupt level.
BIT 3 = 0 - Disconnects service interrupt and resets any active interrupt.
= 1 - Connects service interrupt to I/O interrupt level. This command is used to reset all status bits in the controller.

DATA OUT

OP CODE

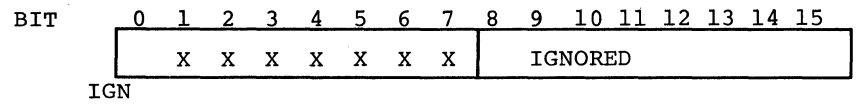
BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	0	1	0	1	0	1	G	G	Ra				U	U	U	U
							*	*					X	X	X	X

* Device Address

BIT 6 & 7 = Group No.
BIT 12-15 = Unit No.

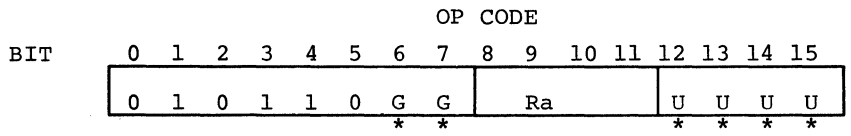
This command conditions the controller to enable data to be transferred from the register specified by Ra in the DATA OUT Command to the controller. The data bits that are received by the controller are shown below and are represented by X's.

This represents contents of Ra



USASCII CODING (64 characters)

INPUT STATUS



* Device Address

BIT 6 & 7 = Group No.

BIT 12-15 = Unit No.

This command enables the controller to transfer its status to the register specified by Ra. The status indicators are listed below:

BIT 0 = 0 - Indicates Bit 3 is set.
= 1 - No errors.
BIT 1&2 Not used.
BIT 3 = 0 - No effect.
= 1 - Inoperable = (Power OFF)
BIT 4-6 = Not used.
BIT 7 = 0 - No effect.
= 1 - Controller busy - indicates the controller/device are busy performing a print/advance on paper advance command.
BIT 8 = 0 - Data Ready, indicates buffer is empty and ready to accept data.
= 1 - No effect.
BIT 9 = 0 - No effect.
= 1 - Paper low.
BIT 10 = 0 - No effect.
= 1 - Bottom of form.
BIT 11 Not used.
BIT 12 = 0 - No effect.

BIT 12 = 1 - Hold Condition - This condition exists when power is on and the select button has not bee depressed. While in the hold condition, a command will be accepted and stored, the command will be acted on when the select button is depressed.

BIT 13-15 Not used.

INTERRUPTS

There are two standard interrupts provided - data and service interrupt. If connected, a data interrupt will be generated for each buffer read (empty) in the register I/O mode. Issuance of an EOB command, whether the controller is busy or not, will also generate a data interrupt.

The service interrupt, if connected, will be generated at the end of (transfer, print and advance) command, end of paper command, or if there is some malfunction in the device during the execution of either above commands. Issuance of a terminate command while the controller is not busy will also cause the immediate generation of an SI.

STANDARD ASSIGNMENTS

DEVICE GROUP	ADDRESS LEVEL	I/O PRIORITY	I/O INTERRUPT LOCATION (HEX)

PHYSICAL CHARACTERISTICS

Speed: 60 LPM
Line Spacing: 6 lines/inch
Character Spacing: 10 characters/inch
Number of Columns: 132 columns/line
Vertical Format: 2 channels
Paper Width: 4 inches to 14-1/2 inch form

SIZE

Height: 11-1/4 inches
WIDTH: 27-1/2 inches
Depth: 19-1/4 inches
Weight: 155 Lbs. - (crated-200 Lbs.)

Power 177VAC $\pm$ 10% 60 HZ

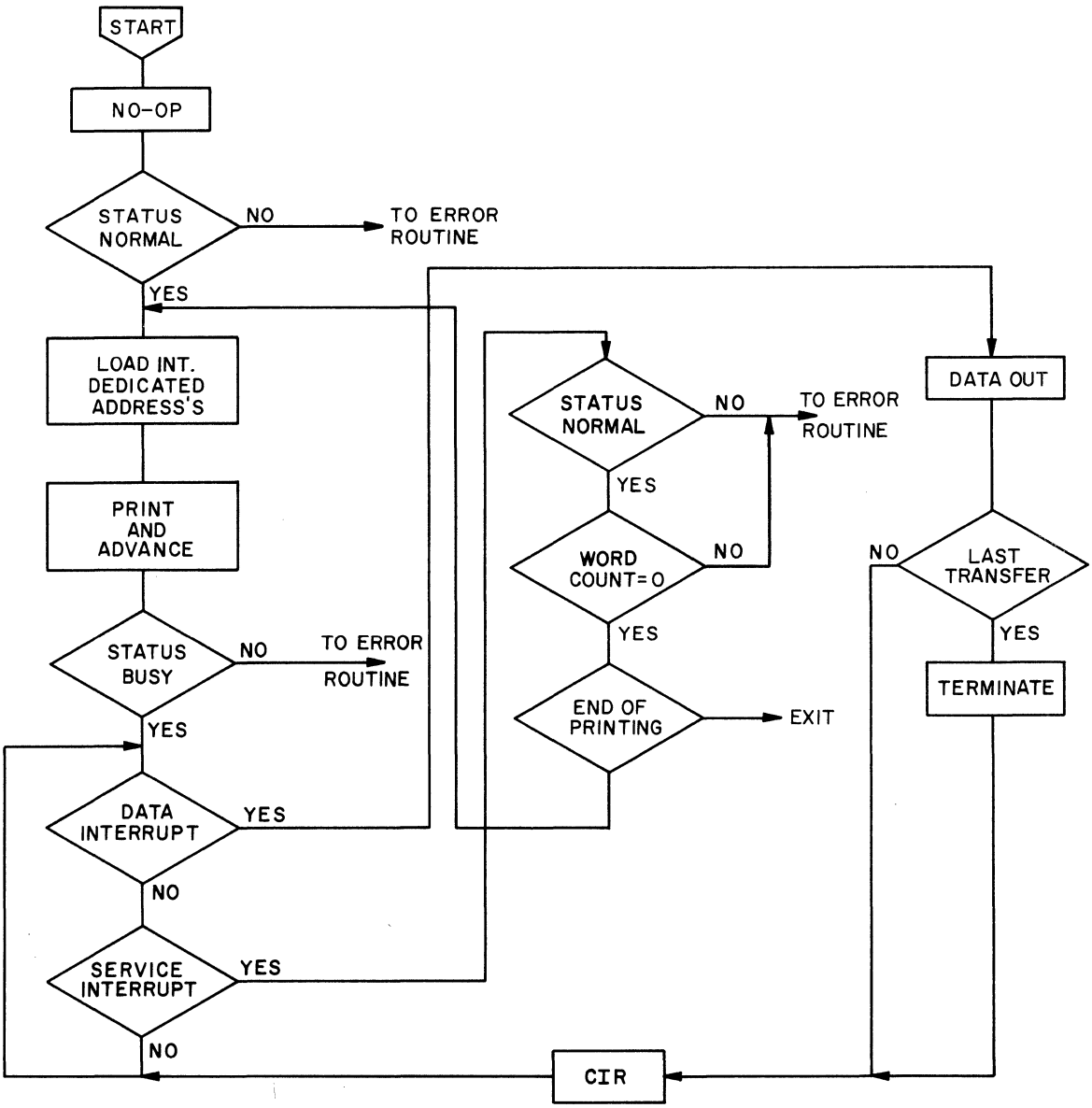
Temperature: Operating 40 degrees F to 100 degrees F
Non-Operating -40 degrees F to 160 degrees F

Humidity % RH: Operating 0 to 95
Non-Operating 0- to 98

OPERATOR CONTROLS

SWITCHES	INDICATORS
Start/Stop	Multiple Purpose
Top of Form	Hardware Alarm
Select Switch	Paper Out
Forms Override	

PROGRAMMING SEQUENCE



APPENDIX A.

PERIPHERAL DEVICE ASSIGNMENTS

PERIPHERAL DEVICE	DEVICE ADDRESS (HEX)	I/O PRIORITY	I/O INTERRUPT LOCATIONS (HEX) DATA	SERVICE	DIRECT MEMORY PROCESSOR LOCATIONS (HEX) TC	TA
DISC, MOVING HEAD	01	0	81	C1	61	71
DISC, FIXED HEAD	02	1	82	C2	62	72
MAGNETIC TAPE-HIGH SPEED	03	4	83	C3	63	73
MAGNETIC TAPE-LOW SPEED	04	7	84	C4	64	74
CARD READER	05	8	85	C5		
CARD PUNCH	06	9	86	C6		
LINE PRINTER	07	11	87	C7		
XY PLOTTER	08	12	88	C8		
HIGH SPEED PAPER TAPE PUNCH	09	13	89	C9		
TTY & HIGH SPEED PAPER TAPE READER	0A	15	8A	CA		
HIGH LEVEL ANALOG INPUT S.S.	10					
DATA INPUT		2	90	D0	60	70
CHANNEL OUTPUT		3	91	D1	61	70
WIDE RANGE ANALOG INPUT S.S.	12		92	D2		
DISCRETE I/O SUBSYSTEM 1	20-2F		A0-A7	E0-E7		
DISCRETE I/O SUBSYSTEM 2	30-3F		B0-B7	F0-F7		