Ultra 603/Ultra 603e/Ultra 604 Programmer's Reference Guide

ULMB60XA/PG2

Notice

While reasonable efforts have been made to assure the accuracy of this document, Motorola, Inc. assumes no liability resulting from any omissions in this document, or from the use of the information obtained therein. Motorola reserves the right to revise this document and to make changes from time to time in the content hereof without obligation of Motorola to notify any person of such revision or changes.

It is possible that this publication may contain reference to, or information about Motorola products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that Motorola intends to announce such Motorola products, programming, or services in your country.

Restricted Rights Legend

If the documentation contained herein is supplied, directly or indirectly, to the U.S. Government, the following notice shall apply unless otherwise agreed to in writing by Motorola, Inc.

Use, duplication, or disclosure by the Government is subject to restrictions as set forth in subparagraph (c)(1)(ii) of the Rights in Technical Data and Computer Software clause at DFARS 252.227-7013.

Motorola, Inc.
Computer Group
2900 South Diablo Way
Tempe, Arizona 85282-9602

Preface

This document provides brief board level information and complete memory map descriptions for the Ultra 603, Ultra 603e, and Ultra 604 PowerPC™ series of motherboard platforms.

This document is intended for anyone who wants to program the system board platform in order to design OEM systems, supply additional capability to an existing PC-compatible system, or work in a lab environment for experimental purposes.

A basic knowledge of computers and digital logic is assumed.

To use this document, you may wish to become familiar with the publications listed in the *Related Documentation* section in *Appendix A*.

Document Conventions

The following conventions are used in this document:

bold

is used for user input that you type just as it appears. Bold is also used for commands, options and arguments to commands, and names of programs, directories, and files.

italic

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples.

`courier`

is used for system output (e.g., screen displays, reports), examples, and system prompts.

<RETURN> or **<CR>**

represents the carriage return key.

CTRL

represents the Control key. Execute control characters by pressing the **CTRL** key and the letter simultaneously, e.g., **CTRL-d**.

Document Terminology

Throughout this document, a convention has been maintained whereby data and address parameters are preceded by a character which specifies the numeric format, as follows:

$	dollar	specifies a hexadecimal number
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

For example, “12” is the decimal number twelve, and “$12” is the decimal number eighteen. Unless otherwise specified, all address references are in hexadecimal throughout this document.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on high to low transition.

In this document, *assertion* and *negation* are used to specify forcing a signal to a particular state. In particular, *assertion* and *assert* refer to a signal that is active or true; *negation* and *negate* indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

Data and address sizes are defined as follows:

A *byte* is eight bits, numbered 0 through 7, with bit 0 being the least significant.

A two-byte is 16 bits, numbered 0 through 15, with bit 0 being the least significant. For other RISC modules, this is called a *half-word*.

A four-byte is 32 bits, numbered 0 through 31, with bit 0 being the least significant. For the other RISC modules, this is called a *word*.

An eight-byte is 64 bits, numbered 0 through 63, with bit 0 being the least significant. For the other RISC modules, this is called a *double-word*.

Safety Summary
Safety Depends On You

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola, Inc. assumes no liability for the customer's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

Keep Away From Live Circuits.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone.

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Use Caution When Exposing or Handling the CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

The computer programs stored in the Read Only Memory of this device contain material copyrighted by Motorola Inc., first published 1991, and may be used only under license such as the License for Computer Programs (Article 14) contained in Motorola's Terms and Conditions of Sale, Rev. 1/79.

This equipment generates, uses, and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used in a cabinet with adequate EMI protection.

Printed in the United States of America

August 1995

List of Tables

Product Description and Memory Maps

1

Introduction

This chapter briefly describes the Ultra 603, Ultra 603e, and Ultra 604 PowerPC™ based motherboard platforms. Unless otherwise specified, both motherboard platforms are hereafter referred to as the system board platform. The chapter begins with a board level overview and features list and ends with a complete description of the memory maps, which are the major part of this chapter.

Overview

The system board platform is an all-in-one motherboard implemented on a nine inch by thirteen inch single-plane printed circuit board. The system board platform accommodates either an MPC603, MPC603e, or MPC604 RISC processor for the MPU (factory-installed option) and an MPC105 PowerPC-to-PCI bridge as the memory controller between the processor (MPU) bus and the Peripheral Component Interconnect (PCI) (local) bus. An Intel i82378ZB PCI-to-ISA bridge component (referred to as the PIB) allows Industry Standard Architecture (ISA) bus-compatible peripherals to be accessed by the MPC60*x* processor. The system board platform also provides for the addition of a riser card which supports PCI bus and/or ISA bus cards.

Some of the standard PC (personal computer) interconnections that are included on the system board platform are:

- Two asynchronous serial ports
- One parallel port
- One IDE controller and connector
- Floppy disk controller and connector
- Keyboard
- Mouse

In addition to the standard PC interconnections, the system board platform also provides a SCSI-2 PCI controller with standard and wide connectors, an Ethernet PCI controller with 10Base-T and AUI connectivity, a graphics PCI controller with SVGA connector, as well as business audio input/output capabilities, all on the primary motherboard.

The system board platform is designed to support Microsoft's Windows NT™ and IBM's AIX™ operating systems.

Another feature of the system board platform is that it can be available as either:

- a motherboard only,
- a motherboard integrated in a chassis, or
- a full computer system with motherboard, chassis, and peripherals.

Features

The following table describes some of the major features of the system board platform:

Table 1-1. Ultra 60x Features

Feature	Description
Microprocessor	MPC603 (@ 66MHz), or MPC603e (@100MHz), or MPC604 (@ 100MHz) RISC
Bridge/memory controller	MPC105 Eagle PowerPC-to-PCI bridge memory controller
Memory bus	64-bits + 8-bits parity, 66MHz local memory bus
Cache	Second-level cache/Processor Direct Slot (PDS)
Platform	PowerPC Reference Platform (PRP) specification enabled
DRAM	Four 72-pin SIMM sockets for 8 to 256 MB of DRAM (with or without parity)

Table 1-1. Ultra 60x Features (Continued)

Feature	Description	
I/O	Ethernet (AUI, 10base-T) interface onboard	
	SCSI-2 (Fast) interface onboard	
	Dual PC16550A asynchronous serial ports	
	IEEE 1284 8-bit bidirectional parallel port	
	Low/high-density floppy disk controller	
	IDE hard-disk drive controller	
	VGA-compatible 8-bit color graphics system and SVGA, with onboard memory expansion capability	
	Stereo 16-bit 44kHz business-class audio system	
	Audio line I/O, internal CD-ROM line inputs, headphone outputs	
	PS/2 keyboard and mouse interface	
	Power management of all onboard peripherals	
Expansion slots	PCI and ISA slot for either of two optional riser cards with PCI/ISA slots utilized as follows:	
	Six-slot card	Five slots usable: Three PCI slots and two ISA slots, or two PCI slots and three ISA slots
	Four-slot card	Three slots usable: Two PCI slots and one ISA slot, or one PCI slot and two ISA slots
Indicators and switches	Onboard status LEDs and switches	
	Provisions for external connections	
Software compatibility	Windows NT™ readiness	
	AIX™ 4.1 readiness	
	Extensive diagnostics included	

Block Diagram

The system board platform block diagram illustrates the general architecture of the system board platform. It provides a functional view of each of the major component sections, grouped by the bus they are located on: the processor bus, the PCI (local) bus, and the ISA bus.

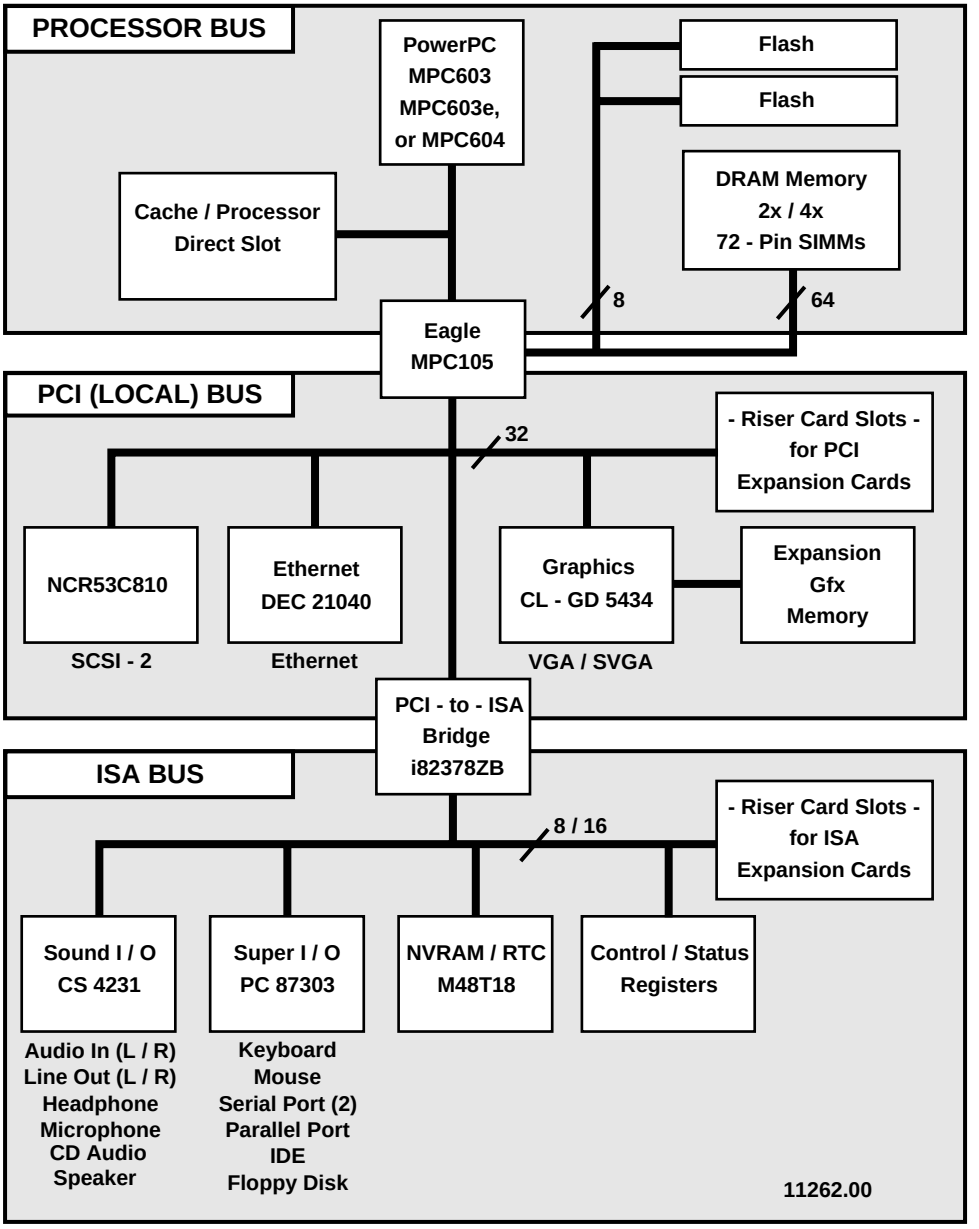

Figure 1-1. System Board Platform Block Diagram

Functional Description

For complete functional description of the major blocks on the system board platform, refer to the *Ultra 603/Ultra 603e/Ultra 604 Installation and Use Manual*.

Programming Model

The following sections describe the programming model for the system board platform.

Memory Maps

This section shows the mapping of onboard resources of the system board platform as viewed from the processor bus, the Peripheral Component (PCI) (local) bus, and the Industry Standard Architecture (ISA) bus.

Processor Memory Space

The system board platform uses the local memory map shown in the following table, by default.

Hardware or software can reconfigure this to use an alternate map.

Table 1-2. Processor View of the Memory Map

Processor Address		Size	PCI Address Generated		Definition	Notes
Start	End		Start	End		
0000 0000	7FFF FFFF	2GB			DRAM - Not forwarded to PCI Bus	
8000 0000	807F FFFF	8MB	0000 0000	007F FFFF	ISA/PCI I/O Space	1, 2, 6
8080 0000	80FF FFFF	8MB	0080 0000	00FF FFFF	PCI Configuration Space	3
8100 0000	BF7F FFFF	1GB -24MB	0100 0000	3F7F FFFF	PCI I/O Space	
BF80 0000	BFFF FFEF	8MB -16B	3F80 0000	3FFF FFEF	Reserved - Forwarded to PCI Bus	
BFFF FFF0	BFFF FFFF	16B	3FFF FFF0	3FFF FFFF	PCI IACK/Special Cycles	7
C000 0000	FEFF FFFF	1GB -16MB	0000 0000	3EFF FFFF	PCI Memory Space	
FF00 0000	FF07 FFFF	512KB			Flash Bank 0	4
FF08 0000	FF0F FFFF	512KB			Flash Bank 1	4
FF10 0000	FFEF FFFF	14MB			Reserved	4, 5
FFF0 0000	FFF7 FFFF	512KB			Flash Bank 0 Repeat	4
FFF8 0000	FFFF FFFF	512KB			Flash Bank 1 Repeat	4

Notes

1. PCI configuration accesses to CF8 (configuration address) and CFC (configuration data) are supported by the MPC105 as specified in the *Peripheral Component Interconnect PCI Local Bus Specification, Revision 2.0*.
2. Both contiguous and discontiguous mappings are supported by the system board platform. Refer to the *ISA I/O Space Mapping* section for more details.

3. This space is used for Direct Mapped PCI Configuration Space accesses. Refer to the *Direct Mapped PCI Configuration Spac*e section for more details.
4. Flash decoding repeats every 1MB for this entire 16MB range.
5. Using this address range for Flash is not recommended since future PowerPC products will redefine this 14MB area.
6. The M48T18 RTC and NVRAM device is mapped in this area. Refer to the *ISA I/O Space Mapping* section for more details.
7. A read of any byte within this 16-byte range (BFFFFFF0 through BFFFFFFF) causes a PCI IACK cycle. The data read is the IACK vector.

Direct Mapped PCI Configuration Space

This map applies to PCI configuration cycles.

Table 1-3. PCI Configuration Space Map

IDSEL	Processor Address		PCI Configuration Space Address		Definition
	Start	End	Start	End	
	8080 0000	8080 07FF	0080 0000	0080 07FF	Reserved
AD11	8080 0800	8080 08FF	0080 0800	0080 08FF	PCI/ISA Configuration Registers
	8080 0900	8080 0FFF	0080 0900	0080 0FFF	Reserved
AD12	8080 1000	8080 10FF	0080 1000	0080 10FF	NCR53C810 Configuration Registers
	8080 1100	8080 1FFF	0080 1100	0080 1FFF	Reserved
AD13	8080 2000	8080 20FF	0080 2000	0080 20FF	Unused
	8080 2100	8080 3FFF	0080 2100	0080 3FFF	Reserved
AD14	8080 4000	8080 40FF	0080 4000	0080 40FF	DEC21040 Configuration Registers
	8080 4100	8080 7FFF	0080 4100	0080 7FFF	Reserved
AD15	8080 8000	8080 80FF	0080 8000	0080 80FF	CL-GD5434 Configuration Registers
	8080 8100	8080 FFFF	0080 8100	0080 FFFF	Reserved
AD16	8081 0000	8081 00FF	0081 0000	0081 00FF	Slot #1 Registers
	8081 0100	8081 FFFF	0081 0100	0081 FFFF	Reserved
AD17	8082 0000	8082 00FF	0082 0000	0082 00FF	Slot #2 Registers
	8082 0100	8083 FFFF	0082 0100	0083 FFFF	Reserved
AD18	8084 0000	8084 00FF	0084 0000	0084 00FF	Slot #3 Registers
	8084 0100	80FF FFFF	0084 0100	00FF FFFF	Reserved

Notes

1. Accessing Reserved space may cause unpredictable results since multiple devices may be selected.

2. This memory map, map “A”, is also referred to as the “IBM” map, and is compatible with the PowerPC Reference Platform (PRP) specification. The alternate map “B”, referred to as the “Apple” map, is not supported.

ISA I/O Space Mapping

The following table details the locations of the peripherals as located on the ISA I/O address range. Whenever possible, addresses used are in compliance with PC-industry standards.

Table 1-4. ISA I/O Space Map

ISA I/O Address	Processor Address		Function	Notes
	Contiguous	Discontiguous		
0000 - 000F	8000 0000 - 8000 000F	8000 0000 - 8000 000F	PIB: DMA1 Registers and Control	2
0020 - 0021	8000 0020 - 8000 0021	8000 1000 - 8000 1001	PIB: Interrupt 1 Control and Mask	2
0040 - 0043	8000 0040 - 8000 0043	8000 2000 - 8000 2003	PIB: Timer Counter 1 Registers	2
0060	8000 0060	8000 3000	PIB: Reset Ubus IRQ12	2
0061	8000 0061	8000 3001	PIB: NMI Status and Control	2
0064	8000 0064	8000 3004	SIO: Keyboard Controller Port	3
0074	8000 0074	8000 3014	NVRAM/RTC Address STB0	
0075	8000 0075	8000 3015	NVRAM/RTC Address STB1	
0077	8000 0077	8000 3017	NVRAM/RTC Data Port	
0080 - 0090	8000 0080 - 8000 0090	8000 4000 - 8000 4010	PIB: DMA Page Registers	2
0092	8000 0092	8000 4012	PIB: Port 92 Register	2
0094 - 009F	8000 0094 - 8000 009F	8000 4014 - 8000 401F	PIB: DMA Page Registers	2
00A0 - 00A1	8000 00A0 - 8000 00A1	8000 5000 - 8000 5001	PIB: Interrupt 2 Control and Mask	2
00C0 - 00CF	8000 00C0 - 8000 00CF	8000 6000 - 8000 600F	PIB: DMA2 Address Registers	2

Table 1-4. ISA I/O Space Map (Continued)

ISA I/O Address	Processor Address		Function	Notes
	Contiguous	Discontiguous		
00D0 - 00DF	8000 00D0 - 8000 00DF	8000 7000 - 8000 700F	PIB: DMA2 Control Registers	2
01F0 - 01F7	8000 01F0 - 8000 01F7	8000 F010 - 8000 F017	SIO: IDE Registers & Control	3
02F8 - 02FF	8000 02F8 - 8000 02FF	8001 7018 - 8001 701F	SIO: Serial Port 2 (COM2)	3
0370 - 0377	8000 0370 - 8000 0377	8001 B010 - 8001 B017	SIO: Secondary FDC	3
0398	8000 0398	8001 C018	SIO: Index Register	3
0399	8000 0399	8001 C019	SIO: Data Register	3
03BC - 03BF	8000 03BC - 8000 03BF	8001 D01C - 8001 D01F	SIO: Parallel Port (LPT1)	3
03F0 - 03F7	8000 03F0 - 8000 03F7	8001 F010 - 8001 F017	SIO: Primary FDC/IDE Control	3
03F8 - 03FF	8000 03F8 - 8000 03FF	8001 F018 - 8001 F01F	SIO: Serial Port 1 (COM1)	3
040A	8000 040A	8002 000A	PIB: Scatter/Gather Interrupt Status Register	2
040B	8000 040B	8002 000B	PIB: DMA1 Extended Mode Register	2
0410 - 041F	8000 0410 - 8000 041F	8002 0010 - 8002 001F	PIB: DMA Scatter/Gather Command and Status Registers	2
0420 - 042F	8000 0420 - 8000 042F	8002 1000 - 8002 100F	PIB: DMA CH0-CH3 Scatter/Gather Descriptor Table Pointers	2

Table 1-4. ISA I/O Space Map (Continued)

ISA I/O Address	Processor Address		Function	Notes
	Contiguous	Discontiguous		
0430 - 043F	8000 0430 - 8000 043F	8002 1010 - 8002 101F	PIB: DMA CH5-CH7 Scatter/Gather Descriptor Table Pointers	2
0481 - 048B	8000 0481 - 8000 048B	8002 4000 - 8002 400B	PIB: DMA High Page Registers	2
04D0	8000 04D0	8002 6010	PIB: INT1 Edge Level Control	2
04D1	8000 04D1	8002 6011	PIB: INT2 Edge Level Control	2
04D6	8000 04D6	8002 6016	PIB: DMA2 Extended Mode Register	2
0800	8000 0800	8004 0000	CPU Type Register	
0801	8000 0801	8004 0001	Reserved	
0802	8000 0802	8004 0002	System Configuration	
0803	8000 0803	8004 0003	Reserved	
0804	8000 0804	8004 0004	DRAM Size Register 1	
0805	8000 0805	8004 0005	Reserved	
0806	8000 0806	8004 0006	Reserved	
0807	8000 0807	8004 0007	Power Control	
0830	8000 0830	8004 1010	Audio: Index Address Register	
0831	8000 0831	8004 1011	Audio: Index Data Register	

Table 1-4. ISA I/O Space Map (Continued)

ISA I/O Address	Processor Address		Function	Notes
	Contiguous	Discontiguous		
0832	8000 0832	8004 1012	Audio: Status Register	
0833	8000 0833	8004 1013	Audio: PIO Data Register	
0C01	8000 0C01	8006 0001	PIB: Test Mode Control Port/ Shadow Register of Port 70	2, 4
0C04	8000 0C04	8006 0004	PIB: Power Control Output Port	2, 4

Notes
1. All ISA I/O locations not specified in this table are user-definable.
2. These locations are internally decoded by the PIB.
3. These locations are internally decoded by the SIO.
4. These locations are undefined.

PCI Space Mapping

The system board platform uses the PCI memory map, shown in the following table, by default.

Hardware or software can reconfigure this to use an alternate map.

Table 1-5. PCI View of the PCI Memory Map

PCI Address		Size	Processor Bus Address		Definition
Start	End		Start	End	
0000 0000	00FF FFFF	16MB	Not forwarded to MPU bus		PCI/ISA Memory Space
0100 0000	7FFF FFFF	2GB -16MB	Not forwarded to MPU bus		PCI Memory Space
8000 0000	FFFF FFFF	2GB	0000 0000	7FFF FFFF (see Note)	Onboard DRAM (via MPC105)
0000 0000	FFFF FFFF	4GB	Not forwarded to MPU bus		PCI/ISA I/O Space

Note This space does not appear on the processor bus, but instead appears on the memory bus.

Interrupts

The assignments of the PCI and ISA interrupts are given in this section.

PCI Interrupts

The following table describes the interrupts dedicated to PCI peripherals. The interrupt sources are connected as shown in the table.

Table 1-6. Riser Card Interrupt Routing

PCI Slot	Riser Card Label		IDSEL	Configuration Address	PCI Board Interrupt Routing			
	6-Slot	4-Slot			PCI INT A	PCI INT B	PCI INT C	PCI INT D
1	J1	J4	AD16	0x8081_0000	PCIINT0	PCIINT1	PCIINT2	PCIINT2
2	J2	J3	AD17	0x8082_0000	PCIINT1	PCIINT2	PCIINT2	PCIINT0
3	J3	N/A	AD18	0x8084_0000	PCIINT2	PCIINT2	PCIINT0	PCIINT1

Note Although the PCI specification accommodates up to four interrupts per PCI card, it is common practice that only one interrupt (PCI INTA*) is implemented. To accommodate PCI cards that may make use of multiple interrupts, the system board platform provides support for up to three PCI interrupts per card (with software ramifications). The interrupt routing is further delineated in a figure in the *Ultra 603/Ultra 603e/Ultra 604 Installation and Use Manual*. The actual mapping of the PCI interrupts is performed in software via the PCI to ISA bridge (PIB). One possible mapping is provided in the table for *ISA Interrupt Assignments*.

ISA Interrupts

The following table describes the interrupts dedicated to ISA peripherals. The interrupt sources are connected as shown in the table.

Table 1-7. ISA Interrupt Assignments

Interrupts		Priority	Connection	Hardware Source	Type	Notes
ISA Bus	PCI Bus					
IRQ0	- - -	1	Interval Timer 1, Counter 0	PIB (Internal)	Edge, High	
IRQ1	- - -	2	Keyboard	SIO	Edge, High	
IRQ2	- - -	3-10	Cascade from slaves (IRQ8-IRQ15)	PIB (Internal)	Edge, High	
IRQ3	- - -	11	COM2, ISA Slots	SIO, Riser	Edge, High	
IRQ4	- - -	12	COM1, ISA Slots	SIO, Riser	Edge, High	
IRQ5	- - -	13	ISA Slots	Riser	Edge, High	
IRQ6	- - -	14	Floppy Disk, ISA Slots	SIO, Riser	Edge, High	
IRQ7	- - -	15	Parallel Port, ISA Slots	SIO, Riser	Edge, High	
IRQ8	- - -	3	Real-Time Clock, Abort Switch	RTC, Abort	Edge, Low	2
IRQ9	PCI INT0	4	Ethernet, PCI Slot 1 (A*), PCI Slot 2 (D*), PCI Slot 3 (C*), ISA Slots	DEC, Riser	Level, Low	2, 3
	PCI INT1		PCI Slot 1 (B*), PCI Slot 2 (A*), PCI Slot 3 (D*), ISA Slots	Riser	Level, Low	3
IRQ10	- - -	5	Audio, ISA Slots	Crystal, Riser	Edge, High	2

Table 1-7. ISA Interrupt Assignments (Continued)

Interrupts		Priority	Connection	Hardware Source	Type	Notes
ISA Bus	PCI Bus					
IRQ11	PCI INT2	6	SCSI, PCI Slot 1 (C*, D*), PCI Slot 2 (B*, C*), PCI Slot 3 (A*, B*), ISA Slots	NCR, Riser	Level, Low	2, 3
	PCI INT3		Graphics, ISA Slots	Cirrus, Riser	Level, Low	2, 3
IRQ12	- - -	7	Mouse, ISA Slots	SIO, Riser	Edge, High	
IRQ13	- - -	8	unused	- - -	Edge, High	1
IRQ14	- - -	9	IDE, ISA Slots	SIO, Riser	Edge, High	
IRQ15	- - -	10	ISA Slots	Riser	Edge, High	

Notes

1. Unused by the system board platform. Available for other uses.

2. Optional internal equipment.

3. If PCI devices are installed, this interrupt level may not be used or shared with ISA interrupts (Edge/Level sensitivity not compatible).

Note PCI interrupts may be shared with other PCI interrupts, but PCI and ISA interrupts may not be mixed. Note that the assignment of PCI interrupts to ISA interrupts is programmed in the PIB, and could be altered by firmware. More ISA interrupts could be made available by placing multiple PCI interrupts onto the same ISA interrupt.

Direct Memory Access (DMA) Channels

The following DMA channels are used by the indicated ISA peripherals. These channels may be shared with devices inserted in the ISA slots.

Table 1-8. DMA Channels

Priority (Note)	DMA Channel	Size	Peripheral
Highest	0	8 bit	-
	1	8 bit	-
	2	8 bit	Floppy Disk
	3	8 bit	Parallel Port
	4	16 bit	(not available)
	5	16 bit	IDE Interface
	6	16 bit	Audio Playback
Lowest	7	16 bit	Audio Capture

Note Default configuration in the PIB; changeable by software.

Control and Status Registers (CSRs) 2

System Board Platform Registers

The CSRs on the system board platform consists of: the CPU Type Register, the System Configuration/Status Register, the DRAM Configuration Register, the Power-Down Control Register, the NVRAM/RTC Address Registers (STB0 and STB1), and the NVRAM/RTC Data Port Register. These registers are all accessible in ISA I/O space.

Note that in the OPER row, R = read only bit, R/W = read or write bit, and W = write only bit.

CPU Type Register

This register contains the board ID code and the size of the cache memory on the system board platform.

REG	CPU Type Register - 80000800h (ISA 0800h)							
BIT	SD07	SD06	SD05	SD04	SD03	SD02	SD01	SD00
FIELD	ID						CSIZE	
OPER	R							
RESET	0100_00XXb							

ID **(Board) ID**. These four bits encode the system board platform ID code. The current ID is 4.

CSIZE **Cache Size.** These bits indicate the amount of cache memory installed on the cache board on the system board platform. The following chart provides the bit code breakdown for the cache memory size.

SD01	SD00	Cache Size
0	0	512K Cache
0	1	256K Cache
1	0	Reserved
1	1	No Cache Installed

System Configuration/Status Register

The system configuration and status register contains information on the configuration of the system board platform as created during manufacture, as well as the SCSI termination power sense status.

REG	System Configuration/Status Register - 80000802h (ISA 0802h)							
BIT	SD07	SD06	SD05	SD04	SD03	SD02	SD01	SD00
FIELD	TERM PW	IDEP-	AUDP-	BUS2X-	TEST-	GFXP-	NETP-	SCSIP-
OPER	R							
RESET	1XX1_XXXXb							

TERMPW **Termination Power**. When set, this bit indicates that the system board platform is supplying power to the SCSI terminators; that is, the termination power has not been overloaded by an external device and has not caused the polyswitch "fuse" to open. If clear, then the SCSI termination power has been disconnected due to some sort of overload condition.

Note This bit is undefined if SCSIP- is not low (i.e., a SCSI controller must be installed as well).

IDEP- **IDE Present**-. When clear, this bit indicates that the system board platform was constructed with an IDE disk controller installed. If set, then no IDE controller was installed.

AUDP- **Audio Present-**. When clear, this bit indicates that the system board platform was constructed with an audio controller installed. If set, then no audio controller was installed.

BUS2X- **Bus Speed 2X-**. When this bit is set, the system board platform was constructed with a bus speed 2X that of the clock (e.g., a 33 MHz system clock and a 66 MHz bus clock); otherwise, the system clock and the bus clock are the same frequency. This bit is used to help system software determine the type of system board platform it is running upon.

TEST- **Test-.** When this bit is clear, the firmware is expected to run diagnostics upon startup. If set, normal operation should occur. This bit should normally be set.

GFXP- **Graphics Present-**. When clear, this bit indicates that the system board platform was constructed with a graphics controller installed. If set, then no graphics controller was installed.

NETP- **Networking Present-**. When clear, this bit indicates that the system board platform was constructed with a network controller installed. If set, then no network controller was installed.

SCSIP- **SCSI Present-**. When clear, this bit indicates that the system board platform was constructed with an SCSI controller installed. If set, then no SCSI was installed.

DRAM Configuration Register

The DRAM configuration register contains status bits describing the type and speed of the SIMM modules installed on the system board platform.

REG	DRAM Configuration Register - 80000804h (ISA 0804h)							
BIT	SD07	SD06	SD05	SD04	SD03	SD02	SD01	SD00
FIELD	SIZEB		SPEEDB		SIZEA		SPEEDA	
OPER	R							
RESET	00h							

SPEEDB **Speed "B"**. These two bits encode the speed of the DRAM SIMMs installed in group "B" (the second set), and applies to the SIMM pair. By decoding these bits using the following chart, the speed of the installed SIMMs may be detected.

MSB	LSB	Speed
0	0	50 ns / 100 ns
1	0	80 ns
0	1	70 ns
1	1	60 ns

Note The system board platform does not detect 100ns SIMMs; it will assume they are 50 ns. The use of 100 ns SIMMs will most likely cause the system to fail or to work unreliably. DO NOT USE 100 ns SIMMs.

SIZEB **Size "B"**. These two bits encode the size of the DRAM SIMMs installed in group "B" (the second set), and applies to the SIMM pair. By decoding these bits using the following chart, the size of the installed SIMMs may be detected.

MSB	LSB	SIMM Size (bytes)
0	0	4MB, 64MB
1	0	32MB
0	1	16MB
1	1	8MB

Note that the size encodings are not unique for each possible part; the values do provide useful hints as to the expected size, but software is expected to resolve the remaining differences.

SPEEDA **Speed "A"**. These two bits encode the speed of the DRAM SIMMs installed in group "A" (the first set), and applies to the SIMM pair. By decoding these bits using the table as described in the **SPEEDB** section, the speed of the installed SIMMs may be detected.

SIZEA **Size "A"**. These two bits encode the size of the DRAM SIMMs installed in group "A" (the first set), and applies to the SIMM pair. By decoding these bits using the table as described in the **SIZEB** section, the size of the installed SIMMs may be detected.

Power-Down Control Register

The power-down control register contains control bits allowing the activation or power-down control of various systems on the system board platform, as well as control of the SCSI termination circuitry. Upon power-up, all devices are fully powered and are operational.

REG	Power-Down Control Register - 80000807h (ISA 0807h)							
BIT	SD07	SD06	SD05	SD04	SD03	SD02	SD01	SD00
FIELD		RSPDN	AMP DN	AUD DN	IODN			TERM-
OPER	W							
RESET	00h							

RSPDN **RS-232 Driver Power-down**. When set, this bit indicates that the RS-232 drivers for the serial ports should be powered down; if clear, the drivers are powered up. This bit controls a power converter, so a few milliseconds should elapse between activating the power and attempting to use the serial I/Os.

AMPDN **Amplifier Power-down**. When set, this bit indicates that the audio speaker amplifier (for the internal speaker) should be disabled. If clear, then audio signals sent to the amplifier will be driven to the speaker.

AUDDN **Audio Power-down**. When set, this bit indicates that the audio CODEC should be powered down. If clear, the audio CODEC will be made active.

IODN **I/O Controller Power-down**. When set, this bit indicates that the audio "Super" I/O controller should be powered down. If clear, the controller will be made active.

TERM- **Termination**. When clear, this bit indicates that the system board platform should enable the on-board SCSI terminators. If set, the internal terminators are disabled and the external SCSI termination must be used.

NVRAM/RTC Address STB0 Register

REG	NVRAM/RTC Address STB0 Register - 80000074h (ISA 0074h)							
BIT	SD07	SD06	SD05	SD04	SD03	SD02	SD01	SD00
FIELD	A7	A6	A5	A4	A3	A2	A1	A0
OPER	W							
RESET	00h							

NVRAM/RTC Address STB1 Register

REG	NVRAM/RTC Address STB1 Register - 80000075h (ISA 0075h)							
BIT	SD07	SD06	SD05	SD04	SD03	SD02	SD01	SD00
FIELD	A15	A14	A13	A12	A11	A10	A9	A8
OPER	W							
RESET	00h							

NVRAM/RTC Data Port Register

REG	NVRAM/RTC Data Port Register - 80000077h (ISA 0077h)							
BIT	SD07	SD06	SD05	SD04	SD03	SD02	SD01	SD00
FIELD								
OPER	R/W							
RESET	xxh							

The NVRAM and RTC is accessed through the above three registers. When reading from a NVRAM/RTC location, you must do the following:

1. write the low address (A0-A7) of the NVRAM to the NVRAM/RTC STB0 register,
2. write the high address (A15-A8) of the NVRAM to the NVRAM/RTC STB1 register, and
3. then read the NVRAM/RTC Data Port to fetch the NVRAM/RTC data.

When writing to a NVRAM/RTC location, you must:

1. write the low address (A0-A7) of the NVRAM to the NVRAM/RTC STB0 register,
2. write the high address (A15-A8) of the NVRAM to the NVRAM/RTC STB1 register, and
3. then write to the NVRAM/RTC Data Port for the write transfer to take place.

For the NVRAM/RTC that has only 13 address bits (A0-A12), the high address bits (A13-A15) are ignored.

Related Documentation A

Motorola Computer Group Documents

The publications listed below are on related products, and some may be referenced in this document. If not shipped with this product, manuals may be purchased by contacting your local Motorola sales office.

Table A-1. Motorola Computer Group Documents

Document Title	Publication Number
PPCBug Debugging Package User's Manual (Parts 1 and 2)	PPCBUGA1/UM PPCBUGA2/UM
PPC1Bug Diagnostics Manual	PPC1DIAA/UM
Ultra 603/Ultra 603e/Ultra 604 Installation and Hardware User's Manual	ULMB60XA/IH
Ultra 603/Ultra 603e/Ultra 604 Programmer's Reference Guide	ULMB60XA/PG

Notes Although not shown in the above list, each Motorola Computer Group manual publication number is suffixed with characters that represent the revision level of the document, such as "/*xx*2" (the second revision of a manual); a supplement bears the same number as the manual but has a suffix such as "/*xx*2A1" (the first supplement to the second revision of the manual).

The above documents can be purchased as a set, packaged under part number **LK-UB60X**.

Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is also provided. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

To further assist your development effort, Motorola has collected some of the non-Motorola documents in this list from the suppliers. This bundle can be ordered as part number **68-PCIKIT**.

Table A-2. Manufacturers' Documents

Document Title and Source	Publication Number
PowerPC 603™ RISC Microprocessor Technical Summary Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430	MPC603/D
PowerPC 603™ RISC Microprocessor User's Manual Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430 OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPC603UM/AD MPR603UMU-01

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
PowerPC 604™ RISC Microprocessor User's Manual Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430 OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPC604UM/AD MPR604UMU-01
MPC105 PCI Bridge/Memory Controller User's Manual Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430	MPC105UM/AD
PowerPC™ Microprocessor Family: The Programming Environments Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430 OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPCFPE/AD MPRPPCFPE-01

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
Alpine™ VGA Family - CL-GD543X Technical Reference Manual Third Edition Cirrus Logic, Inc. (or nearest Sales Office) 3100 West Warren Avenue Fremont, California 94538-6423 Telephone: (510) 623-8300 FAX: (510) 226-2180	GD543X-TRM-003 (part number 385439-003)
DECchip 21040 Ethernet LAN Controller for PCI Hardware Reference Manual Digital Equipment Corporation Maynard, Massachusetts DECchip Information Line Telephone (United States and Canada): 1-800-332-2717 TTY (United States only): 1-800-332-2515 Telephone (outside North America): +1-508-568-6868	EC-N0752-72
PC87303VUL (Super I/O™ Sidewinder Lite) Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, IEEE 1284 Parallel Port, and IDE Interface National Semiconductor Corporation Customer Support Center (or nearest Sales Office) 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, California 95052-8090 Telephone: 1-800-272-9959	PC87303VUL
PC87323VF (Super I/O™ Sidewinder) Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, IEEE 1284 Parallel Port, and IDE Interface National Semiconductor Corporation Customer Support Center (or nearest Sales Office) 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, California 95052-8090 Telephone: 1-800-272-9959	PC87323VF

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
M48T18 CMOS 8K x 8 TIMEKEEPER™ SRAM Data Sheet SGS-Thomson Microelectronics Group Marketing Headquarters (or nearest Sales Office) 1000 East Bell Road Phoenix, Arizona 85022 Telephone: (602) 867-6100	M48T18
DS1643 Nonvolatile Timekeeping RAM Data Manual Dallas Semiconductor 4401 South Beltwood Parkway Dallas, Texas 75244-3292	DS1643/ DS1643LPM
82378 System I/O (SIO) PCI-to-ISA Bridge Controller Intel Corporation Literature Sales P.O. Box 7641 Mt. Prospect, Illinois 60056-7641 Telephone: 1-800-548-4725	290473-003
NCR53C810 PCI-SCSI I/O Processor Data Manual NCR Corporation Microelectronics Products Division 1635 Aeroplaza Drive Colorado Springs, Colorado 80916 Telephone: (719) 596-5795 NCR Hotline: 1-800-334-5454 FAX: (719) 527-8225	T46923I
NCR 53C8XX Family PCI-SCSI I/O Processors Programming Guide NCR Corporation Microelectronics Products Division 1635 Aeroplaza Drive Colorado Springs, Colorado 80916 Telephone: (719) 596-5795 NCR Hotline: 1-800-334-5454 FAX: (719) 527-8225	J10931I

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
SCC (Serial Communications Controller) User's Manual (for Z85230 and other Zilog parts) Zilog, Inc. 210 East Hacienda Ave., mail stop C1-0 Campbell, California 95008-6600 Telephone: (408) 370-8016 FAX: (408) 370-8056	DC-8293-02
Z8536 CIO Counter/Timer and Parallel I/O Unit Product Specification and User's Manual (in Z8000® Family of Products Data Book) Zilog, Inc. 210 East Hacienda Ave., mail stop C1-0 Campbell, California 95008-6600 Telephone: (408) 370-8016 FAX: (408) 370-8056	DC-8319-00
CS4231 Parallel Interface, Multimedia Audio Codec Data Sheet Crystal Semiconductor Corporation 4210 South Industrial Drive P.O. Box 17847 Austin, Texas 78744-7847 Telephone: 1-800-888-5016 Telephone: (512) 445-7222 FAX: (512) 445-7581	DS111PP4
CSB4231/4248 Evaluation Board Data Sheet Crystal Semiconductor Corporation 4210 South Industrial Drive P.O. Box 17847 Austin, Texas 78744-7847 Telephone: 1-800-888-5016 Telephone: (512) 445-7222 FAX: (512) 445-7581	DS111DB4

Related Specifications

For additional information, refer to the following table for related specifications. Sources for the listed documents are also provided. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table A-3. Related Specifications

Document Title and Source	Publication Number
ANSI Small Computer System Interface-2 (SCSI-2) Global Engineering Documents 15 Inverness Way East Englewood, CO 80112-5704 Telephone: 1-800-854-7179 Telephone: (303) 792-2181	X3.131.1990
ANSI Std X3T9.2, 1994 AT Attachment Interface for Disk Drives Global Engineering Documents 15 Inverness Way East Englewood, CO 80112-5704 Telephone: 1-800-854-7179 Telephone: (303) 792-2181	ANSI X3.221
Bidirectional Parallel Port Interface Specification Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE Standard 1284
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386 Draft 1.3

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386.1 Draft 1.3
IEEE Standard for Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE 802.3
Information Technology - Local and Metropolitan Networks - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications International Organization for Standardization (ISO) *(This document can also be obtained through the national standards body of member countries.)*	ISO/IEC 8802-3
Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange (EIA-232-D) Electronic Industries Association Engineering Department 2001 Eye Street, N.W. Washington, D.C. 20006	ANSI/EIA-232-D Standard
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.0 PCI Special Interest Group P.O. Box 14070 Portland, Oregon 97214-4070 Marketing/Help Line Telephone: (503) 696-6111 Document/Specification Ordering Telephone: 1-800-433-5177 Telephone: (503) 797-4207 FAX: (503) 234-6762	PCI Local Bus Specification

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
PowerPC Reference Platform Specification, Third Edition, Version 1.0, Volumes I and II International Business Machines Corporation Power Personal Systems Architecture 11400 Burnet Road Austin, Texas 78758-3493 Document/Specification Ordering Telephone: 1-800-POWERPC Telephone: 1-800-769-3772 Telephone: (708) 296-9332	MPR-PPC-RPU-02

Glossary

Abbreviations, Acronyms, and Terms to Know

This glossary defines some of the abbreviations, acronyms, and key terms used in this document.

10base-5 See thick Ethernet.

10base-2 See thin Ethernet.

10base-T See twisted-pair Ethernet.

ACIA **A**synchronous **C**ommunications **I**nterface **A**dapter

AIX **A**dvanced **I**nteractive e**X**ecutive (IBM version of UNIX)

architecture The main overall design in which each individual hardware component of the computer system is interrelated. The most common uses of this term are 8-bit, 16-bit, or 32-bit architectural design systems.

ASCII **A**merican **S**tandard **C**ode for **I**nformation **I**nterchange. This is a 7-bit code used to encode alphanumeric information. In the IBM-compatible world, this is expanded to 8-bits to encode a total of 256 alphanumeric and control characters.

ASIC **A**pplication-**S**pecific **I**ntegrated **C**ircuit

AUI **A**ttachment **U**nit **I**nterface

BBRAM **B**attery **B**acked-up **R**andom **A**ccess **M**emory

bi-endian Having big-endian and little-endian byte ordering capability.

big-endian A byte-ordering method in memory where the address *n* of a word corresponds to the most significant byte. In an addressed memory word, the bytes are ordered (left to right) 0, 1, 2, 3, with 0 being the most significant byte.

BIOS **B**asic **I**nput/**O**utput **S**ystem. This is the built-in program that controls the basic functions of communications between the processor and the I/O (peripherals) devices. Also referred to as ROM BIOS.

BitBLT **Bit** Boundary **BL**ock **T**ransfer. A type of graphics drawing routine that moves a rectangle of data from one area of display memory to another. The data specifically need not have any particular alignment.

BLT **BL**ock **T**ransfer

board The term more commonly used to refer to a PCB (printed circuit board). Basically, a flat board made of nonconducting material, such as plastic or fiberglass, on which chips and other electronic components are mounted. Also referred to as a circuit board or card.

bpi **b**its **p**er **i**nch

bps **b**its **p**er **s**econd

bus The pathway used to communicate between the CPU, memory, and various input/output devices, including floppy and hard disk drives. Available in various widths (8-, 16-, and 32-bit), with accompanying increases in speed.

cache A high-speed memory that resides logically between a central processing unit (CPU) and the main memory. This temporary memory holds the data and/or instructions that the CPU is most likely to use over and over again and avoids accessing the slower hard or floppy disk drive.

CAS **C**olumn **A**ddress **S**trobe. The clock signal used in dynamic RAMs to control the input of column addresses.

CD **C**ompact **D**isc. A hard, round, flat portable storage unit that stores information digitally.

CD-ROM **C**ompact **D**isk **R**ead-**O**nly **M**emory

CFM **C**ubic **F**eet per **M**inute

CISC **C**omplex-**I**nstruction-**S**et **C**omputer. A computer whose processor is designed to sequentially run variable-length instructions, many of which require several clock cycles, that perform complex tasks and thereby simplify programming.

CODEC **CO**der/**DEC**oder

Color Difference (CD) The signals of (R-Y) and (B-Y) without the luminance (-Y) signal. The Green signals (G-Y) can be extracted by these two signals.

Composite Video Signal (CVS/CVBS) Signal that carries video picture information for color, brightness and synchronizing signals for both horizontal and vertical scans. Sometimes referred to as "Baseband Video".

cpi **c**haracters **p**er **i**nch

cpl **c**haracters **p**er **l**ine

CPU **C**entral **P**rocessing **U**nit. The master computer unit in a system.

DCE **D**ata **C**ircuit-terminating **E**quipment.

DLL **D**ynamic **L**ink **L**ibrary. A set of functions that are linked to the referencing program at the time it is loaded into memory.

DMA **D**irect **M**emory **A**ccess. A method by which a device may read or write to memory directly without processor intervention. DMA is typically used by block I/O devices.

DOS **D**isk **O**perating **S**ystem

dpi **d**ots **p**er **i**nch

DRAM **D**ynamic **R**andom **A**ccess **M**emory. A memory technology that is characterized by extreme high density, low power, and low cost. It must be more or less continuously refreshed to avoid loss of data.

DTE **D**ata **T**erminal **E**quipment.

ECC **E**rror **C**orrection **C**ode

ECP **E**xtended **C**apability **P**ort

EEPROM — **E**lectrically **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory. A memory storage device that can be written repeatedly with no special erasure fixture. EEPROMs do not lose their contents when they are powered down.

EISA (bus) — **E**xtended **I**ndustry **S**tandard **A**rchitecture (bus) (IBM). An architectural system using a 32-bit bus that allows data to be transferred between peripherals in 32-bit chunks instead of 16-bit or 8-bit that most systems use. With the transfer of larger bits of information, the machine is able to perform much faster than the standard ISA bus system.

EPP — **E**nhanced **P**arallel **P**ort

EPROM — **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory. A memory storage device that can be written once (per erasure cycle) and read many times.

ESCC — **E**nhanced **S**erial **C**ommunication **C**ontroller

ESD — **E**lectro-**S**tatic **D**ischarge/Damage

Ethernet — A local area network standard that uses radio frequency signals carried by coaxial cables.

FDC — **F**loppy **D**isk **C**ontroller

FDDI — **F**iber **D**istributed **D**ata **I**nterface. A network based on the use of optical-fiber cable to transmit data in non-return-to-zero, invert-on-1s (NRZI) format at speeds up to 100 Mbps.

FIFO — **F**irst-**I**n, **F**irst-**O**ut. A memory that can temporarily hold data so that the sending device can send data faster than the receiving device can accept it. The sending and receiving devices typically operate asynchronously.

firmware — The program or specific software instructions that have been more or less permanently burned into an electronic component, such as a ROM (read-only memory) or an EPROM (erasable programmable read-only memory).

frame — One complete television picture frame consists of 525 horizontal lines with the NTSC system. One frame consists of two Fields.

graphics controller On EGA and VGA, a section of circuitry that can provide hardware assist for graphics drawing algorithms by performing logical functions on data written to display memory.

HAL **H**ardware **A**bstraction **L**ayer. The lower level hardware interface module of the Windows NT operating system. It contains platform specific functionality.

hardware A computing system is normally spoken of as having two major components: hardware and software. Hardware is the term used to describe any of the physical embodiments of a computer system, with emphasis on the electronic circuits (the computer) and electromechanical devices (peripherals) that make up the system.

HCT **H**ardware **C**onformance **T**est. A test used to ensure that both hardware and software conform to the Windows NT interface.

I/O **I**nput/**O**utput

IBC PCI/**I**SA **B**ridge **C**ontroller

IDE **I**ntelligent **D**evice **E**xpansion

IEEE **I**nstitute of **E**lectrical and **E**lectronics **E**ngineers

interlaced A graphics system in which the even scanlines are refreshed in one vertical cycle (field), and the odd scanlines are refreshed in another vertical cycle. The advantage is that the video bandwidth is roughly half that required for a non-interlaced system of the same resolution. This results in less costly hardware. It also may make it possible to display a resolution that would otherwise be impossible on given hardware. The disadvantage of an interlaced system is flicker, especially when displaying objects that are only a few scanlines high.

IQ Signals Similar to the color difference signals (R-Y), (B-Y) but using different vector axis for encoding or decoding. Used by some USA TV and IC manufacturers for color decoding.

ISA (bus)	**I**ndustry **S**tandard **A**rchitecture (bus). The de facto standard system bus for IBM-compatible computers until the introduction of VESA and PCI. Used in the reference platform specification. (IBM)
ISASIO	**ISA S**uper **I**nput/**O**utput device
ISDN	**I**ntegrated **S**ervices **D**igital **N**etwork. A standard for digitally transmitting video, audio, and electronic data over public phone networks.
LAN	**L**ocal **A**rea **N**etwork
LED	**L**ight-**E**mitting **D**iode
LFM	**L**inear **F**eet per **M**inute
little-endian	A byte-ordering method in memory where the address *n* of a word corresponds to the least significant byte. In an addressed memory word, the bytes are ordered (left to right) 3, 2, 1, 0, with 3 being the most significant byte.
MBLT	**M**ultiplexed **BL**ock **T**ransfer
MCA (bus)	**M**icro **C**hannel **A**rchitecture
MCG	**M**otorola **C**omputer **G**roup
MFM	**M**odified **F**requency **M**odulation
MIDI	**M**usical **I**nstrument **D**igital **I**nterface. The standard format for recording, storing, and playing digital music.
MPC	**M**ultimedia **P**ersonal **C**omputer
MPC105	The PowerPC-to-PCI bus bridge chip developed by Motorola for the Ultra 603/Ultra 604 system board. It provides the necessary interface between the MPC603/MPC604 processor and the Boot ROM (secondary cache), the DRAM (system memory array), and the PCI bus.
MPC601	Motorola's component designation for the PowerPC 601 microprocessor.
MPC603	Motorola's component designation for the PowerPC 603 microprocessor.
MPC603e	Motorola's component designation for the PowerPC 603e microprocessor.

MPC604 Motorola's component designation for the PowerPC 604 microprocessor.

MPU **M**icro**P**rocessing **U**nit

MTBF **M**ean **T**ime **B**etween **F**ailures. A statistical term relating to reliability as expressed in power on hours (poh). It was originally developed for the military and can be calculated several different ways, yielding substantially different results. The specification is based on a large number of samplings in one place, running continuously, and the rate at which failure occurs. MTBF is not representative of how long a device, or any individual device is likely to last, nor is it a warranty, but rather, of the relative reliability of a family of products.

multisession The ability to record additional information, such as digitized photographs, on a CD-ROM after a prior recording session has ended.

non-interlaced A video system in which every pixel is refreshed during every vertical scan. A non-interlaced system is normally more expensive than an interlaced system of the same resolution, and is usually said to have a more pleasing appearance.

nonvolatile memory A memory in which the data content is maintained whether the power supply is connected or not.

NTSC **N**ational **T**elevision **S**tandards **C**ommittee (USA)

NVRAM **N**on-**V**olatile **R**andom **A**ccess **M**emory

OEM **O**riginal **E**quipment **M**anufacturer

OMPAC **O**ver - **M**olded **P**ad **A**rray **C**arrier

OS **O**perating **S**ystem. The software that manages the computer resources, accesses files, and dispatches programs.

OTP **O**ne-**T**ime **P**rogrammable

palette The range of colors available on the screen, not necessarily simultaneously. For VGA, this is either 16 or 256 simultaneous colors out of 262,144.

parallel port A connector that can exchange data with an I/O device eight bits at a time. This port is more commonly used for the connection of a printer to a system.

PCI (local bus) **P**eripheral **C**omponent **I**nterconnect (local bus) (Intel). A high-performance, 32-bit internal interconnect bus used for data transfer to peripheral controller components, such as those for audio, video, and graphics.

PCMCIA (bus) **P**ersonal **C**omputer **M**emory **C**ard **I**nternational **A**ssociation (bus). A standard external interconnect bus which allows peripherals adhering to the standard to be plugged in and used without further system modification.

PDS **P**rocessor **D**irect **S**lot

physical address A binary address that refers to the actual location of information stored in secondary storage.

PIB **P**CI-to-**I**SA **B**ridge

pixel An acronym for picture element, and is also called a pel. A pixel is the smallest addressable graphic on a display screen. In RGB systems, the color of a pixel is defined by some Red intensity, some Green intensity, and some Blue intensity.

PLL **P**hase-**L**ocked **L**oop

PMC **P**CI **M**ezzanine **C**ard

POWER **P**erformance **O**ptimized **W**ith **E**nhanced **R**ISC architecture (IBM)

PowerPC™ The trademark used to describe the **P**erformance **O**ptimized **W**ith **E**nhanced **R**ISC microprocessor architecture for **P**ersonal **C**omputers developed by the IBM Corporation. PowerPC is superscalar, which means it can handle more than one instruction per clock cycle. Instructions can be sent simultaneously to three types of independent execution units (branch units, fixed-point units, and floating-point units), where they can execute concurrently, but finish out of order. PowerPC is used by Motorola, Inc. under license from IBM.

PowerPC 601™ The first implementation of the PowerPC family of microprocessors. This CPU incorporates a memory

management unit with a 256-entry buffer and a 32KB unified (instruction and data) cache. It provides a 64-bit data bus and a separate 32-bit address bus. PowerPC 601 is used by Motorola, Inc. under license from IBM.

PowerPC 603™ The second implementation of the PowerPC family of microprocessors. This CPU incorporates a memory management unit with a 64-entry buffer and 8KB instruction and data caches. It provides a selectable 32-bit or 64-bit data bus and a separate 32-bit address bus. PowerPC 603 is used by Motorola, Inc. under license from IBM.

PowerPC 603e™ A high-performance extension of the PowerPC 603. Contains 16KB instruction and data caches. PowerPC 603e is used by Motorola, Inc. under license from IBM.

PowerPC 604™ The third implementation of the PowerPC family of microprocessors. This CPU incorporates a memory management unit with a 128-entry buffer and 16KB instruction and data caches. It provides a 64-bit data bus and a separate 32-bit address bus. PowerPC 604 is used by Motorola, Inc. under license from IBM.

PowerPC Reference Platform (PRP)
A specification published by the IBM Power Personal Systems Division which defines the devices, interfaces, and data formats that make up a PRP-compliant system using a PowerPC processor.

PowerStack™ RISC PC (System Board)
A PowerPC-based computer board platform developed by the Motorola Computer Group. It supports Microsoft's Windows NT and IBM's AIX operating systems.

PRP See PowerPC Reference Platform (PRP).

PRP-compliant See PowerPC Reference Platform (PRP).

PRP Spec See PowerPC Reference Platform (PRP).

PROM **P**rogrammable **R**ead-**O**nly **M**emory

PS/2 **P**ersonal **S**ystem/**2** (IBM)

QFP **Q**uad **F**lat **P**ackage

RAM **R**andom-**A**ccess **M**emory. The temporary memory that a computer uses to hold the instructions and data currently being worked with. All data in RAM is lost when the computer is turned off.

RAS **R**ow **A**ddress **S**trobe. A clock signal used in dynamic RAMs to control the input of the row addresses.

Reduced-Instruction-Set Computer (RISC) A computer in which the processor's instruction set is limited to constant-length instructions that can usually be executed in a single clock cycle.

RFI **R**adio **F**requency **I**nterference

RGB The three separate color signals: **R**ed, **G**reen, and **B**lue. Used with color displays, an interface that uses these three color signals as opposed to an interface used with a monochrome display that requires only a single signal. Both digital and analog RGB interfaces exist.

RISC See Reduced Instruction Set Computer (RISC).

ROM **R**ead-**O**nly **M**emory

RTC **R**eal-**T**ime **C**lock

SBC **S**ingle **B**oard **C**omputer

SCSI **S**mall **C**omputer **S**ystems **I**nterface. An industry-standard high-speed interface primarily used for secondary storage. SCSI-1 provides up to 5 Mbps data transfer.

SCSI-2 (Fast/Wide) An improvement over plain SCSI; and includes command queuing. Fast SCSI provides 10 Mbps data transfer on an 8-bit bus. Wide SCSI provides up to 40 Mbps data transfer on a 16- or 32-bit bus.

serial port A connector that can exchange data with an I/O device one bit at a time. It may operate synchronously or asynchronously, and may include start bits, stop bits, and/or parity.

SIM **S**erial **I**nterface **M**odule

SIMM — **S**ingle **I**nline **M**emory **M**odule. A small circuit board with RAM chips (normally surface mounted) on it designed to fit into a standard slot.

SIO — **S**uper **I/O** controller

SMP — **S**ymmetric **M**ulti**P**rocessing. A computer architecture in which tasks are distributed among two or more local processors.

SMT — **S**urface **M**ount **T**echnology. A method of mounting devices (such as integrated circuits, resistors, capacitors, and others) on a printed circuit board, characterized by not requiring mounting holes. Rather, the devices are soldered to pads on the printed circuit board. Surface-mount devices are typically smaller than the equivalent through-hole devices.

software — A computing system is normally spoken of as having two major components: hardware and software. Software is the term used to describe any single program or group of programs, languages, operating procedures, and documentation of a computer system. Software is the real interface between the user and the computer.

SRAM — **S**tatic **R**andom **A**ccess **M**emory

SSBLT — **S**ource **S**ynchronous **BL**ock **T**ransfer

standard(s) — A set of detailed technical guidelines used as a means of establishing uniformity in an area of hardware or software development.

SVGA — **S**uper **V**ideo **G**raphics **A**rray (IBM). An improved VGA monitor standard that provides at least 256 simultaneous colors and a screen resolution of 800 x 600 pixels.

Teletext — One way broadcast of digital information. The digital information is injected in the broadcast TV signal, VBI, or full field, The transmission medium could be satellite, microwave, cable, etc. The display medium is a regular TV receiver.

thick Ethernet (10base-5)
An Ethernet in which the physical medium is a doubly shielded, 50-ohm coaxial cable capable of carrying data at 10 Mbps for a length of 500 meters (also referred to as thicknet).

thin Ethernet (10base-2)
An Ethernet in which the physical medium is a single-shielded, 50-ohm RG58A/U coaxial cable capable of carrying data at 10 Mbps for a length of 185 meters (also referred to as AUI or thinnet).

twisted-pair Ethernet (10base-T)
An Ethernet in which the physical medium is an unshielded pair of entwined wires capable of carrying data at 10 Mbps for a maximum distance of 185 meters.

UART **U**niversal **A**synchronous **R**eceiver/**T**ransmitter

UV **U**ltra**V**iolet

UVGA **U**ltra **V**ideo **G**raphics **A**rray. An improved VGA monitor standard that provides at least 256 simultaneous colors and a screen resolution of 1024 x 768 pixels.

VAFC **V**ESA **A**dvanced **F**eature **C**onnector.

Vertical Blanking Interval (VBI)
The time it takes the beam to fly back to the top of the screen in order to retrace the opposite field (odd or even). VBI is in the order of 20 TV lines. Teletext information is transmitted over 4 of these lines (lines 14-17).

VESA (bus) **V**ideo **E**lectronics **S**tandards **A**ssociation (or VL bus). An internal interconnect standard for transferring video information to a computer display system.

VGA **V**ideo **G**raphics **A**rray (IBM). The third and most common monitor standard used today. It provides up to 256 simultaneous colors and a screen resolution of 640 x 480 pixels.

virtual address A binary address issued by a CPU that indirectly refers to the location of information in primary memory, such as main memory. When data is copied from disk to main memory, the physical address is changed to the virtual address.

VL bus See **V**ESA **L**ocal bus (VL bus).

VMEchip2 MCG second generation VMEbus interface ASIC (Motorola)

VME2PCI MCG ASIC that interfaces between the PCI bus and the VMEchip2 device.

volatile memory A memory in which the data content is lost when the power supply is disconnected.

VRAM **V**ideo (Dynamic) **R**andom **A**ccess **M**emory. Memory chips with two ports, one used for random accesses and the other capable of serial accesses. Once the serial port has been initialized (with a transfer cycle), it can operate independently of the random port. This frees the random port for CPU accesses. The result of adding the serial port is a significantly reduced amount of interference from screen refresh. VRAMs cost more per bit than DRAMs.

Windows NT™ The trademark representing **Windows N**ew **T**echnology, a computer operating system developed by the Microsoft Corporation.

XGA E**X**tended **G**raphics **A**rray. An improved IBM VGA monitor standard that provides at least 256 simultaneous colors and a screen resolution of 1024 x 768 pixels.

Y Signal Luminance. This determines the brightness of each spot (pixel) on a CRT screen either color or B/W systems, but not the color.

Index

INDEX