V162PFXA/LT2
May 2000

Dear Valued Customer:

Thank you for your purchase of a Motorola MVME162P-series Embedded Controller. These products, which incorporate the new “Petra” ASIC, provide owners of existing MVME162 boards a means of migrating to updated boards while preserving their investments in associated software and equipment. The information in this letter applies to those MVME162 products built to support 4 IP (IndustryPack) modules.

Background

Due to evolution in technology, the production of certain ASICs used on first- and second-generation MVME162/172 series boards has ended. The discontinued ASICs are the MC, MC2, IPIC, IP2, and MCECC chips. The Petra chip was developed to replace these discontinued ASICs.

The Petra ASIC is functionally compatible with each of the components that it replaces. In cases where functionality between the previous ASICs is exclusive, configuration switches or jumpers are provided to let you select the desired functionality. For instance, the MC and MC2 chips differed in their implementation of Flash write protection. Boards built with the Petra ASIC, accordingly, have a configuration switch so that you can determine which method to use.

Motorola is committed to providing long-term support for the widely used 68K product family. In order to continue offering this family of products and to maintain the current programming model, large quantities of end-of-life parts have been procured and the boards have been redesigned to use newer component technologies where necessary. While these new products are designed for compatibility with previous 68K family products, some differences do exist.

New Models

The new MVME162 board will be offered in the versions listed in the table below. Existing applications should be mapped to one of these versions. If that is not possible, please contact your local Motorola sales office for assistance.

Note that all versions of the board are built with 16 MB of SDRAM, which can be reconfigured as needed to model 1-, 4-, 8-, or 16MB memory for your applications.

New Model No.	Characteristics	Replaces. . .
MVME162P-244L	25MHz 68LC040, 16MB SDRAM, 2 SIO, 4 DMA IP	MVME162-410
MVME162P-244LE	25MHz 68LC040, 16MB SDRAM, 2 SIO, 4 DMA IP, E-net	MVME162-432, -412
MVME162P-244LSE	25MHz 68LC040, 16MB SDRAM, 2 SIO, 4 DMA IP, SCSI/E-net	MVME162-433, -413
MVME162P-344	32MHz 68040, 16MB SDRAM, 2 SIO, 4 DMA IP	MVME162-520A, -510A, -510B, -510C
MVME162P-344S	32MHz 68040, 16MB SDRAM, 2 SIO, 4 DMA IP, SCSI	MVME162-511A, -511B, -511C
MVME162P-344E	32MHz 68040, 16MB SDRAM, 2 SIO, 4 DMA IP, E-net	MVME162-532A, -522A, -512A, -512B, -512C
MVME162P-344SE	32MHz 68040, 16MB SDRAM, 2 SIO, 4 DMA IP, SCSI/E-net	MVME162-533A, -523A, -513A

Differences

Although every attempt has been made to preserve compatibility with earlier models of the MVME162 series, there are some differences that should be noted. The major differences between the previous and the new versions of the MVME162 are:

1. The functions formerly implemented in the IP2 and MC2 ASICs are now combined in a single new ASIC called Petra.
2. The memory mezzanines have been replaced by 16MB of on-board SDRAM.
3. Memory performance is improved.
4. Single-bit error correction and double-bit error detection have replaced memory parity protection.
5. Larger SDRAM and Flash memory configurations can be supplied on request.
6. The front panel dual-LED assemblies have been replaced by surface-mount LEDs and light pipes (*on evaluation boards only; production models will preserve the existing LED configuration*).
7. The dual-cell battery has been replaced by a coin-cell battery.
8. The power consumption has been reduced.

LEDs and Battery

MVME162 boards are now manufactured with a double-sided surface-mount process. Because the front panel LEDs and the SRAM battery used on previous products are not compatible with this process, the battery has changed from a dual-cell battery that plugged into the board to a single coin cell that installs in a surface mount holder. The dual-module LEDs were changed to

LEDs that are surface-mounted on the board with light pipes routed to the front panel. In applications where the standard front panel is removed or replaced, modifications may be necessary to support the new LED configuration.

(*As noted above, this change applies only to evaluation boards; production models will preserve the existing LED configuration.*)

Power Consumption

In the course of the redesign, many board components were integrated or updated to more current technologies. This has reduced component count and lowered the power consumption of the MVME162 boards.

SRAM Backup

The new MVM162 products allow the SRAM to receive backup power from the VMEbus standby power (+5STDBY) pin. Previous boards used a resistor and zener diode to reduce the +5 volts from the VMEbus to the +3 volts required for backup. A drawback was that the zener diode produced a rather high current drain from the +5STDBY pin. The new boards use an active component to reduce the voltage; the current drain from the +5STDBY pin is consequently much lower.

Memory Control

The functions formerly implemented in the MC2 ASIC are now incorporated into the functions of the Petra ASIC. The revision code has been changed to $02. While the programming model and functionality have not changed, the physical implementation of the memory subsystem has changed. Memory mezzanine boards are no longer used; the memory devices have changed from page mode DRAMs to SDRAMs. This modification has improved the performance of the memory subsystem.

The minimum factory memory configuration is 16MB. Configuration switches on the board permit the memory size to be tailored to appear as 1MB, 4MB, or 8MB for applications that require the smaller memory configurations. Regardless of how the board is ordered, the memory size can always be reconfigured in the field.

The new MVME162 boards use single-bit error correction and double-bit error detection (ECC) to replace the memory parity protection used on the earlier boards. When parity is enabled in the memory controller, the ECC function is used to provide memory protection. If a single-bit error occurs, the error is automatically corrected. If a double-bit error occurs, then a parity error is generated.

The Petra ASIC also supports the flash write protection modes of the MC chip and the MC2 chip. A switch on the board regulates this function (refer to the summary table below for additional information).

The MC2 interface to the Z85230 Serial Communications Controller did not support direct access to the data port. The Petra ASIC supports both direct and indirect modes of access.

The Petra ASIC also incorporates the functionality of the MCECC memory controller ASIC. This capability enables the MVME162 to support 32MB or 64MB of SDRAM memory and 2MB of Flash memory. If your application can benefit from these increased memory sizes, please contact your local Motorola sales office for assistance.

IP Interface

The functions formerly implemented in the IP2 ASIC are now incorporated into the functions of the Petra ASIC. The revision code has been changed to $02. Several improvements have been made to the IP interface logic.

The Petra ASIC supports the IP reset modes of both the IP chip and the IP2 chip. A switch on the board regulates this function (refer to the summary table below for additional information).

The IP2 ASIC had no mechanism to flush the IP DMA FIFO buffers. The Petra ASIC includes a new control bit that will cause the data in the FIFO buffers to be automatically transferred to memory if the DMA terminates before the byte count reaches zero.

In the IP2 ASIC, DMA chaining did not work at 32MHz. This flaw has been corrected in the Petra ASIC.

The IP DMA controller in the Petra ASIC has a bug that did not occur in the IP2 ASIC: setting the DHALT bit for DMA channel A will cause all DMA channels to halt. This problem and a workaround for it are described in the *MVME1x2PFX Embedded Controller Programmer's Reference Guide*.

The differences between the original MVME162 boards with the MC and IP ASICs, the current MVME162 boards with the MC2 and IP2 ASICs and new MVME162 boards with the Petra ASIC are summarized in the following table. For additional information on the new MVME162 products, please refer to the programming guide (V1x2PFXA/PG) and the installation/use manual (V162PFXA/IH).

Once again, thank you for purchasing Motorola products. If you have any questions or comments, please contact your local Motorola sales representative.

This customer letter is also posted at Motorola's World Wide Web site under www.motorola.com/computer/literature.

Table 1. List of Changes

Function	Implementation		
	Previous [MVME162, MC, IP]	**Current [MVME162FX, MC2, IP2]**	**New [MVME162, Petra ASIC]**
User configuration	Jumper headers.	Jumper headers.	Jumper headers, hardware/ software switches.
LEDs	Dual LED modules.	Dual LED modules.	Surface mount LEDs with light pipes (*on evaluation boards only*).
SRAM battery	Through-hole, dual battery (100 mah).	Through-hole, dual battery (100 mah).	Surface mount holder for coin cell (220 mah).
DRAM	1-, 4-, 8-, 16MB fast page DRAM.	4-, 8-, 16MB fast page DRAM.	16MB SDRAM, configurable to 1-, 4-, 8-, 16MB.
Memory control	MC ASIC, revision 00	MC2 ASIC, revision 01	Petra ASIC, revision 02
Flash memory write enable	Flash writes enabled/ disabled via memory map.	Flash writes enabled/disabled via control bit in register.	Map or control-bit enable/ disable of Flash writes selectable via board configuration switch.
Serial I/O	MC ASIC supported both direct and indirect access to 85230 data port.	MC2 ASIC did not support direct access to data port. Software used indirect access.	Petra ASIC supports both direct and indirect access modes.
Memory protection	Parity protection for MC memory.	No parity protection for MC2 memory due to availability of DRAM devices.	MC2 memory model has ECC protection if parity is enabled.
IP interface control	IP ASIC, revision 00	IP2 ASIC, revision 00	Petra ASIC, revision 02.
IP reset	IP Reset Control bit in local bus memory map at location $FFFBC01F. Local bus resets, power-up resets, and software writes to this location all produce an IP reset. The IP Reset bit is cleared automatically.	IP Reset Control bit in local bus memory map at location $FFFBC01F. No local bus resets; only power-up resets and software writes to this location produce an IP reset. Software must clear the IP Reset bit.	IP Reset bit is under control of software configuration switch. Both IP and IP2 reset modes available.

Table 1. List of Changes (Continued)

Function	Implementation		
	Previous [MVME162, MC, IP]	**Current [MVME162FX, MC2, IP2]**	**New [MVME162, Petra ASIC]**
IP DMA flush	No DMA: no flush mechanism.	DMA bug in IP2 ASIC: no flush mechanism.	New control register bit supplies flush mechanism. IP DMA FIFOs will flush if a DMA data stream ends before the byte count reaches zero.
IP DMA chaining	No DMA: no chaining.	IP chained DMA functional at 8MHz, but not at 32MHz.	Chained DMA now functional with 32MHz IP bus frequency as well as 8MHz.
Check bits	Two banks of eight bits each.	Two banks of eight bits each.	Single bank of seven bits.
Register shadowing	Registers shadowed by a second set of registers.	Registers shadowed by a second set of registers.	No register shadowing.
Ethernet	N82C501AD device.	N82C501AD device.	LXT901 device (software-transparent)