MOTOROLA

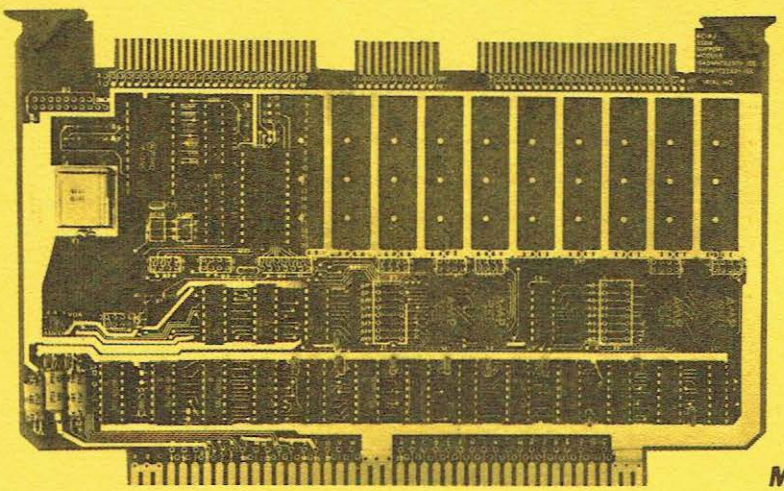
MEX68502(D)

MEX6850-2

ACIA/SSDA MODULE

User's Guide

SYSTEMS



MICROSYSTEMS

MEX68502(D)
JUNE 1978

MEX6850-2

ACIA/SSDA MODULE
USER'S GUIDE

First Edition

24-A79/2.0

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, preparation for use and installation instructions, programming considerations, and theory of operation for the MEX6850-2 ACIA/SSDA Support Module. A typical module is illustrated in Figure 1-1.

1.2 FEATURES

The features of the ACIA/SSDA Module include:

- Eight and nine-bit transmission
- Program selectable odd, even, or no parity
- Program selectable ÷ 16 and ÷ 64 clock modes
- Program selectable one or two stop bits
- Eight jumper selectable baud rates between 110 and 9600 baud
- Provisions on the module to construct custom circuitry
- May be configured to appear as a terminal or as a modem to an external communications device

1.3 ACIA/SSDA MODULE SPECIFICATIONS

The ACIA/SSDA Module specifications are identified in Table 1-1.

1.4 GENERAL DESCRIPTION

The MEX6850-2 ACIA/SSDA Module provides the user with a flexible means of interfacing his EXORciser user's system with a communications device. The user has the option of interfacing this module with a TTY, cassette handlers, disk drives, external terminal, or an RS-232C compatible device, by constructing a custom interface circuit. This module may be configured to appear as a data terminal or as a modem to the external communications device.

In preparing the module to work with the EXORciser, the user selects the data transfer rate and base memory for the MC68B50 ACIA or the MC68B52 SSDA device. The module provides eight standard jumper selectable baud rates between 110 and 9600 baud. The EXORciser's MPU Module addresses the MC68B50 ACIA or the MC68B52 SSDA device as if it were memory. The base memory address switches on the ACIA/SSDA Module allow the user to select the base memory address for the ACIA or SSDA device.

In preparing his user programs for this module, the user determines parity, the number of stop bits, and the ACIA's clock mode. The user selects one or two stop bits; odd, even, or no parity; divide-by-16 or divide-by-64 clock mode; the number of data bits to be transferred; SSDA synchronization mode; and byte transfer.

The module has provisions for standard wirewrap sockets, allowing the user to construct custom circuitry on the module. The module also supplies a sufficient number of jumper connections to modify this module, as required, to meet the user's interface needs.

TABLE 1-1. ACIA/SSDA Module Specifications

CHARACTERISTICS	SPECIFICATIONS
Power Requirements	+5 Vdc at 500 mA
Data Terminal Interface Baud Rate, jumper selectable	110, 150, 300, 600, 1200, 2400, 4800, 9600
Parity	Program selectable: odd, even, or no parity
Stop Bit Select	Program selectable: one or two stop bits
Number of Bits Transferred	Program selectable: eight or nine data bits
Physical Characteristics	
Width X Height Board Thickness	9.75 in. x 6.15 in. 0.062 in.
Operating Temperature	0^{o} to 70^{o}c

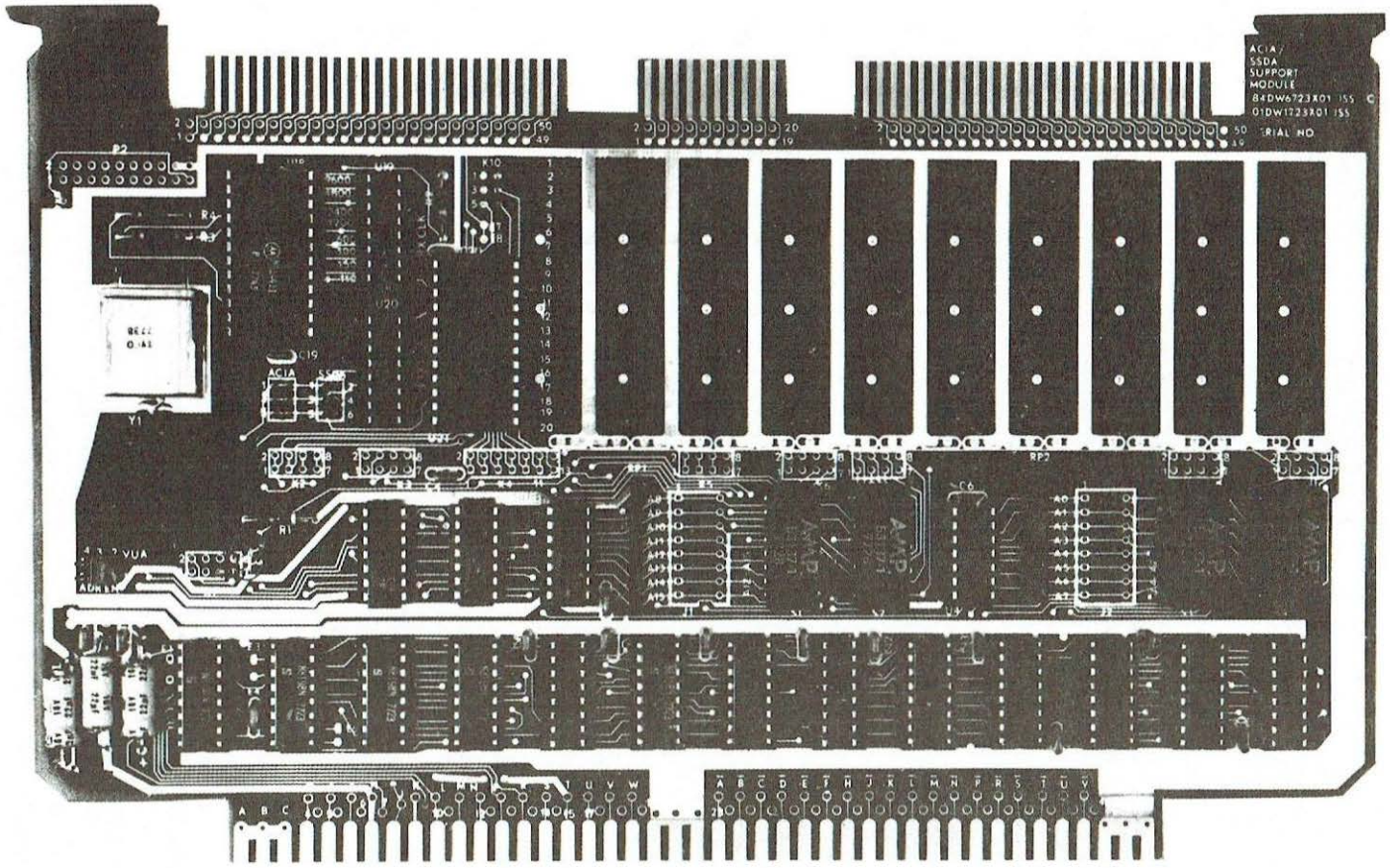


FIGURE 1-1. MEX6850-2 ACIA/SSDA Module

CHAPTER 2

INSTALLATION, PROGRAMMING, AND INTERCONNECTION CONSIDERATIONS

2.1 INTRODUCTION

This chapter provides the unpacking, inspection, installation, and preparation for use instructions for the MEX6850-2 ACIA/SSDA Module. This chapter also discusses the module bus interconnection signals, the function of the module switches, and the module programming considerations.

2.2 UNPACKING

Unpack the ACIA/SSDA Module from its shipping carton and, referring to the packing list, verify that all of the parts are present. Save the packing material for storing the module. If the shipping carton is damaged upon receipt, request that the carrier's agent be present while the module is being unpacked and inspected.

2.3 INSPECTION

The ACIA/SSDA Module should be inspected upon receipt for broken, damaged, or missing parts, and the printed circuit board for physical damage.

2.4 HARDWARE PREPARATION

2.4.1 Module Switches and Jumpers

Figure 2-1 identifies the location of the switches on the ACIA/SSDA Module, and Table 2-1 identifies the function of each of the module switches and jumpers.

TABLE 2-1. ACIA/SSDA Module and Jumper Functions

REFERENCE DESIGNATION	DESCRIPTION
ADDRESS LINE SELECT (J1-J2)	These address line select pads enable the user to simulate his system by disabling the address lines he is not using.
ACIA/SSDA ADDRESS (S1-S4)	The ACIA/SSDA ADDRESS switches select the base memory address for the ACIA/SSDA device.
I/O SELECT (K10)	This header gives the user access to the data and control lines of the ACIA or SSDA.
ADDR BUS CONNECT (K6-K9)	Provides user access to the buffered address bus with user supplied headers.
DATA BUS CONNECT K2,K4	Provides user access to the buffered data bus and provisions for bus driver control with user supplied headers.
TIMING AND CONTROL CONNECTS K1,K3,K5	Provides user access to various bus timing and control signals with user supplied headers.

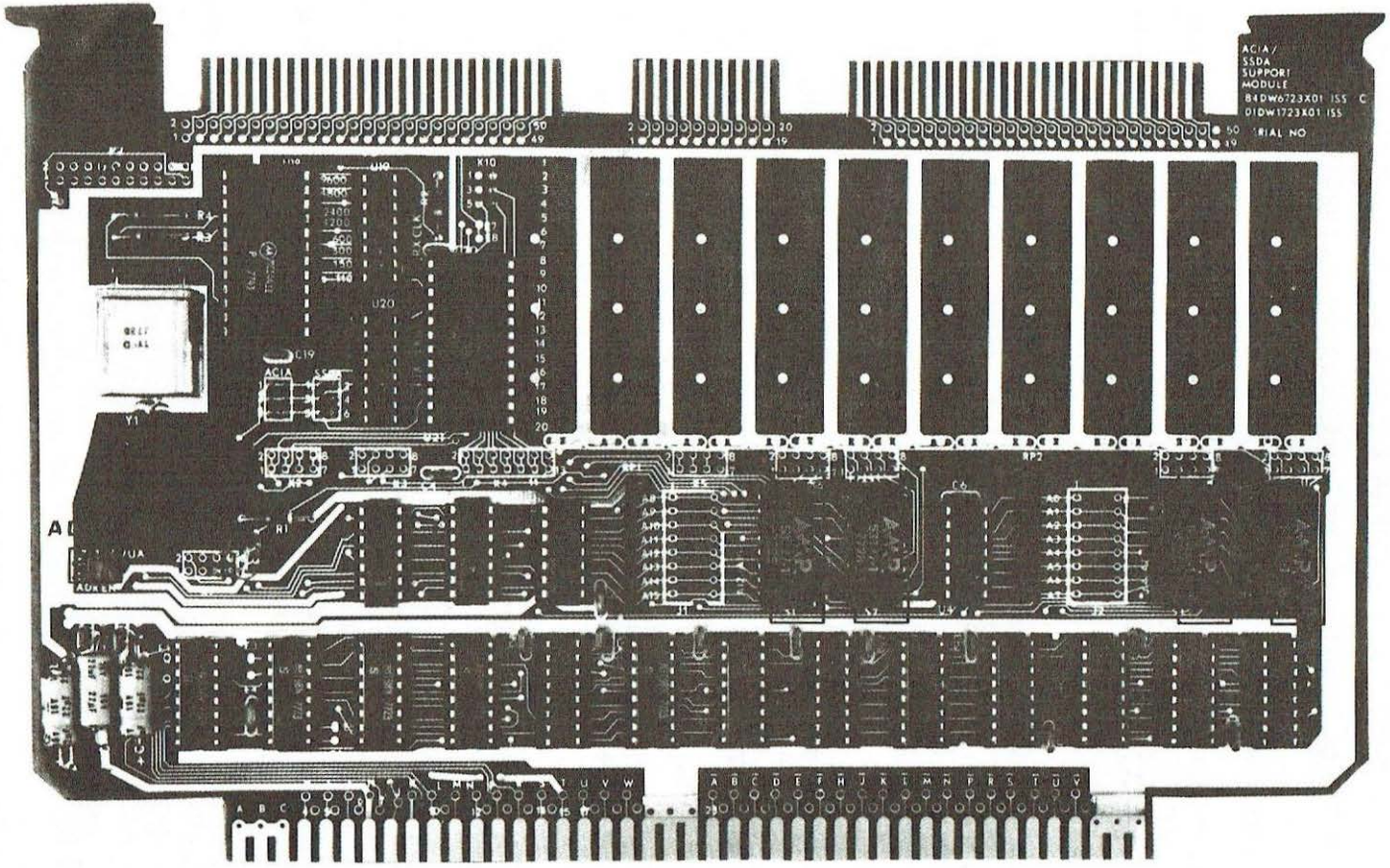


FIGURE 2-1. MEX6850-2 ACIA/SSDA Module, Switch Locations

2.4.2 Module and Device Interconnections

The following paragraphs discuss the ACIA/SSDA Module interconnections with the EXORciser bus. Also included in these paragraphs are methods of preparing custom circuitry.

2.4.3 Module Interface

The ACIA/SSDA Module interconnects directly with the EXORciser bus. The bus signals are identified in Table 2-2. This table lists each pin connection, the signal mnemonic, and the signal characteristics.

TABLE 2-2. Connector P1 Bus Interface Signals

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
A,B,C	+5 VDC	+5 Vdc - Used for the module logic circuits.
D	$\overline{IRQ}$	INTERRUPT REQUEST - This signal requests that an MPU interrupt sequence be generated within the machine. The MPU will wait until it completes the current instruction that it is executing before it recognizes the request. At that time, if the interrupt mask bit in the MPU condition code register is not set (interrupt not masked), the MPU will begin the interrupt sequence. The ACIA or SSDA on the Module, at the user's option, is capable of generating an $\overline{IRQ}$ signal.
E,F		Not used.
H	GND	GROUND for ±12 Vdc.
J	ø2	Phase 2 (ø2) clock signal - Used to transfer data between the ACIA or SSDA and the MPU Module.
K	GND	GROUND for ±12 Vdc.
L		Not used.
M	-12 VDC	-12 Vdc - Usable with custom interface circuitry.
N,P,R,S		Not used.
T	+12 VDC	+12 Vdc - Usable with custom interface circuitry.
U,V		Not used.
X,Y,Z	GND	GROUND
$\overline{A}$-$\overline{F}$		Not used.
$\overline{H}$	$\overline{D3}$	DATA BUS ($\overline{D3}$) - This bi-directional line, when enabled, provides a two-way transfer between the MPU Module and the ACIA/SSDA Module. The data bus receivers on the ACIA/SSDA Module are in their off or high-impedance state except when the Module is selected during a memory write operation. The data bus drivers on this module are in their off or high-impedance state except when the Module is selected during a memory read operation.

TABLE 2-2. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
J	D7	DATA BUS (D7) - Same as D3 on P1-H.
K	D2	DATA BUS (D2) - Same as D3 on P1-H.
L	D6	DATA BUS (D6) - Same as D3 on P1-H.
M	A14	ADDRESS BUS (A14) - This address line, when enabled, transfers the MPU program counter output to the ACIA/SSDA Module.
N	A13	ADDRESS BUS (A13) - Same as A14 on P1-M.
P	A10	ADDRESS BUS (A10) - Same as A14 on P1-M.
R	A9	ADDRESS BUS (A9) - Same as A14 on P1-M.
S	A6	ADDRESS BUS (A6) - Same as A14 on P1-M.
T	A5	ADDRESS BUS (A5) - Same as A14 on P1-M.
U	A2	ADDRESS BUS (A2) - Same as A14 on P1-M.
V	A1	ADDRESS BUS (A1) - Same as A14 on P1-M.
W,X,Y	GND	GROUND
1,2,3	+5 VDC	+5 Vdc - Used for the module logic circuits.
4,5		Not used.
6	R/W	READ/WRITE - This MPU output signal indicates to the ACIA/SSDA Module whether the MC6800 MPU is performing a memory read (high) or write (low) operation. The normal standby state of this signal is read (high). Also, when the MC6800 is halted, this signal will be in the read state.
7		Not used.
8,9	GND	GROUND for ±12 Vdc
10	VUA	VALID USER'S ADDRESS - This signal, when high, indicates that the address on the address bus is valid and the EXORciser is not addressing its EXbug Memory Map.
11	-12 VDC	-12 Vdc - Used with custom interface circuitry.
12,13,14,15		Not used.
16	+12 VDC	+12 Vdc - Used with custom interface circuitry.
17,18		Not used.
19	VXA	VALID EXBUG ADDRESS - This signal, when high, indicates that the address on the address bus is valid and the EXORciser is EXbug Memory Map.
20,21,22	GND	GROUND
2[illegible]		Not used.
29	D1	DATA BUS (D1) - Same as D3 on P1-H.
30	D5	DATA BUS (D5) - Same as D3 on P1-H.
31	D0	DATA BUS (D0) - Same as D3 on P1-H.
32	D4	DATA BUS (D4) - Same as D3 on P1-H.

TABLE 2-2. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
33	A15	ADDRESS BUS (A15) - Same as A14 on P1-$\overline{M}$.
34	A12	ADDRESS BUS (A12) - Same as A14 on P1-$\overline{M}$.
35	A11	ADDRESS BUS (A11) - Same as A14 on P1-$\overline{M}$.
36	A8	ADDRESS BUS (A8) - Same as A14 on P1-$\overline{M}$.
37	A7	ADDRESS BUS (A7) - Same as A14 on P1-$\overline{M}$.
38	A4	ADDRESS BUS (A4) - Same as A14 on P1-$\overline{M}$.
39	A3	ADDRESS BUS (A3) - Same as A14 on P1-$\overline{M}$.
40	A0	ADDRESS BUS (A0) - Same as A14 on P1-$\overline{M}$.
41,42,43	GND	GROUND

2.4.4 ACIA/SSDA Configuration

The MEX6850-2 ACIA/SSDA Module is factory wired for operation with an MC68B50 ACIA installed in U21. Operation of an MC68B52 SSDA device can be accomplished by cutting jumpers 1-2, 3-4, and 5-6 on the ACIA personality header, and installing jumpers 1-2, 3-4, and 5-6 on the SSDA personality header.

CAUTION

STORE UNUSED ACIA OR SSDA DEVICE IN CONDUCTIVE FOAM TO PREVENT POSSIBLE DAMAGE.

2.4.5 Customized Circuitry

The wirewrap section of the module provides the user with the option of constructing customized circuitry on the module to meet his specific needs. Install customized circuitry as follows:

a. Remove the MC68B50 ACIA or MC68B52 SSDA device from the module.

CAUTION

REMOVE THE MC68B50 ACIA or MC68B52 SSDA DEVICE WHILE CONSTRUCTING OR CHANGING YOUR CUSTOMIZED CIRCUITRY. DO NOT INSTALL THE MC6850 ACIA UNTIL YOU HAVE COMPLETED AND CHECKED OUT YOUR CIRCUITRY. INCORRECT AND INDUCTED VOLTAGES MAY DESTROY THE ACIA OR SSDA. ALSO, STORE THE ACIA AND SSDA IN CONDUCTIVE FOAM WHEN NOT IN THE CIRCUIT.

b. Install the wirewrap sockets on the module

c. Construct your circuit on the module. Refer to Table 2-3 for I/O select pinout.

d. After you have checked out your circuitry, reinstall the MC68B50 ACIA or MC68B52 SSDA device on the module.

TABLE 2-3. Device I/O Connector (K10)

PIN NO.	REFERENCE	FUNCTION
1	Rx Data	High impedance TTL compatible input through which data is received in a serial format.
2	TX Data	Transfers serial data out to a modem or other peripheral.
3	RTS/DTR	With an MC68B50 ACIA installed, this enables control over a peripheral. With an MC68B52 SSDA installed, this provides four functional synch match outputs depending on SSDA control bits.
4	$\overline{CTS}$	Provides a real time inhibit to the serial transmitter section.
5	$\overline{IRQ}$	TTL compatible, open drain, active low output used to interrupt the MPU.
6	$\overline{DCD}$	Provides a real time inhibit to the serial receiver section.

2.4.6 RS-232C Interface Connections and Interconnect Preparations

The ACIA/SSDA Module can interface with an RS-232C compatible communications device, and may be configured to appear as a modem or as a terminal. Table 2-4 identifies the RS-232C signals, their mnemonics, and their characteristics. Customized circuitry is required in preparing the ACIA/SSDA Module as a terminal or as a modem.

2.4.7 Available Interconnects

Three input/output edge connectors, one 20-pin and two 50-pin, are provided for custom circuitry interface. The 120 lines are accessible at plated-through holes. If the user desires to implement header connectors rather than the edge type, the mechanical arrangement of the plated-through holes will accommodate connectors with .100 inch pin spacing and .025 inch pin diameter.

2.4.8 Transmit/Receive Clock

The ACIA/SSDA Module can transfer and receive data at differing baud rates. Configure the module as follows:

a. Referring to the schematic, install a jumper between the selected transmit data baud rate terminal and TX CLK on jumper platform U20.

b. Install a jumper between the selected data receive rate and RX CLK on jumper platform U19.

2.4.9 $\overline{IRQ}$ Interrupt Enable

If you are using the $\overline{IRQ}$ interrupt capability of the MC68B50 ACIA or MC68B52 device, connect driving circuitry to K3, pin 1.

TABLE 2-4. RS-232C Interconnections

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
1	PROTECTIVE GROUND	POWER GROUND - Common for the 12 volt source. This line provides a safety ground connection to the RS-232C compatible terminal.
2	TRANSMIT DATA	TRANSMIT DATA - This line transfers data from a modem to a terminal.
3	RECEIVE DATA	RECEIVE DATA - This line transfers data from a modem to a terminal.
4	REQUEST TO SEND	REQUEST TO SEND - This signal prepares the modem for data transfer. When high, this signal places the modem in the transmit mode and, when low, in the receive mode.
5	CLEAR TO SEND	CLEAR TO SEND - This signal, when high, indicates the modem is ready to transmit data.
6	DATA SET READY	DATA SET READY - This signal is a high level when the modem is connected to the terminal and indicates to the terminal that the modem is ready.
7	SIGNAL GROUND	SIGNAL GROUND - This line provides a common signal connection to the RS-232C communications device.
8	RECEIVED LINE SIGNAL DETECTOR	RECEIVED LINE SIGNAL DETECTOR - This signal is a high level when the modem is receiving a signal meeting its criteria.
9-19		Not used.
20	DATA TERMINAL READY	DATA TERMINAL READY - This line, when high, indicates to the modem that the terminal is connected into the system is ready.
21-25		Not used.

2.5 PROGRAMMING CONSIDERATIONS

The programming considerations in this chapter are a supplement to the M6800 User's Guide, and discuss only the specific programming consideration of this module.

2.5.1 Module Programming Considerations

The ACIA Module provides the user with the capability of interfacing an MC6850-2 ACIA/SSDA Module to a communications device. In using this device, the user must determine:

- Whether to use the module's $\overline{IRQ}$ interrupt capability or a polling routine.
- The ACIA clock mode - divide-by-16 or divide-by-64.
- The number of data bits to be transferred.
- Parity - odd, even, or no parity.

. The number of stop bits to be used - one or two.

. Checking the status word for errors and if an error exists, reverting to the appropriate error routine in the user's program.

Switches S1 through S4 on the module allow the user to select the base memory address for the ACIA.

2.5.2 MC68B50 ACIA and MC68B52 SSDA Device Programming Information

The MC68B00 MPU addresses the MC68B50 ACIA and MC68B52 SSDA as if it were memory. Therefore, all commands to the Module are executed by the MPU as memory reference instructions. The M6800 Systems Reference and Data Sheets illustrate the ACIA/SSDA addressing the operation being performed by the selected register. Note that the MPU can only read the receive data register and the status register and can write into the transmit data register and control registers.

The M6800 System Reference and Data Sheets also discuss the function of each of the bits in the control register and the function of the bits in the status register.

2.5.3 Module Programming Instructions

a. Construct a memory map and assign the base memory address for the MC6850-2 ACIA/SSDA Module.

b. Determine the address lines that are going to be used in your system.

c. Determine whether you are going to use the module's $\overline{IRQ}$ interrupt capability or use a polling routine.

d. Prepare the appropriate command words for the selected number of stop bits, parity, the number of bits to be transferred, the module's clock mode, etc.

e. Incorporate in your program routines to check the appropriate status word for errors and the appropriate error routines.

2.6 SWITCH SETTINGS

Set the ACIA/SSDA Module switches as follows:

a. Set the address switches (S1 through S4) to the selected base memory address.

b. Referring to step b of Paragraph 2.5.3, cut jumpers on J1 and J2 to disable the address lines not being used.

2.7 INSTALLATION INSTRUCTIONS

Install the ACIA/SSDA Module as follows:

a. Turn the PWR switch OFF.

CAUTION

INSERTING AN ACIA/SSDA MODULE WHILE POWER IS APPLIED TO THE EXORciser MAY RESULT IN DAMAGE TO COMPONENTS ON THE MODULE.

b. Install the module in the selected card slot. This module may be installed only in the six outside card slots (three on each side).

c. Connect any custom external device to the ACIA/SSDA Module.

d. Turn the PWR switch ON.

CHAPTER 3

THEORY OF OPERATION

3.1 INTRODUCTION

This chapter provides a block diagram description of the MEX6850-2 ACIA/SSDA Module. A block diagram of this module is illustrated in Figure 3-1, and its schematic diagram is presented in Figure 3-2.

3.2 BLOCK DIAGRAM DESCRIPTION

The MEX6850-2 ACIA/SSDA Module (illustrated in Figure 3-1) receives the 16 address bits A0 through A15 along with the ø2 timing signal, the VUA (Valid User's Address), VXA (Valid EXbug Address), and the R/W (Read/Write) command during each MPU memory operation. THE VA (Valid Address) signal is made by jumpering to VUA, VXA, or PAGE ENABLE. During a memory write operation, this module also receives the data bits D0 through D7. The module applies the 16 address bits to the address bus interface and the ø2 timing signal, the VA signal, and the R/W command to the control bus interface. The address bus interface, after buffering its inputs, applies the address bit A0 directly to the MC68B50 ACIA or MC68B52 SSDA device, address bit A0 to the baud rate generator, and the 15 address bits A1 through A15 with their complements to the address decoder.

The control bus interface, after buffering its inputs, applies the VA signal, ø2 timing signal, and the R/W command to the control logic and to the MC68B50 ACIA or MC68B52 SSDA device.

The data bus interface provides a two-way data transfer between MC68B50 ACIA or MC68B52 SSDA device and the EXORciser bus. The drivers and receivers in the bus interface are three-state logic devices and in their disabled state, provide a high impedance output. The control logic circuit controls the operation of the data bus interface.

The address decoder circuit, consisting of the base memory address switches, the address line enable/disable jumpers, and a decoding network, decodes the 15 address bits it receives and determines when the EXORciser is addressing its MC68B50 ACIA or MC68B52 SSDA device. The base memory address switches select the base memory address for the ACIA/SSDA device. The address select line jumpers enable/disable the individual address lines. Disabling individual address lines enables the user to emulate systems using and not using all of the MPU address lines. The decoding network determines when the MPU is addressing the ACIA or SSDA device. This circuit, on determining that the EXORciser MPU is addressing the ACIA or SSDA device, couples a CS (Chip Select) signal to the ACIA and the control lock. The CS bit with address bit A0 is used to address the ACIA or SSDA device.

The operation of the MC68B50 ACIA and MC68B52 SSDA devices are discussed in the M6800 System Reference and Data Sheets.

During an MPU memory read operation, the control bus interface receives a high level R/W command and applies this command to the MC68B50 ACIA or MC68B52 SSDA device. This interface circuit also applies the R/W command with its complement to the control logic. The high level R/W command enables the ACIA or SSDA to transfer a status or data word to the data bus interface. (Refer to the ACIA programming considerations in Chapter 2 to determine the information being transferred.) At this time, the control logic applies a $\overline{\text{DATA OUT EN}}$ signal to the data bus interface. This enables the data bus interface to transfer data from the MC68B50 ACIA to the EXORciser data bus lines $\overline{\text{D0}}$ through $\overline{\text{D7}}$.

During an MPU memory write operation, the control bus interface receives a low level R/W command and the data bus interface receives an eight bit input from the MPU via the EXORciser bus. This input may be a data word or a command word. (Refer to the ACIA programming considerations in Chapter 2 to determine the data being transferred.) The control bus interface applies a low level R/W command to the ACIA device and to the control logic. It also applies the high level $\overline{\text{R/W}}$ command to the control logic and baud rate generator. The control logic now applies a $\overline{\text{DATA IN EN}}$ signal to the data bus interface, enabling this circuit to transfer data from the EXORciser bus to the ACIA device and data bit D1 to the baud rate generator. The ACIA is enabled at this time by the low level R/W command to accept and process the word on the EXORciser bus. During the transfer of a command word to the ACIA, the R/W command enables the baud rate generator to accept data bit D1.

The baud rate generator provides the ACIA/SSDA Module with eight standard jumper selectable baud rates between 110 and 9600 baud. This crystal controlled circuit, through data bit D1 of the command word, allows the user to select the divide-by-16 or divide-by-64 clock mode. The baud rate generator is configured to apply baud rate signals to the ACIA for transmitting (TXCLK) and receiving (RXCLK) data. Jumper options on the module allow the user to configure the module for different data transmit and receive rates. This circuit also supplies the module with six additional jumper selectable baud rates.

The TTY interface circuit interfaces the ACIA/SSDA Module with a TTY data terminal configured for full duplex, 20mA neutral current loop operation. This interface circuit also provides a READER CONTROL signal to control the operation of modified manual TTY data terminals.

The RS-232C interface circuit interfaces the ACIA/SSDA Module with an RS-232C communications device. As shown on the block diagram and schematic, this circuit is configured to appear as a modem to a data terminal. The user can, by making the appropriate jumper connections (discussed in Chapter 2), reconfigure this circuit to appear as an RS-232C data terminal to an external device.

The ACIA/SSDA Module has provisions for standard wirewrap sockets allowing the user to build custom circuitry on this modul . This circuitry may include programmable baud rates or custom interface circuitry.

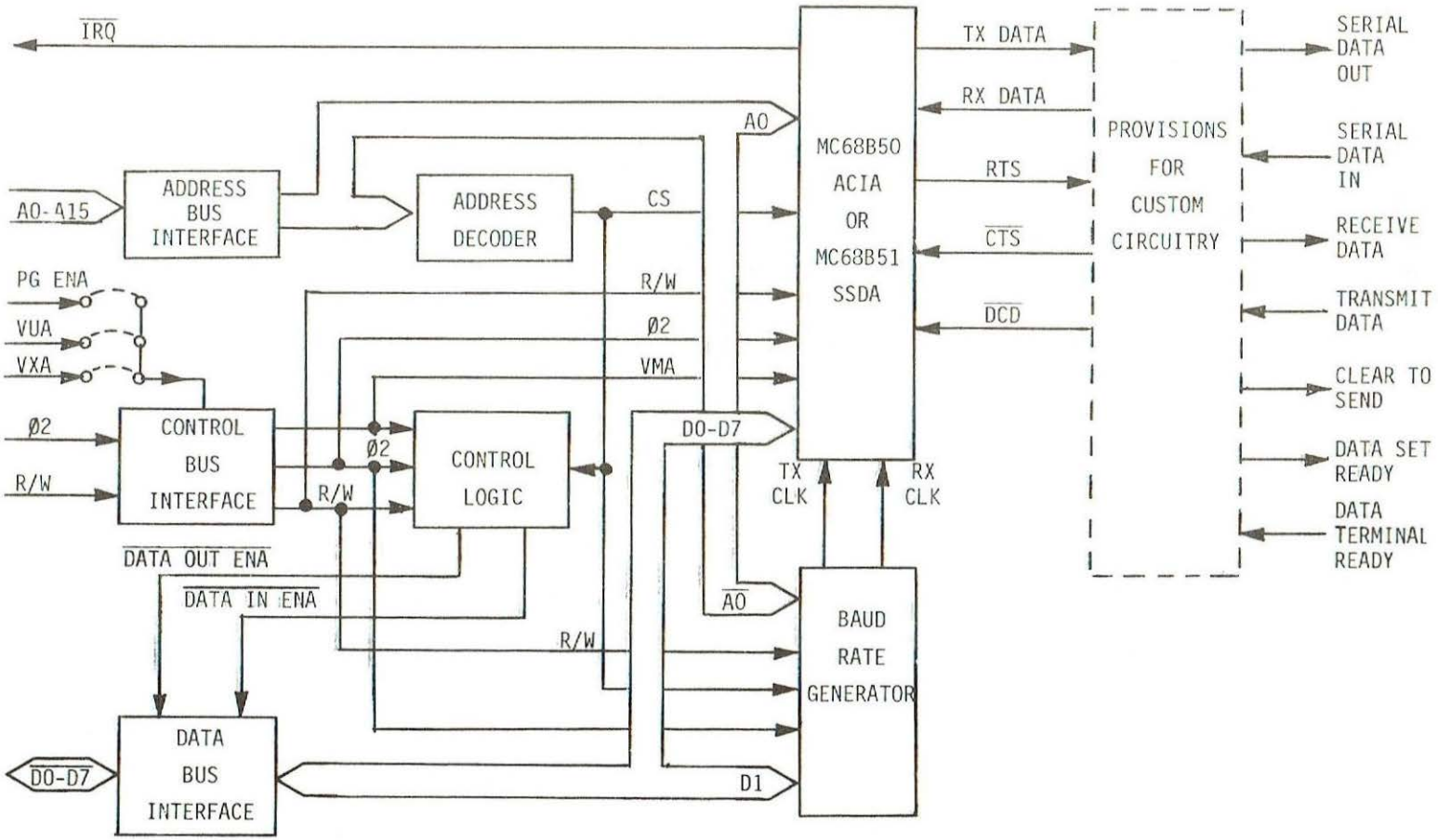
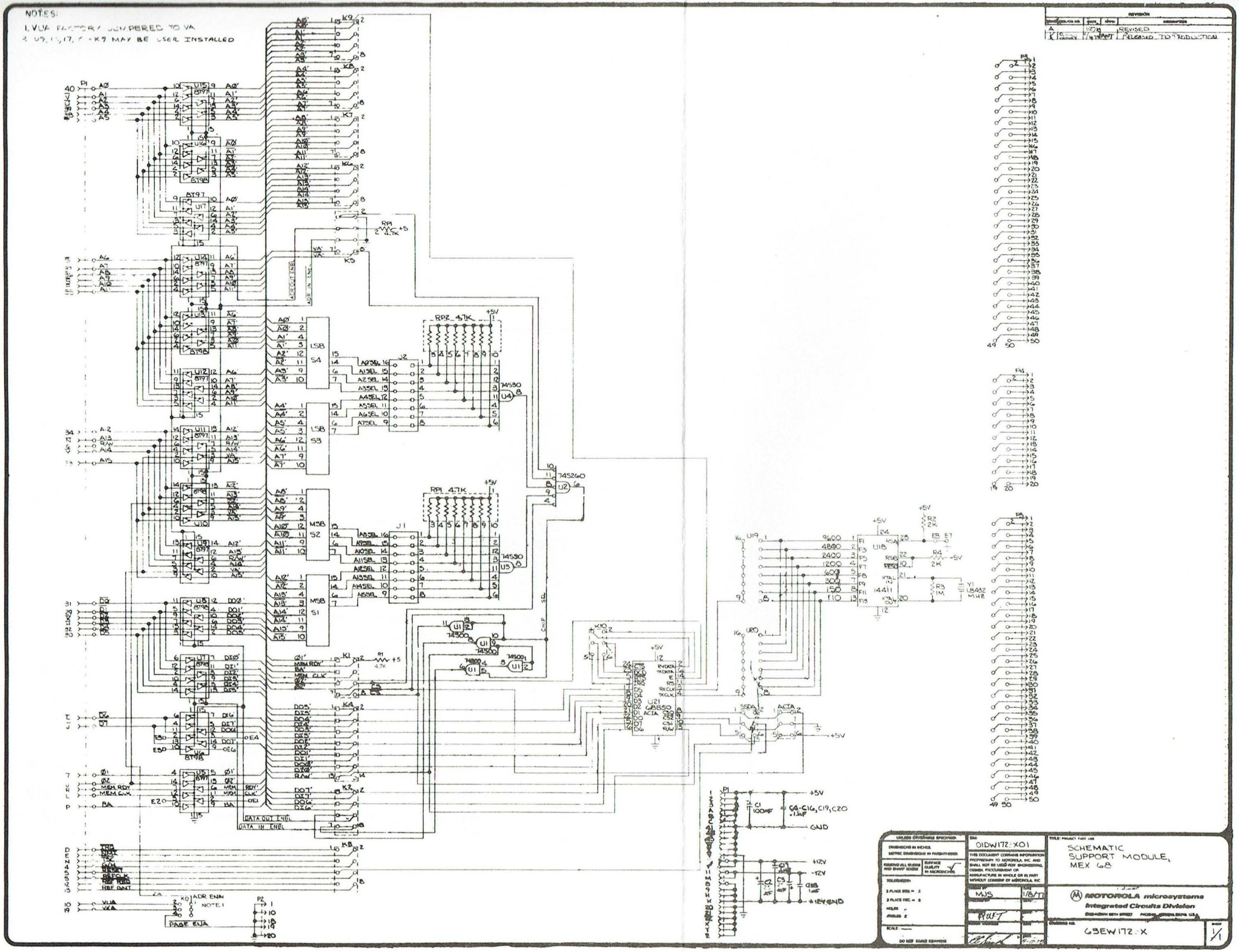


FIGURE 3-1. MEX6850-2 ACIA/SSDA Module Block Diagram


NOTES:
1. VUA FACTORY JUMPERED TO VA
2. U9, 15, 17, & K7 MAY BE USER INSTALLED
REVISION
A REVISED
RELEASED TO PRODUCTION
74S30
74S260
74S00
6850 ACIA
14411
1.8432 MHz
+5V
-12V
+12V
GND
PAGE ENA
DATA OUT ENBL
DATA IN ENBL
ADR ENA
CHIP SEL
UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
METRIC DIMENSIONS IN PARENTHESES
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CHAPTER 4

PARTS

4.1 INTRODUCTION

This chapter provides the parts list for the MEX6850-2 ACIA/SSDA Module. The list reflects the latest issue of hardware at the time of printing. Parts locations are shown on Figure 4-1.

TABLE 4-1. MEX6850-2 ACIA/SSDA Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
U5, U11, U14, U15	51NW9615B71	I.C., (8T97)	K
U6-U8, U10, U13, U16	51NW9615C36	I.C., (8T98)	K
U3, U4	51NW9615D93	I.C., SN74S30N	K
U2	51NW9615E67	I.C., SN74S260N	K
U1	51NW9615C94	I.C., SN74S00N	K
RP1, RP2	51NW9626A41	Resistor Network	K
C4-C20	21NW9702A09	Capacitor, Ceramic, 01 uf, 50 VDC	K
C1-C3	23NW9618A33	Capacitor, Elect., 25 uf, 16 VDC	K
S1-S4	40NW9801A31	Switch, HEX	K
U21	51NW9615D86	I.C., ACIA, Hi-Speed	K
U18	51NW9615B54	I.C., MC14411P	K
U19, U20	28NW9802B07	Socket, Dual Inline I.C.	K
K0-K10	28NW9802B88	Header, Post	K
U21	28NW9802B08	Socket, DIL I.C.	K
Y1	48BW1357X01	Crystal Osc., 1.8432 MHz	K
R3	06SW-124B22	Resistor, 1M, 5%, 1/4W	K
R2, R4	06SW-124A26	Resistor, 2K, 5%, 1/4W	K
U19, U20	28NW9802B16	Component Socket Adaptor	K
R1	06SW-124A65	Resistor, 4.7K, 5%, 1/4W	K

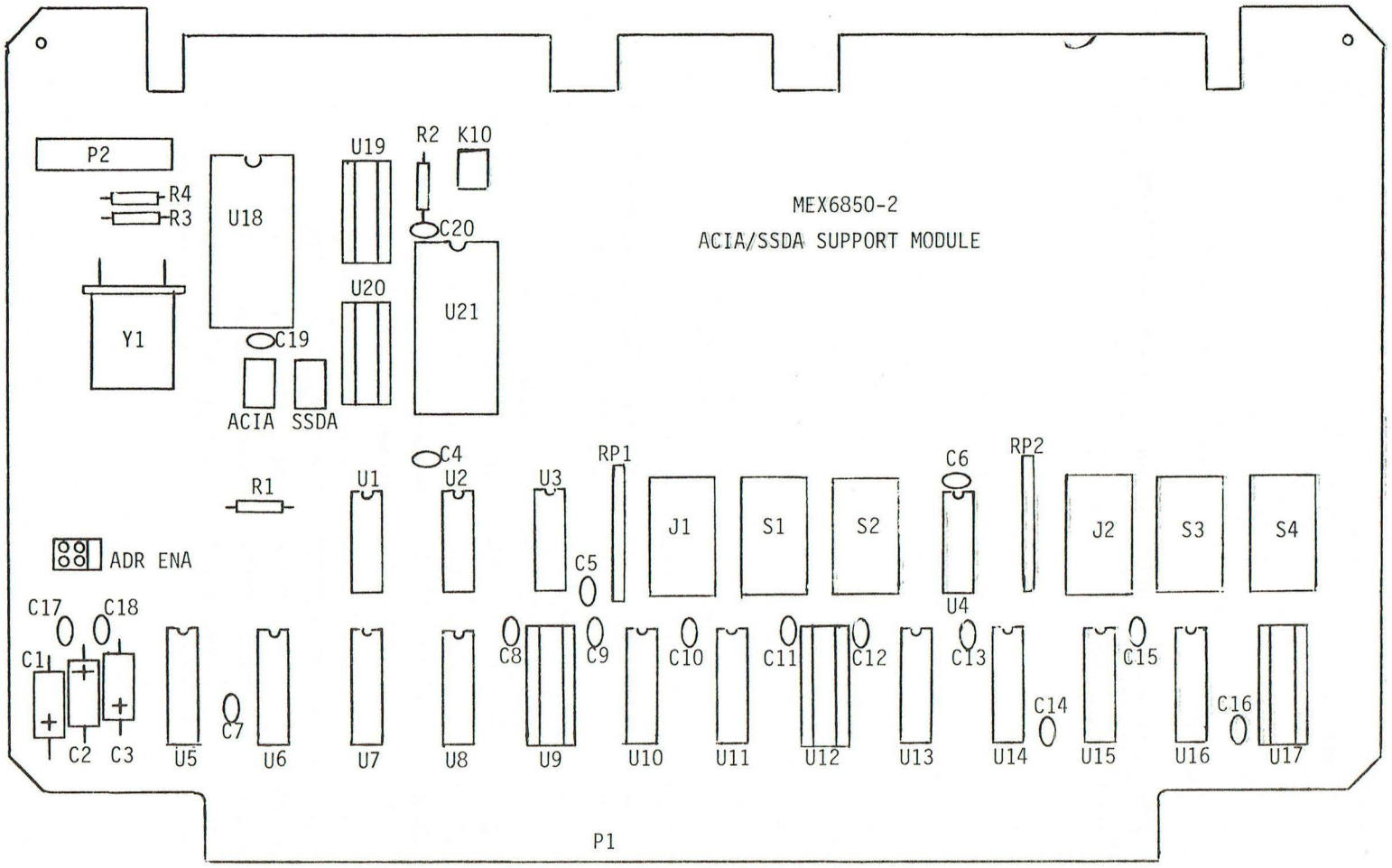

FIGURE 4-1. MEX6850-2 ACIA/SSDA Module, Parts Location