NS23L

TECHNICAL MANUAL

National Semiconductor

Memory Systems

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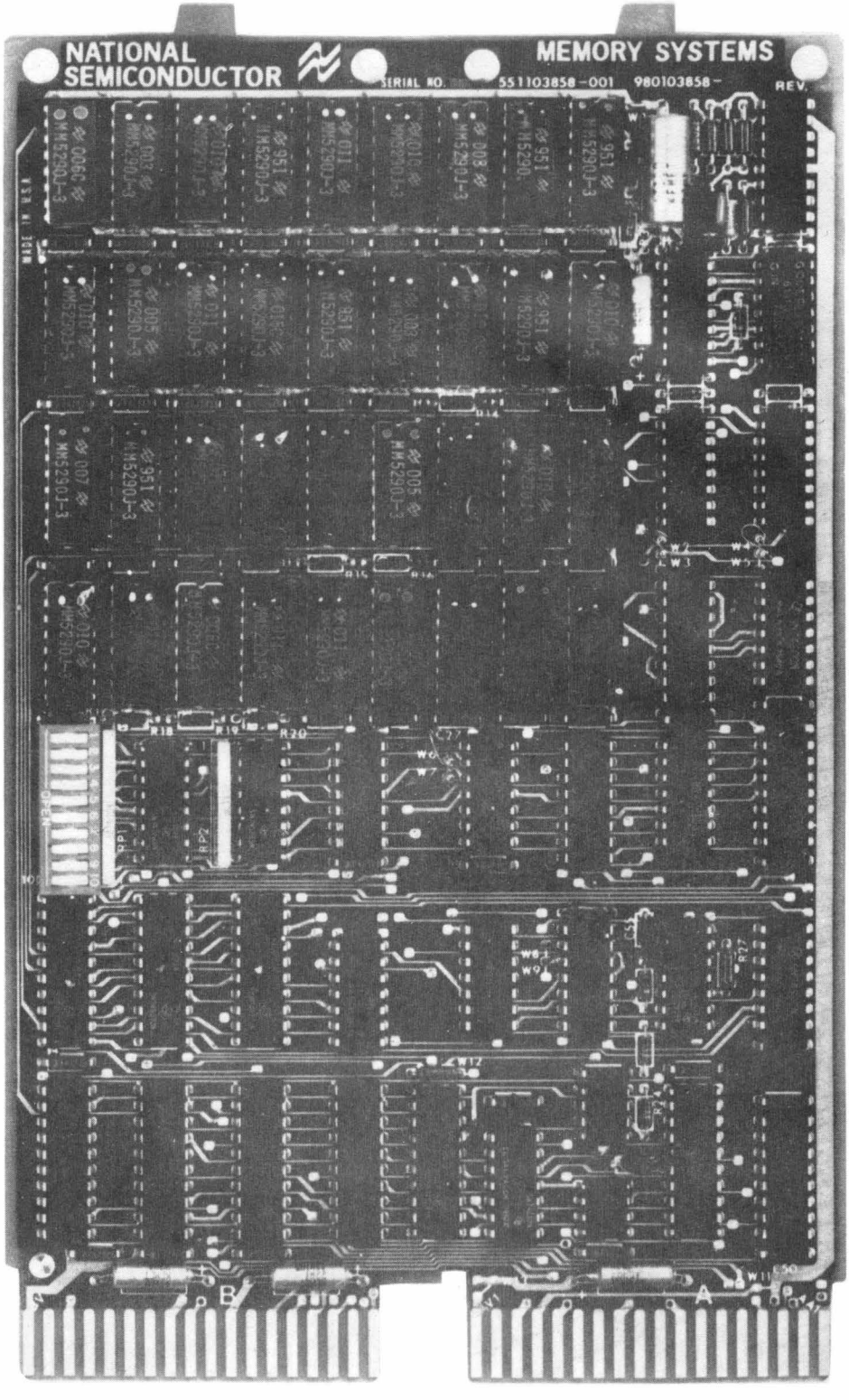


NS23L MEMORY MODULE

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual contains four sections which describe the NS23L Add-in Memory System. This information includes a general description, an installation and maintenance section, theory of operation, and an appendix containing assembly drawings schematics and bill of materials. Figure 1-1 is a photograph of the NS23L Memory card.

1.2 PURPOSE

The NS23L Memory Card is an add-in memory for the DEC (Digital Equipment Corp.) LSI-11 Microcomputer system.

The card has been designed to be mechanically and electrically compatible with the LSI-11, PDP-11/03, LSI-11/2 and PDP-11/23 Systems. The card is compatible with DEC MSV11-D and MSV11-E series semiconductor memory cards, and can be installed in the H9281, H9270, H9273-A (connector A&B only) or DDV11-B backplanes.

1.3 MECHANICAL DESCRIPTION

The physical and mechanical details of the memory card are outlined in this section.

1.3.1 GENERAL

The NS23L Memory is completely contained on one multilayer printed circuit board.

A. Standard LSI-11 Backplanes

The NS23L Memory Card is designed to plug directly into standard H9270 ("Quad") and H9281 ("Dual") LSI-11 backplane/card guide assemblies, and the DDV11-B ("Hex") expansion unit.

B. Precautions

In the H9270 and H9281 backplanes, slot one is reserved for the LSI-11 processor. The Memory Card may be inserted into any slot in these backplanes with the exception of slot number one.

If the DDV11-B expansion backplane is utilized, the memory card must be inserted into the A and B connectors of the backplane.

1.3.2 DIMENSIONS

PCB	Thickness	0.056" Nominal
	Width	5.19"
	Length	8.93"(Includes Plastic Handles)
Max. Component Height		0.375"
Total thickness max		0.490"

1.4 ENVIRONMENTAL SPECIFICATIONS

The NS23L is designed to operate over a variety of environmental conditions. Listed below are the environmental conditions and specifications.

1.4.1 OPERATING SPECIFICATIONS

- TEMPERATURE.....Ambient Air temperature range of $0^{o}C$ to $+55^{o}C$.
- THERMAL SHOCK....The NS23L Memory can withstand a thermal shock with a maximum rate of change of $30^{o}C$ per hour during operation.
- HUMIDITY.....0% to 95% relative humidity (without condensation).
- ALITIUDE.....-1000 feet msl to +10,000 feet msl.
- COOLING.....Suggested minimum air flow of 25 cfm.

1.4.2 SHIPPING AND STORAGE SPECIFICATIONS

- TEMPERATURE.....The NS23L Memory can withstand a temperature range of $-40^{o}C$ to $+85^{o}C$ during shipment or storage.
- THERMAL SHOCK....A thermal rate of change as high as $10^{o}C$ per minute can be tolerated by the Memory.
- ALTITUDE.....A Shipping Altitude of 40,000 feet can be withstood.
- MECHANICAL SHOCK.The NS23L Memory, housed in its shipping container, can tolerate mechanical shock resulting from drop tests performed in accordance with MIL-STD-810B, Method 516, procedure V, without exhibiting damage or degradation.

1.5 POWER REQUIREMENTS

1.5.1 PARAMETERS AND CONDITIONS

The NS23L Memory Card requires the following voltages:

1. +5.0 volts ± 5%
2. +12.0 volts ± 5%

1.5.2 POWER CONSUMPTION

The NS23L Memory Card, in a 32Kx18 configuration, has the following current requirements:

	STANDBY	OPERATING
+ 5.0 Volts	1.5 A Max. 1.2 A typ.	1.5 A Max. 1.2 A Typ.
+12.0 Volts	80 mA typ. 110 mA max.	350 mA typ. 400 mA max.

1.5.3 BATTERY BACK UP VOLTAGE REQUIREMENTS

The battery back-up voltages must meet the following requirements:

1. +12 ± 5% @ 110mA max.
80mA typ.

2. +5 ± 5% @ 550mA typ.
775mA max.

These current requirements are on a per-card basis.

1.6 ACCESS AND CYCLE TIMES

The performance of the memory card in an LSI-11 system is as follows:

Memory Function	Bus Cycle Type	Access Time (max)	Cycle Time (max)
Read	DATI	190ns	490ns
Write (Byte)	DATO (B)	90ns	390ns
Read/Modify/Write	DATIO (B)	700ns	1000ns

Notes: 1. If a memory cycle is requested during a Refresh operation, a delay of up to 500ns can be added to the above cycle times.

2. Read (DATI) cycle access time is defined as internal SYNC H to RPLY H with 25ns from SYNC H to DIN H. Write (DATO) cycle access time is defined as internal SYNCH H to RPLY H with 50ns from the SYNC H to DOUT H. All timings are taken at bus receiver outputs and bus driver inputs.

3. Cycle time is defined as SYNC H to SYNC H negated at maximum allowable LSI-11 bus speed.

1.7 OPTIONS

The NS23L is available with a varity of options to enhance the card.

1.7.1 MEMORY CAPACITY

The standard memory capacity of the memory card is:

32,768 words by 18 bits (32Kx18)

The 32,768 words can be assigned anywhere within the LSI-11 128K word* address space in 4K word increments.

* Optional extended addressing is available to 2 megawords.

1.7.2 OPTIONAL CAPACITIES

Optional capacities are available from a minimum of:

16,384 words by 16 bits (16Kx16) to a maximum of: 32,768 words by 18 bits (32Kx18).

1.7.3 PARITY GENERATION AND CHECK

See section 3.5

1.7.4 EXTENDED ADDRESS DECODING

Address decoding may be extended to 22 address lines for a total address range of two mega-words (four mega-bytes). See section 2.7 for implementation.

1.8 RELIABILITY

This card was designed to the best commercial standards of workmanship. Vigorous testing is conducted (including testing over operating temperature range) to ensure a reliable service of ten years at 24-hours per day usage (exclusive of routine maintenance time). The design is such that catastrophic failure occurrence is minimized and minimal propagation of such failure will be experienced.

SECTION II

INSTALLATION AND MAINTENANCE

2.1 GENERAL

This section contains the basic information for installing the NS23L memory module.

The NS23L can be installed in any backplane that is wired for DEC "Q Bus".

2.2 TOOLS REQUIRED

No special tools are required for installation. A ball-point pen or small stylus may be needed to set the switches mounted on the memory module.

2.3 UNPACKING AND INSPECTION

Carefully unpack the memory module and visually examine it for physical shipping damage; i.e. broken, bent or dented parts.

CAUTION

Do not attempt to install or operate memory if physical damage is apparent.

2.4 BACKPLANES

The NS23L will operate in the following backplanes as described.

H9270 - In the A-B or the C-D connector rows except the processor location.

H9273-A - Only in the A-B connector row.

H9281 - Any slot except slot 1 which must contain the processor board.

DDV11-B - In the A-B or the C-D connector row except the processor location. It cannot be installed in the E-F row unless the Q-BUS has been installed by the user.

2.5 PROCESSORS

The NS23L memory module will work with all standard LSI-11 and KDF11 processor modules. It should be noted that many LSI-11 processor modules have memory on board and the NS23L must be configured not to respond to the address range that is assigned to the resident memory. The MXV11 multi-function module may also have on board memory.

2.6 POWER CONSIDERATIONS

The NS23L requires only +5 vdc and +12 vdc. Jumper points are provided to implement battery backup voltages if desired. The module has the following maximum current requirements:

	NON-BATTERY OPERATING	BACKUP STANDBY	BATTERY BACKUP STANDBY ONLY
+5	1.5A	1.5A	-
+12v	.4A	.11A	.11A
+5vb	-	-	.770A

2.7 ADDRESS RANGE SELECTION

If using a processor that has an address space of 128K words refer to section 2.7.1 for switch settings. If memory management has increased the address space beyond 128K refer to section 2.7.2 for switch settings.

Switches S1 thru S12 assign the starting address of the module. The stopping address of the module is controlled by installing jumper W6 or W7, and the size of the memory. For a 16K word memory the stopping address is the starting address plus 16K. For a 32K word memory, the stopping address is the starting address plus 32K words. Jumper definitions are listed in table 2.3 and jumper locations are shown in figure 2.1.

2.7.1 STARTING ADDRESS ASSIGNMENT, 128K WORD

The NS23L memory may be started at any 4K word boundry in the LSI-11 128K word address space. Refer to table 2.1.

2.7.2 STARTING ADDRESS ASSIGNMENT GREATER THAN 128K WORD

When installing the NS23L in a bus where the maximum address is greater than 128K words, it is necessary to use table 2.2 in conjunction with table 2.1. It is also necessary to install jumper W12 and remove W16 (Etch cut).

First, determine the necessary starting address, then select the range, from table 2.2, that the starting address falls in. This will determine the setting for switches S6 thru S9.

Second, subtract the lower end of the range selected from the starting address. The difference will determine, from table 2.1, the settings for switches S1 thru S5. The following example may be helpful.

Example: It is desired to set the switches for a starting address of 1188K words.

1. 1188K falls in the range (from table 2.2) 1152K - 1278K, therefore switches S6 thru S9 would be set as follows, (from table 2.2).

ADDRESS RANGE	S6	S7	S8	S9
1152K-1278K	1	0	0	1

2. Subtract the lower end of the range selected from table 2.2 from the desired starting address:

   1188K - 1152K= 36K

3. Set switches S1 thru S5 according to the row in table 2.1 for 36K.

2.8 BATTERY BACK-UP

To implement battery back-up, etch jumpers must be cut between designated points and other wire jumpers installed. Feed thru's for installing BBU option jumpers are provived.

2.6.1 +5 VOLT BATTERY VOLTAGE

+5 volt battery voltage may be implemented by cutting etch jumper W13 and installing jumper W10. Jumper locations are shown in figure 2.1.

2.6.2 +12 VOLT BATTERY VOLTAGE

+12 volt battery voltage may be implemented by cutting etch jumpers W14 and W15 and installing jumper W11. Jumper locations are shown in figure 2.1.

STARTING ADDRESS*	SWITCH SETTINGS** S1	S2	S3	S4	S5
0K	0	0	0	0	0
4K	1	0	0	0	0
8K	0	1	0	0	0
12K	1	1	0	0	0
16K	0	0	1	0	0
20K	1	0	1	0	0
24K	0	1	1	0	0
28K	1	1	1	0	0
32K	0	0	0	1	0
36K	1	0	0	1	0
40K	0	1	0	1	0
44K	1	1	0	1	0
48K	0	0	1	1	0
52K	1	0	1	1	0
56K	0	1	1	1	0
60K	1	1	1	1	0
64K	0	0	0	0	1
68K	1	0	0	0	1
72K	0	1	0	0	1
76K	1	1	0	0	1
80K	0	0	1	0	1
84K	1	0	1	0	1
88K	0	1	1	0	1
92K	1	1	1	0	1
96K	0	0	0	1	1
100K	1	0	0	1	1
104K	0	1	0	1	1
108K	1	1	0	1	1
112K	0	0	1	1	1
116K	1	0	1	1	1
120K	0	1	1	1	1
124K	1	1	1	1	1

* In 4K word increments

** 0=OPEN (OFF)
1=CLOSED (ON)

STARTING ADDRESS SELECTION

TABLE 2-1

ADDRESS RANGE	SWITCH SETTINGS S6	S7	S8	S9
0K-128K*	1	1	1	1
0K-128K**	0	0	0	0
128K-256K	1	0	0	0
256K-384K	0	1	0	0
384K-512K	1	1	0	0
512K-640K	0	0	1	0
640K-768K	1	0	1	0
768K-896K	0	1	1	0
896K-1024K	1	1	1	0
1024K-1152K	0	0	0	1
1152K-1280K	1	0	0	1
1280K-1408K	0	1	0	1
1408K-1536K	1	1	0	1
1536K-1664K	0	0	1	1
1664K-1792K	1	0	1	1
1792K-1920K	0	1	1	1
1920K-2048K	1	1	1	1

0=OPEN (OFF)
1=CLOSED (ON)

* Standard configuration - Jumper W12 removed, W16 installed.

** Extended address option - Jumper W12 installed and W16 removed.

ADDRESS RANGE SELECTION

TABLE 2-2

TABLE 2.3

Jumper Definitions

Jumper	Purpose	Configuration
W1	-5V supply to array	I=Standard Configuration R=Factory Test Purposes Only
W2	Factory Test Aid	I=Standard Configuration R=Factory Test Purposes Only
W3	Factory Test Aid	I=Factory Test Purposes Only R=Standard Configuration
W4	Parity Error Enbl	I=Standard Configuration R=Factory Test Purposes Only
W5	Factory Test Aid	I=Factory Test Purposes Only R=Standard Configuration
W6	Mem Size Select	I=16K Word Memory R=32K Word Memory
W7	Mem Size Select	I=32K Word Memory R=16K Word Memory
W8	Refresh Select	I=External Refr Sel R=Internal Refr Sel
W9	Refresh Select	I=Internal Refr Sel R=External Refr Sel
W10	+5V Batt Supply	I=Batt Back-up Option R=Non-BBU
W11	+12V Batt Supply	I=Batt Back-up Option R=Non-BBU
W12	Extended Addr. Option	I=2M Word Addr Range R=0-128K Addr Range
W13 W14 W15	Standard Voltage Supplies	Etch Jumpers Remove for Battery Back-up option
W16	Extended Address Option	I=0-128K Address Range R=2M Word Address Range

Note 1 I= Installed
R= Removed

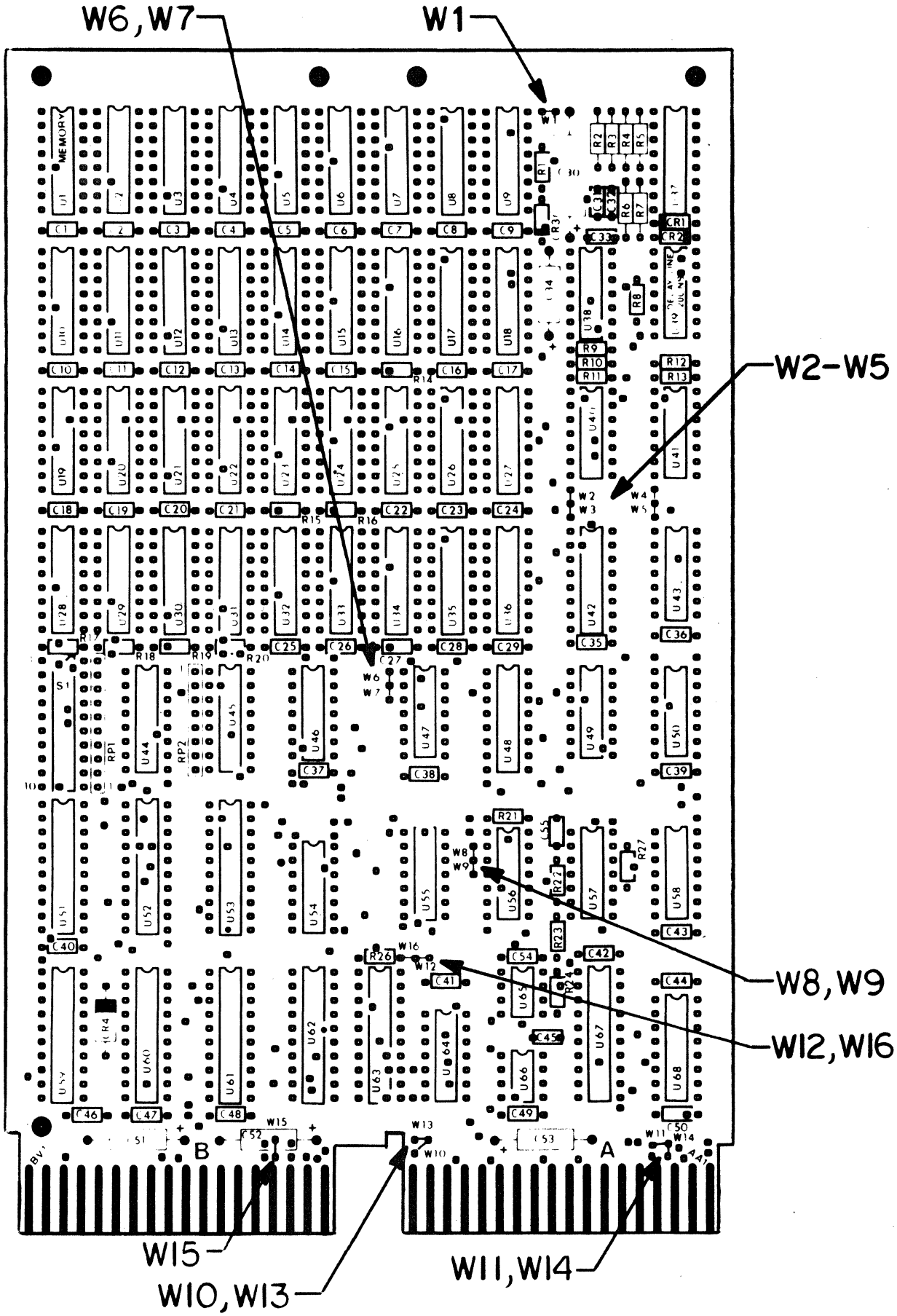


FIGURE 2.1 JUMPER LOCATION CHART

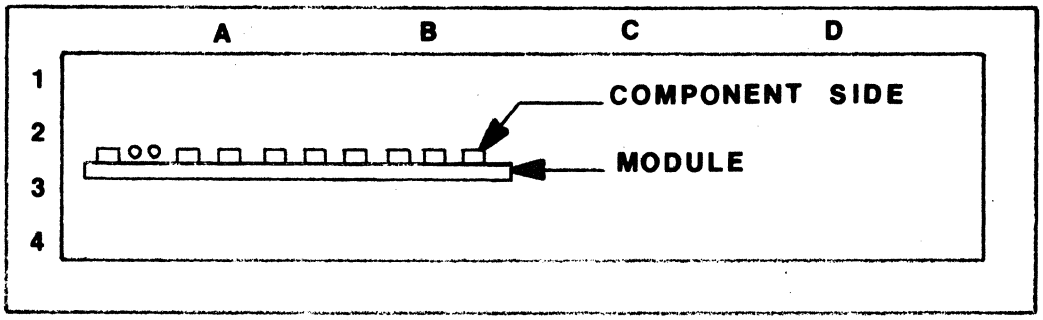


FIGURE 2.2 MODULE ORIENTATION

2.9 INSTALLING MEMORY MODULES

2.9.1 The memory module must be inserted into the backplane with components facing row 1 as shown in Figure 2-2.

CAUTION

Do not attempt to install or remove memory modules with DC power applied to the backplane. Damage to the memory may occur.

2.9.2 Insert the memory into connector slots A and B only if using a H9273A or H9281 backplane. If using a H9270 or a DDV11-B backplane, the memory may be installed in slots A and B or C and D.

2.10 VERIFYING MEMORY OPERATION

When memory modules are installed, apply DC power and verify operation by running the system diagnostics; in particular, those that test the memory.

2.11 MAINTENANCE

2.11.1 GENERAL

The memory itself does not require routine maintenance on a regularly scheduled basis. Systems diagnostics should be performed from time to time to verify correct operation.

2.11.2 TROUBLESHOOTING

In the event problems are encountered:

- Are all power supplies turned on? Verify that +5V and +12V power is applied to the backplane.
- Is the system configured properly? Verify that all modules are firmly seated and inserted into the backplane in their proper slots.
- Is the DMA priority daisy chain maintained? Verify that there are no empty slots between the first and last module.
- Are all system cables properly installed? Check that the cables are connected at each end.

SECTION III

THEORY OF OPERATION

3.1 GENERAL

The details in this section describe the operation of the memory card in the LSI-11 system.

3.2 INTERFACE

3.2.1 INTERFACE TIMING

Timing as given in figures 3-1 and 3-2 is taken at the bus receiver outputs and bus driver inputs.

It is assumed that all of the LSI-11 bus lines have proper termination. The timing as shown in Figures 3-1 and 3-2 is referenced to the +1.5V level of the signal transitions shown.

The timing values given in Paragraph 1.6 are also referenced to the same +1.5V level.

3.2.2 INTERFACE LOGIC LEVELS

The logic levels for the signals in/out of the memory card are as follows:

a) Input Signal Logic Levels

1) Logic One = 1.3 volts maximum
30 ua type. at 0.8V.

2) Logic Zero= 1.7 volts minimum
80 ua max. at 2.5V.

b) Output Signal Logic Levels

1) Logic One = 0.7 volts max. at 70 ma

2) Logic Zero= 2.4 volts min.
25 ua max. at 3.8 volts.

3.2.3 INTERFACE SIGNALS

There are seven (7) input control signals, two (2) output control signals, and twenty-two (22) bi-directional signal lines (address and data) on

the memory card. Refer to Figure 3-3 for the block diagram of internal signal flow.

Input Signals

The seven input control signals to the memory card are:

SIGNAL	CONNECTOR PIN
1. BDOUT	AE2
2. BDIN	AH2
3. BSYNC	AJ2
4. BWTBT	AK2
5. REFRESH(optional	AR1
6. BDCOK	BA1
7. BINIT	AT2

The memory card presents one standard bus load to the LSI-11 bus for each of the signals.

The standard input control signals perform the following functions:

BDOUT (AE2)

This signal, when asserted, indicates that a WRITE cycle (DATO) or the write portion of a READ-MODIFY-WRITE cycle (DATIO) is to be performed by the memory.

BDIN (AH2)

This signal, when asserted, indicates that a READ cycle (DATI) or the read portion of a READ-MODIFY-WRITE cycle (DATIO) is to be performed by the memory.

BSYNC (AJ2)

This signal, when asserted, indicates that a valid address is on the bus. When the address is in the operating range of the memory module, BSYNC will also initiate a memory cycle. The type of memory cycle is determined by the state of BDIN, BDOUT and BWTBT.

PARERR (AC1, BDAL 16)

See Paragraph 3.5.

BRPLY (AF2)

This signal is asserted in response to a memory cycle request. During write cycles (DATO, DATIO), RPLY indicates acceptance of data from the bus. During read cycles (DATI, DATIO), RPLY indicates that valid data will be on the bus within 125ns.

Bidirectional Signals

The twenty-two (22) bidirectional signal lines provide the memory card with address and data information. These lines are time-multiplexed between the address and data in/out during any cycle requested of the memory card externally.

The twenty-two (22) signals are:

SIGNAL	CONNECTOR PIN
1) BDAL 0L	AU2
2) BDAL 1L	AV2
3) BDAL 2L	BE2
4) BDAL 3L	BF2
5) BDAL 4L	BH2
6) BDAL 5L	BJ2
7) BDAL 6L	BK2
8) BDAL 7L	BL2
9) BDAL 8L	BM2
10) BDAL 9L	BN2
11) BDAL 10L	BP2
12) BDAL 11L	BR2
13) BDAL 12L	BS2
14) BDAL 13L	BT2
15) BDAL 14L	BU2
16) BDAL 15L	BV2
17) BDAL 16L	AC1
18) BDAL 17L	AD1
19) MMU DAL 18H	BC1
20) MMU DAL 19H	BD1
21) MMU DAL 20H	BE1
22) MMU DAL 21H	BF1

BWTBT (AK2)

This signal, when asserted during the leading edge of a BSYNC signal, indicates a write cycle (DATO or DATOB) is to be performed. If asserted during the duration of BDOUT, a byte write DATOB or DATIOB) will take place. The byte to be written is determined by the state of BDALØ during the leading edge of BSYNC. BDALØ = Ø indicates byte Ø; BDALØ = 1 indicates byte 1.

Refresh (AR1)

This is not a standard LSI-11 bus signal. If the memory module has been configured for the external refresh option, a high-to-low transition of this signal will trigger a refresh request into the memory refresh arbitration circuitry. If a memory cycle is in progress, the request will be honored at the end of the cycle and prior to initiating another cycle. A refresh cycle must be initiated once every 15±1 us. The external refresh signal can be synchronous or asynchronous.

BDCOK (BA1)

This signal goes active HI 3ms min. after DC is applied. It falls LO 5us min. before DC voltages are out of tolerance.

It is used to prevent the memory card from being selected on power-up or power-down.

BINIT (AT2)

This signal is used to reset internal select registers.

Output Signals

The two (2) output control signals available from the memory card are:

SIGNAL	CONNECTOR PIN
1. PARERR	AC1 (BDAL 16)
2. BRPLY	AF2

The standard output control signals perform the following functions:

The card interprets the data on these lines as shown in Figures 2-1 or 2-2 in relationship to BSYNC, BDIN, BDOUT and BRPLY. As shown in these Figures, the card interprets the data on these lines to be address information -75 to +25 nanoseconds around the leading edge of BSYNC. At all other times the information on these lines is interpreted by the card as either data into the card or data out of the card.

3.2.4 I/O CONNECTOR PIN LIST

The I/O Connector Pin List for the memory card is shown in Table 3-1.

Table 3-1. I/O Connector Pin List

Component Side	Pin	Pin	Solder Side
A Connector			
	A1	A2	+5 Volts
	B1	B2	
BDAL16 L	C1	C2	Ground
BDAL17 L	D1	D2	+12 Volts
	E1	E2	DBOUT L
	F1	F2	BRPLY L
	H1	H2	BDIN L
Ground	J1	J2	BSYNC L
	K1	K2	BWTBT L
	L1	L2	
Ground	M1	M2	BIAKI L
	N1	N2	BIAKO L
	P1	P2	BBS7 L
BREF L	R1	R2	BDMGI L
+12V BATT	S1	S2	BDMGO L
Ground	T1	T2	BINIT L
	U1	U2	BDAL00 L
+5V BATT	V1	V2	BDAL01 L
B Connector			
BDCOK	A1	A2	+5 Volts
	B1	B2	
MMU DAL 18H	C1	C2	Ground
MMU DAL 19H	D1	D2	+12 Volts
MMU DAL 20H	E1	E2	BDAL02 L
MMU DAL 21H	F1	F2	BDAL03 L
	H1	H2	BDAL04 L
Ground	J1	J2	BDAL05 L
	K1	K2	BDAL06 L
-5 Volts in	L1	L2	BDAL07 L
Ground	M1	M2	BDAL08 L
	N1	N2	BDAL09 L
	P1	P2	BDAL10 L
	R1	R2	BDAL11 L
	S1	S2	BDAL12 L
Ground	T1	T2	BDAL13 L
	U1	U2	BDAL14 L
+5 Volts	V1	V2	BDAL15 L

3.3 ADDRESSING

All addresses are received from BDALØ and MMU DAL 18-21. The BDAL lines are received thru 2908 transceivers and the MMU DAL lines are received thru 74LS241 bus receivers. The outputs of the bus receivers (DALØ-21) are routed to address latches and card selection logic. DAL 1-7 are routed to an eight bit latch as DAL 8-14. The outputs of these two latches,and the outputs of the refresh address latches are wire-ORed together and routed to the memory array.

DAL 14-21 goes to the address selection logic to determine if an "in range" address is present. If an "in range" address is detected and BS7 is not active, +SEL, is generated and stored in the control latch (74S175). DAL Ø and DAL 15 are also stored in the control latch. The outputs of the control latch (+LSEL, AØ, A15) will be discussed with the timing and control. (Section 3.7).

3.4 DATA

There are 16 data bits on the LSI-11 bus. These are received from BDALØ thru 15. The 2908 bus transceivers contain a transparent latch on each bus receiver output and an edge triggered latch on each bus driver input. These latches are used to latch data into the memory card on a write cycle and data out of the card on a read cycle, therefore no other data latches are required. The latched bus receiver outputs (DAL Ø-15) are used to drive the data inputs of the memory array directly on a write cycle. On a read cycle the data outputs of the memory array are used to drive the bus driver inputs of the 2908 transceivers, and at valid data time, the data is clocked into the bus driver latches.

3.5 PARITY GENERATION AND CHECKING

Each 2908 bus transceiver contains parity generation and checking circuitry over the 4 bits it passes. The parity information is available as an odd parity output from each bus transceiver. The two bits generated over the lower byte (BDAL Ø-7) are exclusive-ORed together and the output is exclusive-ORed with DAL 16 which, when driven active during BDOUT time on a write cycle, causes wrong parity to be generated. The output of this second exclusive-OR gate is stored in memory as even parity over the lower byte. Parity is generated over the upper byte in an identical manner. During a memory read cycle, the bus transceivers generate odd parity over the read data and the parity outputs are passed thru the same circuitry as on a write cycle. The write wrong parity input is disabled, and a third esclusive-OR is used to compare the generated parity data with the stored parity data. Parity is generated over the upper byte in an identical manner and the outpus are ORed together and routed to BDAL 16.

If BDAL 16 is active during a read cycle at data time, a parity error has occured.

3.6 ARBITRATION

The NS23L memory uses 16Kxl dynamic memory chips that must be refreshed every 2ms. This requires that 1 refresh cycle be preformed every 15±1μs to completely refresh the memory is 2ms. Due to the refresh timing being generated asynchronusly with read/write cycles, it is necessary for the memory card to arbitrate between cycles requested from the LSI-11 bus and refresh cycles requested by the internal refresh timer, or external refresh requests if that option is being utilized.

A LM555 timer with a period of 15±1μs is used as the refresh timer; it's output is passed through an AND gate that may be used as an internal refresh disable. The output of the AND gate is passed thru an OR gate which external refresh requests may be supplied if internal refresh is disabled. The output of the OR gate clocks a flip-flop which sets a refresh request that goes to the arbitration circuit.

The path, thru which a cycle requested by the bus reaches the arbitration network, is as follows. The address selection circuitry generates a -SEL, which is stored in the control latch if an "in range" address is present on the LSI-11 bus. The output of this latch, +LSEL, is ANDed with SYNC, DCOK, -REFH, -REFH REQ, BUSY and -R/W to determine if a cycle may be started. This AND gate is the first level of the arbitration. If -REFH or -REFH REQ or -BUSY or -R/W are not present and DCOK and SYNC are present, the BUS CYC flip flop will be set, refresh cycles will be blocked, and a cycle started. If -REFH, -REFH REQ, -BUSY or -R/W is present and the LSI-11 bus requested a cycle the LSI-11 bus must wait until the present cycle is finished and the busy conditions are removed before it can start.

If a refresh cycle is requested during a cycle that was requested by the LSI-11 bus, it is held off by ANDing REFH REQ with the negative output of the BUS CYC flip flop. In the event a refresh cycle is requested at the same time a bus cycle is requested, the bus cycle is given priority over the refresh cycle and the refresh cycle request is saved until the bus cycle is complete.

3.7 TIMING AND CONTROL

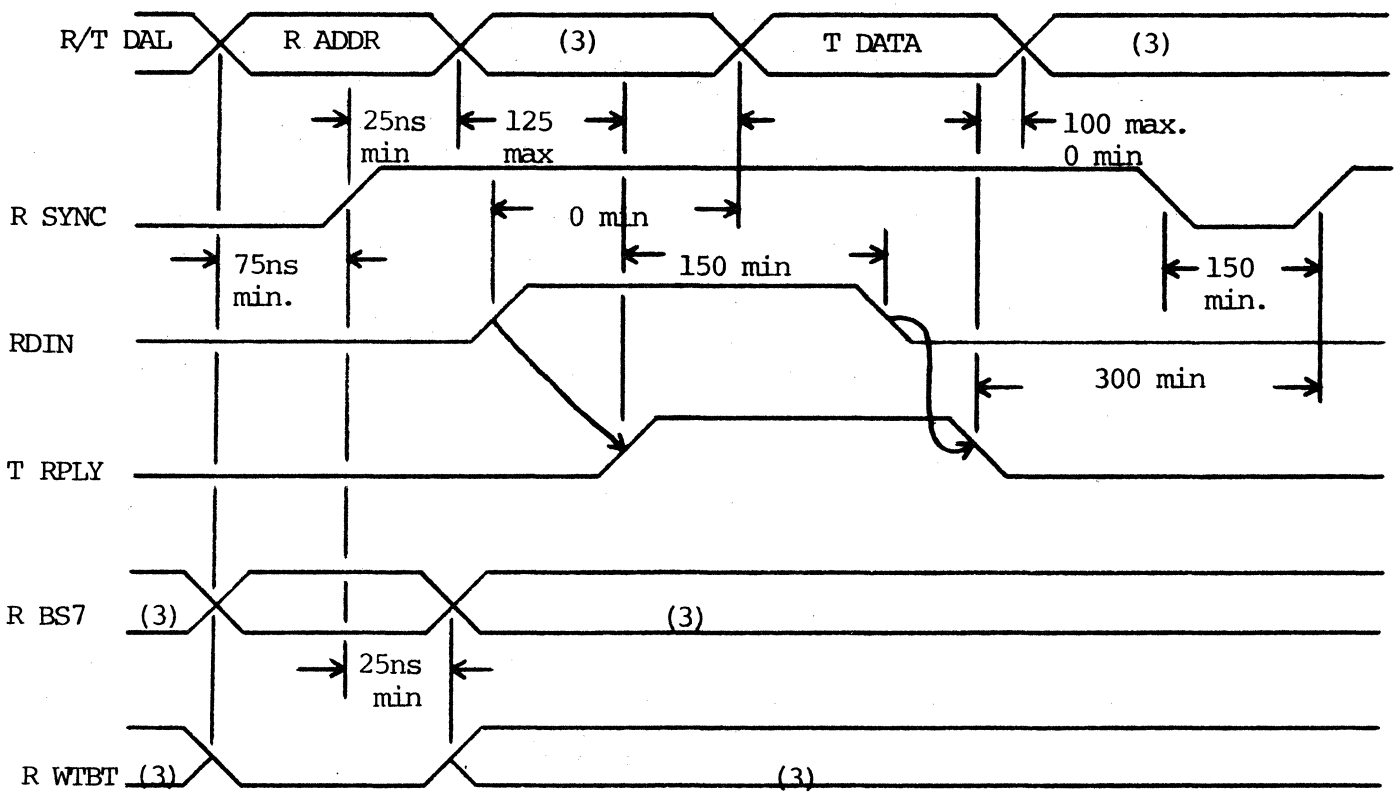
The timing is simply a 200ns delay line fed by a OR function of BUS CYC flip flop, and REFH. flip flop. Appropriate taps are selected for generation of RAS, CAS and address mux. During a refresh cycle, CAS is blocked and a RAS only refresh cycle is performed.

The bus transceivers are controlled by DIN, DOUT and the timing chain. On a write cycle, DOUT is used to latch data into the transceivers latches. During a read cycle DIN is used as the bus driver enable (BE) and DIN ANDed with a tap from the delay line (indicating valid data) is used to latch data into the bus driver latches.

DOUT, in conjuction with WTBT and AØ, is used as write enable (we) to the memory array. If WTBT is active during DOUT time, a byte write is preformed. AØ, which has been latched in the control latch, determines which byte is to be written.

If the bus requests a Read Modify Write (RMW) cycle the memory also performs a RMW cycle on the 16K RAM. This timing and control is handled by using DIN as the bus enable and DOUT as write enable (WE) to the memory array.

All timing to the 32Kx2 bit parity storage array is identical to the memory array timing.



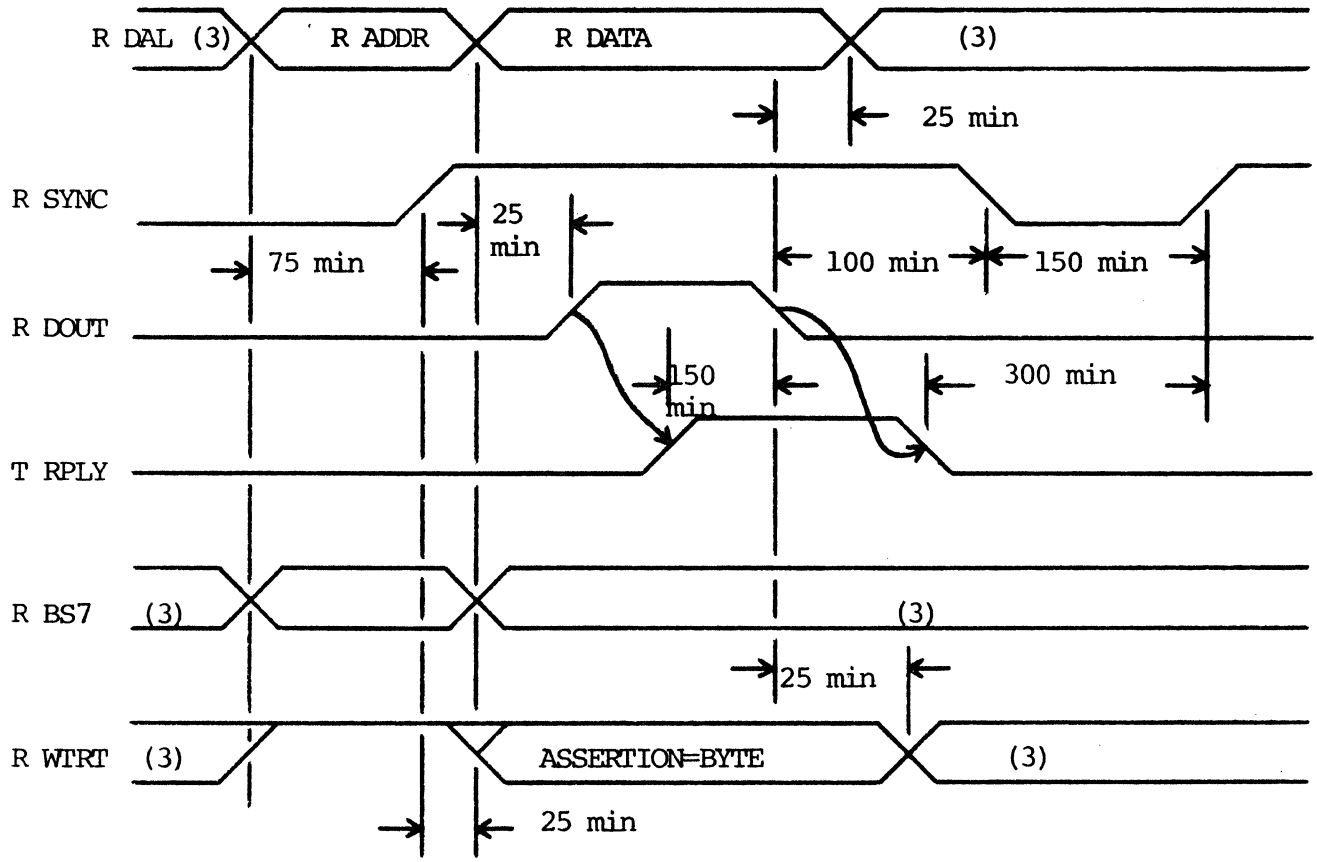
NOTES:

1. Timing shown at Bus Driver Inputs and Bus Receiver Outputs
2. Signal name prefixes are defined below:

   T. Bus Driver Input
   R. Bus Receiver Output

3. Don't care condition
4. All timing given in nanoseconds.

FIGURE 2-1a DATI Bus Cycle Timing (Read Memory)



NOTE:

1. Timing shown at Bus Driver Inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   T. Bus Driver Input
   R. Bus Receiver Output
3. Don't care condition

FIGURE 2-1b DATO or DATOB

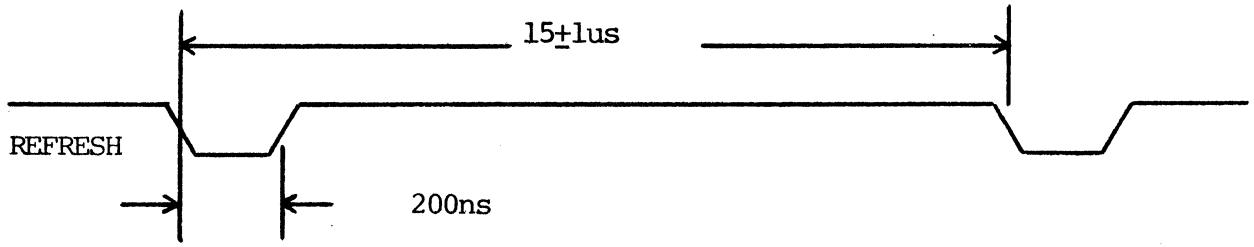
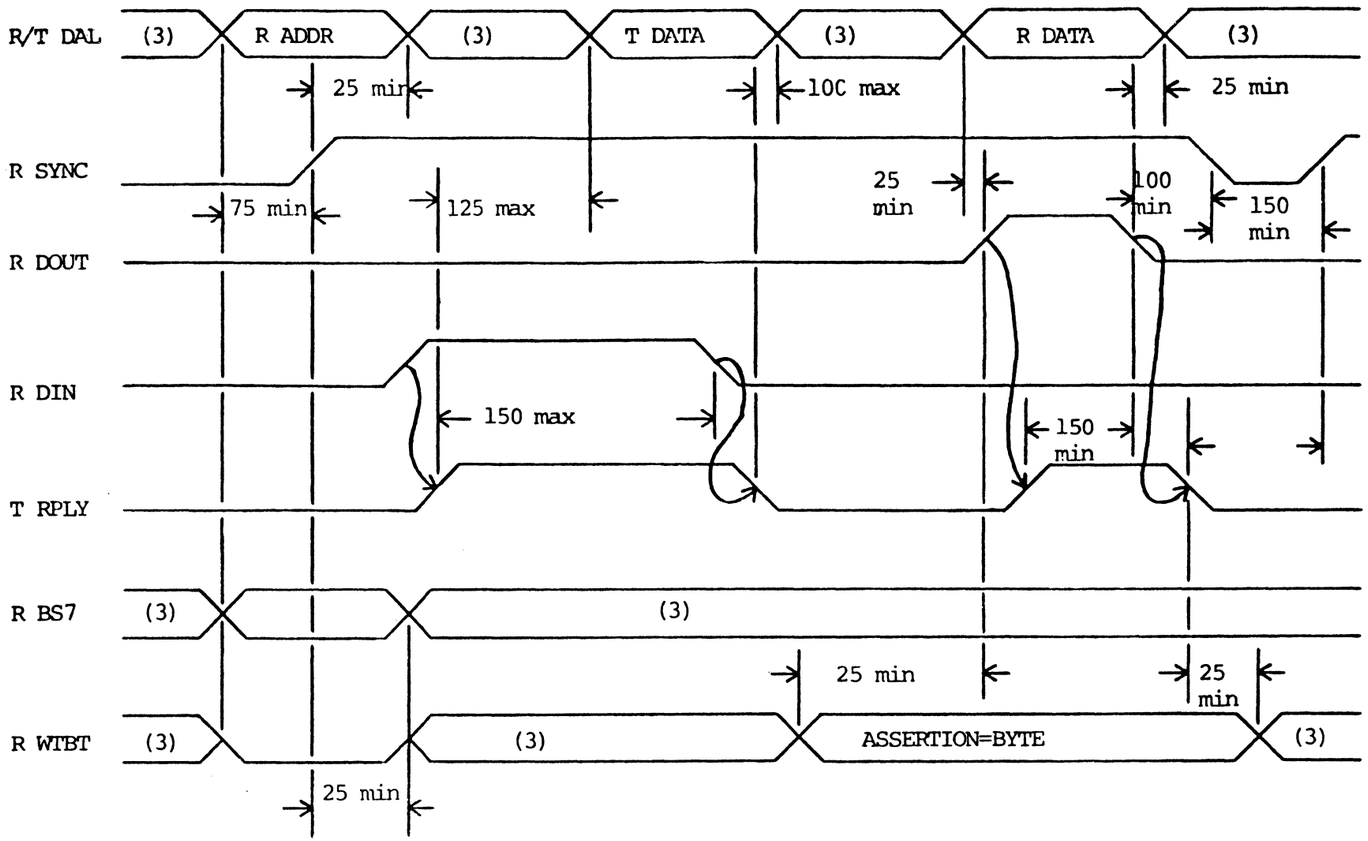


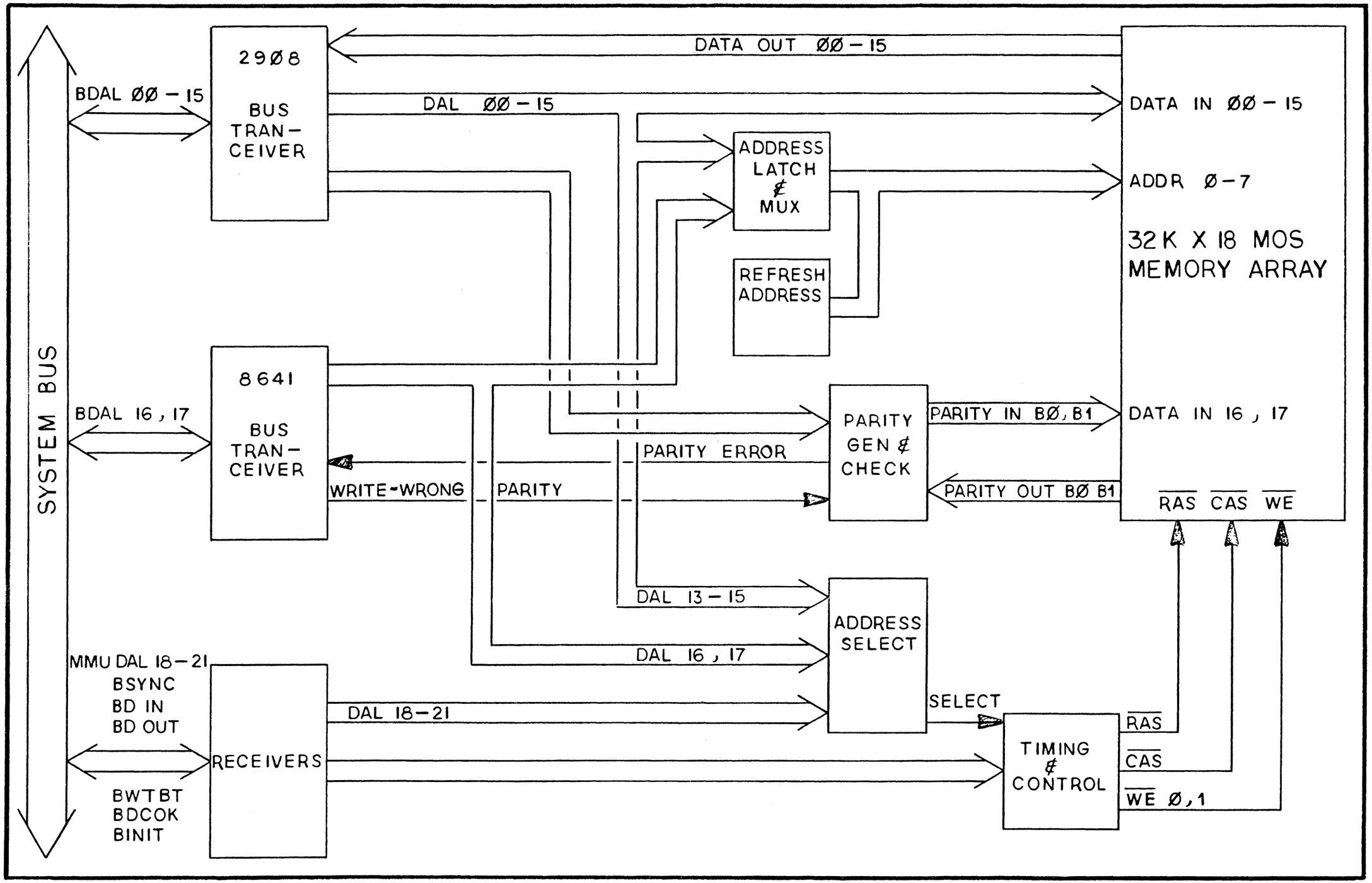
FIGURE 2-2b External Refresh Cycle Timing



NOTE:

1. Timing shown at Bus Driver Inputs and Bus Receiver Outputs
2. Signal name prefixes are defined below:
   - T. Bus Driver Input
   - R. Bus Receiver Output
3. Don't care condition
4. All timings are given in nanoseconds

Figure 2-2a DATIO or DATIOB Bus Cycle Timing


SYSTEM BUS
BDAL ØØ – 15
2908
BUS TRAN– CEIVER
DATA OUT ØØ – 15
DAL ØØ – 15
DATA IN ØØ – 15
ADDRESS LATCH & MUX
ADDR Ø–7
32K X 18 MOS MEMORY ARRAY
REFRESH ADDRESS
8641
BUS TRAN– CEIVER
BDAL 16 , 17
PARITY GEN & CHECK
PARITY IN BØ, B1
DATA IN 16 , 17
PARITY ERROR
WRITE-WRONG
PARITY
PARITY OUT BØ B1
RAS CAS WE
DAL 13 – 15
ADDRESS SELECT
DAL 16 , 17
MMU DAL 18–21
BSYNC
BD IN
BD OUT
BWTBT
BDCOK
BINIT
RECEIVERS
DAL 18–21
SELECT
TIMING & CONTROL
RAS
CAS
WE Ø,1

APPENDIX A

REFERENCE DRAWINGS

This appendix contains the required reference drawings for the NS23L Memory Card.

870103858-001	Schematic
980103858-000	Assembly Drawing
980103858-000	Bill of Materials

VOLTAGE TABLE						
DEVICE TYPE	+12V	+12VB	+5V	+5VB	GND	REFERENCE DESIGNATIONS
DELAY LINE 200 NS					1,14	U39
74LS00			14		7	U43
74S00				14	7	U58
74LS04				14	7	U50
74S08				14	7	U49
74S30				14	7	U64
74S32			14		7	U46
74S37				14	7	U38, U40, U41
74S74				14	7	U55
74LS74				14	7	U56
74S132				14	7	U57
74S135			16		8	U42
74S175			16		8	U48
74LS240				20	10	U67
74LS241				20	10	U63
74S260				14	7	U47
74S283			16		8	U44, U45
74S373				20	10	U51, U52, U53
74LS393				14	7	U54
75452				8	4	U66
LM 555				8	1	U65
LM 3524	15				8	U37
2908			20		5,15	U59, U60, U61, U62
8641				16	8	U68

REVISIONS		
LTR	DATE	DESCRIPTION
A	8-14-80	PCO 24034
B	8-22-80	PCO 24036
C	9-3-80	PCO 24038
D	9-10-80	PCO 24041
E	9-29-80	PCO 24048
F	10-6-80	PCO 24049
G	10-30-80	PCO 24054
H	12-9-80	RELEASE ECO 44158
I	2-24-81	ECO 44171
J	3-24-81	ECO 44205
K	1-8-82	ECO 44347

NOTES: UNLESS OTHERWISE SPECIFIED.

1. CAPACITANCE VALUES IN MICROFARADS, 50V, 10%.
2. RESISTANCE VALUES IN OHMS, 1/8W, 5%.
3. ALL DIODES ARE IN914B.
4. △ DENOTES +5V BATTERY BACKUP.

SPARE GATES

9 U49 8
10 LS08

+12V — AD 2 — W14 — BD 2
+12VB — AS 1 — W15 — W11

BIAKIL — AM 2
BIAKOL — AN 2

BDMGIL — AR 2
BDMGOL — AS 2

U37 LM 3524: 15 VIN; 16 VREF; 2 NI; 1 INV; 6 RT; 7 CT; 3 OSC; 10 SHT DWN; 9 COMP; 8 GND; 12 CA; 11 EA; 13 CB; 14 EB; 4 CL+; 5 CL−

R2 15.4K
R5 5.11K
R4 5.11K
R3 5.11K
R7 2.21K
C32 .1 +80% −20%
C31 .01
C33 .001 100V
R6 51.1K
CR1
CR2
CR3
C34 22 35V 20%
C51 22 35V 20% + .47
C30 47 20V 20%
C2,3,5,7,8,11,12, 14,16,19,20,22, 23,25,27,28 (X16)
+12V (TO ARRAY)

W1
C1,4,6,9,10,13,15, 17,18,21,24,26 (X12) — .47
CR4 IN5817
−5V_IN (TO ARRAY)

+5V — AA 2 — BA 2 — BV 1 — W13 — W10
C52 22 35V 20%
C53 6.8 35V, 20%
C29,35,36,37,40, 44,46,47,48,50 (X10) — .47
+5V (LOGIC & ARRAY)

+5VB (BATTERY BACKUP) — AV 1
C38,39,41,42, 43,49,55 (X7) — .47
+5VB (LOGIC BACKUP)

GROUND — AC 2, AJ 1, AM 1, AT 1, BC 2, BJ 1, BM 1, BT 1
GND

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C55	
CR4	
S1	
R27	R25, R12
RP2	
W16	
U68	

MATERIAL
FINISH
J.C. Jacobs 7-24-80
UNLESS OTHER SPECIFIED
SCHEMATIC DIAGRAM
NS 23 L
TOLERANCE
ANG. 2 PL. 3 PL.
NEXT ASSY USED ON
B 870103858 001
NONE 1 4

REVISIONS			
REV	DATE	ECO NO.	APPVD
		SEE SHEET 1	

SH 3 A +SYNC
SH 4 B DFM PØ
SH 3 C PU 1
SH 4 D DFM P1
SH 3 E +D OUT
SH 4 F DFM Ø–15

DTM PØ S SH 4
DTM P1 T SH 4

AU 2 BDAL Ø
AV 2 BDAL 1
BE 2 BDAL 2
BF 2 BDAL 3
BH 2 BDAL 4
BJ 2 BDAL 5
BK 2 BDAL 6
BL 2 BDAL 7
BM 2 BDAL 8
BN 2 BDAL 9
BP 2 BDAL 10
BR 2 BDAL 11
BS 2 BDAL 12
BT 2 BDAL 13
BU 2 BDAL 14
BV 2 BDAL 15
SH 3 H DRCP
AC 1 BDAL 16
AD 1 BDAL 17

RLE U62 2908 — DAL Ø, DØ, DAL 1, D1, DAL 2, D2, DAL 3, D3
RLE U61 2908 — DAL4, D4, DAL5, D5, DAL6, D6, DAL7, D7
RLE U60 2908 — DAL8, D8, DAL9, D9, DAL 10, D10, DAL 11, D11
RLE U59 2908 — DAL12, D12, DAL13, D13, DAL14, D14, DAL15, D15
U68 8641 △ — DAL16, D16, DAL17, D17
DAL 16

U42 S135 · U43 LS00 · W2 · W3 · W4 · W5

U50 LS04 · U43 LS00 · U48 S175 (ID CK 1Q 1Q̄ 2Q 2Q̄ 3Q 3Q̄ 4Q 4Q̄ CL) · +LSEL U SH 3 · AI5 V SH 3 · LAØ W SH 3

DALØ 13 · U49 △ LS08

DAL 13 DAL 14 DAL 15 DAL 16 DAL 17 DAL 18 DAL 19 DAL 20 DAL 21

U46 S32 · U44 S283 · U45 S283 · W6 · W7 · U47 S260 △

RP2 10K · +5V

S1 · RP1 · +5V · 10K

U54 LS 393 △ (1A 2A 1QA 1QB 1QC 1QD 2QD 1QA 2QA 2QC CL CL)

U52 S373 △ · U53 S373 △ · U51 S373 △ (G OC)

R14 A6 · R20 A5 · R15 A4 · R16 A3 · R18 A2 · R19 A1 · R17 AØ 15

X SH 4 AØ–A6

DAL 1 DAL 2 DAL 3 DAL 4 DAL 5 DAL 6 DAL 7
DAL 8 DAL 9 DAL 10 DAL 11 DAL 12 DAL 13 DAL 14

DAL Ø–15 Y SH 4

SH 3 K BE
SH 3 L DAL 18–21
SH 3 M +BS7
SH 3 J +REFH
SH 3 N RON
SH 3 P RAON
SH 3 R CAON

MATERIAL · FINISH · TOLERANCE ANG. 2 PL .3 PL · UNLESS OTHER SPECIFIED · DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICAL OR APPLIED OR PLATED FINISHES · REMOVE BURRS AND SHARP EDGES BREAK SHARP CORNERS .015 MAX.
NEXT ASSY · USED ON
DR BY J.C. Jacobs 7-24-80 · CHK BY · MFG · ENG · PM
National Semiconductor Corporation
SCHEMATIC DIAGRAM
NS 23 L
SIZE D · DWG NO 870103858 001 · SCALE NONE · SHEET 2 4

SEE SHEET 1

SH 2 W LAØ

+BS7 M SH 2

AP 2 BBS7L
AH 2 BDIN L
AK 2 BWTBTL
AE 2 BD OUT L
AR 1 BREF L
AJ 2 BSYNC L

U67 LS240

R1 15 WE L Z SH 4
R8 15 WE U AA SH 4

U40 S37 · U68 8641 · U41 S37

+REFH J SH 2
+D OUT E SH 2

U57 S132 · R22 100 · C55 100PF

+SYNC
+DCOK
+LSEL

U64 S30

U55 S74

U47 S260 · 75452 U66 · +5VB R27 1K

U39 DELAY LINE IN 200NS 200 20 60 100 120 · R13 100 · U38 S37 · U50 LS04

AT 2 BINIT L
BA 1 BDCOK H
BC 1 BDAL 18
BD 1 BDAL 19
BE 1 BDAL 20
BF 1 BDAL 21

U63 LS241

DAL18
DAL19
DAL20
DAL21

−R/W CYC
−MEM BSY
−REFH
−REFH REQ

U50 L904 · U55 S74 · R9 15 CAS AB SH 4

U41 S37 · R11 15 RAS U AC SH 4

DAL 18−21 L SH 2

R10 15 RAS L AD SH 4

W12 W16 R26 1K +5VB

+5VB R23 27K · R24 68K · C45 100PF · C54 .47 · R21 1K

U65 LM555

W8 W9

U56 LS74

U50 LS04 · U58 S00

RAON P SH 2
DRCP H SH 2
CAON R SH 2
RON N SH 2
PU1 C SH 2

U63 LS241 · U58 S00 · 75452 U66

BRPLY L AF 2

U49 LS08 · U67 LS240

BE K SH 2

+SYNC A SH 2

SH 2 U +LSEL
SH 2 V AI5

U49 LS08 · U43 S00

MATERIAL
FINISH
NEXT ASSY
USED ON
TOLERANCES
UNLESS OTHER SPECIFIED

J.C. Jacobs 7-29-80

SCHEMATIC DIAGRAM
NS 23 L

D 870103858 001
NONE 3 4

REVISIONS

REV	DATE	
		SEE SHEET 1

SH 2 T DTM P1
SH 2 S DTM PØ
SH 3 Z WE L
SH 2 X AØ–A6
SH 3 AC RAS U
SH 3 AA WE U
SH 3 AD RAS L
SH 3 AB CAS
SH 2 Y DAL Ø–15

DFM PØ B SH2
DFM P1 D SH2
DFM Ø–15 F SH2

U8 U7 U6 U5 U4 U3 U2 U1 U9
U17 U16 U15 U14 U13 U12 U11 U10 U18
U26 U25 U24 U23 U22 U21 U20 U19 U27
U35 U34 U33 U32 U31 U30 U29 U28 U36

Pin 5 AØ, 7 A1, 6 A2, 12 A3, 11 A4, 10 A5, 13 A6, 4, 15 RAS; 3 WE; 14 VCC; 2 VSS

U8	Ø	U9	PØ
U7	1	U18	P1
U6	2	U10	15
U5	3	U11	14
U4	4	U12	13
U3	5	U13	12
U2	6	U14	11
U1	7	U15	10
U17	8	U16	9
U26	Ø	U27	PØ
U25	1	U36	P1
U24	2	U28	15
U23	3	U29	14
U22	4	U30	13
U21	5	U31	12
U20	6	U32	11
U19	7	U33	10
U35	8	U34	9

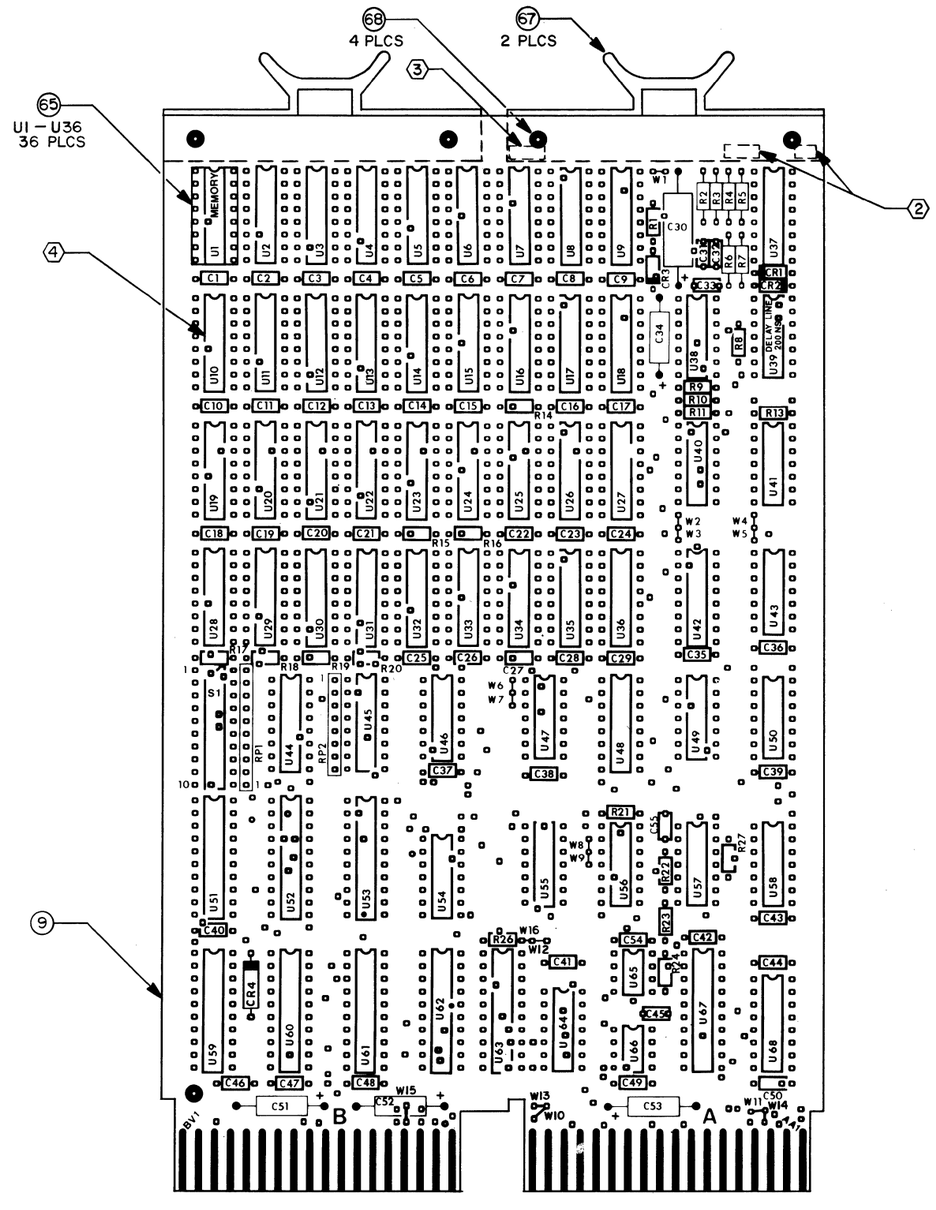
16K RAM (TYP X36)

VBB	1	16	VSS
DI	2	15	CAS
WE	3	14	DO
RAS	4	13	A6
AØ	5	12	A3
A2	6	11	A4
A1	7	10	A5
VDD	8	9	VCC

MATERIAL
FINISH
NEXT ASSY | USED ON
DR J.C. Jacobs 7-24-80
CHK BY
MFG
ENG
PE
UNLESS OTHER SPECIFIED
TOLERANCES
ANG | 2 PL | 3 PL
REMOVE BURRS AND SHARP EDGES

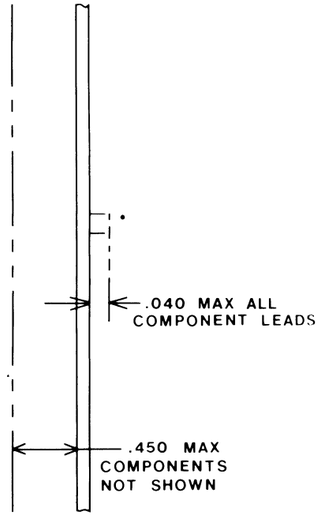
SCHEMATIC DIAGRAM
NS 23 L

SIZE D | CAGE NO 870103858 | 001
SCALE NONE | SHEET 4 OF 4



REVISIONS			
REV	DATE	ECO NO	APPVD
A	8-14-80	PCO 24034	
B	8-22-80	PCO 24036	
C	9-3-80	PCO 24038	
D	9-10-80	PCO 24041	
E	9-22-80	PCO 24048	
F	10-6-80	PCO 24049	
F1	10-13-80	PCO 24053	
B	10-30-80	PCO 24054	
H	12-9-80	RELEASE ECO 44158	
I	2-24-81	ECO 44171	
J	3-24-81	ECO 44205	
K	3-31-81	ECO 44211	
K1	7-24-81	ECO 44261	
L	1-8-82	ECO 44347	

1. ASSEMBLE AND SOLDER PER NSC SPEC. 429306098.
2. MARK ASSY. DASH NO. AND REV. LEVEL WITH .12 – .18 HIGH CHARACTERS WHERE SHOWN.
3. MARK ASSY. S/N WITH .12 – .18 HIGH CHARACTERS WHERE SHOWN.
4. INSTALL MEMORY IC'S ACCORDING TO THE MEMORY ELEMENT POPULATION CHART.
5. INSTALL JUMPERS ACCORDING TO THE TEST CONFIGURATION JUMPER TABLE.
6. AFTER TEST, AND BEFORE FINAL CPU TEST, INSTALL JUMPERS ACCORDING TO THE FACTORY INSTALLED JUMPER TABLE.
7. JUMPERS W2 THRU W5 ARE WIRE WRAP JUMPERS. FIRST INSTALL ITEM 74, THEN INSTALL ITEM 72 USING A WIRE WRAP TOOL.



LAST USED	NOT USED
C55	
CR4	
S1	
R27	R25, R12
RP2	
W16	
U68	

MATERIAL
FINISH
TOLERANCE
ANG | 2 PL | 3 PL
UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
REMOVE BURRS AND SHARP EDGES BREAK SHARP CORNERS .015 MAX

DR H.C. Jacobs 7-24-80
CHK BY
ME
TT
M Galvick 8-14-80

National Semiconductor Corporation
2900 Semiconductor Drive Santa Clara, Calif 95051

PWB ASSEMBLY DRAWING
NS 23L

SIZE D | DR NO 980103858 | 000
SCALE 2:1 | SHEET 1 OF 3

SEE SHEET 1

④ MEMORY ELEMENT POPULATION CHART		
DASH NO.	POPULATE LOCATIONS	REMARKS
-XY0	NONE	NO MEMORY ELEMENTS
-XY1	U1-U36	32 K, PARITY
-XY2	U1-U18	16 K, PARITY
-XY3	U1-U8, U10-U17, U19-U26, U28-U35	32 K, NON-PARITY
-XY4	U1-U8, U10-U17	16 K, NON PARITY

DASH NUMBER CODE-REFERENCE ONLY -XYZ		
X	Y	Z
0 = ITEM 64 CERDIP RAM 5 = ITEM 63 PLASTIC RAM	0 = 128 KW ADDRESSING 1 = 2 MEG. W. ADDRESSING	0 = UNPOPULATED VERSION 1 = 32K WORD, PARITY 2 = 16K WORD, PARITY 3 = 32K WORD, NON-PARITY 4 = 16K WORD, NON-PARITY

⑤ TEST CONFIGURATION JUMPER TABLE	
INSTALLED	REMOVED
W1, W3, W5, W7, W9	W2, W4, W6, W8, W10, W11, W12

MARKETING CONFIGURATION CODE	REFERENCE ONLY - USER SELECTABLE OPTIONS		
	INSTALL	REMOVE	REMARKS
NONE	W9*	W8, W10, W11	INTERNAL REFRESH
X1	W8	W9*	EXTERNAL REFRESH
1X	W10, W11	W13, W14, W15*	BATTERY BACKUP

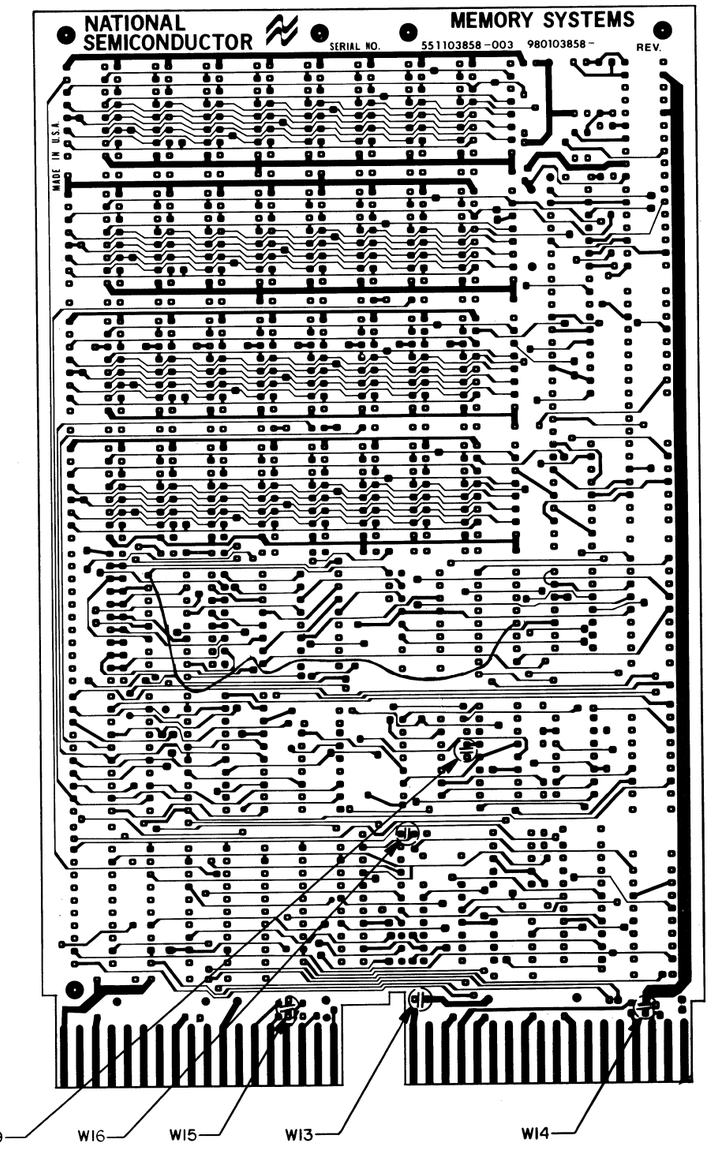
* W9, W13, W14, W15 ARE ORIGINALLY IN ETCH, TO REMOVE, THE SECTION OF ETCH BETWEEN THE FEED-THRUS MUST BE REMOVED AS SHOWN ON SHEET 3. THESE JUMPERS MAY BE REINSTATED BY JUMPERING BETWEEN THE FEED-THRUS.

⑥ FACTORY INSTALLED JUMPER TABLE			
DASH NO.	INSTALLED	REMOVED	NOTES
ALL	W1, W2, W4	W3, W5	
-XY1-XY3	W7	W6	32 KW
-XY2-XY4	W6	W7	16 KW
-X0Z	W16*	W12	128 KW ADDR
-X1Z	W12	W16*	2 MW ADDR

* W16 IS ORIGINALLY IN ETCH

MATERIAL
FINISH
TOLERANCE
ANG 2 PL 3 PL
NEXT ASSY USED ON
S.C. Jacobs 7-24-80
UNLESS OTHER SPECIFIED
PWB ASSEMBLY DRAWING
NS 23 L
D 980103858 000
NONE SHEET 2 OF 3

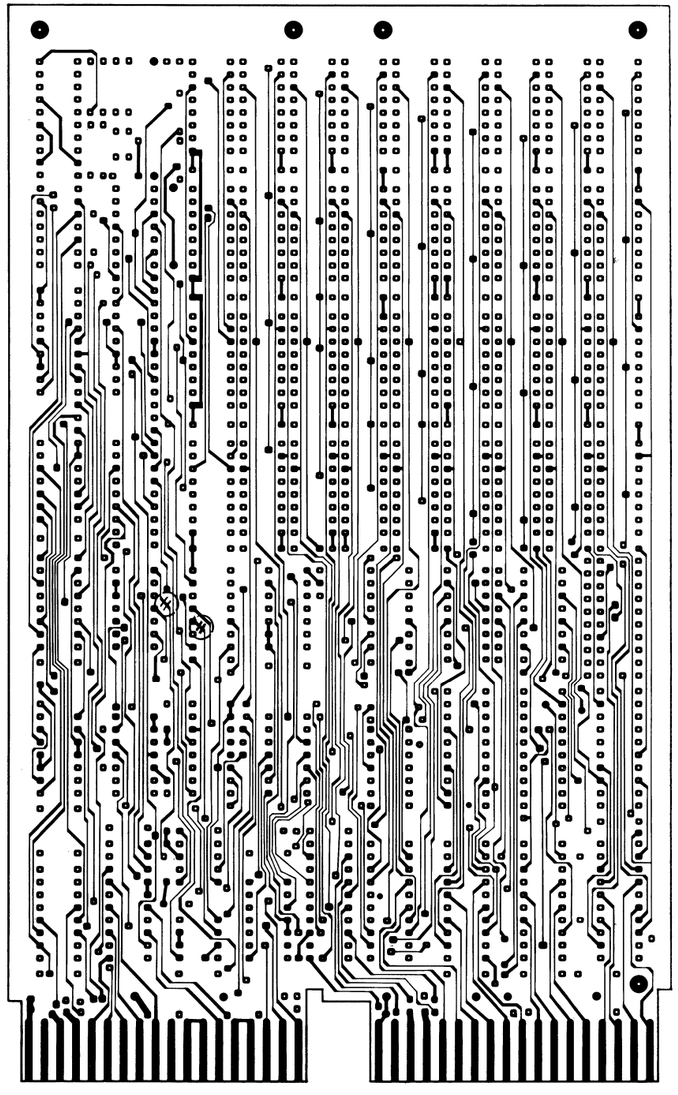
REVISIONS			
REV	DATE	ECO NO	APPVD
		SEE SHEET 1	



COMPONENT SIDE

COMPONENT SIDE

1.ADD JUMPER:
FROM U49-1
TO U49-2
2.ADD JUMPER:
FROM U48-12
TO U44-1



CIRCUIT SIDE

REWORK INSTRUCTIONS SHEET

CIRCUIT SIDE

1.CUT TRACE:
BETWEEN U49-1 AND FEEDTHRU NEAR R24.
2.CUT TRACE:
AT U48-12

MATERIAL	DR K.C. Jacobs 10-6-86	National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara, Calif 95051	
FINISH	CHK BY	PWB ASSEMBLY DRAWING NS23L	
	MFG		
	EE		
	PE		
UNLESS OTHER SPECIFIED		SIZE D	DR NO 980103858 000
TOLERANCE ANG 2 PL 1 PL		SCALE NONE	SHEET 3 OF 3

UNIT OF MEAS = EA : EACH, IN : INCH, FT : FEET, BK : BULK, AR : AS REQ'D

BILL OF MATERIALS NO. 980103858-000

ITEM FIND NO	QUANTITY PER ASSEMBLY	UNIT OF MEAS	PART NUMBER/REFERENCE DOCUMENT	DESCRIPTION	REF DESIGNATOR
1					
2					
3	0		870103858-001	SCHEMATIC DIAGRAM	
4	0		427103858-001	TEST PROCEDURE	
5	0		425103858-001	TEST SPEC	
6	0		426103858-001	PRODUCT SPEC	
7					
8					
9	1	EA	551103858-003	P C BOARD	
10	1	EA	482000354-001	I.C. 74LS00	U43
11	1	EA	482000079-001	I.C. 74S00	U58
12	1	EA	482100785-001	I.C. 74LS04	U50
13	1	EA	482000335-001	I.C. 74S30	U64
14	1	EA	482101026-001	I.C. 74S32	U46
15	3	EA	482100777-001	I.C. 74S37	U38, U40, U41
16	1	EA	482100365-001	I.C. 74LS74	U56
17	1	EA	482000179-001	I.C. 74S74	U55
18	1	EA	482100840-001	I.C. 74S132	U57
19	1	EA	482101174-001	I.C. 74S135	U42
20	1	EA	482000437-001	I.C. 74S175	U48
21	1	EA	482103984-001	I.C. 74LS240	U67
22	1	EA	482107010-001	I.C. 74LS241	U63

ENG CHG	REV	J	K	K1	L	I
	CHG NO	ECO 44205	ECO 44211	ECO 44261	ECO 44347	ECO 44171
	DATE	3-24-81	3-31-81	7-24-81	1-8-82	2-25-81
	APPR					

NOTES:

TITLE: NS 23L

PREPARED BY	CHECKED BY	APPROVED BY
JC Jacobs		
DATE 7-24-80	DATE	DATE 8-14-80

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, Calif. 95051

SIZE A

BILL OF MATERIALS NO. 980103858-000

SH 1 OF 4

UNIT OF MEAS: EA = EACH, IN = INCH, FT = FEET, BK = BULK, AR = AS REQ'D

BILL OF MATERIALS NO. 980103858-000

ITEM FIND NO	QUANTITY PER ASSEMBLY (000)	UNIT OF MEAS	PART NUMBER/REFERENCE DOCUMENT	DESCRIPTION	REF DESIGNATOR
23	1	EA	482101177-001	I.C. 74S260	U47
24	2	EA	482102505-001	I.C. 74S283	U44, U45
25	2	EA	482102641-001	I.C. 74S373	U52, U53
26	1	EA	482102639-001	I.C. 74LS393	U54
27	1	EA	482103971-001	I.C. 75452	U66
28	4	EA	482107001-001	I.C. 2908	U59–U62
29	1	EA	482100770-001	I.C. 74LS08	U49
30	1	EA	482102160-001	I.C. 555	U65
31	1	EA	482104567-002	I.C. 3524	U37
32	1	EA	482103697-001	I.C. 8641	U68
33	1	EA	611102702-200	DELAY LINE 200NS	U39
34	1	EA	513107003-010	SWITCH, DIP 10 POS	S1
35	1	EA	471400807-066	RES, MOD. 8 PIN SIP; 7/10K	RP2
36	1	EA	471401854-002	RES. MOD. 10PIN SIP, 9/10K	RP1
37	3	EA	470101134-063	RES. CC, 1K, 1/8 W, 5%	R21, 26, 27
38	12	EA	470101134-019	RES. CC, 15Ω, 1/8 W, 5%	R1, 8-11, 14-20
39	1	EA	482102641-002	I.C. 74S373	U51
40	2	EA	470101134-039	RES. CC, 100Ω, 1/8W, 5%	R22, R13
41					
42	1	EA	470101134-097	RES. CC, 27K, 1/8W, 5%	R23
43	1	EA	470101134-107	RES. CC, 68K, 1/8 W, 5%	R24
44	3	EA	474102565-073	RES. FILM, 5.11K, 1/8W, 1%	R3, R4, R5

ENG CHG

REV	SEE SHEET 1				
CHG NO					
DATE					
APPR					

NOTES:

TITLE: NS 23 L

PREPARED BY	CHECKED BY	APPROVED BY
JC Jacobs		
DATE 7-24-80	DATE	DATE

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, Calif. 95051

SIZE A | BILL OF MATERIALS NO. 980103858-000 | SH 2 OF 4

UNIT OF MEAS = EA : EACH, IN : INCH, FT : FEET, BK : BULK, AR : AS REQ'D

BILL OF MATERIALS NO. 980103858-000

ITEM FIND NO	QUANTITY PER ASSEMBLY 000	UNIT OF MEAS	PART NUMBER/REFERENCE DOCUMENT	DESCRIPTION	REF DESIGNATOR
45	1	EA	474102565-0388	RES. FILM, 2.21K 1/8W, 1%	R7
46	1	EA	474102565-1186	RES. FILM, 15.4K 1/8W, 1%	R2
47	1	EA	474102565-1666	RES. FILM, 51.1K 1/8W, 1%	R6
48			-		
49			-		
50	3	EA	481000083-001	DIODE, IN914B	CR1, CR2, CR3
51	1	EA	481108530-001	DIODE, IN5817	CR4
52	1	EA	151101308-0377	CAP. CER, .01UF, 100V, 10%	C31
53	1	EA	151000048-001	CAP. CER, .1UF, +80% -20% 50V	C32
54			-		
55	2	EA	150101081-0366	CAP. MICA, 100PF, 500V, 5%	C45, C55
56	1	EA	155100632-0399	CAP. TANT, 6.8UF, 35V, 20%	C53
57	3	EA	155100630-0255	CAP. TANT. 22UF, 15V, 20%	C34, C51, C52
58	1	EA	155100624-0499	CAP. TANT, 47UF, 20V, 20%	C30
59	1	EA	151101308-0255	CAP. CER, .001UF, 100V, +10%	C33
60	45	EA	151104975-0122	CAP. CER, .47UF, 50V, 10%	C1-29, 35-44,
61			-		46-50, 54
62			-		
63	0	EA	482107048-0001	I.C. 16K RAM, PLASTIC	
64	0	EA	482103730-0001	I.C. 16K, RAM, 190NS	
65	36	EA	214102685-0033	SOCKET, DIL, 16 PIN	U1-U36
66			-		

ENG CHG

REV	SEE SHEET1				
CHG NO					
DATE					
APPR					

NOTES:

TITLE: NS 23 L

PREPARED BY	CHECKED BY	APPROVED BY
J.C. Jacobs		
DATE 7-24-80	DATE	DATE

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, Calif. 95051

SIZE A

BILL OF MATERIALS NO. 980103858-000

SH 3 OF 4

UNIT OF MEAS: EA = EACH, IN = INCH, FT = FEET, BK = BULK, AR = AS REQ'D

BILL OF MATERIALS NO. 980103858-000

ITEM FIND NO	QUANTITY PER ASSEMBLY 000	UNIT OF MEAS	PART NUMBER/REFERENCE DOCUMENT	DESCRIPTION	REF DESIGNATOR
67	2	EA	7401010100 6-001	HANDLE	
68	4	EA	2831011300 3-003	RIVET, 1/8 x 3/16	
69					
70	.1	FT	6001001551 5-005	Wire, PVC, 24 AWG	W1, W6-W11, W13,
71					W14, W15
72	.1	FT	6001001581 5-005	Wire, PVC, 30 AWG	W2-W5
73					
74	6	EA	2831020191 9-001	Posts, Wire Wrap	W2-W5
75					
76					
77					
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87					
88					

ENG CHG					
REV	SEE SHEET 1				
CHG NO					
DATE					
APPR					

NOTES:

TITLE: NS 23 L

PREPARED BY	CHECKED BY	APPROVED BY
J.C. [illegible]		
DATE 7-24-80	DATE	DATE

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, Calif. 95051

SIZE A | BILL OF MATERIALS NO. 980103858-000 | SH 4 OF 4