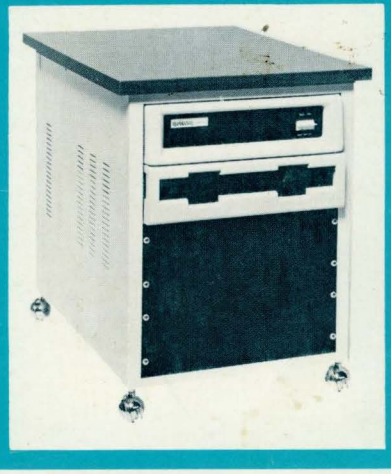
netcom products, inc.

REPRESENTED.....
DISTRIBUTED BY
ROHR ASSOCIATES
P. O. Box 27040
Philadelphia, PA 19118
(215) 836-2200

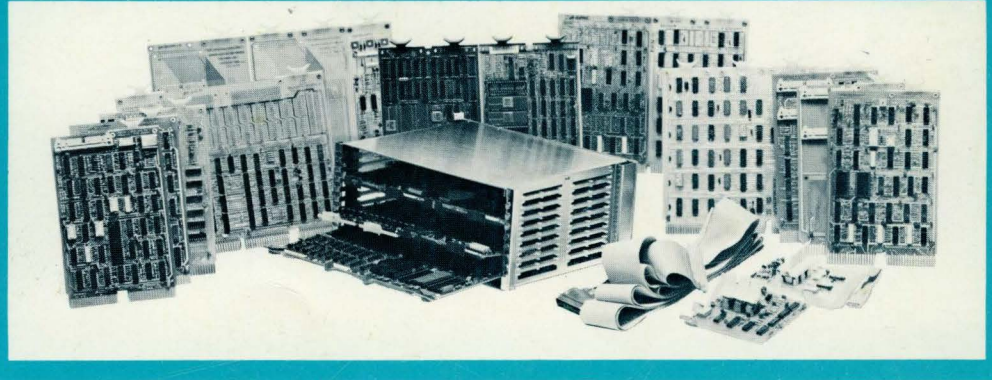
NDRV-11B PARALLEL DMA INTERFACE

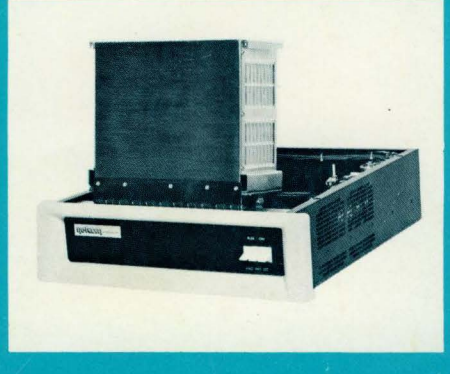
LSI-11* SYSTEM BUILDING OPTIONS

systems

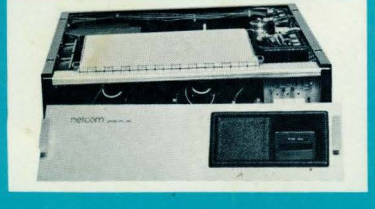


modules





enclosures



*TM — Digital Equipment Corporation

netcom products, inc. • 430 Toyama Drive • Sunnyvale, CA 94086 • (408) 734-8732

NDRV-11B PARALLEL DMA INTERFACE

DP 7620052 7/80

TABLE OF CONTENTS

INDEX OF FIGURES

INDEX OF TABLES

NDRV-11B

USER'S GUIDE

1.0 GENERAL DESCRIPTION

The NDRV-11B is a general purpose DMA I/O board designed to directly transfer data between an I/O device and the LSI-11 system memory.

The processor must program the NDRV-11B to transfer a specified number of 8- or 16-bit words to or from specified memory locations. Once the transfer is initiated, no further processor intervention is required. The NDRV-11B can transfer up to 250K 16-bit words per second in single cycle mode and up to 500K 16-bit words per second in burst mode. The sequence structure also allows read-modify-restore operations.

1.1 FEATURES

- Compatible with Digital Equipment Corporation's DRV11-B DMA Interface
- Compatible with LSI-11 bus
- Buffered input/output data
- 3 User defined status lines
- 3 User defined function bits
- 16 bit CSR available for control and status
- Transfer of up to 32K of 16-bit words
- Two 40 pin I/O connectors mounted on module for interface with users hardware
- Switch selectable device address and interrupt vector
- Transfer rate of up to 500K 16-bit words per second in burst mode

2.0 CONFIGURATION

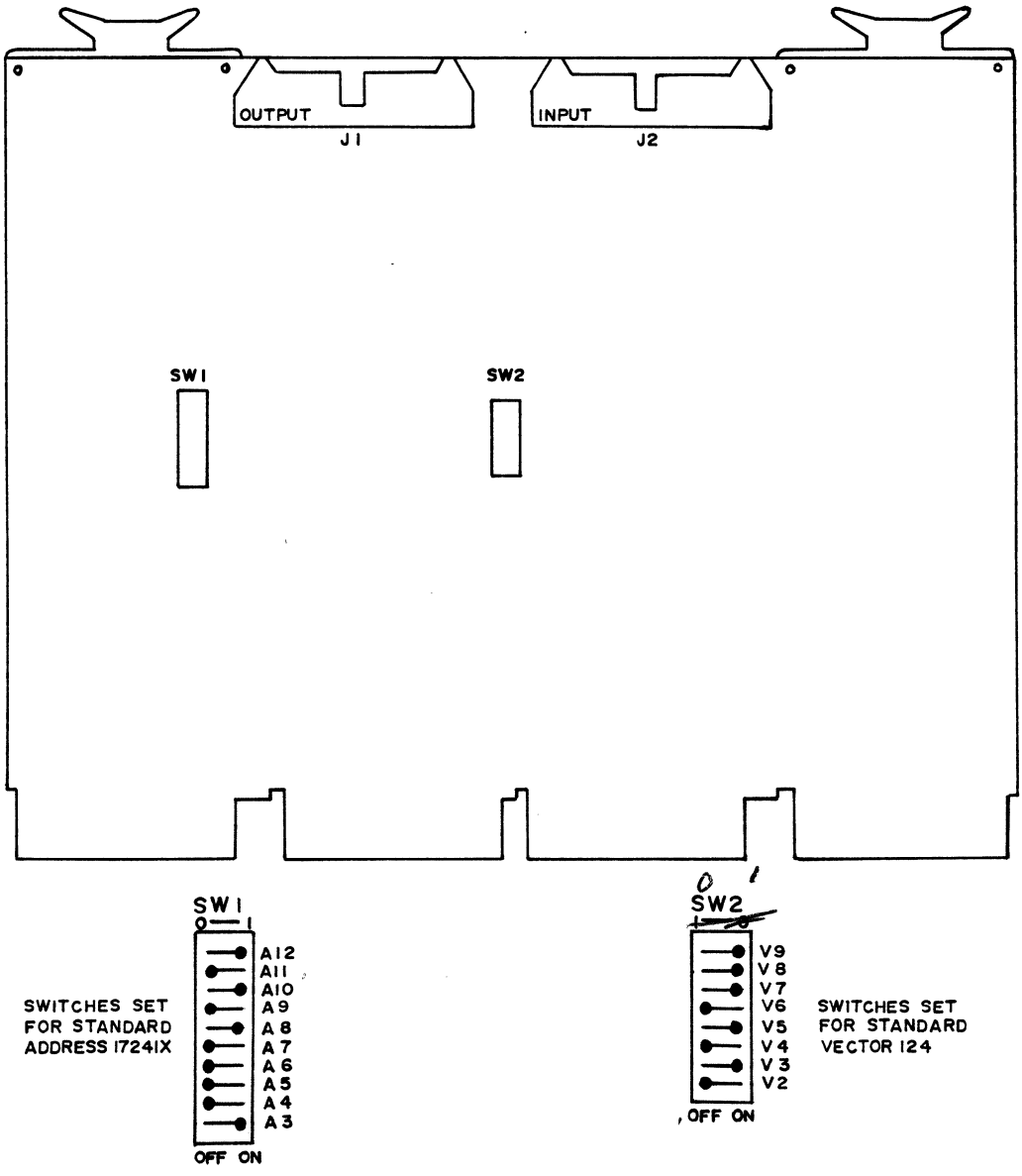
The NDRV-11B has five registers: Word Count Register (WCR); Bus Address Register (BAR); Control Status Register (CSR); Input Data Buffer Register (IBUF);

and Output Data Buffer Register (OBUF). It also has bus transceivers, I/O buffers, and logic for address control, interrupt request, and DMA requests and sequencing.

Two switches on the NDRV-11B are used to configure the board address and vector. SW1 configures the address and SW2 the vector.

2.1 SWITCHES

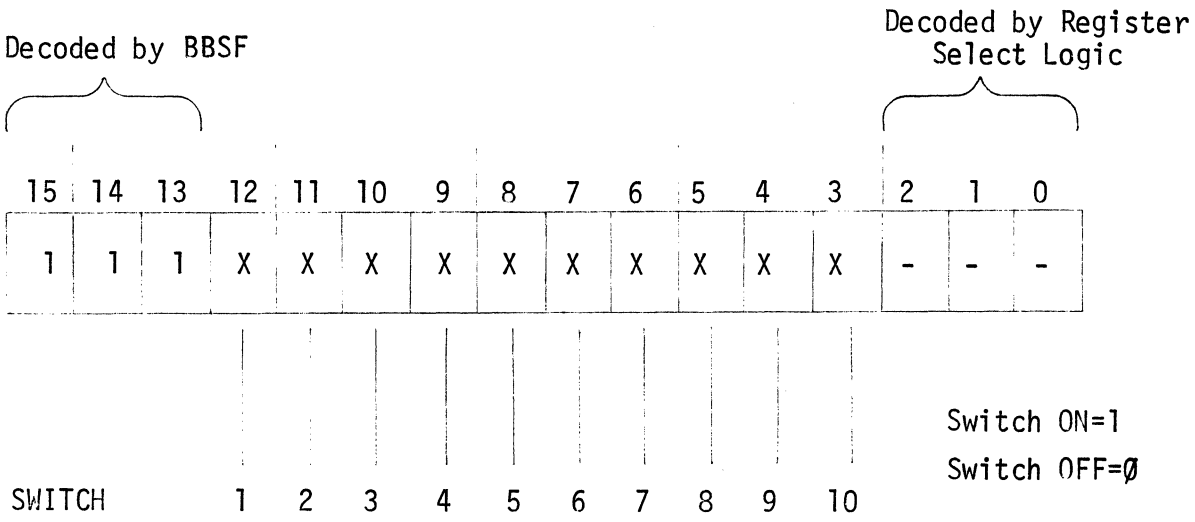
Figure 1 shows the switch locations and Figure 2 shows the relationship between the address and vector formats and the switch locations. The switches are set to the OFF position (OPEN) to select a zero bit, and the ON position (CLOSED) to select a one bit for the address. The switches are set to the ON position (CLOSED) to select a zero bit, and the OFF position (OPEN) to select a one bit for the vector.



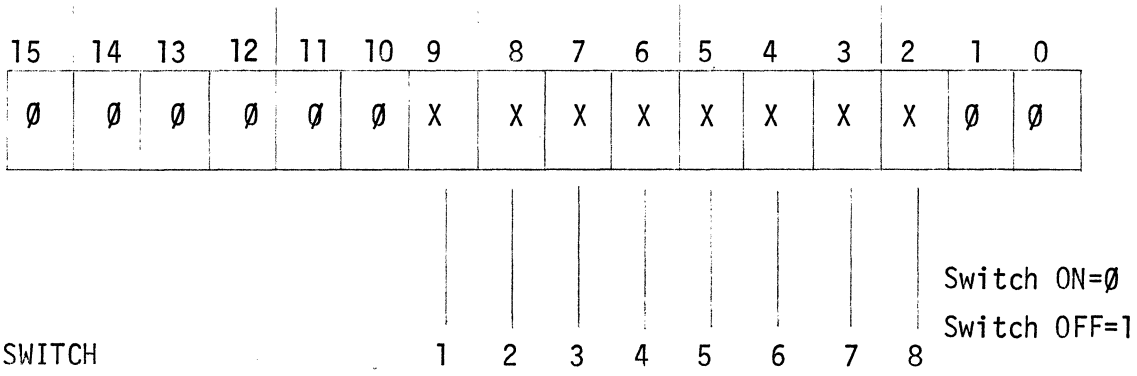
Device Address

Vector Address

FIGURE 1. ADDRESS SWITCH LOCATION



Device Address Selection Switch SW 1



Interrupt Vector Selection Switch SW 2

FIGURE 2. SWITCH ASSIGNMENTS FOR ADDRESS AND VECTOR

2.2 DEVICE ADDRESS FORMAT

The NDRV-11B decodes four addresses, one for each of the registers (except 1XXXX6 which is an IBUF on a DATI cycle and an OBUF on a DATO cycle). The registers and addresses are listed below:

REGISTER	OCTAL ADDRESS
WCR	1XXXX0
BAR	1XXXX2
CSR	1XXXX4
IBUF/OBUF	1XXXX6

Switches SW1-1 through SW1-10 select the base address as indicated by the X in the octal address, and the individual registers are decoded by the DMA board according to the state of bits 01 and 02. The addresses assigned to the NDRV-11B normally start at 172410_8 and progress upward. The standard addresses are shown in Table 1.

Table 1. Standard Addresses

DESCRIPTION	MEMONIC	READ/WRITE	STANDARD ADDRESS
REGISTER			
WORD COUNT	WCR	R/W	172410
BUS ADDRESS	BAR	R/W	172412
CONTROL/STATUS	CSR	R/W	172414
INPUT DATA BUFFER	IBUF	R	172416
OUTPUT DATA BUFFER	OBUF	W	172416
INTERRUPT			
INTERRUPT VECTOR			124

2.3 INTERRUPT VECTOR SELECTION

When the NDRV-11B requests an interrupt, the processor responds by asserting BDIN then BIAKO, which is received by the NDRV-11B as BIAKI. The NDRV-11B then places a vector on the BDAL lines and asserts BRPLY. After the interrupt cycle is terminated, the processor uses the vector to point to a service program.

The vector for the NDRV-11B is switch selectable via SW2 (see Figure 2). The switches control the vector data placed on BDAL lines 2 through 9.

2.4 REGISTERS

The NDRV-11B has five registers, each of which is addressable by the processor. The BAR, WCR, and CSR are read/write registers while the IBUF is a read-only and the OBUF a write-only register.

2.4.1 WORD COUNT REGISTER (WCR)

The WCR (see Figure 3) is a 16-bit read/write counter that controls the number of DMA transfers. Under program control, this register is loaded with the 2's compliment of the number of words or bytes to be transferred between memory and the I/O device at one time. At the end of each transfer, the WCR is incremented. When the contents of the WCR are incremented to zero, (all 16 bits = 0), the transfers are terminated, READY is set, and if enabled, an interrupt is requested. The WCR is word-addressable only.

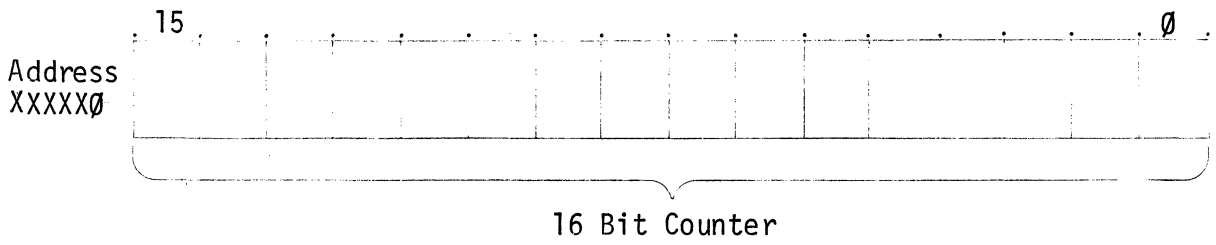


FIGURE 3. WORD COUNT REGISTER

2.4.2 BUS ADDRESS REGISTER (BAR)

The BAR (see Figure 4) is a 16-bit read/write register used to generate the bus address that specifies the memory location to or from which data is transferred. Fifteen of the sixteen bits are loaded under program control. Bit zero is controlled by the user device through the input data/control buffer. The BAR is incremented after each transfer and can be incremented across 32K memory boundaries via the extended address bits provided on the NDRV-11B. If the system has only 16 address bits, the NDRV-11B will "wrap-around" to location zero when the extended address bits are incremented. The BAR is word-addressable only.

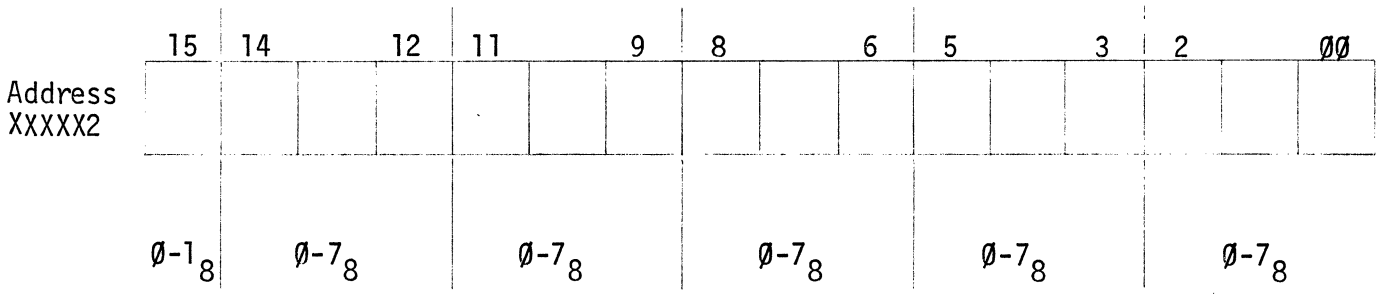


FIGURE 4. BUS ADDRESS REGISTER

2.4.3 CONTROL/STATUS REGISTER (CSR)

The CSR (see Figure 5) is a 16-bit read/write register used to control DMA transfers and provide status information to the processor under program control. It is both byte- and word-addressable. Bit Ø is a write-only bit and is always read as zero. Bits Ø-6, 8, and 12 are read/write bits while bits 7, 9-11 and 13-15 are read-only bits. Bit 14 can be written to a zero. See Table 2 for functional description of the operation of the individual bits.

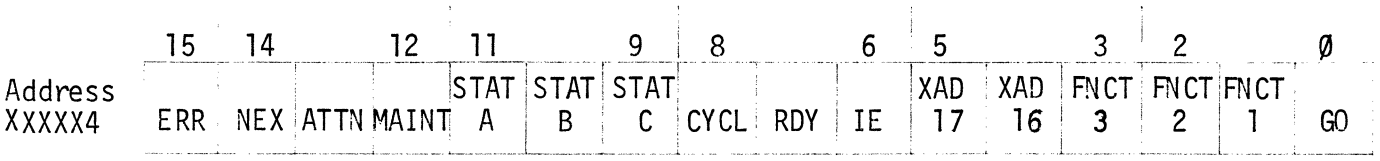


FIGURE 5. CONTROL/STATUS REGISTER

Table 2. Control/Status Register Bit Function Description

BIT	NAME	DESCRIPTION
15	Error (Read-Only)	1. Indicates a special condition. a. NEX (bit 14) b. ATTN (bit 13) 2. Sets READY (bit 7) and causes interrupt if IE (bit 6) is set. 3. Cleared by removing the special condition. a. NEX is cleared by writing to zero. b. ATTN is cleared by the user device.
14	NEX	1. Non-existent memory indicates that as bus master, the NDRV-11B did not receive BRPLY or that a DATIO cycle was not completed. 2. Sets error (bit 15). 3. Cleared by INIT or by writing to zero.
13	ATTN (Ready/Only)	1. Indicates the state of the ATTN user signal. 2. Sets error (bit 15).
12	MAINT (Read/Write)	Maintenance bit used with diagnostic program.
11	STAT A (Read-only)	1. Device status bits that indicate the state of the STATUS A, B, AND C USER signals. 2. Set and cleared by user control only.
10	STAT B (Read-only)	
9	STAT C (Read-only)	
8	CYCLE (Read-Write)	Cycle is used to prime a DMA bus cycle.

Table 2. Control/Status Register Bit Function Description, con't.

BIT	NAME	DESCRIPTION
7	READY (Read-only	1. Indicates that the NDRV-11B is able to accept a new command. Requests an interrupt if IE (bit 6) is set. 2. Set by INIT.
6	IE (Read/Write)	1. Enables interrupts to occur when READY is set. 2. Cleared by INIT.
5	XAD 17 (Read/Write)	Extended address bit 17; cleared by INIT.
4	XAD 16 (Read/Write)	Extended address bit 16; cleared by INIT.
3	FNCT 3 (Read/Write)	1. Three bits made available to user device. User-defined. 2. Cleared by INIT.
2	FNCT 2 (Read/Write)	
1	FNCT 1 (Read/Write)	
0	GO (Write-only)	Causes "NOT READY" to be sent to the user device indicating a command has been issued. Clears READY (bit 7). Enables DMA transfers.

2.4.4 INPUT DATA BUFFER REGISTER (IBUF)

The IBUF (Figure 6) is a 16-bit read-only register used to transfer data from the user's device. Data is loaded into the IBUF by the user's device and then transferred to memory under DMA control by the NDRV-11B, or under program control by the processor as either a 16-bit word, an 8-bit high byte or an 8-bit low byte. The IBUF interfaces to the user device via J2.

Both the input and output registers respond to the same address, but the IBUF responds to a read operation and the OBUF responds to a write operation.

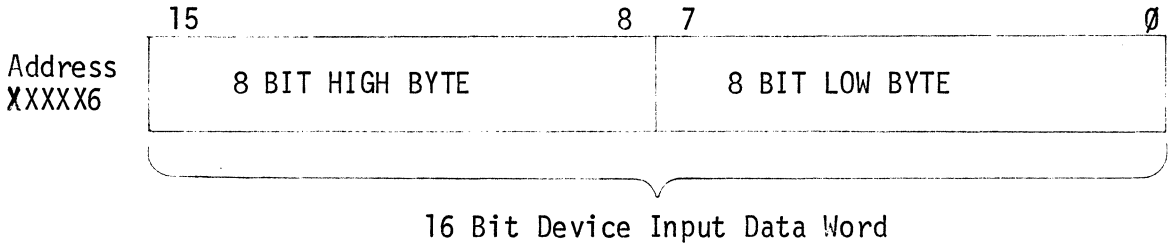


FIGURE 6. INPUT DATA BUFFER REGISTER

2.4.5 OUTPUT DATA BUFFER REGISTER (OBUF)

The OBUF (Figure 7) is a 16-bit write-only register used to transfer data to the user's device. Data from memory is loaded into the OBUF under DMA control by the NDRV-11B or under program control by the processor so that it can be read by the user's device. The OBUF can be loaded with a 16-bit word, an 8-bit high byte, or an 8-bit low byte. The OBUF interfaces the user's device via J1.

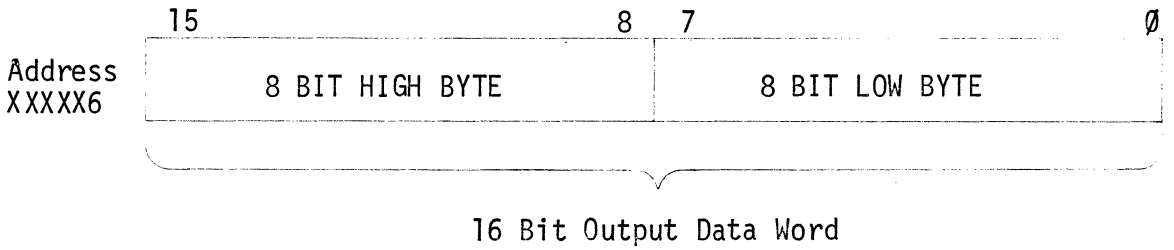


FIGURE 7. OUTPUT DATA BUFFER REGISTER

2.5 CABLE CONNECTORS

The NDRV-11B has two 40-pin connectors used to interface with the user's device. One connector is associated with input functions and the other with ouput functions. Table 3 lists the input connector (J2) signals and Table 4 lists the output connector (J1) signals.

TABLE 3. NDRV-11B Input Connector Signals

J2 CONNECTOR PIN	SIGNAL NAME	UNIT LOADS*	SIGNAL DESCRIPTION
1	IN 15 H	1	Data Input
3	IN 14 H	1	Data Input
5	IN 13 H	1	Data Input
7	IN 12 H	1	Data Input
9	IN 11 H	1	Data Input
11	IN 1Ø H	1	Data Input
13	IN 9 H	1	Data Input
15	IN 8 H	1	Data Input
16	IN 7 H	1	Data Input
14	IN 6 H	1	Data Input
12	IN 5 H	1	Data Input
1Ø	IN 4 H	1	Data Input
8	IN 3 H	1	Data Input
6	IN 2 H	1	Data Input
4	IN 1 H	1	Data Input
2	IN Ø H	1	Data Input
23	FNCT 1 H	1Ø (DRIVE)	User Defined to Control Device Functions
27	FNCT 2 H	1Ø (DRIVE)	User Defined to Control Device Functions
31, 32	FNCT 3 H	1Ø (DRIVE)	User Defined to Control Device Functions
25	C1 H	1	Control for Transfer Cycle Type
29	CØ H	1	Control for Transfer Cycle Type
33	BA INC ENB H	1	Allows Bus Address to Increment

*UNIT LOAD = 40 microamps in the HIGH state (logic "1")
1.6ma in the LOW state (logic "Ø")

Table 3. NDRV-11B Input Connector Signals, con't.

J2 CONNECTOR PIN	SIGNAL NAME	UNIT LOADS*	SIGNAL DESCRIPTION
35	AØØ H	1	Controls Bit Ø of Bus Address Register
37	ATTN H	1	Terminates DMA Transfers
39	$\overline{\text{BUSY}}$ H	1Ø (DRIVE)	Low Indicates Transfer in Progress
17	GND		
18	GND		
19	GND		
20	GND		
21	GND		
22	GND		
24	GND		
26	GND		
28	GND		
30	GND		
34	GND		
36	GND		
38	GND		
40	GND		

*UNIT LOAD = 40 microamps in the HIGH state (logic "1")
1.6ma in the LOW state (logic "Ø")

Table 4. NDRV-11B Output Connector Signals

J1 CONNECTOR PIN	SIGNAL NAME	UNIT LOADS*	SIGNAL DESCRIPTION
1	OUT 15 H	1Ø (DRIVE)	Data Output
3	OUT 14 H	1Ø (DRIVE)	Data Output
5	OUT 13 H	1Ø (DRIVE)	Data Output
7	OUT 12 H	1Ø (DRIVE)	Data Output
9	OUT 11 H	1Ø (DRIVE)	Data Output
11	OUT 1Ø H	1Ø (DRIVE)	Data Output
13	OUT 9 H	1Ø (DRIVE)	Data Output
15	OUT 8 H	1Ø (DRIVE)	Data Output
16	OUT 7 H	1Ø (DRIVE)	Data Output
14	OUT 6 H	1Ø (DRIVE)	Data Output
12	OUT 5 H	1Ø (DRIVE)	Data Output
1Ø	OUT 4 H	1Ø (DRIVE)	Data Output
8	OUT 3 H	1Ø (DRIVE)	Data Output
6	OUT 2 H	1Ø (DRIVE)	Data Output
4	OUT 1 H	1Ø (DRIVE)	Data Output
2	OUT Ø H	1Ø (DRIVE)	Data Output
23, 25	STATUS C H	1	User Defined to Receive Device Status
27	STATUS B H	1	User Defined to Receive Device Status
31	STATUS A H	1	User Defined to Receive Device Status
29	INIT H	1Ø (DRIVE)	Used to Initialize User's Device
33	WC INC ENB H	1	Allows Word Count to Increment
35	READY H	1Ø (DRIVE)	Indicates User Device May Initiate DMA Transfer

*1 UNIT LOAD = 40 microamps in the HIGH state (logic "1")
1.6ma in the LOW state (logic "Ø")

Table 4. NDRV-11B Output Connector Signals, con't.

J1 CONNECTOR PIN	SIGNAL NAME	UNIT LOADS*	SIGNAL DESCRIPTION
37	INIT V2 H	1Ø (DRIVE)	Alternate Initialization Signal
39	CYCLE REQUEST H	1	Initiates DMA Request
32	SINGLE CYCLE H	1	Controls Burst Mode Operation
17	GND		
18	GND		
19	GND		
20	GND		
21	GND		
22	GND		
24	GND		
26	GND		
28	GND		
30	GND		
34	GND		
36	GND		
38	GND		
40	GND		

*1 UNIT LOAD = 40 microamps in the HIGH state (logic "1")
1.6ma in the LOW state (logic "Ø")

3.0 FUNCTIONAL DESCRIPTION

This section describes the NDRV-11B bus operations and control lines required for DMA transfers and DMA transfer timing. A block diagram of the NDRV-11B is shown in Figure 8. The registers were discussed in the REGISTERS Section.

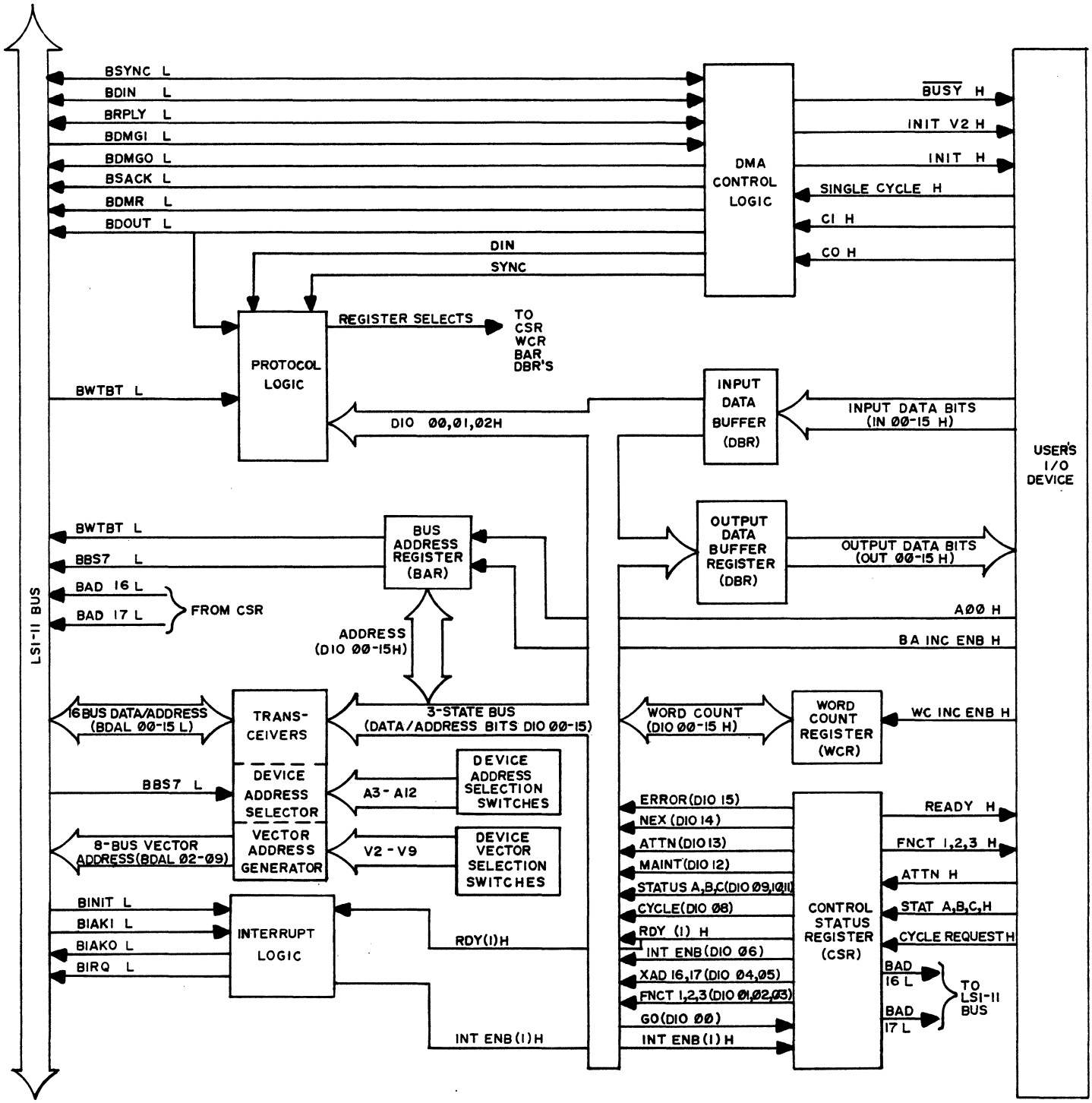


FIGURE 8. LOGIC BLOCK DIAGRAM

3.1 PROGRAMMING

The NDRV-11B can operate as either a slave or master device. When the NDRV-11B is not in control of the bus, all data transfers out (DATO, DATOB) and all data transfers in (DATI, DATIB) are in respect to the processor. Once bus mastership is granted to the NDRV-11B by the processor, all data transfers are in respect to the NDRV-11B until bus mastership is released.

3.1.1 PROGRAM CONTROL TRANSFERS

Data transfers may be performed under program control by addressing the IBUF or OBUF and reading or writing data respectively. One might use the function and status bits to control the passage of data in this mode.

3.1.2 DMA Control Transfers

The NDRV-11B interface is constructed so that DMA transfers can be accomplished in one of two ways. The NDRV-11B is always initialized for DMA transfer by having the processor load the BAR, WCR, and CSR. The CSR must have the GO bit (bit ØØ) set to a 1. This sets the READY line. The user's I/O device can respond by asserting the CYCLE REQUEST for a minimum of one microsecond to initiate a DMA transfer, or under program control, the processor can write a 1 into the CYCLE bit (bit 8) of the CSR at the same time it sets the GO bit. For convenience, only the user-initiated cycle (started by asserting CYCLE REQUEST) will be discussed. The DMA cycle is the same when initiated by CYCLE except for the start.

NDRV-11B DMA operation is initialized under program control by loading the following information into the stated registers: the 2's compliment of the number of words to be transferred goes into the WCR; the BAR is loaded with the first address of the memory location from or to which data is to be transferred; and the CSR is loaded with the desired control bits including

a 1 in bit ØØ. Data transfers are under control of the DMA logic after the NDRV-11B has been initialized.

DMA data input (DATI) or output (DATO) transfers can occur after the processor clears READY H by writing a 1 into bit ØØ of the CSR. When the user's I/O device is ready for a DMA cycle, it presents the control bits [bus address increment enable (BA INC ENB), word count increment enable (WC INC ENB), C1 and CØ (defines cycle type), AØØ and ATTN] to the NDRV-11B (see Table 5). Then it asserts CYCLE REQUEST H to gain use of the LSI-11 bus. When CYCLE REQUEST is asserted, the control bits are latched into the NDRV-11B DMA control logic and busy goes low.

If it is a DATO cycle (NDRV-11B to memory transfer), the input data is latched into the IBUF when CYCLE REQUEST H is asserted. If the transfer is a DATI cycle (memory to NDRV-11B), the output data is latched into the OBUF at the end of the bus cycle.

A DATO or DATI cycle is performed directly to or from the memory location specified by the BAR when the NDRV-11B is bus master. At the end of each cycle, the WCR and BAR are incremented (if WC INC ENB and BA INC ENB are high as they would be in a word transfer), $\overline{\text{BUSY}}$ goes high and READY remains low. A second DATO or DATI cycle is initiated when the user's I/O device again asserts CYCLE REQUEST. DMA transfers will continue until the WCR increments to zero, at which time READY goes high. The NDRV-11B will generate an interrupt to the processor at this time if interrupt enable is set.

Only one CYCLE REQUEST is needed for the complete transfer of the specified number of data words if burst mode is selected (SINGLE CYCLE H low). In the normal mode (SINGLE CYCLE H high), bus control is returned to the processor between transfers.

3.2 TYPE OF I/O TO BE PERFORMED

The user must select the type of I/O. (DATO, DATOB, DATI, DATIO) to be performed by asserting CØ and C1 as follows:

CØ	C1	TYPE OF CYCLE
Ø	Ø	DATI
1	Ø	DATIO
Ø	1	DATO
1	1	DATOB

If byte transfers are performed, the byte address bit (AØØ) and the BA INC ENB line must be manipulated by the user. The WC INC ENB line must be manipulated also depending on whether the user is counting words or bytes being transferred.

Table 5. Description of I/O Connector Lines

MNEMONIC	DESCRIPTION
OUT ØØ-OUT 15	16 TTL output lines from the NDRV-11B to the user's I/O device. These lines contain the same data as that in the OBUF. One=High.
IN ØØ-IN 15	16 TTL input lines to the NDRV-11B from the user's I/O device. These 16 lines input data to the IBUF. One=High.
STATUS A,B,C,	Three TTL status input lines to the NDRV-11B from the user's I/O device. The function of these lines is defined by the user.
FNCT 1,2,3	Three TTL output lines to the user's I/O device from the NDRV-11B. While the function of these lines is defined by the user, FNCT 2 will assert INIT V2 when it is asserted.
INIT	One TTL output line used to initialize the user's I/O device. This line is asserted when the system initialize line, BINIT, is asserted on the LSI-11 backplane.
INIT V2	One TTL output used for interprocessor buffer applications. This line is asserted when INIT is asserted or FNCT 2 is asserted.
)Ø	One TTL input line from the user's I/O device to the NDRV-11B. This line is used to control bit ØØ when the BAR places an address on the bus. AØØ is normally low for word operations. During byte transfers, AØØ is controlled to determine whether a high (AØØ=1) or low (AØØ=Ø) byte is written into memory.
$\overline{\text{BUSY}}$	One TTL output line to the user's I/O device from the NDRV-11B used to indicate whether the board is "$\overline{\text{busy}}$" or not. This line is low when the NDRV-11B is requesting bus mastership or performing a DMA cycle. A low to high transition indicates end of cycle.
READY	One TTL output line to the user's device from the NDRV-11B. When READY is low, DMA transfers may be initiated by the user's I/O device. READY goes low when the GO bit (bit ØØ) of the CSR is written to a 1.
CØ, C1	Two TTL input lines to the NDRV-11B from the user's device. These lines control what kind of LSI-11 bus cycle will occur for the DMA transfer. The four possible bus cycles corresponding to the status of CØ and C1 are shown below: CØ C1 BUS CYCLE Ø Ø DATI 1 Ø DATIO Ø 1 DATO 1 1 DATOB

Table 5. Description of I/O Connector Lines, con't.

MNEMONIC	DESCRIPTION
WC INC ENB	One TTL input line to the NDRV-11B from the user's I/O device to control incrementing of the NDRV-11B word count register. This line is normally high to enable incrementing; a low disables incrementing.
BA INC ENB	One TTL input line to the NDRV-11B from the user's I/O device to control incrementing of the NDRV-11B bus address register. This line is normally high to allow the bus address counter to increment. A low disables the incrementing function.
CYCLE REQUEST	One TTL input line to the NDRV-11B from the user's I/O device. A low-to-high transition initiates a DMA request when held high for a minimum of 1 microsecond and when the READY line is low.
ATTN	One TTL input line to the NDRV-11B from the user's device. This line is driven high to terminate DMA transfers, set READY, and request an interrupt if the interrupt enable bit is set.
SINGLE CYCLE	One TTL input line from the user's device to the NDRV-11B. This line is pulled high on the NDRV-11B by a pull-up resistor for normal DMA transfers. SINGLE CYCLE is pulled low by the user's I/O device for burst mode operation. When SINGLE CYCLE is driven low, total system operation is affected because the LSI-11 bus becomes dedicated to the DMA device and other devices cannot use the bus.

3.2.1 SINGLE CYCLE VS. BURST MODE DMA

Single cycle DMA allows asynchronous transfer between the user's I/O device and LSI-11 memory. The NDRV-11B is initialized by loading the BAR, WCR, and CSR. Bit ØØ of the CSR should be written to a "one". After initialization, each time the user's I/O device is ready for a transfer, it asserts CYCLE REQUEST for a minimum of 1 microsecond. This causes the NDRV-11B to request bus mastership and when this is granted, the $\overline{\text{BUSY}}$ line is negated to inform the user that a data transfer is under way. If the DMA cycle is a DATI or DATIO, the user must set up input data when CYCLE REQUEST is asserted and hold it valid until $\overline{\text{BUSY}}$ has gone low and then high again. If the DMA cycle is a DATO or DATOB, the user can strobe the output data from the NDRV-11B I/O device on the rising edge of $\overline{\text{BUSY}}$. The NDRV-11B output data will be valid at best 250 nanoseconds prior to the rising edge of $\overline{\text{BUSY}}$. Figures 9 and 10 show detailed timing diagrams.

Burst mode allows synchronous transfer of data between the NDRV-11B and the user's I/O device. When ouputting data from the user's I/O device, the data to be transferred must be set up on the falling edge of READY for the first transfer and the rising edge of $\overline{\text{BUSY}}$ for subsequent transfers. When in burst mode, the NDRV-11B will transfer data at the rate of 500K words per second, or one word every 2 microseconds. Figures 11 and 12 detail the timing.

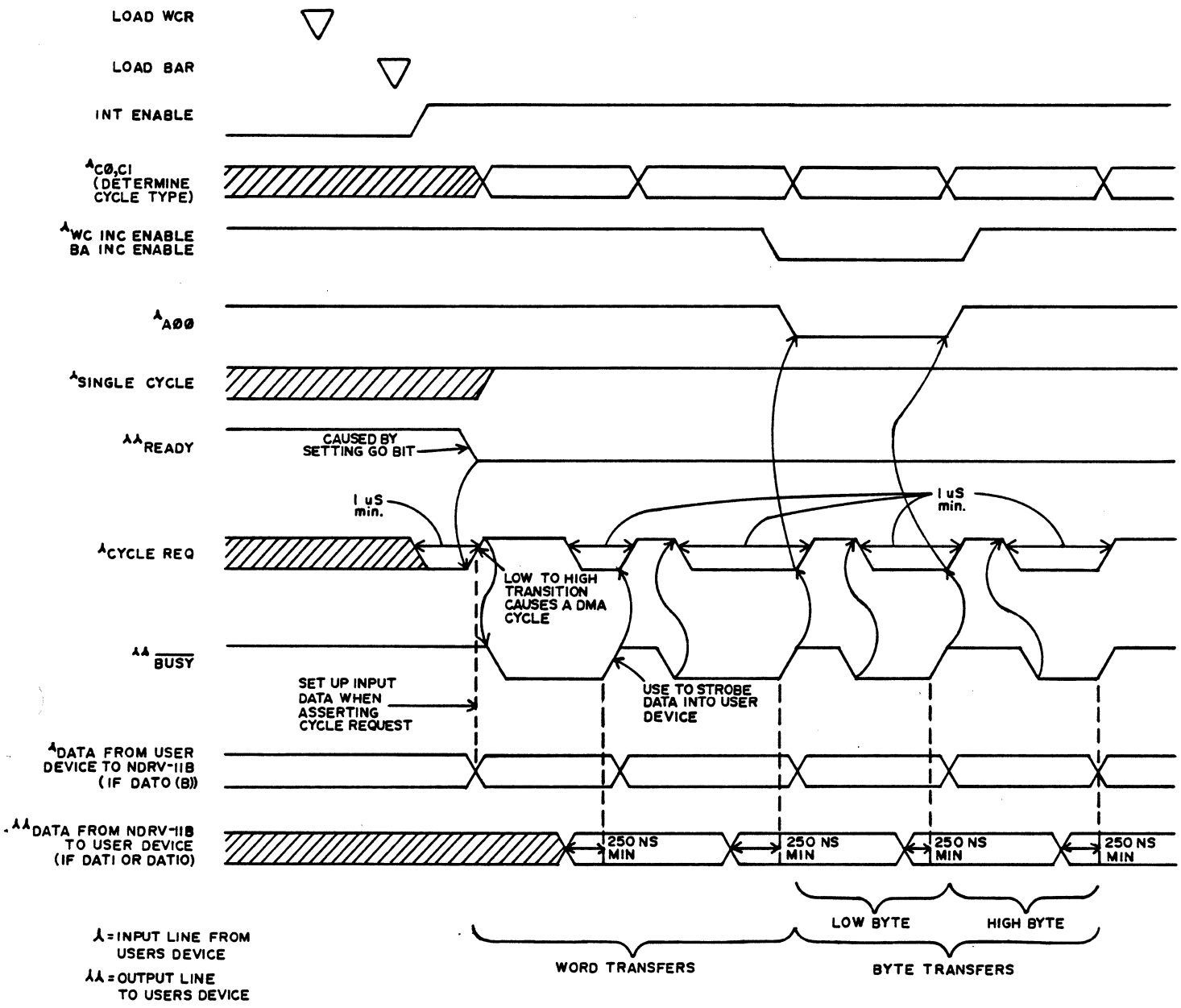


FIGURE 9. NDRV-11B ASYNCHRONOUS SINGLE CYCLE TIMING, USER INITIATED

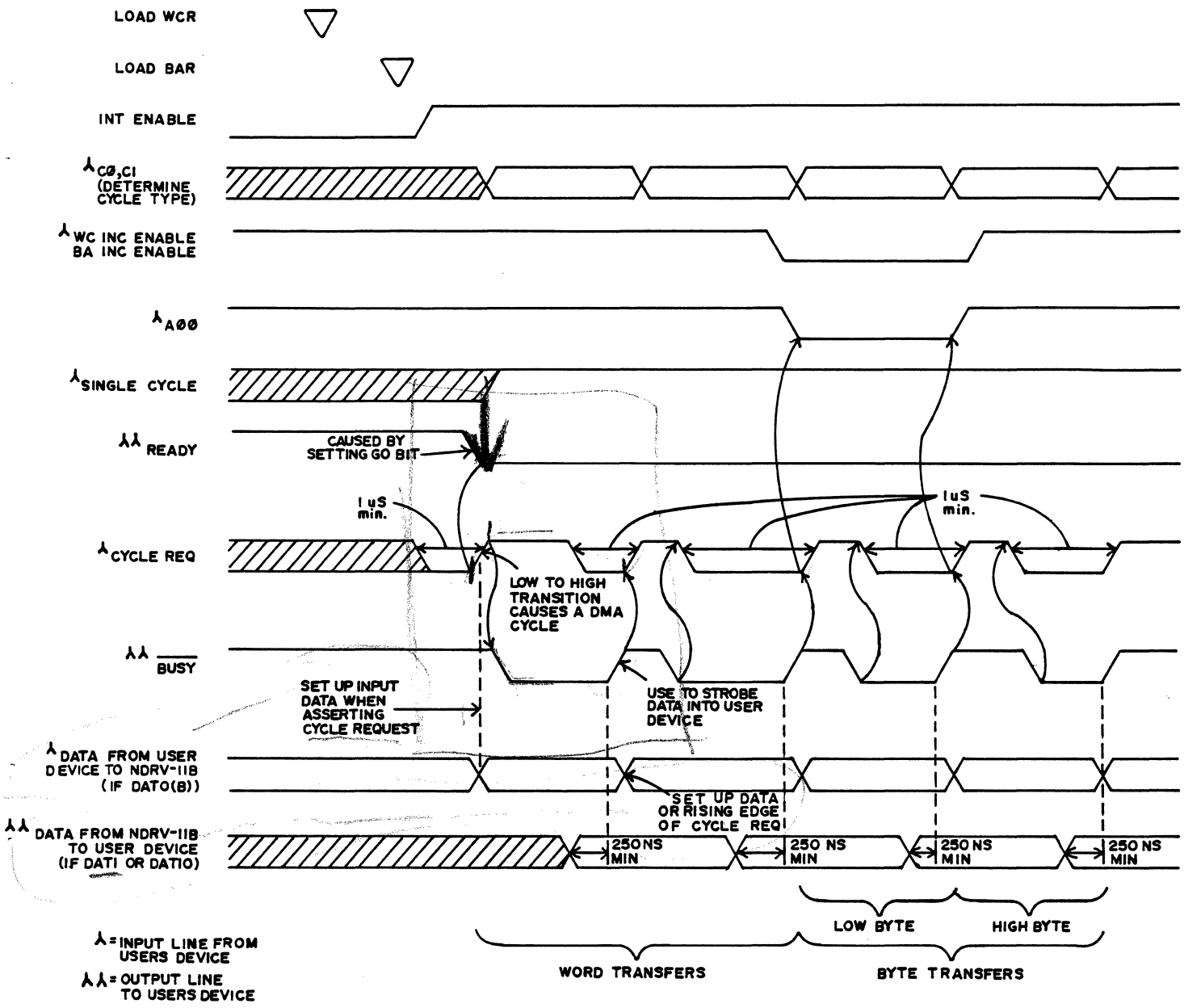
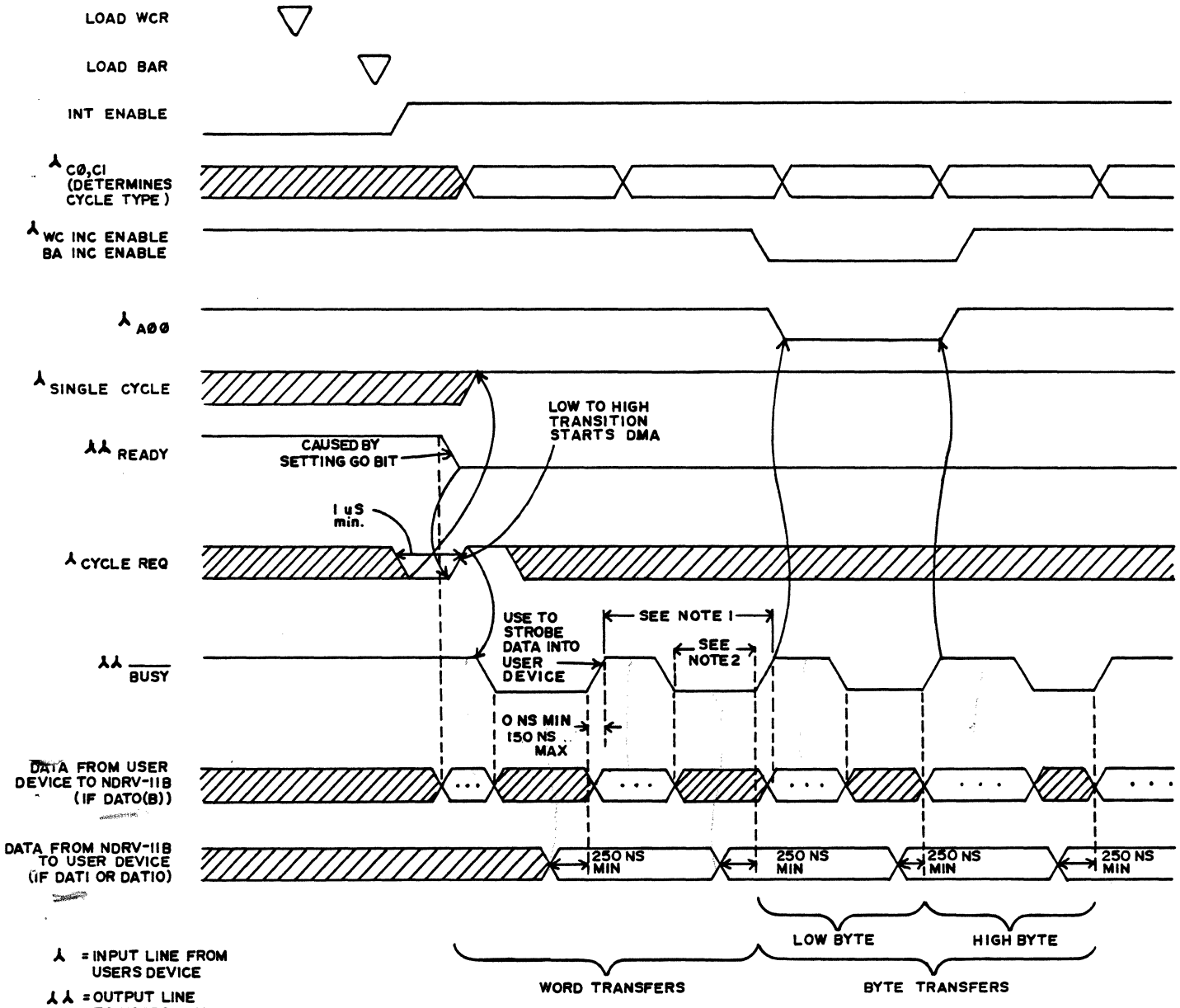


FIGURE 10. NDRV-11B ASYNCHRONOUS SINGLE CYCLE TIMING, PROGRAM INITIATED



= INPUT LINE FROM USERS DEVICE

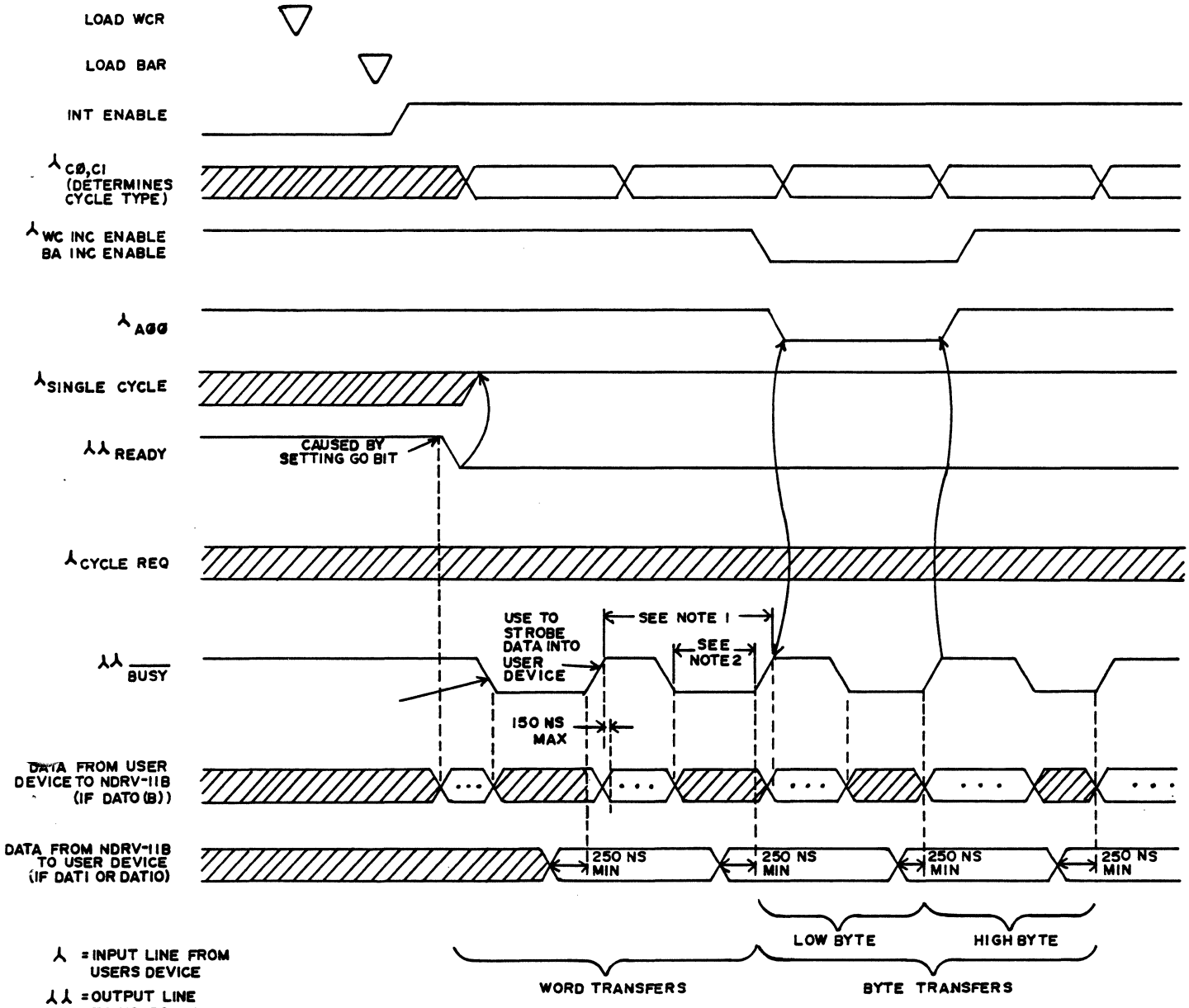
= OUTPUT LINE TO USERS DEVICE

• • • = INPUT DATA MUST BE STABLE

NOTE 1. THIS PULSE WIDTH PERIOD IS EQUAL TO THE TIME BETWEEN CONSECUTIVE ASSERTIONS OF BSYNC ON THE LSI-11 BUS. WHILE THIS IS DEPENDENT ON MEMORY REPLY TIMES. THE NOMINAL VALUE IS 2 uS.

NOTE 2. THE WIDTH OF THIS PULSE IS DETERMINED BY THE WIDTH OF BRPLY ON THE LSI-11 BUS. WHILE THIS IS DEPENDENT ON THE MEMORY REPLY TIME. IT IS NOMINALLY 200 NS.

FIGURE 11. NDRV-11B BURST MODE TIMING, USER-INITIATED



= INPUT LINE FROM USERS DEVICE

= OUTPUT LINE TO USERS DEVICE

• • • = INPUT DATA MUST BE STABLE

NOTE 1. THIS PULSE WIDTH PERIOD IS EQUAL TO THE TIME BETWEEN CONSECUTIVE ASSERTIONS OF BSYNC ON THE LSI-11 BUS. WHILE THIS IS DEPENDENT ON MEMORY REPLY TIMES. THE NOMINAL VALUE IS 2 uS.

NOTE 2. THE WIDTH OF THIS PULSE IS DETERMINED BY THE WIDTH OF BRPLY ON THE LSI-11 BUS. WHILE THIS IS DEPENDENT ON THE MEMORY REPLY TIME. IT IS NOMINALLY 200 NS.

FIGURE 12. NDRV-11B BURST MODE TIMING, PROGRAM-INITIATED

3.2.2 WORD VS. BYTE TRANSFERS

The NDRV-11B will transfer either words or bytes from the user's I/O device to memory. When transferring a byte, the full word will appear on the LSI-11 bus, but the unused byte will be ignored by memory. To transfer bytes of data, the following guidelines should be adhered to:

1. AØØ must be manipulated by the user's I/O device to determine which byte, low or high, will be transferred. AØØ must be low when addressing the low byte, and high when addressing the high byte.

2. The byte to be transferred into memory must be input into the NDRV-11B IBUF in the correct position; i.e., if the low byte is to be transferred, it must be loaded via lines IN Ø-IN 7 and if a high byte is to be transferred, it must be loaded via lines IN 8-IN 15.

3. BA INC ENB must be held low during the write cycle of the low byte of each word to inhibit the BAR from incrementing. If the WCR is loaded with the 2's compliment of the number of words to be transferred, then it too must be held low during the write cycle of the low byte of each word so that it does not increment. If the 2's compliment of the number of bytes is loaded into the WCR, WC INC ENB should be held high during all write cycles.

3.3 HAND-SHAKING AND STATUS LINES

Four sets of signals have been provided for handshaking, status, and control between the processor and the user's I/O device. They are:

STATUS A, B, C - These three TTL lines are user-defined. They are used to input status to the NDRV-11B from the user's I/O device.

FNCT 1, 2, 3 - These three TTL lines are user-defined. They are used to output status to the user's I/O device from the NDRV-11B. The FNCT 2 line will also raise INIT V2 when it is driven high.

INIT, INIT V2 - INIT is asserted whenever BINIT is asserted on the LSI-11 bus. INIT V2 is asserted whenever INIT is asserted or the FNCT 2 bit is a 1.

ATTN - ATTN terminates a DMA transfer. It will set the READY bit and cause an interrupt if interrupts are enabled.

3.4 USER'S I/O DEVICE TO SYSTEM MEMORY TRANSFER (DATO or DATOB)

Data transfers from the user's I/O device to memory under NDRV-11B control without processor intervention, except for initialization, are DMA transfers. Figure 13 illustrates that the I/O device data in a DMA DATO or DATOB cycle bypasses the processor and is deposited directly in memory. DMA transfers are initialized under program control by loading the NDRV-11B WCR with the 2's compliment of the number of words to be transferred, the BAR with the starting memory address of word storage, and the CSR control bits for transfers.

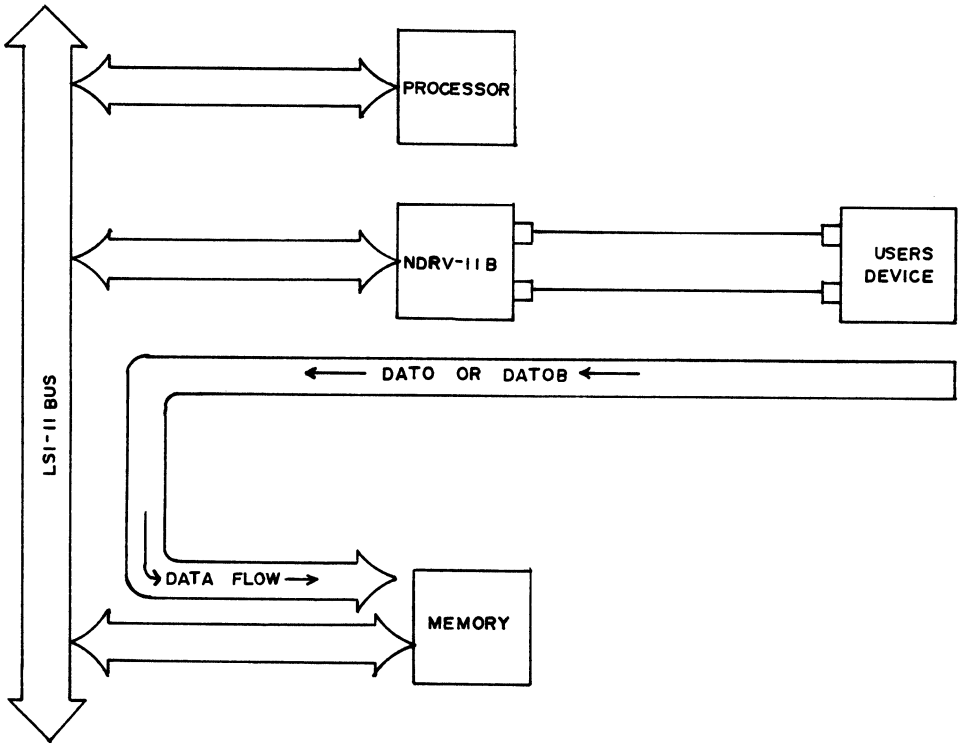


FIGURE 13. DATA FLOW DIAGRAM FOR A DATO/DATOB DMA CYCLE

When the GO bit of the CSR is written to a "one", READY goes low. This signals the user's I/O device that DMA transfers may start. When the user's I/O device is ready, it conditions the BA INC ENB, WC INC ENB, AØØ, SINGLE CYCLE, CØ, C1 and ATTN and then asserts CYCLE REQUEST. The input data bits and control bits (CØ, C1 and SINGLE CYCLE) are latched into the respective NDRV-11B registers. CYCLE REQUEST sets CYCLE and causes $\overline{\text{BUSY}}$ to go low while asserting the NDRV-11B BDMR line, which makes an LSI-11 bus request. The processor asserts BDMGO which is received as BDMGI in response to BDMR. The NDRV-11B becomes bus master, asserts BSACK, and negates BDMR.

When the NDRV-11B becomes bus master, it performs a DATO or DATOB bus cycle by placing the memory address on BDAL lines and asserting BWTBT, then asserting BSYNC. The memory latches the address and BWTBT (depending on the memory) on BSYNC and decodes the address. The NDRV-11B holds the address on the BDAL lines and the state of the BWTBT line for a set time. At the end of that period, the NDRV-11B negates BWTBT (BWTBT will remain active for a DATOB)

and removes the address from the BDAL lines. The NDRV-11B then places the user's input data on the BDAL lines and asserts BDOUT. Memory receives the data and asserts BRPLY. In response to BRPLY, the NDRV-11B negates BDOUT and then removes the user's input data from the BDAL lines. The memory then negates BRPLY and the bus cycle is terminated. The bus is released when the NDRV-11B negates BSACK and BSYNC.

At the end of a transfer, the NDRV-11B BAR and WCR are incremented (if BA INC ENB and WC INC ENB respectively are high), and $\overline{\text{BUSY}}$ goes high while READY remains low. With $\overline{\text{BUSY}}$ high and READY low, the user's I/O device can initiate another DATO or DATOB cycle by again asserting CYCLE REQUEST. DMA transfers can continue until the WCR increments to zero, at which time READY goes high and an interrupt request is generated by the NDRV-11B if the interrupt enable bit is set.

An interrupt request from the NDRV-11B will be generated when the WCR increments to zero (if the interrupt enable bit is set), the user's I/O device asserts ATTN, or the NDRV-11B accesses a nonexistent memory location while doing a DMA operation. The interrupt generated by the WCR incrementing to zero is a normal condition. The interrupt generated by the assertion of ATTN is a special condition interrupt that may be defined by the user to override the WCR. The interrupt generated when no BRPLY is received from memory addressed during a DMA transfer, is a special condition interrupt produced by the NDRV-11B. All of these conditions share the same interrupt vector.

To request an interrupt, the NDRV-11B asserts BIRQ. The processor responds by asserting BDIN followed by BIAKO which is received by the NDRV-11B as BIAKI. The NDRV-11B places a vector address on the BDAL lines in response to BIAKI, asserts BRPLY and negates BIRQ. The vector address is received by the processor

which then negates BDIN and BIAKI. The NDRV-11B then negates BRPLY and the processor exits the main program, and enters a service program for the NDRV-11B via the vector address.

3.5 SYSTEM MEMORY TO USER'S I/O DEVICE TRANSFER (DATI or DATIO)

DMA transfers from system memory to the user's I/O device occur in a manner similar to that of the user's I/O device to system memory transfer, except that the direction of the data path is different. Figure 14 demonstrates the data path of a DATI or DATIO cycle. Under program control, the NDRV-11B is initiated by loading the WCR with the 2's compliment of the number of words to be transferred, the BAR with the memory address of the first location from which data is to be taken, and the CSR with the appropriate control bits.

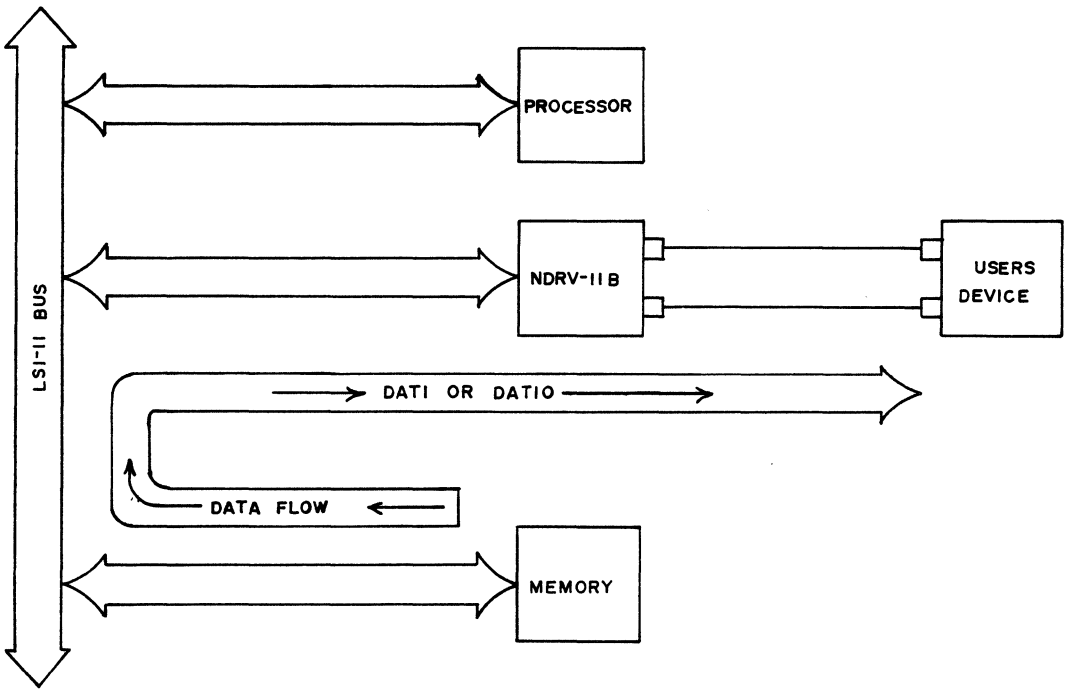
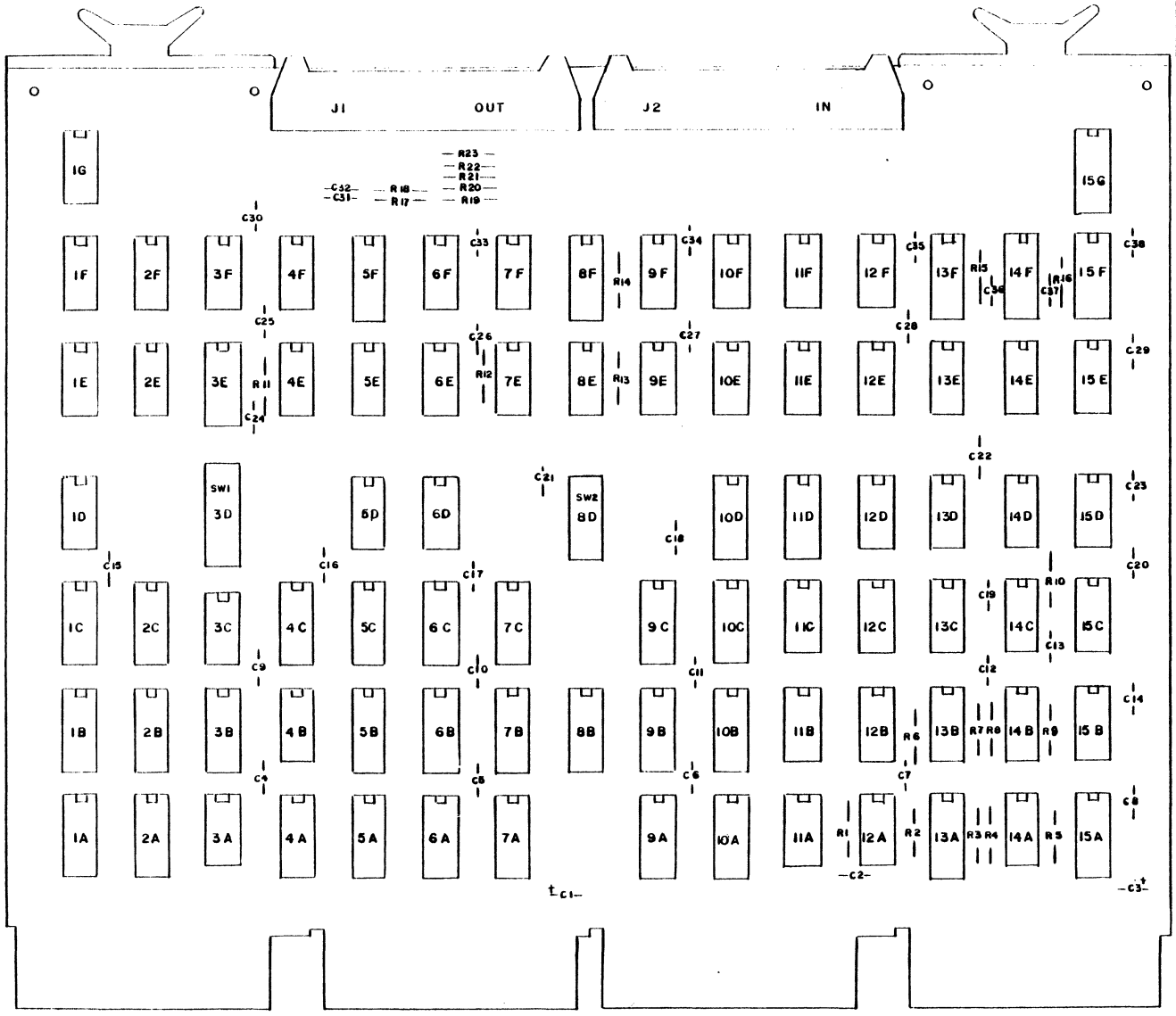


FIGURE 14. DATI/DATIO DMA DATA FLOW DIAGRAM (SYSTEM MEMORY TO USER'S DEVICE)

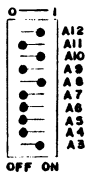
When the GO bit is set high in the CSR, READY goes low and the user's device may condition the control lines CØ, C1, BA INC ENB, WC INC ENB, SINGLE CYCLE, ATTN and then latch them into the NDRV-11B by asserting CYCLE REQUEST. The NDRV-11B responds to CYCLE REQUEST by bringing $\overline{\text{BUSY}}$ low and asserting BDMR to request bus mastership. The processor, in response to BDMR asserts BDMGO which is received as BDMGI. The NDRV-11B then becomes bus master, asserts BSACK, and negates BDMR. The bus grant sequence is terminated when the processor negates BDMGO.

Upon becoming bus master, the NDRV-11B will perform a DATI or DATIO bus cycle. (A DATI cycle is described here). The NDRV-11B places the address of the memory location to be accessed on the BDAL lines and latches it into the memory by asserting BSYNC. After a set time, the NDRV-11B removes the address from the BDAL lines and asserts BDIN. The memory responds by placing the input data on the BDAL lines and then asserting BRPLY. The input data is received by the NDRV-11B, which subsequently negates BDIN. Memory negates BRPLY, and the NDRV-11B terminates the bus cycle and releases the bus by negating BSACK and BSYNC. The data from memory is stored in the NDRV-11B OBUF for the user's I/O device. The data can be read by the user's I/O device on the low-to-high transition of $\overline{\text{BUSY}}$ although the data will remain present until new data is loaded into the OBUF.

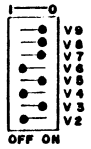
At the end of each transfer, the NDRV-11B BAR and WCR are incremented (if BA INC ENB and WC INC ENB respectively are high), BUSY goes high, and READY remains low unless the WCR has incremented to zero. If the WCR has not incremented to zero, the user's I/O device can initiate another DATI or DATIO cycle by again asserting cycle request. DMA transfers can continue until the WCR increments to zero and generates an interrupt request (if the interrupt enable bit has been set).



SW 1



SW 2



G F E D C B A

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

PARTS LIST DRAWING NO. — PL 762-0035

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN	12/3/79
CHECKED	1/25/80
RH	2/29/80

netcom products, inc.

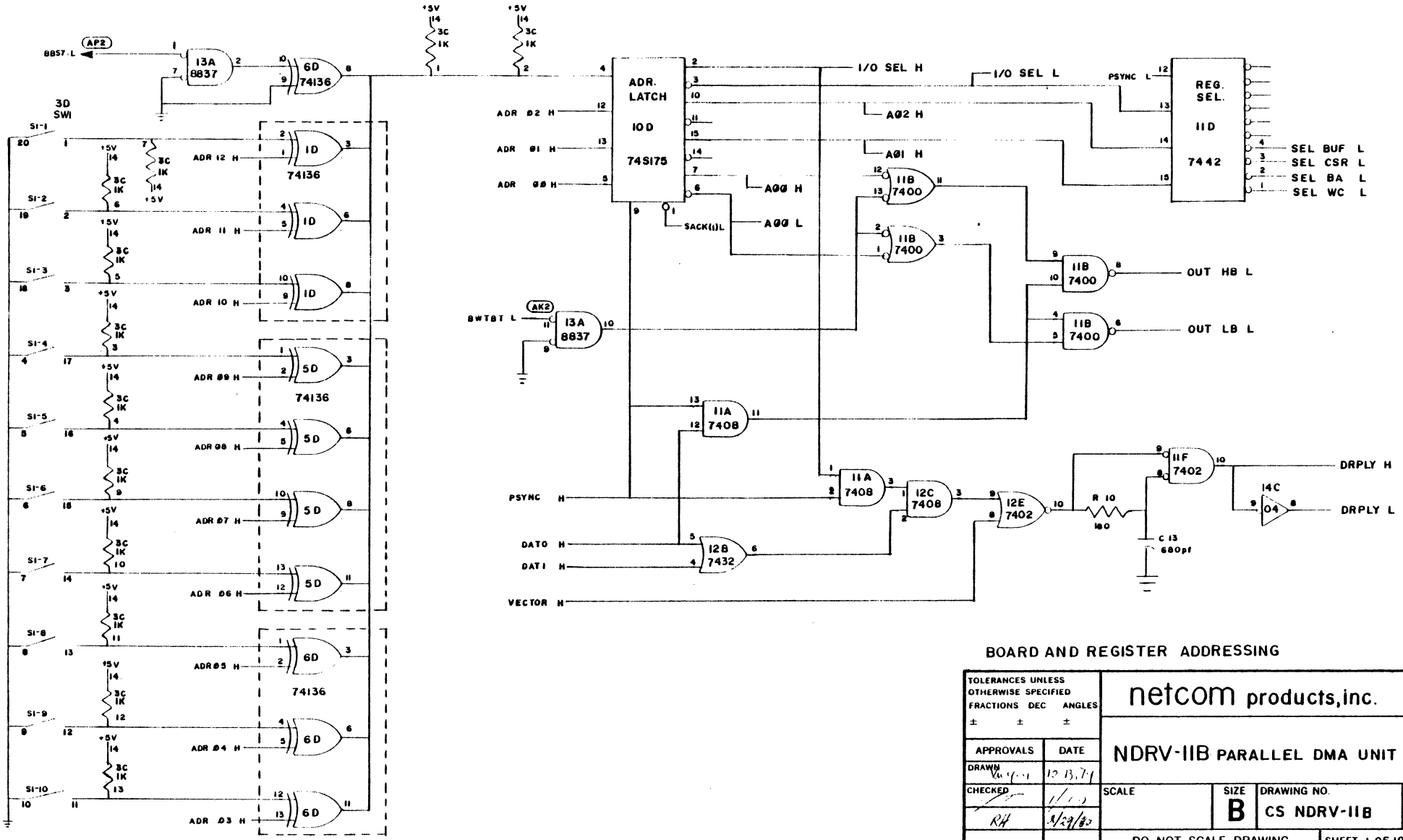
NDRV-11B DMA BOARD

SCALE	SIZE	DRAWING NO.	REV
	B	AD NDRV-11B	

DO NOT SCALE DRAWING — SHEET 1 OF 1

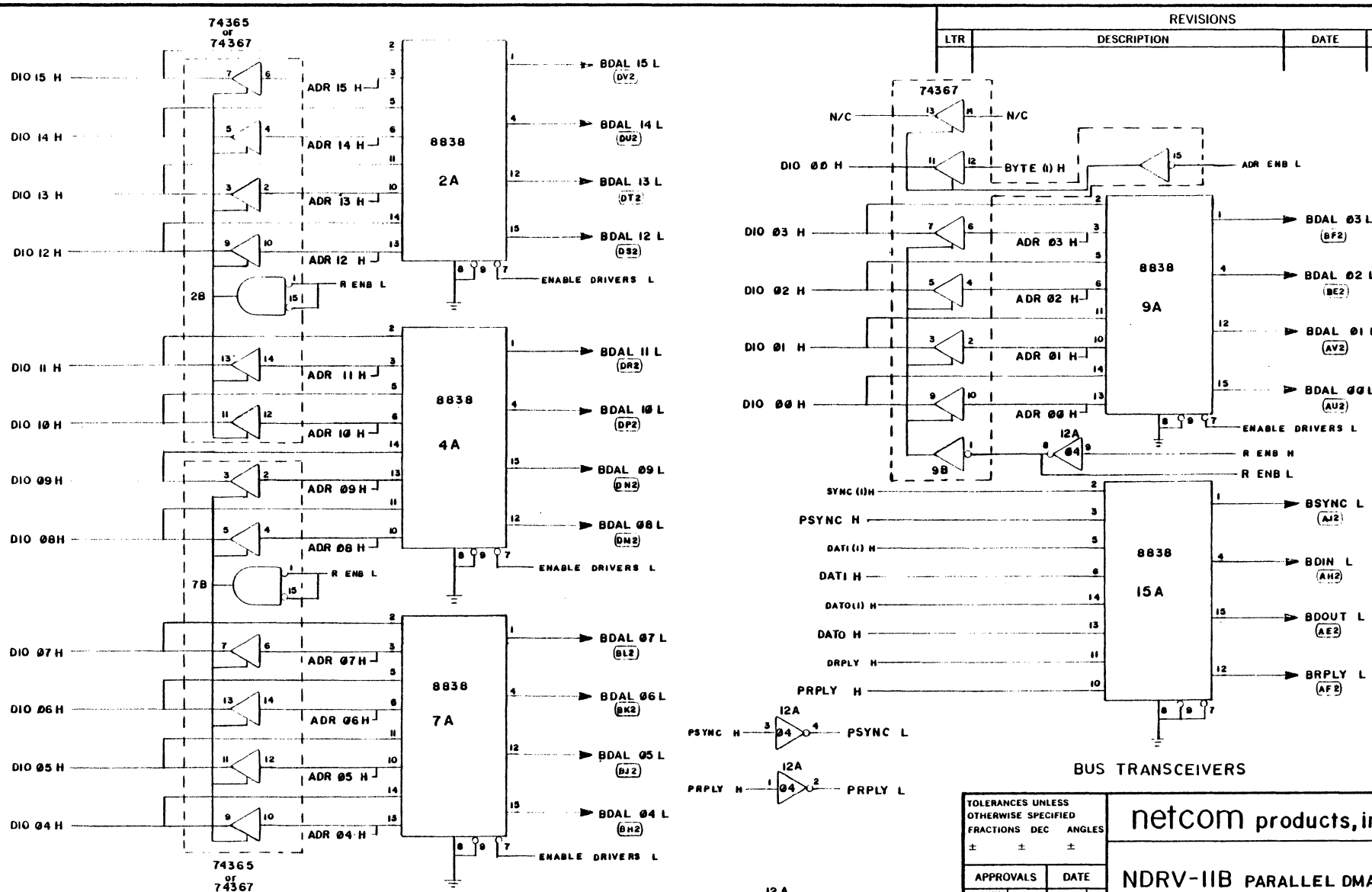
NOTE: 14C IS A 7404

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



BOARD AND REGISTER ADDRESSING

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		netcom products,inc.			
APPROVALS	DATE	NDRV-11B PARALLEL DMA UNIT			
DRAWN	12 13 79	SCALE	SIZE B	DRAWING NO. CS NDRV-11B	REV
CHECKED	1/1/80				
RH	3/29/80	DO NOT SCALE DRAWING		SHEET 1 OF 10	



BUS TRANSCEIVERS

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
± ± ±

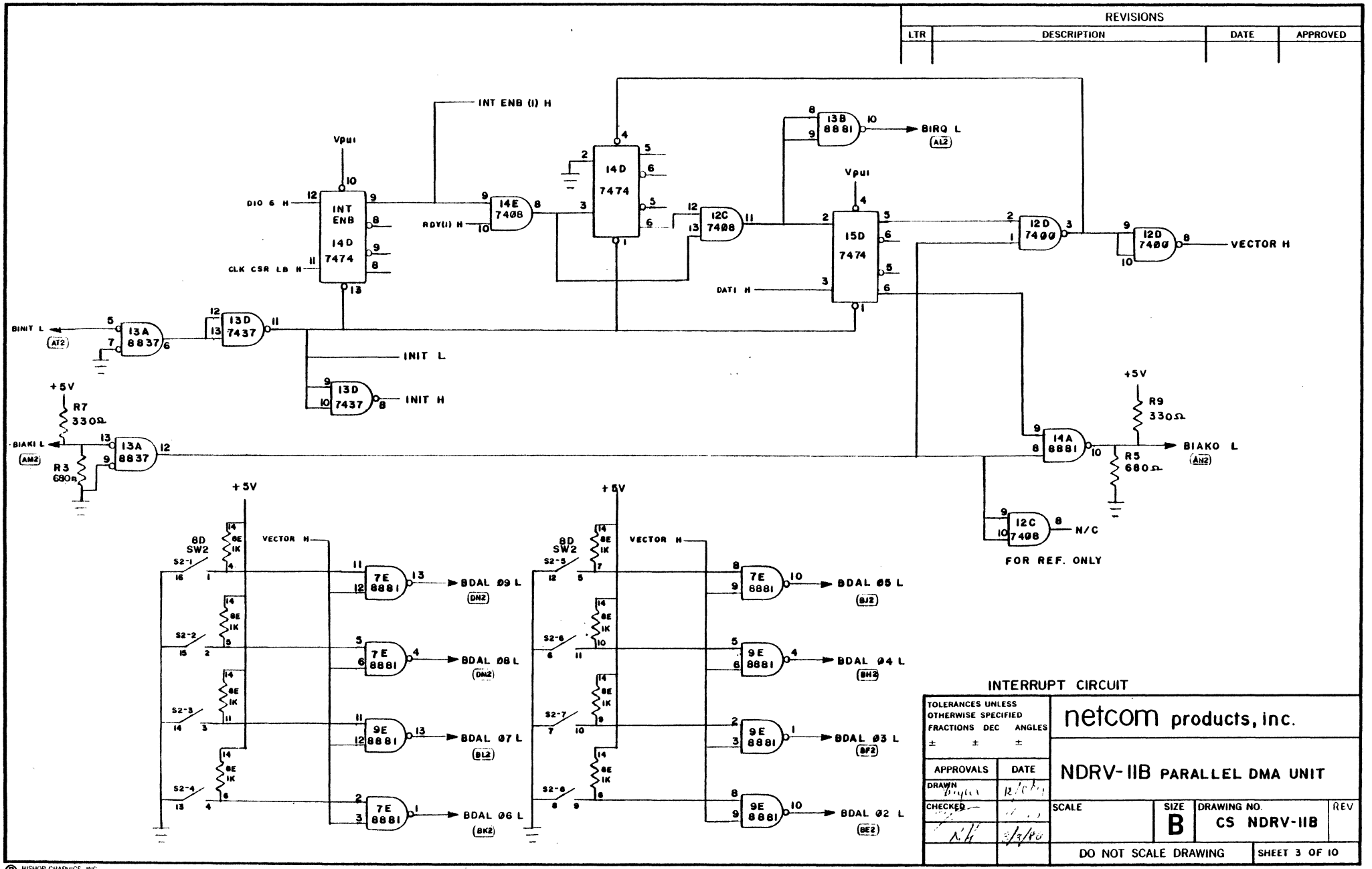
APPROVALS	DATE
DRAWN	12/17/79
CHECKED	1/22/80
RH	2/27/80

netcom products, inc.

NDRV-11B PARALLEL DMA UNIT

SCALE	SIZE	DRAWING NO.	REV
	B	CS NDRV-11B	

DO NOT SCALE DRAWING | SHEET 2 OF 10

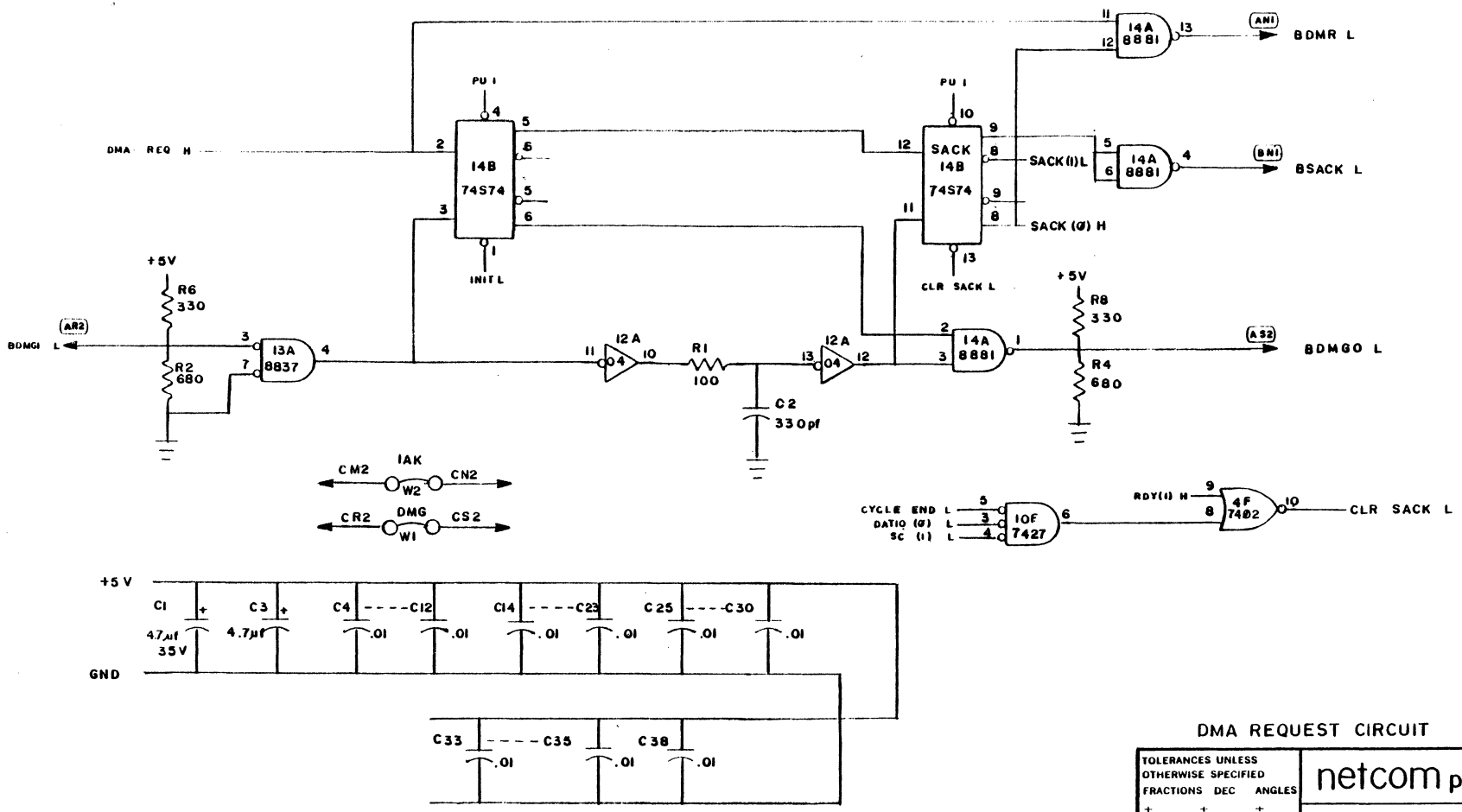


INTERRUPT CIRCUIT

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS ± DEC ± ANGLES ±		netcom products, inc.	
APPROVALS	DATE	NDRV-IIB PARALLEL DMA UNIT	
DRAWN	12/6/79		
CHECKED		SCALE	SIZE B — DRAWING NO. CS NDRV-IIB — REV
	2/3/80	DO NOT SCALE DRAWING	SHEET 3 OF 10

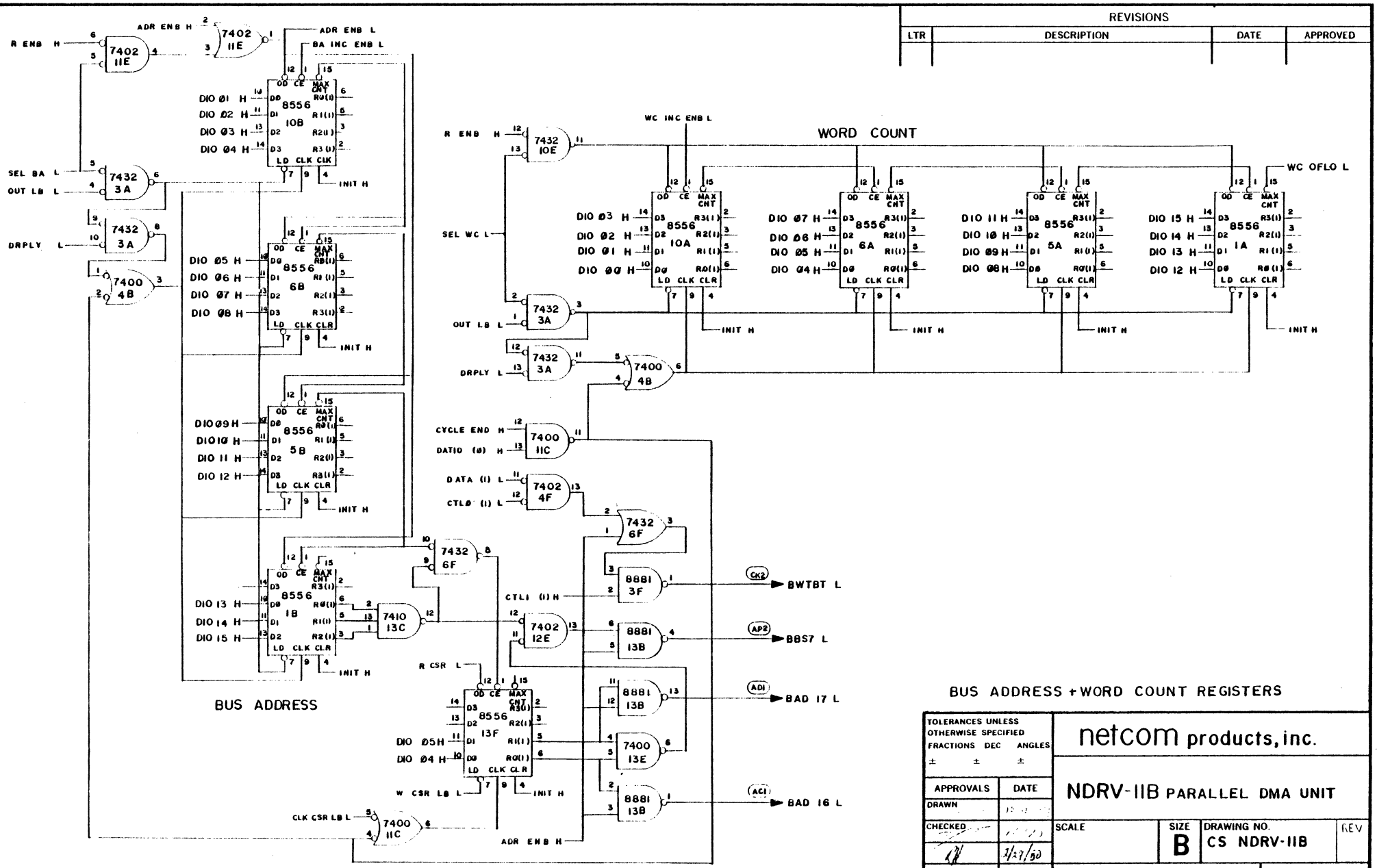
NOTE: 12A IS A 7404.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

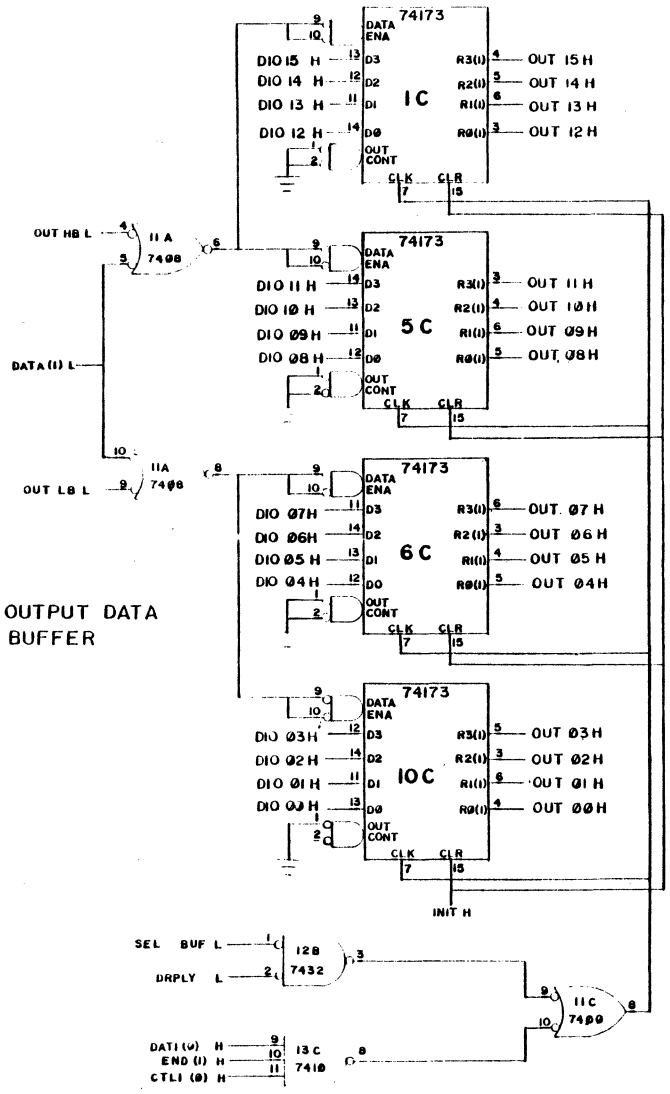


DMA REQUEST CIRCUIT

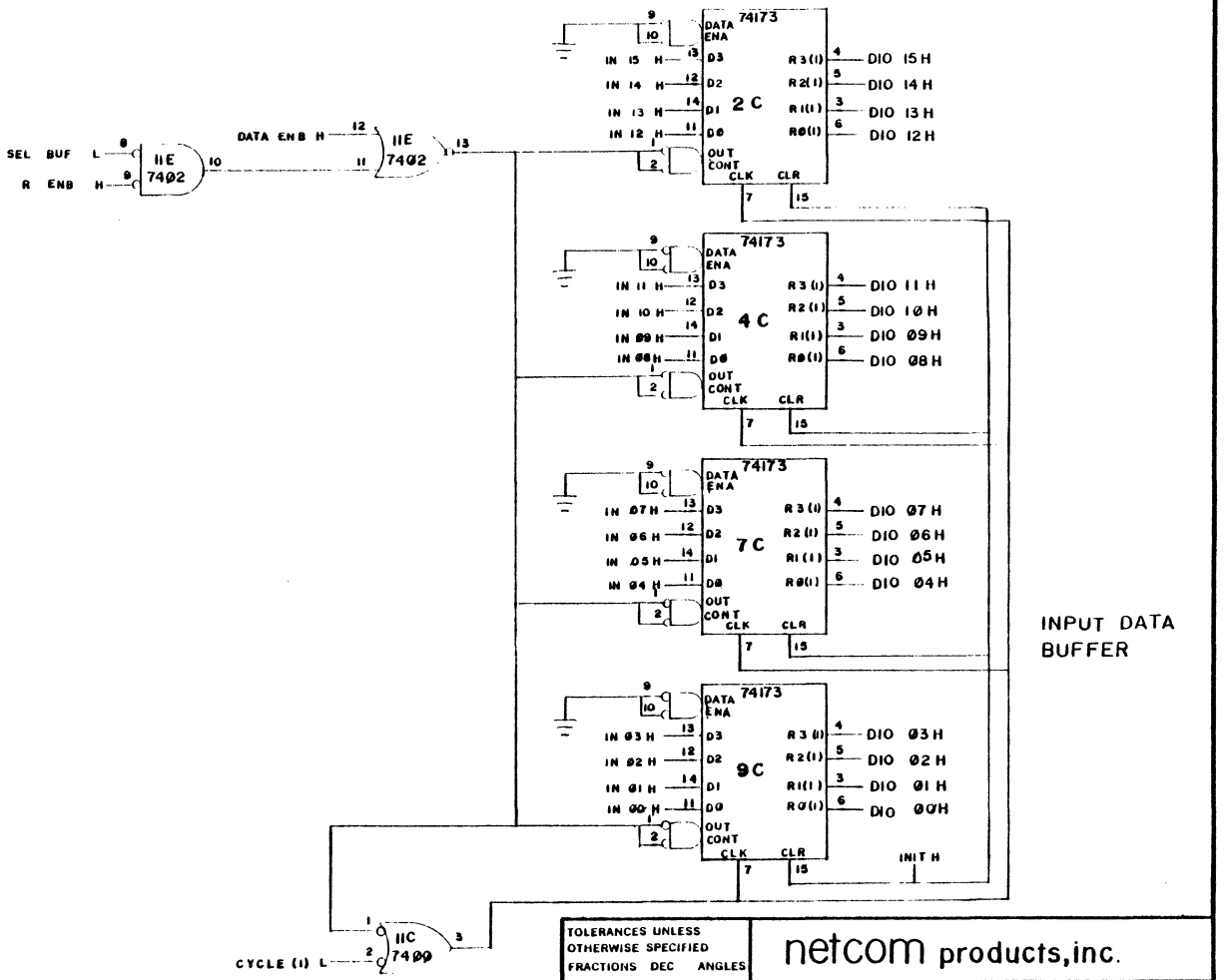
TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		netcom products, inc.			
APPROVALS	DATE	NDRV-IIB PARALLEL DMA UNIT			
DRAWN	11-21-77	SCALE	SIZE B	DRAWING NO. CS NDRV-IIB	REV
CHECKED		DO NOT SCALE DRAWING		SHEET 4 OF 10	
	2/24/78				


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
BUS ADDRESS
WORD COUNT
BUS ADDRESS + WORD COUNT REGISTERS
BWTBT L
BBS7 L
BAD 17 L
BAD 16 L
netcom products, inc.
NDRV-11B PARALLEL DMA UNIT
DRAWING NO. CS NDRV-11B
SIZE B
SCALE
REV
DO NOT SCALE DRAWING
SHEET 5 OF 10
APPROVALS
DRAWN
CHECKED
DATE
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



OUTPUT DATA BUFFER



INPUT DATA BUFFER

DATA BUFFERS

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

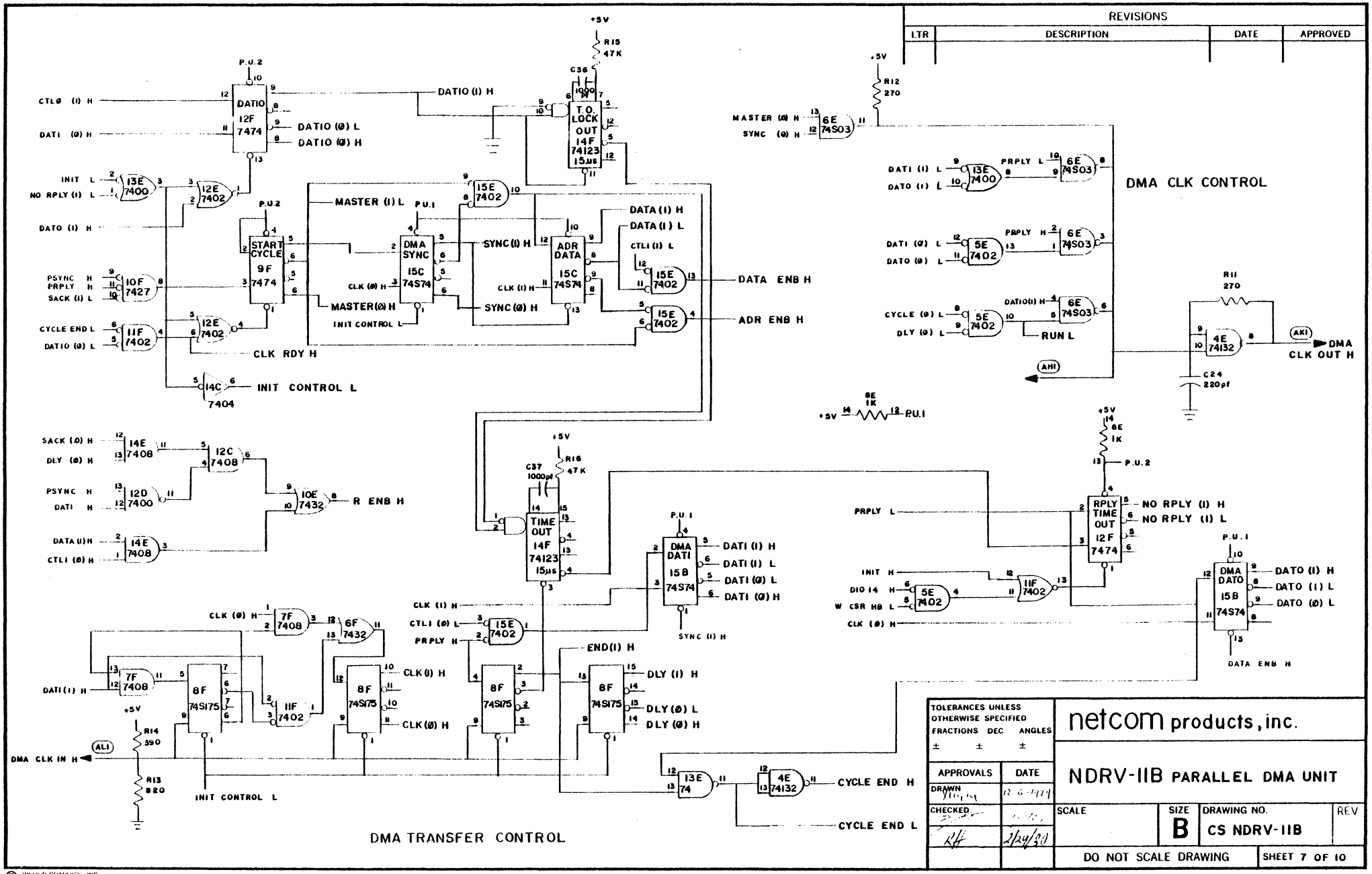
APPROVALS	DATE
DRAWN	
CHECKED	
	3/14/80

netcom products, inc.

NDRV-11B PARALLEL DMA UNIT

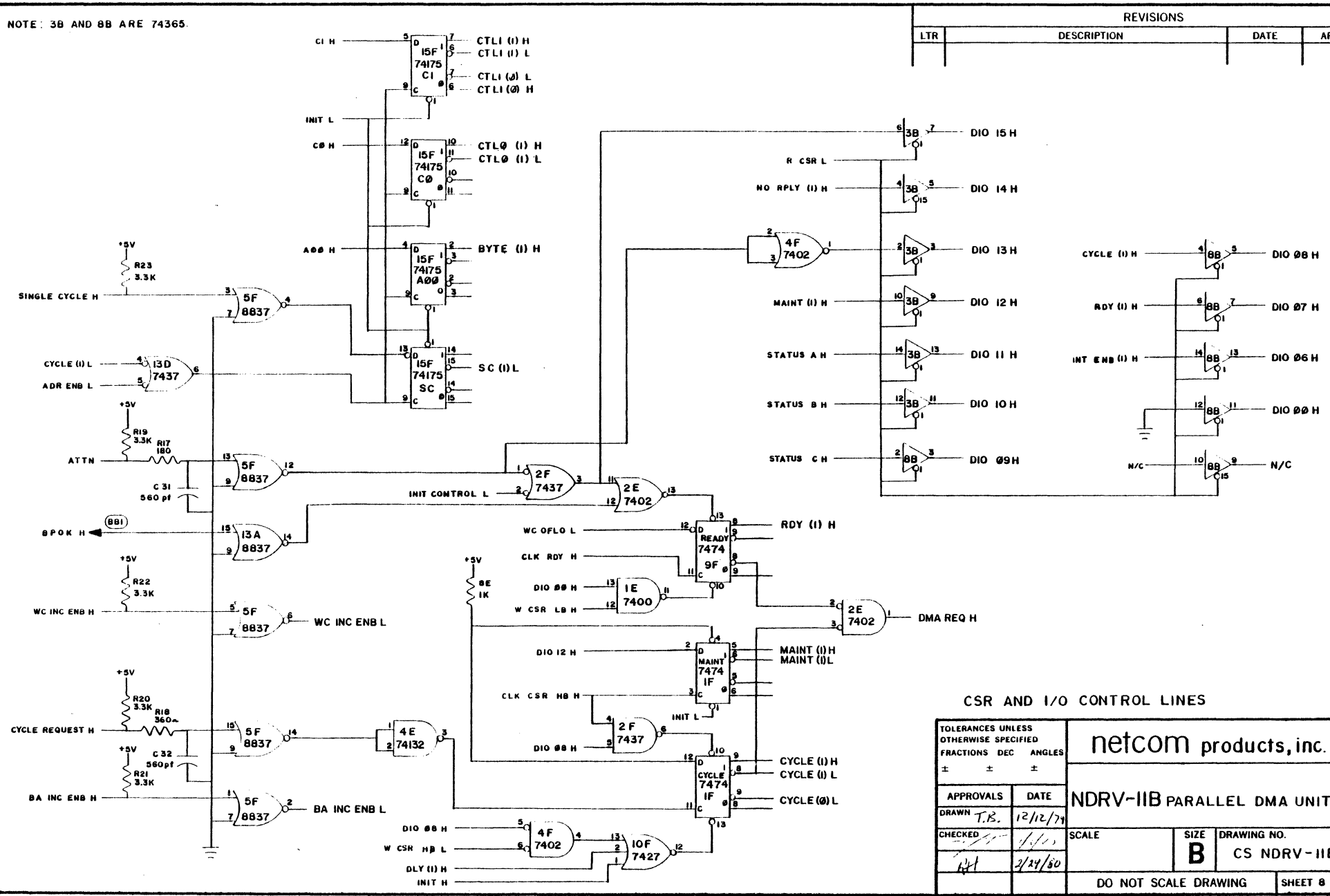
SCALE	SIZE	DRAWING NO.	REV
	B	CS NDRV-11B	

DO NOT SCALE DRAWING | SHEET 6 OF 10



NOTE: 3B AND 8B ARE 74365.

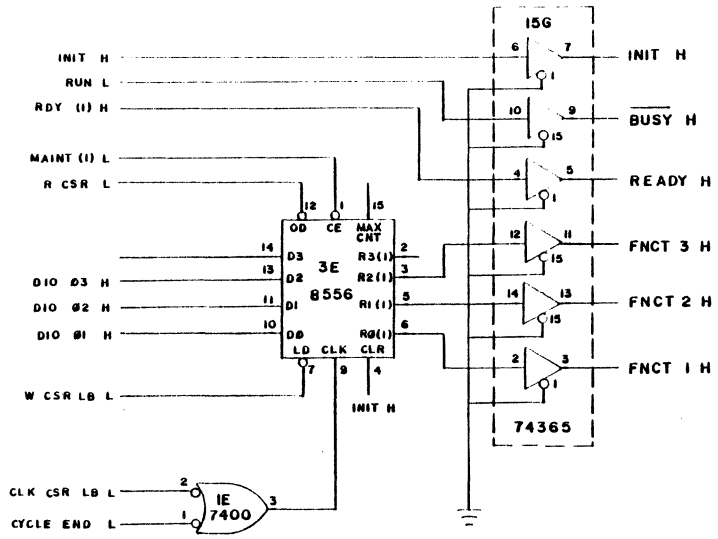
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

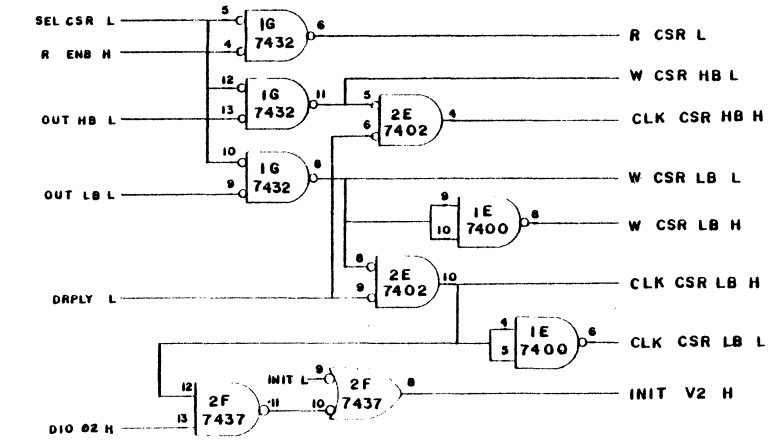


CSR AND I/O CONTROL LINES

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		netcom products, inc.			
APPROVALS	DATE	NDRV-11B PARALLEL DMA UNIT			
DRAWN T.B.	12/12/79	SCALE	SIZE B	DRAWING NO. CS NDRV-11B	REV
CHECKED	/ /				
	2/29/80	DO NOT SCALE DRAWING		SHEET 8 OF 10	

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





I/O CONTROL LINES AND CSR ADDRESSING

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±	netcom products, inc.
APPROVALS / DATE	NDRV-IIB PARALLEL DMA UNIT
DRAWN / CHECKED / 3/27/80	SCALE / SIZE B / DRAWING NO. CS NDRV-IIB / REV.
DO NOT SCALE DRAWING	SHEET 9 OF 10