MOTOROLA® ALS-TTL MACROCELL ARRAY LIBRARY

Preliminary
June 1985

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PERSONAL CAD SYSTEMS INC.

000-0083-00

PERSONAL CAD SYSTEMS

MOTOROLA(R) ALS-TTL MACROCELL ARRAY LIBRARY

SCHEMATIC SYMBOLS

Preliminary

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June 1985

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CONTENTS

INTRODUCTION

This manual and the two Motorola ALS-TTL Macrocell Array Library Symbol Diskettes comprise the P-CAD Motorola ALS-TTL Macrocell Array Library.

The library diskettes contain the following files for use with the PC-CAPS schematic capture program:

- Component files
- Special symbol files
- Layer structure file, ICLAYS.SCH
- Standard-size drawing sheet files, ASIZE.SCH through ESIZE.SCH.

The library has been developed at the request of our users, and we welcome any suggestions for improvements or additions.

The first section of the manual outlines a directory structure that is recommended for storage of the library files. The second section describes the special library files provided for translation of the user's circuit netlist into a LOGCAP(TM) output recognized by Motorola CAD systems. The third section provides guidelines on the design of a circuit for use with the NX-MLCP interface program.

The remainder of the manual is devoted to lists of components by sequence and function, component pin sequences, and component plots.

DIRECTORY STRUCTURE

For more efficient storage and easier access to the library, P-CAD recommends that you store the library components within a directory structure tailored to your particular applications and design methods. Figure 1 is an example of an efficient directory structure for storage of the library symbols and parts.

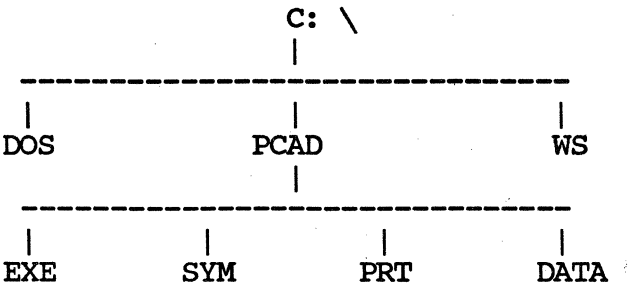


Figure 1. Sample Directory Structure

In this example, symbols are stored in the SYM directory and parts are stored in the PRT directory.

SPECIAL FILES AND SYMBOLS

In addition to the standard Motorola component symbols, the P-CAD Motorola ALS-TTL Macrocell Array Library contains a special layer structure file, standard-size drawing sheet files, and special symbol files. These special files are used to translate the user's schematic netlist into a format that is compatible with Motorola CAD systems. Each of these files is discussed below.

Layer Structure File

The ICLAYS.SCH layer structure shown below is a modified version of the standard P-CAD layer structure (LAYS.SCH). ICLAYS.SCH was used to create the Motorola ALS-TTL symbols included in this library.

Layer	Name	Pen	Status	Use
1	WIRES	1	OFF	Interconnecting wires
2	BUS	1	OFF	Interconnecting busses/wires
3	GATE	2	ABL	Gate geometry/symbol
4	IEEE	2	OFF	Not used
5	PINFUN	3	OFF	Not used
6	PINNUM	1	OFF	Not used

Layer	Name	Pen	Status	Use
7	PINNAM	6	ABL	Pin names
8	PINCON	4	ABL	Pin connections (dot)
9	REFDES	2	OFF	Not used
10	ATTR	6	OFF	Visable attributes
11	SDOT	1	OFF	Not used
12	DEVICE	5	ABL	Macrocell ID
13	OUTLIN	5	ABL	Macrocell outline
14	ATTR2	6	OFF	Invisible attributes
15	NOTES	6	OFF	Notes/text
16	NETNAM	4	OFF	Net names
17	CMPNAM	5	OFF	Component instance names
18	BORDER	5	OFF	Drawing border

Drawing Sheets

The library includes standard-size drawing sheet files, ASIZE.SCH through ESIZE.SCH, for circuit design. These files provide the ICLAYS.SCH layer structure plus a drawing sheet border. They can be used in place of the ICLAYS.SCH layer structure.

Special Symbol Files

In addition to the standard Motorola component symbols, the library includes special "non-component" symbols. These symbols are interpreted by the NX-MLCP Motorola IC Interface program, which translates the user's design information into a LOGCAP format compatible with Motorola CAD systems. Each symbol used in the circuit is described on a line of the LOGCAP output. The symbols include:

- PADIN.SYM and PADOUT.SYM to represent circuit inputs and outputs
- WAND2.SYM to represent a Wired-AND with two inputs
- WOR2.SYM through WOR8.SYM for Wired-OR components with from 2 to 8 inputs.

A test schematic containing the special symbols is shown in Figure 2; the corresponding LOGCAP output is shown in Figure 3. Refer to the appropriate Motorola documentation or consult Motorola technical support personnel for further information on the use of special symbols in a specific circuit design.

For a complete description of the NX-MLCP interface program, see the NX-MLCP User's Manual.

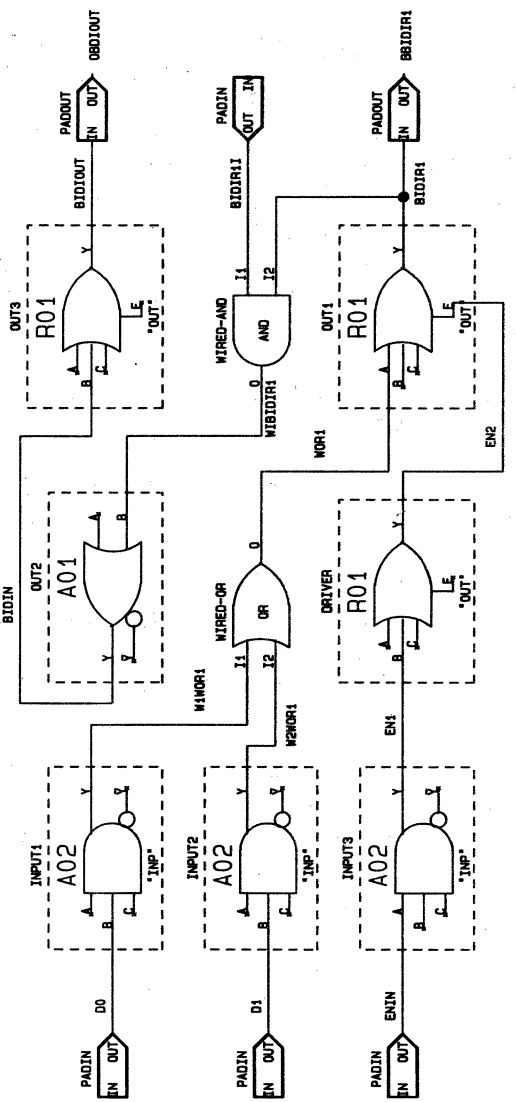


Figure 2. Test Schematic

```
$$*************************************************
$$                                                *
$$  Copyright (C) 1985 - Personal CAD Systems, Inc.  *
$$                                                *
$$  Program  :   NX-MLCP  VERSION 1.24            *
$$  Date     :   May 10 1985                      *
$$  Time     :   09:15:30 AM                      *
$$  File In  :   LCPTST.NLT                       *
$$  File Out :   LCPTST.LCP                       *
$$  Format   :   LOGCAP LIST                      *
$$                                                *
$$*************************************************

$NETWORK
$INP D0 D1 ENIN BIDIR1I
$OUT OBDIOUT BBIDIR1
$AND 0 0
WIBIDIR1 2 BIDIR1I BIDIR1
$OR 0 0
WOR1 2 W1WOR1 W2WOR1
$SUBU A02
UN0 W1WOR1 / &
CON1 D0 CON1
$SUBU A02
UN1 W2WOR1 / &
CON1 D1 CON1
$SUBU A02
UN2 EN1 / &
ENIN CON1 CON1
$SUBU R01
EN2 / &
CON0 EN1 CON0 CON1
$SUBU R01
BIDIR1 / &
WOR1 CON0 CON0 EN2
$SUBU R01
BIDIOUT / &
CON0 BIDIN CON0 CON1
$SUBU A01
UN3 BIDIN / &
CON0 WIBIDIR1
$SUBU BOUT
OBDIOUT / &
BIDIOUT
$SUBU BOUT
BBIDIR1 / &
BIDIR1
```

Figure 3. LOGCAP Output

CIRCUIT DESIGN

To design the circuit, run PC-CAPS. After the menu is displayed, select FILE/LOAD. Load the ICLAYS.SCH layer structure or one of the drawing sheets supplied with the library (ASIZE.SCH through ESIZE.SCH).

Create the design by entering the appropriate components, wires, text, instance, and net names. Step-by-step instructions are given in the tutorial section of your PC-CAPS User's Manual.

Each PC-CAPS symbol contains the electrical "intelligence" required to create schematics and extract data.

Special Attributes

Two types of attributes have been assigned to the library symbols for use with the Motorola NX-MLCP IC Interface program. One attribute has the form FTYPE="INP" or FTYPE="OUT". It is used with certain input or output cells that have one or more unconnected input pins and/or an unconnected enable pin named "E". In the LOGCAP $SUBU statement describing the cell inputs and output, the unconnected pins will be designated "CON0" or "CON1", as appropriate. Several examples are shown on the schematic and accompanying LOGCAP output (Figures 2 and 3).

The other attribute is used with an alternative symbol for a macrocell. The form of the attribute is ALT=<filename>, where <filename> is the macrocell ID. For example, the M50 macrocell has two library symbols, M50.SYM and M50A.SYM. The alternative symbol, M50A, has the attribute ALT="M50" and will be shown in the LOGCAP output as "M50".

Input and Output Signals

For each input signal to the circuit there must be a PADIN.SYM with input and output pins. A net must be connected to each output pin. A net connected to the output pin of a PADIN.SYM will be listed as an input signal on the $INP line of the LOGCAP output. This signal can be viewed as the input signal to the circuit from an external source.

For each output from the circuit there must be a PADOUT.SYM with input and output pins. A net must be connected to each of the pins. A net connected to the output pin of a PADOUT.SYM will be listed as an output signal on the $OUT line of the LOGCAP output. This signal can be viewed as the output signal to the external environment.

Nets connected to the pins of the PADOUT symbols will also be listed as input and output signals in the $SUBU BOUT statement of the LOGCAP output.

Bidirectional Pads

Each bidirectional pad must be modeled by a two-input Wired-AND, an input pad, and an output pad. The Wired-AND must be represented by a WAND2.SYM symbol. See the test schematic, Figure 2, for an example of this configuration. For each WAND2.SYM in the circuit there will be an $AND statement in the LOGCAP output (see Figure 3).

Wired-OR

For each Wired-OR component used in the circuit there must be one WOR.SYM with the appropriate number of inputs. The library provides WOR symbols for Wired-OR components with from two to eight inputs. An $OR statement will appear in the LOGCAP output for each WOR.SYM in the circuit.

COMPONENT LIST BY SEQUENCE

Number	Page	Disk
H01	24	1
H02	24	1
H03	24	1
H04	24	1
H05	24	1
H06	24	1
H07	24	1
H08	24	1
H09	24	1
H10	24	1
H11	24	1
H12	24	1
M13	25	1
M14	25	1
H15	25	1
H16	25	1
H17	25	1
H18	25	1
M19	26	1
M20	26	1
M21	26	1
M22	26	1
M23	26	1
M24	27	1
M25	27	1
M26	27	1
H27	27	1
M28	28	1
M29	28	1
M30	28	1
H31	28	1
M32	28	1
H33	28	1
H34	29	1
H35	29	1

Number	Page	Disk
M36	29	1
M37	29	1
M38	29	1
M39	29	1
H40	29	1
H41	29	1
H42	29	1
H43	29	1
M44	29	1
M45	29	1
M46	29	1
M47	29	1
M48	29	1
M49	29	1
M50	30	1
M50A	30	1
M51	30	1
M51A	30	1
H52	30	1
H52A	30	1
M53	30	1
H54	30	1
M55	30	1
M56	31	1
H57	31	1
H58	31	1
H59	31	1
H60	31	1
H61	31	1
H62	31	1
H63	31	1
H64	31	1
H65	32	1
H66	32	1
H67	32	1
M68	32	1
H69	32	1
H81	32	1

Number	Page	Disk
H82	32	1
A01	32	2
A02	32	2
R01	32	2
R02	32	2
R03	32	2
R04	32	2
R05	32	2
R06	32	2
B01	32	2
B02	32	2
F01	32	2
F02	32	2
F03	32	2
F04	32	2
WAND2	33	2
WOR2	33	2
WOR3	33	2
WOR4	33	2
WOR5	33	2
WOR6	33	2
WOR7	33	2
WOR8	33	2
PADIN	33	2
PADOUT	33	2

COMPONENT LIST BY FUNCTION

Gates

H01
H02
H03
H04
H05
H06
H07
H08
H09
H10
H11
H12
M13
M14
H15
H16
H17
H18
M19
M20
M21
M22
M23
M24
M25
M26
H27
M28
M29
M30
M55
M56
H57
H58
H59

Gates (Cont'd)

H60
H61
H62
H63
H64
H65
H66

Flip-Flops

H31	Dual D F/F
M32	D F/F with Mux
H81	Dual D F/F with Diff, Clock and Data
H82	Dual D F/F with Set and Reset

Latches

H33	Dual 2 Bit Latch
H34	Dual Latch with Mux
H35	Quad Latch
H67	Dual Latch

Multiplexers

M36	4 to 1 Mux with Enable
M37	4 to 1 Mux with Enable
M38	4 to 1 Mux with Enable
M39	4 to 1, 2 to 1 Mux
H40	Quad 2 to 1 Mux, Com Sel
H41	Quad 2 to 1 Mux
H42	Quad 2 to 1 Mux with Enable
H43	Dual 2 to 1 Mux
M68	4 to 1 Mux
H69	Dual 2 to 1 Mux

Decoders

M44	1/4 Decoder (High)
M45	1/4 Decoder (Low)
M46	1/4 Decoder (High)
M47	1/4 Decoder (Low)

Adders

M50	Full Adder
M50A	Full Adder
M51	Full Adder
M51A	Full Adder
H52	Dual Full Adder
H52A	Dual Full Adder
M53	Full Adder and Half Adder
H54	Dual Half Adder

Miscellaneous Functions

M48	Priority Encoder
M49	Priority Expander

MCA500ALS Input Cells

A01
A02

MCA500ALS Output Cells

R01
R02
R03

MCA500ALS Output Cells (Cont'd)

R04
R05
R06

MCA1300ALS Input Cells

B01
B02

MCA1300ALS Output Cells

F01
F02
F03
F04

Special Symbols

WAND2	2 Input Wired-AND
WOR2	2 Input Wired-OR
WOR3	3 Input Wired-OR
WOR4	4 Input Wired-OR
WOR5	5 Input Wired-OR
WOR6	6 Input Wired-OR
WOR7	7 Input Wired-OR
WOR8	8 Input Wired-OR
PADIN	Input Pad
PADOUT	Output Pad

COMPONENT PIN SEQUENCES

H01:	Y'	Y	Z	Z'	A	B	C		
	D	E	F	G					
H02:	Y	Y'	Z'	Z	A	B	C		
	D	E	F	G					
H03:	Y	Y'	Z'	Z	A	B	C		
	D	E	F	G					
H04:	Y'	Y	Z	Z'	B	C	A	D	E
H05:	Y	Y'	A	B	C	D	E	F	G
H06:	Y	Y'	A	B	C	D	E	F	
H07:	Y	B	C	A	D	E	F		
H08:	Y	B	C	A	D	E	F		
H09:	Y'	Y	A	B	C	D			
H10:	Y	Y'	A	B	C				
H11:	Y	A	B	C	D				
H12:	Y	A	B	C	D				
M13:	Y	Y'	A	B	C	D	E		
	F	G	H	I	J	K	L		
M14:	Y'	Y	A	B	D	E	G		
	H	J	K	C	F	I	L		
H15:	Y	Y'	A	B	C	D	E	F	
H16:	Y'	Y	A	B	C	D	E	F	
H17:	Y	Y'	A	B	C	D	E	F	G

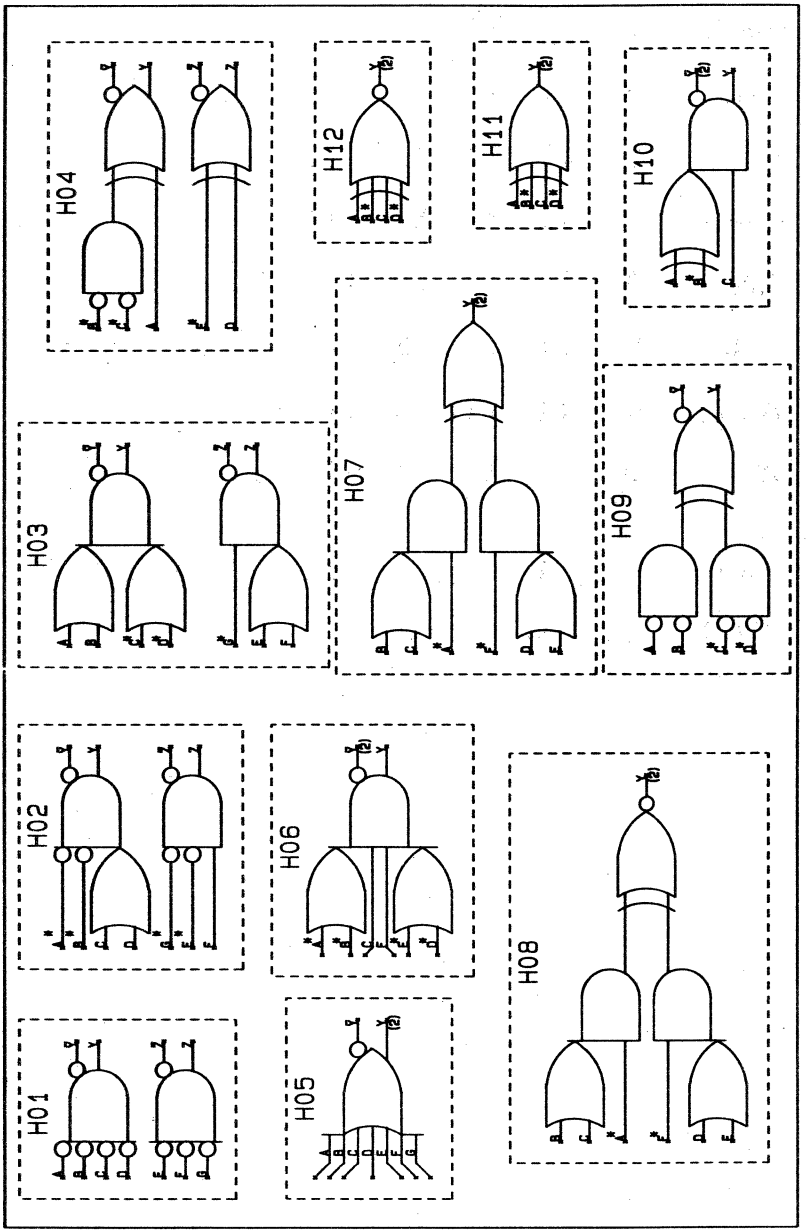
H18:	Y	A	B	C	D	E		
M19:	Y	Z	A	B	C	D	E	
	F	G	H					
M20:	Y	Y'	A	B	C	D	E	
	F	G	H	I	J	K	L	
M21:	Y	Y'	A	B	C	D	E	
	F	G	H	I	J	K	L	
M22:	Y	Y'	A	B	C	D	E	
	F	G	H	I	J	K	L	
M23:	Z	Y'	Y	Z'	A	B	C	D
	E	F	G	H	I	J	K	
M24:	Y	Y'	A	B	C	D	E	F
	G	H	I	J	K	L	M	N
M25:	Y	Y'	A	B	C	D	E	F
	G	H	I	J	L	M	N	
M26:	Y'	Y	A	B	C	D	E	
	F	G	H	I	J	K	L	
H27:	Y	Y'	A	B	C	D	E	
M28:	Y'	Z'	Y	Z	A	B	C	D
	E	F	G	H	I	J	K	L
M29:	Y'	Y	A	B	C	D	E	
	L	F	G	H	I	J	K	
M30:	Z'	Y	Z	Y'	A	B	C	D
	E	F	G	H	I	J	K	
H31:	Q	Q'	C1	C2	D	R		
M32:	Q	Q'	C1	C2	D0	D1	S	R

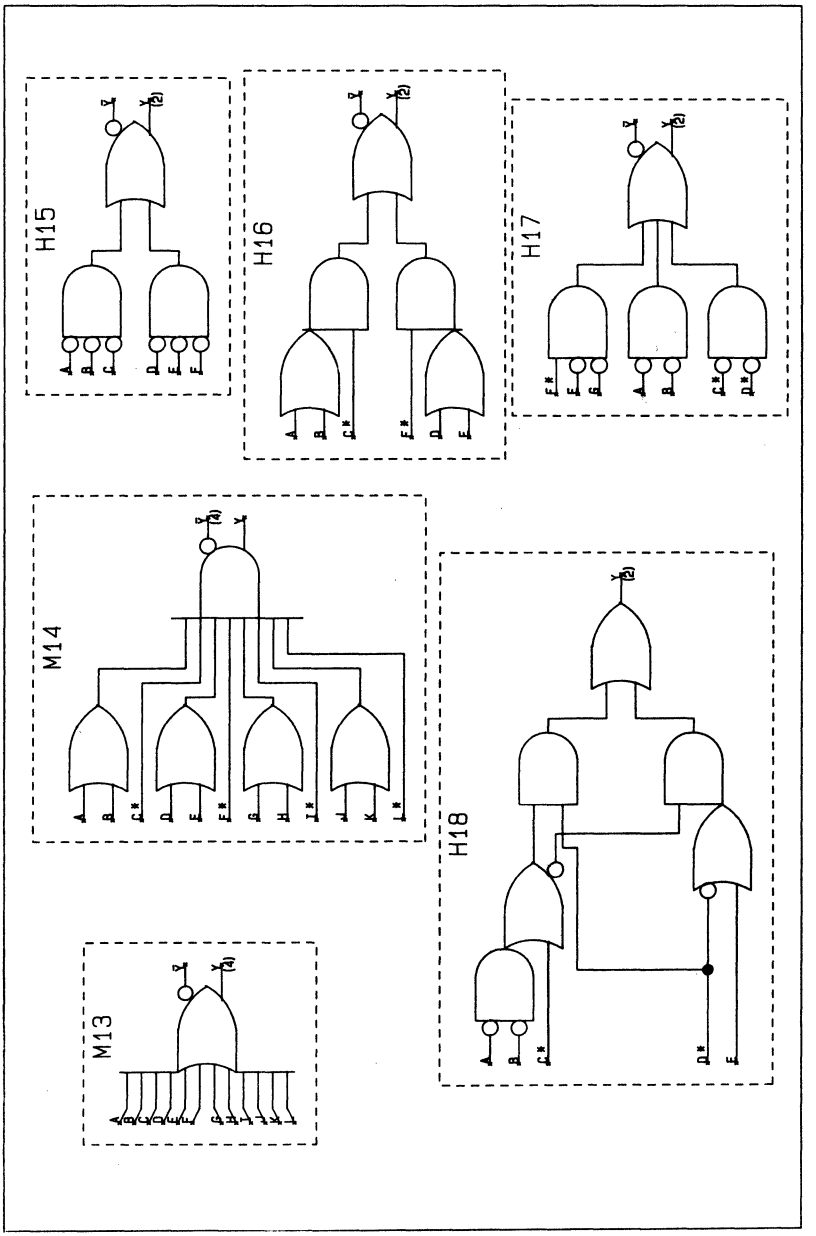
M50A:	CO	S	B1	B2	A	CI
M51:	S	CO	B1	B2	A	CI
M51A:	S	CO	B1	B2	A	CI
H52:	S	CO	B1	B2	A	CI
H52A:	S	CO	B1	B2	A	CI
M53:	P	H1	H0	CO	G	A0
	B0	A1	B1	CI		
H54:	CO	S	A1	A2	B1	B2
M55:	Y	A	B	C	D	E
	F	G	S			
M56:	Y	A	B	C	D	E
	F	G	H	I	S	
H57:	Y	A	B	C	D	
H58:	Y	A	B	C	D	
H59:	Y'	Y	Z	Z'	A	B
	C	D	E	F	G	H
H60:	Y	Y'	Z'	Z	A	B
	C	D	E	F	G	H
H61:	Y	Y'	Z'	Z	A	B
	C	D	E	F	G	H
H62:	Y'	Y	Z	Z'	A	B
	C	D	E	F		
H63:	Y'	Y	A	B	C	D
H64:	Y	Y'	A	B	C	D

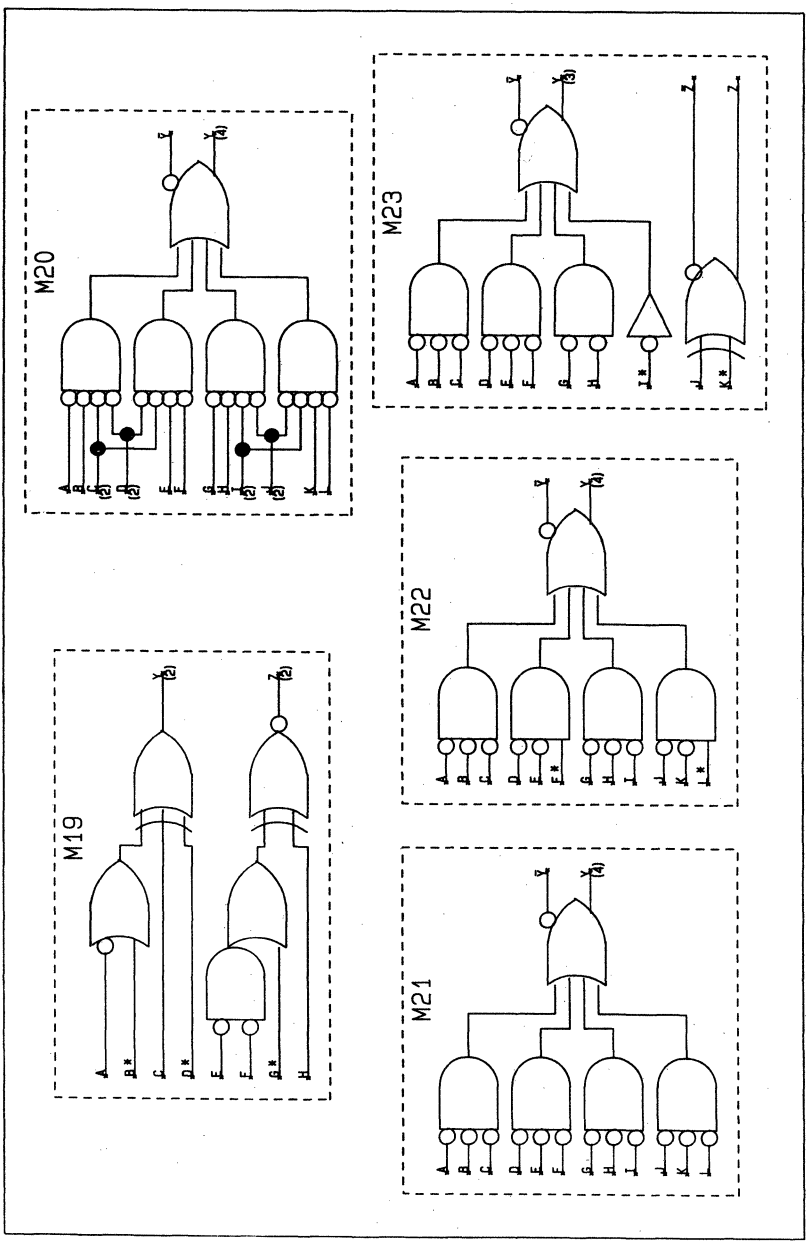
H65:	Y	Y'	A	B	C	D		
H66:	Y'	Y	A	B	C			
H67:	Q'	Q	D	E				
M68:	Y	A0	A1	A2	A3	S0	S1	
H69:	Y	Y'	A0	A1	SA			
H81:	Q	Q'	C+	C-	D+	D-	R1	R2
H82:	Q'	Q	C1	C2	D	R	S	
A01:	Y'	Y	A	B				
A02:	Y'	Y	A	B	C			
R01:	Y	A	B	C	E			
R02:	Y	A	B	C	E			
R03:	Y	A	B	C	E			
R04:	Y	A	B	C	E			
R05:	Y	A	B	C				
R06:	Y	A	B	C				
B01:	Y'	Y	A	B				
B02:	Y	Y'	A	B	C			
F01:	Y	A	B	C	E			
F02:	Y	A	B	C				
F03:	Y	A	B	C	E			

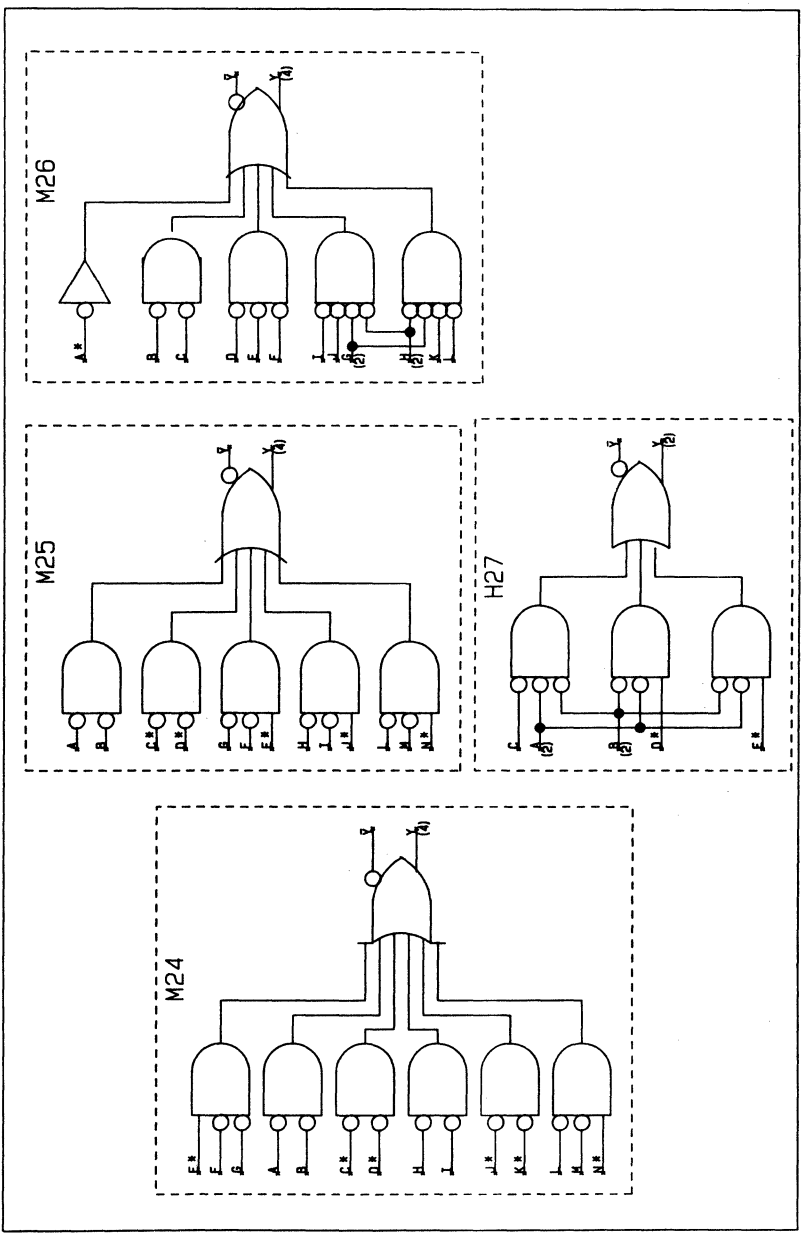
F04:	Y	A	B	C				
WAND2:	O	I1	I2					
WOR2:	O	I1	I2					
WOR3:	O	I1	I2	I3				
WOR4:	O	I1	I2	I3	I4			
WOR5:	O	I1	I2	I3	I4	I5		
WOR6:	O	I1	I2	I3	I4	I5	I6	
WOR7:	O	I1	I2	I3	I4	I5	I6	I7
WOR8:	O	I1	I2	I3	I4	I5	I6	I7
	I8							
PADIN:	OUT	IN						
PADOUT:	OUT	IN						

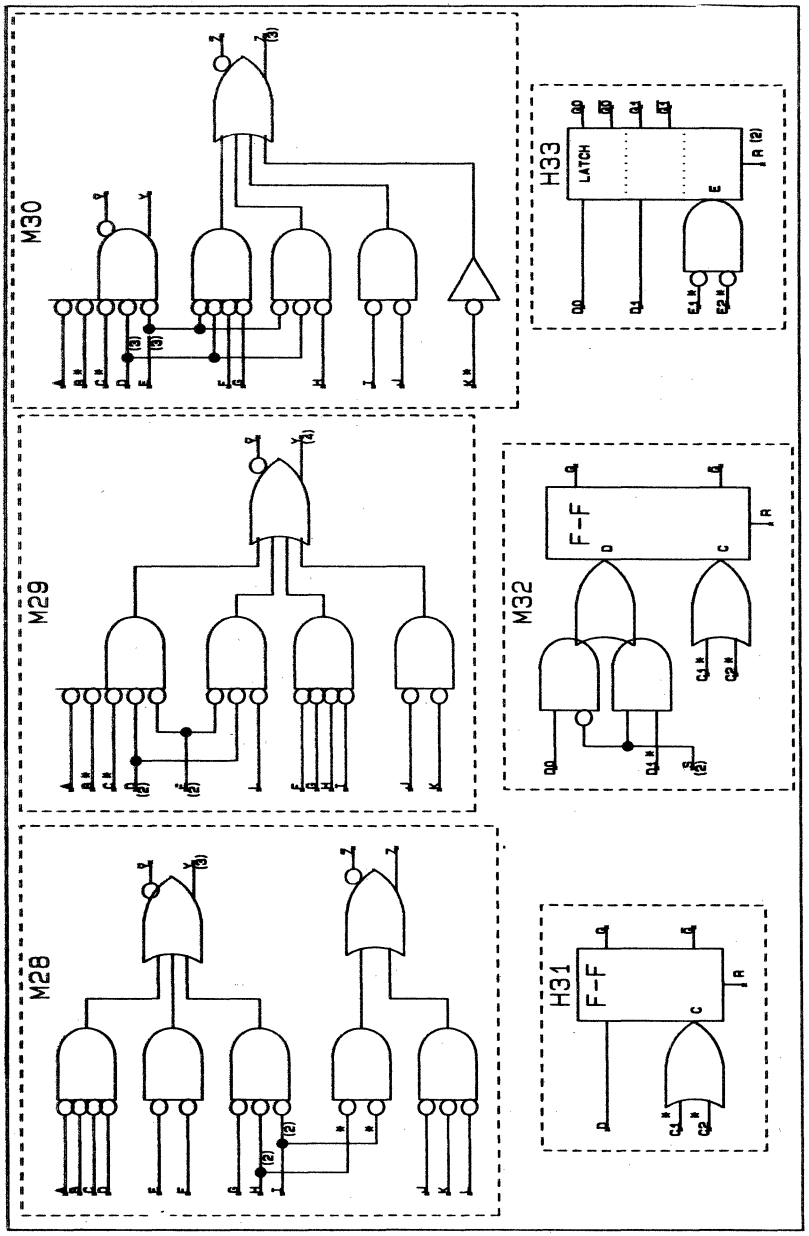
COMPONENT PLOTS

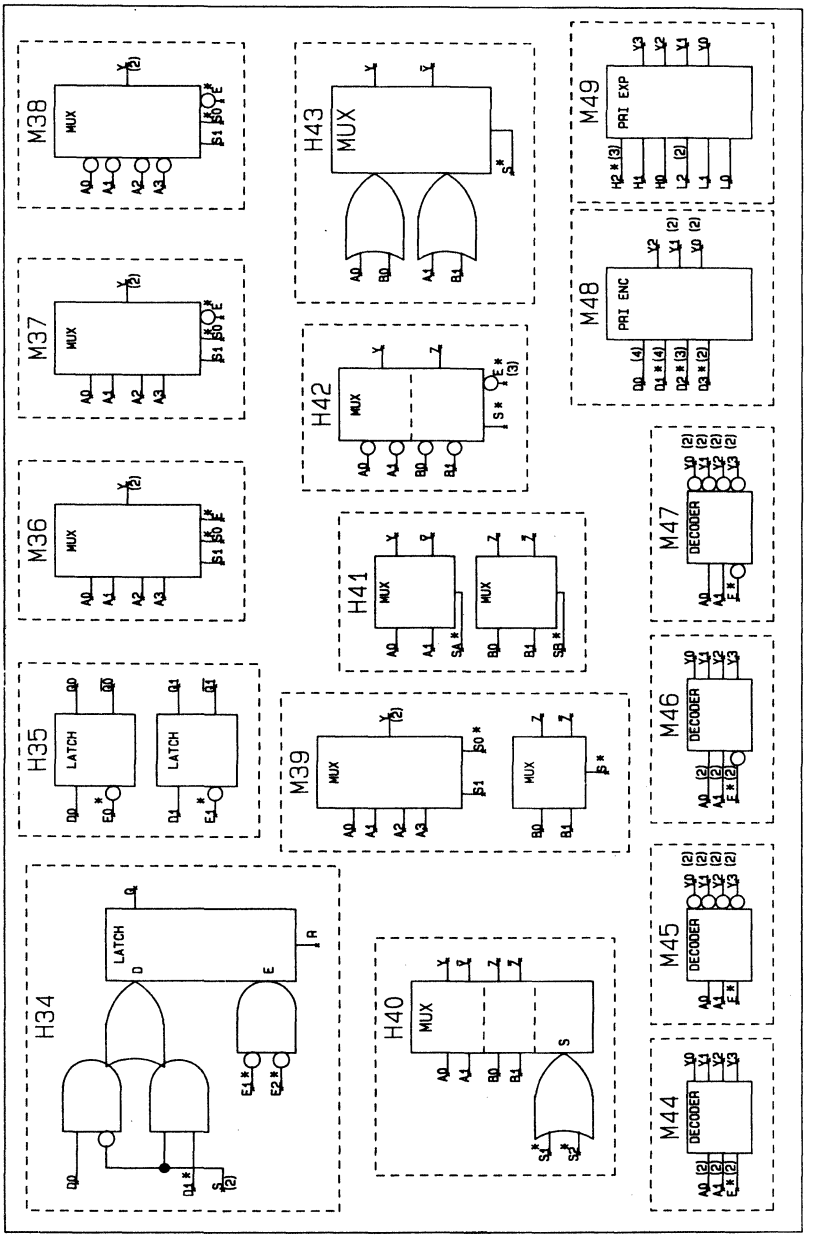


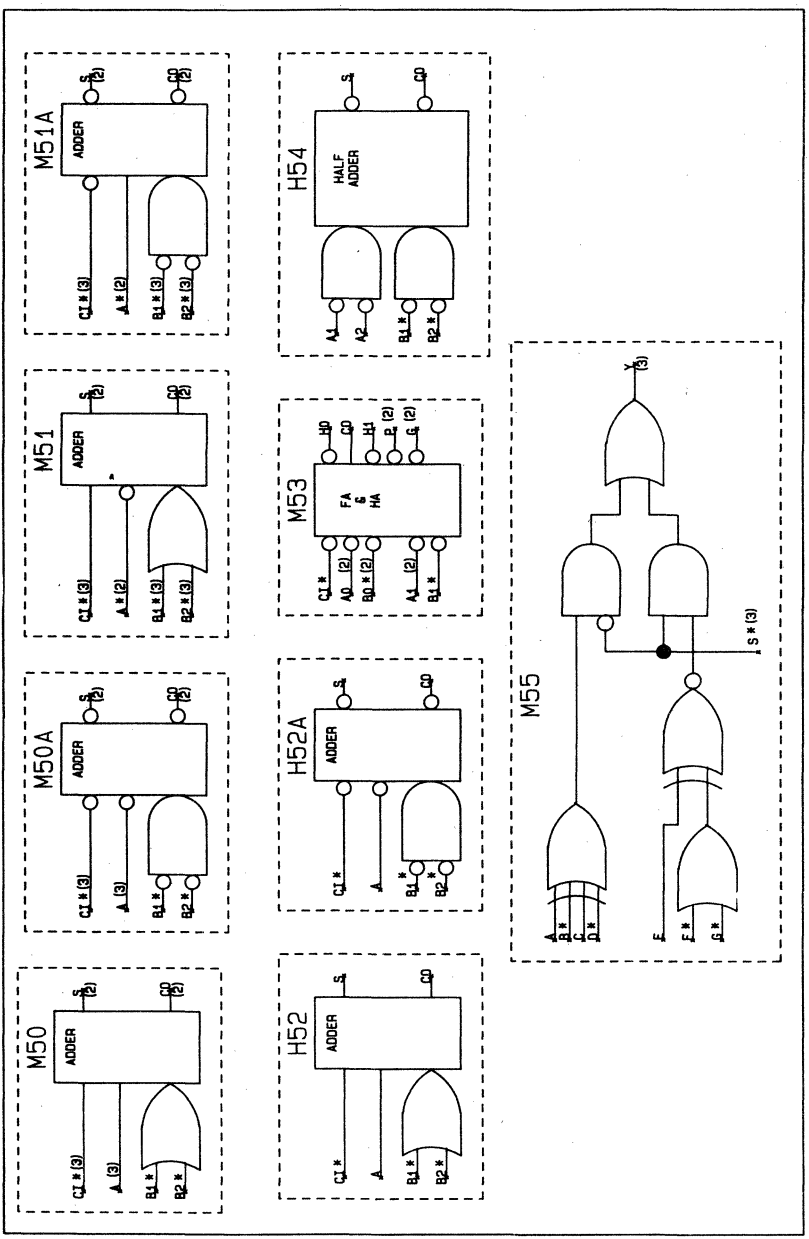

H15
H16
H17
M14
H18
M13

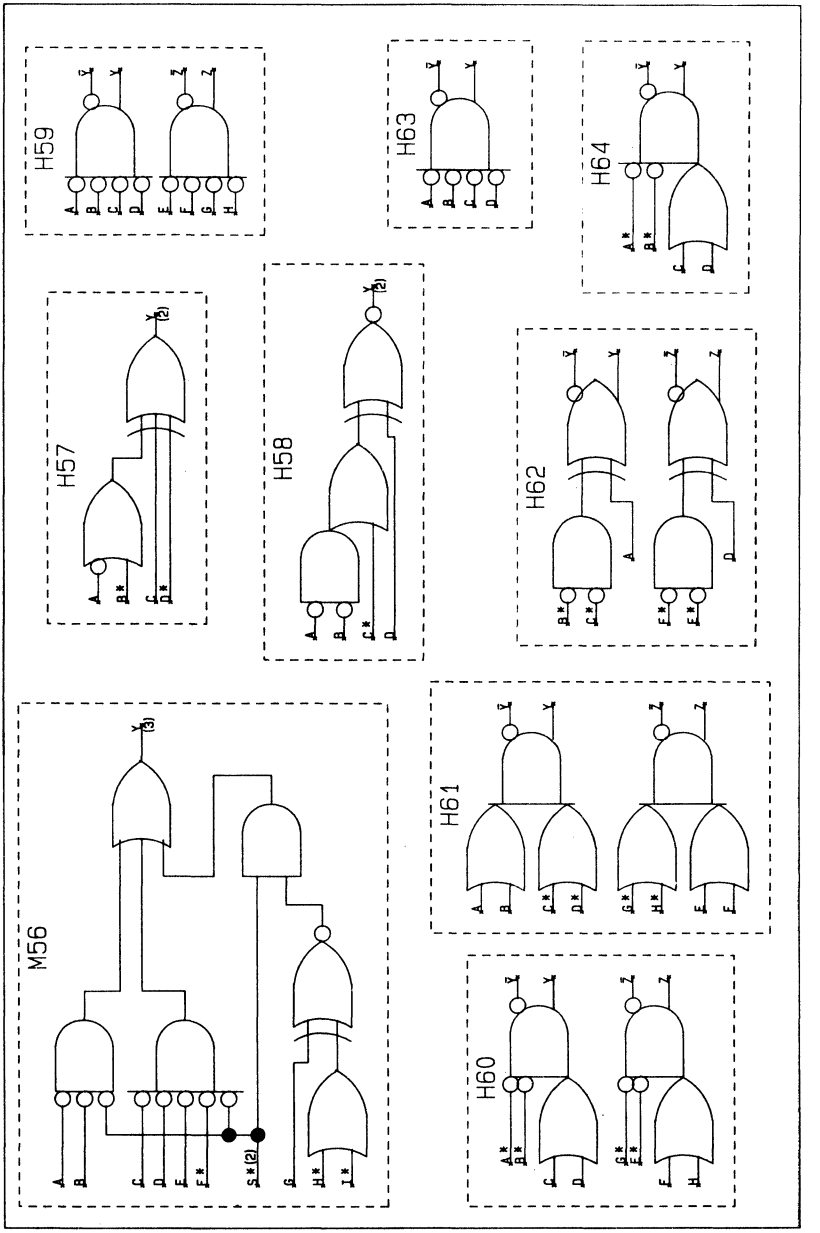

M20
M23
M22
M19
M21

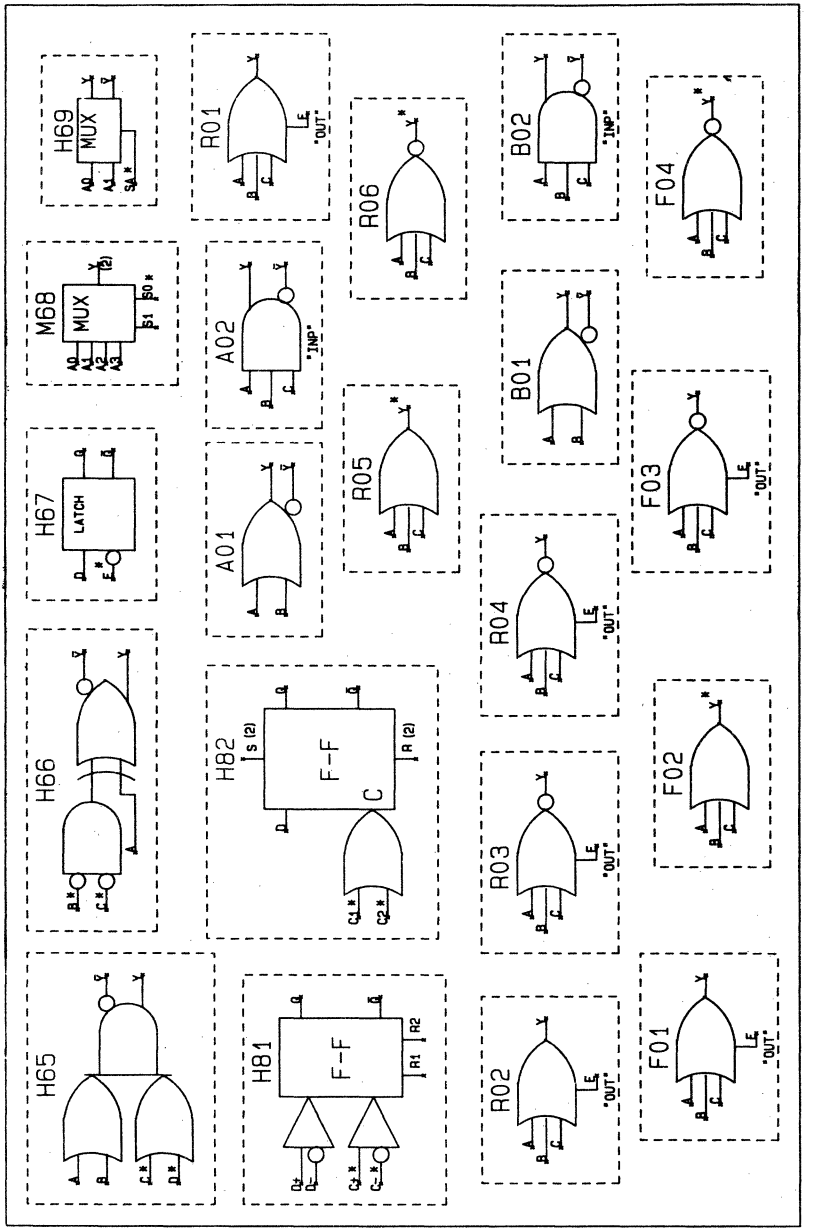

M26
M25
H27
M24

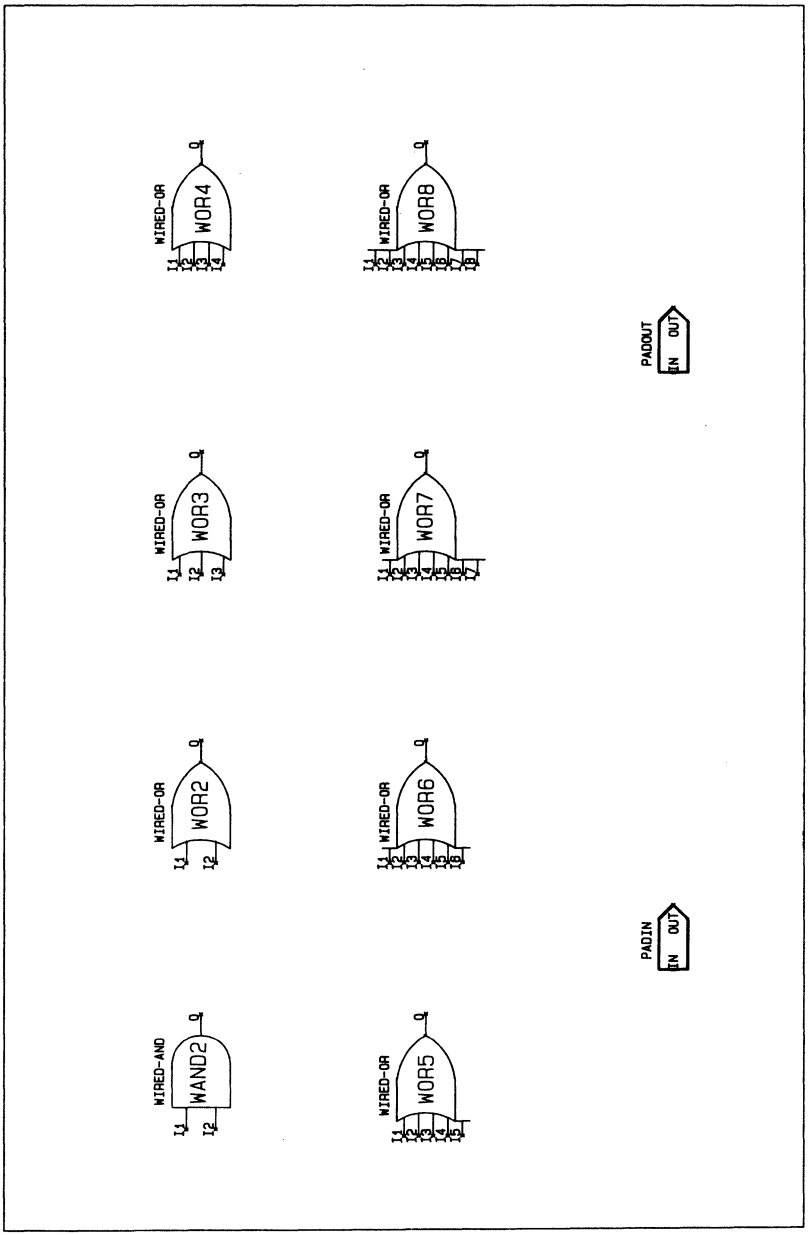

M30
M29
M28
H33
LATCH
M32
F-F
H31
F-F


M38
MUX
M37
MUX
M36
MUX
H35
LATCH
LATCH
H34
LATCH
H43
MUX
H42
MUX
H41
MUX
MUX
M39
MUX
MUX
H40
MUX
M49
PRI EXP
M48
PRI ENC
M47
DECODER
M46
DECODER
M45
DECODER
M44
DECODER


M51A
ADDER
S (2)
CO (2)
CI * (3)
A * (2)
B1 * (3)
B2 * (3)
M51
ADDER
S (2)
CO (2)
CI * (3)
A * (2)
B1 * (3)
B2 * (3)
M50A
ADDER
S (2)
CO (2)
CI * (3)
A (3)
B1 *
B2 *
M50
ADDER
S (2)
CO (2)
CI * (3)
A (3)
B1 *
B2 *
H54
HALF ADDER
S
CO
A1
A2
B1 *
B2 *
M53
FA & HA
H0
CO
H1
P (2)
G (2)
CI *
A0 (2)
B0 * (2)
A1 (2)
B1 *
H52A
ADDER
S
CO
CI *
A
B1 *
B2 *
H52
ADDER
S
CO
CI *
A
B1 *
B2 *
M55
Y (3)
S * (3)
A *
B *
C *
D *
E
F *
G *


H59
H63
H64
H57
H58
H62
M56
H61
H60


H69
MUX
M68
MUX
H67
LATCH
H66
H65
H82
F-F
H81
F-F
R01
A02
A01
R06
R05
R04
R03
R02
B02
B01
F04
F03
F02
F01


WIRED-OR
WOR4
WIRED-OR
WOR8
PADOUT
IN OUT
WIRED-OR
WOR3
WIRED-OR
WOR7
WIRED-OR
WOR2
WIRED-OR
WOR6
PADIN
IN OUT
WIRED-AND
WAND2
WIRED-OR
WOR5