PHILCO

A SUBSIDIARY OF *Ford Motor Company*

COMPUTER DIVISION

ELECTRONIC DATA PROCESSING SYSTEMS

PHILCO 1000 COMPUTER SERIES

TM-22

PHILCO 1000
COMPUTER SERIES

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PHILCO CORPORATION

A SUBSIDIARY OF Ford Motor Company

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TM-22

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SECTION 1

INTRODUCTION TO THE PHILCO 1000

GENERAL DESCRIPTION

The Philco 1000 Computer Series consists of a number of stored-program computer systems which process information on a character-at-a-time basis. A high-speed, solid-state data processing series, the Philco 1000 relieves the Philco 210, 211 or 212 computer systems of routine data handling functions such as input formatting and verification, file searching, conversion of punched-card information to tape, and editing of output for the printer.

Various models of Central Processors are available, each with magnetic core storage and selected input-output devices. The Central Processors are general-purpose digital computers which process data for the input-output devices shown in Figure 1.

Stored-Program Control

The Philco 1000 provides input-output control without costly individual control units. Stored-program logic controls both input-output operations and internal data handling. Editing and data manipulation by the stored program allows the selection and positioning of data characters individually, without plugboards or fixed format controls.

Non-Obsolescence

The asynchronous operation of the Philco 1000 Central Processor memory and control sections allows each section to proceed at its own speed, without being limited by a master clock. Future developments can thus be integrated into the system regardless of their timing cycles, without obsoleting the system as a whole. The character-oriented input-output interfaces also permit a wide variety of present and future input-output units to be handled.

Variable-Length Data

Data transfers are serial by character. The length of each field is designated by either the stored program or an End-of-Field character, thereby permitting optimum use of memory.

Simultaneous Operations

Two Central Processors may be included in the system, thereby permitting two simultaneous data processing operations.

Shared I-O Devices

Each Central Processor can access and share any input-output device connected to the system.

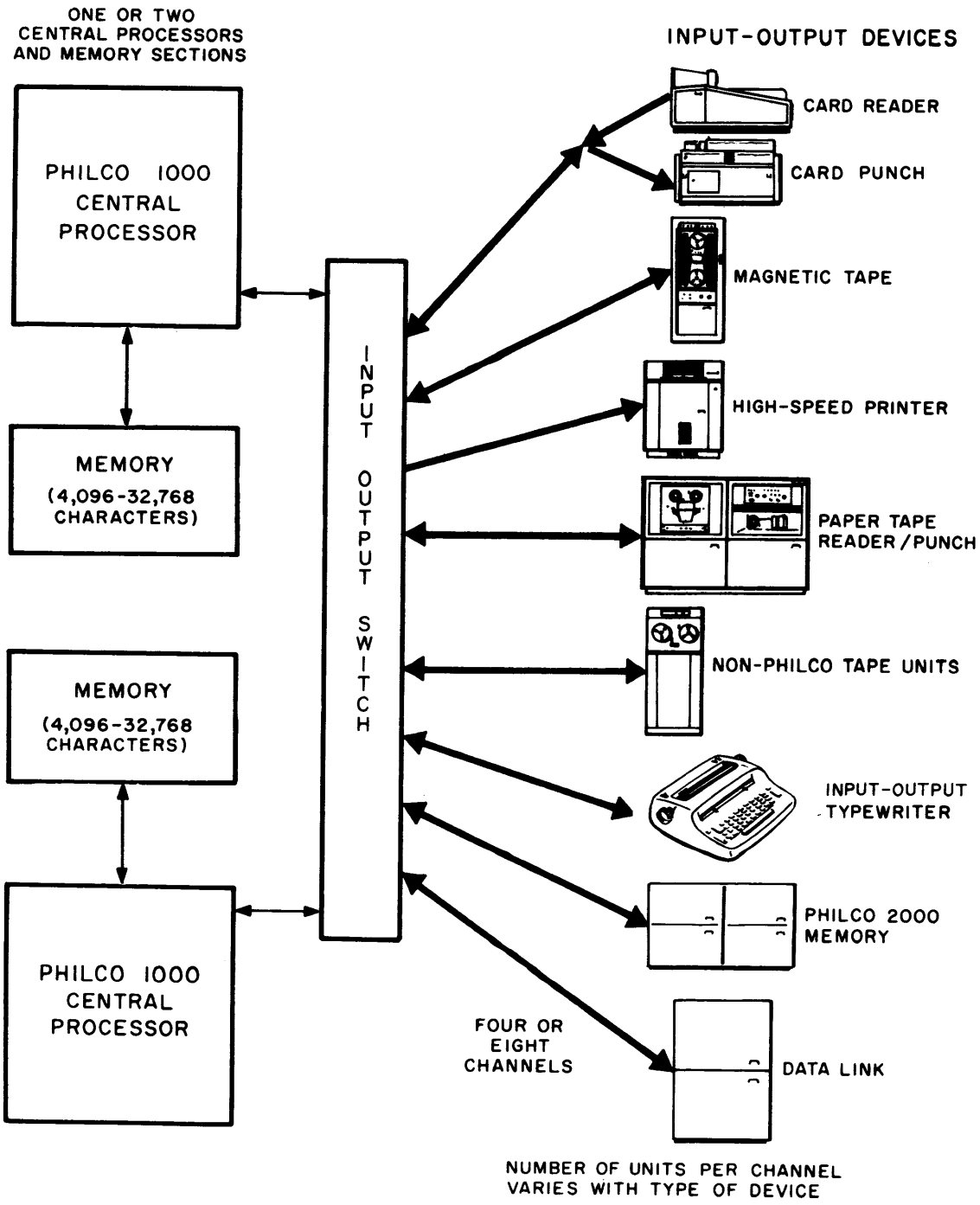

Figure 1. Philco 1000 System Configuration

SYSTEM CONFIGURATIONS

A computer system in the Philco 1000 series may consist of any of the following equipment:

- One or two Central Processor Units
- 4096, 8192, 16,384 or 32,768 character Magnetic Core Storage per Central Processor
- Input-Output Switch with four or eight input-output channels; each channel contains controls for a specific type of device
- The number of devices on each channel of the Input-Output Switch varies with the type of device
- Card Punches - 250 or 100 cards per minute
- Card Reader - 2000 cards per minute
- High-Speed Printer - 900 lines per minute, 120 columns
- 90,000 character per second Magnetic Tape Units
- 240,000 character per second Magnetic Tape Unit (available for Central Processors with 8192 character or larger memories)
- Paper Tape Reader - 1000 characters per second
- Paper Tape Punch - 60 characters per second
- Non-Philco Tape Units
- Input-Output Typewriter - Up to 15 characters per second
- Memory-to-Memory Controller (Philco 1000 - Philco 2000)
- Data Link

INPUT-OUTPUT SWITCHES

Each computer in the Philco 1000 series must contain one of the following Input-Output Switches equipped with either four or eight input-output channels. These units provide for the flow of information between the selected input-output devices and the memory.

1x4 and 1x8 Input-Output Switches

When one Central Processor is used, a 1x4 or a 1x8 Input-Output Switch must be specified. These contain four or eight input-output channels. Each channel may be connected to up to eight similar input-output units.

2x4 and 2x8 Input-Output Switches

If two Central Processors are used, a 2x4 or 2x8 Input-Output Switch must be specified. These contain four or eight channels, any two of which may be used to control two simultaneous transmissions, one transmission with each Central Processor.

MAGNETIC CORE STORAGE

The memory of any Central Processor provides program and data storage, plus input-output buffering. This memory is a random-access, coincident-current magnetic core storage with a total read/write cycle time of 5 microseconds for each character in a 4096 character memory. Overlapped accesses to characters automatically distributed to separate banks in memories larger than 4096 characters provide an effective read/write cycle time of less than 3 microseconds.

Each Central Processor has its own magnetic core memory. Each character is individually addressable and consists of six information bits, plus a parity bit which is checked each time the character is accessed.

Parity Checks

If a parity fault is detected while accessing an instruction, that Central Processor halts after instruction accessing is complete, and an indication of the Parity fault (P) is made on the Operator's Console. (See Section 5.) If a parity fault is detected while operands are being accessed, bit 6 of the Fault register is set and processing continues. (See Appendix A.) The Central Processor halts after completing the operation.

If a character with a parity fault is transmitted from an input-output device to memory, it will be stored in memory with the parity fault. Bit 6 of the Fault register will be set and processing will continue. (See Appendix A.) Bit 1 of the Fault register is set after an input-output device has detected a parity error.

SECTION 2
PROGRAM CONTROL

CENTRAL PROCESSOR ORGANIZATION

Each Central Processor in the Philco 1000 series contains a Program Control section and an Arithmetic section, as shown in Figure 2. The Arithmetic section contains no addressable registers, performing its operations by accessing and storing one character (6 bits) at a time, maintaining carries and intermediate results when necessary until the entire function specified by the instruction is completed.

Each instruction in machine language is four characters in length. The Program Control section decodes and sequences the instructions, and contains a number of addressable registers providing the designation of where data is located, how many characters are to be accessed by an instruction, and indications of the results of comparisons and fault tests.

Address Registers A, B, C, D

The address registers A, B, C, and D are 15-bit registers set by the program. *They are used by many instructions to indicate the location of the first character to be accessed.* The address portion of these instructions designates the number of characters to be accessed. In other instructions the address portion designates the location of the first instruction to be accessed. Associated with each of the address registers is an Adder which permits the incrementing or decrementing of the registers by an amount specified.

Direction Setting

Associated with each address register is a program-controlled direction setting indicator which designates whether the address register is to be incremented or decremented by one for each character accessed by reference to the address register.

Automatic Reset (R Option)

During execution of instructions which reference data by an address register, the address register is incremented or decremented for each character as it is accessed. Many instructions provide an option for automatic resetting of that register after execution of the instruction to its setting before the instruction was executed.

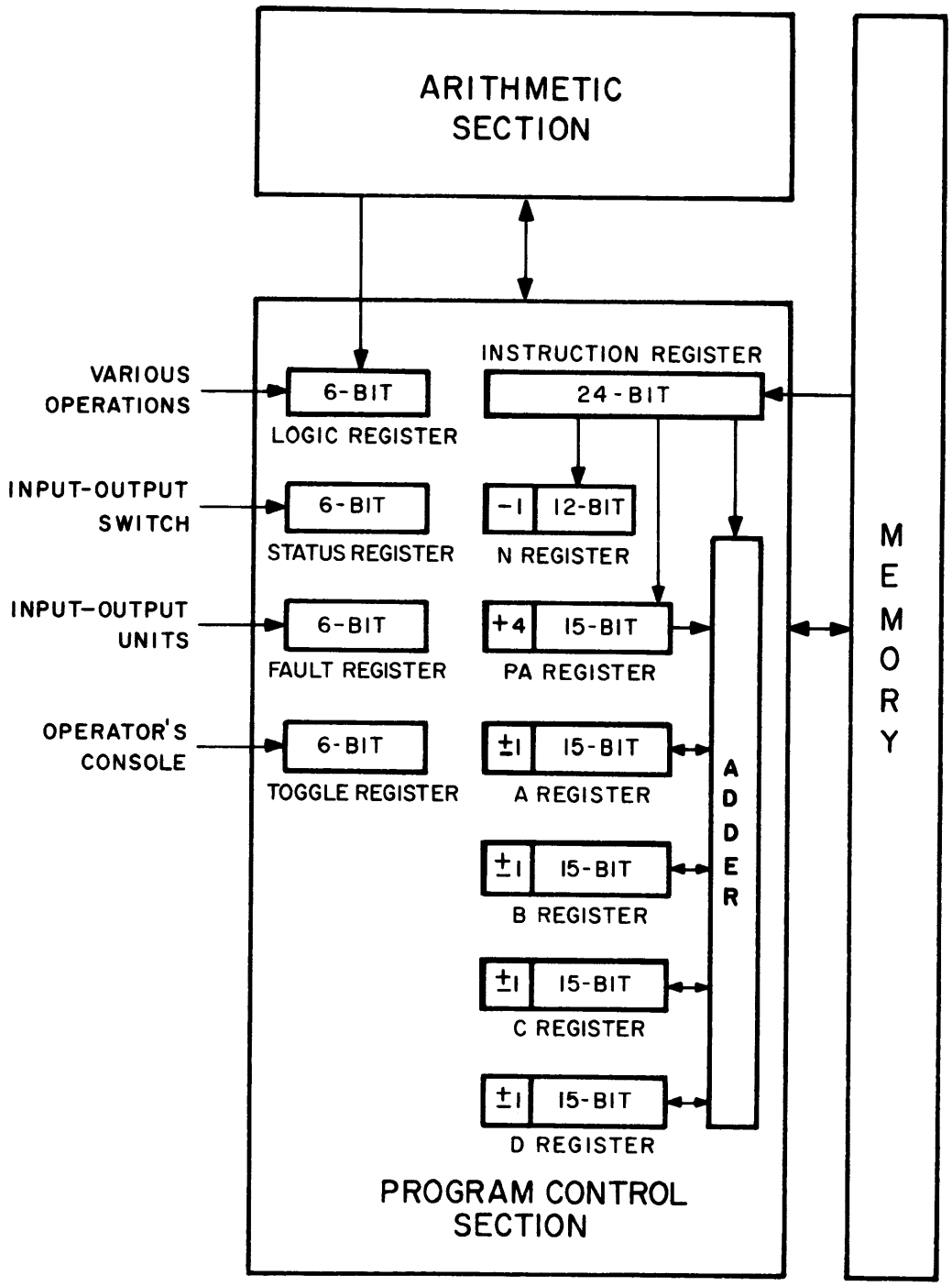

Figure 2. Philco 1000 Central Processor

Program Address Register (PA)

The location of the next instruction is contained in the 15-bit Program Address register, PA, at the completion of the current instruction access. When each instruction access is completed, this register is normally incremented by four. Certain instructions, such as the Jump and Skip instructions, permit the PA register to be replaced or incremented by other values, providing for a program branch at such points.

N Register

The N register is a 12-bit register used to count the number of characters being accessed by an instruction. The maximum number of characters to be accessed may be specified in the instruction itself, particularly those instructions which use the address registers (A, B, C, and D) to specify the starting address.

N Register Option

An option available with many instructions permits the instruction to designate that the maximum number of characters to be accessed is already in the N register. When this option is used, the N register is reset at the completion of the instruction to its initial setting.

If the N register option is selected for an instruction which allows less than 12 bits to specify the number of characters, only those low-order bits which the instruction permits are used.

Variable-Length Fields, End-of-Field Character

Less than the maximum number of characters, designated in the instruction or the N register, may be accessed by certain instructions if an End-of-Field (octal 77) character is detected. This is counted as a character accessed, but is not otherwise involved in the operation except to stop it from proceeding further. At this point, the N register will indicate the number of characters remaining to be accessed. Control will pass to the next instruction with this value in the N register.

Filler Character

The Filler character (octal 32) is used to fill out blocks of data on magnetic tape where the number of valid characters specified by the output instruction is less than the number of characters in the block or record size of the tape being used. It is counted as a character accessed, but is not otherwise involved in the operation.

Other Registers L, F, S and T

The Program Control section of each Central Processor also has four 6-bit registers: a Logic register (L), a Fault register (F), a Status register (S), and a Toggle register (T). The functions of

these are described below. Additional details concerning the first three registers are given in Appendix A.

- Logic (L) Register - Contains information of the results of operations performed on data fields and information on any illegal characters that may be detected in converting from Hollerith to Philco code and from Binary-Coded Decimal characters to binary code.

- Fault (F) Register - Contains fault information on the performance of a specific input-output device.

- Status (S) Register - Indicates why a specified input-output device is not available to the Central Processor.

- Toggle (T) Register - Indicates the setting of toggle switches on the console, providing a six-bit (one character) input to the program.

Register Length

Address registers A, B, C, and D and the Program Address (PA) register are always 15 bits in length and operate modulo 32,768 (regardless of the size of memory). They will count, therefore, beyond the maximum memory address in Central Processors with memory sizes of less than 32,768. However, only the appropriate number of bits are used to address characters within the available memory.

SECTION 3
PHILCO 1000 INSTRUCTIONS

INSTRUCTION FEATURES

Any computer system in the Philco 1000 series can perform the operations specified by the following types of instructions. Additional instructions are described with the descriptions of specific computers in the Philco 1000 series.

- Program Control - Set, modify, and store the contents of various Program Control section registers:
  LOAD, TAB, SAVE, JMP, HLT, NOP
- Data Handling - Move, convert, fill with, and shift characters:
  COPY, MOVE, HTP, PTH, BTD*, DTB*, FILL, SHL, SHR
- Arithmetic and Logical Operations - Perform arithmetic and Boolean functions:
  ADD, SUB, MPY*, DIV*, AWC, OR, EX, EXZ, INC, DEC
- Data Testing - Compare and test data fields and registers:
  COMP, SKE, SKNE, SKAN, SKAL
- Input-Output Operations - Connect and disconnect Central Processor and input-output units, transmit data:
  CON, DIS, specific input-output instructions

Instruction Format

Each instruction in machine language consists of four 6-bit characters, the first two of which generally indicate the function to be performed, the address registers to be used, and the options selected. The last two characters generally designate, in binary, the number of characters to be accessed by the instruction or, in some cases, an address or a value to be placed in a specified address register. In this latter case, the last three bits of the second character are also used to make up the 15 bits required for an address.

The instructions for the Philco 1000 are written on the standard 80-column Philco Coding Form (Figure 3) with the FUNCTION, REGISTERS, and OPTIONS specified in the COMMAND columns (17 to 24). The remainder of the required information is written in the ADDRESS and REMARKS columns (25 through 80).

* *Optional*

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PHILCO CODING FORM

Page.....of.....

Program:	Programmer:	Date:

IDENTITY AND SEQUENCE	L	LOCATION	COMMAND	ADDRESS AND REMARKS
1 2 3 4 5 6 7 8	9	10 11 12 13 14 15 16	17 18 19 20 21 22 23 24	25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80

TF-25

Figure 3. Philco Coding Form

The FUNCTION is written as specified in the instruction charts.

The REGISTERS are designated as follows:

- Address Registers - A, B, C, and D
- N Register - N
- Logic Register - L
- Fault Register - F
- Status Register - S
- Toggle Register - T

The OPTIONS which may be specified are as follows:

- Forward Direction Setting - F
- Backward Direction Setting - B
- Reset Address Register - R
- N Register Option - N
- Reset Address Register *and* N Register Options - X

The ADDRESS field generally contains a decimal value, the range of which, for each particular instruction, is specified on the instruction charts. In some cases, an additional value or character is required, specified in these charts as "constant."* This constant may be any of the Philco characters designated in Appendix B.

The time required to access and execute each instruction is described in Appendix C.

The machine language code for each Philco 1000 instruction is listed in Appendix D in octal. Each instruction is four characters in length; the characters are designated C1, C2, C3, and C4.

LOAD Instructions

The LOAD instructions transmit a value to the N register or an address register.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
LOAD	A, B, C, or D	F or B	0-32,767	Transfers the address field to the designated address register and specifies the direction setting. If the option is omitted, F is assumed.
LOAD	N		0-4095	Transfers the address field to the N register.

* *The assembly program which translates the mnemonic codes shown into machine language provides several means of expressing this constant and other types of constants.*

The option designates the setting of the direction indicator. F (or omission of the option) indicates that the address register will be set to increment once for each character accessed by subsequent instructions that use the address register to locate a data field; B indicates that it will decrement.

TAB Instructions

The TAB instructions change the absolute value of a specified address register by adding or subtracting a designated value to or from the register. They do not change the direction setting of the address register.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
TAB	A, B, C, or D	F or B	0-32,767	Modifies a specified address register by adding or subtracting the address field. Does not change the direction setting of the address register.

SAVE Instructions

The SAVE instructions store the contents of a specified register into memory. If the specified register is an address register, its contents will be stored into three consecutive character locations, starting at the location specified in the address field. The three high-order bits of the first character stored are set to zero; the low order bits of this character are set by the address register.

If the specified register is the N register, its contents will be stored into two consecutive characters starting at the location specified in the address field. If the specified register is the L, F, S, or T register, its contents will be stored into the character specified by the address field.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
SAVE	A, B, C, D, N, L, F, S, or T		0-32,767	Stores the contents of a specified register in memory starting at the location designated by the address field.

Jump Instructions

The Jump instructions change the sequence of instructions by placing an address in the Program Address (PA) register. The next instruction to be executed starts at this address.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
JMP	A, B, C or D		0-32,767	Places the address of the next sequential instruction following the JMP instruction in the specified address register. The address part of this JMP instruction is then placed in the PA register and is used as the address of the next instruction.
JMP			0-32,767	Places the address field of this instruction in the PA register without affecting any other register. This address is used as the address of the next instruction.
JBT			0-32,767	Causes the computer to halt if the console JBT switch is ON; pressing the CONT (Continue) button on the Operator's Console then allows this instruction to be executed as a JMP instruction. If the JBT is OFF, this instruction acts as a JMP.

HLT, NOP Instructions

The HLT instruction is used to stop the processor. The CONT (Continue) button on the Operator's Console can then be used to restart the processor and execute the next instruction.

The NOP instruction steps the program to the next consecutive instruction, increasing the PA register by four.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
HLT				Stops the Central Processor.
NOP				Steps the program to the next instruction. (No Operation)

COPY Instructions

The COPY instructions transmit a specified number of characters from one area of memory to another. The starting addresses of the transmitting and receiving areas are specified by a pair of address registers.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
COPY	A, B, C, D (any two)	R, N, or X	0-4095	Transmits the number of characters specified from one area to another.

This instruction initially clears the Logic register. When the instruction is complete, bit 5 of the Logic register is set to one if the field moved consisted entirely of zeros. Two address registers must be selected, the first designating the transmitting area, the second the receiving area.

MOVE Instructions

The MOVE instructions transmit a specified number of characters from one area of memory to another. Two address registers must be selected. The first specifies the sending area, the second the receiving area.

MOVE instructions are similar to the COPY instructions, except that they check for Filler (octal 32) and End-of-Field (octal 77) characters. A Filler character will not be transmitted. It will be counted as a character moved from the transmitting area but not as received in the receiving area. An End-of-Field character will be counted, but not moved. It will stop the transmission, and the number of characters remaining to be transmitted will be in the N register after transmission is stopped.

This instruction initially clears the Logic register to zero. After the instruction is completed, bit 5 of the Logic register is set if the field received was all zeros. Bit 4 of the Logic register is set if an End-of-Field character was encountered.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
MOVE	A, B, C, D (any two)		0-4095	Transmits the number of characters specified from the area designated by the first register to the area designated by the second. Filler characters are sensed but not moved. An End-of-Field character is not moved and stops the transmission.

FILL Instructions

The FILL instructions place a specified six-bit configuration (one character) into 0 to 4095 consecutive character locations, starting at the location designated by the address register. The six-bit configuration (FILL character) is specified in the address portion of the instruction.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
FILL	A, B, C, or D	R	Constant, 0-4095	Fills the number of characters specified, starting at the location designated by the address register selected, with the character specified by the constant.

Shift Instructions

The Shift instructions perform a one-bit right or left shift of a specified number of characters. The starting address of the first character to be shifted is specified by an address register. The location of each sequential character is designated by the specified address register.

In the first character shifted, the vacated position is filled with a zero. The bit shifted out of the first and subsequent characters is placed in the vacated position of the following character. The bit shifted out of the last character is lost.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
SHL	A, B, C, or D	R, N, or X	0-4095	Shifts the number of characters specified left one bit position.
SHR	A, B, C, or D	R, N, or X	0-4095	Shifts the number of characters specified right one bit position.

The Logic register is initially cleared by these instructions. If the bit shifted out of the last character is a one, bit 6 of the Logic register is set.

Logical Operation Instructions

The logical bit-by-bit operations include the Exclusive OR (AWC), Inclusive OR (OR), Logical Multiply (EX), and Logical Complimented Multiply (EXZ). These operations are always performed on one field starting at the character designated by address register A, and a second field starting at the character designated by address register B. The result is placed in memory starting at the character designated by address register C. The length of each operand and the result are specified in the instruction or in the N register.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
AWC		R, N, or X	0-4095	Adds the number of characters specified without carry; always $A \wedge B \longrightarrow C$.
OR		R, N, or X	0-4095	Performs inclusive OR operation; always $A \vee B \longrightarrow C$.
EX		R, N, or X	0-4095	Performs logical bit-by-bit multiplication; always $A \cdot B \longrightarrow C$.
EXZ		R, N, or X	0-4095	Performs logical bit-by-bit multiplication using the one's compliment of the B field; always $A \cdot \bar{B} \longrightarrow C$.

The results of each operation, assuming one-character fields, are as follows:

FIELD	INSTRUCTION			
	AWC	OR	EX	EXZ
A	001100	001100	001100	001100
B	000101	000101	000101	000101
C (Result)	001001	001101	000100	001000

These instructions initially clear the Logic register. After execution of the instruction, bit 5 of the Logic register is set if the result is a field of all zeros.

Arithmetic Instructions

The following arithmetic instructions perform binary addition, subtraction, multiplication* and division.* The operations are performed on fields of a designated length. During ADD and SUB instructions, the Arithmetic section accesses a pair of six-bit characters (one from each operand) at a time. Each six bits of the result are automatically stored in memory before the next pair of characters are accessed. Any indication of carries or borrows is maintained in the Arithmetic section to provide an adjustment for this next pair of characters.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
ADD		R, N, or X	0-4095	Performs binary addition on the number of characters specified; always A + B ⟶ C.
SUB		R, N, or X	0-4095	Performs binary subtraction on the number of characters specified; always A - B ⟶ C.
MPY		R, N, or X	0-63	Performs binary multiplication on the number of characters specified; always A x B ⟶ C.
DIV		R, N, or X	0-63	Performs binary division on the number of characters specified; always A ÷ B ⟶ C, and remainder in D.

** Optional*

The following points should be noted when performing arithmetic operations:

- Address registers A and B always specify the least significant six bits of the operands.
- Sequential groups of six bits are accessed according to the direction setting of the appropriate register.
- Each sequential group of six bits is always operated on with its rightmost bit considered least significant.
- Results are always stored as specified by address register C. In the case of division, the remainder is stored starting with the least significant digit in the location specified by address register D. The remainder will always be the number of characters specified in the address part of the instruction or by the N register if the N option is used.
- The least significant group of six bits is stored first, except for the DIV (Divide) instruction, which stores the most significant six bits of the quotient first.

The Logic register is initially cleared to zero by the Arithmetic instructions. If a result is all zeros, bit 5 will be set. An attempt to carry or borrow beyond the number of characters specified will result in bit 6 of the Logic register being set. The character following the last character will not be affected. If the attempt was made in a subtraction operation to borrow from a character outside the designated field length, the borrow would be simulated. If a division would result in a quotient greater than can be contained in the specified number of characters, the division will not take place and bit 6 of the Logic register will be set.

Increment Decrement Instructions

The following instructions increment or decrement a field by adding or subtracting one binary digit. The least significant six bits are specified by an address register designated in the instruction. A carry, if any, will take place through the number of characters specified, accessed according to the direction setting of the designated register. No character beyond the field length will be affected.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
INC	A, B, C, or D	R, N, or X	0-4095	Increments the specified number of characters by one bit.
DEC	A, B, C, or D	R, N, or X	0-4095	Decrements the specified number of characters by one bit.

The Logic register is initially cleared by these instructions. Bit 5 will be set if the result is a field of zeros. Bit 6 will be set if overflow occurs.

Compare Instructions

These instructions compare a specified number of characters of two fields located by two address registers designated in the instruction. The comparison assumes both fields to be positive binary integers. The first characters of the fields to be accessed are assumed to be the most significant characters. The number of characters specified in the address applies to both fields.

The Logic register is initially cleared by this instruction. Bit 1 is set if the first value is greater than the second, bit 2 if they are equal, and bit 3 if the first value is less than the second.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
COMP	A, B, C, D (any two)	R, N, or X	0-4095	Compares two fields with lengths and locations specified by the instruction. Sets the Logic register according to the results of the comparison.

Skip Instructions

The Skip instructions test the contents of a specified register or memory location for a six-bit configuration designated in the instruction. If the conditions designated by the specific Skip instruction exist, the number of characters specified will be skipped. This value may be from 0 to 63. If the condition is not met, the next instruction following the Skip will be executed.

If the A, B, C, or D register is specified, the six-bit configuration given will be compared against the character in memory designated by the specified address register. If the Logic, Fault, Status, or Toggle register is specified, the contents of that register are tested. The reset option may be used if a character in memory is being tested, but *may not* be used when testing the contents of the Logic, Fault, Status, or Toggle registers.

If the value represented by the constant is zero, the skip will not take place for the SKAN instruction and will always take place for the SKAL instruction.

The HTP and PTH instructions translate a specified number of characters from six-bit Philco code to 12-bit Hollerith code (PTH) or from Hollerith code to Philco code (HTP). Two address registers must be selected. The first designates the sending field, the second designates the receiving field.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
SKE	A, B, C, D, L, F, S, or T	R (A, B, C, D only)	Constant, 0-63	Skips the number of characters designated (by the second parameter in the Address Field) if the six bits (representing the character in the constant) are equal to the six bits in the designated memory location or register.
SKNE	A, B, C, D, L, F, S, or T	R (A, B, C, or D only)	Constant, 0-63	The skip is performed only if the six bits of the character in the constant are not equal to the six bits in the designated memory location or register.
SKAN	A, B, C, D, L, F, S, or T	R (A, B, C, or D only)	Constant, 0-63	Skips only if any one bit of the character in the constant is matched by its respective bits in the designated memory location or register.
SKAL	A, B, C, D, L, F, S, or T	R (A, B, C, or D only)	Constant, 0-63	Skips only if all one bits in the constant are matched by all one bits in the designated memory location or register.

Translation Instructions

In Philco-to-Hollerith translation, twice the specified number of characters is stored. In Hollerith-to-Philco translation, one-half the specified number of characters is stored. In an HTP operation, if the specified number is odd, one additional character will be accessed.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
HTP	A, B, C D (any two)		0-4095	Translates the number of characters specified from Hollerith to Philco code.
PTH	A, B, C, D (any two)		0-4095	Translates the number of characters specified from Philco to Hollerith code.

The HTP instruction clears the Logic register. If an illegal Hollerith code is received for translation, bit 4 of the Logic register will be set; an indeterminate Philco character will be produced; and the operation will continue.

Conversion Instructions*

The BTD instruction is used to convert a binary field in a specified number of character locations to six-bit Binary-Coded Decimal (BCD) characters. Two address registers must be selected. The first designates the most significant digit of the binary field; the second designates the least significant digit of the BCD field. The BCD field resulting from the conversion may be as much as twice the number of characters specified in the instruction.

The DTB instruction is used to convert a specified number of BCD characters to a binary field. Two address registers must be selected. The first designates the most significant digit of the BCD field, the second designates the location of the least significant six bits of the binary field. The binary field resulting from the conversion may be as little as half the number of characters specified. Note that address register D may not be specified. The number of characters specified in the address part of the instruction in the area designated by address register D may be altered by the conversion.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
BTD	A,B,C,D (any two)	R, N, or X	0-63	Converts a specified number of characters from binary to BCD.
DTB	A, B, C (any two)	R, N, or X	0-63	Converts a specified number of characters from BCD to binary.

Both instructions initially clear the Logic register. If a non-numeric BCD character is detected in a DTB operation, bit 4 of the Logic register will be set and the operation ends. In both BTD and DTB operations, bit 5 is set if the resulting field is all zeros.

* *Optional*

SECTION 4
INPUT—OUTPUT OPERATIONS

CHANNEL ASSIGNMENTS

Up to eight similar devices can be connected to each of the four or eight input-output channels on the Input-Output Switch, numbered 0 - 7. The normal assignment of input-output devices is as follows:

- Channel 0: Card Reader, Card Punch
- Channel 1: High-Speed Printer
- Channel 2: Philco 90,000 character per second Magnetic Tape Units
- Channel 3-7: Any selected devices

INPUT-OUTPUT TRANSMISSIONS

Two Central Processors in a Philco 1000 system may both be connected to the same Input-Output Switch and share connected input-output devices. An interlock prevents one processor from addressing a device currently connected to the other. To reserve a unit for its own use, a processor issues a CON (Connect) instruction to the device. If the device is available, a connection is made, and the next sequential instruction is skipped. Otherwise, an indication as to why the connection could not be made is set in the Status register and the next sequential instruction is executed. Once a connection has been made by an instruction, the program can issue input-output instructions to that, and only that device. The other Central Processor cannot issue instructions to that device or any device on that channel until the connection is broken.

The completion of an input-output instruction leaves the device connected to the processor. The DIS (Disconnect) instruction is used to break the connection between a processor and an input-output device.

The starting address of most input-output transmissions is specified by address register D, which is unchanged upon completion of the transmission. When cards are punched, checking is performed using address register C.

Connect and Disconnect Instructions

These instructions are used to connect (CON) or disconnect (DIS) an input-output device and a Processor. Only one device may be connected to a Processor at one time.

The CON instruction clears the Status register and the Fault register. If the connection is not made, the appropriate bits 1-3

of the Status register will be set and the next instruction executed. If the connection is made, the next sequential instruction is skipped.

The DIS instruction does not clear any register or set any bits. If the processor is not connected to a device, the DIS instruction acts as a NOP (page 3-5).

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
CON			Channel number, Device number.	Connects the Central Processor to the designated device on the channel specified.
DIS				Disconnects the Central Processor from any connected input-output device and channel.

Input-Output Instructions

The processor may issue the input-output instructions to a specific device once a CON instruction has made a connection between the Central Processor and the device. After any of the input-output instructions has been issued, the Processor will not go on to the instruction following until the specified transmission is completed. As soon as the number of characters specified by the instructions has been transferred, the next instruction is executed even though there may be non-transmission portions of the input-output function still being performed. If the transmission cannot be completed, the Central Processor waits at the input-output instruction until the operator intervenes.

Fault Testing

The Fault register is cleared prior to any input-output instruction. Faults are indicated in the Fault register following the completion of the transmission portion of an input-output instruction.

The Fault register may be tested by a Skip instruction, or stored in memory by a SAVE instruction, as long as the input-output device is still connected. If the non-transmission portion of an input-output function is not complete, the processor will wait at the Skip or SAVE instruction until it is completed.

Punched-Card

The Punched-Card Reader and Card Punch are used to transmit and record information exactly as it appears in memory. The Card Reader operates at the rate of 2000 cards per minute, the Card Punches operate at 250 or 100 cards per minute.

Each column on the card is represented by two consecutive characters (12 bits, one for each row) in memory. If the card read

in (or to be punched) is in Hollerith code, conversions between this code and Philco code may be performed internally by the HTP and PTH instructions. (See page 3-11) The corresponding Hollerith and Philco codes are shown in Appendix B.

The Punched-Card instructions include the following:

- Read a Card and Feed the Next Card - RCDF
- Read a Card - RCD
- Punch a Card - PCD
- Punch a Card and Check Previously Punched Card - PCDCK
- Check Previously Punched Card - CKCD

The storing address of the 160 characters (80 columns) to be read or punched is specified in address register D.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
RCDF				Causes a card to be read into memory in image mode and starts a second card on its way to the read station. Another card read instruction must be given within 5 ms. to avoid losing data from the second card.
RCD				Same as above except that a second card is not started toward the read station.
PCD				Causes a card to be punched from the 160 character area specified by address register D.
PCDCK				Causes a card to be punched starting with the address specified in address register D and causes the card previously punched to be checked against the area of memory specified by address register C.
CKCD				Causes the card last punched to be checked against the area of memory specified by address register C. A blank card is fed through the punch.

High-Speed Printer

The High-Speed Printer prints any of the characters shown in Appendix B. A line of 120 characters is printed at the rate of 900 lines per minute.

The printer instructions permit a line to be printed and paper to be advanced. Vertical line spacing is performed if the paper advance is specified by the program. The Central Processor proceeds with its program while spacing is done. A line counter, which counts up to 66, is set by either the PAGE, SPACE, or LINE instruction. When the line counter counts beyond 66, the paper is advanced to the next page to the line determined by the amount beyond 66 that it had counted.

The first character of the line of 120 characters to be printed is always specified by address register D.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
PRINT				Causes a line of 120 characters to be printed.
PAGE				Sets the line counter to the first line of the next page and advances the paper to this line.
SPACE			0-63	Adds the number specified to the current setting of the line counter, and advances the paper to this line.
LINE			0-63	Sets the line counter to the number of lines specified and advances the paper to this line. The paper is advanced to the next page if the number is less than the current line counter setting.

Magnetic Tape

The following Magnetic Tape instructions are used to transmit information between Philco 90,000 character per second or Philco 240,000 character per second Magnetic Tape units and the Philco 1000 Central Processor. Transmissions with the 90,000 character per second tape units are performed in groups of 1024 characters (blocks). These groups are bounded on each side by automatically recorded block marks. If an area of tape cannot be recorded, the block marks in this area may be erased.

The number of characters transmitted between these tape units and memory cannot be greater than 1024. If a value greater than 1024 is specified, only 1024 (one block) characters will be transmitted. If fewer than 1024 characters are specified in a Read operation, the number of characters specified will be read into

memory and the tape will be spaced to the end of that block. If fewer than 1024 characters are specified in a Write operation, the number of characters specified will be written and the remainder of the block will be filled with Filler characters (octal 32). Bit 4 of the Logic register will be set if the value specified in the address field of a Read or Write instruction is greater than 1024. The operation will proceed with one block being transmitted.

COMMAND			ADDRESS	REMARKS
Function	Registers	Options		
RMTF			0-4095	Reads the specified number characters, as indicated above, from magnetic tape into memory. The tape is read in a forward direction. If less than 1024, the tape is spaced to the end of a group of 1024 characters after reading the characters, which may not exceed 1024. Tape is not moved if the number specified is zero.
RMTB			0-4095	Same as RMTF except that the tape is moved in a reverse direction.
WMT			0-4095	Writes a specified number of characters onto magnetic tape. If less than 1024, the remainder of a group of 1024 characters is filled with filler characters (octal 32).
SMTF				Spaces the tape forward over one group of 1024 characters.
SMTB				Spaces the tape backward over one group of 1024 characters.
ERASE				Erases the tape one block (or record) in a backward direction.
RWD				Rewinds the tape reel.
RWDL				Rewinds the tape reel with lockout. The tape unit is unavailable until the operator intervenes.

Transmissions with 240,000 character per second tape units are performed on variable sized records. If an area of tape cannot be recorded on, record marks can be erased. Read and Write instructions for these tape units can specify up to 4095 characters per record.

With either type of tape unit, if the number of characters specified is zero, tape is not moved.

SECTION 5
OPERATOR CONTROLS

OPERATOR'S CONSOLE

Each Philco 1000 Central Processor provides a visual display of the current instruction, the address registers, the N and the Program Address registers, and any selected character. The Operator's Console is illustrated in Figure 4. Controls and indicators not discussed in this section are of interest to operators or maintenance personnel only.

Automatic Program Load

The operator initiates the input of programs by pressing the PROCESSOR CLEAR button and the AUTO LOAD button on the control panel. The first section of input data (one card or one group of 1024 characters on tape) is read into memory starting at the location specified by the ADDRESS TOGGLES. The Central Processor then executes the instructions starting at this location. This process sets all registers to zero, the direction indicators to forward, but does not affect any part of memory except the area into which data has been read.

Programs may be loaded from a Card Reader (AUTO LOAD 1) or Magnetic Tape unit (AUTO LOAD 2). AUTO LOAD control buttons for up to four input devices are available with each Central Processor unit.

TOGGLE ENTRY Switches

The operator may provide a one-bit input to the Toggle register by setting the TOGGLE ENTRY switches. This setting in the Toggle register may be examined by the program with a SAVE or Skip instruction.

Breakpoint Switch (JBT)

The Breakpoint (JBT) toggle on the console permits the operator to alter the program sequence wherever a JBT instruction occurs in a program. The program halts at this point if the switch is ON. If the switch is OFF, the instruction is executed as a JMP.

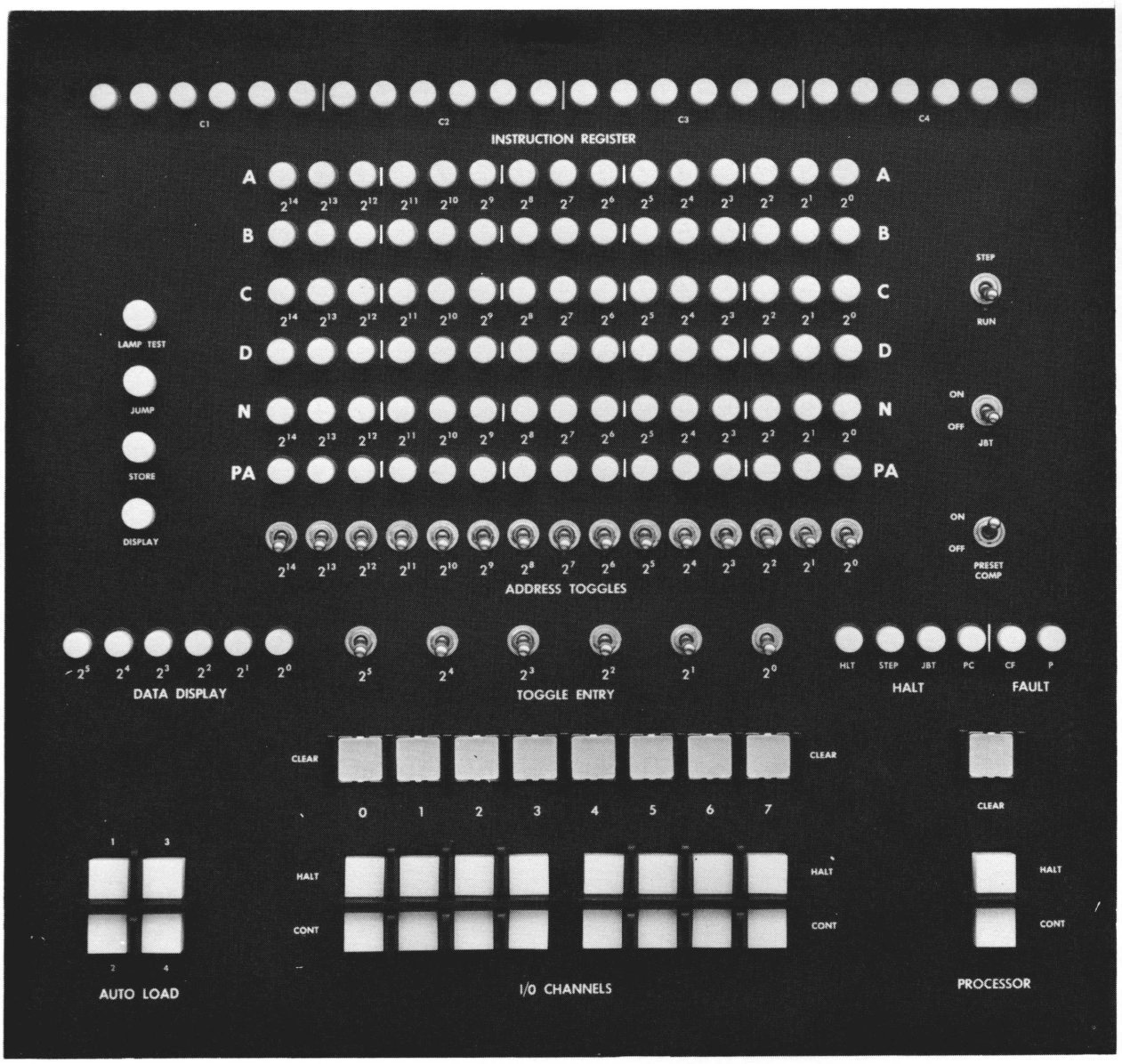

Figure 4. Philco 1000 Operator's Console

ADDRESS TOGGLES

The ADDRESS TOGGLES designate a location in memory which may be:

- Jumped to if the operator presses the JUMP button.
- Filled with the character designated by the six TOGGLE ENTRY switches if the operator presses the STORE button.
- Displayed as an instruction in the INSTRUCTION REGISTER if the operator presses the DISPLAY button.
- Used as a starting address for AUTO LOAD.

These functions will only be performed if the computer is not sequencing instructions.

PRESET COMP Switch

The PRESET COMP (Comparison) toggle switch, if set, will cause the computer to halt if the location set up in the ADDRESS TOGGLES is referenced as either a data or an instruction character. The computer will halt after execution of the instruction.

APPENDIX A

SIGNIFICANCE OF SPECIAL REGISTER BIT SETTINGS

LOGIC REGISTER

The Logic register may be set as a result of a number of instructions as indicated below:

BIT	SIGNIFICANCE	INSTRUCTIONS WHICH SET BITS
1	Greater	COMP
2	Equal	COMP
3	Lesser	COMP
4	End-of-Field, illegal Hollerith character, field-length error, or Non-numeric BCD character detected	MOVE, HTP, DTB, RMTF, RMTB, WMT
5	Result is field of zeros	MOVE, COPY, ADD, SUB, MPY, DIV, INC, DEC, AWC, OR, EX, EXZ, BTD, DTB
6	Overflow	ADD,SUB,DIV,INC,DEC,SHL,SHR

FAULT REGISTER

The Fault Register is initially cleared by each input-output instruction. When a SAVE F or Skip instruction (which tests the Fault register) is given, bits will be set in the Fault register as indicated below according to the device connected.

BIT	MEMORY	MAG TAPE	CARD READER	PRINTER
1		Parity error on tape	Second read station on card reader indicates both reads were not identical	
2		End-of-Block mark missing	RCDF instruction not followed by a RCDF or RCD within 5 ms.	Print wheel synchronization error
3		Beginning block mark missing	Skewed card has been read	
4		Less than 1024 characters in a 90,000 cps tape block	Row timing failure	
5		End of tape		
6	Parity error detected in operand access	Parity error on character received in memory	Parity error on character received in memory	

STATUS REGISTER

The status register is set if a CON (Connect) instruction (page 4-1) cannot be accepted. A connection cannot be made between a designated device or channel and the Central Processor. The significance of each bit set in the Status register is listed below:

BIT	SIGNIFICANCE
1	Processor already connected
2	Channel busy
3	Device mechanically unavailable
4	Not assigned
5	Not assigned
6	Not assigned

APPENDIX B

PHILCO 1000 CODE COMBINATIONS

Philco Character	Octal Code	Hollerith Punch ①	Philco Character	Octal Code	Hollerith Punch ①
0	00	0	-	40	11
1	01	1	J	41	11-1
2	02	2	K	42	11-2
3	03	3	L	43	11-3
4	04	4	M	44	11-4
5	05	5	N	45	11-5
6	06	6	O	46	11-6
7	07	7	P	47	11-7
8	10	8	Q	50	11-8
9	11	9	R	51	11-9
@	12	8-2 ②	¬	52	11-8-2 ②
=	13	8-3	$	53	11-8-3
;	14	8-4	*	54	11-8-4
≡	15	8-5	<	55	11-8-5 ②
&	16	8-6 ②	#	56	11-8-6 ②
'	17	8-7	␣	57	11-8-7 ②
+	20	12	Δ ④	60	Blank
A	21	12-1	/	61	0-1
B	22	12-2	S	62	0-2
C	23	12-3	T	63	0-3
D	24	12-4	U	64	0-4
E	25	12-5	V	65	0-5
F	26	12-6	W	66	0-6
G	27	12-7	X	67	0-7
H	30	12-8	Y	70	0-8
I	31	12-9	Z	71	0-9
n ③	32	12-8-2 ②	|	72	0-8-2 ②
.	33	12-8-3	,	73	0-8-3
)	34	12-8-4	(	74	0-8-4
%	35	12-8-5 ②	>	75	0-8-5 ②
?	36	12-8-6 ②	:	76	0-8-6 ②
"	37	12-8-7 ②	e ⑤	77	0-8-7 ②

① The Hollerith punch shown is that required on the punched card to represent the Philco character. The 12 rows of each column on a card are read into two consecutive characters in memory, with the 9-8-7-6-5-4 rows in the six bits of the first character, in that order, and the 3-2-1-0-11-12 rows in the second character. A one in any position represents a punch in that row. These Hollerith codes may be translated to or from Philco 6-bit code by the HTP and PTH instructions.

② Multiple punching on the key punch is required to produce this Hollerith code.

③ Filler Character.

④ Leaves blank column on Printer.

⑤ End-of-Field character.

APPENDIX C
TIMING PROGRAMS FOR THE PHILCO 1000

INSTRUCTION TIMING

All instructions described in this manual perform the operations designated in the memory cycle time of each character involved in the operation. The memory cycle time, per character, for a 4096 character memory Central Processor is less than 5 microseconds. The effective memory cycle time for a Central Processor with a memory over 4096 characters is less than 3 microseconds per character, since the access time for characters in separate memory banks is overlapped.

To add two values together, each with an operand of 24 bits (4 characters), the total number of accesses required is 4 for the instruction, 4 for each operand, and 4 for the result, a total of 80 microseconds for the entire operation. On a Central Processor with an 8192 character memory a total of 16 character accesses at 3 microseconds each would be required, a total of 48 microseconds for the entire operation.

INPUT-OUTPUT OPERATIONS

All input-output transmissions cause the Central Processor to wait at the input-output instruction until the transmission portion of the instruction is completed. Thus, input-output operations are a function of the speed of the device being used. The computer will go on to the next instruction as soon as the transmission is completed. Note that any attempt to check the status of the device being used will cause the computer to wait at the SAVE or Skip instruction until all functions designated by a prior input-output instruction are completed.

APPENDIX D

PHILCO 1000 MACHINE CODES

This appendix lists the four-character machine codes for the Philco 1000 instructions. The characters are designated as C1, C2, C3, and C4. The mnemonic codes and page references for each instruction are also listed.

An "x" in the C2, C3, or C4 columns indicates that that portion of the character is not significant and is not examined by the Central Processor. An "n" in these columns indicates that the programmer must designate an address or quantity which the assembly program converts to binary and places in these bits.

If the Central Processor attempts to decode any instruction whose machine code is not indicated below, the processor will halt and a command fault (CF) will be indicated on the Operator's Console (Figure 4).

The notes following the instruction lists present the bit configurations for C2 when C2 can vary.

MACHINE CODE				MNEMONIC CODE	PAGE
C1	C2	C3	C4		
00	0x	xx	xx	HLT	3-5
01	0x	nn	nn	CON	4-1
01	4x	xx	xx	DIS	4-1
02	0n	nn	nn	SAVE N	3-4
02	4x	nn	nn	LOAD N	3-3
03	xx	xx	xx	NOP	3-5
04	31	xx	xx	PAGE	4-4
04	60	xx	xx	RWDL	4-4
04	64	xx	xx	RWD	4-4
04	74	xx	xx	ERASE	4-4
04	76	xx	xx	SMTB	4-4
04	77	xx	xx	SMTF	4-4
05	32	xx	nn	LINE	4-4
05	33	xx	nn	SPACE	4-4
06	21	xx	xx	RCD	4-2
06	22	xx	xx	RCDF	4-2

MACHINE CODE				MNEMONIC CODE	PAGE
C1	C2	C3	C4		
06	25	xx	xx	CKCD	4-2
06	26	xx	xx	PCD	4-2
06	27	xx	xx	PCDCK	4-2
06	34	xx	xx	PRINT	4-4
07	71	nn	nn	WMT	4-4
07	72	nn	nn	RMTB	4-4
07	73	nn	nn	RMTF	4-4
10	(See note 1)	nn	nn	INC	3-9
11	(See note 1)	nn	nn	DEC	3-9
12	(See note 1)	nn	nn	SHL	3-7
13	(See note 1)	nn	nn	SHR	3-7
14	0n	nn	nn	SAVE A	3-4
14	1n	nn	nn	SAVE B	3-4
14	2n	nn	nn	SAVE C	3-4
14	3n	nn	nn	SAVE D	3-4
14	4n	nn	nn	SAVE T	3-4
14	5n	nn	nn	SAVE L	3-4
14	6n	nn	nn	SAVE F	3-4
14	7n	nn	nn	SAVE S	3-4
15	(See note 2)	nn	nn	SKE	3-10
15		nn	nn	SKNE	3-10
15		nn	nn	SKAN	3-10
15		nn	nn	SKAL	3-10
20	(See note 3)	nn	nn	COPY	3-5
21	(See note 4)	nn	nn	MOVE	3-6
22	(See note 4)	nn	nn	HTP	3-11
23	(See note 4)	nn	nn	PTH	3-11
24	(See note 3)	nn	nn	COMP	3-10

MACHINE CODE				MNEMONIC CODE	PAGE
C1	C2	C3	C4		
26	(See note 3)	xx	nn	BTD*	3-12
27	(See note 5)	xx	nn	DTB*	3-12
30	(See note 6)	nn	nn	AWC	3-7
31	(See note 6)	nn	nn	OR	3-7
32	(See note 6)	nn	nn	EX	3-7
33	(See note 6)	nn	nn	EXZ	3-7
34	(See note 6)	nn	nn	ADD	3-8
35	(See note 6)	nn	nn	SUB	3-8
36	(See note 6)	xx	nn	MPY*	3-8
37	(See note 6)	xx	nn	DIV*	3-8
40	0n	nn	nn	LOAD A F	3-3
41	0n	nn	nn	LOAD B F	3-3
42	0n	nn	nn	LOAD C F	3-3
43	0n	nn	nn	LOAD D F	3-3
44	0n	nn	nn	LOAD A B	3-3
45	0n	nn	nn	LOAD B B	3-3
46	0n	nn	nn	LOAD C B	3-3
47	0n	nn	nn	LOAD D B	3-3
50	0n	nn	nn	TAB A F	3-4
51	0n	nn	nn	TAB B F	3-4
52	0n	nn	nn	TAB C F	3-4
53	0n	nn	nn	TAB D F	3-4
54	0n	nn	nn	TAB A B	3-4
55	0n	nn	nn	TAB B B	3-4
56	0n	nn	nn	TAB C B	3-4
57	0n	nn	nn	TAB D B	3-4
60	nn	nn	nn	FILL A	3-6
61	nn	nn	nn	FILL B	3-6

** Optional*

MACHINE CODE				MNEMONIC CODE	PAGE
C1	C2	C3	C4		
62	nn	nn	nn	FILL C	3-6
63	nn	nn	nn	FILL D	3-6
64	nn	nn	nn	FILL A R	3-6
65	nn	nn	nn	FILL B R	3-6
66	nn	nn	nn	FILL C R	3-6
67	nn	nn	nn	FILL D R	3-6
70	0n	nn	nn	JMP A	3-5
71	0n	nn	nn	JMP B	3-5
72	0n	nn	nn	JMP C	3-5
73	0n	nn	nn	JMP D	3-5
74	0n	nn	nn	JMP	3-5
75	0n	nn	nn	JBT	3-5

Note 1:

BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6
1=N Option	00=A 01=B 10=C 11=D		Not used		1=R Option

Note 2:

BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6
000=A 001=B 010=C 011=D	100=Toggle 101=Logic 110=Fault 111=Status		00=Equal (SKE) 01=Unequal (SKNE) 10=Any Ones (SKAN) 11=All Ones (SKAL)		1=R Option

Note 3:

BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6
1=N Option	From: 00=A 01=B 10=C 11=D		To: 00=A 01=B 10=C 11=D		1=R Option

Note 4:

BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6
Not used	From: 00=A 01=B 10=C 11=D		To: 00=A 01=B 10=C 11=D		Not used

Note 5:

BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6
1=N Option	From: 00=A 01=B 10=C 11=Illegal		To: 00=A 01=B 10=C 11=Illegal		1=R Option

Note 6:

BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6
1=N Option	Not used		Not used		1=R Option

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