POTTER

PRODUCT DATA

1-409

MA 751 READ/WRITE SWITCHING AMPLIFIER

POTTER INSTRUMENT CO., INC.®

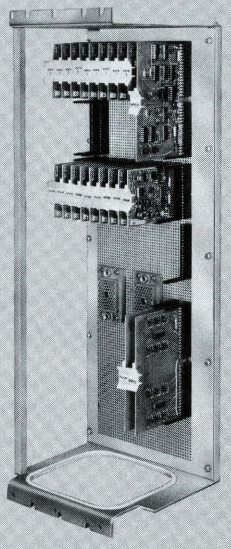
FEATURES

- Write and/or Read 1600 cpi Phase Encoded magnetic tapes which are compatible and interchangeable with tapes recorded on IBM 2400 Series Tape Units.
- Amplifier sharing of up to eight tape units.
- Information transfer rates up to 320 kilocharacters per second.
- Write data electronics includes required circuitry to record customer generated Identification Burst, Preamble, Postamble and Tape Mark. Input data is clocked serial-by-bit, parallel-by-character, binary. Data is converted to phase encoded format prior to recording on magnetic tape.
- Read Data Electronics includes required circuitry to strip the Preamble, Postamble, and to detect the Tape Mark. Read electronics also provide read deskew and single track error correction. Read output consists of 9-bytes of data, binary format with read clock signal.
- Automatic head degauss cycle reduces erasure and pulse distortion.
- Shaped write current optimizes data recording symmetry.
- Designed to minimize maintenance costs. Accessible test points at front of chassis permit most adjustments to be made with modules in normal position. Extension frames included provide complete exposure of all plug-in modules for circuit testing under actual operating condition.

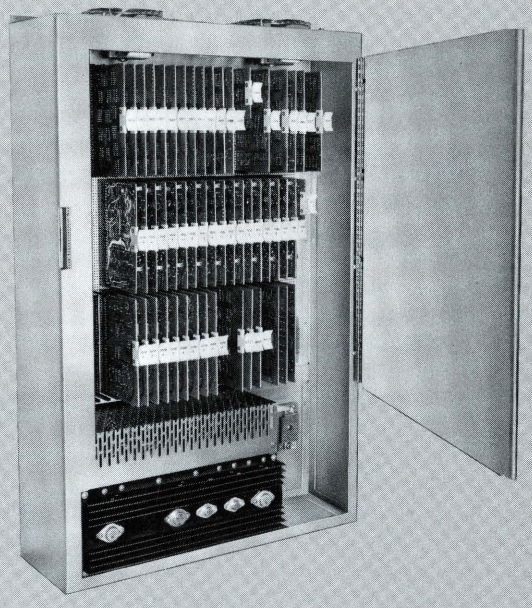
INTRODUCTION

Potter Model MA751 Read/Write Switching Amplifier records and reproduces magnetic tapes in industry standard 1600 cpi phase encoded format. Unlike NRZI format which records a flux reversal in either direction on a "1" bit, the Phase Encoding method of recording records information by producing a distinct flux reversal on tape, for the "0" and "1' information bits (See Figure 1). A "1" is recorded as a reversal to the polarity of the interrecord gap; a "0" as a reversal opposite to the polarity of the interrecord gap. Therefore, when recording a typical 10101 pattern we have reversals at bit times only.

In Phase Encoded recording like bits require reversals in the same direction, and thereby necessitate the insertion of an additional "phase transition" between reversals to achieve proper polarity of data. The phase bit reversal, although not used as data, increases the recording density to 3200 flux reversals per inch.



MA 751 Local Read/Write Switching Amplifier



MA 751 Common Electronics

EFFECTIVE: July 15, 1970

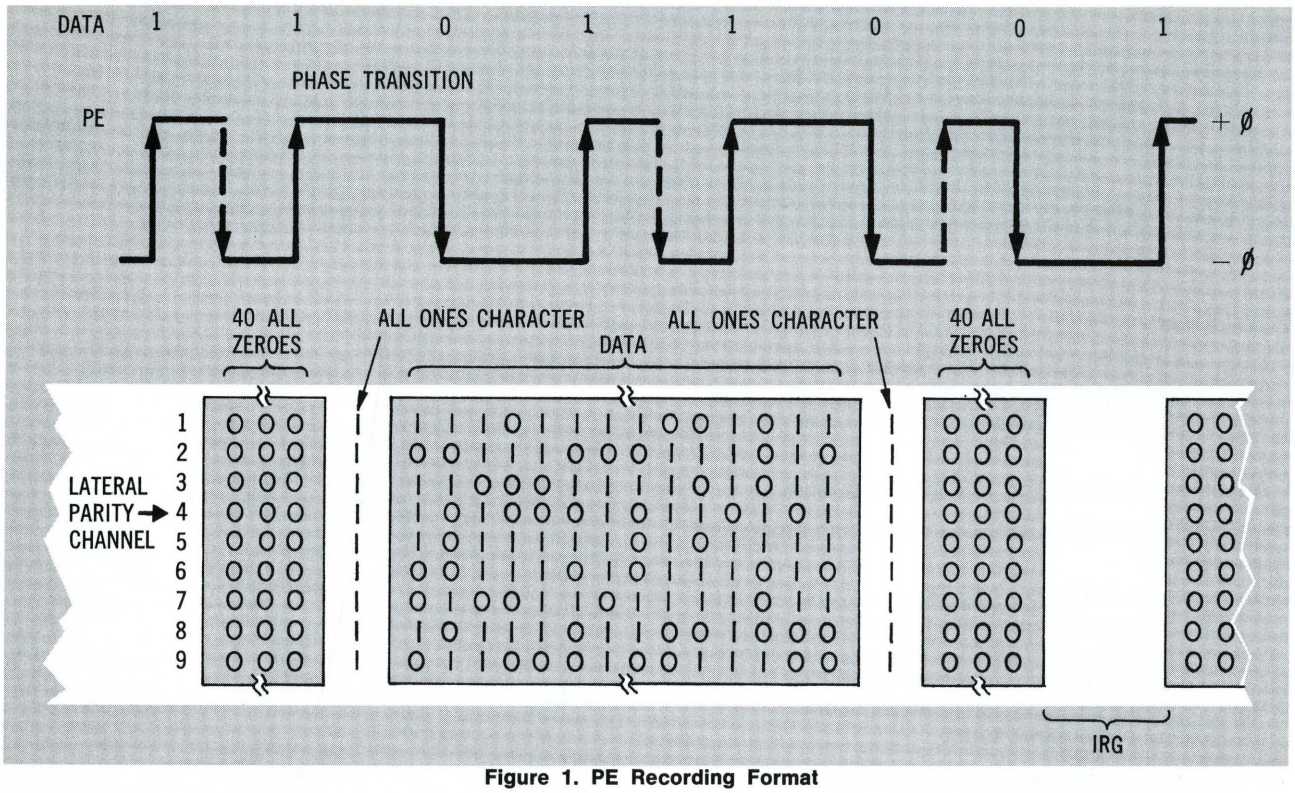


Figure 1. PE Recording Format

When recording in the Phase Encoded mode, each block of information is preceded by, and followed by, a burst of synchronizing information — the preamble — and the postamble. The preamble consists of 40 characters containing "0" bits in all tracks including parity followed by a single character of "1" data in all tracks. The postamble contains a single character of "1" data in all tracks, followed by 40 characters containing "0" bit data in all tracks.

Although the Phase Encoded format increases the recording density of the system, the discrete transition and clock techniques eliminate many of the problems normally encountered with 800 bpi NRZI recording systems. Phase Encoded recording properly compensates for the errors associated with static and dynamic skew, "drop outs", "drop ins" (noise) and speed variation and thereby improves the inherent system reliability.

The Phase Encoded system and Potter MA 751 Amplifier provide the following features:

. . . Static and Dynamic Skew: The deskewing (egg-crate) buffer, in conjunction with the preamble, automatically deskews the recorded information. No static or dynamic deskewing one-shots nor deskewing delay lines are required in Phase Encoded format even though the recorded tape can contain as much as one full bit time of skew and the guidance system of the tape handler reading this tape can add an additional cell of skew time.

. . . Drop outs: The read sensitivity of the Phase Encoded system is fixed at 15% of standard recording level. If the signal from any single track drops below the 15% level, the information for this track is reconstructed from the information supplied by the remaining 8 tracks. Under most conditions,

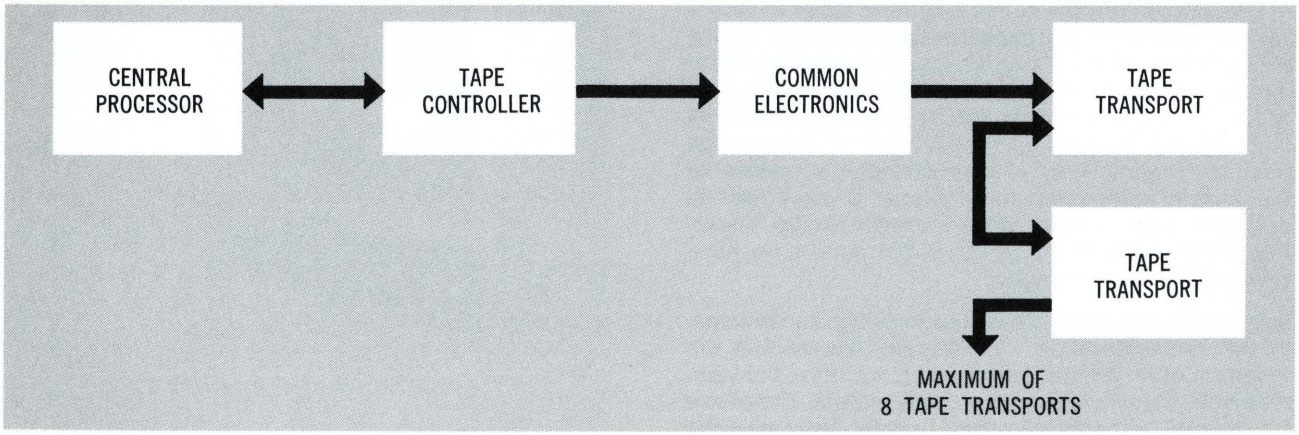


Figure 2. Magnetic Tape System

this 'force feeding' method of data correction reduces the error rate caused by bit drop outs by a factor of 10.

. . . Drop ins: In Phase Encoded recording if an information block is not preceded and terminated with a preamble and postamble, the recorded data is not accepted as valid information. In addition to synchronizing data and clock, the preamble and postamble reduce the incidence of reading, as data, spurious signals which appear within the inter-record gap.

. . . The discrete transitions associated with the "0" data bit in Phase Encoded recording eliminates many of the drop in errors attributed to noise distortion in NRZI format.

. . . Speed variations: The speed at which Phase Encoded tapes can be recorded can vary within ±4% of nominal. The short term speed variation can add up to ±10% at a rate of change of 0.5% per character. To assure reliable read data output, Potter's MA 751 Amplifier will accommodate the change in transfer rate due to speed variation and compensate any additional changes due to the reproducing system. The amplifier compensates the speed of each track independently by utilizing a variable frequency flywheel oscillator with multi-zone synchronization circuits.

FUNCTIONAL OPERATION

The Common Electronics provides interface control for transmitting data between the central processor and the tape transports in the system, as shown in figure 2. The amplifier provides up to 1x8 Switching and all input/output lines to tape transport are daisy-chained with appropriate termination in the chain's last unit. During reading, the CE detects zero crossings of the 9-channel data signal from the Read/Write Amplifier located in the Tape Units. After detection, the signals are decoded, deskewed, checked for format and parity and then transmitted to the central processor at digital levels. When writing data, the data is encoded by the CE. The data and required control signals are transmitted from the central processor to the CE. The CE provides the proper control functions and the encoded write signals to the local amplifier for subsequent recording on tape. The CE also provides decoding circuits for converting binary coded 4-line Transport Unit selection signals into discrete selection signals for each of the eight Transport Units.

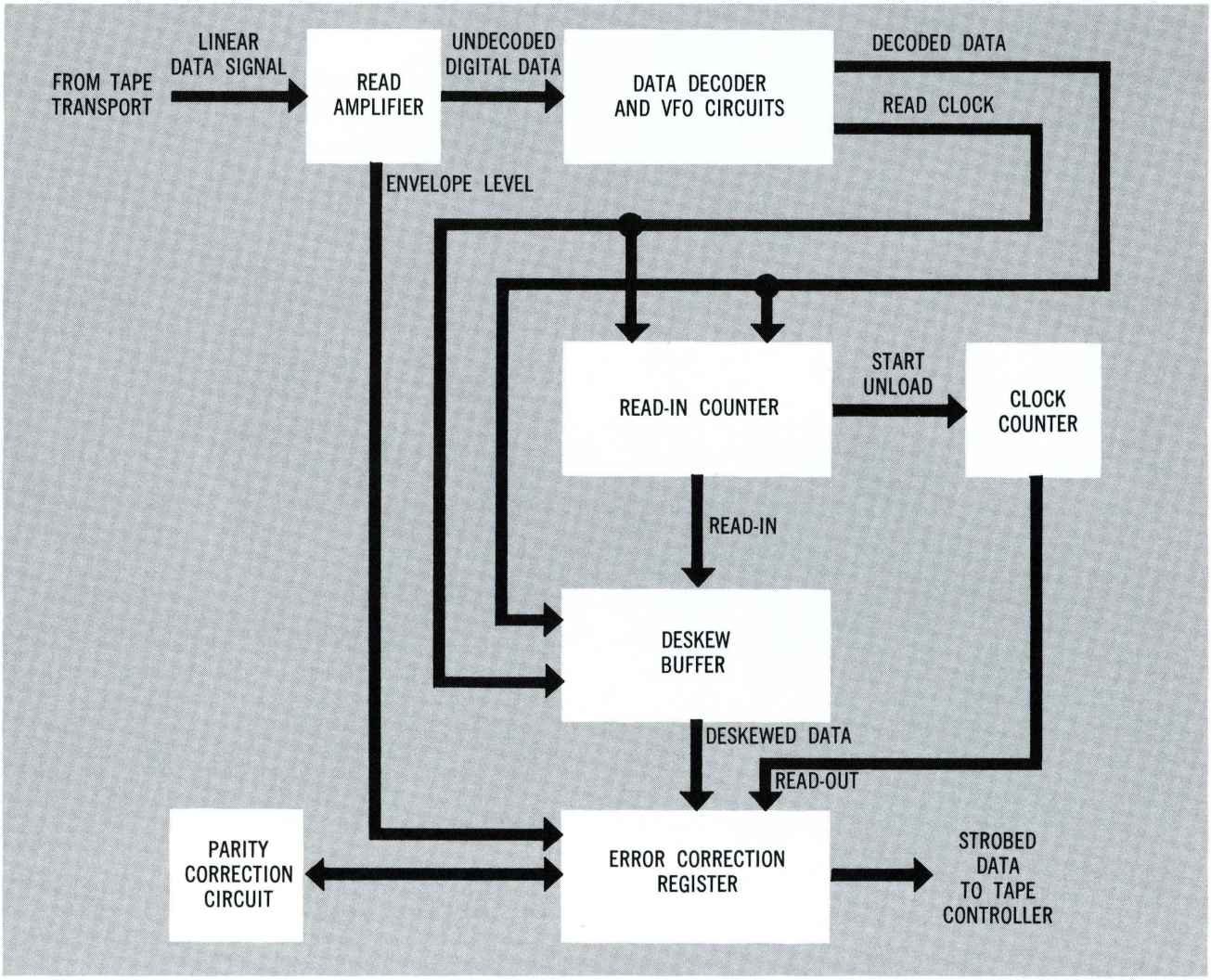


Figure 3. Read Circuits, Block Diagram

READ OPERATION

The data record transmitted to the CE is preceded by a preamble consisting of 40 all zeros and an all ones character for purposes of synchronizing and data decoding. The preamble is then followed by the data record which is then followed by a postamble. The postamble facilitates data synchronization when operating in the read reverse mode.

The purpose of the preamble is to allow the decoding circuits to synchronize with the incoming data. This is accomplished by a phase test which checks whether zeros are misinterpreted as ones. If they are, the circuits shift the clock 180 degrees so that zeros are correctly interpreted as zeros. No data is transferred to the Tape Control Unit until the all ones character is decoded. The purpose of the all ones character and the 40 all zeros in the postamble is to detect the end of the data block during writing or during reading.

During a read operation, the signal from the Tape Transport is applied to the read amplifier portion of the read circuits where amplitude checks and zero crossover detection is accomplished (Figure 3). The read amplifier provides undecoded digital data which is then applied to the data decoder and variable frequency oscillator (VFO) circuits. The speed variation component of the data is eliminated as an aid to reliable detection.

The data decoder circuits decode the signal from the read amplifiers, and decoded data together with a self-generated read clock are applied to the read-in counter and the deskew buffer circuits. The read-in counter determines into which stage of the deskew buffer a data bit is stored. In addition, the read-in counters provide a start unload signal to the clock counter for reading out data. Deskewed data is then read out to the Error Correction Registers. Data is then strobed and read out to the Tape Control Unit. In the event that a single track output signal drops below the 15% threshold during a read mode, data will be reconstructed for the dropped track.

The Read Amplifier digitizes the incoming data signal from the tape transport by detecting zero crossings of the data signal. In addition, the read amplifier detects the envelope of the incoming data signal and allows transmission of the digitized data when the envelope is present.

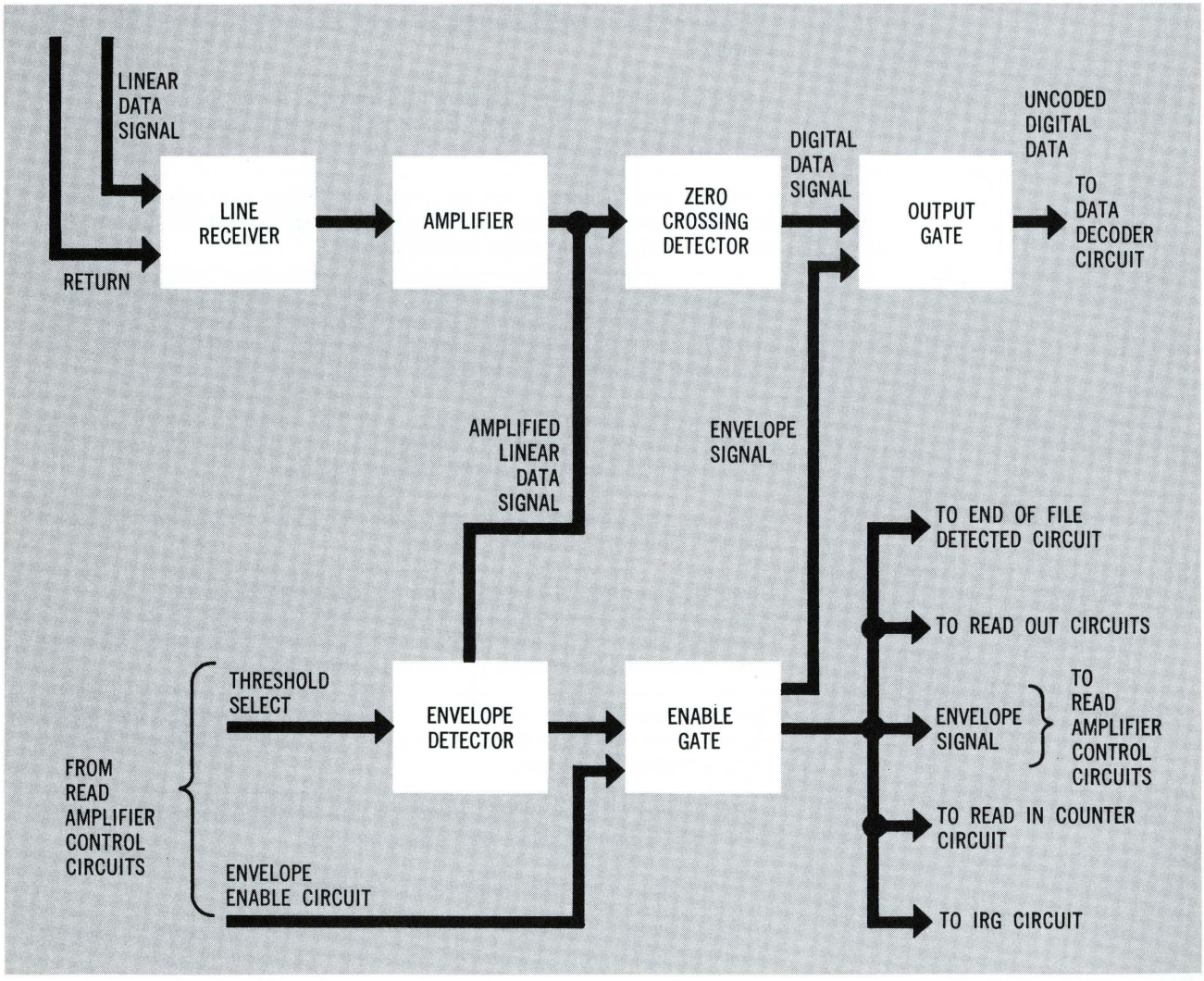


Figure 4. Read Amplifier, Block Diagram

CONTROL ELECTRONICS MODULES

MODULE	FUNCTION
Common Electronics Receiver	Contains circuits which invert the Transport Unit output signal levels to Common Electronics operating levels and act as line terminators.
Clock Counter	Contains the Read Out Counter circuit which generates the signals to transmit the data to TCU.
Deskew Buffer and Control	Contains the Read In Counter which indicates the stage of the deskewing buffer into which the decoded data are to be stored. The deskewing buffer allows data alignment on each channel so that each bit of a character is presented simultaneously to the tape control unit.
Decoder Control	Contains the circuits which enable the internal Read Forward and Read Reverse decoder signals. Also generates the Phase Test Pulse, Master Reset to the decoder circuits, and the signal which inhibits data from the start of block until phase test is checked.
End File and Parity Control	Contains the circuits which enable the envelope detector and the End-of-Block signal that occurs when a valid postamble is detected. The module generates the End of File signal, the Error Correct mode signal, and detects Interrecord Gaps.
Gates	Contains gating circuits which detect the all zeros character in the deskew buffer (ZERO) and the all ones character in the error check Register.
Logical Block Detect	Contains the circuits which generate the data block detection signals, Active Envelope Level, Valid Block and the Detection of Data Block. It also generates the Zone Signals and the Error Level Signal.
One Shot	Contains the circuits which generate the pulses that inhibit the read operation during BOT and accelerate. Also generates the End-of-File detector and Leading Edge of IRG signals.
PE Decoder	Contains the circuits which together with the circuits on the Phase Encoded Servo Loop module, process the digitized data from the read amplifier by converting the PE coded data into digital data. Also generates the internal data clock for the deskewing buffer.
Phase Encoding Servo Loop	Contains the comparator circuits and the ramp generator circuits necessary to convert the PE coded data into digital data. Generates the Variable Frequency Compensation signals.
Postamble Detect and Control	Contains the circuits which generate the End of Information Level and the Data Transmission Signal.
Parity Check	Contains the circuits to determine the parity of the data.
Read Amplifier	Contains the circuits that digitize the incoming data signal from the tape transport and checks the data signal envelopes.
Receiver	Contains the circuits which act as line terminators for the digital signals from the Tape Control Unit and converts control unit signals to acceptable CE signals.
Reset Control	Contains the circuits which generate the Threshold Select, reset of write coders, and reset of deskewing buffers.
Transmitter	Converts data to correct logic levels for use by CP.
Unit Select	Contains the circuits which convert the four bit binary coded transport selection signal into any one of eight discrete select signals.
Write Coder	Contains the circuits which convert the binary input write data from the tape control unit into PE coded data.

LOCAL READ/WRITE AMPLIFIER CHASSIS

The Local Read/Write Amplifier chassis is equipped with Write Amplifier plug-in modules which convert and record digital information on magnetic tape. The chassis also includes read preamplifier modules which reproduce recorded data and, on command, transfers this data over the read buss. A Write Control module controls the recording current levels, and degausses the write heads whenever the 'set write' condition is disabled.

MODULE	FUNCTION
Read Preamplifier	The nine read preamplifiers detect the output of the nine read channels, amplify these outputs and feed the amplfiied signals, in parallel, to Read Amplifier modules located in the CE.
Write Control	The write control circuits provide the signals which control the operation of the write amplifier circuits. These circuits also generate signals which control the operation of the erase head. In addition, this module contains the automatic degauss circuit.
Write Amplifier	The function of the nine write amplifier circuits is to receive phase encoded write data from the CE, amplify it, and apply this data to the nine write channels. These circuits also provide the degauss function to the write head.

SPECIFICATIONS

Read/Write Format	Phase Encoded (PE)		
Recording Density	1600 cpi, 3200 FRPI		
Tape Speed (single)	20 ips to 200 ips		
Data Frequency	Up to 320 Kilocharacters/second		
Read Direction	Forward/Reverse		
Compatible Head Types	20-45 ips	50-150 ips	200 ips
Simultaneous Read/Write	HD 903	HD 901	HD 902
Read Only	HS 901	HS 903	HS 902
Input Power	115 VAC ±10% 60 Hz Single Phase or 208/230 VAC ±10% 50/60 Hz, Single Phase		
Input/Output Levels			
Input	Logic "1" = OV ±0.7 V 3 MA Logic "0" = +5 VDC ±1.0 V 5 MA		
Output	Logic "1" = Ground ±0.7 V 20 MA Sink Logic "0" = +5 VDC ±1.0 V 3 MA Source		
Ambient Amplifier Operating Temperatures	45°F to 110°F with 20% to 95% Relative Humidity		
	Common Electronics	Local Electronics	
Height	33.5 inches	23.5 inches	
Width	22.0 inches	8.5 inches	
Depth	7.5 inches	6.5 inches	
Weight	85 lbs.	15 lbs.	

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