PRIME Technical Update

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Applicable Software: N/A

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Abstract: Reviews configuration rules for 1Ø- and 17-slot backplanes, the priority network, 32K memory boards, extended control store, and writable control store.

This bulletin is one in a series of documentation supplements that supply current information on Prime hardware, software and documentation products. Prime Technical Updates introduce product improvements and revisions, and update existing Prime Computer user documentation.

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BACKPLANE CONFIGURATION RULES

This memo defines the configuration rules for the standard 10 slot and 17 slot backplanes as well as the special rules associated with the interim (two piece) 17 slot backplane.

1. The following rules apply for the 10 slot and new, one-piece 17 slot backplanes.

    1.1 The first increment of memory plugs into the top slot.

    1.2 All memory modules must be in adjacent slots.

    1.3 The preferable location for the CPU is between the memory and option boards.

    1.4 Priority for the option boards is established by relative position with the bottom slot having highest priority.

    1.5 No more than three slots can be skipped between options using the interrupt priority network.

    1.6 No more than seven slots can be skipped between options using the DMA priority network.

    1.7 There may be additional configuration requirements dictated by power distribution and supply limitations.

2. The following rules apply for the two-piece 17 slot backplanes.

    2.1 The first increment of memory plugs into the top slot of bottom 10 slot portion. All memory modules must be in adjacent slots and may only be plugged into the bottom 10 slot portion of the backplane.

    2.2 If a system has three or more memory boards then the slot just below the memory must be occupied by an option which uses the interrupt priority net to insure that priority is passed on to the upper seven slot position of the backplane.

2.3 If a system has seven or more memory boards then the slot just below the memory must be occupied by an option which uses the DMA priority net to insure that it gets passed on to the upper seven slot portion of the backplane.

2.4 Priority for the option boards is established by relative position with the bottom slot having highest priority.

2.5 The CPU must plug into the bottom ten slot portion.

2.6 No more than three slots can be skipped between options using the interrupt priority network.

2.7 No more than seven slots can be skipped between options using the DMA priority network.

2.8 There could be additional configuration requirements dictated by power distribution and supply limitations.

2.9 The slot select addresses are identical for the top seven slots of the ten slot section and the top seven slot section.

PRIORITY NETWORK CONFIGURATION

In recent weeks some systems have been put together that have had priority network problems. In order to clear up some of the confusion about how the option boards pass on the pri-net, I have included a list of options showing how each passes on the pri-net. I also have included some sample configurations to show how to avoid trouble. I have included some blank Backplane Configuration sheets, and I recommend that a sheet be filled out for each system in order to be sure the pri-net is OK. The difficulty with pri-net configurations arises because there are several techniques for passing on the network. I recommend that all future options pass on the pri-net via gates rather than jumpers.

Jumpering of Pri-Net by Option - Table 1

OPTION	INT NET	DMX NET
CPU (WW)	Jumper (CA-17 to CA-19)	Jumper (CA-7 to CA-9)
CPU (etch)	Jumper (CA-17 to CA-18)	Jumper (CA-7 to CA-8)
Option A (etch)	Gate	Jumper (CA-7 to CA-8)
Option B	Gate	Gate
Control Panel	- No Affect on Pri-Nets -	
GPIB	Gate	Gate
PRIMAD	Gate	Gate
Memory	Jumper (CA-17 to CA-18)	Jumper (CA-7 to CA-8)
MPC	Gate	Gate
Mag Tape	Gate	Gate
MSLC	Gate	Gate
AMLC	Gate	Gate
IPC	Gate	Gate
Dig Out	Gate	Gate
Dig In	Gate	Gate
XCS/FLT	Gate	Gate
BPIOC	Gate	Gate
D/A	Gate	Gate
MACI	Gate	Gate
DS	Gate	Gate
Diskette	Gate	Gate
CR/CP/LP (MPC)	Gate	Gate

The example below does not include power supply load considerations.

EXAMPLE 1

CPU, 32K mem, Option A, Option B AMLC. (See configuration sheet for example 1.)

The equipment requires:

CPU	- 2 slot (wirewrap)
32K	- 4 slots
Option A	- 1 slot
Option B	- 2 slots
AMLC	- 2 slots
	11 slots

Must use 17-slot backplane - starting at the top put in memory.

Step 1 - Draw in memories starting at top.

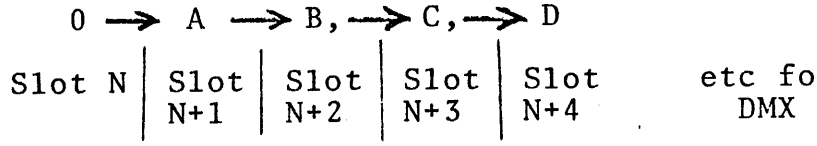
Step 2 - Decide what priority options are suppose to have. For purposes of discussion assume that the priority on the interrupt net is to be as follows: Option B, Option A, AMLC in order of higher to lower. Therefore, Option B goes in a lower slot # than either Option A or AMLC. Assume the following placement:

Slot 2 - Option B
Slot 4 - Option A
Slot 6 - AMLC
Slot 8 - CPU

Step 3 - List options in left hand column and draw in the way the options pass on the pri-net. Consult Table 1 to find out how the option passes on the net. From Table 1 - Option A (etch) - Jumpers CA-7 to CA-8. All other options use a gate.

Step 4 - Sketch in the pri-net interconnection on the backplane. The pri-net of each slot is connected on the backplane as follows:

0 is the driven point



Step 5 - By observation of sketch determine if network is OK (unbroken). The network in the example is OK.

Example 1A shows a configuration in which net is broken.

This simple example demonstrates the technique to be used. It is very important to follow the procedure for large systems, particularly if options are to be left out of the backplane because of a ship-short situation. I have included two other examples of large systems that were shipped. Example 2 shows a broken pri-net which causes a problem while trying to run DOS-VM. Example 3 shows a system which had to ship-short two boards. The sketch allows the configuration to be checked.

Some General Comments

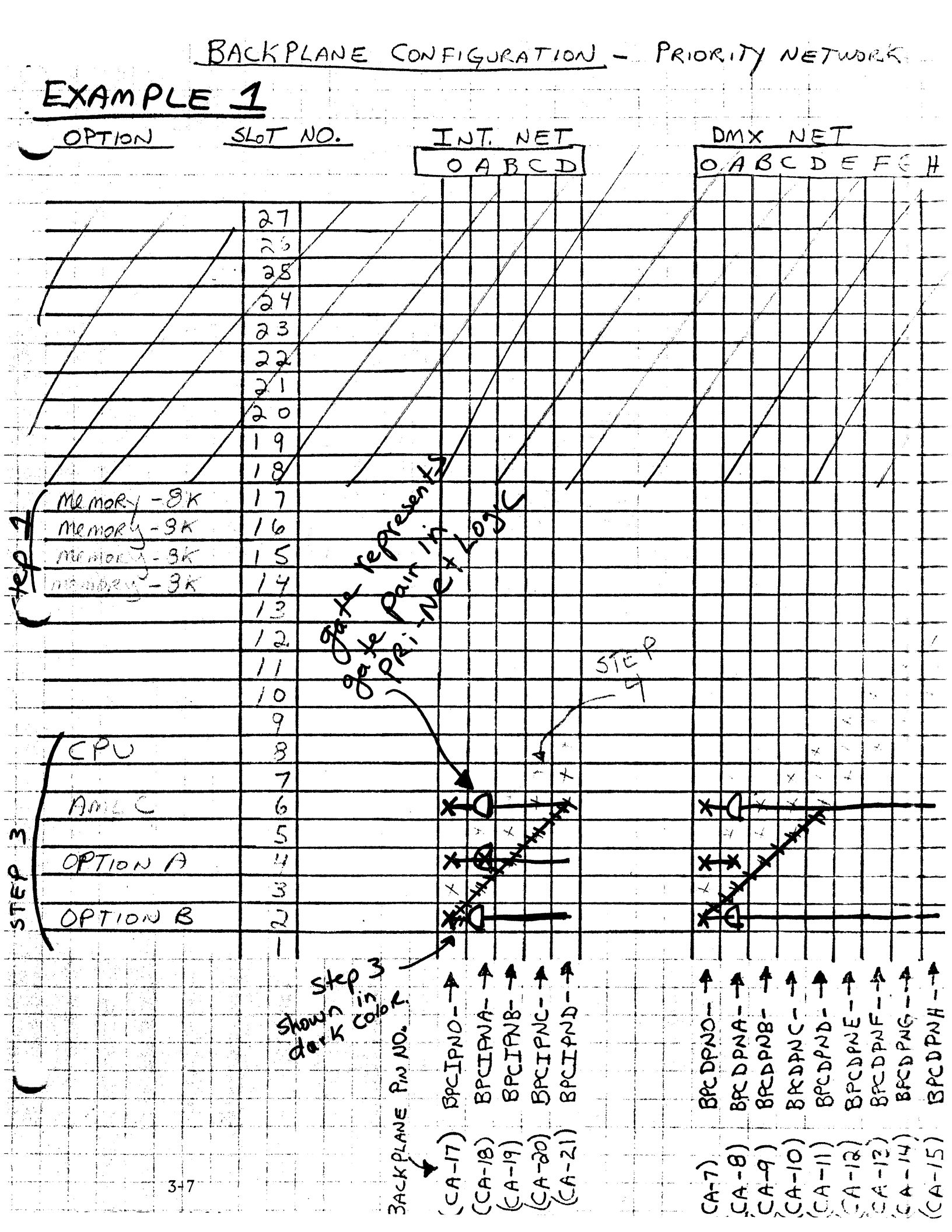
The rule of thumb that says no more than three slots between boards for the interrupt net and not more than seven slots between boards for the DMX net holds true if the nets are passed on by gates; however, options which jumper the net can cause trouble.

The maximum number of gate pairs for the INT net is four. The maximum number of gate pairs for DMX net is two. This constraint affects the number of blank slots that can be between options - see Example 4.

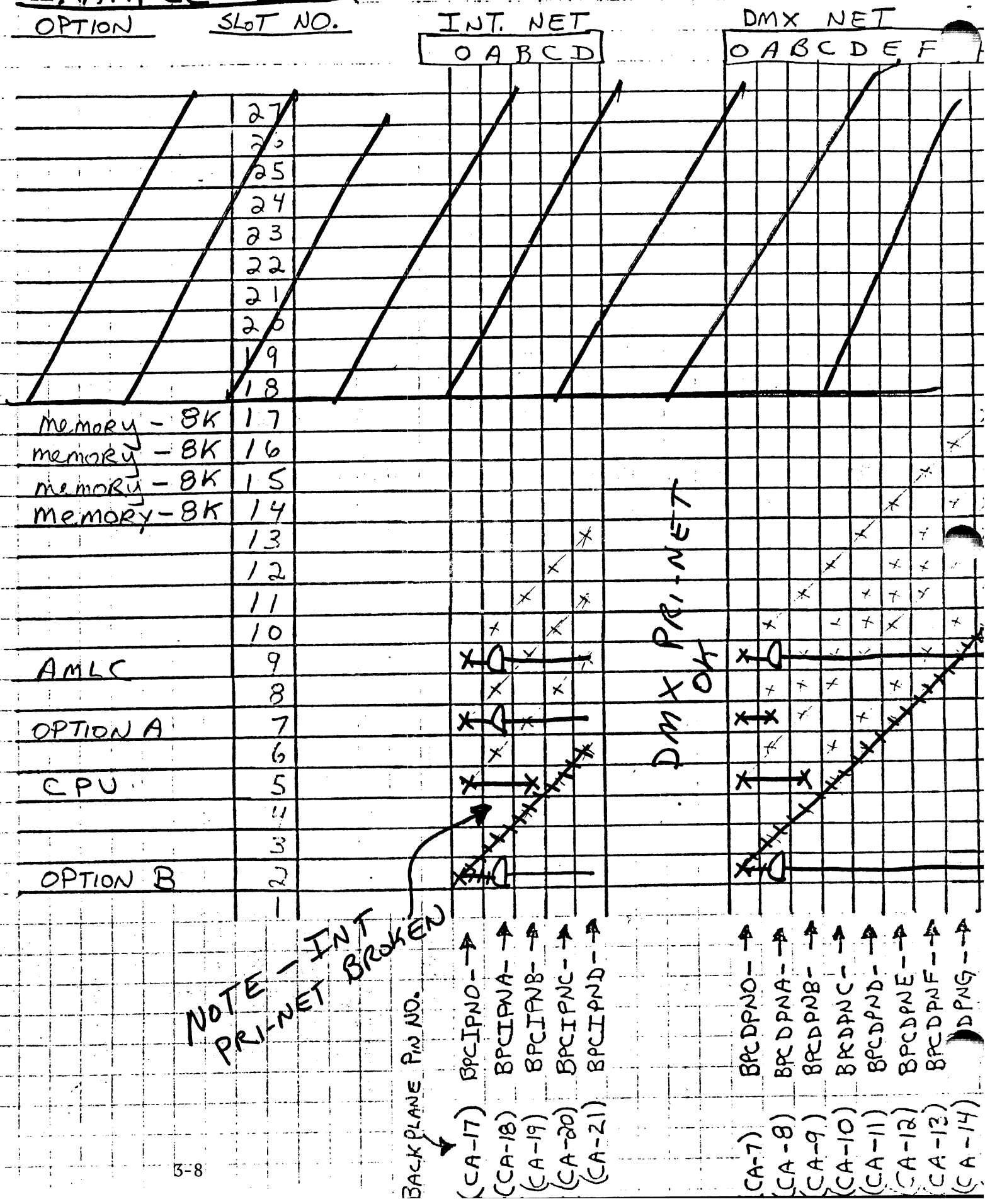
Avoid configuring memories such that options appear on either side as shown in Example 2. This means that some gates drive a large number of pins and thus a large amount of capacitance slowing down the pri-net.

BACKPLANE CONFIGURATION - PRIORITY NETWORK

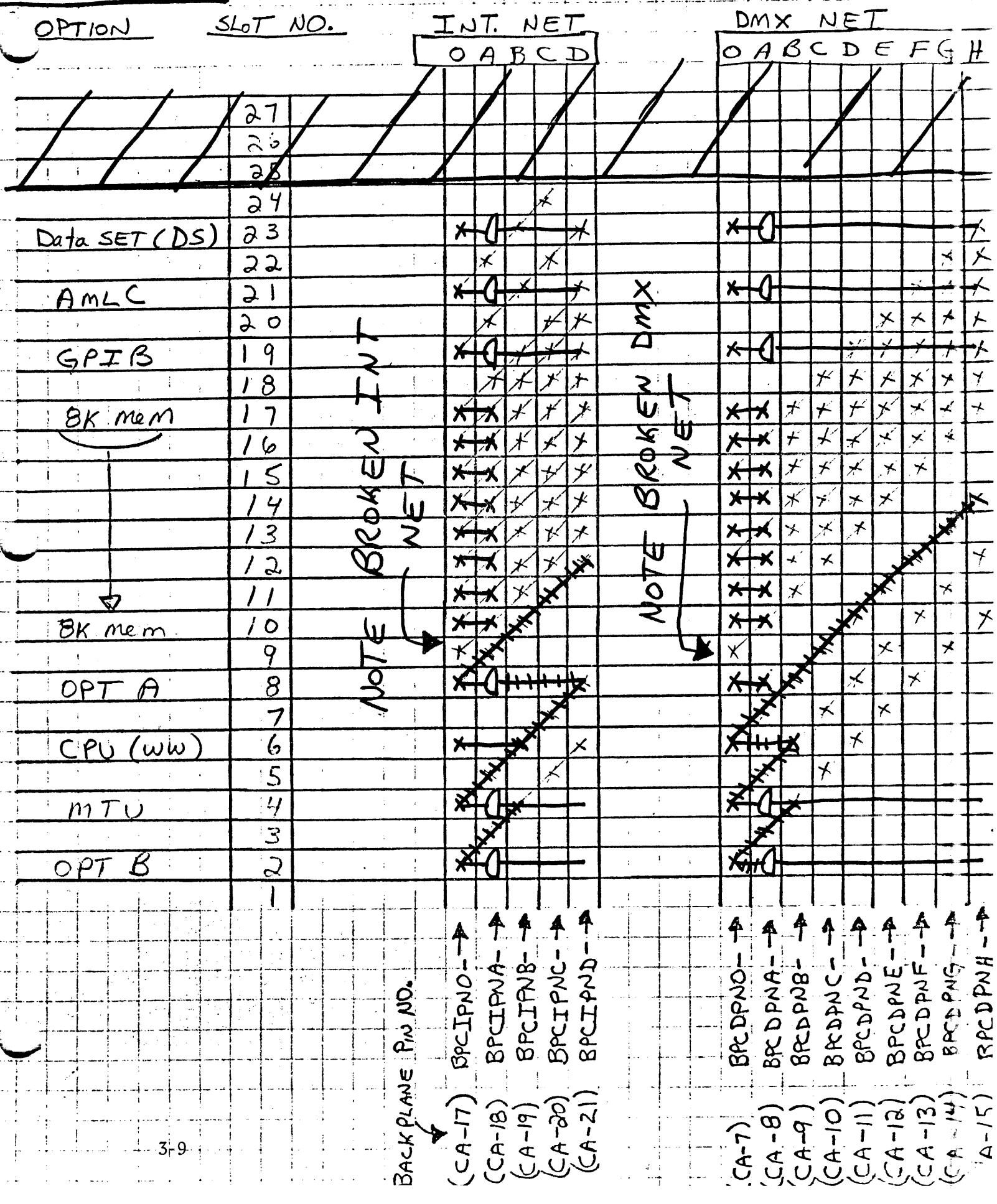
EXAMPLE 1



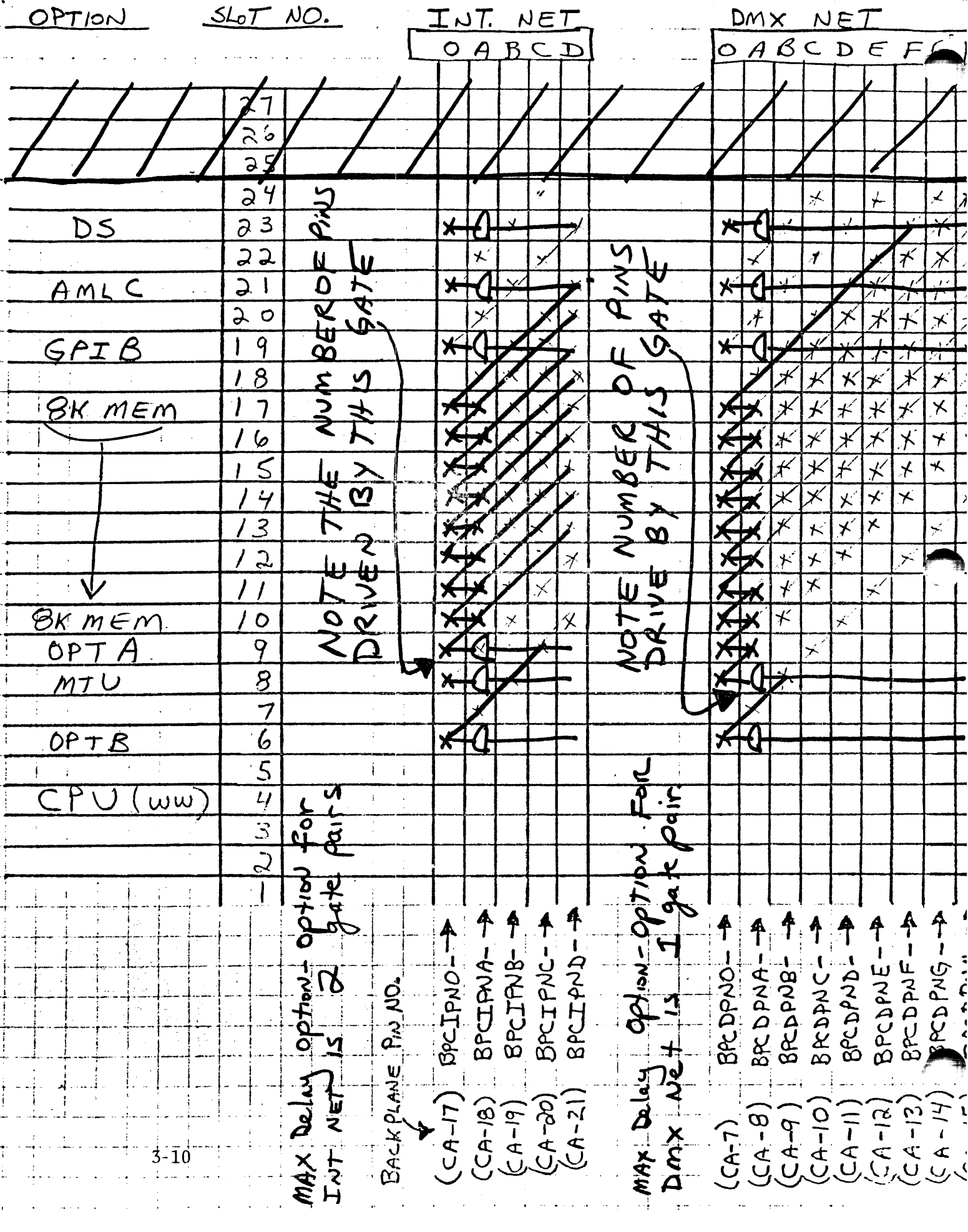
EXAMPLE 1A


OPTION
SLOT NO.
INT. NET
O A B C D
DMX NET
O A B C D E F
27
26
25
24
23
22
21
20
19
18
Memory - 8K 17
memory - 8K 16
memory - 8K 15
Memory - 8K 14
13
12
11
10
AMLC 9
8
OPTION A 7
6
CPU 5
4
3
OPTION B 2
1
DMX OR PRI-NET
NOTE - INT PRI-NET BROKEN
BACKPLANE PIN NO.
(CA-17) BPCIPNO-
(CA-18) BPCIPNA-
(CA-19) BPCIPNB-
(CA-20) BPCIPNC-
(CA-21) BPCIPND-
(CA-7) BPCDPNO-
(CA-8) BPCDPNA-
(CA-9) BPCDPNB-
(CA-10) BPCDPNC-
(CA-11) BPCDPND-
(CA-12) BPCDPNE-
(CA-13) BPCDPNF-
(CA-14) DPNG-

EXAMPLE 2 - BROKEN PRI-NET



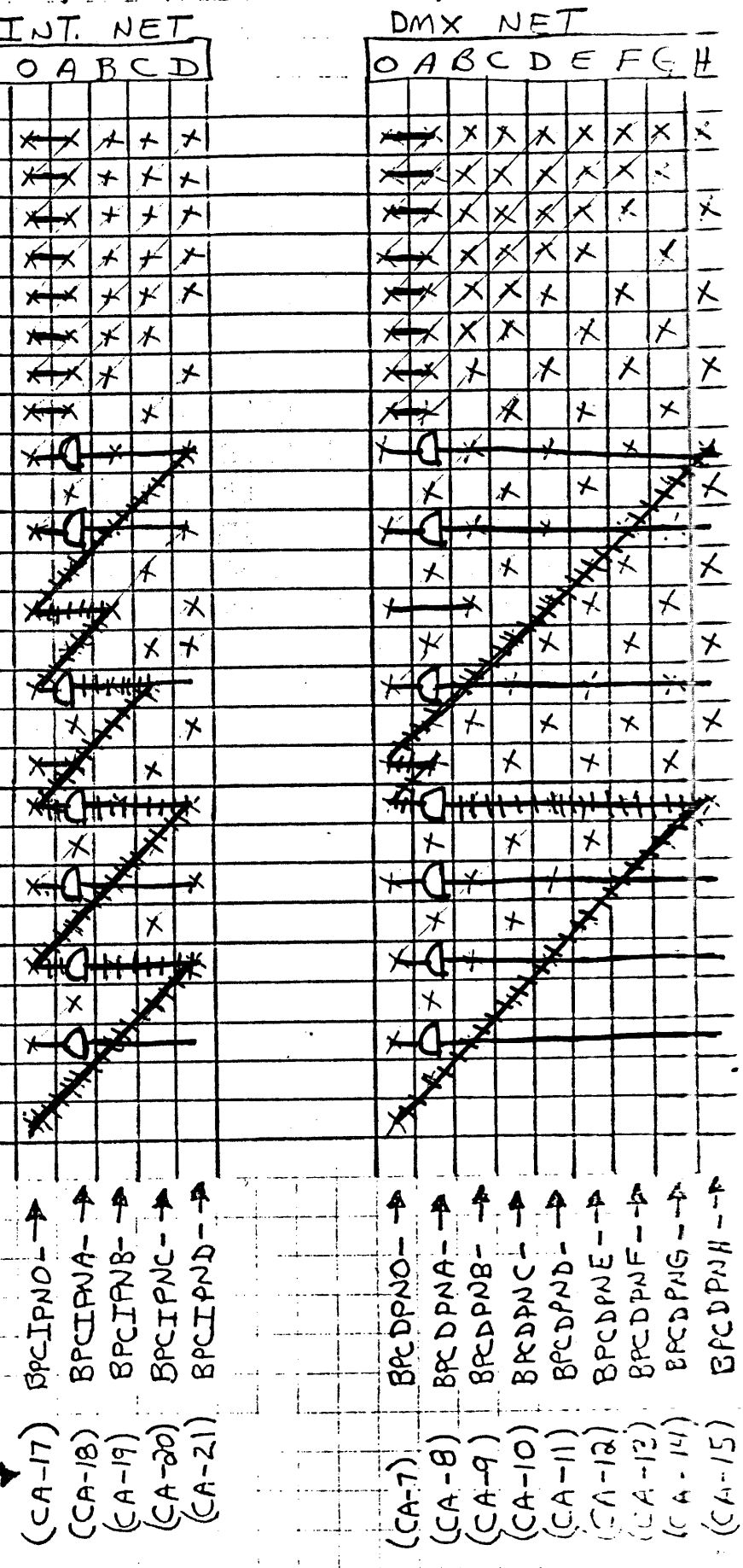
EXAMPLE - 2A — CORRECTED NET



[redacted] BACKPLANE CONFIGURATION - PRIORITY NETWORK

UNIVERSITY OF MICH. - EXAMPLE 3

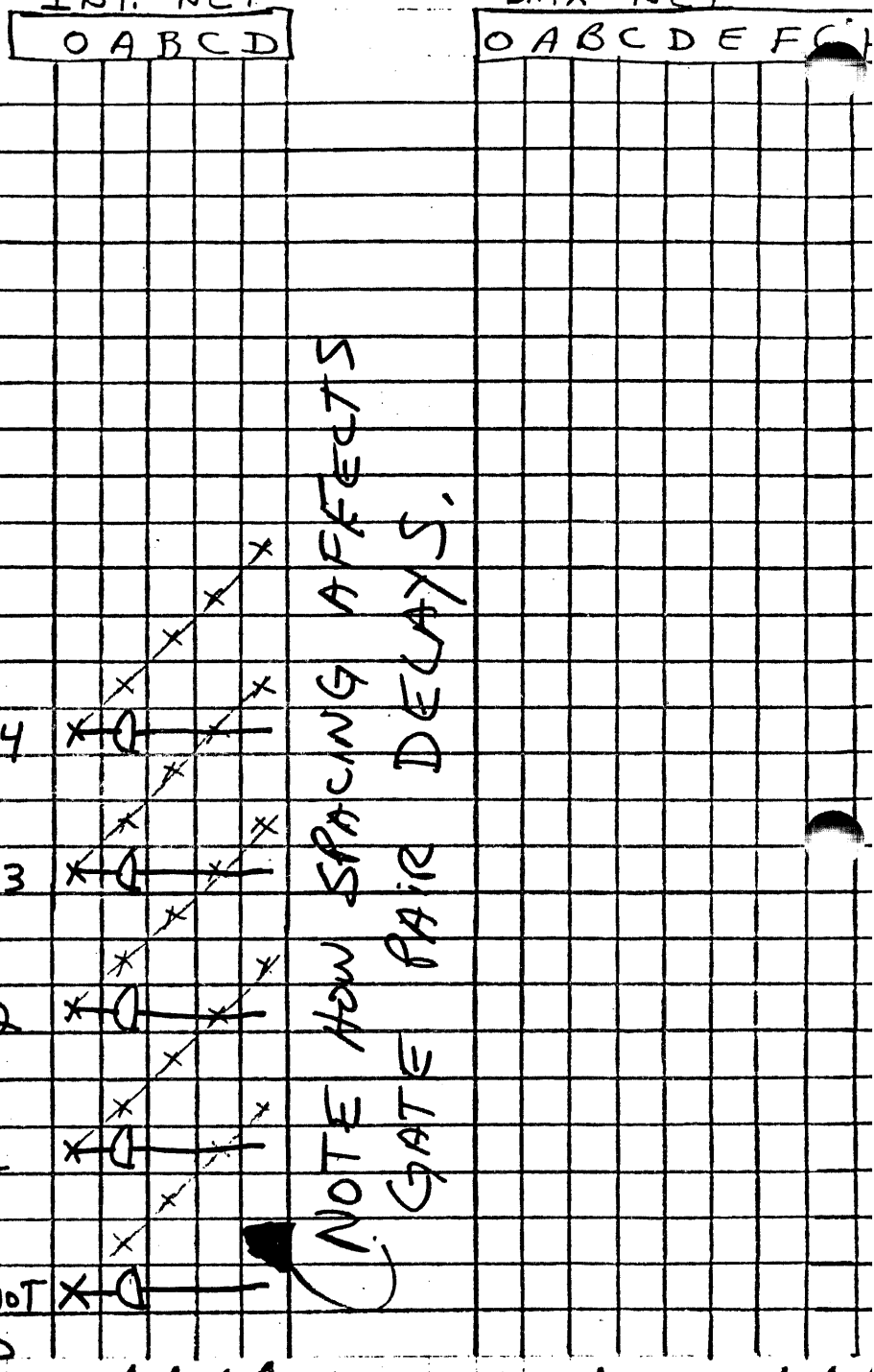
OPTION	SLOT NO.
8K MEMORY	27
	26
	25
	24
	23
	22
	21
8K MEMORY	20
MAG TAPE	19
	18
* MSLC	17
	16
CPU	15
	14
WCS	13
	12
OPT A	11
AMLC	10
	9
AMLC	8
	7
DS	6
	5
* MACI	4
	3
OPT B	2
	1



* NOTE: WERE LEFT OUT OF BKPL AT TIME OF SHIPMENT BUT DONT BREAK PRIORITY NETWORK

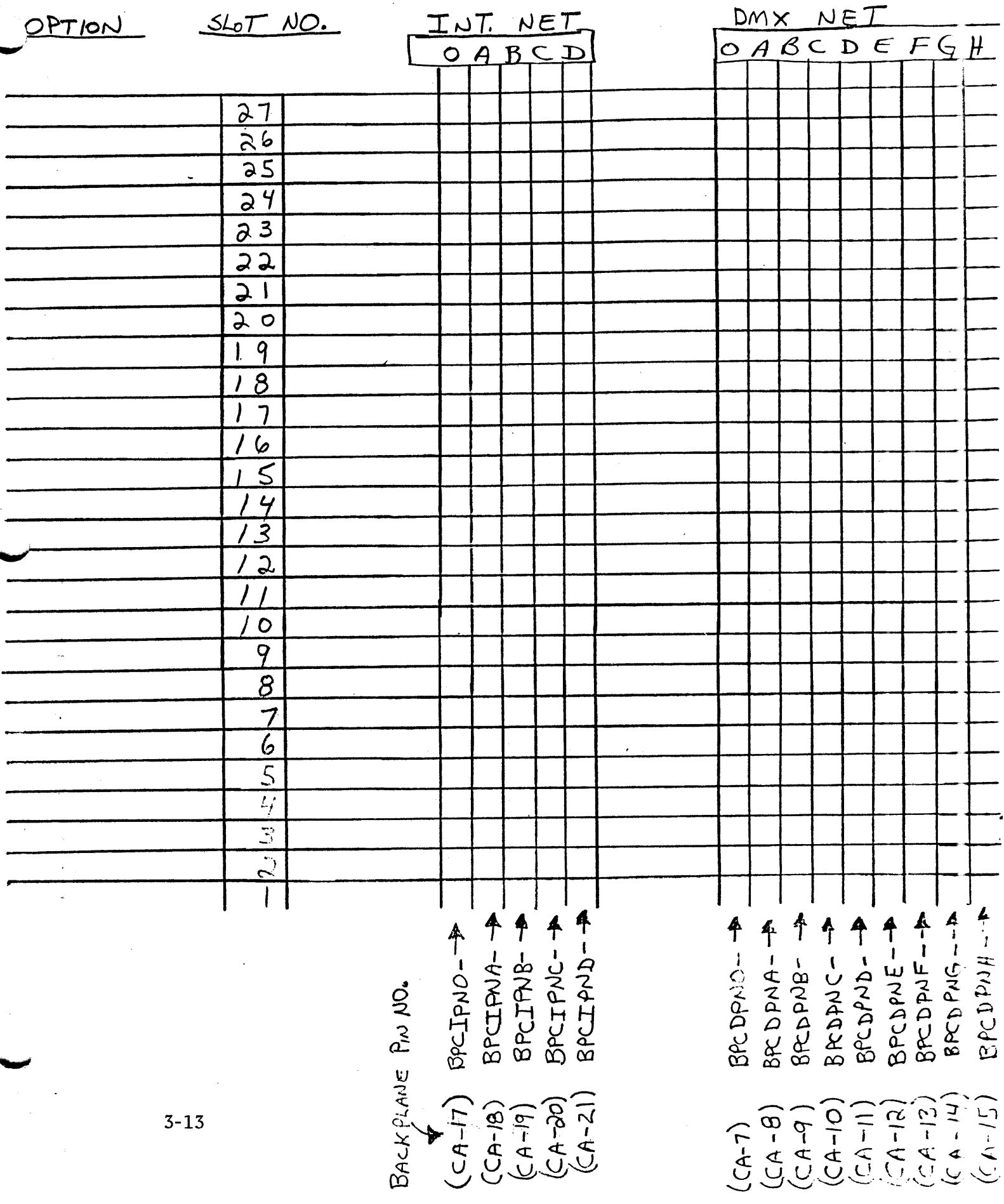
EXAMPLE 4

OPTION	SLOT NO.	
	27	
	26	
ANY OPTION IN A SLOT AFTER 18 IS exceeding the spec.	25	
	24	
	23	
	22	
	21	
	20	
	19	
	18	
	17	
	16	
	15	
MSLC	14	gate pair 4
	13	
	12	
AMLC	11	gate pair 3
	10	
	9	
AMLC	8	gate pair 2
	7	
	6	
AMLC	5	gate pair 1
	4	
	3	
OPTION B	2	gate pair NOT COUNTED
	1	



VERY POOR CONFIGURATION

BACKPLANE CONFIGURATION - PRIORITY NETWORK



SYSTEM CONFIGURATIONS WITH 32K MEMORY BOARDS

This memo discusses the system characteristics of the 32K board relative to power, physical slot location, and mixing with 8K boards.

Characteristics:

1. The 32K board has approximately the same power requirements as the 8K board.

2. The PRIME power supplies will support eight boards maximum. Therefore, no combination of the two board types may exceed this maximum.

3. The present 32K board operates at 750 ns read cycle and 600 ns access. It is therefore compatible with the P100, P300 and the P300 with P200 memory interface timing. ECO #1511, 1512 must be installed in a CPU to make it compatible with this memory.

4. It is anticipated that a faster version of this board will be available in 2Q75 and will operate at the standard P300 speeds of 600 ns cycle and 440 ns access.

5. Timing adjustments are made on the board with the cycle being initiated by PRECH. No adjustments are necessary or permitted.

6. The attached charts (A and B) show the response of the 8K and 32K modules to address stimulus for the various physical slots. Referring to these charts, one can see that multiple configurations are permitted.

   For a 10 slot backplane:

   1. 8K modules are addressed sequentially from slot 10 to slot 1 permitting addressing up to 80K. The 32K modules are addressed sequentially from slot 10 through slot 3 permitting addressing up to 256K. Slots 2 and 1 repeat the selection of up to 32K and up to 64K. Therefore, for a machine having 128K, it is possible to configure four 32K boards in the following ways:

      1. 10, 9, 8, 7

      2. 2, 9, 8, 7

      3. 10, 1, 8, 7

      4. 2, 1, 8, 7

For a 17 slot backplane:

1. 8K modules are addressed sequentially from slot 17 through slot 1 permitting addressing up to 136K. The 32K modules are addressed sequentially from slot 17 to slot 10 permitting up to 256K. Slots 9 to 2 repeat the sequence of up to 256K and slot 1 becomes the third slot addressing the first 32K of memory. Again for a 128K system there are numerous combinations of slot assignments:

    1. 17, 16, 15, 14
    2. 9, 8, 7, 6
    3. 17, 16, 7, 6
    4. 9, 8, 15, 14
    5. etc., etc.

Mixing Modules:

The 8K and 32K boards may be mixed in a system provided that there is no overlap in address space per charts A and B. If contiguous memory addressing is required, it is generally easier to use the 32K boards in the lower addressing space.

Example 1 - Upgrade 32K of 8K modules (4) to 96K.

Solution I - 1. 32K board slot 17
2. 32K board slot 16
3. 8K board slot 9
8K board slot 8
8K board slot 7
8K board slot 6

Solution II - 1. 8K board slot 17
8K board slot 16
8K board slot 15
8K board slot 14
2. 43K board slot 8
3. 32K board slot 7

Example 2 - Upgrade 48K of 8K modules (6) by adding two 32K modules and obtaining 112K.

Solution I - 1. 32K board slot 17
2. 32K board slot 16
3. 8K board slot 9
4. 8K board slot 8
5. 8K board slot 7
6. 8K board slot 6
7. 8K board slot 5
8. 8K board slot 4

Solution II - 1. 8K board slot 17
2. 8K board slot 16
3. 8K board slot 15
4. 8K board slot 14
5. 32K board slot 8
6. 32K board slot 7
7. 8K board slot 5
8. 8K board slot 4

DOS/VM:

The above examples illustrated means of obtaining contiguous memory with mixed boards. DOS/VM requires that the first 32K be contiguous, but the remaining memory may have "holes" in the addressing scheme. Therefore, there is some added flexibility in configuring this type of system.

Chart A

10 Slot

Slot Number	Slot Address Bits	Memory Increment 8K Bd	32K Bd
10	11111	8	32
9	11110	16	64
8	11101	24	96
7	11100	32	128
6	11011	40	160
5	11010	48	192
4	11001	56	224
3	11000	64	256
2	10111	72	32
1	10110	80	64

Chart B

17 Slot

Slot Number	Slot Address Bits	Memory Increment 8K Bd	32K Bd
17	11111	8	32
16	11110	16	64
15	11101	24	96
14	11100	32	128
13	11011	40	150
12	11010	48	192
11	11001	56	224
10	11000	64	256
9	10111	72	32
8	10110	80	64
7	10101	88	96
6	10100	96	128
5	10011	104	160
4	10010	112	192
3	10001	120	224
2	10000	128	256
1	01111	136	32

SYSTEM CONFIGURATION OF XCS

CPU and XCS or Floating Point should both be powered from the same power supply on the same backplane.

All Writeable Control Store configuration should be configured below the CPU.