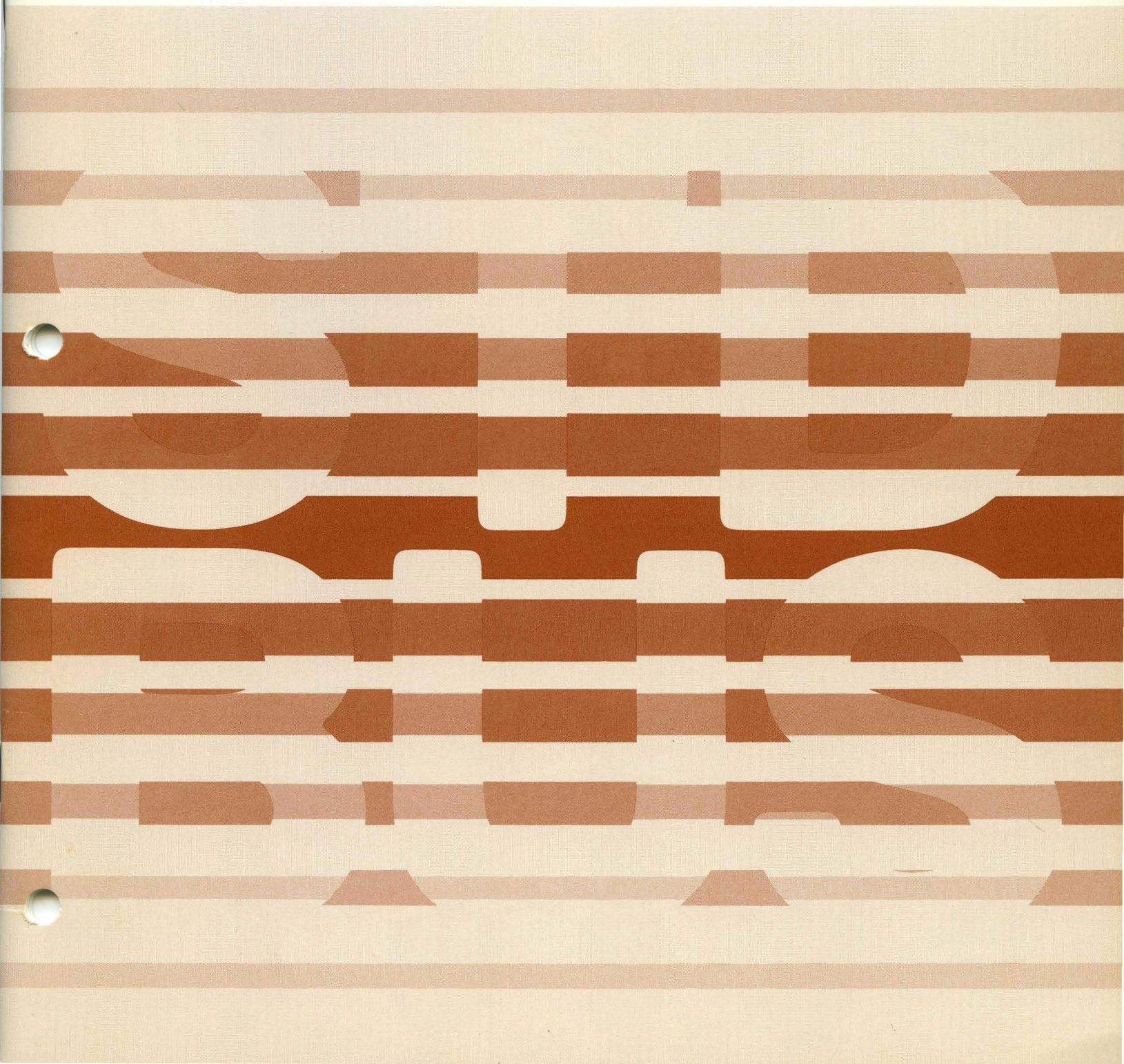
PRO-LOG CORPORATION

STD 7000

7304
Dual UART Card

USER'S MANUAL



7304
Dual UART Card
USER'S MANUAL

PRELIMINARY

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PRODUCT OVERVIEW

The 7304 provides two, fully independent, RS-232C serial data communication channels on a single STD card. Asynchronous operation up to 19,200 baud is supported for full duplex DTE (Data Terminal Equipment) or DCE (Data Communications Equipment) applications.
Capabilities include a TTY interface provision for one channel and polled interrupt logic for both channels.

PRODUCT FEATURES

RS-232C Serial Interface specification
Dual, independent 8241A USARTS
Independent program selectable baud rates to 19200 baud for RS-232C
Independent polled interrupt logic
Connection available for 7320 priority interrupt card
Selectable DTE/DCE configuration for each channel
Dual 26 pin male header connectors
+5V, ±12V operation
Socketed ICs
ASR-33 TTY interface circuit
Fully compatible with 7801, 7802, and 7803 CPU cards

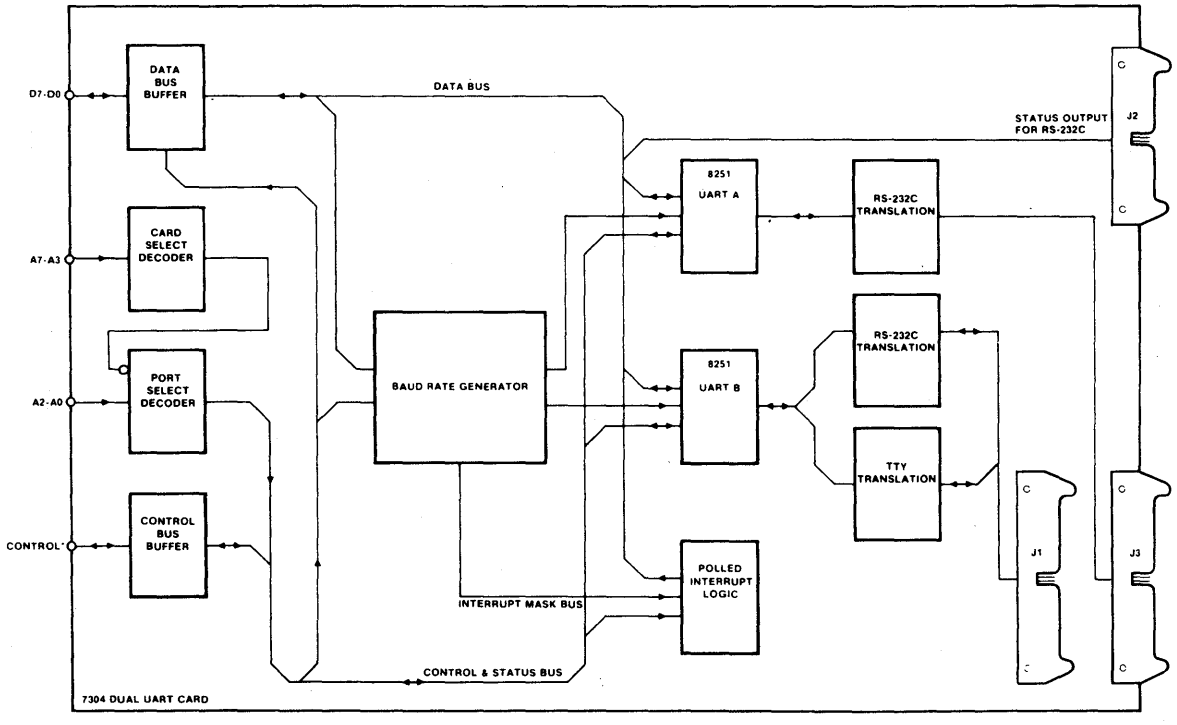


FIGURE 1
7304 BLOCK DIAGRAM

FUNCTIONAL CAPABILITY

- Industry standard 8251A USART, functional in asynchronous mode of operation only
- Asychronous RS-232C operation to 19,200 baud
- Independent baud rates of 110, 150, 300, 1200, 1800, 2400, 4800, 9600 and 19,200 baud.
- Variable character length of 5, 6, 7 or 8 bits
- Optional parity checking for odd or even parity
- Varible stop time of 1, 1 1/2, or 2 stop bits
- Optional configuration for data terminal equipment or data communications equipment
- Transmit handshake capability (CTS, RTS)
- Equipment status handshake capability (DTR, DSR)
- Overrun detection
- Polled interrupt logic on board for use with 8085, Z80 and 6800.
- Vectored interrupt available using 7320 Priority Interrupt Card
- TTY interface for one channel using Pro-Log standard

MAPPING

- Occupies 8 read/write ports
- Standard mapping of EØ through E7
- Remapping allowed by changing wire jumpers

ENVIRONMENTAL SPECIFICATIONS

- Free air operating temperature from $0^{o}C$ to $55^{o}C$
- Free air storage temperature from $-40^{o}C$ to $75^{o}C$
- Operating humidity from 0% to 95% non-condensing relative humidity

POWER REQUIREMENTS

- Vcc requirement of +5 ±0.25 volt at 660mAmp maximum
- Aux +V requirement of +12 ± 0.60 volt at 120mAmp maximum
- Aux -V requirement of -12 ± 0.60 volt at 120mAmp maximum

RS-232C INTERFACE SPECIFICATIONS

- High level output at +9.0 volt minimum
- Low level output at -9.0 volt maximum
- High level short circuit current of +12.0 mAmp maximum
- Low level short circuit current of -12.0 mAmp maximum
- Output range of change of 30 volt/user maximum

J1 CONNECTOR PIN LIST FOR RS-232C					
PIN NUMBER	SIGNAL FLOW	SIGNAL	PIN NUMBER	SIGNAL FLOW	SIGNAL
		2	1		
		4	3	IN/OUT	TXD (BA)
		6	5	IN/OUT	RXD (BB)
		8	7	IN/OUT	RTS (CA)
		10	9	IN/OUT	CTS (CB)
		12	11	IN/OUT	DSR (CC)
DTR (CD)	IN/OUT	14	13		SIGNAL GND (AB)
		16	15		
		18	17		
		20	19		
		22	21		
		24	23		
		26	25		

CONNECTOR J1 PIN LIST FOR RS-232C

J3 CONNECTOR PIN LIST FOR RS-232C					
PIN NUMBER	SIGNAL FLOW	SIGNAL	PIN NUMBER	SIGNAL FLOW	SIGNAL
		2	1		
		4	3	IN/OUT	TXD (BA)
		6	5	IN/OUT	RXD (BB)
		8	7	IN/OUT	RTS (CA)
		10	9	IN/OUT	CTS (CB)
		12	11	IN/OUT	DSR (CC)
DTR (CD)	IN/OUT	14	13		SIGNAL GND (AB)
		16	15		
		18	17		
		20	19		
		22	21		
		24	23		
		26	25		

CONNECTOR J3 PIN LIST FOR RS-232C

J1 CONNECTOR PIN LIST FOR TTY						
PIN NUMBER	SIGNAL FLOW	SIGNAL	PIN NUMBER	SIGNAL FLOW	SIGNAL
TAPE DRIVE	OUT	2	1	IN	TAPE RETURN
TRANSMIT DRIVE	OUT	4	3		
TRANSMIT RETURN	IN	6	5		
RECEIVE INPUT	IN	8	7	OUT	RECEIVE RETURN
		10	9	OUT	PULL-UP
		12	11		
		14	13		
		16	15		
		18	17		
		20	19		
		22	21		
		24	23		
		26	25		

CONNECTOR J1 PIN LIST FOR TTY

STD/7304 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
+5 VOLTS	IN		2	1		IN	+5 VOLTS
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	1	60	8	7	60	1	D3
D6	1	60	10	9	60	1	D2
D5	1	60	12	11	60	1	D1
D4	1	60	14	13	60	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*	1		32	31	1		WR*
MEMRQ*			34	33	1		IORQ*
MEMEX*			36	35	1		IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*		60	44	43	1		INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47	1		SYSRESET*
CNTRL*			50	49			CLOCK*
PC1	IN		52	51		OUT	PC0
AUX GND			54	53			AUX GND
AUX-V (-12V)	IN		56	55		IN	AUX +V (+12V)

* Low Level Active

Edge Connector Pin List

STD CONNECTOR PIN LIST

2 FUNCTIONAL OPERATION AND PROGRAMMING

The operation of each data channel may be divided into three functional areas. The first area involves programming the 8251A USART which includes mode control/commands, status, parallel data output and parallel data input. Because the characteristics of this industry standard USART are unaltered for asynchronous operation in this application, only a short description of operation will be included here. For an extended description of operation, consult one of the major suppliers of the this integrated circuit.

8251A OPERATION AND PROGRAMMING

The 8351A must be reset following power on and maybe reset at any following time after completion of an operation and before a new operation is started. After a reset, the USART enters an initialization state where it waits for two bytes from the CPU. Note that during this initialization state the USART may neither transmit nor receive data. The first byte sent after reset is interpreted by the USART as a control byte.

CONTROL BYTES

After reset the first byte sent to the command register is interpreted as a control byte. The control byte format is shown in Figure 2. Control codes bits 1 and 0 must be set to a non-zero value to define asynchronous operation and to define the relationship between data transfer baud rate and receiver or transmitter clock rate. Note that the 7304 supports the asynchronous mode of operation only. Asynchronous serial data may be received or transmitted on every clock pulse, on every 16th clock pulse, or on every 64th clock pulse. Normally these two bits should be programmed as 10 to select the 16X baud rate factor. See figure 5 for further details.
Control bits 3 and 2 determine the number of data bits which will be present in each data character.

Bits 5 and 4 determine whether there will be a parity bit in each character, and if there is, whether odd or even parity will be used when transmitting or when checking during receiving.

Control bits 7 and 6 determine the number of stop bits that will be appended to each serial byte when transmitting and the number allowed when receiving each serial byte.

COMMAND BYTE

After reset the second byte and every subsequent byte thereafter sent to the command register is interpreted as a command byte. The command byte may therefore be sent at any time to control the USART operation. The format of the command word is shown in Figure 3.

Bit 0 of the command word is the transmit enable bit. Output data from the USART cannot take place unless this bit is in the active state.

D7	D6	D5	D4	D3	D2	D1	D0
STOP BIT		EVEN PARITY	PARITY ENABLE	BITS/CHARACTER		RATE FACTOR	

STOP BIT - 00 INVALID
01 1 STOP BIT
10 1 1/2 STOP BITS
11 2 STOP BITS

EVEN PARITY - 0 ODD PARITY
1 EVEN PARITY

PARITY ENABLE - 0 PARITY DISABLE
1 PARITY ENABLE •

BITS/CHARACTER - 00 5 BITS PER CHARACTER
01 6 BITS PER CHARACTER
10 7 BITS PER CHARACTER
11 8 BITS PER CHARACTER

RATE FACTOR - 00 INVALID
01 ASYNC MODE 1X BAUD RATE
10 ASYNC MODE 16X BAUD RATE
11 ASYNC MODE 64X BAUD RATE

FIGURE 2

CONTROL BYTE FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
---	SR	TH	ER	SBRK	REN	ERO	TEN

SR - SOFTWARE RESET - 0 INACTIVE
1 MOMENTARY ACTIVE

TH - TRANSMITE HANDSHAKE - 0 INACTIVE
1 ACTIVE (RTS FOR DTE CTS FOR DCE)

ER - ERROR FLAG RESET - 0 INACTIVE
1 MOMENTARY ACTIVE

SBRK - SEND BREAK - 0 INACTIVE
1 ACTIVE

REN - RECEIVE ENABLE - 0 INACTIVE
1 ACTIVE

ERO - EQUIPMENT READY OUTPUT - 0 INACTIVE
1 ACTIVE (DTR FOR DTE, DSR FOR DCE)

TEN - TRANSMIT ENABLE - 0 INACTIVE
1 ACTIVE

FIGURE 3

COMMAND BYTE FORMAT

Bit 1 of the command word is the equipment ready output bit. When the 7304 channel is configured as DTE, this bit sends the data terminal ready (DTR) message. When the 7304 channel is configured as DCE, this bit sends the data set ready (DSR) message.

Bit 2 is the receive enable command bit. This bit is used to enable the received ready signal. This bit does not prevent the assembly of serial characters, however. Note that an overrun error may occur if characters are continuously sent. To insure proper operation, the overrun error is usually reset with the same command that sets the receive enable command bit.

Bit 3 is the send break command bit. When this bit is set, the serial transmitted data is interrupted and a continuous low level (spacing) signal is transmitted. This signal will be sent continuously as long as this bit is set.

Bit 4 is the error reset bit. This bit clears the three error flags in the status register. This bit performs a momentary function.

Bit 5 is the transmit handshake bit. When the 7304 is configured as DTE, this bit sends the request to send (RTS) message. When the 7304 is configured as DCE, this bit sends the clear to send (CTS) message.

Bit 6 is the software reset bit. The USART channel enters the initialize state. This bit performs a momentary function. For a description of the initialized state, see the beginning of this section.

STATUS BYTE

The status byte for each channel may be obtained by reading the port address shown in Figure 6 . The format of the status byte is shown in Figure 4

Bit 0 is the transmit ready bit. This bit indicates that the transmit character buffer is empty and that the USART can accept a new character for transmission. This bit is cleared when the transmit buffer is loaded by the CPU.

Bit 1 is the receive ready bit. This bit indicates that the receive buffer has a character available. This bit is cleared when the receive buffer has been emptied by the CPU.

Bit 2 indicates when the transmit output buffer is empty.

Bit 3 is the parity error signal which indicates that the received character has an error. This bit is reset by the error reset bit in the command word.

Bit 4 is the overrun error bit which indicates that the received character has been overwritten by the next character. This bit is reset by the error reset bit in the command word.

Bit 5 is the framing error bit which indicates that the received character had either an incorrect number of bits or the wrong number of stop bits. This bit is reset by the error reset bit in the command word.

D7	D6	D5	D4	D3	D2	D1	D0
ERI	---	FE	OE	PE	TOE	RRDY	TRDY

ERI - EQUIPMENT READY INPUT - 0 INACTIVE
1 ACTIVE (DSR FOR DTE, DTR FOR DCE)

FE - FRAMING ERROR - 0 INACTIVE
1 ACTIVE

OE - OVERRUN ERROR - 0 INACTIVE
1 ACTIVE

PE - PARITY ERROR - 0 INACTIVE
1 ACTIVE

TOE - TRANSMIT OUTPUT BUFFER EMPTY - 0 INACTIVE
1 ACTIVE

RRDY - RECEIVE READY BIT - 0 INACTIVE
1 ACTIVE

TRDY - TRANSMIT READY BIT - 0 INACTIVE
1 ACTIVE

FIGURE 4

STATUS BYTE FORMAT

Bit 6 is not used.

Bit 7 is the equipment ready input bit. When the 7304 channel is configured as DTE, this bit indicates the state of data set ready (DSR) line. When the 7304 channel is configured as DCE, this bit indicates the state of the data terminal ready (DTR) line.

BAUD RATE OPERATION AND PROGRAMMING

Each channel of the 7304 must have the buad rate selected before data can be transmitted or received. This is accomplished by writing to the baud rate register with the appropriate value as shown in Figure 5. Normally the baud rate is selected before the 8251 control and command bytes are programmed.

The transmit and receive baud rates are equal for each channel. The baud rates for each channel are completely independent from each other. This is accomplished by generating all eight baud rate frequencies simultaneously. The baud rate multiplexer for each channel then selects the frequency desired for that channel.

The two interrupt enable bits for each channel will be described in the interrupt programming section.

INTERRUPT OPERATION AND PROGRAMMING

The 7304 has a polled interrupt capability for each channel. This logic will generate an interrupt request to the CPU if the interrupt is enabled and the interrupt condition becomes true. Combined enables for transmit and receive ready conditions are located in the baud rate register and must be set to 'one' for an interrupt to occur. Conditions causing an interrupt to occur include the transmit ready bit going true (TRDY-BIT 0 of the status byte) or the receive ready bit going true (RRDY-BIT 1 of the status byte) for either channel.

The interrupt is acknowledged (cleared) by the CPU taking action on the request. This would include reading a data byte for the RRDY bit becoming true or writing a data byte for the TRDY bit becoming true. The CPU may determine the source of the interrupt by reading the status from each channel ("polling").

This method of interrupt processing is fully compatible with the Z80 Mode 1, 8085 and 6800. For use with other processor specific interrupt types, a connector is available for use with other interrupt controllers such as the 7320.

TTY CONFIGURATION

The 7304 contains a standard Pro-Log TTY interface circuit. The capability may be selected only for channel B by placing an on-board configuration jumper in the correct position (see Mechanical Section). This interface operates only as DCE at speeds up to 300 baud. See the 7301 Data Sheet for further details.

D7	D6	D5	D4	D3	D2	D1	D0
EA	BAUD RATE A			EB	BAUD RATE B		

BAUD RATE A AND B (for x16 factor)	000	110 BAUD
	001	150 BAUD
	010	300 BAUD
	011	1200 BAUD
	100	1800 BAUD
	101	2400 BAUD
	110	4800 BAUD
	111	9600 BAUD

BAUD RATE A AND B (for x1 factor)	000	1760 BAUD
	001	2400 BAUD
	010	4800 BAUD
	011	19200 BAUD
	100	---
	101	---
	110	---
	111	---

EA - INTERRUPT ENABLE CHANNEL A 0 DISABLE INTERRUPT
1 ENABLE INTERRUPT

EB - INTERRUPT ENABLE CHANNEL B 0 DISABLE INTERRUPT
1 ENABLE INTERRUPT

FIGURE 5

BAUD RATE REGISTER FORMAT

3 MAPPING

The 7304 appears to the programmer as a series of ports as shown in Figure 6 Each UART channel has a read data/write data port, a command/status port, and a baud rate select port.

The I/O ports of the 7304 are selected by a decoded combination of address lines A7 through A0. The 7304 is shipped with the port assignments shown in Figure 6 The user may change the port address assignments by changing jumper wires SX and SY. Refer to Figure 13 for the position of SX and SY. Refer to the Series 7000 STD BUS Technical Manual for additional card mapping information for the eight port per card scheme.

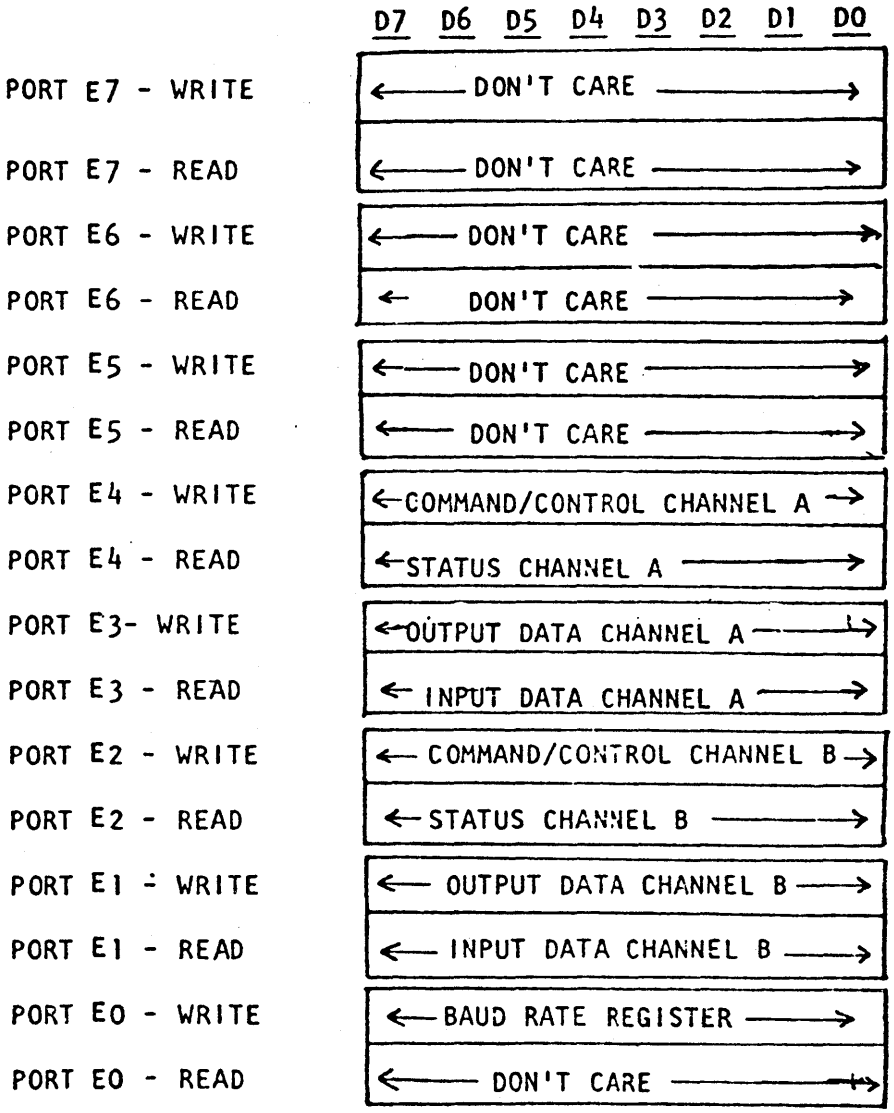


FIGURE 6

7304 MAPPING

4. OPERATION AND PROGRAMMING EXAMPLES

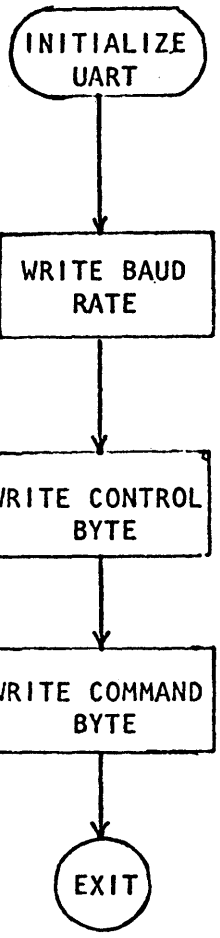
Typical operation of the 7304 involves three basic functions. These functions include:

1. Initializing the UART
2. Writing a character to the UART
3. Reading a character from the UART

A flowchart of each operation is included with subroutines for Pro-Log's 7801 808 5A CPU card.
The initialize subroutine first sets the desired baud rate as shown in Figure 7. Because interrupt processing is not needed in this example, the interrupt enable bit will be set to zero for the desired channel. The control byte is written out next with bits set as shown in Figure 2. The command byte is written out last with bits shown in Figure 3. Because a control byte is sent there is an assumption that the subroutine is called only once after power on or system reset. See Section 2 for further details.

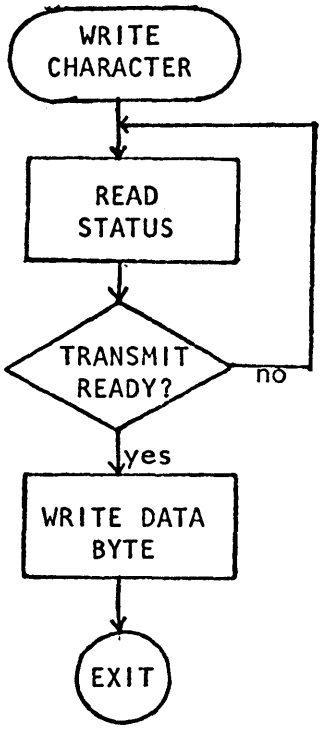
To write a character out, the flowchart in Figure 8 may be used. The first operation performed is reading the UART status to determine if the UART transmitter is ready for a data byte. If it is, the data character is output to the data port. If the UART is not ready, the program waits until it is ready. After the character is output the subroutine exits.

To read a character in, the flowchart in Figure 9 may be used. The first operation performed is reading the UART status to determine if the UART receiver has received a data byte. If no character has been received, the program waits until a data byte is input. When the input character has been assembled into an 8-bit wide character in the receiver, several checks are made to determine if the character is valid. The parity of the character is checked against the parity bit to determine if any bits in the character were altered. An overrun error is detected if the current byte was sent while the previous byte was still in the UART. This error indicates the microprocessor system is not servicing the UART fast enough. A framing error is detected if either an incorrect number of data bits were received or if an incorrect number of stop bits were used to terminate the character. If any of these error conditions are true, an error flag in memory is set, the UART error is reset, and the subroutine exits. If the data byte is error-free, the data byte is read, the correct number of bits is masked off, and the subroutine exits.



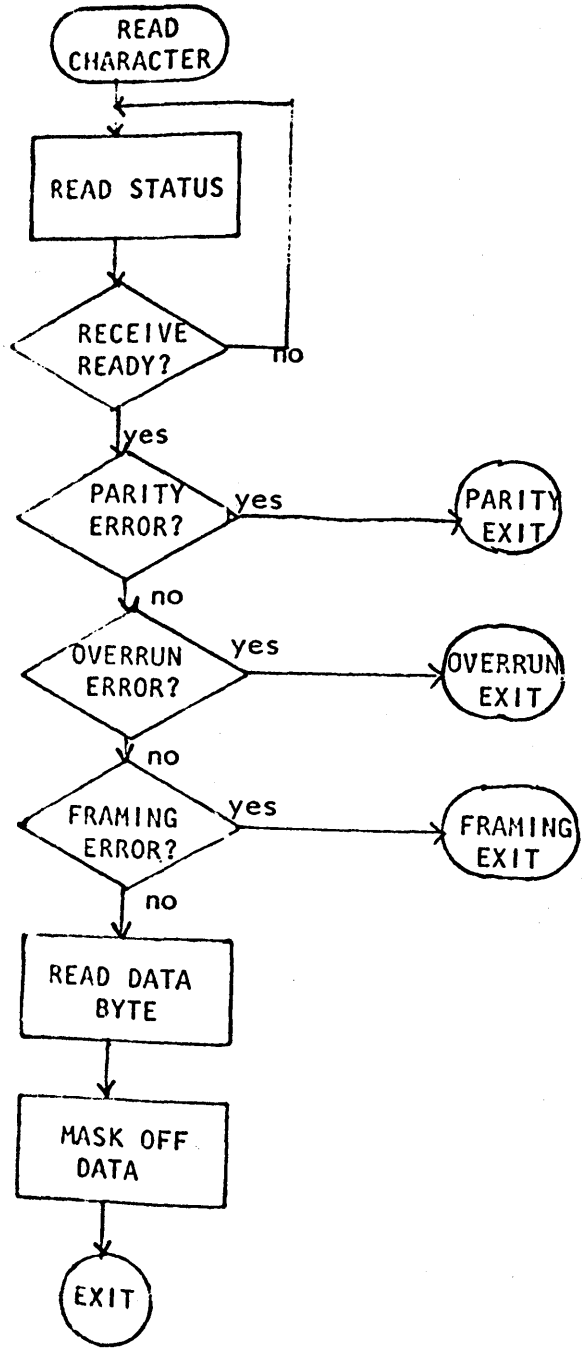
INITIALIZE UART FLOWCHART

FIGURE 7



WRITE CHARACTER FLOWCHART

FIGURE 8



READ CHARACTER FLOWCHART
FIGURE 9

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR	MNEMONIC MODIFIER	TITLE / COMMENTS / DATE
11	00	00	INITIALIZE UART	NOP		
	1	00		NOP		
	2	00		NOP		
	3	3E		LDAI		- WRITE BAUD RATE
	4	33		-	33	←1200 B MASK A
	5	D3		OPA		
	6	E0		-	E0	
	7	3E		LDAI		- WRITE CONTROL BYTE
	8	CA		-	CA	←2 STOP BITS, NO PARITY, 8 BITS PER CHAR, 1X BAUD
	9	D3		OPA		
	A	E4		-	E4	
	B	D3		OPA		
	C	E2		-	E2	
	D	3E		LDAI		- WRITE COMMAND BYTE
	E	37		-	37	
	F	D3		OPA		
	0	E4		-	E4	
	1	D3		OPA		
	2	E2		-	E2	
	3	C9		RTS		
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

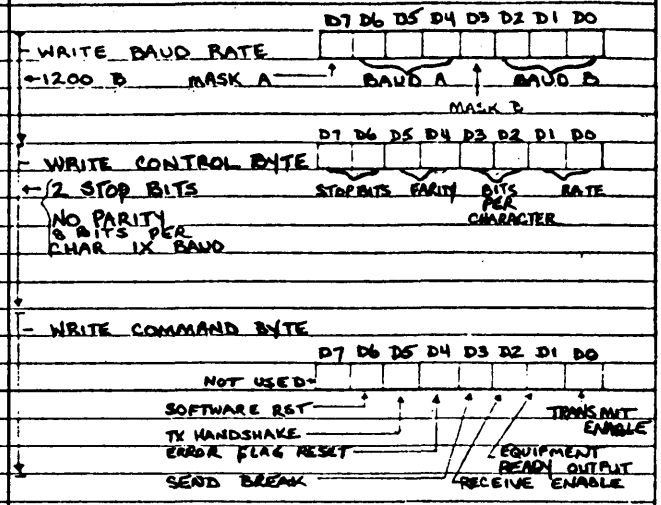


FIGURE 10 - INITIALIZE SUBROUTINE FOR 8085

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR	MNEMONIC MODIFIER	TITLE / COMMENTS / DATE
11	20	DB	(WRITE UART A)	IPA		- WAIT FOR READY
	1	E4		-	UART CONTROL (A)	
	2	E6		ANAI		
	3	01		-	01	
	4	CA		JP	Z1	
	5	20		-	(WRITE UART A)	
	6	11		-		
	7	7E		LDA	M(HL)	- WRITE ASCII
	8	D3				
	9	E3		-	UART DATA (A)	
	A	C9		RTS		
	B					
	C					
	D					
	E					
	F					
11	30	DB	(WRITE UART B)	IPA		- WAIT FOR READY
	1	E2		-		
	2	E6		ANAI		
	3	01		-	01	
	4	CA		JP	Z1	
	5	30		-	(WRITE UART B)	
	6	11		-		
	7	7E		LDA	M(HL)	- WRITE ASCII
	8	D3		OPA		
	9	E1		-	UART DATA (B)	
	A	C9		RTS		
	B					
	C					
	D					
	E					
	F					

FIGURE 11 - WRITE SUBROUTINE FOR 8085

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PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR	MNEMONIC MODIFIER	TITLE / COMMENTS / DATE
11	40	DB	(READ CHARACTER A)	IPA		WAIT FOR EXITS WITH DATA IN MEMORY
	1	E4		-	UART CONTROL A	RECEIVE POINTED TO BY AL
	2	47		LDB	A	READY
	3	E6		ANAI		
	4	02		-	02	
	5	CA		JP	Z1	
	6	40		-	(READ CHARACTER A)	
	7	11		-		
	8	78		LDA	B	CHECK FOR PARITY ERROR
	9	E6		ANAI		
	A	08		-	08	
	B	C2		JP	Z0	
	C	XX		-		
	D	XX		-		
	E	78		LDA	B	
	F	E6		ANAI		
	50	10		-	10	
	1	C2		JP	Z0	
	2	XX		-	OVERRUN ERROR	
	3	XX		-		
	4	78		LDA	B	CHECK FOR FRAMING ERROR
	5	E6		ANA	I	
	6	20		-	20	
	7	C2		JP	Z0	
	8	XX		-	FRAMING ERROR	
	9	XX		-		
	A	DB		IPA		INPUT ASCII
	B	E3		-	UART DATA A	
	C	F6		ORAI		SET PARITY BIT
	D	80		-	80	
	E	77		STAN	(HL)	STORE IN MEMORY
	5F	C9		RTS		

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FIGURE 12. READ SUBROUTINE FOR 8085

PRO-LOG CORPORATION

PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR	MNEMONIC MODIFIER	TITLE / COMMENTS / DATE
11	60	DB	(READ CHARACTER B)	IPA		WAIT FOR EXITS WITH DATA IN MEMORY
	1	E2		-	UART CONTROL B	RECEIVE POINTED TO BY AL
	2	47		LDA	A	READY
	3	E6		ANAI		
	4	02		-	02	
	5	CA		JP	Z1	
	6	60		-	(READ CHARACTER B)	
	7	11		-		
	8	78		LDA	B	CHECK FOR PARITY ERROR
	9	E6		ANAI		
	A	08		-	08	
	B	C2		JP	Z0	
	C	XX		-	PARITY ERROR	
	D	XX		-		
	E	78		LDA	B	CHECK FOR OVERRUN ERROR
	6F	E6		ANAI		
	70	10		-	10	
	1	C2		JP	Z0	
	2	XX		-	OVERRUN ERROR	
	3	XX		-		
	4	78		LDA	B	CHECK FOR FRAMING ERROR
	5	E6		ANA	I	
	6	20		-	20	
	7	C2		JP	Z0	
	8	XX		-	FRAMING ERROR	
	9	XX		-		
	A	DB		IPA		INPUT ASCII
	B	E1		-	UART DATA B	
	C	F6		ORAI		SET PARITY BIT
	D	90		-	80	
	E	77		STAN	(HL)	STORE IN MEMORY
	7F	C9		RTS		

7304 DUAL UART CARD ENVIRONMENTAL SPECIFICATIONS

RECOMMENDED OPERATING LIMITS				ABSOLUTE NON-OPERATING LIMITS		
PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
Free Air Temperature	0	25	55	-40	75	°C
Humidity	0		95 ①	0	95 ①	%RH
Shock	Not Specified			Not Specified		
Vibration	"			"		
EMI	"			"		
ESD	"			"		

① NON-CONDENSING RELATIVE HUMIDITY

7304 DUAL UART CARD ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING LIMITS				ABSOLUTE NON OPERATING LIMITS		
PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
V_{CC}	4.75	5.00	5.25	0.0	7.00	Volt
AUX +V	11.40	12.00	12.60	0.0	15.00	Volt
AUX -V	-12.60	-12.00	-11.40	-15.0	0.0	Volt

RS-232C USER INTERFACE ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING LIMITS

PARAMETER	MIN	TYP	MAX	UNITS
HIGH LEVEL OUTPUT VOLTAGE (1)	9.0	10.0		Volt
LOW LEVEL OUTPUT VOLTAGE (1)		-10.0	-9.0	Volt
HIGH LEVEL SHORT-CIRCUIT CURRENT	+6.0	+10.0	+12.0	mA
LOW LEVEL SHORT-CIRCUIT CURRENT	-12.0	-10.0	-6.0	mA
HIGH LEVEL INPUT THRESHOLD VOLTAGE			3.0	Volt
LOW LEVEL INPUT THRESHOLD VOLTAGE	-3.0			Volt

(1) At termination resistance of 3.0K Ω minimum

TTY USER INTERFACE ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING LIMITS

PARAMETER	MIN	TYP	MAX	UNITS
HIGH LEVEL OUTPUT CURRENT (1)			0.0	mA
LOW LEVEL OUTPUT CURRENT (2)			25.0	mA
HIGH LEVEL INPUT CURRENT (1)			1.0	mA
LOW LEVEL INPUT CURRENT (2)			0.00	mA

(1) At a compliance voltage of +11.40 volt minimum

(2) At a voltage of 0.0 volt minimum

6. STD BUS ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATION LIMITS

PARAMETER	MIN	TYP	MAX	UNITS
Vcc SUPPLY CURRENT		400	660	mA
AUX +V SUPPLY CURRENT		76	120	mA
AUX -V SUPPLY CURRENT		72	120	mA
STD BUS INPUT LOAD	See Figure 17			
STD BUS OUTPUT DRIVE	See Figure 17			

6. SWITCHING CHARACTERISTICS OVER RECOMMENDED OPERATING LIMITS

PARAMETER	MIN	TYP	MAX	UNITS
RS-232C OUTPUT RATE OF CHANGE			30	V/μsec
RS-232C BAUD RATE			9600	Baud
CURRENT LOOP BAUD RATE		110	300	Baud

7 MECHANICAL

Refer to Figure 13 for component placement informaton. The 7304 meets all STD BUS general mechanical specifications. The 7304 requires one card slot in a standard STD BUS card rack.

To configure data communications Channel A for DTE or DCE modes of operation, shorting jumper block 'A' should be moved to the 'DTE' or 'DCE' positions shown in Figure 13. Physical connection to the RS-232C signals are provided at connector J3 which is a 26 pin locking male PC board header. Connection to the industry standard 25 pin 'D' connector should be made with a cable link equivalent to RC-25-M for the DTE configuration or RC-25-F for the DCE configuration. These assemblies are available from Pro-Log and are described in a separate data sheet.

Mechanical configuration of Channel B is similar to the procedure for Channel A. In addition, to configure Channel B for the TTY interface option, shorting jumper block 'B' should be moved to the 'TTY' position shown in Figure 13 Physical connection to the current loop signals are provided at connector J1 which is also a 26 pin locking male PC board header. Connection to the Pro-Log standard 9 pin 'D' connector should be made with a cable link equivalent to RC-9-M (see separate data sheet).

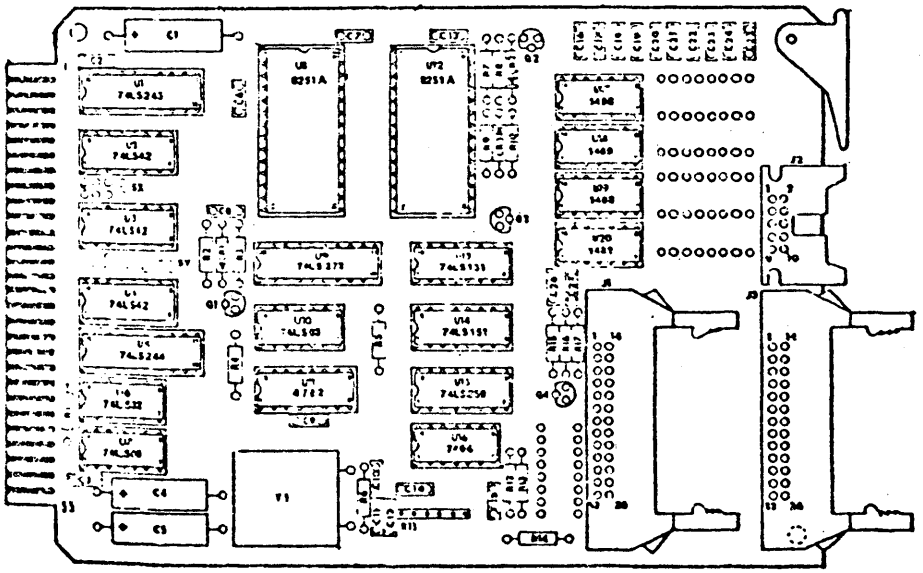

FIGURE 13

7304 COMPONENT PLACEMENT

USER'S MANUAL

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Monterey, California 93940
Telephone: (408) 372-4593
TWX: 910-360-7082

106242B 600 9/81