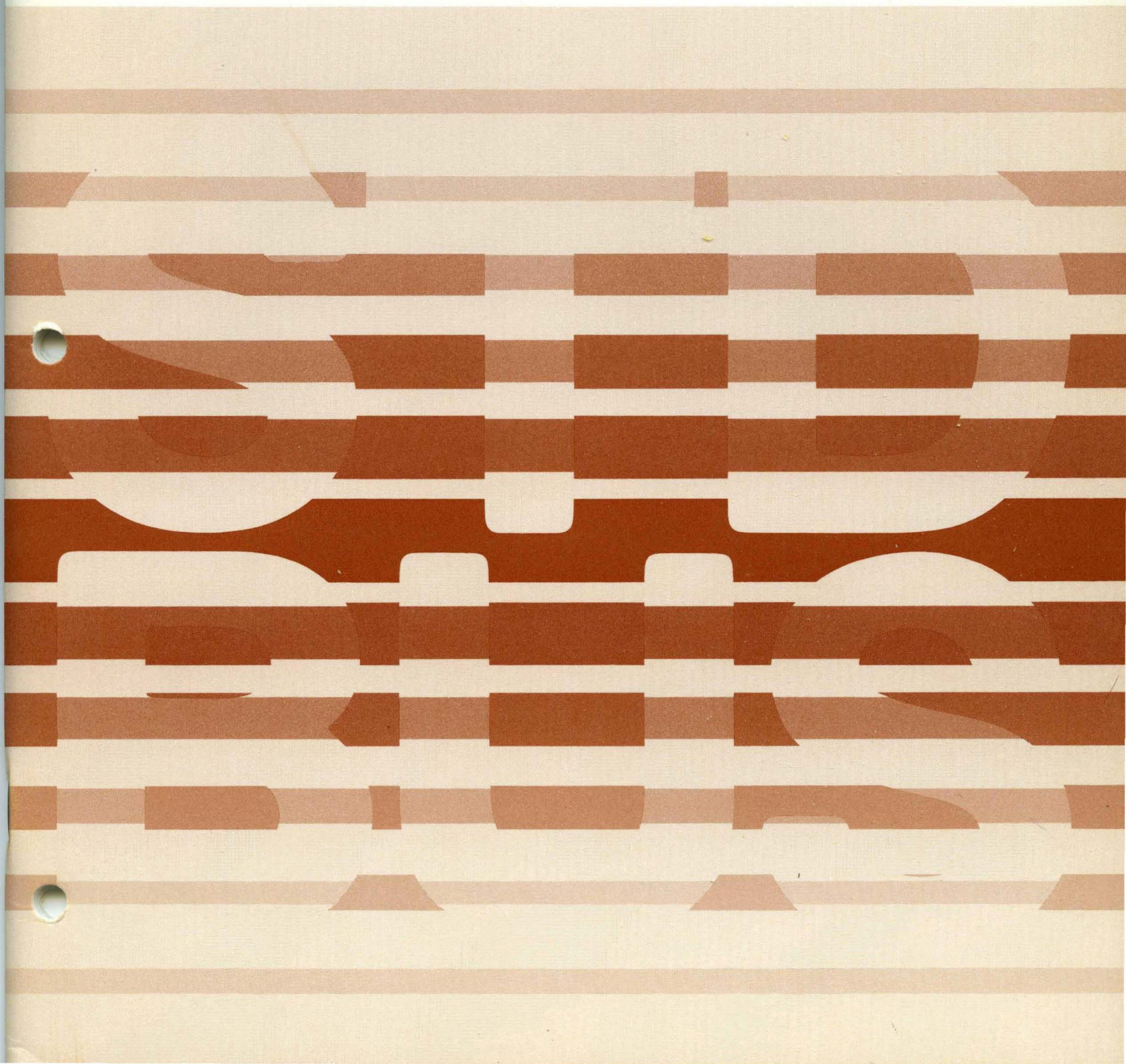
PRO-LOG
CORPORATION

STD 7000

7705
32K EPROM
Memory Card

USER'S MANUAL



NOTICE

The information in this document is provided for reference only. Pro-Log does not assume any liability arising out of the application or use of the information or products described herein.

This document may contain or reference information and products protected by copyrights or patents and does not convey any license under the patent rights of Pro-Log, nor the rights of others.

PRO-LOG
CORPORATION

STD 7000

7705
32K EPROM
Memory Card

USER'S MANUAL

FOREWORD

This manual explains how to use Pro-Log's 7705 32K EPROM Memory Card. It is structured to reflect the answers to basic questions that you, the user, might ask yourself about the 7705. We welcome your suggestions on how we can improve our instructions.

The 7705 is part of Pro-Log's Series 7000 STD BUS hardware. Our products are modular, and they are designed and built with second-sourced parts that are industry standards. They provide the industrial manager with the means of utilizing his own people to control the design, production, and maintenance of the company's products that use STD BUS hardware.

Pro-Log supports its products with thorough and complete documentation. Also, to provide maximum assistance to the user, we teach courses on how to design with, and to use, microprocessors and the STD BUS products.

You may find the following Pro-Log documents useful in your work: *Microprocessor User's Guide* and the *Series 7000 STD BUS Technical Manual*. If you would like a copy of these documents, please submit your request on your company letterhead.

Contents

Figures

SECTION 1
Purpose and Main Features

Purpose

The 7705 Card (Fig. 1-1) provides the user with eight sockets for 2732/2732A EPROMs, giving a total 32K bytes of memory. The memory resides in one continuous block, which can be mapped to either the upper or lower half of a 64K memory system. (See Fig. 1-2 for the block diagram.)

The 7705 can respond to the STD BUS MEMEX line, allowing two cards to reside in the same address field. A system using four 7705 cards, plus a Pro-Log processor card capable of controlling MEMEX, provides 124K bytes of memory with no additional cards or signal lines.

Also, the 7705 can respond to an external segment select line, allowing its use in large-scale bank select schemes. The segment select line can be controlled by a memory segment controller or by I/O ports. One output port controls eight 7705 cards. Also, the 7705 can be tailored to fit small-scale applications. Unused sockets can be disabled, allowing the card to occupy as little as 4K bytes of memory space, which can be mapped anywhere within a 64K-byte system.

Main Features

- **Eight 2732/A EPROM sockets — 32K-byte capacity**
- **User-selectable memory mapping**
- **No wasted memory space — unused sockets can be disabled**
- **Responds to STD BUS MEMEX line**
- **Responds to external segment select line**
- **Processor independent — use with 8085, Z80, 6800, 8088, and others.**

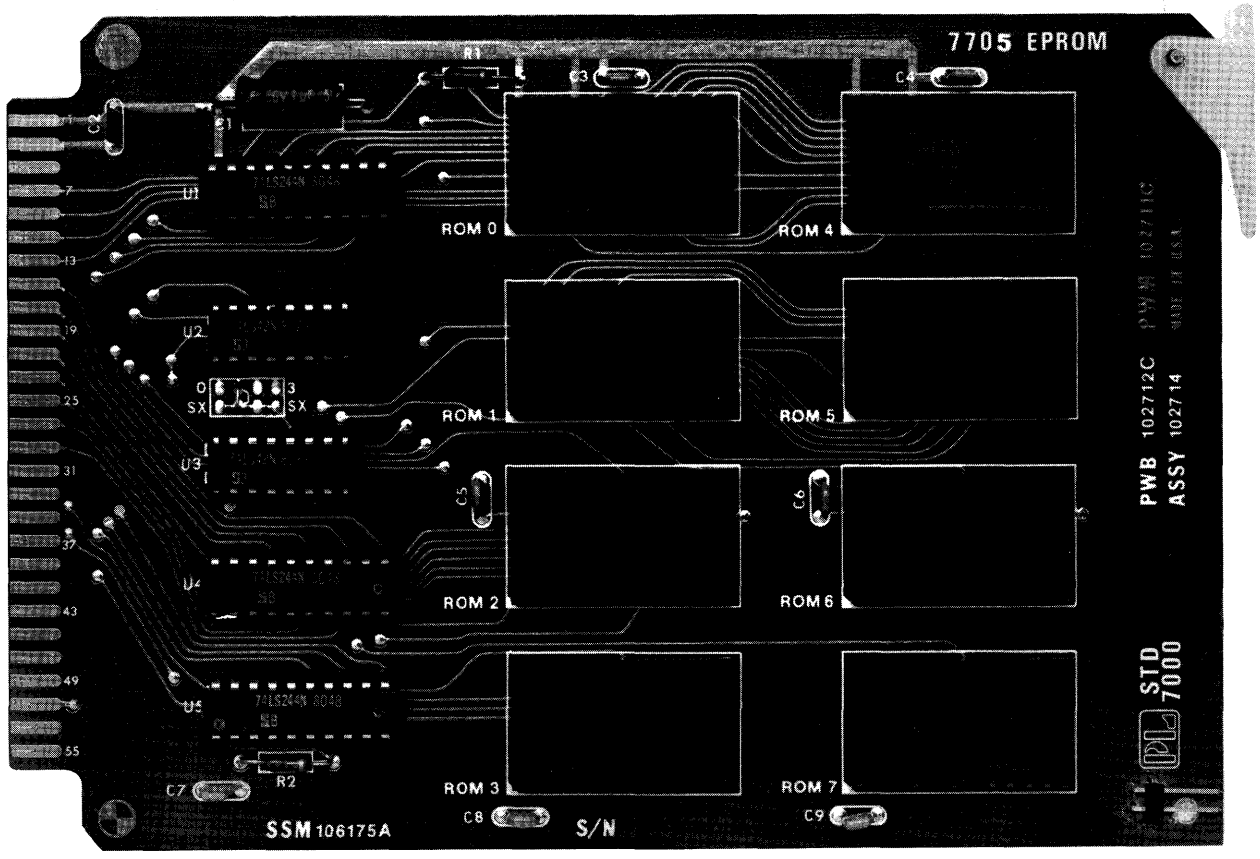


Figure 1-1. 7705 32K EPROM Memory Card

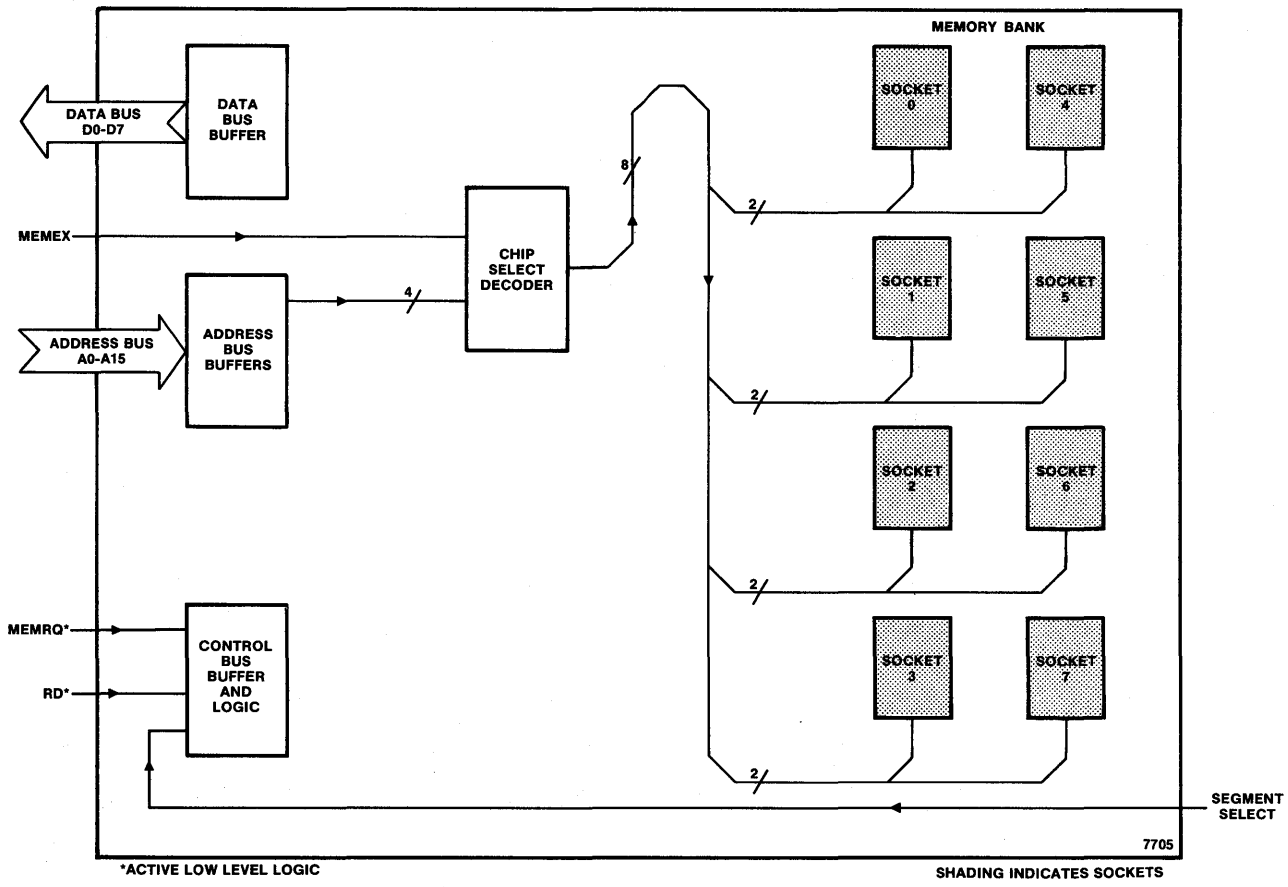


Figure 1-2. Block Diagram of 7705 32K EPROM Memory Card.

SECTION 2
Installation and Specifications

Introduction

The 7705 operates as part of an STD BUS card rack system. You can plug it directly into the STD BUS backplane, as shown in Fig. 2-1. Optionally, you can extend it from the motherboard with a 7901 card extender. Plug the 7901 into any slot in the card rack and then plug the 7705 into the connector on the 7901; this gives you access to the 7705 for testing or other purposes.

CAUTION

To prevent possible damage to your STD BUS system, make sure that power is off before inserting a card into the card rack, or before removing a card from the card rack.

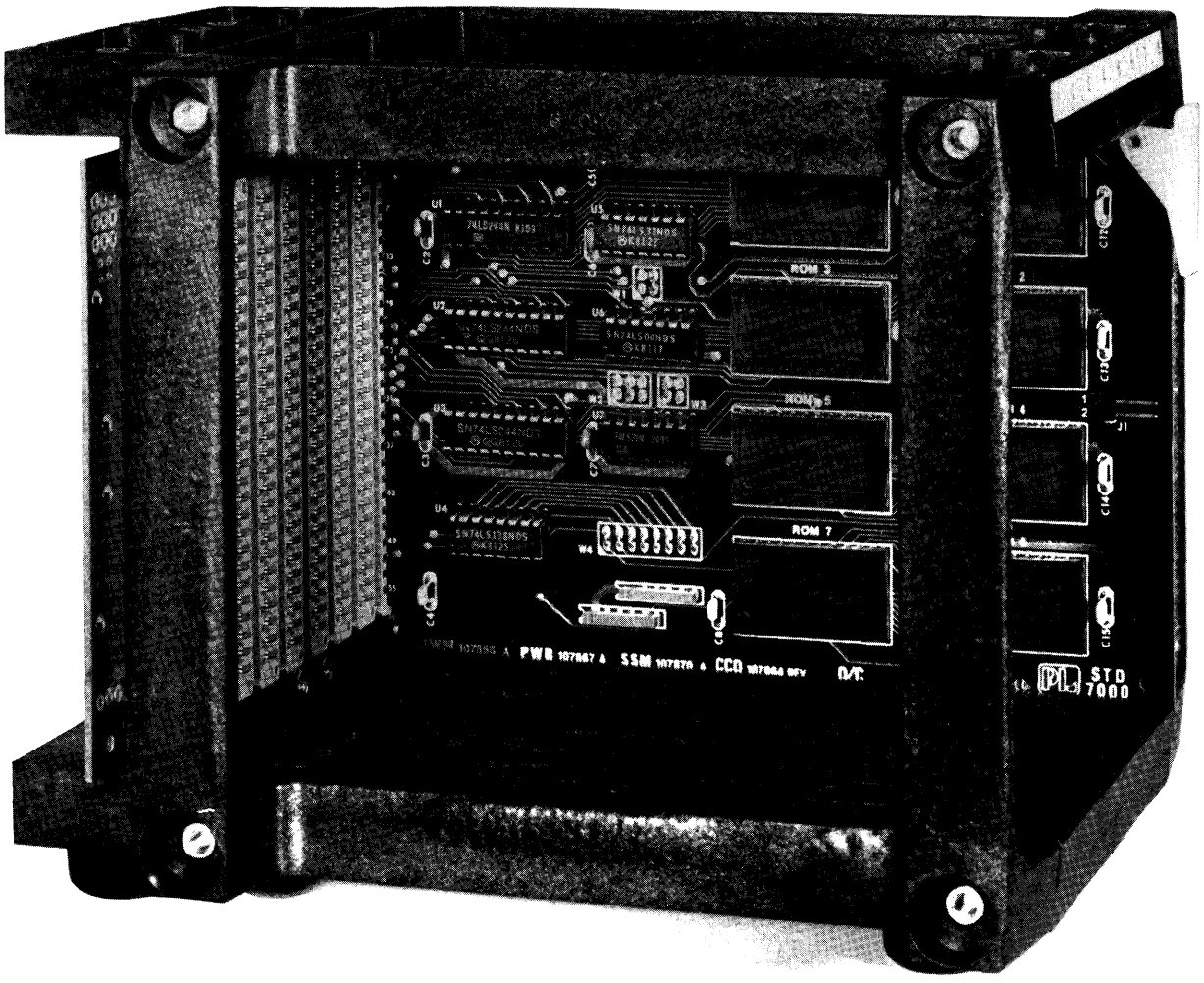


Figure 2-1. Installation of 7705 Card in STD BUS Card Rack.

The 7705 can occupy any slot in the card cage. Install it with the card ejector towards the top of the card rack as shown in Fig. 2-1.

If you use the external segment select line, attach it as shown in Fig. 2-2, using a two-pin 0.1-inch center connector. The twisted pair cable (Pro-Log RC704 or equivalent) consists of one signal line and one ground line for added noise immunity. It can connect the 7705 to an I/O card such as Pro-Log's 7605.

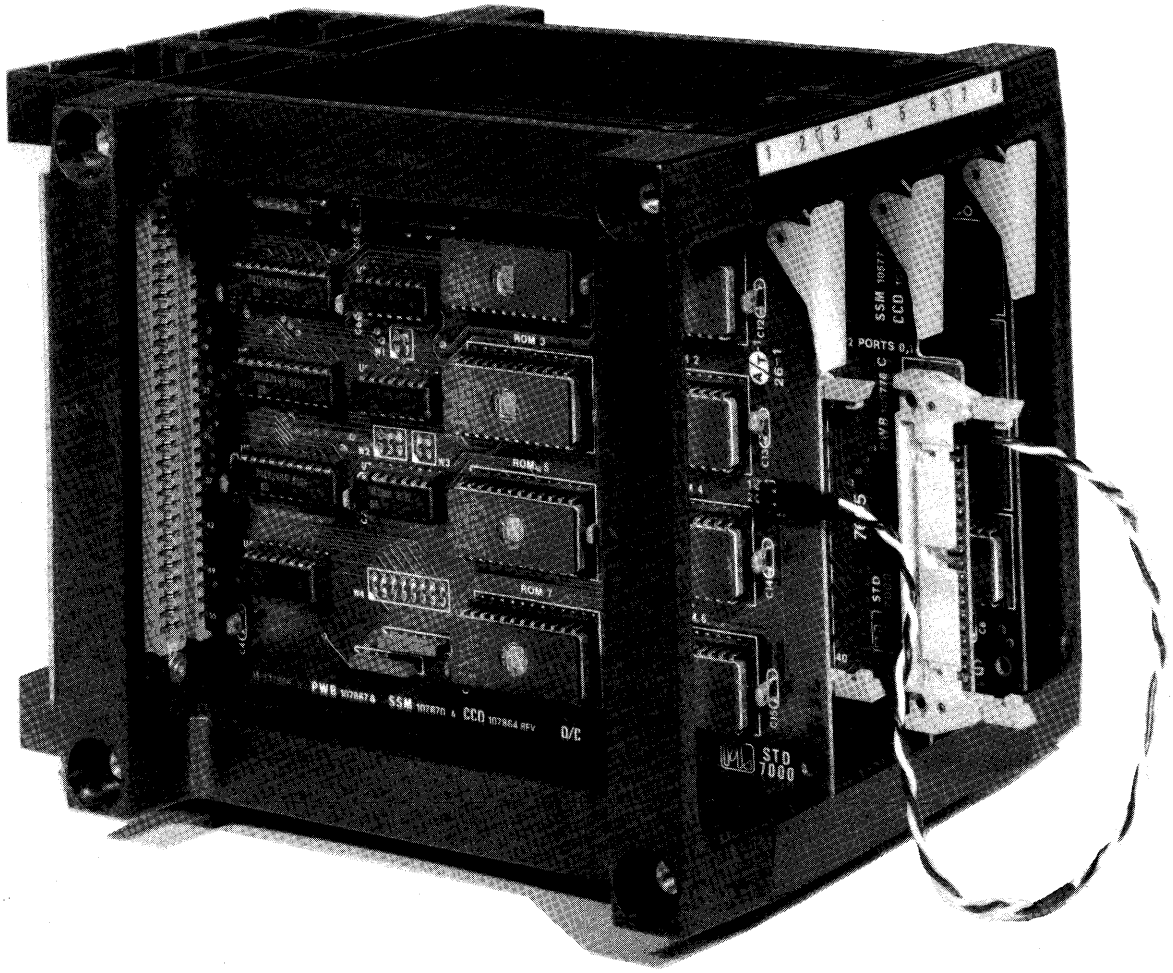


Figure 2-2. Segment Select Connection — 7705 Installation.

Address Mapping

The 7705 card occupies 32K bytes of memory space. It decodes 16 address lines and can reside in either the upper or lower half of a 64K-memory system.

As shipped from the factory, the 7705 occupies memory addresses 8000-FFFF. By way of jumper W1, shown in Fig. 2-3, the card's address mapping can be changed so that it occupies memory addresses 0000-7FFF. If you change it, remove jumper W1 from position 3-4 and replace it with one at position 1-2.

If you use less than the full 32K bytes of memory, disable the unused sockets by removing the proper wire jumpers. Jumper W4, positions 15-16 through 1-2 correspond to sockets 0-7, respectively (Fig. 2-3).

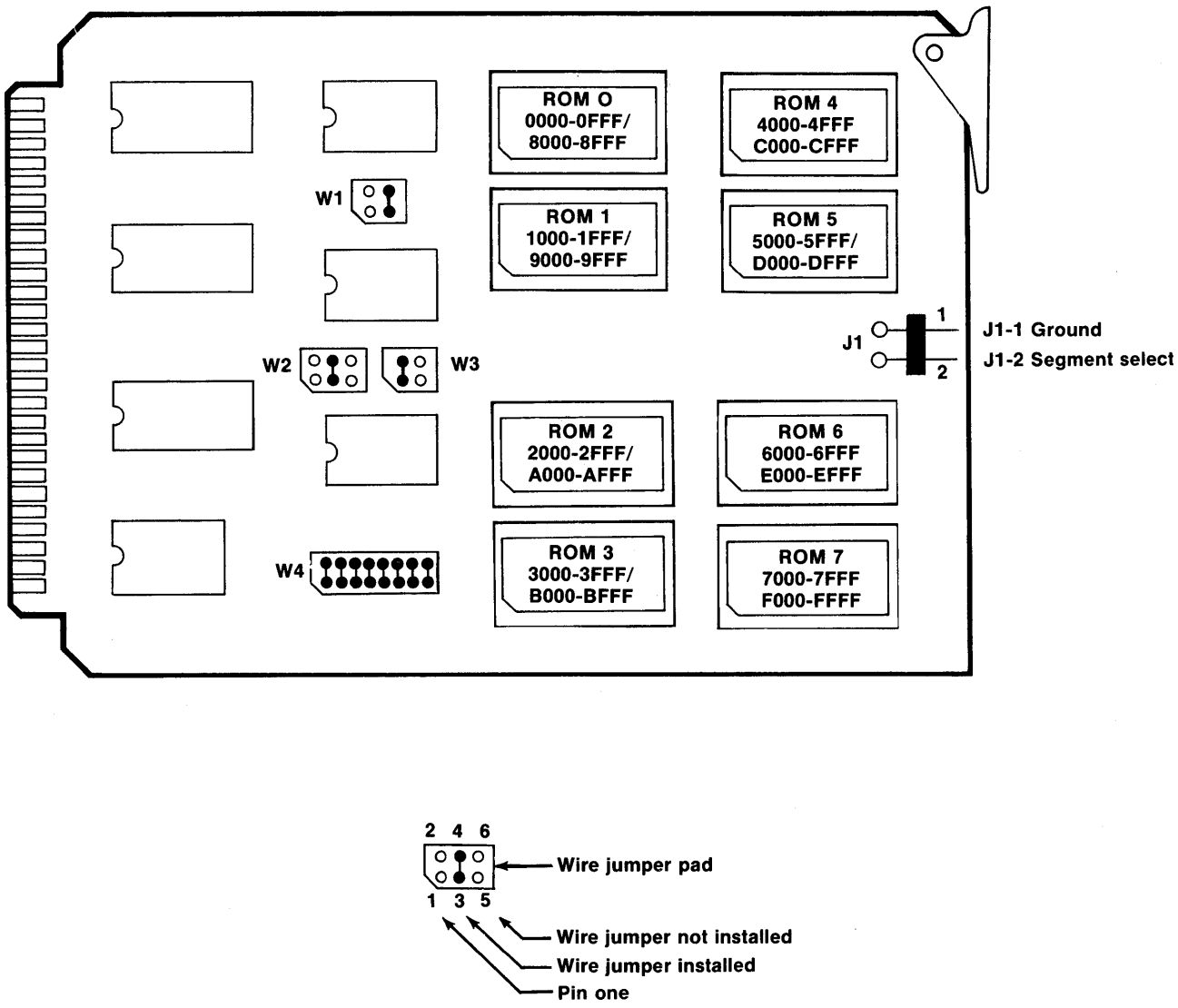


Figure 2-3. Main Components of the 7705

When a socket is disabled, the chip-enable signal is disconnected from the socket. Also, the data-bus buffer no longer responds to memory requests in the address range of the unused socket. This means that memory on other cards in the system can occupy this address space without interference from the 7705 card. For a full description of how this works, see "Chip-Enable Circuit," Section 5.

Any number and combination of sockets may be disabled. By this method, you can configure the 7705 card to occupy as little as 4K of memory space. These 4K blocks can occupy adjacent address fields or they can be widely separated. They can be mapped anywhere within a 64K-memory system on the natural 4K boundaries.

Figure 2-4 shows some of the possible mapping options and how to configure the wire jumpers for each option.

ADDRESS RANGE	JUMPERS INSTALLED										COMMENTS
	W1 POSITION		W4 POSITION								
	1-2	3-4	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	
0000-0FFF	•									•	There are over 500 possible mapping combinations. A few of the most commonly used combinations, and a few examples of how the 7705 can be used in situations requiring extreme flexibility are shown here.
0000-1FFF	•								•	•	
0000-2FFF	•							•	•	•	
0000-3FFF	•						•	•	•	•	
0000-4FFF	•					•	•	•	•	•	
0000-5FFF	•				•	•	•	•	•	•	
0000-6FFF	•			•	•	•	•	•	•	•	
0000-7FFF	•		•	•	•	•	•	•	•	•	
0000-8FFF		•								•	
8000-9FFF		•							•	•	
8000-AFFF		•						•	•	•	
8000-BFFF		•					•	•	•	•	
8000-CFFF		•				•	•	•	•	•	
8000-DFFF		•			•	•	•	•	•	•	
8000-EFFF		•		•	•	•	•	•	•	•	
8000-FFFF		•	•	•	•	•	•	•	•	•	Standard configuration
3000-3FFF	•						•				Example of how minimum 4K can be mapped anywhere.
F000-FFFF		•	•								For 6800 series start-up program or for bootstrap.
0000-0FFF/ 7000-7FFF	•		•							•	Example of noncontinuous memory mapping.

Symbol • means jumper installed.

Figure 2-4. Memory Mapping Options for the 7705.

Jumper Options Affecting MEMEX

The function and operation of the MEMEX line are described in Section 3. This subsection explains the jumper options that affect MEMEX.

As shipped, the 7705 card is enabled when MEMEX is low. To reverse the card's polarity, remove jumper W2 from position 3-4 and replace it with one at position 5-6 (see Fig. 2-3 for the jumper's location). When using two 7705 cards that are both going to occupy the same address field, change the polarity on one of the cards.

Make sure that the MEMEX line is not left floating. The line must be either controlled by some other card in the system, or tied to ground on the 7705 itself. Pro-Log's processor cards either control the MEMEX line or simply tie it to ground. If there is no card in the system controlling MEMEX, or if you want the card to disregard MEMEX, remove jumper W2 from position 3-4 and replace it with one at position 1-2; this will tie the line to ground and permanently enable the card.

Jumper Options Affecting Segment Select

The function and operation of the segment select line are described in Section 3. This subsection explains the jumper options that affect the segment select line.

Segment select is not a part of the STD BUS. It is an external line. When you use it, connect it on the card ejector side of the 7705 (see Fig. 2-2).

Use a two-pin 0.1-inch center connector to attach the line to the 7705. Also, use a twisted pair cable, consisting of one signal line and one ground line for added noise immunity (see Fig. 2-3 for the signal and ground pins).

An I/O card, such as Pro-Log's 7605, along with an RC 704 cable can be used to control the line. One output bit or output line per 7705 card is required. Thus, one output port can control eight 7705 cards.

As shipped, the card is enabled when the segment select line is in the high state. The card's polarity can be reversed by removing jumper W3 from position 1-2 and replacing it with one at position 3-4 (see Fig. 2-3).

With jumper W3 in position 1-2, the segment select line can be left unconnected. A pull-up resistor on the line will hold it in the active condition. However, if jumper W3 is in position 3-4, the line must be controlled in some manner, or the card will remain permanently disabled.

Electrical and Environmental Specifications

See Figs. 2-5 through 2-8 for the 7705's electrical and environmental specifications. Timing diagrams are shown in Figs. 2-9 through 2-13.

Mechanical Specifications

The 7705 card meets all general mechanical specifications of the STD BUS.

Electrical and Environmental Specifications

SYMBOL	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
		MIN	TYP	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.75	5.00	5.25	0	5.50	V
T_A	Free-air temperature	0	+25	+55	-40	+75	°C
R_H	Humidity [1]	5	—	95	0	95	%RH

[1] Noncondensing.

Figure 2-5. Operating Limits of Electrical and Environmental Parameters for 7705 Card.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Icc	Vcc supply current	—	300	600	mA
—	STD BUS input load	See Fig. 2-8		See Fig. 2-8	
—	STD BUS output load	See Fig. 2-8		See Fig. 2-8	

NOTE: Assumes all memory sockets loaded with one selected and seven in standby. For unused 2732A sockets, subtract 150mA maximum selected or 30mA maximum in standby.

Figure 2-6. STD BUS Electrical Specifications Over Recommended Operating Limits for the 7705.

PIN NUMBER			PIN NUMBER		
INPUT (LSTTL DRIVE)				INPUT (LSTTL DRIVE)	
MNEMONIC				MNEMONIC	
SEGMENT[1]	5	2	1	GROUND	

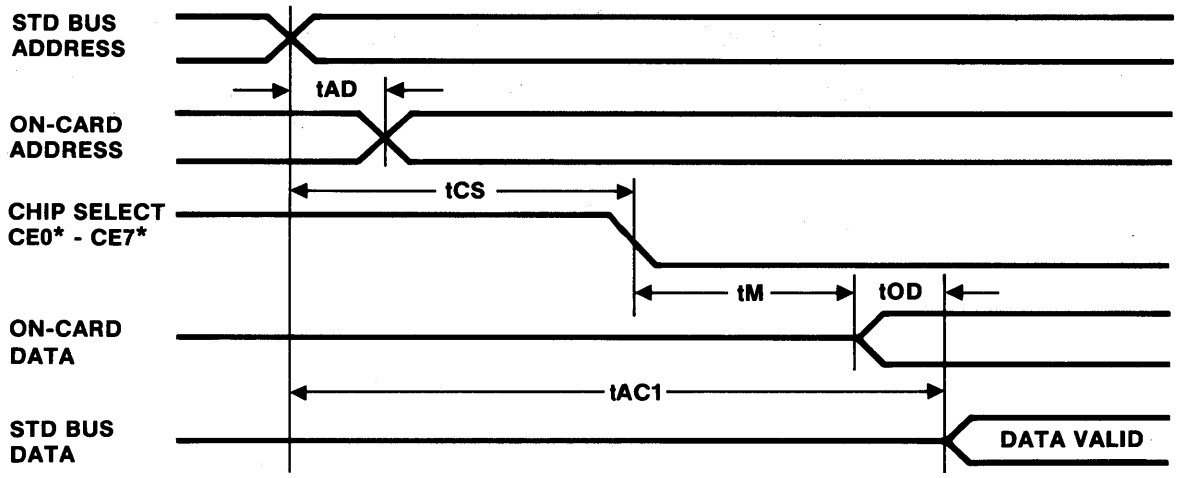
[1] Selectable logic polarity.

Figure 2-7. 7705 Segment Connector Pin List.

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
+5V	Vcc		2	1		Vcc	+5V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7		55	8	7	55		D3
D6		55	10	9	55		D2
D5		55	12	11	55		D1
D4		55	14	13	55		D0
A15	2		16	15		1	A7
A14	1		18	17		1	A6
A13	1		20	19		1	A5
A12	1		22	21		1	A4
A11	1		24	23		1	A3
A10	1		26	25		1	A2
A9	1		28	27		1	A1
A8	1		30	29		1	A0
RD*	1		32	31			WR*
MEMRQ*	1		34	33			IORQ*
MEMEX[1]	1		36	35			IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Active low-level logic
[1] Open-collector driver

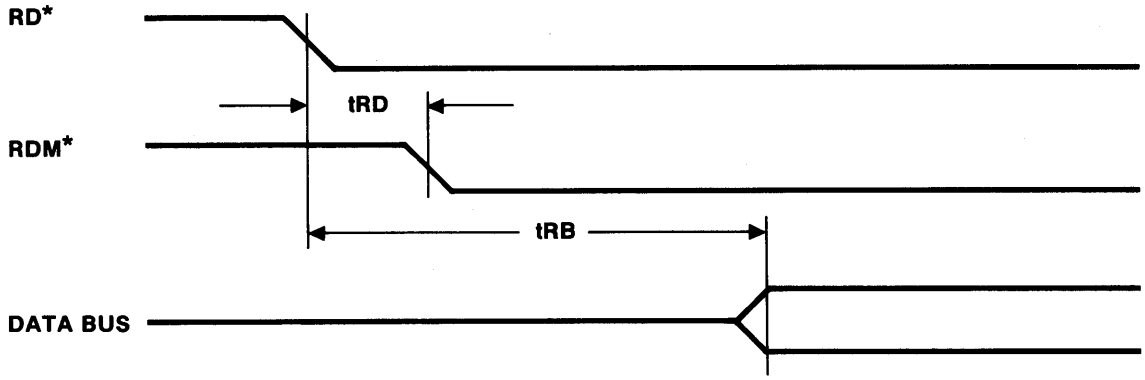
Figure 2-8. 7705 Edge Connector Pin List.



SYMBOL	PARAMETER	MIN	TYP	MAX
tAC1	Minimum safe access time for read	175		
tAD	Address buffer time delay		15	30
tCS	Chip select logic time		35	60
tOD	Data bus buffer time delay		15	30
tM	Data buffer enable time		60	100

All times given in nanoseconds. Above times assume that RD*, MEMRQ*, MEMEX, and SEGMENT* are active before STD BUS address becomes valid.

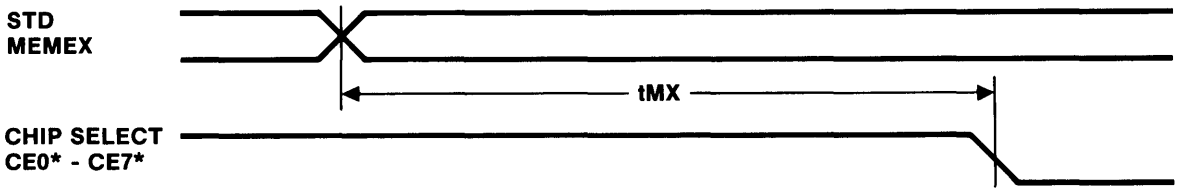
Figure 2-9. 7705 Address Access Timing.



SYMBOL	PARAMETER	TYP	MAX
tRD	Time RD* till RDM*	25	50
tRB	Time RD* till data bus buffer enabled		100

All times given in nanoseconds. RD* can go active up to 115 ns after MEMRQ*, and up to 125 ns after address valid, without affecting access time. If RD* comes later, add the time to the minimum access time of the card. Normally RD* goes true during the memory device access time and, therefore, does not affect access time for the card.

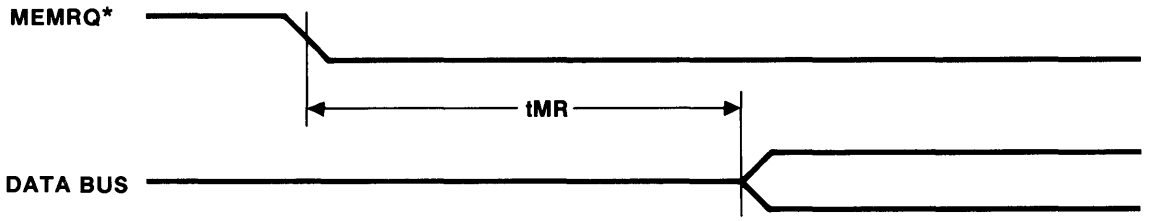
Figure 2-10. 7705 RD* Access Timing.



SYMBOL	PARAMETER	TYP	MAX
tMX	Time MEMEX active to chip select* active	45	75

All times given in nanoseconds. The above parameter is true if all other signals are active before MEMEX goes active.

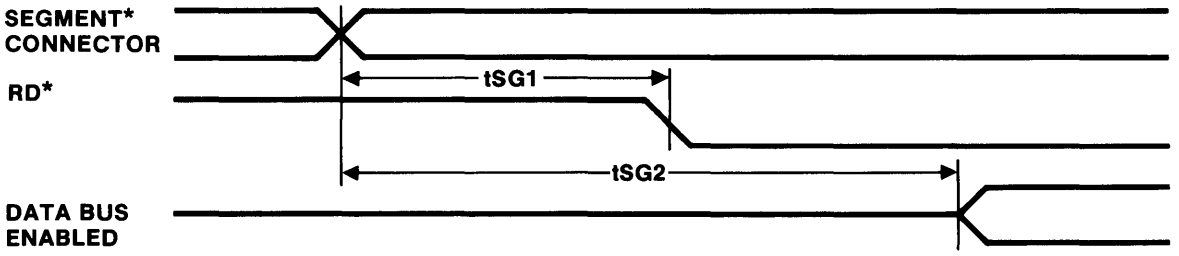
Figure 2-11. 7705 MEMEX Timing.



SYMBOL	PARAMETER	TYP	MAX
tMR	Time MEMRQ* active till data-bus buffer enabled		100

All times given in nanoseconds.

Figure 2-12. 7705 MEMRQ* Timing.



SYMBOL	PARAMETER	TYP	MAX
tSG1	SEGMENT* active to RD*	40	65
tSG2	SEGMENT* active to data bus driver enabled	70	120

All times given in nanoseconds. The above parameters are true if all other signals are active before SEGMENT* goes active.

Figure 2-13. 7705 Segment Timing.

SECTION 3
Operation and Programming

Introduction

This section describes the functions and use of the 7705 card, which is designed to be a versatile part of your memory system.

The 7705 is suitable for both small- and large-scale applications. By using the memory size and mapping options described in Section 2, and the MEMEX and segment select lines described in this section, the 7705 can fill the ROM memory requirements of virtually any system.

MEMEX

The MEMEX line is a part of the STD BUS. It is used as a memory bank select line, allowing two banks of memory to occupy the same address field. Only one of the banks is selected at a time, depending on the logic state of the MEMEX line.

MEMEX is normally controlled by a memory segment controller, or by an output port. The segment controller or output port can be either on the processor card, or on some other card in the system. Some Pro-Log processor cards have an onboard output port for controlling MEMEX.

MEMEX System Memory Example. An example of how MEMEX can be used is shown in Fig. 3-1. It displays a 124K memory system, comprising 4K of RAM and 120K of ROM. The RAM is on the processor card and is permanently enabled, i.e., it ignores MEMEX. The ROM is in two 60K banks. Each bank consists of two 7705 cards. Only two cards are enabled at a time: two on the left when MEMEX is low, and two on the right when MEMEX is high.

At power-up, the MEMEX port is low; therefore, the primary memory bank is enabled. The processor can then choose primary or expanded memory simply by manipulating the MEMEX line.

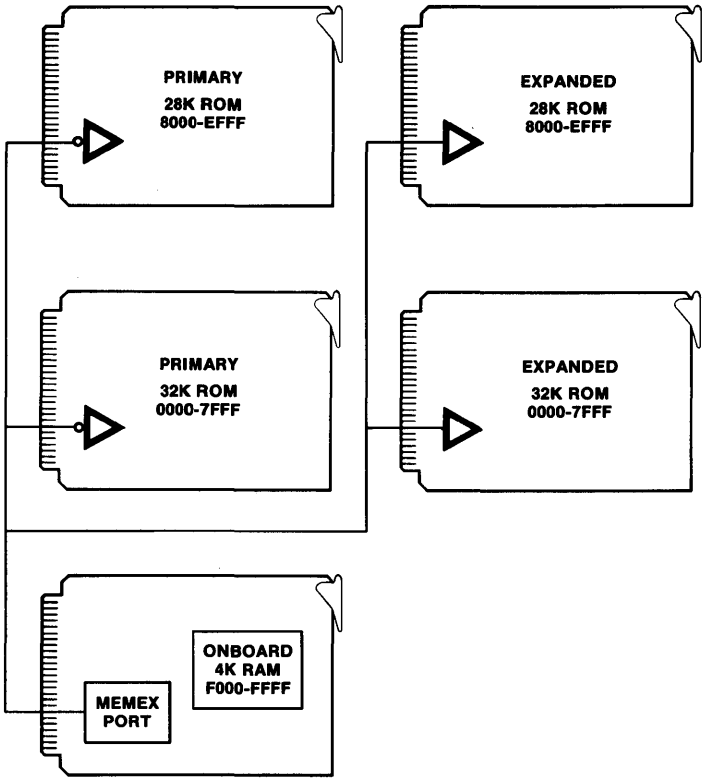


Figure 3-1. MEMEX Example for the 7705, showing 124K Memory System.

MEMEX Control Software. The software for controlling MEMEX requires some special consideration, to prevent problems with the processor when changing memory banks. These problems can be dealt with in a number of ways, as exemplified in this subsection.

Example 1: In many systems that use MEMEX, it will be to your advantage to keep some section of memory permanently enabled, i.e., a section that disregards MEMEX. This may be a section of ROM memory at the low-order addresses, or a section of RAM that stores registers, program variables, and the stack, or a section of ROM that contains interrupt service routines for quick accessibility at all times.

If your system has a permanently enabled section of memory, locate the MEMEX control software in this section. If the section is ROM, the software simply resides in ROM. If the section is RAM, the processor can load the software into RAM. Store the software in ROM, disk, or some other nonvolatile memory. The processor should load the software into RAM as part of the power-up initialization process.

Using the memory system in Fig. 3-1 as a model, a program could be written like the one shown in Fig. 3-2, which depicts two programs: one to jump to a subroutine in expanded memory and one to jump to a subroutine in primary memory. The program assumes that you jump from a main program in one bank to a subroutine in the other bank. The address of the subroutine you are jumping to must be in the H, L register pair. The program selects the proper memory bank and jumps to the subroutine. When the subroutine is exited, the processor returns to the MEMEX control program, which reselects the original bank and then returns to the program from which it came.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE MEMEX SOFTWARE EX. DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
FF	E 0	3E	(TO EXP.)	LDA	I	SET MEMEX HIGH, ENABLES
	1	01		—	01	EXPANDED MEMORY
	2	D3		OPA		
	3	XX		—	XX	← PORT ADDRESS
	4	E5		PSP	H,L	PUSH RETURN ADDRESS (FFEA)
	5	21		LDPI	H,L	ON TO STACK
	6	EA		—		
	7	EF		—		
	8	E3		XCPT	H,L	
	9	E9		JPN	(H,L)	JUMP TO SUBROTINE AT H,L
	A	3E		LDA	I	SET MEMEX LOW ENABLES
	B	00		—	00	PRIMARY MEMORY
	C	D3		OPA		
	D	XX		—	XX	← PORT ADDRESS
	E	C9		RTS		EXIT
	F					
	F 0	3E	(TO PRI.)	LDA	I	SET MEMEX LOW, ENABLES
	1	00		—		PRIMARY MEMORY
	2	D3		OPA		
	3	XX		—		← PORT ADDRESS
	4	E5		PSP	H,L	PUSH RETURN ADDRESS (FFFA)
	5	21		LDPI	H,L	ONTO STACK
	6	FA		—		
	7	EF		—		
	8	E3		XCPT	H,L	
	9	E9		JPN	(HL)	JUMP TO SUBROUTINE AT H,L
	A	3E		LDA	I	SET MEMEX HIGH, ENABLES
	B	01		—		EXPANDED MEMDRY
	C	D3		OPA		
	D	XX		—		← PORT ADDRESS
	E	C9		RTS		EXIT
	F					

PERMANENT MEMORY

100001 2/77

Figure 3-2. Example 1 of MEMEX Software for the 7705.

Example 2: In the first example, it was assumed that when the program jumped from one bank to the other, it jumped to a subroutine. Example 2 depicts a program that jumps from one bank to the other, but not to a subroutine.

Instead, the program simply changes the state of the MEMEX line and then jumps to the address in the H, L register pair. Again the program is divided up into two sections: one that goes from primary to expanded memory, and one that goes from expanded to primary memory.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE MEMEX SOFTWARE EX. 2 DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
FF	F 0	3E	TO EXP.	LDA	I	PERMANENT MEMORY: SET MEMEX HIGH, SELECTS EXPANDED MEMORY
	1	01		—		1
	2	D3		OPA		← PORT ADDRESS
	3	XX		—		
	4	F9		JPN	(H,L)	↓ JUMP TO ADDRESS IN H,L PAIR
	5					
	6					
	7					
	8					
	9	3E	TOPRI.	LDA	I	SET MEMEX LOW, SELECTS PRIMARY MEMORY
	A	00		—		
	B	D3		OPA		
	C	XX		—		← PORT ADDRESS
	D	E9		JPN	(H,L)	↓ JUMP TO ADDRESS IN H,L PAIR
	E					
	F					
	0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

100001 2/77

Figure 3-3. Example 2 of MEMEX Software for the 7705.

Example 3: So far, we have looked at MEMEX control software residing in a section of memory that is permanently enabled. Figs. 3-4 and 3-5 show how the control software can reside in memory that is affected by MEMEX.

Fig. 3-4 depicts a program that jumps from a program in primary memory to a subroutine in expanded memory. Note that both sections of the program reside at the same addresses. However, one part is in primary memory and one part is in expanded memory.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE MEMEX SOFTWARE EX. 3 DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS	
EF	F 0	3E		LDA	I	JUMP TO EXPANDED MEMORY	PRIMARY MEMORY
	1	01		←			
	2	D3		OPA			
	3	XX		—		← PORT ADDRESS	
	4	00		NOP		UNUSED	
	5	00		NOP			
	6	00		NOP			
	7	00		NOP			
	8	00		NOP			
	9	00		NOP			
	A	00		NOP			
	B	00		NOP			
	C	00		NOP			
	D	00		NOP			
	E	C9		RTS		EXIT	
	F						
EF	F0	00		NOP		UNUSED	EXPANDED MEMORY
	1	00		NOP			
	2	00		NOP			
	3	00		NOP			
	4	E5		PSP	H,L	PUSH RETURN ADDRESS (EFFA)	
	5	21		LDPI	H,L	ONTO STACK	
	6	FA		—			
	7	EF		—			
	8	E3		XCPT	H,L		
	9	E9		JPN	(H,L)	JUMP TO SUBROUTINE AT H,L	
	A	3E		LDA	I	JUMP TO PRIMARY MEMORY	
	B	00		—	00		
	C	D3		OPA			
	D	XX		—		← PORT ADDRESS	
	E	00		NOP		UNUSED	
	F						

100001 2/77

Figure 3-4. Example 3 of MEMEX Software for the 7705.

Fig. 3-5 shows how the program looks to the processor. When it runs, it becomes one coherent program.

Note that this example program only jumps from primary memory to a subroutine in expanded memory and then returns. In normal operations you would probably also want one to do the opposite.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE RUNNING EX.3 DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
EF	F0	3E		LDA	I	PRI.MEM — JUMP TO EXPANDED MEMORY
	1	01		—		
	2	D3		DPA		
	3	XX		—		← PORT ADDRESS
	4	E5		PSP	HL	EXP. MEM — PUSH RETURN ADDRESS (EFFA)
	5	21		LDPI	HL	ONTO STACK
	6	FA		—		
	7	EF		—		
	8	E3		XCPT	HL	
	9	E9		JPN	HL	JUMP TO SUBROUTINE AT H,L
	A	3E		LDA	I	JUMP TO PRIMARY MEMORY
	B	00		—	00	
	C	D3		OPA		
	D	XX		—		← PORT ADDRESS
	E	C9		RTS		PRI.MEM — EXIT
	F					
	0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

100001 2/77

Figure 3-5. Running Example 3 Software for the 7705.

To use the example program, the processor must be running primary memory. When you want to jump to a subroutine in expanded memory, load the address of the subroutine into the H,L register pair. Then perform a jump-to-subroutine to the MEMEX control program. The program directs the processor to change memory banks and jumps to your subroutine. After running the subroutine, the processor returns to your original program.

Example 4: This example (Fig. 3-6) is similar to the last example. However, rather than jumping from one bank to another as a subroutine, example 4 program performs a simple jump.

The program is in two sections: one that goes from primary to expanded memory and one that goes from expanded to primary memory.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE MEMEX SOFTWARE EX. 4 DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
EF	F0	3E	TO EXP.	LDA	I	PRIMARY MEMORY — JUMP TO EXPANDED MEMORY
	1	01		—	01	
	2	D3		OPA		
	3	XX		—		← PORT ADDRESS
	4	00		NOP		UNUSED
	5					
	6					
	7					
	8	00	TO PRI.	NOP		
	9	00		NOP		UNUSED
	A	00		NOP		
	B	00		NOP		
	C	E9		JPN	HL	
	D					JUMP TO ADDRESS IN H,L
	E					
	F					
EF	F0	00	TO EXP.	NOP		EXPANDED MEMORY — UNUSED
	1	00		NOP		
	2	00		NOP		
	3	00		NOP		
	4	E9		JPN	HL	JUMP TO ADDRESS IN H,L
	5					
	6					
	7					
	8	3E	TO PRI.	LDA	I	JUMP TO PRIMARY MEMORY
	9	00		—	00	
	A	D3		OPA		
	B	XX		—		← PORT ADDRESS
	C	00		NOP		UNUSED
	D					
	E					
	F					

100001 2/77

Figure 3-6. Example 4 of MEMEX Software for the 7705.

Figure 3-7 shows how the program looks to the processor.

To use example 4, load the address of the program you want to jump to into the H,L register pair. Then, jump to the MEMEX control program. The processor is directed to change memory banks and to jump to the program you requested.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE RUNNING EX.4 DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
EF	F 0	3E	TO EXP.	LDA	I	PRI. MEM — JUMP TO EXPANDED MEMORY
	1	01		—	01	
	2	D3		OPA		
	3	XX		—		← PORT ADDRESS
	4	E9		JPN	H,L	JUMP TO ADDRESS IN H,L
	5					EXP. MEM
	6					
	7					
	8	3E	TO PRI.	LDA	I	JUMP TO PRIMARY MEMORY
	9	00		—	00	
	A	D3		OPA		
	B	XX		—		← PORT ADDRESS
	C	E9		JPN	H,L	JUMP TO ADDRESS IN H,L
	D					PRI. MEM
	E					
	F					
	0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

100001 2/77

Figure 3-7. Running Example 4 Software for the 7705.

MEMEX Interrupt Control Software. This last example shows how interrupt service can be handled in a system using MEMEX. One method, previously mentioned, is to set aside an area of memory for interrupt service. This area would be permanently enabled.

A second method, if the interrupt service routines are short enough, is to use identical service routines in both primary and expanded memory. Both routines reside at the same addresses. However, this method uses up too much memory space.

A third method, shown in Figs. 3-8, 3-9, and 3-10, allows the service routines to reside in only one bank of memory. In the example shown, they reside in primary memory.

The function of the program is to coordinate the jumping to, and returning from, the interrupt routine. The program ensures that the processor accesses the service routine. If the processor is in expanded memory, the program directs the processor to switch to primary memory. The program also ensures that the processor returns to the correct bank, after the interrupt is serviced.

The interrupt routine resides at address 0024. This is the address an 8085 processor jumps to when it receives a nonmaskable interrupt.

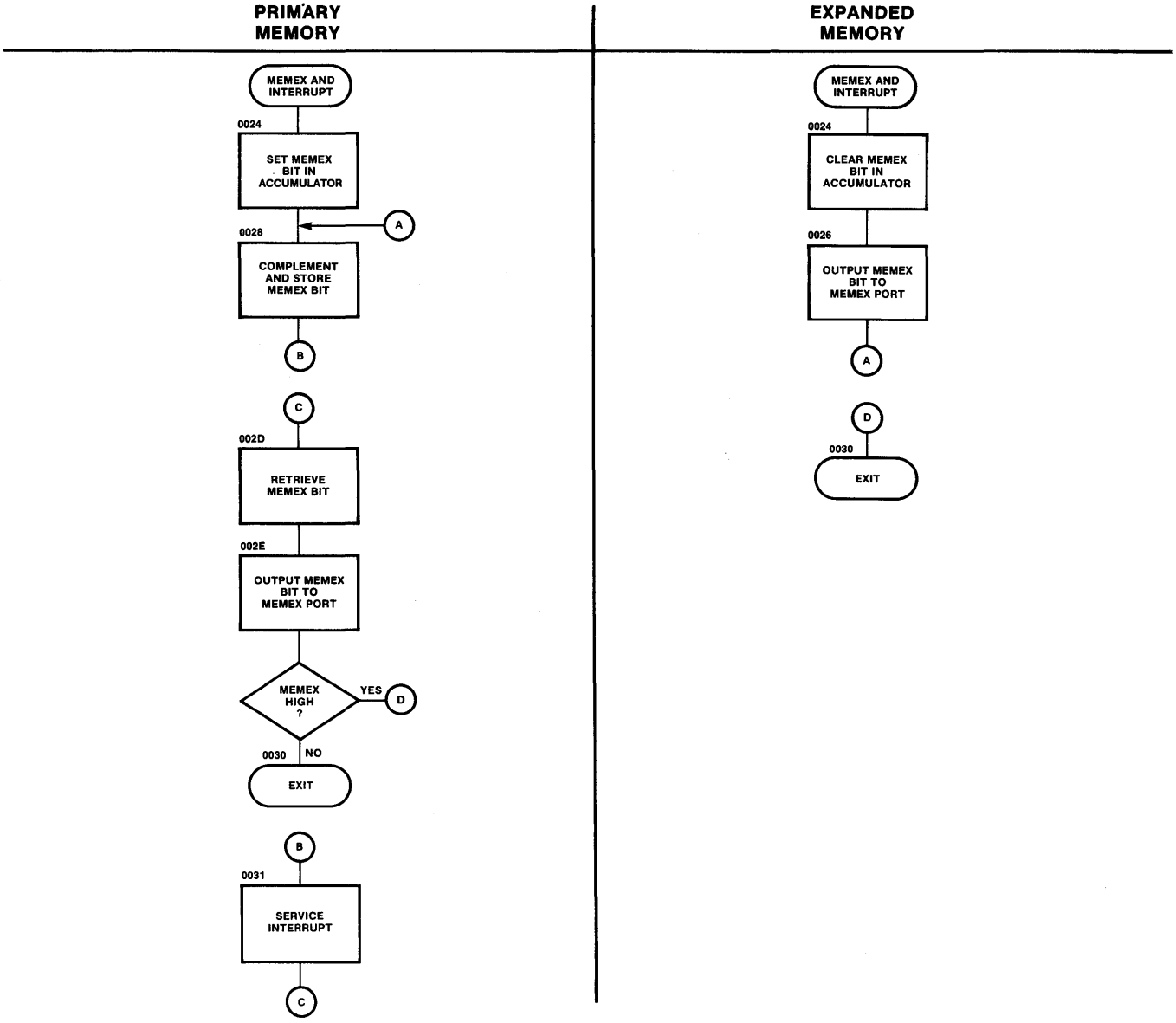


Figure 3-8. Flowchart — MEMEX Interrupt Control Software.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE MEMEX + INTER — DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
00	20					PRIMARY MEMORY
	1					
	2					
	3					
	24	3E	(MEMEX + INTER.)	LDA	I	SET MEMEX BIT IN ACCUMULATOR
	5	01		—	01	
	6	00		NOP		
	7	00		NOP		
	8	2F		CMA		COMPLEMENT AND STORE
	9	F5		PSP	AF	MEMEX BIT
	A	C3		JP	UN	SKIP OVER "EXIT" TO "INTER"
	B	31		—		
	C	00		—	INTER	
	D	F1	EXIT	PLP	AF	RETRIEVE AND OUTPUT MEMEX BIT
	E	D3		OPA		
	F	XX		—		← PORT ADDRESS
	30	C9		RTS		EXIT (PRIMARY MEMORY)
	1	XX	INTER			INTERRUPT SERVICE
	2	XX				
	3	XX				
	4	XX				
	5	XX				
	6	XX				
	7	XX				
	8	XX				
	9	XX				
	A	XX				
	B	XX				
	C	XX				
	D	C3		JP	UN	GO EXIT
	E	2D		—		
	F	00		—	EXIT	

100001 2/77

Figure 3-9. Example of MEMEX Interrupt Software, Primary Memory, for the 7705.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE MEMEX + INTER — DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
00	20					EXPANDED MEMORY
	1					
	2					
	3					
	24	3E	(NEMEX + INTER)	LDA	I	CLEAR AND OUTPUT MEMEX BIT,
	5	00		—	00	SELECTS PRIMARY MEMORY
	6	D3		OPA		
	7	XX		—		← PORT ADDRESS
	8	00		NOP		UNUSED
	9	00		NOP		
	A	00		NOP		
	B	00		NOP		
	C	00		NOP		
	D	00		NOP		
	E	00		NOP		
	F	00		NOP		
	30	C9		RTS		EXIT (EXPANDED MEMORY)
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

100001 2/77

Figure 3-10. Example of MEMEX Interrupt Software, Expanded Memory, for the 7705.

Follow the flowchart in Fig. 3-8 and assume that the processor is in expanded memory when it is interrupted. The program then directs the processor to select primary memory, by clearing the MEMEX bit in the accumulator and writing it out to the MEMEX port. In primary memory, the processor complements and stores the MEMEX bit. After the interrupt is serviced, the MEMEX bit is retrieved. When the bit is output to the MEMEX port, the processor is first returned to expanded memory and then to the program from which it was interrupted.

If the processor is in primary memory when it is interrupted, it sets the MEMEX bit in the accumulator to a one. The one is then complemented and stored. After the interrupt is serviced, the MEMEX bit is retrieved and is output to the MEMEX port; this has no effect, however, since the MEMEX line is already low. The processor simply continues in primary memory. It then returns to the program from which it was interrupted.

Figures 3-9 and 3-10 show how this program can be written. The program in Fig. 3-9 resides in primary memory and the program in Fig. 3-10 resides in expanded memory. This program should reside at each address where an interrupt service routine is located.

Segment Select

The segment select line is not a part of the STD BUS. It is an external line that must be connected on the card ejector side of the 7705 when it is used. Fig. 2-2 shows the location of the connector. The purpose of the line is to allow the 7705 card to participate in large-scale memory bank select schemes, in which multiple cards occupy the same address field.

Whereas the MEMEX line can be used to select one of two banks of memory, the segment select line can choose one of any number of memory banks.

The line is normally controlled by a memory segment controller or by output ports. An I/O card (e.g., Pro-Log's 7605) along with an RC704 cable can be used to control the line. One output port can control eight cards.

Example 1: Figure 3-11 exemplifies how you can use the segment select line. It shows a 128K memory system with 32K of RAM and 96K of ROM. The 32K RAM is on two cards that are permanently enabled. The 96K ROM is on three cards. Each card has its segment select line connected to a bit of an output port on an I/O card. All three cards occupy the same address field.

At power-up, the output port bits are low. One of the 7705 cards configured for low-level active segment select. The other two are high-level active. Therefore, one of the cards is automatically selected at power-up. Thereafter, the processor chooses which card it wants simply by writing to the output port.

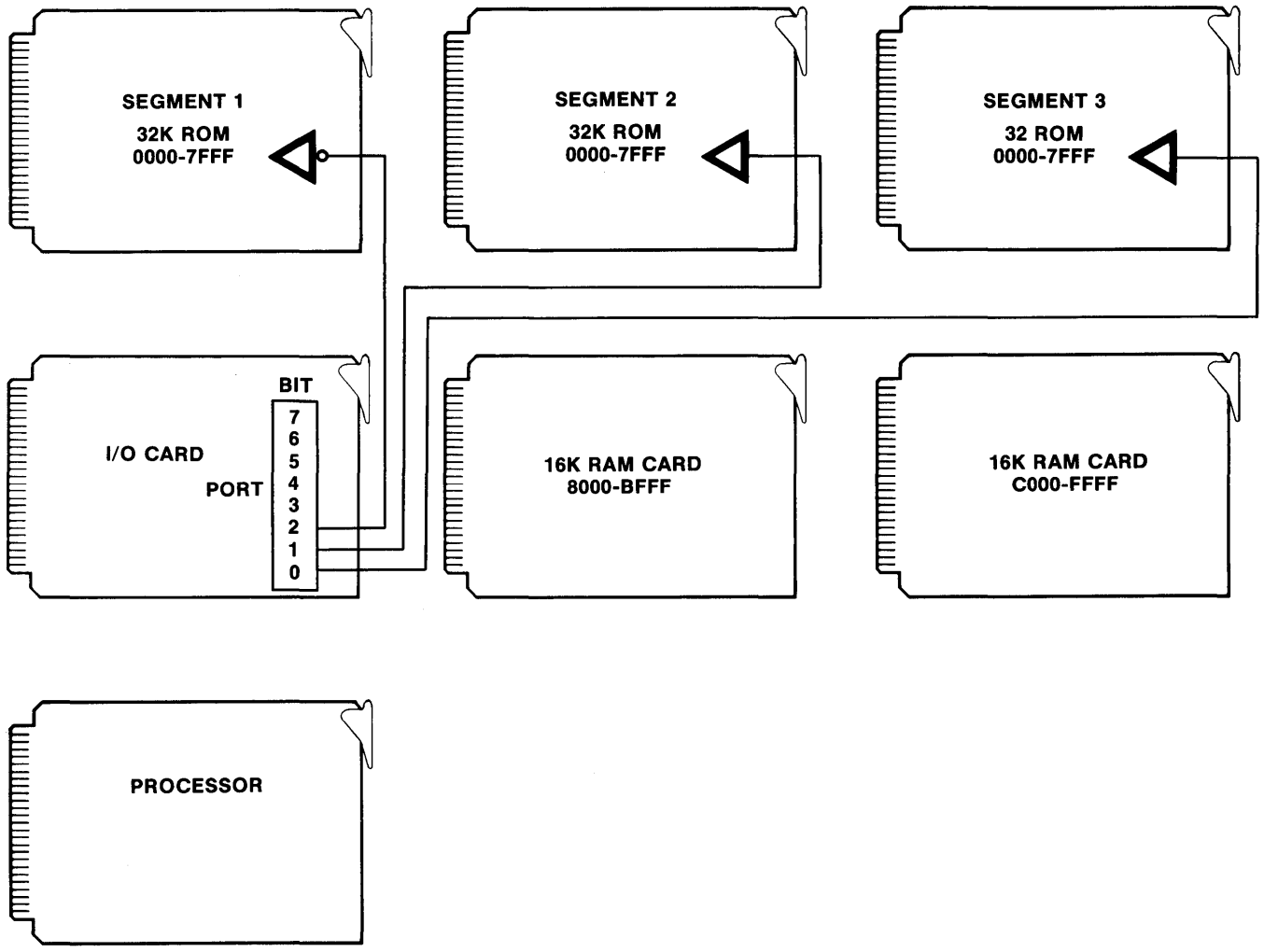


Figure 3-11. Example 1 of Segment Select for the 7705.

Example 2: This example is shown in Fig. 3-12. In this case, two cards are connected to each output line being used. On the processor card, 4K of RAM is permanently enabled. The 180K of ROM is in three banks. Each bank consists of two cards.

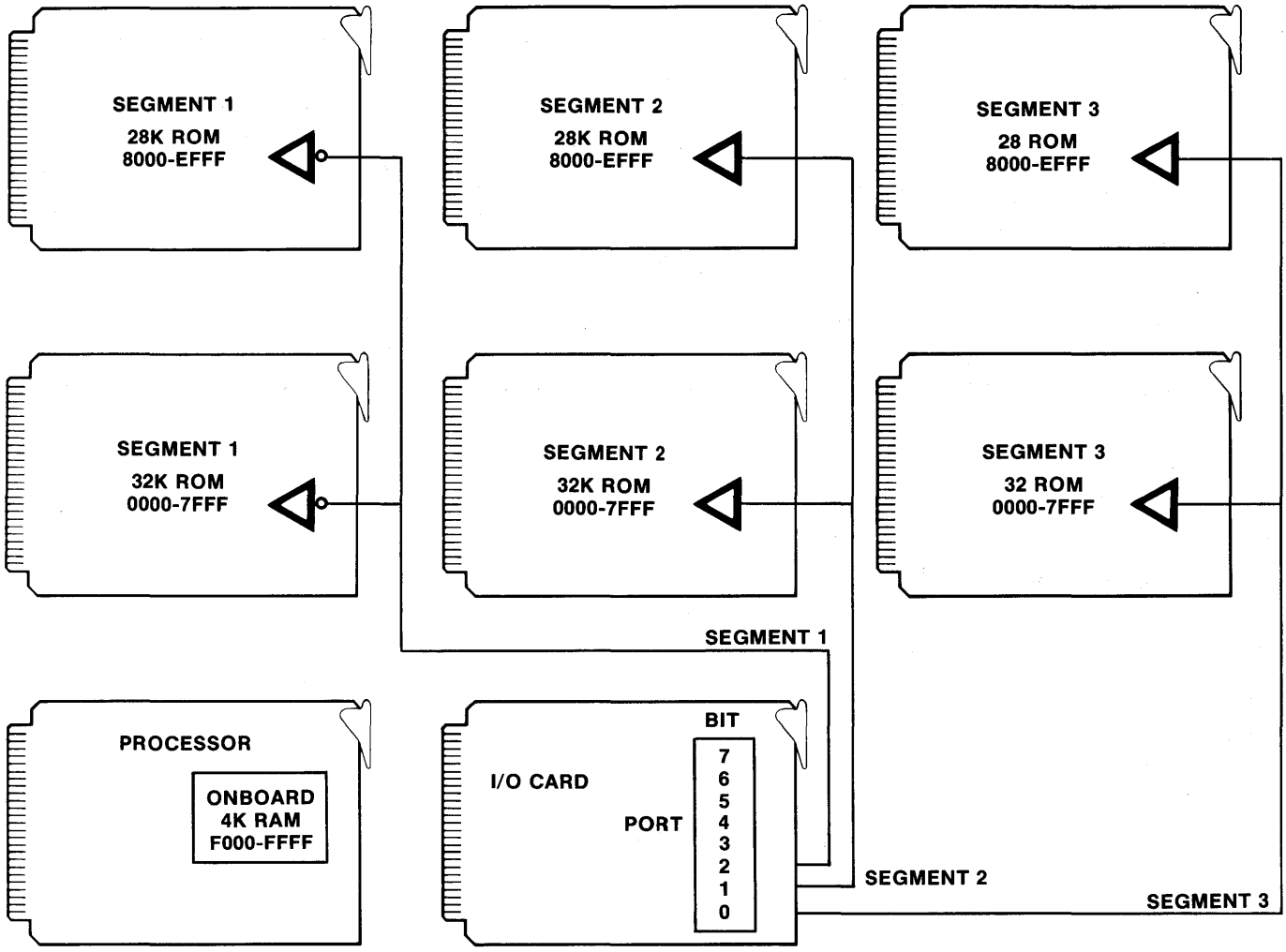


Figure 3-12. Example 2 of Segment Select for the 7705, Showing 184K Memory System.

Example 3: This example combines MEMEX and segment select. Normally, MEMEX should be used, since it requires no additional lines. But if segment select is used, MEMEX should probably not be used. However, they can be used together.

Figure 3-13 exemplifies a 160K combined MEMEX and segment select system. The system has 32K of RAM, permanently enabled. The rest, 128K of ROM, is in four banks.

The processor card is a Pro-Log 7804. It has one output line, used here for segment select, which is connected to all four ROM cards. The two marked "Segment 1" are enabled when segment select is low. The two marked "Segment 2" are enabled when segment select is high.

Of the two cards marked "Segment 1," one card is enabled when MEMEX is low, and one card is enabled when MEMEX is high. The same is true for the cards marked "Segment 2."

The processor selects one segment, or pair, of cards by setting the segment select line high or low. It then selects which of the cards in the pair is enabled, by setting the MEMEX line high or low.

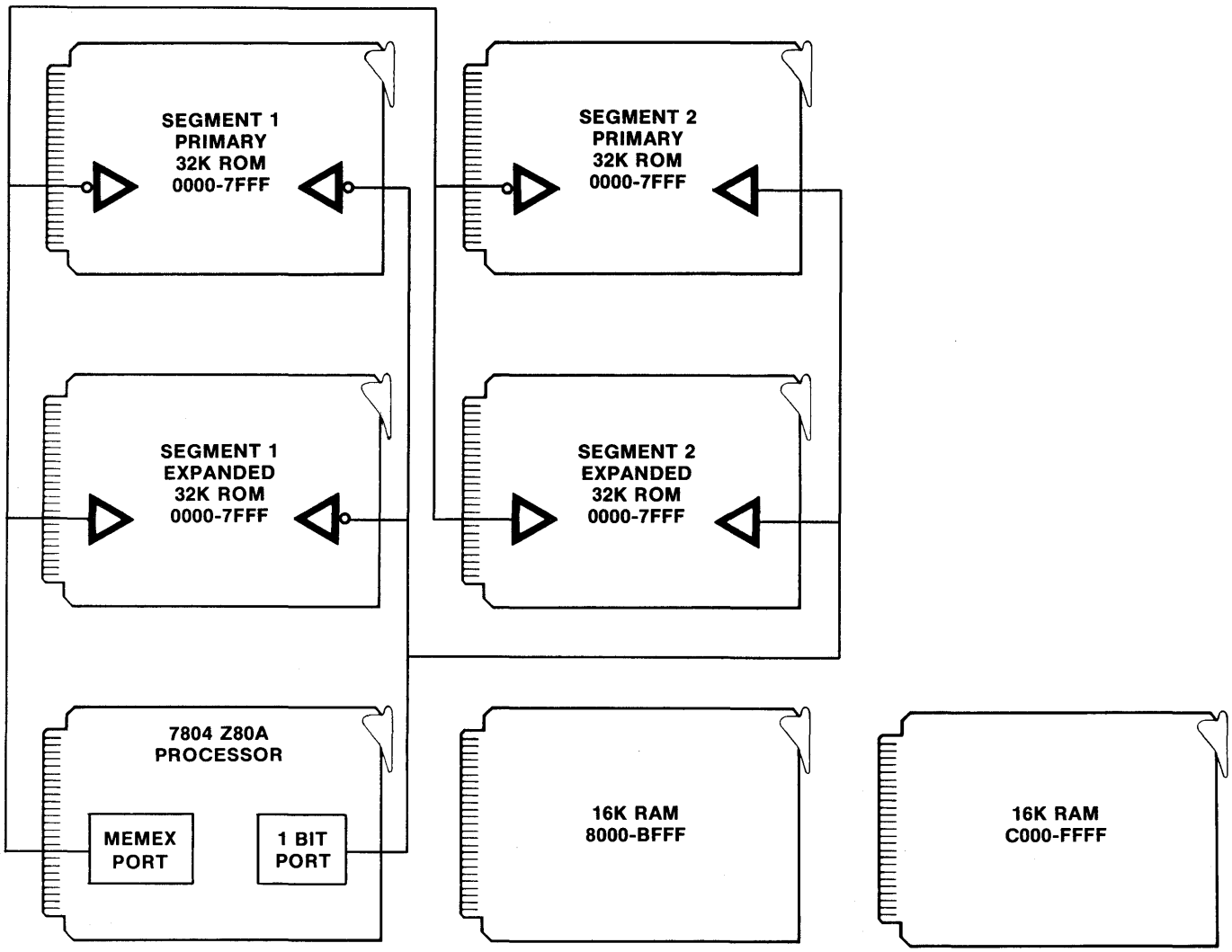


Figure 3-13. Example 3: MEMEX and Segment Select Combination for the 7705, Showing 160K Memory System.

Segment Select Control Software The control software for segment select is similar to that used for MEMEX. However, it differs in that it must be able to control more than two segments, i.e., the program must be told what segment to jump to; also, it must be told what segment to return to.

As with MEMEX, many applications require an area of permanent memory. The simplest software can reside in this area (see Fig. 3-14 for an example).

The segment select control software is similar to the program in MEMEX software "Example 1." It coordinates jumping from one segment to a subroutine in another segment. The difference here is that you must enter the program with two additional variables. Register A must have the number of the segment you are jumping to. Register B must have the number of the segment you are jumping from.

The "number" of the segment is one of the following: 01, 02, 04, 08, 10, 20, 40, or 80 hexadecimal, one bit for each segment; therefore, this program can control up to eight segments.

You can adapt any of the MEMEX control software examples for segment select control, or you can write entirely different control software.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE SEGMENT CONTROL DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS	
FF	F0	D3		OPA		SWITCH TO DESIRED SEGMENT	PERMANENT MEMORY
	1	XX		—		← PORT ADDRESS	
	2	C5		PSP	BC	SAVE ORIGINAL SEGMENT NUMBER	
	3	E5		PSP	H,L	PUSH RETURN ADDRESS ON (FFF9)	
	4	21		LDPI	H,L	TOP OF STACK	
	5	F9		—			
	6	FF		—			
	7	E3		XCPT	H,L		
	8	E9		JPN	H,L	JUMP TO SUBROUTINE AT H,L	
FF	F9	C1		PLP	B,C	RETURN TO ORIGINAL SEGMENT	
	A	78		LDA	B		
	B	D3		OPA			
	C	XX		—		← PORT ADDRESS	
	D	C9		RTS		EXIT	
	E						
	F						
	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
	8						
	9						
	A						
	B						
	C						
	D						
	E						
	F						

100001 2/77

Figure 3-14. Example 1 of Segment Control Software for the 7705.

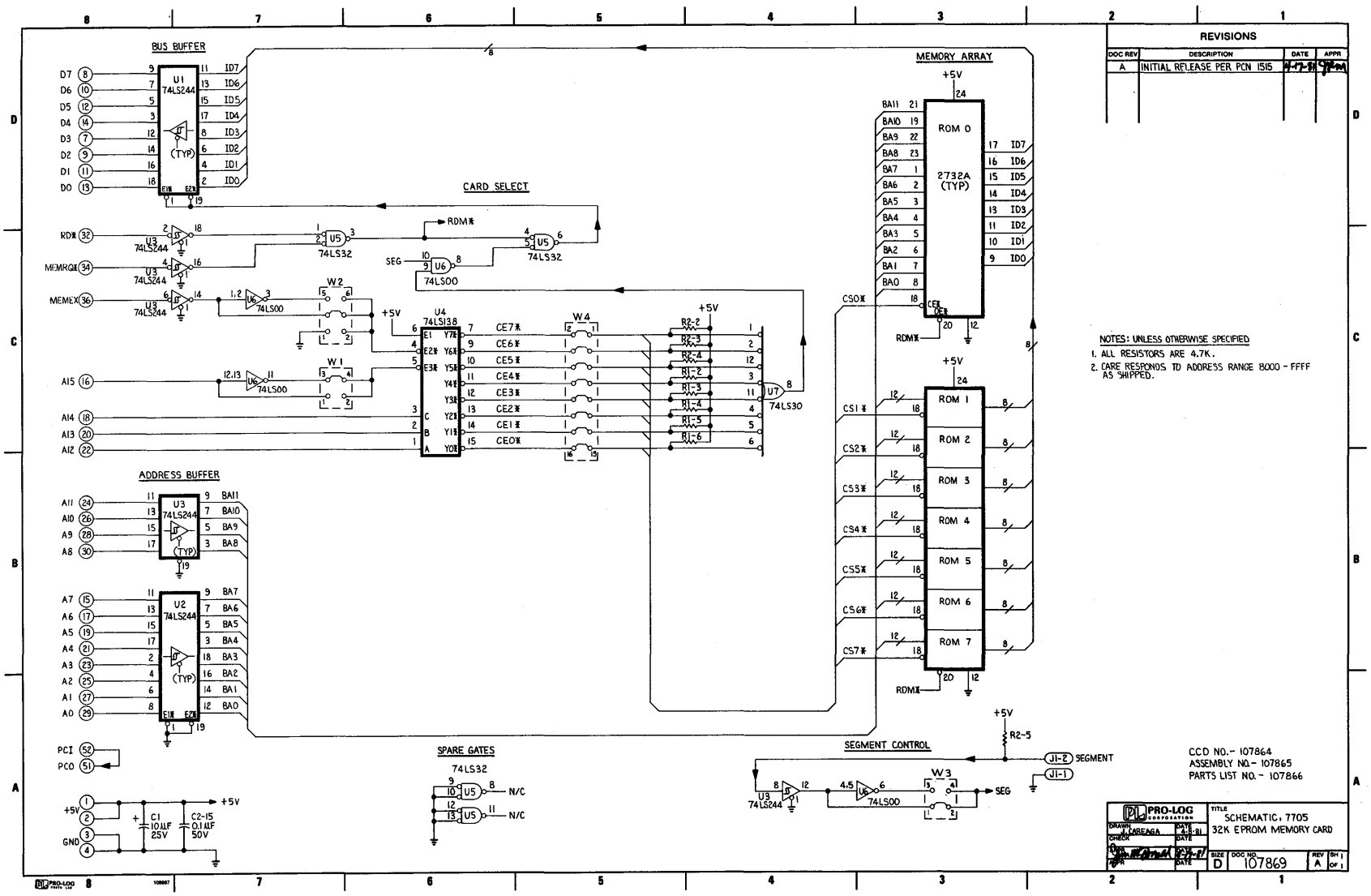
SECTION 4
Operating Software

This section is usually reserved for operating software. However, the 7705 card requires no software except for those examples given in Section 3.

SECTION 5
Maintenance

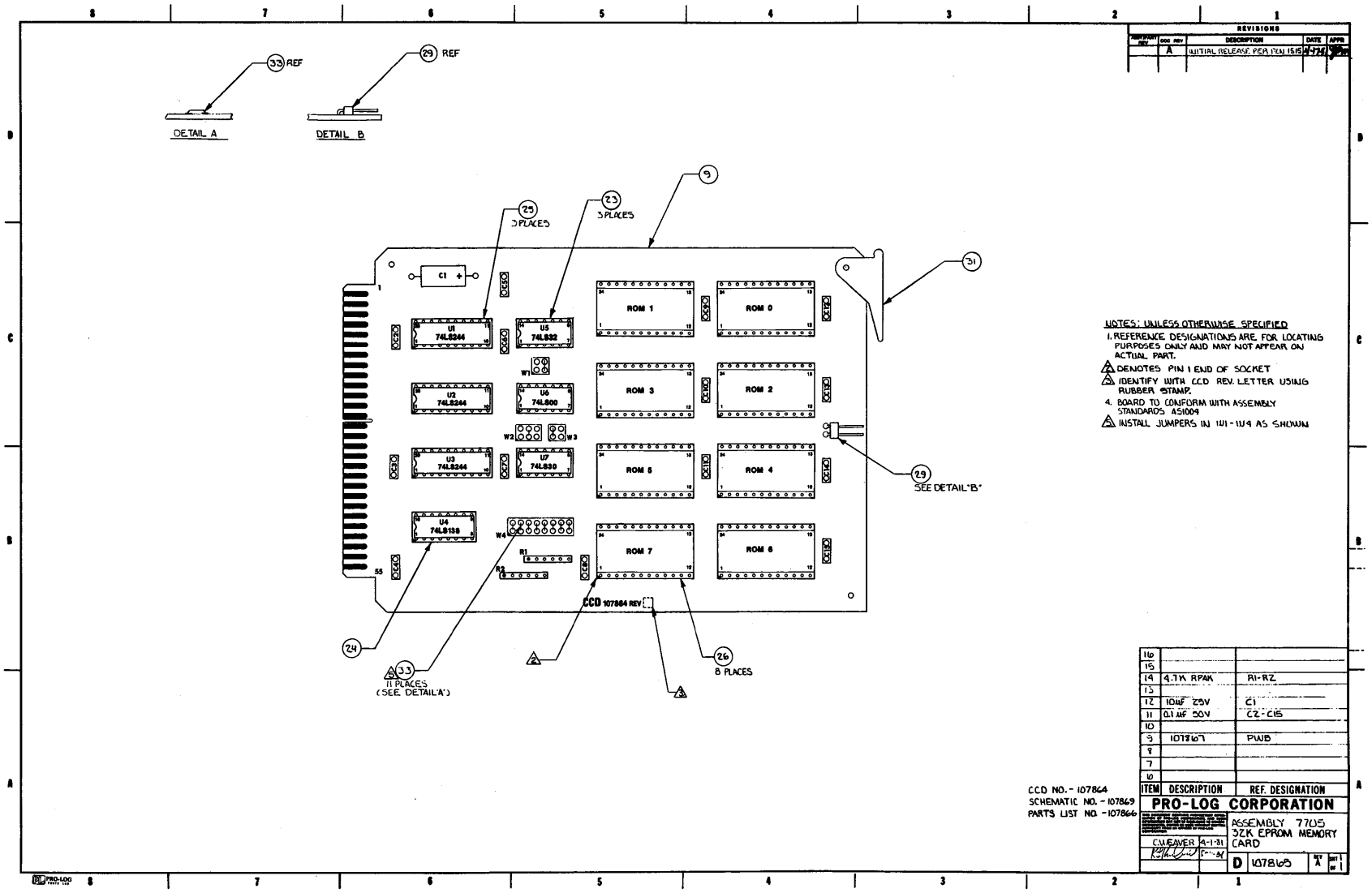
Reference Drawings

The schematic (Fig. 5-1) and assembly drawing (Fig. 5-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. They may differ in some respects from the card and documentation that the user received from Pro-Log. The schematic and assembly drawings shipped by Pro-Log with the card are those from which the card was manufactured.



REFERENCE ONLY

Figure 5-1. Schematic for the 7705 (Reference Only).



REFERENCE ONLY

Figure 5-2. Assembly for the 7705.

Address Decoding Circuit

Address lines A0-A7 go through buffer U2 and address lines A8-A11 go through buffer U3. They then go directly to the EPROM sockets (see Fig. 5-3).

Address lines A12-A15 are decoded by U4 along with the MEMEX line. Address line A15 is inverted by U6 and then connects to U4 through jumper W1, position 3-4. This maps the card to addresses 8000-FFFF. To remap the card to addresses 0000-7FFF, remove jumper W1 from position 3-4 and replace it with one at position 1-2; this bypasses the inverter and connects A15 directly to U4.

The MEMEX input to U4 is low-level active. If the input is tied to ground (by placing a jumper at the W2 position 1-2), the card is permanently enabled and ignores MEMEX.

If MEMEX is controlled externally, the incoming signal can be either high-level active or low-level active. After being buffered by U3, the line can be either inverted by U6, or it can bypass the inverter. With jumper W2 in position 5-6 , the line is high-level active. With jumper W2 in position 3-4 , as it is when the card is shipped, the line is low-level active.

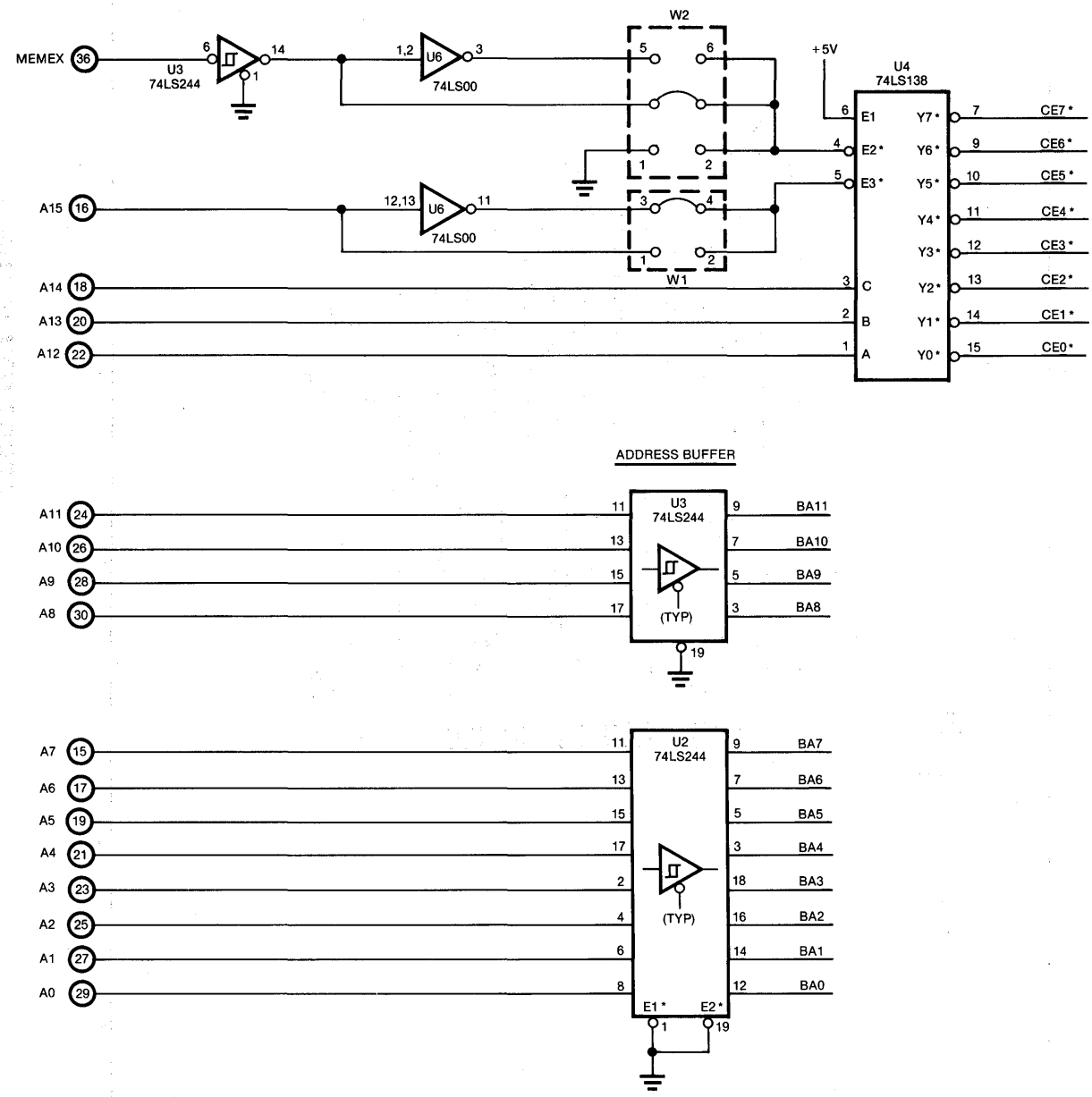


Figure 5-3. Address Decoding Circuit for the 7705.

Chip-Enable Circuit

The chip-enable signals CEO*-CE7*, generated by address decoder U4, go directly to the EPROM sockets, one to each socket (see Fig. 5-4). Any unused socket can be disabled by removing the correct jumper. Jumper W4's positions 15-16 through 1-2 correspond to sockets 0-7, respectively. Besides removing the chip-enable signal from the socket, the removal of one of these jumpers also disables the data-bus buffer over the address range of the unused socket, because the chip-enable signals also go to OR gate U7. The resulting signal is part of the data-bus buffer logic. If a chip-enable jumper is removed, the data-bus buffer does not get enabled. Note that the chip-enable lines contain pull-up resistors, to ensure that the lines stay in the inactive state if a jumper is removed.

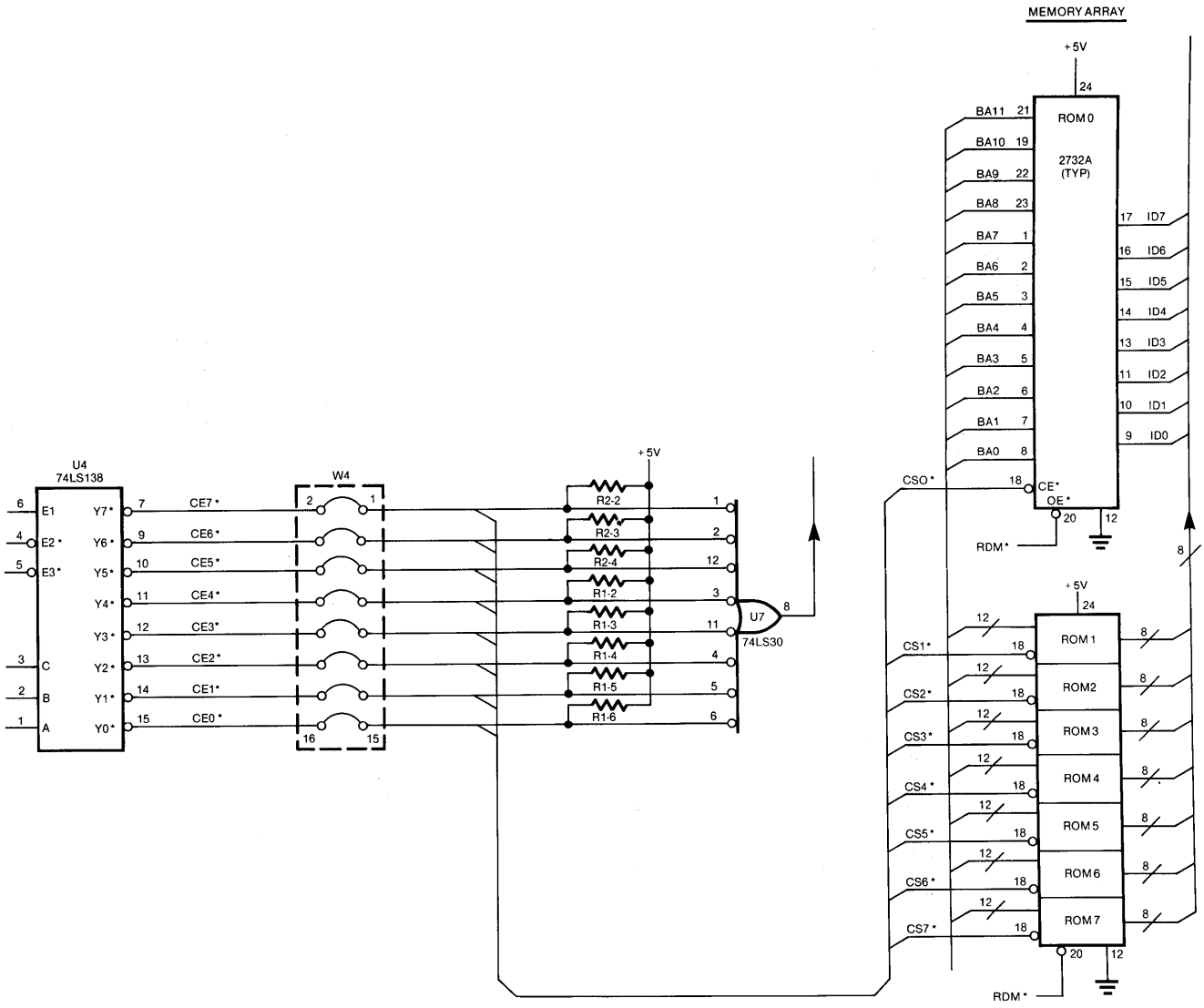


Figure 5-4. Chip-Enable Circuit for the 7705.

Output-Enable Circuit

The output-enable signal required by 2732/2732A EPROMs is generated by a combination of the RD* and MEMRQ* signals (see Fig. 5-5). Both of these lines are buffered by U3, then ANDed together by U5. The resulting signal, RDM*, is common to all eight sockets and serves as the output-enable signal.

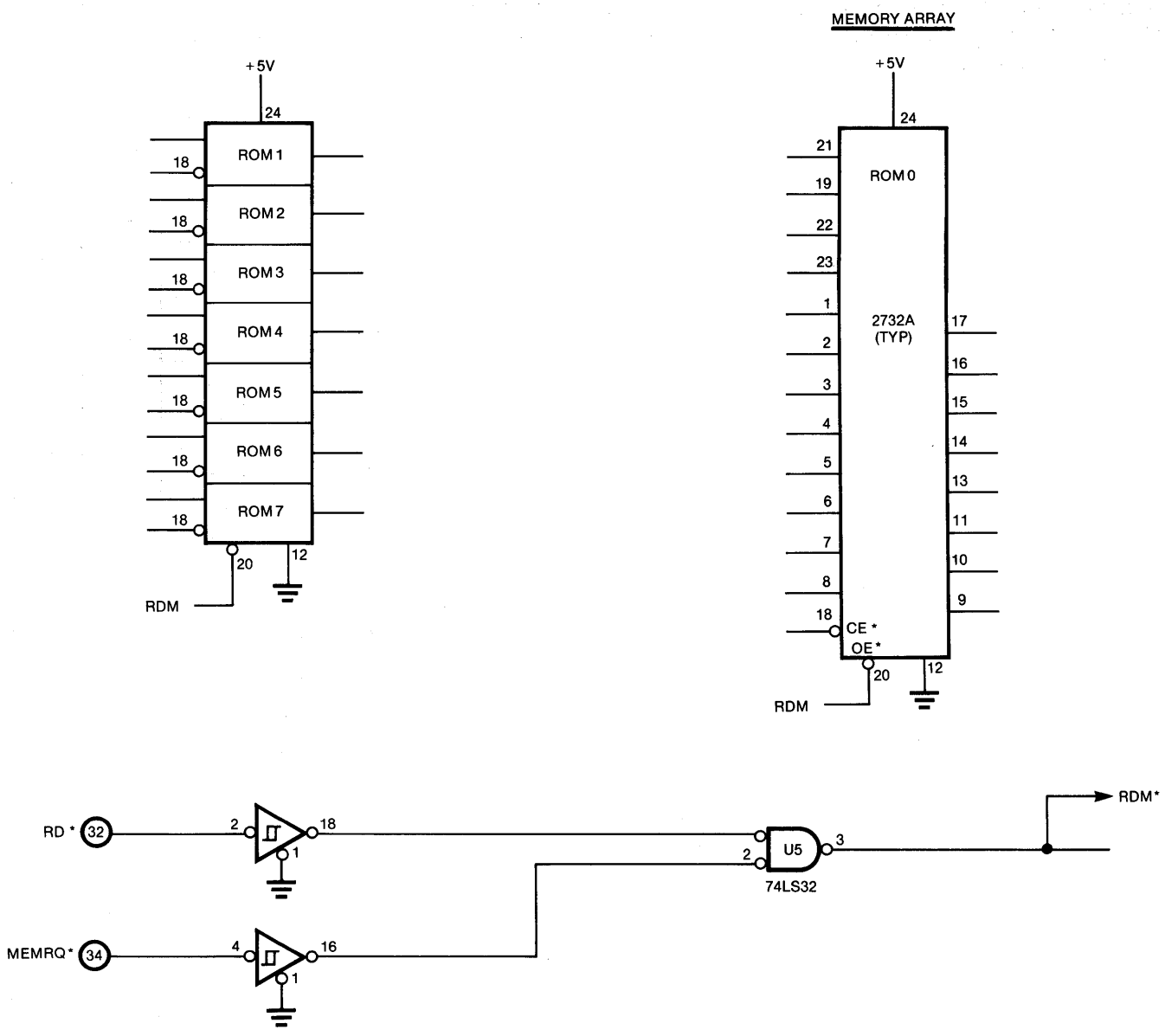


Figure 5-5. Output-Enable Circuit for the 7705.

Data-Bus Buffer Circuit

The data-bus buffering is done by U1 (see Fig. 5-6). It is unidirectional, three-state, and noninverting. The logic that controls the buffer-enable signal comprises two gates from U5 and one from U6. The conditions that need to exist for the bus buffer to be enabled are as follows:

First, the output of the OR gate U7 signal must be active. This is a function of the address lines, the MEMEX line, and the chip-enable lines. The address lines and MEMEX line are explained in the "Address Decoder Circuit" subsection. The chip-enable lines are explained in the "Chip-Enable Circuit" subsection.

Second, the segment select line must be active. Segment select, after being buffered by U3, can be inverted or not inverted depending on the position of jumper W3. When jumper W3 is in position 1-2, as it is when the 7705 is shipped, segment select is high-level active. When the jumper W3 is in position 3-4, it is low-level active. Note that a pull-up resistor is on the line, where it enters the card. This means that if the line is left unconnected, jumper W3 should be left in position 1-2 for the card to be enabled.

Third, the RDM* signal must be active. This signal is a combination of RD* and MEMRQ*, as described in the previous subsection.

When all of these conditions exist, the buffer is enabled-out; otherwise, it is left floating.

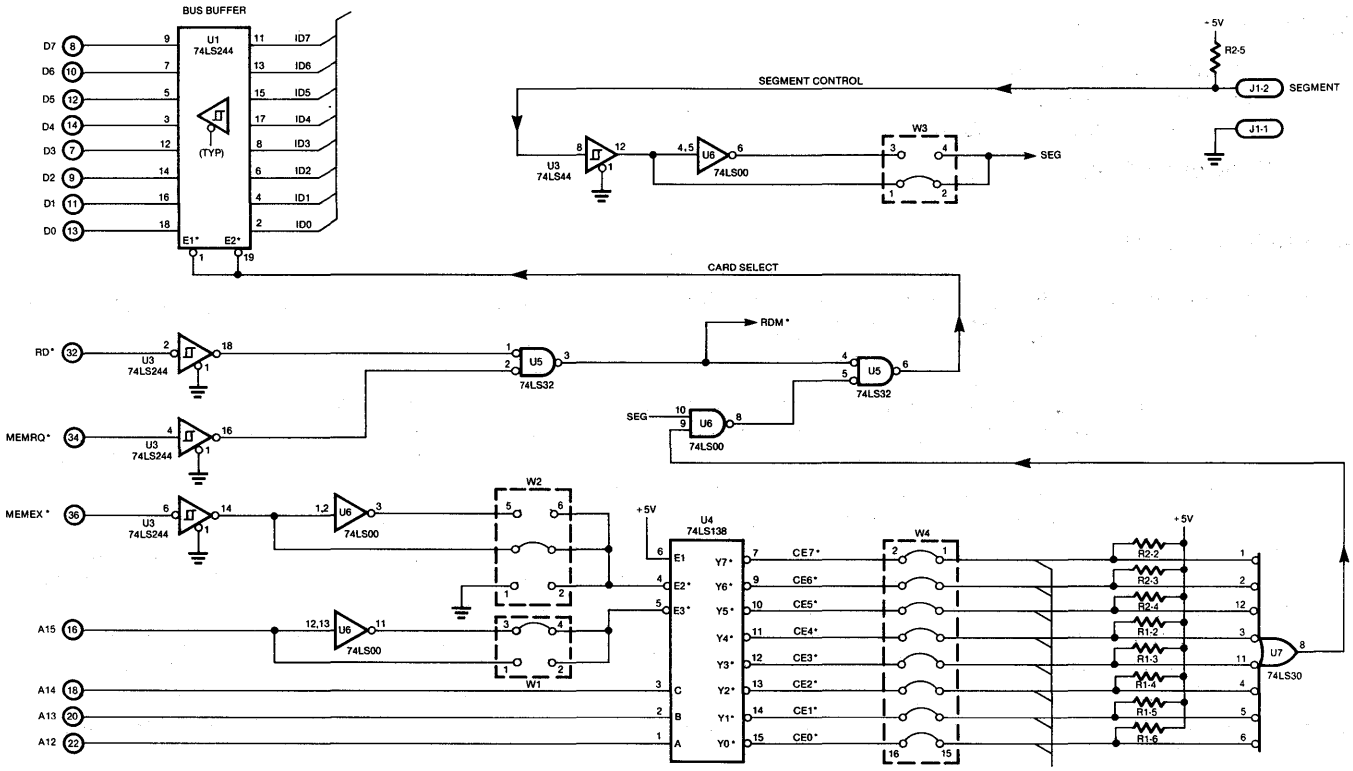


Figure 5-6. Data-Bus Buffer Circuit for the 7705.

Return for Repair Procedures

Domestic Customers:

1. Call our factory direct at (408) 372-4593, and ask for CUSTOMER SERVICE.
2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.
3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment, if applicable, reason for return, and the name and telephone number of the person we should contact (preferably the user), if we have any further questions.
4. Package the equipment in a solid cardboard box secured with packing material.

   CAUTION: Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during shipment. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.
5. Ship prepaid and insured to:

   Pro-Log Corporation
   2411 Garden Road
   Monterey, California 93940

   Reference CRO # _____ .

International Customers:

Equipment repair is handled by your local Pro-Log Distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

Limited Warranty: Seller warrants that the articles furnished hereunder are free from defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. The liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned F.O.B. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorizd repair or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller or the repaired or replaced part whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to Buyer's specifications except as specifically stated in writing by Seller and contained in the contract.

USER'S MANUAL

PRO-LOG CORPORATION

2411 Garden Road
Monterey, California 93940
Telephone: (408) 372-4593
TWX: 910-360-7082
Telex: 171829

107877

~~108776A 3.5K 12/81~~