CUTS, COMPUTER USERS TAPE SYSTEM

ASSEMBLY and TEST INSTRUCTIONS

Processor Technology Corporation
6200 Hollis Street
Emeryville CA 94608

SECTION I

INTRODUCTION and

GENERAL INFORMATION

CUTS, COMPUTER USERS TAPE SYSTEM

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1.1 INTRODUCTION

This manual supplies the information needed to assemble, test and use the CUTS, Computer Users Tape System. We suggest that you first scan the entire manual before starting assembly. Then, make sure you have all the parts and components listed in the "Parts List" (Table 2-1) in Section II. When assembling the module, follow the instructions in the order given.

Should you encounter any problem during assembly, call on us for help if necessary. If your completed module does not work properly, recheck your assembly step by step. Most problems stem from poor soldering, backward installed components, and/or installing the wrong component. Once you are satisfied that the module is correctly assembled, feel free to ask for our help.

1.2 GENERAL INFORMATION

1.2.1 CUTS Description

CUTS, The Computer Users Tape System is a high speed, simple to use audio cassette interface that operates at 300 and 1200 bps data rates under program control. The recording technique used is asynchronously Manchester coded at 1200 or 2400 Hz and is CUTS/Byte/ Kansas City Standard compatible.

Two separate tape transport control outputs and two common audio inputs and outputs are provided to drive one or two recorders. In addition, CUTS has provision for selecting 1) a low level audio output signal for driving the microphone input to an audio recorder, 2) a high level audio output signal for driving the auxiliary input to an audio recorder, and 3) a 5-volt peak-to-peak square save output for driving a digital recorder. A fully automatic gain control operates in the read mode. Unlike other cassette interfaces, CUTS has absolutely no critical adjustments that must be preset or adjusted during operation.

NOTE

All Processor Technology software is available on CUTS cassettes at lower cost than equivalent paper tapes.

1.2.2 Receiving Inspection

When your kit arrives, examine shipping container for signs of possible damage to the contents during transit. Then inspect the contents for damage. (We suggest you save the shipping materials for use in returning the module to Processor Technology should it become necessary to do so.) If your CUTS kit is damaged, please write us at once describing the condition so that we can take appropriate action.

1.2.3 Warranty Information

In brief, parts that fail because of defects in materials or workmanship are replaced at no charge for 3 months for kits, and one year for assembled products, following the date of purchase. Also, products assembled by the buyer are warranted for a period of 3 months after the date of purchase; factory assembled units carry a one year warranty. Refer to Appendix I for the complete "Statement of Warranty".

1.2.4 Replacement Parts

Order replacement parts by component nomenclature (DM8131 IC or 1N2222 diode, for example) and/or a complete description (680 ohm, ¼ watt, 5% carbon resistor, for example).

1.2.5 Factory Service

In addition to in-warranty service, Processor Technology also provides factory repair service on out-of-warranty products. Before returning the unit to Processor Technology, first obtain our authorization to do so by writing us a letter describing the problem. After you receive our authorization to return the unit, proceed as follows:

1. Write a description of the problem.

2. Pack the unit with the description in a container suitable to the method of shipment.

3. Ship prepaid to Processor Technology Corporation, 6200 Hollis Street, Emeryville, CA 94608.

Your unit will be repaired as soon as possible after receipt and return shipped to you prepaid. (Factory service charges will not exceed $20.00 without prior notification and your approval.)

SECTION II

ASSEMBLY

and

TEST

CUTS, COMPUTER USERS TAPE SYSTEM

Processor Technology

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6200 Hollis Street
Emeryville CA 94608

2.1 PARTS AND COMPONENTS

Check all parts and components against the "Parts List" (Table 2-1 on Page II-2). If you have difficulty in identifying any parts by sight, refer to Figure 2-1 on Page II-3.

2.2 ASSEMBLY TIPS

1. Scan Section II in its entirety before you start to assemble your CUTS kit.

2. In assembling your CUTS, you will be following a step-by-step assembly procedure. FOLLOW THE INSTRUCTIONS IN THE ORDER GIVEN.

3. Assembly steps and component installations are preceded by a set of parentheses. Check off each installation and step as you complete them. This will minimize the chances of omitting a step or component.

4. When installing components, make use of the assembly aids that are incorporated on the CUTS PC board and the assembly drawing. (These aids are designed to assist you in correctly installing the components.)

   a. The circuit reference (R3, C10 and U7, for example) for each component is silk screened on the PC board near the location of its installation.

   b. Both the circuit reference and value or nomenclature (1.5K and 74LS08, for example) for each component are included on the assembly drawing near the location of its installation.

5. To simplify reading resistor values after installation, install resistors so that their color codes read from left-to-right and top-to-bottom as appropriate (board oriented as defined in Paragraph 2.5 on Page II- .)

6. Unless specified otherwise in the instructions, install components--especially disc capacitors--as close to the board as possible.

7. Should you encounter any problem during assembly, call on us for help if needed.

Table 2-1. CUTS Parts List

INTEGRATED CIRCUITS

1	1458 or 5558 (U6)	1	6011 (U18)
2	4013 (U3 & U4)	1	74LS04 (U24)
1	4019 (U9)	2	74LS08 (U25 & U26)
1	4023 (U1)	1	74LS109 (U20)
1	4024 (U10)	1	74LS132 (U21)
1	4027 (U2)	2	74LS136 (U14 & U15)
1	4030 (U19)	1	74LS155 (U23)
1	4046 (U11)	1	74LS163 (U12)
1	4049 (U22)	1	74LS175 (U13)
1	4520 (U8)	2	74367 (U16 & U17)

REGULATORS

1	7805UC or LM340T-5.0 (U7)
1	78L12 (U5)

TRANSISTORS

3	2N2222 (Q1, Q3 & Q4)
1	2N2907 (Q5)
1	2N4360 (Q2)

DIODES

3	1N4148 (D1, D2 & D4)
1	1N5242 (D3)

RELAYS

2	DIP Reed, SIGMA 191TE1A1-55 (K1 & K2)

Table 2-1. CUTS Parts List (Continued).

RESISTORS

1	39	ohm, 2 watt, 5%
1	100	ohm, ¼ watt, 5%
2	470	ohm, ¼ watt, 5%
3	1.5K	ohm, ¼ watt, 5%
9	10 K	ohm, ¼ watt, 5%
4	100 K	ohm, ¼ watt, 5%
2	150 K	ohm, ¼ watt, 5%
2	1 M	ohm, ¼ watt, 5%
1	2.2M	ohm, ¼ watt, 5%
1	50 K	ohm Potentiometer
2	2.2K	ohm Resistor Network

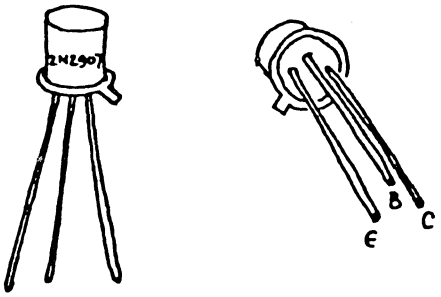
CAPACITORS

1	470	pfd, disc
4	.001	ufd, disc
1	.001	ufd, Mylar tubular
1	.01	ufd, Mylar tubular
19	.1	ufd, disc
2	1	ufd, tantalum dipped
3	15	ufd, tantalum dipped

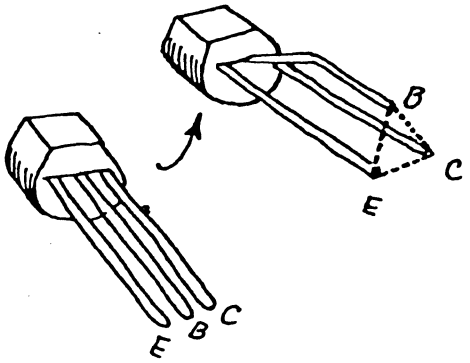
MISCELLANEOUS

1	CUTS PC Board
1	Heat Sink
11	14-pin DIP Socket
11	16-pin DIP Socket
1	40-pin DIP Socket
1	8-position DIP Switch
2	Right Angle Molex Connector, Male (J1 & J2)
2	Mating Connector for Above, Female (P1 & P2)
10	Molex Crimp Pins for Female Mating Connector
3	Augat Pin
1	Length #24 Bare Wire
1	Length Solder
3	6-32 x ½ Screw
3	#6 Lockwasher
3	6-32 Hex Nut
1	Manual

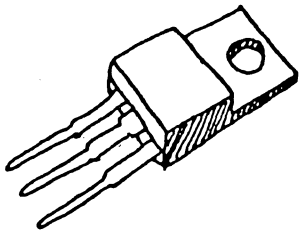
TRANSISTOR
TO-18 Package (Metal Can)



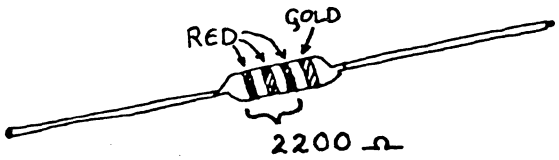
TRANSISTOR
TO-92 Package (Plastic)



TRANSISTOR, POWER or
REGULATOR IC
TO-220 Package

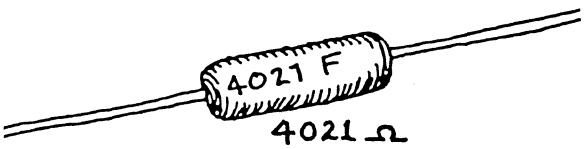


CARBON RESISTOR



5% (gold), 10% (silver)
See Appendix III for Color Code

METAL FILM PRECISION RESISTOR
(1% Tolerance)



RESISTOR NETWORK

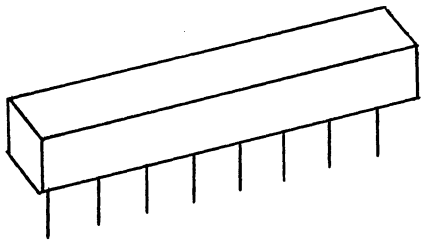
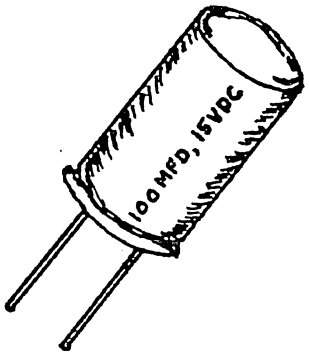
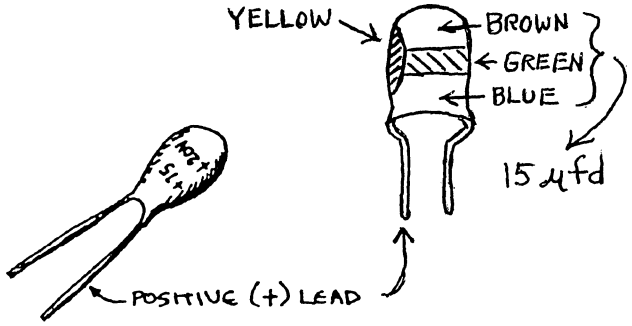


Figure 2-1. Identification of components.

ELECTROLYTIC CAPACITOR
(Vertical Mount)

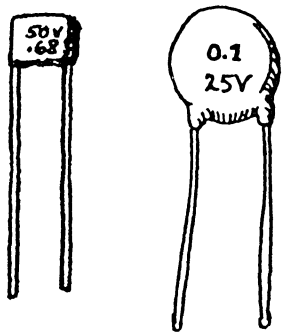


DIPPED TANTALUM ELECTROLYTIC CAPACITOR



See Appendix III for Color Code

DISC CAPACITOR



Monolythic (left) and Ceramic

MYLAR TUBULAR CAPACITOR

INTEGRATED CIRCUIT, Dual Inline Package (DIP)
(6,8,14,16,24 and 40 pin)

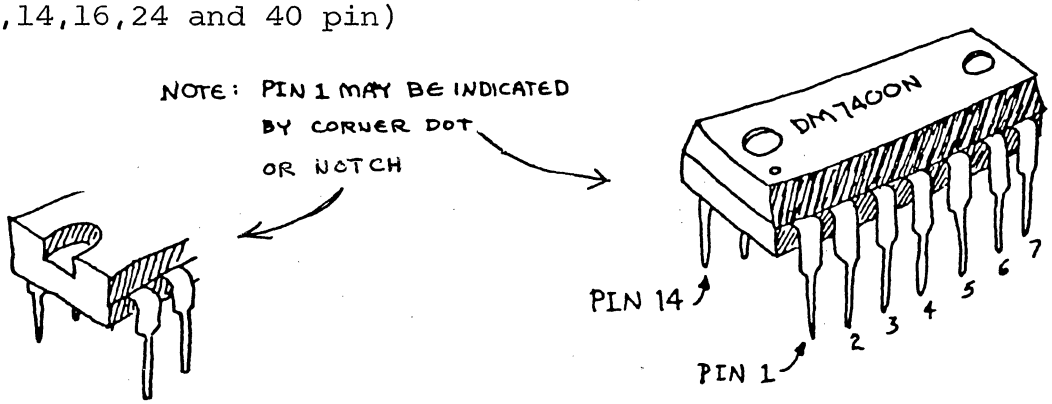


Figure 2-1. Identification of components.

2.3 ASSEMBLY PRECAUTIONS

2.3.1 Handling MOS Integrated Circuits

Many of the IC's used in the CUTS are MOS devices. They can be damaged by static electricity discharge. Always handle MOS IC's so that no discharge will flow through the IC. Also, avoid unnecessary handling and wear cotton--rather than synthetic--clothing when handling these IC's.

2.3.2 Soldering **IMPORTANT**

1. Use a fine tip, low-wattage iron, 25 watts maximum.

2. DO NOT use excessive amounts of solder. DO solder neatly and as quickly as possible.

3. Use only 60-40 rosin-core solder. NEVER use acid-core solder or externally applied fluxes.

4. To prevent solder bridges, position iron tip so that it does not touch adjacent pins and/or traces simultaneously.

5. DO NOT press tip of iron on pad or trace. To do so can cause the pad or trace to "lift" off the board and permanently damage it.

6. The CUTS circuit board has plated-through holes. Solder flow through to the component (front) side of the board can produce solder bridges. Check for such bridges after you install each component.

7. The CUTS circuit board has an integral solder mask (a lacquer coating) that shields selected areas on the board. This mask minimizes the chances of creating solder bridges during assembly. DO, however, check all solder joints for possible bridges.

8. Additional pointers on soldering are provided in Appendix III of this manual.

2.3.3 Installing and Removing CUTS Module

NEVER install the CUTS in, or remove it from the computer with the power on. To do so can damage the module.

2.3.4 Installing and Removing Integrated Circuits.

NEVER install or remove integrated circuits while power is applied to the CUTS. To do so can damage the IC.

2.3.5 Use of Clip Leads

NEVER attach clip leads to the top edge of the CUTS PC board. To do so can short the +8, +16 and -12 V dc buses to one another.

2.4 REQUIRED TOOLS, EQUIPMENT AND MATERIALS

The following tools, equipment and materials are recommended for assembling and testing the CUTS Module:

1. Needle nose pliers
2. Diagonal cutters
3. Scredriver
4. Sharp knife
5. Controlled heat fine tip soldering iron, 25 watts
6. 60-40 rosin-core solder (supplied)
7. #24 bare wire (supplied)
8. Volt-ohm meter

2.5 ORIENTATION

The heat sink area (large foil area) will be located in the upper right-hand corner of the board when the edge connector is at the bottom. In this position, the component (front) side of the board is facing up and the solder (back) side is facing down. In addition the IC legends (U1 through U4, U8 through U15, etc.) will read from left to right. Subsequent position references in the instructions related to the CUTS PC board assume this orientation.

2.6 ASSEMBLY-TEST

Refer to the assembly drawing in Section VI.

CAUTION

THE CUTS MODULE USES MANY MOS AND CMOS INTEGRATED CIRCUITS. THEY CAN BE DAMAGED BY STATIC ELECTRICITY DISCHARGE. HANDLE THESE IC's SO THAT NO DISCHARGE FLOWS THROUGH THE IC. AVOID UNNECESSARY HANDLING AND WEAR COTTON--RATHER THAN SYNTHETIC--CLOTHING WHEN YOU DO HANDLE THESE IC's. (STATIC CHARGE PROBLEMS ARE MUCH WORSE IN LOW HUMIDITY CONDITIONS.)

2.6.1 Circuit Board Check

( ) Visually check CUTS PC board for solder bridges (shorts) between traces, broken traces and similar defects.

( ) Check board to insure that the +8-volt line, +16-volt line, +5-volt bus, +12-volt bus and -12-volt bus are not shorted to one another or to ground. Using an ohmmeter, make the following measurements (refer to CUTS assembly drawing in Section VI.):

( ) +8-volt Line Test. Measure between edge connector pin 1 or 51 (left end of connector) and pin 50 or 100 (right end of connector). There should be no continuity.

( ) +16-volt Line Test. Measure between edge connector pin 2 or 52 and pin 50 or 100. There should be no continuity.

( ) 8/16 Volt Line Test. Measure between edge connector pin 1 or 51 and pin 2 or 52. There should be no continuity.

( ) +5-volt Bus Test. Measure between the upper mounting pad for D2 (to the left of location K2) and pin 50 or 100 of the edge connector. There should be no continuity.

( ) +12-volt Bus Test. Measure between upper mounting pad for C9 (in upper right corner below C8) and pin 50 or 100 of edge connector. There should be no continuity.

( ) -12-volt Bus Test. Measure between upper mounting pad for C18 (between U16 and U17) and pin 50 or 100 of edge connector. There should be no continuity.

( ) 5/12/(-12) Volt Bus Test. Measure between upper mounting pad for C21 (lower left corner) and upper pad for C9, between upper pad for C21 and upper mounting pad for C18, and between upper pad for C9 and upper pad for C18. You should measure no continuity in any of the three measurements.

If visual inspection reveals any defects, or you measure continuity in any of the preceding tests, return the board to Processor Technology for replacement.

If the board is not defective, go on to next paragraph.

2.6.2 Assembly-Test Procedure

Step 1. Install heat sink. Position the large, black heat sink (flat side to board) over the square foil area in the upper right corner. Orient the sink so that the two triangles of mounting holes in the board are under the two triangular cutouts in the sink. Using two 6-32 screws, lockwashers and nuts, attach heat sink to board. Insert the screws from back (solder) side of board. (See Figure 2-2.)

Step 2. Install U7 (7805UC or LM340T-5.0). Position U7 over left-hand cutout in heat sink and observe how the leads must be bent to fit the mounting holes. Note that the center lead (3) must be bent downwards at a point approximately 0.2 inches further from the body than the other two leads. Bend the leads so that no contact is made with the heat sink when U7 is flat against the sink and its mounting hole is aligned with the hole in the sink. Fasten U7 to sink using a 6-32 screw, lockwasher and nut. Insert screw from back (solder) side of board. Solder and trim leads. (Refer to Figure 2-2.)

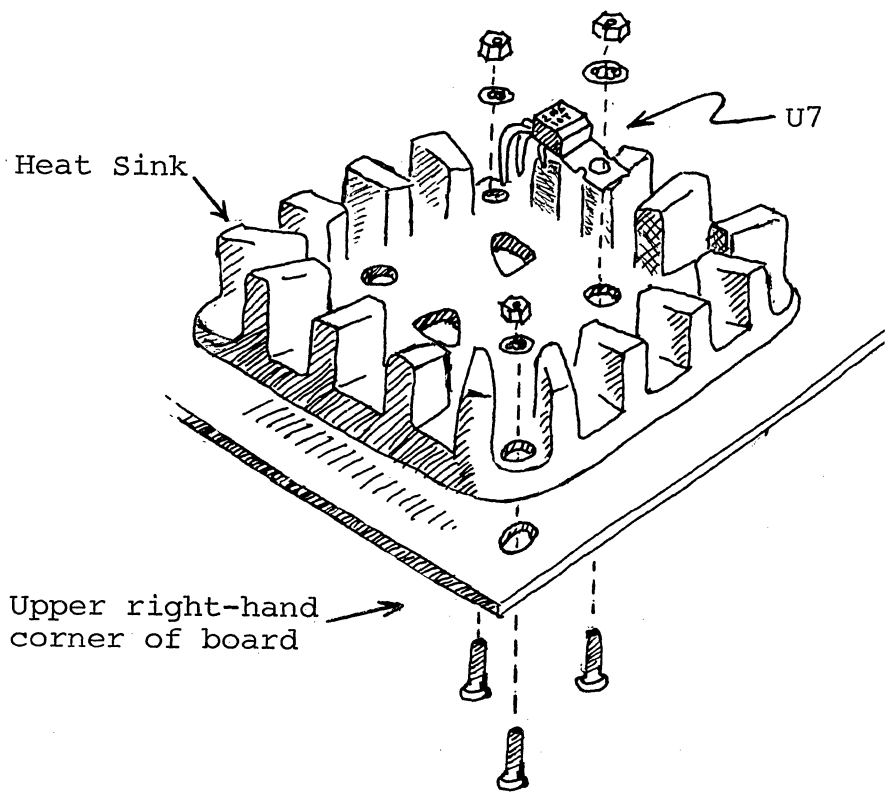


Figure 2-2. Heat sink and U7 installation.

( ) Step 3. Install male Molex right angle connectors in locations J1 and J2. Position connector with longer pins facing the top of the board, insert leads in mounting holes and solder.

( ) Step 4. Install diodes D1, D2 and D4 (1N4148) in their respective locations. Position D1 and D2 with their dark band mark (cathode) at the top and position D4 with its band at the right. Solder and trim leads.

( ) Step 5. Install diode D3 (1N5242) in its location. Position D3 with its dark band mark (cathode) at the right.

( ) Step 6. Install transistors Q1, Q3 and Q4 (2N2222) in their respective locations. Position Q1 with its emitter lead (closest to tab on can) at the top and its base lead at the left. Position both Q3 and Q4 with their emitter leads at the right and their base leads at the top. Insert leads and push straight down on transistor until it is 3/16" above the surface of the board. Solder and trim leads.

( ) Step 7. Install transistor Q2 (2N4360) in its location. Position Q2 with its flat side at the bottom, insert leads and push straight down on transistor until it is 3/16" above the surface of the board. Solder and trim leads.

( ) Step 8. Install transistor Q5 (2N2907) in its location. Position Q5 with its emitter lead (closest to tab on can) at the right and its base lead at the top. Insert leads and push straight down on transistor until it is 3/16" above the surface of the board. Solder and trim leads.

( ) Step 9. Install all resistors in numerical order in the indicated locations. Bend leads to fit distance between mounting holes, insert leads, pull down snug to board, bend leads outward on solder (back) side of board, solder and trim.

	LOCATION	VALUE (ohms)	COLOR CODE
( )	R1	100 K	brown-black-yellow
( )	R2	10 K	brown-black-orange
( )	R3	1.5K	brown-green-red
( )	R4	10 K	brown-black-orange
( )	R5	1.5K	brown-green-red
( )	R6	1.5K	" " "
( )	R7	10 K	brown-black-orange
( )	R8	150 K	brown-green-yellow
( )	R9	10 K	brown-black-orange
( )	R10	1 M	brown-black-green
( )	R11	10 K	brown-black-orange

Continued on Page II-11.

Step 9 continued.

	LOCATION	VALUE (ohms)	COLOR CODE
( )	R12	2.2M	red-red-green
( )	R13	10 K	brown-balck-orange
( )	R14	150 K	brown-green-yellow
( )	R15	10 K	brown-black-orange
( )	R16	470	yellow-violet brown
( )	R17	100	brown-black-brown
( )	R18	100 K	brown-black-yellow
( )	R19	10 K	brown-black-orange
( )	R20	10 K	" " "
( )	R21	470	yellow-violet-brown
( )	R22	39,2 watt	orange-white-black
( )	R23	100 K	brown-black-yellow
( )	R24	100 K	" " "
( )	R25	1 M	brown-black-green
( )	VR1	50 K	Potentiometer

( ) Step 10. Install resistor networks RX1 and RX2 (2.2K ohms) in their respective locations. Position RX1 so that the dot on its package is at the right end. Position RX2 with its dot at the left end.

CAUTION

THESE RESISTOR NETWORKS ARE DELICATE.
HANDLE WITH CARE.

( ) Step 11. Install the five tantalum capacitors in the following locations. Take care to observe proper values and the correct orientation.

	LOCATION	VALUE (ufd)	ORIENTATION
( )	C7	15	"+" lead left
( )	C8	15	"+" lead top left
( )	C21	1	"+" lead top
( )	C24	15	"+" lead right
( )	C29	1	"+" lead top

( ) Step 12. Install the following capacitors in the indicated locations. Take care to observe the proper value and type for each installation. Bend leads outward on solder (back) side of board, solder and trim.

Continued on Page II-12.

Step 12 continued.

NOTE

Disc capacitor leads are usually coated with wax during the manufacturing process. After inserting leads through mounting holes, remove capacitor and clear the holes of any wax. Re-insert and install.

LOCATION	VALUE (ufd)	TYPE
C1	.1	Disc
C2	.1	"
C3	.1	"
C4	.01	Mylar tubular
C5	.1	Disc
C6	.1	"
C9	.1	"
C10	.1	"
C11	.001	"
C12	.1	"
C13	.1	"
C14	.001	"
C15	.1	"
C16	.1	"
C17	.1	"
C18	.1	"
C19	.1	"
C20	.001	"
C22	.001	"
C23	.1	"
C25	.001	Mylar tubular
C26	.1	Disc
C27	.1	"
C28	.1	"
C30	.1	"
C31	470 pfd	"

Step 13. Install Augat pins in mounting holes A, B and C. (These three holes are located to the left of U16, just below the lower mounting hole for R17.)

NOTE

You will find it helpful to hold the board between two objects so that it stands on edge.

Continued on Page II-13.

Step 13 continued.

To install an Augat pin, insert it into the mounting hole from the component (front) side of board and solder the pin from the solder (back) side of the board so the solder "wicks up" to the front side. (This will hold the pin firmly in place.)

Then insert a component lead into the pin and reheat the solder. Using the component lead, adjust pin until it is perpendicular to board. Allow solder to cool while holding the pin as steady as possible.

NOTE

If the cooled solder is mottled or crystallized, a "cold joint" is indicated, and the solder should be reheated.

( ) Step 14. Install DIP switch in location S1. Position switch so Switch No. 1 is at the left. (With this orientation, the ON position of each switch is up.) Note that only the first seven switches are active.

( ) Step 15. Install DIP reed relays in locations K1 and K2. Be sure to position each relay with its end notch at the top (pin 1 in upper left corner). These relays are soldered to the board. (Refer to "Loading DIP Devices" in Appendix IV.)

( ) Step 16. Install U6 (1458 or 5558) in its location. Position U6 with its end notch at the top (pin 1 in upper left corner) and solder to board. (Refer to "Loading DIP Devices" in Appendix IV.)

( ) Step 17. Install U5 (78L12) in its location just above U6. Position U5 with its flat side at the bottom, insert leads and push straight down until it is 3/16" above the surface of the board. Solder and trim leads.

( ) Step 18. Install DIP sockets. Install each socket in the indicated location with its end notch oriented as shown on the circuit board and assembly drawing. Take care not to create solder bridges between the pins and/or traces.

INSTALLATION TIP

Insert socket pins into mounting pads of appropriate location. On back (solder) side of board, bend pins at opposite corners of socket (e.g. pins 1 and 9 on a

Continued on Page II-14.

Step 18 continued.

16-pin socket) outward until they are at a 45° angle to the board surface. This secures the socket until it is soldered. Repeat this procedure with each socket until all are secured to the board. Solder the unbent pins on all sockets. Then straighten the bent pins to their original position and solder.

LOCATION	TYPE SOCKET
U1	14 pin
U2	16 pin
U3	14 pin
U4	14 pin
U8	16 pin
U9	16 pin
U10	14 pin
U11	16 pin
U12	16 pin
U13	16 pin
U14	14 pin
U15	14 pin
U16	16 pin
U17	16 pin
U18	40 pin
U19	14 pin
U20	16 pin
U21	14 pin
U22	16 pin
U23	16 pin
U24	14 pin
U25	14 pin
U26	14 pin

( ) Step 19. Using #24 bare wire, install jumpers according to your selection of the options described in Section III.

( ) Step 20. Set DIP switches (S1) to select port address as described in Section III.

NOTE

All Processor Technology software is written with a CUTS port of FA (hex). To set the DIP switches for port FA, place Switch No. 2 in OFF position and the remaining switches in the ON position.

( ) Step 21. Check operation of the regulators. This check is made to prevent potential damage to the IC's from incorrect voltages.

( ) Using an ohmmeter, make the following measurements:

SUPPLY	MEASUREMENT POINTS
+ 5 V dc	Ground to right-hand lead of U7 Ground to left-hand lead of U7
+12 V dc	Ground to positive (+) lead of C8 Ground to Pin 8 of U6 socket
-12 V dc	Across C21

You should measure some resistance in all three measurements. Zero resistance indicates a short. If required, find and correct the problem before proceeding.

( ) Install CUTS in computer. (The use of a Processor Technology EXB Extender Board is recommended.)

CAUTION

NEVER INSTALL OR REMOVE CIRCUIT BOARD WITH POWER ON.

( ) Turn power on and make the following voltage measurements:

MEASUREMENT POINTS	VOLTAGE (±5%)
Ground to Pin 1 of U18 Socket	+ 5 V dc
Ground to Pin 8 of U6 Socket	+12 V dc
Ground to Pin 2 of U18 Socket	-12 V dc

If any voltage is incorrect, determine and correct the cause before proceeding.

If voltages are correct, turn power off, remove CUTS from computer and go on to Step 22.

( ) Step 22. Install the following IC's in the indicated locations. Pay careful attention to the proper orientation.

Continued on Page II-16.

Step 22 Continued.

NOTE

Pin 1 is positioned at the upper left corner of each IC location, and is indicated by a dot on the PC board and assembly drawing.

IC NO.	TYPE
U1*	4023*
U2*	4027*
U3*	4013*
U4*	4013*
U8*	4520*
U9*	4019*
U10*	4024*
U11*	4046*
U12	74LS163
U13	74LS175
U14	74LS136
U15	74LS136
U16	74LS367
U17	74LS367
U18*	6011*
U19*	4030*
U20	74LS109
U21	74LS132
U22*	4049*
U23	74LS155
U24	74LS04
U25	74LS08
U26	74LS08

*MOS device. Refer to CAUTION on Page II-7.

( ) Step 23. Adjust VR1.

NOTE

If you do not have a voltmeter, set arrow on VR1 to the "10 o'clock" position (as viewed from front side of board when VR1 is at the top) and go on to Step 24. (In nearly all cases CUTS operates with VR1 at 10 o'clock.)

Continued on Page II-17

Step 23 continued.

(✓) If you selected either the digital or microphone audio output options in Step 19, remove the jumper and install a jumper between Augat pins A and B.

(✓) If you selected the auxiliary option in Step 19, leave the jumper between Augat pins A and B installed.

(✓) Connect pin 2 of J1 (IN) to pin 4 of J1 (OUT).

( ) Install CUTS in computer and turn power on.

( ) Set VR1 fully clockwise (CW).

( ) Measure the DC voltage at pin ~~2~~ 9 of ~~U2~~ U11 and write the measured voltage down. (Call this Voltage A.)

( ) Set VR1 fully counterclockwise (CCW).

( ) Measure the DC voltage at pin ~~2~~ 9 of ~~U2~~ U11 and write the measured voltage down. (Call this Voltage B.)

( ) Add Voltages A and B and divide the sum by 2. (Call the result Voltage C.) An example follows:

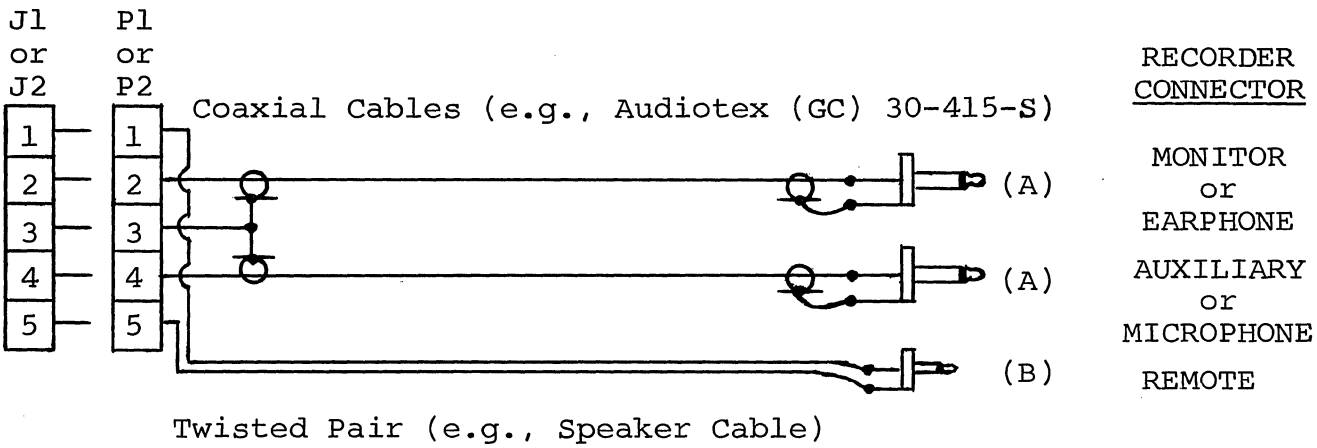
Voltage A (VR1 fully CW):	3.45 V dc
Voltage B (VR1 fully CCW):	1.80 V dc
A + B =	5.25 V dc
Voltage C = 5.25 V dc/2 =	2.63 V dc

( ) Adjust VR 1 so that the voltage at pin 3 of U2 equals Voltage C. (In the preceding example this would be 2.63 V dc.)

( ) Step 24. Disconnect pin 2 of J1 from pin 4 of J1.

( ) Step 25. If required by your option selection, remove the A-to-B jumper and re-install the A-to-D or A-to-C jumper as appropriate. Otherwise, leave the A-to-B jumper in and go on to Step 26.

( ) Step 26. Using the two female mating connectors supplied for J1 and J2, fabricate one or two, as required by your needs, CUTS-to-Recorder interconnect cables as shown in Figure 2-3 on Page II-18.



1 - Transport
2 - Audio In
3 - Ground
4 - Audio Out
5 - Transport Return

(A) Miniature Phone Plug
(B) Subminiature Phone Plug

Figure 2-3. CUTS-transport interconnect cabling.

SECTION III

OPTION SELECTION

CUTS, COMPUTER USERS TAPE SYSTEM

Processor Technology

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6200 Hollis Street
Emeryville CA 94608

3.1 OPTION SELECTION

Jumper options that control two operating parameters, data rate and audio output, are provided on the CUTS Module. The port address for the module is selectable with seven switches. Use the following selection instructions along with the assembly drawing in Section VI.

3.2 PORT ADDRESS SELECTION (DIP Switch, S1)

One of 130 possible port addresses, from Ø through FA (hex), 254 (decimal), for the CUTS is selectable with the first seven DIP switch positions in location S1.

All Processor Technology software is written for a CUTS port assignment of FA (hex). To configure your CUTS for this port, set Switch No. 2 (S1-2) to OFF and Switch No's. 1 (S1-1) and 3 through 7 (S1-3 through S1-7) to ON.

To select another port, set S1-1 through S1-7 as required for the desired address. With these switches the address increases from Ø (all seven switches open) in a binary fashion to 254, decimal, (all seven switches closed). When setting these switches, keep in mind that 1) S1-7 and S1-1 are the most and least significant bits respectively and 2) a closed switch is equivalent to a binary 1.

3.3 AUDIO OUTPUT SELECTION

The A, B, C, D jumper arrangement (to the left of U16) determines the audio output signal supplied to J1 and J2. Three choices are available: 1) a 5 V peak-to-peak signal for driving digital recorders, 2) a 250 mV signal for driving the auxiliary input to an audio cassette recorder, and 3) a 50 mV signal for driving the microphone input to an audio cassette recorder.

NOTE

For audio cassette recorders, the auxiliary input is preferred and recommended over the microphone input.

To select the digital recorder output, install a jumper (#24 bare wire is recommended) between Augat pin A and the mounting pad labeled D.

To select the auxiliary output to drive the auxiliary input (the recommended input) to an audio cassette recorder, install a jumper (#24 bare wire is recommended) between Augat pins A and B.

To select the microphone output to drive the microphone input to an audio cassette recorder, install a jumper (#24 bare wire is recommended) between Augat pins A and C.

3.4 DATA RATE SELECTION

Your CUTS is presently wired for both 1200 and 300 Baud operation, with the selection being program controlled. CUTS is designed, however, for operating at data rates up to 9600 Baud. The pad labeled AA, K, L, Q, R, S, T, U, V, W, X, Y and Z are provided for increasing the data rate. How the board is configured for higher rates will be the subject of a future addendum to this manual.

At this point in time Processor Technology does not recommend operation higher than 1200 Baud.

SECTION IV

OPERATING PROCEDURES

CUTS, COMPUTER USERS TAPE SYSTEM

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6200 Hollis Street
Emeryville CA 94608

4.1 TAPE RECORDER

Any standard cassette tape recorder can be used with CUTS providing it has the following features:

- ALC (automatic level control) in record mode
- "Remote" on-off control input jack
- "Monitor" or "earphone" output jack

Though not required, the following recorder features will be useful:

- Tone control
- Tape counter
- "Cue", "Pause" or "Instant Stop" control

NOTE

Processor Technology currently uses the Panasonic Model RQ-413S with consistently good results.

4.2 CUTS-RECORDER INTERCONNECT (Single Recorder)

Using the interconnect cabling you fabricated in Step 26 of the "Assembly-Test Procedure" (Section II), make the following connections: (Refer to Figure 4-1 on Page IV-3. You may use either output connector J1 or J2 on the CUTS.)

1. Plug transport cable (Pins 1 and 5 of J1 or J2) to remote jack on recorder.
2. Connect "audio out" cable (Pin 4 of J1 or J2) to microphone or auxiliary jack on recorder, with the choice depending on the audio output selection you made. (Refer to Paragraph 3.3 in Section III.) The auxiliary input is preferred and recommended over the microphone input.
3. Connect "audio in" cable (Pin 2 of J1 or J2) to monitor or earphone jack on recorder.

4.3 CUTS-RECORDER INTERCONNECT (Two Recorders)

Two recorders, under program control, can be driven by CUTS. In this case you will need two sets of the interconnect cabling described in Step 26 of the "Assembly-Test Procedure" (Section II).

Using these interconnect cables, connect the CUTS and recorders as shown in Figure 4-1.

When using two recorders you may read or write to both under program control as well as read one tape while writing on the other.

If you intend to read one tape while writing on the other, however, you may have to disconnect the "monitor" plug from the write unit, with the need for disconnect being determined by the recorder design. The monitor disconnect must be made if the recorder provides a "monitor" output in the record mode. (Panasonic RQ-413S and RQ-309DS do, for example.)

NOTE 1

Recorders on which the "monitor" jack is labeled MONITOR usually provide a monitor output in the record mode. If the jack is labeled EAR or EARPHONE, the recorder usually does not provide a monitor output in the record mode.

NOTE 2

To determine if your recorder provides a monitor output in the record mode, install a blank tape, plug earphone into "monitor" jack and microphone into microphone jack, set recorder controls to record, and speak into microphone while listening with the earphone. If you hear yourself through the earphone, your recorder does provide a monitor output in the record mode.

4.4 RECORDER ADJUSTMENTS

4.4.1 Volume Control

Since CUTS incorporates AGC (automatic gain control) circuitry in the read mode and the recorder has ALC in the record mode, the Volume Control setting should not be critical for either read or write operations. Simply set the control at midrange and forget it.

4.4.2 Tone Control

If your recorder has a Tone Control, set it at the top (high end) of its range. Tone controls usually have little effect, but it is safer to obtain a fairly high frequency response by setting the control as just described.

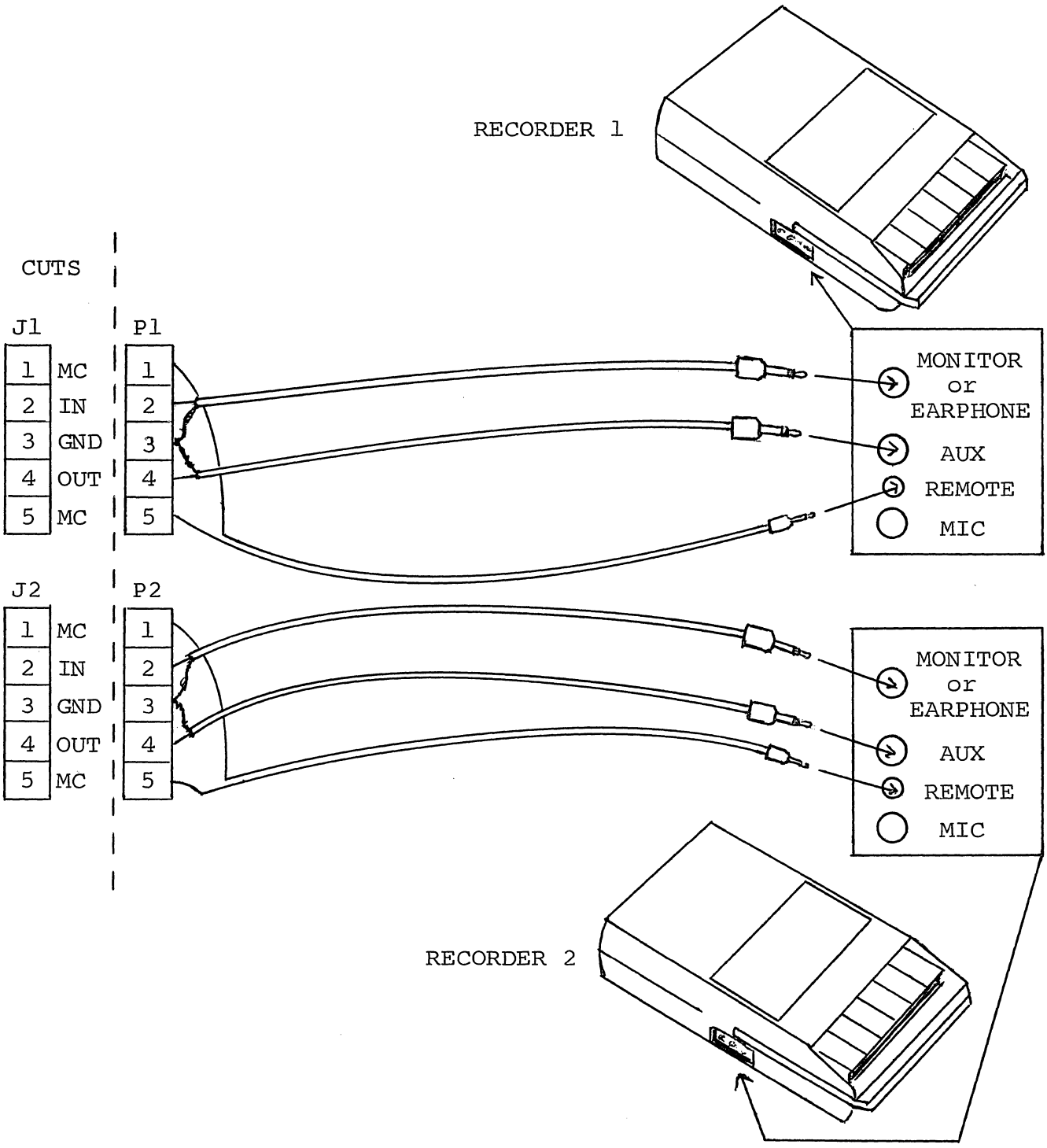


Figure 4-1. CUTS-recorder interconnect (two recorders).

4.5 WRITE OPERATIONS

Other than placing the recorder in the record mode, loading the tape and making sure that the head is on tape (not leader), no manual operations are needed to write on tape.

4.6 READ OPERATIONS

When reading tapes, you must start the tape at least two seconds ahead of the data block you want to read. (CUTS tapes have a standardized header before each data block.) This two second delay is needed to allow the recorder playback electronics and the CUTS circuitry to stabilize after power is turned on.

Use the following procedure for loading tapes:

1. Disconnect monitor and remote plugs from recorder. (On most recorders this must be done in order to listen to the tape.)

2. Load prerecorded cassette and play tape until you hear data. (Data sounds like noise in CUTS format.)

NOTE

Absence of data is indicated by a pure 1200 Hz or 2400 Hz tone if recorded at 1200 bps or 300 bps respectively in the Byte/Kansas City Standard format.

3. Rewind tape far enough so it will take two seconds to reach the data block you want to read after the recorder is placed in the playback mode. STOP RECORDER AT THIS POINT.

4. Set Volume Control as specified in Paragraph 4.4.1 if necessary.

5. Reconnect monitor and remote plugs to recorder.

6. Place "play" control on recorder in play position.

7. Type in appropriate command on your keyboard. After you strike the RETURN key (in most programs), the recorder will automatically start and data will be read into memory at the locations specified by the CUTS data header or, in the case of BASIC-5 or Processor Technology 8K BASIC, into the proper File or READ statement.

SECTION V

THEORY OF OPERATION

CUTS, COMPUTER USERS TAPE SYSTEM

Processor Technology

Processor Technology Corporation
6200 Hollis Street
Emeryville CA 94608

5.1 INTRODUCTION

The CUTS module functions to transfer data bidirectionally between a computer and one or two audio cassette recorders. To perform its function, the module contains circuitry related to:

1. port address recognition,
2. computer-CUTS buffering,
3. computer input/output command decoding,
4. timing,
5. status reporting,
6. recorder on/off control,
7. parallel-to-serial and digital-to-audio conversions in the write mode,
8. audio-to-digital and serial-to-parallel conversions in
9. and conversion of read data to NRZ (non-return to zero) format.

5.2 BLOCK DIAGRAM ANALYSIS

A simplified block diagram of the CUTS module is provided in Figure 5-1.

An address selector defines the port address for the CUTS module. It works with the address decoder to determine if the address on A1-7 matches the port address for the module. If it does, the decoder produces the indicated CARD SELECT output to enable the status in/out and strobe decoders.

Once an input or output request from the processor is recognized, the status in/out decoder enables a PRDY line driver in the wait state generator. This generator inserts one wait state into every input or output request from the processor.

The strobe decoder decodes the indicated inputs from the processor to produce the STATUS WRITE, READ STATUS, DATA READ and DATA WRITE strobe signals.

On an input cycle when AØ is low, AØ enables status outputs from the UART, and the strobe decoder outputs a READ STATUS signal. READ STATUS produces a delayed DRIVER ENABLE which gates the UART status to the DI bus. Should AØ be high, however, the strobe decoder outputs a DATA READ to indicate to the UART that its data has

been accepted. It also resets the driver enable generator to immediately enable the DI bus drivers.

If the cycle is an output cycle and AØ is high, the strobe decoder outputs a DATA WRITE which transfers DO bus data into the UART and initiates serial transmission by the UART. Should AØ be low, the strobe decoder outputs a STATUS WRITE. STATUS WRITE strobes the data on DO4-7 into the status latch.

The four status bits in this latch are concerned with recorder motor control and data rate. One output turns one recorder motor on and off, another turns a second recorder motor on and off, a third selects a low data rate, and the fourth selects a high data rate.

Timing for the CUTS module is supplied by the clock circuits and read clock. Clock circuitry manipulates Ø2 to supply WRITE CLOCK as well as various other timing signals required to obtain two data rates. Read clock uses NRZ data transitions and one of two clock signals to generate READ CLOCK for use in the read mode.

When CUTS is in the write mode, parallel data on DOØ-7 is serialized in the UART and applied to a synchronizer in the NRZ format. The synchronizer in turn establishes the time at which the bit cell from the UART starts. The digital-to-audio converter converts the data bit levels into corresponding audio signals. These signals are then fed through a driver to the audio output jacks.

In the read mode, inputs from the recorders are mixed and amplified, with an AGC circuit operating on the second stage. Following amplification the audio signals are converted into digital signals, the transitions of which are detected and converted into the NRZ format. NRZ data is applied to the UART which performs the required serial-to-parallel conversion and supplies the parallel data to the DI bus drivers.

5.3 THEORY OF OPERATION

Refer to CUTS schematic in Section VI.

5.3.1 Timing

All timing for the CUTS module is derived from, or related to, the 2 MHz Ø2 clock from the computer. As can be seen on the schematic, Ø2 is received on pin 24 of the S-100 bus by a hysteresis receiver, U21. The inverted Ø2 directly clocks both sections of U20 as well as U12. One half of U20 (clock pin 12) serves as the wait state generator; the other half generates the $\overline{\text{DRIVER ENABLE}}$ signal.

U12, preset to count 3, divides Ø2 by 13 to produce a 153.85 KHz signal on pin 11. The output of U12 is in turn counted down in

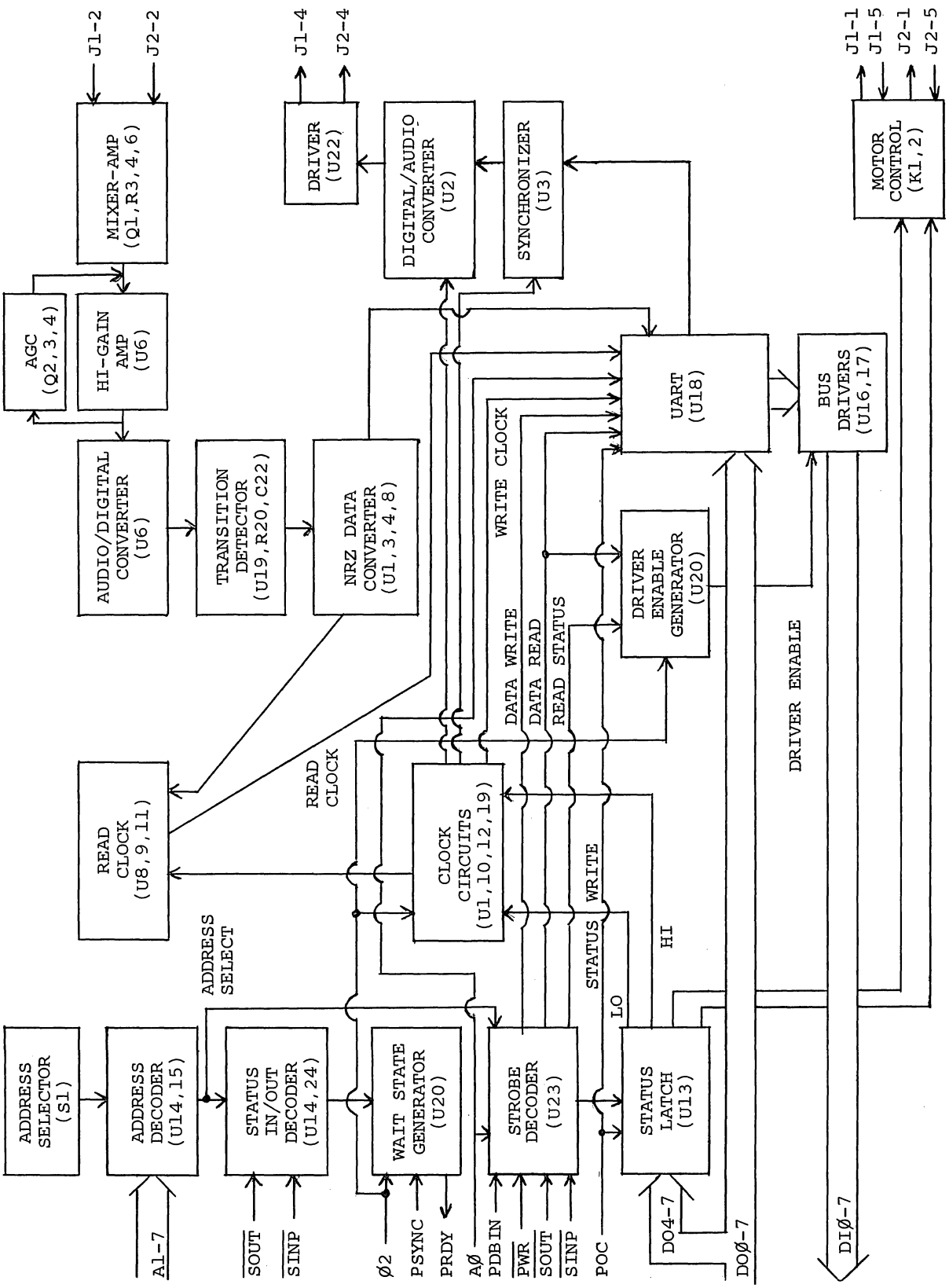


Figure 5-1. CUTS, simplified block diagram.

U10, a seven-stage binary counter, to provide 38.4 KHz on Q2, 19.2 KHz on Q3, 4800 Hz on Q5, 2400 Hz on Q6 and 1200 Hz on Q7. The clocks on Q6 and Q7 are used in the write data synchronizer (U3) and and the digital-to-audio converter (U2).

The remaining outputs from U10 are fed to two sections of U9, a quad multiplexer or select gate. All four sections of U9 are used to select clocks for low speed or high speed operation according to the select inputs, pins 9 (a) and 14 (B). The states of these two select inputs must be complementary to each other in order to select the high or low speed clocks. Specifically, A must be high and B low to select high speed clocks; the converse condition selects low speed clocks. The select inputs are supplied by the complementary outputs of one section in U13, the status latch.

The output of the second section of U9 is WRITE CLOCK, 4800 Hz on low speed and 19.2 KHz on high speed. The third section outputs a 19.2 KHz (high speed) or 38.4 KHz (low speed) timing signal to U8 in the NRZ data conversion circuit.

READ CLOCK is produced by U11 (a phase locked loop), U8 (a binary counter) and the remaining two sections in U9. The signal input (pin 14) to U11 is supplied from pin 1 of U3 in the NRZ data conversion circuit. It is a constant frequency, regardless of whether one or two transitions are detected in the read data during the count out time (12 counts) of the counter (U8) in the NRZ conversion circuit. A phase comparator in U11 compares the signal input to the output of a voltage controlled oscillator (VCO) in U11 (pin 4). By feeding the VCO output through a counter (the other half of U8) before feeding the counter output back to the compare input (pin 3) of U11, the circuit acts as a frequency multiplier. The output of this circuit remains locked, therefore, to a multiple of the signal input on pin 14 of U11.

The output of U11 is nominally 19.2 KHz. Remember that the actual output is determined by the signal input which in turn is a function of tape speed. In other words, the phase lock loop circuit tracks input frequency variations. And it will track such variations within its locking range which is determined by the setting of VR1 (connected to pin 12 of U11).

On high speed, the divide by four output of U8 (pin 12) is selected as RECEIVE CLOCK. The VCO output of U11 is selected for the low speed RECEIVE CLOCK.

5.3.2 Control

Basically the wait state generator (½ of U20), address selector and decoder (S1, U14 and U15), strobe decoder (U23), driver enable generator (½ of U20), the status latch (U13), the status in/out decoder (U14 and 24), motor control (K1 and 2), and power on clear (U21) comprise the CUTS control circuitry.

The address selector and decoder consists of seven open collector exclusive-OR gates, the inputs of which are connected to A1-7, RX1 and S1. RX1 and S1 function as the selector which is configured to reflect the complement of the module address. That is, a response to a high on an address line is generated by the applicable gate by grounding the other input by closing the appropriate DIP switch position. When the decoder senses an address match, all the gates respond true and RX2-4 pulls the outputs up to a high level CARD SELECT signal.

CARD SELECT enables the output gate (U21) in the status in/out decoder. This gate is satisfied if, and only if, SOUT or SINP is active to indicate either an input or output operation is under way. The output (pin 6) of U21 enables the PRDY line driver.

The input to this driver is provided on pin 10 of U20, the wait state generator which is clocked by Ø2 and reset by PSYNC. Thus, pin 10 of U20 goes high on the falling edge of Ø2 after PSYNC. This is the time during which the processor tests for wait requests. The purpose of this half of U20, therefore, is to insert one wait state into every input or output request by the processor. This is required to lengthen the data strobes to durations required by the UART.

U23, the strobe decoder, decodes SINP, PDBIN, SOUT, $\overline{\text{PWR}}$ and AØ to produce $\overline{\text{STATUS WRITE}}$, $\overline{\text{READ STATUS}}$, $\overline{\text{DATA READ STROBE}}$, and $\overline{\text{DATA WRITE STROBE}}$. The truth table for U23 is provided in Table 5-1 on Page V-6. All outputs from U23 are low active.

$\overline{\text{READ STATUS}}$ is applied to the J and $\overline{\text{K}}$ inputs to the other half of U20 which is clocked by Ø2. Thus, an active $\overline{\text{READ STATUS}}$ signal produces a $\overline{\text{DRIVER ENABLE}}$ which is delayed from the strobe by one-half a Ø2 cycle. This signal enables the tri-state buffers (U16 and 17) to place data on the DI bus. Note that a $\overline{\text{DATA READ STROBE}}$ resets U20 to immediately enable the DI bus buffers.

The status latch, U13, latches data present on DO4-7. (Note that the data on DO4 is not used.) Data is loaded into U13 when the strobe decoder outputs a $\overline{\text{STATUS WRITE STROBE}}$. Four output bits from this latch select data rate and control the tape recorders. A low on pin 14 energizes K2 to turn recorder #1 on; a high on this pin de-energizes K2 to turn recorder #1 off. The output on pin 11 of U13 does the same thing for K1 which controls recorder #2. (D1 and D2, which shunt K2 and K1 respectively, prevent damage to the logic circuitry due to inductive kickback.) The remaining two outputs from U13, the complementary outputs associated with DO5, select either low or high speed operation by selecting the appropriate clocks out of U9. Low speed is selected when pins 3 and 2 of U13 are high and low respectively. When the converse relationship exists, high speed is selected.

Table 5-1. Strobe Decoder (U23) Truth Table.

INPUTS						ACTIVE OUTPUT (Low)
AØ*	CARD SELECT	PDBIN*	SINP*	$\overline{PWR}$*	SOUT*	
L	H	H	H	-	-	$\overline{\text{READ STATUS}}$
H	H	H	H	-	-	$\overline{\text{DATA READ STROBE}}$
L	H	-	-	L	H	$\overline{\text{STATUS WRITE STROBE}}$
H	H	-	-	L	H	$\overline{\text{DATA WRITE STROBE}}$
*Inputs to CUTS module.						

The remaining control circuit, POC (power on clear), initializes the CUTS whenever power is applied. When power is applied, $\overline{POC}$ on S-100 bus pin 99 goes low. $\overline{POC}$ is inverted in one section of U21 to clear the logic in the UART (U18). In addition, the inverted $\overline{POC}$ is again inverted in one section of U24 to clear the status register, U13. This clear sets both motor control outputs as well as the high speed select bit high.

5.3.3 Write Mode

When the CUTS is in the write mode, data is input to the UART (U18) under control of the $\overline{\text{DATA WRITE STROBE}}$ signal from U23. Upon completion of this strobe, the transmit sequence is initiated within the UART, with the transmission rate being governed by WRITE CLOCK.

The transmission sequence begins with a start bit, a low (data zero) on the UART's TO output. It is followed by eight data bits and two stop bits, with the number of bits being fixed by the connections to pins 34 through 39 of U18. This data stream is called NRZ data (non-return to zero) because the data never returns to zero until the next bit cell.

NRZ data from U18 is applied to the D input of U3, a D-type flip-flop which is clocked at 1200 Hz. Consequently, the output on pin 13 of U3 follows the input data on pin 9 after the rising edge of the 1200 Hz clock. This output is connected to the reset (pin 12) of U2, so when the data out of the UART is high, the first section in U2 is forced to a reset condition. In this condition the J and K inputs to the second stage of U2 are held high which allows the flip-flop to change state on the rising edge of the clock.

The clock for U2 is 2400 Hz in the high speed mode or 4800 Hz in the low speed mode. This clock is derived from the 2400 Hz output of U10 in conjunction with the low speed select signal NAND gate U1 and exclusive-OR gate U19.

In the high speed mode, pins 4 and 5 of U1 are held low, thus holding pin 6 of U1 high. As a result the 2400 Hz signal is inverted in U1l9 to become the clock for U2.

Pins 4 and 5 of U1 are held high, however, in the low speed mode to enable U1. In this case R19 and C20 provide a delay in the U1 gate. When the 2400 Hz signal on pin 9 of U19 changes state, so does pin 10 of U19. Also, C20 charges through R19 for several hundred nanoseconds, at which point pin 6 of U1 is brought to the opposite polarity. The output from U19 then goes high. A series of positive pulses, with a pulse width approximately equal to the R19, C20 time constant and occuring at every transition of the 2400 Hz signal, appears on pin 10 of U19. This circuit thus operates as a frequency doubler in the low speed mode to provide a 4800 Hz clock for U2.

The 2400 Hz signal from which the U2 clocks are derived also produces the 1200 Hz clock signal for U3 by toggling the flip-flop in U10. As a result the 1200 Hz signal changes state following a propagation delay after the 2400 Hz signal falls.

As previously stated, the second stage of U2 is allowed to change state on the positive going transitions of the U2 clock as long as the data out of the synchronizer is a "1". The end result is an output on pin 2 of U2 that is one-half the clock frequency (1200 Hz and 2400 Hz in the high and low speed modes respectively).

Assume the data stream out of the UART goes low ("0"). On the next rising edge of the 1200 Hz signal, U3 will reset with Q low and $\overline{Q}$ high. A low reset on pin 12 of U2 enables the first U2 stage to toggle on the next rising edge of the U2 clock which occurs 1/2400 second after the synchronizer output falls. Remember that the U2 clock moves from a low to a high shortly before the 1200 Hz signal did. The reset on pin 12 of U2 is thus removed slightly after the U2 clock occurred. With the J and K inputs to the first U2 stage high, its output will change state on each succeeding low to high transition of U2 clock. The second U2 stage in turn can only toggle on the positive going transition of U2 clock when its J and K inputs are high. Since the inputs are high at one-half the clock rate, by virtue of the first U2 stage, the second U2 stage toggles at one-fourth the clock rate.

The two sections of U2, therefore, operate as a frequency divider, dividing the clock by two when the write data is a "1" and by four when the data is a "0". Thus, in the low speed mode, four cycles of the 1200 Hz represent a "0" and eight cycles of 2400 Hz represent a "1". In the high speed mode, one cycle of

1200 Hz represents a "1" and one-half cycle of 600 Hz represents a "0".

The output on pin 2 of U2 is applied to one section in U22 which provides sufficient current drive for the R15,16 and 17 divider network. This divider and a jumper arrangement allow selecting one of three outputs to be fed to the audio output jack *J1-4 and J2-4). The A-to-D jumper selects a 4-volt peak-to-peak square wave output for a digital recorder; the A-to-B jumper selects a 270 mv signal for the auxiliary input to an audio recorder; the A-to-C jumper selects a 50 mv signal for the microphone input to an audio recorder.

5.3.4 Read Mode

When CUTS is in the read mode, data from the recorders enters on J1-2 and J2-2. These two inputs are mixed through a resistive mixer (R3,4 and 6) and fed to Q1, an emitter follower, the output of which is applied to the negative input (pin 2) of operational amplifier U6.

The first section of U6 is a high gain amplifier, with its gain being determined by R9 and R10. The output from this amplifier is coupled to the input (pin 6) of the following U6 stage and the base of a Darlington pair (Q3 and 4) which provides high current gain.

Current into the base of Q3 causes C29 to discharge. (C29 charges through R25 to 5 V dc.) The voltage on C29 in turn controls the gate of FET (field effect transistor) Q2. Q2 functions as a variable resistor which can be changed by its gate voltage. Since Q2 is connected between ground and the input network to the first U6 stage, it serves as a variable shunt. A low gate voltage on Q2 decreases the shunt resistance and the input to U6. In a like manner, a high voltage on C29 results in an increased input to U6. Q2, 3 and 4 with their associated circuitry, therefore, serve as an AGC circuit which limits the input to the second U6 stage to approximately a 2 volt peak signal.

The second stage of U6 performs the needed audio to digital conversion. Feedback resistor R12, in conjunction with R13, establishes the level on the positive input (pin 5) of U6. This level, be it positive or negative, is the threshold which the negative input (pin 6) must exceed in order for the output of U6 to switch levels, positive to negative and the converse. Since the feedback loop is regenerative, U6 switches at its maximum rate, and U6 switches on each transition of the audio signal input. It is in this manner that U6 performs the audio to digital conversion.

The digital output of U6 is inverted in one section of U22 and applied to pin 2 of U19, an exclusive-OR gate which is connected as a buffer without inversion. If the output of U22 is low, the

output on pin 3 of U19 is also low and the output on pin 11 of U19 is high. The voltage across C22 under this condition is minimal. When the output of U22 goes high, C22 starts to charge through R20 until pin 2 of U19 crosses the threshold of that gate. At this point pin 3 of U19 goes high, and since the two inputs to the second exclusive-OR gate are both high, pin 11 of U19 goes low. C22 now discharges because pins 2 and 3 of U19 are at the same level so that the circuit can repeat the operation on the next high to low transition at pin 4 of U22. R20, C22 and U19 consequently serve as a transition detector that produces a pulse less than one microsecond long for each transition of the output on pin 4 of U22, regardless of the polarity of the transition.

Transition pulses from U19 clock ½ of U3 and ½ of U4, both of which are D-type flip-flops. A transition pulse clocks U3 to set Q high and $\overline{Q}$ low to enable a binary counter, U8. The Q output of U3 is applied to pin 5 of U4 and the circuit remains in this state until one of two things occurs: 1) a second transition pulse arrives before U8 reaches count 12 or 2) U8 reaches count 12.

If a second transition pulse arrives before count 12, the first U4 stage is set and presents a "1" to pin 9 of U4. This is clocked by the reset of U3 as a low to pin 12 of U4.

If a transition pulse does not arrive before count 12, the first U4 stage presents a "0" to pin 9 of U4. On count 12, the C and D outputs of U8 go high to reset U3 through U1. As a result the U4 second stage clock goes high, as does pin 12 of U4. The output on pin 12 of U4, in the NRZ format, is inverted by U22 and applied to the receive input of the UART.

The Q output of U3, which occurs at the actual bit rate of the incoming data, is also used by the receive clock circuitry to reconstruct the receive clock from the data signal.

Received data undergoes serial-to-parallel conversion in the UART and placed on the RO1-8 data outputs of the UART WHEN ROD (pin 4 of the UART) is low. The received data is then gated through U16 and 17 to the DI bus.

Four status outputs from the UART can also be enabled when SFD (pin 16) is low. These four bits are FE (framing error), OE (overrun error), DR (data ready) and TBRE (transmitter buffer register empty). They are also gated through U16 and 17 to DI3,4,6 and 7 respectively by a delayed $\overline{\text{READ STATUS}}$ signal.

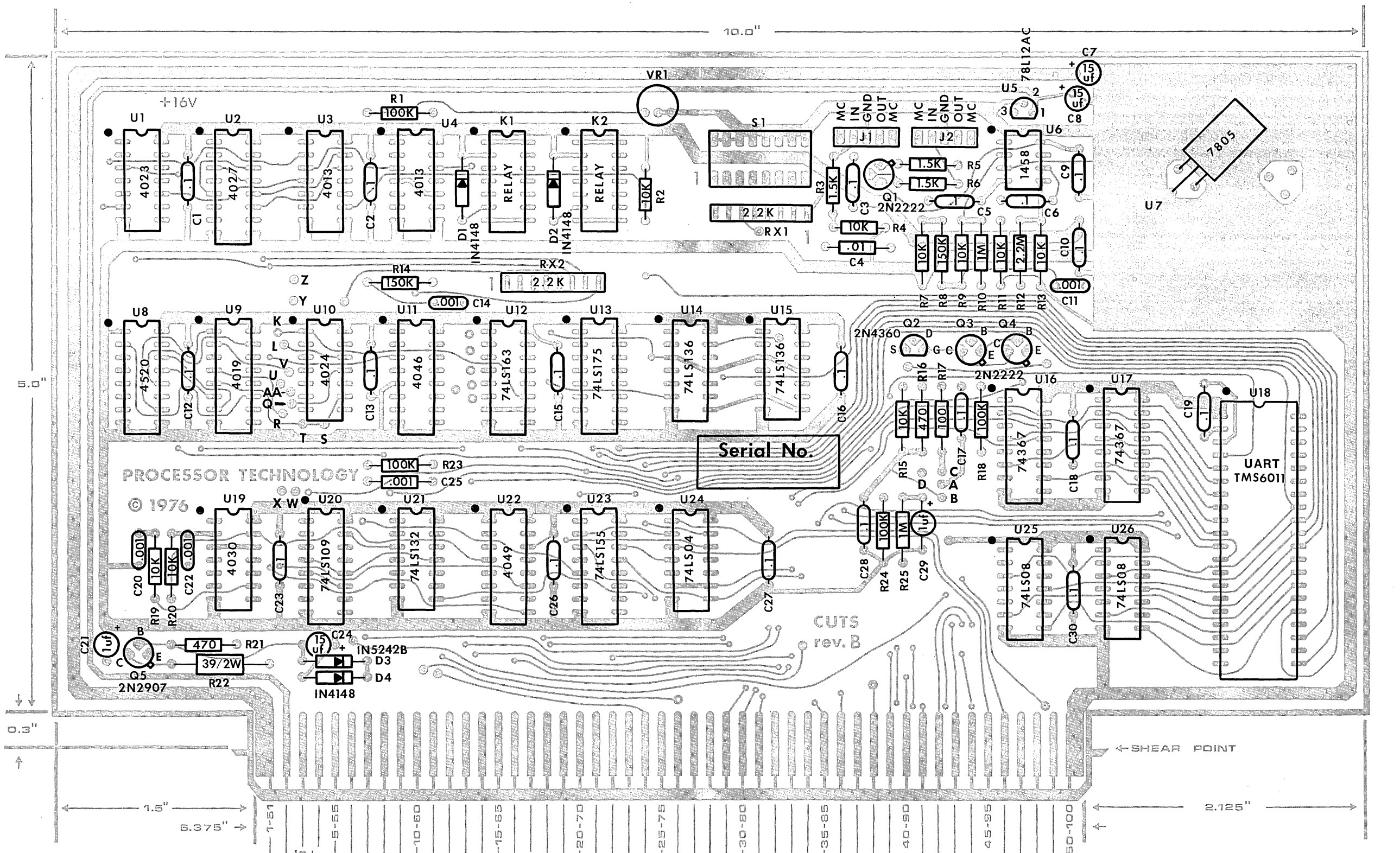
SECTION VI

DRAWINGS

CUTS, COMPUTER USERS TAPE SYSTEM

Processor Technology

Processor Technology Corporation
6200 Hollis Street
Emeryville CA 94608



COMPONENT WIRING		
+8	+8	1-51
+16	+16	
XRDY	SSW DSB	
VI0	EXT CLR	5-55
VI1	RTC	
VI2	STSTB	
VI3	DIG1	
VI4	FRDY	
VI5		10-60
VI6		
VI7		
XRDY2		
		15-65
	PHANTOM	
STA DSB	MWRT	
C/C DSB	PS	20-70
UNPROC	PROC	
SS	RUN	
ADD DSB	PRDY	
DO DSB	PINT	
ø2	CLK - PHOLD	25-75
ø1	CLK - PRESET	
PHLDA	PSYNC	
PWAIT	PWR	
PINTE	PDBIN	
A5	A0	30-80
A4	A1	
A3	A2	
A15	A6	
A12	A7	
A9	A8	35-85
DO 1	A13	
DO 0	A14	
A10	A11	
DO 4	DO 2	
DO 5	DO 3	40-90
DO 6	DO 7	
DI 2	DI 4	
DI 3	DI 5	
DI 7	DI 6	
SMI	DI 1	45-95
SOUT	DI 0	
SINP	SINTA	
SMER	SWO	
SHLTA	SSTACK	
CLOCK	POC	
GND	GND	50-100

DESIGNED BY: RMM
DATE: 9 21 76

LAYOUT BY: JD
DATE: 10 7 76

REVISION: B RM
DATE: 11 15 76

Processor Technology Corporation
6200 Hollis Street (415)652-8080
Emeryville, Ca 94608

STANDARD CARD OUTLINE

Title: **CUTS** Rev: B
Side: BOTH Component
Assembly

NOTES:
1. 16 I/O CONNECTOR
2. 16 S-100 CONNECTION
3. 16 S-100 CONNECTION

J1 AUDIO IN
J2 AUDIO IN
DATA

HIGH SPEED = 19.2 KHZ
LOW SPEED = 38.4 KHZ

COUNTER
1/2 4520

UART
TM5601I

DATA READ STROBE
RECOVERED READ CLOCK
WRITE CLOCK
HIGH SPEED = 1920 HZ
LOW SPEED = 4800 HZ
DRIVER ENABLE
DATA WRITE STROBE
NRS DATA OUT
SYNCHRONIZED DATA

STATUS LATCH
CARD SELECT
READ STATUS
DIP SWITCH
HIGH WHEN CARD IS ADDRESSED

153.85 KHZ
HS = 1200
LS = 2400
A = HSPEED
B = LSPEED
H1 = 1200
2400 HZ
H1 = 300
1200 HZ
PLL DIVIDER/COUNTER

BT97 OR 74367

+5V REG.
+12V REG.
-12V REG.
C1,2,10,12,13,15,16 C18,23,26,27 C30
C9
C21 1µF TANT
C5,6,19 0.1
C7 15µF TANT
C8 15µF TANT
C24 15µF TANT
Q5 2N2907
D3 12V ZENER IN5242B
D4 IN4148
R22 39/2W
R21 470

C17 0.1 DISC
C3 0.1 DISC
R15 10K
R16 470
R17 100
C28 0.1
(250 MV)
(50 MV)

95	DI Ø
94	DI 1
41	DI 2
42	DI 3
91	DI 4
92	DI 5
93	DI 6
43	DI 7
51	+8V
2	+16V
52	-16V
4	J2 AUDIO OUT
4	J1 AUDIO OUT
50	GROUND
100	GROUND
72	PRDY
1	J1 TAPE TRANSPORT 1
5	J1 TAPE TRANSPORT 1 RETURN
1	J2 TAPE TRANSPORT 2
5	J2 TAPE TRANSPORT 2 RETURN

DO Ø	36	A Ø	79
DO 1	37	PDBIN	78
DO 2	88	SOUT	45
DO 3	89	PWR	77
DO 4	38	A1	80
DO 5	39	A2	81
DO 6	40	A3	31
DO 7	90	A4	30
PDI	98	A5	29
SINP	46	A6	82
		A7	83
		Ø2	24
		PSYNC	76

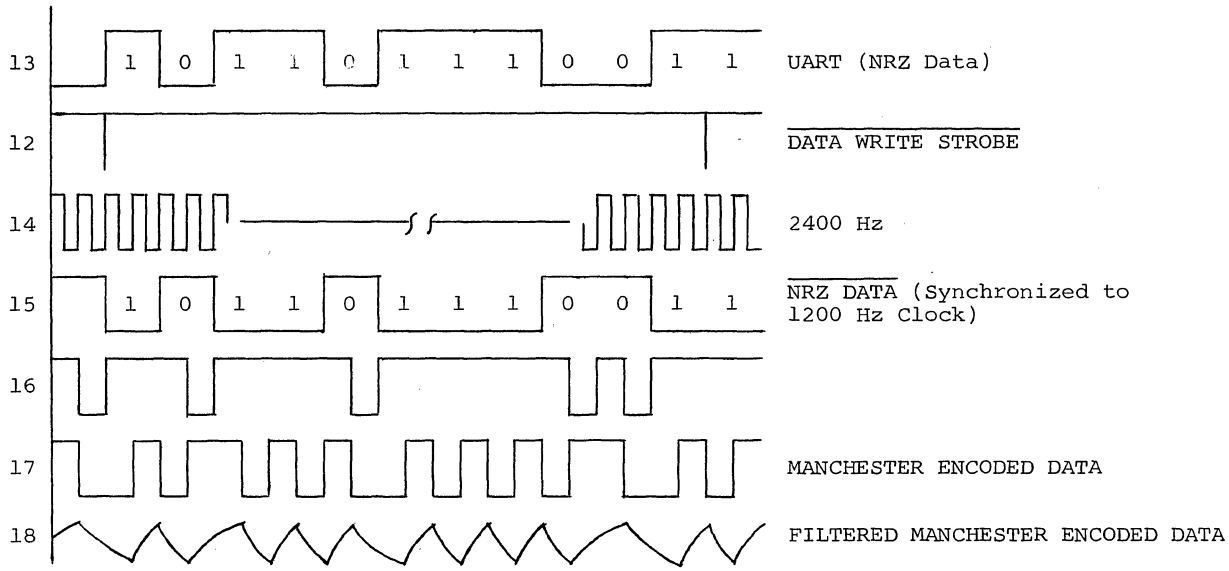
SCHEMATIC, S-100 CUTS

SCALE:	APPROVED BY: R. MARSH	DRAWN BY LITO
DATE: 9-21-76		REVISED 02-3-77

PROCESSOR TECHNOLOGY

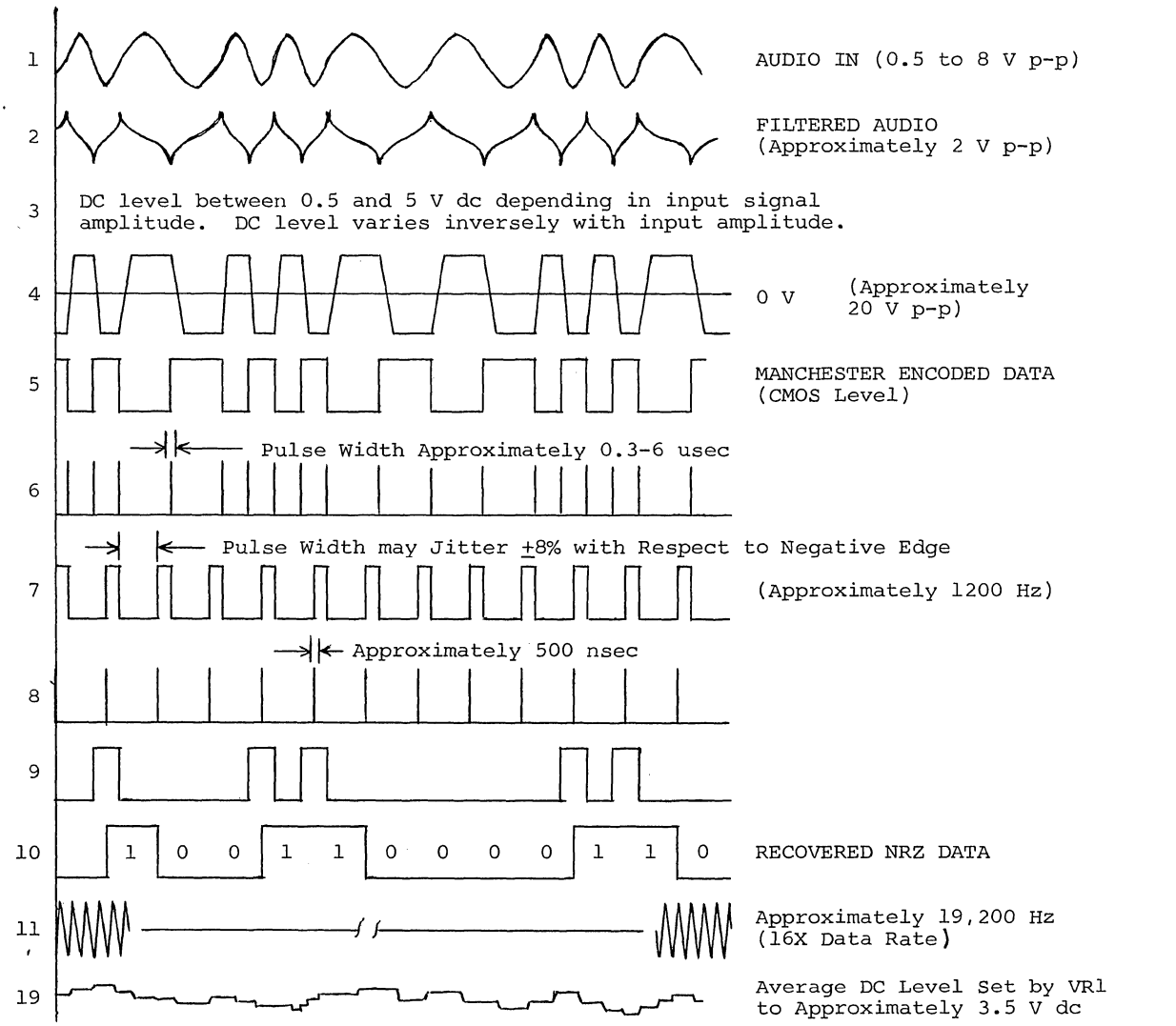
Rev. B | DRAWING NUMBER

CUTS TIMING, WRITE MODE (1200 Baud Operation)



NOTE: 1200 Baud NRZ data (13) is not necessarily synchronized with 1200 Hz clock. Signal at 15 and its complement on pin 12 of U3 are.

CUTS TIMING, READ MODE (1200 Baud Operation)



APPENDICES

Processor Technology Corporation
6200 Hollis Street
Emeryville CA 94608

Warranty

PROCESSOR TECHNOLOGY CORPORATION, in recognition of its responsibility to provide quality components and adequate instruction for their proper assembly, warrants its products as follows:

All components sold by **Processor Technology Corporation** are purchased through normal factory distribution and any part which fails because of defects in workmanship or material will be replaced at no charge for a period of 3 months for kits, and one year for assembled modules, following the date of purchase. The defective part must be returned postpaid to **Processor Technology Corporation** within the warranty period.

Any malfunctioning module, purchased as a kit directly from **Processor Technology** and returned to the factory within the three-month warranty period, which in the judgement of **PTC** has been assembled with care and not subjected to electrical or mechanical abuse, will be restored to proper operating condition and returned, regardless of cause of malfunction, without charge. Kits purchased from authorized **PTC** dealers should be returned to the selling dealer for the same warranty service.

Any modules purchased as a kit and returned to **PTC,** which in the judgement of **PTC** are not covered by the above conditions, will be repaired and returned at a cost commensurate with the work required. In any case, this charge will not exceed $20.00 without prior notification and approval of the owner.

Any modules, purchased as assembled units are guaranteed to meet specifications in effect at the time of manufacture for a period of at least one year following purchase. These modules are additionally guaranteed against defects in materials or workmanship for the same one year period. All warranted factory assembled units returned to **PTCO** postpaid will be repaired and returned without charge.

This warranty is made in lieu of all other warranties expressed or implied and is limited in any case to the repair or replacement of the module involved.

00	NOP		28	---		50	MOV	D,B	78	MOV	A,B	A0	ANA	B	C8	RZ		F0	RP				
01	LXI	B,D16	29	DAD	H	51	MOV	D,C	79	MOV	A,C	A1	ANA	C	C9	RET		F1	POP	PSW			
02	STAX	B	2A	LHLD	Adr	52	MOV	D,D	7A	MOV	A,D	A2	ANA	D	CA	JZ		F2	JP	Adr			
03	INX	B	2B	DCX	H	53	MOV	D,E	7B	MOV	A,E	A3	ANA	E	CB	---		F3	DI				
04	INR	B	2C	INR	L	54	MOV	D,H	7C	MOV	A,H	A4	ANA	H	CC	CZ	Adr	F4	CP	Adr			
05	DCR	B	2D	DCR	L	55	MOV	D,L	7D	MOV	A,L	A5	ANA	L	CD	CALL	Adr	F5	PUSH	PSW			
06	MVI	B,D8	2E	MVI	L,D8	56	MOV	D,M	7E	MOV	A,M	A6	ANA	M	CE	ACI	D8	F6	ORI	D8			
07	RLC		2F	CMA		57	MOV	D,A	7F	MOV	A,A	A7	ANA	A	CF	RST	1	F7	RST	6			
08	---		30	---		58	MOV	E,B	80	ADD	B	A8	XRA	B	D0	RNC		F8	RM				
09	DAD	B	31	LXI	SP,D16	59	MOV	E,C	81	ADD	C	A9	XRA	C	D1	POP	D	F9	SPHL				
0A	LDAX	B	32	STA	Adr	5A	MOV	E,D	82	ADD	D	AA	XRA	D	D2	JNC	Adr	FA	JM	Adr			
0B	DCX	B	33	INX	SP	5B	MOV	E,E	83	ADD	E	AB	XRA	E	D3	OUT	D8	FB	EI				
0C	INR	C	34	INR	M	5C	MOV	E,H	84	ADD	H	AC	XRA	H	D4	CNC	Adr	FC	CM	Adr			
0D	DCR	C	35	DCR	M	5D	MOV	E,L	85	ADD	L	AD	XRA	L	D5	PUSH	D	FD	---				
0E	MVI	C,D8	36	MVI	M,D8	5E	MOV	E,M	86	ADD	M	AE	XRA	M	D6	SUI	D8	FE	CPI	D8			
0F	RRC		37	STC		5F	MOV	E,A	87	ADD	A	AF	XRA	A	D7	RST	2	FF	RST	7			
10	---		38	---		60	MOV	H,B	88	ADC	B	B0	ORA	B	D8	RC							
11	LXI	D,D16	39	DAD	SP	61	MOV	H,C	89	ADC	C	B1	ORA	C	D9	---							
12	STAX	D	3A	LDA	Adr	62	MOV	H,D	8A	ADC	D	B2	ORA	D	DA	JC	Adr						
13	INX	D	3B	DCX	SP	63	MOV	H,E	8B	ADC	E	B3	ORA	E	DB	IN	D8						
14	INR	D	3C	INR	A	64	MOV	H,H	8C	ADC	H	B4	ORA	H	DC	CC	Adr						
15	DCR	D	3D	DCR	A	65	MOV	H,L	8D	ADC	L	B5	ORA	L	DD	---							
16	MVI	D,D8	3E	MVI	A,D8	66	MOV	H,M	8E	ADC	M	B6	ORA	M	DE	SBI	D8						
17	RAL		3F	CMC		67	MOV	H,A	8F	ADC	A	B7	ORA	A	DF	RST	3						
18	---		40	MOV	B,B	68	MOV	L,B	90	SUB	B	B8	CMP	B	E0	RPO							
19	DAD	D	41	MOV	B,C	69	MOV	L,C	91	SUB	C	B9	CMP	C	E1	POP	H						
1A	LDAX	D	42	MOV	B,D	6A	MOV	L,D	92	SUB	D	BA	CMP	D	E2	JPO	Adr						
1B	DCX	D	43	MOV	B,E	6B	MOV	L,E	93	SUB	E	BB	CMP	E	E3	XTHL							
1C	INR	E	44	MOV	B,H	6C	MOV	L,H	94	SUB	H	BC	CMP	H	E4	CPO	Adr						
1D	DCR	E	45	MOV	B,L	6D	MOV	L,L	95	SUB	L	BD	CMP	L	E5	PUSH	H						
1E	MVI	E,D8	46	MOV	B,M	6E	MOV	L,M	96	SUB	M	BE	CMP	M	E6	ANI	D8						
1F	RAR		47	MOV	B,A	6F	MOV	L,A	97	SUB	A	BF	CMP	A	E7	RST	4						
20	---		48	MOV	C,B	70	MOV	M,B	98	SBB	B	C0	RNZ		E8	RPE							
21	LXI	H,D16	49	MOV	C,C	71	MOV	M,C	99	SBB	C	C1	POP	B	E9	PCHL							
22	SHLD	Adr	4A	MOV	C,D	72	MOV	M,D	9A	SBB	D	C2	JNZ	Adr	EA	JPE	Adr						
23	INX	H	4B	MOV	C,E	73	MOV	M,E	9B	SBB	E	C3	JMP	Adr	EB	XCHG							
24	INR	H	4C	MOV	C,H	74	MOV	M,H	9C	SBB	H	C4	CNZ	Adr	EC	CPE	Adr						
25	DCR	H	4D	MOV	C,L	75	MOV	M,L	9D	SBB	L	C5	PUSH	B	ED	---							
26	MVI	H,D8	4E	MOV	C,M	76	HLT		9E	SBB	M	C6	ADI	D8	EE	XRI	D8						
27	DAA		4F	MOV	C,A	77	MOV	M,A	9F	SBB	A	C7	RST	0	EF	RST	5						

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

Adr = 16 bit address

HEX-ASCII TABLE

Non-Printing

00	NULL
07	BELL
09	TAB
0A	LF
0B	VT
0C	FORM
0D	CR
11	X-ON
12	TAPE
13	X-OFF
14	
1B	ESC
7D	ALT MODE
7F	RUB OUT

HEX-ASCII TABLE

Printing		Characters		
30	0	40	@	
31	1	20	space	
32	2	21	!	
33	3	22	"	
34	4	23	#	
35	5	24	$	
36	6	25	%	
37	7	26	&	
38	8	27	'	
39	9	28	(	
		29	)	
41	A	2A	*	
42	B	2B	+	
43	C	2C	,	
44	D	2D	-	
45	E	2E	.	
46	F	2F	/	
47	G	3A	:	
48	H	3B	;	
49	I	3C	<	
4A	J	3D	=	
4B	K	3E	>	
4C	L	3F	?	
4D	M	5B	[	
4E	N	5C	\	
4F	O	5D	]	
50	P	5E	↑	(^)
51	Q	5F	←	(_)
52	R			
53	S			
54	T			
55	U			
56	V			
57	W			
58	X			
59	Y			
5A	Z			

Processor Technology Corporation
6200 Hollis Street
Emeryville CA 94608

JUMP

C3	JMP	Adr
C2	JNZ	
CA	JZ	
D2	JNC	
DA	JC	
E2	JPO	
EA	JPE	
F2	JP	
FA	JM	
E9	PCHL	

CALL

CD	CALL	Adr
C4	CNZ	
CC	CZ	
D4	CNC	
DC	CC	
E4	CPO	
EC	CPE	
F4	CP	
FC	CM	

RETURN

C9	RET	
C0	RNZ	
C8	RZ	
D0	RNC	
D8	RC	
E0	RPO	
E8	RPE	
F0	RP	
F8	RM	

RESTART

C7	RST	0
CF	RST	1
D7	RST	2
DF	RST	3
E7	RST	4
EF	RST	5
F7	RST	6
FF	RST	7

ROTATE†

07	RLC	
0F	RRC	
17	RAL	
1F	RAR	

CONTROL

00	NOP	
76	HLT	
F3	DI	
FB	EI	

MOVE IMMEDIATE

06	MVI	B,	D8
0E	MVI	C,	
16	MVI	D,	
1E	MVI	E,	
26	MVI	H,	
2E	MVI	L,	
36	MVI	M,	
3E	MVI	A,	

Acc IMMEDIATE*

C6	ADI	D8	
CE	ACI		
D6	SUI		
DE	SBI		
E6	ANI		
EE	XRI		
F6	ORI		
FE	CPI		

LOAD IMMEDIATE

01	LXI	B,	D16
11	LXI	D,	
21	LXI	H,	
31	LXI	SP,	

DOUBLE ADD†

09	DAD	B
19	DAD	D
29	DAD	H
39	DAD	SP

STACK OPS

C5	PUSH	B
D5	PUSH	D
E5	PUSH	H
F5	PUSH	PSW
C1	POP	B
D1	POP	D
E1	POP	H
F1	POP	PSW*
E3	XTHL	
F9	SPHL	

SPECIALS

EB	XCHG	
27	DAA*	
2F	CMA	
37	STC†	
3F	CMC†	

INPUT/OUTPUT

D3	OUT	D8
DB	IN	D8

MOVE

40	MOV	B,B
41	MOV	B,C
42	MOV	B,D
43	MOV	B,E
44	MOV	B,H
45	MOV	B,L
46	MOV	B,M
47	MOV	B,A
48	MOV	C,B
49	MOV	C,C
4A	MOV	C,D
4B	MOV	C,E
4C	MOV	C,H
4D	MOV	C,L
4E	MOV	C,M
4F	MOV	C,A
50	MOV	D,B
51	MOV	D,C
52	MOV	D,D
53	MOV	D,E
54	MOV	D,H
55	MOV	D,L
56	MOV	D,M
57	MOV	D,A

MOVE (cont)

58	MOV	E,B
59	MOV	E,C
5A	MOV	E,D
5B	MOV	E,E
5C	MOV	E,H
5D	MOV	E,L
5E	MOV	E,M
5F	MOV	E,A
60	MOV	H,B
61	MOV	H,C
62	MOV	H,D
63	MOV	H,E
64	MOV	H,H
65	MOV	H,L
66	MOV	H,M
67	MOV	H,A
68	MOV	L,B
69	MOV	L,C
6A	MOV	L,D
6B	MOV	L,E
6C	MOV	L,H
6D	MOV	L,L
6E	MOV	L,M
6F	MOV	L,A
70	MOV	M,B
71	MOV	M,C
72	MOV	M,D
73	MOV	M,E
74	MOV	M,H
75	MOV	M,L

77	MOV	M,A
78	MOV	A,B
79	MOV	A,C
7A	MOV	A,D
7B	MOV	A,E
7C	MOV	A,H
7D	MOV	A,L
7E	MOV	A,M
7F	MOV	A,A

ACCUMULATOR*

80	ADD	B
81	ADD	C
82	ADD	D
83	ADD	E
84	ADD	H
85	ADD	L
86	ADD	M
87	ADD	A
88	ADC	B
89	ADC	C
8A	ADC	D
8B	ADC	E
8C	ADC	H
8D	ADC	L
8E	ADC	M
8F	ADC	A
90	SUB	B
91	SUB	C
92	SUB	D
93	SUB	E
94	SUB	H
95	SUB	L
96	SUB	M
97	SUB	A
98	SBB	B
99	SBB	C
9A	SBB	D
9B	SBB	E
9C	SBB	H
9D	SBB	L
9E	SBB	M
9F	SBB	A
A0	ANA	B
A1	ANA	C
A2	ANA	D
A3	ANA	E
A4	ANA	H
A5	ANA	L
A6	ANA	M
A7	ANA	A
A8	XRA	B
A9	XRA	C
AA	XRA	D
AB	XRA	E
AC	XRA	H
AD	XRA	L
AE	XRA	M
AF	XRA	A
B0	ORA	B
B1	ORA	C
B2	ORA	D
B3	ORA	E
B4	ORA	H
B5	ORA	L
B6	ORA	M
B7	ORA	A
B8	CMP	B
B9	CMP	C
BA	CMP	D
BB	CMP	E
BC	CMP	H
BD	CMP	L
BE	CMP	M
BF	CMP	A

INCREMENT**

04	INR	B
0C	INR	C
14	INR	D
1C	INR	E
24	INR	H
2C	INR	L
34	INR	M
3C	INR	A
03	INX	B
13	INX	D
23	INX	H
33	INX	SP

DECREMENT**

05	DCR	B
0D	DCR	C
15	DCR	D
1D	DCR	E
25	DCR	H
2D	DCR	L
35	DCR	M
3D	DCR	A
0B	DCX	B
1B	DCX	D
2B	DCX	H
3B	DCX	SP

LOAD/STORE

0A	LDAX	B
1A	LDAX	D
2A	LHLD	Adr
3A	LDA	Adr
02	STAX	B
12	STAX	D
22	SHLD	Adr
32	STA	Adr

PSEUDO INSTRUCTION

ORG	Adr	
END		
EQU	D16	
DS	D16	
DB	D8	[ ]
DW	D16	[ ]

CONSTANT DEFINITION

0BDH	Hex
1AH	
105D	Decimal
105	
72O	Octal
72Q	
11011B	Binary
00110B	
'TEST'	ASCII
'A' 'B'	

OPERATORS

\+ −

STANDARD SETS

A	SET	7
B	SET	0
C	SET	1
D	SET	2
E	SET	3
H	SET	4
L	SET	5
M	SET	6
SP	SET	6
PSW	SET	6

D8 constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

all Flags (C,Z,S,P) affected

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

† = only CARRY affected

Adr = 16 bit address

** = all Flags except CARRY affected; (exception: INX & DCX affect no Flags)

The electrical value of many types of resistors and capacitors is printed on the component. Other types, however, are identified by color coding which gives all the information needed to correctly identify the component. In most cases color coding conforms with the EIA (Electronic Industries Association) Standard Color Code. In other cases a manufacturer will adapt the standard to fit his particular requirement. Both the Standard Color Code and a code used to identify tantalum dipped capacitors are provided below.

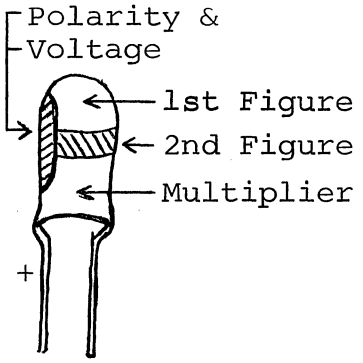
STANDARD COLOR CODE FOR RESISTORS AND CAPACITORS

COLOR	SIGNIFICANT FIGURE	DECIMAL MULTIPLIER	TOLERANCE (%)	VOLTAGE RATING*
Black	0	1		--
Brown	1	10		100
Red	2	100		200
Orange	3	1,000		300
Yellow	4	10,000		400
Green	5	100,000		500
Blue	6	1,000,000		600
Violet	7	10,000,000		700
Gray	8	100,000,000		800
White	9	1,000,000,000		900
Gold	-	0.1	5	1000
Silver	-	0.01	10	2000
None	-	---	20	500

*Applies to capacitors only.

COLOR CODE FOR TANTALUM DIPPED CAPACITORS

Rated Voltage VDC 25°C	Color	CODE FOR CAPACITANCE IN PICOFARADS		
		1st Figure	2nd Figure	Multiplier uuF
3-4	Black	0	0	1
3-6	Brown	1	1	10
3-10	Red	2	2	100
3-15	Orange	3	3	1,000
3-20	Yellow	4	4	10,000
3-25	Green	5	5	100,000
3-35	Blue	6	6	1,000,000
3-50	Violet	7	7	10,000,000
	Gray	8	8	
3	White	9	9	



LOADING DIP (DUAL IN-LINE PACKAGE) DEVICES

Most DIP devices have their leads spread so that they can not be dropped straight into the board. They must be "walked in" using the following procedure:

(1) Orient the device properly. Pin 1 is indicated by a small embossed dot on the top surface of the device at one corner. Pins are numbered counterclockwise from pin 1.

(2) Insert the pins on one side of the device into their holes on the printed circuit card. Do not press the pins all the way in, but stop when they are just starting to emerge from the opposite side of the card.

(3) Exert a sideways pressure on the pins at the other side of the device by pressing against them where they are still wide below the bend. Bring this row of pins into alignment with its holes in the printed circuit card and insert them an equal distance, until they begin to emerge.

(4) Press the device straight down until it seats on the points where the pins widen.

(5) Turn the card over and select two pins at opposite corners of the device. Using a fingernail or a pair of long-nose pliers, push these pins outwards until they are bent at a 45° angle to the surface of the card. This will secure the device until it is soldered.

SOLDERING TIPS

(1) Use a low-wattage iron--25 watts is good. Larger irons run the risk of burning the printed-circuit board. Don't try to use a soldering gun, they are too hot.

(2) Use a small pointed tip and keep it clean. Keep a damp piece of sponge by the iron and wipe the tip on it after each use.

(3) Use 60-40 rosin-core solder ONLY. DO NOT use acid-core solder or externally applied fluxes. Use the smallest diameter solder you can get.

NOTE: DO NOT press the top of the iron on the pad or trace. This will cause the trace to "lift" off of the board which will result in permanent damage.

(4) In soldering, wipe the tip, apply a light coating of new solder to it, and apply the tip to both parts of the joint, that is, both the component lead and the printed-circuit pad. Apply the solder against the lead and pad being heated, but not directly to the tip of the iron. Thus, when the solder

melts the rest of the joint will be hot enough for the solder to "take", (i.e., form a capillary film).

(5) Apply solder for a second or two, then remove the solder and keep the iron tip on the joint. The rosin will bubble out. Allow about three or four bubbles, but don't keep the tip applied for more than ten seconds.

(6) Solder should follow the contours of the original joint. A blob or lump may well be a solder bridge, where enough solder has been built upon one conductor to overflow and "take" on the adjacent conductor. Due to capillary action, these solder bridges look very neat, but they are a constant source of trouble when boards of a high trace density are being soldered. Inspect each integrated circuit and component after soldering for bridges.

(7) To remove solder bridges, it is best to use a vacuum "solder puller" if one is available. If not, the bridge can be reheated with the iron and the excess solder "pulled" with the tip along the printed circuit traces until the lump of solder becomes thin enough to break the bridge. Braid-type solder remover, which causes the solder to "wick up" away from the joint when applied to melted solder, may also be used.

INSTALLING AUGAT PINS

Augat pins are normally supplied on carriers (e.g., 8-pin and 16-pin carriers). In many cases the PC board layout permits Augat pins to be installed while still attached to the carrier or a portion of the carrier. In other cases the pins must be installed singly.

To install two or more pins that are still attached to the carrier, proceed as follows:

NOTE

It is perfectly alright to appropriately cut a carrier to accommodate the installation. For example, an 8-pin carrier can be cut in half (4 pins each) across the short dimension to fit a 4-pin, 4-corner layout. It may also be cut in half along the long dimension to fit a 4-pin, inline layout.

(1) Insert pins in the mounting holes from the front (component) side of board. (The carrier will hold the pins perpendicular to the board.)

(2) Solder all pins from back (solder) side of board so the solder "wicks up" to the front side.

(3) Check for solder bridges.

(4) Remove carrier.

To install single pins, proceed as follows:

(1) Hold board between two objects so that it stands on edge.

(2) Insert pins in the mounting holes from front (component) side of board.

(3) Solder pins from back (solder) side of board so the solder "wicks up" to the front side. (This will hold the pins firmly in place.)

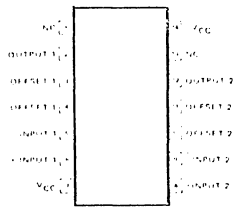
(4) Insert a component lead into one pin and reheat the solder. Using the component lead, adjust pin until it is perpendicular to board. Allow solder to cool while holding the pin as steady as possible. Remove component lead. Repeat this procedure with other pins.

NOTE

If cooled solder is mottled or crystallized, a "cold joint" is indicated, and the solder should be reheated.

(5) Check each installation for cold joints and solder bridges.

1458 or 5558



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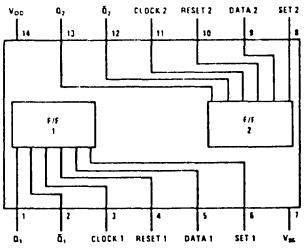

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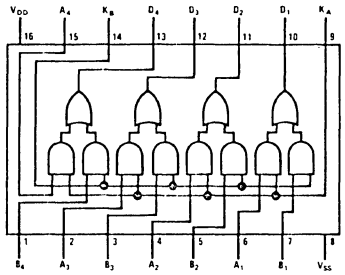

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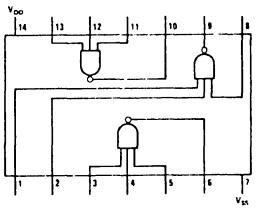

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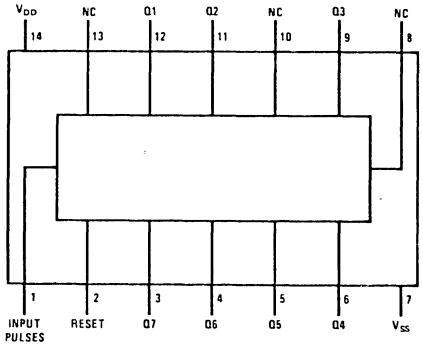

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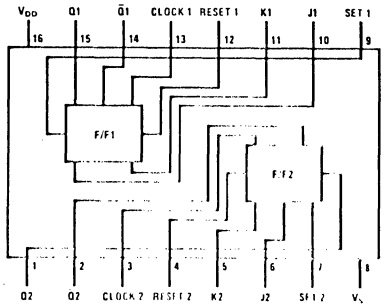

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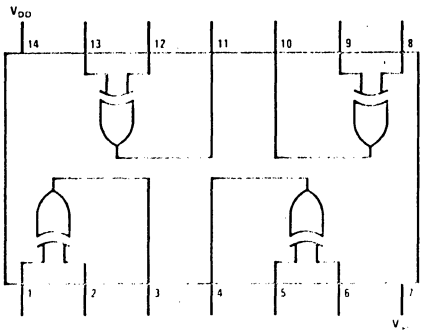

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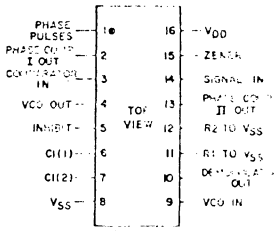

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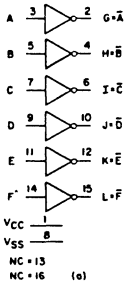

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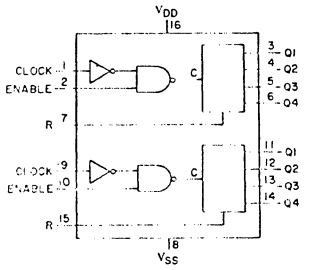

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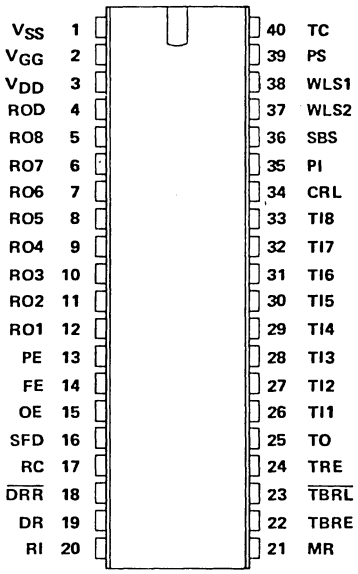

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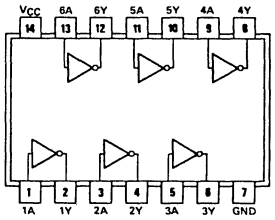

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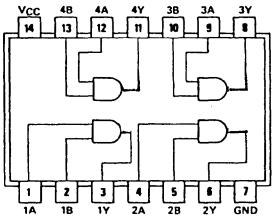

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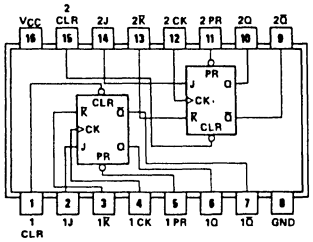

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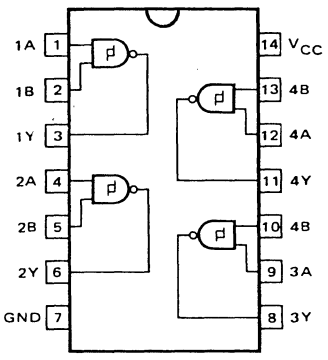

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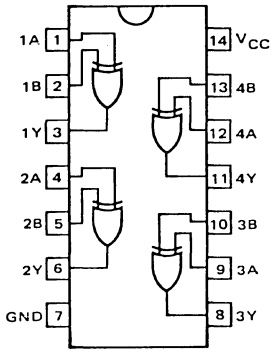

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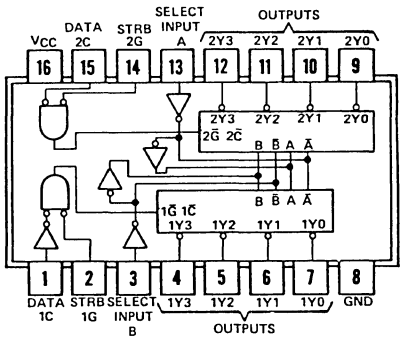

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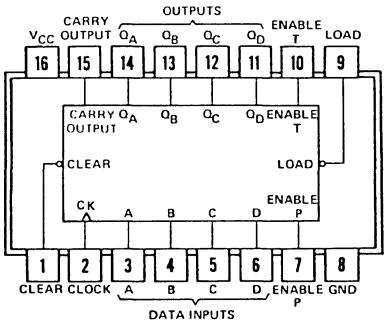

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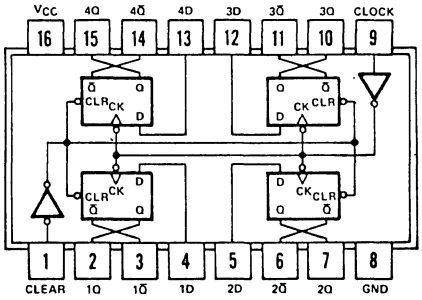

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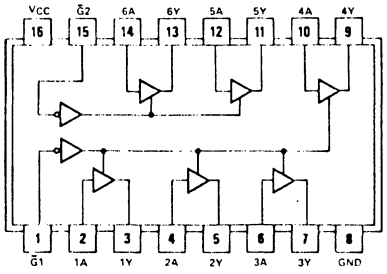


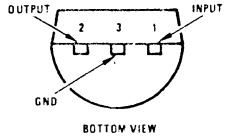
7805UC

P SUFFIX
PLASTIC PACKAGE
CASE 199-04

Pin 1 Input (Base)
Pin 2 Output (Emitter)
Pin 3 Ground (Collector)

Heat sink surface connected to pin 3.

78L12

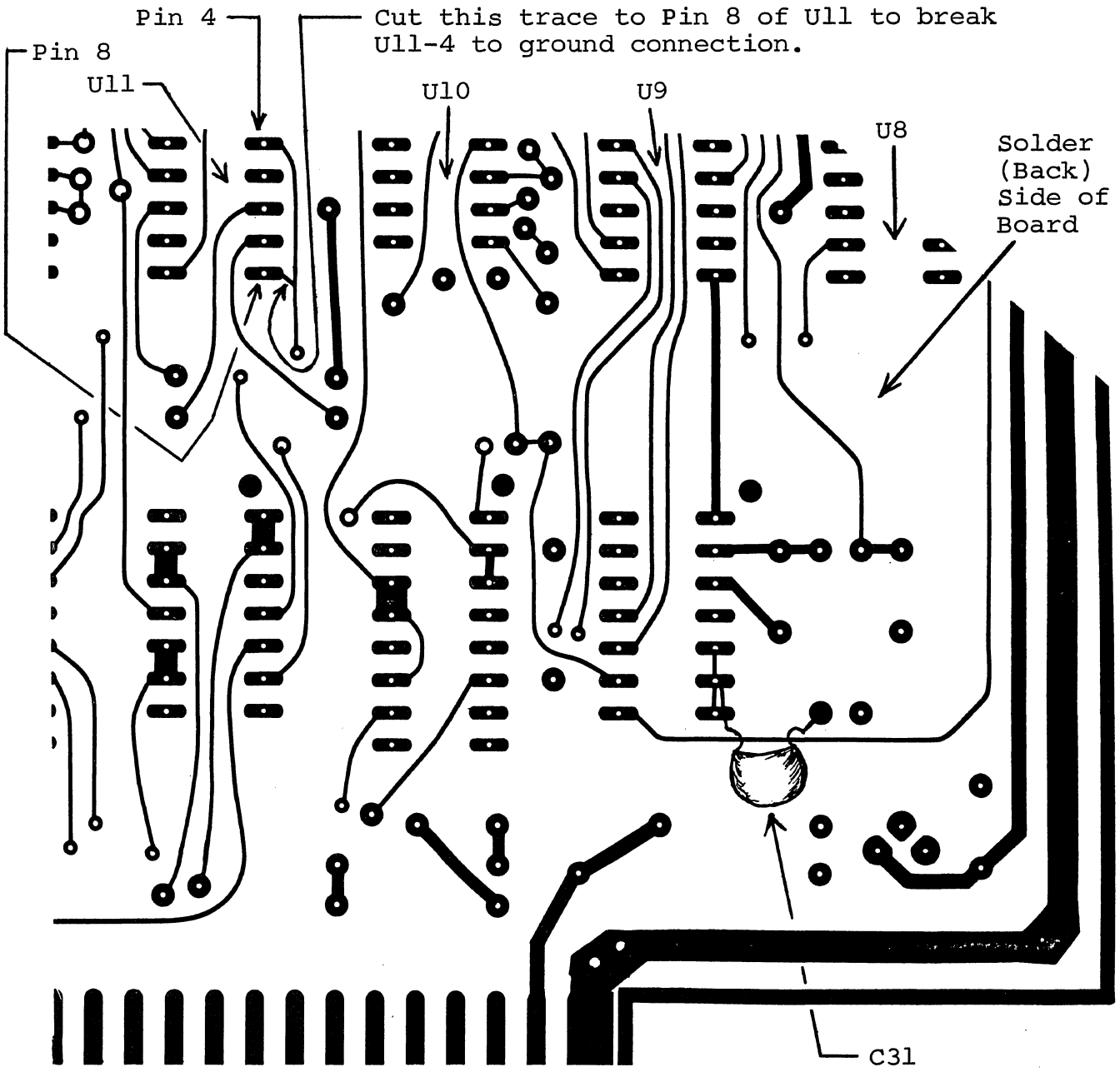


CUTS (Applies only to Rev B and below circuit boards)

Processor Technology

ASSEMBLY PROCEDURE CHANGE NOTICE #2

Rev B and below CUTS circuit boards have an error that was introduced during their manufacture: A trace was connected to pin 8 of U11 which shorts the voltage controlled oscillator (VCO) output on pin 4 of U11 to ground. CORRECT THIS ERROR AS SHOWN BELOW BEFORE YOU CHECK THE BOARD AND START ASSEMBLY.



PROCESSOR TECHNOLOGY CORPORATION 6200 HOLLIS STREET EMERYVILLE CA 94608 (415) 652-8080
CABLE ADDRESS "PROCTEC"

CUTS (Applies only to Rev B and below circuit boards)

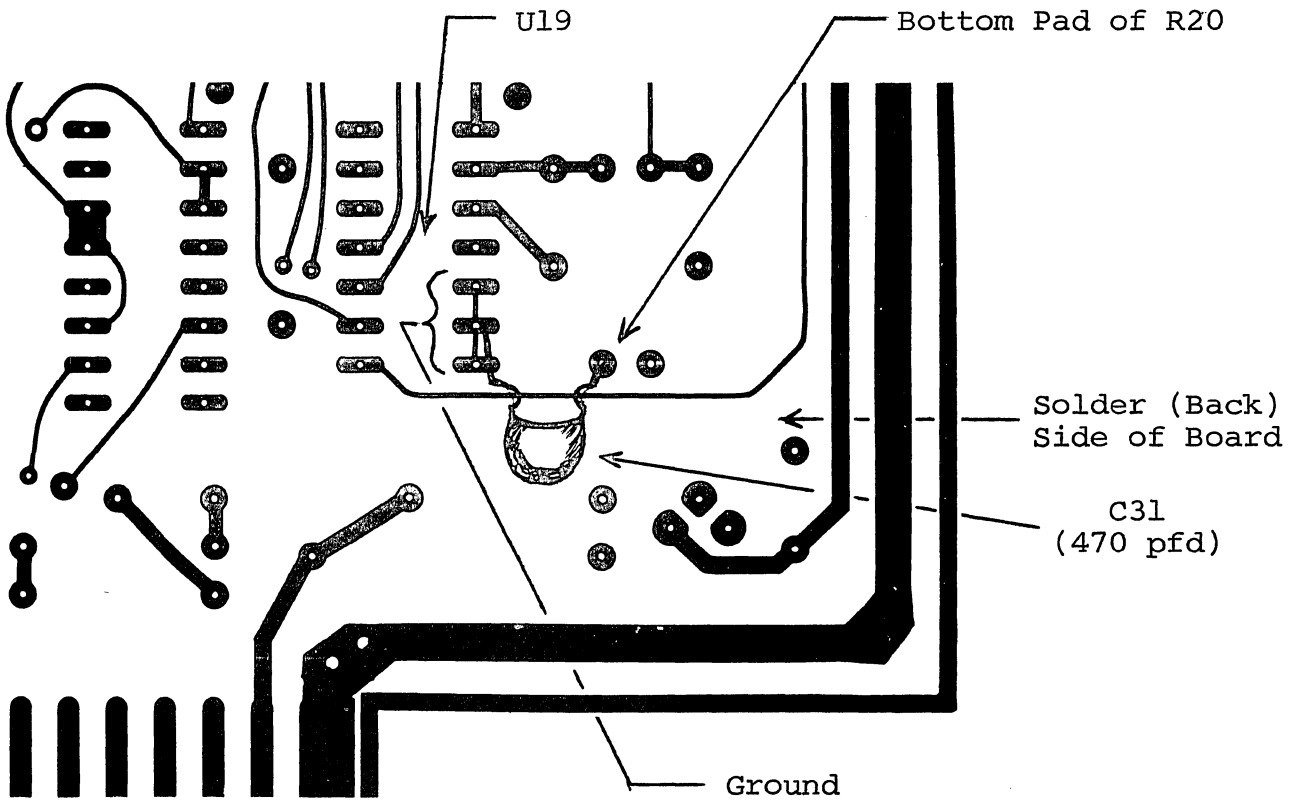
Processor Technology

ASSEMBLY PROCEDURE CHANGE NOTICE #1

Reference Section II, Step 12, Page II-

Capacitor C31 is a new addition to the CUTS circuitry made after the manufacture of Rev B circuit boards.

On Rev B and below boards, install C31 on the solder (back) side of the board as shown below.



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Processor Technology

ERRATA SHEET #1

Reference Step 23 on Page II-17

The sixth paragraph should read as follows:

( ) Measure the DC voltage at pin 9 of U11 and write the measured voltage down. (Call this Voltage A.)

The eighth paragraph should read as follows:

( ) Measure the DC voltage at pin 9 of U11 and write the measured voltage down. (Call this Voltage B.)

MAKE THESE CORRECTIONS IN YOUR MANUAL BEFORE YOU START TO ASSEMBLE YOUR CUTS MODULE.

ES1-3/77

PROCESSOR TECHNOLOGY CORPORATION 6200 HOLLIS STREET EMERYVILLE CA 94608 (415) 652-8080
CABLE ADDRESS "PROCTEC"

PROCESSOR TECHNOLOGY CORP.
6200 HOLLIS STREET
EMERYVILLE, CALIF. 94608

MANUAL DATA
CUTS READ AND WRITE ROUTINES

```
0001 *
0002 *
0003 *
0004 *         TAPE READ AND WRITE ROUTINES FOR CUTS BOARDS
0005 *
0006 *
0007 *   THESE ROUTINES WERE EXTRACTED FROM "SOLOS"TM AND "CUTER"TM
0008 * TO ILLUSTRATE THE REQUIREMENTS OF THE CUTS BOARD FOR
0009 * READING AND WRITING TO THE CASSETTE TAPE.  BOTH SOLOS AND
0010 * CUTER ALSO HAVE FILE BUFFERING ROUTINES TO PROVIDE BYTE
0011 * BY BYTE TRANSFERS TO THE CASSETTE TAPE.
0012 *
0013 *   CUTER resides on cassette tape and is available at your
0014 * local Processor Technology Dealer for $11.00 or ROM
0015 * resident for use on the GPM module.  The CUTER program
0016 * requires 2K of memory plus 1k of RAM work area.  A short
0017 * bootstrap program is used to load CUTER from cassette
0018 * tape.
0019 *
0020 *   CUTER is relocatable to any 256 byte boundary and has a
0021 * built in command processor and support for serial,
0022 * parallel, keyboard and VDM I/O as well as CUTS cassette
0023 * routines.  The CUTER software is necessary for all major
0024 * Processor Technology or Software Technology programs.
0025 *
0026 *       CUTER COMMAND LIST
0027 *
0028 *  DUMP        Dump memory
0029 *  ENTER       Enter to memory
0030 *  EXECUTE     Execute a program
0031 *  TLOAD       Load programs or data from cassette
0032 *  TSAVE       Save programs or data to cassette
0033 *  TXEQ        Load and run program from tape
0034 *  TCAT        List names of files on tape
0035 *  CUST        Enter or delete custom command name
0036 *  SET di      Set display speed
0037 *  SET nu      Set output nulls
0038 *  SET ta      Set tape speed
0039 *  SET in      Set input port  (0-3)
0040 *  SET out     Set output port  (0-3)
0041 *  SET cin     Set custom input driver address
0042 *  SET cout    Set custom output driver address
0043 *  SET xeq     Set auto execute address to header
0044 *  SET type    Set type in header
0045 *
0046 *
0047 *
0048 *
0049 *
0050 *
0051 *                    <<=-   TAPE READ ROUTINES   -=>>
```

MANUAL DATA
CUTS READ AND WRITE ROUTINES

PROCESSOR TECHNOLOGY CORP.
6200 HOLLIS STREET
EMERYVILLE, CALIF. 94608

```
                    0052 *
                    0053 *
                    0054 *      ON ENTRY:     A   - HAS UNIT AND SPEED
                    0055 *                    HL  - POINT TO HEADER BLOCK
                    0056 *                    DE  - HAVE OPTIONAL PUT ADDRESS
                    0057 *
                    0058 *      ON EXIT:      CARRY IS SET IF ERROR OCCURRED
                    0059 *                    DE HAVE SIZE OF BLOCK READ
                    0060 *                    TAPE UNITS ARE OFF
                    0061 *
                    0062 *
0000 D5             0063 RTAPE     PUSH      D           SAVE OPTIONAL ADDRESS
0001 06 03          0064           MVI       B,3         SHORT DELAY
0003 CD 1D 01       0065           CALL      TON
0006 DB FB          0066           IN        TDATA       CLEAR THE UART FLAGS
                    0067 *   LOOP HERE UNTIL VALID HEADER IS FOUND
0008 E5             0068 PTAP1     PUSH      H           HEADER ADDRESS
0009 CD 5F 00       0069           CALL      RHEAD       GO READ HEADER
000C E1             0070           POP       H
000D DA 49 00       0071           JC        TERR        IF AN ERROR OR ESC WAS RECEIVED
0010 C2 08 00       0072           JNZ       PTAP1       IF VALID HEADER NOT FOUND
                    0073 *   FOUND A VALID HEADER NOW DO COMPARE
0013 E5             0074           PUSH      H           GET BACK AND RESAVE ADDRESS
0014 11 2D 01       0075           LXI       D,THEAD
0017 CD 0F 01       0076           CALL      DHCMP       COMPARE DE-HL HEADERS
001A E1             0077           POP       H
001B C2 08 00       0078           JNZ       PTAP1       DIDN T COMPARE...GO BACK TO LOOP
                    0079 *   FOUND IT.. NOW ADJUST REGISTERS FOR READ
001E D1             0080           POP       D           OPTIONAL  PUT" ADDRESS
001F 7A             0081           MOV       A,D
0020 B3             0082           ORA       E           SEE IF DE IS ZERO
0021 2A 34 01       0083           LHLD      BLOCK       GET BLOCK SIZE
0024 EB             0084           XCHG      .            ..TO DE
                    0085 *  DE HAS HBLOCK....HL HAS USER OPTION
0025 C2 2B 00       0086           JNZ       RTAP        IF DE WAS ZERO GET TAPE LOAD ADDRESS
0028 2A 36 01       0087           LHLD      LOADR       GET TAPE LOAD ADDRESS
                    0088 *
                    0089 *
                    0090 *      THIS ROUTINE READS "DE" BYTES FROM THE TAPE
                    0091 *      TO ADDRESS HL.  THE BYTES MUST BE FROM ONE
                    0092 *      CONTIGUOUS PHYSICAL BLOCK ON THE TAPE.
                    0093 *
                    0094 *           HL HAS "PUT" ADDRESS
                    0095 *           DE HAS SIZE OF TAPE BLOCK
                    0096 *
002B D5             0097 RTAP      PUSH      D           SAVE SIZE FOR RETURN TO CALLING PROGRAM
                    0098 *
002C 7A             0099 LOLOOP    MOV       A,D         GET COUNT
002D B3             0100           ORA       E
002E CA 5A 00       0101           JZ        RTOFF       COUNT IS ZERO-TURN OFF TAPE AND RETURN
0031 EB             0102           XCHG                  GET COUNT TO HL
                    0103 *
0032 01 00 FF       0104           LXI       B,-256      THIS MANY PRIOR TO CRC TEST
```

PROCESSOR TECHNOLOGY CORP.
6200 HOLLIS STREET
EMERYVILLE, CALIF. 94608

MANUAL DATA
CUTS READ AND WRITE ROUTINES

```
0035 09              0105          DAD     B          A LITTLE MATH
0036 D2 4E 00        0106          JNC     LBLK       NO CARRY  IT S THE LAST BLOCK
0039 06 00           0107          MVI     B,0        256 TO READ
003B D3 FC           0108          OUT     0FCH       DING THE PORT FOR INSECURE ROBERTS
                     0109 *
003D 0E 00           0110 RDBLK    MVI     C,0        ZERO THE CRC
003F EB              0111          XCHG    .          ROUND ROBIN
                     0112 *
0040 CD 7D 00        0113 RTLOP    CALL    RHED1      READ IN THIS BLOCK
0043 DA 49 00        0114          JC      TERR       IF ERROR OR ESC
0046 CA 2C 00        0115          JZ      LOLOOP     CONTINUE LOOP IF CRC TEST IS OK
                     0116 *
                     0117 *  ERROR RETURN
                     0118 *
0049 AF              0119 TERR     XRA     A
004A 37              0120          STC     .          SET ERROR FLAGS
004B C3 5B 00        0121          JMP     RTOF1
                     0122 *
                     0123 *  LAST BLOCK--PUT FINAL COUNT IN B
                     0124 *
004E 45              0125 LBLK     MOV     B,L        GET LOWER PORTION OF COUNT
004F 21 00 00        0126          LXI     H,0        TELL DE WE ARE FINISHED
0052 C3 3D 00        0127          JMP     RDBLK
                     0128 *
                     0129 *
0055 06 01           0130 TOFF     MVI     B,1        SHORT DELAY AFTER WRITE
0057 CD 1F 01        0131          CALL    DELAY
                     0132 *
005A AF              0133 RTOFF    XRA     A
005B D3 FA           0134 RTOF1    OUT     STAPT      TURN OFF THE TAPE
005D D1              0135          POP     D          RETURN BYTE COUNT
005E C9              0136          RET
                     0137 *
                     0138 *
                     0139 *
                     0140 *   READ THE HEADER
                     0141 *
005F 06 0A           0142 RHEAD    MVI     B,10       FIND 10 NULLS
0061 CD 8F 00        0143 RHEA1    CALL    STAT
0064 D8              0144          RC                 IF ESCAPE
0065 DB FB           0145          IN      TDATA      IGNORE ERROR CONDITIONS
0067 B7              0146          ORA     A          ZERO?
0068 C2 5F 00        0147          JNZ     RHEAD
006B 05              0148          DCR     B
006C C2 61 00        0149          JNZ     RHEA1      LOOP UNTIL 10 IN A ROW
                     0150 *
                     0151 *    WAIT FOR THE START CHARACTER
                     0152 *
006F CD 9D 00        0153 SOHL     CALL    TAPIN
0072 D8              0154          RC      .          ERROR OR ESCAPE
0073 3D              0155          DCR     A
0074 C2 6F 00        0156          JNZ     SOHL       WAIT FOR A '1
                     0157 *
```

```
                    0158 *
                    0159 *     NOW GET THE HEADER
                    0160 *
0077 21 2D 01       0161          LXI     H,THEAD     POINT TO BUFFER
007A 01 00 10       0162          LXI     B,HLEN*256  LENGTH OF HEADER IN  B ,C<0
                    0163 *
007D CD 9D 00       0164 RHED1    CALL    TAPIN       GET BYTE
0080 D8             0165          RC
0081 77             0166          MOV     M,A         STORE IT
0082 23             0167          INX     H           INCREMENT ADDRESS
0083 CD E6 00       0168          CALL    UDCRC       NOW CALCULATE THE CRC
0086 05             0169          DCR     B           WHOLE HEADER YET?
0087 C2 7D 00       0170          JNZ     RHED1       LOOP UNTIL DONE
                    0171 *
                    0172 *   THIS ROUTINE GETS THE NEXT BYTE AND COMPARES IT
                    0173 * TO THE VALUE IN REGISTER C.  THE FLAGS ARE SET ON
                    0174 * RETURN.
                    0175 *
008A CD 9D 00       0176 CRCCK    CALL    TAPIN       GET CRC BYTE
008D A9             0177          XRA     C           COMPARE IT WITH CALCULATED (CLEAR CARRY)
008E C9             0178          RET
                    0179 *
                    0180 *
                    0181 *     THIS ROUTINE GETS THE NEXT AVAILABLE BYTE FROM THE
                    0182 *  TAPE.  WHILE WAITING FOR THE BYTE THE KEYBOARD IS TESTED
                    0183 *  FOR AN ESC COMMAND.  IF RECEIVED THE TAPE LOAD IS
                    0184 *  TERMINATED AND A RETURN TO THE COMMAND MODE IS MADE
                    0185 *
008F DB FA          0186 STAT     IN      STAPT
0091 E6 40          0187          ANI     TDR
0093 C0             0188          RNZ     .           WHEN CHARACTER IS READY
0094 DB 01          0189          IN      KDATA
0096 FE 1B          0190          CPI     MODE         ESC ?
0098 C2 8F 00       0191          JNZ     STAT
009B 37             0192          STC     .           SET ERROR FLAG
009C C9             0193          RET                 AND RETURN
                    0194 *
                    0195 *
                    0196 *
009D CD 8F 00       0197 TAPIN    CALL    STAT        WAIT UNTIL A CHARACTER IS AVAILABLE
00A0 D8             0198          RC
                    0199 *
00A1 DB FA          0200 TREDY    IN      STAPT
00A3 E6 18          0201          ANI     TFE+TOE     DATA ERROR?
00A5 DB FB          0202          IN      TDATA       GET THE DATA
00A7 C8             0203          RZ      .           IF NO ERRORS
00A8 37             0204          STC     .           SET ERROR FLAG
00A9 C9             0205          RET
                    0206 *
                    0207 *
                    0208 *
                    0209 *
                    0210 *                  WRITE TAPE BLOCK ROUTINE
```

```
                        0211 *
                        0212 *   ON ENTRY:   A - HAS UNIT AND SPEED
                        0213 *               HL - HAVE POINTER TO HEADER
                        0214 *
                        0215 *
00AA E5                 0216 WTAPE    PUSH     H          SAVE HEADER ADDRESS
00AB CD ED 00           0217          CALL     WHEAD      WRITE THE HEADER
00AE E1                 0218          POP      H
00AF 11 07 00           0219          LXI      D BLKOF    OFFSET TO BLOCK SIZE IN HEADER
00B2 19                 0220          DAD      D          HL POINT TO BLOCK SIZE
                        0221 *  GET ADDRESS AND SIZE FROM HEADER
00B3 5E                 0222          MOV      E,M
00B4 23                 0223          INX      H
00B5 56                 0224          MOV      D,M        DE HAVE SIZE
00B6 23                 0225          INX      H          POINT TO STARTING ADDRESS
00B7 7E                 0226          MOV      A,M
00B8 23                 0227          INX      H
00B9 66                 0228          MOV      H,M
00BA 6F                 0229          MOV      L,A        HL HAVE STARTING ADDRESS
00BB E5                 0230 WRLO1    PUSH     H          FOR STACK CLEAN UP ON TURN OFF
                        0231 *
                        0232 *
                        0233 *    THIS ROUTINE WRITES ONE PHYSICAL BLOCK ON THE
                        0234 *  TAPE "DE" BYTES LONG FROM ADDRESS "HL .
                        0235 *
00BC 7A                 0236 WRLOP    MOV      A,D
00BD B3                 0237          ORA      E          TEST IF COUNT IS ZERO
00BE CA 55 00           0238          JZ       TOFF
00C1 01 00 FF           0239          LXI      B,-256     SUBTRACT 256 FROM IT
00C4 EB                 0240          XCHG
00C5 09                 0241          DAD      B
00C6 D2 D4 00           0242          JNC      WLBLK      IF 256 WEREN T LEFT
00C9 06 00              0243          MVI      B,0
                        0244 *
00CB 0E 00              0245 WDBLK    MVI      C,0        CRC STARTS WITH ZERO
00CD EB                 0246          XCHG                RESTORE COUNT TO DE, ADDRESS TO HL
00CE CD 02 01           0247 WDBL1    CALL     WLOOP      WRITE OUT THE BLOCK
00D1 C3 BC 00           0248          JMP      WRLOP      AND GO BACK TO MAJOR LOOP
                        0249 *
00D4 45                 0250 WLBLK    MOV      B,L        REMAINDER OF COUNT
00D5 21 00 00           0251          LXI      H,0        TELL DE WE ARE DONE
00D8 C3 CB 00           0252          JMP      WDBLK
                        0253 *
00DB F5                 0254 WRBYT    PUSH     PSW        SAVE CHARACTER
00DC DB FA              0255 WRWAT    IN       0FAH       GET UART STATUS
00DE E6 80              0256          ANI      80H
00E0 CA DC 00           0257          JZ       WRWAT      WAIT UNTIL IT IS READY
00E3 F1                 0258          POP      PSW
00E4 D3 FB              0259          OUT      0FBH       OUTPUT THE CHARACTER
                        0260 *
                        0261 *    THIS ROUTINE UPDATES THE CRC
                        0262 *
00E6 91                 0263 UDCRC    SUB      C          FORM PARTIAL
```

MANUAL DATA
CUTS READ AND WRITE ROUTINES

PROCESSOR TECHNOLOGY CORP
6200 HOLLIS STREET
EMERYVILLE CALIF 94608

```
00E7 4F              0264           MOV      C,A         SAVE IT
00E8 A9              0265           XRA      C           NOW BEND IT OUT
00E9 2F              0266           CMA      .           GET A FF
00EA 91              0267           SUB      C           CRC+1-1 IS NOT THE SAME
00EB 4F              0268           MOV      C,A         AND RESAVE IT
00EC C9              0269           RET
                     0270 *
                     0271 *
                     0272 *    THIS ROUTINE WRITES THE HEADER POINTED TO BY
                     0273 *    HL TO THE TAPE.
                     0274 *
00ED CD 1B 01        0275 WHEAD     CALL     WTON        TURN ON THE TAPE AND DELAY
00F0 16 32           0276           MVI      D,50        WRITE 50 ZERØS
00F2 AF              0277 NULOP     XRA      A
00F3 CD DB 00        0278           CALL     WRBYT
00F6 15              0279           DCR      D
00F7 C2 F2 00        0280           JNZ      NULOP
                     0281 *
00FA 3E 01           0282           MVI      A,1         50 ZERØS FOLLOWED BY A ONE
00FC CD DB 00        0283           CALL     WRBYT
00FF 01 00 10        0284           LXI      B,HLEN*256  HEADER LENGTH TO B, ZERO TO C
                     0285 *
0102 7E              0286 WLOOP     MOV      A,M         GET CHARACTER
0103 CD DB 00        0287           CALL     WRBYT       WRITE IT TO THE TAPE
0106 05              0288           DCR      B
0107 23              0289           INX      H
0108 C2 02 01        0290           JNZ      WLOOP
010B 79              0291           MOV      A,C         GET CRC
010C C3 DB 00        0292           JMP      WRBYT       PUT IT ON THE TAPE AND RETURN
                     0293 *
                     0294 *
                     0295 *    THIS ROUTINE COMPARES THE HEADER IN THEAD TO
                     0296 *    THE USER SUPPLIED HEADER ADDRESS IN HL.
                     0297 *    ON RETURN IF ZERO IS SET IF THE TWO NAMES COMPARED
                     0298 *
010F 06 05           0299 DHCMP     MVI      B,5         COMPARE FIVE CHARACTERS
0111 1A              0300 DHLOP     LDAX     D           GET ONE PART
0112 BE              0301           CMP      M           COMPARE IT WITH THE OTHER
0113 C0              0302           RNZ      .           RETURN IF NOT THE SAME
0114 05              0303           DCR      B
0115 C8              0304           RZ       .           IF ALL FIVE COMPARED
0116 23              0305           INX      H           COMPARE THE NEXT
0117 13              0306           INX      D
0118 C3 11 01        0307           JMP      DHLOP
                     0308 *
                     0309 *
011B 06 04           0310 WTON      MVI      B,4         SET LOOP DELAY
011D D3 FA           0311 TON       OUT      STAPT       TURN ON THE SELECTED DRIVE
                     0312 *
011F 11 00 00        0313 DELAY     LXI      D,0
0122 1B              0314 DLOP1     DCX      D
0123 7A              0315           MOV      A,D
0124 B3              0316           ORA      E
```

MANUAL DATA
CUTS READ AND WRITE ROUTINES

PROCESSOR TECHNOLOGY CORP
6200 HOLLIS STREET
EMERYVILLE, CALIF. 94608

```
0125 C2 22 01          0317           JNZ       DLOP1       LOOP HERE UNTIL DE ARE ZERO
0128 05                0318           DCR       B
0129 C2 1F 01          0319           JNZ       DELAY       LOOP HERE UNTIL B IS ZERO
012C C9                0320           RET
                       0321 *
                       0322 *
                       0323 *
                       0324 *
                       0325 *
                       0326 *
                       0327 *           PORT ASSIGNMENTS
                       0328 *
     00 FA             0329 STAPT     EQU       0FAH        STATUS PORT GENERAL
     00 FB             0330 TDATA     EQU       0FBH        TAPE DATA
     00 01             0331 KDATA     EQU       1           KEYBOARD DATA PORT FOR ESCAPE TEST
     00 1B             0332 MODE      EQU       1BH         ESCAPE KEY
                       0333 *
                       0334 *
                       0335 *
                       0336 *           BIT ASSIGNMENT MASKS
                       0337 *
                       0338 *
     00 08             0339 TFE       EQU       8           TAPE FRAMING ERROR
     00 10             0340 TOE       EQU       16          TAPE OVERFLOW ERROR
     00 40             0341 TDR       EQU       64          TAPE DATA READY
     00 80             0342 TTBE      EQU       128         TAPE TRANSMITTER BUFFER EMPTY
                       0343 *
     00 40             0344 TAPE1     EQU       64          TAPE ONE  OFF  BIT
     00 80             0345 TAPE2     EQU       128         TAPE TWO  OFF  BIT
                       0346 *
                       0347 *
                       0348 *
                       0349 *
                       0350 *                 GLOBAL AREA
                       0351 *
                       0352 *
                       0353 *
                       0354 *           SYSTEM PARAMETER AREA
                       0355 *
                       0356 *
                       0357 *
012D                   0358 THEAD     DS        5           NAME
0132                   0359           DS        1           THIS BYTE MUST BE ZERO FOR AUTO EXECUTE
0133                   0360 HTYPE     DS        1           TYPE
0134                   0361 BLOCK     DS        2           BLOCK SIZE
0136                   0362 LOADR     DS        2           LOAD ADDRESS
0138                   0363 XEQAD     DS        2           AUTO EXECUTE ADDRESS
013A                   0364 HSPR      DS        3           SPARES
                       0365 *
     00 10             0366 HLEN      EQU       $-THEAD     LENGTH OF HEADER
     00 07             0367 BLKOF     EQU       BLOCK-THEAD  OFFSET TO BLOCK SIZE
                       0368 *
                       0369 *
```

PROCESSOR TECHNOLOGY CORP.
6200 HOLLIS STREET
EMERYVILLE, CALIF. 94608

MANUAL DATA
CUTS READ AND WRITE ROUTINES

0370 *

PROCESSOR TECHNOLOGY CORP.
6200 HOLLIS STREET
EMERYVILLE CALIF. 94608

MANUAL DATA
CUTS READ AND WRITE ROUTINES

WRWAT	00DC	0257
WTAPE	00AA	
WTON	011B	0275
XEQAD	0138	