Q200 Series™
Intelligent Disk Drives
Technical Reference Manual

For Q250, Q280
Disk Drives

Q200 SERIES^{tm}
INTELLIGENT DISK DRIVES

Q250/Q280
DISK DRIVES

Technical Reference Manual

Publication No. 81-45528
REV A

PREFACE

This manual contains technical reference information describing the Q250 and Q280 rigid disk drives. Information is intended for technicians and engineers evaluating or maintaining the drives, or integrating them into systems.

Quantum reserves the right to make changes and/or improvements to its products without incurring any obligation to incorporate such changes or improvements in units previously sold or shipped.

Additional information on the Q250 and Q280 is given in the following manuals:

Publication No.	Title
Quantum 81-45233	Q250/Q280 Disk Drives. OEM Manual
Quantum 81-45416	Q200 Series Programmer's Manual
ANSI X3.131-1986	Small Computer System Interface (SCSI)

Quantum publications may be requested from your Quantum Sales Representative, or may be ordered from Quantum in the same manner as spare parts.

Publication No 81-45528 Rev. KL587

UL/CSA/VDE

UL recognition granted under File No. E78016
CSA certification granted under File Nos. LR496896-8 and LR496896-11
VDE certification granted per File No. 11342-3250-1002

WARRANTY

Model Q250 and Q280 disk drives are warranted against defects in material and workmanship for a period of one year from date of shipment. The warranty includes parts and labor. This is a limited warranty and further details can be obtained from your Quantum sales representative. All requests for service should be directed to the Quantum service center in your area.

PATENTS

The product described herein is covered by U.S. Patent No. 4,538,193, and is the subject of allowed pending patent applications from which U.S. Patents are expected to issue in 1987.

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L I S T O F T A B L E S

1.1 Features

Q250 and Q280 drives feature on-board, ANSI-standard, Small Computer System Interface (SCSI) controllers, and, with the exception of a plug-in EPROM IC, both models use the same printed circuit board (PCB). These drives require no operational adjustments. All electronics except the spindle motor, headstack, flex circuit, heads, and actuator rotor are contained on the PCB. A single IC is mounted on the flex circuit inside the sealed assembly.

The following features of the Q250/Q280 drives enable high data throughput:

- Seeks are initiated immediately--other commands are processed simultaneously.
- 14 KByte FIFO data buffer balances the transfer of data to and from the SCSI bus as well as to and from the drive.
- Optional DisCache increases data buffer size to 60 KBytes. (See the Q200 Series Programmers Manual for details concerning this option.)
- Cylinder and head skewing scheme minimizes latency when accessing data sequentially across cylinder boundaries.
- Defect management scheme minimizes seeks to spare sectors.
- Multiple block transfer of up to 64K-1 blocks, each with up to 2 Kbytes.
- RLL 1,7 (run-length-limited) encoding increases data density on the disks.

SCSI commands relieve the host system of many tasks, such as defect management, error correction, and physical sector addressing. Programmable options allow users flexible ways to handle defects initially and throughout the product's life. For example, (1) defective sectors can be automatically reassigned without the need to reformat, (2) data can be corrected with a Reed-Solomon error correcting code (ECC), or (3) all error detection and correction can be handled in the host computer. The ECC can correct one burst error of 17 bits, or detect three burst errors of 17 bits each.

Q200 Series^{tm} drives employ a hard-sectored format with servo data factory-written in wedges between all sectors on all surfaces. Thus, thermal and mechanical effects which tend to misalign heads on the headstack assembly are minimized, in comparison with other drives which use a dedicated servo surface. In addition, conservative linear bit and track densities ensure high data integrity. Logical block sizes of 512, 1024, and 2048 bytes are supported.

1.2 Logic Conventions

Signals on the SCSI bus are all true or asserted when they are at low level, and false or non-asserted when they are at high level. In this document, the names of such signals are always preceded by a minus, as "-ACK," and the timing diagrams are drawn to show the signals asserted when they are low, as they might be observed with an oscilloscope.

Other signals, as on the PCB, are indicated as follows:

Signal Type	Examples
Asserted when low	-POR
Asserted when high	+POR
Differential	Asserted when +READ SIG is more positive than -READ SIG
Analog	WRITE CURRENT, 5 V

Note that the ANSI Standard for SCSI, ANSI X3.131-1986 uses, for example, "-ACK" when listing connector pin connections, but describes the signals as "ACK" in the text, and shows positive true signals "+ACK" on timing diagrams.

SECTION 2. PRINCIPLES OF OPERATION

2.1 Head Disk Assembly (HDA)

2.1.1 Base Casting Assembly

The single piece, aluminum alloy base casting provides a mounting surface for the rest of the drive mechanism, PCB, and shock mount brackets. See Figure 2-1 for relative locations.

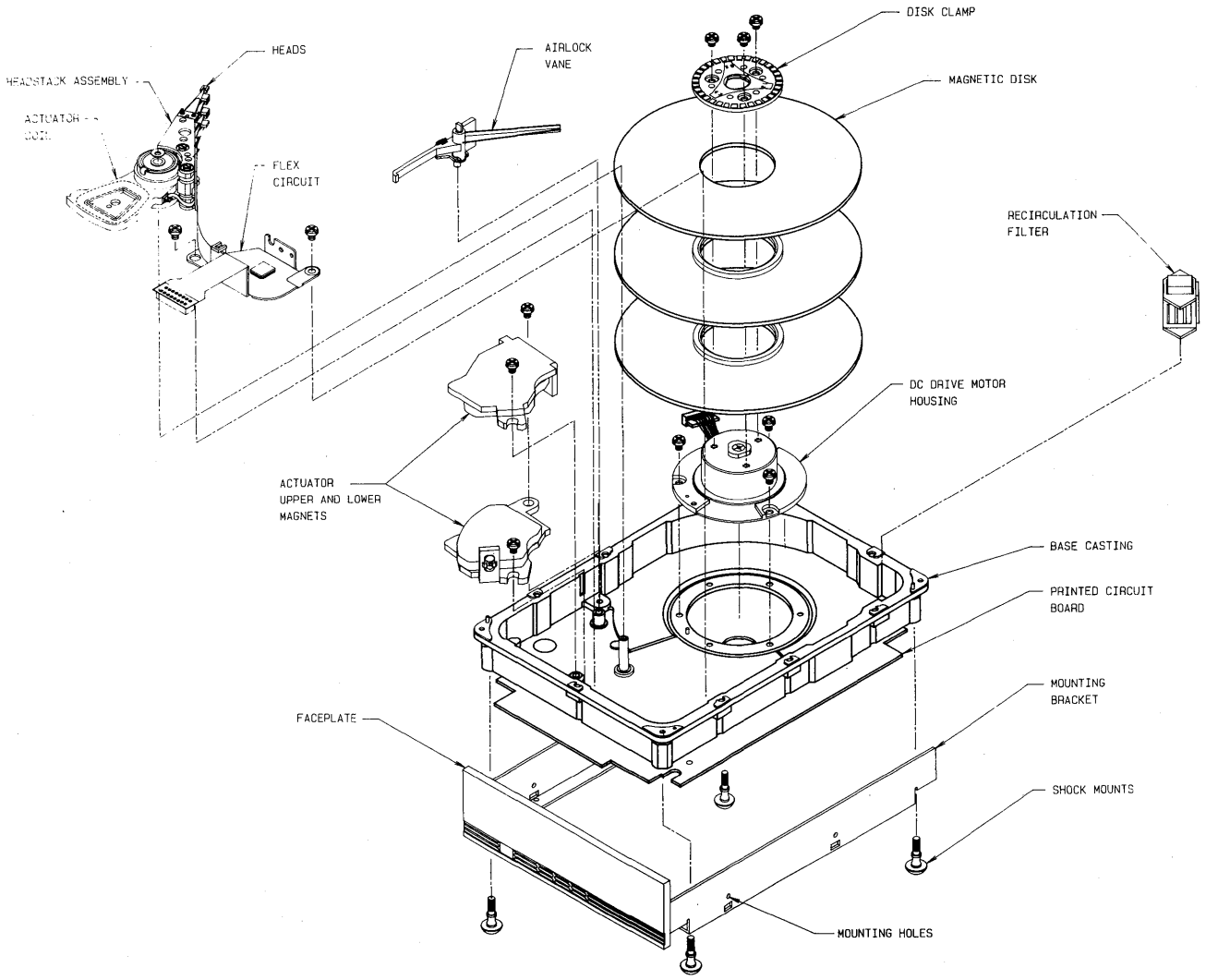


Figure 2-1: Exploded View

2.1.2 Disk Stack Assembly

Three aluminum alloy disks (two for the Q250) are placed on the motor hub and clamped in place. A thin film magnetic metal is sputtered on the surfaces of the disks, and lubricated with a carbon overcoat that prevents head and media wear when the heads are in contact with the head surface. This only occurs in the landing zone outside the data area, and when the disks are not rotating at full speed.

2.1.3 Rotary Positioner Assembly (Actuator)

The positioner is a proprietary design consisting of upper and lower permanent magnet plates, and a rotary single phase coil molded to the headstack mounting hub shaft. The magnets are composed of two alternating poles bonded to the magnet plates which, in turn, are bolted to the base casting. Resilient crash stops are mounted to the magnet plates. These prevent the heads from being driven into the spindle or off of the disk surface.

2.1.4 Headstack Assembly

The headstack assembly consists of the read/write heads, spacers, flex circuit, and rotary positioner assembly. The head arms and rotary positioner assembly balance each other so that the mass center of the entire stack is at the center of the mounting hub. The heads are mini-composite slider-type heads, mounted to Whitney-style spring steel flexures. The heads and actuator are connected by the flex circuit, which contains a read preamplifier/write driver chip.

2.1.5 Automatic Actuator Lock (AIRLOCK)

AIRLOCK is a mechanical means of locking the headstack in the landing zone, and is covered by U.S. Patents and pending patent applications. The dedicated landing zone for the heads ensures data integrity and prevents damage during shipment. When dc power is removed from the motor, an electronic return spring extracts energy from the spinning motor and pulls the headstack into the landing zone. AIRLOCK latches it in place. As dc power is applied to the motor and the disk stack starts spinning, airflow increases, and the airvane on AIRLOCK rotates, releasing the headstack.

2.1.6 DC Drive Motor

To achieve accurate speed control with minimum electromagnetic interference, the Q250/Q280 uses a brushless dc spindle motor in a closed-loop digital servo system, synchronized by a 2 MHz clock. The motor is dynamically balanced, four pole, three phase, and rotates at 3662 rpm. A 12 V motor control IC commutates the motor coils in

accordance with signals from three Hall-effect devices mounted at 120 degrees around the motor. The IC also limits the motor current on start up and produces dynamic braking to stop the motor quickly.

Contaminants are kept out of the drive by mounting the motor inside a heavy aluminum housing, bolted to the base casting. Two conductive ferro-fluid magnetic seals prevent outside air from entering the drive through the bearing core or along the bearing shaft. Motor components are processed and coated to eliminate dust, chips, and oxides, and final assembly is in a Class 100 clean room environment. EMI (Electromagnetic Interference) and electrostatic discharge (ESD) are reduced by grounding the rotating shaft with a brush of conductive teflon.

2.1.7 Air Filtration

The Q250 and Q280 are Winchester drives with a nominal flying height of 11 microinches.

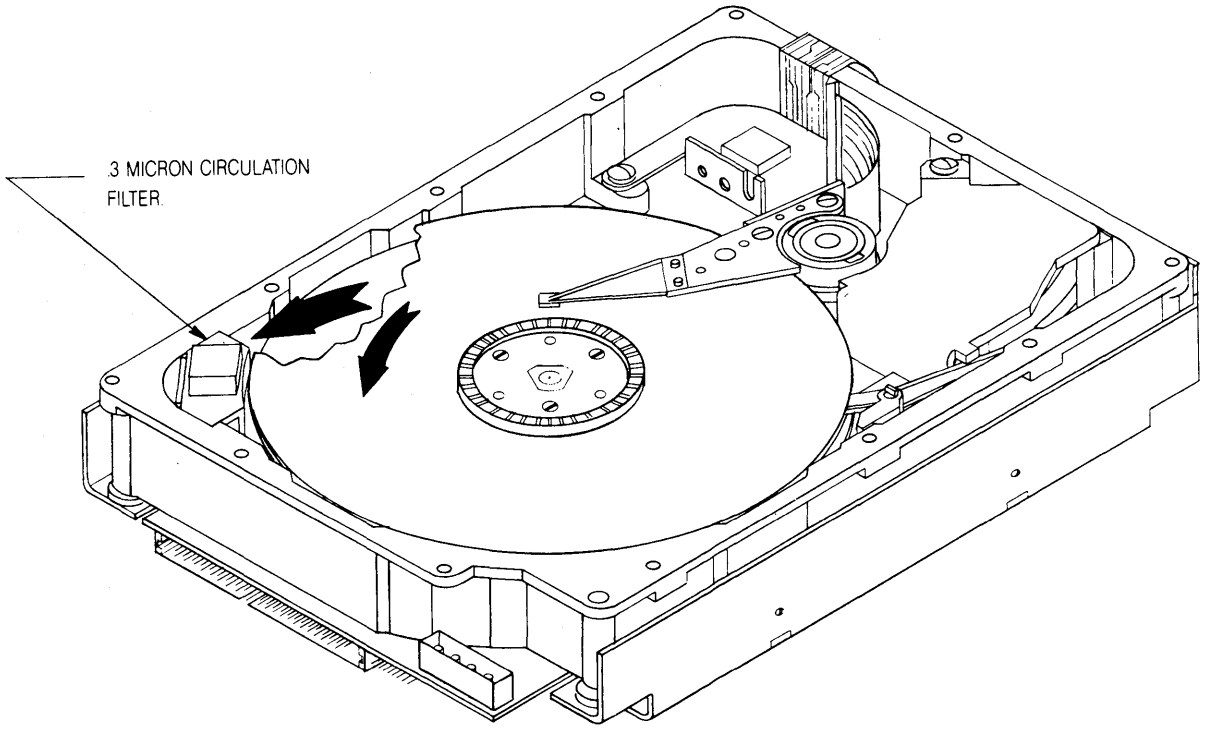


Figure 2-2: Inside View of Drive, Showing Air Filtration

To keep the air circulating within the drive free of particles, the drives are assembled in a Class 100 clean room environment, and then sealed with a metal cover. During the life of the drive, the rotating disks pump the enclosed air through an internal 0.3 micron recirculation filter, as shown in Figure 2-2. Another 0.3 micron filter, not shown, allows outside air into the sealed area of the drive to equalize internal and external pressures.

2.2 Drive Electronics

2.2.1 Disk Format

Q200 Series drives employ 823 user tracks (refer to Figure 2-3), while seven tracks are reserved for disk drive system uses -- such as defect lists, serial number ID and factory test data. Each data track contains thirty-two sectors and thirty-two servo wedges. Each user data area consists of a preamble and synchronization area, 512 bytes of data, and 12 bytes of ECC. A short postamble flushes the ECC buffers in DICEY.

Within the servo wedges are the servo tracks--three times as many as the data tracks--written in staggered sequence so they don't overlap on the disk. In a wedge, a servo track starts with a unique qual area that identifies the area as a wedge, and ends with a servo burst. As with the data areas, each burst begins with a preamble and synchronization area. In the bursts, this is followed by the servo track number, the head number (bursts A and C) or the sector number (bursts B and D), a checksum that allows error detection, and a short postamble.

At 3662 rpm, a complete sector, including wedge and 512-byte data area, passes under its head in 512 microseconds. The data itself passes under the head in about 410 microseconds, giving a maximum user data transfer rate of about 10 M bits/sec, i.e., 1.25 MBytes/sec.

2.2.2 Simplified Explanation--Block Diagram

This section summarizes the operation of the drive, as an introduction to the more detailed sections that follow. Refer to Figure 2-4, a simplified block diagram of the system.

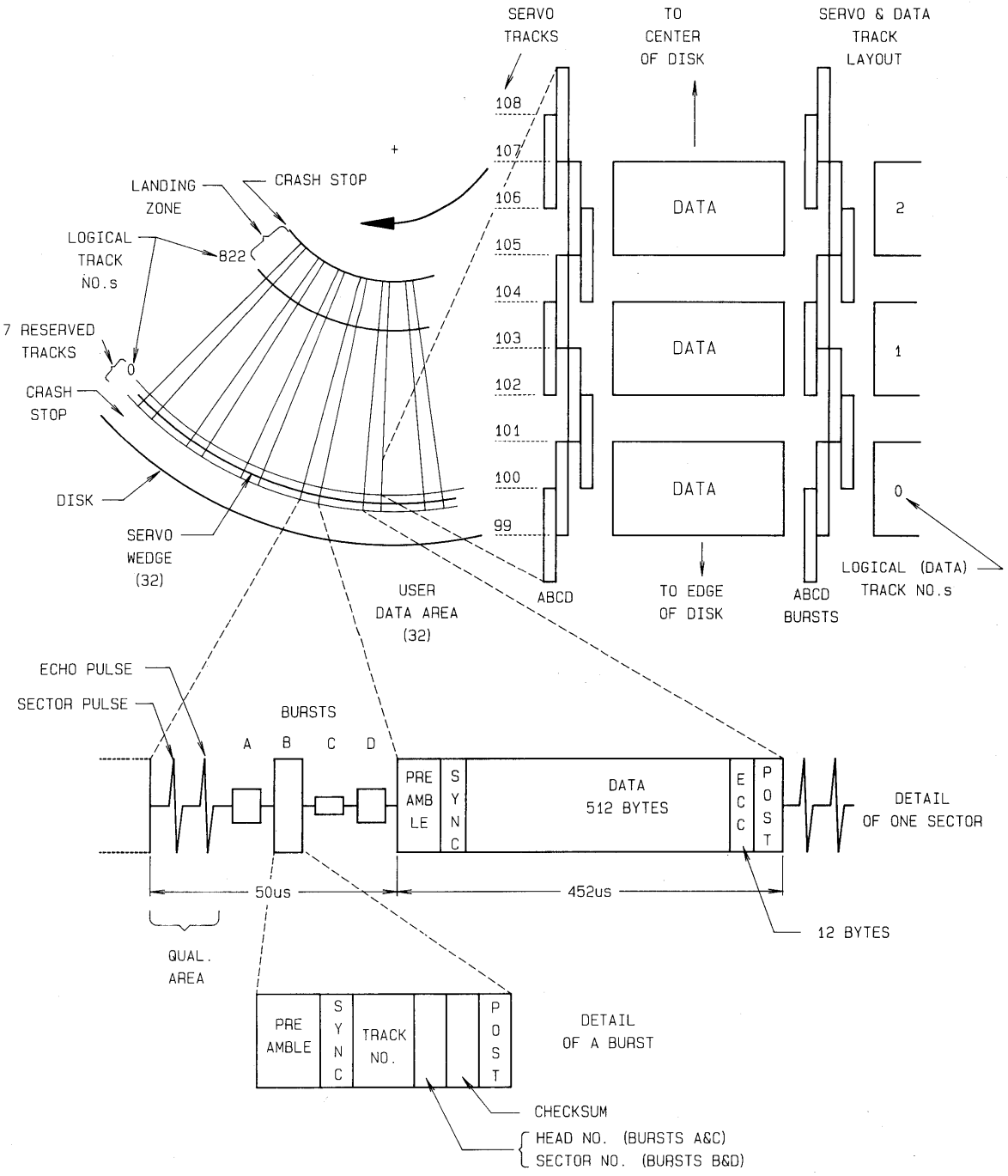


Figure 2-3: Disk Format: Wedges, Sectors, and Tracks

Power-On

Voltages may be applied in any sequence. When the dc voltages are low, as when the power has failed or has just been applied, the power-on-reset (POR) circuit resets the major circuits and keeps them reset until the voltages are high enough and stable.

At initial power-on, the drive is recalibrated: the actuator seeks to the inner, outer, and middle tracks; at each location, servo-burst amplitude measurements are made and from these the microprocessor calculates and stores adaptive gain parameters that are later used to optimize seek and settle times.

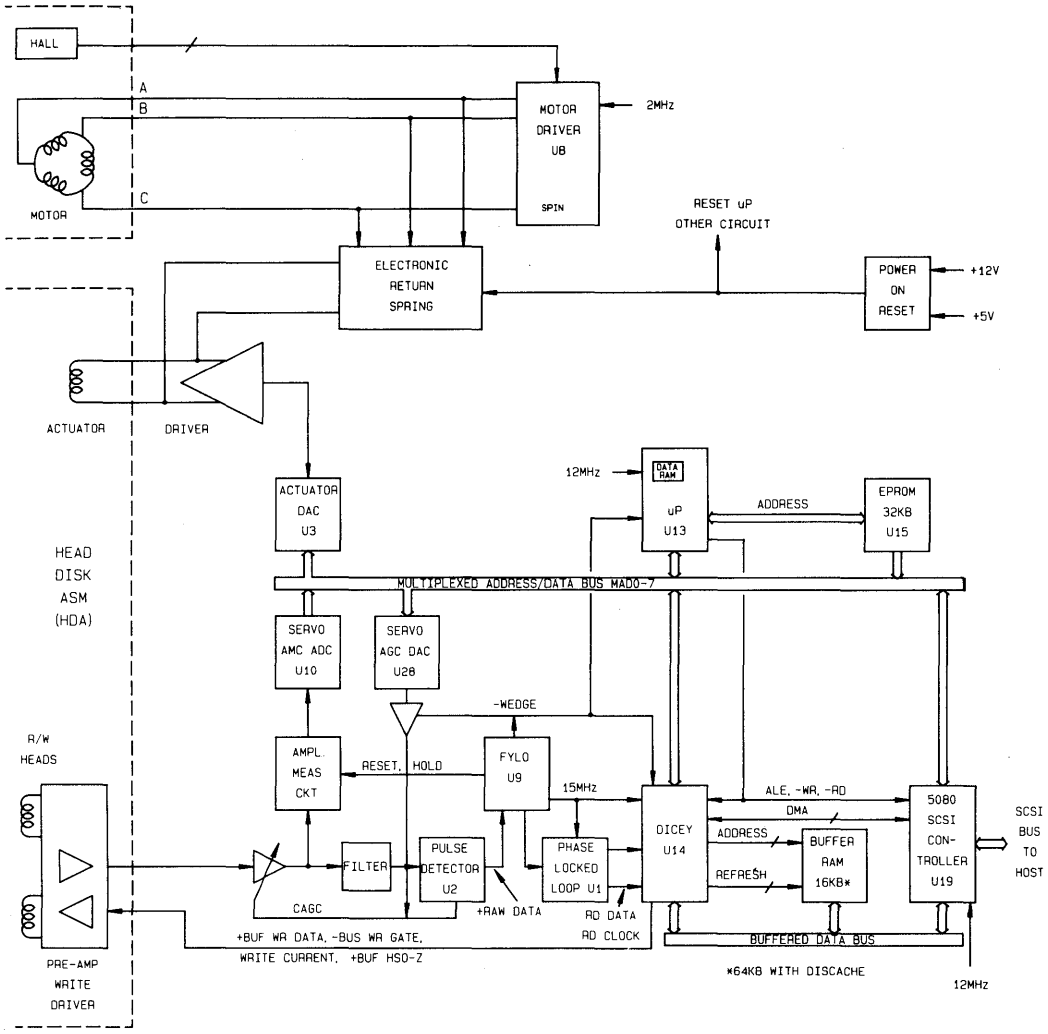


Figure 2-4: Electronics Block Diagram

Architecture

A standard 8-bit microprocessor operated at 12 MHz controls each Q200 Series drive. An 8031 is used for drives without DisCache, an 8032 for drives with it. Firmware is in a plug-in 32 K X 8 EPROM. Different EPROMS are used for the Q250 and Q280, and for drives with and without DisCache. Special EPROMs may be used for custom applications.

Communication between the major circuit components is over the 8-bit MAD (multiplexed address/data) bus. DICEY, a proprietary data-controller IC, manages access to the buffer, which is 16 KBytes of dynamic RAM (64 KBytes for drives with DisCache). The upper 2 KBytes of RAM (4 KBytes with DisCache) is reserved for Q250/Q280 use. DICEY is the DMA controller, performs serial to parallel and parallel to serial conversions, handles all RLL encoding and decoding, and generates the ECC syndrome.

SCSI Bus Operations

Communications with the host and other SCSI devices is over the SCSI bus. The interface is implemented with a 5080 SCSI Controller IC that can play the role of initiator or target, and performs disconnect/reconnect and arbitration functions.

Before the disk is written to, a full sector of incoming SCSI data is accumulated in buffer RAM (via DMA transfers). As the disk is being read from, data is also stored in RAM. After a full sector is read, the data is checked with the error-correcting code (at the user's option), transferred through the 5080 via DMA, then on to the SCSI bus. Users can select the action to be taken in the event that an error is detected, via the MODE SELECT command.

Servo

While track-following, track and sector numbers of the current position are stored in buffer RAM--the microprocessor knows the exact head position at all times. When a READ or WRITE command arrives, the microprocessor immediately starts a seek by commanding the head position DAC (digital-to-analog converter) via the MAD bus. The DAC output is converted to a high current, which drives the actuator. New track and sector numbers are read on the fly from the servo bursts, forming a closed loop. The microprocessor accelerates, then decelerates, the actuator via the head position DAC to achieve the seek in the shortest time.

As servo bursts pass under the head, their amplitudes are measured by the AMC (amplitude measurement circuit), and placed on the MAD bus by the servo ADC (analog-to-digital converter). When seeking, the microprocessor reads head position from the burst with the highest amplitude, if possible. Once the head is on track, the microprocessor

keeps the head following the track exactly, by adjusting the head position so that the amplitudes of the two servo bursts written on each side of the data track are equal. For example, in Figure 2-3, bursts A and D on logical track 0 are kept equal.

Read

There is one head for each surface: four on the Q250, six on the Q280. Each head can either read or write. When reading, the output is amplified first by the preamplifier chip in the HDA, then by an AGC (automatic-gain-control) amplifier. That output is filtered, then differentiated to find the zero crossings, and converted to pulses by a pulse detector. A phase-locked loop circuit derives synchronized data and clock signals for DICEY. Careful design makes drop-ins or drop-outs rare. RLL 1,7 encoding allows 1.33 data bits to be stored for every magnetic transition on the disk.

Write

The preamplifier/write driver chip inside the HDA selects the head (under command of the microprocessor) and sends current reversals to the head, which writes magnetic transitions on the disk.

2.2.3 SCSI Bus Physical Interface

A 50-pin connector is provided at position J1 on the PCB for connecting to the standard SCSI bus. See Figures 2-5 and 2-9. The standard SCSI single-ended non-shielded connector is used. J1 is a Universal Header connector and has a key slot to prevent installing the mating connector improperly. The recommended mating connector is AMP receptacle P/N 1-499508-2 (with strain relief) or P/N 1-746195-2 (without strain relief), or equivalent. Unkeyed mating connectors should not be used due to the danger of plugging the connector in backwards.

A 50-conductor flat cable or a 25-signal twisted-pair ribbon cable with a minimum conductor size of 28 AWG and a characteristic impedance of 100 ohms +/- 10% is recommended. SCSI devices are daisy-chained together using a common cable. To minimize discontinuities and signal reflections, cables of different impedances should not be used in the same bus. Table 2-1 gives J1 pin assignments. Note that to achieve satisfactory transmission quality, all odd pins except pin 25 are connected to ground; pin 25 is left open. Maximum total cable length is 20 feet (6 meters), a length suitable for use in a cabinet.

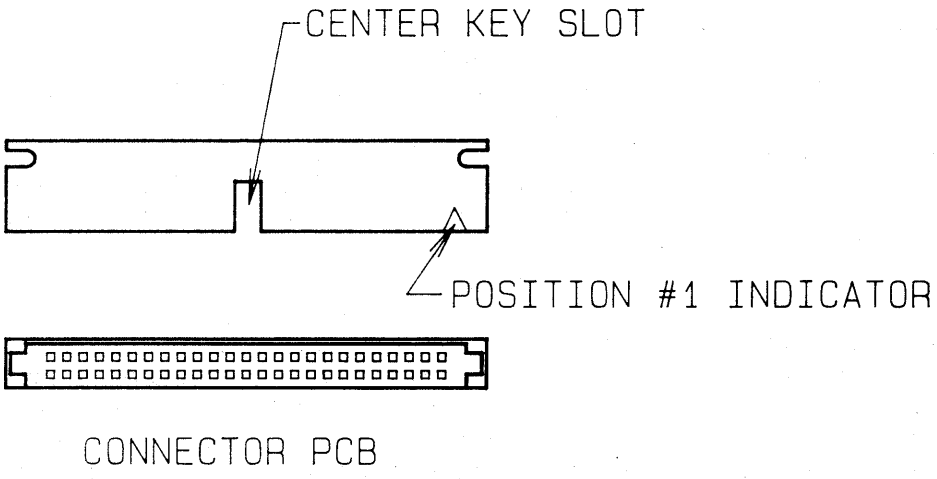


Figure 2-5: J1 Connector

Table 2-1: J1 Pin Assignments

Ground	Signal	Name
1	2	-Data Bit 0 (-DB0)
3	4	-Data Bit 1 (-DB1)
5	6	-Data Bit 2 (-DB2)
7	8	-Data Bit 3 (-DB3)
9	10	-Data Bit 4 (-DB4)
11	12	-Data Bit 5 (-DB5)
13	14	-Data Bit 6 (-DB6)
15	16	-Data Bit 7 (-DB7)
17	18	-Data Bit P (-DBP)
19	20	Ground
21	22	Ground
23	24	Ground
25		Open
	26	Terminator Power (TERMPWR)
27	28	Ground
29	30	Ground
31	32	-ATN
33	34	Ground
35	36	-BSY
37	38	-ACK
39	40	-RST
41	42	-MSG
43	44	-SEL
45	46	-C/D
47	48	-REQ
49	50	-I/O

2.2.4 SCSI Bus Signal Descriptions

All signals are true low and use open collector drivers (see Figure 2-6 for a typical circuit). A termination is required at each physical end of the bus. Three resistor networks in sockets are provided as terminators. Drives are shipped from the factory with the terminators plugged in. See Figure 2-9 for locations on the PCB.

CAUTION

Only the two devices at the physical ends of the SCSI bus are allowed to have terminators: remove terminators from all other devices on the bus (unplug all three terminator packages). If the additional terminators are not removed, the bus drivers may be damaged because they will sink more current from the +5 V supply than the 48 mA they are rated to carry.

CAUTION

Plug-in terminator packages are polarized, and must be plugged in correctly. On each package, pin 1 is marked with a dark band, and must face the "1" that is screened on the PCB. All terminators face the same way. If in doubt about the correct orientation, consult Figure 2-9.

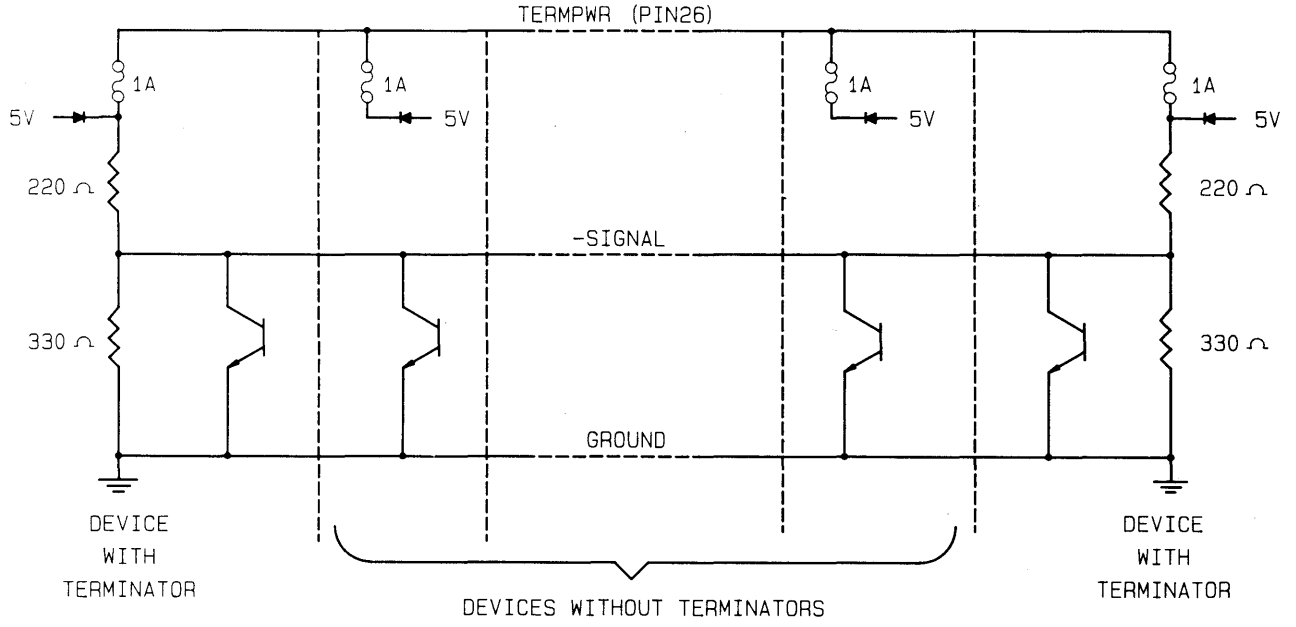


Figure 2-6: SCSI Bus. Typical Circuit of a Signal Line

Each Q250/Q280 bus driver has the following output characteristics:

True (Signal Asserted) = 0.0 to 0.4 V dc at 48 mA.
False (Signal Non-Asserted) = 2.5 to 5.25 V dc.

Each signal received by the Q250 or Q280 must have the following input characteristics:

True (Signal Asserted) = 0.0 to 0.8 V dc.
Maximum total input load = -0.4 mA at 0.4 V dc.
False (Signal Non-Asserted) = 2.0 to 5.25 V dc.
Minimum input hysteresis = 0.2 V dc.

SCSI Bus Signals

Up to eight devices can be supported on the SCSI bus, but communication is allowed between only two SCSI devices at any given time.

Information transfers on the SCSI DATA BUS are asynchronous and follow a defined -REQ/-ACK (request/acknowledge) handshake protocol. One byte of information can be transferred with each handshake. There are a total of 18 logic signals: nine control signals and nine signals that comprise an 8-bit DATA BUS with parity. Each of the signals is described briefly below.

-BSY (BUSY). An "OR-tied" signal that indicates that the bus is being used.

-SEL (SELECT). A signal used by an initiator to select a target or by a target to reselect an initiator.

-C/D (CONTROL/DATA). A signal driven by a target that indicates whether CONTROL or DATA information is on the DATA BUS. Assertion indicates CONTROL.

-I/O (INPUT/OUTPUT). A signal driven by a target that controls the direction of data movement on the DATA BUS with respect to an initiator. Assertion indicates input to the initiator. This signal is also used to distinguish between SELECTION and RESELECTION phases.

-MSG (MESSAGE). A signal driven by a target during the MESSAGE phase.

-REQ (REQUEST). A signal driven by a target to indicate a request for a -REQ/-ACK data transfer handshake.

-ACK (ACKNOWLEDGE). A signal driven by an initiator to indicate an acknowledgement for a -REQ/-ACK data transfer handshake.

-ATN (ATTENTION). A signal driven by an initiator to indicate the ATTENTION condition.

-RST (RESET). An "OR-tied" signal that indicates the RESET condition.

-DB(7-0,P) (DATA BUS). Eight data-bit signals, plus a parity-bit signal, that form a DATA BUS. -DB(7) is the most significant bit and has the highest priority during the arbitration phase. Bit number, significance, and priority decrease downward to -DB(0). A data bit is defined as one when the signal is asserted and is defined as zero when the signal is non-asserted.

Data parity -DB(P) is odd. The use of parity is a system option (i.e., a system is configured so that all SCSI devices on a bus generate parity and have parity detection enabled, or all SCSI devices have parity detection disabled or not implemented). Parity is not valid during the ARBITRATION phase.

TERMPWR. 4.0 V dc to 5.25 V dc provided by each device for the bus terminations in other SCSI devices, to keep the line terminated in the event of 5 V failure.

2.2.5 SCSI Bus Timing

Delay-time measurements for each SCSI device are calculated from signal conditions existing at that device's own SCSI bus connector. Thus, the following delays (except cable skew delay) can be measured without considering delays in the cable.

ARBITRATION DELAY (2.2 microseconds). The minimum time an SCSI device must wait from asserting -BSY for arbitration until the DATA BUS can be examined to see if arbitration has been won. There is no maximum time.

BUS CLEAR DELAY (800 nanoseconds). The maximum time for an SCSI device to stop driving all bus signals after:

(1) The BUS FREE phase is detected (-BSY and -SEL both deasserted for a bus settle delay period).

(2) -SEL is received from another SCSI device during the ARBITRATION phase.

(3) The transition of -RST to asserted.

NOTE: For the first condition above, the maximum time for an SCSI device to clear the bus is 1200 nanoseconds from -BSY and -SEL first becoming both deasserted. If an SCSI device requires more than a bus settle delay to detect BUS FREE phase, it must clear the bus within a bus clear delay minus the excess time.

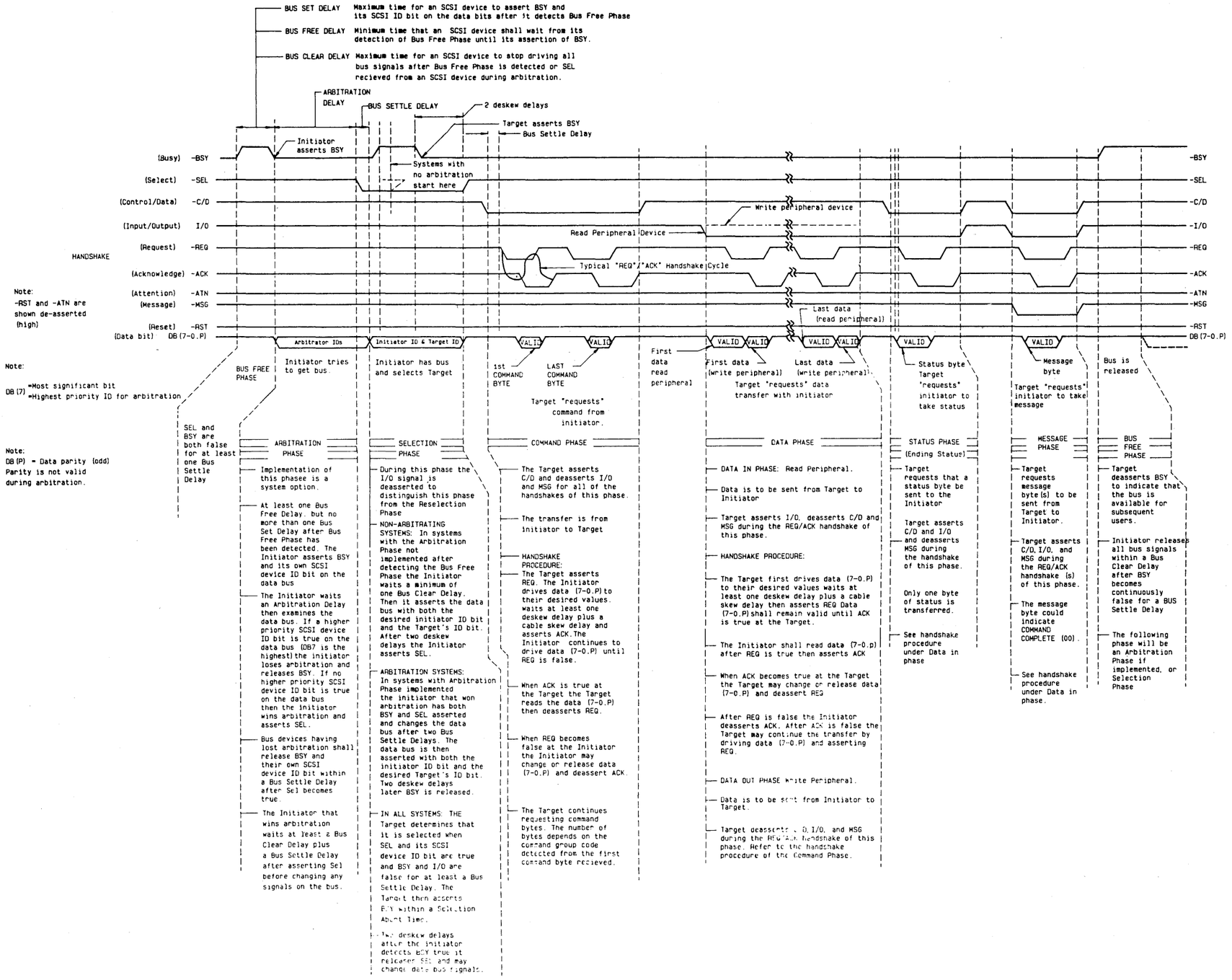


Figure 2-7: SCSI Bus Timing Diagram

BUS FREE DELAY (800 nanoseconds). The minimum time that an SCSI device must wait from its detection of the BUS FREE phase (-BSY and -SEL both deasserted for a bus settle delay) until its assertion of -BSY when going to ARBITRATION phase.

BUS SET DELAY (1.8 microseconds). The maximum time for an SCSI device to assert -BSY and its SCSI ID bit on the DATA BUS after it detects BUS FREE phase (-BSY and -SEL both deasserted for a bus settle delay) for the purpose of entering ARBITRATION phase.

BUS SETTLE DELAY (400 nanoseconds). The time to wait for the bus to settle after changing certain control signals as called out in the protocol definitions.

CABLE SKEW DELAY (10 nanoseconds). The maximum difference in propagation time allowed between any two SCSI bus signals when measured between any two SCSI devices.

DATA RELEASE DELAY (400 nanoseconds). The maximum time for an initiator to release the DATA BUS signals following the transition of the I/O signal from deasserted to asserted.

DESKEW DELAY (45 nanoseconds). The minimum time required for deskew of certain signals.

RESET HOLD TIME (25 microseconds). The minimum time for which -RST is asserted. There is no maximum time.

SELECTION ABORT TIME (200 microseconds). The maximum time that a target (or initiator) takes from its most recent detection of being selected (or reselected) until asserting a -BSY response. This time-out is required to ensure that a target (or initiator) does not assert -BSY after a SELECTION (or RESELECTION) phase has been aborted. This is not the selection timeout period.

SELECTION TIMEOUT DELAY (250 milliseconds). The minimum time that an initiator (or target) waits for a -BSY response during the SELECTION (or RELSELECTION) phase before starting the timeout procedure.

Figure 2-7 is an SCSI bus timing diagram showing all of the SCSI bus signals and many of the above delays.

2.2.6 Power Requirements

Voltage and current requirements for the dc power supplied to the drive are listed in Table 2-2. There is no regulation on the drive; regulated power must be supplied. Supply returns are connected together, to the PCB ground plane, the headstack, and the base casting. An external ground may be connected to a tab on the base casting (see Section 4.3).

No damage to data occurs if power is applied or removed in any order or manner, but data may be lost in the sector being written at the time of power loss. This includes shorting out or opening up either voltage or return line, transient voltages +10% to -100% from nominal, and while powering up or down.

Table 2-2: DC Power Requirements

Specified Voltage	Typical Idle	Typical Seeking	Maximum Current	Max. Ripple and Noise	POR Voltage Limits*
4.75-5.25	0.8 A	0.8 A	1.8 A	50 mV p-p	4.6 - 4.2
10.8-13.2	1.2 A	1.5 A	3.0 A	150 mV p-p	10.4 - 9.7

*Typical POR hysteresis is 50 mV on 5 V; 100 mV on 12 V.

Figure 2-8 shows the drive startup current profile. The Wait Spin shorting plug option can be used to delay startup until the host issues SCSI START/STOP UNIT commands, thereby limiting the surge current when starting multiple drives. Before the motor is started, the +12 V current is 0.4 A.

An additional 0.8 A is required from the 5 V supply if the SCSI line TERMPWR, pin 26, is connected. This current supplies the terminators at the two SCSI devices that are equipped with terminators, if the 5 V fails at those units. See Figure 2-6 for the schematic.

A drive is reset by the POR circuit on the PCB if the voltage falls below the POR limits. However, the drive may not operate correctly at those limits, which are below normal. The POR circuit does not guarantee that supply levels are within specification.

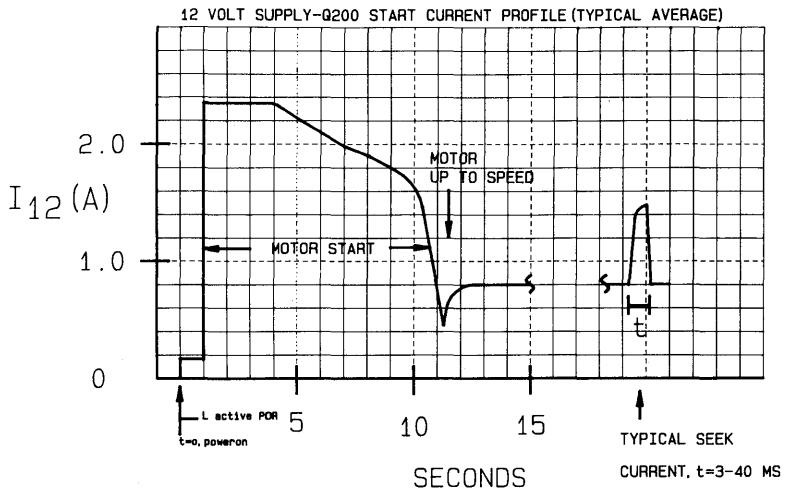


Figure 2-8: Drive Startup Current Profile

2.2.7 Shorting Plug Options

Figure 2-9 is a top view of the PCB, showing the locations of shorting plugs, terminators, and connectors.

SCSI Bus Device Address

Three shorting plugs A2, A1, and A0, determine the unique address (0-7) assigned to each drive. The address determines the priority level of each device and therefore which device wins arbitration if several devices are contending for the SCSI bus simultaneously. Highest priority is address 7, usually given to the host, and lowest priority is address 0. The three plugs establish a 3-bit binary number with the following values: A2 = 4, A1 = 2, A0 = 1. With no plugs inserted, the address is 0; with all plugs inserted, the address is 7. Drives are shipped with plugs in A2 and A1 (address 6).

Enable Parity (EP)

When shorting plug EP is installed, parity checking of data across the SCSI bus is enabled. With EP removed, parity is not performed. The use of parity is a system option. See the description of signal -DB(7-0,P) in Section 2.2.4 for additional information.

Drives are shipped from the factory with parity enabled (plug EP installed).

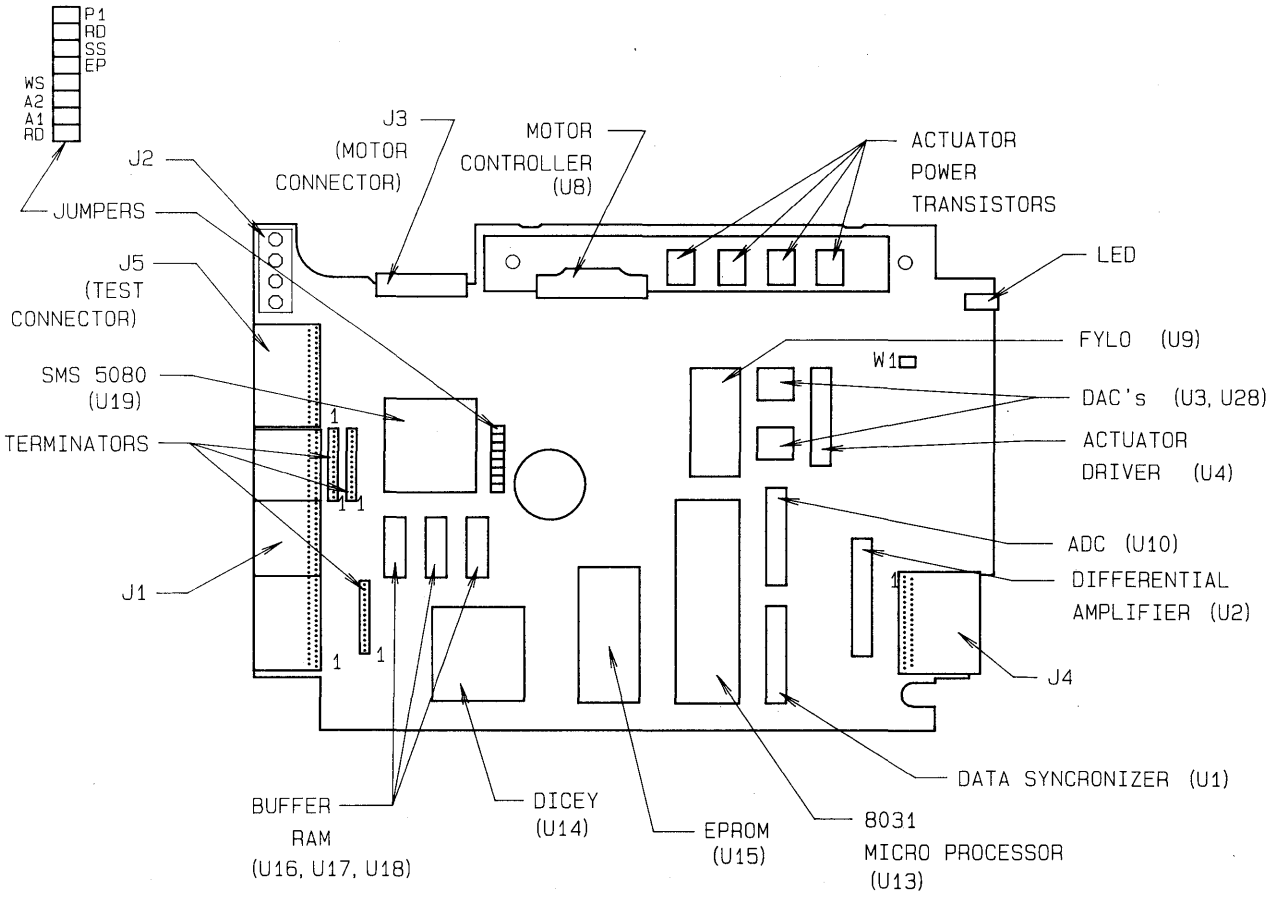


Figure 2-9: General PCB Layout; Plug, Terminator and Connector Locations

Wait Spin Option (WS)

When the WS shorting plug is installed, the motor waits for a START/STOP UNIT command from the host via the SCSI bus before spinning. Multiple drives can then be started in sequence to avoid overloading the system power supply. Once the START/STOP UNIT command is received, a drive is ready within 30 seconds.

With the WS shorting plug not installed, the motor automatically starts spinning when power is applied, and the drive is ready in 30 seconds. Drives are shipped from the factory in this condition.

Self Seek Option (SS)

This option is provided as a method to continuously exercise the drive. With shorting plug SS installed, the drive continuously executes a "butterfly" seek pattern. The drive need not be connected to a SCSI bus. No test results are given, but if the drive stops, a malfunction has occurred.

Drives are shipped from the factory with SS disabled (shorting plug SS not installed).

Reset Option (RO)

Shorting plug RO determines whether a drive responds to the SCSI bus signal -RST (reset) with a cold reset (plug installed) or a warm reset (plug not installed). The Q250 and Q280 never assert -RST.

If cold reset is selected, (RO plug installed) the drive immediately performs a POR (Power-On-Reset) when the -RST signal is detected: it resets all drive functions including write to disk, performs a complete recalibration, reevaluates all shorting plugs except Wait Spin, and goes to the SCSI bus free phase. Unrecoverable read errors may result if a drive is cold reset while writing. Cold reset typically takes six seconds, during which time the drive cannot respond to commands.

If warm reset (RO plug not installed) is selected and the -RST signal is detected, the drive completes writing the current sector, performs a partial servo resynchronization, and goes to the SCSI bus free phase. Warm reset typically requires 200 ms. It is particularly useful when the host issues multiple -RSTs.

Both warm and cold resets meet the ANSI requirements for a "hard" reset. Drives are shipped from the factory set for warm reset (RO plug not installed).

External LED (W1)

If an external LED will be connected to J6, remove shorting plug W1. Leave W1 installed to use the LED on the face of the drive.

Drives are shipped with W1 installed.

Spare Shorting Plug (P1)

For the convenience of customers, drives are shipped from the factory with a spare shorting plug installed in position P1. No drive function is affected by P1.

2.2.8 Flex Circuit

The Flex Circuit is a flexible printed circuit mounted in the sealed HDA, close to the heads to improve the signal-to-noise ratio. One end of the thin flexible circuit is clamped under the cover and terminates in a 16-pin connector which mates with J4 on the PCB. A special purpose preamplifier/write driver IC (SSI 501) is soldered to the circuit inside the drive. This chip:

- Selects the head according to three-bit logic input +BUF HS2, +BUF HS1, +BUF HS0, from the microprocessor, through DICEY.
- Switches from reading to writing when DICEY asserts -BUF WR GATE.
- When writing, multiplies WRITE CURRENT. On successive falling edges of +BUF WR DATA, the chip sources the multiplied current through alternate sides of the coil, reversing the magnetic field and magnetizing the spinning media in alternate directions.
- Amplifies read signals from each head about 100 times.
- Detects fault conditions such as defective heads, write current while reading, no write current, and write data transitions too infrequent. If faults are detected, asserts +WR UNSAFE.

The output is the differential signal RDX and RDY.

2.3 PCB Functional Elements

2.3.1 Power-On-Reset (POR) and Warm Reset

A cold reset is triggered by:

- Low supply voltage
- SCSI bus signal -RST asserted by the host, with the RO shorting plug installed in the drive.

POR resets the microprocessor, DICEY, the 5080 SCSI controller, and the actuator driver, and enables the electronic return spring (after a delay). POR dynamically brakes the motor by clamping all coil output voltages to 6 V. Transistor switches perform each function.

POR is released 11 ms to 60 ms after +5 V and +12 V are normal, a delay that ensures that the power is stable and also allows the logic to initialize during power up. To avoid multiple resets, the POR thresholds are set below the normal power operating ranges and a

small hysteresis between the upper and lower thresholds is maintained. Overvoltage conditions are not detected. After POR is released, the drive is recalibrated, typically taking six seconds.

Circuit Description

See the schematics in SECTION 3 for the POR circuit. Comparators U6 (output pins 13 and 14) compare the supply voltages to voltage reference CR12 to produce the signals -PORA, -PORB, and +POR. C24 sets the 11 to 60 ms delay. When the voltage across C24 rises above the CR12 reference, the U6 (output pin 1) comparator deasserts the three POR signals.

Pin 56 (-RESET CAP) on the 5080 is an input if a POR is initiated at the Q250/Q280: the 5080 is reset by the POR circuit either through the RO plug or through Q28.

On the other hand, when the host asserts -RST on the SCSI bus, the 5080 pulls the -RESET CAP pin (now an output) low. If the RO plug is installed, -POR A is also pulled low and a cold reset is triggered. If the RO plug is not installed, Q28 remains turned off, and the POR circuit is unaffected. However, a warm reset now follows, controlled by the microprocessor, which has been triggered by an interrupt from the 5080.

At the start of a warm reset, flip-flop U29 (Q = pin 9) is toggled on by -RESET CAP, U29 then deasserts the SCSI lines -MSD, -C/D, -I/O via gates U24 and U26. Later, the microprocessor clears the flip-flop and enables the lines via DICEY pin AUX 6.

2.3.2 Motor Control Circuit

Refer to the schematic in SECTION 3 for the circuit diagram. The motor control IC (U8) senses the differential output signals from the three Hall-effect devices mounted around the motor, and drives currents through the three delta-wound motor coils. The Hall signals replace a commutator by indicating when to commutate current to the coils. Speed is sensed from a Hall signal and compared in U8 to a 2 MHz clock from FYLO. Starting current is inversely proportional to R97. Loop gain and bandwidth of the op-amp current integrator are controlled by R95, R96, C35, and C42. C36 filters the integrator output. C39, C40, and C41 reduce ringing.

COIL A to COIL B voltage is processed by comparator U6 (output pin 2) to generate MOTOR POSITION, which the microprocessor checks to determine that the motor is up to speed. The signal is two cycles per revolution.

Q24 turns off the motor when -POR B is asserted or when the microprocessor causes DICEY to deassert -SPIN, which turns off Q8. Back EMF generated by the spinning motor flows through the IC drivers, whose outputs are clamped to 6 V, producing dynamic braking.

2.3.3 Electronic Return Spring

When the drive is powered down, the electronic return spring utilizes the back EMF from the slowing motor, switching it to the actuator, thus forcing the headstack into the landing zone.

At power-on-reset, -POR turns Q3 off after a delay set by C29. This delay allows the driver currents to fall to a safe level (while Q5 discharges C36 and clamps the U8 current integrator output). Q4, Q7, and Q14 turn on. Twice per revolution Q7 passes current from the motor to the actuator, then through Q14 and R42 to ground.

If the +12 V dc supply has failed, the circuit still functions, but if the +12 V dc is maintained, more current is supplied to the actuator. Only milliseconds are required to move the actuator into the landing zone; AIRLOCK operates about 30 seconds later. Do not handle the drive during this period.

2.3.4 5080 SCSI Bus Controller

A 5080 SCSI Controller IC is used to implement the SCSI interface. CMOS technology reduces the power consumption. All inputs and outputs conform to standard 5 V logic levels. The SCSI bus pins of the 5080 meet the ANSI standards, and are connected directly to the SCSI bus. The 5080 can operate with various microprocessors; in this application it is strapped to operate with an 8031 or 8032 by tying the CONFIG pin low and the IOEN pin high. Pins XOR A7-A5 are strapped so the 5080 is selected when address bits MAD7-5 are 110 (address range C0 - DF).

On command of the microprocessor, the 5080 reads the SCSI address of the drive and the options set by the shorting plugs, which are connected to 5080 pins IN 0-5.

Figure 2-10 is a conceptual block diagram of the 5080. Figure 2-11 emphasizes the external interfaces. The signals mentioned below are shown on the schematics in SECTION 3 and in Figure 2-4.

Registers in the 5080 are written and read by the microprocessor over the MAD bus. In this way, for example, the microprocessor can (1) switch the 5080 from target to initiator mode, (2) assert and deassert SCSI bus signals, (3) read the state of SCSI bus control signals from the host, and (4) set the programmable timing for the SCSI SELECTION/ RESELECTION and ARBITRATION phases. The 5080 provides logic for arbitration.

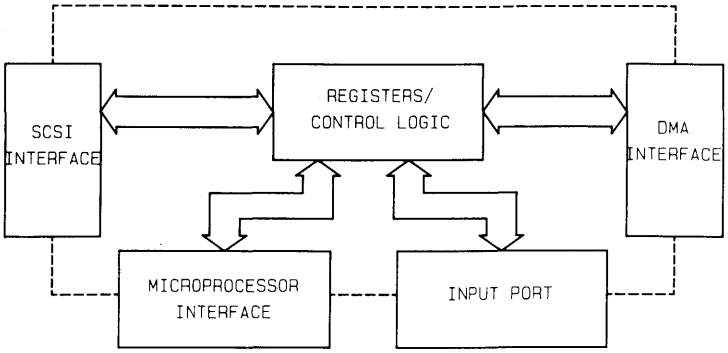


Figure 2-10: 5080 Conceptual Block Diagram

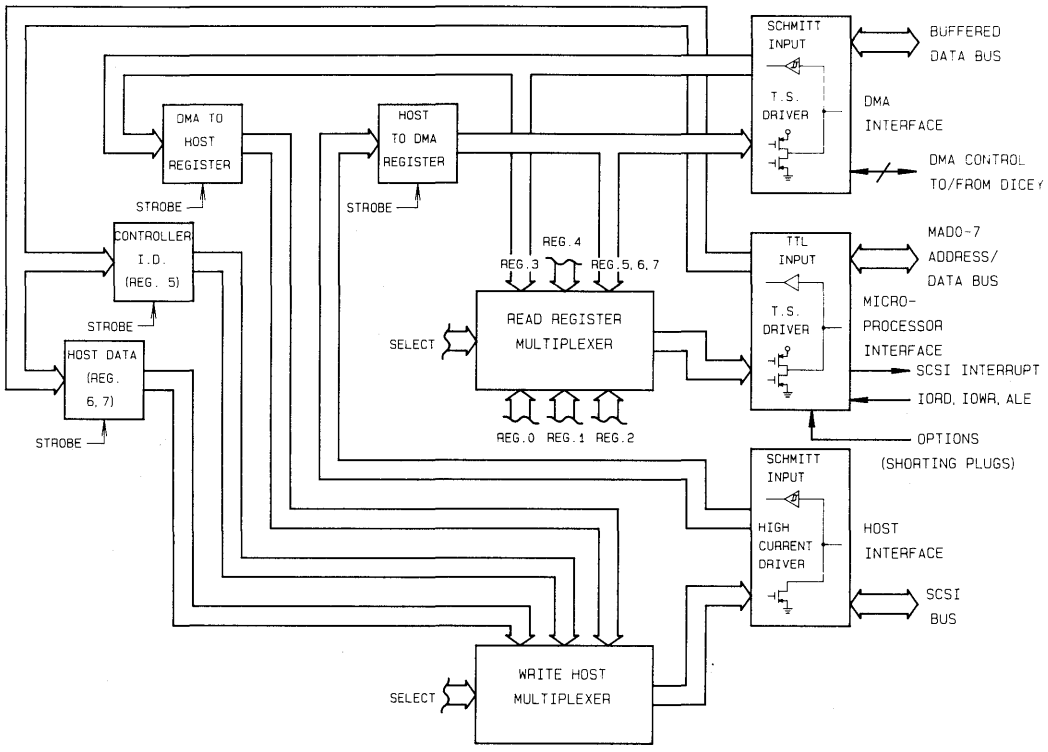


Figure 2-11: 5080 Interface Diagram

The microprocessor strobes an address into the 5080 on the falling edge of ALE (address latch enable). If the 5080 is selected, -IORD strobes data from the MAD bus; -IOWR strobes data to the MAD bus.

DICEY controls a DMA read or write to buffer RAM over the BDATA0-7 (buffered data) bus:

- When -DMA I/O is asserted, data flow is from RAM to the 5080. -DMA CLK strobes the data from the bus to the DMA to HOST register.

- When -DMA I/O is deasserted, data flow is from the 5080 to RAM. -DMAIENB turns on the 5080 drivers, placing data from the HOST to DMA register onto the bus.

Handshaking between DICEY and the 5080 is controlled by -DMA REQ (to DICEY) and -DMA ACK (from DICEY). DICEY handles addressing of the buffer RAM without intervention by the 5080. Timing for the 5080 arbitration logic is set by the 12 MHz clock from FYLO.

2.3.5 Servo Control, AMC and Servo AGC

Before reading this section, read the summary description in Section 2.2.2. Follow this explanation on Figure 2-4, a simplified block diagram of the drive. Figure 2-3 shows the disk format including details of the servo signals in the wedges.

Seeking

While a drive is seeking, the read circuit reads the servo track numbers from the data in the servo bursts, thus determining the head position. As each wedge passes under the moving head, the AMC measures the peak amplitudes of the burst's preambles, which depend upon how nearly the bursts are centered under the moving head. The microprocessor attempts to use the servo track number from the burst with the highest amplitude, because the head is over the servo track corresponding to that burst. But if the checksum bits indicate that the data is invalid, data from the next largest amplitude burst is used. If data from all bursts in a wedge is invalid, the microprocessor infers the head position from previous data, and then reads data from the bursts in the next wedge.

Track Following

While track following, the track, head and sector numbers from each wedge are stored in RAM as they are read. Also, the AMC measures the servo-burst amplitudes in order to center the head over the track: when the head is centered, the head equally overlaps the servo bursts written on each side of the data track--the microprocessor positions

the head so the AMC gives equal amplitudes for these two bursts. The difference between the burst amplitudes is a measure of how closely the head is centered; if the difference becomes too large (about one-fifth of a head width), the drive stops reading or writing.

Adaptive Gain Parameters

To improve servo operation, three adaptive gain parameters are measured during recalibration and stored in RAM. In addition, two of these values are updated while the drive is operating. See the Power-Up Sequence, Figure 2-15.

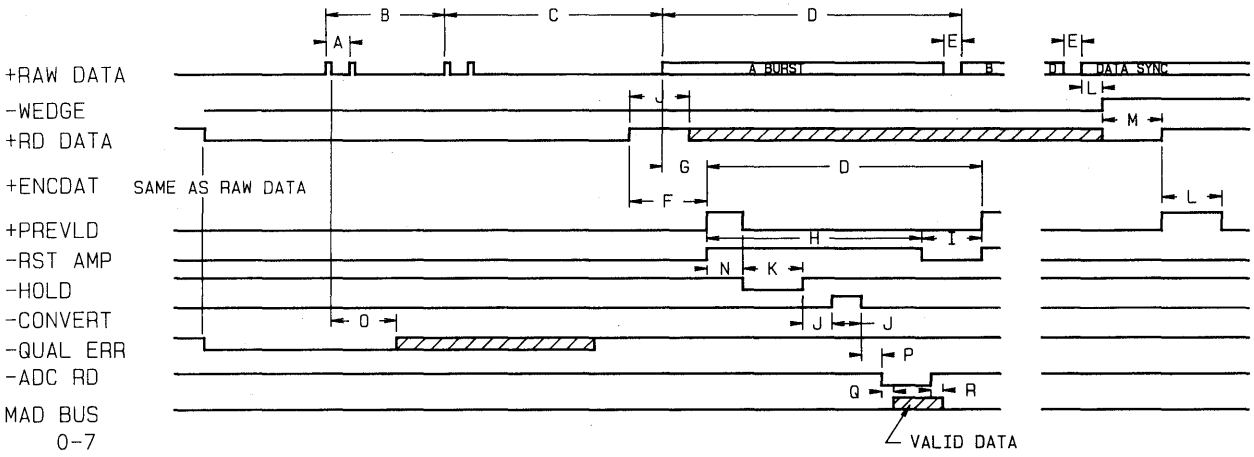
- KAG, or servo gain. This is essentially a measure of the physical head width, though it depends to a lesser extent upon other factors. Since the head width doesn't vary with temperature, KAG is measured for each head, but only once--at the middle track, during recalibration. This is a feed-forward value, used by the microprocessor to predict and compensate for burst amplitude variations when switching heads.

- NULL I, or force bias. This is the dc actuator current required to overcome forces on the actuator from bearings, windage, the flex circuit, gravity (in some orientations), and to compensate for any offset in the actuator circuitry. NULL I is measured by changing the value in small steps until the head accurately centers over the track. It is measured at the inner cylinder and outer cylinder, and is the same for all heads. Linear extrapolation between the two values accurately predicts the parameter for all cylinders. Since NULL I changes with temperature, it is constantly measured and the value in RAM is updated.

- Servo AGC, the gain of a head when reading head position data from bursts. It is measured for each head, at the inner and outer cylinders. Linear extrapolation accurately predicts the parameter at other cylinders. To correct for changes with temperature, a fixed offset from the predicted value is constantly measured, and the updated offset is stored in RAM. When reading servo data in a wedge, Servo AGC overrides the CAGC signal from U2 (B), and controls the gain of the U2 (A) AGC amplifier.

AMC Circuit Description

The AMC measures servo-burst amplitude by full-wave rectifying the signal, integrating it, and then converting it from analog to digital.



A= 400ns	H= 6.200us	O= 933ns
B= 4.200us	I= 2.600us	P= 600ns min.
C= 9.067us	J= 600ns	Q= 70ns max.
D= 8.800us	K= 1.333us	R= 60ns max.
E= 1.333us	L= 1.000us	
F= 733ns	M= 6.000us	
G= 533ns	N= 667ns	

Figure 2-12: Servo AMC and ADC Circuit Waveforms

Refer to the schematic diagrams in SECTION 3, and the waveforms in Figures 2-12, 5-1, 5-2 and 5-3. The differential signal from the AGC amplifier is +READ SIG and -READ SIG. Transistors (1, 2, 3, and 5, 4, 3) in transistor array U11 full-wave rectify the signal and convert it to a proportional current, which is mirrored by Q17 and Q18. Transistor (6, 7, 8) in U11 sinks the mirrored current when no burst is present.

At the beginning of a burst, -RST AMP is asserted, which turns off U11 transistor (12, 13, 14). In turn, this biases Q20 on and discharges C72, initializing the sample and hold integrator U12 (pins 5, 6, 7). During the preamble period of a burst, FYLO deasserts -RST AMP, allowing current from the current mirror to flow through CR5 and charge C72. The charge accumulates during an integral number of cycles of the preamble signal, until FYLO asserts +HOLD and turns on Q19, sinking the current that would otherwise flow through CR5.

BURST PEAK, the output of U12 (pin 7), is now a voltage inversely proportional to the charge on C72, and thus to the burst amplitude. When FYLO asserts -CONVERT, the AMC DAC converts this voltage to an 8-bit number. The microprocessor places it on the MAD bus by causing DICEY to assert -ADC RD.

Burst Amplitude	U12 Integrator Output	U10 ADC Output
Maximum	2.5 volts	0 (decimal)
Zero	3.7	255

Servo AGC Circuit Description

Follow this explanation on the schematics in SECTION 3.

To control the Servo AGC, the microprocessor selects AGC DAC U28 by placing 8 bits corresponding to the desired Servo AGC on the MAD bus, strobes the bits into the DAC with -DAC CS and -WR, and asserts +AGC DAC. The U12 (pins 1, 2, 3) op-amp output is 3.7 to 7.4 volts for 0 to 255 (decimal) DAC input. The DAC output is divided and becomes the input to Q10, an emitter follower. Transistor array U27 is switched on when -WEDGE is asserted, and then mirrors the current from Q10 and converts it to a high-current output. This output connects to CAGC, and overrides the CAGC signal produced by pulse detector U2 (B). Therefore, the Servo AGC sets the U2 (A) amplifier gain when reading bursts, but the U2 (B) circuit sets the amplifier gain when reading data from the user areas.

2.3.6 Actuator Positioning Circuit

While reading the following, refer to the schematics in SECTION 3. To control the actuator, the microprocessor calculates the desired actuator current, places 8 bits corresponding to the current on the MAD bus, strobes the bits into actuator DAC U3 with -DAC CS and -WR, and asserts +ACT DAC. The output of op-amp U21 is 3.7 volts to 7.4 volts for 0 to 255 (decimal) DAC input.

U5 is another voltage amplifier; its output swings around the reference voltage--the full range of positive and negative actuator currents is obtained even though a negative supply is not available. A DAC output of 128 (decimal) corresponds to zero (nominal) actuator current. While seeking, the gain of U5 is four times its gain when settling and following. The gain is switched by +GAIN LOW, which turns on Q11 and connects R72 into the feedback path.

U4 (A) is an error amplifier, a part of the actuator driver chip U4. Driver stage U4 (B) has a differential output. Power transistors Q12 through Q15 limit the dissipation in U4 (B), and force through the actuator coil a differential current that is proportional to the output of the error amplifier. U5 senses the current as the difference voltage across R42 and R43, amplifies it by four, and closes the loop, giving accurate positioning.

The R-C network from output to input of U4 (A) compensates for the actuator coil time constant; the R-C network from U4 (A) output to ground plus C62 and C63 compensate U4 (B). CR13 - CR16 suppress inductive transients across the actuator coil.

2.3.7 Read/Write Circuit

Read

Follow this circuit description on Figure 2-4, a block diagram of the drive, and the schematics in SECTION 3. The waveforms are shown in Figure 2-13.

The alternating magnetic fields on the disk generate a differential voltage across the coil in the head selected by +BUF HS0 - +BUF HS2. This voltage is preamplified by the chip in the flex circuit (giving RDX and RDY), and ac coupled to the AGC amplifier, U2 (A), part of the 8464 pulse detector U2. The AGC amplifier output is filtered by a balanced five pole filter that slims the pulse to reduce shouldering errors. Q1, Q9, Q2, and Q16 drive the filter, which is terminated in R57 and R63. Q23 and Q26 are emitter followers that couple the filter output to the U2 (B) pulse detector inputs.

The AGC circuit samples the filtered differential signal, and controls the U2 (A) amplifier gain to keep the average peak-to- peak amplitude constant (actually, four times the voltage applied to VREF). C9 and R9 set the averaging time constant so the gain decreases rapidly for high peak signal amplitudes and increases more slowly when the signal amplitude is low.

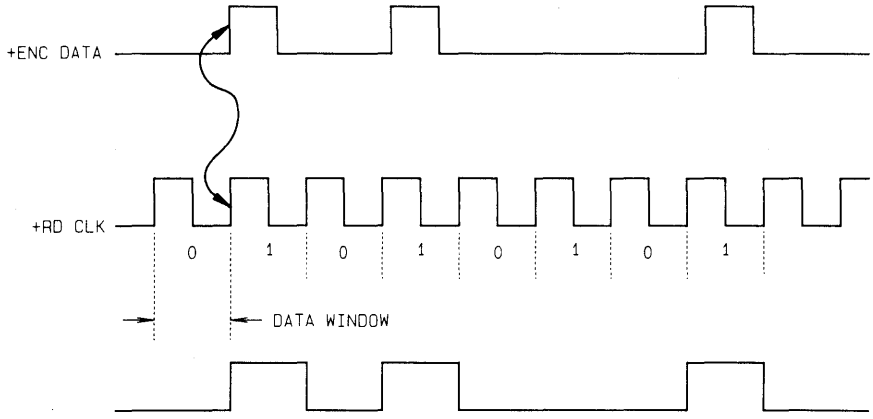


Figure 2-13: Read Circuit Waveforms

Each signal peak corresponds to a magnetic transition written on the disk. The 8464 first differentiates the filtered signal to convert the peaks to zero crossings with a high rate of change of voltage with time, easily detected. Noise pulses are suppressed by qualifying the zero crossings: to qualify, they must be caused by alternating positive and negative peaks of the filtered, but undifferentiated signal that exceed the level set by VHYS. Qualified zero crossings trigger a one-shot, producing a pulse for each signal peak. This is the output signal, +RAW DATA. C7 sets the pulse width, and R1, C1 set the differentiation time constant.

When no data is being read, AND gate U23 (pin 12) keeps the U1 PLL output (+RD CLK) locked to the 15 MHz clock input, thus reducing the PLL synchronization time. FYLO predicts a preamble and asserts +READ GATE twice per sector: once at the A burst preamble, and again at the user data preamble. FYLO asserts +PREVLD whenever the head should be over a valid preamble, and DICEY then asserts +PLL HBW to hold the PLL in a high gain tracking mode and allow fast phase lock onto +ENCODED DATA, which is buffered +RAW DATA. Later, while track following, DICEY de-asserts +PLL HBW for lower PLL gain and less jitter.

As the preamble is being read, +READ CLK quickly synchronizes to the positive-going transitions of +ENCODED DATA. DICEY strobes +RD DATA with +READ CLK to determine which bit cells contain encoded data

pulses, and then transforms this data from 2/3 RLL (1,7) encoded data to an 8-bit data byte. The byte is passed from DICEY to buffer RAM in a DMA transfer.

R17, R18, C20, and C21 set the PLL gain and bandwidth. C22 sets the VCO frequency, and R21 the VCO operating current. C17, C18, and R20 set the PLL loop bandwidth and damping, and integrate the PLL charge pump current. R19, C15, and C16 compensate for phase shift, and are selected for the 10 Mbit/sec data rate.

Write

See the description of the Flex Circuit, Section 2.2.8, for an outline of write circuit operation. In write mode, data received by the 5080 SCSI Controller is stored in RAM and passed to DICEY via DMA. DICEY encodes the data from its 8-bit form to a serial stream of 2/3 RLL (1,7) coded data.

DICEY asserts -WR GATE when it detects a user area, thereby switching the flex circuit chip from preamplifier to write driver. U20 contains six non-inverting buffers, used to improve signal immunity to noise: the inputs are 1A - 6A; the corresponding outputs are 1Y - 6Y.

Write current in the head is proportional to the current from WRITE CURRENT to ground. The microprocessor compensates for the lower output of the outer tracks: through DICEY, it asserts AUX 5, turning on Q21, inserting R22 in parallel with R23 and thus increasing WRITE CURRENT. On a reset, POR B turns off Q22, reducing WRITE CURRENT to near zero.

2.3.8 FYLO Timing Controller IC, and Xtal Oscillators

FYLO is a custom IC proprietary to Quantum that incorporates a number of timing functions. See device U9 on the schematics in SECTION 3 for the pinout. FYLO performs the following functions:

- Accepts +RAW DATA, and buffers the signal to produce +ENCODED DATA.
- Derives the 2 MHz clock from the 12 MHz clock, and buffers the 2 MHz, 12MHz, and 15 MHz clocks.
- Outputs -WEDGE to identify the wedge area.
- Controls the servo AMC sample and hold timing with outputs -RST AMP and +HOLD.
- Begins servo-burst A/D conversion by asserting -CONVERT.

- Asserts +READ GATE to indicate when data should be processed through the read data synchronizer.

- Asserts +PREVLD to indicate to DICEY that a valid preamble should be present.

- Asserts +QUAL ERR to indicate to the microprocessor and DICEY that the wedge area does not meet the qualification criteria, which are: (1) sector and echo pulses appear at the correct times, and (2) no pulses are detected in the three dc erase fields.

  Note: to avoid overwriting the servo tracks, writing is inhibited in a wedge. Moreover, the microprocessor inhibits writing data in the sector if QUAL ERR is asserted.

Several variations of the crystal oscillator circuits have been manufactured; the PCB accomodates either (1) a 12 MHz crystal driven by the microprocessor, with a 15 MHz crystal and associated driver IC in a metal can at U25, or (2) a dual- frequency 12 MHz and 15 MHz crystal oscillator module with driver ICs in a metal can at U25. AND gate (pins 3 - 6) in U23 is required only for option (1).

2.3.9 DICEY Data Controller IC

DICEY is a custom data controller IC, a 100-pin device proprietary to Quantum and designed by Quantum for the Q200 series disk drives. See U14 on the schematics in SECTION 3 for the pinout and Figure 2-14 for the block diagram. All pins conform to standard 5 V logic levels. DICEY performs several functions, listed below, including miscellaneous "glue logic," thereby significantly reducing the number of chips on the PCB, and improving the drive reliability.

DICEY has these features:

- Controlled by microprocessor, which communicates with DICEY over the MAD bus.

- Microprocessor sees DICEY as a set of 34 registers to which it can write to control data transfer, or read to determine status, etc.

- Performs serial-to-parallel and parallel-to-serial conversions.

- Encodes all data written to disk and decodes all data read from the disk, using a 2/3 RLL (1,7) code. The notation means that the code maps two data bits into three code bits,

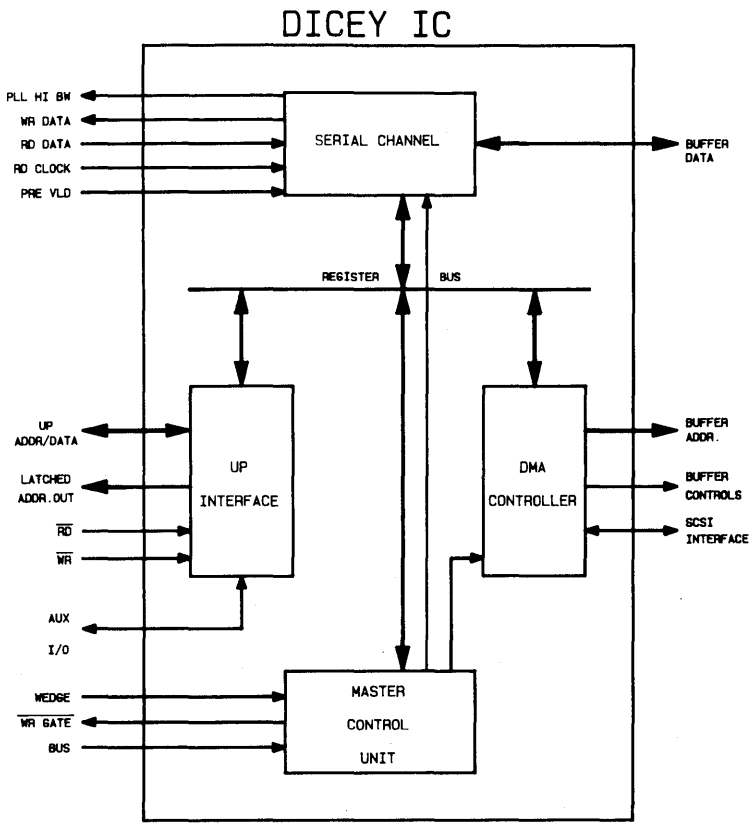


Figure 2-14: DICEY Block Diagram

and that the encoded bit stream has between one and seven 0 bits between each 1 bit.

- Generates a sync time-out error if sync is not detected after pll locks on the preamble (an alternating field of 1s and 0s).

- Detects sync pattern (100100) and generates a sync error if there is a drop out, drop in, or shifted bit.

- Controls access to buffer RAM via DMA transfers, in this priority: (1) disk, including user data and servo position data, (2) microprocessor, and (3) 5080 SCSI controller.

- DMA cycles are controlled by a state machine in the Master Control Unit, synchronized to the 15 MHz clock from FYLO.

- Disk and write functions are controlled by a state machine in the serial channel, synchronized to READ CLOCK.

- Can read and write to buffer RAM (to and from both the disk and the SCSI bus) at the burst transfer rate of 1.25 Mbytes/sec.

- Checks buffer RAM during initialization.
- Generates parity and checks parity, for buffer RAM.
- Refreshes Buffer RAM.
- Contains latches for the low-byte EPROM address (outputs LAD 0-7).
- Provides additional microprocessor I/O (pins AUX 0-7).
- Contains 12-byte ECC syndrome generator. (See Section 4.2.1).

2.3.10 Microprocessor and EPROM

Q250 and Q280 drives use 12 MHz industry-standard 8-bit microprocessors as shown in the following table:

Table 2-3: Microprocessors and Buffer RAM

DisCache	Microprocessor	Internal Data RAM	FIFO Buffer RAM	Buffer
No	8031	128 X 8	16 Kbytes	14 KBytes
Yes	8032	256 X 8	64 Kbytes	60 KBytes

The Internal data RAM is used for look-up tables that require fast access. Communication with other devices is over the 8-bit MAD bus. Firmware for the drive is stored in a 32 KB EPROM, a 27256, located at U15. There are four different EPROMS: for Q250 and Q280, each with and without DisCache.

2.4 Power-Up Sequence/Recalibration

This section explains the special features of the power-up sequence, which is shown in Figure 2-15.

After RAM tests and circuit initialization, the drive can respond to the SCSI bus, although the drive cannot read or write for several seconds.

No mechanical or absolute position information is used in the Q250/Q280, as the actuator finds its position by reading information from the servo wedges. At power-up, the position is determined by seeking toward the middle of the disk, then braking and reading the wedges while the radial velocity is zero.

Once the actuator position is known, the drive is recalibrated: the actuator seeks to the outer, middle, and inner tracks, and at each position, the peak amplitudes of the servo bursts are read. From this information, the adaptive gain parameters are calculated and written into buffer RAM. The W-list, or working list of defective sectors, is then read from reserved tracks into buffer RAM. A duplicate copy of the list is stored on each surface so that it is always available, even if one or more copies is damaged. Finally, the drive seeks to cylinder 0, and is ready.

2.5 Read Command Sequence

This Section explains the special features of the Read Command Sequence, Figure 2-16. For additional information, see the Q200 Series Programmers Manual.

The READ command contains the starting logical block address and the transfer length in blocks. Before reading each sector, the Q250/Q280 checks the defect list and seeks to the correct position. After each sector is read into buffer, the data is checked for correctness; the action taken is that specified by the Error Recovery Parameters of the MODE SELECT command.

2.6 Write Command Sequence

This Section explains the special features of the Write Command Sequence, Figure 2-17. For additional information, see the Q200 Series Programmers Manual.

The WRITE command contains the starting logical block address and the transfer length in blocks. Before writing each sector, the Q250/Q280 checks the defect list and seeks to the correct position.

Writing to disk doesn't start until a complete block is available in the buffer. Then, the Q250/Q280 writes to the disk from buffer, and transfers data from the SCSI bus to buffer almost simultaneously (actually interleaved, a byte at a time). When the full transfer length of data has been transferred from the SCSI bus to the buffer, and from the buffer to the disk, the transfer is complete and the Q250/Q280 sends Status and Message to the host.

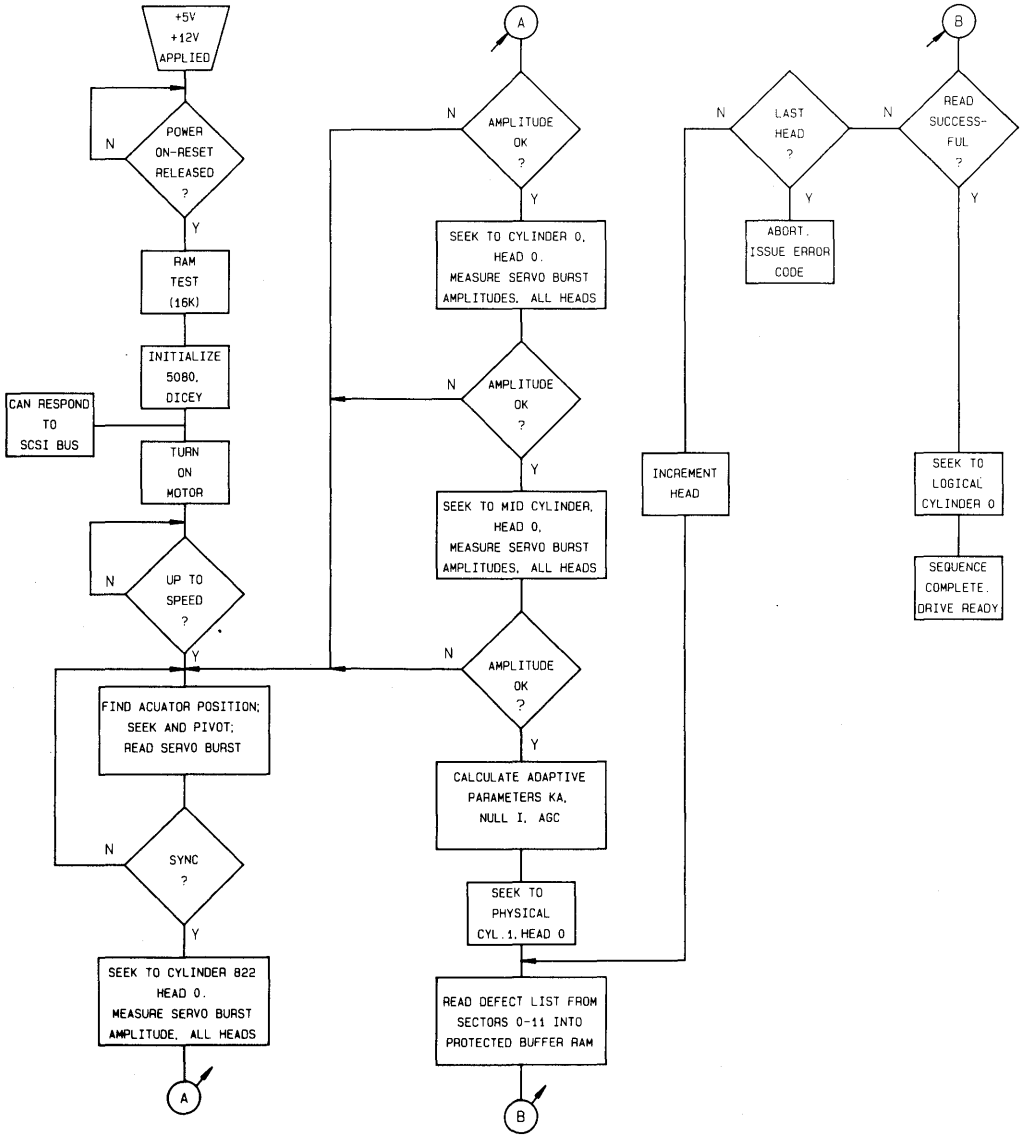


Figure 2-15: Power-Up Sequence

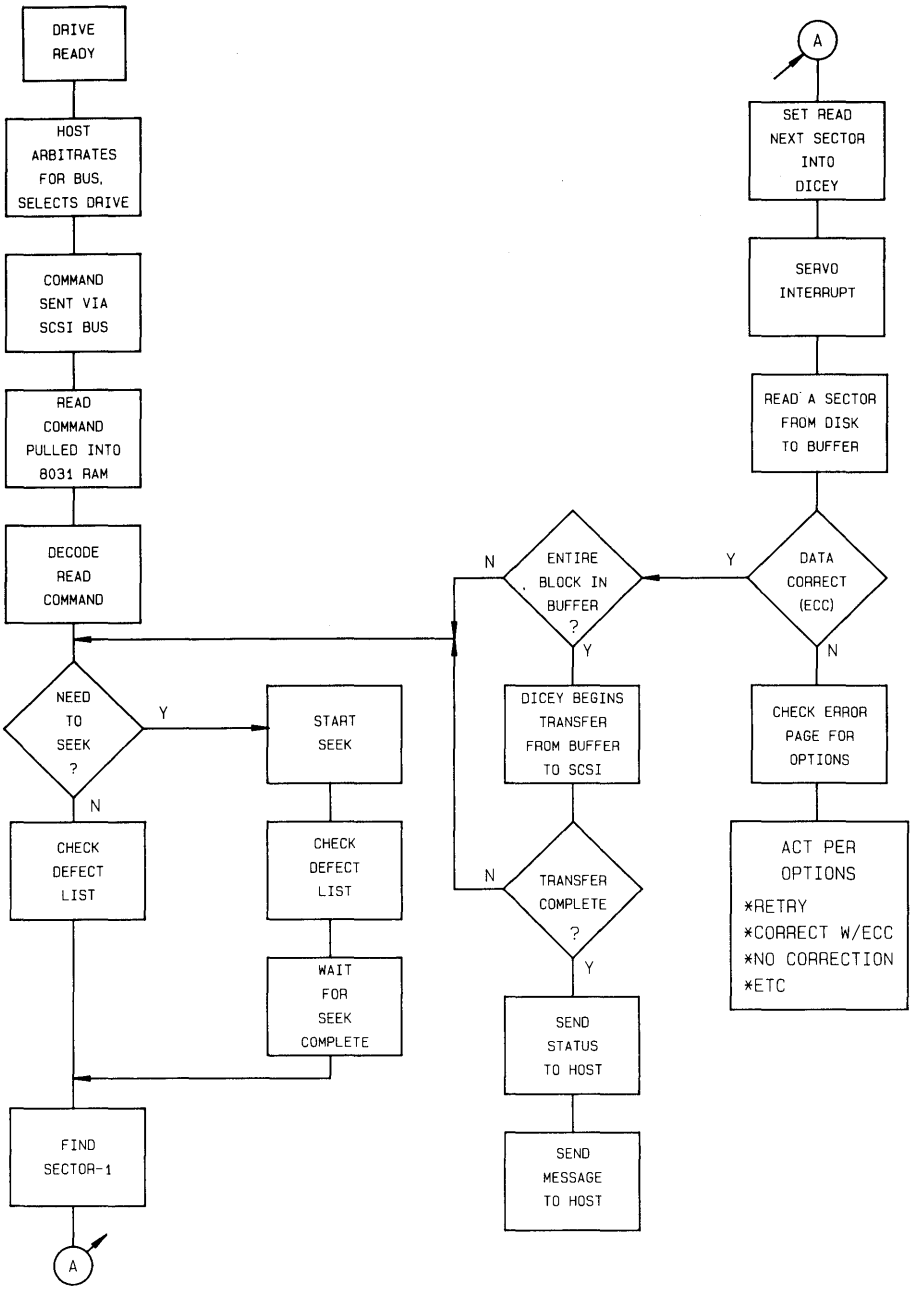


Figure 2-16: Read Command Sequence

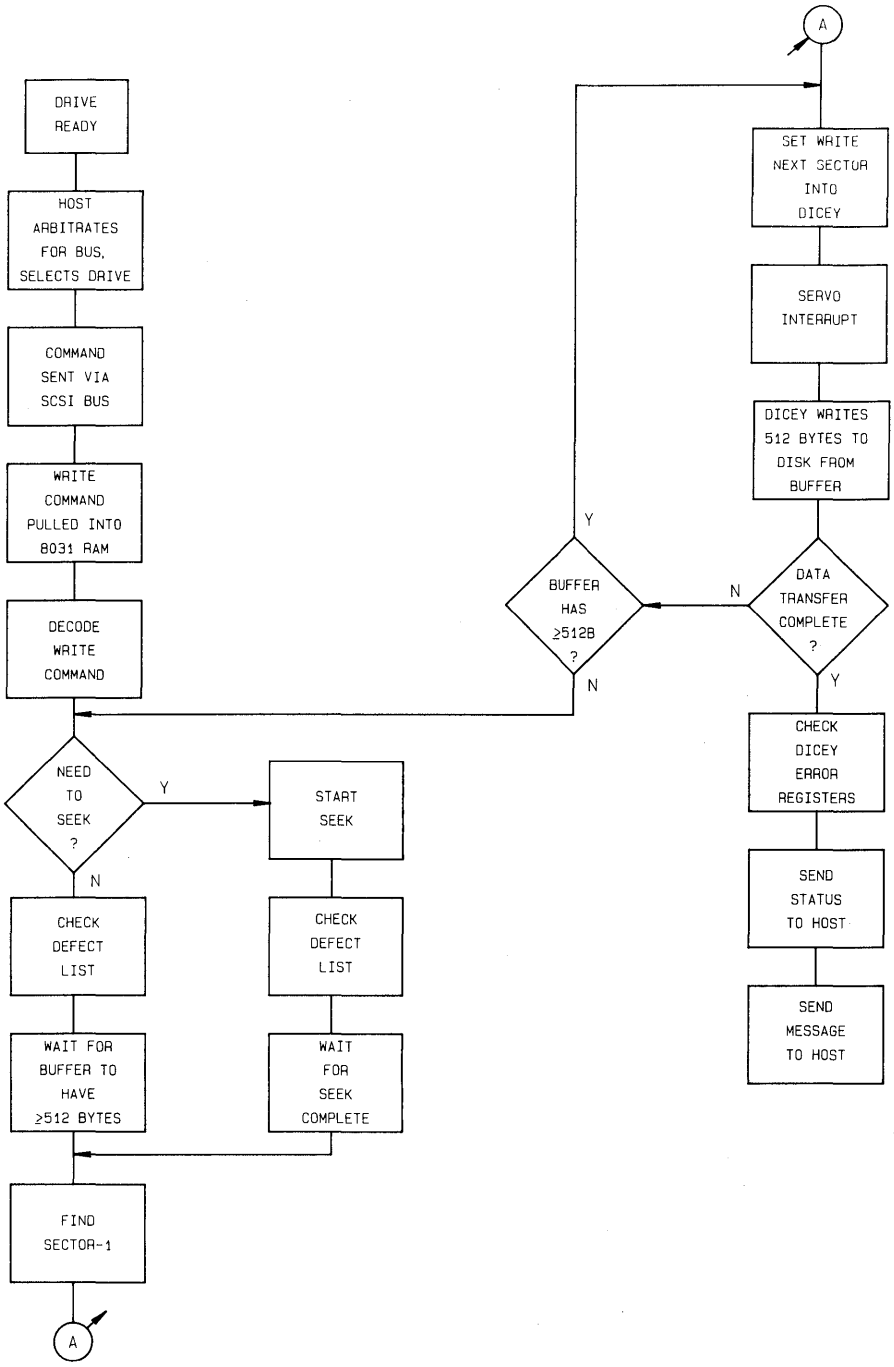


Figure 2-17: Write Command Sequence

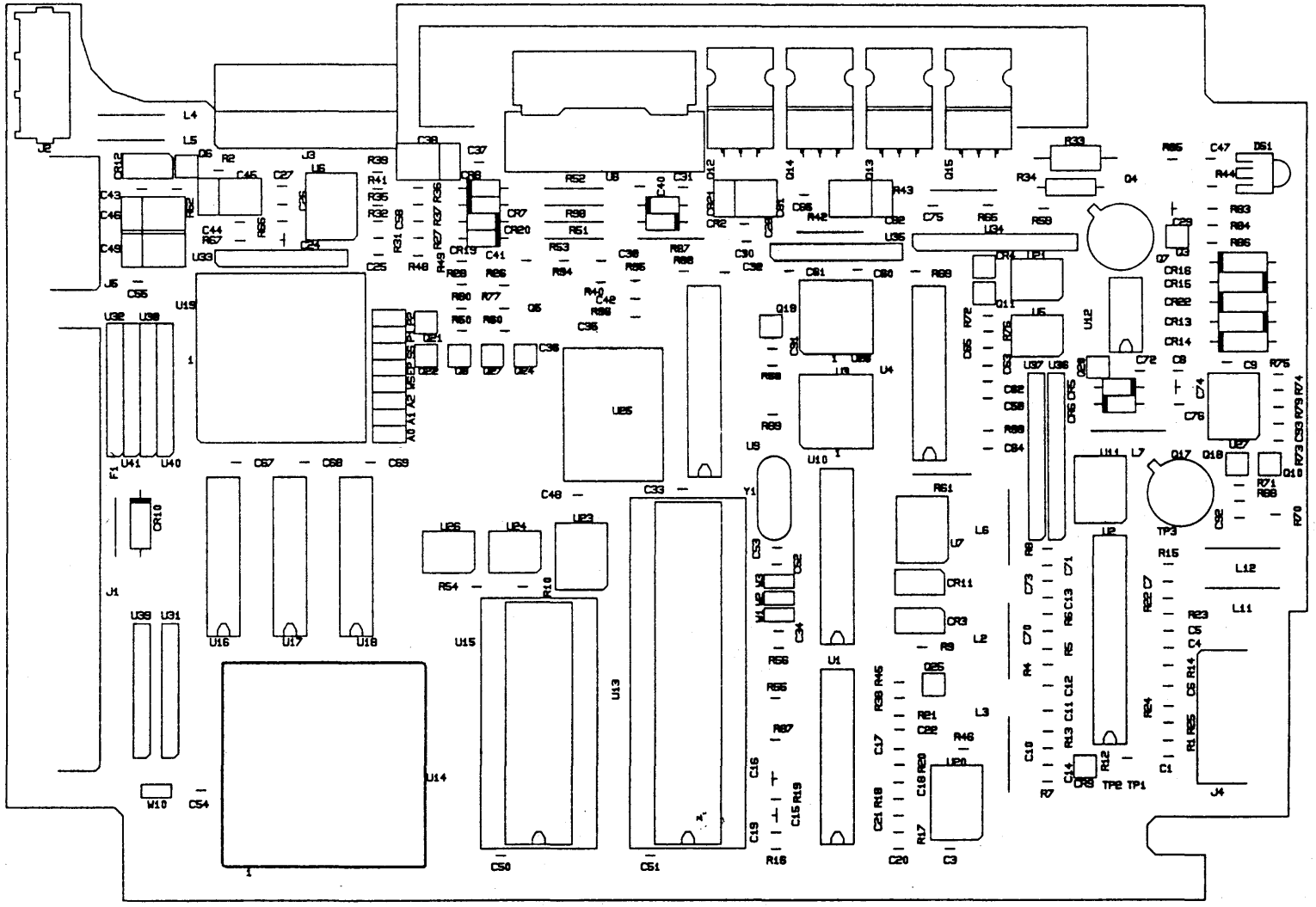
SECTION 3. Q200 SERIES ENGINEERING DRAWINGS

The following drawings illustrate the Q200 Series Printed Circuit Boards for several revisions. Depending on the specific PCB that is applicable, please refer to PCB-7, PCB-8, or PCB-9 drawing groups.

PCB-7 Engineering Drawings

PCB-8 Engineering Drawings

PCB-9 Engineering Drawings



QUANTUM CORP.
Q200 PCB 7 FAB 10-22007
SILKSCREEN
ARTWORK 30-22007 REV 02
CRD A026 4-4-86 KRL

Figure 3-1: Printed Circuit Board Parts Locations

TES: UNLESS OTHERWISE SPECIFIED.

THIS SCHEMATIC APPLIES TO ASSEMBLY 20-22007
OF THE SAME REVISION LEVEL.

ALL RESISTOR VALUES ARE IN OHMS.
ALL CAPACITOR VALUES ARE IN MICROFARADS.
ALL INDUCTOR VALUES ARE IN MICROHENRIES.

SHORTING PLUG OPTIONS ARE SHOWN AS:

—o o— OPEN CONNECTION

—o-o— TRACE OR WIRE CONNECTION

—o-o— SHORTING PLUG INSTALLED

POWER CONNECTIONS

I.C.	REF	5 V	12 V	GROUND
DP8455	U1	20	NONE	10, 19
DP8464	U2	NONE	9	17, 20
DAC0832	U3 U28	19	20	3, 8
EL2017	U4	NONE	20	10
LM358A	U5	NONE	8	4
LM339	U6	3	NONE	12
7406	U7	14	NONE	7
HA13426	U8	NONE	1	5, 7
TMG CTLR	U9	12, 22	NONE	1, 11, 18
AD7820	U10	7, 20	NONE	10, 13
3046	U11	NONE	NONE	NONE
MC34072AP	U12	NONE	8	4
8031	U13	40	NONE	20
DATA CTLR	U14	8, 17, 25, 33 50, 58, 68, 75, 86, 100	NONE	3, 13, 20, 28, 38, 45, 53, 63, 73, 80, 88
27256	U15	28	NONE	14
4416	U16 U17 U18	9	NONE	1, 18
5080	U19	20, 49, 65	NONE	1, 12, 17, 23 35, 46, 52, 57, 61, 62, 64
74LS365A	U20	16	NONE	8
LM358A	U21	NONE	8	4
74HC11	U23	14	NONE	7
75453	U24 U26	8	NONE	4
OSC	U25	11, 14	NONE	7
220 ohm/ 330 ohm	U31 U32 U38	NONE	NONE	1
100K ohm	U39 U40 U41	1	NONE	NONE

CONNECTOR PIN ASSIGNMENTS

REF.	PIN	SIGNAL NAME	PAGE
J1	01	GND	3R
	02	-DB0	3R
	03	GND	3R
	04	-DB1	3R
	05	GND	3R
	06	-DB2	3R
	07	GND	3R
	08	-DB3	3R
	09	GND	3R
	10	-DB4	3R
	11	GND	3R
	12	-DB5	3R
	13	GND	3R
	14	-DB6	3R
	15	GND	3R
	16	-DB7	3R
	17	GND	3R
	18	-DBP	3R
	19	GND	3R
	20	GND	3R
	21	GND	3R
	22	GND	3R
	23	GND	3R
	24	GND	3R
	25	N/C	

REF.	PIN	SIGNAL NAME	PAGE
J1	26	TERMPWR	3R
	27	GND	3R
	28	GND	3R
	29	GND	3R
	30	GND	3R
	31	GND	3R
	32	-ATN	3R
	33	GND	3R
	34	GND	3R
	35	GND	3R
	36	-BSY	3R
	37	GND	3R
	38	-ACK	3R
	39	GND	3R
	40	-RST	3R
	41	GND	3R
	42	-MSG	3R
	43	GND	3R
	44	-SEL	3R
	45	GND	3R
	46	-C/D	3R
	47	GND	3R
	48	-REQ	3R
	49	GND	3R
	50	-I/O	3R

REF.	PIN	SIGNAL NAME	PAGE
J2	01	12 V DC	1L
	02	12 V RT	1L
	03	5 V RTN	1L
	04	5 V DC	1L

REF.	PIN	SIGNAL NAME	PAGE
J3	01	HALL GND	2R
	02	HALL 1+	2L
	03	HALL 1-	2L
	04	HALL 2+	2L
	05	HALL 2-	2L
	06	HALL 3+	2L
	07	HALL 3-	2L
	08	HALL 12 V	2R
	09	COIL A	2R
	10	COIL B	2R
	11	COIL C	2R

REF.	PIN	SIGNAL NAME	PAGE
J4	01	ACT COIL2	2R
	02	ACT COIL1	2R
	03	FIL 12 V	1R
	04	GND	1R
	05	+BUF WR DATA	3R
	06	+WR UNSAFE	3L
	07	GND	1R
	08	FIL 5 V	1R
	09	+BUF HS1	3R
	10	+BUF HS2	3R
	11	RDX	2L
	12	+BUF HS0	3R
	13	WR CURRENT	2R
	14	RDY	3R
	15	GND	1R
	16	-BUF WR GATE	3R

REF.	PIN	SIGNAL NAME	PAGE
J5	01	C AGC	2L
	02	BURST PEAK	3R
	03	SET HYST	3L
	04	DET REF	2L
	05	-WEDGE	3R
	06	GND	1L
	07	5 V	1L
	08	12 V	1L
	09	12 V	1L
	10	5 V	1L
	11	GND	1L
	12	N/C	
	13	+ENCODED DATA	3R
	14	+DATA LOCK	3R
	15	N/C	
	16	+TEST RD CLK	3R

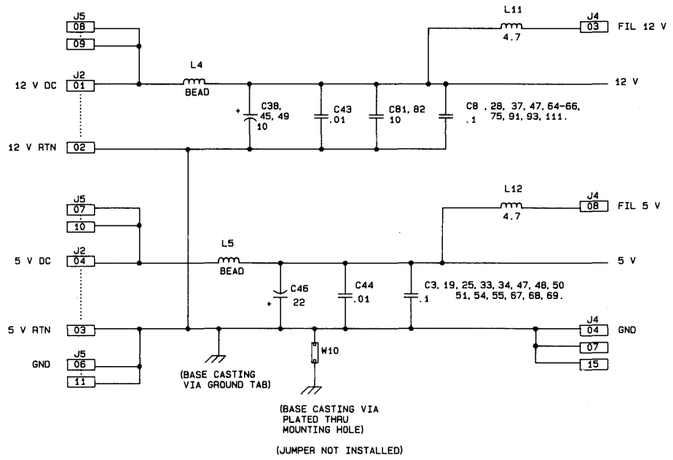


Figure 3-2
Sheet 1

File: 8022007A
Drwng: NAM NG
REV: L

Page 01 of 03
Date: 4/10/87

MUST CONFORM TO ENGINEERING SPEC.

MATERIAL

TOLERANCE UNLESS OTHERWISE NOTED

LINEAR: .XX
.XXX

CASE DEPTH

HARDNESS

ANGULAR:

SURFACE TREATMENT

CORNERS EDGES BROKEN: OUTSIDE MAX, INSIDE MAX

Quantum

TITLE SCHEMATIC, Q200 PCB7

DETAIL

DESIGN

APPRO

RELEASED FOR ASSEMBLY

SHEET 1 OF 3

D

SCALE NONE

80-22007

REV

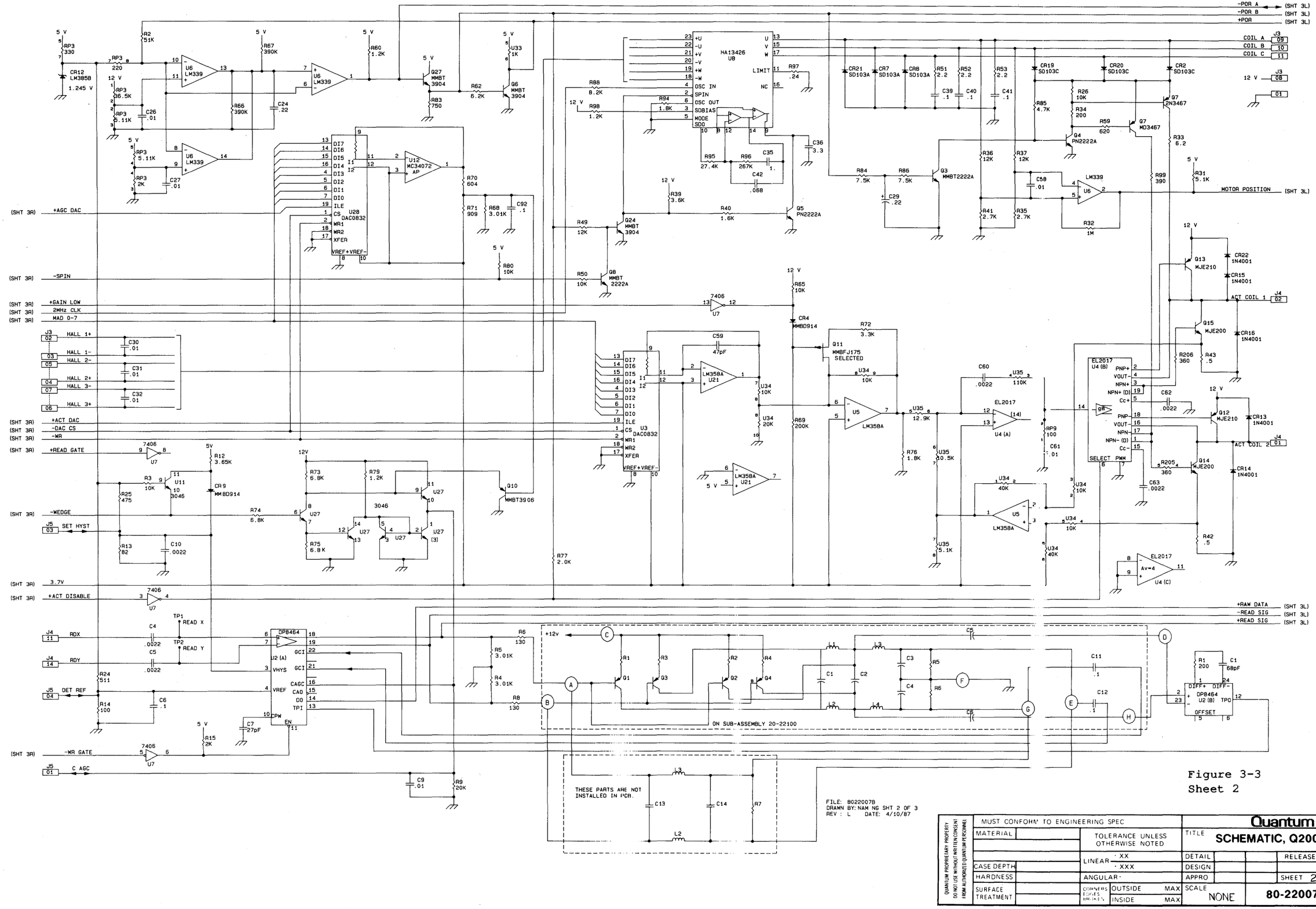


Figure 3-3
Sheet 2

QUANTUM PROPRIETARY PROPERTY DO NOT USE WITHOUT WRITTEN CONSENT FROM AUTHORIZED QUANTUM PERSONNEL	MUST CONFORM TO ENGINEERING SPEC		TITLE	Quantum SCHEMATIC, Q200 PCB7
	MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DETAIL	RELEASED FOR ASSEMBLY
	CASE DEPTH	LINEAR .XX .XXX	DESIGN	
	HARDNESS	ANGULAR ·	APPRO	SHEET 2 OF 3 D
	SURFACE TREATMENT	CORNERS EDGES BREAKS OUTSIDE MAX INSIDE MAX	SCALE NONE	80-22007 REV

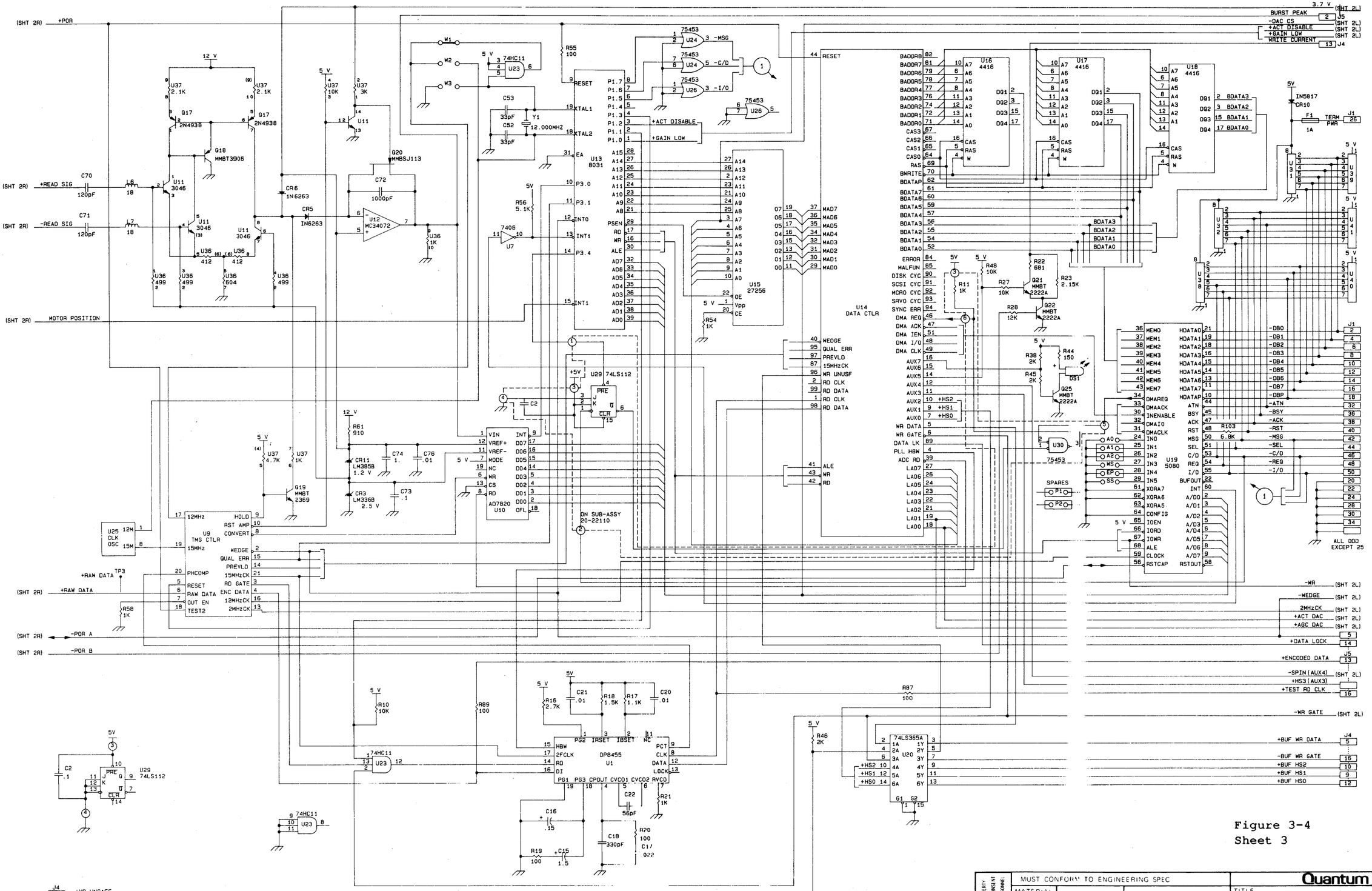


Figure 3-4
Sheet 3

File: 8022007C
Drwng: NAM NG
Rev: L

Page 03 of 03
Date: 4/10/87

QUANTUM PROPRIETARY PROPERTY: DO NOT USE WITHOUT WRITTEN CONSENT FROM AUTHORIZED QUANTUM PERSONNEL

MUST CONFORM TO ENGINEERING SPEC

MATERIAL

TOLERANCE UNLESS OTHERWISE NOTED

LINEAR .XX / .XXX

ANGULAR

CASE DEPTH

HARDNESS

SURFACE TREATMENT

CORNER EDGES BROKEN OUTSIDE MAX / INSIDE MAX

Quantum

TITLE SCHEMATIC, Q200 PCB7

DETAIL | RELEASED FOR ASSEMBLY

DESIGN

APPRO

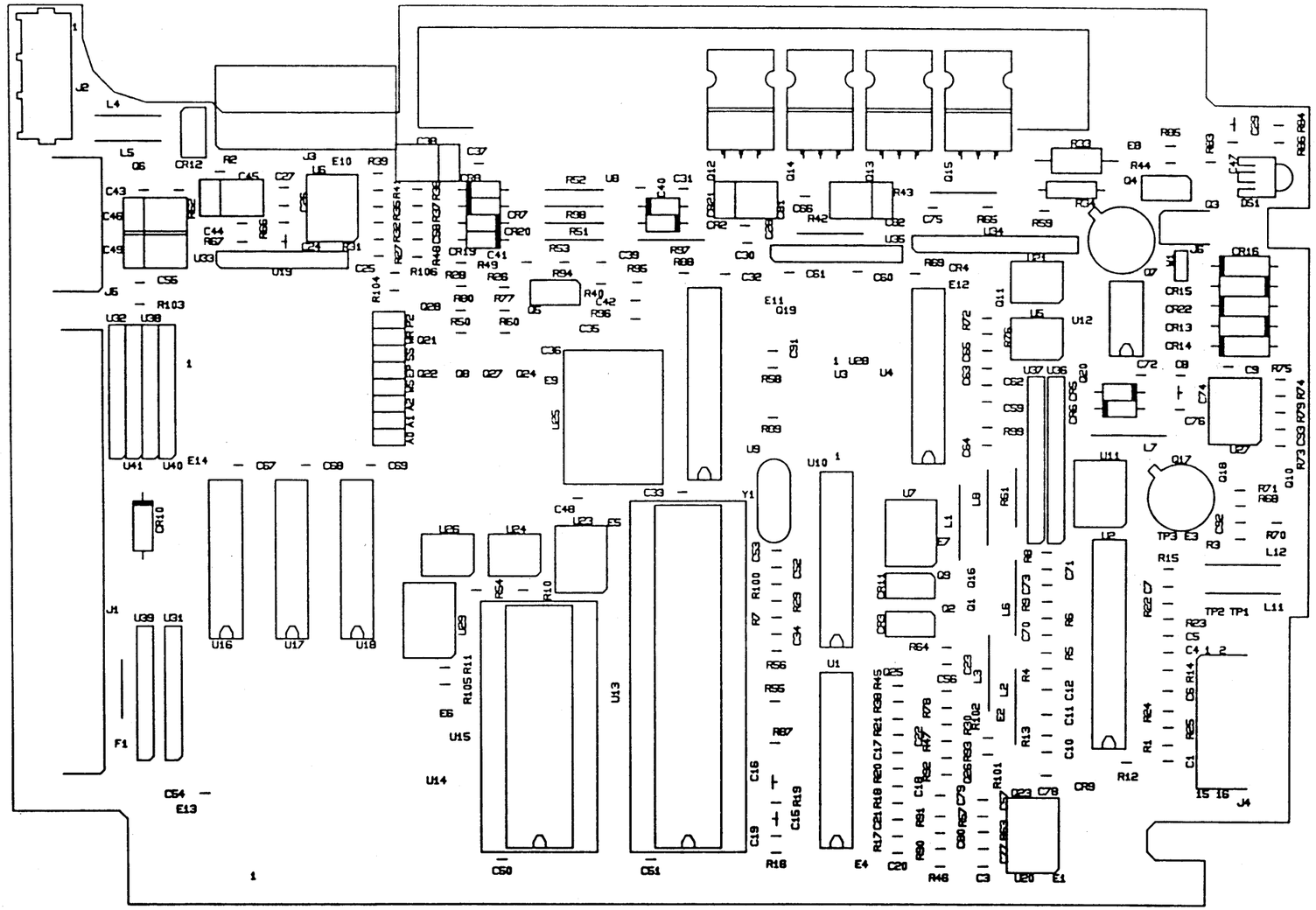
SHEET 3 OF 3

D

SCALE NONE

80-22007

REV



QUANTUM CORP.
Q200 PCB 8 FAB 10-22008
SILKSCREEN
ARTWORK 30-22008 REV 02
CRD A038B KRL 8-6-86

Figure 3-5: Printed Circuit Board Parts Locations

'ES: UNLESS OTHERWISE SPECIFIED.

THIS SCHEMATIC APPLIES TO ASSEMBLY 20-22008 OF THE SAME REVISION LEVEL.

ALL RESISTOR VALUES ARE IN OHMS,
ALL CAPACITOR VALUES ARE IN MICROFARADS,
ALL INDUCTOR VALUES ARE IN MICROHENRIES.

R29, 100 ARE NOT INSTALLED IN THIS ASSEMBLY.

SHORTING PLUG OPTIONS ARE SHOWN AS FOLLOWS:

1 o o 2 OPEN CONNECTION

1 o-o 2 SHORTING PLUG INSTALLED

POWER CONNECTIONS

I.C.	REF	5 V	12 V	GROUND
DP8455	U1	20	NONE	10, 19
DP8464	U2	NONE	9	17, 20
DAC0832	U3 U28	19	20	3, 8
EL2017	U4	NONE	20	10
LM358A	U5	NONE	8	4
LM339	U6	3	NONE	12
7406	U7	14	NONE	7
HA13426	U8	NONE	1	5, 7
TMG CTLR	U9	12, 22	NONE	1, 11
AD7820	U10	7, 20	NONE	10, 13
3046	U11	NONE	NONE	NONE
MC34072AP	U12	NONE	8	4
8031	U13	40	NONE	20
DATA CTLR	U14	8, 17, 25, 33 50, 58, 68, 75, 86, 100	NONE	3, 13, 20, 28, 38, 45, 53, 63, 73, 80, 88
27256	U15	28	NONE	14
4416	U16 U17 U18	9	NONE	1, 18
5080	U19	20, 49, 65	NONE	1, 12, 17, 23 35, 46, 52, 57, 61, 62, 64
74LS365A	U20	16	NONE	8
LM358A	U21	NONE	8	4
74HC11	U23	14	NONE	7
75453	U24 U26	8	NONE	4
OSC	U25	11, 14	NONE	7
220 ohm/ 330 ohm	U31 U32 U38	NONE	NONE	1
100k ohm	U39 U40 U41	1	NONE	NONE
74LS112	U29	16	NONE	8

CONNECTOR PIN ASSIGNMENTS

REF.	PIN	SIGNAL NAME	PAGE
J1	01	GND	3R
	02	-DB0	3R
	03	GND	3R
	04	-DB1	3R
	05	GND	3R
	06	-DB2	3R
	07	GND	3R
	08	-DB3	3R
	09	GND	3R
	10	-DB4	3R
	11	GND	3R
	12	-DB5	3R
	13	GND	3R
	14	-DB6	3R
	15	GND	3R
	16	-DB7	3R
	17	GND	3R
	18	-DBP	3R
	19	GND	3R
	20	GND	3R
	21	GND	3R
	22	GND	3R
	23	GND	3R
	24	GND	3R
	25	N/C	

REF.	PIN	SIGNAL NAME	PAGE
J1	26	TERMPWR	3R
	27	GND	3R
	28	GND	3R
	29	GND	3R
	30	GND	3R
	31	GND	3R
	32	-ATN	3R
	33	GND	3R
	34	GND	3R
	35	GND	3R
	36	-BSY	3R
	37	GND	3R
	38	-ACK	3R
	39	GND	3R
	40	-RST	3R
	41	GND	3R
	42	-MSG	3R
	43	GND	3R
	44	-SEL	3R
	45	GND	3R
	46	-C/D	3R
	47	GND	3R
	48	-REQ	3R
	49	GND	3R
	50	-I/O	3R

REF.	PIN	SIGNAL NAME	PAGE
J2	01	12 V DC	1L
	02	12 V RT	1L
	03	5 V RTN	1L
	04	5 V DC	1L

REF.	PIN	SIGNAL NAME	PAGE
J3	01	HALL GND	2R
	02	HALL 1+	2L
	03	HALL 1-	2L
	04	HALL 2+	2L
	05	HALL 2-	2L
	06	HALL 3+	2L
	07	HALL 3-	2L
	08	HALL 12 V	2R
	09	COIL A	2R
	10	COIL B	2R
	11	COIL C	2R

REF.	PIN	SIGNAL NAME	PAGE
J4	01	ACT COIL2	2R
	02	ACT COIL1	2R
	03	FIL 12 V	1R
	04	GND	1R
	05	+BUF WR DATA	3R
	06	+WR UNSAFE	3L
	07	GND	1R
	08	FIL 5 V	1R
	09	+BUF HS1	3R
	10	+BUF HS2	3R
	11	RDX	2L
	12	+BUF HS0	3R
	13	WR CURRENT	2R
	14	RDY	3R
	15	GND	1R
	16	-BUF WR GATE	3R

REF.	PIN	SIGNAL NAME	PAGE
J6	01	LED RETURN	3R
	02	LED SOURCE	3R
	03	LED RETURN	3R

REF.	PIN	SIGNAL NAME	PAGE
J5	01	C AGC	2L
	02	BURST PEAK	3R
	03	SET HYST	3L
	04	DET REF	2L
	05	-WEDGE	3R
	06	GND	1L
	07	5 V	1L
	08	12 V	1L
	09	12 V	1L
	10	5 V	1L
	11	GND	1L
	12	N/C	
	13	+ENCODED DATA	3R
	14	+DATA LOCK	3R
	15	N/C	
	16	+TEST RD CLK	3R

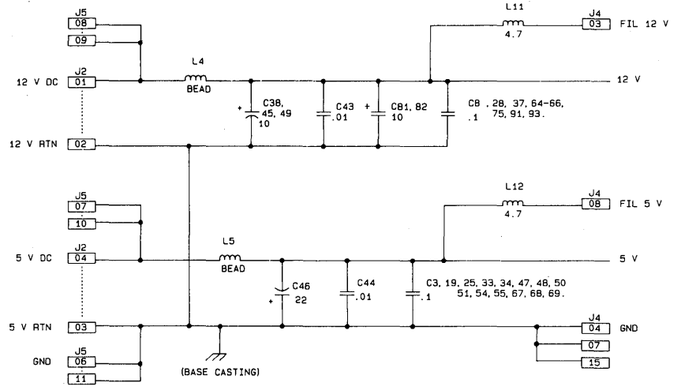


Figure 3-6
Sheet 1

File: B022008A
Drwng: E.M
REV: F

Page 01 of 03
Date: 04/8/87

QUANTUM PROPRIETARY PROPERTY DO NOT USE WITHOUT WRITTEN CONSENT FROM AUTHORIZED QUANTUM PERSONNEL	MUST CONFORM TO ENGINEERING SPEC	Quantum	
	MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE SCHEMATIC, Q200 PCB8
	CASE DEPTH	LINEAR ·XX ·XXX	DETAIL / RELEASED FOR ASSEMBLY
	HARDNESS	ANGULAR·	DESIGN / APPRO / SHEET 1 OF 3 — D
	SURFACE TREATMENT	CORNERS EDGES BROKEN: OUTSIDE MAX, INSIDE MAX	SCALE NONE — 80-22008 — REV

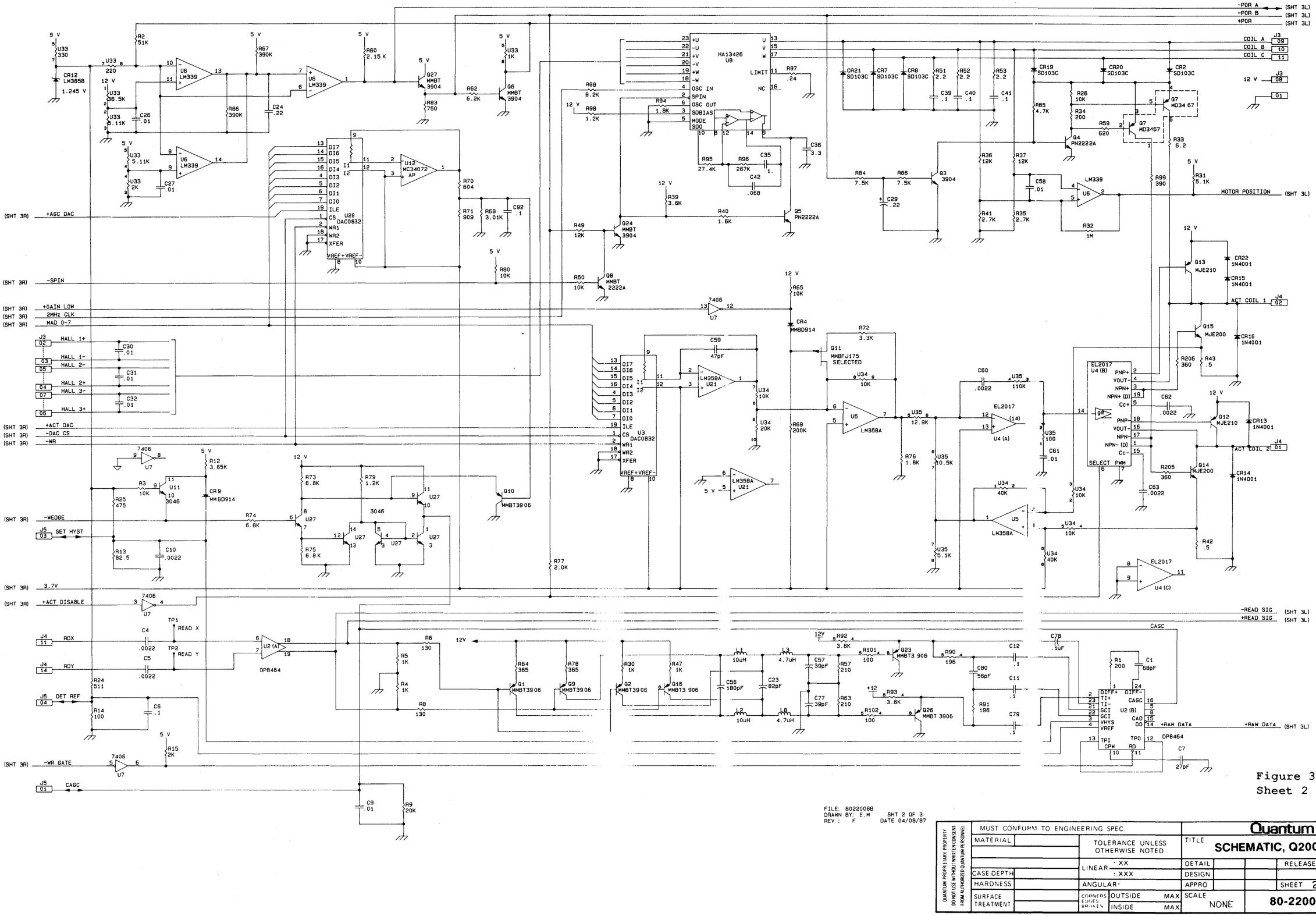


Figure 3-7
Sheet 2

FILE: 80220088
DRAWN BY: E.M SHT 2 OF 3
REV : F DATE 04/08/87

MUST CONFORM TO ENGINEERING SPEC

MATERIAL

TOLERANCE UNLESS OTHERWISE NOTED

LINEAR · XX
· XXX

ANGULAR ·

CASE DEPTH

HARDNESS

SURFACE TREATMENT

CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX

Quantum

TITLE
SCHEMATIC, Q200 PCB8

DETAIL RELEASED FOR ASSEMBLY

DESIGN

APPRO

SHEET 2 OF 3

D

SCALE NONE

80-22008

REV

NOTE: R29 AND R100 ARE NOT USED ON THIS ASSEMBLY.

Figure 3-8
Sheet 3

File: 8022008C
Drwng: E.M Page 03 of 03
Rev: F Date: 04/08/87

QUANTUM PROPRIETARY PROPERTY
DO NOT USE WITHOUT WRITTEN CONSENT FROM AUTHORIZED QUANTUM PERSONNEL

MUST CONFORM TO ENGINEERING SPEC.

MATERIAL

TOLERANCE UNLESS OTHERWISE NOTED
LINEAR .XX .XXX
ANGULAR

CASE DEPTH
HARDNESS
SURFACE TREATMENT
CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX

Quantum

TITLE SCHEMATIC, Q200 PCB8

DETAIL RELEASED FOR ASSEMBLY
DESIGN
APPRO
SHEET 3 OF 3

SCALE NONE

80-22008

REV D

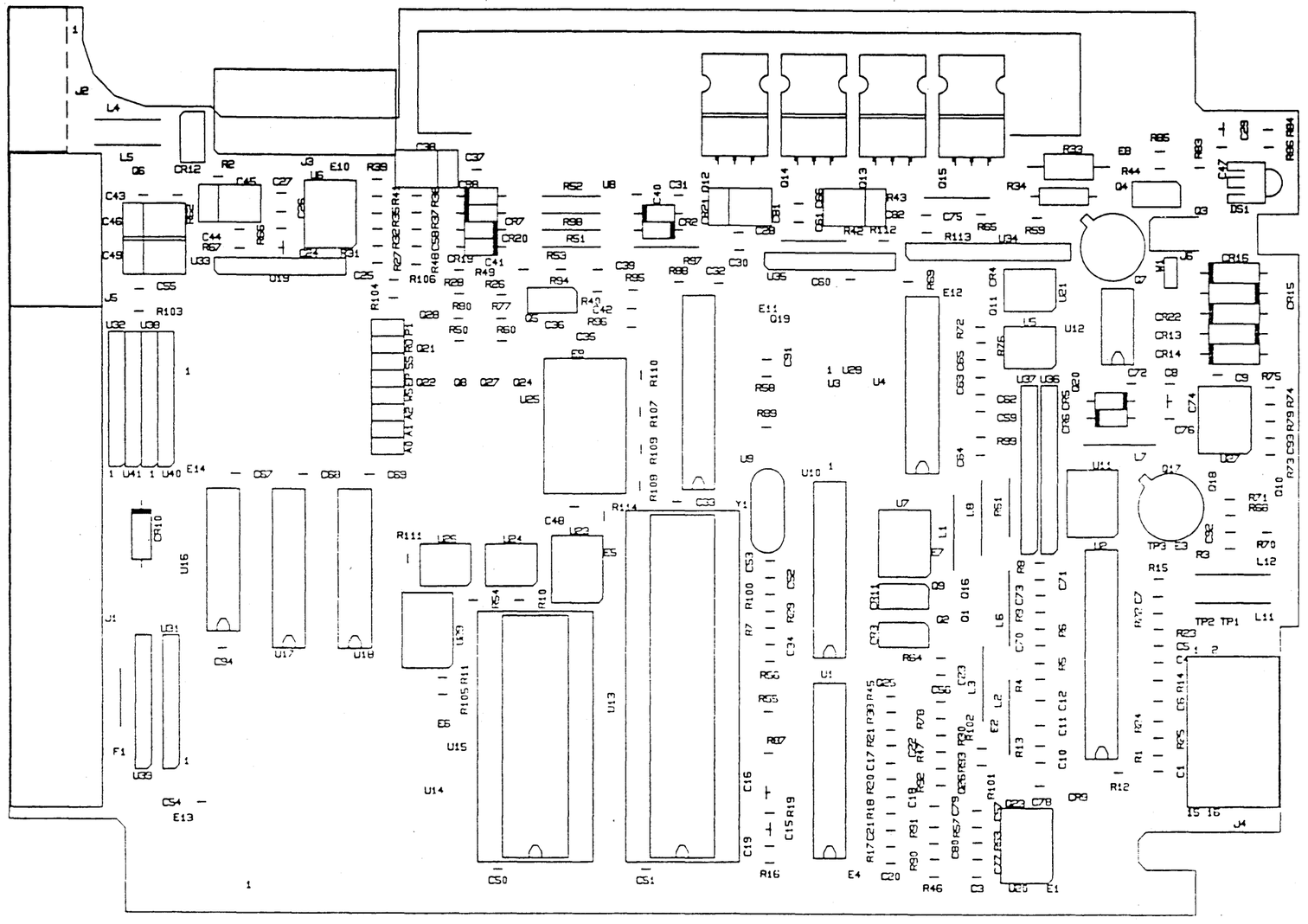


Figure 3-9: Printed Circuit Board Parts Locations

QUANTUM CORP.
Q200 PCB 9 FAB 10-22009
SILKSCREEN
ARTWORK 30-22009 REV 01
CRD A072A KRL 12-19-86

TES: UNLESS OTHERWISE SPECIFIED.

THIS SCHEMATIC APPLIES TO ASSEMBLY 20-22008
OF THE SAME REVISION LEVEL.

ALL RESISTOR VALUES ARE IN OHMS,
ALL CAPACITOR VALUES ARE IN MICROFARADS,
ALL INDUCTOR VALUES ARE IN MICROHENRIES.

R29, 100, 111 ARE NOT INSTALLED IN THIS ASSEMBLY.

JUMPER OPTIONS ARE SHOWN AS:

1 o o 2 OPEN CONNECTION

1 o-o 2 PUSH-ON JUMPER INSTALLED

POWER CONNECTIONS

I.C.	REF	5 V	12 V	GROUND
DP8455	U1	20	NONE	10, 19
DP8464	U2	NONE	9	17, 20
DAC0832	U3 U28	19	20	3, 8
EL2017	U4	NONE	20	10
LM358A	U5	NONE	8	4
LM339	U6	3	NONE	12
7406	U7	14	NONE	7
HA13426	U8	NONE	1	5, 7
TMG CTLR	U9	12, 22	NONE	1, 11
AD7820	U10	7, 20	NONE	10, 13
3046	U11	NONE	NONE	NONE
MC34072AP	U12	NONE	8	4
8031	U13	40	NONE	20
DATA CTLR	U14	8, 17, 25, 33 50, 58, 68, 75, 86, 100	NONE	3, 13, 20, 28, 38, 45, 53, 63, 73, 80, 88
27256	U15	28	NONE	14
4164	U16	8	NONE	16
4416	U17 U18	9	NONE	1, 18
5080	U19	20, 49, 65	NONE	1, 12, 17, 23 35, 46, 52, 57, 61, 62, 64
74LS365A	U20	16	NONE	8
LM358A	U21	NONE	8	4
74HC11	U23	14	NONE	7
75453	U24 U26	8	NONE	4
OSC	U25	11, 14	NONE	7
220 ohm/ 330 ohm	U31 U32 U38	NONE	NONE	1
100K ohm	U39 U40 U41	1	NONE	NONE
74LS112	U29	16	NONE	8

CONNECTOR PIN ASSIGNMENTS

REF.	PIN	SIGNAL NAME	PAGE
J1	01	GND	3A
	02	-DB0	3A
	03	GND	3A
	04	-DB1	3A
	05	GND	3A
	06	-DB2	3A
	07	GND	3A
	08	-DB3	3A
	09	GND	3A
	10	-DB4	3A
	11	GND	3A
	12	-DB5	3A
	13	GND	3A
	14	-DB6	3A
	15	GND	3A
	16	-DB7	3A
	17	GND	3A
	18	-DBP	3A
	19	GND	3A
	20	GND	3A
	21	GND	3A
	22	GND	3A
	23	GND	3A
	24	GND	3A
	25	N/C	

REF.	PIN	SIGNAL NAME	PAGE
J1	26	TERMPWR	3A
	27	GND	3A
	28	GND	3A
	29	GND	3A
	30	GND	3A
	31	GND	3A
	32	-ATN	3A
	33	GND	3A
	34	GND	3A
	35	GND	3A
	36	-BSY	3A
	37	GND	3A
	38	-ACK	3A
	39	GND	3A
	40	-RST	3A
	41	GND	3A
	42	-MSG	3A
	43	GND	3A
	44	-SEL	3A
	45	GND	3A
	46	-C/D	3A
	47	GND	3A
	48	-REQ	3A
	49	GND	3A
	50	-I/O	3A

REF.	PIN	SIGNAL NAME	PAGE
J2	01	12 V DC	1L
	02	12 V RT	1L
	03	5 V RTN	1L
	04	5 V DC	1L

REF.	PIN	SIGNAL NAME	PAGE
J3	01	HALL GND	2A
	02	HALL 1+	2L
	03	HALL 1-	2L
	04	HALL 2+	2L
	05	HALL 2-	2L
	06	HALL 3+	2L
	07	HALL 3-	2L
	08	HALL 12 V	2A
	09	COIL A	2A
	10	COIL B	2A
	11	COIL C	2A

REF.	PIN	SIGNAL NAME	PAGE
J4	01	ACT COIL2	2A
	02	ACT COIL1	2A
	03	FIL 12 V	1A
	04	GND	1A
	05	+BUF WR DATA	3A
	06	+WR UNSAFE	3L
	07	GND	1A
	08	FIL 5 V	1A
	09	+BUF HS1	3A
	10	+BUF HS2	3A
	11	RDX	2L
	12	+BUF HS0	3A
	13	WR CURRENT	2A
	14	RDY	3A
	15	GND	1A
	16	-BUF WR GATE	3A

REF.	PIN	SIGNAL NAME	PAGE
J6	01	LED RETURN	3A
	02	LED SOURCE	3A
	03	LED RETURN	3A

REF.	PIN	SIGNAL NAME	PAGE
J5	01	C AGC	2L
	02	BURST PEAK	3A
	03	SET HYST	3L
	04	DET REF	2L
	05	-WEDGE	3A
	06	GND	1L
	07	5 V	1L
	08	12 V	1L
	09	12 V	1L
	10	5 V	1L
	11	GND	1L
	12	N/C	
	13	+ENCODED DATA	3A
	14	+DATA LOCK	3A
	15	N/C	
	16	+TEST RD CLK	3A

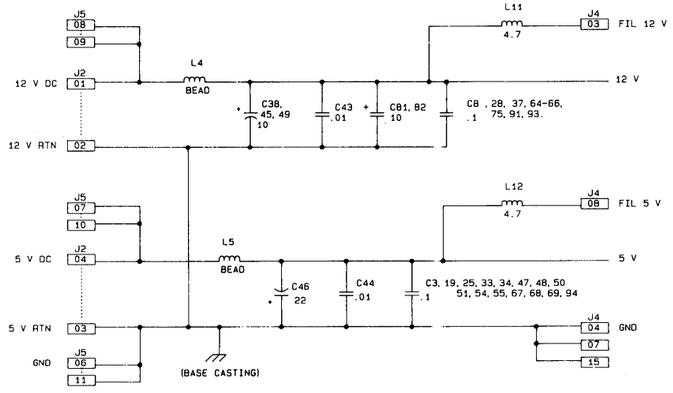


Figure 3-10
Sheet 1

File: 8022009A
Drwng: E M
REV: C

Page 01 of 03
Date: 4/28/87

MUST CONFORM TO ENGINEERING SPEC		Quantum	
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE	SCHEMATIC, Q200 PCB9
	LINEAR — .XX	DETAIL	RELEASED FOR ASSEMBLY
CASE DEPTH	.XXX	DESIGN	
HARDNESS	ANGULAR ·	APPRO	SHEET 1 OF 3 D
SURFACE TREATMENT	OUTSIDE MAX	SCALE NONE	80-22009 REV
	INSIDE MAX		

Figure 3-11
Sheet 2

FILE: 80220098
DRAWN BY: E.M
REV C
SHT 2 OF 3
DATE 04/28/87

QUANTUM PROPRIETARY PROPERTY DO NOT USE WITHOUT WRITTEN CONSENT FROM AUTHORIZED QUANTUM PERSONNEL	MUST CONFORM TO ENGINEERING SPEC		Quantum
	MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE: SCHEMATIC, Q200 PCB9
		LINEAR .XX	DETAIL — RELEASED FOR ASSEMBLY
	CASE DEPTH	.XXX	DESIGN — D
	HARDNESS	ANGULAR	APPRO — SHEET 2 OF 3
	SURFACE TREATMENT	OUTSIDE MAX	SCALE: NONE — 80-22009 — REV

NOTE: R7 IS NOT USED ON THIS ASSEMBLY.

NOTE: A11 IS NOT INSTALLED IN THIS ASM.

Figure 3-12
Sheet 3

QUANTUM PROPRIETARY PROPERTY DO NOT USE WITHOUT WRITTEN CONSENT FROM AUTHORIZED QUANTUM PERSONNEL	MUST CONFORM TO ENGINEERING SPEC	Quantum	
	MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE: SCHEMATIC, Q200 PCB9
		LINEAR .XX	DETAIL — RELEASED FOR ASSEMBLY
	CASE DEPTH	.XXX	DESIGN
	HARDNESS	ANGULAR	APPRO — SHEET 3 OF 3 — D
	SURFACE TREATMENT	OUTSIDE MAX	SCALE: NONE — 80-22009 — REV
		INSIDE MAX	

File: 8022009C
Drwng: E.M Page 03 of 03
Rev: C Date: 04/11/87

SECTION 4. APPLICATIONS

4.1 Special Considerations

The following descriptions detail strategies for optimizing data transfer from Q200 Series drives to host systems.

4.1.1 -REQ/-ACK Handshake

To achieve an optimal transfer rate, the host must assert SCSI signal -ACK as soon as the data is latched. At the Q250/Q280 target, -ACK should be received within about 100 ns of the time that the target has asserted -REQ. If the host waits to assert -ACK until the host has completed its DMA cycle, the data transmission rate may be significantly impaired.

Figure 4-1 illustrates the -REQ/-ACK handshake for a situation where the Q250/Q280 is the target and is transferring data to the host (the initiator). The target (Q250/Q280) performs an internal DMA cycle to bring data from buffer RAM to the SCSI bus; when the data is stable, the target asserts -REQ. When the initiator detectes -REQ asserted, it latches the SCSI data and begins its own DMA cycle to transfer the SCSI data to its internal memory. Two handshake sequences are now possible.

The sequence for fastest data transfer on the SCSI bus is marked "Host latches -ACK; 1.25 MByte/sec Transfer Rate." Here the initiator asserts -ACK as soon as the data is latched, and begins its DMA cycle. When the target (Q250/Q280) observes -ACK asserted, it deasserts -REQ to inform the initiator that the data is no longer valid, and immediately begins a new DMA cycle. The initiator and target DMA cycles overlap, and a new SCSI cycle begins quickly.

The sequence marked "Host Delays -ACK; 625 KByte/sec Transfer Rate" results in slower data transfer. Here the initiator does not assert -ACK until its own DMA cycle is complete. The target does not know if the initiator has received the data, and must wait for the initiator to assert -ACK, keeping the data valid during this time. When the initiator completes its DMA cycle and asserts -ACK, the target deasserts -REQ to inform the initiator that the data is no longer valid, and begins a new DMA cycle. The initiator and target DMA cycles are serial in time.

When the host delays asserting -ACK, the reduction in data transfer rate is greater than adding the DMA cycle times. DICEY is a state machine with 400 ns cycle times, servicing the SCSI bus on alternate cycles. If the target (Q250/Q280) does not observe the assertion of -ACK within the current SCSI cycle, the Q250/Q280 waits for the next SCSI cycle, and the data transfer may take twice as long.

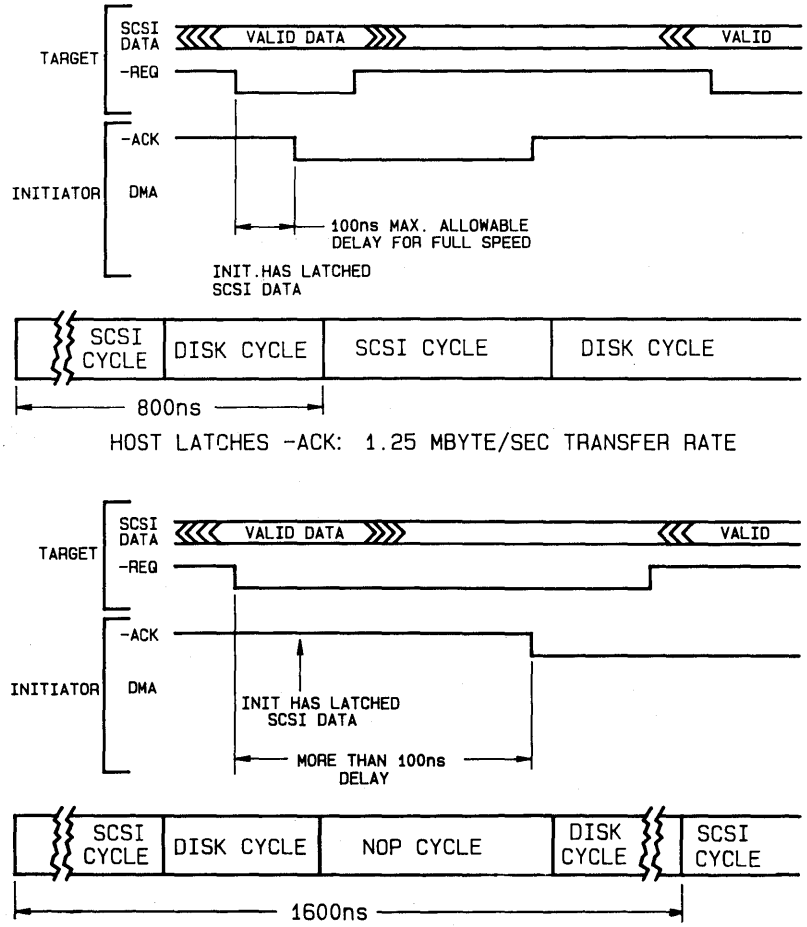


Figure 4-1: -REQ/-ACK Handshake. Q250/Q280 Target Sends Data

4.1.2 Hints for Software Driver Writers

Software driver writers may find the following hints useful when trying to increase data throughput.

1. At the beginning of a MESSAGE phase, a target asserts SCSI bus signals -C/D, -I/O, and -MSG at staggered times. Some hosts detect a change in bus phase and latch data as soon as the signals are received, although the ANSI standard requires that the target confirm the phase change by asserting -REQ. In the Q250/Q280, the -C/D, -I/O, and -MSG outputs of the 5080 are tristated (not used), and are replaced by OR gates U24 and U26, so that -C/D, -I/O, and -MSG are asserted almost simultaneously.

   Software writers may use the simultaneous assertion of the three signals to indicate that valid MESSAGE data is on the bus and avoid the wait for -REQ to be asserted. Note, however, that this is a violation of the ANSI standard, and involves some risk of receiving an invalid MESSAGE from devices other than Q200 Series drives.

2. Set the Buffer Full Ratio and Buffer Empty Ratio (see the Q200 Series Programmers Manual for details) to improve bus utilization by optimizing disconnect/reconnect phases. In the following examples, a rough rule of thumb is that the drive can transfer data to and from the 14 KByte buffer memory at a maximum rate of about 14 KBytes/14 ms and at a sustained rate, including wedges, of about 14 KBytes/19 ms. When the drive is seeking, transfers to and from the disk are delayed. See Figure 4-2 for a diagrammatic representation of the situation.

   The transfer rate on the SCSI bus depends upon how fast the host can "-ACK," and on the block sizes it requests. This data must be known to correctly set the Buffer Full and Empty Ratios.

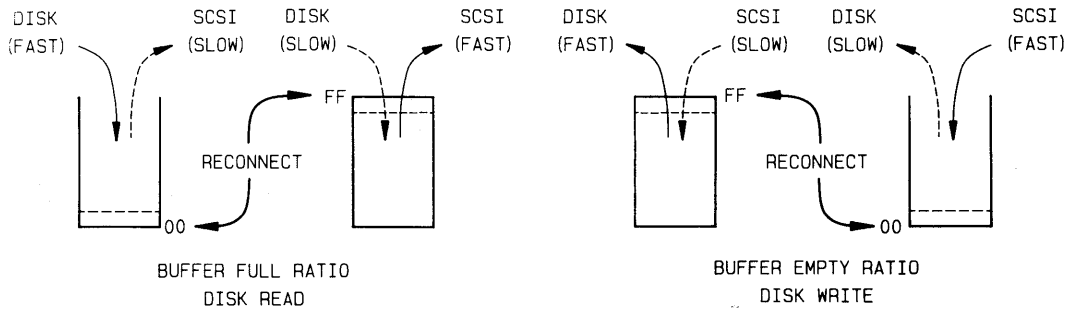


Figure 4-2: Buffer Full and Empty Ratios

The Buffer Full Ratio applies when the drive is reading from the disk. The drive fills buffer memory while the SCSI bus is emptying it. If the drive must seek for more data, the SCSI bus may empty the buffer, at which time the drive disconnects. Now assume the drive is much faster than the SCSI bus: then the drive should reconnect as soon as there is anything in the buffer, and the Buffer Full Ratio should be set to 00. Conversely, if the SCSI bus is much faster than the drive, the drive shouldn't reconnect until the buffer is full (Buffer Full Ratio = FF).

In many situations, the host will request a transfer of a specific size; near optimum bus utilization is obtained by setting the Buffer Full Ratio so the drive has filled the buffer with that much data before reconnecting: if the host asks for 4 KBytes, wait for the drive to transfer 4 KBytes to the buffer before reconnecting. This strategy avoids excessive disconnect/reconnect SCSI bus overhead.

Buffer Empty Ratio applies when the drive is writing, and is the mirror image of the situation when the drive is reading. The SCSI bus fills buffer memory while the drive is emptying it. If the drive must seek, the SCSI bus may fill the buffer, at which time the drive disconnects. Now assume that the SCSI bus is much faster than the drive: then the drive should reconnect even if the buffer is nearly empty (Buffer Empty Ratio = 00). Conversely, if the drive is much faster than the SCSI bus, the drive should reconnect when the buffer is full (Buffer Empty Ratio = FF).

If the host transfers data in known size blocks, near optimum bus utilization is obtained by setting the Buffer Empty Ratio so the buffer is filled with that much data before reconnecting.

3. When transferring data, use the maximum number of blocks within a single read or write command. Since each individual command has an overhead associated with it, the more individual commands used, the lower the data throughput. If a file consists of several blocks located in sequentially increasing LBAs (logical block addresses), use one command to read all of the blocks, instead of many commands of one block reads or writes.

   Also, adjust the block size with the MODE SELECT command to allow up to 4 sectors to be read with a single block command. Since the Q250/Q280 drives are hard sectored and have a fixed interleave of 1:1, optimizing the block size and number of blocks per read can have a dramatic impact on overall performance.

4. For maximum compatibility with various vendors and models, use only the ANSI "Mandatory" commands.

5. Program only the error Sense Keys into the driver code, not the additional Sense Codes. The driver code can make decisions based only on the Sense Keys, such as retry or abort. However, the Sense Codes should be displayed or printed, as they can greatly enhance diagnosis of problems with the drives while troubleshooting.

4.2 Errors and Media Defects

4.2.1 Errors

Q200 Series drives incorporate integrated media defect handling and ECC capabilities that eliminate the requirement for user defect maps, and for writing dedicated defect-mapping software. This also reduces test time during system integration. A Q200 Series drive is capable of detecting and compensating for any new defective sectors that may be detected during the life of the drive.

Errors Defined

Any discrepancy between recorded data and recovered data is defined as a data error. Errors are either "soft"--those not readily repeatable, or "hard"--those repeatable with high probability. Soft errors are generally related to the signal-to-noise ratio of the system, and represent marginal conditions of the media, heads, and circuitry, or even interference from other equipment. Hard errors are most often due to defects, pits, scratches, or thin spots in the media. These defective media areas can be detected and skipped (not used).

Error Correcting Code

The ECC is a byte-based Reed-Solomon (t = 2) double burst correcting code with an interleave of 3, resulting in a 96-bit ECC. This code allows correction of any sector having one burst of 17 bits incorrect, and detection of any sector having up to three bursts of 17 bits incorrect. If the errors begin on byte boundaries, the code corrects or detects a full three bytes (24 bits) incorrect. Further, it detects many errors worse than stated with very high probability, while the probability of misdetection is very low.

At the start of a write operation, the ECC syndrome is zeroed. DICEY computes the syndrome as each byte is written. After the last byte of data, DICEY appends the syndrome to the end of the data on the sector. Later, when the sector is read, DICEY calculates another syndrome from the data and the ECC bytes originally written on the sector. If the syndrome is zero, no errors have occurred in writing and reading. A non-zero syndrome indicates an error, and the user's Error Recovery Parameters (previously selected with the MODE SELECT command) determine the action to be taken. See the Q200 Series Programmers Manual for full details.

The basic strategy coded in firmware is to continue retrying a read operation until a stable syndrome is found (i.e., the same syndrome is obtained when the sector is read twice in a row). This strategy avoids invoking correction on soft errors and dramatically reduces the probability of miscorrection. When a stable syndrome is found, the drive attempts to use ECC to correct the data, if ECC correction is enabled. If the number of retries reaches the maximum specified by the user, the drive again attempts to correct the error, even if a stable syndrome has not been found (again, only if ECC correction is enabled).

4.2.2 Allocating Replacement Sectors

Traditionally, replacement sectors are put in a reserved area of the drive far from the inside or outside diameter of the disk. Thus, when a defective sector is found, a long seek to the replacement sector is required.

Q200 Series drives use an alternate approach: two spare sectors are reserved at the end of every cylinder for the replacement of defective sectors. Long seeks to the replacement sectors are eliminated.

When a drive is formatted, either in the factory or later in the field, an "in-line sparing" method is used: defective sectors are replaced with adjacent sectors, and all subsequent sectors are shifted up (see Figure 4-3). In the rare instance where more than two defects are found within the same cylinder, the "In-Line Sparing Overflow" method is used: additional defects are mapped into the nearest adjacent cylinder with spare sectors available (see Figure 4-4).

With this approach, cylinder boundaries are well defined, with a simple relationship between each cylinder's physical and logical block addresses--thus providing the host a method to ensure that file records are stored within cylinder boundaries.

When Automatic Read Reallocation is enabled (with the MODE SELECT command), field-found or "grown" defects are automatically mapped directly into spare sectors without shifting subsequent logical blocks, as shown in Figure 4-5.

HEAD 0	x	x + 1	x + 2		x + 29	x + 30	x + 31
HEAD 1	x + 32	(Bad) XXXX	x + 33		x + 60	x + 61	x + 62
•							
•							
•							
HEAD 5	x + 159	x +160	x + 161		x + 188	x + 189 (spare)	(spare)

x = logical block address of initial sector
Q280: cylinder number × 190; Q250; cylinder × 126
(Assuming 512 byte logical block size)
XXXXX = deallocated sector

Figure 4-3: In-Line Sparing of Defective Sectors

HEAD 0	x	x + 1	x + 2		x + 29	x + 30	x + 31
HEAD 1	x + 32	(Bad) XXXX	x + 33		(Bad) XXXX	x + 60	(Bad) XXXX
•	x + 61						
HEAD 5	x + 157				x + 186	x + 187 (spare)	x + 188 (spare)
•							
NEXT CYL						(spare)	x + 189 (spare)

x = logical block address of initial sector
Q280: cylinder number × 190; Q250; cylinder × 126
(Assuming 512 byte logical block size)
XXXXX = deallocated sector

Figure 4-4: In-Line Sparing Overflow of Defective Sectors

HEAD 0	x	x + 1	x + 2		x + 29	x + 30	x + 31
HEAD 1	x + 32	(Bad) XXXX	x + 34		x + 61	x + 62	x + 63
•							
•							
•							
HEAD 5	x + 160	x +161	x + 162		x + 189	(spare)	x + 33 (spare)

x = logical block address of initial sector
Q280: cylinder × 190; Q250: cylinder × 126
(Assuming 512 byte logical block size)
XXXXX = deallocated sector

Figure 4-5: Sparing of Field-Found Defective Sectors

Table 4-1 shows the number of sectors available for Models Q250 and Q280.

Table 4-1: Available Spare and Defective Sectors

Model	Cylinders	User Sectors	Spare Sectors	Maximum Defective Sectors at Factory
Q250	823	103,698	1,646	50
Q280	823	156,370	1,646	80

4.2.3 Creating the Defect Lists

Defect lists map the defective sectors. The lists are written on a system reserved cylinder; the W-list is downloaded into buffer RAM during power-on. Copies of the lists are replicated on every head of the drive as backups. Before a read or write, the W-list is checked to determine whether the sector is defective or not, and if so, the location of the sector which replaces it. See the Sequence descriptions, Figures 2-15 through 2-17.

Defect lists are created by the FORMAT UNIT command, the REASSIGN BLOCKS command, or during read operations when Automatic Read Reallocation is enabled.

There are four different defect lists:

P-list. The primary defect list: the list of defects found when the drive is tested in the factory. It is written on a system reserved track and can never be modified by a user--it is preserved for the life of the drive.

G-list. The grown defect list: the list of accumulated defects detected during field operation of the drive. The defects are detected either by the user, or by the read operation.

D-list. The defect data list: the list of defective sectors provided by the user to request the drive to map them out. The D-list will be merged into the G-list.

W-list. The working list: the list of defective sectors and their replacements. The W-list is constructed from the defects combined from the P-list, G-list, and D-list. This list is used during operation of the drive.

4.2.4 Updating the Drive Using the Defect Lists

At any time during normal operation, the user can choose to:

- Map out the defective blocks. The user can submit a D-list of defects, and uses the REASSIGN BLOCKS command.

- Rely on the Automatic Read Reallocation option of the MODE SELECT command. The drive automatically detects drive idefects and reallocates the sectors.

- Reformat the drive with the FORMAT UNIT command, using these combinations of defect lists:

Without defect lists	(use no defect lists)
Factory defects only	(use P-list only)
Grown defects only	(use G-list only)
Existing defects	(use P-list and G-list)
Provided defects only	(use D-list only)
Factory and provided defects	(use P-list and D-list)
Grown and provided defects	(use G-list and D-list)
All known defects	(use P-list, G-list, D-list)

In any of the above cases, the drive reconstructs the W-list and updates the G-list. The P-list, however, remains untouched.

See the Q200 Series Programmers Manual for details on use of the commands and options mentioned.

4.3 Grounding, Electrostatic Discharges, and EMI

The 5 Vdc and 12 Vdc returns are connected to the base casting. The metal shock mount brackets are electrically isolated, and the face-plate is plastic. Therefore, mounting the drives by the mounting holes in the shock mount brackets does not directly connect the base casting to cabinet ground. If desired, an installer can run a ground wire (a heavy braid is recommended to ensure low impedance to high frequencies) from cabinet ground to the male tab-type grounding lug fastened to the base casting. The male lug is AMP Faston P/N 61761-2. One suitable mating part is a push-on receptacle, AMP P/N 62187-1, which accomodates 18 AWG wire. The mating part used should be chosen to accept the grounding braid.

Such a ground connection is desirable if:

- Electrostatic discharges occur (for example, by personnel touching the drive after walking over a carpet). These may cause soft (random, non-repeating) errors, but discharges over 20 kilovolts may cause permanent damage.

- Electromagnetic Interference (EMI) is present. Excessive EMI may also cause soft errors.

EMI may be due to nearby radio or TV stations, chopper-type power supplies (especially those operating from the same 5 volts or 12 volts as the Q250/Q280 drive), heavy electrical machinery such as elevators and motors, even lamp dimmers. The drive is rated to operate in a strong field: up to 4 volts/meter over a range of 20 Hz to 20 MHz.

If EMI is suspected and grounding doesn't help, use some common sense analysis: see if the problems occur only when the suspected source is operating; try different, dedicated sources of 5 volts and 12 volts. Surge suppressors in the ac lines to other equipment may help. If the problem persists, contact Quantum's Technical Support Group.

SECTION 5. MAINTENANCE

5.1 Maintenance Precautions

- Preventive maintenance is not required. There are no adjustments, either to the HDA or on the printed circuit board.
- DO NOT open the HDA or attempt to remove the labels, some of which are also seals.
- Do not lift the drive by its faceplate or printed circuit board. Always handle the drive by its shock mount brackets.
- Do not operate the drive without its shock mount brackets.
- Avoid harsh shocks to the drive at any time. Always set it down carefully.
- Do not move the drive for 30 seconds after power has been removed. This time is required for the AIRLOCK to lock the headstack assembly in the landing zone.

5.2 Level 1 Maintenance

- Replacement of the entire drive.
- Replacement of plug-in EPROM on printed circuit board (PCB).

CAUTION

Do not exchange different EPROMs without approval from Quantum. The wrong EPROM may cause user data to be lost, or servo tracks to be written over and destroyed.

- Exchange of PCB. See Section 5.5 for information on isolating the problem to the HDA or the PCB. Note that Models Q250 and Q280, and drives with and without DisCache require different EPROMs, and that drives with DisCache require a PCB equipped with 64 Kbytes of RAM (U16, U17, and U18).
- Replacement of shock mounts, brackets, and faceplate, as listed in SECTION 6. Besides the replacement parts, only common hand tools are required.

NOTE

Users must limit their service to Level 1 during the warranty period. The Quantum warranty is null and void if the HDA is opened or any Level 2 procedure is attempted. All time and material to repair the drive will be billed at the prevailing rates.

5.3 Level 2 Maintenance

Level 2 maintenance is performed by trained personnel at an authorized service center or at the factory.

- Level 1 plus repair of HDA and PCBs.

5.4 Connector Maintenance

Both intermittent problems and solid problems can be caused by connectors. Before troubleshooting by observing waveforms, inspect the ribbon cable connector on the SCSI bus: check visually with a 3X to 10X magnifier that all wires are crimped to the contacts; flex the cable gently while the drive is operating and watch for intermittents; clean the contacts by wiping them with a lint-free cloth moistened with a contact-cleaning solvent.

5.5 PCB Waveforms and Techniques

The waveforms described in this Section may be observed for troubleshooting: to determine if the PCB is operating correctly, or to isolate a problem to the board or the HDA.

If a drive successfully recalibrates when operating in a system, the following waveform tests are not likely to reveal any problems, since most circuits must operate: power, POR, RAM test, motor control, microprocessor, EPROM, DICEY, FYLO, seek, servo, read, phase-locked-loop, write, and SCSI interface.

These waveform tests are primarily useful with a drive that doesn't recalibrate. They concentrate on read functions; these exercise almost all circuits and require the least special test equipment. It is easier to check write functions by noting the Sense Error Codes and Sense Keys reported to the host over the SCSI bus.

5.5.1 Special Test Equipment

- 150 MHz (or better) oscilloscope with differential input and two or four channels. High impedance probes are required, and a delaying sweep is useful.

- o Various clip-on connections for tiny 100-pin IC legs.
- o Digital dc voltmeter.
- o Extension cable, allowing the drive to be operated on a bench while connected to power. Connection to the SCSI bus is not required.

5.5.2 Techniques and Waveform Descriptions

Place the drive so the PCB is easily accessible. Remove the WS shorting plug, if installed. Plug in power, but not the SCSI bus connector. The waveforms are shown in Figures 2-12, 5-1, 5-2 and 5-3 and the schematics are in SECTION 3.

CAUTION

Be careful not to short IC pins together or to ground. Be especially careful with -WR GATE and -BUF WR GATE. If either of these signals is shorted to ground or another signal, the drive may write over and destroy data and servo tracks.

Some of the signals can be observed at J5, the test connector, where there is less danger of shorts.

1. DC Voltages

Measure (all + with respect to ground):

5 V dc and 12 V dc input power, near J2, or on J5.
3.7 V dc reference voltage at pin 10 of U28.
2.5 V dc reference voltage at pin 11 of U10.
3.7 V dc reference voltage at pin 12 of U10.

2. Spin-up

Listen to the motor spin up. In order for the motor to spin, there must be:

- o A continuous low level on U8, pin 2. DICEY asserts this -SPIN signal after the RAM test and other initialization tests are passed.
- o 1 V peak-to-peak at 2 MHz on top of 1 V dc, on U8, pin 4. The 2 MHz is derived from the 12 MHz clock, divided down by FYLO, U9.

3. RDX, RDY, and -WEDGE

Use the oscilloscope differential input and connect the probes to pins 6 and 7 of U2. This is RDX and RDY, the analog signal from a read head, amplified by the flex circuit. Expect about 20 mV p-p at the disk outer diameter, 15 mV at the inner diameter. This signal is difficult or impossible to sync, and shows a broad band on the screen.

Now, trigger the oscilloscope on -WEDGE, pin 12 of U13, or pin 5 of J5. The servo bursts can now be observed, but all wedges are on top of one another. To separate them and observe the details of just one wedge, trigger on pin 5 of U13, and delay the sweep.

Note that -WEDGE requires that the pulse detector and FYLO be working.

4. +RAW DATA

Use another oscilloscope channel, and simultaneously with RDX and RDY, observe +RAW DATA, the input signal to FYLO, on pin 6 of U9. Observe a TTL-type pulse for each transition of RDX and RDY.

5. +ENCODED DATA

Observe at pin 4 of U9, or pin 13 of J5. +ENCODED DATA is the output of FYLO, and is the same as +RAW DATA.

6. +READ DATA

Observe this at the same time as RDX and RDY. It is a TTL-type signal, the input to DICEY, ready to be decoded. It is synchronous to RD CLOCK, and its presence means the servo is keeping the head on track, and that the pulse detector and FYLO are operating.

7. AMC Circuit

Observe BURST PEAK, pin 1 of U10, or pin 2 of J5. Trigger using the signal -WEDGE. Look for a series of pulses (each about 10 microseconds in duration) going negative from a 3.7 V dc base line. The pulse amplitude (from the 3.7 V dc base line) is proportional to the amplitude of the servo bursts, and the group occurs simultaneously with -WEDGE. FYLO must be working to observe this.

5.5.3 Test Connector J5 Signals

Test connector J5 is used in the factory to test the PCB, but it also provides a convenient place to observe some signals for troubleshooting. The signals are listed in Table 5-1.

Table 5-1: Test Connector J5 Signals

Pin	Signal Name	Description
1	CAGC	AGC voltage for U2 (B). See Section 2.3.5 and Section 2.3.7.
2	BURST PEAK	See AMC Circuit in Section 5.5.2, and Figure 5-3.
3	SET HYST	1.2 V dc. This voltage is changed in factory test to check the drive's margin.
4	DET REF	0.2 V dc. This voltage is changed in factory test to check the drive's margin.
5	-WEDGE	See RDX, RDY, and -WEDGE in Section 5.5.2, and Figure 5-2.
6	GND	
7	5 Vdc	
8	12 Vdc	
9	12 Vdc	
10	5 Vdc	
11	GND	
12	N/C	
13	+ENCODED DATA	Same as +RAW DATA. See Figure 5-1.
14	+DATA LOCK	TTL Level. Asserted by DICEY at end of sync pattern check.
15	N/C	
16	+TEST RD CLOCK	Same as +RD CLOCK. See Figure 2-13.

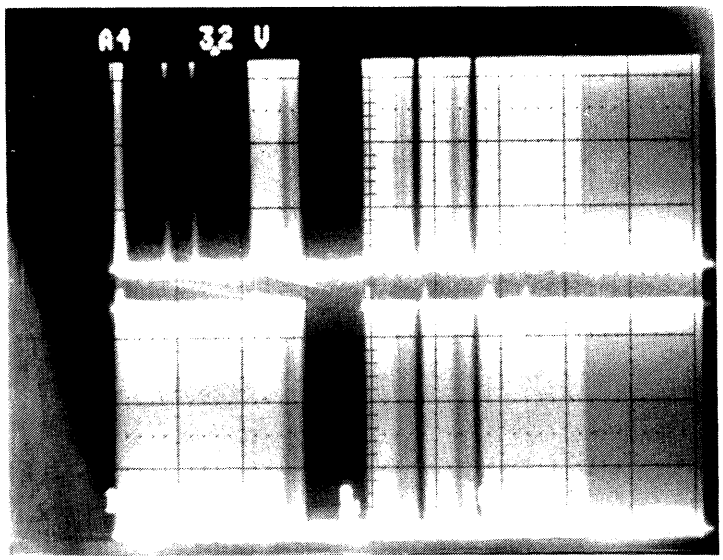


Figure 5-1: Test Waveforms(1)

TOP: +RAW DATA (1 V/div.)
BOTTOM: +RD DATA (1 V/div.)

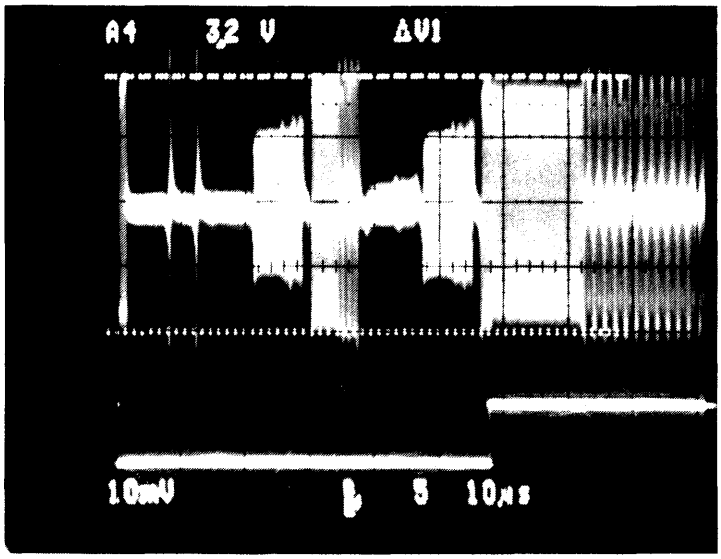


Figure 5-2: Test Waveforms(2)

TOP: RDX, RDY
(Differential, 5 mv/div.)
BOTTOM: -WEDGE (5 V/div.)

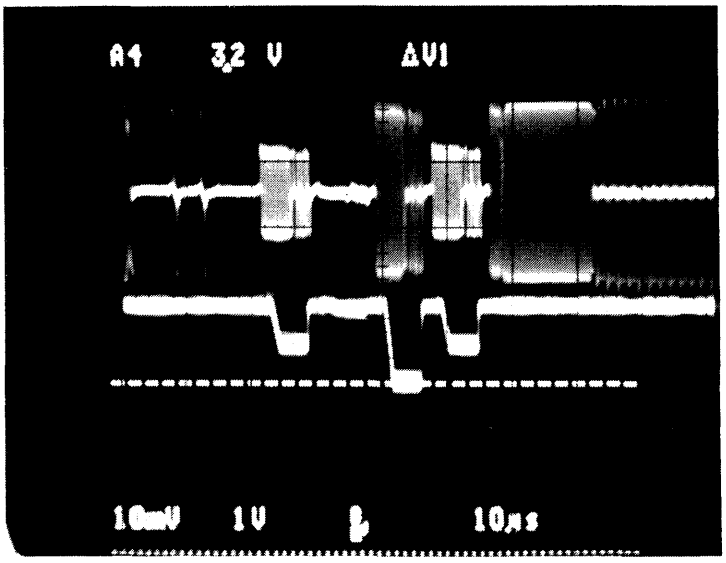


Figure 5-3: Test Waveforms(3)

TOP: -READ SIG, +READ SIG
(Differential, 100 mv/div.)
BOTTOM: BURST PEAK (1 V/div.)

SECTION 6. PARTS LISTS

6.1 Spare Parts List

The following abbreviated list provides part numbers for subassemblies available through Quantum's Customer Support Department. Note that this is a very limited list. For a complete list of PCB components, refer to Section 6.2.

Part Number	Description
20-22007	PCB-7 (standard)
20-22017	PCB-7 (standard with warm-reset rework)
20-22027	PCB-7 (standard with DisCache rework)
20-22008	PCB-8 (standard with warm-reset)
20-22018	PCB-8 (standard with warm-reset and DisCache)
20-22009	PCB-9 (standard with warm-reset and green LED)

6.2 Reference Parts List(s)

The following parts lists correspond to the PCB layouts (Parts Locations illustrations) provided in Section 3. As in Section 3, several iterations of the Q200 Series PCB are detailed in these lists. Specifically, the most current revisions of PCB-7, PCB-8 and PCB-9 are documented here.

Quantum Corporation
1804 McCarthy Blvd.
Milpitas, CA 95035