DESIGN GUIDE

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TABLES

Section 1 Background Information

1.1 General Description

Sirocco is a family of half-height 3.5-inch rigid disk products with capacities of 1.7 GB and 2.5 GB. SCSI and AT interfaces will be available.

Description	# of Data Disks	# of Data Surfaces	Capacity
A. 1" SCSI	2	4	1.7 GB
B. 1" AT	2	4	1.7 GB
C. 1" SCSI	3	6	2.5 GB
D. 1" AT	3	6	2.5 GB

Table 1-1 Summary of Sirocco product line.

1.2 Basic Development Assumptions

The need to bring Sirocco to market within a critical "time-window" dictates that fast time-to-volume is the top development priority.

Manufacturing will be done in Japan by MKE, lowering process risk and increasing cost competitiveness.

Design Leverage from Fireball and TrailBlazer as much as possible to cut development time and risk.

1.2.1 Top Development Priorities

1. Time to Volume: Pre Mass Pro by 10/95.
2. Low cost
3. Performance/Features (2,3 Disk).

1.2.2 Top Development Risks

1. MR heads and MR Preamp.
   - Cost
   - Availability
   - Technical maturity
2. Resources for program support.
3. Maturity of leveraged technology.
4. Potentially late to market relative to IBM.

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Section 2 Specifications

This section provides the physical, electrical, and environmental specifications for the Sirocco 1700/2550 MB hard disk drive.

2.1 Key Specification Comparison

The following are the key specification comparisons between Sirocco, Fireball, and TrailBlazer:

Sirocco	Fireball	TrailBlazer
• 4500 RPM	5400 RPM	4500 RPM
• 5850 TPI	4200 TPI	3794 TPI
• 11.5 ms Avg. Seek Time	12 ms Avg. Seek Time	14 ms Avg. Seek Time
• 850 MB/Disk	526.63 MB/Disk	425.07 MB/Disk
• 3 Disk/6 Head (Max)	2 Disk/4 Head (Max)	2 Disk/4 Head (Max)
• 72.2 Mb/s Max Data Rate	81.1 Mb/s Max Data Rate	53.7 Mb/s Max Data
• MR Head	TF Head	MIG Head
• PRML Channel	PRML Channel	Peak Det.

2.2 General Specification

2.2.1 Capacity/Format/Channel Specification

MODEL	1700 MB	2550 MB
Spindle Speed	4500 RPM	4500 RPM
Servo Method	Embedded	Embedded
Servo Sample Per Track	90	90
OD Radius	1.8104 in	1.8104 in
ID Radius	0.7984 in	0.7984 in
Stroke	1.0120 in	1.0120 in
Recording Code	16/17 PRML	16/17 PRML
Recording Zone	16	16
TPI	5850	5850
Flux Change Per Inch (Max)	115,176	115,176
Bits Per Inch (Max)	108.4 K	108.4 K
Areal Density	643.78 Mb/in^2	643.78 Mb/in^2
Data Rate	72.2 Mb/s (Max) 40.8 Mb/s (Min)	72.2 Mb/s (Max) 40.8 Mb/s (Min)
Number of Disks	2	3
Number of Heads	4	6
Formatted Capacity	1700 MB	2550 MB
Cylinders	5920	5920
User Data Cylinders	5900	5900
Data Tracks	23600	35400
Data Surfaces	4	6
Sectors Per Track	96 - 180	96 - 180
Data Bytes Per Sector	512	512
Spare Sectors (2 per cylinder)	11800	11800
SCSI Logical Blocks	3,353,536	5,030,304
AT Logical Capacity	1724.79 MB	2587.18 MB
AT Logical Sectors	63	63
AT Logical Cylinder	3342	5013
AT Logical Heads	16	16
AT Logical Sectors/Track	TBD	TBD
Buffer & RAM (128 KB)	Single 64x16 DRAM	Single 64x16 DRAM
Cache Size (Minimum)	76 KB	76 KB
Data Format (Multiple Sectors per Wedge)	I.D. after Wedge	I.D. after Wedge
ECC (with Cross Check)	160 bit RS	160 bit RS

Table 2-1 Capacity/Format/Channel Specification

2.2.2 AT Interface Specification

Interface Features		
	Auto Task Register Updates[1]	
	Multi Block Auto Read [1]	
	Multi Block Auto Write[1]	
	Cable Select	
	Local Bus PIO and DMA timing	
	Multiword DMA Transfer	
	Multi Command Auto Read	
Interface	ATA/CAM	
Interface Transfer Rate		
	PIO[2]	
	Mode 3	11 MB/s
	Mode 4	16 MB/s TBD
	DMA	
	Mode 1	13 MB/s
	Mode 2	16 MB/s
	Mode 3	20 MB/s TBD
Performance		
Sequential Throughput[3]		
Read	5 MB/s (4096 Byte record)	
Write	5 MB/s (4096 Byte record)	
PC Bench Disk Harmonic	TBD	
Q-Bench Data Access Time	TBD	
Signal Conditioning I/O Drivers	Edge Rate Control (5 ns rise & fall times minimum) High hysteresis noise rejecting input buffers	

Table 2-2 AT Interface Specification

Notes to Table 2-2:

1. Auto features support CHS, LBA, and DMA transfer, Read multiple, Write multiple.
2. Rates above 6 MB/s require IOCHRDY.
3. Sequential performance is typical performance at O.D. data zone.

2.2.3 SCSI Interface Specification

Interface Features	
	SCSI-2 supported SCSI-3 TBD SCAM Active Negation drivers Active Termination Single Ended 8-Bit Fast SCSI at 10 Mbyte/sec
Interface	SCSI-2
Interface Transfer Rate	
	Asynch 6 MB/s Sync 10 MB/ s
Performance	
Sequential Throughput[1]	
Read	5 MB/s
Write	5 MB/s
Random Throughput	
Read	30 KB/s (512 Bytes per command)
Write	28 KB/s
I/O per second[2]	68
Q-Bench Data Access Time	TBD
Signal Termination	Active Electrically Switchable
Signal Conditioning I/O Drivers	Edge rate control (5 nsec rise-fall time min) High hysteresis noise rejecting buffers

Table 2-3 SCSI Interface Specification

Notes to Table 2-3:

1. Sequential performance is typical performance at O.D. data zone, 10 MB command.
2. Calculated typical value 1/(Avg Access TIme + Latency). Command overhead not included.

2.3 Timing Parameters

2.3.1 Timing Specifications

	Typical Nominal[1]	Maximum Worst Case[1]
Sequential Cylinder Switch Time[2]	3.5 ms[4]	N/A[6]
Sequential Head Switch Time[3]	3.0 ms[4]	N/A[6]
Random Average (Read or Seek)	11.5 ms	13.0 ms
Random Average (Write)	13.5 ms	15.0 ms
Full Stroke Seek	22 ms	25 ms
Average Rotational Latency	6.7 ms	
Power on to Drive Ready[5]	9 s	15 s

Table 2-4 Timing Specifications

Notes to Table 2-4:

Quoted seek times include head settling time, but do not include command overhead time or rotational latency time.

1. Nominal conditions are defined as 25 °C ambient, nominal supply voltages and no applied shock or vibration. Worst case conditions are defined as worst case extremes of "operating" temperature, humidity, and supply voltages.
2. Sequential Cylinder Switch Time is the time from the conclusion of the last sector of a cylinder to the first logical sector on the next cylinder.
3. Sequential Head Switch Time is the time from the conclusion of the last sector of a track to the beginning of the first logical sector on the next track of the same cylinder.
4. Including sequencer overhead for write setup on head & cylinder switch. No more than 5% of head / cylinder switches will exceed this value.
5. At power on startup error algorithms are used and these may require additional time in coming ready. These recovery routines may extend the time to ready to as large as 30 seconds.
6. Not applicable due to no effect in throughput.

2.4 Disk Errors

Error Type	
Uncorrected Read Errors[1]	1 Event per 10^7 bits read[2]
I.D. Error [3]	1 Event per 10^7 bits read[2]
Recovered Read Errors[4]	1 Event per 10^{10} bits read
Multi Read Recovered Errors[5]	1 Event per 10^{12} bits read
Unrecovered Data Error[6]	1 Event per 10^{14} bits read
Transferring erroneous data to customer[7]	
On the Fly (Single or Double correction)	1Event per 5.88 x10^{25} bits read
Off LIne Correction (Triple correction)	1Event per 1.19 x10^{38} bits read
Seek Errors[8]	1 Error per 10^6 seeks
Bump/Gray Code error rate[9]	1 event per 10^7 bits written

Table 2-5 Error types and rates

Notes to Table 2-5:

1. Uncorrected Read Errors are those read errors with Read on arrival, ECC on the fly and retries disabled. For monitoring the manufacturing process only.
2. Error rates are for worst case temperature & voltage.
3. I.D. Errors are defined as TBD.
4. Recovered Read errors are those which require retries for data correction. Errors corrected by ECC on the fly are not considered recovered read errors. Read on arrival is disabled to meet this specification.
5. Triple Burst recovered errors are those read errors which require the triple burst error correction algorithm to be applied for data correction. This correction is typically applied only after the programmed retry count is exhausted.
6. Unrecovered read errors are those errors that is not correctable using an error correcting code (ECC) or retries. The drive terminates retry reads either when a repeating error pattern occurs or after eight unsuccessful retries and application of double burst error correction.
7. Probability of misdetection.
8. A seek error occurs when the actuator fails to reach or remain on the requested cylinder, and the drive requires the execution of the full recalibration routine to locate the requested cylinder.
9. Bump/gray code errors are servo field read errors that require sequencer shutdown during a write operation and invocation of a write retry. This error rate does not apply with externally applied vibration. Bump error rate should be set such that write throughput does not degrade by more than 5% from best case.

For explanation of terms and more detailed information regarding how these numbers were arrived at, please see Section 7.3. ECC.

2.5 Power Requirements

Sirocco hard disk drive operates from two supply voltages:

- +12 V ± 10%
- + 5 V ± 5%

The allowable ripple and noise for each voltages:

- +12 V 250 mV P-P 1Hz-100MHz
- + 5 V 100 mV P-P 1Hz-100MHz

2.5.1 Drive Power Dissipation

Mode of Operation	Maximum Avg. Current[7]	Typical Avg Current (mA)	Maximum Avg. Current (mA)	Typical Avg Current (mA)	Maximum Avg. Power (Watts)	Typical Avg. Power (Watts)
	+12 V	+12 V	+5 V	+5 V		
Start up[1]	TBD	TBD	TBD	TBD	TBD	TBD
Idle[2]	TBD	TBD	TBD	TBD	TBD	TBD
Read/Write Ontrack[3]	TBD	TBD	TBD	TBD	TBD	TBD
Read/Write/ Seek[4]	TBD	TBD	TBD	TBD	TBD	TBD
Max Seeking[5]	TBD	TBD	TBD	TBD	TBD	TBD
Standby[6]	TBD	TBD	TBD	TBD	TBD	TBD
Sleep	TBD	TBD	TBD	TBD	TBD	TBD

Table 2-6 Power dissipation in various modes

Notes to Table 2-6:

1. Startup is stated as the peak (>10 ms) power required during spindle startup. This power will be required for less than 5 seconds.
2. Idle: when the drive is not reading, writing, or seeking. the motor is up to speed and DRIVE READY condition exists. Actuator is residing on last track accessed.
3. Read/Write/Ontrack: is for 50% read operations and 50% write operations on a single physical track.
4. Read/Write/Seek: when data is being read from or written to the disk. The head is assumed to be on-track. Implies no more than 40% of the time is spent seeking, 30% of reading and 30% of writing.
5. Max Seeking: is for continuous random seek operations with no controller delay.
6. Standby: when the motor is stopped, actuator parked, and all electronics except the interface control is in low power state. STANDBY will occur after a programmable time-out since last host access occurs. Drive ready and seek complete status exist. The drive will leave STANDBY upon receipt of a command which requires disk access or upon receipt of a spin-up command.
7. Maximum Average Current: Mean +3 Standard Deviation.
8. Power requirements reflect nominal values for +12v and +5v power supplies and do not include power required for the SCSI termination resistors.
9. Current is rms. (except for Startup)

2.5.2 Power Sequencing

No damage or loss of data will occur if power is applied or removed in any order or manner, except that data may be lost in the sector being written at the time of power loss. This includes shorting out or opening up either voltage return line, and transient voltages of +10% to -100% from nominal, while powering up or down.

2.5.3 Power Reset Limits

When powering up, the drive will remain reset (inactive) until both VHT reset limits are exceeded. When powering down, the drive will become reset when either supply voltage drops below the VLT threshold.

DC	5V Discrete		12V Discrete		5V Might		12V Might	
	(MAX)	(MIN)	(MAX)	(MIN)	(MAX)	(MIN)	(MAX)	(MIN)
VLT	4.647V[1]	4.288V	9.60V[1]	8.48V	4.65V[1]	4.40V	9.42V[1]	8.70V
VHT	4.750V	4.288V[1]	9.79V	8.48V[1]	4.65V	4.40V [1]	9.40V	8.70V[1]
Hyst	50 mV		98 mV		50 mV (TYP)		100 mV (TYP)	

Table 2-7 Power Reset Limits

Notes to Table 2-7:

1. Includes a 100 mV Peak-Peak ripple on 5V or 250 mV Peak-Peak ripple on 12V to maximize or minimize values.

2.6 Environmental

2.6.1 Environmental Conditions

The drive will meet all of its operating performance specifications when operated within its operating environment and will sustain no damage or permanent performance degradations when subjected to the non-operating environment. Where applicable, SI units as well as American Standard units have been given.

Parameter	Operating	Non-operating
Temperature non-condensing	5°C to 55°C 41°F to 131°F	-40°C to 65°C -40°F to 149°F
Temperature Gradient non-condensing	24°C/hr. Maximum	48°C/hr. Maximum
Humidity1 Max. Wet Bulb Temp.	10 to 90% RH 29°C 84.2°F	5 to 95% RH 35°C 95°F
Humidity Gradient	30% per hour	30% per hour
Altitude2	-650 to 7,000 ft -200 to 2100 m	-650 to 40,000 ft -200 to 12000 m
Altitude Gradient	1.5kPa/min	8kPa/min
Shock3	10.0 G, 11 ms, 1/2 sine 20.0 G, 3 ms, 1/2 sine	70.0 G, 11 ms, 1/2 sine 110 G, 3 ms, 1/2 sine
Vibration3 1 octave/min	1 G (p-p) 5-500 Hz	2 G (p-p) 5-500Hz

Table 2-8 Environmental Specifications

Notes to Table 2-8:

1. Humidity: these figures do not take condensation into account. See Appendix E for humidity charts for low and medium temperatures.
2. Altitude: relative to sea level.
3. NO Un-Recovered Errors.

2.6.2 Electromagnetic Conditions

2.6.2.1 EMI/RFI Susceptibility

4 volts/meter over a range of 20 Hz to 20 MHz.

2.6.2.2 Electrostatic Discharge

The drive shall mount inside the system with normal functional operation when subjected to electrostatic discharges, a minimum of 30 seconds apart from a 150 pF capacitor discharged through a 330 ohm resistor to exposed ten times to four different locations on the computer unit: two on the front and side and two on the back.

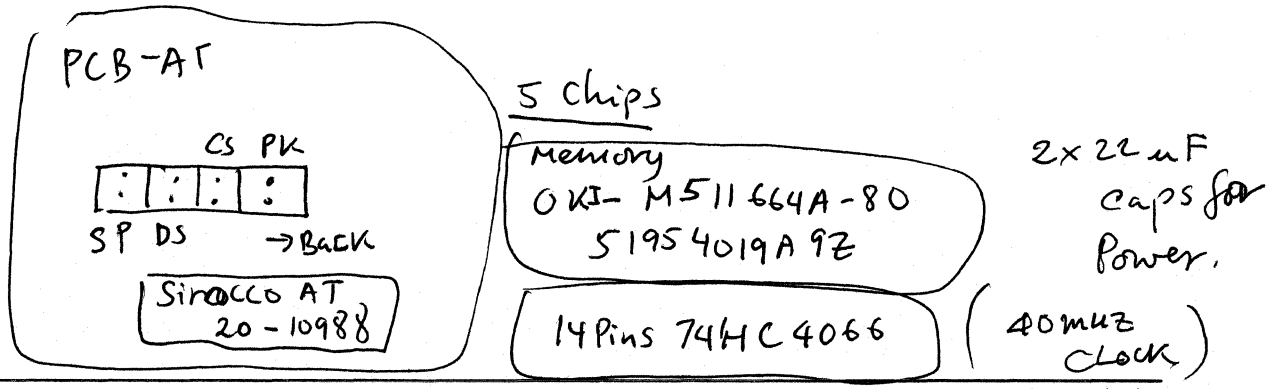
- **0 - 10 kV** Average of **<0.3** soft error per discharge
- **10 - 25 kV** no catastrophic failures

2.6.2.3 Sensitivity to Magnetic Fields

The drives will meet all specifications with less than 6 gauss field applied in any orientation.

2.7 Mechanical

Height	1.00 in (25.4 mm)
Length	5.75 in (146.2 mm)
Width	4.00 in (101.6 mm)
Weight	<1.4 lb
Spindle Motor	Integrated, Halless
Actuator	Rotary Flat Coil
Mounting Holes	See Figure 2.8.
Mounting Position	Any
Min Clearance to HDA	0.5 mm
PCB Component height	4.6 mm
Shock Mounts	None



2.8 Acoustics

Drive acoustics will be measured in a semi-anechoic chamber, with background noise at least 10dB(A) less than expected sound pressure, Lp(A).

2.8.1 Sound Power[1]

		Measured Noise
Idle on Track[2]	Lw(A)	3.6B (mean) 3.9B (mean + 3 std dev)
Seek[2,3]	Lw(A)	4.2B (mean) 4.5B (mean + 3 std dev)

Table 2-9 Acoustical specifications

Notes to Table 2-9:

1. To distinguish between sound power and sound pressure, standards specify sound power, Lw(A), in Bel, (B). 1 Bel = 10dBA.
2. The statistical values (mean and std. deviation) are to be determined separately for each drive capacity. A sample lot of 30 drives is recommended for each.
3. *Seek rate* $N_s = 0.4/(T_t + T_l)$. Where Ns = average seek rate in seeks/sec, T_t = Quantum's published time to seek from one random track to another without latency, and T_l = equivalent time, in seconds, for the drive to rotate by half a revolution. (Delay time, $T_d = 1.5T_t + 2.5T_l$). Described in section C.9.3.2 ECMA-74/ISO 7779)

2.8.2 Sound Pressure

		Measured Noise
Idle on Track[1,2,3,4]	Lp(A)	33 dBA (mean) 36 dBA (mean + 3 std dev)
Seek[1,2,4,5]	Lp(A)	40 dBA (mean) 43 dBA (mean + 3 std dev)

Table 2-10 Acoustical specifications

Notes to Table 2-10:

1. Corrections for background noise must be made if the background Lp(A) is less than 10dBA below the drive Lp(A).
2. Drive is to be tested over a reflecting plane, mounted on two one-inch thick foam blocks (3" X 4" X 1"). The microphone is to be centered one meter above the drive surface. The orientation, (i.e., pcb up or pcb down), with the greatest Lp(A) is to be used to determine conformance to spec.
3. No discrete tones. Tones to be determined using a spectral bandwidth of 1/10 octave or less, and comparing the tone level, L_t, to the arithmetic mean of the level of the masking noise, L_s, in the critical bandwidth. A discrete tone is present if : Lt - Ls > 10log (Δf/fcritical)dB.

4. The statistical values (mean and std dev) are to be determined separately for each drive capacity. A sample lot of 30 drives is recommended for each.
5. *Seek rate* $N_s = 0.4/(T_t + T_l)$. Where Ns = average seek rate in seeks/sec, T_t = Quantum's published time to seek from one random track to another without latency, and T_l = equivalent time, in seconds, for the drive to rotate by half a revolution. (Delay time, T_d, = $1.5T_t + 2.5T_l$). Described in section C.9.3.2 ECMA-74/ISO 7779)

2.8.3 Sound Quality[1]

Idle on Track[2,3,4,5]	Listening panel percentile rating of 50%
Seek[2,3,4,5,6]	Listening panel percentile rating of 50%

Table 2-11 Acoustical specifications

Notes to Table 2-11:

1. *Sound quality* measurements are qualitative and are meant to represent the actual user impression of the drive's acoustic performance.
2. Listening tests are performed using high-quality binaural digital recordings played back through headphones. Recording setup is per document XXX. Subjects rate each drive on seven-point semantic differential scales for the following attributes:

LOUD	vs	SOFT
PULSATING	vs	STEADY
WHINING	vs	NOT WHINING
INAPPROPRIATE	vs	APPROPRIATE
HARSH	vs	NOT HARSH
ANNOYING	vs	PLEASANT
LOW QUALITY	vs	HIGH QUALITY

   Overall scores are tabulated for each drive during idle and seek operation modes for comparison to competitive drives.
3. Listening panel members are selected from representative OEM customers and development engineers. No fewer than three OEMs and seven engineers should participate in listening tests.
4. Disk drive peer group should be selected by marketing and should number no fewer than two Quantum drives and four competitor's drives of most recent vintage.
5. Percentile rating = rank of overall score compared to disk drive peer group
6. *Seek rate* $N_s = 0.4/(T_t + T_l)$. Where Ns = average seek rate in seeks/sec, T_t = Quantum's published time to seek from one random track to another without latency, and T_l = equivalent time, in seconds, for the drive to rotate by half a revolution. (Delay time, T_d, = $1.5T_t + 2.5T_l$). Described in section C.9.3.2 ECMA-74/ISO 7779)

2.9 Reliability

MTBF[1] @ 55° C (Bellcore Issue #3)	**TBD POH**
MTBF[1] (Predicted Field)	**500,000 POH**
Component Life	**5 YEARS**
Contact Start/Stops[2]	**40,000**

Table 2-12 Reliability specifications

Notes to Table 2-12:

1. The Quantum MTBF numbers represent MTBF predictions per TR-TSY-000332 issue #3 Bell-Core,Sept.1990 and represent the minimum MTBF that Quantum or a customer would expect from the drive.
2. CSS specification assumes a duty cycle of 1 power off operation for every 4 idle mode spin down.

2.10 Hard Defects During Manufacture

During manufacturing and test, no drive re-allocate more than **1block/2** Megabyte, and a maximum of **TBD** blocks per surface.

2.11 SCSI Connector/Jumper

2.11.1 SCSI I/O Power Connector (J1)

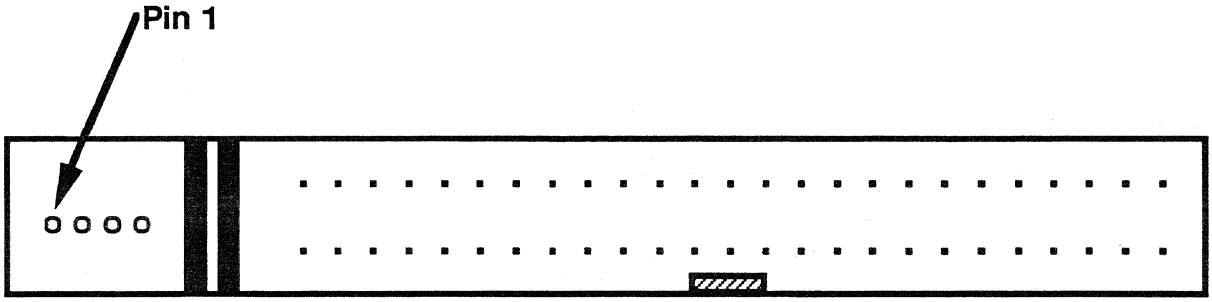


Figure 2-1 SCSI I/O DC Power Connector (J1)

Pin 1	+12.0 V DC
Pin 2[1]	+12.0 V Return (Ground)
Pin 3[1]	+5.0V Return (Ground)
Pin 4	+5.0 V DC

Table 2-13 4 Pin Power Connector pin assignments

Notes to Table 2-13:

1. Pins 2 and 3 are connected on the drive PCB.

The Combination Power/Interface Connector (J1) is mounted on the back edge of the PCB. The recommended mating connector for the 4 Pin Power connector is **(AMP P/N 1-480424-0)** utilizing AMP pins **[P/N VS 61117-4 (strip) or P/N VS 60619-4 (loose piece)]**, or equivalent.

2.11.2 SCSI 5PIN Control Connector (J5)

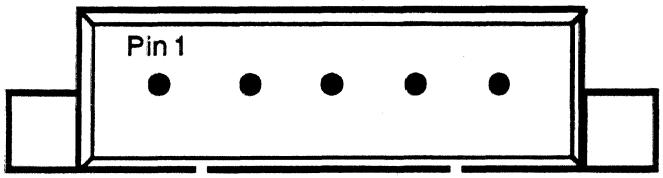


Figure 2-2 SCSI 5 pin Connector (J5)

Pin 5	Ground
Pin 4	A2
Pin 3	A1
Pin 2	A0
Pin 1	N/C (Reserved for future Sync. Spindle)

Table 2-14 5 Pin Connector pin assignments

Notes to Table 2-14:

1. The 5 pin Connector is a remote ID selector for SCSI customers only.

The recommended mating connector for the 5 pin control connector is **Molex P/N 51021-0500**, loose piece contacts is **Molex P/N 50058-8100**, or equivalent.

2.11.3 SCSI 2Pin LED Connector (J2)

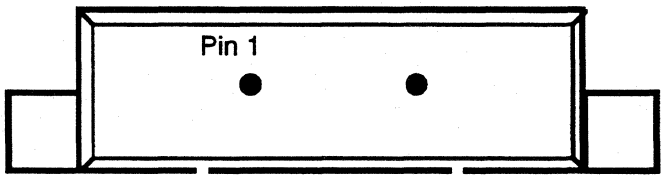


Figure 2-3 2 pin LED Connector (J2)

Pin 2	-LED
Pin 1	+LED

Table 2-15 2 Pin Connector pin assignments

Notes to Table 2-15:

1. The 2 pin LED Connector may be used to connect an external LED for monitoring drive activity.

The recommended mating connector for the 2 pin LED connector is **Molex P/N 51021-0200**, loose piece contacts is **Molex P/N 50058-8100**, or equivalent

2.11.4 SCSI JUMPER

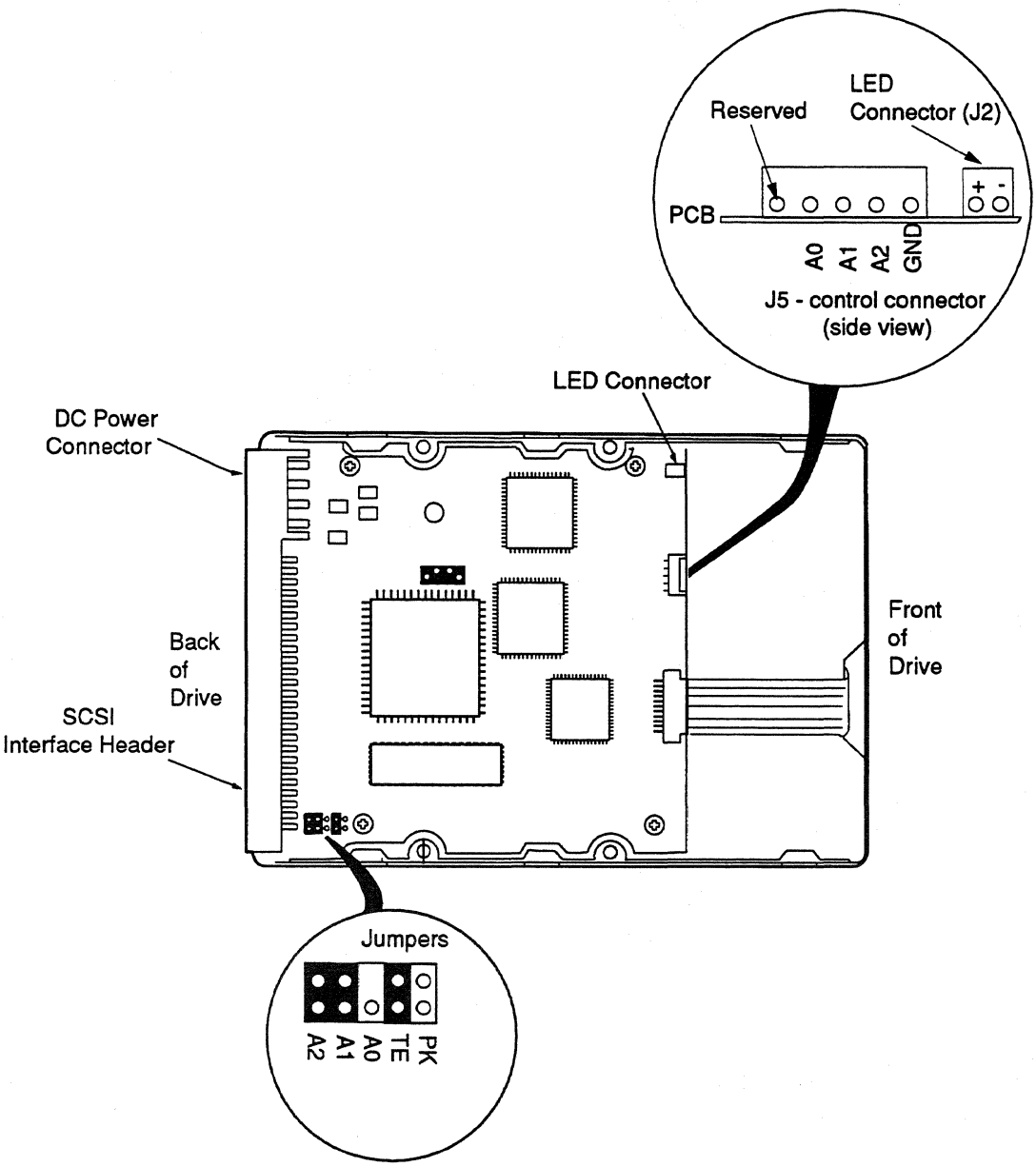


Figure 2-4 Jumper location on the SCSI PCB

A2, A1, A0	SCSI-Bus Identification
TE	Termination Enable
PK	Jumper Parking Position (enables CSS code on drives before PMP)

Table 2-16 SCSI Jumper Operational Mode

2.11.5 SCSI ID Jumper Settings

JUMPER SETTINGS			SCSI ID
A2	A1	A0	
OFF	OFF	OFF	0
OFF	OFF	ON	1
OFF	ON	OFF	2
OFF	ON	ON	3
ON	OFF	OFF	4
ON	OFF	ON	5
ON*	ON*	OFF*	6*
ON	ON	ON	7

Table 2-17 SCSI ID Jumper Configurations

Notes to Table 2-17:

1. ON indicates a jumper is installed. OFF indicates that no jumper is installed. The asterisk (*) indicates the default setting.

Used in combination, the jumper settings across pins A2,A1, and A0 determine the hard disk drive's SCSI-bus device identification (SCSI ID). By default, the drive configured with a SCSI ID of six; that is, with jumpers installed across the pins labeled A2 and A1, and no jumper installed across the pins labeled A0.

The SCSI bus supports up to eight devices, including the host system. A device's identification number determines its priority and must be unique in the system.

2.12 AT Connector/Jumper

2.12.1 AT I/O DC 3 IN 1 Power Connector

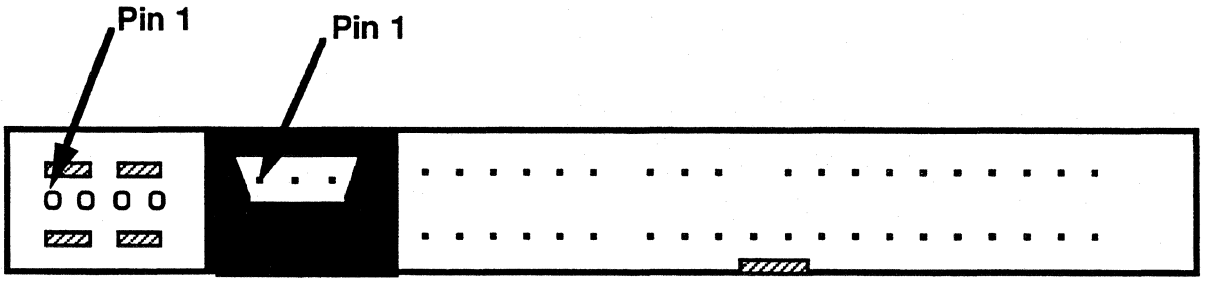


Figure 2-5 AT I/O DC 3 IN 1 Power Connector (J1)

4-Pin Power:	Pin 1	+12V DC
	Pin 2	+12 V Ground
	Pin 3	+5 V Ground
	Pin 4	+5 V DC
3-Pin Power:	Pin 1	+5 V DC
	Pin 2	+12 V DC
	Pin 3	Ground

Table 2-18 3 IN 1 3 Pin Power Connector pin assignments

Notes to Table 2-18:

1. Pins 2 and 3 are connected on the drive PCB. The combination Power/Interface connector (J1) is mounted on the back edge of the PCB. The recommended mating connector for the 4-pin power connector is AMP P/N 1-48024-0, utilizing AMP pins P/N VS 61117-4 (strip) or P/N VS 60619-4 (loose piece), or equivalent. For the 3-pin power connector, the recommended mating connector is MOLEX P/N 5484 39-27-0032 or equivalent.

2.12.2 AT JUMPER

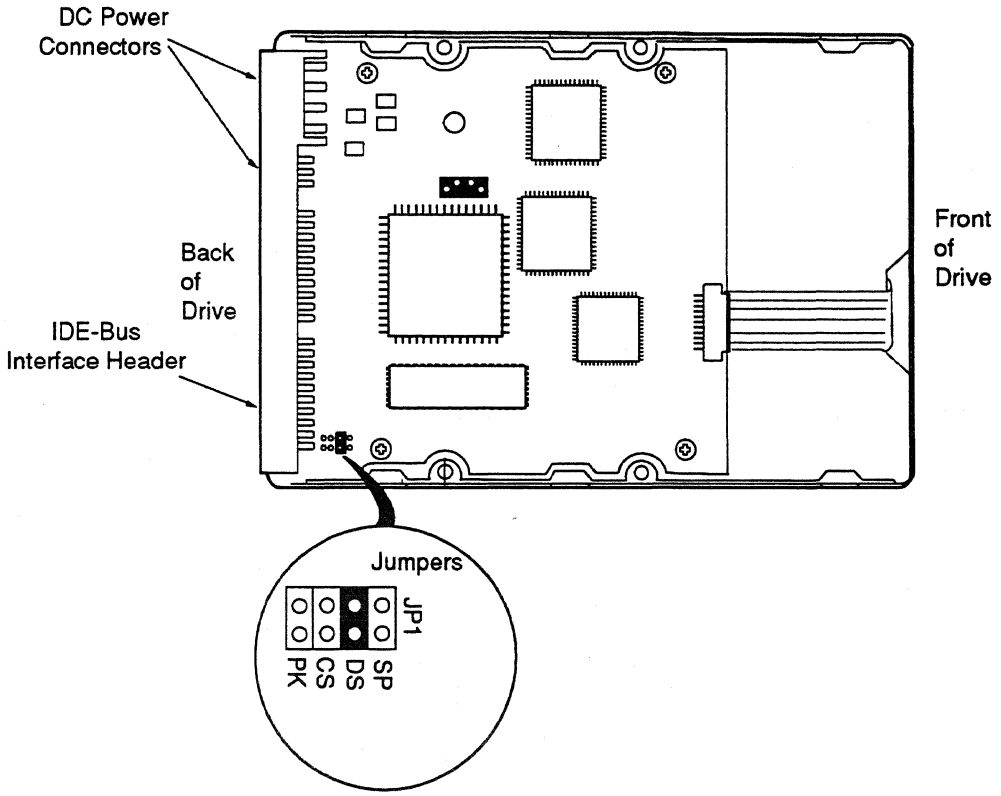


Figure 2-6 Jumper location on the AT PCB

PK	Jumper Parking Position (enables CSS code on drives before PMP)
CS	Cable Select
DS	Drive Select
SP	Slave Present

Table 2-19 AT Jumper Operational Mode

The AT PCB has three jumper locations provided for configuration options in a system. These jumpers are used to configure the drive for master/slave operation in a system.

The default configuration for the drive as shipped from the factory is with a jumper across the DS location and open positions in the CS and SP positions.

The following table defines the operation of the CS, SP, and DS jumpers and their function relative to pin 28 on the interface.

PK	CS	DS	SP	Pin28	Action
x	0	0	0	x	Drive Configured as a Slave.
x	0	1	0	x	Drive Configured as Master
x	1	0	1	open	Drive Configured as Slave
x	1	0	0	gnd	Drive Configured as Master

Table 2-20 AT Jumper Options

Note: 0 = jumper removed, 1= jumper installed, x = don't care.

2.12.3 Cable Select (CS) Jumper

With the CS jumper installed, the drive uses pin 28 of the interface connector to determine wether it is a master or slave. If pin 28 of the interface connector is grounded the drive is configured as a Master. If pin 28 of the interface is not connected, an internal pullup drives the pin high and the drive will be configured as a Slave.

2.12.4 Drive Select (DS) Jumper

For systems that do not support the cable select feature, setting a drive to master or slave requires the use of the DS jumper and removal of the CS jumper. If the DS jumper is installed the drive is configured as a Master. If the DS jumper is removed then the drive is configured as a Slave.

2.12.5 Jumper Parking (pk) Position

The PK position is used as a holding place for the jumper for a slave drive, in systems that do not support Cable Select.

2.13 Connector and Jumper Location

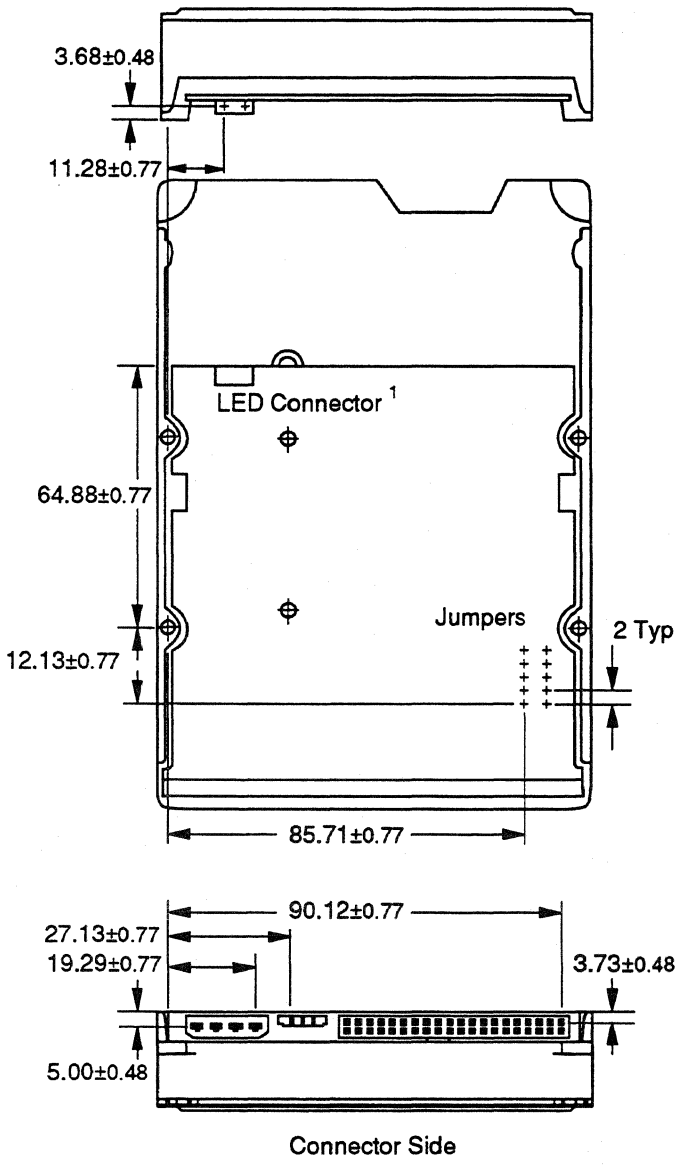


Figure 2-7 Connector and Jumper Location

2.14 Mounting

2.14.1 Orientation

Drive may be mounted in any orientation. The nominal position is PCB face down.

2.14.2 Mounting

For mounting, #6-32 UNC screws are recommended. To avoid stripping the mounting-hole threads, the maximum torque applied to the screws must not exceed 8 inch-pounds.

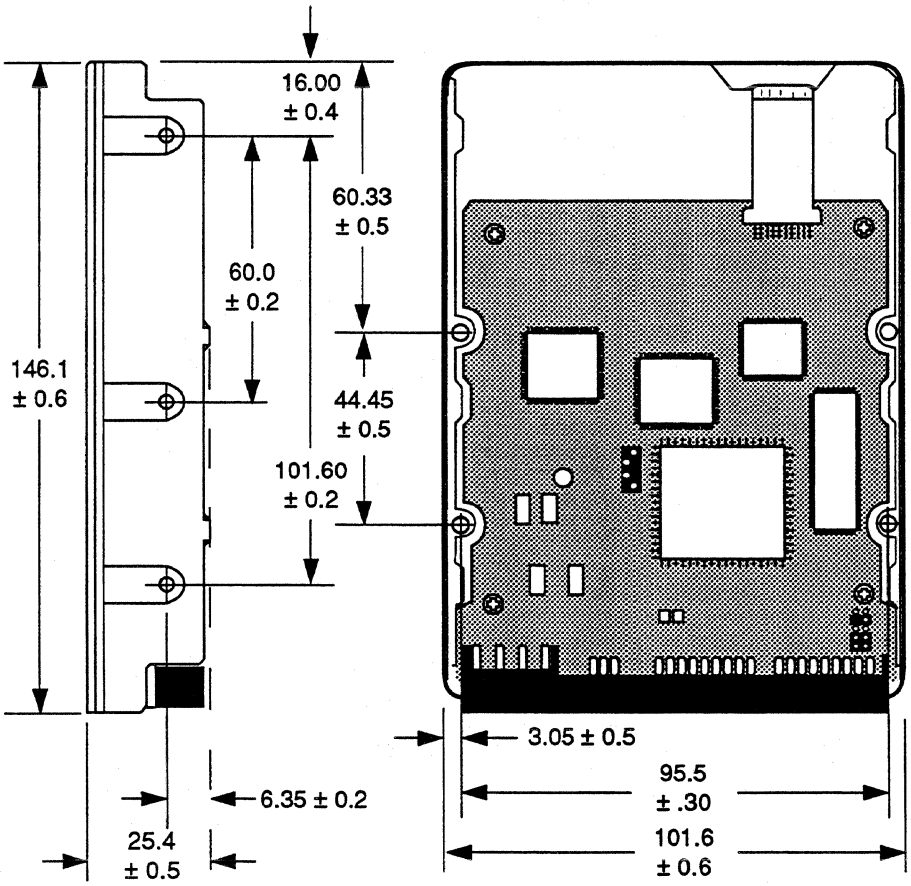


Figure 2-8 Mounting Dimensions

2.14.3 Clearance

The printed-circuit board assembly (PCBA) is very close to the mounting holes. Clearance from the drive to any other surface—except mounting surfaces—must be 1.25 millimeters (0.05 inches) minimum. Figure 2-9 specifies the clearance between the screws in the mounting holes and the PCBA. Do not use mounting screws longer than the maximum lengths specified in Figure 2-9. The specified screw length allows full use of the mounting-hole threads, while avoiding damaging or placing unwanted stress on the PCBA.

2.14.3.1 HDA Mounting Screw Clearance

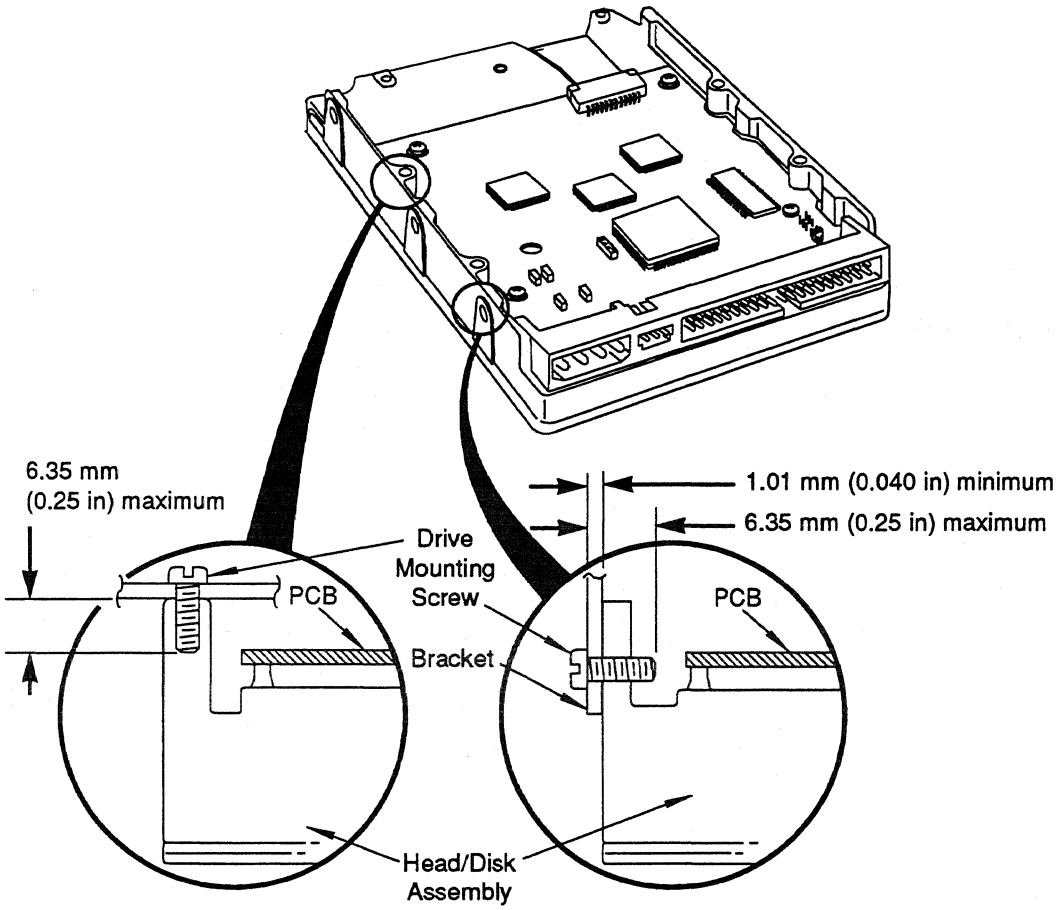


Figure 2-9 Mounting Screw Clearance

Notes to Figure 2-9

The Printed-Circuit Board (PCB) is very close to the mounting holes. Do not exceed the specified length for the mounting screws. The screw length should allow full use of the mounting-hole threads, while avoiding damaging or placing unwanted stress on the PCB.

Figure 2-8 specifies the minimum clearance between the PCB and the screws in the mounting hole. To avoid stripping the mounting-hole threads, the maximum torque applied to the screws must not exceed 8 inch-pounds.

2.15 Passport XL Support

To support the Passport product the following existing hardware and firmware hooks must be maintained in the new designs as they are developed. The following set of guidelines have been recommended by engineering.

- Four (4) QCP (Quantum Communication Port) Pads on the top side of the drive PCB. Please use the same square configuration that was used on previous designs. Three of the pads should be connected to three bi-directional I/O port pins on the Microprocessor. The fourth pin is a no connect pin. If possible, locating the pads in the same location as on the previous generation drive will minimize support efforts.
- An EPROM, jumper or some other method to allow the firmware to recognize the drive as a Passport.
- Firmware hooks are needed as follows:
  - Install hooks for SCSI commands 1B (Load/Unload) and 1E (Prevent/Allow Medium Removal).
  - Install hooks for Superset commands F3 (Group Read), F4 (Group Write) and F6 (Lock/Unlock).
  - Allow for support to patch Inquiry and Sense commands as the point where data is send to the host.

Sirocco provides the 4 required pads, all 4 pads are connected to microprocessor port pins. The NO connect requirement is done by programming into a tri-state condition. An EEPROM mode is used for passport recognition.

Passport XL is supported on SCSI interface drives only.

Section 3 Track Specifications

The Sirocco disk drives are shipped from the factory as "hard sectored" drives. That is, all physical sector addresses are written on the disks before the drives are shipped. As a result, sector size and number of sectors per track are not user selectable. The information given in this section is the physical format of Sirocco as it is defined at the factory prior to shipment.

Note that the physical format is in contrast to the logical format of the drive, which is how the drive appears to the host system.

3.1 Track Locations

Location	Description	Radius	Slider Radius @ Gap	Slider Radius @ Inside Corner of Flexure	Slider Radius @ Outside Corner of Slider	Clearance
OD	OD edge of disk (Nom)	47.500				
OD	Disk chamfer (Nom)	47.320				
OD	Slider ABS to chamfer clearance-crash comp allowance (Nom)					1.109
OD	Slider ABS to chamfer clearance-crash comp allowance (-3sig)					0.689
OD	Touch outer crash stop (+3sig)		46.480		46.631	
OD	Touch outer crash stop (Nom)		46.060		46.211	
OD	Touch outer crash stop (-3sig)		45.640			
OD	Guard band allowance-thermal					0.110
OD	System cylinder start : Cyl -20 (Nom)		45.973			
OD	Zone 1 outside radius: Track 0 (Nom)		45.887			
ID	Zone 15 inside radius: Track 5899 (Nom)		20.280			
ID	System cylinder end: Cyl 5900-5925 (Nom)		20.168			
ID	Touch airlock stoP (+3sig)				20.140	
ID	Touch crash stop (Nom)		18.710	17.220		
ID	Touch crash stop (-3sig)		18.260	16.760		
ID	Flexure to hub clearance-crash comp allowance (Nom)					1.707
ID	Flexure to hub clearance-crash comp allowance (-3sig)					1.242
ID	Hub radius	15.500				

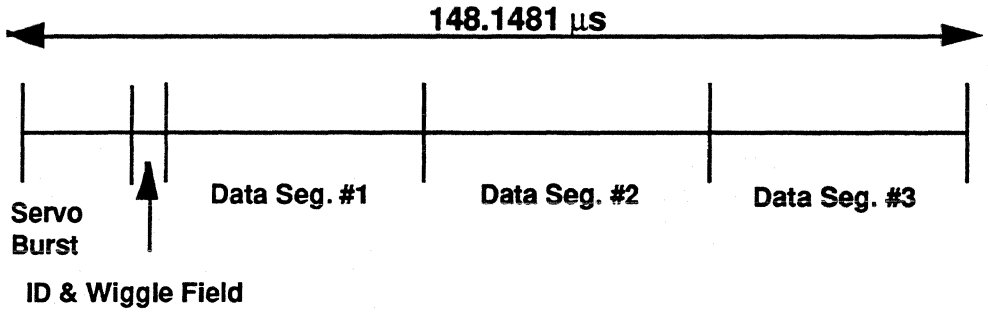
Table 3-1 Track Locations

Notes to Tables 3-1 and 3-2:

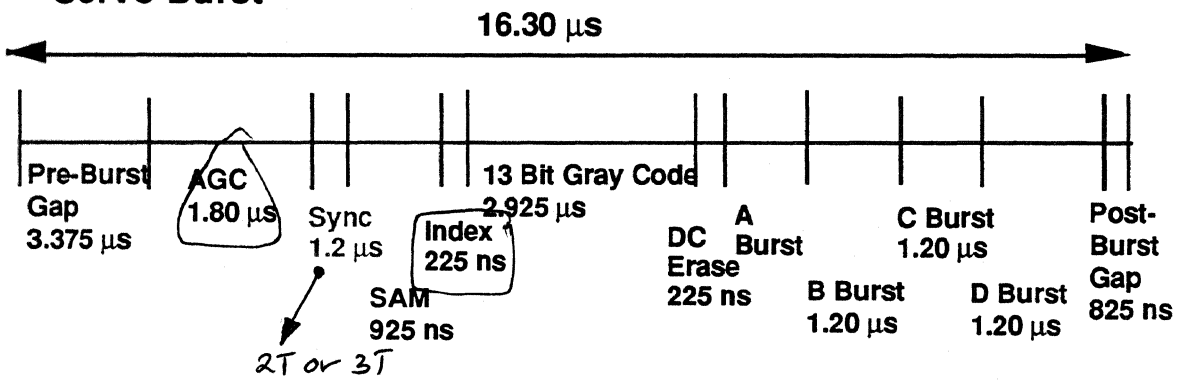
1. Actuator sweeps out an angle of 29.38° from crash stop to crash stop.
2. From the start of the data to the end of the data, the pivot angle is 27.74°

3.2 Track Format

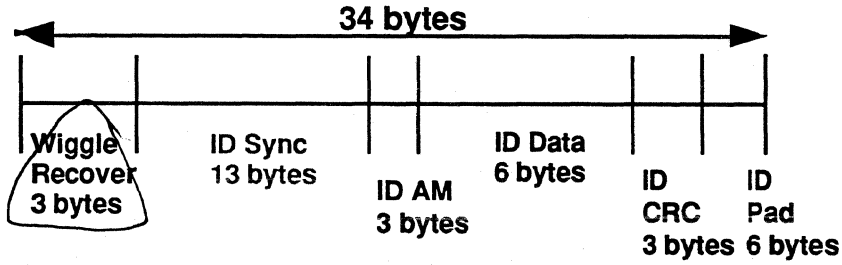
Wedge (90 x's per rev)



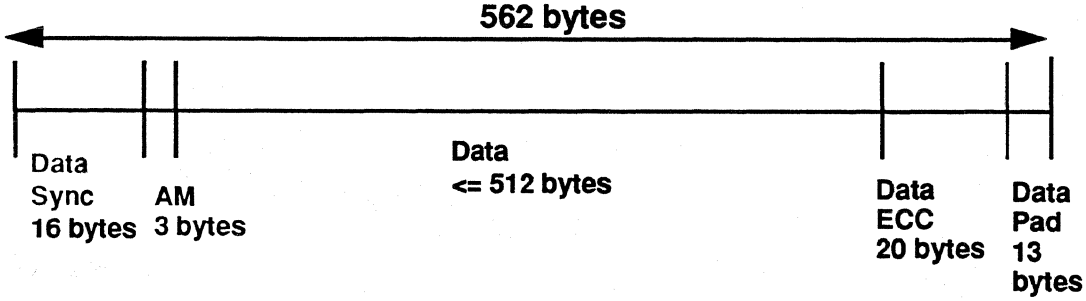
Servo Burst



ID and Wiggle Field



Data Segment



Zone #	Zone Outside Radius	Zone Inside Radius	# Cyl.	Sectors/ Track	Sectors/ Zone	Byte/ Sector	Sector Time (us)	Data Rate (Mb/s)	Write Clk (MHz)	Fmax (MHz)
G. Band		1.8104	14	N/A	N/A	N/A	N/A	N/A	N/A	N/A
System	1.8104	1.8069	20	139	2780	512	78.32	57.10	60.667	30.333
0	1.8069	1.7405	389	180	70020	512	61.98	72.16	76.667	38.333
1	1.7405	1.6760	377	180	67860	512	61.98	72.16	76.667	38.333
2	1.6760	1.6150	357	174	62118	512	63.07	70.90	75.333	37.667
3	1.6150	1.5522	367	171	62757	512	64.21	69.65	74.000	37.000
4	1.5522	1.5066	267	167	44589	512	65.39	68.39	72.667	36.333
5	1.5066	1.4087	573	156	89388	512	69.88	64.00	68.000	34.000
6	1.4087	1.3630	267	153	40851	512	71.27	62.75	66.667	33.333
7	1.3630	1.3003	367	146	53582	512	74.24	60.24	64.000	32.000
8	1.3003	1.2375	367	140	51380	512	77.47	57.73	61.333	30.667
9	1.2375	1.1577	467	135	63045	512	80.08	55.84	59.333	29.667
10	1.1577	1.1121	267	131	34977	512	81.92	54.59	58.000	29.000
11	1.1121	1.0422	397	123	48831	512	86.92	51.45	54.667	27.333
12	1.0422	0.9815	367	117	42939	512	91.38	48.94	52.000	26.000
13	0.9815	0.9239	337	110	37070	512	96.31	46.43	49.333	24.667
14	0.9239	0.8611	367	103	37801	512	101.82	43.92	46.667	23.333
15	0.8611	0.7984	367	96	35232	512	109.65	40.78	43.333	21.667

Table 3-2 Zone Specifications

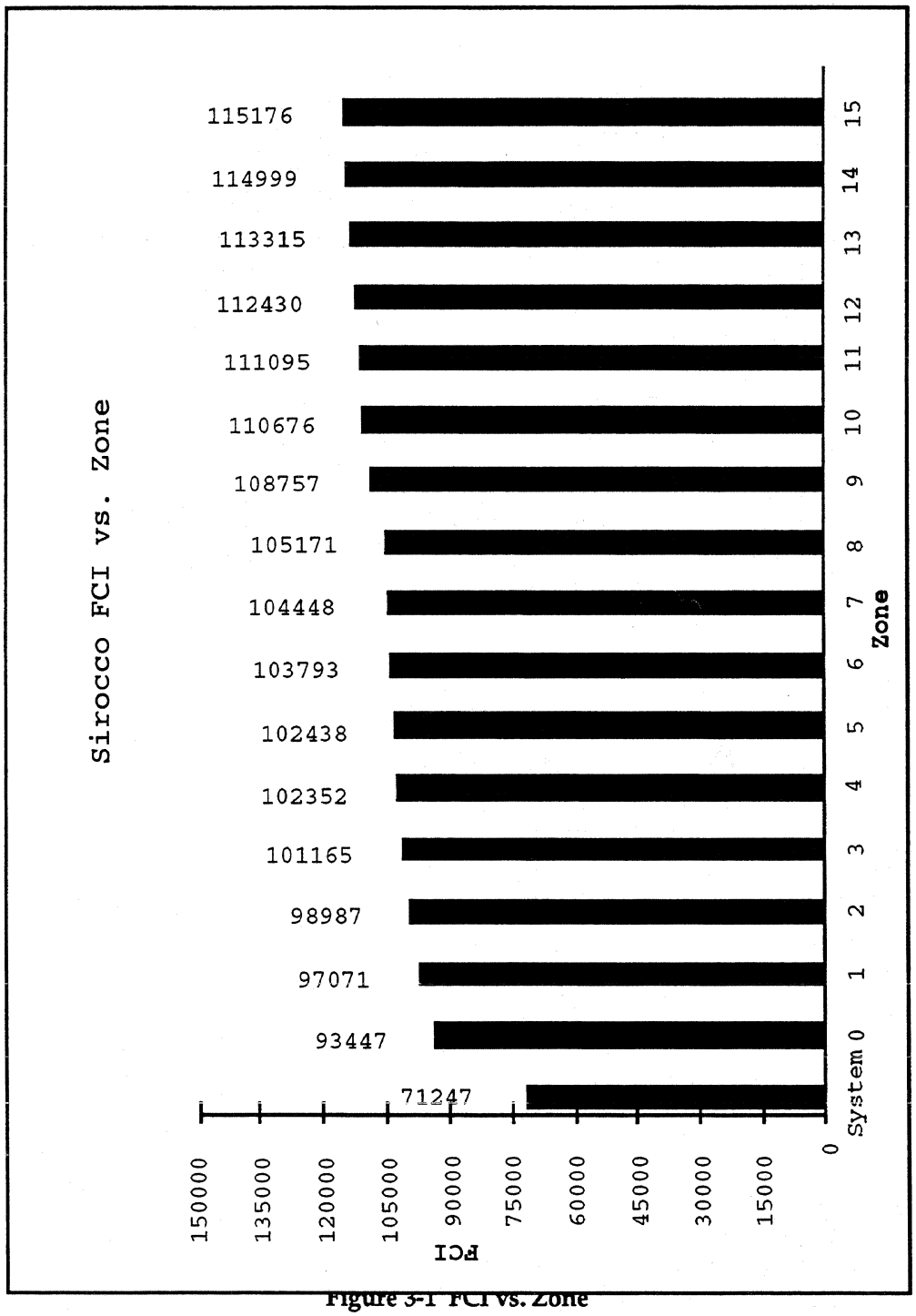


Figure 3-1 FCI vs. Zone

3.3 Cylinder Contents

Cylinder Contents	Zone	Cylinder Range	Date Rate Mb/S	Sectors Per Track
Servo Inner Guardband	15	5920 to 5925	N/A	N/A
3X Sample Rate	15	5917 to 5919	N/A	N/A
Guard band	15	5916	N/A	N/A
S/W Information	15	5911 to 5915	N/A	N/A
S/W Serial Number	15	5905 to 5910	N/A	N/A
Guard Band	15	5904	N/A	N/A
Microjog Calibration	15	5901 to 5903	N/A	N/A
Guard Band	15	5900	N/A	N/A
User Data	15	5533 to 5899	40.78	96
	14	5166 to 5532	43.92	103
	13	4829 to 5165	46.43	110
	12	4462 to 4828	48.94	117
	11	4065 to 4461	51.45	123
	10	3798 to 4064	54.59	131
	9	3331 to 3797	55.84	135
	8	2964 to 3330	57.73	140
	7	2597 to 2963	60.24	146
	6	2330 to 2596	62.75	153
	5	1757 to 2329	64.00	156
	4	1490 to 1756	68.39	167
	3	1123 to 1489	69.65	171
	2	766 to 1122	70.90	174
	1	389 to 765	72.16	180
	0	0 to 388	72.16	180
Guard Band	No Access	-1	N/A	139
System	System	-2	57.10	139
Copy of -2	System	-3	57.10	139
Diskware	System	-4	57.10	139
Copy of -4	System	-5	57.10	139
Compressed Test Data	System	-6	57.10	139
Records Data	System	-7	57.10	139
Test Equip Data/Error	System	-8	57.10	139
Self Scan Results	System	-9	57.10	139
Guard band	No Access	-10	N/A	139
Microjog Calibration	System	-11 to -13	57.10	139
Guard band	No Access	-14	N/A	139
Servo Outer Guard Band	System	-15 - -17	N/A	139
3X Sample Rate	System	-18 to -20	57.10	139

Table 3-3 Cylinder Contents Breakdown.

Notes to Table 3-3:

1. Zone 0 is the outermost zone, zone 15 is the innermost zone.
2. Six cylinders on all drives are reserved for system, Diskware and test usage. These cylinders contain drive configuration information, drive test information, and diskware. Customers cannot access these reserved cylinders. The reserved cylinders are only accessible with physical address commands which are protected diagnostic commands.
3. Data is repeated on cyl -2 and cyl -3, also repeated on cyl -4 and cyl -5, and is stored in the OD system areas for redundancy. Data is read from and written to these areas according to the firmware redundancy algorithm.
4. The test equipment cylinder is reserved for test equipment usage. This cylinder contains test parameters and data collected during production test. Writing on this cylinder may erase some important information and cause the drive to be rejected and sent back to the servo writer station.

   The sector usage is as follows:

Sector	Usage
0	Copy of Servo writer Serial Number Data
1	Test Process Interlock
2	Reserved.. for Reclassification .. NA on Sirocco
3	Configuration Center Control
4	Reserved... for Expansion
5 - 14	Test Process History Que
15 - 30	Process Test Defect List
31	Error log. (Header and count need for Apple burn-in)
32 - 40	Self Scan results
41 - 48	Self Scan test parameters
49 - 59	Self Scan defect list
60 - 61	Self Scan - PRO/NPRO results
62 - 63	Servo defect map
64 - 65	Self Scan command history
66 - 70	Adaptive Results
71 - 94	Selfscan overlay number 1. (12K = 12*2= 24)
95 - 110	Selfscan overlay number 2. (8K = 8*2= 16]
111 -126	Selfscan overlay number 3. (8K = 8*2= 16]
127 -138	Reserved for in-line defect sparing

5. The System cylinder is reserved for system usage. It contains ① mode page information, ② configuration information, ③ defect lists, and ④ format information for the drive. Writing on this cylinder may erase some important information and prohibit the drive from operating.

   The sector usage is as follows:

Sector	Usage
0	Saved mode pages.
1 - 8	Configuration pages
9 - 16	Working defect list
17 - 24	Primary defect list
25 - 32	Temporary defect list (may not be needed)
33 - 48	Format header bytes - zone 0-15
49	Apple system sector/ Servo Recall record
50	Passport sector

51	Servo defect list
52 - 61	Log sense and Log select
62 - 121	Error log.(detail log)
122 -138	Reserved for in-line defect sparing

6. The Diskware cylinder is reserved for Diskware usage. The data is repeated on cyl -5.

   The sector usage is as follows:

Sector	Usage
0 - 1	Boot Loader
2 - 113	Diskware 56K segment
114 - 126	Not in use
127 - 138	Reserved for in-line defect sparing

7. The -6 Cylinder contains compressed test.out file.

0 - 126	Test.out files
127 - 138	Reserved for in-line defect sparing

* Preliminary Spec. Subject to change

3.4 Track and Cylinder Skewing

Head Switch 3.0 ms RPM 4500 WORST CASE: (± 0.25%)

Single SEEK 3.5 ms

Zone Number	Sect/ TRK	uSecs/ Sect	Raw Track Skew	Rounded Track Skew	Number Of Cyl.	uSecs/ Sect	Raw Cyl. Skew	Rounded Cyl. Skew
0	180	61.98	TBD	TBD	389	61.98	TBD	TBD
1	180	61.98	TBD	TBD	377	61.98	TBD	TBD
2	174	63.07	TBD	TBD	357	63.07	TBD	TBD
3	171	64.21	TBD	TBD	367	64.21	TBD	TBD
4	167	65.39	TBD	TBD	267	65.39	TBD	TBD
5	156	69.88	TBD	TBD	573	69.88	TBD	TBD
6	153	71.27	TBD	TBD	267	71.27	TBD	TBD
7	146	74.24	TBD	TBD	367	74.24	TBD	TBD
8	140	77.47	TBD	TBD	367	77.47	TBD	TBD
9	135	80.08	TBD	TBD	467	80.08	TBD	TBD
10	131	81.92	TBD	TBD	267	81.92	TBD	TBD
11	123	86.92	TBD	TBD	397	86.92	TBD	TBD
12	117	91.38	TBD	TBD	367	91.38	TBD	TBD
13	110	96.31	TBD	TBD	337	96.31	TBD	TBD
14	103	101.82	TBD	TBD	367	101.82	TBD	TBD
15	96	109.65	TBD	TBD	367	109.65	TBD	TBD

Assumptions made:

1. All skew numbers with tenth digit ≥ 0.01 were rounded up to the next integer.

2. Worst case RPM was used to give a slightly larger safety margin.

Since the Sirocco drives are storage subsystems with integrated controllers, the function and design of the controller can be optimized specifically for the drive. One method of optimization employed by Quantum to improve data throughput is skewing sector addresses. The purpose of track and cylinder skewing is to minimize latency time and thus increase data throughput when data is sequentially accessed to or from the disk. The two types of skewing employed, track and cylinder skewing, are described below.

3.4.1 Track Skewing

Track skewing reduces latency time which results when the drive must switch read/write heads to access sequential data. A track skew is employed such that the next logical sector of data to be accessed will be under the read/write head once the head switch is made and data is ready to be accessed. Since head switch times are defined on Sirocco, the sector addresses can be optimally positioned across track boundaries to minimize the latency time which results when a head switch has to be performed.

3.4.2 Cylinder Skewing

Cylinder skewing is also used on Sirocco to minimize latency time during sequential accessing of data. However, instead of minimizing latency time due to head switching, as with track skewing, cylinder skewing is used to minimize latency time due to a single-cylinder seek. The next logical sector of data which crosses a cylinder boundary is positioned on the drive such that after a single-cylinder seek is performed, and the drive is ready to continue accessing data, the sector to be accessed is positioned directly under the read/write head. Therefore, the cylinder skew takes place between the last sector of data on the last head at a cylinder and the first sector of data on the first head at the next cylinder. Since single-cylinder seek times are defined on the drive, the sector addresses can be optimally positioned across cylinder boundaries to minimize the latency time which results when a seek has to be performed.

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Section 4 Mechanical

4.1 Motor

The 3.5" spindle motor to be used in the Sirocco Hard Disk Drive has a "doubly supported shaft" design that is integral to the drive base.

4.1.1 Reference Documents

Base Motor Assembly	75-108273-XX
Disk 95mm X 25mm X 0.8mm	61-109199-01
Disk Clamp	40-108854-01 (2 Disks) 49-109438-01 (3 Disks)
Disk Spacer	40-108865-01
Cover	49-108586
Spindle Motor Driver	Mighty

Table 4-1 Reference documents for spindle motor

4.1.2 General Specifications

Number of Poles	12
Number of Phases	3
Motor Type	Brushless DC
Driving Mode	BiPolar Y, with center tap
Commutation	Back- emf (Hall-less)
Number of Stator Slots	9
Mounting Orientation	Any Orientation
	Flex Circuit Pin Descriptions
	Pin 1 u
	Pin 2 v
	Pin 3 w
	Pin 4 center tap

Table 4-2 General specifications for spindle motor

4.1.3 Operating Parameters

Rotational Speed		4500 RPM ± 0.2%
Direction of Rotation (hub side view)		Counterclockwise
Operating Load		
	Inertial Load	Mass load
2 Disk	354 gm-cm^2	34 g
3 Disk	526 gm-cm^2	48 g
Spin Up Time (from power on to 4500 RPM)		< 5 sec

Table 4-3 Performance specifications for spindle motor

4.1.4 Mechanical Characteristics

Bearing Vendor	NMB or NSK
Bearing Size	5x13x3 mm
Bearing PreLoad	1.0 - 2.0 kg
Ball Complement	8x2.0 mm Diameter
Lubrication	Multemp
Rotor Hub Inertia	≤ 25 gm-cm^2
Frictional Load	TBD
Starting Torque	132 gm - cm@ 1A
Running Torque	TBD
Repetitive Run-out (RRO)	Radial< 300 µin (p-p) Axial< 400 µin (p-p)
Non-Repetitive Run-out (NRRO)	Radial< 8 µin (p-p) AxialN/A
Balance	≤ 0.05 gm-cm
Acoustic noise	< 30 dBA @ 1 m < 44 dBA @ 1/4 m
Seal Type	Labyrinth

Table 4-4 Mechanical specifications for spindle motor

4.1.5 Electrical Characteristics

Supply Voltage Requirements	12 V (DC) ± 10%
Driver Resistance	TBD TBD
Current Sense Resistance	TBD
Coil Resistance (2 phase) Coil Inductance (f =1kHz, line to line or 2 phase)	6.0 Ω ± 8% 1.80 mH (max.)
Torque Constant	166 gmf-cm/amp
Back EMF (4500 RPM)	8.0V± 5%
Average Running Current	56 mA (no load)
Magnetic Flux Leakage[1]	< 6Gauss
Spin Up Time	< 5 Sec
Phase Windings	 Wire diameter0.17 mm # of turns81/slot
High Voltage Insulation[2]	250 V DC @ 1 Sec, 1mA

Table 4-5 Electrical specifications for spindle motor

Notes to Table 4-5:

1. Measured in any orientation at a radius of 20 mm from the motor centerline.
2. Breakdown voltage measured @ between motor frame and coil lead wire or winding. The resistance of the insulation must exceed 50 MΩ when tested @ 500 volts DC.

4.1.6 Materials

Hub	Aluminum Alloy T-6061 or A-2011
Magnets	Plastic bonded Nd Fe B, NP11L
Shaft	Martensitic stainless steel (series 400) passivated

4.1.7 Environment

	Operating	Non-Operating	Storage
Temperature	5°C to 55°C 41°F to 131°F	-40°C to 65°C -40°F to 149°F	-40°C to 70°C -40°F to 167°F
Humidity[1] Max wet bulb	8% to 85% RH 29°C	5% to 95% RH 35°C	
Altitude	-650 to 10,000 ft -200 to 3000 m	-650 to 40,000 ft -200 to 12,000 m	
Shock[2]	10 G, 11 ms, 1/2 sine 20 G, 3 ms, 1/2 sine	70 G, 11 ms, 1/2 sine 110 G, 3 ms, 1/2 sine	
Vibration [3]	1G 5-500 Hz (p-p)	2G 5-500 Hz (p-p)	

Table 4-6 Environment specifications for spindle motor

Notes to Table 4-6:

1. No condensation allowed.
2. Half sine wave shock in 3 mutually perpendicular axes; 3 shocks for each axis.
3. Sine Sweep 1 octave/minute on 3 mutually perpendicular axis.

4.1.8 Quality Assurance Provisions

4.1.8.1 Burn In

All motors shall be "burnt in" at 75°C for 7 hours (motor not running).

4.1.8.2 Reliability

The L1 life is to be greater than 44,000 hours.

4.1.9 Cleanliness

4.1.9.1 Cleanliness of Assembly Area

The motor shall be assembled and sealed in an individual bag in a Class 100 cleanliness area.The assembly area must be maintained for the specified cleanliness.

4.1.9.2 Particles from the Motor

Under running conditions, the motor must support the Class 100 cleanliness environment when measured one minute after start-up.

Particulate generation allowable per cubic foot of air when operating at 4500 rpm:

< 20 particles 0.1 to 0.8 micron

4.1.9.3 Visual Inspection

The motor shall be free of dirt, chips and other foreign materials.

4.1.10 UL, CSA TUV and VDE Requirements

4.1.10.1 Components and Materials

All parts, components and materials must meet or exceed the minimum requirements for UL, CSA, TUV and VDE as required for electronic equipment.

4.1.10.2 Flexible Circuit Specifications

Any flexible circuit elements used must be capable of meeting the UL, VW-1 Vertical Flame Test or 94 v-2 rating as assembled in the motor.

4.1.10.3 Vendors

If required in order to obtain certification for the complete motor assembly, any parts, materials and components (including printed circuit boards) must be manufactured by vendors approved by UL, CSA TUV and VDE.

4.1.10.4 Certification Cards

UL, CSA TUV and VDE certification cards for affected parts and materials are required for initial qualification and changes.

4.2 VCM

- Rotary Flat Coil Actuator.
- Double Bipolar Magnet Neodymium
- Cold Rolled Steel Return Plates SAE 1006-1010 2.3mm thick

4.2.1 Specifications

• Torque constant	730 gm-cm/A
• Flux in gap	7900 gauss (max)
• Magnet material	41 MgOe, NdFeB
• Coil Resistance	11.2 Ω @ 22°C
• Number of turns	180
• Actuator Imbalance	< 1 gm-cm
• Bearing	9mm OD x 5mm ID x 3mm Thick 10 x 3/64 diameter Balls

4.3 Actuator

• Die Cast Aluminum E- Block	ADC 12
• Copper Magnet Wire (insulated)	0.160 mm diameter
• Overmold	PPS EC-10
• Total Weight of moving mass	2-Disk 10.06 gm 3-Disk 11.0 gm
• Total Inertia	2-Disk 43.00 gm-cm^2 3-Disk 43.00 gm-cm^2

4.4 Latch

Magnetic return spring air lock/unlock—leveraged from current Fireball design

4.5 Crash Stops

Plastic cantilever—leveraged from current Fireball design

4.6 FPCB (?)

- Conventional MR Pre-Amp package mounting techniques, miniature 38-pin package
- Accommodate MR Pre-Amp size, pin-out and external components for actuator mounting
- Minimize bias force over stroke with short loop length
- ZIFF connection to PCB

4.7 Base/Cover/PCB

• Cast Base	thickness varies per design
• Flat Cover	1.0 mm thick total
• Acoustic Foam	≈ 2.0 mm Polyurethane Foam
• Motor Connector	header/receptacle

Section 5 Heads/Media

5.1 Heads

The following table lists the Sirocco head specifications.

Specification	Value
TPI, FCI	5850, 115K (max)
Channel	(0,4/4)8/9, PRML
Write Width	3.5±0.40 µm, **Measured Optically**
Write Pole (P2) Thickness	3.5±0.35 µm, (Reference Spec)
Write Gap	0.4 µm (Reference Spec)
Write Head Turns	12 to 15
Write Current	25 mA (base_peak)
Write Inductance @ 1 MHz	< 250 nH
Write Resistance	< 22 Ω
Read Width	2.6 ± 0.3 µm, **Measured Magnetically**
Read Gap (shield-shield)	0.3 µm± 0.05 (Reference Spec)
Mid Shield (P1 Thickness)	3.0 µm nominal (shared pole design)
R/W Separation	3.55 µm nominal and 4 µm max
R/W Offset	0.58 ± 5 µm, as measured optically **(subject to change)**
R/W Magnetic Offset	0 ± 0.8 µm at radius MD, as measured magnetically
Read DC Resistance	15 to 30 Ω
Read Inductance @ 1 MHz	<= 50 nH
Bias Current	12 to 14 mA
Flying Height[1]	2.75 (nominal) 2.25 µinch (minimum) at lowest point
Head Overcoat	<= 0.01 µm
Gram Load	5.0 grams ±0.5
Suspension	Type 850 LSF through etch, low-profile swage, 2.5 mil load beam
HTI P/N	0111652 for UF and 0111656 for DF
NHK P/N—FA7302L000	FA7302L000 for UP and FA7302R000 for DF
Wire/Tube	Semi-tubeless wire MR (Red +, Grn -) TF (Blk, Blk)
Overweight	0.25
HFTAA p-p @ any track	575 µV (nominal) and 500 µV (minimum)
PW50	380 nm (nominal) and 460 nm (maximum)
OW (4T/16T)	> 32dB
Amplitude COV	< 2.5%
Resolution (16T/4T)	> 70%
Amplitude Asymmetry	-15% to + 15%
NLTS, 5th Harmonic	< -12 dB

1. Fly height values a referenced to the surface of any head overcoat (i.e., includes the DLC) and measured with a PhaseMetrics AFHT tester with 1.8 mil spot size or with an equivalent fly height tester that us correlated to Quantum's PhaseMetrics tester.

5.1.1 Test Media

Specification	Value
Hc	2200 Oe
MrT	1.2 memu/cm^2
Carbon overcoat	≤ 150A°
Glide	1.5 µinch
CSS	40,000 cycles
Coefficient of stiction	<= 1.5

5.1.2 Test Conditions

ID Gap Radius	0.830"	ID HF Freq	11.80 MHz
ID Gap Skew	0.0°	ID LF Freq	2.95 MHz
ID Gap Radius	1.252"	MD HF Freq	18.2 MHz
ID Gap Radius	9.5"	MD LF Freq	4.55 MHz
ID Gap Radius	1.798"	OD HF Freq	23.6 MHz
ID Gap Radius	19.5"	OD LF Freq	5.90 MHz

5.2 Media

5.2.1 Mechanical Characteristics

Specification	Value
Disk Substrate	95 mm x 25 mm, aluminum, 31.5 mil thick
Media	Thin Film
Carbon Overcoat	15 nm maximum

5.2.2 Magnetic Characteristics

Specification	Value
Hc	2200 Oe ±100
MrT	1.0 to 1.2 memu/cm^2
Carbon Overcoat	≤150A°

5.2.3 Mechanical Performance Requirements

Specification	Value
Glide[1]	1.5 µinch maximum
Glide Avalanche	1.2 µinch
CSS	40,000 cycles under environmental conditions
Stiction Coefficient	<= 1.5

1. Fly height tester used to characterize Glide heads must be PhaseMetrics AFHT with 1.8 mil spot size or an equivalent tester that is correlated to Quantum's PhaseMetrics AFHT with 1.8 mil spot size.

5.2.4 Electrical Performance Requirements

Specification	Value
HFTAA p-p @ any track	5 75 µV (nominal) and 500 µV (minimum)
PW50	380 nm (nominal) and 460 nm (maximum)
OW (4T/16T)	> 32dB
Amplitude COV	< 2.5%
Resolution (16T/4T)	> 70%
Amplitude Asymmetry	-15% to + 15%
MP Defect Avalanche Threshold	>= TBD
EP Defect Avalanche Threshold	<= TBD

5.2.5 Test Head

Specification	Value
Head Type	MagnetoResistive
Flying Height w/ DLC OC	2.75 (nominal) 2.25 µinch (minimum)
Head Overcoat	<= 0.01 µm
Height	0.029"

5.2.6 Test Conditions

ID Gap Radius	0.830"	ID HF Freq	11.80 MHz
ID Gap Skew	0.0°	ID LF Freq	2.95 MHz
ID Gap Radius	1.252"	MD HF Freq	18.2 MHz
ID Gap Radius	9.5"	MD LF Freq	4.55 MHz
ID Gap Radius	1.798"	OD HF Freq	23.6 MHz
ID Gap Radius	19.5"	OD LF Freq	5.90 MHz

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Section 6 Drive Electronics

6.1 Read Channel Piranha

ATT 91C04SA
9535A-ESN
2104974

The ATT 91C04 is a complete read channel device, including not only the read channel, but an ENDEC, servo demodulator, write precompensation, clock synthesis, quality monitoring, and power down options. The read channel utilizes adaptive equalization to force a class IV partial response and Viterbi detection of the resulting sequence to allow the realization of the higher areal densities.

6.1.1 Read Channel Piranha Features:

- Custom LSI, single chip, 44pin PLCC
- Single +5V supply
- Low power consumption (400 mW typical)
- Power down mode:<5 mW
- Capability of handling up to 85 MBits/sec data rates
-
- 5 step, 12 dB range input attenuator extends AGC range
- AGC digitally controlled in READ mode, analog control in SERVO mode
- 4th order Butterworth continuous time data filter with 2 independently programmable zeroes
-
- 10 tap discrete time adaptive FIR equalizer with digitally controlled tap weights
-
- DFE equalizer with digitally controlled tap weights for trailing and leading undershoot cancellation of thin film head (not used in Sirocco)
-
- Interleaved dicode Viterbi detectors
- Encode supports 8/9 and 16/17 density codes: includes preamble generation, sync mark generation, fault tolerant sync mark recognition and scrambling
-
- Write data outputs programmable CMOS or low- noise differential pseudo- ECL
-
- Quality monitor flags high error rate conditions and measures rms noise
- Generates own late1, late2 control signals
-
- Filter flash cuts servo mode programming independent from data mode
- Analog servo field AGC loop independent from read channel gain control
- Servo demodulation from via "weighted sum" averaging peak detection
- Pulse position detector for reading grey code and sector sync mark
-
- Programmable prescaler, feedback divider for worst case 1% resolution on time base generator
- Internal programmable loop filter saves external components and eliminates externally injected noise

① read channel
② ENDEC
③ Servo Demodulation (also reading grey code/sync mark
④ write precomp.
⑤ clock synthesizer.
⑥ adaptive equalizer (class IV partial response)
⑦ Verterbi detector.

6.1.2 Read Channel Block Diagram

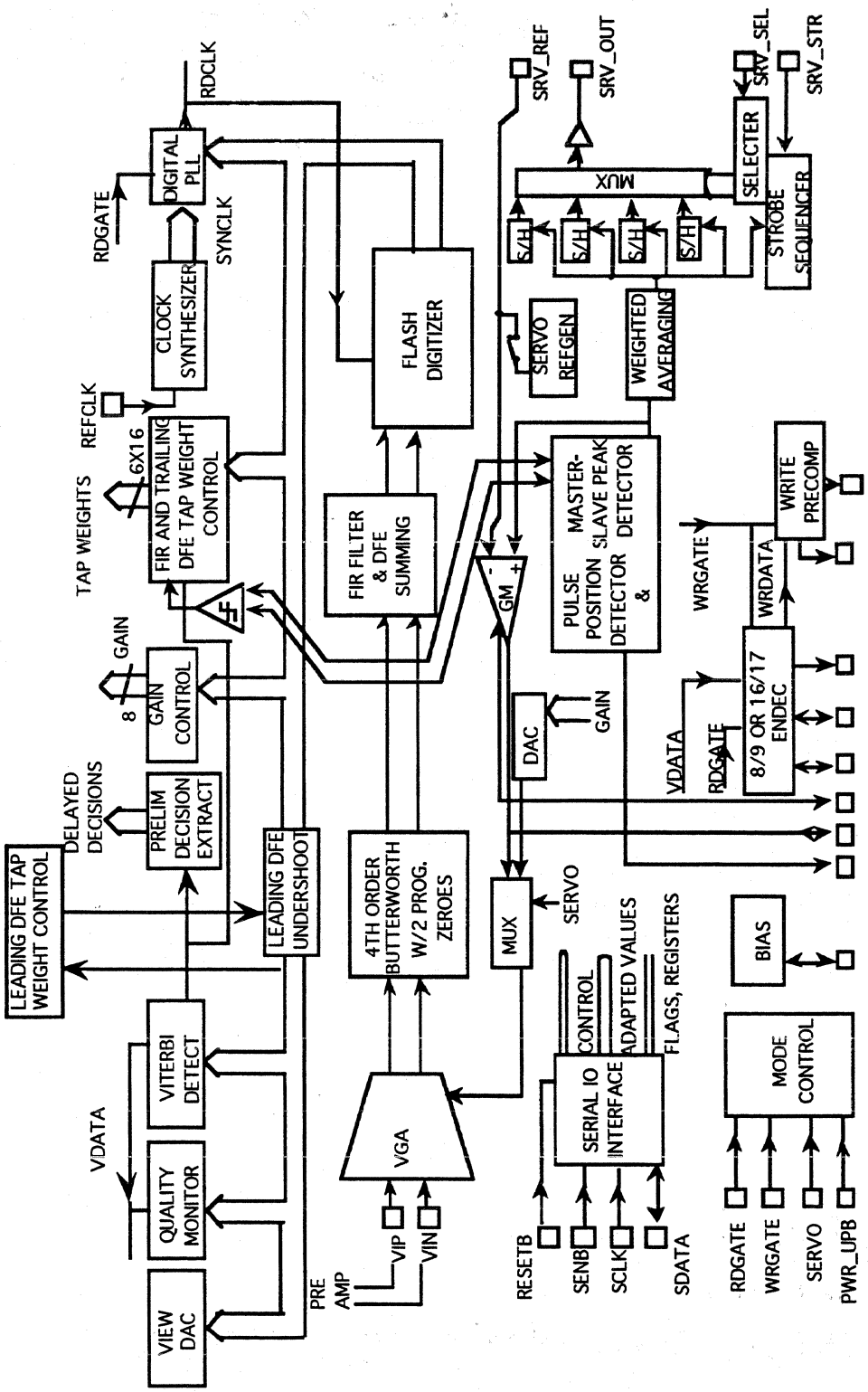

Figure 6-1 Piranha Block Diagram

6.2 Preamp

- Current Bias/Current Sense Architecture
- Designed with LinIMPACT-C™ BiCMOS Technology
- Operates From a Single +5V Supply (+10%,-10%)
- Low Power Idle Mode
- 2- and 6-Channel Capability
- Single-Ended Input to Reader With One Side Grounded
- True Differential Read Output
- Wide MR Resistor Range: Rmr = 10Ω to 40Ω
- Programmable MR Head Bias Current: Ib =10 mA to 18mA
- Gain of 241 V/V @ Rmr = 20Ω
- Bandwidth: BW = 65 MHz at -1 dB (Rmr = 20Ω)
  BW = 140 MHz at -3 dB (Rmr = 20Ω)
- Equivalent Input Noise: Vn = 0.55nV/sqrt Hz @ Rmr = 20Ω
- PSRR 50 dB at 25 MHz (input referred)
- Channel Separation 70 dB at f = 25 MHz
- Buffered Head Voltage (BHV) Monitor
- PECL Inputs for WDX and WDY
- Write Data Divided-by-2 (FF) circuit available (Metal option)
- Programmable Write Head Current: Iw = 10 mA to 30 mA (base to peak)
- Output Capacitance = 8.5 pF for writer
- Fast rise/fall time 3.7 ns (Iw=25 mA(0-p), Ltf = 180 nH, Rtf = 15Ω, Llead = 50 nH)
- Multi-Channel Servo Writer: Upper or Lower Half, every two channels, or all
- Fast Recovery Times: W/R = 0.4 µs (XIBON = L)
  R/W = 50 nS
- Read Fault (RUS) and Write Fault (WUS) detection
- MR Head Short Protection available (Metal Option)
- Thermal Asperity Detection available (Metal Option)
- MR Bias on During Write Mode. Programmable On/Off.
- Input Control Lines:
  - Head Select, with internal pull-up resistors
  - R/XW with internal pull-up resistor
  - XCS with internal pull-up resistor
  - XIBON with internal pull-down resistor
- Plastic 30-pin (2-channel) and 38-pin (6-channel) TSSOP Packages
- The device is optimized for Chip-On-Arm application.

6.3 Microprocessor

6.3.1 Description

The µPD787012 and µPD78P7012 are members of the K-Series® of microcontrollers. These 32-/16-bit devices—with a minimum instruction time of 60 ns at 33 MHz—are designed for high-speed real-time process control. They feature a 32-bit CPU, an 8- or 16-bit external data bus, sixteen banks of eight 32-bit general-purpose registers, an advanced interrupt handling facility, and a powerful set of memory-mapped on-chip peripherals. A variety of 16-bit multiply-and-accumulate instructions with overflow/underflow detection and saturation provide hardware convolution capability. A hardware multiplier executes a 16-bit unsigned or signed multiplication or a 16-bit multiplication and accumulate in 180 ns at 33 MHz. On-board memory includes 1024 bytes of RAM (includes 512 bytes of general-purpose registers) and 32K bytes of mask ROM, UVEPROM or one-time programmable (OTP) ROM.

The advanced interrupt handling facility provides eight levels of programmable hardware priority control and three separate methods of servicing interrupt requests including vectoring, hardware context switch-

ing, and macro service. The macro service facility reduces the CPU overhead involved in servicing peripheral interrupts by transferring data between the memory-mapped special function registers (SFRs) and memory without the use of time consuming interrupt service routines. In addition, the macro service facility can be used to perform certain CPU functions, such as event counting, math-oriented data alterations, or data comparisons.

6.3.2 Features

- Complete single-chip microcontroller
  - 32-bit ALU
  - 16 register banks (eight 32-bit registers each)
  - 1024 bytes of RAM (includes 512 bytes of general registers)
  - 32K bytes of ROM (μPD787012) or PROM (μPD78P7012)

- Powerful instruction set
  - General-purpose register architecture
  - Fourteen data addressing modes
  - 16-bit unsigned and signed multiply
  - 16-bit unsigned and signed divide
  - 16-bit multiply and accumulate instructions
    - Overflow/underflow detection with saturation
    - 40-bit result register
  - 8-,16-, and 32-bit data transfer, shift, and rotate instructions
  - 1-, 8-,16-, and 32-bit logic instructions
  - String instructions
  - MINMAX instruction for fuzzy logic interface

- Minimum instruction execution: 60 ns at 33 MHz
- 16-bit hardware multiplier (180 ns at 33 MHz)
- Memory space
  - 16M byte linear address space
  - Relocatable internal RAM/SFR space

- Software configurable external memory interface
  - Up to four independent memory blocks
  - 8- or 16-bit external data bus
  - Up to seven data and one address wait states
  - External wait input

- Large I/O capacity
  - Up to 60 I/O port lines
    - One input port
    - 59 I/O ports

- Memory-mapped, on-chip peripherals (special function registers)
- Real-time pulse unit (RPU)
  - 16-bit timer/event counter 1
    - Four 16-bit capture/compare registers
    - Four external interrupt capture lines
    - One external event counter input
    - Two timer outputs
  - 16-bit interval timer 4
    - One 16-bit compare register

- Asynchronous serial interface (UART)
  - Dedicated baud rate generator

- Interrupts
  - Three nonmaskable interrupts
  - Twelve maskable interrupt requests
    - Three external interrupts
    - Five internal interrupts
    - Four software selectable as external or internal
  - Three software interrupts
  - Three exception traps

- Programmable priority interrupt controller (eight levels)
- Three methods of interrupt service
  - Vectored interrupts
  - Context switching with hardware register bank switch
  - Macro service mode with choice of six different functions

- Watchdog timer with dedicated output
- STOP, HALT, and IDLE standby functions
- Single 5-volt power supply

6.3.3 Overall K7 Address Map

K7 ADDRESS	USAGE	DRAM ADDRESS[1]
FFFFFF - FFF000	4K SFR	FFFB00 - FFFCFF Resides here CPU Internal
FFEFFF - FFE000	4K Internal RAM space(1K used now) Variables & Tables	
FFDFFF - FF8400	23K DRAM Tables & variables	7DFFF-78400[2]
FF83FF - FF8000	1K ASIC registers(16 bit only)	FF8000 - FF81FFExpandable with ASIC Change
FF7FFF - FF0000	32K DRAM Variables[3]	77FFF-70000
FEFFFF - FE0000	1K ASIC registers(8 bit only)	FEFB00 - FEFCFF
FDFFFF - FD0000	64K External SRAM or EPROM[4]	
FCFFFF - FC0000	64K External SRAM or EPROM[4]	
FBFFFF - FB0000	64K External SRAM or EPROM[4]	
FAFFFF - FA0000	64K External SRAM or EPROM[4]	
F9FFFF - F90000	64K External SRAM or EPROM[4]	
F8FFFF - F80000	64K External SRAM or EPROM[4]	
F7FFFF - F00000	512K Mirror of F80000- FFFFFF[3]	
EFFFFF - 800000	7168K Mirror of F00000- FFFFFF[3]	
7FFFF - 200000	6144K Mirror of 000000- 1FFFFF[3]	
1FFFFF - 180000	512K Mirror of 100000- 17FFFF[3]	
17FFFF - 170000	64K DRAM Tables & Variables	7FFFF - 70000
16FFFF - 160000	64K DRAM code	6FFFF - 60000
15FFFF - 150000	64K DRAM Buffer	5FFFF - 50000
14FFFF - 140000	64K DRAM Buffer	4FFFF - 40000
13FFFF - 130000	64K DRAM Buffer	3FFFF - 30000
12FFFF - 120000	64K DRAM Buffer	2FFFF - 20000
11FFFF - 110000	64K DRAM Buffer	1FFFF - 10000
10FFFF - 100000	64K DRAM Buffer	0FFFF - 00000
0FFFFF - 010000	960K Mirror of 000000-0FFFFF[3]	
00FFFF - 0080000 07FFF - 000000	32K Unused 32K Internal Rom Space	

1. Four high-order address bits required:
   Bit 23 = 1 => stack and ASIC
   Bit 23 = 0 => DRAM
   Bits[18-26] decode the eight 64K pages of DRAM
2. Allows for local jump (±32K) from Internal ROM space for Variables and Tables
3. Unused, alternate DRAM access area
4. Unused, available for external memory

Table 6-1 K7 Address Map

6.4 Controller (TI 14-108384-ØZ)/F642791APGF/HA 58NFCHJ

RAION-AµE is a CMOS VLSI component that combines a programmable RAM-based disk formatter, a high-bandwidth Buffer Controller, and the Beavis AT host interface.

RAION-AmE is divided into the following 10 main blocks.

1) • Host Interface	(AT) Beavis module
2) • Buffer Control	(BFR) module
3) • Motor/VCM Interface	(MTR) module
4) • Analog to Digital Converter	(ADC)module
5) • Servo Control	(TNA) module
6) • Serial Interface	(SER) module
7) • Microprocessor Interface	(µPI) module
8) • Sequencer Control	(SEQ) module
9) • Error Correction Control	(ECC) module
10) • Top Test	(TST) module

6.4.1 Capabilities and Features

6.4.1.1 Host Interface

1) AT Interface

- Support mode 4 PIO.
- LBA and extended CHS modes supported.
- Transfer counter on-the-fly update.
- On-chip single ended 48mA drivers.
- Auto CHS/LBA. (?)
- ✓Auto read/write multiple.
- ✓Auto multiple-write sectors and -read sectors.

1) SCSI Interface

- 6 Mbyte asynchronous data transfer
- 10 Mbyte synchronous data transfer, up to 8 byte offset
- Transfer counter on-the-fly update Driving to High instead of release high (Pull up)
- ✓On-chip single ended 48mA drivers, with active negation option available.
- Glitch filter on-RST input, optional glitch filter on-ACK input
- Initiator and target mode

5) #### 6.4.1.2 Embedded Servo

- Generates control signals for burst amplitude measurement. (A&B&CED) code .
- Detects necessary syncs (2T or 3T) in wedge area.
- Keeps wedge high in find mode until locked.
- Reads track number in wedge area. (read Grey code)
- Supports Thermal Asperity logic (to be used in Sirocco at P2)

2) #### 6.4.1.3 DRAM Buffer Interface

- Supports 64K x 16 or 256K x 16 DRAM, no parity.
- ✓Bufferware, µP firmware executes from the DRAM buffer memory.
- CPU direct access, µP accesses directly from the DRAM buffer memory.
- Wait state control.
- 33.3 Mbyte/sec maximum buffer bandwidth. 33.3 Mbyte (BW.)

6.4.1.4 Control Disk Read/Write

- Generates Read gate, Write gate, etc. for R/W components.
- 2-bit wide decoded data "Shiva" or "Piranha" type interface.
- RAM-based control store (30 bits x 36 words).
  - Handles split data fields for constant rate servo wedges in multiple zone drives.
  - No microprocessor intervention needed for up to full track read/writes.
  - Format information (where variable breaks for sector are) contained in the headers.
- ID after wedge.

6.4.1.5 Microprocessor Functions

- Supports K7 and 352/40 MHz NEC Microprocessors.
- Single Crystal architecture use for both system and Microprocessor clocks.
- Memory mapping allows access to full DRAM.
- Demuxes MAD bus.
- Generates different clock rates to the microprocessor, allows clocks to be slowed or stopped for power conserving modes.

6.4.1.6 Serial Interface Functions

- Serial interface with Read & Write mode to R/W and Spindle & VCM drivers.
- Allows 10, 20, and 40-MHz operating modes for R/W channel and 10-MHz for Spindle and VCM drivers.

6.4.1.7 Analog to Digital & Digital to Analog Converter Functions for (Read channel.)

- Successive approximation type 8-bit A/D Converter, 3.3 µsec conversion time, linearity +1/2 LSB, with power down mode.
- Supports new Read channel "Shiva" or "Piranha" interface.

6.5 DRAM

A 1Mbit 80 nS Fast Page Mode DRAM in a 64 K x 16 organization with upper and lower write enable packaged in a 40 pin SOJ.

The address map is in the RAION specification.

6.6 EEPROM (SCSI Only)

Regs bits
64 x 16 = 1024 bits total

The EEPROM table information is only available for SCSI product. It is a 1K bit Serial EEPROM memory device organized in 64 registers of 16 bits. The firmware is written to support multiple vendors. The device is designed to endure 10,000 erase/write cycles and has data retention of 10 years.

The EEPROM table can be accessed through READ/WRITE BUFFER command with Vendor Unique bit set and SUPER MODE must be enabled, and transfer length of 128 bytes. The table is also be accessed through READ/WRITE CONFIGURATION page 0, page 5, page 22 (EEPROM Configuration Page), and as well as Mode Select pages. During the power on process, the EEPROM will be validated, drive serial number verified and an update the EEPROM will take place if necessary.

can be access through 'Rd/Wr Config pages 0/5/22.

Byte	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	SCSI Inquiry Information (LSB)															
.	SCSI Inquiry Information															
.	SCSI Inquiry Information															
46	SCSI Inquiry Information (MSB)															
48	WS	DPC	SS STR	DLY WS	PO EP	PO SS	PO DIS	PO FLT	ACK	Reserved for Future Use						
50	Active Pull Up Control								QCP Configuration Byte 0							
	REQ SLEW		DATA SLEW		DAT/ REQ PULLUP		UNUSED (0)									
52	QCP Configuration Byte 1								QCP Configuration Byte 2							
54	SCSIADR			SS	Reserved = 0				Drive Type							
56	Customer ID #								Motor Delay Value (1 unit = 10 ms)							
58	Reserved = 0															
.	Reserved = 0															
.	Reserved = 0															
123	Reserved = 0															
134-127	EEPROM Signature Bytes															

Table 6-2 EEPROM Generic Format Layout

128 bytes = 64 words

Byte	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	SCSI Inquiry Information (LSB)															
.	SCSI Inquiry Information															
.	SCSI Inquiry Information															
26	SCSI Inquiry Information (MSB)															
28	Reserved = 0								DEF - EXTENTS							
30	SCSI Group 0 (LSB) 00h								D9h							
32	B0h								27h							
34	SCSI Group 0 (MSB) 34h								SCSI Group 1(LSB) 01h							
36	04h								B3h							
38	01h								SCSI Group 1(MSB) 1Bh							
40	SCSI Group 7(LSB) 07h								00h							
42	A0h								00h							
44	SCSI Group 7(MSB) 00h								Terminator FFh							
46	Reserved = 0															

Table 6-3 EEPROM Apple Format Layout

Byte	Bit	Descriptions
0 - 7		Vendor Identification' Quantum'
8 - 23		Vendor identification (model) /(PART NUMBER)
24 - 27		ROM revision level 'vcod' match required to validate EEPROM data
28 - 35		ROM date.
28 - 35		generic = ROM date = 'mm/dd/yy'
28 - 34		apple = 0, 0, 0, d9h, b0h, 27h, 34h (SCSI group 0)
		DRIVE SERIAL NUMBER
36 - 47		GENERIC = Drive Serial # (12 digits)
35 - 39		APPLE = 1, 7, B3H, 1, 1BH (SCSI Group 1)
40 - 44		APPLE = 7, 0, A0H, 0, 0 (SCSI Group 2)
45 - 47		APPLE = 0, 0, 0 Reserved = 0
48		SOFT JUMPERS CONTROL WORD
	0	WS (Wait Spin) = 1 then Wait Spins enabled.
	1	DPC (Disable Parity Check) = 1 then parity checking disabled
	2	SS (Self Seek) = 1 the Self Seek enabled.
	3	DLY STR (Delay Start) = 1 then Motor turn on delay by MDV.
	4	=0, No longer used. Reserved for backward compatibility.
	5	=0, No longer used. Reserved for backward compatibility.
	6	=0, No longer used. Reserved for backward compatibility.
	7	=0, No longer used. Reserved for backward compatibility.
49	8	ACK FLT (ACK FILTER ENABLE) =1, Enable SCSI -3 glitch filter, do not enable >10 Mbyte/Sec data rate.
	9 - 15	Reserved for future use.
50		ACTIVE PULL UP CONTROL (LEO register 2EH).
	0-1	REQ SLEW = 0 0, No longer used. Reserved for backward compatibility.
	2-3	DATA SLEW = 0 0, No longer used. Reserved for backward compatibility.
	4	DATA APU = 1 then active negation is enabled on the data bus.

Byte	Bit	Descriptions
	5	REQ APU = 1 then active negation is enabled on the REQ.
	6-7	Unused = 0.
51		QCP INFORMATION BYTE 0.
	8	QCP = 0 then drive is configured for OEM/DISTI product.
		QCP = 1 then drive is configured for QCP product and it will not initialize the SCSI interface. (so the drive will not respond to any SCSI commands).
	9 - 15	Reserved for QCP future use.
52		QCP INFORMATIONS BYTE 2.
	0 -7	Backup copy of byte 0.
53		QCP INFORMATION BYTE 3.
	8 - 15	Backup copy of byte 0.
54		SOFT SCSI ID.
	0 - 2	SCSIADR (SCSI Address) = 0 7, drive LUN # if SSID bit set.
	3	SSID (Soft Selectable ID) = 0 then read PCB jumpers for SCSI ID #.
		SSID (Soft Selectable ID) 1 The SCSIADR bits (2-0) determines the drive's SCSI ID and PCB address jumpers will be ignored.
	4 - 7	Reserved = 0.
55		DRIVE TYPE.
	8 - 15	Number of heads per cylinder.
56		CUSTOMER ID #.
	0 - 2	0 = GENERIC..
		1 = APPLE.
		2 = SUN.
		3 = Nixdorf.
		4 = MEI (panasonic).
		5 = HP.
		6 = DEC.
		7 = COMPAQ.
	3 - 7	Reserved.
57	8-15	MDV, Motor Delay Value, Motor turn on delay in units of 10 mS used when DLY STR is enabled.
58		INHIBIT SCAM.
59		CHECK SUM.
60- 127		RESERVED BYTES.

Table 6-4 EEPROM Descriptions of Format

6.7 Motor/VCM (Phillips TDA5147 (Rev 7G))

M IGHTY (TDA5147) is a fully analog combination chip that includes the VCM driver, the spindle motor driver, the VCM park circuitry and the power on reset circuitry.

Overview:

Spindle Motor Driver

- Internal 1.0 Amp peak current power drivers.
- Low Rds (on) 1.0 Ω total for high, low, and isolation drivers.
- Induction sense start up option.
- External current sense resistor.
- Slew rate control of upper and soft switching lower drivers.
- Programmable linear or PWM spindle mode
- Provide spindle active dynamic braking mode.

Voice Coil Motor Driver

- 0.8 Amp VCM power driver.
- Maximum of 1 volt drop across the power driver at 0.8 amp.
- External current sense resistor, with sense amplifier.
- External current control loop compensation.
- 10 KHz minimum VCM current control loop bandwidth.
- Three mode operation: Enable VCM, Retract, and Disable.

Power Monitor And Retract Circuit

- +5 volts and +12 volts power monitor threshold accuracy +/- 2%.
- Hysteresis on both power monitor comparators.
- Precision Internal voltage generator +/- 2%.
- Buffered reference voltage out pin.
- Retract circuit works down to 2 volts.
- Internal thermal sense circuitry with an overtemperature shut down option.
- Internal boost voltage generator.
- Sleep Mode.

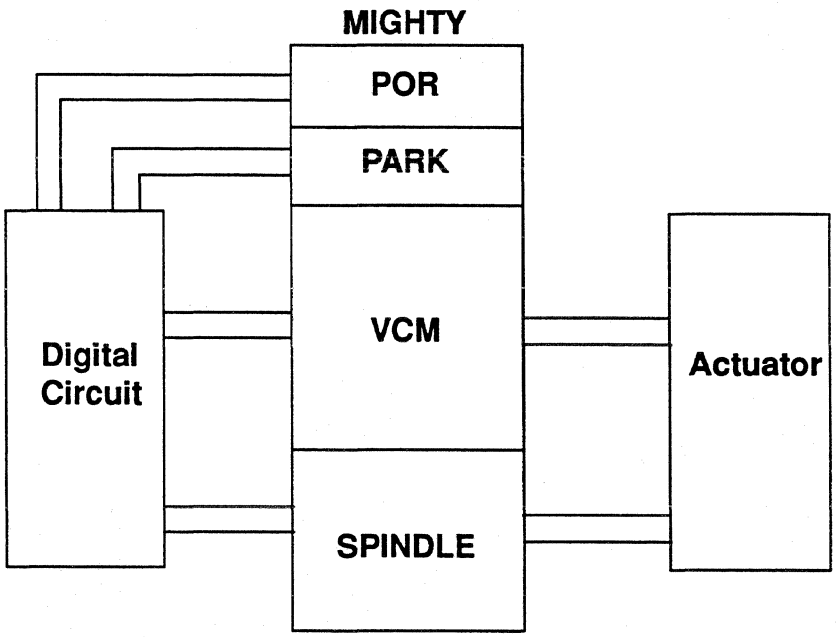

Figure 6-2 Mighty System Block Diagram

6.8 SCSI Integrated Active Terminator

The Integrated Terminator is a 18 - channel monolithic active terminator designed for single - ended SCSI bus termination.

A user- controlled STANDBY is provided to reduce standby power. If STANDBY is open or high, the terminator will be standby mode. In standby mode the terminator turns off the internal regulator and all terminative resistors.

6.8.1 Features

- Silicon monolithic bipolar IC
- 18 - channel SCSI active termination
- User - controlled terminator turning off function
- Standby function for reducing the supply current
- Low dropout internal regulator
- Thermal shutdown

6.8.2 Block Diagram

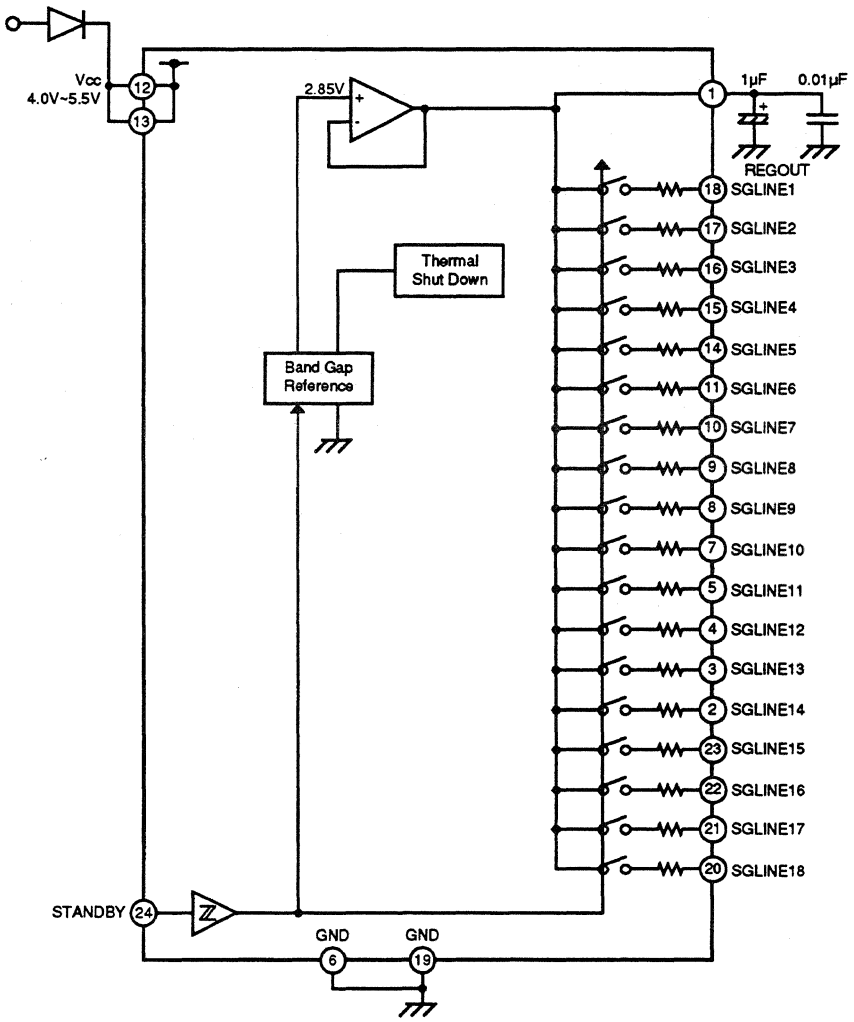

Figure 6-3 Integrated Terminator Block Diagram

6.9 PCB

6.9.1 PCB Layout Consideration

The PCB consists of four layers: a component/signal plane, a +5V power plane , a ground plane and a signal plane. The PCB has components only on one side. The four layer design provides an opportunity to:

- Separate high frequency clock signals and other high current traces from noise-sensitive low amplitude analog signals such as readback signals.
- Shield high frequency digital signals so as to reduce the energy dissipated by RFI emissions.
- Provide ample ground planes for better ESD protections.
- Use wide voltage and ground planes to prevent current loops that creates impedance difference between the power supplies and various parts of the PCB.
- Provide adequate heatsinking capability for high current lines (spindle motor and VCM).
- Provide power plane and trace keep out area's where drive mounting screw damage can occur. See Figure 6-6.
- Provide for PCB self-test of LED, jumper, and fuse functions.

6.9.2 Component Selection and Assembly Process

All land sizes were chosen for best placement registration to avoid misalignment, no contact, tombstoning resulting from unequal termination wetting and other SMD parts related solder problems. The fudicial marks at PCB corners help the high resolution vision feedback IC placement machine, especially necessary for fine-pitched QFP placements.

PCB components selection was limited, besides performance, price and availability considerations, by package to fit the form factor, automatic placement, solder and other assembly equipment restrictions, ease of testing requirements, etc. The height requirement for the top side is 4.57 mm max, and for the bottom side 0.4 mm max. In order to meet these requirements, all components are mounted only on the top side while traces run on both sides. The current MKE PCB assembly process is illustrated in the next page.

6.9.3 PCB Assembly Process

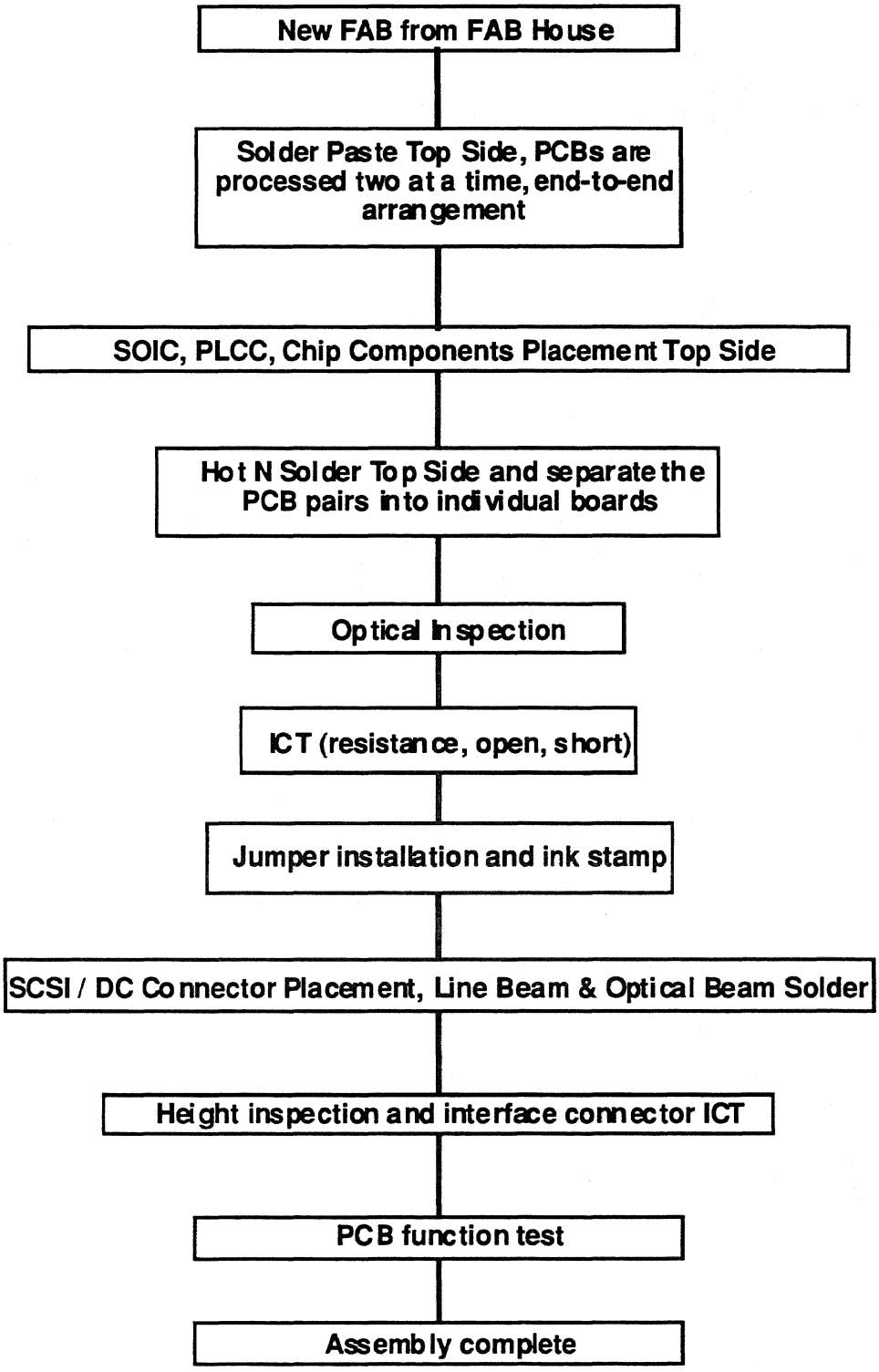

Figure 6-4 PCB Assembly Process

6.9.4 Connectors

In the current version of the Sirocco design, the following connectors are used:

Connector	Type	Part Number
J1	SCSI/DC COMB 2/1 CONN.	QNTM # 22-103860-02
	AT/DC COMB 3/1 CONN.	QNTM # 22-103854-02
J2	LED CONN. (SCSI ONLY)	QNTM # 22-102264-01
J3	R/W FLEX CONN. (20-pin)	QNTM # 22-108145-01
J4	MOTOR CONN.	QNTM # 22-107249-02
J5	ID CONN. (SCSI ONLY)	QNTM # 22-103422-01
JP1	ID JUMPER	
	SCSI	QNTM # 22-107097-01
	AT	QNTM # 22-108544-01

6.9.5 AT and SCSI PCB Block Diagram

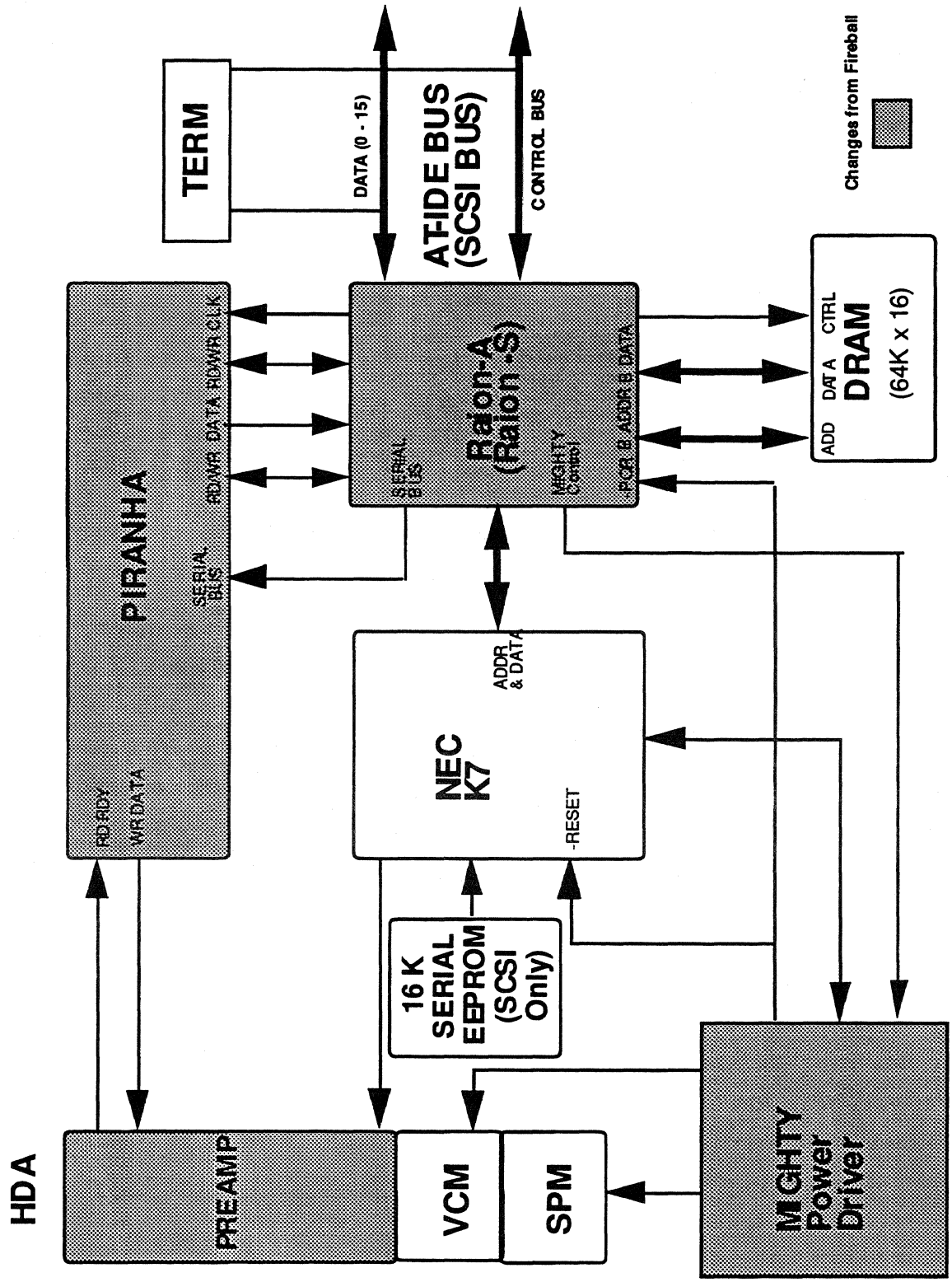

Figure 6-5 AT and SCSI PCB Block Diagram

6.9.6 PCB Non-Component Area

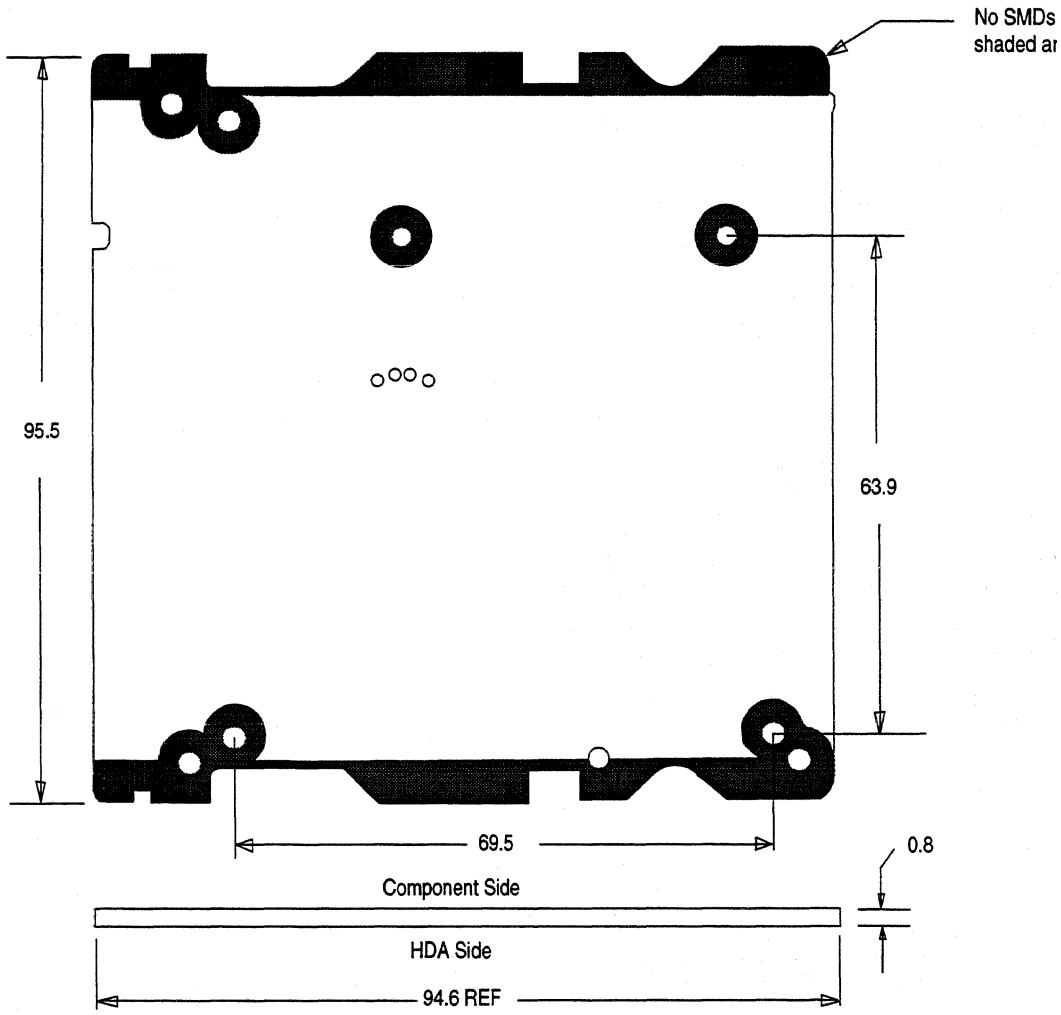

Figure 6-6 PCB Non-Component Area

Section 7 Firmware Organization

7.1 Firmware Feature

The following features are based on Fireball:

SCSI

- Support SCSI-3 Power Management modes and
- SCSI-3 mode pages.
- Error Logging/Failure Prediction
- SCAM

AT

- Support LEO Auto Features
- Auto Read/Auto Write/Auto Transfer)
  - Multiple Auto Read/Write transfers
  - CHS, LBA and DMA transfers
- Auto feature interfacing with Cache
- Error Logging/Failure Prediction
- Local Bus IDE/Fast DMA/Fast ATA and DMA (16 Mb/s)

7.2 New Firmware Features for Sirocco

Sirocco firmware will be developed from the FireBall base, where appropriate firmware features will be leveraged from other programs such as Maverick. Because of the overlapping development schedules periodic updates from the FireBall code base will be performed during the firmware development. The following new firmware features will be developed for Sirocco.

- Multiple Spares/Cylinder
- Servo Defect Mapping
- ATA compliant Master/Slave Implementation
- Cache Performance Optimization
- Power Savings Optimization
- Quantum Diskware Download
- Quantum DPA
- Quantum Power Management
- SelfScan Universal Process Test 2

7.2.1 Multiple Spares/Cylinder

The defect management scheme used in Maverick allowed only one sector per platter to be inline spared. (i.e. 2 in-line spares allowed on a 2-disk HDA.) With the increasing numbers of disks used in 3.5" products, the introduction of servo defect mapping, and the use of ID after wedge disk format this is often not sufficient to allow all factory defects to be inline spared. As a result some defects may have to be offline spared resulting in a lower performance and a wider distribution of throughput between drives. While it is possible to allow more than one sector per cylinder with the original scheme to do so increases number of sectors per cylinder that need to be reserved for defect management and thus lowers the capacity of the drive.

7.2.2 Servo Defect Mapping

The design of prior 3.5" products required the servo wedge data to be defect free in the area of the servo bursts. This requirement resulted in a yield loss in SelfScan where a drive can fail servo verify because of a single servo defect. A Servo Defect Mapping scheme has been proposed for Sirocco that would allow servo defects to be mapped out. The servo code will be modified to allow it to coast through known bad wedges without creating error status. The data sectors affected by the servo defects will be mapped out by the reg-

ular defect management and will not be written or read during normal operation. More details of this scheme can be found in the Sirocco Firmware Manual.

7.2.3 ATA compliant Master/Slave Implementation

7.2.4 Cache Performance Optimization

7.2.5 Power Savings Optimization

7.2.6 Quantum Diskware Download

7.2.7 Quantum DPA

7.2.8 Quantum Power Management

7.2.9 SelfScan Universal Process Test 2

7.3 Caching

Sirocco incorporates DisCache, a 76K cache, to enhance drive performance. This integrated feature is user-programmable, using the MODE SELECT command, and can significantly improve system throughput.

7.3.1 Read Cache

DisCache anticipates host-system requests for data and stores that data for faster access. When the host requests a particular segment of data, the caching feature uses a prefetch strategy to "look-ahead" and automatically store the subsequent data from the disk into high-speed RAM (Random Access Memory). If the host requests this subsequent data, the RAM is accessed rather than the disk.

Since typically 50 percent or more of all disk requests are sequential, there is a high probability that subsequent data requested will be in the cache. This cached data can be retrieved in microseconds rather than milliseconds. As a result, DisCache can provide substantial time savings during half or more of all disk requests. In these instances, DisCache may save most of the disk transaction time by eliminating the seek and rotational latency delays that dominate the typical disk transaction. For example, in a 1K-byte data transfer, these delays comprise 90 percent of the elapsed time.

DisCache works by continuing to fill its cache memory with adjacent data after transferring data requested by the host. Unlike a non-caching controller, Quantum's disk controller continues a read operation after the requested data has been transferred to the host system. This read operation terminates after a programmed amount of subsequent data has been read into the cache segment.

The cache memory is a 76K DRAM buffer allocated to hold the data which can be directly accessed by the host via the READ and WRITE commands. The memory functions as a group of segments (ring buffers) with rollover points at the end of each segment (buffer). The unit of data stored is the logical block (i.e., a multiple of the 512 byte sector). Therefore, all accesses to the cache memory must be in multiples of the sector size. In those cases where the cache memory must be used for scratch memory, as in the case of a FORMAT UNIT command, or where the size of the logical block may change, as in the MODE SELECT command, the cache will be emptied. The commands that will force emptying of the cache are:

SCSI:

- FORMAT UNIT
- INQUIRY
- READ DEFECT DATA
- READ LONG
- READ CAPACITY
- WRITE LONG

- MODE SELECT
- MODE SENSE
- REASSIGN BLOCKS
- VERIFY

AT:

- WRITE BUFFER
- SET FEATURES
- DRIVE FAILURE PREDICTION
- WRITE CONFIGURATION
- DOWNLOAD
- BUFFER RAM TEST

7.3.2 Write Cache

When a write command is executed with write caching enabled, the drive stores the data to be written in a DRAM cache buffer and immediately sends a COMMAND COMPLETE message to the host before the data is actually written on the disk. The host is then free to move on to the other tasks, such as preparing data for the next data transfer, without having to wait for the drive to seek to the appropriate track or rotate to the specified sector.

While the host is preparing data for the next transfer, the drive immediately writes the cached data to the disk, usually completing the operation after issuing COMMAND COMPLETE.

WriteCache allows data to be transferred in a continuous flow to the drive rather than as individual blocks of data separated by disk access delays. This is achieved by taking advantage of the ability to write blocks of data sequentially on a disk that is formatted with a 1: 1 interleave. This means that as the last byte of data is transferred out of the write cache, and the head passes over the next sector of the disk, the first byte of the next block of data is ready to be transferred; thus there is no interruption or delay in the data transfer process.

The WriteCache algorithm writes data to the cache buffer while simultaneously transferring data to the disk that was previously written to the cache.

7.3.3 Performance Benefits

In a drive without DisCache, during sequential reads, there would be a delay due to rotational latency even if the disk actuator were already positioned at the desired cylinder. DisCache eliminates this rotational latency time -- 6.67 milliseconds on average -- when requested data resides in the cache.

Moreover, the drive often must service requests from multiple processes in a multitasking or multiuser environment. In these instances, while each process may request data sequentially, the disk drive must share time among all these processes. In most disk drives, the heads must move from one location to another. With DisCache, even if another process interrupts, the drive continues to access the data sequentially from its high-speed memory. In handling multiple processes, DisCache achieves it most impressive performance gains, saving both seek and latency time when desired data resides in the cache.

7.3.4 Flexibility, Ease Of Use, Speed

DisCache was originally designed to be flexible because cache performance is highly application-dependent. Several parameters are automatically adjusted by the drive, this allows the drive to continuously optimize its performance. The remaining options which are still programmable enable users to adjust caching parameters to optimize performance. These options can be specified and subsequently modified using the SCSI MODE SELECT OR AT SET CONGIGURATION command. Table 7-1 outlines both the pro-

grammable and the fixed parameters; the discussion following the table explains the parameters and how they can be used.

Parameter	DisCache Function Range	Input Value	Default
Read Cache disable	Activates read cache when cleared (bit=0)	0,1	0
Write Cache enable	Activates write cache when set (bit=1)	0,1	1
No. of Cache Segments	Sets number of cache segments to be maintained	not changeable	dynamic (0 - 28)
Maximum Prefetch			dynamic
Minimum Prefetch			dynamic
Disable Prefetch Transfer Length	Enable/Disable = 0 prefetch	0-FFFF	FFFF

Table 7-1 DisCache Parameters

Through the use of these programmable parameters, the caching feature can be tailored to optimize individual system performance. The programmable parameters shown in Table 7-1 can be found on MODE SELECT Page 38H. When the Read Cache Disable bit is set to one, caching is disabled. Disabling the cache reduces command overhead. When disabling the cache, you essentially disable the prefetching and housekeeping required to manage the cache. The default value of this bit is zero (Cache enabled).

The Read cache is divided into segments. Each segment contains one cache entry. A cache entry consists of the requested READ data plus its corresponding prefetch data.

The requested READ data takes up a certain amount of space in the cache segment so the corresponding prefetch data could essentially occupy the rest of the space within the segment.

7.4 Error Correcting Code

7.4.1 ECC Features

- 8 bits per symbol.
- 3 interleaves.
- 6 redundancy bytes per interleave.
- 2 cross-check bytes.
- 18 ECC bytes and 2 cross-check bytes: total of 20 redundancy bytes.
- ECC hardware includes Reed-Solomon encoder/decoder circuit that is used to generate redundancies during write mode and syndromes during read mode. The hardware also checks the values of the syndromes to detect error. All corrections will be done in firmware.
- Single-Error Correction:
  - Correct up to 24 bits (i.e. 1 byte per interleave).
  - Guarantee to correct 17 bits.
- Double-Error Correction:
  - Correct up to 48 bits (i.e. 2 bytes per interleave).
  - Guarantee to correct 41 bits.
- Triple-Error Correction:
  - Correct up to 72 bits (i.e. 3 bytes per interleave).
  - Guarantee to correct 65 bits.
- Random Multiple-burst error case: correct up to 9 bytes.
- Scan-path is available for testability.
- ECC syndromes and cross-checks can be observed by selecting the ECC registers from E0h to F3h.

7.4.2 7.3.2 ECC Equations

7.4.2.1 Galois Field

The Galois field for the ECC and cross-check polynomials is generated using the extension field theory and is described as follows:

- Sub Field $GF(2^4)$:

  Let elements of the sub field be represented by powers of beta. The sub field is defined by the following polynomial:

  $P_{sub}(X) = X^4 + X + 1$

  with $beta^1$ = (02)h as the first element of $GF(2^4)$ over GF(2).

- Extension Field $GF(2^8)$:

  Let elements of the extension field be represented by powers of alpha. The extension field is defined by the following polynomial:

  $P(Z) = Z^2 + Z + f_0$

  where

  f_0 = (08)h as a constant and

  $alpha^1$ = (12)h as the first element of $GF(2^8)$ over GF(2).

7.4.2.2 ECC Polynomial

The ECC polynomial is defined as follows:

$$ECC(X) = X^6 + alpha^{169} * X^5 + alpha^{179} * X^4 + alpha^{25} * X^3 + alpha^{184} * X^2 + alpha^{179} * X + alpha^{15}$$

$$= (X + 1) * (X + alpha^1) * (X + alpha^2) * (X + alpha^3) * (X + alpha^4) * (X + alpha^5)$$

7.4.2.3 Cross - Check Polynomial

The Cross - Check Polynomial is defined as follows:

$$XC(X) = X^2 + alpha^{143} * X + 1$$

$$= (X + alpha^{127}) * (X + alpha^{128})$$

7.5 Description of CRC

7.5.1 CRC for ID Field

The ID data is protected by 3-byte Reed-Solomon CRC. The values of CRC bytes can be observed by selecting the following registers: (F4)h for CRC0, (F5)h for CRC1, and (F6)h for CRC2.

7.5.2 CRC Equations

7.5.2.1 Galois Field

The Galois field for the CRC polynomial is the same as the ECC and the cross-check polynomials.

7.5.2.2 CRC Polynomial

The CRC polynomial is defined as follows:

$$CRC(X) = X^3 + alpha^{203} * X^2 + alpha^{203} * X + 1$$

$$= (X + alpha^{-1}) * (X + alpha^0) * (X + alpha^1)$$

7.6 Probabilities

7.6.1 Probability Model

Assumption 1: every symbol has equal error probability and error pattern is occurred completely random.

Assumption 2: each error burst is associated with a single byte.

Probability numbers are defined as follows:

- Ps : raw error rate (events/bit). This number is obtained before ECC system.
- Ph : probability of hard error (events/bit) obtained after on-the-fly ECC.

- Pue : probability of uncorrectable errors (events/bit) when the number of symbol errors exceeds the correction capability of the code.
- Pmc: probability of miscorrection. This is a conditional probability that depends on the number of errors occurring.
- Pxc : misdetection probability of the cross-checks.
- Pe : probability of decoding error when the ECC incorrectly decodes and sends erroneous data to customer.

7.6.1.1 Probability of Uncorrectable Errors:

Probability of uncorrectable errors (events/bit) when the number of symbol errors exceed the correction capability of the code.

$$Pu = \frac{1}{n \times m} \sum_{i>t}^{n} \binom{n}{i} (P_s \times m)^i \times (1 - P_s \times m)^{n-i}$$

where

n : number of symbols per interleave including redundancy symbols.

m: symbol width in bits.

t : correction capability in symbols.

Ps*m : raw symbol error rate (events/symbol).

7.6.1.2 Probability of Miscorrection

The Reed-Solomon ECC is characterized as a maximum distance separable (MDS) code in which d = n - k + 1. We are using an incomplete decoder for a t-error-correcting code that t is equal to (n - k)/2. This means that the ECC only corrects all errors with t symbols or less and does not attempt to correct more than t error symbols. When an error burst of a received word is less than or equal to t symbols, the code corrects without any miscorrection errors. This means that Pmc is equal to zero. If there is error greater than t symbols, the code either sends an uncorrectable message or decodes the error patterns and error locations incorrectly. The value of Pmc then can be estimated as follows:

$$Pmc = q^{-r} * V(t) \qquad (2)$$

where

$q = 2^m = 2^8 = 256.$

r = n - k –> (code's redundancy).

$$V(t) = \sum_{t=0}^{t} \binom{n}{s} \times (q-1)^s$$ (volume of a Hamming sphere of radius t)

Therefore,

for $e \leq t$, $Pmc = 0$ (3a)

$$\text{For } e > t, \qquad Pmc = \frac{\sum_{t=0}^{t} \binom{n}{s} \times (q-1)^{s}}{q^{r}} \qquad (3b)$$

(where e: number of symbol errors).

7.6.1.3 Probability of Misdetection of Cross-Checks

The probability of misdetection of the cross-checks can be estimated as follows:

$$Pxc = \frac{1}{q^{rxc}} \qquad (4)$$

where

rxc : number of cross-check symbols.

7.6.1.4 Probability of Decoding Error

This probability can be translated as the probability of transferring erroneous data to customer. Pe can be obtained by taking the product of Pu, Pmc, and Pxc :

$$P_e = P_u * P_{mc} * P_{xc} \qquad (5)$$

7.6.2 Error Probabilities

7.6.2.1 On-the-fly Correction (Single- Or Double-error Correction)

Assumption: $P_s = 10^{-7}$ (raw soft error rate).

$$Pu = \frac{1}{176 \times 8} \sum_{i=3}^{176} \binom{176}{i} \left(8 \times 10^{-7}\right)^{i} \times (1 - 10^{-7} \times 8)^{176-i}$$

$$= 3.3 * 10^{-16}$$

$$Pmc = \frac{\sum_{(s=0)}^{2} \binom{176}{s} \times (256-1)^{s}}{256^{6}}$$

$$= 3.5 * 10^{-6}$$

$$Pxc = \frac{1}{256^2}$$

$$= 1.5 * 10^{-5}$$

$$P_e = P_u * P_{mc} * P_{xc} = 1.7 * 10^{-26}$$

7.6.2.2 Off-line Correction (Triple-error Correction)

Assumption: $P_s = P_h = 10^{-10}$ —> hard error rate (i.e. hard errors beyond the correction capability of on-the-fly ECC)

$$Pu = \frac{1}{176 \times 8} \sum_{i=4}^{176} \binom{176}{i} (10^{-10} \times 8)^i \times (1 - 10^{-10} \times 8)^{176-i}$$

$$= 1.12 * 10^{-32}$$

$$Pmc = \frac{\sum_{(s=0)}^{3(2)} \binom{176}{s} \times (256-1)^s}{256^6}$$

$$= 5.0 * 10^{-2}$$

$$Pxc = \frac{1}{256^2}$$

$$= 1.5 * 10\text{-}5$$

$$P_e = P_u * P_{mc} * P_{xc} = 8.4 * 10^{-39}$$

7.6.2.3 Summary

In the off-line correction case, the probability of miscorrection (P_{mc}) is 5.0E-2 that is quite high and unacceptable. In order to improve this probability number we use two cross-checks to detect miscorrection. These two cross-checks make the effective miscorrection probability equal to 7.0E-7 (i.e. $P_{mc} * P_{xc}$ = 5E-2 * 1.5E-5 = 7.0E-7) which is better than P_{mc} by itself.

In addition to the two cross-checks, we also employ an off-line correction algorithm in firmware that rereads a number of times with on-the-fly ECC, and performs triple-error correction only when hard error is detected. These criteria improve P_s from 10^{-7} to 10^{-10} (i.e. P_h) which effectively improve the probability of transferring erroneous data to customer as depicted above. Note that we assume the worst case here with $P_h = 10^{-10}$, because the typical number should be about 10^{-14}.

7.7 Microprocessor Memory Map, Diskware and F/W Organization

The Sirocco architecture has been designed to support Diskware. Part of the Buffer memory is used to load firmware from disk and the processor is able to execute the firmware directly from the buffer memory.

The firmware is partitioned between the CPU ROM and the Diskware. The CPU ROM code contains all of the routines necessary to power up the drive and read the Diskware into the Buffer. It also contains routines that allow the Diskware to be written to the disk via the host interface. All time critical code is located in the CPU ROM because the processor is able to execute CPU ROM code much faster than Diskware code. The Diskware code contains firmware that is not required for powering up the drive. The Diskware code also contains provisions to allow for possible engineering firmware changes in the CPU ROM code to be corrected by mapping erroneous subroutines from CPU ROM into the Diskware.

The Diskware code space is partitioned into three parts, a resident part, an overlay part and an Selfscan part. The resident Diskware is loaded during the drive power up initialization and remains in memory while the drive is powered on. The overlay Diskware is loaded on as needed basis. The Selfscan Diskware is loaded on an as needed basis into memory space designated as the Cache space as an overlay during drive process test.

The Diskware is stored on reserved system cylinders in memory image format. A new configuration page 15 specifies where the overlays are stored on the system cylinders and where the overlays are loaded into the processor memory. Generally system cylinder information is stored in multiple places for redundancy, the overlay configuration page only specifies where the first copy of the Diskware is stored. Redundant copies of the Diskware are stored according to the firmware redundancy algorithm for system cylinder information. The Sirocco firmware stores redundant system cylinder information on all physical heads in system cylinder areas. See Section (TBD) for reserved system cylinder information.

Configuration Page 15 - Overlay Page

TBD

The NEC 787012 microprocessor has a 16 MB address space. On Sirocco, DRAM allocation is organized as follows:

SIROCCO MEMORY ALLOCATION

TBD

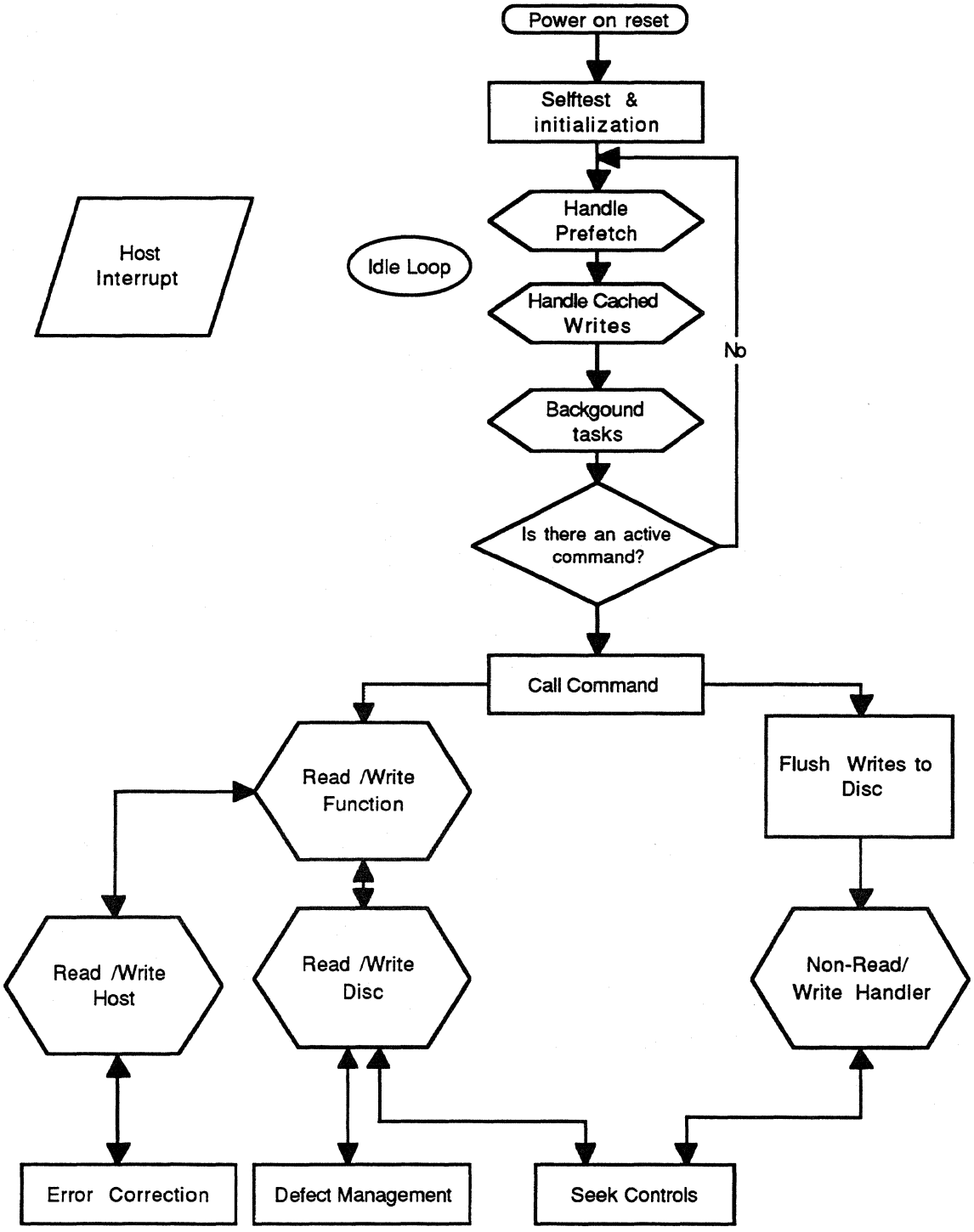

Figure 7-1 Firmware Organization

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Section 8 Servo Design

8.1 General Description

The Sirocco servo is an embedded sector servo system using MR technology to achieve high TPI. State space control technique is used for its ability to handle sensor noise and the flexibility to allow more involved algorithm, such as adaptation, should the situation require.

8.2 MR Head Considerations

The use of MR head, with advantages such as high level signal which is independent of the head/media speed, adds considerable complexity to the servo system, some of which are briefly described in this section

8.2.1 Microjog

The MR head uses separate elements for the read and write operations. As a result, the servo must "microjog" when it changes the write operation to read, or vice versa. This microjog distance is dependent on:

- Track number
- Tangential read/write element separation
- Radial offset between the magnetic centers of the read and write element. This offset is used as a head design parameter to balance the microjog distance (opposite direction) at the ID and OD, which minimizes the amount of track servoing.

8.2.2 Ontrack/Offtrack Servo

Ontrack servo is defined as the servo operation to maintain track following when servo burst A = C. Offtrack servo is the operation to maintain track following with an offset between -50% to +50% of a track. The ontrack servo uses the best linear region of the servo bursts, which results in better track following performance than offtrack servo. Therefore, the **ontrack servoing is used in the write data operations.** On the other hand, the offtrack servoing is used mainly in read operations. For a read operation on any track, the servo seeks to that track with an offset that is equal to the microjog distance associated with that track (and head). The servo settles directly to the offtrack position.

Besides read operations, offtrack servoing is also used for formatting, read/write offset measuring, and other testing and optimization during the development and manufacturing processes. The following factors can affect offtrack servoing:

1. The linear property of the servo track profile, particularly at the offtrack region where the decoding algorithm must switch between different bursts to calculate the position error signal (PES).
2. The gray code near the track boundary region may not be accurate (error = ± 1) and it also may result in a soft error. Currently, the servo code ignores these errors while offtrack is more than 25%.

The offtrack servo necessitates the addition of the 4th burst.

8.2.3 Read/Write element offset measurement

In order to calculate the amount of microjog needed at each track, the read/write element offset must be measured at the Inner Diameter (ID) and Outer Diameter (OD) tracks. This measurement requires offtrack servoing with an offtrack range more than the normal microjog distance.

8.2.4 Bias current

MR head requires bias current to "rotate" the magnetic domain to the appropriate operating point. This bias current has strong effects on the slope of the PES signal, which is calibrated by the RECAL routine at

power up time. It is essential to keep the bias current constant to avoid the need to recalibrate PES slope other than at the power up time.

8.2.5 Read width vs. write width

The MR head allows the designer to select different widths for the read and write elements. In general, a separated and narrower read element requires less stringent TMR; however, the read element cannot be too narrow, as it would decrease signal amplitude and it would create problems in the servo track profile, which would have a steeper slope and a wider saturated region. The read element width of 2/3 of the track width was selected for this reason, and it also allows the possibility of using the servo burst width equal to 2/3 of the track width, if needed, to improve the servo track profile linearity.

8.2.6 ID Field

Accessing the ID field affects the servo function in a number of ways, such as:

1. The requirement to position the head to assure the ID field reading
2. Ability to servo offtrack during formatting of the ID field

8.3 Mode of Operation

Head position is digitally controlled in a servo interrupt service routine (ISR). The microprocessor is interrupted by the TNA one time for every servo wedge. In the ISR, the servo firmware looks at the state of some flags to decide how to handle the position information available. One of three general control algorithm is used for generating current commands:

- Velocity seek
- Settle
- Track Follow

8.3.1 Seek Mode

The primary objective of Seek Mode is to move the read/write head from one concentric track radial position to another concentric track radial position under the physical constraints of the actuator acceleration factor and power consumption. In doing so, it has to accelerate the actuator as quickly as possible and then switch to controlled deceleration as soon as possible to stop just in time when it arrives at the target track position.

A long seek (seek length > 80 tracks) consists of accelerating, coasting, decelerating, linear velocity, and then settling. A medium seek (seek length between 3 and 80 tracks) starts immediately with linear velocity. A short seek (seek length < 3 tracks) also starts with linear velocity using low bandwidth coefficients.

In order to have the correct acceleration to deceleration switching and controlled deceleration operation for various seek lengths, a phase plane velocity vs. position trajectory guide is employed. Hence, both position and velocity state information of the actuator are vital.

Control strategy should avoid excessive overshoot of velocity profile trajectory when switching, and should make actuator adhere to the trajectory profile while decelerating without too much noise in the control by using feed forward. It should also provide consistent final conditions of seek mode for the next servo settle mode initial conditions.

8.3.2 Settle Mode

The Settle Mode is designed with high DC stiffness and high phase margin for good damping and fast settling for seek arrival transients. The servo switches from seek mode to settle mode when it is within position error and velocity limits. When the head is moved more than 1/4 track from the target, the servo also switches back to the linear velocity.

8.3.3 Track Follow Mode

When the servo stays within position error and velocity limits for a certain number of consecutive samples, it switches to the track following mode with write enabled. When the servo detects a bump and an error condition in the previous sample (including a bump condition), it disables write and switches to linear velocity to bring the head back to target.

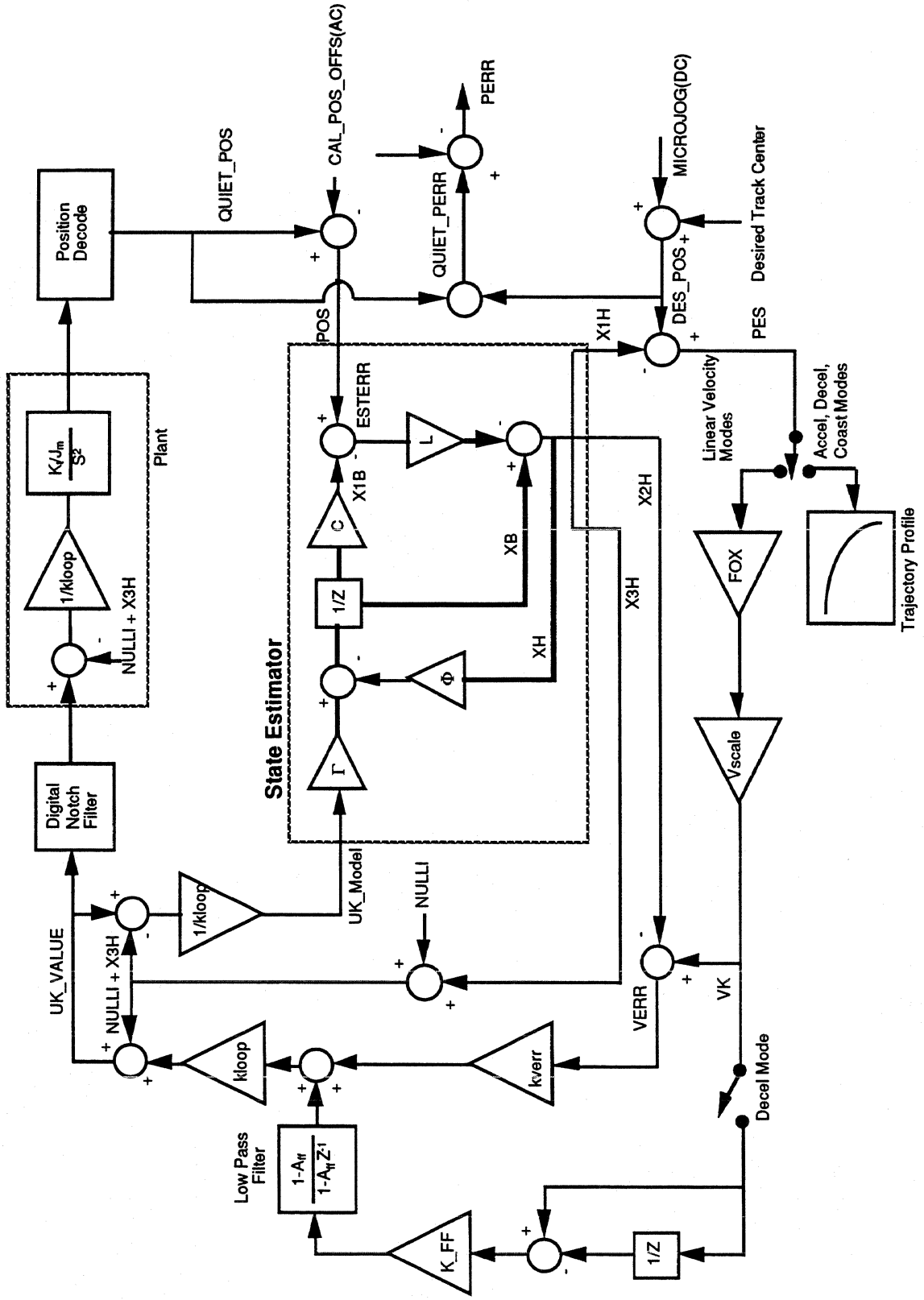

Figure 8-1 Seek Mode

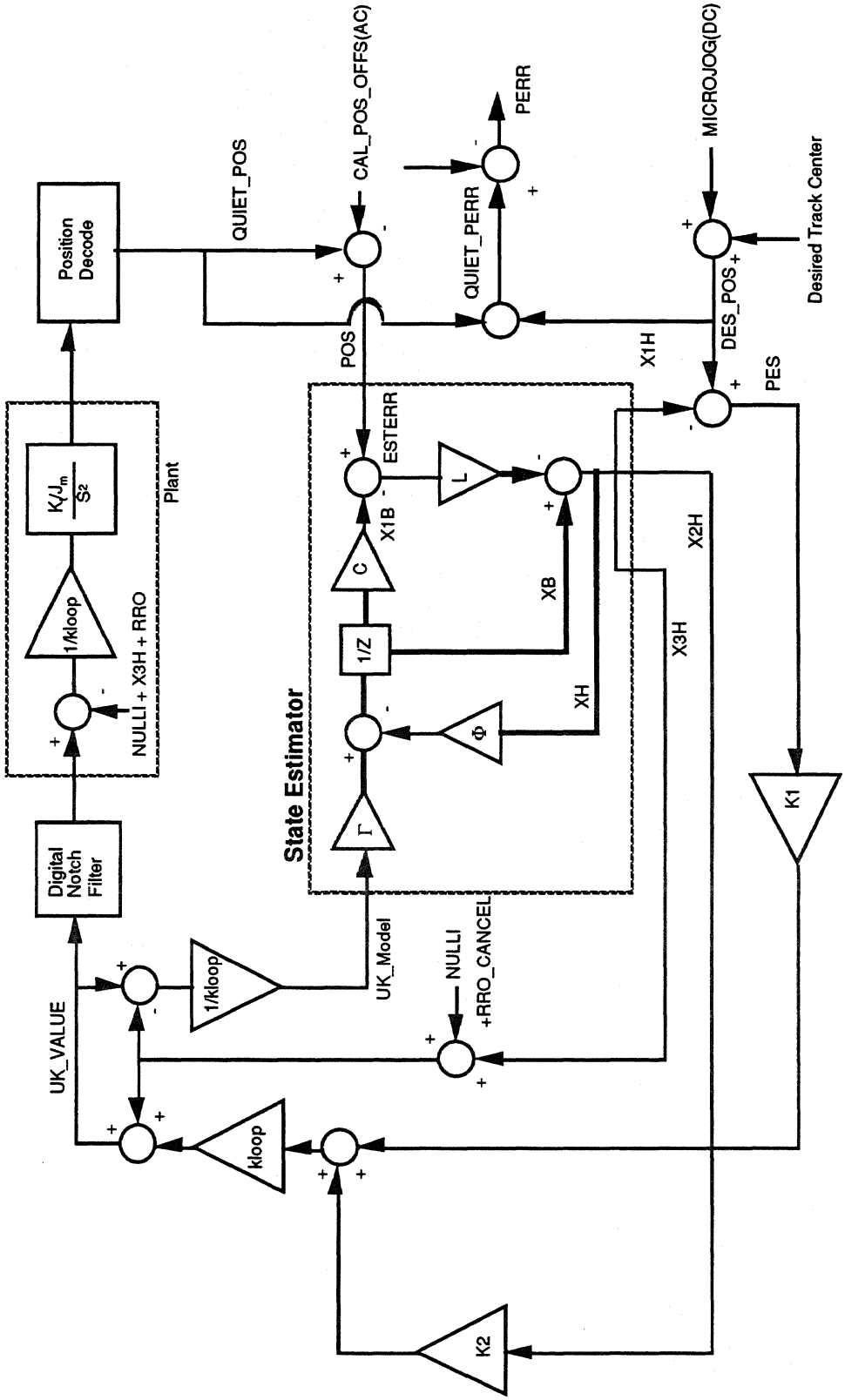

Figure 8-2 Settle/Track-Follow Mode

8.4 Servo Error Budget

Description	Dist. Type	Dist. Parameters (all units in tracks)	
Spindle NRRO	Normal	Mean = 0.00%	3 Sigma = 3.51%
Servo Dither			
Write	Normal	Mean = 0.00%	3 Sigma = 2.85%
Read	Normal	Mean = 0.00%	3 Sigma = 3.60%
Settling Transient			
Random Seek, Write	Measured	Mean = 0.00%	99.74% level = 3.50%
Random Seek, Read	Measured	Mean = 0.00%	99.74% level = 6.00%
RRO Residual			
Write Mode	Normal	Mean = 0.00%	3 Sigma = 5.63%
Read Mode	Normal	Mean = 0.00%	3 Sigma = 7.66%
Servowriter Errors (W/W Only)			
DC Component	Normal	Mean = 0.00%	3 Sigma = 0.53%
AC Component	Normal	Mean = 0.00%	3 Sigma = 3.12%
Operating Vibration (Worst Case)			
Random Seek	Measured	Mean = 0.00%	99.74% level = 5.00%
Operating Shock			
Write Bump Limits + Uncertainty	Uniform	Min = -13.50%	Max = 13.50%
Read Bump Limits + Uncertainty	Uniform	Min = -22.50%	Max = 22.50%

Table 8-1 Sirocco Error Budget

Notes to Table 8-1:

1. All distributions above were approximated from actual data or simulation studies.
2. -3 sigma to + 3 sigma contain (or hold) 99.74% of total histogram, and histogram not necessarily Gaussian distribution.

8.5 Servo System Parameters

Components or parameter	Sirocco Spec	
TPI	5850	track/inch (intended)
# of cylinders	5920	cylinder
# of sector/rev	90	sector
Spindle speed	4500	RPM
Sample period	148	µsec
Alias frequency	3375	Hz
Arm radius to head[1]	2.142	inch
Inertia[2]	43	gm-cm^2
Torque constant[3]	730	gm-cm/amp
Acceleration factor	16654	1/amp-sec^2
Coil resistance (@ 25°C)4	11.2	ohm
Max. head velocity	100	in/sec
Power amp gain[5]	2.354E^{-4}	amp/bit
Coil inductance[6]	1.96	mH
Max. voltage[7]	11.5	volt

Table 8-2 Servo Related Parameters

Notes to Table 8-2:

1. The distance from actuator pivot to read/write head gap is measured by Quality Assurance X-Y table and caliper measurement.
2. Inertia is measured by means of the Torsion pendulum method.
3. Torque factor is measured by applying a constant current to voice coil and measuring the torque on the actuator across the ID- to -OD band. The current applied are ± 100 ma, ± 200 ma, and 300ma respectively for each measurement.
4. Coil resistance is measured by means of a Digital ohmmeter.
5. Gain of DAC stage included.
6. Coil inductance is measured by means of a Digital impedance meter
7. Available @ Power amp outputs w/ nominal 12 volt supply.

8.6 Servo Wedge Format

Figure 8-3 shows the Sirocco servo wedge format. Every wedge consists of four separate fields: (1) Automatic Gain Control (AGC)/Sync field, (2) Servo Address Mark (SAM) field, (3) Track Number, and (4) Burst area. Since a Phase Lock Loop (PLL) is not used in the servo wedge area, time discrimination is used. Timing for all four fields is generated from the same crystal reference. This clock has a period of 25 nanoseconds, and will be referred to as T. Data is encoded in the following manner:

Servo Data Bit "0" = 10 000 010 0,
Servo Data Bit "1" = 10 010 000 0,

Since each digit has T width, the length of a Servo Data Bit is 9T.

1. The AGC/Sync field consists of a 3T patterns, and is used by the Read/Write channel to acquire the proper amplitude for the encoded track number and position bursts. It is also used to synchronize the raw data pulses in order to detect SAMs. The total length of the AGC/Sync field is 72T + 48T = 120T.
2. The SAM follows the sync field. It consists of a default 14T repeated twice, followed by a servo data bit 0. Following the servo data bit 0 is either a servo data bit 0 or 1, which is also known as the index bit. If a one is decoded, then an index pulse is generated. The total length of the SAM field is 37T.
3. Following the index bit is the track number. The track number is a 13-bit Gray coded number. The Gray code to binary conversion is done in the Servo Controller module of the Disk Controller and Host Interface ASIC. Each Gray code bit is encoded as servo data bits. The total length of the track number is 117T.
4. Following the track number is the burst area. There are four bursts per servo wedge time, an A burst followed by the B burst, then the C burst, and finally the D burst. When on track, the A and C burst will be equal at half amplitude, with the B burst at full amplitude for even tracks, and zero amplitude for the odd tracks.

   The A, B, C, and D bursts are each 48T long. There is a DC erase area of 9T before and post burst gap of 33T after, giving a total time of 234T for the burst area.

The Servo Controller module reports status to the microcontroller when it detects errors in the servo wedge. The errors include missing Syncs, missing SAMs, error reading Gray code, and Speed error (i.e., SAMs detected outside the ±0.25% speed tolerance window). When a missing Sync or SAM condition is encountered, the Servo Controller module sets its timer to a known value. This is to compensate for the elapsed time lost while looking for SAMs. This way, the servo burst can continue to be sampled, and the servo wedge will still terminate correctly. The servo firmware, however, will be aware of this condition and acts accordingly depending on the error type and any error from previous samples.

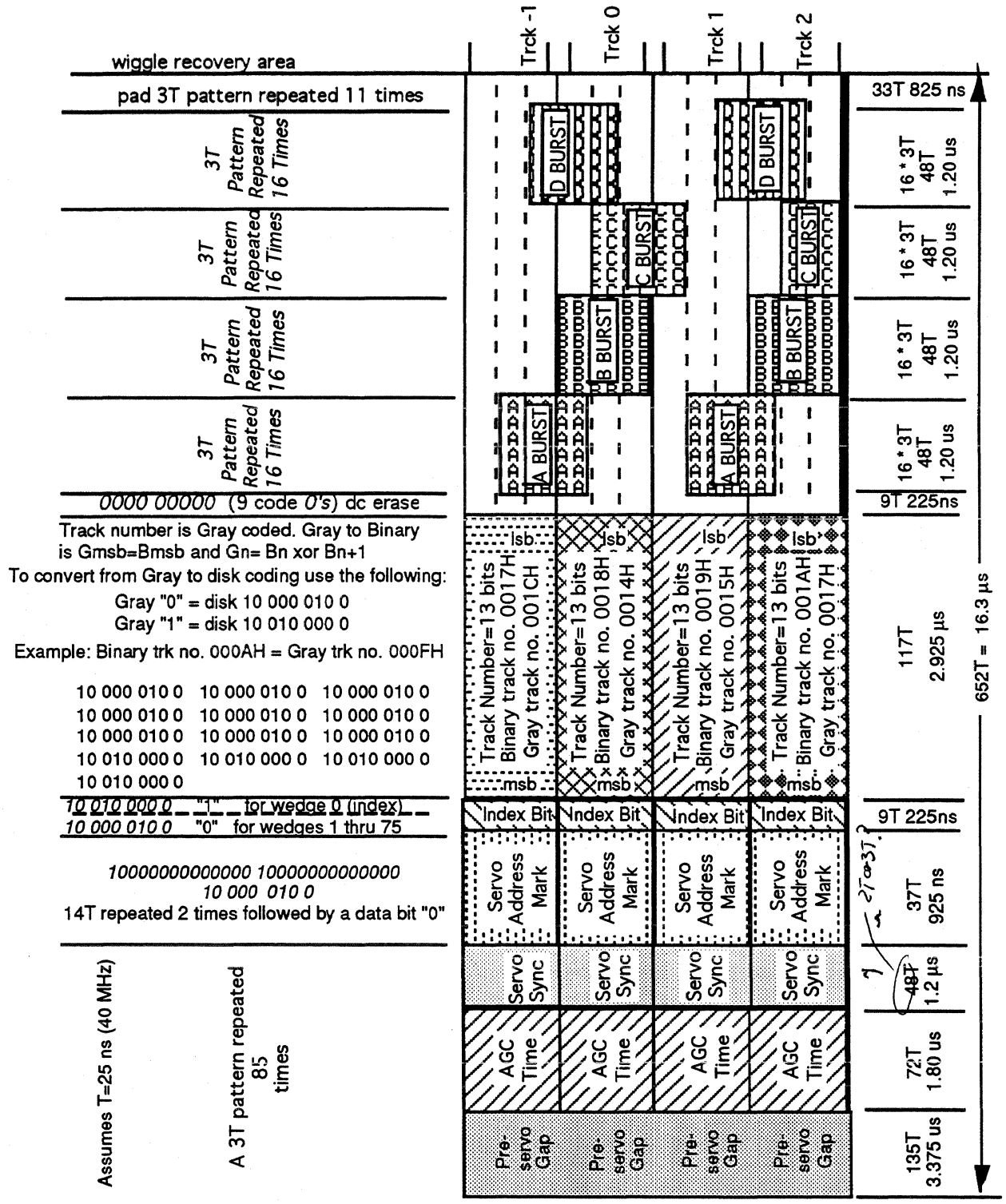

Figure 8-3 Servo Wedge Format

8.7 Servo Electronics

8.7.1 Peak Detect Channel for Servo Bursts

The peak detector channel extracts the amplitude of the A, B, C and D Bursts from the servo wedges. A weighted average Peak and Hold circuit, which resides in the Read/Write ASIC, was implemented. The gate inputs to the peak detector, and the control of which bursts are sampled, are sent from the Servo Controller module of the Disk Controller and Host Interface ASIC. The timing of these gate inputs (i.e., delay to start and duration) is programmable.

The analog average output of the sampled servo bursts are converted to digital format via the eight-bit Analog to Digital Converter (ADC). This ADC is also part of the Servo Controller module in the Disk Controller and Host Interface ASIC. The servo firmware reads the digital burst value to determine the actual head position.

8.7.2 Actuator Driver

Actuator driver / Voice Coil motor drive / spindle driver / Park ckt are in 1 chip?

The actuator driver includes a 13-bit effective DAC, a power amplifier capable of ±1.0 A and a precision current sense amplifier that can detect load current with a single resistor in series with the voice-coil motor (VCM). The retract control circuitry is fully integrated and does not require external isolation of the device power supply terminals such as external isolation transistor/diodes. Voice coil driver auxiliary digital control functions include an output-disable and low-power sleep mode following a retract of the VCM to the landing zone. During a fault condition, the actuator is disabled.

The actuator driver is integrated with the spindle driver in one IC.

8.8 Servo Error Recovery

Servo errors can be classified into two types: self-recovered servo errors (1) and fatal servo errors (2). Self-recovered servo errors are errors that the servo can recovered by itself without external interference. Examples of these errors are missing Syncs, missing SAMs, bumps, speed errors, and servo defects. Fatal servo errors require recalibration to bring the servo back. This is the case when a seek time-out or offtrack time-out occurred, or when servo lost locks to servo signal from the disk (five consecutive missing Syncs/SAMs in a row).

8.8.1 Self-recovered Servo Errors

The background code that monitoring the servo simply has to report to the host the recovered error that servo has found.

8.8.2 Fatal Servo Errors

When a recalibration is required to recover from a fatal servo error, four retries are allowed. The first three retries uses the short recalibration, and the last retry uses the long recalibration.

8.8.2.1 Short Recalibration

In this recalibration, the servo interrupt is disabled, the read/write channel is re-initialized, and the actuator unpark operation is performed, followed by track lock by servo. The seek back to the original head and cylinder is then executed. Each short recalibration process and the seek back takes about 250 msec to complete.

8.8.2.2 Long Recalibration

This calibration extends the short calibration to include the PES Gain calibration and Bias Forces calibration. It takes about 1.5 seconds to complete this recalibration to re-position the actuator to the original head and track.

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Section 9 Test Plan

9.1 Process Flow Summary

The diagram below shows the logical flow of the HDA, PCB, and assembled drive from Servowrite through Final Station at masspro.

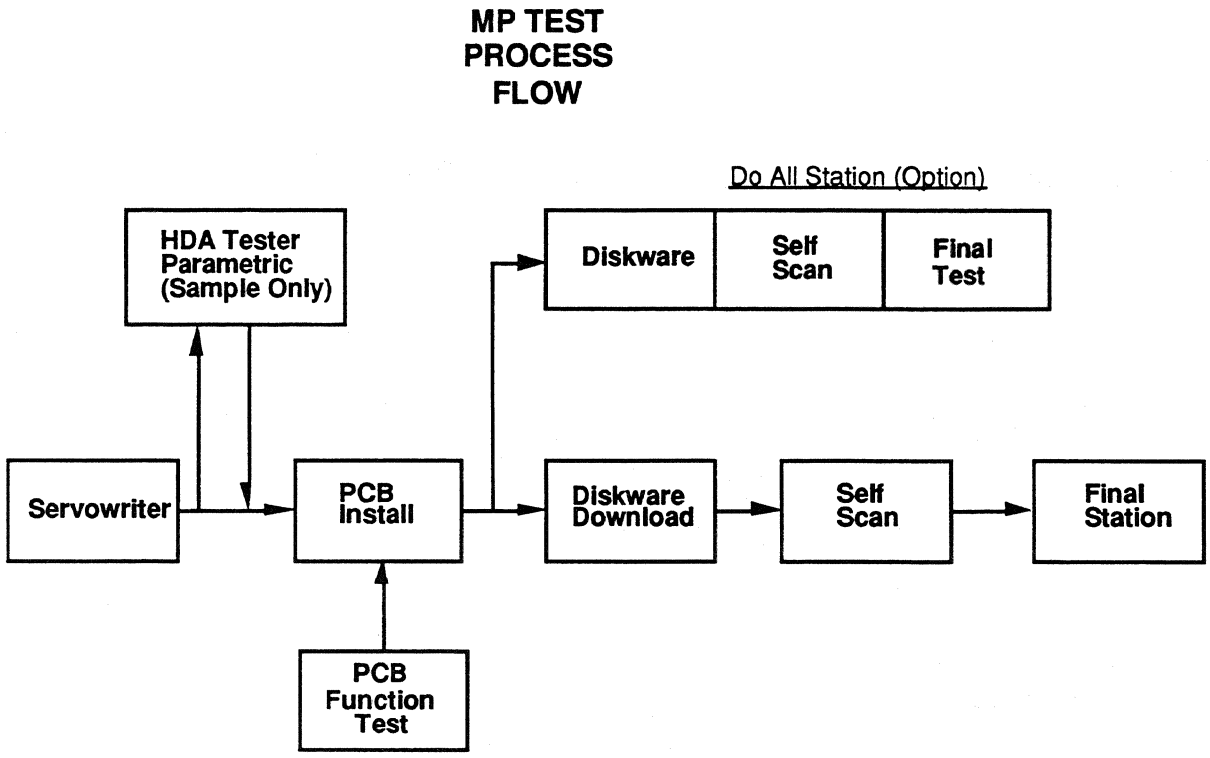

Figure 9-1 MP Test Process Flow

9.1.1 Test Process (Masspro) Detail

The Do All station can be run, at the manufacturer's discretion, as an alternative to the Diskware Download, Self Scan, and Final Station separate station method.

9.2 Servo Writer Station

The Sirocco drive uses a push-pin mechanism to position the head during the writing of the servo wedges with the cover on the HDA. The servo-writer writes wedges on each track of each surface using a staggered write method. It uses a laser positioning system to control the precise radial placement of the servo tracks.

After writing the servo wedges on all cylinders, it verifies the integrity of the wedges. In verify mode, the head is positioned at the track center of the outermost track, and then moved in one track increments to each successive track center, using the laser as the position reference. Checks are made of the amplitudes of each servo burst against the maximum and minimum amplitude required for the drive AGC and servo to operate. Also, a check of the encoded track number, and of the Sync and Servo Address Mark (SAM) fields are made. The number of tracks that are verified is reduced after masspro as the product maturity improves.

- Barcode S/N
- Initialize
- Motor Speed

- Parametric
  - Track Average Amplitude (TAA)
  - Resolution
  - Positive and Negative Modulation

- Find OD Crash Stop
- Measure Stroke
- AirLock

- Write Clock Track
  - Write Servo Wedges
  - Write Normal Pattern
  - Write 3 Times Sample rate
  - Write HDA S/N and Servowriter ID/Date/Time

- Verify Servo Wedges
  - Track Tests
  - Wedge Tests
    A/B/C Burst Verification
    AGC Field Verification
    A+C to B Verification
    TNA Check
    Wedge PES Verification

- SpinDown
- Generate TEST.OUT

9.3 PCB Test

The purpose of PCB function test is to screen out PCBs with workmanship problems or defective components, before drive level testing. This is truly a functional test in that no environmental stress, such as elevated temperature or voltage margining is applied

This test is run on a slave HDA, using pogo pins to connect with the PCB under test and the PC. Pogo pin connections are made to the following points:

- 20 to the flex connector (from below)
- 4 to the motor connector (from below)
- 4 to the power connector (from above)
- 50 to the SCSI connector (from above)
- 40 to the AT connector (from above)

To accomplish the DMA test for AT, the cable interface board is modified to include the REQ and ACK lines. Note that these lines are both ground on the SCSI cable.

This test is run on every PCB. The following test steps comprise the PCB function test sequence.

- Power Up/Detect
- Read/Write Test
- RAM Test
- Seek Test
- Jumper Test
- LED and Fuse Test (SCSI only)
- DMA Connectivity Test (AT only)
- PDIAG/DASP Connectivity Test (AT only)

9.4 HDA Parametric Test

The HDA Test will be done on an as needed basis during mass production. It will be used to monitor the consistency of parametric distributions resulting from the head/disk interface, investigate yield problems, and evaluate process changes to incoming heads and media.

The HDA Tester consists of a 486 PC operating a LeCroy 7200A (Digitizing Oscilloscope) through a GPIB port. The HDA under test is connected to the LeCroy via a captured product board and a converter board.

Since the LeCroy 7200 is a digitizing oscilloscope, there are practical limitations on the amount of sample points that can be stored and analyzed in a reasonable amount of time As a result, the data sample for the parametric tests is gathered by looking at a "segment" of the wedge to wedge data area between the 76 servo wedges.

The tests that are performed by the HDA Tester are organized below by the read/write patterns they employ. Any of these tests may be run in any or all zones depending on the requirements of the program.

- Microjog
- HFTAA
- LFTAA
- Resolution
- + Modulation
- - Modulation
- + PW50
- - PW50

- Asymmetry
- Overwrite
- NLTS
- ACSN

9.5 Diskware Station

On the Sirocco drive, firmware is partitioned and stored in two different locations. The portion of the firmware that allows the drive to accomplish basic operations (such as motor control and servo control) is located in the Read Only Memory (ROM) on the CPU, while the remainder is stored in the system cylinders on the disk. When the drive is powered up, the firmware that is stored on the disk (Diskware) is loaded into buffer memory and a complete set of firmware is available for the drive to operate. In this way, most of the firmware can be stored on the disk. This allows a cost savings to be achieved by using a smaller ROM.

The Diskware Download Station sets up the drive to begin the test process. This is accomplished by loading firmware onto the drive, preparing the system cylinders to receive data, and then writing the diskware blocks and some basic files required for the drive to function. It also writes a Self Scan "script" to a special sector on one of the drive's negative cylinders. With the Self Scan script loaded, the drive automatically executes the self scan sequence the next time it is powered up. The cycle time is the same for the 2- and 3-disk versions.

The following sequences comprise the diskware download process.

- Detect drive type
- Load ramware/CP10 and 17
- Read power up current
- Get model information
- Display CP10 zone info
- Read serial number and servo writer info
- Display power-up parameters (recal time)
- Display page 14
- Display page 17
- Set write bump to 20% (disabled)
- Coarse microjog calibration plus FIR warm-up
- Channel training zone 0 and 15, all heads
  - Input ATT for zone 0 only
  - Write precomp
  - CTF
  - TDFE
  - FIR: is it redundant?

- Turn off drive microjog control
- Microjog calibration zone 0 and 15
- Compute slope
- Display and save Cp17 and 23 to drive and files.
- Turn on drive microjog
- Train zone 0 and 15 again.
- Save page 17 to drive and file.
- Format system tracks.
- If SCSI, modify mode pages
- Turn off ECC
- Defect scan system area
- ECC on
- If SCSI, update mode pages, issues logSelect

- Load diskware twice. First time ignore errors.
- SuperOn twice
- TUR twice to clear errors
- SuperOn twice
- Check powerup current

9.6 Load Self Scan Script

Self scan is a self-contained series of processes and test sequences that comprise the core of the complete drive test sequence. As many attributes of the total drive test sequence as possible are implemented in self scan.

Self scan is run using self scan firmware and requires only power to be applied to the drive. The self scan firmware is written on the drive's negative cylinders at the diskware download station. An ASCII file called a script is used to control the test sequence. It is also loaded at diskware download.

Since the application of drive power automatically starts the self scan sequence, a password is used to enable or disable the automatic execution of the test. The password is disabled at the completion of the self scan test.

The drive, operating under its own control, executes a series of operations designed to verify the drive's functionality, calibrate the servo system, train the read channel, and "map out" defects in the media.

Media defects are identified using digital defect scanning techniques. Defect locations are discovered quickly by adding stress to the read channel while simultaneously disabling its ability to do error correction. Self scan will produce a defect map that will be used during factory format for sector relocation and defect sparing.

The Self Scan test is a high temperature (50°C) environment to simulate a worst-case operating condition for the drive.

Each routine saves test and process data to cylinder -1. The data is read and manipulated by the host computer at final station.

The following sequences comprise the self scan process.

- Power Up
- KLOOP/PES Calibration (TBD by Servo and F/W Groups)
- Servo Verify Test
- Start/Stop Test
- Null Current Test
- Runout Test
- Fixed Length Seek Time Test (One-Third Stroke and Full-Third Stroke)
- Head Switch/Single Track Seek Test
- Random Seek Test
- Adaptive Equalization
  - FIR Training
  - Input Attenuation
  - Adaptive Write PreComp
  - Continuous Time Filter

- Guard-Band Erase
- Wedge to Wedge Scan
- Format Drive
- Physical Sequential Stress Write/Read with ECC Disabled
- Format In Line
- Logical Sequential/Random Write/Read with H/W ECC Channel
- Defect Verify/Scratch Check/Scratch Fill
- ECC Test
- Sequential Throughput Test
- Random Throughput Test
- Buffer RAM Test
- Delete Password
- Microjog Calibration
- Servo Stability Test (TBD by Servo and F/W Groups)
- Servo Resonance test (TBD by Servo and F/W Groups)

9.7 Final Station

This station is used to test the drive through the interface and to collect all the self scan information. This is the only test in our process where we are able to simulate a customer environment. At this station, we should only be testing the things that can't be tested at self scan. The faster the host system, the more complete the testing we can perform. Due to manufacturing considerations, this test should be limited to less than five minutes.

The following sequences comprise the final station process.

- Read Servo Writer Serial Number
- Read SelfScan Report
- Enable DPA for AT
- Start/Stop Test (10 Start/Stop, use Super Command)
- Short Logical Scan
- Throughput Test
  - Random Throughput Test
  - If SCSI, turn on Sync Mode
  - Sequential Throughput Test

- Write Configuration Pages

Appendix A Schedule and Major Milestones

Date	Goal	Location	# HDA's	# SCSI	# AT
10/10/94	E0	Quantum	<20		
12/12/94	E1	Quantum	50		
3/9/95	E2	MKE	150		
6/15/95	P0	MKE			
7/15/95	P1	MKE	400		
9/21/95	P2	MKE	1500		
11/27/95	PMP	MKE	3000		
12/95	Mass Pro	MKE	Large	Large	Large

Table A-1 Scheduling Goals for Sirocco Program

	E0	E1	E2	P1	P2	PMP
Objectives	• Familiarization with MR heads, preamp, media	• Demonstrate recording density	• EVT for new components • Prelim DVT, if possible • Process debug • Test Engr debug for P1 • First MKE build	• H/M matrix evaluation • DVT • Full suite of CSS tests • Compat test start • Create eng samples	• FMT and DMT • Customer qual units	• Prove drive, process, and components mature enough to ramp
Heads and Media	• Standard media, any usable MR heads (Europa heads, if necessary)	• Utilize first "per spec" MR heads, if available	• Multiple viable vendors participating in bid • Acquire preliminary ESD statistics from HSA operation	• Full matrix of possible MP participants • Correlate A/P to drive level performance • Identify all unique MR head phenomena/failure modes	• Acceptable yields from all MP H/M combos • All required MR head recovery algorithms proven	• Identify H/M combos OK for MP, or later qual

	E0	E1	E2	P1	P2	PMP
Hardware Level	• Modified Fireball • DC-DC converters • Differential preamps, TI and VTC • Investigate 3 possible motion control drivers	• First single-disk and multiple-disk protos	• Includes mods from design review • Reduce motion control drive options • 2nd Si preamps	• Hardware as close to MP as possible • Minimize parallel paths and options • Identify possible "late release" acyclical IC Rev deliveries	• All MP hardware in place	AT and SCSI into MROM
Drive Functionality (relative to spec)	• Check 1/3 Tk servowrite concept with Fireball hardware •Preliminary checkout of MR preamp and flex ASMs • Servo, if possible • Single sector data transfer	• Prove servo capability with MR heads • Drive level SNR and BER measurements • Functional with host computer	• Initial error rate measurements at NTNV • Identify preliminary DVT problems and likely P1 failures	• Identify major failure modes at P1 • Maximum passing drives through process, with relaxed P/F criteria identified • DVT failures identified, with corrective action	• Drive meets all specs	• No outstanding DVT/DMT issues
Test Equipment Requirements						
•servowriter	• Servo writer supports E0	• Servowriter supports E1	• Servo write without verify	• All equipment debugged at MKE	• Satisfactory throughput for MP	• All P/F test limits agreed upon with MKE
• analog parametrics	• N/A	• N/A	• No A/P	• Major throughput issues identified		
• PCB functional test	• N/A	• N/A	• Prelim PCBA functional test • All functions ready for P1 and tested in USA			

	E0	E1	E2	P1	P2	PMP
Process Goals	• N/A	• N/A	• Attempt diskware download at MKE • P1-Start process demo'ed in USA before P1	• Process to evolve from P1-Start version • Selfscan completion expected to be MR head-dependent	• Selfscan/ DoAll • Digital Scan only as an engineering tool	• Digital scan not used at PMP • Process finalized for MP
Acceptance Criteria • Expected Eng/ Qual testing	• Meet minimum functionality only	• Drive functionality rqmts. only	• Full function drives proven through P1 process	• Major specs met at NTNV and MKE test temperatures	• FMT passed for PMP start	• All yield issues cleared with MKE
• Drive characterization			• EVT summary report	• DVT complete. Issues and actions decided	• DMT complete. Issues and actions defined	• Any 2nd release reqmts identified and planned out
• Yield goals			• P1 yield estimate made from process "Dry Run"	• Yield goal is 50% minimum • Remaining process changes identified	• Yield goal is 75% minimum • Drive meets specs at all T and V	• Yield goal is 85% minimum

Table A-2 Models Defined

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Appendix B Standards

Sirocco drives will meet the following regulatory specifications:

Underwriter Laboratory (UL)

Sirocco drive will meet the current edition of UL 1950, Standard for safety: Information technology equipment including business equipment.

Locked Rotor Test acceptable for UL 1950, No.950 will be included as part of UL Certification.

UL Recognition shall be obtained without any special or unusual conditions of acceptability. A copy of the UL Recognition Report, including Conditions of acceptability, will be provided.

The drive will bear the UL required identification markings which provide proof of UL Recognition. Use of the UL backwards "UR" is preferred.

Canadian Standards Association (CSA)

Sirocco drive will meet the current edition of CSA - C22.2 No. 950-M89.

information technology equipment including business equipment.

Locked Rotor Test acceptable for CSA 22.2, No. 950 will be included as part of CSA

Certification.

CSA Certification shall be obtained without any special or unusual conditions of acceptability. A copy of the CSA Certification Report, including Conditions of acceptability, will be provided.

The drive will bear the CSA required identification markings which provide proof of CSA Certification.

European standards (VDE and TUV)

Verband Deutscher Electroechnier (VDE)

Technisher Uberwachungs Verein (TUV)

Sirocco drive will meet the current edition of EN 60 950. European Community Regulations for safety of Information technology equipment including Electrical business equipment and IEC950, Safety of Information technology equipment including Electrical business equipment.The drive will also meet the requirements of DIN/VDE 0805,Safety specification for business machines.

Locked Rotor Test acceptable for EN60 950 and IEC 950 will be included as part of VDE and

TUV approval.

Approval shall be obtained without any special or unusual conditions of acceptability. A copy of the report, License and Construction Data Forms will be provided.

The drive will bear VDE or TUV required identification markings which provide proof of VDE and TUV approval.

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Appendix C Packing

General Information

Quantum seeks not only to ship products that provide the latest in technological features, but also to ensure that these products arrive at the customer's site in the same condition that they left our factories.

Shipping Containers

Two (2) sizes of shipping containers will be required for Sirocco products. These are:

- 1-Pack Shipping Container
- 12-Pack Shipping Container.

The 1-Pack Container holds one (1) disk drive and the 12-Pack holds twelve (12).

- The shipping containers shall be sufficient to protect the parts enclosed, and must comply with the packaging requirements of the latest issue of Uniform Freight Classification Rules, or other applicable carrier requirements.
- The containers are intended for single-use.
- Container sizes should be selected such that when arranged upright on a 4-way 40"Wx48"D pallet, the containers do not overhang the edges of the pallet deck. Containers when arranged on the pallet, should maximize utilization of the pallet deck area and the available 48" load height.
- Closures must permit handling without specific precautions.
- The corrugation used in these containers must have sufficient strength to prevenat collapsing of the container under double stacked pallet loads.

Identification

- Each shipping container must be identified on sides #3 and #4 (See FigureC-2) with the following basic information:

  Quantum Logo
  Symbols to indicate:
  - The proper orientation of the TOP of the container.
  - The container contents are FRAGILE.
  - The container should be protected from water, rain, etc.
  - The container contents are sensitive to static electricity.

- The following letters should appear on side #5: "_ of _". This permits identifying each container as part of a group with a marking pen, e.g. 5 of 12.

Documention

- 1- Pack Carton: TBD
- 1-Pack Insert: TBD
- 2-Pack Carton: TBD
- 2-Pack Insert: TBD
- Plastic Bag: TBD
- Static Warning Label: TBD

Packaged Finished Goods Product Shock & Vibration Test Standards

This section outlines the laboratory test levels required to assure the arrival of Quantum Finished Goods (F/G) products to the end user without damage or loss of performance beyond the published specifications. The packaged products must be tested prior to product release to assure adequate protection against the shipping and handling hazards anticipated in the domestic and international distribution network.

- REFERENCE CONDITIONS and TOLERANCES
  Unless otherwise stated, the ambient conditions of the laboratory and tolerances for test conditions are:

Temperature	23 °C ± 5°C
Humidity	30% to 70% RH (not controlled)
Acceleration	+15%, -5% Peak
Velocity Change	+10%, -2%
Frequency	± 0.5Hz

Table C-1 Assumed ambient conditions and tolerance for test conditions

- APPLICATION
  This specification shall apply to all Quantum products which are identified with the name "Quantum" and/or the Quantum logo applied to the product regardless of whether the product was fully or partially manufactured and packaged by Quantum or an outside supplier.

NOTE: This test standard is a procedure to assure the maximum values of shock (Critical Acceleration) are NOT exceeded. Also, this standard details the vibration tests required to assure the packaged cushion resonances will NOT damage the Quantum F/G packaged product.

- EXCEPTIONS OR DEVIATIONS
  Any exceptions or deviations from the product standards must be approved by the Engineering Product Manager, the Product Marketing Manager and Quality Assurance. Any deviation or exemptions must noted in the Product Plan. Quantum O.E.M. customer and O.E.M. supplier requirements must be reviewed by Quality Assurance prior to contractual finalization by Quantum to avoid both over-packaging and under-packaging of Quantum products.

- FINISHED GOODS PRODUCT TESTS
  - Vibration
  a. resonance search / Dwell
  b. resonance endurance - SINE wave
  c. stacked resonance

  - Shock: "Free Fall Drop"

- PRE-TEST AND POST-TEST INSPECTION AND FUNCTIONAL TEST
  All specimens must be thoroughly functionally tested prior for submission of packaging testing and the characteristic data recorded for comparison with post test data. The product must be visually inspected prior to packaged testing.
  After the shock and vibration tests are performed the specimen must be functionally tested to assure the unit is performing to specification. The specimens must be carefully inspected for structural,cosmetic and mechanical damage after shock and vibration tests.
  The units under test shall be inspected and functionally tested between each segment of the shock and vibration tests series.

- PACKAGING ACCEPTANCE
  If during any segment of the F/G packaged product test the product fails to meet the required functional specifications, or the product has incurred structural damage, or the unit has been cosmetically blemished (other than fixturing markings), the packaging shall be considered "FAILED".
  Note: any intermittent problems should be considered "FAILED".
  If packaging is considered "FAILED", the system should be rechecked to assure the system under test was not an unreliable sample and more samples must be tested to confirm either an acceptable or non-acceptable sample.
  Before final acceptance, the system under test will be "burned-in" for 30 continuous days and retested to assure there are no latent failures introduced in the abuse

- CARTON ORIENTATION
  The cartons are identified by figure C-1.

- • VIBRATION TESTS
  - Resonance Search
  Resonance search within a range of 3-200-3 Hz. at a constant acceleration input of 0.5Gs must be performed on three axes of the packaged assembly. An X-Y Log-Log plot must be permanently recorded for each axis tested at each monitoring position. If the packaged unit can conceivable be shipped in a position other than the upright position, all three axes must undergo a resonance search.

  - Resonance Dwell-SINE Wave
  Each potential shipping axis must be endurance tested for a total one hour, 15 minutes per resonant frequency at an input of 0.5Gs acceleration. If the requirement of a full one hour cannot be achieved, the balance of the hour must be performed with the vibration system continually sweeping from 3-200-3 Hz. 0.5Gs constant acceleration input.

  - Pallet Stack, Resonance Endurance Test must be performed with the Finished Goods cartons stacked in the normal shipping orientation in a single column to the anticipated maximum height of a pallet load. For safety reasons, the proper fences (lateral support restraints) must be utilized. After each axis is endurance tested, inspect all products in the column stack for cosmetic and structural damage. Then perform a functional test on the unit checking for intermittent or permanent malfunction.

- RESONANCE SEARCH
  The vibration system frequency adjusted for stacked resonance (maximum displacement of the top unit) at an input acceleration of 0.5Gs of the table.

- RESONANCE DWELL
  The endurance test to run a total of 15 minutes at the stacked resonance frequency.

- SHOCK TEST: FREE FALL DROP TEST
  The free fall drop test must be performed using a drop test mechanism which will provide accurate and repeatable drop heights. Also, the mechanism must be able to assure accurate and repeatable package orientation during impacts.
  The acceleration levels must be monitored by the use of accelerometers and the resulting curves permanently recorded on photographs. The levels detected must not exceed the critical acceleration determined by the bare unit damage boundary tests.

- TEST SEQUENCE

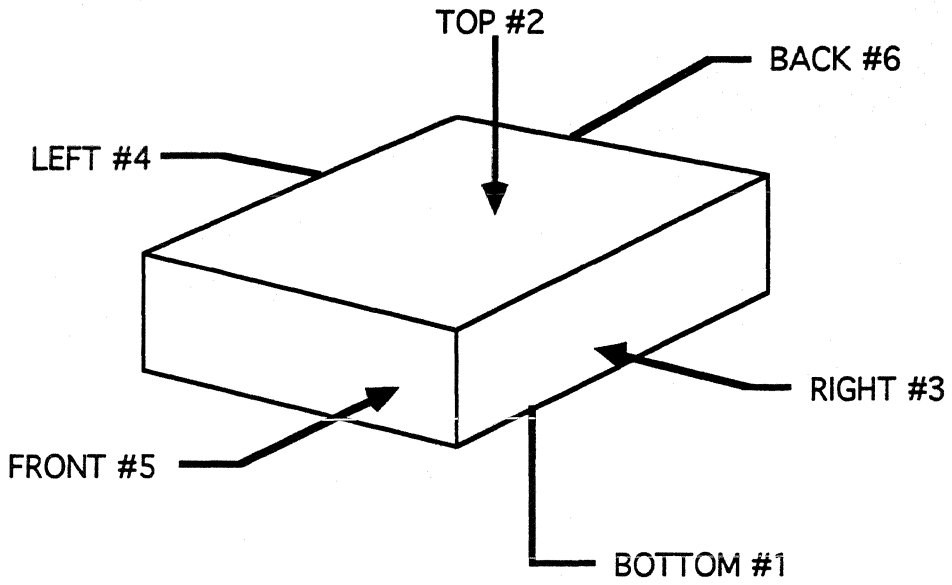

Figure C-1 Sirocco carton face identification.

The package product shall be shock tested by dropping the F/G package in the following sequence:

DROP #	IMPACT
1	bottom (1)
2	top (2)
3	right (3)
4	left (4)
5	front (5)
6	back(6)
7	edge (2-3)
8	edge (5-3)
9	edge (5-2)
10	corner (2-3-5)

Table C-2 Free fall drop testing sequence.

- DROP HEIGHTS

Gross Weight	Drop Height	No. of Drop
0 - 20 lbs.	30 inches	10
21 - 40 lbs.	24 inches	10
41 - 60 lbs.	18 inches	10
61 - 80 lbs.	12 inches	10
81 - 200 lbs.	6 inches	10
200 lbs. and above1	15/9 inches2	1/5

Table C-3 Drop heights required for F/G Quantum products

Notes to Table C-3:

1. If the F/G items are unitized (palletized), 10 impacts at 9 inches are required on the bottom orientation only.
2. First number is the base or bottom drop, second number is the drops on all other surfaces.

After drop testing the product, reinspect for structural and cosmetic damage. Also retest for intermittent and permanent functional malfunction. Subject the units run through the shock tests to a 30 day burn-in test before the final functional test is performed.

- COMPRESSION TEST
  Floating platen compression test equipment shall be used in this test in accordance with ASTM D-642-76. The test shall be conducted on five (5) identical packages with all internal packaging components and an actual product or dummy load. The average of the five (5) tests shall be used to determine the acceptability of the container/package system.
  Compressive forces are to be taken to the maximum required load or to failure.
  The maximum compressive rate is 0.5 inches per minute.

  The minimum acceptable compressive resistance (load) will be based on the HIGHEST value calculated by using the following methods:

  - A. Four (4) times the greatest expected compressive load during transportation or storage.
  - B. Ten (10) times the weight of the product intended to be packaged.
  - C. 300 lbs. compression resistance.

- REFERENCE DOCUMENTS
  National Safe Transit Association (N.S.T.A.) Test procedures Project 1A.1973

- A.S.T.M. Documents
  D-642-76 Compression Test for Shipping Containers
  D-775-61(73) Drop Test for Shipping Containers
  D-880-79 Incline Impact Test For Shipping Containers
  D-996-78 Packaging and Distribution Environments def. of terms
  D-999-76 Vibration Testing of Shipping Containers
  D-1083-53(79) Testing Large Shipping Containers and Crates
  D-3331-77 Assessment of Mechanical-Shock Fragility Using Package Cushioning Materials
  D-3332-77 Mechanical-Shock Fragility of Products, Using Shock Machines
  D-35680-80 Vibration (Vertical Sinusoidal Motion) Test of Products

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Appendix D Air Cleanliness

Classification of air cleanliness is based on particle count with maximum allowable number of specified minimum sized particles per unit volume and on statistical average particles size distribution.

DEFINITION OF CLASS 1001

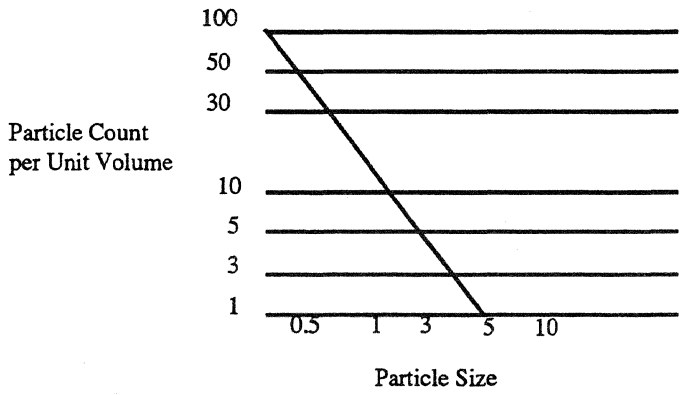
The particle count shall not exceed a total of 100 particles per cubic foot (3.5 particles per liter) of size 0.5 µm or larger.

The statistical average particle size distribution may deviate from this curve because of local or temporary conditions. Counts below 10 particles per cubic foot (0.35 particles per liter) are unreliable except when a larger number of samplings are taken.

TEST METHOD2

For particles in the 0.5 to 5.0 µm size range, equipment employing light scattering principles shall be used. The air in the controlled environment is sampled at a known flow rate. Particles contained in the sampled air are passed through an illuminated sensing zone in the optical chamber of the instrument. Light scattered by individual particles is received by a photodetector which converts the light pulses into electrical current pulses. An electronic system relates the pulse height to particle size and counts the pulses such that the number of particles in relation to particle size is registered or displayed.

The count of particles of a given size shall not exceed value shown in the graph below.



1. U.S.A. Federal Standard 209B, available from the General Services Administration; Specifications Activity; Printed Materials Supply Division; Building 197; Naval Weapons Plant; WashingtonD.C. 20407, U.S.A.

2. American Society for Testing and Materials; Standard ASTM F 50; 1916 Race Street; Philadelphia, Pennsylvania 19103, U.S.A. Society for Testing and Materials; Standard ASTM F.

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Appendix E Humidity Charts

These charts are given as reference for any who care to gain a greater understanding of the humidity specifications given in the Environment section. Except for references to specific figure numbers, the explanation is quoted directly from that monster of a book that Don Westwood owns, Marks' Standard Handbook for Mechanical Engineers, McGraw-Hill Book Co., Eighth Edition, New York, © 1978.

Psychrometric charts are usually plotted, as indicated by the example Figure E-1, with dry-bulb temperature as abscissa and specific humidity as ordinate. Since the specific humidity is determined by the vapor pressure and the barometric pressure (which is constant for a given chart), and is nearly proportional to the vapor pressure, a second ordinate scale, departing slightly from uniform graduations, will give the vapor pressure. The saturation curve (relative humidity = 100%) gives the specific humidity and vapor pressure for a mixture of air and saturated vapor. Similar curves below it give results for various values of relative humidity. Inclined lines of one set carry fixed values of the wet-bulb temperature, and those of another set carry fixed values of va, cubic feet per pound of air. Many charts carry additional scales of enthalpy or Σ function.

Any two values will locate the point representing the state of the atmostphere, and the desired values can be read directly. Figures E-2 and E-3 are psychrometric charts from the General Electric Company and Ellenwood and Mackey, "Thermodynamic Charts," covering a dry-bulb temperature range from 32 to 300°F. They are accurate only for a barometric pressure of 29.92

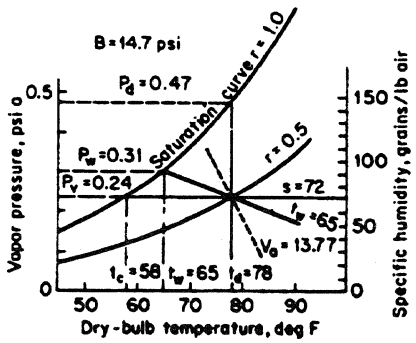

Figure E-1 Skeleton humidity chart.

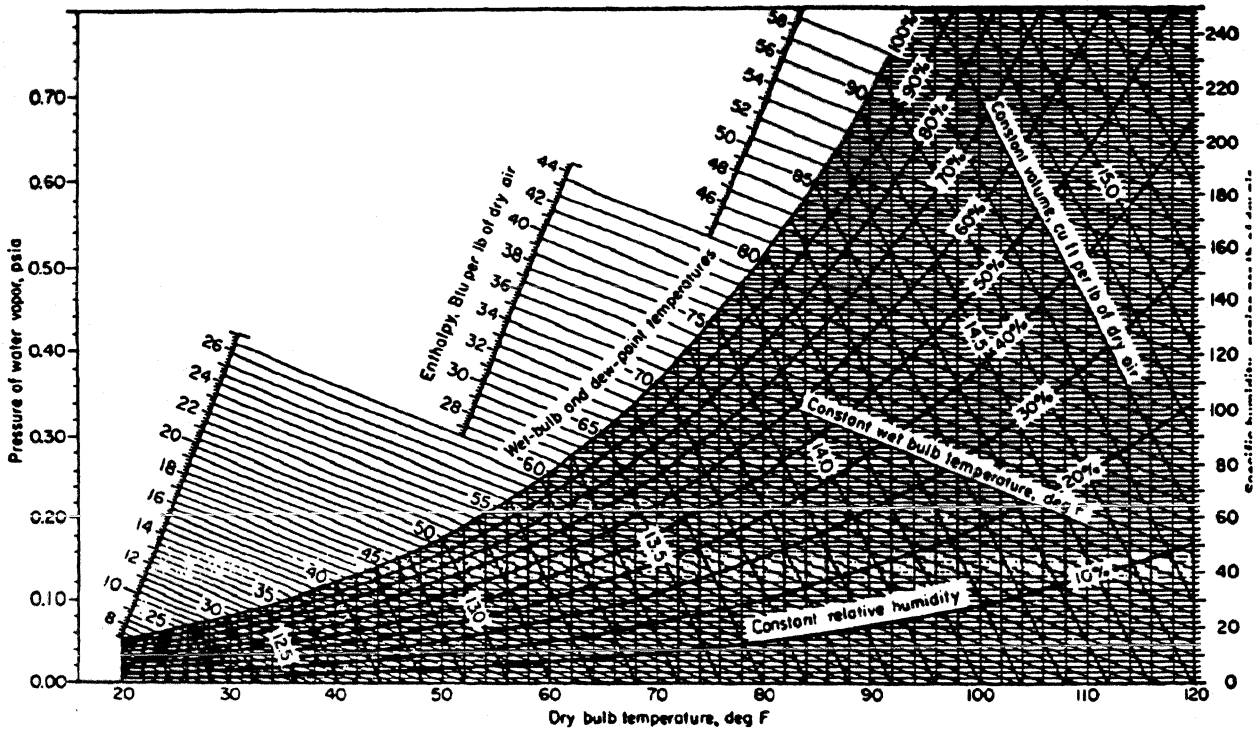

Figure E-2 Humidity chart for low temperatures. Barometric pressure 14.969 psia.
(Copyright by General Electric Co.)

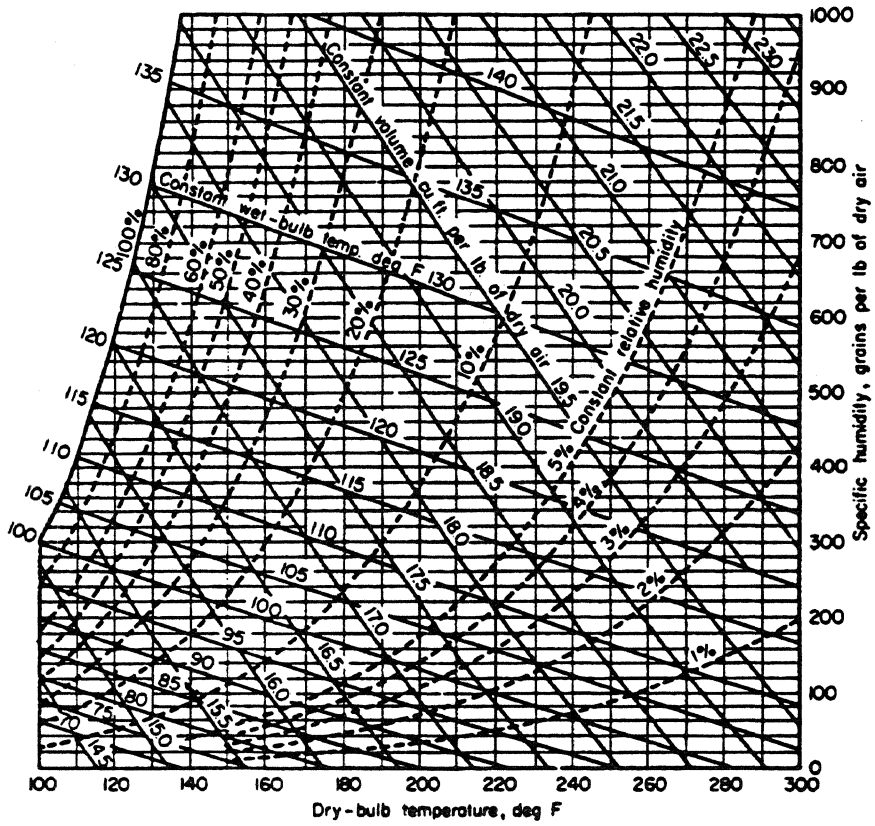

Figure E-3 Humidity chart for medium temperatures.
(from Ellenwood and Mackey, " Vapor Charts, " Wiley.)

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