Bigfoot 1.2 / 2.5 GB

Field Engineering
Training Guide

January 1996

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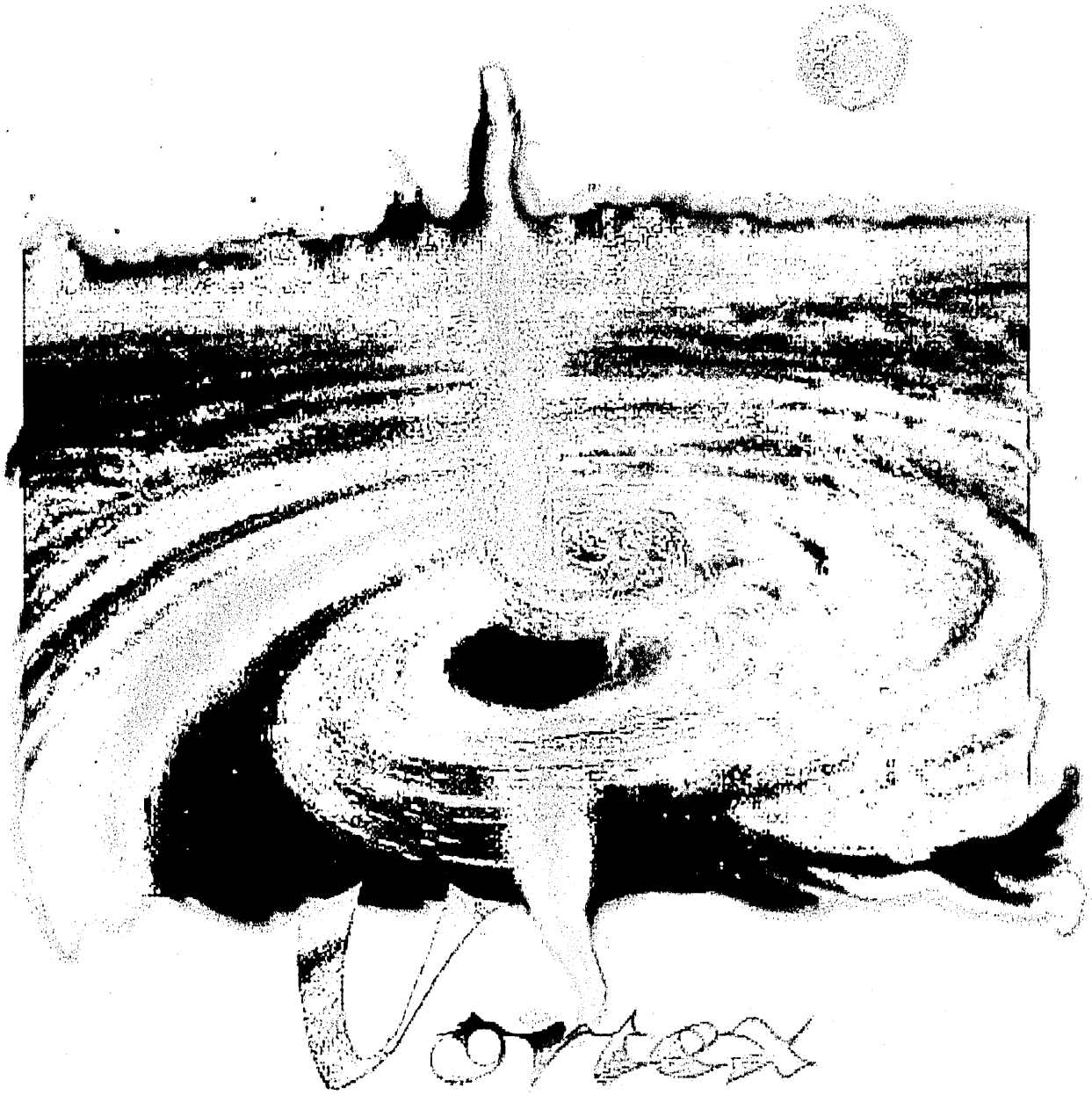

Vortex

Data Guide

November 1995

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Section 1Background Information

1.1 General Description

Vortex is a family of low profile 5.25 - inch rigid disk products with capacities of 1280 MB and 2560 MB . Only the AT interface will be supported.

Description	# of Data Disks	# of Data Surfaces	Capacity
A. 0.750" AT	1	2	1280 MB
B. 0.750" AT	2	4	2560 MB

Table 1-1. Summary of Vortex product line.

1.2 Basic Development Assumptions

The need to bring Vortex to market within a critical "time-window" dictates that Fast Cycle Time methods be used in the product development.

Manufacturing will be done in Japan by MKE, lowering process risk and increasing cost competitiveness.

1.2.1 Top Development Priorities

1) Low cost: BOM cost < $100.00 at mass pro start for 1280MB.
2) Time to market: full spec. evaluations by March1996.
3) Performance: 17 ms seek with large ultra thin HDA.

1.2.2 Top Development Risks

1) Mechanical
   - Achieve 17 ms seek time.
   - Meet 40 dB idle acoustic.

2) Motor, VCM Hitachi "Combo" " Mighty" Backup

3) Heads & Media
   - Signal to Noise at 461 Mb/in^2 with 4298 TPI, and 114k FCI.
   - Fly Height Control, may not be able to meet Altitude Spec.
   - 20,000 CSS with Low Glide.
   - 5.25" Media Availability.

4) Test Process
   - Servo Writer mechanics for 5$^{1/4}$" HDA..

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Section 2 Specifications

This section provides the physical, electrical, and environmental specifications for the Vortex 1280/2560 MB hard disk drive.

2.1 General Specification

2.1.1 Capacity/Format/Channel Specification

MODEL	1280 MB	2560 MB
Spindle Speed	3599.5 RPM	3599.5 RPM
Servo Method	Embedded	Embedded
Servo Sample Per Track	96	96
Outer Radius	2.4740 in	2.4740 in
Inner Radius	1.1311 in	1.1311 in
Stroke	1.3429in	1.3429in
Recording Code	16/17 PRML	16/17 PRML
Recording Zone	15	15
TPI	4298	4298
Flux Change Per Inch (Max)	113,922	113,922
Bits Per Inch (Max)	107,221	107,221
Areal Density	460.84 Mb/in^2	460.84 Mb/in^2
Data Rate	84 Mb/s (Max) 43 Mb/s (Min)	84 Mb/s (Max) 43 Mb/s (Min)
Number of Disks	1	2
Number of Heads	2	4
Formatted Capacity	1290.98 MB	2581.96 MB
Total Cylinders	6004	6004
User Data Cylinders	5738	5738
System Cylinder	34	34
Data Tracks	11,476	22,952
Data Surfaces	2	4
Sectors Per Track	149 - 276	149 - 276
Data Bytes Per Sector	512	512
Spare Sectors (1 per cylinder + 20 tracks)	8608	8613
Logical Blocks	2,512,844	5,034,291
AT Logical Capacity	1286 MB	2577 MB
AT Logical Sectors	2,511,936	5,033,952
AT Logical Cylinder	2492	4994
AT Logical Heads	16	16
AT Logical Sectors/Track	63	63
Buffer & RAM (128 KB)	Single 64 x16 DRAM	Single 64 x16 DRAM
Cache Size	87 KB (Minimum)	87 KB (Minimum)
Data Format	I.D. after Wedge (Multiple Sectors per Wedge)	I.D. after Wedge (Multiple Sectors per Wedge)
ECC	160 bit RS with Cross Check	160 bit RS with Cross Check

Table 2-1. Capacity/Format/Channel Specification

2.1.2 AT Interface Specification

Interface Features	
	Auto Task Register Updates[1] Multi Block Auto Read [1] Multi Block Auto Write[1] Cable Select Local Bus PIO and DMA timing Multiword DMA Transfer Multi Command Auto Read S.M.A.R.T Phase 4
Interface	ATA/CAM
Interface Transfer Rate	
	PIO[2] Mode 3 11 MB/s Mode 4 16 MB/s **DMA** Mode 1 13 MB/s Mode 2 16 MB/s
Performance	
Sequential Throughput[3]	
Read	5.7 MB/s (4096 Byte record)
Write	5.7 MB/s (4096 Byte record)
Random Throughput	
Read	19 KB/s (512 Bytes per command)
Write	17 KB/s (512 Bytes per command)
PC Bench Disk Harmonic	**TBD**
Q-Bench Data Access Time	**TBD**
Sustained Throughput Read	**TBD**
Signal Conditioning I/O Drivers	Edge Rate Control (5 ns rise & fall times minimum) High hysteresis noise rejecting input buffers

Table 2-2. AT Interface Specification

Notes to Table 2-2:

1. Auto features support CHS, LBA, and DMA transfer, Read multiple, Write multiple.
2. Rates above 6 MB/s require IOCHRDY.
3. Sequential performance is typical performance at O.D. data zone.

2.2 Timing Parameters

1280/2560 MB Timing Specifications

	Typical Nominal[1]	Maximum Worst Case[1]
Sequential Cylinder Switch Time[2]	3.5 ms	5.0 ms[4]
Sequential Head Switch Time[3]	3.0 ms	5.0 ms[4]
Random Average (Read or Seek)	15.5 ms	18.5 ms
Random Average (Write)	17.0 ms	18.5 ms
Full Stroke Seek	30.0 ms	34 ms
Average Rotational Latency	8.33 ms	
Standby or Power on to Drive Ready[5, 6]	11.5 s	18 s
Stop Time	TBD	TBD

Table 2-3. Timing Specifications

Notes to Table 2-3:

Quoted seek times include head settling time, but do not include command overhead time or rotational latency time.

1. Nominal conditions are defined as 25 °C ambient, nominal supply voltages and no applied shock or vibration. Worst case conditions are defined as worst case extremes of "operating" temperature, humidity, and supply voltages.

2. Sequential Cylinder Switch Time is the time from the conclusion of the last sector of a cylinder to the first logical sector on the next cylinder averaged across stroke.

3. Sequential Head Switch Time is the time from the conclusion of the last sector of a track to the beginning of the first logical sector on the next track of the same cylinder averaged across stroke.

4. Including sequencer overhead for write setup on head & cylinder switch. No more than 5% of head /cylinder switches will exceed this value.

5. At power on startup error algorithms are used and these may require additional time in coming ready. These recovery routines may extend the time to ready to as large as 30 seconds.
6. Recal Record enabled for typical nominal

2.3 Disk Errors

Error Type	
Uncorrected Read Errors[1]	1 Event per 10^7 bits read[2]
I.D. Error [3]	1 Event per 10^7 bits read[2]
Recovered Read Errors[4]	1 Event per 10^{10} bits read
Multi Read Recovered Errors[5]	1 Event per 10^{12} bits read
Unrecovered Data Error[6]	1 Event per 10^{14} bits read
Transferring erroneous data to customer[7]	
On the Fly (Single or Double correction)	1 Event per 5.88 x10^{25} bits read
Off Line Correction (Triple correction)	1 Event per 1.19 x10^{38} bits read
Seek Errors[8]	1 Error per 10^6 seeks
Bump/Gray Code error rate[9]	TBD

Table 2-4. Error types and rates

Notes to Table 2-4:

1. Uncorrected Read Errors are those read errors with Read on arrival, ECC on the fly and retries are disabled. It's to monitor manufacturing process only.

2. Error rates are for worst case temperature & voltage.

3. I.D. Errors are defined as any read error (or sequence of read errors) causing the firmware to exhaust its ID search retry count without retrieving the required ID data. (For internal use only)

4. Recovered Read errors are those which require retries for data correction. Errors corrected by ECC on the fly are not considered recovered read errors. Read on arrival is disabled to meet this specification.

5. Triple Burst recovered errors are those read errors which require the triple burst error correction algorithm to be applied for data correction. This correction is typically applied only after the programmed retry count is exhausted. (For internal use only)

6. Unrecovered read errors are those errors that are not correctable using an error correcting code (ECC) or retries. The drive terminates retry reads either when a repeating error pattern occurs or after eight unsuccessful retries and application of double burst error correction.

7. Probability of misdetection. (For reference only)

8. A seek error occurs when the actuator fails to reach or remain on the requested cylinder, and the drive requires the execution of the full recalibration routine to locate the requested cylinder.

9. Bump/gray code errors are servo field read errors that require sequencer shutdown during a write operation and invocation of a write retry. This error rate does not apply with externally applied vibration. Bump error rate should be set such that write throughput does not degrade by more than 5% from best case.

   For explanation of terms and more detailed information regarding how these numbers were arrived at, please see Section 7.3. ECC.

2.4 Power Requirements

1280/2560 MB hard disk drive operates from two supply voltages:

- +12 V ± 10%
- + 5 V ± 5%

The allowable ripple and noise for each voltage:

- +12 V 250 mV P-P 1Hz-100MHz
- + 5 V 100 mV P-P 1Hz-100MHz

2.4.1 Drive Power Dissipation

1 Disk Power Dissipation

Mode of Operation	Typical Avg. Current (mA)	Typical Avg. Current (mA)	Typical Avg. Power (Watts)
	+12V	+5V	
Start up[1]	1400	425	19
Idle[2]	230	250	4.0
Read/Write Ontrack[3]	230	450	5.0
Read/Write/Seek[4]	360	420	6.5
Max Seeking[5]	550	380	8.5
Standby[6]	5	190	1.0
Sleep	5	190	1.0

Table 2-5. 1 Disk Power dissipation in various modes

2 Disk Power Dissipation

Mode of Operation	Typical Avg. Current (mA)	Typical Avg. Current (mA)	Typical Avg. Power (Watts)
	+12V	+5V	
Start up[1]	1400	425	19
Idle[2]	270	250	4.5
Read/Write Ontrack[3]	270	450	5.5
Read/Write/Seek[4]	400	420	7.0
Max Seeking[5]	590	380	9.0
Standby[6]	5	190	1.0
Sleep	5	190	1.0

Table 2-6. 2 Disk Power dissipation in various modes.

Notes to Table 2-5, 2-6 :

1. Startup is stated as the peak (>10 ms) power required during spindle startup. This power will be required for less than 6 seconds.

2. Idle: when the drive is not reading, writing, or seeking. the motor is up to speed and DRIVE READY condition exists. Actuator is residing on last track accessed.

3. Read/Write/Ontrack: is for 50% read operations and 50% write operations on a single physical track.

4. Read/Write/Seek: when data is being read from or written to the disk. The head is assumed to be on-track. Implies no more than 40% of the time is spent seeking, 30% of reading and 30% of writing.

5. Max Seeking: is for continuous random seek operations with 8.3 ms delay between seek complete indication and next seek command.

6. Standby: when the motor is stopped, actuator parked, and all electronics except the interface control is in low power state. STANDBY will occur after a programmable time-out since last host access occurs. Drive ready and seek complete status exist. The drive will leave STANDBY upon receipt of a command which requires disk access or upon receipt of a spin-up command.

7. Power requirements reflect nominal values for +12v and +5v power supplies.

8. Current is rms. (except for Startup)

2.4.2 Power Sequencing

No damage or loss of data will occur if power is applied or removed in any order or manner, except that data may be lost in the sector being written at the time of power loss. This includes shorting out or opening up either voltage return line, and transient voltages of **+10% to -100%** from nominal, while powering up or down.

2.4.3 Power Reset Limits

When powering up, the drive will remain reset (inactive) until both V_{HT} reset limits are exceeded. When powering down, the drive will become reset when either supply voltage drops below the V_{LT} threshold.

POR THRESHOLDS

DC	5V Combo		12V Combo	
Combo	(MAX)	(MIN)	(MAX)	(MIN)
V_{LT}	4.65V[1]	4.30V	9.70V[1]	8.40V
V_{HT}	4.70V	4.30V[1]	10.70V	8.40V[1]
Hyst	13 mV (TYP)		26 mV (TYP)	

Table 2-7. Power Reset Limits

Notes to Table 2-7 :

1. Includes a 100 mV Peak-Peak ripple on 5V or 250 mV Peak-Peak ripple on 12V to maximize or minimize values.

2.5 Environmental

2.5.1 Environmental Conditions

The drive will meet all of its operating performance specifications when operated within its operating environment and will sustain no damage or permanent performance degradations when subjected to the non-operating environment. Where applicable, SI units as well as American Standard units have been given.

Parameter	Operating	Non-operating
Temperature non-condensing	0°C to 55°C -32°F to 131°F	-40°C to 75°C -40°F to 167°F
Temperature Gradient non-condensing	24°C/hr. Maximum	48°C/hr. Maximum
Humidity[1] Max. Wet Bulb Temp.	5 to 85% RH 29°C 86°F	5 to 95% RH 46°C 114.8°F
Humidity Gradient	30% per hour	30% per hour
Altitude[2, 3]	-650 to 8,000 ft -200 to 2400 m	-650 to 40,000 ft -200 to 12000 m
Altitude Gradient	1.5kPa/min	8kPa/min
Shock[3]	10.0 Gs, 11mSec 1/2 sine	70 Gs, 11mSec 1/2 sine
Vibration[3] 1 octave/min	1 G P-P 5 - 500 Hz (X & Y axis) 1 G P-P 5 - 200 Hz (Z axis)	2 Gs P-P 5 - 500 Hz

Table 2-8. Environmental Specifications

Notes to Table 2-8:

1. Humidity: No condensation allowed. See Appendix for humidity charts for low and medium temperatures.

2. Altitude: relative to sea level.

3. NO Un-Recovered Errors.

2.5.2 Electromagnetic Conditions

2.5.2.1 EMI/RFI Susceptibility
4 volts/meter over a range of 20 Hz to 20 MHz.

2.5.2.2 Electrostatic Discharge
The drive shall mount inside the system with normal functional operation when subjected to electrostatic discharges, a minimum of 30 seconds apart from a 150 pF capacitor discharged through a 330 ohm resistor to exposed ten times to four different locations on the computer unit: two on the front and side and two on the back.

0 - 10 kV Average of <0.3 soft error per discharge

10 - 25 kV no catastrophic failures

2.5.2.3 Sensitivity to Magnetic Fields
The drives will meet all specifications with less than 6 gauss field applied in any orientation.

2.6 Mechanical

			Tolerance
Height	0.75 in	(19.05 mm)	±.02 in (.50 mm)
Length	8.0 in	(203.2 mm)	±.04 in (1.0 mm)
Width	5.75 in	(146.05 mm)	±.02 in (.50 mm)
Weight (lb)	2- Disk	1-Disk	
(without dampers)	1.64	1.55	±.20 lb
(with dampers)	2.25	2.16	±.20 lb
Spindle Motor	Integrated , Hall-Less		
Actuator	Rotary Flat Coil		
Mounting Holes	see Figure 2-4		
Mounting Position	Any		
Min Clearance to HDA	0.5 mm		
PCB Component height	4.57 mm (Both sides with restrictions)		
Shock Mounts	None		

2.7 Acoustics

This will be measured in an anechoic chamber, with background noise < 25 dbA.

2.7.1 Sound Power

	Measured Noise (with dampers)	Measured Noise (without dampers)
Idle on Track	3.9 bels[1] typical 4.2 bels max	4.1 bels typical 4.5 bels max
Seeking Random[2]	4.5 bels typical 4.8 bels max	4.6 bels typical 5.1 bels max

Table 2-9. Acoustical specifications.

Notes to Table 2-9:

1. ISO 7779 and 3745 specifies sound power in bels. The relationship between bels and dbA for sound power is 1 bel = 10dbA.
2. 43 ms latency between seeks is applied to random seek for acoustic measurement.

2.7.2 Sound Pressure

	Measured Noise (with dampers)	Measured Noise (without dampers)
Idle on Track	32 dbA typical 37 dbA max	35 dbA typical 1M 40 dbA max 1M
Seeking Random[1]	38 dbA typical 43 dbA max	42 dbA typical 1M 48 dbA max 1M

Table 2-10. Acoustical specifications.

Notes to Table 2-10

1. 46 ms latency between seeks is applied to random seek for acoustic measurement.

2.8 Reliability

MTBF[1] @ 55° C (Bellcore Issue #3)	**TBD POH**
MTBF[1] (Predicted Field)	**300,000 POH**
Component Life	**5** YEARS
Contact Start/Stops[2]	**20,000**

Table 2-11. Reliability specifications.

Notes to Table 2-11:

1. The Quantum MTBF numbers represent MTBF predictions per TR-TSY-000332 issue #3 Bell- Core,Sept.1990 and represent the minimum MTBF that Quantum or a customer would expect from the drive.

2. CSS specification assumes a duty cycle of 1 power off operation for every 4 idle mode spin down. Ambient temperature and humidity conditions apply to the CSS specification.

2.9 Hard Defects During Manufacture

During manufacturing and test, no drive will re-allocate more than 1block/2 Megabytes (on average), and a maximum of 500 blocks per surface.

2.10 AT Connector/Jumper

2.10.1 AT I/O DC 3 IN 1 POWER CONNECTOR

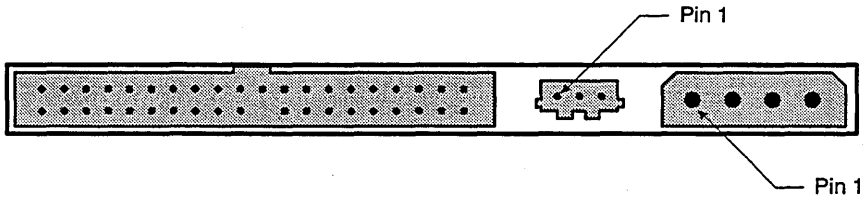

Figure 2-1. AT I/O DC 3 IN 1 Power Connector (J1).

Pin 1	+5.0V DC
Pin 2	+12.0 V DC
Pin 3	Ground

Table 2-12. 3 IN 1 3 Pin Power Connector pin assignments.

2.10.2 AT JUMPER

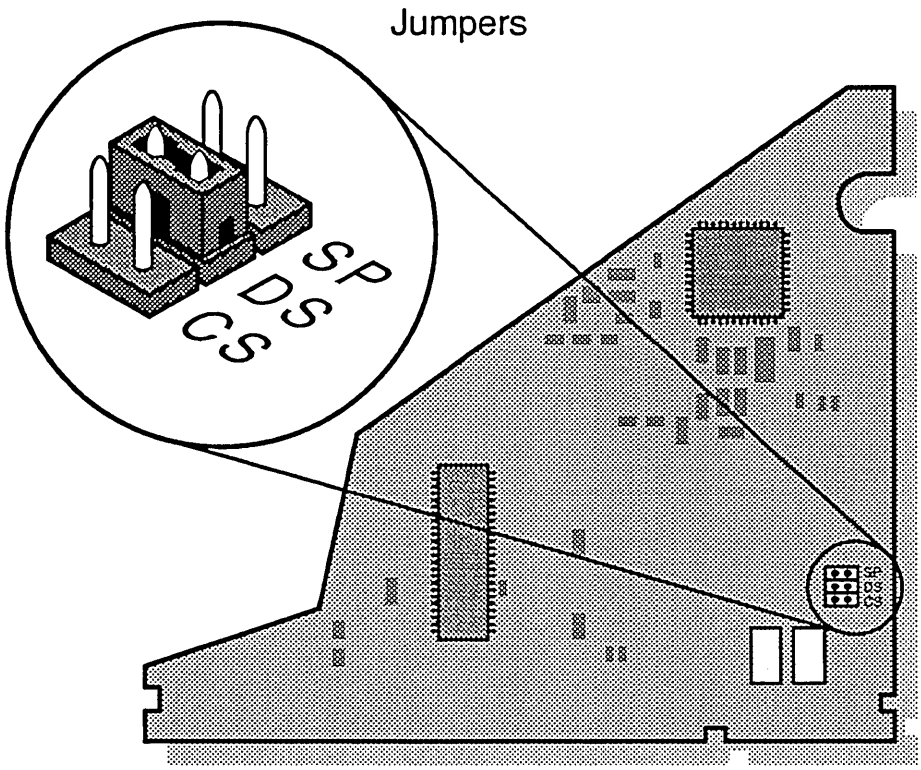

Figure 2-2. Jumper location on the AT PCB

CS	Cable Select
DS	Drive Select
SP	Slave Present

Table 2-13. AT Jumper Operational Mode

The AT PCB has three jumper locations provided for configuration options in a system. The three jumpers are CS, DS and the SP jumper. These three jumpers are used to configure the drive for master/slave operation in a system.
The default configuration for the drive as shipped from the factory is with a jumper across the DS location and open positions in the CS and SP positions.

The Following table defines the operation of the CS , DS and SP jumpers and their function relative to pin 28 on the interface.

CS	DS	SP	Pin28	Action
0	0	0	x	Drive Configured as a Slave.
0	0	1	x	Drive Configured as a Slave. SP position used as jumper parking position.
0	1	0	x	Drive Configured as Master
0	1	1	x	Drive Configured as Master. Non-CAM Slave Present
1	x	0	open	Drive Configured as Slave
1	x	0	gnd	Drive Configured as Master
1	x	1	gnd	Drive Configured as Master. Non-CAM Slave Present.

Table 2-14. AT Jumper Options

Note: 0 = jumper removed, 1= jumper installed, x = don't care.
Non-CAM slave present requires a second jumper which is not supplied with the drive, this feature is intended for Compaq only.

2.10.3 Cable Select (CS) Jumper

With the CS jumper installed, the drive uses pin 28 of the interface connector to determine whether it is a master or slave. If pin 28 of the interface connector is grounded the drive is configured as a Master. If pin 28 of the interface is not connected, an internal pullup drives the pin high and the drive will be configured as a Slave.

2.10.4 Drive Select (DS) Jumper

The default shipping configuration for the drive is to be used in systems that implement the drive select feature of the ATA specification.

For systems that do not support the cable select feature, setting a drive to master or slave requires the use of the DS jumper and removal of the CS jumper. If the DS jumper is installed the drive is configured as a Master. If the DS jumper is removed then the drive is configured as a Slave.

2.10.5 Slave Present (SP) Jumper

The purpose of the SP jumper is primarily to allow for non CAM/ATA handshaking for master slave operation. Normally the drive detects the presence of a slave by the -DASP line on the AT interface.

If the drive is a Master and a drive that does not use DASP for handshaking is used for a Slave, then installing a jumper at the SP location will indicate the presence of a Slave.

2.11 Connector and Jumper Location

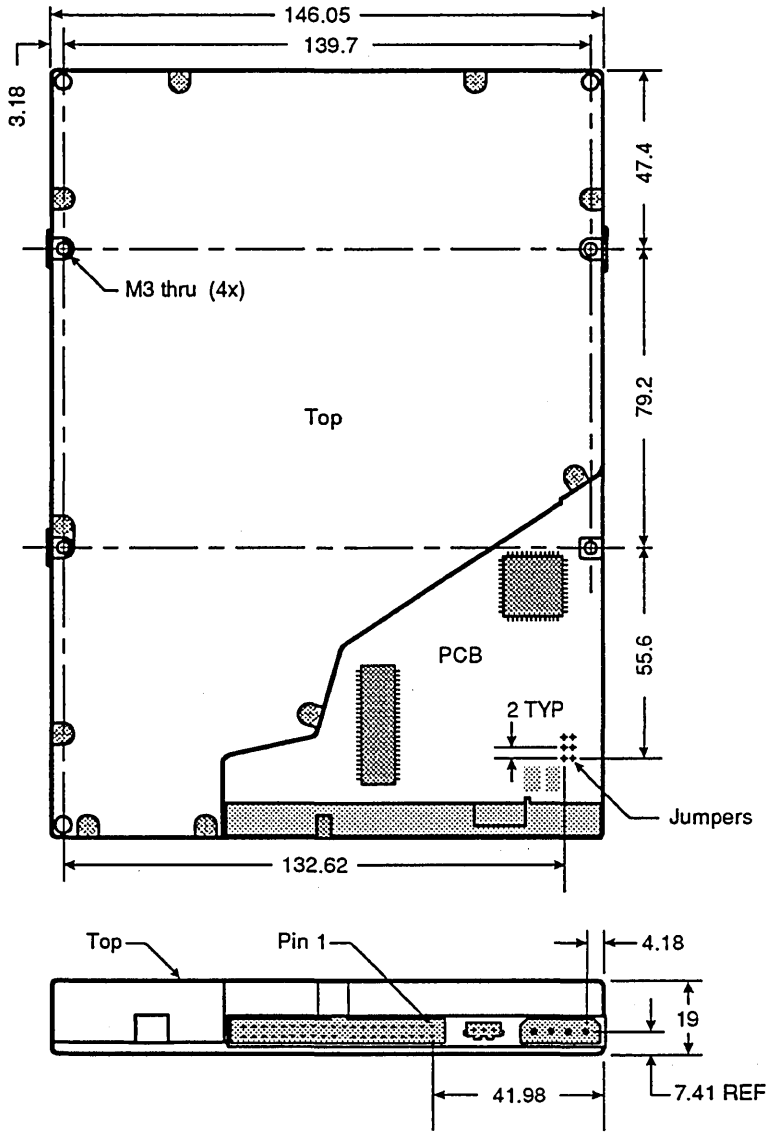

Figure 2-3. Connector and Jumper Location

2.12 Mounting

2.12.1 Orientation

Drive may be mounted in any orientation and nominal position is PCB face down.

2.12.2 Mounting

For mounting, M3 screws are recommended. To avoid stripping the mounting-hole threads, the maximum torque applied to the screws must not exceed 5 kg-cm.

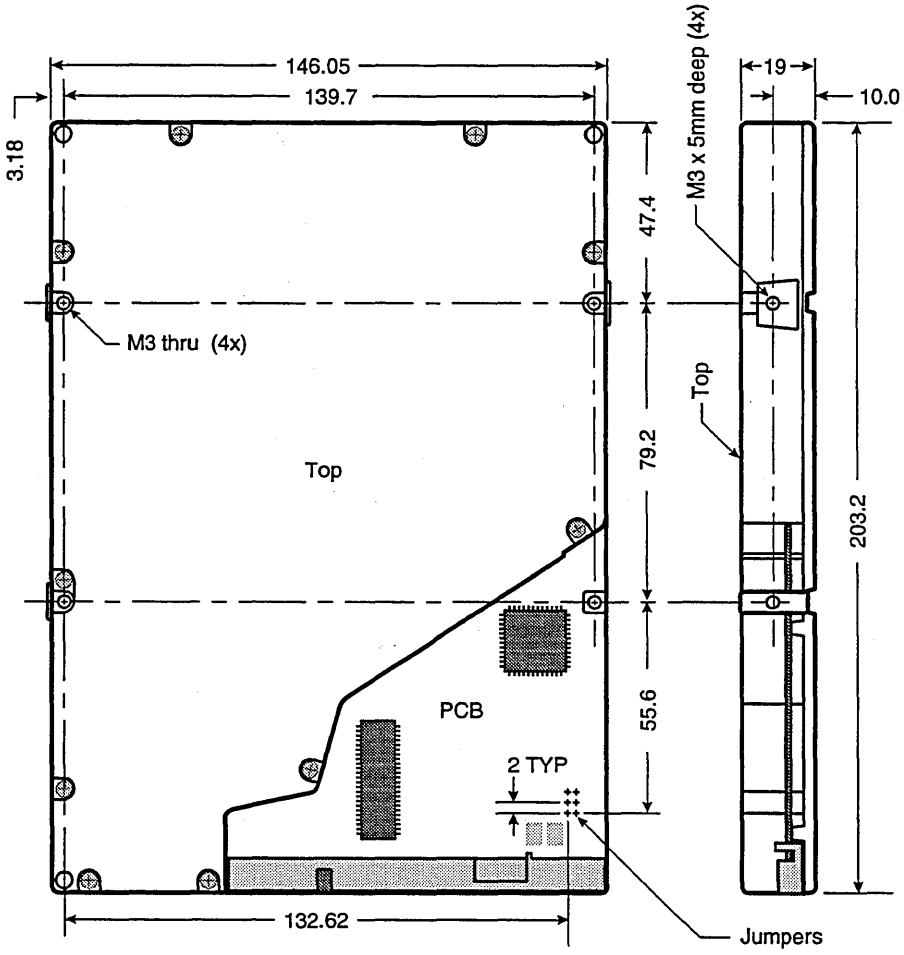

Figure 2-4. Mounting Dimensions

2.12.3 Clearance

Clearance from the drive to any other surface—except mounting surfaces—must be 1.25 millimeters (0.05 inches) minimum. Figure 2-5 specifies the clearance of the screws in the mounting holes. Do not use mounting screws longer than the maximum lengths specified in Figure 2-5. The specified screw length allows full use of the mounting-hole threads.

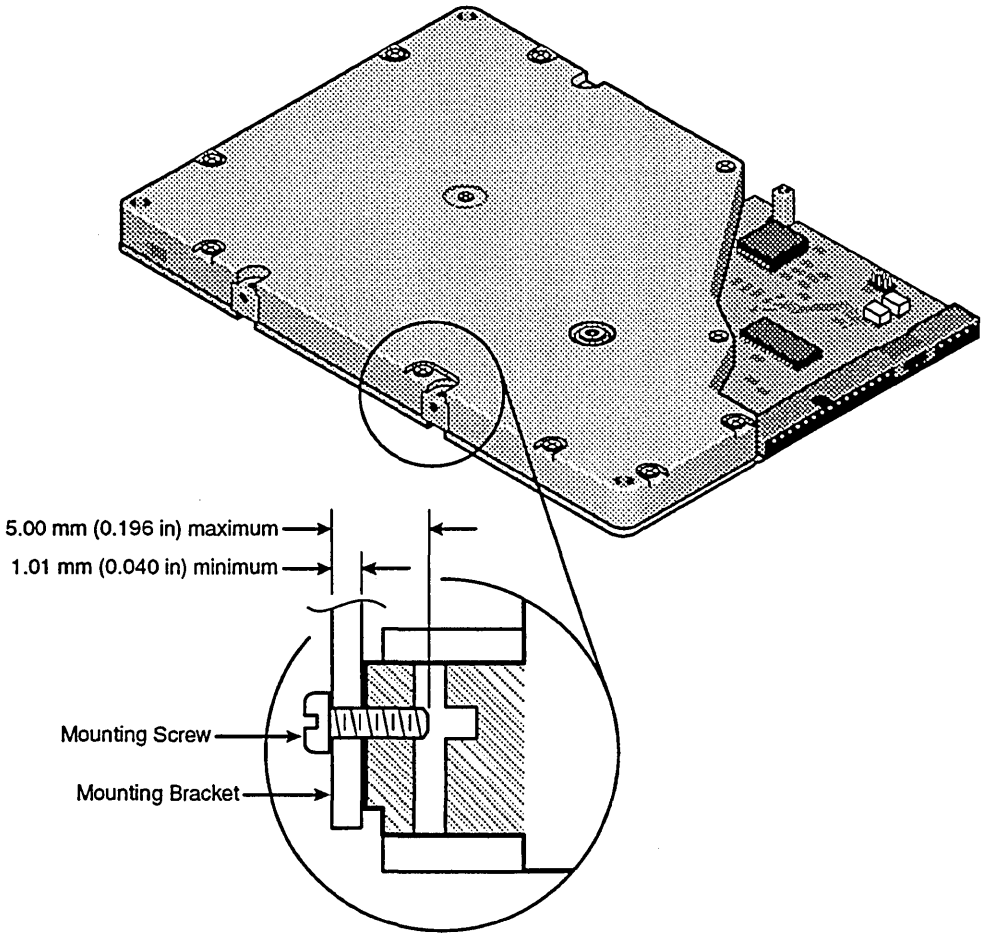

Figure 2-5. Drive Mounting Screw Clearance

Notes to Figure 2-5:

Do not exceed the specified length for the mounting screws. The screw length should allow full use of the mounting-hole threads. To avoid stripping the mounting-hole threads, the maximum torque applied to the screws must not exceed 5 kg-cm.

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Section 3 Track Specifications

The Vortex disk drives are shipped from the factory as "hard sectored" drives. That is, all physical sector addresses are written on the disks before the drives are shipped. As a result, sector size and number of sectors per track are not user selectable. The information given in this section is the physical format of Vortex as it is defined at the factory prior to shipment.

Note that the physical format is in contrast to the logical format of the drive, which is how the drive appears to the host system.

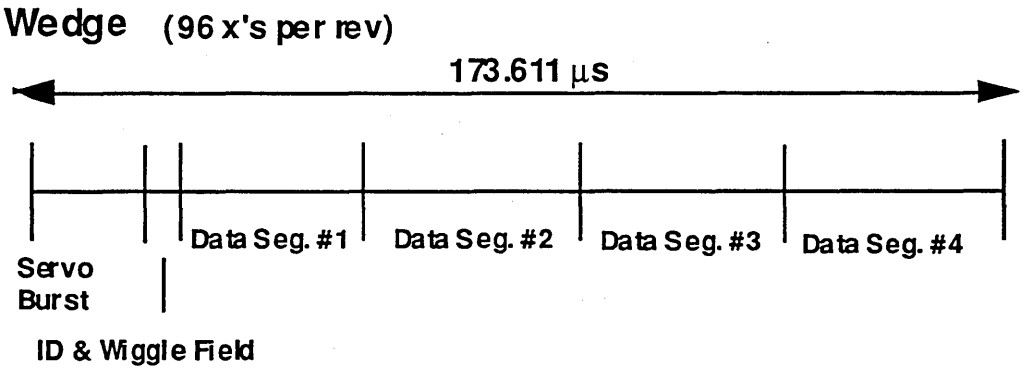
3.1 Track Locations

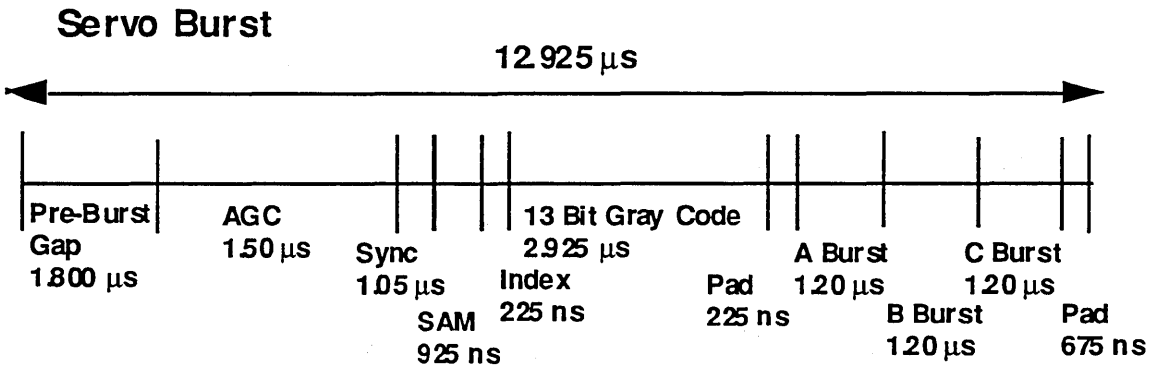
	Nom. Gap Centerline	Inside Corner of Slider	Inside ABS Rail	Outside ABS Rail
Disk edge radius	2.559			
Disk chamfer radius	2.553			
Compressed Outer crash stop radius	2.547	N/A	N/A	2.555
Touch Outer crash stop radius	2.488	N/A	N/A	
System data (Cyl -24)	2.502			
Zone 0 outside radius	2.468			
Zone 15 inside radius	1.147		1.092	
Landing zone radius (outer boundary)	1.129	N/A	N/A	1.142
Touch Inner crash stop radius	1.089	N/A	N/A	
Compressed Inner crash stop radius	1.030	0.649		
Disk spacer radius	0.886			
Pivot-to-spindle distance	3.152			
Pivot- to gap distance	2.908			
Pivot- to load point distance	2.876			

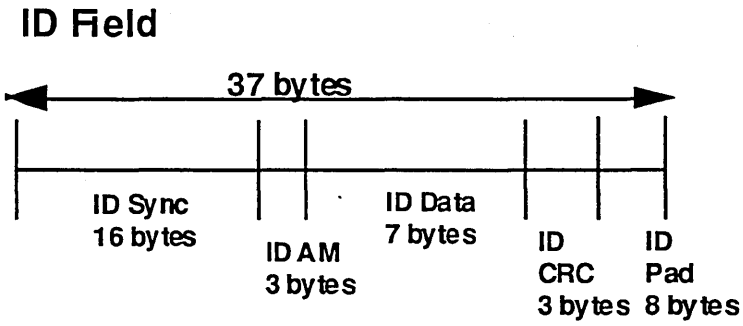
Table 3-1. Track Locations

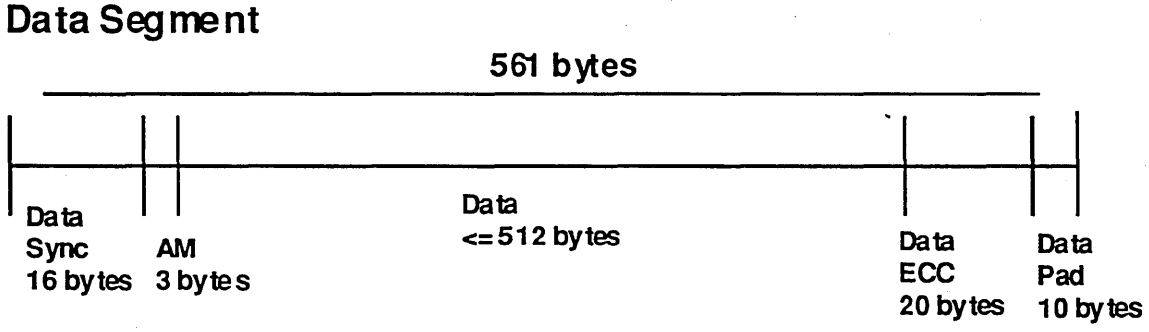
The actuator sweeps out an angle of 28.09°. from crash stop to crash stop.
The angle from the start of data to the end of data is 26.95°.

3.2 Track Format









Vortex Track Layout and Frequency Chart (16,17)PRML

Zone	# of cyl	Max. FCI	DataRate Mb/s	VCO MHz	Fmax MHz	Tcell nS	Synthesizer Feedback	Synthesizer Prescaler
System	24	65763	57.58	61.33	30.67	16.30	92	15
1	383	99402	83.76	89.17	44.58	11.21	107	12
2	383	103270	83.22	89.17	44.58	11.21	107	12
3	383	104910	82.57	87.06	43.53	11.49	148	17
4	383	106053	79.33	84.44	42.22	11.84	152	18
5	383	107177	77.18	81.74	40.87	12.23	188	23
6	383	108016	74.40	78.75	39.38	12.70	126	16
7	383	108394	71.61	75.38	37.69	13.27	98	13
8	383	109357	68.83	72.38	36.19	13.82	152	21
9	382	110175	65.43	69.23	34.62	14.44	90	13
10	382	111096	62.42	66.09	33.04	15.13	152	23
11	382	109259	57.58	61.33	30.67	16.30	92	15
12	382	111864	56.47	59.05	29.52	16.94	124	21
13	382	113043	53.34	55.88	27.94	17.89	95	17
14	382	113922	49.27	52.50	26.25	19.05	105	20
15	382	110846	46.48	47.37	23.68	21.11	79	19

Table 3-2 Zone Specifications

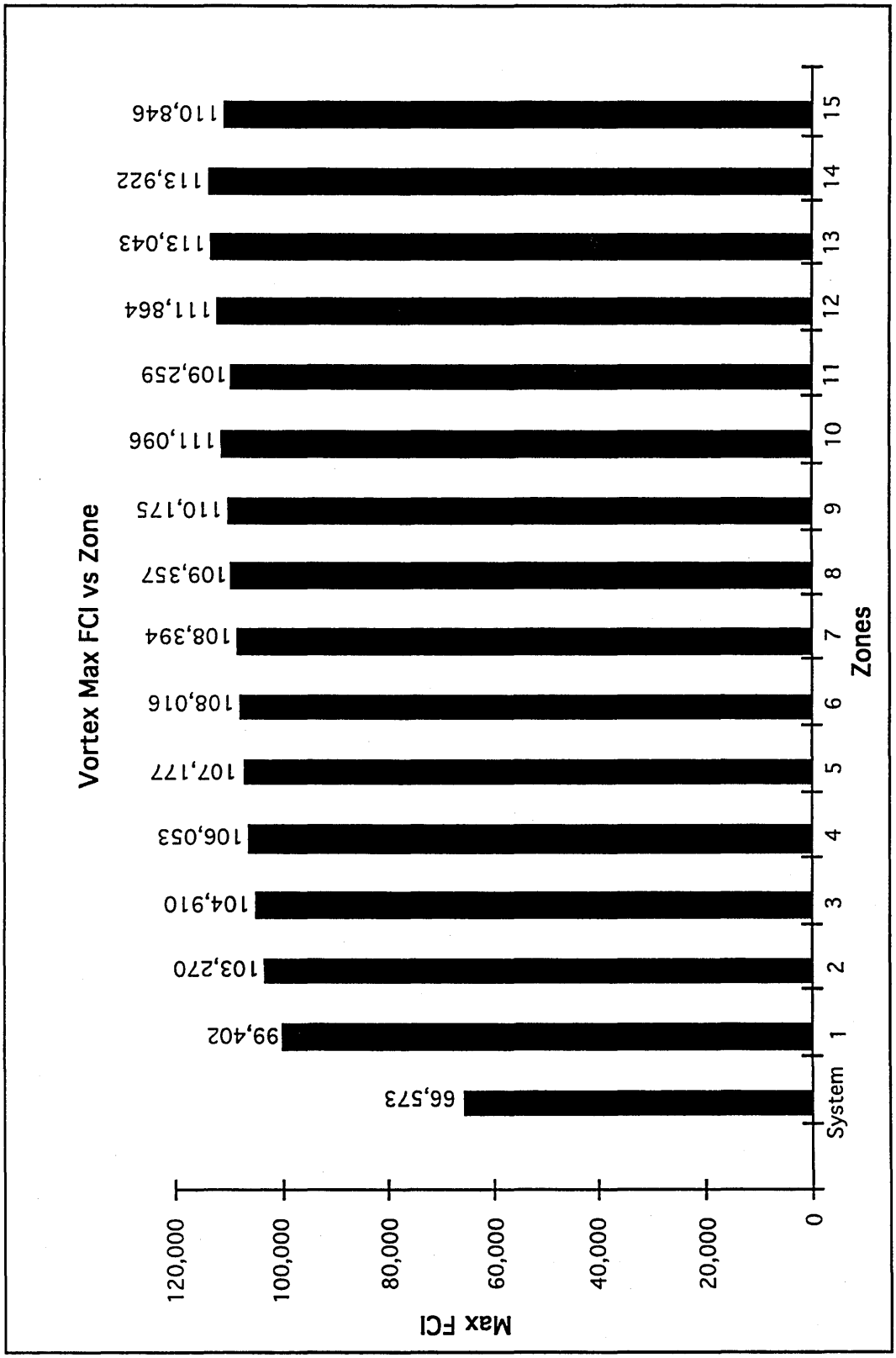


Figure 3-1. FCI vs Zone

3.3 Cylinder Contents

Cylinder Contents	Zone	Cylinder Range	Date Rate Mb/S	Sectors Per Track
Servo Inner G.B	15	5704 - 5705	N/A	N/A
S/W Info.	15	5699 - 5703	N/A	N/A
S/W Serial Number	15	5693 - 5698	N/A	N/A
Servo Inner G.B	15	5689 - 5692	N/A	N/A
Servo Test 3X Sample Rate	15	5685 - 5688	N/A	N/A
Servo Inner G.B	15	5669 - 5684	N/A	N/A
User Data	15	5292 - 5669	46.48	149
	14	4914 - 5291	49.27	160
	13	4536 - 4913	53.34	172
	12	4158 - 4535	56.47	183
	11	3780 - 4157	57.58	192
	10	3402 - 3779	62.42	204
	9	3024 - 3401	65.43	214
	8	2646 - 3023	68.83	225
	7	2268- 2645	71.61	235
	6	1890- 2267	74.40	245
	5	1512- 1889	77.18	256
	4	1134- 1511	79.33	261
	3	756- 1133	82.57	273
	2	378 - 755	83.22	276
	1	0- 377	83.76	276
Test Equip. Data Error logging	System	-1	57.58	192
System	System	-2	57.58	192
Copy of cylinder -2	System	-3	57.58	192
Diskware	System	-4	57.58	192
Copy of cylinder -4	System	-5	57.58	192
Compressed Test Data	System	-6	57.58	192
Records Data	System	-7	57.58	192
Servo Outer G.B	System	-8 to -16	N/A	N/A
Servo Test 3X Sample Rate	System	-17 to -24	N/A	N/A

Table 3-3. Cylinder contents breakdown.

Notes to Table 3-3:

1. Zone 1 is the outermost zone, zone 15 is the innermost zone.

2. Seven cylinders on all drives are reserved for system, Diskware and test usage. These cylinders contain drive configuration information, drive test information, and diskware. Customers cannot access these reserved cylinders. The reserved cylinders are only accessible with physical address commands which are protected diagnostic commands.

3. Data is repeated on cyl -2 and cyl -3, also repeated on cyl -4 and cyl -5, and is stored in the OD system areas for redundancy. Data is read from and written to these areas according to the firmware redundancy algorithm.

4. The test equipment/error logging cylinder (-1) is reserved for test equipment usage. This cylinder contains test parameters and data collected during production test. Writing on this cylinder may erase some important information and cause the drive to be rejected and sent back to the servo writer station.
   The sector usage is as follows and may be subject to change:

Sector	Usage
0	Copy of Servo writer Serial Number Data.
1	Test Process Interlock
2	Reserved .. for Reclassification .. NA on AD1
3	Configuration Center Control.
4	Reserved .. for Expansion.
5 - 14	Test Process History Queue.
15 - 30	Process Test Defect List.
31	Not Used
32 - 39	Self Scan results (8).
40	Not Used
41 - 48	Self Scan test parameters (8).
49 - 51	Not Used
52 - 75	Self Scan defect list (24).
76	Servo defect map (1).
77 - 78	Not Used
79	Soft error table (1).
80 - 81	Not Used
82 - 85	Runout Results (4)
86 - 99	Not Used
100 - 101	CSS Test Error Log
102 - 131	Not Used
132	Selfscan Variables Save/Restore (1)
133 - 137	Not Used
138 - 139	Performance Test Results (2)
140 - 159	Adaptive Results (2).
160 - 175	Not Used
176 - 191	Reserved for in-line defect sparing.

5. The System cylinder (-2) is reserved for system usage. It contains mode page information, configuration information, defect lists, and format information for the drive. Writing on this cylinder may erase some important information and prohibit the drive from operating. The data is repeated on cyl -3. The sector usage is as follows:

Sector	Usage
0	Saved mode pages.
1 - 8	Configuration pages.
9 - 24	Working defect list .
25 - 40	Primary defect list .
57 - 75	Format header bytes - zone 0-15.
75	Servo Defect list
76 - 92	Error log (detail log)
76 - 77	Recal Record
106 - 107	S.M.A.R.T Attributes/Variables/Thresholds
176 - 191	Reserved for in-line defect sparing.

6. The Diskware cylinder (-4) is reserved for Diskware usage. The data is repeated on cyl -5. The sector usage is as follows:

Sector	Usage
0 - 47	Diskware 24K segment.
48 - 112	Overlays
176 - 191	Reserved for in-line defect sparing.

7. The -6 Cylinder contains compressed test.out file.

0 - 268	Test.out files
176 - 191	Reserved for in-line defect sparing.

3.4 Track and Cylinder Skewing

Head Switch Time Worst Case 5.0 ms
RPM 3600

ZONE NUMBER	NUMBER OF CYL	NUMBER OF SECT	HEAD SKEW	CYL SKEW
1	378	276	98	115
2	378	276	97	115
3	378	273	94	111
4	378	261	91	107
5	378	256	87	103
6	378	245	85	100
7	378	235	81	96
8	378	225	78	92
9	378	214	75	88
10	378	204	71	83
11	378	192	68	80
12	378	183	64	75
13	378	172	60	71
14	378	160	57	67
15	378	149	53	62

Assumptions made:

1. All skew numbers with tenth digit ≥ 0.01 were rounded up to the next integer.

2. Worst case RPM was used to give a slightly larger safety margin.

Since the Vortex drives are storage subsystems with integrated controllers, the function and design of the controller can be optimized specifically for the drive. One method of optimization employed by Quantum to improve data throughput is skewing sector addresses. The purpose of track and cylinder skewing is to minimize latency time and thus increase data throughput when data is sequentially accessed to or from the disk. The two types of skewing employed, track and cylinder skewing, are described below.

3.4.1 Track Skewing

Track skewing reduces latency time which results when the drive must switch read/write heads to access sequential data. A track skew is employed such that the next logical sector of data to be accessed will be under the read/write head once the head switch is made and data is ready to be accessed. Since head switch times are defined on VORTEX, the sector addresses can be optimally positioned across track boundaries to minimize the latency time which results when a head switch has to be performed.

3.4.2 Cylinder Skewing

Cylinder skewing is also used on Vortex to minimize latency time during sequential accessing of data. However, instead of minimizing latency time due to head switching, as with track skewing, cylinder skewing is used to minimize latency time due to a single-cylinder seek. The next logical sector of data which crosses a cylinder boundary is positioned on the drive such that after a single-cylinder seek is performed, and the drive is ready to continue accessing data, the sector to be accessed is positioned directly under the read/write head. Therefore, the cylinder skew takes place between the last sector of data on the last head at a cylinder and the first sector of data on the first head at the next cylinder. Since single-cylinder seek times are defined on the drive, the sector addresses can be optimally positioned across cylinder boundaries to minimize the latency time which results when a seek has to be performed.

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Section 4 Mechanical

4.1 Motor

This specification along with its associated documents defines the electrical and mechanical requirements for a 5.25" Hard Disk Drive spindle motor to be used in the VORTEX 2-disk product. The motor is intended to be a fixed-shaft, integral to base design.

4.1.1 Reference Documents

Base Motor Assembly	75-110002-01 (2 Disk) 75-110002-01 (1 Disk)
Disk 130mm X 40mm X 1.27mm	61-109962-01
Disk Clamp	40-109959-01 (2 Disk) TBD (1 Disk)
Disk Spacer	40-109961-01 (2 Disk)
Cover (machined)	40-110007-01
Spindle Motor Driver	TBD

Table 4-1. Reference documents for spindle motor

4.1.2 General Specifications

Number of Poles	12
Number of Phases	3
Motor Type	Brushless DC
Driving Mode	BiPolar Y, with center tap
Commutation	Back- emf (Hall-less)
Number of Stator Slots	9
Mounting Orientation	Any Orientation
Flex Circuit Pin Descriptions	
Pin 1	u
Pin 2	v
Pin 3	w
Pin 4	center tap

Table 4-2. General specifications for spindle motor

4.1.3 Operating Parameters

Rotational Speed	3600 RPM ± 0.5%
Direction of Rotation (hub side view)	Counterclockwise
Inertia Load	
2 Disk, clamp, spacer, 6 screws	TBD gm-cm^2
1 Disk, clamp, spacer, 6 screws	TBD gm-cm^2
Frictional Load (Max.)	
Static Load	16.0 gm-cm pk
Dynamic Load	28.0 gm-cm
Spin Up Time @ 25°C 12 Volt	< 9 sec

Table 4-3. Performance specifications for spindle motor

4.1.4 Mechanical Characteristics

Bearing Type	Single shielded NMB		
Bearing Size	5 mm X 13mm X 3mm		
Bearing PreLoad	2.0 Kg		
Lubrication	SRL Multemp		
Torque Constant	195.9+/-7.5%gm-cm/A pk		
Starting Torque[1]	110 gm - cm (min)		
Running Torque @ 3600 RPM	31.7 gm - cm (min)		
Repetitive Run-out (RRO) @3600 RPM Max.	Radial	393 u"(10 um)	
	Axial	590 u"(15 um)	
Non-Repetitive Run-out (NRRO)[2] Max.	Radial	13.8 u"(.35 um)	p - p
0 Hz - 50 Hz	4 u"	(0.10 um)	0-p
50 Hz - 100 Hz	2 u"	(0.05 um)	0-p
100 Hz - 200 Hz	1.5 u"	(0.038 um)	0-p
>200 Hz	1 u"	(0.025 um)	0-p
Imbalance	< 0.07 gm-cm		
Acoustic noise[3]	< 4.2 bel @ 1 m 3.9 bel Typ.		
Resonances (lower dynamic rocking mode)	230 Hz or higher		
Seal Type[4]	Labyrinth Seal above top brg		

Table 4-4. Mechanical specifications for spindle motor

Notes to Table 4-4:

1. Minimum torque is in addition to static frictional load and is measured with 850 mA supplied to the motor, in any rotor position, throughout environmental temperature range.

2. This value must reflect the average max radial NRRO plus (+) 3 standard deviations for any given population sample greater than (>) 50 motors.

3. With no prominent discreet tones. Prominent tones defined as frequency bands (1/3 octave bands) which have a db level higher than average of the two adjacent bands by 5 db. Noise to be measured in semi-anechoic chamber with disk stack and cover installed.

4. Seal must withstand 100 mm of H_2O (internal or external pressure, while rotating) without fluid leaking.

4.1.5 Electrical Characteristics

Supply Voltage Requirements	12 V (DC) ± 10%
Minimum Motor Voltage	10.5 V (DC)
Coil Resistance	9.18 Ω @ 24°C
Coil Inductance (Max.)	< 2.0 mH
Voltage Constant	0.0192 V-s /radian @ 24°C
BEMF at 24°C and 3600 RPM	7.24V +/- 7.5% (0-P)
Running Current[1]	<210 mA
Starting Current	1.3 Amp
Magnetic Flux Leakage[2]	< 5 Gauss 0-P
Spin Up Time	< 9 sec
Insulation resistance	50 MΩ (min)
Breakdown voltage	AC 250V for 1 sec

Table 4-5. Electrical specifications for spindle motor

Notes to Table 4-5:

1. Measured with disk stack and cover assembled after 15 sec. run - in.

2. Measured in any orientation at a radius of 25 mm from center of motor hub @ 3600 RPM.

4.1.6 Materials

Hub Thermal Expansion	Aluminum A2011/A6061 22.9X10E-6/°C (0°C-100°C)
Magnets	Neodymium sintered, or Neodymium plastic-bonded/encapsulated
Shaft	SUS (420J2,420F,430f,416)

4.1.7 Environment

	Operating	Non-Operating	Storage
Temperature	0°C to 55°C -32°F to 131°F	-40°C to 75°C -40°F to 167F	-40°C to 75°C -40°F to 167°F
Humidity[1] Max wet bulb	5% to 85% RH 29°C 86°F	5% to 95% RH 46°C 114.8°F	
Altitude	-650 to 8,000 ft -200 to 2400 m	-650 to 40,000 ft -200 to 12,000 m	
Shock[2]	10 G 11 ms 1/2 sine	70 G 11 ms 1/2 sine	
Vibration [3]	1 G 5-500 Hz (p-p) (X & Y axis) 1 G 5-200 Hz (p-p) (Z axis)	2 G 5-500 Hz (p-p)	

Table 4-6. Environment specifications for spindle motor

Notes to Table 4-6:

1. No condensation allowed.
2. Half sine wave shock in 3 mutually perpendicular axes; 3 shocks for each axis.
3. Sine Sweep 1 octave/minute on 3 mutually perpendicular axis.

4.1.8 Quality Assurance Provisions

4.1.8.1 Identification
All motors carry a manufacturer identification, a revision level and manufacturing date code on the base side.

4.1.8.2 Burn In
All motors shall be "burnt in" at 75° C for 4 hours (motor not running).

4.1.8.3 Reliability
The L1 life is to be 40,000 power on hours at 60° C, 80%RH.

4.1.9 Cleanliness

4.1.9.1 Cleanliness of Assembly Area
The motor shall be assembled and sealed in an individual bag in a Class 100 cleanliness area. The assembly area must be maintained for the specified cleanliness.

4.1.9.2 Particles from the Motor
Under running conditions, the motor must support the Class 100 cleanliness environment when measured one minute after start-up.

Particulate generation allowable per cubic foot of air when operating at 5401.9 rpm:

< 10 particles > 0.5 micron

< 38 particles > 0.3 micron

< 380 particles > 0.1 micron

4.1.9.3 Visual Inspection
The motor shall be free of dirt, chips and other foreign materials.

4.1.10 Packaging

The motor must be packaged so that it can withstand a drop of 90cm onto a concrete floor without performance degradation.

4.1.11 UL, CSA TUV and VDE Requirements

4.1.11.1 Components and Materials
All parts, components and materials must meet or exceed the minimum requirements for UL, CSA, TUV and VDE as required for electronic equipment

4.1.11.2 Vendors
If required in order to obtain certification for the complete motor assembly, any parts, materials and components (including printed circuit boards) must be manufactured by vendors approved by UL, CSA TUV and VDE.

4.1.11.3 Certification Cards
UL, CSA TUV and VDE certification cards for affected parts and materials are required for initial qualification and changes.

4.2 VCM

The Vortex VCM design utilizes a 'side plate configuration' Side plates essentially are extensions of the upper magnet plate which provide an additional return path around the sides of the VCM. With this additional return path the thickness of the steel can be reduced in the upper and lower magplate allowing the packaging of a greater amount of magnet material in a given vertical space.

4.2.1 Specifications

Torque constant	1103 g-cm/Amp
Flux in gap	5600K Gauss p - p
Magnet material	Sumitomo Neomax 40BH
Coil resistance	11.28Ω ± 0.5Ω @ 20°C
Moment of Inertia	130 gm-cm^2 (2 Disk)
	120 gm-cm^2 (1 Disk)

4.3 Actuator

The actuator will utilize some type of constant fly height sliders.

4.4 Airlock

The Vortex HDA will use an airlock design similar to TrailBlazer. A small steel ball is placed on the "Locking Arm" part of the Airlock. The ball is attracted to the VCM magnet, hence closing the airlock.

4.5 Crash Stops

The Vortex will utilize the traditional rubber stop at the arm for ID stop and encapsulation for OD stop.

4.6 FPCB

The FPCB uses the short loop design like TrailBlazer , Uzi and Daytona design. By placing the preamp close to the heads an improvement in the R/W signal to noise ratio is expected.

4.7 Basecasting/Top cover

Both basecasting and top cover will be made of die cast aluminum material to preserve the rigidity needed for the short Z- Height.

Section 5 Heads/Media

5.1 Heads/Media General Requirements

Operating Environment

Temperature	0° to 55° C (-32° to 131° F)
Maximum Temperature Gradient	24° C/hr (75.2° F/hr)
Humidity	5 to 85% RH, non-condensing
Maximum Wet-Bulb Temperature	29° C (86° F)
Altitude	-200 to 2100 m (-650 to 8,000 ft)
Cleanliness	Class 100
Stray Magnetic Field	< 25 Oe

Shipping and Storage Environment

Temperature	-40° to 75° C (-40° to 167° F)
Maximum Temperature Gradient	48° C/hr (118.4° F/hr)
Humidity	5 to 95% RH, non-condensing
Maximum Wet-Bulb Temperature	46° C (114.8° F)
Altitude	-200 to 12,000m (-650 to 40,000 ft)
Cleanliness	Class 100
Stray Magnetic Field	< 50 Oe

Test Environment

Temperature	23 ± 3° C (73 ± 5° F)
Humidity	30 to 70% RH, non-condensing
Altitude	0 to 914 m (0 to 3,000 ft)
Cleanliness	Class 100
Rotational speed	3600 ± 36 rpm
Stray Magnetic Field	< 6.25 Oe

Stiction/friction testing will be performed under the Operating environmental conditions.

Zone Descriptions of Head/Disk Test

Zone Radii

The applicable zone radii, shown in the table below are referenced to the gap of the transducer.

Radius	mm	in.	Zone description	Skew at CG	Skew at Gap
R1	20.00	0.787	Disk ID		
R2	27.310	1.0752	Loading Zone ID	-3.433	-1.222
R3	29.134	1.1470	Recording Zone - Z 16 (ID)	-1.778	0.263
R4	29.192	1.1493	Recording Zone - Z 15 (ID)	-1.727	0.309
R5	31.425	1.2372	Recording Zone - Z 14 (ID)	0.148	2.005
R6	33.660	1.3252	Recording Zone - Z 13 (ID)	1.895	3.597
R7	35.893	1.4131	Recording Zone - Z 12 (ID)	3.536	5.103
R8	38.128	1.5011	Recording Zone - Z 11 (ID)	5.094	6.541
R9	40.361	1.5890	Recording Zone - Z 10 (ID)	6.581	7.922
R10	42.596	1. 6770	Recording Zone - Z 9 (ID)	8.011	9.259
R11	44.828	1.7649	Recording Zone - Z 8 (ID)	9.393	10.555
R12	47.064	1.8529	Recording Zone - Z 7 (ID)	10.735	11.820
R13	49.296	1.9408	Recording Zone - Z 6(ID)	12.043	13.058
R14	51.532	2.0288	Recording Zone - Z 5 (ID)	13.323	14.275
R15	53.764	2.1167	Recording Zone - Z 4 (ID)	14.579	15.471
R16	55.999	2.2047	Recording Zone - Z 3 (ID)	15.816	16.654
R17	58.232	2.2926	Recording Zone - Z 2 (ID)	17.035	17.823
R18	60.647	2.3806	Recording Zone - Z 2 (ID)	18.242	18.984
R19	62.700	2.4685	Recording Zone - Z 1 (ID)	19.437	20.135
R20	62.837	2.4739	Recording Zone - Z 0 (OD)	19.510	20.206

Media Magnetic Requirements (Reference only)

Magnetic Material	CoCrTa , CoCrPt, CoCrTaPt or CoNiCrPt
Coercivity	1950 ± 100 Oe (Ref)
Remanence - Thickness Product	0.0023 emu/cm^2 ±0.000125 emu/cm^2
Squareness (Br/Bs)	≥ 0.8

5.2 Heads Mechanical Requirements

5.2.1 Slider Specifications

Transducer, Pole Tip Area, Face View

Primary Pole Width	4.8 ± 0.50 µm	(197 ± 19.7 µin)
Primary Pole Thickness	3.5 ± 0.35 µm	(138 ± 13.8 µin)
Secondary Pole Width	4.8 ± 0.50 µm	(197 ± 19.7 µin)
Secondary Pole Thickness	3.5 ± 0.3 5µm	(138 ± 13.8 µin)
Gap	0.25 ± 0.05 µm	(9.45 ± 1.9 µin)
Pole Inset	≥ 0 and ≤ 1.5 µm	(≥ 0 and ≤ 59 µin)
Pole Wraparound	None permitted	
Undercoat Thickness	≥ 10 µm (Ref)	(≥ 394 µin)
Overcoat Thickness (above the top pole)	≥ 8 µm (Ref)	(≥ 315 µin)

Transducer, Pole Tip Area, Profile View

Pole Tip Recession	≤ 10 nm (Ref)	(≤ 0.4 µin)
Pole Tip Protrusion	None allowed	

Turns	42
Leads	2

Slider Dimensions

Length	2.000 ± 0.025 mm	(0.0787 ± 0.001 in)
Width	1.575 ± 0.025 mm	(0.0620 ± 0.001 in)
Thickness	0.425 ± 0.028 mm	(0.0167 ± 0.0011 in)

ABS Rails (TPC Design)

Width	292 ± 10 µm (Ref)	(0.0115 ± 0.0004 in)
Taper Angle	30 ± 10 minutes	
Taper Length	305 ± 50 µm	(0.012 ± 0.002 in)
Bleed Slot Depth	≥ 20 µm (Ref)	(≥ 0.0007 in)
Bleed Slot Width	≥ 300 µm (Ref)	(≥ 0.0118 in)
Surface Finish	≤ 13 nm	(≤ 0.5 µin)
Crown (TPC) HGA level (NPAB)	20 nm Min TBD	(0.80 µin Min)
Camber	1 ± 6 nm	(0.04 ± 0.24 µin)
Flatness	≤ 20 nm	(≤ 0.8 µin)

ABS Blend (Reference Only)

Side edge width	7.1 ± 3.6 µm	(280 ± 140 µin)
Side edge rolloff	0.25 ± 0.13 µm	(10 ± 5 µin)
Trailing edge width	7.1 ± 3.6 µm	(280 ± 140 µin)
Trailing edge rolloff	0.25 ± 0.13 µm	(10 ± 5 µin)
Corner width	36 ± 18 µm	(1400 ± 700 µin)
Corner rolloff	0.40 ± 0.20 µm	(16 ± 8 µin)

5.2.2 Head Load Force

Preload in nominal flying position 0.049 ± 0.005 N (5.0 ± 0.5 grams force)

5.2.3 Z-Height

The z-height is to be 0.7366 mm (0.029 in)

5.2.4 Flying Height

Innermost Track
With the transducer at radius R4, the disk rotating at 3600 rpm, and a skew angle of -0.57 degree at the gap, the following flying characteristics shall be achieved:

Minimum transducer rail clearance	44.5 nm	(1.75 µin)
Suggested mean transducer rail clearance	57.2 nm	(2.25 µin)
Slider roll, trailing edges	0 ± 50.8 nm	(0 ± 2.0 µin)
Slider pitch, both rails	180 ± 101 nm	(7 ± 4 µin)

Note: The mean transducer rail clearance shall be at least 3.0 sigma greater than the minimum transducer rail clearance and shall be sufficiently low such that all dynamic electrical specifications are met. See POS where appropriate.

Outermost Track
With the transducer at radius R19, the disk rotating at 3600 rpm, and a skew angle of 18.7 degree at the gap, the following flying characteristics shall be achieved:

Minimum transducer rail clearance	44.5 nm	(1.75 µin)
Suggested mean transducer rail clearance	57.2 nm	(2.25 µin)
Slider roll, trailing edges	0± 50.8 nm	(0 ± 2.0 µin)
Slider pitch, both rails	457 nm	(18 µin) Max

Note: The mean transducer rail clearance shall be at least 3.0 sigma greater than the minimum transducer rail clearance and shall be sufficiently low such that all dynamic electrical specifications are met. See POS where appropriate.

Minimum Flying Height (at sea level)
The minimum flying height of any point on either rail shall always exceed 44.45 nm (1.75 µin) at any disk radius in the Flyable Zone.

Maximum Flying Height (at sea level)
The flying height at the transducer shall never exceed 69.9 nm (2.75 µin)(REF) at any disk radius in the Flyable Zone.

Flight-height measurements taken with equipment based on a Photo Research flying height transducer (or equivalent), with a spot size not to exceed 60 µm (0.0024 in),are acceptable when calibrated by a method and schedule approved by the equipment manufacturer.

5.2.5 Suspension

5.2.5.1 Suspension Configuration

Suspension is a Type 850, upfacing rail, semi tubeless design with 12 mil crimp tabs at the base.

Detailed definition is found in the following :

	Part#	Name	Boss Type	Actuator Position
HTI	0109763 or Quantum Approved Equivalent	850 LSF Through etch	Low Profile Swage	Up facing
HTI	0109759 or Quantum Approved Equivalent	850 LSF Through etch	Low Profile Swage	Dn facing
NHK	FA0849L000 or Quantum Approved Equivalent	T850	Low Profile Swage	Up facing
NHK	FA0849R000 or Quantum Approved Equivalent	T850	Low Profile Swage	Dn facing

5.2.5.2 · HGA Resonance Specifications

The resonances performance of the HGA is to meet or exceed the following specifications when measured at the Z-height noted, using the Phase Metrics HRT - 1 Resonance Tester or suitable equivalent qualified by Quantum Head-Media Engineering.

Mode Vibration	Minimum Freq.	Maximum Freq.	HGA Gain Upper Spec. Limit	Z-height for Measurement
First Torsion	2500 Hz	2900 Hz	12 dB	0.019 inch
First Torsion	2500 Hz	2900 Hz	12 dB	0.039 inch

5.2.5.3 Suspension Resonance Specification

Resonance performance specification and control of the suspensions and its components is the responsibility of the HGA vendor. Suitable margin should be allowed to account for handling effects during HGA assembly.

5.2.5.4 Suspension Supplier Qualification

Head suppliers must qualify any and all suspension suppliers prior to commencement of mass production. The requirements for this qualification are specified in the Proc. Suspension Qualification, Quantum Document No. 84-106741-01. Suspension qualification should be done during Quantum P1 build for existing suspension designs, and during P2 for new suspension designs. Suspensions used in the qualification tests must be produced from production- level tooling.

5.2.6 Bond Strength

Slider - to -Flexure
The slider - to - flexure bond strength, when measured by a shear test shall be ≥ 150 gm.

Wire - to - Bond Pad
The single-wire wire-to-bond-pad bond strength, when measured by a pull test (before conformal coat applied) at 30° from the bond-pad plane, shall be ≥ 8 gm.

5.2.7 Slider Material

Aluminum Oxide Titanium Carbide

5.2.8 Wire and Tubing

Tubing to be made of Teflon. The color shall be : Unique for each supplier.
Wire colors shall be red and green. Wire type to be gold plated copper alloy with double -layer polyethylene coating.
Wire twist shall be 25 ± 3 turns/inch. The local variation, anywhere over the length, shall not exceed the average variation by more than 10%.

The wire insulation shall withstand temperatures up to 343 °C (650 °F) with no change in physical properties.

The wire insulation shall withstand wire tinning temperatures up to TBD °C (TBD °F).

The wire insulation shall not generate static electricity at the low temperatures of the operating, shipping, and storage conditions of Secs. 5.1.

The wire gage shall be 44, 47 or 48.

The wire shall withstand a pull test of 10 grams.

5.2.9 Durability of the Slider

Start/Stop Test

Procedure:
The test shall be performed for a minimum of **40,000 stop/start cycles** in the drive. The head gap shall be positioned over the disk at radius R2with -4.557° skew (at the gap). The disk speed shall be **3600 ± 36 RPM.** The acceleration and deceleration time shall be 25 ± 5 sec, with a minimum stop time between cycles of 3 sec.

Results:
The head shall have no apparent signs of wear or degradation. The Slider shall meet electrical performance specifications at all times during the test. Maximum coefficient of stiction between the disk surface and a head shall not exceed 1.5 after 40,000 start/stop cycles. After completion of the test, there shall be no signs of wear through the carbon layer of the disk.

5.3 Heads Static Electrical Characteristics

5.3.1 DC Resistance

The DC head resistance, as measured between tinned portions of leads, shall be ≤ 35 Ω.

5.3.2 Inductance

The inductance at the wire terminals, when measured at 5 MHz, shall be ≤ 800 nH.

5.3.3 Hi-Pot Test

The resistance between the coil winding and any conductive part on the flexure assembly shall be > $1x10^9$ Ω with 15 v DC applied. This is applicable with the head in either the loaded or unloaded position.

The resistance across the slider - to - flexure bond shall be < 2 KΩ.

The breakdown voltage between the coil and the pole tips must be > 300 v DC.

The resistance between the coil winding and permalloy poles shall be > $1x10^9$ Ω with 15 v DC applied.

5.4 Heads Dynamic and Electrical Characteristics

5.4.1 Test Conditions

Test Environment
The test environment shall conform to Section 5.1 Test Environment.

DC Erasure
Unless otherwise specified, all write operations shall be preceded by a DC erase operation.

Radius	Radius ID (mm)	Radius ID (in)	HF (MHz)	MF (MHz)	LF (MHz)	O/W Freq 1/6 of MF	Harm. Elim. Bandpass Filter
R3	29.134	1.1470	24.69	12.35	4.12	2.06	8.23
R4	29.187	1.1490	24.69	12.35	4.12	2.06	8.23
R5	31.285	1.2317	26.18	13.09	4.36	2.18	8.73
R6	33.386	1.3144	28.04	14.02	4.67	2.34	9.35
R7	35.484	1.3970	29.67	14.84	4.95	2.48	9.89
R8	37.577	1.4794	30.52	15.30	5.10	2.55	10.20
R9	39.669	1.5618	32.62	16.31	5.44	2.72	10.87
R10	41.763	1.6442	34.21	17.11	5.70	2.85	11.40
R11	43.855	1.7266	35.71	17.86	5.95	2.98	11.90
R12	45.948	1.8090	37.17	18.59	6.20	3.10	12.39
R13	48.041	1.8914	38.44	19.22	6.41	3.21	12.81
R14	50.134	1.9738	40.00	20.00	6.67	3.34	13.33
R15	52.227	2.0562	41.00	20.50	6.83	3.42	13.67
R16	54.323	2.1387	42.89	21.45	7.15	3.58	14.30
R17	56.416	2.2211	44.21	22.11	7.37	3.69	14.74
R18	58.509	2.3035	44.50	22.25	7.42	3.71	14.83
R19	60.602	2.3859	44.50	22.25	7.42	3.71	14.83
R20	62.694	2.4683	44.50	22.25	7.42	3.71	14.83
R21	63.551	2.5020	44.50	22.25	7.42	3.71	14.83

5.4.2 Read/Write Electronics

Read/Write Preamp
The read/write preamp will have **no external** damping resistor across the head. The total lumped and distributed capacitance across the head, excluding the preamp, shall be < 10.5 pF.

Write current
The current amplitude measured at the head termination connector shall be 10 ± 2 mA (0-P).

Waveform Asymmetry
The difference between any two positive and negative current pulses shall be ≤ 1ns. The risetime T_r and falltime T_f shall be <5.5 ns.

Overshoot
5 -15% of I_W where $I_W = I_{W+} - I_{W-}$

DC Erase Current
The DC erase current shall be 10 ± 2 mA 0-P.

Post-Amplification Frequency and Phase Characteristics
The frequency response, of any post-amplifier, shall be flat, to within ± 0.5 dB, to 60 MHz. The -3dB rolloff point shall be 80 MHz. The attenuation above TBD MHz shall not be less than that given by a line drawn through 0dB at 60 MHz with a slope of 18dB/octave. The group delay shall be flat to within ± 2 ns over the range from 150KHz to 60 MHz.

Transfer Characteristics
For inputs between 0.15mV and 3 mV, the transfer characteristics shall be linear within ± 3%.

Processing filters
For parametric measurements, a 5-pole Butterworth filter (f_{CO} = 47.0 MHz) is required.

5.5 Heads Acceptance Requirements

Track Average Amplitude (TAA)
Using a Test Disk, track average amplitude is defined as the average peak-to-peak amplitude over the entire track under test.

Amplitude
$TAA_{HF} \geq 325$ µV at radius R4.

Resolution
The resolution shall be > 40% for any track.

Overwrite
The overwrite shall be more negative than - 26 dB for any track.

Isolated Pulse Width ($PW_{50}/T = 2.2$)
The PW_{50} shall be ≤ 44.0 ns at radius R4.
The PW_{50} shall be ≤ 24.0 ns at radius R14.

Pulse Asymmetry
TBD

Undershoots
< 5% of the Isolated pulse Base to Peak amplitude.

Write current Delta Resolution
TBD

NonLinear Transition Shift(NLTS) Harmonic Elimination
≤ -14dB(20%) anywhere in the recording zone.

Wave form Stability

NOTE: **Any of the tests listed below may be used alone but additionally, the popcorn test must be performed and requirements met.**

Sigma Amplitude
The sigma of the TAA_{HF} shall be ≤ 3 % of the mean TAA_{HF} when the TAA_{HF} is measured at any radius.

Popcorn Noise
No more than 100 counts are allowed in 1,000 complete cycles.

5.6 Heads Physical Defects

The performance levels and allowable defects contained in this specification represent minimum acceptable level of performance.

5.7 Heads Approved Manufacturers List (AML)

For Approved Manufacture List, see Quantum P/N (TBD)

5.8 Heads Packaging Requirements

Current Requirements
Head packaging shall provide complete protection against physical damage, electrostatic discharge, or contamination. The packaging surface, both inside and outside, shall not accumulate static charge resulting in greater than 100 v of surface voltage. Any anti-static chemicals used must not degrade the Class 100 environment.

Production Requirements
For Head Packaging Instructions, see Quantum P/N (TBD).

5.9 Media Mechanical Requirements

5.9.1 Dimensions

Outside Diameter	130.00 ± 0.10 mm (5.118 ± 0.004 in)
Inside Diameter	40.00 + 0.06/-0.00 mm (1.575 + 0.002/-0.000 in)
Concentricity of OD to ID	≤ 50 µm (0.002 in)
Thickness	1.270 ± 0.013 mm (0.050 ± 0.0005 in)
Flatness	25 µm (0.001 in) diametral 50 µm (0.002 in) circumferentially
OD Roundness	< 12.5 µm (0.0005 in)

Edge Condition
The outside and inside edges of the disk shall be chamfered to the following dimensions:

Angle:	45 ± 5 degrees
Length:	0.15 ± 0.05 mm (0.006 ± 0.002 in)

Taper
The substrate thickness, measured on any radial line from OD to ID, shall at the OD be the same as the ID to within the tolerance +12.7/-51 um (+0.0005/-0.002 in).
Dimensions are to be interpreted as per ANSI Y14.5.
Measurements are to be made at 23 ± 2°C (73 ± 4° F)

5.9.2 Physical Characteristics

Surface Roughness

The axial surface roughness shall be measured with an optical profilometer.

Flyable Zone(Reference)
The arithmetic-average surface roughness shall be 5 nm (0.2 µin), with a maximum protrusion height of 38 nm (1.5 µin) above the average.

Clamping Zone
The arithmetic-average surface roughness shall be 400 nm (16 µin), with a maximum protrusion height of 1.0 µm (39 µin) above the average.

Axial Runout, Velocity and Acceleration

Measurement Method
Using a WYCO model 6000 or 400 Interferometer. The RPM is set to 3600 and the measurements are anywhere in the GUARANTEED DATA ZONE.

Axial Runout(PV)
The axial runout shall be ≤ 15 µm (0.00059 in) TIR and contained within the deflection limits given below.

Axial Deflection
The axial deflection at radius R6 shall be ≤ ± 0.05 mm (0.002 in) from the reference plane defined by the lower clamping surface.

Axial Velocity(PV)	≤ 5 mm/sec (0.2 in/sec)
Axial Acceleration(PV)	≤ 5 m/sec^2 (197 in/sec^2)

Moment of Inertia	≤ 0.032 gm-m^2 (0.0045 in-oz-sec^2)

Glide Height
In the Flyable Zone , there shall be no head-to-disk contacts when the head is flying at the flight heights shown below:

Disk Radius		Flying Height	
mm	in	µm	µin
25.91 - 63.75	**1.020 - 2.510**	**0.0381**	**1.50**

Coefficient of Thermal Expansion
The coefficient of thermal expansion of the disk substrate material shall be 24 ± 1 x 10^{-6}/ ^{0}C over a range of 10 to 57 ^{0}C (13.3 ± 0.5 x 10^{-6}/ ^{0}F over a range of 50 to 135 ^{0}F).

Maximum Speed
The disk shall be capable of meeting all requirements after withstanding the effect of stress induced at a speed of 6000 RPM for 1 minute.

5.9.3 Clamping Zone

For all points on both surfaces in the Clamping Zone, the axial deviation from a flat plane shall be ≤ 5 µm (200 µin).

No identification, part, or serial numbers; logos; manufacturing identifiers; or similar information shall be placed in the Clamping Zone and must not affect flatness, load, or durability.

Both sides of the disk shall be electrically conductive.

5.9.4 Durability of the Magnetic Surfaces

The test shall be performed for a minimum of 40,000 stop/start cycles in the Drive. The head gap shall be positioned over the disk at radius R3 with -1.4° skew. The disk speed

shall be 3600 ± 36 RPM. The acceleration and deceleration time shall be 6 ± 5 sec, with a minimum stop time between cycles of 3 sec. Idle at speed for a minimum of 20 secs

Results:
The disk shall have no apparent signs of wear or degradation. The Disk shall meet all electrical performance specifications at all times during the test. Maximum coefficient of stiction between the disk surface and a head shall not exceed 1.5 after 40,000 start/stop cycles. After completion of the test, there shall be no signs of wear through the carbon layer of the disk.

Continuous-Running Wear Test

The disk shall withstand the effects of a Test Head gliding on the disk at 100 ± 2 rpm, at radius R4, for 48 hours. After completion of this test, any HF amplitude change due to disk wear shall be less than 10%.

5.9.5 Overcoat and Friction of Magnetic Surfaces

Overcoat of the Magnetic Surface

Overcoat Material and Thickness
The disk overcoat material shall be sputtered carbon of thickness not to exceed 200 nm (0.787 µin).

Overcoat Durability
The top coat shall be able to withstand the operating and storage requirements of Sections 5.1 and the durability requirements of Sections 5.9.4.

Head/Disk Friction

Test Requirements
The coefficient of friction between the disk surface and a head, the test method, and the methods of calculation are described in ANSI X3B7/88-02, and shall be performed over the entire Flyable Zone, and for any operating or storage condition of Sections 5.1.

Dynamic Friction Coefficient
The dynamic friction coefficient shall not exceed 0.3 using a Test Head with a 5.0 gm load.

Stiction
The measurement shall be made with a Test Head which has a 5.0 gm preload. The static friction coefficient shall not exceed 0.5 after contact for 24 hours, and shall not exceed 1.5 after any time period and after 40,000 contact start/stop cycles as described in Section 5.9.4.

5.10 Media Testing of Magnetic Characteristics

5.10.1 Test Conditions

Test Environment
The test environment shall conform to Section 5.1 Test Environment.

DC Erasure
Unless otherwise specified, all write operation shall be preceded by a DC erase operation.

5.10.2 Track and Recorded Information

Tested Area
All functional tests and all track-quality tests shall be performed in the Recording Zones.

Test Frequencies

Radius	Radius ID (mm)	Radius ID (in)	HF (MHz)	MF (MHz)	LF (MHz)	O/W Freq 1/6 of MF	Harm. Elim. Bandpass Filter
R3	29.134	1.1470	24.69	12.35	4.12	2.06	8.23
R4	29.187	1.1490	24.69	12.35	4.12	2.06	8.23
R5	31.285	1.2317	26.18	13.09	4.36	2.18	8.73
R6	33.386	1.3144	28.04	14.02	4.67	2.34	9.35
R7	35.484	1.3970	29.67	14.84	4.95	2.48	9.89
R8	37.577	1.4794	30.52	15.30	5.10	2.55	10.20
R9	39.669	1.5618	32.62	16.31	5.44	2.72	10.87
R10	41.763	1.6442	34.21	17.11	5.70	2.85	11.40
R11	43.855	1.7266	35.71	17.86	5.95	2.98	11.90
R12	45.948	1.8090	37.17	18.59	6.20	3.10	12.39
R13	48.041	1.8914	38.44	19.22	6.41	3.21	12.81
R14	50.134	1.9738	40.00	20.00	6.67	3.34	13.33
R15	52.227	2.0562	41.00	20.50	6.83	3.42	13.67
R16	54.323	2.1387	42.89	21.45	7.15	3.58	14.30
R17	56.416	2.2211	44.21	22.11	7.37	3.69	14.74
R18	58.509	2.3035	44.50	22.25	7.42	3.71	14.83
R19	60.602	2.3859	44.50	22.25	7.42	3.71	14.83
R20	62.694	2.4683	44.50	22.25	7.42	3.71	14.83
R21	63.551	2.5020	44.50	22.25	7.42	3.71	14.83

5.10.3 Write Channel

Write Current
The HF write current shall conform to Figure 5-1. The current amplitude measured at the head termination connector shall be 10 ± 2 mA (0 to peak).

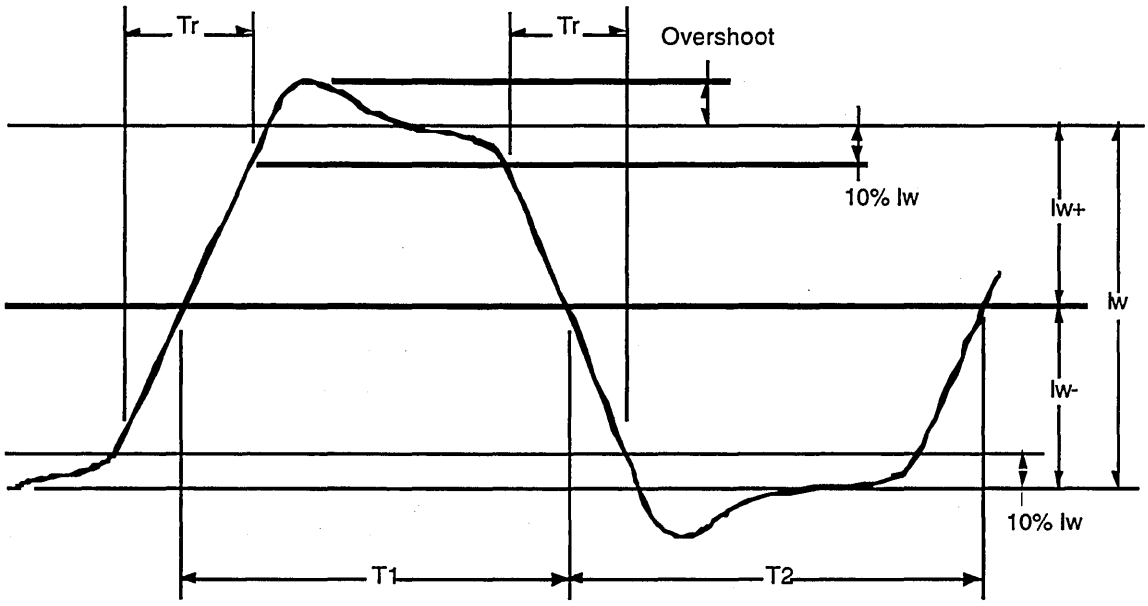


Figure 5-1. Write Current

Asymmetry
The difference between the positive and negative amplitude of the write c current, $I_{W+} - I_{W-}$, shall be ≤ 1 mA. The risetime T_r and falltime T_f shall be ≤ 5.5 ns.

Overshoot
5 - 15 % of I_W where $I_W = I_{W+} - I_{W-}$

DC Erase Current
The DC erase current shall be 10 ± 2 mA (0 - P).

DC Erase
Unless otherwise specified, all write operations shall be preceded by a DC erase operation.

5.10.4 Read Channel

Preamplifier
The read/write preamp will have no external dampening resistor across the head. The total lumped and distributed capacitance seen across the head excluding the preamplifier shall be < 10 pF.

Post-Amplification Frequency and Phase Characteristics
The frequency response, of any post-amplifier, shall be flat, to within ± 0.5 dB, to 60 MHz. The -3 dB rolloff point shall be 80 MHz. The attenuation above 60 MHz shall not be less than that given by a line drawn through 0 dB at 60 MHz with a slope of 18 dB/octave. The group delay shall be flat to within ± 2 ns over the range from 150 kHz to 60 MHz.

Transfer Characteristics
For inputs between 0.15 mV and 3 mV, the transfer characteristics shall be linear within ± 3%.

Automatic Gain Control (AGC) Amplifier
The AGC amplifier shall produce an output voltage V_{AC} that is constant within ± 1% over the frequency range from 1 MHz to 30MHz, for input voltages 0.15 mV p-p ≤ V_{in} ≤ 3 mV p-p. Its response time shall be 10 µs. All frequencies below 10 kHz shall be attenuated at a rate of 6 dB/octave. This section is applicable only for the missing pulse test.

5.11 Media Acceptance Requirements

Track Average Amplitude (TAA)
Using a Test Disk, track average amplitude is defined as the average peak-to-peak amplitude over the entire track under test.

Amplitude
$TAA_{HF} \geq 350\mu V$ at radius R4

Resolution
The resolution shall be > 40 % for any radius.

Overwrite
OVWT shall be more negative than -26dB at any radius.

PW50
The PW_{50} shall be ≤ 44.0 ns at radius R4.
The PW_{50} shall be ≤ 24.0 ns at radius R14.

AC Noise
The media AC noise ratio shall not be more positive than 27 dB at any radius.

Positive Modulation
No positive modulation shall be allowed within the Recording Zones.

Negative Modulation
No negative modulation shall be allowed within the Recording Zone.

Non Linear Transition Shift-Harmonic Elimination
Procedure
The average amplitude of a recorded NLTS Pattern (A1), measured at the output of the bandpass filter(F1) is store. DC erase, write Pattern (A2), the average amplitude is measured at the output of the Bandpass filter(F1) and stored.

NLTS dB = 20 LOG [A1/A2]

For R4 the use the following patterns and filters(51.7 Mflux/sec)
Pattern A1: A0008000H (10100000000000001000000000000B) of length 30 bits
Pattern A2: 80000000H(10000000000000000000000000000000B) of length 30 bits.
F1 : 8.62 MHz, bandpass filter.

Defects
Definition
A defect is physical imperfection on the disk that causes either an extra or a missing pulse in the Recording Zones. See Media Spec. Appendix A Section A.6.9 for the missing pulse and extra pulse test procedures.

There shall be ≤ 80 defects per surface and the length of any one defect shall not exceed 16 bytes when using the test frequencies in Section 5.10.2.

Defect scanning shall be performed at a maximum track-to-track Test-Head step increment of 200 µin.

There shall be no more than 1 defects per track.

5.12 Media Approved Manufacturers List (AML)

For Approved Manufacturer List, see Quantum P/N (TBD).

5.13 Media Packaging Requirements

For Disk Packaging Instructions, see Quantum P/N (TBD).

Section 6 Drive Electronics

6.1 Read Channel Piranha

The AT&T 91C30 is a complete read channel device, including not only the read channel, but an ENDEC, servo demodulator, write precompensation, clock synthesis, quality monitoring, and power down options. The read channel utilizes adaptive equalization to force a class IV partial response and Viterbi detection of the resulting sequence to allow the realization of the higher areal densities.

6.1.1 Read Channel Piranha Features:

- Custom LSI, single chip, 44pin PLCC
- Single +5V supply
- Low power consumption (400 mW typical)
- Power down mode:<5 mW
- Capability of handling up to 85 MBits/sec data rates

- 5 step, 12 db range input attenuator extends AGC range
- AGC digitally controlled in READ mode, analog control in SERVO mode
- 4th order Butterworth continuous time data filter with 2 independently programmable zeroes

- 10 tap discrete time adaptive FIR equalizer with digitally controlled tap weights

- DFE equalizer with digitally controlled tap weights for trailing and leading undershoot cancellation of thin film head

- Interleaved dicode Viterbi detectors
- Encode supports 8/9 and 16/17 density codes: includes preamble generation, sync mark generation, fault tolerant sync mark recognition and scrambling

- Write data outputs programmable CMOS or low- noise differential pseudo-ECL

- Quality monitor flags high error rate conditions and measures rms noise
- Generates own late1, late2 control signals

- Filter flash cuts servo mode programming independent from data mode
- Analog servo field AGC loop independent from read channel gain control
- Servo demodulation from via "weighted sum" averaging peak detection
- Pulse position detector for reading grey code and sector sync mark

- Programmable prescaler, feedback divider for worst case 1% resolution on time base generator
- Internal programmable loop filter saves external components and eliminates externally injected noise

6.1.2 Read channel block diagram

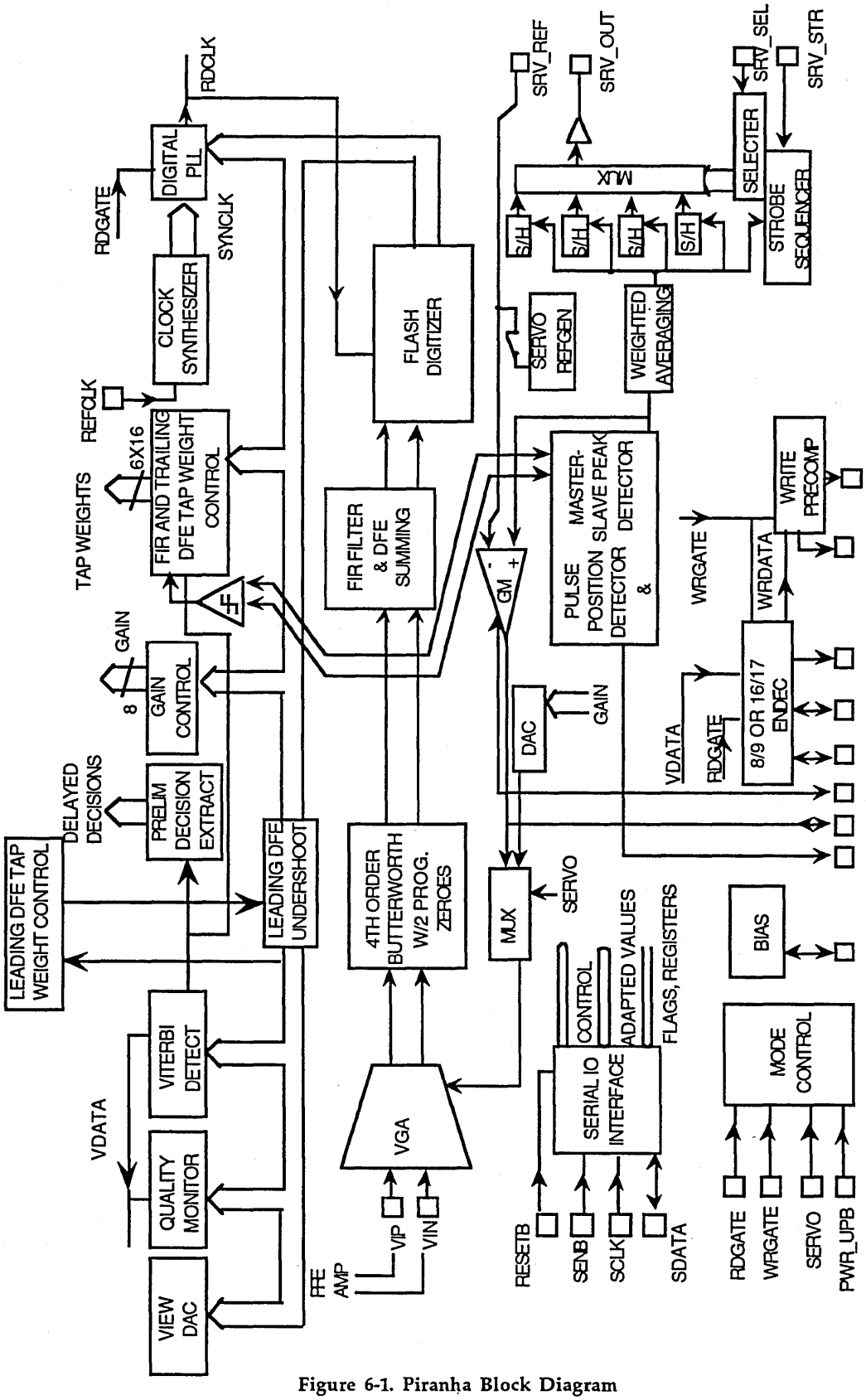


Figure 6-1. Piranha Block Diagram

6.2 Preamp

- Supply Voltage: 5±10%
- 20 & 24 pin SOP
- Low Noise: 0.5 nV/root Hz max
- Differential Voltage Gain: 370±10%
- Write Current Rise Time: 5.5 nS

6.3 Microcontroller

The NEC μPD78352 is a member of the K-Series of microcontrollers.

6.3.1 Features

- 40MHz Clock Operation
- Built-in ROM 54K X 8bits
- Built-in RAM 640 X 8 bits
- Compatible with μP78350

The NEC 78352 microprocessor has a 64K address space. On Vortex, it is organized as follows:

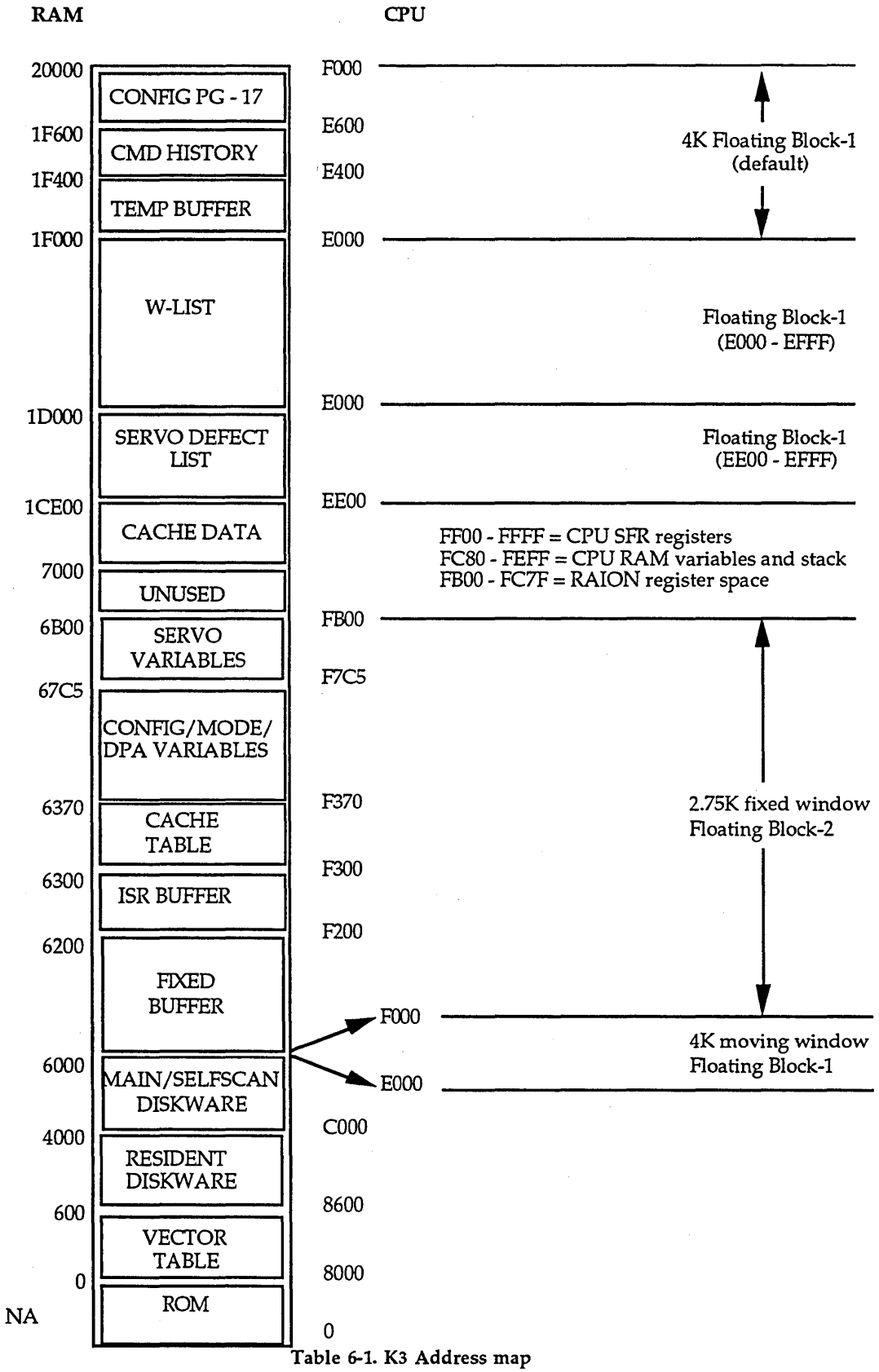


Table 6-1. K3 Address map

6.4 ASIC

The RAION is a CMOS VLSI component that combines a programmable RAM-base disk formatter, the high bandwidth Buffer Controller, and a host interface for both ATA and SCSI standards.

The RAION has power saving features built in, it provides an automatic low-power dynamic mode to stop transactions on the ATA or SCSI bus, as well as stopping internal clock in each separate block or shut off internal clock completely in sleep mode.

The RAION combined from 10 main blocks:

- Host Interface (AT) or (SCSI) module
- Buffer Control (BFR) module
- Motor Interface (MTR) module
- Analog to Digital Converter (ADC) module
- Servo Control (TNA) module
- Serial Interface (SER) module
- Microprocessor Interface (UPI) module
- Sequencer Control (SEQ) module
- Error Correction Control (ECC) module
- Top Test (TST) module

6.4.1 Capabilities and Features

6.4.1.1 Host Interface

ATA Standard Interface

- Supports ATA Standards Interface
- Use same I/O cell as SCSI interface with the DC pull up mode
- 16 bit wide fast DMA transfer on host bus up to16 Mbytes/sec
- Supports Auto Functions
- LBA and CHS support
- Transfer rate: 6 Mb/s in sustained mode and 16 Mb/s in burst mode

6.4.1.2 Embedded Servo

- Generates control signals for burst amplitude measurement
- Support tri-burst and quad-burst servo wedge
- SAM: 14T or 9T programmable
- Detects necessary syncs 2T vs 3T in wedge area
- Keep wedge high in find mode until locked
- Read tracks number in wedge area
- Supports Thermal Asperity logic (Not used in Vortex)

6.4.1.3 DRAM Buffer Interface

- Support 64K x 16 (dual-WE) or 256K x16 (dual-CAS) DRAM, no parity
- Bufferware, uP firmware executes from the DRAM buffer memory
- CPU direct access, uP accesses directly from the DRAM buffer memory
- Wait state control
- 32 Mbytes/s maximum buffer bandwidth
- 11 Mbytes/s maximum disk channel bandwidth
- 10 Mbytes/s maximum host channel bandwidth

6.4.1.4 Control Disk Read/Write

- Generates Readgate, Write gate, etc. for R/W component
- 2 bit wide decoded data "Piranha" type interface
- RAM based control store (30 bits x 36 words)
  - Handles split data fields for constant rate servo wedges in multiple zone drives
  - No microprocessor intervention needed for up to full track read/write
  - Format information (where variable breaks for sector are) contained in the headers
- ID after wedge
- 24 bit CRC and Triple burst with 160 bit REED-SOLOMON ECC algorithm, allows 'ECC On-the-fly"

6.4.1.5 Microprocessor Functions

- Supports K3 NEC Microprocessors
- Single Crystal architecture use for both system and Microprocessor clocks
- Memory mapping allows access to full DRAM
- Demuxes MAD bus
- Generates different clock rates, allows clocks to be slowed or stopped for power conserving modes

6.4.1.6 Serial Interface Functions

- Serial interface with Read and Write mode to R/W and spindle , VCM driver
- Allows 10, 20 and 40 MHz operating modes

6.4.1.7 Analog to Digital & Digital to Analog Converter Functions

- Successive approximation type 8 bits A/D Converter, 3.3 usec conversion time, linearity ± 1/2 LSB, with power down mode
- Supports new Read channel " Piranha" interface
- 13 bit effective DAC formed by external 32:1 gain summing of 6 and 5 bit PWMs with 4 x oversample

6.5 DRAM

A 1Mbit 80 nS Fast Page Mode DRAM in a 64 K x 16 organization with upper and lower write enable packaged in a 40 pin SOJ.

6.6 Motor/VCM

COMBO (HA13545F) is a combination chip that includes the VCM driver, the spindle motor driver, the VCM park circuitry and the power on reset circuitry.

Overview:

- No external power drivers
- Dynamic braking for non-power down situations
- 1.8 A max spindle drive
- 1.2 A max VCM drive
- Soft switching spindle drive
- POR monitors both 5 v and 12 v supply
- Auto-park in case of power down
- Speed discrimination

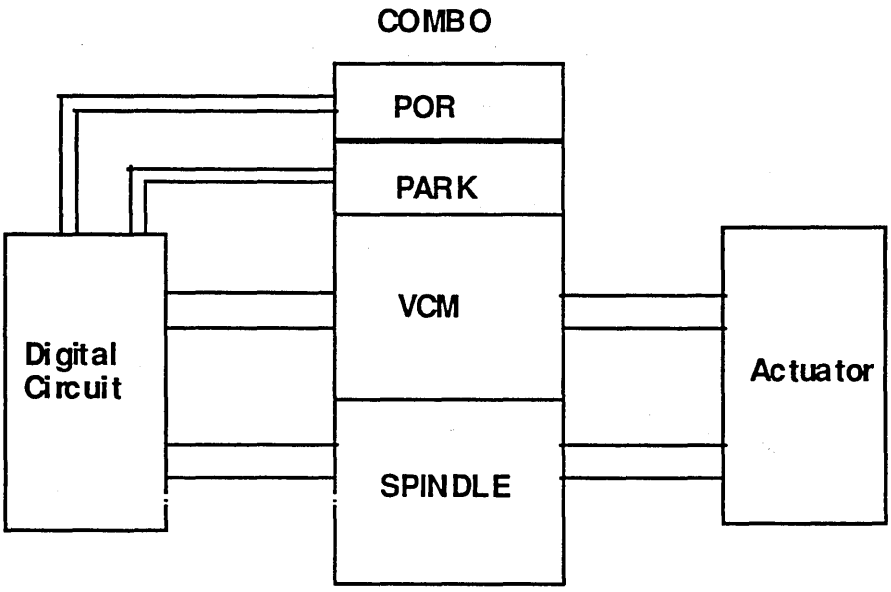


Figure 6-2. Combo System Block Diagram

6.7 PCB

6.7.1 PCB Layout Consideration

The PCB consists of four layers: a component/signal plane, a +5V power plane , a ground plane and a signal plane. The PCB has components on both sides. The four layer design provides an opportunity to:

6.7.1.1 Separate high frequency clock signals and other high current traces from noise-sensitive low amplitude analog signals such as readback signals.

6.7.1.2 Shield high frequency digital signals so as to reduce the energy dissipated by RFI emissions.

6.7.1.3 Provide ample ground planes for better ESD protections.

6.7.1.4 Use wide voltage and ground planes to prevent current loops that creates impedance difference between the power supplies and various parts of the PCB.

6.7.1.5 Provide adequate heatsinking capability for high current lines (spindle motor and VCM).

6.7.1.6 Provide power plane and trace keep out area's where drive mounting screw damage can occur. See Figure 6-6.

6.7.2 Component Selection and Assembly Process

All land sizes were chosen for best placement registration to avoid misalignment, no contact, tombstoning resulting from unequal termination wetting and other SMD parts related solder problems. The fudicial marks at PCB corners help the high resolution vision feedback IC placement machine, especially necessary for fine-pitched QFP placements(TBD mm pin spacing).

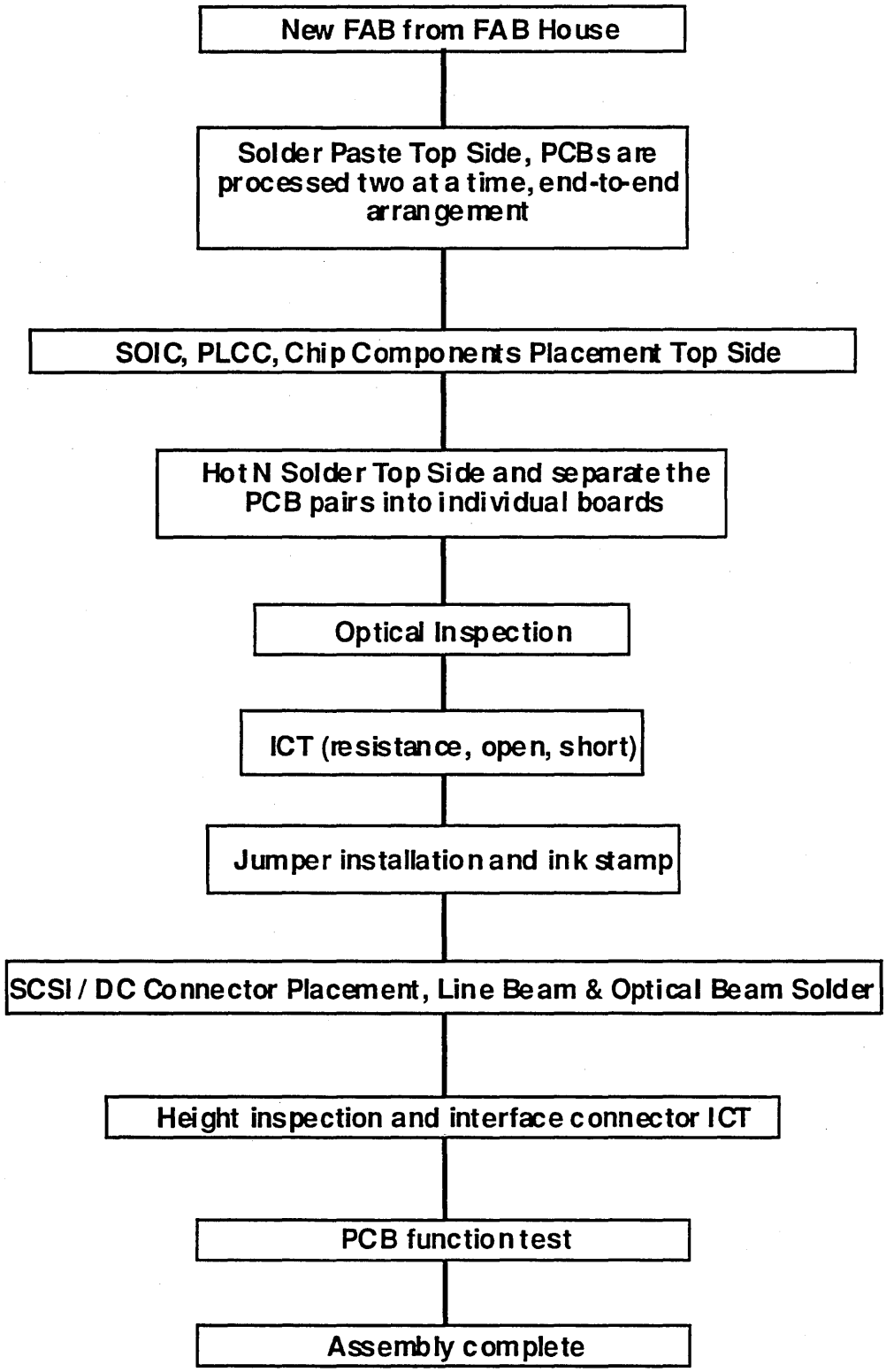
PCB components selection was limited, besides performance, price and availability considerations, by package to fit the form factor, automatic placement, solder and other assembly equipment restrictions, ease of testing requirements, etc. The height requirement for the top side is 4.57 mm max, and for the bottom side 0.4 mm max. In order to meet these requirements, all components are mounted only on the top side while traces run on both sides. The current MKE PCB assembly process is illustrated in the next page.

Silver paste thru-hole process PCB will not be evaluated for the Vortex project.

6.7.3 Compression Connector

The choice of a 20-position AMP compression connector was to facilitate automated assembly at MKE while making maximum use of limited boardspace provided. The compression connector is designed for maximum immunity to crosstalk between the R/W and motor pins as well as for solid mounting with minimum sensitivity to PCB flexure. Guide pins are built onto the connector on both sides to limit mounting tolerance with respect to fab and HDA.

6.7.3 PCB Assembly Process



6.7.4 Connectors

In the current version of the Vortex design, the following connectors are used:

J1	AT/DC COMB 3/1 CONN.	QNTM # 22-103854-02
J22	R/W-MOTOR COMPRESSION CONN.	QNTM # 22-109938-20
JP1	ID JUMPER AT	QNTM # 22-105849-01

6.7.5 AT PCB Block Diagram

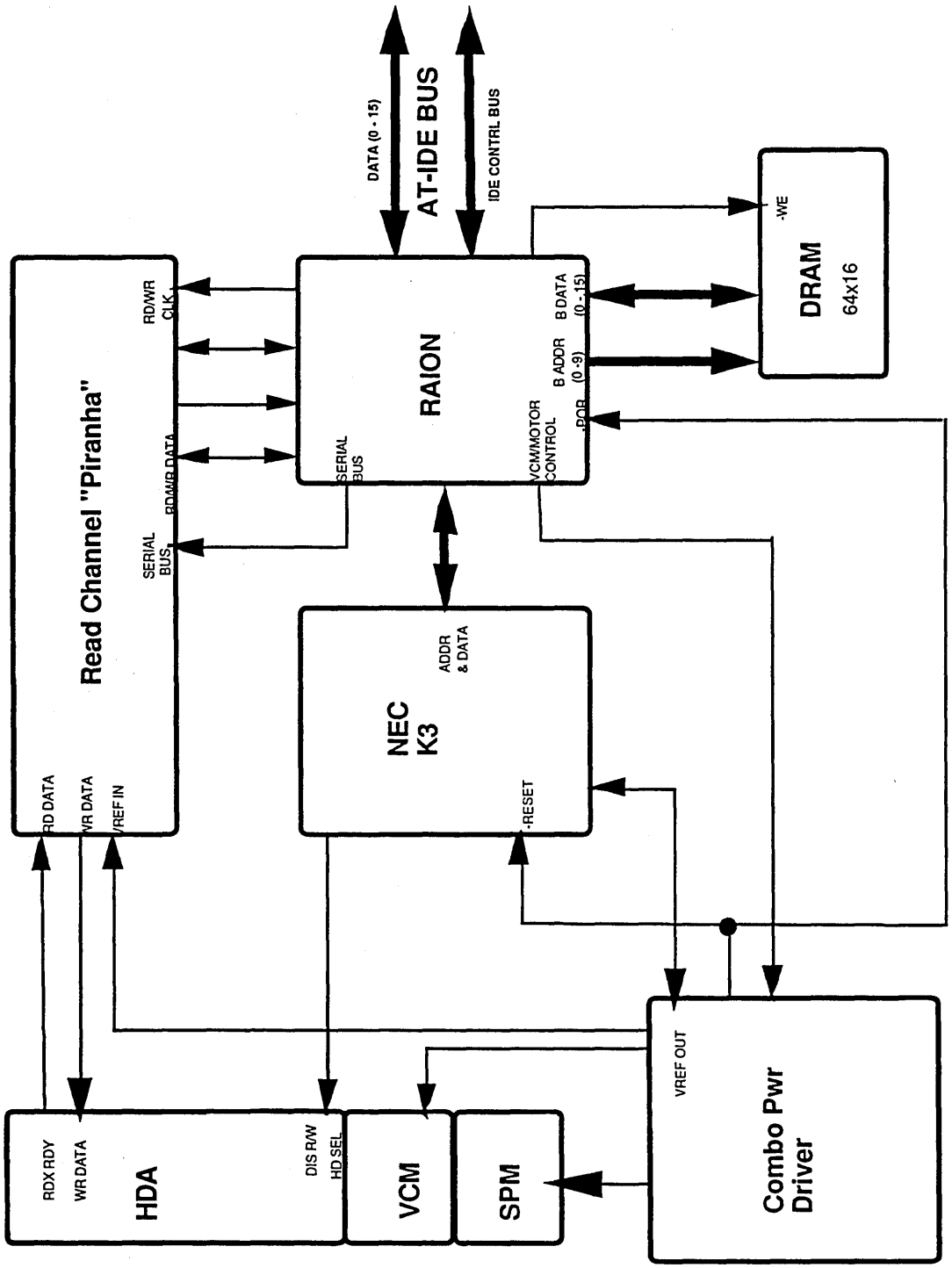


Figure 6-3. AT PCB Block Diagram

6.7.6 PCB Non-Component Area

TBD

Figure 6-4. PCB Non-component Area

6.8 Power Budget

6.8.1 Power Budget with Combo

	Typical Power mW				
	Startup	Idle	Sleep or Standby	Max Seeking	Read or Write
K3 (5V)	300	300	300	300	300
RAION (5V)	500	500	500	600	650
DRAM (5V)	70	15	3	20	70
Piranha (5V)	200	200	200	475	740
PreAmp (5V)	95	95	1	145	145
Others (5V)	25	25	1	25	25
Combo (5V)	110	110	1	110	110
Total Power (5V)	1300	1245	1006	1675	2040
Total Power (12V)	15000	2400	1	6720	2400
Total in Watts	**16.3 W**	**3.6 W**	**1.0 W**	**8.4 W**	**4.4 W**

Table 6-2. 2 Disk Power Budget Combo—E2

Section 7 Firmware Organization

7.1 Firmware Features

The Vortex firmware was derived from the Trailblazer code base. Features were added to support the Shiva read channel and much of SelfScan was changed to implement a Test Process that is similar to Fireball. Additionally a new Defect Management scheme (LBA Based Defect Management) was implemented. The major areas of change are detailed below.

7.1.1 SUPPORT FOR MORE THAN 256 SECTORS PER TRACK

Vortex is the first Quantum drive to have more than 256 sectors per physical track. The original firmware architecture was optimized, due to code efficiency considerations, for less than 256 sectors per track. In order to support more than 256 sectors per track , a number of data structures and internal calculations were changed to support word size rather than byte size data. Additionally, the I/O structures for the Superset commands were changed.

The RAION ASIC does not provide direct support for more than 256 sectors per track; however, using a special "Double Sectors per Track" format with the corresponding sequencer wcs program it is possible to support up to 512 sectors per track. Additionally, the track format was modified for four count bytes per wedge to improve format efficiency.

7.1.2 LBA-BASED DEFECT MANAGEMENT

At the start of the Vortex program, the defect characteristics of the media were not well understood and there was consideration given to using uncertified media to reduce media costs. Additionally, with the large number of sectors per track it is likely that some tracks will contain multiple defects.

The principal advantage of the LBA-Based Defect Management scheme, compared to other methods, is that it allows multiple inline defects on a track with no reduction in drive performance. In Vortex, this feature is also taken advantage of to support sparing of sectors around a defective servo wedge and to allow bad track sparing for tracks that contain too many servo defects.

7.1.3 S.M.A.R.T Phase 4

Vortex supports version 4 of the S M.A.R.T feature. The main change in phase 4 is the addition of the off-line test

7.1.4 SERVO DEFECT MAPPING

The Servo Defect mapping scheme used in Fireball was ported to Vortex. This feature allows two defective wedges per track to be mapped out. The defective servo wedges are determined during SelfScan Servo Verify and a Servo Defect List is constructed and saved to disk. During the set up for a seek operation, the Servo Defect List is searched for the destination track and if an entry is found it is copied to the Wedge Defect List. During the servo interrupt in track following mode the current wedge number is compared to the Wedge Defect List entries. If the entry matches, the position information for the current wedge is ignored and the servo free-wheels through the wedge. In Vortex the servo defect list scheme has been extended to allow consecutive bad wedges (in this case the six following wedges are mapped out in the Data Defect List). Also, a special entry in the servo defect list is used to indicate a bad track that has been spared.

7.1.5 READ CHANNEL OPTIMIZATION

Read channel optimization algorithms developed by the Vortex Read/Write Group were implemented in SelfScan. These algorithms use iterative methods to provide better optimized parametrics in less time than the previous method used in Fireball.

7.1.6 WEDGE TO WEDGE SCAN

The Piranha read channel optimizations make use of the wedge to wedge sequencer programs.

It is generally accepted that wedge to wedge scanning provides better coverage for sync field and ECC field areas than can be achieved through sector scanning. Also it is possible to stress the channel more during wedge to wedge scan to enhance the defect detection because a fixed data pattern without ECC bytes is used.

For these reasons, and to make the Test Process equivalent to Fireball, a Wedge to Wedge Scan was implemented as part of SelfScan.

7.1.7 SCAN IMMEDIATE/SCAN MULTIPLE

To make the defect scanning more efficient it is desirable to reduce the amount of time spent in latency and seeking compared to that read and writing.

In Vortex a technique called Scan Immediate was implemented for both wedge to wedge and sector scans. This technique samples the current rotational position when starting a read or write operation and if the target sector/wedge is not within a predetermined window adjusts the target so that the reading or writing can start sooner. This allows much of the latency time during scanning to be eliminated.

The Scan Multiple feature scans each track using multiple data patterns before seeking to the next track, which reduces the total seek time required. This method was already implemented in the Trailblazer code base; however, it was enhanced to allow more data patterns and to allow the data patterns to be optionally scanned with offset.

7.1.8 CUSTOMER SCAN

Customer Scan was modified to provide a soft error rate measurement equivalent to Fireball. In Vortex, Customer Scan is only used for soft error rate measurement and as a confidence scan to verify the inline formatting. It is not used for defect mapping because defect mapping can be done more efficiently using wedge to wedge and physical sector scanning.

7.1.9 SELFSCAN CSS

SelfScan CSS is intended to duplicate the normal CSS testing done via the drive interface. The advantage of SelfScan CSS is the reduction in the equipment required to support qualification CSS testing. For Vortex, MKE requested that SelfScan CSS be available for P1

7.1.10 RECAL RECORD

Recal-Record is used to shorten the time to Ready. The basic scheme is to record certain variables during a recal operation on to the disk in the system cylinder area. The Recal Record is written to the disk after the last recal steps are performed. After the record is loaded into the buffer, the data is CRC'd, with the CRC value appended to the end of the record.

Presently, the data that is recorded in this sector is from NULLI tables and the VSCALE feed forward values. The NULLI and VSCALE values were chosen because they are PCB and HDA dependent and they are adapted while the drive is operating. On subsequent power-on cycles, the record is read and, if valid, the stored values are used instead of performing the recal steps. This is good for a 3-4 second savings in Time-to-Ready.

7.2 Caching

Vortex incorporates DisCache, an 87K cache, to enhance drive performance. This integrated feature is user-programmable, using the MODE SELECT command, and can significantly improve system throughput.

7.2.1 READ CACHE DESCRIPTION

DisCache anticipates host-system requests for data and stores that data for faster access. When the host requests a particular segment of data, the caching feature uses a prefetch strategy to "look-ahead" and automatically store the subsequent data from the disk into high-speed RAM (Random Access Memory). If the host requests this subsequent data, the RAM is accessed rather than the disk.

Since typically 50 percent or more of all disk requests are sequential, there is a high probability that subsequent data requested will be in the cache. This cached data can be retrieved in microseconds rather than milliseconds. As a result, DisCache can provide substantial time savings during half or more of all disk requests. In these instances, DisCache may save most of the disk transaction time by eliminating the seek and rotational latency delays that dominate the typical disk transaction. For example, in a 1K-byte data transfer, these delays comprise 90 percent of the elapsed time.

DisCache works by continuing to fill its cache memory with adjacent data after transferring data requested by the host. Unlike a non-caching controller, Quantum's disk controller continues a read operation after the requested data has been transferred to the host system. This read operation terminates after a programmed amount of subsequent data has been read into the cache segment.

The cache memory is a 87K DRAM buffer allocated to hold the data which can be directly accessed by the host via the READ and WRITE commands. The memory functions as a group of segments (ring buffers) with rollover points at the end of each segment (buffer). The unit of data stored is the logical block (i.e., a multiple of the 512 byte sector). Therefore, all accesses to the cache memory must be in multiples of the sector size. In those cases where the cache memory must be used for scratch memory, as in the case of a FORMAT UNIT command, or where the size of the logical block may change, as in the MODE SELECT command, the cache will be emptied. The commands that will force emptying of the cache are:

- FORMAT UNIT
- INQUIRY
- READ DEFECT DATA
- READ LONG
- READ CAPACITY
- WRITE LONG
- MODE SELECT
- MODE SENSE
- REASSIGN BLOCKS

7.2.2 WRITE CACHE

When a write command is executed with write caching enabled, the drive stores the data to be written in a DRAM cache buffer and immediately sends a COMMAND COMPLETE message to the host before the data is actually written on the disk. The host is then free to move on to the other tasks, such as preparing data for the next data transfer, without having to wait for the drive to seek to the appropriate track or rotate to the specified sector.

While the host is preparing data for the next transfer, the drive immediately writes the cached data to the disk, usually completing the operation after issuing COMMAND COMPLETE.

WriteCache allows data to be transferred in a continuous flow to the drive rather than as individual blocks of data separated by disk access delays. This is achieved by taking advantage of the ability to write blocks of data sequentially on a disk that is formatted with a 1: 1 interleave. This means that as the last byte of data is transferred out of the write cache, and the head passes over the next sector of the disk, the first byte of the next block of data is ready to be transferred; thus there is no interruption or delay in the data transfer process.

The WriteCache algorithm writes data to the cache buffer while simultaneously transferring data to the disk that was previously written to the cache.

7.2.3 PERFORMANCE BENEFITS

In a drive without DisCache, during sequential reads, there would be a delay due to rotational latency even if the disk actuator were already positioned at the desired cylinder. DisCache

eliminates this rotational latency time -- 8.33 milliseconds on average -- when requested data resides in the cache.

Moreover, the drive often must service requests from multiple processes in a multitasking or multiuser environment. In these instances, while each process may request data sequentially, the disk drive must share time among all these processes. In most disk drives, the heads must move from one location to another. With DisCache, even if another process interrupts, the drive continues to access the data sequentially from its high-speed memory. In handling multiple processes, DisCache achieves it most impressive performance gains, saving both seek and latency time when desired data resides in the cache.

7.2.4 FLEXIBILITY, EASE OF USE, SPEED

DisCache was originally designed to be flexible because cache performance is highly application-dependent. Several parameters are automatically adjusted by the drive, this allows the drive to continuously optimize its performance. The remaining options which are still programmable enable users to adjust caching parameters to optimize performance. These options can be specified and subsequently modified using the set configuration command. Table 7-1 outlines both the programmable and the fixed parameters; the discussion following the table explains the parameters and how they can be used.

Parameter	DisCache functionRange	Input Value	Default
Read Cache disable	Activates read cache when cleared (bit=0)	0,1	0
Write Cache enable	Activates write cache when set (bit=1)	0,1	1
No. of Cache Segments	Sets number of cache segments to be maintained	not changeable	dynamic
Maximum Prefetch			dynamic
Minimum Prefetch		dynamic	
Disable Prefetch Transfer Length	Enable/Disable = 0 prefetch	0-FFFF	FFFF

Table 7-1. DisCache parameters.

Through the use of these programmable parameters, the caching feature can be tailored to optimize individual system performance. The programmable parameters shown in Table 7-1 can be found in the AT READ/SET configuration command. When the Read Cache Disable bit is set to one, caching is disabled. Disabling the cache reduces command overhead. When disabling the cache, you essentially disable the prefetching and house-keeping required to manage the cache. The default value of this bit is zero (Cache enabled).

The Read cache is divided into segments. Each segment contains one cache entry. A cache entry consists of the requested READ data plus its corresponding prefetch data.

The requested READ data takes up a certain amount of space in the cache segment so the corresponding prefetch data could essentially occupy the rest of the space within the segment.

7.3 Error Correcting Code

7.3.1 ECC Features

- 8 bits per symbol.
- 3 interleaves.
- 6 redundancy bytes per interleave.
- 2 cross-check bytes.
- 18 ECC bytes and 2 cross-check bytes: total of 20 redundancy bytes.
- ECC hardware includes Reed-Solomon encoder/decoder circuit that is used to generate redundancies during write mode and syndromes during read mode. The

hardware also checks the values of the syndromes to detect error. All corrections will be done in firmware.

- Single-Error Correction:
  — Correct up to 24 bits (i.e. 1 byte per interleave).
  — Guarantee to correct 17 bits.

- Double-Error Correction:
  — Correct up to 48 bits (i.e. 2 bytes per interleave).
  — Guarantee to correct 41 bits.

- Triple-Error Correction:
  — Correct up to 72 bits (i.e. 3 bytes per interleave).
  — Guarantee to correct 65 bits.

- Random Multiple-burst error case: correct up to 9 bytes.

- Scan-path is available for testability.

- ECC syndromes and cross-checks can be observed by selecting the ECC registers from (E0)h to (F3)h.

7.3.2 ECC Equations

7.3.2.1 Galois Field

The Galois field for the ECC and cross-check polynomials is generated using the extension field theory and is described as follows:

- Sub Field $GF(2^4)$:
  Let elements of the sub field be represented by powers of beta. The sub field is defined by the following polynomial:

  $$P_{sub}(X) = X^4 + X + 1$$

  with $beta^1$ = (02)h as the first element of $GF(2^4)$ over GF(2).

- Extension Field $GF(2^8)$:
  Let elements of the extension field be represented by powers of alpha. The extension field is defined by the following polynomial:

  $$P(Z) = Z^2 + Z + f_0$$

  where
  f_0 = (08)h as a constant and
  $alpha^1$ = (12)h as the first element of $GF(2^8)$ over GF(2).

7.3.2.2 ECC Polynomial

The ECC polynomial is defined as follows:

$$ECC(X) = X^6 + alpha^{169}*X^5 + alpha^{179}*X^4 + alpha^{25}*X^3 + alpha^{184}*X^2 + alpha^{179}*X + alpha^{15}$$

$$= (X + 1)*(X + alpha^1)*(X + alpha^2)*(X + alpha^3)*(X + alpha^4)*(X + alpha^5)$$

7.3.2.3 Cross - Check Polynomial

The Cross - Check Polynomial is defined as follows:

$$XC(X) = X^2 + alpha^{143}*X + 1$$
$$= (X + alpha^{127})*(X + alpha^{128})$$

7.4 Description of CRC

7.4.1 CRC for ID Field

The ID data is protected by 3-byte Reed-Solomon CRC. The values of CRC bytes can be observed by selecting the following registers: (F4)h for CRC0, (F5)h for CRC1, and (F6)h for CRC2.

7.4.2 CRC Equations

7.4.2.1 Galois Field

The Galois field for the CRC polynomial is the same as the ECC and the cross-check polynomials.

7.4.2.2 CRC Polynomial

The CRC polynomial is defined as follows:

$$CRC(X) = X^3 + alpha^{203}*X^2 + alpha^{203}*X + 1$$

$$= (X + alpha^{-1})*(X + alpha^0)*(X + alpha^1)$$

7.5 Probabilities

7.5.1 Probability Model

Assumption 1: every symbol has equal error probability and error pattern is occurred completely random.

Assumption 2: each error burst is associated with a single byte.

Probability numbers are defined as follows:

- P_s : raw error rate (events/bit). This number is obtained before ECC system.
- P_h : probability of hard error (events/bit) obtained after on-the-fly ECC.
- P_{ue} : probability of uncorrectable errors (events/bit) when the number of symbol errors exceeds the correction capability of the code.
- P_{mc}: probability of miscorrection. This is a conditional probability that depends on the number of errors occurring.
- P_{xc} : misdetection probability of the cross-checks.
- P_e : probability of decoding error when the ECC incorrectly decodes and sends erroneous data to customer.

7.5.1.1 Probability of Uncorrectable Errors:

Probability of uncorrectable errors (events/bit) when the number of symbol errors exceed the correction capability of the code.

$$R_u = \frac{1}{n^* m} \sum_{i>t}^{n} \binom{n}{i} (P_s^* m)^{i} * (1 - P_s^* m)^{n-i} \qquad (1)$$

where

n : number of symbols per interleave including redundancy symbols.
m: symbol width in bits.
t : correction capability in symbols.
P_s*m : raw symbol error rate (events/symbol).

7.5.1.2 Probability of Miscorrection

The Reed-Solomon ECC is characterized as a maximum distance separable (MDS) code in which d = n - k + 1. We are using an incomplete decoder for a t-error-correcting code that t is equal to (n - k)/2. This means that the ECC only corrects all errors with t symbols or less and does not attempt to correct more than t error symbols. When an error burst of a received word is less than or equal to t symbols, the code corrects without any miscorrection errors. This means that P_{mc} is equal to zero. If there is error greater than t symbols, the code either sends an uncorrectable message or decodes the error patterns and error locations incorrectly. The value of P_{mc} then can be estimated as follows:

$$P_{mc} = q^{-r} * V(t) \qquad (2)$$

where

$q = 2^m = 2^8 = 256$.

$r = n - k$ –> (code's redundancy).

$$V(t) = \sum_{s=0}^{t} \binom{n}{s} * (q-1)^s$$ (volume of a Hamming sphere of radius t)

Therefore,

- For $e \le t$, $P_{mc} = 0$ (3a)

- For $e > t$, $$P_{mc} = \frac{\sum_{s=0}^{t} \binom{n}{s} * (q-1)^s}{q^r}$$ (3b)

(where e: number of symbol errors).

7.5.1.3 Probability of Misdetection of Cross-Checks

The probability of misdetection of the cross-checks can be estimated as follows:

$$P_{xc} = \frac{1}{q^{xc}} \qquad (4)$$

where

rxc: number of cross-check symbols.

7.5.1.4 Probability of Decoding Error

This probability can be translated as the probability of transferring erroneous data to customer. P_e can be obtained by taking the product of P_u, P_{mc}, and P_{xc} :

$$P_e = P_u * P_{mc} * P_{xc} \qquad (5)$$

7.5.2 Error Probabilities

7.5.2.1 ON-THE-FLY CORRECTION (SINGLE- OR DOUBLE-ERROR CORRECTION)

Assumption: $P_s = 10^{-7}$ (raw soft error rate).

$$P_u = \frac{1}{176*8}\sum_{i=3}^{176}\binom{176}{i}(10^{-7}*8)^i * (1-10^{-7}*8)^{176-i}$$

$$= 3.3 * 10^{-16}$$

$$P_{mc} = \frac{\sum_{s=0}^{2}\binom{176}{s} * (256-1)^s}{256^6}$$

$$= 3.5 * 10^{-6}$$

$$P_{xc} = \frac{1}{256^6} = 1.5 * 10^{-5}$$

$$P_e = P_u * P_{mc} * P_{xc} = 1.7 * 10^{-26}$$

7.5.2.2 OFF-LINE CORRECTION (TRIPLE-ERROR CORRECTION)

Assumption: $P_s = P_h = 10^{-10}$ --> hard error rate
(i.e. hard errors beyond the correction capability of on-the-fly ECC)

$$P_u = \frac{1}{176*8}\sum_{i=4}^{176}\binom{176}{i}(10^{-10}*8)^i * (1-10^{-10}*8)^{176-i}$$

$$= 1.12 * 10^{-32}$$

$$P_{mc} = \frac{\sum_{s=0}^{3} \binom{176}{s} * (256-1)^s}{256^6}$$

$$= 5.0 * 10^{-2}$$

$$P_{xc} = \frac{1}{256^2} = 1.5 * 10^{-5}$$

$$P_e = P_u * P_{mc} * P_{xc} = 8.4 * 10^{-39}$$

7.5.2.3 Summary

In the off-line correction case, the probability of miscorrection (P_{mc}) is 5.0E-2 that is quite high and unacceptable. In order to improve this probability number we use two cross-checks to detect miscorrection. These two cross-checks make the effective miscorrection probability equal to 7.0E-7 (i.e. $P_{mc} * P_{xc}$ = 5E-2 * 1.5E-5 = 7.0E-7) which is better than P_{mc} by itself.

In addition to the two cross-checks, we also employ an off-line correction algorithm in firmware that rereads a number of times with on-the-fly ECC, and performs triple-error correction only when hard error is detected. These criteria improve P_s from 10^{-7} to 10^{-10} (i.e. P_h) which effectively improve the probability of transferring erroneous data to customer as depicted above. Note that we assume the worst case here with P_h = 10^{-10}, because the typical number should be about 10^{-14}.

7.6 Microprocessor Memory Map, Diskware and F/W Organization

The Vortex architecture has been designed to support Diskware. Part of the Buffer memory is used to load firmware from disk and the processor is able to execute the firmware directly from the buffer memory.

The firmware is partitioned between the CPU ROM and the Diskware. The CPU ROM code contains all of the routines necessary to power up the drive and read the Diskware into the Buffer. It also contains routines that allow the Diskware to be written to the disk via the host interface. All time critical code is located in the CPU ROM because the processor is able to execute CPU ROM code much faster than Diskware code. The Diskware code contains firmware that is not required for powering up the drive. The Diskware code also contains provisions to allow for possible engineering firmware changes in the CPU ROM code to be corrected by mapping erroneous subroutines from CPU ROM into the Diskware.

The Diskware code space is partitioned into three parts, a resident part, an overlay part and an Selfscan part. The resident Diskware is loaded during the drive power up initialization and remains in memory while the drive is powered on. The overlay Diskware is loaded on as needed basis. The Selfscan Diskware is loaded on an as needed basis into memory space designated as the Cache space as an overlay during drive process test.

The Diskware is stored on reserved system cylinders in memory image format. A new configuration page 15 specifies where the overlays are stored on the system cylinders and where the overlays are loaded into the processor memory. Generally system cylinder information is stored in multiple places for redundancy, the overlay configuration page only specifies where the first copy of the Diskware is stored. Redundant copies of the Diskware are stored according to the firmware redundancy algorithm for system cylinder information. The VORTEX firmware stores redundant system cylinder information on all physical heads in system cylinder areas. See Section 3.3 for reserved system cylinder information.

Configuration Page 15 - Overlay Page

Field Offset	Description
0	00h - Overlay 0 - Resident Diskware.
1	Load address.
3	Number of sectors.
4	Cylinder.
6	Head.
7	Starting sector.
8	01h - Overlay 1 - Normal operating Diskware.
9-15	Same field as above.
16	02h - Overlay 2 - Selfscan Diskware.
17-23	Same field as above.
24	FFh - End marker.

The NEC 787012 microprocessor has a 16 MB address space. On Vortex, DRAM allocation is organized as follows:

VORTEX MEMORY ALLOCATION

K3 ADDRESS		DRAM ADDRESS
Floating Block 1 (default) 0E600h	CONFIG PAGE 17 2.5 K HARDWARE ZONE VALUES	20000h 1F600h
Floating Block 1 (default) 0E5FFh 0E400h	COMMAND HISTORY 0.5 K	1F5FFh 1F400h
Floating Block 1 (default) 0E3FFh 0E000h	TEMP BUFFER 1 K	1F3FFh 1F000h
Floating Block 1 0EFFFh 0E000h	W LIST 8 K	1EFFFh 1D000h
Floating Block 1 0EFFFh 0EE00h	SERVO DEFECT LIST 0.5 K	1CFFFh 1CE00h
Floating Block 1 0EFFFh 0E000h	CACHE BUFFER 87.5 K	1CDFFh 7000h
Floating Block 1 0EFFFh 0EC00h	ERROR LOGGING 1 K	6FFFh 6C00h
Floating Block 1	NOT USED 0.25 K	6BFFh 6B00h
Floating Block 2 0FAFFh 0F300h	FIRMWARE TABLES, VARIABLES AND CONFIG PAGES 2 K	6AFFh 6300h
Floating Block 2 0F2FFh 0F200h	ISR BUFFER 0.25 K	62FFh 6200h
Floating Block 2 0F1FFh 0F000h	FIXED BUFFER 0.5 K	61FFh 6000h
Direct Access 0DFFFh 0C000h	OVERLAY DISKWARE 8 K	5FFFh 4000h
Direct Access 0BFFFh 08000h	RESIDENT DISKWARE 16 K	3FFFh 00000h
Direct Access 07FFFh 00000h	ROM CODE 32 K	N/A

Figure 7-1. DRAM memory map.

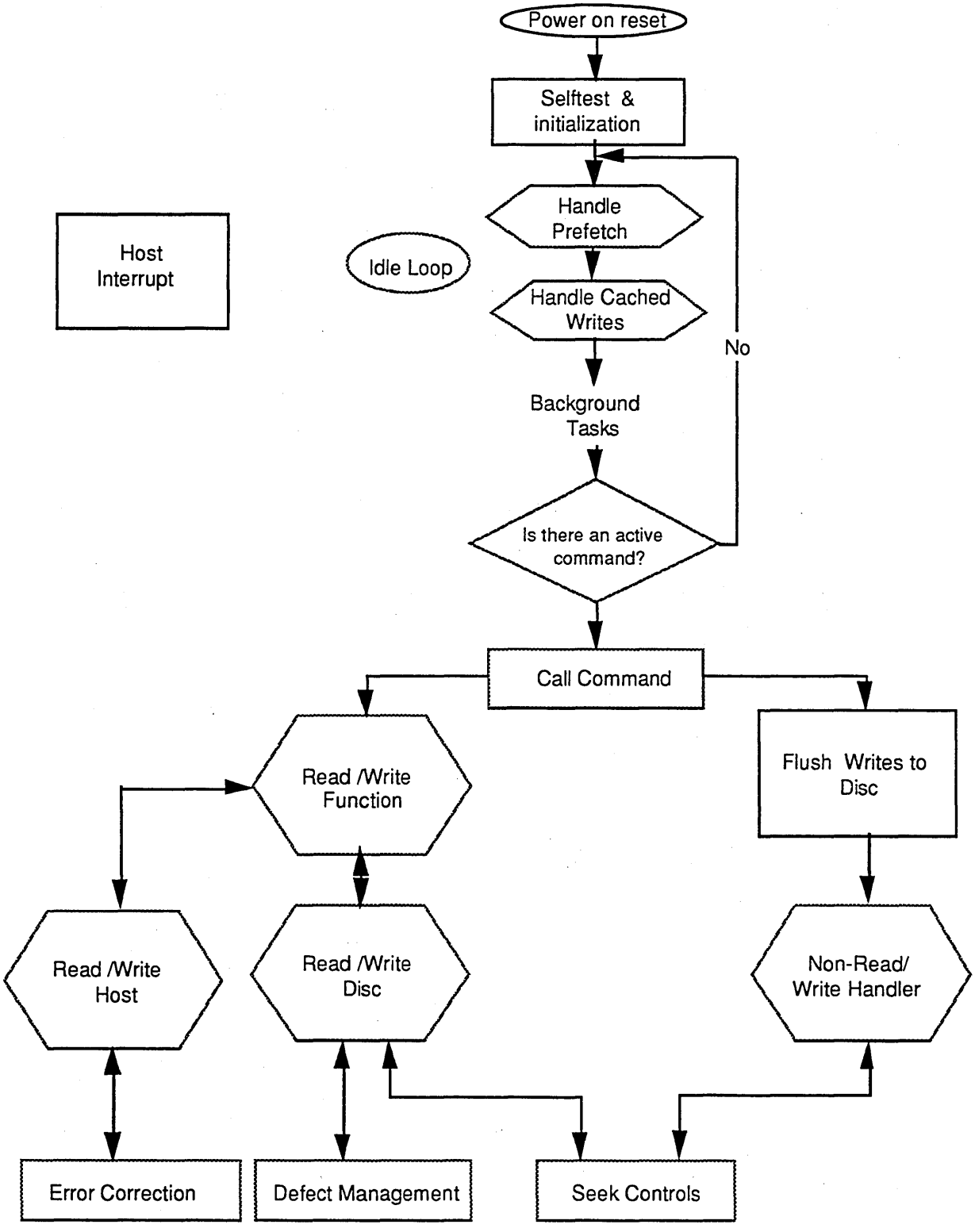


Figure 7-2. Firmware organization.

Section 8 Servo Design

8.1 General Description

Vortex servo is a high performance embedded sector servo system. It is designed to utilize the foremost performance dynamic allowed with adequate self calibration and adaptability to margin parameters and stochastic process variance in the servo system.

The read/write head position feedback transducer system is a scheme of regularly spaced multiple servo sectors embedded into the plural concentric circular data tracks about the rotational axis of the disk. Such servo sectors constitute a constant regular periodic discrete position information feedback to the servo system as the disk is spun at a constant rotational revolution per minute speed.

Any read/write head to position transducer offset is eliminated by the virtue of the transducer position information it derives from the read/write head and part of the data tracks itself.

Since maximizing the data capacity per track by reducing the number of servo sectors per concentric track is contrary to the requirement of the servo to have higher sample rate to improve its TMR performance and to facilitate higher TPI for areal density, the servo design has to utilize all the hardware and microprocessor resources available to achieve the best TMR with the lowest sample rate in conjunction with the rest of the system dynamic limitations.

Also, special considerations are made in the design to minimize the effect of the mechanical resonances, and to minimize the acoustic noise emitted during accessing.

8.2 Servo System Parameters

Components or parameter	Vortex Spec	
TPI	4298.00	track/inch
# of cylinders	5670	cylinder
# of sector/rev	96.00	sector
Spindle speed	3599.50	RPM
Sample period	173.61	µsec
Alias frequency	2879.63	Hz
Arm radius to head[1]	2.829	inch (Pending)
Inertia[2]		
(2 head)	120	gm-cm^2 (Pending)
(4 head)	130	gm-cm^2 (Pending)
Torque constant[3]		
(2 head/ 4 head)	0.1081	Nm/amp (Pending)
Acceleration factor		
(1 disk)	9008	1/(amp-sec^2)
(2 disk)	8315	1/(amp-sec^2)
Coil resistance (@ 25°C)[4]	11.28	ohm
Max head velocity	89.6	in/sec
Power amp gain[5]	0.0002354	amp/bit
Coil inductance[6]		
(1 disk)	1.2	mH
(2 disk)	1.2	mH
Max voltage[7]	11.5	volt

Table 8-1. Servo related parameters.

Notes to Table 8-1:

1. The distance from actuator pivot to read/write head gap is measured by Quality Assurance X-Y table and caliper measurement.
2. Inertia is measured by means of the Torsion pendulum method.
3. Torque factor is measured by applying a constant current to voice coil and measuring the torque on the actuator across the ID-to-OD band. The currents applied are ± 100 mA, ± 200 mA, and ± 300 mA respectively for each measurement.
4. Coil resistance is measured by means of a Digital ohmmeter.
5. Gain of DAC stage included.
6. Coil inductance is measured by means of a Digital impedance meter.
7. Available @ Power amp outputs w/ nominal 12 volt supply.

8.3 Servo Wedge Format

Figure 8-1 shows Vortex servo wedge format. Every wedge consists of four separate fields: (1) Automatic Gain Control (AGC)/Sync field, (2) Servo Address Mark (SAM) field, (3) Track Number, and (4) Burst area. Since a Phase Lock Loop (PLL) is not used in the servo wedge area, time discrimination is used. Timing for all four fields is generated from the same crystal reference. This clock has a period of 25 nanoseconds, and will be referred to as T.

Data is encoded in the following manner:

Servo Data Bit "0" = 10 000 010 0,

Servo Data Bit "1" = 10 010 000 0,

Since each digit has T width, the length of a Servo Data Bit is 9T.

1. The AGC/Sync field consists a default 2T (3T optional), and is used by the Read/Write channel to acquire the proper amplitude for the encoded track number and position bursts. It is also used to synchronize the raw data pulses in order to detect SAMs. The total length of the AGC/Sync field is 60T + 42T = 102T.

2. The SAM follows the sync field. It consists of a default 14T (9T optional) repeated twice, followed by a servo data bit 0. Following the servo data bit 0 is either a servo data bit 0 or 1, which is also known as the index bit. If a one is decoded, then an index pulse is generated. The total length of the SAM field is 27T. (46T optional)

3. Following the index bit is the track number. The track number is a 13-bit Gray coded number. The Gray code to binary conversion is done in the Servo Controller module of the Disk Controller and Host Interface ASIC. Each Gray code bit is encoded as servo data bits. The total length of the track number is 117T.

4. Following the track number is the burst area. There are three bursts per servo wedge time, a Bburst followed by the A burst, and finally the C burst. When on track, the A and C burst will be equal at half amplitude, with the B burst at full amplitude for even tracks, and zero amplitude for the odd tracks.

   The A, B, And C bursts are each 48T long. There are DC erase areas of 9T before and post burst gap of 27T after , giving a total time of 180T for the burst area.

The Servo Controller module reports status to the microcontroller when it detects errors in the servo wedge. The errors include missing Syncs, missing SAMs, error reading Gray code, and Speed error (i.e., SAMs detected outside the ±0.25% speed tolerance window). When a missing Sync or SAM condition is encountered, the Servo Controller module sets its timer to a known value. This is to compensate for the elapsed time lost while looking for SAMs. This way, the servo burst can continue to be sampled, and the servo wedge will still terminate correctly. The servo firmware, however, will be aware of this condition and acts accordingly depending on the error type and any error from previous samples.

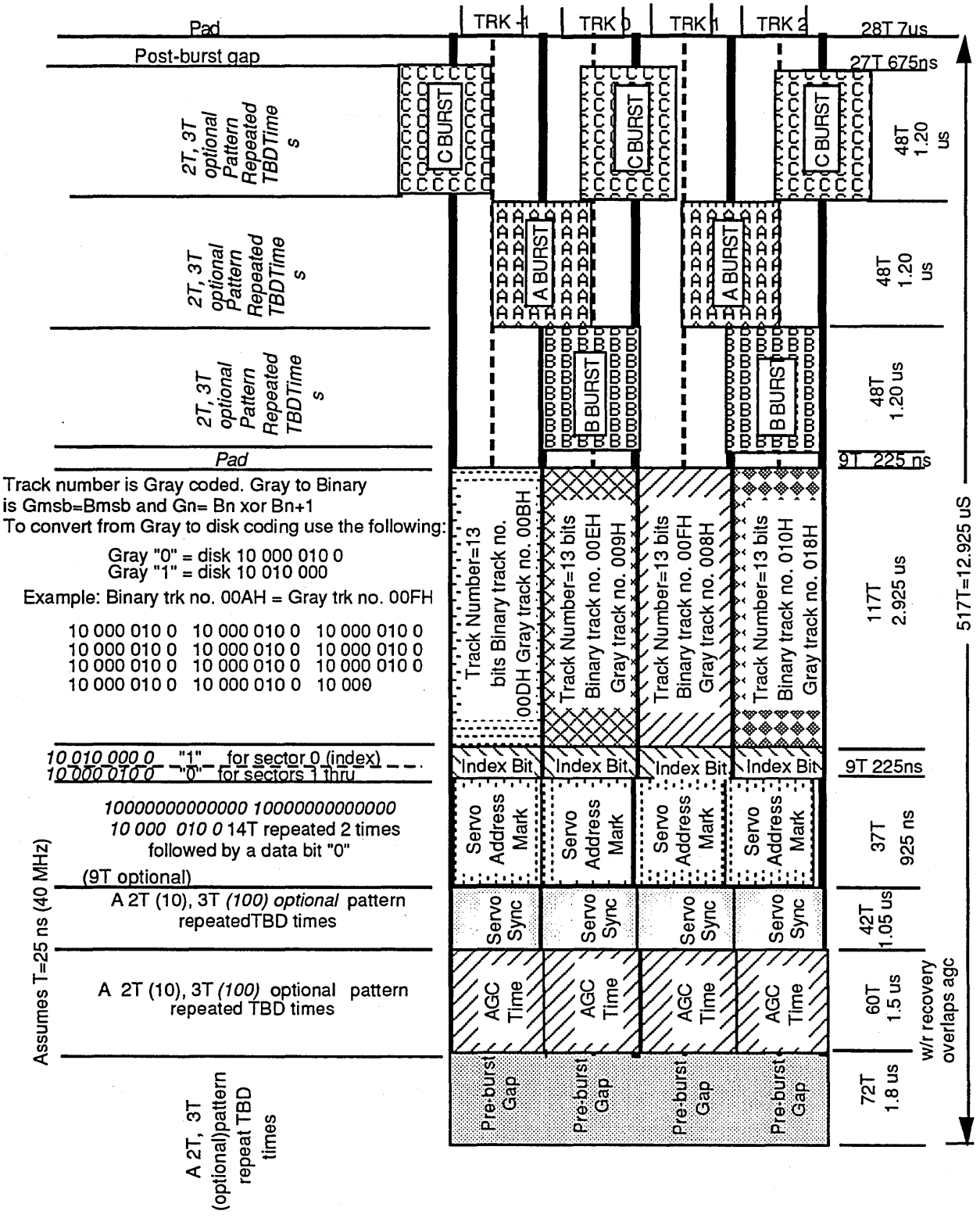


Figure 8-1. Servo Wedge Format

8.4 Servo Electronics

8.4.1 Peak Detect Channel for Servo Bursts

The peak detector channel extracts the amplitude of the A, B, and C Bursts from the servo wedges. A weighted average Peak and Hold circuit, which resides in the Read/Write ASIC, was implemented. During Seek and Coarse Settle modes, the A and B bursts are used. During Fine Settle and Track-Follow modes, the A and C bursts are used. During calibration A,B +C bursts are sampled. The gate inputs to the peak detector, and the control of which bursts are sampled, are sent from the Servo Controller module of the Disk Controller and Host Interface ASIC. The timing of these gate inputs (i.e., delay to start and duration) is programmable.

The analog average output of the servo bursts are converted to digital format via the eight-bit Analog to Digital Converter (ADC). This ADC is also part of the Servo Controller module in the Disk Controller and Host Interface ASIC. The servo firmware reads the digital burst value to determine the actual head position.

8.4.2 Actuator Driver

The actuator driver consists of two components: the PWM filter, and VCM driver. The Disk Controller and Host Interface ASIC puts out a 6-bit plus 5-bit PWM with 4 x oversample output which are summed externally to provide 13 bits to control the magnitude of the VCM coil current . The PWM value is received from the microcontroller, under the direction of servo firmware.

Since these PWM signals are power-supplied by an on-board voltage regulator , power supply variations do not affect the servo gain at all. In addition, all voltage references in the servo section are derived from the on-board voltage regulator in order to ensure that the servo gain is not affected by power supply variations.

The low-pass filter, used for extracting the DC component from the summed signal, is a three-pole Butterworth type. The -3 dB cutoff of the LPF is set at 30-50 KHz, and the attenuation at the PWM beat frequency (1.25 MHz) is about 80 dB; hence, no ripples are observed at the input of the preceding VCM driver.

8.5 Modes of Operation

The servo has three primary modes of operation:

1. Seek mode
2. Settle mode
3. Track follow mode

8.5.1 Seek Mode:

The task of the servo while in seek mode is to move the read/write head as fast as possible from one track to another. The seek mode actually ends just short of the target track where control is transferred to the settle mode. The seek mode must end with the head sufficiently under control that the settle mode firmware can easily deliver the head to the center of the target track.

For most seeks the seek mode firmware passes through three phases called (1) acceleration, (2) deceleration, and (3) linear range. During all three phases the servo is using a state estimator - a firmware model of the electrical and mechanical hardware - to estimate the velocity of the head. This "estimate" is actually a good measure of the head velocity. The servo compares the estimated velocity to a pre-determined desired velocity that is computed based on the number of tracks left to go to get to the target. This pre-determined function of velocity versus tracks to go is roughly parabolic in shape. It is designed to move the head as fast as possible within the constraints of the electrical and mechanical components and their tolerances over time and temperature.

During the acceleration phase, the servo determines that the estimated velocity is still far below the desired velocity so it just applies full power to the VCM. The estimator used in this phase is different from the one used in the other phases because the electrical and mechanical hardware must be modeled differently when full power is applied to the VCM.

When the servo finds that the difference between the estimated and desired velocities is small, it switches to the deceleration phase. As the head gets closer to the target track, the desired velocity decreases. The servo works to keep the error between the estimated and desired velocities small by using both velocity error feedback and a "feed-forward" value fed directly into the control output.

When the head reaches a predetermined number of tracks to go, the servo switches to the linear range phase. In this phase the desired velocity as a function of tracks to go is a straight line. This is less aggressive than the parabolic shape used in the deceleration phase and allows for a smoother transition into the settle mode which follows.

During both the decelerate and linear range phases the control output is offset by a value proportional to the bias force acting on the actuator which holds the read/write heads. This bias force is primarily due to the action of the flex cable attached to the actuator. The bias force estimate used here comes not from the estimator but from a bias force profile versus head position that is initialized when the drive is powered up and updated whenever the head is sitting on track.

For seek lengths below about 100 tracks the seeking process just described does not work too well. Therefore, for seeks of about 20 to 100 tracks, the servo does not go through the accelerate and decelerate phases. The entire seek is done in linear range mode. For even shorter seeks, those below about 20 tracks, the servo skips the seek mode altogether and goes directly to settle mode.

8.5.2 Servo Architecture Block Diagram: Linear Range Seek Mode

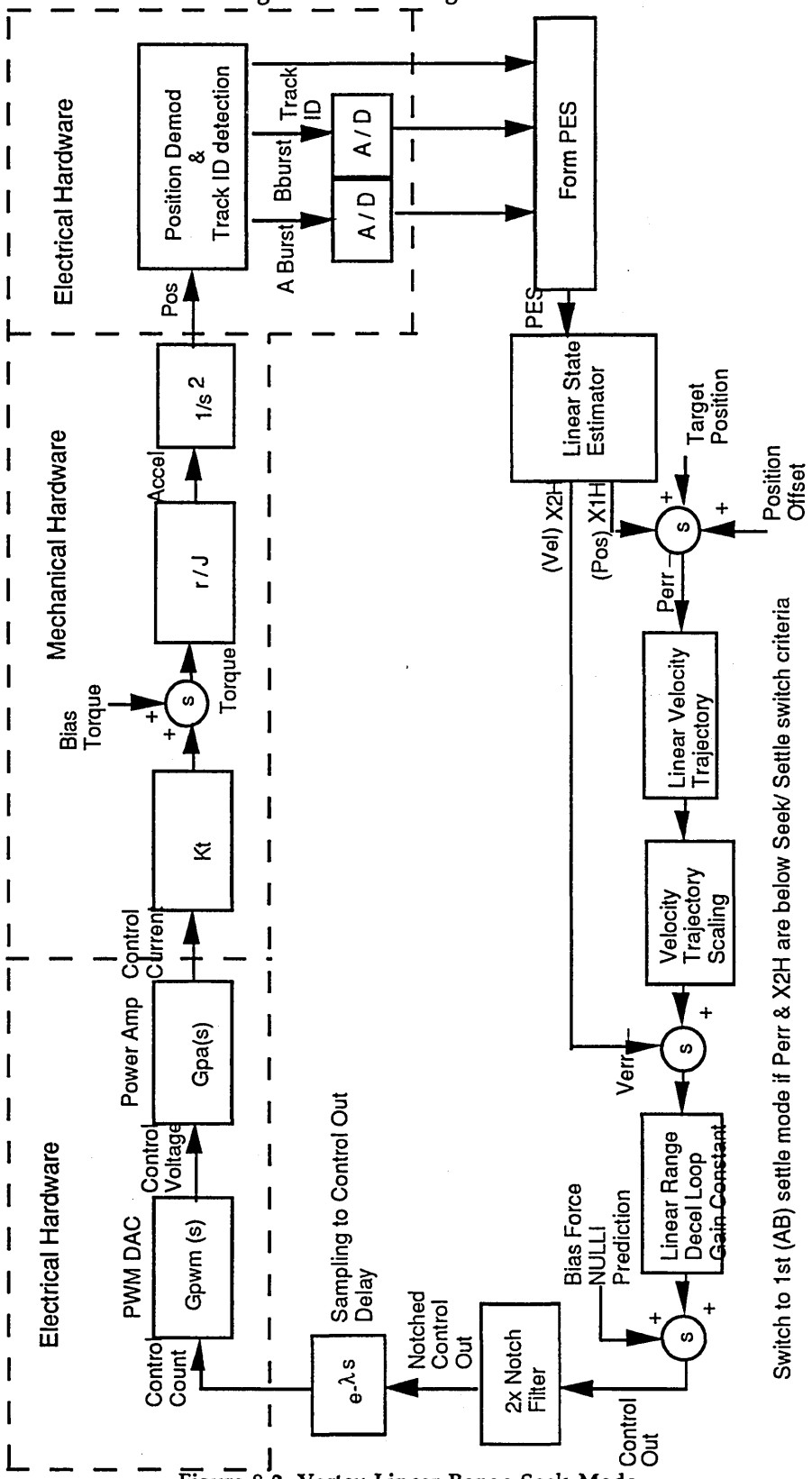


Figure 8-2. Vortex Linear Range Seek Mode

8.5.3 Servo Architecture Block Diagram: Long Seek Mode Acceleration Phase

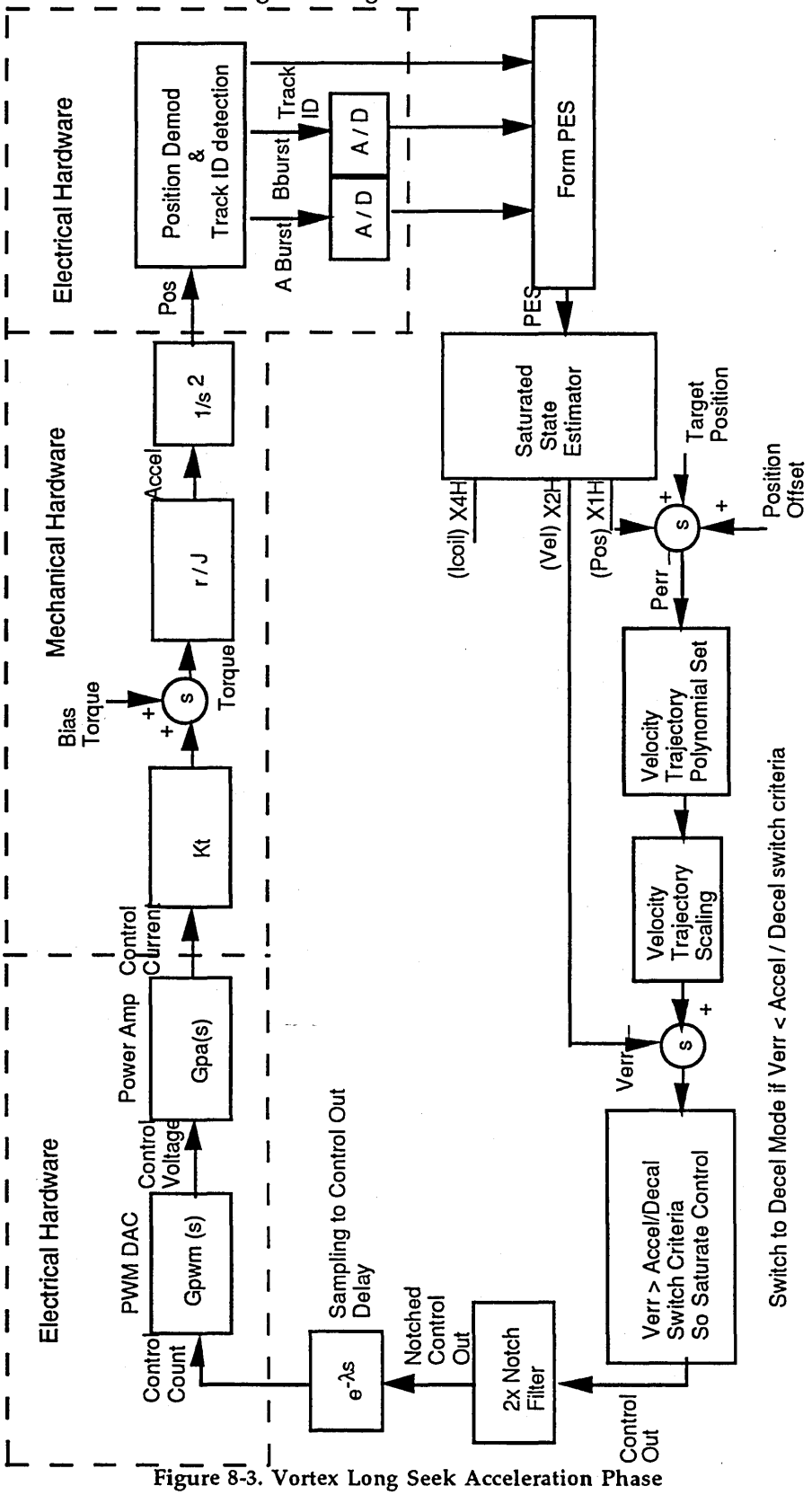


Figure 8-3. Vortex Long Seek Acceleration Phase

8.5.4 Servo Architecture Block Diagram: Long Seek Mode Deceleration Phase

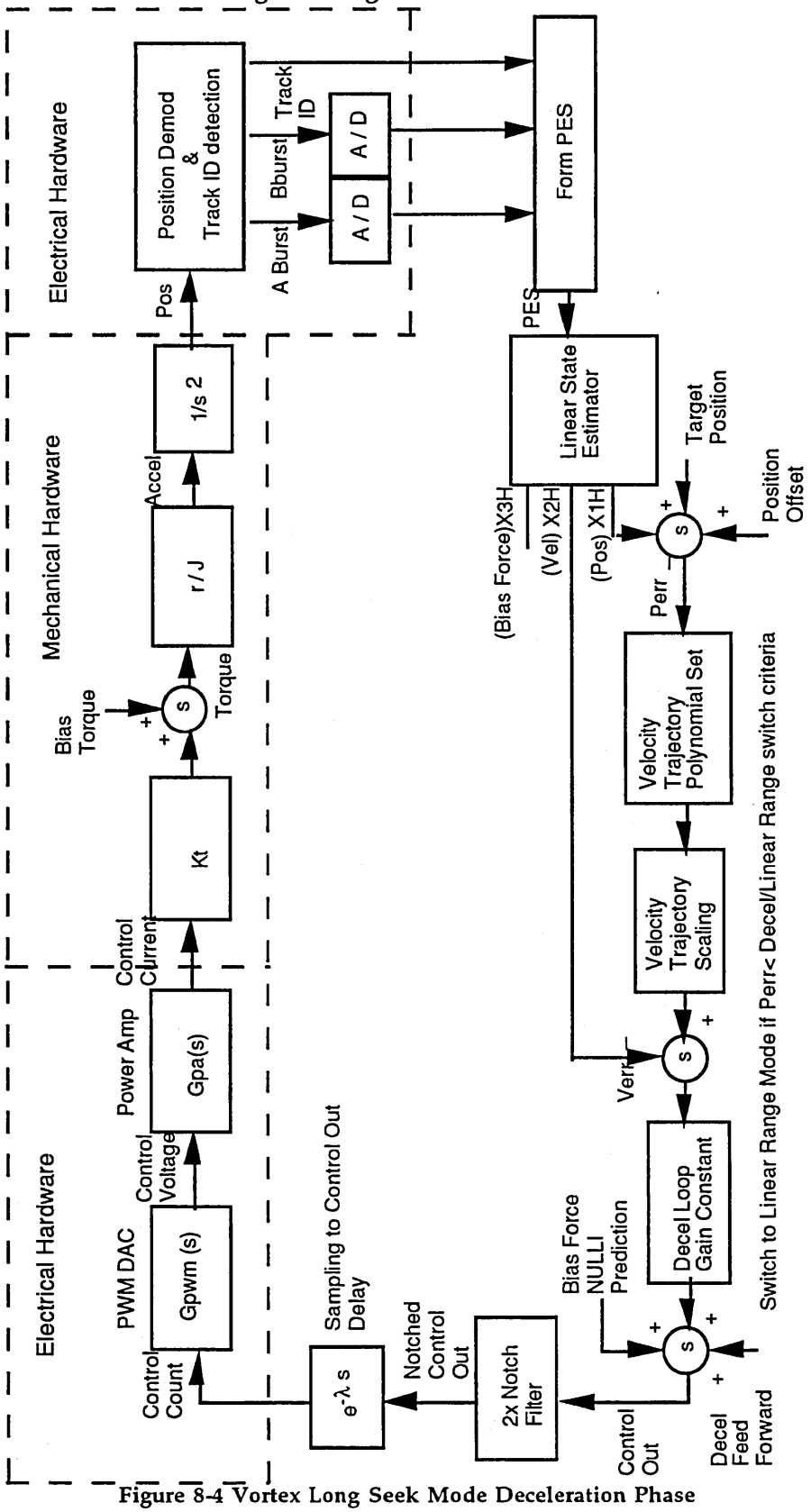


Figure 8-4 Vortex Long Seek Mode Deceleration Phase

8.5.5 Servo Architecture Block Diagram: Short Seek Mode Acceleration

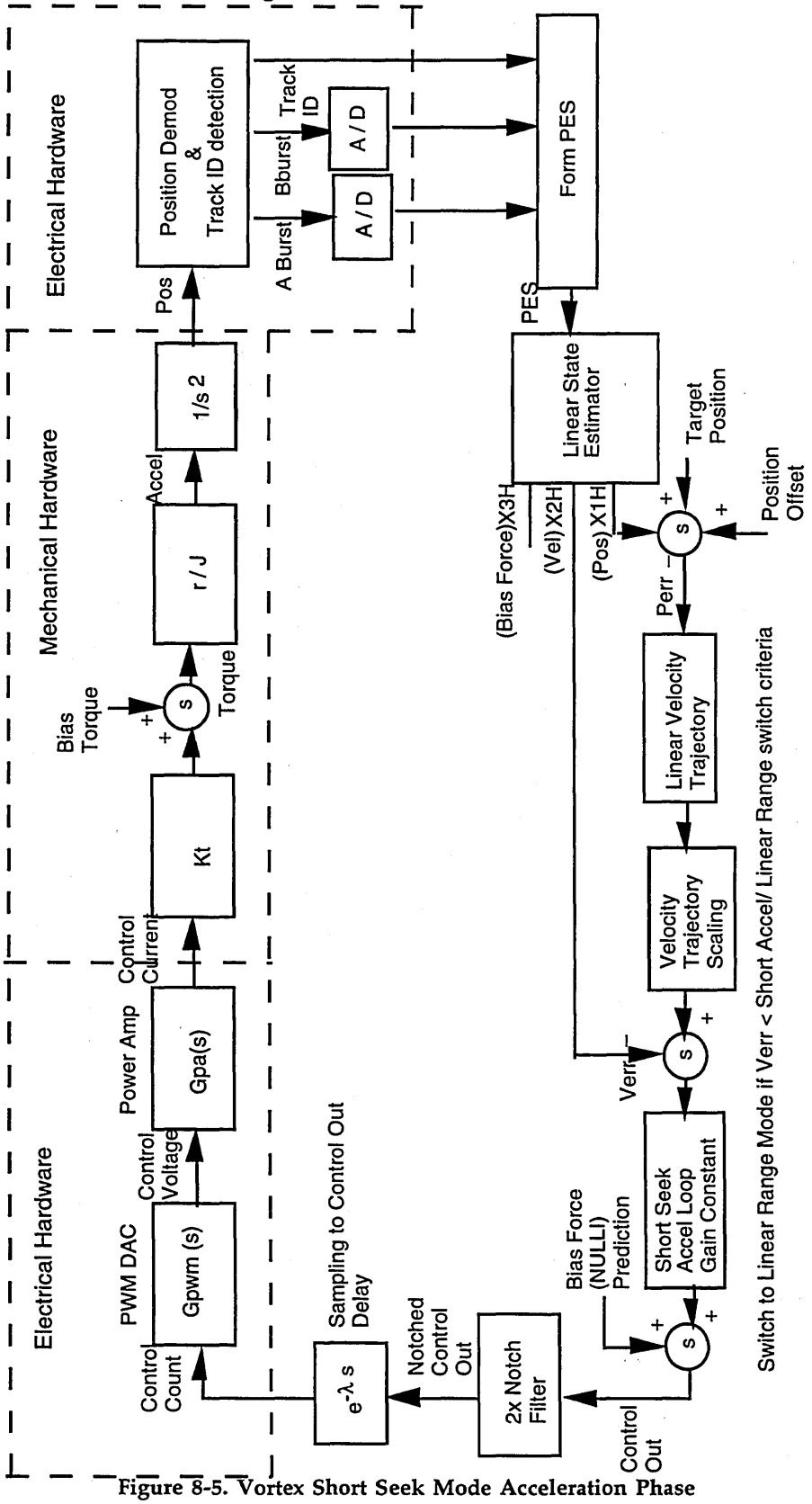


Figure 8-5. Vortex Short Seek Mode Acceleration Phase

8.5.6 Settle Mode

When the servo switches from seek mode to settle mode it begins controlling with position error feedback instead of velocity error feedback. At first it still uses position information from the A and B bursts as it did in the seek mode. The A and B bursts must be used for constant linear position information until the head gets close to the track center - within about 25% of a track width. After certain position and velocity criteria are met the servo begins using the difference between the A and C burst amplitudes for its fine positioning information. Additional sets of tighter position criteria must be met to turn on the track following integrator and later to allow writing to occur. Reads are allowed a little earlier since their is no downside to attempting to read as soon as is reasonably possible.

8.5.7 Track Follow Mode

In track follow mode the servo block diagram is identical to what it was in the late stages of settling. The servo-mechanical open loop transfer function crosses through zero dB at about 350 Hz. It has about 38 degrees of phase margin and about 6 dB of gain margin. While track following, the servo firmware continually checks for errors in the "digital" servo wedge information read off the disk: the sync pattern, the servo address mark (SAM) pattern, and the track address. It can tolerate a single occurrence of these types of errors. If it sees two in a row it will disable writing and begin a recovery process. The servo also detects if the head has moved more than 10% off track or if the spindle speed has gone more than 0.3% away from its nominal value. In these cases writing will be disabled and a recovery process will begin immediately.

8.5.8 Servo Architecture Block Diagram: Track Follow & Settle Mode

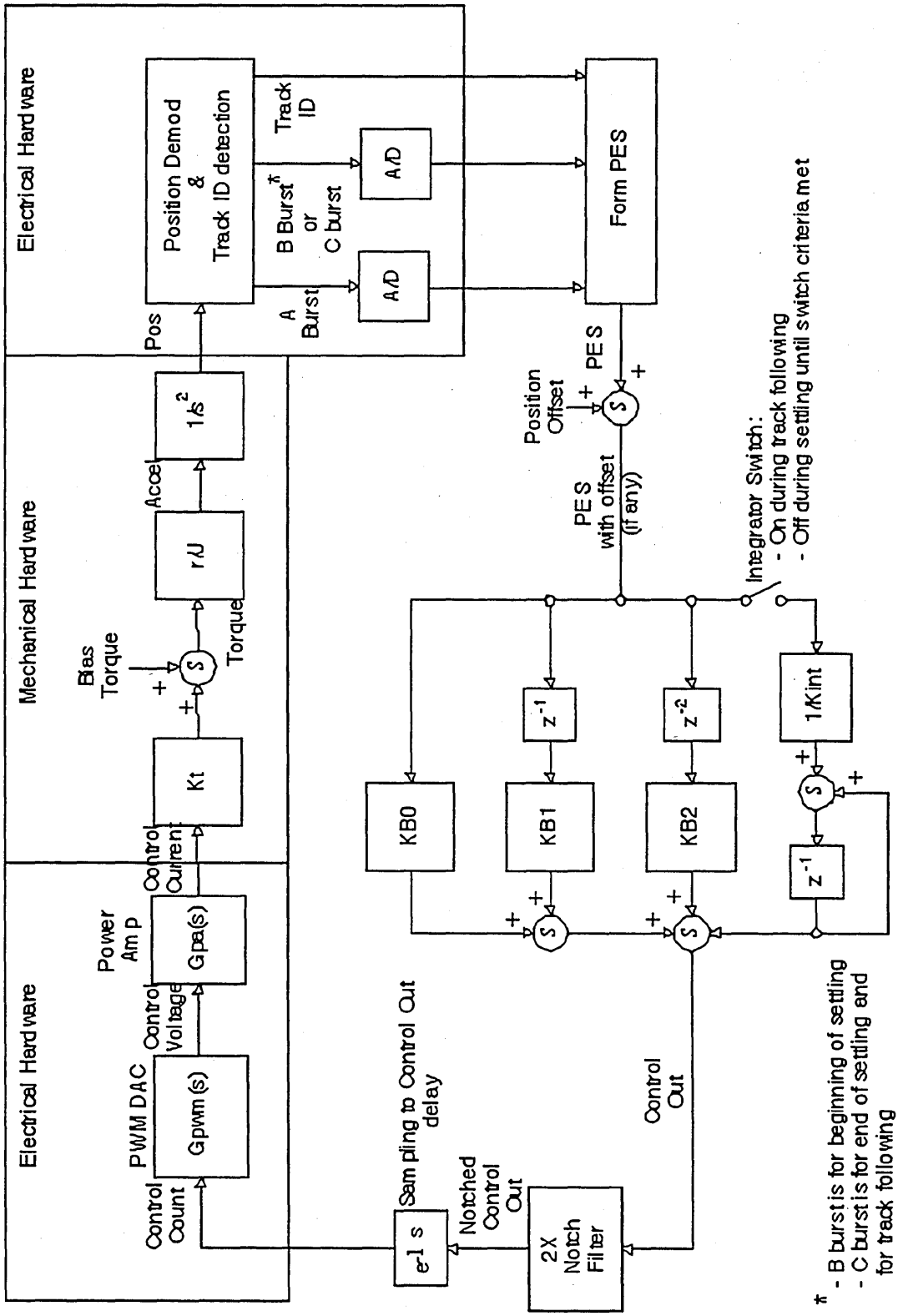


Figure 8-6. Vortex Track Follow & Settle Mode

8.6 Servo Error Recovery

Servo errors can be classified into two types: self-recovered servo errors, and fatal servo errors. Self-recovered servo errors are errors that the servo can recovered by itself without external interference. Examples of these errors are missing Syncs, missing SAMs, bumps, speed errors, and servo defects. Fatal servo errors require recalibration to bring the servo back. This is the case when a seek time-out or offtrack time-out occurred, or when servo lost locks to servo signal from the disk (five consecutive missing Syncs/SAMs or Speed errors in a row).

8.6.1 Self-recovered Servo Errors

The way servo firmware handles this type of errors has been discussed in the Servo System Control Modes section. The background code that monitoring the servo simply has to report to the host the recovered error that servo has found.

8.6.2 Fatal Servo Errors

When a recalibration is required to recover from a fatal servo error, four retries are allowed. The first three retries uses the short recalibration, and the last retry uses the long recalibration.

Short Recalibration

In this recalibration, the servo interrupt is disabled, the read/write channel is re-initialized, and the actuator unpark operation is performed, followed by track lock by servo. V_Scale adaptation is also done, but only four full stroke seeks in each direction allowed. The seek back to the original head and cylinder is then executed. Each short recalibration process and the seek back takes about 250 msec to complete.

Long Recalibration

This calibration extends the short calibration to include the PES Gain calibration and Bias Forces calibration. It takes about 1.5 seconds to complete this recalibration to re-position the actuator to the original head and track.

8.7 Servo Error Budget

TMR ITEMS	PROPOSED	
	-3 SIGMA	+ 3 SIGMA
NRRO (No vibration)	TBD	TBD
NRRO(under vibration)	TBD	TBD
NRRO (under shock)	TBD	TBD
Settling, Read Ready	TBD	TBD
Settling, Write Ready	TBD	TBD
Servo Dither	TBD	TBD
Servowriter DC Error	TBD	TBD
Servowriter AC Error	TBD	TBD
Elastic Thermal Disk Shift	TBD	TBD
Perm.Thermal Disk Shift	TBD	TBD
Actuator Dither (under vibration)	TBD	TBD
Actuator Dither (under shock)	TBD	TBD

Table 8-2. Error Budget.

Notes to Table 8-2:

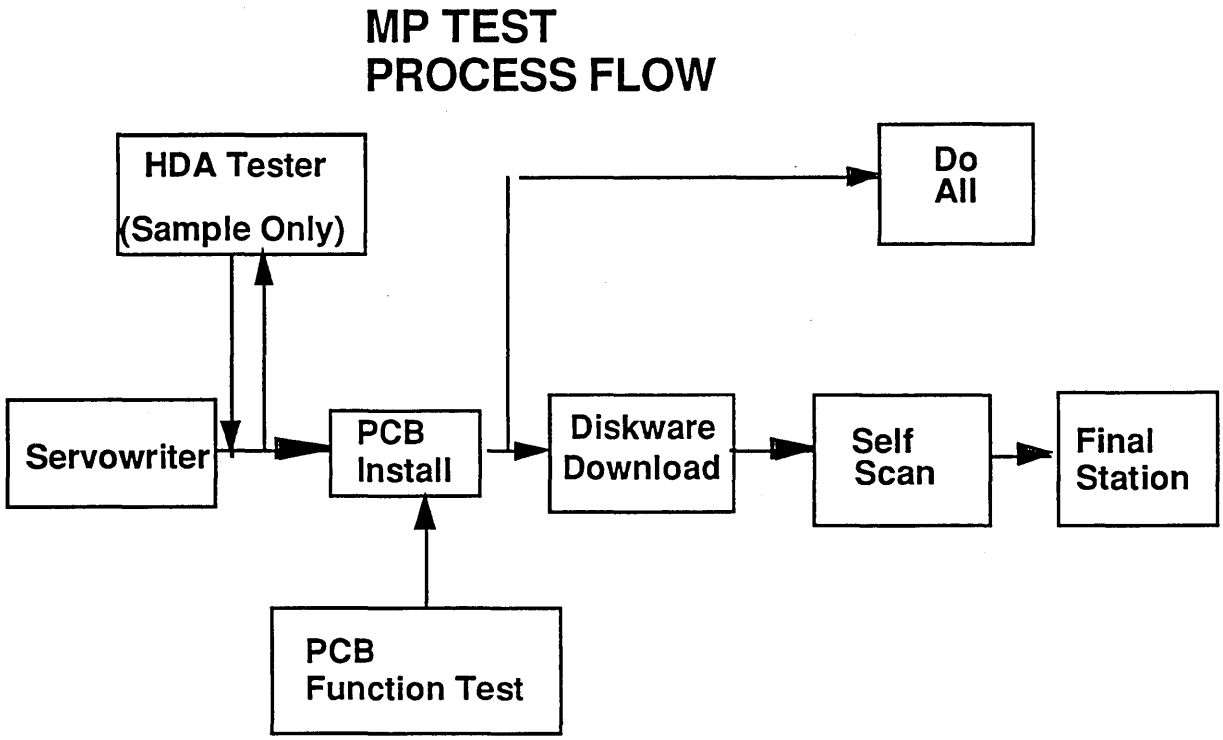
1. All distributions above were approximated from actual data or simulation studies.

2. -3 sigma to + 3 sigma contain (or hold) 99.74% of total histogram, and histogram not necessarily Gaussian distribution.

Section 9 Test Plan

9.1 Process Flow Summary

The illustration below shows the physical flow of the HDA, PCB and assembled drive from Servowrite through Final Station at mass pro.



Test Process (Mass Pro) Detail

The Do All station can be run, at manufacturing's discretion, as an alternative to the combination of Diskware Download, Self Scan and Final Station. Use of the Do All station reduces labor and manufacturing floor space requirements by eliminating two handling steps but requires more chamber capacity.

It is anticipated that MKE will employ a mix of both process flows until sufficient chamber capacity is on-line to implement 100% Do All Stations.

Refer to the process test plan contains details on all the tests, and all the builds.

9.2 Servo Writer Station

The Vortex Servo Writer uses a push-pin mechanism to write the servowedges with the cover on the HDA. The servowriter writes wedges on each track of each surface. It uses a laser positioning system to control the precise radial placement of the servowedges. It uses a clock head to control the circumferential placement of the servowedges.

After writing the servowedges on all cylinders, it verifies the integrity of the wedges. In verify mode, the head is positioned at the track center of the outermost track, and then moved in one track increments to each successive track center, using the laser as the position reference. Checks are made of the amplitudes of each servo burst against the minimum and maximum amplitude required for the drive AGC and servo to operate. Also, a check of the encoded track number, and of the Sync and Servo Address Mark (SAM) fields are made. The total stroke of the actuator (crash stop to crash stop) is checked. The number of tracks which are verified is reduced after mass pro as the product maturity improves.

9.2.1. Barcode S/N

9.2.2. Initialize

9.2.3. Motor Speed

9.2.4. Parametric
- 9.2.4.1. Track Average Amplitude (TAA)
- 9.2.4.2. Resolution
- 9.2.4.3. Positive and Negative Modulation

9.2.5. Find OD Crash Stop

9.2.6. Measure Stroke

9.2.7. AirLock

9.2.8. Write Clock Track
- 9.2.8.1. Write Servo Wedges
- 9.2.8.2. Write Normal Pattern
- 9.2.8.3. Write 3 Times Sample Rate
- 9.2.8.4. Write HDA S/N and Servowriter Id/Date/Time

9.2.9. Verify Servo Wedges
- 9.2.9.1. Track Tests
- 9.2.9.2. Wedge Tests
- 9.2.9.2.1. A/B/C Burst Verification
  AGC Field Verification
  A+C to B Verification
  TNA Check:
  Wedge PES Verification

9.2.10. Spin Down

9.2.11. Generate TEST.OUT

9.3 PCB Test

The purpose of PCB Function Test is to screen out PCBs, with workmanship problems or defective components, before drive level testing. In addition, some functions which can not be tested with existing drive test hardware are included in the PCB function test sequence. This is truly a functional test in that no environmental stress, such as elevated temperature or voltage margining, is applied.

This test is run on a slave HDA, using pogo pins to connect with the PCB under test and the PC. The slave HDA is taken from a drive which has passed the drive test process and is trained in all zones. Pogo pin connections are made to the following points:

← 16 to the flex circuit connector (from below).
← 4 to the motor connector (from below).
← 4 to the power connector (from above).
← 40 to the AT connector (from above).

To accomplish the DMA test for AT, the cable interface board is modified to short the REQ and ACK lines. Note these lines are both ground on the SCSI cable.

This test is run on every PCB. The following test steps comprise the PCB function test sequence.

9.3.1. Power Up/Detect

9.3.2. Read/Write Test

9.3.3. RAM Test

9.3.4. Seek Test

9.3.5. DMA Connectivity Test (A/T Only)

9.4 HDA Test

The HDA Test will be done on an as needed basis during mass production. It will be used to monitor the consistency of parametric distributions resulting primarily from the head/disk interface, investigate yield problems and evaluate process changes to incoming heads and media.

The HDA Tester consists of a 486 PC operating a LeCroy 7200A (Digitizing Oscilloscope) through a GPIB port. The HDA under test is connected to the LeCroy via a captured product board and converter board.

Since the LeCroy 7200 is a digitizing oscilloscope, there are practical limitations on the amount of sample points which can be stored and analyzed in a reasonable amount of time. As a result, the data sample for the parametric tests is gathered by looking at a "segment" of the wedge to wedge data area between the 96 servo wedges.

The tests which are performed by the HDA Tester are organized below by the read/write patterns they employ. Any of these tests may be run in any or all zones depending on the requirements of the program.

9.4.1. System Initialization
- 9.4.1.1. HDA Spin Up
- 9.4.1.2. Verify and Reset LeCroy Scope
- 9.4.1.3. Check LeCroy Configuration

9.4.2. Load RAM Ware
- 9.4.2.1. Auto Detect
- 9.4.2.2. Write Buffer
- 9.4.2.3. Modify Config page 16
- 9.4.2.4. Load Page 10 and 17
- 9.4.2.5. Read Drive Serial Number

9.4.3. HF and LF Frequency Testing
- 9.4.3.1. Amplitude Calibration
- 9.4.3.2. HF TAA
- 9.4.3.3. Amplitude Variance
- 9.4.3.4. LF TAA
- 9.4.3.5. Resolution
- 9.4.3.6. Modulation
- 9.4.3.7. Overwrite Test
- 9.4.3.8. Phase Distortion

9.4.4. Isolated Pulse Testing
- 9.4.4.1. PW50 Test

9.4.5. Pseudo Random Pattern Testing
- 9.4.5.1. Non Linear Transition Shift
- 9.4.5.2. Signal to Noise Ratio

9.5 Diskware Station

On the Vortex drive, firmware is partitioned and stored in two different locations. The portion of the firmware which allows the drive to accomplish basic operations (such as motor control and servo control) are stored in the Read Only Memory (ROM) on the CPU while the remainder is stored on the system cylinders on the disk. When the drive is powered up, the firmware which is stored on the disk (Diskware) is loaded into buffer memory and a complete set of firmware is available for the drive to operate. In this way most of the firmware can be stored on the disk. This allows a cost saving to be achieved by using a smaller ROM.

The Diskware Download Station sets up the drive to begin the test process. This is accomplished by loading firmware onto the drive, preparing the system cylinders to receive data and then writing the diskware blocks and some basic files required for the drive to function. It also writes a Self Scan "script" to a special sector on one of the drive's negative cylinders. With the self scan script loaded, the drive will automatically execute the self scan sequence the next time it is powered up. The cycle time is the same for the 1 disk and the 2 disk versions.

The following sequences comprise the diskware download process.

9.5.1. Power Up

9.5.2. Load RAM Ware
- 9.5.2.1. Detect
- 9.5.2.2. Write Buffer
- 9.5.2.3. Load Config Page 10 and 17
- 9.5.2.4. Interrogate Drive
- 9.5.2.5. Read Drive Serial Number

9.5.3. Stability Margin Test

9.5.4. Format System Cylinders
- 9.5.4.1. Format
- 9.5.4.2. Reload RAM Ware
- 9.5.4.3. System Cylinder Training
- 9.5.4.4. Reformat System Cylinders
- 9.5.4.5. Load SCSI Mode Pages
- 9.5.4.6. Defect Scan

9.5.5. In Line Spare

9.5.6. Load Diskware
- 9.5.6.1. Write Configuration Pages
- 9.5.6.2. Initialize Defect Lists
- 9.5.6.3. Write Format File
- 9.5.6.4. Write Buffer Download

9.5.7. Power Cycle Test

9.6 Load Self Scan Script

Self scan is a self-contained series of process and test sequences which comprise the core of the complete drive test sequence. As many attributes of the total drive test sequence as possible are implemented in self scan.

Self scan is run using self scan firmware and requires only power to be applied to the drive. The self scan firmware is written on the drives negative cylinders at the diskware download station. An ASCII file called a script is used to control the test sequence. It is also loaded at diskware download.

Since the application of drive power automatically starts the self scan sequence, a password is used to enable or disable the automatic execution of the test. The password is disabled at the completion of the self scan test.

The drive, operating under its own control, executes a series of operations designed to verify the drive's functionality, calibrate the servo system, train the read channel and "map out" defects in the media.

Media defects are identified using digital defect scanning techniques. Defect locations are discovered quickly by adding stress to the read channel while simultaneously disabling its ability to do error correction. Self Scan will produce a defect map that will be used during factory format for sector relocation and defect sparing.

The Self Scan test is conducted in a high temperature (50°C) environment to simulate a worst case operating condition for the drive.

Each routine saves test and process data to cylinder -1. The data is read and manipulated by the host computer at final station.

The following sequences comprise the self scan process.

9.6.1. Power Up

9.6.2. Buffer RAM Test

9.6.3. Start/Stop Test

9.6.4. Servo Verify Test

9.6.5. Read Channel Training

9.6.6. Write Current Optimization

9.6.7. Write Precomp Optimization

9.6.8. Bandwidth Optimization

9.6.9. TAP4 Optimization

9.6.10. Boost Optimization

9.6.11. TDFE Optimization

9.6.12. Bandwidth Optimization

9.6.13. Performance Test

9.6.14. Head Switch / Single Track Seek Test

9.6.15. Third Stroke Seek Test

9.6.16. Full Stroke Seek Time Test

9.6.17. Random Seek Test

9.6.18. Null Current Test

9.6.19. Runout Test

9.6.20. Wedge to Wedge Scan

9.6.21. Convert Wedge and Servo Defects to CHS Defects

9.6.22. Format Drive

9.6.23. Physical Sequential Stress write / read with ECC disabled

9.6.24. Format In line

9.6.25. ECC Test

9.6.26. Start/Stop Test

9.6.27. Customer Scan (Logical Sequential/Random R/W) Test

9.6.28. Sequential Throughput Test

9.6.29. Random Throughput Test

9.6.30. Customer Scan (Confidence and Error Rate) Test

9.6.31. Delete Password

9.7 Final Station

This station is used to test the drive through the interface, and to collect all the self scan information. This is the only test in our process where we are able to simulate a customer environment. At this station, we should only be testing the things which can't be tested at self scan. The faster the host system, the more complete the testing we can perform. Do to manufacturing considerations, this test should be limited to less than 5 minutes.

The following sequences comprise the final station process.

9.7.1. Servowriter Report

9.7.2. Self scan Report

9.7.3. Start/Stop Test

9.7.4. Full Compare Test

9.7.5. Bonus Test

9.7.6. Logical Sequential Test

9.7.7. Throughput Test

9.7.8. Configuration

9.7.9. Diskware Version Check

9.7.10 Write Results

Appendix A Schedule and Major Model Milestones

Build	Date	Location	Quantity
E1	06/01/95	Quantum	30
E2	08/28/95	MKE	200
P1	09/28/95	MKE	1,000
P2	12/01/95	MKE	2,500
PMP	01/29/96	MKE	5,000
MP	02/15/96	MKE	Large

Table A-1. Scheduling goals from E1 build through mass production.

H/W Level	E1	E2	P1	P2
Mechanics	• Hog-out base w/ new fixed shaft motor & Soft-tooled actuator shaft tied to top cover.	• Soft-tooled mechanics with proven design implementation.	• Hard-tooled mechanics.	• Pre-Masspro level mechanics.
Electronics	• Form factor PCB w/ Fireball based electronics.	• Select motor driver. • Finalized Servo requirements. • Electrical subsystem supports full process functionality.	• Full function PCB, may not be to spec.	• Full function, full spec PCB.
Head/Media	• Fireball heads w/ ABS optimized for 3600rpm. • W/Tblz, FB suspensions. • Media from Komag, Showa Denka.	• Vortex head w/ chosen suspension from E1.	• Heads meet critical specs & key performance characteristics.	• Pre-MP level performance.
Firmware	• Support test requirement: seek, format, R/W physical.	• Full function not optimized selfscan.	• Full function optimized selfscan.	• Full function optimized selfscan.
Process Test	• Servowriter capability @ QNTM.	• Servowriter capability @ MKE. • Partial process capability.	• Full process capability.	• Full process capability to Spec.

H/W Level	E1	E2	P1	P2
Objective	• Engineering verification of new mechanics, motor, acoustics, resonance. • First pass CSS.	• HDA characterization • Compatibility test.	• DVT • Mfg. process & test process evaluation • Demonstrate drive capacity and meeting error rate at ambient & 50°C • Demo units • Compatibility Test • Customer Test	• DMT • Mfg process & test process validation • Demonstrate drive capacity and meeting error rate at all environmental conditions • Qual Units
Acceptance Criteria	• Complete all bench level testing of major components. • Obtain all head parametric & media magnetic performance. • Establish TMR contributions from the Mech. • Complete EVT1. • Simple self scan demonstrated.	• Complete EVT2. • Acquire head & media performance parameters to finalize P1 criteria. • Establish drive error rate capability. • Validate TMR goals. • Full test process capability demonstrated before P1 build.	• Meet 80% yield • Complete DVT: issues identified & critical design changes made to meet design criteria • Preliminary CSS results for 40K cycles.	• Meet 90% yield • Drive meets all performance specs. • All FMT issues identified and closed prior to PMP build. • Complete DMT.

Figure A-1. Models defined.

Appendix B Standards

Vortex drives will meet the following regulatory specifications:

Underwriter Laboratory (UL)

Vortex drive will meet the current edition of UL 1950, Standard for safety: Information technology equipment including business equipment.

Locked Rotor Test acceptable for UL 1950, No.950 will be included as part of UL Certification.

UL Recognition shall be obtained without any special or unusual conditions of acceptability. A copy of the UL Recognition Report, including Conditions of acceptability, will be provided.

The drive will bear the UL required identification markings which provide proof of UL Recognition. Use of the UL backwards "UR" is preferred.

Canadian Standards Association (CSA)

Vortex drive will meet the current edition of CSA - C22.2 No. 950-M89.
information technology equipment including business equipment.

Locked Rotor Test acceptable for CSA 22.2, No. 950 will be included as part of CSA Certification.

CSA Certification shall be obtained without any special or unusual conditions of acceptability. A copy of the CSA Certification Report, including Conditions of acceptability, will be provided.

The drive will bear the CSA required identification markings which provide proof of CSA Certification.

European standards (VDE and TUV)

Verband Deutscher Electroechnier (VDE)
Technisher Uberwachungs Verein (TUV)

Vortex drive will meet the current edition of EN 60 950. European Community Regulations for safety of Information technology equipment including Electrical business equipment and IEC950, Safety of Information technology equipment including Electrical business equipment. The drive will also meet the requirements of DIN/VDE 0805,Safety specification for business machines.

Locked Rotor Test acceptable for EN60 950 and IEC 950 will be included as part of VDE and TUV approval.

Approval shall be obtained without any special or unusual conditions of acceptability. A copy of the report, License and Construction Data Forms will be provided.

The drive will bear VDE or TUV required identification markings which provide proof of VDE and TUV approval.

CE Mark

The Vortex Product shall meet the requirements as defined in the following directives:

EMC Directive:	89/336/EEC, 92/31/EEC, L 139/19, C 162/7
Low Voltage Directive:	73/23/EEC

Appendix C Packing

General Information

Quantum seeks not only to ship products that provide the latest in technological features, but also to ensure that these products arrive at the customer's site in the same condition that they left our factories.

Shipping Containers

Two (2) sizes of shipping containers will be required for Vortex products. These are:

1. 1-Pack Shipping Container
2. 10-Pack Shipping Container.

The 1-Pack Container hold one (1) disk drive, and the 10-Pack holds ten (10).

* The shipping containers shall be sufficient to protect the parts enclosed, and must comply with the packaging requirements of the latest issue of Uniform Freight Classification Rules, or other applicable carrier requirements.

* The containers are intended for single-use.

* Container sizes should be selected such that when arranged upright on a 4-way 40"Wx48"D pallet, the containers do not overhang the edges of the pallet deck. Containers when arranged on the pallet, should maximize utilization of the pallet deck area and the available 48" load height.

* Closures must permit handling without specific precautions.

* The corrugation used in these containers must have sufficient strength to prevent collapsing of the container under double stacked pallet loads.

Identification

- Each shipping container must be identified on sides #3 and #4 (See Figure C-1) with the following basic information:

  A. Quantum Logo
  B. Symbols to indicate:
  1. The proper orientation of the TOP of the container.
  2. The container contents are FRAGILE.
  3. The container should be protected from water, rain, etc.
  4. The container contents are sensitive to static electricity.

Documentation

- 1-Pack Carton **ASSEMBLY**: TBD

- 10-Pack Carton **ASSEMBLY**: TBD

Packaged Finished Goods Product Shock & Vibration Test Standards

This section outlines the laboratory test levels required to assure the arrival of Quantum Finished Goods (F/G) products to the end user without damage or loss of performance beyond the published specifications. The packaged products must be tested prior to product release to assure adequate protection against the shipping and handling hazards anticipated in the domestic and international distribution network.

- REFERENCE CONDITIONS AND TOLERANCES

  Unless otherwise stated, the ambient conditions of the laboratory and tolerances for test conditions are:

Temperature	23 °C ± 5°C
Humidity	30% to 70% RH (not controlled)
Acceleration	+15%, -5% Peak
Velocity Change	+10%, -2%
Frequency	±0.5 Hz

Table C-1. Assumed ambient conditions and tolerances for test conditions.

- APPLICATION

  This specification shall apply to all Quantum products which are identified with the name "Quantum" and/or the Quantum logo applied to the product regardless of whether the product was fully or partially manufactured and packaged by Quantum or an outside supplier.

NOTE: This test standard is a procedure to assure the maximum values of shock (Critical Acceleration) are NOT exceeded. Also, this standard details the vibration tests required to assure the packaged cushion resonances will NOT damage the Quantum F/G packaged product.

- EXCEPTIONS OR DEVIATIONS

Any exceptions or deviations from the product standards must be approved by the Engineering Product Manager, the Product Marketing Manager and Quality Assurance. Any deviation or exemptions must noted in the Product Plan. Quantum O.E.M. customer and O.E.M. supplier requirements must be reviewed by Quality Assurance prior to contractual finalization by Quantum to avoid both over-packaging and under-packaging of Quantum products.

- FINISHED GOODS PRODUCT TESTS

- Vibration
  a. resonance search / Dwell
  b. resonance endurance - SINE wave
  c. stacked resonance

- Shock: "Free Fall Drop"

- PRE-TEST AND POST-TEST INSPECTION AND FUNCTIONAL TEST

All specimens must be thoroughly functionally tested prior for submission of packaging testing and the characteristic data recorded for comparison with post test data. The product must be visually inspected prior to packaged testing.

After the shock and vibration tests are performed the specimen must be functionally tested to assure the unit is performing to specification. The specimens must be carefully inspected for structural, cosmetic and mechanical damage after shock and vibration tests.

The units under test shall be inspected and functionally tested between each segment of the shock and vibration tests series.

- PACKAGING ACCEPTANCE

If during any segment of the F/G packaged product test the product fails to meet the required functional specifications, or the product has incurred structural damage, or the unit has been cosmetically blemished (other than fixturing markings), the packaging shall be considered "FAILED".

Note: any intermittent problems should be considered "FAILED".

If packaging is considered "FAILED", the system should be rechecked to assure the system under test was not an unreliable sample and more samples must be tested to confirm either an acceptable or non-acceptable sample.

Before final acceptance, the system under test will be "burned-in" for 30 continuous days and retested to assure there are no latent failures introduced in the abuse testing.

- CARTON ORIENTATION

  The cartons are identified by figure C-1.

- VIBRATION TESTS

  - Resonance Search

    Resonance search within a range of 3-200-3 Hz. at a constant acceleration input of 0.5Gs must be performed on three axes of the packaged assembly. An X-Y Log-Log plot must be permanently recorded for each axis tested at each monitoring position. If the packaged unit can conceivable be shipped in a position other than the upright position, all three axes must undergo a resonance search.

  - Resonance Dwell-SINE Wave

    Each potential shipping axis must be endurance tested for a total one hour, 15 minutes per resonant frequency at an input of 0.5Gs acceleration. If the requirement of a full one hour cannot be achieved, the balance of the hour must be performed with the vibration system continually sweeping from 3-200-3 Hz. 0.5Gs constant acceleration input.

  - Pallet Stack, Resonance Endurance Test must be performed with the Finished Goods cartons stacked in the normal shipping orientation in a single column to the anticipated maximum height of a pallet load. For safety reasons, the proper fences (lateral support restraints) must be utilized.

    After each axis is endurance tested, inspect all products in the column stack for cosmetic and structural damage. Then perform a functional test on the unit checking for intermittent or permanent malfunction.

- RESONANCE SEARCH

  The vibration system frequency adjusted for stacked resonance (maximum displacement of the top unit) at an input acceleration of 0.5Gs of the table.

- RESONANCE DWELL

  The endurance test to run a total of 15 minutes at the stacked resonance frequency.

- SHOCK TEST: FREE FALL DROP TEST

  The free fall drop test must be performed using a drop test mechanism which will provide accurate and repeatable drop heights. Also, the mechanism must be able to assure accurate and repeatable package orientation during impacts.

  The acceleration levels must be monitored by the use of accelerometers and the resulting curves permanently recorded on photographs. The levels detected must not exceed the critical acceleration determined by the bare unit damage boundary tests.

- TEST SEQUENCE

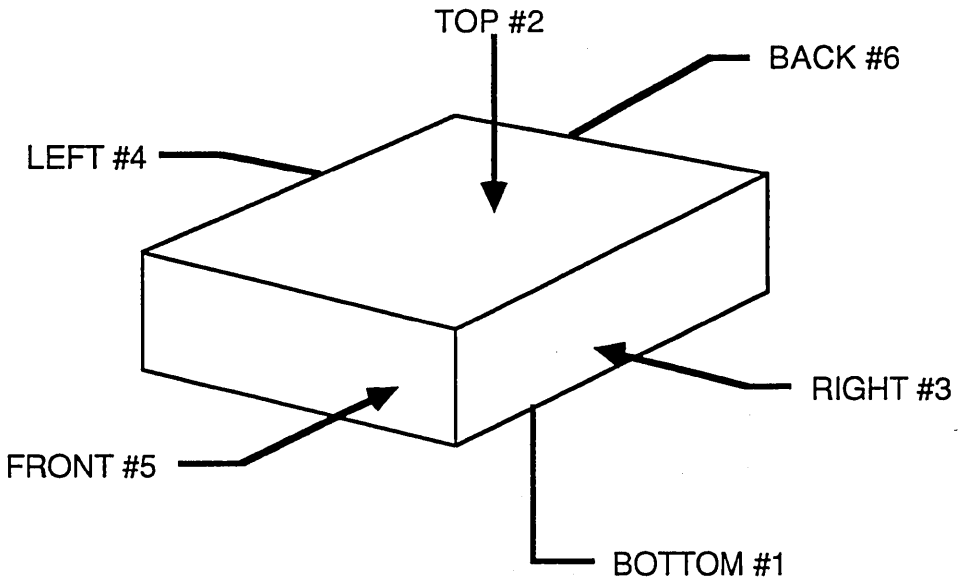


Figure C-1. Vortex carton face identification.

The package product shall be shock tested by dropping the F/G package in the following sequence:

DROP #	IMPACT
1	bottom (1)
2	top (2)
3	right (3)
4	left (4)
5	front (5)
6	back(6)
7	edge (2-3)
8	edge (5-3)
9	edge (5-2)
10	corner (2-3-5)

Table C-2. Free fall drop testing sequence.

- DROP HEIGHTS

Gross Weight	Drop Height	No. of Drops
0 - 20 lbs.	30 inches	10
21 - 40 lbs.	24 inches	10
41 - 60 lbs.	18 inches	10
61 - 80 lbs.	12 inches	10
81 - 200 lbs.	6 inches	10
200 lbs. and above[1]	15/9 inches[2]	1/5

Table C-3. Drop heights required for F/G Quantum products

Notes to Table C-3:

1. If the F/G items are unitized (palletized), 10 impacts at 9 inches are required on the bottom orientation only.

2. First number is the base or bottom drop, second number is the drops on all other surfaces.

After drop testing the product, reinspect for structural and cosmetic damage. Also retest for intermittent and permanent functional malfunction. Subject the units run through the shock tests to a 30 day burn-in test before the final functional test is performed.

- COMPRESSION TEST

Floating platen compression test equipment shall be used in this test in accordance with ASTM D-642-76. The test shall be conducted on five (5) identical packages with all internal packaging components and an actual product or dummy load. The average of the five (5) tests shall be used to determine the acceptability of the container/package system.

Compressive forces are to be taken to the maximum required load or to failure. The maximum compressive rate is 0.5 inches per minute.

The minimum acceptable compressive resistance (load) will be based on the HIGHEST value calculated by using the following methods:

A. Four (4) times the greatest expected compressive load during transportation or storage.

B. Ten (10) times the weight of the product intended to be packaged.

C. 300 lbs. compression resistance.

- REFERENCE DOCUMENTS

National Safe Transit Association (N.S.T.A.) Test procedures Project 1A.1973

- A.S.T.M. DOCUMENTS

D-642-76	Compression Test for Shipping Containers
D-775-61(73)	Drop Test for Shipping Containers
D-880-79	Incline Impact Test For Shipping Containers
D-996-78	Packaging and Distribution Environments def. of terms
D-999-76	Vibration Testing of Shipping Containers
D-1083-53(79)	Testing Large Shipping Containers and Crates
D-3331-77	Assessment of Mechanical-Shock Fragility Using Package Cushioning Materials
D-3332-77 Machines	Mechanical-Shock Fragility of Products, Using Shock
D-35680-80	Vibration (Vertical Sinusoidal Motion) Test of Products

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Appendix D Air Cleanliness (Class 100)

Classification of air cleanliness is based on particle count with maximum allowable number of specified minimum sized particles per unit volume and on statistical average particles size distribution.

DEFINITION OF CLASS 100[1]

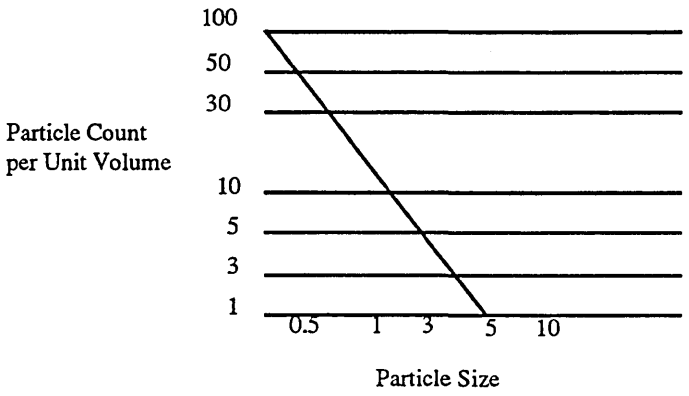
The particle count shall not exceed a total of 100 particles per cubic foot (3.5 particles per liter) of size 0.5 µm or larger.

The statistical average particle size distribution may deviate from this curve because of local or temporary conditions. Counts below 10 particles per cubic foot (0.35 particles per liter) are unreliable except when a larger number of samplings are taken.

TEST METHOD[2]

For particles in the 0.5 to 5.0 µm size range, equipment employing light scattering principles shall be used. The air in the controlled environment is sampled at a known flow rate. Particles contained in the sampled air are passed through an illuminated sensing zone in the optical chamber of the instrument. Light scattered by individual particles is received by a photodetector which converts the light pulses into electrical current pulses. An electronic system relates the pulse height to particle size and counts the pulses such that the number of particles in relation to particle size is registered or displayed.

The count of particles of a given size shall not exceed value shown in the graph below.



1. U.S.A. Federal Standard 209B, available from the General Services Administration; Specifications Activity; Printed Materials Supply Division; Building 197; Naval Weapons Plant; Washington D.C. 20407, U.S.A.

2. American Society for Testing and Materials; Standard ASTM F 50; 1916 Race Street; Philadelphia, Pennsylvania 19103, U.S.A. Society for Testing and Materials; Standard ASTM F

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Appendix E Humidity Charts

These charts are given as reference for any who care to gain a greater understanding of the humidity specifications given in the Environment section. Except for references to specific figure numbers, the explanation is quoted directly from Marks' Standard Handbook for Mechanical Engineers, McGraw-Hill Book Co., Eighth Edition, New York, © 1978.

Psychrometric charts are usually plotted, as indicated by the example Figure E-1, with dry-bulb temperature as abscissa and specific humidity as ordinate. Since the specific humidity is determined by the vapor pressure and the barometric pressure (which is constant for a given chart), and is nearly proportional to the vapor pressure, a second ordinate scale, departing slightly from uniform graduations, will give the vapor pressure. The saturation curve (relative humidity = 100%) gives the specific humidity and vapor pressure for a mixture of air and saturated vapor. Similar curves below it give results for various values of relative humidity. Inclined lines of one set carry fixed values of the wet-bulb temperature, and those of another set carry fixed values of v_a, cubic feet per pound of air. Many charts carry additional scales of enthalpy or Σ function.

Any two values will locate the point representing the state of the atmosphere, and the desired values can be read directly. Figures E-2 and E-3 are psychrometric charts from the General Electric Company and Ellenwood and Mackey, "Thermodynamic Charts," covering a dry-bulb temperature range from 32 to 300°F. They are accurate only for a barometric pressure of 29.92 in Hg.

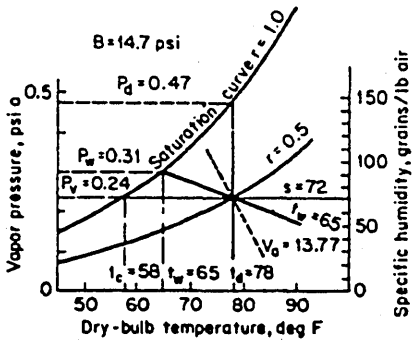


Figure E-1. Skeleton humidity chart.

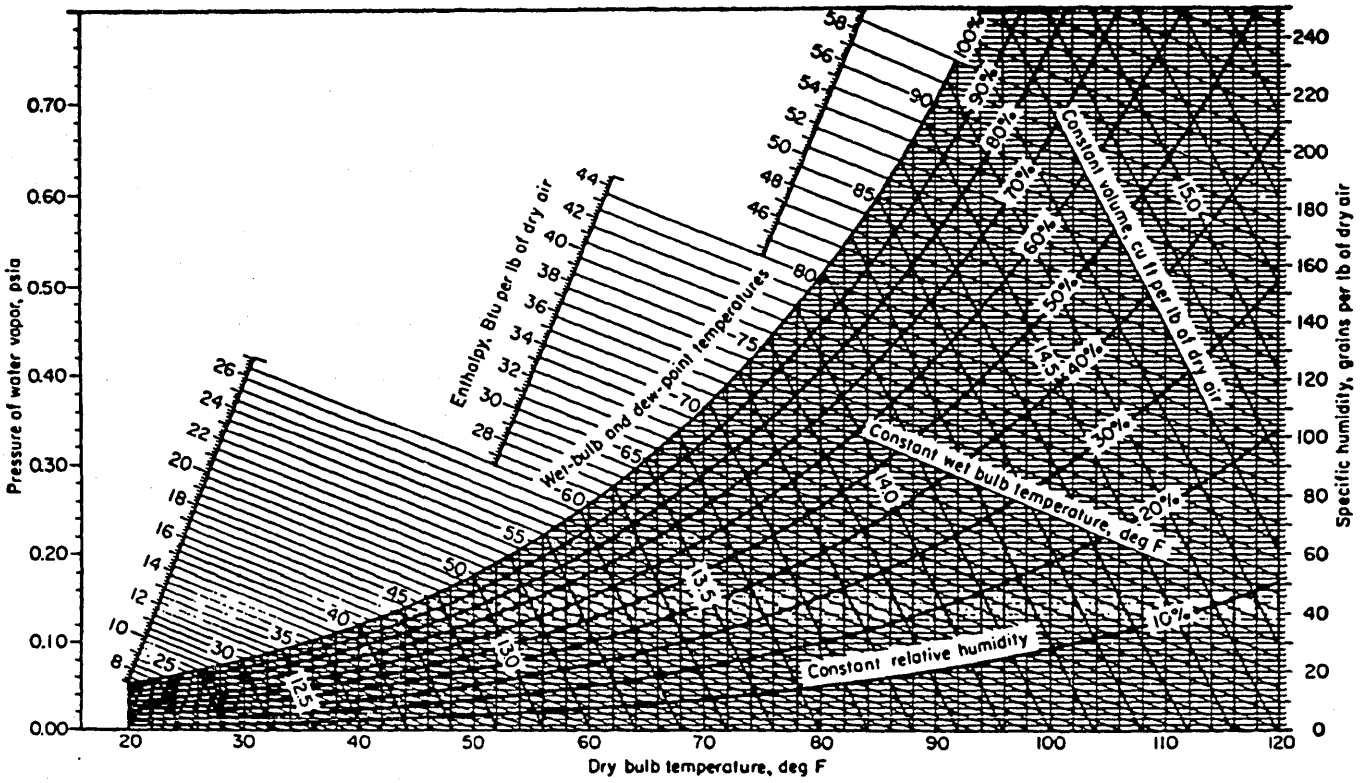


Figure E-2. Humidity chart for low temperatures. Barometric pressure 14.969 psia.
(Copyright by General Electric Co.)

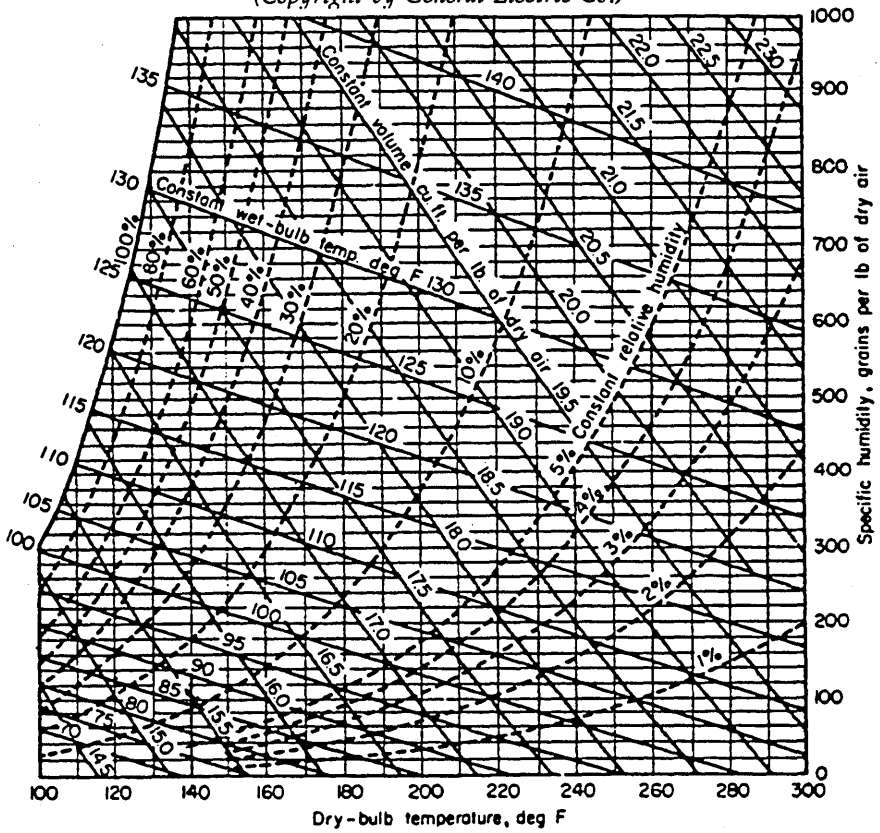
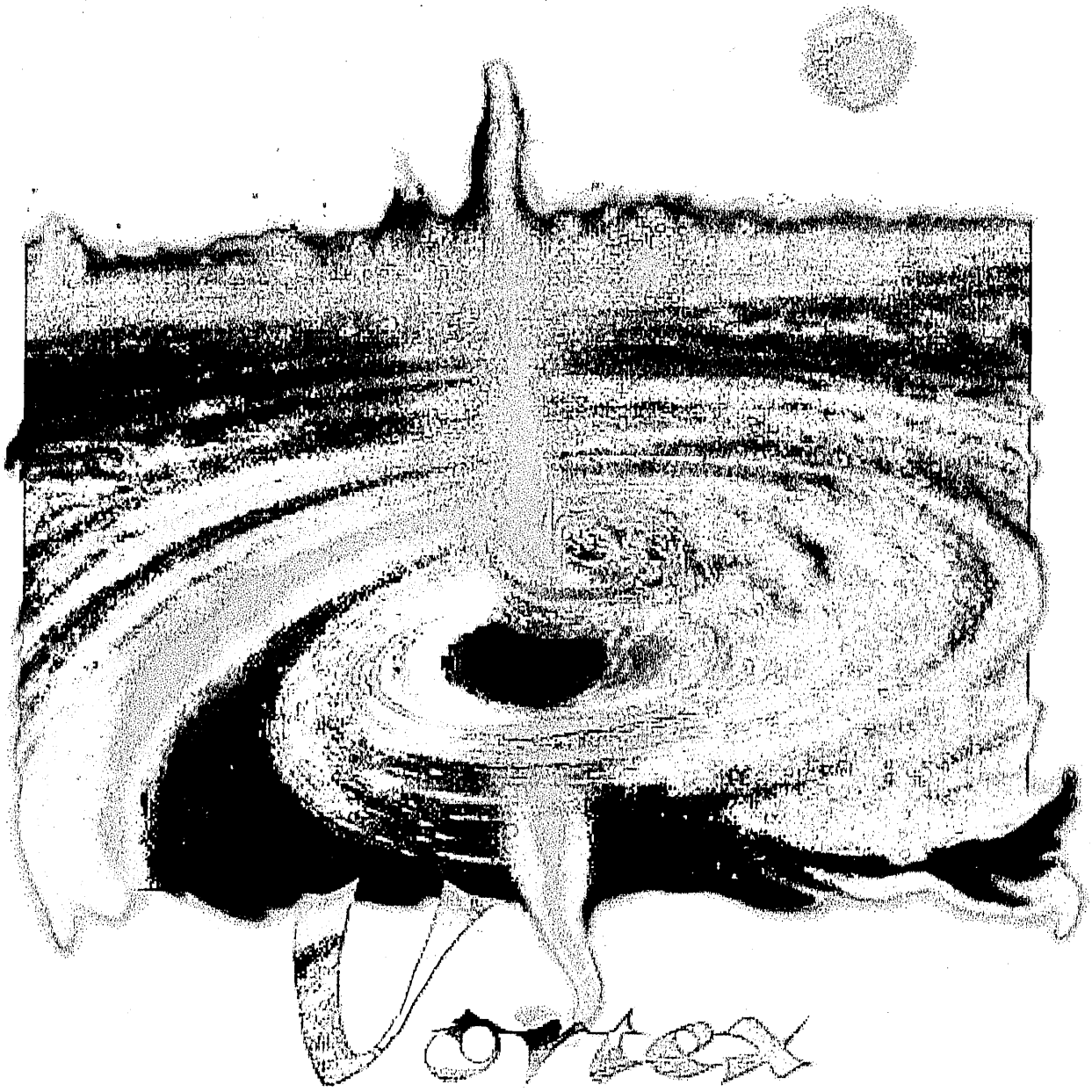


Figure E-3. Humidity chart for medium temperatures.
(From Ellenwood and Mackey, "Vapor Charts," Wiley.)



FIRMWARE MANUAL

NOVEMBER, 1995

REV. A

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Chapter 1 General Information

1.1 Revision History

REVISION	CONTACT	DATE	DESCRIPTION
A	Nick Warner	11/31/95	Initial Release

1.2 Scope

The purpose of this manual is to document the Vortex firmware commands. This manual documents the AT specifications. In addition to documenting the external interface, certain internal features of the firmware and its architecture are described.

1.3 Vortex Firmware Features

The Vortex firmware was derived from the Trailblazer code base. Features were added to support the Shiva read channel and much of SelfScan was changed to implement a Test Process that is similar to Fireball. Additionally a new Defect Management scheme (LBA Based Defect Management) was implemented. The major areas of change are detailed below.

- Support for more than 256 sectors per track
- LBA based Defect Mangement
- Servo Defect Mapping
- Improved Defect Scaning Algorithms
- Read Channel Optimization
  - Read channel optimization algorithms developed by the Vortex Read/Write Group were implemented in SelfScan. These algorithms use iterative methods to provide better optimized parametrics in less time than the previous method used in Fireball.
- S.M.A.R.T. Phase 4
  - Vortex supports version 4 of the S.M.A.R.T. feature. The main change in phase 4 is the addition of the off-line test.

1.4 Applicable Documents

CAM ATA Specification
RAION Specification.
Vortex Selfscan User's Guide (QNTM P/N)
Vortex AT Product Manual (QNTM P/N)
Quantum DPSG Unified Superset Command Manual
Quantum DPA Implementation Guide
Compaq ATA Drive Failure Prediction Spec. Version 1.30 Proposal
Quantum SMART phase 4 specification

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Chapter 2 Vortex Track Format

2.1 Introduction

Vortex is the first Quantum drive to have more than 256 sectors per physical track. The original firmware architecture was optimized, due to code efficiency considerations, for less than 256 sectors per track. In order to support more than 256 sectors per track a number of data structures and internal calculations were changed to support word size rather than byte size data. Additionally the I/O structures for the Superset commands were changed.

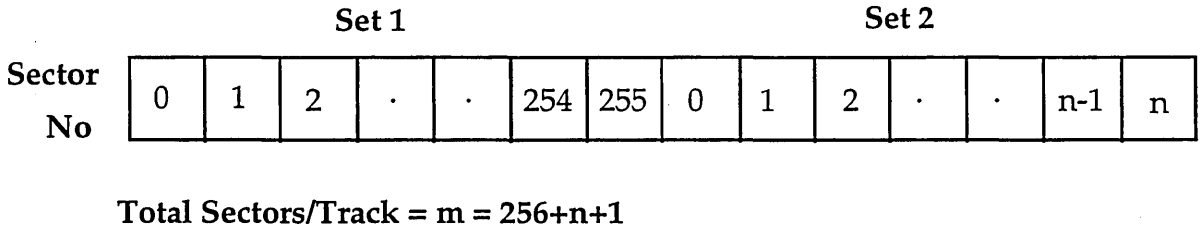
The RAION ASIC does not provide direct support for more than 256 sectors per track, however, using a special 'Double Sectors per Track' format with the corresponding sequencer wcs program it is possible to support up to 512 sectors per track. Additionally the track format was modified for four count bytes per wedge to improve format efficiency.

2.2 Double Sectors Per Track Format

This is a method for handling disk formats of greater than 256 sectors per track using RAION . The principal idea is to divide the track into two parts so that if there are m sectors on the track the formatted track will contain two sets of sectors, with one set numbered from 0 to 255 and the other numbered 0 to m-256-1. Additionally one bit of the cylinder/head ID byte will be used to distinguish between the two sets of sector numbers.

2.3 ID Format

The two sets of sectors are written sequentially on the track as shown. A restriction of this format is that the first sector of each set must start immediately after a wedge and that the number of sectors in the second set is less than the number of sectors in the first set.



Total Sectors/Track = m = 256+n+1

Figure 2-1 Double Sectors Format

The format of the ID bytes after the wedge is shown below. The format for Vortex uses up to four sector splits between wedges, RAION is capable of supporting this although previous products used a maximum of three sector splits. Currently we do not plan to use the Burst Correction Value (PES) feature of RAION . The new/changed ID fields (compared to previous products) are shown in underline.

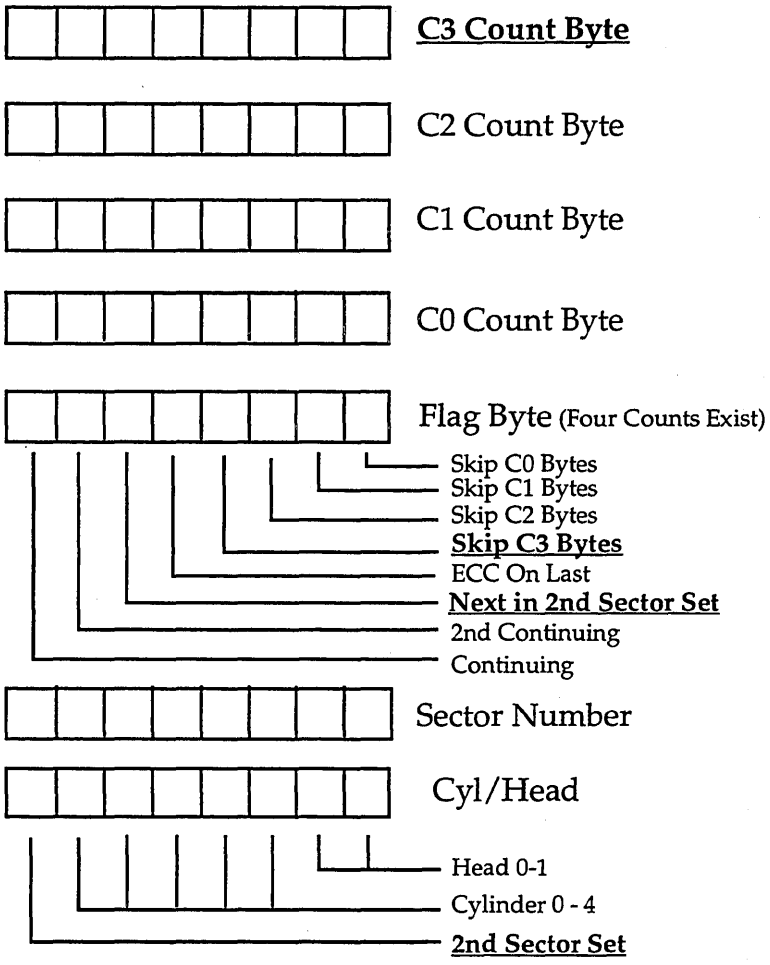


Figure 2-2 ID bytes Format Format

2.4 Sequencer WCS Program

The sequencer wcs program can be modified to handle the above format with the addition of about four instructions. The Sequencer Flag is used to determine if the target sector is in the first or second set of sectors. Before starting the sequencer the Sequencer Flag is set according to the position of the target sector. The wcs program contains instructions for comparing the ID field with either the cyl/hd byte for the first set or the cyl/hd byte for the second set of sectors, it selects which instruction to use based on the Sequencer Flag state. When all the sectors in the wedge have been read/written the sequencer sets the Sequencer Flag for the next wedge to the state of the 'Next in 2nd Sector Set' (formerly Skip Next Header) bit in the Serial Flag Byte. This will allow the sequencer to read continuously all of the sectors on the track. (The Skip Next Header bit was intended to be used for formatting with a moved ID field and is not used during read/write. In the Fireball and Trailblazer code moved ID is not implemented so the bit is available for use.)

2.5 Sequencer Routines

Routines interfacing with the sequencer must take account of the sector numbering used in the ID fields and set up and interpret the sequencer registers accordingly. The rollover register must be set to the last sector in the first set of sectors, note that this may be less than 255 if there are inline defects.

The loop counter will not be large enough to accommodate a full track at the OD so it will sometimes be necessary to startup the sequencer with a partial loop count and add to the loop count as the sequencer is executing. This shouldn't be a problem for normal read/write because the buffer size will limit the transfer, however, it will affect SelfScan when whole tracks are read/written.

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Chapter 3 Defect Management

3.1 Introduction

At the start of the Vortex program the defect characteristics of the media were not well understood and there was consideration given to using uncertified media to reduce media costs. Additionally with the large number of sectors per track it is likely that some tracks will contain multiple defects.

The principal advantage of the LBA Based Defect Management scheme, compared to other methods, is that it allows multiple inline defects on a track with no reduction in drive performance. In Vortex this feature is also taken advantage of to support sparing of sectors around a defective servo wedge and to allow bad track sparing for tracks that contain too many servo defects.

3.2 The Defect List

Two different lists are stored on system cylinder -2 and -3:

1. Primary defect list (P list) - this list contains the defects found in defect scans at the factory. Only the factory test software has the capability to define the P list. The P list contains the description for defects only. No information regarding their replacement is included.

2. Working list (W list) - typically, the W list is a union of the P and G lists, plus it contains all information necessary to locate the replacement to all defects.
   Grown defect list (G list) - this list contains the defects found in the field during operation of the drive. All user's reassigned defects (i.e. with Reassign Block) and auto-reallocated defects are recorded in this list.

The host may access the W list only with the Read Defect AT Extended command. The G list is decoded from information stored in the W list.

The W list is used by defect management whenever a logical-to-physical address conversion is called for.

3.2.1 Replacement Strategy

Vortex reserves one spare sector per cylinder for offline spares. It utilizes two methods for sector replacement - inline and offline sparing.

3.2.1.1 Inline Sparing

Inline sparing is where a defective sector is replaced by the next immediate sector; all sectors thereafter are shifted, logically, by one. A number of spare tracks are reserved at the ID of the drive to accommodate these shifted logical blocks. (see figure 2.1) The access penalty is very small for inline replacement which is one sector time. Whenever possible, defects are spared with inline replacement at the factory. All grown defects are offline spared during drive operation.

3.2.1.2 Offline Sparing

Off line sparing is where a defective sector is replaced by a spare sector located at the end of a cylinder. Defect management will try to replace the defective sector with a spare on the same cylinder. If this is not possible, as in the case of the spare is already in use, defect management will find a spare sector located on an adjacent cylinder. The disadvantage to this is the performance hit caused by the seek. Figure 2.1 contains an example of an offline spare.

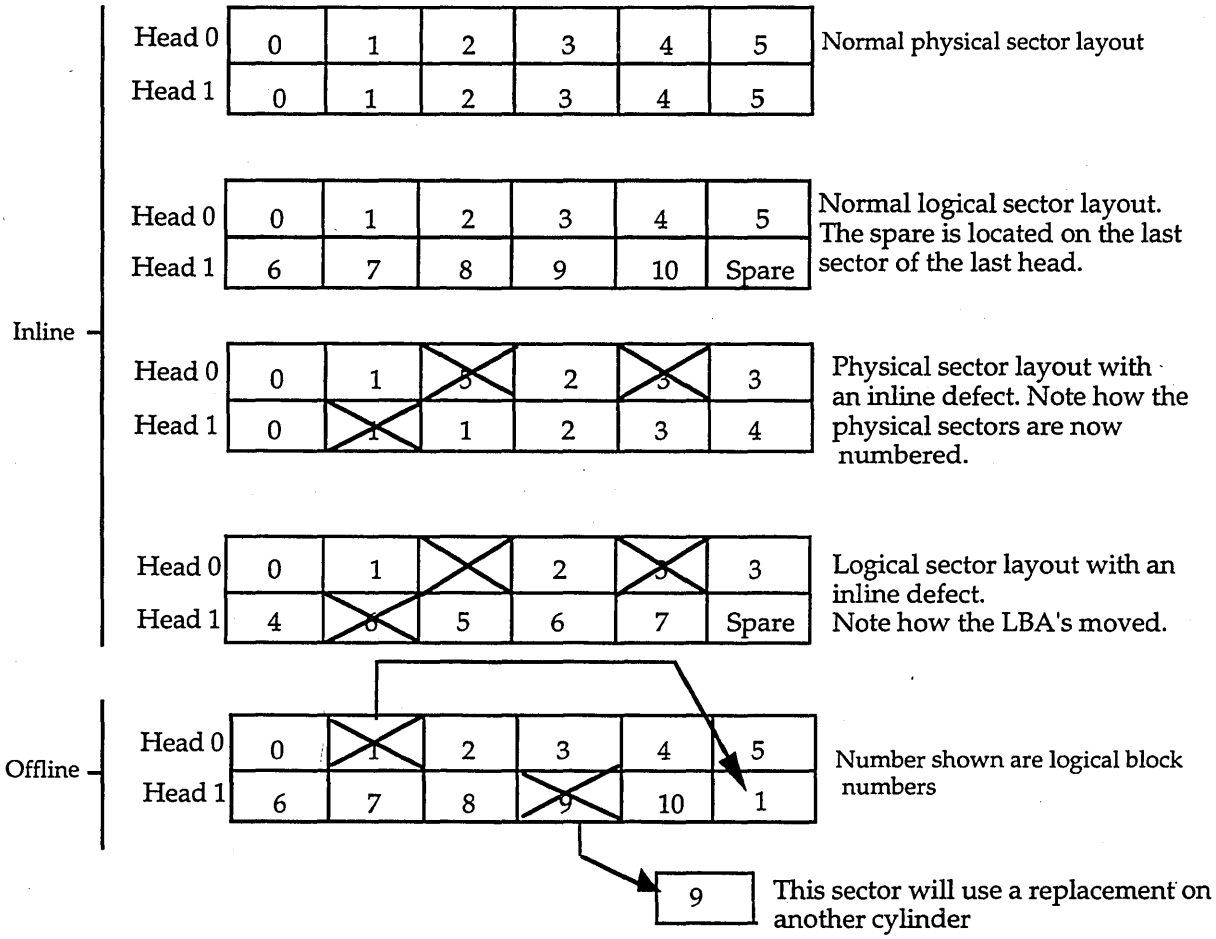

Figure 3-1 Inline and Offline Examples

3.2.1.3 Orphans

An orphan occurs when a replacement sector goes bad. The replacement is assigned a new sector and the original replacement sector is tagged as an orphan in the defect list. It is no longer used. Defect management skips over defect entries that are tagged orphans.

3.2.2 Defect List Data Structure

The defect lists maintained and accessed by the defect management system consist of 8 byte defect entries. The P list contains only defect entries while the W list contains both defect and replacement cylinder information. The defect list structure is illustrated below.

P- List Defect Data Structure

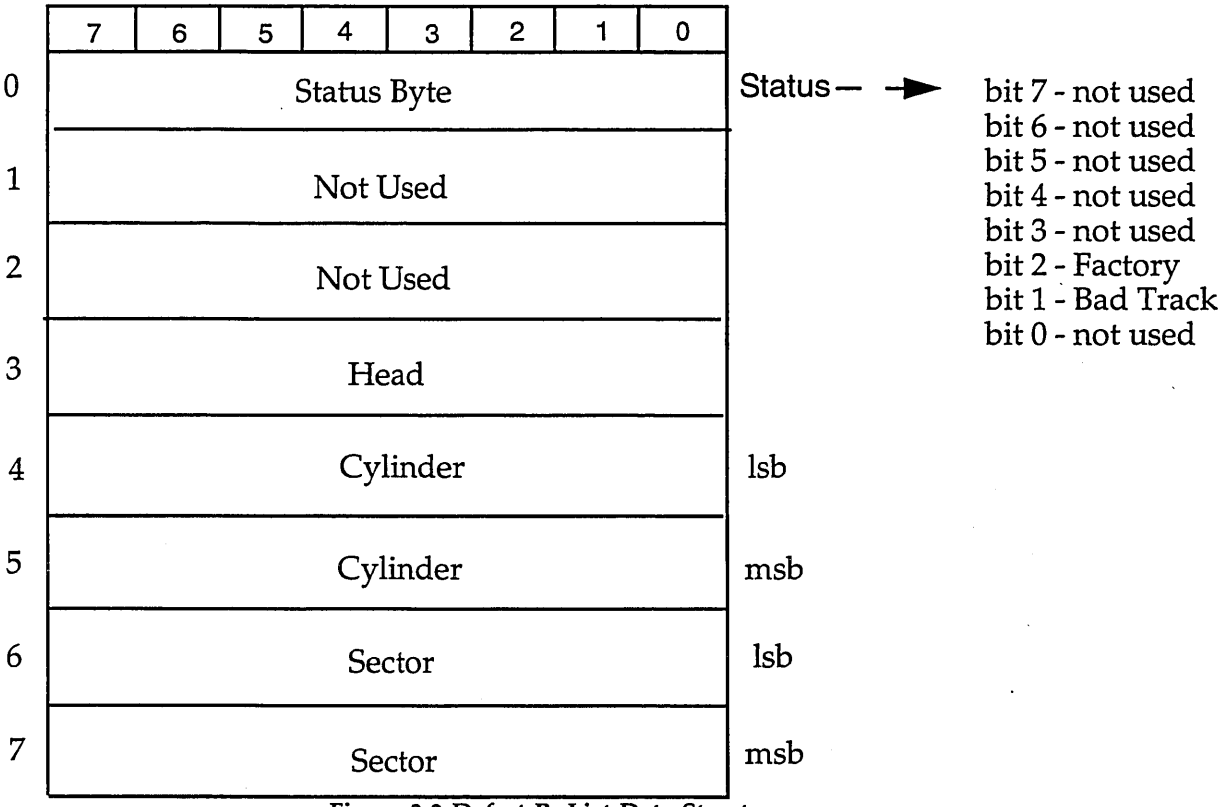

Figure 3-2 Defect P- List Data Structure

- P -List is sorted by CHS.

W-List Defect Data Structure

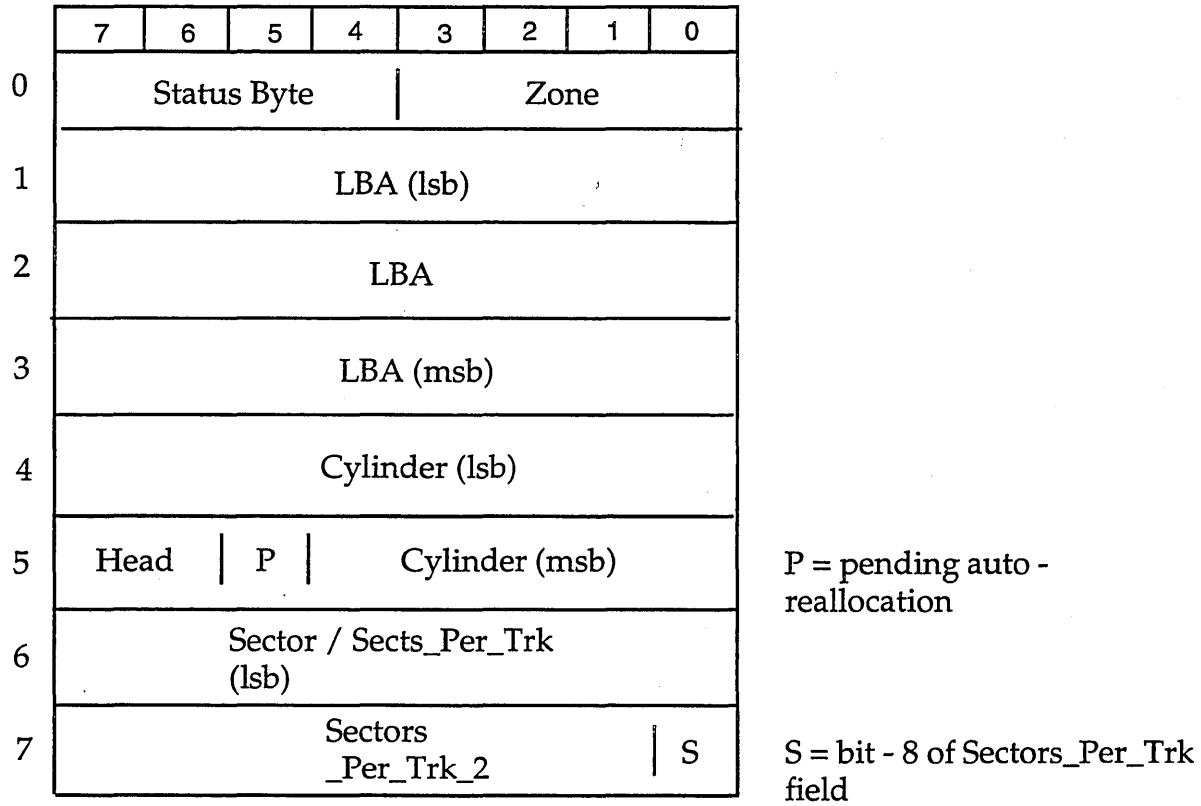

Figure 3-3 Defect W- List Data Structure

- W-List is sorted by lba.

Byte 0 (Status/Zone)

This byte contains combined zone/status information. This will be 0FFH in the end marker.

Bits 0-3 = zone number. The meaning depends on the type of entry:

Zone/Inline entries.....	this is the zone of the zone/inline track.
Offline entries.....	this is the zone of the replacement sector.
New pending entries.....	this is the zone of the pending defective sector.
Orphan entries.....	this is the zone of the orphan sector.

Bits 4-5 = entry type.....	bit-5	bit-4	
	0	0	Zone entry.
	0	1	Offline entry.
	1	0	Inline Entry.
	1	1	Invalid (end marker).
Bits 6-7 = source.....	bit-7	bit-6	
	0	0	Factory.
	0	1	Auto-reallocated.
	1	0	User-reassigned.
	1	1	New pending auto-reallocation.

Bytes 1-3 (lba)

This is the 3-byte lba (lsb first). The meaning of the lba depends on the type of entry:

Zone/Inline entries.....	this is the lba of the first sector on the zone/inline track.
Offline entries.....	this is the lba of the defective sector.
New pending entries.....	this is the lba of the pending defective sector.
Orphan entries.....	this value is set to 0FFFFFEH.

Bytes 4-5 (cylinder/head)

This word contains the cylinder/head information and pending status of the entry:

The cylinder consists of byte-4 (lsb) and bits 0-4 of byte-5 (msb).

The head consists of bits 6-7 of byte-5.

Bit-5 of byte-5 is the pending auto-reallocation bit. Pending auto-reallocation is explained below.

Zone/Inline entries.....	the cylinder/head defines the physical zone/inline track.
Offline entries.....	the cylinder/head defines the physical track of the replacement sector.
New pending entries.....	the cylinder/head defines the physical track of the pending defect.
Orphan entries.....	the cylinder/head defines the physical track of the orphan sector.

Bytes 6-7 (sector/spt)

This word contains the sector number or sector-per-track information of the entry:

Zone entries.....	this word is the sectors-per-track in the zone.
Offline entries.....	this word is the physical sector number of the replacement sector.
New pending entries.....	this word is the physical sector number of the pending defect.
Orphan entries.....	this word is the physical sector number of the orphan sector.

For inline entries:

Byte-6 (lsb) together with bit-0 of byte-7 (msb) form a 9-bit sectors-per-track value. This is the number of sectors on the track (after inlining) not including any offline spare replacement sectors. The offline spare replacement sectors are always the last physical sector of the last track of each cylinder (i.e. max head).

Bits 1-7 of byte-7 form a 7-bit value that gives the number of sectors on the track (after inlining) that are in the '2nd set' of sectors. These are the sectors that have physical sector numbers greater than 255 before inlining. This value is needed by the defect management logic to determine the 'rollover sector number' from the 1st to 2nd set of sectors on a track.

3.2.2.2 Transparent Auto- Reallocation (Pending Defect Entries)

In this new method of handling auto-reallocation of uncorrectable read errors, such sectors are not auto-reallocated until there is a write operation to the sector. To implement this, when an uncorrectable read error occurs (and auto-reallocation of uncorrectable reads are enabled), a pending entry is entered into the W-List (i.e. an offline entry in the W-List with the pending bit set). If the pending defect was already in the W-List as an existing offline replacement sector, then just the pending bit is set in the existing entry. However if the pending defect is not already in the W-List, then a new offline entry is created with the pending pit set and with bits 6-7 of the status/zone byte both set to '1' to indicate this is a 'new pending' entry. When the pending defective sector is subsequently written to, the sector is auto-reallocated. If the pending entry was a 'new pending' type, this entry is changed to a normal offline entry mapping to the closest available replacement sector. If the pending entry was on an existing offline replacement, then an orphan entry is generated for the original offline replacement sector, and a new offline entry is generated mapping to the closest available replacement sector.

3.2.2.3 Inline Spare Tracks

In the Vortex defect management scheme, all inline defects cause the lba values of the following sectors to be adjusted accordingly. In this way inlined defects are 'slipped' to the 'end' of the drive. That is, at the ID of the drive there are a dedicated set of cylinders used for accommodating the inlined defects. Currently, both the 1-disk and 2-disk models of Vortex have 20 such dedicated "inline spare tracks".

3.2.2.4 Mapped -Out Tracks

A new feature in vortex is the ability to map out entire tracks. When SelfScan identifies such a track (currently due to more than 2 bad wedges on a track), it places a special entry in the drive's servo defect list. These tracks are then mapped-out by placing an inline entry in the W-List which indicates zero sectors-per-track.

3.2.2.5 Orphan Entries

Orphan defect entries can occur in one of the following ways:

1) An unused offline-spare sector is user-reassigned.
2) A used offline-spare replacement sector is either user-reassigned or auto-reallocated.
3) A sector on one of the inline spare tracks at the ID of the drive is user-reassigned.

3.3 Defect List Storage

Up-to-date versions of the P and W lists are saved on the disk, only the W list needs to be resident in RAM during drive operation. Each defect list may require up to 8192 bytes of storage, therefore, a total of 16 sectors list are reserved to hold the defect lists on a system track. See section 3 for System Cylinder layout for the location of the lists.

3.4 LBA to CHS Conversion

There are two entry points for performing the LBA to CHS conversion. Given an LBA, the caller invokes INIT_LBA_TO_CHS to initiate the conversion process.

INIT_LBA_TO_CHS determines the destination physical CHS. The function returns the CHS of the first valid sector plus a value indicating the number of consecutive data sectors starting from the first accessible sector.

It is left to the caller to decide how many sectors are actually required to complete its operation. If sectors are needed in addition to the first series of consecutive sectors, the caller uses the NEXT_LBA_TO_CHS function to locate the next series of sectors. NEXT_LBA_TO_CHS requires no input parameter and returns the same information as INIT_LBA_TO_CHS.

3.5 Auto Reallocation

Vortex has implemented a new method for auto-reallocation of uncorrectable read errors. The method is called 'transparent auto-reallocation' and is based on the implementation first included in the Fireball product.

The functionality of auto-reallocation for write errors and correctable read errors has not been changed. For these errors, the auto-reallocation of the defective sector (assuming the auto-reallocation is enabled in the drive's configuration settings) is done during the write or read operation that generated the error.

Previously, the same was true for auto-reallocation of uncorrectable read errors as well. With transparent auto-reallocation, the defective sector is not auto-reallocated at the time of the read operation that generated the error. Subsequent read operations from the same LBA will continue to result in DATA_ECC error status without auto-reallocation of the sector. If at any time after the read that initially generated the error, there is a write operation to this defective LBA, the auto-reallocation of the sector will then be performed during this write operation.

Note that with the previous method, once the uncorrectable read error caused the auto-reallocation, the original good data could never be recovered. With the new method, subsequent re-reads of the defective sector could possibly allow the original data to be recovered. The original data is not guaranteed to be lost until the host decides to write some other data to the sector.

Reallocation during read or write operation is processed on sector by sector basis. Reallocation operation is done differently between a read and write command. The differences are identified below:

3.5.1 Read Operation

Uncorrectable Error (Assuming reallocation is enabled for such error) :
If an uncorrectable error occurred, the sector in error is still considered as a potential defective sector and auto reallocation will not be perform immediately. A defect entry will be added to the W- list with a special bit set to indicate the defect is a pending defect.
If subsequent write is performed on the sector, the sector will be reallocated at that time (subject to the 10 - write /verify operation).

Correctable Error (Assuming reallocation is enabled for such error):
Correctable error are reallocated at the time of the read error (subject to the 10 - wtite/verify operation).

3.5.2 Write Operation

For write command, the correct data that was received from the host is already available in the buffer so it safe to perform the ten write/verify test on the defective sector. If any of the ten tests fail, the defect is considered repeatable and the sector is reallocated. If all ten tests pass, then the failure is considered non-repeatable and the sector is left as is and the correct data is written to this sector.

3.5.3 Super Mode

For testing purpose, a user can create ECC error and then force auto reallocation with a write command. Each time an ECC error is created, the sector is added to the W-list as pending defect. A write command causes auto reallocation to occur and the pending defect entry is removed from W-list after auto reallocation is finished.

Chapter 4 Servo Defect Mapping

4.1 Introduction

The Servo Defect mapping scheme used in Fireball was ported to Vortex. This feature allows two defective wedges per track to be mapped out. The defective servo wedges are determined during SelfScan Servo Verify and a Servo Defect List is constructed and saved to disk. During the set up for a seek operation the Servo Defect List is searched for the destination track and if an entry is found it is copied to the Wedge Defect List. During the servo interrupt in track following mode the current wedge number is compared to the Wedge Defect List entries, if the entry matches the position information for the current wedge is ignored and the servo free-wheels through the wedge. In Vortex the servo defect list scheme has been extended to allow consecutive bad wedges (in this case the six following wedges are mapped out in the Data Defect List), also a special entry in the servo defect list is used to indicate a bad track that has been spared.

Servo Defect List Data Structure

	7	6	5	4	3	2	1	0
0	Cylinder CSB						Head	
1	Cylinder MSB							
2	Wedge 1							
3	Wedge 2							

- Up to 63 entries in Servo Defect List
- Unused Wedge Entry = OFFh
- Defective Track Entry = OFEh

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Chapter 5 System Cylinders

5.1 General Information

Five cylinders on all drives are reserved for system and test usage. These cylinders contain drive configuration information, drive test information, and diskware. Customers cannot access these reserved cylinders. The reserved cylinders are only accessible with physical address commands which are protected diagnostic commands.

Data is stored on heads 0 and 1 in the OD system area.

The reserved cylinders are assigned as follows:

Cylinder	Description Outer System Area
-1	Test data/Error logging
-2	System
-3	Copy of cylinder -2
-4	Diskware
-5	Copy of cylinder -4

Note : The data on the system cylinder, unless specified otherwise, will use the following rules:

ASCII fields must be left justified, terminated with binary 0, and padded with binary 0's. ASCII fields read by the drive firmware, such as the serial number, must be right justified with spaces and terminated with 0.

5.2 Test Equipment / Error logging Cylinders

The test equipment cylinder is reserved for test process usage. This cylinder contains test parameters and data collected during production test.

The sector usages of cylinder -1 are as follows:

Sector	Description
0	Copy of Servo writer Serial Number Data.
1	Test Process Interlock
2	Reserved .. for Reclassification .. NA on AD1
3	Configuration Center Control.
4	Reserved .. for Expansion.
5 - 14	Test Process History Queue.
15 - 30	Process Test Defect List.
31	Not Used
32 - 39	Self Scan results (8).
40	Not Used
41 - 48	Self Scan test parameters (8).
49 - 51	Not Used
52 - 75	Self Scan defect list (24).
76 - 78	Servo defect map (1).
79	Soft error table (1).
80 - 81	Not Used
82 - 85	Runout Results (4)
86 - 99	Not Used
100 - 105	Not Used
106 - 108	S.M.A.R.T Attributes/Variables/Thresholds
109 - 131	Not Used
132	Selfscan Variables Save/Restore (1)
133 - 137	Not Used
138 - 139	Performance Test Results (2)
140 - 159	Adaptive Results (2).
160 - 175	Not Used
176 - 191	Reserved for in-line defect sparing.

5.3 System / Firmware Cylinders

This cylinder is reserved for system and firmware usage. It contains modepage information, configuration information, defect list, and format information for the drive.

Sector usages of cylinder -2 and -3 are as follows :

Sector	Description
0	Saved mode pages
1 - 8	Configuration pages
9 - 24	Working defect list
25 - 40	Primary defect list
41 - 56	T - List
57 - 72	Format header bytes - zone 0-15
73 - 74	Not Used
75	Servo Defect list
76 - 77	Recal Record
78 - 92	Not Used
93 - 105	Not Used
106 - 175	Not Used
176 - 191	Reserved for in-line defect sparing

Sector Usages of cylinder -4 and -5 are as follows:

Sector	Description
0 - 2	Vector Table
3 - 31	Resident
32 - 47	Overlay 2
48 - 55	Overlay 9
56 - 63	Unused
64 - 68	Overlay 3
69 - 79	Overlay 4
80 - 90	Overlay 5
91 - 101	Overlay 6
102 - 112	Overlay 7
113 - 123	Overlay 8
124 - 175	Not Used
176 - 191	Reserved for in-line defect sparing

- **Configuration Pages**
  This area contains the drives configuration information such as the revision level, number of heads, etc. See the Read Configuration superset command for a detailed explanation of the data contained in this sector.

- **Defect List Sectors**
  These sectors contain the defect lists used during the drives normal operation. See the chapter on Defect Management for more information.

- **Format Header Sectors**
  In order for the firmware to format the drive, it needs to know the count byte information for the split sector data fields. Since there is no simple algorithm to generate this

information, the count bytes must be stored in a table. We allocated 16 sectors on the system cylinder to hold this information. Each sector contains the count byte information for a particular zone.

Chapter 6 Defect Scaning

6.1 Wedge to Wedge Scan

The Shiva read channel optimizations make use of the wedge to wedge sequencer programs.

It is generally accepted that wedge to wedge scanning provides better coverage for sync field and ECC field areas than can be achieved through sector scanning. Also it is possible to stress the channel more during wedge to wedge scan to enhance the defect detection because a fixed data pattern without ECC bytes is used.

For these reasons, and to make the Test Process equivalent to Fireball a Wedge to Wedge Scan was implemented as part of SelfScan.

6.2 Scan Immediate/Scan Multiple

To make the defect scanning more efficient it is desirable to reduce the amount of time spent in latency and seeking compared to that read and writing.

In Vortex a technique called Scan Immediate was implemented for both wedge to wedge and sector scans. This technique samples the current rotational position when starting a read or write operation and if the target sector/wedge is not within a predetermined window adjusts the target so that the reading or writing can start sooner. This allows much of the latency time during scanning to be eliminated.

The Scan Multiple feature scans each track using multiple data patterns before seeking to the next track, this reduces the total seek time required. This method was already implemented in the Trailblazer code base, however, it was enhanced to allow more data patterns and to allow the data patterns to be optionally scanned with offset.

6.3 Customer Scan

Customer Scan was modified to provide a soft error rate measurement equivalent to Fireball. In Vortex Customer Scan is only used for soft error rate measurement and as a confidence scan to verify the inline formatting. It is not used for defect mapping because defect mapping can be done more efficiently using wedge to wedge and physical sector scanning.

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Chapter 7 Diskware

7.1 Introduction

The Vortex architecture is designed to support diskware and memory overlay. Part of the Buffer memory is used to load firmware from disk and the processor is able to execute the firmware directly from the buffer. When the Vortex drive is power up, a portion of the Vortex diskware is loaded into Resident Diskware area in RAM from system cylinder. This portion in Resident Diskware is permanent during whole run-time. The overlay Diskware area stores one of five overlays at a time which is loaded dynamically based on which is needed.

7.2 Memory Map

The DRAM memory map for Vortex is organized as follows:

K3 ADDRESS			DRAM ADDRESS
0EE00h - 0EFFFh	CONFIG. PAGE 21 ADAPTIVE SERVO PARAMETERS		1FE00h - 1FFFFh
0E600h - 0EDFFh	CONFIG. PAGE 17 HARDWARE ZONE VALUES	2.5K	1F600h - 1FDFFh
0E400h - 0E5FFh	COMMAND HISTORY	0.5K	1F400h - 1F5FFh
0E000h - 0E3FFh	TEMP BUFFER	1K	1F000h - 1F3FFh
0E000h - 0EFFFh	WORKING DEFECT LIST	8K	1D000h - 1EFFFh
0EE00h - 0EFFFh	SERVO DEFECT LIST	0.5K	1CE00h - 1CFFFh
0E000h - 0EFFFh	CACHE BUFFER	87.5K	07000h - 1CDFFh
0EC00h - 0EFFFh	ERROR LOGGING	1K	06C00h - 06FFFh
	NOT USED	0.25K	06B00h - 06BFFh
0F300h - 0FAFFh	FIRMWARE TABLE VARIABLES & CONFIG. PAGES	2K	06300h - 06AFFh
0F200h - 0F2FFh	ISR BUFFER	0.25K	06200h - 062FFh
0F000h - 0F1FFh	FIXED BUFFER	0.5K	06000h - 061FFh
0C000h - 0DFFFh	OVERLAY DISKWARE	8K	04000h - 05FFFh
08000h - 0BFFFh	RESIDENT DISKWARE	16 K	00000h - 03FFFh
00000h - 07FFFh	ROM CODE	32 K	N/A

The firmware is partitioned between the ROM code and the Diskware. The ROM code contains all of the routines necessary to power up the drive and read the diskware into the Buffer. It also contains routines that allow the Diskware to be written to the disk via the host interface. All time critical code is located in the ROM because the processor is able to execute ROM code much faster than Diskware code. The Diskware code contains non time critical code that is not required for powering up the drive. The Diskware code also contains provisions to allow firmware bugs in the ROM code to be corrected by mapping erroneous subroutines from ROM into the Diskware.

7.3 Diskware Code Organization

The diskware code space is partitioned into two parts, a resident part and an overlay part. The Resident diskware is loaded during the drive power up initialization and remains in memory while the drive is powered on. The Overlay diskware is loaded when needed.

Address Range	Description
8000h - BFFFh	Resident Diskware (Vector Table; Code)
C000h - DFFFh	Overlay Diskware

The Resident Diskware contains a vector table which is used by the ROM code for accessing Diskware subroutines and data, and for mapping erroneous ROM subroutines into Diskware subroutines. During power up initialization a default vector table is copied from ROM, this is replaced by the actual vector table when the Diskware is loaded from disk.

7.4 Diskware Storage Requirements

The diskware is stored on reserved system cylinders in memory image format. Configuration page 15 specifies where the overlays are stored on the system cylinders and where the overlays are loaded into the processor memory. Generally system cylinder information is stored in multiple places for redundancy, although the overlay configuration page only specifies where the first copy of the diskware is stored. Redundant copies of the diskware are stored according to the firmware redundancy algorithm for system cylinder information. The Vortex firmware stores redundant system cylinder information on physical head 0 and 1 in system cylinder areas.

Configuration Page 15 - Overlay Page

Field Offset	Description
0	Element number definition
1 - 3	Load address
4	Size- number of sectors
5 - 6	Cylinder
7 - 8	Alternate Cylinder
9 - 10	Starting Sector
11	Element number definition
12 - 21	Same fields as above
:	:
111	FFh - End marker

7.5 Write Buffer Command

Write Buffer command with the download option for SCSI and ATA is used to update the diskware. The Write Buffer command is described in the respective interface documents (SCSI ANSI X3T9.2/375R, ATA ANSI X3T9.2/791D). The download options are vendor specific, this specification will define the Quantum implementation of this option.

7.5.1 SCSI Write Buffer Command

	7	6	5	4	3	2	1	0
0	Opcode = 03Bh							
1	LUN = 0			Reserved		Mode		
2	Q	Reserved = 0						
3	Reserved = 0							
4	Reserved = 0							
5	Reserved = 0							
6	Parameter list length (MSB)							
7	Parameter list length							
8	Parameter list length (LSB)							
9	Reserved = 0						F	L

Mode 100 - Download Diskware. (Ramware)
Q 0 - Servo recal
1 - No servo recal (Quiet mode)

101 - Download Diskware and save.
Q x - ignored

7.5.2 ATA Write Buffer Command

The command is an optional, class 3 command. The op code used is 92h. Parameters used are the FR, SC, SN, CY registers. (see table 9-1 of the ATA specification). It is also a PIO Data Out command (see section 10.2 of the ATA specification). The head bits of the Drive/Head register shall always be set to zero. The Sector register shall be used to extend the Sector Count register, creating an effective sector count 16 bits long. The Cylinder High and Low registers are reserved.

The value of the Features register shall be used to determine the time the update takes effect, whether it is saved for future use, and any future functions:

Feature register values for Download diskware.

bit 2 1 0	
0 0 1	download is for immediate, temporary use. (Ramware)
1 1 1	save downloaded code for future reference by value of cylinder and specify it as the default for immediate and future use.

Feature register value of 0FEh specifies a download for immediate temporary use with no servo recal.

7.6 Diskware Download Theory of Operation

The write buffer command will download diskware. The download elements are a diskware downloader, an optional diskware boot loader, diskware control page, and diskware overlay entries. The diskware downloader shall be validated by a good checksum, valid product code, compare of the ROM version stamp and ROM checksum. Once the diskware downloader is validated, the diskware downloader will execute.

The diskware downloader will validate the diskware control page and diskware overlay entries by a good checksum, valid product code, compare of the ROM version stamp and ROM checksum. The diskware downloader will put the drive in a "ROM only" state (servo and spindle to run out the ROM) and move the overlay entries to the locations directed to by the diskware control page. The last overlay entry to move is the vector table. Care must be exercised to disable the currently running functions when this table is loaded (i.e. servo and spindle functions that are currently running in "ROM only" mode). Upon completion of the vector table move, the handler will initialize drive mode and configuration page parameters with the ROM defaults. The handler will start execution of the diskware in ram.

The download and save mode will additionally save the diskware data to the reserved cylinders as specified in the diskware control page.

The optional diskware boot loader is firmware that at power up will be read from disk and it will read and validate the remaining diskware elements.

7.7 Diskware Elements

All the diskware elements have a common header at the beginning of each element. The diskware element header is defined as follows:

Byte	Definition of field
0	Element Type
1	Product Code
2-4	ROM Version Stamp
5-6	ROM Checksum
7	Length of the element
8-14	Element dependent
15	Checkbyte
16	Start of element data
n	End of element data

Description of the bytes in the page

Byte 0	Type of element. 80h - Diskware downloader 81h - Diskware control page 82h - Diskware boot loader 00h - Vector Table 01h - Resident 1xh - Resident overlay x 03h - Self Scan resident 3xh - Self Scan overlay x
Byte 1	Product code unique to each product.
Byte 2-4	Copy of the ROM version stamp.
Byte 5-6	Copy of the ROM checksum.
Byte 7	Length of this data page in 512 sectors.
Byte 8-14	Element dependent.
Byte 15	Checkbyte of the element.
Byte 16	Start of the diskware element data.
Byte n	End of the diskware element data.

7.8 Diskware Downloader

The diskware downloader consists of element header and data. The downloader definition is defined as follows:

Byte	Definition of field
0	Element type (080h).
1	Product Code
2-4	ROM Version Stamp
5-6	ROM Checksum
7	Size of the downloader
8-11	Downloader execution address
12-14	Reserved
15	Checkbyte
16	Start of downloader code
n	End of downloader code

Description of the bytes in the diskware downloader.

Byte 0	Element type for the diskware downloader.
Byte 1	Product code unique to each product.
Byte 2-4	Copy of the ROM version stamp.
Byte 5-6	Copy of the ROM checksum.
Byte 7	Length of this data page in 512 sectors.
Byte 8-11	Downloader start of execution address.
Byte 12-14	Reserved.
Byte 15	Checkbyte of the diskware downloader.
Byte 16	Start of the diskware downloader program.
Byte n	End of the diskware downloader program.

7.9 Diskware Control Page

The Diskware control page contains diskware entries. A maximum of twenty entries are available in this page. The diskware control page is 512 bytes long and is defined as follows:

Byte	Definition of field
0	Element Type (81h)
1	Product Code
2-4	ROM Version Stamp
5-6	ROM Checksum
7	Length of the page (01h)
8-14	Reserved
15	Checkbyte
16	Element type 0
17-19	Load Address
20	Size
21-22	Cylinder
23-24	Alternate Cylinder
25-26	Starting Sector
27	Element type 1
28-37	Definitions same as bytes 17-26
38	Element type 2
39-48	Definitions same as bytes 17-26
49	Element type 3
50-59	Definitions same as bytes 17-26
60	Element type 4
61-70	Definitions same as bytes 17-26
71	Element type 5
72-81	Definitions same as bytes 17-26
82	Element type 6
83-92	Definitions same as bytes 17-26
93	Element type 7
94-103	Definitions same as bytes 17-26
104	Element type 8
104-114	Definitions same as bytes 17-26
115	Element type 9
116-125	Definitions same as bytes 17-26
n	End of overlay entries (0FFh)
n+1-511	Fill (00h)

Description of the bytes in the page

Byte 0	Element type overlay control page (081h)
Byte 1	Product code unique to each product.
Byte 2-4	Copy of the ROM version stamp.
Byte 5-6	Copy of the ROM checksum.
Byte 7	Length of this data page in 512 sectors.
Byte 8-14	Reserved.
Byte 15	Checkbyte of diskware control page.
Byte 16	Element number definition.
Byte 17-19	Load address is the memory address of the overlay. The load address is three bytes of a four byte address with the least significant byte zero.
Byte 20	Size in 512 sectors
Byte 21-22	Cylinder is where primary copies of the overlay will be stored.
Byte 23-24	Alternate Cylinder is where alternate copies of the overlay will be stored.
Byte 25-26	Starting sector is where the overlay starts.
Byte 27-n	Additional overlay entries.
Byte n+1	End of overlay entries (0FFh marks the end of the entries).
Byte n+2-511	Fill pads out from the End of overlay marker to byte 511.

7.10 Diskware Overlay Entry Data

All the disk parameters for the diskware data are defined in the diskware control page. Each overlay has a element header. The overlay data is defined as follows:

Byte	Definition of field
0	Element Type
1	Product Code
2-4	ROM Version Stamp
5-6	ROM Checksum
7	Size
8-14	Reserved
15	Checkbyte
16	Start of overlay data
n	End of overlay data

Description of the bytes in the page

Byte 0	Element type.
Byte 1	Product code unique to each product.
Byte 2-4	Copy of the ROM version stamp.
Byte 5-6	Copy of the ROM checksum.
Byte 7	Length of this data page in 512 sectors.
Byte 8-14	Reserved.
Byte 15	Checkbyte of the overlay entry data.
Byte 16	Start of the overlay entry data.
Byte n	End of the overlay entry data.

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Chapter 8 Error Correcting Code

8.1 ASIC ECC Comparison

RAION	Vs	KONI
• 8 bits per symbol		Same
• 3 interleaves		Same
• 6 redundancy bytes per interleave		4 redundancy bytes per interleave.
• 2 cross-check bytes		Same
• 18 ECC bytes and 2 CRC bytes		12 ECC bytes and 2 CRC bytes
• Single-Error Correction:		Same
• Double-Error Correction on the fly		Not on the fly
• Triple-Error Correction		Not available
• 3 Bytes CRC per ID field		Same

8.2 Reed Solomon Generator Polynomial in RAION ASIC

8.2.1 ECC Polynomial

The ECC polynomial is defined as follows:

$$G(X) = X^6 + \text{alpha}^{169} * X^5 + \text{alpha}^{179} * X^4 + \text{alpha}^{25} * X^3 + \text{alpha}^{184} * X^2 + \text{alpha}^{179} * X + \text{alpha}^{15}$$

$$= (X + 1)*(X + \text{alpha}^1)*(X + \text{alpha}^2)*(X + \text{alpha}^3)*(X + \text{alpha}^4)*(X + \text{alpha}^5)$$

8.2.2 Cross Check Polynomial

The Cross - Check Polynomial is defined as follows:

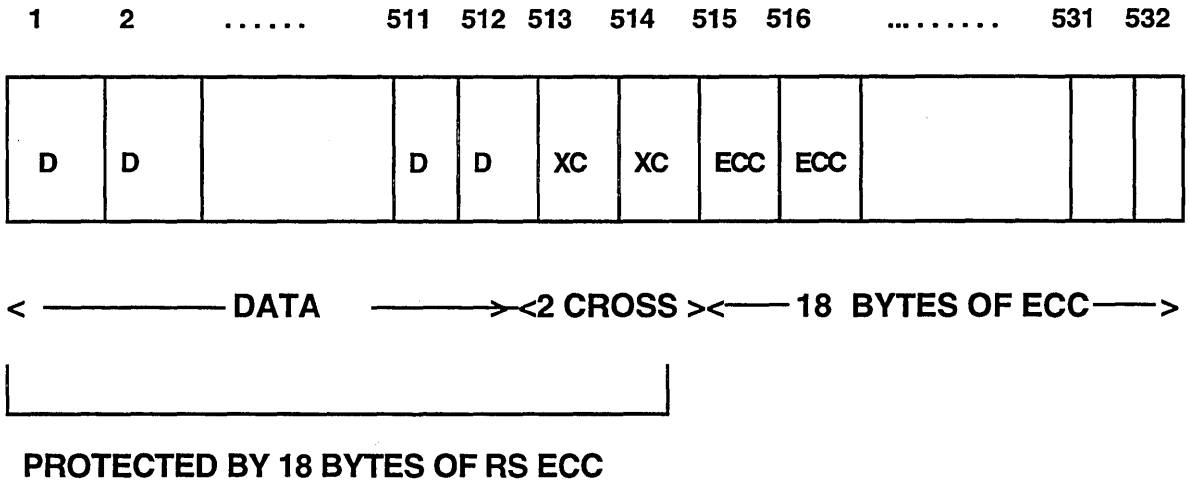
$$XC(X) = X^2 + \text{alpha}^{143} * X + 1$$
$$= (X + \text{alpha}^{127})*(X + \text{alpha}^{128})$$

8.2.3 CRC Polynomial

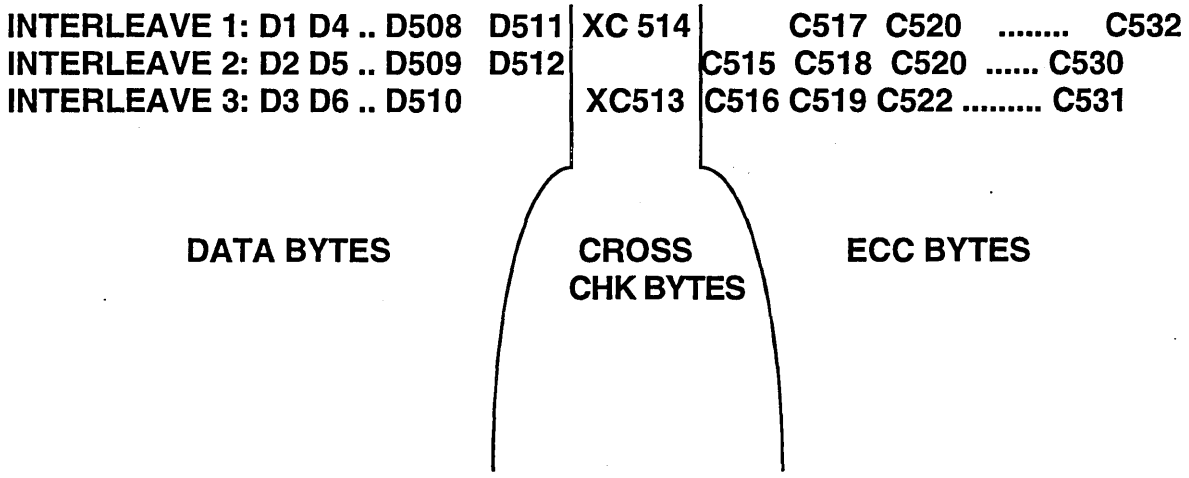
$$CRC(X) = X^3 + \text{alpha}^{203} * X^2 + \text{alpha}^{203} * X + 1$$
$$= (X + \text{alpha}^{-1})*(X + \text{alpha}^0)*(X + \text{alpha}^1)$$

8.3 RAION ASIC

8.3.1 1 Sector Data Field with ECC Bytes



8.3.2 Bytes Interleaving



8.4 ECC Principles of Operation

- ECC hardware includes REED-SOLOMON (RS) Encoder/Decoder circuit that is used to generate redundancies during write mode and syndromes during read mode.
- ECC hardware also checks the values of the syndromes to detect errors.
- All corrections will be done in Firmware.

8.5 Cross Check Bytes

- There are 2 cross check bytes per data filed.
- Used to " Double Check" the main correction, and therefore reduced the miscorrection probability of the REED-SOLOMON (RS) ECC correction.

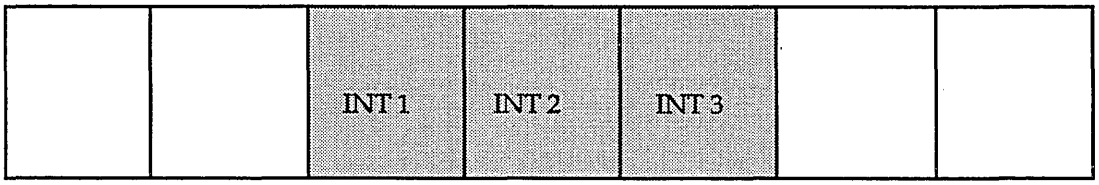
8.6 ECC Correction On - the - Fly

- The expression "On - the - Fly" means an error correction process which is carried out with minimized data flow interruption, and which does not requires one or more disk rotation latencies (revolutions) for carrying out the correction process.
- In order to perform ECC "On - the Fly", it is necessary to detect and correct the data errors in the background while the sequencer is still active, so that is does not stop the flow of data block during a typical transfer of multiple blocks.

8.7 Single Burst Error

- Single burst error is defined as an error occurring in one byte within one of the interleaves.
- Can have up to three erroneous bytes within a sector, provided that each byte of the three occupies a different interleave.
- Correct up to 24 bits I.E., 1 byte per interleave. Guarantee to correct 17 bits.

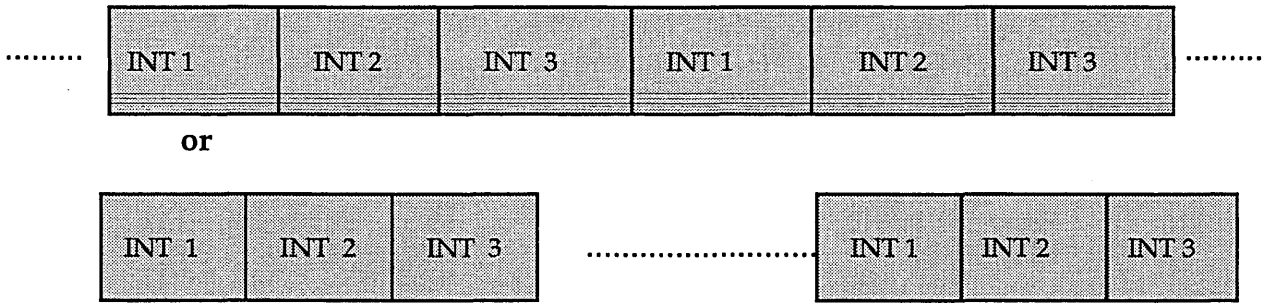
8.7.1 Correctable of 24 Bit Single Burst Error



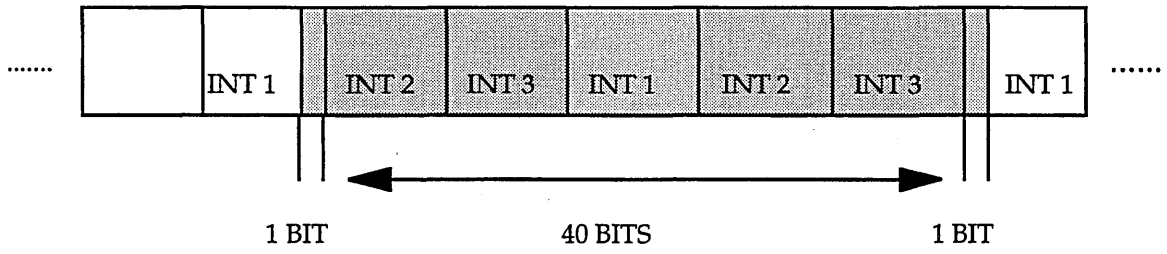
8.8 Double Burst Error

- A double burst error is defined as an error occurring in two bytes within one of the interleaves.
- Correctable double burst errors must have two or fewer erroneous bytes per interleaves.
- Correct up to 48 bits I.E., 2 bytes per interleave. Guarantee to correct 41 bits.

8.8.1 Correctable 48 Bit of Double Burst Error



8.8.2 Uncorrectable (On - the -Fly) 42 Bit of Double Burst Error

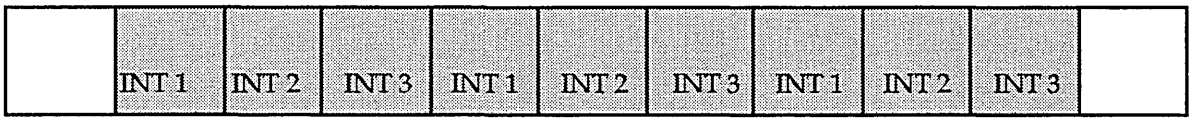


Note :
The 42 bit error is uncorrectable, while the other two 48 bit errors are correctable. The reason for the 42 bit error is uncorrectable is that occupies two interleave 2S, and two interleave 3S, but occupies three interleave 1S, where as the limit is two bytes per interleave. This 42 bit error can be corrected if the drive rereads the sector and applies triple burst error correction techniques.

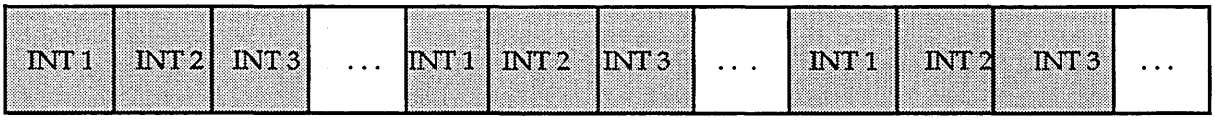
8.9 Triple Burst Error

- Triple burst error is defined as an error occurring in three bytes within one of the interleaves.
- Correctable triple burst errors must have three or fewer erroneous bytes per interleaves.
- Correct up to 72 bits I.E., 3 bytes per interleave. Guarantee to correct 65 bits.

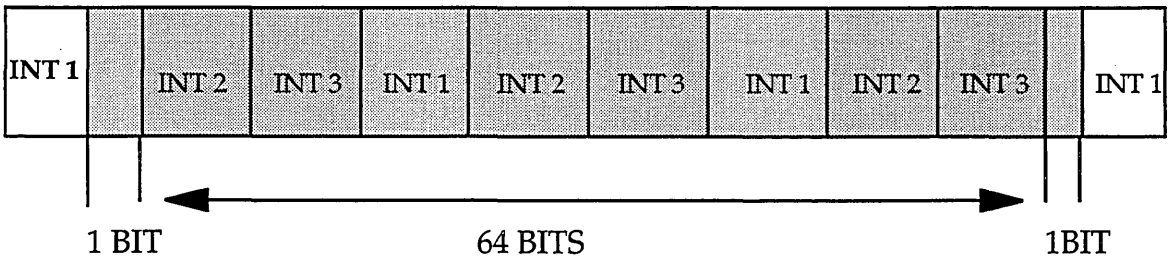
8.9.1 Correctable 72 Bit of Triple Burst Error



or



8.9.2 Uncorrectable 72 Bit of Triple Burst Error



8.10 Multiple Random Burst Errors

- Can correct up to 72 bits of multiple random errors, provided that the bytes in error follow the guidelines for correctable triple burst errors. Up to 48 bits of multiple random errors can be corrected On- the -Fly if two or fewer bytes per interleave.

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Chapter 9 Miscellaneous Information

9.1 Programmable Trigger

Firmware allows certain conditions to generate a scope trigger. The conditions under which a trigger pulse is generated is controlled by Configuration Page 12 which consists of one byte. The eight bits are used to control whether a pulse is to be generated on an associated condition. If the bit is set and the condition occurs, a 1 microsecond (approximately) pulse is generated. Multiple trigger conditions may be specified at a time. The supported bits and associated conditions are as follows:

Bit	Description
0	True bump
1	Seek time out
2	Seek fault
3	Tunafish error
4	ECC error
5	Sequencer read/write error
6	Sequencer overrun/underrun
7	Sequencer time out

As an example, to enable a pulse on either a seek time-out or ECC error, enter the following DIAG command line: DEPB 0 18 , WRCONF 12

The programmable scope trigger magically appears on microprocessor port P0.7.

9.2 Drive Parameter Analysis

Drive Parameter Analysis (DPA) feature has been implemented on Vortex AT drives. The DPA feature can be turned on by setting bit 7 byte 1 of config page 19 to one. Once the DPA feature is turned on the user can send **dpa enable** command to start monitoring some parameters of the Vortex AT drive.

A set of two sectors (107, 108) have been reserved on Cylinder -2 and -3 to store DPA related data and variables. Sector 107 to store DPA related variables and sector 108 is used to store Warranty Threshold Values.

An opcode B0H has been defined for DPA related commands. This command has a number of separate functions which are selectable by a subopcode via the Features Register. The drive checks a specific password in Cylinder Low & High Registers before it accepts a DPA Command as valid.

Password for a valid DPA Command is:

0x4F	Cylinder Low
0xC2	Cylinder High
0xB0	Command Opcode

The Vortex drive supports following DPA commands:

DPA Subcode	Function
0xD0	Returns Drive Attribute Values. The drive returns 512 bytes and saves the attributes to disk (sector 89 Cylinder -1)
0xD1	Read Warranty Threshold Values. The drive returns 512 bytes of data from Warranty Threshold values sector (sector 90 Cylinder -2, -3)
0xD2	Enable/ Disable Autosave
0xD3	Write Current Attribute Values to the disk (sector 89 Cylinder -2, -3)
0xD4	Perform Off - line data collection immediate Offline collection will start and scan the disk drive randomly for raw read error, this will execute until completion. This is background process and transparent to host. Activity will resume immediately if it is interupted by Host command.
0xD7	Write Warranty Threshold values to the disk (sector 90 Cylinder -2, -3)
0xD8	Enable DPA data collection and DPA Command decode
0xD9	Disable DPA data collection and DPA Command decode
0xDA	Check Warranty
0xDB	Enable/ Disable Off - line When Enable, Off-line data collection will be activated when there is no activity for certain period (specify by Enable command). Activity will be aborted if interrupt by Host command, and timer to activate again will be reset to next period. Every host command will reset to next period.

9.2.1 Drive Attributes Supported

Attribute ID Number	Attribute Name
1	Raw Error Rate
3	Spin Up Time
4	Start/stop Count
5	Reallocated Sector Count (grown defects)
7	Seek Error Rate
9	Power On Hours Count
11	Recal Retry Count
12	Drive Power Cycle Count
13	Read Soft Error Rate

9.2.2 Drive Attribute Value Data Structure

The following data structure defines the 512 bytes that make up the Drive Attribute Value information.

Bytes	Drive Attribute Data Structure Description
2	Data Structure Revision Number
12	First of the supported Drive Attributes
12	Second of the supported Drive Attribute
	..
	..
	..
12	30th of the supported Drive Attributes

6 Off - line data collection status bytes
Bytes

1 Off-line data collection Status Byte

0x8X The Auto-Off-Line feature is enable.
0xX0 No off-line data collection activity is in progress by the drive.
0xX2 All segment(s) of off-line asctivity were completed without error by the drive.
0xX4 Off-line data collection activity by the drive was suspended by an interrupting command from the host.
0xX5 Off-line data collection activity by the drive was aborted by an interrupting command from the host.
0xX6 Off-line data collection activity was aborted by the drive with fatal error.

2 Total segments required for off-line data collection byte. [0x01]
3-4 Total time in seconds to complete next segment bytes. [0x0016]
5 Current segment pointer. [0x01]
6 Off-line data collection Capability. [0x03]

0x01 EXECUTE OFF-LINE command is supported.
0x02 ENABLE / DISABLE AUTOMATIC OFF-LINE command is supported.

2 Drive Failure Prediction Capability Word
Bit
0 = Attributes Saved by Drive before Entering Power Mode
1 = Attributes Auto Save Capability
92 Reserved (0x00)
48 Vendor Unique (0x00)
1 Quantum Checksum Byte
1 Data Structure Checksum Byte
Total 512

The Data Structure Revision Number identifies which version of this data structure is implemented.
Quantum Checksum Byte is calculated so that sum of all bytes in Data Structure is 'C'.
The Data Structure Checksum is a simple 8 bit addition of the first 511 bytes in the data structure with the Checksum value being the two's complement of this sum.

9.2.3 Drive Attribute Format

Bytes	Drive Attribute Description
1	Attribute ID Number
2	Status Flags
1	Normalized Attribute Value
1	Worst Ever Normalized Attribute Value
6	Raw Attribute Value
1	Reserved (0x00)
Total 12	

9.2.4 Status Flags

Bit	Description
0	If set to 1, an Attribute value exceeding Threshold constitute a failure
1	If set to 1, the Attribute value is updated during on line testing
2	If set to 1, it's a performance Attribute
3	If set to 1, it's an error rate Attribute
4	If set to 1, it's an event count Attribute
5	If set to 1, it's self preserving Attribute
6	Reserved
7	Reserved
8-15	Reserved

9.2.5 Normalized Attribute Value

Valid numbers are 0x01 - 0xFE

Normalized Value	Description
0x01	Minimum value
0x64	Initial value prior to data collection
0xFE	Maximum value. Data count is saturated. Value not valid

9.2.6 Worst Ever Normalized Attribute Value

Valid numbers are 0x01 - 0xFE

Normalized Value	Description
0x01	Minimum value
0x64	Initial value prior to data collection
0xFE	Maximum value. Data count is saturated. Value not valid

9.3 AT Configuration Command Format

BYTE	BITS								DEFAULT
	7	6	5	4	3	2	1	0	
0-31	QUANTUM CONFIGURATION KEY								
32	RESERVED = 0						PE	CE	03H
33	Number of CACHE Segments								08H
34	RESERVED = 0								00H
35	RESERVED = 0								00H
36	AWRE	ARRE	TB	RC	EEC	PER	DTE	DCR	C0H
37	NUMBER OF RETRIES								08H (1)
38	ECC CORRECTION SPAN								18H (2)
39	0	ARE	AARM	RESERVED = 0		WCE	RUEE	0	66H
40-511	RESERVED = 0								00H

KEY:

PE	Prefetch Enable
CE	Cache Enable
AWRE	Automatic Write Reallocation Enable
ARRE	Automatic Read Reallocation Enable
TB	Transfer Block
RC	Read Continuous
EEC	Enable Early Correction
PER	Post Error
DTE	Disable Transfer on Error
DCR	Disable Correction
ARE	Auto Read Enable
AARM	Auto Arm Auto Read
WCE	Write Cache Enable
RUEE	Reallocation Uncorrectable Error Enable

COMMENTS:
1. This number reflects number of times through group retry sequence.
2. Triple burst correction and double burst on the fly enabled.

9.4 Configuration Pages

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 0	0	0	Customer no.		1	1	0
Pg 1	0	1	Jumper setting		2	2	0
Pg 2	0	15	Vendor name	16 bytes ASCII characters	16	16	"QUANTUM "
Pg 3	0	15	Product ID	16 bytes ASCII characters—model dependent	16	16	"VORTEX_1275A " or "VORTEX_2550A "
Pg 4	0	7	Drive Revision	where I = interface (A/S) rr = rom rev dd = diskware rev c = fmt/conf rev s = selfscan rev	8	8	Irr.ddcs
Pg 5	0	11	Drive Serial No.	12 bytes of drive serial # in ASCII	12	12	—
Pg 6	0	31	Customer Name	32 bytes customer name in ASCII	32	32	"GENERIC" padded with " "
Pg 7	0	0	AT Config Flags	Misc1	1	10	060h
	1	1		Misc2	1		04Ch
	2	3		Logical cylinders/drive	2		2492/4994
	4	4		Logical heads/cylinder	1		16
	5	5		Logical sectors/track	1		63
	6	6		Minimum power time	1		1
	7	7		Transfer read delay	1		80
	8	8		Transfer write delay	1		80
	9	9	Page revision number		1		0
Pg 8	0	0	Number of heads	Model dependent	1	1	2 or 4
Pg 9	0	15	Configuration validation	0, 1, FF,2,FE,3,FD,4,FC,5, FB,6,FA,7,F9,8	16	16	<---
Pg 10			Non Adaptive Zone Table			491	
	0	1	starting cylinder		2		0
	2	5	Starting logical sector address		4		xxxx
	6	7	Sectors per track	192 sect/track for Z0, system	2		0C0h
	8	9	Sectors per zone		2		xx
	10	10		Unused			0
	11	11	Z0_10	M value for clock synthesizer	1		5B

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 10	12	12	Z0_11	N value for clock synthesizer	1		1D
	13	13	Z0_12	Clock synthesizer loop res/multiplier	1		E4
	14	14	Z0_17	Servo Continuous Filter Cutoff Freq	1		5A
	15	15	Z0_19	Tune	1		4A
	16	16	Z0_1A	TWAI/TWAO	1		5
	17	17	Z0_1B	8 LSBs flash digitizer output latch counter	1		0
	18	18	Z0_1D	AGC internal capacitor	1		BF
	19	19	Z0_1E	Servo Control	1		F1
	20	20	Z0_21	TST1/TST2 output port select	1		40
	21	21	Z0_23	Frequency	1		80
	22	22	Z0_26	Quality Monitor Control	1		A0
	23	23	Z0_27	ENDEC Control	1		E0
	24	24	Z0_28	ENDEC Control	1		7
	25	25	Z0_29	RD/WR Gate Logic/Extended WR gate	1		61
	26	26	Z0_2A	Power Mode Select	1		80
	27	27	Z0_2D	Read Path test	1		0
	28	28	Z0_2E	Digital Test	1		0
	29	29	Z0_2F	Test Mode Select	1		0
			Zone				
	30	59	1	Same as 0-29	30		
	60	89	2	Same as 0-29	30		
	90	119	3	Same as 0-29	30		
	120	149	4	Same as 0-29	30		
	150	179	5	Same as 0-29	30		
	180	209	6	Same as 0-29	30		
	210	239	7	Same as 0-29	30		
	240	269	8	Same as 0-29	30		
	270	299	9	Same as 0-29	30		
	300	329	10	Same as 0-29	30		
	330	359	11	Same as 0-29	30		
	360	389	12	Same as 0-29	30		
	390	419	13	Same as 0-29	30		
	420	449	14	Same as 0-29	30		
	450	479	15	Same as 0-29	30		
	480	481	Total Cylinders	Data Cylinders=5738	2		166A
	482	485	Maximum Logical Sector Address		4		2512843 or 5034290 (2 disk)

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 10		486	Head (track) wedge skew	Set to 40	1		28h
		487	Cylinder wedge skew	Set to 44	1		2Ch
		488	Number of Zones	N=16	1		10H
		489	Wedges Per Track	W=96	1		60h
		490	Page Revision Number		1		0
Pg 11	0	3	Number of User Sectors	# of user accessible sector at ROM default—LSB first	4	4	0FFH, 0FFH, 0FFH, 0FFH
Pg 12	0	0	Trigger Msk	0 - true bump 1 - seek timeout 2 - servo fault 3 - tunafish error 4 - ecc error 5 - sequencer r/w error 6 - sequencer underrun/overrun 7 - sequencer timeout	1	1	00
Pg 13	0	1	Drive family and Model	Family = 0CH, Model = 2, 4 (heads)	2	2	0CH, 2 or 0CH, 4
Pg 14	0	5	HW head map	Hardware head map, user head map	6	6	03H,0,0, 03H,0,0 or 0FH,0,0, 0FH,0,0
Pg 15			Diskware Overlay				
	0	0	overlay number: 0	Vector table	1	111	
	1	3	RAM load address		3		
	4	4	Size in sectors		1		
	5	6	Cylinder		2		
	7	8	Alternate cylinder		2		
	9	10	Sector		2		
	11	21	Overlay 1	F/W Resident overlay	11		
	22	32	Overlay 2	Main Overlay	11		
	33	43	Overlay 3	SelfScan Overlay 0	11		
	44	54	Overlay 4	SelfScan Overlay 1	11		
	55	65	Overlay 5	SelfScan Overlay 2	11		
	66	76	Overlay 6	SelfScan Overlay 3	11		
	77	87	Overlay 7	SelfScan Overlay 4	11		
	88	98	Overlay 8	Reserved	11		
	99	109	Overlay 9	Reserved	11		

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 15	110	110	Page rev. no.		1		0
Pg 16	0	1	HDA control Flags	0 - no_spin_down 1 - rcal_on_fatal_err 2 - no_find_mode 3 - kill_low_pwr 4 - temp_idle_servo 5 - trace_dac_on 6 - rd_on_arrival 7 - physical_8k_buf	2	2	40H, 0
Pg 17			Adaptive Zone Table				
	0	0	Z0_HD0_00	DC Tap	1	1985	A0h (Adaptive)
	1	1	Z0_HD0_01	TAP 1	1		64h
	2	2	Z0_HD0_02	TAP 2	1		D2h
	3	3	Z0_HD0_03	TAP 4	1		B4h
	4	4	Z0_HD0_04	TAP 5	1		5Ah
	5	5	Z0_HD0_05	TAP 6	1		B4h
	6	6	Z0_HD0_06	TAP 7	1		46h
	7	7	Z0_HD0_07	TAP 8	1		6Eh
	8	8	Z0_HD0_08	TAP 9	1		91h
	9	9	Z0_HD0_09	TAP 10	1		46h
	10	10	Z0_HD0_0A	TDFE TAP 1	1		91h
	11	11	Z0_HD0_0E	TDFE TAP 2	1		91h
	12	12	Z0_HD0_0C	TDFE TAP 3	1		78h
	13	13	Z0_HD0_0D	TDFE TAP 4	1		73h
	14	14	Z0_HD0_0E	TDFE TAP 5	1		78h
	15	15	Z0_HD0_0F	VGA	1		82h
	16	16	Z0_HD0_13	FRNGR	1		6Bh
	17	17	Z0_HD0_14	ZERO Frequency	1		95h
	18	18	Z0_HD0_15	ATT	1		62h
	19	19	Z0_HD0_18	Servo Zero Frequency	1		2Ah
	20	20	Z0_HD0_1F	AQUAL	1		08h
	21	21	Z0_HD0_20	Write Precompensation	1		84h
	22	22	Z0_HD0_22	GUG/TWUG	1		C3h
	23	23	Z0_HD0_24	PHUG	1		4Fh
	24	24	Z0_HD0_30	PA	1		40h
	25	25	Z0_HD0_31	LDFE TAP 1	1		20h
	26	26	Z0_HD0_32	LDFE TAP 2	1		20h
	27	27	Z0_HD0_33	LDFE TAP 3	1		20h
	28	28	Z0_HD0_34	LDFE TAP 4	1		20h
	29	29	Z0_HD0_35	DFE Delay	1		03h
	30	30	Z0_HD0_WCR	Write Current	1		02h
			Head				
	31	61	HD1	Same as 0 - 30	31		
	62	92	HD2	Same as 0 - 30	31		
	93	123	HD3	Same as 0 - 30	31		

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 17			Zone				
	124	247	1	Same as 0 - 123	124		
	248	371	2	Same as 0 - 123	124		
	372	495	3	Same as 0 - 123	124		
	496	619	4	Same as 0 - 123	124		
	620	743	5	Same as 0 - 123	124		
	744	867	6	Same as 0 - 123	124		
	868	991	7	Same as 0 - 123	124		
	992	1115	8	Same as 0 - 123	124		
	1116	1239	9	Same as 0 - 123	124		
	1240	1363	10	Same as 0 - 123	124		
	1364	1487	11	Same as 0 - 123	124		
	1488	1611	12	Same as 0 - 123	124		
	1612	1735	13	Same as 0 - 123	124		
	1736	1859	14	Same as 0 - 123	124		
	1860	1983	15	Same as 0 - 123	124		
		1984	Page rev. no.		1		0
Pg 18	0	355	Non Adaptive Servo		364	364	
Pg 19			DPA (phase4)		23	23	0
	0	0	EL_PERIOD	Auto update period	1		0
	1	1	DPA Master Switch	Bit 7=On/Off = Enable/Disable	1		80h
	2	5	SEEK_DR	Max. # of seeks/data range	4		16000
	6	7	MAX_SK_ERROR_DR	Max. # of seek errors/data range	1		13
	8	11	READ_DR	Max. # of sectors read/data range	4		100000
	12	12	MAX_RD_ERROR_DR	Max. # of read errors/data range	1		13
	13	14	SPINUP_DR	Max. # of spinup/data range	2		20
	15	16	MAX_SPIN-UP_DR	Maximum spinup time	2		25000
	17	17	RECAL_DR	Max. # of recal/data range	1		10
	18	18	EL_SPARE	SPARE	1		0
	19	20	MAX_OFF LINE_BLK_ DR	Max # of offline read per segment	2		2500
	21	21	MICRO_OFF LINE_BLK	Max # of offline read per random LBA	1		255
	22	22	MAX_OFF LINE_ERR_ DR	Max # of offline read error per segment	1		250

Page	From byte	To byte	Function	Description	Bytes	Length	Default
	23	23	Page Revision Number		1		0-DPA Rev.
Pg 20	0	0	Not Used		1	1	0
Pg 21	0	511	Adaptive Servo		512	512	-
Pg 22			Not Used				
Pg 23	0	0		Not Used	1	1	0
Pg 24				Identify Drive Page			
	0	137		Parameters for AT Identify Drive Command (i.e. DMA cycle timing parameters)	138	138	Up to 69 words of AT CAM Spec. ID Command. Words 70- 256 = Reserved.

9.5 Firmware Error Code

Error Code	Description
0	No Error detected at Drive level
1	EC_BUFFER_RAM Error probably found in diagnostIc
2	EC_SEQ_RAM_FAIL Fail write sequencer format table
3	EC_SEQ-ROLLOVER Fail write sequencer format table
4	EC_ROM_CHKSUM Internal ROM checksum error
5	EC_DW_CHKSUM Internal ROM checksum error
6	EC_READ_DISKWARE Error during reading of diskware
7	EC_WRONG_VERSION Markers incompatible
8	EC_INV_COMMAND Invalid command
9	EC_INV_LBA Invalid LBA
A	EC_INV_CDB Invalid bits set in CDB
B	EC_INV_PARAMETER Invalid field in parameters
C	EC_INVALID_CYL Invalid cylinder specified
D	EC_INVALID_HEAD Invalid head specified
E	EC_INVALID_SECTOR Invalid sector specified
F	EC_REC_BAD_FORMAT Read Defect Data format not avail
10	EC_BAD_MODE_PAGE Bad parms in mode page while init
11	EC_RESET_OCCURRED Reset occurred
12	EC_BAD_DFCT_LIST Bad defect list
13	EC_NO_ALT_SECTS No more alternate sectors available
14	EC_DFCT_LIST_FULL Defect list is full
15	EC_ASSERT_ERROR Firmware consistency check err
16	EC_WRITE_SYSTEM Error in writing system sector
17	EC_READ_SYSTEM Error in reading system sector
18	EC_FW_AUTOWRERR Autowr cmd received while host channel disabled
19	EC_BAD_FMT_HEADER Bad format header data
1A	SYS_NOT_USED_1
1B	SYS_NOT_USED_2
1C	SYS_NOT_USED_3
1D	SYS_NOT_USED_4
1E	EC_DATA_SYNC_TMO Data field sync timeout
1F	EC_DATA_SYNC_TMO Recovered data field sync timeout
20	EC_ID_ECC ID ECC error
21	EC_ID_ECC Recovered ID ECC error
22	EC_ID_SYNC_TMO AM not found for ID field
23	EC_ID_SYNC_TMO Recovered ID AM mark not found
24	EC_NO_RECORD_FOUND No record found
25	EC_NO_RECORD_FOUND Recovered no record found
26	EC_CRC_CONT Marker for CRC/Continue
27	EC_CRC_CONT Recovered marker for CRC/Continue
28	EC_ID_MISCOMP Read, write ID miscompare
29	EC_ID_MISCOMP Recovered read, write ID miscompare
2A	EC_ID_AM_CONT AM not found ID intern continue
2B	EC_ID_AM_CONT Recovered ID AM not found continue
2C	EC_INVALID_DATA Realloc of uncorrectbl data
2D	EC_INVALID_DATA Recovered realloc of uncorrectbl data
2E	EC_UNDERRUN Underrun error
2F	EC_UNDERRUN Recovered underrun error
30	EC_WG_IN_WEDGE Write gate asserted wedge detected
31	EC_NO_INDEX FOUND No disk index found on track

Error Code	Description
32	EC_WRITE_FAULT Write fault
33	EC_WRITE_FAULT Recovered Write fault
34	EC_SEQ_TIMEOUT Sequencer timeout
35	EC_SEQ_TIMEOUT Recovered sequencer timeout
36	EC_UNXPCTD_TIMEOUT Unexpected sequencer error
37	EC_UNXPCTD_TIMEOUT Recovered unexpected sequencer error
38	EC_DATA_ECC Uncorrect data field ECC error
39	EC_DATA_ECC Recovered uncorrect data field ECC error
3A	EC_ON_FLY_CORRECTED
3B	EC_REC_DATA_EQUAL Recovered data w/2 = syndromes
3C	EC_REC_DATA_LAST Recovered data ECC last retry
3D	EC_EC_STATUS Invalid error _code in r/w
3E	EC_ECC_UNDER_WEDGE
3F	EC_ECC_UNDER_WEDGE Recovered
40	RW_NOT_USED_3
41	RW_NOT_USED_4
42	EC_RECALING Drive up to speed and recaling
43	EC_SPINNING Drive is spinning up
44	EC_STOPPED Drive not been told to spin up
45	SV_NOT_USED_5
46	SV_NOT_USED_6
47	EC_SERVO_DEFECT Unrecoverable Servo Defect
48	EC_SERVO_DEFECT Recovered Servo Defect
49	EC_BAD_SYNC Unrecoverable Bad servo sync
4A	EC_BAD_SYNC Recovered Bad servo sync
4B	EC_BAD-SAM Unrecoverable Bad SAM
4C	EC_BAD-SAM Recovered Bad SAM
4D	EC_BAD_TRKNUM_OR_INDEX Unrecovered Bad track numb data
4E	EC_BAD_TRKNUM_OR_INDEX Recovered Bad track numb data
4F	EC_BAD_HEAD_SELECT Head from ID != selected head
50	EC_BUMPED Unrecoverable Bump
51	EC_BUMPED Recovered Bump
52	EC_BUMP_TIMEOUT Bump timeout
53	EC_BUMP_TIMEOUT Recovered bump timeout
54	EC_UNEXPECTED_TRK_ID Unrecovrd Gray code != desired
55	EC_UNEXPECTED_TRK_ID Recovrd Gray code != desired
56	EC_LOST_LOCK Unrec mult bad Sync/SAM Settle/Ontrk
57	EC_LOST_LOCK Recovered mult bad Sync/SAM Settle/Ontrk
58	EC_OUT_SPEED Unrecoverable Speed out of range
59	EC_OUT_SPEED Recovered Speed out of range
5A	EC_SVO_STATUS Invalid servo_status w/err bits set
5B	EC_SVO_STATUS Recovered invalid servo_status
5C	SVO_NOT_USED_1
5D	SVO_NOT_USED_2
5E	SVO_NOT_USED_3
5F	SVO_NOT_USED_4
60	EC_SEEK_ERROR Seek error
61	EC_SEEK_ERROR Recoverd seek error
62	EC_SEEK-TIMEOUT Seek timeout with no servo fault
63	EC_SEEK-TIMEOUT Recovered seek timeout with no servo fault
64	EC_SEEK_LOST_LOCK Unrec mult bad Sync/SAM Seek ISR
65	EC_SEEK_LOST_LOCK Recovered mult bad Sync/SAM Seek ISR

Error Code	Description
66	SK_NOT_USED_0
67	SK_NOT_USED_1
68	EC_MOTOR_FAULT Motor unable to get up to speed
69	EC_MOTOR_FAULT Recovered motor unable to get up to speed
6A	EC_RCL_CS_PES Coarse Slope PES Gain calibration
6B	EC_RCL_CS_PES Recovered coarse Slope PES Gain calibration
6C	EC_RCL_AEQBH Fine Slope PES Gain calib AEQBH
6D	EC_RCL_AEQBH Recovered fine Slope PES Gain calib AEQBH
6E	EC_RCL_AEQBL Fine Slope PES Gain calib AEQBL
6F	EC_RCL_AEQBL Recovered fine Slope PES Gain calib AEQBL
70	EC_RCL_ON_TRACK RCL FLT Cannot Lock to track
71	EC_RCL_ON_TRACK Recovered cannot Lock to track
72	EC_RCL_NO_SAM Can't detect SAM during unparking
73	EC_RCL_NO_SAM Recovered detect SAM during unparking
74	EC_RCL_DAC_OFF DAC offset calibration failure
75	EC_RCL_DAC_OFF Recovered DAC offset calibration failure
76	EC_RCL_MAP_HDS Cant detect reliable SAM any head
77	EC_RCL_MAP_HDS Recovered detect SAM on any head
78	EC_RCL_SK_OD Can't seek to OD near Sys Cyl
79	EC_RCL_SK_OD Recovered seek to OD near Sys Cyl
7A	EC_RCL_SK_FS_PES Cant seek Fine Slope PES cal trk
7B	EC_RCL_SK_FS_PES Recovered seek Fine SLP cal trk
7C	EC_RCL_SK_NULLI Seek fail during Nulli calibratn
7D	EC_RCL_SK_NULLI Recovered seek fail during Nulli calibratn
7E	EC_RCL_SK_VSCALE Seek fail during V_SCALE adapt
7F	EC_RCL_SK_VSCALE Recovered seek fail during V_SCALE adapt
80	EC_RCL_SK_KLOOP Seek failure during KLOOP calibr
81	EC_RCL_SK_KLOOP Recovered seek failure during KLOOP calibr
82	EC_RCL_SK_RRO Seek failure during RRO calibration
83	EC_RCL_SK_RRO Recovered seek fail during RRO calibration
84	EC_RCL_SK_REZERO Seek failure to track 0 during rezero
85	EC_RCL_SK_REZERO Recovered seek fail to track 0 during rezero
86	EC_RCL_KLOOP Unable to complete KLOOP calibration
87	EC_RCL_KLOOP Recovered to complete KLOOP calibration
88	EC_RCL_RRO Unable to complete RRO calibration
89	EC_RCL_RRO Recovered to complete RRO calibration
8A	EC_RCL_LOCK_SAM Unable to lock TNA in OD unpark
8B	EC_RCL_LOCK_SAM Recovered lock TNA in OD unpark
8C	EC_RCL_UNPRK_TRK_TOUT TNA lock tout wait unpk trk
8D	EC_RCL_UNPRK_TRK_TOUT Recovered found unpk trk
8E	EC_RCL_CANT_READ_TRK TNA lock, trkid fail unpktrk
8F	EC_RCL_CANT_READ_TRK Recovered trk id while unprk
90	EC_RCL_CANT_STOP_VCM VCM too fast
91	EC_RCL_CANT_STOP_VCM Recovered VCM too fast
92	RCL_NOT_USED_0
93	RCL_NOT_USED_1
94	RCL_NOT_USED_2
95	RCL_NOT_USED_3
96	RCL_NOT_USED_4
97	EC_INV_FP_REVISION Invalid revision in the failure prediction structure
98	EC_INV_FP_FEATURES Invalid function in the features register

Error Code	Description
99	EC_FP_DISABLE Failure prediction operations are disabled
9A	EC_READ_FP_SECTORS Unable to read the failure prediction parameters from the media
9B	EC_WRITE_FP_SECTORS Unable to write the failure prediction parameters from the media
9C	EC_INV_FP_PASSWORD Invalid password for executing drive failure prediction
9D	EC_INV_FP_CHKSM Invalid checksum in the warranty threshold data structure

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Firmware

Bill Levdar

BIGFOOT

Firmware Presentation

by Bill Levdar

Bigfoot Firmware Features

- *1. Firmware derived from Trailblazer code*
- *2. Support for Shiva read channel*
- *3. Selfscan implementation similar to Fireball*
- *4. Superset cmds implementation similar to Fireball*
- *5. New defect management*

Major areas of Change

- *Support for more than 256 sectors per track*
- *LBA based Defect Management*
- *Servo Defect Mapping*
- *Improved Defect Scanning Algorithms*
- *Read Channel Optimization*
- *S.M.A.R.T. Phase 4*

Bigfoot Track Format

- *First Quantum drive to support more than 256 sectors per track ;*

  data structures,

  internal calculations, and
  I/O structures for Superset cmds

  were changed to support ***Word size***

  data

Double Sectors per Track Format

- *RAION ASIC does not support > 256 sec/trk*
- *Implementation :*

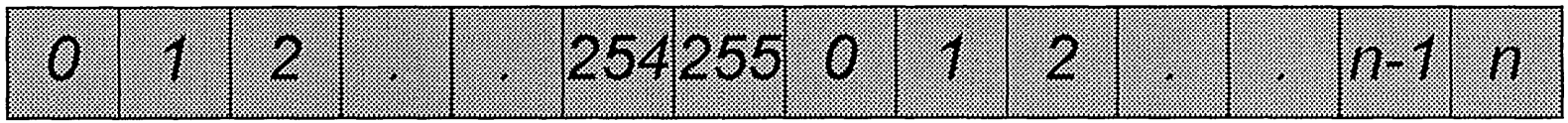
  Track divided into two parts...

  *If **"m"** is number of sectors per track.*

  First set of sectors 0 to 255

  *Second set , 0 to **"m"**-256 -1 plus one bit of cylinder/head ID byte*

set 1 *set 2*



Total sectors/Track = m = 256 +n+1

Servo Defect Mapping

- *Fireball Servo Defect mapping scheme*
  - *. Two defective wedges per track allowed*
  - *. Determined during SelfScan Servo Verify*
  - *. Servo Defect List saved to disk*
- *Bigfoot Scheme*
  - *. Six consecutive wedges mapped out in Data Defect List*
  - *. Special entry for a Bad Track*
  - *. 127 Entries allowed in Servo Defect List*

System Cylinders

- *Five System Cylinders Reserved*

  Data is stored on heads 0 & 1 in OD area.

  Customer cannot access, physical address cmds only.

Cylinder	***Description***
-1	*Test Data/Error Logging*
-2	*System*
-3	*Copy of Cylinder -2*
-4	*Diskware*
-5	*Copy of Cylinder -4*

Test Equipment and Error Logging Cylinders

- *Copy of servo writer Serial Number Data*
- *Test Process Interlock*
- *Configuration Center Control*
- *Test Process History Queue*
- *Process Test Defect List*
- *Self Scan Results*
- *Self Scan Test Parameters*
- *Self Scan defect list*
- *Self Scan Servo defect map*
- *Soft error table*
- *Runout results*
- *S.M.A.R.T attributes/variables/thresholds*
- *Self Scan variables Save/Restore*
- *Performance Test results*
- *Adaptive results*

System Cylinders

- Cylinders -2 and -3
  - Saved Mode Parameters
  - Configuration Pages
  - Working Defect List
  - Primary Defect List
  - T- List
  - Format Header Bytes (zone 0 - 15)
  - Servo Defect List
  - Recal Record

Firmware Cylinders

- *Cylinders -4 and -5*
  - *Vector table*
  - *Resident Code*
  - *Overlays*

Rom and Diskware Code

- NEC K-3 Microprocessor

Rom Code	32 K
Resident Diskware	16 K
Overlay Diskware	8 K
Cache Buffer	87.5 K

Rom Code

- Firmware in ROM
  - Code to power up drive
  - Code to Download Diskware into Buffer
  - Code to allow Diskware to be written to disk via Host Interface
  - Minimal Superset cmds for debug
  - All time critical Code

Diskware Code

- *Firmware in Diskware*
  - *Resident .. Vector Table, Code*
  - *Overlay .. SelfScan*
  - *Provisions for ROM bugs to be fixed in Diskware*

Diskware Download Operation

- *Write Buffer Cmd will download Diskware.*
- *Download Elements*
  - *Diskware Downloader*
  - *Diskware Control Page*
  - *Diskware Overlay Entries*

Diskware Downloader

- *Validate Diskware Control Page and Diskware Overlay Entries with checksum*
- *Validate Product Code*
- *Compare ROM version stamp and checksum*
- *Load Diskware directed by Diskware Control Page*
- *Initialize Mode ,Configuration Pages, and Run*
- *Download and Save as specified in Control Page*

Error Correcting Code

RAION	**vs**	**KONI**
* 8 bits per symbol		Same
* 3 Interleaves		Same
* 6 redundancy bytes per int'lv		4 redundancy bytes..
* 2 cross-check bytes		Same
* 18 ECC bytes & 2 CRC bytes		12 ECC & 2 CRC
* Single Error Corr'tn(on-the-fly)		Same
* Double Error Corr'tn(on-the-fly)		Not on-the-fly
* Triple Error Correction		Not Available
* 3 Bytes CRC per ID field		Same

ECC Summary

- *ECC hardware is REED-SOLOMON .*
- *All corrections done in Firmware*
- *Cross-check bytes used to "double check" the correction.*
- *ON-the-fly correction does not require more than one disk rotation to do correction*
- *Triple burst can correct up to 72 bits*

Programmable Trigger

- *Firmware allows Config page 12 to program a trigger output. (1Us) Port P0.7*
  - *True Bump*
  - *Seek Time Out*
  - *Seek Fault*
  - *Tunafish Error*
  - *ECC Error*
  - *Sequencer Read/Write Error*
  - *Sequencer overrun/underrun*
  - *Sequencer Time Out*

Defect Management

Kurt Rusnak

BIGFOOT DEFECT MANAGEMENT

BIGFOOT DEFECT MANAGEMENT

I. Overview

A. Previous Methods

1. Working list (W-List) is sorted by physical CHS of the defects.
2. W-List entries contain the physical CHS of each defect.
3. Inline defects limited (usually 'n' per cylinder). Inlines cause LBAs to 'slip' to the spare sectors at the end of each cylinder.

B. New Method ("LBA Based")

1. Working list (W-List) is sorted by LBA.
2. W-List entries do **not** contain the physical CHS of the defects.
3. Inline defects are virtually unlimitted. Inlines cause LBAs to 'slip' to the spares tracks at the ID of the drive.
4. Allows mapping out entire tracks.
5. Offline spares unchanged (still 1 spare per cylinder).

C. SelfScan/Process Considerations

1. Bigfoot has sufficient spare tracks at the ID to allow all defects found in SelfScan to be inlined.
2. However there may be factory-offlines do to 'additional defects' found in SelfScan after the inline process.

II. Defect List Structures

A. SelfScan/Servo Defect Lists

1. SelfScan defect list contains all relevant information on defects found by SelfScan (such as counts, patterns, etc.).

2. UPT2 'rptss' script can be used to interpret the SelfScan list entries.

3. Only C,H,S fields are used by defect management. Each Selfscan list entry generates one P-List entry.

4. Servo defect list is generated by SelfScan Servo Verify and contains a list of mapped-out wedges (up to 2 non-consecutive wedges per track). This list is then used by the Servo-System firmware.

B. P-List

1. This is the 'primary-list' or 'factory-found' defect list. It is normally generated from the SelfScan and Servo defect lists in the SelfScan Factory-Format command (sometimes called the Format-Inline command). It may also be generated from user-supplied defect entries via the Factory-Format superset command.

2. The P-List is stored in the system area (cylinder -2, sectors 25-40) and is not maintained in RAM during normal drive operation.

3. Each entry in the P-List specifies either a single defective sector, or a single defective track. This list is sorted by ascending CHS.

4. Each P-List entry is 8-bytes, formatted as follows:

Byte Offset	Contents	
0	Status Byte	<<~~~~ bit-1: defective track
1-2	not used	bit-2: factory (always set)
3	Defect Head	bit-3: ID defect (not used)
4-5	Defect Cylinder	
6-7	Defect Sector	(= FEFEH if 'defective track' bit set)

C. T-List

1. In the SelfScan or superset Factory-Format command, the P-List is used to generate the working list (W-List). In the process of generating the W-List, a temporary list (T-List) is created and saved in the system area (cylinder -2, sectors 41-56).

2. The format of the T-List entries is identical to that of the P-List with one exception. Bit-5 of the Status Byte is set for defect entries that are inlines or defective tracks, and this bit is clear for defect entries that are offlines.

D. W-List

1. This is the working list which is generated from the P-List in the SelfScan or superset Factory-Format command. It is stored in the system area (cylinder -2, sectors 9-25) and is also maintained in the drive's buffer RAM at all times during normal operation.

2. Initially (upon leaving the factory), the W-List corresponds exactly to the P-List (which in turn corresponds to the SelfScan defect list).

3. The W-List may subsequently deviate from it's initial factory condition in several ways. In all cases, the current W-List in RAM is always the same as that stored in the system area of the drive.

    i) "Grown (offline) defects" may be added to the W-List by means of the Auto-Reallocation feature.

    ii) User-specified (offline) defects may be added to the W-List by means of the Reassign-Physical superset command.

    iii) The W-List may be cleared by means of the Format-Drive superset command. (This command also performs a Format Track Physical on every track of the drive.)

4. The contents of the W-List may be displayed using the 'rddef' command under DIAG or ATADIAG.

III. The Working List (W-List)

A. W-List: Entry Format

1. Unlike previous defect management methods, each entry in the W-List does not necessarily correspond to a single defective sector. In fact, the meaning of each field in an entry depends on the 'type' of entry. Each entry consists of 8 bytes with the following format:

Byte Offset		Contents
0	bits 0-3	Zone number
	bits 4-7	Entry type
1-3		LBA
4		Cylinder (lsb)
5	bits 0-4	Cylinder (msb)
	bit 5	Pending bit
	bits 6-7	Head
6		Sector/SPT (lsb)
7	bit 0	Sector/SPT (msb)
	bits 1-7	SPT2

2. Note that byte-4 and bits 0-4 of byte-5 form a 13 bit Cylinder field. Note that byte-6 and bit-0 of byte 7 form a 9 bit Sector/SPT field. The meanings of "Pending bit" and "SPT2" will be described later.

3. The 'entry type' field defines the type of entry, which in turn affects the meaning of the other fields:

	entry type				
Byte-0, bit....	7	6	5	4	
	x	x	1	1	.....end marker
	x	x	0	0	.....zone (factory)
	x	x	1	0	.....inline (factory)
	0	0	0	1	.....offline (factory)
	0	1	0	1	.....offline (auto-reallocated)
	1	0	0	1	.....offline (host-reassigned)
	1	1	0	1	.....offline (new pending-auto)

B. W-List: Zone Entries

1. Zone entries do not correspond to defects, but rather denote the starting track of each user-zone on the drive. These are the points of discontinuity where the "sectors-per-track" values change.

2. Initially (in a drive with no mapped defects), the W-List contains only the zone entries followed by the end-marker.

3. The fields in a zone entry have the following meanings:

   i) "Zone Number" has the obvious meaning. In Bigfoot, the system zone is zone-0 and only user-area defects are put into the W-List. Therefore, Zone Number field values range from 1 to 15.

   ii) "LBA" is the LBA number of the first sector of the zone. Note that in the sequential numbering of LBA values, inlined defects (and the offline spare sector at the end of each cylinder) are skipped. Thus, the LBA value for a zone entry depends on the number of inlines preceding the zone. For example, on a Bigfoot-2550 with no inlines, the first LBA in zone-2 is 6603DH. However, if there are 5 inline defects in zone-1, then the first LBA in zone-2 will be 66038H. This means that the physical sector corresponding to LBA 6603DH has been 'shifted' 5 sectors toward the ID of the drive.

   iii) "Cylinder" and "Head" are the physical cylinder and head values of the first track of the zone. (Note that the Head value is always zero.) Thus the Cylinder/Head fields of the zone entries define the physical zone boundaries of the drive.

   iv) "Sector/SPT" is the 'raw' sectors-per-track value for the zone. This is the number of sectors on tracks that have no inlines.

   v) "Pending Bit" and "SPT2" are not used in zone entries and will have zero values.

C. W-List: Inline Entries

1. As with zone entries, each inline entry in the W-List does not specify an individual defect. Rather each inline entry specifies a track which contains one or more inlined sectors. Note that zone and inline entries specify tracks where the sectors-per-track value has a discontinuity.

2. An inline entry specifies a track's physical location, its starting LBA, and information regarding the number of inlines on the track. The actual sector-numbers of the inlined sectors are not available in the W-List.

3. The fields in an inline entry have the following meanings:

   i) "Zone Number" is the zone number of the track containing the inlines.

   ii) "LBA" is the LBA number of the first sector of the track containing the inlines.

   iii) "Cylinder" and "Head" are the physical cylinder and head values of the track containing the inlines. The "Pending Bit" is not used by inline entries.

   iv) "Sector/SPT" is the sectors-per-track remaining on the track after the inlined defective sectors have been removed. This value does not include the offline spare sector at the end of each cylinder. The number of inlines on the track equals the sectors-per-track in the zone minus the value of this field. We map out an entire track by specifying a zero value for this field.

   v) "SPT2" is the number of sectors on the track that have original physical sector numbers greater than 255. Due to the way that the firmware supports tracks with more than 255 sectors (this is not directly supported by RAION), the sectors are divided into 2 sets: the "1st set" of sectors are those with sector numbers less than 256, and the "2nd set" are those with sector numbers greater than or equal to 256. Thus "SPT2" is the number of sectors in the "2nd set". This is needed to determine the Sequencer Rollover value for RAION.

D. W-List: Offline Entries

1. Unlike zone and inline entries, each offline entry corresponds to a single defective sector. However, the offline entry contains only the LBA and replacement sector information, not the physical location of the defect (except in the case of "pending defects" described below).

2. Bigfoot allows factory-generated offline defects to be added to the W-List in SelfScan in the following way. After all physical scanning is done in SelfScan, the defects found are inlined in the Factory-Format command. This causes tracks with inlines to be re-formatted, which can cause the IDs on the track to be positioned slightly differently than they were during the scanning. As a result, very small defects which were previously undetected could generate ID errors after the inlining. Thus, if such defects are found in the initial customer-scan after the inline process, we will offline-spare them.

3. Under normal user operation, all defects added to the W-List are added as offline entries. These additional defects may be created in 2 ways:

   i) By auto-reallocation of grown defects.

   ii) By the reassign-physical superset command.

4. The fields in an offline entry have the following meanings:

   i) "Zone Number" is the zone number of the replacement sector.

   ii) "LBA" is the LBA of the defective (replaced) sector.

   iii) "Cylinder", "Head", "Sector/SPT" is the physical C,H,S of the replacement sector.

   iv) "SPT2" is not used by offline entries.

   v) "Pending Bit" is used by the auto-reallocation feature. This bit indicates that the sector generated an uncorrectable read error, but the sector has not yet been auto-reallocated. In this case, the "Cylinder,"Head","Sector/SPT" fields define the physical C,H,S of the sector that generated the error.

IV. Auto-Reallocation

A. Mode Settings

1. There are 3 bits in the AT Read/Write Configuration commands that affect auto-reallocation. The current generic factory configuration for Bigfoot is that all 3 modes are enabled:

   i) AWRE...."automatic write reallocation enable". Enables auto-reallocation of unrecoverable write errors. This bit is bit-7 of "ERBITS" of DIAG/ATADIAG's "atrdconfig/atwrconfig" commands.

   ii) ARRE...."automatic read reallocation enable". Enables auto-reallocation of ECC (non on-the-fly) correctable read errors. This bit is bit-6 of "ERBITS" of DIAG/ATADIAG's "atrdconf/atwrconf" commands.

   iii) RUEE...."reallocate uncorrectable error enable". Enables auto-reallocation of uncorrectable read errors. This bit is bit-1 of the "CONFLAGS" byte of DIAG/ATADIAG's "atrdconf/atwrconf" commands.

2. If an unrecoverable write error occurs during a hyper-write operation, (where the drive has already accepted the data from the host and posted good status) then the drive will force an auto-reallocation of the sector independent of the mode settings.

B. Write, Correctable-Read, Uncorrectable-Read Errors

1. In the cases of write-reallocation and correctable read-reallocation, the auto-reallocation to an offline replacement is done at the time of the write or read operation that generated the error. The correct data is of course written to the replacement sector.

2. In the case of uncorrectable read-reallocation, the sector is not auto-reallocated at the time of the read error. Instead, a "pending offline" entry is added to the W-List. This allows the host to attempt future reads of the same physical sector in an attempt to recover the data. Upon the next write to the pending defect, the sector will be auto-reallocated to an offline spare using the data from the write command.

C. Verification

1. In all cases described above, before the auto-reallocation is actually done, there is a verification process that is performed to ensure that there is a level of "hardness" to the defect. This prevents spurious auto-reallocations of soft errors, as well as preventing auto-reallocation in cases where the data was written incorrectly (as for example in a 'read long, modify data, write long' sequence of operations).

2. The verification process consists of a sequence of 10 write/verify operations. If any of the 10 operations results in an error, then the reallocation will be performed.

3. For debugging purposes, this verification process is disabled when the drive is placed in superset mode. This allows auto-reallocation to be performed using "read long, modify data, write long" sequences.

V. Locating Defective Sectors

A. Inlines

1. As explained befire, the W-List entry for inline defects only contains the physical location (cylinder and head) of the track containing inlines and the number of inlines, but not the original sector numbers of the defect locations.

2. To obtain the original sector numbers, one may either examine the SelfScan defect list (using UPT2's "rptss" script for example), or by reading the drives P-List (read-physical with pc=-2, ps=25, nb=16).

3. Even knowing the original defective sectors, one cannot read or write these sectors without re-formatting the track (because even read and write physical commands will skip over inlined sectors). Once the track has been re-formatted (using DIAG/ATADIAG's "ftp" command), the sectors may then be accessed using read/write physical commands. Note however that this practice is dangerous because the inlines on the drive will no longer match the inlines specified in the W-List, which can result in errors such as "sector not found".

B. Offlines

1. Pending offline defects contain the defective physical sector location in the "Cylinder","Head","Sector/SPT" fields of the W-List entry. These locations may then be accessed using read/write physical commands.

2. Host-reassigned and Auto-reallocated offline defect entries do not contain the physical defect location, but rather the physical location of the replacement sector. The physical defect location may be found by performing a "clba" (convert lba to chs) superset command on the LBA following the defective LBA.

   For example if the LBA in the offline entry is E73FH, in DIAG/ATADIAG do the following: "lba 0e740, clba". If the result is "C=54, H=1, S=13", then the physical location of the defect is C=54, H=1, S=12. We have moved to the LBA beyond the defective one, determined the CHS of this LBA, then backed-up one sector.

Mechanical

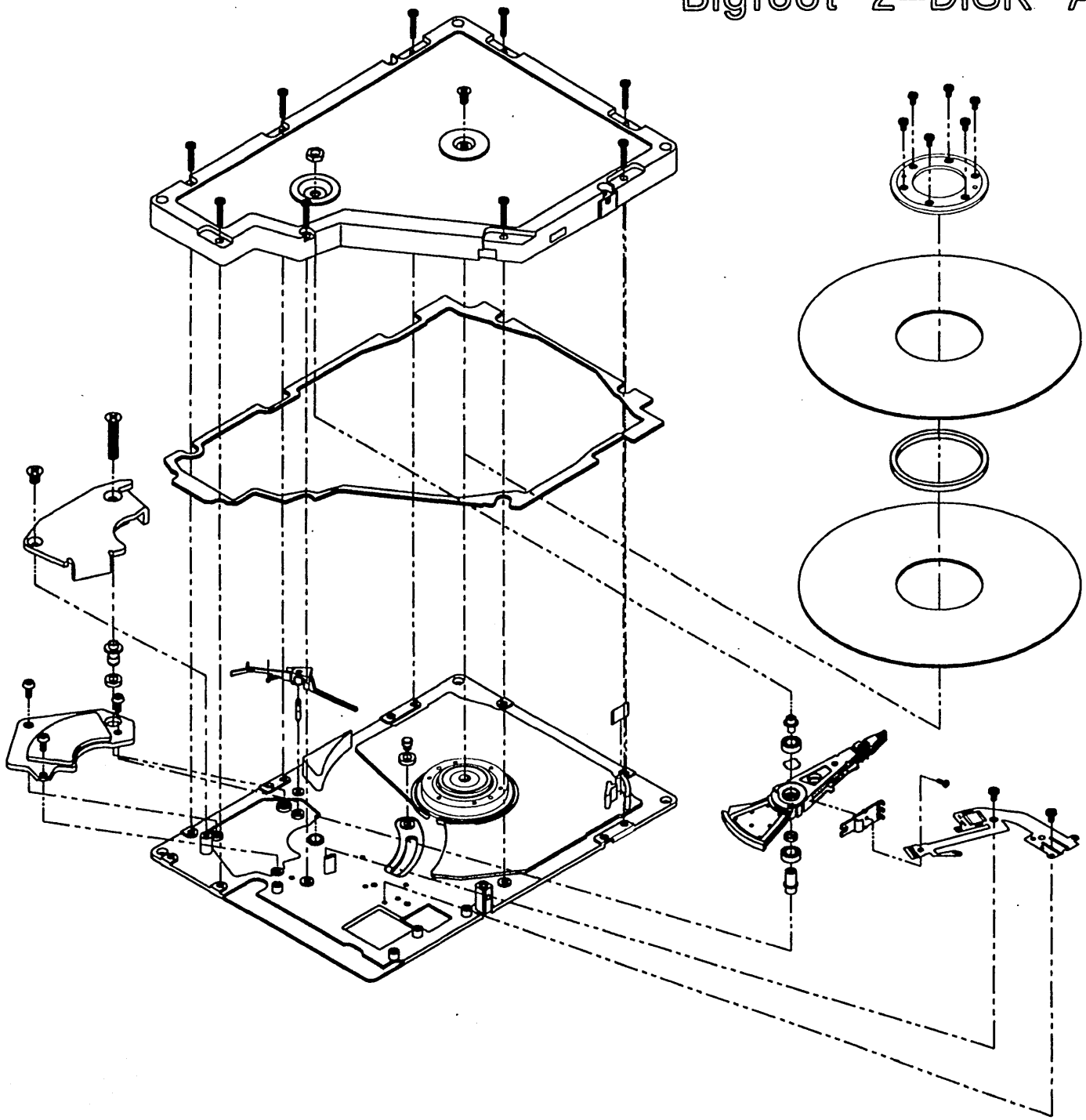
Wallace Chang

BIG FOOT TRAINING CLASS
MECHANICAL SESSION

Agenda

- Drive's Assembly Isoview.
- The Spindle Motor and Disk Clamp.
- The Suspension and Actuator.
- The Airlock.
- Crash Stop Location.
- Shock and Vibration Spec.
- P2 Mechanical Issues.
- Questions and Answers.

Bigfoot 2-DISK ASSEMBLY



■ Spindle Motor

Rotational Speed	3600 rpm± 0.5%	
Starting Torgue	110 gm-cm (min)	
Max RRO_{p-p}	radial	393 μ"
	axial	590 μ"
Max NRROp-p	radial	13.8 μ"
Imbalance	<0.07 gm-cm	
Resonance	230 Hz or higher	

(lower dynamic rocking mode)

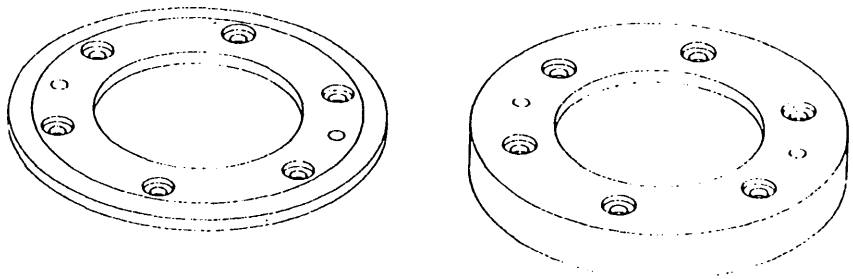
■ Disk Clamp

Number of Screws: 6

Torque in 1.5 kg-cm each.

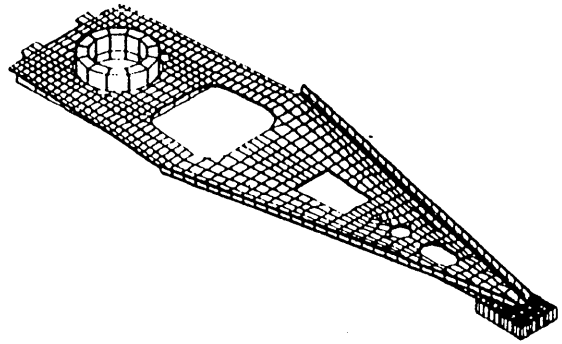
(3 screws per time;will try 6 screws one time)

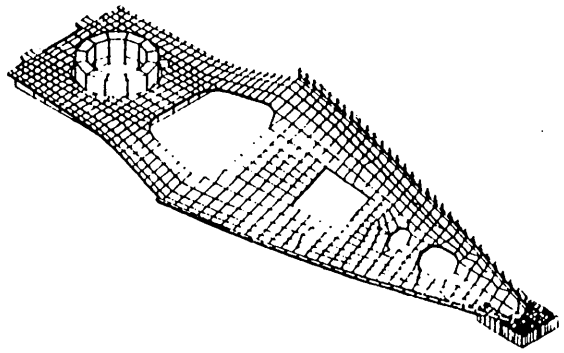
2-disk (stamped) 1-disk (machined)



■ Suspension - Type 850

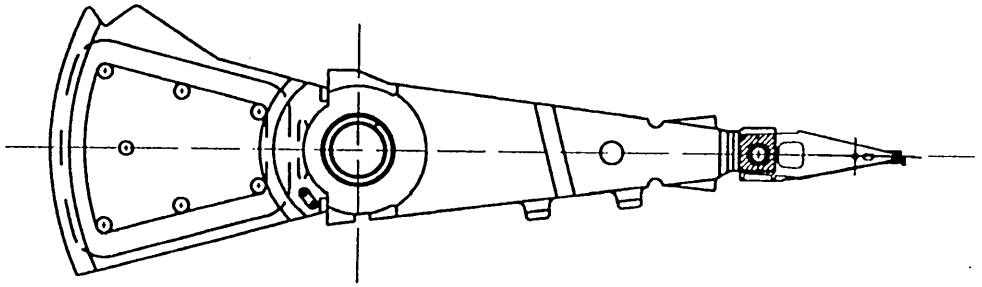
1st torsional mode 2.4Khz

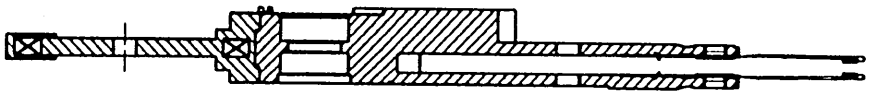


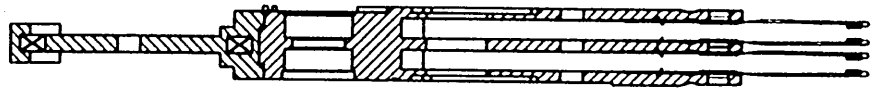


first torsion
2,464 Hz

■ Actuator:

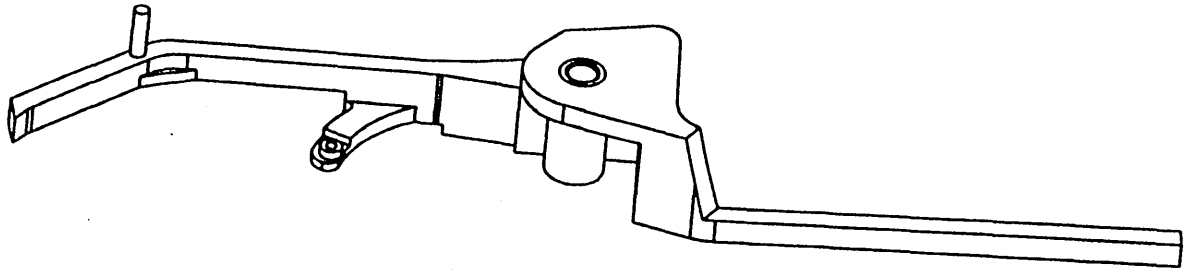




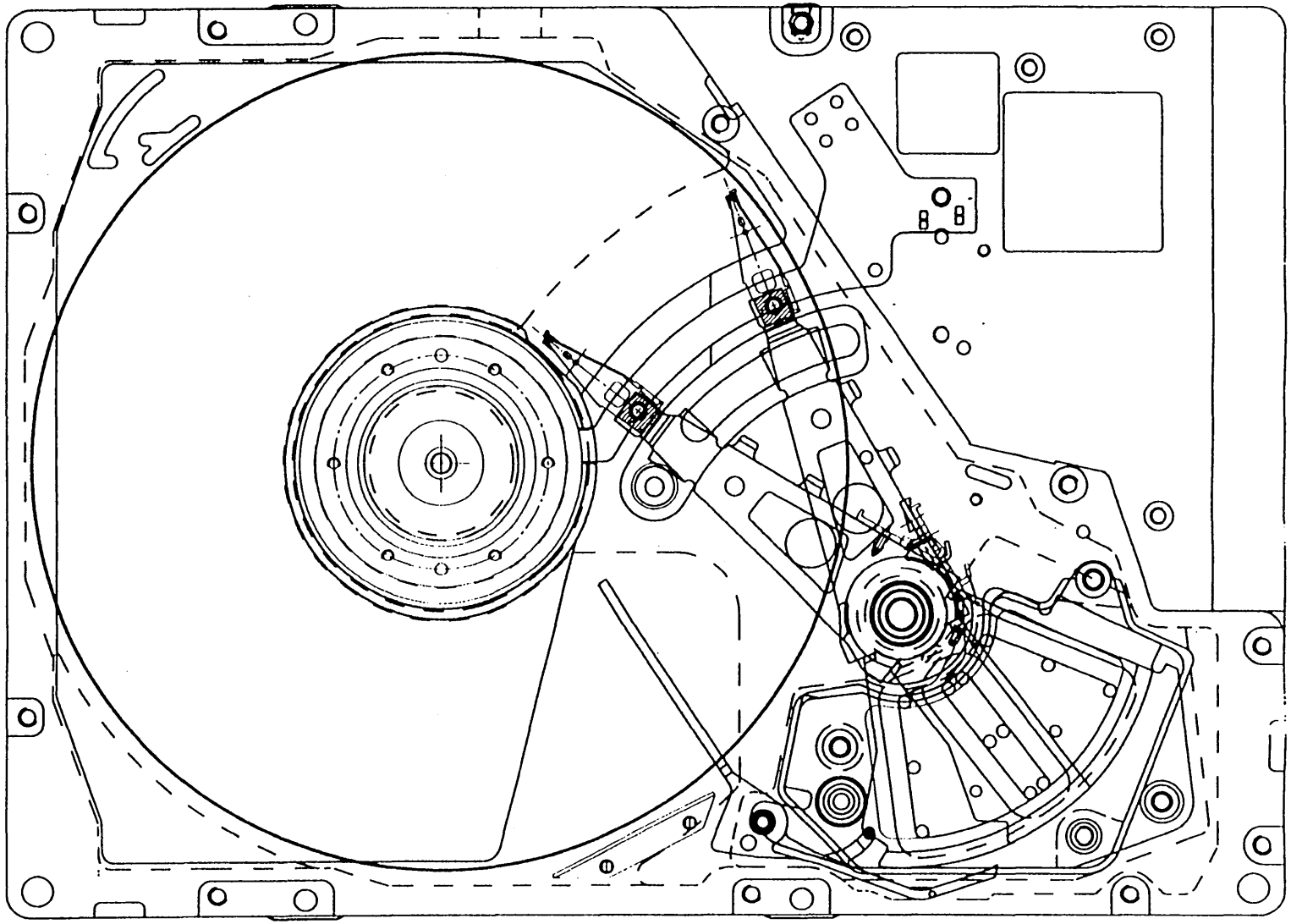


The Airlock

- The Big Foot HDA will use an airlock design similiar to TrailBlazer. A small steel ball is placed on the "Locking Arm" part of the Airlock. The ball is attached to the VCM magnet, hence closing the airlock.
- Since there is no dynamic break after the spindle motor spins down, the windage force will keep the airlock open until the magnetic force steps in. In the worst case, the airlock will open for about 30 seconds after power down.



Crash Stop Location



Shock and Vibration Spec.

■ Operating Shock	10G, 11ms 1/2sine
■ Non-op Shock	70G, 11ms 1/2 sine
■ Operating Vibration	$1G_{p-p}$ 5-500 Hz (X & Y axis) $1G_{p-p}$ 5-200 Hz (Z- axis)
■ Non-op Vibration	$2G_{p-p}$ 5-500 Hz

P2 Mechanical Issues

- Airlock can not open because of the high magnetic force. The fix was to push the magplate a little away from the airlock ball to reduce the attractive force, will redesign the airlock location in PMP.
- Runout (5 or 6 times a round) problem caused by the bad spindle motor. Root causes were the bearing defect frequency was too close to the rocking mode frequency.
- Seeking noise was caused by the loose actuator bearings - process problem.
- New durometer crash stop is still in evaluation. Current crash stops have problems of creating new defects after actuator hitting in the worst case (850 mA).

Quaestions and Answers

PCB / Hardware

Keith Yamada

PCB Design Goals

- Execute existing design (Fireball electronics) in smaller area
- Conform to unique physical dimensions required for low profile 5.25 inch design
- Provide optimum heat dissipation for motor driver IC
- Implement compression connector interface to HDA
- Control Noise interference by separating high speed digital and the R/W sections
- Manufacturing enhancement. No flip in drive assembly process, robotic mount
- Reduce cost

VORTEX Design Leverage

- Fireball Plus head & media specifications
- Same PRML channel as Fireball (Piranha)
- 2nd generation FB ASIC for low cost (Raion)
- Fireball Combo Motor Driver (Hitachi 13545)
- Mirrored versions of Fireball preamps
- Larger DRAM package for low cost

VORTEX Design Features

- K3 microprocessor for cost
  - TrailBlazer / Maverick Servo code base
- Fully automatable low cost pcb design
  - compression connector for R/W & motor (no ZIF's)
  - 0.8mm thick 4 layer pcb
  - Single orientation process
- Improved Self Scan
  - Most comprehensive read channel optimization
  - MSE based channel characterization & debug
- Improved Motor Driver mounting
  - Thermal bosses to improve heat dissipation
- Low noise FPCB
  - Short direct run to compression connector
- ASIC
  - Improved I/O cell for lower noise and improved I/F signals

Raion Vs. Leo

- .50 Micron Technology vs. .72 Micron For Leo
- Raion is based on Leo-A3 Letlist...No circuit changes
- ATA cells changed to handle higher frequency interface activity
- Change delay in FLL circuit to eliminate factory screens on Leo

Technical Overview

- Capacity
  - 1 disk: 1286 MB
  - 2 disk: 2577 MB
- Format Changes from FB+:

	FB635	VORTEX	% Increase
Max FCI	116 KFCI	114 KFCI	-1.7%
Max BPI	109 KBPI	107 KBPI	-1.7%
TPI	4270 TPI	4298 TPI	.66%
Stroke	0.970 in	1.343 in	38.4%
Max Data Rate	83.4 Mb/s	83.9 Mb/s	.6%
Min Data Rate	47.1 Mb/s	44.6 Mb/s	-5.3%
Data Segs between wedges	3	4	
Data Area	7.95 in^2	15.2 in^2	+91%

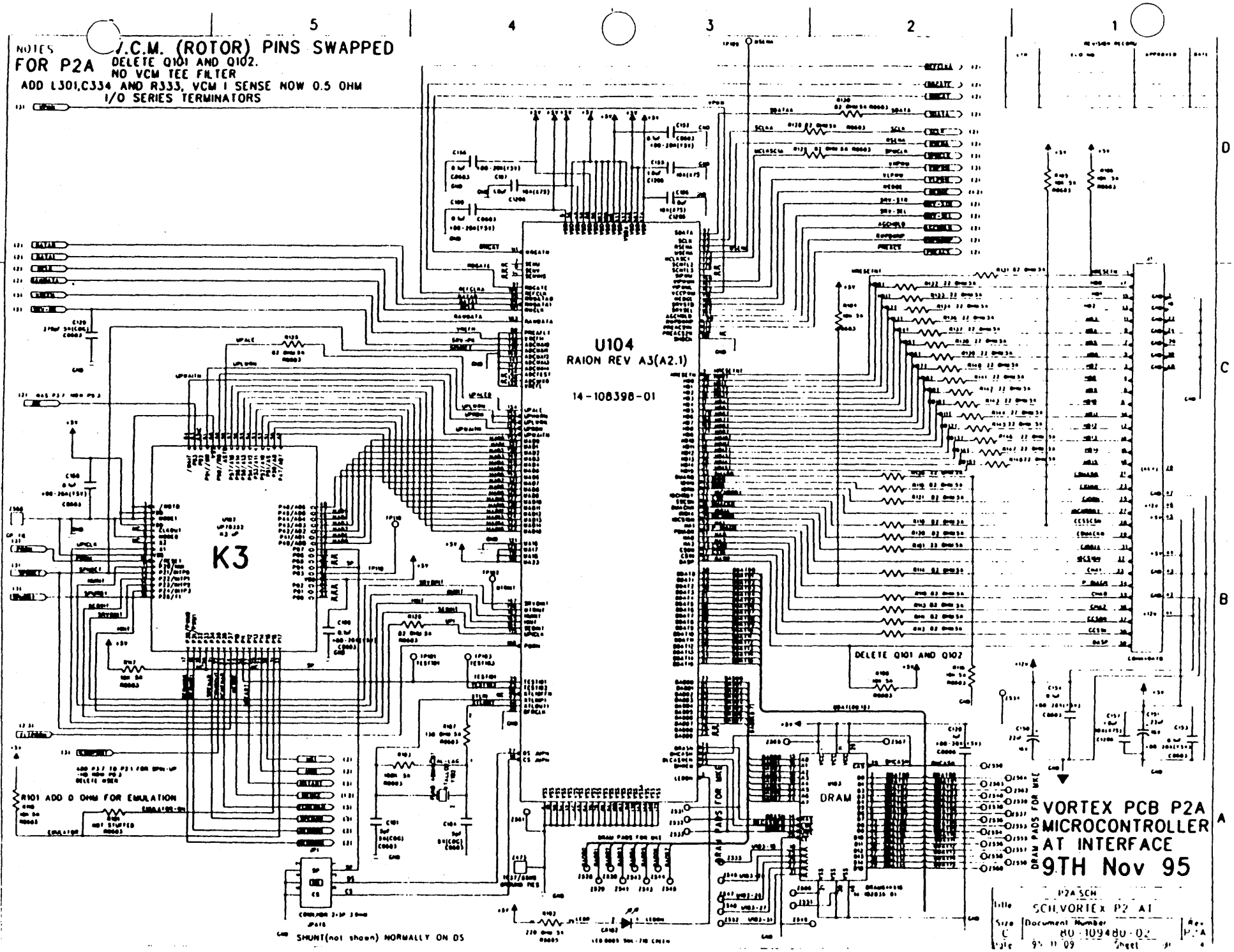
Power Dissipation Vortex Vs. Fireball

1-Disk

Mode	Typical Avg. Power (W) Vortex	Fireball	
Start-up	19.0	19.0	(Peak)
Idle	4.0	3.5	
Read/Write	5.0	5.0	
Read/Write/Seek	6.5	6.0	
Max Seek	8.5	7.5	
Standby	1.0	0.8	
Sleep	1.0	0.8	

2-Disk

Mode	Typical Avg. Power (W) Vortex	Fireball	
Start-up	19.0	19.0	(Peak)
Idle	4.5	4.0	
Read/Write	5.5	5.5	
Read/Write/Seek	7.0	6.5	
Max Seek	9.0	8.0	
Standby	1.0	0.8	
Sleep	1.0	0.8	


NOTES
FOR P2A
V.C.M. (ROTOR) PINS SWAPPED
DELETE Q101 AND Q102.
NO VCM TEE FILTER
ADD L301,C334 AND R333, VCM I SENSE NOW 0.5 OHM
I/O SERIES TERMINATORS
U104
RAION REV A3(A2.1)
14-108398-01
K3
DELETE Q101 AND Q102
R101 ADD 0 OHM FOR EMULATION
SHUNT(not shown) NORMALLY ON DS
DRAM
VORTEX PCB P2A
MICROCONTROLLER
AT INTERFACE
9TH Nov 95
VORTEX PCB MARKED P2A
P2A.SCH
SCH,VORTEX P2 AT
80-109480-02
95 11 09

MARKED P2A

LAYER 4 SILK

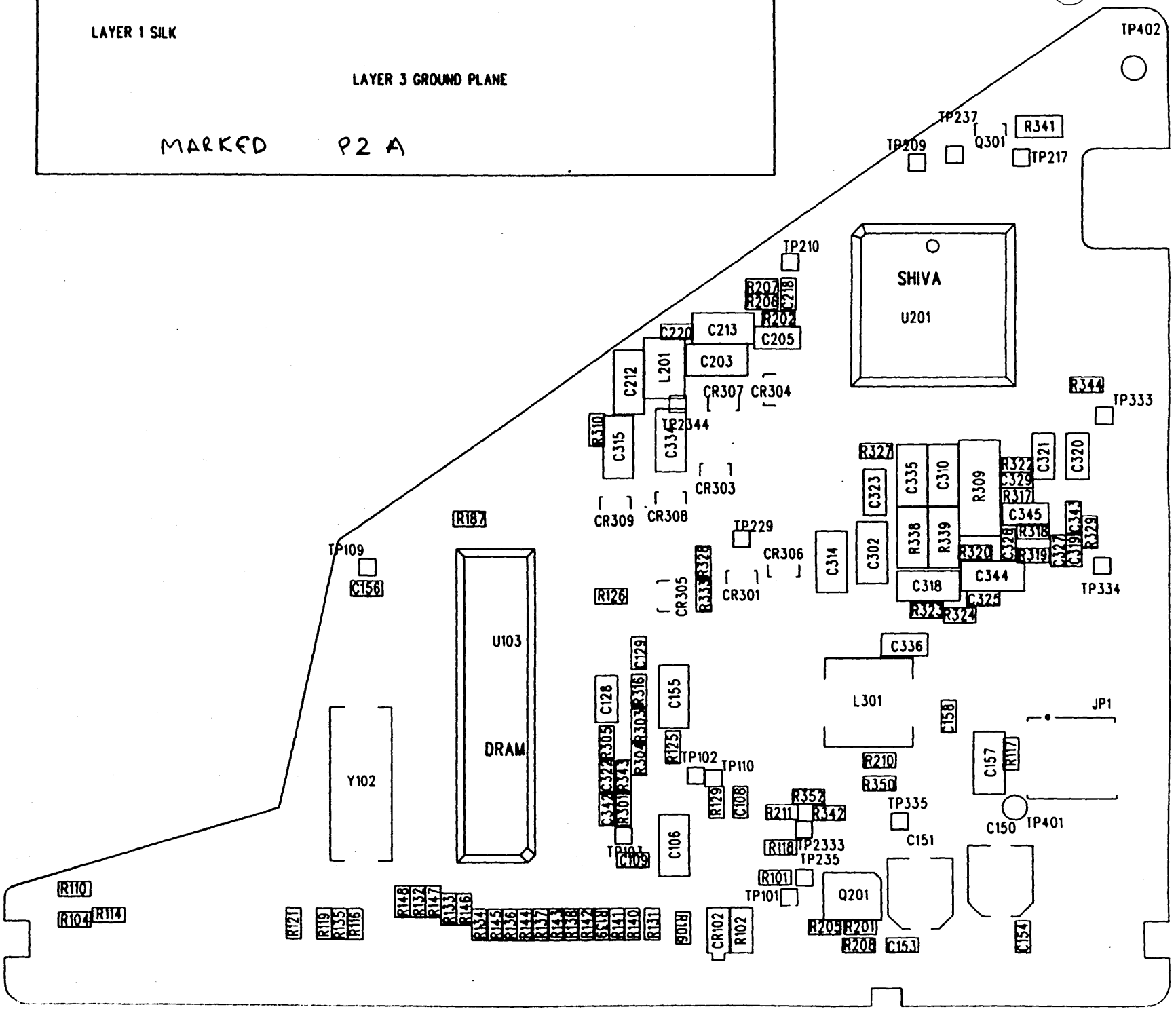
BASE HDA SIDE

VORTEX AT STYLE 11-7-95 K3 KOMBO: SOLID PLANE ARTWORK # 30-109480-02 REV P2 A

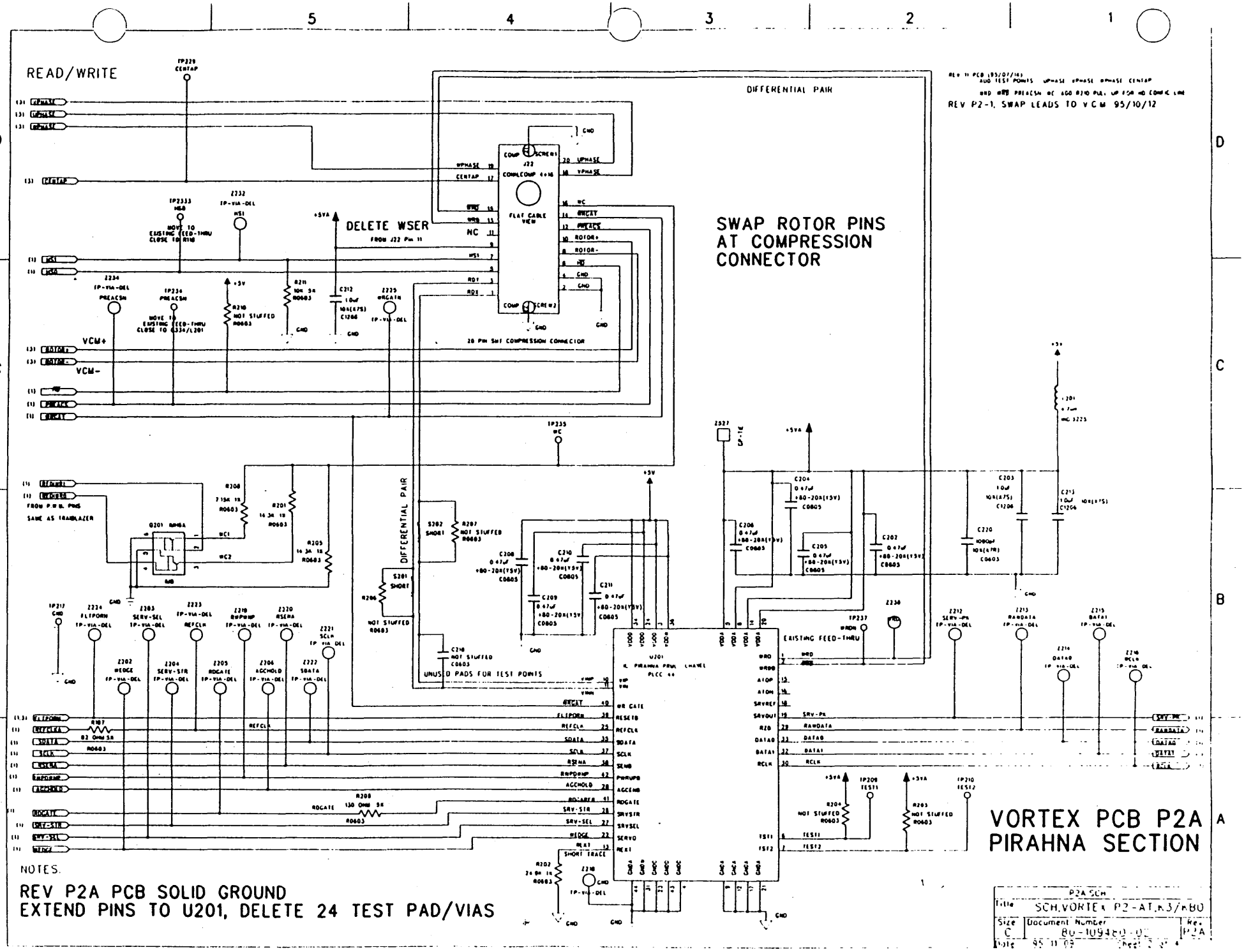
LAYER 1 SILK

LAYER 3 GROUND PLANE

MARKED P2 A

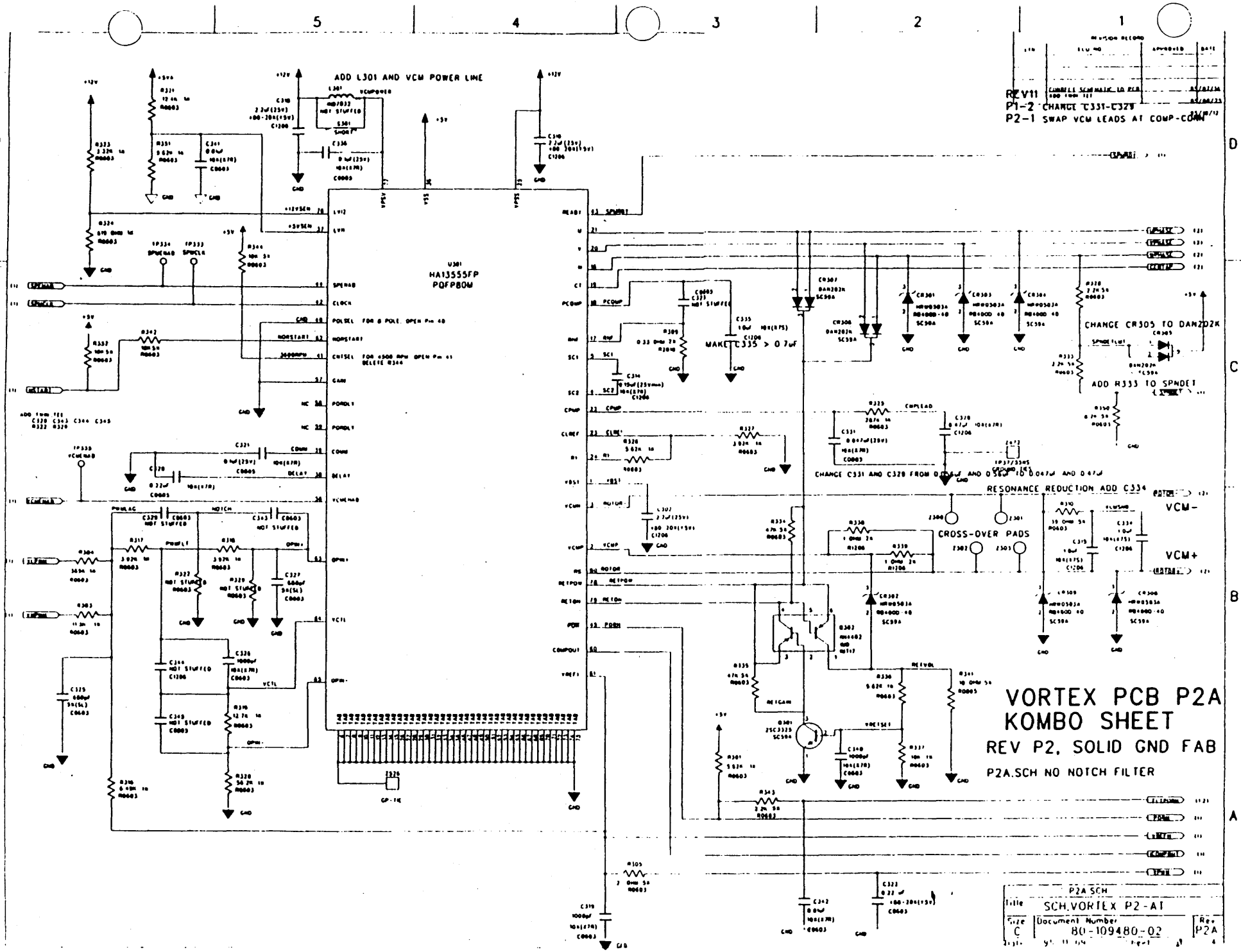


NON-VGA SIDE


READ/WRITE
DIFFERENTIAL PAIR
REV P2-1, SWAP LEADS TO VCM 95/10/12
SWAP ROTOR PINS
AT COMPRESSION
CONNECTOR
DELETE WSER
FROM J22 Pin 11
NC
VCM+
VCM-
20 PIN SMT COMPRESSION CONNECTOR
DIFFERENTIAL PAIR
EXISTING FEED-THRU
UNUSED PADS FOR TEST POINTS
VORTEX PCB P2A
PIRAHNA SECTION
VORTEX PCB MARKED P2A
NOTES.
REV P2A PCB SOLID GROUND
EXTEND PINS TO U201, DELETE 24 TEST PAD/VIAS
P2A SCH
SCH.VORTEX P2-AT.K3/KBO
Size C
Document Number 80-109360-0
Rev P2A
Date 95 11 03

5 4 3 2 1

D C B A


ADD L301 AND VCM POWER LINE
REV11
P1-2 CHANGE C331-C329
P2-1 SWAP VCM LEADS AT COMP-COMP
U301
HA13555FP
PQFP80M
CHANGE CR305 TO DAN202K
ADD R333 TO SPNDET
MAKE C335 > 0.7uF
CHANGE C331 AND C328 FROM 0.047uF AND 0.047uF TO 0.047uF AND 0.47uF
RESONANCE REDUCTION ADD C334
CROSS-OVER PADS
VCM-
VCM+
VORTEX PCB P2A
KOMBO SHEET
REV P2, SOLID GND FAB
P2A.SCH NO NOTCH FILTER
P2A SCH
SCH.VORTEX P2-AT
80-109480-02
P2A
VORTEX PCB MARKED P2A

Heads / Media

Rex Niedermeyer

Vortex/Bigfoot Tech. Review: Head/Media

Presentation Outline

1. Head/Media comparison (Fireball Vs Vortex/Bigfoot)

2. Head/Media vendor comparison

3. Current Head/Media vendor issues

4. Head/Media performance data

Vortex/Bigfoot Tech. Review: Head/Media

Head Comparison

Parameter	Fireball	Fireball 2	Vortex/Bigfoot
Slider size	50%	50%	50%
Air bearing	TPC,NPAB	TPC,NPAB	TPC,NPAB
Pole geometry (um)	4.8	4.8	4.8,4.5
Fly height (u-in.)	2.25	2.25	2.25
Suspension	850	850	850
Gram load	5	5	5
Turns	42	42	42
Max Inductance (uH)	0.8	0.8	0.8
TPI	4200	4270	4298
Max KFCI	100	116	114
Max Aerial Density (Mbit/in^2)	390	460	460
Capacity/disk (Mbytes)	540	640	1280
RPM	5400	5400	3600
Max data rate (Mbits/sec)	83.5	83.4	83.9

Vortex/Bigfoot Tech. Review: Head/Media

Media Comparison

Parameter	Fireball	Fireball 2	Vortex/Bigfoot
Media Mrt (memu/cm^2)	2.2	2.0	**2.0**
Media Coercivity (Oersteds)	1800	1950	**1950**
Media Glide Height (u-in.)	1.5	1.5	**1.5**
Max overcoat [carbon+lube] (u-in.)	0.787	0.787	**0.787**
Disk diameter (mm)	90	90	**130**
Disk thickness (mils)	31	31	**50**
Disk data area/surface (in^2)	7.64	7.93	**15.10**

Vortex/Bigfoot Tech. Review: Head/Media

Head Supplier Comparison

Head Vendor	Air Bearing	Track Trim	Trackwidth (nominal)	Undershoot Supression	Device	Inductance (nominal)
AMC	NPAB	No	4.5 μm	No	42T/4 layer	635 nH
Read-Rite	TPC	Yes	4.8 μm	No	42T/4 layer	590 nH
TDK	TPC	Pseudo	4.8 μm	No	42T/4 layer	750 nH
Yamaha	TPC	Pseudo	4.8 μm	Partial	42T/4 layer	710 nH
RHG	NPAB	No	4.8 μm	No	42T/4 layer	525 nH

- **Both Read-Rite, RHG and Yamaha heads use the same wafers as used in Fireball 2.**
- **The current TDK head selections include both a Fireball 2 type ABS level pole trim (without undershoot suppresion) and a wafer level pole trim variety. We hope to go with the wafer level pole trim head as it is lower cost and has better volume availability than the current ABS trimmed head.**
- **The AMC non-pole trim head is unique to Vortex/Bigfoot and is being considered as a low cost addition to the other head vendors.**

Vortex/Bigfoot Tech. Review: Head/Media

Media Supplier Comparison

Media Vendor	Coercivity (Oersteds)	Mrt (memu/cm^2)	Glide Height (μ")	Comments
Fuji	1950	2.0	1.5	first time with 130 mm
Showa Denko	1950	2.0	1.5	relatively new vendor
Komag/AKCL	1885	2.0	1.5	AKCL new at 130 mm

- **While Fuji media is used on Fireball and Fireball 2 this is the first time Fuji has done 130 mm disks. The media magnetics used on Vortex/Bigfoot are the same as Fireball 2. Fuji is considered one of our primary media vendors.**

- **Showa Denko media does not have as much history on Quantum products as Fuji but has experience producing 130 mm media and is considered vital to the success of Vortex/Bigfoot.**

- **While Fireball 2 is using AKCL media we are currently evaluating 130 mm disks from its sister company Komag (USA) , we expect to see first samples from AKCL at PMP.**

Vortex/Bigfoot Tech. Review: Head/Media

Current Vortex/Bigfoot Head/Media Vendor Issues: Heads

- **AMC Overwrite problems.**
  AMC are continuing to make changes in wafer design of head to address poor overwrite performance seen at P1 and while improved at P2 they are still 2-3 dB poorer than other vendors.

- **P2 TDK wafer level track trim heads have lower performance than at P1.**
  TDK wafer trim heads performance was compromised by higher fly heights and excessive side reading . Are working with vendor to fix.

- **P2 Yamaha heads are using a new ABS design ("step flat") to lower cost. Have also seen some evidence of excessive "popcorn" noise with a few heads.**
  We are waiting for CSS data on this new ABS design to determine acceptability. Have notified vendor concerning the "Barkhousen noise" problem.

- **RHG heads will first be seen at PMP.**
  Historical problems with RHG CSS using NPAB ABS. New texturing of ABS surface expected to help improve CSS performance.

Vortex/Bigfoot Tech. Review: Head/Media

Current Vortex/Bigfoot Head/Media Vendor Issues: Media

- **First samples of AKCL to be seen at PMP.**
  First attempt by AKCL to make 130 mm media (uses Komag process).

- **We will not see first samples from Fuji's actual Vortex/Bigfoot production line till PMP.**
  We are currently working with Fuji to facilitate any qualification tests needed to bring them to full production with minimal delays.

- **Fuji defect counts increased significantly from P1 to P2.**
  Vendor claims problem due to high particle count in clean rooms due to construction of new sputtering line, will be fixed by PMP.

- **Fuji CSS performance was poor at P1.**
  Steps were taken by vendor to improve CSS for P2 but still waiting P2 CSS test results to confirm (initial stiction values are improved).

- **Due to concerns about Showa "dip lube" media having possible worse CSS performance than their "spin lube" variety we will use only "spin lube" media for PMP.**
  If P2 CSS tests look OK for the "dip lube" media, then it will be phased in during MP.

Vortex/Bigfoot Tech. Review: Head/Media

HDA Analog Parametrics for P2 build: ID TAA (mV)

Media Vendor	Head Vendor AMC	Read-Rite	TDK (ABS trim)	TDK (Wafer trim)	Yamaha
Fuji	103.79	103.22*	98.50	100.10	114.03
Showa-D	100.17	108.90*	99.32	94.25*	115.42
Showa-S	100.98	108.23*	98.67	92.50*	111.92
Komag	105.19	105.42*	100.23	101.30	108.25*

* - Used SSI Preamp which may have had slightly lower gain.

HDA Analog Parametrics for P2 build: ID PW50/T

Media Vendor	Head Vendor AMC	Read-Rite	TDK (ABS trim)	TDK (Wafer trim)	Yamaha
Fuji	1.58	1.67*	1.62	1.53	1.70
Showa-D	1.58	1.70*	1.65	1.63*	1.71
Showa-S	1.56	1.62*	1.60	1.61*	1.75
Komag	1.74*	1.71*	1.66 .	1.59	1.78*

* - Used SSI Preamp which may have caused slightly broader PW50's.

Vortex/Bigfoot Tech. Review: Head/Media

HDA Analog Parametrics for P2 build: Overwrite (dB)

Media Vendor	Head Vendor				
	AMC	Read-Rite	TDK (ABS trim)	TDK (Wafer trim)	Yamaha
Fuji	26.38	28.98	30.24	27.60	29.74
Showa-D	27.4	28.28	29.79	27.40	29.50
Showa -S	27.12	31.01	30.92	28.82	29.90
Komag	27.21	29.92	29.65	27.60	29.05

HDA Analog Parametrics for P2 build: NLTS (%)

Media Vendor	Head Vendor				
	AMC	Read-Rite	TDK (ABS trim)	TDK (Wafer trim)	Yamaha
Fuji	12.41	11.16*	12.95	14.68	12.66
Showa-D	11.10	9.97*	13.19	12.38*	11.70
Showa -S	12.24	9.88*	13.56	12.85*	12.83
Komag	13.30	11.98*	13.79	14.40	13.48

* - Used SSI preamp which displayed somewhat lower NLTS than other preamp vendors.

Vortex/Bigfoot Tech. Review: Head/Media

P2 Performance Data (Average MSE[1])

Media Vendor	Head Vendor AMC	Read-Rite	TDK (ABS trim)	TDK (Wafer trim)	Yamaha
Fuji	104	97	111	111	89
Showa -S	95	90	108	104	90
Showa-D	103	91	110	104	89
Komag	106	97	114	109	95

1 - MSE = Mean Squared Error - number read from detector and proportional to random error rate.

Parametric specifications limits based on P2 build*

Parametric Parameter	Spinstand spec limits
MF TAA (ID)	> 230uV
PW50 (ID/MD)	< 44.7 nSec/24.8 nSec
Overwrite (MF/(MF/6))	< -25 dB
NLTS	< -13 dB (20%)

* - Determined by correlation analysis with MSE data

Read / Write

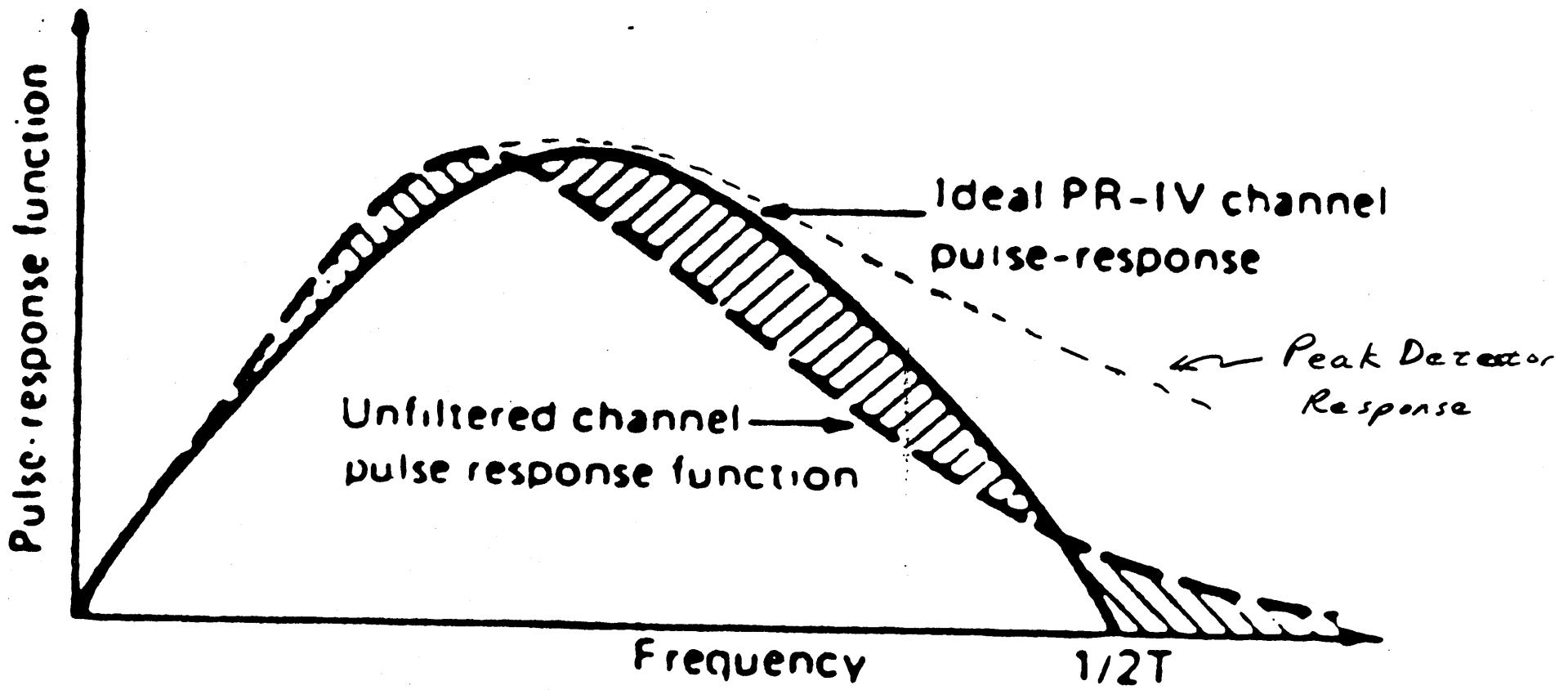
Tehri Lee

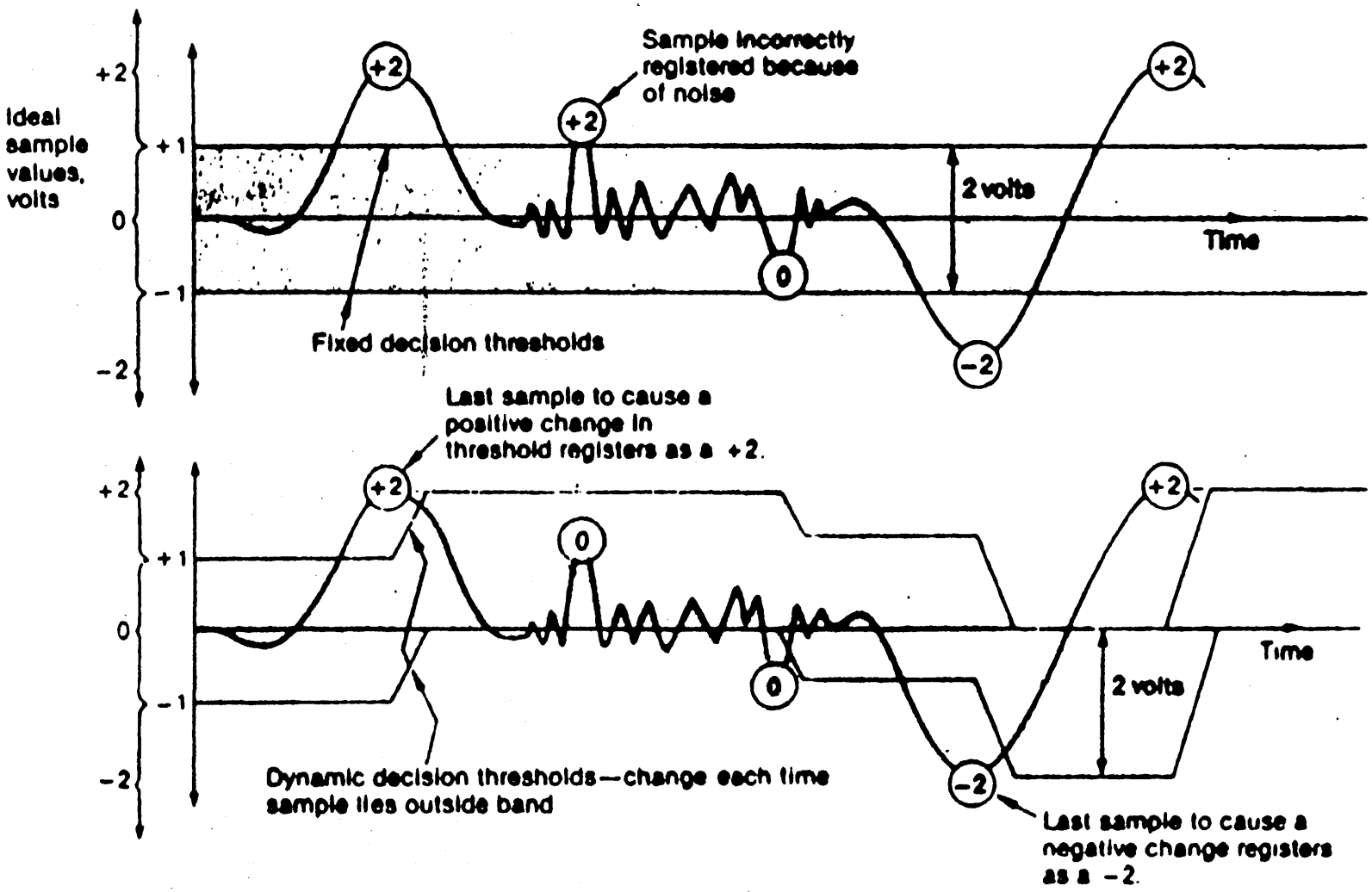
VORTEX 1286 MBytes

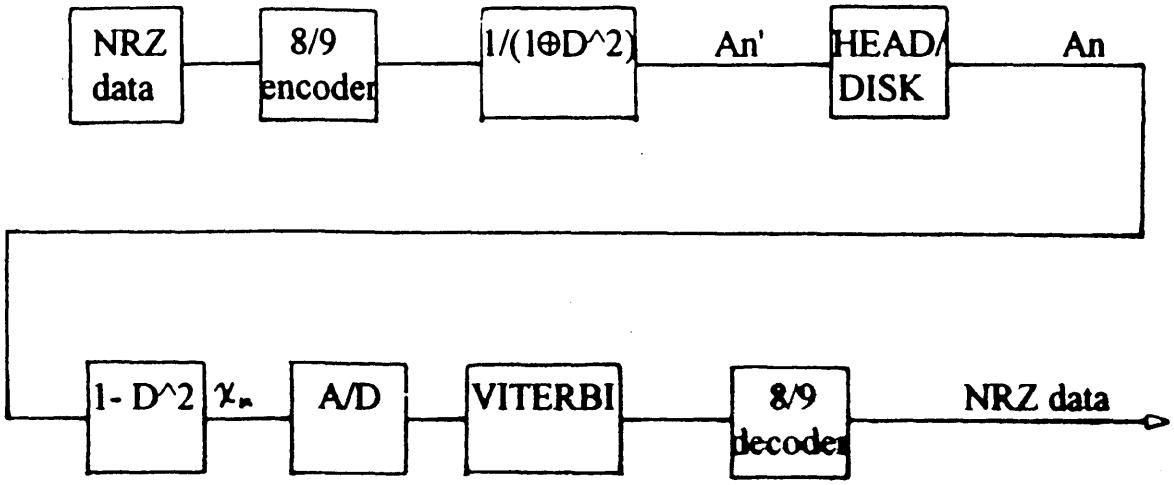
16/17, PRML, SHIVA, 16zones

Last Rev:	6/23/1995	9:44	Pad	0.675	uSec	Srv Fq	40	MHz	Total	1286.37	MBytes
Req Cap	1286	MBytes	Extra	0	Bytes	Srv Clk	25	nSec		100.02	%
Spare	1	per cyl				Srv N	490	Clocks			
	1	trk/zone	ID Pre	16	Bytes	Nservos	96	samples			
	in	mm	ID AM	3		Tservo	12.25	uSec			
Rod	2.4740	62.8400	ID Data	7		Tdata	161.361	uSec			
Rid	1.1311	28.7300	ID CRC	3							
Stroke	1.3429	34.1100	ID Pad	8		Srv OH	07.06	%			
						Fmt OH	14.48	%			
Trk Den	4298		DSg Pre	16	Bytes						
			DSq AM	3		Rcd Den	460.847	Mb/in2			
RPM	3600	rpm	DSg Pad	10		Cap / Sur	643.183	MB/surface			
Trot	16666.7	uSec	Dag ECC	20							

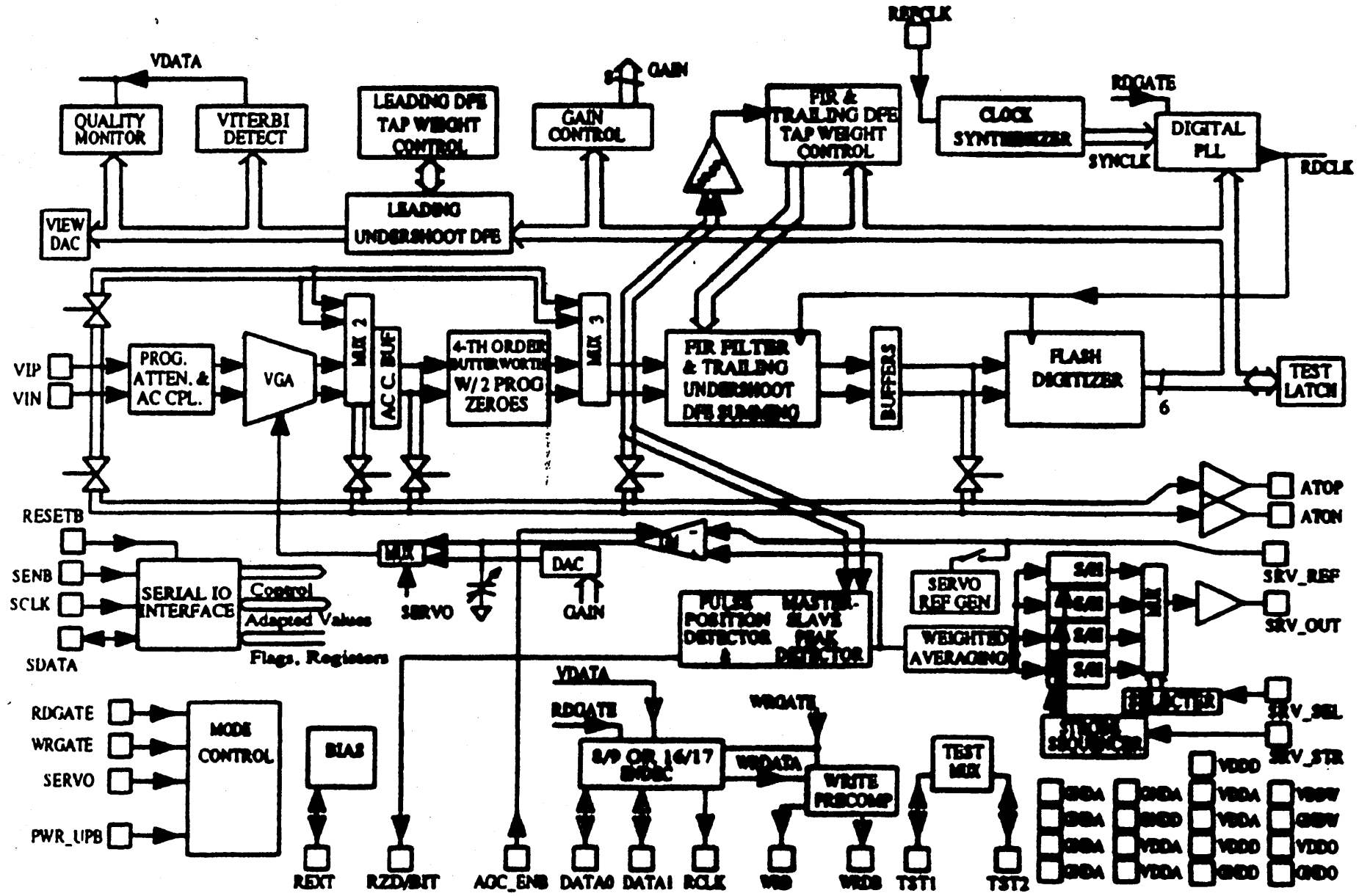
Zone	Router	Rinner	N trks	Last Trk	Nsect	BPI	FCI	Fsynth (MHz)	Fmax (MHz)	Window (nsec)	Synth M	Synth N	Bytes /wedge
OD	2.4740												
System	2.4739	2.4685	24		192	61,895	65,763	61.33	30.67	16.30	92	15	1159
1	2.4683	2.3794	383	382	276	93,555	99,402	89.17	44.58	11.21	107	12	1685
2	2.3792	2.2903	383	765	276	97,195	103,270	89.17	44.58	11.21	107	12	1685
3	2.2901	2.2012	383	1148	270	98,739	104,910	87.06	43.53	11.49	148	17	1645
4	2.2010	2.1121	383	1531	261	99,815	106,053	84.44	42.22	11.84	152	18	1596
5	2.1119	2.0230	383	1914	253	100,873	107,177	81.74	40.87	12.23	188	23	1545
6	2.0228	1.9339	383	2297	243	101,662	108,016	78.75	39.38	12.70	126	16	1488
7	1.9337	1.8448	383	2680	233	102,018	108,394	75.38	37.69	13.27	98	13	1425
8	1.8446	1.7557	383	3063	224	102,925	109,357	72.38	36.19	13.82	152	21	1368
9	1.7554	1.6668	382	3445	212	103,694	110,175	69.23	34.62	14.44	90	13	1308
10	1.6666	1.5779	382	3827	202	104,561	111,096	66.09	33.04	15.13	152	23	1249
11	1.5777	1.4890	382	4209	192	102,832	109,259	61.33	30.67	16.30	92	15	1159
12	1.4888	1.4002	382	4591	180	105,284	111,864	59.05	29.52	16.94	124	21	1116
13	1.3999	1.3113	382	4973	169	106,393	113,043	55.88	27.94	17.89	95	17	1056
14	1.3111	1.2224	382	5355	160	107,221	113,922	52.50	26.25	19.05	105	20	992
15	1.2222	1.1335	382	5737	144	104,325	110,846	47.37	23.68	21.11	90	19	895
Diag	1.1333	1.1312	10										


Pulse-response function
Ideal PR-IV channel
pulse-response
Peak Detector
Response
Unfiltered channel
pulse response function
Frequency
1/2T

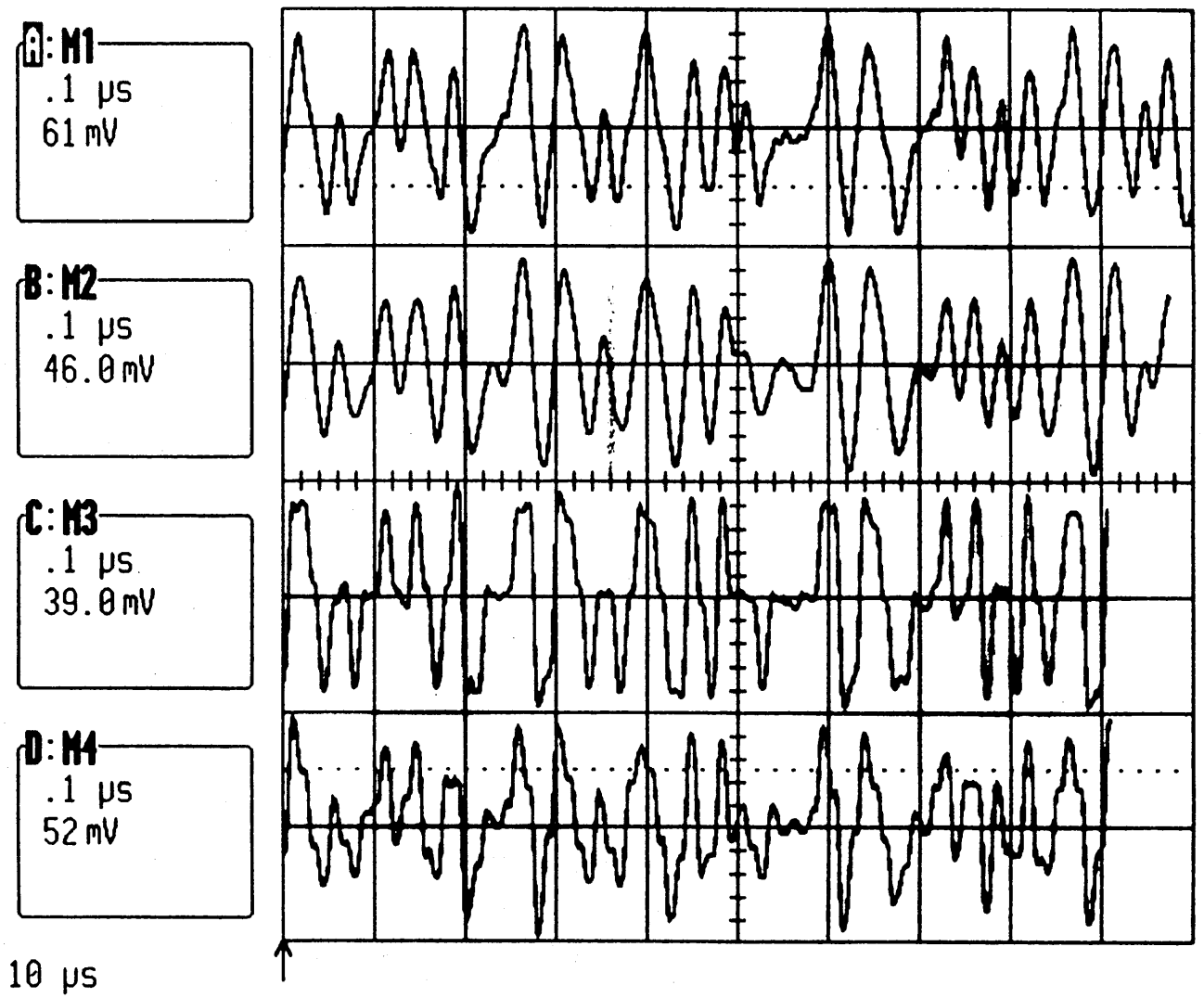

Ideal sample values, volts
+2
+1
0
−1
−2
+2
+2
Sample incorrectly registered because of noise
0
−2
2 volts
Time
Fixed decision thresholds
Last sample to cause a positive change in threshold registers as a +2.
+2
+1
0
−1
−2
+2
0
0
−2
2 volts
Time
Dynamic decision thresholds—change each time sample lies outside band
Last sample to cause a negative change registers as a −2.



8/9	1	0	1	0	0	1	1	0	1	0	0	0	1	1
1/(1⊕d^2)	0	0	1	0	1	1	0	1	1	1	1	1	0	0
An' (Iw)	-1	-1	+1	-1	+1	+1	-1	+1	+1	+1	+1	+1	-1	-1
χ_n = An (1-d^2)			+2	0	0	+2	-2	0	+2	0	0	0	-2	-2
8/9			1	0	0	1	1	0	1	0	0	0	1	1



ATT91C040 (SHIVA) BLOCK DIAGRAM - Figure 1



Preamp o/p

CTF o/p

FIR o/p (locked)

FIR o/p (Not locked)

Head	Zone	Cyl.	Wdge	ERRTE	GAIN	ATT/VGA	FREQ	TAP RANGE
0	1	382	96	90	5 .7	2/149	128	11/247
0	2	765	96	99	5 .6	2/147	128	14/249
0	3	1148	96	99	5 .8	2/151	127	31/219
0	4	1531	96	103	5 .7	2/150	127	47/215
0	5	1914	96	90	5 .8	2/151	128	31/225
0	6	2297	96	95	5 .8	2/151	127	60/190
0	7	2680	96	93	6 .1	2/155	127	49/195
0	8	3063	96	100	6 .6	2/162	128	70/191
0	9	3445	96	94	6 .7	2/164	127	54/206
0	10	3827	96	98	7 .0	2/168	127	70/189
0	11	4209	96	96	7 .4	2/174	128	58/198
0	12	4591	96	97	7 .9	2/179	128	75/178
0	13	4973	96	96	8 .7	1/145	128	76/186
0	14	5355	96	97	9 .5	1/153	127	72/186
0	15	5737	96	92	10 .3	1/160	127	58/211
		AVERAGE		96	7 .0			

Head	Zone	Cyl.	Wdge	ERRTE	GAIN	ATT/VGA	FREQ	TAP RANGE
1	1	382	96	98	6 .2	2/156	128	41/208
1	2	765	96	105	6 .0	2/153	128	61/197
1	3	1148	96	120	6 .4	2/159	128	69/199
1	4	1531	96	112	6 .4	2/159	127	68/184
1	5	1914	96	122	6 .6	2/162	128	87/189
1	6	2297	96	107	6 .6	2/162	128	64/185
1	7	2680	96	109	6 .5	2/160	128	55/194
1	8	3063	96	107	7 .1	2/169	128	73/174
1	9	3445	96	108	7 .2	2/170	127	52/204
1	10	3827	96	111	7 .4	2/173	127	78/173
1	11	4209	96	106	7 .8	1/134	128	58/202
1	12	4591	96	122	8 .6	1/144	127	84/164
1	13	4973	96	116	9 .6	1/154	127	72/188
1	14	5355	96	116	10 .1	1/159	127	73/183
1	15	5737	96	111	10 .4	1/161	128	80/164
		AVERAGE		111	7 .5			

Head	Zone	Cyl.	Wdge	ERRTE	GAIN	ATT/VGA	FREQ	TAP RANGE
2	1	382	96	72	5 .0	2/136	128	18/234
2	2	765	96	79	4 .7	2/130	127	60/178
2	3	1148	94	90	4 .7	2/131	127	26/223
2	4	1531	96	90	5 .2	2/140	127	38/208
2	5	1914	96	92	5 .3	2/141	127	22/236
2	6	2297	96	99	5 .5	2/146	127	55/205
2	7	2680	96	92	6 .0	2/154	127	38/216
2	8	3063	96	97	6 .0	2/154	128	52/187
2	9	3445	96	108	6 .7	2/163	127	68/191
2	10	3827	96	103	7 .6	2/176	127	12/231
2	11	4209	96	99	7 .4	2/173	127	67/182
2	12	4591	96	113	7 .6	2/176	127	66/190
2	13	4973	96	116	8 .9	1/147	128	72/185
2	14	5355	96	118	9 .8	1/156	127	83/179
2	15	5737	96	116	10 .9	1/166	127	46/216
		AVERAGE		99	6 .8			

VORTEX MACRO DESCRIPTION (By Tehri S. Lee, 1/5/96)

Majority of the following macro commands require *.vtx batch files. To ensure that they work, it is recommended that all *.vtx batch files be loaded into the directory where DIAG is located.

	WWW	Writes between all wedges in wedge to wedge format.
	SWW	Adapts the read channel by reading wedge-to-wedge and stores VGA, ERRTE, FREQ, and DCTAP values in the buffer at the end of each wedge read.
	CWC	Controls the write current.
-	RDSV	Reads Shiva register address in r0 and returns the register value in r0.
-	WRSV	Writes the value in r63 into Shiva register address in r3.
	ERS	Erases between the wedges of current track.
-	SVC	Enables controlling the entire Shiva parameters, selectively. The circuit block to be controlled can be selected from Main menu.
-	SVR	Reads the entire Shiva registers and breaks them down by each individual parameter values. Lists all register values at the end. Also, stores all register values in a file as well as generating an output file containing what was displayed.
-	SVW	Writes all register values contained in the file generated by SVR into Shiva.
-	SVA	Displays all adapted values on the fly as read operation is performed.
-	SVD	Displays all Shiva parameter description. The circuit block of interest can be selected from the Main menu.
-	RPAR	Reads all Shiva parameters in Config page 10 and 17 and generates output files by each parameter.
	WPAR	Loads all Shiva parameters into Config page 10 and 17 from the file generated from RPAR.
-	RCONF10	Reads all zone dependent Shiva parameters (not head dependent and not optimized) and displays as well as generating an output file.
	WCONF10	Loads all zone dependent Shiva parameters into respective Config pages from the output file generated by RCONF10.
	RDCTAP	Reads all DCTAP values from Config page 17 and displays by zone and head.
	WDCTAP	Loads all DCTAP values into Config page 17 from the file generated by RDCTAP.
	RTAP1 - 10	Reads TAPW values from Config page 17 and displays by zone and head.
	WTAP1 - 10	Loads TAPW values into Config page 17 from the file generated by RTAP.
	RTDFE1 - 5	Reads TDFE values from Config page 17 and displays by zone and head.
	WTDFE1 - 5	Loads TDFE values into Config page 17 from the file generated by RTDFE.
	RLDFE1 - 4	Reads LDFE values from Config page 17 and displays by zone and head.
	WLDFE1 - 4	Loads LDFE values into Config page 17 from the file generated by RLDFE.
	RTDLY	Reads TDFEDLY values from Config page 17 and displays by zone and head.
	WTDLY	Loads TDFEDLY values into Config page 17 from the file generated by RTDLY.
	RLDLY	Reads LDFEDLY values from Config page 17 and displays by zone and head.
	WLDLY	Loads LDFEDLY values into Config page 17 from the file generated by RLDLY.
	RPFR	Reads FRNGR & CTFFR values from Config page 17 and displays by zone and head.
	WPFR	Loads FRNGR & CTFFR values into Config page 17 from the file generated by RPFR.

RZFR	Reads ZFCR & ZFR values from Config page 17 and displays by zone and head.
WZFR	Loads ZFCR & ZFR values into Config page 17 from the file generated by RZFR.
RVGA	Reads ATT & VGA values from Config page 17 and displays by zone and head.
WVGA	Loads ATT & VGA values into Config page 17 from the file generated by RVGA.
RCMP	Reads LATE values from Config page 17 and displays by zone and head.
WCMP	Loads LATE values into Config page 17 from the file generated by RCMP.
RMIS	Reads ACC, GUG, TWUG, FUG, PHUG, FAST_ACQ values from Config page 17 and displays by zone.
WMIS	Reads ACC, GUG, TWUG, FUG, PHUG, FAST_ACQ values into Config page 17 from the file generated by RMIS.
OPBW	Optimizes bandwidth of CTF.
OPBST	Optimizes boost of CTF.
OPT4	Optimizes TAPW4.
OPTDLY	Finds trailing undershoot location.
OPLDLY	Finds leading undershoot location.
OPCMP	Optimizes write precompensation.
OPWC	Optimizes write current.
OPALL	Optimizes all optimized parameters.
TST	Tests channel performance by measuring MSE (ERRTE).
LZF	Lists M1, N1, Fsyn, and 127 bit time by zone.
FZON	Finds current zone number, no. of blocks, and bytes per wedge.
PSOFF	Turns off power saving mode.
PSON	Turns on power saving mode.
SCRON	Turns on the SCRAMBLER.
SCROFF	Turns off the SCRAMBLER.
NRZON	Turns off the SCRAMBLER, ENDEC, PRECODER to enable the writing of NRZ data.
NRZOFF	Undo NRZON.
ISOP	Writes isolated pulses between all wedges.
1T	Writes 1T pattern between all wedges.
2T	Writes 2T pattern between all wedges.
3T	Writes 3T pattern between all wedges.
4T	Writes 4T pattern between all wedges.
5T	Writes 5T pattern between all wedges.
8T	Writes 8T pattern between all wedges.
16T	Writes 16T pattern between all wedges.
RND	Writes random pattern between all wedges.
WWT	Writes 1t, 2t, or 4t pattern between selected wedges.
WWP	Writes 1byte repeating pattern between selected wedges in wedge-to-wedge format.
RWP	Reads one selected wedge to wedge data written by WWP into buffer.
ECC0	Turns off all ECC and Retries.

ECCS	Sets ECC to single burst and Retries to 0.
ECCD	Sets ECC to double burst and Retries to 0.
ECCD1	Sets ECC to double burst and Retries to 1.
ECCF	Turns on all ECC and Retries.
FORMAT	Formats all or selected head and tracks.
TIO	Controls test MUX 1&2 in RAION.
ERRP	Performs error rate test in physical mode.
ERRL	Performs error rate test in logical mode.
FNLTS	Loads NLTS measurement pattern into buffer (for auto-correlation method).
WNLTS	Writes NLTS measurement pattern between wedges.
~~CWCD~~	~~Controls write current~~
SVFY	Servo-verifies all or selected heads and tracks.

VGA> ATT 2 ACC 2 GUG 3 AGCCOMP 1 VGA 124 VGA_FLG 0
CTF(61)> CTFFR 22 ZHPR 1 ZFCR 0 ZFR 26 CTFQSR 1 TUNE 9
(5)> CTFFS 26 ZHPS 1 ZFCS 1 ZFS 10 CTFQSS 0
F(N)> TAP_FLG 0 TWUG 3 TW4SGN 0 TDFE_OFF 0 DCTAP 108 RSVDB 0
TAPW1 116 TAPW2 175 TAPW4 150 TAPW5 71 TAPW6 136 TWA_DLY 1
TAPW7 88 TAPW8 121 TAPW9 141 TAPW10 111 DCTAP 108 TWA_ROT 1
T(L DFE)> TDFE_OFF 0 TDFENU 0 TDFEDLY 3 EMLDFE 1 LDFENU 1
TDFEW1 149 TDFEW2 129 TDFEW3 133 TDFEW4 134 TDFEW5 135
LDFEW1 32 LDFEW2 44 LDFEW3 46 LDFEW4 47 LDFEDLY 11
DPLL> FUG 3 PHUG 3 FAST_ACQ 0 PLLFFLG 0 FREQ 127
PABJE 0 FADRE 0 PA 0
ENDEC> SCR_BY 0 PRE_BY 0 COD_BY 0 SEL89 0
SM_BY 0 RSVDA 1 RSVDB 1
[illegible]> EENEND 0 TOGGLE 1 PECLM 1 MRDACT 1
PECLPDN 0 SERIAL 0 MRGATEHI 0 MRG_EX 1
[illegible]> MP_EN 1 LATE 0
SYNTH> N1 106 N1 23 VCO_S 1 LFR 3 LFI 2
SERVO> NIBBIT 1 PHL_EZY 0 AQUAL 9 POSONLY 0
S_REF_IN 0 SGFRNDAC 0 CAGCS 31 SLOW_PD 0
THERMRST 1 WATAU 3 TIMER 0 DROOP 1 S_PWR_ON 0
MISC> RCLKDS 1 RESET 0 S_IDLE 0 SLEEP 0 SYNTHPWR 1
RDGATEHI 1 RCLKREF 0 VD_BY 0 RCLK_C 3 POSTRZD 0
[illegible]> PHASEN 0 GMEASS 0 RSVDC 0 GMSLCE 0 GMRESET 1
ANALOG 1 ADSD2 0 ER_FLA 0 ERRTE 76

[illegible] TEST> TWAI 0 TWAG 5
HIGH FREQ TEST MODE> TESTM 0 IENTST 0 EENTST 0
LOW FREQ DC TEST> DCTST 0 ENDCTST 0
MISC TEST MODE> ENDAC 0 EENEND 0 TMCE 0 TPLE 0 TTBE 0
FACTORY TEST> TLCNTL 0 RFOFF 2 SZON 5 RZON 4 SFOFF 2
TLCNTHI 3 TRIMT 0 YH 0 Y 0 E 0 X 0
TS 0 ID 34 DTEST 34

REGISTER VALUES

r0h-106(6ah) r1h-116(74h) r2h-175(afh) r3h-150(96h) r4h-71(47h)
r5h-136(88h) r6h-88(58h) r7h-121(79h) r8h-141(8dh) r9h-111(6fh)
rah-[illegible] rbh-129(81h) rch-133(85h) rdh-134(86h) reh-135(87h)
rfh-128(7ch) r10h-106(6ah) r11h-23(17h) r12h-230(e6h) r13h-22(16h)
r14h-154(9ah) r15h-98(62h) r16h-3(3h) r17h-90(5ah) r18h-42(2ah)
r19h-77(4dh) r1ah-5(5h) r1bh-0(0h) r1ch-172(ach) r1dh-191(bfh)
r1eh-241(f1h) r1fh-9(9h) r20h-136(88h) r21h-64(40h) r22h-195(c3h)
r23h-127(7fh) r24h-15(fh) r25h-76(4ch) r26h-160(a0h) r27h-224(e0h)
r28h-7(7h) r29h-97(61h) r2ah-130(82h) r2bh-0(0h) r2ch-0(0h)
r2dh-0(0h) r2eh-34(22h) r2fh-[illegible](2h) r30h-96(60h) r31h-32(20h)
r32h-44(2ch) r33h-46(2eh) r34h-47(2fh) r35h-179(b3h) r36h-48(30h)
r37h-34(22h)

Servo

Oliver Northrup

Vortex Servo System

• TPI	4298
• Track Pitch	233 uin
• Total Cyl	5738
• RPM	3600
• Number Samples	96
• Servo Sample Rate	5760 Hz
• Servo Sample Period	173.6 us
• Open Loop Bandwidth	360 Hz

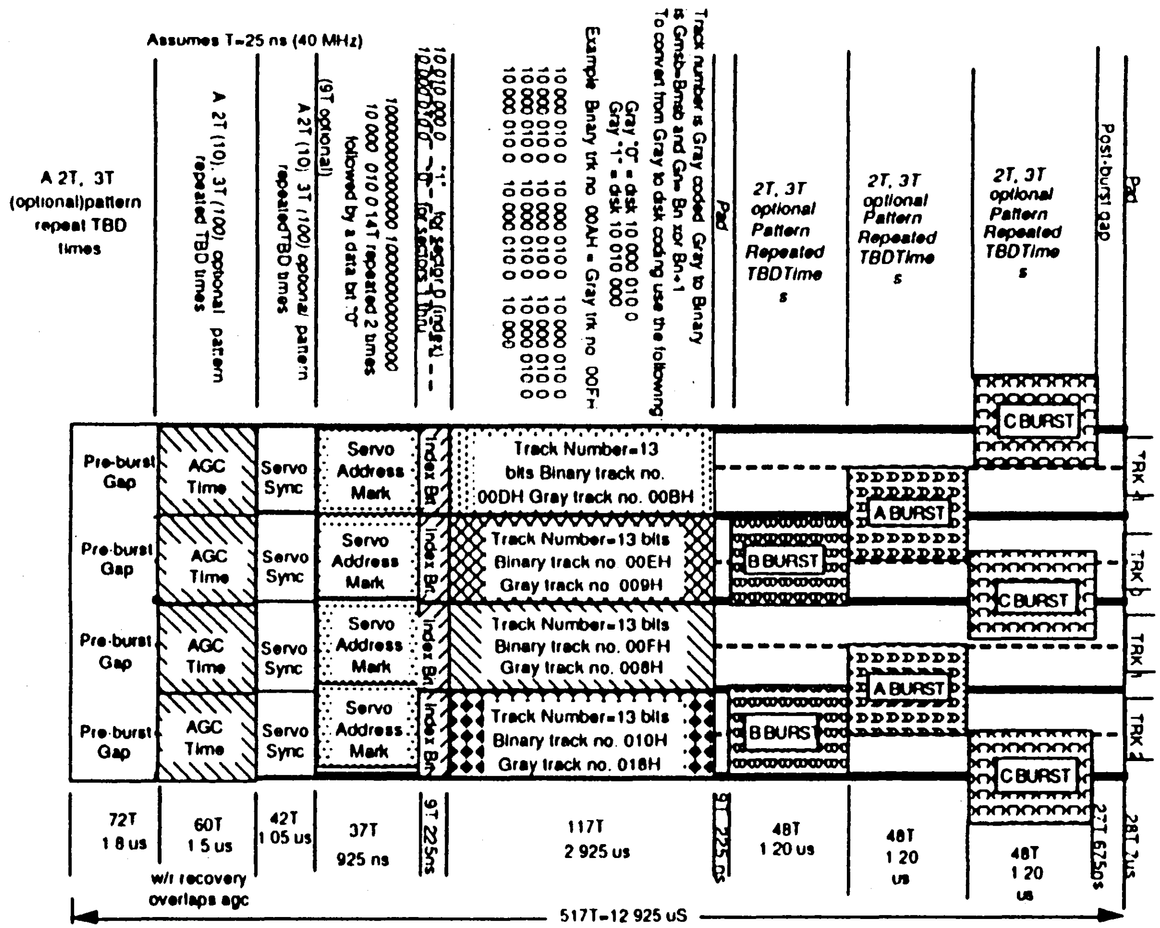
Vortex Servo--Firmware

- Trailblazer Firmware
- Modifications to support 5760 Hz sample rate
- Config Page 18 for servo related parameters
- Config Page 21 added for Self Scan measured parameters--like Fireball
- Recal Record to reduce time to ready
- Servo Defect Map--No more erased C-bursts
  Only bumps are mapped (> 8.5% during SS)

Vortex Servo--Wedge Format

- 40 MHz TNA clock
- T=25 ns
- 2T SYNC, AGC and bursts
- 14T SAM
- 13 Bit Track ID

Vortex Servo--Wedge Format



O. Northrup

1/8/96

Vortex Servo--Seek Modes

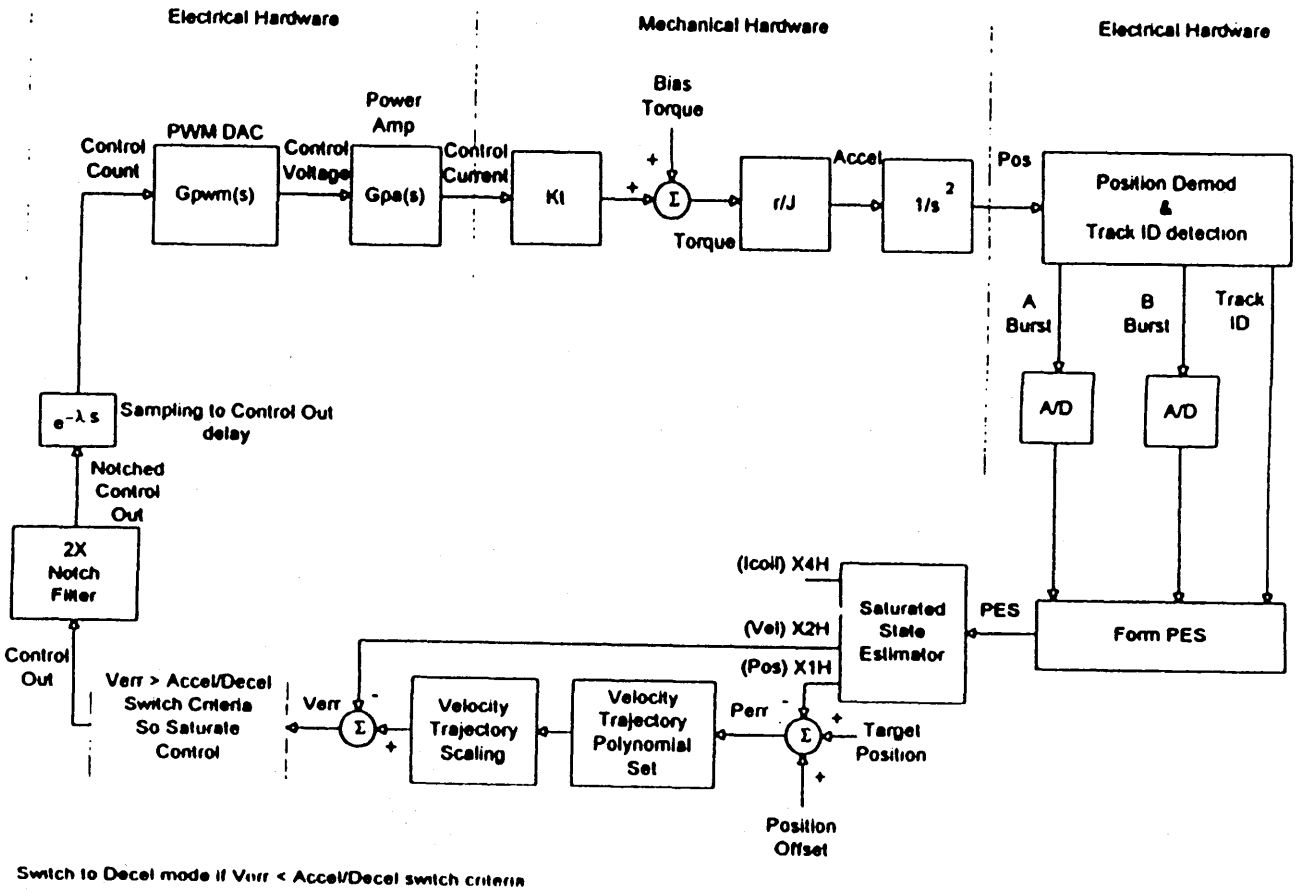
- Long Seeks: Seek Length > 90 tracks
  Nonlinear velocity trajectory
  Feedforward During Decel
- Short Seeks: 50 < Seek Length < 90
  Linear velocity trajectory/No Feedforward
- Settle Seeks: Seek Length < 50 tracks

Vortex Servo--Seek

- Position, Velocity and VCM Current state estimator during acceleration mode
- Position and Velocity state estimator during deceleration mode
- NULLI used for bias cancellation
- Switch to AB Settle mode when velocity and position are within specified criteria

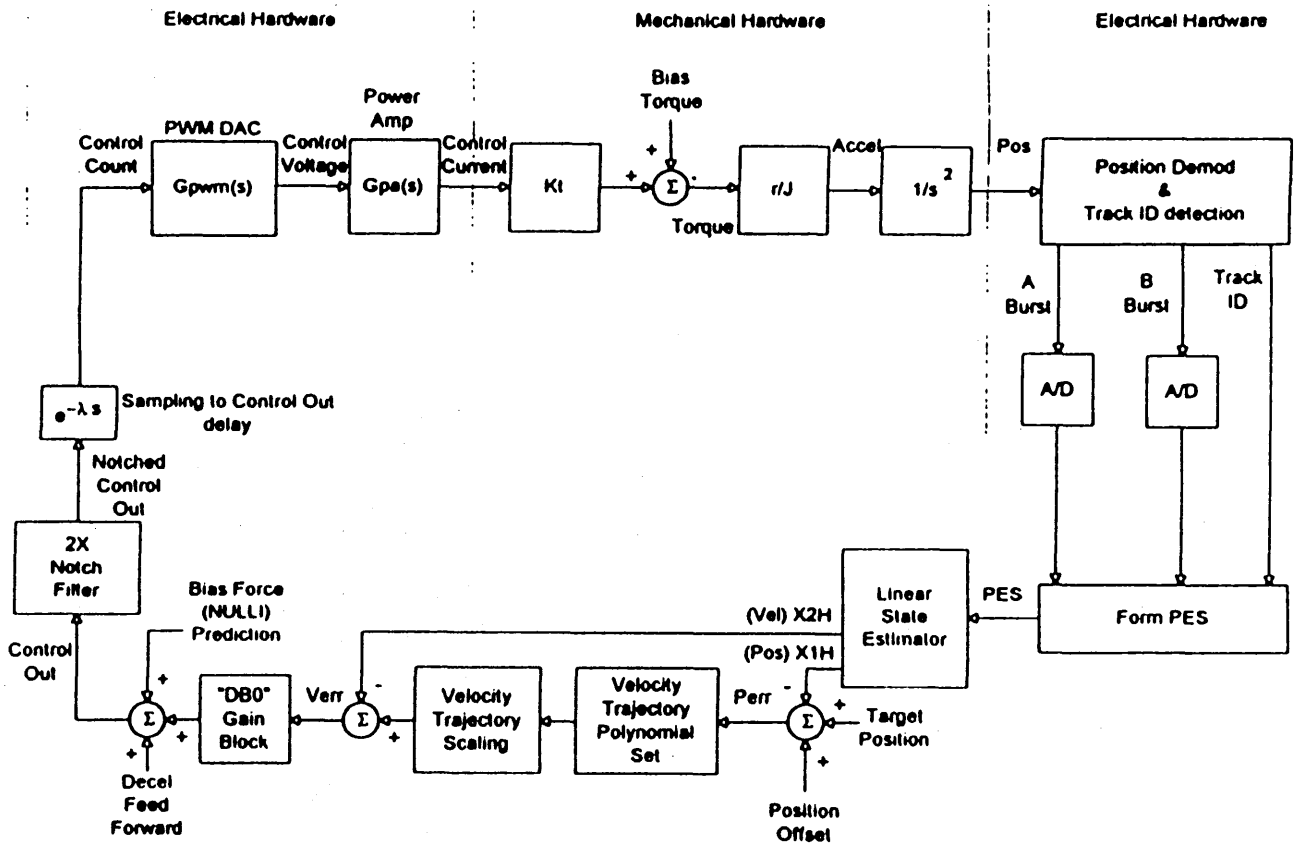
Vortex Servo System

"Long" Seek Mode - Acceleration Phase



Vortex Servo System

"Long" Seek Mode - Deceleration Phase



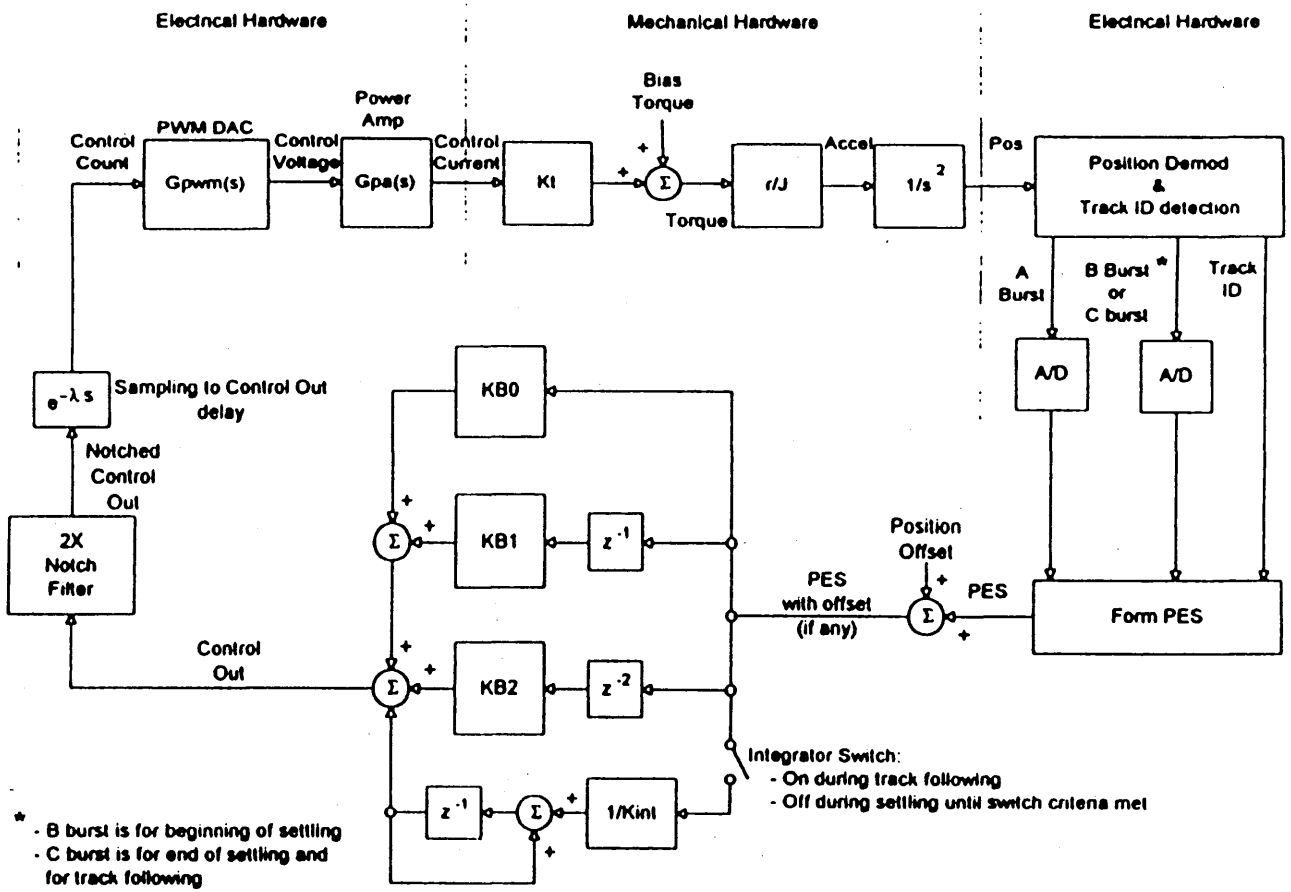
Switch to Linear Range mode if Perr < Decel/LinearRange switch criteria

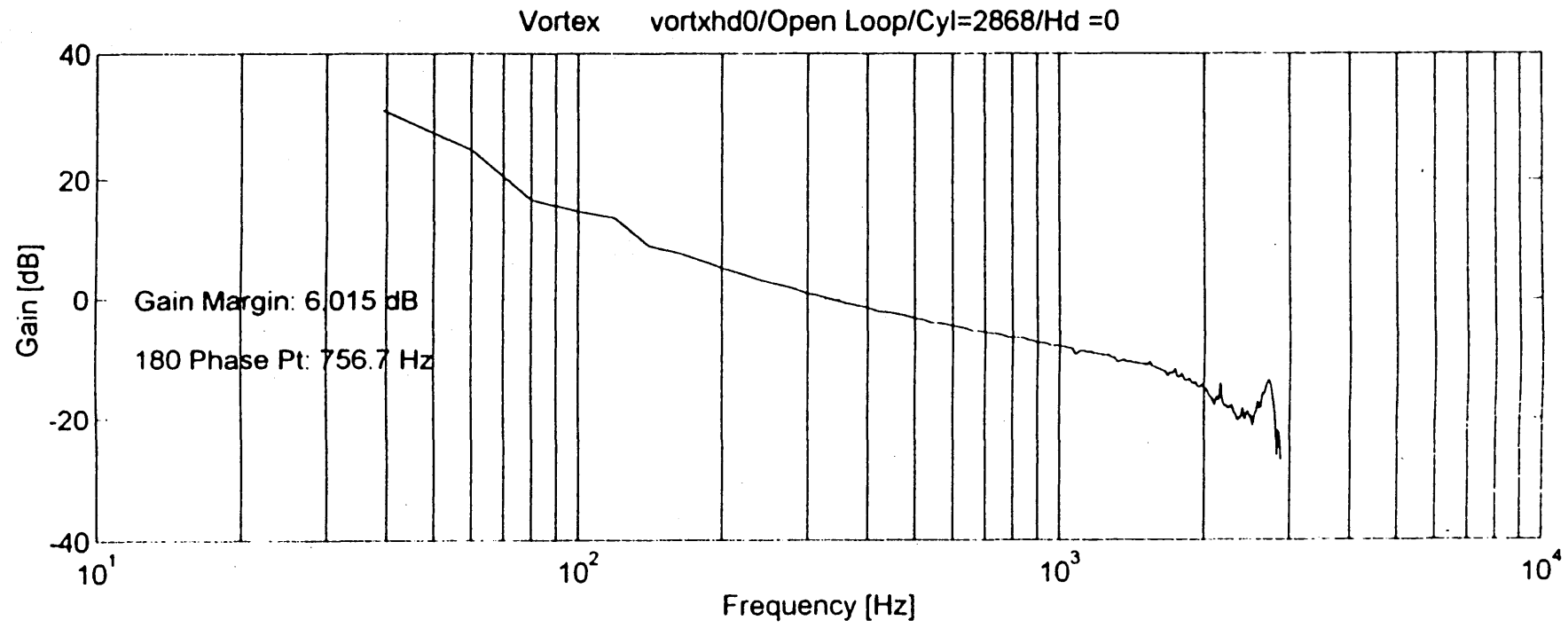
Vortex Servo--On Track

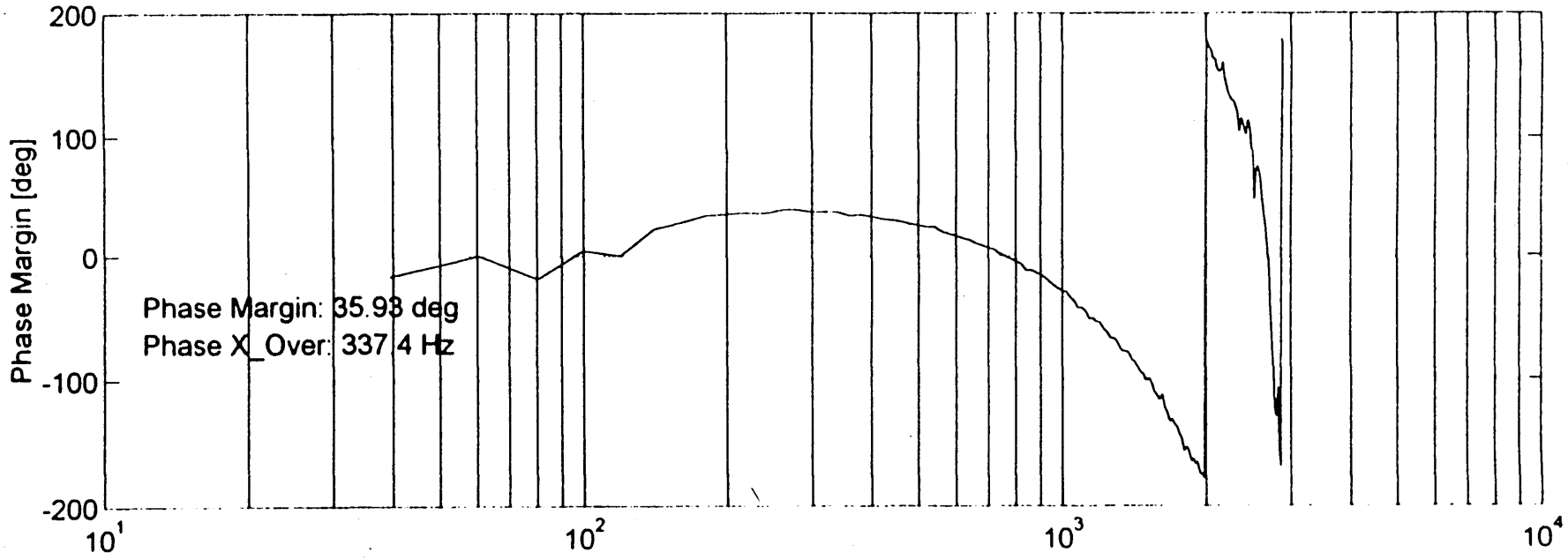
- FIR (Finite Impulse Response) filter with integrator
- AB_SETTLE, AC_SETTLE and ONTRACK modes all use FIR filter
- 360 Hz Open Loop Bandwidth set during Self Scan ==> CP 21 KLOOP
- Servo ISR: ~85 us (49%)

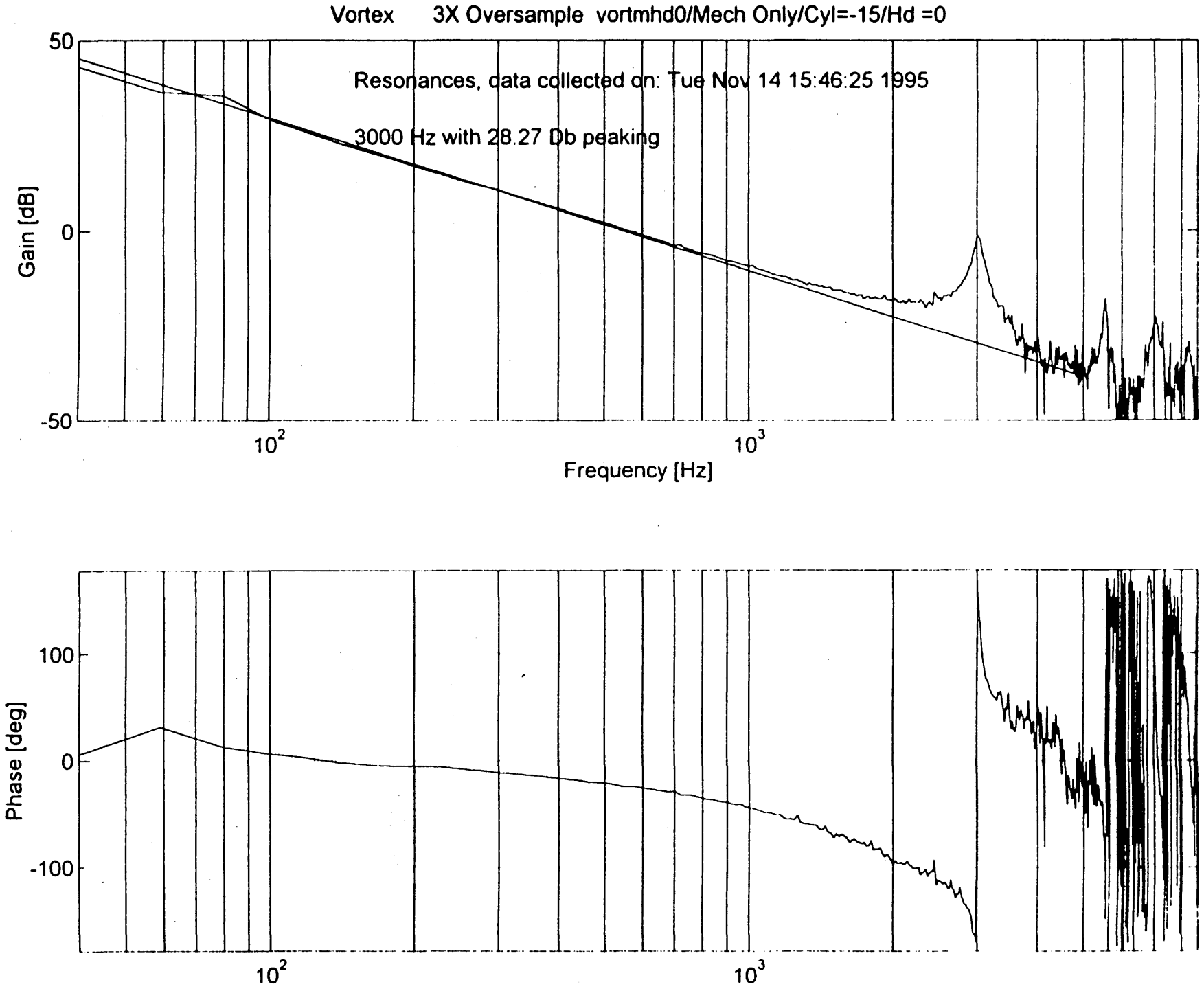
Vortex Servo System

Track Follow & Settle Modes



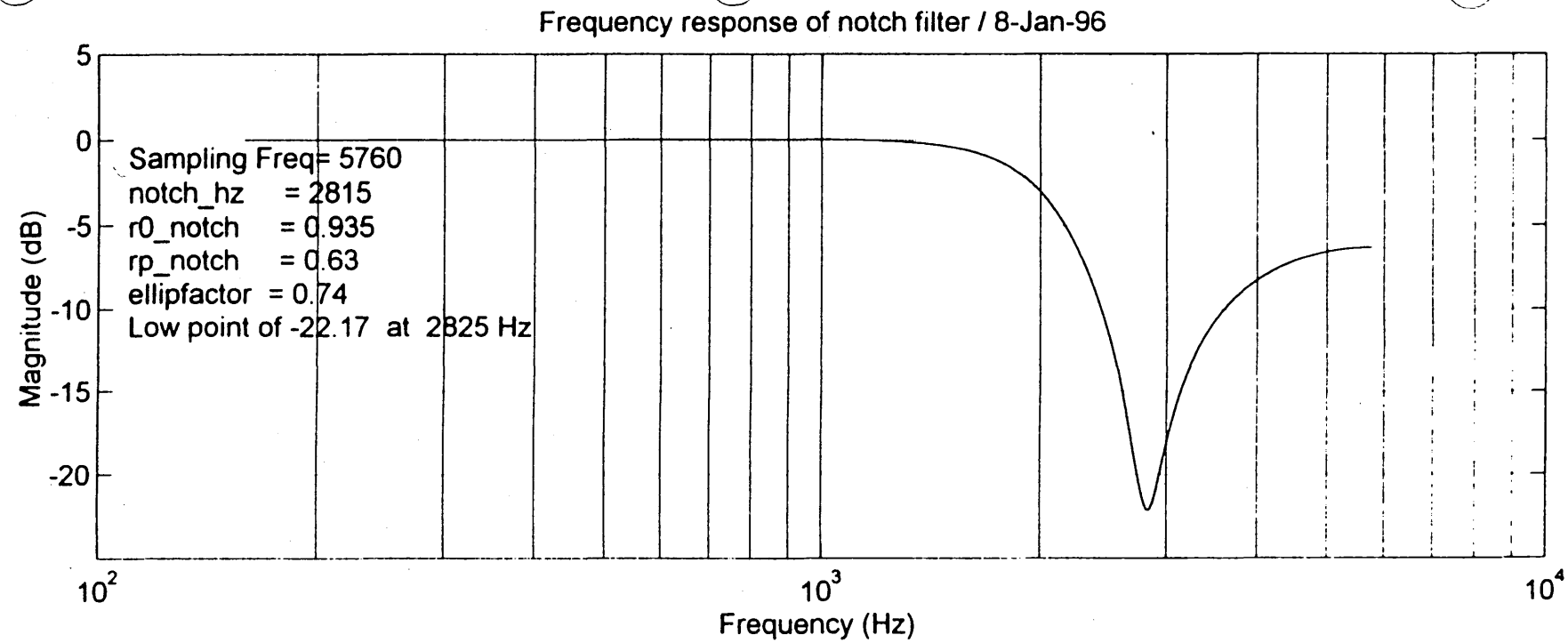

Vortex vortxhd0/Open Loop/Cyl=2868/Hd =0
Gain [dB]
40
20
0
-20
-40
Gain Margin: 6.015 dB
180 Phase Pt: 756.7 Hz
10^1
10^2
10^3
10^4
Frequency [Hz]

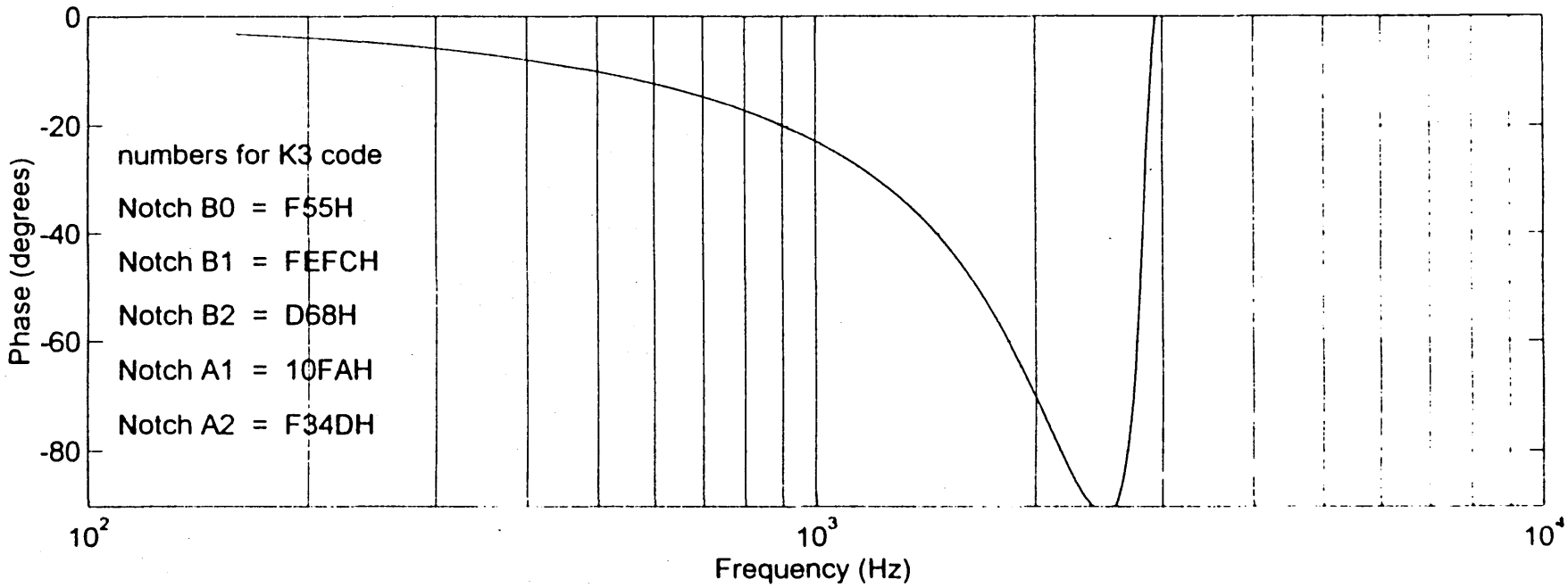

Phase Margin [deg]
200
100
0
-100
-200
Phase Margin: 35.93 deg
Phase X_Over: 337.4 Hz
10^1
10^2
10^3
10^4


Vortex 3X Oversample vortmhd0/Mech Only/Cyl=-15/Hd =0
Resonances, data collected on: Tue Nov 14 15:46:25 1995
3000 Hz with 28.27 Db peaking
Gain [dB]
50
0
-50
10^2
10^3
Frequency [Hz]
Phase [deg]
100
0
-100
10^2
10^3

Vortex Servo--Notch Filter

- Single notch design for Seek & Servo
- 2X oversample (11520 Hz)
- 2815 Hz center frequency
- -22 dB peak attenuation


Frequency response of notch filter / 8-Jan-96
Sampling Freq= 5760
notch_hz = 2815
r0_notch = 0.935
rp_notch = 0.63
ellipfactor = 0.74
Low point of -22.17 at 2825 Hz
Magnitude (dB)
5
0
-5
-10
-15
-20
10^2
10^3
10^4
Frequency (Hz)


numbers for K3 code
Notch B0 = F55H
Notch B1 = FEFCH
Notch B2 = D68H
Notch A1 = 10FAH
Notch A2 = F34DH
Phase (degrees)
0
-20
-40
-60
-80
10^2
10^3
10^4
Frequency (Hz)

Vortex Servo--Error Detection

Error Type	Stop Write	Stop Read
Bump	1	2
SAM	2	2
SYNC	2	2
SPEED	1	1
Track ID	2	2

Vortex Servo--Config Page 21

- CP 21==>Self Scan calibrated variables
- Measured at 16 points over stroke
- Measured Parameters:
  -KLOOP
  -AEQBH/AEQBL switch points
  -AB_SLP
  -AC_SLP
- CP 21 saved results are used after initial kickout if CP 21 is valid

Vortex Servo--Recal Record

- NULLI & V_SCALE servo parameters are saved to disk to improve time to ready
- If RECAL RECORD is enabled, these parameters are not calibrated at recal
- NULLI offset and V_SCALE are updated adaptively during normal drive operation

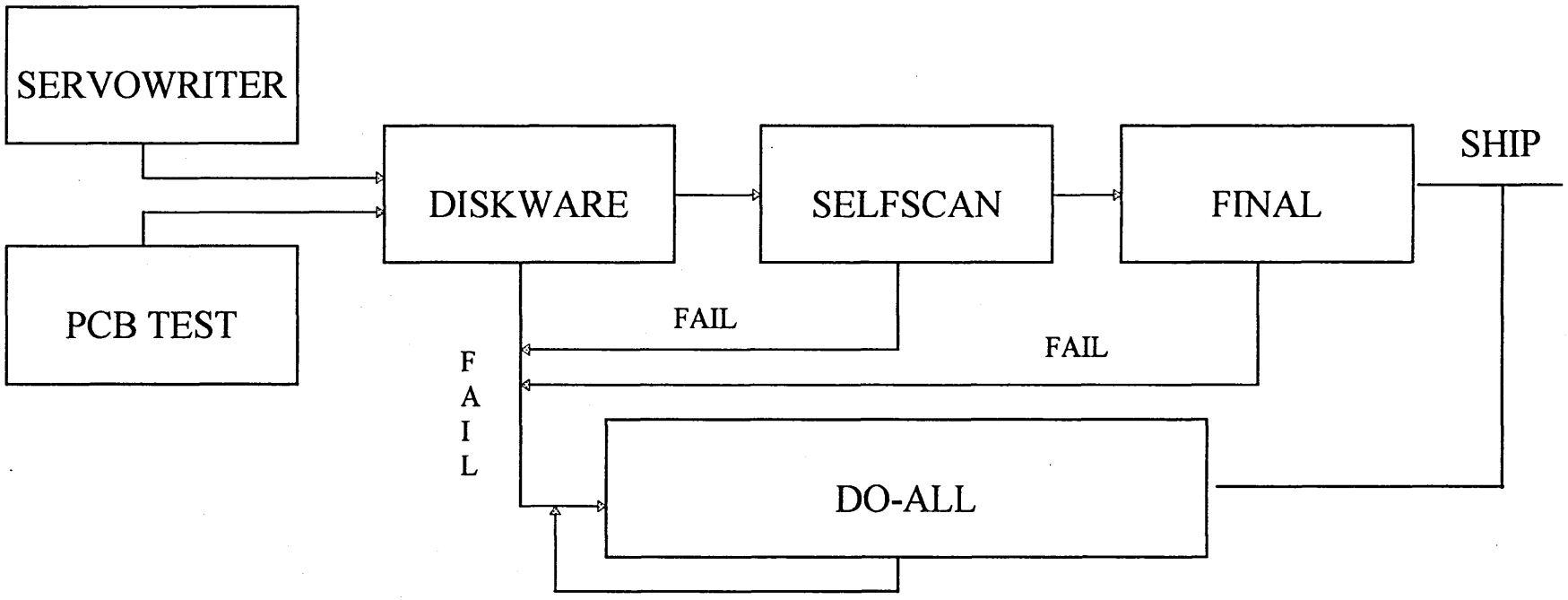
Test Process

Ali Noorian

BIGFOOT TEST PROCESS

Ali Noorian

BIGFOOT TEST PROCESS



SERVOWRITER STATION

- HEAD CONTINUITY TEST (PARAMETRICS)
- WRITE SERVO PATTERNS
- SERVO VERIFY (BUMP/COHERENCE/DROPOUTS, AUDIT)
- SAM2SAM TIMING (FM CHECK)
- TEST TIME ~ 6 MINUTES

PCB TEST STATION

- LOAD RAMWARE
- READ/WRITE TEST
- LOGICAL SCAN (DMA MODE)
- FIXED LENGTH SEEK
- MEMORY TEST
- I/O READY TEST
- TEST TIME ~ 2 MINUTES

PCB TEST STATION

- FIXED LENGTH SEEK < 31 ms

DISKWARE STATION

- ERASE GUARDBANDS
- LOAD RAMWARE
- FORMAT SYSTEM CYLINDERS
- VERIFY SYSTEM CYLINDERS
- INITIALIZE DEFECT LIST
- LOAD DISKWARE
- WRITE SELFSCAN SCRIPT
- TEST TIME ~ 2 MINUTES

SELFSCAN STATION

- RAM TEST
- START/STOP
- SERVO VERIFY
- KLOOP
- READ CHANNEL OPTIMIZATION
- HEAD SWITCH
- THIRD STROKE SEEK
- FULL STROKE SEEK
- RANDOM SEEK
- NULLI
- RUNOUT
- FORMAT
- SEQUENTIAL DEFECT SCAN
- CUSTOMER SCAN
- ECC TEST
- THROUGHPUT TEST
- CUSTOMER SCAN
- START/STOP
- DEFECT SCAN (W2W)
- CSS
- TEST TIMES 4 HRS/7 HRS

SELFSCAN STATION

- START/STOP < 16 sec
- HEAD SWITCH
- < 5ms head switch
- < 7ms head switch + track switch
-
- THIRD STROKE SEEK < 20ms
- FULL STROKE SEEK < 34 ms
- RANDOM SEEK < 18.5 ms
- RUNOUT
- 75 max RRO& NRRO (.1% of track)

- THROUGHPUT TEST
- Read > 4,500,000 bytes
- Write > 4,000,000 bytes
- Random > 2,000,000 bytes
-
- START/STOP < 16 sec
-
- CSS 400 loops

FINAL TEST STATION

- READ SELFSCAN RESULTS
- START/STOP TEST
- CONFIGURE DPA
- LOGICAL SCAN
- THROUGHPUT TEST
- ENABLE DPA
- TEST TIME ~ 4 MINUTES

FINAL TEST STATION

- START/STOP TEST < 18 sec
-
- THROUGHPUT TEST > 1,000,000 bytes

DO-ALL TEST STATION

- DISKWARE STATION
- POWER OFF/POWER ON
- START SELFSCAN
- WAIT SELFSCAN TIME
- POWER OFF/POWER ON
- FINAL TEST STATION
- TEST TIMES 4.5 HRS / 7.5 HRS

There is no document available for UPT, only windows help file that could be used in windows.

BORG\VOL2: \TE\UPT2\UPT.HLP

Marketing Strategy

Joel Mattox

Bigfoot

Market Summary

January 1996

- Product Overview
- Product Positioning and Differentiation
- Market Overview
- Customer
- Competition
- Followon Products
- Appendix:
  - CD-ROM designs
  - Enclosure designs

Bigfoot Overview

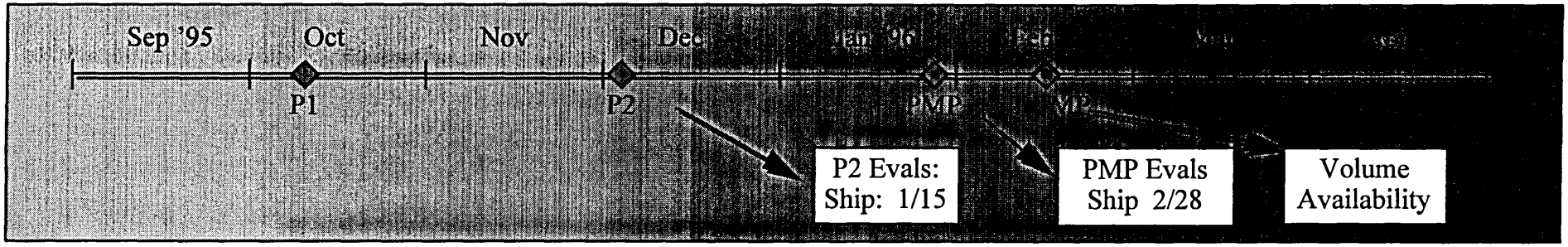
Objectives:

- Be first to ship 5.25" high capacity consumer market products
- Ship 4M units by end of September, 1996
- Successfully position Cyclone
- Establish barriers to entry
- Establish Quantum brand preference in consumer market
- Establish channels/partners for Cyclone and beyond

Program Highlights:

- First "Consumer" drive using 5.25" form factor
- Targeted at consumer markets where only disk drive capacity is advertised
- Early customer feedback is enthusiastic: Great concept, first-to-market

Milestones:



Program Status:

- P2 build completed 12/20; yields 90%
- DVT and Compatibility testing started with no major concerns

- Bigfoot uses mature, low-risk technology and CD-ROM form factor bays to provide the most economical support possible at two key capacity points for high capacity consumer PC systems
  - 2.5GB
    - 18% more storage than 2.1GB
    - Could download 3 full CD-ROMs and have over 500MB left
  - 1.2GB
    - 635MB popularity: natural 2X progression
    - Could download one full CD-ROM (680MB) and have almost 600MB left
- Bigfoot establishes a new HDD form factor by taking advantage of the CD-ROM form factor to create a break-through cost/MB product
- Bigfoot establishes Quantum/MKE's leadership in the consumer market, growing our overall market share and positioning follow-on consumer market products

Bigfoot Description

- Low profile 5.25" 1.2 GB/disk 1.2GB/2.5GB
- Interface: Fast ATA-2
- 3600 RPM, 15.5ms seek
  - Adjustment needed for recognize linear speed and sector per track advantages of 5.25" form factor
- Thin Film Head technology
- Mature, low risk components leveraged wherever possible

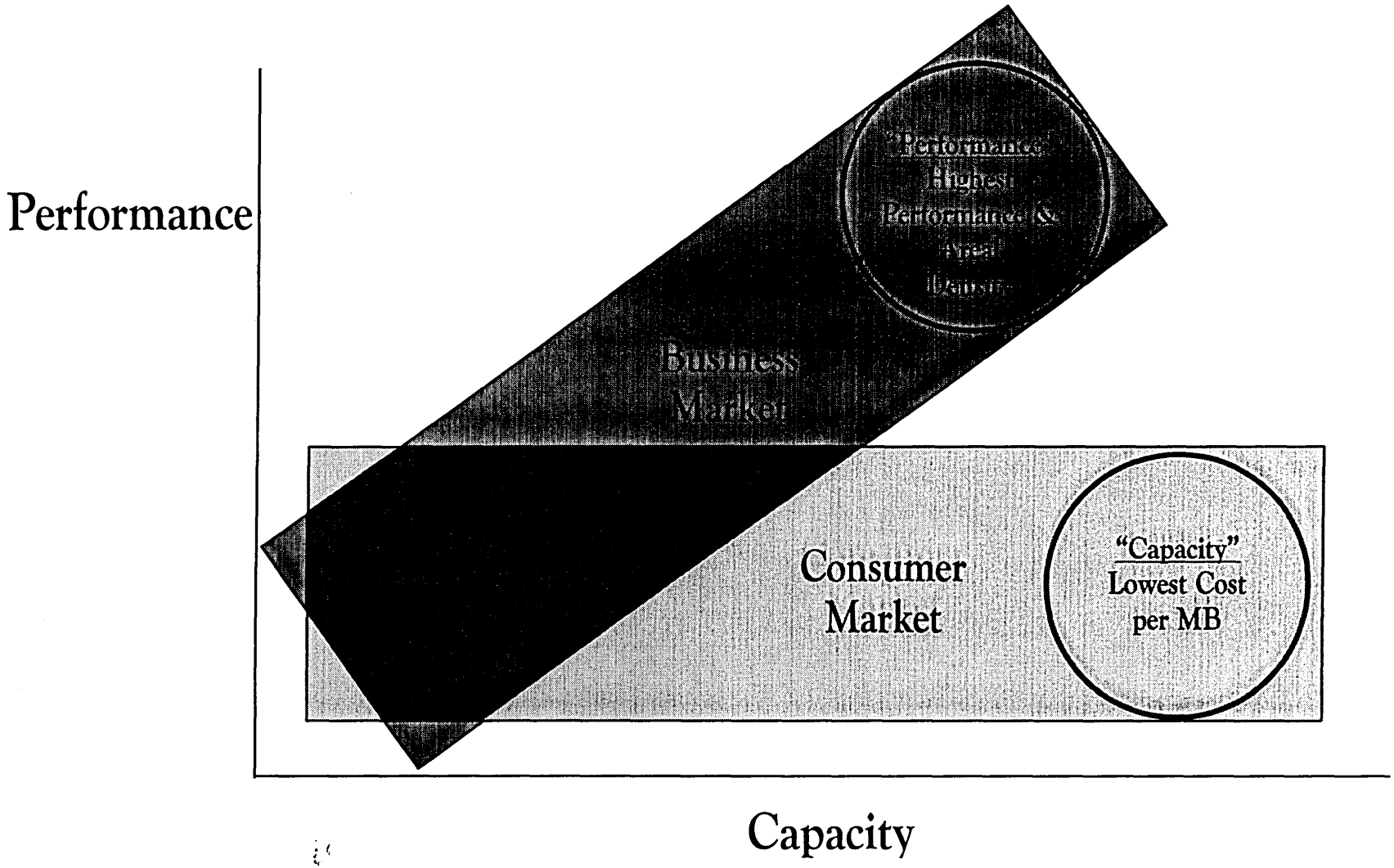
Why Bigfoot?

- Provides advantageous cost/MB at key 1.2GB and 2.5GB capacity points with performance acceptable for consumer products
- Relies on proven, readily available Areal Density technology (Fireball-type TF heads)
- Is designed for MKE automated production, to continue record of highest quality and reliability products
- Provides opportunities for innovative system designs with its ultra-low profile
- Is scheduled well before competitive drives, with First Customer Ship in March 1996

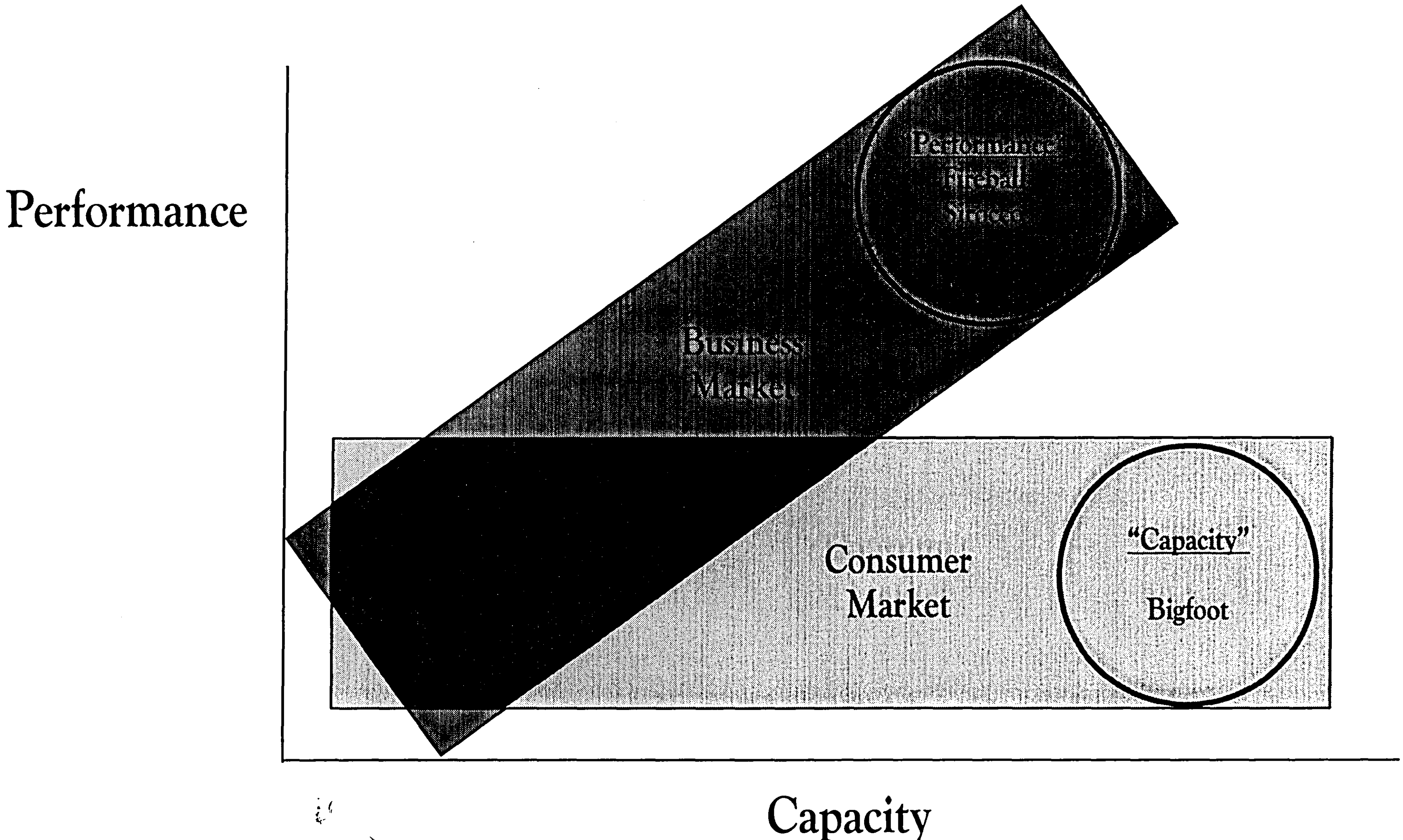
- The consumer market is more willing than the business market to trade performance for cost/MB
  - Since the consumer is self-sufficient they use a wide variety of applications and need more storage capacity than a business PC user
  - Transferring files from CD-ROMs to Bigfoot provides much faster response:
  - A 5.25" HDD has increased stroke and actuator mass and does not provide the seek performance associated with a 3.5" HDD with similar characteristics
  - Leveraged electronics from 3.5" products establishes the linear density and data rate, constraining the feasible 5.25" RPM
    - 25% slower RPM on a 5.25" HDD vs. a 3.5" drive matches data rates
- Differences in 5.25" and 3.5" access performance will be used to segment the market
  - consumer market ⟶ capacity/cost more important ⟶ 5.25" products
  - business PC market ⟶ access more important ⟶ 3.5" products

- 5.25" advantages over a 3.5" product
  - Cost/MB,
  - Independent of exotic AD technology supply base (MR Heads, e.g.)
- 3.5" advantages over a 5.25" product...
  - Established form factor
  - Traditional Performance Specifications
    - Seek, RPM
  - Power Consumption
  - Acoustics
  - SCSI availability

Desktop PC Disk Drive Positioning



Desktop PC Disk Drive Positioning



Similar Features/Specs

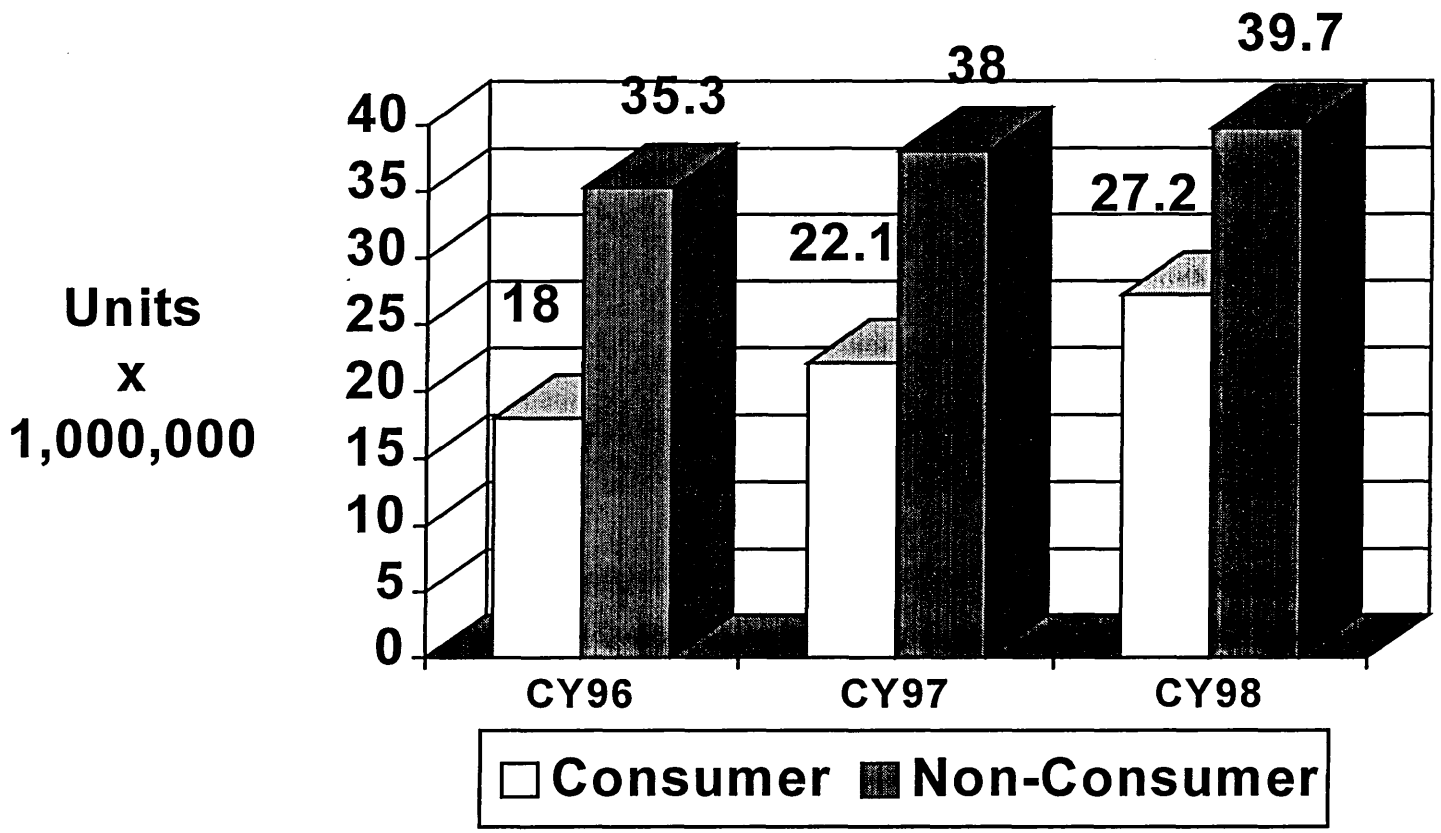
- ATAPI CD-ROM cable sharing
- SMART
- Fast ATA-2

Performance Comparisons

	Average Seek (read, ms)	Motor Speed (RPM)	Data Rate (Mb/sec)
• Fireball	12	5400	84
• Trailblazer	14	4500	54
• Bigfoot	15.5	3600	84
• Quad Speed CD-ROM			
– (for reference)	100-200 (access)	800-2120	4.8 (600Kbyte/sec)

- Traditional usage as main "C" drive for consumer systems
- "D" drive to accelerate/multitask CD-ROM applications
  - Copying CD-ROM apps to HDD will improve speed as well as support multitasking of multiple CD-ROM applications
    - Fastest 6x CD-ROMs: 900KB/s, 120ms access

WW Desktop PC Demand by Market

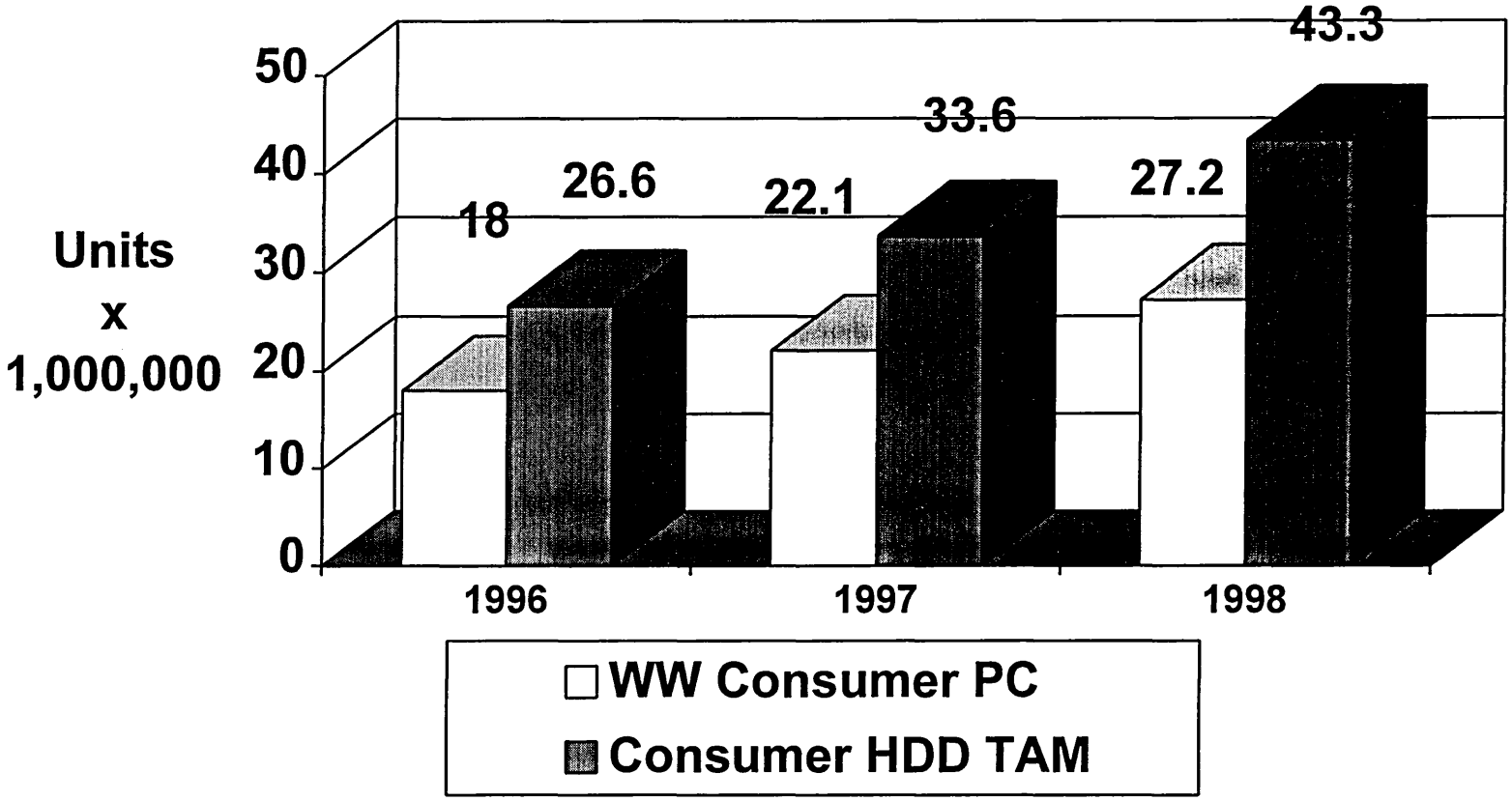


Consumer market provides most of the growth in overall PC shipments

	96-98 Growth
Consumer:	9.2M
Non-Consumer:	4.4M

Source: IDC, DQ

Consumer HDD TAM



1996-8 WW Consumer PC Market:	67.3M units
Average HDD/PC ratio:	1.53
1996-8 WW Consumer HDD market size:	103.5M units

Source: IDC, DQ

CD-ROM Acceptance in Consumer Market

- CD-ROM penetration rate in Home PCs:
  - 1996: 75%
  - 1997: 80%
  - 1998: 85%
- New CD-ROM standards will increase capacity but will keep existing footprint for backward compatibility and recording area

OEMs will continue to provide 5.25" bays, in addition to bays for 3.5" HDD, for consumer PC designs

Source: DQ

Consumer Market Attributes

- Owners highly educated (60% attended college)
- Children, Adult Students, Above Average Income levels associated with presence of home PC
- Teenagers drive vendor selection: computer literate, know what hardware they want (often more than parents), and brag about their computer hardware: Megabytes has replaced horsepower!!
- Parents fear obsolescence (Commodore, Coleco, PC. Jr., etc.)
- Top Home Applications: Household management, schoolwork, games, work brought home

Home Use Needs/Wants

- Easy (if any) installation: NO configuration if possible
- Plug and play, less the plug. Pre-installation strongly preferred, kits next in preference
- Bigger storage at affordable prices
- Faster response on CD-ROM games, other applications
- Capability of multitasking CD-ROM applications

- "SOHO" owners need more functionality than office users
  - No corporate resources to utilize
  - Need to perform many functions at the same time: Multitasking crucial
  - Select hardware capability after determining functionality requirements
  - No 'Red Tape' No Requisition, No budget process
    - Will buy from first source stocking the solution to their needs
    - No Corporate policies limiting type of system or upgrade: can buy whatever they need
  - Tend to buy pre-configured systems

Bigfoot Customer Feedback

- Top Tier:
  - Bigfoot value offering has substantial appeal. OEMs who have been briefed are integrating Bigfoot into their late winter/early spring product plans
  - Ratio starts at about 60% 1D, 40% 2D
  - Capacity point matches with other Quantum products are key
- Distribution:
  - Distribution marketing and sales forecasting Bigfoot demand at over 600K in FQ1
  - Distribution customer feedback: need mockups for form factor support, need <16ms performance

- Performance 5.25"
  - Dominated by Seagate, Micropolis is also shipping
  - Very different target customers: Workstation OEMs
    - Performance, Workstation features demanded
      - ❑ Full Height Form Factor
      - ❑ 10-12 platter
      - ❑ High Performance (5400->7200 RPM)
      - ❑ Workstation oriented interfaces: no demand for ATA
      - ❑ High Cost Designs
  - Very different price point expectations
    - Elite 9: retails for $2,800+
- Consumer 5.25"
  - None currently, but WD, SEG have begun work
    - WD CQ3'96 1-2-3D 1.7GB/Platter 5.25"
    - SEG CQ4'96 1-2D 1-1.2GB/Platter 5.25"
  - Start-ups
    - Difficulty in sourcing media expected to limit real impact of small/new players

Followon 5.25" Products

- 5.25" consumer market is sufficiently attractive to support at least two development teams, potentially more
- Current preliminary thinking about follow-on products:
  - Next 5.25" product: Cyclone
    - 2.1GB/Disk, Q4 CY96 masspro, 1,2,3 disk, 1" high
  - Conceptual Bigfoot III
    - 2.8-3.4GB/Disk, CY97 masspro, 5.25" form factor 1,2,3 disk, 1" high

Quantum's 5.25" Advantages

- Quantum will be first to market with a consumer market 5.25" product
- Quantum will have experience curve and scale advantages over other 5.25" suppliers
- Bigfoot will have availability in mass volumes by Spring 96 for Holiday 96 ramps
- Bigfoot will have Quantum/MKE's traditional industry-leading quality and reliability
- Quantum is convinced that the 5.25" consumer market sufficiently attractive to support at least two development teams
- Second 5.25" product family will be ready in Q4 CY96

- Existing CD-ROM media size and CD-ROM drive footprint will remain mainstream
  - The current media has significant momentum due to the installed base of players and software using 12cm CD-ROM disks
  - The CD-ROM industry is currently standardizing higher capacity format(s) to accommodate digital video and needs the existing 12cm recording area, keeping today's 5.25" CD-ROM drive footprint
  - Systems accommodating a 5.25" CD-ROM drive will also accept a 5.25" hard disk drive.

- The majority of newer systems provide 2 or more 5.25" half-height (1.625") bays
  - of 165 general purpose PC systems reviewed in the 12/94 PC Magazine annual review of IBM-compatible systems, 160 (97%) had three or more 5.25" bays
  - of 556 non-server PCs reviewed between June 1994 and May 1995, 472 (85%) had at least one 5.25" bay available as shipped
  - Bay availability will not limit Bigfoot for most systems
- Restrictive Enclosures
  - Some large Quantum customers have some enclosure designs which may need modification to supply a bay for Bigfoot: all of these either have already been briefed or will have been briefed by October
    - All customers notified so far who have restrictive enclosures are modifying them to support Bigfoot

Diagnostics

Lance Beazley

Quantum DIAGs / APE Tools Discussion Outline

The ISO 9000 Guys

Existing DIAGs (ATADIAG.EXE, SCSIDIAG.EXE, DIAG.EXE)

- Support and Distribution (Amy Hansen x5797)
- Alerts

Other Tools

Faceless DIAG Kernel (Amy Hansen / Mark Martinez)

- ITF - IDLess Track Format Viewer / Generator (Jim Gill)
- FlagMan - Performance Analysis Data Base (Richard Bothne)
- Data Leach - General Purpose Data Logger

New In-House Test Adapter (Symbios based)

PCI Solution

- Ultra, Wide, Differential

New DIAGs

it?

- When will it be released?
- How big is it?
- Will it still have memory problems?
- Is it faster then the old DIAGs?
- Do I need to learn "C"
- What is the documentation like?
- What can it do?
  - Platforms - DOS, Windows (3.1, 4.0, NT), Unix, MAC
  - User Interface
  - Script Language is "C"
    - Variables and Types
    - Function Calls
    - Macros
  - Old Scripts vs New Scripts
  - DLL Architecture
    - BaseCmds.DLL, Buffers.DLL, BasicDrv.DLL, IDEDrv.DLL, SCSIDrv.DLL, FireBall.DLL
  - Drive DLLs, Contexts and Templates
  - User DLLs - (Its extendible)
  - DLLs, VXDs, TSRs, Thunking and other weird jargon.

- Any User Questions
- Qengine -
- SCSI
- ISA /
- What to call

WITs

Paul Heft

Worldwide Issue Tracking System

1 *Welcome To WITS*

2 *Overview*
- WITS Organizational Benefits
- WITS Features, Architecture
- FA/CA Business Workflow
- Using WITS for Case Management
- Reports

3 *WITS Organizational Benefits*
- Clear Ownership of Issues
- Traceability
- Automatic Notification
- Process Measurement
- Solution Knowledge Base
- Document Accessibility

4 *WITS Network Services*

5 *WITS Software Model*

6 *FA/CA Business Process*

7 *Applying WITS to Workflow*

8 *WITS Case Management*

9 *Create*
- FE or QR Opens WITS
- Enters a Title
- Enters Site and Product Data
- Defines Case Type, Severity
- Reports Symptoms
- Saves Case
- Dispatches to Next Group
  - (CSE/CACE, FA/PE)

10 *CaseScreen*

11 *WITS Concepts - Queues*
- Queues and Cases
  - Queues are used to transfer cases from owner to owner
  - A queue may contain many cases
- Queues and Membership
  - Cases in a queue can be accepted only by queue members
  - When a queue member accepts a case, he/she becomes the new owner
- Cases come out of Queues Into Acceptor's WIPbin

12 *WITS Case Routing - I*

13 *WITS Case Routing - II*

14 *WITS Case Routing - III*

Worldwide Issue Tracking System

15 **WITS Case Routing - IV**

- WITS Automatically Tracks Case Originator *and* Subsequent Owners
- Automatically Notifies Queue Members When a Case is Dispatched
- Any Queue Member Can Accept a Case

16 **Ownership Responsibility**

- Case Arrives at Queue
  - Queue Members (Including Supervisor) Notified
- Case Is In Queue
  - Queue Supervisor and Owner Notified Every Two Days
  - It's Still Your Responsibility
  - Can Contact Group Directly If Necessary, Especially If Severity Is High
- Case Is Accepted
  - New Owner Now Has Responsibility Until Dispatch or Close

17 **Update**

- CSE/CACE - Evaluates Customer Issues, Can Solve or Identify Group to Solve Issue
- FA/PE - Begin Work to Identify Detailed Cause of Product Failure
- Can Change Severity, Status, Write Notes, Attach Documents, Create Subcases, Solve
- Saves, Dispatches to Next Group or QA (Corrective Action)

18 **Escalation Level**

- Is Based Upon Status, Severity and Age
- Only Calculated When Customer Close Date Not Entered
- Customer Issues Only
- Replaces Old Calculation That Included Short Term CA Date and Problem Containment Date

19 **Escalation Level - Severity 0**

20 **Escalation Level - Severity 1**

21 **Quality Assurance Intake**

- Monitors Corrective Action
- Groups Similar Problems
- Dispatches Problems to Appropriate Organization for Resolution
- Monitors Specific CARs for Completeness and Appropriateness

22 **Corrective Action Groups Input**

- Determine Failure Root Cause
- Determine Corrective Action for Vendor Supplied Parts and Materials
- Dispatches (Returns) Case to QA

23 **Quality Assurance Wrap Up**

- Evaluate Corrective Action Recommended

- Evaluate Completeness and Appropriateness of CA
- Returns Case to CA Group When Necessary
- Dispatches Problem to Originator or CSE/CACE

24 **Closing a Case**

- Customer Close Date
  - Might Be Prior to Case Closure
- Originator Closes Case
  - Can Be Closed By Non-Originator
    - Case Originator is Notified
  - Reviews Case Resolution
  - Contributes Additional Notes, Comments
  - Writes Closing Summary

25 **Reports**

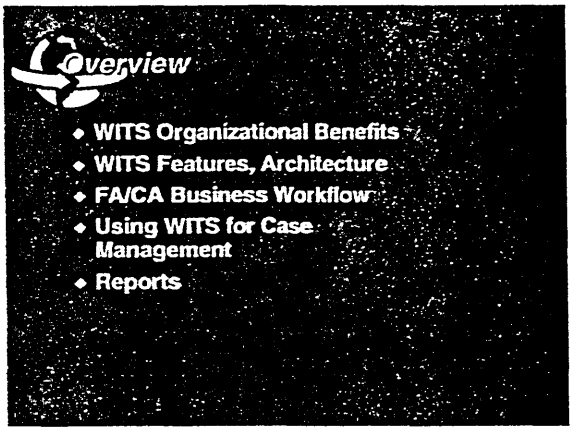
- Case Reports
  - Internal Case Summary Report
  - MKE Report
  - 2 - Line Case Summary Report
  - 3-to-a-Page Case Summary Report
  - Customer Case Summary Report
  - 2-to-a-Page Customer Case Summary Report
  - Case Detail Report - Coming 2/96
- Aging & Escalation Reports

26 **Summary**

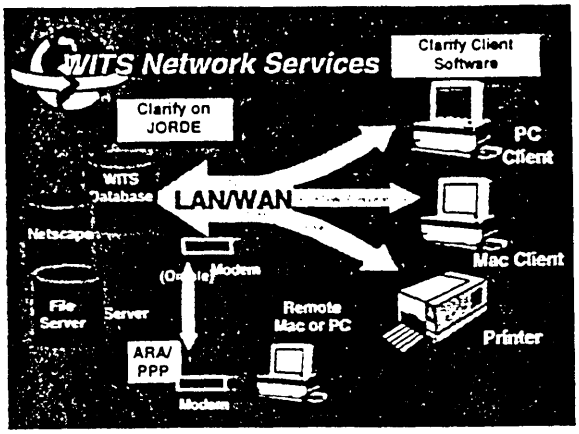
- WITS Organizational Benefits
- WITS Features, Architecture
- FA/CA Business Workflow
- Using WITS for Case Management
- Reports

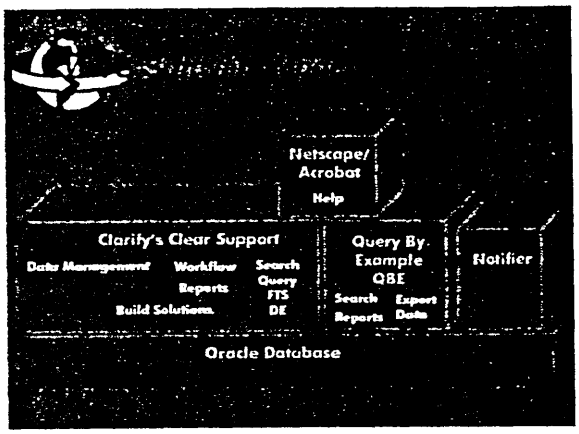
27 **Worldwide Issue Tracking System**

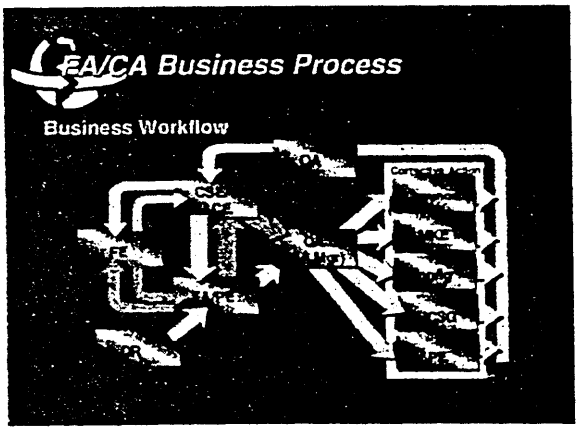
Worldwide Issue Tracking System



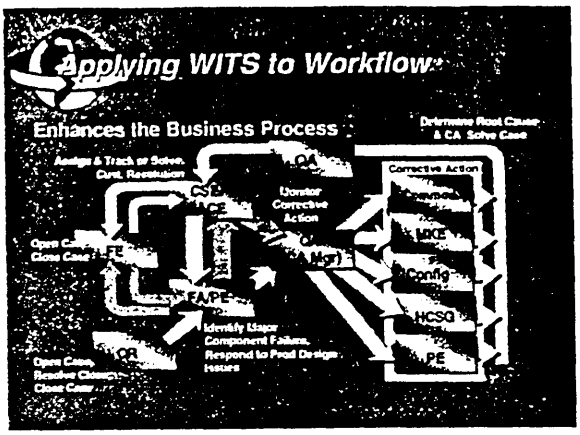
Worldwide Issue Tracking System

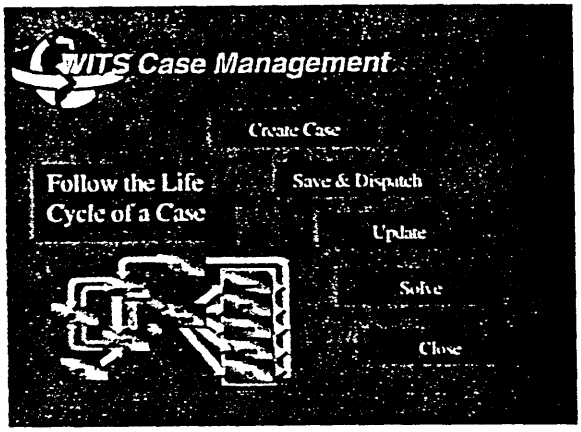


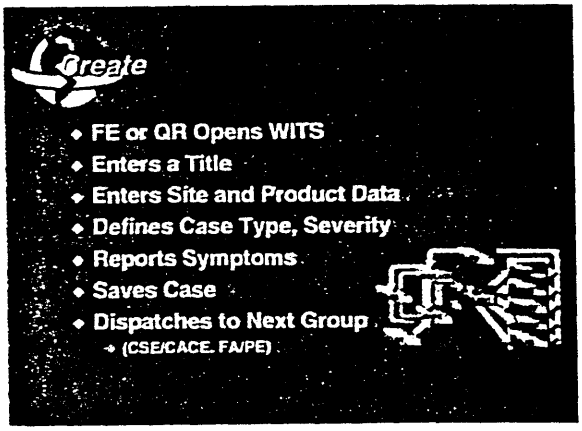




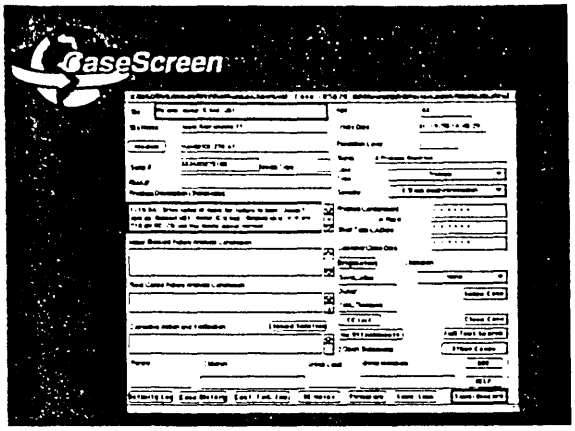
Worldwide Issue Tracking System

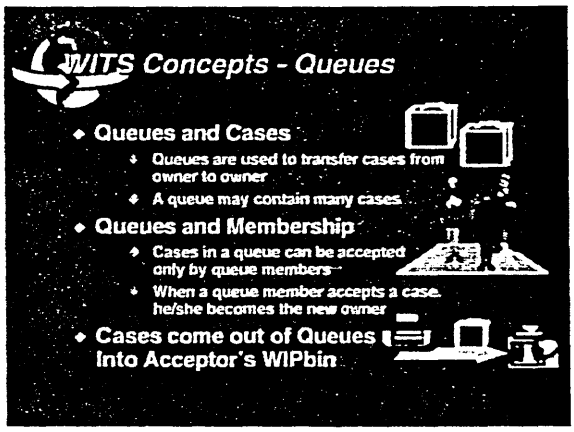


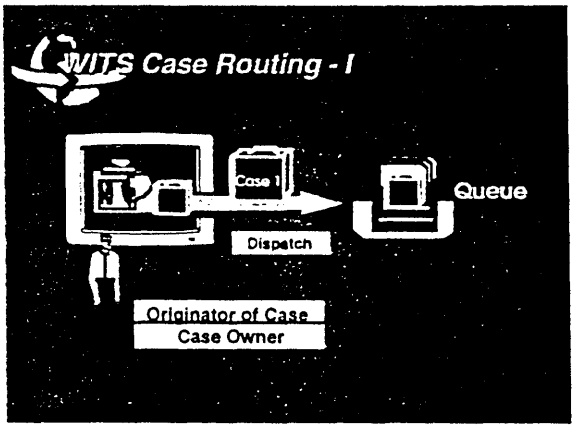




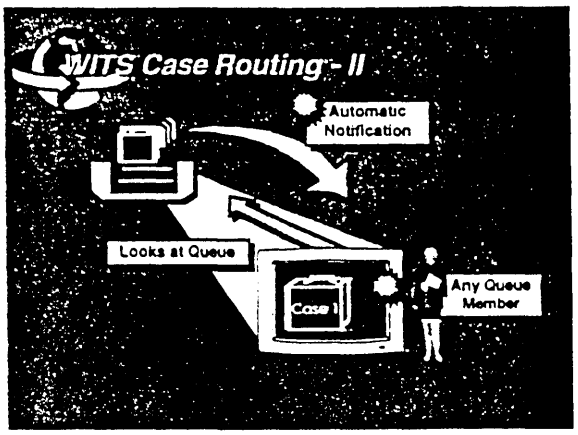
Worldwide Issue Tracking System

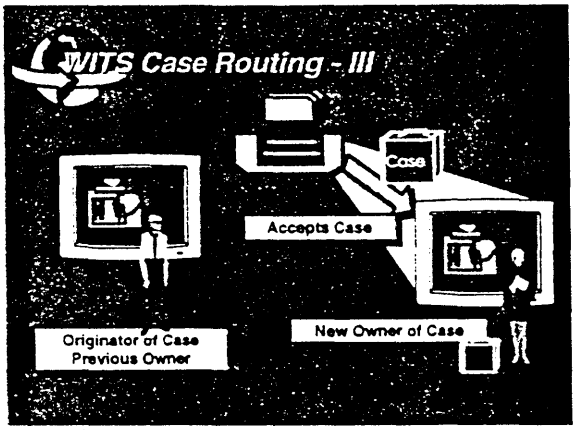


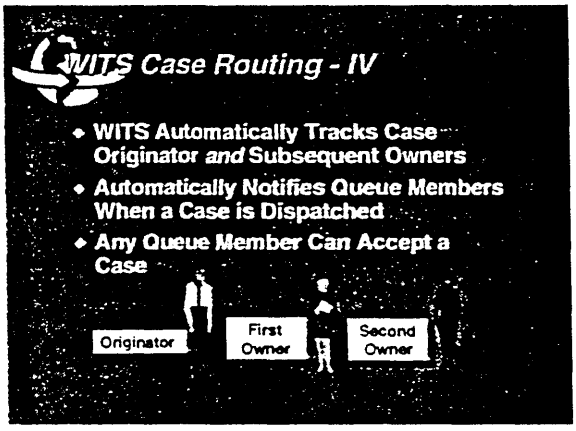




Worldwide Issue Tracking System







Worldwide Issue Tracking System

Ownership Responsibility

- Case Arrives at Queue
  - Queue Members (Including Supervisor) Notified
- Case Is In Queue
  - Queue Supervisor and Owner Notified Every Two Days
  - It's Still Your Responsibility
  - Can Contact Group Directly if Necessary, Especially if Severity is High
- Case Is Accepted
  - New Owner Now Has Responsibility Until Dispatch or Close

Update

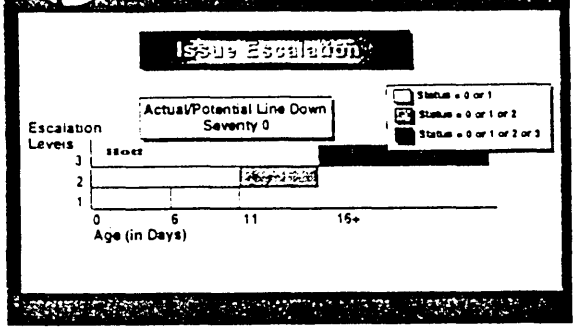
- CSE/CACE - Evaluates Customer Issues, Can Solve or Identify Group to Solve Issue
- FA/PE - Begin Work to Identify Detailed Cause of Product Failure
- Can Change Severity, Status, Write Notes, Attach Documents, Create Subcases, Solve
- Saves, Dispatches to Next Group or QA (Corrective Action)

Escalation Level

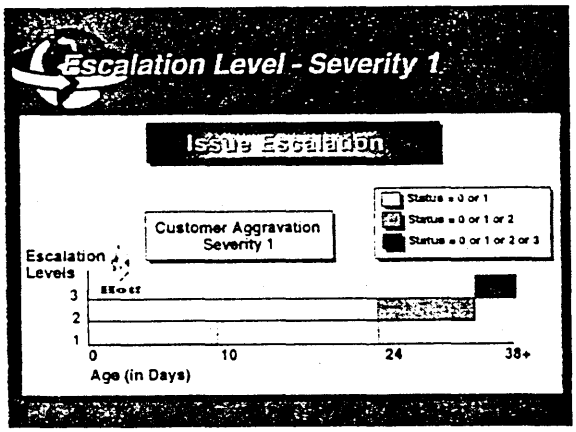
- Is Based Upon Status, Severity and Age
- Only Calculated When Customer Close Date Not Entered
- Customer Issues Only
- Replaces Old Calculation That Included Short Term CA Date and Problem Containment Date

Worldwide Issue Tracking System

Escalation Level - Severity 0



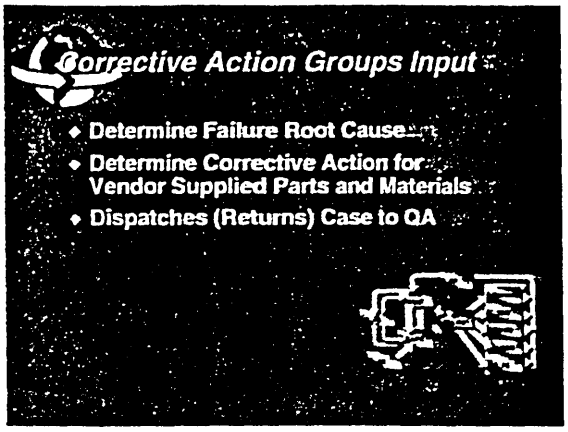
Escalation Level - Severity 1

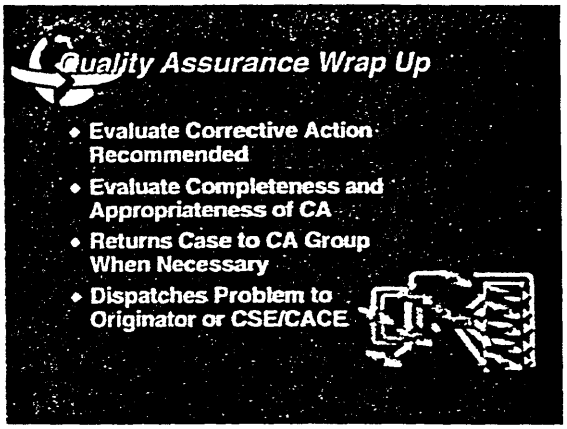


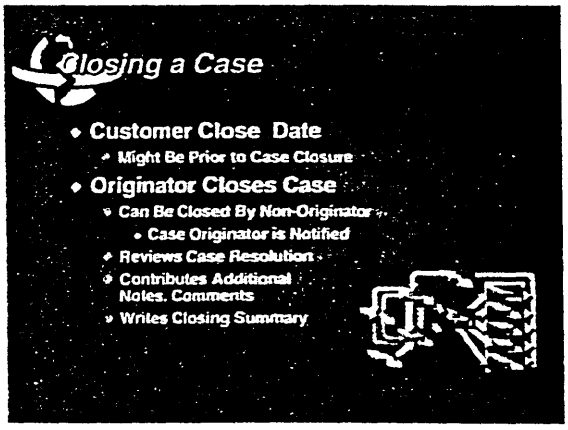
Quality Assurance Intake

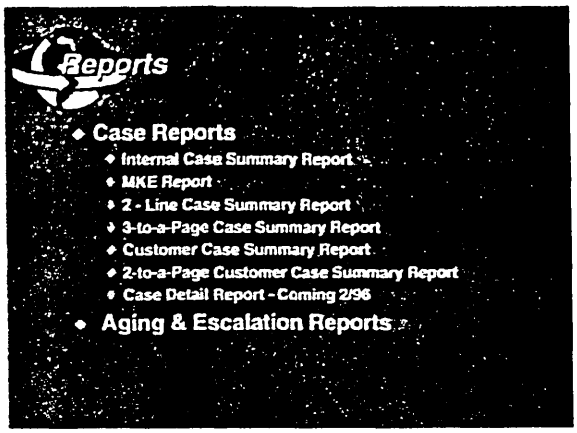
- Monitors Corrective Action
- Groups Similar Problems
- Dispatches Problems to Appropriate Organization for Resolution
- Monitors Specific CARs for Completeness and Appropriateness

Worldwide Issue Tracking System








Reports
Case Reports
Internal Case Summary Report
MKE Report
2 - Line Case Summary Report
3-to-a-Page Case Summary Report
Customer Case Summary Report
2-to-a-Page Customer Case Summary Report
Case Detail Report - Coming 2/96
Aging & Escalation Reports


Summary
WITS Organizational Benefits
WITS Features, Architecture
FA/CA Business Workflow
Using WITS for Case Management
Reports


Worldwide
Issue
Tracking
System

DPA

Kevin Tso

S.M.A.R.T

Presented by
Tim Nelson

Systems Engineering Department

January 10, 1996

Overview

- SMART originated as a joint venture between Compaq and Quantum as a means of monitoring the ongoing reliability of the drive.

- This feature started out as Failure prediction, was renamed **D**rive **P**arameter **A**nalysis and is now called SMART for **S**elf Monitoring and **R**eporting **T**echnology

- SMART does not enhance the reliability of the drive, it enhances the reliability of the *data* by warning users of potential drive failure situations.

- This was a feature on AT drives only but is being added to SCSI as well.

Overview

- Phase 1 SMART was a prototype only
- Phase 2 SMART has been implemented on Maverick, Roadrunner, Thunderbolt and on Lightning.
- Phase 3.5 SMART has been implemented on Fireball, Trailblazer Sirocco and Europa..
- Phase 4 SMART is being implemented on Saguaro, Stratus, and Vortex. This is the current 'state of the art'

Overview

Phase 2 SMART started by tracking the following drive parameters:

- Number of grown defects.
- Power on time. (hours)
- Number of start cycles. (Contact Start/Stop)
- Number of power cycles

Overview

Phase 3 SMART added the following drive parameters:

- Spin up time
- Read Soft Error rate
- Seek Error rate
- Recal retry count

Phase 3.5 added a command to self check SMART for failure. No Phase 3 drives were shipped. Only phase 3.5

Overview

Phase 4 SMART added:

- Raw Read error rate testing
- Offline Testing
- Automatic Offline testing
- Early Calculation on some attributes:
  - Seek error rate
  - Read soft error rate

Other comments:

- Data is transferred as a single block of 512 bytes.
- User Enable/disable with AT command B0 and subcode.
- ***Attributes*** are what we call the different parameters.
- Attribute data is preserved on the disk and may be updated by:
  1. Write attribute command
  2. Read attribute command (will update disk and return data)
  3. Spindown (power saving mode)
  4. An auto timer.

SMART COMMANDS :

TASK FILE REGISTER SETUP.

TF.0 = NA
TF.1 = Function subcode (D0-D9) see below
TF.2 = Sector count (1 = data txfer, 0 = no data txfer)
TF.3 = NA (Sector number, always set 1)
TF.4 = Password low (= 4Fh)
TF.5 = Password High (= C2h)
TF.6 = Drive /head (**drive select**, head doesn't matter)
TF.7 = 0B0H (The SMART **generic access command**)

SMART COMMANDS:

The following is a summary of the function subcodes passed in the *features register* when issuing a command:

0D0H	Read Drive Attribute values
0D1H	Read Warranty Failure Threshold
0D2H	Auto update enable/disable
0D3H	Write Drive Attribute values
0D4H	Offline Test command
0D5H-0D7H	Reserved
0D8H	Enable failure prediction data collection
0D9H	Disable failure prediction data collection
0DAH	Check SMART or Internal Compare
0DBH	Offline test timer enable/disable

SMART COMMANDS:

Feature register:	**Description of command:**
0D0H	Read Drive Attribute values Returns 512 bytes of stored failure prediction data See '*Returned Data Format*' for details.
0D1H	Read Warranty Failure Threshold. 512 bytes of data used to compare to Attribute data. (i.e. is Attribute < Warranty?) See '*Warranty Data Format*' for details.

SMART COMMANDS:

Feature register:	Description of command:
0D2H	Auto update enable/disable. *Sector count* register sets the update time. This is the same as the power management timer. Sector count values are: 0- disable timer. 1-240 (value * 5) seconds 241-251 (value - 240) * 30) minutes 252 21 minutes 253 Vendor unique period between 8 and 12 hours 254 Reserved 255 21 minutes 15 seconds

SMART COMMANDS:

Feature register:	Description of command:
0D3H	Write Drive Attribute values This will flush the data to the disk. We also include a flush to disk as part of the Read Attribute command. The stored data may also be updated on spindown or by the automatic timer. (see above).

SMART COMMANDS:

Feature register:	Description of command:
0D4H	Offline Test request This command will tell the drive to commence a raw read error rate test by itself
0DBH	Offline Test timer enable This command will set a timer (Timer value in TF.2 - the same as the auto save or power mode timer). If the drive is idle for the given time then it will perform offline testing on its own.

SMART COMMANDS:

Feature register:	**Description of command:**
0D8H	Enable failure prediction data collection Turn on the Failure prediction firmware.
0D9H	Disable failure prediction data collection. All commands will be invalid **EXCEPT** *ENABLE*. Although SMART is disabled the following attributes will be preserved: Power Cycles — Contact Start/Stop Grown Defects — Spin up time

SMART COMMANDS:

Feature register: **Description of command:**

0DAH Internal Compare. Introduced in Phase 3.5.
Compare the CURRENT Normalized attribute to the warranty threshold. If the drive detects a warranty threshold exceeded then we flip the nibbles in the cylinder low and high register as shown below.

	TF.0	TF.1	TF.2	TF.3	TF.4	TF.5	TF.6	TF.7
PASS	NA	DA	0	1	***4F***	***C2***	A0	B0
FAIL	NA	DA	0	1	***F4***	***2C***	A0	B0

SMART ATTRIBUTES:

Attribute ID numbers for returned data

#	Attribute
1	Raw Read Error Rate
3	Spin up time
4	Start stop count
5	Re-allocated sector count
7	Seek error rate
9	Power on hours
11	Drive recalibration retry count
12	Power cycle count
13	Read Soft error rate
21-30	Vendor Unique Attributes

Attributes numbers 2, 6, 8, 10, 13-20 are Reserved

DRIVE ATTRIBUTE DATA:

Return data format

Entry	Length	Offset
Data Structure revision number	2 bytes	0
1st drive attribute structure	12 bytes	2
2nd drive attribute structure	12 bytes	14
3rd drive attribute structure	12 bytes	26
.....		
30th drive attribute structure	12 bytes...	350
Offline data collection	6 bytes	362
Drive fail prediction	2 bytes	368
Reserved	92 bytes	370
Vendor Unique	49 bytes	462
Checksum	1 byte	511

SMART ATTRIBUTE DATA:

Format of each Data structure entry:

Field	# bytes
Attribute ID #	1
Status Flags	2
Normalized Attribute Value	1
Worst ever Normalized attribute	1
Raw Attribute Value	6
Reserved	1
---	---
Total bytes	12

SMART ATTRIBUTE DATA:

Format of Data structure entry:

Attribute ID: This byte will identify the attribute field. Refer back to attribute ID's

Status Flags:	**bit**	
Pre failure warranty flag	0001	If set, an attribute failure covered under warranty
On line collection bit	0002	Attribute Value updated during online OR offline testing
Performance attribute type	0004	If set this is a performance issue
Error rate attribute type	0008	If set this is an error rate attribute
Event count Attribute	0010	If set, this is an event count attribute

Self preserving attribute	0020	If set then this is preserved even if SMART is disabled (Power cycles, grown defects)
Reserved	bits 15-6	are reserved

Normalized Attribute Value: Values here are *Normalized* for a range of 1 to 100. Algorithms to convert raw data into a normalized value vary from product to product and from attribute to attribute.

Worst ever Normalized value: This returns the worst case occurrence. On occasion a drive may go from good to bad and then recover. Again the Valid values are from 01 to 100 decimal. Note that this is initialized to 0FDh.

RAW Attribute Value: The six bytes used store the raw data.

SMART Attribute Status values:

Attribute		Status byte	Self preserving 20H	Event count 10H	Error rate 08	Performanc type 04	Online collection 02	Prefailure warranty 01
1	Raw Read error rate	09			X			X
3	Spin up time	27	X			X	X	X
4	Start/Stop count	32	X	X			X	
5	Grown Defect	33	X	X			X	X
7	Seek error	0B			X		X	X
9	Power on hours	12		X			X	
11	Recal retry	13		X			X	X
12	Power cycle	32	X	X			X	
13	Read error rate	0B			X		X	X

Example of READ ATTRIBUTE DATA:

ATTRIB	Off-set	ATB#	STATUS		NORM	WORST NORM	RAW DATA	RES
REV	00	04	00					
Read error rate	02	01	0B	00	4D	3E	03 00 00 00 00 00	00
Spin up time	0E	03	27	00	64	64	00 00 00 00 00 00	00
Start/Stop count	1A	04	32	00	64	64	01 00 00 00 00 00	00
Grown Defect	26	05	33	00	64	64	00 00 00 00 00 00	00
Seek error	32	07	0B	00	64	64	00 00 00 00 00 00	00
Power on hours	3E	09	12	00	64	64	03 00 00 00 00 00	00
Recal retry	4A	0B	13	00	64	64	00 00 00 00 00 00	00
Power cycle	56	0C	32	00	64	64	01 00 00 00 00 00	00
End	62	00	00	00				
Checksum	1FE	04	BD		Two checksums:Quantum and Compaq			

Example of READ WARRANTY DATA:

ATTRIB	Off-set	ATB#	Threshold	All remaining bytes = 0
REV	00	04	00	
Read error rate	02	01	14H	00 00 00 00 00 00 00 00 00 00
Spin up time	0E	03	14H	00 00 00 00 00 00 00 00 00 00
Start/Stop count	1A	04	08H	00 00 00 00 00 00 00 00 00 00
Grown Defect	26	05	14H	00 00 00 00 00 00 00 00 00 00
Seek error	32	07	14H	00 00 00 00 00 00 00 00 00 00
Power on hours	3E	09	1	00 00 00 00 00 00 00 00 00 00
Recal retry	4A	0B	14H	00 00 00 00 00 00 00 00 00 00
Power cycle	56	0C	08H	00 00 00 00 00 00 00 00 00 00
End	62	00		
Checksum	1FF	53		

SMART command (summary)

Summary of command format:

	TF.0	TF.1	TF.2	TF.3	TF.4	TF.5	TF.6	TF.7
Read attribute values	NA	D0	1	1	4F	C2	A0	B0
Read Warranty Threshold	NA	D1	1	1	4F	C2	A0	B0
Auto Update	NA	D2	XX	1	4F	C2	A0	B0
Write Attributes	NA	D3	0	1	4F	C2	A0	B0
Perform Offline testing	NA	D4	0	1	4F	C2	A0	B0
Enable	NA	D8	0	1	4F	C2	A0	B0
Disable	NA	D9	0	1	4F	C2	A0	B0
Internal Compare	NA	DA	0	1	4F*	C2*	A0	B0
Set Offline Timer	NA	DB	XX	1	4F	C2	A0	B0

S.M.A.R.T

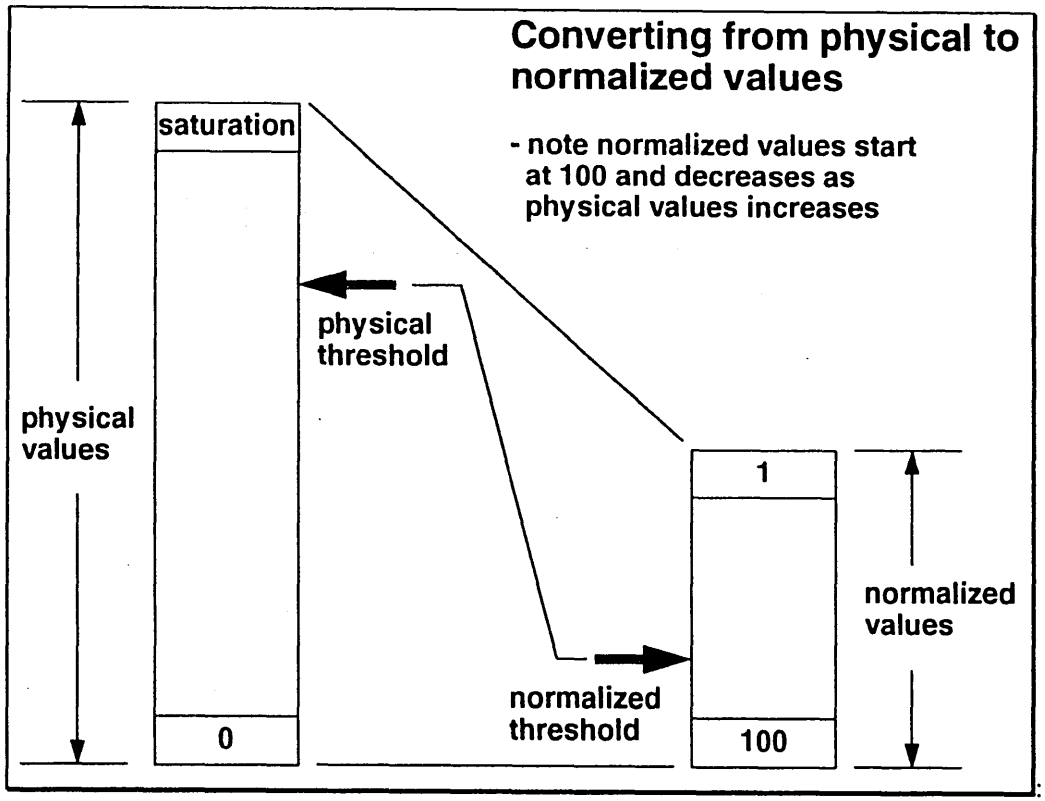
Part II: Implementation Details

Tim Nelson
Systems Engineering Department

January 10, 1996

The Concept of Normalization

A physical attribute value is converted to a logical value ranging from 1 to 100, representing the percentage of the saturation point of that attribute. Therefore, 100 is usually the value when the drive first comes out of the factory.



$$NormalizedValue = 100 - 100 * \frac{PhysicalValue}{PhysicalSaturation}$$

Configuration Page 19

Configuration page 19 holds the 'Master switch' to turn the entire SMART feature on and off and also some of the parameters we need to set. Bytes 18-22 are new for SMART Phase 4

Byte	Setting	Meaning
0	0	Timer setting - unused
1	80h	Master switch 80h = ON 00h = OFF
2-5	3E80h (16000)	Seek error sample size
6	0Dh (13)	Seek error saturation size
7-10	17D78h (97656)	Read error sample size
11	0Dh (13)	Read error saturation value
12-13	14h (20)	Spin up time sample size
14-15	30D4 (12500)	Spin up time saturation value mSec.
16	0Ah (10)	Recal retry sample size
17		Spare
18-19	TBD	Raw Read error: Total Blocks to Read
20	TBD (32 now)	Logical blocks/seek
21	TBD	Read error Saturation value/segment
22	05	Revision # for config page 19

Configuration Page 19

Following is a data dump from a typical page 19 read of a Fireball (SMART Phase 3.5)

> RDCONF 19
History Logging Frequency = 0 seconds

> dmp 0 bytes-1

00 80 80 3E 00 00 0D 78 D7 01 00 0D 14 00 D4 30 0A 01

Initialize SMART command

- The INIT SMART command will initialize the attribute fields in to starting condition. This will zero out counts such as Power-on-hours and Contact-start-stop. Macro is as follows:

```
macro  init   super, func skp, cdb.2 49h, cdb.3 4eh, cdb.4 49h,
              cdb.5 54h, cdb.6 28h, excdb
```

Write Warranty Command

- The Write Warranty command uses Subcode 0D7h.
  (tf.1 0d7h, tf.2 1, tf.3 1, tf.4 04fh, tf.5 0c2h, tf.7 0b0h)

- The write warranty command is used to write the threshold information to the disk. See warranty information format for details.

- It is ONLY available when SUPER is enabled.

- The warranty threshold information should be written at MKE or at configuration time.

- It is not to given to customers and is not for their use.

Summary of commands

	TF.0	TF.1	TF.2	TF.3	TF.4	TF.5	TF.6	TF.7
Read attribute values	NA	D0	1	1	4F	C2	A0	B0
Read Warranty Threshold	NA	D1	1	1	4F	C2	A0	B0
Auto Update	NA	D2	XX	1	4F	C2	A0	B0
Write Attributes	NA	D3	0	1	4F	C2	A0	B0
Offline Data Collection	NA	D4	0	1	4F	C2	A0	B0
Read Logging sectors *1	NA	D5	1	1	4F	C2	A0	B0
Write Logging Sectors *1	NA	D6	1	1	4F	C2	A0	B0
WriteWarrantyThreshold *2	NA	D7	1	1	4F	C2	A0	B0
Enable	NA	D8	0	1	4F	C2	A0	B0
Disable	NA	D9	0	1	4F	C2	A0	B0
Internal Compare	NA	DA	0	1	4F*	C2*	A0	B0
Set Offline timer	NA	DB	XX	1	4F	C2	A0	B0

*1 Unused

*2 Super mode only

Overview of Attributes parameters:

#	Attribute	Threshold	Saturation Value	Sample size	Threshold fails at
1	Raw Read error rate	TBD	TBD	See config page 19	TBD
3	Spin up time (in mSec)	20%	12500	20	10000
4	Contact Start Stop	8%	65535	NA	60260
5	Grown defects	20%	Varies*	NA	Varies*
7	seek error	20%	13	16000	11
9	Power on Hours	1%	65535	NA	64485
11	Recal retries	20%	5 TRB 4 FRB	10	4 TRB 3.2 FRB
12	Power cycle	8%	65535	NA	60260
13	Read Soft error rate	20%	13	97656 sectors	11

Attribute # 01 The *Raw Read Errors* attribute

- New for Phase 4. ID#1 is now ID#13
- Status:09 = ErrorRate + Warranty
- Sample size = TBD
  Saturation value = TBD
  Warranty threshold = TBD

- Seek to a random CHS, read/verify 'n' sectors and log the errors. re-seek and read until the requisite number of blocks has been read.
- Errors logged are:
  - Errors that are ECC correctable
  - Errors that are ECC uncorrectable
  - Errors recovered with retry.
  - ECC on-the-fly errors are ***not*** counted

Attribute # 03 The *Spin Up Time* attribute

- Spin up time is measure in milliseconds.
- Status: 27h= Self preserving + Performance Attribute + Online collection + Warranty
- Sample size = 20
  Saturation value = 12500 (mSec)
  Warranty threshold = 20% (average spin up of 10 Sec.)
- Accumulate spin up times is milliseconds for 20 spin ups, then set new raw value and Normalize.

Attribute # 04 The *Contact Start/Stop* attribute

- Raw data hold count of start cycles.
- Counter incremented on Spin up from standby mode or power on.
- Status: 32h= Self preserving + Event count attribute + Online
- Sample size = NA
  Saturation value = 65535
  Warranty threshold = 8 (corresponds to 60260 start/stops)

Attribute # 05 The *Grown Defects* attribute

- Raw data holds number of *grown defects* - Does not include Factory defects.

- Status: 32h= Self preserving + Event count attribute + Online + Warranty attribute

- Sample size = NA
  Saturation value = Number of grown defect available (I.E. Total defect list size - factory defects)
  Warranty threshold = 20 (corresponds to 92 % remaining defects filled)

- NORM = 100 - 100*(raw_data_count /max # grown defects).

Attribute # 07 The *Seek Errors* attribute

- Raw data holds number of Seek errors ecnoutnered during one Sample size
- Status: 0B = ErrorRate + Online collection + Warranty
- Seek error rate of 6.25 E-4 corresponds to 10 errors in 16000 seeks.
- Sample size = 16000 seeks,
  Saturation value = 13 seek errors
  Warranty threshold = 20 (corresponds to 11 errors in 16000)
- NORM = 100 - 100*(raw_data_count / saturation value).

Attribute # 09 The *Power-on-hours* attribute

- Raw data holds number of Power on hours
- Status: 012h = Event count + Online collection
- Sample size = NA
  Saturation value = 65535 hours
  Warranty threshold = 1 (corresponds to 64845 hours)
- NORM = 100 - 100*(raw_data_count / saturation value).

Attribute # 11 The *Recal Retries* attribute

- Raw data holds the number of retries
- Status: 013h = Event count + Online collection + Warranty
- Sample size = 10
  Saturation value = 5 Trailblazer or 4 Fireball.
  Warranty threshold = 20 (corresponds to 4 TRB, 3.2 FRB)
- NORM = 100 - 100*(raw_data_count / saturation value).

Attribute # 12 The *Power Cycles* attribute

- Raw data holds the number of power cycles
- Status: 032h = Self Preserving + Event count + Online
- Sample size = NA
  Saturation value = 65535
  Warranty threshold = 8 (corresponds to 60260 power cycles)
- NORM = 100 - 100*(raw_data_count / saturation value).

Attribute #13 The *Read Soft Errors* attribute

- New ID for Phase 4. Phase 2-3.5 *was* ID#1
- A read soft error is a firmware ecc corrected error.
  This does ***not*** include:
  - Retry recovered errors,
  - Ecc on the fly recovered errors,
  - Unrecoverable errors
- Status: 0B = ErrorRate + Online collection + Warranty
- Read error rate of 10 errors in 4E8 bits corresponds to
  1 *read soft error* in 97656 sectors
- Sample size = 97656
  Saturation value = 13
  Warranty threshold = 20%. (corresponds to 11 errors)

MISCELLANEOUS

- Documents, Diag programs, macros and other information can be found on the server:
  BORG\VOL1:\SHARE\SE\DOCUMENT\STANDARD\SMART

- Some of the information found in this presentation is still confidential between Compaq and Quantum.

Commands Overview

	TF.0	TF.1	TF.2	TF.3	TF.4	TF.5	TF.6	TF.7
Read attribute values	NA	D0	1	1	4F	C2	A0	B0
Read Warranty Threshold	NA	D1	1	1	4F	C2	A0	B0
Auto Update	NA	D2	XX	1	4F	C2	A0	B0
Write Attributes	NA	D3	0	1	4F	C2	A0	B0
Perform offline	NA	D4	0	1	4F	C2	A0	B0
Enable	NA	D8	0	1	4F	C2	A0	B0
Disable	NA	D9	0	1	4F	C2	A0	B0
Internal Comp.	NA	DA	0	1	4F	C2	A0	B0
(Internal comp register on fail)	NA	DA	0	1	F4	2C	A0	B0
Set offline timer	NA	DB	XX	1	4F	C2	A0	B0

DIAG MACROS

Read Attributes	macro	rdatb	func rd, tf.1 0d0h, tf.2 1, tf.3 1, tf.4 04fh, tf.5 0c2h, tf.6 0a0h, tf.7 0b0h, extf
Read Warranty	macro	rdwarnty	func rd, tf.1 0d1h, tf.2 1, tf.3 1, tf.4 04fh, tf.5 0c2h, tf.6 0a0h, tf.7 0b0h, extf
Write attributes to disk	macro	wratb	func sk, tf.1 0d3h, tf.2 0, tf.3 1, tf.4 04fh, tf.5 0c2h, tf.6 0a0h, tf.7 0b0h, extf
not used	macro	offline	func sk, tf.1 0d4h, tf.2 0, tf.3 1, tf.4 04fh, tf.5 0c2h, tf.6 0a0h, tf.7 0b0h, extf
not used	macro	rdlog	func rd, tf.1 0d5h, tf.2 1, tf.3 1, tf.4 04fh, tf.5 0c2h, tf.6 0a0h, tf.7 0b0h, extf
not used	macro	wrlog	func wr, tf.1 0d6h, tf.2 1, tf.3 1, tf.4 04fh, tf.5 0c2h, tf.6 0a0h, tf.7 0b0h, extf
Write warranty Threshold (SUPER)	macro	wrwarnty	func wr, tf.1 0d7h, tf.2 1, tf.3 1, tf.4 04fh, tf.5 0c2h, tf.6 0a0h, tf.7 0b0h, extf
dpa enable command	macro	dpaenb	func sk, tf.1 0d8h, tf.2 0, tf.3 1, tf.4 04fh, tf.5 0c2h, tf.6 0a0h, tf.7 0b0h, extf
dpa disable command	macro	dpadsb	func sk, tf.1 0d9h, tf.2 0, tf.3 1, tf.4 04fh, tf.5 0c2h, tf.6 0a0h, tf.7 0b0h, extf
dpa 'master switch'	macro	dpaon	rdconf 19, depb 1 80h, wrconf 19
initialize DPA (SUPER)	macro	init	super, func skp, cdb.2 49h, cdb.3 4eh, cdb.4 49h, cdb.5 54h, cdb.6 28h, excdb
Internal Compare	macro	intcmp	func sk, tf.1 0d9h, tf.2 0, tf.3 1, tf.4 04fh, tf.5 0c2h, tf.6 0a0h, tf.7 0b0h, extf

Documents and batch files available on the server BORG\VOL1:\SHARE\SE\DOCUMENT\STANDARD\SMART

Overview of attributes

#	Attribute	Threshold	Saturation	Sample size	Threshold fails at		Status byte	Self preserve 20H	Event count 10H	Error rate 08	Performance type 04	Online 02	Warranty 01
1	Raw Read error	?	?	?	?					X			X
3	Spin up time (mSec)	20	12500	20	10000		27	X			X	X	X
4	Contact Start Stop	8	65535	NA	60260		32	X	X			X	
5	Grown defects	20	Varies*	NA	Varies*		33	X	X			X	X
7	seek error	20	13	16000	11		0B			X		X	X
9	Power on Hours	1	65535	NA	64845		12		X			X	
11	Recal retries	20	5 TRB 4 FRB	10	4 TRB 3.2 FRB		13		X			X	X
12	Power cycle	8	65535	NA	60260		32	X	X			X	
13	Read soft error	20	13	97656	11		0B			X		X	X

Config page 19

Byte	Setting	Meaning
0		Auto timer setting
1	80h	Master switch 80h=ON 00= OFF
2-5	3E80h (16000)	Seek error sample size
6	0Dh (13)	Seek error saturation size
7-10	17D78h (97656)	Read error sample size
11	0Dh (13)	Read error saturation value
12-13	14h (20)	Spin up time sample size
14-15	30D4 (12500)	Spin up time saturation val mSec.
16	0Ah (10)	Recal retry sample size
17		Spare
18-19	TBD	Raw Read error:Total Blcks to RD
20	TBD (32 now)	Logical blocks/seek
21	TBD	Read error Saturation val/segment
22	05	Revision # for config page 19

TF.2 Values for Programming the Auto-timer	
0	disable timer.
1-240	(value * 5) seconds
241-251	((value - 240) * 30) minutes
252	21 minutes
253	Vendor unique period 8 - 12 hours
254	Reserved
255	21 minutes 15 secondS

SMART Development Models

By Kevin Tso

Based on perceived Compaq requirements, I have grouped what development teams need to do into three models. Resource constraint and SMART development objectives will dictate which model you will select.

It is likely that Compaq will demand some sort of data showing the effectiveness of SMART. From past experience, data from the CSS test, which measures spin-up time, and detects read errors, seem to be sufficient for them.

Model #1 - Bare Bones

Pros
Can be done without additional resources, providing that Q/R is already doing CSS testing to failure. Otherwise, we may need to change the CSS testing methodology.

Cons
Large padding in the thresholds may make them ineffective. There is little experimental data to show whether thresholds are effective until the completion of CSS test, which takes two months. There is no data to show that SMART won't fail drives straight out of the factory.

Activities
- Pass Functional Test
- Pass Feature Test
- Select thresholds with lots of padding
- Provide Compaq with SMART data from CSS testing

Model #2 - Middle of the Road

Pros
The addition of MKE pre-pro data gathering provides the peace of mind that marginal drives will not fail SMART straight out of the factory. The same data may show that the thresholds can be set tighter than what is possible without the data.

Cons
Need resources to collect, graph, and analyze the information. May or may not need additional head count for this.

Activities

- Pass Functional Test
- Pass Feature Test
- Get large statistical samples at MKE pre-pros
- Select thresholds with tighter margins
- Provide Compaq with SMART data from CSS testing

Model #3 - The Works

Pros

Provides the most comprehensive data gathering and analysis effort for SMART. If Failure Creation Lab is staffed, it can serve as the SMART engineering knowledge center, consulting multiple development teams on setting tight thresholds. The effort put into developing SMART can be used to really understand the drive failure mechanism.

Cons

Requires up to three engineers or technicians for performing Failure Acceleration Testing for products in development and possibly failure analysis of drives at the Repair Center.

Activities

- Pass Functional Test
- Pass Feature Test
- Get large statistical sample at MKE
- Analyze DVT data
- Perform Failure Acceleration Testing
- Select the tightest thresholds possible
- Provide Compaq with SMART data from Failure Acceleration Testing
- Provide Compaq with SMART data from CSS testing
- Failure analysis at the Repair Center

And The Envelop, Please...

Due to the lack of additional resources, DPSG engineering management has decide to implement the Bare Bones model. Compaq has agrees to wait for data collected from the field before changing any thresholds; this process can take up to two years. So in the mean time, all parties are happy with the current Phase 4 implementation.

SMART Development Process

By Kevin Tso

(For Quantum internal distribution only)

History

In early 1994, Compaq handed Quantum an interface spec. for a feature that is known today as SMART. At the same time they handed us the spec., Compaq asked to put this feature into products that were already in mass production, and to put additional functionality into products that are in development at the time. This customer-generated pressure sets the tone for SMART development at Quantum today.

The phases described below are Quantum internal groupings. The concept is that newer products do not implement a lower phase than the current one in production. This is done to fulfill Compaq's requirement that predictability increase over time across products.

Name

SMART stands for Self-Monitoring Analysis Reporting Technology, and is the name used all around the industry today.

In the beginning, it had many names. The following are a few:

DPA - Drive Parameter Analysis (Quantum Milpitas internal name)
EWS - Early Warning System (Quantum Shrewsbury internal name)
DFP - Drive Failure Prediction (Compaq)
PFA - Predictive Failure Analysis (IBM)

Phase 1

A few early prototypes were put together on the Maverick product for Compaq. The SMART feature on these drives were mock-ups only.

Phase 2

Maverick, RoadRunner, and Lightning were retrofitted with CSS, power cycles, power-on hours, and grown-defect list counters. Only the grown-defect list is warrantiable. These attributes were chosen because they were easy to implement and were well understood.

Phase 3

Fireball and TrailBlazer installed the previous attributes and additionally triple-burst corrected error rate, seek error rate, spin-up time, and recal-retry count. Initially, we were only willing to put in spin-up time, but Compaq insisted on more. These attributes were chosen because they make common sense.

Phase 3.5

The Internal Compare command was added to Fireball and TrailBlazer to allow the drive to return a simple pass/fail status. All mass-production level unit for Fireball and TrailBlazer contain SMART Phase 3.5. Sirocco is also implementing to this level.

Phase 4

If we had started the research for Phase 4 at the time we started developing Phase 3, we probably would have an attribute that is more predictive than Raw Error Rate. However, due to the need to work on Phase 2 and 3 at the same time, and concurrently develop an interface protocol, we neglected starting the Phase 4 research

The decision to use Raw Error Rate is based on the premise that it is more effective than the Triple-Burst Error Rate attribute used in Phase 3.

The raw error rate is additionally implemented in Vortex and Tempest. Due to the need to sample all areas on the drive, this attribute required the off-line mode operation to be defined and implemented. Stratus, Cyclone, and Saguaro will also implement this phase.

Phase 5

APE and ART have agreed to develop the "signal quality monitor" as a potential attribute for Phase 5. There are currently no products designated as Phase 5.

Organizational Structure

DPA Core Team (former)

This group was established in the early days to oversee the SMART development. It was the SMART connection to Compaq, representing the overall Quantum. However, as time went on, development teams were confused as to who has the responsibility to develop SMART. Also, it was difficult, if not impossible, to represent all development teams in front of a customer. Due to these reasons, the DPA Core Team was disbanded, and SMART development responsibility returned to the development teams.

SMART Steering Committee

John Levy (leader), John Squire, Rick Brown, Dennis Hollenbeck, Dave Sutton, and Rob Strieby are part of this committee. It oversees the overall direction of SMART and allocates resources if necessary. Disbanded

SMART Strategy Team

Dave Tang (Strategic Marketing, leader), Kevin Tso (Systems Engineering), Larry Toombs (Failure Creation Lab), Seed Foudeh (ART), Gaylon Lovelace (APE), and Sid Sigh (Quality) are members of the Strategic Team. The mission of this team is to oversee the operation of future SMART development, and feedback data from field returns. Disbanded

SMART Exchange

Formerly named the Phase 4 Coordination Team, this body coordinates leveraging across development teams and provide supporting tools. The name was changed from the Coordination Team to the SMART Exchange to emphasize the fact that this is not a body to issue and monitor specific tasks. Each development team should develop their own expertise and determine their own activities and schedules. SMART Exchange will get the teams together to exchange information, so there is a common understanding, resulting in a common philosophy and implementation. I am the leader of the SMART Exchange.

Failure Creation Lab (FCL)

The original concept is to have an actual department, complete with two to four technicians and lab equipment to support the threshold determination activities in all development team. Each development team still must provide their own coordinator, who will help the Failure Creation Lab define tests. The job of selecting thresholds still rests with each development team. The Failure Creation Lab is there to provide test equipment and resources.

However, due to limited budget, upper management is unable to provide the staffing, so FCL is still a virtual lab right now.

From past experience in dealing with Compaq, it is likely that they will ask for data verifying the effectiveness of the SMART feature. Specifically, Compaq will be very interested in seeing data for the Phase 4 Raw Error Rate attribute. If the FCL is not going to be a reality, the functions perform by FCL need to done somewhere. The risk of not doing any effectiveness study is the chance of upsetting Compaq.

Feature Development Philosophy

The Steering Committee is finally pondering the big question: what is the goal of developing SMART? Up until now the answer was vague. We were marching to the beat of full support for SMART, but without necessary resources allocated. Now the issue is on the table. Because the Steering Committee is faced with a hefty resource requirement, it is re-evaluating the goal of SMART. The current question is whether we can satisfy the customer, namely Compaq, without expending extra resources. This would probably mean setting conservative thresholds that still show some experimental effectiveness.

Feature Development Process

There are several steps in developing SMART. In summary they are:

1. Define specification
2. Firmware development
3. Firmware functional testing
4. Firmware feature testing
5. Get large statistical reading from MKE builds

6. Failure acceleration testing
7. DVT data gathering
8. Threshold determination
9. Field data feedback

Define Specification

Compaq has been the main driving force in our effort to gain additional predictiveness. Interface specifications usually are first drafted by Compaq and refined by Quantum. However, selection of the attributes is defined by Quantum.

Inside Quantum, Systems Engineering is responsible for the consistent definition of the feature. Product Engineering and APE have assisted or is assisting in attribute selection. Strategic and Technical Marketing has played a part in bringing the specification to the industrial standards committees.

We normally define SMART in terms of phases. In each phase, the feature is implemented similarly across products. One desire is to not regress on phases, meaning that once a product has gone on a new phase, later products will not go back to a previous phase. This is to satisfy Compaq's requirement that predictability increase over time. Currently we are implementing Phase 4 and researching Phase 5.

At the end of this process, a Feature Specification is generated. This is a Quantum-internal engineering document stating fully the functionality of the feature.

Firmware Development

Usually a lead team will develop the initial firmware, then the other teams will leverage the firmware. This has worked well when the microprocessor in use is the same. There had been cases where the difference in microprocessor caused firmware bugs during the code port. This problem can also be attributed to a lack of complete feature specification, and lack of thorough firmware testing in earlier phases.

Firmware Functional Testing

Compatibility Test Engineering is responsible for developing the Functional Test. This test covers the basic workings of the feature. It checks all the commands, verifying that they return the proper data. It checks the status flags to make sure that they reflect the proper status.

Firmware Feature Testing

Systems Engineering is responsible for developing the Feature Test. This is a more in-depth test that verifies that the firmware is indeed counting what it is suppose to be counting. System Engineering standardized a test interface to all the products in Phase 4. Although the software is developed by Systems Engineering, each firmware group is expected to run this software and debug their own firmware.

Get Large Statistical Readings

In order to feel safe about the feature, some development teams gather SMART information during MKE pre-production builds. During digital scan, the drives are put into a special mode, in which sample sizes are set to the maximum possible, and SMART data collected as part of the normal run. A few hundred drives are involved, and the Test Process group assisted in collecting and analyzing the data.. This data gives the mean, standard deviation, lower bound, and upper bound for each attribute. The information is used later to determine a safe threshold.

DVT Data Gathering

Because the main goal of DVT is to verify drive functionality, and not SMART functionality, some of the tests do not go the extreme conditions that are needed for determining SMART thresholds. Q/R has agreed to gather SMART data during testing for Phase 4 products. The specific tests involved were: 4-Corners, Strife, and CSS. In the past, Compaq has shown interest in obtaining SMART data from the CSS test.

Failure Acceleration Testing

The extreme conditions that cannot be reached in DVT are applied here. Specific tests are designed for SMART threshold determination. In Phase 3, these tests have included: Variable Voltage On Spin-Up, Non-operating Shock, Operating Vibration, and Operating Thermal. Phase 3 results have shown, that under some conditions, SMART is effective in predicting drive failures.

In Phase 3, failure acceleration tests are designed by Systems Engineering in conjunction with Scott Shellard's Failure Analysis group.

With Phase 4, the test design responsibility is supposed to rest in each development team, working in conjunction with the Failure Creation Lab. The execution of the tests is supposed to be the responsibility of the Failure Creation Lab. However, due to the Failure Creation Lab not getting any resources, Failure Acceleration Testing may have to be skipped, or done by each individual development team.

Compaq has been adamant about pushing Quantum to obtain data that shows SMART is effective in experimental tests. Specifically, Compaq wanted to see, in the long-term CSS testing, that SMART is effective in predicting spin-up and read/write failures. There is reason to believe that Compaq will be demanding the same or more test data for Phase 4 products.

Thresholds Determination

There are two things that we are looking for in determining thresholds:

- The threshold is safe for drives in good condition
- The threshold is effective for drives in deteriorating condition

The Threshold Is Safe

Analyzing the statistical data from MKE pre-production builds, each development team will initially select a threshold that is safe for drives in good condition.

The Threshold Is Effective

Taking data from DVT and Failure Acceleration Testing, each development team will incrementally advance the thresholds such that they will predict drive failure.

Threshold Determination Process

Generally the process involved in setting a threshold is as follows:

- Determine the worst error rate the drive can tolerate before giving up. This is usually several orders of magnitude away from the drive specification
- Select this as the initial threshold
- Run Failure Acceleration Tests to prove or disprove the effectiveness of the selected threshold
- If effectiveness is disproved, make decision to stay put, or select a more aggressive threshold
- Re-run tests with failure accelerators
- Select final threshold

It is appropriate for each development team to have a person responsible for selecting the threshold. The specific condition on a product can only be focused on by someone in the development team. This person needs to be aware of all data gathering operations and coordination all activities in selecting thresholds for his particular product.

Field Data Feedback

Currently the Strategy Team is working with the Repair Center to collect SMART data on drives returned from the field. At this moment, no data is available due to few Fireballs and TrailBlazers returned with SMART being turned on. The uncertainty of condition of drives return from the field is another problem. Many drives are returned without proper packaging, and damage has been incurred during transit. This makes verifying SMART functionality difficult. It is wise that we either perform some form of ORT testing, or periodically do failure analysis on SMART drives in the Repair Center.

SMART Threshold
Safety and Effectiveness Studies

By Kevin Tso

(For internal distribution only)

Many tests were conducted to examine the safety of the Phase 3 and 3.5 attributes. The initial agreement with Compaq was to set conservative thresholds and collect data for analysis only. In fact, Ken Bush of Compaq suggested not setting any thresholds at all and only collect data. However, subsequently Compaq reversed their stand and wanted Quantum to prove SMART's effectiveness. That request sent us into a mad scramble to conduct new tests. Even today, our understanding rests mainly with making the thresholds safe.

Prove the Safety of the Thresholds

The following tests were done to prove the safety of SMART thresholds.

STRIFE

SMART data was collected from Fireball drives in the STRIFE test. Data showed that drives with known bad heads failed SMART under conditions beyond spec. (5 degrees C). We concluded that SMART was safe for normal drives operating under normal conditions.

4-Corners

SMART data was collected from Fireball drives in the 4-Corners test. Very cold conditions (0 degrees C) causes some drives with known bad heads to exceed SMART thresholds. We concluded that SMART was safe for normal drives operating under normal conditions.

Spin-Up Time Under Voltage and Current

Tests conducted on Fireball and TrailBlazer indicated that differences in voltage and current do not significantly alter spin-up time.

Operating Vibration

The TrailBlazer was tested in very high G conditions to evaluate SMART's sensitivity to vibration. Thresholds were not exceeded even for conditions exceeding the product spec.

RoadRunner CSS Test

CSS results from the RoadRunner product gave us a profile of spin-up time as the drives go through CSS cycles. Drives exhibited varying spin-up characteristics over time, some reaching 8 seconds at about 60,00 cycles. We concluded that our selected threshold was safe at 10 seconds.

Repair Center Data

One hundred RoadRunner drives were intercepted and examined upon return to the Repair Center. Data shows that only drives with gross problems (excessive run-out or dead head) can potentially cross the SMART thresholds. Note that RoadRunner drives don't have the Read and Seek Error Rate attributes, so data collected is only an approximation of what SMART will see.

Prove the Effectiveness of the Thresholds

The following tests were conducted to evaluate the effectiveness of SMART thresholds. We plotted host-seen errors against SMART measurements. Failure predictability was defined as SMART attributes crossing their thresholds before host-seen errors occur.

Non-Operating Shock and Operating Vibration

Two Fireball drives were put into the destructive tests. Data shows that the Triple-Burst Error Rate attribute was not an effective predictor of read errors.

Cold Test

SMART measurements from Fireball DVT tests were plotted against unrecoverable failures. The conclusion was that the Triple-Burst Error Rate was not an effective predictor of read errors.

CSS Test

Spin-up time data was collected from the SCSI Fireball CSS tests. The data was collected from the host software, not from SMART because SMART is not implemented on SCSI products. There were several drives with known stiction problems which exhibited excessive spin-up time. We postulated that if SMART was implemented, it would correctly indicate the elevated spin-up time. However, due to the sample size being set too large, the threshold would not have crossed before drive failure.

Subsequent CSS tests were conducted with IDE drives and with SMART turned on. I don't know the results of those tests.

Heat and Voltage Test

TrailBlazer drives were put into a chamber and applied incremental heat and voltage. The drives were allowed to soak at conditions beyond spec. to accelerate aging. The result of this test indicated that the Seek Error Rate is an effective predictor of servo failures. Interestingly, the servo system tries to recover from positional problems, but does not warn the host of this effort. SMART effectively served as the warning indicator for excessive servo retries.

Notes

Product Manual

Quantum®

Quantum Vortex 1275/2550 AT
Preliminary Product Manual

DRAFT
DATE 12-21-95

DRAFT
DATE 12-21-95

November 1995
81-XXXXXX-01

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Chapter 1
ABOUT THIS MANUAL

This chapter gives an overview of the contents of this manual, including the intended audience, manual organization, and terminology and conventions. In addition, it provides a list of other references that might be helpful to the reader.

1.1 AUDIENCE DEFINITION

Quantum Vortex 1275/2550AT product manual is intended for several audiences including the original equipment manufacturer (OEM), distributor, installer, and end user. The manual provides you with information about installation, principles of operation, interface command implementation, and maintenance.

1.2 MANUAL ORGANIZATION

This manual provides information about installation, principles of operation, and interface command implementation. It is organized into the following chapters:

- Chapter 1—About This Manual
- Chapter 2—General Description
- Chapter 3—Installation
- Chapter 4—Specifications
- Chapter 5--Basic Principles of Operation
- Chapter 6—IDE-Bus Interface and ATA Commands

In addition, this manual contains a glossary of terms and an index to help you locate important information.

1.3 TERMINOLOGY AND CONVENTIONS

The abbreviations listed below are used in this manual. You can find definitions of the following terms in the Glossary at the back of this manual.

- bpi Bits per inch
- dB Decibels
- dBA decibels, A weighted
- fci Flux changes per inch
- Hz Hertz
- KB Kilobytes
- lsb Least-significant bit
- mA Milliampere

- MB — Megabytes (1 MB = 1,000,000 bytes when referring to disk storage, and 1,048,576 bytes in other cases)
- m — Meter
- Mbit/s — Megabits per second
- MB/s — Megabytes per second
- MHz — Megahertz
- ms — Millisecond
- msb — Most-significant bit
- mV — Millivolts
- ns — Nanoseconds
- tpi — Tracks per inch
- µs — Microseconds
- V — Volts

The following conventions are used in this manual:

- **Commands and Messages**

  Commands, status or error messages, sent between the drive and the host, are listed in all capitals. For example:

  WRITE LONG
  ABORTED COMMAND

- **Parameters**

  Parameters are given as initial capitals when spelled out and as all capitals when abbreviated. For example:

  Prefetch Enable, PE
  Cache Enable, CE

- **Names of Bits and Registers**

  Bit names and register names are presented in initial capitals. For example:

  Host Software Reset
  Alternate Status Register

- **Hexadecimal Notation**

  The hexadecimal notation "H" is given in subscript form. For example:

  30_H

- **Register Names:** ← REMOVE COLON

  Registers are given in this manual with initial capitals. An example is the Alternate Status Register.

- **Signal Negation**

  A signal name that is defined as active low is listed with a minus sign following the signal. For example:

  RD–

- Notes

  Notes are used after tables to provide you with supplementary information.

- **Host**

  In general, the system in which the drive resides is referred to as the host. The AT/IDE host adapter is considered to be part of the host.

- **Computer Voice:** This refers to items you type at the computer keyboard. These items are listed in 10-point, all capitals, courier font. An example is `FORMAT C:/S.`

1.4 REFERENCES

For additional information about the AT interface, refer to:

- IBM Technical Reference Manual #6183355, March 1986
- ATA Common Access Method Specification, Revision 3, January 17, 1995
- Small Form Factor Specification for ATA Timing Extensions #8011, July 2, 1993

Chapter 2
GENERAL DESCRIPTION

This chapter summarizes general functions and key features of the Quantum Vortex™ 1275/2550AT hard disk drive, as well as the applicable standards and regulations it meets.

2.1 PRODUCT OVERVIEW

Quantum's Vortex 1275/2550AT hard disk drives are part of a family of high-performance, 19 mm-high (0.75 in), hard disk drives manufactured to meet the highest product quality standards. Vortex 1275/2550AT hard disk drives use nonremovable, 130 mm (5 1/4-in) hard disks. These drives can be used in IBM® PC/AT-compatible host computer systems, which provide an AT Attachment (ATA) Interface either on an adapter board or on the system motherboard.

Note: Sometimes, the ATA Interface is referred to as the *AT Bus* or *IDE Interface.*

Vortex 1275/2550AT hard disk drives feature an embedded IDE drive controller and use ATA commands. The drive manages media defects and error recovery internally, so these operations are transparent to the user.

The innovative design of Vortex 1275/2550AT hard disk drives enables Quantum to produce a family of low-cost, high-reliability drives.

2.2 KEY FEATURES

Vortex 1275/2550AT hard disk drives include the following key features:

General

- Formatted storage capacity of 1275 MB (1 disk), or 2550 MB (2 disk)
- Industry-standard, 130 mm (5 1/4-in) form factor
- Low-profile, 19 mm (0.75 in), height
- Emulation of IBM® PC/AT® task file register and all ATA fixed-disk commands
- Embedded servo design
- Fast ATA-2 support

Performance

- Data transfer rate of up to 8.33 MB/s, using programmed I/O (PIO), 16.67 MB/s using PIO with IORDY, 16.67 MB/s using multiword DMA Mode
- Average seek time of 15.5 ms
- Average rotational latency of 8.33ms
- 1:1 interleave on read/write operations
- 128K buffer with 76K dynamic segmentation cache. Look-ahead DisCache ® feature with continuous prefetch, and WriteCache™ write-buffering capabilities
- Support for all ATA data transfer modes with PIO Mode 4 and multiword DMA mode 2
- Auto Write, Auto Read, and Auto Transfer

Reliability

- Power-Up Self diagnostic firmware
- 160-bit, interleaved Reed-Solomon Error Correcting Code (ECC), with cross-checking and double- and triple-burst correction for bursts up to 72bits in length
- Double-burst ECC correction on-the-fly
- 300,000 hour Mean Time Between Failure (MTBF) in the field
- Automatic retry on read errors
- 20,000 Contact Start/Stop cycles (controlled)
- Transparent media-defect mapping
- Reassignment of defective sectors discovered in the field, without reformatting
- High-performance, in-line defective sector skipping
- Patented AIRLOCK® automatic shipping lock and dedicated landing zone
- Failure prediction

Versatility

- Power-saving modes
- Downloadable firmware
- Cable select feature
- Ability to daisy-chain two drives on the interface
- Multi-Sector Auto Read and Multiple Auto Write transfer
- LBA mode addressing/Extended CHS mode

2.3 STANDARDS AND REGULATIONS (Pending)

Vortex 1275/2550AT hard disk drives satisfy the following standards and regulations:

- Federal Communications Commission (FCC): FCC Rules for Radiated and Conducted Emissions, Part 15, Sub Part J, for Class B Equipment in an enclosure.
- Underwriters Laboratory (U.L.): Standard 1950. Information technology equipment including business equipment.
- Canadian Standards Association (CSA): Standard C22.2 No. 950. Information technology equipment including business equipment.
- European Standards – Verband Deutscher Electroechnier (VDE) DIN VDE 0805-5.90 and Technisher Uberwachungs Verein (TUV): Standard EN 60 950 (IEC 950). Information technology equipment including business equipment in an enclosure.

Note: The Standards and Regulations information is pending

Chapter 3
INSTALLATION

This chapter explains how to unpack, configure, mount, and connect the Vortex 1275/2550AT hard disk drive prior to operation. It also explains how to start up and operate the drive.

3.1 SPACE REQUIREMENTS

Quantum ships the Vortex 1275/2550AT hard disk drive without a faceplate. Figure 3-1 shows the external dimensions of the drive.

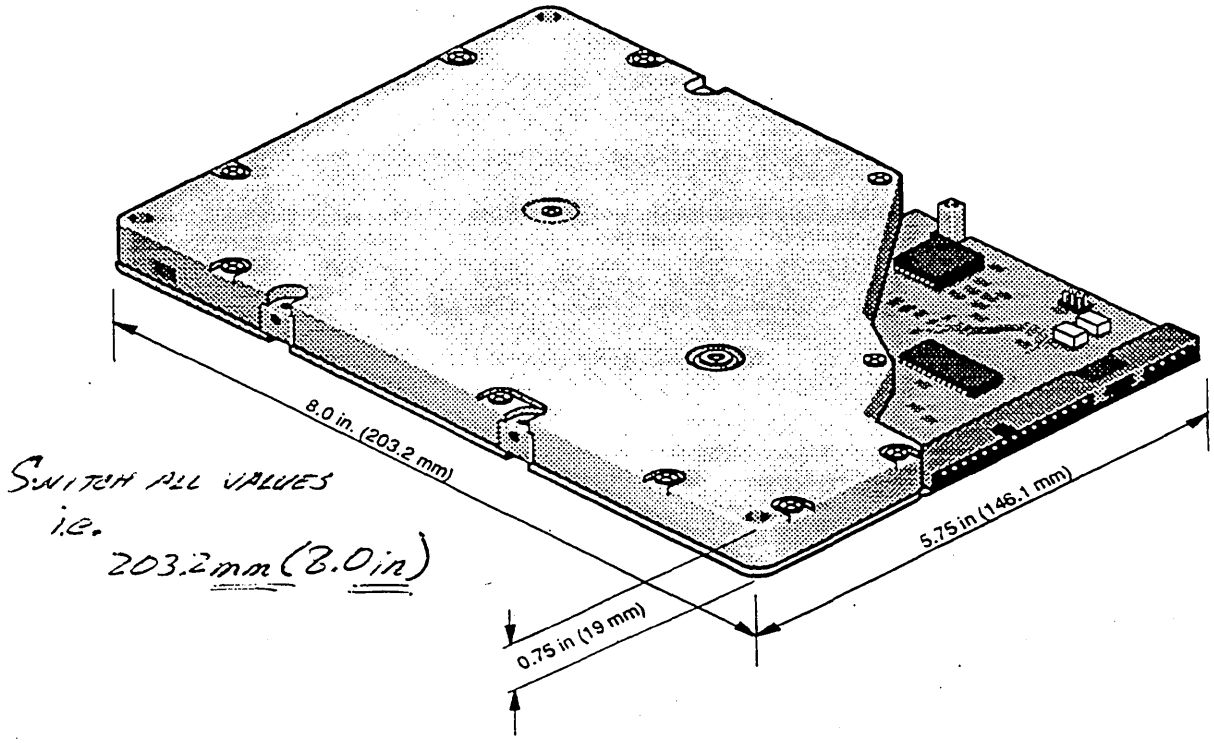


Figure 3-1 *Vortex 1275/2550AT Mechanical Dimensions*

3.2 UNPACKING INSTRUCTIONS

CAUTION: The maximum limits for physical shock can be exceeded if the drive is not handled properly. Special care should be taken not to bump or drop the drive.

1. Open the shipping container.
2. Remove the upper protective packaging pad from the box.

   Figure 3-2 shows the packaging for the Vortex 1275/2550AT hard disk drive in a 1-pack shipping container. (A 12-pack shipping container is available for multiple drive shipments and has the same type of protective packaging.)

3. Remove the drive from the box.

CAUTION: During shipment and handling, the drive is packed in an antistatic electrostatic discharge (ESD) bag to prevent electronic component damage to ESD sensitive devices. Remove the drive from the ESD bag only when you are ready to install it. To avoid accidental damage to the drive, do not use a sharp instrument to open the ESD bag.

4. Save the packaging materials for possible future use.

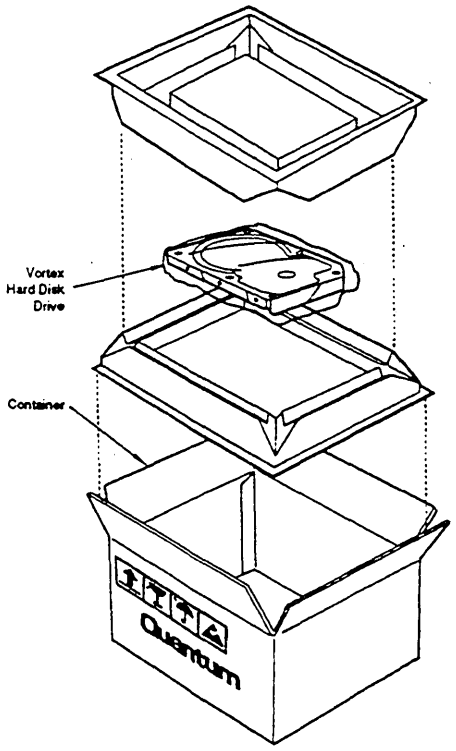


Figure 3-2 *Packaging for a 1-Pack Shipping Container*

3.3 JUMPER SETTINGS

The configuration of a Vortex 1275/2550AT hard disk drive depends on the host system into which it is to be installed. This section describes the jumper setting options you must take into account prior to installation. Figure 3-3 shows the printed circuit board assembly (PCBA), including the location of the jumpers that control some of these options.

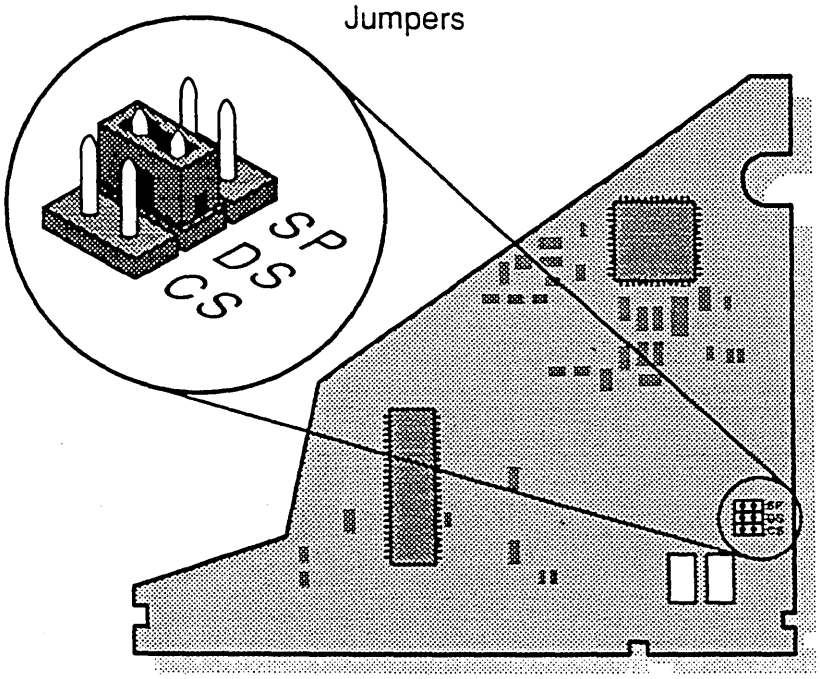


Figure 3-3 *Jumper Locations on the Drive PCBA*

The configuration of three jumpers controls the drive's mode of operation:

- CS—Cable Select
- DS—Drive Select
- SP—Slave Present

Table 3-1 defines the jumper configurations for the drive and the operational modes that result from the configurations. A "1" indicates that the specified jumper is installed; a "0", that the jumper is not installed.

Table 3-1 *Vortex 1275/2550AT Jumper Options*

CS	DS	SP	DESCRIPTION
0	0	0	Slave Drive Compatible with drives using the PDIAG– line to handle Master/Slave communications.
0*	1*	0*	Master Drive Uses DASP– to check for the presence of a Slave.
0	1	1	Master Drive Uses the SP jumper to determine whether a Slave is present, without checking PDIAG– or DASP–.
1	X	X	Slave or Master Drive, depending on the state of the Cable Select signal (pin 28) at the IDE-bus interface connector. If the signal state is set to 0 (grounded), then the drive is configured as if DS were 1, described above. If the Cable Select signal is set to 1 (high), then the drive is configured as if DS were 0, described above.

Note: In Table 3-1, a 0 indicates that the jumper is removed, a 1 indicates that the jumper is installed, and X indicates the jumper setting does not matter. An asterisk (*) indicates the factory default setting.

3.3.1 Drive Select (DS) Jumper

You can configure two drives on the ATA Interface as Master (Drive 0) and Slave (Drive 1) using the DS jumpers. Set the CS jumpers to 0 for each drive. Then, set the DS jumper to 1 on one drive to configure that drive as Master. Set the DS jumper to 0 on the other drive to configure that drive as Slave.

Quantum ships Vortex 1275/2550AT hard disk drives from the factory with the DS jumper installed—that is, the DS jumper is set to 1 to configure the drive as Master. To configure a drive as the Slave, set the DS jumper to 0.

Note: For drives configured using the DS jumper, the order in which drives are connected in a daisy chain has no significance.

3.3.2 Cable Select (CS) Jumper

When two Vortex 1275/2550AT hard disk drives are daisy-chained together, they can be configured as Master and Slave by using the CS jumper or by using the DS jumper— but not both. To configure the two drives using the CS jumper, set the CS jumper to 1 (installed) and the DS jumper to 0 (uninstalled) on each drive.

Once you install the CS jumper, the drive is configured as a Master or Slave by the state of the Cable Select signal, which is pin 28 at the IDE-bus interface connector. According to the ATA (AT Attachment) specification referred to in Section 1.4, pin 28 may be used for either Cable Select or spindle synchronization. Quantum uses the pin 28 Cable Select function but does not implement the spindle synchronization function.

Pin 28 is grounded—that is, set to 0—on the cable coming from the host. This configures the first drive as Master. Then, pin 28 on the connector at the second drive should be made an open circuit by a cut in signal line 28 in the cable from the first drive, so it becomes high—that is, set to 1—due to a pull-up in the second drive. This configures the second drive as Slave.

3.3.3 Slave Present (SP) Jumper

The SP jumper normally is not needed. However, when the Vortex 1275/2550AT is configured as Master and is connected to a Slave drive that does not implement the Drive Active/Slave Present (DASP–) signal, it is necessary to set the SP jumper to 1 on the Vortex 1275/2550AT hard disk drive.

3.4 IDE-BUS ADAPTER

There are two ways you can configure a system to allow the Vortex 1275/2550AT hard disk drive to communicate over the IDE-bus of an IBM or IBM-compatible PC:

1. Connect the drive to a 40-pin IDE-bus connector (if available) on the motherboard of the PC.

2. Install an IDE-compatible adapter board in the PC and connect the drive to the adapter board.

3.4.1 40-Pin IDE-Bus Connector

Many of the later design PC motherboards have a built-in 40-pin, IDE-bus connector that is compatible with the 40-pin IDE interface of the Vortex 1275/2550AT hard disk drive. If the motherboard has an IDE connector, simply connect a 40-pin ribbon cable between the drive and the motherboard.

You should also refer to the motherboard instruction manual and refer to Chapter 6 of this manual to ensure signal compatibility.

3.4.2 Adapter Board

If your PC motherboard does not contain a built-in, 40-pin IDE-bus interface connector, you must install an IDE-bus adapter board and connecting cable to allow the drive to interface with the motherboard. Quantum does not supply such an adapter board, but they are available from several third-party vendors.

Please read over carefully the instruction manual for the adapter board you purchase as well as Chapter 6 of this manual to ensure signal compatibility between the adapter board and the drive. Also, make sure that the adapter board jumper settings are appropriate.

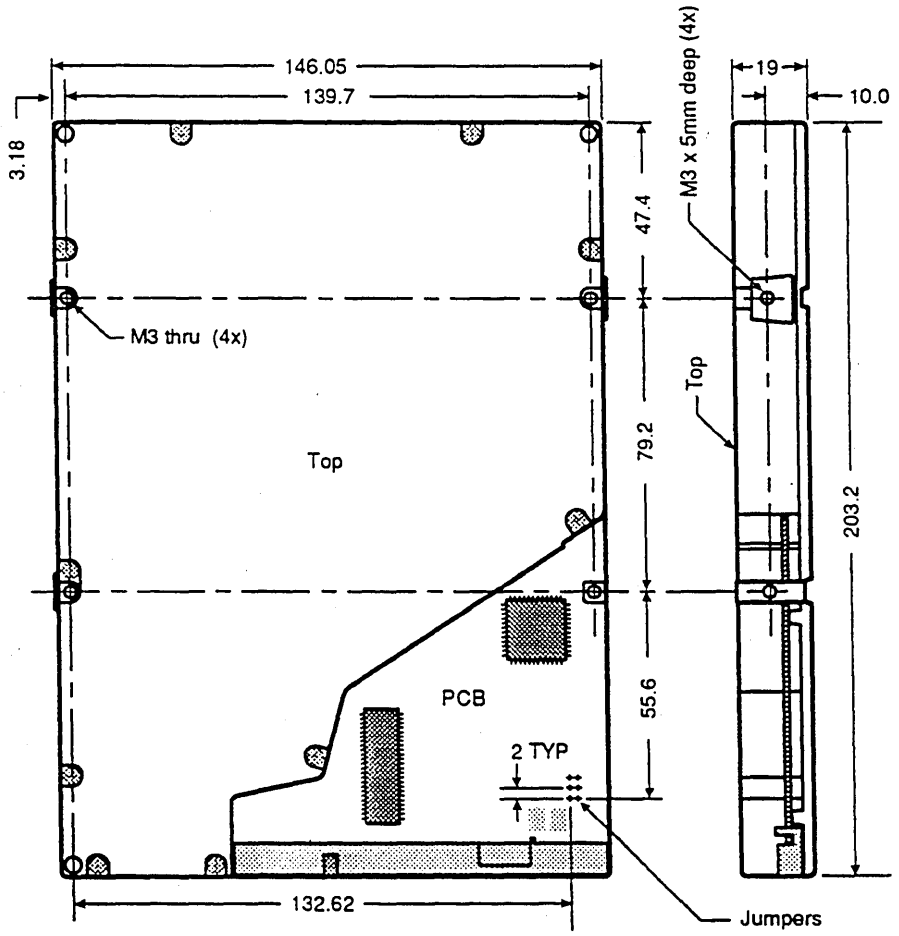
3.5 MOUNTING

Drive mounting orientation, clearance, and ventilation requirements are described in the following subsections. For mounting, M3 screws are recommended. To avoid stripping the mounting-hole threads, the maximum torque applied to the screws must not exceed TBD ~~inch-pounds~~.

5 kg-cm

3.5.1 Orientation

The mounting holes on the Vortex 1275/2550AT hard disk drive allow the drive to be mounted in any orientation.



PUT ALL VALUES WITH SAME DECIMAL PT. FORMAT i.e. X.XX

Figure 3-4 *Vortex 1275/2550AT Mounting Dimensions (in Millimeters)*

3.5.2 Clearance

The printed-circuit board assembly (PCBA) is very close to the mounting holes. Clearance from the drive to any other surface—except mounting surfaces—must be 1.25 mm (0.05 inches) minimum. Figure 3-5 specifies the clearance between the screws in the mounting holes and the PCBA. Do not use mounting screws longer than the maximum lengths specified in Figure 3-5. The specified screw length allows full use of the mounting-hole threads, while avoiding damaging or placing unwanted stress on the PCBA.

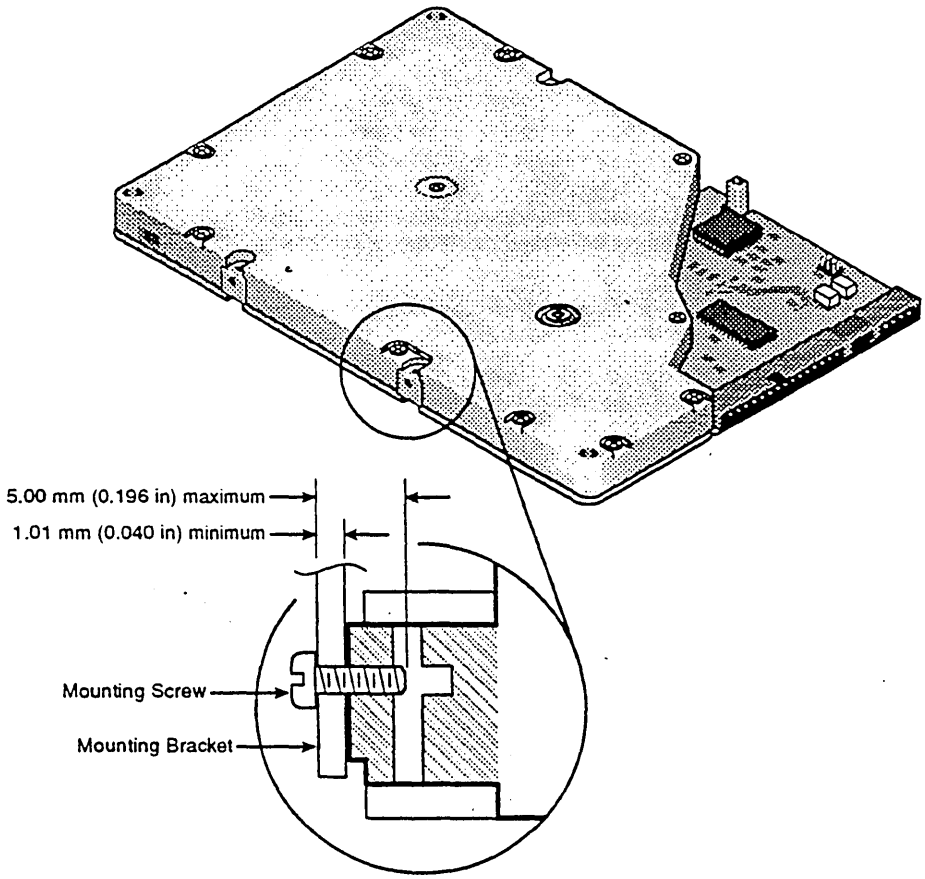


Figure 3-5 *Mounting Screw Clearance*

CAUTION: The PCBA is very close to the mounting holes. Do not exceed the specified length for the mounting screws. The specified screw length allows full use of the mounting-hole threads, while avoiding damaging or placing unwanted stress on the PCBA. Figure 3-5 specifies the minimum clearance between the PCBA and the screws in the mounting holes. To avoid stripping the mounting-hole threads, the maximum torque applied to the screws must not exceed TBD inch-pounds.

3.5.3 Ventilation

The Vortex 1275/2550AT hard disk drive operates without a cooling fan, provided the ambient air temperature does not exceed 131°F (55°C).

3.6 COMBINATION CONNECTOR

As shown in Figure 3-6, there is a three-section combination connector mounted on the back edge of the PCBA. The drive's DC power can be applied to either the 3-pin or 4-pin connector. The IDE-bus interface uses section the 40-pin connector.

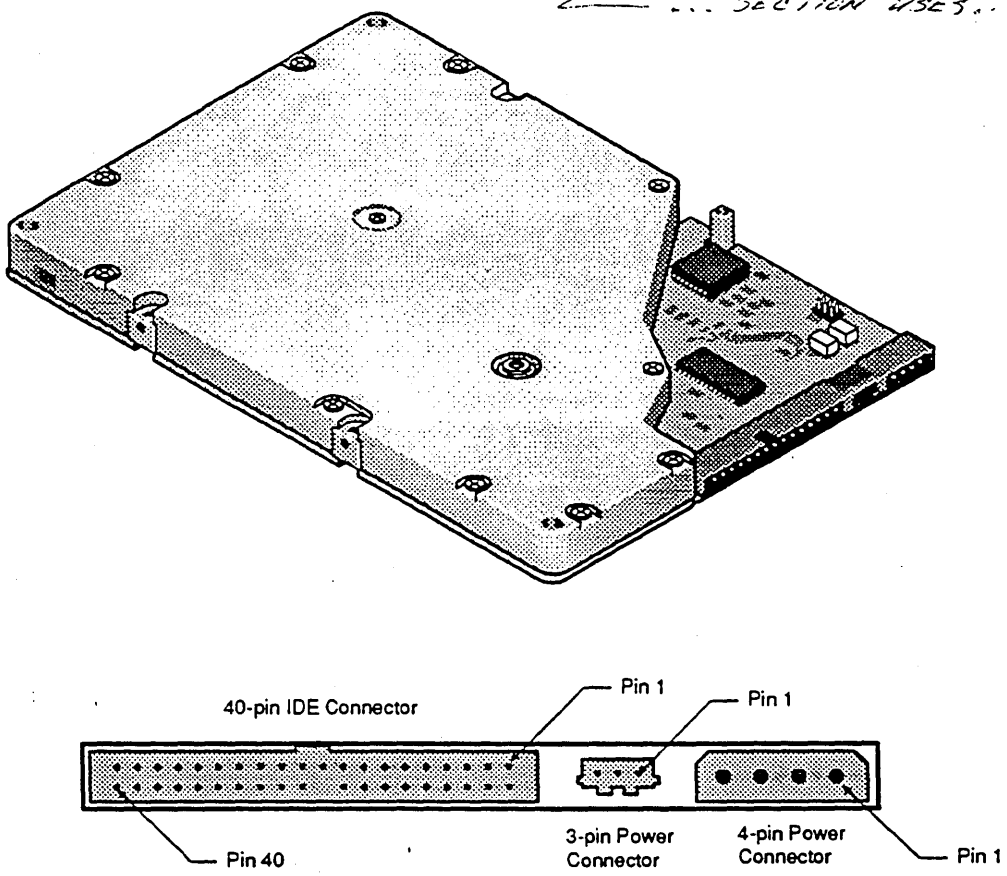


Figure 3-6 *DC Power and IDE-Bus Combination Connector*

3.6.1 DC Power

The recommended mating connectors for the +5 Vdc and +12 Vdc input power are listed in Table 3-2.

Table 3-2 *Power*

	PIN NUMBER	VOLTAGE LEVEL	MATING CONNECTOR TYPE AND PART NUMBER (OR EQUIVALENT)
4-Pin Connector	1	+12 Vdc	4-Pin Connector: AMP P/N 1-480424-0
	2	+12 Vdc Return (Ground)	Loose piece contacts: AMP P/N 61173-4
	3	+5 Vdc Return (Ground)	Strip contacts: AMP P/N 350078-4
	4	+5 Vdc	
3-Pin Connector	1	+5 Vdc	3-Pin Connector Molex P/N 39-01-0033
	2	+12 Vdc	Loose piece contacts: Molex P/N 39-00-00341
	3	Ground	Strip contacts: Molex P/N 39-00-0023

Note: Power can be applied to either the 3-pin or 4-pin connector. Labels indicate the pin numbers on the connector. On the 3-pin connector, pins 2 and 3 (the +5 and +12 Vdc returns) are connected on the drive.

3.6.2 IDE-Bus Interface Connector

On the Vortex 1275/2550AT hard disk drive, the IDE-bus interface cable connector is a 40-pin Universal Header, as shown in Figure 3-6.

See Chapter 6, "IDE-Bus Interface and ATA Commands," for more detailed information about the required signals. Refer to Table 6-1 for the pin assignments of the IDE-bus connector.

For mating with the 40-pin connector, recommended cable connectors include the following parts or their equivalents:

AMP receptacle with strain relief	P/N 1-499506-0
AMP receptacle without strain relief	P/N 1-746193-0

To key the 40-pin cable connector, you must plug the hole that corresponds to pin 20.

Other recommended part numbers for the mating connector include:

40-Pin Connector	3M 3417-7000 or equivalent
Strain Relief	3M 3448-2040 or equivalent
Flat Cable (Stranded 28 AWG)	3M 3365-40 or equivalent
Flat Cable (Stranded 28 AWG)	3M 3517-40 (shielded) or equivalent

3.7 DRIVE INSTALLATION

You can install the Vortex 1275/2550AT hard disk drive in an AT-compatible system in two ways:

3.7.1 For Systems With A Motherboard IDE Adapter

You can install the Vortex 1275/2550AT hard disk drive in an AT-compatible system that contains a 40-pin IDE-bus connector on the motherboard.

To connect the drive to the motherboard, use a 40-pin ribbon cable. Ensure that pin 1 of the drive is connected to pin 1 of the motherboard connector.

3.7.2 For Systems With An IDE Adapter Board

To install a Vortex 1275/2550AT hard disk drive in an AT-compatible system without a 40-pin IDE-bus connector on its motherboard, you need a third-party IDE-compatible adapter board.

3.7.2.1 Adapter Board Installation

Carefully read the manual that accompanies your adapter board before installing it. Make sure that all the jumpers are set properly and that there are no addressing or signal conflicts. Install the adapter board in your system according to the adapter board manual.

3.7.2.2 Connecting the Adapter Board and the Drive

Use a 40-pin ribbon cable to connect the drive to the board. See Figure 3-7. To connect the drive to the board:

1. Insert the 40-pin cable connector into the mating connector of the adapter board. Make sure that pin 1 of the connector matches with pin 1 on the cable.

2. Insert the other end of the cable into the header on the drive. When inserting this end of the cable, make sure that pin 1 of the cable connects to pin 1 of the drive connector.

3. Secure the drive to the system chassis by using the mounting screws, as shown in Figure 3-8.

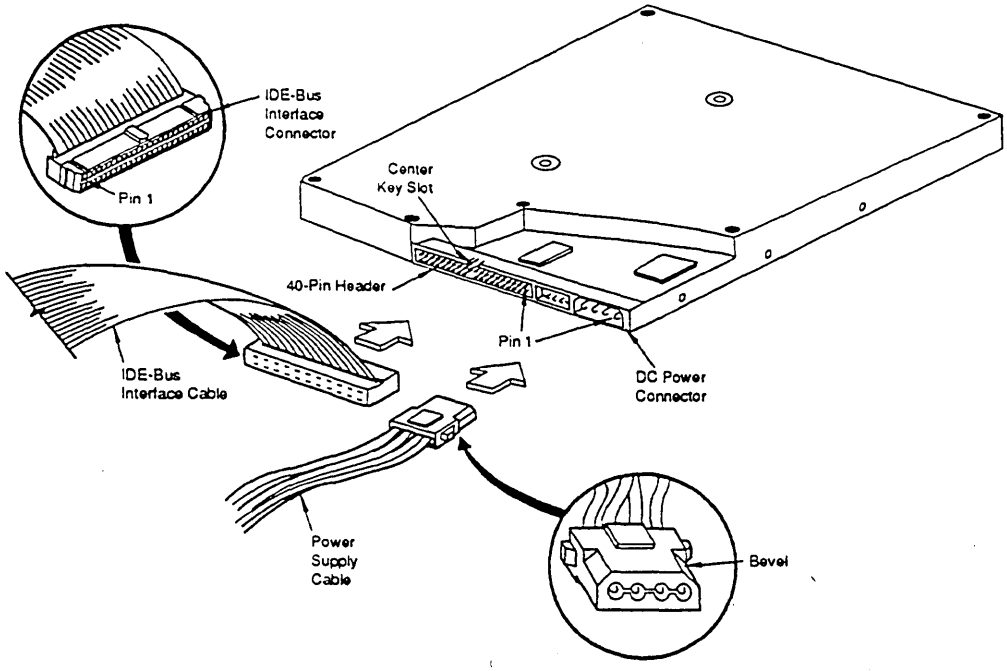


Figure 3-7 *Drive Power Supply and IDE-Bus Interface Cables*

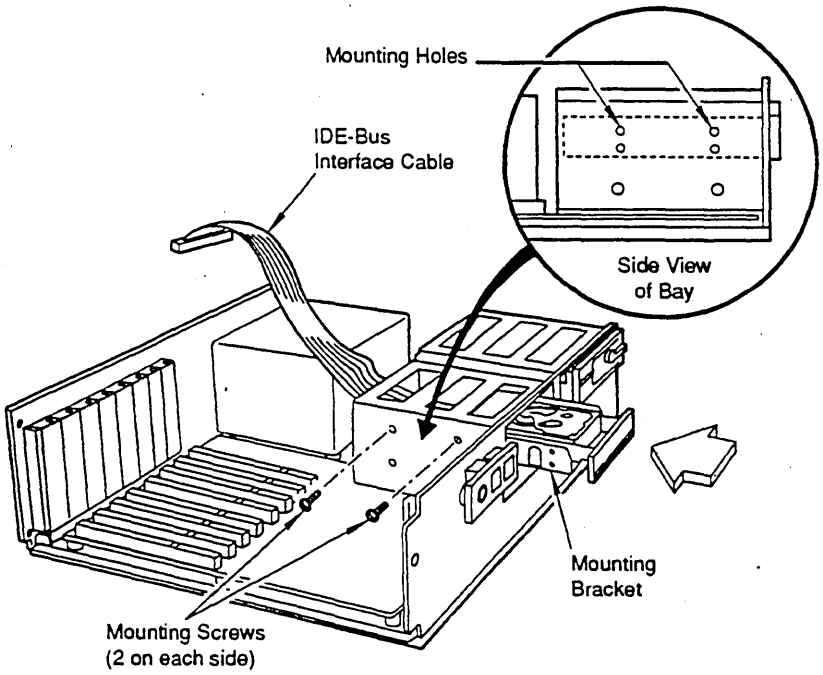


Figure 3-8 *Drive Installation*

3.8 SYSTEM STARTUP AND OPERATION

Once you have installed the Vortex 1275/2550AT hard disk drive and adapter board (if required) in the host system, you are ready to partition and format the drive for operation. To set up the drive correctly, follow these steps:

1. Power on the system.

2. Run the SETUP program. This is generally on a Diagnostics or Utilities disk, or within the system's BIOS.

   The SETUP program allows you to enter the types of optional hardware installed—such as the hard disk drive type, the floppy disk drive capacity, and the display adapter type. The system's BIOS uses this information to initialize the system when the power is switched on. For instructions on how to use the SETUP program, refer to the system manual for your PC.

3. Enter the appropriate parameters.

During the AT system CMOS setup, you must enter the drive type for the Vortex 1275/2550AT hard disk drive. This procedure allows the system to recognize the drive by translating its *physical* drive geometry parameters such as cylinders, heads, and sectors per track, into a *logical* addressing mode.

Vortex 1275/2550AT drives can work with different BIOS drive-type tables of various host systems. You can choose any drive type that does not exceed the capacity of the drive. Table 3-3 gives the logical parameters that provide the maximum capacity on Vortex 1275/2550AT hard disk drives.

Table 3-3 *Logical Addressing Format*

	Vortex 1275AT	Vortex 2550AT
Logical Cylinders	2492	4994
Logical Heads	16	16
Logical Sectors/Track	63	63
Total Number Logical Sectors	2,511,936	5,033,952
Logical Capacity	1,286,111,232	2,577,383,424

To match the logical specifications of the drive to the drive type of a particular BIOS, consult the system's drive-type table. This table specifies the number of cylinders, heads, and sectors for a particular drive type.

You must choose a drive type that meets the following requirements:

For the Vortex 1275AT
SCSI Logical Blocks x 512 = 1,286,576,128

For the Vortex 2550AT
SCSI Logical Blocks x 512 = 2,557,566,992

4. Boot the system using the operating system installation disk—for example, *MS-DOS*—then follow the installation instructions in the operating system manual.

If you are using a version of MS-DOS below 4.01:

1. Run FDISK or a third-party partitioning program.

Note: If you use DOS version 3.2 or an earlier version, the DOS partition will employ only 32 MB (33,554,432 bytes) of the drive's capacity. With DOS 3.3, you can partition the drive in multiples of 32 MB. If you use DOS 4.01 or later, or if you use a third-party partitioning program, you can create partitions that exceed 32 MB.

2. To format the drive with a high-level format and transfer the operating system to the drive, type `FORMAT C:/S`. Once this command executes, you can boot the system from the hard drive.

   You do not need to perform a low-level format on the drive because it was done at the factory before shipment.

Chapter 4
SPECIFICATIONS

This chapter gives a detailed description of the physical, electrical, and environmental characteristics of the Vortex 1275/2550AT hard disk drive.

4.1 SPECIFICATION SUMMARY

Table 4-1 gives a summary of the Vortex 1275/2550AT hard disk drive.

Table 4-1 *Vortex 1275/2550AT Specifications*

DESCRIPTION	Vortex 1275AT	Vortex 2550 AT
Capacity (formatted)	1286.57 MB	2577.55 MB
Nominal rotational speed (rpm)	3,600	3,600
Number of disks	1	2
Number of R/W heads	2	4
Data Organization		
Zones per surface	16	16
Tracks per surface	5,738	5,738
Total tracks	11,476	22,952
Sectors per track		
Inside zone	149	149
Outside zone	276	276
Total User Sectors	2,512,844	5,034,291
Bytes per sector	512	512
Number of tracks per cylinder	2	4
Recording		
Recording technology	Multiple Zone	Multiple Zone
Maximum linear density	113,922 fci	113,922 fci
Maximum Recording Density	107,221 (bpi)	107,221 (bpi)
Encoding method	PRML 16/17	PRML 16/17
Interleave	1:1	1:1
Track density	4,298 tpi	4,298 tpi
Effective areal density	460.84 Mbit/in^2	460.84 Mbit/in^2

Table 4-1 *Vortex 1275/2550AT Specifications (Continued)*

DESCRIPTION		Vortex 1275/2550AT
Performance		
Typical Seek times[1]		
Average seek		15.5 ms
Track-to-track		3.5 ms
Full stroke		30 ms
Sequential Head Switch		4.5 ms
Rotational Latency		8.33 ms
Data Transfer rate		
Disk to Read Buffer[2]		46.5 to 83.8 Mb/s[3]
Read/Write Buffer to IDE-bus (PIO Mode)	Without IORDY	8.33 MB/s max.
	With IORDY	16.67 MB/s max.
Read/Write Buffer to IDE-bus (DMA Mode)		16.67 MB/s max.
Buffer size (The upper 32K is used for firmware)		128 KB
Projected MTBF		300,000 hrs
Contact Start/Stop Cycles[4]		20,000
Auto head-park method		AirLock

1. Seek times are at nominal conditions and include settling.
2. Disk to read buffer transfer rate is zone-dependent.
3. Megabits per second.
4. CSS specifications assume a duty cycle of one power off operation for every four idle spin-down.

4.2 FORMATTED CAPACITY

At the factory, the Vortex 1275/2550AT receives a low-level format that creates the actual tracks and sectors on the drive. Table 4-2 shows the capacity resulting from this process. For operation with DOS, UNIX, or other operating systems, formatting done at the user level results in less capacity than the physical capacity shown in Table 4-2.

Table 4-2 *Formatted Capacity*

	Vortex 1275AT	Vortex 2550AT
Number of 512-byte sectors	2,512,844	5,034,291

4.3 DATA TRANSFER RATES

Data is transferred from the disk to the read buffer at a rate up to 6.5 MB/s in bursts. Data is transferred from the read buffer to the AT bus at a rate of up to 6.0 MB/s, using programmed I/O without IORDY. If IORDY is used, then this transfer rate can be increased to 16.67 MB/s. Refer to paragraph 6.6.15 IDENTIFY DRIVE command for additional information. Using the Multiword DMA protocol, transfer rates of 16.67 MB/s. are achievable (burst mode only).

4.4 TIMING SPECIFICATIONS

Table 4-3 illustrates the timing specifications of the Vortex 1275/2550AT hard disk drive.

Table 4-3 *Timing Specifications*

Parameter	Vortex 1275/2550AT	
	Typical Nominal[1]	Maximum Worst Case[2]
Single Track Seek[3]	3.5 ms	5.0 ms
Sequential Cylinder Switch Time[4]	3.5 ms	5.0 ms
Sequential Head Switch Time[5]	3.0 ms	5.0 ms
Random Average (Read or Seek)[6]	15.5 ms	18.5 ms
Random Average (Write)	17.0 ms	18.5 ms
Full-Stroke Seek	30 ms	34 ms
Average Rotational Latency	8.33 ms	—
Power On[7] to Drive Ready[8]	11.5 seconds	18.0 seconds
Power On to Interface Ready[9]	11.5 seconds	18.0 seconds
Standby[10] to Drive Ready	11.5 seconds	18.0 seconds
Drive Ready to Shutdown	5 seconds	20 seconds[11]

1. Nominal conditions are as follows:
   - Nominal temperature (25° C)
   - Nominal supply voltages (12.0V, 5.0V)
   - No applied shock or vibration

2. Worst-case conditions are as follows:
   - Worst-case temperature extremes (4°C to 71°C)
   - Worst-case supply voltages (12V ±10%, 5V±5%)

3. Seek time is defined as the time required for the actuator to seek and settle on-track. It is measured by averaging 5000 seeks of the indicated type as shown in this table. The seek times listed include head settling time, but do not include command overhead time or rotational latency delays.

4. Sequential Cylinder Switch Time is the time from the conclusion of the last sector of a cylinder to the first logical sector on the next cylinder.

5. Sequential Head Switch Time is the time from the last sector of a track to the beginning of the first logical sector of the next track of the same cylinder.

6. Average seek time is the average of 5000 random seeks. When a seek error occurs, recovery for that seek can take up to seven seconds.

7. Power On is the time from when the supply voltages reach operating range to when the drive is ready to accept any command.

8. Drive Ready is the condition in which the disks are rotating at the rated speed and the drive is able to accept and execute commands requiring disk access without further delay.

9. Interface Ready is the condition in which the drive is ready to accept any command, before the disks are rotating at rated speed.

10. Standby is the condition in which the microprocessor is powered, but not the HDA. When the host sends the drive a standby command, the drive parks the heads away from the data zone and spins down to a complete stop.

11. After 20 seconds, it is safe to move the disk drive.

4.5 POWER

The Vortex 1275/2550AT hard disk drive operates from two supply voltages:

- +12V ±10%
- +5V ±5%

The allowable ripple and noise for each voltage is 250 mV for the +12 Vdc supply and 100 mV for the +5 Vdc supply.

4.5.1 Power Sequencing

You can apply the power in any order or manner, or short or open either the power or power-return line with no loss of data or damage to the disk drive. However, data may be lost in the sector being written at the time of power loss. The drive can withstand transient voltages of +10% to −100% from nominal while powering up or down.

4.5.2 Power Reset Limits

When powering up, the drive remains reset until both of the reset limits in Table 4-4 are exceeded. When powering down, the drive becomes reset when either supply voltage drops below the lower threshold.

Table 4-4 *Power Reset Limits*

DC VOLTAGE	THRESHOLD	
	On (max)	Off (min.)
+5 V	4.7 V	4.65 V
+12 V	10.7 V	9.7 V

4.5.3 Power Requirements

Table 4-5 lists the voltages and corresponding current for the various modes of operation of the Vortex 1275/2550AT hard disk drive.

Table 4-5 *Typical Power and Current Consumption*

MODE OF OPERATION	Typical Average Current (mA rms)[8]				TYPICAL AVERAGE POWER (WATTS)	
	Vortex 1275AT		Vortex 2550AT			
	+12V	+5V	+12V	+5V	1275AT (1 disk)	2550AT (2 disks)
Startup[1] (peak)	1400	425	1400	425	19	19
Maximum Seek[2]	550	380	590	380	8.5	9.0
Read/Write/Seek[3]	360	420	400	420	6.5	7.0
Read/Write on Track[4]	230	450	270	450	5.0	5.5
Idle[5]	230	250	270	250	4.0	4.5
Standby[6]	5	190	5	190	1.0	1.0
Sleep[7]	5	190	5	190	1.0	1.0

Notes: 1. Startup is stated as the peak (>10 ms) power required during spindle startup. This power will be required for less than 6 seconds.

2. Maximum Seek is for continuous random seek operations with 8.3 ms delay between seek complete indication and the next seek command.

3. Read/Write/Seek mode is defined when data is being read from or written to the disk. It is computed based on 40% seeking, 30% on-track reading and 30% on-track writing.

4. Read/Write/Ontrack is defined as 50% read operations and 50% write operations on a single physical track.

5. Idle is when the drive is not reading, writing, or seeking, the motor is up to speed and the DRIVE READY condition exists. Actuator is residing on last track accessed.

6. Standby is when the motor is stopped, actuator parked, and all electronics except the interface control is in a low power state. STANDBY will occur after a programmable time-out from the last host access. Drive ready and seek complete status exist. The drive will leave STANDBY upon receipt of a command that requires disk access or upon receipt of a spin-up command.

7. Sleep is when the spindle and actuator motors are off with the heads latched in the landing zone. The microprocessor has also entered the halt or power-down state. Receipt of a reset causes the drive to transition from the sleep to the standby mode.

8. Current is rms. (except for startup)

4.6 ACOUSTICS

Table 4-6 and Table 4-7 specifies the acoustical characteristics of the Vortex 1275/2550AT hard disk drive.

Table 4-6 *Acoustical Characteristics – Sound Pressure*

OPERATING MODE	MEASURED NOISE	DISTANCE
Idle On Track	35 dbA (mean) 40 dbA (maximum)	39.3 in (1 m)

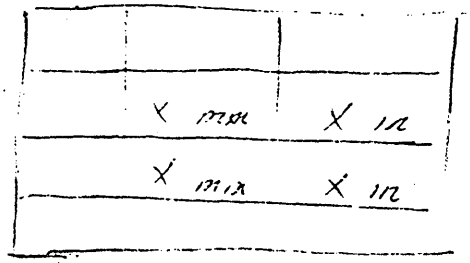
Table 4-7 *Acoustical Characteristics—Sound Power*

Operating Mode	Measured Noise (Sound Power per ISO 7779)
Idle On Track	4.1 Bels (mean) 4.5 Bels (maximum)

4.7 MECHANICAL DIMENSIONS

Table 4-8 specifies the mechanical dimensions of the Vortex 1275/2550AT hard disk drive. Dimensions measurements do not include the faceplate.

Table 4-8 *Mechanical Dimensions*



Dimension	Inches	Millimeters
Height	0.625 in	15.9 mm
Width	5.75 in	146.2 mm
Depth	8.0 in	203.2 mm

Mechanical Weight

	Pounds	Grams
1-Disk	1.55 lbs.	703.07 gm.
2-Disk	1.64 lbs.	743.89 gm.

4.8 ENVIRONMENTAL CONDITIONS

Table 4-9 summarizes the environmental specifications for the Vortex 1275/2550AT hard disk drive.

Table 4-9 *Environmental Specifications*

PARAMETER	OPERATING	NONOPERATING
Temperature	5° to 55°C -15° to 131°F	-40° to 75°C -40° to 167°F
Temperature Gradient	24°C/hr	48°C/hr
Humidity[1] Maximum Wet Bulb	5% to 85% rh 29°C (84°F)	5% to 95% rh 46°C (115°F)
Humidity Gradient	30% hr	30% hr
Altitude[2]	–200 m to 2.4 km (–650 to 8,000 ft.)	–200 m to 12 km (–650 to 40,000 ft.)
Altitude Gradient	1.5 kPa/min.	8 kPa/min.

Notes: [1] No condensation.
[2] Altitude is relative to sea level.

4.9 SHOCK AND VIBRATION

The Vortex 1275/2550AT hard disk drive can withstand levels of shock and vibration applied to any of its three mutually perpendicular axes, or principal base axes, as specified in Table 4-10. A functioning drive can be subjected to specified *operating* levels of shock and vibration. When a drive has been subjected to specified *nonoperating* levels of shock and vibration, with power to the drive off, there will be no change in performance at power on.

When packed in either the 1-pack or 10-pack shipping container, Vortex 1275/2550AT drives can withstand a drop from 30 inches onto a concrete surface on any of its surfaces, six edges, or three corners.

Table 4-10 *Shock and Vibration Specifications*

	OPERATING	NONOPERATING
Shock	10G, 1/2 sine wave, 11 ms TBDG, 1/2 sine wave, 2ms	70G, 11ms, 1/2 sine wave TBDG, 2ms 1/2 sine wave
Vibration[1] 1.0 octave/minute sweep	1G p-p, 5-500 Hz (X and Y axis) 1 G p-p, 5-200 Hz (Z axis)	2G p-p, 5-500 Hz

1. No unrecovered errors.

4.10 RELIABILITY

Mean Time Between Failures (MTBF):	The projected field MTBF is 300,000 hours (150,000 Power On Hours (POH), typical usage). The Quantum MTBF numbers represent Bell-Core TR-TSY-000332 MTBF predictions and represent the minimum MTBF that Quantum or a customer would expect from the drive.
Preventive Maintenance (PM):	Not required
Start/Stop:	20,000 cycles (minimum)
Component Life:	5 Years

4.11 DISK ERRORS

Table 4-11 provides the error rates for the Vortex 1275/2550AT hard disk drive.

Table 4-11 *Error Rates*

ERROR TYPE	MAXIMUM NUMBER OF ERRORS
Reallocated data errors:	
Correctable read errors[1]	1 error per 10^{12} bits read
Uncorrectable read errors[2]	1 error per 10^{14} bits read
Seek Errors[3]	1 error per 10^{6} seeks

Notes:

[1] Correctable read errors are read errors that are recovered by retries or by application of the triple-burst error correction algorithm.

[2] Uncorrectable read errors are errors that are not correctable using ECC or retries. The drive will terminate retry reads either when a repeating error pattern occurs, or after eight unsuccessful retries and the application of triple-burst error correction.

[3] Seek errors occur when the actuator fails to reach (or remain) over the requested cylinder or if the drive executes a recalibration routine to find the requested cylinder (a full recalibration takes about seven seconds).

Chapter 5
BASIC PRINCIPLES OF OPERATION

This chapter describes the operation of Quantum Vortex 1275/2550AT functional subsystems. It is intended as a guide to the operation of the drive, rather than a detailed theory of operation.

5.1 QUANTUM VORTEX DRIVE MECHANISM

This section describes the drive mechanism. Section 5.2 describes the drive electronics. The Quantum Vortex 1275/2550AT hard disk drive consists of a mechanical assembly and a PCB as shown in Figure 5-1. The drawing is illustrated with two disks, showing the Quantum Vortex 2550AT drive configuration. The Quantum Vortex 1275AT hard disk drive contains only one hard disk.

The head/disk assembly (HDA) contains the mechanical subassemblies of the drive, which are sealed under a metal cover. The HDA consists of the following components:

- Base casting
- DC motor assembly
- Disk stack assembly
- Headstack assembly
- Rotary positioner assembly
- Automatic actuator lock
- Air filter

The drive is assembled in a Class-100 clean room.

> **CAUTION:** To ensure that the air in the HDA remains free of contamination, never remove or adjust its cover and seals. Tampering with the HDA will void your warranty.

The Quantum Vortex 1275/2550AT drive is a one or two disk product family. The Quantum Vortex 1275AT hard disk drive contains one magnetic disk and two read/write heads. The Quantum Vortex 2550AT drive contains two magnetic disks and four read/write heads.

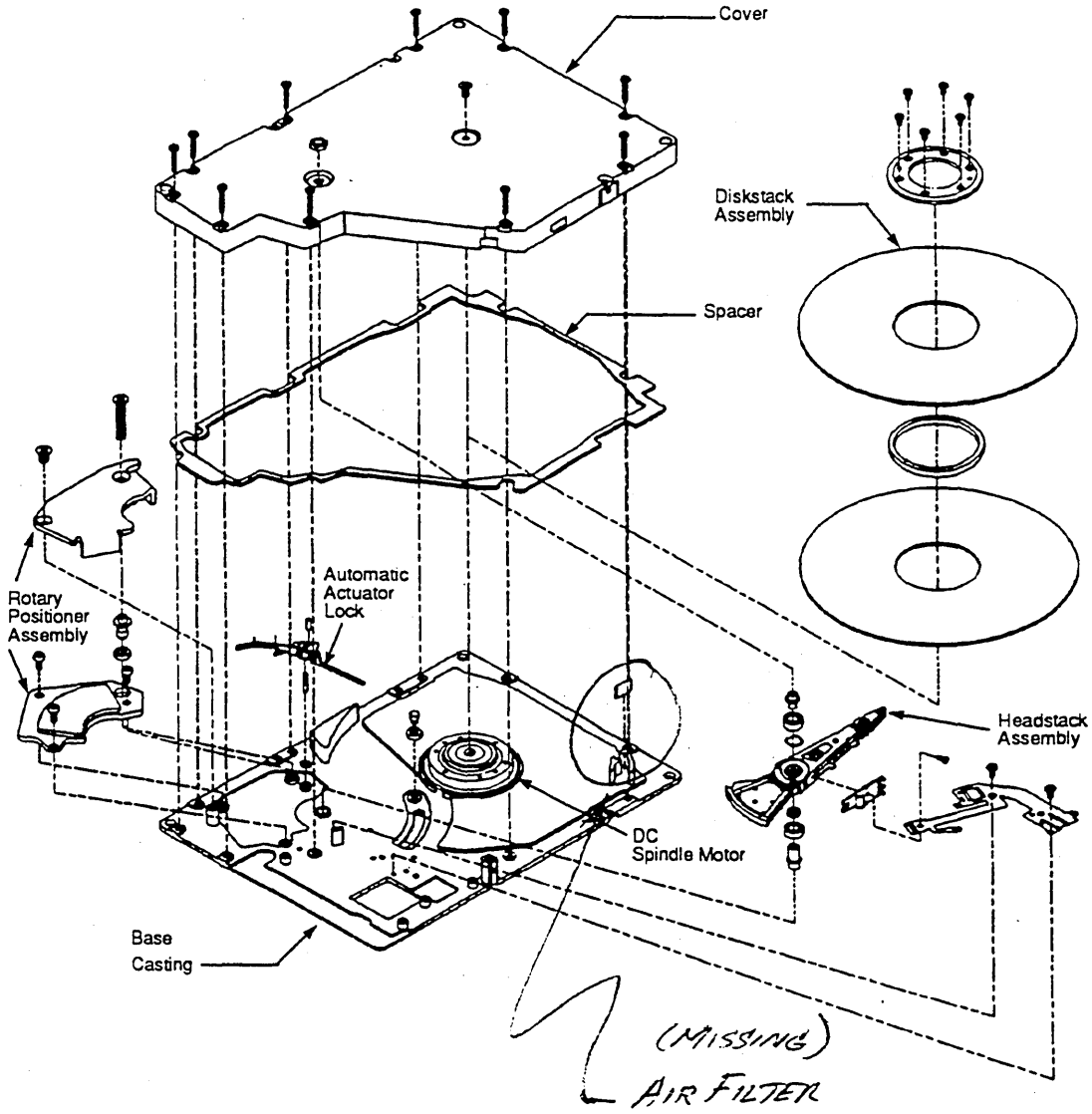


Figure 5-1 *Quantum Vortex 2550AT Hard Disk Drive Exploded View*

5.1.1 Base Casting Assembly

A single-piece, aluminum-alloy base casting provides a mounting surface for the drive mechanism and PCB. The base casting also acts as the flange for the DC motor assembly. To provide a contamination-free environment for the HDA, a gasket provides a seal between the base casting and the metal cover that encloses the drive mechanism.

5.1.2 DC Motor Assembly

Integral with the base casting, the DC motor assembly is a fixed-shaft, brushless DC spindle motor that drives the counter-clockwise rotation of the disks.

5.1.3 Disk Stack Assemblies

The disk stack assembly in the Quantum Vortex 1275AT hard disk drive consists of one disk secured by a disk clamp. The Quantum Vortex 2550AT hard disk drives contains two disks. The aluminum-alloy disks have a sputtered thin-film magnetic coating.

A carbon overcoat lubricates the disk surface, to prevent head and media wear due to head contact with the disk surface during head takeoff and landing. Head contact with the disk surface occurs only in the landing zone outside of the data area, when the disk is not rotating at full speed. The landing zone is located at the inner diameter of the disk, beyond the last cylinder of the data area.

The Quantum Vortex 1275/2550AT hard disk drive has 5,762 tracks per recording surface. Of these tracks, 24 are used for system data, leaving 5,738 for data. The data tracks are divided into 15 recording zones. The drive uses multiple zone recording, where each data track contains between 149 and 276 sectors, depending on the recording zone. The sectors per track allocation for each zone is provided in Table 5-1.

Table 5-1 *Cylinder Contents*

ZONE[1]	NUMBER OF TRACKS	SECTORS PER TRACK	DATA RATE (Mbit/s)
0	24	192	57.58
1	378	276	83.76
2	378	276	83.22
3	378	273	82.57
4	378	261	79.33
5	378	256	77.18
6	378	245	74.40
7	378	235	71.61
8	378	225	68.83
9	378	214	65.43
10	378	204	62.42
11	378	192	57.58
12	378	183	56.47
13	378	172	53.34
14	378	160	49.27
15	378	149	46.48

1. For user data, zone 15 is the innermost zone and zone 1 is the outermost zone.

CYLINDER CONTENTS	ZONE[1]	NUMBER OF TRACKS	SECTORS PER TRACK	DATA RATE (Mbits/sec)
System Data	0	24	192	57.58
User Data	1	383	276	83.76
"	2	383	276	83.22
"	3	383	270	82.57
"	4	383	261	79.33
"	5	383	253	77.18
"	6	383	243	74.40
"	7	383	233	71.61
"	8	383	224	68.83
"	9	382	212	65.43
"	10	382	202	62.42
"	11	382	192	57.58
"	12	382	180	56.47
"	13	382	169	53.34
"	14	382	160	49.27
User Data	15	382	144	46.48

Note 1. For user data, zone 15 is the innermost zone and zone 1 is the outermost zone.

5.1.4 Headstack Assembly

The headstack assembly consists of read/write heads, an E-block and coil joined together by insertion molding to form an E-block/coil subassembly, bearings, and a flex circuit. Read/write heads mounted to spring-steel flexures are swage mounted onto the rotary positioner assembly arms. The E-block is a single piece, die-cast design.

The flex circuit exits the HDA between the base casting and the cover. A cover gasket seals the gap. The flex circuit connects the headstack assembly to the PCB. The flex circuit contains a read preamplifier/write driver IC.

5.1.5 Rotary Positioner Assembly

The rotary positioner, or rotary voice-coil actuator, is a Quantum-proprietary design that consists of an upper permanent magnet plate and lower flux plate bolted to the base casting, a rotary single-phase coil molded around the headstack mounting hub, and a bearing shaft. The single bi-polar magnet consists of two alternating poles and is bonded to the magnet plate. A resilient crash stop prevents the heads from being driven into the spindle or off the disk surface

Current from the power amplifier induces a magnetic field in the voice coil. Fluctuations in the field around the permanent magnet cause the voice coil to move. The movement of the voice coil positions the heads over the requested cylinder.

5.1.6 Automatic Actuator Lock

To ensure data integrity and prevent damage during shipment, the drive uses a dedicated landing zone and Quantum's patented Airlock®. The Airlock holds the headstack in the landing zone whenever the disks are not rotating. It consists of an air vane mounted near the perimeter of the disk stack and a locking arm that restrains the actuator arm assembly.

When DC power is applied to the motor and the disk stack rotates, the rotation generates an airflow on the surface of the disk. As the flow of air across the air vane increases with disk rotation, the locking arm pivots away from the actuator arm, enabling the headstack to move out of the landing zone. When DC power is removed from the motor, an electronic return mechanism automatically pulls the actuator into the landing zone, where the Airlock holds it in place.

5.1.7 Air Filtration

The Quantum Vortex 1275/2550AT hard disk drives are Winchester-type drives. The heads fly very close to the media surface. Therefore, it is essential that the air circulating within the drive be kept free of particles. Quantum assembles the drive in a Class-100, purified air environment, then seals the drive with a metal cover. When the drive is in use, the rotation of the disks forces the air inside of the drive through an internal filter.

The highest air pressure within the HDA is at the outer perimeter of the disks. A constant stream of air flows through a 0.3-micron circulation filter positioned in the base casting. As illustrated in Figure 5-2, air flows through the circulation filter in the direction of disk rotation. This design provides a continuous flow of filtered air when the disks rotate.

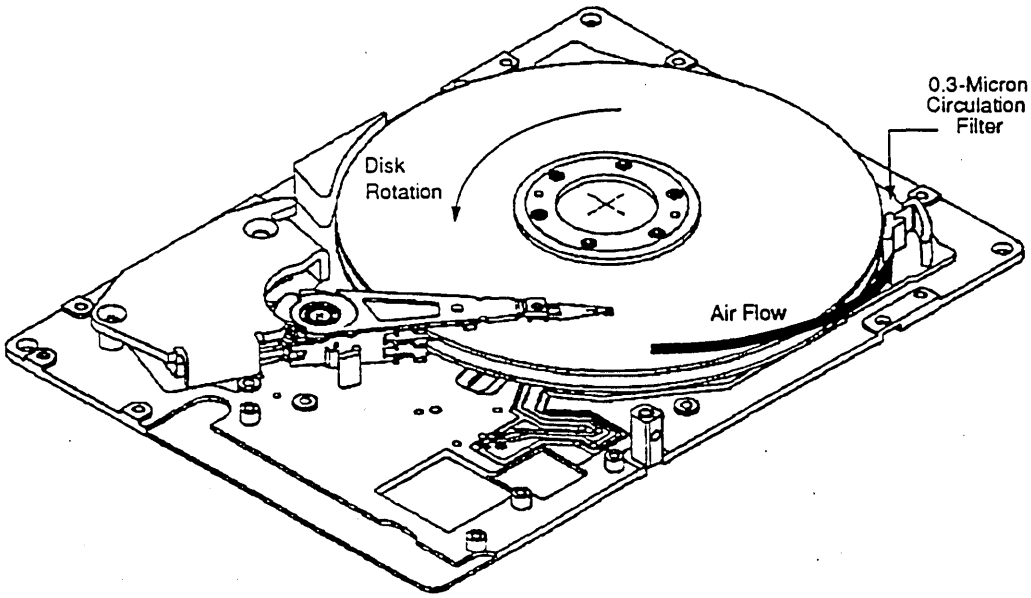


Figure 5-2 *HDA Air Filtration*

5.2 DRIVE ELECTRONICS

Advanced circuit design and the use of miniature surface-mounted devices and proprietary VLSI components enable the drive electronics, including the IDE bus interface, to reside on a single printed circuit board assembly (PCBA).

Note: The components are mounted on only one side of the PCB.

Figure 5-3 contains a simplified block diagram of the Quantum Vortex 1275/2550AT hard disk drive electronics.

The only electrical component not on the PCBA is the PreAmplifier and Write Driver IC. It is on the flex circuit (inside of the sealed HDA). Mounting the preamplifier as close as possible to the read/write heads improves the signal-to-noise ratio. The flex circuit (including the PreAmplifier and Write Driver IC) provides the electrical connection between the PCB, the rotary positioner assembly, and read/write heads.

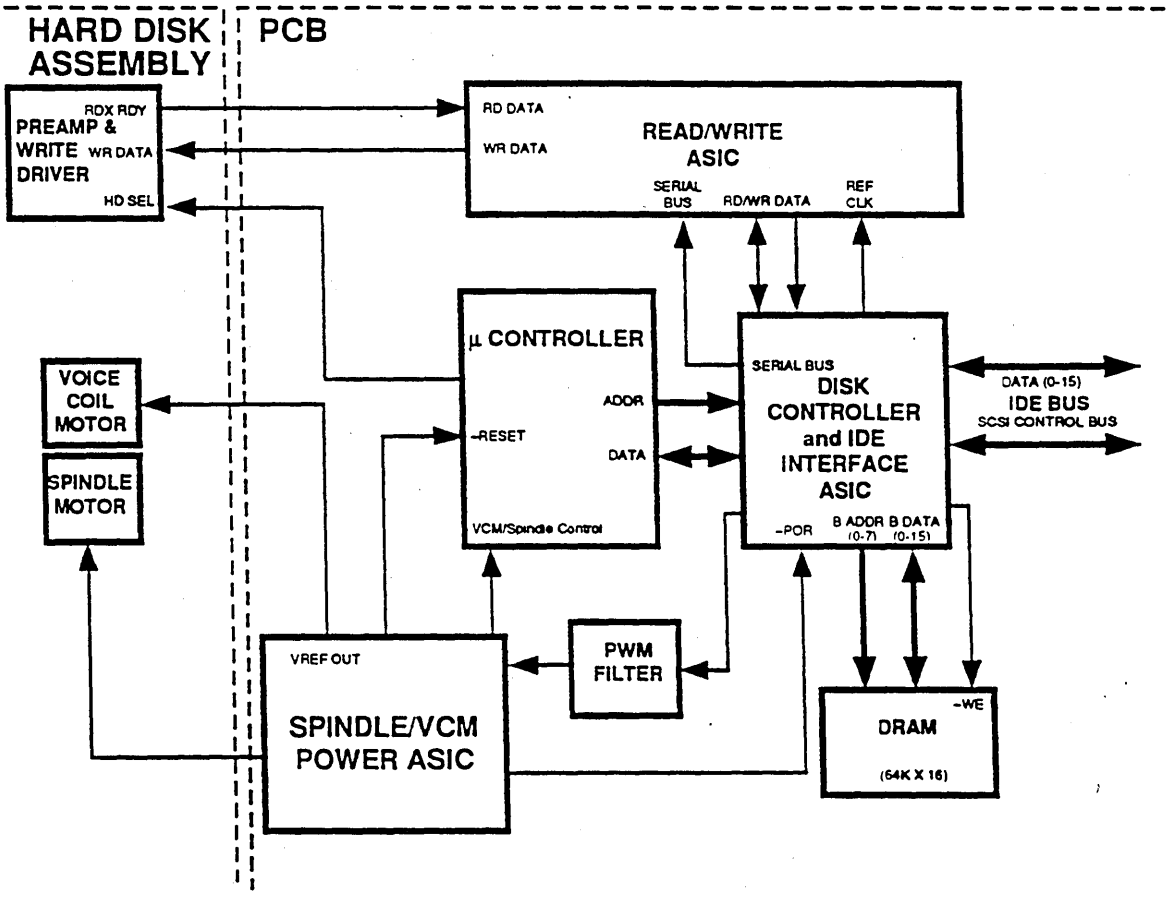


Figure 5-3 *Quantum Vortex 1275/2550AT Hard Disk Drive Block Diagram*

5.2.1 µController

The µController provides local processor services to the drive electronics under program control. The µController manages the resources of the Disk Controller and IDE Interface ASIC (DCIIA), the Read/Write ASIC, and the Spindle/VCM Driver. In addition, it controls the head selection process.

An internal 54 Kbyte ROM contained within the µController provides program code that the µController executes to complete a drive spinup and recalibration procedure, after which the µController reads additional control code from the disk (diskware) and stores it in the buffer DRAM.

5.2.2 DCIIA

The DCIIA (Disk Controller and IDE Interface ASIC) shown in Figure 5-4 provides control functions to the drive under the direction of the µController.

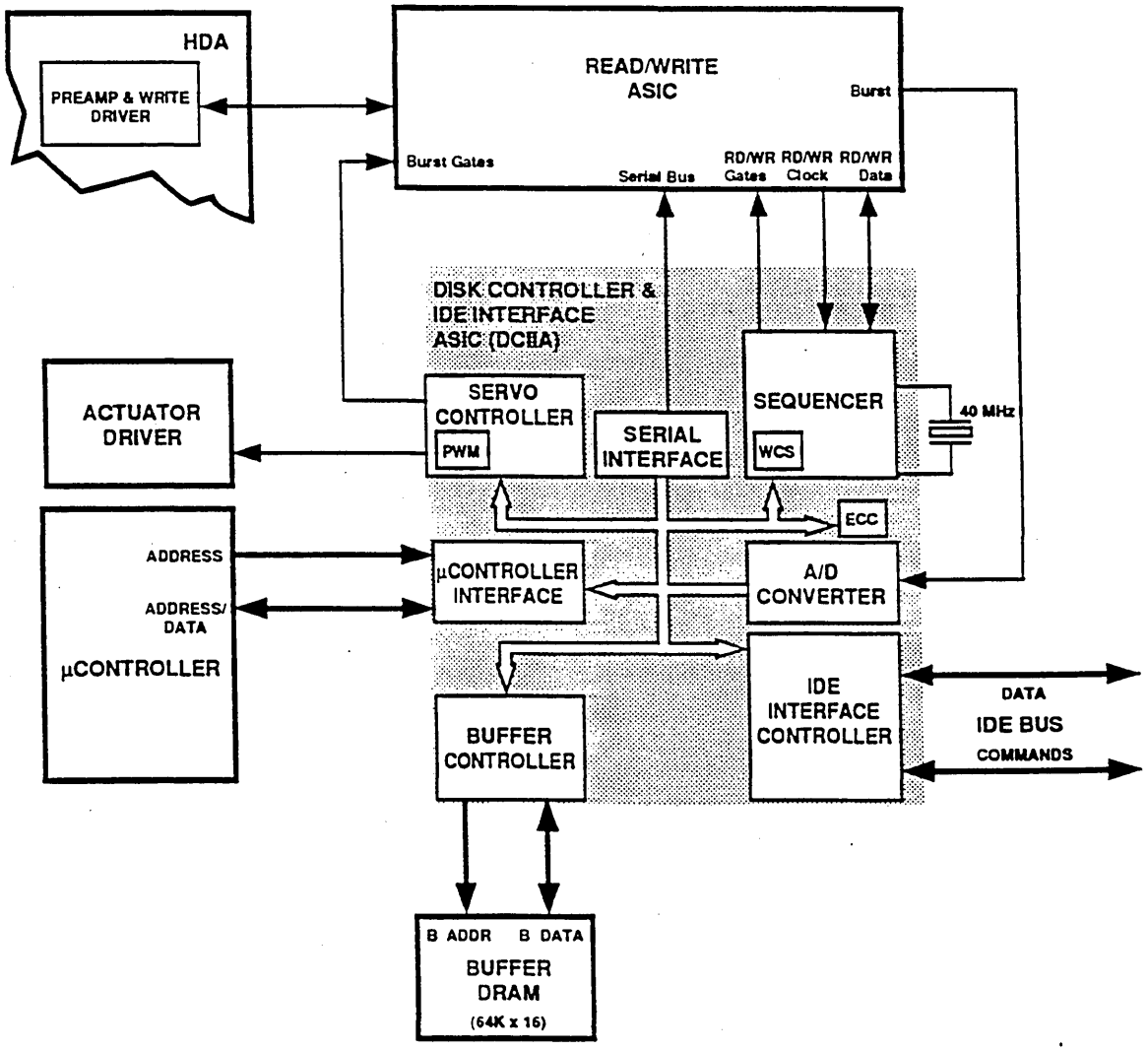


Figure 5-4 *DCIIA Block Diagram*

The DCIIA is a proprietary ASIC developed by Quantum. The DCIIA comprises eight functional modules (described below):

- 8-bit A/D Converter
- Error Correction Control
- Sequencer
- Buffer Controller
- µController Interface
- Servo Controller, including PWM
- Serial Interface
- IDE Interface Controller

5.2.2.1 A/D Converter

The Analog to Digital converter (A/D) receives multiplexed burst analog inputs from the Read/Write ASIC. The A/D is used to sample the demodulated position information (burst inputs) and convert it to a digital signal the Servo Controller uses to position the HDA actuator.

5.2.2.2 Error Correction Control

The Error Correction Control block utilizes a Reed-Solomon encoder/decoder circuit that is used for disk read/write operations. It uses a total of 20 redundancy bytes organized as 18 ECC (Error Correction Code) bytes and two cross-check bytes. The ECC uses eight bits per symbol and three interleaves. This allows triple-burst error correction of at least 51, and as many as 72 bits in error.

5.2.2.3 Sequencer

The sequencer controls the operation of the read and write channel portions of the DCIIA. To initiate a disk operation, the µController loads a set of commands into the WCS (writable control store) register. Loading and manipulating the WCS is done through the µController Interface registers.

The sequencer also directly drives the read and write gates (RG, WG) of the Read/Write ASIC and the R/W Preamplifier, as well as passing write data to the Precompensator circuit in the Read/Write ASIC.

5.2.2.4 Buffer Controller

The buffer controller supports a 128 Kbyte buffer, which is organized as 64 K x 16 bits. The 16-bit width implementation provides a 32 MB/s maximum buffer bandwidth, which allows 11 MB/s maximum disk channel bandwidth. This increased bandwidth allows the µController to have direct access to the buffer, eliminating the need for a separate µController RAM IC.

The buffer controller supports both drive and host address rollover and reloading, to allow for buffer segmentation. Drive and host addresses may be separately loaded for automated read/write functions.

The Buffer Controller operates under the direction of the µController.

5.2.2.5 µController Interface

The µController Interface provides the means for the µController to read and write data to the DCIIA modules to control their operation or supply them with needed information. It consists of both physical and logical components.

The physical component of the interface comprises the 16-bit MAD (Multiplexed Address/Data) bus, four additional address lines, read and write strobe, an address latch enable (ALE) signal, and a wait control line.

The logical component of the interface comprises internal control and data registers accessible to the µController. By writing and reading these registers, the µController loads the Sequencer, controls and configures the Buffer controller, and passes coded servo information to the Servo Controller.

5.2.2.6 Servo Controller

The Servo Controller contains a 13-bit Digital to Analog converter (D/A), in the form of a Pulse Width Modulator (PWM). The PWM signal is output to the Actuator Driver to control the motion of the actuator. The Servo Controller also decodes raw data from the disk to extract the current position information. The position information is read by the µController and is used to generate the actuator control signal that is sent to the PWM. The actuator driver is an analog power amplifier circuit external to the DCIIA. The Servo Controller operates under the direction of the µController.

5.2.2.7 Serial Interface

The Serial Interface provides a high speed Read/Write interface path to the Read/Write ASIC under the direction of the µController.

5.2.2.8 IDE Interface Controller

The IDE Interface Controller portion of the DCIIA provides data handling, bus control, and transfer management services for the IDE interface. Configuration and control of the interface is accomplished by the µController across the MAD bus. Data transfer operations are controlled by the DCIIA Buffer Controller module.

5.2.3 Read/Write ASIC

The Read/Write ASIC shown in Figure 5-5 provides write data precompensation and read channel processing functions for the drive. The Read/Write ASIC receives the RD GATE signal, reference oscillator, serial programming, and servo burst and sample gates from the DCIIA. The Read/Write ASIC sends decoded read data and the read reference clock, and receives write data from the DCIIA. This a highly integrated circuit which is completely under digital control from the DCIIA.

The Read/Write ASIC comprises 11 main functional modules (described below):

- Pre-Compensator
- Variable Gain Amplifier (VGA)
- Butterworth Filter
- FIR Filter
- Flash A/D Converter
- Viterbi Detector
- ENDEC
- Servo Detector and Sample/Hold
- Clock Synthesizer
- PLL
- Serial Interface

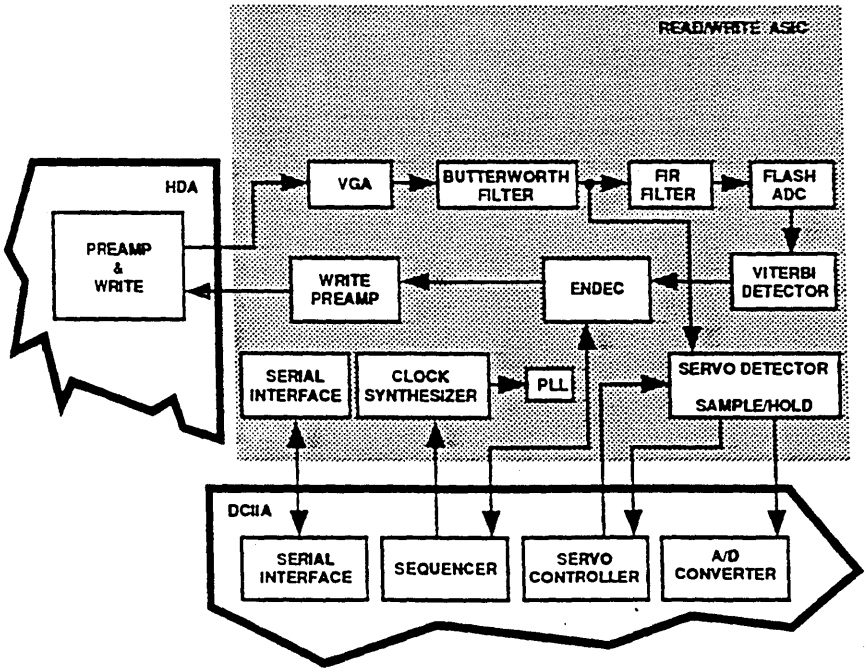


Figure 5-5 *Read/Write ASIC Block Diagram*

5.2.3.1 Pre-Compensator

The pre-compensator introduces pre-compensation to the write data received from the sequencer module in the DCIIA. The pre-compensated data is then passed to the R/W Pre-Amplifier and written to the disk. Pre-compensation reduces the write interference from adjacent write bit.

5.2.3.2 Variable Gain Amplifier (VGA)

Digital and analog controlled AGC function with input attenuator for extended range.

5.2.3.3 Butterworth Filter

Continuous time data filter which can be programmed for each zone rate.

5.2.3.4 FIR Filter

Digitally controlled and programmable filter for partial response signal conditioning.

5.2.3.5 Flash A/D Converter

Provides very high speed digitization of the processed read signal.

5.2.3.6 Viterbi Detector

Decodes ADC result into binary bit stream.

5.2.3.7 ENDEC

Provides 16/17 code conversion to NRZ. Includes preamble and sync mark generation and detection.

5.2.3.8 Servo Detector and Sample/Hold

Peak detection with weighted averaging and multiple sample and hold of servo bursts.

5.2.3.9 Clock Synthesizer

Provides programmable frequencies for each zone data rate.

5.2.3.10 PLL

Provides digital read clock recovery.

5.2.3.11 Serial Interface

High speed interface for digital control of all internal blocks.

5.2.4 PreAmplifier and Write Driver

The PreAmplifier And Write Driver provides write driver and read pre-amplifier functions, and R/W head selection. The write driver receives precompensated write data from the PreCompensator module in the Read/Write ASIC. The write driver then sends this data to the heads in the form of a corresponding alternating current. The read pre-amplifier amplifies the low-amplitude differential voltages generated by the R/W heads and transmits them to the VGA module in the Read/Write ASIC. Head select is determined by the µController.

5.3 SERVO SYSTEM

5.3.1 General Description

The servo system controls the positioning of the read/write heads and holds the read/write heads on track during read/write operations. The servo system also compensates for thermal offsets between heads on different surfaces, and any shock and vibration the drive is subjected to.

The Quantum Vortex 1275/2550AT hard disk drive uses a sectored servo system. Positioning information is radially encoded in evenly-spaced servo bursts on each track. These servo burst wedges provide radial position information for each data head. Because the drive uses multiple zone recording, where each zone has a different bit density, split data fields are necessary to optimally utilize the non-servo area of the disk. The split data fields are achieved by special processing through the DCIIA, and their presence is transparent to the host system. The servo area remains phase coherent across the surface of the disk, even though the disk is divided into various data zones. The main advantage of the sectored servo systems is that the data heads are also servo heads, which means that sectored servo systems eliminate the problems of static and dynamic offsets between heads on different surfaces.

The Quantum Vortex 1275/2550AT hard disk drive servo system is also classified as a digital servo because track following compensation is done in firmware. The bump detect, on-track, velocity profiles, and other "housekeeping" tasks are also done in firmware.

The state of the servo system determines how the position information is derived. During seeking, the position signal is the convolution of the track number and A or B burst values and has a 1/256 of a track pitch resolution—about 0.4%. During track following, the A and C bursts are used for the position information, and the resolution is at least 1/512th of a track pitch—about 0.2%.

5.3.2 Servo Burst and Track Information

Positional information is encoded on all tracks on all data surfaces. All data heads are also servo heads. The areas with servo/position information are called wedge areas. These wedge areas are evenly spaced radially around the disk, like spokes on a wheel. There are 96 wedge areas per track. Since the disk rotation is 90.0 revolutions/second, the position information is updated at 5760 Hz (96 x 90.0). This is also known as the sampling frequency fs. The sample period, Ts, is $1/fs$ = 174 µs. Every wedge area consists of four separate fields: (1) Automatic Gain Control (AGC)/ Sync field, (2) Servo Address Mark (SAM) field, (3) Track number and (4) Burst area. Since a Phase Lock Loop (PLL) is not used in the servo wedge area, time discrimination is used. Timing for all four fields is generated from the same crystal reference.

5.4 READ AND WRITE OPERATIONS

The following paragraphs provide descriptions of the read channel, write channel, and IDE interface control operations.

5.4.1 The Read Channel

The drive has one read/write head for each data surface (two for the Quantum Vortex 1275AT drive and four for the Quantum Vortex 2550AT drive). The signal path for the read channel begins at the read/write heads. As the magnetic flux transitions recorded on a disk pass under a head, they generate low-amplitude, differential output voltages. These read signals pass from the read/write head to the flex circuit's read preamplifier, which amplifies the signal. To ensure a high signal to noise ratio, preamplification occurs on the flex circuit because of its proximity to the heads.

The flex circuit transmits the preamplified signal from the HDA to the drive PCB. On the PCB, the Read/Write ASIC further processes the read signal to reduce ambiguities (for example, drop-ins, drop-outs, and peak shift). In addition, it converts the signal from the serial encoded head data to a synchronized data stream, with its accompanying clock. The Read/Write ASIC then sends the resynchronized and decoded data output to Quantum's proprietary Disk Controller and IDE Interface ASIC (DCIIA).

The DCIIA manages the flow of data between on the Read/Write ASIC and its IDE Interface Controller. It also controls data access for the external RAM buffer. The DCIIA format provides a serial bit stream. This NRZ (Non-Return to Zero) serial data is converted to an 8-bit byte. The Sequencer module identifies the data as belonging to the target sector. Data is presented to the host in a 16-bit word.

After a full sector is read, the DCIIA checks to see if the firmware needs to apply ECC on-the-fly or single-, double-, or triple-burst correction to the data. The buffer controller section of the DCIIA stores the data in the Cache and transmits the data to the IDE Interface Controller module, which transmits the data to the IDE bus.

5.4.2 The Write Channel

For the write channel, the signal path follows the reverse order of that for the read channel. The host presents a 16-bit word of data, by means of the IDE bus, to the DCIIA IDE Interface Controller. The Buffer Controller section of the DCIIA stores the data in the cache. Because data can be presented to the drive at a rate that exceeds the rate at which the drive can write data to a disk, data is stored temporarily in the cache. Thus, the host can present data to the drive at a rate that is independent of the rate at which the drive can write data to the disk.

Upon correct identification of the target address, the data is shifted to the Sequencer where an error correcting code is generated and appended. The Sequencer then converts the bytes of data to a serial bit stream. The DCIIA transmits the data to the Read/Write ASIC where the data is encoded and precompensated to reduce intersymbol interference. The data is then transmitted to the Write Driver by means of the write data lines.

The drive's DCIIA switches the Preamplifier Write Driver IC to write mode and selects a head. Once the Write driver receives a write gate signal, it transmits current reversals to the head, which induces magnetic transitions on the disk.

5.4.3 Interface Control

The interface with the host system is through a 40-pin IDE interface connector. The DCIIA IDE Interface Controller module implements the IDE interface logic. Operating under the drive's µprocessor control, the DCIIA receives and transmits words of data over the IDE bus.

The DCIIA Buffer Controller writes data to or reads data from the Cache over 16 data lines. Under µController direction, the DCIIA controls the transfer of data and handles the addressing of the Cache. The internal data transfer rate to and from the Cache is 32 MB/s. This high transfer rate allows the DCIIA to communicate over the IDE interface at a PIO data transfer rate of 6.67 MB/s without using IORDY, up to 16.67 MB/s with PIO using IORDY, or a DMA transfer rate of up to 16.67 MB/s while it simultaneously controls disk-to-RAM transfers and microcontroller access to control code stored in the buffer RAM.

5.5 FIRMWARE FEATURES

This section describes the following firmware features:

- Disk caching
- Track and cylinder skewing
- Error detection and correction
- Defect management

5.5.1 Disk Caching

The Quantum Vortex 1275/2550AT hard disk drive incorporates DisCache, a 80 K disk cache, to enhance drive performance. This integrated feature is user-programmable and can significantly improve system throughput. Read and write caching can be enabled or disabled by using the Set Configuration command.

5.5.1.1 Adaptive Caching

The cache buffer for the Quantum Vortex drive features adaptive segmentation for more efficient use of the buffer's RAM. With this feature, the buffer space used for read and write operations is dynamically allocated. The cache can be flexibly divided into several segments, under program control. Each segment contains one cache entry.

A cache entry consists of the requested read data plus its corresponding prefetch data. Adaptive segmentation allows the drive to make optimum use of the buffer, the amount of stored data can be increased.

5.5.1.2 Read Cache

DisCache anticipates host-system requests for data and stores that data for faster access. When the host requests a particular segment of data, the caching feature uses a prefetch strategy to "look ahead" and automatically store the subsequent data from the disk into high-speed RAM. If the host requests this subsequent data, the RAM is accessed rather than the disk.

Since typically 50 percent or more of all disk requests are sequential, there is a high probability that subsequent data requested will be in the cache. This cached data can be retrieved in microseconds rather than milliseconds. As a result, DisCache can provide substantial time savings during at least half of all disk requests. In these instances, DisCache could save most of the disk transaction time by eliminating the seek and rotational latency delays that dominate the typical disk transaction. For example, in a 1K data transfer, these delays make up to 90 percent of the elapsed time.

DisCache works by continuing to fill its cache memory with adjacent data after transferring data requested by the host. Unlike a noncaching controller, Quantum's disk controller continues a read operation after the requested data has been transferred to the host system. This read operation terminates after a programmed amount of subsequent data has been read into the cache segment.

The cache memory consists of a 80 K DRAM buffer allocated to hold the data, which can be directly accessed by the host by means of the READ and WRITE commands. The memory functions as a group of segments (ring buffers) with rollover points at the end of each segment (buffer). The unit of data stored is the logical block (that is, a multiple of the 512 byte sector). Therefore, all accesses to the cache memory must be in multiples of the sector size. The following commands force emptying of the cache:

- RESET
- WRITE LONG
- EXECUTE DRIVE DIAGNOSTIC
- FORMAT TRACK
- READ CONFIGURATION
- READ DEFECT LIST
- READ LONG
- IDENTIFY DRIVE
- SET CONFIGURATION
- WRITE BUFFER
- SLEEP

5.5.1.3 Write Cache

When a write command is executed with write caching enabled, the drive stores the data to be written in a DRAM cache buffer and immediately sends a GOOD STATUS message to the host before the data is actually written to the disk. The host is then free to move on to other tasks, such as preparing data for the next data transfer, without having to wait for the drive to seek to the appropriate track or rotate to the specified sector.

While the host is preparing data for the next transfer, the drive immediately writes the cached data to the disk, usually completing the operation in less than 20 ms after issuing GOOD STATUS. With WriteCache, a single-block, random write, for example, requires only about 3 ms of host time. Without WriteCache, the same operation would occupy the host for about 20 ms.

WriteCache allows data to be transferred in a continuous flow to the drive rather than as individual blocks of data separated by disk access delays. This is achieved by taking advantage of the ability to write blocks of data sequentially on a disk that is formatted with a 1:1 interleave. This means that as the last byte of data is transferred out of the write cache and the head passes over the next sector of the disk, the first byte of the of the next block of data is ready to be transferred, thus there is no interruption or delay in the data transfer process.

The WriteCache algorithm fills the cache buffer with new data from the host while simultaneously transferring the data to the disk that the host previously stored in the cache.

5.5.1.4 Performance Benefits

In a drive without DisCache, there is a delay during sequential reads because of the rotational latency even if the disk actuator already is positioned at the desired cylinder. DisCache eliminates this rotational latency time (5.56 ms on average) when requested data resides in the cache.

Moreover, the disk must often service requests from multiple processes in a multitasking or multiuser environment. In these instances, while each process might request data sequentially, the disk drive must share time among all these processes. In most disk drives, the heads must move from one location to another. With DisCache, even if another process interrupts, the drive continues to access the data sequentially from its high-speed memory. In handling multiple processes, DisCache achieves its most impressive performance gains, saving both seek and latency time when desired data resides in the cache.

The cache can be flexibly divided into several segments, under program control. Each segment contains one cache entry. A cache entry consists of the requested read data plus its corresponding prefetch data.

The requested read data takes up a certain amount of space in the cache segment so the corresponding prefetch data can essentially occupy the rest of the space within the segment. The other factors determining prefetch size are the maximum and minimum prefetch. The drive's prefetch algorithm dynamically controls the actual prefetch value based on the current demand, with the consideration of overhead to subsequent commands.

5.5.2 Track and Cylinder Skewing

Track and cylinder skewing in the Quantum Vortex 1275/2550AT drive minimizes latency time and thus increases data throughput.

5.5.2.1 Track Skewing

Track skewing reduces the latency time that results when the drive must switch read/write heads to access sequential data. A track skew is employed such that the next logical sector of data to be accessed will be under the read/write head once the head switch is made and the data is ready to be accessed. Thus, when sequential data is on the same cylinder but on a different disk surface, a head switch is needed but not a seek. Since the sequential head-switch time is well defined on the Quantum Vortex 1275/2550AT drive, the sector addresses can be optimally positioned across track boundaries to minimize the latency time during a head switch. See Table 5-2.

5.5.2.2 Cylinder Skewing

Cylinder skewing also is used to minimize the latency time associated with a single-cylinder seek. The next logical sector of data that crosses a cylinder boundary is positioned on the drive such that after a single-cylinder seek is performed, and when the drive is ready to continue accessing data, the sector to be accessed is positioned directly under the read/write head. Therefore, the cylinder skew takes place between the last sector of data on the last head of a cylinder and the first sector of data on the first head of the next cylinder. Since single-cylinder seeks are well defined on the Quantum Vortex 1275/2550AT drive, the sector addresses can be optimally positioned across cylinder boundaries to minimize the latency time associate with a single-cylinder seek. See Table 5-2.

NEW TABLE ON FOLLOWING PAGE.

Table 5-2 *Track and Cylinder Skews*

ZONE	SECTORS PER TRACK	µS PER SECTOR	ROUNDED TRACK SKEW (IN SECTORS)	NUMBER OF CYLINDERS	ROUNDED CYLINDER SKEW (IN SECTORS)
15	149	46.48	53	378	62
14	160	49.27	57	378	67
13	172	53.34	60	378	71
12	183	56.47	64	378	75
11	192	57.56	68	378	80
10	204	62.42	71	378	83
9	214	65.43	75	378	88
8	225	68.33	78	378	92
7	245	71.61	81	378	96
6	245	74.40	85	378	100
5	256	77.18	87	378	103
4	261	79.33	91	378	107
3	273	82.57	94	378	111
2	276	83.22	97	378	115
1	276	83.76	98	378	115

5.5.3 Error Detection and Correction

As disk drive areal densities increase, obtaining extremely low error rates requires a new generation of sophisticated error correction codes. Quantum Vortex 1275/2550AT hard disk drive series implement 160-bit triple-burst Reed-Solomon error correction techniques to reduce the uncorrectable read error rate to less than one bit in 1×10^{14} bits read.

When errors occur, an automatic retry, a double-burst, and a more rigorous triple-burst correction algorithm enable the correction of any sector with three bursts of three incorrect bytes each or up to nine multiple random one-byte burst errors. In addition to these advanced error correction capabilities, the drive uses an additional cross-checking code and algorithm, to double check the main ECC correction. This greatly reduces the probability of a miscorrection.

ZONE	SECTORS PER TRACK	uS PER SECTOR	ROUNDED TRACK SKEW (IN SECTORS)	NUMBER OF CYLINDERS	ROUNDED CYLINDER SKEW (IN SECTORS)
1	276	83.76	98	383	115
2	276	83.22	98	383	115
3	270	82.57	96	383	113
4	261	79.33	92	383	109
5	253	77.18	90	383	105
6	243	74.40	86	383	101
7	233	71.61	83	383	97
8	224	68.33	79	383	93
9	212	65.43	75	382	88
10	202	62.42	72	382	84
11	192	57.58	68	382	80
12	180	56.47	64	382	75
13	169	53.34	60	382	70
14	160	49.27	57	382	67
15	144	46.48	51	382	60

5.5.3.1 Background Information on Error Correction Code and ECC On-the-Fly

A sector for Quantum Vortex 1275/2550AT drive comprises of 512 bytes of user data, followed by two cross-checking (XC) bytes (16 bits), followed by eighteen ECC check bytes (144 bits). The two cross-checking bytes are used to double check the main ECC correction and reduce the probability of miscorrection. Errors of up to 48 bits within one sector can be corrected "on-the-fly," in real time as they occur, allowing a high degree of data integrity with no impact to the drive's performance.

The drive does not need to re-read a sector on the next disk revolution or apply ECC for those errors that are corrected on-the-fly. Errors corrected in this manner are invisible to the host system.

When errors cannot be corrected on-the-fly, an automatic retry, and a more rigorous triple-burst error correction algorithm enables the correction of any sector with three bursts of three incorrect bytes each (up to 9 contiguous bytes) or up to 9 multiple random one-byte burst errors. In addition to this error correction capability, the drive's implementation of an additional cross-checking code and algorithm double checks the main ECC correction and greatly decreases the likelihood of miscorrection.

The eighteen ECC check bytes shown in Figure 5-6 are used to detect and correct errors. The cross-checking and ECC data is computed and appended to the user data when the sector is first written.

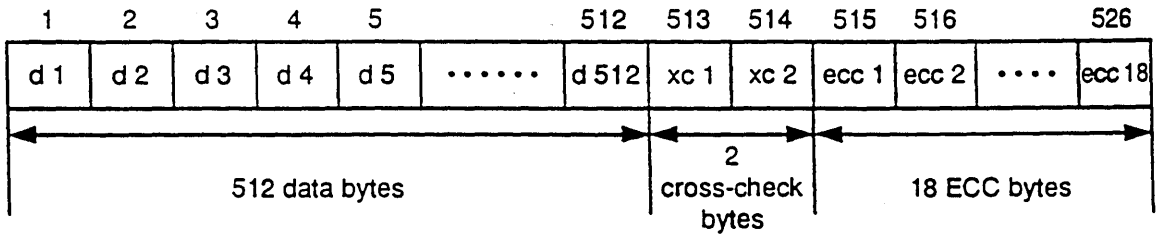


Figure 5-6 *Sector Data Field with ECC Check Bytes*

To obtain the ECC check byte values, each byte (including cross-checking and ECC bytes) within the sector is interleaved into one of three groups, where the first byte is in interleave 1, the second byte is in interleave 2, the third byte is in interleave 3, the fourth byte is in interleave 1, the fifth byte is in interleave 2, and so on, as shown in Figure 5-7.

Interleave 1 ⇨	d1	d4	• • • •	d508	d511	xc2	ecc3	ecc6	ecc9	ecc12	ecc15	ecc18
Interleave 2 ⇨	d2	d5	• • • •	d509	d512	ecc1	ecc4	ecc7	ecc10	ecc13	ecc16	
Interleave 3 ⇨	d3	d6	• • • •	d510	xc1	ecc2	ecc5	ecc8	ecc11	ecc14	ecc17	

Figure 5-7 *Byte Interleaving*

Note: ECC interleaving is not the same as the sector interleaving that is done on the disk.

Each of the three interleaves is encoded with six ECC bytes, resulting in the eighteen ECC bytes at the end of the sector. The two cross checking bytes are derived from all 512 data bytes. The combination of the interleaving and the nature of the ECC formulas enable the drive to know where the error occurs.

Because the ECC check bytes follow the cross checking bytes, errors found within the cross-checking bytes can be corrected. Due to the power and sophistication of the code, errors found within the ECC check bytes can also be corrected.

Each time a sector of data is read, the Quantum Vortex 1275/2550AT drives will generate a new set of ECC check bytes and cross-checking bytes from the user data. These new check bytes are compared to the ones originally written to the disk. The difference between the newly computed and original check bytes is reflected in a set of eighteen *syndromes* and two cross checking syndromes, which corresponds to the number of check bytes. If all of the syndrome values equal zero, the data was read with no errors, and the sector is transferred to the host system. If any of the syndromes do not equal zero, an error has occurred. The type of correction the drive applies depends on the nature and the extent of the error.

High speed on-the-fly error correction saves several milliseconds on each single-, or double- burst error, because there is no need to wait for a disk revolution to bring the sector under the head for re-reading.

Correction of Single-, or Double-Burst Errors On-the-Fly

Single-burst errors may have up to three erroneous bytes (24 bits) within a sector, provided that two bytes of the three must occur in a different interleave.

The Quantum Vortex 1275/2550AT drives have the capability to correct double-burst errors on-the-fly as well. Double-burst errors can be simply viewed as two spans of errors within one sector. More specifically, correctable double-burst errors must have two or fewer erroneous bytes per interleave.

The drive's Reed-Solomon ECC corrects double-burst errors up to 48 bits long, (provided that the error consists of two or fewer bytes residing in each of the interleaves).

Double-Burst Error Examples

In the example shown in Figure 5-8 C, the 42-bit error is uncorrectable since it occupies more than two erroneous bytes per interleave.

The other two 48-bit errors, shown in Figure 5-8 A and B, are correctable because no more than two error bytes of the entire error reside in any one of the interleaves.

Note: Any 41-bit error burst can be corrected on-the-fly using double-burst error correction because no more than two bytes can occupy each interleave.

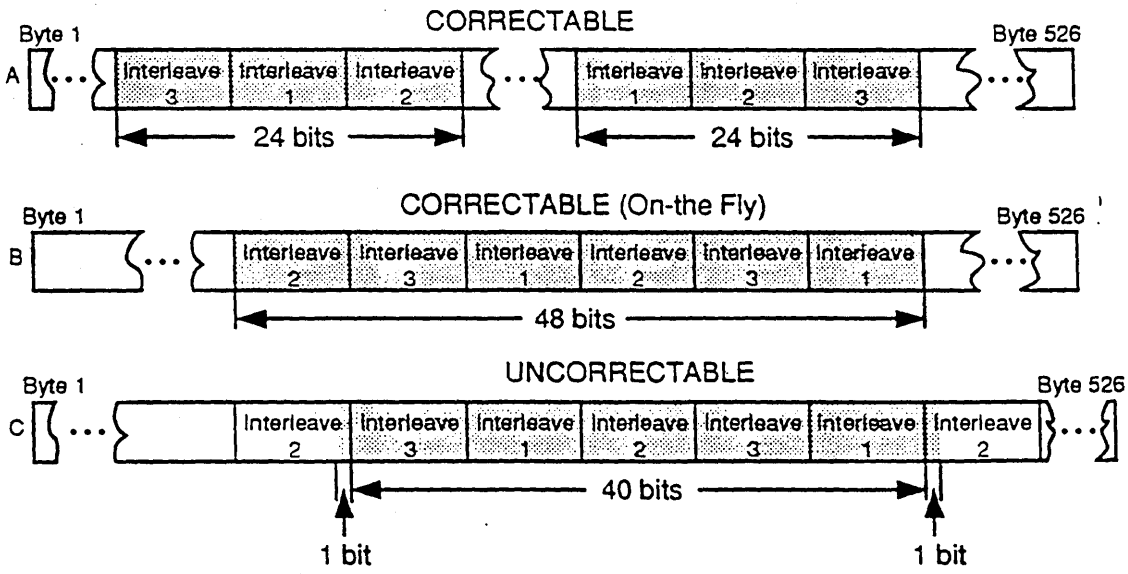


Figure 5-8 *Correctable and Uncorrectable Double-Burst Errors*

Correction of Triple-Burst Errors

Through sophisticated algorithms, Quantum Vortex 1275/2550AT drives have the capability to correct triple-burst errors, even though the probability of their occurrence is low. Triple-burst errors can be simply viewed as three spans of errors within one sector. More specifically, correctable triple-burst errors must have three or fewer erroneous bytes per interleave, and will not be corrected on-the-fly.

The drive's Reed-Solomon ECC corrects triple-burst errors up to 72 bits long, (provided that the error consists of three or fewer bytes residing in each of the interleaves).

If the triple-burst correction is successful, the data from the sector can be written to a spare sector and the logical address will be mapped to the new physical location.

Triple-Burst Error Examples

In the example shown in Figure 5-9 C, the 66-bit error is uncorrectable since it occupies more than three erroneous bytes per interleave.

The other two 72-bit errors, shown in Figure 5-9 A and B, are correctable because no more than two error bytes of the entire error reside in any one of the interleaves.

Note: Any 65-bit error burst can be corrected using triple-burst error correction because no more than three bytes can occupy each interleave.

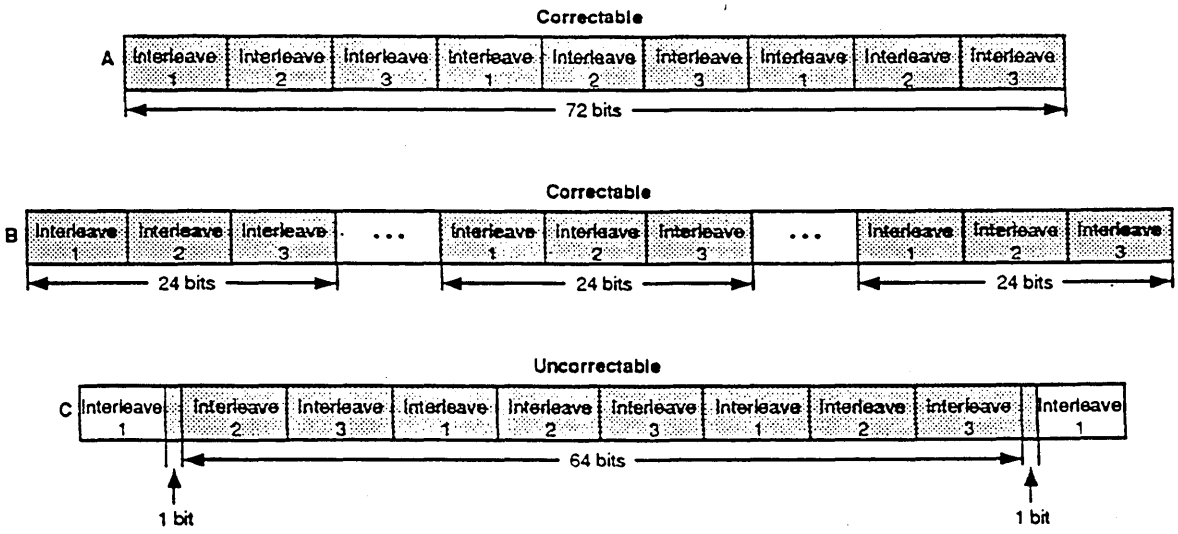


Figure 5-9 *Correctable and Uncorrectable Triple-Burst Errors*

Multiple Random Burst Errors

The drive's ECC can correct up to 72 bits of multiple random errors, provided that the incorrect bytes follow the guidelines for correctable triple-burst errors. Up to 48 bits of multiple random errors can be corrected on-the-fly, provided that the incorrect bytes follow the guidelines for correctable double-burst errors. Up to 24 bits of multiple random errors can be corrected on-the-fly if two bytes per interleave contains an error. If more than three bytes in any one interleave are in error, the sector cannot be corrected. Figure 5-10 shows an example of a correctable random burst error consisting of 9 bytes (72 bits). This random burst error is correctable because no more than three bytes within each interleave are in error.

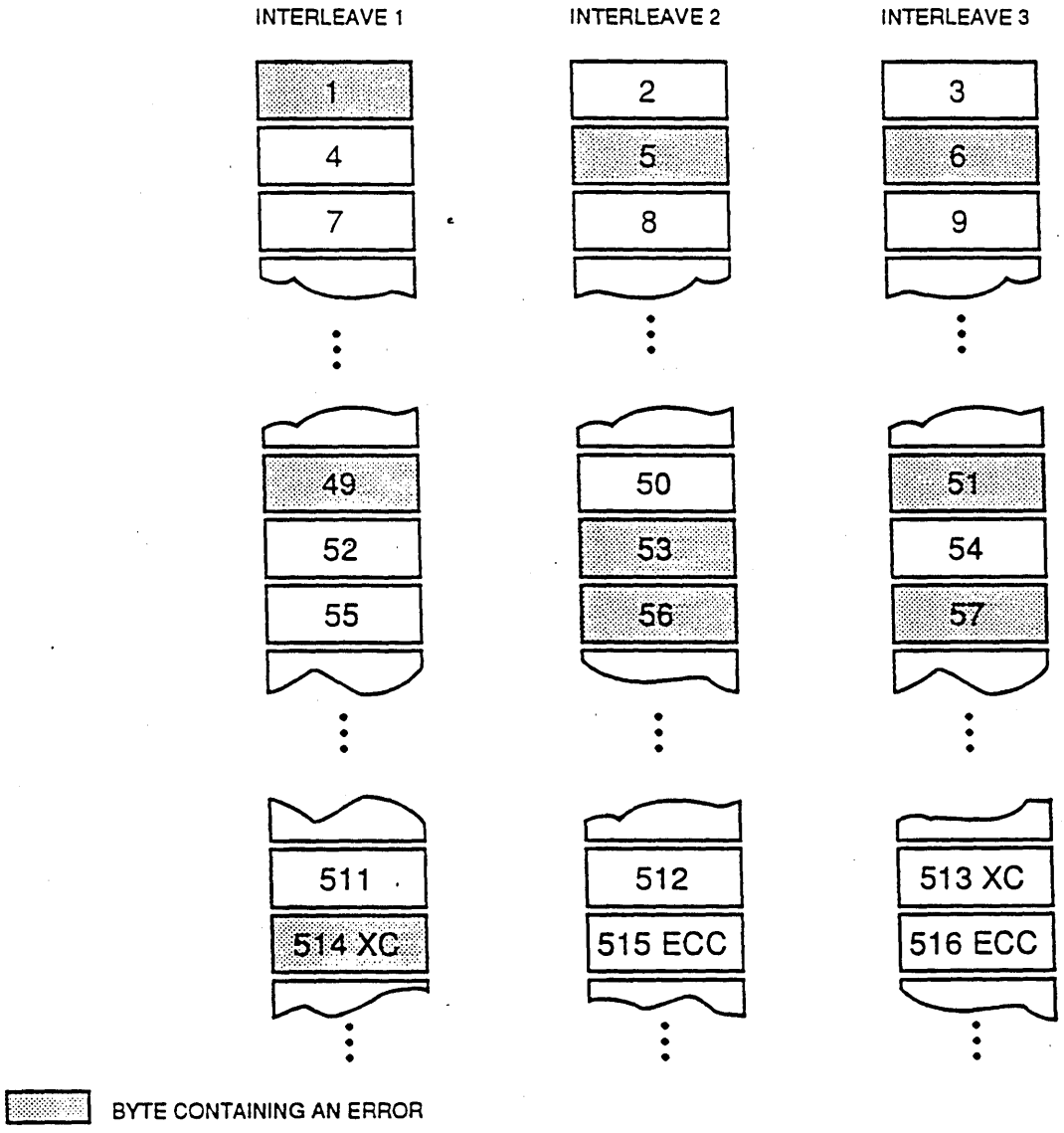


Figure 5-10 *Nine Correctable Random Burst Errors*

5.5.3.2 ECC Error Handling

When a data error occurs, the Quantum Vortex 1275/2550AT hard disk drive checks to see if the error is correctable on-the-fly. This process takes about 200 µs. If the error is correctable on-the-fly, the error is corrected and the data is transferred to the host system.

If the data is not correctable on-the-fly, the sector is re-read in an attempt to read the data correctly without applying the triple-burst ECC correction. Before invoking the complex triple-burst ECC algorithm, the drive will always try to recover from an error by attempting to re-read the data correctly. This strategy prevents invoking correction on non-repeatable errors. Each time a sector in error is re-read a set of ECC syndromes is computed. If all of the syndrome values equal zero, the data was read with no errors, and the sector is transferred to the host system. If any of the syndrome values do not equal zero, an error has occurred, the syndrome values are retained, and another re-read is invoked.

Note: Non-repeatable errors are usually related to the signal to noise ratio of the system. They are not due to media defects.

When the sets of syndromes from two consecutive re-reads are the same, a stable syndrome has been achieved. This event may be significant depending on whether the automatic read reallocation or early correction features have been enabled. If the early correction feature has been enabled and a stable syndrome has been achieved, triple-burst ECC correction is applied, and the appropriate message is transferred to the host system (e.g., corrected data, etc.).

Note: These features can be enabled or disabled through the ATA Set Configuration command. The EEC bit enables early ECC triple-burst correction if a stable syndrome has been achieved before all of the re-reads have been exhausted. The ARR bit enables the automatic reallocation of defective sectors.

If the automatic read reallocation feature is enabled, the drive, when encountering triple-burst errors, will attempt to re-read up to 8 times the retry count set in the AT Configuration bytes.

Note: The Quantum Vortex 1275/2550AT drive is shipped from the factory with the automatic read reallocation feature enabled so that any new defective sectors can be easily and automatically reallocated for the average AT end user.

5.5.4 Defect Management

The Quantum Vortex 1275/2550AT drive allocates one sector per cylinder as a spare. In the factory, the media is scanned for defects. If a sector on a cylinder is found to be defective, the address of the sector is added to the drive's defect list. Sectors located physically subsequent to the defective sector are assigned logical block addresses such that a sequential ordering of logical blocks is maintained. This inline sparing technique is employed in an attempt to eliminate slow data transfer that would result from a single defective sector on a cylinder.

If more than one sector is found defective on a cylinder, the above inline sparing technique is applied to the first sector only. The remaining defective sectors are replaced with the nearest available spare sectors on nearby cylinders. Such an assignment of additional replacement sectors from nearby sectors rather than having a central pool of spare sectors is an attempt to minimize the motion of the actuator and head that otherwise would be needed to find a replacement sector. The result is minimal reduction of data throughput.

Defects that occur in the field are known as *grown* defects. If such a defective sector is found in the field, the sector is reallocated according to the same algorithm used at the factory for those sectors that are found defective *after* the first defective sector on a cylinder; that is, inline sparing is not performed on these grown defects. Instead, the sector is reallocated to an available spare sector on a nearby cylinder.

Sectors are considered to contain grown defects if the triple-burst ECC algorithm must be applied to recover the data. If this algorithm is successful, the corrected data is stored in the newly allocated sector. If the algorithm is not successful, the erroneous data is stored in the newly allocated sector, and a flag is set in the data ID field that causes the drive to report an ECC error each time the sector is read. This condition remains until the sector is rewritten.

Chapter 6
IDE BUS INTERFACE AND ATA COMMANDS

This chapter describes the interface between Quantum Vortex 1275/2550AT hard disk drives and the IDE bus. The commands that are issued from the host to control the drive are listed, as well as the electrical and mechanical characteristics of the interface.

6.1 INTRODUCTION

Quantum Vortex 1275/2550AT hard disk drives use the standard IBM PC IDE bus interface, and are compatible with systems that provide an IDE interface connector on the motherboard. It may also be used with a third-party adapter board in systems that do not have a built-in IDE adapter. The adapter board plugs into a standard 16-bit expansion slot in an AT-compatible computer. A cable connects the drive to the adapter board.

6.2 SOFTWARE INTERFACE

The Quantum Vortex 1275/2550AT drives are controlled by the Basic Input/Output System (BIOS) program residing in an IBM PC AT, or compatible PC. The BIOS communicates directly with the drive's built-in controller. It issues commands to the drive and receives status information from the drive.

6.3 MECHANICAL DESCRIPTION

6.3.1 Drive Cable and Connector

The hard disk drive connects to the host computer by means of a cable. This cable has a 40-pin connector that plugs into the drive, and a 40-pin connector that plugs into the host computer. At the host end, the cable plugs into either an adapter board residing in a host expansion slot or an on-board IDE adapter.

If two drives are connected by a cable with two 40-pin drive connectors, the cable-select feature of the Quantum Vortex 1275/2550AT drive automatically configures each as either drive 0 or drive 1 depending on the configuration of pin 28 on the connector. See Section 3.3.1, "Cable Select (CS) Jumper," for more information about the cable select jumper.

3.3.2

6.4 ELECTRICAL INTERFACE

6.4.1 IDE Bus Interface

A 40-pin IDE interface connector on the motherboard or an adapter board provides an interface between the drive and a host that uses an IBM PC AT bus. The IDE interface contains bus drivers and receivers compatible with the standard AT bus. The AT-bus interface signals D8–D15, INTRQ, and IOCS16– require the IDE adapter board to have an extended I/O-bus connector.

The IDE interface buffers data and control signals between the drive and the AT bus of the host system, and decodes addresses on the host address bus. The Command Block Registers on the drive accept commands from the host system BIOS.

Note: Some host systems do not read the Status Register after the drive issues an interrupt. In such cases, the interrupt may not be acknowledged. To overcome this problem, you may have to configure a jumper on the motherboard or adapter board to allow interrupts to be controlled by the drive's interrupt logic. Read your motherboard or adapter board manual carefully to find out how to do this.

6.4.1.1 Electrical Characteristics

All signals are transistor-transistor logic (TTL) compatible—with logic 1 greater than 2.0 volts and less than 5.25 volts; and logic 0 greater than 0.0 volts and less than 0.8 volts. Neither the adapter board, motherboard interface, or drives require terminating resistors.

6.4.1.2 Drive Signals

The drive connector (J1, section C) connects the drive to an adapter board or onboard IDE adapter in the host computer. J1, section C is a 40-pin shrouded connector with two rows of 20 pins on 100-mil centers. J1 has been keyed by removing pin 20. The connecting cable is a 40-conductor flat ribbon cable, with a maximum length of 18 inches.

Table 6-1 describes the signals on the drive connector (J1, section C). The drive does not use all of the signals provided by the IDE bus. Table 6-2 shows the relationship between the drive connector (J1, section C) and the IDE bus.

Note: In Table 6-1, the following conventions apply:

A minus sign follows the name of any signal that is asserted as active low.
Direction (DIR) is in reference to the drive.
IN indicates input to the drive.
OUT indicates output from the drive.
I/O indicates that the signal is bidirectional.

Table 6-1 *Drive Connector Pin Assignments (J1, Section C)*

SIGNAL	NAME	DIR	PIN	DESCRIPTION
Reset	RESET–	IN	1	Drive reset signal from the host system, inverted on the adapter board or motherboard. Asserted for at least 300 ns during start up and deasserted thereafter, unless some event subsequently requires that the drive be reset.
Ground	Ground	—	2	Ground between the host system and the drive.
Data Bus		I/O	3–18	An 8/16-bit, bidirectional data bus between the host and the drive. D0–D7 are used for 8-bit transfers, such as registers and ECC bytes.
	DD0		17	Bit 0
	DD1		15	Bit 1
	DD2		13	Bit 2
	DD3		11	Bit 3
	DD4		9	Bit 4
	DD5		7	Bit 5
	DD6		5	Bit 6
	DD7		3	Bit 7
	DD8		4	Bit 8
	DD9		6	Bit 9
	DD10		8	Bit 10
	DD11		10	Bit 11
	DD12		12	Bit 12
	DD13		14	Bit 13
	DD14		16	Bit 14
	DD15		18	Bit 15
Ground	Ground	—	19	Ground between the host system and the drive.
Keypin	KEYPIN	—	20	Pin removed to key the interface connector.
DMA Request	DMARQ	OUT	21	Asserted by the drive when it is ready to exchange data with the host. The direction of the data transfer is determined by DIOW– and DIOR–. DMARQ is used in conjunction with DMACK–
Ground	Ground	—	22	Ground between the host system and the drive.
I/O Write	DIOW–	IN	23	The rising edge of this write strobe provides a clock for data transfers from the host data bus (DD0–DD7 or DD0–DD15) to a register or to the drive's data port.
Ground	Ground	—	24	Ground between the host system and the drive.

Table 6-1 *Drive Connector Pin Assignments (J1, Section C) (Continued)*

SIGNAL	NAME	DIR	PIN	DESCRIPTION
I/O Read	DIOR–	IN	25	The rising edge of this read strobe provides a clock for data transfers from a register or the drive's data port to the host data bus (DD0–DD7 or DD0–DD15). The rising edge of DIOR– latches data at the host.
Ground	Ground	—	26	Ground between the host system and the drive.
I/O Channel Ready	IORDY	OUT	27	When the drive is not ready to respond to a data transfer request, the IORDY signal is asserted active low to extend the host transfer cycle of any host register read or write access. When IORDY is deasserted, it is in a high-impedance state and it is the host's responsibility to pull this signal up to a high level (if necessary).
Cable Select (Quantum specific)		—	28	This is a Quantum-specific signal from the host that allows the drive to be configured as drive 0 when the signal is 0 (grounded), and as drive 1 when the signal is 1 (high).
DMA Acknowledge	DACK1–	IN	29	Used by the host to respond to the drive's DMARQ signal. DMARQ signals that there is more data available for the host.
Ground	Ground	—	30	Ground between the host system and the drive.
Interrupt Request	INTRQ	OUT	31	An interrupt to the host system. Asserted only when the drive microprocessor has a pending interrupt, the drive is selected, and the host clears nIEN in the Device Control Register. When nIEN is a 1 or the drive is not selected, this output signal is in a high-impedance state, regardless of the presence or absence of a pending interrupt. INTRQ is deasserted by an assertion of RESET–, the setting of SRST in the Device Control Register, or when the host writes to the Command Register or reads the Status Register. When data is being transferred in programmed I/O (PIO) mode, INTRQ is asserted at the beginning of each data block transfer. Exception: INTRQ is not asserted at the beginning of the first data block transfer that occurs when any of the following commands executes: FORMAT TRACK, Write Sector, WRITE BUFFER, or WRITE LONG.

Table 6-1 *Drive Connector Pin Assignments (J1, Section C) (Continued)*

SIGNAL	NAME	DIR	PIN	DESCRIPTION
16-Bit I/O	IOCS16–	OUT	32	An open-collector output signal. Indicates to the host system that the 16-bit data port has been addressed and that the drive is ready to send or receive a 16-bit word. When transferring data in PIO mode, if IOCS16– is not asserted, D0–D7 are used for 8-bit transfers; if IOCS16– is asserted, D0–D15 are used for 16-bit data transfers.
Drive Address Bus				A 3-bit, binary-coded address supplied by the host when accessing a register or the drive's data port.
Bit 1	DA1	IN	33	
Bit 0	DA0	IN	35	
Bit 2	DA2	IN	36	
Passed Diagnostics	PDIAG–	I/O	34	Drive 0 (Master) monitors this Drive 1 (Slave) open-collector output signal, which indicates the result of a diagnostics command or reset. Each drive has a 10K pull-up resistor on this signal. Following the receipt of a power-on reset, software reset, or RESET– drive 1 negates PDIAG– within 1 ms. PDIAG– indicates to drive 0 that drive 1 is busy (BSY=1). Then, drive 1 asserts PDIAG– within 30 seconds, indicating that drive 1 is no longer busy (BSY=0) and can provide status information. Following the assertion of PDIAG–, drive 1 is unable to accept commands until drive 1 is ready (DRDY=1)—that is, until the reset procedure for drive 1 is complete. Following the receipt of a valid EXECUTE DRIVE DIAGNOSTIC command, drive 1 negates PDIAG– within 1 ms, indicating to drive 0 that it is busy and has not yet passed its internal diagnostics. If drive 1 is present, drive 0 waits for drive 1 to assert PDIAG– for up to 5 seconds after the receipt of a valid EXECUTE DRIVE DIAGNOSTIC command. Since PDIAG– indicates that drive 1 has passed its internal diagnostics and is ready to provide status, drive 1 clears BSY prior to asserting PDIAG–. If drive 1 fails to respond during reset initialization, drive 0 reports its own status after completing its internal diagnostics. Drive 0 is unable to accept commands until drive 0 is ready (DRDY=1)—that is, until the reset procedure for drive 0 is complete.

Table 6-1 *Drive Connector Pin Assignments (J1, Section C) (Continued)*

SIGNAL	NAME	DIR	PIN	DESCRIPTION
Chip Select 0	CS1FX–	IN	37	Chip-select signal decoded from the host address bus. Used to select the host-accessible Command Block Registers.
Chip Select 1	CS3FX–	IN	38	Chip select signal decoded from the host address bus. Used to select the host-accessible Control Block Registers.
Drive Active/Slave Present	DASP–	I/O	39	A time-multiplexed signal that indicates either drive activity or that drive 1 is present. During power-on initialization, DASP– is asserted by drive 1 within 400 ms to indicate that drive 1 is present. If drive 1 is not present, drive 0 asserts DASP– after 450 ms to light the drive-activity LED. An open-collector output signal, DASP– is deasserted following the receipt of a valid command by drive 1 or after the drive is ready, whichever occurs first. Once DASP– is deasserted, either hard drive can assert DASP– to light the drive-activity LED. Each drive has a 10K pull-up resistor on this signal. If an external drive-activity LED is used to monitor this signal, an external resistor must be connected in series between the signal and a +5 volt supply in order to limit the current to 24 mA maximum.
Ground	Ground	—	40	Ground between the host system and the drive.

6.4.1.3 IDE Bus Signals

See Table 6-2 for the relationship between the drive signals and the IDE bus.

Table 6-2 *Relationship of Drive Signals to the IDE Bus*

DRIVE CONNECTOR (J1)		DIRECTION	IDE BUS	
1	RESET–	<—(INV)	B2	RESET DRV
2	GROUND	—	—	GROUND
3	DD7	<—>	A2	SD7
4	DD8	<—>	C11	SD8
5	DD6	<—>	A3	SD6
6	DD9	<—>	C12	D9
7	DD5	<—>	A4	SD5
8	DD10	<—>	C13	SD10
9	DD4	<—>	A5	SD4
10	DD11	<—>	C14	SD11
11	DD3	<—>	A6	SD3
12	DD12	<—>	C15	SD12
13	DD2	<—>	A7	SD2
14	DD13	<—>	C16	SD13
15	DD1	<—>	A8	SD1
16	DD14	<—>	C17	SD14
17	DD0	<—>	A9	SD0
18	DD15	<—>	C18	SD15
19	GROUND	—	—	GROUND
20	KEYPIN	—	—	NO CONNECTION
21	DMARQ	—>	—[1]	DRQ
22	GROUND	—	—	GROUND
23	DIOW–	<—	B13	DIOW–
24	GROUND	—	—	GROUND
25	DIOR–	<—	B14	IOR–
26	GROUND	—	—	GROUND
27	IORDY	—>	A10	I/O CH RDY
28	CABLE SELECT	<—	—[2]	NO CONNECTION
29	DMACK–	<—	—[3]	DACK–
30	GROUND	—	—	GROUND
31	INTRQ	—>	D7	INTRQ
32	IOCS16–	—>	D2	I/O CS16–
33	ADDR1	<—	A30	SA1
34	PDIAG–	—	—	NO CONNECTION
35	DA0	<—	A31	SA0
36	ADDR2	<—	A29	SA2
37	CS1FX–	<—	—[4]	CS0–
38	CS3FX–	<—	—[4]	CS1–
39	DASP–	—	—[4]	NO CONNECTION
40	GROUND	—	—	GROUND

1. DMARQ from the drive must be jumpered to one of the DRQ lines on the motherboard or host adapter (normally connected to DRQ6).
2. Pin 28 is a vendor-specific pin that Quantum is using for a specific purpose. See Chapter 3 for details.
3. DACK– from the drive must be jumpered to one of the DACK– lines on the motherboard or host adapter (normally connected to DACK6–).
4. CS1FX–, CS3FX–, and DASP– originate on the adapter board.

6.4.2 Host Interface Timing

6.4.2.1 Programmed I/O (PIO) Transfer Mode

The PIO host interface timing shown in Table 6-3 is in reference to signals at 0.8 volts and 2.0 volts. All times are in nanoseconds, unless otherwise noted. Figure 6-1 provides a timing diagram.

Table 6-3 *PIO Host Interface Timing*

SYMBOL	DESCRIPTION	MIN/MAX	MODE 4[1] (local bus)	QUANTUM VORTEX AT
t0	Cycle Time	min	120	120
t1	Address Valid to DIOW–/DIOR–Setup	min	25	25
t2	DIOW–/DIOR– Pulsewidth (8- or 16-bit)	min	70	70
t2i	DIOW–/DIOR– Negated Pulsewidth	min	25	25
t3	DIOW–Data Setup	min	20	20
t4	DIOW– Data Hold	min	10	10
t5	DIOR– Data Setup	min	20	20
t5a	DIOR– to Data Valid	max	—	—
t6	DIOR– Data Hold	min	5	5
t6z	DIOR– Data Tristate	max	30	30
t7	Address Valid to IOCS16– Assertion	max	N/A	N/A
t8	Address Valid to IOSC16– Deassertion	max	N/A	N/A
t9	DIOW–/DIOR– to Address Valid Hold	min	10	10
tA	IORDY[2] Setup Time	min	35	35
tB	IORDY Pulse Width	max	1250	1250
tR	Read Data Valid to IORDY active (if IORDY is initially low after tA)	min	0	0

1. ATA Mode 4 timing is listed for reference only.
2. Transfer rates above 6 MB/s require the use of IORDY.

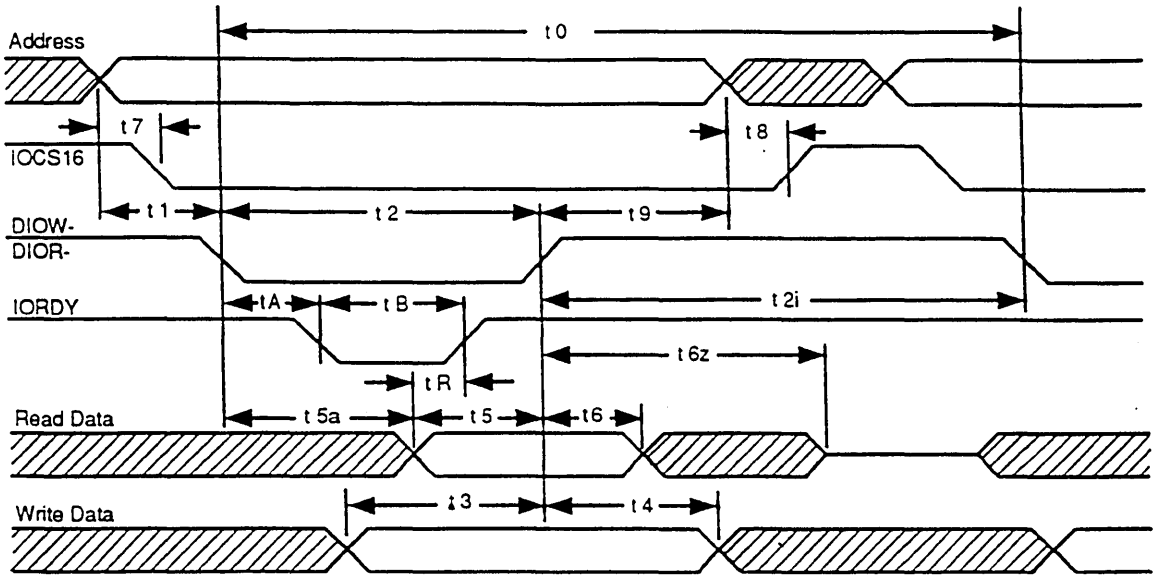


Figure 6-1 *PIO Interface Timing*

6.4.2.2 Multiword DMA Transfer Mode

The multiword DMA host interface timing shown in Table 6-4 is in reference to signals at 0.8 volts and 2.0 volts. All times are in nanoseconds, unless otherwise noted. Figure 6-2 provides a timing diagram.

Table 6-4 *Multiword DMA Host Interface Timing*

SYMBOL	DESCRIPTION	MIN/MAX	MODE 2[1] (local bus)	QUANTUM VORTEX AT
t0	Cycle Time	min	120	120
tD	DIOR–/DIOW– Pulsewidth	min	70	70
tE	DIOR– to Data Valid	max	–	–
tF	DIOR– Data Hold	min	5	5
tFz	DIOR– Data Tristate[2]	max	20	20
tG	DIOW– Data Setup	min	20	20
tH	DIOW– Data Hold	min	10	10
tI	DMACK to DIOR–/DIOW– Setup	min	0	0
tJ	DIOR–/DIOW– to DMACK– Hold	min	5	5
tK	DIOR–/DIOW– Negated Pulsewidth	min	25	25
tL	DIOR–/DIOW– to DMARQ Delay	max	35	35
tz	DMACK– Data Tristate[3]	max	25	25

1. ATA Mode 2 timing is listed for reference only.
2. The Quantum Vortex 1275/2550AT drive tristates after each word transferred.
3. Symbol tz only applies on the last tristate at the end of a multiword DMA transfer cycle.

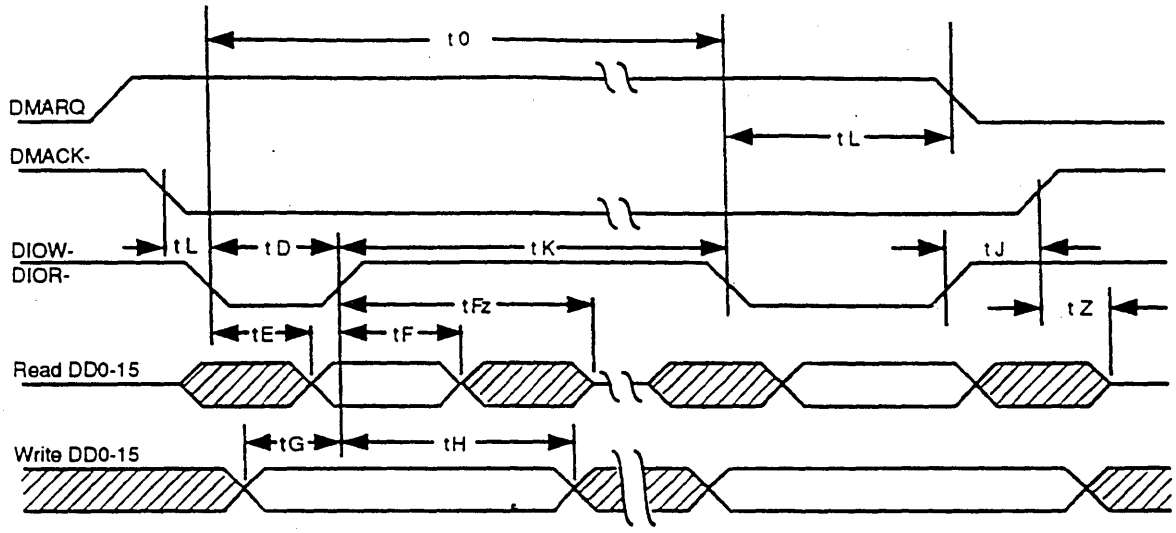


Figure 6-2 *Multiword DMA Bus Interface Timing*

6.4.2.3 Host Interface RESET Timing

The host interface RESET timing shown in Table 6-5 is in reference to signals at 0.8 volts and 2.0 volts. All times are in nanoseconds, unless otherwise noted. Figure 6-3 provides a timing diagram.

Table 6-5 *Host Interface RESET Timing*

SYMBOL	DESCRIPTION	MINIMUM	MAXIMUM
tM	RESET– Pulse width	300	—

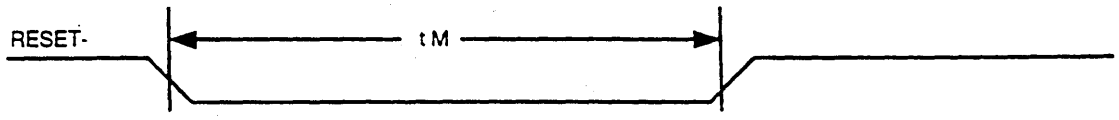


Figure 6-3 *Host Interface RESET Timing*

6.5 REGISTER ADDRESS DECODING

The host addresses the drive by using programmed I/O. Host address lines A0–A2, chip-select CS1FX– and CS3FX–, and IOR– and IOW– address the disk registers. Host address lines A3–A9 generate the two chip-select signals, CS1FX– and CS3FX–.

- Chip Select CS1FX– accesses the eight Command Block Registers.
- Chip Select CS3FX– is valid during 8-bit transfers to or from the Alternate Status Register.

The drive selects the primary or secondary command block addresses by setting Address bit A7.

Data bus lines 8–15 are valid only when IOCS16– is active and the drive is transferring data. The drive transfers ECC information only on data bus lines 0–7. Data bus lines 8–15 are invalid during transfers of ECC information.

I/O to or from the drive occurs over an I/O port that routes input or output data to or from selected registers, by using the following encoded signals from the host: CS1FX–, CS3FX–, DA2, DA1, DA0, DIOR–, and DIOW–. The host writes to the Command Block Registers when transmitting commands to the drive, and to the Control Block Registers when transmitting control, like a software reset. Table 6-6 lists the selection addresses for these registers.

Table 6-6 *I/O Port Functions and Selection Addresses*

FUNCTION		HOST SIGNALS				
CONTROL BLOCK REGISTERS		CS1FX–	CS3FX–	DA2	DA1	DA0
READ (DIOR–)	WRITE (DIOW–)					
Data Bus High Impedance	Not Used	N[1]	N	X[2]	X	X
Data Bus High Impedance	Not Used	N	A[3]	0	X	X
Data Bus High Impedance	Not Used	N	A	1	0	X
Alternate Status	Device Control	N	A	1	1	0
Drive Address	Not Used	N	A	1	1	1
COMMAND BLOCK REGISTERS						
READ (DIOR–)	WRITE (DIOW–)					
Data Port	Data Port	A	N	0	0	0
Error Register	Features	A	N	0	0	1
Sector Count	Sector Count	A	N	0	1	0
Sector Number[4]	Sector Number	A	N	0	1	1
LBA Bits 0–7[5]	LBA Bits 0–7	A	N	0	1	1
Cylinder Low[4]	Cylinder Low	A	N	1	0	0
LBA Bits 8–15[5]	LBA Bits 8–15	A	N	1	0	0
Cylinder High[4]	Cylinder High	A	N	1	0	1
LBA Bits 16–23[5]	LBA Bits 16–23	A	N	1	0	1
Drive/Head[4]	Drive/Head	A	N	1	1	0
LBA Bits 24–27[5]	LBA Bits 24–27	A	N	1	1	0
Status	Command	A	N	1	1	1
Invalid Address	Invalid Address	A	A	X	X	X

1. N = signal deasserted
2. X = signal either asserted or deasserted
3. A = signal asserted
4. Mapping of registers in CHS mode
5. Mapping of registers in LBA mode

After power on or following a reset, the drive initializes the Command Block Registers to the values shown in Table 6-7.

Table 6-7 *Command Block Register Initial Values*

REGISTER	VALUE
Error Register	01
Sector Count Register	01
Sector Number Register	01
Cylinder Low Register	00
Cylinder High Register	00
Drive/Head Register	00

6.6 REGISTER DESCRIPTIONS

The Quantum Vortex 1275/2550AT hard disk drive emulates the ATA Command and Control Block Registers. Functional descriptions of these registers are given in the next two sections.

6.6.1 Control Block Registers

6.6.1.1 Alternate Status Register

The Alternate Status Register contains the same information as the Status Register in the command block. Reading the Alternate Status Register does not imply the acknowledgment of an interrupt by the host or clear a pending interrupt. See the description of the Status Register in section 6.6.2.8 for definitions of bits in this register.

6.6.1.2 Device Control Register

This write-only register contains two control bits, as shown in Table 6-8.

Table 6-8 *Device Control Register Bits*

BIT	MNEMONIC	DESCRIPTION
7	Reserved	–
6	Reserved	–
5	Reserved	–
4	Reserved	–
3	1	Always 1
2	SRST[1]	Host software reset bit
1	nIEN[2]	Drive interrupt enable bit
0	0	Always 0

1. SRST = Host Software Reset bit. When the host sets this bit, the drive is reset. When two drives are daisy-chained on the interface, this bit resets both drives simultaneously.
2. nIEN = Drive Interrupt Enable bit. When nIEN equals 0 or the host has selected the drive, the drive enables the host interrupt signal INTRQ through a tristate buffer to the host. When nIEN equals 1 or the drive is not selected, the host interrupt signal INTRQ is in a high-impedance state, regardless of the presence or absence of a pending interrupt.

6.6.1.3 Drive Address Register

The Drive Address Register returns the head-select addresses for the drive currently selected. Table 6-9 shows the Drive Address bits.

Table 6-9 *Drive Address Register Bits*

BIT	MNEMONIC	DESCRIPTION
7	HiZ[1]	High Impedance bit
6	nWTG[2]	Write Gate bit
5	nHS3[3]	Head Address msb
4	nHS2	–
3	nHS1	–
2	nHS0	Head Address lsb
1	nDS1[4]	Drive 1 Select bit
0	nDS0	Drive 0 Select bit

1. HiZ = High Impedance bit. When the host reads the register, this bit will be in a high impedance state.
2. nWTG = Write Gate bit. When a write operation to the drive is in progress, nWTG equals 0.
3. nHS0–nHS3 = Head Address bits. These bits are equivalent to the one's complement of the binary-coded address of the head currently selected.
4. nDS0–nDS1 = Drive Select bits. When drive 1 is selected, nDS1 equals 0. When drive 0 is selected, nDS0 equals 0.

6.6.2 Command Block Registers

6.6.2.1 Data Port Register

All data transferred between the device data buffer and the host passes through the Data Port Register. The host transfers the sector table to this register during execution of the FORMAT TRACK command. Transfers of ECC bytes during the execution of READ LONG or WRITE LONG commands are 8-bit transfers.

6.6.2.2 Error Register

The Error Register contains status information about the last command executed by the drive. The contents of this register are valid only when the Error bit (ERR) in the Status Register is set to 1. The contents of the Error Register are also valid at power on, and at the completion of the drive's internal diagnostics, when the register contains a status code. When the error bit in the Status Register is set to 1, the host interprets the Error Register bits as shown in Table 6-10.

Table 6-10 *Error Register Bits*

MNEMONIC	BIT	DESCRIPTION
BBK	7	Bad block detected in the required sector's ID field.
UNC	6	Uncorrectable data error encountered.
–	5	Not used.
IDNF	4	Requested sector's ID field not found.
–	3	Not used.
ABRT	2	Requested command aborted due to a drive status error, such as Not Ready or Write Fault, or because the command code is invalid.
TK0NF	1	Track 0 not found during execution of RECALIBRATE command.
AMNF	0	Data Address Mark not found after correct ID field format.

6.6.2.3 Sector Count Register

The Sector Count Register defines the number of sectors of data to be transferred across the host bus for a subsequent command. If the value in this register is 0, the sector count is 256 sectors. If the Sector Count Register command executes successfully, the value in this register at command completion is 0. As the drive transfers each sector, it decrements the Sector Count Register to reflect the number of sectors remaining to be transferred. If the command's execution is unsuccessful, this register contains the number of sectors that must be transferred to complete the original request.

When the drive executes an INITIALIZE DRIVE PARAMETERS or Format Track command, the value in this register defines the number of sectors per track.

6.6.2.4 Sector Number Register

The Sector Number Register contains the ID number of the first sector to be accessed by a subsequent command. The sector number is a value between one and the maximum number of sectors per track. As the drive transfers each sector, it increments the Sector Number Register. See the command descriptions in section 6.7 for information about the contents of the Sector Number Register after successful or unsuccessful command completion.

In LBA mode, this register contains bits 0 to 7. At command completion, the host updates this register to reflect the current LBA bits 0 to 7.

6.6.2.5 Cylinder Low Register

The Cylinder Low Register contains the eight low-order bits of the starting cylinder address for any disk access. On multiple sector transfers that cross cylinder boundaries, the host updates this register when command execution is complete, to reflect the current cylinder number. The host loads the least significant bits of the cylinder address into the Cylinder Low Register.

In LBA mode, this register contains bits 8 to 15. At command completion, the host updates this register to reflect the current LBA bits 8 to 15.

6.6.2.6 Cylinder High Register

The Cylinder High Register contains the eight high-order bits of the starting cylinder address for any disk access. On multiple sector transfers that cross cylinder boundaries, the host updates this register at the completion of command execution, to reflect the current cylinder number. The host loads the most significant bits of the cylinder address into the Cylinder High Register.

In LBA mode, this register contains bits 16 to 23. At command completion, the host updates this register to reflect the current LBA bits 16 to 23.

6.6.2.7 Drive/Head Register

The Drive/Head Register contains the drive ID number and its head numbers. By executing the INITIALIZE DRIVE PARAMETERS command, the host defines the contents of the Drive/ Head Register.

In LBA mode, this register contains bits 24 to 27. At command completion, the host updates this register to reflect the current LBA bits 24 to 27.

Table 6-11 shows the Drive/Head Register bits.

Table 6-11 *Drive Head Register Bits*

MNEMONIC	BIT	DESCRIPTION
Reserved	7[1]	Always *1*
L	6[2]	*0* for CHS mode *1* for LBA mode
Reserved	5	Always *1*
DRV	4[3]	*0* indicates the Master drive is selected *1* indicates the Slave drive is selected
HS3	3[4]	Most significant Head Address bit in CHS mode Bit 24 of the LBA Address in LBA mode
HS2	2	Head Address bit for CHS mode Bit 25 of the LBA Address in LBA mode
HS1	1	Head Address bit for CHS mode Bit 26 of the LBA Address in LBA mode
HS0	0	Least significant Head Address bit in CHS mode Bit 27 of the LBA Address in LBA mode

1. Bits 5–7 define the sector size set in hardware (512 bytes).
2. Bit 6 is the binary encoded Address Mode Select. When bit 6 is set to 0, addressing is by CHS mode. When bit 6 is set to 1, addressing is by LBA mode.
3. Bit 4 (DRV) contains the binary encoded drive select number. The Master is the primary drive; the Slave is the secondary drive
4. In CHS mode, bits 3–0 (HS0–HS3) contain the binary encoded address of the selected head. At command completion, the host updates these bits to reflect the address of the head currently selected. In LBA mode, bits 3–0 (HS0–HS3) contain bits 24–27 of the LBA Address. At command completion, the host updates this register to reflect the current LBA bits 24 to 27.

6.6.2.8 Status Register

The Status Register contains information about the status of the drive and the controller. The drive updates the contents of this register at the completion of each command. When the Busy bit is set (BSY=1), no other bits in the Command Block Registers are valid. When the Busy bit is not set (BSY=0), the information in the Status Register and Command Block Registers is valid.

When an interrupt is pending, the drive considers that the host has acknowledged the interrupt when it reads the Status Register. Therefore, whenever the host reads this register, the drive clears any pending interrupt. Table 6-12 defines the Status Register bits.

6.6.2.9 Command Register

The host sends a command to the drive by means of an 8-bit code written to the Command Register. As soon as the drive receives the command in its Command Register, it begins execution of the command. Table 6-13 lists the hexadecimal command codes and parameters for each executable command. The code F0h is common to all of the extended commands. Each of these commands is distinguished by a unique subcode. For a detailed description of each command, see Section 6.7, "COMMAND DESCRIPTIONS," found later in this chapter.

Table 6-12 *Status Register Bits*

MNEMONIC	BIT	DESCRIPTION
BSY	7	**Busy bit.** Set by the controller logic of the drive whenever the drive has access to and the host is locked out of the Command Block Registers. BSY is set under the following conditions: • Within 400 ns after the deassertion of RESET- or after SRST is set in the Device Control Register. Following a reset, BSY will be set for no longer than 30 seconds. • Within 400 ns of a host write to the Command Block Registers with a Read, READ LONG, READ BUFFER, SEEK, RECALIBRATE, INITIALIZE DRIVE PARAMETERS, Read Verify, Identify Drive, or EXECUTE DRIVE DIAGNOSTIC command. • Within 5 µsec after the transfer of 512 bytes of data during the execution of a Write, Format Track, or WRITE BUFFER command, or 512 bytes of data and the appropriate number of ECC bytes during the execution of a WRITE LONG command. When BSY=1, the host cannot write to a Command Block Register and reading any Command Block Register returns the contents of the Status Register.
DRDY	6	**Drive Ready bit.** Indicates that the drive is ready to accept a command. When an error occurs, this bit remains unchanged until the host reads the Status Register, then again indicates that the drive is ready. At power on, this bit should be cleared, and should remain cleared until the drive is up to speed and ready to accept a command.
DWF	5	**Drive Write Fault bit.** When an error occurs, this bit remains unchanged until the host reads the Status Register, then again indicates the current write fault status.
DSC	4	**Drive Seek Complete bit.** This bit is set when a seek operation is complete and the heads have settled over a track. When an error occurs, this bit remains unchanged until the host reads the Status Register, when it indicates the current seek-complete status.
DRQ	3	**Data Request bit.** When set, this bit indicates that the drive is ready to transfer a word or byte of data from the host to the data port.
CORR	2	**Corrected Data bit.** The drive sets this bit when it encounters and corrects a correctable data error. This condition does not terminate a multi-sector read operation.
IDX	1	**Index bit.** This bit is set when the drive detects the index mark, once per disk revolution.
ERR	0	**Error bit.** When set, this bit indicates that the previous command resulted in an error. The other bits in the Status Register and the bits in the Error Register contain additional information about the cause of the error.

Table 6-13 *Quantum Vortex 1275/2550AT Command Codes and Parameters*

COMMAND		PARAMETER				
NAME	CODE	SC	SN	CY	DS	HD
RECALIBRATE	1Xh				V	
READ SECTORS, with retry	20h	V	V	V	V	V
READ SECTORS, no retry	21h	V	V	V	V	V
READ LONG, with retry	22h	V	V	V	V	V
READ LONG, no retry	23h	V	V	V	V	V
WRITE SECTORS, with retry	30h	V	V	V	V	V
WRITE SECTORS, no retry	31h	V	V	V	V	V
WRITE LONG, with retry	32h	V	V	V	V	V
WRITE LONG, no retry	33h	V	V	V	V	V
READ VERIFY SECTORS, with retry	40h	V	V	V	V	V
READ VERIFY SECTORS, no retry	41h	V	V	V	V	V
FORMAT TRACK	50h	V		V	V	V
SEEK	7Xh		V	V	V	V
EXECUTE DRIVE DIAGNOSTIC	90h					
INITIALIZE DRIVE PARAMETERS	91h	V			V	V
READ MULTIPLE	C4h	V	V	V	V	V
WRITE MULTIPLE	C5h	V	V	V	V	V
SET MULTIPLE MODE	C6h	V			V	
READ DMA, with retry	C8h	V	V	V	V	V
READ DMA, no retry	C9h	V	V	V	V	V
WRITE DMA, with retry	CAh	V	V	V	V	V
WRITE DMA, no retry	CBh	V	V	V	V	V
STANDBY IMMEDIATE	E0h					V
IDLE IMMEDIATE	E1h					V
STANDBY MODE (AUTO POWER-DOWN)	E2h	V				V
IDLE MODE (AUTO POWER-DOWN)	E3h	V				V
READ BUFFER	E4h				V	
CHECK POWER MODE	E5h	V				V
SLEEP MODE	E6h					V
WRITE BUFFER	E8h				V	
IDENTIFY DRIVE	ECh				V	
READ DEFECT LIST—extended cmnd.	F0h	V	V	V	V	V
READ CONFIGURATION—extended cmnd.	F0h	V	V	V	V	V
SET CONFIGURATION—extended cmnd.	F0h	V	V	V	V	V

Note: The following information applies to Table 6-13:

SC = Sector Count Register
SN = Sector Number Register
CY = Cylinder Low and High Registers
DS = Drive Select bit (Bit 4 of Drive/Head Register)
HD = 3 Head Select Bits (Bits 0–3 of Drive Head Register)

V = Must contain valid information for this command

6.7 COMMAND DESCRIPTIONS

The Quantum Vortex 1275/2550AT hard disk drive supports all standard ATA drive commands. The drive decodes, then executes, commands loaded into the Command Block Register. In applications involving two hard drives, both drives receive all commands. However, only the selected drive executes commands—with the exception of the EXECUTE DRIVE DIAGNOSTIC command, as explained below. The procedure for executing a command on the selected drive is as follows:

1. Wait for the drive to indicate that it is no longer busy (BSY=0).
2. Load the required parameters into the Command Block Register.
3. Activate the Interrupt Enable (–IEN) bit.
4. Wait for the drive to set RDY (RDY=1).
5. Write the command code to the Command Register.

Execution of the command begins as soon as the drive loads the Command Block Register. The remainder of this section describes the function of each command. The commands are listed in the same order they appear in Table 6-13.

6.7.1 Recalibrate

The RECALIBRATE command moves the read/write heads from any location on the disk to cylinder 0. On receiving this command, the drive sets the BSY bit and issues a seek command to cylinder 0. The drive then waits for the seek operation to complete, updates status, negates BSY, and generates an interrupt. If the drive cannot seek to cylinder 0, it posts the message TRACK 0 NOT FOUND.

6.7.2 Read Sectors

The Read Sectors command reads from 1 to 256 sectors, beginning at the specified sector. As specified in the Command Block Register, a sector count equal to 0 requests 256 sectors. When the drive accepts this command, it sets BSY and begins execution of the command.

6.7.2.1 Read Long

When the Long bit is set in the command code, a READ LONG command executes, returning the data and the ECC bytes contained in the data field of the requested sector. During a READ LONG operation, the drive does not check the ECC bytes to determine if a data error of any kind has occurred.

6.7.2.2 Multiple Sector Reads

Multiple sector reads set DRQ. After reading each sector, the drive generates an interrupt when the sector buffer is full and the drive is ready for the host to read the data. Once the host empties the sector buffer, the drive immediately clears DRQ and sets BSY.

If an error occurs during a multiple sector read, the read terminates at the sector in which the error occurred. The Command Block Register contains the cylinder, head, and sector numbers of the sector in which the error occurred. The host can then read the Command Block Register to determine what kind of error has occurred, and in which sector. Whether the data error is correctable or uncorrectable, the drive loads the data into the sector buffer.

6.7.3 Write Sector

The WRITE SECTOR command writes from 1 to 256 sectors, beginning at the specified sector. As specified in the Command Block Register, a sector count equal to 0 requests 256 sectors. When the drive accepts this command, it sets DRQ and waits for the host to fill the sector buffer with the data to be written to the drive. The drive does not generate an interrupt to start the first buffer-fill operation. Once the buffer is full, the drive clears DRQ, sets BSY, and begins execution of the command.

6.7.3.1 Write Long

When the Long bit is set in the command code, a WRITE LONG command writes the data and the ECC bytes directly from the sector buffer. The drive does not generate the ECC bytes itself.

6.7.3.2 Multiple Sector Writes

The MULTIPLE SECTOR WRITES command sets DRQ. The drive generates an interrupt whenever the sector buffer is ready to be filled. When the host fills the sector buffer, the drive immediately clears DRQ and sets BSY.

If an error occurs during a multiple sector write operation, the write operation terminates at the sector in which the error occurred. The Command Block Register contains the cylinder, head, and sector numbers of the sector in which the error occurred. The host can then read the Command Block Register to determine what kind of error has occurred, and in which sector.

6.7.4 Read Verify Sectors

The execution of the READ VERIFY SECTORS command is identical to that of the READ SECTORS command. However, the Read Verify command does not cause the drive to set DRQ, the drive transfers no data to the host, and the Long bit is invalid. On receiving the READ VERIFY command, the drive sets BSY. When the drive has verified the requested sectors, it clears BSY and generates an interrupt. On command completion, the Command Block Registers contain the cylinder, head, and sector numbers of the last sector verified.

If an error occurs during a multiple sector verify operation, the read operation terminates at the sector in which the error occurred. The Command Block Registers contain the cylinder, head, and sector numbers in which the error occurred.

6.7.5 Format Track

The host specifies the track addresses by writing to the Cylinder and Head Registers. When the drive accepts a FORMAT TRACK command, it sets the DRQ bit, then waits for the host to fill the sector buffer. When the buffer is full, the drive clears DRQ, sets BSY, and begins command execution. The contents of the sector buffer are not written to the disk, and may be ignored or interpreted as shown in Table 6-14.

Table 6-14 *Sector Buffer Contents*

DD15 — DD0		DD15 — DD0	
First Sector Descriptor	: : : : : : : : : : : : : :	Last Sector Descriptor	Remainder of buffer filled with zeros

On the Quantum Vortex 1275/2550AT hard disk drive, the FORMAT TRACK command writes zeros to the data fields in the sectors on the specified logical track. The drive writes no headers at these locations. The Sector Count register contains the number of sectors per track.

One 16-bit word represents each sector (the words are contiguous from the start of the sector).

Note: Any words remaining in the buffer after the representation of the last sector must be filled with zeros.

DD15–8 contain the sector number. DD7–0 contain a descriptor value that is defined below. The words must appear in sequential order starting at sector one and ending on the last sector number of the track.

- 00h Format sector as good
- 20h Unassign the alternate location for this sector
- 40h Assign this sector to an alternate location
- 80h Format sector as bad

6.7.6 Seek

The SEEK command causes the actuator to seek to the track to which the Cylinder and Drive/Head registers point. When the drive receives this command in its Command Block Registers, it performs the following functions:

1. Sets BSY
2. Initiates the seek operation
3. Resets BSY
4. Sets the Drive Seek Complete (DSC) bit in the Status Register

The drive does not wait for the seek to complete before it sends an interrupt. If the BSY bit is *not* set in the Status Register, the drive can accept and queue subsequent commands while performing the seek. If the Cylinder registers contain an illegal cylinder, the drive sets the ERR bit in the Status Register and the IDNF bit in the Error Register.

6.7.7 Execute Drive Diagnostic

The EXECUTE DRIVE DIAGNOSTIC command performs the internal diagnostic tests implemented on the drive. Drive 0 sets BSY within 400 ns of receiving of the command.

If Drive 1 is present:

- Both drives execute diagnostics.
- Drive 0 waits up to six seconds for drive 1 to assert PDIAG–.
- If drive 1 does not assert PDIAG– to indicate a failure, drive 0 appends 80h with its own diagnostic status.
- If the host detects a drive 1 diagnostic failure when reading drive 0 status, it sets the DRV bit, then reads the drive 1 status.

If Drive 1 is not present:

- Drive 0 reports only its own diagnostic results.
- Drive 0 clears BSY and generates an interrupt.

If drive 1 fails diagnostics, drive 0 appends 80h with its own diagnostic status and loads that code into the Error Register. If drive 1 passes its diagnostics or no drive 1 is present, drive 0 appends 00h with its own diagnostic status and loads that code into the Error Register.

The diagnostic code written to the Error Register is a unique 8-bit code. Table 6-15 lists the diagnostic codes.

Table 6-15 *Diagnostic Codes*

DIAGNOSTIC CODE	DESCRIPTION
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Drive 1 Failed

6.7.8 Initialize Drive Parameters

The INITIALIZE DRIVE PARAMETERS command enables the host to set the logical number of heads and the logical number of sectors per track. On receiving the command, the drive sets the BSY bit, saves the parameters, clears BSY, and generates an interrupt.

The only two register values used by this command are the Sector Count Register, which specifies the number of sectors; and the Drive/Head Register, which specifies the number of heads, minus 1. The DRV bit assigns these values to drive 0 or drive 1, as appropriate.

This command does not check the sector count and head values for validity. If these values are invalid, the drive will not report an error until another command causes an illegal access.

6.7.9 Read Multiple

The execution of the READ MULTIPLE command is identical to that of the Read Sectors command. However, the READ MULTIPLE command:

- Transfers blocks of data to the host without intervening interrupts
- Requires DRQ qualification of the transfer only at the start of the block—*not* at each sector
- Invalidates the Long bit

The SET MULTIPLE MODE command specifies the block count, or the number of sectors to be transferred as a block. This command executes prior to the READ MULTIPLE command. When the host issues a READ MULTIPLE command, the Sector Count Register contains the number of sectors requested—not the number of blocks or the block count.

If this sector count is not evenly divisible by the block count, the drive transfers as many full blocks as possible to the host, followed by a final partial-block transfer. The partial-block transfer is for *n* sectors, where:

n = (sector count) module (block count)

If the drive attempts execution of a READ MULTIPLE command before executing the SET MULTIPLE MODE command or if READ MULTIPLE commands are disabled, an abort command error occurs.

The drive reports disk errors encountered during READ MULTIPLE commands at the beginning of a block or partial-block transfer. However, the drive still sets DRQ and transfers the data—including any corrupted data.

6.7.10 Write Multiple

The execution of the WRITE MULTIPLE command is identical to that of the Write Sectors command. However, the WRITE MULTIPLE command:

- Causes the controller to set BSY within 400 ns of accepting the command
- Causes the drive to transfer multiple-sector blocks of data to the drive without intervening interrupts
- Requires DRQ qualification of the transfer only at the start of the block, not at each sector
- Invalidates the Long bit

The SET MULTIPLE MODE command specifies the block count, or the number of sectors to be transferred as a block. This command executes prior to the WRITE MULTIPLE command. When the host issues a WRITE MULTIPLE command, the Sector Count Register contains the number of sectors requested—not the number of blocks or the block count.

If this sector count is not evenly divisible by the block count, the drive transfers as many full blocks as possible, followed by a final partial-block transfer. The partial-block transfer is for *n* sectors, where:

$$n = \text{(sector count) module (block count)}$$

If the drive attempts to execute a WRITE MULTIPLE command before executing the SET MULTIPLE MODE command or while WRITE MULTIPLE commands are disabled, an Abort Command error occurs.

During the execution of a WRITE MULTIPLE command, the drive reports all disk errors encountered, following an attempted disk write of the block or partial block. When an error occurs, the WRITE MULTIPLE command ends at the sector that contains the error—even if it is in the middle of a block—and does not transfer subsequent blocks. The drive generates interrupts by setting DRQ at the beginning of each block or partial block.

6.7.11 Set Multiple Mode

The SET MULTIPLE MODE command enables the controller to perform READ MULTIPLE and WRITE MULTIPLE operations, and establishes the block count for these commands.

Prior to issuing a command, the host should load the Sector Count Register with the number of sectors per block. On receiving this command, the drive sets BSY and checks the contents of the Sector Count Register.

If the Sector Count Register contains a valid value and the controller supports block count, the controller loads the values for all subsequent READ MULTIPLE and WRITE MULTIPLE commands and enables execution of these commands. Any unsupported block count in the register causes an Aborted Command error, and disables execution of READ MULTIPLE and WRITE MULTIPLE commands.

If the Sector Count Register contains a zero value when the host issues the command, READ MULTIPLE and WRITE MULTIPLE commands are disabled. Any unsupported block count in the register causes an aborted command error, and disables READ MULTIPLE and WRITE MULTIPLE commands. After the command is executed, the controller clears BSY. At power on, or after a software or hardware reset, the default mode for the READ MULTIPLE and WRITE MULTIPLE commands is disabled.

6.7.12 Read Buffer

The READ BUFFER command enables the host to read the current contents of the drive's sector buffer. When the host issues this command, the drive sets BSY, sets up the sector buffer for a read operation, sets DRQ, class BSY, and generates an interrupt. The host then reads up to 512 bytes of data from the buffer.

The drive can synchronize READ BUFFER and WRITE BUFFER commands from the host; that is, sequential READ BUFFER and WRITE BUFFER commands can access the same 512 bytes within the buffer.

6.7.13 Write Buffer

The WRITE BUFFER command allows the host to write the first 512 bytes of the drive's buffer. On receiving this command in its Command Block Register, the drive sets BSY and prepares for a write operation. When ready, the drive sets DRQ, resets BSY, and generates INTRQ, allowing the host to the buffer.

6.7.14 Power Management Commands

The Quantum Vortex 1275/2550AT hard disk drive provides numerous management options. Two important options center around a count down counter known as the automatic power down counter or APD. This counter can trigger one of two power saving events depending on which of the two commands was most to write to the buffer.

- Standby: Once a standby command is issued, the drive enters the standby mode. Further, each time the APD counter reaches zero in the future, the drive enters the standby mode, the spindle and actuator motors are off and the heads are parked in the landing zone. Receipt of any command that requires media access causes the drive to exit the standby command and service the host request. Each time the drive executes the standby command, the drive will reenter the standby mode when the APD counter reaches zero.
- Idle: Once an idle command is issued, each time the APD counter reaches zero, the drive enters the standby mode. In the standby mode, the actuator and spindle motors are off with the heads locked in the landing area. This is the default setting.
- Automatic Power Down (APD) Mode: When in APD mode, the drive transitions to standby mode when the APD time elapses. Receipt of any command that requires media access causes the drive to exit standby mode. Upon receiving a command, the drive resets the APD counter to zero and starts it again (with the exception of the Check Power Mode Command, which does not reset the APD counter).

Three commands are available which are not dependent upon the APD counter reaching zero:

- Sleep: When a sleep command is received, the drive enters the sleep mode. In the sleep mode, the spindle and actuator motors are off and the heads are latched in the landing zone. Receipt of a reset causes the drive to transition from the sleep to the standby mode.
- Standby Immediate: When a standby immediate command is received, the drive immediately enters the standby mode.
- Idle Immediate: When an idle immediate command is received, after the first decrement of the APD counter, the drive enters the idle mode.

The sleep, standby immediate, and idle immediate commands differ in a significant way from the standby and idle commands. Specifically, sleep, standby immediate, and idle immediate have a one-time effect and must be reissued each time their effect is desired. In contrast, standby and idle operate in conjunction with the APD counter and stay in effect continually, becoming non-effectual only upon issuance of the other of these two commands. Thus, for example, once the standby command is issued just one time, each time the APD counter reaches zero the drive will enter the standby mode.

Note: The user has the ability to determine the value to which the APD counter is set upon completion of any command. This value is set by writing to the Sector Count Register a number between 12 and 255 just prior to issuance of a standby or idle command. Each increment represents a five-second time interval.

6.7.14.1 Standby Immediate Mode – E0h

The Standby Immediate Mode power command immediately puts the drive in the Standby Mode. Power is removed from the spindle motor (the drive's PCB power remains) and the heads are parked.

6.7.14.2 Idle Immediate Mode – E1h

The Idle Immediate Mode power command immediately puts the drive in the Idle Mode.

6.7.14.3 Standby Mode, Automatic Power-Down – E2h

The Standby Mode, Automatic Power-Down (APD) command immediately puts the drive in the Standby Mode. The Sector Count Register is then examined. If the value in this register is not zero, the Auto Power-Down feature is enabled and will take effect once the countdown timer reaches zero. The valid count range is Table 6-16. Each time the drive is accessed, the countdown timer is reset to the value originally set in the Sector Count Register at the time the Standby Mode-Auto Power Down command was issued.

Note: If the value in the Sector Count Register is zero, the Auto Power-Down feature is disabled.

Table 6-16 *Valid Count Range*

SECTOR COUNT	TIME
1 to 12	1 minute
13 to 240	(Value * 5) seconds
241 to 251	(Value – 240) * 30 seconds
252 to 255	((Value * 5) seconds

6.7.14.4 Idle Mode, Automatic Power-Down – E3h

The Idle Mode, Automatic Power-Down command immediately puts the drive into the Idle Mode. The Sector Count Register is then examined. If the value in this register is not zero, the Auto Power-Down feature is enabled and takes effect once the countdown timer reaches zero. The valid count range is listed in Table 6-16. Each time the drive is accessed, the countdown timer is reset to the value originally set in the Sector Count Register at the time the Idle Mode-Auto Power Down command was issued.

Note: If the value in the Sector Count Register is zero, the Auto Power-Down feature is disabled.

6.7.14.5 Check Power Mode – E5h

The CHECK POWER MODE command writes FFh into the Sector Count Register provided that the drive is in the Idle Mode, even if it is in Automatic Power-Down mode. However, if it is in Standby mode, the drive returns a value of 00h in the Sector Count Register.

6.7.14.6 Sleep Mode – E6h

The Quantum Vortex drive considers the Sleep Mode to be the equivalent to the Standby Mode, except that a reset is required before issuing a command requiring media access.

6.7.15 Identify Drive

The IDENTIFY DRIVE command enables the host to receive parameter information from the drive. When the host issues this command, the drive sets BSY, stores the required parameter information in the sector buffer, sets DRQ, and generates an interrupt. The host then reads the information from the sector buffer. The Identify Drive Parameters Table, shown in Table 6-17, defines the parameter words stored in the buffer. All reserved bits should be zeros. A full explanation of the parameter words is listed below:

Default Logical Cylinders: The number of translated cylinders in the default translation mode.

Number of Logical Heads: The number of translated heads in the default translation mode.

Number of Unformatted Bytes Per Track: The number of unformatted bytes per translated track in the default translation mode.

Number of Unformatted Bytes Per Sector: The number of unformatted bytes per sector in the default translation mode.

Number of Logical Sectors Per Track: The number of sectors per track in the default translation mode.

Serial Number: The contents of this field are left aligned and padded with spaces (20h).

Buffer Type: The contents of this field are as follows:

- 0000h = Not specified
- 0001h = A single-ported, single-sector buffer capable of data transfers either to or from the host or to or from the disk
- 0002h = A dual-ported, multiple-sector buffer capable of simultaneous data transfers either to and from the host, or from the host and the disk
- 0003h = A dual-ported, multiple-sector buffer capable of simultaneous data transfers with read caching
- 0004 – FFFFh = Reserved

Firmware Revision: The contents of this field are left-aligned and padded with spaces (20h).

Model Number: The contents of this field are left-aligned and padded with spaces (20h). The low-order byte appears first in a word.

Table 6-17 *Identify Drive Parameters*

WORDS[1]			PARAMETER DESCRIPTION (Statements below are true if the bit is set to 1)
WORD	BIT	BIT VALUE	
0	15	0	Reserved for nonmagnetic drives
	14	0	Format speed tolerance gap required
	13	0	Track offset option available
	12	0	Data strobe offset option available
	11	0	Rotational speed tolerance is > 0.5%
	10	1	Disk transfer rate > 10 Mbit/s
	9	0	Disk transfer rate > 5 Mbit/s, but < 10 Mbit/s
	8	0	Disk transfer rate <= 5 Mbit/s
	7	0	Reserved for removable-cartridge drive
	6	1	Hard disk drive
	5	0	Spindle motor control option implemented
	4	1	Head-switch time > 15 µs
	3	1	Not MFM-encoded
	2	0	Soft-sectored
	1	1	Hard-sectored
	0	0	Reserved
1		1275AT = 2,492 2550AT = 4,994	Default logical cylinders
2		0	Reserved

WORDS[1]			PARAMETER DESCRIPTION (Statements below are true if the bit is set to 1)
WORD	BIT	BIT VALUE	
3		1275AT = 16 2550 AT = 16	Default number of logical heads
4			Number of unformatted bytes per track
5		512	Number of unformatted bytes per sector
6		1275AT = 63 2550 AT = 63	Default number of logical sectors per track
7–9		5154h	Vendor-unique
10–19			Serial number (20 ASCII characters)[2]
20		3	Buffer type
21		A7h	Buffer size in 512-byte increments
22		4	Number of ECC bytes passed on READ/WRITE LONG commands
23–26			Firmware revision (8 ASCII characters)
27–46			Model number (40 ASCII characters)
47	15–8 7–0	80h 08h	Vendor Unique Maximum number of sectors that can be transferred per interrupt is set to 8 for READ MULTIPLE and WRITE MULTIPLE commands.
48		0	Cannot perform double word I/O
49	15–12 11 10 9 8 7–0	0 1 1 1 1 0	Reserved 1 = I/O Ready is supported 1 = I/O Ready can be disabled 1 = LBA supported 1 = DMA supported Vendor Unique
50		0	Reserved
51	15–8 7–0	2 0	PIO data-transfer cycle timing mode Vendor Unique
52	15–8 7–0	2 0	DMA data-transfer cycle timing mode Vendor Unique
53	15–2 1 0	0 1 1	Reserved 1 = The fields in words 64–70 are valid 1 = The fields in words 54–58 are valid
54			Number of current cylinders
55			Number of current heads
56			Number of current sectors per track
57–58			Current capacity in sectors (CHS mode only)

WORDS[1]			PARAMETER DESCRIPTION (Statements below are true if the bit is set to 1)
WORD	BIT	BIT VALUE	
59	15–9 8 7–0	0 1 n[3]	Reserved Multiple sector setting is valid Current setting for number of sectors that can be transferred per interrupt on R/W Multiple commands
60–61		1275AT = 2,511,936 2550 AT = 5,033,952	Total number of User Addressable Sectors (LBA Mode only)
62	15–8 7–0	4 7	Single-word DMA transfer mode active (Mode 2) Single-word DMA transfer modes supported (Mode 2)
63	15–8 7–0	4 7	Multiword DMA transfer mode active (Mode 1) Multiword DMA transfer modes supported (Mode 1)
64		3	Advanced PIO Mode is supported
65		120	Minimum multiword DMA transfer cycle time (ns) per word
66		333	Manufacturer's recommended multiword DMA cycle time (ns)
67		333	Manufacturer's PIO cycle time (ns) without flow control
68		120	Manufacturer's PIO cycle time (ns) with flow control

1. The format of an ASCII field specifies that, within a word boundary, the low-order byte appears first.
2. The serial number has the following format: 00QTMTCYJJJLSSSSBBB

   where: 00 = Placeholders
   QT = Quantum
   M = Place of manufacture
   T = Drive type family (fixed at 4)
   C = Drive capacity (5 = 1275 MB, 1 = 2550 MB)
   Y = Last digit of year drive built
   JJJ = Julian date
   L = Manufacturing production line
   SSSS = Sequence of manufacture
   BBB = Blanks (placeholders)

3. n is a variable from zero to 8.

6.7.16 Set Features

The SET FEATURES command is used by the host to establish certain parameters which control execution of the following drive features:

- 02h – Enable write cache feature
- 03h – Set transfer mode based on value in Sector Count Register
- 55h – Disable read look-ahead feature
- 82h – Disable write cache feature
- AAh – Enable read look-ahead feature

At power-on, or after a reset accomplished by either the hardware or software, the default mode is 4 bytes of ECC, read look-ahead, and write cache enabled.

A host can choose the transfer mechanism by Set Transfer Mode and specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

PIO Default Transfer Mode, Disable IORDY	00000 001
Single Word DMA Mode x	00010 nnn
Multiword DMA Mode x	00100 nnn

Where "nnn" is a valid mode number for the associated transfer type.

6.7.17 Read Defect List

The READ DEFECT LIST command enables the host to retrieve the drive's defect list. When the host writes the bytes at addresses 1F2H–1F6H, followed by F0h at address 1F7h, the drive sets BSY, retrieves the defect list, sets DRQ, and resets BSY. The first byte, 07h, is a subcode to the extended command code F0h. The host can now read seven sectors (3584 bytes) of data. An INTRQ precedes each sector. Table 6-18 lists the bytes for this command.

Table 6-18 *READ DEFECT LIST Command Bytes*

ADDRESS	VALUE	DEFINITION
1F2	07h	Defect List Subcode
1F3	FFh	Password
1F4	FFh	Password
1F5	3Fh	Password
1F6	AXh (Drive 0)	Drive Select
	BXh (Drive 1)	—
1F7	F0h	Extended Command Code

In Table 6-18:

- Registers 1F2h through 1F5h must contain the exact values shown. These values function as a key. The drive issues the abort error message if the bytes are not entered correctly.

- To select the proper drive, set register 1F6h. For execution of the command to begin, load register 1F7h with F0h.

The seven bytes listed in Figure 6-4 describe each defect or replacement in a physical cylinder, head, and sector.

6.7.18 Defect List Data Structure

The defect lists maintained and accessed by the defect management system consist of 7 byte defect entries. The P list contains only defect entries while the W list contains both defect and replacement cylinder information. The defect list structure is illustrated in Figure 6-4.

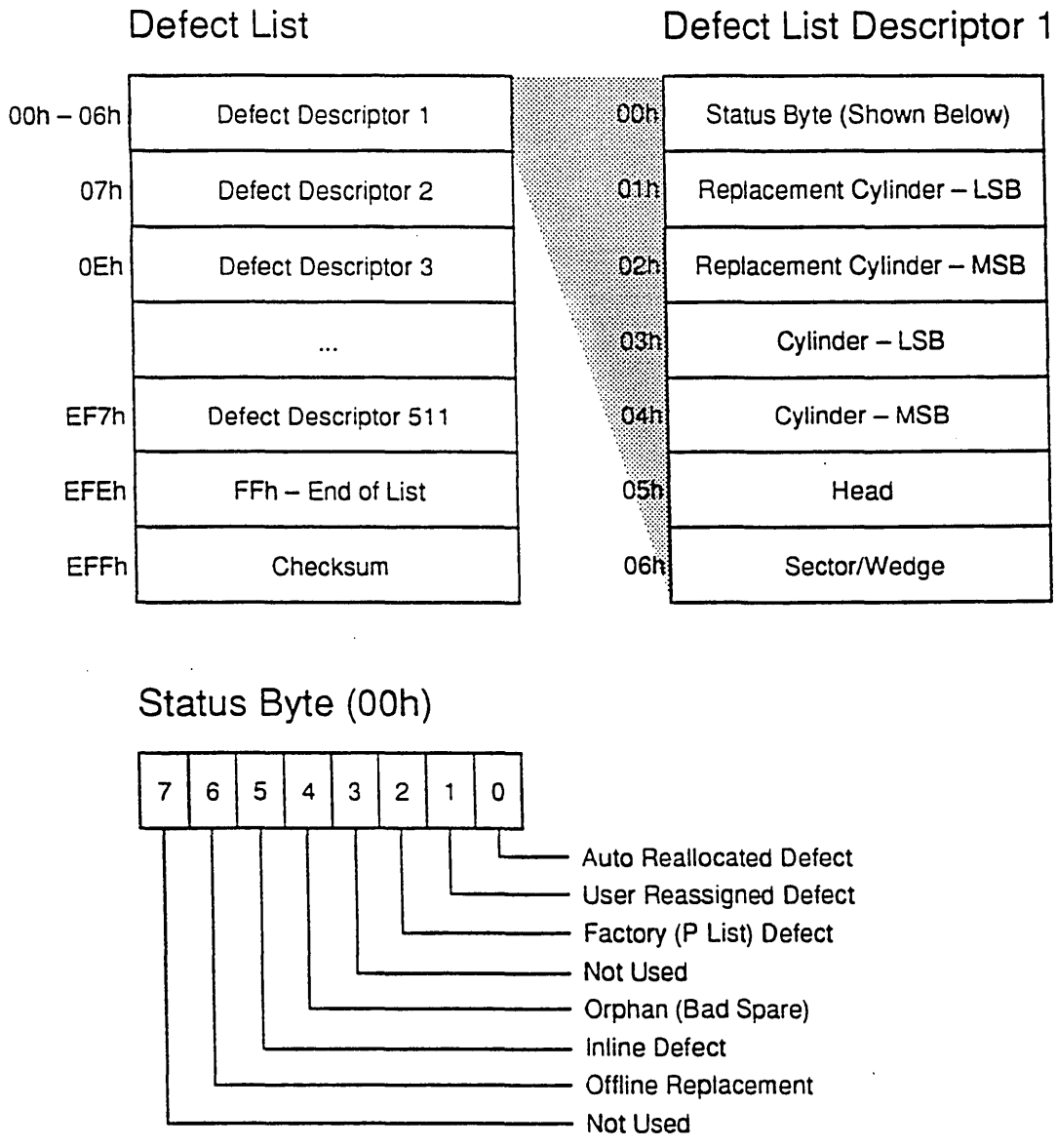


Figure 6-4 *Defect List Data Structure*

The end of list marker is placed after the last entry in the list (i.e., if there is only one defect, the end of list marker would be located at byte 07h).

The checksum is placed at the end of the list, and the empty area in the list is filled with zeros.

Table 6-19 shows a sample defect list.

Table 6-19 *Sample Defect List*

ENTRY	VALUE	DESCRIPTION
Defect Descriptor 1	24h	Factory-found defect—spared inline transparently
	07h	Replacement Cylinder = 07 (LSB)
	00h	Replacement Cylinder = 00 (MSB)
	07h	Defective Cylinder = 07 (LSB)
	00h	Defective Cylinder = 00 (MSB)
	00h	Defective Head = 00
	02h	Defective Sector = 02
Defect Descriptor n	41h	Field-found defect—automatically reallocated offline
	08h	Replacement Cylinder = 08 (LSB)
	00h	Replacement Cylinder = 00 (MSB)
	07h	Defective Cylinder = 07 (LSB)
	00h	Defective Cylinder = 00 (MSB)
	01h	Defective head = 01
	04h	Defective sector = 04
	FFh	End of list marker

6.7.19 Configuration

In addition to the SET FEATURES command, the Quantum Vortex 1275/2550AT hard disk drive provides two configuration commands:

- The SET CONFIGURATION command, which enables the host to change DisCache and Error Recovery parameters
- The READ CONFIGURATION command, which enables the host to read the current configuration status of the drive

See Chapter 5 for more details about DisCache and setting cache parameters. See Chapter 5 also for more information about error detection and defect management.

6.7.19.1 Read Configuration

The READ CONFIGURATION command displays the configuration of the drive. Like the SET CONFIGURATION command, this command is secured to prevent accidentally accessing it. To access the READ CONFIGURATION command, you must write the pattern shown inTable 6-20 to the Command Block Registers. The first byte, 01h, is a subcode to the extended command code, F0h.

Table 6-20 *Accessing the READ CONFIGURATION Command*

ADDRESS	VALUE	DEFINITION
1F2h	01h	Read Configuration Subcode
1F3h	FFh	Password
1F4h	FFh	Password
1F5h	3Fh	Password
1F6h	AXh (Drive 0)	Drive Select
	BXh (Drive 1)	Drive Select
1F7h	F0h	Extended Command Code

Note: In Table 6-20:

Only the value in address 1F2h of the Command Block Registers is different from the SET CONFIGURATION command.

Registers 1F2h through 1F5h must contain the exact values shown in Table 6-20. These values function as a key. The drive issues the message ILLEGAL COMMAND if the key is not entered correctly.

To select the drive for which the configuration is to be read, set register 1F6h. For execution of the command to begin, load register 1F7h with F0h.

A 512-byte data field is associated with the READ CONFIGURATION command. A 512-byte read sequence sends this data from the drive to the host. The information in this data field represents the current settings of the configuration parameters. The format of the READ CONFIGURATION command data field is similar to that for the data field of the SET CONFIGURATION command, shown in Table 6-21. However, in the READ CONFIGURATION command, bytes 0 through 31 of the data field are *not* KEY information, as they are in the SET CONFIGURATION command. The drive reads these bytes as *QUANTUM CONFIGURATION*, followed by eleven spaces. Users can read the configuration into a buffer, then alter the configuration parameter settings.

6.7.19.2 Set Configuration

The SET CONFIGURATION command is secured to prevent accessing it accidentally. To access the SET CONFIGURATION command, you must write the pattern shown in Table 6-21 to the Command Block Registers. The first byte, FFh, is a subcode to the extended command code F0h.

Table 6-21 *Accessing the SET CONFIGURATION Command*

ADDRESS	VALUE	DEFINITION
1F2h	FFh	Set Configuration Subcode
1F3h	FFh	Password
1F4h	FFh	Password
1F5h	3Fh	Password
1F6h	AXh (Drive 0)	Drive Select
	BXh (Drive 1)	Drive Select
1F7h	F0h	Extended Command Code

Note: In Table 6-21:
Registers 1F2h through 1F5h must contain the exact values shown above. These values function as a key. The drive issues the message ILLEGAL COMMAND if the key is not entered correctly.
To select the drive being reconfigured, register 1F6h should be set. For execution of the command to begin, load register 1F7h with F0h.

6.7.19.3 Set Configuration Without Saving to Disk

The SET CONFIGURATION WITHOUT SAVING TO DISK command is secured to prevent accidentally accessing it. To access this command, you must write the pattern shown in Table 6-22 to the Command Block Registers. The first byte, FFh, is a subcode to the extended command code F0h.

Table 6-22 *Accessing the SET CONFIGURATION WITHOUT SAVING TO DISK Command*

ADDRESS	VALUE	DEFINITION
1F2h	FEh	Set Configuration Subcode
1F3h	FEh	Password
1F4h	FEh	Password
1F5h	3Fh	Password
1F6h	AXh (Drive 0)	Drive Select
	BXh Drive 1)	Drive Select
1F7h	F0h	Extended Command Code

Note: In Table 6-22:
Registers 1F2h through 1F5h must contain the exact values shown above. These values function as a key. The drive issues the message ILLEGAL COMMAND if the key is not entered correctly.
To select the drive being reconfigured, set register 1F6h. For execution of the command to begin, load register 1F7h with F0h.

6.7.19.4 Configuration Command Data Field

A 512-byte data field is associated with this command. This data field is sent to the drive through a normal 512-byte write handshake. Table 6-23 shows the format of the data field. Bytes 0 through 31 of the data field contain additional KEY information. The drive issues the message ILLEGAL COMMAND if this information is not entered correctly. Bytes 32 through 35 control the operation of DisCache. Bytes 36 through 38 control operation of the error recovery procedure. The drive does not use bytes 40 through 511, which should be set to 0.

Table 6-23 *Configuration Command Format*

BYTE	BIT							
	7	6	5	4	3	2	1	0
0–31	QUANTUM CONFIGURATION KEY							
32	RESERVED = 0						PE	CE
33	RESERVED							
34	RESERVED = 0							
35	RESERVED = 0							
36	AWRE	ARR	N/A	RC	EEC	N/A	N/A	DCR
37	NUMBER OF RETRIES							
38	ECC CORRECTION SPAN							
39	RESERVED = 0					WCE	RUEE	0
40–511	RESERVED = 0							

Note: All fields marked RESERVED or N/A should be set to zero.

6.7.19.5 Quantum Configuration Key (Bytes 0-31)

Bytes 0–6 must contain the ASCII characters *Q, U, A, N, T, U,* and *M*; byte 7, the ASCII character *space*; and bytes 8–20 must contain the ASCII characters *C, O, N, F, I, G, U, R, A, T, I, O,* and *N*. Bytes 21–31 must contain an ASCII *space*. If this information is not entered correctly, the drive aborts the COMMAND.

6.7.19.6 DisCache Parameters

PE – Prefetch Enable (Byte 32, Bit 1): When set to 1, this bit indicates that the drive will perform prefetching. A PE bit set to 0 indicates that no prefetching will occur. The CE bit (bit 0) must be set to 1 to enable use of the PE bit. The default value is 1.

CE – Cache Enable (Byte 32, Bit 0): When set to 1, this bit indicates that the drive will activate caching on all READ commands. With the CE bit set to 0, the drive will disable caching and use the RAM only as a transfer buffer. The default setting is 1.

6.7.19.7 Error Recovery Parameters

AWRE – Automatic Write Reallocation Enabled (Byte 36, Bit 7): When set to 1, indicates that the drive will enable automatic reallocation of bad blocks. Automatic Write Reallocation is similar to the function of Automatic Read Reallocation, but is initiated by the drive when a defective block has become inaccessible for writing. An AWRE bit set to 0 indicates that the Quantum Vortex 1275/2550AT drive will not automatically reallocate bad blocks. The default setting is 1.

ARR – Automatic Read Reallocation (Byte 36, Bit 6): When set to 1, this bit indicates that the drive will enable automatic reallocation of bad sectors. The drive initiates reallocation when the ARR bit is set to 1 and the drive encounters a hard error—that is, if the triple-burst ECC algorithm is invoked. The default setting is 1. When the ARR bit is set to 0, the drive will not perform automatic reallocation of bad sectors. If RC (byte 36, bit 4) is 1, the drive ignores this bit. The default value is 1.

RC – Read Continuous (Byte 36, Bit 4): When set to 1, this bit instructs the drive to transfer data of the requested length without adding delays to increase data integrity—that is, delays caused by the drive's error-recovery procedures. With RC set to 1 to maintain a continuous flow of data and avoid delays, the drive may send data that is erroneous. When the drive ignores an error, it does *not* post the error. The RC bit set to 0 indicates that potentially time-consuming operations for error recovery are acceptable during data transfer. The default setting is 0.

EEC – Enable Early Correction (Byte 36, Bit 3): When set to 1, this bit indicates that the drive will use its ECC algorithm if it detects two consecutive equal, nonzero error syndromes. The drive will not perform rereads before applying correction, unless it determines that the error is uncorrectable. An EEC bit set to 0 indicates that the drive will use its normal recovery procedure when an error occurs: rereads, followed by error correction. If the RC bit (byte 36, bit 4) is set to 1, the drive ignores the EEC bit. The default setting is 0.

DCR – Disable Correction (Byte 36, Bit 0): When set to 1, this bit indicates that all data will be transferred without correction, even if it would be possible to correct the data. A DCR bit set to 0 indicates that the data will be corrected if possible. If the data is uncorrectable, it will be transferred without correction, though the drive will attempt rereads. If RC (byte 36, bit 4) is set to 1, the drive ignores this bit. The default setting is 0. The drive will post all errors, whether DCR is set to 0 or 1.

NUMBER OF RETRIES (Byte 37): This byte specifies the number of times that the drive will attempt to recover from data errors by rereading the data, before it will apply correction. The drive performs rereads before ECC correction—unless EEC (byte 36, bit 3) is set to 1, enabling early correction. The default is eight.

ECC CORRECTION SPAN (Byte 38): This byte specifies the maximum number of bits per interleave that can be corrected using triple-burst ECC. The value for this byte is fixed at 24.

6.7.19.8 Drive Parameters

FIX SPACING

WCE – Write Cache Enable (Byte 39, Bit 2) : When this bit is set to 1, the Quantum Vortex 1275/2550AT hard disk enables the Write Cache. This indicates that the drive returns GOOD status for a write command after successfully receiving the data, but before writing it to the disk. A value of zero indicates that the drive returns GOOD status for a write command after successfully receiving the data and writing it to the disk.

If the next command is another WRITE command, cached data continues to be written to the disk while new data is added to the buffer. The default setting is 1.

RUEE – Reallocate Uncorrectable Error Enables (Byte 39, Bit 1): When set to 1, this bit indicates that the Quantum Vortex 1275/2550AT hard disk drive will automatically reallocate uncorrectable hard errors, if the ARR bit (byte 36, bit 6) is set to 1. The default setting is 1.

6.8 ERROR REPORTING

At the start of a command's execution, the Quantum Vortex 1275/2550AT hard disk drive checks the Command Register for any conditions that would lead to an abort command error. The drive then attempts execution of the command. Any new error causes execution of the command to terminate at the point at which it occurred. Table 6-24 lists the valid errors for each command.

Table 6-24 *Command Errors*

COMMAND	ERROR REGISTER						STATUS REGISTER				
	BBK	UNC	IDNF	ABRT	TKO	AMNF	DRDY	DWF	DSC	CORR	ERR
Check Power Mode				V			V	V	V		V
Read Defect List	V	V	V	V		V	V	V	V	V	V
Execute Drive Diag.											V
Format Track			V	V			V	V	V		V
Identify Drive				V			V	V	V		V
Initialize Parameters							V	V	V		
Invalid Cmnd. Codes				V			V	V	V		V
Read Buffer				V			V	V	V		V
Read DMA	V	V	V	V		V	V	V	V	V	V
Read Configuration	V	V	V	V		V	V	V	V	V	V
Read Multiple	V	V	V	V		V	V	V	V	V	V
Read Sectors	V	V	V	V		V	V	V	V	V	V
Read Sectors Long	V		V	V		V	V	V	V		V
Read Verify Sectors	V	V	V	V		V	V	V	V	V	V
Recalibrate				V	V		V	V	V		V
Seek			V	V			V	V	V		V
Set Configuration	V		V	V			V	V	V		V
Set Features				V			V	V	V		V
Set Multiple Mode				V			V	V	V		V
Write Buffer				V			V	V	V		V
Write DMA	V		V	V			V	V	V		V
Write Multiple	V		V	V			V	V	V		V
Write Sectors	V		V	V			V	V	V		V
Write Sectors Long	V		V	V			V	V	V		V

Note:
V = Valid errors for each command
ABRT = Abort command error
AMNF= Data address mark not found error
BBK = Bad block detected
CORR= Corrected data error
DRDY= Drive ready
DSC = Disk seek complete not detected
DWF = Drive write fault detected
ERR = Error bit in the Status Register
IDNF = Requested ID not found
TK0 = Track zero not found error
UNC = Uncorrectable data error

Glossary

A

ACCESS – (v) Read, write, or update information stored on a disk or other medium. (n) The operation of reading, writing, or updating stored information.

ACCESS TIME – The interval between the time a request is made by the system and the time the data is available from the drive. Includes the seek time, rotational latency, and command processing overhead time. (See also *seek*, *rotational latency*, and *overhead*.)

ACTUATOR – Also known as the *positioner*. The internal mechanism that moves the read/write head to the proper track. The Quantum actuator consists of a rotor connected to head mounting arms that position the heads over the desired cylinder. Also known as rotary actuator.

AIRLOCK – A patented Quantum feature that ensures durable and reliable data storage. Upon removal of power from the drive for any reason, the read/write heads automatically park and lock in a non data area called the landing zone. AIRLOCK allows the drive to withstand high levels of non-operating shock. When power is applied to the drive, airflow created from the spinning disks causes the AIRLOCK arm to swing back and unlock the actuator, allowing the heads to move from the landing zone. Upon power down, the AIRLOCK swings back to the locked position, locking the heads in the landing zone. A park utility is not required to park the heads on drives equipped with AIRLOCK (all Quantum drives).

ALLOCATION – The process of assigning particular areas of the disk to specific data or instructions. An allocation unit is a group of sectors on the disk reserved for specified information. On hard disks for small computer systems, the allocation unit is usually in the form of a sector, block, or cluster. (See also *allocation unit*.)

ALLOCATION UNIT – An allocation unit, also known as a *cluster*, is a group of sectors on the disk that can be reserved for the use of a particular file.

ASIC – Acronym for *Application Specific Integrated Circuit*.

AT – An interface designed for IBM PCs and compatible systems. Also known as IDE. (See also *interface*.)

AVERAGE SEEK TIME – The average time it takes for the read/write head to move to a specific location. Calculated by dividing the time it takes to complete a large number of random seeks by the number of seeks performed.

B

BACKUP – A copy of a file, directory, or volume on a separate storage device from the original, for the purpose of retrieval in case the original is accidentally erased, damaged, or destroyed.

BAD BLOCK – A block (usually the size of a sector) that cannot reliably hold data due to a physical flaw or damaged format markings.

BAD TRACK TABLE – A label affixed to the casing of a hard disk drive stating which tracks are flawed and cannot hold data. This list is typed into the low-level formatting program when the drive is installed. Quantum users can ignore bad track tables since Quantum's built-in defect-management protections compensate for these flaws automatically.

BEZEL – A plastic panel that extends the face of a drive so that it covers a computer's drive bay opening. The bezel usually contains a drive-activity LED. Also known as the *faceplate*.

BIOS – Acronym for Basic Input / Output System. The firmware portion of a computer that manages the flow of signals through the system bus and to the attached cards and peripheral devices.

BIT – Abbreviation for binary digit. A binary digit may have one of two values—1 or 0. This contrasts with a decimal digit, which may have a value from 0 to 9. A bit is one of the logic 1 or logic 0 binary settings that make up a byte of data. (See also *byte*.)

BLOCK – In UNIX workstation environments, the smallest contiguous area that can be allocated for the storage of data. UNIX blocks are generally 8 Kbytes (16 sectors) in size. In DOS environments, the block is referred to as a cluster. (Note: This usage of the term block at the operating system level is different from its meaning in relation to the physical configuration of the hard drive. See *sector* for comparison.) While an operating system may have its

block size set at 8K, the drive usually assigns its "logical block" size to 1 sector (1 OS block = 16 drive locical blocks).

BPI – Bits Per Inch. A measure of how densely information is packed on a storage medium. (See also *FCI.*)

BUFFER – An area of RAM reserved for temporary storage of data that is waiting to be sent to a device that is not yet ready to receive it. The data is usually on its way to or from the hard disk drive or some other peripheral device.

BUS – The part of a chip, circuit board, or interface designed to send and receive data.

BYTE – The basic unit of computer memory, large enough to hold one character of alphanumeric data. Comprised of eight bits. (See also *bit.*)

C

CACHE – High-speed RAM used as a buffer between the CPU and the hard disk. Since the CPU can get information more quickly from the cache than from main memory, the cache usually contains information that is used frequently by the system.

CAPACITY – The amount of information that can be stored on a hard drive. Also known as storage capacity. (See also *formatted capacity.*)

CLEAN ROOM – An environmentally controlled dust-free assembly or repair facility in which hard disk drives are assembled or can be opened for internal servicing.

CLUSTER – In DOS environments, the smallest contiguous area that can be allocated for the storage of data. DOS clusters are usually 2 Kbytes (4 sectors) in size.

CONTROLLER – The chip or circuit that translates computer data and commands into a form suitable for use by the hard drive. Also known as disk controller.

CONTROLLER CARD – An adapter containing the control electronics for one or more hard disks. Usually installed in a slot in the computer.

CPU – Central Processing Unit. The microprocessor chip that performs the bulk of data processing in a computer.

CRC – Cyclic Redundancy Check. An error detection procedure that identifies incomplete or faulty data in each sector.

CYLINDER – When disks are placed directly above one another along the shaft, the circular, vertical "slice" consisting of all the tracks located in a particular position.

D

DATA SEPARATOR – The circuit that extracts data from timing information on drives that store a combined data and clock signal.

DEDICATED SERVO – A positioning mechanism using a dedicated surface of the disk that contains timing and positioning information only, as compared to surfaces that are also used for data. (See also *embedded servo.*)

DEFECT MANAGEMENT – A technique ensuring long-term data integrity. Consists of scanning disk drives both at the factory and during regular use, de-allocating defective sectors before purchase and compensating for new defective sectors afterward.

DISK – In general, any circular-shaped data-storage medium that stores data on the flat surface of the platter. The most common type of disk is the magnetic disk, which stores data as magnetic patterns in a metal or metal-oxide coating. Magnetic disks come in two forms: floppy and hard. Optical recording is a newer disk technology that gives higher capacity storage but at slower access times.

DISK CONTROLLER – A plug-in board, or embedded circuitry on the drive, that passes information to and from the disk. The Quantum hard disk drives all have controllers embedded on the drive printed-circuit board. (See also *controller.*)

DMA – Direct Memory Access. A process for transferring data directly to and from main memory, without passing through the CPU. DMA improves the speed and efficiency by allowing the system to continue processing even while new data is being retrieved.

DOS – Disk Operating System. The most common operating system used in IBM PCs. Manages all access to data on the disk.

DRIVE – Short form of *disk drive.*

DRIVE GEOMETRY – The functional dimensions of a drive, including the number of heads, cylinders, and sectors per track. (See also *logical format.*)

E

ECC – Error Correction Code. The incorporation of extra parity bits in transmitted data in order to detect errors that can be corrected by the controller.

EISA – Extended Industry Standard Architecture. An enhanced AT bus architecture designed by nine manufacturers of PC compatibles and announced in September 1988. EISA promises the advantages of IBM Micro Channel Architecture with the advantage of downward compatibility to the current standard AT bus. (See also *ISA.*)

EMBEDDED SERVO – A timing or location signal placed on tracks that store data. These signals allow the actuator to fine-tune the position of the read/write heads.

ENCODING – The conversion of data into a pattern of On/Off or 1/0 signals prior to being written on the disk surface. (See also *RLL* and *MFM.*)

EPROM – Erasable Programmable Read-Only Memory. An integrated circuit memory chip that can store programs and data in a non-volatile state. These devices can be erased by ultraviolet light and reprogrammed with new data.

EXTERNAL DRIVE – A drive mounted in an enclosure separate from the computer system enclosure, with its own power supply and fan, and connected to the system by a cable.

F

FAT – File Allocation Table. A data table stored on the outer edge of a disk, telling the operating system which sectors are allocated to each file and in what order.

FCI – Flux Changes per Inch. The number of magnetic field patterns that can be stored on a given area of disk surface, used as a measure of data density. (See also *BPI.*)

FILE SERVER – A computer that provides network stations with controlled access to shareable resources. The network operating system is loaded on the file server, and most shareable devices (disk subsystems, printers) are attached to it. The file server controls system security and monitors station-to-station communications. A dedicated file server can be used only as a file server while it is on the network. A non dedicated file server can be used simultaneously as a file server and a workstation.

FIRMWARE – Permanent instructions and data programmed directly into the circuitry of read-only memory for controlling the operation of the computer. Distinct from software, which can be altered by programmers.

FLUX DENSITY – The number of magnetic field patterns that can be stored in a given length of disk surface. The number is usually stated as flux changes per inch (FCI), with typical values in the thousands. (See also *FCI.*)

FLYING HEIGHT – The distance between the read/write head and the disk surface, made up of a cushion of air that keeps the two objects from touching. Smaller flying heights permit denser data storage but require more precise mechanical designs. Also known as fly height.

FORMAT – To write a magnetic track pattern onto a disk surface, specifying the locations of the tracks and sectors. This information must exist on a disk before it can store data.

FORMATTED CAPACITY – The amount of room left to store data on a disk after writing sector headers, boundary definitions, and timing information during a format operation. The size of a Quantum drive is always expressed in formatted capacity, accurately reflecting the usable space required.

FORM FACTOR – The industry standard that defines the physical, external dimensions of a particular device. For example, most Quantum hard disk drives use a 3 1/2-inch form factor.

G

GUIDE RAILS – Plastic strips attached to the sides of a hard disk drive in an IBM PC/AT or compatible computer so that the drive easily slides into place.

H

HALF-HEIGHT – Standard drive size equivalent to half the vertical space of a 5 1/4-inch drive.

HARD DISK – A type of storage medium that retains data as magnetic patterns on a rigid disk, usually made of an iron oxide or alloy over a magnesium or aluminum platter. Because hard disks spin more rapidly than floppy disks, and the head flies closer to the disk, hard disks can transfer data faster and store more in the same volume.

HARD ERROR – A data error that persists when the disk is re-read, usually caused by defects in the physical surface.

HARD-SECTORED – The most common method of indicating the start of each sector on a disk, based on information located in the embedded servo. This method is more precise than soft-sectored techniques and results in lower overhead. (See also *soft-sectored.*)

HEAD – The tiny electromagnetic coil and metal pole used to create and read back magnetic patterns on the disk. Also known as read/write head.

HEAD CRASH – Damage to the read/write head, usually caused by sudden contact with the disk surface. Head crash can also be caused by dust and other particles.

HIGH-CAPACITY DRIVE – By industry conventions typically a drive of 100 megabytes or more.

HIGH-LEVEL FORMATTING – Formatting performed by the operating system to create the root directory, file allocation tables and other basic configurations. (See also *low-level formatting.*)

HOME – Reference track used for recalibration of the actuator. Usually the outermost track (track 0).

HOST ADAPTER – A plug-in board that acts as the interface between a computer system bus and the disk drive.

I

IDE – Integrated Device Electronics. The term used for the interface on drives with embedded controllers that can be directly connected to the AT system bus. This connection can be through a 40-pin connector on the motherboard or an adapter board that contains only the drive-select decoding logic. Quantum AT drives use the IDE interface.

INITIALIZATION – See *low-level formatting.*

INTERFACE – A hardware or software protocol, (contained in the electronics of the disk controller and disk drive) that manages the exchange of data between the drive and computer. The most common interfaces for small computer systems are AT (also known as IDE) and SCSI.

INTERLEAVE – The arrangement of sectors on a track. The Interleave Factor is the number of sectors that pass beneath the read/write heads before the next sector arrives. For example, a 3:1 interleave factor means that the heads read a sector, then let two pass by before reading another, requiring three full revolutions of the disk to access the complete data track. Quantum drives have an interleave factor of 1:1, allowing the system to access a full track of data in a single revolution.

INTERLEAVE FACTOR – The number of sectors that pass beneath the read/write heads before the next numbered sector arrives. When the interleave factor is 3:1, a sector is read, two pass by, and then the next is read. It would take three revolutions of the disk to access a full track of data. Quantum drives have an interleave of 1:1, so a full track of data can be accessed within one revolution of the disk, thus offering the highest data throughput possible.

INTERNAL DRIVE – A drive mounted inside one of a computer's drive bays, or a hard disk on a card installed in one of the computer's expansion slots.

ISA – Industry Standard Architecture. The standard 16 bit AT bus as designed by IBM for their PC/AT system. This has been the only industry standard bus for PCs until the recent release of MCA (Micro Channel Architecture) and EISA (Extended Industry Standard Architecture). (See also *EISA.*)

J

JUMPER – A tiny box that slips over two pins on a circuit board, connecting the pins electrically. Some board manufacturers use Dual In-Line Package (DIP) switches instead of jumpers.

K

KILOBYTE (K) – A unit of measure consisting of 1,024 (2^{10}) bytes.

L

LANDING ZONE – A non-data area on the disk's inner cylinder where the heads can rest when the power is off.

LATENCY – The time during which the read/write heads wait for the data to rotate into position after the controller starts looking for a particular data track. If a disk rotates at 3,600 rpm, the maximum latency time is 16.4 milliseconds, and the average latency time is 8.2 milliseconds.

LOGICAL BLOCK - See Block.

LOGICAL FORMAT – In connection with standard disk formatting, refers to low-level formatting. In relation to DOS-specific format requirements, refers to the translations accomplished by the controller in situations where the hard drive data configurations do not match DOS format limitations.

LOOK AHEAD – The process of anticipating events in order to speed up computer operations. For example, the system can buffer data into cache RAM by reading blocks in advance, preparing the system for the next data request.

LOW-LEVEL FORMATTING – The process of creating sectors on the disk surface so that the operating system can access the required areas for generating the file structure. Quantum drives are shipped with the low-level formatting already completed. Also known as *initialization.*

M

MB – See *megabyte.*

MEDIA – The magnetic film that is deposited or coated on an aluminum substrate which is very flat and in the shape of a disk. The media is overcoated with a lubricant to prevent damage to the heads or media during head take off and landing. The media is where the data is stored inside the disk in the form of magnetic flux or polarity changes.

MEGABYTE (MB) –Quantum defines megabyte as 10^6 bytes or 1,000,000 bytes.

MEGAHERTZ – A measurement of frequency in millions of cycles per second.

MHz – See *megahertz.*

MICROPROCESSOR – The integrated circuit chip that performs the bulk of data processing and controls the operation of all of the parts of the system. A disk drive also contains a microprocessor to handle all of the internal functions of the drive and to support the embedded controller.

MICROSECOND (µs) – One millionth of a second (.000001 sec.).

MILLISECOND (ms) – One thousandth of a second (.001 sec.).

MTBF – Mean Time Between Failure. Reliability rating indicating the failure rate expected of a product expressed in power on hours (POH). Since manufacturers differ in the ways they determine the MTBF, comparisons of products should always take into account the MTBF calculation method.

MTTR – Mean Time To Repair. The average time it takes to repair a drive that has failed for some reason. This only takes into consideration the changing of the major sub-assemblies such as circuit board or sealed housing. Component level repair is not included in this number as this type of repair is not performed in the field.

O

OVERHEAD – *Command overhead* refers to the processing time required by the controller, host adapter, or drive prior to the execution of a command. Lower command overhead yields higher drive performance. (See also *zero command overhead.*) *Disk overhead* refers to the space required for non-data information such as location and timing. Disk overhead often accounts for about ten percent of drive capacity. Lower disk overhead yields greater disk capacity.

OVERWRITE – To write data on top of existing data, erasing it.

OXIDE – A metal-oxygen compound. Most magnetic coatings are combinations of iron or other metal oxides, and the term has become a general one for the magnetic coating on tape or disk.

P

PARTITION – A portion of a hard disk dedicated to a particular operating system and application and accessed as a single logical volume.

PERFORMANCE – A measure of the speed of the drive during normal operation. Factors affecting performance are seek times, transfer rate and command overhead.

PERIPHERAL – A device added to a system as an enhancement to the basic CPU, such as a disk drive, tape drive or printer.

PHYSICAL FORMAT – The actual physical layout of cylinders, tracks, and sectors on a disk drive.

PLATED MEDIA – Disks that are covered with a hard metal alloy instead of an iron-oxide compound. Plated disks can store greater amounts of data than their oxide-coated counterparts.

PLATTER – Common term referring to the hard disk.

POH – Power On Hours. The unit of measurement for Mean Time Between Failure as expressed in the number of hours that power is applied to the device regardless of the amount of actual data transfer usage. (See also *MTBF.*)

POSITIONER – See *actuator.*

PROGRAMMED I/O – In a disk drive with an AT interface, data may be transferred between the drive and host using programmed I/O (PIO). In this case, the registers in the disk drive are accessed using host

address lines A0-A2, chip select signals CS1FX-and CS3FX-, and read/write signals IOR– a nd IOW–. The host uses PIO to write to the Command Block Registers when transmitting commands to the drive, and to the Control Block Registers when transmitting control, such as a software reset.

R

RAM – Random Access Memory. An integrated circuit memory chip that allows information to be stored and retrieved by a microprocessor or controller. The information may be stored and retrieved in any order, and all storage locations are equally accessible.

RAM DISK – A "phantom" disk drive created by setting aside a section of RAM as if it were a group of regular sectors. Access to RAM disk data is extremely fast, but is lost when the system is reset or turned off.

READ AFTER WRITE – A mode of operation requiring that the system read each sector after data is written, checking that the data read back is the same as the data recorded. This operation lowers system speed but raises data reliability.

READ VERIFY – A data accuracy check performed by having the disk read data to the controller, which then checks for errors but does not pass the data on to the system.

READ/WRITE HEAD – The tiny electromagnetic coil and metal pole piece used to create and read back the magnetic patterns (write or read information) on the disk. Each side of each platter has its own read/write head.

REMOVABLE DISK – Generally said of disk drives where the disk itself is meant to be removed, and in particular of hard disks using disks mounted in cartridges. Their advantage is that multiple disks can be used to increase the amount of stored material, and that once removed, the disk can be stored away to prevent unauthorized use.

RLL – Run Length Limited. A method of encoding data into magnetic pulses. The RLL technique permits 50% more data per disk than the MFM method, but requires additional processing.

ROM – Read-Only Memory. Integrated circuit memory chip containing programs that can be accessed and read but can not be modified.

ROTARY ACTUATOR – The rotary actuator replaces the stepper motor used in the past by many hard disk manufacturers. The rotary actuator is perfectly balanced and rotates around a single pivot point. It allows closed-loop feedback positioning of the heads, which is more accurate than stepper motors.

ROTATIONAL LATENCY – The delay between when the controller starts looking for a specific block of data on a track and when that block rotates around to where it can be read by the read/write head. On average, it is half of the time needed for a full rotation (about 8 ms.).

S

SECTOR – On a PC hard drive, the minimum segment of track length that can be assigned to store information. On Macintosh and UNIX drives, sectors are usually grouped into blocks or logical blocks that function as the smallest data unit permitted. Since these blocks are often defined as a single sector the terms block and sector are sometimes used interchangeably in this context. (Note: The usage of the term block in connection with the physical configuration of the disk is different from its meaning at the system level. See also *block* and *cluster* for comparison.)

SEEK – A movement of the disk read/write head to a specific data track.

SERVO DATA – Magnetic markings written on the media that guide the read/write heads to the proper position.

SERVO SURFACE – A separate surface containing only positioning and disk timing information but no data.

SETTLE TIME – The interval between the arrival of the read/write head at a specific track, and the lessening of the residual movement to a level sufficient for reliable reading or writing.

SHOCK RATING – A rating, expressed in "G's", of how much shock a disk drive can sustain without damage.

SOFT ERROR – A faulty data reading that does not recur if the same data is reread from the disk, or corrected by ECC. Usually caused by power fluctuations or noise spikes.

SOFT-SECTORED – Old time-based method of indicating the start of each sector on a disk. Soft-sectored drives require that location instructions be located in the data fields. (See also *hard-sectored.*)

SPINDLE – The drive's center shaft, on which the hard disks are mounted. A synchronized spindle is a shaft that allows two disks to spin simultaneously as a mirror image of each other, permitting redundant storage of data.

SPUTTER – A special method of coating the disk that results in a hard, smooth surface capable of storing data at a high density. Quantum disk drives use sputtered thin film disks.

STEPPER – A type of motor that moves in discrete with each electrical pulse. Stepper were originally the most common type of actuator engine, since they can be geared to advance a read/write head one track per step. However, they are not as fast, reliable, or durable as the voice coil actuators found in Quantum disk drives. (See also *voice coil.*)

SUBSTRATE – The material underneath the magnetic coating of a disk. Common substrates include aluminum or magnesium alloys for hard drives, glass, for optical disks, and mylar for floppy disks.

SURFACE – The top or bottom side of a disk, which is coated with the magnetic material for recording data. On some drives one surface may be reserved for positioning information.

T

THIN FILM – A type of coating allowing very thin layers of magnetic material, used on hard disks and read/write heads. Hard disks with thin film surfaces can store greater amounts of data.

TPI – Tracks Per Inch. The number of tracks written within each inch of disk's surface, used as a measure of how closely the tracks are packed on a disk surface. Also known as *track density.*

TRACK – One of the many concentric magnetic circle patterns written on a disk surface as a guide for storing and reading data. Also known as *channel.*

TRACK DENSITY – How closely the tracks are packed on a disk surface. The number is specified as tracks per inch (TPI).

TRACK-TO-TRACK SEEK TIME – The time required for the read/write heads to move to an adjacent track.

TRANSFER RATE – The rate at which the disk sends and receives data from the controller. The sustained transfer rate includes the time required for system processing, head switches and seeks, and accurately reflects the drive's true performance. The burst mode transfer rate is a much higher figure that refers only to the movement of data directly into RAM.

U

UNFORMATTED CAPACITY – The total number of usable bytes on a disk, including the space that will be required to later to record location, boundary definitions, and timing information. (See *formatted capacity* for comparison.)

V

VOICE COIL – A fast and reliable actuator motor that works like a loud speaker, with the force of a magnetic coil causing a proportionate movement of the head. Voice coil actuators are more durable than their stepper counterparts, since fewer parts are subject to daily stress and wear. Voice coil technology is used in all Quantum drives.

W

WEDGE SERVO – The position on every track that contains data used by the closed loop positioning control. This information is used to fine tune the position of the read/write heads exactly over the track center.

WINCHESTER DISKS – Former code name for an early IBM hard disk model, sometimes still used to refer to hard drives in general.

WRITE ONCE – An optical disk technology that allows the drive to store and read back data, but prevents the drive from erasing information once it has been written.

X

XT – On the bus level, the original 8-bit version of what is now the AT bus.

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