SPECTRA 70

RADIO CORPORATION OF AMERICA • ELECTRONIC DATA PROCESSING

SYSTEMS INFORMATION MANUAL

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SYSTEMS DESCRIPTION

INTRODUCTION

The RCA Spectra 70 Series provides an open-ended family of compatible data processing systems. Spectra 70 with its wide range of system configurations and all-purpose design meets the requirements of the user in all areas of commercial, scientific, multisystem, control, and communications applications. Through the use of the RCA Standard Interface (standard input-output packaging), new devices for general or special applications can be added without undergoing major redesign costs. In addition, the RCA Standard Interface permits the extension of possible system configurations at an extremely favorable, cost-performance basis.

The RCA Spectra 70 Series is a multilingual system capable of accepting and processing a wide variety of industry accepted codes and programming languages. The high-order models feature micromagnetic memories for nanosecond processing power and extensive instruction complements. Internal circuitry consists of the latest developments in the state of the art. As an example, two models use full third-generation circuitry featuring monolithic integrated circuits that produce the best combination of reliability and physical size yet achieved by the industry. Design has been left open-ended to permit the addition of subsequent advanced concepts as they become available.

SYSTEMS STRUCTURE

The RCA Spectra 70 Series consists of a line of extremely fast and powerful processors with the capability to process a variety of diverse applications. An unexcelled throughput rate is ensured by offering a complete range of input-output devices that can be applied throughout the series.

Presently there are four processors offered within the Spectra 70 Series; Models 70/15, 70/25, 70/45, and 70/55. The common code structure is based on the Extended Binary Coded Decimal Interchange Code (EBCDIC) of eight bits plus parity. The standard memory unit is termed a byte. Memory access ranges from two microseconds down to 0.84 microsecond. Transfer at these access speeds varies from one to four bytes, depending upon the model processor used.

Memory storage capability starts at 4,096 bytes and extends to 524,288 bytes. The user is provided with extensive memory overlap between models; thus, system growth can be directed towards increased memory requirements and/or increased processing power.

In the area of system throughput, simultaneous input-output processing is provided by the use of input-output channels. A selector channel is capable of addressing up to 256 devices, one at a time. The number of selector channels depends upon the processor. In addition, a multiplexor channel capable of simultaneously addressing up to 256 input-output devices is available on Models 70/25, 70/45 and 70/55 Processors. The multiplexor provides simultaneous operation of devices by time-sharing the channel.

RCA Model 70/15 Processor

The RCA Model 70/15 is a small-scale processor that allows the user to handle varied applications. It can stand alone as a data processor, function as satellite support for larger systems, or operate as a remote communication terminal.

Memory is available in either 4,096 bytes or 8,192 bytes. Memory-cycle time is two microseconds to access one byte of information.

RCA Model 70/25 Processor

The RCA Model 70/25 is a small-to-medium size processor that accommodates a wide-range of applications. It may be used as a free standing data processor or as a subsystem of a multisystem complex.

High-throughput rate is facilitated by fast memory cycle time and a high degree of input-output simultaneity. The 70/25, equipped with selector channels and a multiplexor channel, concurrently operates up to eight slow-speed devices in addition to eight high-speed devices.

Memory storage is expandable from 16,384 bytes to 32,768 bytes or 65,536 bytes. Memory-cycle time is 1.5 microseconds to access four bytes information.

RCA Model 70/45 Processor

The Model 70/45 is a medium-scale processor with a high performance capability for business, scientific, communications, and real-time applications. A complete and powerful instruction complement with floating-point operation as an option is available to the 70/45 user.

The 70/45, equipped with a communication multiplexor, addresses up to 256 communications lines in addition to a full range of peripherals. Thus, the 70/45 is an ideal system central for a multisystem operation and/or a powerful communication switching system up to 259-way simultaneity is possible.

Memory storage is expandable from 16,384 bytes to 32,768 bytes to 65,536 bytes to 131,072 bytes to 262,144 bytes. Memory-cycle time is 1.44 microseconds to access two bytes of information.

RCA Model 70/55 Processor

The RCA Model 70/55 is a medium-to-large scale processor with excellent performance characteristics. Though capable of the most demanding scientific applications, the 70/55 maintains a high-throughput capability with up to 14-way simultaneity, thereby offering a total solution to all data-processing requirements.

Memory storage is expandable from 65,536 bytes to 131,072 bytes to 262,144 bytes to 524,288 bytes. Memory-cycle time is 0.84 microsecond to access four bytes of information.

Input-Output Devices

Input-output devices in the Spectra 70 Series are systems-oriented towards the processing task to be performed:

- Card punches are fully buffered and punch at either 100 or 300 cards per minute.
- Three models of printers are offered. A medium-speed printer prints up to a rate of 600 lines per minute, and a high-speed printer prints up to a rate of 1,250 lines per minute, both printers contain a 132 print-position carriage. A bill-feed printer is also available which prints at a speed of 600 lines per minute on continuous forms and a print rate of 800 cards per minute on card documents. A read-compare feature is optional. To ensure maximum system capability, all printers are fully buffered.
- Card reading up to 1,435 cards per minute is performed photoelectrically. Optional mark reading is available.
- Paper-tape capability of 5, 6, 7 or 8-channel operation is offered at a reading rate of 200 characters per second and a punching rate of up to 100 characters per second.
- Three versions of magnetic tape units are available. Tape speeds are 30, 60, or 120 kilobytes per second. In a numeric mode, tape reading and writing are performed up to 240,000 digits per second. All units are industry-compatible and contain extensive accuracy control features. Either 7 or 9-channel tape code can be read in either the forward or reverse direction.
- Within the Spectra 70 Series, a complete complement of auxiliary storage devices capable of use on either a random or serial basis is available including:
  a. High-speed drum with an average access time of 8.6 milliseconds and a capacity of up to one-million bytes.
  b. Interchangeable disc-storage units storing up to 7.25 million bytes with a transfer rate of 156 kilobytes per second.
  c. Mass storage units capable of accessing multi-billion bytes of information in the millisecond range.
- The growing importance of optional-character reading is recognized in the Spectra 70 Series by the inclusion of the Videoscan Document Reader capable of reading up to 1,300 documents per minute on demand. An optional feature allows the Videoscan to function as a slow-speed card reader.
- In addition, a wide range of special-purpose, input-output devices is offered to the Spectra 70 user.

SYSTEMS CHARACTERISTICS

Design Philosophy

The prime design criteria of the Spectra 70 Series was to engineer a group of data processing systems utilizing the latest RCA technological developments. This concept produced an advanced series of computing systems which can be effectively and efficiently used to solve present and future problems. The inclusion of highly advanced circuitry in the Spectra 70 Series provides speed, accuracy, and reliability at lower cost.

The use of monolithic integrated circuits in the RCA Models 70/45 and 70/55 safeguards system longevity by producing a series of data processors with the highest order of compactness and reliability. Circuits are produced by advanced photographic and thin-film techniques and are hermetically sealed to ensure optimum efficiency in their operating environment. Circuits that formerly required a full board for construction are now placed on a 4-millimeter square. Coupled with reliability, this compactness illustrates the significance of the monolithic integrated circuit.

The internal speed of the processors in the series is another achievement in the overall advanced-system design. The ability to combine internal processing speeds and potential data throughput rates with the various peripheral devices allows for the creation of a systems series

which provides an ideal balance between processing capacity and cost. Scratch-pad memories in the higher range models operating at billionths of a second speed provide intermediate storage for registers and interrupt control.

The accuracy and reliability of data are maintained through the system by continued parity checking. Each memory access embodies a parity check to assure accuracy. If an error occurs, the processor interrupts processing until parity is restored.

Expandability

The RCA Spectra 70 Series provides memory expansion and peripheral expansion in both throughput capabilities and in the number of input-output devices. Fourteen separate processors are offered within the series, ranging from a 4,096-byte memory and expanding to a 524,288-byte memory. This model array allows the user up to a threefold-horizontal increase in processing power within a given memory size, and a vertical increase in memory size within an individual processor model.

Input-output simultaneity is a function of the selector and multiplexor channels in a system. The user can adjust the throughput capability of a Spectra 70 system by the addition of extra channels. Depending upon the series model, up to eight selector channels and one multiplexor channel can be added.

A variety of input-output devices varying in speed and capacity allows for peripheral expansion. This is accomplished by the use of the RCA Standard Interface which permits interchangeability of peripherals between processors without a penalty of increased control costs or abridgement of the device-rated speed.

Compatibility

The Spectra 70 Series features program compatibility between individual models. Equipment compatibility may be upward as in the 70/15 to 70/25, 70/25 to 70/45 and 70/55, or upward and downward as in the 70/45 and 70/55. Program compatibility requires that the ensuing model have at least the configuration of its predecessor, and that timings, both internal and external, are not adversely effected.

Spectra 70 program compatibility offers the user the advantages of systems back-up, ease in system growth, and reduction in the personnel training between series models.

Programming Systems

Advanced-programming systems including input-output control systems, operating systems, generative systems, multiprocessing, COBOL, and FORTRAN IV are offered within the Spectra 70 Series.

The level of programming-system support is classified primarily by available memory in addition to the input-output orientation of the particular series model. Provisions are made for the user to elect either a completely programmed operating environment or one where the system is under operator supervision or a combination of both.

Code Structure

The Spectra 70 Series coding structure is based on the widely used Extended Binary Coded Decimal Interchange Code (EBCDIC). The series also offers the facilities for generating and using the American Standard Code for Information Interchange (ASCII).

To facilitate efficient manipulation of alphanumeric data, an 8-bit byte is used to represent each character. This allows the Spectra 70 Series to accept most present or future character codes. An 8-bit byte may represent one alphanumeric character, two decimal digits or eight binary digits (bits).

Fixed-length data of 16, 32, or 64 bits may be processed. Variable-length data of up to 256 characters in eight bit bytes may be processed. For purposes of data description the terms character, halfword, word, and double word are used. These are defined as one, two, four, and eight bytes respectively.

Machine Addressing

The Spectra 70 Series uses a two-part system of memory addressing consisting of a base address and a displacement address. A standard 12-bit instruction enables the programmer to address up to 4,096 bytes. This part is termed the displacement. A base address, stored in a General Register, consists of a maximum 32 bits and addresses memory beyond the capacity of the displacement address. Thus, the base address, in effect, subdivides memory into 4,096 bytes in that the displacement addresses the individual byte within the 4,096-byte module. The memory capacity of the Model 70/15 Processor obviates the need for a base address in that the displacement has the necessary addressing range by the addition of a high-order bit to permit addressing of up to 8,192 bytes.

Instruction Format

The Spectra 70 Series uses a variable-instruction format consisting of 2, 4, or 6-byte instructions. Each instruction contains an operation halfword (two bytes), and one or two register and/or memory addresses as required. Each address may be indexed by any of the General-Purpose registers in combination with the Base Address register.

The smaller processors contain instruction complements which are functional subsets of the larger 70/45 and 70/55 instruction complements. Floating-point operation is standard on the 70/55 and optional on the 70/45. Direct-control and memory-protect are optional features on both the 70/45 and 70/55. There are provisions for expanding the instruction complement to 256 order codes.

Arithmetic Operations

Complete flexibility in handling arithmetic operations is offered in the Spectra 70 Series. Decimal and binary operations are available throughout the series model. Floating-point operations are available on the 70/45 and 70/55 Processors.

Decimal operations are performed on variable or fixed-signed fields in packed format (two digits per byte). The maximum field size permitted is 31 digits plus sign and the operation is performed storage to storage.

Binary or fixed-point arithmetic operations uses either storage or registers for computation depending on the series model. In the 70/15 and 70/25, a 127-bit field plus sign is permissible. In the 70/45 and 70/55 the limit is a 31-bit field (plus sign) and arithmetic is performed in the registers (registers may be coupled to preserve precision).

Where floating-point arithmetic operations are provided, four additional double-length registers are provided for computation and storage of results. Both short and long precision, four and eight bytes respectively, are provided for either a speed or precision option. Limits of floating-point values are 2.4×10^{-78} to approximately 7.2×10^{75}.

Interrupt

The Spectra 70 Series includes a comprehensive set of system interrupts. These interrupts allow the particular series model to respond to various internal and external conditions affecting systems operation. Processing at the time of the interrupt may be terminated, suppressed, or completed, depending on the cause of the interrupt. Processor interrupts, in general, may be controlled by the program through the use of interrupt masks.

Interrupts are divided into the following classifications:

Program Interrupts — program errors such as overflows and illegal operation codes.

External Interrupts — servicing remote and operator-controlled devices, such as console intervention and requests from display or analog devices.

Supervisor Call Interrupts — interrupts caused by the user's program to request various functions in the operating system.

Input-Output Interrupts — input-output servicing of devices, such as terminations, transfer errors, and inoperable conditions.

Machine Interrupts — equipment malfunctions such as parity error or power shut-down.

If more than one interrupt occurs simultaneously, the interrupts will be serviced in a fixed-order of priority. After servicing of the interrupt condition, linkage will be provided to the pre-interrupt conditions, if desired.

Processor States

Concurrent with the interrupt mechanism, Spectra 70 Systems may have up to four processor states. These processor states facilitate program control of interrupt conditions and normal processing operations. In effect, processor states reflect the particular status of a system at a given time in relation to the functions being performed.

These processor states deal with normal processing, interrupt mechanism, operating systems, and machine malfunctions. The 70/15 and 70/25 contain two processor states while the 70/45 and 70/55 contain four processor states.

In the 70/45 and 70/55 the combinations of interrupt and processor states are carried to their logical extension in that each state contains its own complete interrupt system. The effect of each state having its own masks, registers, and instruction sets facilitates the servicing of the interrupt mechanism with a minimum of program manipulation.

Input-Output Channels

The control of the transmission of data between the processor and an associated peripheral device is accomplished through channels and the RCA Standard Interface. A channel may be considered as an independent unit controlling data flow to and from the processor, and releasing control to the input or output device. This release allows the processor to function simultaneously with the input-output operation.

Each channel utilizes its own set of commands to perform input-output operations. These commands, referenced as channel commands, control the device once a start command has been given by the processor. Chaining of channel commands provides a means by which several operations, such as multiple reads, may be completed independently of the processor.

The RCA Standard Interface functions as a connector between the channel and a device control. The interface establishes an identical relationship with each input-output device in that any device may be connected to the interface regardless of type, size, or speed. The number of channels and interfaces connected varies with the processor model. Within the Spectra 70 Series there are two types of channels: selector channels and multiplexor channels.

Selector Channel

The selector channel in the Spectra 70 Series controls the transfer of data to and from a peripheral device. These selector channels operate independently of the processor. A selector channel has from one to four trunks, depending upon the processor model. A controller determines the number of devices that can be connected to a trunk. For example, a tape controller controls as many as 16 tape devices. Channels can operate concurrently resulting in the overlap of input-output operations. The transfer rate of the selector channel depends upon the speed of the particular processor.

Multiplexor Channel

The multiplexor channel provides a unique method through which varying speed peripheral devices may be attached. Speed variances are accommodated by having available two different transmission modes: Multiplex mode and Burst mode.

The Multiplex mode is used when low-speed devices are attached to a processor and the channels data track is time-shared by all of the low-speed devices connected to the multiplexor. In this instance, every low-speed device may be operated simultaneously by the multiplexor channel sending and receiving the required data. The devices in the slow-speed range are printers, card readers, card punches, paper-tape reader-punch, and display terminals.

The Burst mode must be used when high-speed devices are operated via the multiplexor; however, in the Burst mode, only a single input-output device may use the channel at one time. Tape drive, disc, drum, and mass memory equipment are devices which must operate in the Burst mode. The multiplexor channel normally runs multiple devices on a time-sharing basis. A Burst mode occurs automatically under certain conditions or is specified by a modification of the input-output command. The Burst mode is limited to the Model 70/45 and 70/55 Processors. The multiplexor channel divides the data track into sub-channels over which the data will flow. Each sub-channel may be individually addressed by the program. The multiplexor channel may contain up to eight input-output trunks from which up to 256 devices may be connected.

Communications

In the normal execution of today's business, data communications is becoming an integral part of the information interchange between operations, administrative, and managerial groups. Efficient operation is a result of using the most current and accurate information available. The integration of communications and processing provides the means for gathering, processing, and disseminating data to the individuals and groups concerned with its use. Message switching, inquiry and response, data collection, and management information systems are indicative of the diversified communications capabilities of the Spectra 70 Series.

To meet the demands of these systems, RCA has designed a comprehensive range of processors and communications equipment in the Spectra 70 Series. The design criteria employed in the series makes it possible for RCA to tailor systems specifically to fit the user's needs.

Each processor in the series has communications capabilities when equipped with the appropriate communication equipment. This equipment provides single and multiple-circuit handling; low and high-speed transmission rates; short and long-distance communications capabilities; and the performance characteristics required to operate with small unsophisticated systems as well as large complex systems.

Communication Control

The communication control provides single-channel, long-distance, processor-to-processor communication via telephone lines. Large volumes of data can be transmitted between processors at distant locations making it possible to shorten reporting and data delivery cycles as well as ensuring the delivery of the most current information available. Speed and accuracy are the prime considerations in the design and operation of this device.

Data Exchange Control (DXC)

The Data Exchange Control (DXC) enables two RCA processors to communicate with each other. Data transmission may be in either direction, but in only one direction at a time. The DXC facilitates transmission of data at high rates dependent upon the type of channel used and the number of simultaneous active devices attached to the transmitting and receiving processors.

The DXC is a powerful tool for multisystem applications. Large volumes of data can be exchanged between processors for storage, further processing, and/or other peripheral action. In a real-time system, status information, and queue tables are transmitted to the backup processor. This data is used by the backup processor in the event of a change in operational tasks. The utilization of a DXC in a multiprocessor system affords flexibility and an extension of processing capabilities.

Communication Multiplexor Channel

Multiple-channel communications capabilities are provided by the Communication Multiplexor Channel (CMC). The CMC performs input and output functions in the 70/45 System by exchanging timing, control, and data over the RCA Standard Interface with the appropriate controls and devices. The CMC is completely flexible with respect to the number of lines, the type of lines, the mixture of speeds, and the variety of remote devices it can communicate with.

The 70/45 Processor equipped with a CMC addresses up to 256 devices. These devices are not limited to communications devices but can be standard input-output peripherals. Any combination of peripheral and communication devices may be connected to the CMC up to the maximum capacity. Inclusion of a communication multiplexor channel, replaces the standard multiplexor channel.

Single station and multistation circuit operations are accommodated by the CMC and its associated control and buffering equipment. Depending upon the system characteristics and the operational requirements, a combination of communication equipment and program provide direction, coordination, and the data-handling capacity necessary for the Model 70/45 Processor to function as a powerful communications center.

The CMC operates with a wide range of devices at a variety of speeds. Both high-speed and low-speed devices may be serviced concurrently. The maximum data rate of the CMC is 62 kilobytes per second.

Communications Buffers

The Spectra 70 Series includes a wide range of communications buffers capable of interfacing telegraph as well as data-communications devices and systems. The operational and performance characteristics of these buffers are selectable. They are dependent upon the requirements of the particular device or system for which they are designed to interface.

Each buffer in the series operates at a specific range of transmission speeds, code levels, and with specific communications devices and systems. The buffer is the interface between the communication line and the communication buffer control. This control enables the 70/45 Processor, equipped with a communication multiplexor channel, to receive and transmit data.

Memory Protect

The protection of memory segments from destruction by programming or input devices is provided in the Models 70/45 and 70/55 Processors through the memory-protect feature.

Memory-protect feature can, depending upon availability of memory, protect up to 15 memory segments or programs from address interaction. The basic segment consists of 2,048 bytes and is increased in multiples of 2,048 bytes. Memory-protect feature is a processor function and does not require memory allocation nor does it increase instruction timing.

Memory-protect feature consists of a set of registers which are constantly scanned during instruction addressing to ascertain that the address falls within preset limits (segments). When an address is detected that exceeds the allowable limitation, an interrupt condition is set and appropriate action is taken.

This feature greatly enhances the capability for multiprogramming in the Spectra 70 Series.

Direct Control

The optional direct-control feature offered in the Models 70/45 and 70/55 Processors provides control and synchronizing information between the processors and/or special external devices. This direct-control feature provides two instructions that implement the transfer of one byte of information between the memory and an external device. The direct control also provides six external-signal lines effecting an external interrupt.

Elapsed-Time Clock

An elapsed-time clock for real-time control is available in the Spectra 70 Series. This feature is standard in the 70/25 system and optional in the 70/45 and 70/55 Systems. The timer is maintained on either a 50 or 60 cycle-per-second-rate providing an interrupt capability every 16.67 milliseconds or at the termination of the timer's full cycle. The elapsed-time clock can be reset by the programmer at any time.

MULTISYSTEM OPERATION

Multisystem operation is available in the Spectra 70 Series. Through the use of shared input-output devices and/or data exchange controls (for memory-to-memory transmission), the expansion of a given processor's power for multisystem communication is provided. In addition, multisystem capability is an added advantage for enhancing system reliability in real-time applications.

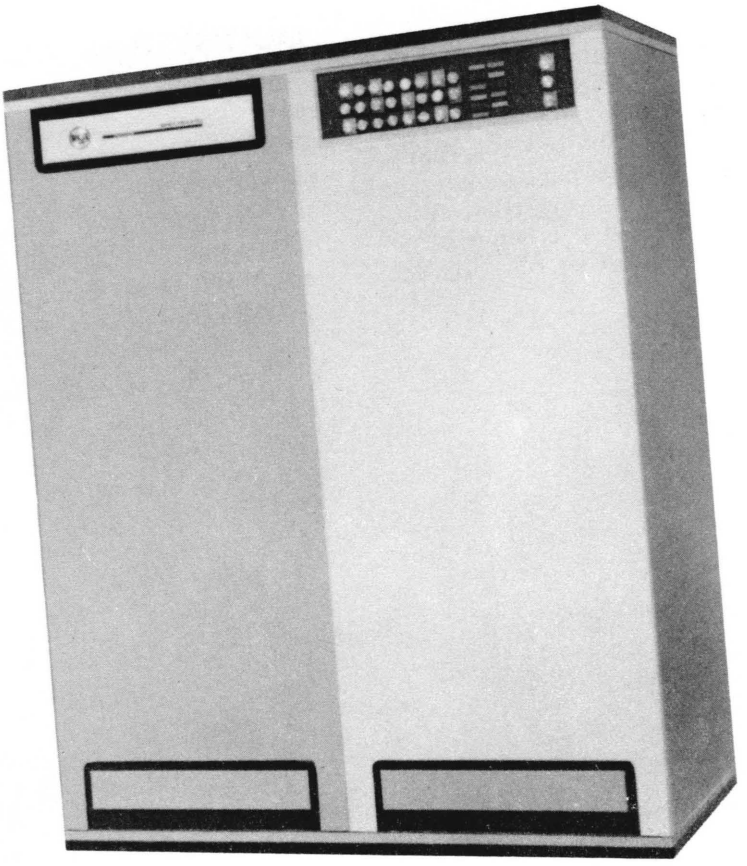

Figure 1. RCA 70/15 System

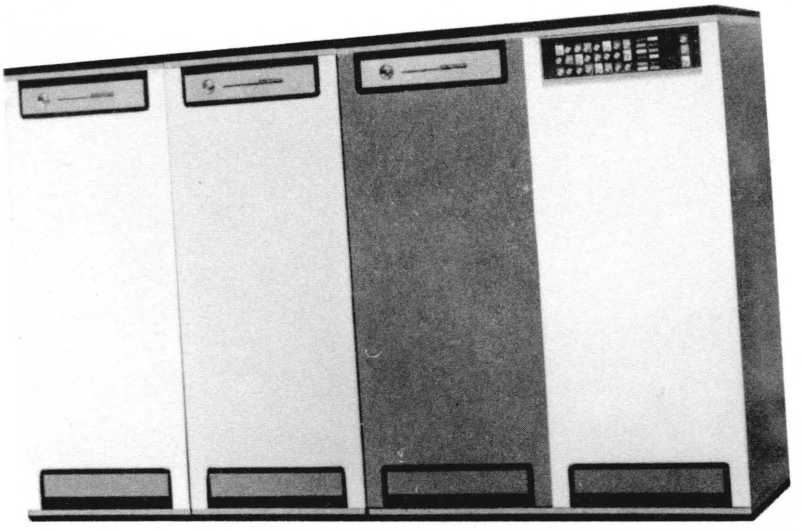

Figure 2. RCA 70/25 System

EQUIPMENT DESCRIPTION

RCA MODEL 70/15 PROCESSOR

General

The RCA Model 70/15 Processor, smallest member of the Spectra 70 Series, is a powerful data processing system designed specifically for small-scale data applications and low-cost remote and satellite operations. The prime objective of this system is to satisfy the ever-increasing need for low-cost off-line processing. Simultaneity is provided through a read-auxiliary command for card readers and magnetic tapes. Peripheral devices such as the card punch and printer are fully buffered.

To fulfill the growth requirements of the user, the 70/15 is upward compatible within the Spectra 70 Series.

The 70/15 is a byte-organized, two-address serial processor consisting of *high-speed memory, program control,* and *input-output control.*

High-Speed Memory

High-speed memory consists of planes of magnetic cores. These planes are 64 x 64 strings; each string is one byte in depth resulting in a basic block of 4,096 bytes of separately addressable core memory. High-speed memory is field-expandable from the basic 4,096 bytes to 8,192 bytes. The byte is the smallest addressable unit in the Model 70/15 Processor.

The basic memory-cycle time is 2.0 microseconds. This is the time to transfer one byte from the 70/15 memory to the Memory register and to regenerate the byte in storage.

The first 50 bytes of high-speed memory are reserved for use by the processor. They are used as utility registers and intermediate storage media in the handling of input-output operations and interrupt processing.

Program Control

The function of the program control unit in the Model 70/15 Processor is to interpret and execute the instructions stored in high-speed memory. Necessary registers and indicators are provided by the program control unit to monitor sequence of operations, to perform automatic accuracy checks, and to communicate with the RCA Standard Interface in the control of input-output devices.

Two *processor states,* each having its own program counter, are present in the Model 70/15 Processor. They provide fast interrupt servicing and facilitate program system control. The processor states and their functions are as follows:

Processing State (P_1) — executes the user's program and is capable of being interrupted. Once interrupted, the conditions existing at the time of interrupt are automatically stored and control is transferred to the *Interrupt State (P_2).*

Interrupt State (P_2) — analyzes an interrupt condition and determines the action to be taken. Control is then transferred back to the *Processing State (P_1)* where the interrupt is serviced. This state may not be interrupted.

Program interruption capabilities are provided in the Model 70/15 Processor as follows:

1. *Request interrupt for an input-output device* — interruption of normal processing takes place upon request from the interrogating typewriter, communications control, or data exchange control to process remote inquiries or data transmissions.
2. *Internal operation code trap* — an interrupt occurs when an undefined operation code in the 70/15 instruction set is recognized. This provides the facility to simulate operations not included in the standard 70/15 instruction set.

When an interrupt signal is received by the processor, the actual interrupt takes place as soon as the current instruction terminates.

All interrupts (except internal operation code trap) may be inhibited if desired. If, however, the interrupt is not inhibited, control will automatically be transferred to the *Interrupt State (P_2).* At this time, conditions existing in the *Processing State (P_1)* are stored by hardware so that an orderly return may be affected once the interrupt has been serviced.

Input-Output Control

The Model 70/15 Processor communicates with all input-output devices through the RCA Standard Interface. The input-output channel transmits data to or from a single peripheral device and is capable of handling high-speed input-output devices. Up to six standard interface trunks may be connected to the channel and each trunk can control up to 16 input-output devices.

Instruction Formats and Timing

The Model 70/15 Processor includes a standard set of 25 instructions. This instruction repertoire performs arithmetic, data handling, decision, control, and input-output operations.

All instructions must start on halfword boundaries (even-numbered byte location). The basic format of the instruction set is two, four, or six bytes long (see table 1). Twenty instructions have a two-address format and are six bytes in length. Three single-address instructions are in the instruction set and are four bytes long. Halt and Post Status instructions require only two bytes. Direct addressing is used up to the maximum of 8,192 bytes.

TABLE 1. INSTRUCTION FORMATS

Halfword			Halfword		Halfword	
Byte 1	Byte 2		Byte 3	Byte 4	Byte 5	Byte 6
8 Op Code	8 L		16 D_1		16 D_2	
8 Op Code	4 L_1	4 L_2	16 D_1		16 D_2	
8 Op Code	4 T	4 U	16 D_1		16 D_2	
8 Op Code	8 M		16 D_1			
8 Op Code	4 T	4 U				
8 Op Code	8 M					

Numbers in upper right corners of blocks indicate number of bits used.

Legend:

D_1 — address of leftmost byte of first operand.

D_2 — address of leftmost byte of second operand.

L — one less than length of first and/or second operand (0–255).

L_1 — one less than length of first operand (0–15).

L_2 — one less than length of second operand (0–15).

M — mask for Branch On Condition, Test Under Mask, and Halt.

T — input-output trunk referenced.

U — input-output device referenced.

A list of the 70/15 standard instruction set and corresponding staticizing and execution timing is tabulated in table 2. For input-output instruction timing, refer to Appendix A.

TABLE 2. INSTRUCTION TIMING

Instruction	Staticizing (μs)	Execution (μs)
ARITHMETIC INSTRUCTIONS		
Add Decimal	20	$18 + 4N_1 + 2N_2$
Add Binary	20	$18 + 4N_1 + 2N_2$
Subtract Decimal	20	$18 + 4N_1 + 2N_2$
Subtract Binary	20	$18 + 4N_1 + 2N_2$
And	20	6N
Or	20	6N
Exclusive Or	20	6N
DATA HANDLING INSTRUCTIONS		
Move	20	4N
Edit	20	4I + 4F + 6D
Pack	20	$16 + 2N_1 + 2N_2$
Unpack	20	$16 + 2N_1 + 2N_2$
DECISION AND CONTROL		
Branch on Condition	16	Branch = 4 No Branch = 2
Compare Decimal	20	$16 + 4N_1 + 2N_2$
Compare Logical	20	6B
Set P_2 Register	16	6
Test Under Mask	16	2
Halt	12	2
INPUT-OUTPUT		
Read Forward	20	See Appendix A
Read Reverse	20	
Read Auxiliary	20	
Write	20	
Write Control	20	
Erase	20	
Sense	20	
Post Status	12	

Legend:

B — number of bytes compared before an inequality occurs.

D — number of digits inserted.

I — number of edit characters inserted.

F — number of fill characters inserted.

N — number of bytes.

N_1 — number of bytes in first operand.

N_2 — number of bytes in second operand.

RCA MODEL 70/25 PROCESSOR

General

The RCA Model 70/25 Processor, the second member of the Spectra 70 Series, is a small-to-medium scale computer designed to satisfy a wide variety of data-processing requirements. The 70/25 is organized as a powerful data processor with the capability to concurrently perform up to 16 input-output operations. This input-output simultaneity, coupled with its communications capabilities, makes the 70/25 a highly efficient vehicle for high-speed remote processing. Provision is made for program compatibility between the Model 70/25 Processor and the larger processors in the Spectra 70 Series.

The 70/25 is a word-organized, variable-data format processor consisting of *high-speed memory, program control,* and *input-output control.*

High-Speed Memory

High-speed memory consists of planes of magnetic cores. These planes are 64 x 64 strings; each string is four bytes in depth resulting in a basic block of 16,384 bytes of separately addressable core memory. High-speed memory is field-expandable from 16,384, 32,768, or 65,536 bytes. The byte is the smallest addressable unit in the Model 70/25 Processor. Four 8-bit bytes are accessed in one memory cycle of 1.5 microseconds. Memory time is the time required to transfer a four-byte word from the 70/25 memory to the Memory register and to regenerate the word in storage.

The first 50 bytes of high-speed memory are reserved for use by the processor. They are used as hardware registers and intermediate storage media in the handling of input-output operations and interrupt processing. The last 100 bytes of high-speed memory are reserved for 15 General-Purpose registers, a Timer register, and Utility registers. In addition to these two memory areas, the inclusion of a multiplexor channel in the RCA 70/25 requires that high-speed memory immediately preceding the last 100 bytes be reserved for Multiplexor Channel Device registers. The amount of memory required for this purpose is dependent upon the number of devices associated with the multiplexor channel.

Program Control

The function of the program control unit in the Model 70/25 Processor is to interpret and execute the instructions stored in high-speed memory. The required registers and indicators are provided by the program control unit to monitor sequence of operations, to perform automatic accuracy checks, and to communicate with the RCA Standard Interface in the control of input-output devices.

Two *processor states,* each having its own program counter, are present in the Model 70/25 Processor. They provide fast interrupt servicing and facilitate program system control. The processor states and their functions are as follows:

Processing State (P_1) — executes the user's program and is capable of being interrupted. Once interrupted, the conditions existing at the time of interrupt are automatically stored and control is transferred to the *Interrupt State (P_2).*

Interrupt State (P_2) — analyzes an interrupt condition and determines the action to be taken. Control is then transferred back to the *Processing State (P_1)* where the interrupt is serviced. This state may not be interrupted.

Program interruption capabilities are provided in the Model 70/25 as follows:

1. *Request or termination interrupt by an input-output device* — interruption of normal processing takes place upon request from the interrogating typewriter, communications control, or data exchange control to process remote inquiries or data transmissions. An interrupt also occurs upon termination of an input-output operation.
2. *Internal operation code trap* — an interrupt occurs when an undefined operation code in the 70/25 instruction set is recognized. This provides the facility to simulate operations not included in the standard 70/25 instruction set.
3. *Arithmetic overflow or divide exception* — an interrupt occurs on all arithmetic-overflow conditions. When a Divide instruction is executed and the quotient is less than one or exceeds 29 digits (plus sign), an interrupt also takes place.
4. *Timer interrupt* — the timer may be set or altered to provide for interruption of normal processing when a specified amount of time has elapsed.

When an interrupt signal is received by the processor, the actual interrupt takes places as soon as the current instruction terminates.

All interrupts (except internal operation code trap) may be inhibited if desired. If the interrupt is not inhibited, control will automatically be transferred to the *Interrupt State (P_2).* At this time, conditions existing in the *Processing State (P_1)* are stored by hardware so that an orderly return may be affected once the interrupt has been serviced.

Input-Output Control

The Model 70/25 Processor communicates with all input-output devices through the RCA Standard Interface. Up to eight selector channels (two of which may be high speed) plus a multiplexor channel may be connected to the system, providing a high degree of simultaneity. Four selector channels (medium-speed) are standard. Each selector channel can control up to 16 devices. A set of registers is provided for each selector channel, making simultaneous operation of all channels possible. Each device (up to 115) on the multiplexor channel has its own sub-channel register. Up to eight of these devices may time-share the channel. It is possible for selector channels and multiplexor channel-connected devices, in any combination, to operate simultaneously with computing.

Instruction Formats and Timing

A comprehensive repertoire of instructions is provided with the Model 70/25 Processor. Thirty-one instructions permit a full range of data-processing capability including powerful arithmetic, data handling, decision, control, and input-output facilities.

All instructions must start on halfword boundaries (even-numbered byte locations). The basic format of the instruction set is two, four, or six bytes in length. Table 3 illustrates these formats and their construction.

TABLE 3. INSTRUCTION FORMATS

Halfword			Halfword		Halfword	
Byte 1	Byte 2		Byte 3	Byte 4	Byte 5	Byte 6
8 Op Code	8 L		4 B_1	12 D_1	4 B_2	12 D_2
8 Op Code	4 L_1	4 L_2	4 B_1	12 D_1	4 B_2	12 D_2
8 Op Code	4 T	4 U	4 B_1	12 D_1	4 B_2	12 D_2
8 Op Code	8 M		4 B_2	12 D_2		
8 Op Code	4 T	4 U				
8 Op Code	8 M					

Numbers in upper right corners of blocks indicate number of bits used.

Legend:

B_1 — register containing base address of first operand.

B_2 — register containing base address of second operand.

D_1 — address of leftmost byte of first operand.

Legend: (Cont.)

D_2 — address of leftmost byte of second operand.

L — one less than length of first and/or second operand (0–255).

L_1 — one less than length of first operand (0–15).

L_2 — one less than length of second operand (0–15).

M — mask for Branch On Condition, Test Under Mask, and Halt.

T — input-output trunk referenced.

U — input-output device referenced.

A list of the 70/25 standard instruction set and corresponding staticizing and execution timing is tabulated in table 4. Staticizing times shown are maximum and can be reduced if instructions are on fullword boundaries. For input-output instruction timing, refer to Appendix A.

TABLE 4. INSTRUCTION TIMING

Instruction	Staticizing (μs)	Execution (μs)
ARITHMETIC INSTRUCTIONS		
Add Binary	13.5	$8.25 + 2.25N_1 + 1.5N_2$
Add Decimal	13.5	$8.25 + 2.25N_1 + 1.5N_2$
Subtract Binary	13.5	$8.25 + 2.25N_1 + 1.5N_2$
Subtract Decimal	13.5	$8.25 + 2.25N_1 + 1.5N_2$
Multiply Decimal	13.5	$12.75 + 9N_1 - 1.5N_2 + C[3.75 (N_1 - N_2) + 3] 3.75 (N_1 - N_2) + 3$
Divide Decimal	13.5	$9 + 29.25N_1 - 27N_2 + 37.5N_2 (N_1 - N_2)$
AND	13.5	3.75N
OR	13.5	3.75N
Exclusively OR	13.5	3.75N
DATA HANDLING INSTRUCTIONS		
Edit	13.5	2I + 2F + 3D
Move	13.5	3W + 3B
Pack	13.5	$6 + 1.5N_1 + 3N_2$
Unpack	13.5	$7.5 + 3N_1 + 1.5N_2$
Translate	13.5	6.75N
DECISION AND CONTROL INSTRUCTIONS		
Branch and Link	9	3.75
Branch On Condition	9	Branch = 2.25; No Branch = 0.5
Branch On Count	9	Branch = 6.75; No Branch = 2.25
Compare Decimal	13.5	$6 + 1.5N_1 + 2.25N_2$

TABLE 4. INSTRUCTION TIMING (Cont.)

Instruction	Staticizing (μs)	Execution (μs)
DECISION AND CONTROL INSTRUCTIONS Cont.		
Compare Logical	13.5	1.5 + 3B
Halt	4.5	1.5
Load Multiple	9	3.75R
Set P_2 Register	9	3
Store Multiple	9	3.75R
Test Under Mask	9	1.5
INPUT/OUTPUT INSTRUCTIONS		
Erase	13.5	
Post Status	9	
Read Forward	13.5	
Read Reverse	13.5	See Appendix A.
Sense	13.5	
Write	13.5	
Write Control	13.5	

Legend:

B — number of bytes processed (or number of bytes outside fullword boundaries).
C — sum of multiplier digits.
D — number of digits inserted.
F — number of fill characters inserted.
I — number of edit symbols inserted.
N — total number of bytes.
N_1 — number of bytes in first operand.
N_2 — number of bytes in second operand.
R — number of registers.
W — number of four-byte words.

RCA MODEL 70/45 PROCESSOR

General

The RCA Model 70/45 Processor, the third member of the Spectra 70 Series, is a powerful, solid-state, general-purpose, digital processor. It is the main element of a system handling medium-large data processing applications. Because of its large storage capacity, fast data transmission, and computation rates, this processor is highly efficient as both a data processor and a scientific-problem solver. The internal logic is controlled by elementary operations stored in a read only control memory.

All instructions, character codes, interrupt facilities, and programming features are functionally the same as corresponding features on the Model 70/55. Programs may be interchanged between processors provided:

1. Systems features are equivalent.
2. Programs are written independently of strict timing considerations.
3. Programs are restricted to specified functions and do not utilize unspecified characteristics peculiar to the hardware of either processor.

The 70/45 is a diad-organized, variable-format processor consisting of *main memory, scratch-pad memory, read only control memory, non-addressable memory, program control,* and *input-output control.*

Main Memory

Main memory consists of expandable magnetic core storage available in sizes of 16,384, 32,768, 65,536, 131,072, or 262,144 bytes. The basic memory-cycle time is 1.44 microseconds. This is the time to transfer two bytes from the main memory to the Memory register and to regenerate the bytes in storage. A byte may consist of a character, two digits, or eight bits. The processor normally operates on two 8-bit bytes at a time although the minimum addressable data unit is one byte and the maximum addressable data unit is 8 bytes.

Scratch-Pad Memory

The scratch-pad memory, a fast micromagnetic storage device, contains the General-Purpose, Floating-Point, and various other registers to facilitate processor and program control. This memory consists of 128 four-byte words. Access time is 300 nanoseconds per word. Locations in the scratch-pad memory are uniquely addressed by the Load-Scratch-Pad and Store-Scratch-Pad instructions.

Four double word Floating-Point registers and 16 General-Purpose registers are contained in the scratch-pad memory. The Floating-Point registers are used in floating-point arithmetic operations. The General-Purpose registers are used in base addressing, indexing, and utility operations.

Read Only Control Memory

The read only control memory contains the internal logic for the elementary operations of the processor. Memory-cycle time is 480 nanoseconds permitting significant reduction in the instruction execution timing.

Non-Addressable Memory

This memory is a portion of the main memory that cannot be addressed by programming. A set of registers that services the devices attached to a multiplexor channel is contained in the non-addressable main memory. The size of this memory

will vary in accordance with the capacity of the main memory selected by the user. Non-addressable memory is in addition to the main memory capacity of the system.

Program Control

The Model 70/45 Processor has four distinct processor states to provide extremely fast interrupt servicing. Combined with the program systems control, these processor states provide an extremely efficient interrupt handling. The four processor states are:

Processing State (P_1) — interprets and executes the user's program. This processing state is the problem-oriented state.

Interrupt Response State (P_2) — performs specific program tasks as dictated by the *Interrupt Control State (P_3)*.

Interrupt Control State (P_3) — is automatically entered upon recognition of an interrupt other than one caused by a machine check or power failure. This state is responsible for performing a detailed analysis of the cause of interrupt and establishing its priority. Once these functions have been performed, linkage is provided to the proper interrupt processing routine in the *Interrupt Response State (P_2)*.

Machine Condition State (P_4) — is entered whenever a machine check or power failure occurs. This state analyzes the cause of a machine interrupt and establishes its priority. Control is then transferred to the *Interrupt Response State (P_2)* so that an indication of the cause of interrupt may be given to the operator.

Table 5 summarizes the type and number of registers uniquely assigned to each processor state.

TABLE 5. PROCESSOR STATE REGISTERS

Register	Processor State			
	P_1	P_2	P_3	P_4
Program Counter	1	1	1	1
General-Purpose Registers	16	16	6	5
Floating-Point Registers	8	*	*	*
Interrupt-Status Register	1	1	1	1
Interrupt-Mask Register	1	1	1	1

* Floating-point instructions executed in these states use the floating-point registers of the Processing State (P_1).

Since each processing state has its own General-Purpose registers, Interrupt Status register, and Interrupt Mask register, the need for storing and reloading registers during interrupt processing is virtually eliminated.

Program interrupts occur as a result of errors in data or instruction specifications, input-output operations, external signals, equipment malfunctions, or arithmetic errors. The instruction being executed at the time of interrupt may be completed, suppressed, or terminated depending on the cause of the interrupt.

Any interrupt may be inhibited or permitted in any state through programming. If an interrupt occurs and is permitted, conditions existing in the interrupted state will be automatically stored. Control is then passed to the *Interrupt Control State (P_3)* or *Machine Condition State (P_4)* depending upon the cause of the interrupt. The priority of the interrupt is established and an analysis is made to determine the proper linkage to the *Interrupt Response State (P_2)* so that the interrupt may be processed. Once interrupt processing has been completed, control is returned to the state which was last interrupted and normal processing is resumed.

If several interrupts occur at the same time, the one having the highest priority will be processed. The remaining interrupts will be processed in turn depending upon their priority.

Table 6 summarizes all of the interrupt conditions, their respective priorities, the interrupt state which each initiates, and a brief description of the cause of interrupt.

TABLE 6. INTERRUPT CONDITIONS

Priority	Condition	State Initiated	Explanation
1	Power Failure	4	Power failure in processor or memory.
2	Machine Check	4	Parity error or equipment malfunction.
3	External Signal 1	3	Signal received on one of the six external lines associated with the direct-control feature.
4	External Signal 2	3	
5	External Signal 3	3	
6	External Signal 4	3	
7	External Signal 5	3	
8	External Signal 6	3	
9	Not Specified		

TABLE 6. INTERRUPT CONDITIONS (Cont.)

Priority	Condition	State Initiated	Explanation
10	Selector 1 Terminate	3	A device on the associated selector channel has terminated.
11	Selector 2 Terminate	3	
12	Selector 3 Terminate	3	
13	Not specified		
14	Not specified		
15	Not specified		
16	Multiplexor Terminate	3	A device on the multiplexor channel has terminated.
17	Elapsed Time Clock	3	Elapsed time count has expired.
18	Console Request	3	Manual request for interrupt by the operator.
19	Not specified		
20	Not specified		
21	Supervisor Call	3	Result of execution of Supervisor Call instruction to utilize programmed routines.
22	Privileged Operation	3	Privileged instruction attempted in non-privileged mode.
23	Op-Code Trap	3	Op Code attempted which is invalid for this model.
24	Address Error	3	Invalid address, specification, or memory protect violation.
25	Data Error	3	Signal of operand incorrect in decimal arithmetic and editing, or incorrect field overlap.
26	Exponent Overflow	3	Result characteristic of floating-point operation is greater than 127.
27	Divide Error	3	Rules pertaining to Divide instruction have been violated.
28	Significance Error	3	Result of floating-point add or subtract has zero fraction.
29	Exponent Overflow	3	Result characteristic of floating-point operation is less than zero.
30	Decimal Overflow	3	Result field is too small to contain the result of a decimal operation.

TABLE 6. INTERRUPT CONDITIONS (Cont.)

Priority	Condition	State Initiated	Explanation
31	Fixed-Point Overflow	3	High-order carry or high-order significant bits lost in fixed-point operation.
32	Test Mode	3	Allows program control over processor during program testing.

Input-Output Control

The Model 70/45 Processor communicates with all input-output devices through the RCA Standard Interface.

One multiplexor channel is available on the 70/45. It can be either a standard multiplexor channel (contained in the basic processor) or a communication multiplexor channel.

A total of 128 input-output devices can be attached to the standard multiplexor and a total of 256 can be attached to the communication multiplexor. A set of sub-channel registers services the devices permitting these devices to time-share the channel. The number of sub-channel registers per multiplexor and the number of devices connected to the multiplexor are determined by the capacity of main memory selected by the user.

In addition, up to three selector channels may be included in the system. Each selector channel has two standard interface trunks and is capable of addressing up to 256 devices one at a time. A set of registers is provided in scratch-pad memory for each selector channel making simultaneous operation of all channels possible.

Selector channels and multiplexor channel-connected devices, in any combination, may be operating simultaneously with computing provided the total system transfer rate has not been exceeded.

Registers are provided in scratch-pad memory and non-addressable memory to control input-output operations while other processing is being performed. Input-output instructions, as they are commonly understood, do not exist in the 70/45 Processor. An input-output operation takes place as follows:

A Channel Address Word (CAW) is defined by the user's program and contains the main memory address of the Channel Command Word (the first Channel Command Word in a sequence).

A Channel Command Word (CCW) is defined by the user's program and is stored in main memory (64 bits). It indicates the specific operation to be performed and the data address to be referenced. One or more CCW's may be used

to define a desired sequence of input-output operations. This results in the ability to "chain" input-output operations. Any number of sequences may be defined.

Prior to a program request for input-output initiation, the proper Channel Address Word is stored in a standard area of main memory.

When a request for input-output initiation is issued, the Channel Address Word is automatically stored in the Channel Address Register (CAR) in scratch-pad memory. The Channel Command Word (addressed by the Channel Address Word) is automatically stored in the Channel Command Register (CCR) in scratch-pad memory.

The Channel Command Register now contains the information required to perform the input-output operation. One Channel Command Register and one Channel Address Register are provided for each selector channel and for the multiplexor channel in scratch-pad memory.

Once the CAR and CCR have been loaded, control of the specific input-output operation is given over to hardware, and the processor is free to perform other tasks until the input-output operation terminates. At that time, control is returned to the program via the proper channel termination interrupt.

Instruction Formats and Timing

The 70/45 instruction set is made up of 144 instructions (including the optional floating-point instructions). This instruction repertoire performs decimal, fixed-point and floating-point (optional) commands as well as data handling, decision, and control operations.

There are five basic instruction formats. All instructions must start on halfword boundaries (an even-numbered byte location). Basic formats of the instructions are 2, 4, or 6 bytes long (see table 7).

TABLE 7. INSTRUCTION FORMATS

Format	1st Halfword			2nd Halfword		3rd Halfword	
	Byte 1	Byte 2		Byte 3	Byte 4	Byte 5	Byte 6
SS	8 Op Code	4 L_1	4 L_2	4 B_1	12 D_1	4 B_2	12 D_2
SI	8 Op Code	8 I_2		4 B_1	12 D_1		
RS	8 Op Code	4 R_1	4 R_3	4 B_2	12 D_2		
RX	8 Op Code	4 R_1	4 X_2	4 B_2	12 D_2		
RR	8 Op Code	4 R_1	4 R_2				

Numbers in upper right corners of blocks indicate number of bits used.

Legend:

B_1 — register containing base address of first operand.
B_2 — register containing base address of second operand.
D_1 — address of leftmost byte of first operand.
D_2 — address of leftmost byte of second operand.
I_2 — immediate operand.
L_1 — one less than length of first operand (0–15).
L_2 — one less than length of second operand (0–15).
R_1 — register operand 1.
R_2 — register operand 2.
R_3 — register operand 3.
X_2 — index register.

In addition to the standard instruction set, optional features are available which allow for protection from inadvertent overlay of specified blocks of storage and for direct control of special external devices. Commands pertinent to these optional features are included as a separate category in the instruction list and timing summary tabulated in table 8.

TABLE 8. INSTRUCTION TIMING

Instruction	Format	Timing* (μs)
BRANCHING INSTRUCTIONS Branch and Link	RR	Branch = 3.84, No Branch = 2.88
Branch and Link	RX	6.24
Branch on Condition	RR	Branch = 3.84, No Branch = 2.88
Branch on Condition	RX	Branch = 6.24, No Branch = 5.76
Branch on Count	RR	Branch = 5.76, No Branch = 4.8
Branch on Count	RX	Branch = 8.64, No Branch = 7.68
Branch on Index High	RS	Branch = 11.76, No Branch = 11.04
Branch on Index Low or Equal	RS	Branch = 11.52, No Branch = 11.28
Execute	RX	6.24 + ED
DECIMAL INSTRUCTIONS Add Decimal	SS	$14.8 + 1.56L_1 + 0.66L_2$
Subtract Decimal	SS	$14.8 + 1.56L_1 + 0.66L_2$
Multiply Decimal	SS	$31.7 + 28.5L_1 - 24.3L_2 + 2.7L_2 (L_1 - L_2)$
Divide Decimal	SS	$26.0 + 43.6L_1 - 40.75L_2 + 6.85L_2 (L_1 - L_2)$
Compare Decimal	SS	$15.9 + 1.08L_1 + 0.42L_2$
Move With Offset	SS	$11.04 + 1.92L_1 + 0.96L_2$
Pack	SS	$12.72 + 1.92L_1 + 0.48L_2$
Unpack	SS	$12.0 + 0.96L_1 + 0.96L_2$
Zero And Add	SS	$14.6 + 0.96L_1 + 0.54L_2$
FIXED-POINT INSTRUCTIONS Add Halfword	RX	9.12
Add Logical	RR	5.28
Add Logical	RX	9.6
Add Word	RR	5.28
Add Word	RX	9.6
Subtract Halfword	RX	9.12
Subtract Logical	RR	5.28
Subtract Logical	RX	9.6
Subtract Word	RR	5.28
Subtract Word	RX	9.6

Legend: See page 19.

* All times are average and include staticizing time.

Instruction	Format	Timing* (μs)
FIXED-POINT INSTRUCTIONS Cont. Multiply Halfword	RX	39.84
Multiply Word	RX	72.84
Multiply Word	RX	78.12
Divide	RR	118
Divide	RX	123.28
Compare Halfword	RX	9.12
Compare Word	RR	4.8
Compare Word	RX	9.6
Convert to Binary	RX	97.2
Convert to Decimal	RX	23.82 to 96.96
Load and Test	RR	5.28
Load Complement	RR	5.28
Load Halfword	RX	9.12
Load Multiple	RS	6.0 + 2.88R
Load Negative	RR	6.72
Load Positive	RR	6.72
Load Word	RR	5.28
Load Word	RX	9.26
Shift Left Double	RS	Under 16 = 11.28 + 0.96N
Shift Left Single	RS	Under 16 = 6.72 + 0.48N
Shift Right Double	RS	Under 16 = 9.12 + 0.96N
Shift Right Single	RS	Under 16 = 8.16 + 0.48N
Store Halfword	RX	6.24
Store Multiple	RS	6.0 + 2.88R
Store Word	RX	8.16
FLOATING-POINT INSTRUCTIONS Add Normalized (Long)	RR	(All floating-point instructions are optional.)
Add Normalized (Long)	RX	
Add Normalized (Short)	RR	
Add Normalized (Short)	RX	
Add Unnormalized (Long)	RR	To be supplied at a later date.
Add Unnormalized (Long)	RX	
Add Unnormalized (Short)	RR	
Add Unnormalized (Short)	RX	
Subtract Normalized (Long)	RR	

TABLE 8. INSTRUCTION TIMING (Cont.)

Instruction	Format	Timing* (μs)
FLOATING-POINT INSTRUCTIONS Cont. Subtract Normalized (Long)	RX	To be supplied at a later date.
Subtract Normalized (Short)	RR	
Subtract Normalized (Short)	RX	
Subtract Unnormalized (Long)	RR	
Subtract Unnormalized (Long)	RX	
Subtract Unnormalized (Short)	RR	
Subtract Unnormalized (Short)	RX	
Multiply (Long)	RR	
Multiply (Long)	RX	
Multiply (Short)	RR	
Multiply (Short)	RX	
Divide (Long)	RR	
Divide (Long)	RX	
Divide (Short)	RR	
Divide (Short)	RX	
Compare (Long)	RR	
Compare (Long)	RX	
Compare (Short)	RR	
Compare (Short)	RX	
Halve (Long)	RR	
Halve (Short)	RR	
Load (Long)	RR	
Load (Long)	RX	
Load (Short)	RR	
Load (Short)	RX	
Load and Test (Long)	RR	
Load and Test (Short)	RR	
Load Complement (Long)	RR	
Load Complement (Short)	RR	
Load Negative (Long)	RR	
Load Negative (Short)	RR	

Instruction	Format	Timing* (μs)
FLOATING-POINT INSTRUCTIONS Cont. Load Positive (Long)	RR	To be supplied at a later date.
Load Positive (Short)	RR	
Store (Long)	RX	
Store (Short)	RX	
LOGICAL INSTRUCTIONS AND	RR	5.28
AND	RX	9.6
AND	SI	6.96
AND	SS	9.18 + 2.22L
OR	RR	5.28
OR	RX	9.6
OR	SI	6.96
OR	SS	9.18 + 2.22L
Exclusive OR	RR	5.28
Exclusive OR	RX	9.6
Exclusive OR	SI	6.96
Exclusive OR	SS	9.18 + 2.22L
Compare Logical	RR	4.8
Compare Logical	RX	9.6
Compare Logical	SI	6.0
Compare Logical	SS	9.24 + 1.44B
Edit	SS	$7.04 + 4.08L_1 - 0.72K$
Edit and Mark	SS	$9.44 + 4.08L_1 - 0.72K$
Insert Character	RX	6.72
Load Address	RX	9.12
Move	SI	5.04
Move	SS	9.12 + 1.44L
Move Numerics	SS	10.12 + 2.22L
Move Zones	SS	10.12 + 2.22L
Shift Left Double Logical	RS	Under 16 = 11.28 + 0.96N
Shift Left Single Logical	RS	Under 16 = 6.72 + 0.48N
Shift Right Double Logical	RS	Under 16 = 9.12 + 0.96N
Shift Right Single Logical	RS	Under 16 = 8.16 + 0.48N
Store Character	RX	6.24
Test Under Mask	SI	6.48

Legend: See page 19.

* All times are average and include staticizing time.

TABLE 8. INSTRUCTION TIMING (Cont.)

Instruction	Format	Timing* (μs)
LOGICAL INSTRUCTIONS Cont.		
Translate	SS	12.0 + 4.8L
Translate and Test	SS	12.36 + 4.32L
INPUT-OUTPUT INSTRUCTIONS		
Start Device	SI	26.4 + CRT
Halt Device	SI	6.0 + CRT
Test Channel	SI	2.88
Test Device	SI	6.0 + CRT
PROCESSING STATE CONTROL INSTRUCTIONS		
Set Program Mask	RR	2.4
Supervisor Call	RR	2.4

* All times are average and include staticizing time.

Legend:

B* — total number of bytes processed.
CRT — channel response time.
EAC — end around carry.
ED — external delay.
K — number of control characters in pattern field.
L — total number of bytes specified by the L field.
L_1 — number of bytes in first operand field.
L_2 — number of bytes in second operand field.
M — number of 2-bit shifts.
N — total number of bits to be shifted.
P — number of 4-bit shifts.

Instruction	Format	Timing* (μs)
PRIVILEGED INSTRUCTIONS (STANDARD)		
Diagnose	SI	not applicable
Load Scratch Pad	SS	6.72 + 2.88R
Idle	SI	4.56
Program Control	SI	6.0
Store Scratch Pad	SS	6.72 + 2.88R
PRIVILEGED INSTRUCTIONS (OPTIONAL)		
Insert Storage Key	RR	To be supplied at a later date.
Set Storage Key	RR	
Read Direct	SI	
Write Direct	SI	

Q — number of 1-bit shifts.
R — number of registers specified.
S** — $[(L_1 - L_2) \div 4]$
S(N) — 1 if N = 0; S(N) = 0 if N = 0.
T** — $(L_2 \div 4)$
W_1 — total number of words in first operand field (including partial field).
W_2 — total number of words in second operand field (including partial field).

* This term occurs if an instruction terminates before the L count is reached.

** If the result is a mixed number the next highest integer is used.

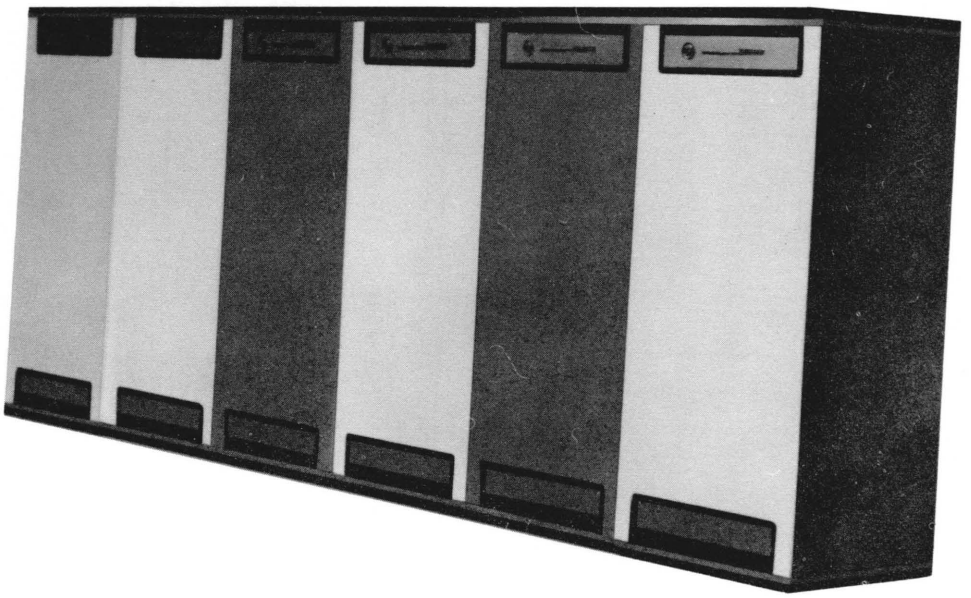

Figure 3. RCA 70/45 System

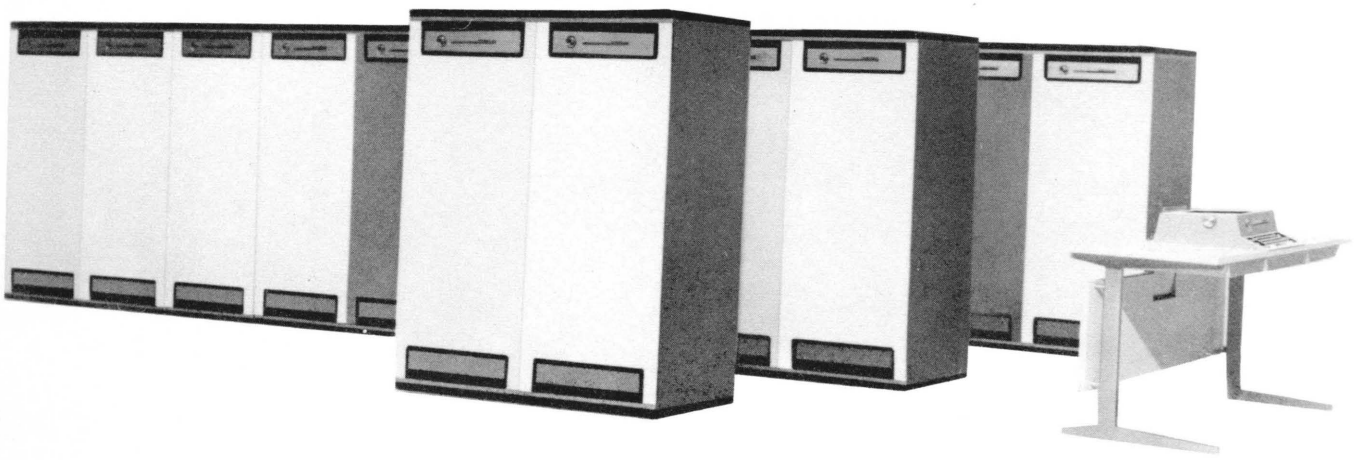

Figure 4. RCA 70/55 System

RCA MODEL 70/55 PROCESSOR

General

The RCA Model 70/55 Processor, fourth and largest of the open-ended Spectra 70 Series, satisfies the most sophisticated data processing or scientific problem-solving requirements. Its order code is implemented by processor logic, resulting in extremely fast data transmission and instruction execution rates.

All instructions, character codes, interrupt facilities, and programming features are functionally the same as corresponding features on the Model 70/45. Programs may be interchanged between the processors provided:

1. Systems features are equivalent.
2. Programs are written independent of strict timing considerations.
3. Programs are restricted to specified functions and do not utilize unspecified characteristics peculiar to the hardware of either processor.

The 70/55 is a word-organized, variable-format processor. Three types of memory are included in the processor: *main memory, scratch-pad memory,* and *non-addressable memory.* In addition, the processor contains *program control* and *input-output control.*

Main Memory

Main memory of the 70/55 is the central storage medium for both the data to be processed and the controlling instructions. Main memory consists of expandable magnetic core storage available in sizes of 65,536, 131,072, 262,144, or 524,288 bytes. Four bytes are accessed and regenerated in one memory cycle of 0.84 microsecond. Although the processor normally operates on fields of four bytes, data may be addressed in units of from one to eight bytes.

Scratch-Pad Memory

The scratch-pad memory, a fast micromagnetic storage device, contains the General-Purpose, Floating-Point, and various other registers to facilitate processor and program control. The 16 General-Purpose registers are used in base-addressing, indexing, and utility operations.

The scratch-pad memory has a capacity of 128 words (512 bytes) and requires 300 nanoseconds to access and regenerate one word (4 bytes). Each word has a discreet address which is not treated as a main memory address.

Non-Addressable Memory

Non-addressable memory provides strict control over the operation of time-shared multiplexor channel input-output devices. It consists of 256 registers, each having a 4-byte capacity. Non-addressable memory is in addition to main memory capacity of the system. The sub-channel registers contained in this memory may not be accessed by programming.

Program Control

The Model 70/55 Processor has four distinct *processor states* to provide control of system and program interrupts. Combined with program systems control, these processor states allow much faster interrupt servicing than could be achieved if control were provided by program systems alone. The four processor states are:

Processing State (P_1) — interprets and executes the program logic defined by the user. This processing state is the problem-oriented state.

Interrupt Response State (P_2) — performs specific program tasks as dictated by the *Interrupt Control State (P_3).*

Interrupt Control State (P_3) — is automatically entered upon recognition of an interrupt other than one caused by a machine check or power failure. This state is responsible for performing a detailed analysis of the cause of interrupt and establishing its priority. Once these functions have been performed, linkage is provided to the proper interrupt processing routine in the *Interrupt Response State (P_2).*

The Machine Condition State (P_4) — is entered whenever a machine check or power failure occurs. This state analyzes the cause of a machine interrupt and establishes its priority. Control is then transferred to the *Interrupt Response State (P_2)* so that an indication of the cause of interrupt may be given to the operator.

Table 9 summarizes the type and number of registers uniquely assigned to each processor state.

TABLE 9. PROCESSOR STATE REGISTERS

Register	Processor State			
	P_1	P_2	P_3	P_4
Program Counter	1	1	6	5
General-Purpose Registers	16	16	6	5
Floating-Point Registers	8	*	*	*
Interrupt Status Register	1	1	1	1
Interrupt Mask Register	1	1	1	1

* Floating-point instructions executed in these states use the floating-point registers of the Processing State (P_1).

Since each processor state has its own General-Purpose registers, Interrupt Status register, and Interrupt Mask register, the need for storing and reloading registers during interrupt processing is virtually eliminated.

Program interrupts occur as a result of errors in data or instruction specifications, input-output operations, external signals, equipment malfunctions, or arithmetic errors. The instruction being executed at the time of interrupt may be completed, suppressed, or terminated depending on the cause of the interrupt.

Any interrupt may be inhibited or permitted in any state through programming. If an interrupt occurs and is permitted, conditions existing in the interrupted state will be automatically stored. Control is then passed to the *Interrupt Control State (P_3)*, or *Machine Condition State (P_4)*, depending upon the cause of the interrupt. The priority of the interrupt is established and an analysis is made to determine the proper linkage to the *Interrupt Response State (P_2)* so that the interrupt may be processed. Once interrupt processing has been completed, control is returned to the state which was last interrupted, and normal processing is resumed.

If several interrupts occur at the same time, the one having the highest priority will be processed. The remaining interrupts will be processed in turn depending upon their priority.

Table 10 summarizes all of the interrupt conditions, their respective priorities, the interrupt state which each initiates, and a brief description of the cause of interrupt.

TABLE 10. INTERRUPT CONDITIONS

Priority	Condition	State Initiated	Explanation
1	Power Failure	4	Power failure in processor or memory.
2	Machine Check	4	Parity error or equipment malfunction.
3	External Signal 1	3	Signal received on one of the six external lines associated with the direct-control feature.
4	External Signal 2	3	
5	External Signal 3	3	
6	External Signal 4	3	
7	External Signal 5	3	
8	External Signal 6	3	
9	Not Specified		
10	Selector 1 Terminate	3	A device on the associated selector or multiplexor channel has terminated.
11	Selector 2 Terminate	3	
12	Selector 3 Terminate	3	
13	Selector 4 Terminate	3	
14	Selector 5 Terminate	3	
15	Selector 6 Terminate	3	
16	Multiplexor Terminate	3	
17	Elapsed Time Clock	3	Elapsed time count has expired.
18	Console Request	3	Manual request for interrupt by the operator.
19	Not Specified		
20	Not Specified		
21	Supervisor Call	3	Result of execution of Supervisor Call instruction to utilize programmed routines.
22	Privileged Operation	3	Privileged instruction attempted in non-privileged mode.
23	Op-Code Trap	3	Op Code attempted which is invalid for this model.
24	Address Error	3	Invalid address, specification, or memory protect violation.
25	Data Error	3	Sign of operand incorrect in decimal arithmetic and editing, or incorrect field overlap.

TABLE 10. INTERRUPT CONDITIONS (Cont.)

Priority	Condition	State Initiated	Explanation
26	Exponent Overflow	3	Result characteristic of floating-point operation is greater than 127.
27	Divide Error	3	Rules pertaining to Divide instruction have been violated.
28	Significance Error	3	Result of floating-point or subtract has zero fraction.
29	Exponent Underflow	3	Result characteristic of floating-point operation is less than zero.
30	Decimal Overflow	3	Result field is too small to contain the result of a decimal operation.
31	Fixed-Point Overflow	3	High-order carry or high-order significant bits lost in fixed-point operation.
32	Test Mode	3	Allows program control over processor during program testing.

Input-Output Control

The Model 70/55 Processor communicates with all input-output devices through the RCA Standard Interface.

One multiplexor channel is available on the 70/55. A total of 128 input-output devices can be attached to the multiplexor channel. A set of subchannel registers services the devices permitting these devices to time-share the channel.

In addition, up to six selector channels may be included in the system providing a high-degree of simultaneity. Each selector channel has four standard interface trunks and is capable of controlling up to 256 devices one at a time. A set of registers is provided in scratch-pad memory for each selector channel, making simultaneous operation of all channels possible.

Selector channels and multiplexor channel-connected devices, in any combination, may be operating simultaneously with computing provided the total system transfer rate has not been exceeded.

Registers are provided in scratch-pad memory and non-addressable memory to control input-output operations while other processing is being performed. Input-output instructions, as they are commonly understood, do not exist in the 70/55 Processor. An input-output operation takes place as follows:

A Channel Address Word (CAW) is defined by the user's program and contains the main memory address of the Channel Command Word (the first Channel Command Word in a sequence).

A Channel Command Word (CCW) is defined by the user's program and is stored in main memory (64 bits). It indicates the specific operation to be performed and the data address to be referenced. One or more CCW's may be used to define a desired sequence of input-output operations. This results in the ability to "chain" input-output operations. Any number of sequences may be defined.

Prior to a program request for input-output initiation, the proper Channel Address Word is stored in a standard area of main memory.

When a request for input-output initiation is issued, the Channel Address Word is automatically stored in the Channel Address Register (CAR) in scratch-pad memory. The Channel Command Word (addressed by the Channel Address Word) is automatically stored in the Channel Command Register (CCR) in the scratch-pad memory.

The Channel Command Register now contains the information required to perform the input-output operation. One Channel Command Register and one Channel Address Register are provided for each selector channel and for the multiplexor channel.

Once the CAR and CCR have been loaded, control of the specific input-output operation is given over to hardware, and the processor is free to perform other tasks until the input-output operation terminates. At that time, control is returned to the program via the proper channel termination interrupt.

Instruction Formats and Timing

The 70/55 instruction set is made up of 144 instructions providing virtually unlimited data processing and scientific problem-solving capabilities. These standard instructions include comprehensive floating-point, decimal, and fixed-point commands, as well as data handling, decision, and control operations.

There are five basic instruction formats. All instructions must start on halfword boundaries (an even-numbered byte location). Basic formats of the instructions are 2, 4, or 6 bytes long.

Table 11 illustrates the basic formats and their construction.

TABLE 11. INSTRUCTION FORMATS

Format	1st Halfword			2nd Halfword		3rd Halfword	
	Byte 1	Byte 2		Byte 3	Byte 4	Byte 5	Byte 6
SS	8 Op Code	4 L_1	4 L_2	4 B_1	12 D_1	4 B_2	12 D_2
SI	8 Op Code	8 I_2		4 B_1	12 D_1		
RS	8 Op Code	4 R_1	4 R_3	4 B_2	12 D_2		
RX	8 Op Code	4 R_1	4 X_2	4 B_2	12 D_2		
RR	8 Op Code	4 R_1	4 R_2				

Numbers in upper right corners of blocks indicate number of bits used.

Legend:

B_1 — register containing base address of first operand.
B_2 — register containing base address of second operand.
D_1 — address of leftmost byte of first operand.
D_2 — address of leftmost byte of second operand.
I_2 — immediate operand.
L_1 — one less than length of first operand.
L_2 — one less than length of second operand.
R_1 — register operand 1.
R_2 — register operand 2.
R_3 — register operand 3.
X_2 — index register.

In addition to the standard instruction set, optional features are available which allow for protection from inadvertent overlay of specified blocks of storage and for direct control of special external devices. Commands pertinent to these optional features are included as a separate category in the instruction list and timing summary tabulated in table 12.

TABLE 12. INSTRUCTION TIMING

Instruction	Format	Timing* (μs)
BRANCHING INSTRUCTIONS Branch and Link	RR	Branch = 2.52, No Branch = 2.04
Branch and Link	RX	2.70
Branch on Condition	RR	Branch = 1.98, No Branch = 1.62
Branch on Condition	RX	Branch = 2.10, No Branch = 1.74
Branch on Count	RR	Branch = 2.40, No Branch = 1.92
Branch on Count	RX	Branch = 2.58, No Branch = 2.22

Legend: See page 26.

* All times are average and include staticizing time.

TABLE 12. INSTRUCTION TIMING (Cont.)

Instruction	Format	Timing* (μs)
BRANCHING INSTRUCTIONS Cont. Branch on Index High	RS	Branch = 3.72, No Branch = 3.36
Branch on Index Low or Equal	RS	Branch = 3.72, No Branch = 3.36
Execute	RX	3.90 + ED
DECIMAL INSTRUCTIONS Add Decimal	SS	$5.40 + 0.96W_2 + 1.92W_1 + 0.48L_1$
Subtract Decimal	SS	$5.40 + 0.96W_2 + 1.92W_1 + 0.48L_1$
Multiply Decimal	SS	$8.88 + 1.20W_1 + 1.08W_2 + 5.16L_2 + 8.88S + 3.12SL_2 + 0.72 (L_1 - L_2)$
Divide Decimal	SS	$11.28 + 1.20W_1 + 0.36L_1 + 0.72S + 0.60W_2 + 0.72L_2 + 4.2T (L_1 - L_2) + 1.08 (L_1 - L_2) + 0.96S (L_1 - L_2)$
Compare Decimal	SS	$5.40 + 0.96W_2 + 1.08W_1 + 0.48L$
Move with Offset	SS	$4.92 + 1.80W_1 + 0.60W_2 + 0.72 (L_1 + L_2)$
Pack	SS	$4.56 + 1.80W_1 + 0.60W_2 + 0.72L_1 + 0.36L_2$
Unpack	SS	$4.80 + 1.80W_1 + 0.60W_2 + 0.36L_1 + 0.72L_2$
Zero and Add	SS	$6.96 + 0.96W_1 + 0.96W_2 + 0.48L_1$
FIXED-POINT INSTRUCTIONS Add Halfword	RX	3.98
Add Logical	RR	1.92
Add Logical	RX	2.58
Add	RR	1.92
Add	RX	2.58
Subtract Halfword	RX	2.58
Subtract Logical	RR	1.92
Subtract Logical	RX	2.58
Subtract	RR	1.92
Subtract	RX	2.58
Multiply Halfword	RX	12.28
Multiply	RR	12.12
Multiply	RX	12.78

TABLE 12. INSTRUCTION TIMING (Cont.)

Instruction	Format	Timing* (μs)
FIXED-POINT INSTRUCTIONS (Cont.) Divide	RR	19.20
Divide	RX	19.86
Compare Halfword	RX	2.58
Compare	RR	1.92
Compare	RX	2.58
Convert to Binary	RX	5.34 to 26.34
Convert to Decimal	RX	5.70 to 23.82
Load and Test	RR	1.98
Load Complement	RR	1.92
Load Halfword	RX	2.58
Load Multiple	RS	2.10 + 0.84R
Load Negative	RR	1.92
Load Positive	RR	1.92
Load	RR	1.98
Load	RX	2.46
Shift Left Double	RS	2.10 + 0.72 (P + Q) + 0.72S(N)
Shift Left Single	RS	2.10 + 0.36 (P + Q) + 0.36S(N)
Shift Right Double	RS	2.10 + 0.72 (P + Q + M) + 0.72S(N)
Shift Right Single	RS	2.10 + 0.36 (P + Q + M) + 0.36S(N)
Store Halfword	RX	4.38
Store Multiple	RS	2.10 + 1.20R
Store	RX	2.70
FLOATING POINT INSTRUCTIONS Add Normalized (Long)	RR	9.12
Add Normalized (Long)	RX	10.50
Add Normalized (Short)	RR	6.48
Add Normalized (Short)	RX	7.62
Add Unnormalized (Long)	RR	8.40
Add Unnormalized (Long)	RX	9.78
Add Unnormalized (Short)	RR	6.12
Add Unnormalized (Short)	RX	7.26

Legend: See page 26.

* All times are average and include staticizing time.

TABLE 12. INSTRUCTION TIMING (Cont.)

Instruction	Format	Timing* (μs)
FLOATING-POINT INSTRUCTIONS (Cont.) Subtract Normalized (Long)	RR	9.12
Subtract Normalized (Long)	RX	10.50
Subtract Normalized (Short)	RR	6.48
Subtract Normalized (Short)	RX	7.62
Subtract Unnormalized (Long)	RR	8.40
Subtract Unnormalized (Long)	RX	9.78
Subtract Unnormalized (Short)	RR	6.12
Subtract Unnormalized (Short)	RX	7.26
Multiply (Long)	RR	43.20
Multiply (Long)	RX	44.58
Multiply (Short)	RR	17.28
Multiply (Short)	RX	18.42
Divide (Long)	RR	73.92
Divide (Long)	RX	75.30
Divide (Short)	RR	21.72
Divide (Short)	RX	22.86
Compare (Long)	RR	6.00
Compare (Long)	RX	7.38
Compare (Short)	RR	5.52
Compare (Short)	RX	6.66
Halve (Long)	RR	2.40
Halve (Short)	RR	1.80
Load (Long)	RR	2.58
Load (Long)	RX	4.02
Load (Short)	RR	1.98
Load (Short)	RX	2.46
Load and Test (Long)	RR	2.58
Load and Test (Short)	RR	1.98
Load Complement (Long)	RR	2.58
Load Complement (Short)	RR	1.98
Load Negative (Long)	RR	2.56
Load Positive (Short)	RR	1.98
Store (Long)	RX	4.50
Store (Short)	RX	3.30

TABLE 12. INSTRUCTION TIMING (Cont.)

Instruction	Format	Timing* (μs)
LOGICAL INSTRUCTIONS AND	RR	1.92
AND	RX	2.58
AND	SI	3.18
AND	SS	3.84 + 1.80W_1 + 0.96W_2 + 0.48L
OR	RR	1.92
OR	RX	2.58
OR	SI	3.18
OR	SS	3.84 + 1.80W_1 + 0.96W_2 + 0.48L
Exclusive OR	RR	1.92
Exclusive OR	RX	2.58
Exclusive OR	SI	3.18
Exclusive OR	SS	3.84 + 1.80W_1 + 0.96W_2 + 0.48L
Compare Logical	RR	1.92
Compare Logical	RX	2.58
Compare Logical	SI	2.46
Compare Logical	SS	3.24 + 0.96W_1 + 0.96W_2 + 0.48B
Edit	SS	3.72 + 1.80W_1 + 0.60W_2 + 0.36L_1 + 0.96L_2 + 0.36K
Edit and Mark	SS	6.00 + 1.80W_1 + 0.60W_2 + 0.36L_1 + 0.96L_2 + 0.36K
Insert Character	RX	2.70
Load Address	RX	2.10
Move	SI	3.18
Move	SS	5.76 + 0.84W_1 + 0.96W_2 + 0.36L
Move Numeric	SS	3.84 + 1.80W_1 + 0.96W_2 + 0.36L
Move Zones	SS	3.84 + 1.80W_1 + 0.96W_2 + 0.36L
Shift Left Double Logical	RS	2.10 + 0.72 (P + Q) + 0.72S(N)
Shift Left Single Logical	RS	2.10 + 0.36 (P + Q) + 0.36S(N)
Shift Right Double Logical	RS	2.10 + 0.72 (P + Q + M) + 0.72S(N)
Shift Right Single Logical	RS	2.10 + 0.36 (P + Q + M) + 0.36S(N)
Store Character	RX	3.18

* All times are average and include staticizing time.

TABLE 12. INSTRUCTION TIMING (Cont.)

Instruction	Format	Timing* (μs)
LOGICAL INSTRUCTIONS (Cont.) Test Under Mask	SI	2.82
Translate	SS	3.24 + 1.20W_1 + 2.88L
Translate and Test	SS	4.56 + 1.20W_1 + 1.80B
INPUT-OUTPUT INSTRUCTIONS Start Device	SI	14.46 + CRT
Halt Device	SI	7.14 + CRT
Check Channel	SI	2.70
Test Device	SI	7.14 + CRT
PROCESSING STATE CONTROL INSTRUCTIONS Set Program Mask	RR	1.80
Supervisor Call	RR	3.36
PRIVILEGED INSTRUCTIONS (STANDARD) Diagnose	SI	Not Applicable
Idle	SI	3.66
Load Scratch Pad	SS	3.60 + 0.96R
Program Control	SI	3.66
Store Scratch Pad	SS	3.60 + 1.20R
PRIVILEGED INSTRUCTIONS (OPTIONAL) Insert Storage Key	RR	To be supplied at a later date.
Set Storage Key	RR	
Read Direct	SI	
Write Direct	SI	

Legend:

B* — total number of bytes processed.
CRT — channel response time.
EAC — end around carry.
ED — external delay.
D — number of control characters in pattern field.
L — total number of bytes specified by the L field.
L_1 — number of bytes in first operand field.
L_2 — number of bytes in second operand field.
M — number of 2-bit shifts.
N — total number of bits to be shifted.
P — number of 4-bit shifts.
Q — number of 1-bit shifts.
R — number of registers specified.
S** — $[(L_1 - L_2) \div 4]$
S(N) — 1 if N = 0; S(N) = 0 if N = 0.
T** — $(L_2 \div 4)$
W_1 — total number of words in first operand field (including partial field).
W_2 — total number of words in second operand field (including partial field).

* This term occurs if an instruction terminates before the L count is reached.
** If the result is a mixed number the next highest integer is used.

INPUT-OUTPUT DEVICES

The RCA Spectra 70 Series includes a wide-range of input-output devices to assist the user in solving all of his data-processing requirements.

Model 70/97 Console and Typewriter

The Model 70/97 Console and Typewriter, available with the RCA Model 70/45 and 70/55 Processors, is a free-standing, self-contained unit which provides sufficient control to enable system operation in conjunction with the operating system programs. The operator has complete control of the system and communication with the system via a set of control switches and a console typewriter.

The set of control switches on the console allows for loading programs or data into memory, starting programs, displaying current processing state, and interrupting processor operation.

A console typewriter mounted on the console enables the operator to communicate with the operating system programs and vice versa.

Control electronics permits communication with the processor via the RCA Standard Interface. The control electronics for the console typewriter generates a parity bit for each character sent to the processor and performs a bit-by-bit echo check on the characters sent to the typewriter.

The following optional feature is available with the console typewriter:

Pin Feed Platen — provides for non-slip continuous-form feeding on the typewriter.

Model 70/214 Interrogating Typewriter

The Model 70/214 Interrogating Typewriter is a send-receive device capable of operating at a speed of up to 10 characters per second.

Bi-directional communication is possible between the typewriter and a Model 70/15 Processor. Up to 72 characters may be printed on a line and one carbon copy can be prepared.

Accuracy control is provided by generating a parity bit for each character sent to the processor and by performing a bit-by-bit echo check on the characters sent to the printer.

The interrogating typewriter provides the facility to manually interrupt the processor. This feature allows for manual insertion of parameters or interrogation information.

The following optional feature is available with this interrogating typewriter:

Pin Feed Platen — provides for non-slip continuous-form feeding.

Model 70/216 Interrogating Typewriter

The Model 70/216 Interrogating Typewriter is a send-receive device capable of operating at a speed of up to 10 characters per second.

Bi-directional communication is possible between the typewriter and a Model 70/25 Processor. Up to 72 characters may be printed on a line and one carbon copy can be prepared.

Accuracy control is provided by generating a parity bit for each character sent to the processor and performing a bit-by-bit echo check on the characters sent to the printer.

The interrogating typewriter provides the facility to manually interrupt the processor. This feature allows for manual insertion of parameters or interrogation information.

The following optional feature is available with the interrogating typewriter.

Pin Feed Platen — provides for non-slip continuous form feeding.

Model 70/221 Paper Tape Reader/Punch

The Model 70/221 Paper Tape Reader/Punch consists of a 200 character-per-second reader and a 100 character-per-second punch. Manual controls are provided for selecting the width of the paper tape to be processed. Both the reader and the punch are capable of handling 5, 6, 7 or 8-channel paper tape. Either gap or gapless tape may be processed.

Parity checking is performed by the reader and the punch to control the accuracy of data. The paper tape reader has a switch which can be set to select odd, even, or no-parity checking. A character on paper tape that has bad parity will be replaced in high-speed memory with the systems error byte.

The reader/punch handles 11/16-inch, 7/8-inch or 1-inch paper tape and provides spooling capability for reels up to 1,000 feet in length. Paper tape strips may also be read by this device.

The following optional features are available with the paper tape reader/punch:

EBCDIC Mode — provides the ability to punch and read a modified EBCDIC code with 8-channel tape. The EBCDIC code from the processor is modified on punching so that even parity is placed on the paper tape. Facility to translate the paper-tape code is contained in the reader.

6-level Advanced Sprocket — provides the ability to read and punch 6-level advanced sprocket-hole tape.

Figure 5. Model 70/97 Console and Typewriter

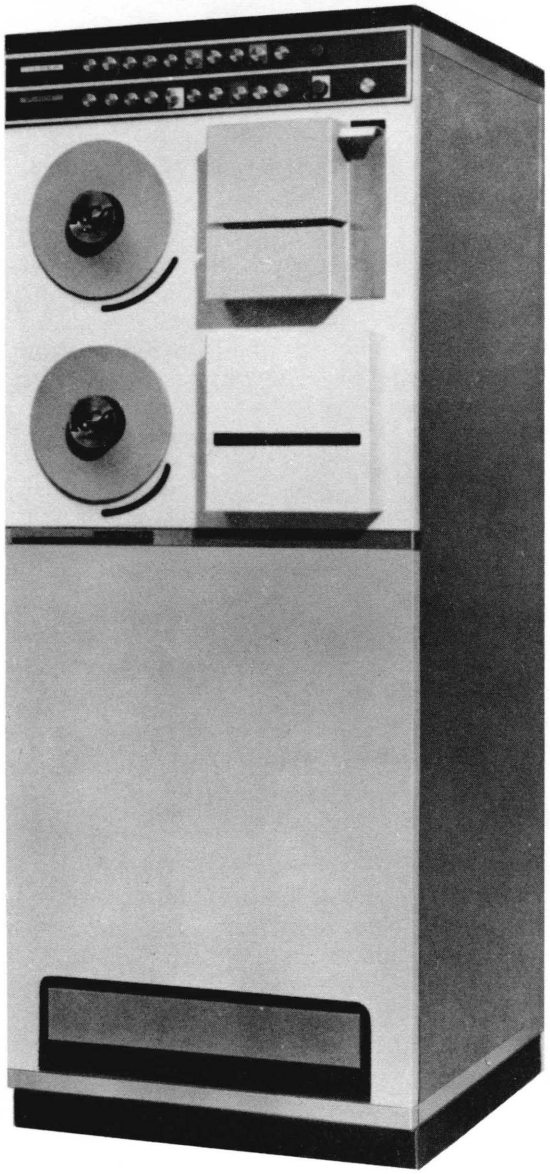

Figure 6. Model 70/221 Paper Tape Reader/Punch

Model 70/234 Card Punch

The Model 70/234 Card Punch is an 80-column row-oriented card punch. The unit is capable of feeding, punching, and checking cards at a rate up to 100 cards per minute.

The device contains a 960-bit storage buffer which provides temporary storage for punched data. This storage buffer allows card-punching operations to be performed independently of the processor.

Transmission of data between the buffer and the punch is checked for parity to ensure data integrity. A read-after-punch feature is provided to give a hole-count accuracy check on the punched data. Card-operated switches indicate hopper-empty or stacker-full conditions to the operator. Both the input hopper and output stacker have a capacity up to 800 cards and can be loaded while the device is operating.

A translation process is performed by the card punch to translate the Extended Binary-Coded-Decimal Interchange Code (EBCDIC) character configurations to the Extended Hollerith card code.

The following optional features are available with this card punch:

Column Binary Feature — provides the ability to punch all possible punch-configurations with a single card.

Scored Card Feature — provides the ability to accept cards which have been scored for subsequent separation into two or more cards.

Model 70/236 Card Punch

The Model 70/236 Card Punch is an 80-column row-oriented card punch capable of feeding, punching, and checking 80-column cards at a rate of up to 300 cards per minute. An 80-byte storage buffer which is loaded asynchronously at rates up to 120 kilobytes per second permits card punching to be performed independently of the processor.

Data is constantly monitored during transmission from the processor to the buffer and from the buffer to the punch. A read-after-punch-feature is provided to give a hole-count accuracy check on punched data.

A translation process is performed by the card punch to translate the Extended Binary-Coded-Decimal Interchange Code (EBCDIC) character configurations to the Extended Hollerith card code. All 256 possible code configurations can be punched.

The input hopper capacity is 1,000 cards and the two selectable output stackers have a capacity of 850 cards each. The device may be loaded while it is operating.

The following optional features are available with this card punch:

Reader Punch Feature — permits punch-read-feed for a single card.

Column Binary Feature — provides the ability to read and/or punch all possible punch configurations from a single card.

Scored Card Feature — provides the ability to accept cards which have been scored for subsequent separation into two or more cards.

Model 70/237 Card Reader

The Model 70/237 Card Reader reads standard 80-column punched cards at a rate of up to 1,435 cards per minute. Cards are read column-by-column and maximum speeds can be obtained on a demand-basis.

The hopper has a capacity of 2,000 cards. Cards may be routed under program control to one of two selectable output stackers. Each stacker holds up to 2,000 cards. Loading and unloading of the reader is permitted while the device is running.

This reader is a self-powered device containing all necessary reading, timing, control, and accuracy-checking circuitry. The reader translates the Extended Hollerith card code to the Extended Binary-Coded-Decimal Interchange Code (EBCDIC). Any punched hole combination for which there exists no corresponding machine code byte causes the systems error byte to be generated and transferred to high-speed memory.

The following optional features are available with this card reader:

Optical Mark Read — provides the capability of reading pencil-mark data from an 80-column card. With this option the reader has the following possible modes of operation:

a. Read punched-hole data only (CR).

b. Read pencil-mark data only (MR).

c. Read punched-hole and pencil-mark data (CR and MR).

The mode of operation is selected at the operator's console and any one of the above three modes is possible in any one document pass.

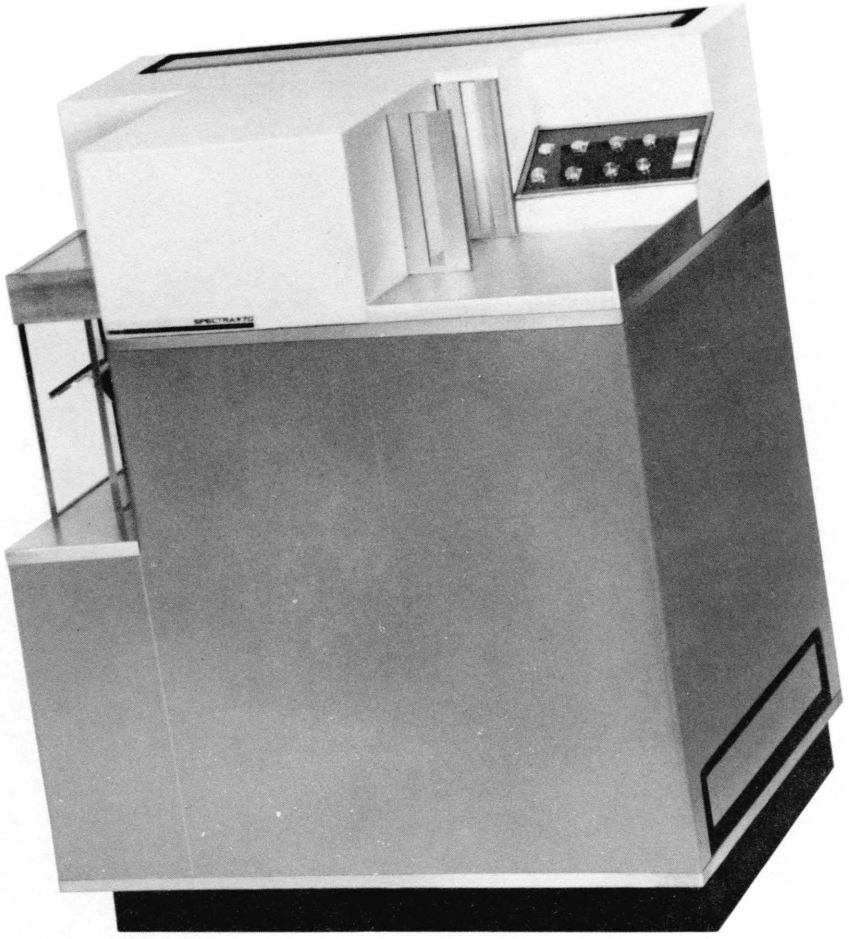

Figure 7. Model 70/236 Card Punch

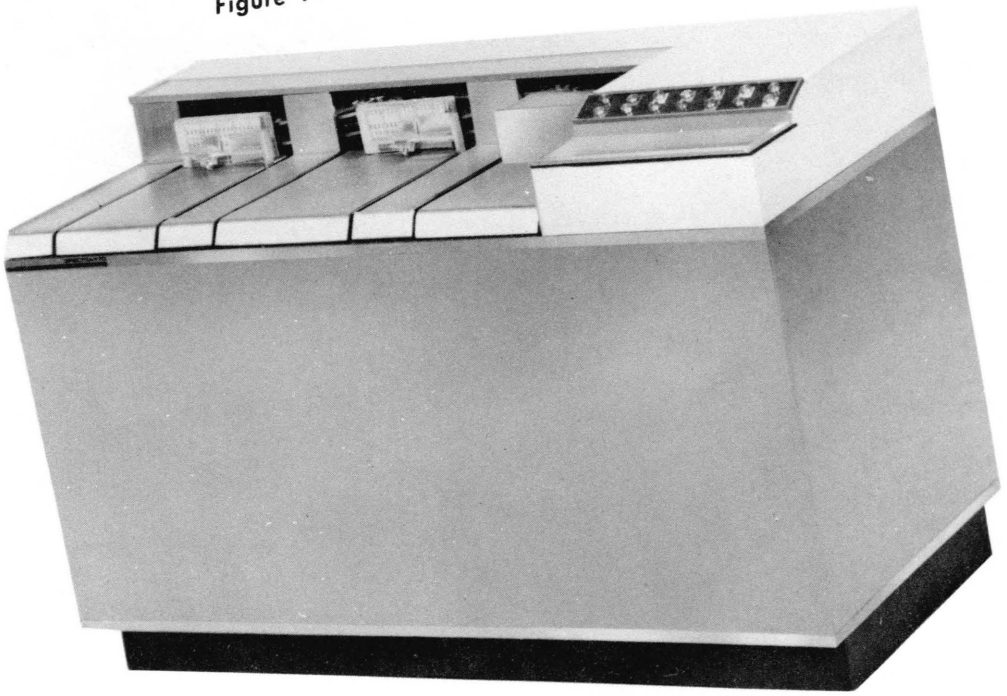

Figure 8. Model 70/237 Card Reader

51-Column Stub Read — permits the feeding, reading, and processing of either 80 or 51-column cards depending upon the setting of a manual switch on the card reader and manual adjustment to the hopper and stackers.

Card-Read Column Binary — permits punched-hole information to be transferred to high-speed memory without translation. Each card column represents two-memory byte locations.

Model 70/242 Printer, Medium Speed

The Model 70/242 Printer, Medium Speed, is a fully buffered, drum-type printer which prepares printed output documents at rates up to 600 lines per minute. A single data line contains 132-print positions. A selected 64-character subset of the Extended Binary-Coded-Decimal Interchange Code (EBCDIC) may be printed.

A control electronics unit in the printer provides the means for communicating between the printer, print buffer, and the RCA Standard Interface. On command from the processor, a data line (any number of characters up to 132) is transferred to the buffer. When the buffer is loaded, printing is performed independently of the processor.

Vertical paper movement can be accomplished by loop control, program control, or a combination of both. Single line paper-advance time is less than 12 milliseconds and vertical tab rate is 27 inches per second.

The printer is capable of handling edge-perforated, fan-fold paper and card stock. Form widths may be 4 inches to 18¾ inches including margins.

Data is checked during transmission from the processor to the buffer and from the buffer to the printer. An indication is sent to the processor when a low-paper condition is detected or when a character which is not included in the 64-character subset is detected in the buffer.

Model 70/243 Printer, Hi-Speed

The Model 70/243 Printer, Hi-Speed, is a fully buffered, drum-type printer which prepares printed documents at rates up to 1,250 lines per minute. A single line contains 132-print positions. A selected 64-character subset of the Extended Binary-Coded-Decimal-Interchange Code (EBCDIC) may be printed.

A control electronics unit in the printer provides the means for communicating between the printer, print buffer, and the RCA Standard Interface. On command from the processor, a data line (any number of characters up to 132) is transferred to the buffer. When the buffer is loaded, printing is performed independently of the processor.

Vertical paper movement can be accomplished by loop control, program control, or a combination of both. Single-line, paper-advance time is less than 12 milliseconds and vertical-tab rate is 27 inches per second.

The printer is capable of handling edge-perforated, fan-fold paper and card stock. Form widths may be 4 inches to 18¾ inches including margins.

Data is checked during transmission from the processor to the buffer and from the buffer to the printer. An indication is sent to the processor when a low-paper condition is detected or when a character which is not included in the 64-character subset is detected in the buffer.

Model 70/249 Bill Feed Printer

The Model 70/249 Bill Feed Printer prints on continuous forms at rates up to 600 lines per minute; or on card documents at rates up to 800 lines per minute (400 cards for each of two feed channels).

A movable print unit allows the operator to easily change from continuous-forms feeding to card-document feeding. Conveniently located controls, hoppers, and stackers, all accessible from the front, permit easy operation.

The bill feed printer can process cards ranging from a single 51-column card to an 80-column card with an 80-column stub. It can also process any two cards that range in size from 51 to 80 columns each at one time.

The hopper and stackers can accommodate 1,200 standard tab cards. Twenty-five lines of data, either from processor storage or the card itself, can be printed on a card. A standard 48-character set consisting of 26 alphabetic, 10 numeric, and 12 special characters may be printed.

The following optional features are available with this printer.

Interchangeable Print Chains — permits changing of printable graphics.

Read Compare — of up to 30 columns from the 160 (2 cards) columns is available as an optional feature. Selection of the desired 30 columns is accomplished by means of an operator-wired plugboard.

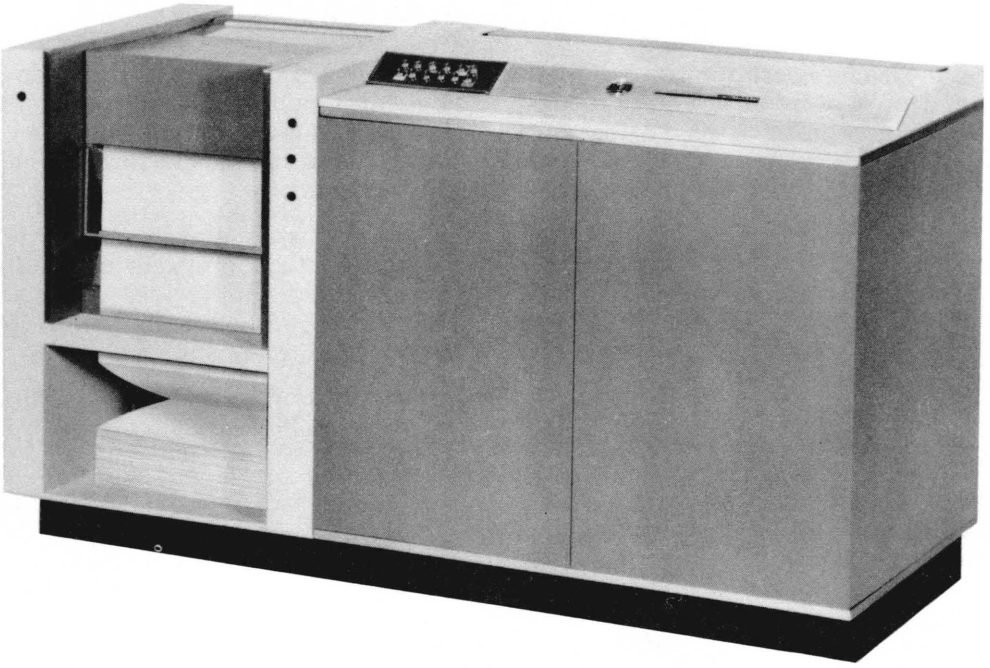

Figure 9. Model 70/243 Printer, Hi-Speed

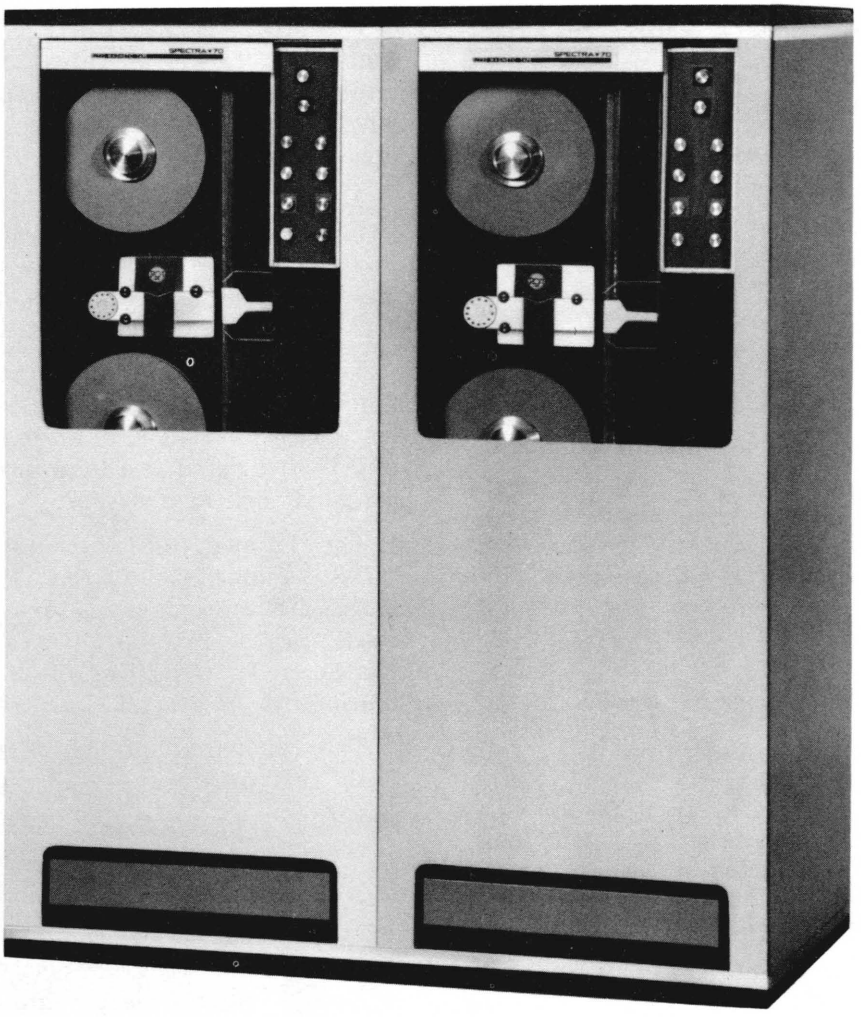

Figure 10. Model 70/432 Magnetic Tape Unit

Model 70/251 Videoscan Document Reader

The Model 70/251 Videoscan Document Reader is a high-speed, on-line optical-character reader capable of reading (on-demand) a single line of printed characters from a document at a rate of up to 1,300 documents per minute. If synchronous feeding is specified by program, a rate of up to 1,800 documents per minute can be achieved. The printed characters may be produced by a standard electric typewriter or a drum-type printer equipped with the RCA N-2 type font. Offset or letterpress printed characters in this font may also be read. The following RCA N-2 characters can be read and will be translated to their equivalent Extended Binary-Coded-Decimal Interchange Code (EBCDIC):

	RCA (N-2 Chars.)
Zero	0
One	1
Two	2
Three	3
Four	4
Five	5
Six	6
Seven	7
Eight	8
Nine	9
Period	.
Dash	-
Dollars	$
Asterisk	*
Blank	

In addition, a long vertical mark (LVM) which may be preprinted or made with a pencil stroke will be recognized and translated to an "at the rate of" symbol @.

The following document sizes can be handled by the transport:

Width — 2.5 inches — 8.5 inches
Height — 2.5 inches — 4.0 inches
Thickness — 0.003 inch — 0.01 inch

Characters are placed on the document 10 to the inch with a maximum of 80 characters on a single document.

The input hopper has a capacity of approximately 17.5 inches. Two output stackers are provided (accept and reject) each with a capacity of 15¾ inches. Both the input hopper and the two output stackers may be loaded or unloaded while the reader is operating.

An off-line select feature permits properly marked documents to be directed to a specific output stacker.

All characters scanned are converted to video signals which are processed and transferred to the Spectra 70 Processors through the RCA Standard Interface. If an unreadable character is detected, a substitute character (systems error byte) will be sent to high-speed memory. Other accuracy controls are provided for detecting double-fed documents and a jam condition.

The following special features are available with the Videoscan Document Reader:

Mark Reading — permits vertical or slant marks made with an ordinary lead pencil to be read. Mark-read grid options of 10, 12, or 12-row binary are available.

Card Reading — permits reading of standard 80-column punched cards at a rate of up to 500 cards per minute. The reader translates the Extended Hollerith card code to the Extended Binary-Coded-Decimal Interchange Code (EBCDIC). A binary card-read option is also available.

Model 70/432 Magnetic Tape Unit

The Model 70/432 Magnetic Tape Unit consists of two tape stations contained in one rack. The Model 70/432-1 permits single tape station operation while the Model 70/432-2 permits simultaneous operation (read-read, read-write, and write-write) of both tape stations. This tape unit can be physically connected to other 70/432 or 70/442 Magnetic Tape Units to make a grouping of four tape stations. Alternatively, it can be connected to one or two Model 70/445 Tape Stations to make a grouping of three or four tape stations.

Each Model 70/432 Tape Station is capable of reading and writing ½ inch, 9-channel, magnetic polyester tape at the rate of 30,000 bytes or 60,000 decimal-digits per second. Reading is possible in the forward or reverse direction. Writing and erasing may be accomplished in the forward direction only. The Model 70/432 Magnetic Tape Unit is completely compatible with all IBM* 2400 Series Tape Units.

70/432 Characteristics

Tape Speed:
37.5 inches per second

Tape Rewind Speed:
100 inches per second

Recording Density:
800 bits per inch

Nominal Gap Size:
0.6 inch

Reel Dimensions:
10.5 inches

Number of Feet per Reel:
2,400

Accuracy controls provided include: remote lockout, local lockout, write lockout, read-after-write, lateral-parity check, longitudinal-parity check, and cyclical-redundancy check.

The following optional feature is available with this tape unit:

7-Channel Tape Feature — permits reading and writing 7-channel tape in IBM binary or BCD mode. Recording density can be specified at 200, 556, or 800 bits per inch providing a 7,500, 20,800 or 30,000 character-per-second transfer rate respectively. Odd or even parity may be specified.

Model 70/442 Magnetic Tape Unit

The Model 70/442 Magnetic Tape Unit consists of two tape stations contained in one rack. The Model 70/442-1 permits single tape station operation while the Model 70/442-2 permits simultaneous operation (read-read, read-write, write-write) of both tape stations. This tape unit can be physically connected to other Model 70/442 or 70/432 Magnetic Tape Units to make a grouping of four tape stations. Alternatively, it can be connected to one or two Model 70/445 Tape Stations to make a grouping of three or four tape stations.

Each Model 70/442 Tape Station is capable of reading and writing ½ inch, 9-channel, magnetic polyester tape at the rate of 60,000 bytes or 120,000 decimal-digits per second. Reading is possible in the forward or reverse direction. Writing and erasing may be accomplished in the forward direction only. The Model 70/442 Magnetic Tape Unit is completely compatible with all IBM 2400 Series Tape Units.

70/442 Characteristics

Tape Speed:
75 inches per second

Tape Rewind Speed:
150 inches per second

Recording Density:
800 bits per inch

Nominal Gap Size:
0.6 inch

Reel Dimensions:
10.5 inches

Number of Feet per Reel:
2,400

Accuracy controls provided include: remote lockout, local lockout, write lockout, read-after-write, lateral-parity check, longitudinal-parity check, and cyclical-redundancy check.

The following optional feature is available with this tape unit:

7-Channel Tape Feature — permits reading and writing 7-channel tape in IBM binary or BCD mode. Recording density can be specified at 200, 556, or 800 bits per inch providing a 15,000, 41,700, or 60,000 character-per-second transfer rate respectively. Odd or even parity may be specified.

Model 70/445 Magnetic Tape Station

The Model 70/445-1 Magnetic Tape Station is capable of reading and writing ½ inch, 9-channel, magnetic polyester tape at the rate of 120,000 bytes or 240,000 decimal digits per second. The Model 70/445-2 Magnetic Tape Station is identical to the 70/445-1 with the exception that it is included in a simultaneous tape grouping (read-read, read-write, write-write). This tape station can be physically connected to another Model 70/445 to make a grouping of up to four tape stations. Alternatively, it can be connected to a Model 70/432 or 70/442 Magnetic Tape Unit to make a group of three or four tape stations.

Reading and writing are possible in the forward or reverse direction. Writing and erasing may be accomplished in the forward direction only. The Model 70/445 Magnetic Tape Station is completely compatible with all IBM 2400 Series Tape Units.

70/445 Characteristics

Tape Speed:
150 inches per second

Tape Rewind Speed:
300 inches per second

Recording Density:
800 bits per inch

Nominal Gap Size:
0.6 inch (reading), 0.65 inch (writing)

Reel Dimensions:
10.5 inches

Number of Feet per Reel:
2,400

Accuracy controls provided include: remote lockout, local lockout, write lockout, read-after-write, lateral-parity check, longitudinal-parity check, and cyclical-redundancy check.

The following optional feature is available with this tape station:

7-Channel Tape Feature — permits reading and writing 7-channel tape in IBM binary or BCD mode. Recording density can be specified at 200, 556, or 800 bits per inch providing a 30,000, 83,400 or 120,000 character-per-second transfer rate respectively. Odd or even parity may be specified.

Model 70/472-108, -116
Tape Controller (Single Channel)

The Model 70/472-108, -116 Tape Controller (single-channel) controls the operation of up to 8 (Model 70/472-108) or 16 (Model 70/472-116) Tape Stations. Any combination of Model 70/445 Tape Stations, 70/432, or 70/442 Tape Units can be operated by this controller.

All accuracy checks and controls associated with tape station operation are indicated to the processor by the tape controller. These accuracy controls include: read-after-write, longitudinal-parity check, lateral-parity check, cyclical-redundancy check (9-level) and re-read with error correction (9-level).

The following optional features are available with these tape controllers:

7-Channel Tape Feature — permits operation of both 7 and 9-channel tape stations or tape units in any combination.

Pack-Unpack Feature — converts four 6-bit characters on tape to three 8-bit characters in high-speed memory when reading and vice versa when writing.

Model 70/472-208, -216
Tape Controller (Dual Channel)

The Model 70/472-208, -216 Tape Controller (dual-channel) controls the operation of up to 8 (Model 70/472-208) or 16 (Model 70/472-216) Tape Stations. Read-read, read-write, or write-write simultaneity is possible on any two tape stations serviced by this controller. Model 70/445-2 Tape Stations, 70/432-2, or 70/442-2 Tape Units in any combination can be utilized.

All accuracy check and controls associated with tape station operation are indicated to the processor by the tape controller. These accuracy controls include: read-after-write, longitudinal-parity check, lateral-parity check, cyclical-redundancy check (9-level) and re-read with error correction (9-level).

The following optional features are available with these tape controllers:

7-Channel Tape Feature — permits operation of both 7 and 9-channel tape stations or tape units in any combination.

Pack-Unpack Feature — converts four 6-bit characters on tape to three 8-bit characters in high-speed memory when reading and vice versa when writing.

Model 70/551 Random Access Controller

The Model 70/551 Random Access Controller operates all random-access devices in the Spectra 70 Series. The following devices are presently available to be operated by the controller.

Model 70/564 Disc Storage Unit
Model 70/565 Drum Memory Unit
Model 70/568 Mass Storage Unit

Up to 8 devices may be operated by one controller. Intermixing of different devices on one controller is permitted but from a programming viewpoint all devices look the same. The controller has a standard set of commands which it translates into specific commands for each of the different devices. The seeking or selecting of specific locations within a file is performed independently of the processor. Facilities for searching or locating a particular data record are also provided by the controller.

The open-ended design of the Model 70/551 Controller allows for inclusion of any new devices should the need arise.

The controller maintains a comprehensive accuracy check on data being read and written. The

data integrity is assured by the addition of two-check characters to the trailing end of each recorded block.

The following optional special features are available with this controller:

Off-Line Scan — provides an automatic rapid search of the random-access file for a specific identifier or condition.

Record Overflow — allows a logical record to overflow from one track to another track. This feature is highly useful in achieving greater data packing efficiency and in formatting records which exceed the capacity of the track.

Model 70/564 Disc Storage Unit

The Model 70/564 Disc Storage Unit provides random-access storage for 7.25 million bytes of information on an interchangeable disc pack. The operation of this device is controlled by the Model 70/551 Random Access Controller and up to eight units may be attached to one controller.

The disc storage unit consists of 203 tracks per read/write head and has 10 heads providing a total disc-pack capacity of 2,030 tracks. With a packing density of 1,100 bits per inch, each track contains 3,660 bytes producing a total information capacity of 7.25 million bytes per disc pack.

The disc pack is removable and interchangeable. Interchangeability denotes the capability of any disc-storage unit to read disc-pack information previously written by any other disc storage unit. The disc pack weighs about 10 pounds and can be changed in less than one minute.

Data is transferred between the processor and the disc pack at the rate of 156,000 bytes per second. The track-to-track access is 30 milliseconds. The average seek time is 85 milliseconds with a maximum of 145 milliseconds. Since the discs rotate at 2,400 RPM there is an average latency of 12.5 milliseconds.

All accuracy control and data validity checking for the Disc Storage Unit are performed in conjunction with the Model 70/551 Random Access Controller.

Model 70/565 Drum Memory Unit

The Model 70/565 Drum Memory Unit consists of a magnetic data drum and associated control electronics. The operation of the device is controlled by the Model 70/551 Random Access Controller. The drum provides random-access storage up to a maximum of 1 million 8-bit bytes.

The drum consists of 16 cylinders, each cylinder containing 32 tracks. A packing density of 570 bits per inch provides a track-storage capacity of 2,020 bytes per track. The drum has 512 read/write heads (one per track) thus making each track individually addressable. A drum speed of 3,600 RPM produces an average access time of 8.6 milliseconds. Data is transferred at approximately 936,000 bits/sec of 117,000 bytes/sec.

All accuracy-control and data-validity checking for this device is performed in conjunction with the Model 70/551 Random Access Controller.

Model 70/568 Mass Storage Unit

The Model 70/568 Mass Storage Unit consists of a mass storage, retrieval unit, and associated control electronics. The operation of this device is controlled by the Model 70/551 Random Access Controller. The Model 70/568-1 consists of from one to eight removable magazines. The Model 70/568-2 Extension Assembly can be added to the mass storage unit to increase the magazine capacity to 16. The mass-storage unit and the expansion assembly are serviced by one read/write station. Up to 8 read/write stations may be attached to a Model 70/551 Random Access Controller, providing multi-billion byte-storage capacity in the millisecond access range.

The basic storage elements of the mass memory unit is a 16-inch by 4½ inch magnetic card. Data is recorded on one side of the card only. Each Model 70/568 card contains 18 separately addressable tracks of 960 bytes each. There are 256 cards housed in each magazine.

A card is removed from a magazine and enters a raceway over which it is transported to a read/write station (revolving capstan). At the read/write station the card passes beneath a set of eight read/write heads where data is either read or recorded. The read/write station includes a gate which controls the recirculation or return of the card to its associated magazine.

All accuracy control and data validity checking for the Mass Storage Unit is performed in conjunction with the Model 70/551 Random Access Controller.

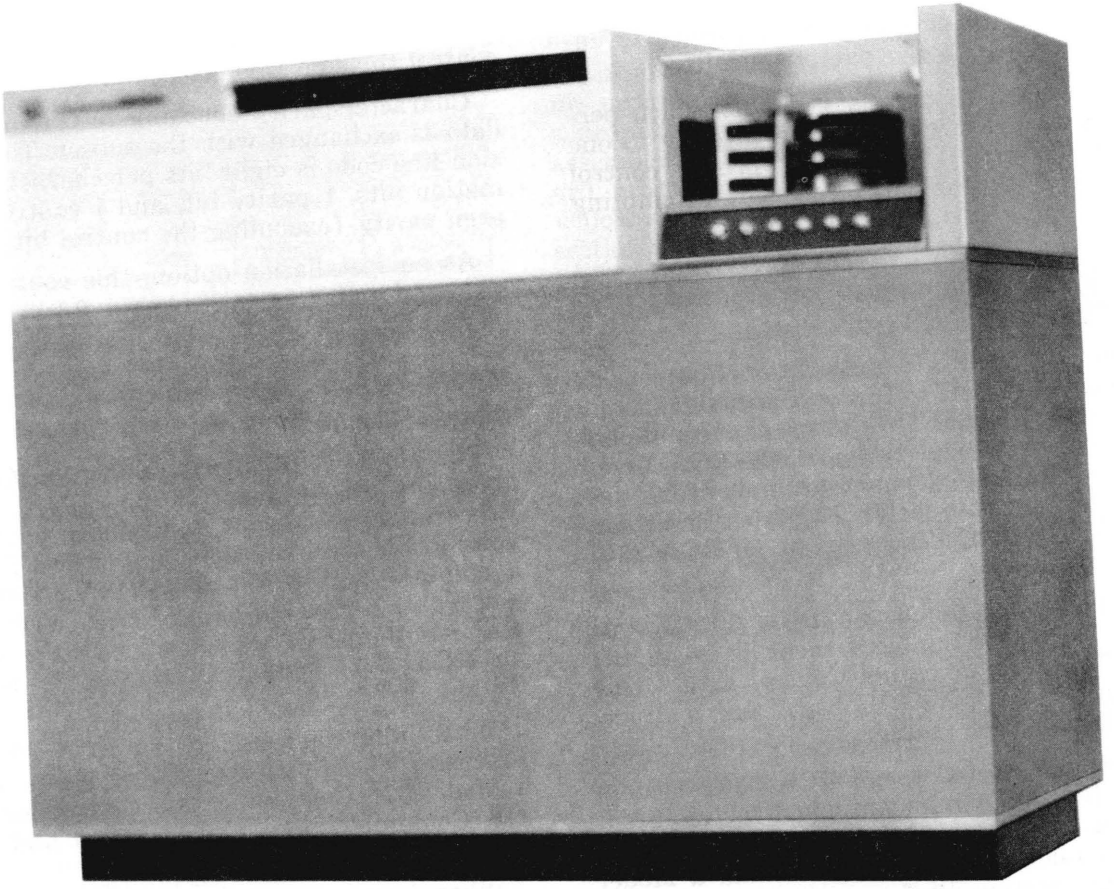

Figure 11. Model 70/568 Mass Storage Unit

Model 70/627 Data Exchange Control

The Model 70/627 Data Exchange Control (DXC) enables any two RCA Spectra 70 Series Processors 70/15, 70/25, 70/45 or 70/55 to communicate with each other. Data transmission may be in either direction but only in one direction at a time.

This unit provides two sets of cables, each of which connects to a processor via the RCA Standard Interface. Data is transmitted between the DXC and a processor in bursts of 8 bytes at the maximum rate of the interconnecting channel. The average data rate depends on the type of channel used and the number of simultaneously active devices attached to the transmitting or receiving processor.

Character-parity checking is performed to ensure the accuracy of the data transmitted.

An installation feature is available which permits the user to assign initiation priority to one of the processors. This ensures proper control over the possibility of two processors attempting to initiate transmission simultaneously.

Model 70/652 Communication Control (Single Channel)

The Model 70/652 Communication Control enables the RCA Model 70/15 Processor to transmit and receive data via 3KC voice-grade communications lines. With this control unit, the RCA Model 70/15 Processor can exchange data over long distances with another Spectra 70 Series Processor, an RCA 301 System Processor, or an RCA 3301 System Processor.

When interconnected to an RCA 301 System Processor the following equipment is required: a Model 376 Communication Control *or* a Model 378 Communication Mode Control and a Model 6012 Communication Buffer.

When interconnected to an RCA 3301 System Processor the following equipment is required: Model 3376 Communication Control *or* a Model 3378 Communication Mode Control and a Model 6012 Communication Buffer.

The communication control unit performs both the transmit function and the receive function, one function at a time, over a single telephone line as in a half-duplex operation. This control unit can operate with public telephone network systems, leased-lines, or private telephone network systems. Digital subsets are required to interface the communications lines. Manual or automatic dialing and automatic answering techniques may be employed.

Model No.	Service	Data Set	Data Rate bits/sec
70/652-26	Message Network—Auto. Dial	AT&T 201A3	2000
70/652-25	Message Network—Manual Dial	AT&T 201A3	2000
70/652-25	Private Line	AT&T 201B	2400
70/652-25	Private Line	W.U. 2241	2400
70/652-25	Broad-band Switching—Manual Dial	W.U. 2241	2400

Transmission rate is at 250 or 300 characters per second for message network and private-wire facilities, respectively.

The communication control interfaces the digital subset and does character framing and serialization of the data being exchanged. Channel coordination functions are effected by program control through this control unit.

Character-parity checking is performed as the data is exchanged with the subset. The transmission line code is eight bits per character (6 information bits, 1 parity bit, and 1 control bit) with even parity (excluding the control bit).

As an installation option, this control unit can be readily adapted to exchange 9-level code.

Model 70/653 Communication Control (Single Channel)

The Model 70/653 Communication Control enables the RCA Model 70/25, 70/45, or 70/55 Processors to transmit and receive data via 3KC voice-grade communications lines or a line having a nominal band-width of 48KC. This control enables data to be exchanged over long distances with another RCA Spectra 70 Series Processor, an RCA 301 System Processor, or RCA 3301 System Processor.

When interconnected to an RCA 301 System Processor the following equipment is required: a Model 376 Communication Control *or* a Model 378 Communication Mode Control and a Model 6012 Communication Buffer.

When interconnected to an RCA 3301 System Processor the following equipment is required: a Model 3376 Communication Control *or* a Model 3378 Communication Mode Control and a Model 6012 Communication Buffer.

The communication control unit performs both the transmit function and the receive function, one function at a time, over a single telephone line as in a half-duplex operation. This control unit can operate with public-telephone network systems, leased-lines, or private-telephone network systems. Digital subsets are required to

interface the communications lines. Manual or automatic dialing and automatic answering techniques may be employed.

Model No.	Service	Data Set	Data Rate bits/sec
70/653-26	Message Network—Auto. Dial	AT&T 201A3	2000
70/653-25	Message Network—Manual Dial	AT&T 201A3	2000
70/653-25	Private Line	AT&T 201B	2400
70/653-25	Private Line	W.U. 2241	2400
70/653-25	Broad-band Switching—Manual Dial	W.U. 2241	2400
70/653-34	AT&T Telpak A	AT&T 301B	40,800

For Models 70/653-5 and 70/653-26, transmission rate via 3KC voice-grade communications lines is 250 or 300 characters per second for message network and private-wire facilities, respectively.

Transmission rate is 5,100 characters per second for Model 70/653-34 over private-leased lines having a nominal bandwidth of 48KC.

The communication control interfaces the digital subset and does character framing and serialization of the data being exchanged. Channel coordination functions are performed automatically. Initiation and termination functions are effected under program control. Character and message-block parity checking is done by this control unit as the data is exchanged with the subset.

The transmission line code is eight bits per character (6 information bits, 1 parity bit, and 1 control bit) with even parity (excluding control bit).

As an installation option, this control unit can be readily adapted to exchange 9-level code.

Model 70/664 Communication Buffer Control

The Model 70/664 Communication Buffer Control provides the interface matching for the Model 70/672 Communication Multiplexor Channel and the communication line buffers (Model 70/710 Telegraph Buffer, Models 70/720, 70/721, 70/722 Communications Buffers, and Model 70/723 Autodin Buffer). The buffer control continuously scans the line buffers transferring status information and data characters to the communication multiplexor channel via the standard interface, as well as interpreting and executing the commands received from the communication multiplexor.

One buffer control services up to 48 line buffers accommodating a variety of grades of communications circuits operating at various transmission rates (45.5 bits per second through 4,800 bits per second). This capability permits simultaneous use of a broad range of communications devices in duplex and half-duplex operation.

When equipped with the Autodin special feature, the buffer control can accommodate up to six Model 70/723 Autodin Buffers.

Model 70/672
Communication Multiplexor Channel

The Model 70/672 Communication Multiplexor Channel (CMC) enables the RCA Model 70/45 to perform simultaneous, multiline servicing for up to 256 remote communications devices or equivalent combination of remote and peripheral devices. This unit replaces the standard multiplexor channel but retains the same basic relationship to the processor and peripheral devices.

The CMC accommodates a wide range of communications facilities, terminals, and channel coordination procedures. Provision is made for the following communications systems' characteristics:

- 5-level telegraph systems using "FIGS H LTRS" terminate sequence (U. S. standard)
- 5-level telegraph systems using "NNNN" terminate sequence (international standard)
- 5-level telegraph systems using RCA 301/3301 compatible control (DD_1, DD_2)
- 6-level teletypesetter systems
- 5, 6, 7, and 8-level data speed models I and II systems using ASCII
- Autodin system field-data code or ASCII Remote UNIVAC 1004 system
- Card Transceiver system using "4 out of 8" constant ratio code
- IBM 1050 systems
- IBM synchronous transmit/receive system (teleprocessing systems)
- Remote terminals using RCA 301/3301 code
- Remote RCA 301/3301 System Processor equipped with a Model 378/3378 Communication Mode Control and Model 6012 Communication Buffer *or* with a Model 376/3376 Communication Control.

By using one or more Model 70/664 Communication Buffer Control (up to a maximum of eight) and the appropriate buffers, any combination of the above communications systems (up to a maximum of eight different systems) can be implemented for a given communication multiplexor channel. As an alternative, any of the above communications systems can be combined with standdard input-output controls and devices within the limitations imposed by available trunk and system capacity.

The communication multiplexor channel executes the input-output instructions initiated by the program of the processor. It performs the channel coordination functions as specified by the program. The program designates the rules under which each communication line and terminal device will operate. These rules include the control characters to be recognized and the action the communication multiplexor channel is to take upon such recognition.

The program-initiated instructions are executed by the multiplexor channel by commands to the Model 70/664 Communication Buffer Control through the standard interface. In addition to executing these commands, the communication buffer control effects the necessary timing, control, and data interchange between the multiplexor and the line buffer. The line buffer provides the proper interface to the line and device by framing inbound characters, serializing outbound characters, and coordinating with the buffer control in the transfer of each character.

Once the input-output instruction is initiated by the processor program, the flow of data is essentially independent of the processor.

The communication multiplexor channel automatically performs character and message block-parity checking as required for any given system.

Transmission rates vary with the characteristics of the individual communication system employed. The buffers used in communications systems previously listed fall into one of the following categories of character configuration and transmission rate:

Bits Per Second	Char. Per Second	Line Code Units per Char.
45.5 to 75	5.3 to 10.0	7.5 to 8.5
75 to 180	10 to 18	9.0 to 11.5
1,050 to 1,800	100 to 180	Always 10.0
2,000 or 2,400	250 or 300	7.0, 8.0, 9.0
1,200 to 4,800	150 to 600	Always 8.0

Model 70/710 Telegraph Buffer

The Model 70/710 Telegraph Buffer permits communications between an RCA Model 70/45 Processor equipped with a Model 70/672 Communication Multiplexor Channel, a Model 70/664 Communication Buffer Control, and remote teletypewriter devices over private-telegraph circuits. This buffer provides two-way, non-simultaneous operation between the processor and the remote devices. Simultaneous operations on a full-duplex circuit requires two buffers. Each buffer is associated with one scan position on the communication buffer control. Single station and multiple station circuits can be accommodated with this buffer. The telegraph buffer operates with 5-level codes at transmission speeds of 60, 66, 75, and 100 words per minute. It also operates with 6-level code at 53 and 66 words per minute. The code levels transmission rates are selected at the time of installation. No data detection is also an installation option.

Model 70/720 Communication Buffer

The Model 70/720 Communication Buffer enables an RCA 70/45 Processor equipped with a Model 70/672 Communication Multiplexor Channel and a Model 70/664 Communication Buffer Control to communicate with remote devices over common-carrier facilities. This buffer provides two-way, non-simultaneous operation between the processor and a remote device and occupies one scan position on the communication buffer control. Two buffers, each occupying a scan position on the communication buffer control, provide two-way simultaneous operation.

A number of installation options are offered with this buffer. Depending on the options selected, this buffer operates with data subsets at speeds up to 180 bits per second on voice and sub-voice grade circuits and up to 110 bits per second on telegraph circuits. Other installation options include no data detection and constant-code ratio.

The following special feature is available with this buffer:

Auto Call — provides automatic dialing facility when used with an AT&T 801A Automatic Calling Unit.

Model 70/721 Communication Buffer

The Model 70/721 Communication Buffer enables the RCA 70/45 Processor equipped with the Model 70/672 Communication Multiplexor Channel and the Model 70/664 Communication Buffer Control to communicate with remote devices over common carrier facilities at transmission speeds up to 1,800 bits per second. The buffer provides two-way non-simultaneous operation between the processor and the remote device and occupies one scan position on the communication buffer control. Two-way simultaneous operation is provided by

two buffers occupying two scan position on the communication buffer control.

Installation options include no data detection and reverse channel. The following special feature is available with this buffer:

Auto Call — provides automatic dialing facility when used with an AT&T 801A Automatic Calling Unit.

Model 70/722 Communication Buffer

The Model 70/722 Communication Buffer enables the RCA 70/45 equipped with the Model 70/672 Communication Multiplexor Channel and the Model 70/664 Communication Buffer Control to communicate with remote devices over common-carrier voice-grade facilities at transmission speeds of up to 2,400 bits per second. This buffer provides two-way, non-simultaneous operation between the processor and the remote devices and occupies one scan position on the communication buffer control. Two-way simultaneous operation requires two buffers and occupies two scan positions on the communication buffer control.

This buffer accommodates transmission line characters containing 7, 8, or 9 bits. Installation options include no data detection and constant ratio code.

The following special feature is available with this buffer:

Auto Call — provides automatic dialing facility when used with an AT&T 801A Automatic Calling Unit.

Model 70/723 Autodin Buffer

The Model 70/723 Autodin Buffer enables the RCA 70/45 Processor equipped with the Model 70/672 Communication Multiplexor Channel and Model 70/664 Communication Buffer Control (with the Autodin Special Feature) to send and receive data via the Autodin Communication Network.

This buffer operates in the full-duplex continuous transmission, Mode -1 of the Autodin Network, utilizing the full Autodin channel coordination procedures.

This buffer functions with Field Data or ASCII Autodin Network synchronous transmission line code. This code accommodates 8-bit characters preserving the parity sense of all characters. The buffer is also capable of operating with government-furnished cryptographic equipment.

Transmission rates ar 1,200, 2,400, and 4,800 bits per second (150, 300, and 600 characters per second respectively).

Model 6050 Video Data Terminal

The Model 6050 Video Data Terminal, a highly reliable keyboard-input and video-display output device, enables the operator to communicate with the RCA Models 70/45 and 70/55 Processors via public or private-telephone networks.

Inquiries and transactions may be composed and visually verified by the operator before being transmitted to the processor. The response from the processor is displayed as long as it is required. It is reset under operator control.

The viewer utilizes a 14-inch rectangular cathode-ray tube. The viewer cabinet is suitable for table-top mounting and also can be readily adapted to customized wall or counter installation.

A control panel which may be attached to the front of the viewer or positioned independently on a desk pedestal, or other convenient horizontal surface, contains the operator's controls and indicators. A conventional 4-row keyboard is incorporated on the control panel for the generation of all data characters and those control characters which are to be transmitted.

Up to 480 characters can be displayed in 15 lines of 32 characters per line. The displayed characters are 0.22-inch high, 0.18-inch wide with 0.4-inch vertical and 0.25-inch horizontal spacing.

Two versions of this terminal are available. Model 6050-1 has a transmission rate of 105 or 180 characters per second. Its transmission line code contains 10 bits (1 start bit, 8 information bits including even parity, and 1 stop bit). Model 6050-2 has a transmission rate of 10 characters per second. Its transmission line code contains 11 bits (1 start bit, 8 information bits, and 2 stop bits).

All characters are checked for even parity upon receipt by the terminal. All transmitted characters have even parity.

Model 6051 Video Data Interrogator

The Model 6051 Video Data Interrogator, a highly reliable keyboard-input and video-display output device, enables the operator to communicate with the RCA 70/45 and 70/55 Processors via public or private-telephone networks at transmission rates of 105 or 180 characters per second. Up to eight of these units are serviced by the Model 6077 Interrogator Control Terminal.

Inquiries and transactions may be composed and visually verified by the operator before being transmitted to the processor. The response from the processor is displayed as long as it is required.

It is reset by the operator. Pre-recorded message formats are instantly available for display, under operator control, to enhance the accuracy and convenience of message composition.

The viewer utilizes a 14-inch rectangular cathode-ray tube. The viewer cabinet is suitable for table-top mounting and can be readily adapted to customized wall or counter installation. A control panel which may be attached to the front of the viewer or positioned independently on a desk pedestal or other convenient horizontal surface, contains the operator's controls and indicators. A conventional 4-row keyboard is incorporated on the control panel for the generation of all data characters and those control characters which are to be transmitted.

Up to 480 characters can be displayed in 15 lines of 32 characters per line (including format characters). The displayed characters are 0.22-inch high, 0.18-inch wide with 0.4-inch vertical and 0.25-inch horizontal spacing.

Model 6077 Interrogator Control Terminal

The Model 6077 Interrogator Control Terminal provides display memory and control for up to eight Model 6051 Video Data Interrogator units.

This display memory provides storage capacity of 480 displayable character locations for each of the eight video data interrogator units it services. In addition, it stores up to 16 pre-recorded message formats which are accessible by any of the interrogator units.

The interrogator control terminal exchanges data with the processor in a half-duplex (non-simultaneous send and receive) operation. It may be used with public or private-telephone networks at transmission rates of 105 or 180 characters per second.

The transmission line code is 10 bits per character (1 start bit, 8 information bits including even parity, and 1 stop bit). All characters are checked for proper parity upon receipt by the terminal.

PROGRAMMING SYSTEMS DESCRIPTION

RCA 70/15 PROGRAMMING SYSTEMS

System Concept

The RCA 70/15 Programming System, a complete and integrated system of related programs, assists the user in the efficient operation of his 70/15 System. The essential tools are provided for a broad-range of applications. The system is flexible in that it may be oriented towards cards and/or magnetic tape. The separation of programs by device requirement is unnecessary since all routines, except those specifically intended for tape, process either punched cards or tape-stored data. The use of optional devices and complete device interchangeability is permitted.

A basic card-oriented library system is available to aid the user in his processing. This library may be enhanced by the addition of magnetic tapes to achieve greater operating efficiency. Provision is also made for library operation of programs stored as card images on magnetic tape.

All programs, with the exception of the Sort/Merge, operate on a basic configuration consisting of a 70/15 Processor with a 4K-byte high-speed memory, a card reader, and a printer. The Sort/Merge requires an additional 4K-byte memory and a minimum of four magnetic tape stations.

This programming system converts symbolic representations to machine instructions, assists in running segmented programs, and provides standard operational subprograms such as input-output control. Parameters initiate program calls and designate device assignments. By stacking the parameter cards, a sequential set of independent or dependent production programs, may be processed.

The 70/15 Programming System facilitates the operation of single-segment programs and program operation involving subprograms or with overlay segments. The system provides, in addition to the normal loading of complete programs, the following features:

1. Linking common references of subprograms during the loading of the program for execution. This linkage is achieved through the facility of the Relocatable Loader routine.
2. Assembling and testing of subprograms as separate entities. At execution time, these subprograms may be bound together as a single processing program, through the use of the system maintenance routines.
3. Overlaying of segmented programs under the control of the programmer in conjunction with the Loader routine.

The 70/15 Programming System consists of various other aids for the user to allow efficient utilization of his equipment. In summary, the entire system meets the needs of the user without the burden of unnecessary program overhead.

Components

The components of the 70/15 Programming System are as follows: Assembly System, Loader Routines, Input-Output Control, Test Routines, Utility Routines, Communication Control, System Maintenance Routines, Report Program Generator, and Sort/Merge. A description of each component follows.

Assembly System

The 70/15 Assembly System provides the user with automatic conversion of a symbolic source language into computer-recognizable object program. This automatic conversion assists the programmer by reducing the amount of complex details required to code in machine language. The source program is written in the assembly language and converted to machine language by the 70/15 Assembler for subsequent machine execution.

Source language input and object program output may be punched on cards or stored on magnetic tape. The Assembler produces a listing of both the source and object programs.

Several of the characteristics of the assembler are summarized below, however, this list of features is neither exhaustive nor detailed.

1. *Operation Code Mnemonics:* Each machine instruction is assigned a unique mnemonic operation code as specified in the assembly language. The programmer uses these mnemonics instead of the less readable binary-bit combinations to specify his desired instructions.
2. *Symbolic Addressing:* Every memory location is available for assignment as a symbolic name for program reference. This symbolic name allows reference to branch points, tables, constants, and storage areas without requiring knowledge of absolute high-speed memory addresses which will subsequently be assigned by the assembler.
3. *Expressions:* The Assembler provides the ability to combine symbols and numeric values to

form desired addresses. For example, relative addressing where items in the program are addressed relative to a defined symbol; i.e., an incremented or decremented value relative to a defined symbolic name.

4. *External References:* The Assembler enables a program or a subprogram to reference data and/or control information outside its boundaries. This feature is provided via a unique program symbolic name that represents the desired reference. Thus, separately assembled subprograms may be linked together at execution time.

In addition to these features, the Assembler also provides for relocatable subprograms and extensive error checking with appropriate warning flags.

Loader Routines

The Loader routines accept assembler-generated output from cards or magnetic tape and inserts it into memory. Under controlled execution, the loaders permit changes to the production program and assist in the acquisition of overlay segments. A self-protection feature of all Loader routines includes an error indication; i.e., whenever a program is assigned to memory locations currently occupied by the Loader routine itself, an error indication is designated. Also, whenever an attempt is made to load a program beyond the memory capacity of the system, an error is so designated. The following Loader routines are available:

1. *Absolute Loader:* The Absolute Loader is required while loading programs into a predesignated location of memory. After the object program has been inserted into memory, control is transferred by the Loader as designated. Optional features of the Absolute Loader permit the use of Patch and Execute cards, and allow for the calling of overlay segments.
2. *Relocatable Loader:* The Relocatable Loader loads and relocates programs in memory. In addition, this routine links together subprograms into memory in a single operation, call another. The abilities to load one or more programs into memory is a single operation, call of overlay segments, and Patch with Execute options are also included.
3. *Tape Scan Loader:* The Tape-Scan Loader is used in conjunction with either the Absolute or Relocatable Loader, and is designed to call programs and program segments from magnetic tapes. Error-recovery procedures are incorporated in this routine.

Input-Output Control

The Input-Output Control provides the user with complete data interchange capability between the processor and on-line peripheral devices. This includes magnetic tape, card reader, paper tape reader/punch, card punch, and printer.

Complete versatility is available in that the control system may be assembled with the user program, linked in the binding run, or loaded and linked with the user's program at object time. Simultaneous processing capabilities are utilized whenever possible and error recovery is initiated when required. Device-type interchangeability is allowed at object-run time.

Test Routines

A set of Test routines is available to assist the user in perfecting the logic of compiled programs. The basic requirements for a complete and efficient test operation are provided for in the following routines:

1. *Test Data Generating:* The Test Data Generator routine provides the user with the ability to generate essentially unlimited amounts of test data from a small number of parameter cards. Output may be written to magnetic tape, paper tape, or cards. The size and type of test data required are designated by the user through a set of parameters. Each field of the record is defined separately and may consist of alphabetic, numeric, alphanumeric, 4-bit decimal, or binary data. Records may be fixed or variable in length and batched or unbatched according to user's requirements. Multireel files or multifile reels may be generated.
2. *Memory Print:* Two versions of the Memory Print routine are provided and their use depends on the availability of memory and the type of print required.
   a. *One-Phase Dump:* prints memory at completion of a test operation. This dump provides complete editing and printing capabilities. The one-phase dump may be assembled with the source program during compilation or entered by use of the Relocatable Loader. The user's requirements determine whether to print all or several non-contiguous parts of memory.
   b. *Two Phase Dump:* this version is used whenever there is insufficient memory available to load the one phase dump. Whenever the user requires a picture of the content of memory, the first phase writes the designated locations of memory to an external

storage media. The second phase reads the external storage media, edits and prints the contents of memory.

The output format of both versions is a line of characters followed by a line of hexadecimal equivalents.

3. *Tape Print Selective:* The Tape Print Selective routine edits and prints all or a designated portion of a magnetic tape. A complete set of options is provided depending on the requirements and control symbols available. The edited output may be printed in graphics and/or hexadecimal whichever the user designates.
4. *Tape Compare:* The Tape Compare routine provides the user with the ability to compare all or selected portions of two magnetic tapes and to produce a listing of any discrepancies. The comparison is done on a record basis even though the tape format may be batched. Automatic recovery from a mis-match is accomplished when the data records are in ascending sequence.

Utility Routines

The Utility routines consists of three media-to-media conversion routines. Complete interchangeability on both input and output devices is included within each routine. All routines are designed so that any two of them may concurrently share the processor. The Utility routines are as follows:

1. *Card-to-Tape:* The Card-to-Tape routine transcribes card records to tape while organizing the data into a variety of desired formats. Cards may be batched and proper control symbols will be generated while creating multireel files or multifile reels. Files may carry standard or non-standard labels; or they may be unlabeled as directed.
2. *Card-to-Punch:* The Card-to-Punch routine accepts batched or single records from cards or tapes and produces a card deck. Records may be batched when tape input is specified. A single file on a multifile tape may be extracted and processed. Also, the facility exists to modify the identification field on program cards before punching.
3. *Card-to-Printer:* The Card-to-Printer routine accepts a deck of input records and after appropriate editing, transcribes them to the printer. Records with or without control information may be printed. When the input is magnetic tape, batched records will be accepted and the additional capability to print a selected file from a multireel file is included. Program library tapes are also acceptable input to this routine.

Communication Control

The Communication Control system consists of a combined Receive/Transmit routine and several optional routines based on the user's specifications. The optional routines include sequential numbering of transmitted messages and sequence number checking of received messages. In addition, a Message-Journalizing routine is available using either magnetic tape or printer as external media.

The receive mode of the Receive/Transmit routine is entered as the result of a device request interrupt. Error checks and initiation for retransmission of error messages are automatic and control is returned to the programmer after the error-free message has been received. The transmit mode is entered by a direct transfer from the user's program. After the completion of a successful transmission, control will be returned to the programmer. Notification of errors will be supplied to the operator via the printer.

System Library Maintenance Routines

The System Library Maintenance routines provide for the updating of programs with changes as well as the combining of subprograms. Magnetic tape libraries and card libraries are maintained by the following routines:

1. *Update:* The Update routine replaces, inserts, and deletes instructions and/or complete programs from tape libraries. Multifile-data reels can also be changed by reference to the file by its name or ordinal position.
2. *Binder:* The Binder routine consolidates (binds) two or more relocatable subprograms into one absolute program. Any number of subprograms may be bound as long as the final output does not exceed the memory capacity. Binding of subprograms provides a single executable program for subsequent operation.

Report Program Generator

The Report Program Generator is a procedure-oriented language that provides a means for producing report programs. The language includes the report features of input data selection, editing, calculating, summarizing, and control breaks. The user provides input and output descriptions and the format required for output. User's own coding can be incorporated at a variety of points in the generated program.

Sort/Merge

The Sort/Merge generates a problem-oriented program to effectively utilize the available equipment configuration. The system permits the user to describe his sorting and merging requirements

(parameters) in the same format as the assembly language. Segmentation and overlays are used to reduce core storage requirements, and complete facilities are available for own coding produced by the user. The Sort/Merge requires an 8K-byte memory and a minimum of four magnetic tapes.

RCA 70/25 PROGRAMMING SYSTEMS

System Concept

Users have traditionally been provided with various programming aids to facilitate common basis tasks of data processing; i.e., compiling and assembling, program testing and production operation. Today, however, advanced technology and a widening range of user applications require increased attention be given to a more complete and systematic approach to these tasks for greater operational efficiency. Additionally, it is equally important to provide programming systems which are efficient for different users with varying size equipment complements. The design objective here must be to minimize the overhead for the smaller complements and to provide for full and effective utilization of larger systems.

The RCA 70/25 Operating Systems are designed to fully meet the total requirements of each user in an efficient and comprehensive manner. The Operating Systems are designed to operate in two modes. The Monitor Operation mode is provided to facilitate the execution of run sequences such as compile, program linkage (binding) and testing, or compile and go. Each of these functions may be accomplished individually or jointly in one sequential operation without operator intervention. The Compile and Go option is suited to single-use program operations and to initiate program testing following final assembly. The Monitor Operation mode will accept the basic program elements (program sections) of the standard library system, and perform the necessary program linkage for testing and execution. This avoids the necessity for creating a production type (load) library.

The Production Operation mode provides for the efficient operation of pre-compiled and tested programs which are frequently run and seldom modified. Normal production-mode operation utilizes the standard load library which consists of all the required programs in a bound and executable form.

In addition, the programming design concept provides for two different levels or types of operating systems. Each level is tailored to a particular equipment environment and is identified as to operating media and core storage available in a system. For example, the Tape Operating System 16 indicates program storage and operation from magnetic tape in a system equipped with a 16K-byte high-speed memory. Finally, multiprogramming capabilities are provided in the operating system at the higher levels. Thus, each operating system is designed for efficient operation of users' programs within the specified environment.

Modes of Operation

MONITORED OPERATION

Monitored operation provides the user with complete and controlled facilities for creating program sections including assembling, testing, and formatting to library requirements without operator intervention. Control is achieved through the use of control cards which are inserted into the program source code input. The Monitor is called by the operator and is given the source code, program data files, and control card input file. The source code may then be assembled or compiled, bound with the required program sections, and/or executed in a diagnostic and test mode. When operating under test conditions, complete result information is supplied. The Monitor also controls compile and go operations where testing is not required and the run-to-run sequences of these operations.

PRODUCTION OPERATION

Under the Production Operation mode of system operation, a program is called in by the Executive Control and then executed. A program which contains overlays is executed starting with its initial segment. The successive overlays are then brought in and executed as required. When the program terminates, the system Executive informs the operator that a program has terminated and the operating system is ready to perform another processing task.

Multiprogramming

Processors with 32K or 65K bytes of memory may be used simultaneously by either two or three independent operations. There is no restriction as to what the three operations can be but they will be given time-shared use of the processor on a priority basis. Priority of a program is fixed during the entire time that the program is resident in memory. Three priority levels are available and are neither assigned nor changed by the system Executive. They can be assigned by the operator when a program is loaded or specified during program assembly. Operations making simultaneous use of the processor must have different priorities.

RCA provides the users with Peripheral and Communications Control systems. The Peripheral Control system contains routines for various peripheral processes such as card-to-tape and tape-

to-print. The Communication Control system contains routines for controlling and servicing communications lines. Either or both of these systems may be used as independent operations which time-share the processor with other operations.

Some examples of the simultaneous use of the processor by various operations are given below.

Example 1

Production Program	Monitored Operation

Example 2

Production Program	Peripheral Control System		
	Card to Tape	Tape to Printer	Tape to Punch

Example 3

Communication Control System	Monitored Operation	Peripheral Control System		
		Card to Tape	Tape to Printer	Tape to Punch

An example of varying use of the processor over a period of time is given below.

Time 1 — Enter Production Program.

Production Program

Time 2 — Production Program Continues.
Enter Peripheral Control System.

Production Program	Peripheral Control System		
	Card to Tape	Tape to Printer	Tape to Punch

Time 3 — Production Program Completed and Removed.
Monitored Operation Entered.

	Monitored Operation	Peripheral Control System		
		Card to Tape	Tape to Printer	Tape to Punch

Time 4 — Communication Control System Entered.

Communication Control System	Monitored Operation	Peripheral Control System		
		Card to Tape	Tape to Printer	Tape to Punch

It should be noted that it is permissible to have one, two, or three production programs operating simultaneously. One monitored operation may be executed simultaneously with any two other type operations.

Library Operation

The basic unit of program construction and the smallest unit of assembly is the program section. The Assembler acts on source code elements to produce program sections.

The basic unit of execution is the load. A load is a group of related coding that coexists in the processor at a given time. Loads are constructed by binding together program sections which are related to each other by reference calls. Loads may be in themselves either complete executable programs, or segments of a program utilized as overlays.

Libraries are utilized and maintained at both the program section and load levels. For example, a program section that is in the process of being assembled will automatically set up calls to standard program sections (i.e., FCP routines, etc.) which will subsequently be found on the program section library. After the calling program section is assembled, all of the called-program sections are bound with it. The bound sections then become a load which may be executed.

The user may then add his program sections and loads to their associated libraries via the System Maintenance routines. The generation and maintenance (i.e., replacement, deletion, and addition) of program section libraries and load libraries are the functions of these routines.

Components

The RCA 70/25 Tape Operating System 16

The RCA 70/25 Tape Operating System 16 is a magnetic tape-oriented programming system which provides efficient operation of a processor equipped with a minimum high-speed memory of 16K bytes and a standard-order code. A console typewriter is required and other optional features and equipment are utilized if available. A complete list of the Tape Operating System 16 components is as follows:

Executive
Monitor
Assembly System
File Control Processor (FCP)
Report Program Generator
Sort/Merge
Peripheral Control System
Communication Control System
(Single Channel)
System Library Maintenance Routines

THE EXECUTIVE

The *Executive* controls the loading of a single program or program system and supplies it with complete control of all peripheral device initiations and terminations, interrupt analysis and processing. The Executive asynchronously performs certain controlling functions such as console control, library search, assignment of devices, and allocation of memory as specified by the operator or by program control parameters. Operations are available for restart and for some classes of error recovery.

THE MONITOR

The *Monitor* controls the sequential execution of a string of programs, each of which requires a number of runs. It is used primarily for run sequences such as compile, bind, and test; or, compile and go for a string of programs to be processed one at a time.

In addition, the Monitor provides the following functions for program testing:

1. Formatting of input test data files and distribution to work tapes.
2. Editing facilities for memory snapshots of data during program execution.
3. Editing facilities for printouts of data in memory and on peripheral devices at the conclusion of a program test operation.
4. Collecting compiler listings, data files, memory data edits, and peripheral device data edits onto one output device for printing.

ASSEMBLY SYSTEM

The *Assembler* translates symbolic machine-oriented source language programs into machine code. The Assembler has provisions for mnemonic operation codes, symbolic addressing, and constant definition. Arithmetic expressions may be used to specify addresses. Symbolic addresses are automatically converted into machine-code base register plus displacement addresses.

Programs being assembled are permitted to make external references to other related but independently assembled programs. In addition, FCP macros are included in the assembly language, thus providing the linkage necessary to utilize this powerful input-output control facility. The Assembler produces object code, and source and object code listings which include error flags where appropriate.

FILE CONTROL PROCESSOR

The *File Control Processor (FCP)* is a generalized input-output system that provides rigorous control over all aspects of input-output operations.

The FCP achieves efficient and flexible input-output control by providing:

1. Efficient routines for simultaneous read and write operations.
2. Conservation of memory space by:
   a. Selecting routines specific to a given set of files.
   b. Eliminating duplicate routines for a set of files.
   c. Providing input-output initiation logic, termination logic, and standard error recovery code for the user.
3. Automatic handling of physical conditions for the user.
4. Standard operating procedures.

FCP Functions

The FCP includes the following functions for controlling input-output operations:

1. *Logical Record Read and Write:*
   Batched-record manipulation and any required physical input-output instructions are automatically provided when a programmer gives a Record Read or Write instruction.
2. *Label Checking and Label Construction:*
   Automatically constructs, inserts, and checks standard begin and end-file labels. Options are provided to omit labels and to provide for nonstandard labels.
3. *Data Handling:*
   The FCP processes the following data structures:
   a. Fixed-length records, unbatched
   b. Fixed-length records, batched
      Fixed or variable number of records in a batch
   c. Variable-length records, unbatched
   d. Variable-length records, batched
      Variable number of variable-length records in a batch
4. *Alternate Input-Output Areas:*
   Processing from one area with simultaneous read or write in the alternate area.
5. *Debatching for Tape Read Forward or Reverse:*
   Provides last record of a batch first on Read Reverse.
6. *Rerun:*
   Defines checkpoints for reruns.
7. *Multifile Control:*
   Automatic tape positioning to the proper file for reels containing more than one file.

8. *Multireel Control:*

   Simultaneous processing and rewind-remount on alternate reels for multireel files.

User Control of Physical Input-Output Devices

Users with unique input-output requirements can use the Executive for direct control of input-output devices. An input-output initiation requires a Supervisor Call to the Executive and an input-output definition set. The input-output definition set specifies the required channel-device name, the address of the desired input-output instruction, and the address of the appropriate interrupt-response code. The user must supply his own interrupt-response code.

Selection and Integration of FCP Program Sections with the User Program

FCP requirements are specified in source code by a set of file definitions for the required file control characteristics. The language processors create a program section containing:

1. The program's logical code.
2. Reference calls to the appropriate FCP program sections on the program section library.
3. A set of FCP parameters for each file.

The selected FCP program sections are bound with the program logical code when executable loads are constructed by Load Bind or Load Library Update routines.

REPORT PROGRAM GENERATOR

The *Report Program Generator* provides the means for producing report programs with a minimum of programmer effort and machine-compiling time.

The specific actions for a report program are written in a simple and convenient language which does not require knowledge of machine-language coding. The common report features of input-data selecting, editing, calculating, summarizing, control breaks, and error checking are available.

The programmer describes the input data, the operations to be performed on the data, and the output equipment to the Report Program Generator. The source program is divided into four parts: the file definitions, the input specifications, the calculation specifications, and the output-format specifications. It is modularly designed so that the user's own-code routines can be easily incorporated at a variety of points in the generated program.

SORT/MERGE

The *Sort/Merge* is a generalized tape sort and merge program. The system allows the user to describe his sort or merge parameters in the assembly language. Parameters and own code, if any, are written together and the Sort/Merge generates a specialized sort or merge program. Sort generation can be performed under monitor control, or specific sorts can exist on the load library.

Sort

The *Sort* capabilities are available as follows:

1. Sorting several full output reels.
2. Processing fixed and variable-size records.
3. Accommodating Spectra 70 Systems standard fixed and variable-data formats.
4. Handling up to 10 sequencing keys. Sequencing keys may be specified as alphanumeric or numeric and as ascending or descending.
5. Providing first, intermediate, and last pass own code options. Records may be added, deleted, or modified during first and last pass. During intermediate passes, records having equal sequencing keys may be processed.
6. Accepting Sort specifications and own coding, if any, in standard assembly language.
7. Accommodating user's own input read routines or final output routine.
8. Displaying error messages on the console typewriter.
9. Providing rerun points between sort passes or between sorting cycles for multireel sorts.

Merge

The *Merge* capabilities are available as follows:

1. Merging from two to 10 data files originating on two or more magnetic tape reels.
2. Processing fixed and variable-size records.
3. Accommodating Spectra 70 Systems standard fixed and variable-data formats.
4. Handling up to 10 sequencing keys. Sequencing keys may be specified as alphanumeric or numeric and may be ascending or descending.
5. Providing last pass own coding options.
6. Accommodating alternate tape units.
7. Accepting merge specifications and own coding, if any, in standard assembly language.
8. Displaying error messages on the console typewriter.
9. Providing rerun points after each output tape of a merge.

PERIPHERAL CONTROL SYSTEM

The *Peripheral Control System* is a single program which consists of several independent input-output processes. Each of these independent processes is a unique routine, such as tape-to-printer and card-to-tape.

Execution of more than one of these independent processes can occur simultaneously. The execution of these different processes is coordinated by the Peripheral Control System. It is, therefore, possible to have more than one utility function proceeding at the same time for maximum utilization of the available input-output devices.

The Peripheral Control System is designed such that the only utility routines in memory are those required to perform current tasks. Thus, the tape-to-printer routine, for instance, would not take up core storage unless a tape-to-printer task needed to be performed.

The Peripheral Control System allows the user to substitute a utility routine of his own for the corresponding standard process and have the Peripheral Control System coordinate the execution of his routine with any others which may be required.

COMMUNICATION CONTROL SYSTEM

A *Communication Control System* is provided to control single channel communications lines, utilizing the Model 70/653 Communication Control (Single-Channel).

Routines included in the Communication Control System are provided in the areas of:

1. Line and termination control.
2. Message control consisting of logging, queuing, code translating, and sequence numbering.

Error checking and re-transmissions (where necessary) are performed by the Communication Control routines.

SYSTEM LIBRARY MAINTENANCE ROUTINES

The 70/25 Tape Operating System 16 contains four System Library Maintenance routines which produce executable machine-coded programs; and, in addition, generate and update system libraries. The system routines are as follows:

1. Program Section Library Insert
2. Program Section Library Update
3. Load Bind
4. Load Library Update

Program section libraries contain an index which defines all of the calling relationships among program sections contained in the library. Replacement and deletion of routines from a program section library require a complete reconstruction of the library's index. Inserting routines require only the appendage of a new set of index entries to the library's index. The Program Section Library Insert routine allows rapid addition of new routines to a program section library. The Program Section Library Update routine includes all of the functions needed to produce a new program section library from a pre-existing one.

Program Section Library Insert Routine

The Program Section Library Insert routine constructs a new program section library. This routine provides the facility for making rapid additions to a program section library. This insert routine uses a major and a minor input program section library and the output from this run is a new program section library.

Program Section Library Update Routine

The Program Section Library Update routine provides program section replacement, deletion, and insertion for changing the set of program sections contained on a program section library. This update routine acts on a program section library that is to be updated and on one containing replacement sections and additional program sections. Additional input is a set of control cards specifying the operations that are to be performed and the output is a new program section library.

Load Bind Routine

The Load Bind routine acts on a program section library containing sets of program sections. The members of each set are related to each other by reference calls. The Load Bind routine constructs a load from each such set. The loads include any standard program sections referenced by members of the set. The standard program sections are obtained from the installation program section library which is used as a second input to the Load Bind routine. The output of the Load Bind routine is a load library containing one load for each input set of program sections.

Load Library Update Routine

The Load Library Update routine contains three options:

1. To bind a set of routines and to insert the resulting loads into the output load library.
2. To automatically correct a load library.
3. To generate a load library containing a selected set of loads from the master load library.

Note: Options 1 and 2 may be used together.

The binding option acts on a program section library containing all of the program sections required by a program. It carries out reference-call binding and constructs a set of loads from the program section library elements. A load library is used as another input to the binding option. The output is a new load library which includes the newly constructed loads. Loads can also be deleted from a load library in the bind option.

The automatic correction option may be used by itself or together with the bind option. It acts on a load library under control of a set of correction specification cards to update loads made from old versions of corrected program sections. The output is a corrected load library.

The option to create a selected set of loads from the master load library requires as input a set of control cards indicating which loads are to be selected and a load library. The output is a selected load library.

RCA 70/25 Tape Operating System 32

The RCA 70/25 Tape Operating System 32, a magnetic tape-oriented programming system, provides for the efficient operation of a processor equipped with a minimum high-speed memory of 32K bytes and a standard order code. A console typewriter is required and other optional features and equipment are utilized if available. A complete list of the Tape Operating System 32 components is as follows:

Executive
Monitor
Assembly System
File Control Processor (FCP)
Report Program Generator
Sort/Merge
Peripheral Control System
Communication Control System
(Single Channel)
System Library Maintenance Routines

All of the components of the Tape Operating System 32 are identical to the Tape Operating System 16 components except for the Executive.

THE EXECUTIVE

The *Executive* for the Tape Operating System 32 provides all of the capabilities of the Tape Operating System 16 Executive. (See page 47.) In addition, it provides multiprogramming facilities for two or three independent programs to utilize the processor simultaneously. Any one of these programs may be running in either a Monitored or Production mode of operation. The programs are executed on a priority basis. These priorities are assigned by the user and programs maintain the same priority throughout their execution. Programs being executed together must have different priorities.

The Role of the Executive

The *Executive* undertakes the management and supervision of the entire system. It provides the basic control and interconnection that is necessary between the user's program and the operating system as well as between various components of the operating system. All input-output initiations and their resulting termination interrupts and any other interrupts, such as a divide error, require action by the Executive. The user's program must be able to communicate with the Executive as to what actions are required to correctly process his program. In order to accomplish this, the user's programs must observe certain conventions with respect to their structure for proper communication with the Executive.

Executive Information Area

A user's program must include unique interrupt-response code for the set of interrupts directly under user-program control. These include various contingency conditions such as overflow and divide errors. The starting addresses of these contingency response operations must be defined in the user's program. User's programs must also include a memory storage area for all of the registers directly related to it. These are the General-Purpose registers which the program uses and whose functions are described below. Contingency starting address and register storage areas are provided within a program in the Executive information area. The Executive information area must be included in every program and it must be located at the beginning of a program's initial load.

Input-Output Determined Program Structure

Input-output terminations are indicated in the 70/25 System by processor interrupts. All programs must include a response code for these interrupts. An interrupt-response code is supplied by RCA in its FCP; however, the Executive does not distinguish user-produced code from RCA-supplied code at the time a program is executed. Programs are structured into sets of main-chain operations and interrupt-response operations. Main-chain operations are the computational operations which do not depend on input-output interrupt for their initiation. Interrupt-response operations carry out the functions required in response to an input-output termination interrupt.

The Executive makes 30 General-Purpose registers available to each user's program; 15 are available for use by main-chain operations and 15 are

available for use by interrupt-response operations. Main-chain and interrupt- response operations do not have direct access to each others' general registers and cannot communicate with each other through these registers. Storage areas for these General-Purpose registers must be provided in the Executive information area.

Programming Input-Output Operations

INPUT-OUTPUT PROCESSES

An input-output operation is initiated by executing an input-output instruction. Termination of the defined input-output operation is indicated to the system by an interrupt. When the input-output interrupt occurs, the status information associated with the termination is passed to the interrupt-response code which checks for errors, etc. If certain standard types of errors are detected, the interrupt-response code can request the Executive to perform standard retry procedures.

THE FUNCTION OF THE EXECUTIVE IN INPUT-OUTPUT OPERATIONS

The Executive issues all input-output instructions and routes input-output interrupts to the pertinent interrupt-response operation. A user's program requiring the initiation of an input-output operation issues an input-output Request Supervisor Call macro to the Executive. This macro specifies a symbolic channel-device name, the location of the input-output instruction and the starting address of the pertinent interrupt-response operation. Input-output request coding is supplied by RCA in its FCP. FCP coding is incorporated into the user's program prior to the time of execution. Input-output request coding is viewed by the Executive as the user's program coding even though it was, in fact, supplied by RCA in its FCP.

The Executive accepts the input-output request, returns control immediately to the requesting program, and issues the input-output operation as soon as the specified channel and device are available. When the termination interrupt occurs, the Executive sets up an entry to the interrupt-response operation at the address which was specified by the input-output requester. Interrupt-response operations release control when the response functions have been completed by issuing a Priority Relinquish Supervisor Call macro to the Executive. This macro notifies the Executive that system control is available to any operation. The Executive will return control to a program's main chain after all its outstanding input-output termination interrupts have been processed. Figure 12 shows the control flow between the user's program and the Executive during an input-output operation.

THE FORM OF AN INPUT-OUTPUT REQUEST

A program issuing an input-output Request Supervisor Call macro on the Executive must use a standard format. The format is:

1. Input-Output Request Supervisor Call.
2. Symbolic channel-device name.
3. Location of the input-output instruction.
4. Address for return of control to requestor.
5. Address of interrupt-response operation.

FCP coding supplied by RCA issues input-output requests in this form. This coding is viewed by the Executive as user-program coding.

Executive Operations

Certain major functions are made available to all users by including them as operations within the Executive. Console control is an example of such an operation. It is not part of the Executive mechanism required for input-output handling, interrupt routing, and multiprogram priority scheduling. (The latter mechanisms are required for the system to operate during any phase of program execution.) Console control, on the other hand, is not required during program execution unless some communication via the console occurs or is required. Although, not necessarily required for program execution, many programs do need access to the console typewriter. And, in addition, the console typewriter must always be available to the machine operator as a communication path to the Executive. For reasons such as these, certain operations are included in the Executive. Operations used to initiate, to load and terminate programs, to provide console communication, to provide facilities for restart and certain classes of error recovery are implemented as executive operations.

CALLING AN EXECUTIVE OPERATION

In general, a program's means of access to the Executive is a Supervisor Call macro. A class of Supervisor Call macros is provided for initiating the execution of Executive operations. Each of these Supervisor Call macros results in the execution of a particular Executive operation. A Supervisor Call macro to an Executive operation must include certain information in the following format:

1. Supervisor Call
2. Message Length
3. Operation Accepted Return Address
4. Operation Completed Return Address
5. Message

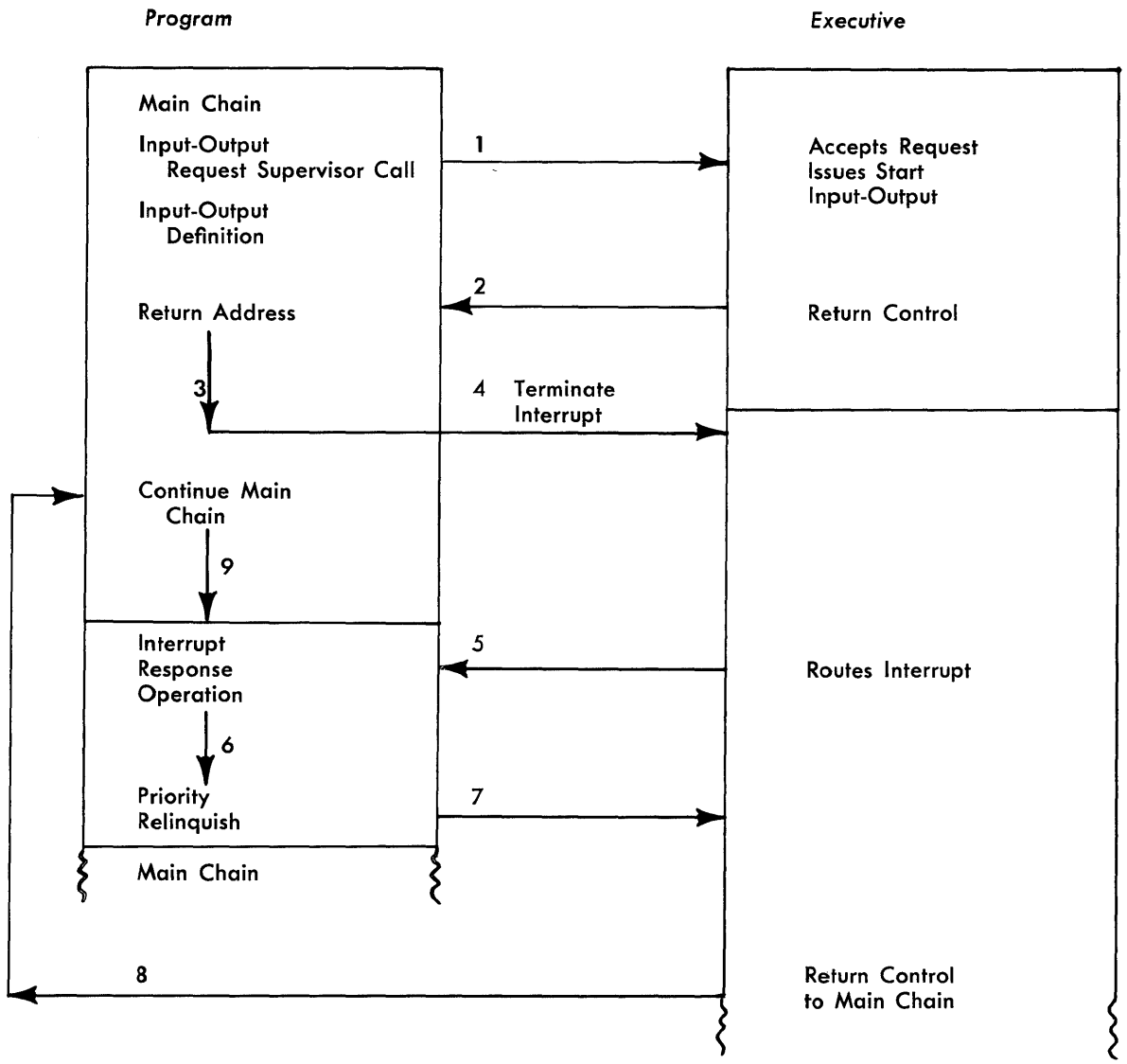

Figure 12. Control Flow During an Input-Output Operation

The *Supervisor Call* defines the desired Executive operation and alerts the Executive to the request by causing an identifiable interrupt.

Message Length defines the length in bytes of the message and hence the length in bytes of the whole Supervisor Call information set.

The *Operation Accepted Return Address* defines the location in the calling program to which control is to be returned after an entry to the Executive operation has been set up and queued.

The *Operation Completed Return Address* defines the location in the calling program to which control is to be returned after the Executive operation is completed. Control will normally be returned to the calling program at the acceptance address before the Executive operation is completed. But, whether this is so or not, control will always be given to the caller's acceptance return address before it is given to the operation completed return address.

The *Message* contains any information that the caller is transmitting to the Executive operation. For example, if a program is calling on the console-control operation to carry out a typeout, the message is that message to be typed out.

Register Preservation in Multiprogrammed System Operation

Register usage conflicts do not normally occur when a single program is running by itself on the computer. Conflicts are eliminated since every program is provided with two separate sets of registers, one for its main-chain operation and one for its interrupt-response operation.

A set of General-Purpose registers may have been used last by one program when the Executive determines that control is to be given to another program which uses the same set of registers. In this case, the Executive first stores the old program's registers in its Executive information area. Next, the new program's registers are loaded from its Executive information area. Finally, after register storing and reloading, the Executive gives control to the next program.

RCA 70/45-55 PROGRAMMING SYSTEMS

System Concept

Users have traditionally been provided with various programming aids to facilitate common basic tasks of data processing; i.e., compiling and assembling, program testing and production operation. Today, however, advanced technology and a widening range of user applications require increased attention be given to a more complete and systematic approach to these tasks for greater operational efficiency. Additionally, it is equally important to provide programming systems which are efficient for different users with varying size equipment complements. The design objective here must be to minimize the overhead for the smaller complements and to provide for full and effective utilization of larger systems.

The RCA 70/45-55 Operating Systems are designed to fully meet the total requirements of each user in an efficient and comprehensive manner. The Operating Systems are designed to operate in two modes. The Monitor Operation mode is provided to facilitate the execution of run sequences such as compile, program linkage (binding) and testing, or compile and go. Each of these functions may be accomplished individually or jointly in one sequential operation without operator intervention. The Compile and Go option is suited to single use program operations and particularly so for scientific "Job Shop" type applications. The Monitor Operation mode will accept the basic program elements (program sections) of the standard library system, and perform the necessary program linkage for testing and execution. This avoids the necessity for creating a production type (load) library. The standard library system performs the necessary program linkage for testing and executing the program. This avoids the necessity for creating a production type (load) library.

The Production Operation mode provides for the efficient operation of pre-compiled and tested program which are frequently run and seldom modified. Normal production-mode operation utilizes the standard load library which consists of all the required programs in a bound and executable form.

In addition, the design concept provides for several different levels or types of operating systems. Each level is tailored to a particular equipment environment and is identified as to operating media and core storage available in a system. For example, the Tape Operating System 16 indicates program storage and operation from magnetic tape in a system equipped with a 16K-byte high-speed memory. Multiprogramming capabilities are provided in the operating systems at the appropriate levels. In addition, multiprocessing functions are provided at the highest level for efficient utilization of a multisystem operation. Thus, each operating system is designed for efficient operation of users' programs within the specified environment.

Modes of Operation

MONITORED OPERATION

Monitor operation provides the user with complete and controlled facilities for creating program sections including assembling, testing, and formatting to library requirements without operator intervention. Control is achieved through the use of control cards which are inserted into the program source code input. The Monitor is called by the operator and is given the source code, program data files, and control card input file. The source code may then be assembled or compiled, bound with the required program sections, and/or executed in a diagnostic and test mode. When operating under test conditions, complete result information is supplied. The Monitor also controls compile and go operations where testing is not required and the run-to-run sequencing of these operations.

PRODUCTION OPERATION

Under the Production Operation mode of system operation, a program is called in by the Executive Control and then executed. A program which contains overlays is executed starting with its initial segment. The successive overlays are then brought in and executed as required. When

the program terminates, the Executive Control informs the operator that a program has terminated and the operating system is ready to perform the next processing task.

Multiprogramming

Processors with 32K or 65K bytes of memory may be used simultaneously by either two or three independent operations. There is no restriction as to what the three operations can be but they will be given time-shared use of the processor on a priority basis. Priority of a program is fixed during the entire time that the program is resident in memory. Three priority levels are available and are neither assigned nor changed by the system Executive. They can be assigned by the operator when a program is loaded or specified during program assembly or compilation. Operations making simultaneous use of the processor must have different priorities.

RCA provides the users with Peripheral and Communications Control systems. The Peripheral Control system contains routines for various peripheral processes such as card-to-tape and tape-to-print. The Communication Control system contains routines for controlling and servicing communications lines. Either or both of these systems may be used as independent operations which time-share the processor with other operations.

Some examples of the simultaneous use of the processor by various operations are given below.

Example 1

Production Program	Monitored Operation

Example 2

Production Program	Peripheral Control System		
	Card to Tape	Tape to Printer	Tape to Punch

Example 3

Communication Control System	Monitored Operation	Peripheral Control System		
		Card to Tape	Tape to Printer	Tape to Punch

An example of varying use of the processor over a period of time is given below.

Time 1 — Enter Production Program.

Production Program	

Time 2 — Production Program Continues. Enter Peripheral Control System.

Production Program	Peripheral Control System		
	Card to Tape	Tape to Printer	Tape to Punch

Time 3 — Production Program Completed and Removed. Monitored Operation Entered.

	Monitored Operation	Peripheral Control System		
		Card to Tape	Tape to Printer	Tape to Punch

Time 4 — Communication Control System Entered.

Communication Control System	Monitored Operation	Peripheral Control System		
		Card to Tape	Tape to Printer	Tape to Punch

It should be noted that it is permissible to have one, two, or three production programs operating simultaneously. One monitored operation may be executed simultaneously with any two other types of operations.

The Disc Operating System supplied for the 262K-byte processor controls the execution of a number of programs. The maximum number of programs controlled is dependent on the relationship between program sizes and memory space.

Library Operation

The basic unit of program construction and the smallest unit of assembly is the program section. Compilation and assembling act on source-code elements to produce program sections.

The basic unit of execution is the load. A load is a group of related coding that coexists in the processor at a given time. Loads are constructed by binding together program sections which are related to each other by reference calls. Loads may be in themselves either complete executable programs, or segments of a program utilized as overlays.

Libraries are utilized and maintained at both the program section and load levels. For example, a program section that is in the process of being assembled will automatically set up calls to standard program sections (e.g., FCP routines) which will subsequently be found in the program section library. After the calling program section is assembled, all of the called program sections are

bound with it. The bound sections then become a load which may be executed.

The user may then add his program sections and loads to their associated libraries via the System Maintenance routines. The generation and maintenance (i.e., replacement, deletion, and addition) of program section libraries and load libraries are the functions of these routines.

Components

RCA 70/45-55 Tape Operating System 16

The RCA 70/45-55 Tape Operating System 16 is a magnetic tape-oriented programming system which provides for efficient operation of a processor equipped with a minimum high-speed memory of 16K bytes and a standard order code. A console typewriter is required and other optional features and equipment are utilized if available.

A complete list of the Tape Operating System 16 components is as follows:

Executive
Monitor
Basic Assembly System
File Control Processor (FCP)
Report Program Generator
COBOL
FORTRAN
Sort/Merge
Peripheral Control System
Communication Control System
(Single-Channel)
System Library Maintenance Routines
Compatibility Support Package

THE EXECUTIVE

The *Executive* controls the loading of a single program or program system and supplies it with complete control of all peripheral device initiations and terminations, interrupt analysis and processing. The Executive asynchronously performs certain controlling functions such as console control, library search, assignment of devices, and allocation of memory as specified by the operator or by program control parameters. Operations are available for restart and for some classes of error recovery.

THE MONITOR

The *Monitor* controls the sequential execution of a string of programs, each of which requires a number of runs. It is used primarily for run sequences such as compile, bind and test; or, compile and go for a string of programs to be processed one at a time.

In addition, the Monitor provides the following functions for program testing:

1. Formatting of input test data files and distributing these files to work tapes.
2. Editing facilities for memory snapshots of data during program execution.
3. Editing facilities for printouts of data in memory and on peripheral devices at the conclusion of program test operation.
4. Collecting compiler listings, data files, memory data edits, and peripheral device data edits onto one output device for printing.

BASIC ASSEMBLY SYSTEM

The *Basic Assembler* translates symbolic machine-oriented source language programs into machine code. The Basic Assembler has provisions for mnemonic operation codes, symbolic addressing, and constant definition. Arithmetic expressions may be used to specify addresses. Symbolic addresses are automatically converted into machine-coded base register plus displacement addresses.

Programs being assembled are permitted to make external references to other related but independently assembled programs. In addition, FCP macros are included in the assembly language, thus providing the linkage necessary to utilize this powerful input-output control facility. The Basic Assembler produces object code, source and object code listings which include error flags where appropriate.

FILE CONTROL PROCESSOR

The *File Control Processor (FCP)* is a generalized input-output system that provides rigorous control over all input-output operations. The FCP achieves efficient and flexible input-output control by providing:

1. Efficient routines for simultaneous read and write operations.
2. Conservation of memory space by:
   a. Selecting routines specific to a given set of files.
   b. Eliminating duplicate routines for a set of files.
   c. Providing input-output initiation logic, termination logic, and standard error recovery codes for the user.
3. Automatic handling of physical conditions for the user.
4. Standard operating procedures.

FCP Functions

The FCP includes the following functions for controlling input-output operations:

1. *Logical Record Read and Write:*
   Batched-record manipulation and the required physical input-output instructions are automatically provided when a programmer gives a Record Read or Write instruction.
2. *Label Checking and Label Construction:*
   Automatically constructs, inserts, and checks standard begin and end file labels. Options are provided to omit labels and to provide for nonstandard labels.
3. *Data Handling:*
   The FCP processes the following data structures:
   a. Fixed-length records, unbatched
   b. Fixed-length records, batched
      Fixed or variable number of records in a batch
   c. Variable-length records, unbatched
   d. Variable-length records, batched
      Variable number of variable-length records in a batch
4. *Alternate Input-Output Areas:*
   Processing from one area with simultaneous read or write in the alternate area.
5. *Debatching for Tape Read Forward or Reverse:*
   Provides last record of a batch first on Read Reverse.
6. *Rerun:*
   Defines checkpoints for reruns.
7. *Multifile Control:*
   Automatic tape positioning to the proper file for reels containing more than one file.
8. *Multireel Control:*
   Simultaneous processing and rewind-remount on alternate reels for multireel files.

User Control of Physical Input-Output Devices

Users with unique input-output requirements can use the Executive for direct control of input-output devices. An input-output initiation requires a Supervisor Call to the Executive and an input-output definition set. The definition set specifies the required channel-device name, the address of a Channel Command Word (CCW) chain, and the address of the appropriate interrupt-response code. The user must supply his own interrupt-response code.

Selection and Integration of FCP Program Sections with the User Program

FCP requirements are specified in source code by a set of file definitions for the required file control characteristics. The language processors create a program section containing:

1. The program's logical code.
2. Reference calls to the appropriate FCP program sections on the program section library.
3. A set of FCP parameters for each file.

The selected FCP program sections are bound with the program logical code when executable loads are constructed by Load Bind or Load Library Update routines.

REPORT PROGRAM GENERATOR

The *Report Program Generator* provides the means for producing report programs with a minimum of programming effort and machine-compiling time.

The specific actions for a report program are written in a simple and convenient language which does not require knowledge of machine-language coding. The common report features of input data selecting, editing, calculating, summarizing, control breaks, and error checking are available.

The programmer describes the input data, the operations to be performed on the data, and the output equipment to the Report Program Generator. The source program is divided into four parts: file definitions, input specifications, calculation specifications, and output format specifications. It is modularly designed so that the user's own-code routines can be easily incorporated at a variety of points in the generated program.

COBOL

COBOL is a business data processing language. The COBOL compiler implements COBOL, as defined in the Department of Defense (DOD) COBOL specifications. Redundant language elements are omitted.

The compiler takes full advantage of available equipment. Compiling efficiency improves when more memory and peripheral devices are added to the system. The compiler is modular in construction and extensions can be included if sufficient memory is available.

FORTRAN

FORTRAN is a processing language for scientific and engineering applications. The FORTRAN compiler implements a subset of FORTRAN IV.

The FORTRAN compiler includes all the standard types of statement governing the functions of assignment, control, input-output, specification, and subprogram.

It should be noted that execution of a FORTRAN object program requires a floating-point arithmetic instruction set in the processor's instruction repertoire.

SORT/MERGE

The *Sort/Merge* is a generalized tape sort and merge program. The system allows the user to describe his sort or merge parameters in the basic assembly language. Parameters and own code, if any, are written together and the Sort/Merge generates a specialized sort or merge program. Sort generation can be performed under monitor control, or specific sorts can exist on the load library.

Sort

The *Sort* capabilities are available as follows:

1. Sorting several full output reels.
2. Processing fixed and variable-size records.
3. Accommodating Spectra 70 Systems standard fixed and variable-data formats.
4. Handling up to 10 sequencing keys. Sequencing keys may be specified as alphanumeric or numeric and as ascending or descending.
5. Providing first, intermediate, and last pass own code options. Records may be added, deleted, or modified during first and last pass. During intermediate passes, records having equal sequencing keys may be processed.
6. Accepting Sort specifications and own coding, if any, in standard basic assembly language.
7. Accommodating user's own input read routines or final output routine.
8. Displaying error messages on the console typewriter.
9. Providing rerun points. Rerun points between sort passes or between sorting cycles for multireel sorts are provided.

Merge

The *Merge* capabilities are available as follows:

1. Merging from two to 10 data files originating on two or more magnetic tape reels.
2. Processing fixed and variable-size records.
3. Accommodating Spectra 70 Systems standard fixed and variable-data formats.
4. Handling up to 10 sequencing keys. Sequencing keys may be specified as alphanumeric or numeric and may be ascending or descending.
5. Providing last pass own coding options.
6. Accommodating alternate tape units.
7. Accepting merge specifications and own coding, if any, in standard basic assembly language.
8. Displaying error messages on the Console Typewriter.
9. Providing rerun points after each output tape of a merge.

PERIPHERAL CONTROL SYSTEM

The *Peripheral Control System* is a single program which consists of several independent input-output processes. Each of these independent processes is a unique routine, such as tape-to-printer and card-to-tape.

Execution of more than one of these independent processes can occur simultaneously. The execution of these different processes is coordinated by the Peripheral Control System. Therefore, it is possible to have more than one utility function proceeding at the same time for maximum utilization of the available input-output devices.

The Peripheral Control System is designed such that the only utility routines in memory are those required to perform current tasks. For instance, the tape-to-printer routine would not occupy core storage unless a tape-to-printer task needed to to be performed.

The Peripheral Control System allows the user to substitute a utility routine of his own for the corresponding standard process and have the Peripheral Control System coordinate the execution of his routine with any others which may be required.

COMMUNICATION CONTROL SYSTEM

A *Communication Control System* is provided to control single-channel communications lines, utilizing the Model 70/653 Communication Control (Single-Channel).

Routines included in the Communications Control system are provided in the areas of:

1. Line and termination control.
2. Message control consisting of logging, queuing, code translating, and sequence numbering.

Error checking and re-transmisions (where necessary) are performed by the Communications Control routines.

SYSTEM LIBRARY MAINTENANCE ROUTINES

The 70/45-55 Operating Systems contain four System Library Maintenance routines which are used to produce executable machine-coded programs; and, in addition, generate and update system libraries. The system routines are as follows:

1. Program Section Library Insert
2. Program Section Library Update
3. Load Bind
4. Load Library Update

Program section libraries contain an index which defines all of the calling relationships among program sections contained in the library. Replacement and deletion of routines from a program section library require a complete reconstruction of the library's index. Inserting routines requires only the appendage of a new set of index entries to the library's index. The Program Section Library Insert routine allows rapid addition of new routines to a program section library. The Program Section Library Update routine includes all of the functions needed to produce a new program section library from a pre-existing one.

Program Section Library Insert Routine

The Program Section Library Insert routine constructs a new program section library. This routine provides the facility for making rapid additions to a program section library and uses a major and a minor input program section library. The output from this run is a new program section library.

Program Section Library Update Routine

The Program Section Library Update routine provides program section replacement, deletion, and insertion for changing the set of program sections contained in a program section library. This update routine acts on a program section library that is to be updated and on one containing replacement sections and additional program sections. Additional input is set of control cards specifying the operations that are to be performed. The output is a new program section library.

Load Bind Routine

The Load Bind routine acts on a program section library containing sets of program sections. The members of each set are related to each other by reference calls. The Load Bind routine constructs a load from each such set. The loads include any standard program sections referenced by members of the set. The standard program sections are obtained from the installation program section library which is used as a second input to the Load Bind routine. The output of the Load Bind routine is a load library containing one load for each input set of program sections.

Load Library Update Routine

The Load Library Update routine contains three options:

1. To bind a set of routines and to insert the resulting loads into the output load library.
2. To automatically correct a load library.
3. To generate a load library containing a selected set of loads from the master load library.

Note: Options 1 and 2 may be used together.

The binding option acts on a program section library containing all of the program sections required by a program. It carries out reference-call binding and constructs a set of loads from the program section library elements. A load library is used as another input to the binding option. The output is a new load library which includes the newly constructed loads. Loads can also be deleted from a load library in the bind option.

The automatic correction option may be used by itself or together with the bind option. It acts on a load library under control of a set of correction specification cards to update loads made from old versions of corrected program sections. The output is a corrected load library.

The option to create a selected set of loads from the master load library requires as input a set of control cards indicating which loads are to be selected and a load library. The output is a selected load library.

COMPATIBILITY SUPPORT SYSTEM

Compatibility between the 70/25 and 70/45-55 Systems is provided by the Compatibility Support System. This system provides a group of aids for preparing 70/25 programs for conversion to 70/45-55 programs. After conversion, these 70/25 programs operate without restrictions on the 70/45-55 Systems.

RCA 70/45-55 Tape Operating System 32

The RCA 70/45-55 Tape Operating System 32, a magnetic tape-oriented programming system, provides for the efficient operation of a processor equipped with a minimum high-speed memory of 32K bytes and a standard order code. A console typewriter is required and other optional features and equipment are utilized if available.

A complete list of the Tape Operating System 32 components is as follows:

Executive
Monitor
Basic Assembly System
Extended Assembly System
File Control Processor (FCP)
Report Program Generator
COBOL
FORTRAN
Sort/Merge
Peripheral Control System
Communication Control System (Single-Channel)
System Library Maintenance Routine
Random Access File Maintenance Routine
Compatibility Support System

All of the components of the RCA 70/45-55 Tape Operating System 32 are identical to the RCA 70/45-55 Tape Operating System 16 components with the exception of the Executive and File Control Processor. In addition, the Extended Assembly System and Random Access File Maintenance routines are provided with the 70/45-55 Tape Operating System 32.

THE EXECUTIVE

The *Executive* in the Tape Operating System 32 provides all of the capabilities of the Tape Operating System 16 Executive. (See page 56.) In addition, it provides multiprogramming facility for two or three independent programs to utilize the processor simultaneously. Any one of these programs may be running in either a Monitored or Production mode of operation. Also, the Executive has the facility for controlling programs that utilize random-access files as data devices. However, only one of the three programs may be of this type.

The programs are executed on a priority basis. The priorities are assigned by the user and programs maintain the same priority throughout their execution. Programs being executed together must have different priorities.

EXTENDED ASSEMBLY SYSTEM

An additional and more powerful assembly system is provided with the 70/45-55 Tape Operating System 32, the Extended Assembly System. The basic assembly language is a subset of the extended assembly language. Enhancements are in two areas:

1. An expanded facility is provided for data definitions particularly with respect to literals and control of externally defined storage.
2. A powerful generative procedural facility is included in the language. This facility includes the ability to generate code conditionally at assembly time with assembler output under control of program-defined format directives.

   The generative macro language provides an alternative to the programmer who cannot express the solution to his problem concisely in one of the standard source code languages such as COBOL or FORTRAN; and, wishes a generalization of procedure beyond that in a "one-for-one" machine-oriented assembler. The extended assembly language is a powerful tool that permits the expression and utilization of application-oriented languages by the programmer.

FILE CONTROL PROCESSOR

The *File Control Processor* for the Tape Operating System 32 provides all the capabilities of the Tape Operating System 16 File Control Processor. (See page 56.) In addition, it provides input-output control for programs utilizing random access files as data devices.

RANDOM ACCESS FILE MAINTENANCE ROUTINES

The *Random Access File Maintenance* routines provide the user with a facility for maintaining an effective file organization through the use of special file loading, dumping, and file revision functions.

File Loading — provision is made for initial file loading, file re-loading, and file re-allocation.

File Dumping — provision is made for dumping an entire random access storage device or selected files onto a backup medium.

File Maintenance — provision is made for maintaining files on the random access equipment. The file maintenance functions are:

Insertion
Deletion
Correction of records within a file.

RCA 70/45-55 Tape Operating System 65

The RCA 70/45-55 Tape Operating System 65 is a magnetic tape-oriented programming system which provides for efficient operation of a processor equipped with a minimum high-speed memory of 65K bytes. A console typewriter is required and other optional features and equipment are utilized if available.

A complete list of the Tape Operating System 65 components is as follows:

Executive
Monitor
Basic Assembly System
Extended Assembly System
File Control Processor (FCP)
Report Program Generator
COBOL
FORTRAN
Sort/Merge
Peripheral Control System
Communication Control System (Single-Channel)
System Library Maintenance Routines
Random Access File Maintenance Routines
Compatibility Support System

All of the components of the RCA 70/45-55 Tape Operating System 65 are identical to the RCA 70/45-55 Tape Operating System 32 components with the exception of the COBOL and FORTRAN compilers.

COBOL

The *COBOL* compiler provided with the 70/45-55 Tape Operating System 65 has all the capabilities of the 70/45-55 Tape Operating System 16 COBOL described previously. In addition, the Tape Operating System 65 COBOL makes maximum use of 65K-byte and larger memories, thus, providing faster compilation time and greater optimization of object code. This compiler includes extension such as:

1. Sort
2. Report Writer
3. Improved Indexing Capability
4. Random Access Input-Output

FORTRAN

The *FORTRAN* compiler implemented in the Tape Operating System 65 is FORTRAN IV. In addition to all the capabilities of the Tape Operating System 16 FORTRAN compiler described previously, the Tape Operating System 65 FORTRAN has the following features:

1. Logical constant definition
2. Double precision constant definition
3. Complex constant definition
4. Logical expressions
5. Data specification statements
6. Labeled common statements

RCA 70/45-55 Disc Operating System 65

The RCA 70/45-55 Disc Operating System 65 provides the user with a complete set of programming components specifically designed to take advantage of 65K-byte and larger memories, and a random-access operating environment. Significantly, the random-access orientation of the system provides facilities required for controlling large real-time communications systems. The Model 70/564 Disc Storage Unit has been designated as the prime program storage and operating media. The Model 70/565 Drum Memory Unit may be used to complement the operating system. A console typewriter is required and other optional features and equipment are utilized if available.

A complete list of the Disc Operating System 65 components is as follows:

Executive
Monitor
Extended Assembly System
File Control Processor (FCP)
Report Program Generator
COBOL
FORTRAN
Sort/Merge
Peripheral Control System
Communication Control System (Multichannel)
System Library Maintenance Routines
Random Access File Maintenance Routines

All of the Disc Operating System 65 components are identical in function to the Tape Operating System 65 components except for the following: Communication Control System (Multichannel) and System Library Maintenance Routines.

COMMUNICATION CONTROL SYSTEM (Multichannel)

The *Communication Control System* (Multichannel) provides the facilities of the single-channel system, services, and controls multiple communications devices with varying transfer rates. The system utilizes the Model 70/664 Communication Buffer Control with the Model 70/672 Communication Multiplexor Channel as well as the Model 70/653 Communication Control Single Channel.

The Communication Control System allows the user to concern himself little, if at all, with the control of the flow of the communication traffic

in and out of his system. Error detection is provided, with re-transmission of erroneous messages under the control of the communications packages. User-selectable routines for unique communications functions such as calling and polling, message queuing, journalizing, code translating, etc. are furnished.

SYSTEM LIBRARY MAINTENANCE ROUTINES

The *Systems Library Maintenance* routines are identical in function to the system library maintenance routines described in the Tape Operating System 65 (see page 60) except that the load bind function is performed by the loader in the Disc Operating System.

RCA 70/45-55 Disc Operating System 262

The RCA 70/45-55 Disc Operating System 262 is a random-access oriented operating system which provides for efficient operation of a processor with a minimum of 262K-byte memory and a standard order code. A console typewriter and the timer and protection options are required for system operation. Other optional features and equipment are utilized if available. The Model 70/564 Disc Storage Unit has been designated as the prime program storage and operating media. The Model 70/565 Drum Memory Unit may be used to complement the operating system.

The following is a complete list of the Disc Operating System 262 components:

Executive
Monitor
Extended Assembly System
File Control Processor (FCP)
Report Program Generator
COBOL
FORTRAN
Sort/Merge
Peripheral Control System
Communication Control System (Multichannel)
System Library Maintenance Routines
Random Access File Maintenance Routines

All Disc Operating System 65 components are applicable to the Disc Operating System 262 except for the Executive and Monitor components. The Disc Operating System 262 removes the limitations inherent in the Disc Operating System 65. It provides increased accessibility to computer facilities and minimizes turnaround time for time sensitive applications.

The Disc Operating System 262 increases computer accessibility by offering facilities for:

1. Accepting internally a large number of job requests, holding the accumulated requests and sequencing them for execution on a time dependent priority basis.
2. Accepting job requests from a large number of remote terminals and integrating such requests in the internal request queues.
3. Providing output to both local and remote terminals.

Turnaround time for time-sensitive jobs is minimized by offering facilities for:

1. Selecting jobs for execution on a time-dependent priority basis.
2. Sharing the total set of available computer facilities amongst a number of jobs, each of which requires only some of the available facilities.
3. Providing multiprocessing to make more than one computer complex available for processing the total work load.

The Role of the Executive

The *Executive* undertakes the management and supervision of the entire system. It provides the basic control and interconnection required between the user's program and the operating system as well as between the various components of the operating system. All input-output initiations and their resulting termination interrupts and any other interrupts, such as a divide error, require action on the part of the Executive. The user's program must be able to communicate with the Executive as to what actions are required to correctly process his program. To accomplish this, the user's programs must observe certain conventions with respect to their structure for proper communication with the Executive.

Executive Information Area

A user's program must include unique interrupt-response codes for the set of interrupts directly under user program control. These include various contingency conditions such as overflow and divide errors. The starting addresses of these contingency response operations must be defined in the user's program. User's programs must also include a memory storage area for all of the registers directly related to it. These are the General-Purpose registers which the program uses and whose functions are described below. Contingency starting address and register storage areas are

provided within a program in the Executive information area. The Executive information area must be included in every program and it must be located at the beginning of a program's initial load.

Input-Output Determined Program Structure

Input-output terminations are indicated in the 70/45-55 Systems by processor interrupts. All programs must include response codes for these interrupts. Interrupt-response code is supplied by RCA in its FCP; however, the Executive does not distinguish user-produced code from RCA-supplied code at the time a program is executed. Programs are structured into sets of main-chain and interrupt-response operations. Main-chain operations are the computational operations which do not depend on an input-output interrupt for their initiation. Interrupt-response operations carry out the functions required in response to an input-output termination interrupt.

The Executive makes 32 General-Purpose registers available to each user program. Sixteen registers are available for use by main-chain operations and 16 registers are available for use by interrupt-response operations. Main-chain and interrupt-response operations do not have direct access to each others' General-Purpose registers and cannot communicate with each other through the registers. Storage areas must be provided for these General-Purpose registers in the Executive information area.

Programming Input-Output Operations

INPUT-OUTPUT PROCESSES

An input-output operation is initiated by executing an input-output instruction. Termination of the defined input-output operation is indicated to the system by an interrupt. When this interrupt occurs, the status information associated with the termination is passed along to the interrupt-response code which checks for errors, etc. If certain standard types of errors are encountered, the interrupt-response code can request the Executive to perform standard retry procedures.

THE FUNCTION OF THE EXECUTIVE IN INPUT-OUTPUT OPERATIONS

The Executive issues all start input-output instructions and routes input-output interrupts to the pertinent interrupt-response operation. A user's program requiring the initiation of an input-output operation issues an input-output Request Supervisor Call to the Executive. Along with the Supervisor Call the user specifies a symbolic channel-device name, the location of a Channel Command Word (CCW) chain, and the starting address of the pertinent interrupt-response operation. Input-output request coding is supplied by RCA in its FCP. FCP coding is incorporated into the user's program prior to the time of execution. Input-output request coding is viewed by the Executive as the user's program coding even though it was, in fact, supplied by RCA in its FCP.

The Executive accepts the input-output request, returns control immediately to the requesting program and issues the start input-output as soon as the specified channel and device are available. When the termination interrupt occurs the Executive sets up an entry to the interrupt-response operation at the address which was specified by the input-output requester. Interrupt-response operations release control and relinquish their priority when the response functions have been completed by issuing a Priority Relinquish Supervisor Call to the Executive. The Priority Relinquish Supervisor Call notifies the Executive that system control is available to any operation. The Executive will return control to a program's main-chain after all its outstanding input-output termination interrupts have been processed. Figure 13 shows the control flow between the user's program and the Executive during an input-output operation.

THE FORM OF AN INPUT-OUTPUT REQUEST

A program issuing an Input-Output Request Supervisor Call on the Executive must use a standard format as follows:

1. Input-Output Request Supervisor Call.
2. Symbolic channel-device name.
3. Location of Channel Command Word (CCW) chain.
4. Address for return of control to requestor.
5. Address of interrupt-response operation.

FCP coding supplied by RCA issues input-output requests in this form. This coding is viewed by the Executive as user-program coding.

Executive Operations

Certain major functions are made available to all users by including them as operations within the Executive. Console control, for example, is not part of the Executive mechanism required for input-output handling, interrupt routing, and multiprogram priority scheduling. (These latter mechanisms are required for the system to operate during any phase of program execution.) Console control, on the other hand, is not required during program execution unless some communication via the console occurs or is required. Although, not necessarily required for program

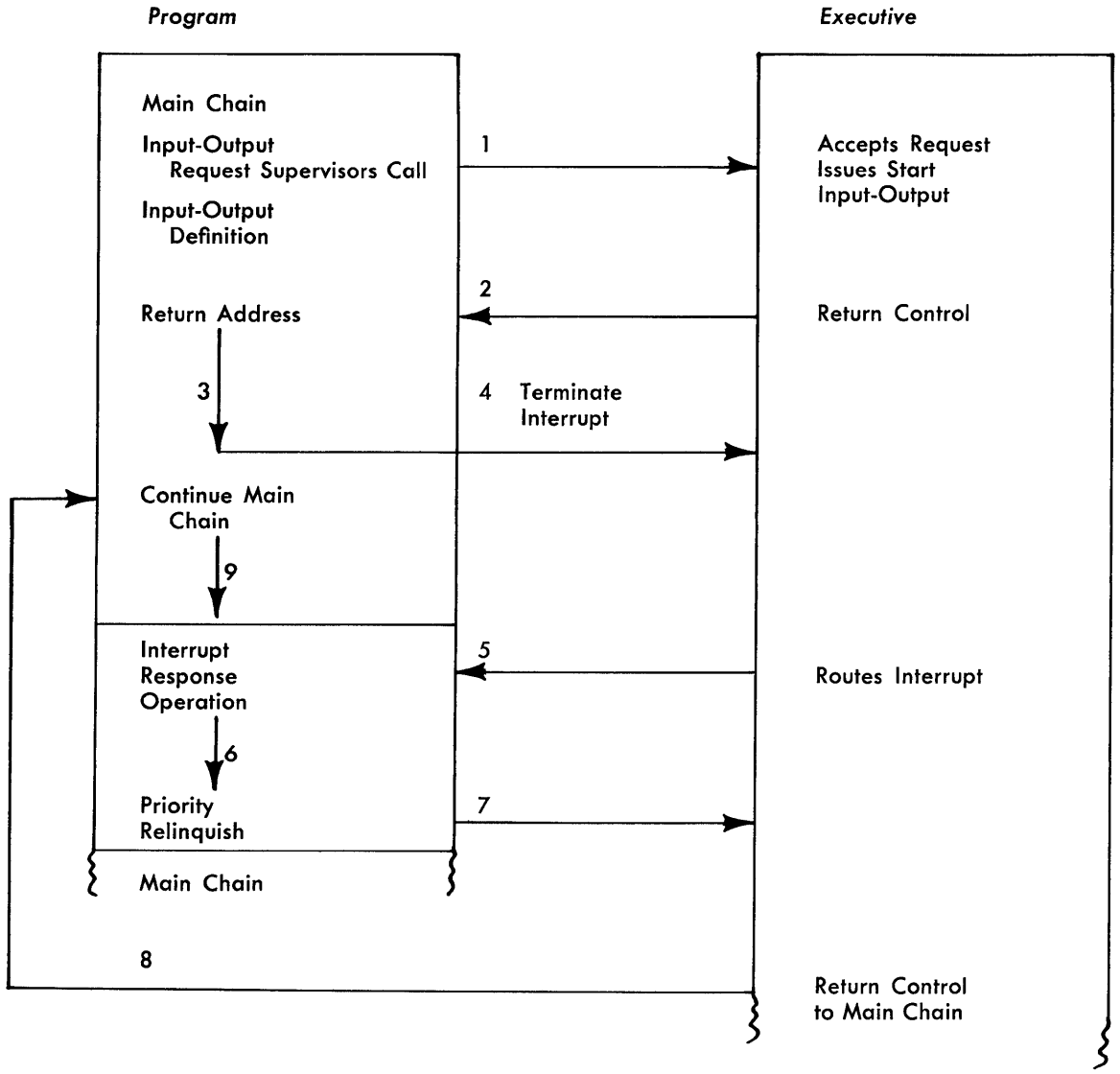

Figure 13. Control Flow During an Input-Output Operation

execution, many programs do need access to the console typewriter. And, in addition, the console typewriter must always be available to the machine operator as a communication path to the system Executive. For reasons such as these, certain operations are included in the Executive. Operations used to initiate, to load and terminate programs, to provide console communication, to provide facilities for restart and certain classes of error recovery are implemented as executive operations.

CALLING AN EXECUTIVE OPERATION

In general, a program's means of access to the Executive is a Supervisor Call. A class of Supervisor Call is provided for initiating the execution of Executive operations. Each of these Supervisor Calls results in the execution of a particular Executive operation. A Supervisor Call to an Executive operation must include certain information in the following format:

1. Supervisor Call
2. Message Length
3. Operation Accepted Return Address
4. Operation Completed Return Address
5. Message

The *Supervisor Call* defines the desired Executive operation and alerts the Executive to the request by causing an identifiable interrupt.

Message Length defines the length in bytes of the message and hence the length in bytes of the whole Supervisor Call information set.

The *Operation Accepted Return Address* defines the location in the calling program to which control is to be returned after an entry to the Executive operation has been set up and queued.

The *Operation Completed Return Address* defines the location in the calling program to which control is to be returned after the Executive operation is completed. Control will normally be returned to the calling program at the acceptance address before the Executive operation is completed. But, whether this is so or not, control will always be given to the caller's acceptance return address before it is given to the operation completed return address.

The *Message* contains any information that the caller is transmitting to the Executive operation. For example, if a program is calling on the console control operation to carry out a typeout, the message is that message to be typed out.

Register Preservation in Multiprogrammed System Operation

Register usage conflicts do not normally occur when a single program is running by itself on the computer. Conflicts are eliminated since every program is provided with two separate sets of registers, one for its main-chain operations and one for its interrupt-response operations.

A set of General-Purpose registers may have been used last by one program when the Executive determines that control is to be given to another program which uses the same set of registers. In this case, the Executive first stores the old program's registers in its Executive information area. Next, the new program's registers are loaded from its Executive information area. Finally, after register storing and reloading, the Executive gives control to the next program.

APPENDIX A
INPUT-OUTPUT TIMING SUMMARY

Buffers:

Devices[1]	Model Number	Data Rate	Code Level
Telegraph Buffer	70/710	45.5, 50, 56.8 and 75 BPS[2]	5 or 6
Communication Buffer	70/720	75, 110, 134.4, 148 and 180 BPS	7 or 8
Communication Buffer	70/721	1,050 BPS up to 1,800 BPS	8
Communication Buffer	70/722	2,000 BPS and 2,400 BPS	7, 8 or 9
Autodin Buffer	70/723	1,200 BPS 2,400 BPS 4,800 BPS	8

NOTES:
1. All Buffers are housed within and connected to the Communication Buffer Control.
2. BPS — bits per second.

Data Exchange and Communications Controls:

Device	Model Number	Data Rate
Data Exchange Control	70/627	Speed is dependent upon the channel and the processor activity at the time of transmission.
Communication Control	70/652-25, -26	2,000 BPS 2,400 BPS
Communication Control	70/653-25, -26	2,000 BPS 2,400 BPS
Communication Control	70/653-34	40,800 BPS

Peripherals:

Device	Model Number	Data Rate
Interrogating Typewriter	70/214	10 cps
Interrogating Typewriter	70/216	10 cps
Paper Tape Reader/Punch	70/221	200 cps Read 100 cps Punch
Card Punch	70/234	100 cpm
Card Punch	70/236	300 cpm

Device	Model Number	Data Rate
Card Reader	70/237	1,435 cpm
Medium-Speed Printer	70/242	600 lpm
High-Speed Printer	70/243	1,250 lpm
Bill-Feed Printer	70/249	600 lpm Forms 800 cpm Cards
Videoscan Document Reader	70/251	1,300 dpm

Legend:
cps — characters per second.
cpm — cards per minute.
lpm — lines per minute.
dpm — documents per minute.

Random-Access Devices:

Device	Model Number	Unit Capacity	Data Rate	Average Access
Disc Storage Unit	70/564	7.25 million bytes	156 KB	97.5 mil.
Drum Memory Unit	70/565	1 million bytes	117 KB	8.6 mil.

APPENDIX A (Cont.)

INPUT-OUTPUT TIMING SUMMARY

Magnetic Tape Units:

Model Number	Data Rate		Recording Density		Tape Speed	Gap Size	Rewind Speed	Tape Controller Required
	9 Track	7 Track	9 Track	7 Track				
70/432-1	30 KB 60 KD	7.5 KC 20.8 KC 30 KC	800 BPI	200 BPI 556 800	37.5 IPS	.6 in. (9-track) .75 in. (7-track)	100 IPS	70/472-108 70/472-116
70/432-2	Same performance characteristics as 70/432-1							70/472-208 70/472-216
70/442-1	60 KB 120 KD	15 KC 41.7 KC 60 KC	800 BPI	200 BPI 566 800	75 IPS	.6 in. (9-track) .75 in. (7-track)	150 IPS	70/472-108 70/472-116
70/442-2	Same performance characteristics as 70/442-1							70/472-208 70/472-216
70/445-1	120 KB 240 KD	30 KC 834 KC 120 KC	800 BPI	200 BPI 566 800	150 IPS	.6 in. Read .65 in. Written (9-track) .75 in. Read .8 in. Written (7-track)	300 IPS	70/472-108 70/472-116
70/445-2	Same performance characteristics as 70/445-1							70/472-208 70/472-216

Legend:
BPI — bytes per inch.
IPS — inches per second.
KB — thousand bytes per second.
KD — thousand 4-bit digits per second
KC — thousand 7-bit characters per second.
Different speed tape units may be intermixed with a single tape controller.

APPENDIX B

EXTENDED BINARY-CODED-DECIMAL INTERCHANGE CODE (EBCDIC)

BIT POSITIONS→ 76 / 54 / 3210	00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
0000					SP	&	—									0
0001							/		a	j			A	J		1
0010									b	k	s		B	K	S	2
0011									c	l	t		C	L	T	3
0100	PF	RE	BY	PN					d	m	u		D	M	U	4
0101	HT	NL	LF	RS					e	n	v		E	N	V	5
0110	LC	BS	EB	UC					f	o	w		F	O	W	6
0111	DL	IL	PR	ET					g	p	x		G	P	X	7
1000									h	q	y		H	Q	Y	8
1001									i	r	z		I	R	Z	9
1010			SM		¢	!		:								
1011					.	$	,	#								
1100					<	*	%	@								
1101					(	)	—	'								
1110					+	;	>	=								
1111					|	¬	?	"								

BIT POSITIONS: 76543210

Control Characters:

PF — Punch Off
HT — Horizontal Tab
LC — Lower Case
DL — Delete
RE — Restore
NL — New Line
BS — Backspace
IL — Idle
BY — Bypass
LF — Line Feed
EB — End of Block
PR — Prefix
PN — Punch On
RS — Reader Stop
UC — Upper Case
ET — End of Transmission
SM — Set Mode
SP — Space

APPENDIX C

AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE
(Extended to 8 Bit)

BIT POSITIONS→ 76	00				01				10				11			
54 →	00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
3210																
0000	NULL	DLE			SP	0	SP	SP			⁄⁄	P				p
0001	SOH	DC1			!	1					A	Q			a	q
0010	STX	DC2			"	2					B	R			b	r
0011	ETX	DC3			#	3					C	S			c	s
0100	EOT	DC4			$	4					D	T			d	t
0101	ENQ	NACK			%	5					E	U			e	u
0110	ACK	SYNC			&	6					F	V			f	v
0111	BELL	ETB			'	7					G	W			g	w
1000	BS	CNCL			(	8					H	X			h	x
1001	HT	EM			)	9					I	Y			i	y
1010	LF	SS			*	:					J	Z			j	z
1011	VT	ESC			+	;					K	[			k	{
1100	FF	FS			,	<					L				l	|
1101	CR	GS			–	=					M	]			m	}
1110	SO	RS			.	>					N	^			n	~
1111	SI	US			/	?					O	\			o	DEL

BIT POSITIONS: 76543210

Control Characters:

NULL — Null/Idle
SOH — Start of Heading (CC)
STX — Start of Text (CC)
ETX — End of Text (CC)
EOT — End of Transmission (CC)
ENQ — Enquiry (CC)
ACK — Acknowledge (CC)
BELL — Audible or attention signal
BS — Backspace (FE)
HT — Horizontal Tabulation (punch card skip) (FE)
LF — Line Feed (FE)
VT — Vertical Tabulation (FE)
FF — Form Feed (FE)
CR — Carriage Return (FE)
SO — Shift Out
SI — Shift In

DLE — Data Link Escape (CC)
DC1
DC2 — Device Controls
DC3
DC4 — Device Control (stop)
NACK — Negative Acknowledge (CC)
SYNC — Synchronous Idle (CC)
ETB — End of Transmission Block (CC)
CNCL — Cancel
EM — End of Medium
SS — Start of Special Sequence
ESC — Escape
FS — File Separator (IS)
GS — Group Separator (IS)
RS — Record Separator (IS)
US — Unit Separator (IS)
DEL — Delete

APPENDIX D
OPTICAL CHARACTER CODE

Following are the RCA N-2 characters which can be read by the 70/251 :

Name	N-2 Char.	Encoded As	Hexadec. Equiv.	Bit Configuration $2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0$
Zero	0	0	F0	1 1 1 1 0 0 0 0
One	1	1	F1	1 1 1 1 0 0 0 1
Two	2	2	F2	1 1 1 1 0 0 1 0
Three	3	3	F3	1 1 1 1 0 0 1 1
Four	4	4	F4	1 1 1 1 0 1 0 0
Five	5	5	F5	1 1 1 1 0 1 0 1
Six	6	6	F6	1 1 1 1 0 1 1 0
Seven	7	7	F7	1 1 1 1 0 1 1 1
Eight	8	8	F8	1 1 1 1 1 0 0 0
Nine	9	9	F9	1 1 1 1 1 0 0 1
Period	.	.	4B	0 1 0 0 1 0 1 1
Dash	-	-	60	0 1 1 0 0 0 0 0
Dollars	$	$	5B	0 1 0 1 1 0 1 1
Asterisk	*	*	5C	0 1 0 1 1 1 0 0
Long Vertical Mark	|	@	7C	0 1 1 1 1 1 0 0
Blank	(Blank)		40	0 1 0 0 0 0 0 0
Unreadable	(Unreadable) Elective		FF	1 1 1 1 1 1 1 1

Any number of blank positions following recognition of a character will be encoded as a single blank.

APPENDIX E
PAPER TAPE CODES

EBCDIC Code	EBCDIC Graphic	Paper Tape Code	EBCDIC Code	EBCDIC Graphic	Paper Tape Code
1100 0001	A	1000 0001	1111 1001	9	1111 1001
1100 0010	B	1000 0010	0100 0000	Space	1100 0000
1100 0011	C	1100 0011	0100 1001		0000 1001
1100 0100	D	1000 0100	0100 1010	¢ (cents)	0000 1010
1100 0101	E	1100 0101	0100 1011	. (period)	0100 1011
1100 0110	F	1100 0110	0100 1100	< (less than)	0000 1100
1100 0111	G	1000 0111	0100 1101	((left parenthesis)	0100 1101
1100 1000	H	1000 1000	0100 1110	+ (plus)	0100 1110
1100 1001	I	1100 1001	0100 1111	| (vertical)	0000 1111
1101 0001	J	1101 0001	0101 0000	& (ampersand)	0101 0000
1101 0010	K	1101 0010	0101 1010	! (exclamation)	0101 1010
1101 0011	L	1001 0011	0101 1011	$ (dollars)	0001 1011
1101 0100	M	1101 0100	0101 1100	* (asterisk)	0101 1100
1101 0101	N	1001 0101	0101 1101	) (right parenthesis)	0001 1101
1101 0110	O	1001 0110	0101 1110	; (semicolon)	0001 1110
1101 0111	P	1101 0111	0101 1111	¬ (not)	0101 1111
1101 1000	Q	1101 1000	0110 0000	— (minus or dash)	0110 0000
1101 1001	R	1001 1001	0110 0001	/ (virgule or slash)	0010 0001
1110 0010	S	1110 0010	0110 1001		0110 1001
1110 0011	T	1010 0011	0110 1011	, (comma)	0010 1011
1110 0100	U	1110 0100	0110 1100	% (percent)	0110 1100
1110 0101	V	1010 0101	0110 1101	— (underline)	0010 1101
1110 0110	W	1010 0110	0110 1110	> (greater than)	0010 1110
1110 0111	X	1110 0111	0110 1111	? (question)	0110 1111
1110 1000	Y	1110 1000	0111 1001		0011 1001
1110 1001	Z	1010 1001	0111 1010	: (colon)	0011 1010
1111 0000	0 (zero)	1111 0000	0111 1011	# (number)	0111 1011
1111 0001	1	1011 0001	0111 1100	@ (at the rate of)	0011 1100
1111 0010	2	1011 0010	0111 1101	' (apostrophe)	0111 1101
1111 0011	3	1111 0011	0111 1110	= (equals)	0111 1110
1111 0100	4	1011 0100	0111 1111	" (quote)	0011 1111
1111 0101	5	1111 0101	1110 0000	Blank	1010 0000
1111 0110	6	1111 0110	0000 0000	gap.	0000 0000
1111 0111	7	1011 0111	0110 1010	(logical and)	0110 1010
1111 1000	8	1011 1000			

APPENDIX F

CONSOLE TYPEWRITER CODE

Symbol	EBCDIC	Teletype	Symbol	EBCDIC	Teletype	
A	1100 0001	1100 0001	9	1111 1001	1011 1001	
B	1100 0010	1100 0010	□	1111 1111	0111 1111	Same as "
C	1100 0011	1100 0011	END	— — —	0000 0100	
D	1100 0100	1100 0100	ERROR	— — — —	0000 0010	
E	1100 0101	1100 0101	TOSL	XXXX 0101	0000 0111	Bell
F	1100 0110	1100 0110	CR. LF	0000 1101	0000 1101	
G	1100 0111	1100 0111	¢	0100 1010	0100 1010	
H	1100 1000	1100 1000	.	0100 1011	0100 1011	
I	1100 1001	1100 1001	<	0100 1100	0100 1100	
J	1101 0001	1101 0001	(	0100 1101	0100 1101	
K	1101 0010	1101 0010	+	0100 1110	0100 1110	
L	1101 0011	1101 0011	⁄m	0100 1111	0100 1111	
M	1101 0100	1101 0100	!	0101 1010	0101 1010	
N	1101 0101	1101 0101	$	0101 1011	0101 1011	
O	1101 0110	1101 0110	*	0101 1100	0101 1100	
P	1101 0111	1101 0111	)	0101 1101	0101 1101	
Q	1101 1000	1101 1000	;	0101 1110	0101 1110	
R	1101 1001	1101 1001	¬	0101 1111	0101 1111	
S	1110 0010	1010 0010	,	0110 1011	0010 1011	comma
T	1110 0011	1010 0011	%	0110 1100	0010 1100	
U	1110 0100	1010 0100	?	0110 1111	0010 1111	
V	1110 0101	1010 0101	:	0111 1010	0011 1010	
W	1110 0110	1010 0110	#	0111 1011	0011 1011	
X	1110 0111	1010 0111	@	0111 1100	0011 1100	
Y	1110 1000	1010 1000	'	0111 1101	0011 1101	apostrophe
Z	1110 1001	1010 1001	=	0111 1110	0011 1110	equal
0	1111 0000	1011 0000	"	0111 1111	0011 1111	
1	1111 0001	1011 0001	Space	0100 0000	0010 0000	
2	1111 0010	1011 0010	—	0110 0000	0100 0000	
3	1111 0011	1011 0011	/	0110 0001	0010 0001	
4	1111 0100	1011 0100	&	0101 0000	0101 0000	
5	1111 0101	1011 0101	—	0110 1101	0010 1101	underscore
6	1111 0110	1011 0110	>	0110 1110	0010 1110	
7	1111 0111	1011 0111	^	0110 1010	0010 1010	
8	1111 1000	1011 1000				

APPENDIX G

CHARACTER CODE TABLE

8-BIT BCD CODE	CHARACTER SET PUNCH COMBINATION	PRINTER GRAPHICS	DECIMAL	HEXADECIMAL
00000000	12,0,9,8,1		0	00
00000001	12,9,1		1	01
00000010	12,9,2		2	02
00000011	12,9,3		3	03
00000100	12,9,4		4	04
00000101	12,9,5		5	05
00000110	12,9,6		6	06
00000111	12,9,7		7	07
00001000	12,9,8		8	08
00001001	12,9,8,1		9	09
00001010	12,9,8,2		10	0A
00001011	12,9,8,3		11	0B
00001100	12,9,8,4		12	0C
00001101	12,9,8,5		13	0D
00001110	12,9,8,6		14	0E
00001111	12,9,8,7		15	0F
00010000	12,11,9,8,1		16	10
00010001	11,9,1		17	11
00010010	11,9,2		18	12
00010011	11,9,3		19	13
00010100	11,9,4		20	14
00010101	11,9,5		21	15
00010110	11,9,6		22	16
00010111	11,9,7		23	17
00011000	11,9,8		24	18
00011001	11,9,8,1		25	19
00011010	11,9,8,2		26	1A
00011011	11,9,8,3		27	1B
00011100	11,9,8,4		28	1C
00011101	11,9,8,5		29	1D
00011110	11,9,8,6		30	1E
00011111	11,9,8,7		31	1F
00100000	11,0,9,8,1		32	20
00100001	0,9,1		33	21
00100010	0,9,2		34	22
00100011	0,9,3		35	23
00100100	0,9,4		36	24
00100101	0,9,5		37	25
00100110	0,9,6		38	26
00100111	0,9,7		39	27
00101000	0,9,8		40	28
00101001	0,9,8,1		41	29
00101010	0,9,8,2		42	2A
00101011	0,9,8,3		43	2B
00101100	0,9,8,4		44	2C
00101101	0,9,8,5		45	2D
00101110	0,9,8,6		46	2E
00101111	0,9,8,7		47	2F
00110000	12,11,0,9,8,1		48	30
00110001	9,1		49	31
00110010	9,2		50	32
00110011	9,3		51	33
00110100	9,4		52	34
00110101	9,5		53	35
00110110	9,6		54	36
00110111	9,7		55	37
00111000	9,8		56	38
00111001	9,8,1		57	39

APPENDIX G

CHARACTER CODE TABLE (Cont.)

8-BIT BCD CODE	CHARACTER SET PUNCH COMBINATION	PRINTER GRAPHICS	DECIMAL	HEXADECIMAL
00111010	9,8,2		58	3A
00111011	9,8,3		59	3B
00111100	9,8,4		60	3C
00111101	9,8,5		61	3D
00111110	9,8,6		62	3E
00111111	9,8,7		63	3F
01000000		space	64	40
01000001	12,0,9,1		65	41
01000010	12,0,9,2		66	42
01000011	12,0,9,3		67	43
01000100	12,0,9,4		68	44
01000101	12,0,9,5		69	45
01000110	12,0,9,6		70	46
01000111	12,0,9,7		71	47
01001000	12,0,9,8		72	48
01001001	12,8,1		73	49
01001010	12,8,2	¢ (cents)	74	4A
01001011	12,8,3	. (period)	75	4B
01001100	12,8,4	< (less than)	76	4C
01001101	12,8,5	((left parens)	77	4D
01001110	12,8,6	+ (plus)	78	4E
01001111	12,8,7	| (stroke)	79	4F
01010000	12	& (ampersand)	80	50
01010001	12,11,9,1		81	51
01010010	12,11,9,2		82	52
01010011	12,11,9,3		83	53
01010100	12,11,9,4		84	54
01010101	12,11,9,5		85	55
01010110	12,11,9,6		86	56
01010111	12,11,9,7		87	57
01011000	12,11,9,8		88	58
01011001	11,8,1		89	59
01011010	11,8,2	! (exclamation)	90	5A
01011011	11,8,3	$ (dollar sign)	91	5B
01011100	11,8,4	* (asterisk)	92	5C
01011101	11,8,5	) (right parens)	93	5D
01011110	11,8,6	; (semicolon)	94	5E
01011111	11,8,7	¬ (logical NOT)	95	5F
01100000	11	- (minus)	96	60
01100001	0,1	/ (virgule)	97	61
01100010	11,0,9,2		98	62
01100011	11,0,9,3		99	63
01100100	11,0,9,4		100	64
01100101	11,0,9,5		101	65
01100110	11,0,9,6		102	66
01100111	11,0,9,7		103	67
01101000	11,0,9,8		104	68
01101001	0,8,1		105	69
01101010	12,11		106	6A
01101011	0,8,3	, (comma)	107	6B
01101100	0,8,4	% (percent)	108	6C
01101101	0,8,5	_ (underline)	109	6D
01101110	0,8,6	> (greater than)	110	6E
01101111	0,8,7	? (question mark)	111	6F
01110000	12,11,0		112	70
01110001	12,11,0,9,1		113	71
01110010	12,11,0,9,2		114	72
01110011	12,11,0,9,3		115	73

APPENDIX G

CHARACTER CODE TABLE (Cont.)

8-BIT BCD CODE	CHARACTER SET PUNCH COMBINATION	PRINTER GRAPHICS	DECIMAL	HEXADECIMAL
01110100	12,11,0,9,4		116	74
01110101	12,11,0,9,5		117	75
01110110	12,11,0,9,6		118	76
01110111	12,11,0,9,7		119	77
01111000	12,11,0,9,8		120	78
01111001	8,1		121	79
01111010	8,2	: (colon)	122	7A
01111011	8,3	# (pound)	123	7B
01111100	8,4	@ (at rate of)	124	7C
01111101	8,5	' (quote)	125	7D
01111110	8,6	= (equal)	126	7E
01111111	8,7	" (quotes)	127	7F
10000000	12,0,8,1		128	80
10000001	12,0,1		129	81
10000010	12,0,2		130	82
10000011	12,0,3		131	83
10000100	12,0,4		132	84
10000101	12,0,5		133	85
10000110	12,0,6		134	86
10000111	12,0,7		135	87
10001000	12,0,8		136	88
10001001	12,0,9		137	89
10001010	12,0,8,2		138	8A
10001011	12,0,8,3		139	8B
10001100	12,0,8,4		140	8C
10001101	12,0,8,5		141	8D
10001110	12,0,8,6		142	8E
10001111	12,0,8,7		143	8F
10010000	12,11,8,1		144	90
10010001	12,11,1		145	91
10010010	12,11,2		146	92
10010011	12,11,3		147	93
10010100	12,11,4		148	94
10010101	12,11,5		149	95
10010110	12,11,6		150	96
10010111	12,11,7		151	97
10011000	12,11,8		152	98
10011001	12,11,9		153	99
10011010	12,11,8,2		154	9A
10011011	12,11,8,3		155	9B
10011100	12,11,8,4		156	9C
10011101	12,11,8,5		157	9D
10011110	12,11,8,6		158	9E
10011111	12,11,8,7		159	9F
10100000	11,0,8,1		160	A0
10100001	11,0,1		161	A1
10100010	11,0,2		162	A2
10100011	11,0,3		163	A3
10100100	11,0,4		164	A4
10100101	11,0,5		165	A5
10100110	11,0,6		166	A6
10100111	11,0,7		167	A7
10101000	11,0,8		168	A8
10101001	11,0,9		169	A9
10101010	11,0,8,2		170	AA
10101011	11,0,8,3		171	AB
10101100	11,0,8,4		172	AC
10101101	11,0,8,5		173	AD

APPENDIX G

CHARACTER CODE TABLE (Cont.)

8-BIT BCD CODE	CHARACTER SET PUNCH COMBINATION	PRINTER GRAPHICS	DECIMAL	HEXADECIMAL
10101110	11,0,8,6		174	AE
10101111	11,0,8,7		175	AF
10110000	12,11,0,8,1		176	B0
10110001	12,11,0,1		177	B1
10110010	12,11,0,2		178	B2
10110011	12,11,0,3		179	B3
10110100	12,11,0,4		180	B4
10110101	12,11,0,5		181	B5
10110110	12,11,0,6		182	B6
10110111	12,11,0,7		183	B7
10111000	12,11,0,8		184	B8
10111001	12,11,0,9		185	B9
10111010	12,11,0,8,2		186	BA
10111011	12,11,0,8,3		187	BB
10111100	12,11,0,8,4		188	BC
10111101	12,11,0,8,5		189	BD
10111110	12,11,0,8,6		190	BE
10111111	12,11,0,8,7		191	BF
11000000	12,0		192	C0
11000001	12,1	A	193	C1
11000010	12,2	B	194	C2
11000011	12,3	C	195	C3
11000100	12,4	D	196	C4
11000101	12,5	E	197	C5
11000110	12,6	F	198	C6
11000111	12,7	G	199	C7
11001000	12,8	H	200	C8
11001001	12,9	I	201	C9
11001010	12,0,9,8,2		202	CA
11001011	12,0,9,8,3		203	CB
11001100	12,0,9,8,4		204	CC
11001101	12,0,9,8,5		205	CD
11001110	12,0,9,8,6		206	CE
11001111	12,0,9,8,7		207	CF
11010000	11,0		208	D0
11010001	11,1	J	209	D1
11010010	11,2	K	210	D2
11010011	11,3	L	211	D3
11010100	11,4	M	212	D4
11010101	11,5	N	213	D5
11010110	11,6	O	214	D6
11010111	11,7	P	215	D7
11011000	11,8	Q	216	D8
11011001	11,9	R	217	D9
11011010	12,11,9,8,2		218	DA
11011011	12,11,9,8,3		219	DB
11011100	12,11,9,8,4		220	DC
11011101	12,11,9,8,5		221	DD
11011110	12,11,9,8,6		222	DE
11011111	12,11,9,8,7		223	DF
11100000	0,8,2	Blank	224	E0
11100001	11,0,9,1		225	E1
11100010	0,2	S	226	E2
11100011	0,3	T	227	E3
11100100	0,4	U	228	E4
11100101	0,5	V	229	E5
11100110	0,6	W	230	E6
11100111	0,7	X	231	E7

APPENDIX G

CHARACTER CODE TABLE (Cont.)

8-BIT BCD CODE	CHARACTER SET PUNCH COMBINATION	PRINTER GRAPHICS	DECIMAL	HEXADECIMAL
11101000	0,8	Y	232	E8
11101001	0,9	Z	233	E9
11101010	11,0,9,8,2		234	EA
11101011	11,0,9,8,3		235	EB
11101100	11,0,9,8,4		236	EC
11101101	11,0,9,8,5		237	ED
11101110	11,0,9,8,6		238	EE
11101111	11,0,9,8,7		239	EF
11110000	0	0	240	F0
11110001	1	1	241	F1
11110010	2	2	242	F2
11110011	3	3	243	F3
11110100	4	4	244	F4
11110101	5	5	245	F5
11110110	6	6	246	F6
11110111	7	7	247	F7
11111000	8	8	248	F8
11111001	9	9	249	F9
11111010	12,11,0,9,8,2		250	FA
11111011	12,11,0,9,8,3		251	FB
11111100	12,11,0,9,8,4		252	FC
11111101	12,11,0,9,8,5		253	FD
11111110	12,11,0,9,8,6		254	FE
11111111	12,11,0,9,8,7	¤ (lozenge)	255	FF

APPENDIX H
HEXADECIMAL TABLE

Decimal (10)	Binary (2)	Hexadecimal (16)
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

APPENDIX I
POWERS OF TWO TABLE

N	2^N
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512
10	1,024
11	2,048
12	4,096
13	8,192
14	16,384
15	32,768
16	65,536
17	131,072
18	262,144
19	524,288

APPENDIX J

HEXADECIMAL-DECIMAL NUMBER CONVERSION TABLE

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	0000	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015
010	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030	0031
020	0032	0033	0034	0035	0036	0037	0038	0039	0040	0041	0042	0043	0044	0045	0046	0047
030	0048	0049	0050	0051	0052	0053	0054	0055	0056	0057	0058	0059	0060	0061	0062	0063
040	0064	0065	0066	0067	0068	0069	0070	0071	0072	0073	0074	0075	0076	0077	0078	0079
050	0080	0081	0082	0083	0084	0085	0086	0087	0088	0089	0090	0091	0092	0093	0094	0095
060	0096	0097	0098	0099	0100	0101	0102	0103	0104	0105	0106	0107	0108	0109	0110	0111
070	0112	0113	0114	0115	0116	0117	0118	0119	0120	0121	0122	0123	0124	0125	0126	0127
080	0128	0129	0130	0131	0132	0133	0134	0135	0136	0137	0138	0139	0140	0141	0142	0143
090	0144	0145	0146	0147	0148	0149	0150	0151	0152	0153	0154	0155	0156	0157	0158	0159
0A0	0160	0161	0162	0163	0164	0165	0166	0167	0168	0169	0170	0171	0172	0173	0174	0175
0B0	0176	0177	0178	0179	0180	0181	0182	0183	0184	0185	0186	0187	0188	0189	0190	0191
0C0	0192	0193	0194	0195	0196	0197	0198	0199	0200	0201	0202	0203	0204	0205	0206	0207
0D0	0208	0209	0210	0211	0212	0213	0214	0215	0216	0217	0218	0219	0220	0221	0222	0223
0E0	0224	0225	0226	0227	0228	0229	0230	0231	0232	0233	0234	0235	0236	0237	0238	0239
0F0	0240	0241	0242	0243	0244	0245	0246	0247	0248	0249	0250	0251	0252	0253	0254	0255
100	0256	0257	0258	0259	0260	0261	0262	0263	0264	0265	0266	0267	0268	0269	0270	0271
110	0272	0273	0274	0275	0276	0277	0278	0279	0280	0281	0282	0283	0284	0285	0286	0287
120	0288	0289	0290	0291	0292	0293	0294	0295	0296	0297	0298	0299	0300	0301	0302	0303
130	0304	0305	0306	0307	0308	0309	0310	0311	0312	0313	0314	0315	0316	0317	0318	0319
140	0320	0321	0322	0323	0324	0325	0326	0327	0328	0329	0330	0331	0332	0333	0334	0335
150	0336	0337	0338	0339	0340	0341	0342	0343	0344	0345	0346	0347	0348	0349	0350	0351
160	0352	0353	0354	0355	0356	0357	0358	0359	0360	0361	0362	0363	0364	0365	0366	0367
170	0368	0369	0370	0371	0372	0373	0374	0375	0376	0377	0378	0379	0380	0381	0382	0383
180	0384	0385	0386	0387	0388	0389	0390	0391	0392	0393	0394	0395	0396	0397	0398	0399
190	0400	0401	0402	0403	0404	0405	0406	0407	0408	0409	0410	0411	0412	0413	0414	0415
1A0	0416	0417	0418	0419	0420	0421	0422	0423	0424	0425	0426	0427	0428	0429	0430	0431
1B0	0432	0433	0434	0435	0436	0437	0438	0439	0440	0441	0442	0443	0444	0445	0446	0447
1C0	0448	0449	0450	0451	0452	0453	0454	0455	0456	0457	0458	0459	0460	0461	0462	0463
1D0	0464	0465	0466	0467	0468	0469	0470	0471	0472	0473	0474	0475	0476	0477	0478	0479
1E0	0480	0481	0482	0483	0484	0485	0486	0487	0488	0489	0490	0491	0492	0493	0494	0495
1F0	0496	0497	0498	0499	0500	0501	0502	0503	0504	0505	0506	0507	0508	0509	0510	0511
200	0512	0513	0514	0515	0516	0517	0518	0519	0520	0521	0522	0523	0524	0525	0526	0527
210	0528	0529	0530	0531	0532	0533	0534	0535	0536	0537	0538	0539	0540	0541	0542	0543
220	0544	0545	0546	0547	0548	0549	0550	0551	0552	0553	0554	0555	0556	0557	0558	0559
230	0560	0561	0562	0563	0564	0565	0566	0567	0568	0569	0570	0571	0572	0573	0574	0575
240	0576	0577	0578	0579	0580	0581	0582	0583	0584	0585	0586	0587	0588	0589	0590	0591
250	0592	0593	0594	0595	0596	0597	0598	0599	0600	0601	0602	0603	0604	0605	0606	0607
260	0608	0609	0610	0611	0612	0613	0614	0615	0616	0617	0618	0619	0620	0621	0622	0623
270	0624	0625	0626	0627	0628	0629	0630	0631	0632	0633	0634	0635	0636	0637	0638	0639
280	0640	0641	0642	0643	0644	0645	0646	0647	0648	0649	0650	0651	0652	0653	0654	0655
290	0656	0657	0658	0659	0660	0661	0662	0663	0664	0665	0666	0667	0668	0669	0670	0671
2A0	0672	0673	0674	0675	0676	0677	0678	0679	0680	0681	0682	0683	0684	0685	0686	0687
2B0	0688	0689	0690	0691	0692	0693	0694	0695	0696	0697	0698	0699	0700	0701	0702	0703
2C0	0704	0705	0706	0707	0708	0709	0710	0711	0712	0713	0714	0715	0716	0717	0718	0719
2D0	0720	0721	0722	0723	0724	0725	0726	0727	0728	0729	0730	0731	0732	0733	0734	0735
2E0	0736	0737	0738	0739	0740	0741	0742	0743	0744	0745	0746	0747	0748	0749	0750	0751
2F0	0752	0753	0754	0755	0756	0757	0758	0759	0760	0761	0762	0763	0764	0765	0766	0767
300	0768	0769	0770	0771	0772	0773	0774	0775	0776	0777	0778	0779	0780	0781	0782	0783
310	0784	0785	0786	0787	0788	0789	0790	0791	0792	0793	0794	0795	0796	0797	0798	0799
320	0800	0801	0802	0803	0804	0805	0806	0807	0808	0809	0810	0811	0812	0813	0814	0815
330	0816	0817	0818	0819	0820	0821	0822	0823	0824	0825	0826	0827	0828	0829	0830	0831
340	0832	0833	0834	0835	0836	0837	0838	0839	0840	0841	0842	0843	0844	0845	0846	0847
350	0848	0849	0850	0851	0852	0853	0854	0855	0856	0857	0858	0859	0860	0861	0862	0863
360	0864	0865	0866	0867	0868	0869	0870	0871	0872	0873	0874	0875	0876	0877	0878	0879
370	0880	0881	0882	0883	0884	0885	0886	0887	0888	0889	0890	0891	0892	0893	0894	0895

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HEXADECIMAL-DECIMAL NUMBER CONVERSION TABLE (Cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
380	0896	0897	0898	0899	0900	0901	0902	0903	0904	0905	0906	0907	0908	0909	0910	0911
390	0912	0913	0914	0915	0916	0917	0918	0919	0920	0921	0922	0923	0924	0925	0926	0927
3A0	0928	0929	0930	0931	0932	0933	0934	0935	0936	0937	0938	0939	0940	0941	0942	0943
3B0	0944	0945	0946	0947	0948	0949	0950	0951	0952	0953	0954	0955	0956	0957	0958	0959
3C0	0960	0961	0962	0963	0964	0965	0966	0967	0968	0969	0970	0971	0972	0973	0974	0975
3D0	0976	0977	0978	0979	0980	0981	0982	0983	0984	0985	0986	0987	0988	0989	0990	0991
3E0	0992	0993	0994	0995	0996	0997	0998	0999	1000	1001	1002	1003	1004	1005	1006	1007
3F0	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023
400	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039
410	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055
420	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071
430	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
440	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103
450	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119
460	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
470	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151
480	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167
490	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
4A0	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199
4B0	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215
4C0	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
4D0	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247
4E0	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263
4F0	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
500	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293	1294	1295
510	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
520	1312	1313	1314	1315	1316	1317	1318	1319	1320	1321	1322	1323	1324	1325	1326	1327
530	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343
540	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1357	1358	1359
550	1360	1361	1362	1363	1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375
560	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391
570	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407
580	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423
590	1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439
5A0	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455
5B0	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
5C0	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487
5D0	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503
5E0	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
5F0	1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535
600	1536	1537	1538	1539	1540	1541	1542	1543	1544	1545	1546	1547	1548	1549	1550	1551
610	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567
620	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583
630	1584	1585	1586	1587	1588	1589	1590	1591	1592	1593	1594	1595	1596	1597	1598	1599
640	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
650	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631
660	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647
670	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663
680	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675	1676	1677	1678	1679
690	1680	1681	1682	1683	1684	1685	1686	1687	1688	1689	1690	1691	1692	1693	1694	1695
6A0	1696	1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711
6B0	1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	1723	1724	1725	1726	1727
6C0	1728	1729	1730	1731	1732	1733	1734	1735	1736	1737	1738	1739	1740	1741	1742	1743
6D0	1744	1745	1746	1747	1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759
6E0	1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771	1772	1773	1774	1775
6F0	1776	1777	1778	1779	1780	1781	1782	1783	1784	1785	1786	1787	1788	1789	1790	1791

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HEXADECIMAL-DECIMAL NUMBER CONVERSION TABLE (Cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
700	1792	1793	1794	1795	1796	1797	1798	1799	1800	1801	1802	1803	1804	1805	1806	1807
710	1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819	1820	1821	1822	1823
720	1824	1825	1826	1827	1828	1829	1830	1831	1832	1833	1834	1835	1836	1837	1838	1839
730	1840	1841	1842	1843	1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855
740	1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867	1868	1869	1870	1871
750	1872	1873	1874	1875	1876	1877	1878	1879	1880	1881	1882	1883	1884	1885	1886	1887
760	1888	1889	1890	1891	1892	1893	1894	1895	1896	1897	1898	1899	1900	1901	1902	1903
770	1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915	1916	1917	1918	1919
780	1920	1921	1922	1923	1924	1925	1926	1927	1928	1929	1930	1931	1932	1933	1934	1935
790	1936	1937	1938	1939	1940	1941	1942	1943	1944	1945	1946	1947	1948	1949	1950	1951
7A0	1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967
7B0	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983
7C0	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999
7D0	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
7E0	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
7F0	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047
800	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063
810	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079
820	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095
830	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111
840	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127
850	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143
860	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159
870	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175
880	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191
890	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207
8A0	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223
8B0	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239
8C0	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255
8D0	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271
8E0	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287
8F0	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303
900	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319
910	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335
920	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351
930	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367
940	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383
950	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399
960	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415
970	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431
980	2432	2433	2434	2435	2436	2437	2438	2439	2440	2441	2442	2443	2444	2445	2446	2447
990	2448	2449	2450	2451	2452	2453	2454	2455	2456	2457	2458	2459	2460	2461	2462	2463
9A0	2464	2465	2466	2467	2468	2469	2470	2471	2472	2473	2474	2475	2476	2477	2478	2479
9B0	2480	2481	2482	2483	2484	2485	2486	2487	2488	2489	2490	2491	2492	2493	2494	2495
9C0	2496	2497	2498	2499	2500	2501	2502	2503	2504	2505	2506	2507	2508	2509	2510	2511
9D0	2512	2513	2514	2515	2516	2517	2518	2519	2520	2521	2522	2523	2524	2525	2526	2527
9E0	2528	2529	2530	2531	2532	2533	2534	2535	2536	2537	2538	2539	2540	2541	2542	2543
9F0	2544	2545	2546	2547	2548	2549	2550	2551	2552	2553	2554	2555	2556	2557	2558	2559
A00	2560	2561	2562	2563	2564	2565	2566	2567	2568	2569	2570	2571	2572	2573	2574	2575
A10	2576	2577	2578	2579	2580	2581	2582	2583	2584	2585	2586	2587	2588	2589	2590	2591
A20	2592	2593	2594	2595	2596	2597	2598	2599	2600	2601	2602	2603	2604	2605	2606	2607
A30	2608	2609	2610	2611	2612	2613	2614	2615	2616	2617	2618	2619	2620	2621	2622	2623
A40	2624	2625	2626	2627	2628	2629	2630	2631	2632	2633	2634	2635	2636	2637	2638	2639
A50	2640	2641	2642	2643	2644	2645	2646	2647	2648	2649	2650	2651	2652	2653	2654	2655
A60	2656	2657	2658	2659	2660	2661	2662	2663	2664	2665	2666	2667	2668	2669	2670	2671
A70	2672	2673	2674	2675	2676	2677	2678	2679	2680	2681	2682	2683	2684	2685	2686	2687

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HEXADECIMAL-DECIMAL NUMBER CONVERSION TABLE (Cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
A80	2688	2689	2690	2691	2692	2693	2694	2695	2696	2697	2698	2699	2700	2701	2702	2703
A90	2704	2705	2706	2707	2708	2709	2710	2711	2712	2713	2714	2715	2716	2717	2718	2719
AA0	2720	2721	2722	2723	2724	2725	2726	2727	2728	2729	2730	2731	2732	2733	2734	2735
AB0	2736	2737	2738	2739	2740	2741	2742	2743	2744	2745	2746	2747	2748	2749	2750	2751
AC0	2752	2753	2754	2755	2756	2757	2758	2759	2760	2761	2762	2763	2764	2765	2766	2767
AD0	2768	2769	2770	2771	2772	2773	2774	2775	2776	2777	2778	2779	2780	2781	2782	2783
AE0	2784	2785	2786	2787	2788	2789	2790	2791	2792	2793	2794	2795	2796	2797	2798	2799
AF0	2800	2801	2802	2803	2804	2805	2806	2807	2808	2809	2810	2811	2812	2813	2814	2815
B00	2816	2817	2818	2819	2820	2821	2822	2823	2824	2825	2826	2827	2828	2829	2830	2831
B10	2832	2833	2834	2835	2836	2837	2838	2839	2840	2841	2842	2843	2844	2845	2846	2847
B20	2848	2849	2850	2851	2852	2853	2854	2855	2856	2857	2858	2859	2860	2861	2862	2863
B30	2864	2865	2866	2867	2868	2869	2870	2871	2872	2873	2874	2875	2876	2877	2878	2879
B40	2880	2881	2882	2883	2884	2885	2886	2887	2888	2889	2890	2891	2892	2893	2894	2895
B50	2896	2897	2898	2899	2900	2901	2902	2903	2904	2905	2906	2907	2908	2909	2910	2911
B60	2912	2913	2914	2915	2916	2917	2918	2919	2920	2921	2922	2923	2924	2925	2926	2927
B70	2928	2929	2930	2931	2932	2933	2934	2935	2936	2937	2938	2939	2940	2941	2942	2943
B80	2944	2945	2946	2947	2948	2949	2950	2951	2952	2953	2954	2955	2956	2957	2958	2959
B90	2960	2961	2962	2963	2964	2965	2966	2967	2968	2969	2970	2971	2972	2973	2974	2975
BA0	2976	2977	2978	2979	2980	2981	2982	2983	2984	2985	2986	2987	2988	2989	2990	2991
BB0	2992	2993	2994	2995	2996	2997	2998	2999	3000	3001	3002	3003	3004	3005	3006	3007
BC0	3008	3009	3010	3011	3012	3013	3014	3015	3016	3017	3018	3019	3020	3021	3022	3023
BD0	3024	3025	3026	3027	3028	3029	3030	3031	3032	3033	3034	3035	3036	3037	3038	3039
BE0	3040	3041	3042	3043	3044	3045	3046	3047	3048	3049	3050	3051	3052	3053	3054	3055
BF0	3056	3057	3058	3059	3060	3061	3062	3063	3064	3065	3066	3067	3068	3069	3070	3071
C00	3072	3073	3074	3075	3076	3077	3078	3079	3080	3081	3082	3083	3084	3085	3086	3087
C10	3088	3089	3090	3091	3092	3093	3094	3095	3096	3097	3098	3099	3100	3101	3102	3103
C20	3104	3105	3106	3107	3108	3109	3110	3111	3112	3113	3114	3115	3116	3117	3118	3119
C30	3120	3121	3122	3123	3124	3125	3126	3127	3128	3129	3130	3131	3132	3133	3134	3135
C40	3136	3137	3138	3139	3140	3141	3142	3143	3144	3145	3146	3147	3148	3149	3150	3151
C50	3152	3153	3154	3155	3156	3157	3158	3159	3160	3161	3162	3163	3164	3165	3166	3167
C60	3168	3169	3170	3171	3172	3173	3174	3175	3176	3177	3178	3179	3180	3181	3182	3183
C70	3184	3185	3186	3187	3188	3189	3190	3191	3192	3193	3194	3195	3196	3197	3198	3199
C80	3200	3201	3202	3203	3204	3205	3206	3207	3208	3209	3210	3211	3212	3213	3214	3215
C90	3216	3217	3218	3219	3220	3221	3222	3223	3224	3225	3226	3227	3228	3229	3230	3231
CA0	3232	3233	3234	3235	3236	3237	3238	3239	3240	3241	3242	3243	3244	3245	3246	3247
CB0	3248	3249	3250	3251	3252	3253	3254	3255	3256	3257	3258	3259	3260	3261	3262	3263
CC0	3264	3265	3266	3267	3268	3269	3270	3271	3272	3273	3274	3275	3276	3277	3278	3279
CD0	3280	3281	3282	3283	3284	3285	3286	3287	3288	3289	3290	3291	3292	3293	3294	3295
CE0	3296	3297	3298	3299	3300	3301	3302	3303	3304	3305	3306	3307	3308	3309	3310	3311
CF0	3312	3313	3314	3315	3316	3317	3318	3319	3320	3321	3322	3323	3324	3325	3326	3327
D00	3328	3329	3330	3331	3332	3333	3334	3335	3336	3337	3338	3339	3340	3341	3342	3343
D10	3344	3345	3346	3347	3348	3349	3350	3351	3352	3353	3354	3355	3356	3357	3358	3359
D20	3360	3361	3362	3363	3364	3365	3366	3367	3368	3369	3370	3371	3372	3373	3374	3375
D30	3376	3377	3378	3379	3380	3381	3382	3383	3384	3385	3386	3387	3388	3389	3390	3391
D40	3392	3393	3394	3395	3396	3397	3398	3399	3400	3401	3402	3403	3404	3405	3406	3407
D50	3408	3409	3410	3411	3412	3413	3414	3415	3416	3417	3418	3419	3420	3421	3422	3423
D60	3424	3425	3426	3427	3428	3429	3430	3431	3432	3433	3434	3435	3436	3437	3438	3439
D70	3440	3441	3442	3443	3444	3445	3446	3447	3448	3449	3450	3451	3452	3453	3454	3455
D80	3456	3457	3458	3459	3460	3461	3462	3463	3464	3465	3466	3467	3468	3469	3470	3471
D90	3472	3473	3474	3475	3476	3477	3478	3479	3480	3481	3482	3483	3484	3485	3486	3487
DA0	3488	3489	3490	3491	3492	3493	3494	3495	3496	3497	3498	3499	3500	3501	3502	3503
DB0	3504	3505	3506	3507	3508	3509	3510	3511	3512	3513	3514	3515	3516	3517	3518	3519
DC0	3520	3521	3522	3523	3524	3525	3526	3527	3528	3529	3530	3531	3532	3533	3534	3535
DD0	3536	3537	3538	3539	3540	3541	3542	3543	3544	3545	3546	3547	3548	3549	3550	3551
DE0	3552	3553	3554	3555	3556	3557	3558	3559	3560	3561	3562	3563	3564	3565	3566	3567
DF0	3568	3569	3570	3571	3572	3573	3574	3575	3576	3577	3578	3579	3580	3581	3582	3583

APPENDIX J

HEXADECIMAL-DECIMAL NUMBER CONVERSION TABLE (Cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E00	3584	3585	3586	3587	3588	3589	3590	3591	3592	3593	3594	3595	3596	3597	3598	3599
E10	3600	3601	3602	3603	3604	3605	3606	3607	3608	3609	3610	3611	3612	3613	3614	3615
E20	3616	3617	3618	3619	3620	3621	3622	3623	3624	3625	3626	3627	3628	3629	3630	3631
E30	3632	3633	3634	3635	3636	3637	3638	3639	3640	3641	3642	3643	3644	3645	3646	3647
E40	3648	3649	3650	3651	3652	3653	3654	3655	3656	3657	3658	3659	3660	3661	3662	3663
E50	3664	3665	3666	3667	3668	3669	3670	3671	3672	3673	3674	3675	3676	3677	3678	3679
E60	3680	3681	3682	3683	3684	3685	3686	3687	3688	3689	3690	3691	3692	3693	3694	3695
E70	3696	3697	3698	3699	3700	3701	3702	3703	3704	3705	3706	3707	3708	3709	3710	3711
E80	3712	3713	3714	3715	3716	3717	3718	3719	3720	3721	3722	3723	3724	3725	3726	3727
E90	3728	3729	3730	3731	3732	3733	3734	3735	3736	3737	3738	3739	3740	3741	3742	3743
EA0	3744	3745	3746	3747	3748	3749	3750	3751	3752	3753	3754	3755	3756	3757	3758	3759
EB0	3760	3761	3762	3763	3764	3765	3766	3767	3768	3769	3770	3771	3772	3773	3774	3775
EC0	3776	3777	3778	3779	3780	3781	3782	3783	3784	3785	3786	3787	3788	3789	3790	3791
ED0	3792	3793	3794	3795	3796	3797	3798	3799	3800	3801	3802	3803	3804	3805	3806	3807
EE0	3808	3809	3810	3811	3812	3813	3814	3815	3816	3817	3818	3819	3820	3821	3822	3823
EF0	3824	3825	3826	3827	3828	3829	3830	3831	3832	3833	3834	3835	3836	3837	3838	3839
F00	3840	3841	3842	3843	3844	3845	3846	3847	3848	3849	3850	3851	3852	3853	3854	3855
F10	3856	3857	3858	3859	3860	3861	3862	3863	3864	3865	3866	3867	3868	3869	3870	3871
F20	3872	3873	3874	3875	3876	3877	3878	3879	3880	3881	3882	3883	3884	3885	3886	3887
F30	3888	3889	3890	3891	3892	3893	3894	3895	3896	3897	3898	3899	3900	3901	3902	3903
F40	3904	3905	3906	3907	3908	3909	3910	3911	3912	3913	3914	3915	3916	3917	3918	3919
F50	3920	3921	3922	3923	3924	3925	3926	3927	3928	3929	3930	3931	3932	3933	3934	3935
F60	3936	3937	3938	3939	3940	3941	3942	3943	3944	3945	3946	3947	3948	3949	3950	3951
F70	3952	3953	3954	3955	3956	3957	3958	3959	3960	3961	3962	3963	3964	3965	3966	3967
F80	3968	3969	3970	3971	3972	3973	3974	3975	3976	3977	3978	3979	3980	3981	3982	3983
F90	3984	3985	3986	3987	3988	3989	3990	3991	3992	3993	3994	3995	3996	3997	3998	3999
FA0	4000	4001	4002	4003	4004	4005	4006	4007	4008	4009	4010	4011	4012	4013	4014	4015
FB0	4016	4017	4018	4019	4020	4021	4022	4023	4024	4025	4026	4027	4028	4029	4030	4031
FC0	4032	4033	4034	4035	4036	4037	4038	4039	4040	4041	4042	4043	4044	4045	4046	4047
FD0	4048	4049	4050	4051	4052	4053	4054	4055	4056	4057	4058	4059	4060	4061	4062	4063
FE0	4064	4065	4066	4067	4068	4069	4070	4071	4072	4073	4074	4075	4076	4077	4078	4079
FF0	4080	4081	4082	4083	4084	4085	4086	4087	4088	4089	4090	4091	4092	4093	4094	4095