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Technical Manual

RAPID ACCESS DATA FILE

MODELS 9367B 9367C-01

SDS 901029A

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SDS

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LIST OF EFFECTIVE PAGES

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LIST OF RELATED PUBLICATIONS

The following publications contain information not included herein but which is necessary for a complete understanding of RAD File Models 9367B and 9367C when used with related SDS equipment.

Publication Title	Publication No.
SDS Computer Model 92 Reference Manual	900505
SDS Computer Model 92 Theory of Operation	900864
SDS Computer Model 925 Reference Manual	900099
SDS Computer Model 925 Theory of Operation	900633
SDS Computer Model 930 Reference Manual	900064
SDS Computer Model 930 Theory of Operation	900066
SDS Computer Model 9300 Reference Manual	900050
SDS Computer Model 9300 Theory of Operation	900570
SDS 92200/93200 Time-Multiplexed Communication Channel, Theory of Operation	900685
SDS 92220 Direct Access Communication Channel, Theory of Operation	900696
SDS 925/930/9300 Input-Output Interface Design Manual	900561
SDS Silicon Logic Circuit Modules, C, H, and L Series, Applications Manual	64-55-14
SDS Power Supply Model PX13, Technical Manual	900001-C
SDS 910, 920, 925, 930, or 9300 Diagnostic Control Program	004009
SDS 92 RAD Apocalyptic Diagnostic	794004
SDS 925/930 RAD Apocalyptic Diagnostic	594003
SDS 9300 RAD Apocalyptic Diagnostic	694010
SDS Automatic Instruction Diagnostic Program for Computer Model 9300	604004
Bryant Computer Products Handbook Auto-Lift Magnetic Storage Drum	BCPH-101-5-64

SECTION I
GENERAL DESCRIPTION

1-1 INTRODUCTION

1-2 SCOPE OF MANUAL

This manual provides technical information pertaining to the Rapid Access Data File Model 9367B (RAD File Model 9367B) and Rapid Access Data File Model 9367C (RAD File Model 9367C) manufactured by Scientific Data Systems, 1649 Seventeenth Street, Santa Monica, California 90404. RAD File Model 9367B contains a drum memory; RAD File Model 9367C contains a disc memory. When either RAD file is installed with an SDS computer, the applicable documents tabulated in the List of Related Publications should be available to supplement the information contained herein. A complete set of documents comprises this manual and related publications, engineering drawings, wire lists, diagnostic programs, and other data supplied with the equipment.

1-3 ORGANIZATION OF MANUAL

The information contained in this manual is organized as follows:

a. Section I General Information: Functional and physical descriptions, model differences, specifications and leading particulars.

b. Section II Operation and Programming: Functions of all controls and indicators, operation and programming information.

c. Section III Theory of Operation: General and detailed theory of operation.

d. Section IV Installation and Maintenance: Installation planning, installation procedure, maintenance, and spares information.

e. Section V Performance Testing and Trouble Analysis: Test procedures, diagnostic programming description, and trouble analysis data for confirming proper operation or locating trouble.

f. Section VI Parts Lists: Location, identification, and listing of all major assemblies, subassemblies, and replaceable parts in RAD File Models 9367B and 9367C.

g. Section VII Drawings: Engineering drawings, wire list identification and clarification.

h. Section VIII Logic Equations: Lists of all logic equations for RAD file subassemblies, relation of the logic equations to logic diagrams and wire lists, and instructions and examples of signal mnemonics interpretation.

1-4 GENERAL DESCRIPTION

1-5 FUNCTIONAL DESCRIPTION

Either RAD file provides on-line, rapid access, auxiliary data storage for SDS Computer Models 92, 925, 930, 940, and 9300. The basic elements of a RAD file are the RAD memory unit, controller, and power protection panel (figure 1-1). The RAD memory unit can store 524,288 characters, 1,048,576 characters, or 2,097,152 characters. A RAD file installation includes up to four memory units with a maximum of 8,388,608 stored six-bit characters accessible to the computer. The stored characters can be transferred between the RAD memory unit and the associated computer at the rate of 588,000 characters per second. The controller functions as the interface between one to four RAD memory units of a RAD file installation and an input/output channel of a computer. The power protection panel enables selected data to be stored in memory in case of power failure.

1-6 PHYSICAL DESCRIPTION

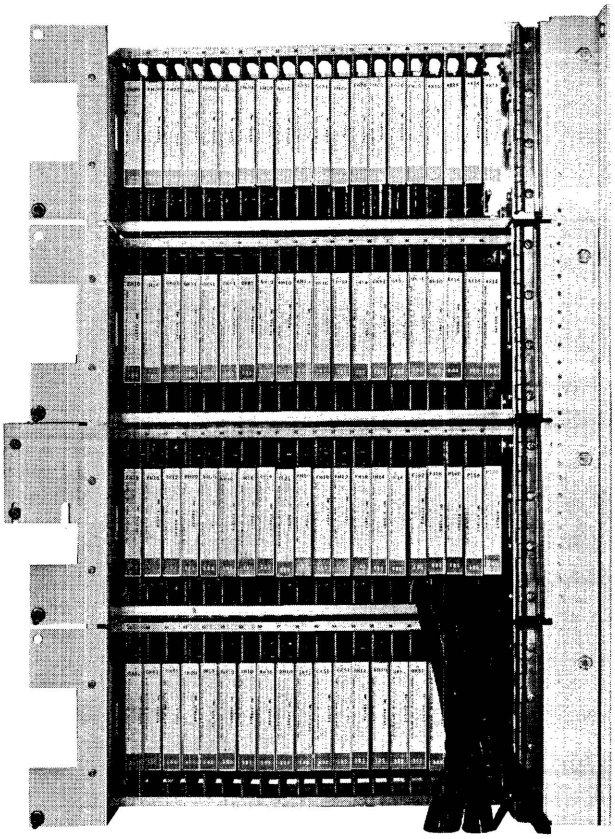
A basic RAD file installation consists of a RAD memory unit, a controller, a power protection panel, and cable assemblies (figure 1-2). The RAD memory unit can be installed remotely from the computer (subject to cable length limitations). The controller and power protection panel are installed in or near the computer also as limited by cable length.

1-7 RAD Memory Unit

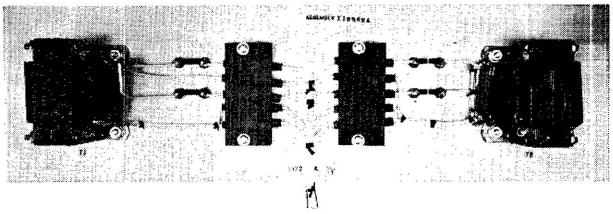
The RAD memory unit contains the memory (disc or drum), selection unit, and power supplies (figure 6-1). The RAD memory unit is connected to an ac source through an 8-foot power cord. The power distribution panel routes ac to other subassemblies of the RAD memory unit and to the ac plug mold. A forced air cooling unit powered from the ac plug mold causes cool air to enter at the bottom of the RAD memory unit and exit through fans at the top. Power Supply Model PX13 is installed in a RAD memory unit to provide dc for the selection unit. One PX13 can supply power for two selection units. A 3 or 4 RAD memory unit installation requires two PX13 power supplies.

1-8 Controller

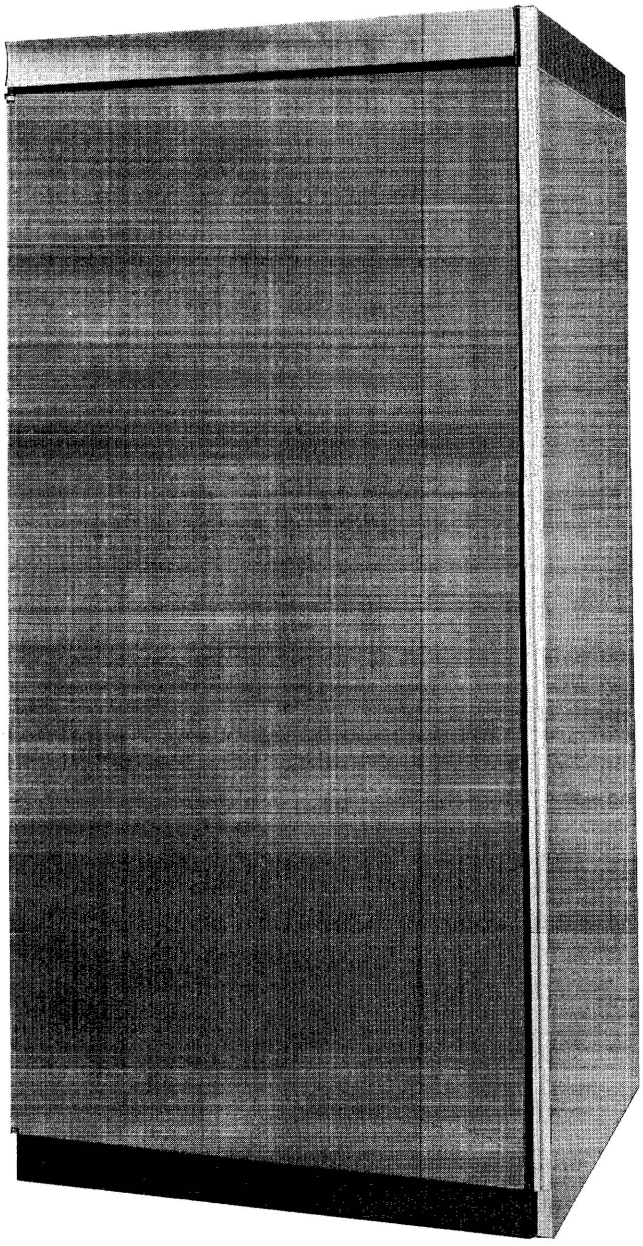
The controller is installed in or near the computer, is connected to the computer input/output channel through four



CONTROLLER UNIT



POWER PROTECTION PANEL



BASIC MEMORY UNIT

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Figure 1-1. RAD File Model 9367B/C

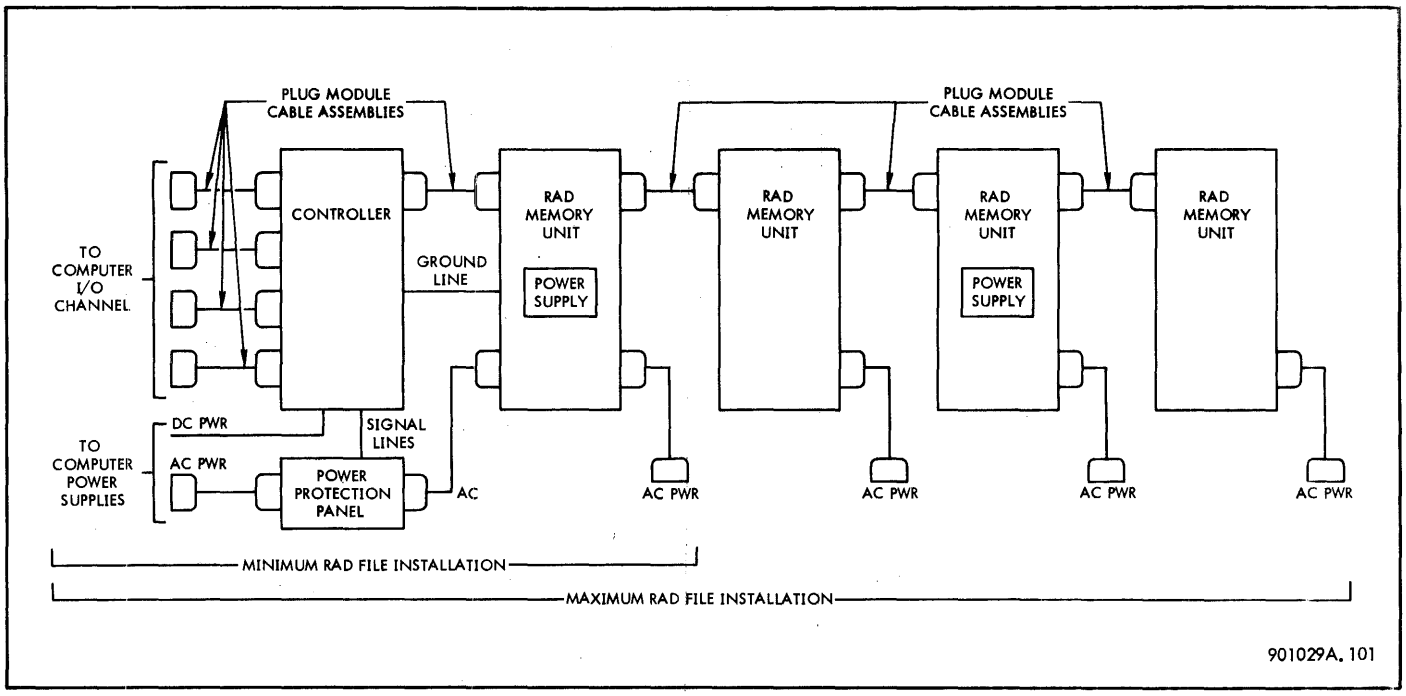


Figure 1-2. RAD File Installation Block Diagram

cable assemblies, and is connected to the selection unit in the RAD memory unit through one cable assembly. The controller draws module dc from the computer. A ground line is connected from the controller to the selection unit in a RAD memory unit.

1-9 Power Protection Panel

All power protection panel components are mounted on a standard 5-1/4 by 19 inch panel. Power protection panel components are connected to the computer ac source, RAD memory ac source, and to control circuits of the controller. The power protection panel must be mounted near these components to enable hookup of panel wiring.

1-10 Cable Assemblies

Each cable assembly consists of two printed circuit boards connected by a wiring harness. Some printed circuit boards include electronic components (diodes, resistors, inductors) connected by additional point-to-point wiring; other printed circuit boards include only point-to-point wiring. The printed circuit boards are the connectors for the plug module cable assemblies and are inserted in specified locations in the same manner as circuit boards containing logic circuits.

1-11 MODEL DIFFERENCES

Characteristics of the six models of RAD File Model 9367B and the four models of RAD File Model 9367C are summarized in table 1-1. The three memory capacities (disc or drum) are approximately half-million, one million, and two million characters. The minimum RAD file (suffix 0X) consists of a RAD memory unit, a controller, a power protection panel, and five cable assemblies (figure 1-2). Four cable assemblies connect the controller to the computer input/output channel; one cable assembly connects the controller to the RAD memory unit. A RAD file installation of more than one RAD memory unit includes a basic RAD file and up to three additional RAD files (suffix 1X). Each of these RAD files includes a RAD memory unit and an interconnecting cable assembly.

1-12 SPECIFICATIONS AND LEADING PARTICULARS

1-13 RAD FILE

Physical characteristics of a RAD file are listed in table 1-2. Environmental and electrical characteristics are listed in table 1-3. Table 1-4 lists memory capacity of RAD file installations in terms of the number and models of RAD files in the installation. These are the major characteristics to be considered when planning a RAD file installation. For detailed information about signal levels, bit rates, and other engineering data, refer to the following SDS documents:

Disc memory purchase specification 113374
Drum memory purchase specification 127890

The module complements of RAD File Models 9367B and 9367C are listed in tables 1-5 and 1-6. Each RAD memory unit in a multiple-unit installation includes a selection unit; therefore, the total module complement is the controller module complement plus the module complement for each RAD memory unit in the installation. The selection

unit is used with either the drum memory or the disc memory.

1-14 Drum Memory

The drum memory in RAD File Model 9367B uses a magnetically coated drum rotating on a vertical shaft. Connector J1 is used for power input, J2 and J4 are for read/write inputs, and J3, J5, and J7 are for clock outputs. Full frequency is defined as reading a track recorded at a density of 900 bits per inch, one bit being represented by a double flux reversal. The frequency is nominally 810 khz (varying with drum rotational speed) or the frequency obtained from a clock track recorded with 28,288 bits around the periphery.

Playback of the track into a load of 560 ohms across two half-coils produces an 11 to 50 mv amplitude output. Three clock tracks are prerecorded by the manufacturer with 27,712 bits. The sector marks consists of 63 single doublets followed by a double doublet index mark. The positive peaks of the single doublets do not deviate more than ±2 μsec. The second doublet of the double doublet occurs 5.0 ±1.0 μsec after the positive peak of the first doublet, with a minimum pulse of 7.5 mv, measured with reference to a zero of 1.5 mv maximum into a load of 2000 ohms. The three clock tracks are identical sine waves.

The interconnecting cables for the drum memory (power, read/write matrix heads, and clock) are interchangeable between all three drums (128, 256, and 512 heads). Drum memory power is controlled at the three-phase circuit breaker on the power distribution panel.

1-15 Disc Memory

The disc memory used in RAD File Model 9367C uses one, two, or four magnetically coated discs rotating on a vertical shaft. Both sides of each disc are used together with 64 read/write heads for each surface, or 128 per disc. Connector J1 is used for power input, J3 is for read/write inputs, and J7 is for clock outputs. The discs and heads are mounted in an air-tight enclosure which must not be opened except in a cleanroom. If the enclosure is opened, the memory must be returned to the factory for cleaning, lubrication, and purging.

A motor starting box on the side of the memory housing is cable interconnected to the motor receptacle on the memory housing. The motor starting box power cord connects to the ac plug mold. The power, read/write matrix, and clock cables are interchangeable between all three disc memories.

Full frequency is defined as recording (after dc erasure) 838 khz on any of 64 tracks on any surface with a resultant playback amplitude across two half-coils of 10 to 48 mv across a load of 560 ohms. The three clock tracks produce the same signals as the drum memory clock tracks.

Disc memory power is controlled at the single-phase circuit breaker on the power distribution panel.

Table 1-1. RAD File Models 9367B and 9367C Model Differences

Model No.	Part No.	Memory	Memory Size (Characters)	Power Supplies	Controller	Power Protection Panel	Cable Assemblies
9367B-01	132802	127898-001	524,288	101270	131564	116989	113896
9367B-02	132803	127898-002	1,048,576	101271			113899
9367B-04	132804	127898-004	2,097,152				113902
							116388
							116513
9367B-11	132805	127898-001	524,288	See Note	None	None	116509
9367B-12	132806	127898-002	1,048,576				
9367B-14	132807	127898-004	2,097,152				
9367C-01	132808	115261-001	524,288	101270	131564	116989	113896
9367C-02	132809	115261-002	1,048,576	101271			113899
							113902
							116388
							116513
9367C-11	132811	115261-001	524,288	See Note	None	None	116509
9367C-12	132812	115261-002	1,048,576				

Note: Requires a power supply if installation includes 3 or 4 RAD memory units

Table 1-2. RAD File Models 9367B and 9367C Physical Characteristics

RAD MEMORY UNIT			
Height (max)	63.47 in.		
Width (max)	28.09 in.		
Depth (max)	25.84 in.		
Weight (max)	760 lbs		
Drum Memory	127898-001	127898-002	127898-004
Height	16-3/8 in.	17-7/8 in.	30-3/4 in.
Width	17-1/2 in.	17-1/2 in.	17-1/2 in.
Depth	17-1/2 in.	17-1/2 in.	17-1/2 in.
Weight	120 lbs	160 lbs	250 lbs
Shipping weight	190 lbs	229 lbs	295 lbs
Disc Memory			
Height	18 in.		
Width	16-1/2 in.		
Depth	21-1/2 in.		
Weight	760 lbs (Shipped in cabinet)		
Controller			
Height (max)	28.00 in.		
Width (max)	18.78 in.		
Depth (max)	8.66 in.		
Weight (max)	90 lbs		
Power Protection Panel			
Height (max)	5.25 in.		
Width (max)	19.03 in.		
Depth (max)	3.81 in.		
Weight (max)	6 lbs		
Plug Module Cable Assembly Lengths			
Controller to RAD Memory Unit	P170/P171	30 ft	
	P155/P156	10 ft	
Computer to Controller	P157/P158	10 ft	
	P159/P160	10 ft	
	P161/P162	10 ft	
RAD Memory Unit to RAD Memory Unit	P168/P169	4 ft	
RAD Memory Unit Power Cable Length		8 ft	

Table 1-3. RAD File Models 9367B and 9367C Environmental and Electrical Characteristics

Operating temperature range	10° to 40°C (50° to 104°F)	
Relative humidity range	10 to 90 percent	
Altitude range	0 to 10,000 feet	
	Unregulated AC (volt-amperes)	Heat Dissipation (btu/hr)
Model 9367B-0X	775	2370
Model 9367B-0X with -1X	1010	3170
Model 9367B-1X No. 1	295	740
Model 9367B-1X No. 2	530	1540
Model 9367B-1X No. 2 with -1X No. 3	765	2340
Model 9367B-1X No. 3	295	740
Model 9367C-0X	935	3090
Model 9367C-0X with -1X	1115	3700
Model 9367C-1X No. 1	455	1460
Model 9367C-1X No. 2	690	2260
Model 9367C-1X No. 2 with -1X No. 3	870	2870
Model 9367C-1X No. 3	455	1460
Dc from computer	+8v, 2.5 amperes +25v, 6.0 amperes -25v, 1.0 ampere	
Ac from computer	220 volt-amperes regulated 245 volt-amperes unregulated	

Table 1-4. Memory Capacity of RAD File Installations

MODEL						TOTAL	CAPACITY IN CHARACTERS (6 bits per character)
-01	-02	-04	-11	-12	-14		
1						1	524,288
	1					1	1,048,576
		1				1	2,097,152
		1	1			2	2,621,430
		1		1		2	3,145,728
		1			1	2	4,194,304
		1	1		1	3	4,718,592
		1		1	1	3	5,242,880
		1			2	3	6,291,456
		1	1		2	4	6,815,744
		1		1	2	4	7,340,032
		1			3	4	8,388,608

Table 1-5. Module Complement of Selection Unit

Module	Reference Designation	Total
Read Input Control AK61	B20	1
Y-Select AK62	B12*, B13*, B14, B15, B16†, B17†, B18†, B19†	8
Write Driver AK63	A14, A15, A16, A17, A18, A19, A22, A25, B4, B5, B6, B7, B8, B9, B10, B11	16
Index/Sector Amplifier AK64	B2	1
Write Clock Amplifier AK65	B1	1
Cable Driver AX14	A4, A5, A6	3
AND/OR Buffer Amplifier BH10	A7	1
DC Flip-Flop FH19	A9	1
Basic Flip-Flop FL21	A2, A3, A30, A31	4
Gate Expander GH14	A8	1
Read Preamplifier HK73	B22, B25, B28, B31	4
Limiter HK74	B21, B24, B27, B30	4
Clock Discriminator HK75	A20, A23, A26, A29	4
Data Decoder HK76	A21, A24, A27, A30	4
Index/Sector Decoder HK77	B3	1
AND Gate/Inverter IL12	A10	1
Read-Write Decoder NK59	B23, B26 B29, B32	4
One-Shot Multivibrator OX12	C43	1
+4v Regulator SX60	A12	1
-8v Regulator SX69	A13	1

*Used in -X2 Models and -X4 Models
†Used in -X4 Models

Table 1-6. Module Complement of Controller

Module	Reference Designation	Total
Signal Amplifier AH10	B36, B37, B38, C36, C40	5
Cable Driver AX14	A28, A29, B26, B27, B28	5
Cable Driver AX16	A26, A27	2
AND/OR Buffer Amplifier BH10	A37, B29, B35, B45, C41, C42, D32, D37, D38, D40	10
DC Flip-Flop FH19	C33, C34, C35, C44, C46	5
Basic Flip-Flop FH20	A30, A31, A32, A33, A34, A38, A39, A40, A41, A43, A44, A45, D42	13
Basic Flip-Flop FL21	C37	1
Diode Gate No. 1 GK51	A35, A36, A42, B30, B31, B32, B39, B40, B41, B42, B43, D30, D31, D34, D35, D36, D43, D44, D45	19
AND/OR Inverter IH10	D39, D41	2
AND Gate/Inverter IH14	B33, B34, B44, C31, C32, C38, C39, D33	8
Relay Module KX12	D27	1
One-Shot Multivibrator OX12	C43	1
Primary Power Detector SK60	D28, D29	2

SECTION II
OPERATION AND PROGRAMMING

2-1 OPERATION

2-2 CONTROLS, INDICATORS, AND WORD FORMAT

This section describes controls and indicators of RAD File Models 9367B and 9367C, routine turn-on/turn-off procedures, and program control of input/output. All programming information in this technical manual is based on the 24-bit word format and instruction format typical of SDS computers 930 and 9300. For selected instruction codes, 15 bits of the 24-bit word format address locations in a RAD file installation. For the 12-bit instruction format of the SDS 92 computer, the 15-bit S-register stores address codes for transfer to the RAD file.

Table 2-1 lists RAD file controls and indicators. All assembly controls and indicators are located in the RAD memory unit. For details concerning Power Supply Model PX13, refer to SDS publication 900001-C.

Prior to equipment operation, the controls and indicators listed in table 2-1 should conform to the following pattern: MEMORY PROTECTION SWITCHES in the up position (preventing writing in all memory locations); all switches and circuit breakers in the position corresponding to power off; and all indicators not lighted. The turn-on procedure in paragraph 2-4 assumes these initial conditions.

Table 2-1. RAD File Controls and Indicators

Control or Indicator	Ref. Desig.	Function
Power Supply Model PX13		
ON/OFF switch	S1	Controls application of ac to Power Supply Model PX13
POWER indicator	DS1	Lighted when ON/OFF switch is ON
Selection Unit		
MEMORY PROTECTION SWITCHES (000 thru 017)	S1 thru S16	In up position, prevents insertion of new data in associated locations
Power Distribution Panel		
Circuit breaker	CB2	Controls application of 1Ø ac
Circuit breaker	CB3	Controls application of 3Ø ac

2-3 START-STOP PROCEDURES

The turn-on procedure in paragraph 2-4 and the turn-off procedure of paragraph 2-5 are used for routine operation. For initial installation and for turn-on following repair, use the performance testing procedure in section V.

2-4 TURN-ON PROCEDURE

Turn on the RAD file installation as follows:

Note

For RAD file installations of more than one RAD memory unit, perform these steps for each RAD memory unit.

a. Check that all controls and indicators are off.

b. At Power Supply Model PX13, place ON/OFF switch ON.

CAUTION

RAD File Model 9367B (drum memory) has a directional arrow marked on the equipment. Immediately after applying power, check that the fan moves in the direction indicated. If not, remove power before drum reaches operating speed.

c. At power distribution panel, set circuit breakers ON and check that:

1. Fans at top of RAD memory unit are operating

2. POWER indicator on Power Supply Model PX13 is lighted

3. Fan in drum memory rotates counterclockwise.

d. At selection unit control panel, place appropriate MEMORY PROTECTION SWITCHES in down position to enable computer to write in memory.

2-5 TURN-OFF PROCEDURE

Since the order of power removal from subassemblies of the RAD file is not critical, turn-off can be accomplished in any of three ways:

a. Place each switch in off position, or

b. Place circuit breaker on power distribution panel OFF, or

c. At external control point (if available) disconnect RAD file power source.

2-6 PROGRAMMING

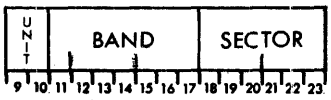
2-7 INSTRUCTIONS

Control signals and data signals exchanged between the RAD file and the computer are related to the following instructions:

Mnemonic	SDS 9300 Code	Name
EOM	02	Energize output M
SKS	20	Skip if signal not set
POT	31	Parallel output (from computer memory)
PIN	33	Parallel input (to computer memory)

Of the 24-bit instruction format (bits 0 through 23), only bits 9 through 23 are read by the RAD file. When bits 0 through 8 indicate an instruction of significance to the RAD file, a signal is generated within either the computer or the input/output channel and transmitted to the RAD file to control operations.

The RAD file response to a parallel output from computer memory (POT) instruction is to accept 15 bits (9 through 23) from the input/output channel. These bits address a location in the RAD file as indicated below:



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Bits 9 and 10 are a 2-bit code identifying one of a maximum of 4 RAD memory units. Bits 11 through 17 address a band on that RAD memory unit; bits 18 through 23 address one of 64 sectors in the band. Each sector contains 128 12-bit codes (64 24-bit words). A total of 128 bands may be contained in each RAD memory unit. Logical design of the controller prevents transfer from location XXX 111 111 111 111 to location XXX 000 000 000 000. Therefore, each RAD memory unit is divided into two groups of bands which must be addressed by separate POT operations. For each revolution of the memory data is read from 32 sectors. Two revolutions therefore are required to read a complete band of 64 sectors. For commands in the non-increment mode, data is read from a sector without incrementing the band address. This mode of operation makes possible reading data beginning with any sector of the band, and returning to read the initial part of the band after reading from an arbitrary location in the band.

The RAD file response to a parallel input to computer memory (PIN) instruction is to enable transmission of 6 bits (bits 18 through 23) to the computer. These bits represent the contents of a counter in the RAD file which identifies the sector currently being read in the addressed RAD memory unit.

All configurations of the energize output M (EOM) and skip if signal not set (SKS) instructions are identified by the mnemonic and a five-digit octal numeral which together define 21 bits of the 24-bit instruction format, as indicated by the following examples:

EOM 10026

XXX 000 010	001	000	000	010	110
EOM	1	0	0	2	6

SKS 13026

XXX 010 000	001	011	000	010	110
SKS	1	3	0	2	6

For any EOM or SKS instruction associated with a RAD file, the last two octal numerals are always 26 or 66. Instructions ending in 26 are related to computer input operations; instructions ending in 66 are related to computer output operations. Other bits of the instructions are related to the mode of operation of the computer or the input/output channel, to the format of the data accepted or transferred to the RAD file, or to other functions related to data exchange and equipment operation. EOM instructions and SKS instructions related to operation of the RAD file are listed in table 2-2.

2-8 SAMPLE PROGRAM

Table 2-3 lists a sample program which causes data stored in RAD file locations 00773 through 01572 (octal, 600 words; decimal, 384 words) to be read from the disc and stored in computer memory core locations 12707 through 13506 (octal). This program is intended only to clarify operations associated with execution of instructions to the RAD file and not to indicate best use of programming capabilities. Each step of the program is explained in the following paragraphs.

The SKS instruction in computer memory location 01202 tests a controller signal for a ready status. If the controller is either reading or writing, the program reads the instruction from location 01203, causing the computer to branch to location 01202. Thus the computer cycles through a two-instruction loop until the controller is ready, when the instruction in location 01204 is read.

The EOM instruction in location 01204 prepares the controller for the POT instruction in location 01205. The POT

instruction transfers the contents of location 01213 to the address register of the controller. This address identifies the first RAD file location from which data is to be transferred to the computer. The EOM instruction in location 01206 selects the W buffer, connects the RAD file to the computer through the W buffer, and establishes the 12-bit character format. The EOM instruction in location 01207 establishes the mandatory IOSD mode of operation and arms the zero-count interrupt of the W buffer.

The POT instruction read from location 01210 causes transfer of the contents of core memory location 01214 to the I/O channel interlace. Bits 0 through 9 of the interlace word contain an octal number equal to the number of words to be transferred. Bits 10 through 23 of the interlace word (12707) contain the address of the first of 600 (octal) core memory locations into which disc memory words are to be transferred. When this portion of the program has provided all parameters required to initiate a transfer of data, the branch instruction location in 01212 returns control to the main program. When the interlace word count reaches zero, the interrupt subroutine tests for possible program errors.

Table 2-2. EOM and SKS Instructions Used With RAD File

Instruction	Operation
EOM 10026	Alert to POT. Prepares controller for POT instruction which always follows alert to POT instruction. POT instruction causes address data to be stored in controller
EOM 02266	Connect RAD memory, write. Causes controller to send interface control signals, starting with the time addressed sector comes under disc memory write heads. Only IOSD (input/output until signal, then disconnect) EOM instructions may be used
EOM 02226	Connect RAD memory, read. Causes controller to send interface control signals, starting with the time addressed sector comes under disc memory read heads. Only IOSD EOM instructions may be used
EOM 11026	Alert to POT, no incrementing of band. Similar to EOM 10026, but used when a full band is to be transferred starting at an arbitrary sector, and band incrementing is not desired after last sector in band. Controller in non-increment mode

(Continued)

Table 2-2. EOM and SKS Instructions Used With RAD File (Cont.)

Instruction	Operation
EOM 1N206	Alert to PIN. Prepares controller for PIN instruction which always follows alert to PIN instruction. PIN instruction causes a 6-bit code representing sector count of addressed RAD memory unit to be transferred to computer. For RAD memory unit 1, 2, 3, or 4, N is 00X, 01X, 10X, or 11X, respectively. Controller disregards least significant bit of N
SKS 10026	Skip if controller ready. Samples controller output which indicates if controller is ready to exchange data with input/output channel
SKS 11026	Skip if no controller error. Samples controller output which indicates if programming error or processing error has occurred
SKS 13026	Skip if band not write-protected. Samples controller output which indicates if addressed memory location can be used for storage of data from computer (not write-protected location)

Table 2-3. Example of RAD File Read Program

Computer Memory Location	Instruction	Operation
01201	- - - -	- - - -
01202	SKS 10026	Skip if controller ready (signal)
01203	BR 01202	Branch to 01202
01204	EOM 10026	Alert to POT
01205	POT 01213	Parallel output of (01213) to controller
01206	EOM 50000	Alert interlace
01207	EOM 15200	IOSD and arm zero word count interrupt
01210	POT 01214	Set up interlace
01211	EOM 02226	Connect memory, read

(Continued)

Table 2-3. Example of RAD File Read Program (Cont.)

Computer Memory Location	Instruction	Operation
01212	BR ----	Branch to main program
01213	00 000 773	RAD file location
01214	30012 707	Interlace word count and starting memory location

2-9 PARTIAL SECTOR READ OR WRITE

Entire 64-word sectors need not be written or read. However, if less than a complete sector is to be transferred restrictions are imposed on the program. For example, if in the sample read program of table 2-3 only 32 words (40 octal) are to be read, the contents of the interlace word 01214 must be 01752707. When the interlace word count reaches zero, the W buffer generates a disconnect signal and the W buffer accepts no additional data from the RAD file.

If less than a complete sector is written or read, the word boundary ranges from the first word. It is not possible to read or write the last 32 words of a sector without reading or writing the first 32 words of the sector. If less than 64 words are to be written into a sector, zeros will be written in all RAD file word locations following the final data word for the sector. For example, if data is written into only the first 20 words of a sector, the remaining 44 words will be all zeros.

2-10 IMMEDIATE MODE ACCESSING

When one complete band (64 sectors) is to be transferred, access time can be reduced to a minimum by special programming techniques. If the program addresses the RAD file without determining the sector being read, access time can be as long as 35 milliseconds. For example, if the program is written to read sector 00 through 77 (octal), and sector 13 is under the read/write heads at the time the transfer is initiated, about 30 milliseconds will be spent before sector 00 comes under the heads and the transfer can begin. During these 30 milliseconds, the I/O channel cannot be used for other input/output operations. This delay can be eliminated if the program is written so that the complete 64 sector band is read in two separate passes. The first pass reads sector n through 77, and the second pass reads sectors 00 through (n-1), where n equals the first sector available during storage. The starting address n is obtained by executing a PIN instruction to determine the current sector address and adding two to this address. For example, if the PIN instruction reads sector 23 as the current address, the first pass reads sectors 25 through 77 and the second pass reads sectors 00 through 24.

Normally, if 64 sectors are to be transferred and the starting address is not 00, the band address will count up as the sector address changes from 77 to 00. To prevent this change, a one is placed in bit 14 of the instruction word to define the non-increment mode as indicated in table 2-2. When using the immediate access mode, the end-of-record interrupt must be armed so that when sector 77 has been read, the interrupt signal will cause the computer to enter the interrupt subroutine. This interrupt subroutine must supply the core memory locations for the transfer of sectors 00 through (n-1).

2-11 INTERRUPT OPTION

Access time can also be reduced by use of the interrupt option. This option allows the program to set up initial transfer conditions without connecting the buffer thereby permitting the selection unit and controller to search for the first address to be transferred without tying up the I/O channel. When the addressed sector is available to the selection unit, the interrupt occurs. The interrupt subroutine connects the controller with a connect-to-read or connect-to-write EOM instruction.

SECTION III
THEORY OF OPERATION

3-1 SCOPE OF SECTION

This section describes the theory of operation of RAD File Models 9367B and 9367C for maintenance, operation, and trouble analysis. For Power Supply Model PX13 information refer to SDS publication 900001. An analysis of common logic circuits is included in SDS publication 64-55-14; circuit analysis of modules designed for use in RAD File Models 9367B and 9367C is included in this section. Table 3-1 relates signal designations of the controller to those listed in SDS publication 900516.

Table 3-1. Controller Input/Output to Computer Input/Output Signal Relation

Controller Signal	DACC Signal	TMCC W Buffer Signal	TMCC Y Buffer Signal
8BUCW	Buz	Buc	Buc
8C09C	C9	C9	C9
thru	thru	thru	thru
8C23C	C23	C23	C23
8C12W	C12	C12	C12
thru	thru	thru	thru
8C23W	C23	C23	C23
9D01A	$\overline{Cd18}$	$\overline{Cd18}$	$\overline{Cd18}$
thru	thru	thru	thru
9D06A	$\overline{Cd23}$	$\overline{Cd23}$	$\overline{Cd23}$
9ECWA	$\overline{Ecz}$	$\overline{Ecw}$	$\overline{Ecy}$
8IOCW	Ioz	Ioc	Ioc
8PINC	Pin	Pin	Pin
8PT1C	Pot 1	Pot 1	Pot 1
8PT2C	Pot 2	Pot 2	Pot 2

(Continued)

Table 3-1. Controller Input/Output to Computer Input/Output Signal Relation (Cont.)

Controller Signal	DACC Signal	TMCC W Buffer Signal	TMCC Y Buffer Signal
8Q20C	Qq2	Qq2	Qq2
9RTIC	$\overline{Rti}$	$\overline{Rti}$	$\overline{Rti}$
9RTOC	$\overline{Rt}$	$\overline{Rt}$	$\overline{Rt}$
8R01W	Rz1	Rw1	Ry1
thru	thru	thru	thru
8R06W	Rz6	Rw6	Ry6
8R07W	Rz7	Rw7	Ry7
thru	thru	thru	thru
8R12W	Rz12	Rw12	Ry12
9SI0A	$\overline{Sio}$	$\overline{Sio}$	$\overline{Sio}$
8ST0C	St	St	St
9V01A	$\overline{Zz1}$	$\overline{Zw1}$	$\overline{Zy1}$
thru	thru	thru	thru
9V06A	$\overline{Zz6}$	$\overline{Zw6}$	$\overline{Zy6}$
9V07A	$\overline{Zz7}$	$\overline{Zw7}$	$\overline{Zy7}$
thru	thru	thru	thru
9V12A	$\overline{Zz12}$	$\overline{Zw12}$	$\overline{Zy12}$
9WHSA	$\overline{Zhs}$	$\overline{Whs}$	$\overline{Yhs}$
9WESA	$\overline{Zes}$	$\overline{Wes}$	$\overline{Yes}$
8W50W	Z5	W5	Y5
8W60W	Z6	W6	Y6

(Continued)

Table 3-1. Controller Input/Output to Computer Input/Output Signal Relation (Cont.)

Controller Signal	DACC Signal	TMCC W Buffer Signal	TMCC Y Buffer Signal
8W90W	Z9	W9	Y9
8W10W	Z10	W10	Y10
thru	thru	thru	thru
8W14W	Z14	W14	Y14
9X12A	Zx12	Wx12	Yx12

Paragraph 3-2 describes RAD file/computer information flow during input and output operations, and timing and major signal flow within the controller, selection unit, and memory. This part of the section also covers functions of the major circuit divisions of the RAD file, the sequence of operations, and timing problems without reference to details of logic circuits. The selection unit in the RAD memory unit is suitable for use with either a disc memory (SDS part number 115621) or a drum memory (SDS part number 127898) without modification.

Paragraphs 3-3 through 3-41 provide detailed descriptions of each major circuit division of the controller and selection unit. Simplified diagrams of the selection unit and controller are provided in this section (refer to section VII for module circuit schematics; detailed logic diagrams and the corresponding equation lists are included in section VIII).

Paragraph 3-42 describes circuits of the RAD file which distribute ac and dc to the subassemblies, and the interlock to disconnect the RAD file in case of power failure. These circuits include Power Supply Model PX13, the power distribution panel, and portions of the controller.

3-2 GENERAL THEORY OF OPERATION

A RAD file installation includes a controller and a maximum of four RAD memory units, each of which contains a selection unit and a memory (figure 3-1). The controller functions as the interface between each RAD memory unit and the computer input/output channel. The computer input/output channel may be a Time-Multiplexed Communication Channel (TMCC) or a Direct Access Communication Channel (DACC).

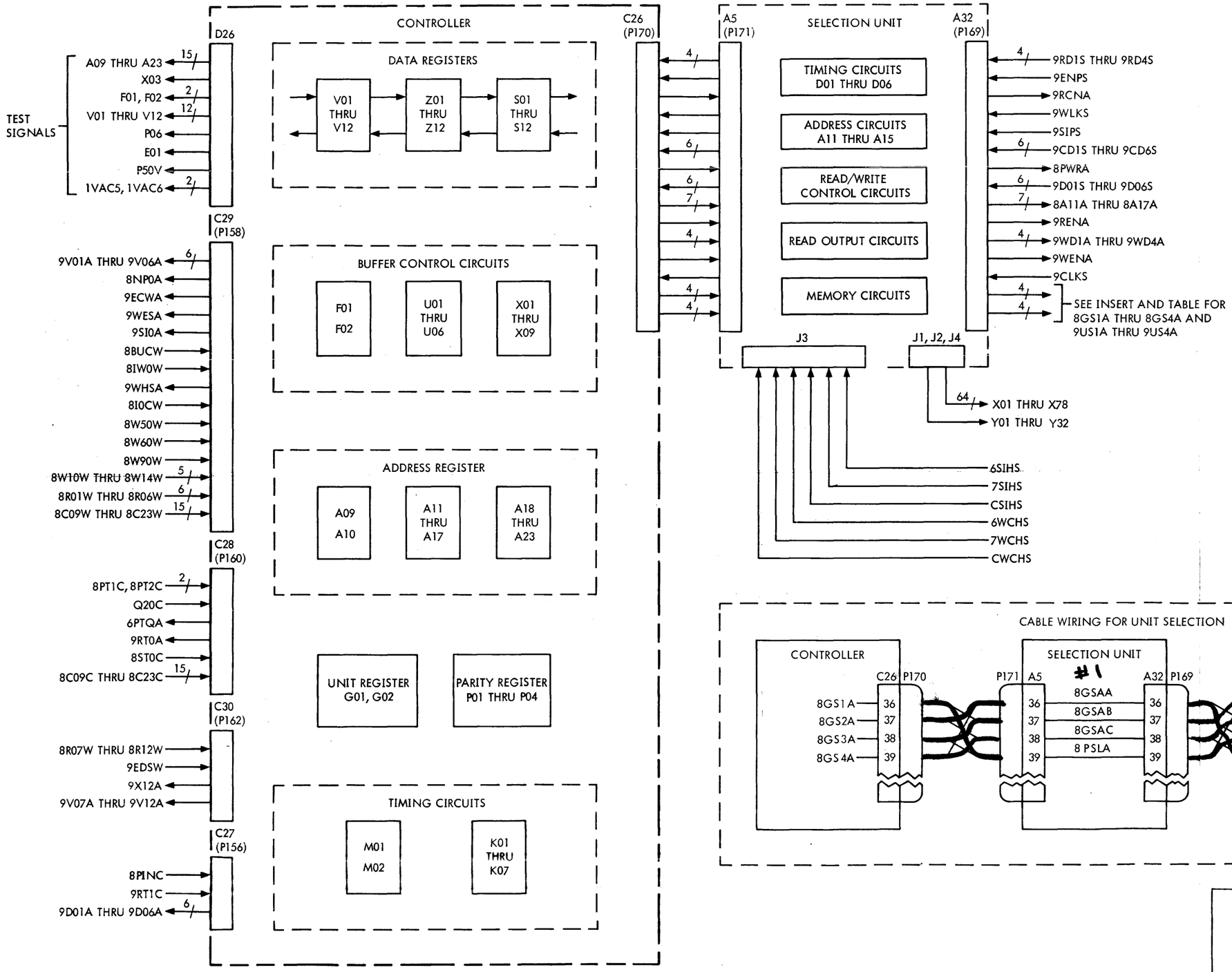
Signals exchanged between the controller and all RAD memory units use a set of lines common to all RAD memory units. To prevent any but the addressed RAD memory unit from controlling or reading signals levels on the common lines, the controller generates two sets of four signals which address the RAD memory units. Two flip-flops in the address register generate four signals which address a RAD memory unit for read or write operations initiated by a POT instruction. The unit register generates four signals which address a RAD memory unit for operations initiated by a PIN instruction. Cable wiring enables each RAD memory unit to interpret one signal from each of these two sets of four as its selection signal. RAD memory units not addressed have no control over common input or output lines. Because selection is established by cable wiring from the controller to a RAD memory unit and from one RAD memory unit to another, two-bit addresses are assigned to RAD memory units simply by connecting the plug module cable assemblies.

The controller and selection unit together form a buffer between data storage devices operating at two independent clock rates. The clock rate of the memory is established by its rotational speed; the clock rate of the computer is established by its timing circuits. When a data transfer takes place, the controller temporarily stores 12-bit codes. Data must be read or written into the memory at its clock rate. During a read operation, the selection unit reads data from four memory outputs at the memory clock rate and transmits data on four outputs to the controller. The controller accepts a 12-bit code every 3 memory clock times and stores the code until the input/output channel can accept the 12-bit codes in parallel. During a write operation the selection unit accepts 12-bit codes 4 bits at a time and writes data on 4 lines. The selection unit uses an encoding method which generates two bits for each data bit received from the controller. This technique permits a higher bit density on magnetic surfaces and is known by a variety of names (such as Manchester, Ferranti, frequency-modulation, modified-non-return-to-zero, and double transition). For either a read or a write operation the controller must exchange data with the computer input/output channel at a rate commensurate with the memory fixed rate and must store 12-bit codes until ready for output to either the computer or selection unit.

The timing circuits include a modulo-3 counter (M01, M02) which counts each group of 3 clock pulses to define the time required to transfer 12-bit codes in 3 groups of 4 bits each. During either read or write operations, the controller processes one sector at a time. Each cycle of the module-3 counter advances the character counter (K01 through K07) which counts the 128 characters of each sector and indicates the end of one write or read process. A sector consists of 1/64 of the data read during a memory revolution.

The data register contains three 12-bit registers (V01 through V12, Z01 through Z12, and S01 through S12). Character codes are stored temporarily in these registers during a data transfer between the memory and computer. During a write operation, data passes from the computer to the V-register, to the Z register, and to the S register. From the S register, the 12-bit codes are transferred to the selection unit 4 bits at a time. During a read operation, the S register accepts 12-bit codes four bits at a time, then transfers 12 bits to the Z register. The Z register transfers the data to the V register, which stores the data until acceptable to the input/output channel.

The address register (A09 through A23) stores a 15-bit code identifying the RAD file location of data to be read or written. At the start of an operation, the address register code indicates the location of the first sector to be processed. Unless the input/output channel disconnects, the address register is counted up by one after each sector is processed.



CONTROLLER	SELECTION UNIT NO. 1	PIN
8GS1A	8GSAA	36
8GS2A	8GSBA	37
8GS3A	8GSCA	38
8GS4A	8PSLA	39
9US1A	9USAA	40
9US2A	9USBA	41
9US3A	9USCA	42
9US4A	9USLA	43

Figure 3-1. RAD File Input and Output Signals Block Diagram

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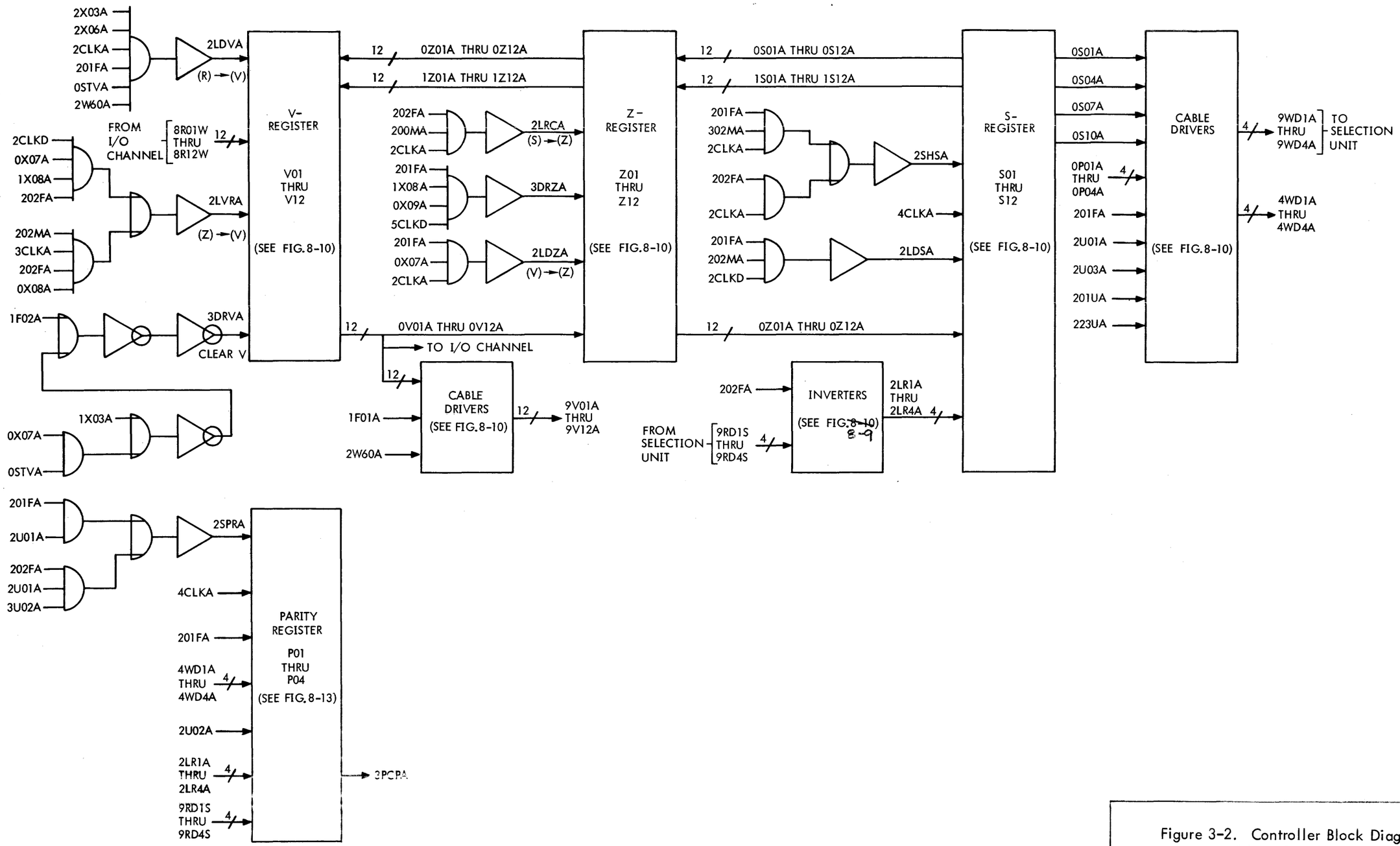

Figure 3-2. Controller Block Diagram
(Sheet 1 of 2)

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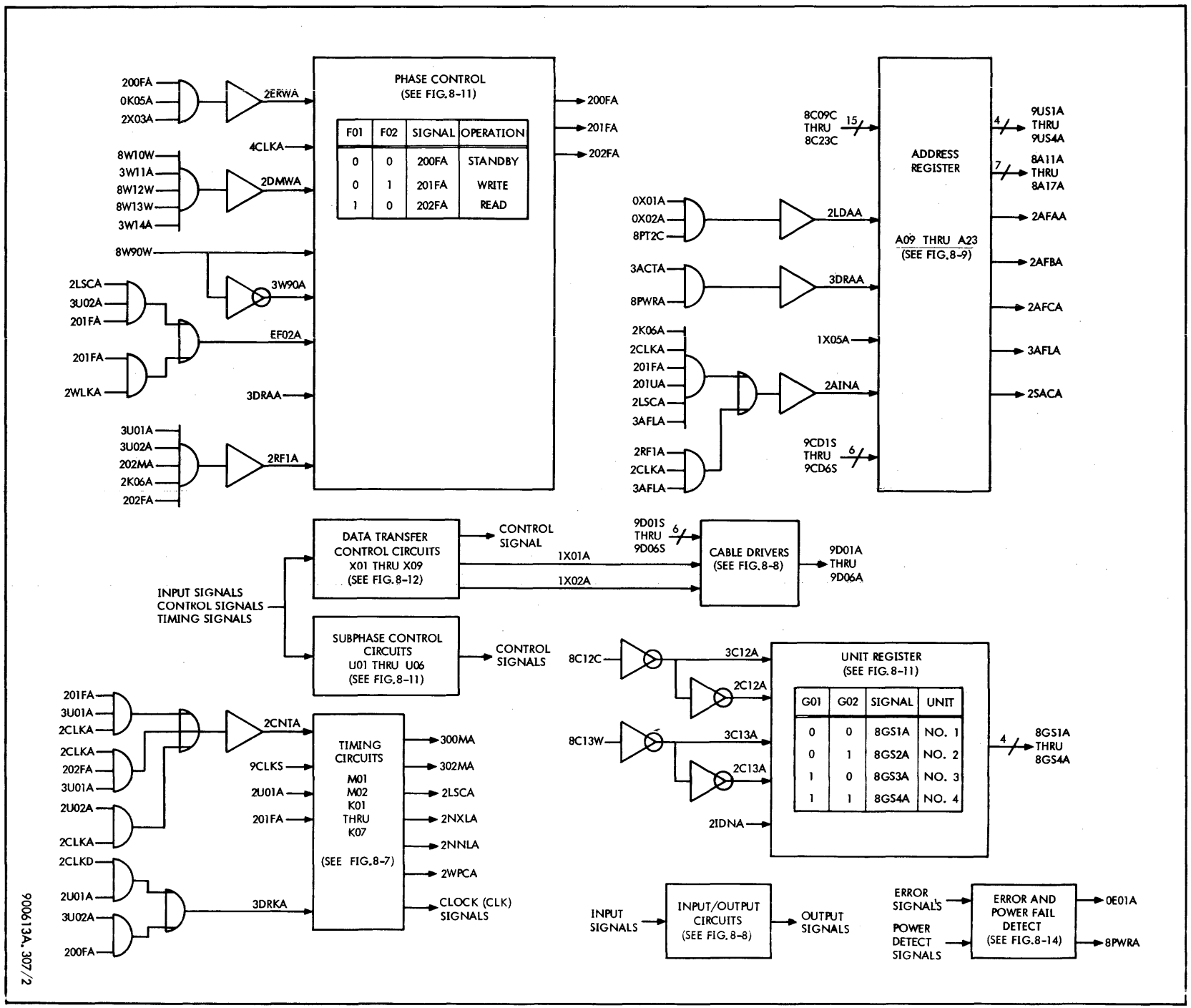


Figure 3-2. Controller Block Diagram (Sheet 2 of 2)

The controller then processes a new sector, if no errors have occurred. This sequence continues until the address register reaches its maximum permissible count, which prevents transfer from the initial RAD memory unit to a new RAD memory unit.

The phase control flip-flops (F01, F02) indicate whether the controller is reading, writing, or waiting for new instructions. The subphase control flip-flops (U01 through U06) control the sequence of events during a read or a write operation. For a write operation, the controller writes sequentially a 10-bit preamble, 128 characters, and parity bits. For a read operation, the controller searches for the preamble, reads the characters, and checks the parity bits. The data transfer control circuits (X01 through X09) control the start of new operations, data transfer during operation, and detection of errors.

The parity flip-flops (P01 through P04) read data passing between the selection unit and controller on the four data lines. For write operations, the parity register generates four parity bits; for read operations, the parity register checks four parity bits.

The selection unit includes the timing circuits, the address circuits, the read/write control circuits, the read output circuits, and the memory circuits. Each selection unit in a RAD file installation receives all controller signals. Only the selection unit addressed by the controller can respond to controller outputs or generate inputs to the controller. The controller can address only one RAD memory unit at a time. A selection unit is activated when the controller addresses the RAD memory unit to begin a write or a read operation, or to determine the sector currently under the read/write heads of the memory circuits.

The timing circuits read permanent timing tracks on the memory, and generate write clock signals, read clock signals, sector signals, and index signals. The memory generates 27,712 clock signals during each revolution. In this interval, data is read from 64 sectors, each of which contains 128 12-bit codes (64 24-bit words) for a total of 98,304 data bits per revolution. These bits are read from 4 lines, each of which stores 24,576 data bits. The difference between 27,712 clock pulses per revolution and 24,576 data bits per revolution is taken up in the parity bit, postamble, and preamble of the sector-to-sector gap.

Each revolution of the memory generates 63 sector pulses and one index pulse. Each sector pulse advances a sector counter which stores the binary code that identifies the sector available at the read/write heads. The sector counter generates two sets of signals. One set is generated to enable the controller to compare data stored in the controller with the code stored in the sector counter. The other set of signals enables the controller to transmit the sector counter code to the computer. The index pulse resets the sector counter once per revolution.

The address signals received from the controller consist of a two-bit track code and a five-bit band code. The two-bit track code selects one four-channel track. The selected four-channel track transmits or receives data from 128 magnetic heads. The five-bit band code selects one of the 32 bands by activating only 4 of the 128 magnetic heads. Address signals are combined with switch-controlled signals to prevent the controller from storing new data in a write-protected band.

The read/write control circuits include 4 write flip-flops, 16 write-drivers, and 16 read/write couplers. Signals originating in the controller enable the read/write coupler to read data from read/write heads and transmit the data to the read output circuits, or to accept data from the write flip-flops and write-drivers and transmit the data to the read/write heads for storage in memory. During a write operation, the write flip-flops accept data from controller inputs, encode the data in modified NRZ format, and pass the encoded data to the write-drivers. The write-drivers store the data in memory through the four read/write couplers selected by the track code.

During a read operation, the read output circuits accept data from selected read/write couplers. The analog data signals pass to a preamplifier and a limiter. The output of the limiter passes through a data decoder which decodes the modified NRZ signal and restores the original data. A clock discriminator extracts the clock signal from the limiter output and generates clock pulses synchronized with the data. The outputs of the data decoder and clock discriminator are inputs to flip-flops. The flip-flops transmit the digital data to the controller through cable drivers.

The memory circuits consist of a matrix of 512 read/write heads from which a set of 4 are selected for read or write operations. The 2-bit track code selects 4 of the 16 read/write couplers, which exchange data with 128 read/write heads. The 5-bit band code activates one of 32 signals. The activated signal grounds 4 of the selected 128 read/write heads. Of the matrix of 512 read/write heads, 4 are selected by a 7-bit address code.

3-3 DETAILED THEORY OF OPERATION

3-4 CONTROLLER

The controller reads computer instruction signals and enables data exchange between the addressed RAD memory unit and the computer through the selection unit (figure 3-2). The controller responds to four types of instructions. The format of each instruction is described in section II. A parallel input (PIN) instruction places the unit register in a state which addresses one of the RAD memory units and causes the state of the selection unit sector counter to be transmitted to the computer as six binary signals. A skip if signal not set (SKS) instruction causes an output of the controller to be sampled to determine if the controller is ready for an output (write), or an input (read) operation. A parallel output (POT) instruction causes data to be stored in the address register. An energize output M (EOM) instruction prepares the controller for a POT or PIN instruction, or causes data write or read in the memory.

The phase control circuits enable the controller to perform a read or write operation, or to wait for instructions. The subphase control circuits establish periods for control of preamble

bits, data bits, or parity bits, and establish waiting periods. The data transfer control circuits cause data to be moved between the V-register, the Z-register, and the S-register, enabling data exchange between storage devices operating at two independent clock rates. The address register identifies the RAD file memory location to be read or written into.

During a write operation, four data bits are transferred from the S-register to the track converter of the selection unit at the clock rate of the memory. As the four data bits are transferred, data is shifted to enable four new data bits to be transferred during the next clock time. Every third clock time, 12 data bits are transferred from the Z-register to the S-register. Data transfer continues at a constant rate while data is written into a sector of the memory. Data from the computer is stored in the V-register and transferred to the Z-register. Each time a data transfer from the V-register to the Z-register takes place, a signal is sent to the computer to enable transfer of new data to the V-register. If the computer fails to keep up with the data transfer rate to the memory, an error is detected. The controller continues to process the current sector, but no new sectors are processed after the current sector is complete.

During a read operation, four data bits are accepted from the track converter of the selection unit at the clock rate of the memory. The four data bits are stored in the S-register each clock time. Every third clock time (after 12 bits have been stored) the 12 bits are transferred from the S-register to the Z-register. Data transfer continues at a constant rate while a sector of the memory is read. When the data is then transferred from the Z-register to the V-register, a signal is sent to the input/output channel. The data must be accepted by the input/output channel and new data transferred from the Z-register to the V-register before data previously stored in the V-register is cleared. If the computer fails to keep pace with the data transfer rate from the memory, the error is detected. The controller continues to process the current sector of data but disconnects from the input/output channel after the sector is processed.

3-5 Timing Circuits

The timing circuits include the modulo-3 counter (flip-flops M01 and M02), the character counter (flip-flops K01 through K07), and associated logic elements (figure 8-7). The timing circuits are controlled by flip-flops F01, F02, U01, U02, and U05, and by signal 9CLKS. Signal 9CLKS – generated in the selection unit under control of the memory – is true 27,712 times for each revolution of the memory (the frequency of the data clock). All clock signals with an odd prefix are at the same logic level as 9CLKS; all clock signals with an even prefix are at the complementary logic level.

The modulo-3 counter repeats the sequence 00, 01, 10, changing state each time signal 2CNTA is true:

$$sM01 = \overline{0M01A}\ 0M02A\ \underline{2CNTA}$$

$$rM01 = \overline{1M01A}\ \underline{2CNTA}$$

$$sM02 = \overline{0M02A}\ 1M01A\ \underline{2CNTA}$$

$$rM02 = \overline{1M02A}\ \underline{2CNTA}$$

Signal 2CNTA is true at the clock rate while U01 is in the reset state during the read phase or the write phase, or when flip-flop U02 is in the set state:

$$2CNTA = 2CLKA\ 3U01A\ 201FA \text{ (write phase)} + 2CLKA\ 3U01A\ 202FA \text{ (read phase)} + 2CLKA\ 2U02A$$

When signal 3DRKA is false, flip-flops M01 and M02 are dc reset. Signal 3DRKA is false during the first clock pulse after flip-flop U01 is set or if flip-flop U02 is in the reset state during the standby phase:

$$zM01 = \overline{3DRKA}$$

$$zM02 = \overline{3DRKA}$$

$$\overline{3DRKA} = 2CLKD\ 2U01A\ 3U02A \text{ (first clock after sU01, or last three clocks of read preamble)} + 200FA\ 3U02A \text{ (standby phase)}$$

The functions of the modulo-3 counter are to define three clock times during which bits are stored in the S-register and to advance the character counter. Signal 00M is true when the modulo-3 counter is in state 00; signal 02M is true when the modulo-3 counter is in state 10:

$$300MA = 200MA$$

$$200MA = 1M01A\ 1M02A$$

$$302MA = 202MA$$

$$202MA = 0M01A$$

The character counter is a binary counter in which flip-flop K07 represents the least significant bit and flip-flop K01 represents the most significant bit. Each flip-flop changes state as the input level of the trigger signal passes from true to false. When signal JK57A is true, flip-flops K05, K06, and K07 advance in normal binary sequence from 000 to 111 each time signal 0M01A changes from true to false (figure 3-3):

$$sK05 = \overline{0K05A}\ \underline{0K06A}\ JK57A$$

$$rK05 = \overline{1K05A}\ \underline{0K06A}$$

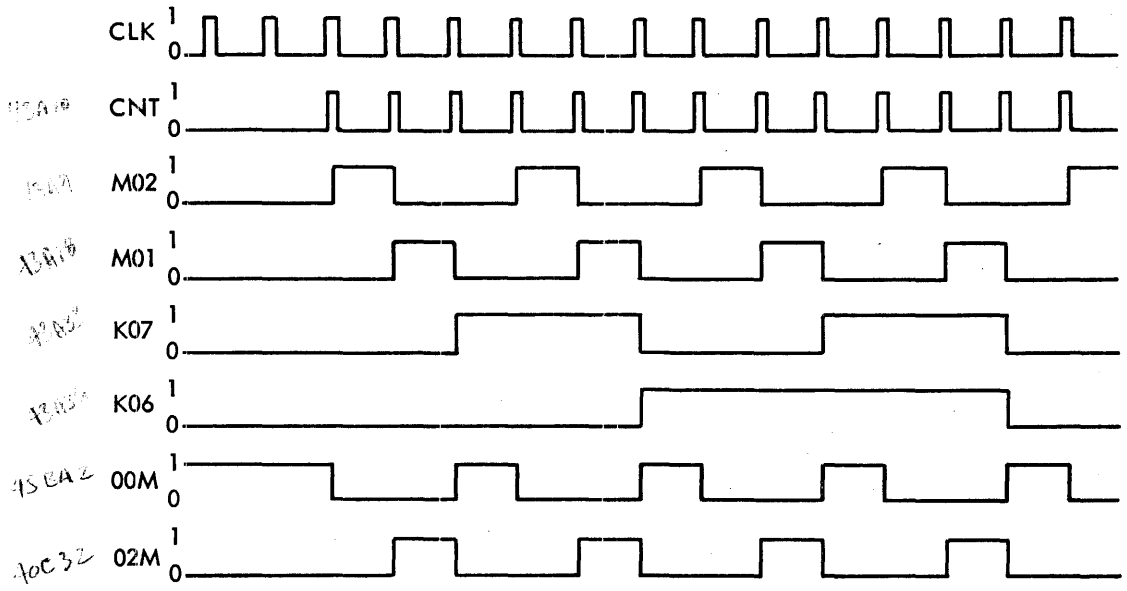
$$sK06 = \overline{0K06A}\ \underline{0K07A}$$

$$rK06 = \overline{1K06A}\ \underline{BK06A}$$

$$sK07 = \overline{0K07A}\ \underline{0M01A}\ JK57A$$

$$rK07 = \overline{1K07A}\ \underline{0M01A}$$

$$BK06A = 2K07A$$



CLOCK*	K04	K05	K06	K07	M01	M02	SIGNAL
1	0	0	0	0	0	0	00M
2	0	0	0	0	0	1	
3	0	0	0	0	1	0	02M
4	0	0	0	1	0	0	00M
5	0	0	0	1	0	1	
6	0	0	0	1	1	0	02M
7	0	0	1	0	0	0	00M
8	0	0	1	0	0	1	
9	0	0	1	0	1	0	02M
10	0	0	1	1	0	0	00M
11	0	0	1	1	0	1	
12	0	0	1	1	1	0	02M
13	0	1	0	0	0	0	00M
14	0	1	0	0	0	1	
15	0	1	0	0	1	0	02M

*STATE WHEN CLOCK N GENERATED

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Figure 3-3. Controller Timing Signals Timing Diagram

During the write phase, signal BK06A is true and signal JK57A is false after flip-flop U01 is set:

BK06A = 201FA 2U01A 0M01A

$\overline{JK57A}$ = 201FA 2U01A 2K06A

thereby causing these flip-flops to count through the sequence 000, 001, 010, 000 each time signal 0M01A is true.

Each time flip-flops K05 through K07 attain a count of 111, the four-bit counter consisting of flip-flops K01 through K04 is triggered through signal 2LSCA:

sK01 = $\overline{0K01A}$ 0K02A

rK01 = $\overline{1K01A}$ 0K02A

sK02 = $\overline{0K02A}$ 0K03A

rK02 = $\overline{1K02A}$ 0K03A

sK03 = $\overline{0K03A}$ 0K04A

rK03 = $\overline{1K03A}$ 0K04A

sK04 = $\overline{0K04A}$ 0K05A 2K06A 2LSCA 2CNTA

rK04 = $\overline{1K04A}$ 0K05A 2K06A 2LSCA 2CNTA

2LSCA = 0M01A 2K07A (every sixth clock)

When signal JK57A is true, the character counter advances in binary sequence from 0 000 000 to 1 111 111. A true 2NNLA signal is generated when the character counter reaches 1 111 100; a true 2NXLA signal is generated when the character counter reaches 1 111 110. The character counter is cleared by a false 3DRKA signal, resetting K01 by an input to the set output:

NXL = K06 NNL (next-to-last character)

$\overline{NNL}$ = K05 K04 K03 K02 K01

3-6 Data Register

The data register includes the V-register (flip-flops V01 through V12), the Z-register (flip-flops Z01 through Z12), the S-register (flip-flops S01 through S12), and associated logic elements (figure 8-8). During read operations, data bits are passed from the S-register to the Z-register to the V-register. During write operations the sequence is reversed.

3-7 Data Flow During Write Operation

During a write operation, the V-register is first cleared by a false 3DRVA signal:

zV01 = $\overline{3DRVA}$

⋮ ⋮

zV12 = $\overline{3DRVA}$

Signal 3DRVA is controlled by F02, X03, and signal 6DRVA. When the controller is in the read phase (F02 reset), signal 3DRVA is held at the true level to prevent interference with data transfer from the Z-register:

3DRVA = $\overline{2DRVA}$

$\overline{2DRVA}$ = 1F02A

When the controller is in the write phase (F02 set) and connected for operation (X03 set), signal 3DRVA is controlled by signal 6DRVA:

6DRVA = X06 $\overline{W50}$ W60 $\overline{CLK}$

thereby enabling clearing of the V-register just before data is accepted from input/output lines R01 through R12 (refer to paragraph 3-19).

When signal LDV is true, data is stored in the V-register through direct set inputs:

yV01 = LDV R01

⋮ ⋮

yV12 = LDV R12

LDV = 01F X03 X06 W60 STV CLK

Signal STV is a short-duration clock that strobes the data into the V-register. The function of signals X06 and W60 are described in paragraph 3-19. After the data is stored in the V-register, the Z-register is cleared:

zZ01 = $\overline{DRZ}$

⋮ ⋮

zZ12 = $\overline{DRZ}$

$\overline{DRZ}$ = 01F X03 X09 $\overline{CLK}$

and the contents of the V-register transferred to the Z-register:

yZ01 = LDZ V01

⋮ ⋮

yZ12 = LDZ V12

LDZ = 01F X07 CLK

The contents of the Z-register are transferred to the S-register at each 02M clock:

yS01 = LDS Z01

⋮ ⋮

yS12 = LDS Z12

LDS = 01F 02M CLK

and transmitted from the S-register to the selection unit by signals WD1 through WD4.

3-8 S-Register Operation

The S-register consists of four groups of identical circuits each containing three flip-flops. During a write operation, 12 bits of data are transferred from the Z-register to the S-register at each 02M clock and read from flip-flops S01, S04, S07, and S10 by signals WD1 through WD4:

$\overline{9WD1A}$ = 4WD1A 201FA
⋮ ⋮
$\overline{9WD4A}$ = 4WD4A 201FA
4WD1A = 223UA 0S01A
4WD2A = 223UA 0S04A
4WD3A = 223UA 0S07A
4WD4A = 223UA 0S10A
223UA = 1U01A 0U02A

After the first bit is read from flip-flop S01, additional bits are shifted from S02 and S03 on successive clock times:

sS01 = S02 SHS CLK
rS01 = $\overline{S02}$ SHS CLK
sS02 = S03 SHS
rS02 = $\overline{S03}$ SHS
SHS = 01F $\overline{02M}$ CLK

A false LR1 signal shifts zeros into S03:

rS03 = $\overline{LR1}$ SHS

so that the S-register is cleared in preparation for the next 02M clock which shifts new bits from the Z-register. In a similar manner, the other three groups of the S-register shift three bits of data to the selection unit.

During a read operation, data is shifted into the S-register from selection unit outputs:

2LR1A = 202FA 2RD1A
⋮ ⋮
2LR4A = 202FA 2RD4A
2RD1A = $\overline{9RD1S}$
⋮ ⋮
2RD4A = $\overline{9RD4S}$

This data is accepted by flip-flops S03, S06, S09, and S12 at a clock rate established by the selection unit:

sS03 = LR1 SHS
rS03 = $\overline{LR1}$ SHS
⋮ ⋮
sS12 = LR4 SHS
rS12 = $\overline{LR4}$ SHS
SHS = 02F CLK

Each group of S-register flip-flops continually shift data at the clock rate established by the selection unit:

sS02 = S03 SHS
rS02 = $\overline{S03}$ SHS
sS01 = S02 SHS CLK
rS01 = $\overline{S02}$ SHS CLK

In a similar manner, the other three groups of S-register flip-flops accept data from the selection unit and continually transfer the data to load 12 bits into the S-register before data transfer to the Z-register.

3-9 Data Flow During Read Operation

During a read operation, data is shifted in the S-register at a clock rate established by the selection unit and transferred to the Z-register at each 00M clock:

sZ01 = S01 LRC
rZ01 = $\overline{S01}$ LRC
⋮ ⋮
sZ12 = S12 LRC
rZ12 = $\overline{S12}$ LRC
LRC = 02F 00M CLK

The contents of the Z-register are transferred to the V-register under control of flip-flops X06 through X09, (refer to paragraph 3-20). Transfer must take place at least once during each 3-clock interval to keep pace with the S-register and the Z-register:

sV01 = LVR Z01
rV01 = LVR $\overline{Z01}$
⋮ ⋮
sV12 = LVR Z12
rV12 = LVR $\overline{Z12}$
LVR = 02F X08 00M $\overline{CLK}$
+ 02F X07 $\overline{X08}$ CLK

The contents of the V-register are transmitted to the input/output channel from signals 9V01A through 9V12A under control of signal W60 generated in the input/output channel:

$\overline{9V01A}$ = 0V01A 2W56A 1F01A
⋮ ⋮
$\overline{9V12A}$ = 0V12A 2W56A 1F01A
2W56A = $\overline{2W50A}$ 3W60A

Signal 1F01A enables control by the V-register during the read operation and causes all output signals to be true during write or standby.

3-10 Address Register

The address register (A-register) includes flip-flops A09 through A23 and associated logic elements (figure 8-9). All flip-flops of the A-register are reset during standby phase (signal 200FA true) if a new address is to be loaded:

zA09 = $\overline{3DRAA}$
⋮ ⋮
zA23 = $\overline{3DRAA}$
$\overline{3DRAA}$ = $\overline{3ACTA}$ 8PWRA
$\overline{3ACTA}$ = 200FA 0U06A 1X03A (new POT operation)

After the A-register is cleared, a new address is loaded from signals 8C09C through 8C23C when signal 2LDAA is true:

yA09 = 2LDAA 8C09C
yA10 = 2LDAA 8C10C
⋮ ⋮
yA23 = 2LDAA 8C23C

2LDAA = 0X01A 0X02A 8PT2C (POT operation)

The A-register is a binary counter in which flip-flop A23 represents the least significant bit and flip-flop A09 represents the most significant bit. The number increases in binary sequence from whatever number is initially stored to XXX 111 111 111 111, in which XXX represents the states of flip-flops A09 through A11. Changes of state of A09 or A10 imply transfer from one RAD memory unit to another. This function is not allowed during a read or write operation. Advance of the binary counter is controlled by signal 2AINA which is true each time an exit from a sector-read or sector-write operation takes place. Advance of the binary counter thus indicates that data has been read or written into one sector of memory.

Flip-flop A23 changes state each time signal 2AINA is true:

sA23 = 0A23A 2AINA
rA23 = 1A23A 2AINA

Signal 2AINA is true after the character counter reaches a maximum value in either the read or the write phase:

2AINA = 201FA 201UA 2LSCA 3AFLA 2K06A 2CLKA (write)
+ 2RF1A 3AFLA 2CLKA (read)
2RFLA = 202FA 3U01A 3U02A 2K06A 202MA

Signal 3AFLA is true until the A-register reaches maximum count:

$\overline{3AFLA}$ = 2AFAA 2AFBA 2AFCA
2AFAA = 0A12A 0A13A
2AFBA = 0A14A 0A15A 0A16A 0A17A
2AFCA = 0A18A 0A19A 0A20A 0A21A 0A22A 0A23A 1X05A

Signal 1X05A inhibits a true 2AFCA signal if the non-increment mode is established.

Signal AIN is equivalent to:

AIN = 02F $\overline{AFL}$ CLK $\overline{U01}$ $\overline{U02}$ 02M K06 (read)
+ 01F $\overline{AFL}$ CLK $\overline{U01}$ $\overline{U02}$ 02M K06 K07 (write)

After the last character is read or written, flip-flops (U01, U02) are placed in state (0, 0) for the postamble phase. Signal AIN is then controlled by timing circuit flip-flops representing the least significant bits of the count (K06, K07, M01, M02). The parity bit is read or written immediately after entry into the postamble phase as the timing circuit flip-flops change from state (0, 0, 0, 0) to state (0, 0, 0, 1). For the read operation, signal AIN becomes true at the eighth clock after the parity bit when the flip-flops are in state (1, 0, 0, 1). For the write operation, signal AIN becomes true at the eleventh clock after the parity bit when the flip-flops are in state (1, 1, 0, 1).

Flip-flops A18 through A22 advance in binary sequence each time flip-flop A23 passes from the set to the reset state:

sA22 = $\overline{0A22A}$ 0A23A
rA22 = $\overline{1A22A}$ 0A23A
sA21 = $\overline{0A21A}$ 0A22A
rA21 = $\overline{1A21A}$ 0A22A
⋮ ⋮
sA18 = $\overline{0A18A}$ 0A19A
rA18 = $\overline{1A18A}$ 0A19A

Each time flip-flops A18 through A23 reach a count of 111 111, a true 2AFCA signal signal toggles flip-flop A17 if flip-flop X05 is in the reset state:

$$sA17 = \overline{0A17A}\ 2AFCA\ \underline{2AINA}$$
$$rA17 = \overline{1A17A}\ 2AFCA\ \underline{2AINA}$$

When flip-flop X05 is set to establish the non-increment mode of operation, the controller enables the computer to read or write into the same sector on two consecutive passes. This feature permits faster operation in some circumstances, as described in section II.

Flip-flops A14 through A16 are connected to form a modulo-8 counter in the same manner as flip-flops A18 through A22 form a modulo-32 counter. Each time flip-flops A14 through A17 reach a count of 1111, a true 2AFBA signal is generated. When flip-flops A14 through A23 attain a count of 1 111 111 111, flip-flop A13 is toggled to advance the modulo-32 counter formed by flip-flops A09 through A13. When flip-flops A12 through A23 are in the set state, signals AFA, AFB, and AFC are true if flip-flop X05 is in the reset state. These signals generate a false AFL signal, inhibiting signal AIN and preventing further incrementing of the address register.

A true sector address compare (SAC) signal is generated when signals A18 through A23 are identical to signals 9CD1S through 9CD6S. Signals CD1 through CD6 represent the state of the sector counter in the selection unit:

$$SAC = (\overline{A18\ \overline{CD1}})\ (\overline{\overline{A18}\ CD1})\ (\overline{A19\ \overline{CD2}})$$
$$(\overline{\overline{A19}\ CD2})\ (\overline{A23\ \overline{CD6}})\ (\overline{\overline{A23}\ CD6})$$

3-11 Parity Circuits

The parity circuits consist of flip-flops P01 through P04 and associated logic elements (figure 8-13). Flip-flops P01 through P04 are direct set at the start of a read or a write operation:

$$yP01 = SPR$$
$$\vdots \qquad \vdots$$
$$yP04 = SPR$$
$$SPR = 01F\ U01 \text{ (write phase)}$$
$$+\ 02F\ U01\ \overline{U02} \text{ (read phase)}$$

During a write operation, each flip-flop changes state each time a one is written into disc memory from the S-register:

$$sP01 = 01F\ WD1\ \underline{CLK}$$
$$rP01 = 01F\ WD1\ \underline{CLK}$$
$$\vdots \qquad \vdots$$
$$sP04 = 01F\ WD4\ \underline{CLK}$$
$$rP04 = 01F\ WD4\ \underline{CLK}$$
$$WD1 = 23U\ S01$$
$$WD2 = 23U\ S04$$
$$WD3 = 23U\ S07$$
$$WD4 = 23U\ S10$$
$$23U = \overline{U01}\ U02$$

After all characters have been written, each flip-flop is in the set state if an even number of ones have been written and in the reset state if an odd number of ones have been written.

After the last character has been written, parity bits are written by transferring the contents of flip-flops P01 through P04 to memory:

$$WD1 = 01U\ P01$$
$$\vdots \qquad \vdots$$
$$WD4 = 01U\ P04$$
$$01U = \overline{U01}\ \overline{U02}$$

After the parity bits are written, an 11-bit postamble of all zeros is written on each track.

During a read operation, each flip-flop changes state each time a one is read from memory into the S-register:

$$sP01 = LR1\ U02\ \underline{CLK}$$
$$rP01 = LR1\ U02\ \underline{CLK}$$
$$\vdots \qquad \vdots$$
$$sP04 = LR4\ U02\ \underline{CLK}$$
$$rP04 = LR4\ U02\ \underline{CLK}$$
$$LR1 = 02F\ RD1$$
$$\vdots \qquad \vdots$$
$$LR4 = 02F\ RD4$$

After the last character has been read, signal PCP compares the parity of flip-flops P01 through P04 with the parity bits read from memory and generates an error signal if the two sets are not identical:

$$WES = 02F\ \overline{PCP}\ \overline{K06}\ \overline{K07}\ \overline{U01}\ \overline{U02}\ 00M\ \underline{CLK}$$
$$\overline{PCP} = \overline{P01}\ LR1$$
$$+\ P01\ \overline{RD1}$$
$$\vdots$$
$$+\ \overline{P04}\ LR4$$
$$+\ P04\ \overline{RD4}$$

3-12 Buffer Control Circuits

The buffer control circuits consist of phase control, subphase control, and data transfer control circuits (figures 8-10 through 8-12). For a read or a write operation, data is exchanged between the computer and RAD file, each of which operate at different clock rates. To enable data exchange, the buffer control circuits identify computer instruction codes, define the start and finish of the data transfer process, monitor the generation and reading of parity bits, and indicate errors of programming, timing, or data transfer.

Read and write operations are initiated by SKS, EOM, and POT instructions from the computer as described in section II. These instructions store an address in the A-register, connect the controller to the input/output channel, and enable transfer from the standby phase to either the read or the write phase (figure 3-4). Once a read or write operation is begun, the controller returns to standby after processing 128 12-bit codes. If the process is complete, the controller is disconnected and remains in standby; if the process is not complete, the controller returns to read or write to complete the operation.

For a PIN (parallel input) operation, the contents of the sector counter in the selection unit are sampled and the data passed through the controller to the input/output channel.

3-13 Start of Read or Write Operation

If the RAD file is addressed by the computer, the contents of the computer C-register generate a true DMA signal:

$$DMA = \overline{C17}\ C19\ \overline{C20}\ C21\ C22\ \overline{C23}$$

While the RAD file is addressed, signal SIO may be sampled by an SKS instruction to determine if the controller is ready as indicated by a false SIO signal:

$$SIO = DMA\ \overline{C13}\ C14\ \overline{E01}\ (SKS\ 11026)\ \text{ERROR}$$
$$+ DMA\ C13\ C14\ \overline{WLK}\ (SKS\ 13026)\ \text{WRITE PROTECT}$$
$$+ DMA\ \overline{C13}\ \overline{C14}\ \overline{X03}\ PUF\ (SKS\ 10026)\ \text{READY}$$
$$PUF = 00F\ (standby\ phase)$$
$$+ \overline{U01}\ \overline{U02}\ (postamble)$$

Signal E01 indicates a processing error; signal WLK indicates a write-protected address stored in the A-register. If signal SOI is sampled as part of the program (as indicated in table 2-3), the controller will be connected by the instructions which follow. If this signal is not sampled, the controller may not be ready when the instructions are read and may disconnect.

If the RAD file is addressed while the computer is in the input/output control mode, flip-flop U06 is set:

$$IDT = DMA\ IOC\ \overline{C16}\ (alert\ to\ POT)$$
$$sU06 = IDT$$

Subsequent events are controlled by the PT1 and PTQ signals, generated while the computer is in the wait phase of the POT instruction. Signal PT1 is true throughout the POT wait phase. Signal PTQ is generated on a circuit card of a plug module cable assembly and is true periodically during the POT wait phase:

$$PTQ = PT1\ Q20$$

If the controller is in the standby phase when flip-flop U06 is set, X01 is set when the PT1 signal is true:

$$sX01 = U06\ NUF\ \underline{PTQ}$$
$$NUF = 00F\ (standby\ phase)$$
$$+ \overline{U01}\ \overline{U02}\ (not\ postamble\ of\ write\ phase)$$

and a true RT0 signal is generated to enable the computer to leave the POT wait phase after a time delay:

$$RT0 = X01\ PT1$$

At the same time, a true ACT signal is generated:

$$ACT = 00F\ U06\ \overline{X03}$$

and a false DRA signal clears the A-register in preparation for a new address:

$$\overline{DRA} = \overline{ACT}\ PWR$$

After flip-flop X01 is set, flip-flop X02 is direct set:

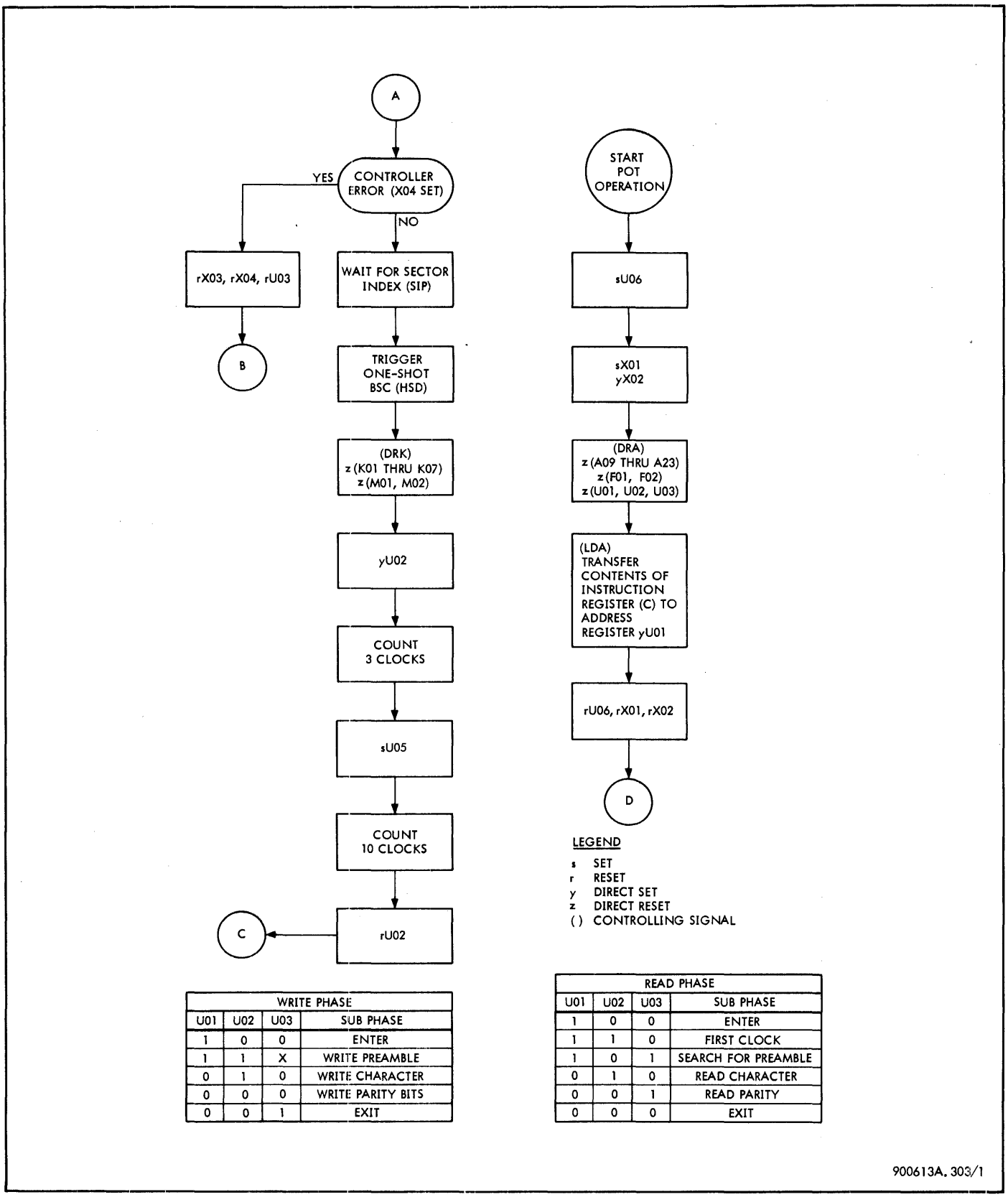
$$yX02 = 00F\ X01\ \overline{X03}$$

and a true LDA signal loads the new address into the A-register and sets flip-flop U01:

$$LDA = X01\ X02\ PT2$$
$$yU01 = LDA$$

since flip-flops U01, U02, U03, F01, and F02 were reset when the A-register was cleared:

$$zU01 = \overline{DRA}$$
$$zU02 = \overline{DRA}$$
$$zU03 = \overline{DRA}$$
$$zF01 = \overline{DRA}$$
$$zF02 = \overline{DRA}$$



WRITE PHASE			
U01	U02	U03	SUB PHASE
1	0	0	ENTER
1	1	X	WRITE PREAMBLE
0	1	0	WRITE CHARACTER
0	0	0	WRITE PARITY BITS
0	0	1	EXIT

READ PHASE			
U01	U02	U03	SUB PHASE
1	0	0	ENTER
1	1	0	FIRST CLOCK
1	0	1	SEARCH FOR PREAMBLE
0	1	0	READ CHARACTER
0	0	1	READ PARITY
0	0	0	EXIT

Figure 3-4. Controller Operation Simplified Flow Diagram (Sheet 1 of 2)

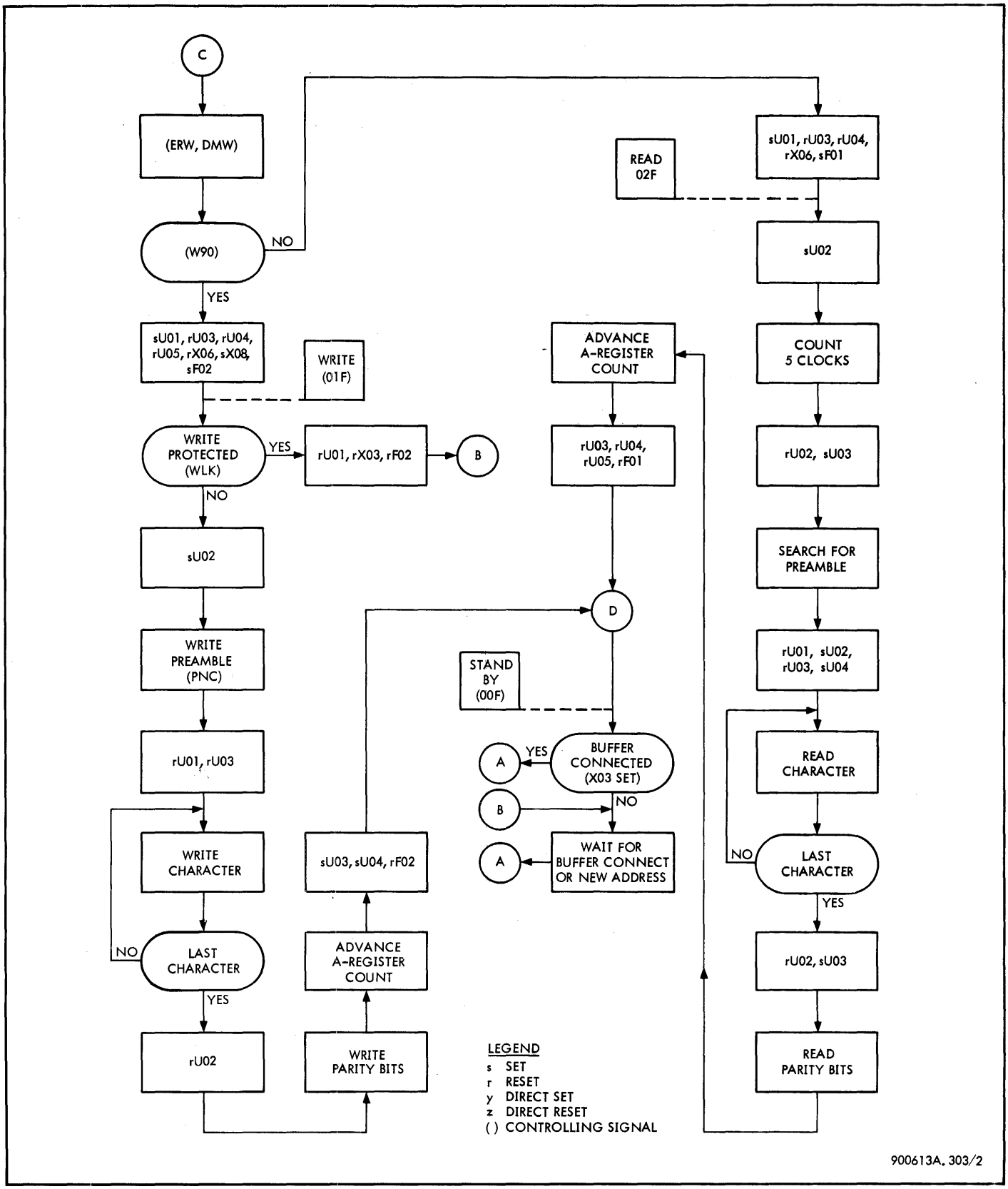


Figure 3-4. Controller Operation Simplified Flow Diagram (Sheet 2 of 2)

The next time signal PTQ is true, flip-flops U06, X01, and X02 are reset:

rU06 = X01 PTQ

rX01 = NUF PT1

rX02 = BX02A

BX02A = 2PT1A

Flip-flop X03 is set when buffer connect signal BUC is generated by the computer:

sX03 = 00F BUC DMA

If the controller is in the postamble of the write phase when flip-flop U06 is set, X01 is not set until the controller enters standby and operations continue as previously described. If the controller is not in standby or the postamble phase when flip-flop U06 is set, flip-flop X01 is set when the controller enters standby. The error flip-flop however, is direct set by the next PT2 signal:

yE01 = X01 $\overline{X02}$ PT2

3-14 Phase Control

Flip-flops F01 and F02 of the phase control circuits establish the three main phases (standby, read, or write). During standby, both flip-flops are in the reset state, and signal 00F is true:

200FA = 1F01A 1F02A

For a transfer from standby, signals ERW and DMW must be true, causing either F01 or F02 to be set:

sF01 = 2ERWA 2DMWA 3W90A 4CLKA
(enter read phase)

sF02 = 2ERWA 2DMWA 8W90W 4CLKA
(enter write phase)

3W90A = $\overline{8W90A}$

Signal DMW is controlled by the input register of the input/output channel and is true when the RAD file is addressed:

DMW = W10 $\overline{W11}$ W12 W13 $\overline{W14}$

Signal DMW may also generate a false X12 signal to indicate exchange of 12-bit codes, an NP0 signal, and a WHS signal:

$\overline{X12}$ = DMW

NP0 = DMW $\overline{F01}$

$\overline{WHS}$ = $\overline{X03}$ $\overline{BUC}$ 00F DMW

Signal W90 indicates if the RAD file is addressed for input to the computer from the RAD file (octal 26, read), or for output from the computer to the RAD file (octal 66, write), and determines whether F01 or F02 is set. Signal ERW is true after a timing interval, as described subsequently.

Signal 01F is true during the entire write phase; signal 02F is true during the entire read phase:

01F = $\overline{F01}$ F02 (write phase)

02F = F01 $\overline{F02}$ (read phase)

The read or the write phase is entered each time data is to be exchanged between the computer and memory. After a full sector of 128 12-bit characters is processed, a return to the standby phase takes place:

rF01 = RF1 CLK

RF1 = 02F $\overline{U01}$ $\overline{U02}$ 02M K06 (exit from read phase)

rF02 = 01F $\overline{U02}$ LSC K06 CLK (exit from write phase)

LSC = M01 K07

As transfer to the read or the write phase takes place, other flip-flops are set or reset to establish initial conditions:

sU01 = ERW CLK

rU02 = 00F K05 CLK

rU03 = ERW CLK

rU04 = ERW 00F

rU05 = ERW DMW W90 CLK (write only)

rX06 = ERW CLK

sX08 = ERW DMW W90 CLK (write only)

3-15 Transfer From Standby Phase (See figure 3-4)

Transfer from standby can occur only if flip-flop X03 is in the set state, indicating that the controller is connected. Flip-flop X03 is initially set when buffer connect signal BUC is generated by the computer after the RAD file is addressed:

sX03 = 00F BUC DMA

and may be reset if a rate error occurs during a read or write operation (if the controller is disconnected by the computer, or if the sector addressed is write-protected):

rX03 = 00F X04 CLK (rate error)

+ 01F WLK CLK (write-protected)

+ $\overline{U01}$ EDS CLK (DACC count 4, SDS 940 only)

+ $\overline{U01}$ $\overline{DMW}$ CLK (RAD not addressed)

Once X03 is set (indicating that the controller is connected), a search is begun for the addressed sector at the direct set input to U02. Flip-flop U02 is set when a new address is stored (HSD), the sector index pulse from the selection unit (SIP) indicates the start of a sector, and the sector address compares with the address stored in the A-register (SAC). When all these conditions are true, one-shot BSC is triggered:

BSC = 00F SIP HSD

HSD = U01 $\overline{X01}$

yU02 = 00F BSC SAC HSD

Before U02 is set, the timing counters are cleared; after U02 is set, the counters begin counting clock signals through signal CNT:

DRK = 00F U02 (clear counters)

CNT = U02 CLK (count clock signals)

If the buffer is not connected when sector address compare occurs, an INT signal is generated. This signal may be used as a priority interrupt:

INT = 00F SAC BUC X01 $\overline{X03}$ U01

After three clock pulses, U05 is set, and a false REN signal is generated:

sU05 = 00F U02 K07 00M

$\overline{REN}$ = U05

After 10 additional pulses, K05 is set, enabling a true ERW signal to reset U02 and causing transfer to either the write or the read phase:

ERW = 00F K05 X03

rU02 = 00F K05 CLK

The timing sequence that occurs between the sector index pulse and exit from standby takes place following each exit from either the read or the write phase provided the controller is still connected (X03) and the maximum A-register count was not reached during the previous read or write operation ($\overline{U03}$):

HSD = $\overline{U03}$ X03

Bit 14 of the computer command distinguishes between the increment mode and the non-increment mode. For the non-increment mode, X05 is set:

sX05 = IDT PUF $\overline{X03}$ C14

rX05 = IDT PUT $\overline{X03}$ $\overline{C14}$

PUF = 00F (standby phase)

+ $\overline{U01}$ $\overline{U02}$ (postamble of write phase)

When X05 is set, the A-register cannot count beyond state XXX XXX XXX 111 111, because signal AFC (which cannot be true) prevents a change of state of A17:

AFC = A18 A19 A20 A21 A22 A23 $\overline{X05}$

sA17 = AFC $\overline{A17}$ AIN

rA17 = AFC A17 AIN

After data has been transferred from the band, the address register is not incremented and exit from standby is permitted if no errors have occurred ($\overline{E01}$):

HSD = $\overline{U01}$ X05 $\overline{E01}$

The controller then processes data from the same band. This function of the controller is used for fast access operation (refer to section II).

3-16 Write Cycle (See figure 3-4)

Once the controller enters the write phase, the controller processes 128 12-bit characters unless the location addressed is write-protected. During the write cycle, the controller first establishes that the location is not write-protected, then writes a preamble to identify the data for readout. After the preamble is generated, the controller accepts 12-bit characters from the input/output channel at its clock rate, and writes data into memory at the memory clock rate. After the data is written, a parity bit is generated for each of the four outputs and the controller returns to the standby phase. The operations of flip-flops X06 through X09 to control the data transfer process are described subsequently. The logic which enables data flow from the input/output channel to the V-register, Z-register, S-register, and selection unit is described in paragraph 3-7.

3-17 Write Order of Operations

Immediately after entering the write phase, write lockout signal WLK from the selection unit is sampled to determine if the location addressed is write-protected. If the location is write-protected, a true WLK signal causes return to the standby phase:

rF02 = 01F WLK CLK

rU01 = 01F WLK CLK

rX03 = 01F WLK CLK

If the location is not write-protected, a false WLK signal sets U02 to begin the write preamble phase:

sU02 = 01F U01 $\overline{WLK}$ CLK

The preamble is written by output signals WD1 through WD4

$\overline{9WD1A}$ = 01F U01 U03

⋮ ⋮

$\overline{9WD4A}$ = 01F U01 U03

which are transmitted to the selection unit. Flip-flop U03 changes state each clock time to write the 10-bit preamble (0101010100):

sU03 = 01F U01 PNC CLK $\overline{\text{U03}}$

rU03 = 01F U01 PNC CLK U03

Signal PNC is true for the first 7 counts of the modulo-3 counter and character counter. However, the timing counters do not start counting until U02 is set. The write preamble therefore is an alternating pattern of zeros and ones until the eighth bit, when signal PNC becomes false. After two additional counts, signal WPC is true, ending the write preamble operation:

rU01 = 01F WPC CLK

WPC = U01 K06 02M

While characters are written, flip-flops U01 and U03 are in the reset state and flip-flop U02 is set. The outputs of the S-register are transmitted from signals WD1 through WD4 to the selection unit:

$\overline{\text{9WD1A}}$ = 01F 23U S01

$\overline{\text{9WD2A}}$ = 01F 23U S04

$\overline{\text{9WD3A}}$ = 01F 23U S07

$\overline{\text{9WD4A}}$ = 01F 23U S10

23U = $\overline{\text{U01}}$ U02

The details of this process are described in paragraph 3-8. A character is written during the three clock periods required to shift data from the S-register. After each character is written, the character counter is advanced:

CNT = 01F $\overline{\text{U01}}$ CLK

When the last character has been written, flip-flop U02 is reset:

rU02 = 01F NXL LSC CLK

NXL = K01 K02 K03 K04 K05 K06

LSC = K07 M01

thereby inhibiting data transfer from the S-register and enabling the parity bits to be written:

$\overline{\text{WD1}}$ = 01F 01U P01

$\overline{\text{WD2}}$ = 01F 01U P02

$\overline{\text{WD3}}$ = 01F 01U P03

$\overline{\text{WD4}}$ = 01F 01U P04

01U = $\overline{\text{U01}}$ $\overline{\text{U02}}$

As the parity bits are written, transfer from the write to the standby phase takes place and the A-register is incremented. After the parity bits are written, an 11-bit postamble of all zeros is written on each track. The A-register cannot be incremented if in state XXX 111 111 111 111 for in this case AFL is true:

AIN = 01F 01U K06 LSC $\overline{\text{AFL}}$ CLK

rF02 = 01F $\overline{\text{U02}}$ LSC CLK

sU03 = 01F $\overline{\text{U02}}$ LSC AFL CLK

sU04 = 01F NNL K07 02M CLK

NNL = K01 K02 K03 K04 K05

LSC = K07 M01

Flip-flop U03 is set only if the A-register has reached maximum count so that return to the write phase is not allowed.

If the controller is still connected (X03 set) and the A-register has not reached its maximum count (U03 reset), signal HSD is true to begin the timing sequence which returns the controller to standby (refer to paragraph 3-15):

HSD = X03 $\overline{\text{U03}}$

3-18 Read Cycle (See figure 3-4)

Once the controller enters the read phase, the controller processes 128 12-bit characters. During the read cycle, the controller first searches for the preamble which identifies the start of data, then reads the characters from selection unit output. After all characters have been read, the parity of the data read from memory is compared with the output of the parity register. The operations of flip-flops X06 through X09 to control the data transfer process are described subsequently. The logic which enables data flow from the selection unit to the S-register, Z-register, V-register, and the input/output channel is described in paragraphs 3-9 and 3-10.

3-19 Search, Read, Check Operations

Flip-flop U02 is set one clock time after the controller enters the read phase:

sU02 = 02F U01 $\overline{\text{U03}}$ 00M CLK

enabling the timing counters to advance on each clock:

CNT = U02 CLK

After five additional clock times, U02 is reset and U03 is set:

rU02 = 02F U01 K07 02M CLK

sU03 = 02F U01 U02 K07 02M CLK

and a search for the preamble is begun. The timing counters are cleared:

DRK = $\overline{U02}$ U01 CLK

and count signal CNT is inhibited until U01 is reset:

CNT = 02F $\overline{U01}$ CLK

The preamble double zero is detected by a zero in S03 while a zero is read from signal RD1:

sU02 = 02F U01 U03 $\overline{RD1}$ $\overline{S03}$ CLK

as data from the selection unit is shifted into the S-register. One clock time after detection of the double zero, U01 is reset, enabling the timing counter:

rU01 = 02F U02 U03 CLK

Flip-flop U03 changes state during the next clock interval at 00M. U04 remains in the reset state until the next 00M interval:

rU03 = 02F U01 U02 00M CLK

sU04 = 02F $\overline{U01}$ 00M

While the character codes are read from the output of the selection unit, the modulo-3 counter is incremented by:

CNT = 02F $\overline{U01}$ CLK

and the character counter is incremented once for each three counts of the modulo-3 counter. When the character counter indicates that the last character has been read, U02 is reset, then U03 is set:

rU02 = 02F NXL LSC CLK

NXL = K01 K02 K03 K04 K05 K06

LSC = K07 M01

sU03 = 02F $\overline{U01}$ $\overline{U02}$ X07 $\overline{X08}$ CLK

and the parity bits are read as described in paragraph 3-11.

As the parity bits are read, the A-register is incremented if it has not reached a count of XXX 111 111 111 111 so that AFL is false:

AIN = RF1 $\overline{AFL}$ CLK

RF1 = 02F $\overline{U01}$ $\overline{U02}$ K06 02M

The transfer to standby is then made:

rF01 = RF1 CLK

rU03 = RF1 $\overline{AFL}$ CLK

rU04 = RF1

rU05 = RF1

3-20 Data Transfer During Write Operation

When the controller is in the write phase, 12-bit character codes are accepted from signals R01 through R12 into the V-register. These character codes are stored in sequence in the Z-register and the S-register and then transmitted to the selection unit, as described in paragraph 3-7 (figure 3-4). This process is controlled by flip-flops X06 through X09. Before the preamble is written, two character codes are stored in the Z-register and the V-register. When the character-write operation begins, data is immediately available for transfer to the selection unit. Once the character-write operation begins, character codes continually flow from the input/output channel through the data register to the selection unit.

As the controller enters the write phase, X06 is reset and X08 is set:

rX06 = ERW CLK

sX08 = ERW DMW W90 CLK

after which X07 is reset and X09 direct set:

rX07 = X07 $\overline{CLK}$

yX09 = U01 $\overline{U02}$

so that the states of (X06, X07, X08, X09) after entering the write phase are (0, 0, 1, 1) (figure 3-5). A true ECW signal is generated:

ECW = 01F $\overline{W50}$ $\overline{W60}$ X03 X08

causing the input/output channel to generate a true W60 signal which makes ECW false, sets X06, and clears the V-register:

sX06 = 01F $\overline{W50}$ W60 $\overline{CLK}$

DRV = F02 X06 $\overline{W50}$ W60 $\overline{CLK}$
(clear V-register)

One clock time after X06 is set, X06 is reset, X08 is reset, and the V-register is loaded from signals R01 through R12:

rX06 = 01F X06 $\overline{CLK}$

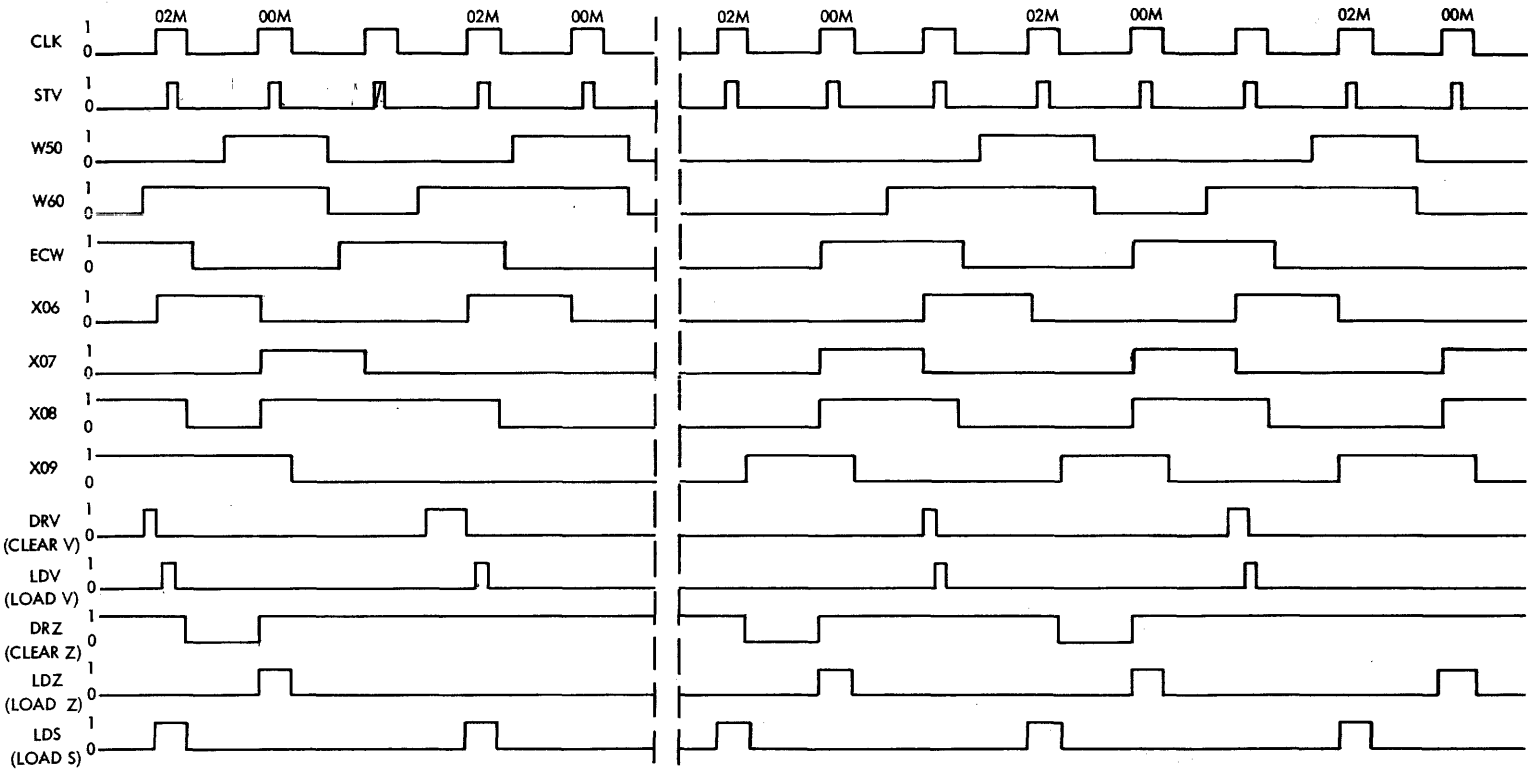
LDV = 01F X03 $\overline{X06}$ W60 STV CLK
(load V-register)

rX08 = 01F X06 CLK

While X08 is reset, the Z-register is cleared, and X07 is set:

DRZ = 01F $\overline{X08}$ X09 $\overline{CLK}$ (clear Z)

sX07 = 01F $\overline{X08}$ X09 $\overline{CLK}$



NOTE: NO TIME SCALE; ONLY SEQUENCE OF EVENTS.

Figure 3-5. Controller Write Phase Timing Diagram

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At the following clock time, the contents of the V-register are transferred to the Z-register, X07 is reset, X08 is set, and X09 is reset:

LDZ = 01F X07 CLK (load Z)
rX07 = X07 $\overline{\text{CLK}}$
sX08 = 01F $\overline{\text{U04}}$ X09 $\overline{\text{CLK}}$
rX09 = 01F U01 X07 CLK

When X08 is set, a false ECW signal is generated again and the resultant true W60 signal enables a new 12-bit code to be stored in the V-register. After X06 is set, X06, X07, and X08 are reset:

DRV = X06 $\overline{\text{W50}}$ W60 $\overline{\text{CLK}}$ (clear V-register)
sX06 = 01F $\overline{\text{W50}}$ W60 $\overline{\text{CLK}}$
LDV = 01F X03 X06 W60 STV CLK (load V-register)
rX06 = 01F X06 $\overline{\text{CLK}}$
rX07 = X07 $\overline{\text{CLK}}$
rX08 = 01F X06 $\overline{\text{CLK}}$

Because X09 is in the reset state, neither X07 nor X08 can be set. One 12-bit code is now in the Z-register and a second is in the V-register. The contents of the Z-register are transferred to the S-register at each 02M clock but the Z-register is not cleared:

LDS = 01F 02M CLK

At the end of the write preamble, X09 is set:

sX09 = 01F WPC CLK

On the following clock pulse, X07 and X08 are set and the Z-register is cleared:

sX07 = 01F $\overline{\text{X08}}$ X09 $\overline{\text{CLK}}$
sX08 = 01F $\overline{\text{U04}}$ X09 $\overline{\text{CLK}}$
DRZ = 01F $\overline{\text{X08}}$ X09 $\overline{\text{CLK}}$ (clear Z-register)

so that a false ECW signal is again generated. The contents of the V-register are transferred to the Z-register and X07 is reset:

LDZ = 01F X07 CLK (load Z-register)
rX07 = X07 CLK

During the remainder of the write operation, X09 will be set as codes are transferred from the Z-register to the S-register:

LDS = 01F 02M CLK (load S-register)
sX09 = 01F $\overline{\text{U01}}$ 02M CLK

After this transfer takes place, the Z-register is cleared and X07 and X08 are set, generating a false ECW signal. Thus the operation of transferring data from the V-register to the Z-register, clearing the V-register, and storing new data in the V-register continues as in previous descriptions of data transfer.

Flip-flop X09 cannot be reset until X07 is set:

rX09 = 01F 02M X07 CLK

which prevents reset of X09 unless new data is stored in the Z-register from the V-register:

sX07 = 01F $\overline{\text{X08}}$ X09 $\overline{\text{CLK}}$
DRZ = 01F $\overline{\text{X08}}$ X09 $\overline{\text{CLK}}$ (clear Z-register)
LDZ = 01F X07 CLK (load Z-register)

If new data is not stored in the Z-register before the 02M clock pulse, an error has occurred and X04 is set:

sX04 = 01F $\overline{\text{U01}}$ X08 X09 02M $\overline{\text{CLK}}$

The data transfer process will continue until the end of the sector and transfer to standby when the controller will be disconnected as described subsequently.

If a disconnect occurs while the controller is in the write phase, flip-flop X06 is set after flip-flop X03 is reset:

sX06 = 01F $\overline{\text{W50}}$ $\overline{\text{X03}}$ CLK

Flip-flops X06 through X09 will then be reset so that all will be in the reset state before transfer to the standby phase:

rX06 = 01F X06 $\overline{\text{CLK}}$
rX07 = X07 $\overline{\text{CLK}}$
rX08 = 01F X06 CLK
rX09 = 01F $\overline{\text{02M}}$ X07 CLK

3-21 Data Transfer During Read Operation

When the controller is in the read phase, 12-bit character codes are accepted from signals RD1 through RD4 into the S-register. These codes are stored in sequence in the Z-register and the V-register, then transmitted to the input/output channel as described in paragraph 3-9 (figure 3-4). This process is controlled by flip-flops X06 through X09. The preamble must be detected before data transfer can begin. Codes are read into the S-register during 3 consecutive clock pulses, after which the 12-bit code is transferred to the Z-register. Transfer of data from the Z-register to the V-register must keep pace with this fixed rate.

After entry into the read phase, X06, X07, and X08 are reset and X09 is direct set (figure 3-6):

rX06 = ERW CLK
rX07 = X07 $\overline{\text{CLK}}$
rX08 = 02F 02M CLK
yX09 = U01 $\overline{\text{U02}}$

This condition is maintained until the preamble double zero is detected. Detection of the preamble double zero sets U02, then resets U01 and U03 to enable logic operations during the character read subphase as described in paragraph 3-18:

sU02 = 02F U01 U03 $\overline{\text{RD1}}$ $\overline{\text{S03}}$ CLK
rU01 = 02F U02 U03 CLK
rU03 = 02F U01 U02 00M CLK

Before ECW becomes false the first time, X06 is set to allow transfer of a code from the S-register to the Z-register. At the first 02M clock X06 is set. At the following 00M clock, data transfer takes place as U04 is set:

sX06 = 02F $\overline{\text{U01}}$ $\overline{\text{U04}}$ 02M $\overline{\text{CLK}}$
LRC = 02F 00M CLK (S to Z)
sU04 = 02F 00M $\overline{\text{U01}}$

At the next 02M clock, X08 is set and the code is transferred to the V-register:

sX08 = 02F X06 $\overline{\text{X09}}$ 02M CLK
LVR = 02F X07 $\overline{\text{X08}}$ CLK (Z to V)

A false ECW signal causes the input/output channel to generate a true W60 signal and sets X06:

sX06 = 02F U04 $\overline{\text{W50}}$ W60 $\overline{\text{CLK}}$

At the next clock pulse, X06 is reset and X07 is set:

rX06 = 02F $\overline{\text{U01}}$ $\overline{\text{U03}}$ $\overline{\text{M01}}$ $\overline{\text{CLK}}$
+ 02F $\overline{\text{U01}}$ $\overline{\text{U03}}$ $\overline{\text{X09}}$ $\overline{\text{CLK}}$
sX07 = 02F X06 $\overline{\text{M01}}$ $\overline{\text{CLK}}$
+ 02F X06 $\overline{\text{X09}}$ $\overline{\text{CLK}}$

After X07 is set, the contents of the Z-register are transferred to the V-register, X07 is reset, and X09 is set to indicate data transfer:

LVR = 02F X07 $\overline{\text{X08}}$ CLK (Z to V)
rX07 = X07 $\overline{\text{CLK}}$
sX09 = 02F X07 $\overline{\text{00M}}$ $\overline{\text{CLK}}$

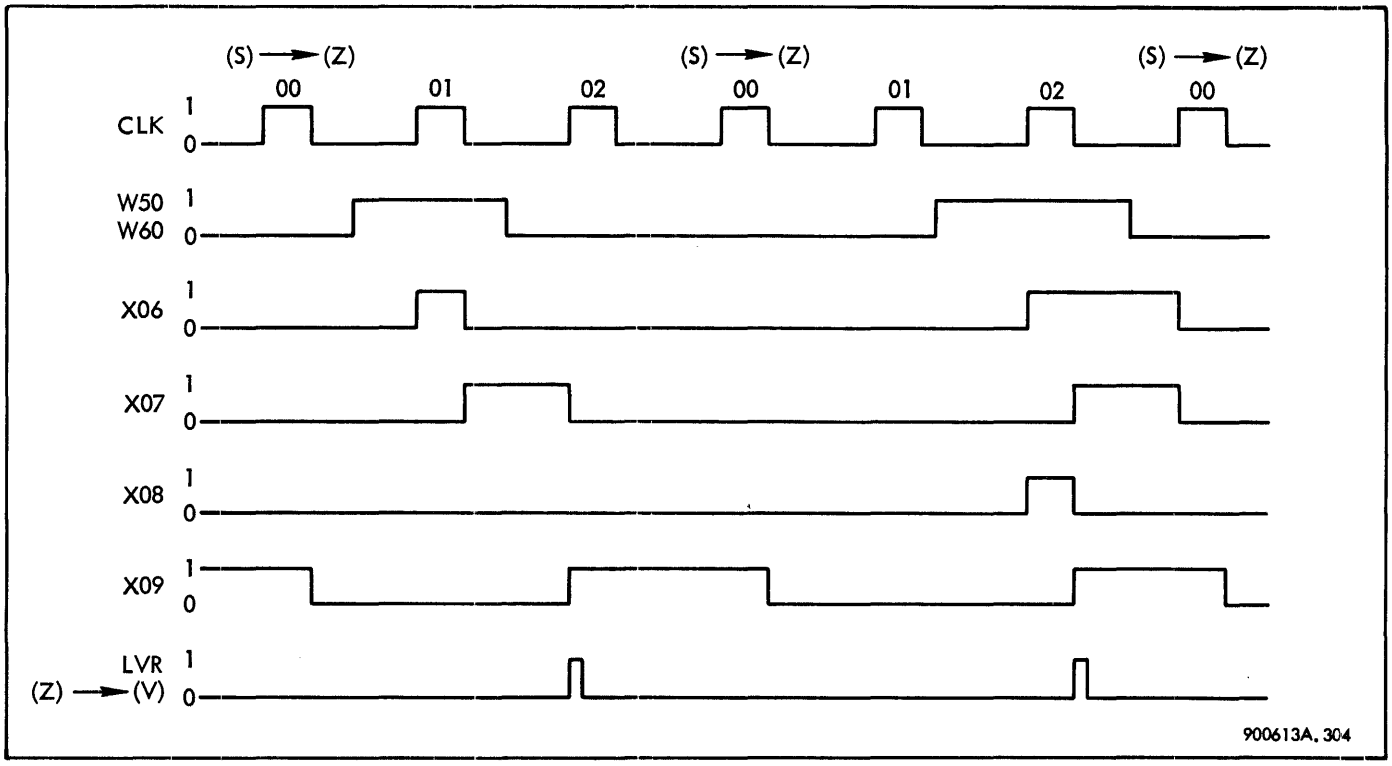


Figure 3-6. Controller Read Phase Timing Diagram

During a normal read process, data is shifted into the S-register at the clock rate and transferred to the Z-register at each 00M clock. Flip-flop X09 is reset as transfer is made:

SHS = 02F CLK (shift S)

LRC = 02F 00M CLK (S to Z)

rX09 = 02F $\overline{U01}$ 00M CLK

A false ECW signal is generated when either X09 or X06 is reset:

$\overline{ECW}$ = 02F $\overline{W50}$ $\overline{W60}$ DMW U04 $\overline{U03}$ $\overline{X09}$
+ 02F $\overline{W50}$ $\overline{W60}$ DMW U04 $\overline{X06}$

The false ECW signal generates a true W60 signal causing X06, X07, and X09 to be set in turn, and enabling data transfer from the Z-register to the V-register:

sX06 = 02F U04 $\overline{W50}$ W60 $\overline{CLK}$

sX07 = 02F X06 $\overline{M01}$ $\overline{CLK}$
+ 02F X06 $\overline{X09}$ $\overline{CLK}$

sX09 = 02F X07 $\overline{00M}$ CLK

LVR = 02F X07 $\overline{X08}$ CLK (Z to V)

If X09 is in the reset state at 00M clock time, an error has occurred and X04 is set:

sX04 = 02F $\overline{U01}$ $\overline{X09}$ 00M PST CLK

PST = U02 (read character subphase) -
+ $\overline{K06}$ (inhibit invalid error signal)

Since X09 is reset at each 00M clock to indicate data transfer from the S-register to the Z-register, X09 must be set at one of the other two clock times to indicate data transfer from the Z-register to the V-register to prevent an error signal. If a late W60 signal sets X06 at the clock before 02M, X08 is set at the 02M clock:

sX08 = 02F X06 $\overline{X09}$ 02M CLK

enabling data transfer at the leading edge of the following 00M clock as X08 is set and X09 resets:

LVR = 02F X08 00M $\overline{CLK}$

rX08 = 02F 02M $\overline{CLK}$

sX09 = 02F X08 $\overline{CLK}$

Data transfer from the S-register to the Z-register and reset of X09 takes place at the trailing edge of the same clock:

LRC = 02F 00M CLK

rX09 = 02F $\overline{U01}$ 00M CLK

If W60 signal is true at a 02M clock, a rate error takes place and the controller is disconnected when entering standby as described subsequently.

After 128 12-bit characters have been read, the controller exits from the character read subphase and checks parity against the parity bits generated during the read process as described in paragraph 3-11.

3-22 Parallel Input From Sector Counter

When the computer requests a parallel input from the sector counter of the selection unit (PIN operation), signals IOC, DMA, and C16 are true, flip-flop X02 is set, and an RT0 signal is generated when the selection unit generates ENP:

DMA = $\overline{C17}$ C19 $\overline{C20}$ C21 C22 $\overline{C23}$

IDN = C16 IOC DMA

sX02 = $\overline{X02}$ IDN

RT0 = $\overline{X01}$ X02 $\overline{ENP}$ (signals stable)

Signal IDN also enables flip-flops G01 and G02 to read bits from signals C12 and C13:

sG01 = C12 IDN

rG01 = $\overline{C12}$ IDN

sG02 = C13 IDN

rG02 = $\overline{C13}$ IDN

Flip-flops G01 and G02 control signals GS1 through GS4, each of which address one of four possible RAD memory units:

8GS1A = $\overline{0G01A}$ $\overline{0G02A}$ (RAD memory unit 1)

8GS2A = $\overline{0G01A}$ $\overline{1G02A}$ (RAD memory unit 2)

8GS3A = $\overline{1G01A}$ $\overline{0G02A}$ (RAD memory unit 3)

8GS3A = $\overline{1G01A}$ $\overline{1G02A}$ (RAD memory unit 4)

The addressed RAD memory unit controls selection unit input signals 9D01S through 9D06S. These signals in turn control outputs 9D01A through 9D06S to the computer:

$\overline{9D01A}$ = $\overline{9D01S}$ (X01 + X02)

⋮ ⋮

$\overline{9D06A}$ = $\overline{9D06S}$ (X01 + X02)

Outputs can be read only after flip-flop X02 is reset by an RTI signal generated in the computer:

rX02 = BX02A

BX02A = 2RTIA

2RTIA = $\overline{9RTIC}$

Error Detection

Error detection is performed by flip-flops E01 and X04, in addition to the parity error signal (refer to paragraph 3-11). When the controller is in the standby phase, X04 is reset:

rX04 = 00F CLK

This flip-flop is set whenever a rate error is detected during a read or a write operation:

sX04 = 01F U01 X08 X09 02M $\overline{\text{CLK}}$ (rate error, write)

+ 02F $\overline{\text{U01}}$ $\overline{\text{X09}}$ PST 00M $\overline{\text{CLK}}$ (rate error, read)

PST = U02 + $\overline{\text{K06}}$

and generates a true WES signal until return to the standby phase takes place:

WES = X04

sX04 = 00F CLK

When the controller is connected, E01 is reset:

rE01 = 00F DMA BUC

This flip-flop is set if an attempt is made to store a new address during a read or a write operation:

yE01 = X01 $\overline{\text{X02}}$ PT2

or if an attempt is made to write in a write-protected location:

sE01 = 01F WLK CLK

When the address register reaches maximum count, U03 is in the set state when return to standby takes place. If a new address is not transferred before the next sector index pulse, a true WHS signal is generated and E01 is set:

rU03 = 00F $\overline{\text{X03}}$ CLK

rX03 = $\overline{\text{DMW}}$ $\overline{\text{U01}}$ CLK

WHS = 00F DMW U03 SIP

sE01 = 00F U03 SIP CLK

A true WHS signal is also generated if the RAD file is disconnected by resetting X03.

rX03 = 00F X04 CLK

+ 01F WLK CLK

WHS = 00F DMW $\overline{\text{X03}}$ $\overline{\text{BUC}}$

3-23 SELECTION UNIT

3-24 Circuit Description

Since selection unit modules perform closely related functions, the following descriptions often refer to inputs from specific modules (indicated by name and type designation). Where modules include a set of identical circuits, the schematic diagrams a typical circuit. Text reference designations refer to typical circuit designations.

3-25 Read Input Control AK61 (See figure 7-7)

Read input control AK61 consists of four NAND gates and a transformer bias source. Each NAND gate includes a 5-input diode AND gate and an inverter. The transformer bias source includes transistors Q2 through Q5 and associated components. The function of read input control AK61 is to accept input signals from logic elements and generate bias signals for the transformers in each read/write coupler NK59.

The NAND gates receive address signals and a read enable signal. When an input signal is false, the inverter output is +8v and the transformer in read/write coupler NK59 is biased to prevent a read output. When all inputs are true, Q1 conducts, the output falls to 0v, and the transformer read output is enabled.

The transformer bias source contains a double inverter (Q2, Q3) and a two-stage power control switch (Q4, Q5). Zener diode VR3, capacitor C2, and resistor R9 supply the collector of Q4 with regulated emitter-follower current. During a read operation the power control switch output functions as a +8v, 160 ma power source. During a write operation, the power control switch is not conducting and -25v is applied to the output through resistor R10.

3-26 Y-Select AK62 (See figure 7-8)

Y-select AK62 includes four 5-input AND gates and two 2-input NAND gates, so connected that a pair of AND gates provide inputs to one NAND gate and amplified gate outputs for use in other circuits. The inputs to all AND gates are address signals; the outputs of Y-select AK62 are used for write-protect and memory control.

The diode AND gate controls Q1 (a conventional inverter) and a two-stage control switch consisting of Q2 and Q3. When any input signal is false (0v), Q3 is cut off and the output is approximately +25v. When all input signals are true (+8v), Q3 conducts to saturation (400 ma at 0v output).

Each 2-input NAND gate consists of a diode gate and an inverter. The outputs from two AND gates provide the inputs to the NAND gates. Diode CR10 is connected to a write-protect switch through external circuits. If the switch is connected to ground, the NAND gate output is 0v regardless of the input; if the switch is open, the NAND

gate output is controlled by the inputs. When both inputs are at the true level (+25v), transistor Q4 conducts and the output is false. If either input is false (0v), transistor Q4 is cut off and the output is true (+8v).

3-27 Write-Driver AK63 (See figure 7-9)

Write-driver AK63 provides the current to saturate a magnetic head when writing in memory. When a write-driver is selected by logic inputs to a gate, a data signal and its complement are received from an external flip-flop. Clock signal inputs control a flip-flop in write driver AK63. Write outputs A and B, which are coupled to the magnetic head through read/write coupler NK59, alternately drive each half-coil in the magnetic field.

When all inputs to diodes CR21 through CR27 are true (+8v or open), write-driver AK63 operates. This seven-input diode gate controls transistors Q10, Q9, Q2, and Q1 to permit operation of the write flip-flop. Transistors Q3 and Q4 are high current drivers which control the state of flip-flops Q5 and Q6. The output of a write flip-flop is received by buffer pairs Q11-Q12 and Q15-Q16 through complementary inputs A and B, respectively. The data inputs control drivers Q7 and Q8, which are coupled to drivers Q3 and Q4 through transformer T1. The clock input to Q14 and Q13 synchronizes the drivers and the flip-flop.

3-28 Index-Sector Amplifier AK64 (See figure 7-10)

Index-sector amplifier AK64 reads sector marks and index marks from the magnetic head associated with the sector track on memory. Each index mark produces an input of four negative-going pulses; each sector mark produces an input of two negative-going pulses. The circuit output is a single negative-going pulse for each input pulse.

The input circuit of index-sector amplifier AK64 is an impedance-matching network which provides proper termination and dc isolation for the magnetic head. Transistors Q1, Q2, and Q3 are differential amplifiers that produce complementary outputs to emitter-followers Q4 and Q5. Transistors Q6 and Q7 rectify the emitter-follower output waveforms by conducting only during the positive half-cycle. Transistors Q8 and Q9 clip the input waveforms to produce square-wave outputs at pin 28.

3-29 Write Clock Amplifier AK65 (See figure 7-11)

The write clock amplifier AK65 input is an 830 khz pulse train from the magnetic head that reads memory input clock track. The output is a 1660 khz pulse train generated by the positive-going portion of a square wave. The input is applied through pins 10 and 12 to an impedance-matching network which provides proper termination and dc isolation. The input pulses are amplified by differential amplifiers Q1 and Q2. Diodes CR3 and CR4 in the circuit of Q2 limit the output by squaring the amplified pulses. The delay line differentiator circuit connected between the collectors of Q3 and Q4 differentiates the limited input to produce pulses at twice the input frequency. The pulses are rectified by Q6 and amplified by Q7. The bias of Q7 is regulated by Q8 to compensate for any dc components in the pulse train.

The collector circuit of Q7 contains the tank circuit consisting of L4, L5, and C12, which is part of the input circuit of Q9. The tank circuit and Q9 form a shock-excited oscillator tuned to a value nearly twice the frequency of the clock track. Each pulse output of Q7 shocks Q9 into oscillation to produce a sinusoidal output applied to emitter-follower Q10. The output of Q10 is applied to differential amplifiers Q11 and Q12. The output of the differential amplifier is clamped at the input to Q13 by diode CR7. The circuit of Q13 and Q14 produces an asymmetrical square wave high approximately 200 nsec and low approximately 400 nsec. Transistor Q13 is alternately driven to conduct and to cut off by Q12 output. While Q13 is cut off, Q14 conducts, connecting C15 to ground and C15 is charged through R54 and R14. When Q13 conducts again, C15 is connected to ground through R45 and the charge on C15 cuts off Q14 for about 200 nsec. Capacitor C15 is then charged to the opposite polarity through R55 and R46 until Q14 conducts. After Q14 conducts for about 400 nsec the cycle repeats.

3-30 Read Preamplifier HK73 (See figure 7-12)

Read preamplifier HK73 receives an analog signal from read/write coupler NK59 and produces an output which is the differentiated form of the input (figure 3-10). The circuit includes an input network and a differential amplifier, a delay line differential amplifier, an amplifier, a limiter, and an emitter follower.

The input network contains 16 diode pairs (CR1 through CR16, and CR19 through CR34), and a diode-resistor network (CR17, CR18, CR35, CR36, R3 through R6). Each diode pair (for example, CR1, CR19) receives complementary inputs from the secondary winding of a transformer in read/write coupler NK59. A +8v bias voltage applied through the transformer center tap to the diode network of read preamplifier HK73 reverse-biases the associated input diodes. When an input is selected for amplification, the bias voltage falls to zero, the input diodes are forward-biased and the analog input signal can be read.

Differential amplifier Q1 is supplied by a constant current source (Q8) for high common-mode noise rejection. The gain of the delay line differential amplifier Q2 is almost linear with frequency up to approximately 2 mhz. Beyond that frequency, gain decreases rapidly for high-frequency noise rejection against fast switching transients. The delay line differentiator (L1, L2, L3 network) transforms signal peaks into zero-reference crossover transitions amplified and limited in the amplifier (Q3) and the limiter (Q4, Q5). Limiting diodes CR37 through CR40 between the collectors of the amplifier and limiter stages square the signal, allowing the amplifier to operate in the active region.

The output stage Q6 and Q7 is an emitter follower low impedance driving source.

3-31 Limiter HK74 (See figure 7-13)

Limiter HK74 receives the differentiated output signal of read preamplifier HK73 and produces a square wave similar to the original write signal (figure 3-10). Limiter HK74 contains three differential limiting amplifiers, a differential switch, and an emitter follower. Limiter HK74 primarily equalizes signal amplitude variations inherent in rotating magnetic memory mechanisms.

In the input circuit transformer T1 provides dc isolation, resistor R1 terminates line impedance, and capacitor C1 makes limiter HK74 less susceptible to switching transient noise. Limiting in the first three stages is by diodes CR1 through CR6, between the collectors of Q1, Q2, Q3, and Q4. Diode CR7 and capacitor C5 provide a voltage reference to the collector loads of the differential switch Q5 and Q6 to assure active region operation of emitter followers Q7 and Q8. The emitter followers are driven by complementary outputs of the diode switch. Limiter HK74 produces two pairs of complementary outputs isolated by resistor pairs R37-R39 and R38-R40.

3-32 Clock Discriminator HK75 (See figure 7-14)

Clock discriminator HK75 extracts the clock pulse from the read data by eliminating segments of the read signal not pertinent to data clocking. The inputs to clock discriminator HK75 are the complementary outputs of limiter HK74. The outputs of clock discriminator HK75 are a clock pulse and a delayed clock pulse (figure 3-10).

When the circuit is in the quiescent state, the undelayed clock output at pin 40 is +8v applied through R31. The complementary inputs are applied through pins 13 and 20 to Q1 and Q2 to feed a one-shot composed of Q3, Q4, Q8, and Q9. Capacitors C5 and C6 are charged by current source Q11-Q12 and determine the one-shot period. When the one-shot is triggered, C5 and C6 discharge, Q13 conducts and the undelayed clock output at pin 40 goes low.

Delay circuits L1, L2, and L3 with associated components, delays and applies the clock pulse to the delayed clock output through Q5, Q6, Q7, and resistor R6. The delayed clock signal is also applied through R3 and R4 to the input circuit. The feedback prevents an input from triggering the one-shot again until the end of the delay.

Transistor Q10 with current source Q11 compensates for peak shifting and the effect of pulse crowding inherent when high bit-packing is combined with modified NRZ recording. Q10 is controlled by a previous data bit pulse fed-back from data decoder HK76. When the pulse is low, Q10 conducts and inhibits Q11, thereby reducing charging current to C5 and C6. Potentiometers R26 and R28 adjust the charging current (which determines the one-shot period).

3-33 Data Decoder HK76 (See figure 7-15)

Data decoder HK76 reads limiter HK74 output (a string of ones and zeros in modified NRZ code) and produces a binary signal in the form originally received as input to the write flip-flops. The output is sampled by read flip-flops and sent to the controller. Data decoder HK76 contains two independent circuits controlled by the outputs of clock discriminator HK75. One circuit is triggered by the falling edge of the undelayed clock signal; the other circuit samples limiter HK74 output at the leading edge of the delayed clock signal. The circuit consisting of transistors Q9 through Q12 is triggered by the falling edge of the clock signal. When this circuit is in the quiescent state, the input at pin 36 is near +4v, transistors Q9 and Q11 are not conducting, and transistor Q12 conducts, generating a 0v output. As input falls from +4v, Q9 and Q11 conduct, Q12 is cut off, and output rises to +8v until capacitor C7 discharges.

Complementary limiter output signals are applied to flip-flop A1 through transistors Q1 and Q2. The flip-flop outputs control transistors Q3 and Q4 to generate the data output. Flip-flop A2 provides the feedback pulse to clock discriminator HK75. This signal compensates for the peak shift effect due to pulse crowding. Flip-flops A1 and A2 are controlled by the delayed clock from clock discriminator HK75. The delayed clock is the input to differential emitter circuit Q5 and Q6, with amplifiers Q7 and Q8. When the delayed clock input becomes high, the clock to A2 becomes high (Q5 and Q8 stop conducting), and the clock to A1 becomes low (Q6 and Q7 start conducting). This sequence decodes the data input to low and high levels with a pulse duration of 1200 nanoseconds.

3-34 Index-Sector Decoder HK77 (See figure 7-16)

The input to index-sector HK77 is the output of index-sector amplifier AK64. Upon detecting four negative-going pulses of the index mark, HK77 generates a single positive-going pulse at index output pin 10. Upon detecting two negative-going pulses of the sector mark, HK77 generates a single positive-going pulse at sector output pin 3. The input circuits of index-sector decoder HK77 include a one-shot formed by transistors Q1-Q2 and integrated circuit flip-flop A1. The one-shot is followed by buffer amplifiers Q3 and Q4. When no pulses are received, transistors Q1 and Q3 are conducting, transistors Q2 and Q4 are not conducting, and the flip-flop is in the reset state.

When the four pulses of an index mark are applied to the one-shot and the flip-flop, the first pulse causes the collector of Q1 to become low, causing the collector of Q4 to become high. The first pulse has no effect on flip-flop A1 because of the inherent delay of the one-shot and buffers. The second pulse of the group acts as a clock pulse and sets A1 because the set input is held high by transistor Q4, which remains high during capacitor C3 discharge. The third pulse sets A2 and resets A1; the fourth pulse sets A1 again. The set outputs of A1 and A2 are

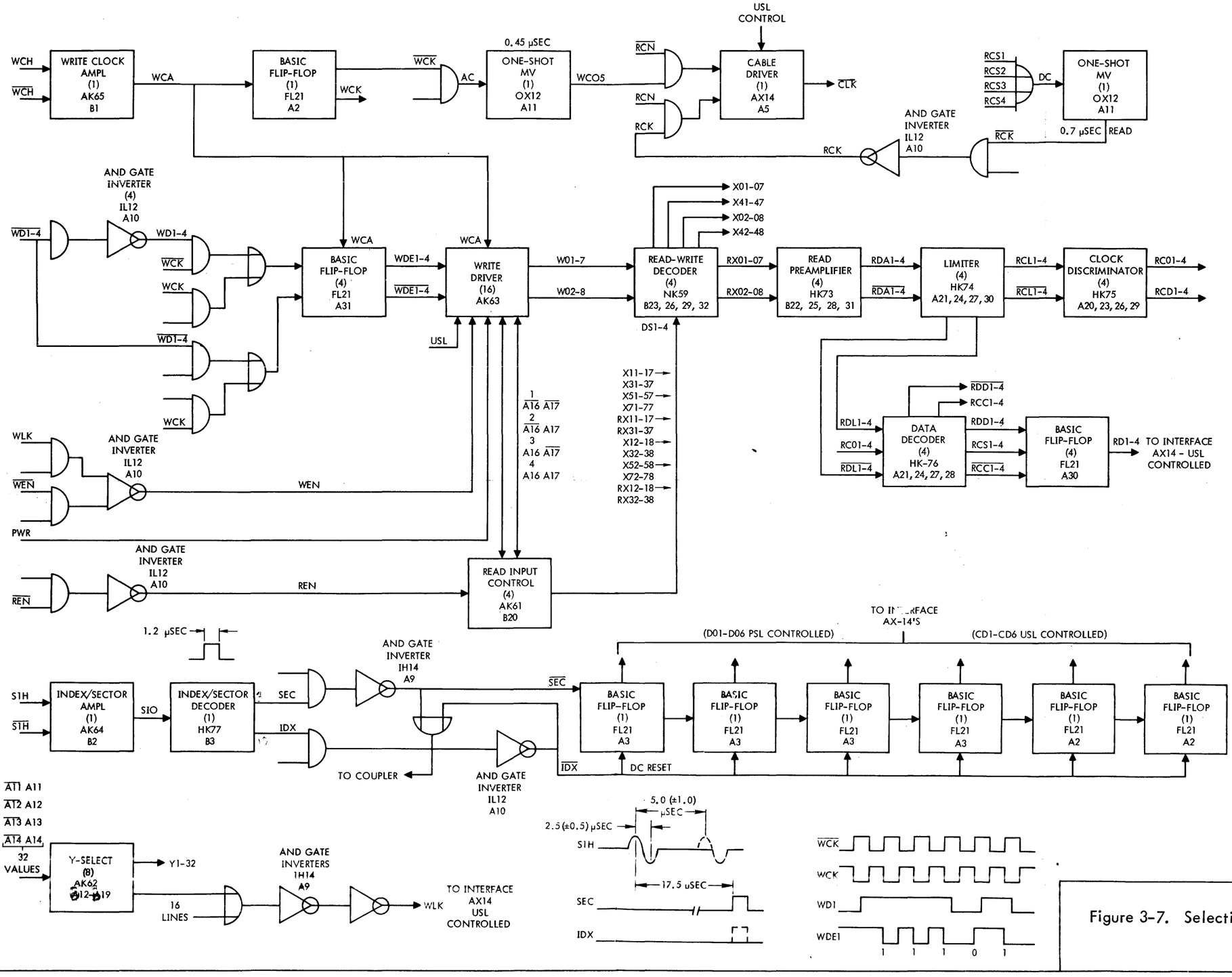


Figure 3-7. Selection Unit Block Diagram

901029A.32

inputs to the AND gate of diodes CR21 through CR23. Inputs to the AND gate of diodes CR24 through CR26 are the set output of A1 and the reset output of A2. When Q4 conducts following the second pulse, transistor Q5 which normally conducts, is interrupted for approximately two microseconds and produces a strobe pulse also applied to the AND gates. Because the gate which provides an input to Q11 and Q12 is the only gate enabled, Q11 conducts, Q12 is cut off, and a single pulse is produced at index output pin 10. Transistors Q6 through Q8 produce a reset pulse which directly reset A1 and A2 to the initial state.

A sector mark generates only two pulses. A2 therefore remains in the reset state and only the gate associated with Q9 and Q10 is enabled, causing Q9 to conduct and Q10 to be cut off. A pulse is produced at sector output pin 3. A1 is reset by the output from Q8 to restore initial conditions.

3-35 Read/Write Coupler NK59 (See figure 7-17)

Read/write coupler NK59 comprises four transformers and coupling networks of resistors and diodes. During a write operation, read/write coupler NK59 accepts the output of write-driver AK63 at input diodes CR5-CR6 and routes the data through diodes CR1-CR3 and CR2-CR4 to magnetic heads in the memory circuits. A signal from a Y-select AK62 module determines which magnetic head is active. During a read operation, data from a magnetic head is received through diodes CR1-CR3 or diodes CR2-CR4 and transmitted to read preamplifier HK73 through the secondary winding of transformer T1. The operation to be performed (read or write) is determined by bias signals generated in read input control AK62 and applied at pins 21 and 5. Address signals applied to write flip-flops, write-drivers, and magnetic heads determine which head functions during an operation.

During a write operation, the input to the primary of transformer T1 through resistor R3 is -25v. This voltage reverse-biases diodes CR7-CR8 and disconnects read output from write input. The input to the secondary of transformer T1 from pin 5 is +8v.

During a read operation, the value of the selected read/write coupler and the input to the secondary are both 0v. The read input is from the magnetic head to the read output circuit through transformer T1.

3-36 Logic Description

The modules described in paragraphs 3-23 through 3-35, and less specialized modules such as gates, flip-flops, inverters, and cable drivers, are interconnected to form the selection unit (figure 3-7). The selection unit is separable into timing circuits, address circuits, read/write control circuits, read output circuits, and memory circuits.

To store 98,304 data bits per revolution, the selection unit writes 24,576 data bits per revolution on four separate channels. A typical write channel is illustrated in figure 3-8. Digital data is received from the controller, encoded in modified NRZ format, and stored in memory. When data is read from memory, the selection unit reads simultaneously from four separate channels. A typical read channel is illustrated in figure 3-9. Analog data is received from the read/write coupler NK59 in the associated read/write control circuit. The analog data is changed to digital, transformed from modified NRZ to the same form in which originally received, and sent to the controller.

3-37 Timing Circuits (See figure 8-2)

The timing circuits include write clock amplifier AK65, index-sector amplifier AK64, index-sector decoder HK77, the read clock circuit, and the sector counter. Write clock signal WCA is true twice for each of the 27,712 write clock marks on the memory clock track. Sector signal SEC is true 63 times, and index signal IDX is true once for each revolution of the memory. If neither sector signal SEC nor index signal IDX is true, a true 3SIMS signal enables each WCA signal to change the state of flip-flop WCK. Each time index pulse IDX is true, flip-flop WCK is dc reset. Thus WCK is true at half the frequency of WCA, and is false at the start of each revolution and sector:

$$sWCK = 1WCKS\ 3SIMS\ 2WCAS$$
$$rWCK = 0WCKS\ 2WCAS$$
$$zWCK = \overline{3IDXS}$$
$$3SIMS = 3SECS\ 3IDXS$$

Signal 2RCSS is true when read output channel signal is true:

$$2RCSS = RCS1 \text{ (read channel 1)} + RCS2 \text{ (read channel 2)} + RCS3 \text{ (read channel 3)} + RCS4 \text{ (read channel 4)}$$

Signal RCS triggers one-shot RCK; signal WCK triggers one-shot WC0. When the selection unit is addressed by the controller, signal 9USLA is false and signal 9CLKS generates a clock signal transmitted to the controller. Either the read clock or the write clock is selected, depending on signal RCN originated in the controller:

$$CLK = WC0\ \overline{RCN} \text{ (write clock selected)} + RCK\ RCN \text{ (read clock selected)}$$

The sector counter consists of flip-flops D01 through D06 and is controlled by signals 2SECS and 3IDXS. When signal 3IDXS is false, the sector counter is cleared to 000 000. Flip-flop D06 represents the least significant bit; flip-flop D01 represents the most significant bit. Flip-flop D06 changes state each time signal 2SECS is true. Each of the other flip-flops change state when the set output of the controlling flip-flop changes from true to false. Each time

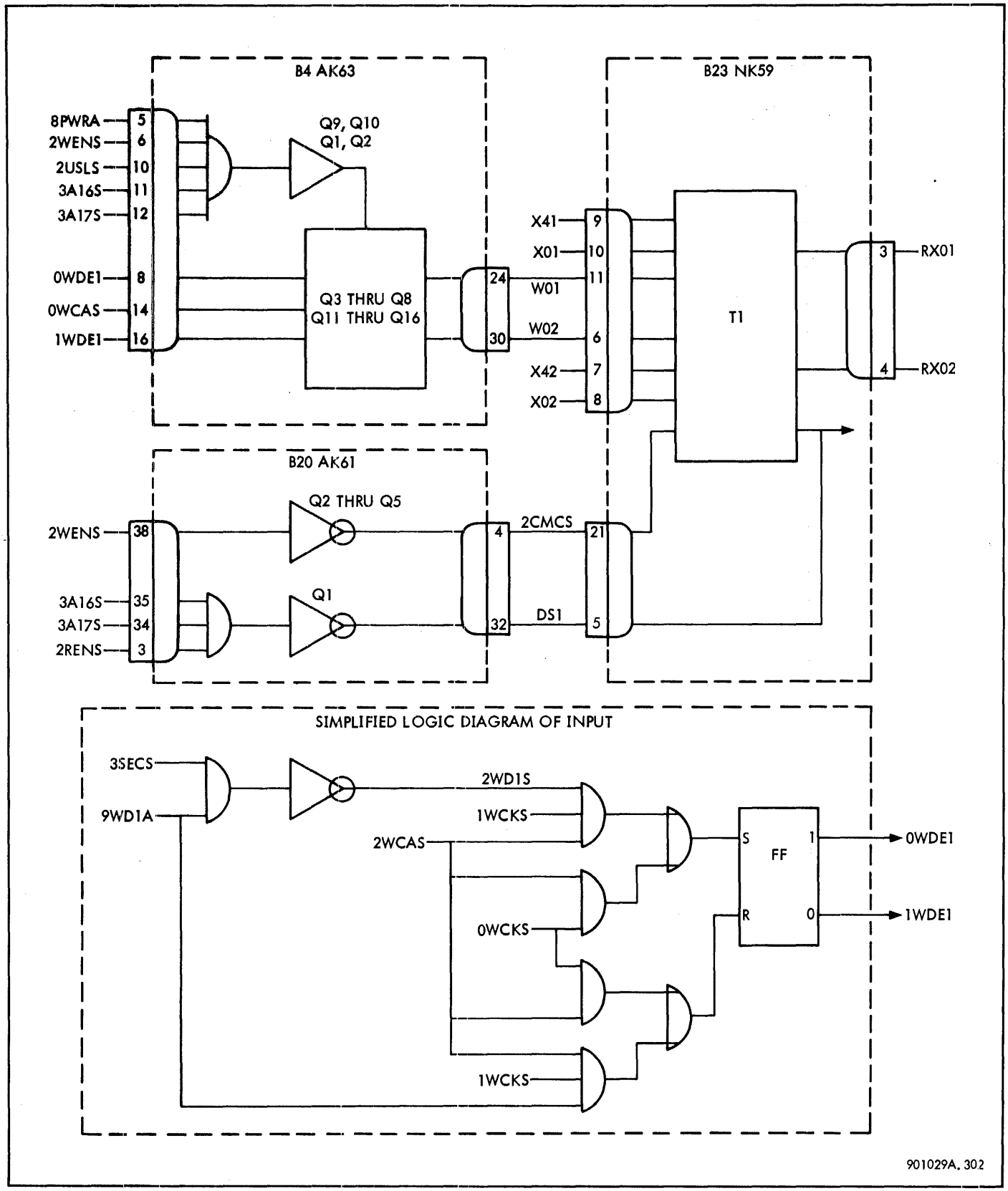


Figure 3-8. Read/Write Control Circuits Block Diagram

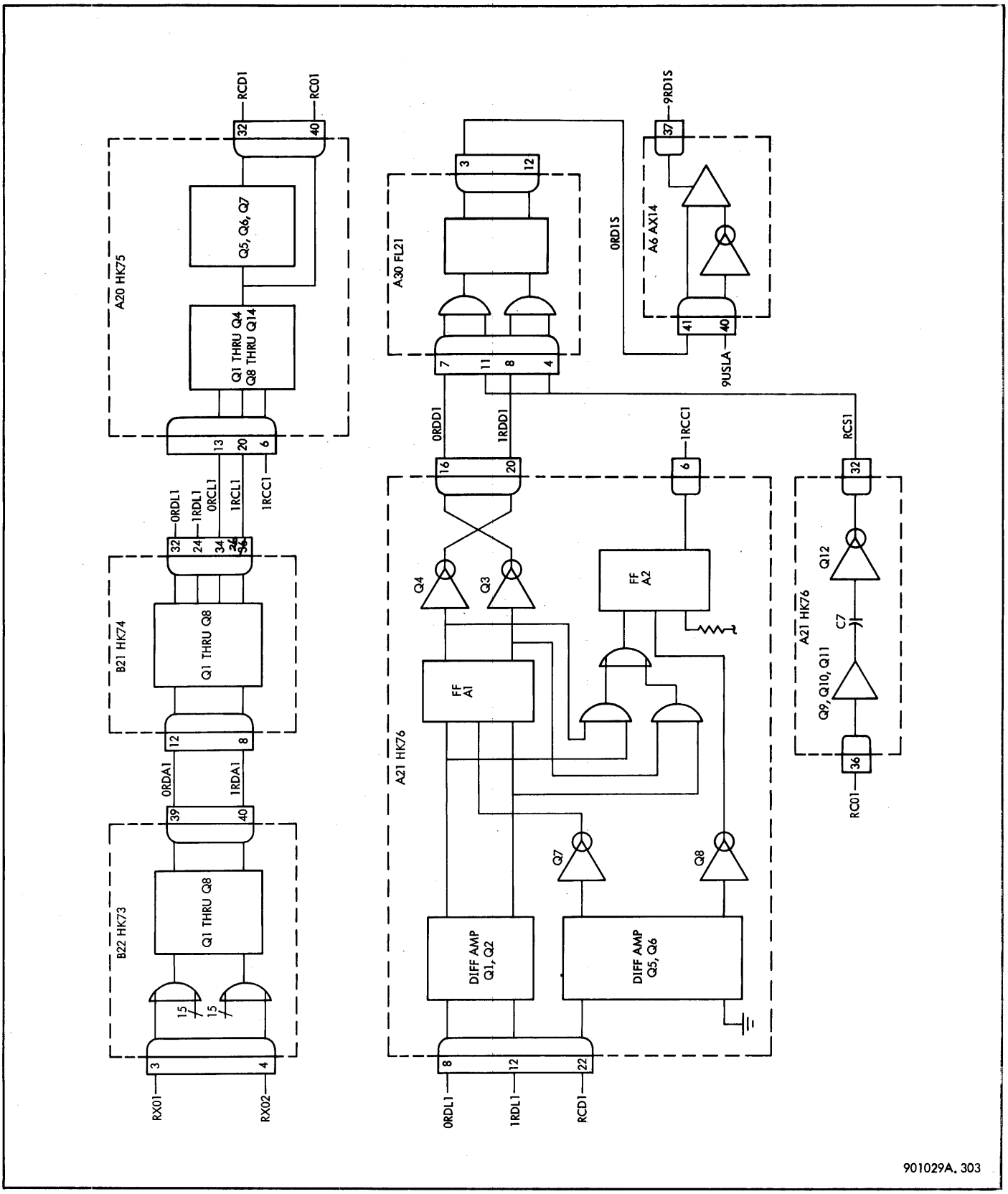


Figure 3-9. Read Output Circuits Block Diagram

signal 2SECS is true therefore, the sector counter advances one count in binary sequence from 000 001 to 111 111:

$$
\begin{aligned}
sD06 &= \overline{0D06S}\ \underline{2SECS} \\
rD06 &= \overline{1D06S}\ \underline{2SECS} \\
sD05 &= \overline{0D05S}\ \underline{0D06S} \\
rD05 &= \overline{1D06S}\ \underline{0D06S} \\
&\vdots \qquad\qquad \vdots \\
sD01 &= \overline{0D01S}\ \underline{0D02S} \\
rD01 &= \overline{1D01S}\ \underline{0D02S} \\
zD06 &= 3IDXS \\
&\vdots \qquad\qquad \vdots \\
zD01 &= 3IDXS
\end{aligned}
$$

When signal 9USLA is false, signals 9CD1S through 9CD6S are controlled by the outputs of flip-flops D01 through D06:

$$
\begin{aligned}
9CD1S &= 9USLA\ 0D01S \\
&\vdots \qquad\qquad \vdots \\
9CD6S &= 9USLA\ 0D06S
\end{aligned}
$$

Signals 9CD1S through 9CD6S are transmitted to the controller and represent the state of the sector counter. Thus if flip-flops D01 through D06 are in state 011 101, signals 9CD1S through 9CD6S are at levels 100 010, respectively. These signals are transmitted to the controller for comparison of the sector counter state with the address register in the controller. When signal 9USLA is true, signals 9CD1S through 9CD6S are all false. Signal 9USLA, (controller-generated to address one of four RAD memory units) is false if the selection unit is addressed and true if the selection unit is not addressed. Signal 9USLA defeats unaddressed selection unit CD1 through CD6 inputs to the controller.

When signal 3PSLS is false, signals 9D01S through 9D06S are controlled by the outputs of flip-flops D01 through D06:

$$
\begin{aligned}
9D01S &= 3PSLS\ 0D01S \\
&\vdots \qquad\qquad \vdots \\
9D06S &= 3PSLS\ 0D06S
\end{aligned}
$$

These circuits are identical to the circuits generating signals 9CD1S through 9CD6S. Signal PSL is generated by the controller to enable sampling of the sector counter state in the addressed RAD memory unit.

Signal 1YSCS is generated in the address circuits at a frequency corresponding to sector count signal SEC. For a false 3PSLS signal, signal 1YSCS generates signal 9ENPS. This signal times the controller for sector count signal sampling.

3-38 Address Circuits (See figure 8-3)

The address circuits generate signals to activate memory channels. Signals RCN, REN, USL, and PSL are inputs from the controller to indicate whether the selection unit is addressed and whether the operation is to be write or read:

$$
\begin{aligned}
2RENS &= \overline{9RENA} \quad \text{(read enable)} \\
2USLA &= \overline{9USLA} \quad \text{(unit select)} \\
2RCNS &= \overline{9RCNA} \quad \text{(read control)} \\
\overline{3PSLS} &= 8PSLA \quad \text{(PIN unit select)}
\end{aligned}
$$

Signals 8A11A through 8A17A include the 5-bit band address (A11 through A15) and 2-bit track address (A16 and A17). The band address bits are stored in flip-flops A11 through A15; the track address bits control signals in the read/write control circuits. Flip-flop YSC is reset each time the index signal is true. YSC is set for each sector signal by the WCK signal which coincides with a sector pulse and reset by the WCA clock signal which coincides with a sector pulse:

$$
\begin{aligned}
sYSC &= \overline{YSC}\ \overline{SIM}\ \underline{WCK} \\
rYSC &= YSC\ SEC\ \underline{WCA} \\
zYSC &= \overline{IDX}
\end{aligned}
$$

Flip-flops A11 through A15 store the band address bits received from the controller. When either a sector pulse or an index pulse is detected, the band address register is cleared:

$$
\begin{aligned}
zA11 &= SIM \\
&\vdots \qquad \vdots \\
zA15 &= SIM
\end{aligned}
$$

While YSC is in the reset state, A11 through A15 may be set if the corresponding controller signal is true. A true set input overrides a true reset input to a flip-flop:

$$
\begin{aligned}
sA11 &= 8A11A\ 1YSCS \\
rA11 &= 1YSCS \\
&\vdots \qquad \vdots \\
sA15 &= 8A15A\ 1YSCS \\
rA15 &= 1YSCS
\end{aligned}
$$

The band select circuits consist of eight Y-select AK62 modules. Band select signals Y01 through Y32 are controlled by outputs from the band address register:

$$
\begin{aligned}
\overline{Y01} &= \overline{A11}\ \overline{A12}\ \overline{A13}\ \overline{A14}\ \overline{A15} \\
\overline{Y02} &= \overline{A11}\ \overline{A12}\ \overline{A13}\ \overline{A14}\ A15 \\
&\vdots \qquad\qquad \vdots \\
\overline{Y31} &= A11\ A12\ A13\ A14\ \overline{A15} \\
\overline{Y32} &= A11\ A12\ A13\ A14\ A15
\end{aligned}
$$

The code stored in the band address register causes one band select signal to be false and all others to be true. The false band address signal grounds the center tap of a set of read/write heads in the memory circuits to enable data to be read or written.

Each pair of band address signals controls a write lockout signal. If all write-protect switches are connected to ground, lockout signal WLK is always false; if any write-protect switch is open, the write lockout signal may be controlled by one of signals SP01 through SP16:

$$\overline{SP01} = Y01\ Y02$$
$$\overline{SP02} = Y03\ Y04$$
$$\vdots \qquad \vdots$$
$$\overline{SP16} = Y31\ Y32$$

Because only one band address signal can be false, only one signal SP01 through SP16 can be true. If either input is false (indicating that one of the bands is addressed) and the write-protect switch is open, the signal will be true, generating a true WLK signal to inhibit write operations.

3-39 Read/Write Control Circuits (See figure 8-4)

The read/write control circuits include 16 write-driver AK63 modules, 16 read/write coupler NK59 modules, and four read input control AK61 modules. The read/write control circuits accept data signals from the controller and write data in memory through four identical channels (figure 3-8). Input signals to the read/write control circuits discriminate read from write operations. Controller inputs are encoded in modified non-return to zero format before being stored in memory.

Write flip-flops WDE1 through WDE4 receive data signals WD1 through WD4 from the controller and transmit signals to the read/write couplers under control of clock signals WCA and WCK. Clock signal WCA is true at twice the frequency of clock signal WCK. When signal WCK is true, each write flip-flop changes state:

$$sWDE1 = \overline{WDE1}\ WCK\ \underline{WCA}$$
$$rWDE1 = WDE1\ WCK\ \underline{WCA}$$
$$\vdots \qquad \vdots$$
$$sWDE4 = \overline{WDE4}\ WCK\ \underline{WCA}$$
$$rWDE4 = WDE4\ WCK\ \underline{WCA}$$

When signal WCK is false, each write flip-flop reads a data signal:

$$sWDE1 = \overline{WDE1}\ \overline{WCK}\ \underline{WCA}\ WD1$$
$$rWDE1 = WDE1\ \overline{WCK}\ \underline{WCA}\ \overline{WD1}$$
$$\vdots \qquad \vdots$$
$$sWDE4 = \overline{WDE4}\ \overline{WCK}\ \underline{WCA}\ WD4$$
$$rWDE4 = WDE4\ \overline{WCK}\ \underline{WCA}\ \overline{WD4}$$

The read/write couplers interface between the memory magnetic heads and other selection unit circuits. For a read operation signal REN is true and one of signals DS1 through DS4 is false, enabling one set of four read/write couplers to feed data to the read output circuits:

$$\overline{DS1} = REN\ \overline{A16}\ \overline{A17} \quad \text{(read channel 1)}$$
$$\overline{DS2} = REN\ A16\ \overline{A17} \quad \text{(read channel 2)}$$
$$\overline{DS3} = REN\ \overline{A16}\ A17 \quad \text{(read channel 3)}$$
$$\overline{DS4} = REN\ A16\ A17 \quad \text{(read channel 4)}$$
$$CMC = \overline{WEN}$$

For a write operation signal REN is false and signal CMC is false if no write lockout signal is generated:

$$\overline{2CMCS} = 2WENS$$
$$\overline{2WENS} = \overline{9WENA} \quad \text{(not write-enable)}$$
$$+\ \overline{2WLKS} \quad \text{(write lockout)}$$

All read/write couplers are activated by signal CMC. Only one group of four receives valid inputs as determined by the track bit inputs to the write-driver AK63 modules. The write flip-flops encode a sequence of data bits to generate two output bits for each input bit. For example, input and output starting from a reset state of WDE may be:

Input: 1 0 0 0 1 0 1 1 1 0

Output: 01 00 10 10 11 00 11 01 01 00

Note that output pairs are the same if previous consecutive input bits are different, and output pairs are different if previous consecutive input bits are the same. In the read/write control circuits the input bit is received from the controller (WD1 through WD4) and the output bits are generated by the associated write flip-flop (WDE1 through WDE4). The write-drivers accept data at the high frequency clock rate as controlled by signal WCA. During each clock interval (27,712 per revolution) output pairs will be either the same polarity or opposite polarity, as established by the write flip-flop outputs (figure 3-10).

The 16 write-drivers read the output of the write flip-flops and write in memory through the read/write couplers. If the power source has not failed (PWR true), the selection unit has been addressed by the controller (USL true), and a write operation is to be performed (WEN true), a group of four write-drivers is then selected for operation by track signals A16 and A17. The active outputs for each track address are listed in table 3-2.

Table 3-2. Write Outputs

Input Data Source	Track Address			
	$\overline{A16}$, $\overline{A17}$	A16, $\overline{A17}$	$\overline{A16}$, A17	A16, A17
WDE1	W01, W02	W11, W12	W21, W22	W31, W32
WDE2	W03, W04	W13, W14	W23, W24	W33, W34
WDE3	W05, W06	W15, W16	W25, W26	W35, W36
WDE4	W07, W08	W17, W18	W27, W28	W37, W38

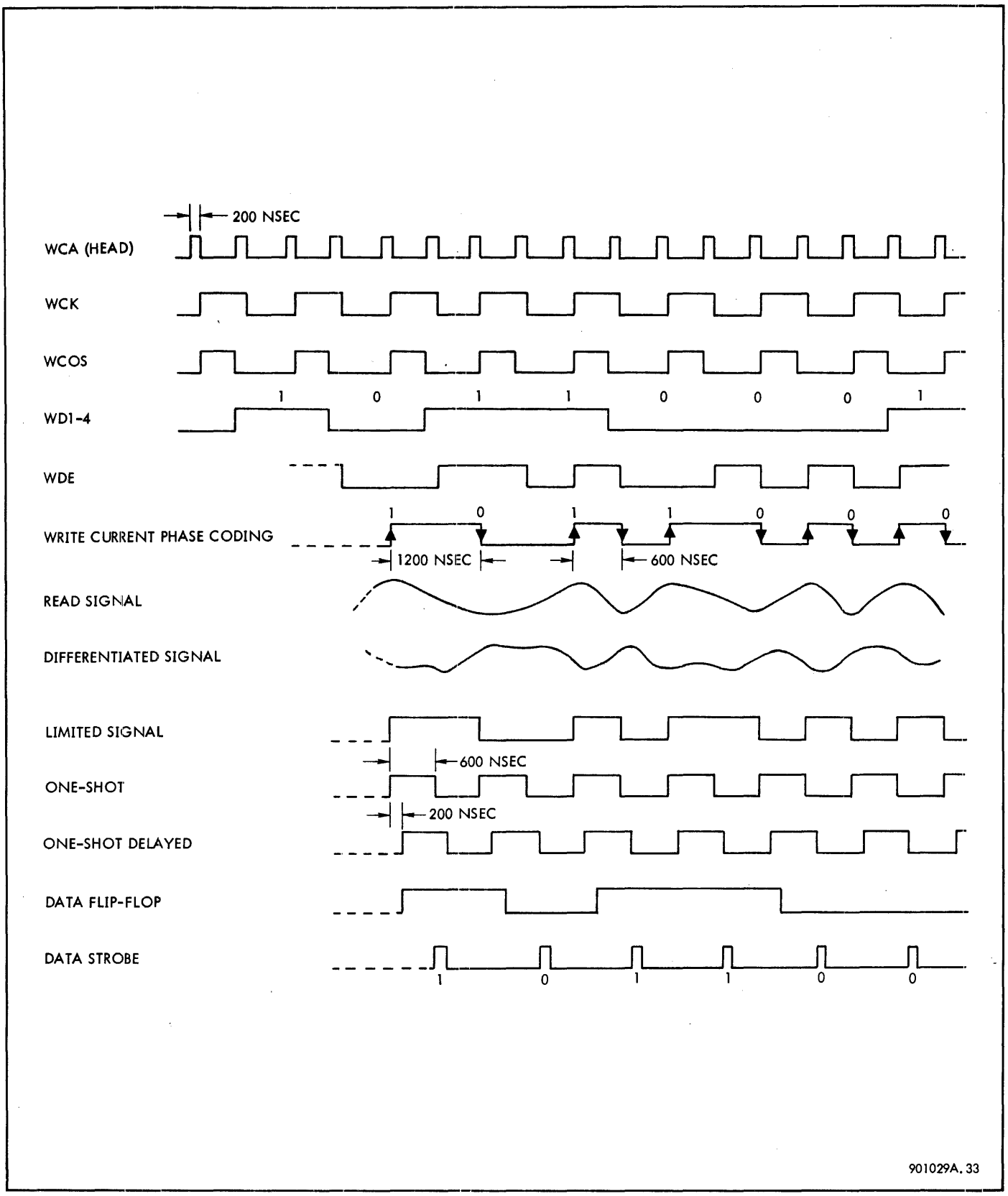


Figure 3-10. Read/Write Timing Diagram

3-40 Read Output Circuits (See figure 8-5)

The read output circuits include four read preamplifier HK73 modules, four limiter HK74 modules, four clock discriminator HK75 modules, and four data decoder HK76 modules. The read output circuits accept the signals read from memory through the read/write couplers of the read/write control circuits. The analog output is changed to a digital form and decoded from modified NRZ to the original data form. Four identical channels are provided (figure 3-9). For a given track address, outputs RDD1 through RDD4 accept data from one set of four read/write couplers, as summarized in table 3-3.

Table 3-3. Read Outputs

Output Data	Track Address			
	$\overline{A16}$, $\overline{A17}$	A16, $\overline{A17}$	$\overline{A16}$, A17	A16, A17
RDD1	RX01, RX02	RX11, RX12	RX21, RX22	RX31, RX32
RDD2	RX03, RX04	RX13, RX14	RX23, RX24	RX33, RX34
RDD3	RX05, RX06	RX15, RX16	RX25, RX26	RX35, RX36
RDD4	RX07, RX08	RX17, RX18	RX27, RX28	RX37, RX38

The read output circuits accept the analog read signal from the read/write couplers (figure 3-10). This signal is differentiated by read preamplifier HK73. Limiter HK74 amplifies and squares the differentiated signal. The output of the limiter provides pairs of complementary inputs to both clock discriminator HK75 and data decoder HK76. The clock discriminator generates a clock pulse and a delayed clock pulse.

The limiter output contains information to regenerate the original code. The limiter output is sampled by A1 of the data decoder at the rising edge of the delayed clock. The falling edge of clock pulse RC01 generates data strobe RCS1. The output of flip-flop A1 is sampled by the data strobe and stored in read flip-flop RD1. Feedback from flip-flop A2 of the data decoder to clock discriminator HK75 is used for adjusting the clock pulse on-time.

During a write operation, preamble 0101010100 is stored in memory before writing data. During a read operation, a timing signal generated in the controller prevents output read until the alternating ones and zeros of the preamble are available. The first double zero detected is always in the preamble. The preamble guards decoding of the modified NRZ data to prevent incorrect data.

3-41 Memory Circuits (See figure 8-6)

Memory circuits consist of 128, 256, or 512 magnetic heads in a matrix. For a read or a write operation, a set of four read/write heads is selected to provide output or receive input. Selection is by the band address signal Y01 through Y32, and by track address signals A16 and A17. The track address signals control circuit elements of gates in the read/write control circuits. The band address signals are connected directly to the memory matrix. A summary of effective signals is provided in table 3-4.

Each false band address signal enables 16 read/write heads. The read/write heads are connected in four sets of four heads each. Complementary outputs are directed to the read/write couplers. The track bits select one head from each set of four by inhibiting inputs or outputs on three of the four pairs. During a read or a write operation, only four heads of the maximum of 512 are active. For example, if the address code A11 through A17 is 10110 01, band address signal Y23 selects the 16 heads indicated in table 3-4, and track address bits $\overline{A16}$ A17 select signals X21 through X28. If the operation is write, signals are received at these inputs; if the operation is read, signals are transmitted from these outputs.

For RAD File Model 9367B, the maximum number of read/write heads is 256, bit A11 is always a zero, and band address signals Y17 through Y32 are always true. For RAD File Model 9367C, the maximum 512 read/write heads may be used.

Table 3-4. Memory Input/Output Signals

Band Address Signal	Track Address			
	$\overline{A16}$, $\overline{A17}$	A16, $\overline{A17}$	$\overline{A16}$, A17	A16, A17
Y01 through Y08	X01, X02	X11, X12	X21, X22	X31, X32
	X03, X04	X13, X14	X23, X24	X33, X34
	X05, X06	X15, X16	X25, X26	X35, X36
	X07, X08	X17, X18	X27, X28	X37, X38
Y09 through Y16	X41, X42	X51, X52	X61, X62	X71, X72
	X43, X44	X53, X54	X63, X64	X73, X74
	X45, X46	X55, X56	X65, X66	X75, X76
	X47, X48	X57, X58	X67, X68	X77, X78

(Continued)

Table 3-4. Memory Input/Output Signals (Cont.)

Band Address Signal	Track Address			
	$\overline{A16}$, $\overline{A17}$	A16, $\overline{A17}$	$\overline{A16}$, A17	A16, A17
Y17 through Y24	X01, X02	X11, X12	X21, X22	X31, X32
	X03, X04	X13, X14	X23, X24	X33, X34
	X05, X06	X15, X16	X25, X26	X35, X36
	X07, X08	X17, X18	X27, X28	X37, X38
Y25 through Y32	X41, X42	X51, X52	X61, X62	X71, X72
	X43, X44	X53, X54	X63, X64	X73, X74
	X45, X46	X55, X56	X65, X66	X75, X76
	X47, X48	X57, X58	X67, X68	X77, X78

3-42 POWER DISTRIBUTION AND CONTROL

3-43 POWER DISTRIBUTION

The controller draws dc from the computer power supply and samples ac to detect power failure (figure 7-27). The memory motor power is from the ac plug mold. The selection unit receives dc from Power Supply Model PX13 in the RAD memory unit in which located, or from the basic RAD memory unit. Ac enters the RAD memory unit through connector J1 and passes through circuit breaker CB1 on the power distribution panel.

3-44 POWER FAIL-SAFE CONTROL

Two SK60 primary power detector modules in the controller deactivate the controller in case of power failure, or if the computer START pushbutton is pressed (figure 8-14). One SK60 detects an ac failure in the input/output buffer that supplies power to the controller; the other SK60 detects ac failures in the selection unit. Stepdown transformers on the power protection panel supply the ac signal.

Under normal operating conditions, outputs 3RLA and 3RL2A are at the ground (false) level, the relays are energized, and signal 8PWRA is at the high (true) level. If primary power fails, the filtered dc supplies in the input/output buffer or in the selection unit will maintain sufficient dc for normal operation for several milliseconds. If ac fails or drops below a threshold adjustment on either SK60, the output goes to +25 volts, the relay is deenergized, and signal 8PWRA is held at the false level at the output of the buffer amplifier. As the signal falls to zero volts, the output drivers of the write amplifiers are inhibited from further writing, the phase circuits of the controller are placed in standby, the buffer disconnects, and flip-flops A09 through A23, U01 through U06, and X01 through X04 are reset through direct inputs:

3DRAA = 3ACTA 8PWRA

$\overline{3ACTA}$ = 200FA 0U06A 1X03A (buffer connect signal)

zA09 = 3DRAA

.
.
.

zA23 = 3DRAA

zF01 = 3DRAA

zF02 = 3DRAA

zU01 = 3DRAA

zU02 = 3DRAA

zU03 = 3DRAA

zU04 = 8PWRA

zU05 = 8PWRA

zU06 = 8PWRA

zX01 = 8PWRA

zX02 = 8PWRA

zX03 = 8PWRA

zX04 = 8PWRA

Signal 8PWRA is also controlled by signal ST0 originating at the START pushbutton on the computer control panel. When the START pushbutton is pressed, signal 8PWRA is grounded, and the same sequence occurs as described for power failure. In addition, flip-flop E01 is set by a signal applied to the output.

SECTION IV
INSTALLATION AND MAINTENANCE

4-1 INSTALLATION

4-2 INSTALLATION PLANNING

A RAD file installation consists of a controller, power protection panel, a maximum of four RAD memory units, and cable assemblies. Verify that all items required for the installation are available, and exercise normal care during unpacking. For some RAD memory units, the memory is shipped separately; for others the memory is shipped in the RAD memory unit with special bracing to be removed during installation.

Space requirements for a RAD memory unit are illustrated in figures 7-24 and 7-25. The primary considerations are provision for heat dissipation and accessibility. Space is required in front of the RAD memory unit for access to a memory when extended from the cabinet and for access to power supplies and the power distribution panel. Space is required at the rear of the RAD memory unit for access to selection unit controls. Minimum recommended space allowances are: 5 feet in front of the unit; 3 feet at the rear of the unit, and 2-1/2 feet on each end of RAD memory units. Since RAD memory units of a multiple-unit installation are bolted together, side panels are included for only the basic unit.

The controller and power protection panel should be installed in the same cabinet as near the computer as possible. Distances between the controller, power protection panel, and RAD memory units are restricted by interconnecting cable assembly lengths. Cable lengths for RAD file interconnecting cables are:

Connection	Length
Controller to computer (signal)	10 ft
Controller to computer (dc)	5 ft
Power protection panel to controller	10 ft
Power protection panel to computer (ac sample)	10 ft
Power protection panel to RAD memory unit (ac)	30 ft
RAD memory unit to RAD memory unit	3 ft
Controller to RAD memory unit	30 ft
RAD memory unit to ac source	8 ft

Because a part of the 30-foot cable between the controller and RAD memory unit must be used within the equipment, the maximum practical distance from controller to RAD memory unit is 20 feet.

4-3 INSTALLATION PROCEDURES

4-4 Installation of RAD File Model 9367B

Install RAD File Model 9367B as follows:

a. Install controller in computer input/output cabinet or if necessary, in a separate cabinet (figure 7-23).

b. Install power protection panel in controller cabinet.

c. Connect computer/controller power wiring as follows:

From (Controller)	To (Computer Source)
B26-44	0 vdc return
B26-45	+ 8v
B26-46	-25v
B26-47	+25v

d. Connect six leads from power protection panel to controller as follows (figures 4-5 and 4-6):

Power Protection Panel	Controller	Function
TB2-5	TB2-1	AC
TB2-4	TB2-2	Bias
TB2-3	TB2-3	AC
TB1-5	TB3-1	AC
TB1-4	TB3-2	Bias
TB1-3	TB3-3	AC

e. Connect 30-foot cable from power protection panel to computer ac source.

Note

Perform steps f through m for each RAD memory unit (figure 7-25).

f. Install and level RAD memory unit within cable reach of controller, or adjacent RAD memory unit as applicable.

g. Remove drum memory shipping hardware as follows:

1. Loosen and remove three red shipping locknuts and screws on top of drum memory and save for future use.

2. Insert three button-head capscrews (attached to top of drum memory) in holes previously occupied by shipping screws.

h. Check that cable assembly 133304 in memory unit is connected from ac plug mold to Power Supply Model PX13.

i. Check that drum matrix cable assembly 131623 is connected from selection unit to drum memory.

j. Check that drum clock cable assembly 132238 is connected from selection unit to drum memory.

k. Check that circuit breaker-to-drum motor cable assembly 131825 is connected from power distribution panel to drum memory.

l. Check that topside fan power cables are connected to ac plug mold.

m. Check that all RAD memory controls and indicators are off.

Note

Refer to section V for performance test (if desired at this point) before connecting power or signal cables, or installing modules.

n. Connect signal cables between controller and RAD memory unit, and between controller and computer (figure 4-1).

o. Connect 30-foot chassis ground wire from controller to RAD memory selection unit.

p. Connect 30-foot ac cable from power protection panel to RAD memory ac plug mold.

q. For multiple-unit installations, connect plug P169 of plug module cable assembly P168/P169 to receptacle A32 of selection unit in RAD memory unit; connect plug P168 to receptacle A5 of selection unit in adjacent RAD memory unit.

r. For multiple-unit installations, connect leads between RAD memory units as illustrated in figure 4-2 and as listed below:

From	To	Function
TB2-1	TB1-9	0 vdc return
TB2-2	TB1-8	+8v
TB2-3	TB1-7	-25v
TB2-4	TB1-6	+25v
TB2-6	TB1-4	+50v

s. Insert modules in controller (figure 4-3).

t. Insert modules in selection unit of each RAD memory unit (figure 4-4).

u. For each RAD memory unit, connect power cable assembly to site ac (figure 4-7).

v. Perform turn-on procedure (refer to paragraph 2-8).

4-5 Installation of RAD File Model 9367C

Install RAD File Model 9367C as follows:

a. Perform steps a through e in paragraph 4-4.

Note

Perform steps b through m for each RAD memory unit (figure 7-24).

b. Install and level RAD memory unit within cable reach of controller, or adjacent RAD memory unit as applicable.

Note

9367C disc memory is shipped separately from memory cabinet.

c. Extend slide assembly mount for disc memory. Rotate support legs down to support disc memory during assembly.

d. Mount disc memory on base plate with 12 8-32NC x 3/4 pan-head screws, 12 flat washers, and 12 internal tooth lockwashers.

e. Slide disc memory into RAD memory unit cabinet.

f. Connect power cable assembly from disc memory to ac plug mold.

g. Connect ground wire from selection unit to top of disc memory.

h. Connect cable assembly from ac plug mold to Power Supply Model PX13.

i. Connect disc matrix cable assembly 131620 from selection unit to disc memory.

j. Connect disc clock cable assembly 132240 from selection unit to disc memory.

k. Check that topside fan power cables are connected to ac plug mold.

l. Check that power cable from ac plug mold is connected to circuit breaker on power distribution panel.

m. Check that all RAD memory controls and indicators are off.

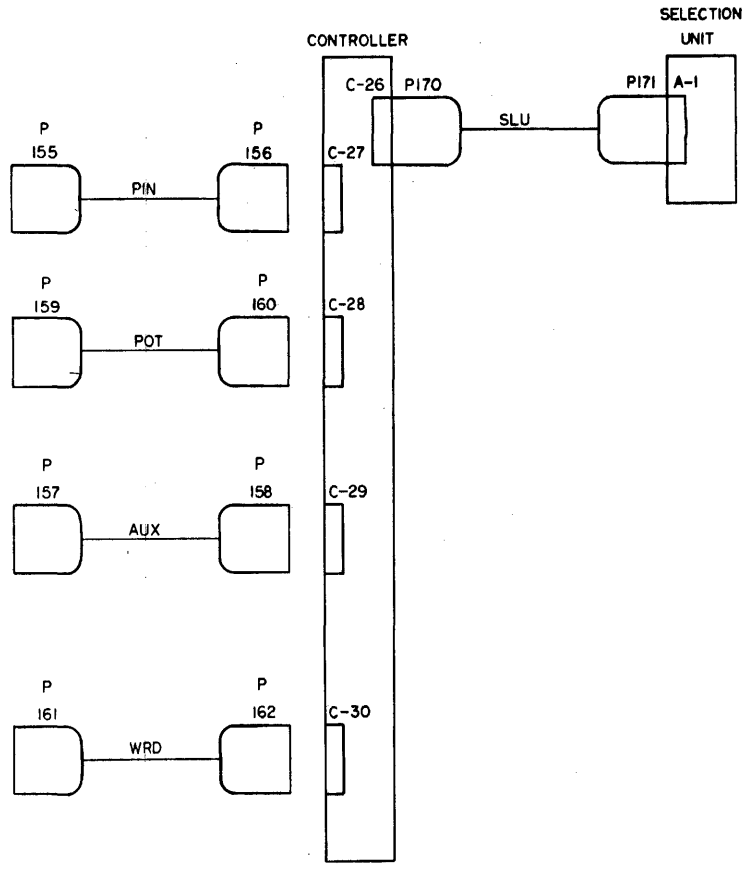
Note

Refer to section V for performance test (if desired at this point) before connecting power or signal cables, or installing modules.

n. Perform steps o through v in paragraph 4-4 to complete installation procedure.

RAD CABLING

	92	925	930	9300
DACC		3F 4F	3F 4F	3F 4F
W&Y BUFFER	31L 32L	31F 32F	31F 32F	31F 32F
DACC		26F 27F	26F 27F	26F 27F
W&Y BUFFER	28L 29L 30L	22F 23F 24F	22F 23F 24F	22F 23F 24F
DACC		23F 24F 25F	23F 24F 25F	23F 24F 25F
Y BUFFER		14F 15F 16F	14F 15F 16F	14F 15F 16F
W BUFFER	26D	19F 20F 21F	19F 20F 21F	19F 20F 21F
DACC		19F 20F	19F 20F	19F 20F
Y BUFFER		8F 9F	8F 9F	8F 9F
W BUFFER	25D	10F 11F	10F 11F	10F 11F



NOTE: REFERENCE SDS DWG: 131820-4B

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Figure 4-1. RAD File Controller-to-Computer Cabling

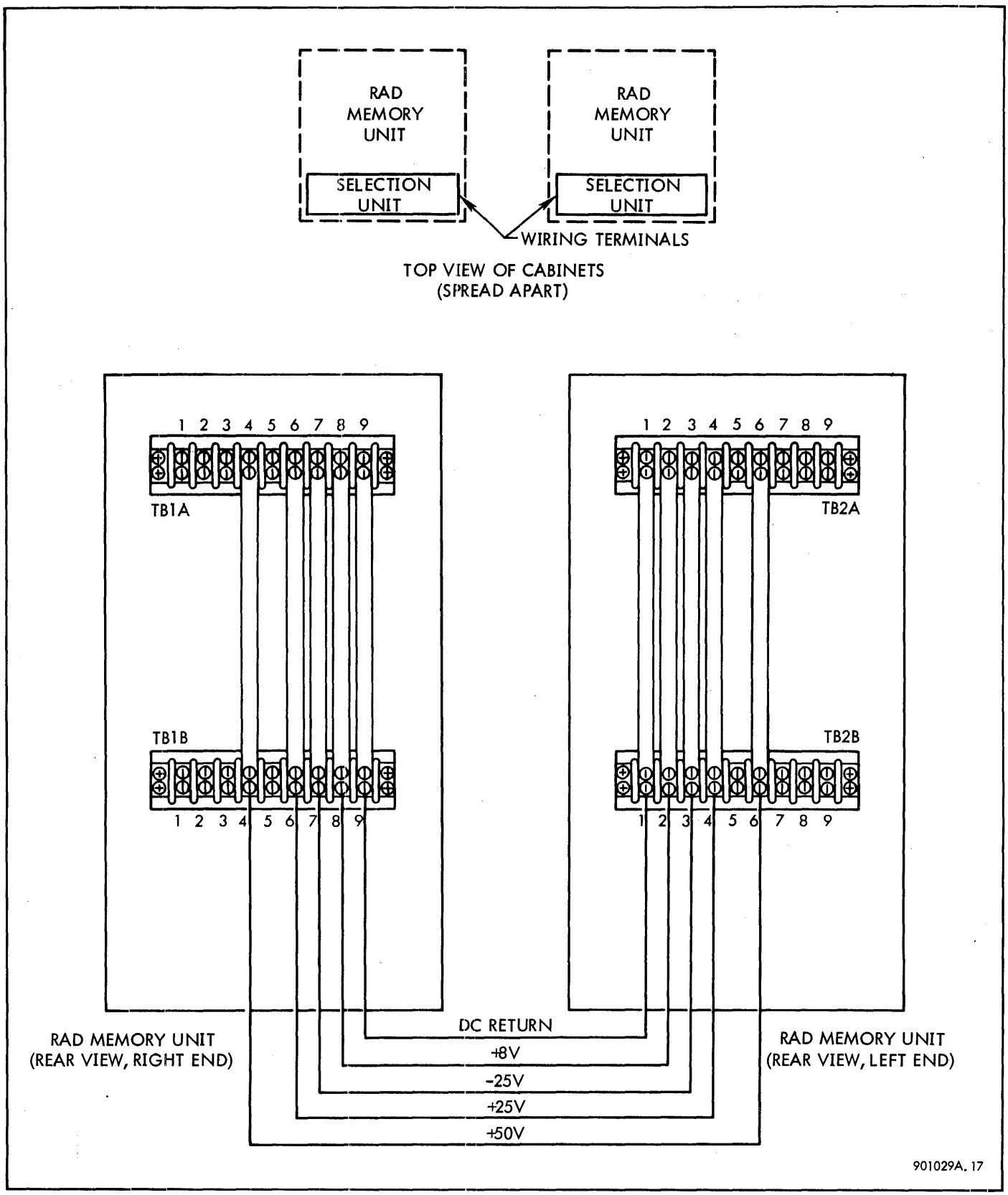

Figure 4-2. Selection Unit Dc Wiring

CHASSIS A

LOCATION	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26
MODULE	FH 20	FH 20	FH 20	GK 51	FH 20	FH 20	FH 20	FH 20	BH 10	GK 51	GK 51	FH 20	FH 20	FH 20	FH 20	FH 20	AX 14	AX 14	AX 16	AX 16

CHASSIS B

LOCATION	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26
MODULE	BH 10	IH 14	GK 51	GK 51	GK 51	GK 51	GK 51	AH 10	AH 10	AH 10	BH 10	IH 14	IH 14	GK 51	GK 51	GK 51	BH 10	AX 14	AX 14	AX 14

CHASSIS C

LOCATION	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26
MODULE	FH 19	FH 19	OX 12	BH 10	BH 10	AH 10	IH 14	IH 14	FL 21	AH 10	FH 19	FH 19	FH 19	IH 14	IH 14	P 162	P 158	P 160	P 156	P 170

CHASSIS D

LOCATION	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26
MODULE	GK 51	GK 51	GK 51	FH 20	IH 10	BH 10	IH 10	BH 10	BH 10	GK 51	GK 51	GK 51	IH 14	BH 10	GK 51	GK 51	SK 60	SK 60	KX 12	*

VIEWED FROM MODULE SIDE.
*CONNECTOR WIRED FOR INDICATING-LAMP TEST MODULE.

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Figure 4-3. Controller Module Complement

CHASSIS A

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
P 171	FL 21	FL 21	AX 14	AX 14	AX 14	BH 10	GH 14	FH 19	IL 12	OX 12	SX 60	SX 69	AK 63	AK 63	AK 63	AK 63	AK 63	AK 63	HK 75	HK 76	AK 63	HK 75	HK 76	AK 63	HK 75	HK 76	HK 76	HK 75	FL 21	FL 21	P 168

NOTE 1 — NOTE 3

NOTE 2

CHASSIS B

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
AK 65	AK 64	HK 77	AK 63	AK 63	AK 63	AK 63	AK 63	AK 63	AK 63	AK 63	AK 62	AK 62	AK 62	AK 62	AK 62	AK 62	AK 62	AK 62	AK 61	HK 74	HK 73	NK 59	HK 74	HK 73	NK 59	HK 74	HK 73	NK 59	HK 74	HK 73	NK 59

NOTES:
1. P171 IS INPUT FROM CONTROLLER TO RAD MEMORY UNIT AS SHOWN. FOR AN ADDITIONAL RAD MEMORY UNIT, THIS CONNECTOR WILL BE P169.
2. AK62-ONE PER 64 HEADS: TWO FOR 128, FOUR FOR 256, OR EIGHT FOR 512 HEADS (MAX), AS SHOWN.
3. P168 IS OUTPUT TO SELECTION UNIT OF ADDITIONAL RAD MEMORY UNIT, IF USED.

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Figure 4-4. Selection Unit Module Complement

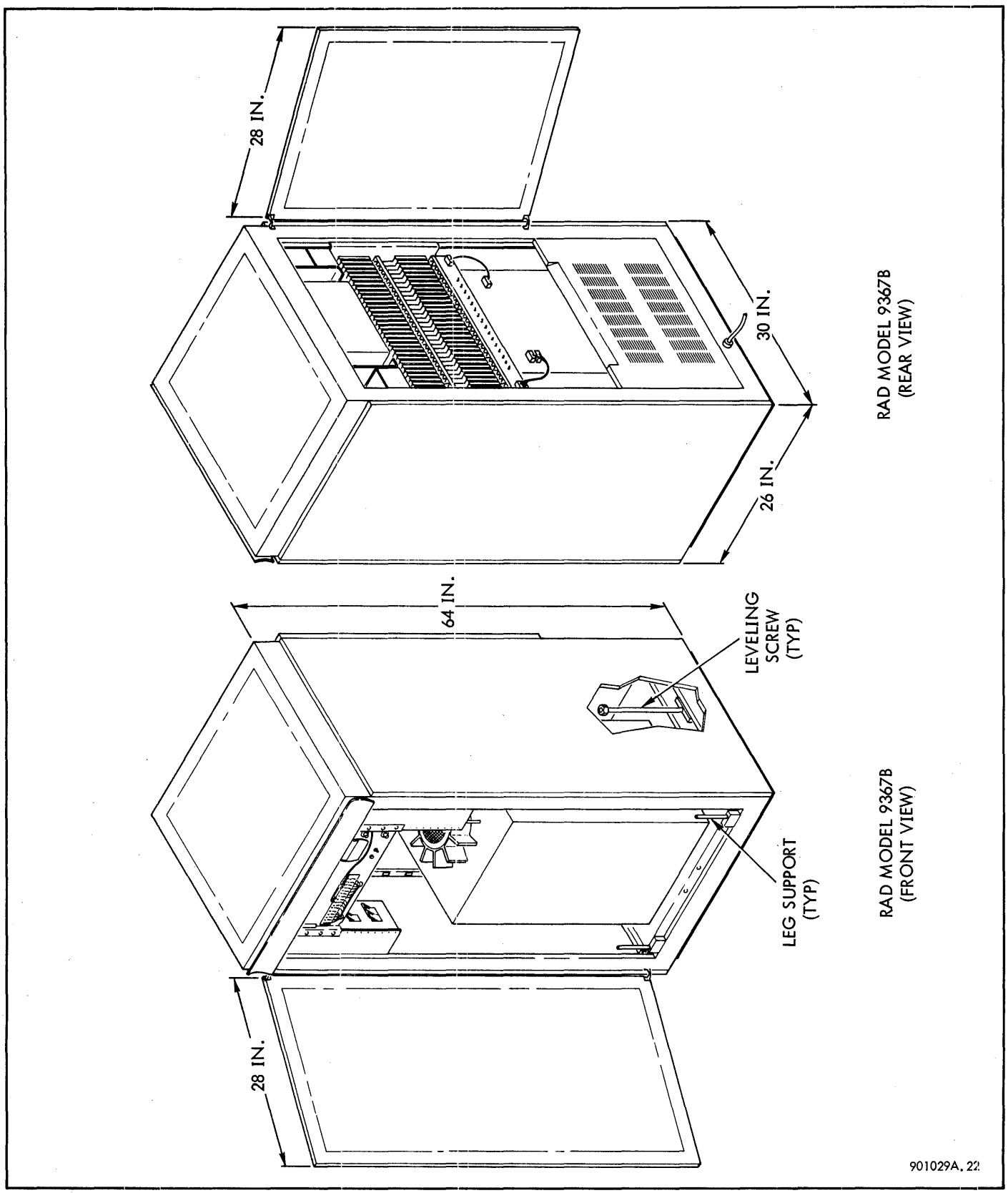


Figure 4-5. RAD File Installation Diagram (Sheet 1 of 2)

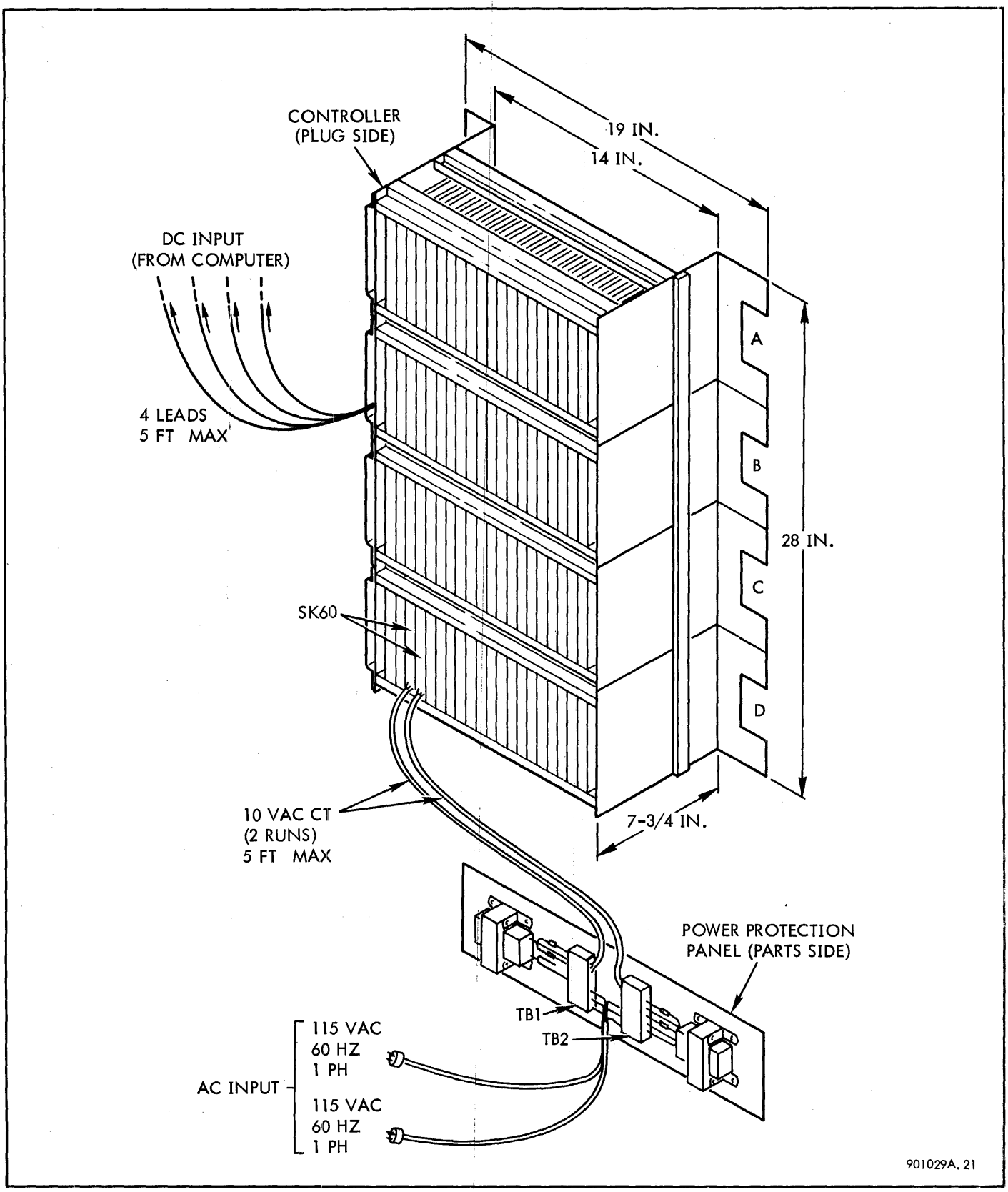


Figure 4-5. RAD File Installation Diagram (Sheet 2 of 2)

4-6. MAINTENANCE

4-7 ROUTINE MAINTENANCE

Routine maintenance or adjustment are not required for the RAD file installation. All variable elements of the modules are shipped calibrated and adjusted. Memory malfunctions are indicated by control panel lamps. A periodic removal of dust in and around cabinets and fans should be scheduled at which time the RAD file installation can be inspected.

4-8 MODULE REPLACEMENT AND ADJUSTMENT

Spare modules are supplied with each model of the RAD file, as listed in table 4-1. A multiple-unit RAD file installation stocks spare modules for the controller plus a set of spare modules for each RAD memory unit. Since at least one spare module of each type is supplied, field maintenance should be limited to replacement of defective modules.

The following adjustment procedures should be used only when abnormal or marginal operation exists and no replacement is available. The location of modules is indicated in figures 4-2 and 4-3. Adjustable elements are identified in section VI, and schematic diagrams are provided in section VII. All adjustment procedures require the use of Tektronix oscilloscope Model 545B or equivalent, with a dual-trace plug-in unit model 82. The oscilloscope must be calibrated immediately prior to starting an adjustment procedure.

Table 4-1. Spare Modules for RAD File Models 9367B and 9367C

Module	RAD File w/o Controller	RAD File with Controller
Signal Amplifier AH10		1
Read Input Control AK61	1	1
Y-Select AK62	1	1
Write-Driver AK63	2	2
Index/Sector Amplifier AK64	1	1
Write Clock Amplifier AK65	1	1
Cable Driver AX14	1	1
Cable Driver AX16		1
AND/OR Buffer BH10	1	2
DC Flip-Flop FH19		1
Basic Flip-Flop FH20		2
Basic Flip-Flop FL21	1	1

(Continued)

Table 4-1. Spare Modules for RAD File Models 9367B and 9367C (Cont.)

Module	RAD File w/o Controller	RAD File with Controller
Gate Expander GH14	1	1
Diode Gate GK51		2
Read Preamplifier HK73	1	1
Limiter HK74	1	1
Clock Discriminator HK75	1	1
Data Decoder HK76	1	1
Index/Sector Decoder HK77	1	1
AND/OR Inverter IH10		1
AND Gate/Inverter IH14	1	1
AND Gate/Inverter IL12	1	1
Relay Module KX12		1
Read-Write Decoder NK59	1	1
One-Shot Multivibrator OX12	1	1
Primary Power Detector SK60		1
+4v Regulator SX60	1	1
-8v Regulator SX69	1	1

4-9 Selection Unit Module Adjustments

+4v Regulator SX60. Adjust +4v regulator SX60 as follows:

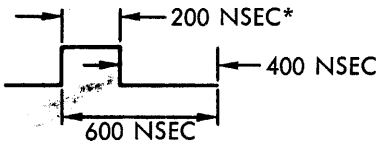
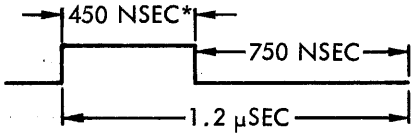
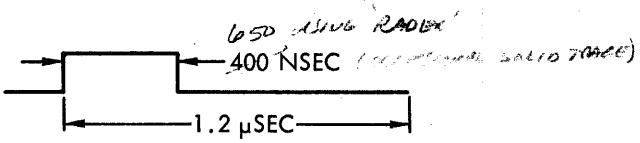
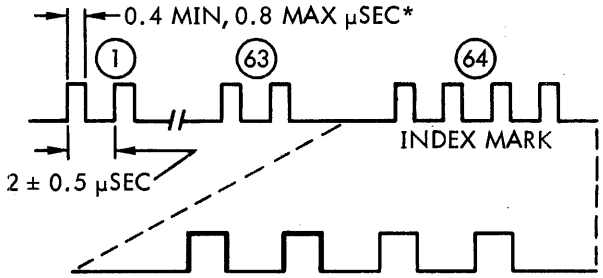
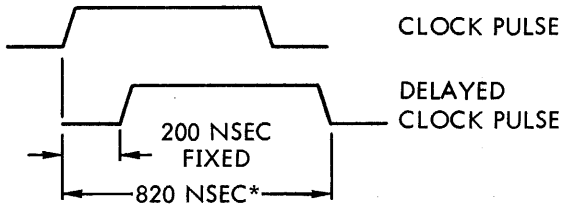
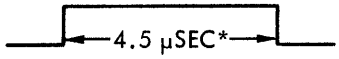
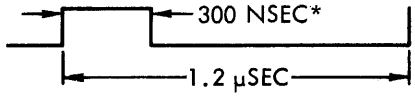
a. Connect oscilloscope to output terminal of regulator in selection unit location A12, pin 40, 41, or 42 (figure 4-2).

b. Adjust R9 for output of +4.00 (±0.04)v (figure 4-8).

-8v Regulator SX69. Adjust -8v regulator SX69 as follows:

a. Connect oscilloscope to output terminal of regulator in selection unit location A13, pin 36 or 37 (figure 4-2).

b. Adjust R6 for output of -8.00 (±0.08)v (see figure 4-8).

MODULE	ADJUSTMENT*	WAVEFORM
AK65 LOC B1	C4	
(SELECTION UNIT) OX12 LOC B2	R4--1 (LOWER)	
	R4--2 (UPPER)	
AK64 LOC B2	R24	
HK75 LOC C26	R26, R28	
OX12 (CONTROLLER) LOC C43	R4--2 (UPPER)	
	R4--1 (LOWER)	

*INDICATES CHANGE BY ADJUSTMENT LISTED.

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Figure 4-8. Adjustment Waveforms

Write Clock Amplifier AK65. Adjust write clock amplifier AK65 as follows:

a. Connect oscilloscope to output terminal of amplifier in selection unit location B1, pin 20 (figure 4-2).

b. Withdraw AK65 module from selection unit. Examine shield on the right-hand side to determine if a hole has been drilled in lower right-hand corner over trimmer capacitor adjustment screw. If not, drill 3/8-inch hole (figure 6-16).

c. Reinstall AK65 module.

d. Insert short non-metallic screwdriver (up to 4-inch length) through access hole in lower left-hand side of selection unit as viewed from front and inside of cabinet.

e. Adjust C4 for maximum output at 200 nsec minimum indication (figure 4-8).

Write Clock Multivibrator OX12. Adjust write clock multivibrator OX12 as follows (adjust read clock multivibrator as described in subsequent and separate adjustment procedure):

a. Connect oscilloscope to output of write clock multivibrator in selection unit location A11, pin 25 (figure 4-2).

b. Adjust R4-1 for positive pulse duration of 450 nsec within normal operating range of 350-550 nsec (figure 4-8 trace for R4-1).

Index-Sector Amplifier AK64. Adjust index-sector amplifier AK64 as follows:

a. Connect oscilloscope to output terminal of amplifier in selection unit location B2, pin 28 (figure 4-2). Use ~~positive~~ NEGATIVE internal synchronization.

b. Adjust R24 for maximum gain and fill-in. Pulses should have a duration of 0.4 to 0.8 μsec.

Note

Pulse train (top trace in figure 4-8 for R24) consists of 63 double timing pulses, followed by 64th double-double pulse. Lower trace shows double-double pulse. CRT persistence causes change in time base to show 63 double pulses stacked with a bright display and double-double index mark to show only faintly. Because of limiter output, control affects fill-in of missing pulses and pulse duration more than pulse amplitude. A low gain setting produces narrow or missing pulses.

Clock Discriminator HK75. Adjust clock discriminator HK75 as follows:

a. Disconnect controller by removing connector P170 from controller location C26 (figure 4-3).

b. If data in memory is known, that data may be used for test. If the data is not known, test program may be used. If not convenient to use test program, writing may be forced as follows:

1. Clip ground lead to AND Gate/Inverter IL12 in selection unit location A10, pin 22 (figure 4-4).

2. Use a second clip lead to connect momentary ground (duration of at least one memory revolution) on same module at pin 28.

3. Provide a read output by using second clip to connect ground to same module at pin 12.

Note

Use dual trace plug-in unit model 82 or equivalent with oscilloscope to display clock pulses and delayed clock pulses simultaneously in following steps. (If not available, the two traces may be examined separately and compared.)

c. Connect oscilloscope to clock output of discriminator in selection unit location A20, A23, A26, or A29, pin 40 (figure 4-4). Observe waveform (figure 4-8) and synchronize with leading edge of clock.

d. Connect oscilloscope to delayed clock output (pin 32) and synchronize with leading edge of clock.

e. Check that variable resistor R26 is in maximum clockwise position.

f. Verify fixed delay of 200 ns.

g. Adjust R28 for total clock time of 820 nsec.

h. Remove two grounds connected in step b.

i. Insert connector P170 in location C26 of controller.

Read Clock Multivibrator OX12. Adjust read clock multivibrator (location A11) as follows:

a. Connect oscilloscope to read clock multivibrator output in location A11, pin 22 (figure 4-3).

b. Connect clip leads as described in step b of procedure for clock discriminator HK75.

c. Disconnect controller by removing connector P170 from controller location C26 (figure 4-4).

d. Adjust potentiometer R4-2 for positive pulse duration of 400 (±50) ns (figure 4-8).

700 ?

e. Remove clip leads connected in step b.

f. Insert connector P170 in controller location C26 (figure 4-4).

4-10 SPECIAL TOOLS

The following special tools are provided for each drum memory:

Description	Bryant Part No.	Quantity
Head adjustment tool	B-AB-022	1
3/16 inch open end wrench	C-56650-1	1
Head squaring fixture	AD-087	1

Refer to Bryant handbook BCPH-101-5-64 for servicing information on drum memory.

SECTION V
PERFORMANCE TESTING AND TROUBLE ANALYSIS

5-1 PERFORMANCE TEST AND DIAGNOSTIC TEST FUNCTIONS

5-2 USE OF PERFORMANCE TESTS

The performance test is intended for use during installation, for major malfunction checkout, or as a preliminary test following major overhaul and repair. A major malfunction includes power failure, discontinuity or short circuits in power cable assemblies, and mechanical defects in modules, connectors, or switches. The performance test also includes the following: adjustment of power failure circuits; locations of test points for timing signals; and characteristics of timing signals and counters.

5-3 USE OF DIAGNOSTIC TEST PROGRAMS

The diagnostic test programs are intended for detailed trouble analysis of a RAD file using a typewriter to input/output a program stored in the SDS computer linked to the RAD file.

5-4 PERFORMANCE TEST PROCEDURE

The performance tests in the following paragraphs are for a RAD file connected to an SDS computer. Any operation prescribed for a RAD memory unit should be performed for all RAD memory units in the installation.

5-5 TEST EQUIPMENT

The following test equipment is required:

Tektronix 545A oscilloscope or equivalent

Tektronix Type CA preamplifier or equivalent

Triplet 630A VOM or equivalent.

5-6 SELECTION UNIT PERFORMANCE TEST

Test selection unit as follows:

a. Disconnect all ac/dc from controller, power protection panel, and RAD memory unit.

b. Remove all modules from controller and from selection unit of each RAD memory unit.

c. Check that all interconnecting cables are installed as indicated in figure 4-1.

d. Inspect selection unit for loose wires, bent pins, and other mechanical defects.

e. Perform continuity checks between selection unit and Power Supply Model PX13 as follows:

PX13	Selection Unit
GRD1, GRD2	A31-1, A32-44, B32-44, B32-1
+8v	A32-45, B32-45
-25v	A32-46, B32-46
+25v	A32-47, B32-47
+50v	A14-41, B11-41

f. Connect RAD memory unit to ac source.

CAUTION

Immediately after applying power in step g, verify that fans in RAD File Model 9367B rotate in correct direction. If fans rotate in reverse, set circuit breaker OFF before drum reaches operating speed. Reverse phase B and phase C power leads (figure 4-7) and repeat step g.

g. Set circuit breakers ON. Verify that fans rotate in direction indicated and that no abnormal sounds (such as scraping or scratching) are audible in the memory unit.

CAUTION

Do not remove or insert modules while power is applied.

h. On Power Supply Model PX13, set POWER switch ON. Measure for following voltages:

Location	Voltage
A32-45, B32-45	+8v
A32-46, B32-46	-25v
A32-47, B32-47	+25v
A14-41, B11-41	+50v

i. At Power Supply Model PX13, set POWER switch OFF. Insert all modules except cable plug modules as indicated in figures 4-2 and 4-3.

j. At Power Supply Model PX13, set POWER switch ON. Adjust voltage margin knob to obtain nominal voltages for +8v, -25v, +25v, and +50v outputs.

k. At selection unit, adjust trimpot on SX60 module for +4.00 (±0.004)v at A12-40.

l. Adjust trimpot on SX69 module for -8.00 (±0.08)v at A13-36.

m. Observe the signals listed in table 5-1 for indicated characteristics. Adjust to tolerance of ±10 percent unless otherwise indicated.

n. Simulate unit select signal by connecting pin A1-43 to ground. Observe sector counter output at following points to verify that all signals are false during sector time preceding index pulse and true during sector time following index pulse:

Signal	Test Point	Pulse Repetition Rate
9CD6S	A1-14	1 ms
9CD5S	A1-13	2 ms
9CD4S	A1-12	4 ms
9CD3S	A1-11	8 ms
9CD2S	A1-10	16 ms
9CD1S	A1-9	33 ms

o. Use clip leads to connect sector counter to Y-select input as follows:

Sector Counter	Y-Select
A3-3	A9-6
A3-13	A9-13
A3-23	A9-20
A3-33	A9-27
A2-3	A9-34

Note

Terminate step p after observing Y8 for models -01 and -11, Y16 for models -02 and -12, and Y32 for models -04 and -14. Sector times 33 to 64 repeat sector times 1 to 32.

p. Synchronize oscilloscope on index pulse. Verify that Y-select outputs are 0v during sector times indicated in table 5-2 and +25v otherwise.

Note

Terminate step q after switch 030-037 for -01 and -11 models, switch 070-077 for -02 and -12 models, and switch 017-177 for -04 and -14 models.

Table 5-1. RAD Memory Unit Test Signals

Function	Mnemonic	Test Point
Basic Write Clock Pulse width: 200 ns Pulse period: 620 ns ± 20 ns Sync: internal positive Adjust capacitor on B-01 (through access hole) for maximum pulse width with minimum jitter	0WCAS	B01-20
Half-Frequency Write Clock Pulse width: 620 ns ± 20 ns Pulse period: 1.24 μs ± 0.04 μs Sync: internal positive	0WCKS	A02-23
Write Clock One-Shot Pulse width: 450 ns Pulse period: 1.24 μs ± 0.04 μs Sync: internal positive Adjust lower trimpot on all for pulse width of 450 ns	0WCOS	A11-25

(Continued)

Table 5-1. RAD Memory Unit Test Signals (Cont.)

Function	Mnemonic	Test Point
Index Sector Amplifier See figure 4-8 for definition of signal characteristics Adjust trimpot on B02 to obtain 750 ns duration of first negative pulse Sync: internal negative	2SIDS	B02-28
Index Pulse Pulse width: 2.5 μs ± 0.5 μs Pulse period: 33.8 ms ± 0.3 ms Sync: internal positive	2IDXS	B03-10
Sector Pulse Pulse width: 2.5 μs ± 0.5 μs Pulse period: 527 μs ± 4 μs Sync: 0B-03-10 (index pulse) One pulse missing at index time	2SECS	B03-03
Sector Index Mark Pulse width: 2.5 μs ± 0.5 μs Pulse period: 527 μs ± 4 μs Sync: 0B-03-10 (index pulse) Inverted sum of sector pulse and index pulse	3SIMS	A02-38
Y-Select Control Pulse width: 3.4 μs ± 0.8 μs Pulse period: 527 μs ± 5 μs Sync: 0B-03-10 (index pulse) Use a delayed sweep to compare signal 1YSCS with signal 3SIMS (0A-02-38). The positive-going edge of signal 1YSCS must be later than signal 3SIMS by 0.6 μs minimum, or 1.4 μs maximum	1YSCS	A09-33

Table 5-2. Y-Select Output Timing

Signal	Y-Select Output	Sector Time Selected
Y01	B12-34	1
Y02	B12-32	2
Y03	B12-10	3
Y04	B12-09	4
Y05	B13-34	5
Y06	B13-32	6
Y07	B13-10	7
Y08	B13-09	8
Y09	B14-34	9
Y10	B14-32	10
Y11	B14-10	11
Y12	B14-09	12
Y13	B15-34	13
Y14	B15-32	14
Y15	B15-10	15
Y16	B15-09	16

(Continued)

Table 5-2. Y-Select Output Timing (Cont.)

Signal	Y-Select Output	Sector Time Selected
Y17	B16-34	17
Y18	B16-32	18
Y19	B16-10	19
Y20	B16-09	20
Y21	B17-34	21
Y22	B17-32	22
Y23	B17-10	23
Y24	B17-09	24
Y25	B18-34	25
Y26	B18-32	26
Y27	B18-10	27
Y28	B18-09	28
Y29	B19-34	29
Y30	B19-32	30
Y31	B19-10	31
Y32	B19-09	32

q. Check that all write-protect switches are in down position, and that signal 2WLKS measured at pin A8-2 is false. Check that signal 2WLKS is true during sectors indicated in table 5-3 as each write-protect switch is individually placed in up position.

r. Remove clip leads connected in step o.

s. Simulate write-enable signal (9WENA) by connecting pin A1-22 to ground. A pattern should be written in channel 0.

t. Remove ground from pin A1-22 and simulate 9RENA read-enable signal by connecting pin A1-30 to ground.

u. Observe signals listed in table 5-4 and adjust to ±10 percent tolerance unless otherwise indicated. Measure all pulse durations at 50 percent level.

Table 5-3. Write-Protect Switch Timing

Switch	Sector Time	Switch	Sector Time
000-007	1, 2	100-107	17, 18
010-017	3, 4	110-117	19, 20
020-027	5, 6	120-127	21, 22
030-037	7, 8	130-137	23, 24
040-047	9, 10	140-147	25, 26
050-057	11, 12	150-157	27, 28
060-067	13, 14	160-167	29, 30
070-077	15, 16	170-177	31, 32

Table 5-4. Selection Unit Test Signals

Function		Mnemonic	Test Point
Limiter Output	(Track 1)	0RCL1	B21-34
Pulse width: 0.6 μs Pulse period: 1.24(±0.04)μs Average dc level: -2v	(Track 2) (Track 3)	0RCL2 0RCL3	B24-34 B27-34
Amplitude: 1.6v Sync: internal	(Track 4)	0RCL4	B30-34
Read Clock	(Track 1)	RC01	A20-40
Pulse width: 0.6 μs Pulse period: 1.24(±0.04)μs Average dc level: +3v Amplitude: 2.1v Sync: use read clock RC0x as sync for delayed read clock RCDx for same track. See delayed read clock	(Track 2) (Track 3) (Track 4)	RC02 RC03 RC04	A23-40 A26-40 A29-40
Delayed Read Clock	(Track 1)	RCD1	A20-32
Pulse width: 0.6 μs Pulse period: 1.24(±0.04)μs Average dc level: 1.5v Amplitude: 1.6v Delay: 200 ns after read clock Sync: sync delayed read clock RCDx on test point of corresponding read clock RC0x Adjustment: observe RC0x on one trace and RCDx on other trace. Turn lower trimpot on module maximum clockwise, then adjust upper trimpot for 800 (±20) ns from rise of RC0x to fall of RCDx	(Track 2) (Track 3) (Track 4)	RCD2 RCD3 RCD4	A23-32 A26-32 A29-32

(Continued)

Table 5-4. Selection Unit Test Signals

Function		Mnemonic	Test Point
Read Clock Strobe	(Track 1)	RCS1	A21-32
Pulse width: 200 (±50) ns	(Track 2)	RCS2	A24-32
Pulse period: 1.24 (±0.04) μs	(Track 3)	RCS3	A27-32
Sync: internal	(Track 4)	RCS4	A28-32
Sine Wave in Read Clock Stabilizer			A31-TP1
Approximate amplitude: 5v Adjustment: adjust for maximum amplitude			

5-7 CONTROLLER PERFORMANCE TEST

Test controller as follows:

a. Inspect controller for bent pins, broken wires, and other evidence of mechanical defects.

b. Verify voltage bus bars are correctly installed and that mechanical connections are tight 5 (figure 4-2).

c. Perform continuity tests on power fail-safe wiring as follows:

Power Protection Panel	Controller
TB1-E-5	D29-12
TB1-E-4	D29-14
TB1-E-3	D29-13
TB2-E-5	D28-12
TB2-E-4	D28-14
TB2-E-3	D28-13

d. Perform continuity tests between controller power source and controller as follows:

Controller Power Source	Controller
+25v	A45-47
	B45-47
	C45-47
	D45-47
-25v	A45-46
	B45-46
	C45-46
	D45-46
+8v	A45-45
	B45-45
	C45-45
	D45-45
0v	A45-44
	B45-44
	C45-44
	D45-44

e. Turn on controller power source.

f. Measure following voltages:

+25v	A45-47
-25v	A45-46
+8v	A45-45
0v	A45-44

g. Turn off controller power source.

h. Insert following modules in controller:

D27	Relay Module KX12
D28	Primary Power Detector SK60
D29	Primary Power Detector SK60

h. At controller power source, turn power on and set power supplies for nominal voltage values, if necessary.

j. Connect 30-foot ac cord from power protection panel to ac plug mold in RAD memory unit.

k. Connect 10-foot power cord from power protection panel to computer ac source.

l. Adjust D29 power fail-safe detection circuit as follows:

1. Measure and record voltage Vp (nominal 115 vac) between terminal TB1-1 and terminal TB1-2 of power protection panel.

2. Measure and record voltage Vs (nominal 10 vac) between terminal TB1-3 and terminal TB1-5 of power protection panel.

3. From recorded values compute: Vb = (70.7Vs/Vp) - 0.4.

4. Measure voltage between test point D29-14 and ground. Adjust trimpot on SK60 module in location D29 so that measured voltage equals that calculated in step l3.

m. Adjust D28 power fail-safe detection circuit as follows:

1. Measure and record voltage Vp (nominal 115 vac) between terminal TB2-1 and TB2-2 of power protection panel.

2. Measure and record voltage Vs (nominal 10 vac) between terminal TB2-3 and TB2-5 of power protection panel.

3. From recorded values compute: Vb = (70.7Vs/Vp) - 0.4.

4. Measure voltage between test point D28-14 and ground. Adjust trimpot on SK60 module in location D28 so that measured voltage equals that calculated in step m3.

n. Turn off controller power supply.

o. Insert following modules:

C38	AND Gate/Inverter IH14
C40	Signal Amplifier AH10

p. Turn on controller power source.

q. Verify that signal 8PWRA at test point C40-1 is +8 vdc nominal (true).

r. Remove ac connection between power protection panel and controller. Verify that signal 8PWRA is 0 vdc nominal (false). Reconnect ac line.

s. Turn off controller power source.

t. Insert all remaining controller modules as indicated in figure 4-3.

u. Verify that all RAD file power supplies are on.

v. Measure signals listed in table 5-5 for indicated characteristics.

5-8 TROUBLE ANALYSIS

5-9 DIAGNOSTIC PROGRAM DOCUMENTS

For detailed trouble analysis refer to information contained in the following documents:

SDS Computer Model	Document Number	Title
SDS 92	SDS 794004	SDS 92 RAD Analytic Diagnostic
SDS 925, 930	SDS 594003	SDS 925/930 RAD Apocalyptic Diagnostic
SDS 9300	SDS 604004	SDS Automatic Instruction Diagnostic Program for Computer Model 9300
SDS 900 Series	SDS 004009	SDS 910, 920, 925, 930, or 9300 Diagnostic Control Program
SDS 9300	SDS 694010	SDS 9300 RAD Apocalyptic Diagnostic

For RAD file tests, refer to SDS publication 004009, and the applicable computer document. SDS publication 004009 includes information common to all diagnostic programs for SDS 900 series computers.

5-10 USE OF DIAGNOSTIC PROGRAM DOCUMENTS

The program documents describe a set of directives (instructions) to write a program to test part or all of a RAD file.

Table 5-5. Controller Test Signals

Function	Mnemonic	Test Point
Basic Clock Pulse Pulse width: 0.45 μs Pulse period: 1.2 μs	4CLKA	B36-01
Sector Pulse Pulse width: 2 μs Pulse period: 500 μs	2SIPA	C43-18
Begin Sector Pulse Pulse width: adjustable Top Pot to 4.5 μs Pulse period: 500 μs. (To test signal connect test point A33-04 to ground)	0BSCA	C43-22
Strobe Pulse Pulse width: adjustable Bottom Pot to 280 ns Pulse period: 1.2 μs	0STVA	C43-25
Ripple Counter (LSB changes state at approximately 500 μs intervals)	2CD6S (LSB) 2CD5S 2CD4S 2CD3S 2CD2S 2CD1S (MSB)	C32-25 C32-32 C32-33 C32-40 C31-01 C31-08

SECTION VI
PARTS LIST

6-1 SCOPE OF SECTION

Figures 6-1 through 6-30 locate and identify all replaceable items in assemblies, subassemblies, and modules of RAD File Models 9367B and 9367C. Tables 6-1 through 6-24 facilitate parts replacement ordering. For parts identification of Power Supply Model PX13 components, consult SDS publication 900001.

6-2 USE OF TABLES

The tables are keyed to the parts identification figures in this section and to the schematic diagrams in section VIII. Refer to table 6-24 for a list of manufacturer code numbers.

6-3 PARTS BREAKDOWN

The parts complement of a RAD file installation depends on the number of RAD memory units included, the power source frequency, and the maximum memory size. A basic RAD file consists of a controller, power protection panel, cable assemblies, and RAD memory unit. A RAD file installation with one RAD memory unit requires all cable assemblies except plug module cable assembly P168/P169 (figure 1-2). A plug module cable assembly P168/P169 is required to connect each additional RAD memory unit. The RAD memory unit ac supply cable is integral to the RAD memory unit.

Power Supply Model PX13 provides sufficient power for two selection units. A one or two RAD memory unit installation requires one power supply; a three or four RAD memory unit installation needs two power supplies.

Table 6-1. RAD File Models 9367B and 9367C Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-1	Rapid Access Data File Model 9367B		SDS	*	
6-1	Rapid Access Data File Model 9367C		SDS	†	
6-2	. Assembly, Cable, Plug Module P155/P156 (see table 6-2)		SDS	113899	1
6-3	. Assembly, Cable, Plug Module P157/P158 (see table 6-3)		SDS	113902	1
6-4	. Assembly, Cable, Plug Module P159/P160 (see table 6-4)		SDS	113896	1
6-5	. Assembly, Cable, Plug Module P161/P162 (see table 6-5)		SDS	116388	1
6-6	. Assembly, Cable, Plug Module P168/P169 (see table 6-6)		SDS	116509	**
6-7	. Assembly, Cable, Plug Module P170/P171 (see table 6-7)		SDS	116513	1
6-9	. Panel, Power Protection (see table 6-8)		SDS	116989	1
6-10	. Controller (see table 6-9)		SDS	131564	1
6-10	. RAD Memory Unit (see table 6-10)		SDS	*	*
6-11	. RAD Memory Unit (see table 6-11)		SDS	†	†

*See table 1-1 for part numbers and model differences. RAD memory unit containing drum used with RAD File Model 9367B

†See table 1-1 for part numbers and model differences. RAD memory unit containing disc used with RAD File Model 9367C

**Required for each additional RAD memory unit connected to basic RAD file installation (figure 1-2)

Table 6-2. Plug Module Cable Assembly P155/P156 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-2	Plug Module Cable Assembly P155/P156 (see table 6-1 for next higher assembly)			113899	1
6-2	. Board, printed wiring	P155	SDS	100682-016	1
6-2	. Board, printed wiring	P156	SDS	111197-016	1
6-8	. Diode, SDS 103 (100091)	CR1 thru CR27	3	FD100	27
6-8	. Inductor, molded, 10 μh (100342-103)	L1 thru L3	41	1537	3
6-8	. Resistor, 100 ohm, 2%, 1/2w (100111-101)	R1 thru R3	96	E009	3
6-8	. Resistor, 8200 ohm, 2%, 1/2w (100111-822)	R4 thru R30	96	E009	27

Table 6-3. Plug Module Cable Assembly P157/P158 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-3	Plug Module Cable Assembly P157/P158 (see table 6-1 for next higher assembly)			113902	1
6-3	. Board, printed wiring	P157	SDS	100682-026	1
6-3	. Board, printed wiring	P158	SDS	111197-020	1
6-8	. Diode, SDS 103 (100091)	CR1 thru CR11	3	FD100	11
6-8	. Inductor, molded, 10 μh (100342-103)	CR1 thru CR31	41	1537	31
6-8	. Inductor, molded, 4.7 μh (100342-472)	CR32	41	1537	1
6-8	. Resistor, 100 ohm, 2%, 1/2w (100111-101)	R1 thru R31	96	E009	31
6-8	. Resistor, 8200 ohm, 2%, 1/2w (100111-822)	R33 thru R43	96	E009	11
6-8	. Resistor, 47 ohm, 2%, 1/2w (100111-470)	R32	96	E009	1

Table 6-4. Plug Module Cable Assembly P159/P160 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-4	Plug Module Cable Assembly P159/P160 (see table 6-1 for next higher assembly)			113896	1
6-4	. Board, printed wiring	P159	SDS	100682-020	1
6-4	. Board, printed wiring	P160	SDS	111197-026	1
6-8	. Diode, SDS 103 (100091)	CR1 thru CR5	3	FD100	5
6-8	. Inductor, molded, 10 μh (100342-103)	L1 thru L40	41	1537	40
6-8	. Resistor, 100 ohm, 2%, 1/2w (100111-101)	R1 thru R40	96	E009	40
6-8	. Resistor, 8200 ohm, 2%, 1/2w (100111-822)	R41 thru R43	96	E009	3

Table 6-5. Plug Module Cable Assembly P161/P162 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-5	Plug Module Cable Assembly P161/P162 (see table 6-1 for next higher assembly)			116388	1
6-5	. Board, printed wiring	P161	SDS	111197-024	1
6-5	. Board, printed wiring	P162	SDS	100682-018	1
6-8	. Diode, SDS 103 (100091)	CR1 thru CR20	3	FD100	20
6-8	. Inductor, molded, 10 μh (100342-103)	L1 thru L20	41	1537	20
6-8	. Resistor, 100 ohm, 2%, 1/2w (100111-101)	R1 thru R20	96	E009	20
6-8	. Resistor, 8200 ohm, 2%, 1/2w (100111-822)	R21 thru R40	96	E009	20

Table 6-6. Plug Module Cable Assembly P168/P169 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-6	Plug Module Cable Assembly P168/P169 (see table 6-1 for next higher assembly)		SDS	116509	*
6-8	. Board, printed wiring	P168, P170	SDS	111197-020	1
6-8	. Board, printed wiring	P169, P171	SDS	111197-018	1

*Required for each RAD memory unit connected to basic RAD file installation (figure 1-2)

Table 6-7. Plug Module Cable Assembly P170/P171 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-7	Plug Module Cable Assembly P170/P171 (see table 6-1 for next higher assembly)		SDS	116513	1
6-8	. Board, printed wiring	P170	SDS	111197-020	1
6-8	. Board, printed wiring	P171	SDS	111197-018	1
6-8	. Resistor, 330 ohm, 2%, 1/2w	R1	96	E009	1
6-8	. Resistor, 47 ohm, 2%, 1/2w	R2 thru R14	96	E009	13
6-8	. Inductor, molded, 10 μh, 10%	L1 thru L13	41	1537	13

Table 6-8. Power Protection Panel, Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-7	Power Protection Panel (see table 6-1 for next higher assembly)		SDS	116989	1
-1	. Plug, male, 3-contact (106691)	P1, P2	106	5266	2
-2	. Transformer, filament, 115v primary, 10v secondary, 4 amp (101126)	T1, T2	151	P5016	2
-3	. Resistor, 33 ohm, 2%, 1w (110996-330)	R1 thru R4	16	C-32	4
-4	. Block, terminal (100094-005)	TB1, TB2	219	601	2

Table 6-9. Controller Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-10	Controller, (see table 6-1 for NHA)		SDS	131564	
6-10-1	. Assembly, chassis		SDS	131823	1
7-23	. Assembly, 20-module chassis		SDS	101141	4
6-10-2	. Module, Signal Amplifier AH10	*	SDS	100839	5
6-10-3	. Module, Cable Driver AX14	*	SDS	102853	5
6-10-4	. Module, Cable Driver AX16	*	SDS	114269	2
6-10-5	. Module, AND/OR Buffer Amplifier BH10	*	SDS	100164	10
6-10-6	. Module, DC Flip-Flop FH19	*	SDS	103134	5
6-10-7	. Module, Basic Flip-Flop FH20	*	SDS	105169	13
6-10-8	. Module, Basic Flip-Flop FL21	*	SDS	110552	1
6-10-9	. Module, Diode Gate No. 1 GK51	*	SDS	100246	19
6-10-10	. Module, AND/OR Inverter IH10	*	SDS	100137	2
6-10-11	. Module, AND Gate/Inverter IH14	*	SDS	104362	8
6-10-12	. Module, Relay KX12	*	SDS	106327	1
6-10-13	. Module, One-Shot Multivibrator OX12	*	SDS	103459	1
6-10-14	. Module, Primary Power Detector SK60	*	SDS	106586	2

*See table 1-5 for reference designations of modules

Table 6-10. RAD Memory Unit With Drum Memory Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-1	RAD Memory Unit (see table 6-1 for NHA)		SDS	*	
6-1-1	. Assembly, cabinet		SDS	131353	1
7-24	. . Receptacle, male, 5-contact	J1	106	3525	1
7-24	. . Panel, filter		SDS	131642	1
7-24	. . Filter, air		300	5251F	2
6-1-10	. . Plug mold, ac		103	G-20GB 306	1
7-24	. . Connector, butt		111	320562	1
6-1-7	. . Assembly, top fan		SDS	123943	2
7-24	. . Cord, Power		SDS	133669	1
7-24	. . . Connector, female, 5-contact		364	45000	1
7-24	. . . Connector, male, 5-contact		364	45000	1
6-23	. . Assembly, Panel, Power distribution		SDS	131365	1
6-23-2	. . . Circuit breaker, 35 amp, 3-pole	CB2	186	220-235-101	1
6-23-1	. . . Circuit breaker, 25 amp, 2-pole	CB1	186	195-225-101	1
6-1-6	. . Power supply PX13		SDS	101270	1†
6-1-8	. . Power supply PX14		SDS	101271	1†
6-1-9	. . Selection unit (see table 6-12 for breakdown)		SDS	129484	1
6-1-11	. . Drum memory		SDS	127898*	1
6-25	. . Assembly, cable, circuit breaker		SDS	131825	
6-25	. . . Connector, female, 11-pin	P101	227	BT06A-18-11S	1
6-26	. . Assembly, cable		SDS	133304	1
6-24	. . Assembly, cable, drum matrix		SDS	131623	1
6-24-1	. . . Connector, male, 50-pin	P11, P22	51	57-40500	2
6-24-2	. . . Connector, male, 75-pin	P2, P4	110	MRAC-75P-JTD-H8	2
6-28	. . Assembly, cable, drum clock			132238	1
6-28-1	. . . Connector, male, 50-pin	P33	51	57-40500	1
6-28-2	. . . Connector, male, 75-pin	P3	110	MRAC-75P-JTD-H8	1

*See table 1-1 for part numbers and model differences

†Not used in -1X models; see table 1-1

Table 6-11. RAD Memory Unit With Disc Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-1	RAD Memory Unit (See table 6-1 for NHA)		SDS	*	
6-1-1	. Assembly, cabinet		SDS	131353	1
7-24	. . Receptacle, male, 5-contact	J1	106	3525	1
7-24	. . Panel, filter		SDS	131642	1
7-24	. . Filter, air		300	5251F	2
6-1-10	. . Plug mold, ac		103	G-20GB 306	1
7-24	. . Connector, butt		111	320562	1
6-1-7	. . Assembly, top fan		SDS	123943	2
7-24	. . Cord, power		SDS	133669	1
7-24	. . . Connector, female, 5-contact		364	45000	1
7-24	. . . Connector, male, 5-contact		364	45000	1
6-23	. . Assembly, panel, power distribution		SDS	131365	1
6-23-2	. . . Circuit breaker, 35 amp, 3-pole	CB2	186	220-235-101	1
6-23-1	. . . Circuit breaker, 25 amp, 2-pole	CB1	186	195-225-101	1
6-1-9	. . Selection unit (see table 6-12)		SDS	129484	1
6-1-6	. . Power supply		SDS	101270	1†
6-1-8	. . Power supply		SDS	101271	1†
7-24	. . Disc memory		SDS	115621	1
6-26	. . Assembly, cable		SDS	133304	1
6-30	. . Assembly, cable, disc matrix		SDS	131620	1
6-30-1	. . . Connector, female, 50-pin	P22, P11	324	17-830	2
6-30-2	. . . Connector, female, 130-pin	P3	82	8017-130-000-011	1
6-29	. . Assembly, cable, disc clock		SDS	132240	1
6-29-2	. . . Connector, female, 50-pin	P7	324	17-830	1
6-29-1	. . . Connector, male, 15-pin	P33	51	DASM-15S	1
6-29-3	. . . Hood, connector		51	DA-20961	1

*See table 1-1 for part numbers and model differences

†Not required in -IX models; see table 1-1

Table 6-12. Selection Unit Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-11	Selection Unit (See tables 6-10 and 6-11 for NHA)		SDS	129484	
6-11-1	. Assembly, chassis		SDS	131393	1
6-11-2	. . Assembly, 32-module chassis, upper		SDS	104911	1
6-11-3	. . Assembly, 32-module chassis, lower		SDS	104912	1
4-2	. . Block, terminal, molded barrier		51	141	4
6-11-4	. . Switch, toggle		106	TS-3A	16
6-11-5	. . Connector, female, 50-pin		51	57-40500	3
6-11-23	. . Module, Read Input Control AK61 (see table 6-13)	*	SDS	131027	1
6-11-24	. . Module, Y-Select AK62 (see table 6-14)	*	SDS	131029	†
6-11-10	. . Module, write driver AK63 (see table 6-15)	*	SDS	131031	16
6-11-26	. . Module, index/sector amplifier AK64 (see table 6-16)	*	SDS	131043	1
6-11-27	. . Module, write clock amplifier AK65 (see table 6-17)	*	SDS	131047	1
6-11-18	. . Module, cable driver AX14	*	SDS	102853	3
6-11-17	. . Module, AND/OR buffer amplifier BH10	*	SDS	100164	1
6-11-15	. . Module, dc flip-flop FH19	*	SDS	103134	1
6-11-7	. . Module, basic flip-flop FL21	*	SDS	110552	4
6-11-16	. . Module, gate expander GH14	*	SDS	104431	1
6-11-21	. . Module, read preamplifier HK73 (see table 6-18)	*	SDS	131035	4
6-11-22	. . Module, limiter HK74 (see table 6-19)	*	SDS	131037	4
6-11-8	. . Module, clock discriminator HK75 (see table 6-20)	*	SDS	131039	4
6-11-9	. . Module, data decoder HK76 (see table 6-21)	*	SDS	131041	4
6-11-25	. . Module, index/sector decoder HK77 (see table 6-22)	*	SDS	131045	1
6-11-14	. . Module, AND gate/inverter IL12	*	SDS	108075	1
6-11-20	. . Module, read-write decoder NK59 (see table 6-23)	*	SDS	131033	4

*See table 1-6 for reference designations of modules
†Two for -X1 Models
Four for -X2 Models
Eight for -X4 Models

(Continued)

Table 6-12. Selection Unit Replaceable Parts (Cont.)

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-11-13	. . Module, one-shot multivibrator OX12	*	SDS	103459	1
6-11-12	. . Module, +4v regulator SX60	*	SDS	110727	1
6-11-11	. . Module, -8v regulator SX69	*	SDS	126999	1

*See table 1-6 for reference designations of modules

Table 6-13. Read Input Control AK61 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-12	Read Input Control AK61 (See table 6-12 for NHA)		SDS	131027	
	. Capacitor, silver mica, 30 pf, 5%, 300v	C1	188	1459	1
	. Capacitor, tantalum, 1.5 µf, 20%, 6v	C2	11	ECM	1
	. Capacitor, tantalum, 4.7 µf, 20%, 50v	C3, C4	192	GA901	2
	. Capacitor, tantalum, 5.6 µf, 20%, 15v	C5, C6	11	ECM	2
	. Diode, SDS 103	CR1-CR4, CR7, CR8	3	FD100	20
	. Diode, SDS 104	CR5, CR6	3	FD-6	2
	. Diode, SDS 101	VR1-VR3	11	1N746	6
	. Resistor, 3.9k, 2%, 1/2w	R1, R4, R6	96	E009	6
	. Resistor, 18k, 2%, 1/2w	R2, 5	96	E009	5
	. Resistor, 680 ohms, 2%, 1/2w	R3	96	E009	4
	. Resistor, 1k, 2%, 1w	R7	16	C-32	1
	. Resistor, 220 ohms, 2%, 1/2w	R8	96	E009	1
	. Resistor, 680 ohms, 2%, 1w	R9	16	C-32	1
	. Resistor, 1.5k, 2%, 1w	R10	16	C-32	1
	. Resistor, 200 ohms, 5%, 1/2w	R11	11	CD 1/2	1
	. Transistor, SDS 216	Q1	3	S6156	4
	. Transistor, SDS 201	Q2, Q3	3	S6325	2
	. Transistor, SDS 226	Q4	3	S6486	1
	. Transistor, SDS 214	Q5	3	S6262	1

Table 6-14. Y-Select AK62 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-13	Y-Select AK62 (See table 6-12 for NHA)				
	. Capacitor, tantalum, 4.7 μf, 20%, 50v	C1, C2	192	GA901	2
	. Capacitor, tantalum, 5.6 μf, 20%, 15v	C3	11	ECM	1
	. Diode, SDS 103	CR1-CR7, CR10	3	FD100	30
	. Diode, SDS 104	CR8, CR9	3	FD-6	4
	. Diode, SDS 101	VR1, VR2	11	1N746	6
	. Resistor, 8.2k, 2%, 1/2w	R1, R8	96	E009	6
	. Resistor, 27k, 2%, 1/2w	R2	96	E009	4
	. Resistor, 15k, 2%, 1/2w	R3	96	E009	4
	. Resistor, 750 ohms, 2%, 1/2w	R4	96	E009	4
	. Resistor, 91 ohms, 2%, 1w	R5	16	C-32	4
	. Resistor, 4.7k, 2%, 1/2w	R6	96	E009	4
	. Resistor, 2k, 2%, 1w	R7	16	C-32	4
	. Resistor, 39k, 2%, 1/2w	R9	96	E009	2
	. Resistor, 1k, 2%, 1/2w	R10	96	E009	2
	. Resistor, 200 ohms, 5%, 1/2w	R11	11	CD 1/2	1
	. Transistor, SDS 216	Q1, Q4	3	S6156	6
	. Transistor, SDS 214	Q2	3	S6262	4
	. Transistor, SDS 226	Q3	3	S6486	4

Table 6-15. Write-Driver AK63 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-14	Write-Driver AK63 (See table 6-12 for NHA)		SDS	131031	
	. Capacitor, tantalum, 5.6 µf, 20%, 15v	C1	11	ECM	1
	. Capacitor, tantalum, 1 µf, 20%, 50v	C2	11	ECM	1
	. Capacitor, tantalum, 4.7 µf, 20%, 50v	C3	11	ECM	1
	. Capacitor, mylar, 4.7 nf, 10%, 80v	C4, C9	192	608	2
	. Capacitor, mylar, 10 nf, 10%, 80v	C10	192	608	1
	. Capacitor, mica, 22 pf, 5%, 300v	C11, C12	188	1459	2
	. Capacitor, tantalum, 6.8 µf, 20%, 6v	C13	11	ECM	1
	. Capacitor, mylar, 1 nf, 10%, 80v	C14, C15	192	608	2
	. Diode, SDS 123	CR1-CR3, CR17, CR5-CR14, CR18, CR34-CR37, CR28, CR31	3	FD6	21
	. Diode, SDS 122	CR15, CR16, CR19-CR27, CR29 CR30, CR32, CR38, CR39	11	GD70	16
	. Diode, SDS 101 3.3v, 4w.	VR1-VR3, VR7-VR10	11	1N746	7
	. Diode, SDS 106 5.6v	VR4, VR11, VR12	11	F1180	3
	. Resistor, 2 ohms, 5%, 1w	R1, R2, R24	36	BWH	3
	. Resistor, 18k, 2%, 1/2w	R3	96	E009	1
	. Resistor, 1.5k, 2%, 1/w	R4, R11, R12	16	C-32	3
	. Resistor, 10k, 2%, 1/2w	R5, R10, R13, R22, R23, R33, R37, R41, R45	96	E009	9
	. Resistor, 10 ohms, 2%, 1/2w	R6, R9, R17, R18	96	E009	4
	. Resistor, 15k, 2%, 1/2w	R7, R8	96	E009	2
	. Resistor, 715 ohms, 1%, 1w	R14, R21	36	CES	2
	. Resistor, 619 ohms, 1%, 1w	R15, R20	36	CES	2

(Continued)

Table 6-15. Write-Driver AK63 Replaceable Parts (Cont.)

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-14 (Cont.)	. Resistor, 562 ohms, 1%, 1w	R16, R19	36	CES	2
	. Resistor, 910 ohms, 2%, 1w	R25, R29	16	C-32	2
	. Resistor, 15k, 2%, 1w	R26, R28	16	C-32	2
	. Resistor, 100 ohms, 2%, 1w	R27	16	C-32	1
	. Resistor, 470 ohms, 2%, 1w	R30	16	C-32	1
	. Resistor, 4.7k, 2%, 1/2w	R31	96	E009	1
	. Resistor, 6.2k, 2%, 1/2w	R32, R36, R40, R44	96	E009	4
	. Resistor, 3.9k, 2%, 1/2w	R34, R38, R42, R46	96	E009	4
	. Resistor, 1.1k, 2%, 1/2w	R47, R49	96	E009	2
	. Resistor, 1.5k, 5%, 1/4w	R50	11	GP 1/4	1
	. Transformer	T1	39	2ZNHA	1
	. Transistor, SDS 238	Q1, Q3-Q6	3	3517	5
	. Transistor, SDS 226	Q2, Q7, Q8	3	S6486	3
	. Transistor, SDS 216	Q9-Q16	3	S6156	8

Table 6-16. Index/Sector Amplifier AK64 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-15	Index/Sector Amplifier AK64 (See table 6-12 for NHA)			131043	
	. Capacitor, tantalum, 5.6 μf, 20%, 15v	C1, C4	11	ECM	2
	. Capacitor, tantalum, 4.7 μf, 20%, 50v	C2, C3	11	ECM	2
	. Capacitor, mica, 510 pf, 5%, 300v	C5	188	1459	1
	. Capacitor, mica, 330 pf, 5%, 300v	C6	188	1459	1
	. Capacitor, mylar, 10 nf, 10%, 80v	C7, C10	192	608	2
	. Capacitor, mylar, 47 nf, 10%, 80v	C8, C9, C11, C12	192	608	4
	. Capacitor, tantalum, 120 nf, 20%, 15v	C13	11	ECM	1
	. Capacitor, mylar, 100 nf, 10%, 80v	C14	192	608	1
	. Diode, SDS 122	CR5-CR16	11	GD70	12
	. Potentiometer, 2.5k, 10%, 1w	R24	35	275P-584	1
	. Resistor, 2 ohms, 5%, 1w	R1, R12	36	BWH	2
	. Resistor, 30 ohms, 2%, 1w	R2	16	C-32	1
	. Resistor, 390 ohms, 2%, 1/2w	R3	96	E009	1
	. Resistor, 1.8k, 2%, 1/2w	R4	96	E009	1
	. Resistor, 1k, 2%, 1/2w	R5	96	E009	1
	. Resistor, 10 ohms, 2%, 1/2w	R6, R7	96	E009	2
	. Resistor, 43 ohms, 2%, 1w	R11	16	C-32	1
	. Resistor, 1.5k, 1%, 1/8w	R13	36	CCM	1
	. Resistor, 3.01k, 1%, 1/8w	R14, R41	36	CCM	2
	. Resistor, 1.0k, 1%, 1/8w	R15, R16, R42	36	CCM	3
	. Resistor, 200 ohms, 1%, 1/8w	R17	36	CCM	1
	. Resistor, 7.5k, 1%, 1/8w	R18, R19, R33, R34 R20, R23	36	CCM	6
	. Resistor, 3.74k, 1%, 1/8w	R21, R22	36	CCM	2
	. Resistor, 75 ohms, 1%, 1/8w	R25, R26	36	CCM	2

(Continued)

Table 6-16. Index/Sector Amplifier AK64 Replaceable Parts (Cont.)

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-15 (Cont.)	. Resistor, 18.7k, 1%, 1/8w	R27, R28	36	CCM	2
	. Resistor, 2.43 ohms, 1%, 1/8w	R29, R30	36	CCM	2
	. Resistor, 100 ohms, 1%, 1/8w	R31, R32	36	CCM	2
	. Resistor, 30 ohms, 2%, 1/2w	R35, R36	96	E009	2
	. Resistor, 2.4k, 2%, 1/2w	R37, R38	96	E009	2
	. Resistor, 3k, 2%, 1/2w	R39, R40, R44	96	E009	3
	. Resistor, 2.2k, 2%, 1/2w	R43	96	E009	1
	. Resistor, 560 ohms, 2%, 1/2w	R45	96	E009	1
	. Resistor, 8.2k, 2%, 1/2w	R46	96	E009	1
	. Transformer	T1	39	2ZNHA	1
	. Transistor, SDS 230	Q1	5	4JX12E1348	1
	. Transistor, SDS 231	Q2, Q3	5	4JX121347	2
	. Transistor, SDS 216	Q4-Q9	3	S6156	6

Table 6-17. Write Clock Amplifier AK65 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-16	Write Clock Amplifier AK65 (See table 6-12 for NHA)		SDS	131047	
	. Capacitor, mica, 220 pf, 5%, 300v	C1, C15	188	1459	2
	. Capacitor, mylar, 47 nf, 10%, 80v	C2, C3	192	608	2
	. Capacitor, mica, 10 pf, 5%, 300v	C4	188	1459	1
	. Capacitor, mica, 100 pf, 5%, 300v	C5, C6	188	1459	2
	. Capacitor, mica, 200 pf, 5%, 300v	C7, C8	188	1459	2
	. Capacitor, mylar, 10 nf, 10%, 80v	C9-C11, C19-C21	192	608	6
	. Capacitor, mica, 68 pf, 5%, 300v	C12	188	1459	1
	. Capacitor, mica, 120 pf, 5%, 300v	C13, C14	188	1459	2
	. Capacitor, tantalum, 4.7 µf, 20%, 50v	C16, C17	11	ECM	2
	. Capacitor, tantalum, 5.6 µf, 20%, 15v	C18	11	ECM	1
	. Diode, SDS 122	CR1-CR7, CR9-CR11	11	GD70	10
	. Diode, SDS 123	CR8	3	FD6	1
	. Diode, SDS 132	VR1, VR2	1	1N936	2
	. Inductor, molded, 47 µh, 5%	L1, L2, L3	41	1537	3
	. Inductor	L5			1
	. Inductor, molded, 330 µh, 5%	L6	41	1537	1
	. Resistor, 1.5k, 2%, 1/2w	R1, R2	96	E009	2
	. Resistor, 1k, 1%, 1/8w	R3, R7	36	CCM	2
	. Resistor, 10 ohms, 5%, 1/4w	R4, R5, R51	11	GP 1/4	3
	. Resistor, 3.01k, 1%, 1/8w	R6, R9-R12	36	CCM	5
	. Resistor, 20 ohms, 2%, 1/2w	R8	96	E009	1
	. Resistor, 100 ohms, 5%, 1/4w	R13, R43, R49	11	GP 1/4	3
	. Resistor, 3.57k, 1%, 1/8w	R14, R15, R21, R22	36	CCM	4
	. Resistor, 5.11k, 1%, 1/8w	R16, R19	36	CCM	2
	. Resistor, 2k, 1%, 1/8w	R17, R18	36	CCM	2

(Continued)

Table 6-17. Write Clock Amplifier AK65 Replaceable Parts (Cont.)

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-16 (Cont.)	. Resistor, 75 ohms, 5%, 1/4w	R20	11	GP 1/4	1
	. Resistor, 511 ohms, 1%, 1/8w	R23, R24	36	CCM	2
	. Resistor, 51 ohms, 5%, 1/4w	R25	11	GP 1/4	1
	. Resistor, 2.61k, 1%, 1/8w	R26, R27, R60, R61	36	CCM	4
	. Resistor, 10k, 2%, 1/2w	R28, R29, R41	96	E009	3
	. Resistor, 51k, 2%, 1/2w	R30	96	E009	1
	. Resistor, 15k, 2%, 1/2w	R31	96	E009	1
	. Resistor, 200 ohms, 5%, 1/4w	R32	11	GP 1/4	1
	. Resistor, 1k, 5%, 1/4w	R33	11	GP 1/4	1
	. Resistor, 47 ohms, 5%, 1/4w	R34, R37, R45, R50, R52	11	GP 1/4	5
	. Resistor, 5.1k, 2%, 1/2w	R35, R36, R42	96	E009	3
	. Resistor, 6.8k, 2%, 1/2w	R38	96	E009	1
	. Resistor, 150 ohms, 2%, 1/2w	R39, R62	96	E009	2
	. Resistor, 100 ohms, 2%, 1/2w	R40	96	E009	1
	. Resistor, 390 ohms, 2%, 1/2w	R44, R54	96	E009	2
	. Resistor, 2.4k, 2%, 1/2w	R46, R55	96	E009	2
	. Resistor, 820 ohms, 2%, 1w	R47	16	C-32	1
	. Resistor, 510 ohms, 5%, 1/4w	R48	11	GP 1/4	1
	. Resistor, 8.2k, 2%, 1/2w	R53	96	E009	1
	. Resistor, 5.6k, 5%, 1/4w	R56	11	GP 1/4	1
	. Resistor, 2k, 5%, 1/4w	R57, R58, R59	11	GP 1/4	3
	. Transformer	T1	39	2ZNHA	1
	. Transistor, SDS 230	Q1	5	4JX12E1347	1
	. Transistor, SDS 231	Q2, Q6	5	4JX12E1348	2
	. Transistor, SDS 222	Q3, Q4	3	S15099	2
	. Transistor, SDS 216	Q7, Q9, Q13, Q14	3	S6156	4
	. Transistor, SDS 219	Q10, Q11, Q8, Q12	3	S7411	4

Table 6-18. Read Amplifier HK73 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-17	Read Amplifier HK73 (See table 6-12 for NHA)		SDS	131035	
	. Capacitor, mylar, 200 nf, 10%, 80v	C2	192	608	1
	. Capacitor, tantalum, 5.6 μf, 20%, 15v	C3, C4	11	ECM	2
	. Capacitor, mylar, 47 nf, 10%, 80v	C5, C7	192	608	2
	. Capacitor, mica, 4.7 pf, 5%, 300v	C8, C11	188	1459	2
	. Capacitor, mica, 100 pf, 5%, 300v	C9, C10	188	1459	2
	. Diode, SDS 134	CR1-CR40	11	TID44	40
	. Inductor, molded, 47 μh, 5%	L1-L3	41	1537	3
	. Resistor, 10 ohms, 2%, 1w	R1	16	C-32	1
	. Resistor, 62 ohms, 2%, 1w	R2	16	C-32	1
	. Resistor, 210 ohms, 5%, 1/4w	R3, R4, R5	11	GP 1/4	3
	. Resistor, 1.47k, 1%, 1/8w	R7, R10, R13, R27, R28	36	CCM	5
	. Resistor, 2.43k, 1%, 1/8w	R8, R22, R23, R31, R32	36	CCM	5
	. Resistor, 681 ohms, 1%, 1/8w	R9	36	CCM	1
	. Resistor, 3.01k, 1%, 1w	R11, R12, R41, R42	36	CES	4
	. Resistor, 75 ohms, 1%, 1/8w	R14, R15, R20, R21	36	CCM	4
	. Resistor, 1.5k, 1%, 1/8w	R16, R19	36	CCM	2
	. Resistor, 1.5k, 1%, 1w	R17, R18	36	CES	2
	. Resistor, 10 ohms, 5%, 1/4w	R24, R25	11	GP 1/4	2
	. Resistor, 3.01k, 1%, 1/8w	R26, R29	36	CCM	2
	. Resistor, 300 ohms, 2%, 1/2w	R30	96	E009	1
	. Resistor, 750 ohms, 1%, 1/8w	R33, R34	36	CCM	2
	. Resistor, 121 ohms, 1%, 1/8w	R35, R37	36	CCM	2
	. Resistor, 3.57k, 1%, 1/8w	R36, R38	36	CCM	2
	. Resistor, 30 ohms, 2%, 1/2w	R39, R40	96	E009	2
	. Resistor, 75 ohms, 2%, 1/2w	R43, R44	96	E009	2
	. Resistor, 2k, 5%, 1/4w	R45, R46, R47	11	GP 1/4	3
	. Transistor, SDS 230	Q1	5	4JX12E1347	1
	. Transistor, SDS 231	Q2, Q3	5	4JX12E1348	2
	. Transistor, SDS 216	Q4-Q8	3	S6156	5

Table 6-19. Limiter HK74 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-18	Limiter HK74 (See table 6-12 for NHA)		SDS	131037	
	. Capacitor, mylar, 10 nf, 10%, 80v	C1	192	608	1
	. Capacitor, tantalum, 4.7 µf, 20%, 50v	C3	192	GA901	1
	. Capacitor, mylar, 47 nf, 10%, 80v	C4	192	608	1
	. Capacitor, tantalum, 1.5µf, 20%, 6v	C5	11	ECM	1
	. Diode, SDS 134	CR1-CR7	11	TID44	7
	. Resistor, 680 ohms, 5%, 1/4w	R1	11	GP 1/4	1
	. Resistor, 3.01k, 1%, 1w	R2	36	CES	1
	. Resistor, 1k, 1%, 1/8w	R3, R12, R13	36	CCM	3
	. Resistor, 1.21k, 1%, 1w	R4-R7	36	CES	4
	. Resistor, 300 ohms, 2%, 1/2w	R8	96	E009	1
	. Resistor, 2.43k, 1%, 1/8w	R9, R10	36	CCM	2
	. Resistor, 2.0k, 1%, 1w	R11, R14	36	CES	2
	. Resistor, 200 ohms, 2%, 1/2w	R15, R28, R29, R38, R40	96	E009	5
	. Resistor, 4.64k, 1%, 1/8w	R16, R17, R33, R34	36	CCM	4
	. Resistor, 10 ohms, 5%, 1/4w	R18, R19, R30, R31	11	GP 1/4	4
	. Resistor, 1.82k, 1%, 1w	R20, R23	36	CES	2
	. Resistor, 357 ohms, 1%, 1/8w	R21, R22	36	CCM	2
	. Resistor, 68.1 ohms, 1%, 1/8w	R24, R25	36	CCM	2
	. Resistor, 4.32k, 1%, 1/8w	R26, R27	36	CCM	2
	. Resistor, 20 ohms, 2%, 1/2w	R32, R37, R39	96	E009	3
	. Resistor, 1.8k, 2%, 1/2w	R35, R36	16	C-32	2
	. Resistor, 10 ohms, 2%, 1/2w	R41	96	E009	1
	. Transformer	T1	39	1ZMHA	1
	. Transistor, SDS 230	Q1	5	4JX12E1347	1
	. Transistor, SDS 231	Q2	5	4JX12E1348	1
	. Transistor, SDS 216	Q3-Q8	3	S6156	6

Table 6-20. Clock Discriminator HK75 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-19	Clock Discriminator HK75 (See table 6-12 for NHA)		SDS	131039	
	. Capacitor, tantalum, 5.6 µf, 20%, 15v	C1, C2	11	ECM	2
	. Capacitor, mica, 100 pf, 5%, 300v	C3, C4, C6, C12, C13	188	1459	5
	. Capacitor, mica, 220 pf, 5%, 300v	C5	188	1459	1
	. Capacitor, mylar, 10 nf, 10%, 80v	C7, C8, C10	192	608	3
	. Capacitor, tantalum, 1.5 µf, 20%, 6v	C9	11	ECM	1
	. Capacitor, mica, 47 pf, 5%, 300v	C11, C14	188	1459	2
	. Diode, SDS 122	CR1-CR7	11	GD70	7
	. Diode, SDS 101	VR1	11	1N746	1
	. Inductor, molded, 47 µh, 5%	L1-L3	41	1537	3
	. Potentiometer, 50k, 10%, 1w	R26	35	275P-584	1
	. Potentiometer, 5k, 10%, 1w	R28	35	275P-584	1
	. Resistor, 2 ohms, 5%, 1w	R1, R2	36	BWH	2
	. Resistor, 300 ohms, 2%, 1/2w	R3, R4	96	E009	2
	. Resistor, 330 ohms, 2%, 1/2w	R5, R6	96	E009	2
	. Resistor, 243 ohms, 1%, 1/8w	R7	36	CCM	1
	. Resistor, 68 ohms, 2%, 1/2w	R8, R9	96	E009	2
	. Resistor, 649 ohms, 1%, 1/8w	R10	36	CCM	1
	. Resistor, 430 ohms, 2%, 1/2w	R11	96	E009	1
	. Resistor, 1k, 1%, 1/8w	R12, R17, R33	36	CCM	3
	. Resistor, 6.2k, 2%, 1/2w	R13	96	E009	1
	. Resistor, 332 ohms, 1%, 1/8w	R14	36	CCM	1
	. Resistor, 619 ohms, 1%, 1/8w	R15	36	CCM	1
	. Resistor, 357 ohms, 1%, 1/8w	R16	36	CCM	1
	. Resistor, 33 ohms, 2%, 1/2w	R18, R20, R21	96	E009	3
	. Resistor, 12k, 2%, 1/2w	R19	96	E009	1
	. Resistor, 2.2k, 2%, 1/2w	R22	96	E009	1
	. Resistor, 10k, 2%, 1/2w	R23	96	E009	1
	. Resistor, 820 ohms, 2%, 1/2w	R24	96	E009	1
	. Resistor, 2.7k, 5%, 1/4w	R25	11	GP 1/4	1
	. Resistor, 2k, 5%, 1/4w	R27, R36, R37	11	GP 1/4	3
	. Resistor, 681 ohms, 1%, 1/8w	R29, R31	36	CCM	2
	. Resistor, 100 ohms, 1%, 1/8w	R30	36	CCM	1

(Continued)

Table 6-20. Clock Discriminator HK75 Replaceable Parts (Cont.)

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-19 (Cont.)	. Resistor, 3.01k, 1%, 1/8w	R32	CCM	36	1
	. Resistor, 560 ohms, 2%, 1/2w	R34	E009	96	1
	. Transistor, SDS 219	Q1-Q8, Q11, Q12	S7411	3	10
	. Transistor, SDS 216	Q9, Q10, Q13, Q14	S6156	3	4

Table 6-21. Data Decoder HK76 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-20	Data Decoder HK76 (See table 6-12 for NHA)		SDS	131041	
	. Capacitor, mylar, 100 nf, 10%, 80v	C1	192	608	1
	. Capacitor, tantalum, 5.6 µf, 20%, 15v	C2, C4	11	ECM	2
	. Capacitor, tantalum, 6.8 µf, 20%, 6v	C3	11	ECM	1
	. Capacitor, mylar, 10 nf, 10%, 80v	C5	192	608	1
	. Capacitor, mica, 100 pf, 5%, 300v	C7	188	1459	1
	. Diode, SDS 122	CR1-CR19	11	GD70	19
	. Integrated circuit, SDS 307	A1, A2	3	U5S114959X	2
	. Resistor, 2 ohms, 5%, 1w	R1, R2, R3	36	BWH	3
	. Resistor, 3.32k, 1%, 1/8w	R4, R5, R28	36	CCM	3
	. Resistor, 432 ohms, 1%, 1/8w	R6	36	CCM	1
	. Resistor, 2.2k, 2%, 1/2w	R7, R8, R11, R12, R13	96	E009	5
	. Resistor, 560 ohms, 2%, 1/2w	R9, R10, R25, R26, R27, R32	96	E009	6
	. Resistor, 330 ohms, 2%, 1/2w	R14, R15	96	E009	2
	. Resistor, 1k, 2%, 1/2w	R16, R17, R24, R37, R38	96	E009	5
	. Resistor, 18k, 2%, 1/2w	R18, R21	96	E009	2
	. Resistor, 680 ohms, 2%, 1/2w	R19, R20, R36	96	E009	3
	. Resistor, 2.7k, 2%, 1/2w	R22, R23	96	E009	2
	. Resistor, 1k, 1%, 1/8w	R29	36	CCM	1
	. Resistor, 619 ohms, 1%, 1/8w	R30	36	CCM	1
	. Resistor, 332 ohms, 1%, 1/8w	R31	36	CCM	1
	. Resistor, 20 ohms, 2%, 1/2w	R33	96	E009	1
	. Resistor, 2.61k, 1%, 1/8w	R34	36	CCM	1
	. Transistor, SDS 216	Q1-Q4, Q7, Q8, Q11, Q12	3	S6156	8
	. Transistor, SDS 219	Q5, Q6, Q9, Q10	3	S7411	4

Table 6-22. Index/Sector Decoder HK77 Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-21	Index/Sector Decoder HK77 (See table 6-12 for NHA)		SDS	131045	
	. Capacitor, tantalum, 5.6 µf, 20%, 15v	C1	11	ECM	1
	. Capacitor, tantalum, 6.8 µf, 20%, 6v	C2	11	ECM	1
	. Capacitor, mylar, 10 nf, 10%, 80v	C3, C7	11	608	2
	. Capacitor, mica, 2.2 pf, 5%, 300v	C4	188	1459	1
	. Capacitor, mylar, 1 nf, 10%, 80v	C5	192	608	1
	. Capacitor, mica, 470 pf, 5%, 300v	C6	188	1459	1
	. Capacitor, tantalum, 4.7 µf, 20%, 50v	C8, C9	11	ECM	2
	. Diode, SDS 122	CR1-CR26	11	GD170	26
	. Diode, SDS 101	VR1-VR4	11	1N746	4
	. Integrated circuit, SDS 307	A1, A2	3	U5S114959X	2
	. Resistor, 2 ohms, 5%, 1w	R1, R2	36	BWH	2
	. Resistor, 750 ohms, 2%, 1/2w	R3, R27	96	E009	2
	. Resistor, 2.2k, 2%, 1/2w	R4, R22-R25, R29-R32	96	E009	9
	. Resistor, 1.65k, 1%, 1/8w	R5	36	CCM	1
	. Resistor, 1.5k, 2%, 1/2w	R6, R14	96	E009	2
	. Resistor, 3.9k, 2%, 1/2w	R7, R15, R37, R38	96	E009	4
	. Resistor, 51 ohms, 2%, 1/2w	R8, R13, R20	96	E009	3
	. Resistor, 1.8k, 2%, 1/2w	R9, R17, R40, R43	96	E009	4
	. Resistor, 680 ohms, 2%, 1/2w	R10, R21, R18, R41, R44	96	E009	5
	. Resistor, 3.57k, 1%, 1/8w	R12	36	CCM	1
	. Resistor, 10k, 2%, 1/2w	R16, R39, R32, R46	96	E009	4
	. Resistor, 330 ohms, 2%, 1/2w	R26, R33, R34	96	E009	3
	. Resistor, 1k, 2%, 1/2w	R28, R35, R36	96	E009	3
	. Resistor, 820 ohms, 2%, 1/2w	R45	96	E009	1
	. Transistor, SDS 216	Q1-Q12	3	S6156	12
	. Resistor, 2.7k, 2%, 1/2w	R19	96	E009	1

Table 6-23. Read/Write Coupler NK59

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
6-22	Read/Write Coupler NK59		SDS		
	. Diode, SDS 134	CR1-CR8	11	TID44	32
	. Resistor, 10 ohms, 5%, 1/4w	R2, R4	11	GP 1/4	8
	. Resistor, 560 ohms, 5%, 1/4w	R3, R5	11	GP 1/4	8
	. Transformer	T1	39	1ZMHA	4

Table 6-24. Manufacturer Supply Codes

Code No.	Name	Address
1	Motorola Semiconductor Products, Inc.	P. O. Box 2953, Phoenix, Ariz. 85002
3	Fairchild Semiconductor	313 Fairchild Dr., Mountain View, Calif. 94041
11	Texas Instruments, Inc.	P. O. Box 6015, Dallas, Tex. 75222
13	TRW Semiconductors, Inc.	14520 Aviation Blvd., Lawndale, Calif.
16	Corning Glass Works	550 High St., Bradford, Pa.
35	Bourns, Inc.	1200 Columbia Ave., Riverside, Calif.
41	Delevan Electronics Corp.	270 Quaker Rd., E. Aurora, N. Y. 14052
48	Littelfuse, Inc.	800 E. Northwest Hwy., Des Plains, Ill.
51	Cinch Manufacturing Co.	1026 S. Homan Ave., Chicago, Ill. 60624
79	Allied Control Co.	2 E. End Ave., New York, N. Y. 10021
96	Amperex Electronics Corp.	230 Duffy Ave., Hicksville, N. Y. 11802
103	The Wiremold Co.	Hartford, Conn.
104	Dialight Corp.	60 Stewart Ave., Brooklyn, N. Y. 11237
105	Heinemann Electric Co.	2636 Brunswick Pike, Trenton, N. J. 08602
106	Arrow-Hart & Hegeman Electric Co.	103 Hawthorne St., Hartford, Conn.
110	Winchester Electronics Corp.	Main & Hillside Aves., Oakville, Conn. 06779
130	C. P. Clare & Co.	3101 Pratt Blvd., Chicago, Ill.
151	Stancor Electronics, Inc.	3501 W. Addison, Chicago, Ill.
188	Aerovox Corp., New Bedford Div.	740 Belleville Ave., New Bedford, Mass. 02741
191	Dearborn Electronics, Inc.	P. O. Box 350, Orlando, Fla.
219	Kulka Electric Corp.	633 S. Fulton Ave., Mt. Vernon, N. Y. 10551
227	Burndy Corp.	Norwalk, Conn. 06854
341	ITT Industrial Products Div.	15151 Bledsoe, San Fernando, Calif.
364	Hubbell	Bridgeport, Conn. 06602
SDS	Scientific Data Systems, Inc.	1649 Seventeenth St., Santa Monica, Calif. 90404

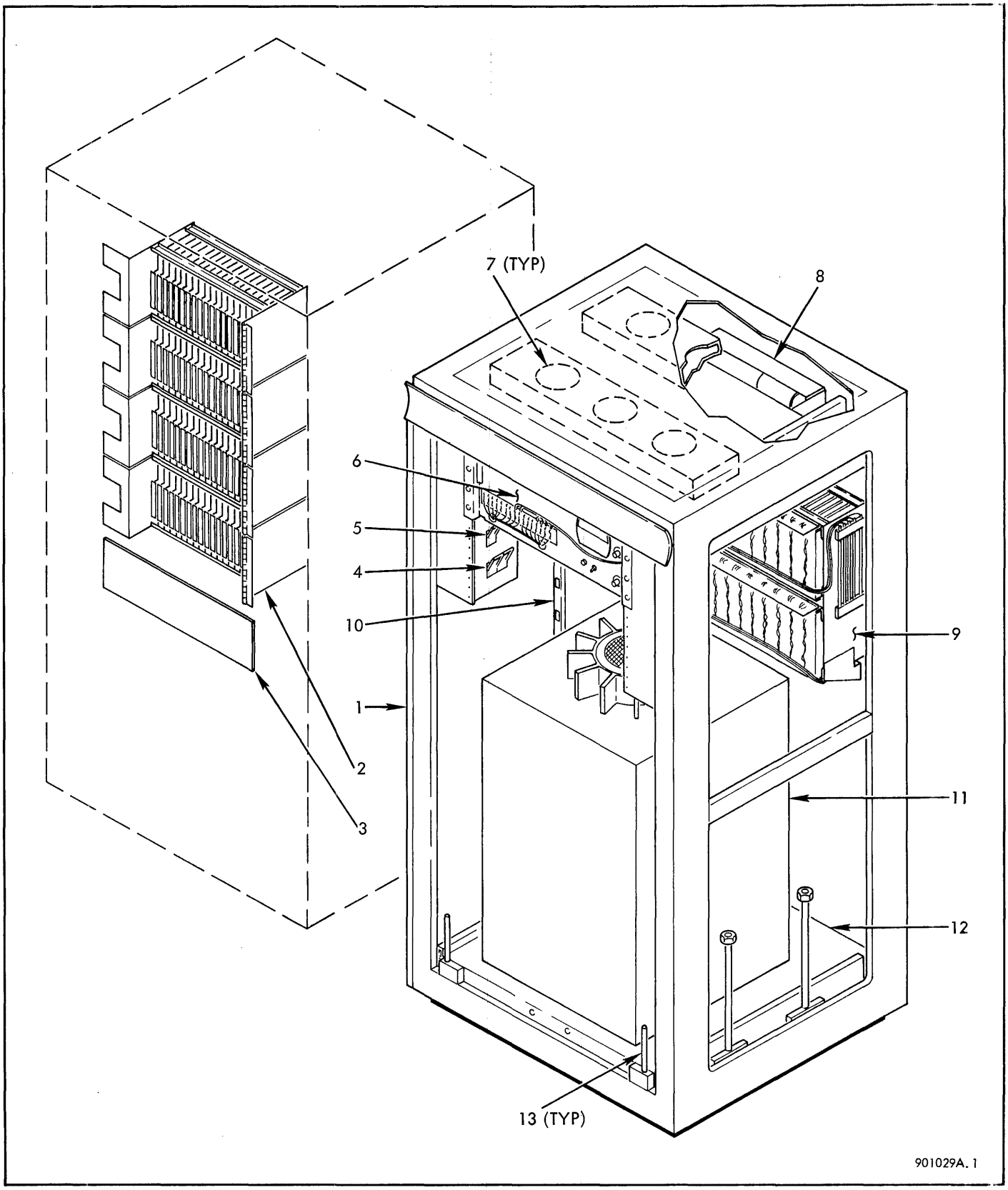
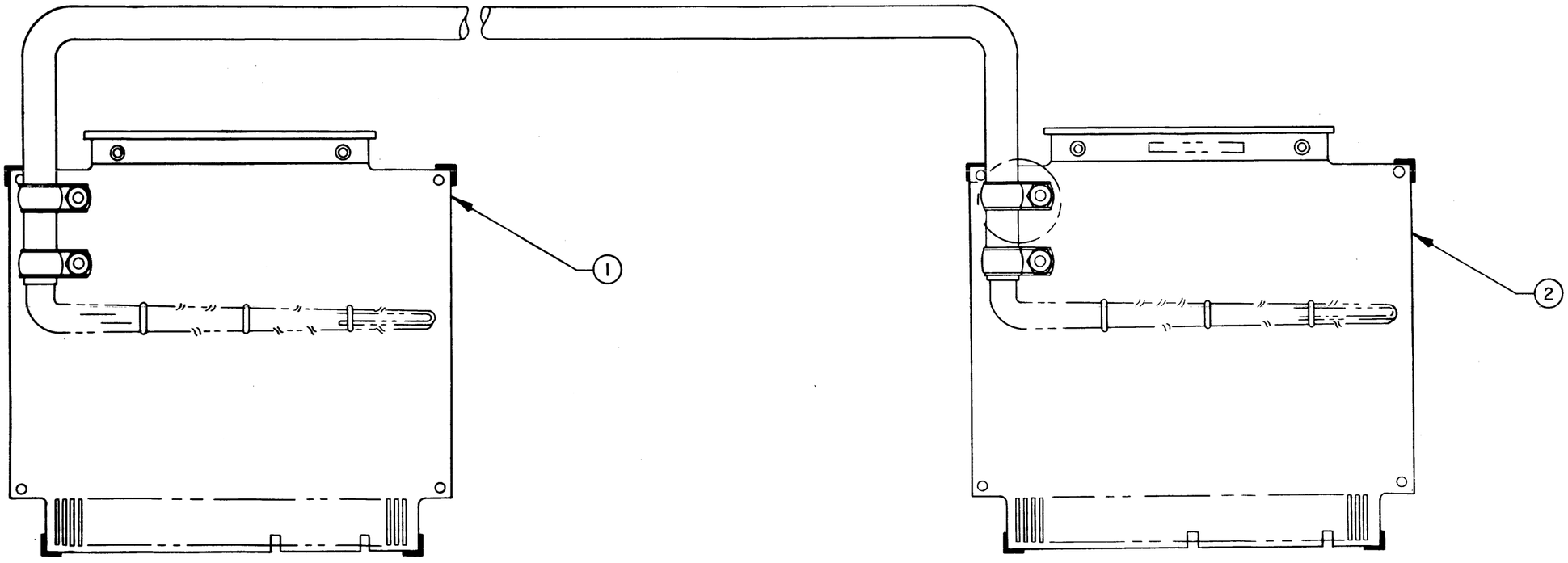


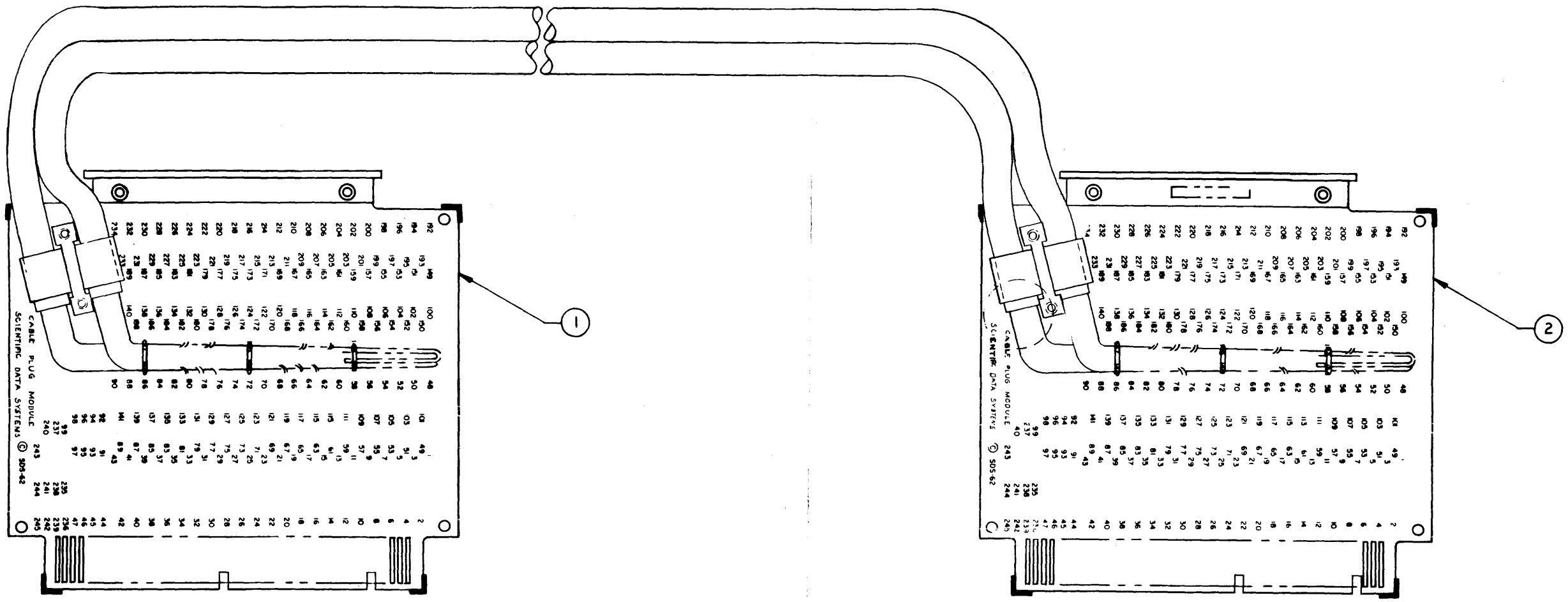
Figure 6-1. RAD File Model 9367B/C Parts Location



NOTE: REFERENCE SDS DWG: 113899-1D

Figure 6-2. Plug Module Cable Assembly P155/P156 Parts Location

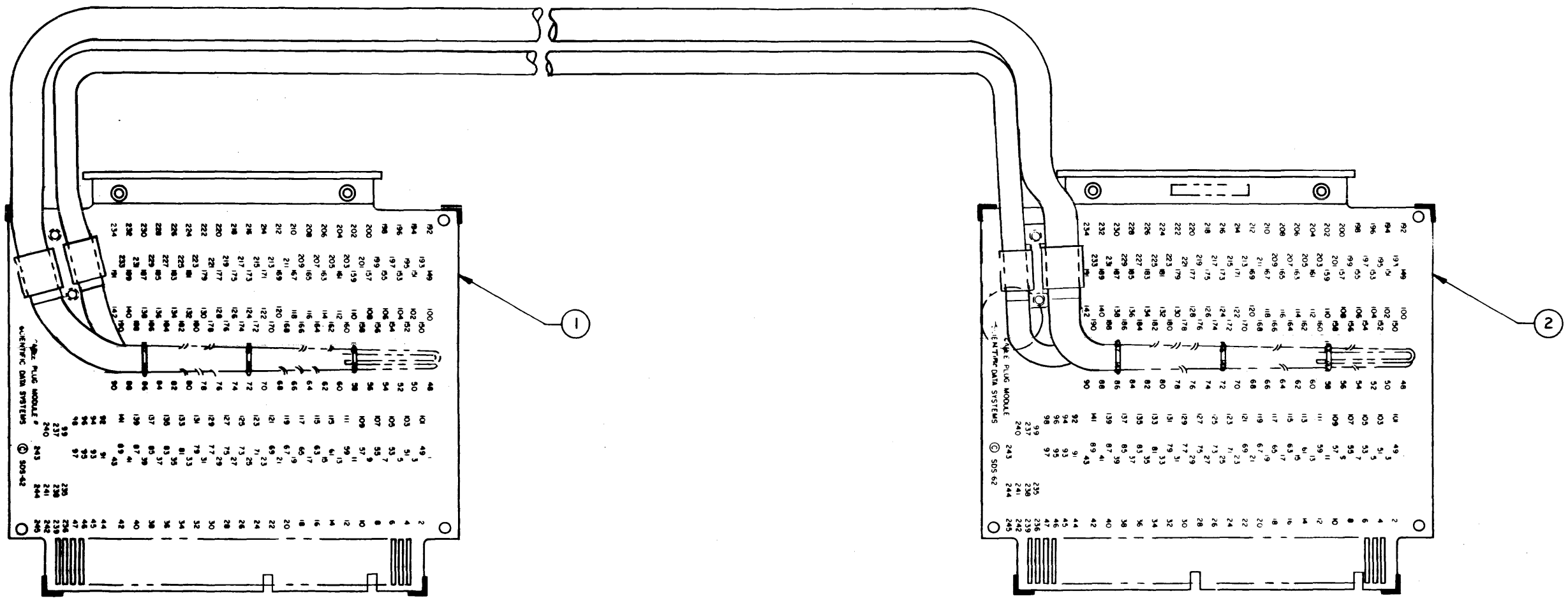
900613A.617



NOTE: REFERENCE SDS DWG: 113902-1G

Figure 6-3. Plug Module Cable Assembly P157/P158 Parts Location

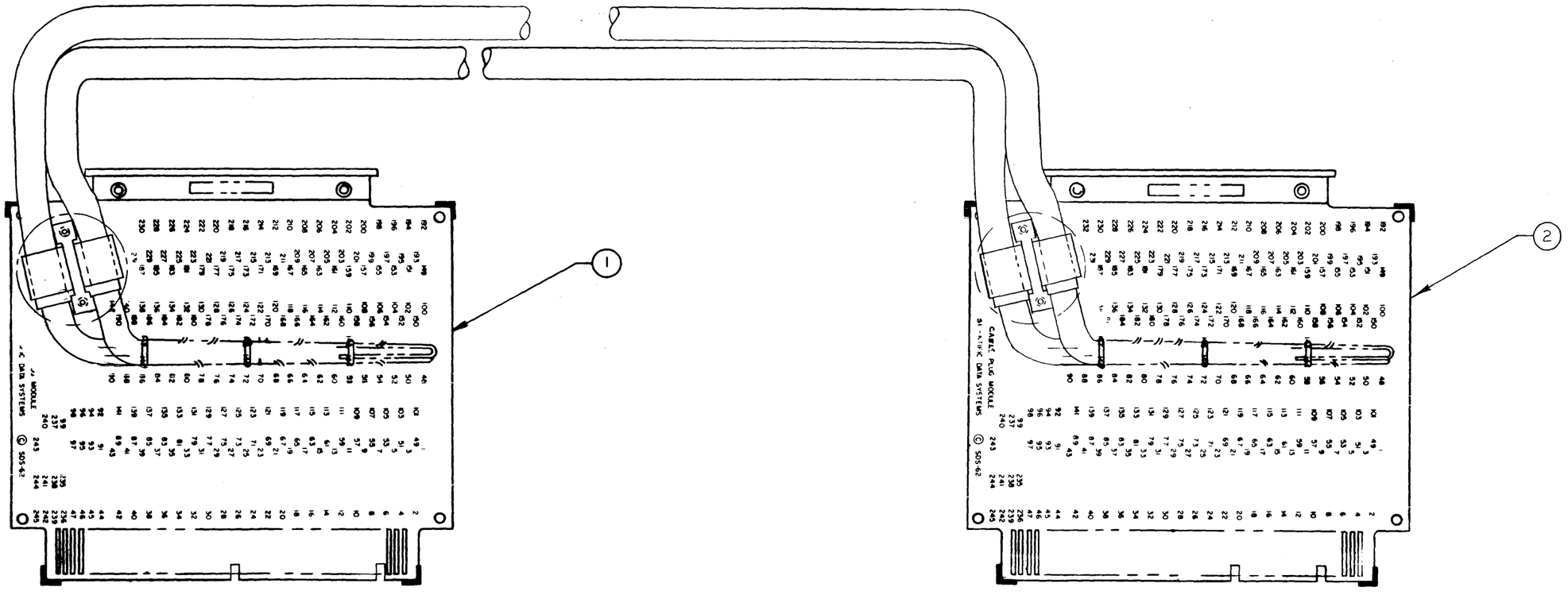
900613A.620



NOTE: REFERENCE SDS DWG: 113896-1B

Figure 6-4. Plug Module Cable Assembly P159/P160 Parts Location

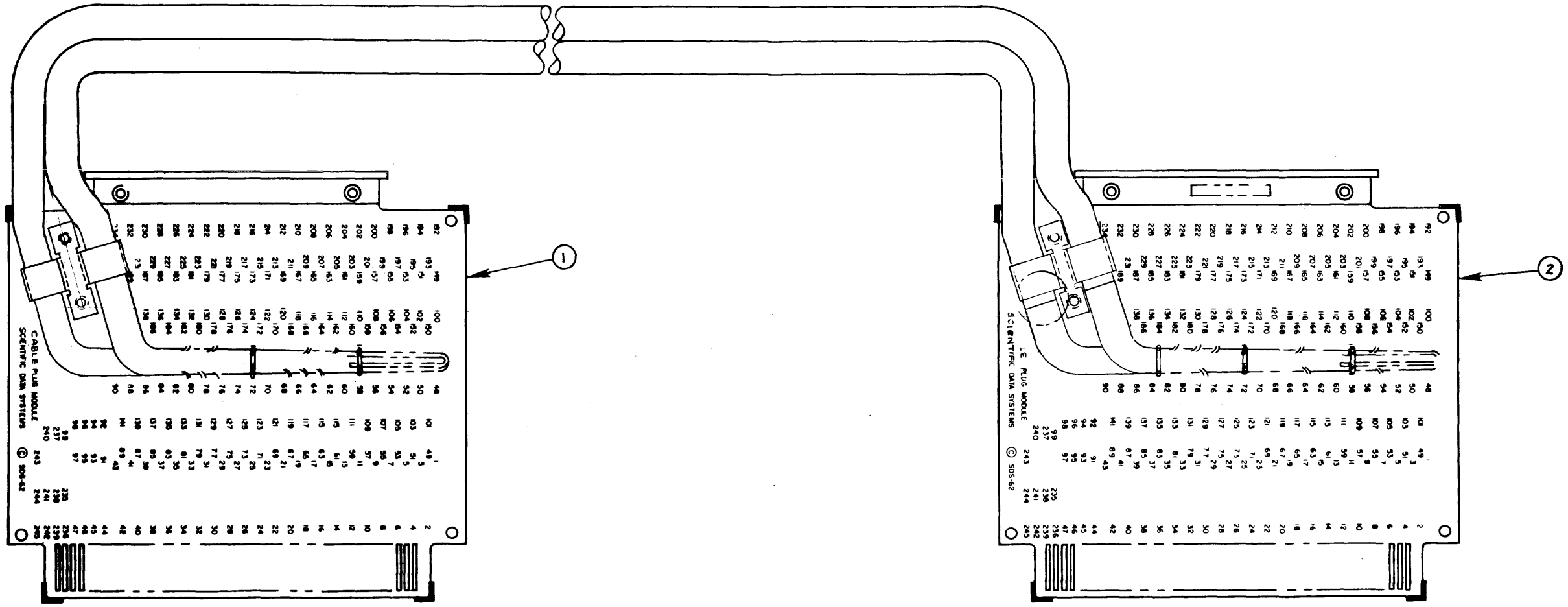
900613A.618



NOTE: REFERENCE SDS DWG: 116388-1E

Figure 6-5. Plug Module Cable Assembly P161/P162 Parts Location

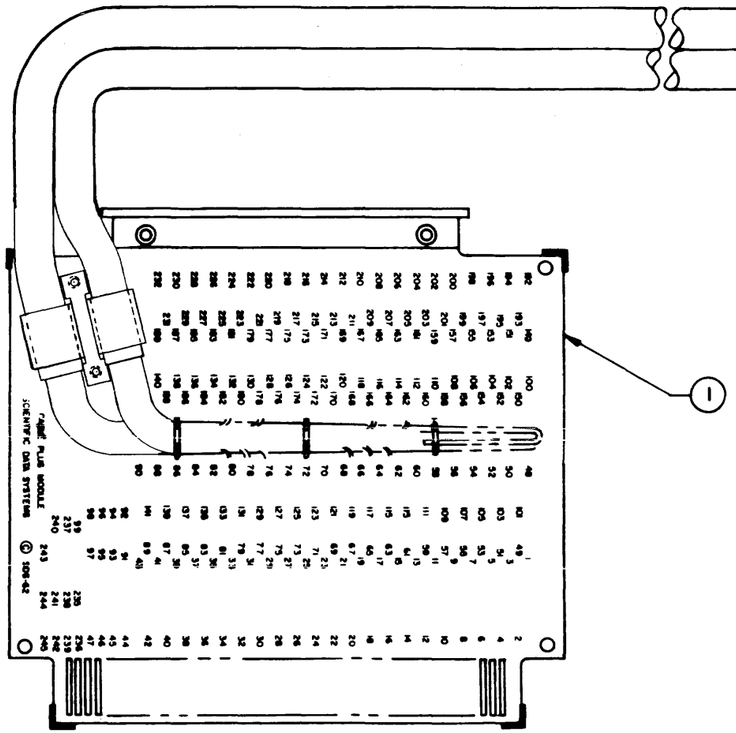
900613A.619



NOTE: REFERENCE SDS DWG: 116509-1E

Figure 6-6. Plug Module Cable Assembly P168/P169 Parts Location

900613A.616



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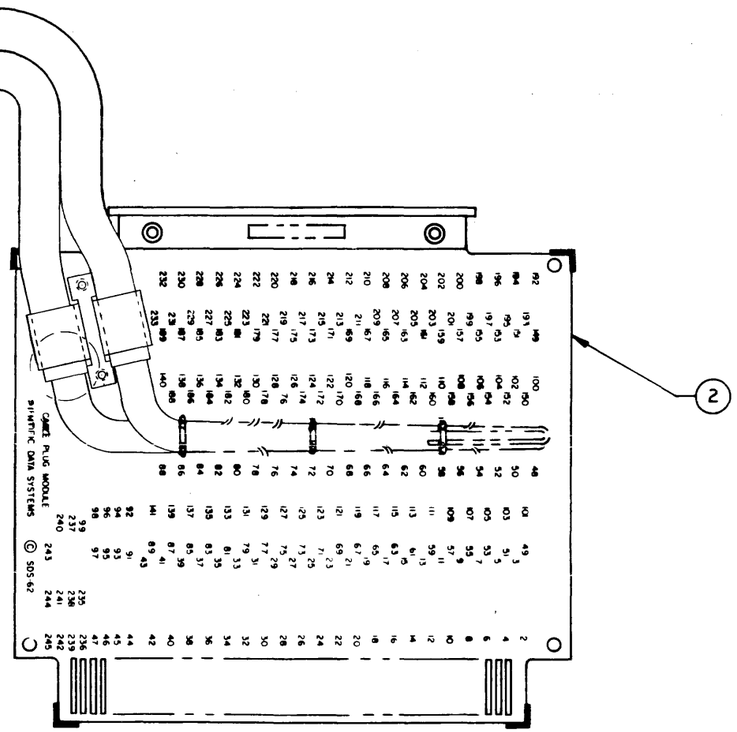


2

NOTE: REFERENCE SDS DWG: 116513-1D

Figure 6-7. Plug Module Cable Assembly P170/P171 Parts Location

900613A.621

PARTS LOCATION

MODULE P155

DIODES

CR27	(3 → 50)	CR13	(31 → 78)
CR26	(15 → 62)	CR12	(32 → 79)
CR25	(16 → 63)	CR11	(33 → 80)
CR24	(20 → 67)	CR10	(34 → 81)
CR23	(21 → 68)	CR9	(35 → 82)
CR22	(22 → 69)	CR8	(36 → 83)
CR21	(23 → 70)	CR7	(37 → 84)
CR20	(24 → 71)	CR6	(38 → 85)
CR19	(25 → 72)	CR5	(39 → 86)
CR18	(26 → 73)	CR4	(40 → 87)
CR17	(27 → 74)	CR3	(41 → 88)
CR16	(28 → 75)	CR2	(42 → 89)
CR15	(29 → 76)	CR1	(43 → 90)
CR14	(30 → 71)		

INDUCTORS

L3	(1 - 48)	L1	(13 - 60)
L2	(8 - 55)		

RESISTORS

R3	(1 - 48)	R18	(233 - 190)
R2	(8 - 55)	R17	(194 - 151)
R1	(13 - 60)	R16	(206 - 163)
R30	(207 - 164)	R15	(212 - 169)
R29	(211 - 168)	R14	(214 - 171)
R28	(213 - 170)	R13	(216 - 173)
R27	(215 - 172)	R12	(218 - 175)
R26	(217 - 174)	R11	(220 - 177)
R25	(219 - 176)	R10	(222 - 179)
R24	(221 - 178)	R9	(224 - 181)
R23	(223 - 180)	R8	(226 - 183)
R22	(225 - 182)	R7	(228 - 185)
R21	(227 - 184)	R6	(230 - 187)
R20	(229 - 186)	R5	(232 - 189)
R19	(231 - 188)	R4	(234 - 191)

PARTS LOCATION

MODULE P160

DIODES

CR2	(192 → 149)
CR1	(199 → 156)

PARTS LOCATION

MODULE P157

DIODES

CR10	(1 → 48)	CR4	(7 → 54)
CR9	(2 → 49)	CR3	(8 → 55)
CR8	(3 → 50)	CR2	(9 → 56)
CR7	(4 → 51)	CR1	(10 → 57)
CR6	(5 → 52)	CR12	(12 → 59)
CR5	(6 → 53)	CR11	(13 → 60)

INDUCTORS

L32	(11 - 58)	L15	(29 - 76)
L30	(14 - 61)	L14	(30 - 77)
L28	(16 - 63)	L13	(31 - 78)
L27	(17 - 64)	L12	(32 - 79)
L26	(18 - 65)	L11	(33 - 80)
L25	(19 - 66)	L10	(34 - 81)
L24	(20 - 67)	L9	(35 - 82)
L23	(21 - 68)	L8	(36 - 83)
L22	(22 - 69)	L7	(37 - 84)
L21	(23 - 70)	L6	(38 - 85)
L20	(24 - 71)	L5	(39 - 86)
L19	(25 - 72)	L4	(40 - 87)
L18	(26 - 73)	L3	(41 - 88)
L17	(27 - 74)	L2	(42 - 89)
L16	(28 - 75)	L1	(43 - 90)

RESISTORS

R38	(192 - 149)	R20	(24 - 71)
R43	(193 - 150)	R19	(25 - 72)
R37	(194 - 151)	R18	(26 - 73)
R42	(195 - 152)	R17	(27 - 74)
R36	(196 - 153)	R16	(28 - 75)
R41	(197 - 154)	R15	(29 - 76)
R35	(198 - 155)	R14	(30 - 77)
R40	(199 - 156)	R13	(31 - 78)
R34	(200 - 157)	R12	(32 - 79)
R39	(201 - 158)	R11	(33 - 80)
R33	(204 - 161)	R10	(34 - 81)
R32	(11 - 58)	R9	(35 - 82)
R29	(14 - 61)	R8	(36 - 83)
R28	(16 - 63)	R7	(37 - 84)
R27	(17 - 64)	R6	(38 - 85)
R26	(18 - 65)	R5	(39 - 86)
R25	(19 - 66)	R4	(40 - 87)
R24	(20 - 67)	R3	(41 - 88)
R23	(21 - 68)	R2	(42 - 89)
R22	(22 - 69)	R1	(43 - 90)
R21	(23 - 70)		

PARTS LOCATION

MODULE P159

DIODES

CR3	(14 → 61)	CR4	(199 → 156)
CR2	(15 → 62)	CR5	(192 → 149)
CR1	(16 → 63)		

INDUCTORS

L40	(1 - 48)	L20	(24 - 71)
L39	(2 - 49)	L19	(25 - 72)
L38	(3 - 50)	L18	(26 - 73)
L37	(4 - 51)	L17	(27 - 74)
L36	(5 - 52)	L16	(28 - 75)
L35	(6 - 53)	L15	(29 - 76)
L34	(7 - 54)	L14	(30 - 77)
L33	(8 - 55)	L13	(31 - 78)
L32	(9 - 56)	L12	(32 - 79)
L31	(10 - 57)	L11	(33 - 80)
L30	(11 - 58)	L10	(34 - 81)
L29	(12 - 59)	L9	(35 - 82)
L28	(13 - 60)	L8	(36 - 83)
L27	(17 - 64)	L7	(37 - 84)
L26	(18 - 65)	L6	(38 - 85)
L25	(19 - 66)	L5	(39 - 86)
L24	(20 - 67)	L4	(40 - 87)
L23	(21 - 68)	L3	(41 - 88)
L22	(22 - 69)	L2	(42 - 89)
L21	(23 - 70)	L1	(43 - 90)

RESISTORS

R43	(162 - 205)	R21	(23 - 70)
R42	(163 - 206)	R20	(24 - 71)
R41	(164 - 207)	R19	(25 - 72)
R40	(1 - 48)	R18	(26 - 73)
R39	(2 - 49)	R17	(27 - 74)
R38	(3 - 50)	R16	(28 - 75)
R37	(4 - 51)	R15	(29 - 76)
R36	(5 - 52)	R14	(30 - 77)
R35	(6 - 53)	R13	(31 - 78)
R34	(7 - 54)	R12	(32 - 79)
R33	(8 - 55)	R11	(33 - 80)
R32	(9 - 56)	R10	(34 - 81)
R31	(10 - 57)	R9	(35 - 82)
R30	(11 - 58)	R8	(36 - 83)
R29	(12 - 59)	R7	(37 - 84)
R28	(13 - 60)	R6	(38 - 85)
R27	(17 - 64)	R5	(39 - 86)
R26	(18 - 65)	R4	(40 - 87)
R25	(19 - 66)	R3	(41 - 88)
R24	(20 - 67)	R2	(42 - 89)
R23	(21 - 68)	R1	(43 - 90)
R22	(22 - 69)		

PARTS LOCATION

MODULE P161

DIODES

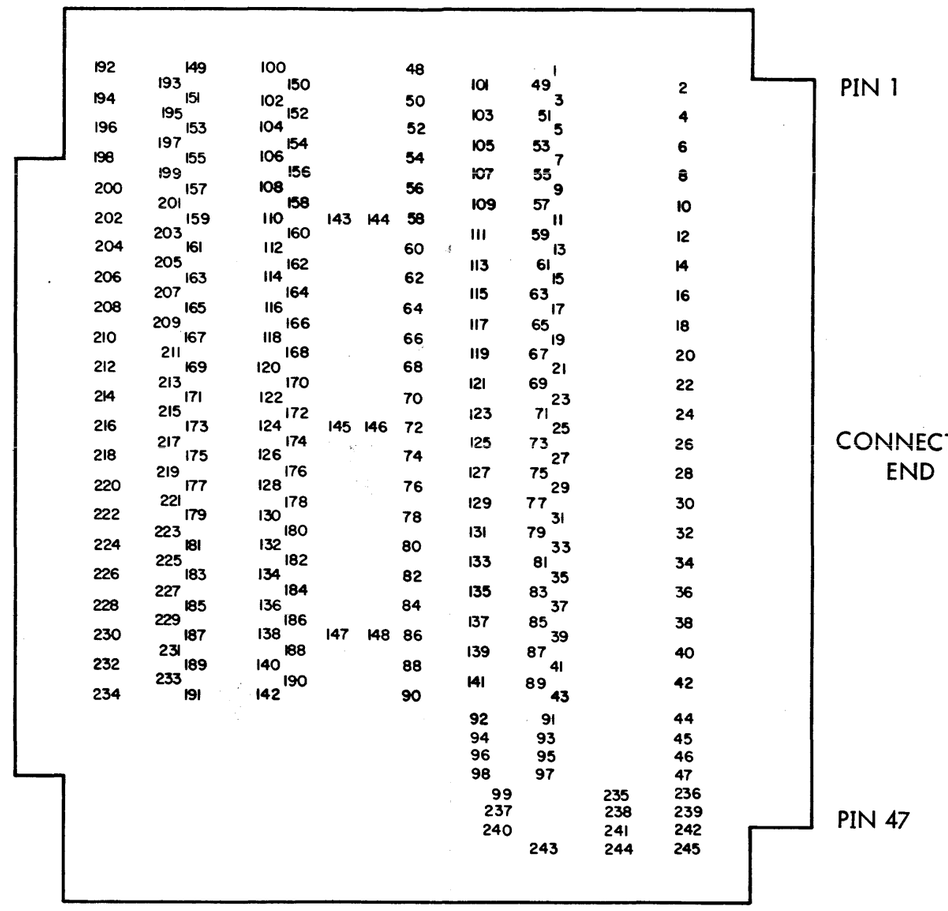
CR20	(23 → 70)	CR10	(33 → 80)
CR19	(24 → 71)	CR9	(34 → 81)
CR18	(25 → 72)	CR8	(35 → 82)
CR17	(26 → 73)	CR7	(36 → 83)
CR16	(27 → 74)	CR6	(37 → 84)
CR15	(28 → 75)	CR5	(38 → 85)
CR14	(29 → 76)	CR4	(39 → 86)
CR13	(30 → 77)	CR3	(40 → 87)
CR12	(31 → 78)	CR2	(41 → 88)
CR11	(32 → 79)	CR1	(42 → 89)

INDUCTORS

L19	(1 - 48)	L9	(11 - 58)
L18	(2 - 49)	L8	(12 - 59)
L17	(3 - 50)	L7	(13 - 60)
L16	(4 - 51)	L6	(14 - 61)
L15	(5 - 52)	L5	(15 - 62)
L14	(6 - 53)	L4	(16 - 63)
L13	(7 - 54)	L3	(17 - 64)
L12	(8 - 55)	L2	(18 - 65)
L11	(9 - 56)	L1	(19 - 66)
L10	(10 - 57)	L20	(20 - 67)

RESISTORS

R29	(171 - 214)	R24	(181 - 224)
R39	(172 - 215)	R34	(182 - 225)
R28	(173 - 216)	R23	(183 - 226)
R38	(174 - 217)	R33	(184 - 227)
R27	(175 - 218)	R22	(185 - 228)
R37	(176 - 219)	R32	(186 - 229)
R26	(177 - 220)	R21	(187 - 230)
R36	(178 - 221)	R31	(188 - 231)
R25	(179 - 222)	R20	(189 - 232)
R35	(180 - 223)	R30	(190 - 233)
R19	(1 - 48)	R9	(11 - 58)
R18	(2 - 49)	R8	(12 - 59)
R17	(3 - 50)	R7	(13 - 60)
R16	(4 - 51)	R6	(14 - 61)
R15	(5 - 52)	R5	(15 - 62)
R14	(6 - 53)	R4	(16 - 63)
R13	(7 - 54)	R3	(17 - 64)
R12	(8 - 55)	R2	(18 - 65)
R11	(9 - 56)	R1	(19 - 66)
R10	(10 - 57)	R40	(20 - 67)



PARTS LOCATION

MODULE P170

RESISTORS

R1	(197 - 154)	R8	(32 - 79)
R2	(6 - 53)	R9	(33 - 80)
R3	(22 - 69)	R10	(34 - 81)
R4	(28 - 75)	R11	(40 - 87)
R5	(29 - 76)	R12	(41 - 88)
R6	(30 - 77)	R13	(42 - 89)
R7	(31 - 78)	R14	(43 - 90)

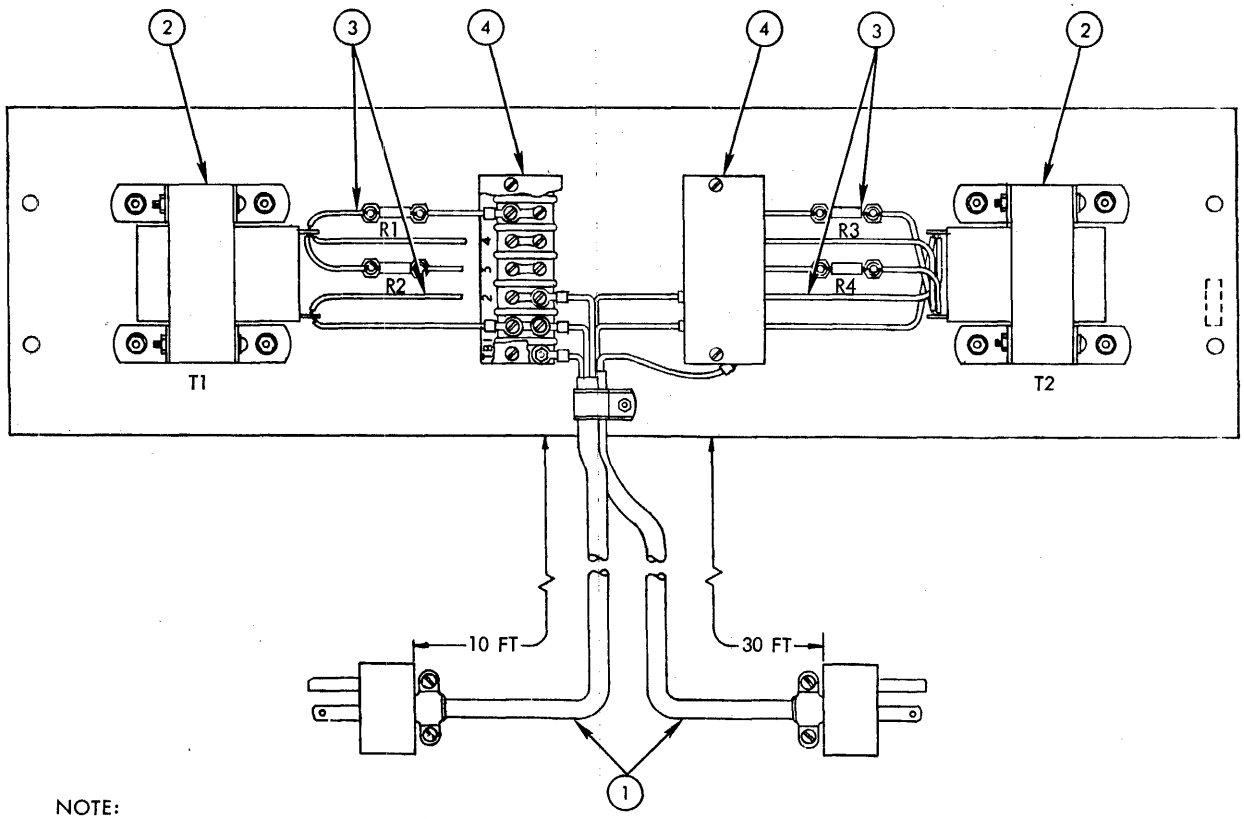
INDUCTORS

L1	(6 - 53)	L8	(33 - 80)
L2	(22 - 69)	L9	(34 - 81)
L3	(28 - 75)	L10	(40 - 87)
L4	(29 - 76)	L11	(41 - 88)
L5	(30 - 77)	L12	(42 - 89)
L6	(31 - 78)	L13	(43 - 90)
L7	(32 - 79)		

NOTE: REFERENCE SDS DWG: 100611B

Figure 6-8. Cable Plug Printed Wiring Board Parts Location

900613A.632



NOTE:
1. REFERENCE SDS DWG: 116989-2C

901029A. 4

Figure 6-9. Power Protection Panel Parts Location

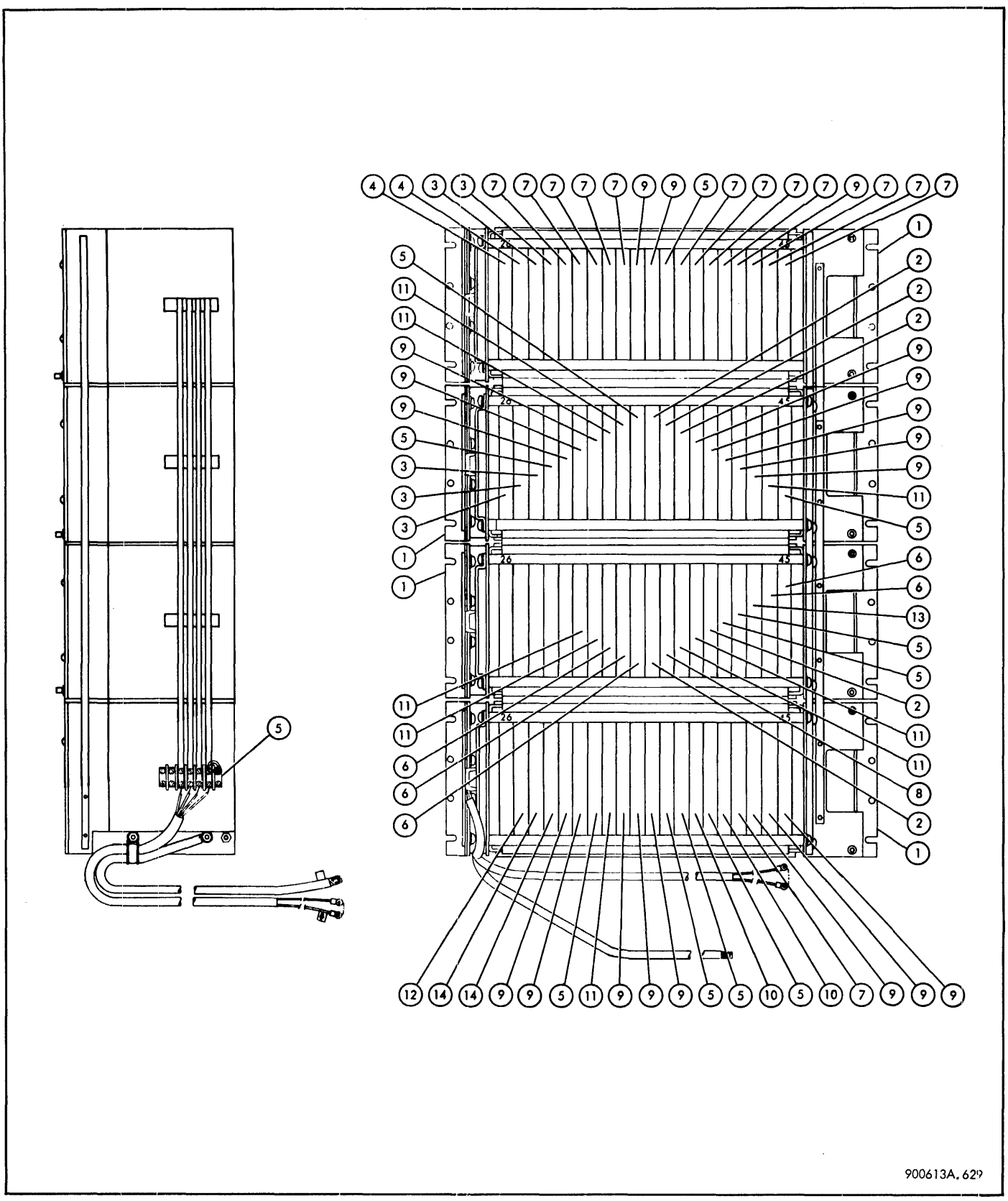


Figure 6-10. Controller Parts Location

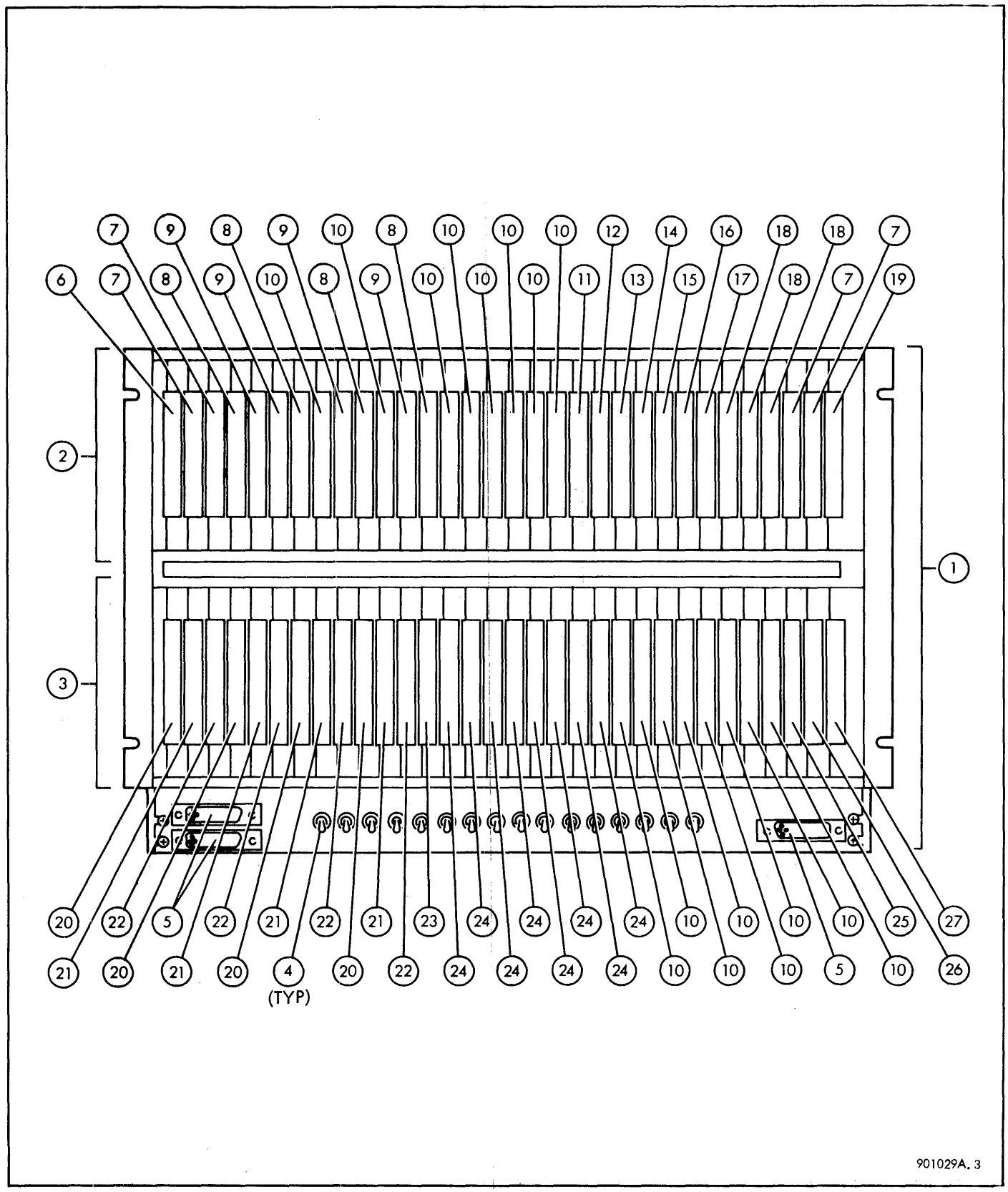


Figure 6-11. Selection Unit Parts Location

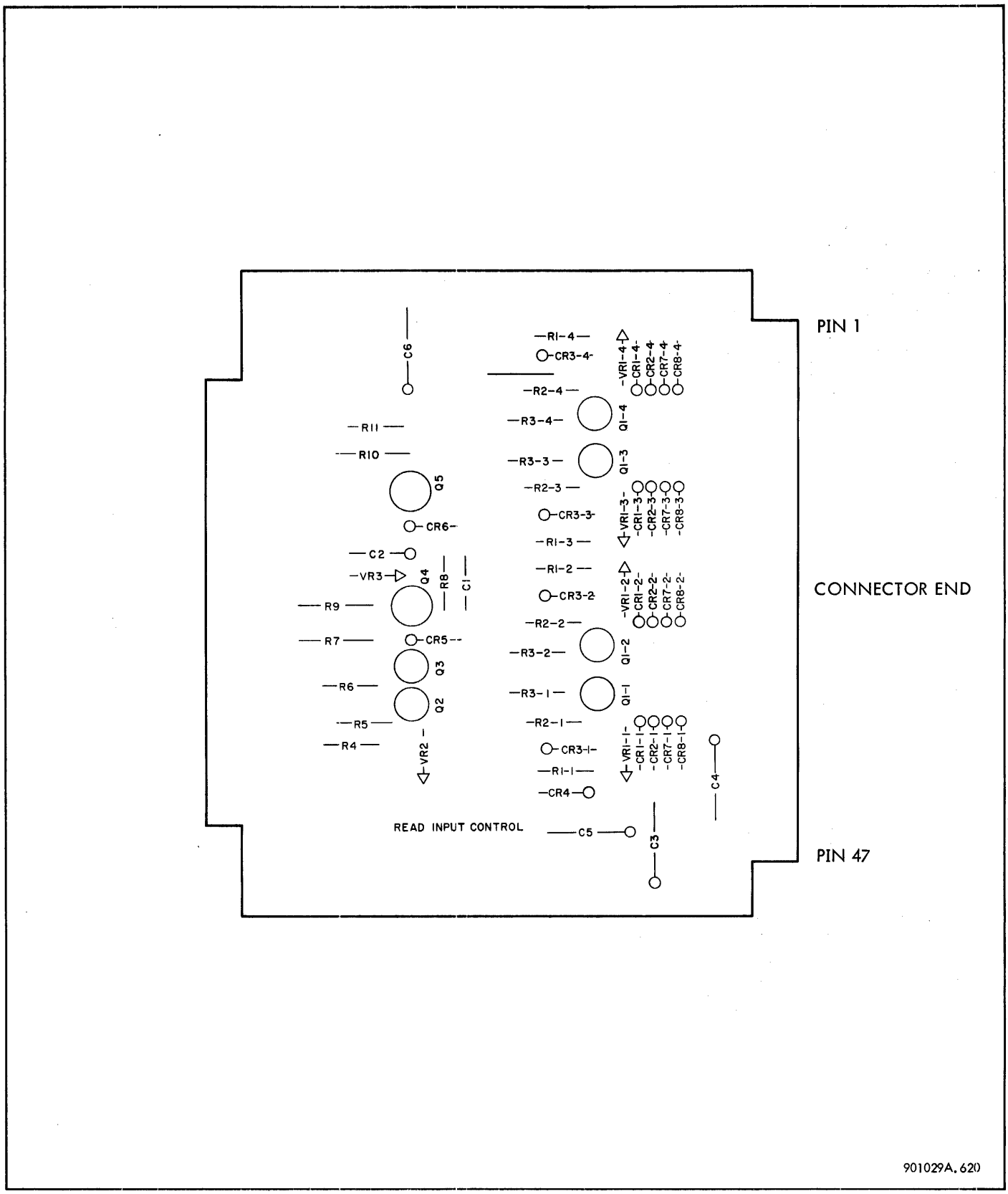


Figure 6-12. Read Input Control AK61 Parts Location

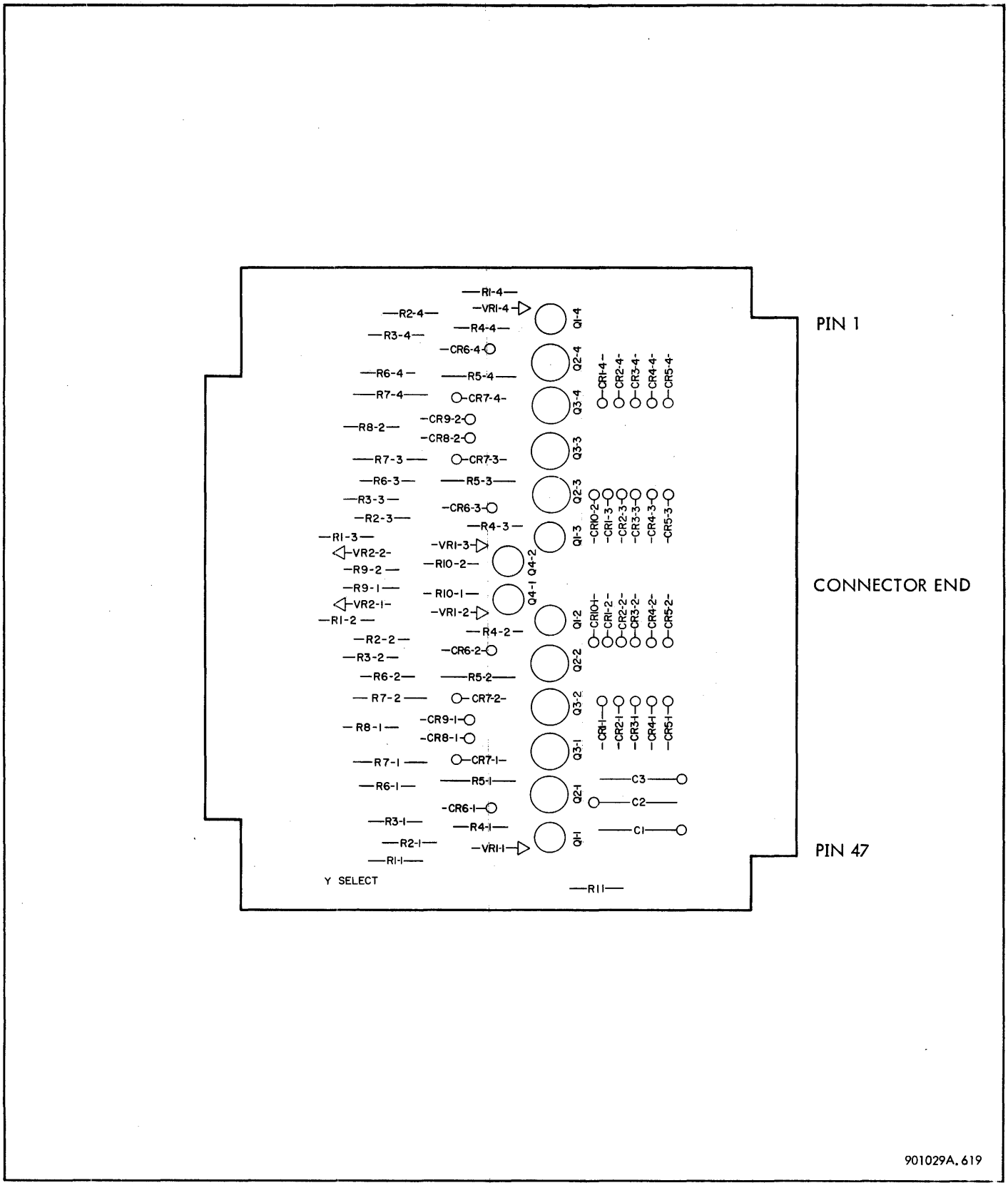


Figure 6-13. Y-Selector AK62 Parts Location

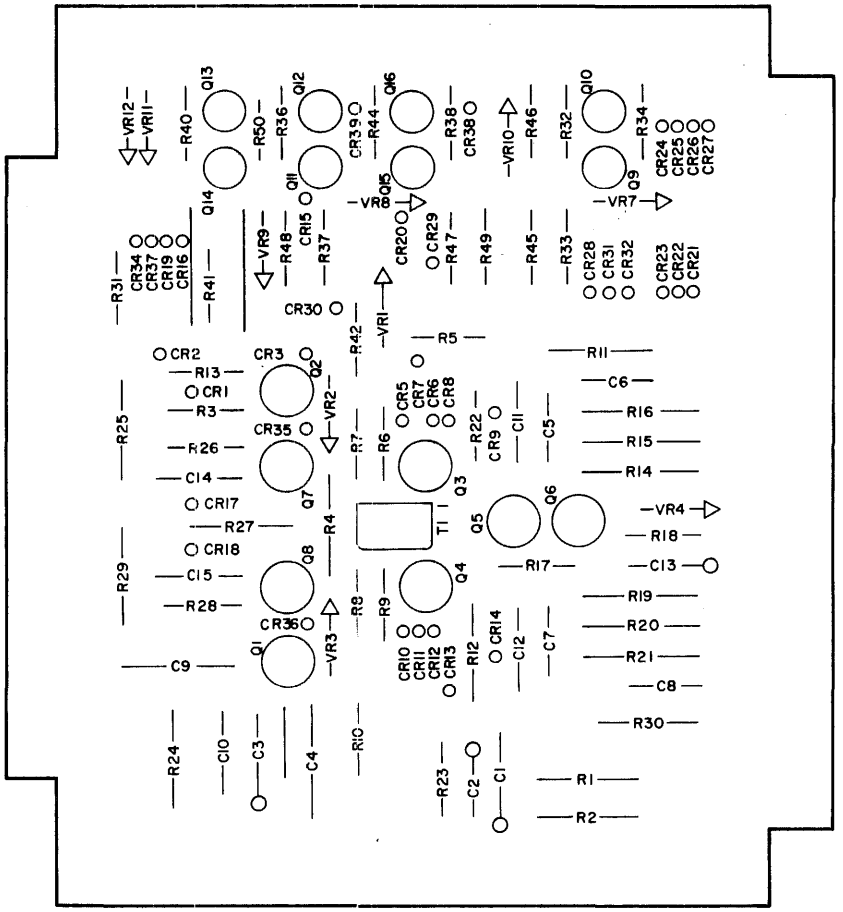


Figure 6-14. Write-Driver AK63 Parts Location

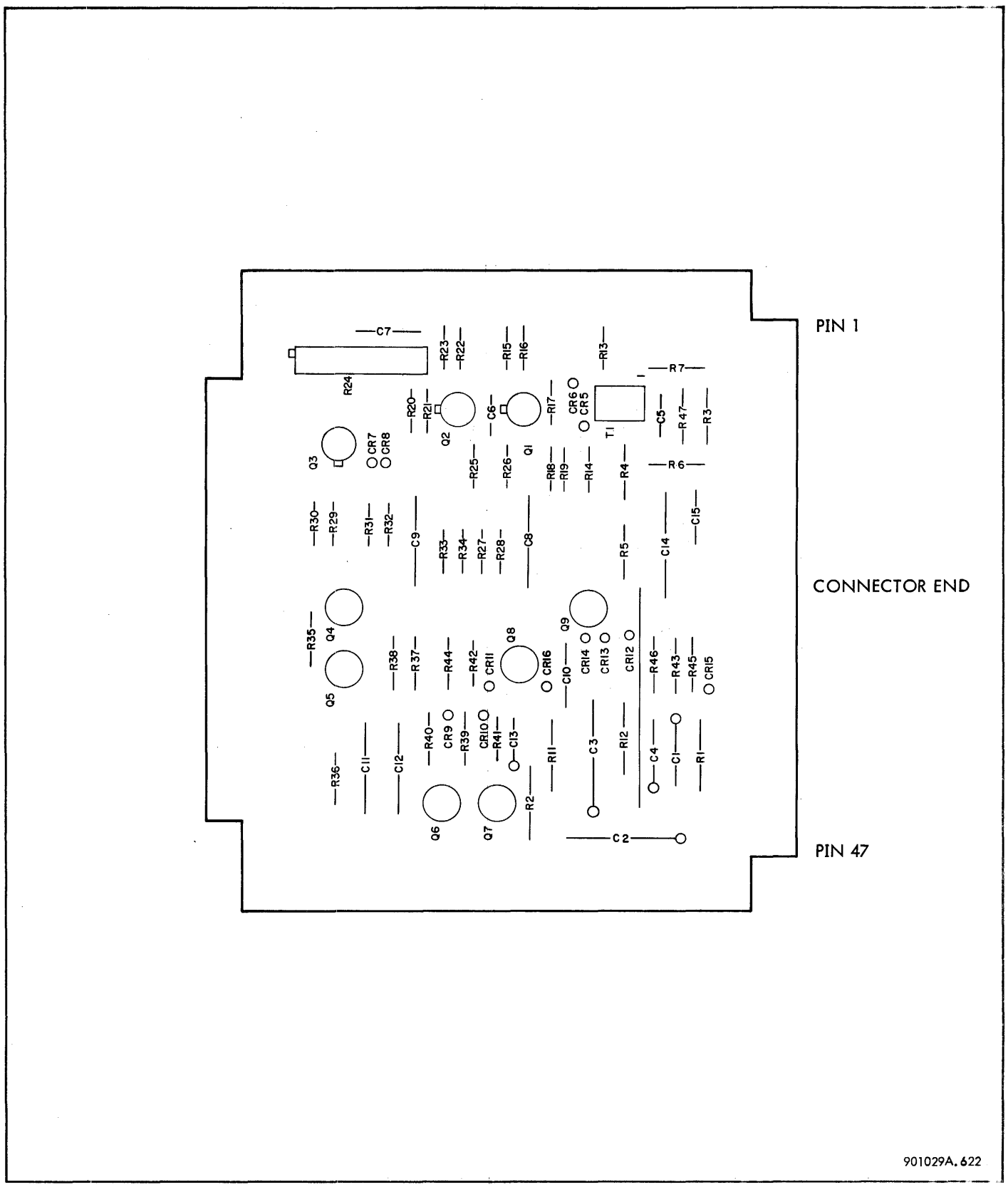


Figure 6-15. Index/Sector Amplifier AK64 Parts Location

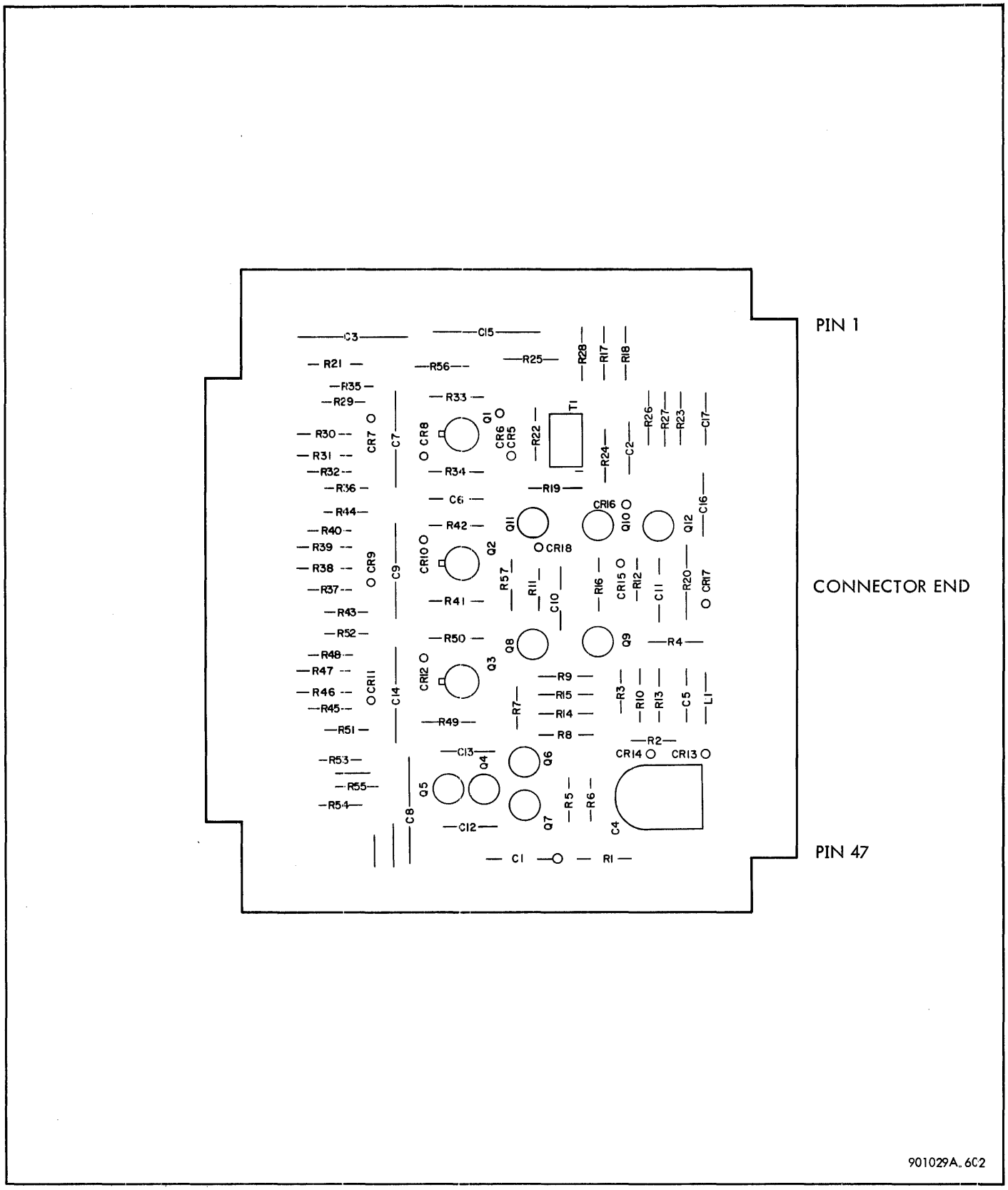


Figure 6-16. Write Clock Amplifier AK65 Parts Location

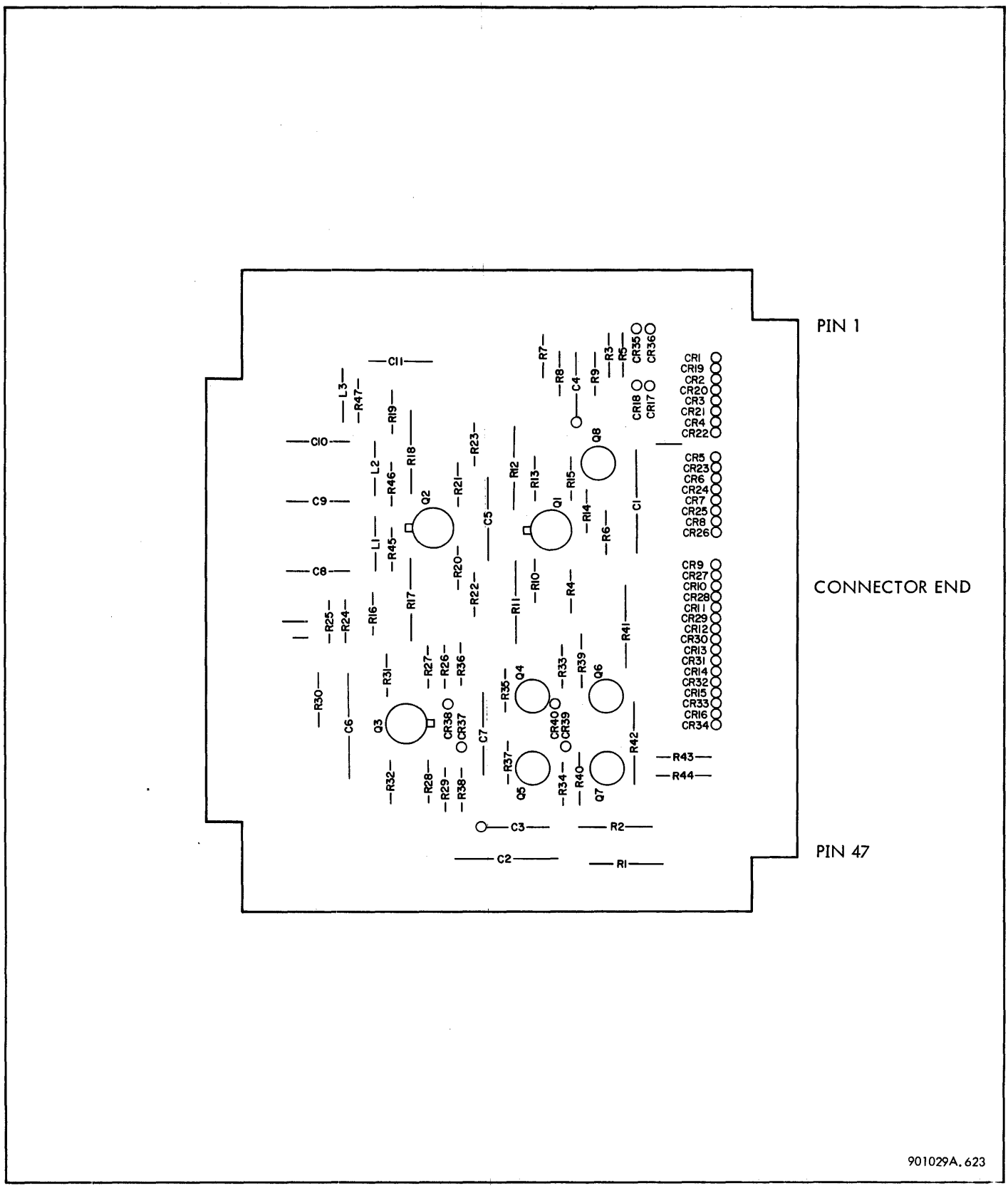


Figure 6-17. Read Preamplifier HK73 Parts Location

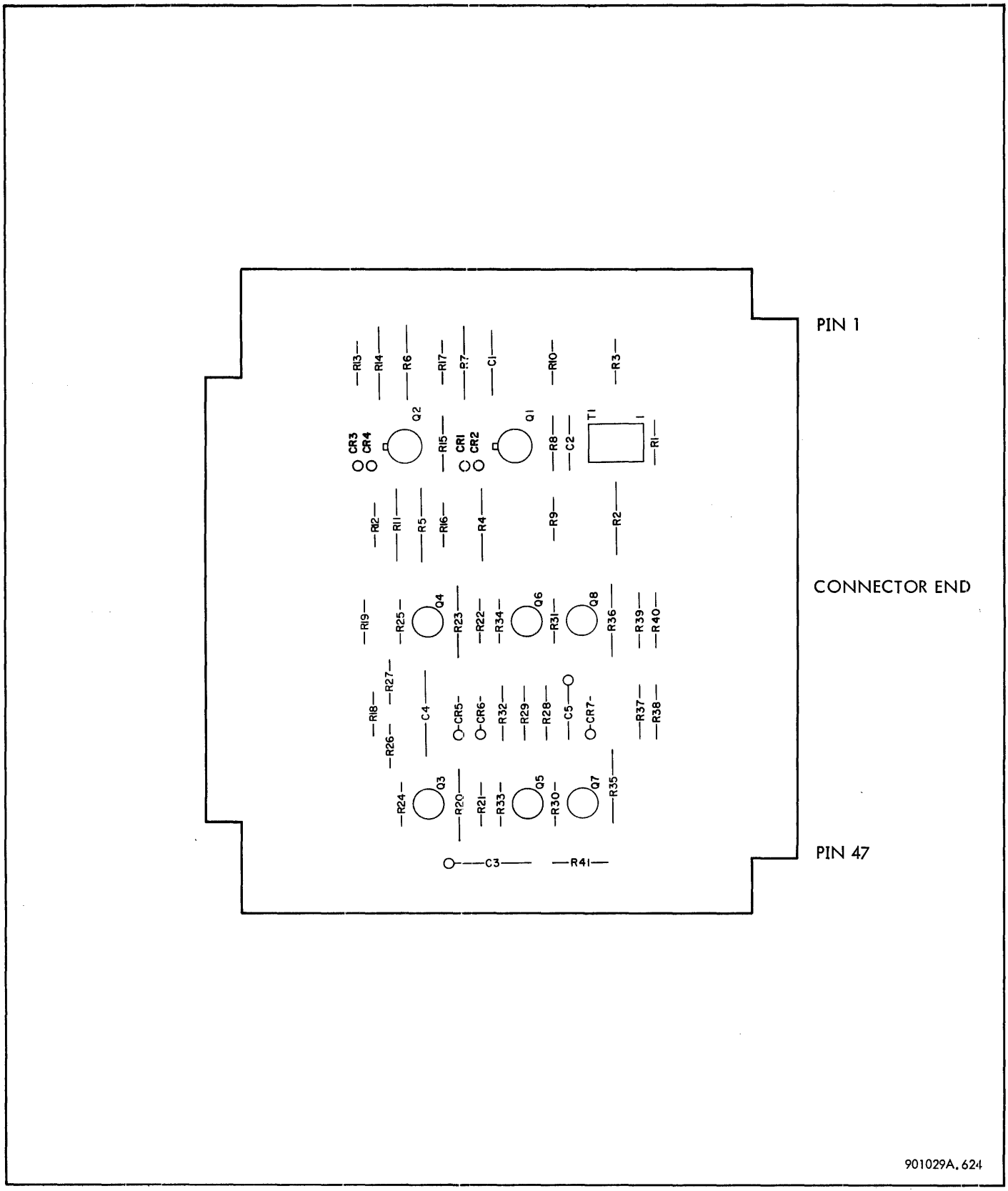


Figure 6-18. Limiter HK74 Parts Location

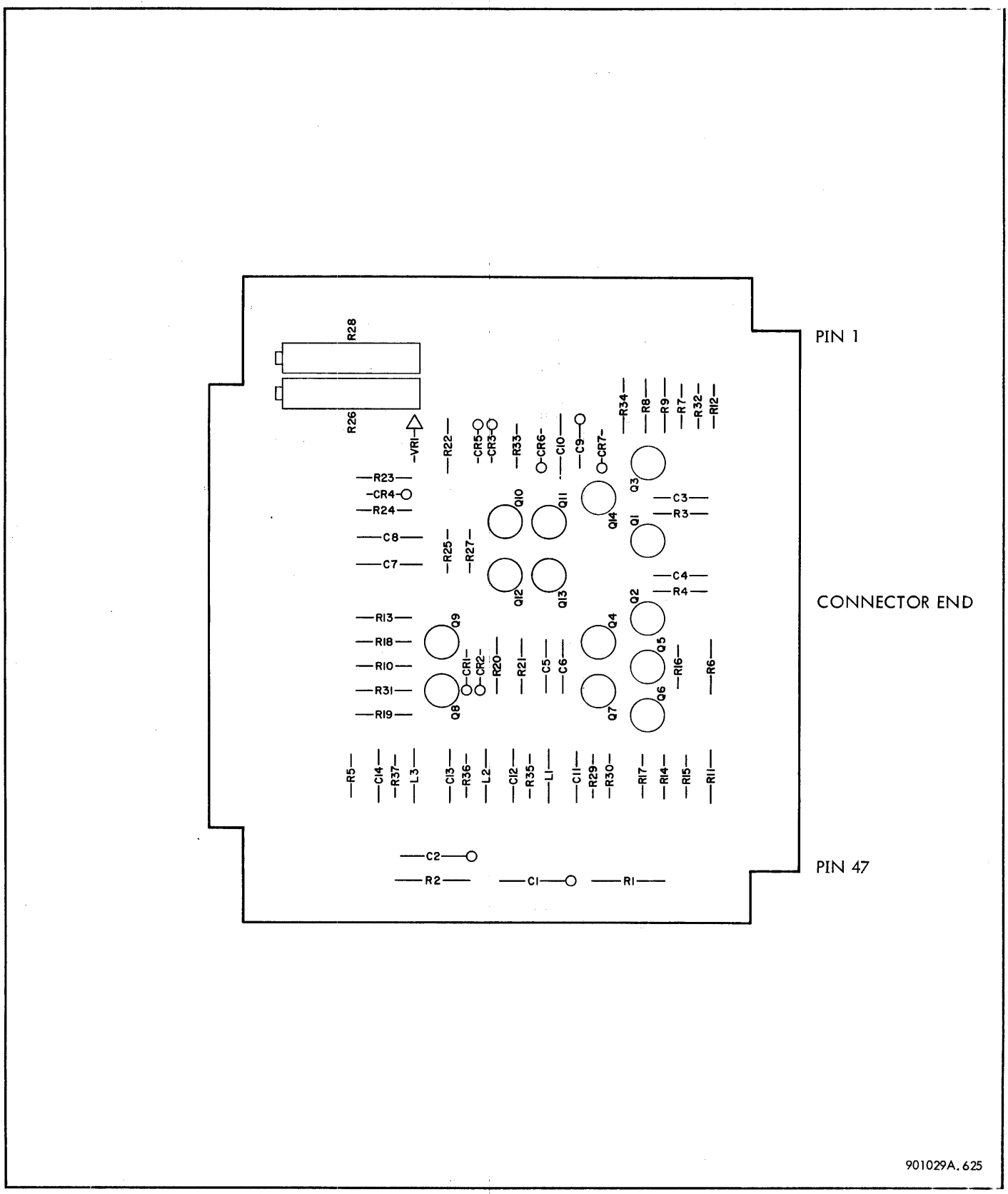


Figure 6-19. Clock Discriminator HK75 Parts Location

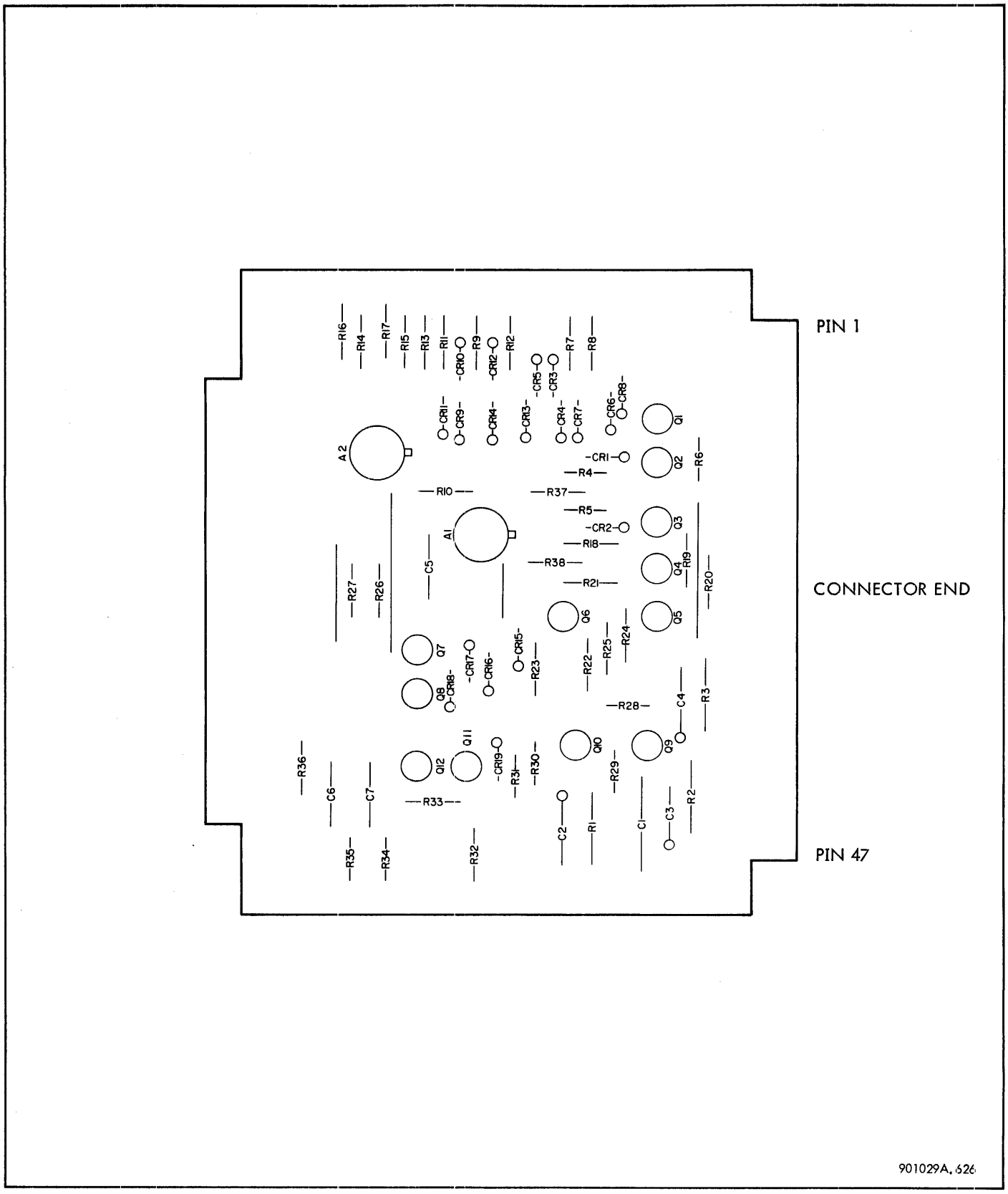


Figure 6-20. Data Decoder HK76 Parts Location

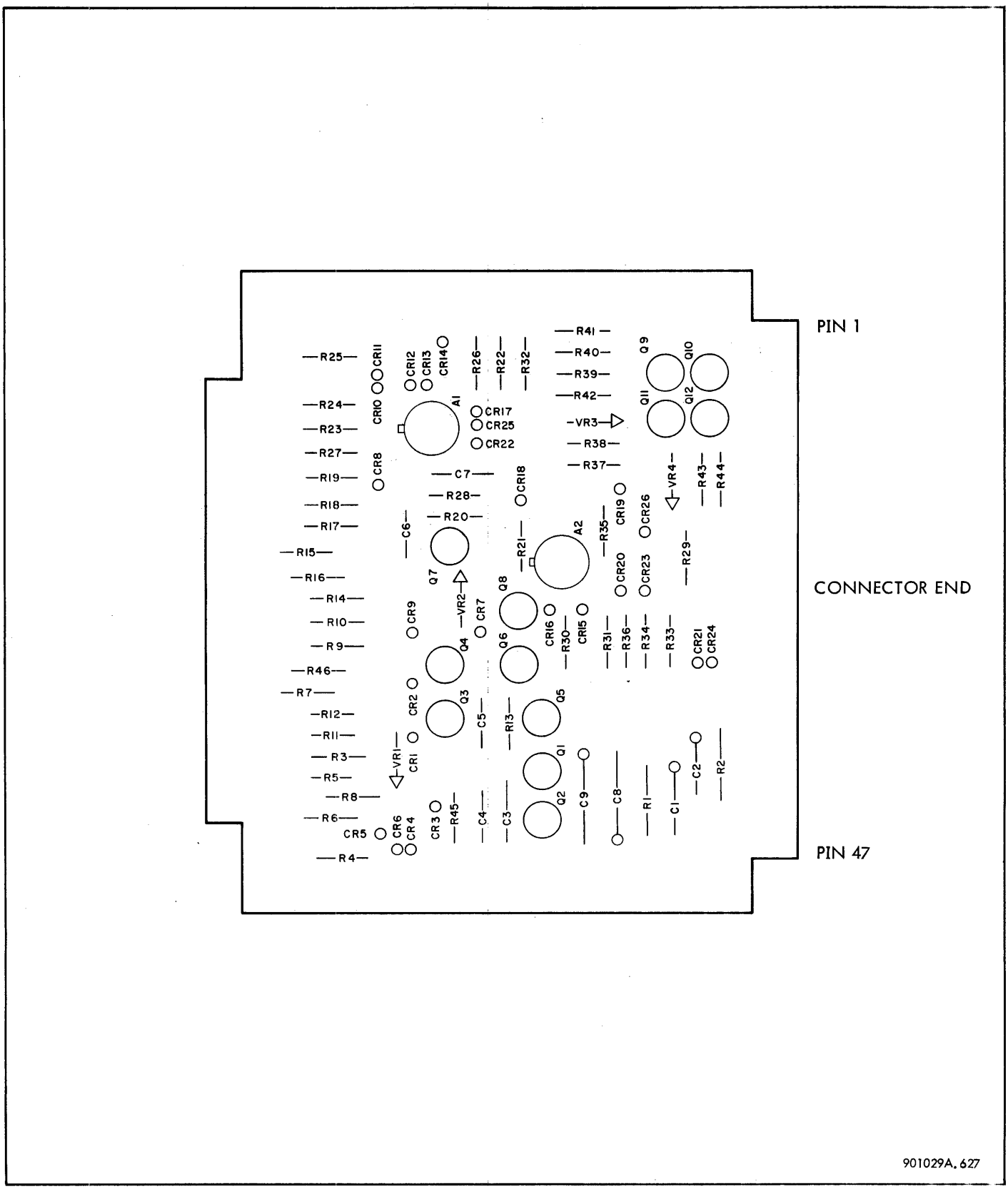


Figure 6-21. Index/Sector Decoder HK77 Parts Location

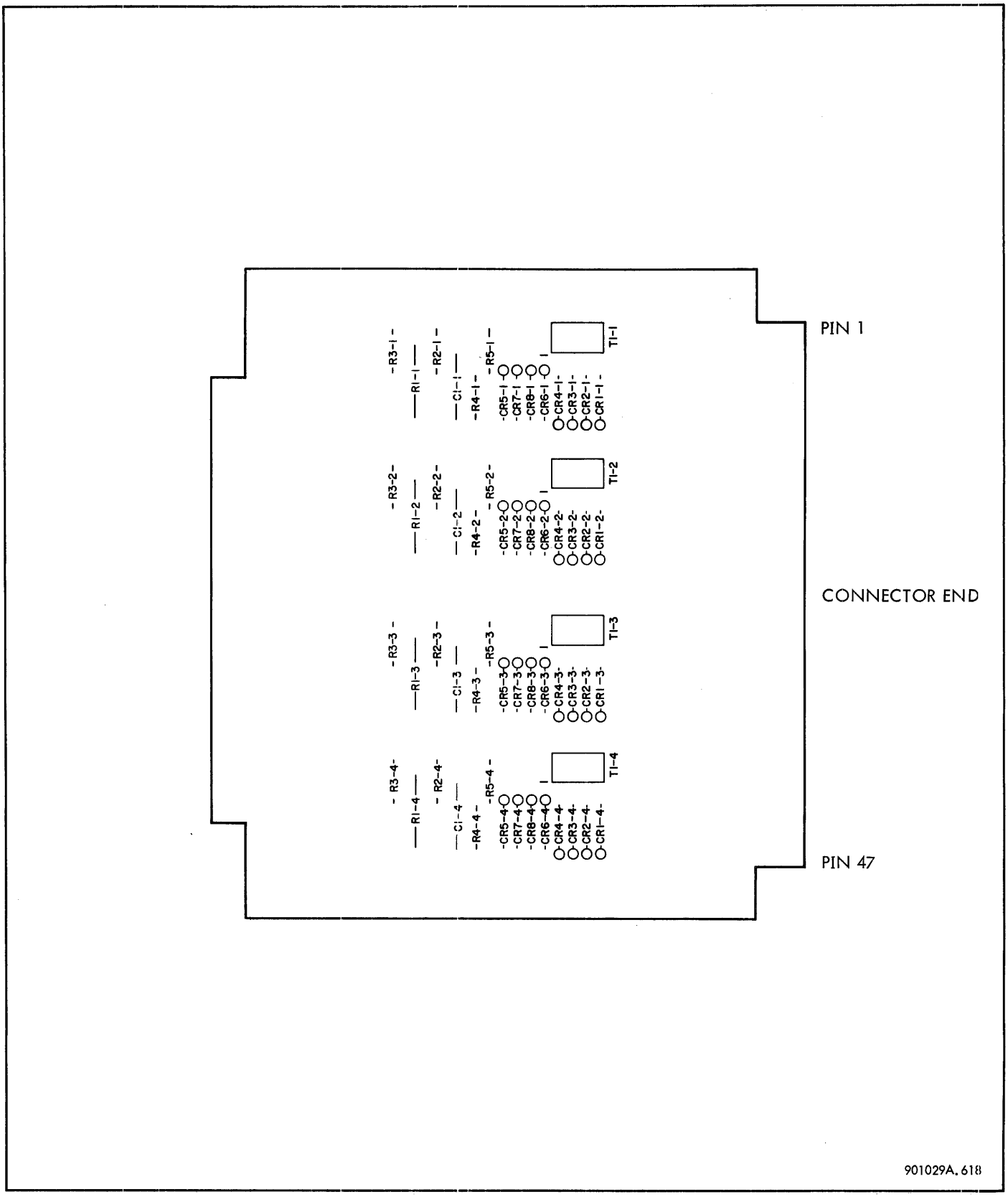
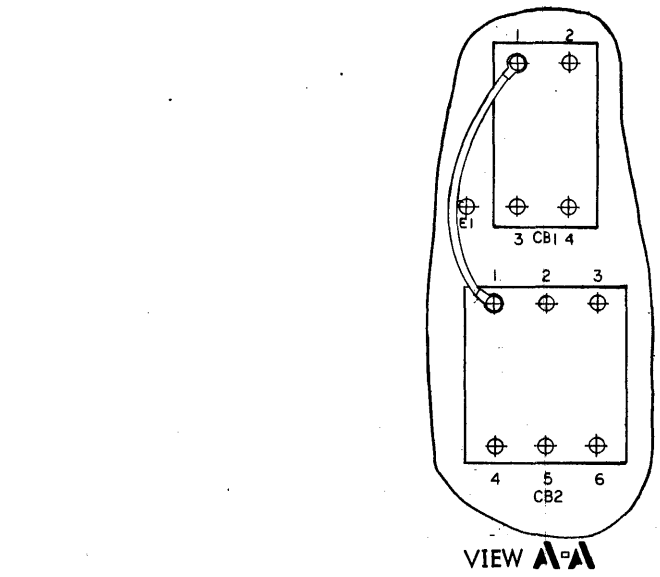
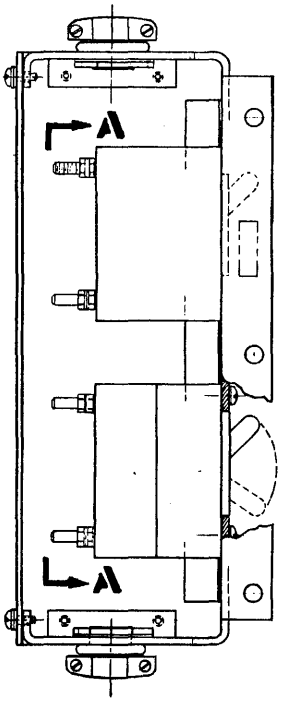
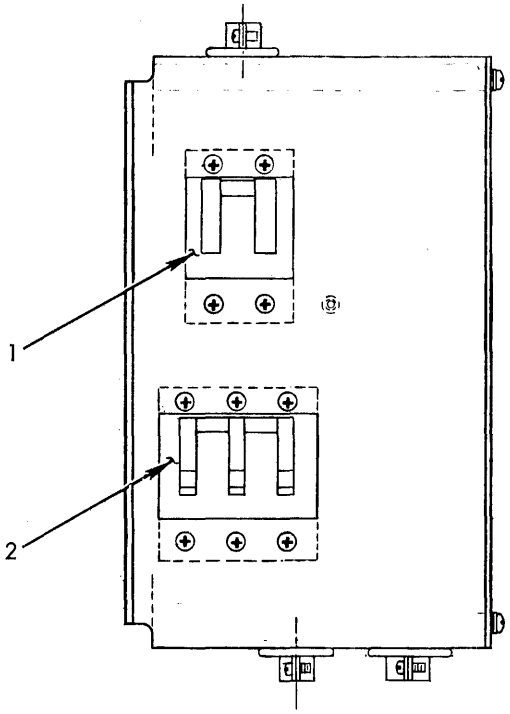


Figure 6-22. Read/Write Decoder NK59 Parts Location







NOTE: REFERENCE SDS DWG: 131365-1D

901029A.629

Figure 6-23. Power Distribution Panel Assembly Parts Location

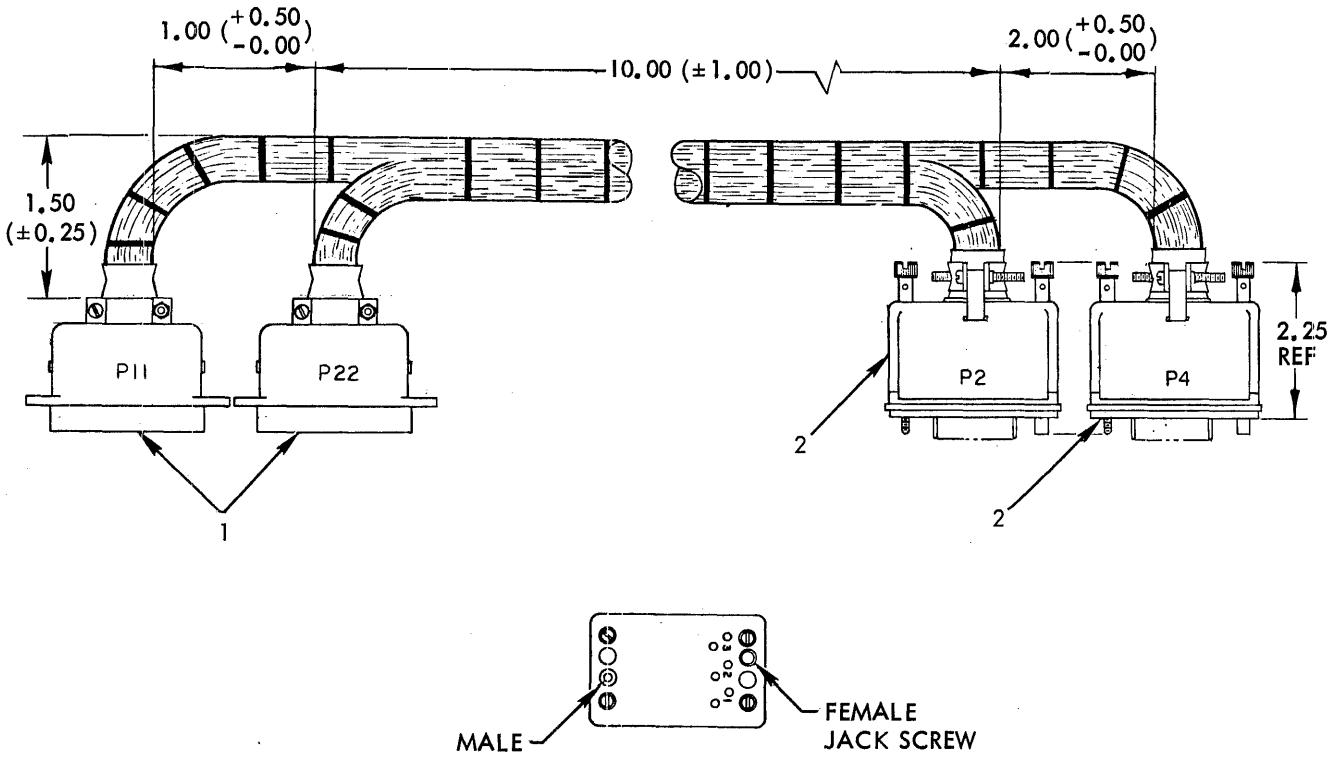
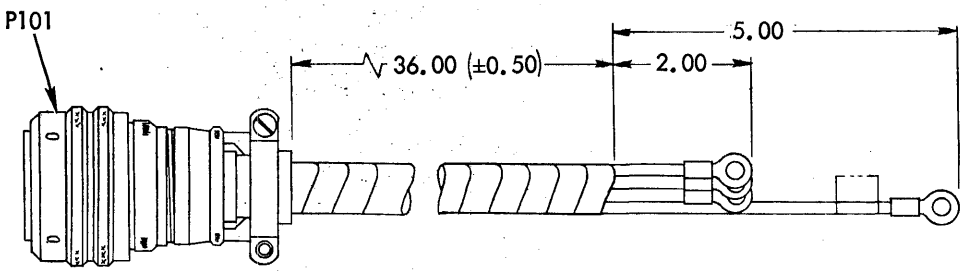


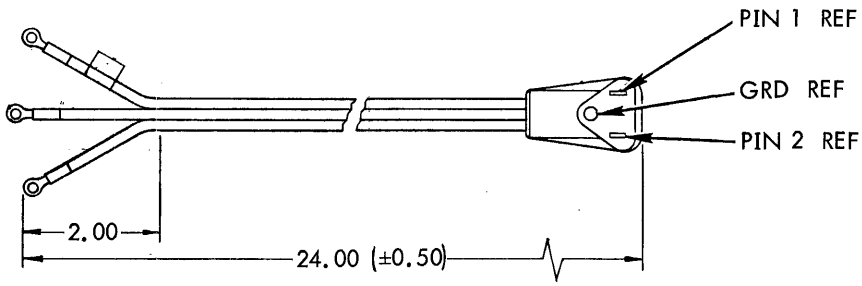
Figure 6-24. Drum Memory Cable Assembly Parts Location



NOTE: REFERENCE SDS DWG: 131825-1A

901029A.631

Figure 6-25. Circuit Breaker to Drum Motor Cable Assembly Parts Location

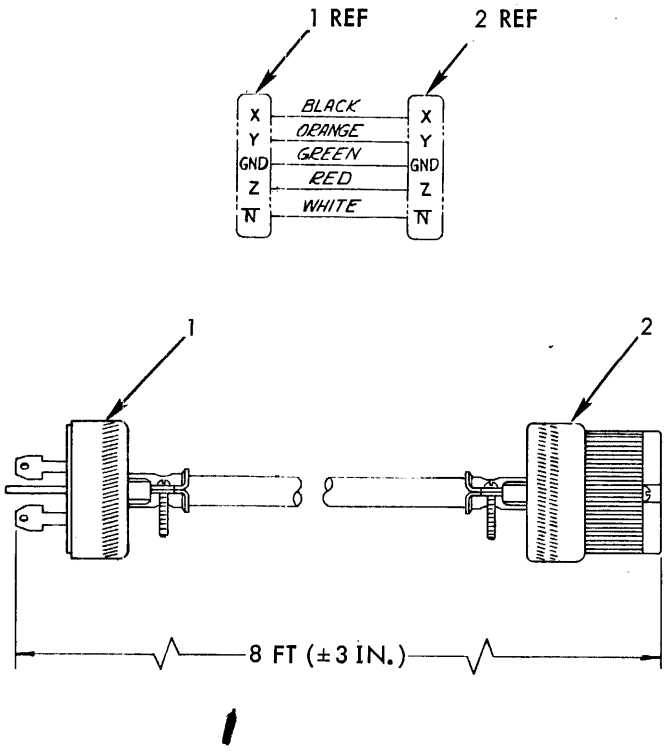


NOTE: REFERENCE SDS DWG: 133304-1B

901029A.632

Figure 6-26. Plug Mold to Power Supply Cable Assembly Parts Location

WIRING DIAGRAM



NOTE: REFERENCE SDS DWG: 133669-1A

901029A.633

Figure 6-27. Power Cord Assembly Parts Location

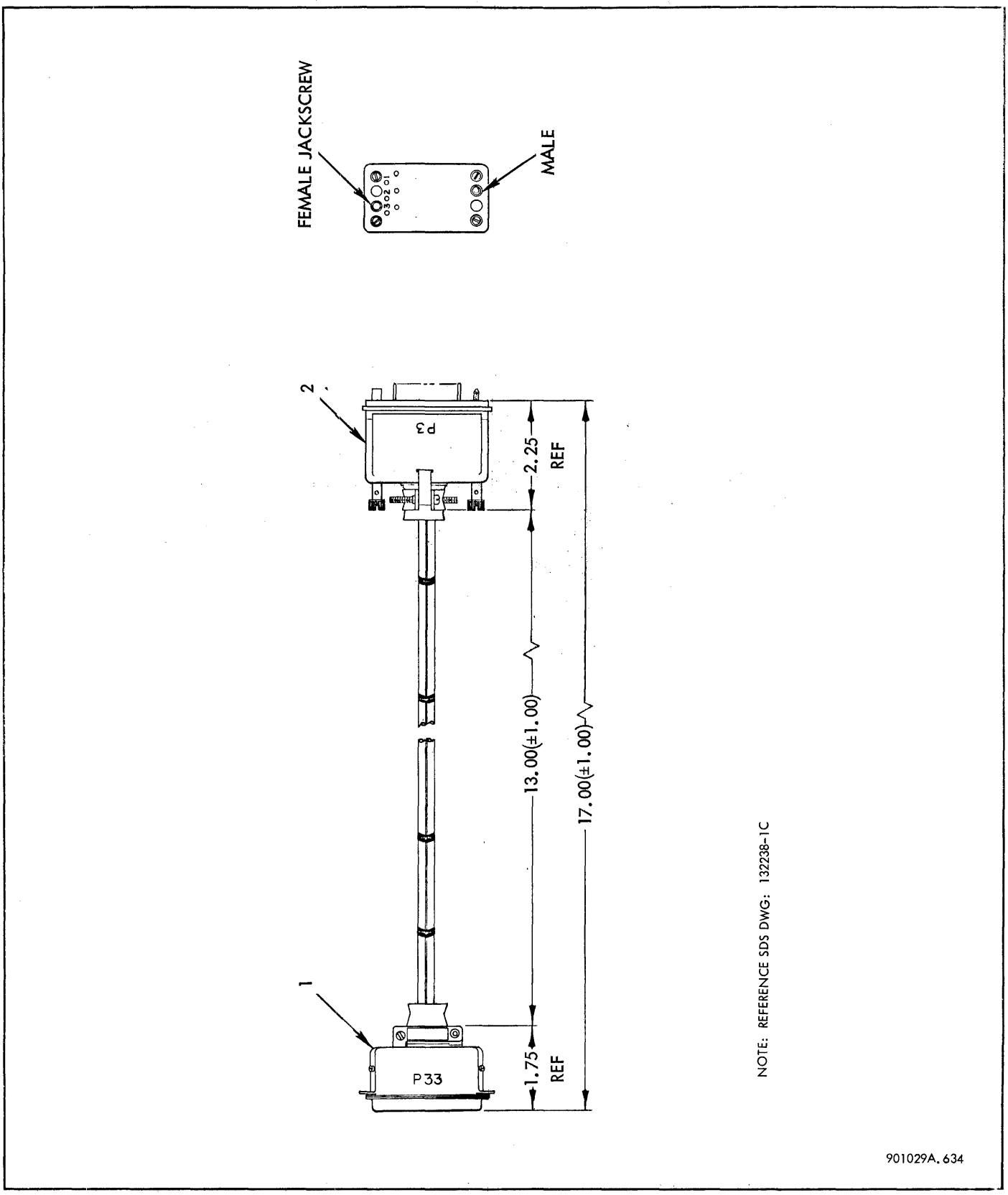
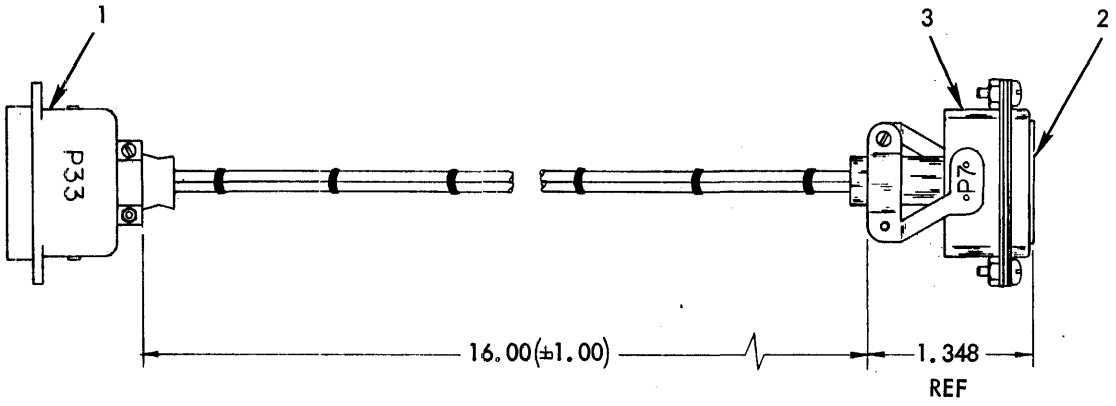


Figure 6-28. Drum Clock Cable Assembly Parts Location



NOTE: REFERENCE SDS DWG: 132240-1D

901029A.635

Figure 6-29. Disc Clock Cable Assembly Parts Location

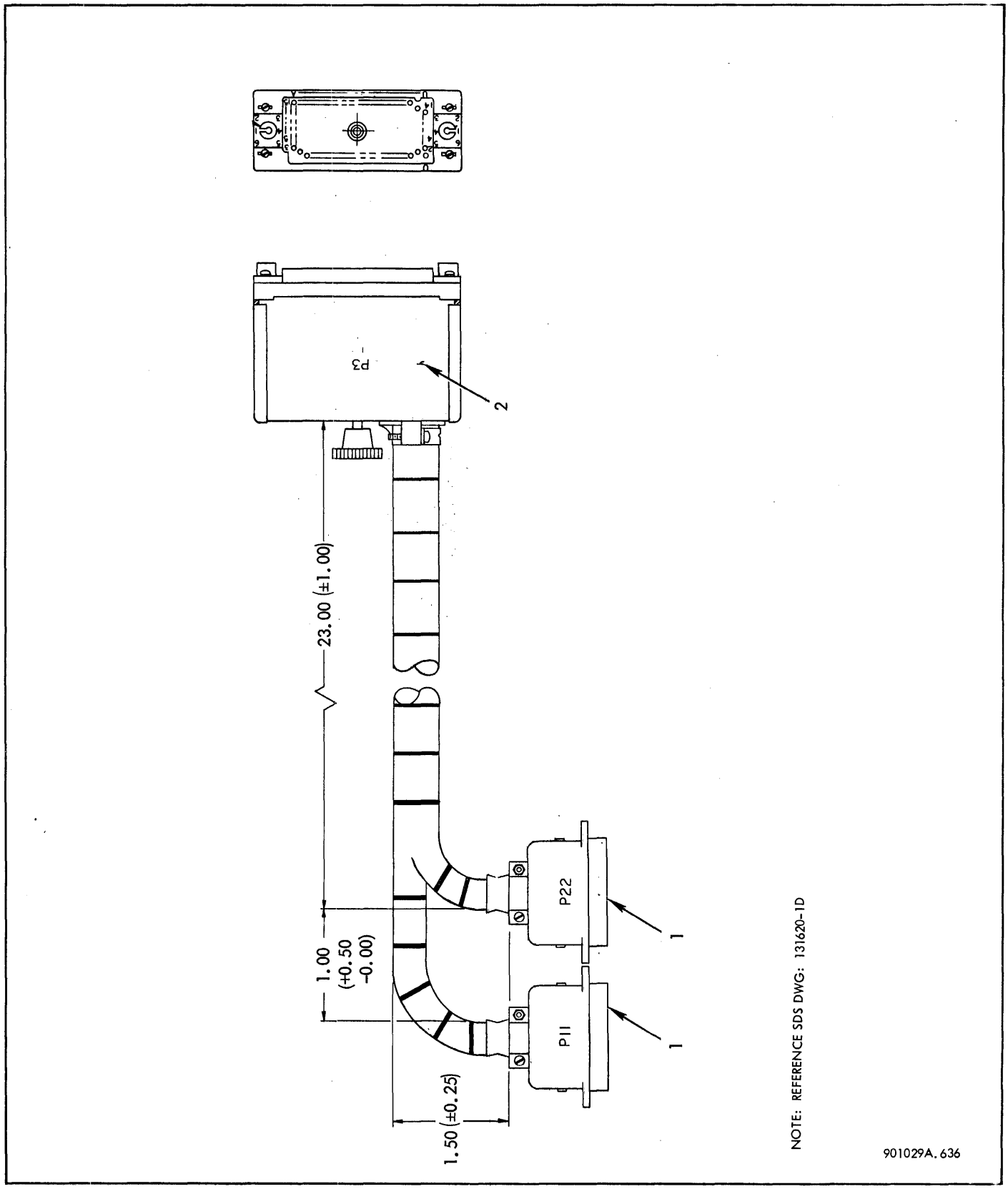


Figure 6-30. Disc Memory Cable Assembly Parts Location

SECTION VII
DRAWINGS

7-1 DOCUMENTATION SOURCES

The documentation package accompanying a RAD file includes a complete set of manufacturing drawings, this technical manual, and selected documents from the List of Related Publications. This section of the manual contains wirelists, schematic diagrams, installation drawings, and assembly drawings (figures 7-1 through 7-25).

7-2 WIRELISTS

7-3 Wirelist Format

Table 7-1 relates RAD file equipment by part number to a specific wirelist document. For the controller and the selection unit, the wirelists provide information in several formats to simplify signal tracing. The basic information provided is the location of all points in the assembly associated with a specific signal mnemonic. Signals are listed alphabetically by the three-character mnemonic, suffix, and prefix. A list of three-character mnemonics in the controller and selection unit, and a description of the relation between three-character mnemonics and five-character mnemonics are included in section VIII.

Wirelist data formats are illustrated in figure 7-1. For each signal, the wirelist provides the following information:

CHASSIS LOCATION	The chassis of the assembly (A, B, C, or D for the controller; A or B for the selection unit)
MODULE LOCATION	The location of the module in the chassis
PIN LOCATION	The connector pin to which the designated signal is fed
MODULE NAME	The module type inserted at the location

7-4 Signal Tracing

The entry for signal (A, figure 7-1) shows that signal BK06A is connected between chassis A, location J37, pin 5, and chassis A, location J43, pin 43. The module in location J43 is a basic flip-flop FH20. The module in location J37 is an AND/OR buffer amplifier BH10.

The wirelist data shown in paragraph 7-3 is categorized three ways: a. All signals are listed; b. A list of all signals in each chassis is provided; and c. A list of all signals crossing from one chassis to another is provided for each chassis (B, figure 7-1).

A dictionary listing provided for each chassis (C, figure 7-1) is a matrix with each possible pin number assigned to a horizontal row, and each possible location number assigned to a vertical column. Each cell of the matrix shows the signal connected to the corresponding location and pin. If no signal is connected to a pin at a particular location, the corresponding cell of the matrix is blank. Each column of the matrix thus indicates all signals to a module in a particular location. No signal is connected to pin 1 of locations 41, 42, or 45 of chassis B. Jumper signal J184 is connected to pin 1 in locations 39 and 40.

Table 7-1. RAD File Wirelists

Equipment	Part Number	Wirelist Document Number
Controller (logic)	131564	131565
Controller (power)	131564	133548
Selection unit (logic)	129484	129485
Selection unit (power)	129484	131613
Selection unit (switch and connector)	129484	132235
Drum matrix cable assembly	131623	132236
Drum clock cable assembly	132238	132239
Disc matrix cable assembly	131620	132237
Disc clock cable assembly	132240	132241
Power protection panel	116989	134018
Plug module cable assembly P155/P156	113899	113900
Plug module cable assembly P157/P158	113902	113903
Plug module cable assembly P159/P160	113896	113897
Plug module cable assembly P161/P162	116388	116389
Plug module cable assembly P168/P169	116509	116511
Plug module cable assembly P170/P171	116513	116515

LOGIC ID	RACK LOCATION	CHASSIS LOCATION		MODULE LOCATION		PIN LOCATION	MODULE NAME	
0K05A		A C	J	42	E	10	BH10	1
						-		3
1K05A		A A	J	44	E	37	FH20	1
		A A	J	44	E	41	FH20	5
								6
BK06A		A A	J	37	E	05	BH10	5
		A A	J	43	E	43	FH20	N
0K06A		A A	J	37	E	29	BH10	
		A A	J	43	E	36	FH20	
		A A	J	44	E	35	FH20	
		A A	J	44	E	43	FH20	

A. SIGNAL LIST

CROSS-CHASSIS WIRELIST

LOGIC ID	RACK LOCATION	CHASSIS LOCATION		MODULE LOCATION		PIN LOCATION	MODULE NAME	
9CD1S		A C	J	31	E	02	IH14	1
		A D	J	30	E	32	GK51	3
								1
2CD2A		A C	J	31	E	01	IH14	5
		A D	J	30	E	20	GK51	6
								5
9CD2S		A C	J	31	E	06	IH14	N
		A D	J	30	E	24	GK51	
2CD3A		A C	J	32	E	40	IH14	
		A D	J	32	E	08	BH10	
9CD3S		A C	J	32	E	34	IH14	
		A D	J	30	E	04	GK51	

B. CROSS-CHASSIS WIRELIST

AS OF 12-03-66

DICTIONARY
DRAWING 131565N
FOR
CHASSIS B

PIN	36	37	38	39	40	41	42	43	44	45	PIN
1	4CLKA	202FA	201FA	J072	J070			J175	6CLKA		1
2		1F02A	0F02A	J054	J056			J034	3W50A	0K04A	2
3				J114	YS06A	J053	J090	J175		6NNLA	3
4	6CLKA	0F01A	1F01A			0U02A		6DRVA		0K03A	4
5					2LDSA	0U01A		1X06A		2TNIA	5
6					0Z06A	0U03A		2W56A	9CLKS	2SPRA	6
7				2LDSA	2LDSA					DK04A	7
8				J072	YS05A	J167	J126	6NNLA	2W50A	2LSCA	8
9				DS01A						0K02A	9
10				0Z01A	0Z05A	2CLKD		0K05A		2K06A	10

C. DICTIONARY

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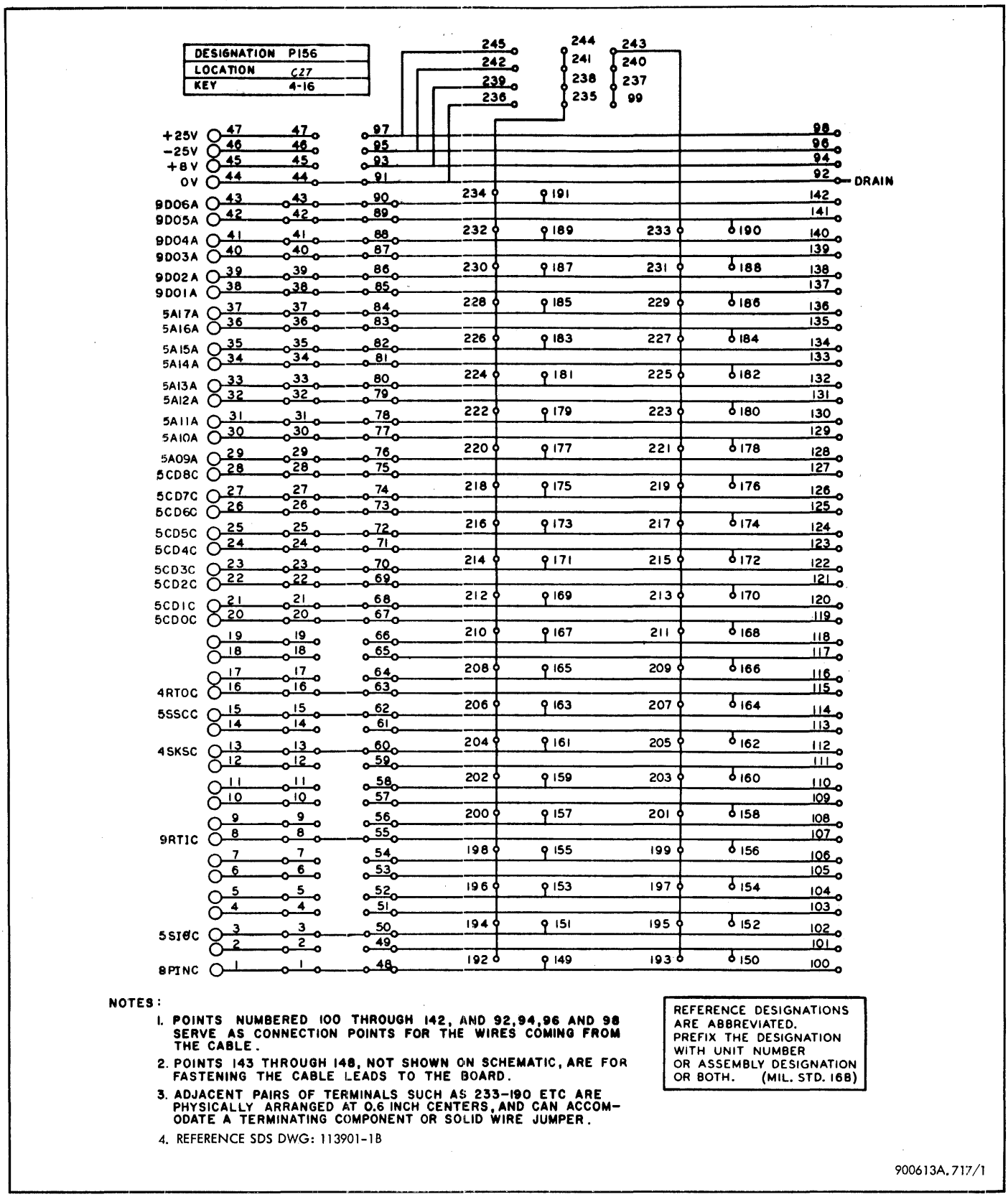
Figure 7-1. Wirelist Data Format



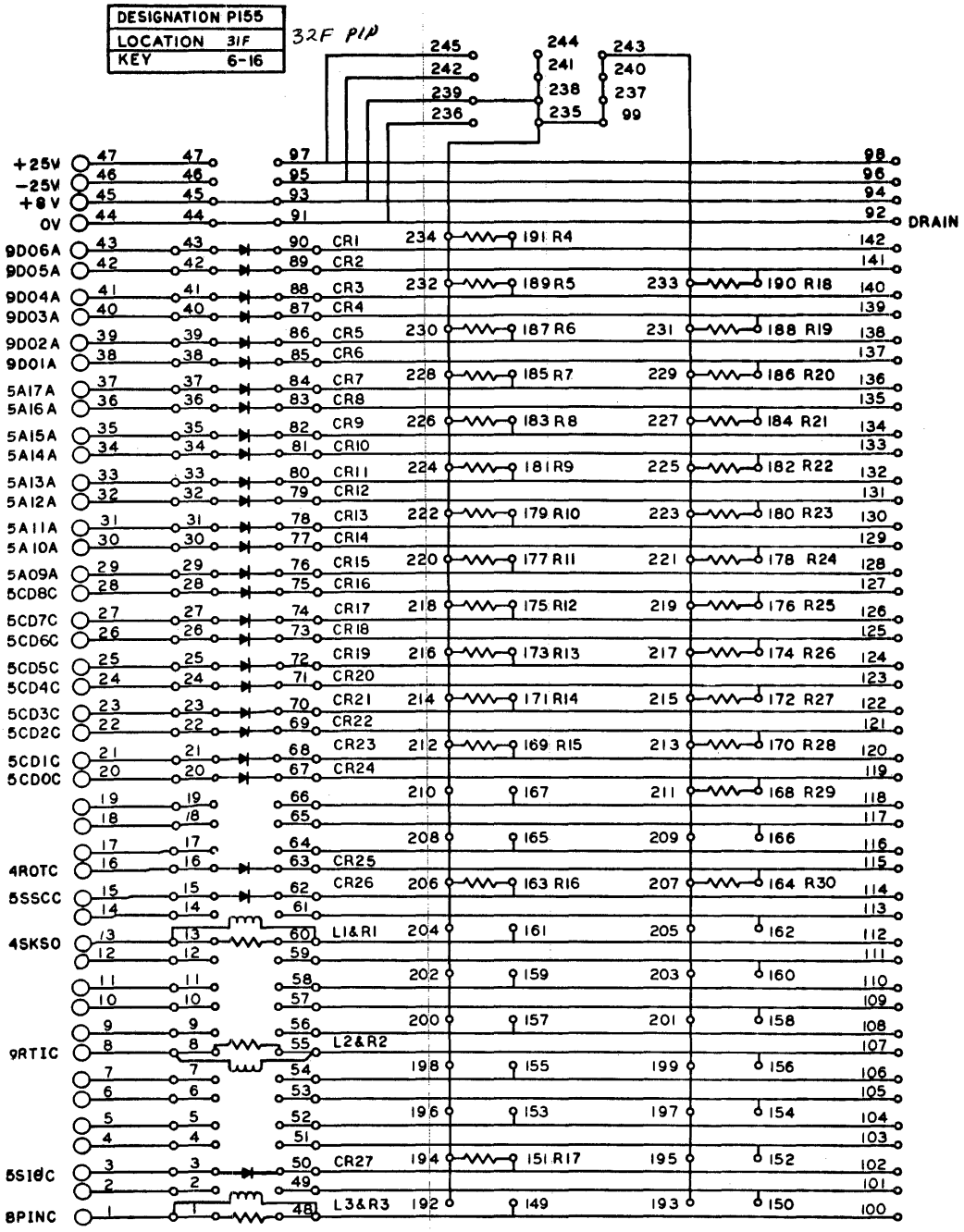
NOTES:

1. POINTS NUMBERED 100 THROUGH 142, AND 92,94,96 AND 98 SERVE AS CONNECTION POINTS FOR THE WIRES COMING FROM THE CABLE.
2. POINTS 143 THROUGH 148, NOT SHOWN ON SCHEMATIC, ARE FOR FASTENING THE CABLE LEADS TO THE BOARD.
3. ADJACENT PAIRS OF TERMINALS SUCH AS 233-190 ETC ARE PHYSICALLY ARRANGED AT 0.6 INCH CENTERS, AND CAN ACCOMODATE A TERMINATING COMPONENT OR SOLID WIRE JUMPER.
4. REFERENCE SDS DWG: 113901-1B

REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH. (MIL. STD. 168)

900613A.717/1

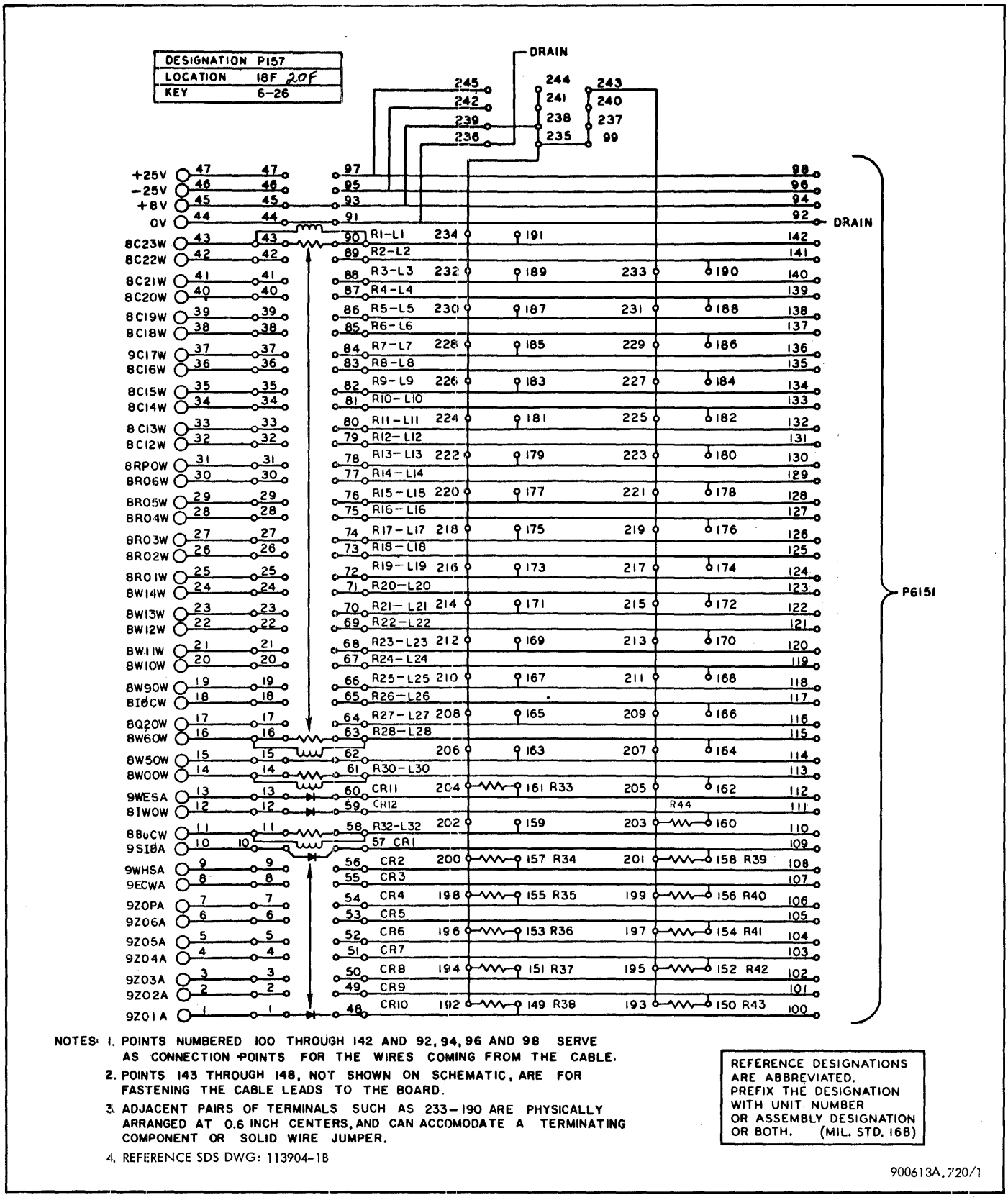
Figure 7-2. Plug Module Cable Assembly P155/P156 Schematic Diagram (Sheet 1 of 2 sheets)



NOTE: REFERENCE SDS DWG: 113901-2B

900613A.717/2

Figure 7-2. Plug Module Cable Assembly P155/P156 Schematic Diagram (Sheet 2 of 2 sheets)



NOTES:
1. POINTS NUMBERED 100 THROUGH 142 AND 92, 94, 96 AND 98 SERVE AS CONNECTION POINTS FOR THE WIRES COMING FROM THE CABLE.
2. POINTS 143 THROUGH 148, NOT SHOWN ON SCHEMATIC, ARE FOR FASTENING THE CABLE LEADS TO THE BOARD.
3. ADJACENT PAIRS OF TERMINALS SUCH AS 233-190 ARE PHYSICALLY ARRANGED AT 0.6 INCH CENTERS, AND CAN ACCOMODATE A TERMINATING COMPONENT OR SOLID WIRE JUMPER.
4. REFERENCE SDS DWG: 113904-1B

REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH. (MIL. STD. 168)

900613A.720/1

Figure 7-3. Plug Module Cable Assembly P157/P158 Schematic Diagram (Sheet 1 of 2 sheets)

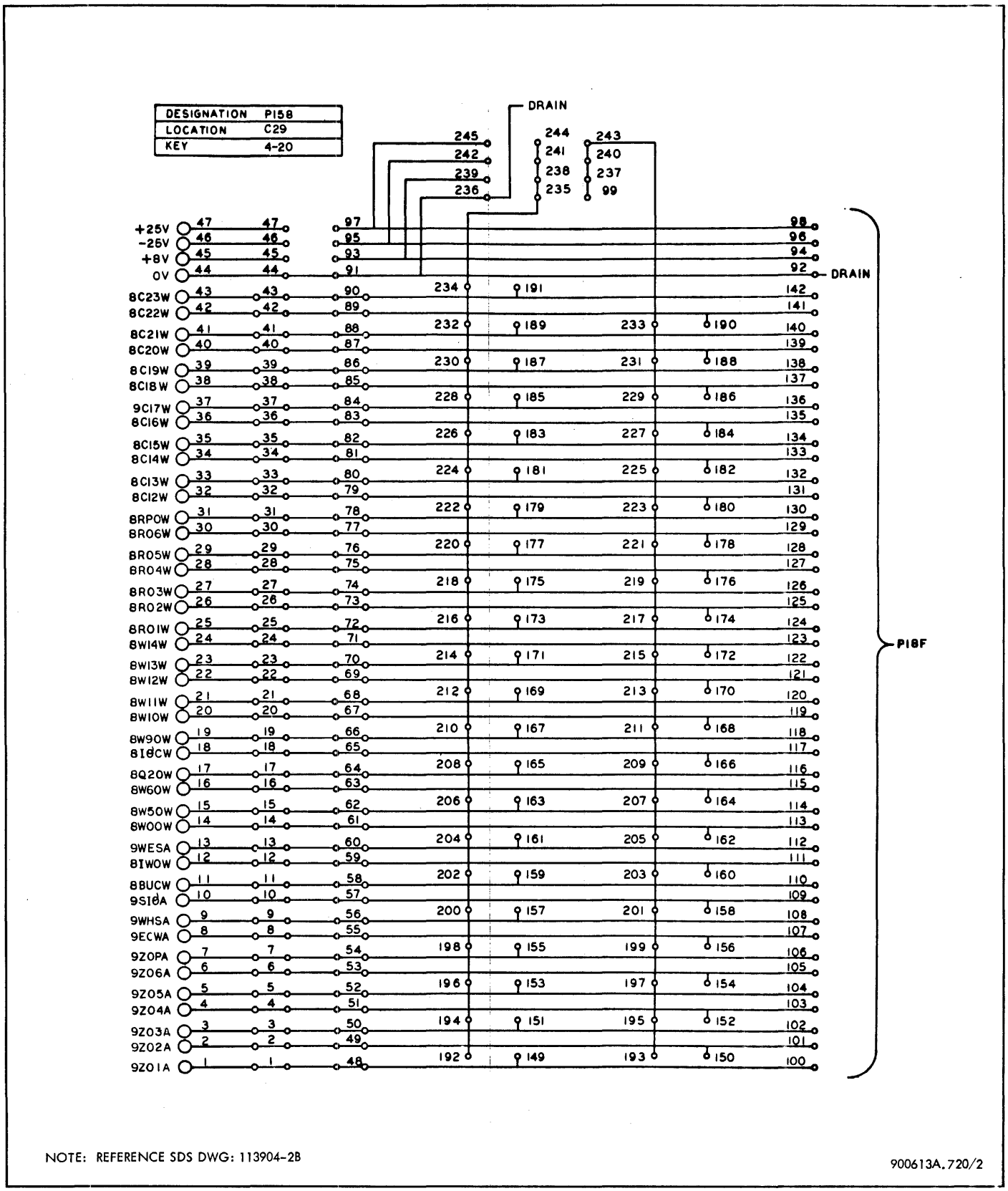
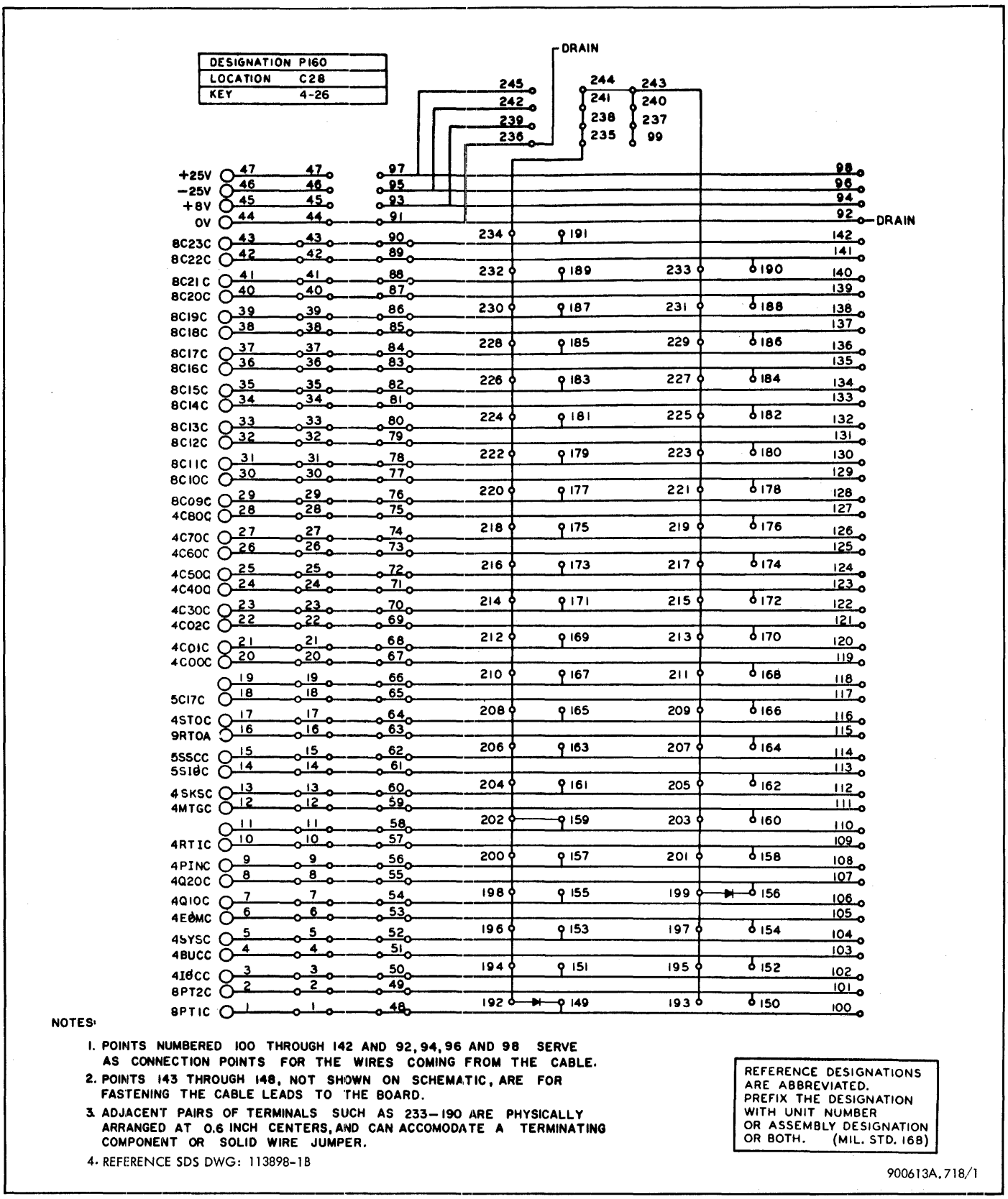


Figure 7-3. Plug Module Cable Assembly P157/P158 Schematic Diagram (Sheet 2 of 2 sheets)



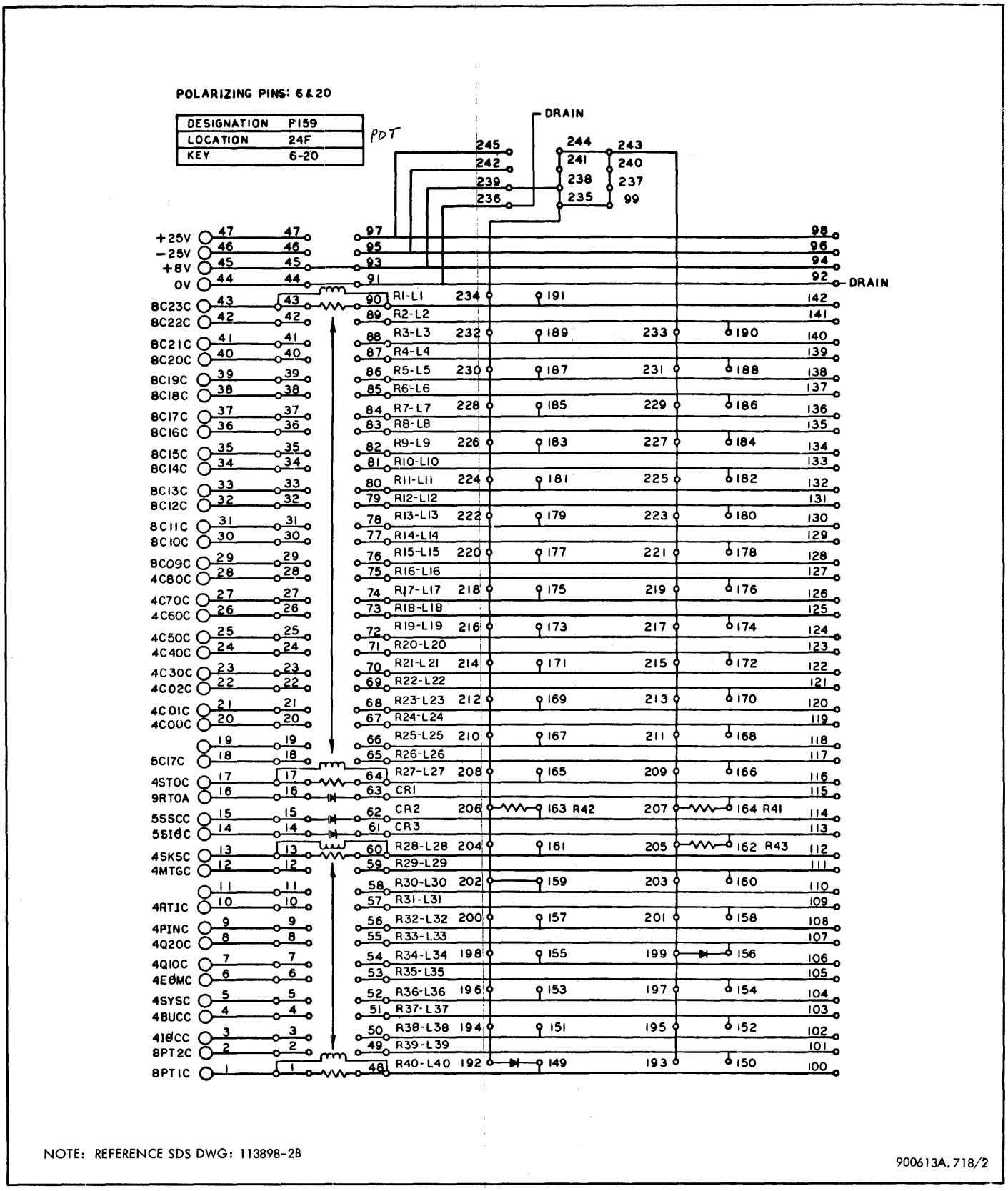
NOTES:

1. POINTS NUMBERED 100 THROUGH 142 AND 92, 94, 96 AND 98 SERVE AS CONNECTION POINTS FOR THE WIRES COMING FROM THE CABLE.
2. POINTS 143 THROUGH 148, NOT SHOWN ON SCHEMATIC, ARE FOR FASTENING THE CABLE LEADS TO THE BOARD.
3. ADJACENT PAIRS OF TERMINALS SUCH AS 233–190 ARE PHYSICALLY ARRANGED AT 0.6 INCH CENTERS, AND CAN ACCOMODATE A TERMINATING COMPONENT OR SOLID WIRE JUMPER.
4. REFERENCE SDS DWG: 113898-1B

REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH. (MIL. STD. 168)

900613A.718/1

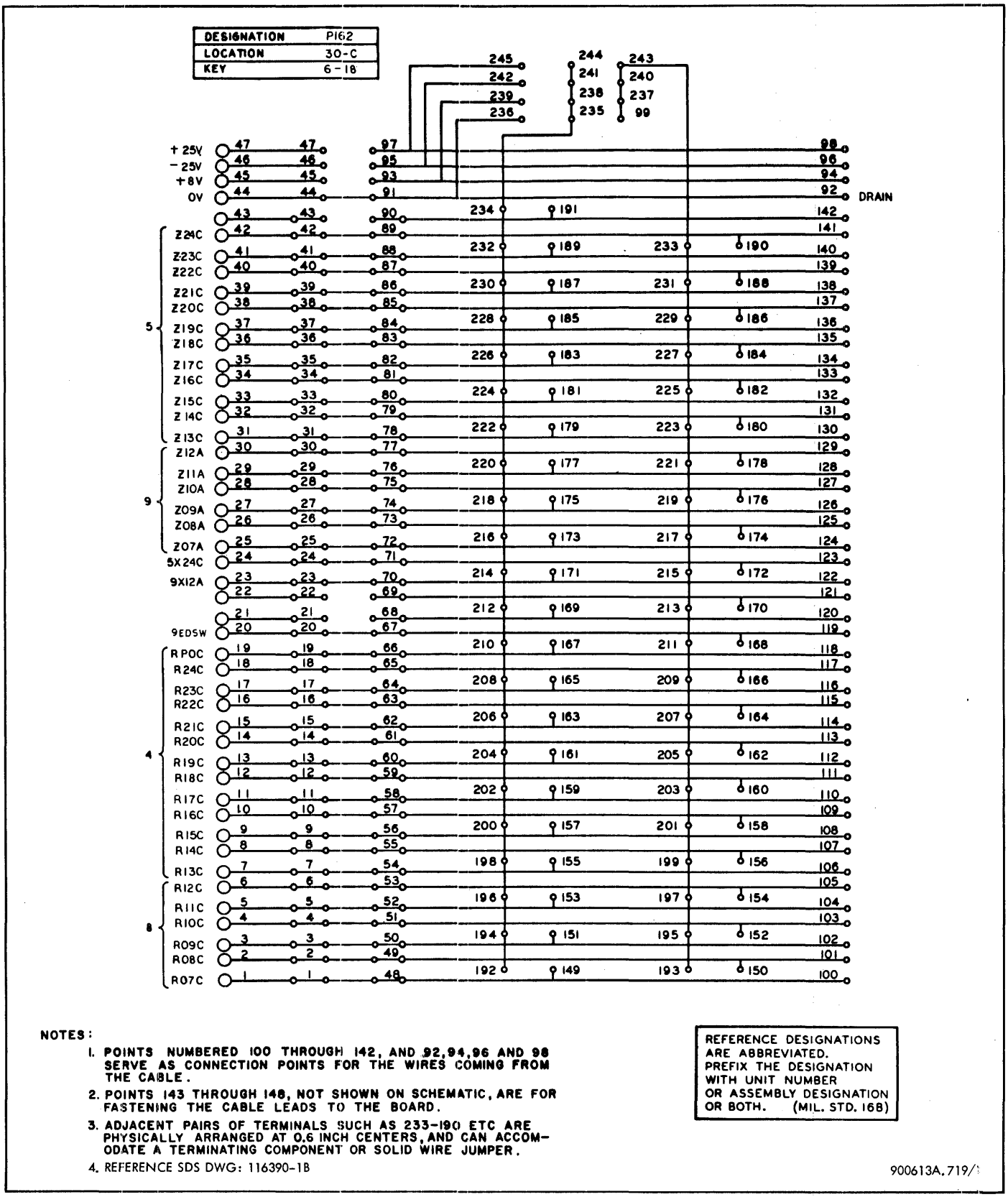
Figure 7-4. Plug Module Cable Assembly P159/P160 Schematic Diagram (Sheet 1 of 2 sheets)



NOTE: REFERENCE SDS DWG: 113898-2B

900613A.718/2

Figure 7-4. Plug Module Cable Assembly P159/P160 Schematic Diagram (Sheet 2 of 2 sheets)



NOTES:

1. POINTS NUMBERED 100 THROUGH 142, AND 92,94,96 AND 98 SERVE AS CONNECTION POINTS FOR THE WIRES COMING FROM THE CABLE.
2. POINTS 143 THROUGH 148, NOT SHOWN ON SCHEMATIC, ARE FOR FASTENING THE CABLE LEADS TO THE BOARD.
3. ADJACENT PAIRS OF TERMINALS SUCH AS 233-190 ETC ARE PHYSICALLY ARRANGED AT 0.6 INCH CENTERS, AND CAN ACCOMODATE A TERMINATING COMPONENT OR SOLID WIRE JUMPER.
4. REFERENCE SDS DWG: 116390-1B

REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH. (MIL. STD. 168)

900613A.719/1

Figure 7-5. Plug Module Cable Assembly P161/P162 Schematic Diagram (Sheet 1 of 2 sheets)

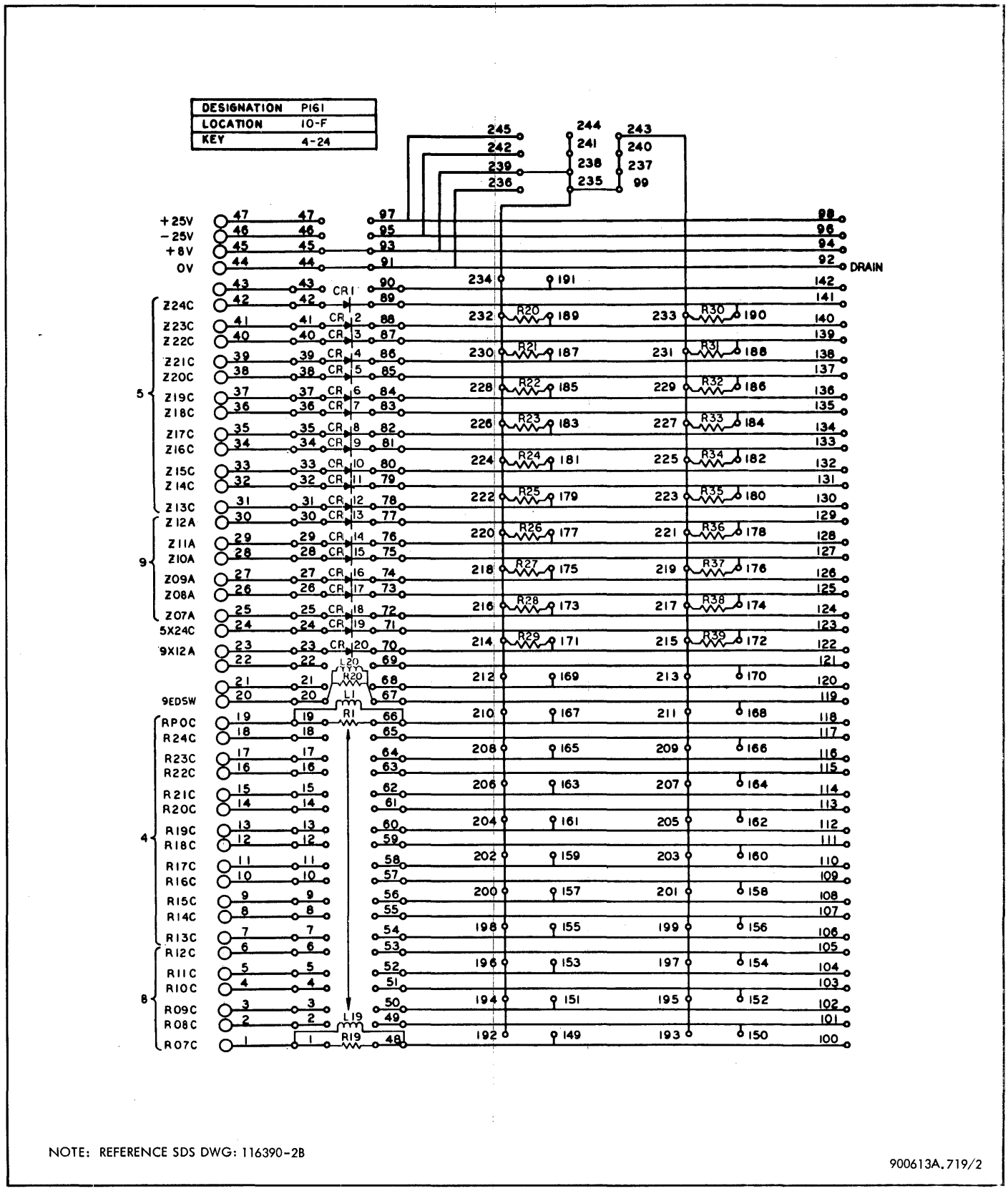
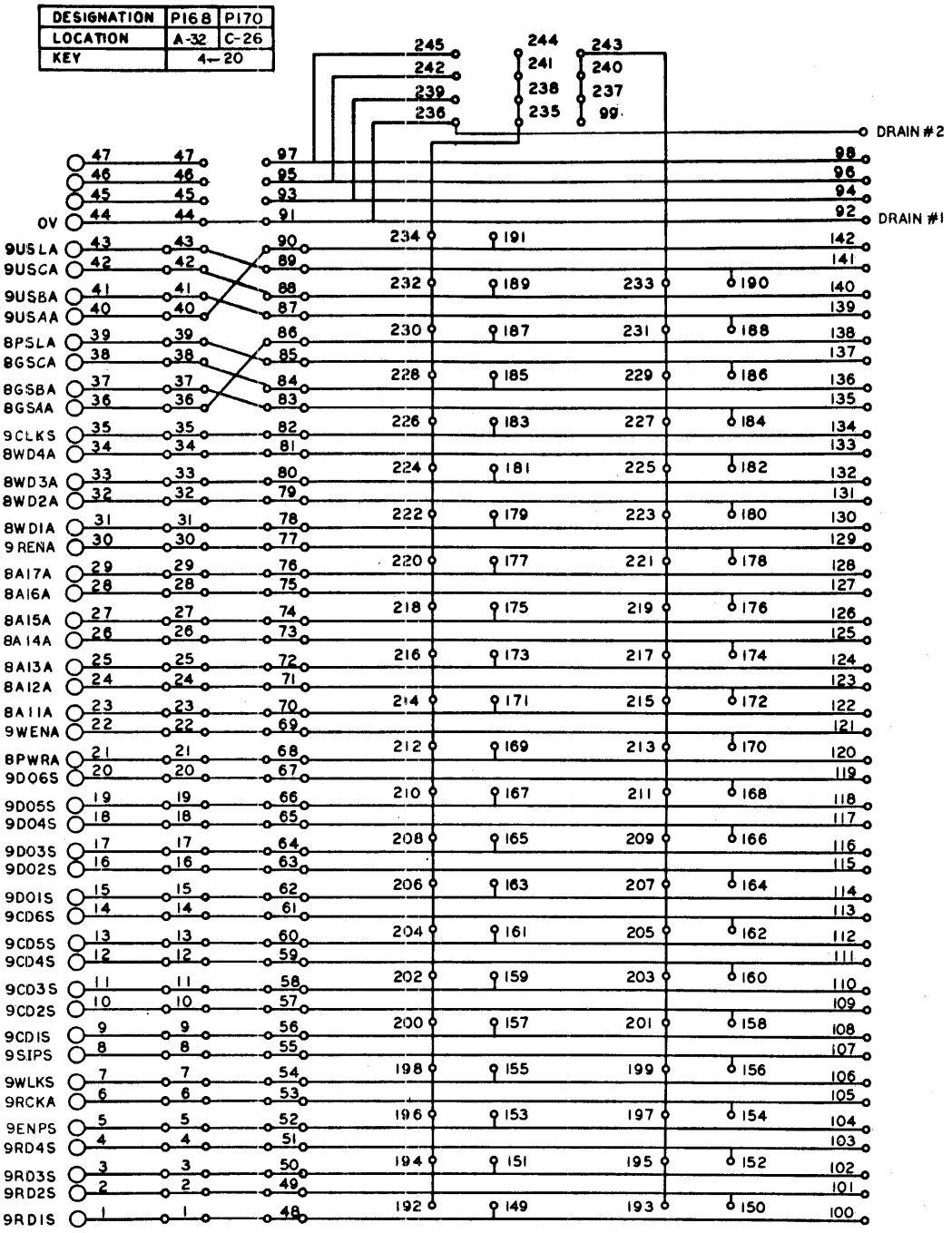


Figure 7-5. Plug Module Cable Assembly P161/P162 Schematic Diagram (Sheet 2 of 2 sheets)



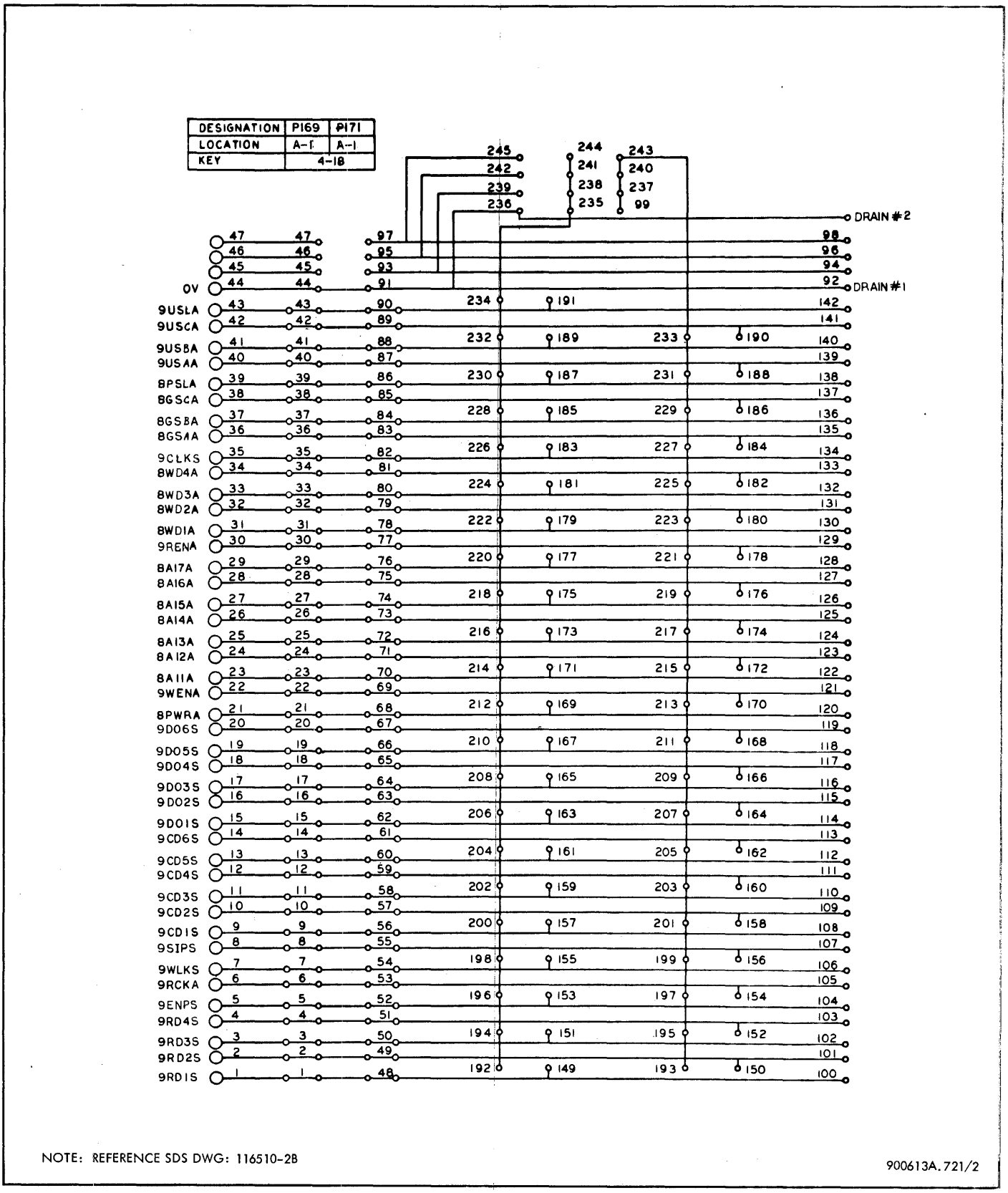
NOTES, UNLESS OTHERWISE SPECIFIED

1. POINTS NUMBERED 100 THROUGH 142, SERVE AS CONNECTION POINTS FOR THE WIRES COMING FROM THE CABLE.
2. POINTS 143 THROUGH 148, NOT SHOWN ON SCHEMATIC, ARE FOR FASTENING THE CABLE LEADS TO THE BOARD.
3. ADJACENT PAIRS TO TERMINALS SUCH AS 233-190 ETC ARE PHYSICALLY ARRANGED AT 0.6 INCH CENTERS, AND CAN ACCOMODATE A TERMINATING COMPONENT OR SOLID WIRE JUMPER.
4. POINT 92 SERVES AS TERMINATION FOR THE DRAIN WIRE FOR THE 30 CONDUCTOR CABLE, AND POINT 236 SERVES AS TERMINATION FOR THE DRAIN WIRE OF THE 14 CONDUCTOR CABLE.
5. REFERENCE SDS DWG: 116510-1B

REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH. (MIL. STD. 16B)

900613A.721/1

Figure 7-6. Plug Module Cable Assembly P170/P171 Schematic Diagram (Sheet 1 of 2 sheets)



NOTE: REFERENCE SDS DWG: 116510-2B

900613A.721/2

Figure 7-6. Plug Module Cable Assembly P170/P171 Schematic Diagram (Sheet 2 of 2 sheets)

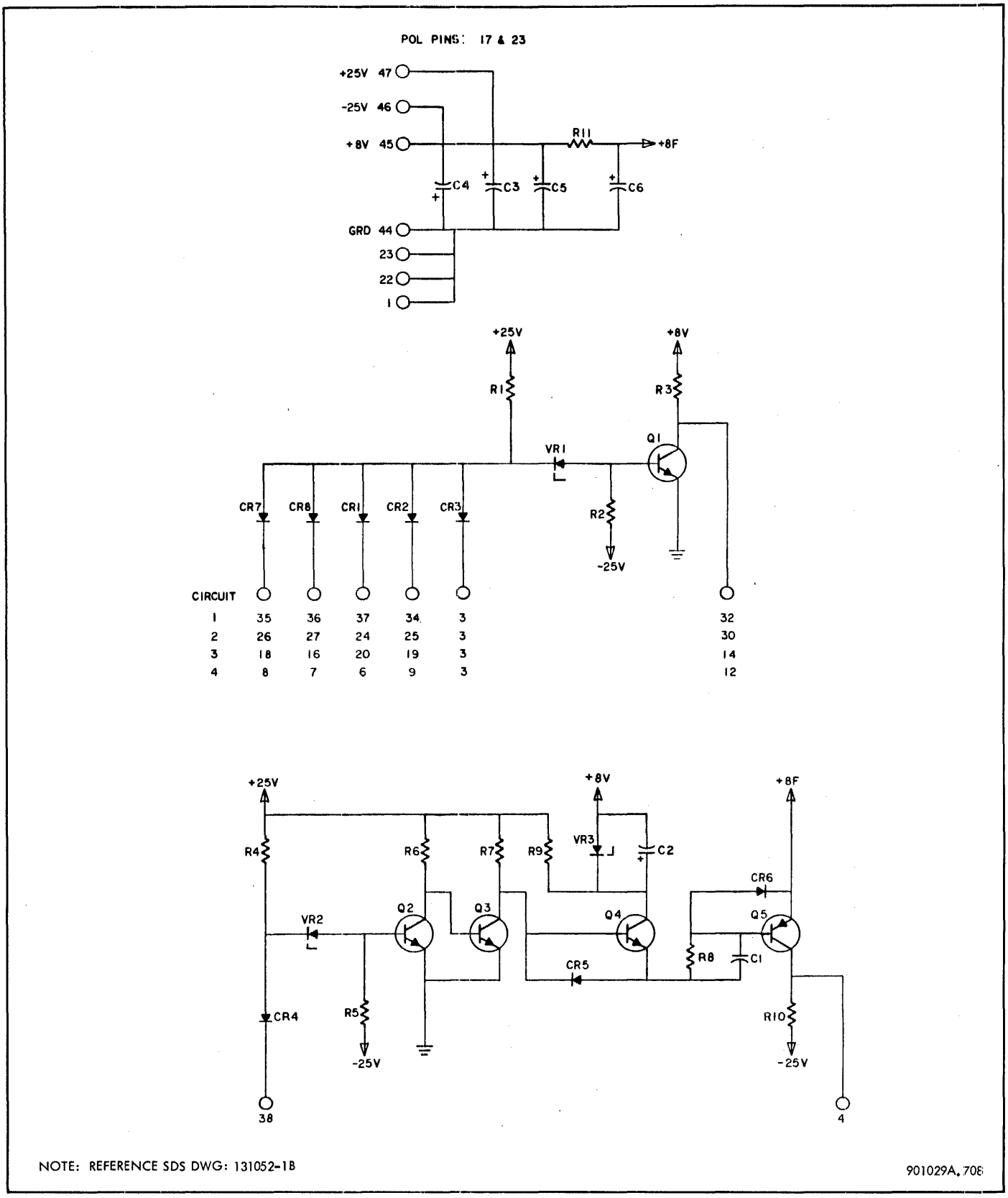


Figure 7-7. Read Input Control AK61 Schematic Diagram

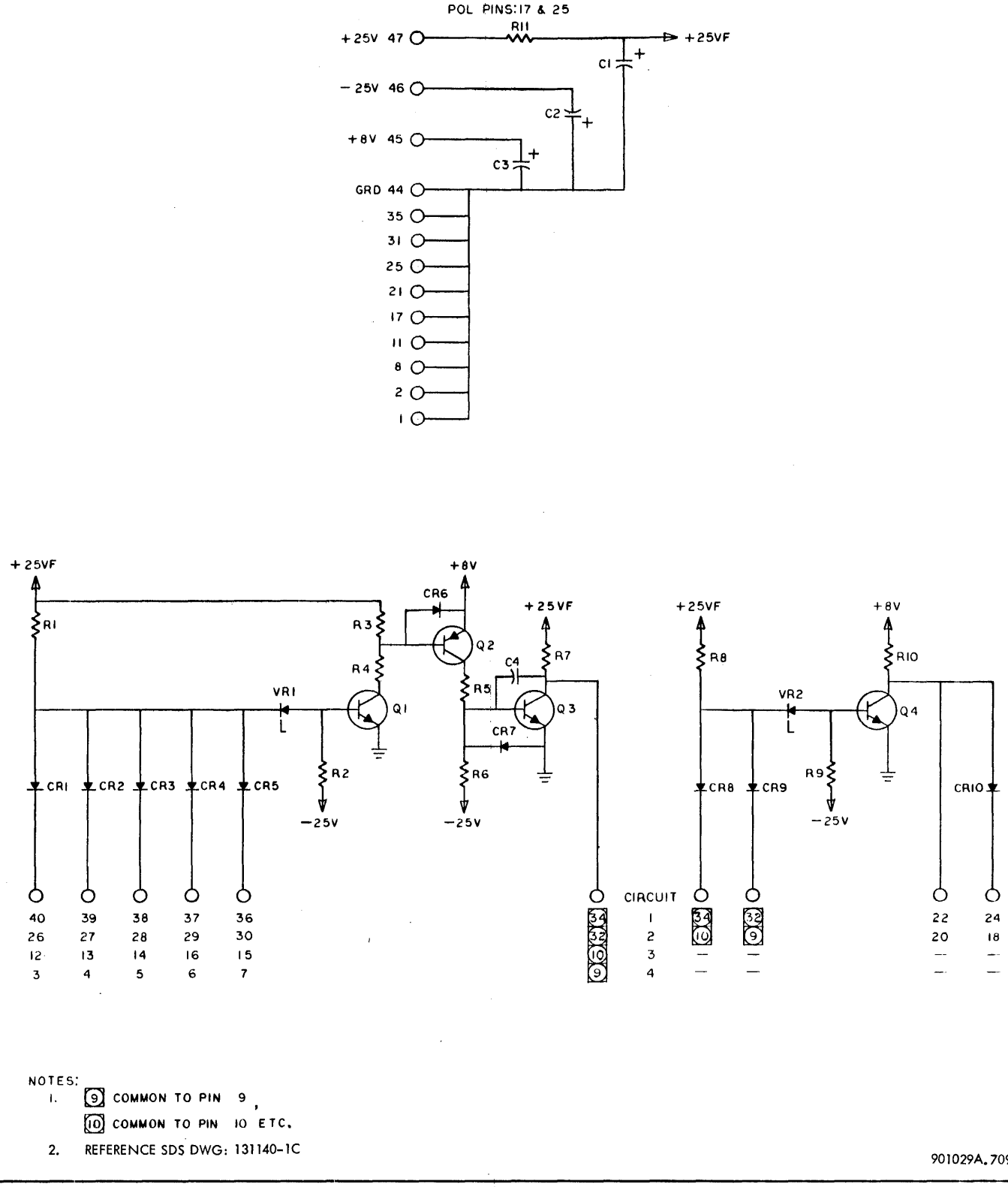
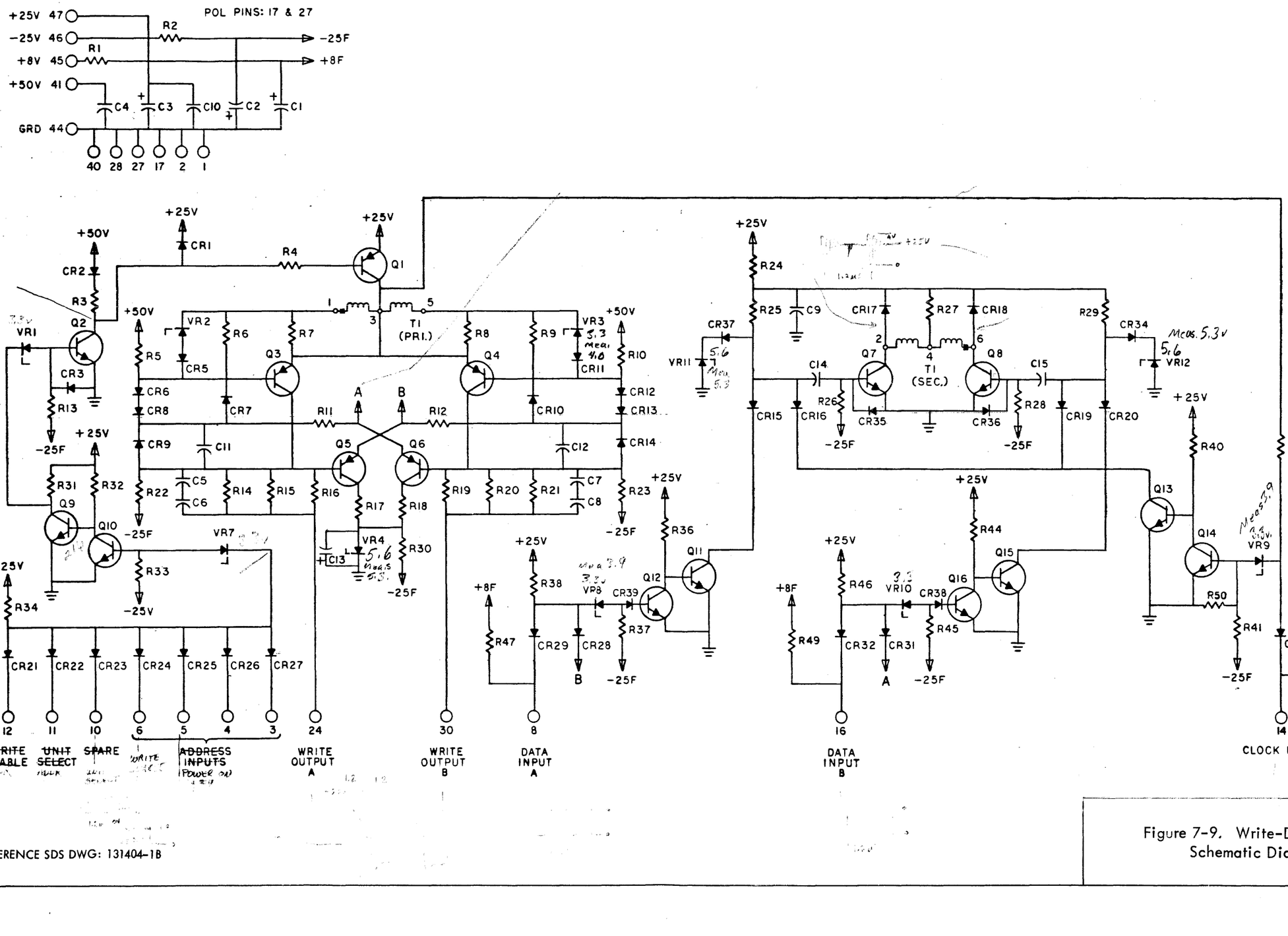


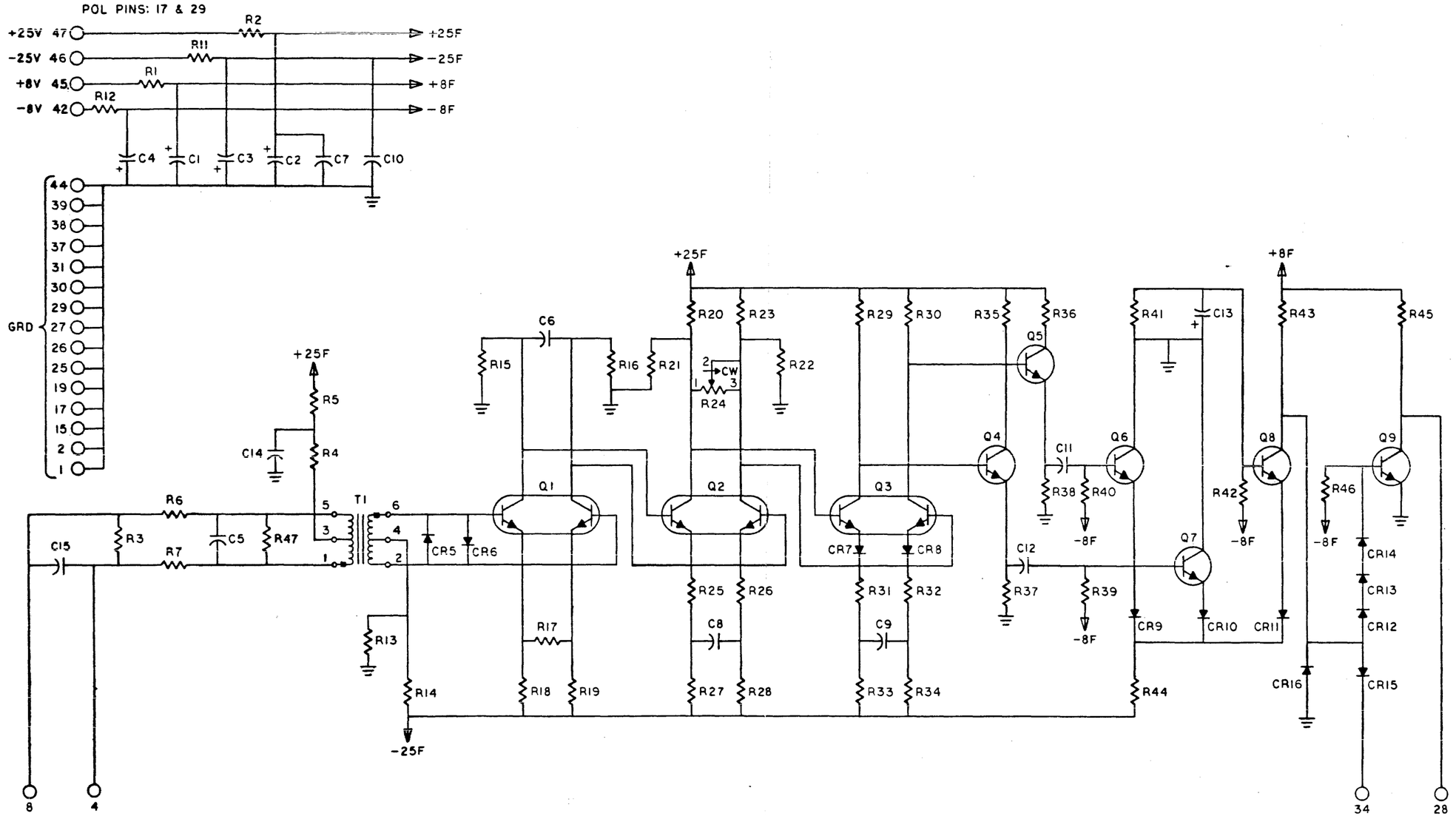
Figure 7-8. Y-Select AK62 Schematic Diagram



NOTE: REFERENCE SDS DWG: 131404-1B

Figure 7-9. Write-Driver AK63 Schematic Diagram

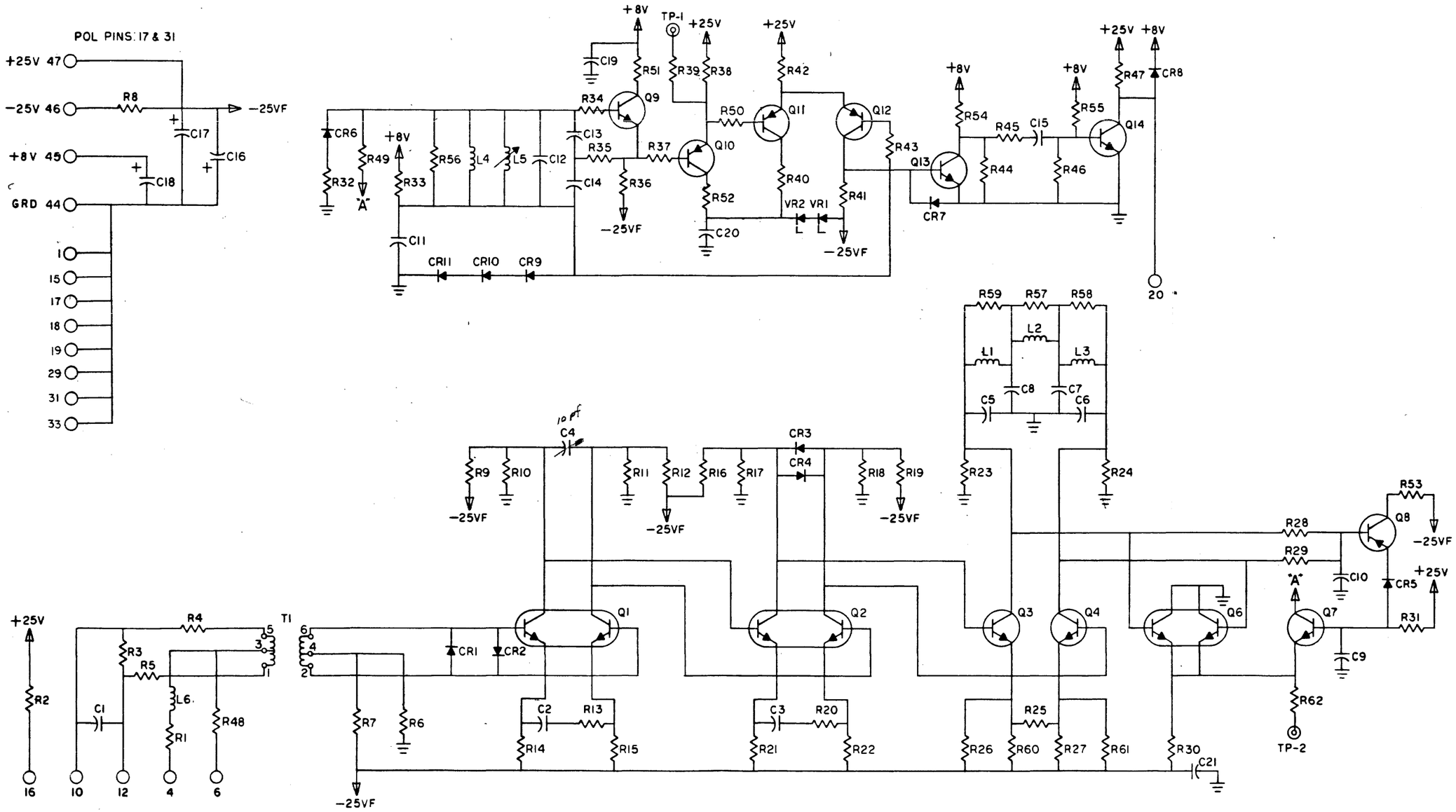
901029A.710



NOTE: REFERENCE SDS DWG: 131244-1C

Figure 7-10. Index/Sector Amplifier AK64 Schematic Diagram

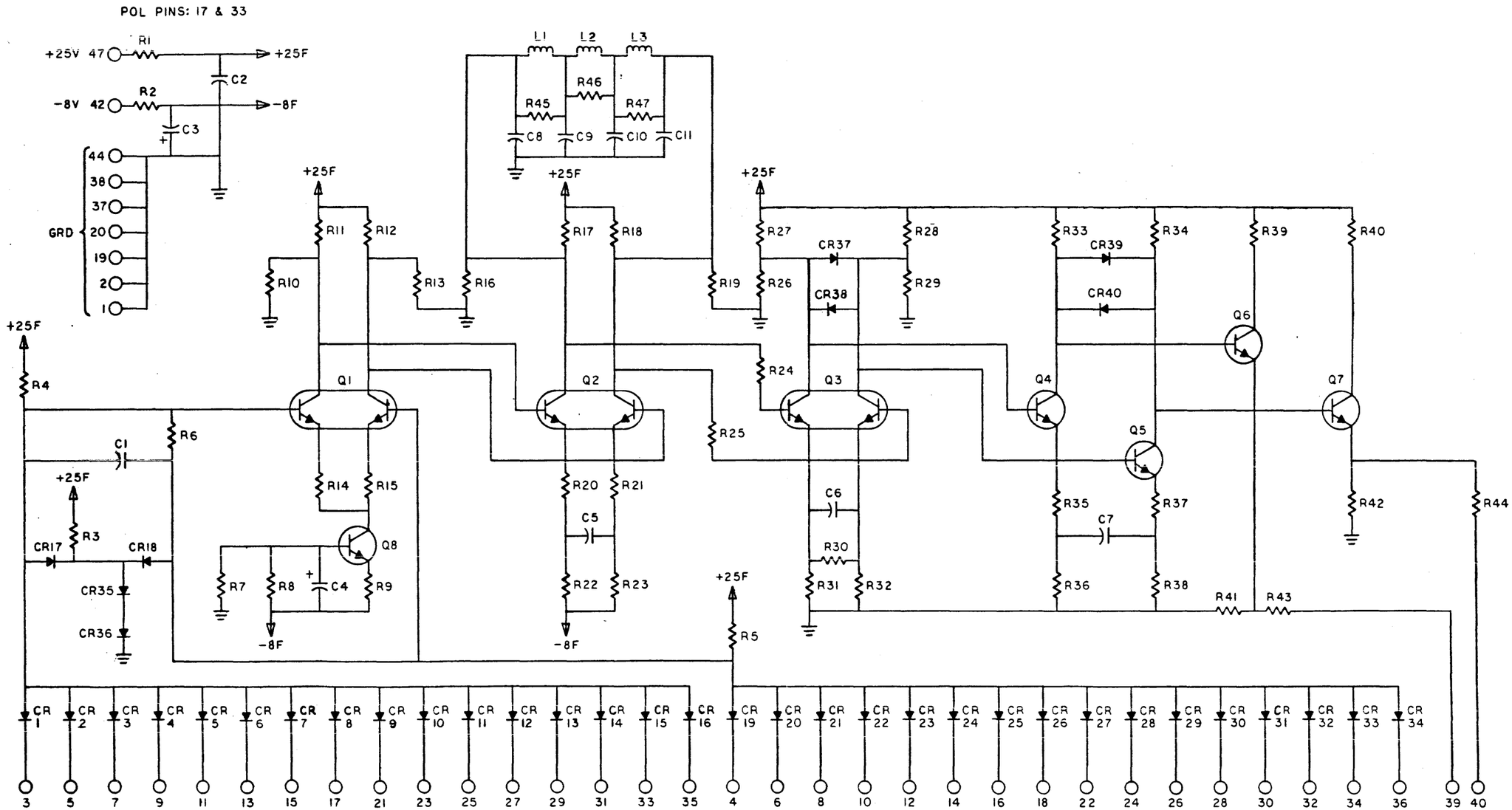
901029A.711



NOTE: REFERENCE SDS DWG: 131342-1D

Figure 7-11. Write Clock Amplifier AK65 Schematic Diagram

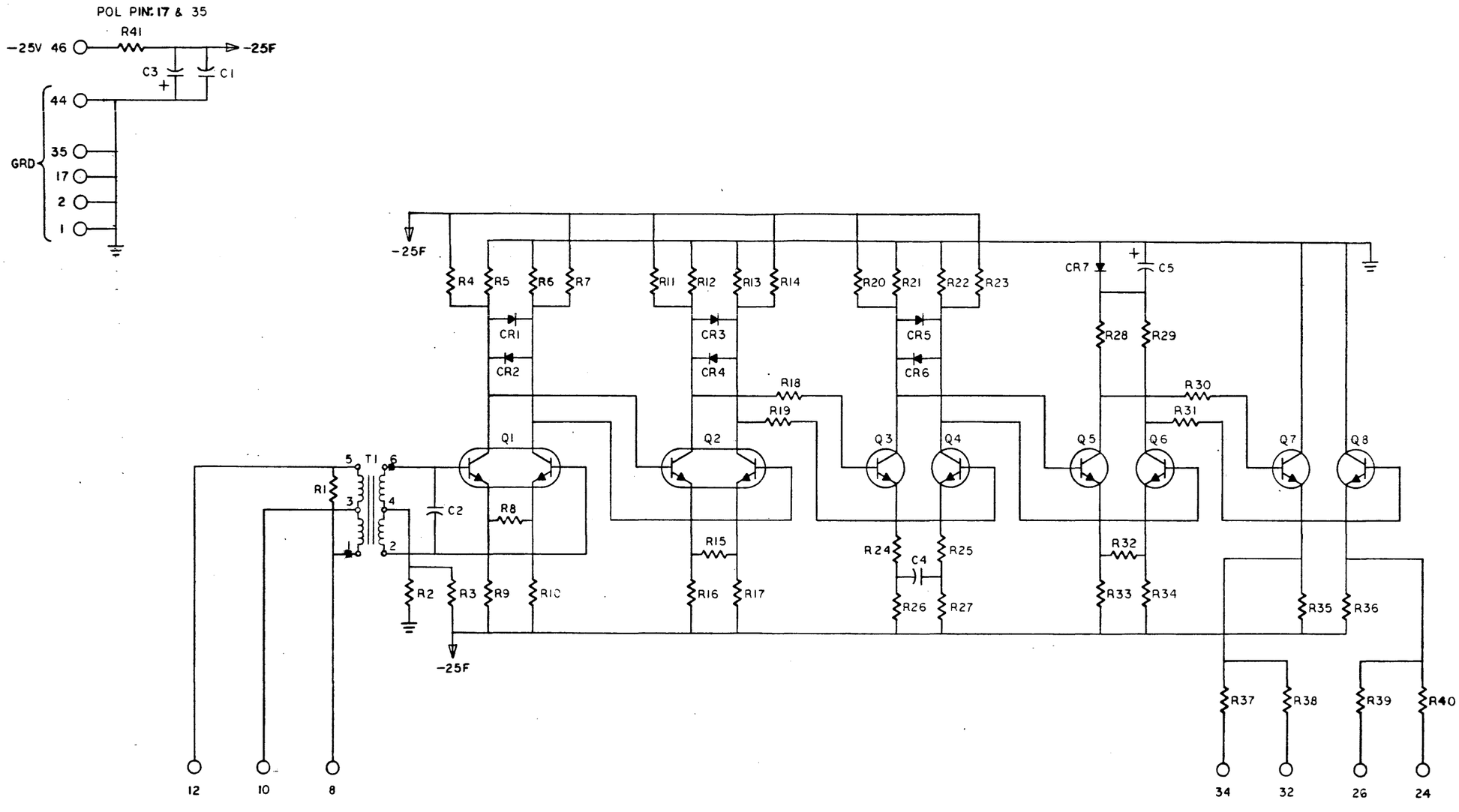
901029A.712



NOTE: REFERENCE SDS DWG: 131384-1B

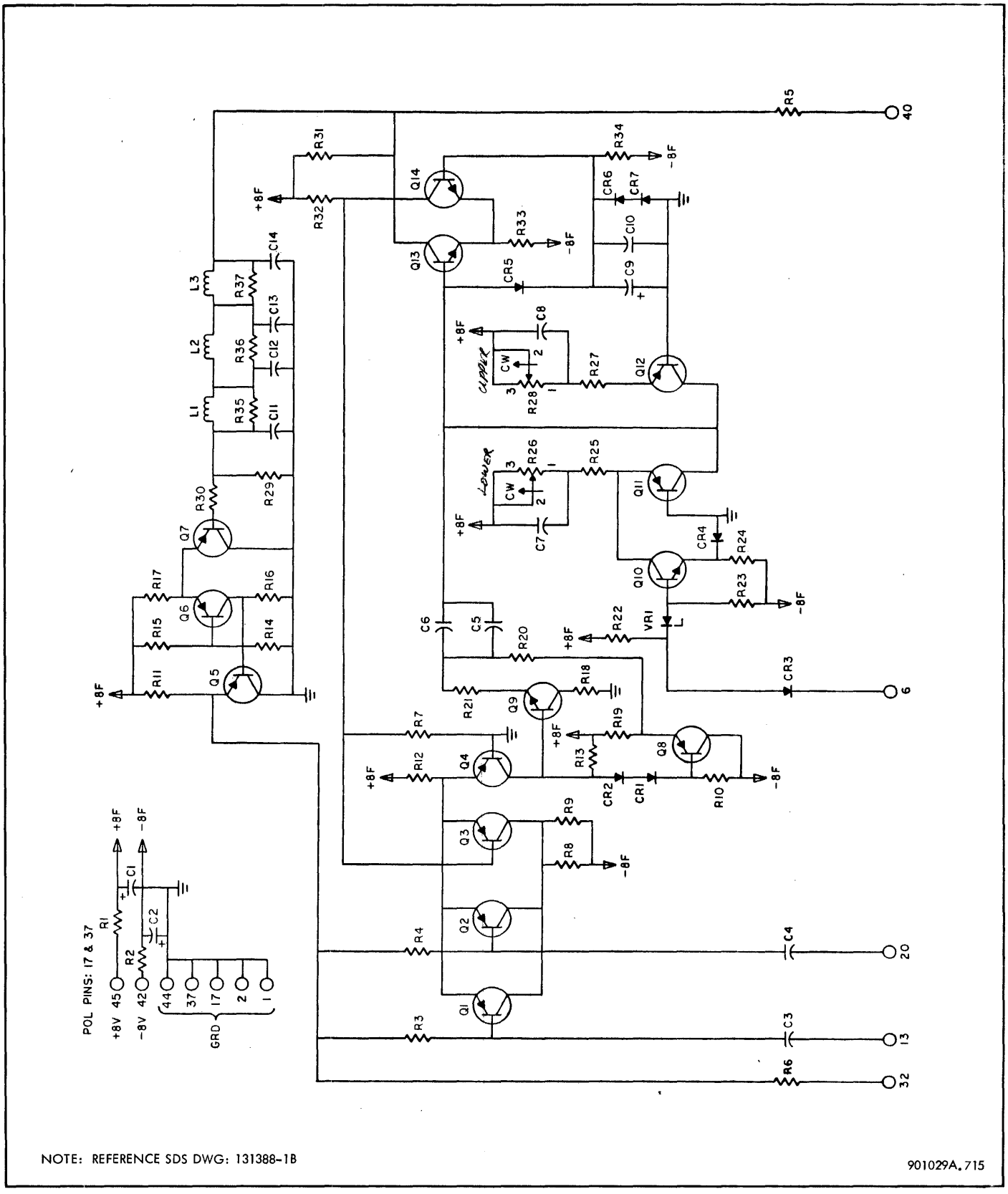
Figure 7-12. Read Preamplifier HK73 Schematic Diagram

901029A.713



NOTE: REFERENCE SDS DWG: 131145-1B

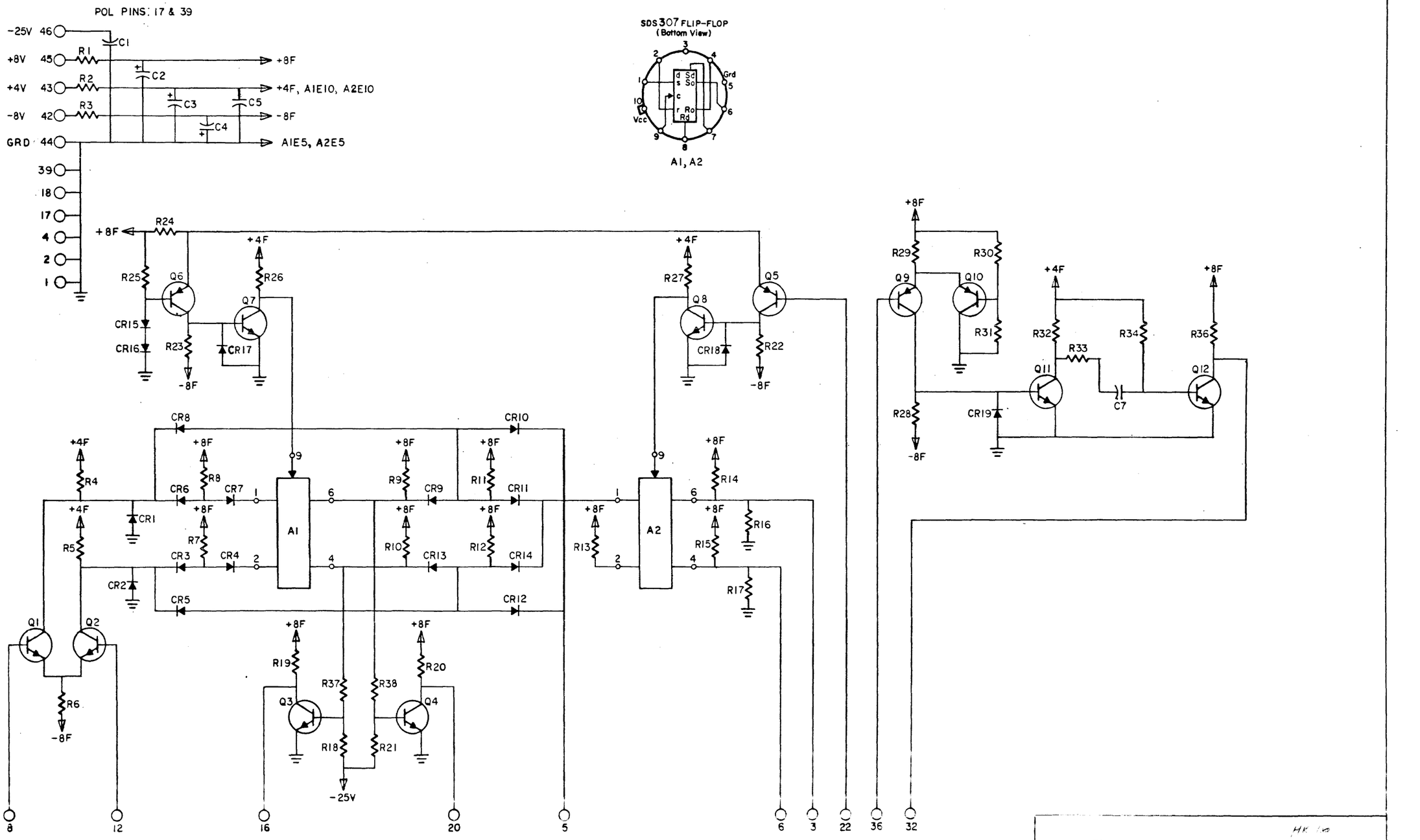
Figure 7-13. Limiter HK74
Schematic Diagram
901029A.714



NOTE: REFERENCE SDS DWG: 131388-1B

901029A.715

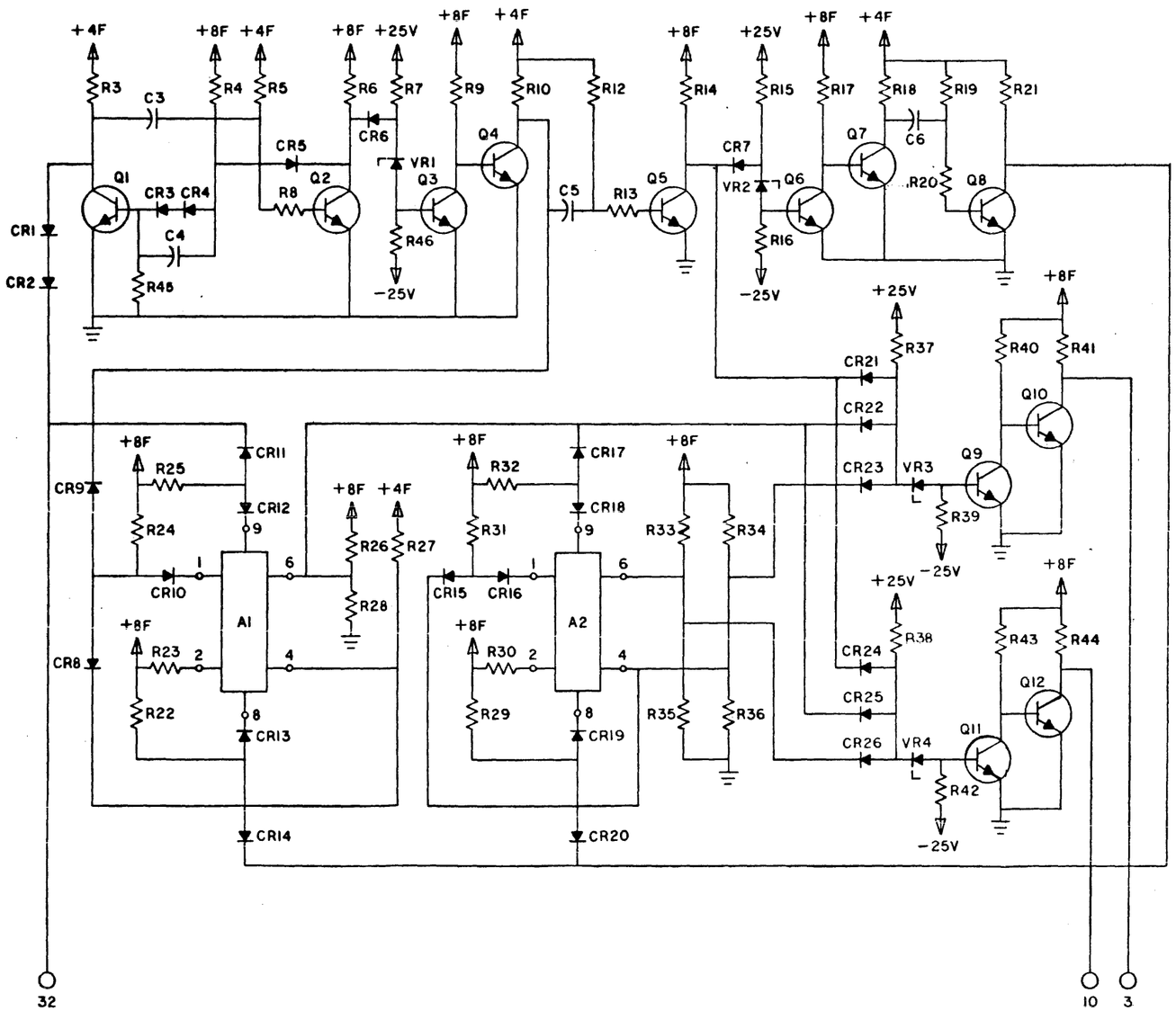
Figure 7-14. Clock Discriminator HK75 Schematic Diagram

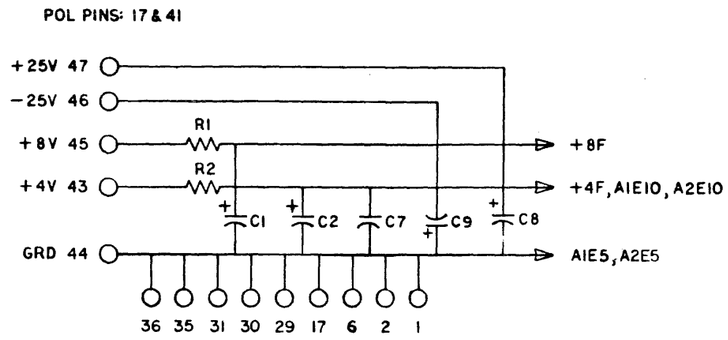


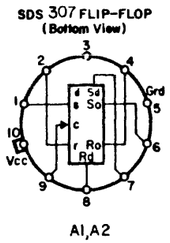
NOTE: REFERENCE SDS DWG: 131377-1B

Figure 7-15. Data Decoder ~~HK75~~
Schematic Diagram

901029A.716







A1, A2

NOTE: REFERENCE SDS DWG: 131239-1E

Figure 7-16. Index/Sector Decoder HK77 Schematic Diagram

901029A.717

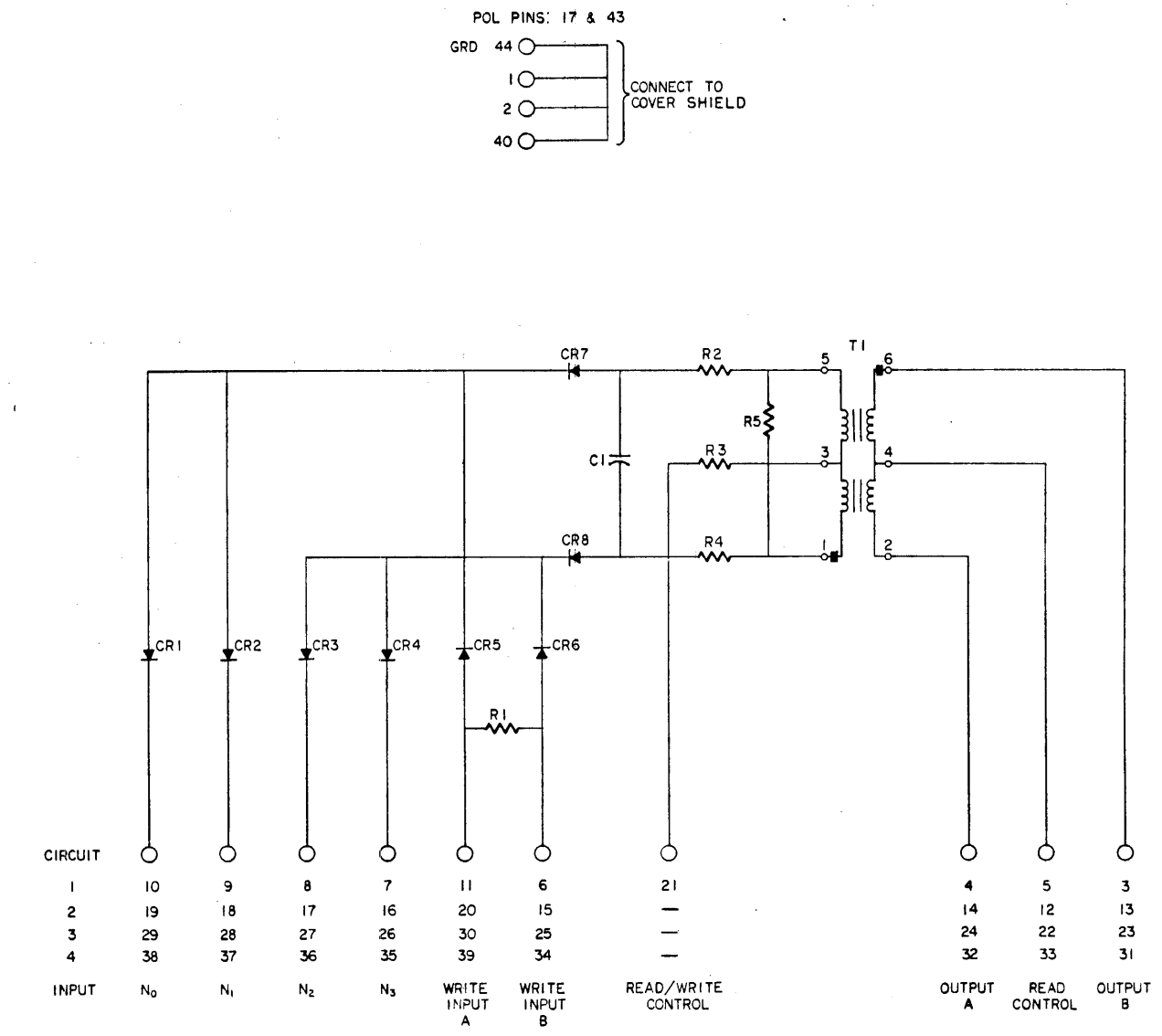
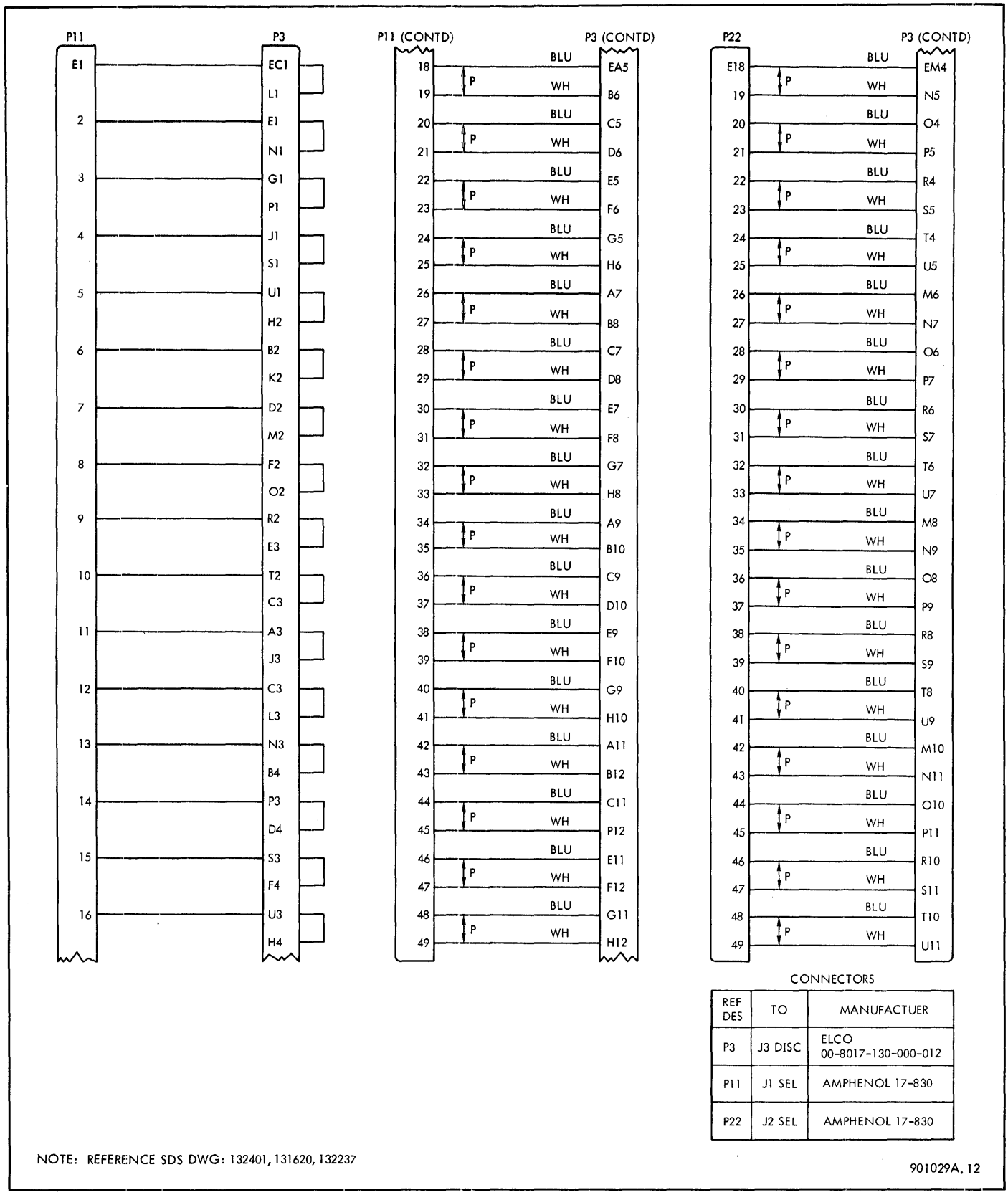


Figure 7-17. Read/Write Decoder NK59 Schematic Diagram



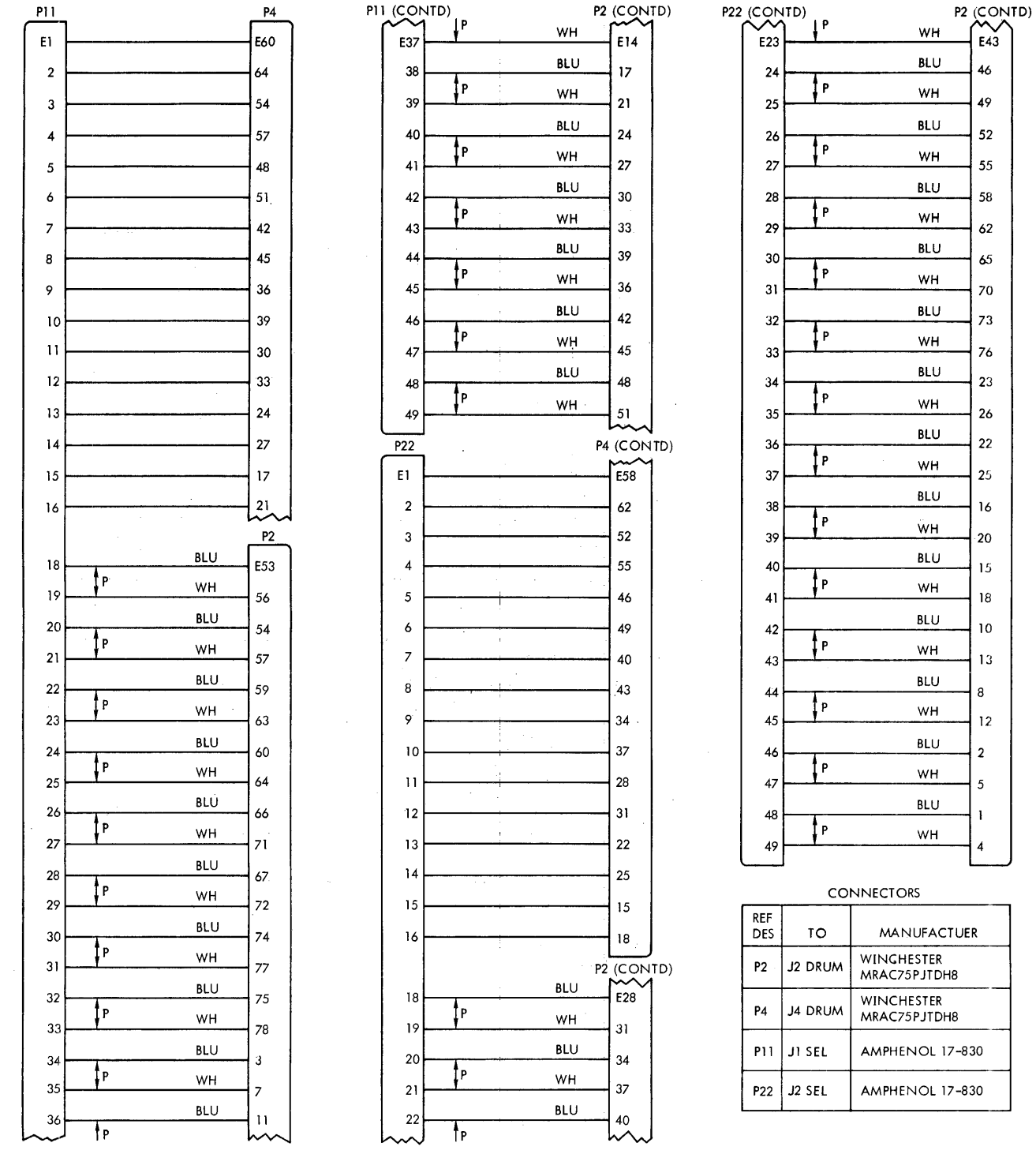
CONNECTORS

REF DES	TO	MANUFACTUER
P3	J3 DISC	ELCO 00-8017-130-000-012
P11	J1 SEL	AMPHENOL 17-830
P22	J2 SEL	AMPHENOL 17-830

NOTE: REFERENCE SDS DWG: 132401, 131620, 132237

901029A.12

Figure 7-18. Disc Matrix Cable Assembly Schematic Diagram



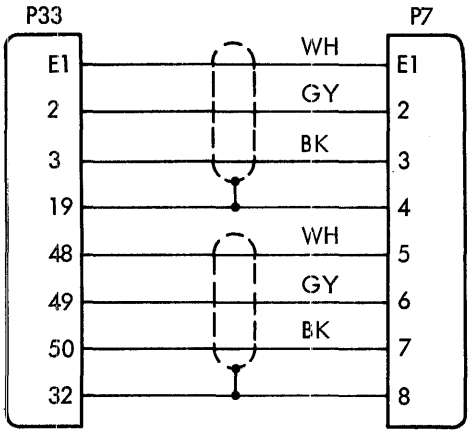
CONNECTORS

REF DES	TO	MANUFACTUER
P2	J2 DRUM	WINCHESTER MRAC75PJTDH8
P4	J4 DRUM	WINCHESTER MRAC75PJTDH8
P11	J1 SEL	AMPHENOL 17-830
P22	J2 SEL	AMPHENOL 17-830

NOTE: REFERENCE SDS DWG: 132396, 131623, 132236

901029A. 10

Figure 7-19. Drum Matrix Cable Assembly Schematic Diagram

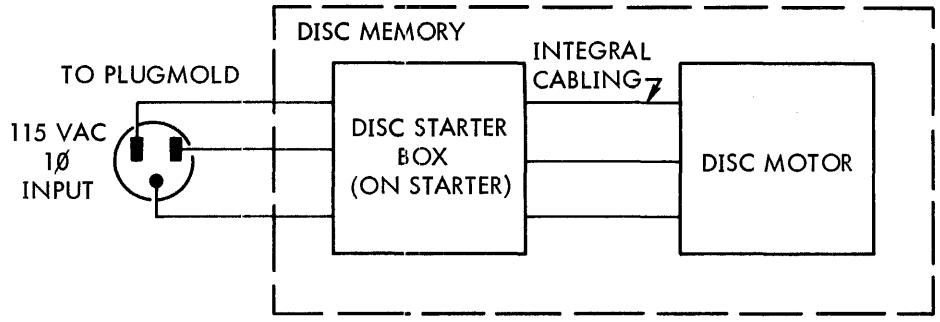


CONNECTORS

REF DES	TO	MANUFACTURER
P7	J7 DISC	AMPHENOL 17-20150-1
P33	J3 SEL	AMPHENOL 17-830

CLOCK CABLE

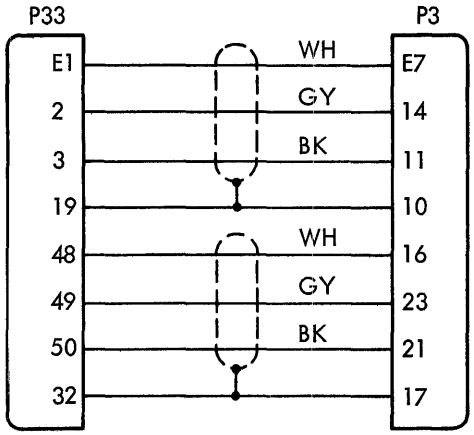
POWER CABLES



NOTE: THIS DRAWING WAS PREPARED FROM THE FOLLOWING ENGINEERING DRAWINGS: 132240, 132241

901029A.13

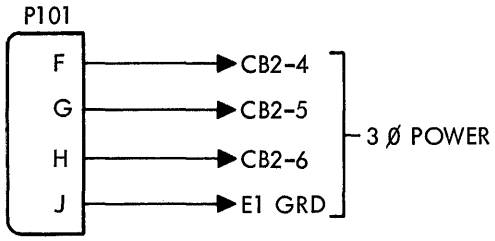
Figure 7-20. Disc Clock and Power Cables Schematic Diagram



CONNECTORS

REF DES	TO	MANUFACTURER
P3	J3/J5/J7 DRUM	WINCHESTER MBAC75PJTDH8
P33	J3 SEL	AMPHENOL 7-830

CLOCK CABLE



CONNECTOR

REF DES	TO	MANUFACTURER
P101	J1 DRUM	BENDIX PT06A-16-115(SR)

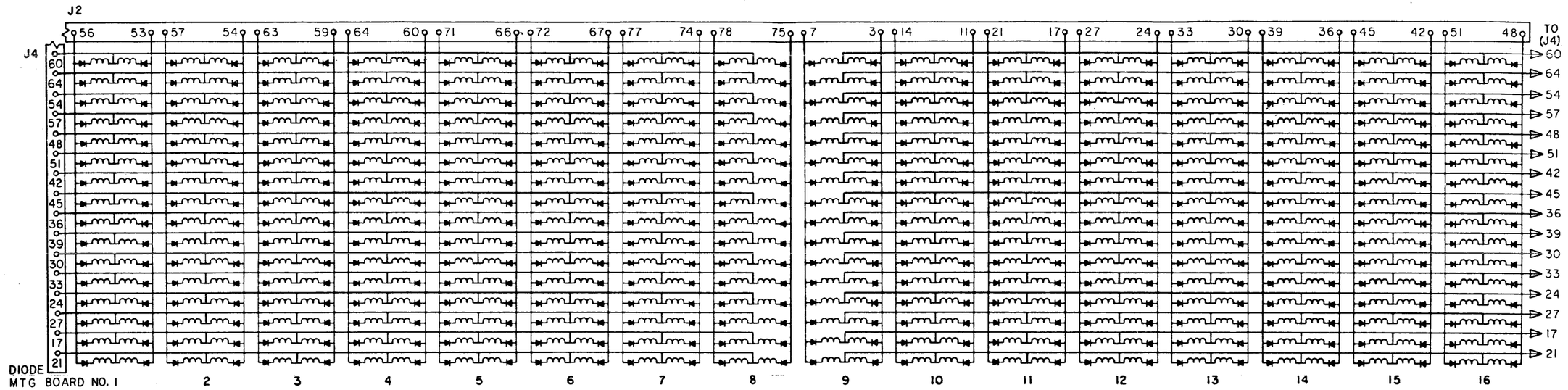
POWER CABLE

NOTE: REFERENCE SDS DWG: 131825, 132238, 132239

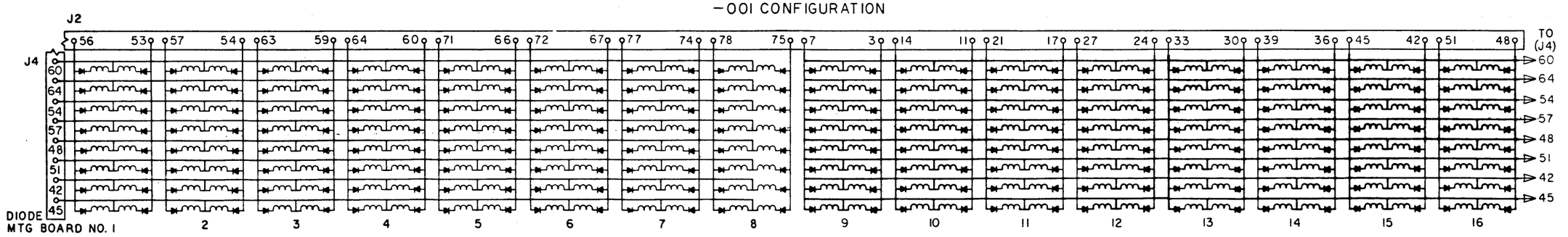
901029A.11

Figure 7-21. Drum Clock and Power Cables Schematic Diagram

-002 CONFIGURATION



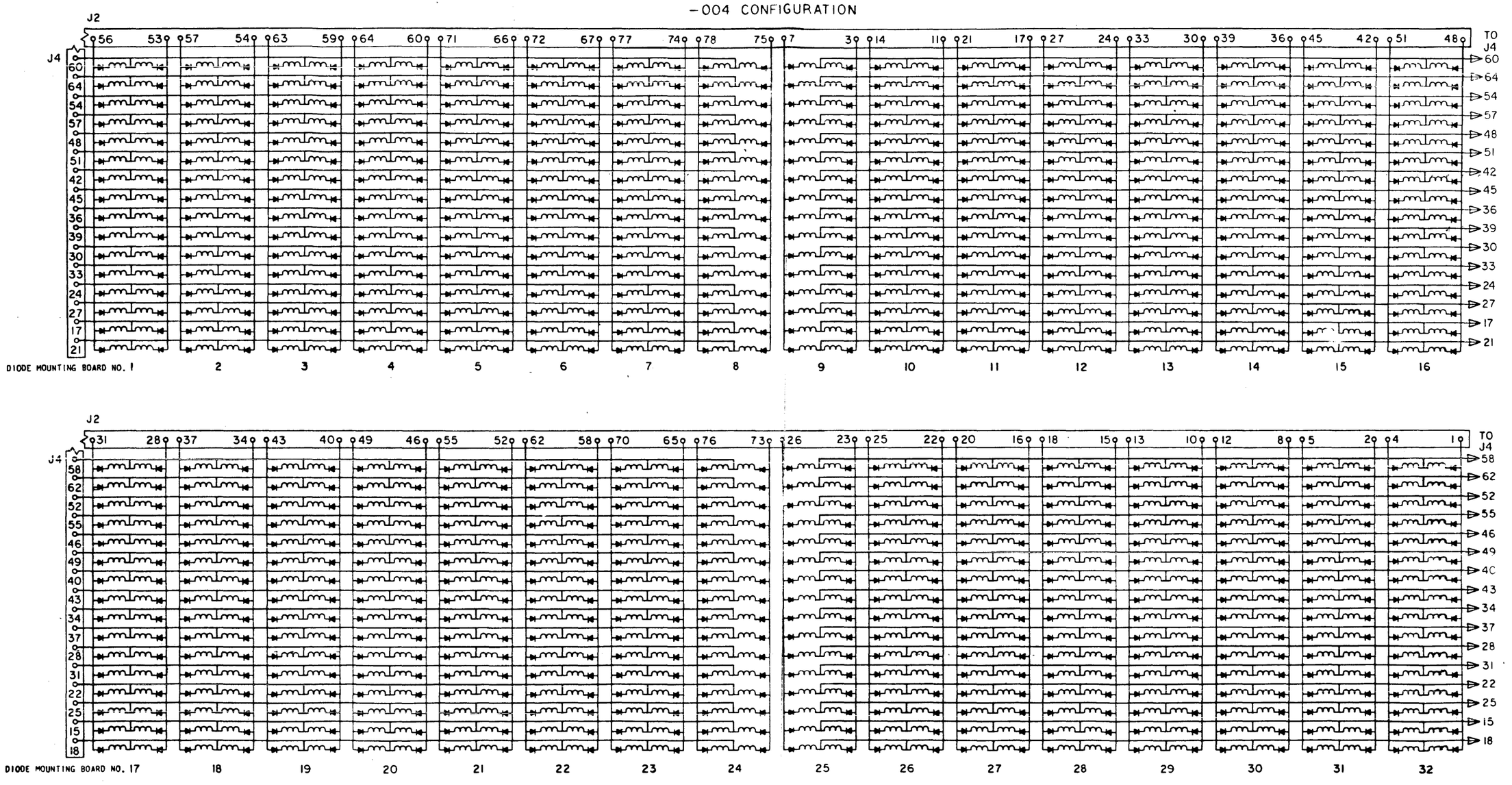
-001 CONFIGURATION



NOTE: REFERENCE SDS DWG: 130139-1B

Figure 7-22. Drum Memory Schematic Diagram (Sheet 1 of 2 sheets)

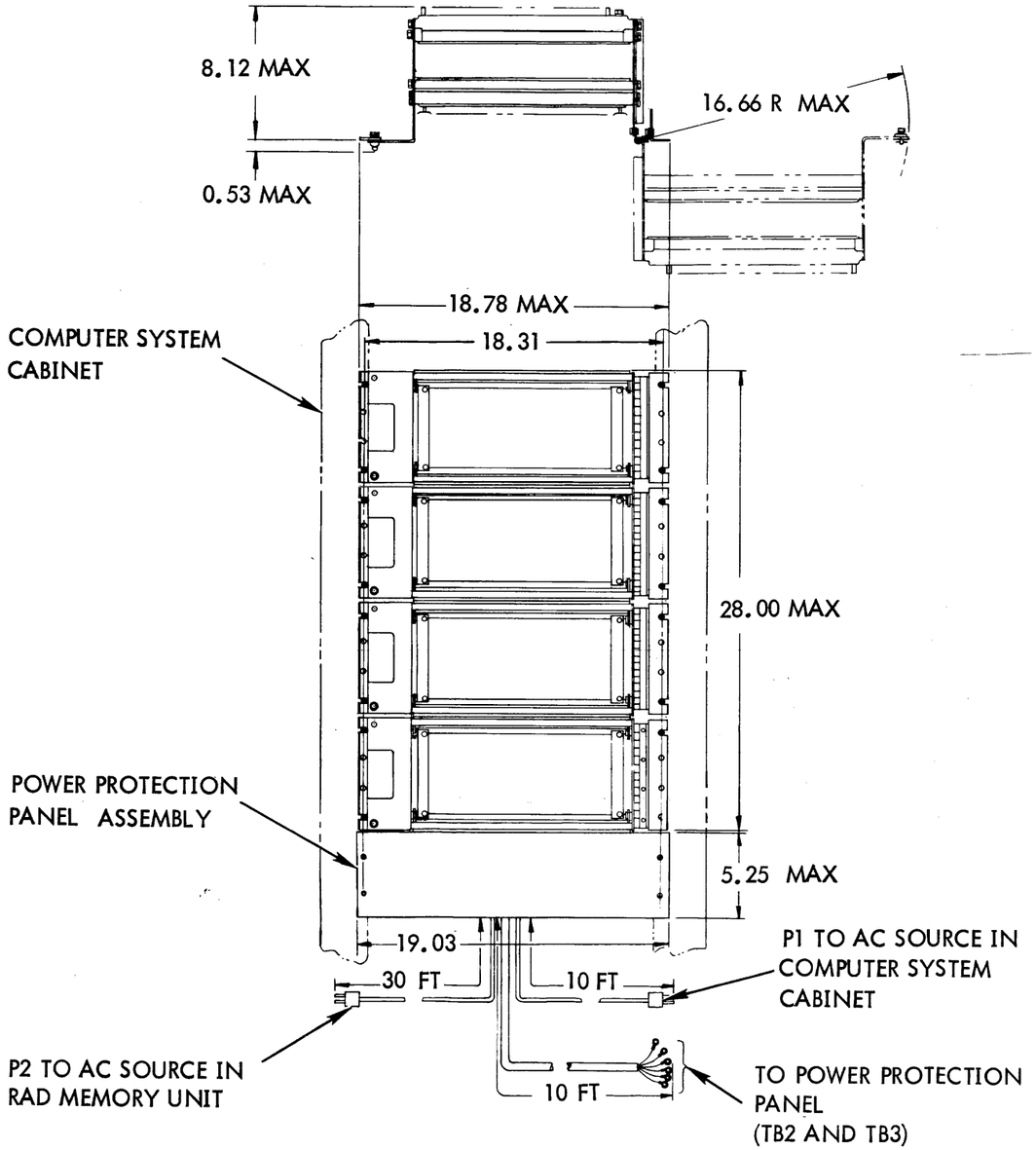
901029A, 701/1

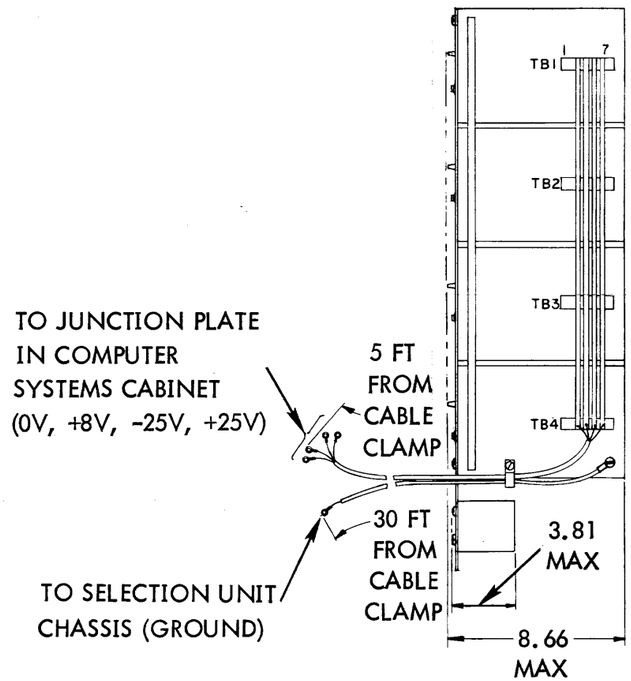


NOTE: REFERENCE SDS DWG: 130139-2B

Figure 7-22. Drum Memory Schematic Diagram (Sheet 2 of 2 sheets)

901029A.701/2

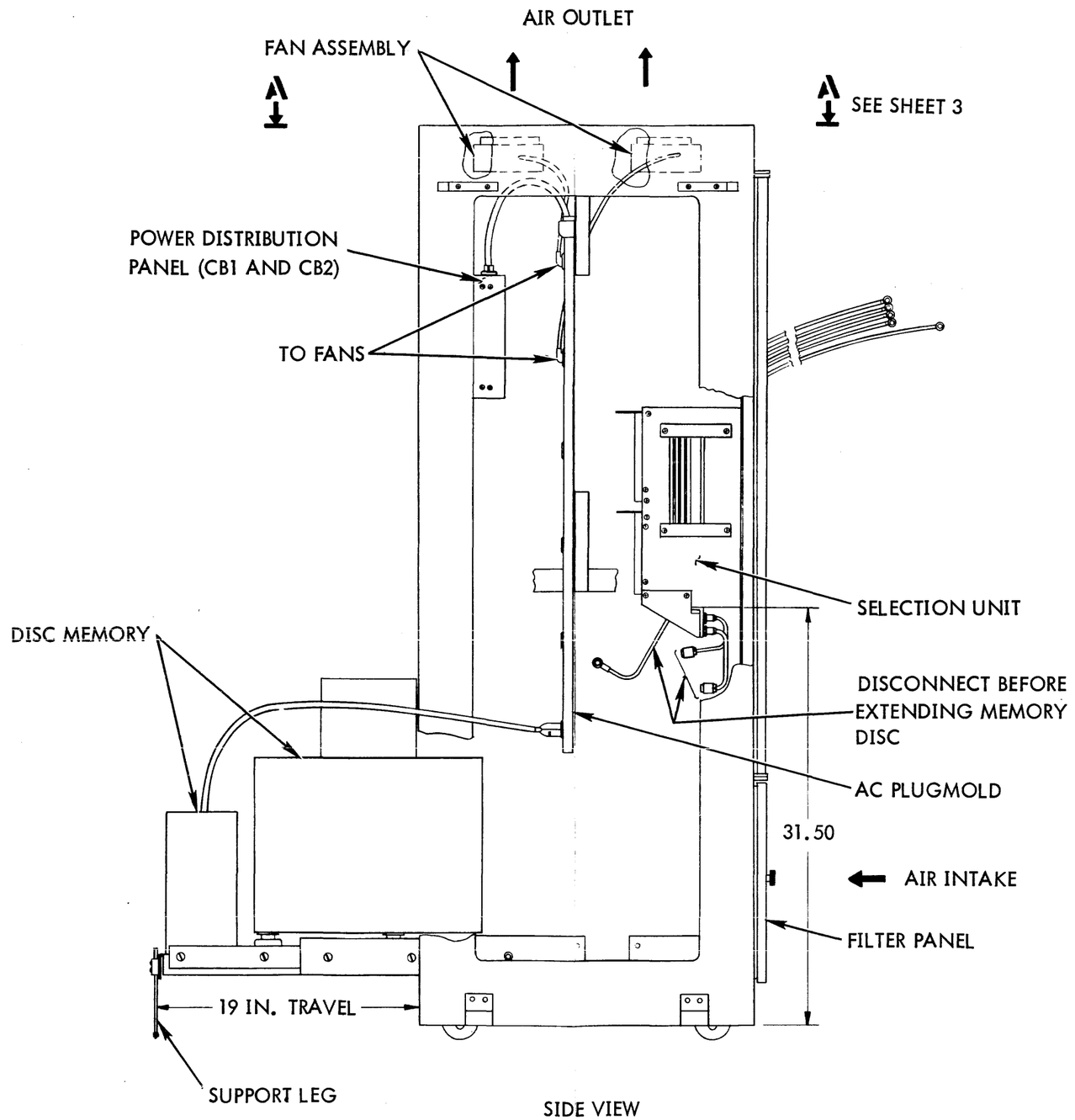




NOTE: REFERENCE SDS DWG: 131819-1A

Figure 7-23. Controller Installation Diagram

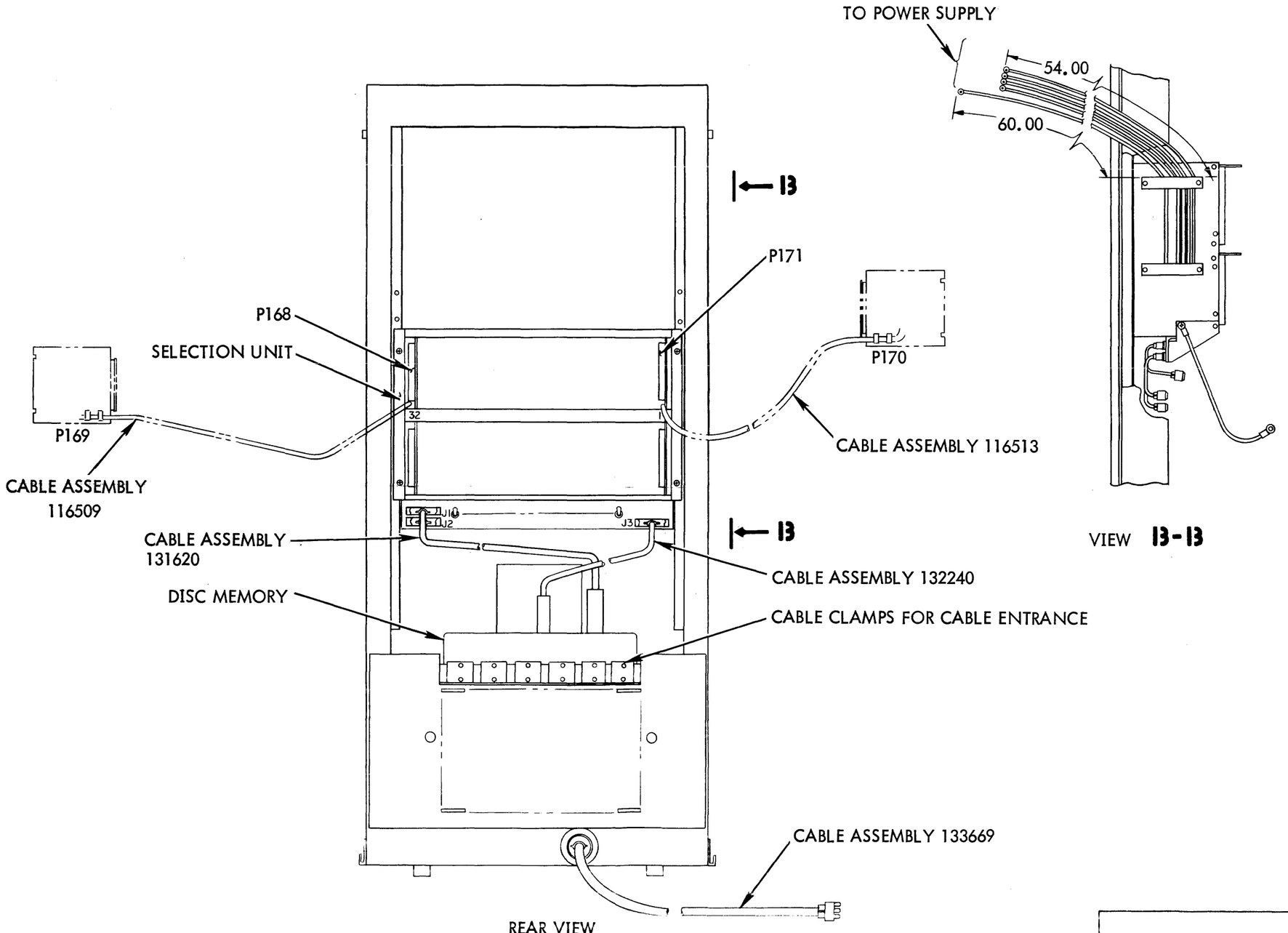
901029A.704



SIDE VIEW
FRONT DOOR OMITTED
DISC MEMORY EXTENDED

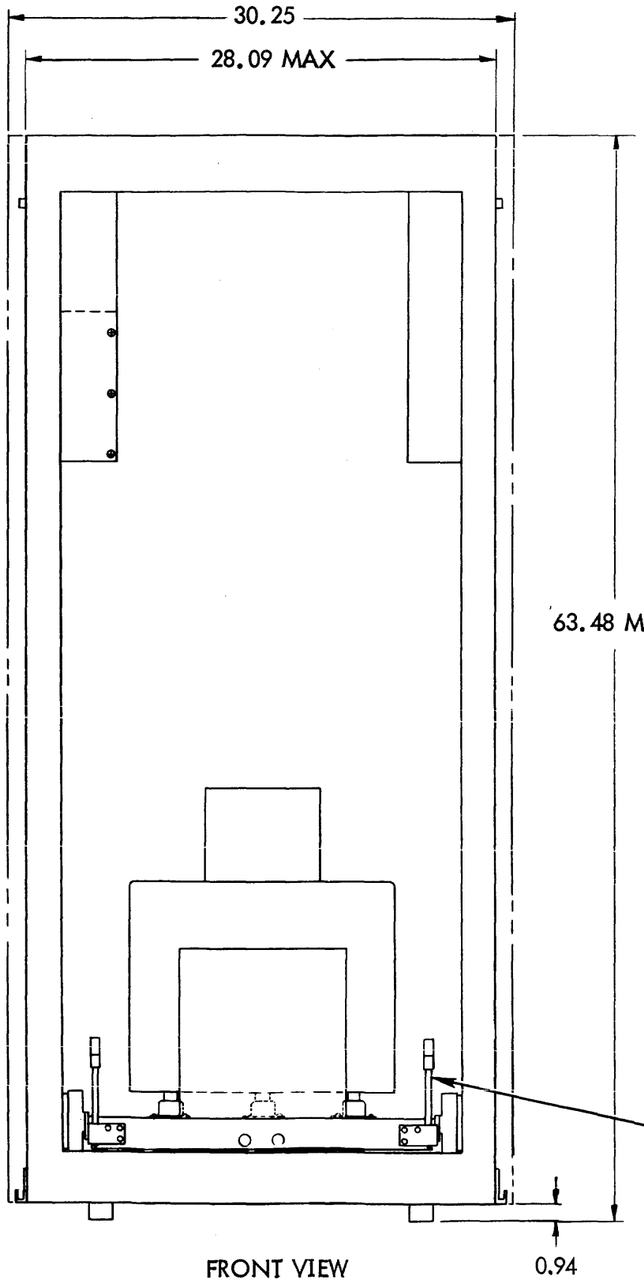
NOTE: REFERENCE SDS DWG: 129776-1A

Figure 7-24. RAD Disc Memory Installation Drawing (Sheet 1 of 3 sheets) 901029A.705/1

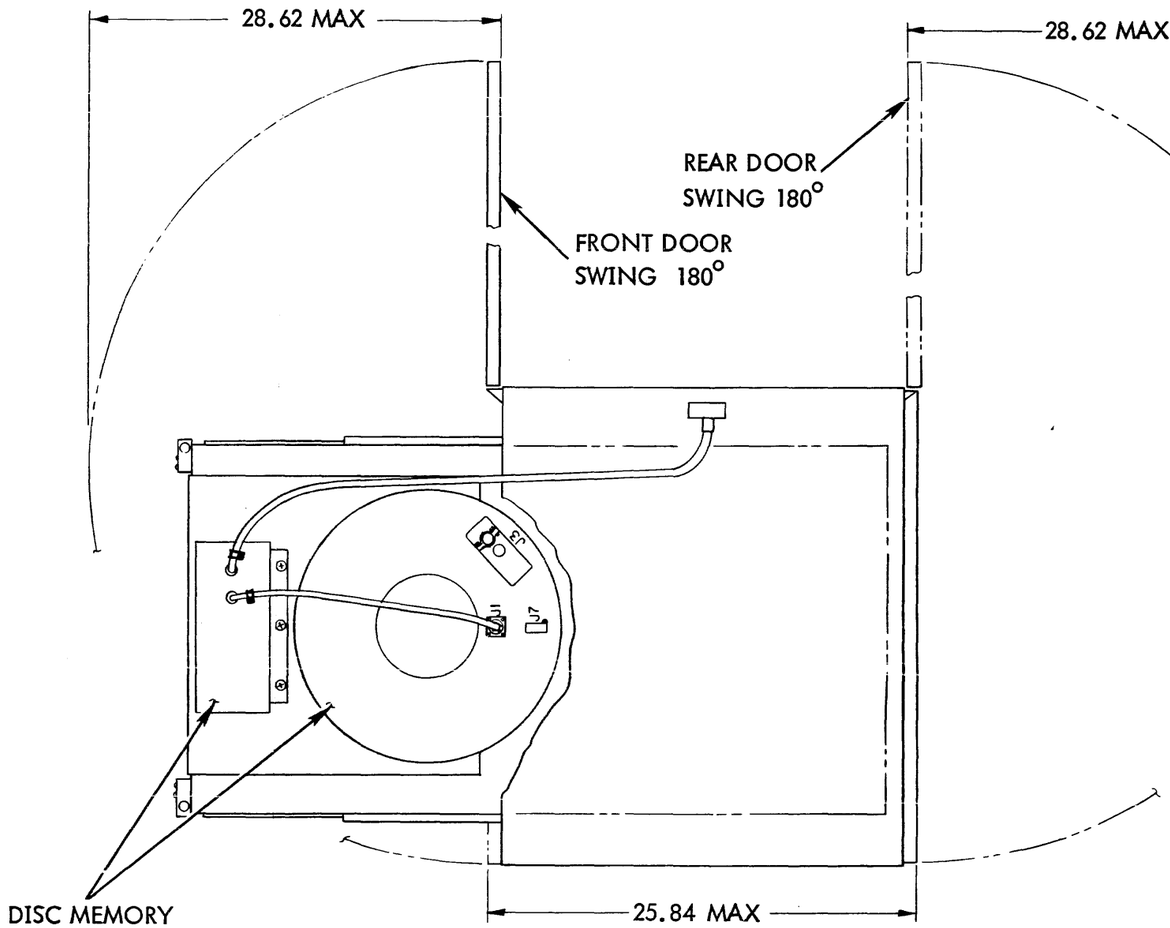


NOTE: REFERENCE SDS DWG: 129776-2A

Figure 7-24. RAD Disc Memory Installation Drawing (Sheet 2 of 3 sheets) 901029A.705/2



FRONT VIEW



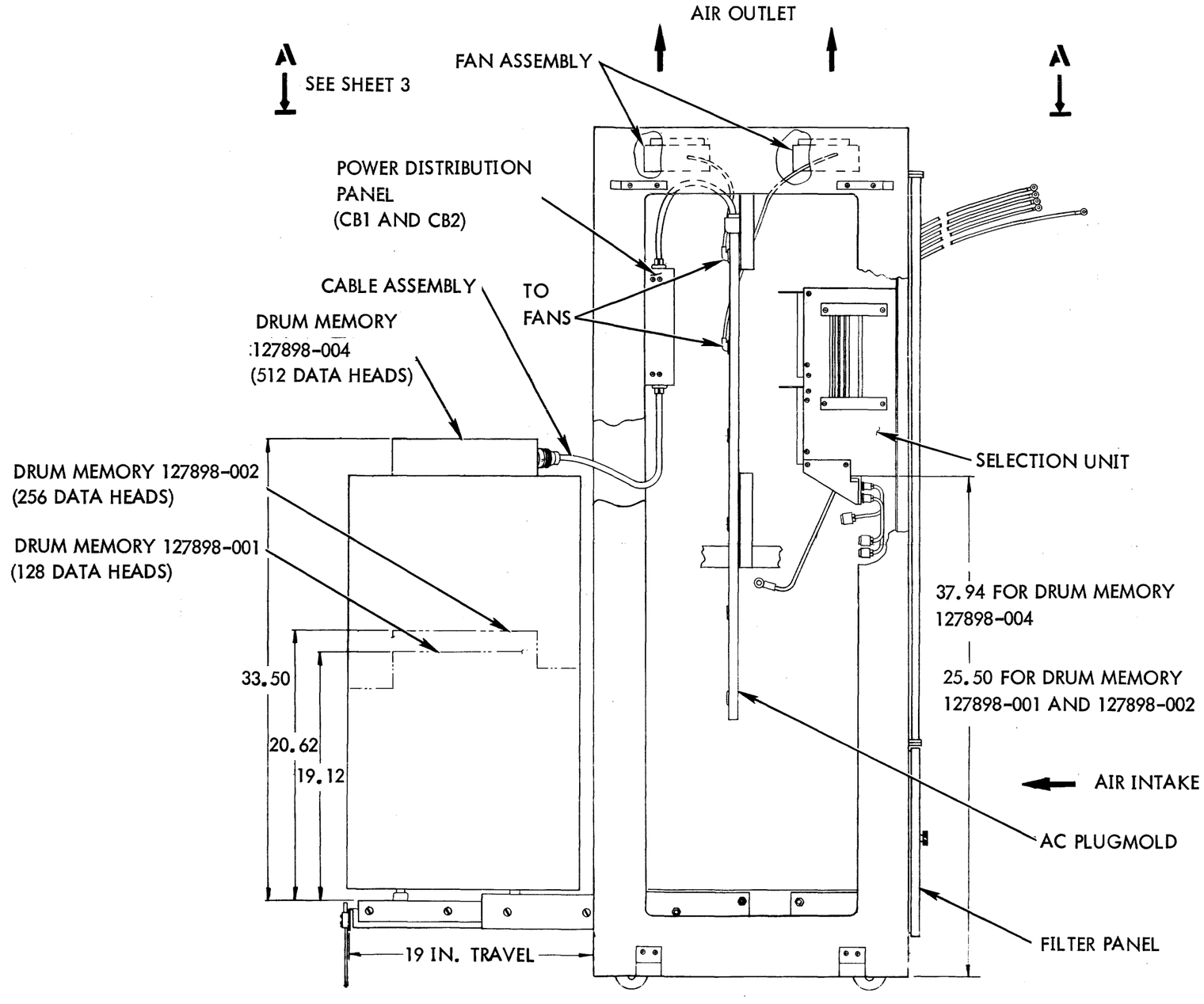
VIEW A-A

SEE SHEET 1

FRONT DOOR OMITTED
DISC MEMORY IN CLOSED POSITION

NOTE: REFERENCE SDS DWG: 129776-3A

Figure 7-24. RAD Disc Memory Installation Drawing (Sheet 3 of 3 sheets) 901029A.705/3

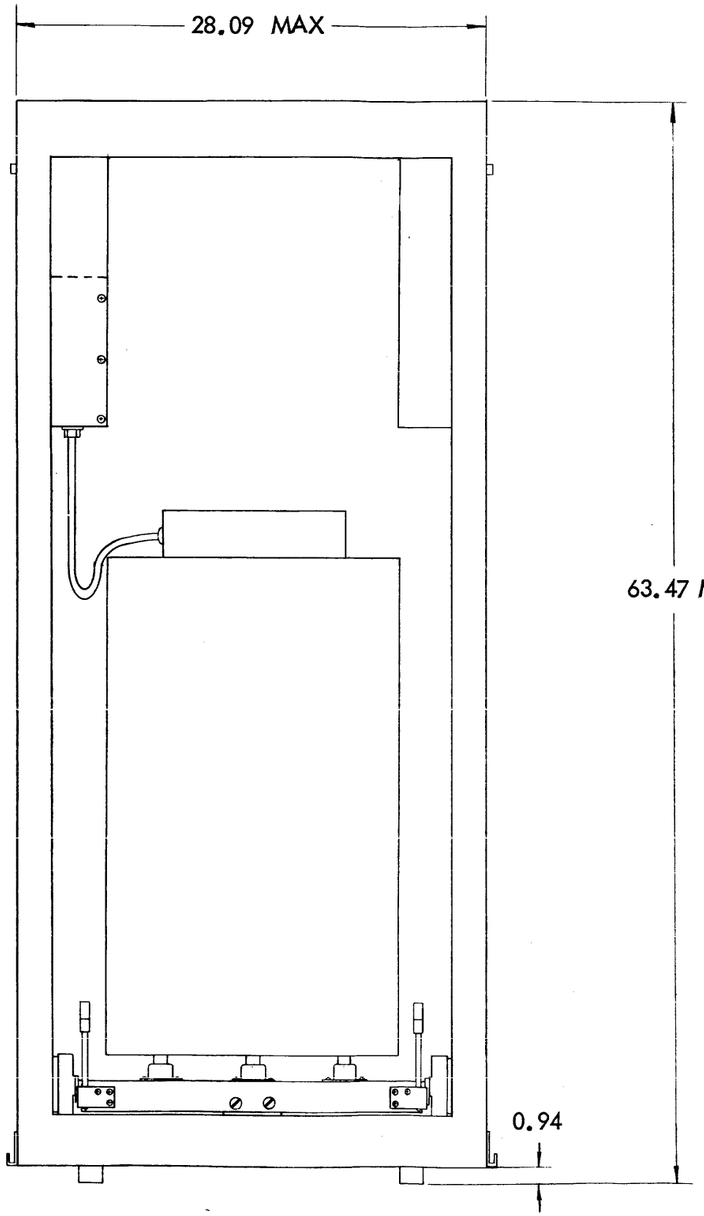


SIDE VIEW
FRONT DOOR OMITTED
DRUM MEMORY EXTENDED

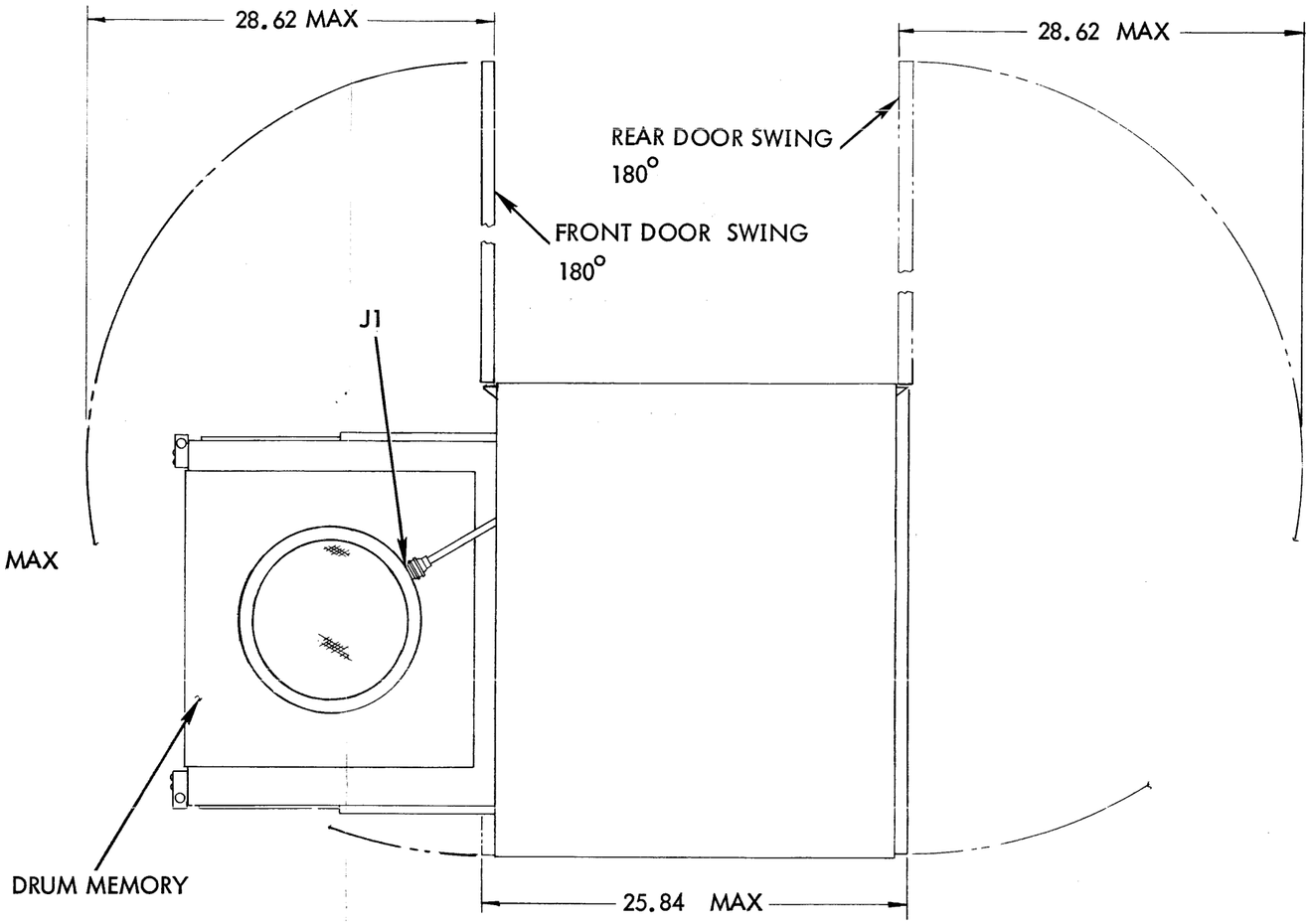
NOTE: REFERENCE SDS DWG: 129775-1A

Figure 7-25. RAD Drum Memory Installation Drawing (Sheet 1 of 3 sheets)

901029A.706/1



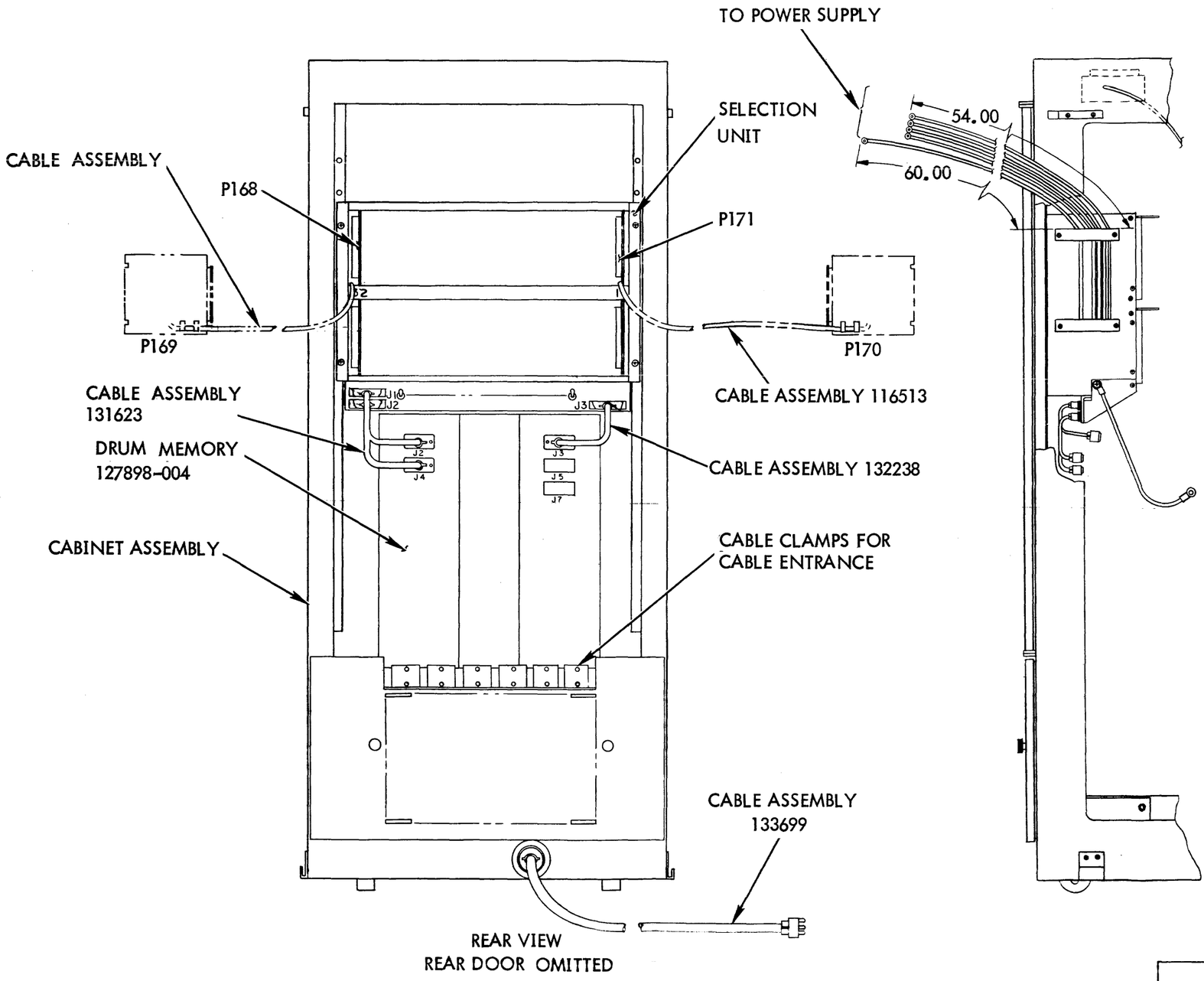
FRONT VIEW, FRONT DOOR OMITTED
DRUM MEMORY IN CLOSED POSITION



VIEW A-A
SEE SHEET 1

NOTE: REFERENCE SDS DWG: 129775-3A

Figure 7-25. RAD Drum Memory Installation Drawing (Sheet 2 of 3 sheets) 901029A.706/2



NOTE: REFERENCE SDS DWG: 129775-2A

Figure 7-25. RAD Drum Memory Installation Drawing (Sheet 3 of 3 sheets) 901029A.706/3

SECTION VIII
LOGIC EQUATIONS

8-1 SCOPE OF SECTION

This section includes: lists for RAD File Model 9367D; signal mnemonic interpretation for the selection unit and controller; a cross-reference for logic diagrams and logic equations.

8-2 SIGNAL MNEMONICS

The mnemonic for a signal in either the selection unit or the controller is normally a three-character code that identifies the signal function or origin combined with a one-character prefix and a one-character suffix. The resultant five-character mnemonic identifies the signal function, the signal origin and relation to other signals of the same three-character mnemonic, but with a different prefix or suffix. The three-character mnemonics for controller signals are listed in table 8-1; the three-character mnemonics for selection unit signals are listed in table 8-2. In these tables, signal mnemonics are listed in alphanumeric order according to the three-character code. Each mnemonic is keyed to the logic diagram for the signal and to the table entry for the related equations.

Table 8-1. Controller Signal Mnemonics

Mnemonic	Description	Figure	Table
ACT	Accept new address	8-9	8-8
AFA	Address bits 9 through 13 all ones	8-9	8-8
AFB	Address bits 14 through 17 all ones	8-9	8-8
AFC	Address bits 18 through 23 all ones	8-9	8-8
AFL	All address bits ones and non-increment mode	8-9	8-8
AIN	Address increment	8-9	8-8
A09 thru A23	Address register flip-flop signals	8-9	8-8
BSC	Begin sector count	8-10	8-9
BUC	Buffer control mode signal from computer	8-15	8-14
CD1 thru CD6	Sector counter signals from selection unit	8-9	8-8
CLH	Compare lower half of sector address	8-9	8-8
CLK	Clock	8-7	8-6
CNT	Count clock pulse	8-7	8-6
CUH	Compare upper half of sector address	8-9	8-8
C09 thru C23	Computer outputs to A-register	8-15	8-14
DAP	Disable lines D01 through D06, and RT0	8-15	8-14
DMA	Disc memory address signal	8-10	8-9
DMW	Disc memory	8-10	8-9
DRA	Clear A-register	8-9	8-8
DRK	Clear K-counter	8-7	8-6
DRV	Clear V-register	8-8	8-6
DRZ	Clear Z-register	8-8	8-7

(Continued)

Table 8-1. Controller Signal Mnemonics (Cont.)

Mnemonic	Description	Figure	Table
D01 thru D06	Sector counter signals	8-15	8-14
ECW	External clock	8-15	8-14
EDS	~~SDS 92 control signal~~ EARLY DISCONNECT	8-12	8-11
ENP	Enable PIN operation	8-15	8-14
ERW	Enter read or write phase	8-10	8-9
E01	Error	8-14	8-13
F01, F02	Phase control flip-flop signals	8-10	8-9
00F	Standby phase signal	8-10	8-9
01F	Write phase signal	8-10	8-9
02F	Read phase signal	8-10	8-9
GS1 thru GS4	RAD memory unit select for PIN operation	8-10	8-9
G01, G02	Unit register	8-10	8-9
HSD	Sector	8-10	8-9
IDN	~~POT~~ input	8-10	8-9
IDT	~~PIN~~ input	8-10	8-9
INT	Interrupt	8-10	8-9
IOC	Input/output computer mode	8-15	8-14
K01 thru K07	Character counter flip-flop signals	8-7	8-6
LDA	Load A-register	8-9	8-8
LDS	Load S-register	8-8	8-7
LDV	Load V-register	8-8	8-7
LDZ	Load Z-register	8-8	8-7
LRC	Load Z-register	8-8	8-7
LR1 thru LR4	Read data input	8-8	8-7
LSC	Last sector	8-7	8-6
LVR	Load V-register	8-8	8-7
M01, M02	Modulo-3 counter	8-7	8-6
NNL	Next to next-to-last sector	8-7	8-6
NXL	Next-to-last sector	8-7	8-6
PIN	Parallel input instruction	8-15	8-14
PT1	Parallel output instruction	8-15	8-14
PT2	Parallel output instruction	8-15	8-14
PWR	Power fail	8-14	8-13
P01 thru P04	Parity register flip-flop signals	8-13	8-12
RCN	Read control	8-10	8-9
REN	Read enable	8-10	8-9

(Continued)

Table 8-1. Controller Signal Mnemonics (Cont.)

Mnemonic	Description	Figure	Table
RF1	Exit from read phase	8-11	8-10
RL1, RL2	Power detection relay control	8-14	8-13
SAC	Sector address compare	8-9	8-8
SHS	Shift S-register	8-8	8-7
SIP	Sector index pulse	8-10	8-9
SPR	Set parity register	8-13	8-12
ST0	Start operation signal from computer	8-14	8-13
STV	One-shot for R-to-V transfer	8-8	8-7
S01 thru S12	S-register flip-flop signals	8-8	8-7
US1 thru US4	Unit select signals	8-8	8-8
U01 thru U06	Subphase flip-flops	8-11	8-10
V01 thru V12	V-register flip-flop signals	8-8	8-7
WD1 thru WD4	Write data output	8-9	8-7
WEN	Write-enable	8-10	8-9
WES	Error signal	8-15	8-14
WHS	Halt signal	8-15	8-14
WLK	Write lockout signal from selection unit	8-10	8-9
WPC	Write preamble	8-7	8-6
W50	Clock timing	8-15	8-14
W60	Clock timing	8-15	8-14
W90	Read/write bit	8-15	8-14
W10 thru W14	RAD address bits	8-15	8-14
X01 thru X09	Data transfer control flip-flops	8-12	8-11
X12	12-bit character	8-10	8-9
Z01 thru Z12	Z-register flip-flop signals	8-8	8-7
00M	Modulo-3 counter, state	8-7	8-6
02M	Modulo-3 counter, state	8-7	8-6
R01 thru R12	Data from input/output channel	8-8	8-7

Table 8-2. Selection Unit Mnemonics

Mnemonic	Description	Figure	Table
A11 thru A17	Band address signals	8-3	8-16
CD1 thru CD6	Sector counter signals	8-2	8-15
CLK	Clock	8-2	
CMC	Write enable	8-4	
DS1 thru DS4	Channel select	8-5	
D01 thru D06	Sector counter flip-flop signals	8-2	8-15
ENP	Enable pulse		
IDX	Index pulse	8-2	
PSL	Select unit for PIN operation	8-3	
PWR	Power-fail		
RCC1 thru RCC4	Read signals	8-5	
RCD1 thru RCD4	Read clock, delayed	8-5	
RCK	Read clock	8-2	
RCL1 thru RCL4	Limiter output	8-5	
RCN	Read control	8-3	
RCS	Read clock	8-2	
RCS1 thru RCS4	Read clock strobe	8-2	
RC01 thru RC04	Read clock	8-5	
RDA1 thru RDA4	Read signals	8-5	
RDD1 thru RDD4	Read signals	8-5	
RDL1 thru RDL4	Read signals	8-5	
RD1S thru RD4S	Read signals	8-5	

(Continued)

Table 8-2. Selection Unit Mnemonics (Cont.)

Mnemonic	Description	Figure	Table
REN	Read enable	8-5	
RX--	Read output signals	8-5	
SEC	Sector pulse	8-2	
SIM	Sector index mark	8-2	
SIP	Sector index pulse P.8-38	8-2	
SP01 thru SP16	Write-protect	8-3	8-16
USA, USB USC, USL	Unit select	8-3	
WCA	Write clock	8-2	
WCH	Write clock head	8-2	
WCK	Half-frequency write clock	8-2	
WCO	Write clock one-shot	8-2	
WDE1 thru WDE4	Encoded write data	8-4	8-17
WD1 thru WD4	Write data	8-4	8-17
WEN	Write enable	8-4	
WLK	Write lockout	8-3	
W--	Write signals		
X--	Memory signals	8-6	
YSC	Y-select control	8-3	
Y01 thru Y32	Write-protect	8-3	8-16

Table 8-3. Interpretation of Mnemonic Prefix

Circuit	Prefix	Interpretation
Flip-flop	0	True if flip-flop is in set state
	1	False if flip-flop is in set state
Signal amplifier or inverter	2	True if condition represented by three-character mnemonic is true
	3	False if condition represented by three-character mnemonic is true
	4	Same as 2
	5	Same as 3
Diode gate	6	Same as 2
	7	Same as 3
Cable driver or special circuit	8	Same as 2
	9	Same as 3

Higher numbers generally indicate later stages of signal amplification or inversion

Table 8-4. Interpretation of Mnemonic Suffix

Suffix	Interpretation
A	Signal originates in controller
C	Signal originates in computer
D	Delayed timing signal
S	Signal originates in RAD memory unit
W	Signal originates in input/output channel

Table 8-5. Examples of Mnemonic Interpretation

Signal	Interpretation
9IDXS	An index signal originating in RAD memory unit; false during index time; output of cable driver or special circuit
2IDXS	An index signal originating in RAD memory unit; true during index time; output of signal amplifier or inverter
0U01A	A signal originating in the controller; true when flip-flop U01 is in set state
2U01A	An output signal of an amplifier or inverter; true when flip-flop U01 is in set state
8BUCW	A buffer control signal originating in input/output channel

(Continued)

Table 8-5. Examples of Mnemonic Interpretation (Cont.)

Signal	Interpretation
3BUCA	A buffer control signal from an amplifier or inverter originating in controller
1VAC5	A test signal for ac voltage
P50V	A test signal for 50 vdc

The meaning of each prefix character is listed in table 8-3; the meaning of each suffix character is listed in table 8-4. Examples of signal mnemonics, including those which do not have prefixes, are provided and interpreted in table 8-5.

8-3 LOGIC EQUATIONS

Logic equations for the selection unit and controller are listed in tables 8-6 through 8-17. The tabulated logic equations correspond to the logic diagrams in figures 8-2 through 8-15. The tables include equations for only those logic elements illustrated in the corresponding figure. To find the source of an input to any diagram, consult tables 8-1 and 8-2 for the figure which shows signal origin.

The logic equations are written in conventional notation of Boolean algebra with the signal mnemonic treated as a Boolean variable. The following notations are used for Boolean operations:

Operation	Notation	Example
OR	+	0X01S + 8PWRA
AND	(none)	0X01S 8PWRA 0U01S
NOT	—	$\overline{\text{0X01S}}$ 8PWRA $\overline{\text{0U01S}}$

In addition to notations of Boolean algebra, an underline is used to identify trigger signal inputs to gates of flip-flops. The trigger signal is the enabling signal for changes of state of ac triggered flip-flops and is the only signal which can cause a change of state. Thus in the equations:

rTC2 = 2LDWS 9WD1A 2CL1S

sTC2 = 2LDWS 2WD1S 2CL1S

flip-flop TC2 cannot be set or reset until signal 2CL1S is true, regardless of the level of other signals. For a detailed description of trigger inputs, refer to SDS publication 64-55-14.

8-4 LOGIC DIAGRAMS

Figure 8-1 shows the relation between symbols used in SDS logic diagrams and simplified symbols. The SDS symbols used in figures 8-2 through 8-15 are related to both the

logical function and circuit design of module components. The simplified symbols in figure 8-1 represent only logical functions corresponding to notations in Boolean algebra. For a detailed description of the information represented by SDS symbols, refer to SDS publication 64-55-14.

The table of logic equations corresponding to a logic diagram sometimes deletes an intervening amplifier or inverter. For example, consider the complete equations for signal 8INTA (see figure 8-10 and table 8-9):

$$8INTA = \overline{3INTA}$$

$$\overline{3INTA} = 6INTA$$

$$6INTA = 200FA\ 2SACA\ 0BSCA\ 2U01A\ 1X03A\ 1X01A$$

For simplicity, the intervening inverter may be deleted:

$$8INTA = 200FA\ 2SACA\ 0BSCA\ 2U01A\ 1X03A\ 1X01A$$

In this case, the related signals for which no equations are given (3INTA, 6INTA) differ from listed signals having the same three-character mnemonic only in the prefix. In all cases in which an intervening amplifier or inverter is deleted from the table, the logic level of the related signals can be determined from the prefix, as summarized in table 8-3.

When a flip-flop is in the set state, output signals with an even prefix (0U01A, 2U01A) are true and output signals with an odd prefix (1U01A, 3U01A) are false. When logic equations are written using three-character mnemonics only, even-numbered output signals take the normal form (U01), and odd-numbered output signals take the complemented form ($\overline{U01}$). For example:

$$INT = 00F\ SAC\ BSC\ U01\ \overline{X03}\ \overline{X01}$$

Table 8-6. Logic Equations for Controller Timing Circuits

Equation	Comment
3CLKA = 9CLKS	Clock
6CLKA = $\overline{9CLKS}$	
2CLKD = $\overline{9CLKS}$	
5CLKD = $\overline{2CLKD}$	
sM02 = 1M01A 2CNTA	Modulo-3 counter
rM02 = 2CNTA	
tM02 = $\overline{3DRKA}$	
sM01 = 0M02A 2CNTA	
rM01 = 2CNTA	

(Continued)

Table 8-6. Logic Equations for Controller Timing Circuits (Cont.)

Equation	Comment
tM01 = $\overline{3DRKA}$	Modulo-3 counter
2CNTA = 2U02A 2CLKA	
+ 201FA 3U01A 2CLKA	Write phase count
+ 202FA 3U01A 2CLKA	Read phase count
$\overline{3DRKA}$ = 200FA	Standby phase
+ 3U02A	
+ 2U01A 2CLKD	
$\overline{300MA}$ = 1M01A 1M02A	
302MA = $\overline{0M01A}$	
2LSCA = 0M01A 2K07A	Last sector
2WPCA = 2K06A 202MA 2U01A	Write preamble
sK01 = 0K02A	
rK01 = 0K02A	
yK01 = $\overline{3DRKA}$	
sK02 = 0K03A	
rK02 = 0K03A	
yK02 = $\overline{3DRKA}$	
sK03 = 0K04A	
rK03 = 0K04A	
yK03 = $\overline{3DRKA}$	
sK04 = 0K05A 0K06A 2LSCA	
2CNTA	
rK04 = 0K05A 0K06A 2LSCA	
2CNTA	
yK04 = $\overline{3DRKA}$	
$\overline{3NNLA}$ = 0K01A 0K02A 0K03A 0K04A 0K05A	
2NXLA = $\overline{3NNLA}$ $\overline{1K06A}$	Next-to-last character (1 111 110)
2NNLA = $\overline{3NNLA}$	
BK06A = 2K07A	
+ 0M07A 2U01A 201FA	
sK05 = $\overline{2U01A}$ $\overline{2K06A}$ $\overline{201FA}$	
0K06A	
rK05 = 0K06A	
tK05 = $\overline{3DRKA}$	
sK06 = 0K07A	

(Continued)

Table 8-6. Logic Equations for Controller Timing Circuits (Cont.)

Equation	Comment
rK06 = BK06A	
tK06 = 3DRKA	
sK07 = 2U01A 2K06A 201FA 0M01A	
rK07 = 0M01A	
tK07 = 3DRKA	

Table 8-7. Logic Equations for Data Registers

Equation	Comment
sS01 = 2LDSA 0Z01A 4CLKA + 2SHSA 0S02A 4CLKA	LDS to load from Z-register SHS to shift and load from selection unit (LR1 through LR4)
rS01 = 2LDSA 1Z01A 4CLKA + 2SHSA 1S02A 4CLKA	
yS02 = 2LDSA 0Z02A	
sS02 = 0S03A 2SHSA	
rS02 = 0S03A 2SHSA	
yS03 = 2LDSA 0Z03A	
sS03 = 2LR1A 2SHSA	
rS03 = 2LR1A 2SHSA	
sS04 = 2LDSA 0Z04A 4CLKA + 2SHSA 0S05A 4CLKA	
rS04 = 2LDSA 1Z04A 4CLKA + 2SHSA 1S05A 4CLKA	
yS05 = 2LDSA 0Z05A	
sS05 = 0S06A 2SHSA	
rS05 = 0S06A 2SHSA	
yS06 = 2LDSA 0Z06A	
sS06 = 2LR2A 2SHSA	
rS06 = 2LR2A 2SHSA	
sS07 = 2LDSA 0Z07A 4CLKA + 2SHSA 0S08A 4CLKA	
rS07 = 2LDSA 1Z07A 4CLKA + 2SHSA 1S08A 4CLKA	
yS08 = 2LDSA 0Z08A	
sS08 = 0S09A 2SHSA	
rS08 = 0S09A 2SHSA	

(Continued)

Table 8-7. Logic Equations for Data Registers (Cont.)

Equation	Comment
yS09 = 2LDSA 0Z09A	
sS09 = 2LR3A 2SHSA	
rS09 = 2LR3A 2SHSA	
sS10 = 2LDSA 0Z10A 4CLKA + 2SHSA 0S11A 4CLKA	
rS10 = 2LDSA 1Z10A 4CLKA + 2SHSA 1S11A 4CLKA	
yS11 = 2LDSA 0Z11A	
sS11 = 0S12A 2SHSA	
rS11 = 0S12A 2SHSA	
yS12 = 2LDSA 0Z12A	
sS12 = 2LR4A 2SHSA	
rS12 = 2LR4A 2SHSA	
sZ01 = 2LDZA 0V01A + 2LRCA 0S01A	LDZ to load from V-register LRC to load from S-register DRZ to clear Z-register
rZ01 = 2LRCA 1S01A	
tZ01 = 3DRZA	
sZ02 = 2LDZA 0V02A + 2LRCA 0S02A	
rZ02 = 2LRCA 1S02A	
tZ02 = 3DRZA	
sZ03 = 2LDZA 0V03A + 2LRCA 0S03A	
rZ03 = 2LRCA 1S03A	
tZ03 = 3DRZA	
sZ04 = 2LDZA 0V04A + 2LRCA 0S04A	
rZ04 = 2LRCA 1S04A	
tZ04 = 3DRZA	
sZ05 = 2LDZA 0V05A + 2LRCA 0S05A	
rZ05 = 2LRCA 1S05A	
tZ05 = 3DRZA	

(Continued)

Table 8-7. Logic Equations for Data Registers (Cont.)

Equation	Comment
sZ06 = 2LDZA 0V06A	LDZ to load from V-register
+ 2LRCA 0S06A	LRC to load from S-register
rZ06 = 2LRCA 1S06A	$\overline{DRZ}$ to clear Z-register
tZ06 = 3DRZA	
sZ07 = 2LDZA 0V07A	
+ 2LRCA 0S07A	
rZ07 = 2LRCA 1S07A	
tZ07 = 3DRZA	
sZ08 = 2LDZA 0V08A	
+ 2LRCA 0S08A	
rZ08 = 2LRCA 1S08A	
tZ08 = 3DRZA	
sZ09 = 2LDZA 0V09A	
+ 3LRCA 0S09A	
rZ09 = 3LRCA 1S09A	
tZ09 = 3DRZA	
sZ10 = 2LDZA 0V10A	
+ 2LRCA 0S10A	
rZ10 = 2LRCA 1S10A	
tZ10 = 3DRZA	
sZ11 = 2LDZA 0V11A	
+ 2LRCA 0S11A	
rZ11 = 2LRCA 1S11A	
tZ11 = 3DRZA	
sZ12 = 2LDZA 0V12A	
+ 2LRCA 0S12A	
rZ12 = 2LRCA 1S12A	
tZ12 = 3DRZA	
sV01 = 2LDVA 8R01W	LDV to load from I/O channel
+ 2LVRA 0Z01A	LVR to load from Z-register
rV01 = 2LVRA 1Z01A	$\overline{DRV}$ to clear V-register
tV01 = 3DRVA	
sV02 = 2LDVA 8R02W	
+ 2LVRA 0Z02A	
rV02 = 2LVRA 1Z02A	
tV02 = 3DRVA	

(Continued)

Table 8-7. Logic Equations for Data Registers (Cont.)

Equation	Comment
sV03 = 2LDVA 8R03W	
+ 2LVRA 0Z03A	
rV03 = 2LVRA 1Z03A	
tV03 = 3DRVA	
sV04 = 2LDVA 8R04W	
+ 2LVRA 0Z04A	
rV04 = 2LVRA 1Z04A	
tV04 = 3DRVA	
sV05 = 2LDVA 8R05W	
+ 2LVRA 0Z05A	
rV05 = 2LVRA 1Z05A	
tV05 = 3DRVA	
sV06 = 2LDVA 8R06W	
+ 2LVRA 0Z06A	
rV06 = 2LVRA 1Z06A	
tV06 = 3DRVA	
sV07 = 2LDVA 8R07W	
+ 2LVRA 0Z07A	
rV07 = 2LVRA 1Z07A	
tV07 = 3DRVA	
sV08 = 2LDVA 8R08W	
+ 2LVRA 0Z08A	
rV08 = 2LVRA 1Z08A	
tV08 = 3DRVA	
sV09 = 2LDVA 8R09W	
+ 2LVRA 0Z09A	
rV09 = 2LVRA 1Z09A	
tV09 = 3DRVA	
sV10 = 2LDVA 8R10W	
+ 2LVRA 0Z10A	
rV10 = 2LVRA 1Z10A	
tV10 = 3DRVA	
sV11 = 2LDVA 8R11W	
+ 2LVRA 0Z11A	
rV11 = 2LVRA 1Z11A	
tV11 = 3DRVA	

(Continued)

Table 8-7. Logic Equations for Data Registers (Cont.)

Equation	Comment
sV12 = 2LDVA 8R12W	
+ 2LVRA 0Z12A	
rV12 = 2LVRA 1Z12A	
tV12 = 3DRVA	
2LDVA = 201FA 2X03A 2X06A 0STVA 2W60A 2CLKA	Load V-register, write phase
2LDZA = 201FA 0X07A 2CLKA	Load Z-register, write phase
2LVRA = 202FA 0X07A 1X08A 2CLKD	Load V-register
+ 202FA 202MA 0X08A 3CLKA	Load V-register
2LRCA = 202FA 200MA 2CLKA	Load Z-register, read phase
0STVA = 3CLKD	
2LDSA = 201FA 202MA 2CLKD	Load S-register from Z write phase
$\overline{3DRZA}$ = 201FA 1X08A 0X09A	Clear Z-register, write phase
2SHSA = 201FA 302MA 2CLKA	Shift S-register, write phase
+ 202FA 2CLKA	Shift S-register, read phase
$\overline{3DRVA}$ = $\overline{7DRVA}$ $\overline{1F02A}$	Clear V-register
$\overline{7DRVA}$ = 1X03A + 1X06A 2W56A 3CLKA	
9V01A = 0V01A 2W60A 1F01A	W60 to transfer contents of V-register to input/output channel
9V02A = 0V02A 2W60A 1F01A	
9V03A = 0V03A 2W60A 1F01A	
9V04A = 0V04A 2W60A 1F01A	
9V05A = 0V05A 2W60A 1F01A	
9V06A = 0V06A 2W60A 1F01A	
9V07A = 0V07A 2W60A 1F01A	
9V08A = 0V08A 2W60A 1F01A	
9V09A = 0V09A 2W60A 1F01A	
9V10A = 0V10A 2W60A 1F01A	
9V11A = 0V11A 2W60A 1F01A	
9V12A = 0V12A 2W60A 1F01A	
8NP0A = 2DMWA 1F01A	
2LR1A = $\overline{9RD1S}$ 202FA	
2LR2A = $\overline{9RD2S}$ 202FA	

(Continued)

Table 8-7. Logic Equations for Data Registers (Cont.)

Equation	Comment
2LR3A = $\overline{9RD3S}$ 202FA	
2LR4A = $\overline{9RD4S}$ 202FA	
$\overline{9WD1A}$ = 201FA 2U01A 2U03A	Write preamble
+ 201FA 201UA 0P01A	Write parity bits
+ 201FA 223UA 0S01A	Write data bits
$\overline{9WD2A}$ = 201FA 2U01A 2U03A	
+ 201FA 201UA 0P02A	
+ 201FA 223UA 0S04A	
$\overline{9WD3A}$ = 201FA 2U01A 2U03A	
+ 201FA 201UA 0P03A	
+ 201FA 223UA 0S07A	
$\overline{9WD4A}$ = 201FA 2U01A 2U03A	
+ 201FA 201UA 0P04A	
+ 201FA 223UA 0S10A	

Table 8-8. Logic Equations for Address Register

Equation	Comment
yA09 = 2LDAA 8C09C	LDA to read POT data and store in A-register $\overline{DRA}$ to clear A-register
sA09 = 0A10A	
rA09 = 0A10A	
tA09 = $\overline{3DRAA}$	
yA10 = 2LDAA 8C10C	
sA10 = 0A11A	
rA10 = 0A11A	
tA10 = $\overline{3DRAA}$	
yA11 = 2LDAA 8C11C	
sA11 = 0A12A	
rA11 = 0A12A	
tA11 = $\overline{3DRAA}$	
yA12 = 2LDAA 8C12C	
sA12 = 0A13A	
rA12 = 0A13A	
tA12 = $\overline{3DRAA}$	
yA13 = 2LDAA 8C13C	
sA13 = 2AFCA 2AFBA 2AINA	
rA13 = 2AFCA 2AFBA 2AINA	

(Continued)

Table 8-8. Logic Equations for Address Register (Cont.)

Equation	Comment
tA13 = $\overline{3DRAA}$	
yA14 = 2LDAA 8C14C	
sA14 = 0A15A	
rA14 = 0A15A	
tA14 = $\overline{3DRAA}$	
yA15 = 2LDAA 8C15C	
sA15 = 0A16A	
rA15 = 0A16A	
tA15 = $\overline{3DRAA}$	
yA16 = 2LDAA 8C16C	
sA16 = 0A17A	
rA16 = 0A17A	
tA16 = $\overline{3DRAA}$	
yA17 = 2LDAA 8C17C	
sA17 = 2AFCA 2AINA	LDA to read POT data and store in A-register
rA17 = 2AFCA 2AINA	
tA17 = $\overline{3DRAA}$	$\overline{DRA}$ to clear A-register
yA18 = 2LDAA 8C18C	
sA18 = 0A19A	
rA18 = 0A19A	
tA18 = $\overline{3DRAA}$	$\overline{DRA}$ to clear A-register
yA19 = 2LDAA 8C19C	
sA19 = 0A20A	
rA19 = 0A20A	
tA19 = $\overline{3DRAA}$	
yA20 = 2LDAA 8C20C	
sA20 = 0A21A	
rA20 = 0A21A	
tA20 = $\overline{3DRAA}$	
yA21 = 2LDAA 8C21C	
sA21 = 0A22A	
rA21 = 0A22A	
tA21 = $\overline{3DRAA}$	
yA22 = 2LDAA 8C22C	
sA22 = 0A23A	
rA22 = 0A23A	
tA22 = $\overline{3DRAA}$	

(Continued)

Table 8-8. Logic Equations for Address Register (Cont.)

Equation	Comment
yA23 = 2LDAA 8C23C	
sA23 = 2AINA	
rA23 = 2AINA	
tA23 = $\overline{3DRAA}$	
2LDAA = 0X01A 0X02A 8PT2C	Load A-register
3DRAA = 3ACTA 8PWRA	Clear A-register
$\overline{3ACTA}$ = 200FA 0U06A 1X03A	Accept address
2AINA = 2CLKA 3AFLA 2RF1A	Read phase increment address
+ 2CLKA 3AFLA 2K06A 2LSCA 201FA 201UA	Write phase increment address
2AFLA = 3AFLA	
3AFLA = $\overline{6AFLA}$	
6AFLA = 2AFAA 2AFBA 2AFCA	A-register all ones
2AFAA = 0A12A 0A13A	
2AFBA = 0A14A 0A15A 0A16A 0A17A	
2AFCA = 0A18A 0A19A 0A19A 0A20A 0A21A 0A22A 0A23A 1X05A	X05 if non-increment mode. (Only sector bits count)
9US1A = $\overline{1A09A}$ $\overline{1A10A}$	Select RAD memory unit 1
9US2A = $\overline{1A09A}$ 0A10A	Select RAD memory unit 2
9US3A = 0A09A $\overline{1A10A}$	Select RAD memory unit 3
9US4A = 0A09A 0A10A	Select RAD memory unit 4
8A11A = $\overline{1A11A}$	Band address signals
8A12A = $\overline{1A12A}$	
8A13A = $\overline{1A13A}$	
8A14A = $\overline{1A14A}$	
8A15A = $\overline{1A15A}$	
8A16A = $\overline{1A16A}$	
8A17A = $\overline{1A17A}$	
2CD1A = $\overline{9CD1S}$	Sector count for PIN operation
2CD2A = $\overline{9CD2S}$	
2CD3A = $\overline{9CD3S}$	
2CD4A = $\overline{9CD4S}$	
2CD5A = $\overline{9CD5S}$	
2CD6A = $\overline{9CD6S}$	

(Continued)

Table 8-8. Logic Equations for Address Register (Cont.)

Equation			Comment
MSAA	=	0A09A 0A10A 0A11A	
2SACA	=	2CUHA 2CLHA	Sector address compare
2CLHA	=	$\overline{7CLHA}$	
2CUHA	=	$\overline{7CUHA}$	
7CLHA	=	0A21A 9CD4S	Compare lower half
		+ 1A21A 2CD4S	
		+ 0A22A 9CD5S	
		+ 1A22A 2CD5S	
		+ 0A23A 9CD6S	
		+ 1A23A 2CD6S	
7CUHA	=	0A18A 9CD1S	Compare upper half
		+ 1A18A 2CD1S	
		+ 0A19A 9CD2S	
		+ 1A19A 2CD2S	
		+ 0A20A 9CD3S	
		+ 1A20A 2CD3S	

Table 8-9. Logic Equations for Phase Control Circuits

Equation			Comment
sF01	=	2ERWA 2DMWA	Enter read phase
		3W90A 4CLKA	
rF01	=	2RF1A 4CLKA	Exit from read phase
tF01	=	$\overline{3DRAA}$	Clear
sF02	=	2ERWA 2DMWA	Enter write phase
		8W90W 4CLKA	
rF02	=	201FA 3U02A 2LSCA 4CLKA	Exit from write phase
		+ 201FA 2WLKA 4CLKA	Exit if write-protected
tF02	=	$\overline{3DRAA}$	Clear
2WLKA	=	$\overline{9WLKS}$	Write lockout
2ERWA	=	200FA 0K05A 2X03A	
2DMWA	=	8W10W 3W11A	RAD addressed
		8W12A 8W13A	
		3W14A	
202FA	=	0F01A 1F02A	Read phase

(Continued)

Table 8-9. Logic Equations for Phase Control Circuits (Cont.)

Equation			Comment
201FA	=	1F01A 0F02A	Write phase
200FA	=	1F01A 1F02A	Standby phase
sG01	=	2C12A 2IDNA	Store RAD memory unit addressed during PIN operation
rG01	=	3C12A 2IDNA	
tG01	=	$\overline{8PWRA}$	
sG02	=	2C13A 2IDNA	
rG02	=	3C13A 2IDNA	
tG02	=	$\overline{8PWRA}$	
2IDNA	=	8C16W 8I0CW 2DMAA	Alert to PIN
2IDTA	=	3C16A 8I0CW 2DMAA	Alert to POT
2DMAA	=	9C17W 8C19W 3C20W 8C21W 8C22W 3C23W	RAD addressed
8GS1A	=	$\overline{0G01A}$ $\overline{0G02A}$	Select RAD memory unit 1
8GS2A	=	$\overline{0G01A}$ $\overline{1G02A}$	Select RAD memory unit 2
8GS3A	=	$\overline{1G01A}$ $\overline{0G02A}$	Select RAD memory unit 3
8GS4A	=	$\overline{1G01A}$ $\overline{1G02A}$	Select RAD memory unit 4
9WENA	=	$\overline{201FA}$	Write-enable
9X12A	=	$\overline{2DMWA}$	
8RCNA	=	$\overline{202FA}$	Read control
9RENA	=	$\overline{0U05A}$	Read-enable after sU05
0BSCA	=	200FA 2HSDA 2SIPA	Initiate read or write operation
2SIPA	=	$\overline{9SIPS}$	Sector index pulse
2HSDA	=	2U01A 1X01A	New address in A-register, POT complete
		+ 3U03A 0X03A	Continue after sector gap
		+ 5U01A 0X05A 1E01A	Non-increment mode
8INTA	=	200FA 2SACA 0BSCA	Priority interrupt
		+ 2U01A 1X03A 0X01A	

Table 8-10. Logic Equations for Subphase Circuits

Equation	Comment
yU01 = 2LDAA	Load A-register
sU01 = 2ERWA 4CLKA	Exit from standby phase
rU01 = 201FA 2WPCA 4CLKA	End write preamble
+ 201FA 2WLKA 4CLKA	Exit if write-protected
+ 202FA 2U02A 2U03A 4CLKA	Preamble
tU01 = $\overline{\text{3DRAA}}$	Clear
yU02 = 200FA 0BSCA 2SACA 2HSDA	Sector address compared
sU02 = 201FA 2U01A 9WLKS 4CLKA	First clock in write phase
+ 202FA 2U01A 3U03A 200MA 4CLKA	First clock in read phase
+ 202FA 2U01A 2U03A 1S03A 9RD1S 4CLKA	Detect read preamble
rU02 = 200FA 0K05A 4CLKA	Stop clock count
+ 201FA 2LSCA 2NXLA 4CLKA	Prepare for exit from write phase
+ 202FA 2LSCA 2NXLA 4CLKA	Prepare for exit from read phase
+ 202FA 2U01A 202MA 0K07A 4CLKA	Start search for preamble
tU02 = $\overline{\text{3DRAA}}$	Clear
sU03 = 201FA 2U01A PNCA 4CLKA	Write preamble
+ 201FA 3U02A 2AFLA 2LSCA 4CLKA	Exit from write phase
+ 202FA 0U01A 0U02A 202MA 0K07A 4CLKA	
+ 202FA 5U01A 1U02A 0X07A 1X08A 4CLKA	
rU03 = 2ERWA 4CLKA	Exit from standby phase
+ 200FA 1X03A 4CLKA	Buffer disconnected
+ 201FA 2U01A PNCA 4CLKA	Write preamble
+ 202FA 2U01A 2U02A 200MA 4CLKA	
+ 2RF1A 3AFLA 4CLKA	Exit from read phase
tU03 = $\overline{\text{3DRAA}}$	Clear
sU04 = 201FA 2NNLA 2K07A 202MA 2CLKD	
+ 202FA 3U01A 200MA	
rU04 = 2RF1A	Exit from read phase
+ 200FA 2ERWA	Exit from standby phase
tU04 = $\overline{\text{8PWRA}}$	Power-fail
sU05 = 200FA 2U02A 200MA 0K07A	Third clock following sU02
rU05 = 2RF1A	Exit from read phase
+ 2ERWA 2DMWA 8W90W 2CLKA	Enter write phase
tU05 = $\overline{\text{8PWRA}}$	Power-fail
sU06 = 2IDTA	Alert to POT
rU06 = 2PTQA 0X01A	
tU06 = $\overline{\text{8PWRA}}$	Power-fail

(Continued)

Table 8-10. Logic Equations for Subphase Circuits (Cont.)

Equation	Comment
2RF1A = 202FA 3U01A 3U02A 202MA 2K06A	Exit from read phase
201UA = 1U01A 1U02A	
223UA = 1U01A 0U02A	
$\overline{\text{PNCA}}$ = 300MA 2K06A	
$\overline{\text{NUFA}}$ = 300FA 201UA	
$\overline{\text{PUFA}}$ = 300FA NUFA	

Table 8-11. Logic Equations for Data Transfer Control Circuits

Equation	Comment
sX01 = 0U06A NUFA 2PTQA	
rX01 = NUFA 2PT1A	
tX01 = 8PWRA	Power-fail
yX02 = 200FA 0X01A 1X03A	
sX02 = 2IDNA	
rX02 = BX02A	
tX02 = 8PWRA	Power-fail
sX03 = 200FA 2BUCA 2DMAA	Buffer connected
rX03 = 200FA 0X04A 2CLKA	Error during read/write
+ 201FA 2WLKA 2CLKA	Write lockout
+ 3U01A $\overline{\text{9EDSW}}$ 2CLKA	
+ 3U01A $\overline{\text{2DMWA}}$ 2CLKA	
tX03 = 8PWRA	Power-fail
sX04 = 201FA 0X08A 0X09A 202MA 5U01A 5CLKD	Write timing error
+ 202FA 1X09A 3U01A 200MA 2CLKD $\overline{\text{1U02A}}$	Read timing error
+ 202FA 1X09A 3U01A 200MA 2CLKD $\overline{\text{2K06A}}$	Read timing error
rX04 = 200FA 2CLKA	Clear
tX04 = 8PWRA	Power-fail
sX05 = 2C14A 2TNIA	
+ $\overline{\text{2C14A}}$ 2TNIA	
sX06 = 201FA 2W56A 3CLKA	Write
+ 201FA 3W50A 1X03A 3CLKA	Write
+ 202FA 3U01A 202MA 1U04A 3CLKA	Read
+ 202FA 2W56A 0U04A 3CLKA	Read
rX06 = 2ERWA 2CLKA	Exit from standby
+ 201FA 3CLKA	Enter write

(Continued)

Table 8-11. Logic Equations for Data Transfer Control Circuits (Cont.)

Equation	Comment
+ 202FA 3U03A 5U01A 3CLKA 1M01A	Read
+ 202FA 3U03A 5U01A 3CLKA 1X09A	
sX07 = 201FA 1X08A 0X09A 3CLKA	Write
+ 202FA 2X06A 1X09A 3CLKA	Read
+ 202FA 0X06A 1M01A 5CLKD 3CLKA	
rX07 = 3CLKA	
sX08 = 2ERWA 2DMWA 8W90W 2CLKA	Exit from standby
+ 201FA 1U04A 0X09A 3CLKA	Write
+ 202FA 0X06A 1X09A 202MA 2CLKA	Read
rX08 = 201FA 2X06A 2CLKA	Write
+ 202FA 202MA 3CLKA	Read
yX09 = 2U01A 3U02A	After exit from standby
sX09 = 201FA 2WPCA 2CLKA	End write preamble
+ 201FA 3U01A 202MA 2CLKA	Write
+ 202FA 0X07A 300MA 3CLKA	Read
+ 202FA 0X08A 3CLKA	
rX09 = 202FA 3U01A 200MA 2CLKA	Read
+ 201FA 0X07A 2CLKA $\overline{202MA}$	Write
+ 201FA 0X07A 2CLKA $\overline{3U01A}$	
2W56A = 2W50A $\overline{3W60A}$	
2TNIA = PUFA 2IDTA 1X03A	
BX02A = 2RTIA	Exit from PIN wait phase
+ 2PT1A	Alert to POT

Table 8-12. Logic Equations for Parity Register

Equation	Comment
yP01 = 2SPRA	WD1 through WD4 for write parity (01F)
sP01 = 201FA 4WD1A 4CLKA	
+ 2U02A 4CLKA 2LR1A	
rP01 = 201FA 4WD1A 4CLKA	LR1 through LR4 for read parity (02F)
+ 2U02A 4CLKA 2LR1A	
yP02 = 2SPRA	
sP02 = 201FA 4WD2A 4CLKA	
+ 2U02A 4CLKA 2LR2A	

(Continued)

Table 8-12. Logic Equations for Parity Register (Cont.)

Equation	Comment
rP02 = 201FA 4WDZA 4CLKA	
+ 2U02A 4CLKA 2LR2A	
yP03 = 2SPRA	
sP03 = 201FA 4WD3A 4CLKA	
+ 2U02A 4CLKA 2LR3A	
rP03 = 201FA 4WD3A 4CLKA	
+ 2U02A 4CLKA 2LR3A	
yP04 = 2SPRA	
sP04 = 201FA 4WD4A 4CLKA	
+ 2U02A 4CLKA 2LR4A	
rP04 = 201FA 4WD4A 4CLKA	
+ 2U02A 4CLKA 2LR4A	
2SPRA = 201FA 2U01A	
+ 202FA 2U01A 3U02A	
3PCPA = 1P01A 2LR1A	
+ 0P01A 9RD1S	
+ 1P02A 2LR2A	
+ 0P02A 9RD2S	
+ 1P03A 2LR3A	
+ 0P03A 9RD3S	
+ 1P04A 2LR4A	
+ 0P04A 9RD4S	

Table 8-13. Logic Equations for Error Circuits and Power Failure Circuits

Equation	Comment
yE01 = 0X01A 0X02A 8PT2A	Illegitimate POT
sE01 = 200FA 2U03A 2SIPA 4CLKA	Address overflow
+ 201FA 2WLKA 4CLKA	Write-protected
rE01 = 200FA 2BUCA 2DMAA	New instruction
E01 = 1STOC	START pushbutton
8PWRA = 8STOC	START pushbutton
+ 3RL1A	Relay control
+ 3RL2A	Relay control

Table 8-14. Logic Equations for Controller Input/Output Signals

Equation	Comment
2D01A = $\overline{9D01S}$	Sector counter signals from selection unit
2D02A = $\overline{9D02S}$	
2D03A = $\overline{9D03S}$	
2D04A = $\overline{9D04S}$	
2D05A = $\overline{9D05S}$	
2D06A = $\overline{9D06S}$	
9D01A = 2D01A 6DAPA	Sector counter signals to TMCC
9D02A = 2D02A 6DAPA	
9D03A = 2D03A 6DAPA	
9D04A = 2D04A 6DAPA	
9D05A = 2D05A 6DAPA	
9D06A = 2D06A 6DAPA	
6DAPA = 1X01A 1X02A	Disable outputs
2PT1A = 8PT1C	POT 1 signal (POT instruction in computer)
2PTQA = 6PTQA	
6PTQA = 8PT1C Q20C	POT 2 signal (T5 thru T1 of POT 1)
2RTIA = $\overline{9RTIC}$	Exit from PIN wait phase
2BUCA = 8BUCW	Buffer control mode
2W60A = 8W60W	Character transfer rate
2W50A = 8W50W	
3W90A = $\overline{8W90W}$	Read/write control
3W11A = $\overline{8W11W}$	
3W14A = $\overline{8W14W}$	
2C12A = 8C12C	
2C13A = 8C13W	
2C14A = 8C14W	
3C16A = $\overline{8C16W}$	Computer register signals
3C20A = $\overline{8C20W}$	
3C23A = $\overline{8C23W}$	
9ECWA = $\overline{6ECWA}$	Clock signal to TMCC
6ECWA = 201FA 3W50A 3W60A 2X03A 0X08A	Enable clock write mode
+ 202FA 3W50A 3W60A 0U04A J201	Enable clock read mode
J201 = 2DMWA 1X06A	
+ 2DMWA 1X09A 1U03A	
9WHSA = $\overline{6WHSA}$	Halt signal

(Continued)

Table 8-14. Logic Equations for Controller Input/Output Signals (Cont.)

Equation	Comment
6WHSA = 200FA 2DMWA	
+ 2U03A 2SIPA	
+ 1X03A 3BUCA	
9WESA = $\overline{6WESA}$	Error signal
6WESA = 0X04A	
+ 202FA 3PCPA 2CLKD 1K06A 1K07A	
+ 202FA 3PCPA 2CLKD 3U01A 3U02A 200MA	
9SIOA = $\overline{6SIOA}$	
6SIOA = 2DMAA 3C13A 2C14A 1E01A	
+ 2DMAA 2C13A 2C14A 9WLKS	
+ 2DMAA 3C13A 3C14A 1X03A $\overline{NUFA}$	
+ 2DMAA 3C13A 3C14A 1X03A $\overline{300FA}$	
9RTOA = $\overline{6RTOA}$	
6RTOA = 2PT1A 0X01A 6DAPA	
+ 1X01A 0X02A 9ENPS 6DAPA	
2W56A = $\overline{7W56A}$	
$\overline{7W56A}$ = $\overline{2W50A}$ $\overline{3W50A}$	

Table 8-15. Logic Equations for Sector Counter

Equation	Comment
sD01 = $\underline{0D02S}$	
rD01 = $\underline{0D02S}$	
tD01 = $\overline{3DRDS}$	
sD02 = $\underline{0D03S}$	
rD02 = $\underline{0D03S}$	
tD02 = $\overline{3DRDS}$	
sD03 = $\underline{0D04S}$	
rD03 = $\underline{0D04S}$	
tD03 = $\overline{3DRDS}$	
sD04 = $\underline{0D05S}$	
rD04 = $\underline{0D05S}$	
tD04 = $\overline{3DRDS}$	
sD05 = $\underline{0D06S}$	
rD05 = $\underline{0D06S}$	
tD05 = $\overline{3DRDS}$	
sD06 = $\underline{2SECS}$	
rD06 = $\underline{2SECS}$	

(Continued)

Table 8-15. Logic Equations for Sector Counter (Cont.)

Equation	Comment
tD06 = $\overline{3DRDS}$	
9CD1S = 0D01S 9USLA	Sector counter compare
9CD2S = 0D02S 9USLA	
9CD3S = 0D03S 9USLA	
9CD4S = 0D04S 9USLA	
9CD5S = 0D05S 9USLA	
9CD6S = 0D06S 9USLA	
9SIPS = 2SIPS 9USLA	
9D01S = 0D01S 3PSLS	Read sector counter for PIN operation
9D02S = 0D02S 3PSLS	
9D03S = 0D03S 3PSLS	
9D04S = 0D04S 3PSLS	
9D05S = 0D05S 3PSLS	
9D06S = 0D06S 3PSLS	
9ENPS = 2SIPS 3PSLS	
3PSLS = $\overline{8PSLA}$	

Table 8-16. Logic Equations for Address Circuits

Equation	Comment
Y01S = 0A11S 1A12S 1A13S 1A14S 1A15S	
Y02S = 1A11S 1A12S 1A13S 1A14S 0A15S	Y02
Y03S = 1A11S 1A12S 1A13S 0A14S 1A15S	
Y04S = 1A11S 1A12S 1A13S 0A14S 0A15S	
Y05S = 1A11S 1A12S 0A13S 1A14S 1A15S	
Y06S = 1A11S 1A12S 0A13S 1A14S 0A15S	
Y07S = 1A11S 1A12S 0A13S 0A14S 1A15S	
Y08S = 1A11S 1A12S 0A13S 0A14S 0A15S	
Y09S = 1A11S 0A12S 1A13S 1A14S 1A15S	
Y10S = 1A11S 0A12S 1A13S 1A14S 0A15S	
Y11S = 1A11S 0A12S 1A13S 0A14S 1A15S	
Y12S = 1A11S 0A12S 1A13S 0A14S 0A15S	
Y13S = 1A11S 0A12S 0A13S 1A14S 1A15S	
Y14S = 1A11S 0A12S 0A13S 1A14S 0A15S	
Y15S = 1A11S 0A12S 0A13S 0A14S 1A15S	
Y16S = 1A11S 0A12S 0A13S 0A14S 0A15S	
Y17S = 0A11S 1A12S 1A13S 1A14S 1A15S	
Y18S = 0A11S 1A12S 1A13S 1A14S 0A15S	
Y19S = 0A11S 1A12S 1A13S 0A14S 1A15S	
Y20S = 0A11S 1A12S 1A13S 0A14S 0A15S	
Y21S = 0A11S 1A12S 0A13S 1A14S 1A15S	
Y22S = 0A11S 1A12S 0A13S 1A14S 0A15S	
Y23S = 0A11S 1A12S 0A13S 0A14S 1A15S	
Y24S = 0A11S 1A12S 0A13S 0A14S 0A15S	
Y25S = 0A11S 0A12S 1A13S 1A14S 1A15S	
Y26S = 0A11S 0A12S 1A13S 1A14S 0A15S	
Y27S = 0A11S 0A12S 1A13S 0A14S 1A15S	
Y28S = 0A11S 0A12S 1A13S 0A14S 0A15S	
Y29S = 0A11S 0A12S 0A13S 1A14S 1A15S	
Y30S = 0A11S 0A12S 0A13S 1A14S 0A15S	
Y31S = 0A11S 0A12S 0A13S 0A14S 1A15S	
Y32S = 0A11S 0A12S 0A13S 0A14S 0A15S	
SP01 = Y01S Y02S	
SP02 = Y03S Y04S	
SP03 = Y05S Y06S	
SP04 = Y07S Y08S	
SP05 = Y09S Y10S	
SP06 = Y11S Y12S	
SP07 = Y13S Y14S	
SP08 = Y15S Y16S	
SP09 = Y17S Y18S	
SP10 = Y19S Y20S	
SP11 = Y21S Y22S	
SP12 = Y23S Y24S	
SP13 = Y25S Y26S	
SP14 = Y27S Y28S	
SP15 = Y29S Y30S	
SP16 = Y31S Y32S	
sA11 = 8A11A 1YSCS	
rA11 = 1YSCS	
tA11 = 3SIMS	
sA12 = 8A12A 1YSCS	
rA12 = 1YSCS	
tA12 = 3SIMS	

(Continued)

Table 8-16. Logic Equations for Address Circuits (Cont.)

Equation	Comment
sA13 = 8A13A 1YSCS rA13 = 1YSCS tA13 = 3SIMS sA14 = 8A14A 1YSCS rA14 = 1YSCS tA14 = 3SIMS sA15 = 8A15A 1YSCS rA15 = 1YSCS tA15 = 3SIMS sYSC = 3SIMS 0WCKS rYSC = 2SECS 2WCAS tYSC = 3IDXS 3SIMS = 3SECS 3IDXS $\overline{3A16A}$ = 8A16A $\overline{3A17A}$ = 8A17A	

Table 8-17. Logic Equations for Read/Write Control Circuits

Equation	Comment
sWDE1 = 2WD1S 1WCKS 2WCAS + 0WCKS 2WCAS rWDE1 = 9WDIA 1WCKS 2WCAS + 0WCKS 2WCAS sWDE2 = 2WD2S 1WCKS 2WCAS + 0WCKS 2WCAS rWDE2 = 9WD2A 1WCKS 2WCAS + 0WCKS 2WCAS sWDE3 = 2WD3S 1WCKS 2WCAS + 0WCKS 2WCAS rWDE3 = 9WD3A 1WCKS + 0WCKS 2WCAS sWDE4 = 2WD4S 1WCKS + 0WCKS 2WCAS rWDE4 = 9WD4A 1WCKS + 0WCKS 2WCAS $\overline{2WD1S}$ = 9WD1A 3SECS $\overline{2WD2S}$ = 9WD2A 3SECS $\overline{2WD3S}$ = 9WD3A 3SECS $\overline{2WD4S}$ = 9WD4A 3SECS	

Similarly, the following signals (see figure 8-9 and table 8-8):

$$2AINA = 6AINA$$

$$6AINA = 2RF1A\ 3AFLA\ 2CLKA + 201FA\ 3AFLA\ 201UA\ 2LSCA\ 2K06A\ 2CLKA$$

simplify to:

$$AIN = RF1\ \overline{AFL}\ CLK + 01F\ \overline{AFL}\ 01U\ LSC\ K06\ CLK$$

and the following signals (see figure 8-15 and table 8-14):

$$2W56A = \overline{7W56A}$$
$$\overline{7W56A} = \overline{2W50A}\ \overline{3W60A}$$

simplify to:

$$W56 = \overline{W50}\ W60$$

Flip-flops may have inputs independent of triggered gating inputs, and may also be controlled by connecting flip-flop outputs to ground. For a detailed description of these operations, refer to SDS publication 64-55-14. Special inputs which set flip-flops are indicated in the logic diagrams by an input at the top of the flip-flop symbol and indicated in the corresponding equations by a lower case y prefix. Special inputs which reset flip-flops are indicated in the logic diagrams by an input at the bottom of the flip-flop symbol and in the corresponding equations by a lower case z prefix. Thus, in the following equations (figure 8-11):

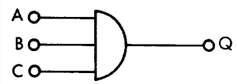
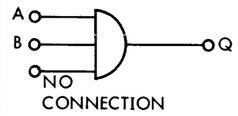
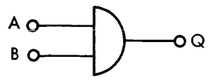
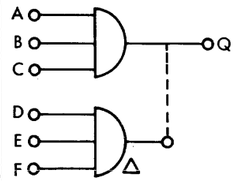
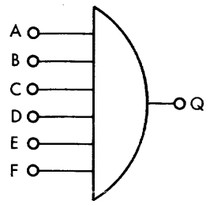
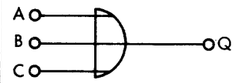
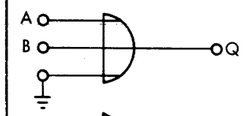
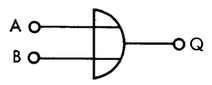
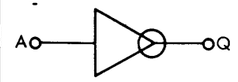
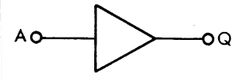
$$yU02 = 200FA\ 0BSCA\ 2SACA\ 2HSDA$$

$$sU02 = 200FA\ 2U01A\ 1U03A\ 200MA\ \underline{4CLKA}$$

$$rU02 = 200FA\ 0K05A\ \underline{4CLKA}$$

$$zU02 = \overline{3DRAA}$$

flip-flop U02 may be set by either of the first two sets of conditions, or reset by either of the second two sets of conditions.

SDS DRAWING SYMBOL	NAME	SIMPLIFIED SYMBOL	LOGIC EQUATION
	AND GATE	SAME	Q = ABC
	AND GATE, ONE TERMINAL UNUSED		Q = AB
	AND GATE, WITH EXTENDER AND GATE		Q = ABCDEF
	OR GATE	SAME	Q = A + B + C
	OR GATE, ONE TERMINAL UNUSED		Q = A + B
	INVERTER	SAME	$Q = \overline{A}$
	BUFFER AMPLIFIER	SAME	Q = A

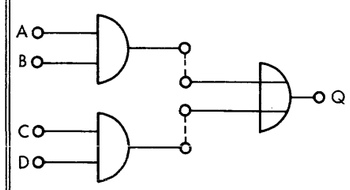
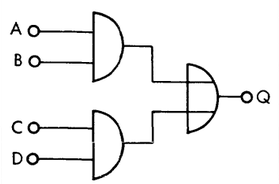
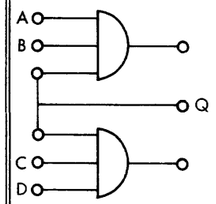
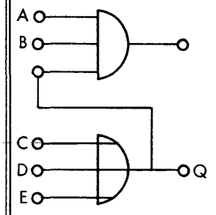
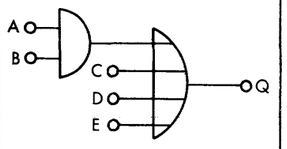
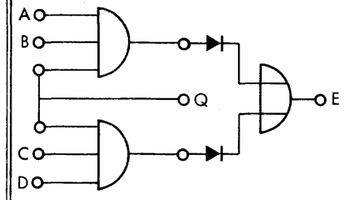
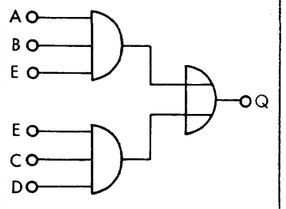
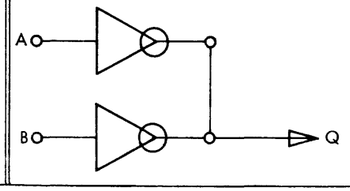
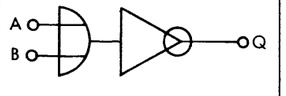
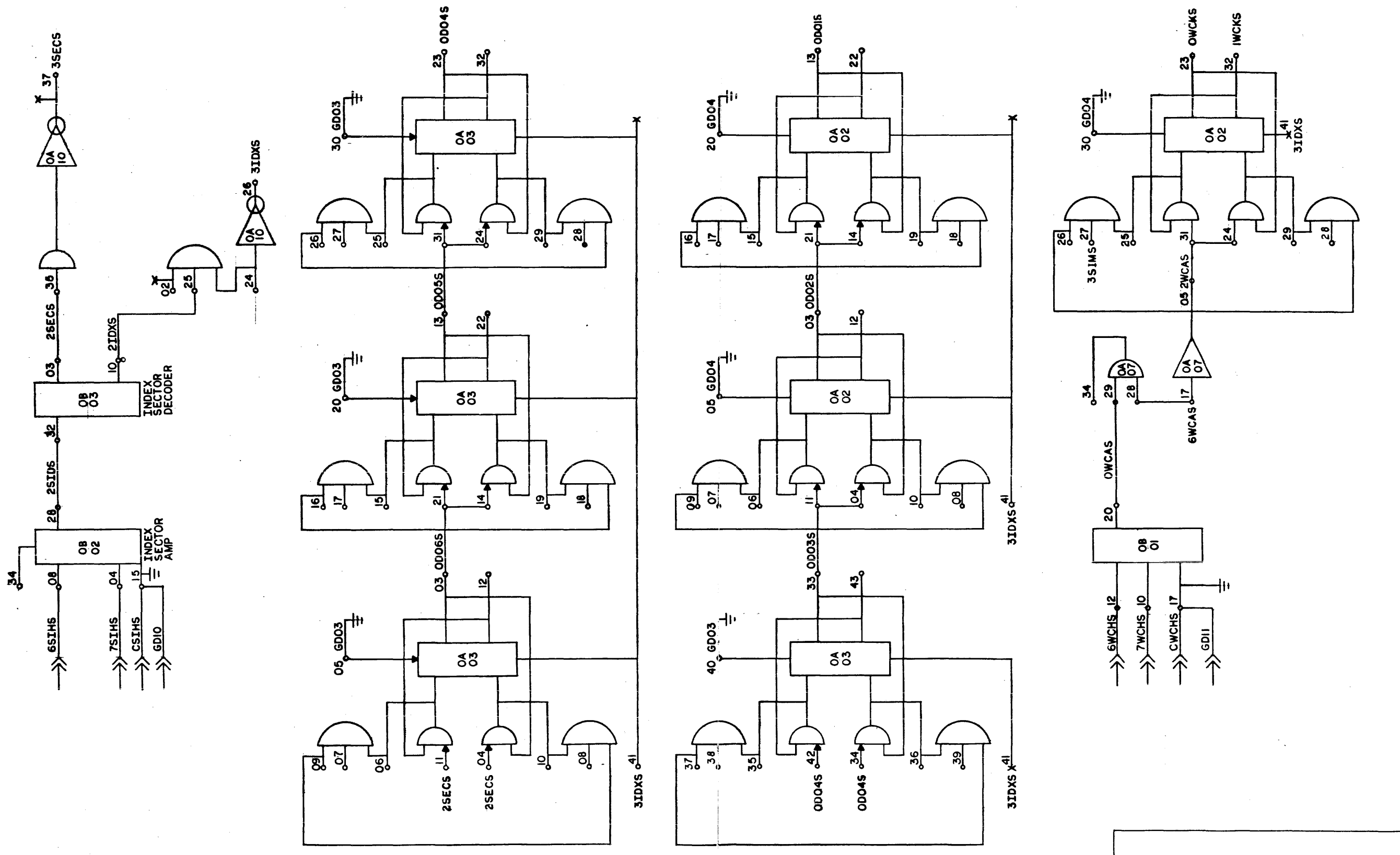
SDS DRAWING SYMBOL	NAME	SIMPLIFIED SYMBOL	LOGIC EQUATION
	GATED INPUT OR GATE		Q = (AB) + (CD)
	PHANTOM OR GATE	SAME AS ABOVE	Q = (AB) + (CD)
	--		Q = (AB) + C + D + E
	--		Q = E [(AB) + (CD)]
	NOR GATE USING INVERTING AMPLIFIERS		$Q = \overline{A + B}$

Figure 8-1. Logic Symbols

901034A.700



NOTE: REFERENCE SDS DWG: 131614-5A

Figure 8-2. Selection Unit Timing Circuits Logic Diagram (Sheet 1 of 2)

901029A.801/1

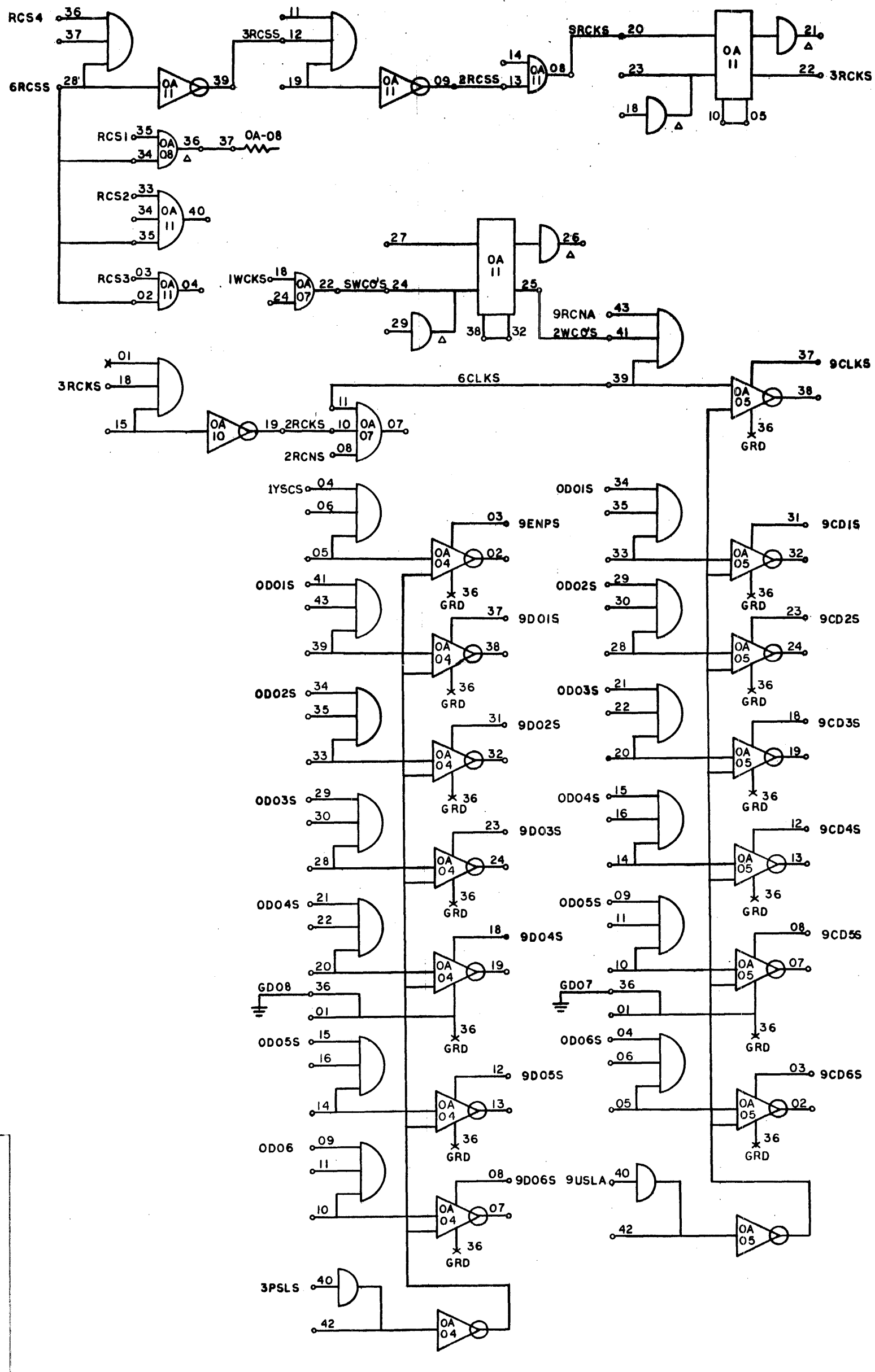


Figure 8-2. Selection Unit Timing Circuits
Logic Diagram (Sheet 2 of 2)
901029A.801/2

NOTE: REFERENCE SDS DWG: 131614-6A

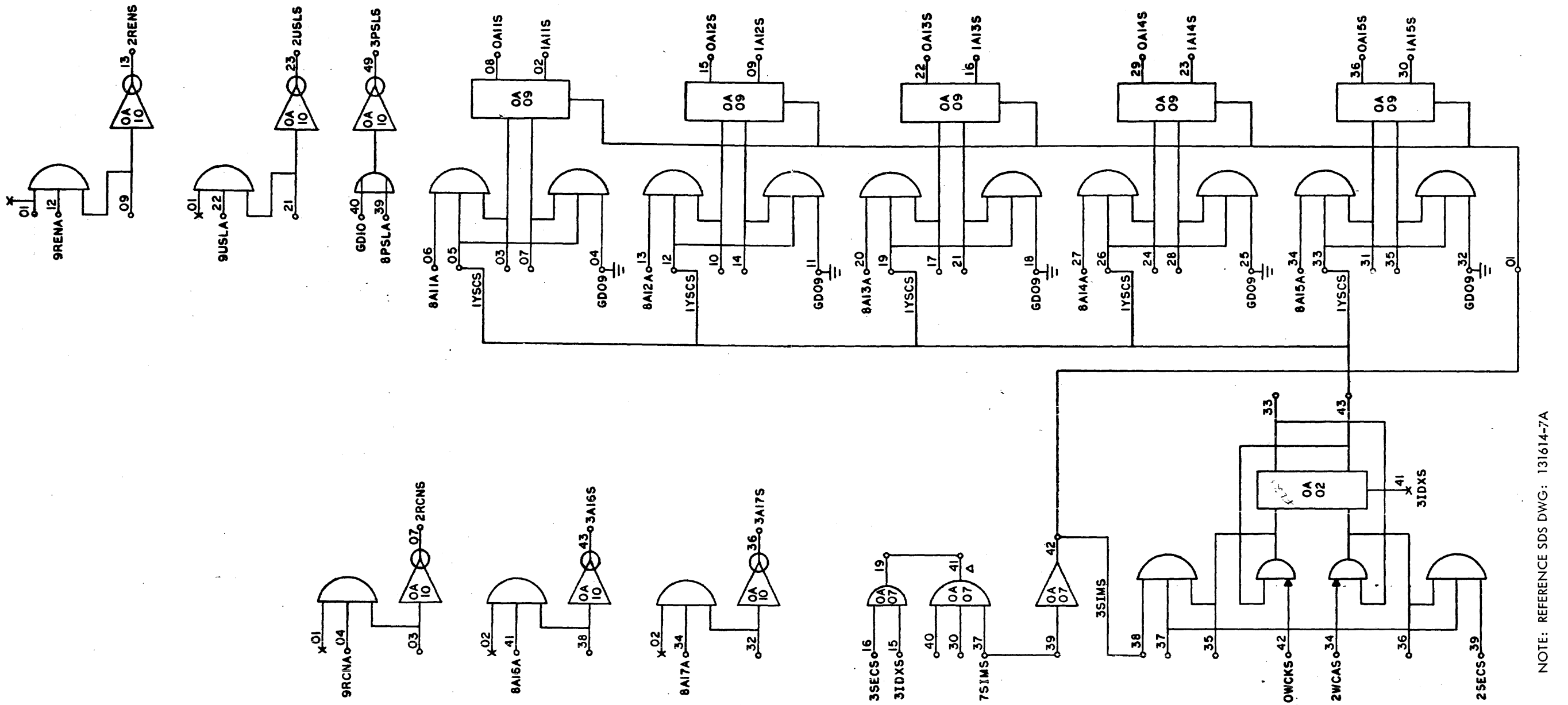


Figure 8-3. Selection Unit Address Circuits Logic Diagram (Sheet 1 of 3)
901029A.802/1

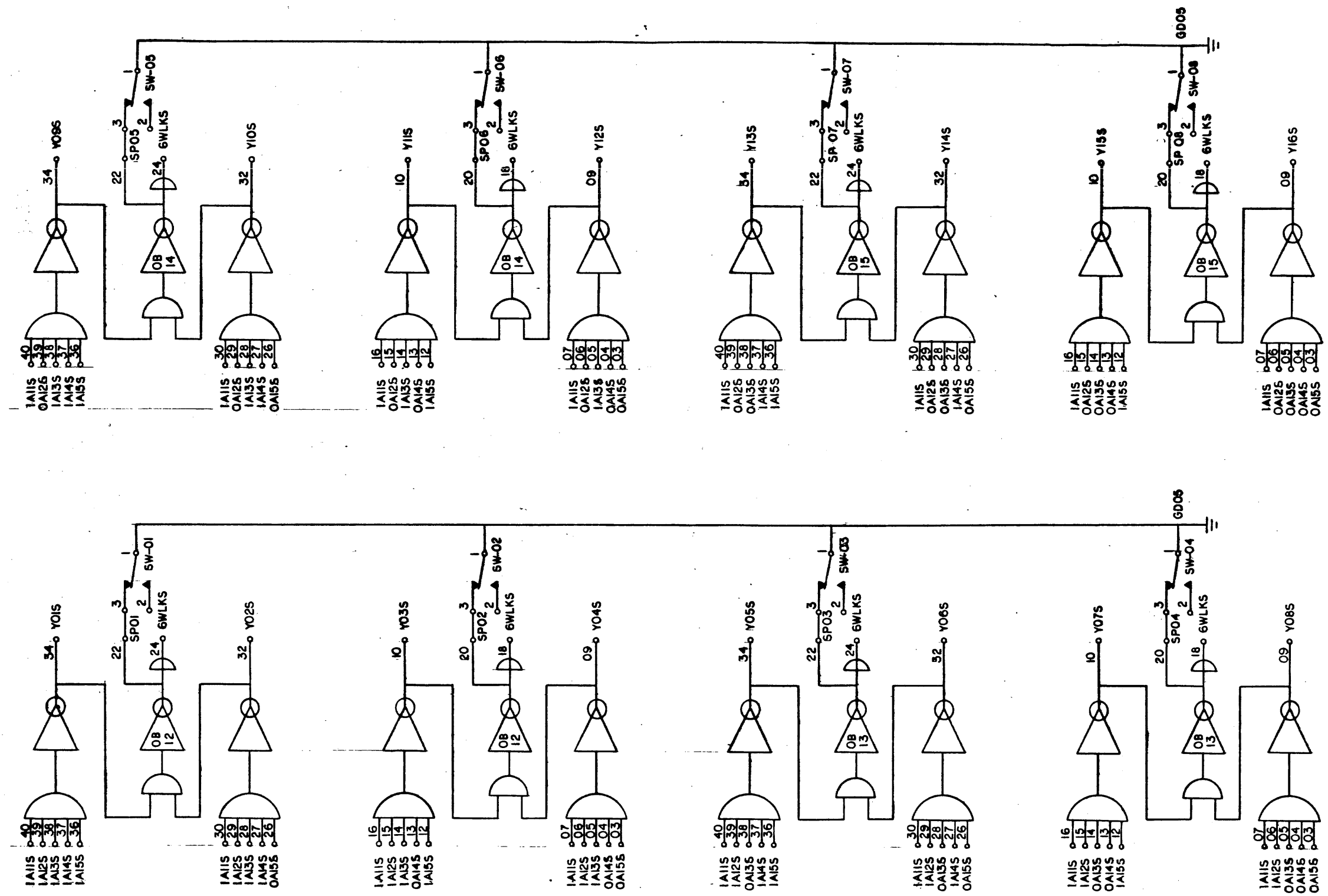


Figure 8-3. Selection Unit Address Circuits Logic Diagram (Sheet 2 of 3)

901029A.802/2

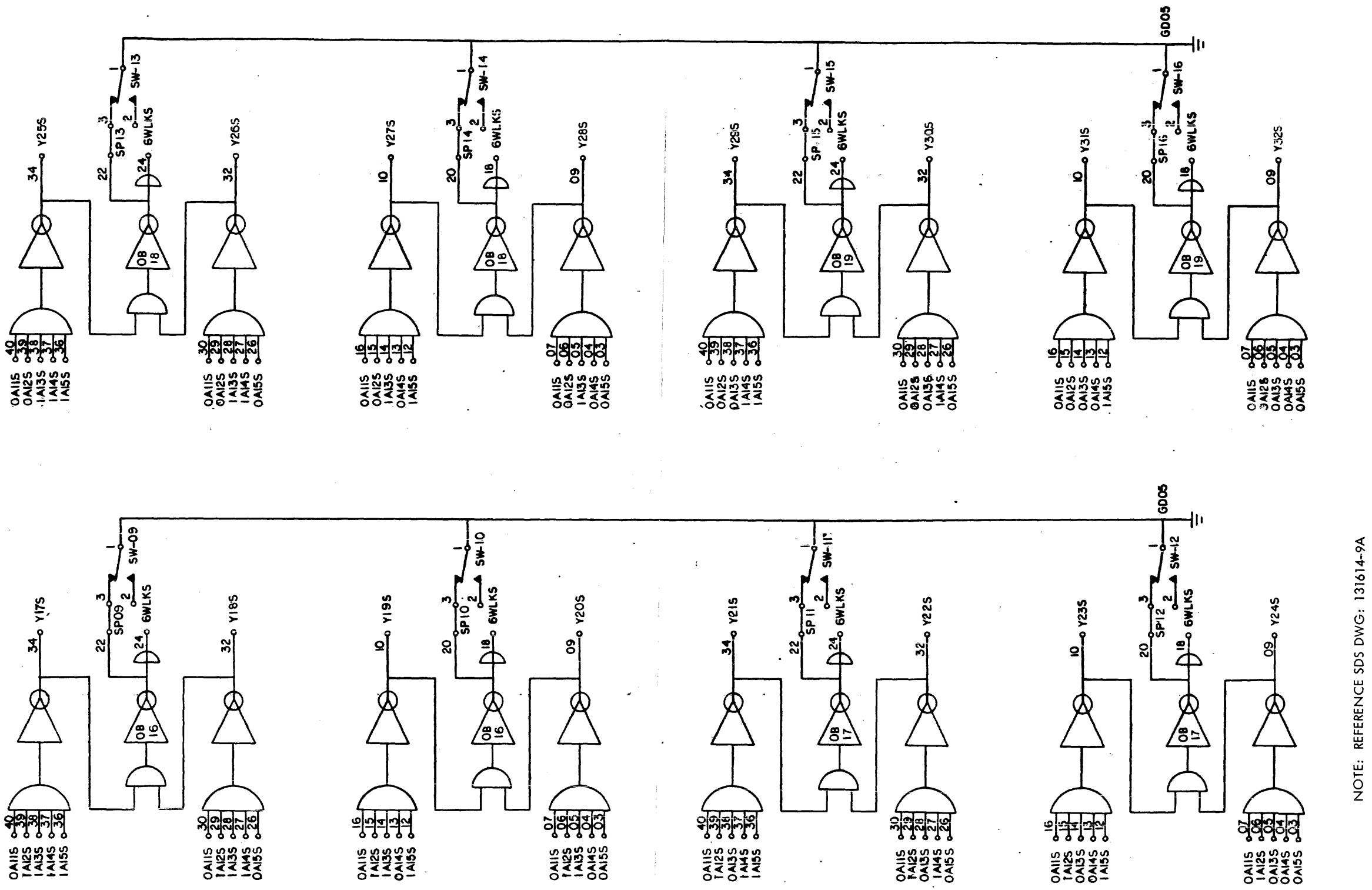


Figure 8-3. Selection Unit Address Circuits Logic Diagram (Sheet 3 of 3)

901029A.802/3

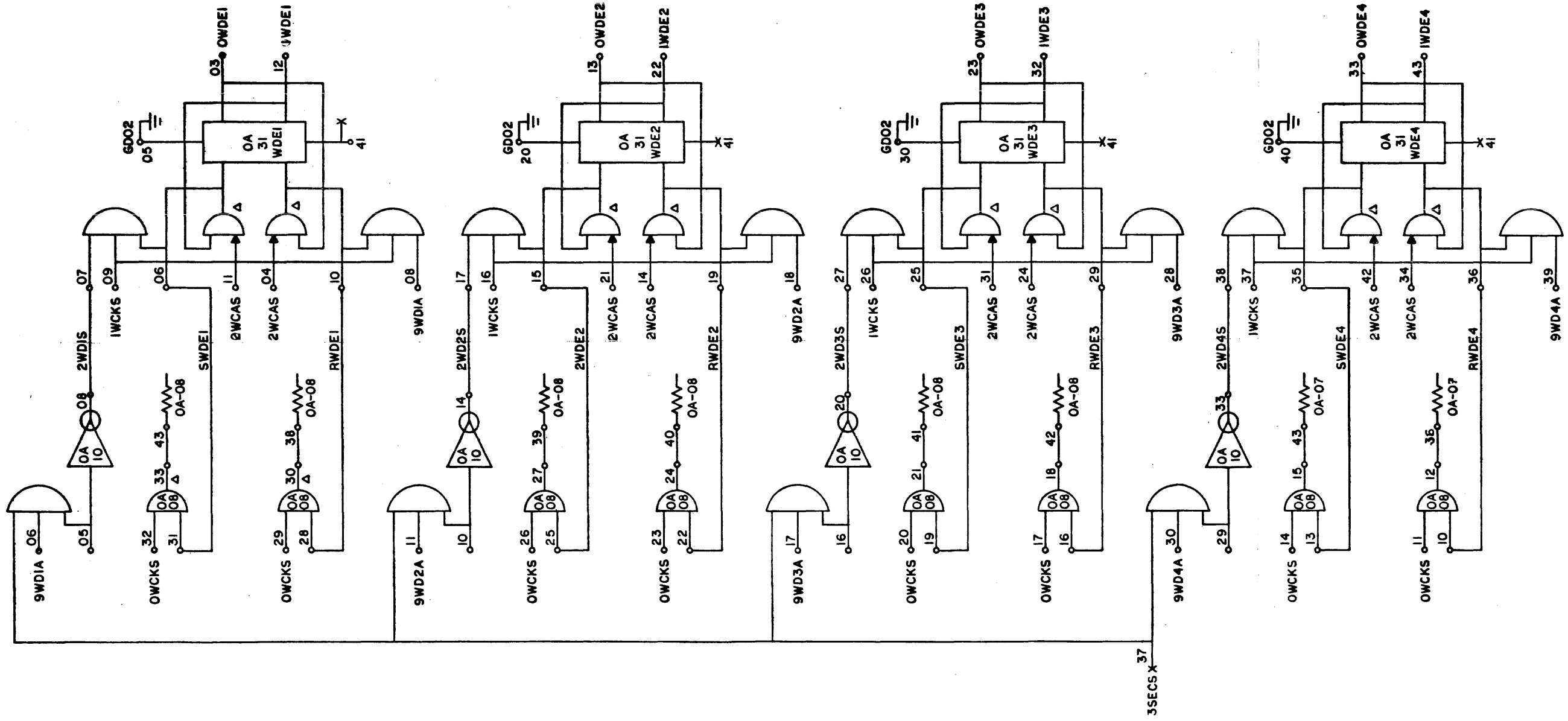


Figure 8-4. Selection Unit Read/Write Control Circuits Logic Diagram (Sheet 1 of 5)

901029A.803/1

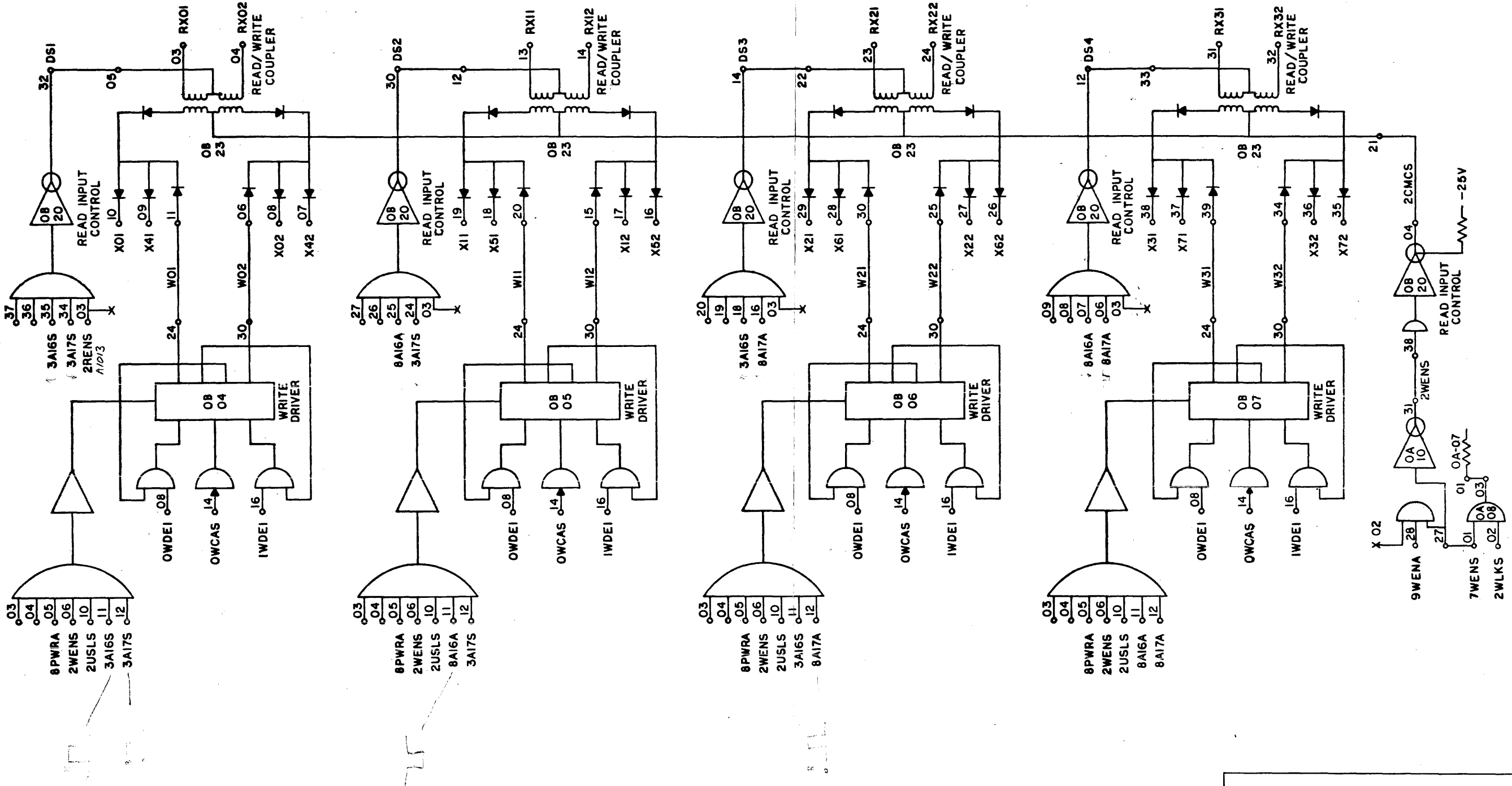
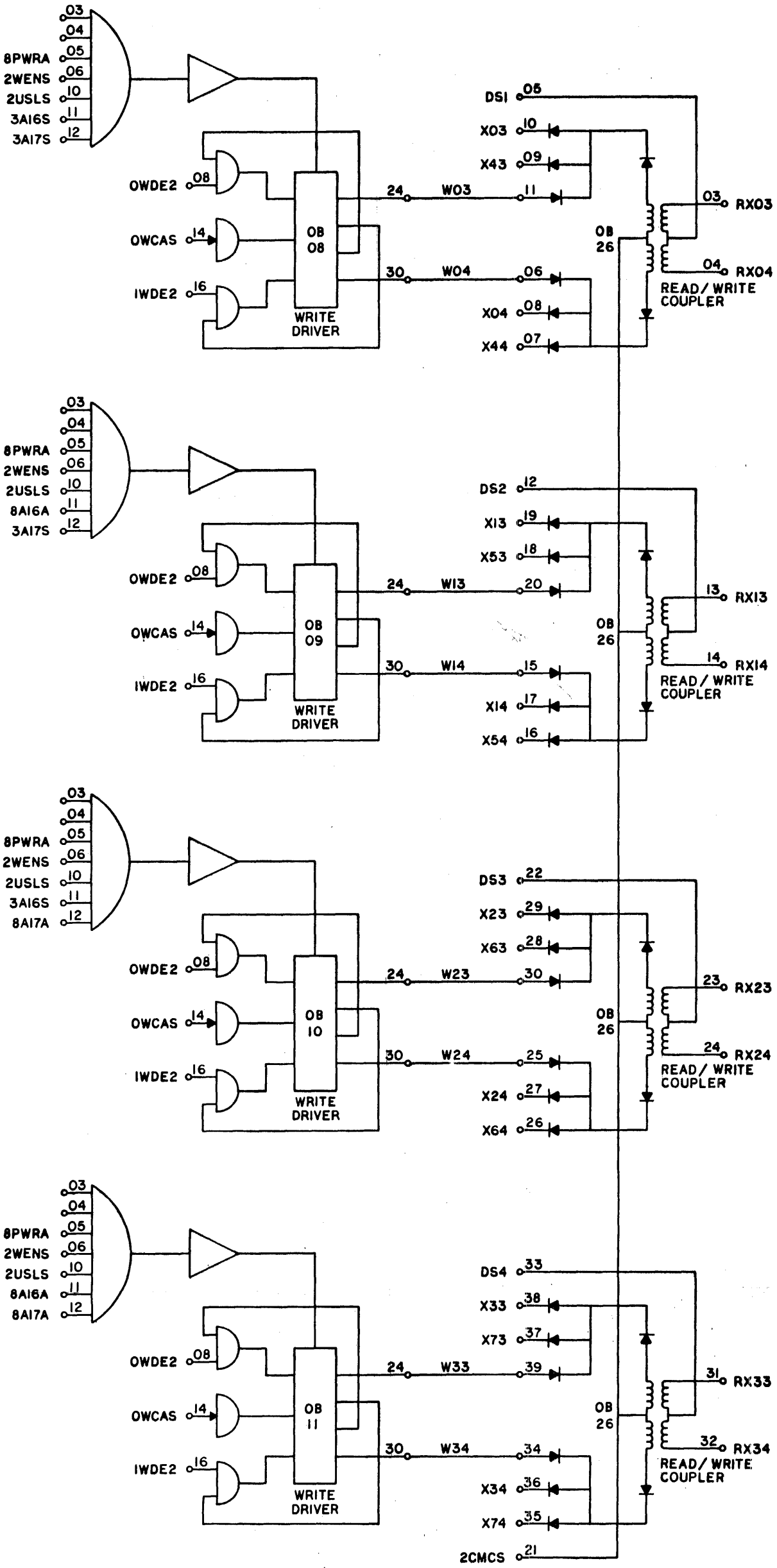


Figure 8-4. Selection Unit Read/Write Control Circuits Logic Diagram (Sheet 2 of 5)
901029A, 803/2



NOTE: REFERENCE SDS DWG: 131614-13A

Figure 8-4. Selection Unit Read/Write Control Circuits Logic Diagram (Sheet 3 of 5)
901029A.803/3

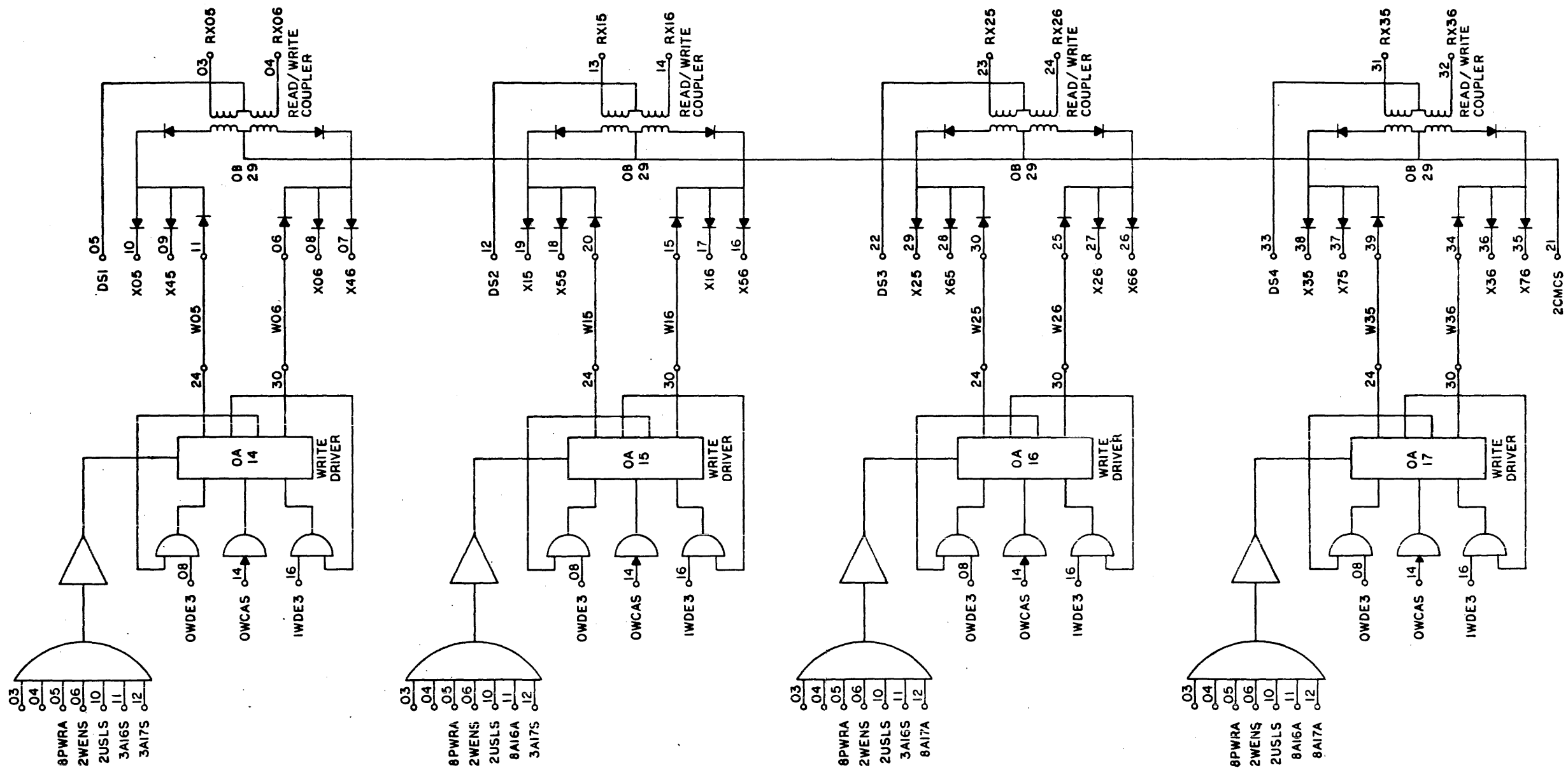
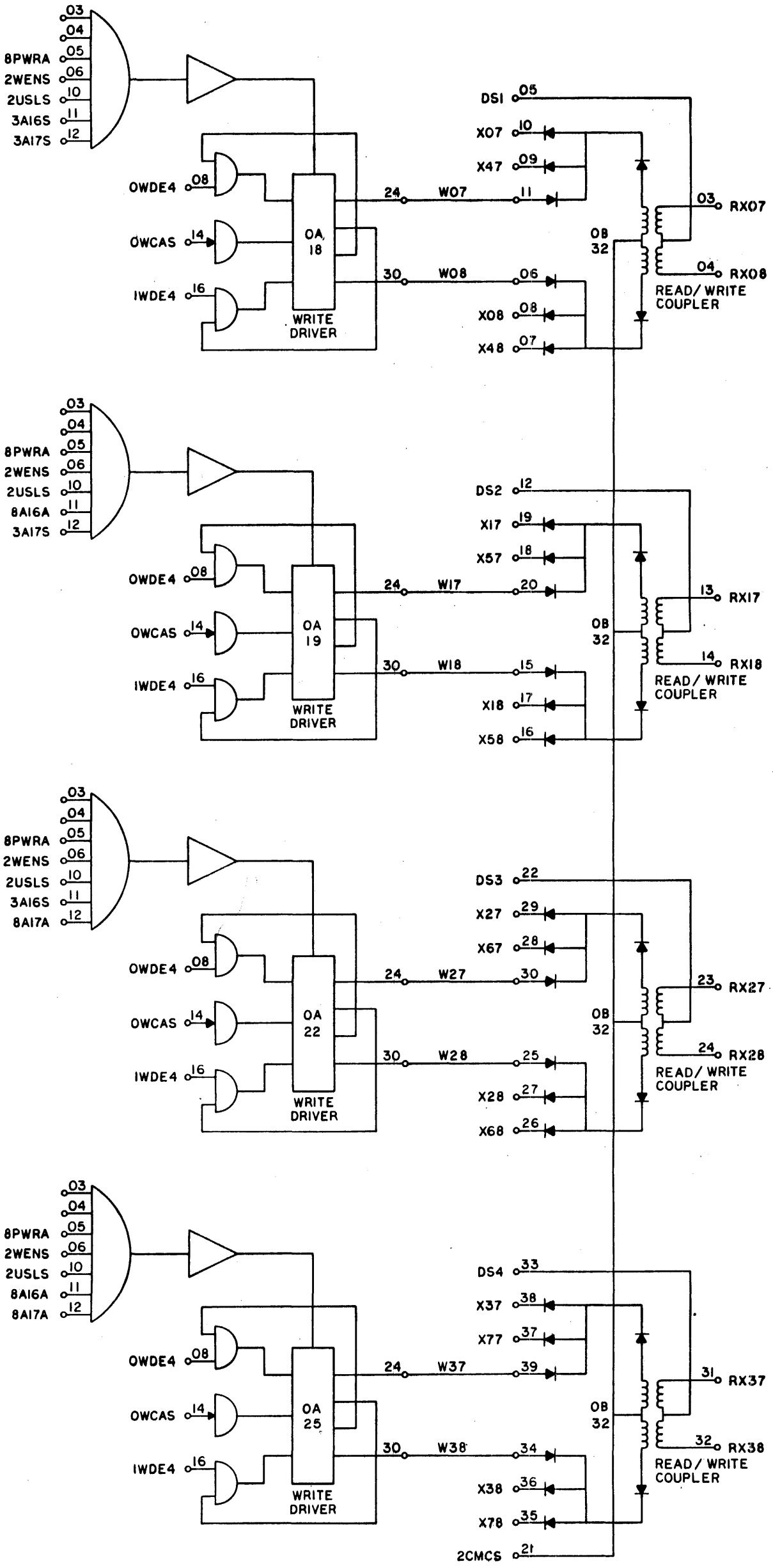


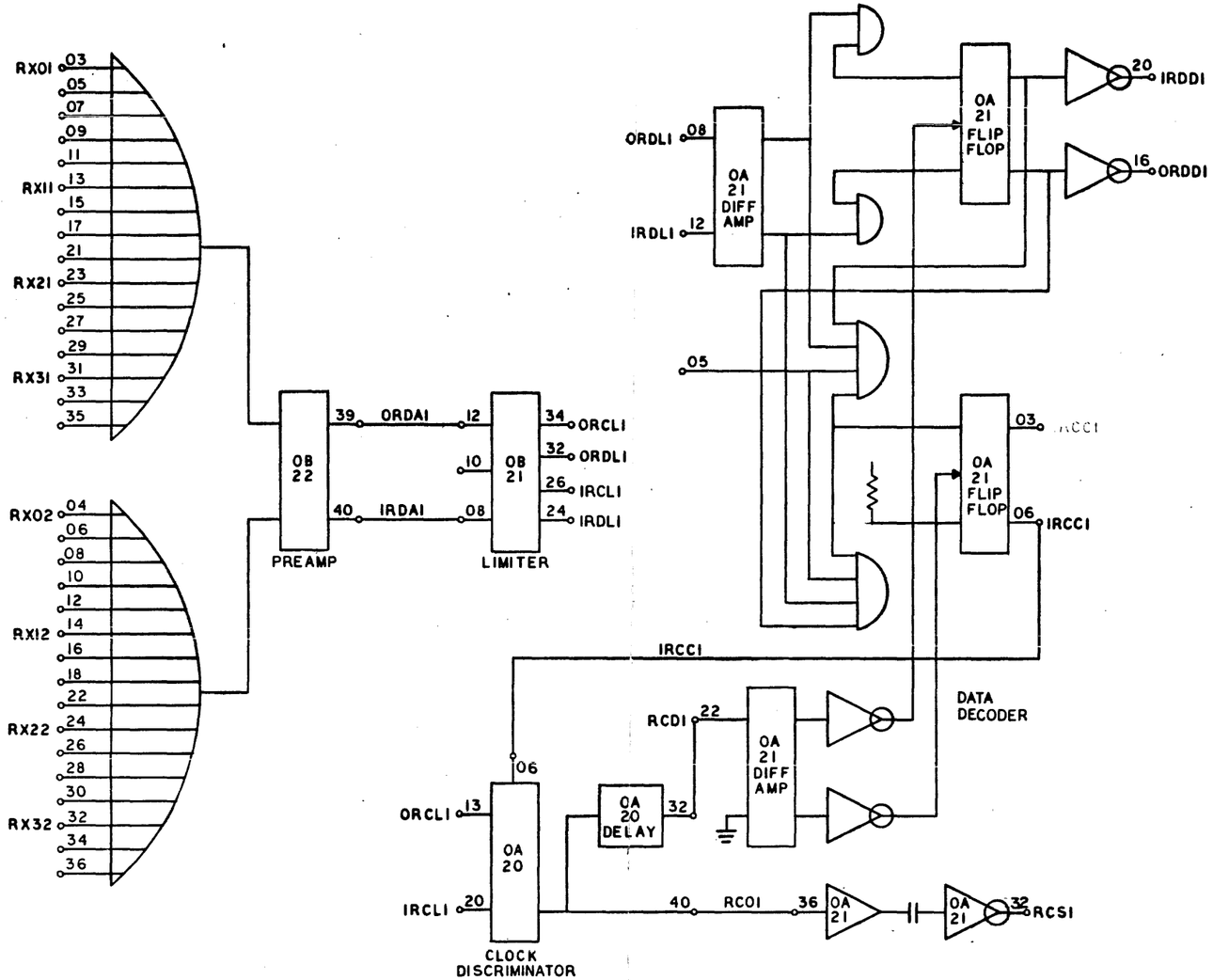
Figure 8-4. Selection Unit Read/Write Control Circuits Logic Diagram (Sheet 4 of 5)

901029A. 803/4



NOTE: REFERENCE SDS DWG: 131614-17A

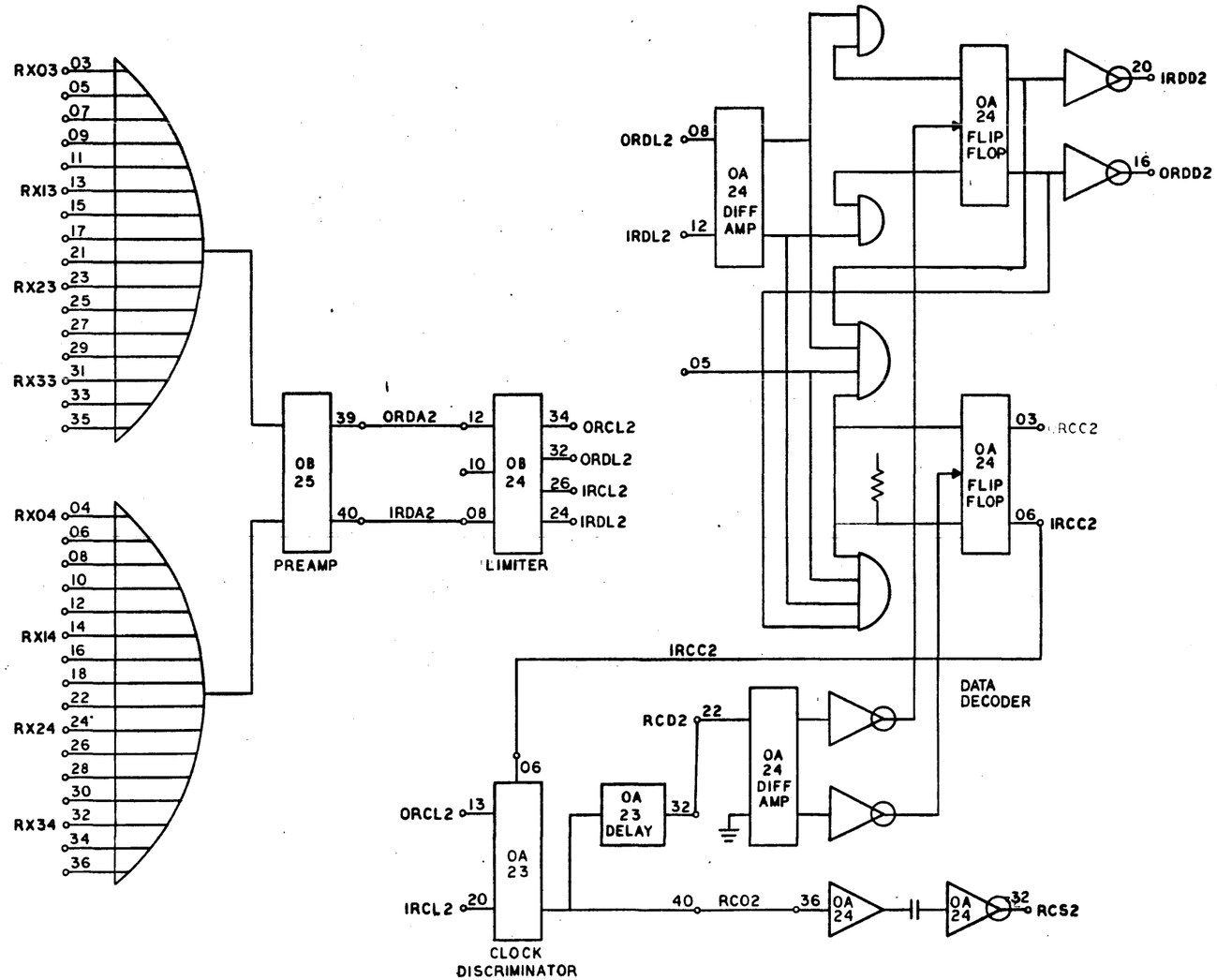
Figure 8-4. Selection Unit Read/Write Control Circuits Logic Diagram (Sheet 5 of 5)
901029A.803/5



NOTE: REFERENCE SDS DWG: 131614-12A

Figure 8-5. Selection Unit Read Output Circuits Logic Diagram (Sheet 1 of 5)

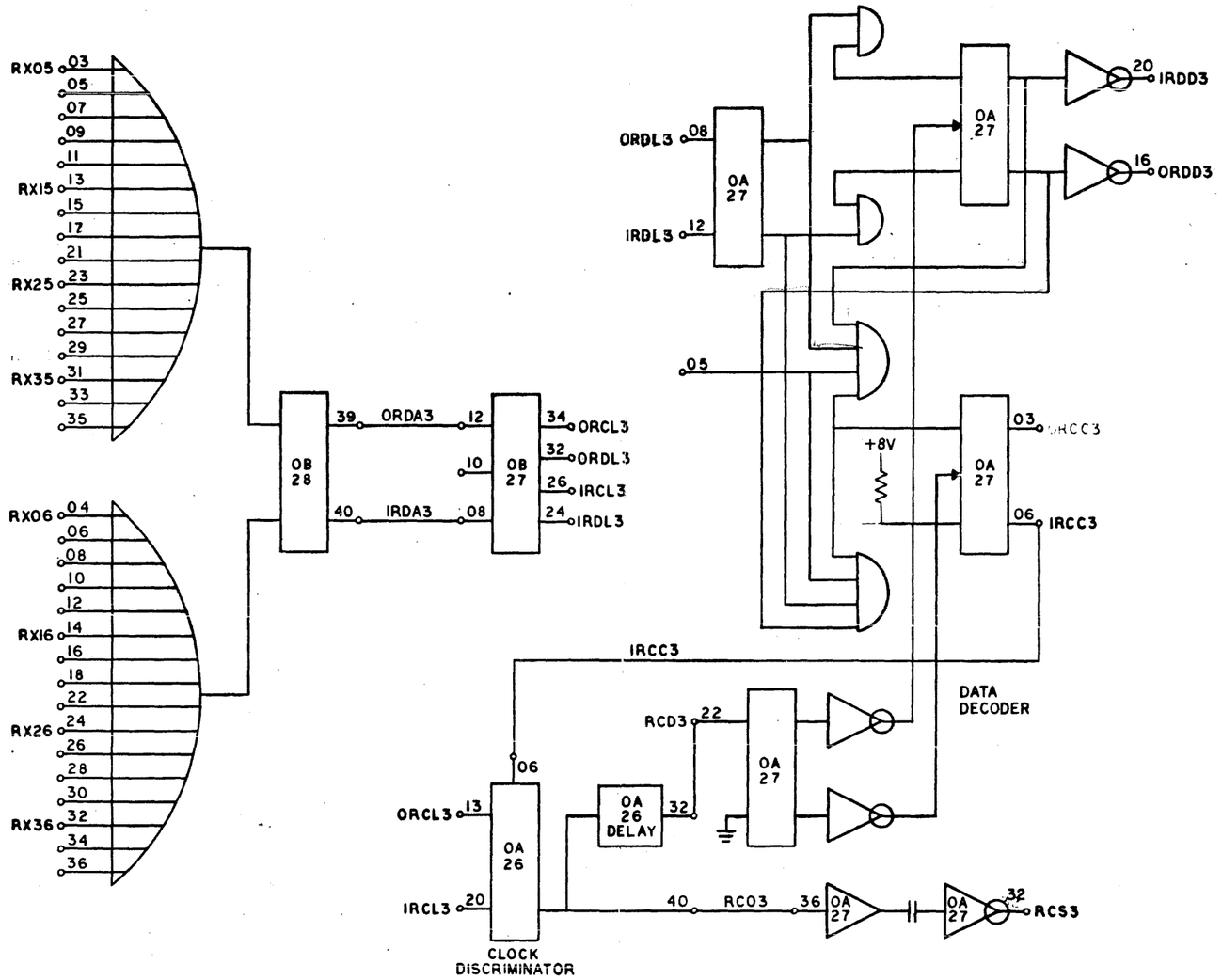
901029A.804/1



NOTE: REFERENCE SDS DWG. 101614-14A

Figure 8-5. Selection Unit Read Output Circuits Logic Diagram (Sheet 2 of 5)

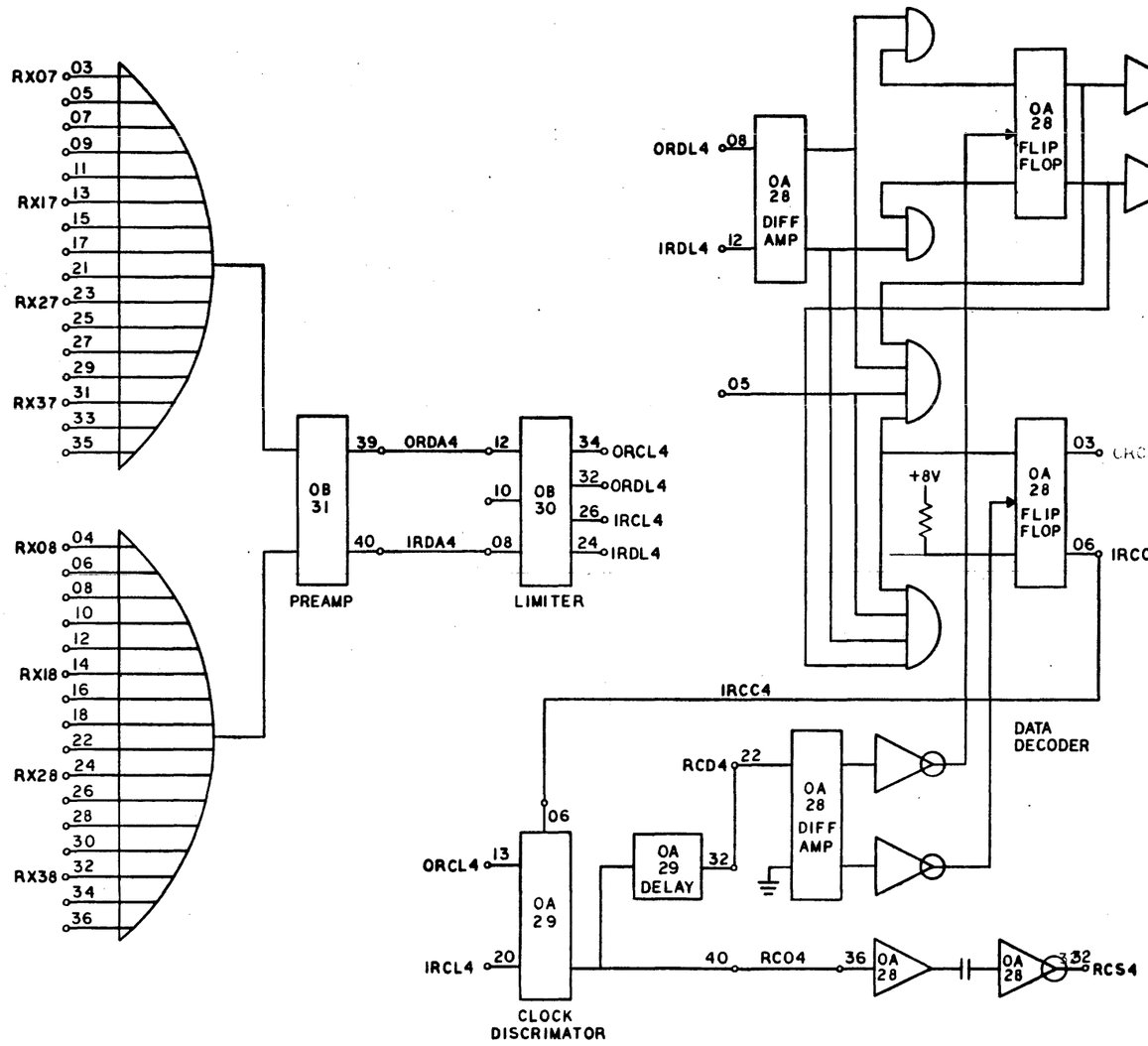
901029A.804/2



NOTE: REFERENCE SDS DWG: 131614-16A

Figure 8-5. Selection Unit Read Output Circuits Logic Diagram (Sheet 3 of 5)

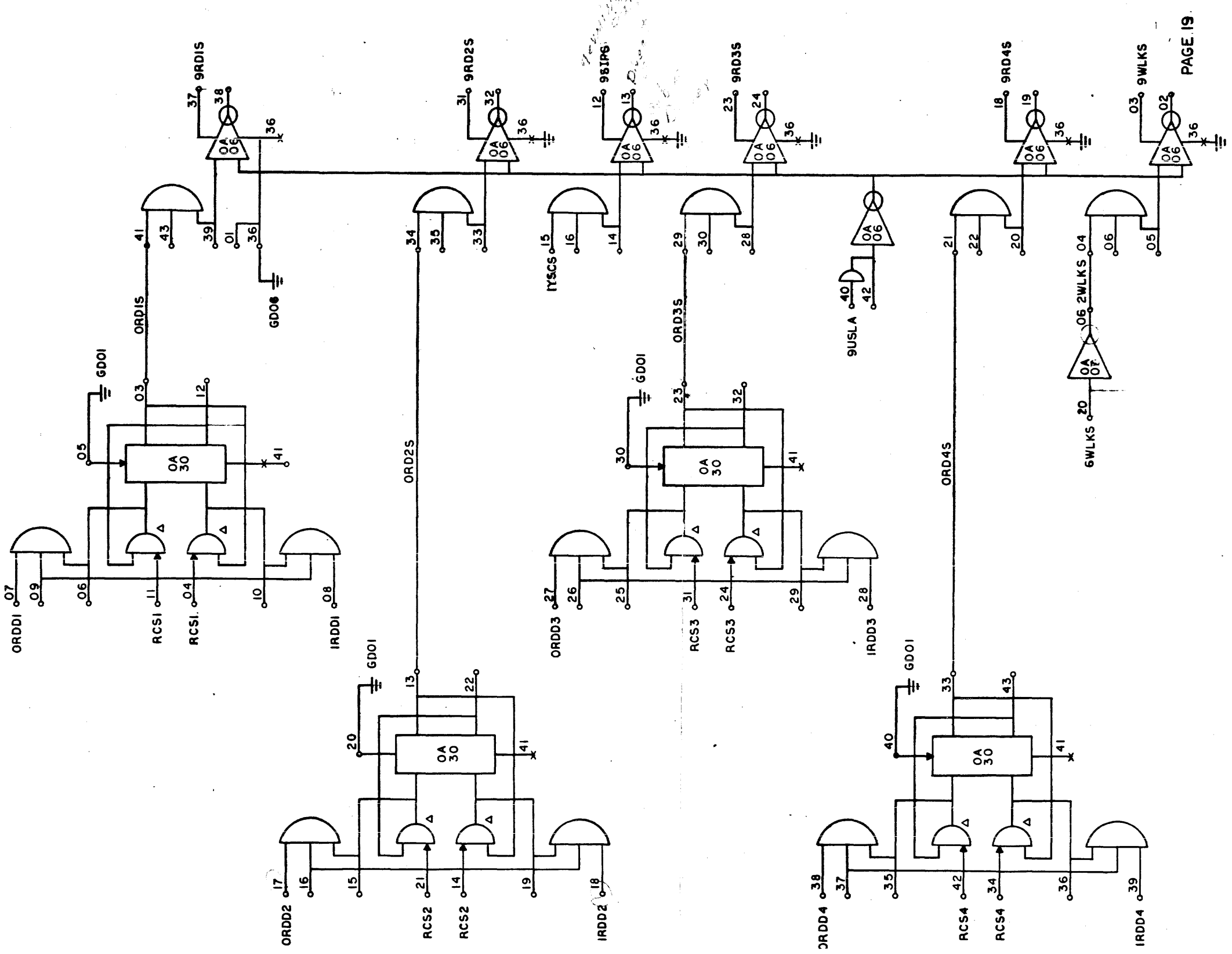
901029A.804/3



NOTE: REFERENCE SDS DWG: 131614-18A

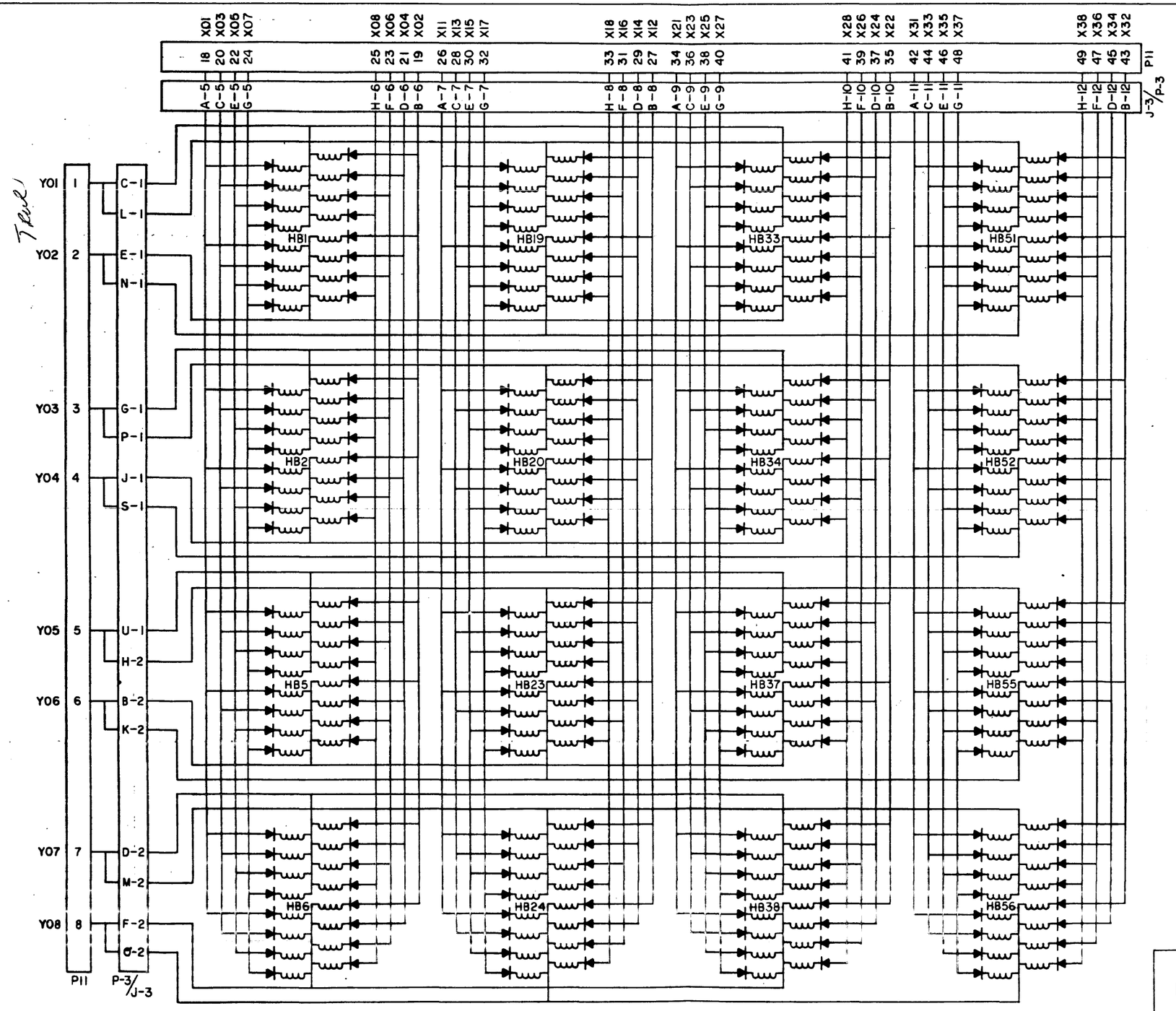
Figure 8-5. Selection Unit Read Output Circuits Logic Diagram (Sheet 4 of 5)

901029A.804/4



NOTE: REFERENCE SDS DWG: 131614-19A

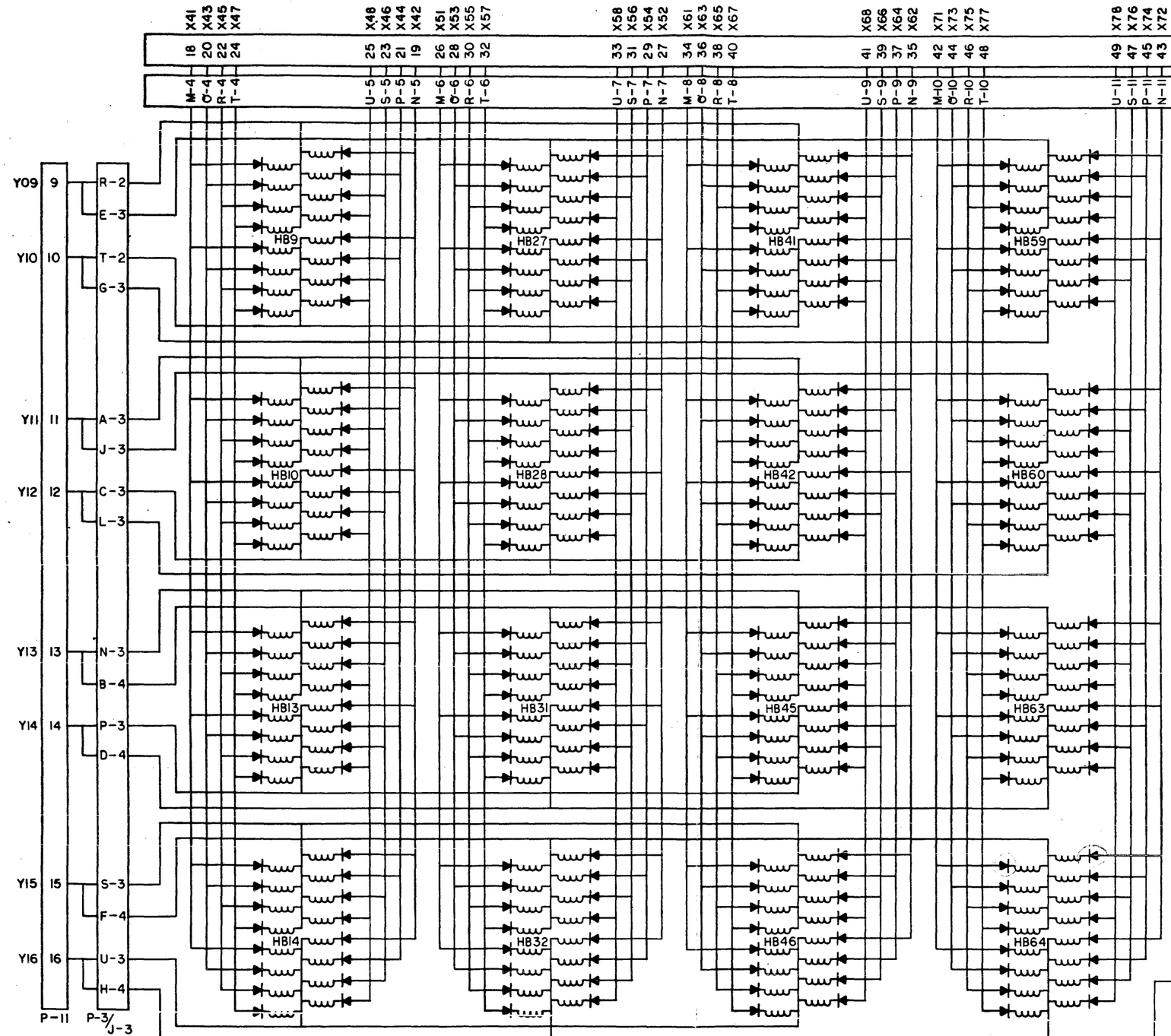
Figure 8-5. Selection Unit Read Output Circuits Logic Diagram (Sheet 5 of 5)
901029A.804/5



NOTE: REFERENCE SDS DWG: 131614-20A

Figure 8-6. Selection Unit Memory Circuits Logic Diagram (Sheet 1 of 3)

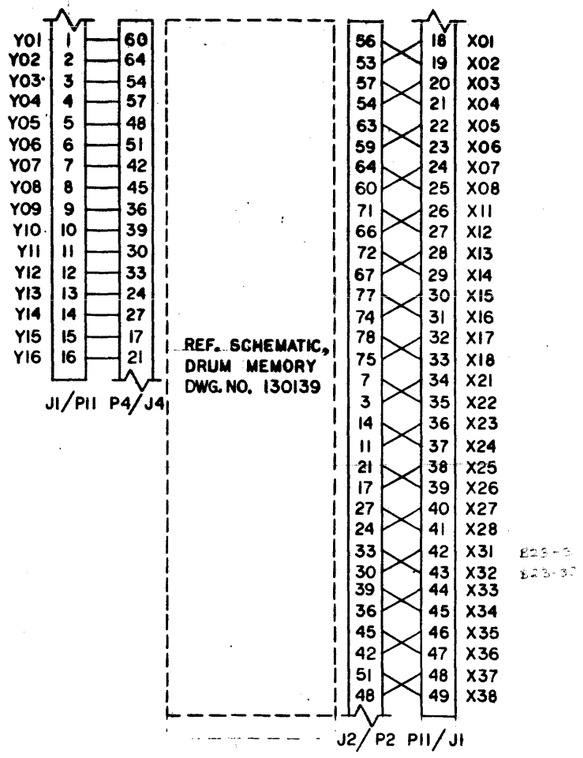
901029A.805/1

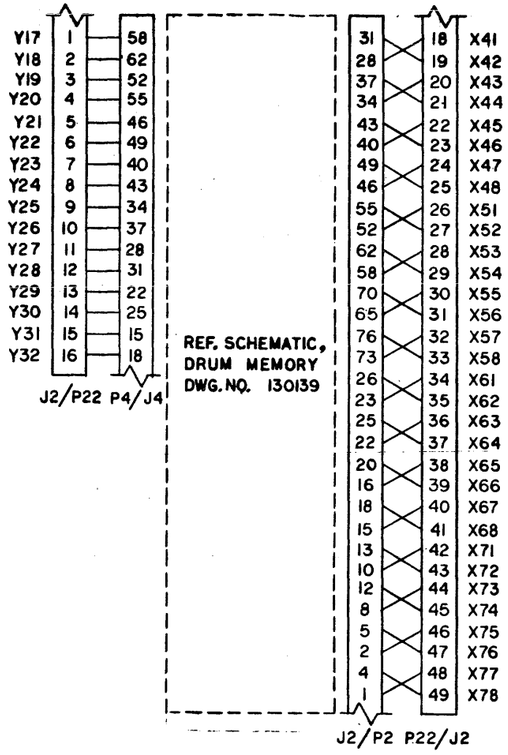


NOTE: REFERENCE SDS DWG: 131614-21A

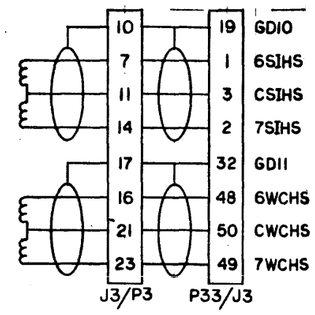
Figure 8-6. Selection Unit Memory Circuits Logic Diagram (Sheet 2 of 3)

901029A.805/2

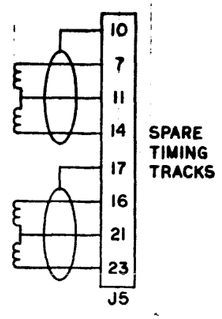


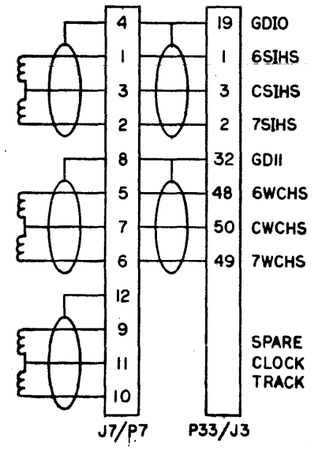


DRUM MEMORY

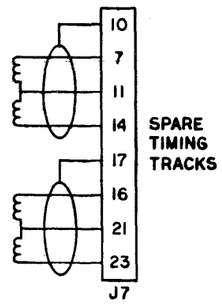


DRUM TIMING TRACKS





DISC TIMING TRACKS



DRUM TIMING TRACKS

NOTE: REFERENCE SDS DWG: 131614-22A

Figure 8-6. Selection Unit Memory Circuits Logic Diagram (Sheet 3 of 3)

901029A.805/3

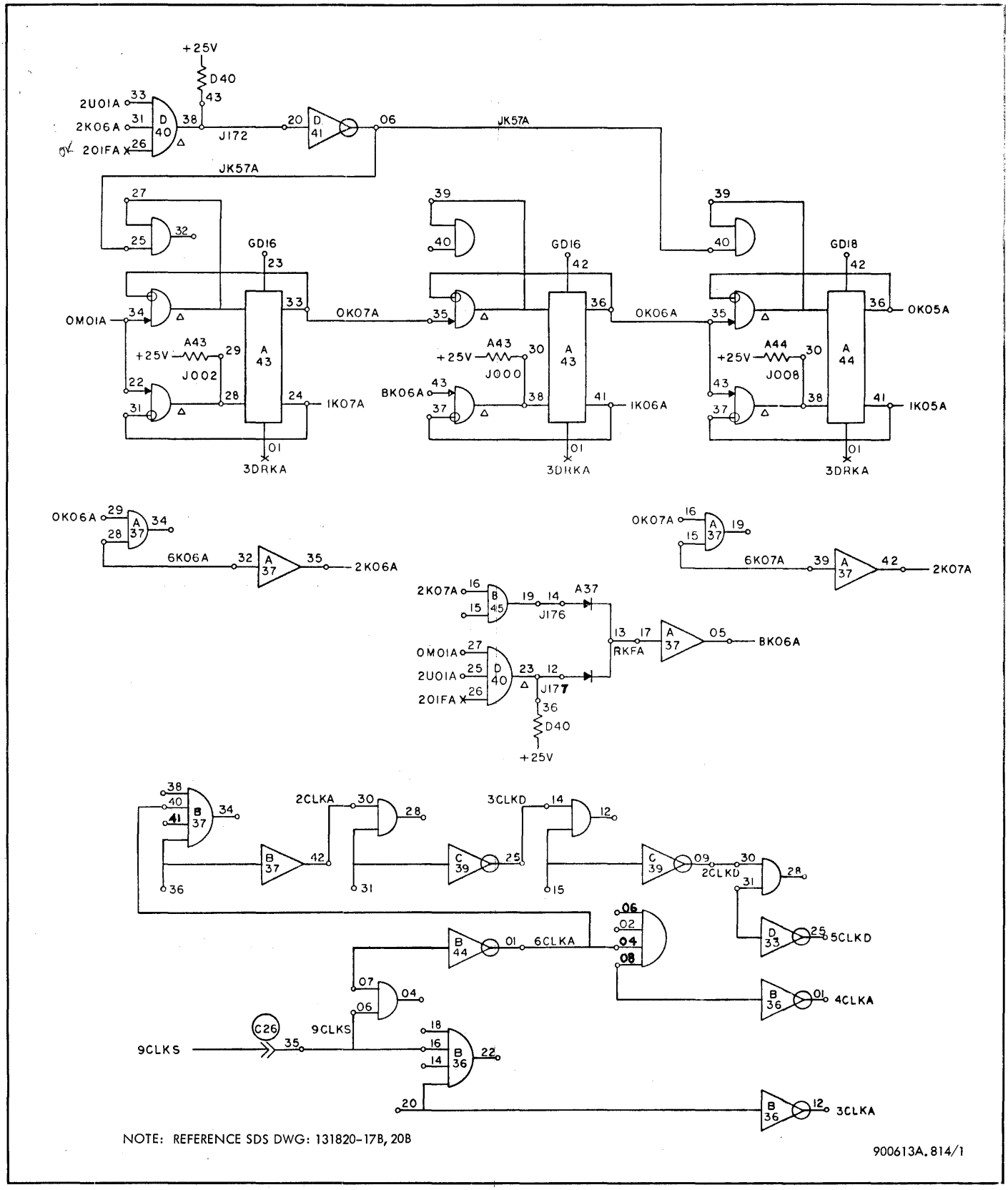


Figure 8-7. Controller Timing Circuits Logic Diagram (Sheet 1 of 3)

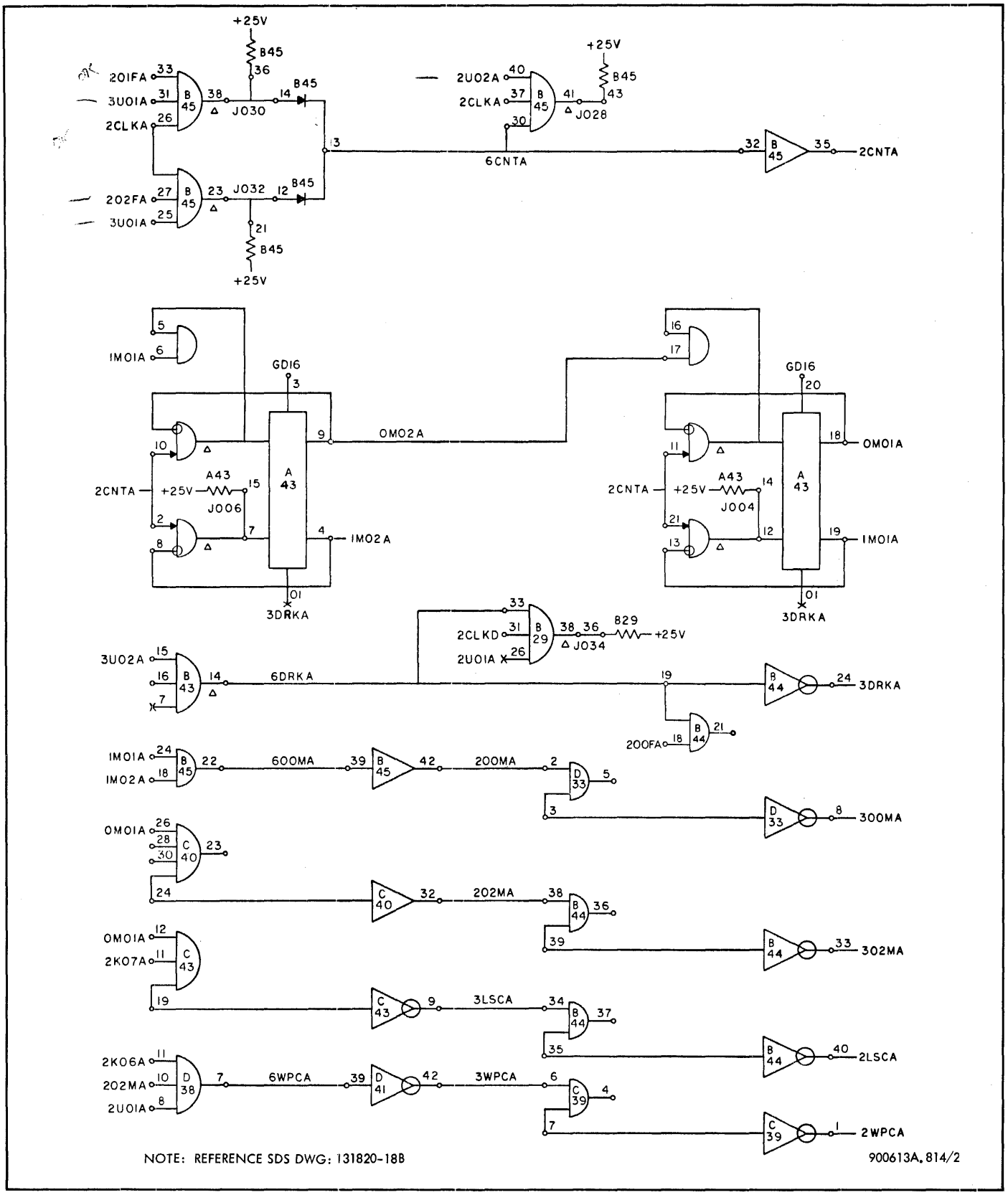


Figure 8-7. Controller Timing Circuits Logic Diagram (Sheet 2 of 3)

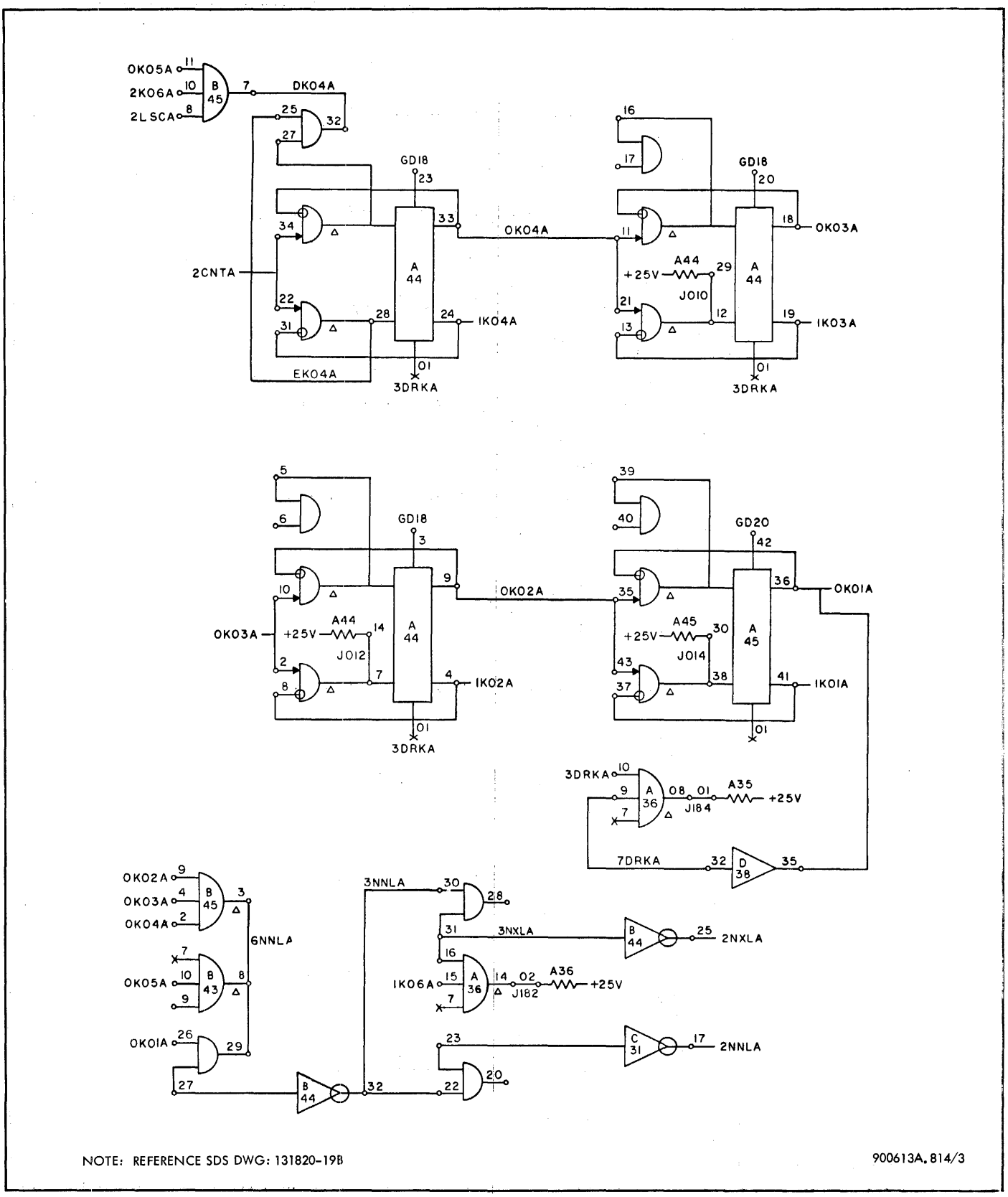


Figure 8-7. Controller Timing Circuits Logic Diagram (Sheet 3 of 3)

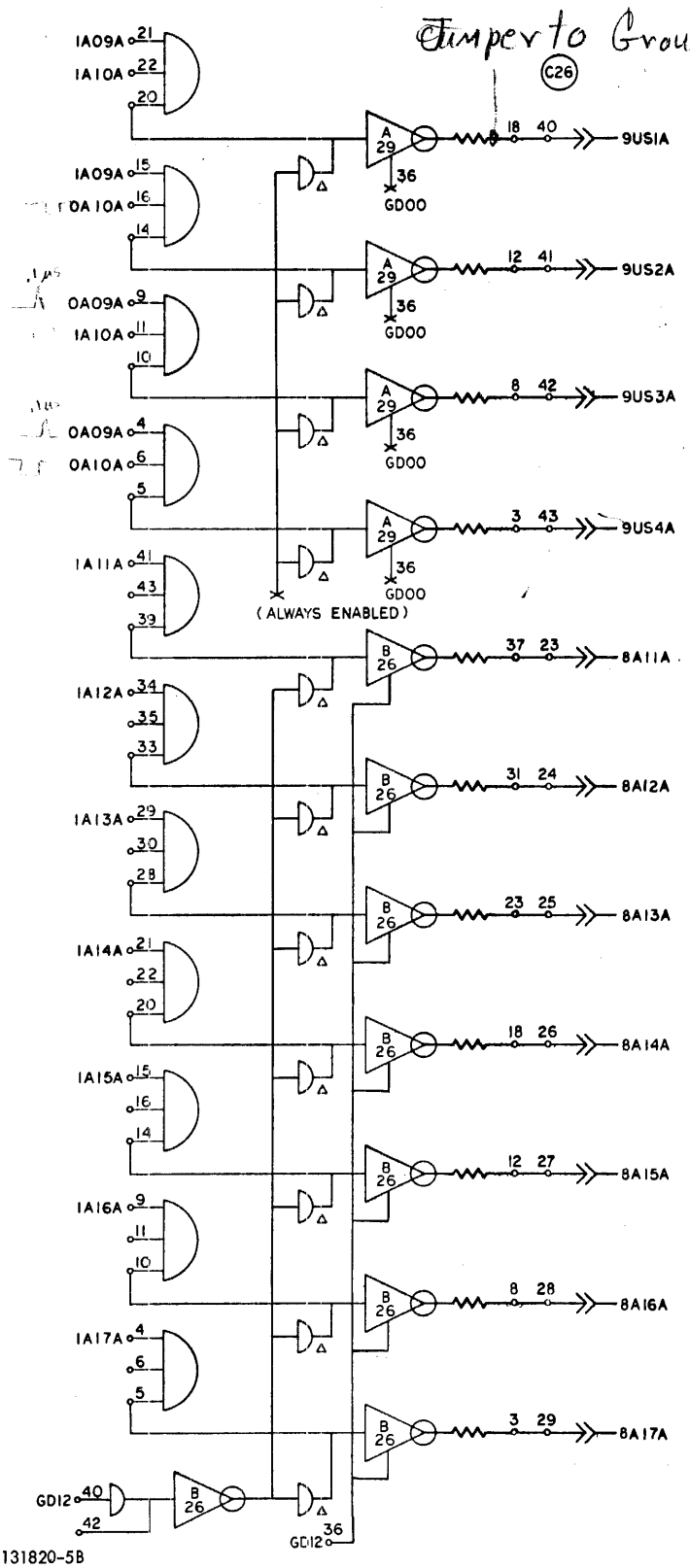
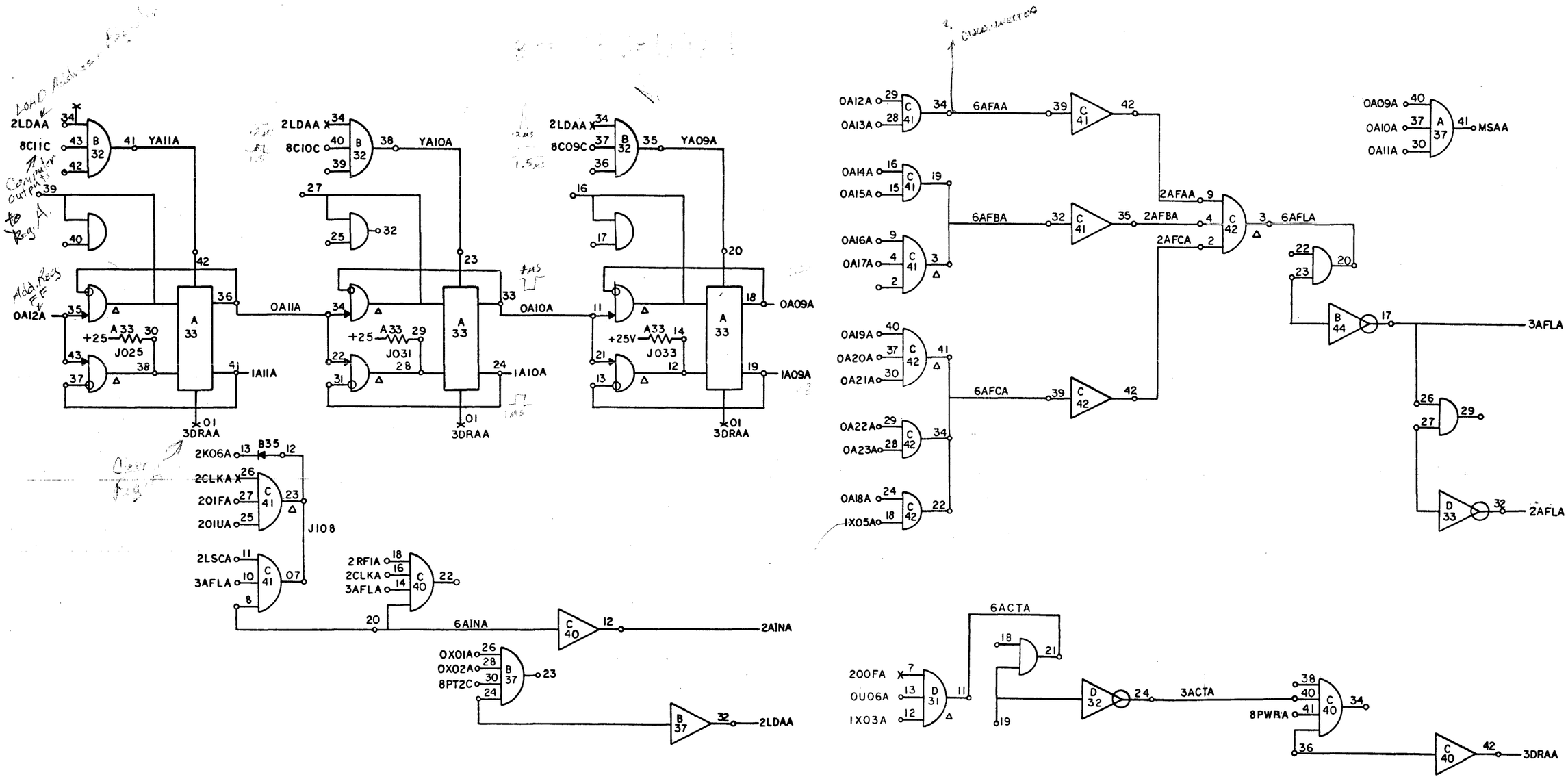
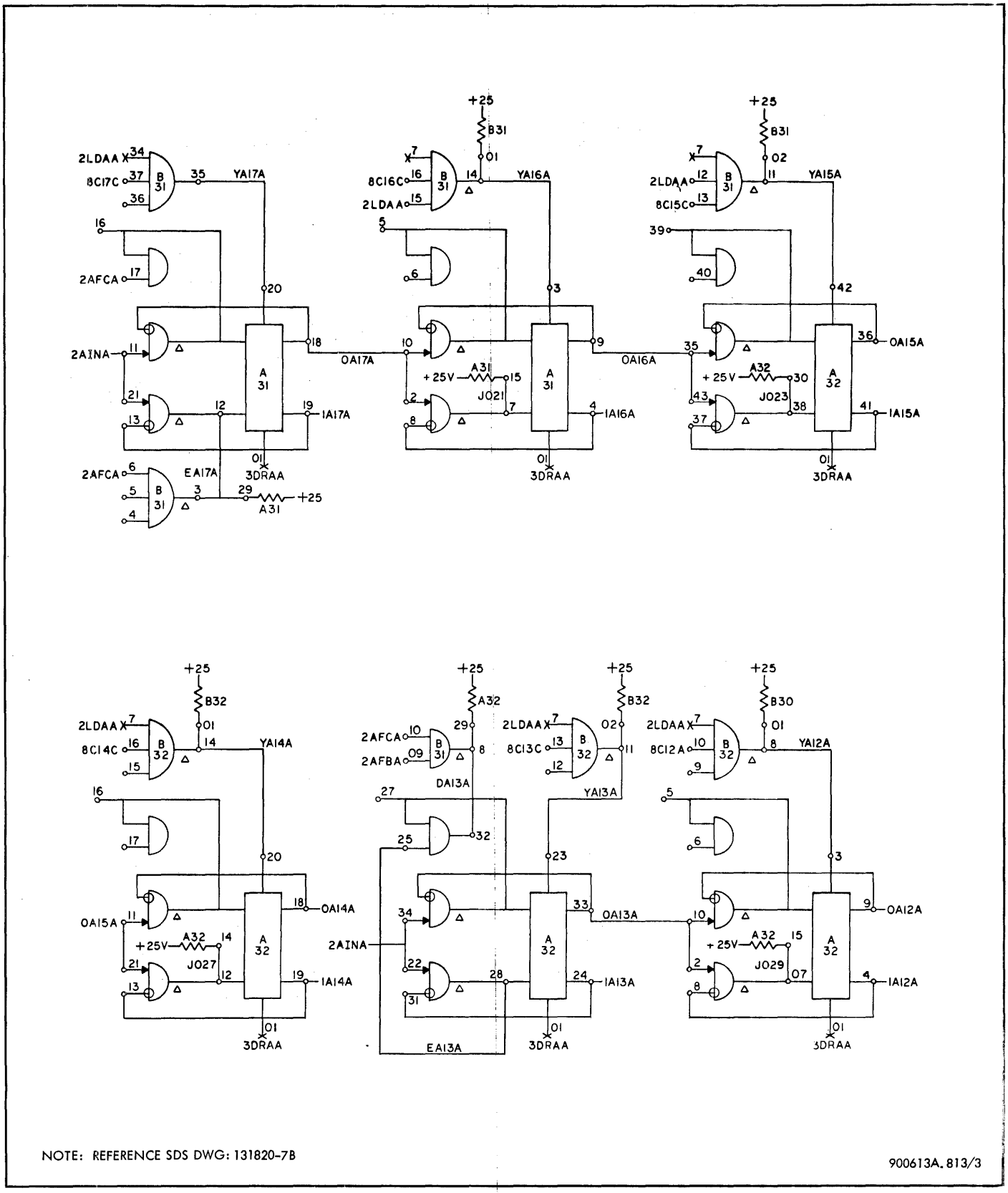


Figure 8-8. Controller Address Register Logic Diagram (Sheet 1 of 5)



NOTE: REFERENCE SDS DWG: 131820-6B, 32B

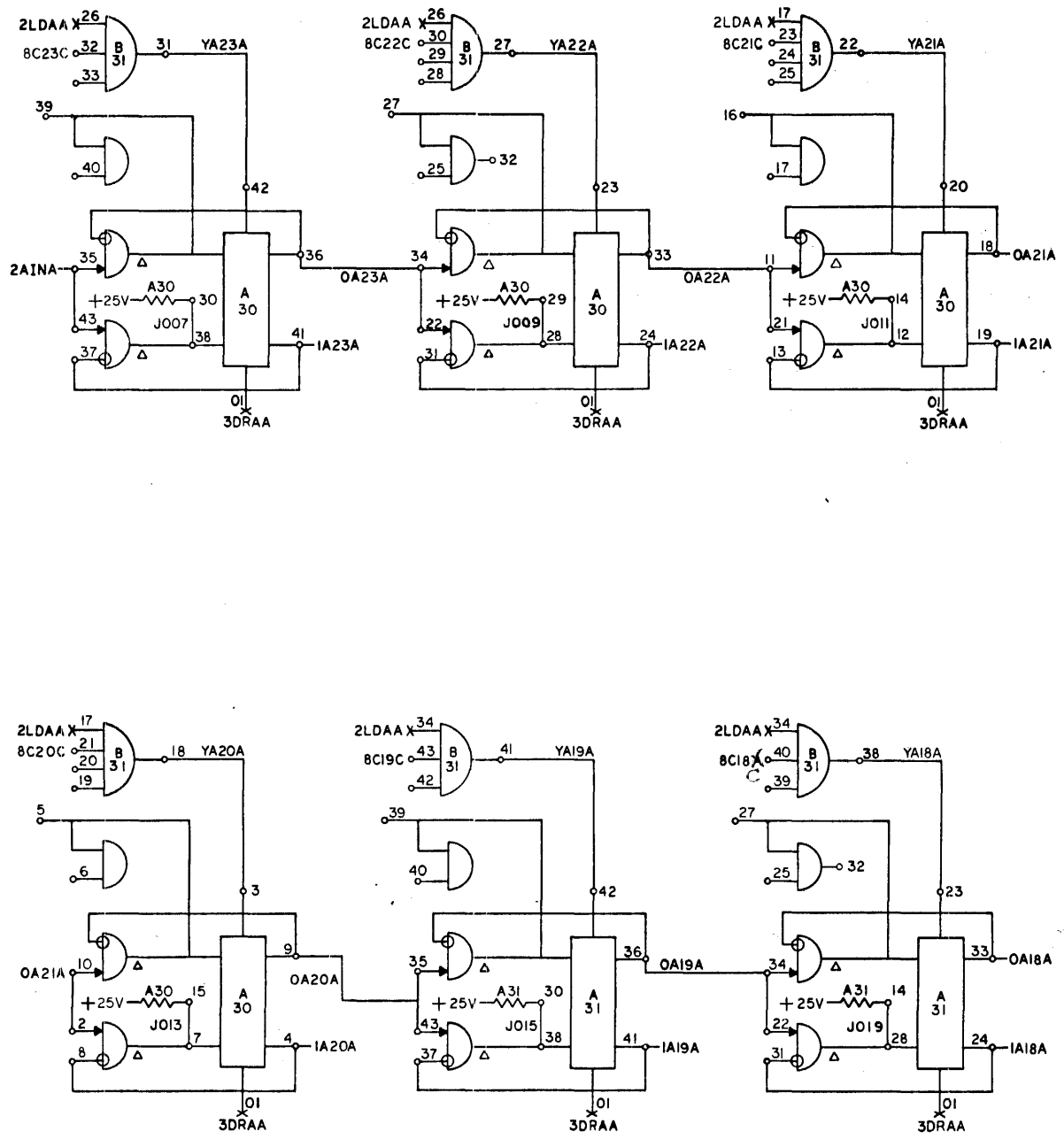
Figure 8-8. Controller Address Register Logic Diagram (Sheet 2 of 5)
900613A.813/2



NOTE: REFERENCE SDS DWG: 131820-7B

900613A.813/3

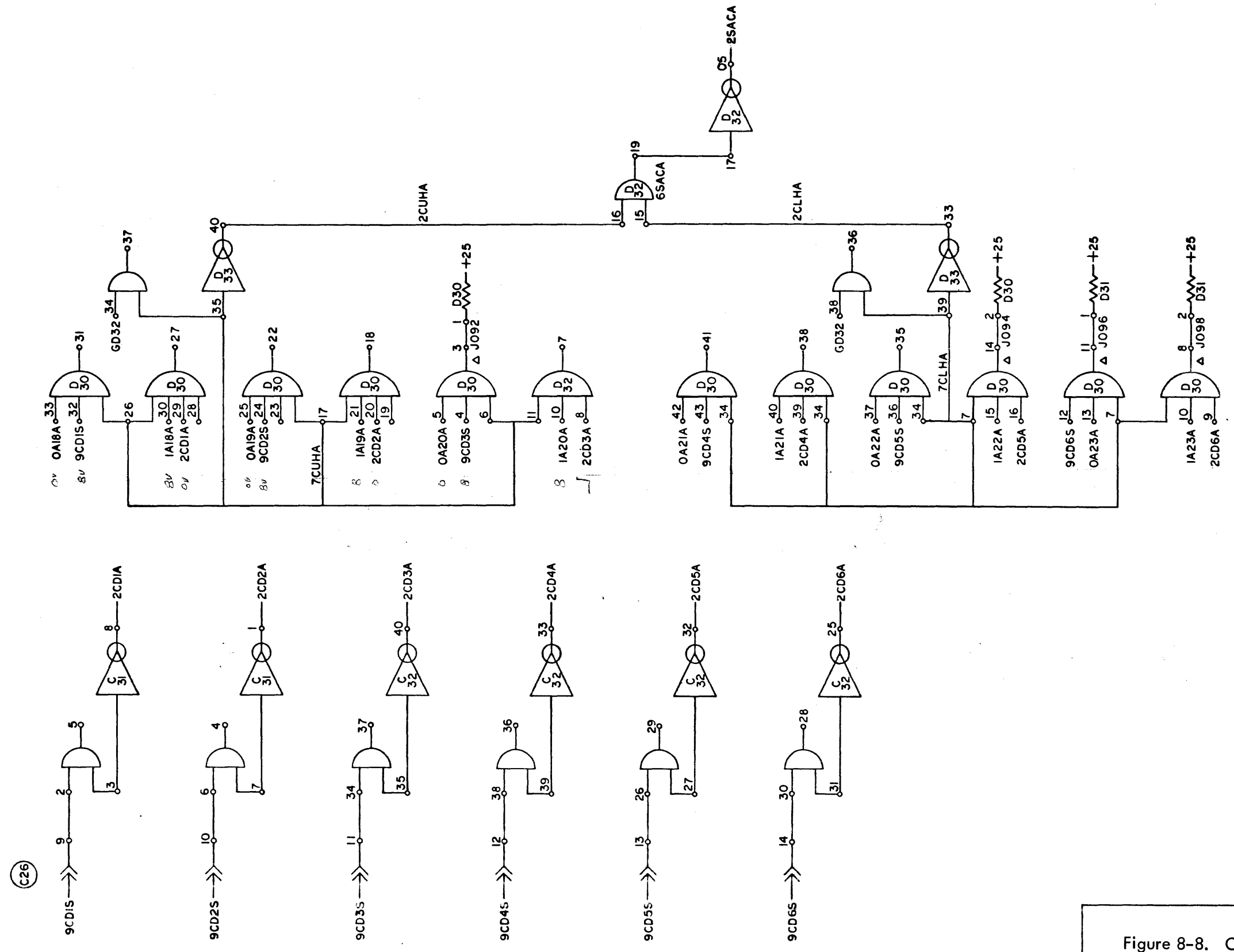
Figure 8-8. Controller Address Register Logic Diagram (Sheet 3 of 5)



NOTE: REFERENCE SDS DWG: 131820-8B

900613A. 813/4

Figure 8-8. Controller Address Register Logic Diagram (Sheet 4 of 5)



NOTE: REFERENCE SDS DWG: 131820-9B

Figure 8-8. Controller Address Register Logic Diagram (Sheet 5 of 5)

900613A.813/5

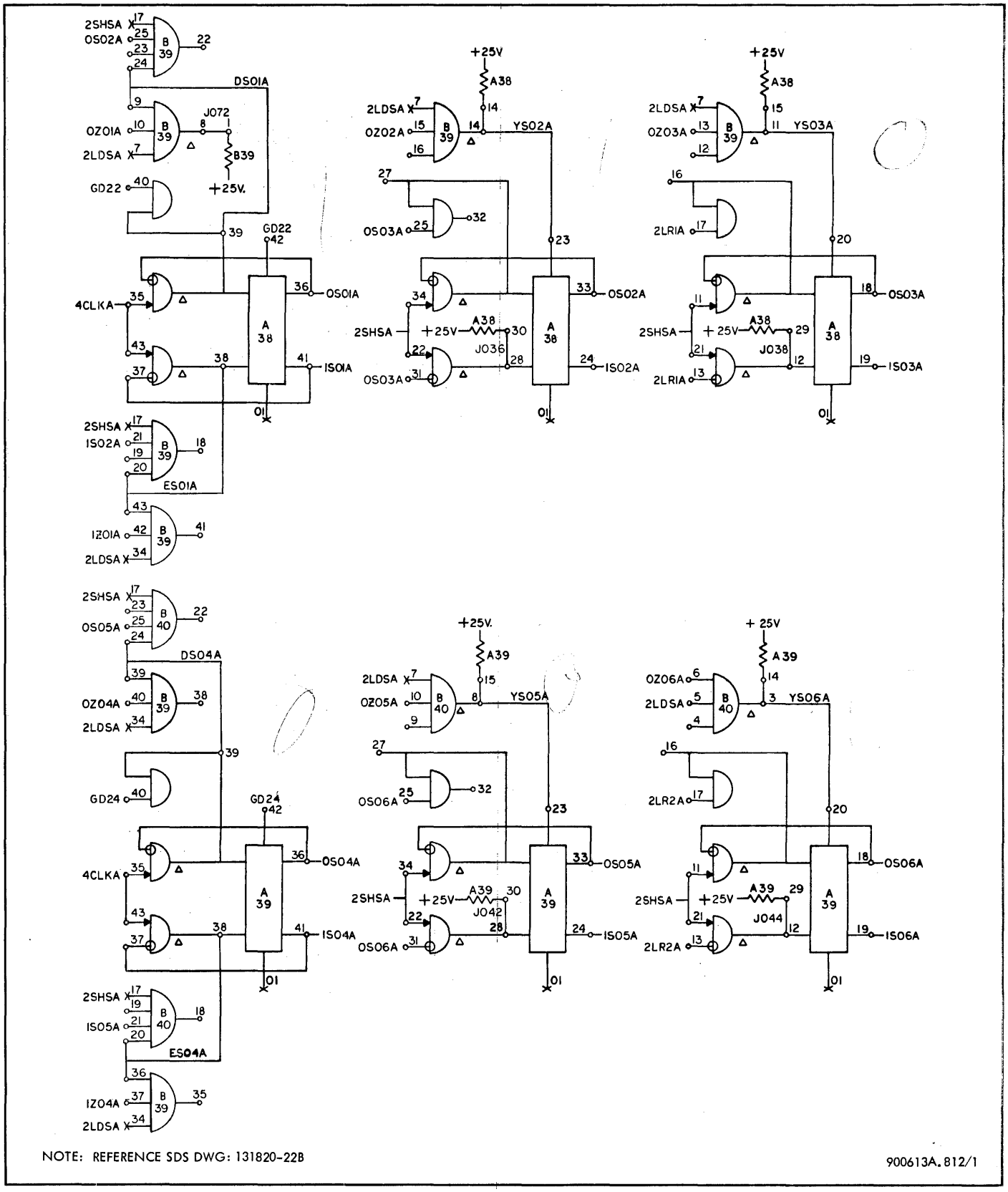


Figure 8-9. Controller Data Register Logic Diagram (Sheet 1 of 7)

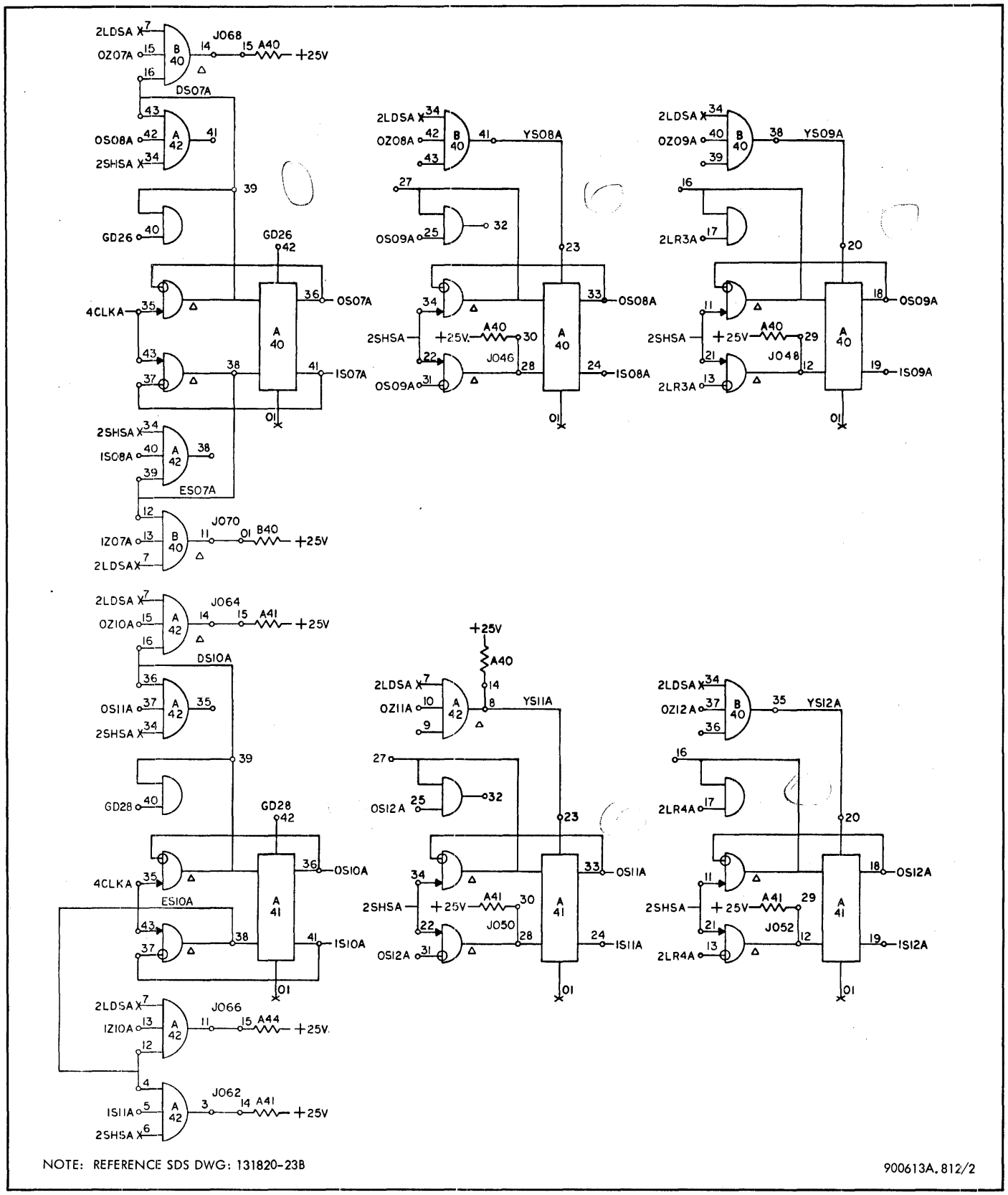
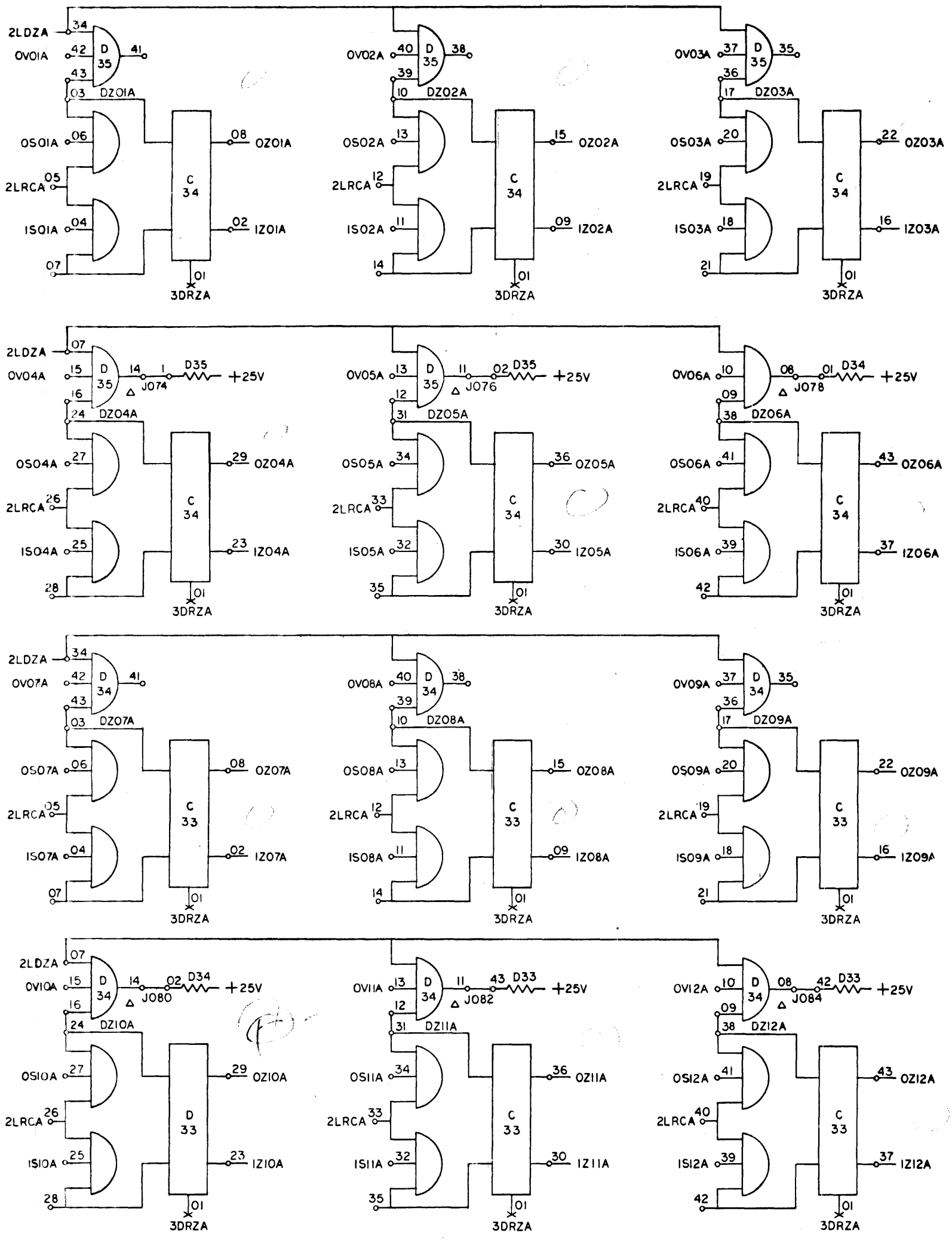


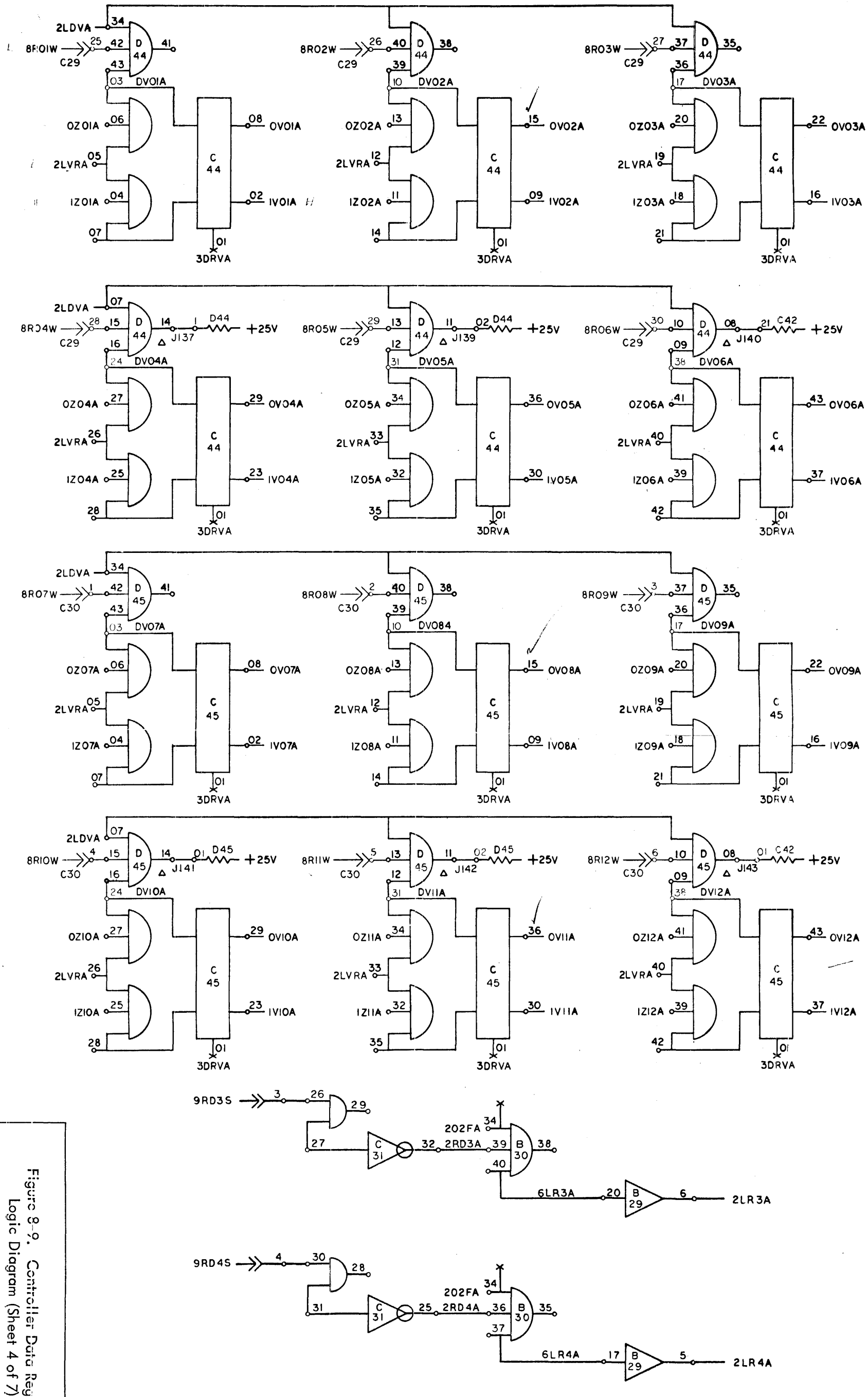
Figure 8-9. Controller Data Register Logic Diagram (Sheet 2 of 7)



NOTE: REFERENCE SDS DWG: 131820-26B, 30B

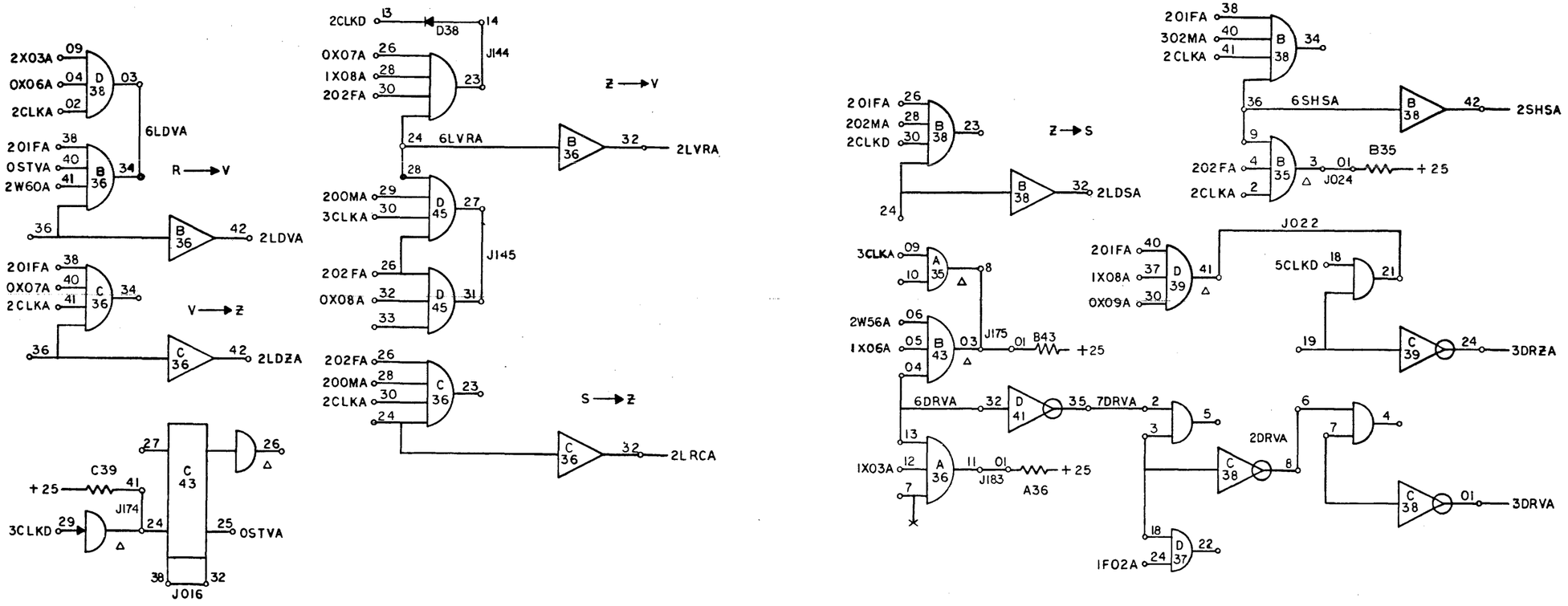
Figure 8-9. Controller Data Register Logic Diagram (Sheet 3 of 7)

900613A, 812/3



NOTE: REFERENCE SDS DWG: 131820-27B, 30B

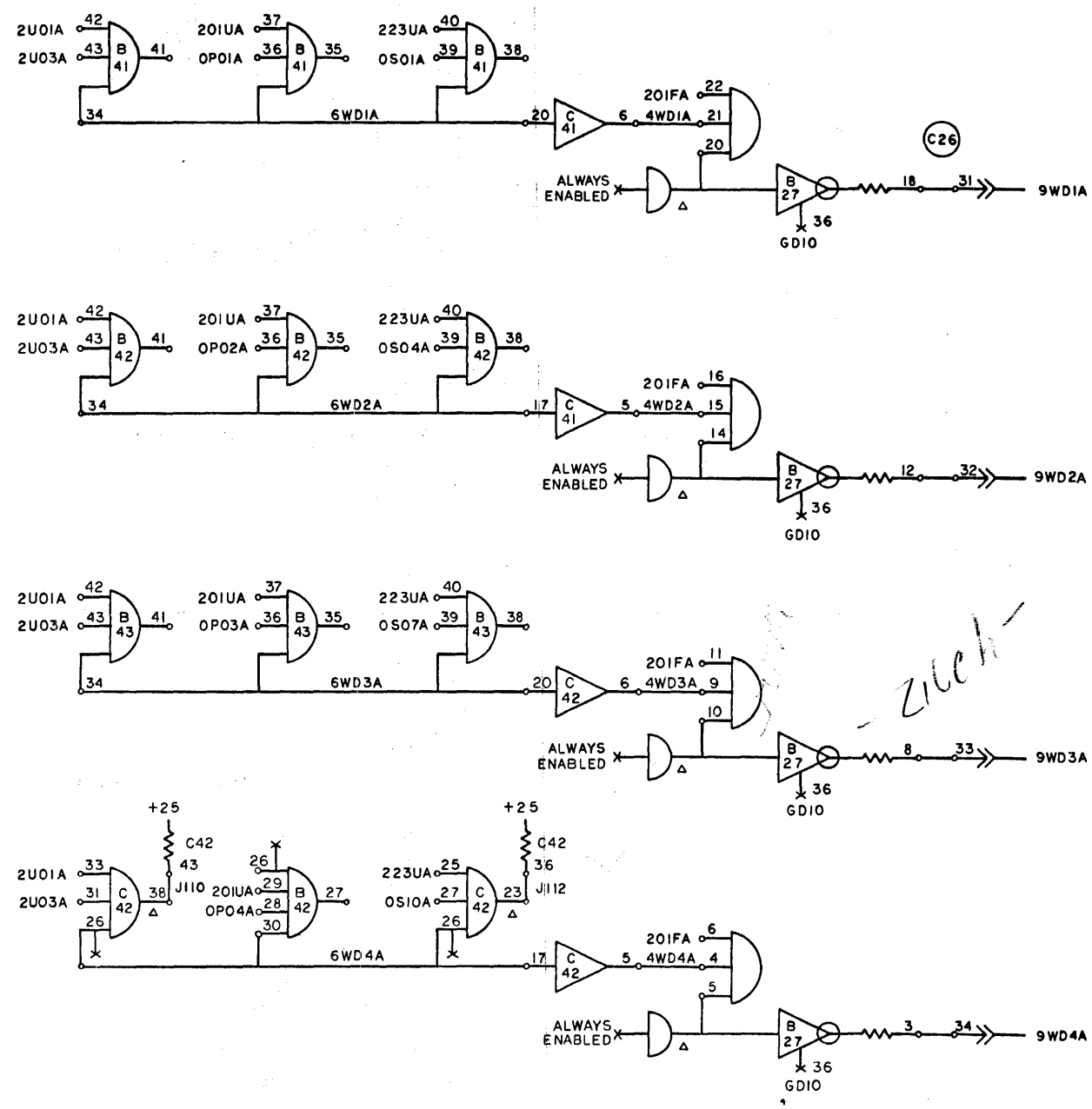
Figure 8-9. Controller Data Register Logic Diagram (Sheet 4 of 7)
900613A.812/4



NOTE: REFERENCE SDS DWG: 131820-28B

Figure 8-9. Controller Data Register Logic Diagram (Sheet 5 of 7)

900613A.812/5



U01	U02	U03	201UA	223UA	2WD1A
→ 0	0	0	1	0	PXX
0	1	0	0	1	SXX
0	1	1	0	1	
1	0	1	0	0 1	ALWAYS ZERO
1	1	1	0	0 1	

NOTE: REFERENCE SDS DWG: 131820-29B

900613A.812/6

Figure 8-9. Controller Data Register Logic Diagram (Sheet 6 of 7)

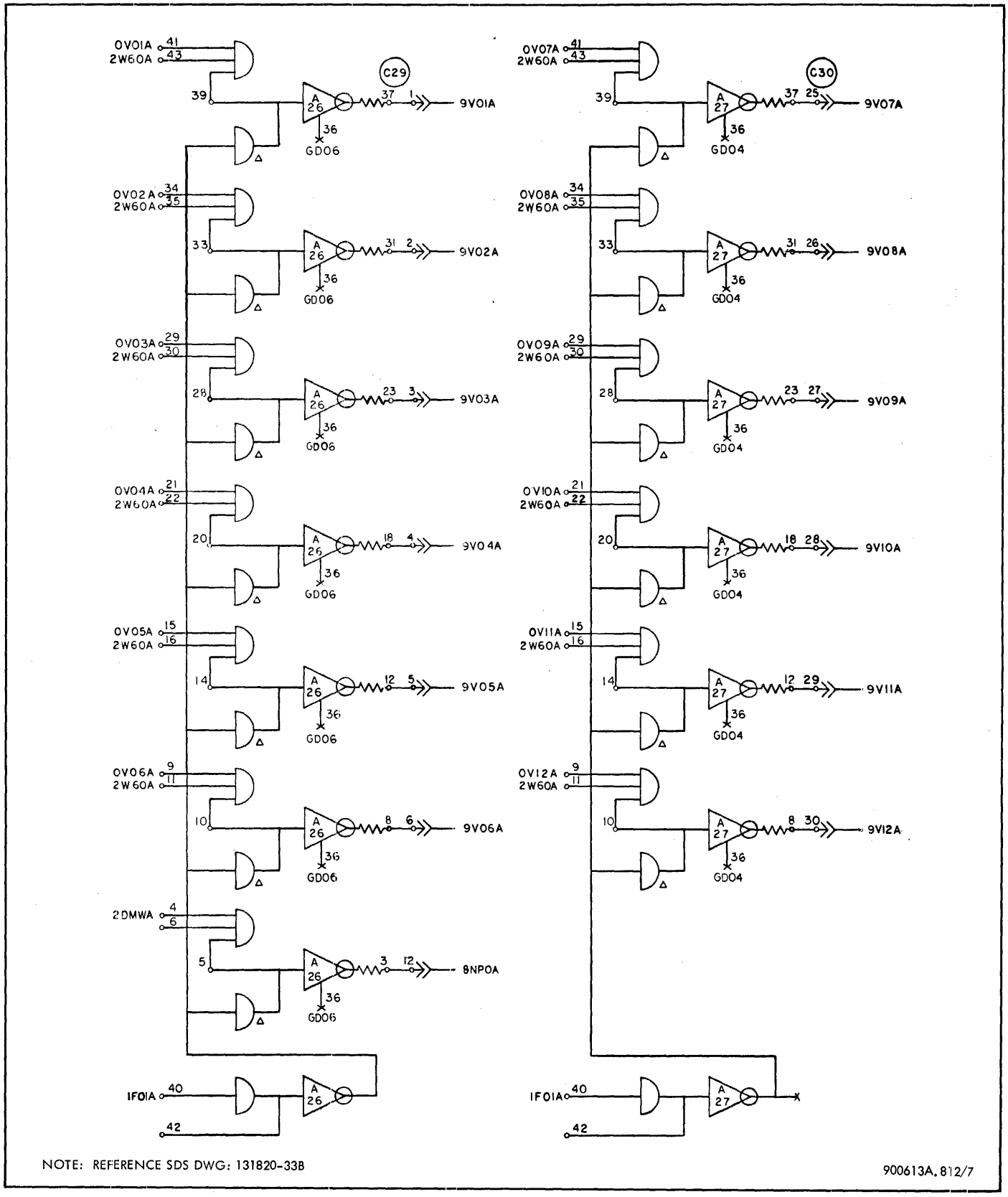


Figure 8-9. Controller Data Register Logic Diagram (Sheet 7 of 7)

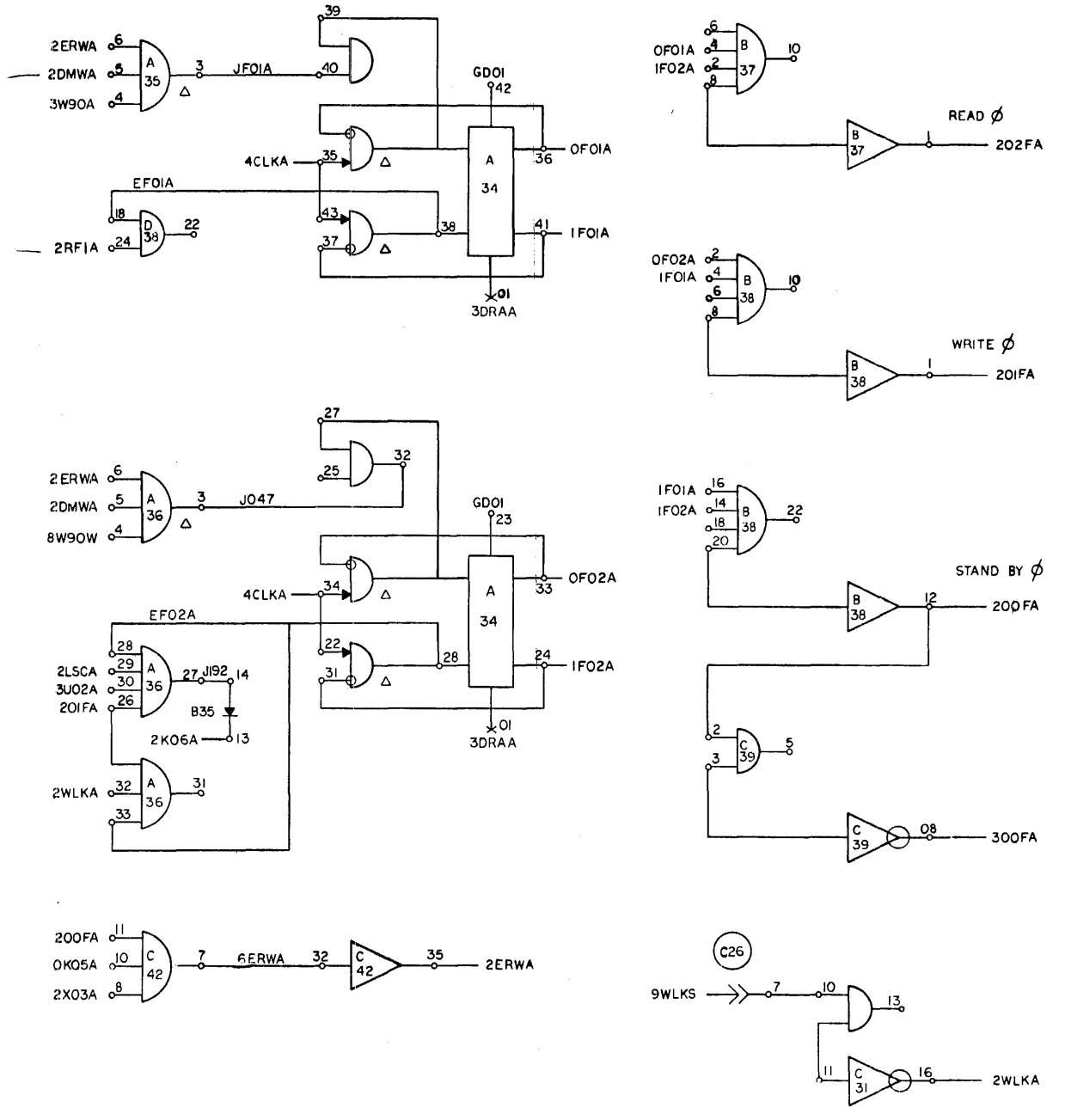
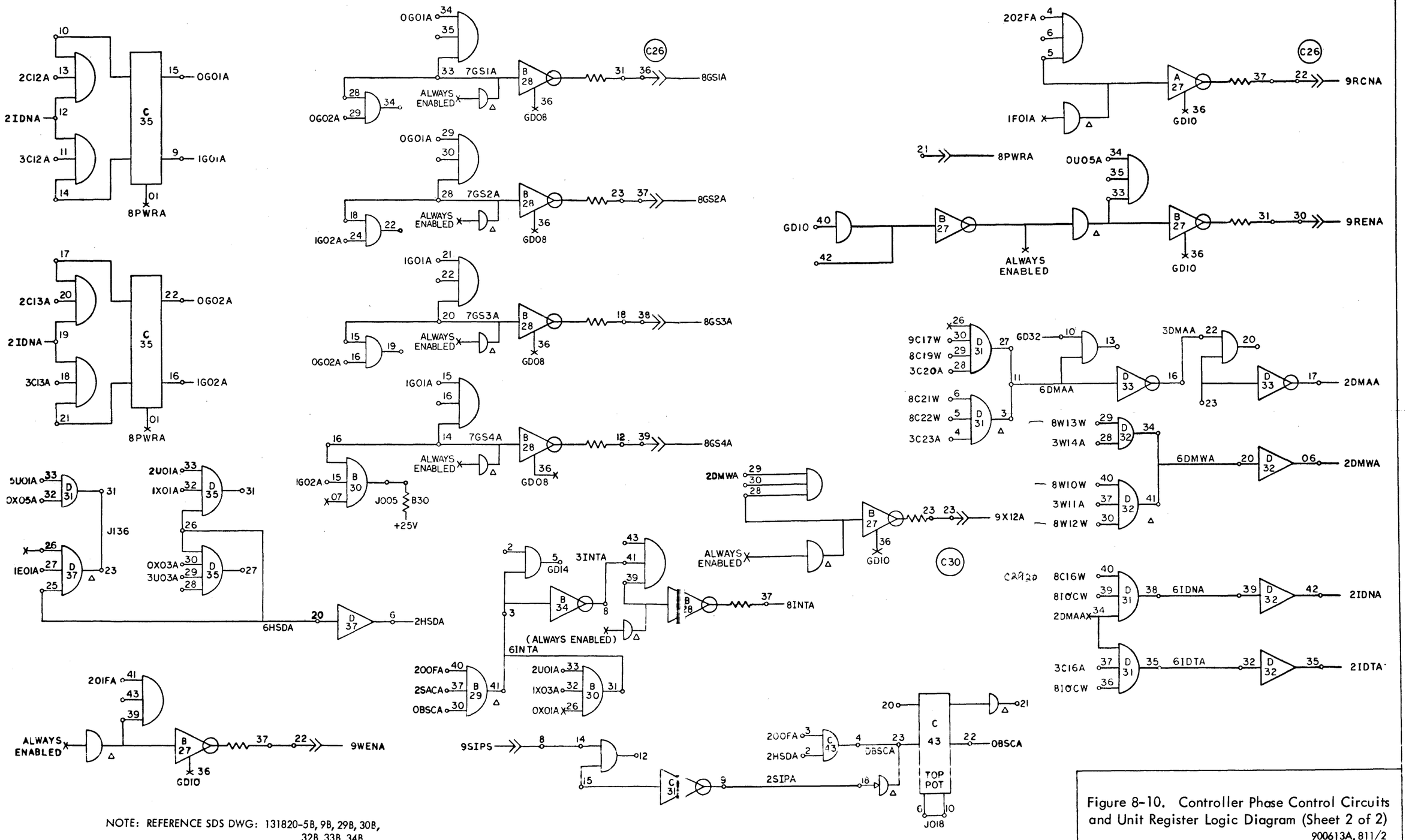


Figure 8-10. Controller Phase Control Circuits and Unit Register Logic Diagram (Sheet 1 of 2)



NOTE: REFERENCE SDS DWG: 131820-5B, 9B, 29B, 30B, 32B, 33B, 34B

Figure 8-10. Controller Phase Control Circuits and Unit Register Logic Diagram (Sheet 2 of 2)
900613A.811/2

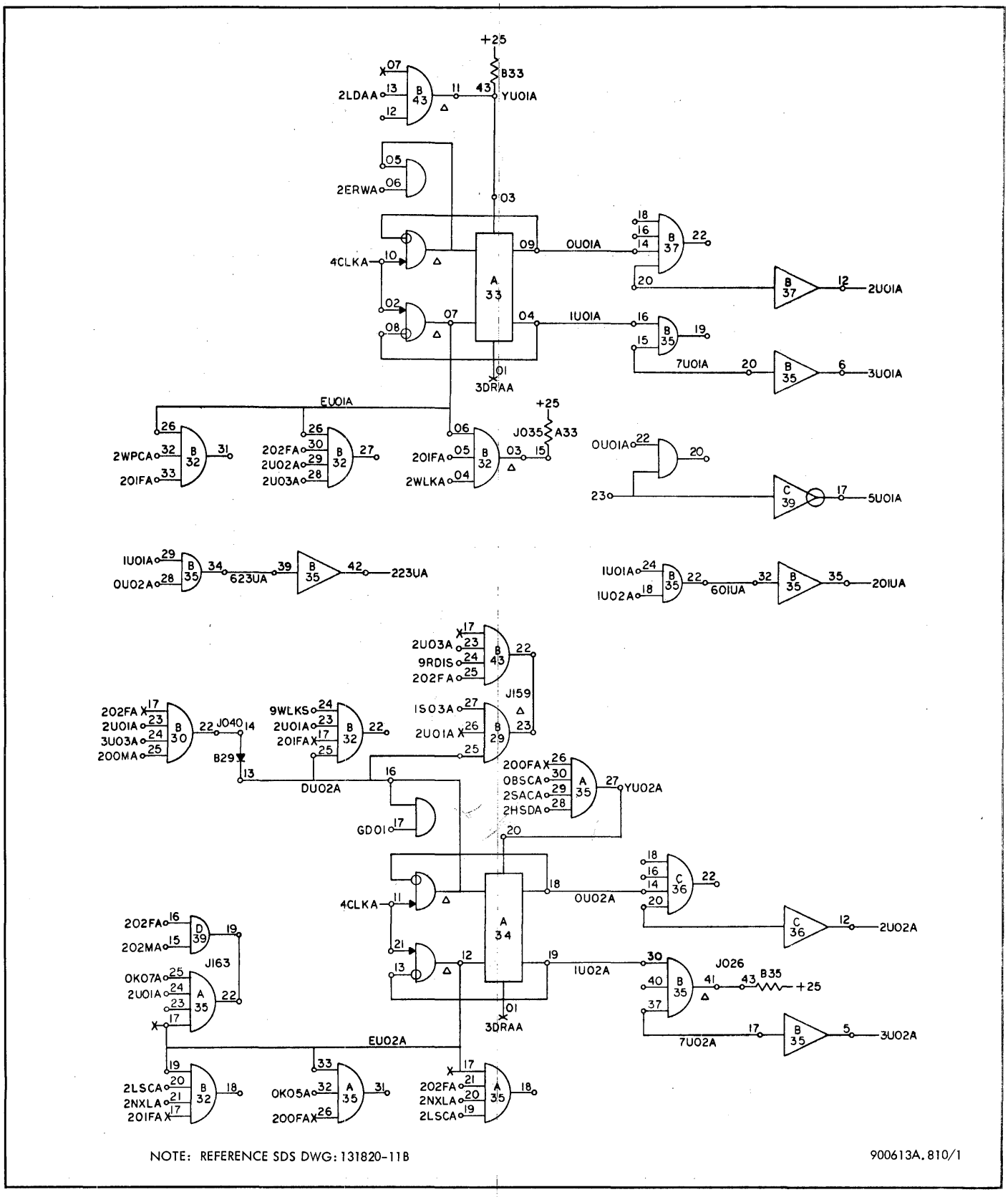
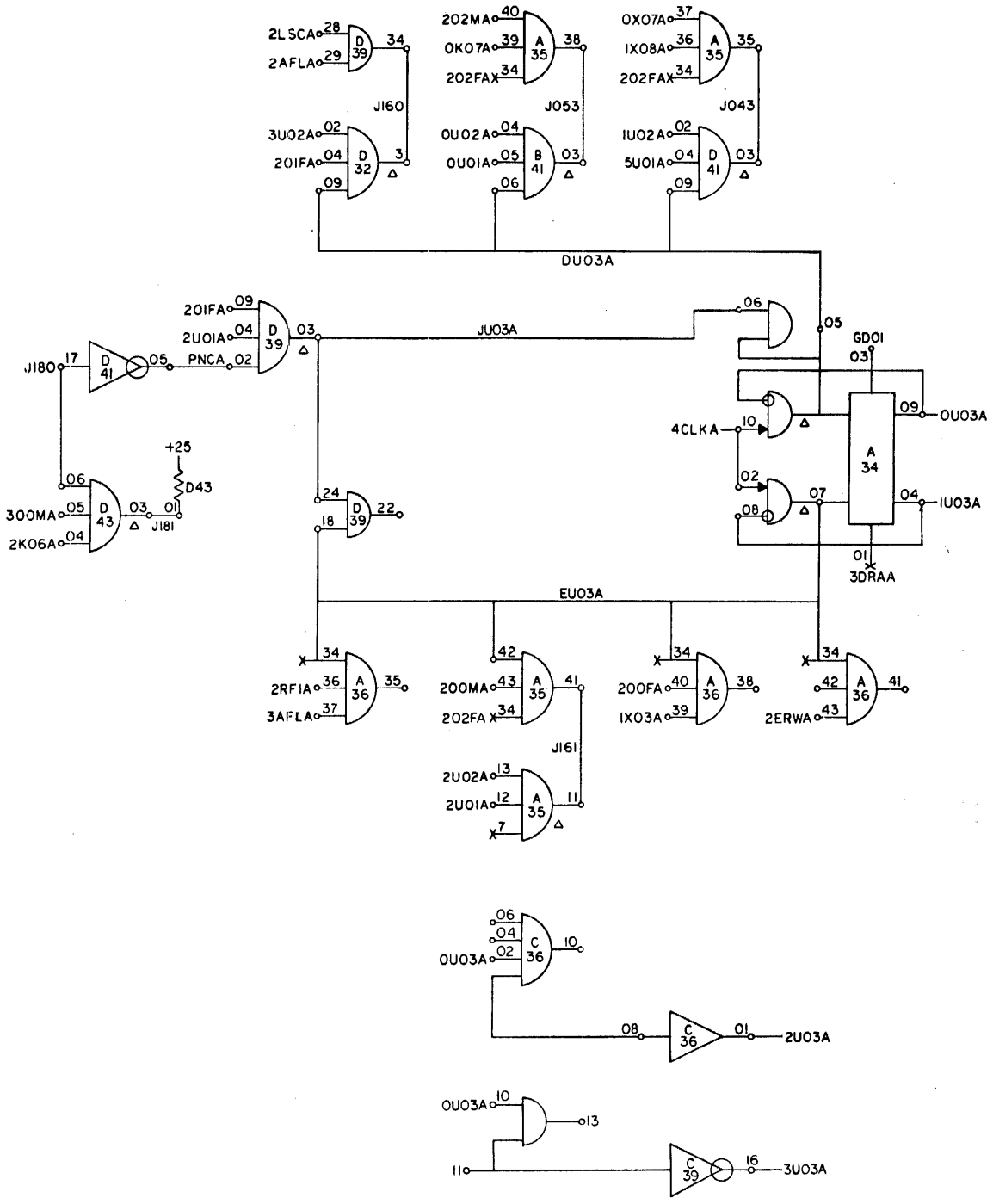


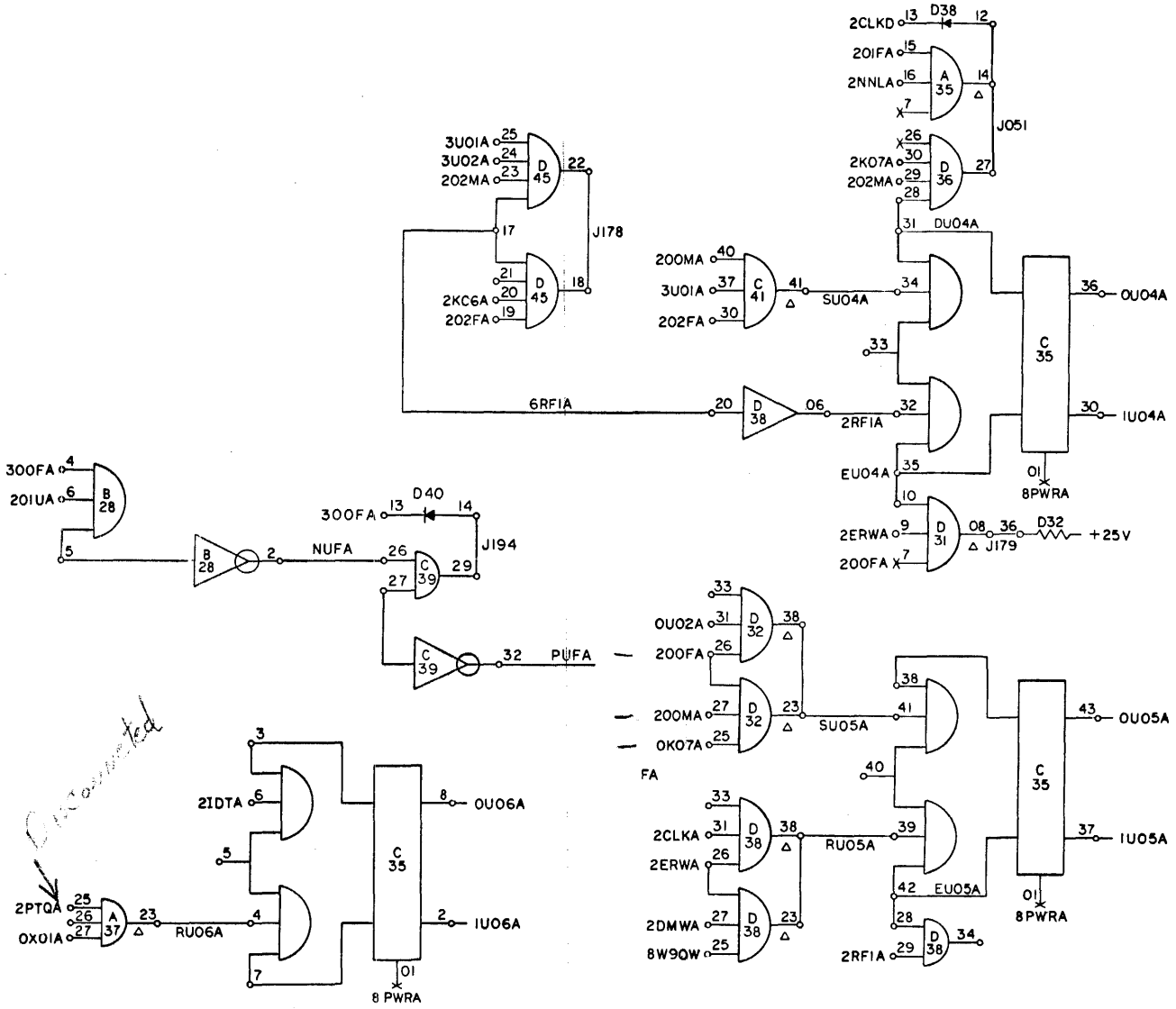
Figure 8-11. Controller Subphase Control Circuits Logic Diagram (Sheet 1 of 3)



NOTE: REFERENCE SDS DWG: 131820-12B

900613A.810/2

Figure 8-11. Controller Subphase Control Circuits Logic Diagram (Sheet 2 of 3)

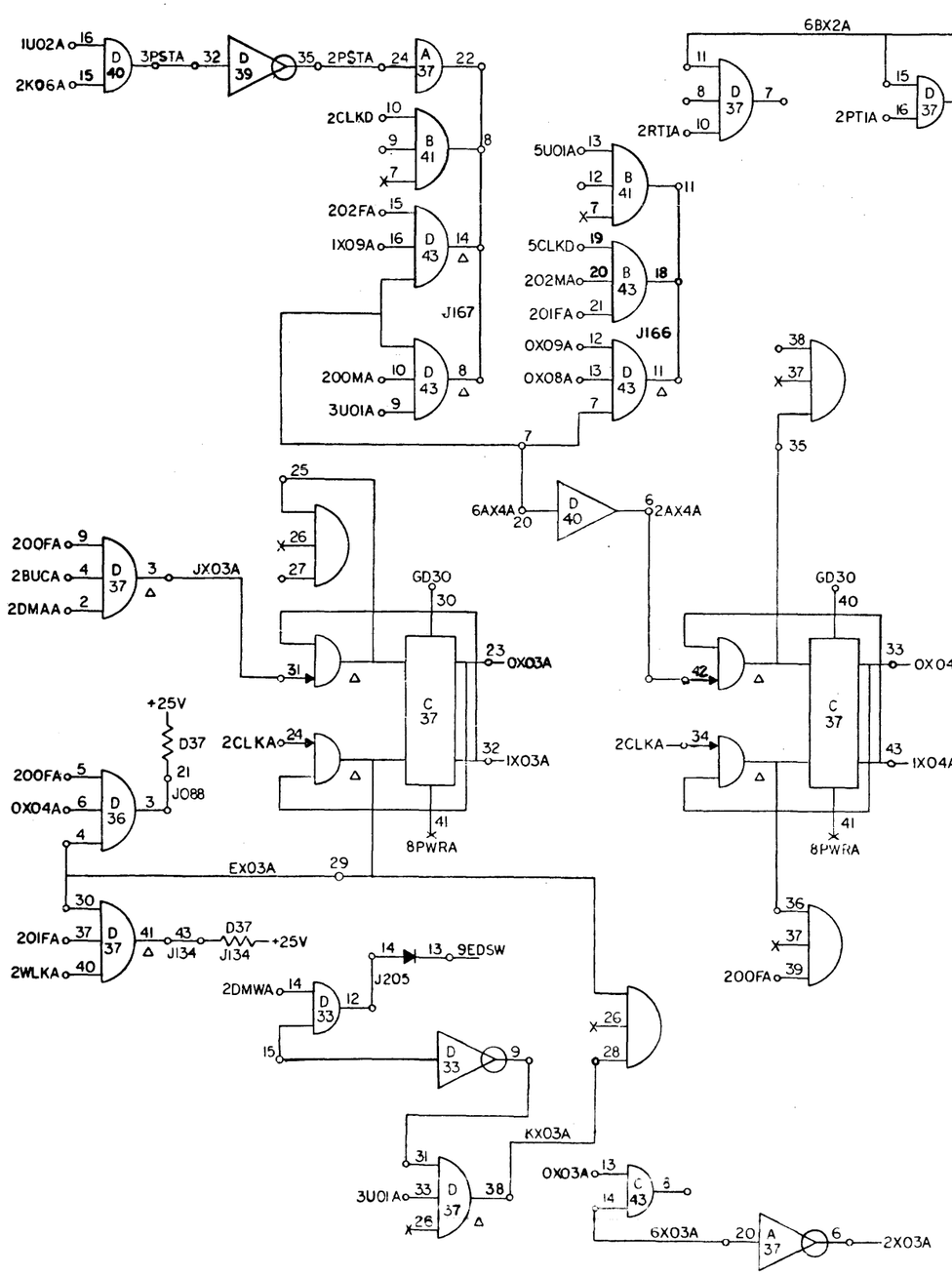


00F	201UA	NUFA	PUFA
0	0	1	0
0	1	0	1
1	0	1	1
1	1	1	1

NOTE: REFERENCE SDS DWG: 131820-13B, 15B, 31B

900613A.810/3

Figure 8-11. Controller Subphase Control Circuits Logic Diagram (Sheet 3 of 3)



NOTE: REFERENCE SDS DWG: 131820-14B

Figure 8-12. Controller Data Transfer Control Circuits Logic Diagram (Sheet 1 of 3)
900613A. 809/1

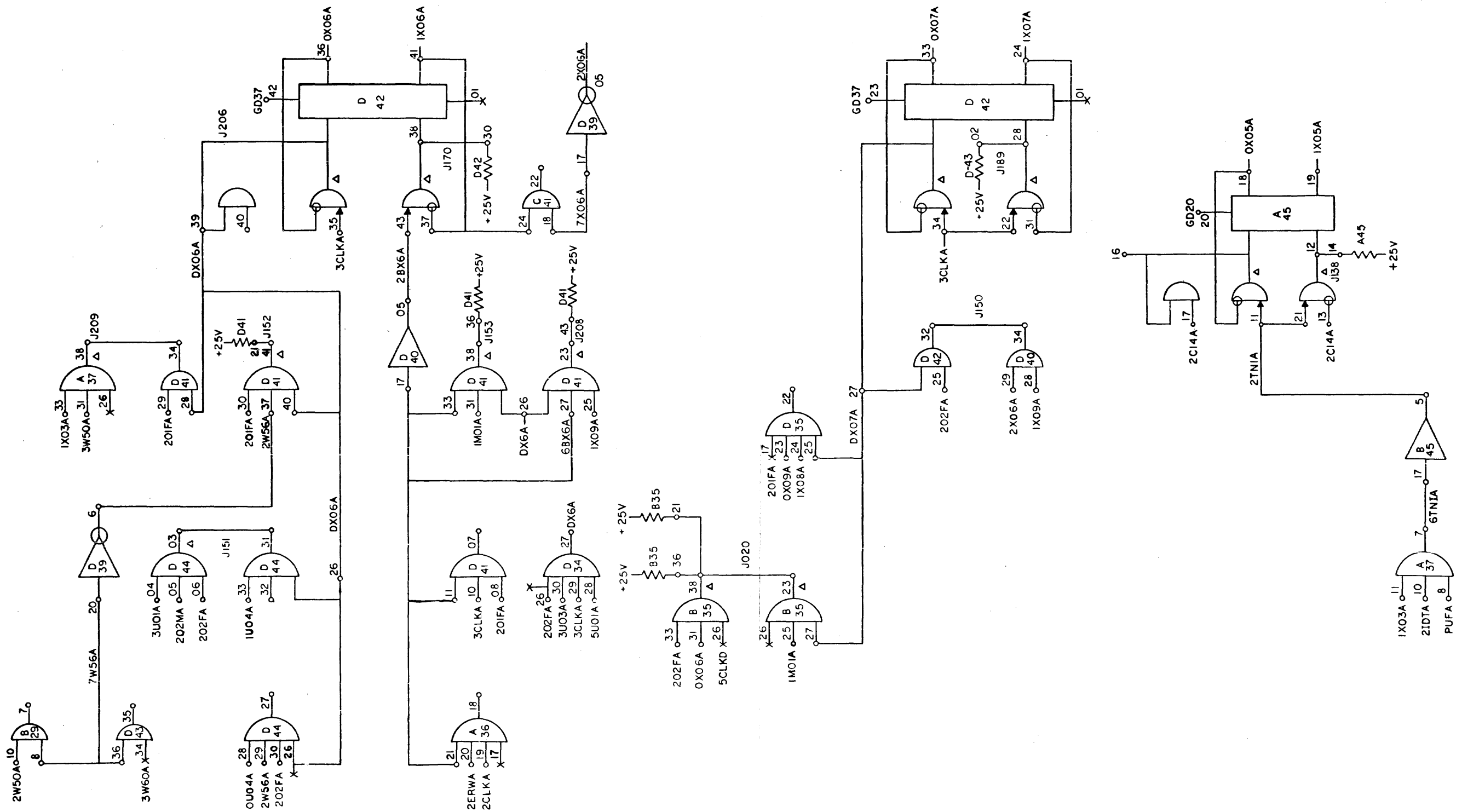


Figure 8-12. Controller Data Transfer Control Circuits Logic Diagram (Sheet 2 of 3)

900613A.809/2

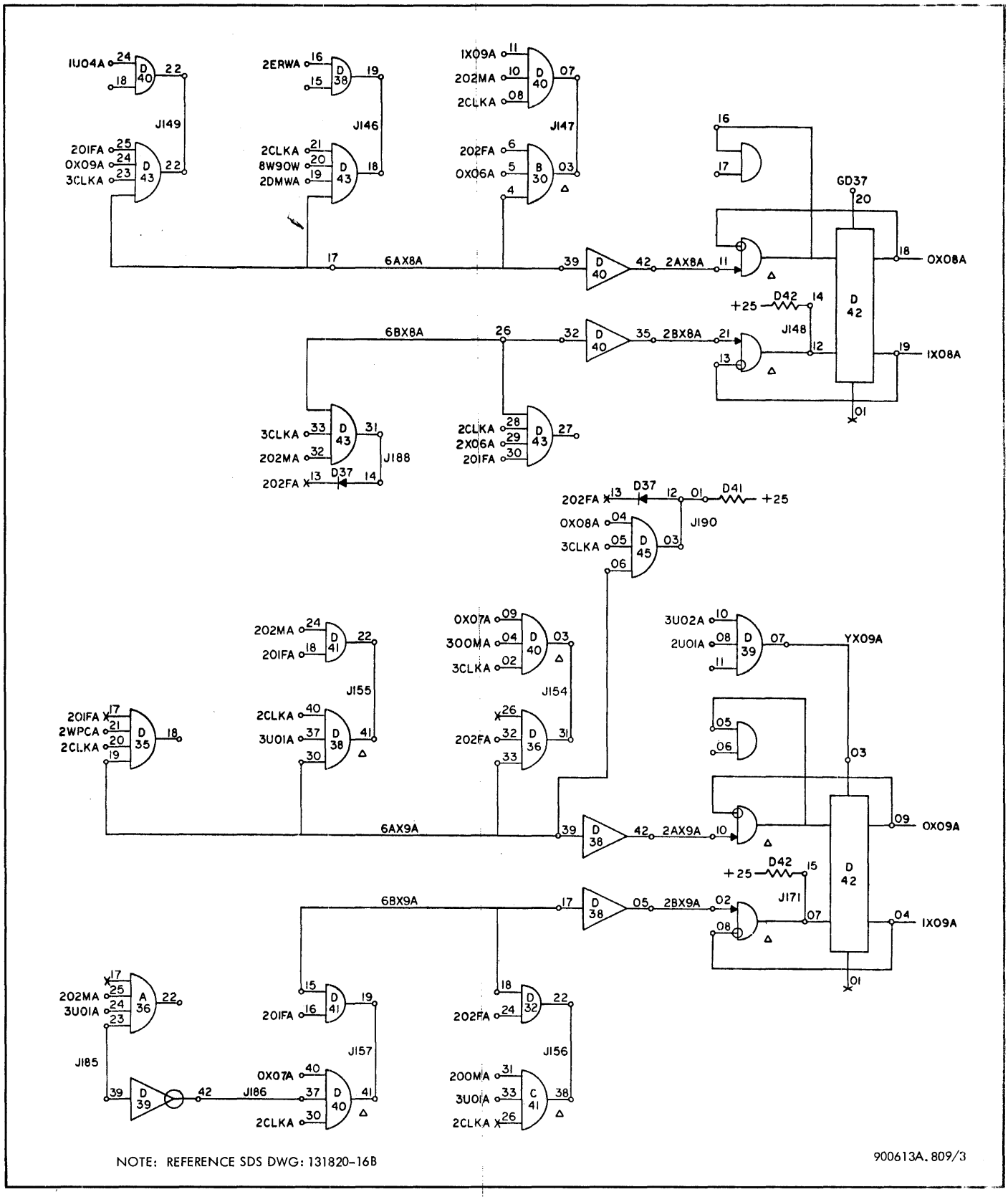
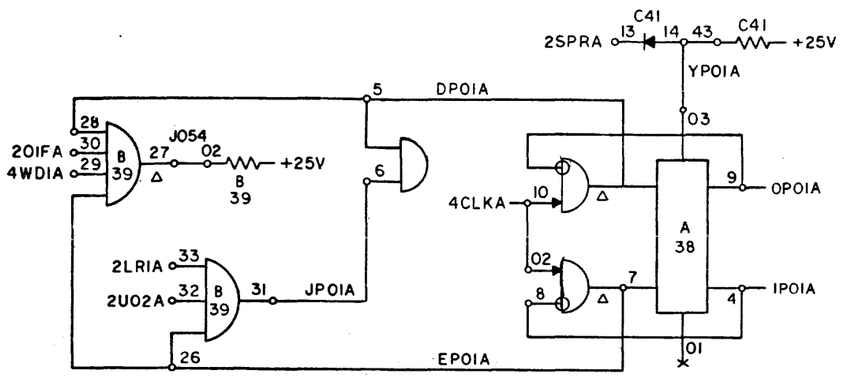
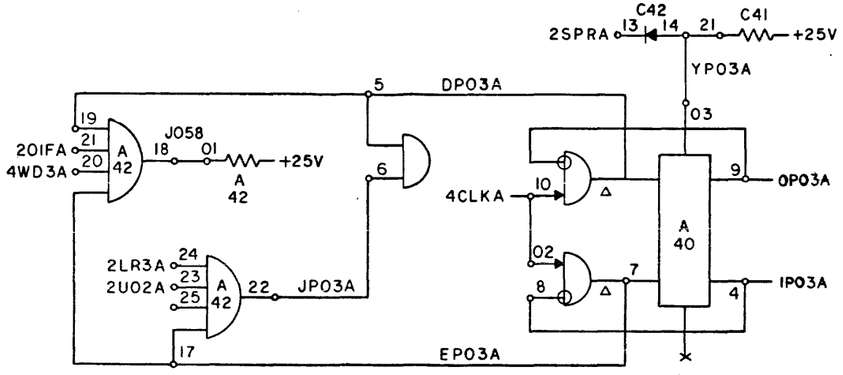
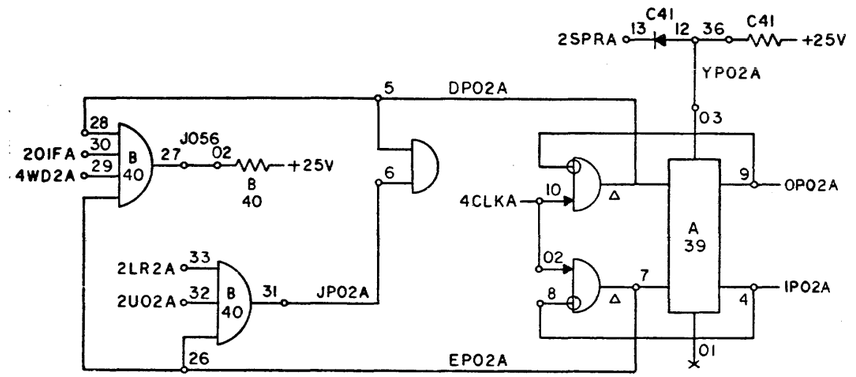
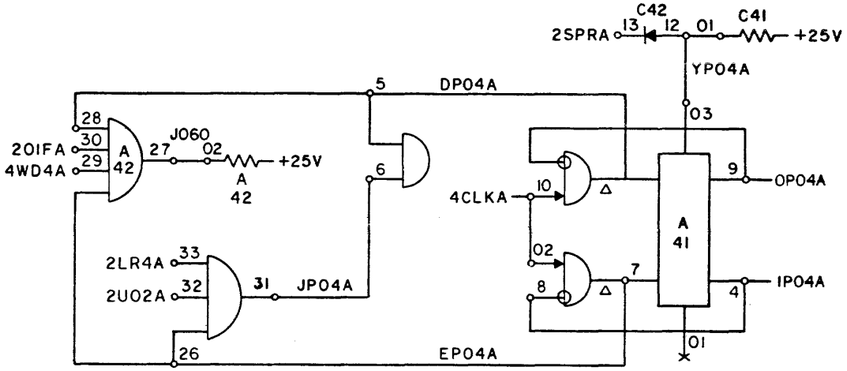


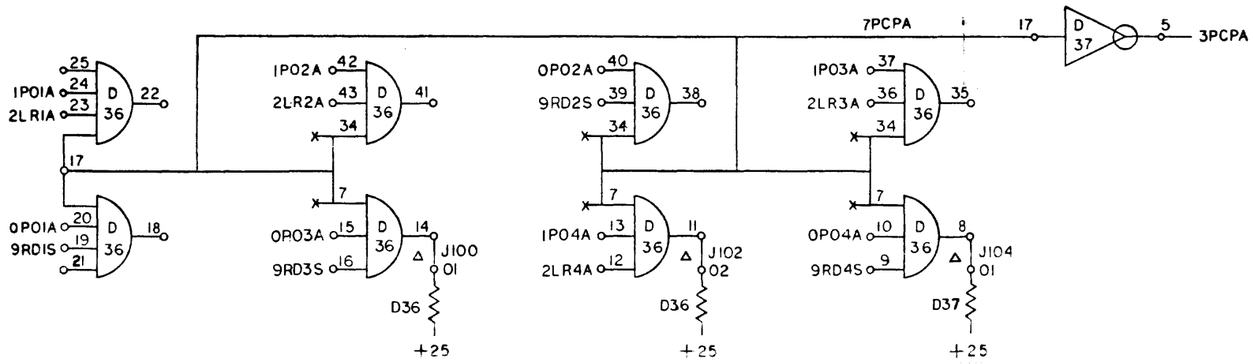
Figure 8-12. Controller Data Transfer Control Circuits Logic Diagram (Sheet 3 of 3)

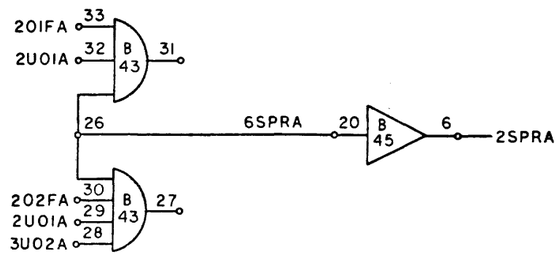








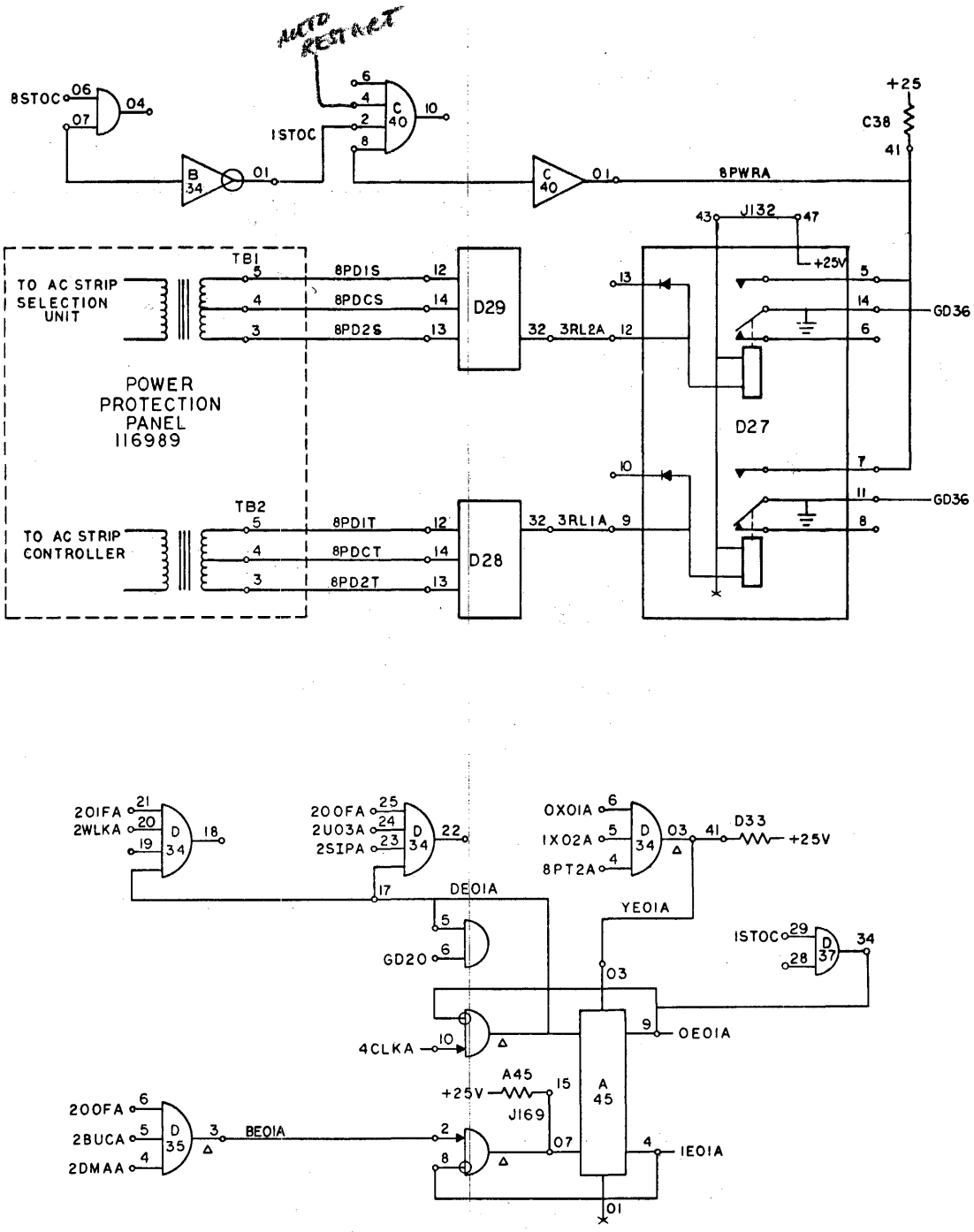




NOTE: REFERENCE SDS DWG: 131820-24B, 25B

Figure 8-13. Controller Parity Circuits Logic Diagram

900613A. 808



NOTE: REFERENCE SDS DWG: 131820-17A, 21B

900613A.807

Figure 8-14. Controller Error and Power Failure Detect Circuits Logic Diagram

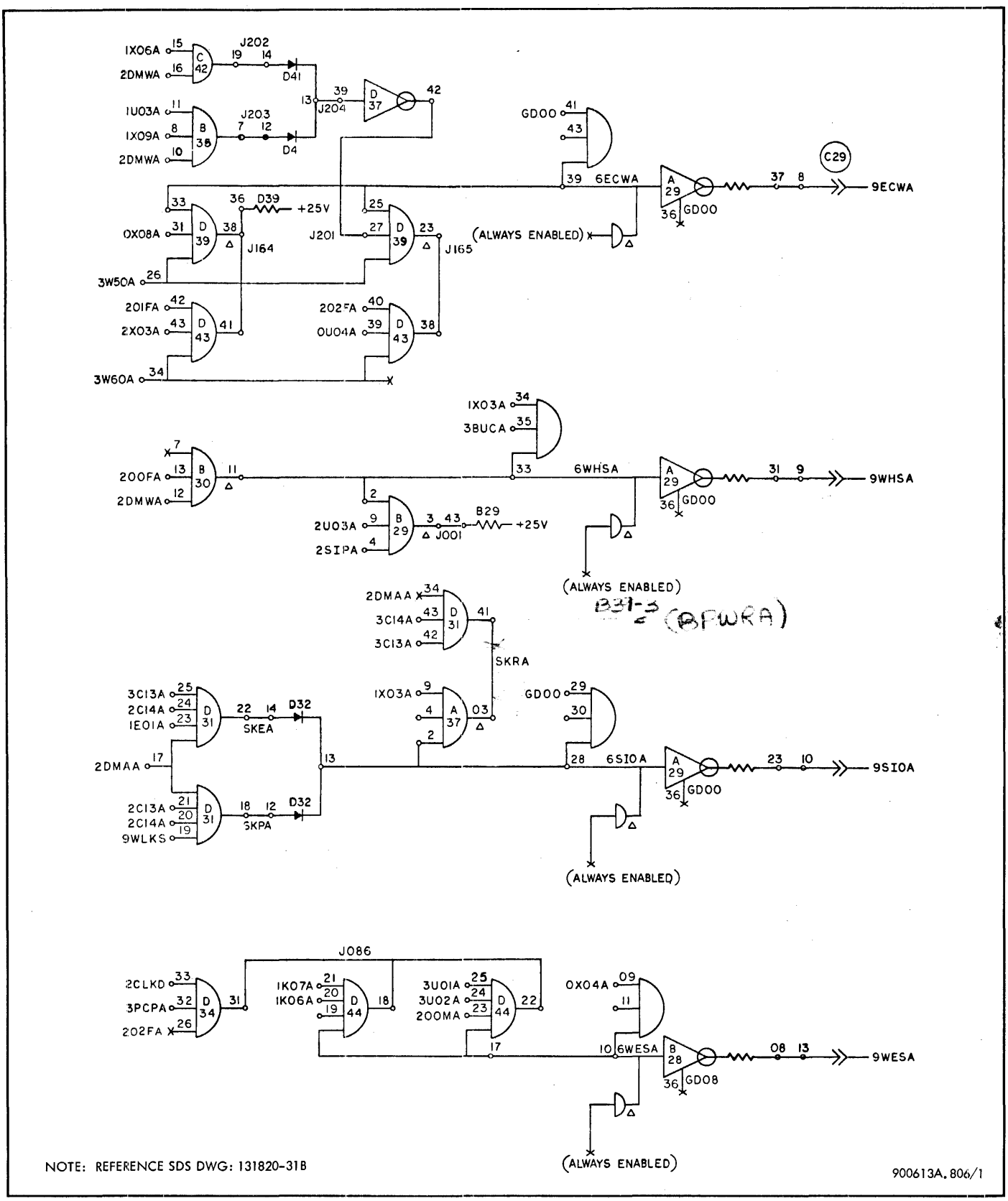
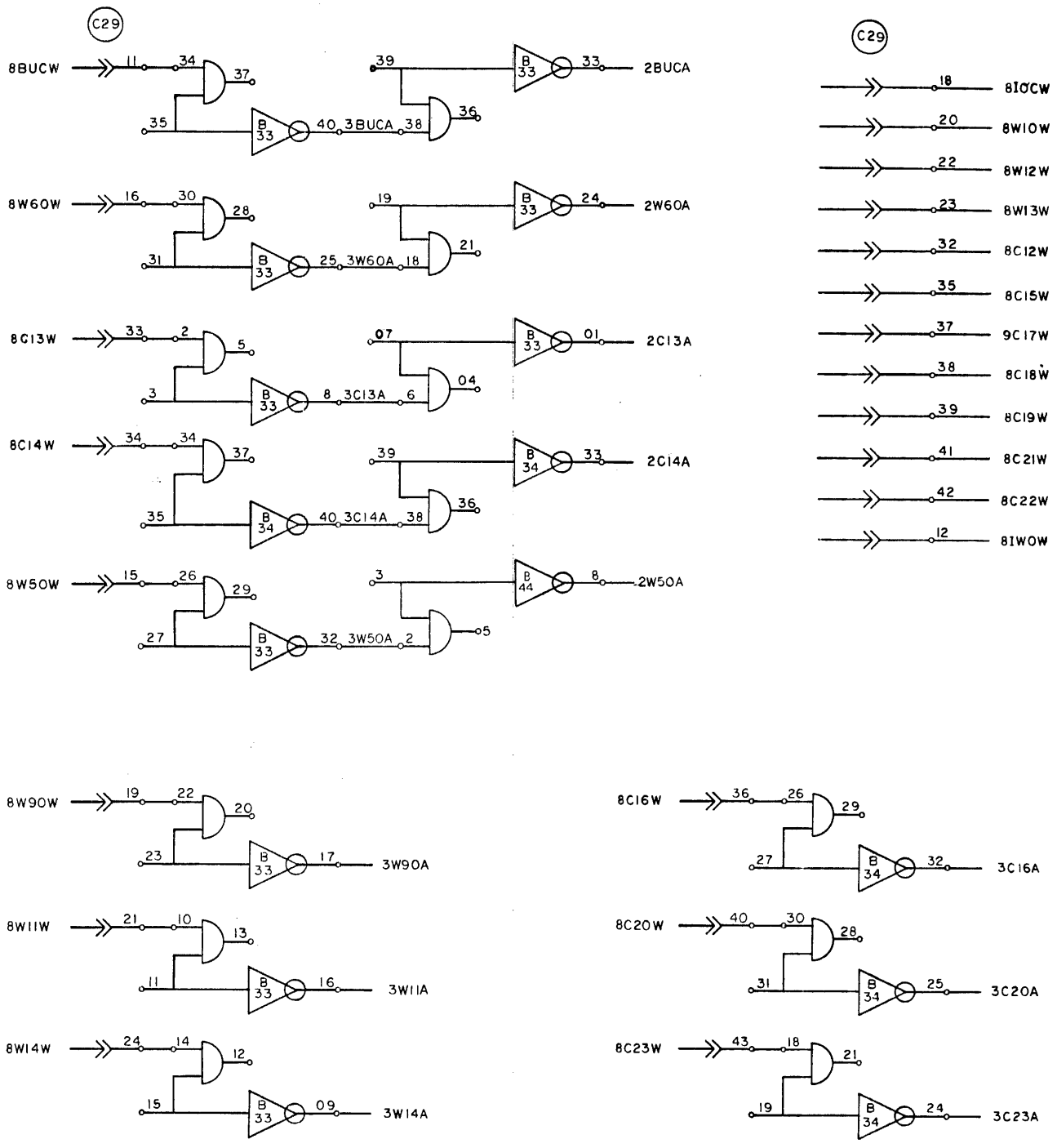


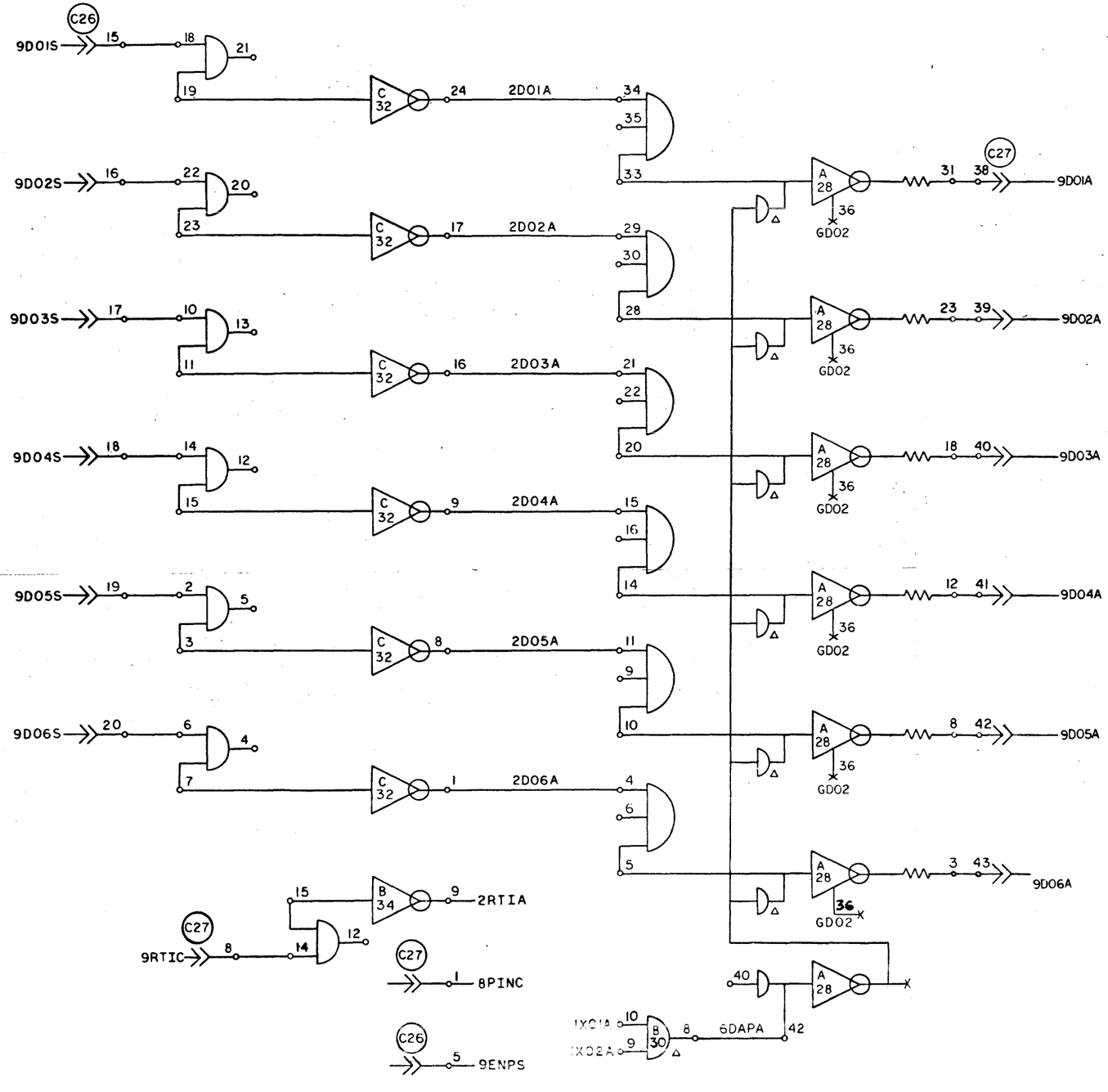
Figure 8-15. Controller Input and Output Signals Logic Diagram (Sheet 1 of 3)

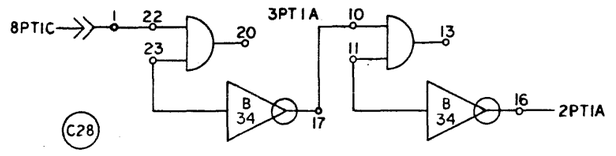


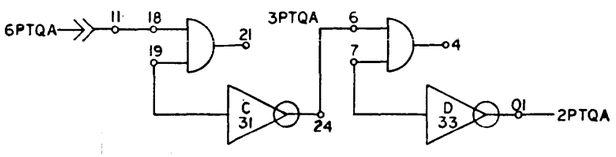
NOTE: REFERENCE SDS DWG: 131820-32B

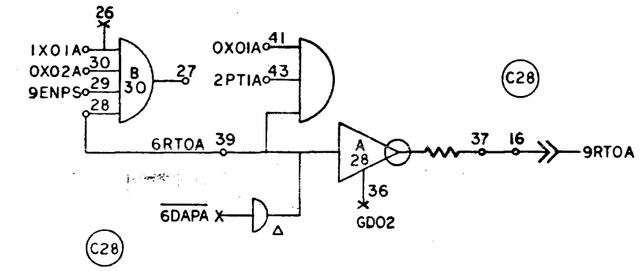
900613A.806/2

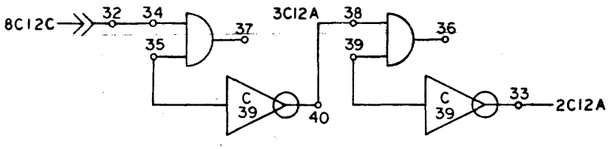
Figure 8-15. Controller Input and Output Signals Logic Diagram (Sheet 2 of 3)

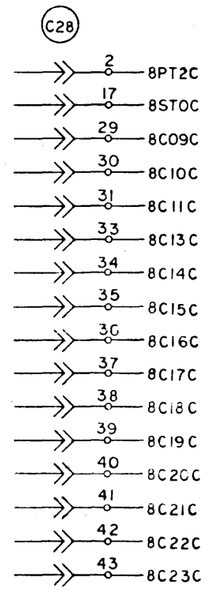


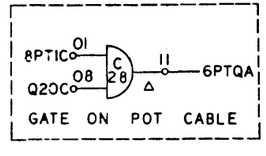












NOTE: REFERENCE SDS DWG: 131820-5B, 34B

Figure 8-15. Controller Input and Output Signals Logic Diagram (Sheet 3 of 3)

900613A.806/3

NATIONAL SOFTWARE SUPPORT MEMORANDUM

64.87.855.01
5 May 1966 (NS6-27)
Rev. 1 November 1, 1966

Subject: PROGRAMMING THE 9367 RAD FILES

From: Jim Gaines

To: Manual Distribution

This NS manual insert provides some perspective on the 9 Series 9367 RAD File.

Jim Gaines

Distribution: Applications Analysts, District Managers, J. DeBetz, Reider Andersen, D. Cizek, J. Sweeney, L. Raphael, S. Schwartz, E. Thompson, R. Nesbitt, S. Zasloff, P. Lebowitz, B. Reid, B. Hartman, D. Taylor (2), H. Tuens, B. Mallonee, National Software Support

JG:cep

64.87.855.01.01
1 November 1966

PROGRAMMING THE 9367 RAD FILES

There is a new product bulletin (64-17-02B (Rev. 2)) which describes both the 9366 and 9367 RAD files. The intent of this memo is to provide some perspective on these files, to explain terminology used in their description and to illustrate techniques of programming the 9367 (fast) RAD. A separate memo on programming the 9366 (slower) RAD will be generated at some time in the future. It is hoped that the product bulletin, supplemented by these descriptions will give the information you require. The contents and specifications described herein are subject to change, and are not binding on SDS.

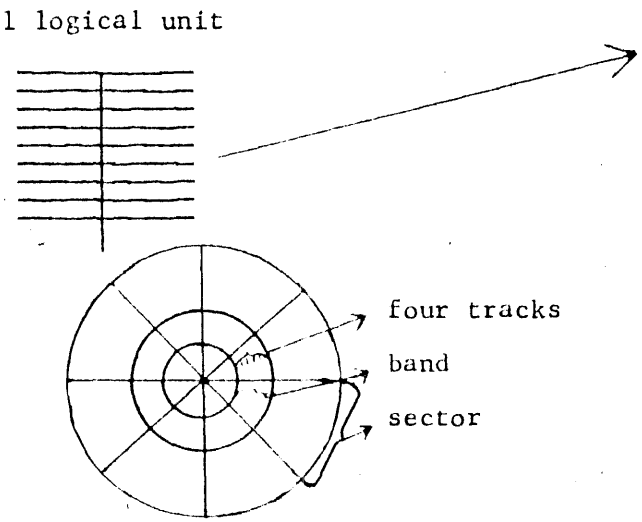
First of all, the 9366 is applicable to the SDS 910/920 only. The 9367 is applicable to the SDS 92, 925, 930, 940 and 9300 only. Since the 9366 can only be attached to a 910/920 Y-Buffer with a 9321 interlace and 912424 24 bit Y buffer, the product bulletin illustrates the EOM/SKS instructions for the 9366 with the Y buffer bit on.

Secondly, the remaining discussion on the 9367 is intended to promote a clear headed way of thinking about this RAD file from a programming point of view, and should not be mis-construed as an exact physical description. In this sense we can compare it to Sigma virtual addresses of data locations being independent from actual core locations as affected by memory mapping and interleaving.

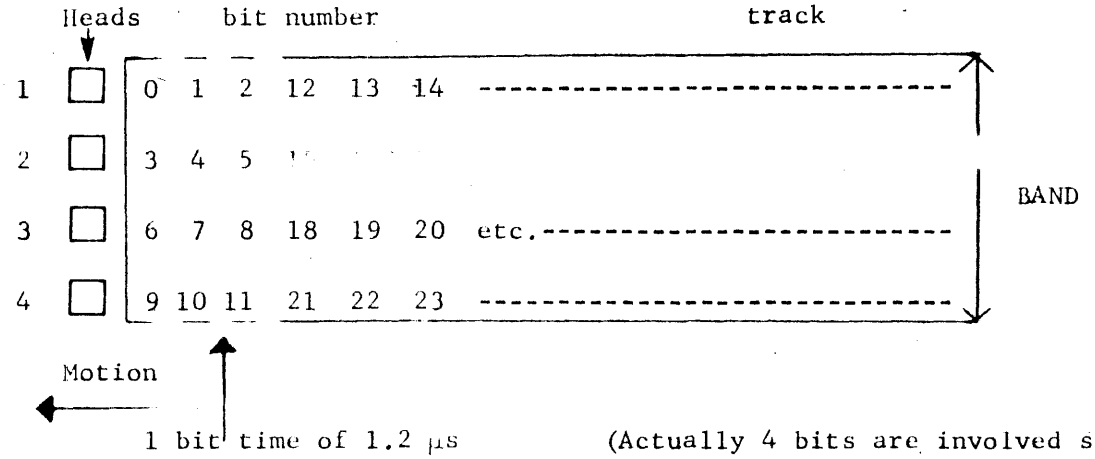
A 9367 RAD controller is attached to an I/O channel. Each controller may control from one to four storage devices. Devices come in three sizes: 524,288 6-bit characters, 1,048,576 6-bit characters or 2,097,152 6-bit characters. The 2 million character storage device is treated as two logical storage units of 1,048,576 characters each. Thus the maximum capacity per controller is 8,388,608 characters.

Each storage unit contains 64 bands (32 bands for a 524,288 character unit), each band contains 64 sectors, and each sector contains 256 6-bit characters. Thus each band contains 16,384 characters or 4096 words. Areas of the 9367 storage are thus addressed by specifying the particular unit, band, and sector. Each particular band is actually recorded in four physical tracks, each with a separate read/write head, thereby eliminating the mechanical complexity and positioning time that are characteristic of movable arm disc files. Note that the word "track" when used with the 9367 RAD file does not describe a program addressable element.

Physically then, the storage unit may be thought of as follows:



The read/write heads actually pick-up/record information four tracks (one band) at a time. A memory word is thus actually recorded in the following way:



Due to the organization of 4 tracks per band, recording of 6-bit characters must be done in multiples of two characters (12 bits) which is what the coupler requires. This means that a 24-bit word to the coupler looks like two 12 bit characters. This is the explanation for selecting the two character per word mode of the EOM when programming the RAD file.

PROGRAMMING CONSIDERATIONS

The rotational latency (35 msec maximum) can be minimized when large blocks of data are transferred between the computer and the Model 9367 RAD unit. This type of large block transfer is frequently encountered in applications such as time sharing and very large simulation problems employing program "overlay" techniques.

A combination of hardware and programming minimized latency. The unit sector address is continually maintained in the coupler. Successive sector addresses are noted and counted, as the bands revolve, as a 6-bit number between 00 and 77 (octal).

The current sector address of any device can be read by the computer's program at any time by an EOM/PIN. Thus, the program can compute the optimum starting point for a data transfer, as illustrated in the following example:

Assume the program is to transfer 010,000 (octal) words from core memory locations 005720-015717 onto sector locations 004200-004277. (band 42, all sectors) Assume that the current sector address is 043. These steps occur:

1. The program tests for coupler ready with an SKS instruction.

2. The program executes an EOM/PIN. The current sector address (043) is read into the computer.

3. The program adds two to the sector address, making it 045. This insures that one sector time is available to the program before reading or writing occurs.
   (The unit could be very near to the end of sector 043 when read and, hence, into sector 044 before a read or write could be initiated, therefore imposing a full rotational delay.)

4. The program sets up two I/O file operations.

   A. The first causes core locations 012420-015717 to be written onto sectors 004245-004277.

   B. The second causes core locations 005720-012417 to be written onto sectors 004200-004244.

In this example, 4096 words are transferred in about 35 msec. If normal programming had been used with the entire record started at sector zero, the operation would have taken almost 50 msec, due to the latency encountered, while the unit rotated from sector 44 to sector 00. Thus, the immediate access capability of the Model 9367 reduced the transfer time by about 30 percent.

NOTE: When a read or write operation is in progress on any of the units connected to the 9367 controller, it is not possible to PIN the current sector address of any of the attached storage devices.

TIMING NOTE

In all cases, the address POT must occur one or more sectors before the start of the desired sector, or one band time is lost.

OPTIONAL PRIORITY INTERRUPT LINE

The 9367 supplies a momentary signal for use in the priority interrupt system. It occurs near the start of the disc sector on which the address matches the contents of the sector address register. Thus it is possible to POT an address n and be interrupted in time to set up a read or write operation on sector n+1.

FILE PROTECTION

Both Model 9366 and Model 9367 RAD units contain provision for manual write protection. A group of toggle switches selectively inhibit writing on band groups associated with each switch. There are a total of sixteen switches, each controlling eight bands, or 32,768 words of storage each. Unimplemented bands on a .5 million character unit will test as file protected if addressed, and the switch for the unimplemented band is set to the protected position.

ADDITIONAL CONSIDERATIONS

The minimum unit written at any time on the RAD is a sector, and all transmission must begin on a sector boundary. If the word count controlling an output operation is not equal to zero modulo 64, the remainder of the last sector will be written as zero (erased). The amount transmitted to memory for an input operation is limited of course to the actual word count specified.

Sector incrementing is automatically performed by the coupler when more than one sector is to be transferred. Unless inhibited, the band number will also be incremented after the last sector in each band if transmission passes a band boundary. It is not possible, however, to increment automatically to a different unit. This means that a single transmission on 2 million character double unit cannot cross the boundary from the first million characters to the second. They are, from a programming point of view, two separate units. Addressing is, therefore, continuous within a unit but not continuous from unit to unit. Similarly, if a million characters of storage are set up as two .5 million character units, it is not possible to increment automatically across the unit boundary.

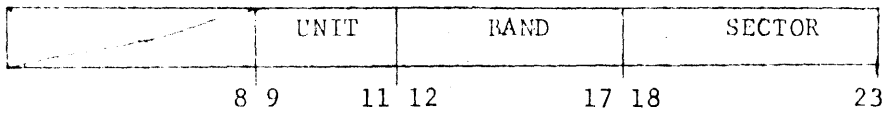
EOM/SKS COMMANDS

The following EOM's and SKS's are applicable to all models of the 9367 RAD files. All EOM's and SKS's are configured for channel A. The bits for channels other than A are the same as would be used for any other device controllers. The META-SYMBOL names and mnemonics are included.

SRA C SET RAD ADDRESS EOM 010026
where C=0-7, the channel number

Action: Alert to POT.

This EOM should be proceeded by the coupler ready test and be immediately followed by a POT instruction whose effective address contains the desired address in the following format.

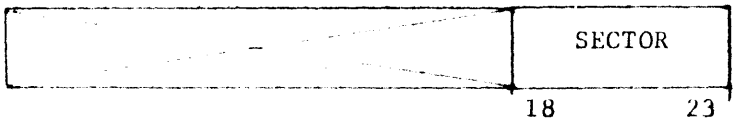


SRAI C SET RAD ADDRESS AND INHIBIT BAND INCREMENT EOM 011026
where C=0-7

Action: Alert to POT and inhibit increment. In addition to performing the function described in the previous alert EOM, this instruction will inhibit the normally automatic incrementation of the band address after sector 77_8. This feature is required to implement the "immediate addressing" technique described in example #3, (Pg. 12).

PRS C,U PIN RAD SECTOR EOM 01U226
where C=0-7; U=0-7 logical units

Action: Alert to PIN. This EOM is immediately followed by a PIN instruction. After execution of the PIN, the contents of the effective address of the PIN will contain the current sector address for the unit specified by U (0-7) in following format.



The PIN instruction will be acknowledged immediately with the exception of a 10 microsecond period at the end of each sector during which time the sector address is incremented.

RRAD C,U,CC READ RAD EOM 02226
WRAD C,U,CC WRITE RAD EOM 02266

Action: Connect for read or write
where CC=1 for 9366 RAD
=2 for 9367 RAD

Standard buffer control (BUC) EOM's are used to connect for read or write using unit addresses 26_8 and 66_8 respectively in the 2 character/word mode.

RRT C RAD READY TEST SKS 010026

Action: Test Coupler Ready

Execution of this instruction will result in a skip if the coupler is ready. The coupler will test not ready if there is a power loss, if the coupler is addressed, or the read/write circuitry is in use. (The words coupler and controller are interchangeable).

FILE PROTECTED TEST

RFPT C RAD FILE PROTECTED TEST SKS 013026

Action: Test for File Protected

Execution of this instruction will result in a skip if the addressed band is not file protected and can be written on. This instruction will not result in a skip if the addressed band is one of eight bands designated protected by a manual switch which is set to the protect position.

> NOTE: Addressed POTted to the RAD controller are not transmitted to the RAD Selection Unit until the next available gaptime. This means that if an RFPT (SKS Write Protect) is performed immediately after the set RAD address POT instruction, the SKS response will refer to the last address held in the Controller's address register rather than the one just POTted. Therefore, a minimum of one sector delay must be programmed to perform the POT/SKS operation.

RET C RAD ERROR TEST SKS 011026

Action: Test for Error in Coupler

Execution of this instruction will result in a skip if no error conditions were encountered. Any one of four (4) conditions in the coupler will result in an error.

1. If the coupler receives or increments into an unimplemented address, or increments across a unit boundary, the error indicator is set and the channel is disconnected. The I1 interrupt will not occur.

2. If the couplers monitoring electronics detect device fault, the error indicator is set and the channel is disconnected. The I1 interrupt will not occur.

3. If a write protected area is specified/encountered during a write operation the error indicator is set and the channel is disconnected. The I1 interrupt will not occur.

4. If either of the alert to POT EOM's are executed when the coupler is busy, the error indicator will be set. The on going operation is only affected by the presence of the error indicator i.e. the channel is not disconnected by the coupler.

CHANNEL ERROR TEST

SKS 011000

For a write operation the channel error will only be set if a data rate error exists. This condition occurs if the channel is not prepared to transmit the next character when requested by the coupler.

For read operation, three distinct conditions will set the channel error.

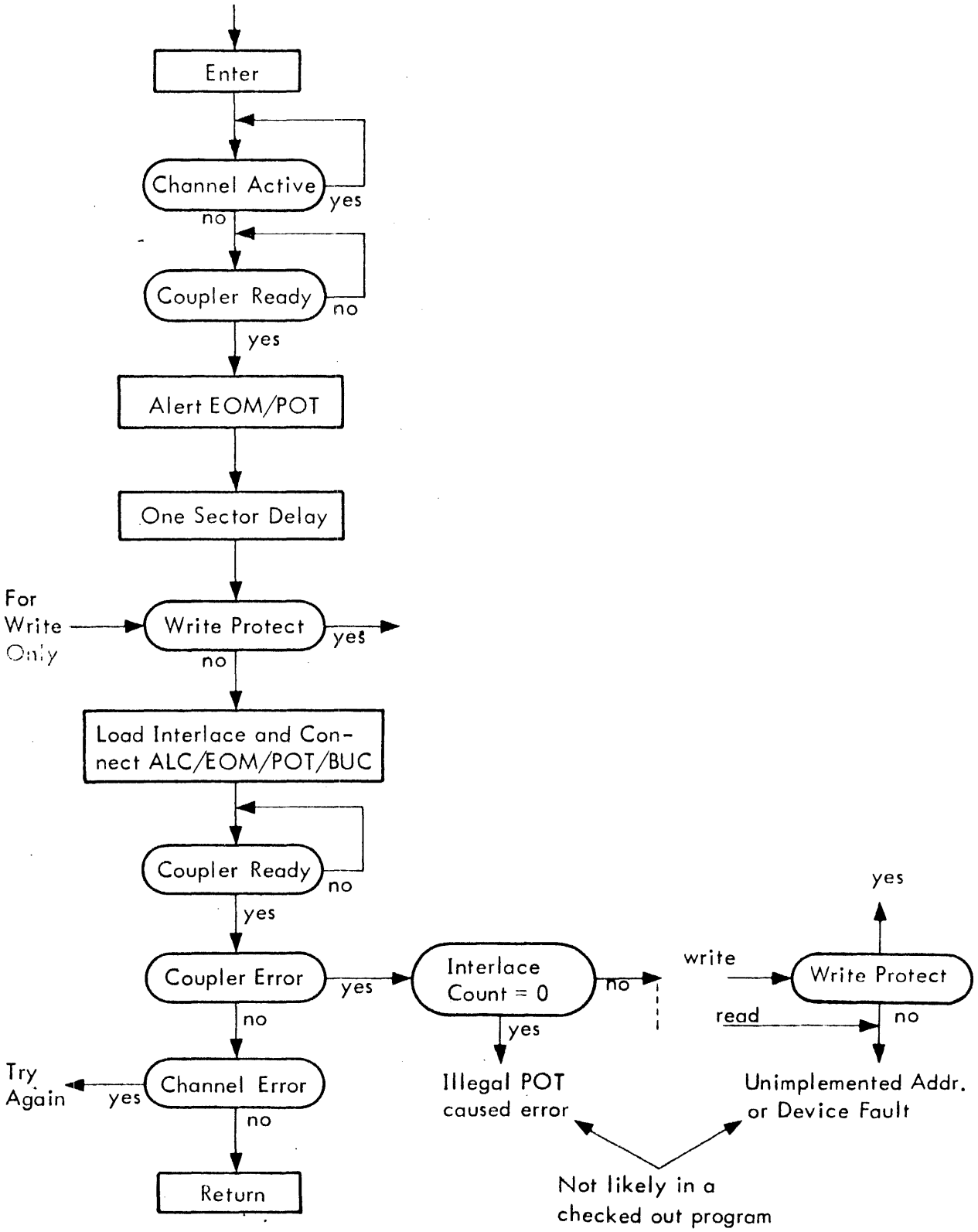
1. A data rate error occurs if the channel is not prepared to receive the next character from the coupler.

2. The channel error will set if the channel detects bad parity on the input character.

3. The channel error will be set if the coupler detects an error via the end of sector parity bits.

EXAMPLE #1

This flow chart describes the requirement for a typical read or write transmission without interrupts.



EXAMPLE #2 *

Code required to implement flow-chart of example #1 for a write operation.

```
*           WRITE 64 WORDS OUT FROM 01000 ONTO UNIT 0, BAND 1, SECTOR 0.
WRITE       PZE     0
            SKS     014000          CHANNEL ACTIVE
            BRU     $-1             YES
            SKS     010026          COUPLER READY
            BRU     $-1             NO
            EOM     010026          ALERT TO POT
            POT     ADDR            POT COUPLER ADDR.
            LDX     =0177343        ONE SECTOR
A           BRX     A               DELAY
            SKS     013026          IS IT WRITE PROTECTED
            BRM     PROTECT         YES. GO TO PROTECTED ROUTINE
            ALC     0               ALERT INTERLACE
            EOM     014200          IOSD, NO INTERRUPTS
            POT     OUTPUT          64 WDS, 01000
            EOM     02266           CONNECT WRITE
            SKS     010026          COUPLER READY
            BRU     $-1             WAIT
            SKS     011026          COUPLER ERROR
            BRU     ERROR           WHAT TYPE
            SKS     011000          CHANNEL ERROR
            BRU     RETRY           AS REQUIRED
            BRR     WRITE           RETURN
ERROR       SKS     012000          INTERLACE COUNT=0
            BRU     ILLEGPOT        ILLEGAL POT
            SKS     013026          WRITE PROTECTED
            BRM     PROTECT         YES. GO TO WRITE PROTECTED ROUTINE
            BRM     OPERATOR        NOTIFY OPERATOR OF ILLEGAL ADDRESS
                                    OR DEVICE FAULT
            BRR     WRITE           EXIT
ADDR        DATA    0100            UNIT 0, BAND 1, SECTOR 0
OUTPUT      DATA    04001000        64 WDS FROM 01000
```

*All data transmission must be performed with function code IOSD. The connect for read/write must follow the interlace load sequence.

Symbols external to this subroutine are assumed to have the following significance:

PROTECT: is a subroutine to handle the error condition that WRITE has been asked to output onto a file protected area of the disc. Note that the second file protect test in this particular example is not required, since the file protection applies to groups of eight bands and only one sector of one band was written. In general the test would mean that during automatic band incrementing, a new band was addressed for writing that was file protected, although the write was initiated for a non-protected band.

RETRY: is a routine which would attempt to recover from the error. For example it might decrement a count, branching to WRITE + 1 if more tries were to be attempted, and to an operator notification routine if the recovery attempt was unsuccessful. The recommended number of read/write tries attempted automatically is three.

OPERATOR: is a routine which will notify the computer operator of the error condition and take whatever action is required to terminate the job, etc.

similarly, ILLEGPOT is a routine to indicate that specific programming error.

EXAMPLE #3

(WRITE ONLY)

ON UNIT 1, BAND 2

WRITE ONE BAND, USING THE IMMEDIATE ADDRESS TECHNIQUE

WITHOUT INTERRUPTS

```
*          CALLING SEQUENCE ASSUMED IS
*            BRM     IMMED
*            DATA    LOC             FIRST OF 4096 WORDS TO BE WRITTEN (15 BIT ADDRESS
*
IMMED        PZE     0
             MIN     IMMED           STEP ENTRY LOCATION
             SKS     014000          CHANNEL ACTIVE
             BRU     $-1             YES
             SRA     0               COUPLER READY
             BRU     $-1             NO
             PRS     0,1             ALERT TO PIN UNIT #1
             PIN     SAVE            SAVE CURRENT SECTOR ADDRESS
             LDA     SAVE            CCE
             ETR     =077            LEAVE SECTOR ADDRESS ONLY
             ADD     =2              ADD TWO
             ETR     =077            CHECK FOR CURRENT SECTOR
             SKE     =0              NOT 62 OR 63
             BRU     $+2             SET UP OK
             ADD     =1              START AT SECTOR 1
             CLB                     CLEAR B
             LSH     6               MULTIPLY BY 64
             STA     SAVE            SAVE FOR POT WORD CALCULATIONS
             RSH     6               RESTORE UNIT NUMBER
             MRG     DISCAD2         MERGE WITH UNIT AND BAND
             STA     DISCAD1         TO SET UP FIRST SECTOR WRITTEN
```

```
*     THE CODE FROM HERE TO LABEL EOM IS NOT
*     PART OF THE I/O, BUT MERELY SET-UP COMPUTATIONS
*     FOR THE INTERLACE POT WORDS AND WT-COUNT BITS
*     IT DOES SERVE TO ILLUSTRATE THE BOOKKEEPING REQUIRED.
*     OBVIOUSLY, IF THE DISC UNIT AND BAND WERE ALSO
*     ROUTINE PARAMETERS, MORE SET-UP THAN ILLUSTRATED
*     WAS REQUIRED BEFORE THIS.

              LDA     *IMMED          GET DATA LOCATION
              ETR     =077777         TO 15 BITS
              LDB     SAVE            FIRST SECTOR *64 IS WORD COUNT
              BRM     FEOMPOT         FORM EOM/POT WORDS
              STA     EOM2            FOR SECOND TRANSMISSION
              STB     SECOND          AND STORE THEM
              LDA     =4096           FORM WORD COUNT
              SUB     SAVE            FOR FIRST TRANSMISSION
              CAB                     PUT IN B FOR FEOMPOT CALL
              LDA     *IMMED          GET DATA LOCATION
              ETR     =077777         PLUS WORDS TO BE DONE WITH
              ADD     SAVE            SECOND TRANSMISSION AS LOCATION
              BRM     FEOMPOT         AT WHICH FIRST TRANSMISSION BEGINS
              STA     EOM1            SAVE EOM/POT FOR
              STB     FIRST           FIRST OUTPUT DONE
EOM           SRAI    0               ALERT TO POT AND INHIBIT
              POT     DISCAD1         1ST DEVICE ADDRESS
              ALC     0               ALERT INTERLACE
EOM1          EOM     014200          IOSD, NO INTERRUPTS
              POT     FIRST           1ST TRANSMISSION
              WRAD    0,1,2           CONNECT WRITE
              SKS     014000          WAIT FOR CHANNEL READY
              BRU   - $-1
```

```
            ALC                     RELOAD INTERLACE
EOM2        EOM     014200          IOSD, NO INTERRUPTS
            POT     SECOND          2ND TRANSMISSION
            RRT     0               COUPLER READY
            BRU     $-1             NO
            RET     0               COUPLER ERROR
            BRU     ERROR           AS REQUIRED
EOM3        SRA     0               ALERT TO POT
            POT     DISCAD2         2ND DEVICE ADDRESS
            SKS     011000          CHANNEL ERROR
            BRU     RECOV           AS REQUIRED
            WRAD    0,1,2           CONNECT FOR 2ND WRITE
            BRR     IMMED
DISCAD1     DATA    0
DISCAD2     DATA    00010200        UNIT 1, BAND 2, SECTOR 0
FIRST       RES     1               STORAGE FOR FIRST POT WORD
SECOND      RES     1               STORAGE FOR SECOND POT WORD
```

A note of explanation may help to clarify Example 3. ERROR is assumed to be a routine which will check whether the condition is due to a device fault, unimplemented address/file protected area, etc. as shown in the Example 1 flow chart, taking appropriate action. RECOV is a routine to bump a counter and retry the operation to see if the data rate error on the channel persists, notify the operator or calling program of the unsuccessful write, etc. Note that IMMED exits before completion of the second write operation, so channel and coupler ready and error testing will need to be done to verify a totally successful transmission. FEOMPOT is assumed to be a routine which given an address and count forms the IOSD EOM with the necessary high count and high order address bits, and generates the POT word in a FORM 10, 14.

For simplicity, no attempt was made to take advantage of the case when the band could be written at sector zero with just one write operation. Special code for this case would save in excess of 500 microseconds of output time when the condition existed, or assuming a 1/64 probability, an average of 8 microseconds would be saved.

Finally, a note about the order in which the code is written may be helpful. The first test on the channel (EOM1 + 3) waits for the zero word count condition. Since the coupler will still be busy, this time is used productively to reload the interlace for the second output required, and then the wait for coupler ready is performed. The existing status of the coupler error flip flop is then tested. Then the channel error indicator is tested before the final connect for write, which reset the channel indicator.

RECOVERY PROCEDURE

Disregarding critical applications, it is recommended that no more than three attempts be made to read or write a portion of the file.

OTHER PROGRAMMING CONSIDERATIONS

1. Care should be exercised when using the I1 (zero word count) interrupt or the count zero test (SKS 012000) since the coupler may disconnect (before count zero) for reasons described previously in the section on coupler errors.

2. The occurrence of an I2 interrupt (or a skip on channel active test) is not necessarily synonomous with the coupler becoming ready. If the word count is modulo 64, the coupler on output must (after zero count) write the last data characters and the check character before indicating ready.

   If the count is no modulo 64, the coupler will be busy after the I2 until trailing words of zero and the check character are written or until the end of the current sector is reached and the check character is verified for reading.

Reference

This diagnostic is available:

SDS 925/930 RAD Aposalyptic
Diagnostic, Prog. No. 594003.

JG:cep