LAL	REVISIONS					154991	B
	REV.	DESCRIPTION		CHK	DATE	APPROVED	
	A	ENGR RELEASE		BZ	8/13/69	JW 8-14-69	
X	B	MFG RELEASE	NO E.O.	BZ	10/15/69	RB 10/15/69 BMK	

CONTROL DRAWING 131

NO. REQ.	DRAWING NO.	DESCRIPTION	REFERENCE DESIGNATION	ITEM NO.

MATERIAL LIST

NOTES UNLESS SPECIFIED

1. TOLERANCES
   .XX ±.030 ANGULAR
   .XXX ±.010 ±½°
2. BREAK ALL SHARP EDGES .010 APPROX.
3. MACH. SURFACES √
4. ALL DIM. IN INCHES

DRAWN	I. Linkous	8-11-69
CHECK	B Zilk	8-13-69
APPR.	JW Baker	8-13-69

SDS
EL SEGUNDO, CALIFORNIA

TITLE

PRODUCT DESIGN SPECIFICATION
INPUT/OUTPUT PROCESSOR, MULTIPLEXING

MODEL NO.	CODE IDENT. NO. 18338	SIZE	DWG. NO.	CHANGE LETTER
8273/8473		A	154991	B
NEXT ASSY. 154560	SCALE	DO NOT SCALE DRAWING	SHEET 1 of 83	

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1.0 INTRODUCTION

1.1 Scope

This specification defines the design requirements for a free-standing multiplexer IOP (MIOP) with optional four-byte data path, memory-bus sharing, and display option to be used with Sigma 5 or Sigma 7 systems. This specification includes the actions and responses required by the MIOP at the CPU interface, the device controller (DC) interface, the core memory interface, and the maintenance subcontroller (MS) display interface. In addition, this specification defines the various required internal IOP operations and sequences.

1.2 Related Documents

Product Planning Specifications:

Sigma Document 316, Planning Specification: Multiplexor IOP with Optional Four-Byte Data Path and Optional Memory Bus-Sharing.

Product Design Specifications:

117336	Specification, Central Processing Unit
117653	Specification, Sigma Memory
123382	Specification, Eight-Bit Data Path
137556	Specification, Four-Byte Data Path
154169	Specification, Maintenance Subcontroller

1.3 General Description

1.3.1 Basic Features

The basic MIOP, model number 8273/8473, provides for coupling Sigma peripheral units to a Sigma 5 or Sigma 7 CPU and core memory. The MIOP responds to service requests from either the CPU or DC's in a time multiplexed fashion. Capability is built into the MIOP which allows it to direct and control I/O operations by executing a command list prepar ed by the CPU.

The basic MIOP provides 8 sub-channel positions to accomodate 8 DC's. Each DC that utilizes the basic 8 sub-channel positions may have as many as 16 devices connected. The data path interconnecting the basic MIOP with DC's is one-byte (8-bits) wide.

At the core memory interface, the MIOP has the capability for addressing memories as large as 131,072 words (524,288 bytes).

1.3.2 Optional Features

A model 8273/8473 MIOP may be supplied with the following optional features:

Model 8274/8474	Bus-sharing feature
Model 8275/8475	Four-Byte interface feature
Model 8276/8476	Additonal eight sub-channels.
Assy. 154999	Display Option. This option is useful only when a Maintenance Subcontroller (154543) is connected to the MIOP.

The model 8274/8474 bus-sharing feature permits two model 8273/8473 MIOP's to share a core memory bus on a time-shared basis. This optional feature consists of a group of modules that are installed into the two MIOP's that are to share the core memory bus.

The model 8275/8475 four-byte interface feature consists of a group of modules that extends the width of the data path at the DC interface from one-byte to four-bytes. This feature enables those DC's that also contain a four-byte wide data path to transmit data at a higher rate than is possible via the one-byte path and thus improve the data throughput for the I/O system.

The model 8276/8476 option consists of a group of modules that provides an additional eight sub-channels to the basic model 8273/8473 MIOP. The MIOP will accommodate a maximum of 24 sub-channels. That is, in addition to the basic eight sub-channel positions a maximum of 16 optional sub-channel positions may be provided in groups of eight. The basic eight sub-channel positions only (addressed 0 through 7) may be used for servicing DC's with multiple devices.

The IOP display option (154999) contains a group of modules that provides the display interface for maintenance purposes. When the option is installed, the MIOP, under program control, can be operated in single phase mode and can send the states of 112 internal signals (16 at a time) to a CPU general register using Read Direct and Write Direct instructions via the DIO interface and the Maintenance Subcontroller, MS.

1.3.3 Functional Requirements

The MIOP responds to service requests from either the CPU or from DC's. In response to service requests from the CPU the MIOP performs operations related to the execution of SIO, TIO, HIO, TDV, and AIO instructions. In response to service requests from DC's the MIOP performs operations designated as Data Out,

Data In, Order Out, and Order In. During the responses mentioned above the MIOP may perform or control certain operations required by the I/O system as follows:

Generation and Transmittal of Terminal Orders

Data Chaining

Command Chaining

Transfer in Channel

Retrieval, Generation, and Storage of Status

Error Checking

2.0 DETAILED DESCRIPTION

2.1 System Interconnection

The IOP's interconnect with the CPU, Memories, Device Controllers, and Maintenance Subcontrollers, as shown in Figure 2.1. IOP's shall be connected by cables to the CPU in a trunk-tail fashion for the purpose of interrupt priority determination. Addressing of eight IOP's is permitted. All IOP's connected to a given CPU shall be connected to the memory bank containing address X'20" and X'21' for that CPU. However, all IOP's need not be connected to all memories. Device Controllers shall be connected to the IOP at the Display Interface through a 100 Ω ribbon cable.

The MIOP may be connected to the Device Controllers and MS with a one byte, or a four byte data path (I/O interface). Also, the MIOP shall be connected by priority cable to the Device Controller and MS for the purposes of service priority determination. The rules of priority assignments to the Device Controllers are described in 123382 and 137556.

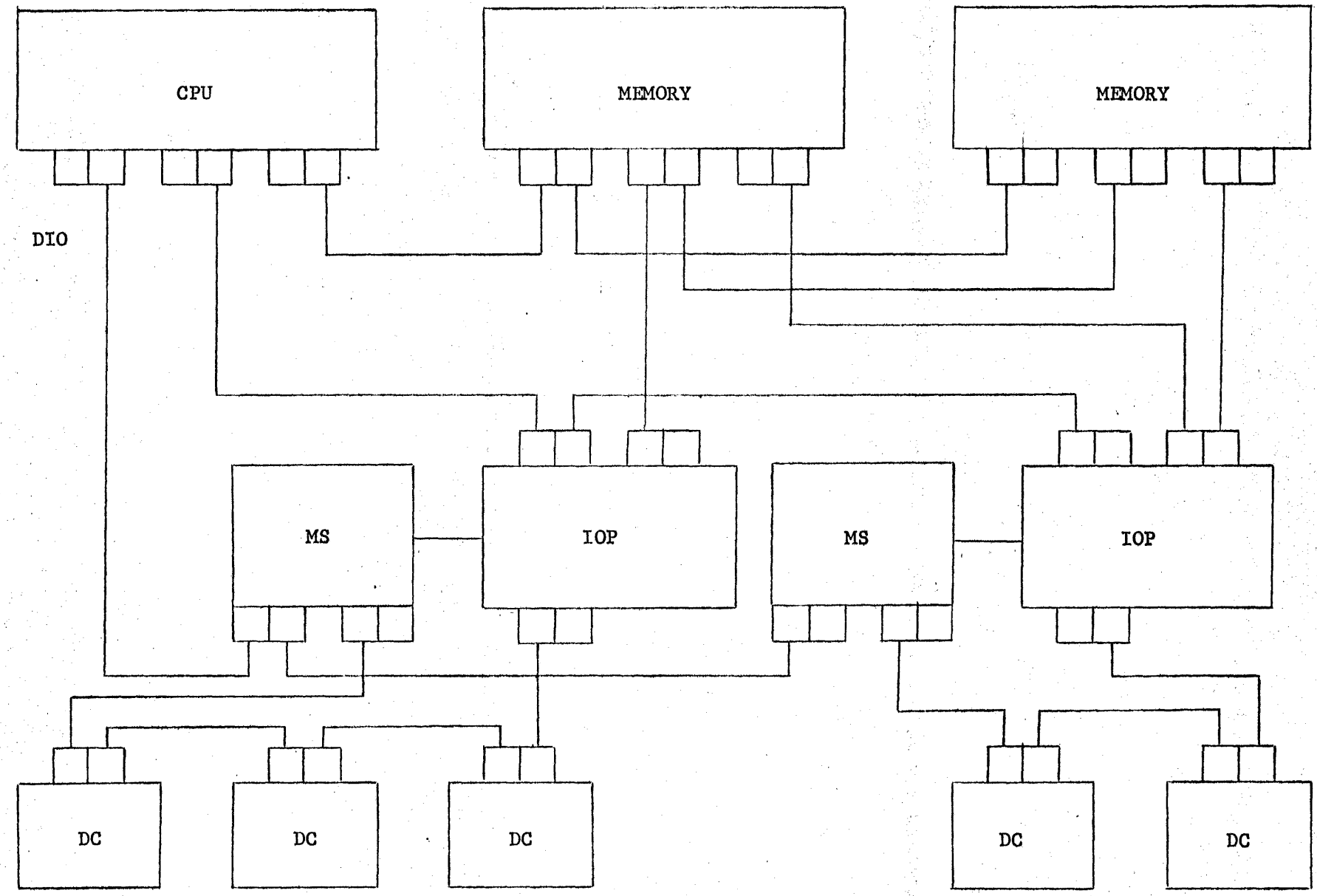

FIG. 2.1 SYSTEM DIAGRAM

TITLE PRODUCT DESIGN SPECIFICATION INPUT/OUTPUT PROCESSOR, MULTIPLEXOR	SDS 154991 B SHEET 9 OF 83

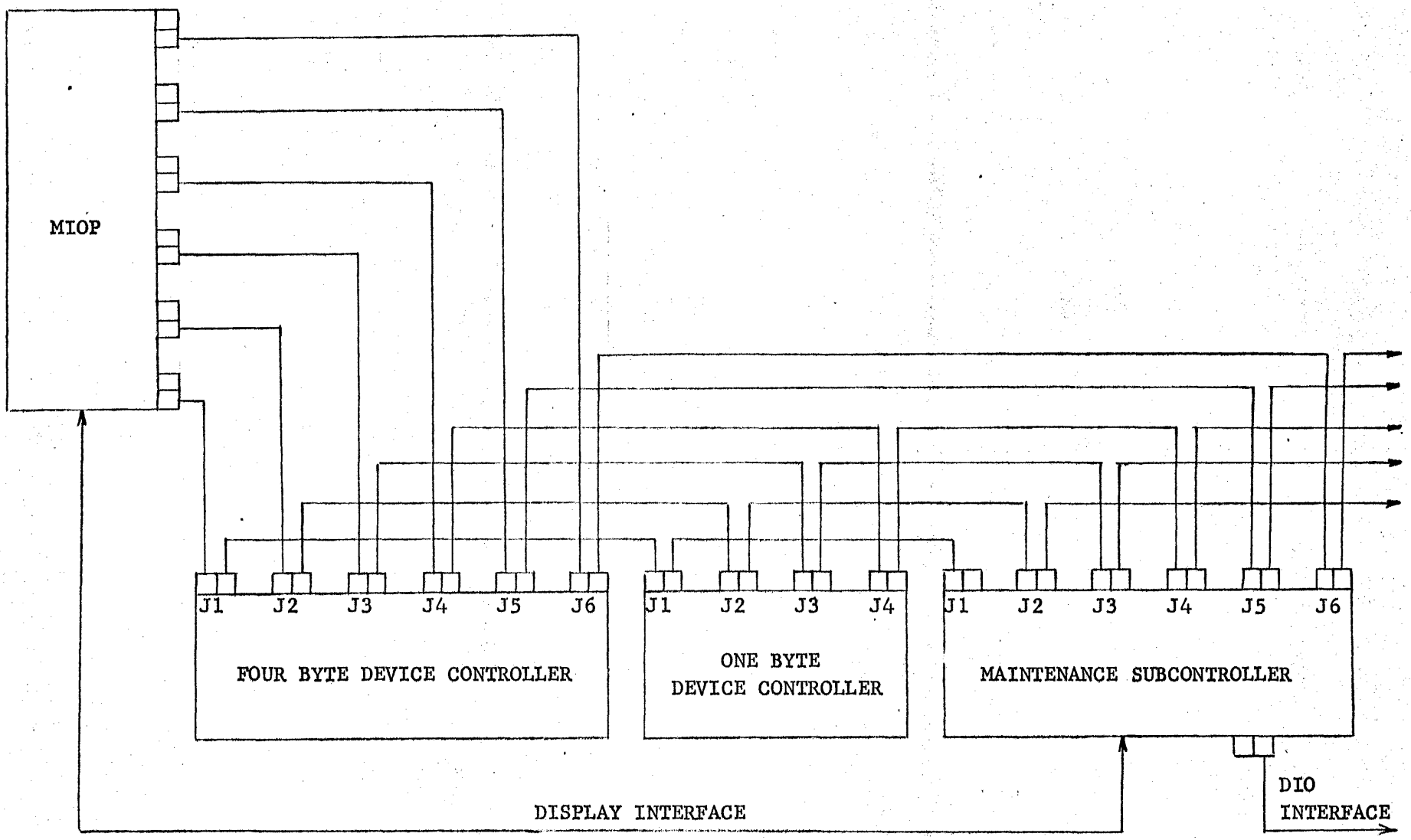

FIGURE 2.2 MIOP TO DEVICE CONTROLLER AND MS CABLING

TITLE	SDS	
PRODUCT DESIGN SPECIFICATION INPUT/OUTPUT PROCESSOR, MULTIPLEXOR	154991	B
	SHEET 10 OF 83	

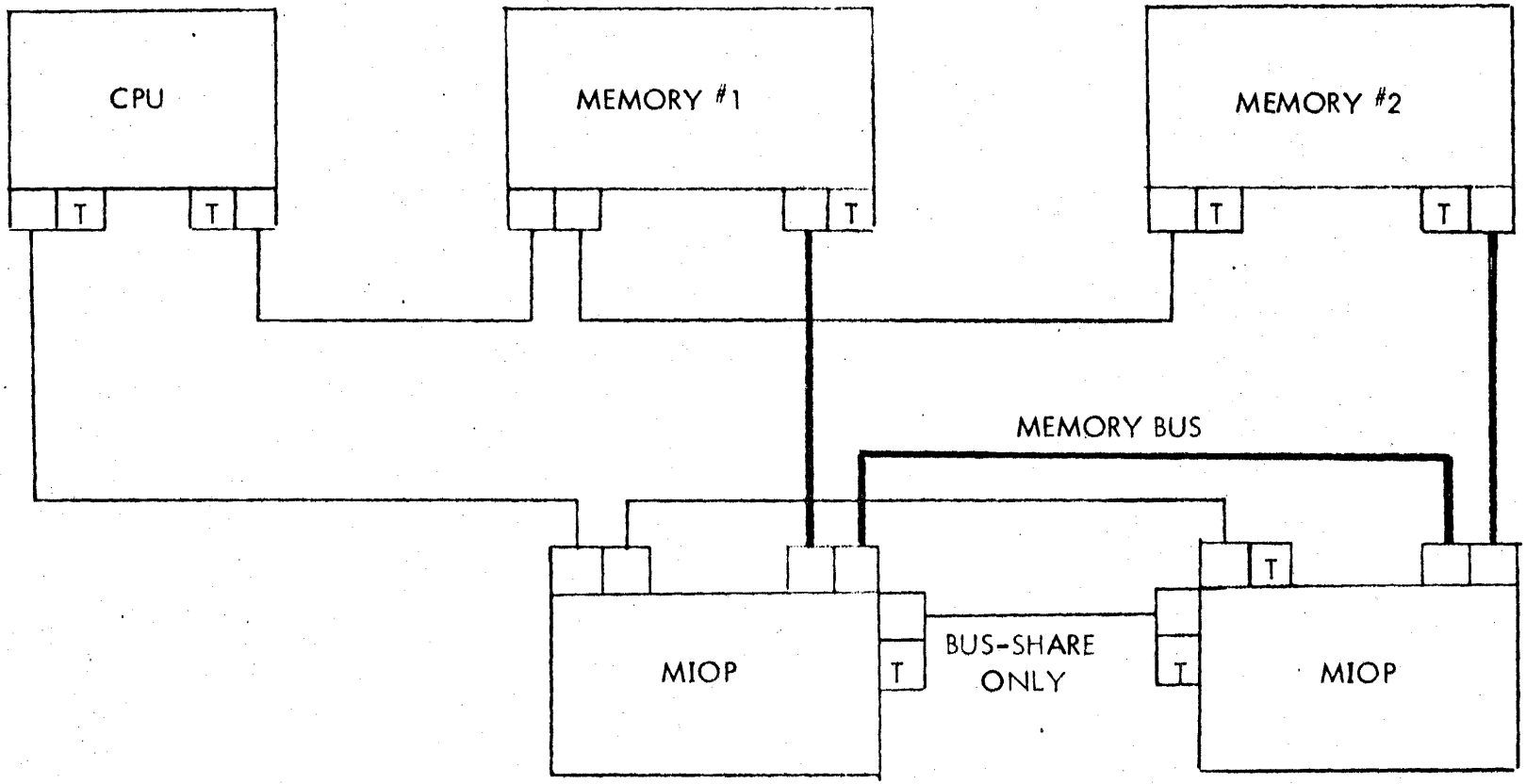

Fig. 2.3 BUS-SHARING MIOP'S

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2.2 Interface Signal Transmission (Except Display Interface)

All interface signal exchange shall be via AT10 Cable Receiver Module (SDS Part No. 123018), AT11 Cable Driver/Receiver Module (SDS Part No. 123019), AT12 Cable Driver Module (SDS Part No. 124629), AT13 Cable Driver/Receiver Module (SDS Part No. 125260), AT61 Cable Driver Module (SDS Part No. 149481), or AT70 Cable Driver/Receiver Module (SDS Part No. 152815) as used throughout the Sigma system.

Communication shall be via terminated shielded conductors having a nominal impedance of 33 ohms. The signal transmission cable consists of 14 shielded conductors as specified under SDS Part No. 101787. Cable connectors are SDS Part No. 115833. These connectors provide for mating with 14 printed wiring contacts on cable plug modules. Cables shall be terminated at the extremities with 33 ohm resistors to ground. The terminating plug assemblies (containing the 33 ohm resistors) are SDS Part No. 127315.

The signal characteristics on the cable shall be as follows:

Logical One = + 2 volts

Logical Zero = 0 volts

2.3 MEMORY INTERFACE

2.3.1 Signal Convention

Signal exchange shall be via AT11 Cable Driver/Receiver, AT12 Cable Driver, AT61 Cable Driver, and AT70 Cable Driver/Receiver Modules. The signals will use a convention of +2 volts as true logic.

2.3.2 Busses

Each MIOP shall have a bus for interfacing with core memories. Two MIOP's may, however, share a core memory bus if the Bus Share option is present in both.

An IOP shall use only a single memory bus and shall not make a memory request before receiving an Address Release signal or an Address Here false signal from the prior request.

2.3.3 Cells 20 and 21

The MIOP uses memory cells 20* and 21* when responding to CPU requests for service. It shall be a requirement that the memory (memories if interleaving is used) that possess IOP memory cells 20* and 21*, must also possess CPU memory cells 20* and 21*. This requirement shall also be true for an IOP which is to provide the CPU with its initial information during a bootstrap load operation.

2.3.4 Ports

The IOP shall normally be connected either to memory port A or memory port B (memory port A having highest priority). However, there shall be no special form of implementation which would preclude the IOP from using port C.

2.3.5 Signal Lines Interconnecting IOP and Memory.

The lines tabulated below interconnect the IOP and memory: (In the table, X refers to one of memory port A, B. or C.)

* Base 16

2.3.5 (cont'd)

Description	Designation	Number of Lines	Direction of Signal Flow	
			IOP to Memory	Memory to IOP
Data Signals	/MX0/ thru /MX31/	32	x	x
Address Signals	/LX15/ thru /LX31/	17	x	
Address Here	/AHX/	1		x
Address Release	/ARX/	1		x
Data Gate	/DGX/	1		x
Parity Error	/PEX/	1		x
Parity O.K.	/POKX/	1		x
Write Byte Signals	/MW0X/ thru /MW3X/	4	x	
Memory Request	/MQX/	1	x	
Data Release	/DRX/	1		x

2.3.6 Signal Timing

Timing of the signals described in 2.3.5 shall conform to the following: (All times as measured at IOP/Cable interface).

2.3.6.1 Data Lines

Data Input to Memory

During a core memory write operation signals on the data lines (MX0 thru MX31) shall be present and stable within 120 nanoseconds after the Memory Request (MQX) is given. The data lines shall remain stable for a minimum of 160 nanoseconds after the Address Release signal is received by the IOP for a full write operation or the Parity OK or Parity Error signal is

received by the IOP for a partial write operation.

Data Output from Memory

During a core memory read operation, signals on the data lines are strobed by the Data Gate Signal into the IOP memory Interface register. The data signals shall not change during the interval 80 nanoseconds before Data Gate falls until 65 nanoseconds after Data Gate falls.

2.3.6.2 Address Lines

Signal on the Address Lines (LX15 thru LX31) shall be stable not less than 90 nanoseconds before the Memory Request signal rises and shall remain stable until 20 nanoseconds after the Memory Request signal has been dropped by the IOP.

2.3.6.3 Data Gate Signal

The Data Gate signal strobes data into the IOP memory interface register during a core memory read operation. The Data Gate signal shall be a positive-going pulse not less than 80 nanoseconds in duration.

2.3.6.4 Parity Error and Parity OK

The Parity Error (PEX) and the Parity OK (POKX) signals shall be positive-going pulses not less than 70 nanoseconds wide and shall indicate the result of the parity check performed during a memory read or partial write operation by the memory.

2.3.6.5 Write Byte Signals

During a Memory full-write or partial write operation, the Write Byte (MW0X thru MX3X) signals shall designate the memory byte or byte into which data is to be written. These signals shall be present and stable within 120 nanoseconds after the Memory Request signal. They shall be present until the Address Release Signal is received at the IOP.

2.3.6.6 Memory Request Signal

The Memory Request signal shall come true when the IOP wishes to make a memory access. This signal shall remain true until the IOP receives the Address Release signal or the Address Here signal is false when strobed.

2.3.6.7 Address Release Signal

The Address Release shall be a positive-going pulse not less than 80 nanoseconds in duration that designates to the IOP that the address lines may be changed and that the Memory Request line may go false.

2.3.6.8 Address Here

The Address Here line when true shall designate to the IOP that the address coded on lines LX15 thru LX31 is an address implemented in the memory or memories to which the IOP is attached. The Address Here line shall be strobed no sooner than 260 nanoseconds after the Address Lines have settled.

2.3.6.9 Data Release Signal

The Data Release signal shall be a positive-going pulse not less than 80 nanoseconds in duration. During a core memory full write cycle initiated by the IOP the Data Release signal shall signify that the memory data lines may be released and that another memory cycle may be initiated.

2.3.7 CABLE LENGTH

The total IOP/Memory cable length shall not exceed 64 feet to the furthest Memory port, (with 8274/8474 Bus-sharing feature cable length shall not exceed 40 feet). The IOP may drive cables in two directions in order to minimize the cable length. All cables in the bus interconnecting an IOP with a particular Memory port shall be of the same nominal length.

2.3.8 CABLE AND CONNECTOR PIN ASSIGNMENT

Five cables are required to interconnect the IOP and memory. The pin assignment of signals in thos cables at the Cable Driver/Receiver and Cable Connector interface shall be as specified below:

Cable 1

AT11 Cable Driver/Receiver Module

Connector Pin	Signal Desig. at Connector	Signal Functional Description
2	/MX0/	Data Line, Port X
1	/MX1/	"
4	/MX2/	"
3	/MX3/	"
5	/MX4/	"
6	/MX5/	"
7	/MX6/	"
8	/MX7/	"
9	/MX8/	"
10	/MX9/	"
11	/MX10/	"
12	/MX11/	"
13	/MX12/	"
14	/MX13/	"

Connector Pin	Signal Desig. at Connector	Signal Functional Description
2	/MX14/	Data Line, Port X
1	/MX15/	"
4	/MX16/	"
3	/MX17/	"
5	/MX18/	"
6	/MX19/	"
7	/MX20/	"
8	/MX21/	"
9	/MX22/	"
10	/MX23/	"
11	/MX24/	"
12	/MX25/	"
13	/MX26/	"
14	/MX27/	"

Cable 3

AT70 Cable Driver/Receiver Module

Connector Pin	Signal Desig. at Connector	Signal Functional Description
2	/MX28/	Data Line, Port X
1	/MX29/	"
4	/MX30/	"
3	/MX31/	"
5	/LX29/	Address Line, Port X
6	/LX30/	"
7	/LX31/	"
8	/MW0X/	Memory Write Byte Line, Port X
9	/MW1X/	"
10	/MW2X/	"
11	/MW3X/	"
12	/DGX/	Data Gate Line, Port X
13	/EDRX/ *	Early Data Release Signal
14	Not Assigned	

* Not used by IOP

Cable 4

AT61 Cable Driver Module

Connector Pin	Signal Desig. at Connector	Signal Functional Description
2	/LX15/	Address Line, Port X
1	/LX16/	"
4	/LX17/	"
3	/LX18/	"
5	/LX19/	"
6	/LX20/	"
7	/LX21/	"
8	/LX22/	"
9	/LX23/	"
10	/LX24/	"
11	/LX25/	"
12	/LX26/	"
13	/LX27/	"
14	/LX28/	"

Connector Pin	Signal Desig. at Connector		Signal Functional Description
2	/MQX/		Request for Memory Access, Port X
1	/AHX/		Address Here, Port X
4	/ARX/		Address Release, Port X
3	/DRX/		Data Release, Port X
5	/PEX/		Parity Error Signal, Port X
6	/SRAX/	*	Second Request Allowed
7	Not Assigned		
8	/ABOA/	*	Abort Memory Lockout Signal
9	/POKX/		Parity OK Signal, Port X
10	/MR/	(1)	Memory Reset
11	/ORX/	*	Override Port
12	/ORIL/	* (1)	Override Interleave
13	/HOF/	* (1)	Halt on Fault
14	/MFR/	* (1)	Memory Fault Reset

* Not used by IOP

(1) Port C only

2.4 CPU INTERFACE

2.4.1 Signal Convention

Signals shall be exchanged via the AT13 Cable Driver/Receiver module, SDS Part No. 125260. Unless otherwise stated, the signals shall use a convention of +2 volts as true logic.

2.4.2 Signal Lines Interconnecting IOP and CPU

IOP's shall be connected in a tail-trunk fashion to a CPU as shown in Figure 2.1. The IOP's shall be arranged in a priority sequence such that during the execution of an AIO instruction the IOP nearest to the CPU with an Interrupt Request pending shall respond to the CPU request for service.

The lines tabulated below shall interconnect the IOP and CPU.

Description	Designation	Number of Lines	Direction of Signal Flow	
			IOP to CPU	CPU to IOP
Function Code	/FNC0/ thru /FNC2/	3		x
IOP Address	/IOPA0/ thru /IOPA2/	3		x
Not Condition Code 1	/NCOND1/	1	x	
Not Condition Code 2	/NCOND2/	1	x	
Clock 1- MHz, Source	/CL1S/	1		x
Reset I/O	/RIO/	1		x
Interrupt Request	/IR/	1	x	
Proceed	/PR/	1	x	
Control Strobe	/CNST/	1		x

2.4.3 Interface Signal Definition and Timing

The utilization of the lines interconnecting the IOP and CPU shall be as follows: (Timing of signals is as measured at the IOP/Cable Interface).

2.4.3.1 Function Code Lines: The CPU shall place on these lines signals representing the I/O instruction being executed. During a CPU request for service, signals on these lines shall be interpreted as follows by the IOP:

	SIO	TIO	TDV	HIO	AIO
/FNC0/	0	0	0	0	1
/FNC1/	0	0	1	1	1
/FNC2/	0	1	0	1	0

The signals on these lines shall be settled 250 nanoseconds before the Control Strobe (CNST) is driven true and shall remain settled for 250 nanoseconds after the Control Strobe is released. These times as measured at the IOP/Cable interface.

2.4.3.2 IOP Address Lines: The CPU shall place on these lines coded signals representing the address of the IOP from which service is requested during the execution of SIO, TIO, TDV, or HIO instructions. When the Function Code lines are coded representing SIO, TIO, TDV, or HIO operations, the IOP shall compare the state of the IOP Address lines with the state of switch contacts within the IOP that designates the IOP address. If the two sets of signals compare (IOP address recognition) then the IOP shall respond to the Control Strobe signal.
When the Function Code lines are coded representing the AIO operation then the IOP Address lines shall have no meaning. The signals on these lines shall be settled 250 nanoseconds before the Control Strobe is driven true and shall remain settled for 250 nanoseconds after the Control Strobe is released. These times are measured at the IOP/Cable interface.

2.4.3.3 Control Strobe: The CPU shall drive this line during the execution of an I/O instruction to request service from an IOP. The IOP shall respond to the Control Strobe as follows:

If the Function Code lines designate an SIO, HIO, TIO, or TDV operation and IOP address recognition exists or if the Function Code lines designate an AIO operation and the Interrupt Request line is true then the IOP shall respond to the Control Strobe and shall not pass the Control Strobe along to the next lower priority IOP. Response of the IOP to specific function codes will be described in later sections. If an SIO, HIO, TIO, or TDV operation is designated and no IOP address recognition exists or if an AIO operation is designated and the Interrupt Request line is false then the IOP shall not respond to the Control Strobe but shall pass the Control Strobe along to the next lowest priority IOP. If, however, the IOP is designated as the last IOP on the tail-trunk cable by the state of a switch contact in the IOP, then the IOP shall cause the Proceed signal to be driven true and shall drive no other lines.

2.4.3.4 Not Condition Code Lines: If, during execution of an SIO, TIO, TDV, or HIO operation the IOP detects a memory parity error while accessing cell 20* then the IOP shall not communicate with any Device Controller and shall hold NCOND1 and NCOND2 false. During execution of an SIO, TIO, TDV, or HIO operation if no memory parity error is detected while reading cell 20* the IOP shall drive the NCOND1 and NCOND2 lines with the same state that the Device Controller dictated on the DOR and IOR lines respectively.

During the execution of an AIO operation the IOP shall drive the NCOND1 and NCOND2 lines as dictated by the Device Controller; however, if the responding Device Controller has the address stored by the IOP and an Unusual End interrupt is pending then the S/IOP shall hold the NCOND2 line false. The signals on these lines shall be settled before the Proceed signal is driven true and shall remain settled until the release of the Control Strobe.

* Base 16

2.4.3.5 Proceed Line: In response to a CPU request for service on the Control Strobe line the IOP shall drive the Proceed line to indicate termination of the service. The Proceed line shall operate in a closed-loop manner with respect to the Control Strobe line; i.e., the IOP shall raise the Proceed line in response to the CPU raising the Control Strobe line and shall drop the Proceed line in response to the CPU dropping the Control Strobe line.

No Address Recognition:
During the response to an SIO, TIO, TDV, or HIO operation with no address recognition or to an AIO operation with the Interrupt Request line false the MIOP shall not respond to the Control Strobe but shall pass the Control Strobe along to the next lower priority IOP. However, if the MIOP is designated as the last IOP on the tail-trunk cable interconnecting IOP's with the CPU then the MIOP shall respond to the Control Strobe by holding NCOND1 and NCOND2 false and driving the Proceed line true immediately.
Address Recognition: If during execution of an SIO, TIO, TDV, or HIO operation the IOP detects a memory parity error while accessing cell 20* then the IOP shall hold the NCOND1 and NCOND2 lines false and shall drive the Proceed line true immediately.
If during execution of an SIO, TIO, TDV, or HIO operation the IOP does not write in memory cells 20* or 21* then the IOP shall respond to the Control Strobe after receiving the Device Controller condition code response on the DOR and IOR lines.
If the IOP writes in memory cells 20* or 21* then the IOP shall raise the Proceed line after receiving an Address Release signal from core memory in response to the last Memory Request.

2.4.3.6 Interrupt Request Line: The IOP shall drive this line true when making a standard I/O interrupt request. All interrupt requests from Device Controllers attached to an IOP are funnelled to this line via the Interrupt Call line at the Device Controller Interface. This line shall go false during the execution of all I/O instructions. If an interrupt is then still pending this line shall again be driven true.

* Base 16

2.4.3.7 Reset I/O Line: The CPU shall drive this line true when the I/O system is to be initialized. The IOP, in response to this signal, shall be initialized in readiness for a service request from the CPU and shall also pass the signal along at the Device Controller interface on the I/O Reset line.

2.4.3.8 Clock, Source Line: The CPU shall drive this line with a periodic timing signal for use by Device Controllers. The IOP shall pass this signal along to the Device Controller at the Device Controller interface on the Clock line.

2.4.4 Cables

As specified in 2.1, IOP's shall be connected to a CPU by cables in a trunk-tail fashion. The total length of cables interconnecting IOP's with a CPU shall not exceed 64 feet. The pin assignment for signals in that cable at the Cable Driver/Receiver and Cable Connector interface shall be as specified below:

Cable 1 — AT13 Cable Driver/Receiver Module

Connector Pin	Signal Desig. at Connector	Signal Functional Description
1	/FNC0/	Function Code
2	/FNC1/	Function Code
3	/FNC2/	Function Code
4	/IOPA0/	IOP Address
5	/IOPA1/	IOP Address
6.	/IOPA2/	IOP Address
7	/CNST/	Control Strobe
8	Not Assigned	
9	/NCOND1/	Not Condition Code 1
10	/NCOND2/	Not Condition Code 2
11	/CL1S/	Timing Signal (1 MHz)
12	/RIO/	I/O Reset
13	/IR/	Interrupt Request
14	/PR/	Proceed

2.5 DEVICE CONTROLLER INTERFACE

2.5.1 Cable Connections - Four cables shall interconnect the IOP and Device Controllers (six cables if Model 8275/8475 four-byte interface option is installed). All Device Controllers shall interconnect in a trunk-tail fashion to the IOP.

2.5.2 Signal Convention - Signal exchange shall be via AT10 Cable Receiver Modules, AT11 Cable Driver/Receiver Modules, and AT12 Cable Driver Modules. Unless otherwise stated, signals shall use a convention of +2 volts for true logic.

2.5.3 Signal-Lines Interconnecting IOP and Device Controllers

The lines tabulated below shall interconnect the IOP and Device Controllers.

Description	Designation	No. of Lines	Direction of Signal Flow	
			IOP to Device Controller	Revice Con-troller to IOP
Data Input/Output (1st byte)	/DA0/ thru/DA7/	8	x	x
Data Input/Output (2nd byte) *	/DB0/ thru /DB7/	8	x	x
Data Input/Output (3rd and 4th bytes) *	/DC0/ thru /DC7/, /DD0/thru DD7/	16	x	x
Data Parity	/DAP/	1	x	x
2 Byte Interface Request	/DX2/	1		x
4 Byte Interface Request	/DX4/	1		x
End Data	/ED/	1	x	x
Parity Check	/PC/	1		x
Data/Order Request	/DOR/	1		x
Input/Output Request	/IOR/	1		x
Function Response	/FR0/ thru /FR7/	8		x
Request Strobe	/RS/	1		x
Function Acknowledge Strobe	/FSL/	1		x
Device Controller Available Output	/AVO/	1		x
Interrupt Call	/IC/	1		x
Service Call	/SC/	1		x
I/O Reset	/RST/	1	x	
Clock, 1MHz	/CL1/	1	x	
End Service	/ES/	1	x	
Request Strobe Acknowledge	/RSA/	1	x	
Start I/O Function Indicator	/SIO/	1	x	
Halt I/O Function Indicator	/HIO/	1	x	
Test I/O Function Indicator	/TIO/	1	x	
Test Device Function Indicator	/TDV/	1	x	
Acknowledge Interrupt Function Indicator	/AIO/	1	x	
Acknowledge Service Call Indicator	/ASC/	1	x	
Function Strobe	/FS/	1	x	
Zero Byte Count Interrupt	/ZBCI/	1	x	
Fast Device Controller	/FAST/	1		x
AVI from IOP	/AVIH1/, AVIH2	2	x	

Description	Designation	No. of Lines	Direction of Signal Flow	
			IOP to Device Controller	Device Con-Troller to IOP
Reset I/O from JX58	/TEST RIO/	1		x
Enable Two-byte Interface *	/EDX2/	1	x	
Enable Four-byte Interface *	/EDX4/	1	x	
Word Aligned Data Required	/WADR/	1	x	
Inhibit Extended Interface Request	/IER/	1	x	

* These signal lines are available only if Model 8275/8475 four-byte interface option is installed.

2.5.4 Definition of Device Controller Interface Lines. All times as measured at IOP/Cable interface.

2.5.4.1 Service Call (SC) Line:

The SC line shall be driven by the Device Controller to request service from the IOP. The IOP shall respond to the request by initiating one of several possible operation sequence, identified as one of the following: Order Out, Order In, Data Out, Data In, or an aborted service request. The Device Controller shall drive the SC line at least until the IOP has driven the ASC function indicator line; otherwise, the IOP shall abort the service request and wait for the next service request from either the CPU or the Device Controller.

CPU service requests shall have priority over Device Controller service requests.

2.5.4.2 Function Indicator Lines (SIO, HIO, TIO, TDV, AIO, ASC):

During the execution of a CPU request to perform an SIO, HIO, TIO, TDV, or AIO operation the IOP shall drive the appropriate Function Indicator line. Similarly, during the response to a Device Controller request for service via the SC line the IOP shall drive the ASC line. The driven line shall be stable for at least 185 nanoseconds before the Function Strobe line is driven and shall not be dropped less than 185 nanoseconds after the Function Strobe line is dropped.

2.5.4.3 Function Strobe (FS), Function Strobe Acknowledge (FSL), and Available Out (AVO) lines:

The Function Strobe line shall operate in a closed-loop fashion with either the FSL or AVO lines; that is, after the IOP has driven the FS line true the Device Controller shall drive either the FSL line or the AVO line and shall drop the FSL or AVO line in response to the IOP dropping the FS line. During the execution of an SIO, HIO, TIO, or TDV operation (if no memory parity error is detected while reading cell 20*) the IOP shall place the Device Controller address on the DA0-7 lines, drive the appropriate Function indicator line, delay, and drive the FS line. If the Device Controller address was not recognized or the addressed Device Controller was off-line then the IOP shall receive AVO in response to the FS signal. Otherwise, the addressed Device Controller shall respond by placing condition code information on the DOR and IOR lines, Device Controller status on the Function Response lines, and driving the FSL line.

During the execution of an AIO operation the IOP shall drive the AIO line, delay, and drive the FS line. If there was no Device Controller interrupt pending then the IOP shall receive AVO in response to the FS signal. Otherwise, the responding Device Controller shall place its address on the Function Response lines, condition code data on the DOR and IOR lines, Device Controller status on the DAO-7 lines, and raise the FSL line.

During the response of the IOP to a Device Controller request for service on the SC line the IOP shall raise the ASC line, delay, and raise the FS line. If the SC line has dropped prior to the time that the IOP raised the ASC line then the IOP shall receive a response on the AVO line. Otherwise, the highest priority service requesting Device Controller shall raise the FSL line. Refer to the One-Byte or Four-Byte Data Path Specification for the description of the Device Controller actions when connecting for service to the IOP.

2.5.4.4 Data/Order Request (DOR) and Input/Output Request (IOR) Lines:

The DOR and IOR lines shall be driven by the Device Controller. The IOP shall interpret the state of these lines as follows:

a) During the execution of a CPU request for service, if the IOP has raised the FS line, then the Device Controller shall place condition code data on these lines. The IOP shall wait for the FSL line to be driven, delay 185 nanoseconds, minimum, and then strobe these lines and store the state for later transmission to the CPU on the NCOND1 and NCOND2 lines. The Device Controller shall not drop these lines until the IOP has dropped the FS line.

b) During a Device Controller service request, if not aborted, the Device Controller shall connect for service at the time that the IOP drops the FS line. The Device Controller shall then drive the DOR and IOR lines with coded signals, drive the Data Lines if IOR is false, and raise the initial Request Strobe (RS). The IOP shall delay 185 nanoseconds minimum after receiving the initial RS of the service sequence and then strobe the DOR and IOR lines.

The IOP shall interpret the state of these lines as follows:

DOR	IOR	
1	1	Order Out
1	0	Order In
0	1	Data Out
0	0	Data In

The IOP shall then perform the sequence of operations dictated by the above coding. These operations will be defined in greater detail in later paragraphs.
The Device Controller shall not change the state of the DOR and IOR lines before the IOP has initially driven the Request Strobe Acknowledge (RSA) lines.

2.5.4.5 Function Response Lines (FR0-7):

The FR0-7 lines shall be driven only by the Device Controller. During the execution of an SIO, HIO, TIO, or TDV operation the Device Controller shall supply Device Controller status on these lines. During an AIO service cycle or during a DC requested service cycle the Device Controller address shall be transmitted on these lines.

The IOP shall delay 185 nanoseconds minimum after the FSL line has been driven true and then strobe the Function Response lines for later transmission of the DC status to Core Memory or for storing the DC address. The Device Controller shall not change the state of the lines until the IOP has dropped the FS line.

2.5.4.6 Request Strobe (RS) and Request Strobe Acknowledge (RSA) lines:
The RS line shall be driven by the Device Controller and the RSA line shall be driven by the IOP. These lines shall operate in a closed-loop fashion; that is, upon sensing that the RS line has been driven true by the Device Controller the IOP shall delay and then drive the RSA line true. Upon sensing that the RS line has dropped the IOP shall immediately drop the RSA line.

The Device Controller, after connecting for service, shall send a succession of RS signals to the IOP until the IOP signals RS A and End Service.

The IOP, after receiving the initial RS of a service sequence, shall delay 185 nanoseconds minimum and then strobe the DOR and IOR lines to determine the type of service requested by the Device Controller. If the service is an output operation the IOP shall immediately access core memory for the data or order, place the data or order on the Data Lines, delay 185 nanoseconds minimum and raise the RSA line. If the service is an input operation then the IOP shall delay 185 nanoseconds minimum and then strobe the Data Lines. This sequence shall continue until either the IOP or the Device Controller signals End Data. The IOP shall then wait for the final RS for the Terminal Order (if End Service was not raised with End Data), place the Terminal Order on the Data Lines, set End Service, delay 185 nanoseconds minimum, and then raise RSA to terminate the service sequence.

2.5.4.7 Data Lines (DA0-7, DAP, DB0-7, DC0-7, DD0-7):

The Data Lines shall be driven by either the IOP or the Device Controller.

The DA0-7 lines are multi-purpose lines and shall be used as follows:

a) During the execution of an SIO, HIO, TIO, or TDV operation the IOP shall place the Device Controller address on the DA0-7 lines, delay 185 nanoseconds minimum, and then drive the FS line. The IOP shall not change the state of the DA0-7 lines until either FSL or AVO have been received.

b) During the execution of an AIO operation the Device Controller shall place the Device Controller status on the DA0-7 lines. The IOP shall delay 185 nanoseconds minimum after receiving the FSL signal and then strobe the lines. The Device Controller shall not change the state of the lines until FS has dropped.

c) During an Order Out service, in response to the initial RS, the IOP shall place the Order on the DA0-7 lines, delay 185 nanoseconds minimum and raise the RSA line. The IOP shall not change the state of the Data Lines until the RS is received for the Terminal Order.

d) During an Order in service, associated with the initial RS, the Device Controller shall place the Operational Status Byte on the DA0-7 lines. The IOP shall delay 185 nanoseconds minimum after receiving RS, then strobe the DA0-7 lines. The IOP shall interpret the Data lines as follows:

DA0	Transmission Error
DA1	Incorrect Length
DA2	Chaining Modifier
DA3	Channel End
DA4	Unusual End

The response of the IOP to the Operational Status Byte will be defined in later paragraphs. The Device Controller shall not change the state of the DA0-7 lines until RSA has been raised.

e) During Data Out service, in response to the RS signal, the IOP shall place the data on the DA0-7, delay 185 nanoseconds minimum and raise RSA. The IOP shall not change the state of the Data Lines until 300 nanoseconds minimum after the RS signal has dropped.

f) During Data In service, the Device Controller shall place the data on the DA0-7 lines and raise the RS line. The IOP shall delay 185 nanoseconds minimum and strobe the lines. The Device Controller shall not change the state of the Data lines until RSA has been received.

g) During any service sequence, in which a Terminal Order is required, the IOP shall raise End Service, place the Terminal Order on the DA0-7 lines, delay 185 nanoseconds minimum and raise RSA.

The definition of the DA0-7 lines during the Terminal Order exchange shall be as follows:

DA0	Interrupt
DA1	Count Done
DA2	Command Chain
DA3	IOP Halt

The condition under which these lines are raised will be discussed in later paragraphs. The IOP shall not change the state of the Data lines until 300 nanoseconds minimum after the RS signal has dropped.

The DAP line shall be used to provide an odd parity bit for the data byte on lines DA0-7 during Data Out or Data in service. The IOP shall provide an odd parity bit for the data byte on the DA0-7 lines during all output operations. If the PC line is true and the four-byte option is absent and the DX4 line is false then the IOP shall check for odd parity if Data In service. If a parity error is detected during a Data In service, the IOP shall set the Transmission Data Error status bit. The timing for the DAP line shall be the same as the timing for the DA0-7 lines during Data Out/In service. The DB0-7, DC0-7 and DD0-7 Data lines shall be used only for the exchange of data during Data Out/In service if the four-byte interface option is installed. The timing for these lines shall be the same as the timing for the DA0-7 lines during Data Out/In service.

If the DX4 line is false during Data Out/In service sequences then the IOP shall exchange data with the Device Controller on the DA0-7 lines only. If the four-byte interface option is installed and the DX4 line is true during Data Out/In service sequences then the IOP shall exchange data with the Device Controller on the DA0-7, DB0-7, DC0-7, and DD0-7 lines where DA0-7 shall be the most significant byte and DD0-7 shall be the least significant byte.

2.5.4.8 End Data (ED) and End Service (ES) Lines:

The ED and ES lines shall designate action to be taken by the IOP and Device Controller during order and data exchanges.

The ED line may be driven true by either the IOP or the Device Controller. The ED line shall always be driven true by the Device Controller with the Initial RS of an Order Out/In sequence. If, during a Data Out/In exchange, either the IOP or the Device Controller drive the ED line; then, this shall signify that no more data be exchanged. The ED line shall be driven true by the IOP under the following conditions:

a) Whenever the ED line has been driven by the Device Controller

b) During Data Out/In sequences if the IOP detects that a core memory word boundary will be crossed if another data exchange is made.

c) During Data Out/In sequences the IOP detected an IOP Halt condition.

d) During Data Out/In sequences the IOP detected a Zero Byte Count.

When the IOP has driven the End Data line the IOP shall delay at least 185 nanoseconds before raising the RSA line. The ES line shall be driven by the IOP only. The ES line shall signify, when true, that the Device Controller service shall terminate; that is, the Device Controller shall not raise RS again during the current service sequence. If, at the time the ED and RSA lines are raised, the ES line is false: then the DC shall request a Terminal Order. The timing of the ES line respect to the RSA line shall be the same as the timing of the DA0-7 lines during Data Out service.

2.5.4.9 Parity Check (PC) Line:

The PC line shall be driven by Device Controllers in which its use has been specified. The IOP; however, shall only respond to the PC line if the DX4 line is false. If the PC line is true under this condition then the IOP shall perform an odd parity check on the DA0-7 and DAP lines. The PC line, if driven, shall be raised with the initial RS of a Data In sequence and shall not be dropped until RSA and ES have been signalled by the IOP.

2.5.4.10 Interrupt Call (IC) Line:

The IC line shall be driven by the Device Controller to make an I/O Interrupt request to the CPU via the IOP. The IOP shall set an Interrupt Request bit whenever the IC line is true and the CPU is not requesting an AIO service from the IOP. The IOP shall clear the Interrupt Request bit whenever the Reset I/O (RIO) line is driven or during the execution of an AIO request from the CPU. The IOP shall drive the Interrupt Request (IR) line at the CPU interface from the output of the Interrupt Request bit.

2.5.4.11 Zero Byte Count Interrupt (ZBCI) and Fast Device Controller (FAST) Lines:

The MIOP shall not respond to the FAST line.

The MIOP shall not drive the ZBCI line.

2.5.4.12 Enable Two-Byte Data Path (EDX2).

Enable Four-Byte Data Path (EDX4), Two-Byte Interface Request (DX2), and Four-Byte Interface Request (DX4):

If the Model 8275/8475 Four-Byte Interface option is installed in the IOP then the IOP shall hold the EDX2 line false and shall always drive the EDX4 line true. If the option is not installed then the state of these lines shall have no meaning (note that if the option is not present and a DC is mechanized to operate on either the two-byte or four-byte interface then these lines may be true in the DC).

The DX2 and DX4 lines are driven by the DC. The IOP shall always ignore the state of the DX2 line. If the Four-Byte Interface option is installed then the IOP shall respond to the DX4 line as follows: During Data Out/In exchanges the IOP shall exchange data with the DC over the one-byte path if DX4 is false and shall exchange data with the DC over the four-byte path if DX4 is true. The DX4 line, if driven by the DC, shall be raised with the initial RS of a Data Out/In sequence and shall not be dropped until RSA and ES have been driven by the IOP.

2.5.4.13 I/O Reset (RST), Reset I/O from JX58, (TESTRIO), One MHz clock (CLI), and AVI from IOP (AVIH) lines.

The I/O Reset (RST) line shall be driven by the IOP and shall have the same state as the RIO line driven by the CPU or the TESTRIO line driven at the DC interface by the JX58 when connected. The TESTRIO line shall be driven at the DC interface by the JX58 tester when connected to the IOP. This line shall be used for initializing the IOP and DC's when using the JX58 for diagnostic testing of the IOP. The TESTRIO line shall cause the same IOP response as does the RIO line driven by the CPU.

The CLI line shall be driven by the IOP and shall have the same state as the CLIS line driven by the CPU. The AVIH lines shall be driven by the IOP when then IOP logic power supply is on to provide the AVI signal to the highest priority DC connected to the IOP.

2.5.4.14 Word Aligned Data Required (WADR) line:

This line shall be held false by the IOP.

2.5.4.15 Inhibit Extended Interface Request (IER):

This line shall be driven by the IOP. Device Controllers that do not use the four-byte interface may ignore the state of this line. Device controllers that use the four-byte interface shall examine the state of this line during Order Out, Data Out, or Data In service when RSA and ES are true. If the IER line is true under the conditions described above, then the device controller shall not raise the DX4 line during the next service cycle (DX4 may or may not be raised if IER is false). During Order Out service or Data Out/In service with chaining the IOP shall raise the IER line if the byte count after chaining is less than eight or the two least significant byte address bits are non-zero. The IOP shall always issue a terminal order to terminate an Order Out or data service with chaining to enable sampling of the IER line when ES and RSA are true after receiving the new command pair. During Data Out/In service without chaining the IOP shall raise the IER line if before final updating the byte count is less than eight or the DX4 line is false and the two least significant byte address bits are not both true. During the update of the byte count during Data Out/In service the IOP shall not change the state of two least significant byte count bits if DX4 is true.

2.5.5 Cable and Connector Pin Assignments

Four cables shall interconnect the IOP and DC's (six cables if Model 8275/8475 four-byte interface option installed). The maximum length of cable interconnecting the IOP and the furthest DC shall not exceed 100 feet (priority cable may be 200 feet). The pin assignment of signals in those cables at the Cable Driver/Receiver and Cable Connector Interface shall be as specified below:

Cable 1

AT10 Cable Driver/Receiver Module

Connector Pin	Signal Desig. at Connector	Signal Functional Description
01	FR7	Function Response (2^0)
02	FR6	Function Response (2^1)
03	FR5	Function Response (2^2)
04	FR4	Function Response (2^3)
05	FR3	Function Response (2^4)
06	FR2	Function Response (2^5)
07	FR1	Function Response (2^6)
08	FR0	Function Response (2^7)
09	RS	Request Strobe
10	IOR	Input/Output Request
11	FSL	Function Acknowledge Strobe
12	DX2	Two Byte Interface Signal
13	IC	Interrupt Call
14	DX4	Four Byte Interface Signal

Connector Pin	Signal Designat Connector	Signal Function Description
01	DA7	Data Input/Output, Byte 1 (2^0)
02	DA6	Data Input/Output, Byte 1 (2^1)
03	DA5	Data Input/Output, Byte 1 (2^2)
04	DA4	Data Input/Output, Byte 1 (2^3)
05	DA3	Data Input/Output, Byte 1 (2^4)
06	DA2	Data Input/Output, Byte 1 (2^5)
07	DA1	Data Input/Output, Byte 1 (2^6)
08	DA0	Data Input/Output, Byte 1 (2^7)
09	DAP	Data Parity Input/Output, Byte 1
10	ED	End Data
11	PC	Parity Check
12	DOR	Data/Order Request
13	SC	Service Call
14	Not Assigned	

Cable 3

AT12 Cable Driver Module

Connector Pin	Signal Desig. at Connector	Signal Functional Description
01	RST	I/O Reset
02	CL1	Clock, 1 megahertz
03	ES	End Service
04	RSA	Request Strobe Acknowledge
05	SIO	Start I/O Function Indicator
06	HIO	Halt I/O Function Indicator
07	TIO	Test I/O Function Indicator
08	TDV	Test Device Function Indicator
09	AIO	Acknowledge Interrupt Function
10	ASC	Acknowledge Service Call Indicator
11	FS	Function Strobe
12	SIC	Set Interrupt Call
13	WADR	Word Aligned Data Required
14	IER	Inhibit Extended Interface Request

Cable 4

AT11 Cable Driver/Receiver Module

Connector Pin	Signal Desig. at Connector	Signal Functional Description
01	HPI *	High Priority Interrupt
02	HPS *	High Priority Service
03	FAST	Fast Device Controller
04	AVO	Available Output
05	Not Assigned #	
06	Not Assigned #	
07	AVIH1	AVI from IOP
08	AVIH2	AVI from IOP
09	Not Assigned #	
10	Not Assigned #	
11	Not Assigned #	
12	TEST RIO #	I/O Reset from JX58
13	LSOR #	Reset LS0 Flip-Flop in IOP
14	LS1S #	Set LS1 Flip-Flop in IOP

* Not used by IOP.

\# Device Controllers may not use these lines.

Connector Pin	Signal Desig. at Connector	Signal Function Description
01	DB0	Data Input/Output, Byte 2 (2^7)
02	DB1	Data Input/Output, Byte 2 (2^6)
03	DB2	Data Input/Output, Byte 2 (2^5)
04	DB3	Data Input/Output, Byte 2 (2^4)
05	DB4	Data Input/Output, Byte 2 (2^3)
06	DB5	Data Input/Output, Byte 2 (2^2)
07	DB6	Data Input/Output, Byte 2 (2^1)
08	DB7	Data Input/Output, Byte 2 (2^0)
09	EDX2	Enable Two-Byte Interface
10	DC0	Data Input/Output, Byte 3 (2^7)
11	DC1	Data Input/Output, Byte 3 (2^6)
12	DC2	Data Input/Output, Byte 3 (2^5)
13	DC3	Data Input/Output, Byte 3 (2^4)
14	EDX4	Enable Four-Byte Interface

Note: This cable installed only if Model 8275/8475 Four-byte interface option installed.

Cable 6

AT11 Cable Driver/Receiver Module

Connector Pin	Signal Desig. at Connector	Signal Functional Description
01	DC4	Data Input/Output, Byte 3 (2^3)
02	DC5	Data Input/Output, Byte 3 (2^2)
03	DC6	Data Input/Output, Byte 3 (2^1)
04	DC7	Data Input/Output, Byte 3 (2^0)
05	Not Assigned	
06	DD0	Data Input/Output, Byte 4 (2^7)
07	DD1	Data Input/Output, Byte 4 (2^6)
08	DD2	Data Input/Output, Byte 4 (2^5)
09	DD3	Data Input/Output, Byte 4 (2^4)
10	DD4	Data Input/Output, Byte 4 (2^3)
11	DD5	Data Input/Output, Byte 4 (2^2)
12	DD6	Data Input/Output, Byte 4 (2^1)
13	DD7	Data Input/Output, Byte 4 (2^0)
14	Not Assigned	

Note: This cable installed only if Model 8275/8475 Four-byte interface option installed.

2.6 Display Interface

2.6.1 Cable Connection - One 100Ω ribbon cable of total 52 conductors shall interconnect the IOP and the MS at the Display Interface. If this cable is not installed, the IOP shall perform its normal operation.

2.6.2 Signal Convention - Signals exchanged via this interface without cable drivers and receivers. The signals will use a convention of +4 volts as true logic.

2.6.3 Display Interface Lines (see Page 47).

2.6.3.1 IOP Display Lines (DIS:00 - DIS:15). These lines shall be driven by the IOP to the MS. There are a total of seven Display Groups, each Display Group containing sixteen IOP signals. During the execution of a READ DIRECT or a WRITE DIRECT instruction, one of the seven groups shall be selected and placed on these lines although signals can pass through to the DIO bus only when a READ DIRECT instruction is issued.

2.6.3.2 Control Input Lines (DIO:DB16:R - DIO:DB31:R). The Control Input Lines shall be driven by the CPU through the MS during the execution of a WRITE DIRECT. Only three of these lines (DIO:DB29:R - DIO:DB31:R) are used by the MIOP to perform the three control functions of (1) reset I/O, (2) stop the normal phase sequence during a CPU or a SC service, and (3) single phase the IOP.

2.6.3.3 Group Address Lines (DIO:A9:R-DIO:A15:R)

These lines are driven by the CPU via MS. A13 thru A15 determine which one of the seven groups of IOP signals shall be selected and placed on DIS:00 through DIS:15 on a READ DIRECT instruction.

2.6.3.4 RD/WD Indicator Line (DIO:RWD:R)

The RD/WD Indicator Line shall be driven by the CPU through the MS. During the execution of a WRITE DIRECT instruction, this line is driven high. During the execution of a READ DIRECT instruction, this line is low.

2.6.3.5 IOP Strobe Line (DIS:STROBE:D)

The IOP Strobe Line shall be driven by the MS to the IOP, initiating MIOP action based on the Control Input Lines, the Group Address Lines, and the RD/WD Indicator Line.

2.6.3.6 MS Wired Ground (NDIS:ABLE)

This line is wired to ground inside MS to indicate the existance of a MS at this interface. When MS is absent at this interface, this line is open, i.e., NDIS is true, and DIS is false, which will make the IOP ignore all other inputs at this interface.

2.6.3.7 Single Phasing Indicator (NDISPHSTOP)

This line shall be driven by MIOP to MS. This line is false when the MIOP is operating in the single phase mode and is used in the MS to permit single service call operation.

DESCRIPTION	DESIGNATION	NO. OF LINES	SIGNAL DIRECTION IOP TO MS	SIGNAL DIRECTION MS TO IOP
IOP Display Lines	DIS:00 thru DIS:15	16	X	
Control Inputs	DIO:DB16:R thru DIO:DB-31:R	16		X
Group Address Lines	DIO:A9:R thru DIO:A15:R	7		X
RD/WD Indicator Line	DIO:RWD:R	1		X
IOP Strobe Line	DIS:STROBE	1		X
MS Wired Ground	NDIS:ABLE	1		X
Single Phasing Indicator	NDIS:PHSTOP	1	X	

2.7 IOP INTERNAL OPERATION

The IOP is a passive link between core memory and the Device Controllers connected to the IOP.

Once an I/O operation has been initiated by the CPU, the operation is performed to completion, independently, by the IOP, Device Controller, and Core Memory. The IOP will perform core memory accesses, as required by the Device Controller, and update current command information. The IOP will also record IOP status for future interrogation by the CPU. During a record, a new command may be loaded by the IOP - making scatter reads and gather writes possible (data chaining). At the end of a record, a new command may be loaded by the IOP and an order sent to the Device Controller - allowing multiple record operations to occur without CPU reinitiation (command chaining). The maximum number of Device controllers that may be attached to an IOP is 24. The basic IOP has eight sub-channel positions and can service up to eight DC's simultaneously. This number of sub-channel positions is expandable (optionally) in groups of eight, to allow 24 DC's to be serviced simultaneously. However, only the basic eight sub-channel positions may be used to service DC's with multiple devices. Limitations on data chaining and number of device controllers that may be connected are functions of device speed, interface width, and cable lengths.

The IOP shall perform the operations described in this section in response to service calls from the CPU or from Device Controllers. Specific interface responses are described in Sections 2.3, 2.4 and 2.5.

2.7.1 CPU Service Calls

The IOP shall respond to service calls from the CPU and perform the following operations: SIO, HIO, TIO, TDV, and AIO. Each IOP shall have the facility for assignment of the IOP address by the setting of switches on a switch module type LT26 (SDS Part No. 126982), located within the IOP.

SIO

The IOP shall decode and recognize the SIO function and shall decode the IOP address lines. If no address recognition, the IOP's shall pass the Control Strobe along to the last IOP and there the Control Strobe shall be returned to the CPU on the Proceed line. If the IOP address is recognized, the IOP shall drive the SIO function indicator to the Device Controller and also shall access cell 20* for the Device address and the next command address. If a memory parity error is detected at this point, the IOP shall terminate the operation and send the Proceed signal with appropriate condition codes. If there is no memory parity error, the IOP transmits Device address at the Device Controller interface and waits for a response. If the Device signals that the address is recognized, then the next command address is loaded into the IOP sub-channel position for the addressed Device. The IOP then completes the SIO operation by loading cells 20* and 21* (dependent on the R field coding) and sending the appropriate condition codes and Proceed signal to the CPU.

HIO,TIO, TDV

These operations are performed in a manner similar to the SIO operation. However, the IOP does not load the next command address in the sub-channel position since the current command address is already loaded there.

*Base 16

AIO

The IOP shall decode and recognize the function. If no interrupt is pending, the IOP's shall pass the Control Strobe along to the last IOP which shall return the strobe to the CPU on the Proceed line with the appropriate condition code settings. The IOP with the highest priority among the IOP's which have an interrupt pending shall pass the AIO function along to the Device Controllers connected to that IOP. The IOP shall then wait for the highest priority Device Controller with interrupt pending to respond with Device/Device Controller address and status. The IOP shall then complete the AIO operation by writing the IOP/Device Controller/Device address and status in cell 20* and sending condition codes and Proceed signal to the CPU.

*Base 16

2.7.2 Device Controller Service Calls

The IOP shall respond to DC service calls as described in detail in Section 2.8 and perform the following operations: Order Out, Order In, Data Out, and Data In.

Data Exchange

The IOP shall perform exchanges of data between the DC and core memory in response to Data Out/In requests from the DC. The basic IOP has a one-byte data path at the DC interface. Therefore, the IOP shall assemble data during Data In operations and disassemble data during Data Out operations. However, if the optional four-byte data path is installed and the DC uses the four-byte path then the IOP shall not assemble or disassemble the data but shall transmit the data in full-word increments. In no case shall the IOP access core memory more than one time for the purpose of exchanging data during a Data Out/In operation. The IOP makes a number of data exchanges with the DC ranging from one to four (dependent on data path width and state of ED line). Data exchanges continue until either the DC or the IOP signal ED. The IOP shall drive the ED line for one of the following reasons:

Core memory word boundary reached

Zero byte count conditions

IOP halt condition.

Data Out

During Data Out operations the IOP shall access the memory location determined by the current byte address. The IOP then exchanges data with the DC until ED is raised. The IOP updates the sub-channel position including the byte address and byte count registers and performs data chaining if required, before terminating the service sequence.

Data In

During Data In operations the IOP accepts data from the DC until ED is raised and then accesses the core memory location determined by the current byte address for a full-word or partial- word write operation. If the four-byte data path option is installed and the DC exchanges data over the four-byte path then the IOP shall perform only a full-word write operation. As for Data Out operations, the IOP updates the sub-channel position, including the byte address and byte count registers, and performs data chaining, if required, before terminating the service sequence.

Parity Generation and Checking

The IOP shall generate odd parity during all output operations over the basic one-byte data path. The IOP shall perform a parity check on data transmitted over the basic one-byte data path during Data In operations only when the PC (Parity Check) line is true.

Order Out

During Order Out operations the IOP shall access the core memory doubleword designated by the command address register, send the order to the Device Controller, store the flags, byte address, and byte count and terminate the operation.

Order In

During Order In operations the IOP shall accept the Operational Status Byte from the Device Controller. The Device Controller may report any of the following conditions in the Operational Status Byte: Transmission Error, Incorrect Length, Chaining Modifier, Channel End, or Unusual End. The IOP shall take action appropriate to the conditions reported by the Device Controller and terminate the operation.

Terminal Orders

A Terminal Order is requested by the Device Controller dependent on the condition of the End Data and End Service lines. The IOP shall always initiate a Terminal Order request to conclude an Order In/Out operation by holding the End Service line false during the initial byte exchange. However, the IOP shall expect the Terminal Order request following a Data In/Out operation only if the IOP holds End Service false with the last data byte transmitted. The IOP may report in the Terminal Order any of the following conditions: Interrupt, Count Done, Command Chain, or IOP Halt.

IOP High Speed Memory

The IOP shall contain a sub-channel position consisting of a fast memory register, 80-bits in length, for each Device Controller connecting to the IOP (24 sub-channel positions maximum). Each sub-channel position shall be used for storing the following kinds of data:

Current command address	16 bits
Current byte address	19 bits
Current byte count	16 bits
Flags and IOP status	29 bits
Total	80 bits

Device Controllers with multiple devices use only sub-channel positions 0-7. Device Controllers with single devices use any of sub-channel positions 0-23. This is determined by the coding of the Device Controller/Device address field in cell 20* by the CPU for SIO, HIO, TIO, to TDV operations or is determined by the coding of the /FR0/ - /FR7/ lines during an AIO operation or during a DC service call.

Cell 20*, Bit	0	1	2	3	4	5	6	7
DC/IOP line	FR0	FR1	FR2	FR3	FR4	FR5	FR6	FR7
DC/Single Device	0			←		DC #		→
DC/Multiple Devices	1	←	DC #	→	←	Device #		→

*Base 16

Referring to the chart above if the most significant address field bit is zero the least significant five-bits are decoded to determine the sub-channel number. If the most significant bit is one then the next three most significant bits are decoded to determine the sub-channel number. This further implies that Device Controllers with single devices may be assigned addresses in the range 00 through 17 (hexadecimal) and Device Controllers with their multiple devices may be assigned address: 80 through FF (hexadecimal).

IOP OPERATIONS DURING CPU REQUESTS FOR SERVICE

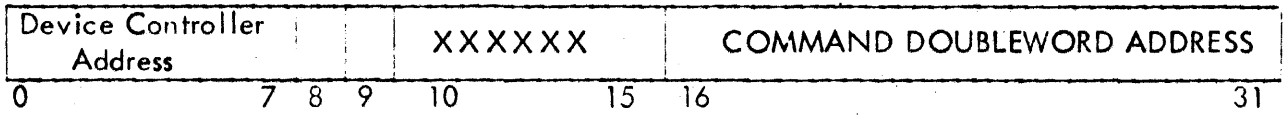
During execution of a CPU request for service the IOP and CPU shall use the lines described in Section 2.4 for direct communication. During execution of a CPU request for service the IOP and CPU shall also communicate indirectly via core memory cells 20* and 21*. The IOP shall also communicate at the Device Controller interface to obtain Condition Code information and Status response.

Specific actions of the IOP during CPU requests for service are described in the paragraphs below.

SIO

The IOP shall make a Memory Request to read memory cell 20*. If a memory parity error is detected the IOP shall terminate the operation immediately. If a memory parity error is not detected then the IOP shall interpret the contents of cell 20* as follows:

Cell 20*



Bits 0 - 7: Contain the Device Controller Address. These bits are transmitted at the Device Controller interface on Data Lines DA0-7. The four least significant bits are also stored in the IOP if the DC goes to the Busy state during the SIO operation.

*Base 16

Bits 8 and 9: Specify the IOP response as follows:

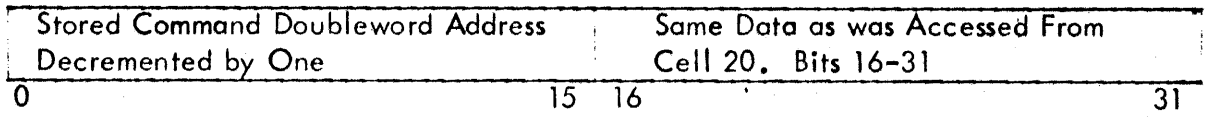
Bit 8	Bit 9	S/IOP Response
0	0	IOP shall respond on NCOND1 and NCOND2 only
0	1	IOP shall respond on NCOND1 and NCOND2 and write in cell 21*
1	1	IOP shall respond on NCOND1 and NCOND2 and write in cells 20* and 21*

Bits 10 - 15: Ignored by the IOP

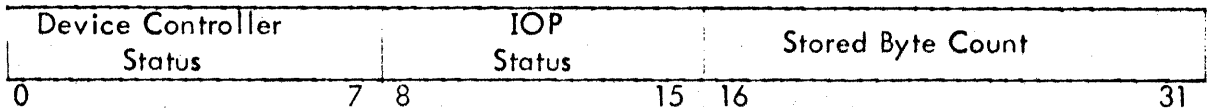
Bits 16 - 31: Contain the Command Doubleword Address that shall subsequently be stored in the IOP if the DC goes to the Busy state during the SIO operation.

The IOP shall communicate at the Device Controller interface with the addressed Device Controller and shall complete the response of the CPU service request by writing into cells 20* and 21* as follows:

Cell 20*



Cell 21*



IOP Status:

*Base 16

TITLE	SDS	
PRODUCT DESIGN SPECIFICATION INPUT/OUTPUT PROCESSOR, MULTIPLEXOR	154991	B
	SHEET 57 OF 83	

The information stored in cells 20* and 21* shall have the following meaning:

Cell 20* Bits 0 - 15: Shall contain the Command Doubleword Address stored in the IOP and decremented by one.

Cell 20* Bits 16 -31: Shall contain the same data as was read from core memory cell 20* bits 16 - 31.

Cell 21* Bits 0 - 7: Shall contain the Device Controller status information obtained from the Function Response lines 0 - 7 at the Device Controller interface.

Cell 21* Bits 8 - 15: Shall contain IOP status information. Bits 8 - 14 shall be cleared prior to termination of the CPU service if the DC goes to the Busy state. The IOP status bits are defined in greater detail below.

Cell 21* Bits 16 - 31: Shall contain the Byte Count currently stored in the IOP.

IOP Status Bits:

Bit 8: Incorrect Length: This bit shall be set true if Incorrect Length was signalled by the Device Controller via the Order In Operational Status Byte.

Bit 9: Transmission Data Error: This bit shall be set true if Transmission Error was signalled by the Device Controller via the Order In Operational Status Byte or if the IOP detected a byte parity error during a Data In operation.

Bit 10: Transmission Memory Error: This bit shall be set true if a Memory Parity Error was detected by the IOP during a Data Out/In operation (memory partial-word write or read operations).

Bit 11: Memory Address Error: This bit shall be set true if a non-implemented memory address was detected by the IOP during a chaining operation or a Data Out/In operation.

*Base 16

Bit 12: IOP Memory Error: This bit shall be set true if the IOP detected a memory parity error while fetching a command.

Bit 13: IOP Control Error: This bit shall be set true if the IOP detected two successive Transfer in Channel commands.

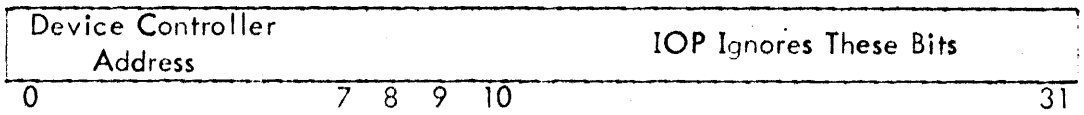
Bit 14: IOP Halt: This bit shall be set true if the IOP detected an IOP Halt condition.

Bit 15: This bit shall be false

2.8.2 HIO, TIO, TDV

The IOP shall make a Memory Request to read cell 20*. If a memory parity error was detected then the IOP shall terminate the operation immediately. If a memory parity was not detected, then the IOP shall interpret the contents of cell 20* as follows:

Cell 20*



Bits 0 - 7: Contain the Device Controller Address. The IOP shall transmit these bits at the Device Controller interface on Data Lines DA0-7.

Bits 8 and 9: The IOP shall respond to these bits as defined in Section 2.7.1 for the SIO operation.

Bits 10 - 31: The IOP shall ignore these bits.

*Base 16

The IOP shall then communicate at the Device Controller interface with the addressed Device Controller and shall complete the response to the CPU request for service by writing - if requested - into cells 20* and 21*. The format of these responses shall be the same as the format of responses defined in Section 2.7.1 for an SIO operation. The definition of the individual bits shall be the same as defined in Section 2.7.1 for an SIO operation.

2.8.3 AIO

During the execution of an AIO instruction the highest priority IOP with an interrupt pending shall inhibit the Control Strobe from passing to lower priority IOP's.

The IOP shall communicate at the Device Controller interface to obtain the address and status of the interrupting Device Controller. The IOP shall then assemble the status and Device Controller address and make a Memory Request to write into cell 20*. The format of the information written into cell 20* shall be as follows:

Cell 20*

Device Controller Status	IOP Status	0 0 0 0 0	IOP Addr	Device Controller Address
0 7	8 15	16 20	21 23	24 31

IOP Status:

IL	TDE	ZBC I	CE I	UE I	0	0	0

* Base 16

Bits 0 - 7: Shall contai n the Device Controller status information received on the Data Lines DA0-7.

Bits 8 - 15: Shall contain IOP status information defined below in further detail.

Bits 16 - 20: Shall always be false.

Bits 21 - 23: Shall contain the address of the responding IOP.

Bits 24 - 31: Shall contain the address of the responding Device Controller. The IOP shall compare this address with the Device Controller address stored in the IOP and shall if the Device Controller also raises the DOR line (CC1 = 0) write the IOP status into bits 8 - 15 of cell 20* and shall then clear the interrupt status bits.

IOP Status Bits:

Bit 8: Incorrect Length: As defined for SIO in Section 6.3.1.

Bit 9: Transmission Data Error: As defined for SIO in Section 6.3.1.

Bit 10: Zero Byte Count Interrupt: This bit shall be set true if the Interrupt on Zero Count flag is true and Zero Byte Count is detected.

Bit 11: Channel End Interrupt: This bit shall be set true if the Interrupt at Channel End flag is true and Channel End is signalled during an Order In via the Operational Status Byte.

Bit 12: Unusual End Interrupt: This bit shall be set true if the Interrupt at Unusual End flag is true and Unusual End is signalled during an Order In via the Operational Status Byte or if IOP Halt is signalled to the Device Controller in the Order In Terminal Order.

* Base 16

Bit 13: This bit shall be false.

Bit 14: This bit shall be false.

Bit 15: This bit shall be false.

2.9 IOP OPERATIONS DURING DEVICE CONTROLLER SERVICE REQUESTS

Responses of the IOP to Device Controller service requests will be defined in this section.

The IOP shall respond to a Service Call from a Device Controller by raising the ASC Function Indicator line, delay, and then raise the Function Strobe line. A Device Controller indicates that it will connect for service by driving the Function Response lines with the Device Controller address and raising the Function Strobe Acknowledge Line; otherwise, the lowest priority Device Controller drives the AVO line and the service request is aborted.

The Device Controller, if connected for service, then initially raises the Request Strobe line. The IOP detects the type of service (Order Out, Order In, Data Out, or Data In) by strobing and decoding the DOR and IOR lines. If an Order In operation is specified the IOP strobes the Operational Status Byte on the DA0-7 lines or strobes the data on the appropriate Data Lines if this is a Data In operation. If an output operation is specified the IOP shall access core memory and if this is an Order Out place the order on the DA0-7 lines or if this is a Data Out operation place data on the appropriate Data Lines. The state of the End Data and End Service lines shall then specify how the service shall terminate.

In the paragraphs that follow the action of the IOP in response to the specific types of service requests (Order Out/In, Data Out/In) will be defined.

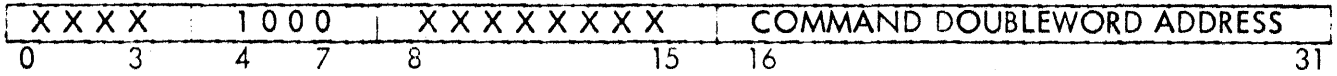
2.9.1 Order Out

If the Device Controller has requested that the IOP perform an Order Out operation by raising DOR and IOR with the initial RS then the IOP shall take the following action:

(a) Examine the state of the Chaining Modifier bit. If the Chaining Modifier is true the IOP shall increment the current Command Doubleword address by one and clear the Chaining Modifier bit.

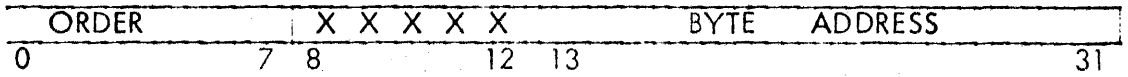
(b) Request a core memory read operation from the memory location specified by the Command Doubleword address. If a Memory Address Error was detected the IOP shall set the Memory Address Error and IOP Halt status bits. If a memory parity error was detected then the IOP shall set the IOP Memory Error and IOP Halt status bits. In either case the IOP shall respond immediately to the initial RS by raising RSA and shall report - at least - IOP Halt in the ensuing Terminal Order.

(c) If a Memory Address Error or Memory Parity Error was not detected then the IOP shall operate on the even Command word as follows:



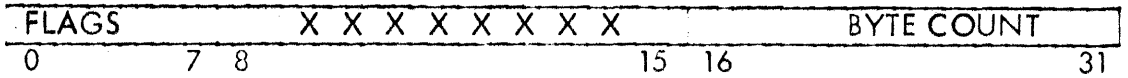
If bits 4-7 are coded as shown above then the IOP shall interpret this as a Transfer in Channel Command, ignore the State of bits 0-3 and bits 8-15 and store the contents of bits 16-31 into the Command Address register. If this is the second successive Transfer in Channel Command, detected by the IOP then the IOP shall set the IOP Control Error and

IOP Halt status bits and immediately respond to the initial RS by raising RSA and report - at least - IOP Halt in the Terminal Order. Otherwise, the IOP shall access the core memory location specified by the Command Address register and operate on the even Command word as follows (if no Memory Address Error or Memory Parity Error):



The IOP shall transfer bits 0-7 unchanged to the DA0-7 lines, delay, and then raise RSA. The IOP shall also examine bits 0-7 to determine whether the Read Backward order (XXXX 1100) has been coded. If this order has been coded then the IOP shall store this state as a control function during Data In operations. The IOP shall ignore the state of bits 8-12 and shall store bits 13-31 into the Byte Address register.

(d) The IOP shall then increment the even Command word address by one and access core memory for the odd Command word and shall also increment the Command Doubleword Address register by one. The IOP shall operate on the odd Command word as follows (if no Memory Parity Error):



Bits 0-7 contain the flags. The IOP shall store these into the flags register. The response of the IOP to the flags will be defined below. The IOP shall ignore the state of bits 8-15 and shall store bits 16-31 into the Byte Count register.

(e) The response of the IOP to the flags shall be as follows:

Bits 0: Data Chain (DC) flag - During a Data Out/In operation if the Byte Count has gone to zero and the Data Chain flag was true then the IOP shall access the next Command Doubleword. During the Data Chaining operation the IOP shall perform all those operations previously defined for the Order Out operation except that the IOP shall not send the order in bits 0-7 of the Command even word to the Device Controller.

Bit 1: Interrupt on Zero Count (IZC) flag - If, during a Data Out/In operation the Byte Count has gone to zero and this flag was true the IOP shall set the Zero Byte Count Interrupt status bit and shall report Interrupt in the Terminal Order.

Bit 2: Command Chain (CC) flag - During each Terminal Order in which the CC flag is true, the IOP shall report Command Chain.

Bit 3: Interrupt at Channel End (ICE) flag - If, during an Order In, the Device Controller reported Channel End and this flag was true then the IOP shall set the Channel End Interrupt status bit and shall report Interrupt in the ensuing Terminal Order.

Bit 4: Halt on Transmission Error (HTE) flag - If, during an Order In, the HTE flag was true and the Device Controller reported Transmission Error or reported Incorrect Length and the Suppress Incorrect Length flag was false then the IOP shall set the IOP Halt status bit and shall report IOP Halt in the ensuing Terminal Order. During a Data In operation if the HTE flag was true and the IOP detected a Transmission Data Error (byte parity error at Device Controller interface)

then the IOP shall set the IOP Halt status bit and report IOP Halt in the Terminal Order. If, during Data Out/In operations, the HTE flag was true and the IOP detected a Transmission Memory Error (memory parity error during read or partial write for data exchange) then the IOP shall set the IOP Halt status bit and report IOP Halt in the Terminal Order.

Bit 5: Interrupt on Unusual End (IUE) flag - If, during an Order In, the Device Controller reported Unusual End of if the IOP Halt state existed at that time and the IUE bit was true then the IOP shall set the Unusual End Interrupt status bit and report - at least - Interrupt in the ensuing Terminal Order.

Bit 6: Supress Incorrect Length (SIL) flag - If, during an Order In operation, the SIL flag was false and the HTE flag was true and Incorrect Length was reported then the IOP shall set the IOP Halt status bit and report - at least - IOP Halt in the ensuing Terminal Order.

Bit 7: Skip (S) flag - If this bit was true the IOP shall during Data Out/In operations perform all functions associated with that operation except core memory accesses.

(f) After operating on the Command odd word as defined in (d) above the IOP shall wait for the Terminal Order Request Strobe from the Device Controller. The IOP shall then set End Service, place the Terminal Order on the DA0-7 lines, delay, and raise RSA to terminate the Order Out sequence. The information exchanged during the Terminal Order will be defined in a later section.

2.9.2 Order In

If the Device Controller has requested that the IOP perform an Order In by raising only the DOR line with the initial RS then the IOP shall take the following action:

(a) The IOP shall strobe the End Data line and the DA0-7 lines. Sensing that the Device Controller has raised the ED line, the IOP shall also drive the ED line. The IOP shall respond to the Operational Status Byte on the DA0-7 lines as follows:

DA0 - Transmission Error: If this line was true the IOP shall set the Transmission Data Error status bit. If the HTE flag was true then the IOP shall also set the IOP Halt status bit and report IOP Halt in the ensuing Terminal Order.

DA1 - Incorrect Length: If this line was true the IOP shall set the Incorrect Length status bit. If the SIL flag was false and the HTE flag was true the IOP shall also set the IOP Halt status bit and report IOP Halt in the ensuing Terminal Order.

DA2 - Chaining Modifier: If this line was true then the IOP shall store this condition. During the next Order Out the IOP shall increment the Command Doubleword Address in the Command Address register by one, as described in Section 2.8.1 and shall clear the Chaining Modifier control bit. IOP shall also during a successful SIO operation clear the Chaining Modifier control bit.

DA3 - Channel End: If this line was true the IOP shall, if the Interrupt at Channel End flag was true, set the Channel End Interrupt status bit and shall also signal Interrupt in the ensuing Terminal Order.

DA4 - Unusual End: If this line was true the IOP shall, if the Interrupt at Unusual End flag was true, set the Unusual End Interrupt status bit and also signal Interrupt in the ensuing Terminal Order.

(b) The IOP shall delay after raising the ED line and then raise the RSA line. The IOP shall then wait for the Terminal Order Request Strobe, place the Terminal Order on the DA0-7 lines, raise the ES line, delay, and raise RSA to terminate the Order In sequence.

2.9.3 Data Out

If the DC requests that the IOP perform a Data Out operation by raising only the IOR line with the initial RS of a service cycle then the IOP shall respond as follows:

(a) Access the core memory address designated by the byte address register and store the data in the memory interface register.

(b) If the DC interface data path is one-byte wide drive the DA0-7 lines with the data byte designated by the current byte address, generate odd parity for that data byte and drive DAP accordingly, increment the byte address register, decrement the byte count register, then delay and drive the RSA line. This cycle repeats until ED is raised. Note that a maximum of four data bytes may be exchanged during a DC service cycle. If the byte count decrements to zero and the data chain flag is true then the IOP shall also access the next command doubleword before termination of the service cycle. If the ES line was not raised with the ED line then the IOP shall expect a Terminal Order request from the DC.

(c) If the four-byte interface option is present and the DX4 line is true then the IOP shall transfer the contents of the memory interface register to the DC interface, increment the byte address register by four, decrement the byte count register by four, drive the ED line, then delay and drive the RSA line in response to the initial RS. Note that only one

data exchange may be made in this case. The IOP shall perform data chaining before termination of the cycle - if required. Dependent on the state of the ES line the IOP shall either terminate the service cycle with the data exchange or shall wait for the terminal order request and then terminate the service cycle.

2.9.4 Data In

If the DC requests that the IOP perform a Data In operation by holding DOR and IOR false with the initial RS then the IOP shall respond as follows:

(a) If the DC interface is one-byte wide the IOP shall delay after receiving each RS, strobe the data lines (except during Terminal Order), check parity if required, transfer the data to the appropriate memory interface register byte, increment the byte address register (decrement if READ BACKWARD was indicated), decrement the byte count register, and raise RSA. The IOP shall repeat this sequence until the ED line is raised (note that four bytes maximum may be exchanged). When ED has been raised the IOP then accesses the core memory address designated by the byte address register and initiates a full or partial-write memory operation. If data chaining is required then the IOP shall access the next command double-word before termination of the service cycle. Dependent on the state of the ES line the IOP shall either terminate the service cycle with the last data exchange or wait for the Terminal Order request from the DC before termination.

(b) If the four-byte interface option is present and the DX4 line is true then the IOP shall delay after receiving the initial RS, strobe the data lines, transfer the word of data to the memory interface register, increment the byte address register by four, decrement byte count register by four, raise ED, then delay and raise RSA. Note that only one data exchange may be made for this case. Note also that the performance of the IOP is not defined for the READ BACKWARD order in this mode of operation. The IOP then accesses

the core memory location designated by the state of the byte address register prior to updating and initiates a full-write memory operation. Again, the IOP shall perform data chaining if required and shall terminate the service cycle with a Terminal Order if the state of the ED and ES lines so dictate.

2.9.5 Terminal Order

As previously defined the IOP shall terminate each Device Controller Order Out/In service sequence with a Terminal Order exchange and may also terminate Data Out/In service sequences with a Terminal Order. The definition of the DA0-3 Data lines during the Terminal Order exchange shall be as follows:

DA0 Interrupt: This line shall be raised by the IOP during the Terminal Order for the following reasons:

(a) During an Order In the Interrupt at Channel End flag was true and the Device Controller signalled Channel End.

(b) During an Order In the Interrupt at Unusual End flag was true and the Device Controller signalled Unusual End or the IOP Halt status bit was true.

(c) If the Byte Count goes to zero and the Interrupt at Zero Byte Count flag is true.

DA1 Count Done: The IOP shall raise this line during the Terminal Order, if the Byte Count has gone to zero, and the Data Chain flag is false.

DA2 Command Chain: The IOP shall raise this line during every Terminal Order exchange in which the Command Chain flag is true.

DA3 IOP Halt: The IOP shall raise this line during every Terminal Order exchange in which the IOP Halt status bit is true.

2.10 Memory Bus Sharing

In this section is defined the bus-sharing interface through which two MIOP's exchange control signals related to this option.. In addition, the actions and responses are described for an MIOP with this option installed.

2.10.1 Cable Connections

MIOP's that share a core memory bus shall connect the five IOP/Core Memory cables to a common memory bus as shown in Figure 2.3. In addition, the bus-sharing interface of the two MIOP's shall be interconnected with a single cable. Signals exchanged at the bus-sharing interface shall be via AT11 cable Driver/Receiver modules.

2.10.2 Switch Settings

An LT26 switch module is located in each of the bus-sharing MIOP's. One switch on the LT26 module designates the relative priority of the two IOP's. The IOP containing the priority determining logic shall be designated as the AIOP. The AIOP shall have this switch set to the ONE state. The other or BIOP shall have this switch set to the ZERO state. When simultaneous requests for the core memory bus are made the BIOP shall have highest priority.

2.10.3 Signal Lines Interconnecting MIOP's at the Bus-sharing Interface

The lines tabulated below shall interconnect two bus-sharing MIOP's at the bus-share interface:

Description	Designation	No. of Lines	Signal Flow Direction	
			AIOP to BIOP	BIOP to AIOP
Memory Bus Request BIOP	MRQB	1		X
Memory Cycle for BIOP	MCFB	1	X	
Memory Cycle for BIOP/1	MCFB/1	1	X	
MCFB Clear	MBRB	1		X
MCFB/1 Clear	MBRB/1	1		X

2.10.4 Definition of Bus-share Interface Lines

Memory Bus Request BIOP (MRQB):

This line shall be driven by the BIOP only. The BIOP shall drive this line to request the use of the core memory bus during those I OP operations in which MIOP/Core Memory data exchanges are required. The BIOP shall drop this line not less than 190 nanoseconds after receiving the MCFB signal at the cable receiver output for I/O instruction sequences (SIO, HIO, TIO, TDV, AIO) or chaining sequences (Order Out or Data Chaining) or after receiving the MCFB/1 signal at the cable receiver output for Data Out or Data In sequences.

In response to a request by theBIOP for the Core Memory Bus, the AIOP shall grant use of the bus by raising the MCFB and MCFB/1 lines.

The BIOP shall have priority over the AIOP in use of the core memory bus.

Memory Cycle For BIOP (MCFB):

The AIOP shall drive this line in response to a memory bus request by the BIOP on the MRQB line. The AIOP shall drop this line in response to an MCFB Clear signal from the BIOP on the MBRB line. When the MCFB line goes true the BIOP shall do the following:

1) Enable the sequence in which the Memory Request (MQ) is raised for I/O instruction sequences (SIO, HIO, TIO, TDV, AIO) or chaining sequences (Order Out of Data Chaining).
2) Enable the following memory interface lines to be driven by the BIOP:
   Address lines (L15-31)
   Data lines (M00-31)
   Write byte lines (MW0-3)

Memory Cycle For BIOP/1 (MCFB/1):

The AIOP shall drive this line in response to a memory bus request by the BIOP on the MRQB line. The AIOP shall drop this line in response to a MCFB/1 clear signal from the BIOP on the MBRB/1 line. When the MCFB line goes true the BIOP shall do the following:

1) Enable the sequence in which the Memory Request (MQ) is raised for Data Out or Data In service.
2) Enable the following memory interface lines to be driven by the SIOP:
   Address lines (L15-31)
   Data lines (M00-31)
   Write byte lines (MW 0-3)

MCFB Clear (MBRB):

The BIOP shall drive this line to request the AIOP to drop the MCFB line. The BIOP shall drive this line not less than 190 nanoseconds after receiving the MCFB signal (measured at cable receiver output) during I/O instruction sequences (SIO, HIO, TIO, TDV, AIO) or chaining sequences (Order Out or Data Chaining) or after receiving the MCFB/1 signal (measured at cable receiver output) during Data Out or Data In sequences. The AIOP shall cause the MCFB line to drop immediately on receiving the MBRB signal.

MCFB/1 Clear (MBRB/1):

The BIOP shall drive this line to request the AIOP to drop the MCFB/1 line. The BIOP shall drive this line at the completion of the use of the bus. Termination of the memory bus use is defined as follows:

1) MQ (Memory Request) not raised
2) MQ raised and non-implemented memory address detected (Not Address Here)
3) MQ raised for full-write and DR (Data Release) received from core
4) MQ raised for partial-write or read and parity release (POK or PE) received.

The AIOP shall cause the MCFB/1 line to drop immediately on receiving the MBRB/1 signal.

2.10.5 Cables

As specified in Section 2.9.1 a single cable shall interconnect two bus-sharing MIOP's at the bus-share interface. The maximum length of this cable shall be 5.5 feet. The pin assignment for signals in that cable at the cable Driver/Receiver and cable connector interface shall be as specified below:

AT11 Cable Driver/Receiver Module

Connector Pin	Signal Designation at Connector	Signal Functional Description
01	MCFB	Memory Cycle For BIOP
02	MRQB	Memory Bus Request BIOP
03	MBRB	MCFB Clear
04	MCFB/1	Memory Cycle For BIOP
05	MBRB/1	MCFB/1 Clear
06	*	
07	*	
08	*	
09	*	
10	*	
11	*	
12	*	
13	*	
14	*	

* NOT ASSIGNED

2.11 IOP Display Operations:

The IOP display option is mainly for the purpose of maintainability and it shall not affect the IOP normal operations. The display interface is actuated by two CPU instructions; Read Direct for putting IOP status information into a CPU general register, and Write Direct for controlling the IOP operation.

2.11.1 Write Direct Instruction

To control the MIOP through its display interface, the Write Direct instruction must address the attached MS with the DIO trunk address lines as follows:

A0 - A2 = 001
A3 - A10 = Determined by the eight switches in the MS selecting DIO address. By convention, the switch associated with A3 will always be set to 0.
A11 = 1
A12 - A15 = Are not significant.

The data word transmitted on DIO lines DB16 thru DB31 is sent to the MIOP on the display interface via DIO:DB16:R thru DIO:DB31:R along with the RD/WD Indicator and the IOP strobe. Only three lines are used to control the MIOP; they are:

DIO:DB29:R - Reset I/O
DIO:DB30:R - Stop Normal Phase Sequence
DIO:DB31:R - Single Phase Step

Only one line of these shall be true at a time. Two or more of the three lines true makes the result unpredictable. The action of the MIOP upon receipt of each of these control lines is as follows:

2.11.1.1 Reset I/O:

When this line is true, the MIOP shall be reset and pass the reset signal to I/O interface /RST/ line. This control performs exactly as /RIO/ at CPU interface.

2.11.1.2 Stop Normal Sequence:

When this line is true, a latch in the MIOP is set and the inputs to the delay line are inhibited. This condition shall exist independent of successive WD instructions making this line false until the above Reset I/O line or (RIO) becomes true.

2.11.1.3 Single Phase Step:

When this line is true, the MIOP shall let the delay line run once if other conditions to start the delay line in the normal MIOP operations are met. This causes the MIOP to complete one phase, and stop at the end of that phase. By issuing this control repeatedly, the MIOP shall go through all the phases in its normal sequence.

2.11.2 Read Direct Instruction

To transfer the states of a group of 16 internal MIOP signals to a CPU general register via the DIO trunk, the Read Direct instruction must address the attached MS in the same manner as described for the Write Direct instruction (2.11.1) except that A13-A15 are sent to the MIOP via the display interface to select which of the seven groups of signals are to be transferred. A13-A15 is the binary group address with A15 the least significant bit.

Upon receipt of the IOP Strobe and the RD/WD Indicator (off for Read Direct), the MIOP decodes the address lines DIO:A13:R-DIO:A15:R and selects one of seven groups of 16 signals to gate into lines DIS:00-DIS:15 of the display interface for transfer to the CPU via the DIO lines DB15-DB31. A detailed chart showing the signals transferred in each group and their respective lines is shown on the next page. Group zero transfers zeros on all 16 lines.

READ DIRECT DISPLAY GROUPS

GROUP	DIS:00	DIS:01	DIS:02	DIS:03	DIS:04	DIS:05	DIS:06	DIS:07	DIS:08	DIS:09	DIS:10	DIS:11	DIS:12	DIS:13	DIS-14	DIS:15
1	PH01/02	PH01/PD2	PH00D1	PH00PD1	PH10D1	PH10PD1	PH11D1	PH11PD1	PH12D1	PH12PD1	PH13D1	PH13PD1	PH14D1	PH14PD1	PR1	PR2
2	PH00D1	PH00PD1	PH01D1	PH01PD1	PH02D1	PH02PD1	PH03D1	PH03PD1	PH04D1	PH04PD1	PH05D1	PH05PD1	PH06D1	PH06PD1	PH07D1	PH07PD1
3	MAE	MAR	MDR	MPE	MRQ	MS	PRCH	TPE	EH	EHE	DL3CYCLE	AIOP	MCFA	MCFA/1	MCFB	MCFB/1
4	ORD	OUT	WI	FIN	FP	TORD	TRA1	ZBC	FS:D	FSL:R	RS:R	RSA:D	LASTSNE	AVO:R		
5	A00	A01	A02	A03	A04	A05	A06	A07	LS0	LS1	LS2	K15	SUB	UNO	UN1	UN2
6	H0	H1	H2	H3	H4	H5	H6	H7	CC1	CC2	CMD	IER:D	IR:D	FNC	J1	J2
7	C00	C01	C02	C03	C04	C05	C06	C07	C08	C09	C10	C11	C12	C13	C14	C15

2.11.3 Typical Programming

The following listing shows typical procedures to display the MIOP status during a SIO and a subsequent Order Out operation.

Step	Instruction	Address to	Function
1	WD	MS	Disconnect all Device Controllers to eliminate undesirable interferences
2	WD	IOP via MS	Reset I/O. To initialize both IOP and MS (Set DB29)
3	RD	IOP, MS	Verify Reset if necessary
4	WD	MS	Load DC address into MS (MS Group A)
5	WD	MS	Load status into MS (MS Group 9)
6	WD	IOP via MS	Stop IOP Normal Phase Sequence (Set DB30)
7	WD	MS	Inhibit SC:D for an O.O. issued by MS immediately after it senses FS drop at IOP phase 12 T2.
8	SIO	IOP, DC	Start I/O. DC address coded in the instruction word is the same as programmed in MS at Step 4. IOP stops at the end of PHOOD1, no PR back to CPU, program TRAP brings back control to next instruction.
9	RD	MS IOP via MS	Display IOP and MS status, one RD for each group
10	WD	IOP via MS	IOP Single phase stepping, IOP enters next phase in sequence. (DB31 set)
11	RD	MS IOP via MS	Display MS and IOP status of next IOP phase
12	RD,WD		Repeat Steps 10, 11 for all phases.

Order Out:

Step	Instruction	Address to	Function
1	WD	MS	Issue SC for O.O. (MS Group B with DB29 set), IOP stops at the end of PHOOD1
2	RD	MS IOP via MS	Display
3	WD	MS	Inhibit next SC for D.O. or D.I.
4	WD	IOP via MS	IOP sequences to the end of next phase.
5	RD, WD		Repeat steps 3, 4 for all phases in sequence.