PIED PIPER™

Technical Reference Manual

PIED PIPER

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Part No.: P/N 20000102
Price: $125.00 in U.S.A.

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First Printing - June 1983

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CHAPTER 1 SPECIFICATIONS

1.1 Hardware

Processor:	Z80A microprocessor 4 Mhz clock
Memory:	64 Kbytes user read/write memory (RAM) 4 Kbytes of read only memory (ROM) 2 Kbytes of video display buffer 2 Kbytes of display read only memory
Keyboard:	Full size, typewriter-style Upper/lower case Control & function keys 2-key lockout with contact debounce auto-repeat on all keys
Parallel Port:	Centronics-type parallel output port
Display:	24 lines of 80 characters each with video monitor (not supplied) 24 lines of 40 characters each with standard television (not supplied) Connector for RF modulator (not supplied) required for TV display Horizontal scrolling keys for TV display allows proper viewing of 80 column lines Displays full ASCII character set, upper and lower case, plus character graphics
Floppy Disk Drive:	5 1/4 inch slimline drive 1 Mbyte unformatted storage capacity per diskette 800 Kbytes formatted storage capacity per diskette
Power Supply:	Switching power supply Sufficient capacity for optional floppy disk drive
Expandability:	Interface for second floppy disk drive built in Interface for optional hard disk drive built in STD bus I/O interface built in Internal provision for mounting one expansion card

1.2 Software

Operating System:

CP/M 2.2 from Digital Research Inc.
PIED PIPER Utilities including formatting, file transfer and backup with one disk drive

Applications:

Perfect Writer - word processing
Perfect Speller - 50,000 word spelling dictionary
Perfect Calc - Electronic spread-sheet
Perfect Filer - Data filing/merging

1.3 General

Dimensions:

Height	Width	Depth
4.0 in.	20.2 in.	10.8 in.
10 cm	51 cm	27 cm

Weight:

12.5 lb. (5.6 Kg.)

Electrical:

115 VAC 60 Hz
230 VAC 50 Hz optional
60 watts maximum power consumption

Environmental:

Operating - 50 F to 95 F (10 C to 35 C)
- 20% to 80% rel. humidity
Storage -
-

CHAPTER 2 SYSTEM OVERVIEW

The PIED PIPER hardware consists of four main modules: the main printed circuit board, the keyboard assembly, the floppy disk drive, and the switching power supply. All modules are mounted inside a shielded plastic case. The software accessible to the user includes the bootstrap program, the video display character generator, and the CP/M BIOS program. This manual will provide technical information on these modules.

2.1 Hardware Configuration

A block diagram of the PIED PIPER hardware organization is given in Fig. 2.1. The main microprocessor is a Z80A running at 4 MHz. The memory space is normally occupied by 64 Kbytes of fast dynamic RAM. After a system reset or on startup, 4 Kbytes of read only memory are switched in to replace the bottom half of the RAM. This is used to start up the system and load the disk operating system. The ROM can also be switched in/out under software control. All the peripheral controllers use programmed data transfers to communicate with the central microprocessor. Eight interrupts are configured for the sytem. Two are used by the floppy disk drive controller to indicate that its data buffer is full (DRQ) or that it has finished executing the last command (INTRQ). The video display controller uses one interrupt to indicate to the CPU when it has completed the requested command. The keyboard controller can use an interrupt to indicate when it contains key-pressed data, but this interrupt is not enabled by the system software. Another interrupt comes from a timer which is contained in the keyboard controller. This interrupt is used as an interval timer by the system software. The remaining three interrupts are available for use by the expansion cards or expansion bus.

In addition to the standard peripheral controllers, the system contains some internal I/O ports which serve the function of control/status registers. By writing data to the control registers, changes can be made to the initial hardware setup (for example, the video display format). By reading data from the status register, information can be obtained on the present state of the hardware peripherals (for example, if any interrupts are pending). These registers are initialized at startup. Changes in their contents should be made with care as it could prevent normal system operation.

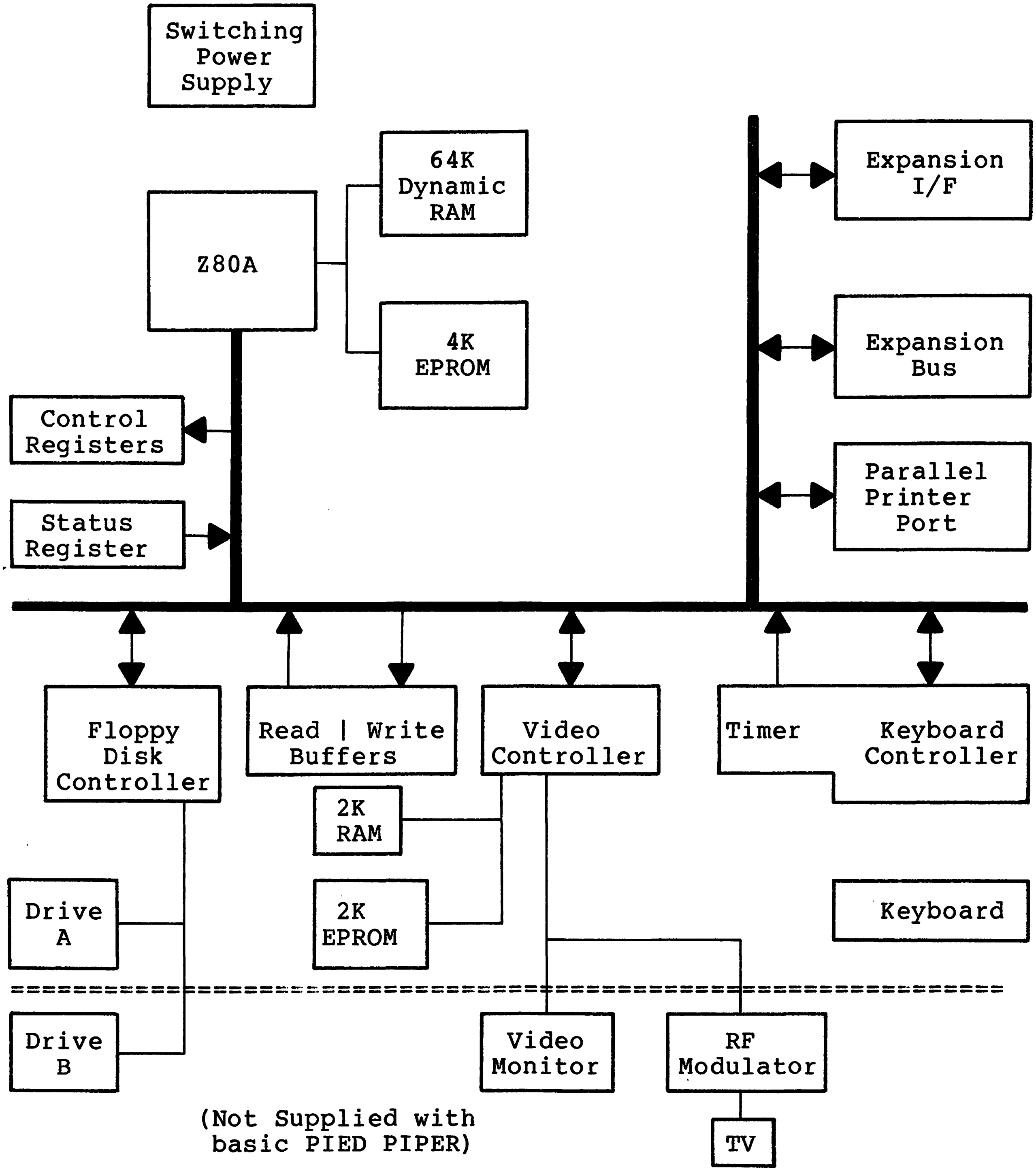


Fig. 2.1 Basic PIED PIPER hardware configuration.

2.2 Memory Map

The PIED PIPER has a total of 72 Kbytes of memory. These include the following:

- 64K RAM system memory
- 4K bootstrap ROM
- 2K RAM display memory
- 2K character generator ROM

Only the bootstrap ROM and the system memory use the Z80A processor memory address space. The display memory is accessed through I/O addresses, and the character generator ROM is accessed solely by the video display controller.

Although the bootstrap ROM is only 4 Kbytes in size, the PIED PIPER is capable of accommodating ROM of up to 16 Kbytes in size. Both the system memory and the bootstrap ROM share the memory addresses from 0000 hex to 7FFF hex, but only one will be activated at any given time. When the ROM is enabled, access to memory addresses 0000 to 7FFF hex will be directed to the ROM. When the ROM is disabled, access will be directed to the system RAM memory.

The bootstrap ROM contains hardware initialization procedures, self test diagnostics, and the bootstrap routine for bringing in the first sector of the first track from the floppy diskette. The content of this ROM is copied to RAM starting from location F000 hex, after some preliminary self tests. The ROM is then disabled, and the remaining self tests plus the bootstrap procedure are executed from the RAM area.

```
FFFFH¯|-----------------------------------|
      |    Interrupt handling routines    |
      |                +                  |
      |    Disk Input/Output routines     |
      |                +                  |
      |    Reserved Data area             |
      |                +                  |
      |    Jump vectors for useful        |
      |            routines               |
FB10H_|-----------------------------------|
      |    Interrupt vectors              |
FB00H_|-----------------------------------|
      |    Reserved area for option       |
      |         card programs             |
F500H_|-----------------------------------|
      |    Basic Input Output System      |
      |             (BIOS)                |
E200H_|-----------------------------------|
      |    Basic Disk Operating System    |
      |             (BDOS)                |
D400H_|-----------------------------------|
      |    Console Command Processor      |
      |             (CCP)                 |
CC00H_|-----------------------------------|
      |                                   |
      |                                   |
      |                                   |
      |                                   |
      |                                   |
      |                                   |
      |                                   |
      |                                   |
      |                                   |
      |                                   |
      |    Transient Program Area         |
      |             (TPA)                 |
      |                                   |
      |                                   |
      |                                   |
      |                                   |
      |                                   |
      |                                   |
      |                                   |
      |                                   |
0100H_|-----------------------------------|
      |    Page 0, reserved for CP/M      |
0000H_-------------------------------------
```

System memory map after initialization.

2.3 I/O Port Assignments

The CPU address lines are decoded, along with the input/output control lines, to split the I/O port address space into banks of I/O ports. There are eight banks decoded, with each bank containing up to eight sequentially addressed I/O ports. Each bank has its own enabling signal (CS0 to CS7).

The I/O port addresses used by the system software and hardware and their functions are described as follows :-

Bank 0: Ports 00H-07H (Enabling Signal CS0)

All Ports Relate to the Video Controller

PORT	READ	WRITE
00H	Interrupt Register	Initialization Register
01H	Status Register	Command Register
02H	Screen Start Address Register (low byte)	Screen Start Address Register (low byte)
03H	Screen Start Address Register (high byte)	Screen Start Address Register (high byte)
04H	Cursor Address Register (low byte)	Cursor Address Register (low byte)
05H	Cursor Address Register (high byte)	Cursor Address Register (high byte)
06H	- -	Pointer Address Register (low byte)
07H	- -	Pointer Address Register (high byte)

Bank 1: Ports 08H-0FH (Enabling Signal CS1)

PORT	READ	WRITE
08H	Keyboard Controller Data Register	Keyboard Controller Data Register
09H	Keyboard Controller Status Register	Keyboard Controller Command Register
0DH	Display Buffer (Read)	Parallel Output (Printer) Port

Bank 2: Ports 10H-17H (Enabling Signal CS2)

All Ports Relate to the Floppy Disk Controller

PORT	READ	WRITE
10H	Status Register	Command Register
11H	Track Register	Track Register
12H	Sector Register	Sector Register
13H	Data Register	Data Register

Bank 3: Ports 18H-1FH (Enabling Signal CS3)

PORT	READ	WRITE
18H	STATUS REGISTER	CONTROL REGISTER I
1CH	- -	Display Buffer (Write)
1DH	- -	CONTROL REGISTER II

Bank 4: Ports 20H-27H (Enabling Signal CS4)

Reserved for Expansion Card #1 [J8]

Bank 5: Ports 28H-2FH (Enabling Signal CS5)

Reserved for Expansion Card #2 [J7]

Bank 6: Ports 30H-37H (Enabling Signal CS6)

Reserved for Hard Disk Interface

Bank 7: Ports 38H-3FH (Enabling Signal CS7)

Reserved for Expansion Bus [J1] and Expansion Cards #1 and #2 [J8,J7]

2.4 Interrupt Assignments

The PIED PIPER is programmed to respond to maskable interrupt mode 2 of the Z80A processor. The interrupt vectors are located from memory address FB00 hex to FB0F hex.

Eight interrupts are supported by the PIED PIPER. These are listed below in descending priority.

1. Disk data request (DRQ)
2. Disk controller interrupt request (INTRQ)
3. Video display controller
4. Keyboard controller
5. Timer
6. Expansion connector J8
7. Expansion connector J7
8. STD Bus connector J1

3.1 Printed Circuit Board Connections

The following sub-sections give pin assignments for all connection points to the printed circuit board. This is intended as a quick reference only. Detailed descriptions of the signal labels and their specifications are included in other sections of this Chapter.

Keyboard Connector [J13]:

The pin assignments for the keyboard connector are as follows:-

Pin No.	Signal Name	Pin No.	Signal Name
1	CNTL	2	CAPLK/
3	SHIFT/	4	RL0
5	RL1	6	RL2
7	RL3	8	RL4
9	RL5	10	RL6
11	CL0	12	RL7
13	CL1	14	CL2
15	CL3	16	CL4
17	CL5	18	CL6
19	CL7	20	Signal Ground
21	CO0/	22	CO1/
23	+5V	24	SPK

Reset Switch:

A push button switch is included on the board to produce the reset signal for the system and any expansion boards. The pin assignment for the reset switch [J5] is as follows:-

Pin No.	Description
1	Signal Ground
2	Reset Signal. This line goes low when the reset button is depressed.

Composite Video Jack [J2]:

This is an RCA phono jack which provides the RS170 standard video signal to the optional video monitor. The pin assignments are as follows : -

Pin No.	Description
1	Composite Video signal of approximately 1.3 volts peak to peak amplitude into a 75 Ohm load impedance
2	Chassis Ground

RF Modulator Jack [J4]:

This is a 5 pin Din type jack compatible with an ASTEC UM1381 Video Modulator or any FCC approved Video Modulator with the same pinout and signal configuration. The pin assignments are as follows:-

Pin No.	Description
1	12V DC Supply
2	Video Shield Ground (0 V)
3	Audio Out (1.0 V_{p-p}, AC-coupled)
4	Video Out (0.8 V_{p-p}, AC-coupled)
5	Not used

Floppy Disk Drive Connector [J12]:

The pin assignments for the connectors for the internal and optional expansion floppy disk drive are as follows:-

Pin No.	Signal Name	Pin No.	Signal Name
2	Not used.	4	Not used.
6	Not used.	8	INDEX/
10	DR1/	12	DR2/
14	Not used.	16	MOTOREN/
18	DIR/	20	STEP/
22	WD	24	WG/
26	TRK00/	28	WPRT/
30	RD	32	SS/
34	Not used.	36	Not used.
38	Not used.	40	Not used.

All odd numbered pins are grounded except pins 35, 37 and 39 which are not used.

Hard Disk Interface Connector [J10]:

The pin assignments for the hard disk interface connector are as follows:-

Pin No.	Signal Name	Pin No.	Signal Name
1	HDAL0	3	HDAL1
5	HDAL2	7	HDAL3
9	HDAL4	11	HDAL5
13	HDAL6	15	HDAL7
17	ABO	19	AB1
21	AB2	23	CS6/
25	IOWR'/	27	IORD'/
29	WAIT'/	31	HDRES'/
33	Not used.	35	HINTRQ'
37	HDRQ'	39	Not used.

All even numbered pins are grounded.

Parallel Output (Printer) Port [J3]:

This is a 15-pin female DB-type jack. The pin assignments are as follows:-

Pin No.	Signal Name	Pin No.	Signal Name
1	DATA1	2	DATA2
3	DATA3	4	DATA4
5	DATA5	6	DATA6
7	DSTR/	8	PRBUSY
9	DATA7	10	DATA8
11	GROUND	12	GROUND
13	GROUND	14	GROUND
15	GROUND		

Speaker [J6]:

The speaker connections are defined as follows:

Pin No.	Name	Description
1	+5V	To be connected to one side of the speaker
2	SPK	Audio output. To be connected to the other side of the speaker

Expansion Card Connectors [J7,J8]:

Two connectors are provided on the board for interfacing to the optional expansion cards. The pin assignments for connector [J7] are as follows :-

Pin No.	Signal Name	Pin No.	Signal Name
1	AB0	2	AB1
3	AB2	4	Ground
5	Ground	6	+5V
7	CS5/	8	RESET/
9	CLK	10	INT1/
11	AUDIO	12	DB7
13	DB6	14	DB5
15	DB4	16	DB3
17	DB2	18	DB1
19	DB0	20	+5V
21	Ground	22	Ground
23	IOWR'/	24	IORD'/
25	WAIT/	26	CS7/
27	+12V	28	-12V

The pin assignments for connector [J8] are as follows:-

Pin No.	Signal Name	Pin No.	Signal Name
1	AB0	2	AB1
3	AB2	4	Ground
5	Ground	6	+5V
7	CS4/	8	RESET/
9	CLK	10	INT2/
11	AUDIO	12	DB7
13	DB6	14	DB5
15	DB4	16	DB3
17	DB2	18	DB1
19	DB0	20	+5V
21	Ground	22	Ground

Pin No.	Signal Name	Pin No.	Signal Name
23	IOWR'/	24	IORD'/
25	WAIT/	26	CS7/
27	+12V	28	-12V

Expansion Bus Edge Connector [J1]:

An edge connector is provided which produces a subset of the STD bus signals and can be used for system expansion. The pin assignments are as follows:-

Pin No.	Signal Name	Pin No.	Signal Name
1	+5V DC	2	+5V DC
3	Ground	4	Ground
5	Not used	6	Not used
7	DB3	8	DB7
9	DB2	10	DB6
11	DB1	12	DB5
13	DB0	14	DB4
15	AB7	16	Not used
17	AB6	18	Not used
19	AB5	20	Not used
21	AB4	22	Not used
23	AB3	24	Not used
25	AB2	26	Not used
27	AB1	28	Not used
29	AB0	30	Not used
31	WR'/	32	RD'/
33	IORQ'/	34	MREQ/
35	AUDIO	36	CS7/
37	Not used	38	Not used
39	Not used	40	Not used
41	BUSAK/	42	BUSRQ/
43	INTAK/	44	INT0/
45	WAIT/	46	NMI/
47	RESET/	48	Not used
49	CLK	50	Not used
51	Not used	52	Not used
53	Ground	54	Ground
55	+12V DC	56	-12V DC

DC Power Connector [J9]:

This is a 4 pin male connector which joins with the DC power cable coming from the internal switching power supply. It provides all the DC power for the main circuit board and any expansion cards attached to board.

The pin assignments are as follows :-

Pin No.	Wire Color	Description
1	Green	Common Electrical Ground
2	Red	+5V
3	Yellow	+12V
4	Blue	-12V

3.2 ROM Selection

The PIED PIPER requires 32 Kbits of read-only memory containing the Boot Utility Program. This ROM must be present in the system from address 0000H to 0FFFH on startup or after a system reset. In order to provide a full 64 Kbyte RAM addressing capability for the system, the memory address space from 0000H to 7FFFH is shared by the ROM and RAM. However, only one is activated at any given time. After a system reset, the ROM is enabled. However, the system CONTROL REGISTER II can be used to enable or disable the ROM under software control. The RAM in the address space from 8000H to FFFFH is independent of the contents of CONTROL REGISTER II. This RAM is always present in the system, whether the ROM is enabled or not.

The circuit is designed to accomodate ROM of up to 128 Kbits in size, which will then occupy memory adddress space from 0000H to 3FFFH. The system is shipped with a 2732-type EPROM containing the PIED PIPER BOOT UTILITY PROGRAM. To use a 2764-type (64 Kbit) EPROM, a jumper must be installed from JU to JU2. To use a 27128-type (128 Kbit) EPROM, a jumper must be installed from JU to JU1 instead. Only one jumper should be installed. The EPROM should have an access time of 450 nsec. or less.

ROM SOCKET PINOUT

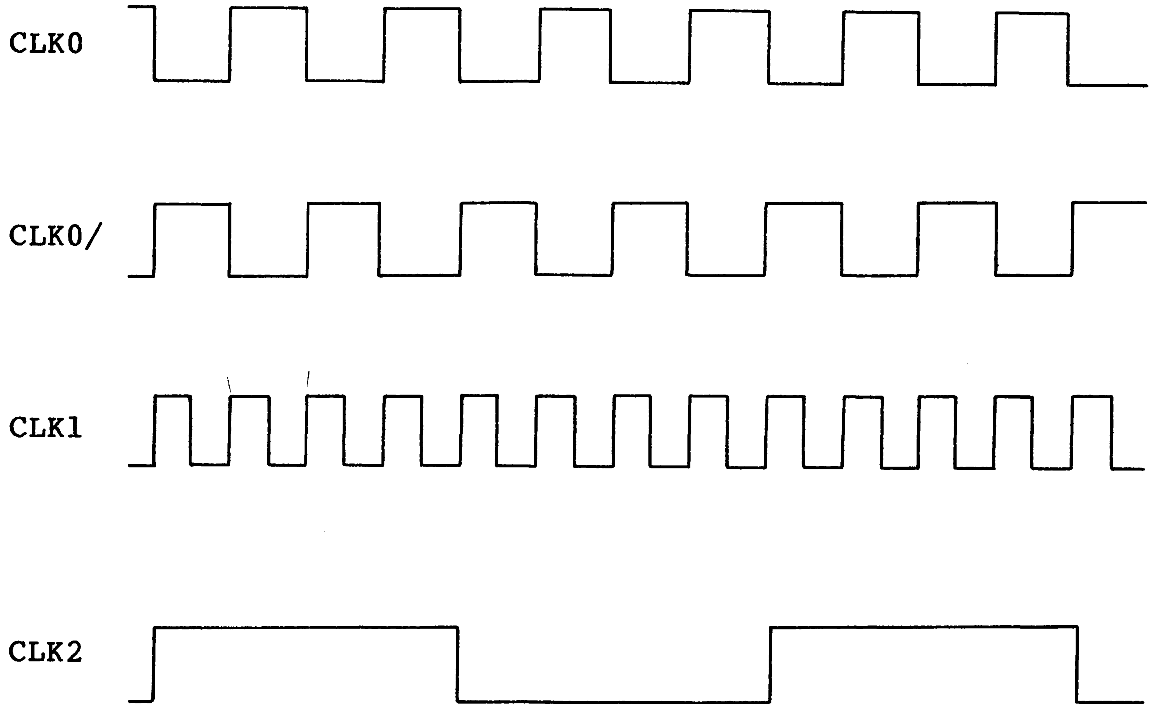
```
           -------------
          |             |
+5V       |1          28| +5V
A12       |2 ------   27| +5V              *JU2 +5V
A07       |3          26| ----------*JU
A06       |4          25| A08              *JU1 A13
A05       |5          24| A09
A04       |6          23| A11
A03       |7          22| OE/
A02       |8          21| A10
A01       |9          20| CE/
A00       |10         19| D07
D00       |11         18| D06
D01       |12         17| D05
D02       |13         16| D04
GND       |14         15| D03
          |_____________|
```

3.3 Clocks/Timing

The 4 MHz microprocessor clock is derived from the clock generator circuit which uses an 8.000 MHz crystal. This system clock is scaled down with a counter [U70] to provide the 1 MHz clock for the peripheral controllers. The clock labels are defined as follows:-

LABEL	DEFINITON
CLK0	System Clock (4.000 MHz)
CLK0/	Complement of CLK0 (4.000 MHz)
CLK1	(8.000 MHz)
CLK2	Keyboard Controller Clock and Floppy Disk Drive Controller Clock (1.000 MHz)

The phase relationship of these clock signals is defined in the following timing diagrams:-



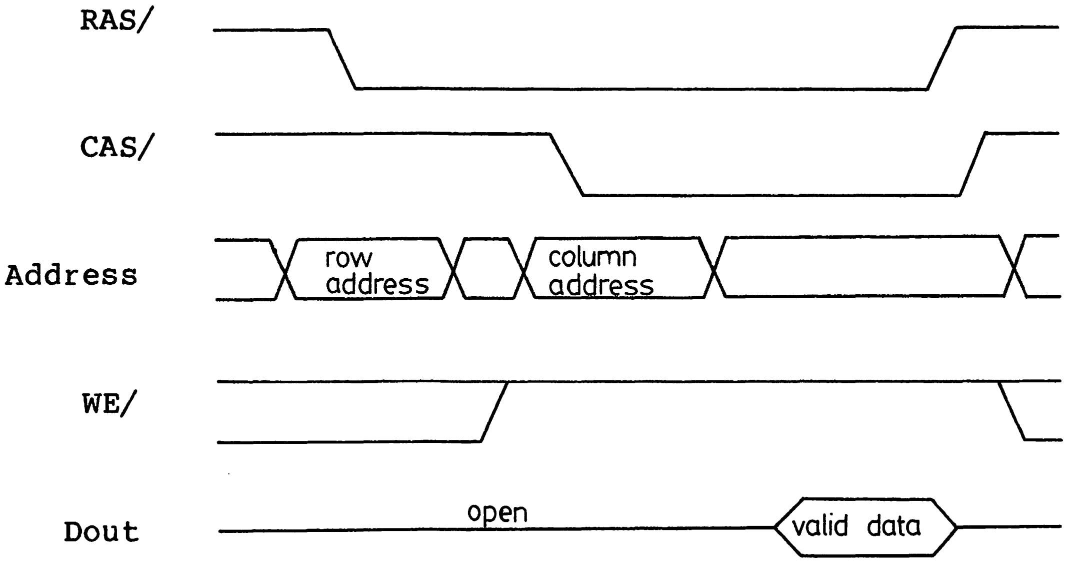
The microprocessor has a 16-bit address bus and an 8-bit data bus. The low order address bus lines and the data bus lines DB0-DB7 are buffered. The BUSRQ/, HALT/, NMI/, INT/, and WAIT/ are held high by 1 KOhm resistors to +5V. I/O write and read signals are decoded by logic gates using signals IORQ/, WR/, and RD/ from the CPU.

The PIED PIPER uses eight 64K x 1 bit Dynamic RAM's to provide 64 Kbytes of user read/write memory. Two multiplexors [U46, U47] use the status of the Row Address Strobe (RAS/) and Column Address Strobe (CAS/) signals to encode the low and high address bytes and supply them to the DRAM's. The data lines are directly tied to the system data bus and the data read/write mode is selected by the write enable line (WE/). A logic high on WE/ selects the read mode and a logic low selects the write mode.

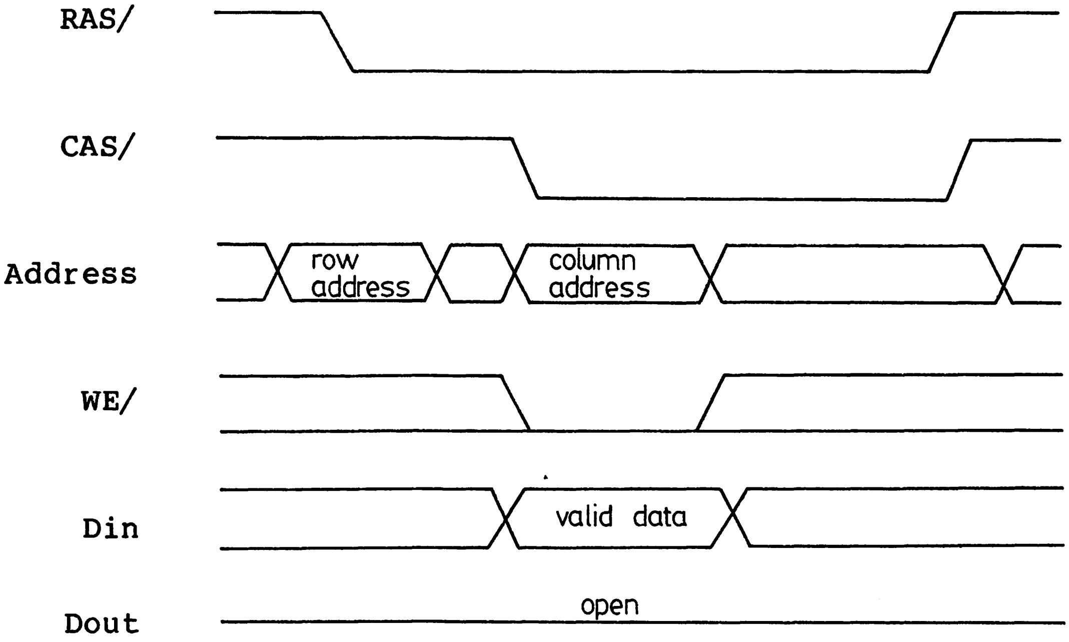
The DRAM's are automatically refreshed during instruction fetch cycles. The CAS/ line is set high when the refresh signal line (RFSH/) is low to avoid any data output during refresh. When RFSH/ and MREQ/ are low, the RAS/ line uses the lower system address byte as a refresh address and causes all bits in each row to be refreshed.

The timing waveforms for memory read, write, and refresh are as follows:-

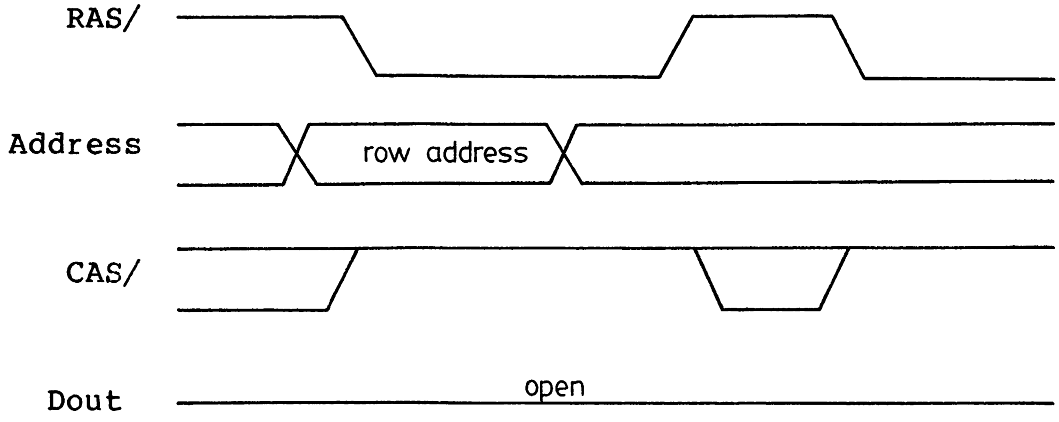
Read Cycle



Write Cycle



RAS/- Only Refresh Cycle



3.4 Keyboard Controller

The keyboard controller uses the Intel 8279 Programmable Keyboard Controller. The controller is mounted on the main printed circuit board and interfaces with the keyboard via the connecting cable attached to connector J13.

The controller rapidly scans through the column lines CL0-CL7 of the keyboard matrix. As each column is enabled, the return lines RL0-RL7 are sensed to determine if any key in that column is closed. If a key closure is detected, then a debounce circuit is activated to check if it is a proper key switch depression. If the closure is shorter than 10 msec, then it is regarded as a bounce and the controller looks for another key closure. Otherwise, it is taken as a proper key depression and the key position is returned together with the status of the CONTROL and SHIFT lines and stored in the controller's character buffer.

When a key closure is detected which lasts for more than 1 second, the keyboard is disabled by resetting the KBREL line and then re-enabled again to check for a key depression. If a key closure is still detected and the key value is the same as that previously stored in the controller's character buffer, then the key is assumed to be in the auto repeat mode. The KBREL line is disabled and re-enabled every 0.05 seconds to generate a multiple key closure effect. This process is repeated until the key is released. If no key, or a different key closure, is detected at any time after the KBREL line is re-enabled, then the controller returns to its normal keyboard scan cycle.

A 24 pin male connector is used to connect the main printed circuit board to the keyboard assembly. The signal descriptions for the connector are as follows :-

Signal Name	Signal flow	Functional description
CL0-CL7	Output	Column scan lines which are used to scan for key switch closure. SL7 is the most significant column number.
RL0-RL7	Input	Return line inputs. Each These line should be pulled high unless a switch closure in the row pulls it low. RL7 is the most significant row number.
CNTL/	Input	This line should be low when either the "CTRL" or "FUNCT" key is depressed.
SHIFT/	Input	This line should be low when either the "SHIFT" or "FUNCT" key is depressed.

KEY DEPRESSION	CTRL/	SHIFT/
FUNCT	Low	Low
CTRL	Low	High
SHIFT	High	Low
NIL	High	High

CAPLK/	Input	This line should be low when the capital lock key "CAPS LOCK" is depressed.
CO0/-CO1/	Output	Drive select indicators. CO0/ is low when drive 1 is selected. CO1/ is low when drive 2 is selected.
SPK	Output	Audio signal Output to speaker mounted on the keyboard PCB.

3.5 Video Controller

The Video Display Controller consists of a Signetics 2672 Programmable Video Timing Controller (PVTC), 2 Kbytes of display buffer memory, a display character generator ROM, and video and attribute control circuitry. The display buffer does not occupy any of the main processors address space but rather is controlled directly by the PVTC. The display buffer is made up of four 1024 x 4 bit static RAMs, giving a total capacity of 2 Kbytes, which is sufficient to store one full display screen. To store data in the display buffer, or read data from it, the main microprocessor makes use of one-byte read and write buffers to store the data. Commands are then issued to the PVTC to execute the desired data transfer using the appropriate buffer.

The PVTC derives its timing from an external Character Clock Generator which uses a 13.000 MHz crystal as its time base and generates all the display timing including scan line per character row, video dot timing, composite sync and other control signals necessary to display characters on the video monitor. It also provides consecutive addressing to the display buffer memory and controls the CPU-display buffer interface.

The PVTC contains 8 internal registers which control its operation and can be accessed by the CPU with input/output instructons. These registers allow the PVTC to be programmed for different display formats, and to execute commands. The status of the display can also be read from these registers. Transfer of data between the CPU and the display memory is accomplished via the read and write display buffers. Each buffer appears as a single input/output port to the CPU. To write data to the display memory, the data is first loaded by the CPU into the write buffer. The CPU then outputs the desired cursor or pointer address where the data is to be stored in the cursor or pointer register of the PVTC. The CPU then issues a write command to the PVTC using its command register. The PVTC then retrieves the data from the write buffer and generates the required control signals to store the data at the correct address in the display memory. To read data from the display memory, the CPU first loads the cursor or pointer register with the desired address. The CPU then issues a read command to the PVTC via its command register. The PVTC then generates the appropriate control signals to take the data from the given address in display memory and place it in the read buffer. The CPU can then retrieve the data from the read buffer. The status register of the PVTC must be polled in both cases to ensure that the PVTC can accept a new command and to sense when the data transfer has actually occurred. The PVTC does not actually write any new data to the display memory until the next display blanking interval in order to avoid any visual disturbances (flashing) on the video screen.

The PVTC can be programmed for a variety of display formats and timing relationships. Two standard setups are provided with the system software to allow suitable displays for either a video monitor or a standard television set with RF modulator. The characteristics for the Monitor and Television modes are summarizd as follows :-

	Monitor	**Television**
Scan Lines per screen	216	216
No. of Rows per Screen	24	24
No. of Characters per Row	80	40
Character Clock Frequency	13.0 MHz	6.5 MHz
Character Width in dots	8	7

The character clock frequency and character width are controlled by the signal lines 40COL and DIV7-8/ respectively.

The dot pattern for the displayable characters is contained in the 2 Kbyte display character generator ROM. The display memory stores the ROM addresses of the characters to be displayed. The character generator ROM outputs the corresponding dot patterns for the characters to the video shift register. The shift register then shifts the dot pattern out to form the video signal. All timing for the video shift register is controlled by the Character Generator Clock, which also drives the PVTC. The PVTC takes care of all timing and display memory address generation to ensure that the next dot pattern is accessed properly. The PVTC also ensures that the columns and rows of the display are generated in the proper order.

The video attribute circuitry can produce dual-intensity, reverse video and black-on-white video effects on the screen depending on the signals HIL, REV and BOW, respectively. Attribute bit CC7, obtained from the display memory along with the ASCII character code, can be used to select either the high intensity or reverse video attribute on a charcter by character basis. The dot pattern shifted out of the video shift register passes through the attribute logic to produce the video output signal.

The composite sync signal generated by the PVTC is combined with the video signal to produce an output which conforms to the EIA RS170 Standard. This signal appears at both Composite Video and RF connectors.

3.6 Floppy Disk Controller

The PIED PIPER's Floppy Disk Drive Controller is built around the Western Digital FD1793 Floppy Disk Formatter/Controller which is configured for 5 1/4" Mini Floppy Disk Drives in double density format. The controller performs all the functions necessary to read and write data to the drive. For the Disk Read operation, data from the disk in Modified-Frequency-Modulated (MFM) format is fed into the Data Separator circuit, made up of a FDC 9216, to retrieve the RAW READ data and the READ CLOCK signals. The serial data is then formed up into words and transferred to the CPU via the Data Bus Lines. The read operation continues until the end of the sector is reached and the Interrupt request line is set.

For the Disk Write operation, the Write Gate is enabled. Write Data in the form of a series of pulses in MFM format is output to the drive. Write Precompensation is performed digitally by the shift register 74LS195 depending on the states of the Write Data, EARLY and LATE signals. Writing to the disk is inhibited when the Write Protect input is at a logical low, in which case any Write Command is immediately terminated.

Connector J12 is a 40 pin male connector for hook up to 5 1/4" mini floppy disk drives. It consists of all the signals required for disk read/write data transfer, motor stepping and step direction, drive status and drive selection.

The signal descriptions are as follows :-

Signal Name	Signal flow	Functional Description
DR1/	Ouptut	Enables Drive A.
DR2/	Output	Enables Drive B.
MOTOREN/	Output	Enables the drive motor.
DIR/	Output	Controls the direction of Read/Write head movement. Low indicates movement away from the centre of the drive and high indicates movement towards the centre of the drive.
STEP/	Output	Steps the read/write head by one track for each step pulse output. The direction is specified by DIR/.

Signal Name	Signal flow	Functional Description
SS/	Output	Side Select. It is low when side 1 of the diskette is selected and high when side 0 is selected.
WD	Output	Writes data to the diskette in MFM format.
WG/	Output	Write Gate Enable. It must be turned on when writing is to be performed on the diskette.
RD	Input	Reads data from the diskette.
Index/	Input	Index Hole Detect. This line is low when the index hole is encountered on the diskette.
TRK00/	Input	Track Zero Indicator. This line is low when the drive head is positioned at track zero and high when it is away from track zero.
WPRT/	Input	Diskette Write Protect. This line is low when the diskette is write protected.

3.7 Hard Disk Interface

This is a 40 pin male connector which is configured to hook up to Western Digital's WD1000 Series Winchester Hard Disk Controller. It consists of an eight bit bi-directional data bus, three bit address bus and seven control lines. All commands, status and data are transferred over this bus. The signal descriptions are as follows :-

Signal Name	Signal flow	Functional Description
HDAL0-HDAL7	Bi-directional	Data Bus Lines. These eight bi-directional data lines transmit and receive data to and from the hard disk controller. HDAL7 is the most significant bit.
AB0-AB2	Output	Address Bus Lines. These three bit address lines are used to select one of the eight registers in the hard disk controller. AB2 is the most significant bit.
CS6/	Output	I/O Select. This line is activated when data is to be read from or written to the hard disk controller.
IOWR'/	Output	Write Command. It indicates that data on the data bus lines is to be accepted by the hard disk controller and put into the registers specified by the address lines.
IORD'/	Output	Read Command. It indicates that the contents of the register whose address is specified by the address lines are to be placed onto the data lines.
WAIT'/	Input	This line should be low when data bus lines are not valid on a read command or when data has not been accepted on a write command.
HINTRQ'	Input	This line should be high whenever the hard disk controller has completed the read or write command.

Signal Name	Signal flow	Functional Description
HDRQ'	Input	This line should be high whenever the sector buffer of the hard disk controller contains data to be read from it, or is waiting for data to be loaded into it. It should be reset whenever the Data Register is read from or written to. The toggling should continue until the buffer is empty.
HDRES'/	Output	Hard Disk Reset. This line is used to reset the hard disk to its initial state.

3.8 Parallel Output (Printer) Port

This is a 15 pin D-type female connector which can be used to attach any Centronics compatible printer. It consists of eight data lines and two control lines for printer handshaking. The signal descriptions are as follows:-

Signal Name	Signal Flow	Description
DATA1-DATA8	Output	Data Lines. These eight data lines are used to transmit data to the printer. DATA8 is the most significant bit.
DSTR/	Output	Data Strobe. This line is set to a low level by system software when the data lines contain a character to be printed. It is returned high after a short delay.
PRBUSY	Input	This line should be high when the printer is busy or not ready to receive data from the printer port.

3.9 Speaker

The PIED PIPER's internal speaker is driven by a Darlington amplifier circuit which delivers about 0.5 watt into an 8 Ohm load. The speaker connector [J6] is a 2 pin connector. The Darlington amplifier gets its signal from bit 7 of the system CONTROL REGISTER II. To produce a tone from the speaker, this bit must be repetitively set and reset at a rate which determines the frequency of the tone. A program example for generating a 1 kHz tone is given in Section 4.8.

3.10 Expansion Board Interface

There are two 28 pin single row male connectors [J7 & J8] on the board which are used to interface with the expansion card options. They may also be used to interface with user designed I/O devices, provided such devices do not present a safety hazard and meet the Class B FCC requirements.

The signal descriptions and Pin Assignments for Connector [J7] are as follows :-

Pin No.	Signal Name	Signal Flow	Description
1	AB0	Ouptut	Address line 0
2	AB1	Output	Address line 1
3	AB2	Output	Address line 2
4	Ground		Signal Ground
5	Ground		Signal Ground
6	+5V	Output	+5V DC
7	CS5/	Output	I/O Select
8	RESET/	Output	System Reset
9	CLK	Output	System Clock
10	INT1/	Input	Interrupt Request
11	AUDIO	Output	Audio output to RF modulator.
12	DB7	Bi-directional	Data line 7
13	DB6	Bi-directional	Data line 6
14	DB5	Bi-directional	Data line 5
15	DB4	Bi-directional	Data line 4
16	DB3	Bi-directional	Data line 3
17	DB2	Bi-directional	Data line 2
18	DB1	Bi-directional	Data line 1
19	DB0	Bi-directional	Data line 0
20	+5V	Output	+5V DC
21	Ground		Signal Ground
22	Ground		Signal Ground

Pin No.	Signal Name	Signal Flow	Description
23	IOWR'/	Output	I/O write
24	IORD'/	Output	I/O read
25	WAIT/	Input	Wait Request
26	CS7/	Output	I/O select
27	+12V	Output	+12V DC
28	-12V	Output	-12V DC

Signal descriptions and Pin Assignments for Bus Connector [J8] are as follows:-

Pin No.	Signal Name	Signal Flow	Description
1	AB0	Ouptut	Address line 0
2	AB1	Output	Address line 1
3	AB2	Output	Address line 2
4	Ground		Signal Ground
5	Ground		Signal Ground
6	+5V	Output	+5V DC
7	CS4/	Output	I/O Select
8	RESET/	Output	System Reset
9	CLK	Output	System Clock
10	INT2/	Input	Interrupt Request
11	AUDIO	Output	Audio output to RF modulator.
12	DB7	Bi-directional	Data line 7
13	DB6	Bi-directional	Data line 6
14	DB5	Bi-directional	Data line 5
15	DB4	Bi-directional	Data line 4
16	DB3	Bi-directional	Data line 3
17	DB2	Bi-directional	Data line 2
18	DB1	Bi-directional	Data line 1
19	DB0	Bi-directional	Data line 0
20	+5V	Output	+5V DC
21	Ground		Signal Ground
22	Ground		Signal Ground
23	IOWR'/	Output	I/O write
24	IORD'/	Output	I/O read
25	WAIT/	Input	Wait Request
26	CS7/	Output	I/O select
27	+12V	Output	+12V DC
28	-12V	Output	-12V DC

3.11 Expansion Bus Interface

The PIED PIPER has a 56 pin card edge connector [J1] which can be used to interconnect with external peripherals or I/O expansion cards. The interface contains a subset of the STD bus signals and is intended to be used with an STD bus card cage expansion module. Normally, only I/O port expansion is possible. Expansion of this type should be done with care so as not to exceed the power supply capabilities or interfere with the operation of the main PIED PIPER circuitry.

The PIED PIPER utilizes only the first 64 I/O port addresses from 00H to 3FH for its internal registers, I/O ports and peripheral controllers. The I/O addresses are decoded with a 74LS138 decoder. Each decoded line (CS0/-CS7/) represents a group of eight I/O addresses. Each line must be combined with other control lines to obtain individual I/O address enable lines for specific functions. Users who want to expand the I/O address lines through the Expansion Bus should use addresses from 40H to FFH by decoding the lower eight bit address lines provided by the BUS Connector. I/O Addresses from 00H to 3FH should not be used.

The Expansion BUS organization consists of a power bus, a Data Bus and a Control Bus. The signals are as follows :-

Signal Name	Signal Flow	Description
DB0-DB7	Bi-directional	Data Bus lines.
AB0-AB7	Output	Address Bus Lines.
WR'/	Output	Write to memory or I/O.
RD'/	Output	Read from memory or I/O.
MREQ/	Output	Memory select.
RESET/	Output	System Reset.
INT0/	Input	Interrupt Request
INTAK/	Output	Interrupt Acknowledge.
NMI/	Input	Non-Maskable Interrupt.
WAIT/	Input	Wait Request.
AUDIO	Input	Source for audio signal output to RF modulator.
BUSRQ/	Input	Bus Request.

Signal Name	Signal Flow	Description
BUSAK/	Output	Bus Acknowledge.
IORQ'/	Output	I/O Request.
CS7/	Output	I/O Select. Also used by Peripheral Card Connector J7 and J8.
CLK	Output	Clock from processor.

3.12 Floppy Disk Drive

The floppy disk drive is a Mitsubishi model M4853 double-sided, double bit and double track density, half-height unit using standard double density, 96TPI 5.25 in. diskettes. It uses a circular gimbal spring in the read/write head suspension mechanism to improve medium tracking performance. The steel band drive system for positioning achieves an inter-track access time of just 3 msec. A maintenance-free, DC, brushless, direct-drive motor is employed to eliminate the drive belt of other units. The unit provides a storage capacity of up to 1000 Kbytes unformatted, or 800 Kbytes formatted.

The performance features of the unit are summarized as follows:

Transfer Rate	250 Kbits/sec
Avg. Latency Time	100 msec
Access Time	
Track to Track	3 msec
Average	94 msec
Settling Time	15 msec
Head Load Time	50 msec
Motor Start Time	250 msec
Recording Density	5922 bits/in.
Encoding Method	MFM
Track Density	96 tracks/in.
Number of Cylinders	80
Number of Tracks	160
Number of Heads	2
Rotation Speed	300 RPM
MTBF	10,000 POH or more
MTTR	30 min.
Error Rate	
Soft Read Error	10^{-9} bit
Hard Read Error	10^{-12} bit
Seek Error	10^{-6} seek

DC Power Requirements	
+5 V	0.5 A typical
+12 V	0.7 A typical (seek)

3.13 Power Supply

The switching power supply is a Sanyo model MC-040BL. This is a triple output supply with a 72 % conversion efficiency. The outputs are rated at +5 V at 3 A, +12 V at 2 A, and -12 V at 0.5 A. All outputs have foldback overcurrent protection. The input AC requirements are 85-132 VAC at 55 +/-10 Hz.

The total current requirements of the standard PIED PIPER are 1.5 A at +5 V, 5 mA at +12 V, and 0 mA at - 12 V. Before adding any user-designed expansion boards to the system which use the excess capacity of this supply, the user should total up the current requirements of the PIED PIPER and any expansion boards or peripherals.

The power supply is protected on the AC line side by a 3.15 A fuse. The rating of this fuse should not be changed under any circumstances.

CHAPTER 4 SOFTWARE

This Chapter describes how the software interacts with the PIED PIPER hardware. The computer uses three internal control/status registers to provide program interaction with the peripherals. In addition, each of the controller chips associated with the peripherals contains internal registers which must be programmed for proper operation. The function of each of these registers will be explained in the following sections, along with some programming examples.

4.1 System Control/Status Registers

There are two system control registers (CONTROL REGISTER I and CONTROL REGISTER II) and one system status register (STATUS REGISTER). The control registers are write-only, and the status register is read-only. It is therefore necessary to keep a record of the current contents of the control registers in memory. Every time a control register is to be modified, its contents must first be obtained from the associated memory location, the appropriate bits modified, the memory location updated, and finally the new value written to the control register. The programming examples in the following sections will reflect this approach

The functions provided by the control registers include:

- floppy disk drive selection
- disk drive read/write head/side selection
- output printer port data strobe
- interrupt enable
- keyboard scan enable/disable
- video display mode selection
- ROM enable/disable
- implementation of bell

The information provided by the status register includes:

- interrupt status
- capital lock key status
- output printer port ready status
- floppy disk drive index hole sense
- keyboard scan reference

The addresses asigned to the system control/status registers are as follows:

CONTROL REGISTER I:	**18H** - Write-only
CONTROL REGISTER II:	**1DH** - Write-only
STATUS REGISTER:	**18H** - Read-only

The current contents of CONTROL REGISTER I are saved in memory location **FFE2H**; that of CONTROL REGISTER II are saved in memory location **FFE0H**.

4.1.1 CONTROL REGISTER I

The bits of CONTROL REGISTER I are defined as follows:

```
-------------------------
|D7|D6|D5|D4|D3|D2|D1|D0|
-------------------------
  |  |  |  |  |  |  |  |
  |  |  |  |  |  |  |  |-> Floppy Disk Drive A Select
  |  |  |  |  |  |  |
  |  |  |  |  |  |  |----> Floppy Disk Drive B Select
  |  |  |  |  |  |
  |  |  |  |  |  |-------> Floppy Disk Side Select
  |  |  |  |  |
  |  |  |  |  |----------> Output Printer Port Data Strobe
  |  |  |  |
  |  |  |  |-------------> Keyboard Interrupt Enable
  |  |  |
  |  |  |----------------> Timer Interrupt Enable
  |  |
  |  |-------------------> Hard Disk Interrupt Enable
  |
  |----------------------> Keyboard Scan Disable
```

Drive A Select:
A "1" level in bit D0 will select floppy disk drive A as the active drive. A "0" level will deselect drive A. Bits D0 and D1 cannot both be "1" simultaneously.

Drive B Select:
A "1" level in bit D1 will select floppy disk drive B as the active drive. A "0" level will deselect drive B. Bits D0 and D1 cannot both be "1" simultaneously.

Floppy Disk Side Select:
If bit D2 is a "0" level, then side 0 of the floppy disk drive is selected. A "1" value selects side 1.

Output Printer Port Data Strobe (DSTR):
This bit supplies the data strobe signal (DSTR/) to the output printer port [pin number 7 of connector J3]. This bit should be set to a "1" level after data has been written to the output port, and then returned to a "0" level after a suitable delay. See Section 4.7 for details on the printer port. (Bit D3 is an inverted version of the actual signal sent to the printer)

Keyboard Interrupt Enable:
If bit D4 is a "1" level , then the keyboard controller interrupt is enabled. An interrupt signal is generated whenever there is data in the keyboard controller FIFO RAM. The interrupt signal is removed every time data is read from this FIFO, but will return high if there is still data in the FIFO. A "0" level disables keyboard controller interrupts, and the only way of sensing the presence of characters in the FIFO is to poll the system STATUS REGISTER or the keyboard controller status register.

Timer Interrupt Enable:
The keyboard controller contains a programmable timer. This timer generates an interrupt signal every 10.24 msec. If bit D5 is a "1" value, this timer interrupt is enabled. A "0" value disables the timer interrupt. Operation of the timer is described in Section 4.2.

Hard Disk Interface Enable:
If bit D6 is a "1" value, then the hard disk interface interrupt is enabled. A "0" value disables the interrupt signal.

Keyboard Scan Disable:
If bit D7 is a "1" value, then keyboard scanning is disabled. A "0" value enables keyboard scanning to continue. This signal is used to implement the "auto-repeat" feature for the keyboard.

Initialization:

After system initialization, the value contained in CONTROL REGISTER I is:

D7	D6	D5	D4	D3	D2	D1	D0
0	**0**	**1**	**0**	**0**	**0**	**0**	**1**

Programming Example:

The following program demonstrates how the contents of a control register can be altered. In this case, it is desired to enable the timer interrupt.

```
LD   A,(0FFE2H)       ; GET CURRENT VALUE
SET  5,A              ; SET TIMER ENABLE
LD   (0FFE2H),A       ; SAVE CHANGED VALUE
OUT  18H,A            ; ENABLE TIMER
```

4.1.2 CONTROL REGISTER II

The bits of CONTROL REGISTER II are defined as follows:

```
-------------------------
|D7|D6|D5|D4|D3|D2|D1|D0|
-------------------------
  |  |  |  |  |  |  |  |
  |  |  |  |  |  |  |  |-> Line Length Select
  |  |  |  |  |  |  |
  |  |  |  |  |  |  |----> Reverse Video Select
  |  |  |  |  |  |
  |  |  |  |  |  |-------> High Intensity Select
  |  |  |  |  |
  |  |  |  |  |----------> Not Used (must be 0)
  |  |  |  |
  |  |  |  |-------------> ROM Disable
  |  |  |
  |  |  |----------------> Black-on-White Select
  |  |
  |  |-------------------> Character Size Select
  |
  |----------------------> Speaker Strobe
```

Line Length Select:

If bit D0 is a "1" value, then a 40 column line length is selected for the display. This is required if the RF modulator and standard television is used. A "0" value selects an 80 column line length for use with a video monitor.

Reverse Video Select:

If bit D1 is a "1" value, then the reverse video attribute is selected for the display. In this mode, each character can appear as black dots in a white character block, or in the normal mode of white dots in a black character block. If bit D1 is a "0" value, this display attribute is disabled. Note that only one of bits D1 or D2 can be set to "1" at the same time.

High Intensity Select:
If bit D2 is a "1" value, then the high intensity attribute is selected for the display. In this mode, characters can appear in either normal or high intensity. A "0" value disables this display attribute. Note that only one of bits D1 or D2 can be set to "1" at the same time.

ROM Disable:
If bit D4 is a "1" value, then the system EPROM is disabled (does not exist in processor memory space). If bit D4 is a "0" value, then the lower 32 Kbytes of system RAM are disabled and the system EPROM is enabled and occupies system memory space starting at address 0000H. Note that the EPROM is actually not dsiabled/enabled until the next time the STATUS REGISTER is read after changing bit D4.

Black-on-White Select:
If bit D5 is a "1" value, then the display is changed to produce black characters on a white background. This format applies to the entire display, and is not a character attribute like reverse video. If bit D5 is a "0" value, then a normal display of white characters on a black background is produced.

Character Size Select:
If bit D6 is a "1" value, then the character block size is selected to be 7 dots wide for the display. If bit D6 is a "0" value, then the character block size will be 8 dots wide.

Speaker Strobe:
Bit D7 produces the signal which drives the internal speaker line. This bit should be alternately set to "1" and "0" levels to produce a continuous tone from the speaker. The pitch of the tone is determined by the frequency with which the bit is being changed. Note that since this technique drives the speaker with a square wave, as opposed to a sinewave, the emitted tone will not be pure but will contain many harmonics.

Initialization:

After system initialization, the contents of CONTROL REGISTER II are as follows:

D7	D6	D5	D4	D3	D2	D1	D0
0	**1**	**0**	**1**	**1**	**1**	**0**	**0**

Programming Example:

The system EPROM can be disabled or enabled by reading the STATUS REGISTER after modifying bit D4 of CONTROL REGISTER II. This capability is useful for OEM users who would like to customize the PIED PIPER for specialized applications by placing their own software routines in EPROM.

To disable the EPROM, bit 4 of CONTROL REGISTER II must be set. The next time the STATUS REGISTER is read, the ROM will be disabled. To enable the EPROM after it has been disabled, bit 4 of CONTROL REGISTER II must be reset, and the STATUS REGISTER must be read. The following programs illustrate how to enable/disable the system EPROM.

Instructions to disable the EPROM:

```
LD   A,(0FFE0H)      ; GET CURRENT MODE
SET  4,A             ; SET TO DISABLE ROM
LD   (0FFE0H),A
OUT  1DH,A
IN   A,18            ; DISABLE ROM
```

Instructions to enable the EPROM:

```
LD   A,(0FFE0H)      ; GET CURRENT MODE
RES  4,A             ; SET TO ENABLE ROM
LD   (0FFE0H),A
OUT  1DH,A
IN   A,18            ; ENABLE ROM
```

4.1.3 STATUS REGISTER

The bits of the STATUS REGISTER are defined as follows:

```
-------------------------
|D7|D6|D5|D4|D3|D2|D1|D0|
-------------------------
  |  |  |  |  |  |  |  |
  |  |  |  |  |  |  |  |---> Interrupt Pending
  |  |  |  |  |  |  |
  |  |  |  |  |  |  |------> Interrupt
  |  |  |  |  |  |--------->
  |  |  |  |  |------------> Source
  |  |  |  |
  |  |  |  |---------------> Capital Lock Key Status
  |  |  |
  |  |  |------------------> Output Printer Port Busy
  |  |
  |  |---------------------> Floppy Disk Index Hole Sense
  |
  |------------------------> Keyboard Scan Status
```

Interrupt Pending:
If bit D0 is a "1" level, then one of the system interrupts (given by the contents of bits D1-D3) is pending. Note that this signal will occur even if the interrupt producing it is not enabled. If bit D0 is a "0" value, then no system interrupts are pending.

Interrupt Source:
Bits D1, D2, and D3 are used to form up a three-bit address which indicates the highest priority interrupt which is pending. The following list gives the address assignments for the interrupts, in order from highest to lowest priority:

D3	D2	D1	Source
0	0	0	Disk Controller Data Request (DRQ)
0	0	1	Disk Controller Interrupt Request (INTRQ)
0	1	0	Video Controller Interrupt
0	1	1	Keyboard Controller Interrupt
1	0	0	Timer Interrupt
1	0	1	Expansion Connector J8 Interrupt
1	1	0	Expansion Connector J7 Interrupt
1	1	1	Expansion Bus J1 Interrupt

Capital Lock Key Status:
The "Capital Lock" is the only key which does not interface directly with the keyboard controller. Bit D5 will be reset to a "0" value whenever the "Capital Lock" key is closed. Otherwise, bit D5 will be a "1" value. If system software detects closure of this key by reading the

STATUS REGISTER, then any letter code read from the keyboard controller will be converted to upper case.

Output Printer Port Busy (PRBUSY):
The value of bit D5 is determined by the value applied to pin 8 of connector J3. Normally, this signal is at a "1" level when the printer is busy or unable to accept data. See Section 4.7 for a discussion of printer interfacing.

Floppy Disk Index Hole Sense:
If bit D6 is a "1" value, then the floppy disk drive which is active has detected the index hole of the floppy diskette.

Keyboard Scan Reference:
Bit D7 alternates between a "0" and "1" value every 10 msec (approximately) in synchronism with the keyboard matrix scanning. This bit is used in the auto-repeat feature implementation. The low-to-high transition is sensed and used to synchronize the disabling of the keyboard scanning with the end of a scan cycle (the scanning must be disabled immediately after a complete scan of the matrix has been completed).

<u>Programming Example:</u>

The STATUS REGISTER can be polled to provide information on the status of the peripheral controllers and so control data transfers. The following example illustrates how the printer status can be polled to determine when the printer is ready to accept another character:

```
LOOP:
    IN   A,18H          ; GET PRINTER STATUS
    BIT  5,A            ; CHECK IF READY
    JR   NZ,LOOP        ; LOOP IF BUSY
```

4.2 Timer

The timer is internal to the keyboard controller. Although it can be programmed to generate different time intervals by accessing the command register of the keyboard controller, this is not advised. The timer is used by the controller to provide debouncing of the keyboard switches. This debounce time is set to match the keyboard of the PIED PIPER. Changing the timer interval could cause unreliable keyboard operation. The timer is set to interrupt the CPU every 10.24 msec.

The timer interrupt is enabled by the contents of CONTROL REGISTER I. When a timer interrupt occurs and is accepted by the CPU, then the interrupt handling software causes the contents of memory location FFCF hex to be incremented. In addition, the keyboard decoding software uses the interrupt to check for any auto-repeat key closures. Finally, a jump vector is included at the end of the interrupt handler (memory address FB92 hex). This jump vector allows OEM users to add their own software to perform special timer interrupt handling. The default value stored for the jump vector is a branch to a 'RET' instruction. OEM users who want to make use of this capability must add their own routine and patch the jump vector to point to the new routine. The routine must set up a local stack. At the end of all processing, a 'RET' instruction must be executed.

During floppy disk accesses, the CPU is being interrupted by the floppy disk controller as the data is transferred. Because of the resulting heavy demand placed on the interrupt system, the CPU might not be able to service both the timer and the floppy disk interrupts. To avoid any conflicts, the timer is disabled during floppy disk access. If the timer is used as a real time clock, accuracy will suffer during disk accesses.

4.3 Keyboard Decoding

The PIED PIPER keyboard has 61 keys. Except for a few special keys, the keyboard ressembles a full sized typewriter keyboard. All keys except FUNCT, SHIFT, CTRL, and CAPS LOCK are arranged in a matrix with the keys located at the crosspoints of the rows and columns. The keyboard controller (an Intel 8279) scans the rows of the matrix one after the other. As each row is enabled, the column lines are sensed to determine if any keys in that row are closed. If a closure is detected, then the row and column values are used to form up a 6-bit value which is essentially the address of the closed key in the matrix. The status of the SHIFT and CONTROL keys is also sensed and used to contribute the remaining two bits of the 8-bit key code. This key code is then used by the decoding software to generate the ASCII code for the pressed key. The CAPS LOCK key is sensed using the system STATUS REGISTER and if closed, the ASCII code of any alphabetic key is modified to upper case. The FUNCT key is connected so as to simulate the simultaneous closure of the SHIFT and CTRL keys. The decoding software interprets this combination as a function code which must be defined by the software.

Although there is no repeat key on the keyboard, by pressing a key without releasing it for more than one second, the key is duplicated automatically every 50 msec. until the key is released. This auto-repeat feature does not work with the FUNCT key. This feature is implemented by software and is described in more detail in a later section.

4.3.1 Keyboard Controller Registers

The 8279 controller chip contains internal registers which are accessed by the CPU as I/O ports. The data register is assigned port 08H, and the command/status register is assigned port 09H. The purpose of these registers is explained in the following sections.

Command Register (Port 09H)

The command register is used to program the operating mode for the 8279. This register also sets the dividing ratio for the counter which forms the system timer. The bits of the command register are defined as follows:

```
-------------------------
|D7|D6|D5|D4|D3|D2|D1|D0|
-------------------------
  |  |  |  |  |  |  |  |
  |  |  |  |  |  |  |  |-->
  |  |  |  |  |  |  |----->
  |  |  |  |  |  |-------->  Command Data Bits
  |  |  |  |  |----------->
  |  |  |  |-------------->
  |  |  |
  |  |  |----------------->
  |  |-------------------->  Command Bits
  |----------------------->
```

The Command Bits specify the command being issued to the 8279, and the Command Data Bits give the data associated with the command. Only three 8279 commands are used by the system software. The function of each of these commands and the definition of the corresponding data bits is as follows:
Keyboard Controller Initialization:

This command must be issued after system startup to define the keyboard scan mode for the controller. This command is defined by the Command Bits:

D7	D6	D5
0	0	0

The Command Data Bits are used to specify which keyboard scan mode is to be used. Only the three least significant bits are used for this purpose and they are defined as follows:

D2	D1	D0	Scan Mode
0	0	0	Encoded Scan - 2-Key Lockout
0	0	1	Decoded Scan - 2-Key Lockout
0	1	0	Encoded Scan - N-Key Rollover
0	1	1	Decoded Scan - N-Key Rollover
1	0	0	Encoded Scan Sensor Matrix
1	0	1	Decoded Scan Sensor Matrix
1	1	0	Strobed Input, Encoded Scan
1	1	1	Strobed Input, Decoded Scan

The PIED PIPER keyboard is encoded, and the system hardware/software is set to operate in the 2-Key Lockout mode, so the only valid value to be issued to the command register for initialization is 00 hex. A system reset will also cause the controller to go to the encoded scan, 2-key lockout mode.

Timer Set:

This command is used to establish the dividing ratio for the timer counter inside the 8279. This timer is used by the 8279 to perform keyswitch debouncing. The timer also generates a system reset to provide a timer function for the system software. The Command Bits used to specify the Timer Set command are as follows:

D7	D6	D5
0	0	1

The incoming clock frequency for the timer is set at 1 MHz. For proper keyswitch debouncing, the dividing ratio should be set to produce an output frequency of 100 kHz (i.e., dividing ratio = 10). The Command Data Bits contain the value of the dividing ratio, which must be an integer between 2 and 31. For the PIED PIPER, the dividing ratio must be set to 10 (01010B). Thus the only valid value which can be issued to the 8279 command register for timer setup is 2A hex.

Read FIFO:

This command is issued to specify that the keyboard FIFO is to be used as the source of data for any subsequent reads of the 8279 data register. The Command Bits for this command are defined as follows:

D7	D6	D5
0	1	0

The 8279 contains a display memory which can also be accessed via the data register but which is not used in the PIED PIPER, therefore the keyboard FIFO is the only valid source of data. This command need only be issued once, as all sebsequent reads of the data register will retrieve data from the keyboard FIFO in the order in which it was entered.

Since the PIED PIPER uses an encoded scan keyboard, the Command Data Bits are irrelelevant and so the only valid value which can be issued to the 8279 command register to implement the Read FIFO command is 40 hex. After a system reset, the 8279 automatically enters this mode.

Status Register (Port 09H)

The Status Register contains the number of codes stored in the FIFO as well as any error flags. The bits of the Status Register are defined as follows:

```
-------------------------
|D7|D6|D5|D4|D3|D2|D1|D0|
-------------------------
  |  |  |  |  |  |  |  |
  |  |  |  |  |  |  |  |-->
  |  |  |  |  |  |  |----->   Number of Key Codes in FIFO
  |  |  |  |  |  |-------->
  |  |  |  |  |
  |  |  |  |  |----------->   FIFO Full
  |  |  |  |
  |  |  |  |-------------->   Error-Underrun
  |  |  |----------------->   Error-Overrun
  |  |
  |  |-------------------->   Not Used
  |----------------------->   Not Used
```

If bit D3 is "1", then the FIFO is full (the FIFO can contain up to eight key codes). The two error conditions which can be detected are underrun and overrun. Underrun occurs when the CPU tries to read data from the Data Register but the FIFO is empty. Overrun occurs when a keyswitch closure is detected but the FIFO is already full. If either error bit is a "1" value, then the corresponding error condition was detected.

Data Register (Port 08H)

The Data Register is used to return the key codes of any pressed keys stored in the FIFO. Up to eight key codes can be stored in the FIFO. Subsequent reads of the Data Register will retrieve the key codes in the order in which they were entered, until the FIFO is empty. The number of key codes stored in the FIFO can be obtained from the contents of the Status Register.

The 8279 forms up the key code for any pressed key by returning the values of the scan (row) and return (column) counters representing the position of the pressed key in the keyboard matrix. The status of the CTRL and SHIFT keys is also returned. The format of the key code returned via the

Data Register is as follows:

```
-------------------------
|D7|D6|D5|D4|D3|D2|D1|D0|
-------------------------
  |  |  |  |  |  |  |  |
  |  |  |  |  |  |  |  |-->
  |  |  |  |  |  |  |----->    Scan Counter Value
  |  |  |  |  |  |-------->
  |  |  |  |  |
  |  |  |  |  |----------->
  |  |  |  |-------------->    Return Line Status
  |  |  |----------------->
  |  |
  |  |-------------------->     SHIFT Key Status
  |
  |----------------------->     CTRL Key Status
```

Scan Counter Value:
    These three bits represent the value of the scan counter and indicate the row of the keyboard matrix that the pressed key was found in.

Return Line Status:
    These three bits indicate the value sensed by the return lines and indicate the column of the keyboard matrix that the pressed key was found in.

SHIFT Key Status:
    If bit D6 is a "0" value, then the SHIFT key was pressed along with the alphanumeric key. Bits D6 and D7 will both be "0" if the FUNCT key was pressed.

CTRL Key Status:
    If bit D7 is a "0" value, then the CTRL key was pressed along with the alphanumeric key. Bits D6 and D7 will both be "0" if the FUNCT key was pressed.

Initialization Example:

The following program demonstrates how to initialize the 8279 controller for the standard PIED PIPER:

```
LD   A,00000000B     ; SET ENCODED SCAN &
OUT  09H,A           ; 2-KEY LOCKOUT
LD   A,00101010B     ; SET UP TIMER
OUT  09H,A
```

4.3.2 Auto Repeat Feature

The 8279 controller does not support the auto-repeat feature. When a key is pressed but not released, the controller only reports a single key pressed event. In order to implement the auto repeat feature, the controller must be tricked into thinking that the key has been released and pressed again. The system timer is used to keep track of key closure times. If an alphanumeric key is closed for more than approximately one second, then the software assumes it is in the auto-repeat mode. The keyboard scan is then disabled by setting bit D7 of system CONTROL REGISTER I. The 8279 controller will not detect any key closures on its next scan through the keyboard matrix since the scan signals do not appear on the row lines of the matrix. The keyboard scan is then re-enabled by resetting bit D7 of CONTROL REGISTER I. The 8279 will now detect a key closure (provided the auto-repeat key was not released) and will report the corresponding key code as if the key had just been pressed. This process will be repeated approximately every 50 msec until either the auto-repeat key is released or a different key closure is detected. The timer is used extensively in controlling the frequency of the above simulation.

4.3.3 Key Codes

The 8-bit value obtained from the keyboard controller FIFO via the data register is the key code. Each alphanumeric key has a unique key code which depends on the status of the SHIFT, CTRL, and FUNCT keys. The key code is used by the decoding software to produce the corresponding ASCII value for the pressed key, which is passed on to the operating system. Although the status of the CTRL, SHIFT, and FUNCT keys alters the key code, the same does not apply to the CAPS LOCK key. The latter key is only taken into account when the key code is translated into the ASCII code. The CAPS LOCK key causes all lower case alphabetic keys to be transformed into upper case ASCII codes. The numeric and symbol keys are not affected.

The CTRL key works with all alphabetic letter keys, plus the following:

- shift 2
- shift 6
- [
-]
- \
- shift -

All other keys are translated as if the CTRL key is not pressed.

The SHIFT key works the same way as on a typewriter; i.e.

letter keys are capitalized, and special characters above the number keys are produced.

The FUNCT key works with all alphabetic letter keys, the number keys except 2 and 6, and the arrow keys. The use of the FUNCT key with the number and arrow keys is reserved for horizontal scrolling with the TV display, and also for display manipulation with the Liquid Crystal Display option. The remaining keys can be used with the FUNCT key to produce unique character codes which can be interpreted by OEM custom application software. These function keys are decoded by calling the CP/M CONIN BDOS function. The translated value of a function key has the most significant bit set.

The following tables give the key codes assigned to the PIED PIPER keyboard. All values are in hexadecimal.

Key	Alone	SHIFT	CTRL	FUNCT
ESC	C0	80	40	00
1 !	C8	88	48	08
2 @	C1	81	41	01
3 #	C9	89	49	09
4 $	CA	8A	4A	0A
5 %	C2	82	42	02
6 ^	C3	83	43	03
7 &	CB	8B	4B	0B
8 *	CC	8C	4C	0C
9 (	C4	84	44	04
0)	C5	85	45	05
- _	CD	8D	4D	0D
= +	CE	8E	4E	0E
£ ~	C6	86	46	06
DELETE	C7	87	47	07
BREAK	CF	8F	4F	0F
TAB	D0	90	50	10

Key	Alone	SHIFT	CTRL	FUNCT
Q	D8	98	58	18
W	D9	99	59	19
E	D1	91	51	11
R	D2	92	52	12
T	DA	9A	5A	1A
Y	DB	9B	5B	1B
U	D3	93	53	13
I	D4	94	54	14
O	DC	9C	5C	1C
P	DD	9D	5D	1D
[{	D5	95	55	15
] }	D6	96	56	16
\ |	DE	9E	5E	1E
BACK SPACE	DF	9F	5F	1F
A	E1	A1	61	21
S	E9	A9	69	29
D	EA	AA	6A	2A
F	E2	A2	62	22
G	E3	A3	63	23

Key	Alone	SHIFT	CTRL	FUNCT
H	EB	AB	6B	2B
J	EC	AC	6C	2C
K	E4	A4	64	24
L	E5	A5	65	25
; :	ED	AD	6D	2D
' "	EE	AE	6E	2E
RETURN	E6	A6	66	26
LINE FEED	E7	A7	67	27
Z	F9	B9	79	39
X	F1	B1	71	31
C	F2	B2	72	32
V	FA	BA	7A	3A
B	FB	BB	7B	3B
N	F3	B3	73	33
M	F4	B4	74	34
, <	FC	BC	7C	3C
. >	FD	BD	7D	3D
/ ?	F5	B5	75	35
← ↑	F6	B6	76	36
→ ↓	FE	BE	7E	3E
SPACE BAR	F8	B8	78	38

4.4 Video Display Controller

The video display is generated using a Signetics 2672 Programmable Video Timing Controller (PVTC) and associated logic and display memory. The controller is connected in the independent buffer mode, in which display memory is separate from main processor memory and data transfers between the CPU and display memory occur via one byte Display Buffers.

The video display is a character block display and supports the following capabilities:

- 80 or 40 column display
- 24 lines
- 7 by 9 character block
- black-on-white or white-on-black display
- one character attribute (reverse video or dual-intensity)
- block cursor

The video display controller is an intelligent controller with many features in addition to the ones described above. The following sections only relate to its use in the PIED PIPER. Please refer to the Signetics 2672 Programmable Video Timing Controller Application Notes for more details.

Video Controller Registers

The PVTC contains eight internal registers which define the display format and contain display memory addresses. The address assignments are as follows:

PORT	READ	WRITE
00H	Interrupt Register	Initialization Register
01H	Status Register	Command Register
02H	Screen Start Address Register (low byte)	Screen Start Address Register (low byte)
03H	Screen Start Address Register (high byte)	Screen Start Address Register (high byte)
04H	Cursor Address Register (low byte)	Cursor Address Register (low byte)
05H	Cursor Address Register (high byte)	Cursor Address Register (high byte)
06H	- -	Pointer Address Register (low byte)
07H	- -	Pointer Address Register (high byte)

Initialization Register (Port 00H)

The normal start-up condition of the PVTC is: 7 by 9 character block, white-on-black screen, 2K character set, dual intensity, and 80 columns display. The cursor is a non-blinking block character. The display is 24 lines. This format is specified to the PVTC via the Initialization Register. Actually, there are 11 initialization registers (IR0 - IR10) which are accessed in sequence by writing 11 bytes of data to the initialization register port address in sequence. The PVTC internally unpacks the bytes and places them in the proper registers. This is the normal initialization procedure which follows system start-up or reset. The PVTC also supports a command which allows one of the registers to be selected and its contents altered without sequencing through all 11 registers.

The PIED PIPER PVTC is initialized by supplying the following bytes in sequence to the initialization register:

	D7	D6	D5	D4	D3	D2	D1	D0	(hex)
IR0	0	1	0	0	0	1	0	0	(44H)
IR1	0	0	1	1	0	0	1	0	(32H)
IR2	0	0	0	0	1	1	1	0	(0EH)
IR3	0	1	1	0	0	1	1	0	(66H)
IR4	0	0	0	1	0	1	1	1	(17H)
IR5	0	1	0	0	1	1	1	1	(4FH)
IR6	0	0	0	0	1	0	0	0	(08H)
IR7	0	0	0	0	1	0	0	1	(09H)
IR8	1	0	0	0	0	0	0	0	(80H)
IR9	0	0	0	1	0	0	0	0	(10H)
IR10	1	0	0	0	0	0	0	0	(80H)

Command Register (Port 01H)

The PVTC commands are divided into two classes: the instantaneous commands, which are executed immediately after they are invoked, and the delayed commands which may require a delay for a blanking interval prior to their execution. The possible instantaneous commands are as follows:

D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	-	Master Reset
0	0	0	1	V	V	V	V	-	Load IR Address
0	0	1	x	1	0	x	0	-	Display Off (*)
0	0	1	x	1	N	x	1	-	Display On (**)
0	0	1	1	x	x	x	0	-	Cursor Off (*)
0	0	1	1	x	x	x	1	-	Cursor On (**)
0	1	0	N	N	N	N	N	-	Reset Interrupt/Status Bits
1	0	0	N	N	N	N	N	-	Disable interrupts
0	1	1	N	N	N	N	N	-	Enable interrupts

(*) Any combination of these two commands is valid.
(**) Any combination of these two commands is valid.
x = don't care

Master Reset:

This command initializes the PVTC and may be invoked at any time to return the PVTC to its initial state. The display is blanked and the interrupt/status bits are reset to 0 (except RDFLG=1).

Load IR Address:

This command is used to preset the initialization register pointer to the value defined by bits D3 to D0. Allowable values are 0 to 10, corresponding to internal registers IR0 to IR10. Any subsequent write operation to the initialization register will result in the data being placed in the internal register specified by this pointer.

Display Off:

This command blanks the display.

Display On:

This command restores the normal display either at the beginning of the next field (N=1) or at the beginning of the next scan line (N=0).

Cursor Off:

This command removes the cursor block from the display.

Cursor On:

This command restores the cursor block to the display.

Reset Interrupt/Status Bits:

This command resets the designated bits in the interrupt and status registers. The corresponding bit in the interrupt/status register is reset to 0 wherever N=1 in the command.

Disable Interrupts:

This command sets up an interrupt mask to disable the designated interrupts and prevent them from generating a system interrupt or from appearing in the interrupt register. The corresponding interrupt in the interrupt register is disabled wherever N=1 in the command.

Enable Interrupts:
This command resets the indicated interrupt and status register bits and sets the corresponding interrupt mask bits to 1 to enable the interrupts. The corresponding interrupt bit is cleared and the interrupt enabled wherever N=1 in the command.

The following commands will either be executed immediately or delayed until the display is blanked (such as during the horizontal retrace time). The amount of delay depends on when the command is invoked. The "Increment Cursor" and "Write from Cursor to Pointer" commands are always executed immediately. The PVTC will set the ready flag (RDFLG) in the Status Register to signify the completion of the command. No other commands should be issued until the current command is completed. The possible delayed commands are as follows:

D7	D6	D5	D4	D3	D2	D1	D0		
1	0	1	0	0	1	0	0	-	Read at Pointer Address
1	0	1	0	0	0	1	0	-	Write at Pointer Address
1	0	1	0	1	0	0	1	-	Increment Cursor Address
1	0	1	0	1	1	0	0	-	Read at Cursor Address
1	0	1	0	1	0	1	0	-	Write at Cursor Address
1	0	1	0	1	1	0	1	-	Read at Cursor Address and Increment Address
1	0	1	0	1	0	1	1	-	Write at Cursor Address and Increment Address
1	0	1	1	1	0	1	1	-	Write from Cursor Address to Pointer Address

Read/Write at Pointer Address:
Data is transferred between the location in display memory whose address is given by the contents of the Pointer Register and the Display Read/Write Buffer.

Increment Cursor Address:
Adds one to the contents of the Cursor Address Register.

Read/Write at Cursor Address:
Data is transferred between the location in display memory whose address is given by the contents of the Cursor Address Register and the Display Read/Write Buffer.

Read/Write at Cursor Address and Increment Address:
Same as "Read/Write at Cursor Address" only after the data is transferred, the contents of the Cursor Address

Register is incremented by one.

Write from Cursor Address to Pointer Address:
The data contained in the Display Write Buffer is transferred into the display memory block from the address given by the contents of the Address Register to the address given by the contents of the Pointer Address Register, inclusive. After completion of the command, the Pointer Address Register contents are unchanged, but the Cursor Address Register contents will be the same as the Pointer Address Register contents.

Interrupt/Status Registers (Ports 00H, 01H)

The Interrupt and Status Registers both provide information on the five possible interrupting conditions. These conditions may be selectively enabled/disabled (masked) by issuing the "Enable/Disable Interrupt" commands to the Command Register. An interrupting condition will always be indicated in the Status Register, whether that interrupt is enabled or not, but an interrupt will not be generated and the corresponding bit not set in the Interrupt Register for any interrupt which is not enabled. Any interrupt bits which are set will remain set until reset by the "Reset Interrupt" command or until a system reset occurs. One other difference between the Interrupt and Status Registers is that the Status Register contains one extra bit (RDFLG) which indicates when the PVTC can accept another command.

The bits of the Interrupt and Status Registers are defined as follows:

```
-------------------------
| 0| 0|D5|D4|D3|D2|D1| 0|
-------------------------
        |  |  |  |  |
        |  |  |  |  |------> Ready
        |  |  |  |
        |  |  |  |---------> Split Screen
        |  |  |
        |  |  |------------> Line Zero
        |  |
        |  |---------------> VBLANK
        |
        |------------------> RDFLG (Status Register Only)
```

Ready:
Certain PVTC commands affect the display and may require the controller to wait for a blanking interval before executing the command. This bit is set to a "1" when execution of the command is completed. No command should be issued unless this bit is a "1".

Split Screen:

This bit is set to a "1" when a match occurs between the current character row number and the value contained in internal Initialization Register 10 (IR10). The comparison is done at the beginning of line zero of each character row. This bit is reset to "0" when either of the Screen Start Address Registers is loaded by the CPU.

Line Zero:

This bit is set to a "1" at the beginning of the first scan line (line 0) of each active character row.

VBLANK:

This bit indicates the beginning of a vertical blanking interval. It is set to a "1" at the beginning of the first scan line of the vertical front porch.

RDFLG:

A "0" indicates that the controller is currently executing the previously issued command. A "1" indicates that the controller is ready to accept a new command.

Address Registers (Ports 02H-07H)

The Screen Start Address Registers contain the address of the first character of the first row (upper left corner of the display). The data in the display memory is displayed sequentially starting from the address contained in the Screen Start Address Registers. The Cursor Address Registers contain the address of the location in display memory of the cursor. The Pointer Address Registers are used to specify display memory addresses required by some commands.

4.4.2 Display Read/Write Buffers

The display memory is separate from the main processor memory, therefore any data transfers between the CPU and display memory must be controlled by the PVTC. The data to be transferred is passed through the Display Read or Write Buffer. These are simply a pair of latched I/O ports which serve as single byte buffers. The Read Buffer is assigned I/O port address 0D hex, the Write Buffer is assigned I/O port address 1C hex. These buffers are normally used with one of the delayed commands of the PVTC.

To transfer data from the main CPU to display memory, the CPU executes an "OUTPUT" instruction to store the data in the Write Buffer. The display memory address where the data is to be stored is then loaded by the CPU into the Pointer Address Registers. The CPU checks the RDFLG of the Status Register and waits for any previous command to conclude. The CPU then issues the "Write at Pointer Address" command to the PVTC Command Register. The PVTC then retrieves the data from the Write Buffer and places it in display memory at the address given by the Pointer Address Register contents. The RDFLG flag is set when the transfer is completed. The Cursor Address Register could also be used instead of the Pointer Register.

To transfer data from display memory to the main CPU, the display memory address where the data is to be stored is first loaded by the CPU into the Pointer Address Registers. The CPU checks the RDFLG of the Status Register and waits for any previous command to conclude. The CPU then issues the "Read at Pointer Address" command to the PVTC Command Register. The PVTC then retrieves the data from display memory at the address given by the Pointer Address Register contents and stores it in the Read Buffer. The RDFLG flag is set when the transfer is completed. The CPU then executes an "INPUT" instruction to read the data from the Read Buffer.

The following program examples are included to demonstrate the use of the PVTC registers and the display buffers.

Example 1: Clear the display.

```
NOTRDY:
     IN   A,01H       ; GET STATUS
     AND  20H         ; CHECK IF READY
     JR   Z,NOTRDY    ; REPEAT IF BUSY
     LD   A,20H       ; SET TO INITIALIZE TO BLANKS
     OUT  1CH,A       ; SEND TO WRITE BUFFER
     LD   A,80H       ; INITIALIZE CURSOR REGISTERS
     OUT  04H,A       ; TO TOP LEFT CORNER OF SCREEN
     LD   A,00H
     OUT  05H,A
     LD   A,0FFH      ; INITIALIZE POINTER REGISTERS
     OUT  06H,A       ; TO BOTTOM RIGHT CORNER
     LD   A,07H       ; OF SCREEN
     OUT  07H,A
     LD   A,10111011B
     OUT  01H,A       ; WRITE CURSOR TO POINTER
```

Example 2: Read contents of display memory at cursor position.

```
                LD   A,10101100B    ; READ AT CURSOR
                OUT  01H,A
        NOTRDY:
                IN   A,01H        ; GET STATUS
                AND  20H          ; CHECK IF READY
                JR   Z,NOTRDY     ; REPEAT IF BUSY
                IN   A,0DH        ; READ DATA FROM READ BUFFER
```

4.4.3 Display Memory Organization

The characters which form up the video display are stored in display memory. The PVTC controller scans through display memory, producing the screen image character by charcter, row by row. Each character is represented in display memory as one byte, the seven least significant bits of which are the ASCII code for the character. The most significant bit is the video attribute bit. If set, it indicates that the character is to be displayed in either high intensity or reverse video (the contents of CONTROL REGISTER II determine which video attribute is selected). If reset, the character is displayed as normal.

The display memory address space goes from 0000 hex to 07FF hex. The Screen Start Registers of the PVTC contain the address of the location in display memory where the first character of the first row (i.e., the top left hand corner of the display screen) is stored. The next higher address indicates the location of the second character of the first row. Each character is stored in sequence in this way. The first character of the second row is stored in the location right after the last character of the first row. The PVTC controller is smart enough to automatically wrap around the display memory. If the end of display memory is reached before the last line of the display is scanned, then the PVTC will display the character stored in location 0000 after the character stored in location 07FF hex, and continue on in sequence from there until the end of the screen is reached. This allows the Screen Start Address Register contents to be changed dynamically to implement such features as scrolling. As an example, the PIED PIPER uses a 24 by 80 display format. The Screen Start Address Register is initialized to 0080 hex. The number of memory cells from 0080 hex to 07FF hex is 1920, which is also equal to the number of characters in a screen (24 times 80). Thus the first character of the first row (upper left hand corner of screen) is stored in location 0080 hex, with the last character of the last row (lower right hand corner of screen) stored in location 07FF hex. If the Screen Start Address Register contents were to be changed to 0120 hex, then row 3 of the previous display would now appear as row 1 on the screen (i.e., the screen would scroll up two rows). Due to the memory wrap around feature, memory location 011F hex will now represent the lower right hand corner of the screen.

The Cursor Address Registers contain the memory address of the current cursor position. For example, if the screen start address is 0120 hex, and the Cursor Address Registers contain the value 01C0 hex, then the cursor block will appear in the first character position of the third row of the screen.

The Pointer Registers are used most of the time to clear (fill with blanks) a portion of the display memory. This is accomplished by using the PVTC command "Write from Cursor to Pointer". Continuing the above example, to blank out the third line of the display, the Pointer Register is filled with the value 023F hex (Cursor Address Register contents + 79 = end of third line). The Write Buffer is then filled with the value 20 hex (ASCII space code) and the PVTC executes the "Write from Cursor to Pointer" command.

4.4.4 Character Set

The character set is contained in EPROM and so can be changed by OEM users. The PIED PIPER displays most characters found on standard video display terminals. Exceptions are:

- the British pound sign "£" replaces the single back quote "`"
- block graphic characters are included

The character set is given in the following table:

Most Significant Bit

	0	1	2	3	4	5	6	7
0	┘	ʳ⊬		0	@	P	£	p
1	┌	÷	!	1	A	Q	a	q
2	┘	≥	"	2	B	R	b	r
3	┐	≤	#	3	C	S	c	s
4	┴	┌	$	4	D	T	d	t
5	┬	└	%	5	E	U	e	u
6	├	▯	&	6	F	V	f	v
7	┤	⊥	'	7	G	W	g	w
8	⌐	↑	(	8	H	X	h	x
9	▨	↓	)	9	I	Y	i	y
A	┼	→	*	:	J	Z	j	z
B	│	←	+	;	K	[	k	{
C	─	\	,	<	L	\	l	|
D	▬	⊃	-	=	M	]	m	}
E	≠	△	.	>	N	^	n	∿
F	○	▽	/	?	O	_	o	■

The PIED PIPER displays all the ASCII characters with the most significant bit used as the video attribute bit. The graphics characters can be displayed along with the alphanumeric characters by directly storing the corresponding code in display memory, or by making use of the lead-in function (see Section 4.4.5). Alphanumeric characters with one video attribute can be displayed along with the graphics characters.

The character generator EPROM contains the dot matrix pattern for each displayable character in a form useable by the PVTC video controller. Sixteen bytes are reserved for each character. In the normal display mode, 9 scan lines are used for each character. One byte is used to store the dot pattern of a scan line. The bytes are stored in EPROM in order from top to bottom of the character. Thus the first nine bytes of each sixteen byte group define a character dot matrix 8 dots wide and 9 dots high. The remaining bytes of each sixteen byte group are not used and so are filled with zeros. Each bit represents a dot in the 8 x 9 matrix. A dot is displayed if the corresponding bit is a "1" and the display mode is white-on-black. The PIED PIPER actually uses a 7 x 9 dot matix, so the least significant bit of each byte is "don't care".

4.4.5 Terminal Emulation

The video display software contains drivers which control all display functions. If applications programs use the normal CP/M BDOS function calls for all console input/output, then these driver routines are automatically used. These routines make the CP/M console device appear as a Hazeltine 1500 terminal to the application program. When configuring application programs which make use of screen functions, select the Hazeltine 1500 as the terminal during the installation procedure.

All functions of the Hazeltine 1500 are emulated, except the following:

- Field Tab
- Block Mode

The following functions, not available on the Hazeltine 1500, have been added:

Function	Code
Turn cursor ON	Lead-in,SOH (7EH,01H)
Turn cursor OFF	Lead-in,STX (7EH,02H)
Turn display ON	Lead-in,ETX (7EH,03H)
Turn display OFF	Lead-in,EOT (7EH,04H)
Graphic character	Lead-in,RS,char (7EH,1EH)

The graphic character function allows application programs to produce video displays which incorporate the graphic character set.

4.5 Floppy Disk Controller

The PIED PIPER contains an integral 5 1/4" double-sided, double-density, 96 TPI (quad-density) floppy disk drive. The floppy diskettes used with the system should be double-sided, double-density and 96 TPI. The unformatted capacity of a diskette is 1 Mbyte. The formatted capacity is 800 Kbyte. The recording technique is MFM.

4.5.1 Floppy Disk Controller Registers

The floppy disk controller is a Western Digital FD1793. This controller has four internal read/write registers which are used to specify controller commands, to transfer data, and to indicate controller status. These registers appear as a set of I/O ports to the CPU, with the following address assignments:

PORT	READ	WRITE
10H	Status Register	Command Register
11H	Track Register	Track Register
12H	Sector Register	Sector Register
13H	Data Register	Data Register

Command Register (Port 10H)

The Command Register is used to pass commands to the floppy disk controller. The commands are divided into four different classifications (Type I to Type IV). The commands used by the PIED PIPER software, and their corresponding codes, are given in the following table:

D7	D6	D5	D4	D3	D2	D1	D0	Type	Command
0	0	0	0	1	1	0	0	I	Restore
0	0	0	1	1	1	0	0	I	Seek
0	1	0	1	1	1	0	0	I	Step In
1	0	0	0	s	0	1	0	II	Read Sector
1	0	1	0	s	0	1	0	II	Write Sector
1	1	0	0	0	0	0	0	III	Read Address
1	1	1	1	0	0	0	0	III	Write Track
1	1	0	1	0	0	0	0	IV	Force Interrupt

s = Side Select Flag
  = 1 for Side 1
  = 0 for Side 0

Restore:

The disk drive read/write head is stepped to the Track 0 position and loaded. The Track Register is loaded with zeros and an interrupt is generated (INTRQ).

Seek:

The read/write head is stepped to the track position given by the contents of the Data Register. The head is loaded and the Track Register contents are updated to the new track number. An interrupt is generated on completion of the command.

Step In:

The read/write head is stepped in one track towards the centre. The head is loaded, and the track register contents are updated to the new track number. An interrupt is generated on completion of the command.

Read Sector:

The head is loaded and the designated sector read, with the data returned in the Data Register. The read/write head must be positioned over the correct track with the correct side selected. The sector to be read is given by the contents of the Sector Register. When the first byte is transferred to the Data Register, a DRQ interrupt is generated. As each successive byte is transferred, DRQ interrrupts are generated. The CPU must transfer the bytes out of the Data Register as fast as the controller transfers them in or bytes will be lost. When the entire sector has been read, an INTRQ interrupt is generated.

Write Sector:

The head is loaded and the designated sector written, with the data supplied by the Data Register. The read/write head must be positioned over the correct track with the correct side selected. The sector to be written is given by the contents of the Sector Register. When the first byte is removed from the Data Register and written to the diskette, a DRQ interrupt is generated to indicate the controller is ready for the next byte. As each successive byte is written, DRQ interrrupts are generated to indicate the controller is ready for the next byte. The CPU must transfer the bytes into the Data Register as fast as the controller writes them to diskette or bytes will be lost. When the entire sector has been written, an INTRQ interrupt is generated.

Read Address:
The head is loaded and the ID field is read from the diskette. As each byte is read, the DRQ interrupt is generated. The Track Address of the ID field is placed in the Sector Register. An INTRQ interrupt is generated when the command is completed.

Write Track:
The head is loaded and one track is written on the diskette. The read/write head must be positioned over the correct track with the correct side selected. The DRQ interrupt is generated every time the controller is ready to accept another byte via the Data Register. An INTRQ interrupt is generated when the command is completed.

Force Interrupt:
This command can be loaded into the controller at any time, even if it is executing another command. It is used to terminate any executing command and clear any interrupts. No INTRQ interrupt is generated.

Status Register (Port 10H)

The Status Register is used to determine the state of the controller as it executes a command. The meaning of the bits depends on the Type of the command being executed.

TYPE I Commands:

```
-------------------------
|D7|D6|D5|D4|D3|D2|D1|D0|
-------------------------
  |  |  |  |  |  |  |  |-----> Busy
  |  |  |  |  |  |  |--------> Index
  |  |  |  |  |  |-----------> Track 0
  |  |  |  |  |--------------> CRC Error
  |  |  |  |-----------------> Seek Error
  |  |  |--------------------> Head Loaded
  |  |-----------------------> Write Protect
  |--------------------------> Not Ready
```

Busy:
A "1" value indicates the controller is presently executing a command. A "0" indicates the controller can accept a new command.

Index:
A "1" value indicates that the diskette index mark was detected by the active disk drive.

Track 0:
A "1" value indicates that the read/write head is located over the Track 0 position.

CRC Error:
A "1" value indicates that a CRC error was encountered in the ID field.

Seek Error:
A "1" value indicates that the seek operation to the desired track position was not verified.

Head Loaded:
A "1" value indicates that the head is loaded and engaged.

Write Protect:
A "1" value indicates that the diskette in the drive is write protected.

Not Ready:
This signal is not implemented on the PIED PIPER.

Type II & III Commands:

```
 -------------------------
 |D7|D6|D5|D4|D3|D2|D1|D0|
 -------------------------
   |  |  |  |  |  |  |  |
   |  |  |  |  |  |  |  |-----> Busy
   |  |  |  |  |  |  |---------> DRQ
   |  |  |  |  |  |------------> Lost Data
   |  |  |  |  |---------------> CRC Error
   |  |  |  |------------------> Record not Found
   |  |  |---------------------> Record Type/Write Fault
   |  |------------------------> Write Protect
   |---------------------------> Time Out
```

Busy:
A "1" value indicates the controller is presently executing a command. A "0" indicates the controller can accept a new command.

DRQ (Data Request):

This bit is a copy of the DRQ interrupt signal. A "1" value indicates that the Data Register contains a byte for the CPU when the controller is executing a read command, or that the Data Register is empty and can accept another byte from the CPU when the controller is executing a write command.

Lost Data:

A "1" value indicates that the CPU did not respond to the DRQ interrupt in time and so the byte to be transferred was lost.

CRC Error:

A "1" value indicates that a CRC error was encountered either in the ID field if bit D4 is "1" or else in the data field.

Record not Found:

A "1" value indicates that the desired track, sector, or side were not found.

Record Type/Write Fault:

For Read Sector command, it indicates the record-type code from the data field address mark. For all other read commands, it is "0". For the Write commands, a "1" value indicates a write fault occurred.

Write Protect:

For all Read commands, it is "0". For the Write commands, a "1" value indicates that the diskette in the drive is write protected.

Not Ready:

This signal is not implemented on the PIED PIPER.

Track Register (Port 11H)

This register is used to contain the track number. It is updated by any seeks or read/write commands so as to always contain the current track position of the read/write head.

Sector Register (Port 12H)

This register is used to contain the sector number.

Data Register (Port 13H)

This register is used to pass data values between the CPU and the floppy controller.

CONTROL REGISTER I/STATUS REGISTER

These system registers are used to enable/disable the floppy interrupts, to select the active disk drive (A or B) and side (0 or 1), and to check the status of the interrupts.

4.5.2 Diskette Format

The physical format of a formatted diskette is:

512 bytes/sector
10 sectors/track
2 tracks/cylinder
80 cylinders/diskette (800 Kbyte/diskette)

The logical format, as seen through CP/M, is:

128 bytes/sector
40 sectors/track
2 tracks/cylinder
80 cylinders/diskette (800 Kbyte/diskette)

128 bytes/record
16 records/block
8 blocks/extent

3 reserved tracks

The reserved tracks reduce the user file storage capacity to 784 Kbytes per diskette.

Blocking Factor:

4 logical sectors (128 bytes) per
physical sector (512 bytes)

Sector Translation Information:

Skew factor = 2

Logical Sector	Physical Sector
1,2,3,4	1
5,6,7,8	3
9,10,11,12	5
13,14,15,16	7
17,18,19,20	9
21,22,23,24	2
25,26,27,28	4
29,30,31,32	6
33,34,35,36	8
37,38,39,40	10

Track Format:

Shown below is the double density format used on the PIED PIPER. In order to format a diskette, the user must issue the Write Track command, and load the Data Register with the following bytes in order:

```
              # of bytes     HEX value

                  50           4E
                  12           00
                   3           F6
                   1           FC
                  50           4E
        -----     12           00
        |          3           F5
        |          1           FE
        |          1          track number   (00 to 4F)
        |          1          side number    (00 to 01)
        |          1          sector number  (01 to 0A)
        |          1           02
    *   |          1           F7
        |         22           4E
        |         12           00
        |          3           F5
        |          1           FB
        |        512           E5
        |          1           F7
        ----      32           4E
           **   1680           4E

    *  Write bracketed field 10 times
    ** Approximate
```

4.5.3 Useful Subroutines

A complete set of utility programs are supplied with the PIED PIPER which are designed to be used with the floppy disk drive. In addition, the CP/M user can access the disk drive controller through the standard BIOS function calls. For OEM users, the following programs are given to demonstrate how the floppy system can be used directly. These routines can be accessed by executing a CALL instruction to their starting address.

TYPEI (Address FFF9H)

This routine handles all the Type I commands of the floppy disk controller. The Type I commands are used to restore the disk to track 0, seek a track, or step from one track to another.

The only input parameter for this routine is the command value, which is passed through the accumulator of the Z80A processor. The status of the command upon completion is passed back through the accumulator. This status is normally the value in the status register. However, if a command is not completed within a reasonable length of time, then a time-out condition is assumed. The controller is then interrupted to force termination of the command and the status register contents are returned with bit D7 set.

Examples:

1) To restore drive A with verify:

```
          LD   A,00000001B     ; SELECT DRIVE A
          CALL 0FFF6H
          LD   A,00001100B     ; SET UP RESTORE COMMAND
          CALL 0FFF9H
```

2) Continuing the above example, to step in one track:

```
          LD   A,01011100B     ; SET UP STEP-IN COMMAND
          CALL 0FFF9H
```

3) To seek to track 40:

```
          LD   A,40            ; SET UP TARGET TRACK
          OUT  13H,A           ; SEND TO DATA REGISTER
          LD   A,00011100B     ; SET UP SEEK COMMAND
          CALL 0FFF9H
```

DELAY (Address FFFCH)

This routine produces a timing delay of approximately 1 millisecond. This routine is used mainly before and/or after issuing a Type I command to produce any needed delays for the disk drive to stabilize (e.g. delay for the head settling time if head is loaded by the command).

No input parameter is required for this routine.

DSKSEL (Address FFF6H)

This routine is used to select the active disk drive (either A or B) and the active side (either 0 or 1). This routine updates memory location FFE2 hex which is assumed by the system software to contain the last value sent to the Command Register.

Since the drive selection or side selection process only affects the three least significant bits of the command register, the only input parameter for this routine is the desired value for those three bits. The three bits are placed in the accumulator as the three least significant bits before calling the routine. Note that when switching sides, the disk drive selection bit for the desired disk drive must also be included as one of the three bits, even if the active drive is not being changed.

The routine first obtains the current value of the Command Register, then updates the three least significant bits based on the input parameter, saves the new value of the Command Register in memory location FFE2 hex, and finally sends the value to the Command Register.

Example:

1) To select Drive B, Side 1:

```
LD   A,00000110B
CALL 0FFF6H
```

FDRWS (Address FFF3H)

This routine is used for handling the read and write functions of the floppy disk. This routine only sets up the command value and directs it to the Command Register. The physical input/output is performed by the interrupt routine.

There are two input parameters for this routine. One is the floppy disk command (either read or write) which is passed through the accumulator. The other parameter is the starting address of the data buffer which is passed via the HL register pair of the Z80A processor. The status of the command upon completion is passed back through the accumulator. This status is normally the value in the status register. However, if a command is not completed within a reasonable length of time, then a time-out condition is assumed. The controller is then interrupted to force termination of the command and the status register contents are returned with bit D7 set.

Examples:

1) To read a sector from the diskette (the disk drive must be selected, the read/write head positioned over the proper track, the side selected, and the desired sector number placed in the Sector Register):

```
LD   A,10000010B    ; SET UP READ SECTOR COMMAND
LD   HL,buffer address
CALL 0FFF3H
```

2) To write a sector to the diskette (the disk drive must be selected, the read/write head positioned over the proper track, the side selected, and the desired sector

number placed in the Sector Register):

```
LD   A,10100010B    ; SET UP WRITE SECTOR COMMAND
LD   HL,buffer address
CALL 0FFF3H
```

4.6 Hard Disk Interface

No supporting software is supplied with the basic PIED PIPER for the hard disk interface.

4.7 Parallel Output (Printer) Port

The standard parallel interface that comes with the PIED PIPER conforms to the Centronics printer standard. For applications programmers, the CP/M BDOS function call "LISTOUT" can be used to send characters to the printer. For OEM users, the printer port can be accessed directly as I/O port address 0D hex. The Data Strobe (DSTR) pulse is programmed via bit D3 of the system COMMAND REGISTER I. The Printer Busy (PRBUSY) signal appears as bit D5 of the system STATUS REGISTER.

4.7.1 Printer Interfacing

To send a character to the printer, the following steps are required:

i) make sure printer is ready
ii) send data byte to port 0DH
iii) set data strobe high
iv) delay to compensate for paper movement
v) reset data strobe

The Printer Busy and Data Strobe manipulation involves the STATUS REGISTER and COMMAND REGISTER I, respectively. The current value of the command register can be obtained from memory location FFE2 hex.

Example: Send a character to the printer.

```
NOTRDY:
     IN    A,18H           ; GET STATUS
     BIT   5,A             ; CHECK IF READY
     JR    NZ,NOTRDY       ; REPEAT IF BUSY
     LD    A,character
     OUT   0DH,A           ; SEND TO PRINTER PORT
     LD    A,(0FFE2H)      ; GET COMMAND REG. VALUE
     SET   3,A             ; SET DATA STROBE HIGH
     OUT   18H,A
     delay
     RES   3,A             ; RESET DATA STROBE
     OUT   18H,A
```

4.8 Speaker

The PIED PIPER contains an internal speaker which can be programmed to serve as a bell or buzzer, or to produce musical tones. The speaker is driven from bit D7 of the system CONTROL REGISTER II. By continuously alternating this bit value between "0" and "1", a square wave signal is produced across the speaker terminals. The speaker will thus emit a tone whose frequency (pitch) is determined by the speed at which the bit is alternated. Since the signal is a square wave, the tone will be rich in harmonics rather than being a pure tone.

As an example, the following program generates a 1 kHz tone for one second:

```
LOOP:
     LD    A,(0FFE0H)      ; GET CONTROL REG. II VALUE
     SET   7,A             ; SET TO ACTIVATE BELL
     OUT   1DH,A           ; SEND TO CONTROL REG. II
     delay for 500 millisecond
     LD    A,(0FFE0H)      ; GET CONTROL REG. II VALUE
     OUT   1DH,A           ; DEACTIVATE BELL
     delay for 500 millisecond

     repeat LOOP so that duration is 1 second
```

CHAPTER 5 OPTIONS

5.1 Dual RS232C Serial Card

Not released with current version of Technical Manual.

5.2 Modem/Serial Card

Not released with current version of Technical Manual.

5.3 Expansion Floppy Disk Drive

Not released with current version of Technical Manual.

A. Connector Placement

B. Circuit Schematics