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Errata #

1

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Shugart

Attached is the SA600 Service and Information Package. This is being issued in lieu of the SA600 Preliminary Service Manual (P/N 39027-0) you requested. Demand for that manual has been minimal, and the product has been discontinued. Due to these factors, it would be futile to publish a formal document for this product.

Sufficient information has been included to cover your needs. Should you find a question arising, due not hesitate to contact Shugart Technical Support for assistance. We regret any inconvenience that may have occured, and pledge to continue to support the SA600 product.

Shugart has chosen to replace the 600 series with our new 706 abd 712 half-height Winchester drives. Complete documentation of the 700 series is available by requesting the Shugart 700 Reference Manual (P/N 39402). We welcome your inquiries.

Thank you.

SA600 SERVICE & INFORMATION PACKAGE

SA600 MICRO DIAGNOSTICS

INCOMING TEST & INSPECTION

FUNCTIONAL SPECIFICATION

ILLUSTRATED PARTS

SCHEMATICS

3/84

Inter-Office Memo

To: Distribution

From: Product Management
Rigid Disk

ORIGINAL

Subject: SA 600 MICRO DIAGNOSTICS

Date: May 31, 1983

Two jumpers are present on the control PCB P/N 26149-X which can enable or disable some exercising and fault detecting features. These "control" jumpers determine the microcomputer response to certain out of specification conditions which may arise. These conditions, as detected by the microcomputer, can be referred to as "control faults" to distinguish them from the read/write faults detected by the drive. Action taken by the microcomputer when these control faults occur depends upon the condition of the control jumpers. One jumper is referred to as the "delay" jumper (E1 to E2) and the other jumper is called the "exercise" jumper (E3 to E4). These jumpers can represent four possible states:

1) Both jumpers not installed (normal state)

2) Only the delay jumper is installed

3) Only the exercise jumper is installed

4) Both jumpers are installed

When a drive error is detected, logic levels corresponding to a single digit hexadecimal number as placed on pins 17 through 20 of the microprocessor chip. A logic high represents a "1" state with pin 17 the MSB and pin 20 the LSB.

The SA 600 power-up is as follows:

1) Microprocessor initializes internal registers input lines, and output lines to the proper initial states.

2) Microprocessor internal RAM is tested. If the RAM test passes, the microprocessor goes to step 3. If RAM test fails, then a hex "0" is put on pin 17-20 and ....

   If the exercise jumper is not installed, then action is halted.

   If only the exercise jumper is installed, the microprocessor loops back to step 1.

   If both jumpers are installed, action is halted.

ORIGINAL

3) The ROM code pattern is tested for validity. If the code is valid, the microprocessor goes to step 4; otherwise a hex "1" is placed on pin 17-20 and ...

If the exercise jumper is not installed, action is halted.

If only the exercise jumper is installed, the microprocessor loops back to step 1.

If both jumpers are installed, action is halted.

4) If exercise jumper is not installed, then the microprocessor goes to step 5; otherwise the output lines from the microprocessor are individually and seqeuentially toggled and checked for the proper response. If the output lines respond properly, then the microprocessor goes to step 5. If any line does not respond, a hex "2" is placed on pins 17-20 and ...

If only the exercise jumper is installed, the microprocessor goes to step 1.

If both jumpers are installed, then action halts.

5) Spindle motor control constants are initialized and the microprocessor waits for about 1/2 second for the spindle motor to "fall off" a possible unstable reluctance torque null point. When the delay is complete, the microprocessor ramps the power applied to the motor from zero to full over a period of about one second using a pulse wave duty cycle control technique. After this, the microprocessor waits about one more second while checking to see that the motor has turned at least three revolutions. If the motor has turned enough, then the microprocessor proceeds to step 6; if not, then a hex "3" is placed on pins 17-20, the drive fault line is asserted, spindle motor power is removed and ...

If the exercise jumper is not installed, action halts.
If only the exercise jumper is installed, then the microprocessor restarts.

If both the exercise and delay jumpers are installed, then action halts.

6) Actuator seeking control constants are initialized. The 100 microsecond interrupts are started and the microprocessor enters the continuous background code loop.

7) The spindle motor fault monitor routine in the background loop continuously checks to see if the spindle has stabilized within +/- 1.78 % of the proper running speed of 3571 RPM for at least two seconds. When this has occurred, the microprocessor proceeds to step 8. Note that the rest of the power up sequence is completed while the foreground and background code is continuously repeating. The tasks are managed, therefore, with a series of flags which allow each task to complete itself and hand control to the next. This process is the software equivalent of a hardware asynchronous state machine with a common clock.

8) If the delay jumper is not installed, then the microprocessor proceeds to step 9. If the delay jumper is installed, the microprocessor then delays for 25 seconds to allow the initial drive thermal transient to flatten out. This feature is used if the systems designer wants to be sure the drive is thermally stable before allowing the user to write any data on the disk.

9) The drive ready line is placed in a true state and power is applied to the stepper motor in a "Phase A" condition. If the actuator is resting at track zero then the microprocessor proceeds to step 10. If the actuator is not at track zero then it is stepped outward a maximum of 256 times until it is resting on track zero. If the actuator lands on track zero before 256 outward steps have occurred, then the actuator stepping is halted and the microprocessor proceeds to step 10. Otherwise the actuator stepping is halted, a hex "5" is placed on pins 17-20, the ready line is set false, actuator power is removed, the fault line is set true and ...

If the exercise jumper is not installed or if both the exercise and delay jumpers are installed, then all other background and foreground tasks are not affected and the microprocessor does not proceed any further in the power initialization proces. This means that if no other problems have been detected by the microprocessor, the spindle continues to turn at the proper running speed and the drive can be controlled from the interface in the normal fashion except the actuator will not respond to step commands. If only the exercise jumper is installed, then spindle motor power is removed, foreground interrupts are disabled and the microprocessor restarts.

10) The actuator will seek from track zero to track 180 and back twice to make sure the bearing lubricant is distributed properly and then the seek complete line is placed in a true state. Then: If the exercise jumper is not installed, the microprocessor proceeds to step 11.

If the exercise jumper is installed, the drive will enter a self exercise mode in which the actuator will be continuously moved in a random direction over a random distance. If the delay jumper is not installed, the actuator will dwell in each track for a period of 10 milliseconds in addition to the damping delay time. If the delay jumper is installed, the actuator will dwell for a period of 500 milliseconds on each track in addition to the damping delay time. The length of the pseudo-random sequence that the actuator will move in corresponds to 1013 seeks, therefore, the movement will repeat after that many seeks. Before each seek operation, the microprocessor will check its internal track position counter against the state of the track zero flag for agreement. If the internal track position counter and the track zero flag state agree, then the self exercise function continues; otherwise, a seek error has occurred so a hex "6" is placed on pins 17-20, the fault line is set true, the self exercise function is halted and ...

If only the exercise jumper is installed the microprocessor restarts.

If the exercise and delay jumpers are installed, the microprocessor goes to step 11. However, the electrical or mechanical cause for the seek error may still exist.

11) Drive power initialization is now complete. Foreground and background routines will continue to operate to respond to the requests from the interface. The spindle motor fault monitor routine will continue to monitor the spindle motor revolution time. If after the power initialization sequence is complete the spindle motor speed goes beyond +/- 1.78 % of 3571 RPM for more than 6 revolutions, then the fault line will be put in a true state. Additionally, if the spindle speed falls below 90 % of 3571 RPM for more than 10 revolutions, then the foreground interrupts will be disabled, a hex "4" will be placed on pins 17-20, the ready line will be set false, the stepper motor and spindle motor power will be removed, the drive fault line will be set and ...

If there are no jumpers installed or if both the exercise and delay jumpers are installed, then action halts.

If only the exercise jumper is installed, the microprocessor will restart.

Additonal Functions Of The Delay Jumper

In addition to changing the characteristics of the power-up sequence the delay jumper modifies the drive's behavior in normal operation. In particular, the drive will respond differently to seek commands depending upon the state of the delay jumper. This only applies when the exercise jumper is not installed.

a) If the delay jumper is not installed, the drive will ignore any outwardly directed step commands if the actuator is resting on track zero. If the actuator is not resting on track zero, however, and an outwardly directed buffered seek command which will result in a track destination less than zero is presented, the drive will attempt to perform the specified seek. This will usually cause the actuator to hit the outer crash stop and come to rest somewhere between track minus two and track ten.

b) If the delay jumper is installed, the drive will attempt to respond to any valid seek command and will not ignore outward seeks when resting on track zero. This allows the actuator to be positioned at tracks more outward than zero in order to align the crash stop during the drive assembly process. In addition, this is compatible to actuator response on the SA1000 product.

1.0 PURPOSE:

This procedure is to define the INCOMING TEST and INSPECTION requirements for Shugart SA600 Series/612 5.25 Fixed Disk Drives.

2.0 SCOPE:

This procedure is recommended to the Customer to assure compatibility and test correlation between the Customer and Shugart.

3.0 APPLICABLE DOCUMENTS :

3.1 Approved Vendor List (Customer)

3.2 Packaging Requirement Specification (Shugart)

3.3 Shugart's performance Specification as described in the 5.25 Inch Fixed Disk Drive Brochure #220000.

3.3.1 Description

3.3.2 Key Features

3.3.3 Performance Specifications

3.3.4 Functional Specifications

3.3.5 Physical Specifications

3.3.6 Reliability Specifications

3.4 Reference Vendor and Part History Records (Customer)

4.0 PACKAGING AND IDENTIFICATION:

4.1 Check individual and palleted containers for damage.

4.2 Each shipment shall contain a packing slip, listing as a minimum the Customer Purchase Order Number, Quantity, Customer Stock Number, Dash Number, and MLC Level.

4.3 Each item shall be individually protected as required - Reference Shugart's Packaging Specification.

4.4 Each container shall be clean and free of foreign matter.

5.0 INSPECTION AND TEST REQUIREMENTS:

5.1 Visual - Mechanical Inspection.

5.1.1. Check Model Number, Serial Number, and MLC Level.

5.1.2 Check for loose screws and sub-assemblies.

5.1.3 Check for loose connectors or missing jumpers.

5.1.4 Check for exposed wires on cables/connectors.

5.2 Functional Testing (Shugart Recommends the ADC T-650 Tester - with Level E3 Software - This Tester is a specially Programmed for all 5.25 and 8 Inch Fixed Disk Products.)

5.2.1 The functional Tests performed by the ADC Tester are as follows:

D = Prompt character and indicates the program's ready to accept commands from the user.

PP = Print Parameters

	604/606	612
Step Rate(X0.1MS) 30	30	30
Margin Code	7	7
Max Head	3	3
Step Mode	0	0
Max Cylinder	160	310
Max Error Cnt	0	0
Buffer Error Retry Limit	5	5
Precomp Start Cylinder	80	128
Low Write Current Start Cylinder	80	128

NOTE: The following EXAMPLE is a print out of the Test Program with the PRINTER Option for ADC.

```
WHICH PHASE? 0
MS/   4                          SET MARGIN CODE
TM/   1                          TEST MARGINS
P2/   1                          SET WORST CASE PATTERN
F1/   1                          FORMAT DISK DENSITY 1
WT/   1                          WRITE DATA INTEGRITY TEST
RT/   1                          READ DATA INTEGRITY TEST
RR/ 500                          RANDOM READ DATA TEST
RV/   1                          READ REVERSE TEST
WA/   1                          OVERWRITE TEST
RA/   1                          OVERREAD TEST
WC/   5                          WORST CASE SEEK TEST
TM/   1                          TEST MARGINS
HO/   1                          HOME THE DRIVE

PK/       182 (600 SERIES) 340 (612 DRIVE)    SET MAX CYLINDER
```

NOTE: The following EXAMPLE is a PRINT OUT of the test performed with the Printer option for the ADC T-650.

```
UNIT # 00  SERIAL #= AF3921          SA 600 SERIES

STEP RATE (X 0.1 MS)=1 EARLY MARGIN CODE = 3 LATE MARGIN CODE = 3
   MAX. HEAD = 3 STEP MODE =0  MAX CYLINDER=  150 MAX ERROR CNT=0
 BUFFER ERROR RETRY LIMIT=5  PRECOMP START CYLINDER=   80
   LOW WRITE I START CYLINDER=  128 DENSITY MODE=1 MFM 32*256
UNITS ONLINE= 0/
UNIT # 00  COUNT=    2   MULTI SIDED  MARGIN TEST
    UNIT # 00   MARGIN CODE=12. (24 NANO-SECONDS)     PASS TEST
    UNIT # 10   MARGIN CODE=12. (24 NANO-SECONDS)     PASS TEST
    UNIT # 20   MARGIN CODE=12. (24 NANO-SECONDS)     PASS TEST
    UNIT # 30   MARGIN CODE=12. (24 NANO-SECONDS)     PASS TEST
    UNIT # 40   MARGIN CODE=12. (24 NANO-SECONDS)     PASS TEST
    UNIT # 50   MARGIN CODE=12. (24 NANO-SECONDS)     PASS TEST
PARK DRIVE AT CYLINDER #   180

**********    END OF FINAL TEST ROUTINE.  TOTAL ERRORS =     0
**********  END OF MT LOOP #    1


                                     SA 612
  UNIT # 00  SERIAL #= BA2267

  STEP RATE (X 0.1 MS)=1 EARLY MARGIN CODE = 3 LATE MARGIN CODE = 3
     MAX. HEAD = 3 STEP MODE =0  MAX CYLINDER=  310 MAX ERROR CNT=0
   BUFFER ERROR RETRY LIMIT=5  PRECOMP START CYLINDER=   80
     LOW WRITE I START CYLINDER=  128 DENSITY MODE=1 MFM 32*256
  UNITS ONLINE= 0/
  UNIT # 00  COUNT=    2   MULTI SIDED  MARGIN TEST
      UNIT # 00   MARGIN CODE=12. (24 NANO-SECONDS)     PASS TEST
      UNIT # 10   MARGIN CODE=12. (24 NANO-SECONDS)     PASS TEST
      UNIT # 20   MARGIN CODE=12. (24 NANO-SECONDS)     PASS TEST
      UNIT # 30   MARGIN CODE=13. (26 NANO-SECONDS)     PASS TEST
  PARK DRIVE AT CYLINDER #   340

  **********    END OF FINAL TEST ROUTINE.  TOTAL ERRORS =     0
  **********  END OF MT LOOP #    1
```

NOTE: THE ABOVE TEST ON THE ADC T650 TESTER TAKES ABOUT 30 MINUTES PER DRIVE

5.2.2 The operation of the ADC T-650 is in the Operations Manual, which comes with the system.

SHUGART ASSOCIATES	CODE	PART NO.	REV EC
ENGINEERING SPECIFICATION	ES	030220-0	2337
		SHEET 1 OF 20	

TITLE FUNCTION SPECIFICATION

PRODUCT SA600

SA600 FUNCTION SPECIFICATION

PENDING
EC 5965 DATE
RFA ____ DATE
S/O ____ DATE

ORIGINATOR					APPROVAL					
EC NO	5529		2243		2337					
DATE	10-81		9/14/82		12/3/82					

TABLE OF CONTENT

I. GENERAL

A. DESCRIPTION

The SA600 series disk drives are 5 1/4 inch Winchester type direct access storage devices. The drives support the SA1000 type signal interface and have DC voltage requirements compatible to those of the SA400 series Minifloppy products. Each drive incorporates a disk spindle which is directly driven by a brushless DC motor, a stepper driven rotary band actuator, a double action spindle/actuator brake, a shock mounted baseplate and two printed circuit boards that contain the necessary read/write and control electronics.

B. PERFORMANCE SPECIFICATIONS

CAPACITY

Unformatted:

	SA602	SA604	SA606	Units
Per Drive	3.33	6.66	10.0	MBytes
Per Surface	1.66	1.66	1.66	MBytes
Per Track	10,416	10,416	10,416	Bytes

Formatted 33 sectors/track:

Per Drive	2.70	5.40	8.11	MBytes
Per Surface	1.35	1.35	1.35	MBytes
Per Track	8448	8448	8448	Bytes
Per Sector	256	256	256	Bytes

Formatted 32 sectors/track:

Per Drive	2.62	5.24	7.86	MBytes
Per Surface	1.31	1.31	1.31	MBytes
Per Track	8192	8192	8192	Bytes
Per Sector	256	256	256	Bytes

TRANSFER RATE: 5 Mbits/s

Access (seek + settle) times in buffered step mode:

Track to Track	16.2 ms
Average	95 ms
Maximum	205 ms

Access time is defined as the time between the falling edge of the last STEP pulse and the rising edge of the SEEK COMPLETE signal.

Average Latency: 8.33 ms

ERROR RATES:

Soft Read Errors	-	1 per 10^{10} bits read
Hard Read Errors	-	1 per 10^{12} bits read
Seek Errors	-	1 per 10^{6} seeks

C. FUNCTIONAL SPECIFICATIONS

Rotational Speed	3600 RPM
Recording Density	7900 bPI (7900 FCI)
Track Density	256 TPI
*No. of Data Cylinders	160
No. of Data Tracks:	SA602-320 SA604-640 SA606-960
No. of R/W Heads:	SA602- 2 SA604- 4 SA606- 6
No. of INDEX per rev.:	1
Data Encode Method:	MFM
Write Precompensation:	Required from cyl. 128 thru 159
Reduced Write Current:	Required from cyl. 128 thru 159

*Shipping zone at cylinder 182

D. ENVIRONMENTAL SPECIFICATIONS

	Operating	Storage/Shipping
Ambient Temperature	50°F to 115°F (10°C to 46°C)	-40°F to 140°F (-40°C to 60°C)
Relative Humidity	8% to 80%	1% to 95%
Maximum Wet Bulb	78°F non condensing	Non Condensing
Temperature Gradient	10°F/ 1/2 Hr. (5.5°C/ 1/2 Hr.)	Below that which can cause condensation
Relative Humidity Variance	20%/Hr	Below that which can cause condensation
Elevation	0 to 6000 ft (0 to 1828 meters)	-1000 to +12,000 ft (-305 to +3656 meters
Vibration	TBD	TBD
Shock	TBD	TBD
Ambient Magnetic Field	TBD	TBD
EMI Compatibility	TBD	TBD

DC Voltage Requirements

+ 12V DC	± 5%	1.8 A Typical,	4.0A Max
+ 5V DC	± 5%	1.8 A Typical,	2.0A Max

E. RELIABILITY

MTBF: 8000 POH Typical Usage
PM : None required
MTTR : 30 Minutes
Component Life : 5 Years

F. MECHANICAL

Height: 3.38 in. (85.9 mm)
Width: 5.88 in. (149.4 mm)
Depth: 8.19 in. (208.0 mm)
Weight: 4 lbs (1.8 kg)
Mounting Configurations:

(i) Horizontal - R/W PCB at bottom
(ii) Vertical - on either side of 8 inch dimension horizontal.

Refer to Figure 1 for detail dimensions and mounting hole locations.

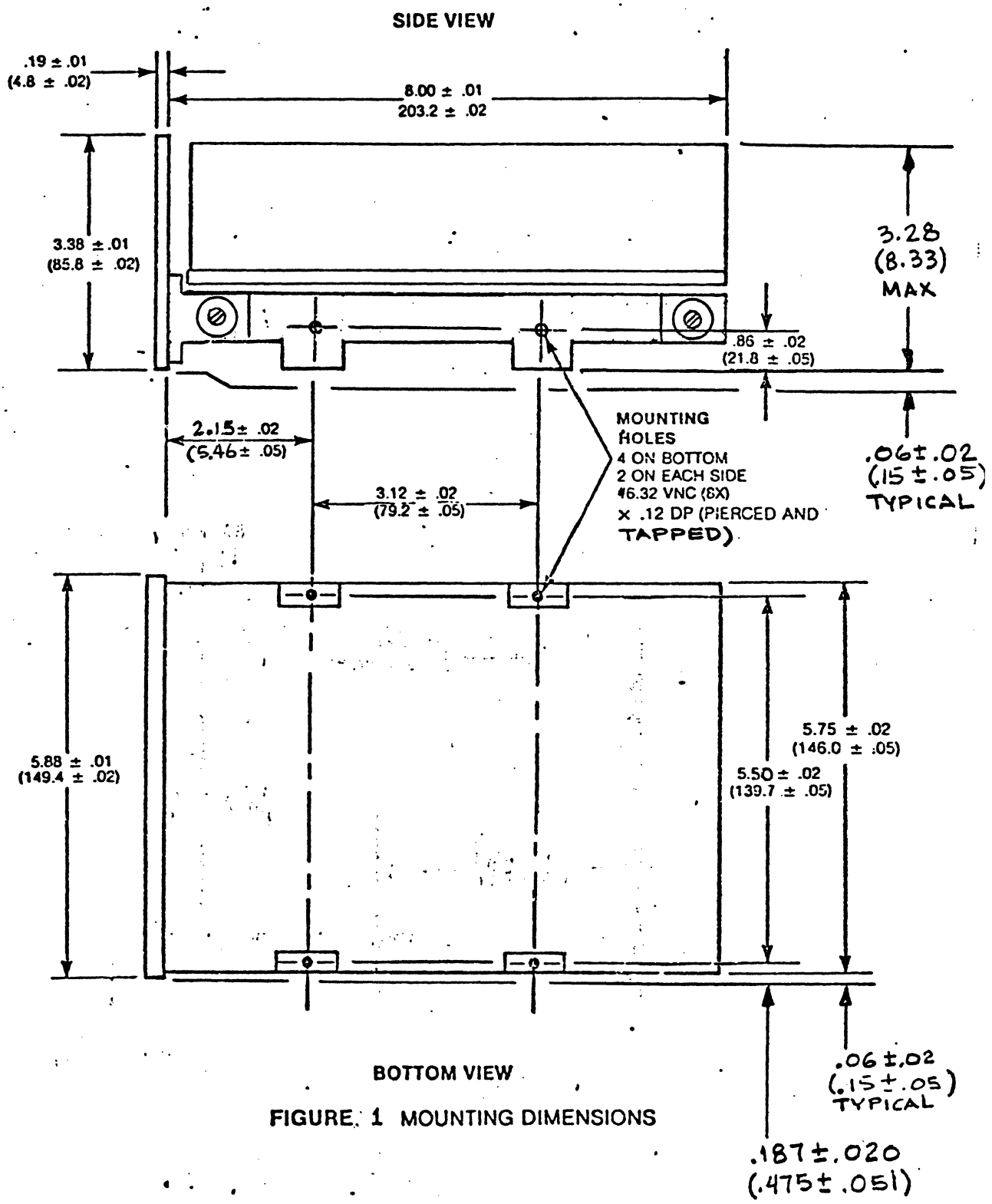


FIGURE 1 MOUNTING DIMENSIONS

II. POWER INTERFACE

A. FRAME GROUND

The baseplate is electrically insulated from the mounting brackets by virtue of the rubber shock mounts. The baseplate is connected to the DC common of the R/W PCB. AC grounding of the baseplate is accomplished by one of two ways:

(i) The DC Returns (Commons) of the +12V and +5V lines are tied to the AC ground at the power supply.

(ii) Attach separate ground wire (AWG 18 or larger) to ground lug on top side of baseplate in the vicinity of the J2 connector.

B. DC POWER (J6/P6)

1. Pin Assignment (See Figure 2)

Pin #	Designation
1	+12V
2	+12V Return
3	+ 5V Return
4	+ 5V

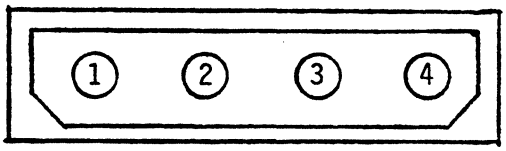


Figure 2 P6 Front View

2. Power Requirement

DC Voltage at Drive	Current Typ.	Current Max	Max Ripple (p-p)
+12V ± .60 v	1.8A	4.0 A	250 mV
+ 5V ± .25 v	1.0A	1.5A	50 mV

3. Cable Length/Wire Size

Max Length	Min Wire Size
20 ft twisted	AWG 18

4. Connector Requirement

J6 Socket (on PCB) : AMP P/N 641734
P6 Plug Housing : AMP P/N 1-480424-0
P6 Pins (4x) : AMP P/N 61473

III. SIGNAL INTERFACE

A. PIN ASSIGNMENT

Refer to Figure 3 for pin assignment on the J1/P1 and J2/P2 cables. The J1 port supports daisy chaining to a maximum of four drives per cable. The 220/330Ω terminator network located near J1 on the PCB should be removed except for the last drive in the chain. See Figure 4 for typical system configuration.

J1/P1			J2/P2		
G*	S*	SIGNAL NAME	G*	S*	SIGNAL NAME
1	2	-REDUCED WRITE CURRENT	2	1	-DRIVE SELECTED
3	4	-HEAD SELECT 2^2	4	3	SPARE
5	6	-WRITE GATE	6	5	SPARE
7	8	-SEEK COMPLETE	8	7	SPARE
9	10	-TRACK 000	10	9	SPARE
11	12	-FAULT	12	11	GND
13	14	-HEAD SELECT 2^0		13	+MFM WRITE DATA
15	16	RESERVED		14	-MFM WRITE DATA
17	18	-HEAD SELECT2^1	16	15	GND
19	20	-INDEX		17	+MFM READ DATA
21	22	-READY		18	-MFM READ DATA
23	24	-STEP	20	19	GND
25	26	-DRIVE SELECT 1			
27	28	-DRIVE SELECT 2			
29	30	-DRIVE SELECT 3			
31	32	-DRIVE SELECT 4			
33	34	-DIRECTION IN			

*G = GROUND PIN
*S = SIGNAL PIN

Figure 3A J1,J2 PIN ASSIGNMENT

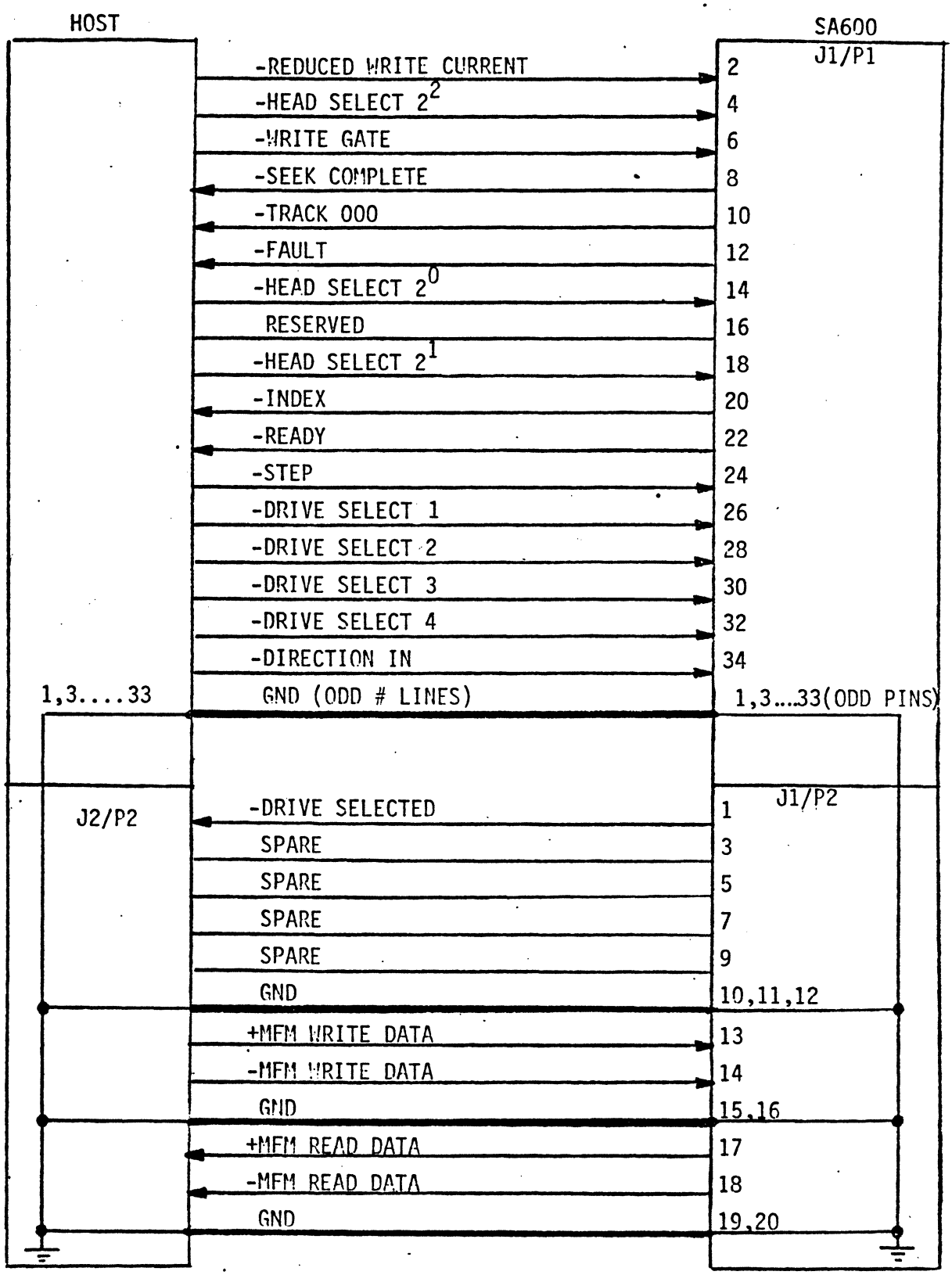
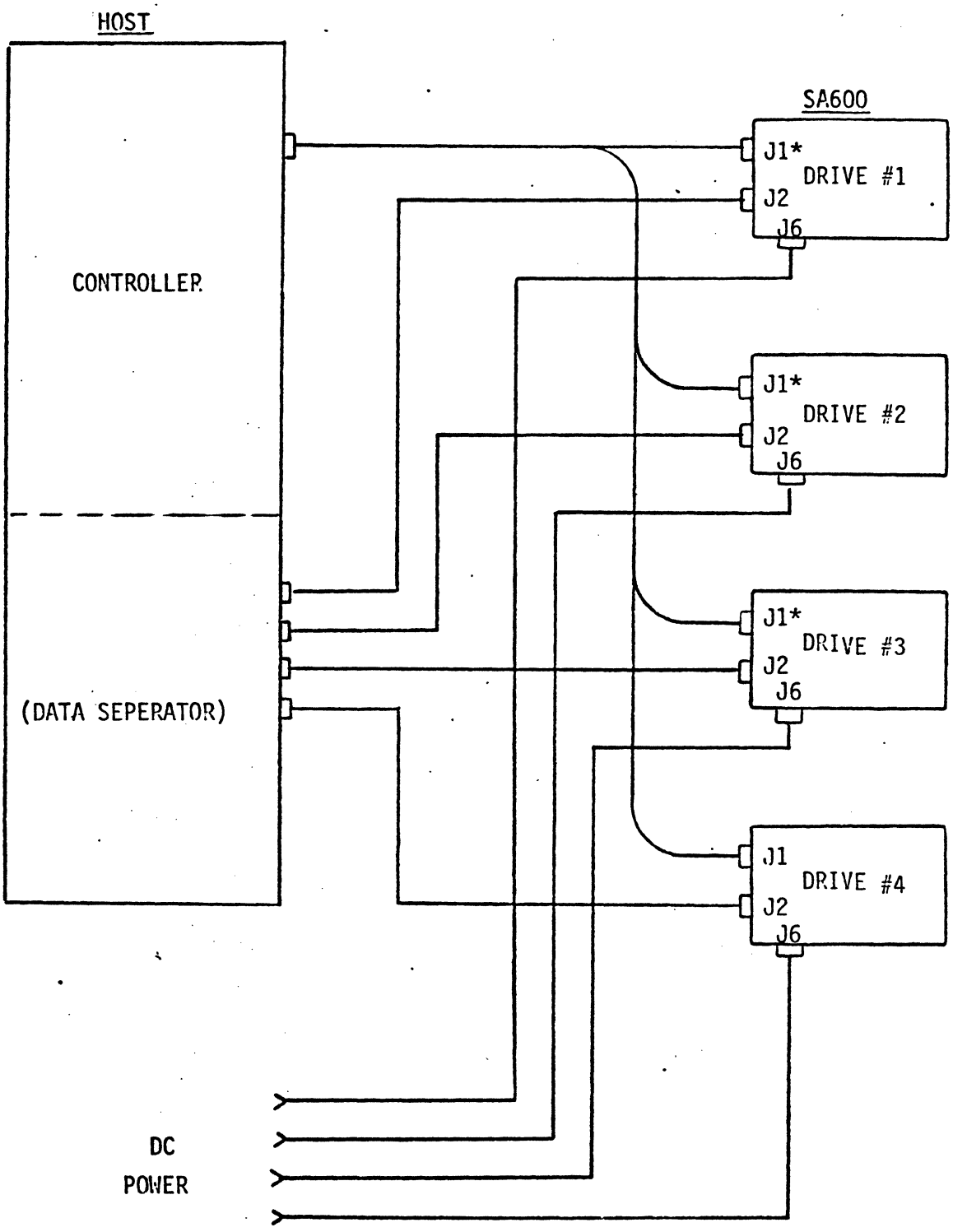


Figure 3B J1, J2 SIGNAL FLOW



*TERMINATOR NETWORK REMOVED

Figure 4. TYPICAL 4-DRIVE SUBSYSTEM

B. CONNECTOR ATTACHMENT

The following lists the typical connector and cable which can be used to connect a drive to a controller.

Port	Connector	Cable	
J1	3M 3463-0001	3M 3365/34	(20 ft max)
J2	3M 3461-0001	3M 3365/20	(20 ft max)

C. CONTROL INPUT LINES (J1/P1)

These are lines that carry control information from the host system to the drive via the multiplexer cable. Each line should be driven by a 7438 type open collector driver, and is terminated at the drive by a 220Ω/330Ω resistor combination as shown in Figure 5. 7414 type Schmitt triggered receivers are used at the input.

Electrical Parameters:

At Driver		At Receiver	
I_{OL} = 40 mA	Max	I_{IL} = -1.6 mA	Min
V_{OL} = .40 v	Max	V_{IL} = .40 v	Max
		I_{IH} = 250 uA	Max
		V_{IN} = 2.0 v	Min

Note: TRUE = Logic Zero = .40 v max, FALSE = Logic One = 2.0 v min.

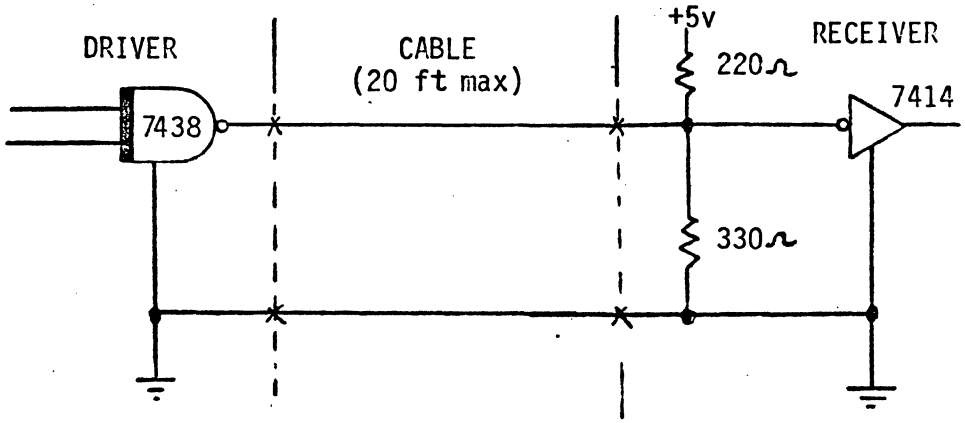


Figure 5 J1/P1 SIGNAL DRIVERS/RECEIVERS

The following paragraphs describe the functions and timings of each control input line.

DRIVE SELECT 1 to 4

DRIVE SELECT, when true, connects the drive to the control lines. Only one DRIVE SELECT may be active at a time.

Jumper options DS1, DS2, DS3, and DS4 are used to program the drive to respond to the respective DRIVE SELECT lines.

DIRECTION IN

This signal defines the direction of motion of the read/write heads when the STEP line is pulsed. An open circuit or logical false, defines the direction as "out" and if a pulse is applied to the STEP line, the read/write head will move away from the center of the disk. If the input is shorted to ground, or logical true, the direction of motion is defined as "in" and if a pulse is applied to the STEP line, the read/write heads will move towards the center of the disk.

A removable 220/330Ω resistor pack, located near the P1 connector, provides input line termination.

STEP

This line causes the read/write heads to move in the direction as defined by the DIRECTION IN line. Any change in the DIRECTION IN line must be made at least 100 ns before the trailing edge of the step pulse. Stepping can be performed in either the Normal or Buffered mode:

Normal Step Mode - In this mode, the read/write heads will move at the rate of the incoming step pulses. Motion is initiated at each true to false transition. The minimum time between successive steps in 3.0ms, with a minimum pulse width of 500 ns. Refer to Figure 6.

Buffered Step Mode - In this mode, the step pulses are received at a high rate and buffered into a counter. After the last step pulse, the read/write heads will begin stepping the desired number of cylinders and SEEK COMPLETE will go true after the read/write heads settle on the cylinder. This mode of operation is automatically selected when the time between step pulses is less than 200 µsec. Refer to Figure 7 for timing requirements.

500 ns after the last step pulse has been sent to the drive, the DRIVE SELECT line may be dropped and a different drive selected.

The maximum time between steps is 200 µs with a minimum pulse width of 500 ns(Refer to Figure 7).

Shipping Zone - The read/write heads can be accessed to the shipping zone by doing a seek to TRK 182.

NOTES: 1. Step pulses with periods between 200 µs and 3.0ms are not permitted. Seek accuracy is not guaranteed if this timing requirement is violated.

2. SEEK COMPLETE may not go false until 500 ns after the true to false transition of THE STEP pulse.

3. A removable 220/330Ω resistor pack, located near the P1 connector, allows for STEP line termination.

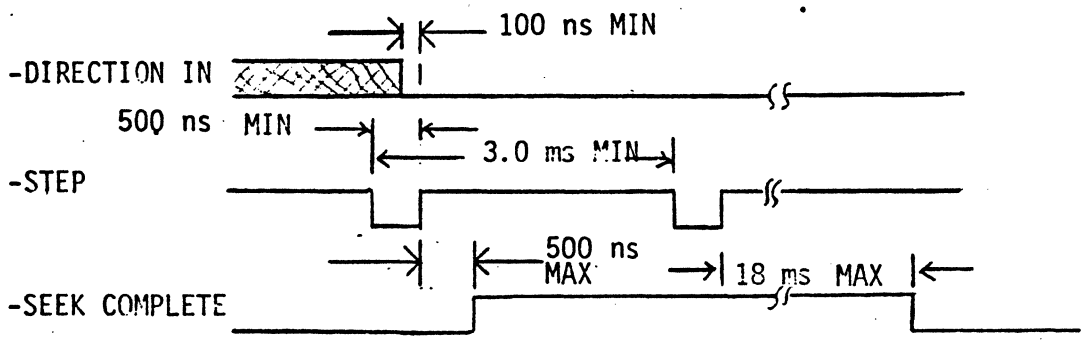


FIGURE 6 NORMAL STEP MODE

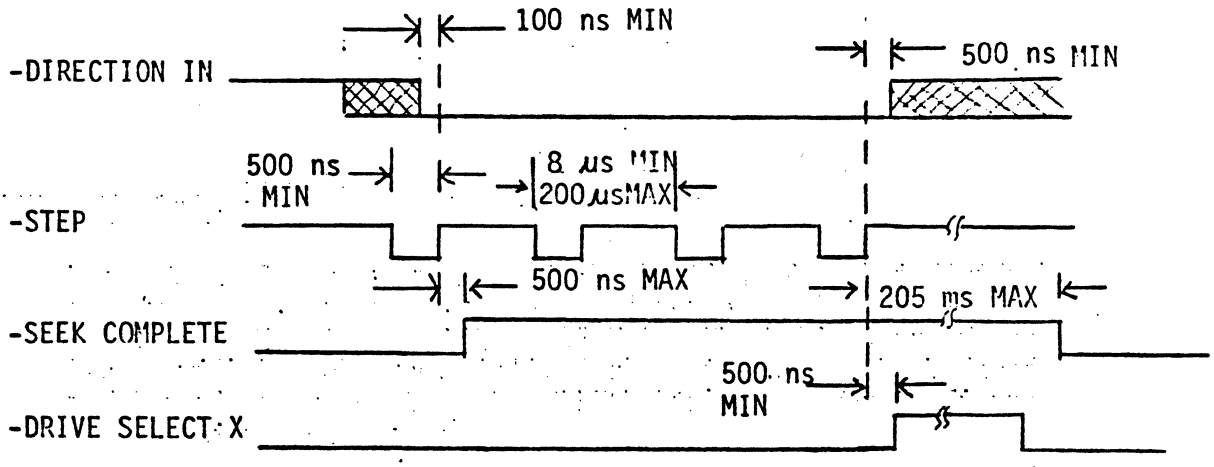


Figure 7 BUFFERED STEP MODE

HEAD SELECT 2^0, 2^1, 2^2

These three lines provide for the selection of each individual read/write head in a binary coded sequence. HEAD SELECT 2^0 is the least significant line. When all HEAD SELECT lines are false, head 0 will be selected. Table 1 shows the HEAD SELECT decode and model variations for the HEAD SELECT lines. (Refer to Figure 8 for the timing sequences).

HEAD SELECT LINE			HEAD SELECTED	HEAD SELECTED	HEAD SELECTED
2^2	2^1	2^0	SA602	SA604	SA606
1	1	1	0	0	0
1	1	0	1	1	1
1	0	1	---	2	2
1	0	0	---	3	3
0	1	1	---	---	4
0	1	0	---	---	5

Table 1. HEAD SELECT (1 = False, 0 = True)

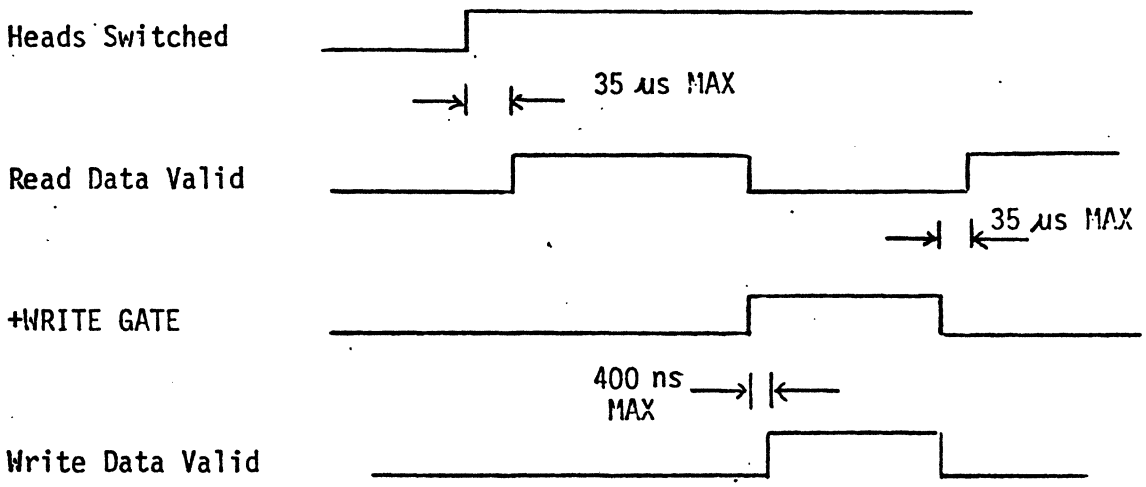


Figure 8. HEAD SELECTION TIMING

WRITE GATE

The active state of this signal (logical zero level) enables WRITE DATA to be written onto the disk. The inactive state of the signal (logical one level) enables data to be transferred from the drive and enables STEP pulses to reposition the head arm. (Refer to Figure 8 for the timing sequences).

A removable 220/330Ω resistor pack, located near the P1 connector, allows for termination of these lines.

REDUCED WRITE CURRENT

When this interface signal is low (true) the lower value of Write Current is selected (for writing on cylinders 128 through 159). When this signal is high (false), the higher value of Write Current is selected (for writing on cylinder 0 through 127). A removable 220/330Ω resistor pack, located near the P1 connector, allows for line termination.

D. CONTROL OUTPUT LINES (J1/P1)

These are the lines on the J1 port which carry status information back to the host (see Figure 3). They have the same electrical parameters and driver/receiver configurations as those described for Control Input lines.

TRK000

This signal, when true, indicates that the read/write heads are positioned (but not necessary settled) at the outermost data track (track zero). SEEK COMPLETE line should be used in conjuction for read/write purposes. This signal is used primarily to facilitate a recalibration process.

INDEX

The drive provides this interface signal once each revolution (16.67 ms) to indicate the beginning of the track. Normally, this signal is a logical one (false) and makes the transition to logical zero (true) for a period of approximately 10 µs once each revolution. Refer to Figure 10.

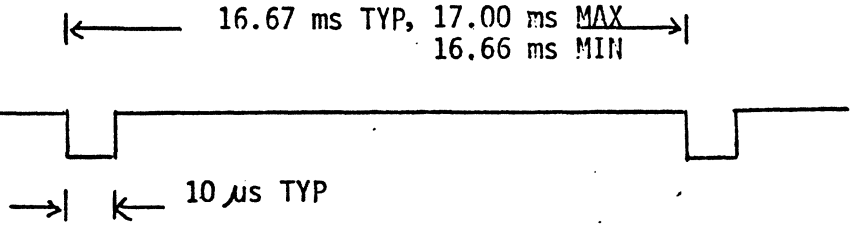


Figure 10. INDEX TIMING

READY

This interface signal when true (logical zero), together with SEEK COMPLETE, indicates that the drive is ready to read, write, or seek and that the signals are valid. When this line is false (logical one), all writing to the disk and seeking is inhibited at the drive.

Ready will be true after the drive is 95 ± 2% up to speed (3348 - 3492 rpm's). The typical time for READY to become true after power on, is 12 seconds. It is now safe to seek the drive, but an

additional 2 minutes should be allowed for thermal expansion to stabilize, before any write operations are performed.

FAULT

This signal, when true, indicates one or more of the following conditions:

(i) Unsafe write current in the read/write heads.

(ii) More than one read/write head is selected.

(iii) Microprocessor sequence error.

Under a fault condition, all writing is inhibited at the drive. If the fault is transient in nature, it can be reset by dropping the SELECT line to the drive. A FAULT caused by condition (iii) above cannot be reset by deselection. A DC power on is necessary to restart the microprocessor.

SEEK COMPLETE

This signal, when true, indicates that the read/write heads have settled on a track. Read/write operations may be initiated if heads are over a valid data track.

Caution: This line may not go false until after 500 ns after the first false to true transition on the STEP line. See Figures 6 and 7.

The SEEK COMPLETE line will remain false at DC power on until an automatic recalibration sequence is complete at the drive.

DATA TRANSFER LINES (J2/P2)

Data transfer is handled by two pairs of differential signals connected radially from the host to the drive at the J2/P2 connector. Pin assignment is given in Figure 4. The driver/receiver combination is given in Figure 10.

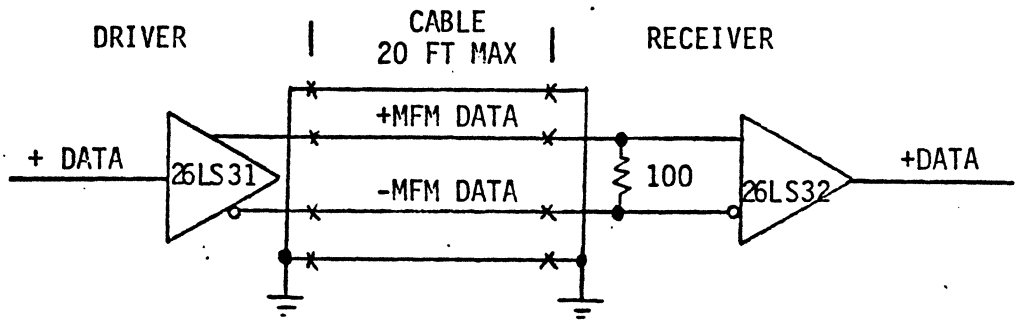


Figure 10. DATA TRANSMITTER/RECEIVER COMBINATION

MFM WRITE DATA

This pair of signals defines the transitions (bits) to be written on the disk. +MFM WRITE DATA going more positive than -MFM WRITE DATA will cause a flux reversal on the track under the selected head providing WRITE GATE is active. This signal must be driven to an inactive state (+MFM WRITE DATA) by the host system when in the read mode. Figure 11 shows the timing for MFM WRITE DATA.

MFM READ DATA

The data recovered by reading a pre-recorded track is transmitted to the host system via the differential pair of MFM READ DATA lines. This transition of the +MFM READ DATA line going more positive than -MFM READ DATA line represents a flux reversal on the track of the selected head while WRITE GATE is inactive. Refer to Figure 11.

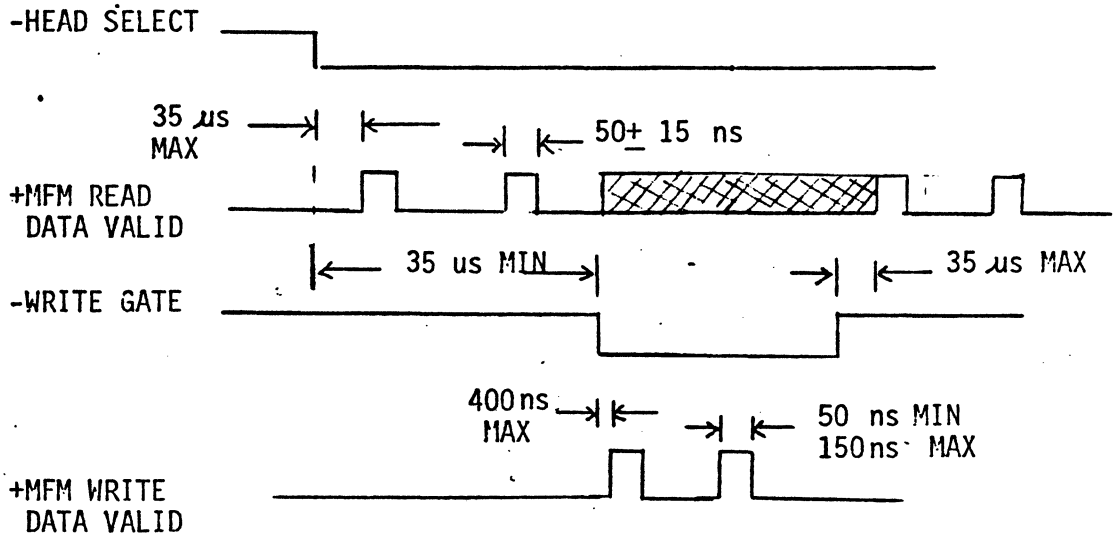


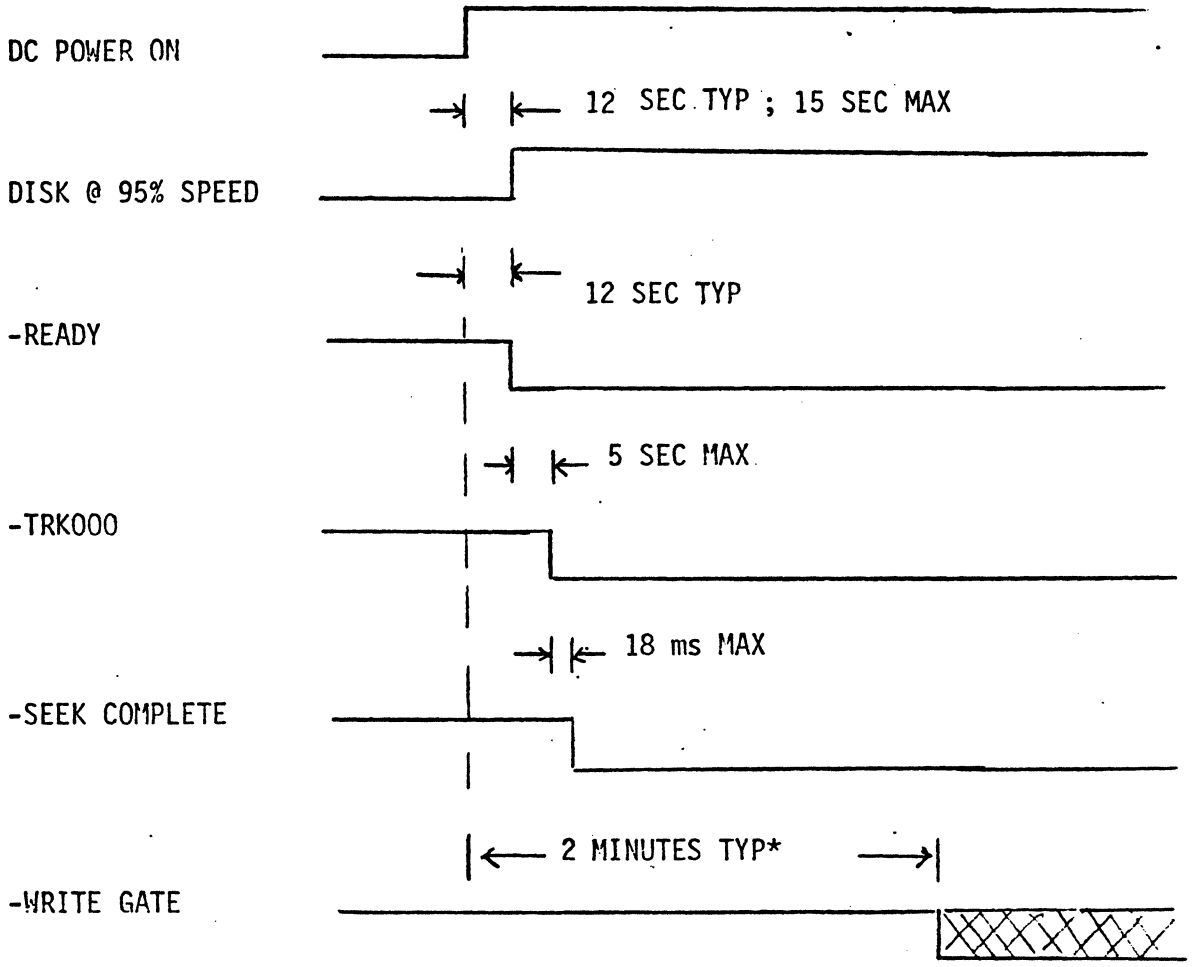
Figure 11. MFM READ/WRITE DATA TIMING

E. SELECT STATUS (J2/P2)

Selection status of a drive is provided by the radial connector J2. The DRIVE SELECTED line is driven by a 7438 type open collector driven as that shown in Figure 5. This line will go true only when the DRIVE SELECT X line is activated by the host, and that the DS jumper on the drive is plugged into the X position (X = 1,2,3 or 4).

F. GENERAL TIMING REQUIREMENTS

The timing diagram in Figure 12 shows the typical sequence of events of a selected drive at DC power on.



*A warm up period of 2 minutes is recommended before any write operation is performed.

Figure 12. GENERAL TIMING

IV. PRINTED CIRCUIT BOARD

A. FABRICATION

Two printed circuit boards (PCB) are used in an SA600. The Read / Write PCB contains the necessary user interface. This PCB is mounted on the bottom side of the drive, with the component side facing down, and the signal and power interface connectors at the read end of the drive. The Control PCB contains the microprocessor control circuitry and does not have any user interface. Outline drawings for the Read/Write and Control PCB's are given in Figures 13 and 14 respectively.

B. CONNECTOR INTERFACE

To be specified.

V. SPECIFICATION SUMMARY

A. READ CHANNEL

Output @ I.D.	Ship/Verify	Field
Linear (J50-3-J50-4)		
1F	290 ± 95 mV p-p	290 ± 105 mV p-p
2F	190 ± 75 mV p-p	190 ± 85 mV p-p
Total (JP3-TP4)		
1F	3.8 $^{+\ 2.0\ V\ p\text{-}p}_{-\ 1.2\ V\ p\text{-}p}$	3.8 $^{+2.0\ V\ p\text{-}p}_{-1.2\ V\ p\text{-}p}$
2F	4.8 $^{-\ 1.2\ V\ p\text{-}p}_{+\ 3.2\ V\ p\text{-}p}$	4.8 $^{-1.2\ V\ p\text{-}p}_{+3.2\ V\ p\text{-}p}$
Resolution (min)	62%	60%
Max 1F Asymmetry (cyl Ø and 159)	20 ns	25 ns
Min Droop (1F)	1.5 V	1.5 V
Read Recovery	30 µs max	35 µs MAX
Max 2F Modulation	15%	20%
Min Window Margin	34%	32%

B. WRITE CHANNEL

Current (p-p)		
O.D. ($\leq$ Tk 127)	50 ± 6 mA	50 ± 8 mA
I.D. ($>$ Tk 127)	45 ± 6 mA	45 ± 8 mA
MFM Write Precompensation	12 ± 3 ns	12 ± 3 ns
Write turn off	1.0 µs Max	1.0 ± .5µs

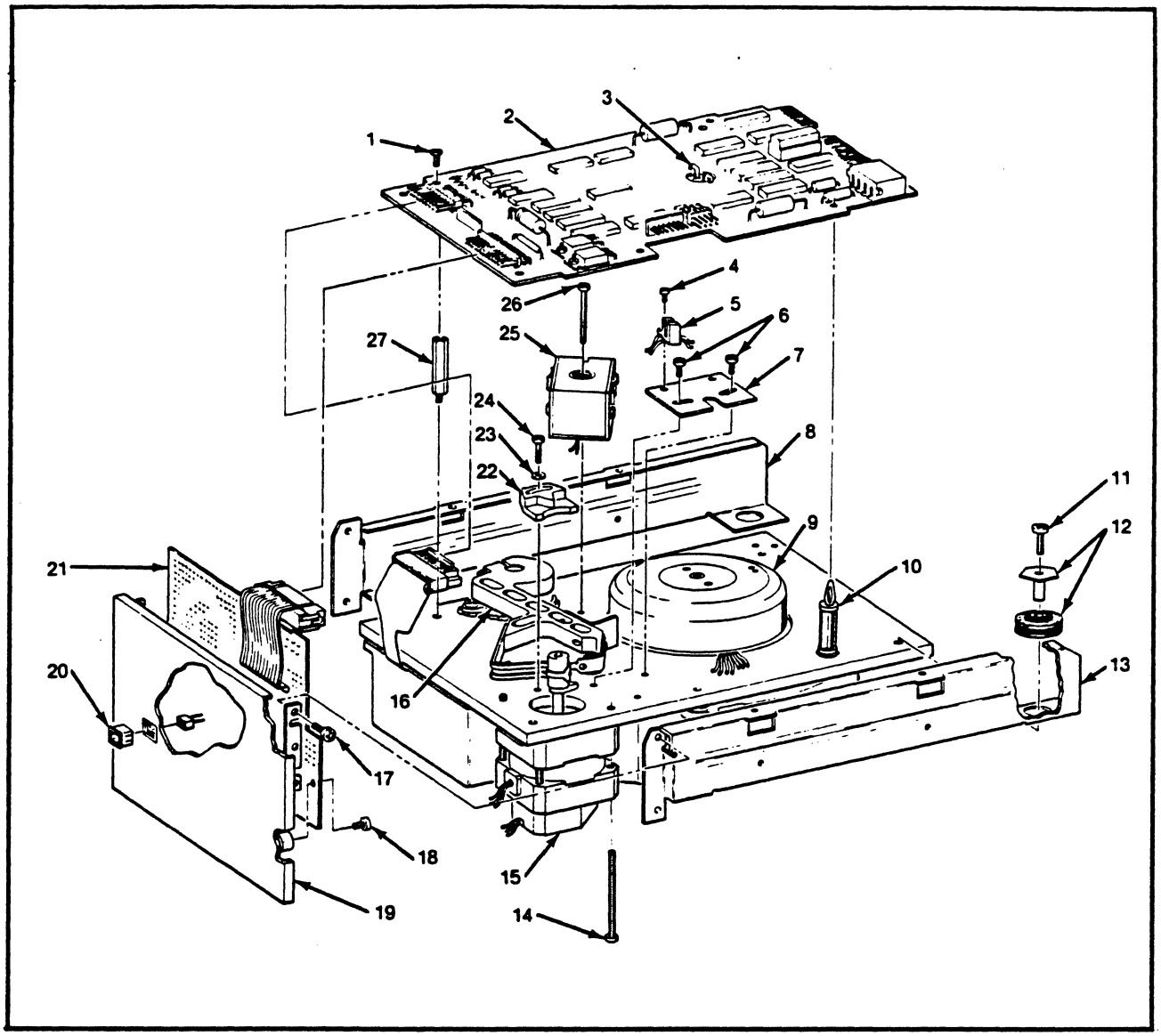
C. ACCESS TIMES (SEEK & SETTLE)

Track to Track	16.2 ms MAX	16.2 ms MAX
Average (53-tracks)	94 ms MAX	99 ms MAX
Maximum (159 tracks)	201 ms MAX	215 ms MAX

D. MECHANICAL

Particle Count	Class 100

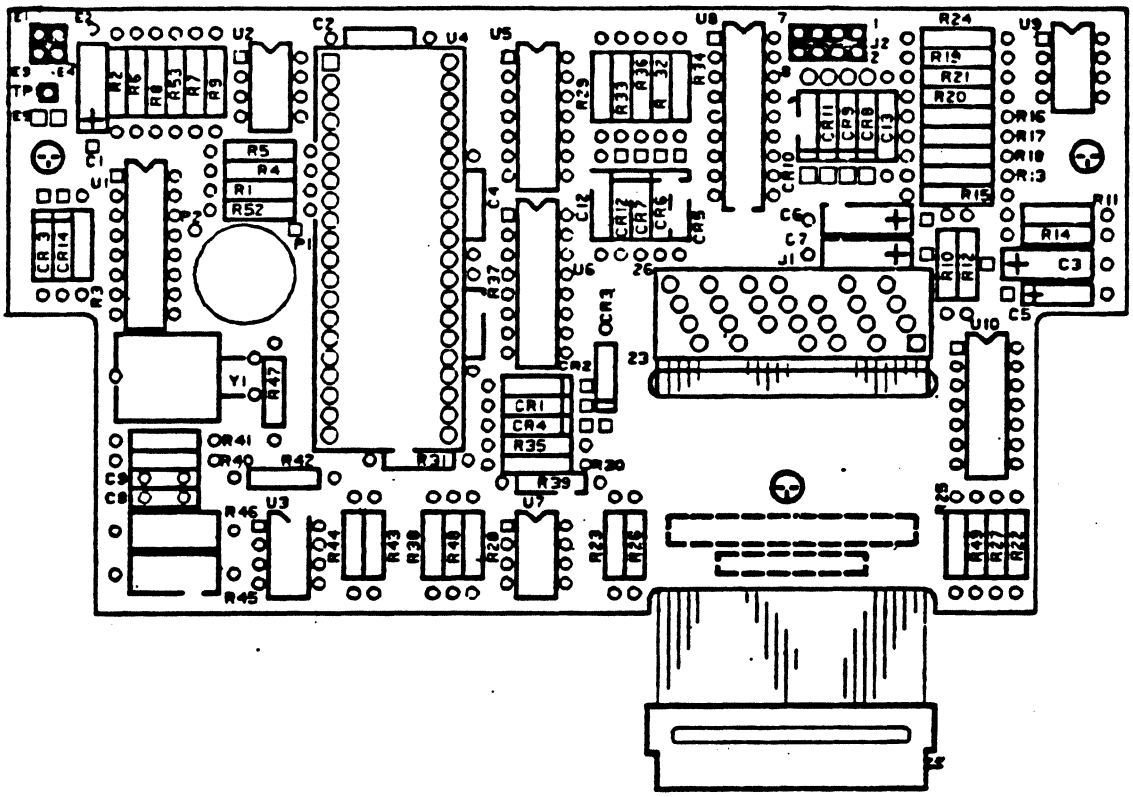
	Ship/Verify	Field
E. MEDIA		
Hard Errors	TBD	



SA612 ILLUSTRATED PARTS BREAKDOWN (MLC-5)

SA612 PARTS LIST (MLC-5)

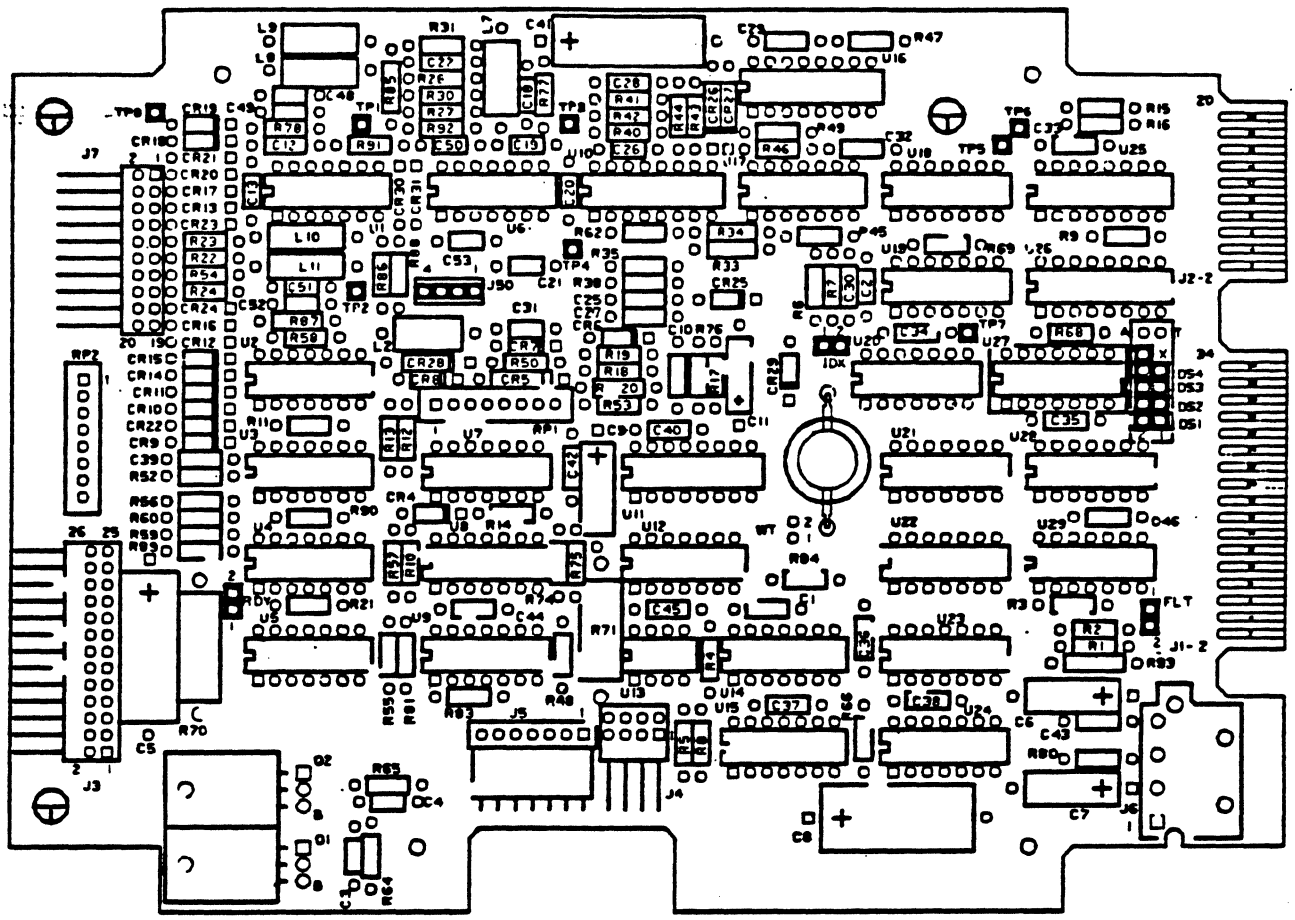
REFERENCE NUMBER	PART NUMBER	DESCRIPTION	QTY PER ASM
1	12087-0	SCREW, Phillips 6-32 × 1/4"	1
2	26145-1	READ/WRITE PCB, Assembly	1
3	60847-0	GROUND BUTTON, Assembly	1
4	10261-0	SCREW, Phillips 4-40 × 1/4"	1
5	17403-0	OPTICAL SWITCH	1
6	12087-0	SCREW, Phillips 6-32 × 1/4"	2
7	60278-1	PLATE OPTICAL SWITCH MOUNTING	1
8	61514-0	BRACKET MOUNTING, Left	1
9	60758-1	DC DRIVE MOTOR	1
10	61525-0	STANDOFF, PCB Nylon	3
11	12237-0	SCREW, Phillips 6-32 × 5/8"	4
12	11223-0	MOUNT SHOCK	4
13	61515-0	BRACKET MOUNTING, Right	1
14	12236-0	SCREW, Phillips 6-32 × 1 7/16"	2
15	61113-1	STEPPER MOTOR	1
16	61122-1	ACTUATOR ARM, Assembly	1
17	12087-0	SCREW, Phillips 6-32 × 1/4"	4
18	12105-0	SCREW, Phillips 4-40 × 3/16"	2
19	60820-1	COVER, Front	1
20	15926-0	GROMMET and RING	1
21	26149-2	CONTROL PCB, Assembly	1
22	60856-0	CRASH STOP, Full Step	1
23	10013-0	WASHER	1
24	12101-0	SCREW, Phillips 6-32 × 7/16"	1
25	61524-0	BRAKE, Double-acting	1
26	12238-0	SCREW, Phillips 6-32 × 15/16"	1
27	60773-0	STANDOFF, PCB	1



SA612 CONTROL PCB, ASSEMBLY

SA612 CONTROL PCB, PARTS LIST

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION	QTY PER ASM
C2,4	15080	CAP, 0.1 μF, +80, 20%, 50 V	2
C5	15122	CAP, 0.068 μF, 10%, 35 V	1
C12,13	15070	CAP, 0.0015 μF, 10%, 50 V	2
C8,9	15040	CAP, .22 μF, 10%, 50 V	2
C1,3,6,7	15086	CAP, 4.7 μF, 20%, 50 V	4
W1	10432	CABLE, Ribbon (26 Conductor)	2.5
P3	17719	CONN, Socket	1
J1	19178	CONN, 26 Pos.	1
J1	61116	CONN, Cover	1
Y1	15705	CRYSTAL, 4 MHz	1
CR1-7,12,13	10062	DIODE, 1N4148	9
CR8-11	15900	DIODE, 1N4003	4
CR14	15908	DIODE, 1N5221B, 5%, 2.4 V	1
U5	10051	IC, 7406	1
U1	12692	IC, 74161	1
U3,7,9	12682	IC, LM358A	3
U2	12673	IC, LM393N	1
U8	12665	IC, UDN2981	1
U10	12693	IC, CD4066B	1
U6	16267	IC, ULN2074B	1
U4	61119-1	IC, Custom IC Chip	1
XU4-1-40	17761	PCB INSERTED IC SOCKET PINS	40
R53	16738	RES., 47 K, 5%, ¼ W	1
R45,46	16956	RES., 1.8 Ω, 1%, ¼ W	2
R1,2	16832	RES., 180 Ω, 5%, ¼ W	2
R3-5,9,29-37	10108	RES., 1 K, 5%, ¼ W	13
R11	16953	RES., 1.8 K, 5%, ¼ W	1
R10,19-21,24	10109	RES., 2 K, 5%, ¼ W	5
R12,13,28	16859	RES., 2.7 K, 5%, ¼ W	3
R14	16779	RES., 3.3 K, 5%, ¼ W	1
R40,41	10111	RES., 4.7 K, 5%, ¼ W	2
R38,39	10113	RES., 10 K, 5%, ¼ W	2
R15-18	16931	RES., 270 K, 5%, ¼ W	4
R22,23,26,26, 48,49	16722	RES., 100 K, 5%, ¼ W	6
R27	16856	RES., 1.1 K, 5%, ¼ W	1
R8	16822	RES., 1 M Ω, 5%, ¼ W	1
R6	16829	RES., 10 K, 1%, 1/8 W	1
R7	16921	RES., 13.3 K, 1%, 1/8 W	1
R42,44	16954	RES., 23.7 K, 1%, 1/8 W	2
R47,43	16955	RES., 681 K, 1%, 1/8 W	2
R52	17003	RES., 100 K, 1%, 1/8 W	1



SA612 READ/WRITE PCB, ASSEMBLY

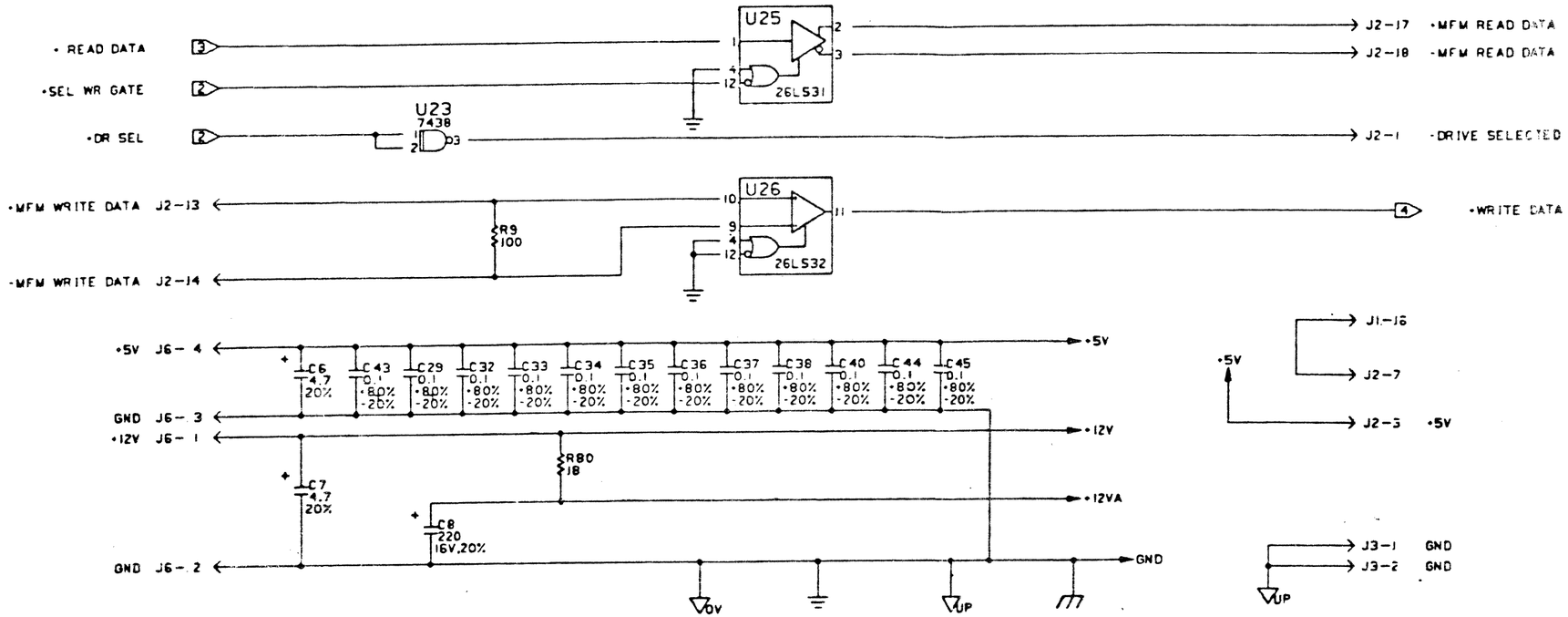
SA612 READ/WRITE PCB, PARTS LIST

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION	QTY PER ASM
C10-13,19,22, 25,27,28,29, 32-38,40, 43-45	15080	CAP, 0.1 UF, +80-20%, 50 V	20
C2-4,20,21,31, 50,53	15073	CAP, Cer., 0.1 UF, 10%, 50 V	8
C30,42	15074	CAP, Cer., .015 UF, 10%, 50 V	2
C51	15053	CAP, Cer., 62 PF, 5%, 50 V	1
C26	15101	CAP, Cer., 10 PF, 5%, 50 V	1
C52	15059	CAP, Cer., 270 PF, 5%, 50 V	1
C18	15061	CAP, Cer., 330 PF, 5%, 50 V	1
C48	15145	CAP, Cer., 75 PF, 5%, 50 V	1
C1,39,46	15067	CAP, Cer., 1000 PF, 5%, 50 V	3
C49	15105	CAP, Cer., 390 PF, 5%, 50 V	1
C11	10088	CAP, Tant, 1.0 UF, 10%, 35 V	1
C6,7,9	15125	CAP, Aluminum Electrolytic, 4.7 UF, 20%, 50 V	3
C5,8,41	15092	CAP, Filter, 200 UF, 20%, 16 V	3
XU27	15672	CONN, IC (Dip) 14 Pin	1
J7	17758	CONN, Header 20 Pos., Right Angle Double	1
J3	17757	CONN, Header 26 Pos., Right Angle Double	1
J4	17759	CONN, 8 Pos. Angle Double Row	1
J6	17752	CONN, Header (Right Angle Mount)	1
J5	17778	CONN, Header (Right Angle 7 Pos.)	1
CR4,6-24,29-31	10062	DIODE, 1N4148	23
CR25	15902	DIODE, 1N5231, Zener, 5.1 V	1
CR26,27	15928	DIODE, 1N5232, Zener, 5.6 V	2
CR28	15929	DIODE, 1N5234, Zener, 6.2 V	1
CR5	15927	DIODE, 1N5239, Zener, 9.1 V	1
L7	16323	INDUCTOR, Molded, 1 μH, 10%, Shielded	1
L11	16322	INDUCTOR, Molded, 18 μH, 10%, Shielded	1
L8	16307	INDUCTOR, Molded, 4.7 μH, 10%, Shielded	1
L2,9	10082	INDUCTOR, Molded, 22 μH, 10%	2
L10	16306	INDUCTOR, Molded, 3.3 μH, Shielded	1
U18	16273	IC, 74LS00	1
U12,22	16274	IC, 74LS02	2
U9	10051	IC, 7406	1
U14	12681	IC, 74LS08	1
U21	12603	IC, 74LS10	1
U15,20,28	16258	IC, 7414	3
U23,29	16207	IC, 7438	2
U11	16280	IC, 7445	1
U17	16281	IC, 74S74	1
U19,24	16203	IC, 7474	2
U16	16213	IC, 74123	1
U10	10055	IC, 8T20	1
U1,6	12723	IC, NE592 Burn-in	2
U4	12678	IC, CA3046 Transistor Array	1
U13	12648	IC, 75454 (Dual Peripheral Driver)	1
U25	12679	IC, 26LS31	1
U26	12680	IC, 26LS32	1
R74,75	17092	RES., 255 Ω, 1%, 1/8 W	2
R20	16700	RES., Fixed, 825 Ω, 1%, 1/8 W	1
R85,87	17023	RES., Fixed 332 Ω, 1%, 1/8 W	2
R22,33,34,54	16708	RES., Fixed, 1.50 K, 1%, 1/8 W	4
R27,28	17091	RES., 174 Ω, 1%, 1/8 W	2

SA612 READ/WRITE PCB, PARTS LIST (CONT.)

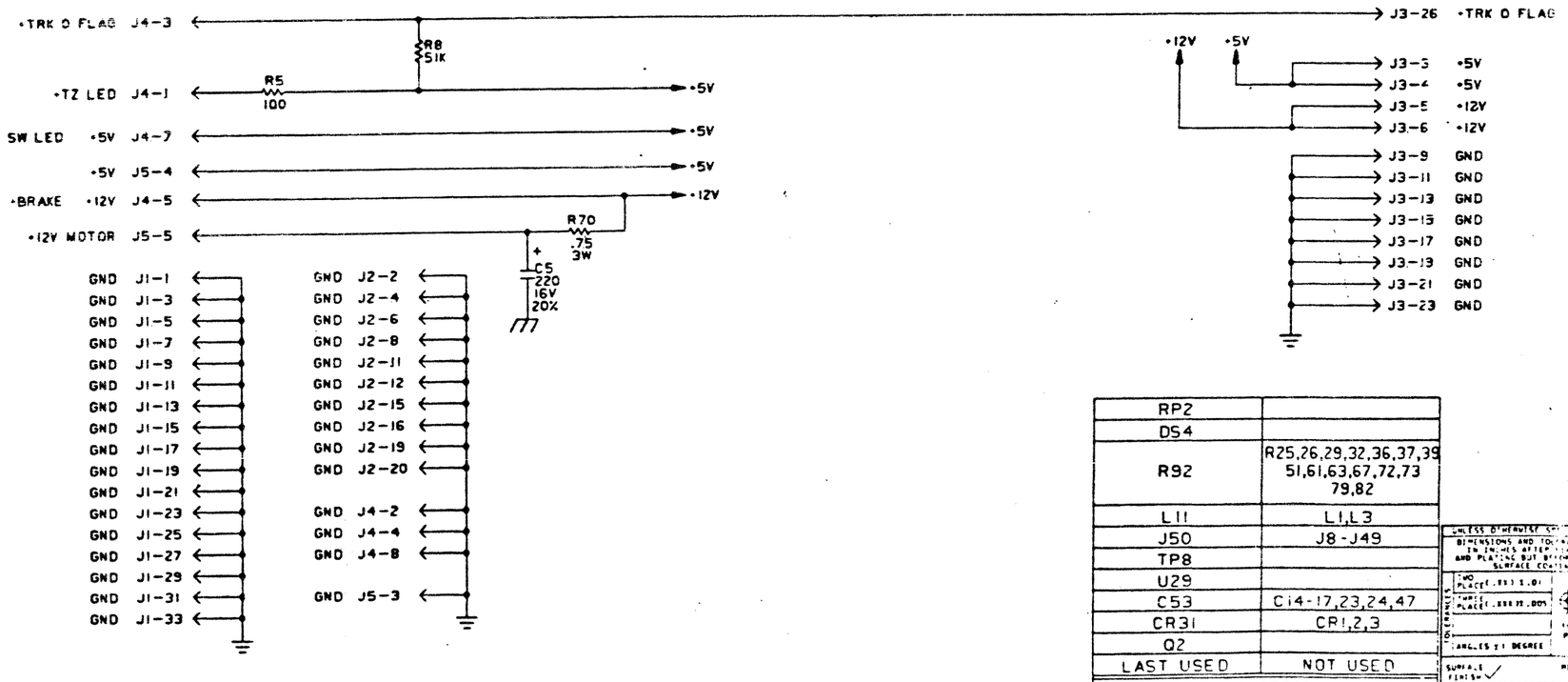
REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION	QTY PER ASM
R38	16774	RES., Fixed, 24 Ω, 5%, ¼ W	1
R78	16732	RES., Fixed, 10 Ω, 5%, ¼ W	1
R80	16791	RES., Fixed, 18 Ω, 5%, ¼ W	1
R50,77	16826	RES., Fixed, 68 Ω, 5%, ¼ W	2
R5,9	10102	RES., Fixed, 100 Ω, 5%, ¼ W	2
R58,12	16777	RES., Fixed, 150 Ω, 5%, ¼ W	2
R1	10103	RES., Fixed, 220 Ω, 5%, ¼ W	1
R14,43,44	16741	RES., Fixed, 270 Ω, 5%, ¼ W	3
R2,30,31	16838	RES., Fixed, 330 Ω, 5%, ¼ W	3
R13	16749	RES., Fixed, 390 Ω, 5%, ¼ W	1
R17	10105	RES., Fixed, 430 Ω, 5%, ¼ W	1
R64,65	16824	RES., Fixed, 470 Ω, 5%, ¼ W	2
R35	10106	RES., Fixed, 510 Ω, 5%, ¼ W	1
R55,59,11	16750	RES., Fixed 620 Ω, 5%, ¼ W	3
R21	10107	RES., Fixed, 560 Ω, 5%, ¼ ²	1
R6,16,41,42,45, 46,48,52,62, 66,68,81,83, 19,7	10108	RES., Fixed, 1 K Ω, 5%, ¼ W	15
R15,23,24	16773	RES., Fixed 1.5 K Ω, 5%, ¼ W	3
R84	10131	RES., Fixed, 22 K Ω, 5%, ¼ W	1
R91,92	16772	RES., Fixed, 39 K Ω, 5%, ¼ W	2
R3,56,57,60	10109	RES., Fixed, 2 K Ω, 5%, ¼ W	4
R53	16859	RES., Fixed, 2.7 K Ω, 5%, ¼ W	1
R18,69,76,86,88	10117	RES., Fixed, 3 K Ω, 5%, ¼ W	5
R4	16779	RES., Fixed, 3.3 K Ω, 5%, ¼ W	1
R40,47,49	16768	RES., Fixed, 5.1 K Ω, 5%, ¼ W	3
R10,89,90	16760	RES., Fixed, 6.2 K Ω, 5%, ¼ W	3
R8	16836	RES., Fixed, 51 K Ω, 5%, ¼ W	1
U5	16936	RES., Network 1.0 K (Dip)	1
U7	16937	RES., Network 4.7 K (Dip)	1
U277	16837	RES., Pack 220 Ω/330 Ω	1
RP2	16962	RES., Network 2 K (Sip), 8 Pin	1
RP1	16963	RES., Network 10 K (Sip), 8 Pin	1
R70	16959	RES., Fixed, 0.75 Ω, 5%, 3 W	1
R71	16961	RES., Fixed, 35 Ω, 5%, 3 W	1
U2,3	16240	QUAD TRANS., PNP Q2T2905	2
U8	16241	QUAD TRANS., NPN Q2T2222	1
Q1,2	17628	TRANS., Power, Tip 120	2
TP1-8,J50(1-4), RDY1-2, FLT1-2, DS1-4, X,IDX1-2	17756	TERM, Post (.025 Sq.) 0.235 Long	27
	11337	RIVET	2
DS1	15648	PLUG, Shorting	1
	60847	GROUND BUTTON, Assembly	1

REVISIONS				
REV	EC	DESCRIPTION	DATE	APPROV
A	5943	PRODUCTION RELEASE	2-17-83	



NOTES
UNLESS OTHERWISE SPECIFIED:

1. ALL CAPACITOR VALUES ARE IN MICROFARADS, 50V, ±10%
2. ALL DIODES ARE IN4148.
3. ALL INDUCTOR VALUES ARE IN MICROHENRIES, ±10%.
4. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
5. ALL TRANSISTORS ARE ———.
6. 1□—□2 INDICATES CUT TRACE OPTION.
7. 1□ □2 INDICATES JUMPER OPTION.
8. ▷ DENOTES OFF-SHEET CONNECTION.



RP2	
DS4	
R92	R25,26,29,32,36,37,39 51,61,63,67,72,73 79,82
L11	L1,L3
J50	J8-J49
TP8	
U29	
C53	C14-17,23,24,47
CR31	CR1,2,3
Q2	
LAST USED	NOT USED
REFERENCE DESIGNATION	

CA3046	U4		—	—
7474	U19,24	U19-1	14	7
Q2T2222	U8		—	—
26LS32	U26		16	8
26LS31	U25		16	8
220/330	U27		14	7
74LS00	U18		14	7
74LS10	U21		14	7
7414	U15,20,28	U15-6,12	14	7
7438	U23,29		14	7
74S74	U17		14	7
74123	U16		16	8
74LS08	U14		14	7
75454	U13		8	4
74LS02	U12,22	U22-13	14	7
7445	U11		16	8
8T20	U10		—	4
7406	U9		14	7
R,DIP(1K)	U5		14	—
R,DIP(4.7K)	U7		—	—
Q2T2905	U2,3		—	—
NE592	U1,6		—	5
TYPE	POSITION	SPARE GATE (OUTPUT PIN)	VCC	GND

IC TABLE

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS AND TOLERANCES ARE IN INCHES AFTER PLATING AND PLACING BUT BEFORE ORGANIC SURFACE COATINGS
TWO PLACE ± .03 I.D.
THREE PLACE ± .005 .005
ANGLES ± 1 DEGREE
SURFACE FINISH ✓
MICROINCHES
DO NOT SCALE DRAWING COPY

USED ON
OA 026145

PREP	CMOD	7-6-82
CHK		
APPD		
APPD		
APPD		

SHUGART ASSOCIATES

READ/WRITE, PCB,SCH

SIZE	DRAWING NO.	REV	EC
D	SC 026145-1	A	5943

SCALE 1/1 | SA612 | SHEET 1 OF 4

-DRIVE SEL 1 J1-26
-DRIVE SEL 2 J1-28
-DRIVE SEL 3 J1-30
-DRIVE SEL 4 J1-32
-STEP J1-24
-WRITE GATE J1- 6
-HEAD SEL 2-0 J1-14
-HEAD SEL 2-1 J1-18
-HEAD SEL 2-2 J1- 4
•IW SENSE
•MULTI HD
-DIRECTION J1-34
RESERVED J1- 2
•FAULT J3- 7
-CLR FLT J3-24
•SEEK COMP J3-22
•TRK 000 J3-20
•READY J3-18
V REF
PU 2
HALL 2 J5-1
HALL 1 J5-2
-MTR INH J3-8
-BRAKE J4-6

•HD 2-0
•HD 2-1
•HD 2-2
J3-14 •SELECT
J1-20 -INDEX
•DR SEL
-DR SEL
J1- 8 -SEEK COMP
J1-22 -READY
J1-10 -TRK 000
J1-12 -FAULT
-SEL WR GATE
-SEL WR GATE
•SEL WR GATE
J3-16 -G STEP
J3-12 •DIRECTION
REDUCED IW
•REDUCED IW
J3-25 REDUCED IW
J3-10 •INDEX
J5- 6 MOTOR A
J5- 7 MOTOR B

SIZE	DRAWING NO.	REV	EC
D	SC 026145-1	A	5949
SCALE 1/1	SA612	SHEET 2 OF 4	

SEE SHEET 1 FOR REVISION LEVEL

- SEL WR GATE 4
- DATA 4
- DATA 4
- READ DATA 1
PU 2 2
- HEAD 0 J7-5
- HEAD 0 J7-7
- HEAD 1 J7-11
- HEAD 1 J7-13
- HEAD 2 J7-17
- HEAD 2 J7-19
- HEAD 3 J7-16
- HEAD 3 J7-18
- HEAD 4 J7-10
- HEAD 4 J7-12
- HEAD 5 J7-4
- HEAD 5 J7-6
J7-1
J7-2
SELECT WIDE 4
SELECT NARROW 4
J50-3 - LINEAR
J50-2 + LINEAR
J50-1 GND
J50-4 GND

U9 7406 R48 1K TP5 U18 74LS00
+5V R49 5.1K U16 74123 CX RX CLR Q
U17 10 7474 D S Q CR
R45 1K +5V
+5V R47 5.1K U16 74123
+12V R38 24 C25 .01 +80-20% R62 1K C41 220 16V 20% R35 510
C26 10PF 5% R40 5.1K U10 8T20 PEC NEC -IN -IN CLR VEE VR VCC A Q
R41 1K R42 1K CR27 IN5232 CR26 IN5232 C28 .01 +80-20% R43 270 R44 270
+12VA R77 68 1/4W 5% C19 .1 +80-20% U6 NE592 C20 .01 C21 .01 L7 C18 330PF 50V 5%
TP3 TP4
R34 1.50K 1/8W 1% R33 1.50K 1/8W 1% C27 .1 +80-20% CR25 IN5231
CR17 CR9 CR13 CR23 CR12 CR16 CR14 CR15 CR10 CR11 CR18 CR19 CR20 CR21 CR22 CR24
R54 1.50K 1% R22 1.50K 1% R23 1.5K R52 1K C39 1000PF 5% R24 1.5K
TP8
+12VA R78 10 C13 .1 +80-20% C12 .1 +80-20% U1 NE592
TP1 TP2
R85 332 1% CR30 IN4148 R91 39K L8 4.7 L9 22 C48 75PF C49 390PF
R87 332 1% CR31 IN4148 R92 39K L10 3.3 L11 18 C51 62PF C52 270PF R88 3K
C50 .01 C53 .01 R86 3K
R28 174 1/8W 1% R30 330 R27 174 1/8W 1% R31 330 C22 .1 +80-20%

SIZE	SC 026145-1	REV	EC
D		A	5949
SCALE 1/1	SAGIZ	SHEET 3 OF 4	