SCD-DLV11J/8P

8-Channel Programmable Interface

Manual

Sigma Information Systems

MA400265 REV B

VDLAB0 PATCH

ERROR	LOCATION / CONTENTS	PATCH	
#10,3464	003562 / 001401	000401	READER ENABLE

SCD-DLV11J/8P

8-Channel Programmable Interface Manual

CORRECTIONS

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~~GARYS~~	~~26-FEB-87~~	~~11~~
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ANAHEIM, CALIFORNIA - OCTOBER 1984

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Section 1 - General Information

1.1 INTRODUCTION

This manual supplies the information needed to install and operate the SCD-DLV11J/8P 8-channel serial line interface module manufactured by Sigma Information Systems, Anaheim, California. The material is arranged into the following sections:

SECTION 1 - GENERAL INFORMATION. This section contains a general description of the interface module, along with features. Specifications are included.

SECTION 2 - INSTALLATION. This section contains the switch selection and associated register formats for device and vector address assignments, baud rates and line parameters. Cabling and backplane installation is included.

SECTION 3 - PROGRAMMING CONSIDERATIONS. This section contains the address/vector formats and register formats for transmit and receive control/status and buffer registers.

APPENDIX A - The appendix lists the bus signals and their associated pin assignments.

APPENDIX B - This appendix contains a complete list of address and vector switch settings for address/vector assignments.

1.2 GENERAL DESCRIPTION

The SCD-DLV11J/8P is a dual-wide asynchronous interface between the LSI-11 bus and up to eight standard serial I/O devices. It is software compatible with DEC* operating systems and diagnostics designed for the DLV11J. It plugs directly into any dual Q bus* slot.

Sigma's SCD-DLV11J/8P has switch selectable address (160000 to 177776) and vector (000 to 776) assignments. Once the initial address and vector are assigned, all eight channels are contiguous except the console channel which, if selected, resides at 177560 with vector at 60.

All channels share a programmable baud rate with a switch selectable default value. Baud rates range from 50 to 19.2K buad. The SCD-DLV11J/8P supports only RS-232C devices with all channels sharing switch selectable line parameters.

The interface module requires two 12-foot, 4-channel cables, each terminating with four DB25P connectors. An optional rackmount panel provides convenient mounting for the eight DB25P connectors.

1.3 FEATURES

The following are some of the features of the SCD-DLV11J/8P.

- Eight asynchronous serial lines can be supported on one dual-wide module.
- The module is plug compatible with LSI-11 backplanes and plugs directly into any Q bus slot without backplane modification.
- The interface is software compatible with operating systems and diagnostics designed for the DLV11J.
- Baud rate is programmable with a switch selectable default value.
- Device address and vector assignments are switch selectable.
- Line parameters are switch selectable.

*DEC and Q bus are registered trademarks of Digital Equipment Corporation.

1.4 SPECIFICATIONS

Power Requirements:	+5VDC AT 2.0A +12VDC at 0.2A
Device Address:	Switch selectable 160000-177776 (Console = 177560)
Vector	Switch selectable 000-776 (console = 60)
Baud Rate:	Programmable per channel: 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 3400, 3600, 4800, 7200, 9600 and 19.2K
Line Parameters:	Switch selectable. Shared by all channels
Data Bit:	7 or 8
Parity:	Odd, even or none
Stop Bit:	1 or 2
Operation:	Full duplex
Interface Type:	RS-232C
Bus Load:	One DC load
Optional Cables:	Requires two 12-ft, 4-channel cables, each terminated with four DB25P connectors. Terminals require null modem cable with DB25S to SCD-DLV11J/8P's terminated connectors.
Optional Panel:	Mounts the eight DB25P connectors for convenient rear rackmount cabling to RS-232C devices.
Installation:	Plugs directly into any standard Q bus slot that provides continuous BIAK1 and BIAK0 lines.
Dimensions:	Single dual-wide module: 5.2"W x 8.9"H (13.2cmW x 22.8cmH)
Temperature	
Operating:	0°C to 50°C
Storage:	-40°C to 85°C
Humidity:	10% to 90% noncondensing

Section 2 - Installation

2.1 UNPACKING AND INSPECTION

The SCD-DLV11J/8P is shipped in a special packing carton designed to keep the module from vibrating and to give it maximum protection during shipment. The packing carton should be retained in case the unit requires reshipment.

Unpack the SCD-DLV11J/8P and visually inspect it for any damage that may have occurred during shipment. If any damage has occurred notify Sigma Information Systems immediately.

2.2 FACTORY-SET PARAMETERS

The SCD-DLV11J/8P is shipped configured with DEC standard operating parameters as defined in Table 2-1. The location of the switches that determine these parameters is shown in Figure 2-1.

Before installing modules, verify that these configurations are properly selected. The following sections describe the procedures to verify and/or reconfigure these operating parameters.

PARAMETER	STATUS
Device Address	176500
Vector Interrupt	300
Baud Rate	9600
Console	
Channel 7	Enabled
Address	177560
Word Format	
Character Length	8 bits
Parity	Disabled
Stop Bits	1
CTS Bias	+12V

TABLE 2-1: FACTORY-SET PARAMETERS

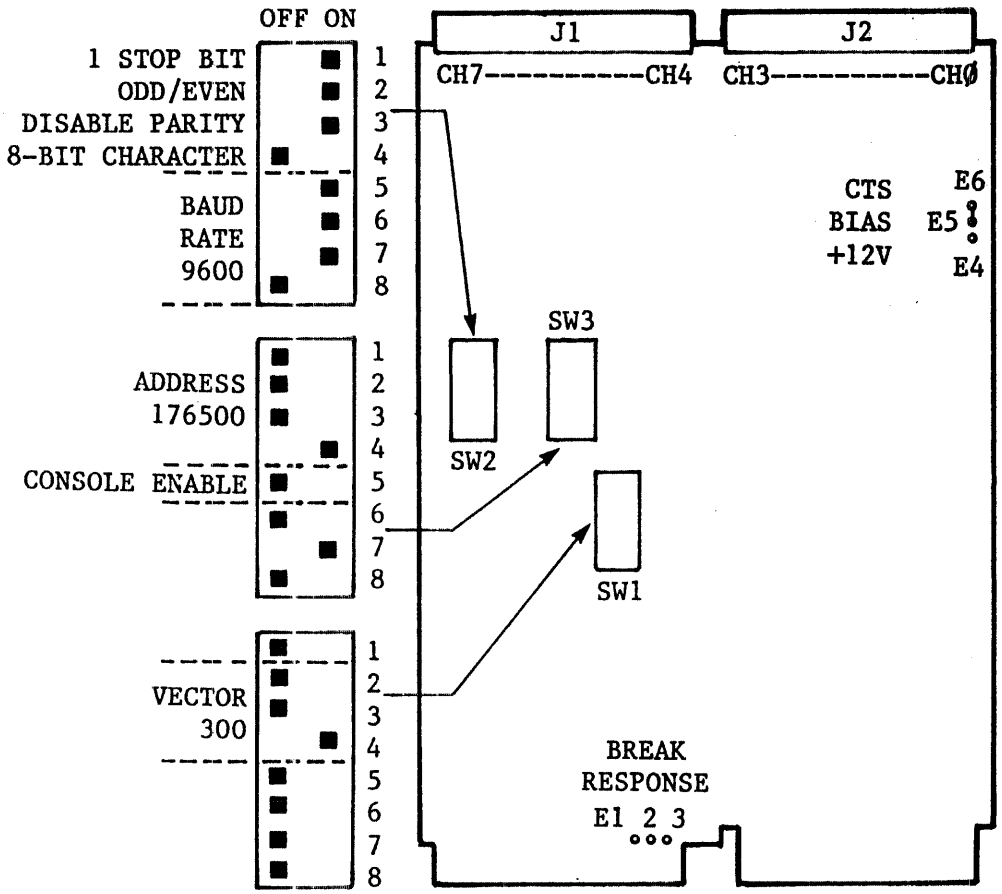
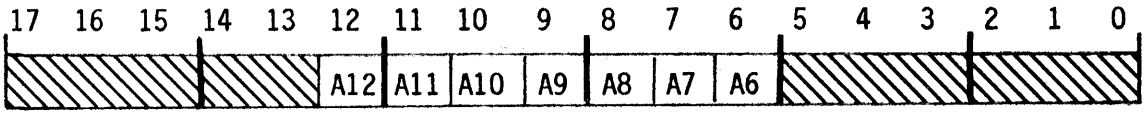


FIGURE 2-1: FACTORY CONFIGURATIONS

2.3 ADDRESS SELECTION

The SCD-DLV11J/8P has switch selectable device addressing in the range of 160000 to 177776 (octal). Once an initial address is assigned, the remaining seven channels are contiguous except the console which, if selected, resides at 177560 as channel 7. Refer to Section 3.1 for a description of the device address and vector interrupt assignments. The initial address format is shown below.



Use the following examples to set SW3. Notice that OFF = 1 and ON = 0.

Set default standard address 176500.

ADDRESS BITS:		A12	A11	A10	A09	A08	A07	A06
SW3 POSITIONS:		1	2	3	4	8	7	6
SW3 SETTINGS:		OFF	OFF	OFF	ON	OFF	ON	OFF
SW3 VALUE:		1	1	1	0	1	0	1
ADDRESS:	1	7		6			5	0

Set address 176400.

ADDRESS BITS:		A12	A11	A10	A09	A08	A07	A06
SW3 POSITIONS:		1	2	3	4	8	7	6
SW3 SETTINGS:		OFF	OFF	OFF	ON	OFF	ON	ON
SW3 VALUES:		1	1	1	0	1	0	0
ADDRESS:	1	7		6			4	0

EXAMPLE 2-1: ADDRESS SELECTION

A complete list of address switch settings is shown in Appendix B.

2.4 VECTOR SWITCH SELECTION

The SCD-DLV11J/8P has switch selectable vector assignments in the range of 000-776 (octal). Once the initial vector is assigned the remaining seven vectors are contiguous except the console which, if assigned, resides at 60 as channel 7. The initial vector format is shown below.

Use the following examples to set SW1. Notice that OFF = 1 and ON = 0.

Set standard default vector 300.

VECTOR BITS:	V8	V7	V6		
SW1 POSITIONS:	4	3	2		
SW1 SETTINGS:	ON	OFF	OFF		
SW1 VALUES:	0	1	1		
VECTOR INTERRUPT:		3		0	0

Set vector 200.

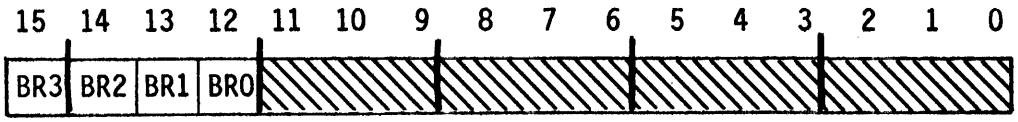
VECTOR BITS:	V8	V7	V6		
SW1 POSITIONS:	4	3	2		
SW1 SETTINGS:	ON	OFF	ON		
SW1 VALUES:	0	1	0		
VECTOR INTERRUPT:		2		0	0

EXAMPLE 2-2: VECTOR INTERRUPT SELECTION

A complete list of vector interrupt switch settings is shown in Appendix B.

2.5 BAUD RATE SELECTION

All channels share the same programmable baud rate. The baud rate format is shown below.



where BR0-BR3 define programmable baud rates and SW2 defines switch selectable baud rates as shown in Table 2-2.

BAUD RATE	†XCSR BITS 15	14	13	12	
	SW2 POSITIONS 5	6	7	8	
50	ON	ON	ON	ON	004200
75	ON	ON	ON	OFF	014200
110	ON	ON	OFF	ON	024200
134.5	ON	ON	OFF	OFF	034200
150	ON	OFF	ON	ON	044200
200	ON	OFF	ON	OFF	054200
300	ON	OFF	OFF	ON	064200
600	ON	OFF	OFF	OFF	074200
1200	OFF	ON	ON	ON	104200
1800	OFF	ON	ON	OFF	114200
2400	OFF	ON	OFF	ON	124200
3600	OFF	ON	OFF	OFF	134200
4800	OFF	OFF	ON	ON	144200
7200	OFF	OFF	ON	OFF	154200
9600*	OFF	OFF	OFF	ON	164200
19.2K	OFF	OFF	OFF	OFF	174200

†OFF = 0, ON = 1 → OFF = 1, ON = 0
*Factory preset

TABLE 2-2: BAUD RATE SELECTION

If programmable baud rate is enabled (XCSR bit 11 is set), the XCSR bits 15-12 override SW2 baud rate selection. See Section 3.4.3 for programmable baud rate selection.

2.6 LINE PARAMETERS SWITCH SELECTION

All eight channels share the same line parameters. The start bit is 1, but data bit, parity and stop bits can be assigned via switch SW2 as shown in Table 2-3.

LINE PARAMETER	SW2 POSITION	DEFINITION
Character Length	4	ON = 7 bits *OFF = 8 bits
Parity Enable	3	*ON = disable parity OFF = enable parity
Parity Type	2	ON = odd parity OFF = even parity
Stop bits	1	*ON = 1 stop bit OFF = 2 stop bits

*Factory preset

TABLE 2-3: LINE PARAMETERS SWITCH SELECTION

2.7 CONSOLE SELECTION

The console, if selected, is assigned channel 7. The SCD-DLV11J/8P is shipped with the console enabled. To disable the console set switch SW3-5 as shown in Table 2-4.

CONSOLE STATUS	SW3-5
Disabled Enabled	ON *OFF

*Factory preset

TABLE 2-4: CONSOLE ENABLE

2.8 BREAK RESPONSE

Channel 7 can be configured to either bootstrap, halt (console emulation mode), or have no response to a receive break condition. A bootstrap operation upon a receive break condition causes the CPU to execute the bootstrap program strating at the memory location defined by the power-up mode jumpers of the CPU. A halt operation unpon a receive break condition causes the processor to halt and the console octal debugging technique (ODT) microcode to be invoked. Configurations are shown in Table 2-5.

BREAK RESPONSE	E1-E2	E1-E3
*None	OUT	OUT
Boot	IN	OUT
Halt	OUT	IN

*Factory Preset

TABLE 2-5: BREAK CONFIGURATIONS

2.9 CTS BIAS

The Clear To Send (CTS) signal bias is factory configured for +12V. The CTS bias can be reconfigured for -12V; however, it is recommended that the factory configuration remain unchanged. CTS configurations are shwon in Table 2-6.

CTS BIAS	E4-E5	E5-E6
*+12V	OUT	IN
-12V	IN	OUT

*Factory Preset

TABLE 2-6: CTS BIAS CONFIGURATON

2.10 CABLING

The SCD-DLV11J/8P has two optional 40-pin connectors, each terminating in four DB25P connectors. The 40-pin connectors and associated 25-pin terminating connector pin assignments are defined in Table 2-7.

SIGNAL	DESCRIPTION	25-PIN DB25P	40-PIN CONNECTOR ---LINE NUMBER--- 0 1 2 3 ←J2 4 5 6 7 ←J1			
Transmit Data	Data transmitted from SCD-DLV11J/8P to terminal	3	33	23	13	3
Receive Data	Data received by SCD-DLV11J/8P from terminal	2	38	28	18	8
Clear to Send	Signal sent by device to SCD-DLV11J/8P to indicate readiness for transmitted data	5	34	24	14	4
Ground	Signal Ground*	7	39	25	12	5
Ground	Protective Ground*	1	32	22	15	2

*Signal and Protective Grounds are connected.

TABLE 2-7: CABLE PIN ASSIGNMENTS

The SCD-DLV11J/8P provides a Clear to Send input which can be driven by the attached serial line device to cause the SCD-DLV11J/8P channel to stop transmitting. The common use for this feature is with a printer that does not support XON-XOFF, but does provide a buffer full signal. This buffer status signal can be used to assert the CTS signal and effectively control transmission of data to the printer from the SCD-DLV11J/8P.

Cabling to terminals requires null modem cables with DB25S sockets between the SCD-DLV11J/8P connectors and associated terminal connectors.

2.11 MODULE INSTALLATION

The SCD-DLV11J/8P plugs directly into any Q bus slot, providing BIAK1 and BIAK0 lines from the interface to the CPU are continuous. Bus signals and associated pin assignments are listed in Appendix A.

2.12 RACKMOUNT PANEL (OPTION)

An optional rackmount panel provides convenient mounting for the eight DB25P connectors. The panel accepts connectors from two 8-channel devices. The panel is illustrated in Figure 2-2.

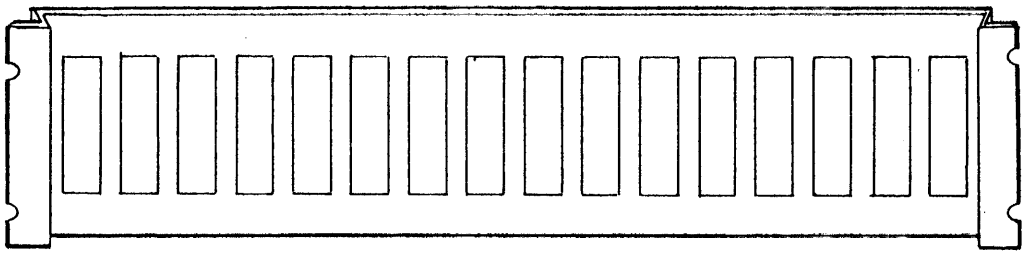


FIGURE 2-2: RACKMOUNT CONNECTOR PANEL

Section 3 - Programming

3.1 INTRODUCTION

The SCD-DLV11J/8P is controlled by four device registers per channel for a total of 32 device registers. The four device registers provided for each of the eight channels are:

RCSR	Receive Control/Status Registers
RBUF	Receive Buffer
XCSR	Transmit Control/Status Register
XBUF	Transmit Buffer

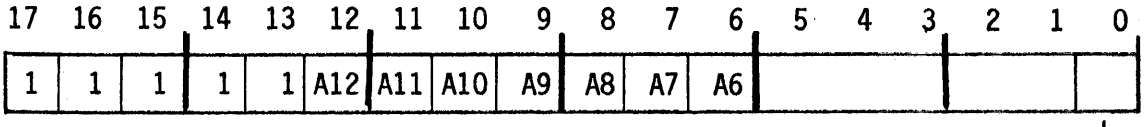
With the exception of the console channel, the device registers are assigned in a contiguous block by setting the address of channel 0. If the SCD-DLV11J/8P is used as the console device, channel 7 is assigned the console address and vector. If the SCD-DLV11J/8P is not used as the console, channel 7 is assigned as the last contiguous address set. Table 3-1 illustrates an initial address and vector assignment with contiguous locations.

ADDRESS	REGISTER	VECTOR	CHANNEL
176500	RCSR	300	0
176502	RBUF		
176504	XCSR	304	0
176506	XBUF		
176510	RCSR	310	1
176512	RBUF		
176514	XCSR	314	1
176516	XBUF		
176520	RCSR	320	2
176522	RBUF		
176524	XCSR	324	2
176526	XBUF		
176530	RCSR	330	3
176532	RBUF		
176534	XCSR	334	3
176536	XBUF		
176540	RCSR	340	4
176542	RBUF		
176544	XCSR	344	4
176546	XBUF		
176550	RCSR	350	5
176552	RBUF		
176554	XCSR	354	5
176556	XBUF		
176560	RCSR	360	6
176562	RBUF		
176564	XCSR	364	6
176566	XBUF		
176570*	RCSR	370	7
176572	RBUF		
176574	XCSR	374	7
176576	XBUF		
*If the console is selected it resides at channel 7, and the last four addresses in this table are:			
177560	RCSR	60	7
177562	RBUF		
177564	XCSR	64	7
177566	XBUF		

TABLE 3-1: STANDARD ADDRESS AND VECTOR ASSIGNMENTS

3.2 DEVICE ADDRESS FORMAT

The address format is shown below.



Bank 7

Selected (1)

Initial Address

(See Section 2.3)

Channel (Device) Select

--Bit-- 5	4	3	Channel Select
0	0	0	CH 0
0	0	1	CH 1
0	1	0	CH 2
0	1	1	CH 3
1	0	0	CH 4
1	0	1	CH 5
1	1	0	CH 6
1	1	1	CH 7

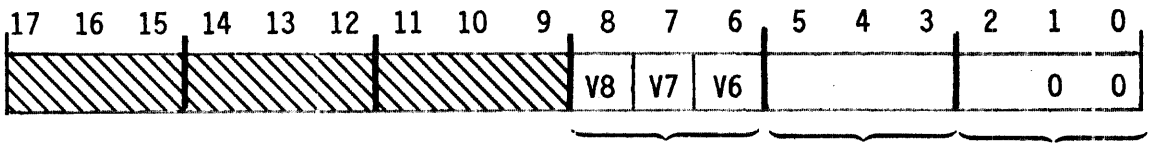
Register Select

Bit 2	1	Interrupt
0	0	RCSR
0	1	RBUF
1	0	XCSR
1	1	XBUF

Byte Pointer

3.3 VECTOR INTERRUPT FORMAT

The interrupt vector format is shown below.



Initial Vector

(See Section 2.4)

Channel Requesting Interrupt

--Bit-- 5	4	3	Channel Select
0	0	0	CH 0
0	0	1	CH 1
0	1	0	CH 2
0	1	1	CH 3
1	0	0	CH 4
1	0	1	CH 5
1	1	0	CH 6
1	1	1	CH 7

Interrupt

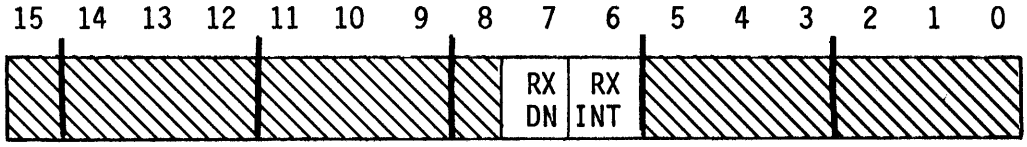
Bit 2	Interrupt
0	Receiver Interrupt
1	Transmitter Interrupt

All bits not used are read as 0.

3.4 WORD FORMATS

The four word formats, one for each device register within a channel, are described in the following sections.

3.4.1 Receive Control/Status Register (RCSR)

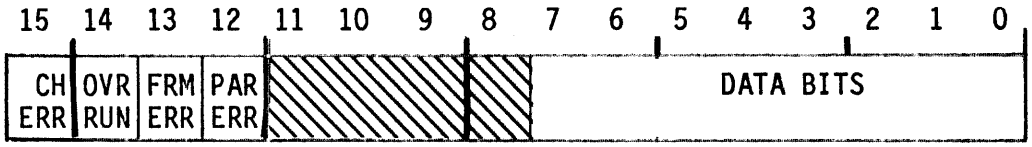


RX DN — RECEIVER DONE. Set when an entire character has been received and is ready for input to the CPU. Cleared when RBUF is read or BINIT L signal goes true. If RX INT (bit 6) is set, setting RX DN starts an interrupt sequence. Read only.

RX INT — RECEIVER INTERRUPT ENABLE. Set under program control to generate a receiver interrupt request (when a character is ready for input to the processor signified by bit 7 being set). Cleared under program control or by BINIT signal. Read/write.

All bits not used are read as 0.

3.4.2 Receiver Buffer (RBUF)



CH ERR — CHANNEL ERROR STATUS. Logical OR of bits 14, 13, and 12. Read only.

OVR RUN — OVERRUN ERROR. When set, indicates that the reading of the previously received character was not completed (receiver done not cleared) prior to receiving a new character. Cleared by BINIT signal. Read only.

NOTE

When "back-to-back" characters are received, one full character time is allowed from the time instant receiver done (bit 7) is set to the occurrence of an overrun error.

FRM ERR — FRAMING ERROR. When set, indicates that the character read had no valid stop bit. Cleared by BINIT signal. Read only.

PAR ERR — PARITY ERROR. When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no-parity operation is configured for the channel. Read only.

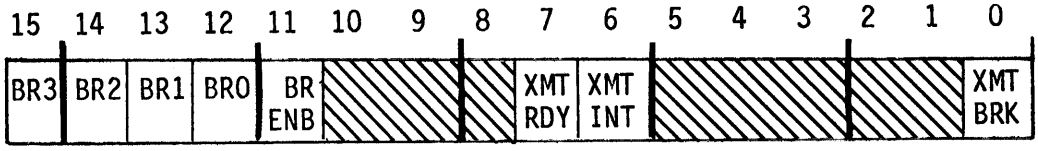
NOTE

Error bits remain valid until the next character is received, at which time the error bits are updated.

DATA BITS — DATA BITS. Contains seven or eight data bits in a right-justified format. Bit 7 = 0 when 7 data bits are enabled. Read only.

All bits not used are read as 0.

3.4.3 Transmit Control/Status Register (XCSR)



BR3-BR0 PROGRAMMABLE BAUD RATE SELECT. When set, these bits choose a baud rate from 50-19.2K baud. BR END must be set for the baud rate to be affective. See section 2.5 to configure baud rate. Write only.

BR ENB PROGRAMMABLE BAUD RATE ENABLE. Must be set in order to select a new baud rate indicated by bits 12-15. Write only.

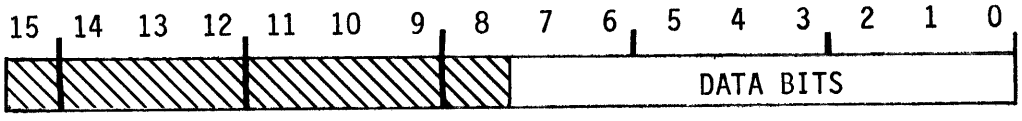
XMT RDY TRANSMIT READY. Set when XBUF is empty and can accept another character for transmission. It is also set by INIT, during power-up or during a reset instruction. Read only.

XMT INT TRANSMIT INTERRUPT ENABLE. Set under program control when it is desired to generate a transmitter interrupt request when transmitter is ready to accept a character for transmission. Cleared under program control, during power-up or reset instruction. Read/write.

XMT BRK TRANSMIT BREAK. Set or reset under program control. When set, a continuous space level is transmitted. However, transmit done and transmit interrupt can still operate, allowing software timing of break. When not set, normal character transmission can occur. Cleared by BINIT. Read/write.

All bits not used are read as 0.

3.4.4 Transmit Buffer (XBUF)



Bits 0-7 contain the seven or eight right-justified data bits, which are loaded under program control for serial transmission. Bits not used are read as 0.

PIN	SIGNAL	LSI-11/2	LSI-11/23	PIN	SIGNAL	LSI-11/2	LSI-11/23
AA1	BIRQ5L			AA2	+5V		
AB1	BIRQ6L			AB2	-12V		
AC1	BDAL16L			AC2	GND		
AD1	BDAL17L			AD2	+12V		
AE1	*SS1	STOP L	SINGLE STEP	AE2	BDOUTL		
AF1	*SRUNL	SRUNL	SRUNL	AF2	BRPLYL		
AH1	*SRUNL	SRUNL	SRUNL	AH2	BDINL		
AJ1	GND			AJ2	BSYNCL		
AK1	*MSPAREA	MTOEL	NOT USED	AK2	BWTBTL		
AL1	*MSPAREB	GND	NOT USED	AL2	BIRQ4L		
AM1	GND			AM2	*BIAK1L	NOT USED	MMUSTRH
AN1	BDMRL			AN2	*BIAK0L		
AP1	BHALTL			AP2	BBS7L		
AR1	BREFL	NOT USED	NOT USED	AR2	*BDMG1L	NOT USED	UBMAAPL
AS1	+12VB			AS2	*BDMG0L		
AT1	GND			AT2	BINITL		
AU1	PSPARE1			AU2	BDAL0L		
AV1	+5VB			AV2	BDAL1L		
BA1	BDCOKH			BA2	+5V		
BB1	BPOKH			BB2	-12V		
BC1	*SSPARE4	SCLK3H	MMUDAL18H	BC2	GND		
BD1	*SSPARE5	SWMIB18H	MMUDAL19H	BD2	+12V		
BE1	*SSPARE6	SWMIB19H	MMUDAL20H	BE2	BDAL2L		
BF1	*SSPARE6	SWMIB20H	MMUDAL21H	BF2	BDAL3L		
BH1	*SSPARE8	SWMIB21H	CLKDISL	BH2	BDAL4L		
BJ1	GND			BJ2	BDAL5L		
BK1	*MSPAREB	NOT USED	NOT USED	BK2	BDAL6L		
BL1	*MSPAREB	NOT USED	NOT USED	BL2	BDAL7L		
BM1	BND			BM2	BDAL8L		
BN1	BSACKL			BN2	BDAL9L		
BP1	BIRQ7L			BP2	BDAL10L		
BR1	BEVNTL			BR2	BDAL11L		
BS1	PSPARE4	PSPARE4	+12VB	BS2	BDAL12L		
BT1	GND			BT2	BDAL13L		
BU1	PSPARE2			BU2	BDAL14L		
BV1	+5V			BV2	BDAL15L		

*NOT BUSSED

Q BUS PIN ASSIGNMENTS

SCD-DLV11J/8P ADDRESS ASSIGNMENTS VIA SW3 SWITCH SETTINGS

NOTES: SW3 POSITIONS ARE NOT LISTED IN NUMERICAL ORDER.
SW3-5 IS CONSOLE ENABLE/DISABLE.

ADDRESS	SW3 SWITCH POSITIONS 1	2	3	4	8	7	6
	ADDRESS BITS A12	A11	A10	A09	A08	A07	A06
160000	ON	ON	ON	ON	ON	ON	ON
160100	ON	ON	ON	ON	ON	ON	OFF
160200	ON	ON	ON	ON	ON	OFF	ON
160300	ON	ON	ON	ON	ON	OFF	OFF
160400	ON	ON	ON	ON	OFF	ON	ON
160500	ON	ON	ON	ON	OFF	ON	OFF
160600	ON	ON	ON	ON	OFF	OFF	ON
160700	ON	ON	ON	ON	OFF	OFF	OFF
161000	ON	ON	ON	OFF	ON	ON	ON
161100	ON	ON	ON	OFF	ON	ON	OFF
161200	ON	ON	ON	OFF	ON	OFF	ON
161300	ON	ON	ON	OFF	ON	OFF	OFF
161400	ON	ON	ON	OFF	OFF	ON	ON
161500	ON	ON	ON	OFF	OFF	ON	OFF
161600	ON	ON	ON	OFF	OFF	OFF	ON
161700	ON	ON	ON	OFF	OFF	OFF	OFF
162000	ON	ON	OFF	ON	ON	ON	ON
162100	ON	ON	OFF	ON	ON	ON	OFF
162200	ON	ON	OFF	ON	ON	OFF	ON
162300	ON	ON	OFF	ON	ON	OFF	OFF
162400	ON	ON	OFF	ON	OFF	ON	ON
162500	ON	ON	OFF	ON	OFF	ON	OFF
162600	ON	ON	OFF	ON	OFF	OFF	ON
162700	ON	ON	OFF	ON	OFF	OFF	OFF
163000	ON	ON	OFF	OFF	ON	ON	ON
163100	ON	ON	OFF	OFF	ON	ON	OFF
163200	ON	ON	OFF	OFF	ON	OFF	ON
163300	ON	ON	OFF	OFF	ON	OFF	OFF
163400	ON	ON	OFF	OFF	OFF	ON	ON
163500	ON	ON	OFF	OFF	OFF	ON	OFF
163600	ON	ON	OFF	OFF	OFF	OFF	ON
163700	ON	ON	OFF	OFF	OFF	OFF	OFF
164000	ON	OFF	ON	ON	ON	ON	ON
164100	ON	OFF	ON	ON	ON	ON	OFF
164200	ON	OFF	ON	ON	ON	OFF	ON
164300	ON	OFF	ON	ON	ON	OFF	OFF
164400	ON	OFF	ON	ON	OFF	ON	ON
164500	ON	OFF	ON	ON	OFF	ON	OFF
164600	ON	OFF	ON	ON	OFF	OFF	ON
164700	ON	OFF	ON	ON	OFF	OFF	OFF

ADDRESS	SW3 SWITCH POSITIONS 1	2	3	4	8	7	6
	ADDRESS BITS A12	A11	A10	A09	A08	A07	A06
165000	ON	OFF	ON	OFF	ON	ON	ON
165100	ON	OFF	ON	OFF	ON	ON	OFF
165200	ON	OFF	ON	OFF	ON	OFF	ON
165300	ON	OFF	ON	OFF	ON	OFF	OFF
165400	ON	OFF	ON	OFF	OFF	ON	ON
165500	ON	OFF	ON	OFF	OFF	ON	OFF
165600	ON	OFF	ON	OFF	OFF	OFF	ON
165700	ON	OFF	ON	OFF	OFF	OFF	OFF
166000	ON	OFF	OFF	ON	ON	ON	ON
166100	ON	OFF	OFF	ON	ON	ON	OFF
166200	ON	OFF	OFF	ON	ON	OFF	ON
166300	ON	OFF	OFF	ON	ON	OFF	OFF
166400	ON	OFF	OFF	ON	OFF	ON	ON
166500	ON	OFF	OFF	ON	OFF	ON	OFF
166600	ON	OFF	OFF	ON	OFF	OFF	ON
166600	ON	OFF	OFF	ON	OFF	OFF	OFF
167000	ON	OFF	OFF	OFF	ON	ON	ON
167100	ON	OFF	OFF	OFF	ON	ON	OFF
167200	ON	OFF	OFF	OFF	ON	OFF	ON
167300	ON	OFF	OFF	OFF	ON	OFF	OFF
167400	ON	OFF	OFF	OFF	OFF	ON	ON
167500	ON	OFF	OFF	OFF	OFF	ON	OFF
167600	ON	OFF	OFF	OFF	OFF	OFF	ON
167700	ON	OFF	OFF	OFF	OFF	OFF	OFF
170000	OFF	ON	ON	ON	ON	ON	ON
170100	OFF	ON	ON	ON	ON	ON	OFF
170200	OFF	ON	ON	ON	ON	OFF	ON
170300	OFF	ON	ON	ON	ON	OFF	OFF
170400	OFF	ON	ON	ON	OFF	ON	ON
170500	OFF	ON	ON	ON	OFF	ON	OFF
170600	OFF	ON	ON	ON	OFF	OFF	ON
170700	OFF	ON	ON	ON	OFF	OFF	OFF
171000	OFF	ON	ON	OFF	ON	ON	ON
171100	OFF	ON	ON	OFF	ON	ON	OFF
171200	OFF	ON	ON	OFF	ON	OFF	ON
171300	OFF	ON	ON	OFF	ON	OFF	OFF
171400	OFF	ON	ON	OFF	OFF	ON	ON
171500	OFF	ON	ON	OFF	OFF	ON	OFF
171600	OFF	ON	ON	OFF	OFF	OFF	ON
171700	OFF	ON	ON	OFF	OFF	OFF	OFF

SCD-DLV11J/8P ADDRESS ASSIGNMENTS VIA SW3 SWITCH SETTINGS (CONTINUED)

ADDRESS	SW3 SWITCH POSITIONS 1	2	3	4	8	7	6
	ADDRESS BITS A12	A11	A10	A09	A08	A07	A06
172000	OFF	ON	OFF	ON	ON	ON	ON
172100	OFF	ON	OFF	ON	ON	ON	OFF
172200	OFF	ON	OFF	ON	ON	OFF	ON
172300	OFF	ON	OFF	ON	ON	OFF	OFF
172400	OFF	ON	OFF	ON	OFF	ON	ON
172500	OFF	ON	OFF	ON	OFF	ON	OFF
172600	OFF	ON	OFF	ON	OFF	OFF	ON
172700	OFF	ON	OFF	ON	OFF	OFF	OFF
173000	OFF	ON	OFF	OFF	ON	ON	ON
173100	OFF	ON	OFF	OFF	ON	ON	OFF
173200	OFF	ON	OFF	OFF	ON	OFF	ON
173300	OFF	ON	OFF	OFF	ON	OFF	OFF
173400	OFF	ON	OFF	OFF	OFF	ON	ON
173500	OFF	ON	OFF	OFF	OFF	ON	OFF
173600	OFF	ON	OFF	OFF	OFF	OFF	ON
173700	OFF	ON	OFF	OFF	OFF	OFF	OFF
174000	OFF	OFF	ON	ON	ON	ON	ON
174100	OFF	OFF	ON	ON	ON	ON	OFF
174200	OFF	OFF	ON	ON	ON	OFF	ON
174300	OFF	OFF	ON	ON	ON	OFF	OFF
174400	OFF	OFF	ON	ON	OFF	ON	ON
174500	OFF	OFF	ON	ON	OFF	ON	OFF
174600	OFF	OFF	ON	ON	OFF	OFF	ON
174700	OFF	OFF	ON	ON	OFF	OFF	OFF

ADDRESS	SW3 SWITCH POSITIONS 1	2	3	4	8	7	6
	ADDRESS BITS A12	A11	A10	A09	A08	A07	A06
175000	OFF	OFF	ON	OFF	ON	ON	ON
175100	OFF	OFF	ON	OFF	ON	ON	OFF
175200	OFF	OFF	ON	OFF	ON	OFF	ON
175300	OFF	OFF	ON	OFF	ON	OFF	OFF
175400	OFF	OFF	ON	OFF	OFF	ON	ON
175500	OFF	OFF	ON	OFF	OFF	ON	OFF
175600	OFF	OFF	ON	OFF	OFF	OFF	ON
175700	OFF	OFF	ON	OFF	OFF	OFF	OFF
176000	OFF	OFF	OFF	ON	ON	ON	ON
176100	OFF	OFF	OFF	ON	ON	ON	OFF
176200	OFF	OFF	OFF	ON	ON	OFF	ON
176300	OFF	OFF	OFF	ON	ON	OFF	OFF
176400	OFF	OFF	OFF	ON	OFF	ON	ON
176500	OFF	OFF	OFF	ON	OFF	ON	OFF
176600	OFF	OFF	OFF	ON	OFF	OFF	ON
176700	OFF	OFF	OFF	ON	OFF	OFF	OFF
177000	OFF	OFF	OFF	OFF	ON	ON	ON
177100	OFF	OFF	OFF	OFF	ON	ON	OFF
177200	OFF	OFF	OFF	OFF	ON	OFF	ON
177300	OFF	OFF	OFF	OFF	ON	OFF	OFF
177400	OFF	OFF	OFF	OFF	OFF	ON	ON
177500	OFF	OFF	OFF	OFF	OFF	ON	OFF
177600	OFF	OFF	OFF	OFF	OFF	OFF	ON
177700	OFF	OFF	OFF	OFF	OFF	OFF	OFF

SCD-DLV11J/8P BASE VECTOR ASSIGNMENTS VIA SWITCH SW1

BASE VECTOR	SW1 POSITIONS 4	3	2
	VECTOR BITS V8	V7	V6
000	ON	ON	ON
100	ON	ON	OFF
200	ON	OFF	ON
300	ON	OFF	OFF
400	OFF	ON	ON
500	OFF	ON	OFF
600	OFF	OFF	ON
700	OFF	OFF	OFF

Refer to DEC's "Microcomputer Interface Handbook, 1980" for recommended address assignments.