

OMTI Chip Set

BUS INTERFACE DEVICES

- OMTI 5080**
SCSI Multifunction Chip
- OMTI 5090**
IBM-PC XT Bus Interface Chip
- OMTI 5098**
IBM-PC AT Bus Interface Chip
- OMTI 5011**
Differential MFM Driver/Receiver

DATA PATH MANAGEMENT DEVICES

- OMTI 5050**
Disk Sequencer Chip
- OMTI 5060**
Buffer Controller Chip
- OMTI 5055**
Kombo Chip

DATA SEPARATOR DEVICES

- OMTI 5027**
2,7 RLL/NRZ Data Separator
- OMTI 5070**
MFM/NRZ Data Separator

ERROR CORRECTION

- OMTI 8510**
3 Way Interleave Chip

DESCRIPTION

The SMS OMTI Chip Set is the ideal solution for the controller electronics in your SCSI, IBM-XT, IBM-AT, or optical drive.

The flexibility of the chip set allows it to be used in a large number of system bus architectures and disk drive interfaces, all at 1:1 interleave.

Only the OMTI Chip Set allows a complete CMOS solution supported by firmware with years of in circuit applica-

tion. Only the OMTI Chip Set is now available in surface mount technology, either PLCC or flat package options. The highly integrated OMTI Chip Sets allow controllers to be built on a low cost, low power, high performance, small profile PC board that is ideal for today's competitive market.

BUS INTERFACE DEVICES

OMTI 5080 SCSI Multifunctions Chip

- 2 Micron CMOS Technology
- Supports SCSI, ST506/412, ESDI, or QIC-02 Interface
- Internal Single Ended Driver/Receiver 48MA Sink Current
- Dual DMA and I/O Data Paths
- Assumes SCSI Initiator and Target Roles
- Supports Disconnect and Reconnect
- Supports Hard and Soft Reset

OMTI 5090 IBM-PC XT Bus Interface Chip

- 3 Micron CMOS Technology
- Data Path To and From the IBM I/O Channel
- Address Decoding for 8 I/O Ports
- Address Decoding for the BIOS ROM
- I/O Channel Interrupt Circuitry
- DMA Transfer Circuitry

OMTI 5098 IBM-PC AT Bus Interface Chip

- 3 Micron CMOS Technology
- IBM-AT Compatible Protocol
- Decodes IBM-AT Floppy Select (PLCC)
- Supports Dual Bus Architecture

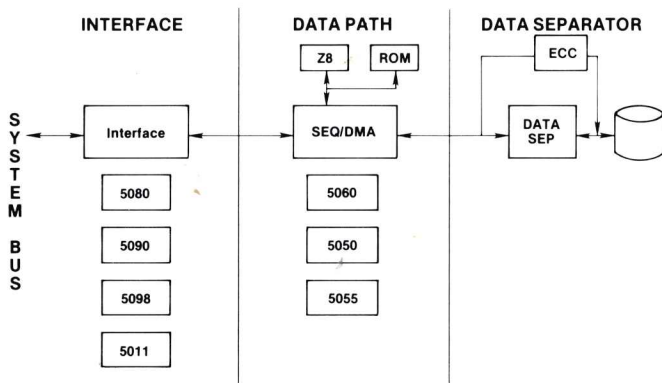
OMTI 5011 Differential MFM Driver/Receiver

- 3 Micron CMOS Technology
- Controls Differential Driver/Receivers for the ST506/412 Interface

DATA PATH MANAGEMENT DEVICES

OMTI 5050 Disk Sequencer Chip

- 2 Micron CMOS Technology
- Controls ST506/412, ESDI, SMD, and Other Interface Disk Drives
- High Speed SERDES Data Functions
- Non Interleave Operations
- NRZ Serial Drive Interface
- 16 Bit CRC for Either Header and/or Data Fields
- Controls Soft or Hard Sector Drives
- Multiple Sector Read/Write Transfers
- Programmable Internal ECC Length 24, 32, 48, 56 or 64 Bits
- Programmable Internal ECC Polynomial
- ESDI Address Mark Detection



OMTI 5060 Controller Chip

- 2 Micron CMOS Technology
- DMA REQ/ACK Handshake Protocol
- Four DMA Port Ring Buffer Control (SCSI, Disk Sequencer, Microprocessor, QIC-02) with Independent Control on Each Port
- Contention Resolution on Port Authority
- 16 Bit Buffer Addressing. Up to 64K Buffer Size.
- Auto Address Increment

OMTI 5055 Kombo Chip

- 2 Micron CMOS Technology
- Dual Bus Architecture
- Dual Independent DMA Channels
- Configurable SCSI REQ/ACK Handshake Protocol
- 10 Mbit/Sec Data Transfer Rate
- Programmable Internal ECC Length 32, 48, 56 Bits
- Sector Size to 64K (By 1 Byte Increments)
- Up to 8K External Buffer Size
- Programmable REQ/ACK/Auto Count Reinit/Access Cycle Timing/Sector Size/ID Data & Size/Gap Size/Header Flag/Auto ID Retries
- Simultaneous Data Transfer and Microprocessor Operations
- Direct ESDI NRZ Interface

DATA SEPERATOR DEVICES

OMTI 5027 2,7 RLL/NRZ Data Seperator

- 2 Micron CMOS Technology
- Internal Encode/Decode/VCO Circuitry
- Internal Phase Locked Loop
- 2,7 to NRZ and NRZ to 2,7 Conversions
- Internal Two Level Precompensation
- Address Mark Detection
- 10 Mbit/Sec Data Rate

OMTI 5070 MFM/NRZ Data Seperator

- 3 Micron CMOS Technology
- Internal Encode/Decode/VCO Circuitry
- Internal Phase Locked Loop
- 5.0 Mbit/Sec Data Rate
- MFM to NRZ and NRZ to MFM Conversions
- Internal Write Precompensation
- Address Mark Detection and Generation
- Internal Early On and Late Timing

ERROR CORRECTION

OMTI 8510 Three Way Interleave Chip

- 2 Micron CMOS Technology
- ECC By Reed-Solomon Codes 4 or 16 Degree Polonomial
- Configurable for Serial or Parallel Data Transfer
- Generates Redundancy on Write
- Generates Composite Syndroms on Read
- Can be Daisy Chained for 10 Way Interleave
- 10 Mbit/Sec Data Rate
- 16/32/48 Reduncancy Bytes Per Sector
- 239/478/717 Data Bytes Per Sector

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