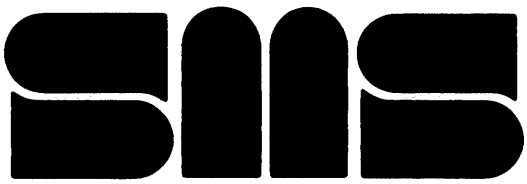

OMTI 8000 SERIES
IBM PC AT
INTELLIGENT DATA CONTROLLERS
REFERENCE MANUAL
JUNE 1986

Scientific Micro Systems, Inc.

OMTI 8000 SERIES
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IBM PC AT

INTELLIGENT DATA CONTROLLERS

REFERENCE MANUAL

Models :

OMTI 8100

OMTI 8200

OMTI 8500

OMTI 8600

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List of changes from previous revision :
- Addition of the READ ESDI DEFECT LIST command

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REVISION: D

Date of this Revision: June 20th, 1986

OMTI 8000
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SECTION 1

INTRODUCTION

1.1. PRODUCT DESCRIPTION

The OMTI 8000 Series is a combination of Winchester disk and floppy disk controller for IBM AT Bus compatible computers (16 bit data path). The OMTI 8000 Series is contained on a single PCB that plugs into an empty slot of the motherboard of the computer.

The OMTI 8000 Series uses SMS' sophisticated VLSI circuitry to provide many advanced features. These include:

- Concurrent support for both ESDI (Enhanced Standard Drive Interface) and ST412 compatible winchester disk drives
- Support for high capacity (1.6 Megabyte) floppies
- High performance (1:1 interleave on disk, 1.6 Megabyte/second transfer on AT Bus)
- 8Kbyte buffer minimum.
- 48 bit Error Correction Code on ESDI drives, 32 bit ECC on ST412 drives
- Concurrent data operations on winchester and floppy disk
- Supports both programmed I/O and DMA data transfers

The above and other features make the OMTI 8000 Series double controller an exceptional value that many have come to expect from SMS' family of data storage products.

BIOS issues : The OMTI 8000 Series is fully AT bus and hardware compatible but, because the BIOS (Basic Input/Output System) is not contained on the OMTI 8000, it is the host's responsibility to ensure software compatibility. The BIOS on the IBM AT will operate correctly with the floppy portion of the OMTI 8800 however in order to provide higher performance the fixed disk command set differs from the IBM controller. The BIOS must therefore be modified to support this enhanced command set and ensure full software compatibility.
As an option SMS provides two EPROMs BIOS to make the 8000 series fully compatible with the IBM controller.

1.2 NUMBER AND TYPE OF DRIVES SUPPORTED

Table 1-1

Model	8100	8200	8500	8600
Number of drives	2 max	4 max	2 max	4 max
Winchesters	up to 2	up to 2	up to 2	up to 2
ESDI drives	no	no	supported	supported
Flexible disks	0	up to 2	0	up to 2

1.3 SPECIFICATION

1.3.1. Features per Peripherals

WINCHESTER DISKS.

- Operates one or two hard or soft sectored ST412 compatible or ESDI Winchester disk(s). The disk can be fixed or removeable. ESDI drives may transfer data at a rate of up to 10 Mbit/sec.
- Supports 256, 512, 1024 or 1056 bytes/sector.
- Supports programmable sector interleave including a 1:1 interleave.
- Addresses up to 2048 tracks and 16 heads.
- Supports overlapped seek.
- Word (16 bits) width data transfer on AT bus.
- Supports both programmed I/O and DMA data transfers.

FLOPPY DISKS

- Operates one or two floppy disk drives
- Supports 48, 96 TPI drives plus the high density AT compatible drives.
- Supports 250, 300, or 500 K bits/sec transfer rate including dual rotational speed floppies
- Host has direct access to floppy disk controller chip (NEC765 or equivalent)

1.3.2 Physical Specifications

Width	3.9 inches
Length	13.25 inches
Height	.75 inches

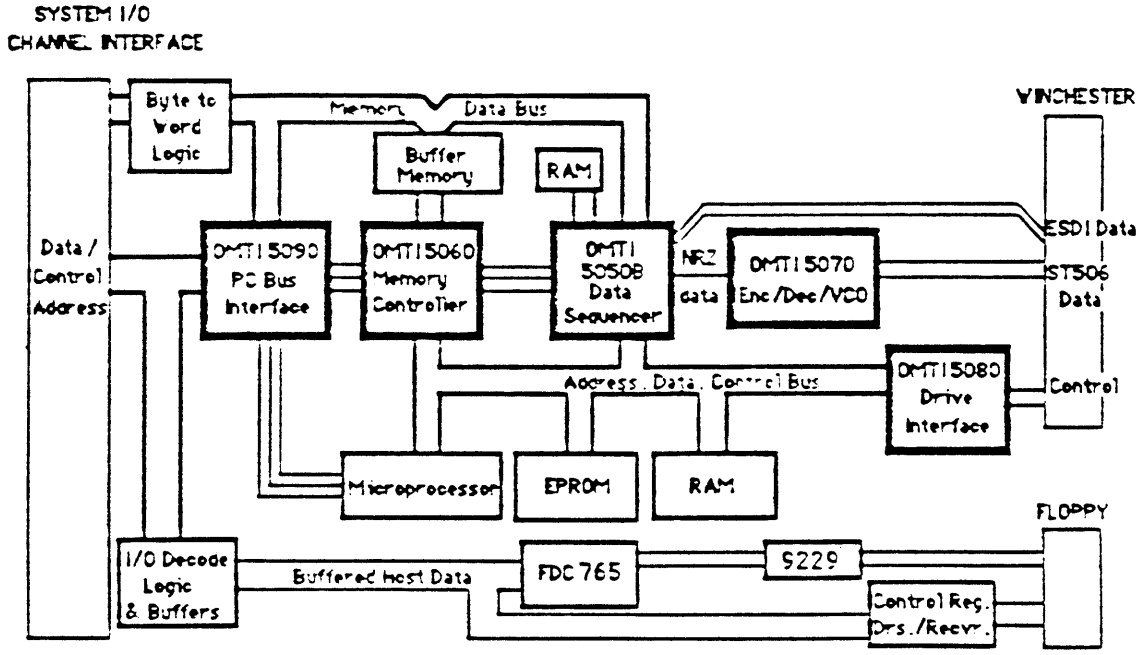
1.3.3 Environmental Specifications

	Operating	Storage
Temperature	0 to 50 deg C	40 to 75 deg C
Relative Humidity	10 to 95% N.C.	10 to 95% Noncondensing
Maximum Wet Bulb	30 deg C	Noncondensing
Altitude	0 to 10,000 ft.	0 to 15,000 ft.

1.3.4. Power Requirements

Voltage	4.75 to 5.25 V DC
Maximum ripple and noise	100 mv
Maximum current drawn	1.5 Amp

Figure 1.1



OMTI 8000 Series

IBM PC AT Controller Block Diagram

SECTION 2

CONFIGURATION AND INSTALLATION

2.1 UNPACKING AND INSPECTION

Upon receipt of your OMTI 8000 Series Data Controllers, inspect the packaging for evidence of damage during transit. Open the package and inspect the controller board for visible damage such as scratches, loose components, or broken connectors. If there is damage, immediately notify the carrier's agent and Scientific Micro Systems' customer service representative. Compare the items listed on your original Purchase Order to the actual contents of the package and the packing list. If discrepencies exist, notify you SMS customer service representative.

Retain the shipping container and packing material for examination (if it has been damaged), or for reuse when returning the controller board to the factory.

2.2 SYSTEM CONFIGURATION

The OMTI 8000 Series Data Controllers are designed to plug directly into any unused location on the system motherboard. The peripherals are connected to the controller by ribbon cables.

After your board is mounted; connect the cables to the disk drive. Refer to Figure 2-1 for the location of connectors on your board. Pin 1 on all connectors is specified by a square solder pad, visible on the soldered side of the board.

The connector's recommended part numbers are as follows:

J2 and J7 - AMP P/N 88373-3 (-34pin)
J3 and J4 - AMP P/N 86904-1 (-20pin)

2.3 BOARD PREPARATION

The appropriate board layout, connector locations, and jumper locations for the OMTI 8000 Series Controllers are illustrated in Figure 2-1. Use Table 2-1 to ensure that the factory installed jumpers are correctly in place.

The OMTI 8000 Series has jumpers which allow the controller to be easily integrated into different systems.

Jumpers W1 through W7 specify parameters of the system-controller interface typically used by a BIOS.
Jumpers W8 through W15 specify drive parameters to be used by the controller.

Table 2-1 defines the jumpers in detail.

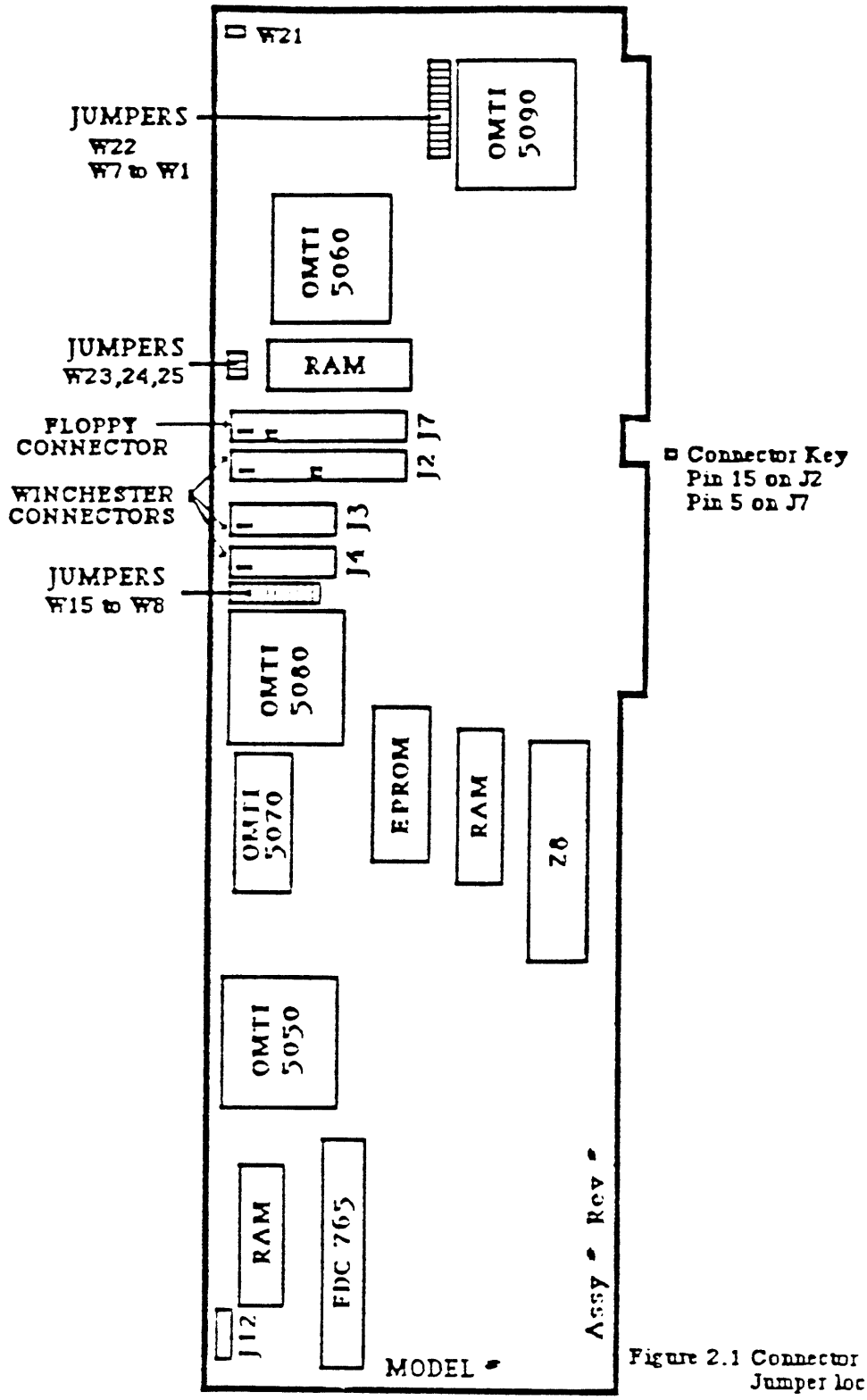


Figure 2.1 Connector and Jumper locations

Jumper Assignments

0 = No jumper installed 1 = Jumper installed * = As shipped

W4	W3	W2	W1	Drive configuration jumpers
0	0	0	0	(Host assigns jumper value)

W6	W5	W22	Winchester I/O port base address
0*	0	1	0320_H
0	1	1	0324_H
1	0	1	0328_H
1	1	1	$032C_H$
0	0	0	$01A0_H$
0	1	0	$01A4_H$
1	0	0	$01A8_H$
1	1	0	$01AC_H$

W7	Floppy disk I/O port base address
0	0370_H
1*	$03F0_H$

W9	W8	Bytes per sector
0*	0	512 (17 Sectors per track)
0	1	512 (18 Sectors per track)
1	0	1024 (9 Sectors per track)
1	1	1056 (9 Sectors per track)

	LUN 0		LUN 1
W10	Sector type	W13	Sector type
0*	Soft sectored	0*	Soft sectored
1	Hard sectored	1	Hard sectored
W11	Drive class	W14	Drive class
0*	ST412 compatible	0*	ST412 compatible
1	ESDI compatible	1	ESDI compatible
W12	Drive type	W15	Drive type
0*	Fixed	0*	Fixed
1	Removeable	1	Removeable

W21, W23, W24, W25 Reserved

Table 2-2 Connector Assignment

J2	FIXED DISK	(34 pin)
J3	FIXED DISK - LUN 0	(20 pin)
J4	FIXED DISK - LUN 1	(20 pin)
J7	FLOPPY DISK	(34 pin)

LED Meaning

Self test diagnostics are run when the unit is powered on. If the LED goes out the diagnostics have passed. If the self test detects a failure the LED will remain on.

SECTION 3

HOST ELECTRICAL INTERFACE

3.1. INTRODUCTION

The OMTI 8000 Series are electrically and mechanically compatible with the bus or Input/Output channel used in the IBM AT computer. Physically this Input/Output channel is contained on two card edge connectors on the OMTI 8000 Series.

The Input/Output channel provides the necessary hardware interface to the host CPU to allow it to communicate with the controller.

3.2 INPUT/OUTPUT CHANNEL PIN ASSIGNMENT

The following figures summarize pin assignments for the Input/Output channel connectors.

INPUT/OUTPUT CHANNEL (COMPONENT SIDE of 62 pin EDGE CONNECTOR)

I/O	Signal Name	Input/Output
A1	-I/O CH CK	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	I/O CH RDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

Input/Output Channel (SOLDER SIDE of 62 pin EDGE CONNECTOR)

I/O Pin	Signal Name	I/O
B1	GND	Ground
B2	RESET DRV	O
B3	+5 Vdc	Power
B4	IRQ9	I
B5	-5 Vdc	Power
B6	DRQ2	I
B7	-12 Vdc	Power
B8	-OWS	I
B9	+12 Vdc	Power
B10	GND	Ground
B11	-SMEMW	O
B12	-SMEMR	O
B13	-IOW	I/O
B14	-IOR	I/O
B15	-DACK3	O
B16	DRQ3	I
B17	-DACK1	O
B18	DRQ1	I
B19	-Refresh	I/O
B20	CLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	-DACK2	O
B27	T/C	O
B28	BALE	O
B29	+5 Vdc	Power
B30	OSC	O
B31	GND	Ground

Input/Output Channel (COMPONENT SIDE of 36 pin EDGE CONNECTOR)

I/O Pin	Signal Name	I/O
C1	-SBHE	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	-MEMR	I/O
C10	-MEMW	I/O
C11	SDO8	I/O
C12	SDO9	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

Input/Output Channel (SOLDER SIDE of 36 pin EDGE CONNECTOR)

I/O Pin	Signal Name	I/O
D1	-MEM CS16	I
D2	-I/O CS 16	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ13	I
D7	IRQ14	I
D8	-DACK0	O
D9	DRQ0	I
D10	-DACK5	O
D11	DRQ5	I
D12	-DACK6	O
D13	DRQ6	I
D14	-DACK7	O
D15	DRQ7	I
D16	+5 Vdc	Power
D17	-MASTER	I
D18	GND	GND

3.3 INPUT/OUTPUT CHANNEL SIGNAL DESCRIPTION

The following is a description of the system board's INPUT/OUTPUT channel signals. All signal lines are TTL-compatible. Input/Output adapters should be designed with a maximum of two low-power Shottky (LS) loads per line.

SA0 through SA19 (Input/Output)

Address bits 0 through 19 are used to address memory and Input/Output devices within the system. These 20 address lines, in addition to LA17 through LA23, allow access of up to 16Mb of memory. SA0 through SA19 are gated on the system bus when "BALE" is high and are latched on the falling edge of "BALE." These signals are generated by the microprocessor or DMA Controller. They also may be driven by other microprocessors or DMA controllers that reside on the Input/Output channel.

LA17 through LA23 (Input/Output)

These signals (unlatched) are used to address memory and Input/Output devices within the system. They give the system up to 16Mb of addressability. These signals are valid when "BALE" is high. LA17 through LA23 are not latched during microprocessor cycles and therefore do not stay valid for the whole cycle. Their purpose is to generate memory decodes for 1 wait-state memory cycles. These decodes should be latched by Input/Output adapters on the falling edge of "BALE." These signals also may be driven by other microprocessors or DMA controllers that reside on the Input/Output channel. Note that it is these signals that are decoded by the Input/Output adapter to generate "MEM CS16" for 16 bit, 1 wait -state memory cycles.

CLK (Output)

This is the 6-MHz system clock. It is a synchronous microprocessor cycle clock with a cycle time of 167 nanoseconds. The clock has a 50% duty cycle. This signal should only be used for synchronization. It is not intended for uses requiring a fixed frequency.

RESET DRV (Output)

"Reset drive" is used to reset or initialize system logic at power-up time or during a low line-voltage outage. This signal is active high.

SD0 through SD15 (Input/Output)

These signals provide bus bits 0 through 15 for the microprocessor, memory, and Input/Output devices. D0 is the least-significant bit and D15 is the most significant bit. All 8-bit devices on the Input/Output channel should use D0 through D7 for communications to the microprocessor. The 16-bit devices will use D0 through D15. To support 8-bit devices, the data on D8 through D15 will be gated to D0 through D7 during 8-bit transfers to these devices; 16-bit microprocessor transfers to 8-bit devices will be converted to two 8-bit transfers.

BALE (Output)(buffered)

"Address latch enable" is provided by the 82288 Bus Controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. It is available to the Input/Output channel as an indicator of a valid microprocessor or DMA address (when used with AEN"). Microprocessor addresses SA0 through SA19 are latched with the falling edge of "BALE." "BALE" is forced high during DMA cycles. Note: that "BALE" is usually used by the IO adapter only to latch the LA17-LA23 address lines (or the decode of LA17-LA23 that indicates an address match for the IO adapter). "BALE" may not occur on all 8-bit Input/Output cycles (which use only address lines SA0-SA9 for device decoding) or on some 8-bit memory transfers.

Input/Output CH RDY (Input)
"Input/Output channel ready" is pulled low (not ready) by a memory or Input/Output device to lengthen Input/Output memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of clock cycles (167 nanoseconds). This signal should be held low for no more than 2.5 microseconds.

IRQ3-IRQ7, IRQ9-IRQ12 and IRQ 14 through 15 (Input)
Interrupt Requests 3 through 7, 9 through 12, and 14 through are used to signal the microprocessor that an Input/Output device needs attention. This interrupt requests are prioritized, with IRQ9 through IRQ 12 and IRQ 14 through IRQ15 having the highest priority (IRQ9 is the highest) and IRQ3 through IRQ7 having the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine). Interrupt 13 is used on the system board and is not available on the Input/Output channel. Interrupt 8 is used for the real-time clock.

-IOR (Input/Output)
'Input/Output Read' instructs an Input/Output device to drive its data onto the databus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the Input/Output channel. This signal is active low.

-IOW (Input/Output)
"-Input/Output Write" instructs an Input/Output device to read the data on the data bus. It may be driven by any microprocessor or DMA controller inthe system. This signal is active low.

-SMEMR (Output) -MEMR (Input/Output)
These signals instruct the memory devices to drive data onto the data bus. "-SMEMR" is active only when the memory decode is within the low 1Mb of memory space. "-MEMR" is active on all memory read cycles. "-MEMR" may be driven by any microprocessor or DMA controller in the system. -SMEMR" is derived from "-MEMR" and the decode of the low 1 Mb of memory. When a microprocessor on the Input/Output channel wishes to drive "-MEMR", it must have the address lines valid on the bus for one system clock period before driving "-MEMR active. Both signals are active LOW.

-SMEMW (Output) -MEMW (Input/Output)
These signals instruct the memory devices to store the data present on the data bus. "-SMEMW" is active only when the memory decode is within the low 1Mb of the memory space. "-MEMW" is active on all memory read cycles. "-MEMW" may be driven by any microprocessor or DMA controller in the system. "-SMEMW" is derived from "-MEMW" and the decode of the low 1Mb of memory. When a microprocessor on the Input/Output channel wishes to drive "-MEMW", it must have the address lines valid on the bus for one system clock period before driving "-MEMW" active. Both signals are active low.

DRQ0-DRQ3 and DRQ5-DRQ7 (Input)
DMA Requests 0 through 3 and 5 through 7 are asynchronous channel requests used by peripheral devices and the Input/Output channel microprocessors to gain DMA service (or control of the system). They are prioritized, with "DRQ0" aving the highest priority and "DRQ7" having the lowest. A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding "DMA Request Acknowledge" (DACK) line goes active. "DRQ0" through "DRQ3" will perform 8-bit DMA transfers; "DRQ5" through "DRQ7" will perform 16-bit transfers. "DRQ4" is used on the system board and is not available on the Input/Output channel.

-DACK to -DACK3 and -DACK5 to -DACK7 (Output)
-DMA Acknowledge 0 to 3 and 5 to 7 are used to acknowledge DMA requests (DRQ) through DRQ7). They are active low.

AEN (Output)
"Address Enable" is used to degate the microprocessor and other devices from the Input/Output channel to allow DMA transfers to take place. When this line is active, the DMA controller has control of the address bus, the data-bus READ command lines (memory and Input/Output, and the Write command lines (memory and Input/Output).

-REFRESH (Input/Output)
This signal is used to indicate a refresh cycle and can be driven by a microprocessor on the Input/Output channel.

T/C (Output)
"Terminal Count" provides a pulse when the terminal count for any DMA channel is reached.

-SBHE (Input/Output)
"Bus High Enable" indicates a transfer of data on the upper byte of the data bus, SD8 through SD15. Sixteen-bit devices use "-SBHE" to condition data bus buffers tied to SD8 through SD15.

-SBHE AND SA0 ENCODINGS:

-SBHE	SA0	FUNCTION
0	0	WORD TRANSFER
0	1	BYTE TRANSFER ON SD8-SD15
1	0	BYTE TRANSFER ON SD0-SD7
1	1	RESERVED

-MASTER (Input)
This signal is used with DRQ line to gain control of the system. A processor or DMA controller on the Input/Output channel may issue a DRQ to a DMA channel in cascade mode and receive a "-DACK". Upon receiving the "-DACK", an Input/Output microprocessor may pull "-MASTER" low, which will allow it to control the system address, data, and control lines (a condition known as tri-state). After -MASTER" is low, the Input/Output microprocessor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a Read or Write command. If this signal is held low for more than 15 microseconds, system memory may be lost because of a lack of refresh.

-MEM CS16 (Input)
"-MEM16 Chip Select" signals the system board if the present data transfer is a 1 wait-state, 16-bit memory cycle. It must be derived from the decode of LA17 through LA23. Note that this requires that all 16-bit memory devices must occupy at least 128 kbytes of address space on the Bus and must not decode the SA address lines as a condition to driving "-MEM CS16" as the SA lines are not valid in time to meet the "-MEM CS16" timing requirements. "-MEM CS16" should be driven with an open-collector or tri-state driver capable of sinking 20 mA.

-Input/Output CS16 (Input)

"-Input/Output 16 bit Chip Select" signals the system board that the present data transfer is a 16-bit, 1 wait-state, Input/Output cycle. It is derived from an address decode. "Input/Output CS16" is active low and should be driven with an open collector or tri-state driver capable of sinking 20mA.

OSC (Output)

"Oscillator" (OSC) is a high-speed clock with a 70 nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle.

-OWS (Input)

The "Zero Wait State" (-OWS) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-bit device without wait cycles, "-OWS" is derived from an address decode gated with a Read or Write command. In order to run a memory cycle to an 8-bit device with a minimum of two wait states, "-OWS" should be driven active one system clock after the Read or Write command is active gated with the address decode for the device. Memory Read and Write commands to an 8-bit device are active on the falling edge of the system clock. Note that "-OWS" must be synchronous to the system clock (CLK) and meet specific set-up and hold timing requirements to prevent undesirable system malfunction (see section 3.1.2.). "-OWS" is active low and should be driven with an open collector or tri-state driver capable of sinking 20mA.

3.4 CONTROLLER HARDWARE ARCHITECTURE

The OMTI 8000 Series are partitioned into two distinct sections - the floppy disk logic and the Winchester disk logic. These two sections share the same physical PCB board but are otherwise independent. This allows full concurrent operations between these two sections. For example, DMA data transfer could be occurring at the same time programmed Input/Output data transfers are occurring on the fixed disk.

SECTION 4

HOST/CONTROLLER SOFTWARE INTERFACE

4.1 OVERVIEW

From the perspective of software executing on the host the OMTI 8000 Series look like two independent controllers
- one controller for the floppy disk
- and one controller for the fixed disk.

The host communicates with the OMTI 8000 Series through two independent sets of registers
- one set for the floppy
- and the other set for the fixed disk.

The host can issue commands, such as READ, via these registers following a specific protocol.

A typical sequence of events for the host to issue commands to the OMTI 8000 Series controller would be :

1) Set up a "Command Descriptor Block" or CDB in memory which contains information required by the controller.

2) Send the CDB to the controller by writing it one byte at a time to the I/O register.

3) Receive or send data if required via programmed I/O or DMA.

4) Receive status via the I/O register set.

A list of commands, their functions and the format of the CDB is given in :

Section 5 for the Fixed disk,

Section 6 for the Floppy disk,

The following sections describe the two register sets and the protocol the host must follow when reading or writing these registers.

4.2 FIXED DISK REGISTERS

There are four registers (or I/O ports) that the host uses to access the fixed disk. The registers have different meanings when they are read or written. These registers are normally located at the I/O address listed in table 4-1 but maybe altered by jumpers described in Section 2. Table 4-1 list these registers and table 4-2 describes these registers in more detail.

Table 4-1 OMTI 8000 Series I/O Port Addresses

PORT	REGISTERS READ	WRITE
320_H	DATA IN	DATA OUT
321_H	STATUS	RESET (Function)
322_H	CONFIGURATION	SELECT (Function)
323_H	N/A	MASK

Table 4-2 OMTI 8000 Series I/O Registers

REGISTER	DEFINITION
Data-In	This is an 8 or 16 bit register depending on the state of the controller (determined by the C/D bit in the STATUS register). It is used to read data a word at a time, or status (not SENSE data) a byte at a time. When the C/D bit is 1 only bits 0-7 are valid. When C/D is 0 all 16 bits are valid with bits 8-15 containing byte 1 and bits 0-7 containing byte 0.
Data Out	This is an 8 bit or 16 bit register depending on the state of the controller (determined by the C/D bit in the STATUS register). It is used to write data a word at a time or commands a byte at a time. When the C/D bit is 1 only bits 0-7 are valid. When C/D is 0all bits are valid with bits 8-15 containing byte 1 and bits 0-7 containing byte 0.
Status	Used to send bit significant control information from the controller to the system. Bit 7 Not Used (Set to 1) Bit 6 Not Used (Set to 1) Bit 5 IREQ (Interrupt Request) 0 = No Interrupt 1 = Command Complete If the Interrupt Enable bit of the MASK byte has been previously set, this bit is set when the controller enters the STATUS State. This bit is set with IRQ14 on the System Bit 4 DREQ (DMA Request) 0 = No DMA Request 1 = DMA Cycle Requested If the DMA ENABLE bit of the MASK BYTE has been previously set, and if the controller is in the DATA State, this bit is set along with DRQ3 on the System Bus when a byte transfer is required to or from the system. Bit 3 BSY (Busy) 0 = Controller is Idle 1 = Controller Selected Bit 2 C/D (Command/Data) 0 = Word being transferred is data, status. 1 = Byte being transferred is a command or status byte NOTE: This bit can be used to determine if word or byte transfers are being done. When C/D is 1 then only bits 0-7 are used in the Data In or Data Out register. When C/D is 0 then all 16 bits in the Data In and Data Out register are valid. In this case byte 0 is in bits 8-15 and byte 1 is in bits 0-7.

Bit 1 I/O (In/Out)
0 = Direction of transfer is from the host to the controller.
1 = Direction of transfer is from the controller to the Host.
Bit 0 REQ (Request)
0 = No Transfer Required
1 = Request transfer of one byte or Word via Data In or Data Out register.

RESET — Writing any value to this register will cause the controller to be reset.
WARNING The host must wait 100 usec after a -RESET before issuing a SELECT.

CONFIG-URATION — Used to send the status of the drive configuration jumpers to the system. Typically, these are used by a BIOS to specify the type of drive(s) attached to the controller.
Bits 7-4 = not used (Set to 1)
Bit 3 = W4
Bit 2 = W3
Bit 1 = W2
Bit 0 = W1

SELECT — Writing any value to this register will cause the controller to begin a Selection Sequence and request a command transfer.

MASK — Enables and disables interrupts and DMA transfers.
Bits 7-2 Not used.
Bit 1 INTERRUPT ENABLE
0 = No system interrupt at data transfer completion.
1 = System interrupt at data transfer completion.
Bit 0 DMA ENABLE
0 = DMA not enabled. (Programmed I/O mode)
1 = DREQ is gated onto system bus on DRQ3 and DREQ set in STATUS register

4.3 FIXED DISK COMMUNICATION PROTOCOL

The fixed disk portion of the OMTI 8000 Series has six logical states which the host sequences through when issuing command. These states are :

RESET
IDLE
SELECTION
COMMAND
DATA
STATUS

The RESET STATE is entered by applying power to the controller (power - on -reset), by the reset signal on the system bus, or by writing the RESET Register (port 321). During this phase, the controller will initialize itself, will set default parameters (ST412) to the LUNs, will de-assert all control functions and clear all bits in the STATUS register. It will then enter the idle state.

WARNING: The host must wait 100 usec after a -RESET before issuing a SELECT.

The IDLE STATE is the only time the controller will respond to a select request. When the SELECT register (port 322) is written by the system, the controller enters the selection state.

During the SELECTION STATE, the controller responds to a selection request by asserting the BSY bit (bit 3) in the STATUS register (port 321). The controller then enters the command state.

The COMMAND STATE is when the controller requests the command bytes to be transferred from the system. First, the C/D bit (bit 2) of the STATUS register is set. Then the REQ bit (bit 0) of the STATUS register is set, asking for the first command byte to be written to the DATA OUT register (port 320) in BYTE mode (bits 0-7). When the command byte is written, the controller de-asserts the REQ bit and moves the command byte into its buffer. This handshaking is repeated until all command bytes are transferred. C/D is then de-asserted and the data state is entered.

The DATA STATE is when data is transferred to or from the system. If no data is required, the status state is entered. Data can be transferred in either programmed mode I/O mode or DMA word mode, as defined by the DMA ENABLE bit in the MASK register. In the programmed I/O mode, data is transferred by handshaking in the same fashion as the command transfer. When the controller requires a word to be transferred, it will set the REQ bit in the STATUS byte. Depending on the direction of transfer (as defined by the I/O bit in the STATUS byte), the system must either write a word to the DATA OUT register or read a word from the DATA IN register. Either action will cause REQ to be cleared. These steps will be repeated until all the data required by the controller has been transferred.

If the DMA ENABLE bit in the MASK byte has been previously set, data will be transferred in DMA mode. When the controller requires a word to be transferred, it will set the DRQ7 bit on the system bus, requesting a DMA cycle. The DREQ bit of the STATUS byte is also set. After the data word has been transferred, DACK7 from the system will clear DRQ7. The DMA transfer will proceed in this fashion until all of the data required by the controller has been transferred.

During the STATUS STATE, the controller will place a STATUS register in the data in register bits 0-7. See Section 5.3 for detailed information on the STATUS byte.

The controller sets the C/D bit and the I/O bit in the STATUS byte. If the INTERRUPT ENABLE bit was previously set in the MASK register, the REQ bit is set in the STATUS byte, along with IRQ14 on the system bus. When the STATUS byte is read from the DATA IN register, the controller clears the IREQ and IRQ14 (if enabled), clears C/D, I/O, and BSY bits in the STATUS Registers, and enters the idle state.

4.4 FLOPPY DISK REGISTERS

There are five I/O registers (eight bits) which the host accesses to communicate with the floppy disk portions of the OMTI 8000 Series controller. The address of these registers is selectable (re: Section 3) to be either at the primary or secondary location as shown in table 4-3.

Table 4-3

I/O Address			
Primary	Secondary	Read	Write
$3F2_H$	372_H	N/A	Digital Output Register
$3F4_H$	374_H	Main Status Register	N/A
$3F5_H$	375_H	Data Register	Data Register
$3F6_H$	376_H	N/A	Additional Control Register
$3F7_H$	377_H	Digital Input Register	Diskette Control Register

The host uses the Main Status Register and Data Register to issue commands to and receive status from the controller. The Digital Input, Digital Output and Diskette Control Register, Additional Control Registers are used to control the specific drive functions as shown:

Register	Definition
Digital Output	This is an output only register used to control drive motors, drive selection, interrupts/DMA and reset. All bits arecleared when a channel reset occurs. Bit 7 Reserved Bit 6 Reserved Bit 5 Drive B Motor Enable when 1 Bit 4 Drive A Motor Enable when 1 Bit 3 Interrupts and DMA enable when 1 Bit 2 Reset floppy disk function when 0. The floppy disk function comes outof reset when this bit is set to 1 Bit 1 Reserved Bit 0 Select Drive-A. A 0 selects drive A, a 1 selects drive B
Digital Input	This is an input only register used by the host to get floppy drive information Bit 7 This bit is received from pin 34 of the floppy disk control cable and is normally used for diskette change status. Bits 0 through 6 are Reserved.

Diskette Control

This is an output only register which givesthe controller data rate information. All bits are cleared when a channel reset occurs.

Bits 2-7 Reserved.

Bits	1	0	Data Rate
	0	0	500 Kbits/sec
	0	1	300 Kbits/sec
	1	0	250 Kbits/sec
	1	1	Reserved

Additional Control

The diskette additional control register is an output-only register user to control the floppy write precompensation and the disk drive dual motor speed control.

Bit 7 Reserved
Bit 6 Reserved
Bit 5 Floppy Interface Pin 6
Bit 4 Floppy Interface Pin 4
Bit 3 Floppy Interface Pin 2 (Dual Speed Floppy Control)
Bit 2 Floppy Write Precompensation 2
Bit 1 Floppy Write Precompensation 1
Bit 0 Floppy Write Precompensation 0

FLOPPY WRITE PRECOMPENSATION TABLE

BITS 0-2			FLOPPY DISKETTE DATA RATE		
PRECOMP BIT			500KBPI	300KBPI	250KBPI
2	1	0	PRECOMP	PRECOMP	PRECOMP
0	0	0	Ons	Ons	Ons
0	0	1	62.5ns	104.2ns	125ns
0	1	0	125ns	208.3ns	250ns
0	1	1	187.5ns	312.5ns	375ns
1	0	0	250ns	416.7ns	500ns
1	0	1	250ns	416.7ns	500ns
1	1	0	312.5ns	520.8ns	625ns
1	1	1	312.5ns	520.8ns	625ns

All bits in this register are cleared by a channel reset to insure compatability with other controllers.

Main Status

This is a read only register used in conjuntion with the Data register to transfer command to the controller.

Bit 7 Request for Master (RQM). Indicates that the data register is ready to send or receive data. This bit must be used by the host to perform handshaking functions between the host and controller. This bit is cleared by reading or writing the Data Register.

Bit 6 Data In/Out (DIO) indicates direction of data transfer. If DIO = 1 then transfer is from the Data Register to the host. If DIO = 0 then it is from the host to the Data Register.

Bit 5 Non-DMA mode when 1. This can occur only during execution phase.

Bit 4 When 1 the controller is busy executing a command.

Bit 3,2 Reserved

Bit 1 Drive B is in the Seek mode when 1.

Bit 0 Drive A is in the Seek mode when 1.

Data This register is used to transfer information to/from the host. This register can be logically viewed as several registers in a stack with only one presented at any time. Data bytes are read out of or written into the Data register in order to program a command or obtain the results after the execution of a command.

4.5 FLOPPY DISK PROTOCOL

The host sends commands to the controller by sending several bytes of information to the controller (via the Data register) synchronized with bits 6 and 7 in the Status register. The sending of command data is called the command phase. The controller then goes "Busy" and executes the command (the command phase). Upon completion of the command the controller becomes "not busy" and results may be obtained from the Data register again synchronized with bit 6 and 7 in the Status register. Floppy commands, parameters and results are listed in section 6.0.

SECTION 5

FIXED DISK FUNCTIONS

5.1 COMMANDS

5.1.1 COMMAND DESCRIPTOR BLOCK (CDB)

The processor specifies the operation or command to be executed by the controller by sending 6 or 10 bytes called a Command Descriptor Block (CDB) as follows :

6 Byte COMMAND FORMAT

Bit / Byte	7	6	5	4	3	2	1	0
0	Command Class			Operation Code				
1	C 10	0	LUN	Head Number				
2	C 09	C 08	Sector Number					
3	Cylinder low (C 07-C 00)							
4	Interleave or Block Count							
5	Control Byte							

Byte 0 — Bits 7,6 and 5 identify the class of the command.
Bits 4,3,2,1, 0 contain the command Opcode.

Byte 1 — Bit 7 identifies bit 10 of the disk cylinder number (MSB)
Bit 6 is not used.
Bit 5 identifies the Logical Unit Number (LUN).
Bits 4,3,2,1, 0 contain the disk head number to be selected.

Byte 2 — Bits 7 and 6 contain bits 9 and 8 respectively of the disk cylinder number.
Bits 5,4,3,2,1, 0 contain the disk sector number

Byte 3 — Bits 7,6,5,4,3,2,1, 0 are the eight least significant bits of the disk cylinder number.

Byte 4 — Bits 7,6,5,4,3,2,1, 0 specify the Interleave Factor for the FORMAT command or the Block Count for disk I/O commands.

Byte 5 — Bits 7,6,5 contain the command Control Byte.
Bits 4,3,2,1,0 are not used.

Refer to the COPY command for the format of the 10 byte CDB.

5.1.2 COMMAND SET SUMMARY

COMMANDS COMMON to ALL MODELS

COMMANDS	CODE (HEX)	Length in Bytes (b) or Blocks (B) COMMAND	DATA
TEST DRIVE READY	00	6	0
RECALIBRATE	01	6	0
REQUEST SENSE	03	6	4(b)
FORMAT DRIVE	04	6	0
READ VERIFY	05	6	0
FORMAT TRACK	06	6	0
FORMAT BAD TRACK	07	6	0
READ	08	6	1-256(B)
WRITE	0A	6	1-256(B)
SEEK	0B	6	0
READ ECC BURST ERROR LENGTH	0D	6	1(b)
READ DATA FROM SECTOR BUFFER	0E	6	1(B)
WRITE DATA TO SECTOR BUFFER	0F	6	1(B)
ASSIGN ALTERNATE TRACK	11	6	4(b)
CHANGE CARTRIDGE	1B	6	0
READ DATA TO BUFFER	1E	6	Up to buffer size
WRITE DATA FROM BUFFER	1F	6	Up to buffer size
COPY	20	10	1-256(B)
RAM DIAGNOSTICS	E0	6	0
READ ID	E2	6	4(b)
DRIVE DIAGNOSTIC	E3	6	0
CONTROLLER INT. DIAGNOSTIC	E4	6	0
READ LONG	E5	6	1(B)+4 or 6(b)
WRITE LONG	E6	6	1(B)+4 or 6(b)

COMMAND SPECIFIC to the ST506/412 drievs

INITIALIZE DRIVE CHARACTERISTICS	0C	6	8(b)

COMMANDS SPECIFIC to the ESDI drives.

CHECK TRACK FORMAT	10	6	0
READ ESDI DEFECT LIST	37	6	256 (b)
READ CAPACITY	EC	6	10(b)

5.2 CONTROL BYTE

The Command Control Byte is the last Byte in the CDB. It specifies the error recovery procedure during the command execution.

CONTROL BYTE FORMAT

Bit	7	6	5	4	3	2	1	0
	R	E/B	C	x	x	S	S	S

R = RETRY option
E = ECC option on data ECC error (READ command)
B = FORMAT BUFFER option.
C = PHYSICAL ADDRESS CONVERSION option
X = Don't care.
S = STEP Option

Bit 7 (R) DISABLE RETRY. If this bit is set to 1, the controller will not perform any retries. Upon encountering an error, the controller will terminate the command by indicating that an error occured in the Status register.Bit 7 is valid for those commands involving retries. If this bit is set to 0, the controller will perform up to 8 retries. If any of the retries is successfull, the controller will attempt to process the next requested block (if any). If the retries are not successfull, the controller will terminate the command by indicating that an error occured in the Status register.
The retry algorithm is 4 retries, 1 recalibration, 4 retries.

Bit 6 (E) DISABLE ECC (Error Correction Code, valid during READ commands). If this bit is set to 1, the controller will terminate the command upon encountering an ECC error after performing retries (if enabled). If the data error is correctable, the corrected data is transferred to the host.
If this bit is set to 0, the controller enables its error correction scheme (ECC) for read retries. The controller will terminate the command upon encountering an uncorrectable ECC error after performing retries (if enabled). If no errors occur, the command is terminated with no error reported in the Status register.

(B) ENABLE FORMAT BUFFER. If this bit is set to 1, the controller will use the data contained in the controller data buffer when formatting each data field. No data is transferred from the host during the FORMAT command. A WRITE DATA BUFFER command should be issued prior to the FORMAT command to specify the data field.
If this bit is set to 0, the controller will write a "$6C_H$" pattern in each data field during a FORMAT command.

Bits 5 (C) ENABLE SECTOR ADDRESS CONVERSION. If this bit is set to 1, the controller will perform a sector address conversion based on 16 heads per cylinder. The number of sectors per track used in the conversion is based on the SECTORS PER TRACK Jumpers (W10 and W9), see Table. This conversion is useful when there is a different number of sectors per track (ESDI) than the DOS is using (17).
If this bit is set to 0, the controller will NOT convert the sector address contained in the CDB.

Warning : The INITIALIZE DRIVE CHARACTERISTICS command (OC_H) must include the true number of heads value of the drive (not 16 as used for the conversion).

Bits 2,1,0. These bits define the STEP option as follows :.

Bits 2	1	0	
0	0	0	3 milliseconds per step.
0	0	1	10 microseconds, buffered step
0	1	0	25 microseconds, buffered step
0	1	1	50 microseconds, buffered step
1	0	0	200 microseconds, buffered step
1	0	1	70 microseconds, buffered step
1	1	0	3 milliseconds per step
1	1	1	3 milliseconds per step

5.3 STATUS REGISTER

Status is available to the host in the Data Register during the Status State at the end of a command. It indicates whether or not an error was detected during execution of the command.

Bit:	7	6	5	4	3	2	1	0
	0	0	LUN	0	S	S	e	0

E = Command status

Bit 1 e = Command status. A value of zero indicates a successfully completed command. A value of one indicates an abnormal condition was encountered during the command execution and caused command termination and ending status with the Command Status Condition (bit 1) set to one.

S = Error Recovery Status

Bit 2,3 (S) Error Recovery Status (valid only for commands which read data from the disk)

Bit 3	2	
0	0	No error recovery
0	1	One retry accomplished successfully
1	0	More than one retry accomplished successfully
1	1	Error correction done successfully

NOTE: On multiple sector transfers, these bits will reflect the worst ECC Retry Count/Correction. If one Retry is done successfully on more than one sector, then Bits 3, 2 = 0 1 respectively. If more than one Retry is done successfully on at least one sector, then bits 3, 2 = 1 0 respectively. If ECC was applied on any sector regardless of the Retry count, bits 3, 2 = 1 1 respectively.

Bit 5 Indicates the LUN address of the device associated with this command.

Bits 7,6,4,0. Set to zero.

5.4 FIXED DISK COMMANDS

The following commands can be issued to the controller.

5.4.1 TEST DRIVE READY Command (00_H)

This command selects the LUN specified and returns a zero status in the Status Register to indicate that the unit is selected, ready and seek (ST drives) or seek/command (ESDI drives) is complete. In the case of a unit with a removable disk, zero status also indicates that a cartridge is installed. The controller will wait up to 50 seconds for the drive to come ready.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0
1	0	0	LUN	0	0	0	0	0
2 through 5	Zero value							

5.4.2 RECALIBRATE Command (01_H)

ST drives : The drive specified by the LUN is stepped toward the outside cylinder until either:

1. Track Zero signal is detected or
2. More steps have been issued than available cylinders for the device type.

The controller issues one step pulse, waits for seek complete, and tests the Track 000 signal.

For LUNs assigned as Removable drive the RECALIBRATE command is performed by issuing the number of step pulses equal to the number of cylinders specified for this drive plus 5 at the buffered rate and then waiting for the Track 000 signal.

ESDI drives : This command selects the LUN specified and issues a recalibrate to cylinder zero.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	1
1	0	0	LUN	0	0	0	0	0
2	Zero value							
3	Zero value							
4	Zero value							
5	0	0	0	0	0	S	S	S

5.4.3 REQUEST SENSE Command (03_H)

This command returns four sense bytes of information for the specified Logical Unit Number during the Data In phase of the command execution. The sense is valid for the Command Status (c) just presented to the host during the Status State of the previous unsuccessfully completed command. Sense data will be cleared upon reception of any subsequent command issued to the controller.

The Error code byte (Byte 0) of the Sense Data is always valid, however, the sector address (defined by bytes 1, 2 and 3) is only valid if the previous command terminated in error. Bit 7 set to 1 indicates the validity of the sector address. If bit 7 is set to 0, the sector address is not valid. Four sense bytes are returned during the Data In State of the command execution.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	1
1	0	0	LUN	Zero value				
2	Zero Value							
3	Zero Value							
4	Zero Value							
5	0	0	C	0	0	0	0	0

SENSE DATA FORMAT

Bit / Byte	7	6	5	4	3	2	1	0
0	SENSE CODE							
1	C 10	0	LUN	HEAD NUMBER				
2	C 09	C 08	SECTOR NUMBER					
3	CYLINDER LOW (C 07 to C 00)							

SENSE DATA WORD FORMAT

Bit / Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	C10	0	LUN	HEAD NUMBER					SENSE CODE							
1	CYLINDER LOW C 07-C 00								C09	C08	SECTOR NUMBER					

See APPENDIX A for SENSE Codes

5.4.4 FORMAT DRIVE Command (04_H)

This command causes the specified Logical Unit Number (LUN) to be formatted using the Interleave Factor specified in byte 4. Formatting starts at the specified track and proceeds until the last track of the unit is formatted. Each track is formatted from index to index. The first sector formatted is always sector Zero. An interleave factor of Zero is set equal to one. Track and cylinder overflow is handled automatically by the controller.

If bit 6 of the Control Byte is set to 0, all data fields are written with the pattern "$6C_H$". If bit 6 of the Control Byte is set to 1, all data fields are written with the pattern contained in the controller data buffer. This allows "worst case" patterns to be written by executing a WRITE DATA BUFFER command prior to the FORMAT command.

The FORMAT command does NOT handle media defects. For verification of format, see the READ VERIFY command or the CHECK TRACK FORMAT command (ESDI drives only). For media defect handling, see the ASSIGN ALTERNATE TRACK command, or the FORMAT BAD TRACK Command.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0
1	C 10	0	LUN	HEAD NUMBER				
2	C 09	C 08	0	0	0	0	0	0
3	CYLINDER LOW (C 07 to C 00)							
4	0	0	0	INTERLEAVE VALUE				
5	R	B	C	0	0	S	S	S

5.4.5 READ VERIFY Command (05_H)

This command verifies ID and DATA integrity of the recorded data starting at the specified address and for the block count specified. This command functions exactly as the READ command with the exception of no data transfer to the host.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	1
1	C 10	0	LUN	HEAD NUMBER				
2	C 09	C 08	SECTOR NUMBER					
3	CYLINDER LOW (C 07 to C 00)							
4	BLOCK COUNT							
5	R	E	C	0	0	S	S	S

5.4.6 FORMAT TRACK Command (06_H)

This command causes the track specified to be formatted using the interleave factor defined in Byte 4. The track is written starting with index. The first sector after index is always sector zero. Interleave factor of zero is set to one. If bit 6 of the control byte is set to zero, all the data fields are written with "$6C_H$". If bit 6 of the control byte is set to one, data fields are written with whatever data is is the data buffer. This allows "worst case" patterns to be written by first executing a WRITE DATA BUFFER command.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0
1	C 10	0	LUN	HEAD NUMBER				
2	C 09	C 08	Zero value					
3	CYLINDER LOW (C 07 to C 00)							
4	0	0	0	INTERLEAVE VALUE				
5	R	B	C	0	0	S	S	S

5.4.7 FORMAT BAD TRACK Command (07_H)

This command is identical to the FORMAT TRACK command except that the defective track flag is set in the ID field. All subsequent accesses to the sectors on this track will result in Bad track Flag set errors.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	1
1	C 10	0	LUN	HEAD NUMBER				
2	C 09	C 08	Zero value					
3	CYLINDER LOW (C 07 to C 00)							
4	0	0	0	INTERLEAVE VALUE				
5	R	B	C	0	0	S	S	S

5.4.8 READ Command (08_H)

This command causes the number of blocks specified by byte 4 to be transferred from the specified LUN to the host. The command executes an implied seek to the starting sector specified. Up to 256 blocks can be transferred with a single READ command (If byte 4 is equal to zero, 256 sectors will be transferred).

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	0
1	C 10	0	LUN	HEAD NUMBER				
2	C 09	C 08	SECTOR NUMBER					
3	CYLINDER LOW (C 07 to C 00)							
4	BLOCK COUNT							
5	R	E	C	0	0	S	S	S

5.4.9 WRITE Command ($0A_H$)

This command causes the number of blocks specified by byte 4 to be transferred from the host to the specified LUN. The command executes an implied seek to the starting sector specified. Up to 256 blocks can be transferred with a single WRITE command (If byte 4 is equal to zero, 256 sectors will be transferred).

Bit: / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	0
1	C 10	0	LUN	HEAD NUMBER				
2	C 09	C 08	SECTOR NUMBER					
3	CYLINDER LOW (C 07 to C 00)							
4	BLOCK COUNT							
5	R	0	C	0	0	S	S	S

5.4.10 SEEK Command ($0B_H$)

This command causes the device addressed by the LUN to be physically positioned to the cylinder as defined in bytes one to three. No attempt to verify seek position is made until a READ or WRITE command is issued. Completion status is returned to the host immediately after issuing all required step pulses or immediately after issuing the command (ESDI drives only). This allows overlap seek operations.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	1
1	C 10	0	LUN	HEAD NUMBER				
2	C 09	C 08	Zero value					
3	CYLINDER LOW (C 07 to C 00)							
4	0	0	0	0	0	0	0	0
5	R	0	C	0	0	S	S	S

5.4.11 INITIALIZE DRIVE CHARACTERISTICS Command ($0C_H$) not valid for ESDI drives.

This command allows the host to specify disk drive parameters for the specified LUN. This allows the controller to communicate with a wide variety of drives from the same or different vendors. The associated Parameter List, including all characteristics of the drive connected, is sent to the controller during the Data Out phase of the command execution. There is no access to the drive during execution of this command.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	0
1	0	LUN		0	0	0	0	0
2 through 5	Zero value							

During the Data Out phase of the command 8 bytes are sent as follows:

Parameter Block Byte Format

Bit / Byte	7	6	5	4	3	2	1	0
0	Maximum Number of Cylinders (MSB)							
1	Maximum Number of Cylinders (LSB)							
2	Maximum Number of Heads							
3	Start Reduced Write Current Cylinder (MSB)							
4	Start Reduced Write Current Cylinder (LSB)							
5	Start Write Precompensation Cylinder (MSB)							
6	Start Write Precompensation Cylinder (LSB)							
7	Set to zero.							

Parameter Block Word Format

Bit / Word	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
0	Maximum Number Cylinder (LSB)	Maximum Number Cylinder (MSB)
1	Start Reduced Wr. Current (MSB)	Maximum Number of Heads
2	Start Write Precomp. (MSB)	Start Reduced Wr. Current (LSB)
3	Zero Value	Start Write Precomp. (LSB)

BYTES 0-1 (Word 0) - NUMBER OF CYLINDERS : This word specifies the maximum number of cylinders on the Disk drive. The controller is capable to address up to 2048 cylinders.

BYTE 2 (LSB of WORD 1) - NUMBER OF HEADS : The value of this byte specifies the number of user heads on the Disk drive. The controller accepts a maximum of up to 16 heads with a value of 15 ($0F_H$). Any value greater than 07_H causes the reduced write current (WSI) function to be disabled.

BYTES 3-4 (MSB of WORD 1, LSB of WORD 2) - START REDUCED WRITE CURRENT CYLINDER : These 2 bytes specify the cylinder address where reduced write current is first applied. Reduced write current is applied to all cylinders greater than or equal to the value of these 2 bytes. This function is disabled for Removable and Fixed/Removable drives.

BYTES 5-6 (MSB of WORD 2, LSB of WORD 3) - START WRITE PRECOMPENSATION CYLINDER : These 2 bytes specify the cylinder address where write precompensation is first applied. Write precompensation is applied to all cylinders greater than or equal to the value of these 2 bytes. The amount of write precompensation is 12 nanoseconds.

5.4.12 READ ECC BURST ERROR LENGTH Command ($0D_H$)

This command returns one word of data during the Data In phase of the command execution. This word contains the length of the ECC error detected during the most recent correctable data field error. The length can range from 1 through 5 bits corrected for ST drives or from 1 to 11 bits corrected for ESDI drives. This command allows the host to decide on the validity of the corrected data. It is used in conjunction with the Disable ECC bit set on a READ command.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	1
1 through 5	Zero value							

ECC ERROR LENGTH BYTE FORMAT

Bit / Byte	7	6	5	4	3	2	1	0
0	ECC error length							

5.4.13 READ DATA FROM SECTOR BUFFER Command ($0E_H$)

Data from the controller buffer is returned to the host. The number of data bytes returned is equal to the jumper selectable sector size times the block count specified in byte 4 of the device control block up to a maximum block count as follows:

Sector Size	Block or Sector Count
512	15
1024	7
1056	7

This command is normally used immediately after a Read Data to Sector Buffer ($1E_H$) command has been issued to enhance performance when data transfers are done using programmed I/O. The controller does not access the disk drive during the execution of this command.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	0
1	Zero value							
2	Zero value							
3	Zero value							
4	BLOCK COUNT							
5	Zero value							

The READ BUFFER Command can also be used to model and status information about the controller. If a READ BUFFER COmmand is issued after a RESET is done (before any other command) the first XX bytes in the buffer contain the following information.

HEX Address	Contents
00 through 0D *	8x00VW.WMMDDYY
0E " 0F	ROM checksum. Word
10-bit 0 ***	ROM checksum error
11-bit 0 ***	Processor Register error
12-bit 0 ***	Buffer Ram error
13-bit 0 ***	Sequencer Register File Error
14-bits 7 & 6	0 - 0 8K buffer size 0 - 1 16K buffer size 1 - 0 32K buffer size 1 - 1 64K buffer size
15-1F	Reserved
20-2F	LUN 0 Default Values **
30-3F	LUN 1 Default Values **
40-4F	Rserved
50-5F	LUN 3 Default Values **

x = 1 for 8100. 2 for 8200. 5 for 8500. 6 for 8600
W = Revision level ** Default Values *** Valid only after a POWER ON or if a occurred diagnostic error (30_H) on the previous POWER ON or RESET.
MM = Month
DD = Day
YY = Year

LUN DEFAULT VALUES

Address		Winchester Disk
Byte 0		00
1		00
2		00
3		00
4	Cylinder High	01
5	Cylinder Low	31
6	Head Count	03
7	Sect/Track (depends on Jumpers)	?
8	Write Precompensation	00
9		80
10	Reduce Write Current	00
11		80
12	Step High	3C
13	Step Low	09
14	Reserved	00
15	LUN FLAG (see below)	82

LUN FLAG Byte, Bit Assignment (Byte 15 of LUN Default Values)

Bit 7 Reserved

Bit 0 & 1 BLOCK SIZE
00 = 512 Bytes/sect (17 sect/track)
01 = 512 Bytes/sect (18 sect/track)
10 = 1024 Bytes/sect
11 = 1056 Bytes/sect

Bits 3 & 2 Reserved

Bit 4 0 = Soft Sector format
1 = Hard Sector format

Bits 5 & 6 DRIVE TYPE

0 0 = Standard ST506/412 (Fixed)
0 1 = ESDI (Fixed)
1 0 = Standard ST506/412 (Removeable)
1 1 = ESDI (Removeable)

5.4.14 WRITE DATA TO SECTOR BUFFER Command ($0F_H$)

This command causes data to be written from the host to the controllers buffer. The number of data bytes that can be written is limited to the jumper selectable sector size times the block count specified in byte 4 of the device control block up to a maximum block count as follows:

Sector Size	Block or Sector Count
256	31
512	15
1024	7
1056	7

The controller does not access the disk drive during the execution of this command.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	1
1	Zero value							
2	Zero value							
3	Zero value							
4	BLOCK COUNT							
5	Zero value							

5.4.15 CHECK TRACK FORMAT Command ($0F_H$). Valid for ESDI drives only.

This command checks the integrity of the track specified against CRC, ECC value.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0
1	C 10	0	LUN	HEAD NUMBER				
2	C 09	C 08	Zero Value					
3	CYLINDER LOW (C 07 to C 00)							
4	0	0	0	0	0	0	0	0
5	R	0	C	0	0	S	S	S

5.4.16 ASSIGN ALTERNATE TRACK Command (11H)

This command is used to assign an alternate track to the track specified in bytes 1 to 3, so that any future accesses to the blocks on the specified track cause the controller to automatically access those blocks on the alternate track. This command sets flags in the ID field and writes the alternate track address in all blocks on the specified track. The alternate track is then formatted with flags set to indicate that this track has been assigned as an alternate track. Future direct accesses to the alternate track will result in an error. Interleave factor of zero is set to one.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	1
1	C 10	0	LUN	HEAD NUMBER				
2	C 09	C 08	Zero Value					
3	CYLINDER LOW (C 07 to C 00)							
4	0	0	0	INTERLEAVE VALUE				
5	R	B	C	0	0	S	S	S

The following 4 bytes (2 words), representing the alternate track address, are sent to the controller during the Data Out phase of the command execution.

ALTERNATE TRACK ADDRESS Descriptor Block - Byte Format

Bit / Byte	7	6	5	4	3	2	1	0
1	C 10	0	0	HEAD NUMBER				
2	C 09	C 08	Zero Value					
2	CYLINDER LOW (C 07 to C 00)							
3	Zero Value							

Note : Data written on the original track as well as on the alternate track will be destroyed. The controller does not check if the track assigned as alternate track has been previously used as alternate track for another track. A track assigned as an alternate may not have an alternate track assigned to it.

ALTERNATE TRACK ADDRESS - Descriptor Block - Word Format

Bit / Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	C09	C08	Zero Value						C10	0	0	HEAD Number				
1	Zero Value								CYLINDER LOW C07- C00							

5.4.17 START/STOP Command ($1A_H$) Valid for ESDI drives only.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	1	0
1	0	LUN	Zero Value					
2	Zero Value							
3	Zero Value							
3	Zero Value							START
5	Zero Value							

To start the unit, the Start bit shall be set to one.
To stop the unit, the Start bit shall be set to zero.
This command returns status immediately after receiving the command bytes, then does not wait for the start or stop spindle operation to complete.

5.4.18 CHANGE CARTRIDGE Command ($1B_H$)

This command is valid only for Removable disk drives. The command causes the "Change Cartridge " line (J2-Pin 2) to be asserted for a period of one (1) millisecond.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	1	1
1 through 5	Zero Value							

5.4.19 READ DATA TO BUFFER ($1E_H$)

This command reads data from the disk to the controller's buffer. It does not transfer the data to the host. The number of data blocks that can be read is limited by the controller's Buffer size as follows:

Sector Size	Block or Sector Count
512	15
1024	7
1056	7

This command can be used in conjunction with the READ DATA FROM BUFFER to enhance performance when data transfer is done in programmed I/O mode.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	0
1	C 10	0	LUN	HEAD NUMBER				
2	C 09	C 08	SECTOR NUMBER					
3	CYLINDER LOW (C 07 to C 00)							
4	BLOCK COUNT							
5	R	E	C	0	0	S	S	S

5.4.20 WRITE DATA FROM BUFFER ($1F_H$)

This command writes data from the controller's buffer to the disk. The number of sectors written is specified by the block count parameter but is limited by the controller's buffer size as follows:

Sector Size	Block or Sector Count
512	15
1024	7
1056	7

An error will be returned if the block count exceeds the above limits.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1
1	C 10	0	LUN	HEAD NUMBER				
2	C 09	C 08	SECTOR NUMBER					
3	CYLINDER LOW (C 07 to C 00)							
4	BLOCK COUNT							
5	R	E	C	0	0	S	S	S

5.4.21 COPY Command (20_H)

This command copies a specified number of blocks (byte 4) from a Source LUN to a Destination LUN. Source and Destination LUN's may be the same. Block sizes on both Source and Destination LUN's must be identical. No data is transferred to the host.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0	0
1	C 10	SOURCE LUN		HEAD NUMBER				
2	C 09	C 08		SECTOR NUMBER				
3	CYLINDER LOW (C 07 to C 00)							
4	BLOCK COUNT							
5	C 10	DEST. LUN		HEAD NUMBER				
6	C 09	C 08		SECTOR NUMBER				
7	CYLINDER LOW (C 07 to C 00)							
8	Zero Value							
9	R	E	C	0	0	S	S	S

Note: If source and destination LUNs have different step rates, the step rate specified in the control byte should be the slower of the two.

5.4.22 READ ESDI DEFECT LIST Command (37_H)

This command cause the specified Logical Unit Number (LUN) to return 256 bytes of drive manufacturer recorded DEFECT LIST during the Data In phase of the command execution. Only the list for the specified HEAD will be returned.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	1	1	0	1	1	1
1	0	0	LUN	HEAD NUMBER				
2	Zero Value							
3	Zero Value							
4	Zero value							
5	Zero Value							

DEFECT LIST Data Format
Header

Bit / Byte	7	6	5	4	3	2	1	0
0	MONTH							
1	DAY							
2	YEAR							
3	HEAD NUMBER							
4	Zero Value							
5	Zero Value							

Bytes 0 through 2 return the date at which the list was recorded.

Defect Descriptor Format

6	CYLINDER (MSB)
7	CYLINDER (LSB)
8	BYTE COUNT FROM INDEX (MSB)
9	BYTE COUNT FROM INDEX (LSB)
10	ERROR LENGTH (IN BITS)

Each defect is listed with a 5 bytes field as described above.

End of List Format

xx-4	FF_H
xx-3	FF_H
xx-2	FF_H
xx-1	FF_H
xx	FF_H

Five FF_H bytes indicate the end of the DEFECT LIST.
The maximum number of defects is 50 per head.

5.4.23 RAM DIAGNOSTIC Command ($E0_H$)

This command performs a pattern test on the internal controller buffer.

Bit / Byte	7	6	5	4	3	2	1	0
0	1	1	1	0	0	0	0	0
1 through 5	Zero Value							

5.4.24 READ ID Command ($E2_H$)

This command returns 4 bytes (2 words) of the ID field of the sector specified during the Data In phase of the command execution. Only one sector is processed per READ ID command.

Bit / Byte	7	6	5	4	3	2	1	0
0	1	1	1	0	0	0	1	0
1	C 10	0	LUN	HEAD NUMBER				
2	C 09	C 08	Zero Value					
3	CYLINDER LOW (C 07 to C 00)							
4	Zero Value							
5	R	0	C	0	0	S	S	S

READ ID Descriptor Block

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	0	C 10	C 09	C 08
1	CYLINDER LOW (C 07 to C 00)							
2	FLAGS			0	HEAD NUMBER			
3	SECTOR NUMBER							

READ ID Descriptor Block - Word Format

Bit / Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CYLINDER LOW C07-C00								0	0	0	0	0	C10	C09	C08
1	SECTOR NUMBER								FLAGS				0	HEAD NUMBER		

Byte 2, HEADS/ FLAGS bit are defined as follows :

Bit	0	=	Head 1
Bit	1	=	Head 2
Bit	2	=	Head 4
Bit	3	=	Head 8
Bit	4	=	0
Bit	5	=	Alternate Track Flag
Bit	6	=	Bad Track with Alternate Assigned
Bit	7	=	Bad Track

5.4.25 DRIVE DIAGNOSTIC Command ($E3_H$)

This command causes the controller to perform the following drive functions; recalibrate sequentially seek to every track and read sector 0.

Bit / Byte	7	6	5	4	3	2	1	0
0	1	1	1	0	0	0	1	1
1	0	LUN		0	0	0	0	0
2	Zero Value							
3	Zero Value							
4	Zero Value							
5	R	0	0	0	0	S	S	S

5.4.26 CONTROLLER INTERNAL DIAGNOSTICS Command ($E4_H$)

This command causes the controller to perform some internal diagnostics including ROM Checksum RAM test, sequencer test and Z8 self test. See Appendix A SENSE code type 3 for detailed error codes.

Bit / Byte	7	6	5	4	3	2	1	0
0	1	1	1	0	0	1	0	0
1 Through 5	Zero Value							

5.4.27 READ LONG Command ($E5_H$)

This command returns the Block size equal to the jumper selected sector size (512, 1024 or 1056) of data plus 4 bytes (for ST506/412 drives) or 6 bytes (for ESDI drives) of ECC data.

Bit / Byte	7	6	5	4	3	2	1	0
0	1	1	1	0	0	1	0	1
1	C 10	0	LUN	HEAD NUMBER				
2	C 09	C 08	SECTOR NUMBER					
3	CYLINDER LOW (C 07 to C 00)							
4	BLOCK COUNT							
5	R	0	C	0	0	S	S	S

5.4.28 WRITE LONG Command ($E6_H$)

This command requires the Block size to be equal to the jumper selected sector size (512, 1024 or 1056) of data plus 4 bytes (for ST506/412 drives) or 6 bytes (for ESDI drives) of ECC data.

Bit / Byte	7	6	5	4	3	2	1	0
0	1	1	1	0	0	1	1	0
1	C 10	0	LUN	HEAD NUMBER				
2	C 09	C 08	SECTOR NUMBER					
3	CYLINDER LOW (C 07 to C 00)							
4	BLOCK COUNT							
5	R	0	C	0	0	S	S	S

5.4.29 READ CONFIGURATION Command (EC_H) valid for ESDI drives only.
This command returns to the host the drive configuration.

READ CONFIGURATION Command Descriptor Block

Bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number				Reserved			
2 through 4	Reserved							
5	0	0	0	0	0	0	0	LINK

HARD and SOFT SECTORED Drives

0	NUMBER OF CYLINDERS (MSB)
1	NUMBER OF CYLINDERS (LSB)(-1)
2	NUMBER OF HEADS (-1)
3	NUMBER OF SECTORS (-1)
4	DRIVE CONFIGURATION WORD (MSB)
5	DRIVE CONFIGURATION WORD (LSB)
6	ISG AFTER INDEX

SOFT SECTORED Drives

7	PLO SYNC Field (ID)
8	PLO SYNC Field (DATA)
9	ISG AFTER SECTOR

HARD SECTORED Drives

7	PLO SYNC Field (ID/DATA)
8	ISG AFTER SECTOR
9	Zero Value

DRIVE CONFIGURATION WORD (Bytes 4 and 5) :
The following tables lists the supported functions of the ESDI drive configuration.

Byte 4	Bits	
ESDI TAPE Drive	7,15	CHECK CONDITION status.
FORMAT SPEED TOLERANCE GAP REQUIRED	6,14	Supported
TRACK OFFSET OPTION AVAILABLE	5,13	Not supported as yet.
DATA STROBE OPTION	4,12	Not supported as yet.
ROTATIONAL SPEED TOLERANCE IS > 0.5 %	3,11	Supported
TRANSFER RATE T > 10 MHZ	2,10	Not Supported
TRANSFER RATE T = 10 MHZ	1,9	Supported
TRANSFER RATE T = 5 MHZ	0,8	Supported

Byte 5	Bits	
ESDI REMOVABLE MEDIA	7	Supported
ESDI FIXED MEDIA	6	Supported
ESDI MOTOR START/STOP OPTION	5	Supported
HEAD SWITCHING TIME > 15 MICROSECONDS	4	Supported
RLL ENCODED, NOT MFM	3	Controller ignores
ESDI SOFT SECTORED	2	Supported
ESDI HARD SECTORED	1	Supported
Reserved	0	

PLO SYNC Field, ISG after INDEX and ISG after SECTOR :
Bytes 6, 7,8,9
The controller accepts a value of up to 255 or FF_H for each of these fields.

SECTION 6

FLOPPY DISK FUNCTIONS

6.1 FLOPPY DISK COMMAND SUMMARY

The following is a list of commands that may be issued to the Floppy section of the disk controller.

READ DATA

FORMAT A TRACK

SCAN EQUAL

SCAN LOW OR EQUAL

SCAN HIGH OR EQUAL

RECALIBRATE

SENSE INTERRUPT STATUS

SPECIFY

SENSE DRIVE STATUS

SEEK

INVALID

6.2 DESCRIPTION OF SYMBOLS

The following are descriptions of the symbols used in the "Command Definitions" later in this section.

A0	Address Line 0- A0 selects the main status register, and a 1 selects the data register.
C	Cylinder Number-Contains the current or selected cylinder number in binary notation.
D	Data-Contains the data pattern to be written to a sector.
D7-D0	Data Bus-An 8-bit data bus in which D7 is the most significant bit and D0 is the least-significant.
DTL	Data Length- When N is 00, DTL is the data length to be read from or written to a sector.
EOT	End of Track- The final sector number on a cylinder.
GPL	Gap Length - The length of gap 3 (spacing between sectors excluding the VCO synchronous field).
H	Head Address - The head number, either 0 or 1, as specified in the ID field.
HD	Head - The selected head number, either 0 or 1. (H=HD in all command words).

HLT Head Load Time - The head load time in the selected drive (2 to 256 milliseconds increments for the 1.2Mbyte drive and 4 to 512 milliseconds in 4 millisecond increments for the 320K-byte drive).

HUT Head Unload Time - The head unload time after a read or write operation (0 to 240 milliseconds in 16 millisecond increments for the 1.2M-byte drive and 0 to 480 milliseconds in 32 millisecond increments for the 320K-byte drive.

MF FM or MFM Mode - A0 selects FM mode and a 1 selects MFM. (MFM is selected only if it is implemented).

MT Multitrack - A1 selects multitrack operation. (Both HD0 and HD1 will be read or written).

N Number - The number of data bytes written in a sector.

NCN New Cylinder - The new cylinder number for a seek operation.

ND Non-Data Mode - This indicates an operation in the non-data mode.

PCN Present Cylinder Number - The cylinder number at the completion of a Sense interrupt status command (present position of the head).

R Record - The sector number to be read or written.

R/W Read/Write - This stands for either a 'read' or 'write' signal.

SC Sector - The number of sectors per cylinder.

SK Skip - This stands for skip deleted-data address mark.

SRT This 4 bit byte indicates the stepping rate for the diskette drive as follows:

1.2M-Byte Diskette Drive

1111 1 millisecond
1110 2 milliseconds
1101 3 milliseconds

320K-Byte Diskette Drive

1111 2 milliseconds
1110 4 milliseconds
1101 6 milliseconds

ST0-ST1 Status 0-Status 3 - One of the four registers that stores status information after a command is completed.

STP Scan Test - If STP is 1, the data in contiguous sectors is compared with the data sent by the processor during a scan operation. If STP is 2, then alternate sectors are read and compared.

US0-US1 Unit Select - The selected driver number encoded the same as bits 0 and 1 of the digital output register (DOR).

6.3 FLOPPY COMMANDS

The following are commands that may be issued to the floppy section of controller.
NOTE: An X is used to indicate a don't care condition.

6.3.1 READ DATA command

Command Pnase : The following bytes are issued by the processor in the command phase:

MT	MF	SK	0	0	1	1	0
X	X	X	X	X	HD	US1	US0
C							
H							
R							
N							
EOT							
GPL							
DTL							

Result Phase : The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

6.3.2 FORMAT A TRACK Command

Command Phase: The following bytes are issued by the processor in the command phase :

0	MF	0	0	1	1	0	0
X	X	X	X	X	HD	US1	US0
N							
SC							
GPL							
D							

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

6.3.3 SCAN EQUAL Command

Command Phase: The following bytes are issued by the processor in the command phase:

MT	MF	SK	1	0	0	0	1
X	X	X	X	X	HD	US1	US0
C							
H							
R							
N							
EOT							
GPL							
STP							

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

6.3.4 SCAN LOW OR EQUAL Command

Command Pnase: The following bytes are issued by the processor in the command phase:

MT	MF	SK	1	1	0	0	1
X	X	X	X	X	HD	US1	US0
C							
H							
R							
N							
EOT							
GPL							
STP							

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

6.3.5 SCAN HIGH OR EQUAL Command

Command Phase: The following bytes are issued by the processor in the command phase:

MT	MF	SK	1	1	1	0	1
X	X	X	X	X	HD	US1	US0
C							
H							
R							
N							
EOT							
GPL							
STP							

Resul: Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

6.3.6 RECALIBRATE Command

Command Phase: The following bytes are issued by the processor in the command phase:

0	0	0	0	0	1	1	1
X	X	X	X	X	0	US1	US0

Result Phase: This command has no result phase.

6.3.7 SENSE INTERRUPT STATUS Command

Command Phase: The following bytes are issued by the processor in the command phase:

0	0	0	0	1	0	0	0

Result Phase: The following bytes are issued by the controller in the result phase:

STO
PCN

6.3.8 SPECIFY Command

Command Phase: The following bytes are issued by the processor in the command phase:

0	0	0	0	0	0	1	1
(	SRT	)	(	HUT	)		
(	HLT				)	ND	

Result Phase: This command has no result phase.

6.3.9 SENSE DRIVER STATUS Command

Command Phase: The following bytes are issued by the processor in the command phase:

0	0	0	0	0	0	1	0
X	X	X	X	X	HD	US1	US0

Result Phase: The following bytes are issued by the controller in the result phase:
ST3

6.3.10 SEEK Command

Command Phase: The following bytes are issued by the processor in the command phase:

0	0	0	0	1	1	1	1
X	X	X	X	X	HD	US1	US0
NCN							

Result Phase: This command has no result phase.

6.3.11 INVALID Command

Command Phase: The following bytes are issued by the processor in the command phase:

Invalid Codes

X	X	X	X	X	HD	US1	US0

Result Phase: The following bytes are issued by the controller in the result phase:
ST0

6.4 COMMAND STATUS REGISTERS

The following is information about the command status registers ST0 through ST3.

6.4.1 Command Status Register 0 (ST0)

The following are bit definitions for command status register 0.

Bit 7-Bit 6 Interrupt Code (IC)

- 00 Normal Termination of Command (NT) - The command was completed and properly executed.
- 01 Abrupt Termination of Command (AT) - The execution of the command was started but not successfully completed.
- 10 Invalid Command Issue (IC) - The issued command was never started.
- 11 Abnormal termination because, during the execution of a command, the 'ready' signal from the diskette drive changed state.

Bit 5 Seek End (SE) - Set to 1 when the controller completes the Seek command.

Bit 4 Equipment Check (EC)- Set if a 'fault' signal is received from the diskette drive, or if the 'track-0' signal fails to occur after 77 step pulses (Recalibrate Command).

Bit 3 and 2 Not Used - Always zero

Bit 1-Bit 0 Unit select 1 and 2 (US 1 and 2) - Indicate a drive's unit number at interrupt.

6.4.2 Command Status Register 1 (ST1)

The following are bit definitions for command status registers 1.

Bit 7 End of Cylinder (EC) - Set when the controller tries to gain access to a sector of a cylinder.

Bit 6 Not Used-Always 0.

Bit 5 Data Error (DE) - Set when the controller detects a CRC error in either the ID field or the data field.

Bit 4 Overrun (OR) - Set if the controller is not serviced by the main system within a certain time limit during data transfers.

Bit 3 Not Used - This bit is always set to 0.

Bit 2 No Data (ND) - Set if the controller cannot find the sector specified in the ID register during the execution of a Read Data, Write Deleted Data, or Scan Command. This flag is also set if the controller cannot read the ID field without an error during the execution of a Read ID command or if the starting sector cannot be found during the execution of a Read Cylinder command.

Bit 1 Not Writeable (NW) - Set if the controller detects a 'write-protect' signal from the diskette drive during execution of a Write Data, Write Deleted Data. or Format Cylinder command.

Bit 0 Missing Address Mark (MA) - Set if the controller cannot detect the ID address mark. At the same time, the MD of status register 2 is set.

6.4.3 Command Status Register 2 (ST2)

Bit 7 Not Used - Always zero.

Bit 6 ****control Mark (CM) - This flag is set if the controller encounters a sector that has a deleted data-address mark during execution of a Read Data or Scan command.

Bit 5 Data Error in Data Field (DD) - Set if the controller detects an error in the data.

Bit 4 Wrong Cylinder (WC) - This flag is related to ND (no data) and when the contents of C on the medium are different from that stored in the ID register, this flag is set.

Bit 3 Scan Equal Hit (SH) - Set if the contiguous sector data equals the processor data during the execution of a Scan command.

Bit 2 Scan Not Satisfied (SN) - Set if the controller cannot find a sector on the cylinder that meets the condition during a Scan command.

Bit 1 Bad Cylinder (BC) - Related to ND; when the contents of C on the medium are different from that stored in the ID register, and the contents of C is FF, this flag is set.

Bit 0 Missing Address Mark in Data Field (MD) Set if the controller cannot find a data address mark or a deleted data address mark when data is read from the medium.

6.4.4 Command Status Register 3 (ST3)

The following are bit definitions for command status register 3.

Bit 7 Not used - always zero.

Bit 6 Write Protect (WP) - Status of the 'write-protect' signal from the diskette drive.

Bit 5 Not used - always zero.

Bit 4 Track 0 (T0) - Status of the 'ready' signal from the diskette drive.

Bit 3 Not used - always zero.

Bit 2 Head Address (HD) - Status of the 'side-select' signal to the diskette drive.

Bit 1 Not used - always zero.

Bit 0 Not used - always 1.

APPENDIX A

SENSE CODE SUMMARY AND DESCRIPTION

SENSE BYTES

At completion of a command, if the Status Resister reports an error condition (Bit 1 set), the system may issue a REQUEST SENSE command (03_H) during which four sense bytes are returned (Byte 0 through 3 as follows).

SENSE DATA BYTE FORMAT

Bit / Byte	7	6	5	4	3	2	1	0
0	AV	0	TYPE		SENSE CODE			
1	C 10	0	LUN		HEAD NUMBER			
2	C 09	C 08	SECTOR NUMBER					
3	CYLINDER LOW (C 00-C 07)							

SENSE DATA WORD FORMAT

Bit / Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	C10	0	LUN		HEAD NO.				AV	0	TYPE		CODE			
1	CYLINDER LOW C07-C00								C09	C08	SECTOR NUMBER					

AV = Address Valid. If set, indicates that the error code in byte 0 applies to the sector address in bytes 1,2,3.

SENSE TYPE (Bits 5 and 4 of Byte 0 or Word 0):

5	4	
0	0	Drive Errors
0	1	Data errors
1	0	Command Errors
1	1	Diagnostic Errors

TYPE 0 - DRIVE ERRORS

5	4	3	2	1	0	
0	0	0	0	0	0	No error
0	0	0	0	0	1	No Index
0	0	0	0	1	0	No seek/command complete
0	0	0	0	1	1	Write/Drive Fault
0	0	0	1	0	0	Drive not selected/ not ready
0	0	0	1	1	0	No track or cylinder zero found
0	0	1	0	0	0	Seek/command in progress
0	0	1	0	0	1	Cartridge changed

TYPE 1 - DATA ERRORS

5	4	3	2	1	0	
0	1	0	0	0	0	ID CRC error (ESDI), ID ECC error (ST412)
0	1	0	0	0	1	Uncorrectable Data Error
0	1	0	0	1	0	ID address Mark not found
0	1	0	0	1	1	Data address mark found
0	1	0	1	0	0	Sector not found
0	1	0	1	0	1	Seek error
0	1	0	1	1	0	Sequencer/DMA failure
0	1	0	1	1	1	Write protected
0	1	1	0	0	0	Correctable Data Error
0	1	1	0	0	1	Bad track encountered
0	1	1	0	1	0	Illegal Interleave Factor
0	1	1	1	0	0	Unable to read Alternate Track data Illegal access to an alternate track
0	1	1	1	0	1	Alternate or Bad Track Already Assigned
0	1	1	1	1	0	No Alternate Track Found
0	1	1	1	1	1	Alternate Assigned To Itself

TYPE 2 - COMMAND ERRORS

5	4	3	2	1	0	
1	0	0	0	0	0	Invalid Command
1	0	0	0	0	1	Illegal Disk Address
1	0	0	0	1	0	Illegal Function for Drive Type
1	0	0	0	1	1	Volume Overflow

TYPE 3 - DIAGNOSTIC ERRORS

5	4	3	2	1	0	
1	1	0	0	0	0	RAM error
1	1	0	0	0	1	Z8 firmware checksum/internal diagnostic error

DESCRIPTION OF ERROR CODES

TYPE 0 - ERROR CODE DESCRIPTIONS

00 **No error or no sense information.** Indicates that there is no specific sense information to be reported for the designated Logical Unit Number. This is the case for the successful completion of the previous command. If a REQUEST SENSE command is issued when there is no error, the Sense information reported specifies the last Sector Address processed.

01 **No Index.** This indicates that during a FORMAT command, no INDEX signal was received from the Logical Unit Number selected within three seconds.

02 **No Seek/Command Complete.** This indicates that no SEEK COMPLETE (OMTI 5510 and 5527) signal or the SEEK/COMMAND COMPLETE (OMTI 6510) signal was received from the Logical Unit Number selected within three seconds.

03 **Write/Drive Fault.** This indicates that during a WRITE/FORMAT command, a fault condition occured. Refer to the disk drive specification for all possible conditions relating to this error.

04 **Drive Not Selected/Not Ready.** This error occurs when the specified drive did not return the DRIVE SELECTED signal or the DRIVE READY signal. Reasons for this error vary from drive to drive, however, a common fault is the select configuration jumpers located on the drive. Absence of cartridge or medium inserted in a removable drive may also cause this error.

06 **No Track zero or Cylinder zero found.** This indicates that during a RECALIBRATION (command or if retries are enabled) no Track or Cylinder zero was detected by the drive. This error occurs if the controller issued 5 steps more than the total number of cylinder as currently defined for this Logical Unit Number, and did not detect the TRACK ZERO or CYLINDER ZERO signal from the drive.

07 **Multiple Drives Selected.** This indicates that the controller detected multiple DRIVE SELECTED signals when it attempted to select the specified Logical Unit Number.

08 **Seek/Command in progress.** This indicates that a seek or command is in progress. This error code is only returned in response to a TEST UNIT READY command. The controller will report this error for every TEST UNIT READY command issued until the seek or command has completed.

09 **Cartridge Changed.** This indicates that the cartridge has been changed since the last access to the specified Logical Unit Number. This error code may only occur on Removable type drives.

TYPE 1 - ERROR CODE DESCRIPTION

10 **ID CRC .**This indicates that at least one ID field on the specified track has a CRC error. This error can only occur on a CHECK TRACK FORMAT command. If a CRC error was encountered on a READ or WRITE command, a RECORD NOT FOUND error will be reported. This is because there is no sure way to determine if the ID in error is the one the controller is searching for.

11 **Uncorrectable Data ECC.** This indicates that a data ECC error was detected which was uncorrectable. The sector in error is NOT transferred to the HOST and the command is terminated without exhausting the block count. The data can be recovered by issuing the READ DATA BUFFER command provided that no other command requiring the data buffer has been issued.

12 **ID Address Mark Not Found.** This indicates that the controller was unable to detect any ADDRESS MARK signals from the selected Logical Unit Number.

13 **Data Address Mark Not Found.** This indicates that the controller was able to locate the sector specified but was unable to locate the data address mark associated with it.

14 **Record Not Found.** This indicates that the controller was able to locate the correct cylinder and head numbers but was unable to locate the correct sector. An ID CRC error can also generate this error.

15 **Seek.** This indicates that a mis-compare of the cylinder and/or head occured between the specified sector address and the actual sector address recorded on the track selected.

16 **Sequencer/DMA.** This indicates that a sequencer/DMA overrun/underrun error occured. These functions are internal to the controller and inform about a serious hardware failure.

17 **Write Protected.** This indicates that during a WRITE/FORMAT command, the controller detected a WRITE PROTECTED signal from the selected Logical Unit Number.

18 **Correctable ECC.** This indicates that a READ command was issued with the DISABLE ECC bit SET and a correctable ECC was encountered. The corrected data will be transferred to the HOST; however, the command will be terminated exhausting the block count. A READ ECC BURST LENGTH command will specify the length of the ECC error. If the DISABLE ECC bit was cleared, the controller will automatically correct the data error and continue the command as if no data error had occurred.

19 **Bad Track Encountered.** This indicates that the specified track has previously been formatted with the BAD TRACK FLAG set in the ID field. It is not possible to access data on this track and the command will be terminated.

1A **Illegal Interleave Factor.** This indicates that a FORMAT/CHECK TRACK FORMAT command was issued with an INTERLEAVE FACTOR greater than the number of sectors on the track or during a CHECK TRACK FORMAT command, the recorded interleave factor did not match the INTERLEAVE FACTOR specified in the CDB.

1C **Illegal Access To An Alternated Track/Unable To Read The Alternate Track Address.** This indicates that a direct access to an alternate track was attempted or upon detecting the ALTERNATE and BAD TRACK flags both SET in an ID field the controller was unable to read the alternate track data specifying the destination cylinder.

1D **Alternate of Bad Track Already Assigned.** This indicates that the destination track of a FORMAT ALTERNATE TRACK command has previously been formatted as an alternate destination or bad. In order to use the specified track as an alternate destination, a FORMAT TRACK command must be issued.

1E **No Alternate Track Found.** This indicates that the controller was directed to an alternate track but did not find the ALTERNATE bit SET in the ID field.

1F **Illegal Alternate Track Address.** This indicates that a FORMAT ALTERNATE TRACK command was issued with the source and destination sector addresses equal.

TYPE 2 - ERROR CODE DESCRIPTION

20 **Invalid Command.** This indicates that the controller decoded a command code that it does not support.

21 **Illegal Disk Address.** This indicates that the controller received a command with a Sector Address beyond the capacity of the drive. Check the number of cylinders, heads and sector size that the drive is configured for.

22 **Illegal Function for Drive Type.** This indicates that a Change Cartridge command (HEX 1B) was issued to a LUN assigned as a Fixed drive type.

23 **Volume Overflow.** This indicates that after the commencement of a multiblock command, the end of volume was reached.

TYPE 3 - ERROR CODE DESCRIPTION

30 **RAM error.** This indicates that the controller detected a data error with its internal RAM buffer of 8K bytes.

31 **EPROM Checksum/Internal Diagnostic error.** This indicates that a checksum error was detected in the EPROM or the controller detected a Data Error in this sequencer register file.

APPENDIX B

INTERLEAVE SCHEME

512 BYTE SECTORS - 17 SECTORS PER TRACK

			INTERLEAVE FACTOR							
			0/1	2	3	4	5	6	7	8
			LOGICAL SECTOR NUMBERS							
P	S	0	0	0	0	0	0	0	0	0
H	E	1	1	2	3	4	5	6	7	8
Y	C	2	2	4	6	8	10	12	14	16
S	T	3	3	6	9	12	15	1	1	1
I	O	4	4	8	12	16	1	7	8	9
C	R	5	5	10	15	1	6	13	15	2
A		6	6	12	1	5	11	2	2	10
L		7	7	14	4	9	16	8	9	3
		8	8	16	7	13	2	14	16	11
		9	9	1	10	2	7	3	3	4
		10	10	3	13	6	12	9	10	12
		11	11	5	16	10	3	15	4	5
		12	12	7	2	14	8	4	11	13
		13	13	9	5	3	13	10	5	6
		14	14	11	8	7	4	16	12	14
		15	15	13	11	11	9	5	6	7
		16	16	15	14	15	14	11	13	15

1024 BYTE SECTORS - 9 SECTORS PER TRACK

			INTERLEAVE FACTOR			
			0/1	2	3	4
			LOGICAL SECTOR NUMBERS			
P	S	0	0	0	0	0
H	E	1	1	2	3	4
Y	C	2	2	4	6	8
S	T	3	3	6	1	1
I	O	4	4	8	4	5
C	R	5	5	1	7	2
A		6	6	3	2	6
L		7	7	5	5	10
		8	8	7	8	3

Note: Interleave factor of zero will be set to one.

Interleave factors greater than one half the total number of sectors per track are not recommended.

ABBREVIATIONS/MNEMONICS

ACK	Acknowledge
ADDR	Address
AM	Address Mark
ATN	Attention
BIOS	Basic input/output System
BSY	Busy
C/D	Control Data
CDB	Command Descriptor Block
CRC	Cyclic Redundancy Check
CYL	Cylinder
DB	Data Bit
D LUN	Destination Logical Unit Number
DP	Data Parity
DRVR	Driver
ECC	Error Correction Code
EPROM	Eraseable Programmable Read only Memory
FDC	Flexible Disk Controller
HD	Head
ID	Identification
I/O	Input/Output
LSB	Least Significant Bit
LSTTL	Low-Power Schottky Transistor-Transistor Logic
LUN	Logical Unit Number
MFM	Modified Frequency Modulation
MHz	Megahertz

ns	Nanosecond
NRZ	Non-Return to Zero
PHY	Physical
RAM	Random Access Memory
RCVR	Receiver
REQ	Request
RST	Reset
SEC	Sector
SEL	Select
S LUN	Source Logical Unit Number
TPI	Track Per Inch
TRK	Track
TTL	Transistor-Transistor Logic
us	Microsecond
VCO	Voltage Control Oscillator
VLSI	Very Large Scale Integration
WSI	Equivalent to: Reduced Write Current
XCVR	Transceiver

APPENDIX C

BIOS INSTALLATION PROCEDURE

The 8000 Series controllers may be delivered as an option with two (2) EPROMs containing an IBM PC/AT DOS compatible BIOS. The EPROMs are inserted in the empty sockets on the PC mother board.

IBM AT (256K):

- the eprom labeled	"EVEN ADDRESSES"
should be inserted into the socket marked	U17.
- the eprom labeled	"ODD ADDRESSES"
should be inserted into the socket marked	U37.

TANDY 3000 (128K):

- the eprom labeled	"EVEN ADDRESSES"
should be inserted into the socket marked	U60.
- the eprom labeled	"ODD ADDRESSES"
should be inserted into the socket marked	U58.

To install the BIOS in other AT compatibles, please contact SMS technical support for socket locations.

You may attach up to two (2) ESDI Winchester drives or up to two (2) ST412 Winchester drives to the 8000 Series controller. You may or may not mix ESDI and ST412 type drives. Jumper settings for ESDI/ST412 drive types are shown below.

Floppy Support:
The 8200 and 8600 controllers provide floppy disk support which is fully AT bus and hardware compatible. Therefore, you may remove the AT Winchester/floppy controller (if installed) and connect the floppy cable to connector J7 on the 8200 or 8600 controller to support the floppy drive. To enable floppy support, jumper W7 must be installed.

Case when a disk controller is already installed:
If you already have a Winchester disk (non-ESDI) attached to IBM AT controller and you wish to attach an ESDI drive to the 8500 or 8600 controller, you may leave the AT controller in place. In this case, only one of the two controllers should control the floppy drive. To avoid conflicts between the two floppy controllers, one of the two controllers must be strapped for the secondary floppy base I/O address and the other for the primary floppy base I/O address.

To set the AT controller to :
- the secondary base address, a jumper must be installed in E1-E2.

Then the 8500 or 8600 controller must be set to :
- the primary base address, with the jumper W7 installed.

To set the 8500 or 8600 controller to :
- the secondary base address, jumper W7 must be removed.

Then the AT controller must be set to :
- the primary base address, a jumper must be installed in E2-E3.

NOTE: IBM's SETUP utility should NOT be informed of the presence of any Hard disks attached to the 8000 Series controller. This utility is only concerned with those drives (if any) which are attached to the AT controller. Thus, if the only Hard Disk (s) installed in the system is (are) attached to the 8000 Series controller, the number of Hard Disks in the system must be reported as zero (0) when initializing the system configuration parameters in the SETUP_ utility.

IBM DOS version 3.1 has imbedded code in the system file IBMBIO.COM intended to patch certain AT Fixed Disk BIOS problems. This code, in certain instances, insists on talking to the AT controller and therefore will not access the 8000 Series controllers properly. The system file must be patched in order to avoid this imbedded AT controller specific code.
The recommended patch is as follows (NOTE: There is NO need to patch MS-DOS version 3.1 - the problem exists only in IBM DOS 3.1! Please ignore this patch if you are running on an AT compatible under MS-DOS!):

In order to edit IBMBIO.COM, you must change the attribute byte in the directory entry for that file in order to make it appear as a non-hidden, read/write file. Use DEBUG.COM to do this (all required keyboard input appears underscored):

```
DEBUG
-L CS:0 0 0 40                ;LOAD 1ST 40H ABSOLUTE SECTORS INTO CS:0
-D A00                        ;CS:A00 SHOULD POINT TO DIRECTORY ENTRY
                               FOR IBMBIO
-E A0B
-XXXX:A0B 20                  ;CHANGE ATTRIBUTE BYTE TO A 20H
-W CS:0 00 40                 ;WRITE THE 1ST 40H SECTORS BACK OUT
-Q                            ; EXIT DEBUG

DIR IBMBIO.COM                ;THIS FILE SHOULD NOW SHOW UP IN YOUR
                               DIRECTORY

DEBUG IBMBIO.COM              ;GO INTO DEBUG WITH THE FILE
-D 13DD                       ;AN ASCII DATE MARKER SHOULD APPEAR:
                               01/10/84
-E 13DD
-XXXX:13DD 31                 ;CHANGE THE DATE MARKER
-W
- writing xxxx bytes
-Q                            ;EXIT DEBUG

DEBUG
-L CS:0 0 0 40                ;LOAD 1ST 40H ABSOLUTE SECTORS INTO CS:0
-D A00                        ;CS:A00 SHOULD POINT TO DIRECTORY ENTRY FOR
                               IBMBIO
-E A0B
-xxxx:A0B 27                  ;CHANGE ATTRIBUTE BYTE BACK TO WHAT IT
                               WAS!
-W CS:0 0 0 40                ;WRITE THE 1ST 40H SECTORS BACK OUT
-Q                            ;EXIT DEBUG
```

This concludes the required patch.

DRIVE TYPE JUMPER SETTINGS (W1, W2, W3, and W4)

1) ESDI drive(s) - All four (4) jumpers must be on. The drive characteristics for an ESDI drive are provided by the drive itself. These characteristics will be stored in the uppermost 1K of system RAM which will be protected by the BIOS from use by the system or any applications.

2) ST412 drive(s) - The remaining fifteen (15) combinations of settings for jumpers W1, W2, W3, and W4 define the following drive types :

JUMPERS				DRIVE/MODEL	#CYL	#HEADS
W4	W3	W2	W1			
1	1	1	1	****THIS SETTING USED BY ESDI DRIVES****		
1	1	1	0	MAXTOR XT1140	918	15
1	1	0	1	VERTEX 170 CYNTHIA 570	987	7
1	1	0	0	CDC 9415-36	697	5
1	0	1	1	RODIME 352 MICROSCIENCE HH312	306	4
1	0	1	0	SEAGATE ST4051	977	5
1	0	0	1	SEAGATE ST4038	733	5
1	0	0	0	CMI 6640 TULIN 240 RODIME 203E	640	6
0	1	1	1	CMI 6426 TULIN 226 RODIME 202E	640	4
0	1	1	0	QUANTUM 540	512	8
0	1	0	1	DMA 360	612	2
0	1	0	0	MINISCRIBE 3012/3212	612	2
0	0	1	1	SEAGATE ST4026	615	4
0	0	1	0	ST225,PT925 (COGITO) CMI 3426	612	4
0	0	0	1	SEAGATE ST419 CMI 5619	306	6
0	0	0	0	SEAGATE ST412/212 CMI 5412 LAPINE 3522	306	4