July 10, 1968

Standard

Standard Computer Corporation
1411 W. Olympic Blvd.
Los Angeles, California 90015
Telephone (213) 387-5267

Mr. J. B. Campbell
Raytheon Company
Department 7
Box 509 Hartwell Road
Bedford, Massachusetts 01730

Dear Mr. Campbell:

We were very pleased to hear from you. Here are a few highlights of the newest addition to the STANDARD Computer product line.

The IC-4000 employs the same field-proven design technology used to advantage in the IC-6000. The key to the outstanding performance of the IC-4000 consists, in essence, of a computer-within-a-computer. By placing the most time consuming algorithms and control functions of FORTRAN IV in the faster, overlapped inner computer, programmed via a micro-coding language called MINIFLOW, compilation speeds up to 4000 statements per minute are being achieved.

In addition to FORTRAN operating under the control of a Monitor, STANDARD offers COBOL, an Assembler, Sort, and Utilities to service the full line of input-output devices: magnetic tape units, disk storage units, high-speed card readers, and high-speed printers.

The IC-4000 is offered in configurations priced from $276,900 to $465,100. Comparable lease/rental prices range from $7,685 to $12,385 per month with attractive discounts available for long-term lease agreements. The IC-4000 optionally emulates the 1130, 7040/7044, and 7090/7094 series.

Because of the low cost, speed, and versatility of the IC-4000, a personal discussion of your firm's specific needs will demonstrate how the IC-4000 can best serve you. We look forward to hearing from you.

Sincerely,

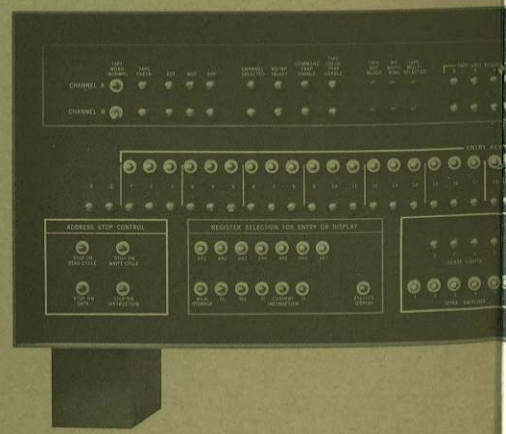
W. L. Woolley

W. L. Woolley
Director of Marketing

WLW:hr

Fortran is faster on the IC-4000

because two memories are better than one.



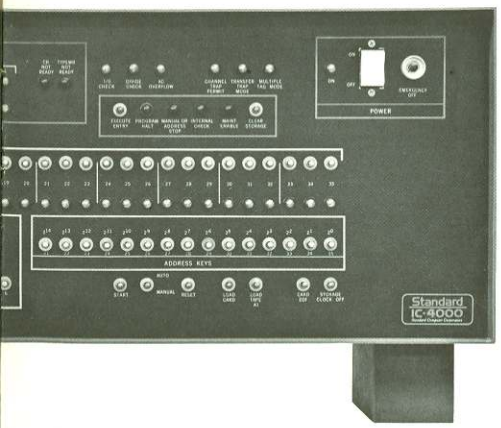
The Computer-Within-A-Computer

The IC-4000 employs the same field-proven design technology used to advantage in the earlier and larger IC-6000. The key to the outstanding performance of these computers consists, in essence, of building a computer-within-a-computer. With this fourth generation development, STANDARD Computer has departed from the traditional design of digital computers.

The IC-4000 is divided into two parts; external functional stations and the inner computer. The external functional stations consist of the main memory, arithmetic units and registers, input-output channels, input-output devices and the console, which perform their normally assigned tasks as in any computer system. The control or inner computer, which consists of a control memory, registers, and indicators, assumes the function of much of the wiring and control logic of conventional computer systems.

The IC-4000 FORTRAN system is constructed around the control memory which contains special micro-coded sequences and subroutines which provide the system with its outstanding speed and throughput. Time consuming compile-time and run-time algorithms, routines and control functions of FORTRAN IV are placed in the inner computer, thus increasing throughput and freeing main memory for data, tables, and user programs. The system fully utilizes the two memories and high speed internal registers of the inner computer. Both memories are overlapped with each other as well as with the Input-Output channels.

In addition to providing the FORTRAN system with increased speed and throughput, the inner computer can emulate the environment of another computer by specifying its characteristics in a micro-coded language called MINI-FLOW. Thus, the IC-4000 emulates the 1130, 7040/7044, and 7090/7094 and permits use of their proven program libraries without modification.



The IC-4000 is the scientists' and engineers' computer, optimizing FORTRAN through a unique process of cross-talk between separate control and main memories. Built completely with integrated circuits, the IC-4000 features a 500 nanosecond control memory which slams through highly used FORTRAN routines and achieves greater speed/volume throughput than other computers which market for twice the cost.

The system itself

IC-4000 System

STORAGE
32,768 words of main storage
2,048 words of read-write control storage

WORD SIZE
36 bits + parity in main computer
18 bits + parity in control computer

ACCESS TIME
2.0 microseconds in main computer
500 nanoseconds in control computer

ARITHMETIC UNIT
36 bit parallel look-ahead arithmetic unit with three working registers.
Selected sub-field arithmetic.

REGISTERS
7 index registers standard
4 accumulators standard

INTERVAL TIMER
Standard feature

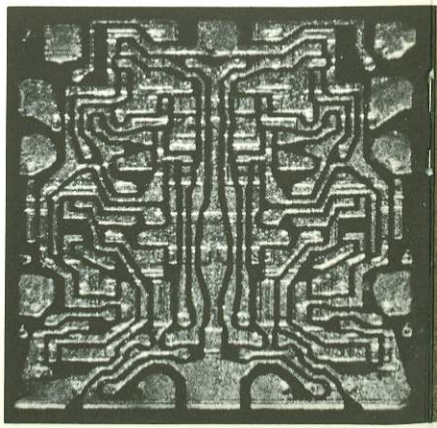
INTERRUPTS
4 levels standard

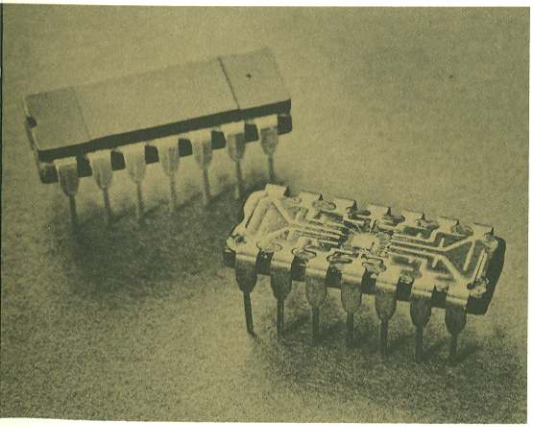
CHANNELS
2 selector-type channels available as options
Data rate up to 300,000 characters per second per channel

CONSOLE
On-line debugging aids, i.e. address stop, dynamic main and control memory display.

INPUT-OUTPUT DEVICES
Card Readers:
100, 800 or 1500 cards per minute fully buffered
Line Printers:
Fully buffered speeds up to 1250 lines per minute
132 print positions with up to 64 different characters
Magnetic Tape:
Speeds of 41.7 – 90kc
Completely IBM Compatible
Single-Capstan Design
Direct Access Devices
Disk Files with capacity of 9,666,000 characters
Average access of 85 milliseconds
Removable disk pack
Data transfer rate of 208,000 characters per second

PHYSICAL CHARACTERISTICS
Monolithic integrated circuit logic
Magnetic core storage
Less than 250 square feet of floor space required
Low power & air conditioning requirements





CTL integrated circuit, one of thousands used in the IC-4000. Close-up of chip on opposite page.

Programming Systems- A competitive edge for the IC-4000

The degree of effective utilization of any computing system is in direct proportion to the scope and versatility of the software. With the IC-4000, STANDARD has combined its experience in micro-programming and emulation systems to provide the ultimate in FORTRAN performance and throughput.

OPERATING SYSTEM

The IC-4000 can be either a tape or disk oriented system which allows the user to assemble, compile, and/or execute one program or a group of programs under control and coordination of a Monitor System. By coordinating the operation of the subsystems, the Monitor permits a job or a series of unrelated jobs to be processed with little or no operator intervention. By reducing the degree of operator participation, the Monitor ensures that jobs are processed faster and more efficiently.

All of the systems for the IC-4000 are designed as an integrated package and each of these programs contributes to a smoother running installation for each user. Consideration has been given in the design of the programming package to the use of the control memory, magnetic tapes, and the disk storage unit.

PROGRAMMING SYSTEMS

The full potential of the IC-4000 programming systems is realized through the full utilization of the two memory systems and high speed internal registers inherent in the hardware. With an effective word access time of 500 nanoseconds, the control memory contains special micro-coded sequences and subroutines which provide the system with its outstanding speed and throughput.

Programming Systems support for the IC-4000 is provided in two categories:

IC-4000 Monitor System / IC-4000 Basic System

The IC-4000 Monitor System is designed for residence on one single disk storage drive or one magnetic tape unit and consists of the following modules:

FORTRAN IV / Monitor / Subroutine Library / Assembler
SPOOL / Utilities / COBOL / SORT

Fortran on the IC-4000

CONCEPT

The IC-4000 FORTRAN was designed to be an extremely fast FORTRAN compiler processing up to 4000 statements per minute. It has all of the most often used features of FORTRAN IV plus many valuable extensions utilizing the two memories and a one-pass compile, load and execute system design.

DESIGN APPROACH

STANDARD's approach is based on three basic criteria:

Minimize compilation and compiled program execution time.
Exploit the control memory of the inner computer fully.
Provide complete FORTRAN IV.

The two memories of the IC-4000 offer a unique opportunity to develop an advanced FORTRAN IV based on modern concept of interpretive compiler design and compiled code execution. STANDARD has applied its experience in interpretive emulation and micro-programming techniques to assure the IC-4000 user maximum effectiveness in software specifically oriented to his problems.

GENERAL DISCUSSION

The design of a FORTRAN compiler is today a choice among many alternatives because of the extensive work that has already been done in FORTRAN compilers. The two most important factors influencing the design are hardware (configuration) and software (operating system).

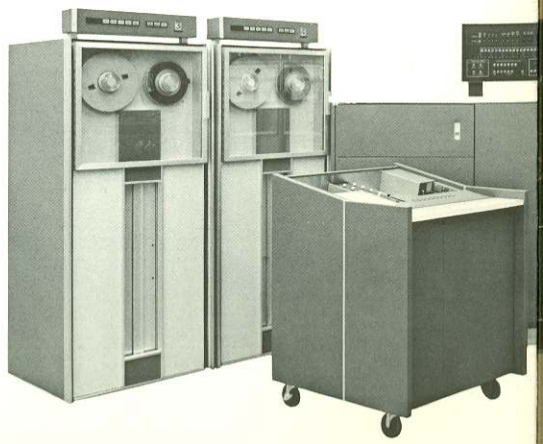
MINIFLOW, the micro-program resident in the read-write control memory specializes the logical design of the IC-4000 for a special purpose: FORTRAN with maximum effectiveness.

CONTROL MEMORY

The 500 nanosecond 2,048 word control memory is used to specialize the logical design of the IC-4000 for a specific purpose: FORTRAN with maximum effectiveness. In the IC-4000, specific hardware features and micro-programs have been devised for the benefit of both the compiler and its object program code. This assures the user of maximum efficiency by tailoring the CPU design to simplify compiler algorithms and condense the size of object programs.

MAIN MEMORY

Construction of the compiler is such that substantial memory space remains for intermediate table storage needed in the process of reducing source statements to executable object code form. Under this concept, very high compilation rates (up to 4,000 statements per minute) are obtained. In order to conserve space, commonly used operations are built into the CPU instruction repertoire. In other cases, closed subroutines are involved. Therefore, the algorithms which operate on various internal structures (scanning, table building, table look-ups, attribute verification, and code production) make most economical use of main memory locations.



Monitor

The disk or tape resident Monitor is a batch processing monitor with the ability to mix sub-programs in combinations of compiler, symbolic, and machine languages, and to compile, and/or assemble, or execute without operator intervention. Provision is made to stack input and output from many runs, compile and execute, and to call for programs and sub-programs from a library as required. A *loader* is included with the Monitor to facilitate ease of operation and to insure a smooth, integrated approach to job processing.

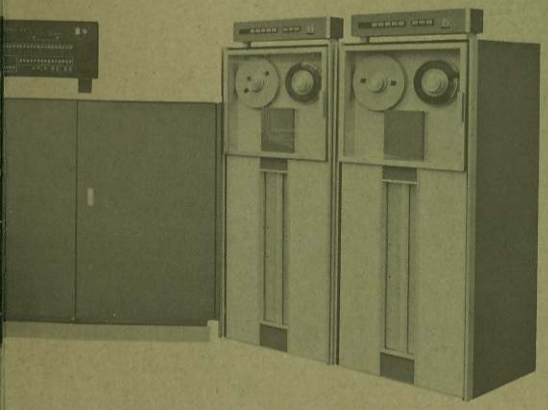
Attractive options

EMULATION

Programs written for the 1130, the 7040/7044 and the 7090/7094 run on the IC-4000 computers specified with the emulation option.

PROBLEM ADAPTION

Utilizing the Inner Computer Assembly Program (ICAP), the user can problem adapt the IC-4000 through intermixing micro-programming and the machine language code.



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DATAMATION 68
April

new products

PRODUCT OF THE MONTH

Standard Computer Corp. has extended the concepts developed for the IC-6000 (DATAMATION, Feb. '67, p. 77) to bring out the IC-4000. While the earlier machine amounted to a low-cost 7094, the 4000 is intended to be a general-purpose computer system, aimed at the scientific/engineering market.

Price range is $7685 to $12,385 per month or $276,900 to $465,100 for purchase. This puts it in the range between the IBM 1130 and 360/44, where it has plenty of company with the CDC 3150 and smaller 3100 configurations, the EMR 6050, the Sigma 5, larger GE-415's, and the 360/40. But Standard's main pitch is better price/performance than its host of rivals.

To achieve this, the company is using its dual-memory approach: a main core unit of 32K and a 2048-word control core unit. Main memory handles 36-bit words with a 2 usec cycle time; the control memory has a 500 nsec access time to its 18-bit words. This smaller memory can be set up with what Standard calls micro-code to offer, in effect, wired-in software. (A FORTRAN IV compiler is ready in this form and others, including COBOL, will follow.) An example of the results is that the 4000 can compile up to 4000 FORTRAN IV statements per minute.

The IC-4000 uses monolithic integrated circuits, has 36-bit-parallel operation, several levels of priority interrupt, word- and character-oriented instructions, seven index registers, and single- and double-precision floating point. Special "problem adapted" instructions are available on request, by use of the control memory. Overlapped I/O channels have a data transfer rate of 300K char/sec.

Peripherals, all buyouts, include card reader, line printer, single-capstan IBM-compatible tape units, and disc pack units. Options are emulators for the IBM 1130, 7040/44, and 7090/94. First deliveries are scheduled for August this year and Standard is aiming at 120-day delivery.

The company, started in late 1965, now has a half dozen of its IC-6000's installed and another 10 on order. For information:

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A look at the inner computer concept in the standard IC-4000

STANLEY GREENBLATT, Auerbach Info, Inc.

Nonconventional design approach permits a user to structure a computer to his own specifications

The conventional approach to computer architecture permanently fixes the computer's instructional repertoire by decoding each instruction with wired-in logic, but Standard Computer Corp., a small company in California, has developed a system for decoding each machine level instruction by a separate subroutine or microprogram written in Standard's MINIFLOW language.

Standard has spent several years implementing this provocative concept in computer architecture. It is an attempt to free the user from the confines of the hardware designers.

Because MINIFLOW is a software feature, one computer can be given the characteristics of any other computer by loading it with an appropriate package of MINIFLOW routines. This feature allows a Standard computer to be utilized in a variety of applications. Currently, Standard supplies MINIFLOW packages that allow a single computer to function as a stand-alone system with supporting software, as an emulator that can use the emulated machine's software, or as an experimental computer system that the user can change with instructions that modify MINIFLOW.

Although the stand-alone and emulating capabilities are of more practical interest, the experimental capability of Standard computers is certainly the most exciting. In principle, any user with sufficient interest, ingenuity, and computer time (perhaps the latter is the more formidable obstacle) can write his own MINIFLOW programs and design a computer to his specifications. Building on the basic hardware system provided by Standard, a pencil, some paper, and a card punch achieve the production status currently held by the wires, chips, and the soldering iron.

The system contains a separate hardware component, the Inner Computer, for storing MINIFLOW routines; the Inner Computer's wired-in logic decodes and implements each MINIFLOW instruction. In effect, an Inner Computer, loaded with a MINIFLOW package, reacts in the same fashion as does a more conventional read-only memory. Because the Inner Computer is controlled by MINIFLOW rather than by factory-installed hardware, the Standard design represents a softening of the read-only memory approach to computer architecture.

Currently, Standard manufactures the IC-4000, a general-purpose 36-bit, word-oriented computer, and the IC-7000, a timesharing computer. The Inner Computer, an essential component in both, will be described here. All references are to Model 9(IC-M9), found in the IC-4000.

Standard Computer uses the term target system to describe the machine produced by a given MINIFLOW package. The target system instruction repertoire is called the object language.

Standard supplies a selection of MINIFLOW packages for the IC-4000; these give the user the choice of emulating second generation 6-bit character-oriented machines or of using the computer as a stand-alone system. When the computer is used as an emulator, the object language instruction repertoire is identical to the emulated machine's instruction repertoire. As a consequence, the user who devoted significant time and money to software does not have to reprogram. Moreover, Standard's emulating target system instruction execution times compare quite favorably with those of the emulated system.

Standard designers achieve favorable system performance characteristics in their computers by separating working storage into two parts: main memory and control memory. For the IC-4000, main memory holds 32,768 36-bit words, and the memory cycle time is 2 μsec per word. Main memory stores programs written in the target system's machine language. The IC-4000's control memory holds 2048 18-bit words, and the memory cycle time is 1 μsec per two words. Control memory stores MINIFLOW subroutines.

All data transfer between the computer and peripheral devices occurs through a buffer area in control memory. Control memory and main memory communicate through registers in the inner computer. The division of storage into two parts confines the inherently higher cost of a high-speed mem-

ory to the part (the control memory) that requires rapid program execution.

Because an emulated target system behaves just like the emulated machine, except for instruction execution times, specific functions such as arithmetic modes and operations, branching and memory referencing, indexing, indirect addressing, and i/o procedure all depend on the particular target system.

Located in the cpu, the Inner Computer holds all the hard-wired logic and software components necessary for translation of object machine language instructions by MINIFLOW. The Inner Computer has access to MINIFLOW routines and can modify individual MINIFLOW instructions. In addition, IC-M9 contains all the hard-wired logic and registers needed for decoding individual MINIFLOW instructions.

The principal hardware components that the IC-M9 uses to decode individual object language instructions are: the main engine—for primary arithmetic, logical, and shifting operations; the mini engine—for MINIFLOW program sequence control and shift counting; the wired-in-sequence—for fetching object instructions and operands from main memory and performing effective address computation; and the Precondition Bits — for modifying individual MINIFLOW instructions. Programing priority in the IC-M9 is maintained by the scheduler, a scanning device that activates program levels on a priority basis.

Standard has designed into the IC-M9 two major software components for controlling the object language instruction's decoding by a MINIFLOW routine; these are the translator table and the control and transfer vector (C&TV). The translator table is a software table designed for the target system. It contains an entry for each object language instruction, such as entries that specify the precondition bit settings and that designate the selection of one of 64 C&TVs. A C&TV, an 18-bit word in control memory, stores the entry address to the object instruction's MINIFLOW decoding routine and contains bits that establish sequencing of the wired-in-sequence. A more detailed description of each major component of the IC-M9 follows.

The main engine is the computational workhorse of the inner computer. It contains a 36-bit adder/subtractor, three special 37-bit (1 sign bit and 36 data bits) registers called the main engine registers, and 12 general-purpose registers referred to as the register stack.

The main engine registers perform all arithmetic, logical, and shifting operations. In addition, they provide a path for address and data exchanges between main memory and control memory. When fetched from main memory, a target system object language instruction is stored in a main engine register during decoding and/or address modification.

The 12 general-purpose registers comprising the register stack operate as the target system registers. Among the register stack components, one 37-bit register serves as the target system accumulator and one of the three 36-bit registers usually serves as the target machine accumulator extension register. The complement of registers is completed by seven 15-bit index registers for object instruction address modification and a 15-bit program counter that supplies the next sequential instruction's address in main memory.

Both the object language program and MINIFLOW can access all the main engine registers. Further, MINIFLOW can control data transfer between the registers.

The mini engine is the inner computer component that controls MINIFLOW program sequencing and shift counting. It accomplishes these operations through three registers; an 8-bit register that stores the shift count or skip distance during execution of a MINIFLOW instruction, an 11-bit register that acts as the MINIFLOW routine's program counter, and an 11-bit register that stores the return address of a call to a MINIFLOW routine.

Eleven precondition bits modify individual instructions in a stored MINIFLOW routine. According to their setting, the precondition bits can modify the sign of control memory operands and main engine register operands, cause a skip on a tested machine condition, and control data flow between registers.

Because individual MINIFLOW instructions can be used by more than one object language instruction, appropriate precondition bit settings for decoding a given object language instruction are specified by Standard Computer Corp. as entries in the translator table supplied for each target system. In addition,

Available MINIFLOW emulators.

MINIFLOW SYSTEM	EMULATED MACHINE	MACHINE CONFIGURATIONS NOT SUPPORTED
MS-EM94-01	IBM 7094	Console keyboard input; line printer; card punch; disk storage drives
MS-EM44-01	IBM 7044	Console keyboard input; card punch; disk storage drives
MS-EM14-01	IBM 1401	Console keyboard input; disk storage drives

DEVICES	PERIPHERAL DEVICE	RATED SPEED
Mass storage	1063-01 Disk storage drive (7.2 x 10^6 8-bit bytes)	145,000 bytes/sec
	1066-01 Disk storage drive (28.8 x 10^6 8-bit bytes)	290,000 bytes/sec
Console typewriter	1002-01 Console printer keyboard	15 char/sec
Printed output	1020-01 Line printer	1250 lines/min
Punched card	1010-01 Card reader	100 cards/min
	1011-01 Card reader	800 cards/min
	1012-01 Card reader	1500 cards/min
	1013-01 Card punch	100-275 cards/min
Magnetic tape	1729-02 Magnetic tape unit (7-channel)	41,700 or 60,000 char/sec
	1729-03 Magnetic tape unit (7-channel)	62,550 or 90,000 char/sec
	1080-01 Magnetic tape unit (7-channel)	41,700 char/sec
	1080-02 Magnetic tape unit (7-channel)	41,700 or 60,000 char/sec
	1080-03 Magnetic tape unit (7-channel)	62,550 or 90,000 char/sec

Peripheral devices available for the Standard IC-4000. Though manufactured by other firms, the devices are plug-to-plug compatible.

MINIFLOW instructions can change precondition bit settings, enhancing MINIFLOW's capability.

The wired-in-sequence (WIS) cycles through a series of steps, each performing a function that is designed into the system hardware and cannot be changed by the programer. WIS steps access control or main memory and perform all indexing and indirect addressing specified in the object language instruction. The program controls the point of entry to the WIS cycle and the particular steps used by the WIS through the settings of the control bits in a C&TV. Since the program can skip some of the steps in the WIS cycle, the programer can control the sequence of steps performed.

The WIS cycle includes the following steps, listed in sequential order:

YA 0—fetches an object language instruction (that was not decoded because of a previous interrupt servicing requirement) from an auxiliary register in control memory and loads it into a main engine register.

YA 1—fetches object language instruction from main memory and loads it in a main engine register.

YA 2—fetches a C&TV from control memory, loads the address field into the mini engine program counter thereby specifying the initial MINIFLOW decoding routine instruction, and uses the control bits to control object instruction address modification and to specify whether the remaining steps of the WIS cycle is executed.

YA 3—if indirect addressing is specified in YA 2, the indexed address is used to fetch the effective address word from main memory and load it into a main engine register.

YA 4—fetches the memory operand from the main memory.

YA 5—depending on the settings of the C&TV control bits, this step bypasses MINIFLOW decoding or fetches the first MINIFLOW instruction.

YA 6—starting with the MINIFLOW instruction fetched in YA 5, this step initiates MINIFLOW instruction execution and provides for exiting to main memory or control memory as determined by the last instruction in the MINIFLOW subroutine.

Standard supplies a hard-wired translator table that contains an entry for each object language instruction to designate up to 64 different C&TVs and the setting of precondition bits appropriate for decoding that instruction. Each item in the table consists of two numbers; a two-digit octal number specifying the control memory address of the C&TV that points to the MINIFLOW subroutine needed to decode the object language instruction, and a three-digit number controlling the precondition bit settings.

A MINIFLOW instruction consists of an 18-bit word, composed of three major fields that provide 50 primary operation (POP) codes, over 150 secondary operation (SOP) codes, and 32 tertiary operation (TOP) codes. Depending upon the requirements of the target system, various combinations of POP,

SOP, and TOP codes can provide thousands of individually distinct MINIFLOW instructions to choose from when forming a target system instruction set.

POP—determines the format of the operation codes in the rest of the instruction; specifies registers as well as all shifting of register contents; tests various general-purpose and special-purpose indicators as well as indicators related to i/o channels.

SOP—specifies all algebraic arithmetic and logical operations between registers as well as all shifting of register contents; tests various general-purpose and special-purpose indicators as well as indicators related to i/o channels.

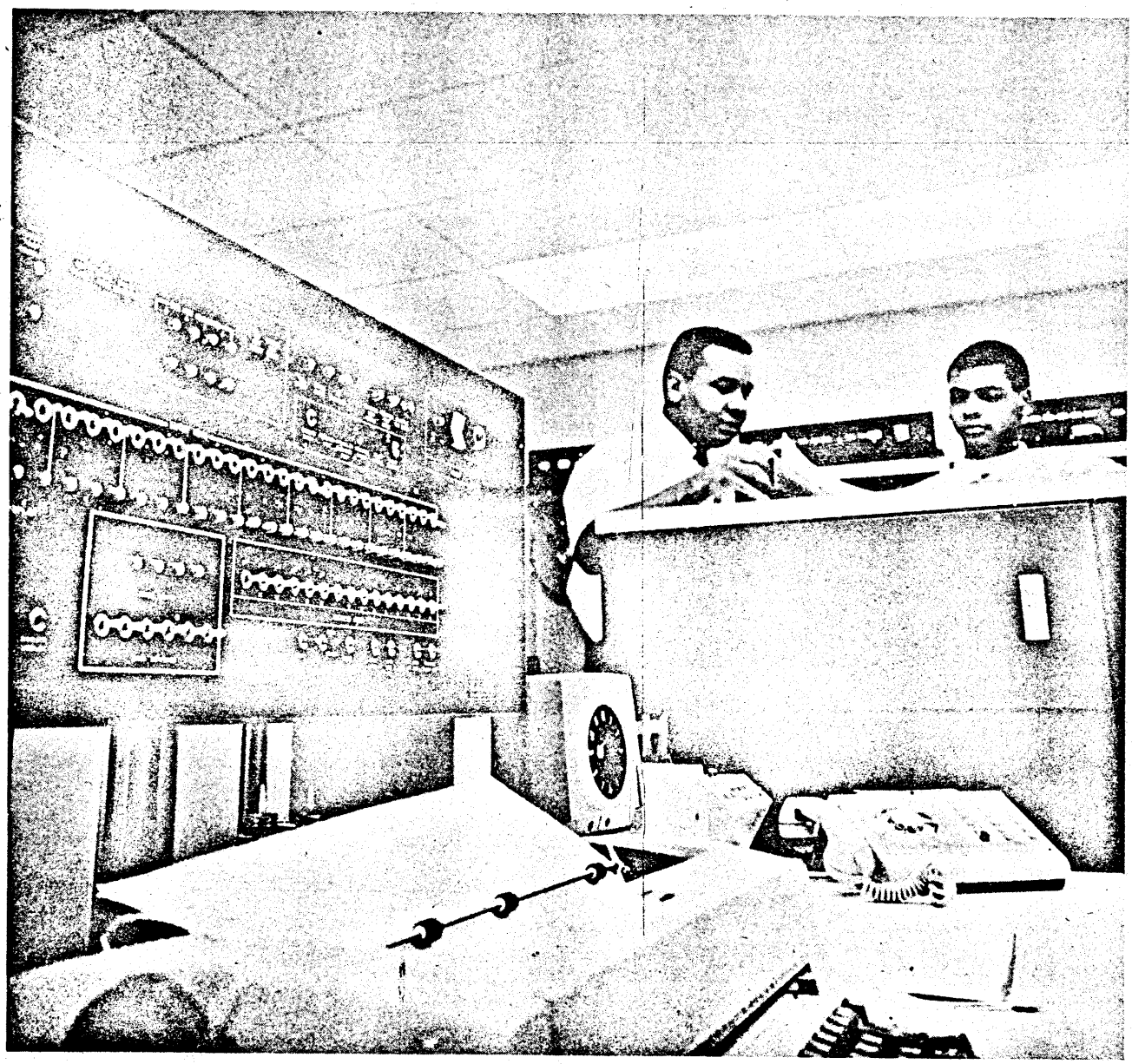
TOP—depending on POP, specifies the bit positions (zones) that are active in the adder and that receive data in the receiving register (the bit positions outside the specified zone in the receiving register are not changed); also depending on POP code, provides a memory address, a skip distance, a shift count, or special control.

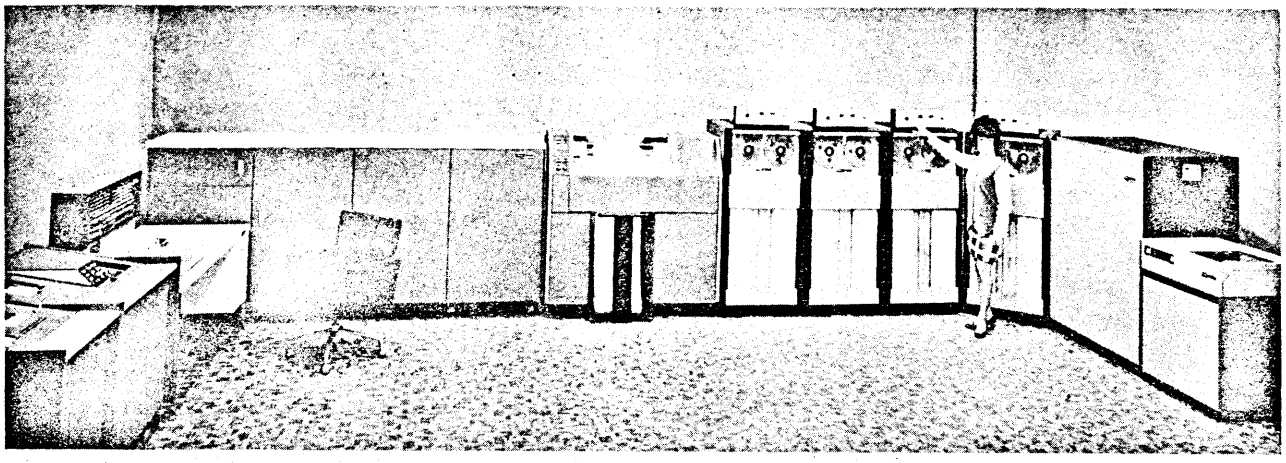
MINIFLOW emulation packages are currently available for supporting most configurations of three 6-bit, character-oriented systems.

In addition, Standard supplies a MINIFLOW that allows the IC-4000 to function as a stand-alone system (Target System ES-01) and one that uses the IC-4000 as an experimental computer (Target System EX-01).

Target System ES-01 is oriented toward support of the 4000 basic programing system, the basic operating software package provided by Standard for those users who wish to use the IC-4000 as a stand-

Top of the line configuration. This Standard IC-4000 system includes punched card i/o unit, keyboard i/o unit, cpu, high-speed line printer, four tape units, and disk storage system.





Operator's console. Roomy layout and accessibility provide ease of operation.

alone system. It is a 6-bit, character-oriented, single address, fixed word length, parallel binary system. Each word consists of 36 bits—35 data bits and one sign bit.

The system contains an adder/subtractor, a 38-bit accumulator register, a 36-bit multiplier-quotient register, i/o channel command registers that hold the i/o command being executed, a 15-bit program counter, and seven 15-bit index registers.

The basic instruction set includes single precision fixed-point and floating-point add, subtract, multiply, and divide instructions; variable-length multiply and divide instructions; as well as logical AND, inclusive OR, and exclusive OR. Separate instructions are provided for comparison of signed and unsigned numbers and character fields. These comparison instructions incorporate a three-way conditional branch that depends upon the outcome of the comparison.

The instruction repertoire also includes the facility for treating the contents of the index registers as operands in arithmetic operations. Instructions are provided for transferring data between the index registers and up to seven contiguous words of core. The transmit instructions transfers a contiguous block of data directly from one area of storage to another without passing through the accumulator. The instruction set provides two methods of indexing. The single tag mode indexes by any one of the seven index registers, and the multiple tag mode indexes by any combination of three specified index registers.

A memory reference instruction can directly address any location in main memory. One level of indirect addressing is provided. When ES-01 supports the 4000 basic programing system, an IC-4000 central processor must be configured with at least one console keyboard-printer for providing low-speed typewriter output. Keyboard input capability with the console keyboard-printer is provided by an optionally available keyboard control unit.

Monthly rental rates, based on a one-year lease, begin at $5810 for a central processor, keyboard, and punched card i/o capability. Rates extend up to $11,025 per month for the central processor, keyboard i/o, and the addition of a high-speed line printer, a 4-tape system, disk storage, and high-speed input.

Peripheral devices available to the IC-4000 computer system are listed.

Target System EX-01 is designed as an experimental object language that enables the user to redefine machine instructions during the course of program execution. Target System EX-01 is similar in many respects to Target System ES-01. It contains instructions that can manipulate 18-bit words, transferring information between main memory core and control memory core. These core-to-core transmission instructions use the contents of the two halves of the accumulator to address main memory and control memory for data transfer. By means of these instructions, Target System EX-01 can modify MINIFLOW during program execution, thus enabling the programer to redesign the computing system during operation.

Standard's Inner Computer design principle results in a flexible system capable of operating in a variety of situations. Besides purchasing a stand-alone system, the user is also acquiring a versatile emulator of other important systems. The Standard Computer can support the operational software provided by the emulated machine's manufacturer. As a consequence, minimal software modification is required when switching to a Standard computer.

The experimental Target System EX-01 should be of special interest to the academic community since its value as a computer research tool is limited only by the ingenuity of the researcher. In addition to designing new systems by MINIFLOW modification, the researcher can develop and test operational software for each system.

This article is based on material published in AUERBACH Scientific and Control Computer Reports, an analytical reference service published by AUERBACH Info, Inc. of Philadelphia.