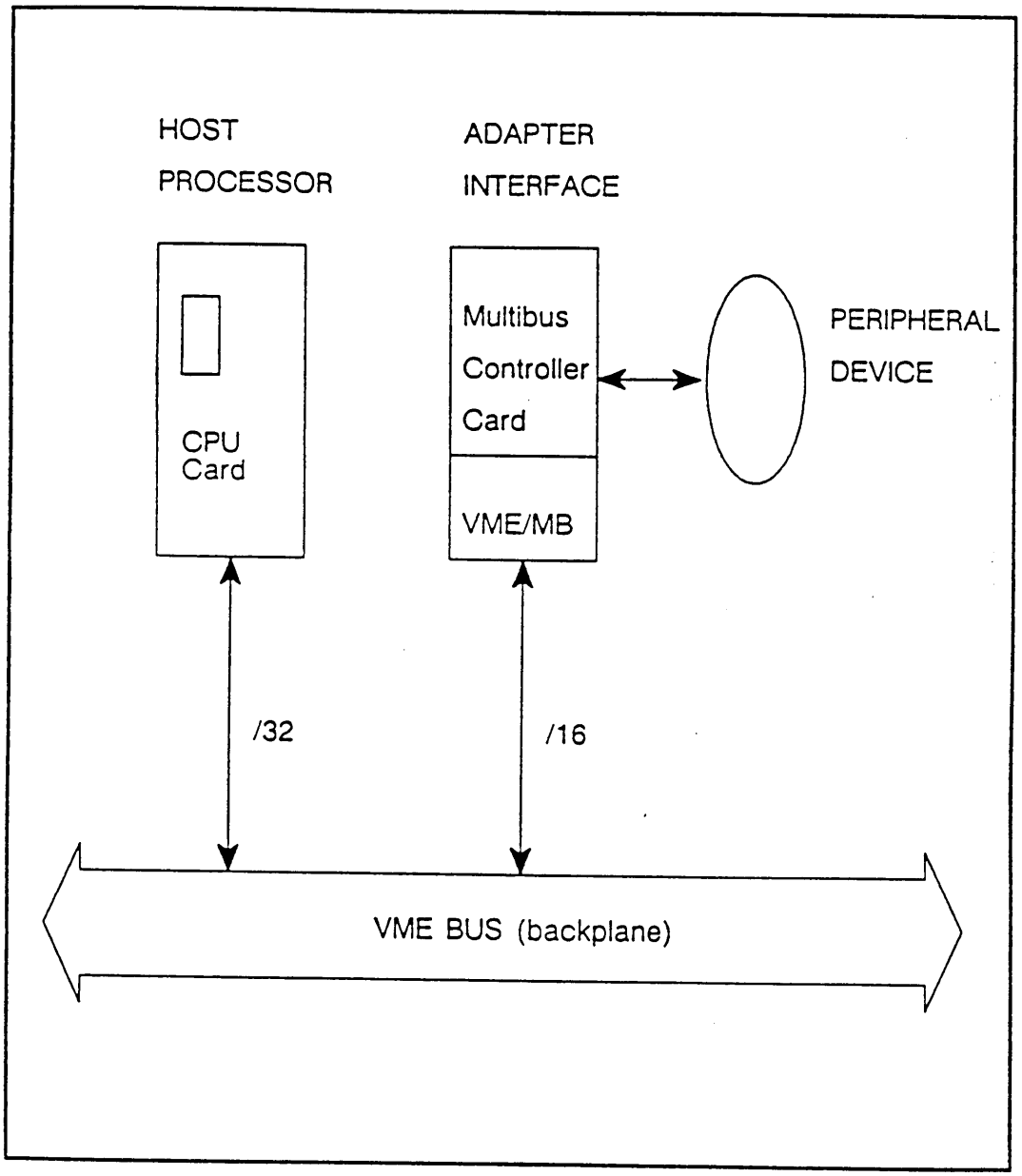
VME to Multibus Adapter Card

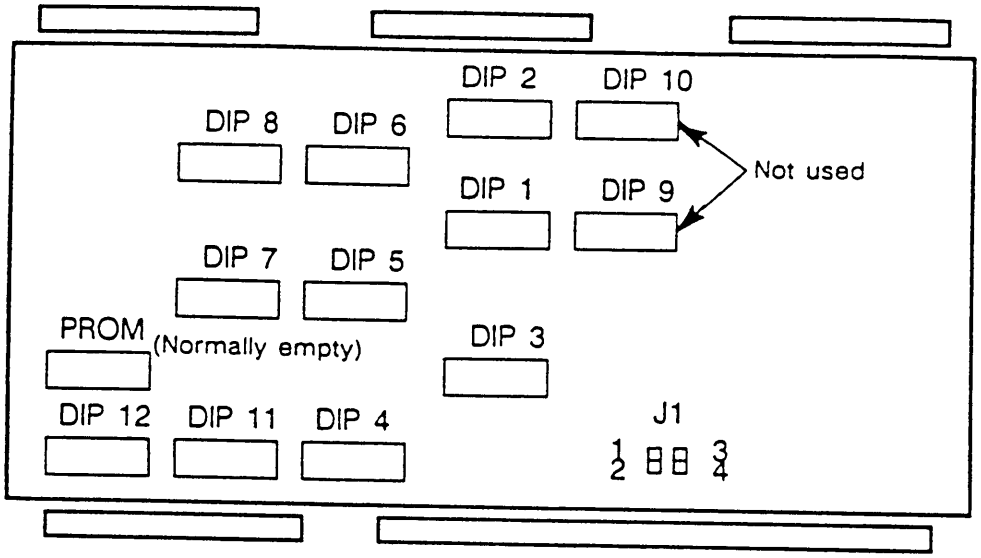


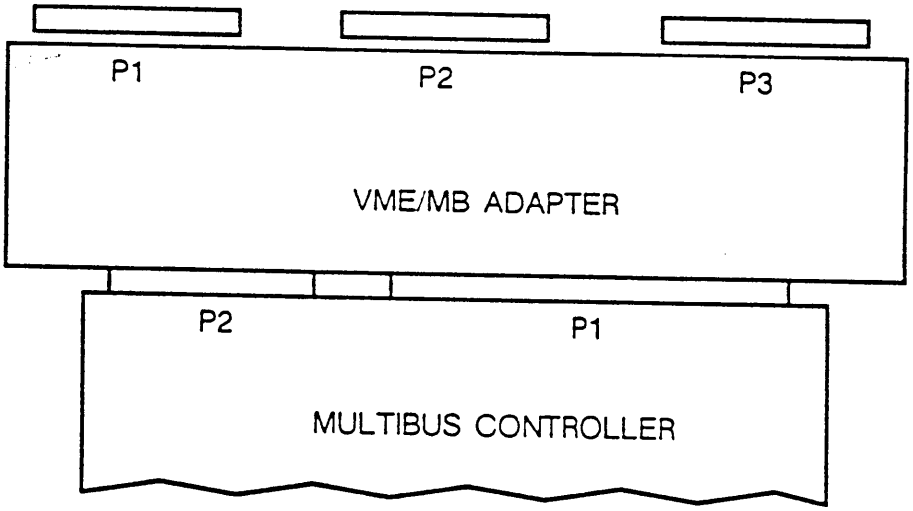
VME to Multibus Adapter Card

This card allows Multibus protocol 2-high cards to work with Sun VMEbus protocol 3-high systems.

The 2-high controller card (example: Xylogics 451 SMD disk) is plugged into the adapter and the entire assembly is plugged into the proper slot as if it were all one card.

VME to Multibus Adapter Layout





VME/MB MOUNTING

VME to Multibus Adapter Layout

- Each DIP has 8 switches 1-8.
- On is up, off is down.
- Do not use lead pencil to change switches.
- The prom socket, usually unstuffed, is for special order Sun Proms which would provide the customer with multiple interrupt vectors.

VME/MB Switch Settings for Xylogics 450/451 Controller Boards

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	OFF	ON	ON	ON	OFF	OFF	ADDR 0x40 I/O
2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/O space=8
3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ADDR 0xEE
4	ON	ON	ON	ON	ON	ON	ON	ON	I/O space=8
5	ON	ON	ON	ON	ON	ON	ON	ON	24–bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24–bit bolck size
7	ON	ON	ON	ON	ON	ON	ON	ON	24–bin addr space
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24–bit block size
11	OFF	OFF	OFF	OFF	ON	ON	ON	ON	Set addr A23–A20
12	ON	ON	ON	OFF	ON	ON	OFF	ON	Int Vec at 0x48
J1	Install pins 1–2 for BCLK					Install pins 3–4 for CCLK			

FIRST SMD (DISK) CONTROLLER

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	OFF	ON	ON	OFF	OFF	OFF	ADDR 0x48 I/0
2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/Ospace=8
3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ADDR 0xEE
4	ON	ON	ON	ON	ON	ON	ON	ON	VME addr space
5	ON	ON	ON	ON	ON	ON	ON	ON	24–bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24–bit block size
7	ON	ON	ON	ON	ON	ON	ON	ON	24–bit addr space
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24–bit block size
11	OFF	OFF	OFF	OFF	ON	ON	ON	ON	Sets addr A23–A20
12	OFF	ON	ON	OFF	ON	ON	OFF	ON	Int Vec 0x49
J1	Install pins 1–2 for BCLK					Install pins 3–4 for CCLK			

SECOND SMD (DISK) CONTROLLER

VME/MB Switch Settings for Xylogics 450/451 Controller Boards

Note: Switch 11, positions 5, 6, 7 and 8 are on for *all* cards except:

- Xylogics 472's.
- Gateway's.

VME/MB Settings For Gateway and Sunlink Controllers

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	ON	ON	ON	ON	ON	ON	ADDR 0x00
2	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No response to I/O space
3	ON	ON	ON	ON	ON	ON	ON	ON	ADDR 0x00
4	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No response to I/O space
5	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24–bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24–bit block size
7	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	24–bit addr space
8	ON	ON	ON	ON	OFF	OFF	OFF	OFF	24–bit block size
11	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Sets addr A23–A20
12	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	Int Vec 0x75
J1	Install pins 1–2 for BCLK					Install pins 3–4 for CCLK			

SECOND ETHERNET

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	ON	ON	ON	OFF	OFF	OFF	ADDR 0x800
2	ON	ON	ON	ON	ON	OFF	OFF	OFF	I/O space = 16
3	ON	ON	ON	ON	OFF	ON	ON	ON	ADDR 0x0800
4	ON	ON	ON	ON	ON	ON	ON	ON	VME addr space
5	ON	ON	ON	ON	ON	ON	ON	ON	24–bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24–bit block
7	ON	ON	ON	ON	ON	ON	ON	ON	24–bit addr space
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24–bit block
11	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Sets addr A23–A20
12	ON	ON	OFF	OFF	ON	ON	ON	OFF	Int Vec 0x8C
J1	Install pins 1–2 for BCLK					Install pins 3–4 for CCLK			

FIRST SUNLINK CONTROLLER

VME/MB Settings for Xylogics 472 Tape and Systech ALM 1 Controllers

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
Dip 1	ON	ON	OFF	OFF	ON	***	OFF	OFF	Addr 0x60 I/O
Dip 2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/O space = 8 bytes
Dip 3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	Addr 0xEE for I/O
DIP 4	ON	ON	ON	ON	ON	ON	ON	ON	I/O space = 8
Dip 5	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
Dip 6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
Dip 7	ON	ON	ON	ON	ON	ON	ON	ON	
Dip 8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
Dip 9	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
Dip 10	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
Dip 11	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Set A23 to A20
Dip 12	***	ON	OFF	ON	ON	OFF	OFF	ON	Int vector set to 0x64
JUMPERS	Install pins 1–2 for BCLK					Install pins 3–4 for CCLK			
*** set ON for xtc0 , set OFF for xtc1									

GCR (6250) 1/2–INCH TAPE CONTROLLER

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
Dip 1	OFF	ON	ON	OFF	ON	ON	OFF	OFF	Addr 0x20 for I/O
Dip 2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/O space = 8
Dip 3	ON	ON	ON	ON	ON	OFF	OFF	ON	Addr 0x06 for I/O
Dip 4	ON	ON	ON	ON	ON	ON	ON	ON	I/O space = 8
Dip 5	ON	ON	ON	ON	ON	ON	ON	ON	VME 24-bit addr space
Dip 6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
Dip 7	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
Dip 8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
Dip 9	---	---	---	---	---	---	---	---	Not Used
Dip 10	---	---	---	---	---	---	---	---	Not Used
Dip 11	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Sets addr A23–A20
Dip 12	ON	ON	ON	OFF	ON	ON	ON	OFF	Int Vec at 0x88
JUMPERS	Install pins 1–2 for BCLK					Install pins 3–4 for CCLK			

SYSTECH ALM 1 (MTI) INTERFACE CONTROLLER

CHAPTER SEVEN SECTION 7C:

VME-MULTIBUS ADAPTER

OVERVIEW

The VME to Multibus board is an adapter which allows the use of Multibus cards on the VME bus for Sun 3 pedestal products. The VME to Multibus card scheme is transparent to the system in that there are no registers on the adapter board that software can modify. The following text defines how VME signals are routed through the adapter so that Multibus cards can be read and written, as well as interrupted using programmed cycles. Functional block diagrams have been included to illustrate how the adapter operates. The following block illustrates the VME interface to the adapter:

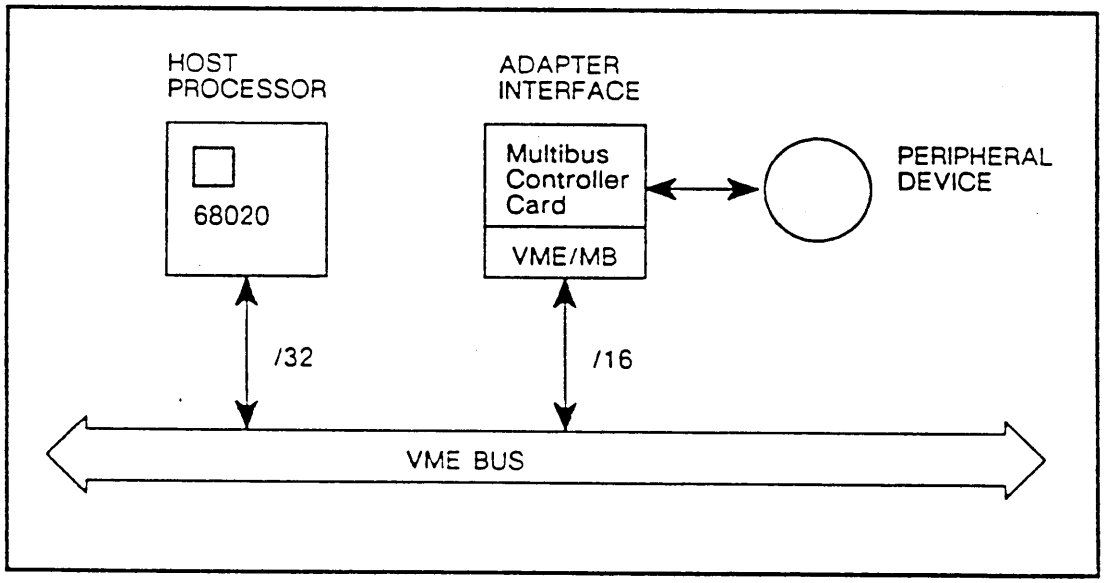


FIGURE 7C-1: VME INTERFACE

7C.1 ADAPTER CONFIGURATION CONSIDERATIONS

There are a number of switch settings which must first be described in order to better understand the functional capabilities of the VME to Multibus board. The adapter board can respond to a block of addresses in the 24-bit VME address space. When the adapter board sees an address within the selected block, it throughputs the address bits to the Multibus board and generates a Multibus

read or write command. The addressing can range from 256K to 16M bytes for Multibus memory address decoding.

This addressing function is controlled by the dip switches (DIP's 5,6,7,8,) which set up in three 8-bit equal-to-comparators. If the comparators match the addresses a select signal is asserted toward a control PAL on the adapter board. At this point, the PAL would assert a 'memory enable' strobe to the 'transfer enable' PAL on the adapter board which selects the bidirectional transceivers for a data transfer. A 'dataout' signal from the same PAL controls the direction of the transfer at the transceivers. Dips 5 and 7 (see Figure 7C-2) select the 24-bit VME space base address for access to the Multibus memory space.

The adapter board can also respond to a block of addresses in the 16-bit VME address space that the board responds to.. Here, when the adapter board sees an address within the selected block, it throughputs the address bits to the multibus board and generates a Multibus read or write. This function is controlled by dip switches on the adapter board (DIP's 8 and 6).

For Multibus I/O addressing, the adapter board can respond to a block of addresses in the 16-bit VME address space. When the adapter sees an address within the block set up by the switches, it passes the address bits to the Multibus board and asserts a Multibus I/O read or write. The address range of these blocks is from 2 Bytes to 64K bytes. This function is set-up in dip switches 1 through four.

The 16-bit address will be set-up in two 8-bit equal-to-comparators, and assert select signals toward the control PAL. This PAL then asserts I/O enable to the transfer PAL. Figure 7C-2 illustrates the configuration selects for the adapter board.

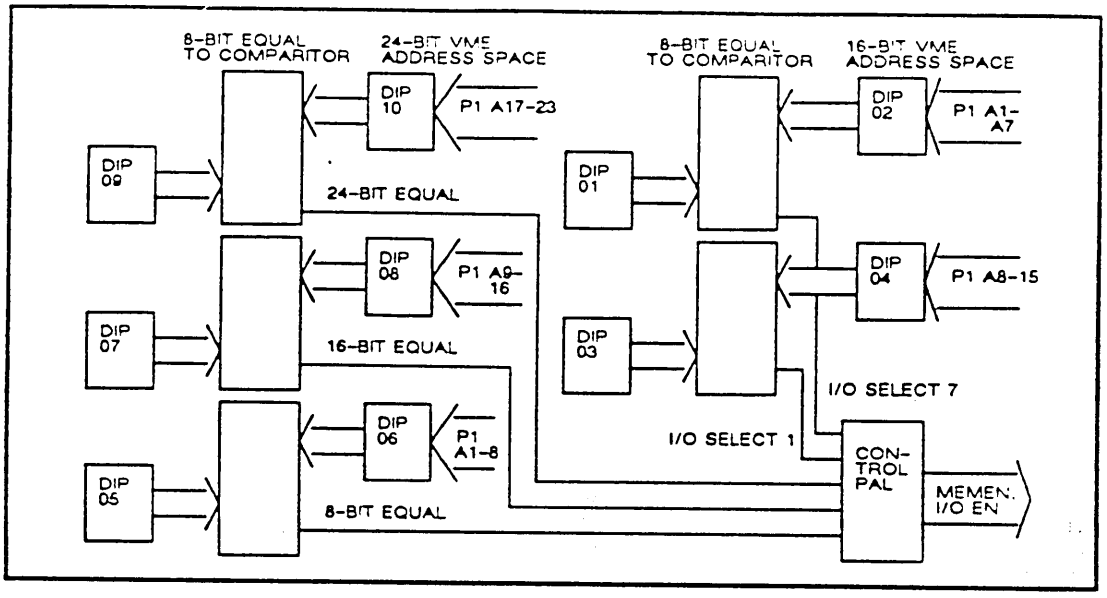


FIGURE 7C-2: CONFIGURATION SELECTS

7C-2 VME BUS TO MULTIBUS ADDRESSING

During a VME read cycle to a Multibus card, P1 address lines A01-A23 are transferred to to the multibus adapter card in conjunction with P1 address strobe (AS) and P1 data strobes (DS0,DS1). Address lines which pass on to Multibus cards are latched onto the adapter by transparent latches with address strobe. After setting up, the inverted address lines are passed onto the Multibus with the assertion of Multibus 'read'.

Note that VME address lines are active high, and Multibus address lines are active low. Address lines are inverted by the latches on the adapter card.

A transfer PAL is used to set up the Multibus read command using address and data strobes. While active, the read signal allows the addresses to pass to the Multibus at connector J700. At the end of the read cycle, the Multibus board will respond by asserting a 'transfer acknowledge' to the adapter, which asserts P1 'data transfer acknowledge', thus, completing the cycle. The following block diagram illustrates this function:

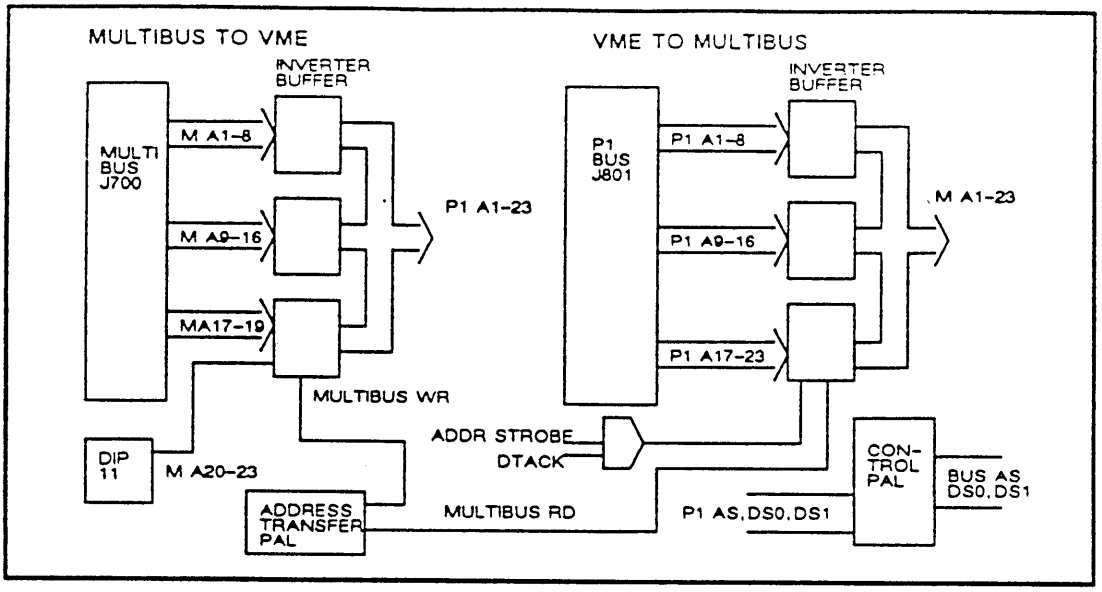


FIGURE 7C-3: VME/MULTIBUS ADDRESSING

7C.3 MULTIBUS TO VME BUS ADDRESSING

In the process of a read cycle from the Multibus to the VME bus, multibus address lines M.A01-A19 are enabled onto the adapter via buffers, which invert the lines and enable (pass) them on to the VME (P1) bus, via connector J801. A dip switch at DIP 11, furnishes the high order address bits (M. A20-A23) to the inverting buffer to complete the 24 bit address to the VME bus.

At the end of the cycle, a P1 'data transfer acknowledge' is sent from the VME bus to the adapter board via a buffer which asserts 'bus data transfer acknowledge' to the transfer acknowledge PAL. Refer to the block diagram above for an illustration of this function.

7C.4 DATA TRANSFERS TO AND FROM THE ADAPTER

During a transfer cycle, data is transferred from the Multibus to the VME bus (and vice versa) via bidirectional transceivers. Two of the transceivers are used when the data transferred is a 16-bit word. For byte transfers the transceivers are used when the data is a byte at an odd address, or when data is a byte at an even address. In a write cycle to the Multibus, 'multibus write' will be active. When the direction is toward the VME bus, 'multibus read' will be active on the adapter. Both signals are asserted via the transfer PAL.

The three transceivers are enabled by 'write enable' signals which are driven by a data transfer enable PAL. The PAL is set-up by 'data strobes' (DS0,DS1)

and bus write conditions originating from the VME (P1) bus during a write cycle to the multibus. For data transfers to the VME bus (from the Multibus), a 'dataout' signal is asserted to the transceivers for direction control toward the P1 data bus. Dataout is also set-up by the data transfer enable PAL. Refer to the following block diagram for an illustration of this function:

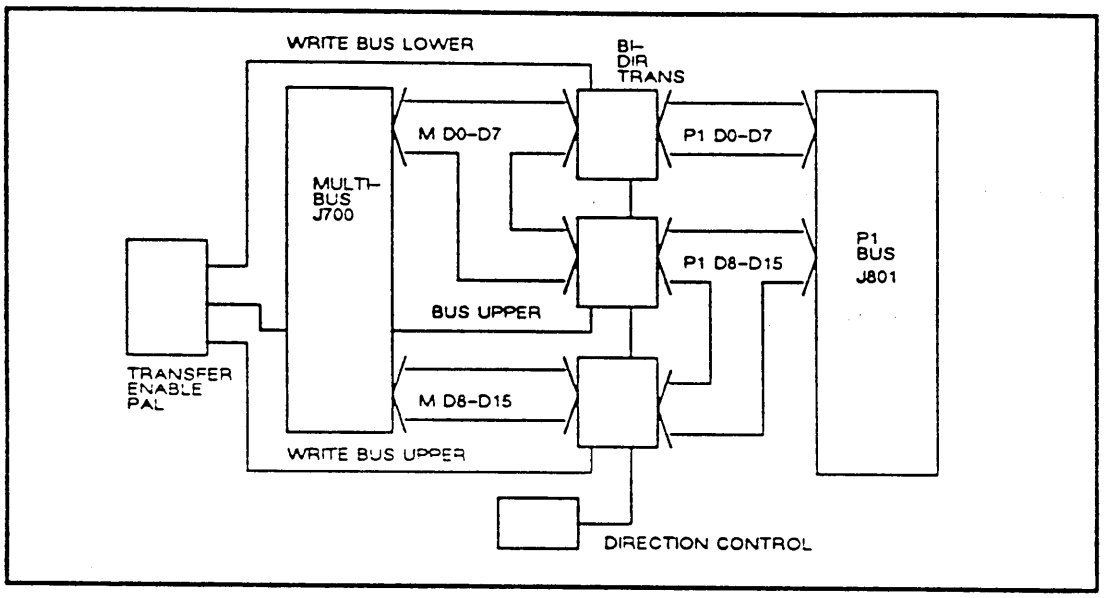


FIGURE 7C-4: VME/MULTIBUS DATA TRANSFERS

7C.5 BUS REQUEST/BUS GRANT LOGIC

For bus requests from the Multibus to the VME bus, the requesting board will assert a 'bus request' and 'bus-priority-in level' to a handshanking PAL on the adapter board. This PAL then asserts a P1 bus request level to the VME (P1) bus. If the bus is not busy, a P1 'bus grant' level will be sent to the handshaking PAL which then asserts the bus grant as a 'multibus- priority-out' to the requesting Multibus board.

7C.6 INTERRUPT LOGIC

Vectored interrupts are not supported on the Multibus, however, they are supported on the VME bus and therefore must be translated by the adapter board. A VME interrupt vector is generated on the adapter board by switches (DIP 12), or by an interrupt PROM(supplied by Sun).

The switches are used if the Multibus board interrupts on one level only. Where a Multibus board interrupts on more than one level, and a separate vector is required for each level, the PROM is used.

When one of the Multibus interrupt lines (INT1-INT7) goes active, it through puts to the VME bus via an open collector buffer (U405). When the processor sees the interrupt, it goes into an interrupt acknowledge cycle by putting the interrupt level on the lower-order address bits (P1 A1-A3), while driving P1 'interrupt acknowledge' and asserting P1 'address strobe'. Note that P1 interrupt acknowledge is bussed to every board on the backplane. A version of P1 'interrupt acknowledge-in/interrupt acknowledge-out' is daisy-chained from board to board.

When the adapter board sees this version of interrupt, it will check to see if the interrupt level specified by the address lines (P1 A1-A3) is in the same level as the one its trying to interrupt on. If so, the adapter will enable the interrupt vector onto the VME bus via the buffer. If the interrupt level is not the one specified by the address lines, the adapter will pass the interrupt on to the next board with P1 'interrupt acknowledge-out'. The following block diagram illustrates this function:

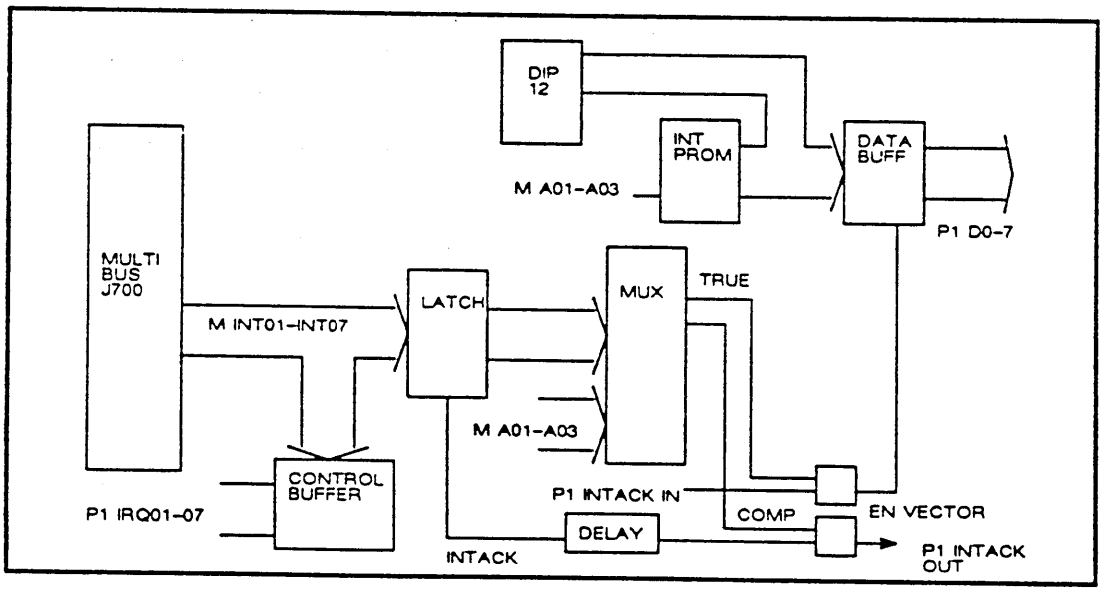


FIGURE 7C-5: INTERRUPT LOGIC

7C.7 VME DMA CYCLE

The adapter board can generate a VME DMA cycle (when the adapter is the VME bus master) in response to a DMA cycle by the Multibus board. The

Multibus board can be a 20-bit address master, or a 24-bit address master (the adapter board is a 24-bit master). If the Multibus board becomes a 24-bit master, the 4-high order bits are generated by the switches on the adapter board which are in DIP 11. DIP 11 generates addresses A20-A23 toward the VME bus via the inverter address buffers.

7C.8 CLOCK LOGIC

For multibus boards which require an external bus clock and constant clock (that is most boards), the adapter provides for those clocks. The clocks originate at a 19.6608 MHz crystal (X1) and is divided down by a flip-flop to provide a 9.8344 MHz clock. A jumper block on the adapter board (J1) allows the enabling/disabling of the bus clock and the constant clock. Pins 1 to 2 should be jumpered for the bus clock, and pins 3 to 4 should be jumpered for the constant clock. Note that the jumpers should be installed to provide the clocks. Refer to the block diagram in Figure 7C-6 for an illustration of these settings.

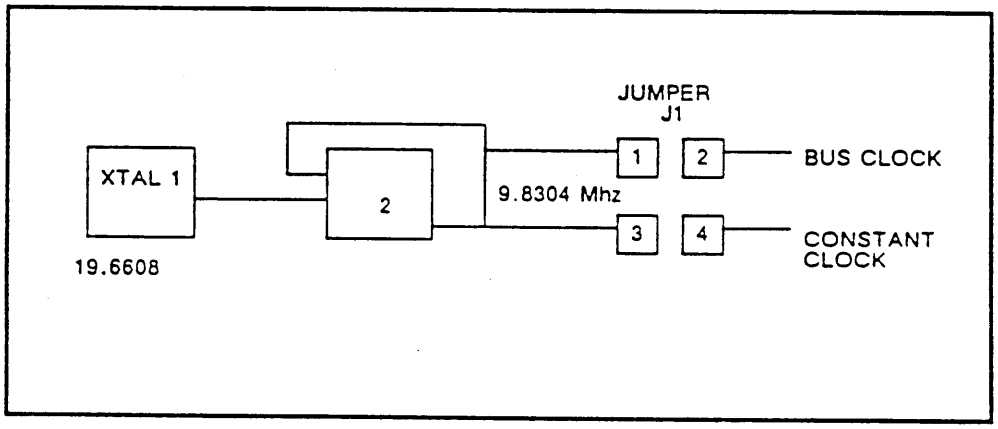


FIGURE 7C-6: CLOCK LOGIC

The next two blocks illustrate the layout of the VME/MB adapter:

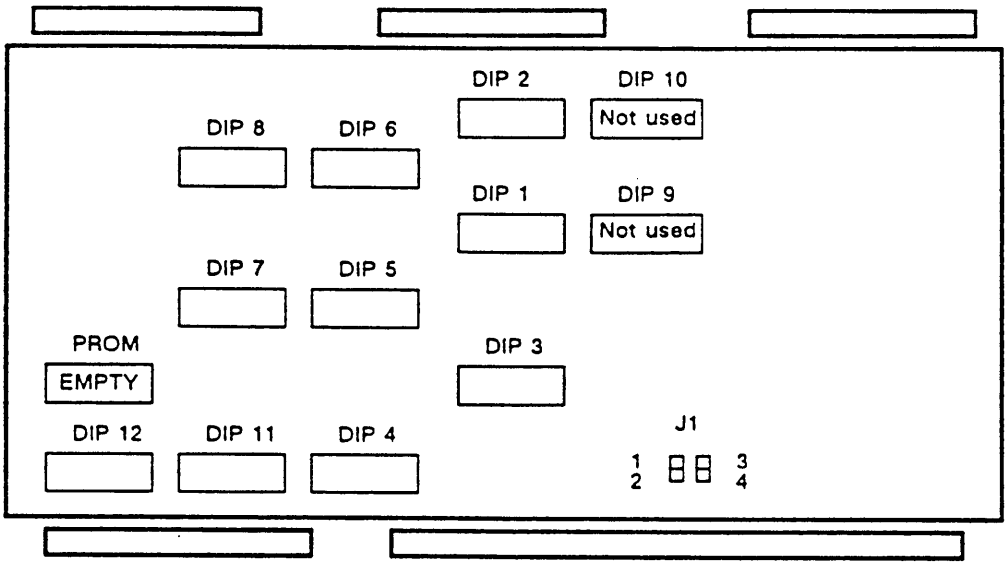


FIGURE 7C-15: VME/MB CARD LAYOUT

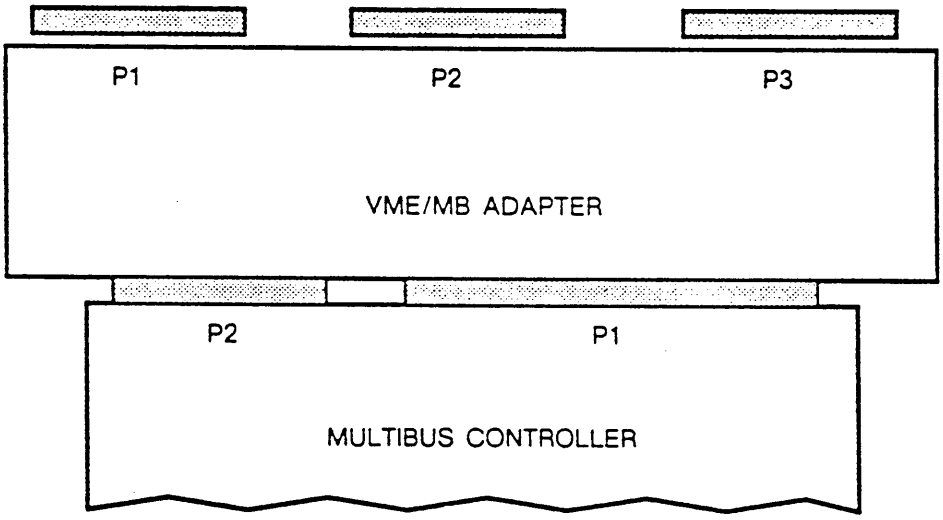


FIGURE 7C-16: VME/MB MOUNTING

7C.9 SUN 3 VME/MB ADAPTER SETTINGS

The following Tables list the default settings for Sun supported controller boards:

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	OFF	ON	ON	ON	OFF	OFF	ADDR 0x40 I/O
2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/O space=8
3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ADDR 0xEE
4	ON	ON	ON	ON	ON	ON	ON	ON	I/O space=8
5	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit bolck size
7	ON	ON	ON	ON	ON	ON	ON	ON	24-bin addr space
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
11	OFF	OFF	OFF	OFF	ON	ON	ON	ON	Set addr A23-A20
12	ON	ON	ON	OFF	ON	ON	OFF	ON	Int Vec at 0x48
J1	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			

FIGURE 7C-7: FIRST SMD CONTROLLER

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	OFF	ON	ON	OFF	OFF	OFF	ADDR 0x48 I/0
2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/Ospace=8
3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ADDR 0xEE
4	ON	ON	ON	ON	ON	ON	ON	ON	VME addr space
5	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
7	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
11	OFF	OFF	OFF	OFF	ON	ON	ON	ON	Sets addr A23-A20
12	OFF	ON	ON	OFF	ON	ON	OFF	ON	Int Vec 0x49
J1	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			

FIGURE 7C-8: SECOND SMD CONTROLLER

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	ON	ON	ON	ON	ON	ON	ADDR 0x00
2	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No response to I/O spac
3	ON	ON	ON	ON	ON	ON	ON	ON	ADDR 0x00
4	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No response to I/O spac
5	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
7	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	24-bit addr space
8	ON	ON	ON	ON	OFF	OFF	OFF	OFF	24-bit block size
11	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Sets addr A23-A20
12	OFF	on	off	on	OFF	off	off	ON	Int Vec 0x75
J1	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			

FIGURE 7C-9: SECOND ETHERNET BOARD

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	ON	ON	ON	OFF	OFF	OFF	ADDR 0x800
2	ON	ON	ON	ON	ON	OFF	OFF	OFF	I/O space = 16
3	ON	ON	ON	ON	OFF	ON	ON	ON	ADDR 0x0800
4	ON	ON	ON	ON	ON	ON	ON	ON	VME addr space
5	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block
7	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block
11	OFF	OFF	OFF	OFF	ON	ON	ON	ON	Sets addr A23-A20
12	ON	ON	OFF	OFF	ON	ON	ON	OFF	Int Vec 0x8C
J1	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			

FIGURE 7C-10: SUNLINK CONTROLLER

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
Dip 1	ON	ON	OFF	OFF	ON	***	OFF	OFF	Addr 0x60 I/O
Dip 2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/O space = 8 bytes
Dip 3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	Addr 0xEE for I/O
DIP 4	ON	ON	ON	ON	ON	ON	ON	ON	I/O space = 8
Dip 5	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
Dip 6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
Dip 7	ON	ON	ON	ON	ON	ON	ON	ON	
Dip 8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
Dip 9	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Not used
Dip 10	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Not used
Dip 11	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Set A23 to A20
Dip 12	***	ON	OFF	ON	ON	OFF	OFF	ON	Int vector set to 0x64
JUMPERS	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			
*** set ON for xtc0 , set OFF for xtc1									

FIGURE 7C-11: GCR 1/2-INCH TAPE CONTROLLER

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
Dip 1	OFF	ON	ON	OFF	ON	ON	OFF	OFF	Addr 0x20 for I/O
Dip 2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/O space = 8
Dip 3	ON	ON	ON	ON	ON	OFF	OFF	ON	Addr 0x06 for I/O
Dip 4	ON	ON	ON	ON	ON	ON	ON	ON	I/O space = 8
Dip 5	ON	ON	ON	ON	ON	ON	ON	ON	VME 24-bit addr space
Dip 6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
Dip 7	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
Dip 8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
Dip 9	---	---	---	---	---	---	---	---	Not Used
Dip 10	---	---	---	---	---	---	---	---	Not Used
Dip 11	OFF	OFF	OFF	OFF	ON	ON	ON	ON	Sets addr A23-A20
Dip 12	ON	ON	ON	OFF	ON	ON	ON	OFF	Int Vec at 0x88
JUMPERS	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			

FIGURE 7C-12: ALM INTERFACE CONTROLLER

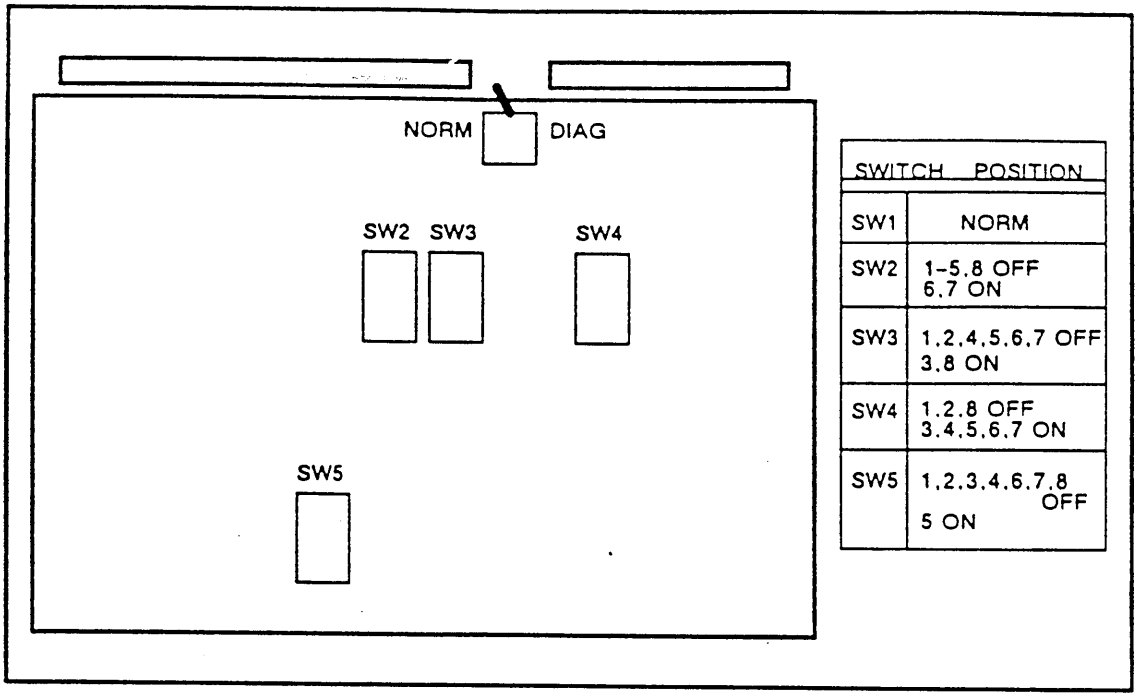


FIGURE 7C-13: ALM BOARD DIP SWITCH SETTINGS

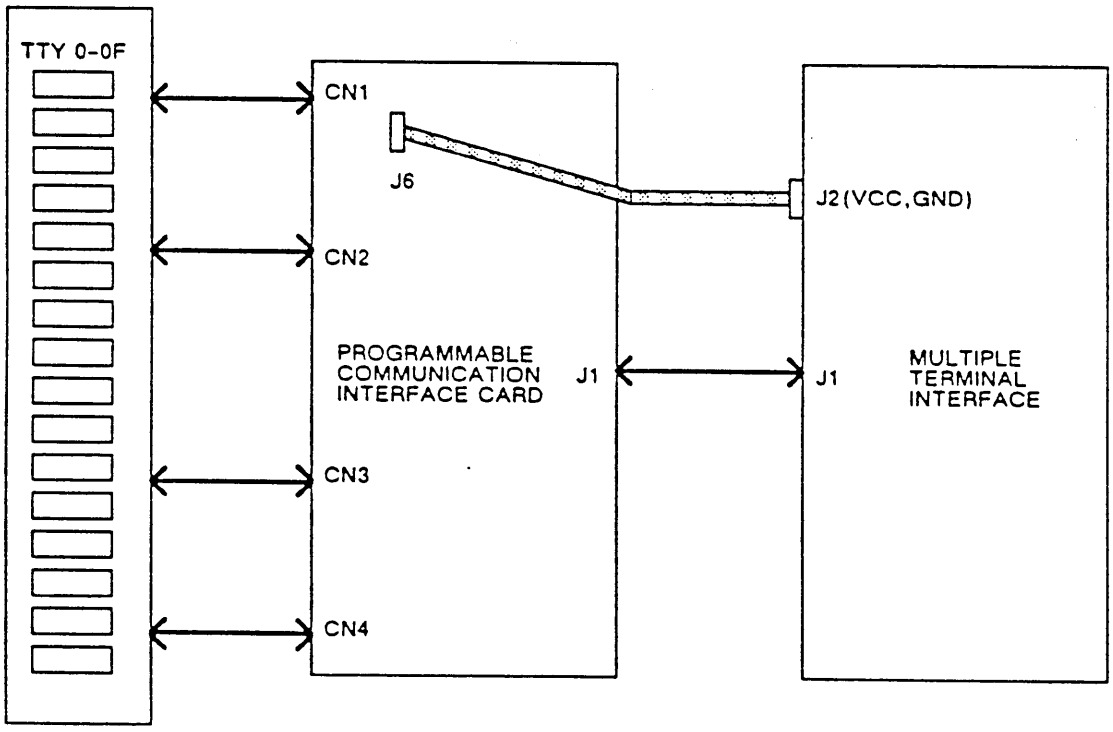


FIGURE 7C-14: PROGRAMMABLE COMMUNICATION INTERFACE (SECOND ALM BOARD)

ECO 2189

DATE APPROVED: 6/19/86

EFFECTIVE DATE: 6/19/86

PART NO. AFFECTED: 501-1054

ECO BOARD REV: FROM 01/C TO 02/A

AVERAGE REWORK TIME: 15 min.

PARTS NEEDED:	DESCRIPTION	SUN PART NO.	QTY.
	Spring finger	340-1228-03	1
	FR4 10 mil	330-1099-01	1
	Foam tape	150-1192-01	2
	Rivets 1/8 in.	240-1320-01	1

ADDITIONAL MATERIALS / TOOLS: Electric Hand Drill with a 1/8 inch bit
3/16 inch socket or nutdriver
Bostik POPRIVETOOL 1/8"-5/32"-3/16"
pop rivet tool or equivalent
Small screwdriver

REWORK INSTRUCTION FOR 2189:

1. Remove one of the pop rivets from the board stiffener with the electric hand drill.

2. Remove the screws and nuts that hold the connectors to the board stiffener with the screwdriver and 3/16" socket or nut driver.

3. Pull the board stiffener away from the printed circuit board and install the spring finger.

4. Place the insulator at the edge of the printed circuit board, near the board stiffener.

5. Place the board stiffener with the spring finger onto the printed circuit board and install the nuts and screws onto the connectors.
   * The springfinger should be resting on the FR4 insulator and not touching the printed circuit board.

6. Mark the revision level of the board with a -02/A.

COMMENTS: ECO 2748 requires the use of the FR4 10 mil insulator that has been installed with this rework instruction.

ECO 2748

DATE APPROVED: 11/06/86

EFFECTIVE DATE: 11/06/86

PART NO. AFFECTED: 501-1054

ECO BOARD REV: FROM 04/E to 05/A

AVERAGE REWORK TIME: 15 Min.

PARTS NEEDED:	DESCRIPTION	SUN PART NO.	QTY.
	FR4 10 mil	330-1099-01	1
	Foam tape	150-1192-01	2

ADDITIONAL MATERIALS / TOOLS: None

REWORK INSTRUCTION FOR ECO 2748:

1. Remove any insulator under the springfinger except the FR4 10 mil insulator.

2. Install a FR4 10 mil insulator under the springfinger held in place by the 2 pieces of foam tape at each end of the insulator.

3. Mark the revision level of the board to a -05/A.

COMMENTS: None

ECO 1609

DATE APPROVED: 05/17/85

EFFECTIVE DATE: 05/17/85

PART NO. AFFECTED: 501-1054

ECO BOARD REV: FROM 03/50 TO 03/51

AVERAGE REWORK TIME: 15 min.

PARTS NEEDED:	DESCRIPTION	SUN PART NO.	QTY.
	8 Pin Dip Switch	150-1006-01	1

ADDITIONAL MATERIALS / TOOLS: 30 guage Kynar wire

REWORK INSTRUCTION FOR 1609:

1) Dip switched Dip1 and Dip2 cut off pins 1 and 16 flush with the Dip switch body.

2) Install the two Dip switched in to the positions marked on the printed circuit board maked Dip1 and Dip2 so that pin 2 of the switch goes into pin 1 on the board.

3) On the solder side of the board, jumper Dip11 pins 1,2,3, and 4 to pin 8 of Dip12.

4) Change the Printed Circuit Board revision level to a -03/51.

Comments: None

ECO 1850

DATE APPROVED: 09/09/85

EFFECTIVE DATE: 09/09/85

PART NO. AFFECTED: 501-1054

ECO BOARD REV: FROM 03/52 TO 04/50

AVERAGE REWORK TIME: 15 min.

PARTS NEEDED: None

ADDITIONAL MATERIALS / TOOLS: None

REWORK INSTRUCTIONS FOR ECO 1850:

1) Remove the P2 VME connector from the VME to Multibus adapter.

2) Change the Printed Circuit Board revision level to a -04/50.

Comments: None

SUMMARY SHEET

VME MULTIBUSS ADAPTER

501-1054 Rev. - 01/29/88

UPDATED PER ECO 3282 / DOCUMENTATION

NOTE: * REQUIRES DEPOT REWORK

ECO #	REV. OUT	EFFECTIVE DATE	CORRECTIVE ACTION
1463	03/50	03/20/85	DOCUMENTATION
1607	03/51	05/17/85	ENGINEERING RELEASE / DOCUMENTATION
*1609	03/51	05/17/85	ON FAB 270-1054-03 REWORK DIP SWITHES 1,2 &11. CUT PINS 1&2 FLUSH TO SWITCH BODY AND MOUNT PIN 2 OF SWITCH TO PIN 1 OF BOARD LOC. ON SOLDER SIDE JUMPER DIP12 PIN 8 TO DIP11 PINS 1,2,3,& 4.

Problem: Board layout was incorrect and dipswitch had two pins not grounded.

1746	03/52	08/20/85	DOCUMENTATION
*1850	04/50	09/09/85	REMOVE P2 CONNECTOR
1725	04/A	09/30/85	PRODUCTION RELEASE
1993	04/B	11/05/85	ADDS BAR CODE LABELS
2080	04/C	12/10/85	DOCUMENTATION
2309	04/D	03/18/86	CHANGE IN BOM
2525	04/E	06/26/86	USE KEPTON TAPE (P/N 150-1180-01) ON BOARD SUPPORTS WHERE OPTION BOARDS REST.
*2189	N/A	06/19/86	SPRING FINGERS

Problem: Add spring fingers to pass FCC Part 15.

*2748	05/A	11/06/86	ADD THICKER INSULATION (FR4) P/N 330-1099-01. ADD DOUBLE SIDED TAPE (P/N 150-1192-01)

Problem: Make the spring finger insulator thicker to prevent the spring finger from shorting to the printed circuit board.

3018	05/B	03/10/87	DOCUMENTATION
3080	05/C	08/03/87	Add Bar Code tabs to BOM.

501-1054

3267	05/D	06/30/87	U locations on the printed circuit board need to be standardized.
3014	05/E	10/12/87	Documentation
3282	05/F	10/08/87	Documentation

Purge Notice

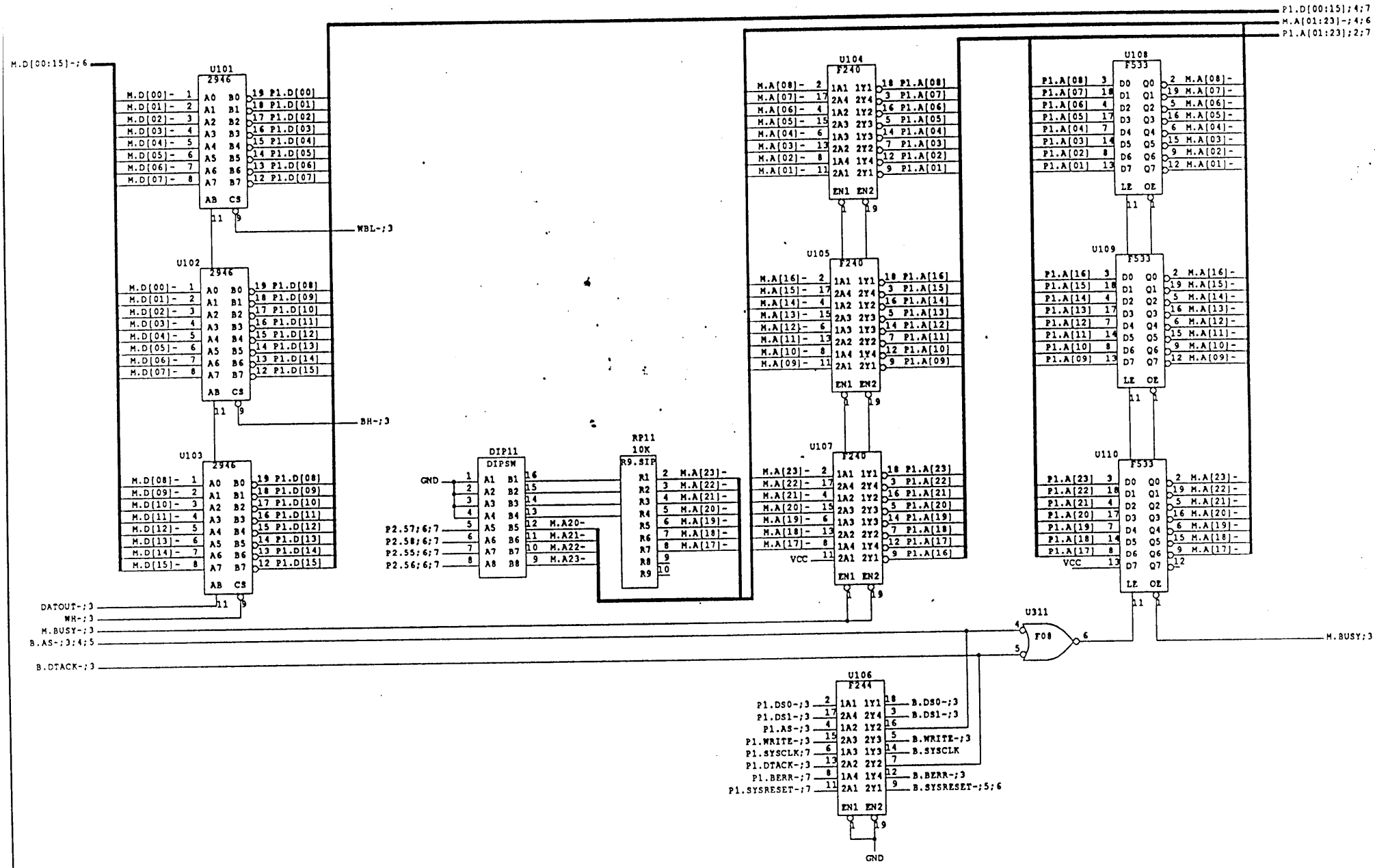
P.N. # 649	06/02/87	PURGE DALE 10K SIP WITH DATE CODE 8649 (P/N 120-1419-01).

VME TO MULTIBUS ADPT.

501-1054-05

Rev B

ECO	Description	Date	Approvals
XXXX		6/19/87	



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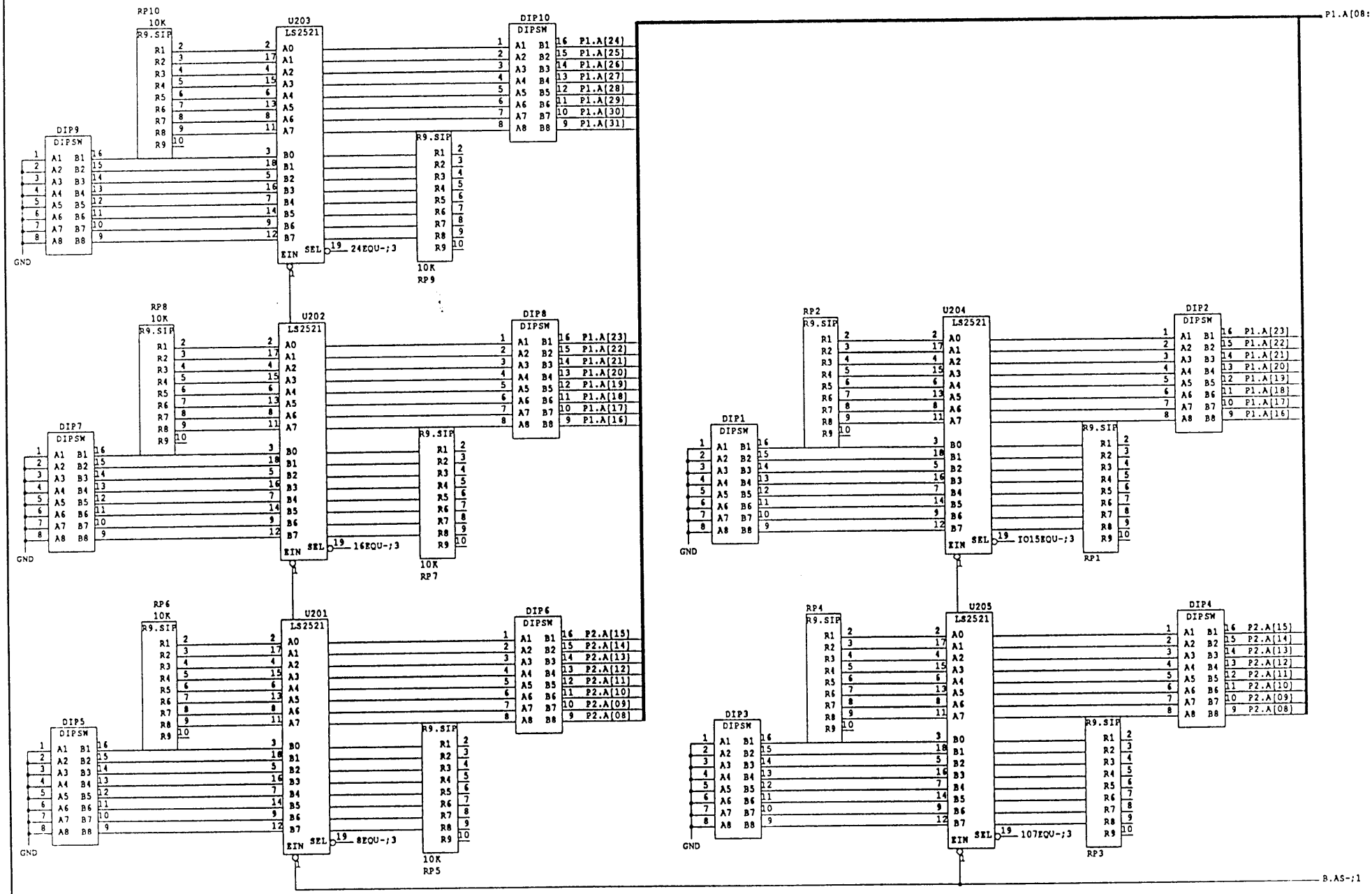
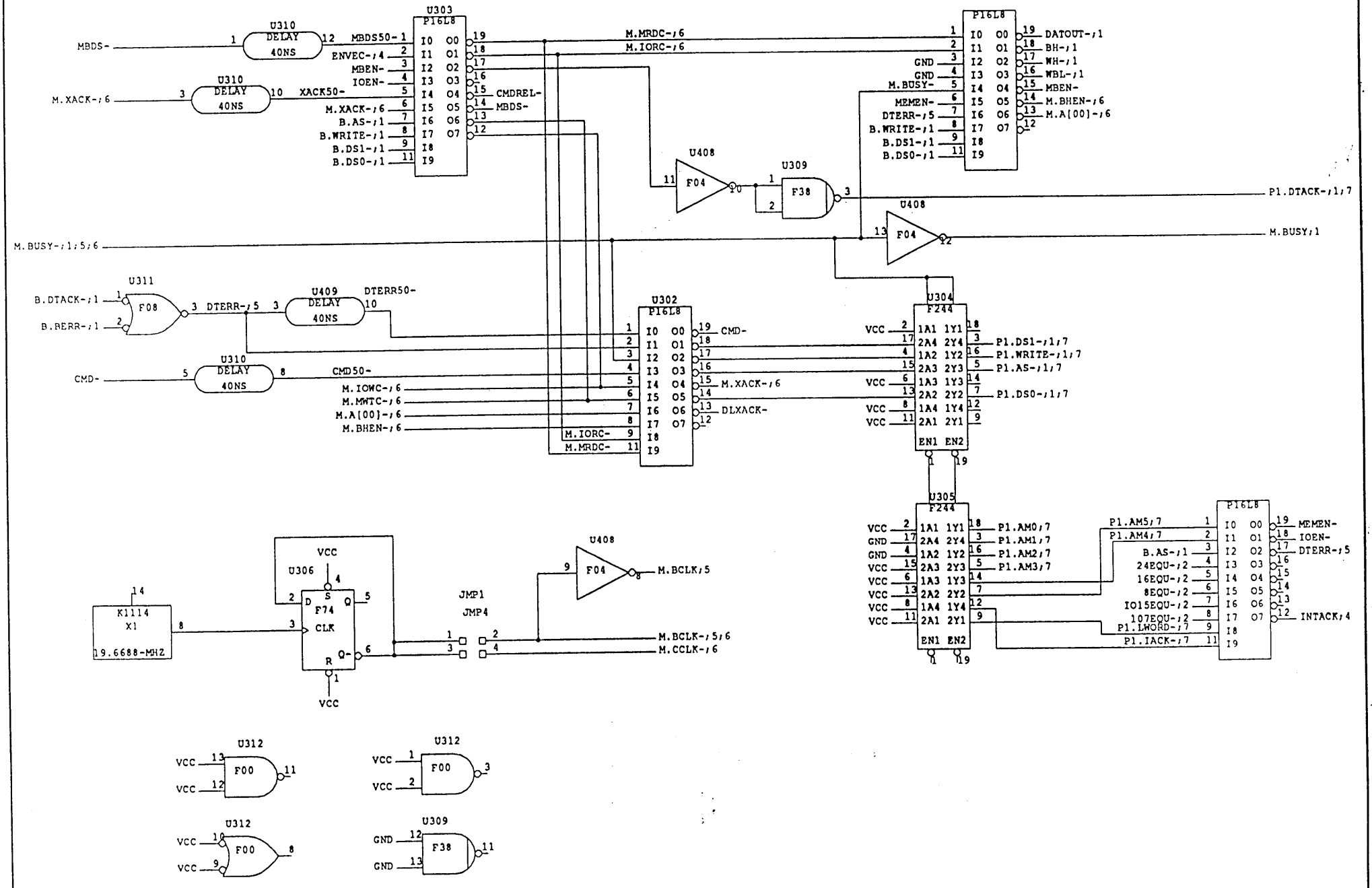
Sheet: 1		File: sh1.d	
Engineer:		Date: Thu Oct 13 11:26:33 1988	

ECO	Description	Date	Approvals



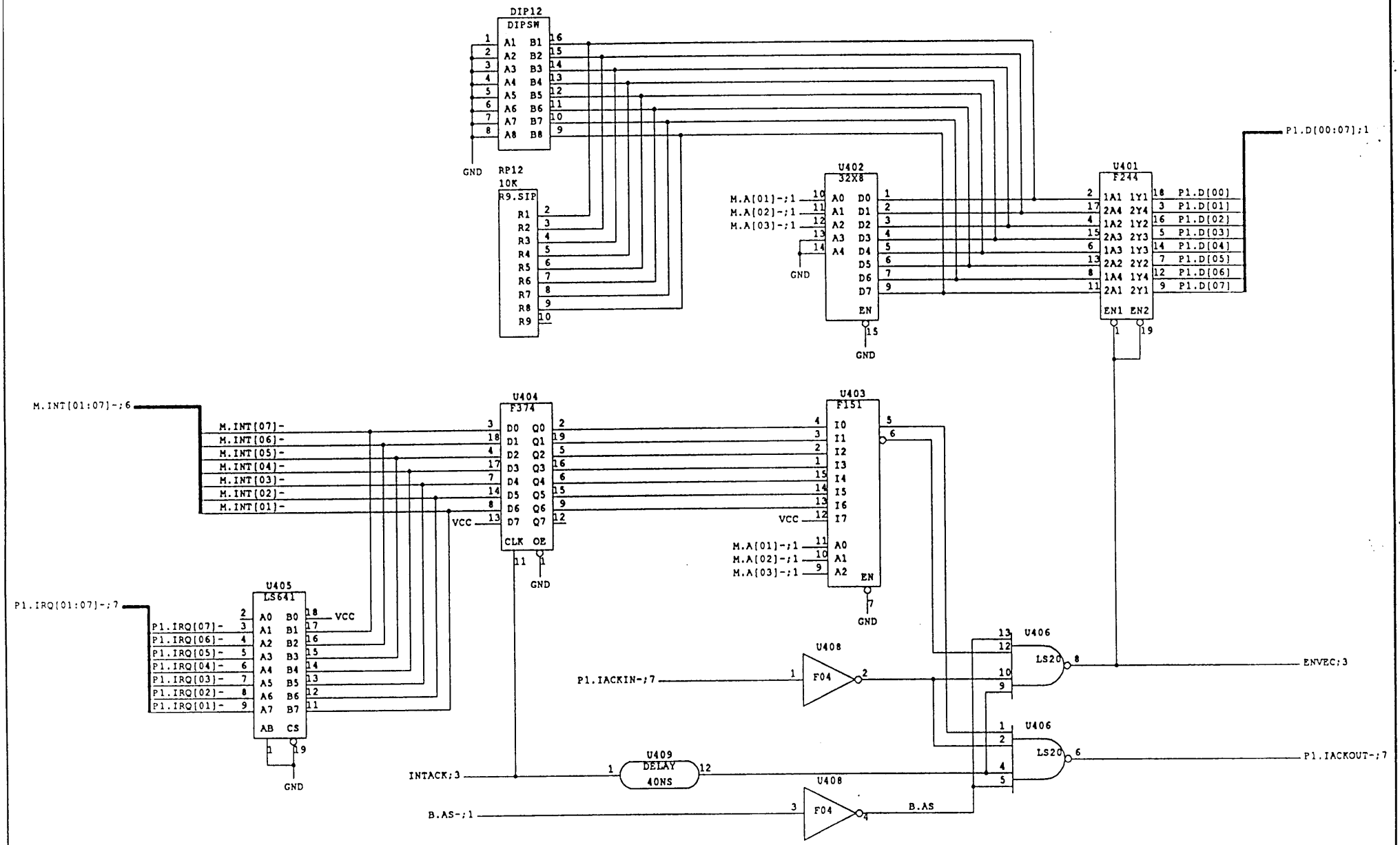
Title:	VME MULTIBUS ADAPTER MOD 160	Drawing: 501-1054-05	Rev: B
Sheet:	2	File:	sh2.d
Engineer:		Date:	Thu Oct 13 11:27:00 1988

ECO	Description	Date	Approvals



Title:	VME MULTIBUS ADAPTER MOD 160	Drawing: 501-1054-05	Rev: B
Sheet:	3	File:	sh3.d
Engineer:		Date:	Thu Oct 13 11:27:24 1988

ECO	Description	Date	Approvals



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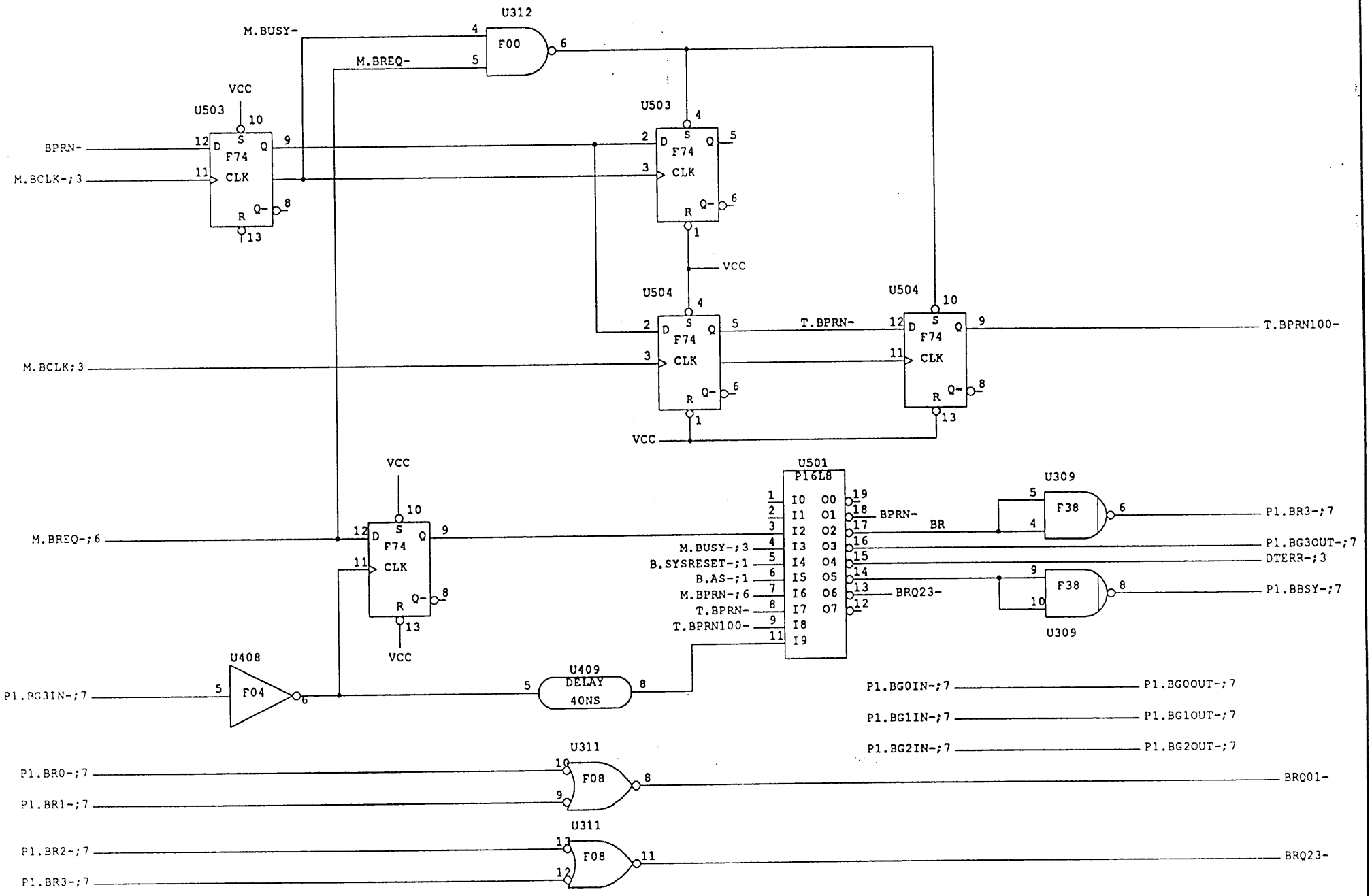
Sheet:	4	File:	sh4.d
Engineer:		Date:	Thu Oct 13 11:27:48 1988

ECO	Description	Date	Approvals



Title:	VME MULTIBUS ADAPTER MOD 160	Drawing: 501-1054-05	Rev: B
Sheet:	5	File:	sh5.d
Engineer:		Date:	Thu Oct 13 11:28:09 1988

ECO	Description	Date	Approvals

RP13
1K
R9.SIP
R1 2 M.INH2-
R2 3 M.INH1-
R3 4 M.IOWC-;3
R4 5 M.MWTC-;3
R5 6 M.BREQ-;5
R6 7
R7 8 B.SYSRESET-;1
R8 9
R9 10

RP14
1K
M.INT[00:07]-;4
R9.SIP
R1 2 M.INTA-
R2 3 M.INT[07]-
R3 4 M.INT[06]-
R4 5 M.INT[05]-
R5 6 M.INT[04]-
R6 7 M.INT[03]-
R7 8 M.INT[02]-
R8 9 M.INT[01]-
R9 10 M.INT[00]-

RP15
1K
R9.SIP
R1 2
R2 3 M.CBRQ-
R3 4 M.LOCK
R4 5 M.XACK-;3
R5 6 M.IORC-;3
R6 7 M.MRDC-;3
R7 8 M.BUSY-;3
R8 9
R9 10

RP16
2.2K
R9.SIP
R1 2 M.D[01]-;1
R2 3 M.D[03]-;1
R3 4 M.D[05]-;1
R4 5 M.D[07]-;1
R5 6 M.D[09]-;1
R6 7 M.D[11]-;1
R7 8 M.D[13]-;1
R8 9 M.D[15]-;1
R9 10

RP17
2.2K
R9.SIP
R1 2 M.D[00]-;1
R2 3 M.D[02]-;1
R3 4 M.D[04]-;1
R4 5 M.D[06]-;1
R5 6 M.D[08]-;1
R6 7 M.D[10]-;1
R7 8 M.D[12]-;1
R8 9 M.D[14]-;1
R9 10

RP18
2.2K
R9.SIP
R1 2 M.A[00]-;1
R2 3 M.A[02]-;1
R3 4 M.A[04]-;1
R4 5 M.A[06]-;1
R5 6 M.A[08]-;1
R6 7 M.A[10]-;1
R7 8 M.A[12]-;1
R8 9 M.A[14]-;1
R9 10

RP19
2.2K
R9.SIP
R1 2 M.A[01]-;1
R2 3 M.A[03]-;1
R3 4 M.A[05]-;1
R4 5 M.A[07]-;1
R5 6 M.A[09]-;1
R6 7 M.A[11]-;1
R7 8 M.A[13]-;1
R8 9 M.A[15]-;1
R9 10

RP20
2.2K
R9.SIP
R1 2 M.A[16]-;1
R2 3 M.A[17]-;1
R3 4 M.A[18]-;1
R4 5 M.A[19]-;1
R5 6 M.A[20]-;1
R6 7 M.A[21]-;1
R7 8 M.A[22]-;1
R8 9 M.A[23]-;1
R9 10 M.BHEN-;3

RP21
1K
R9.SIP
R1 2 P2.17;7
R2 3 P2.18;7
R3 4 P2.19;7
R4 5 P2.20;7
R5 6 P2.13;7
R6 7
R7 8
R8 9
R9 10

J700
D86

GND	1	2	GND
VCC	3	4	VCC
VCC	5	6	VCC
+12V	7	8	+12V
-5V	9	10	-5V
GND	11	12	GND
M.BCLK-;3	13	14	B.SYSRESET-;1
M.BPRN-;5	15	16	M.BPRO-
M.BUSY-;3	17	18	M.BREQ-;5
M.MRDC-;3	19	20	M.MWTC-;3
M.IORC-;3	21	22	M.IOWC-;3
M.XACK-;3	23	24	M.INH1-
M.LOCK-	25	26	M.INH2-
M.BHEN-;3	27	28	M.A16-;1
M.CBRQ-	29	30	M.A17-;1
M.CCLK-;3	31	32	M.A18-;1
M.INTA-	33	34	M.A19-;1
M.INT06-;4	35	36	M.INT07-;4
M.INT04-;4	37	38	M.INT05-;4
M.INT02-;4	39	40	M.INT03-;4
M.INT00-;4	41	42	M.INT01-;4
M.A[14]-;1	43	44	M.A[15]-;1
M.A[12]-;1	45	46	M.A[13]-;1
M.A[10]-;1	47	48	M.A[11]-;1
M.A[08]-;1	49	50	M.A[09]-;1
M.A[06]-;1	51	52	M.A[07]-;1
M.A[04]-;1	53	54	M.A[05]-;1
M.A[02]-;1	55	56	M.A[03]-;1
M.A[00]-;1	57	58	M.A[01]-;1
M.D[14]-;1	59	60	M.D[15]-;1
M.D[12]-;1	61	62	M.D[13]-;1
M.D[10]-;1	63	64	M.D[11]-;1
M.D[08]-;1	65	66	M.D[09]-;1
M.D[06]-;1	67	68	M.D[07]-;1
M.D[04]-;1	69	70	M.D[05]-;1
M.D[02]-;1	71	72	M.D[03]-;1
M.D[00]-;1	73	74	M.D[01]-;1
GND	75	76	GND
	77	78	
-12V	79	80	-12V
VCC	81	82	VCC
VCC	83	84	VCC
GND	85	86	GND

J701
D60

P2.1;7	1	2	P2.2;7
P2.3;7	3	4	P2.4;7
P2.5;7	5	6	P2.6;7
P2.7;7	7	8	P2.8;7
P2.9;7	9	10	P2.10;7
P2.11;7	11	12	P2.12;7
P2.13;7	13	14	P2.14;7
P2.15;7	15	16	P2.16;7
P2.17;7	17	18	P2.18;7
P2.19;7	19	20	P2.20;7
P2.21;7	21	22	P2.22;7
P2.23;7	23	24	P2.24;7
P2.25;7	25	26	P2.26;7
P2.27;7	27	28	P2.28;7
P2.29;7	29	30	P2.30;7
P2.31;7	31	32	P2.32;7
P2.33;7	33	34	P2.34;7
P2.35;7	35	36	P2.36;7
P2.37;7	37	38	P2.38;7
P2.39;7	39	40	P2.40;7
P2.41;7	41	42	P2.42;7
P2.43;7	43	44	P2.44;7
P2.45;7	45	46	P2.46;7
P2.47;7	47	48	P2.48;7
P2.49;7	49	50	P2.50;7
P2.51;7	51	52	P2.52;7
P2.53;7	53	54	P2.54;7
P2.55;7	55	56	P2.56;7
P2.57;7	57	58	P2.58;7
P2.59;7	59	60	P2.60;7

Title:	VME MULTIBUS ADAPTER MOD 160	Drawing: 501-1054-05	Rev: B
Sheet:	6	File:	sh6.d
Engineer:		Date:	Thu Oct 13 11:28:32 1988

ECO	Description	Date	Approvals

J800

DIN CONNECTOR

1 P2.2;6	33 VCC	65 P2.1;6
2 P2.4;6	34 GND	66 P2.3;6
3 P2.6;6	35	67 P2.5;6
4 P2.8;6	36 P1.A[24];2	68 P2.7;6
5 P2.10;6	37 P1.A[25];2	69 P2.9;6
6 P2.12;6	38 P1.A[26];2	70 P2.11;6
7 P2.14;6	39 P1.A[27];2	71 P2.13;6
8 P2.16;6	40 P1.A[28];2	72 P2.15;6
9 P2.18;6	41 P1.A[29];2	73 P2.17;6
10 P2.20;6	42 P1.A[30];2	74 P2.19;6
11 P2.22;6	43 P1.A[31];2	75 P2.21;6
12 P2.24;6	44 GND	76 P2.23;6
13 P2.26;6	45 VCC	77 P2.25;6
14 P2.28;6	46 P1.D[16];1	78 P2.27;6
15 P2.30;6	47 P1.D[17];1	79 P2.29;6
16 P2.32;6	48 P1.D[18];1	80 P2.31;6
17 P2.34;6	49 P1.D[19];1	81 P2.33;6
18 P2.36;6	50 P1.D[20];1	82 P2.35;6
19 P2.38;6	51 P1.D[21];1	83 P2.37;6
20 P2.40;6	52 P1.D[22];1	84 P2.39;6
21 P2.42;6	53 P1.D[23];1	85 P2.43;6
22 P2.44;6	54 GND	86 P2.45;6
23 P2.46;6	55 P1.D[24];1	87 P2.47;6
24 P2.48;6	56 P1.D[25];1	88 P2.49;6
25 P2.50;6	57 P1.D[26];1	89 P2.51;6
26 P2.52;6	58 P1.D[27];1	90 P2.53;6
27 P2.54;6	59 P1.D[28];1	91 P2.55;1;6
28 P2.56;1;6	60 P1.D[29];1	92 P2.57;1;6
29 P2.58;1;6	61 P1.D[30];1	93 P2.59;6
30 P2.60;6	62 P1.D[31];1	94
31	63 GND	95
32	64 VCC	96

J801

DIN CONNECTOR

1 P1.D[00];1	33 P1.BBSY-;5	65 P1.D[08];1
2 P1.D[01];1	34 P1.BCLR-	66 P1.D[09];1
3 P1.D[02];1	35 P1.ACFAIL-	67 P1.D[10];1
4 P1.D[03];1	36 P1.BG0IN-;5	68 P1.D[11];1
5 P1.D[04];1	37 P1.BG0OUT-;5	69 P1.D[12];1
6 P1.D[05];1	38 P1.BG1IN-;5	70 P1.D[13];1
7 P1.D[06];1	39 P1.BG1OUT-;5	71 P1.D[14];1
8 P1.D[07];1	40 P1.BG2IN-;5	72 P1.D[15];1
9 GND	41 P1.BG2OUT-;5	73 GND
10 P1.SYSCLK;1	42 P1.BG3IN-;5	74 P1.SYSFAIL-
11 GND	43 P1.BG3OUT-;5	75 P1.BERR-;1
12 P1.DS1-;3	44 P1.BR0-;5	76 P1.SYSRESET-;1
13 P1.DS0-;3	45 P1.BR1-;5	77 P1.LWORD-;3
14 P1.WRITE-;3	46 P1.BR2-;5	78 P1.AM5;3
15 GND	47 P1.BR3-;5	79 P1.A[23];2
16 P1.DTACK-;3	48 P1.AM0;3	80 P1.A[22];2
17 GND	49 P1.AM1;3	81 P1.A[21];2
18 P1.AS-;3	50 P1.AM2;3	82 P1.A[20];2
19 GND	51 P1.AM3;3	83 P1.A[19];2
20 P1.IACK-;3	52 GND	84 P1.A[18];2
21 P1.IACKIN-;4	53 P1.SERCLK;1	85 P1.A[17];2
22 P1.IACKOUT-;4	54 P1.SERDAT	86 P1.A[16];2
23 P1.AM4;3	55 GND	87 P1.A[15];2
24 P1.A[07];2	56 P1.IRQ[07]-;4	88 P1.A[14];2
25 P1.A[06];2	57 P1.IRQ[06]-;4	89 P1.A[13];2
26 P1.A[05];2	58 P1.IRQ[05]-;4	90 P1.A[12];2
27 P1.A[04];2	59 P1.IRQ[04]-;4	91 P1.A[11];2
28 P1.A[03];2	60 P1.IRQ[03]-;4	92 P1.A[10];2
29 P1.A[02];2	61 P1.IRQ[02]-;4	93 P1.A[09];2
30 P1.A[01];2	62 P1.IRQ[01]-;4	94 P1.A[08];2
31 -12V	63 +5VSTDBY	95 +12V
32 VCC	64 VCC	96 VCC

J802

DIN CONNECTOR

1 VCC	33	65 GND
2 VCC	34	66 GND
3 VCC	35	67 GND
4 VCC	36	68 GND
5 VCC	37	69 GND
6 VCC	38	70 GND
7 VCC	39	71 GND
8 VCC	40	72 GND
9 VCC	41	73 GND
10 VCC	42	74 GND
11 VCC	43	75 GND
12 VCC	44	76 GND
13 VCC	45	77 GND
14 VCC	46	78 GND
15 VCC	47	79 GND
16 VCC	48	80 GND
17 VCC	49	81 GND
18 VCC	50	82 GND
19 VCC	51	83 GND
20 VCC	52	84 GND
21 VCC	53	85 GND
22 VCC	54	86 GND
23 VCC	55	87 GND
24 VCC	56	88 GND
25 VCC	57	89 GND
26 +12V	58	90 +12V
27 +12V	59	91 +12V
28 -12V	60	92 -12V
29 -12V	61	93 -12V
30 -5V	62	94 -5V
31 -5V	63	95 -5V
32 -5V	64	96 -5V

Title: VME MULTIBUS ADAPTER MOD 160		Drawing: 501-1054-05	Rev: B
Sheet: 7		File: sh7.d	
Engineer:		Date: Thu Oct 13 11:28:52 1988	