TANDBERG 5 1/4 " Streaming 1/4" Tape Cartridge Drive Maintenance and Parts Manual

TDC 3319

Maintenance Manual

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Since this manual was produced while the TDC 3319 was still in its early stages, there are discrepancies between some of the descriptions in it and the actual product.

Most of them are known to us and will be corrected when the manual is updated. Nevertheless we would very much appreciate your corrections and comments. Please write or phone our Documentation Department at the address on the left below.

TANDBERG DATA A/S
P.O. Box 9 Korsvoll
N-0808 OSLO 8
NORWAY
Phone (47-2) 23 20 80
Telex 72633 tdata n

TANDBERG DATA INC.
571 N. Poplar, Suite H
Orange, CA 92668
USA
Phone 714-978-6771

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Publ. no.	Part no.	Title
5446	402451	TDC 3319 Reference Manual
5455	402508	TDC 3319 Reference Card
5447	402732	TDC 3200 The QIC-24 and QIC-02 Standard, Revision D

We appreciate any comments on this publication.

CONTENTS

Continued overleaf

1. READ THIS FIRST

This manual is intended for service technicians who have attended a Tandberg Data service course on TDC 3300 drives.

To avoid a lot of double work and to save space, we have left out of this manual such descriptions of the drive that are already given in the "TDC 3319 Reference Manual" (part number 402451, publication number 5446). We therefore strongly recommend that the reference manual be considered a part of the maintenance manual, and that you use it as a source of details that this manual does not supply.

This manual can be regarded as divided into three main parts. The first part (chapters 1, 2, and 3) gives a general description of the drive. It comprises an illustrated description, an interconnection diagram and block diagrams.

The second part (chapters 4, 5, 6, and 7) contains schematics, parts lists, mnemonics lists, and component location drawings of each printed circuit board. Adjustments, where relevant, are dealt with in the description of each schematic diagram.

The third part (chapters 8, 9, 10, and appendix) explains the drive's resident selftests and how to replace all mechanical assemblies. Furthermore you'll find an illustrated spare module list and summaries of commands and status bytes for the basic drive.

Contact our local representative or our Sales Department if you have any questions regarding service courses or additional documentation.

Updating/backdating

The updating routine for this manual is based on the distribution of ECNs (Engineering Change Notices). The ECNs describe changes in hardware and firmware from the time of the first release of the product.

If you want updating/backdating for your maintenance manual, please fill in the updating card which is inserted in the front of this manual and mail it to us. This is definitely the easiest way to get your name on our ECN mailing list!!

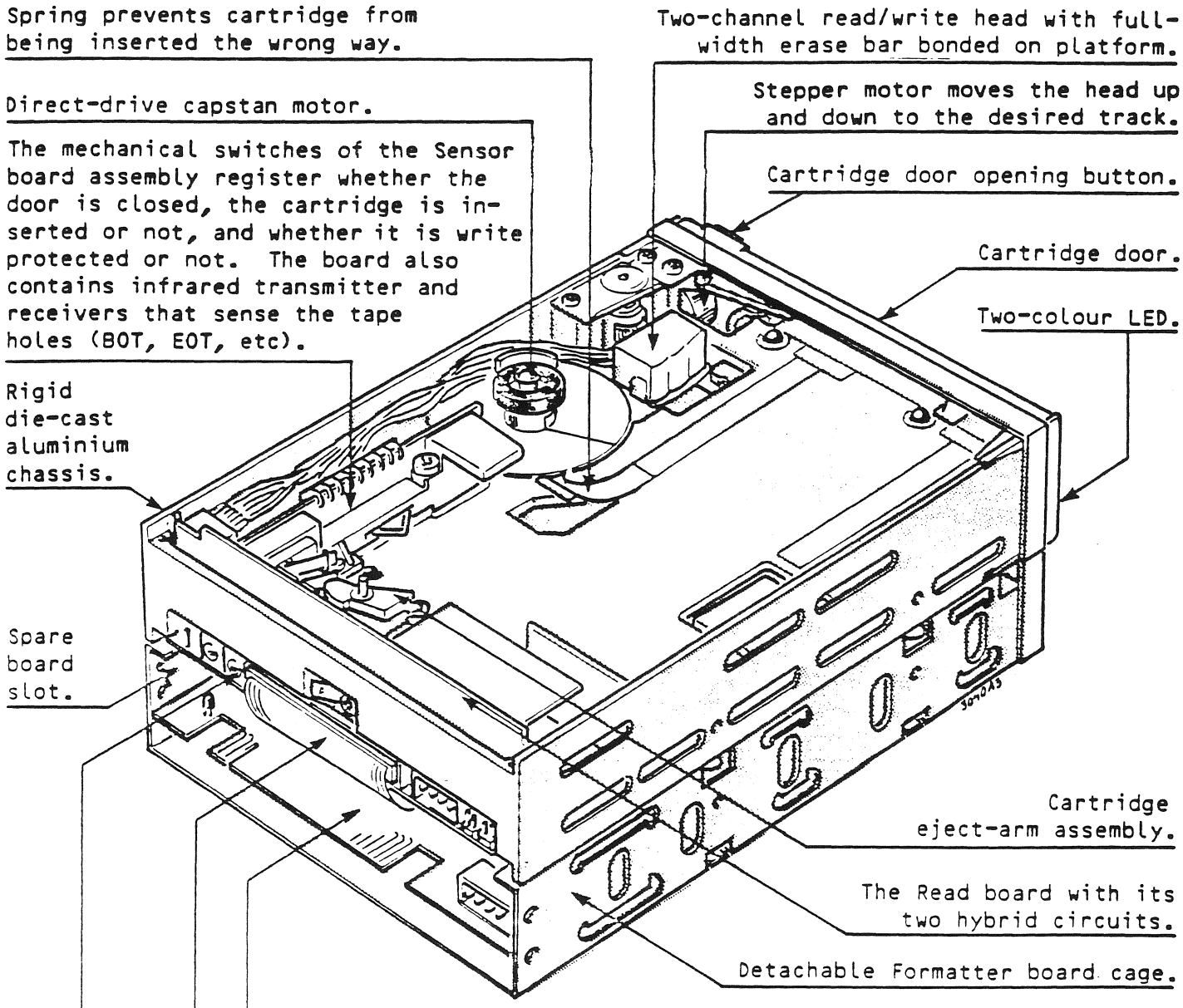
Since this manual was produced while the TDC 3319 was still in its early stages, there are discrepancies between some of the descriptions in it and the actual product.

Most of them are known to us and will be corrected when the manual is updated. Nevertheless we would very much appreciate your corrections and comments.

2. A SHORT DESCRIPTION OF THE DRIVE

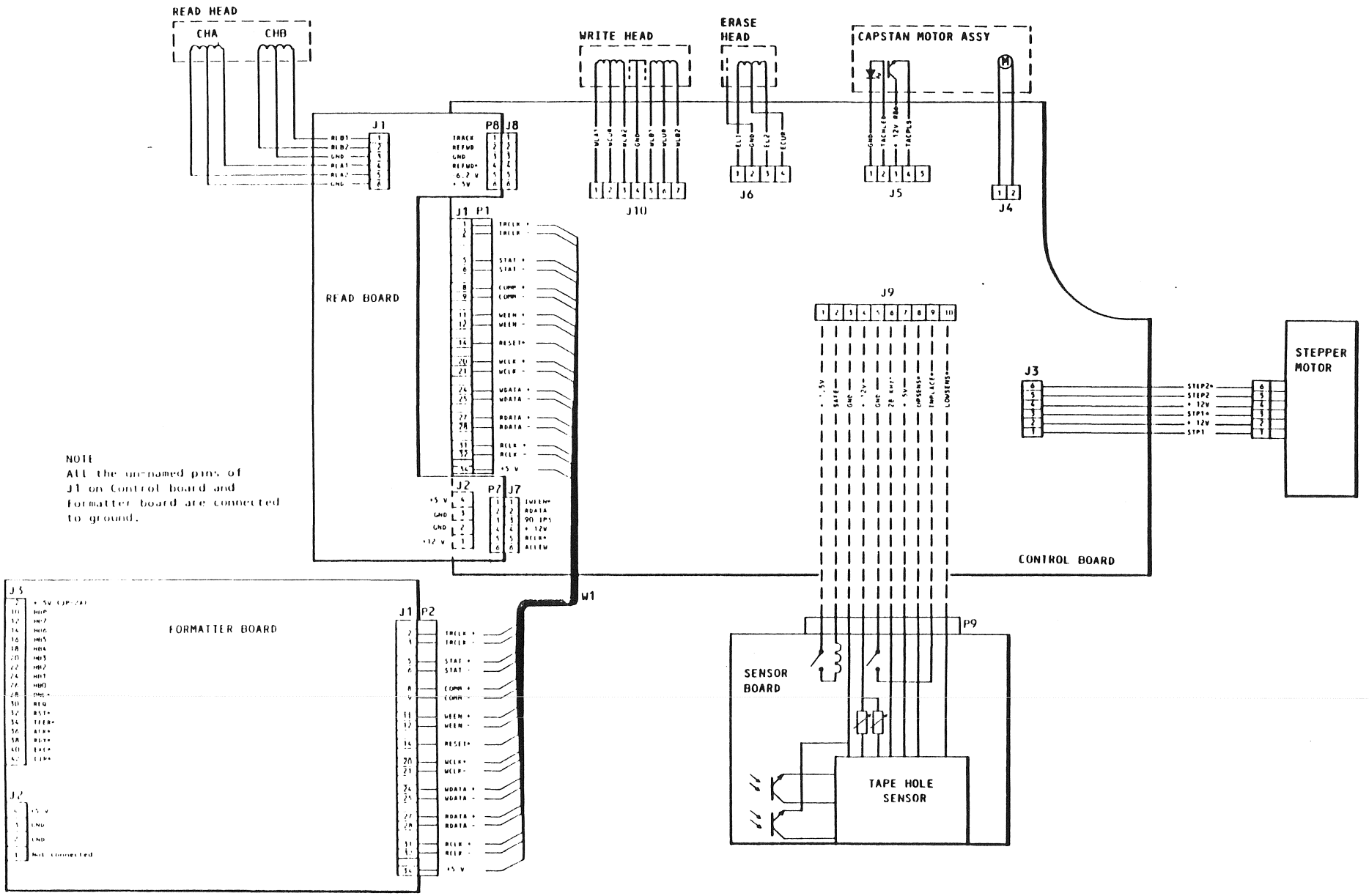
2.1 Illustrated Description

The Tandberg Data TDC 3319 is a streaming 1/4" tape cartridge drive comprising the TDC 3309 (basic drive) and the TDC 3350 (intelligent formatter). It records and reads serially on nine tracks, and can store from 45 Mbytes to 60 Mbytes depending on tape length. The mode of operation is streaming, i.e. the drive is designed to run the whole length of the tape without (normally) interruption.



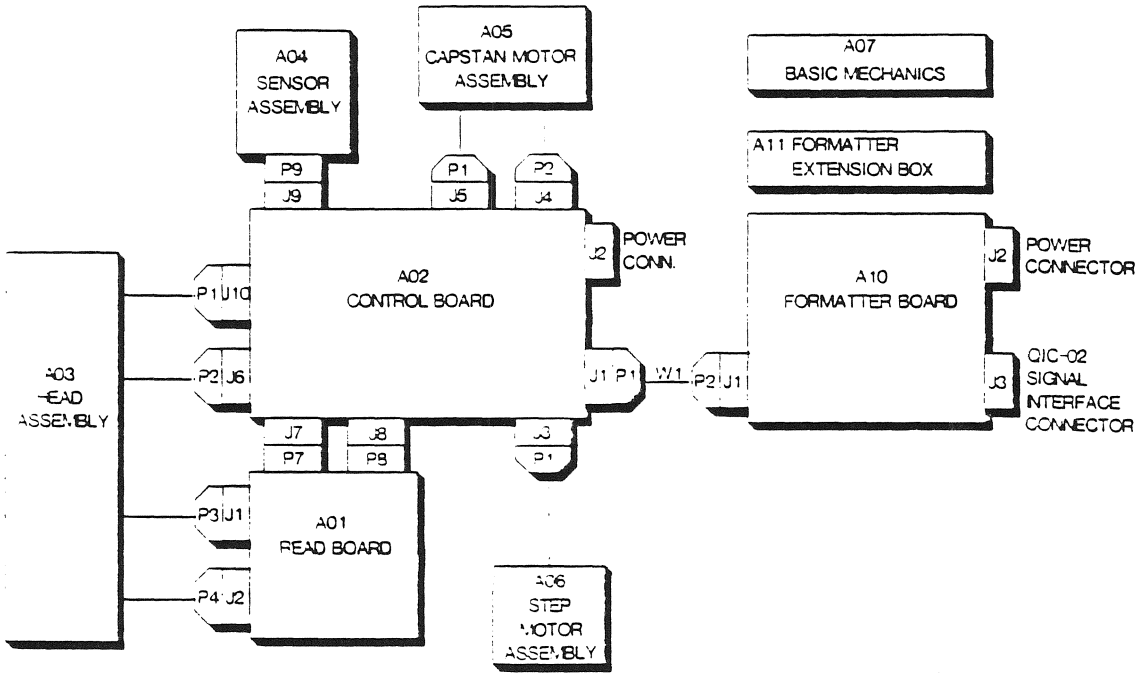
NOTE: Drive shown without top cover!

2.2 Interconnection Diagram



3. BLOCK DIAGRAMS

3.1 Overall Block Diagram



Overall block diagram.

CAPSTAN MOTOR ASSEMBLY

The capstan Motor with its built-in tacho sensor is part of the Capstan Servo which provides the tape motion required for the various operating modes: 45/90 ips, read/write, wind/rewind. The motor is DC operated. See separate block diagram of Capstan Servo.

STEPPER MOTOR ASSEMBLY

Part of the head motion system which ensures that reading or writing takes place on the exact track requested by the host. The high-resolution stepper mechanism has 122 steps between each track (5 micro-metres per step). The head motion is controlled by the basic drive microprocessor which allows high accuracy dynamic head positioning. A detailed description of the principles for the track position algorithm is given in the TDC 3319 Reference Manual, section 2.3.

HEAD ASSEMBLY

The read/write and erase functions are combined in one common head. The erase section is active over the full width of the tape and thus erases all tracks in one operation.

The read/write sections are active only for one track at a time. Since a read check is always carried out after the writing of each block of data, the head has one section for forward tape motion and one section for reverse tape motion. Track location on the tape is illustrated in the TDC 3319 Reference Manual, subsection 3.5.2.

SENSOR ASSEMBLY

The following sensors are located on the Sensor board (see interconnection diagram, section 2.2):

- SAFE: A microswitch operated by the write protect switch on the tape cartridge. Prevents writing when the cartridge is write protected.

- IN PLACE/DOOR CLOSED: A microswitch operated by the tape cartridge. Prevents operation when the door is not closed or when no cartridge is inserted.

- LP/BOT/EOT/EW: Opto-electronic sensors that detect holes in the upper and lower half of the tape. The sequence of pulses from the two sensors allow the control logic to determine whether a BOT, an EOT, an LP or an EW has been detected.

CONTROL BOARD

See separate block diagram and description, section 3.2.

READ BOARD

See separate block diagram and description, section 3.4.

FORMATTER BOARD

See separate block diagram and description, section 3.5.

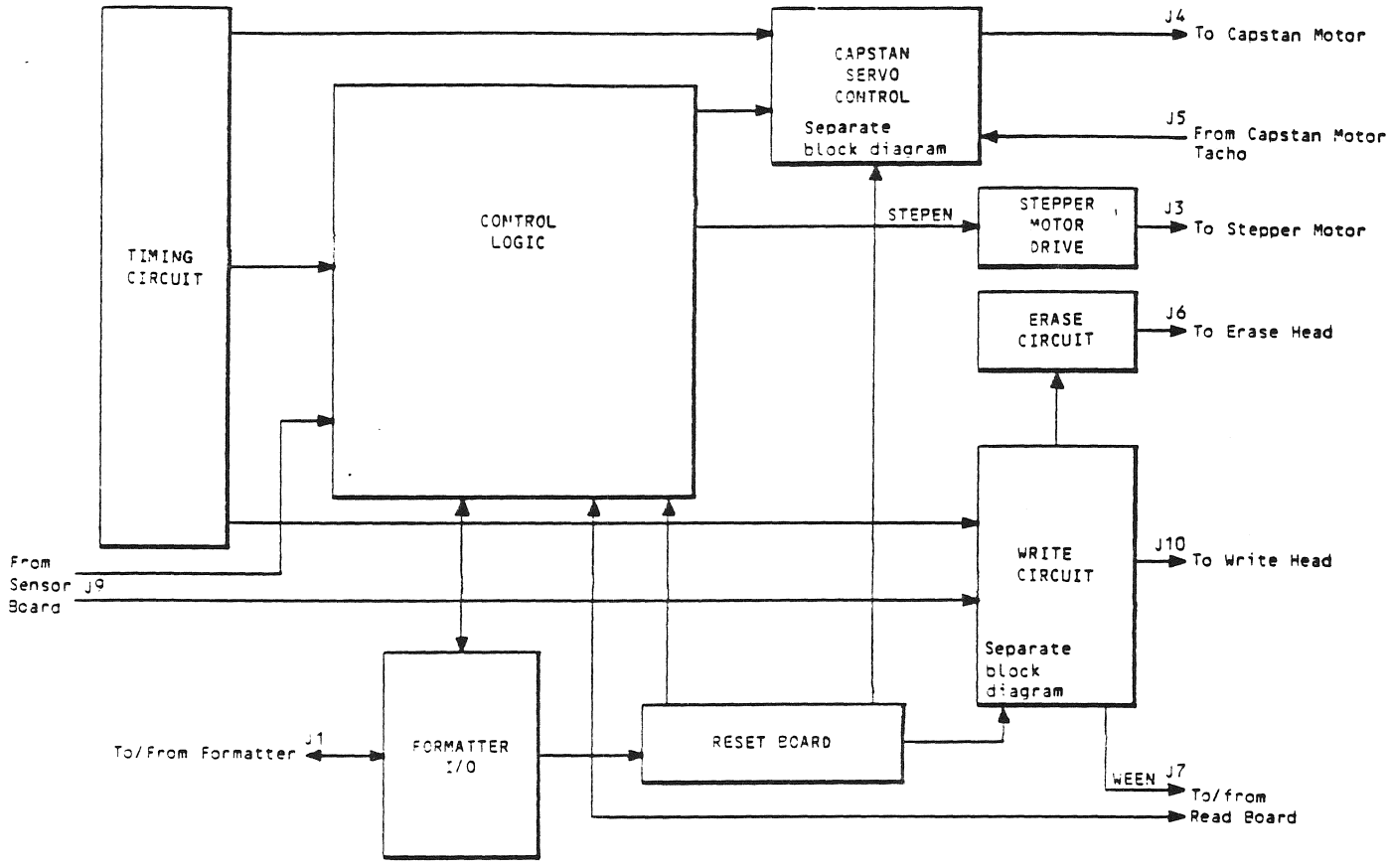
3.2 Control Board Block Diagram

CONTROL LOGIC

The central component of this block is a microprocessor that reads the status of all sensors, executes commands from the Formatter and accordingly controls the read/write and erase circuits, head motion circuits and supervises the Capstan Servo. The processor is automatically programmed during reset/power-up to operate in single-chip mode as an input/output processor.

WRITE CIRCUIT

The read/write head and the Write Amplifier have two channels: channel A for forward direction and channel B for reverse direction. Write current is supplied to the head when a not-write-protected cartridge is inserted and the drive is set in Write mode. The circuit also adjusts the write current according to the tape type in use.
Refer to detailed diagram in chapter 4 (Control board sheet 3).



Block diagram of the Control board.

ERASE CIRCUIT

Supplies erase current to the erase head.

TIMING CIRCUITS

A stable 7.2 MHz signal from a crystal controlled oscillator is scaled down to provide the various timing signals used in the Control Logic, the Write Circuit and the Capstan Servo Control.

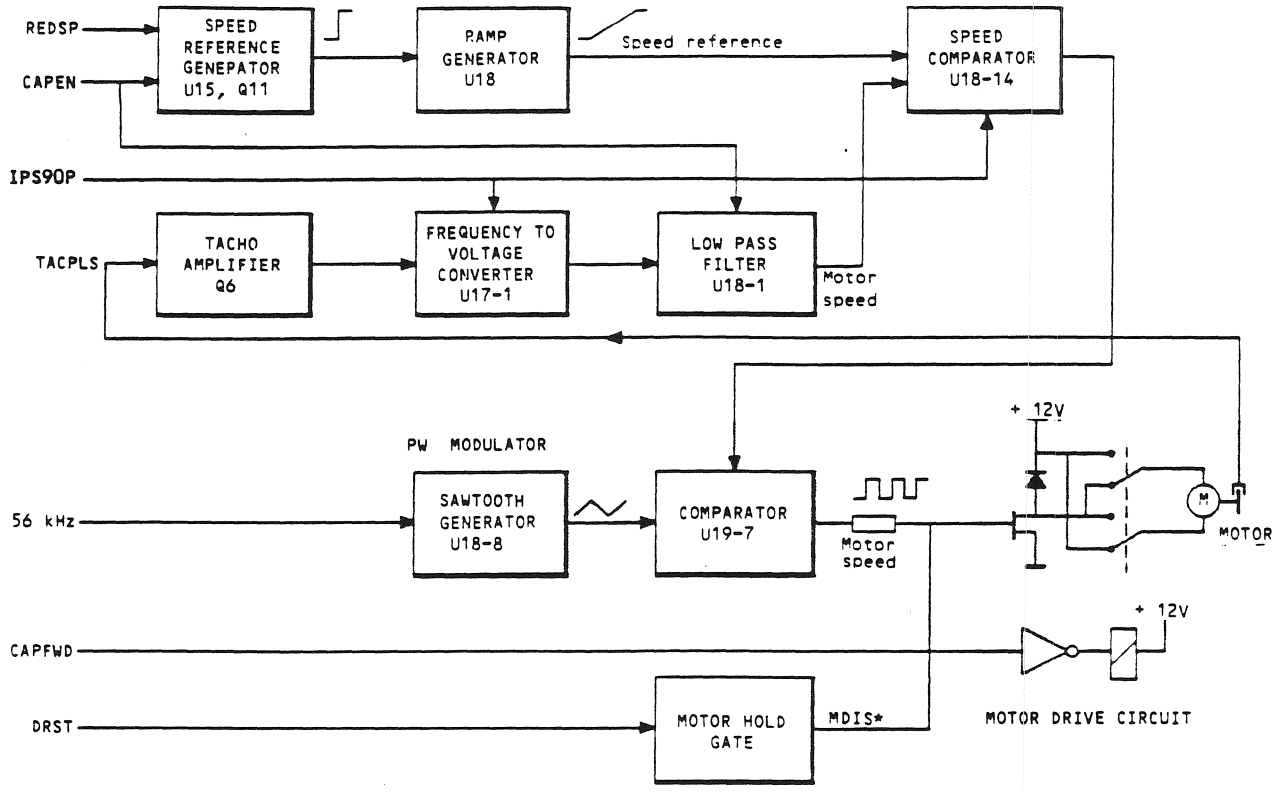
FORMATTER I/O

Input and output buffers for signals from and to the Formatter.

CAPSTAN SERVO CONTROL

See separate block diagram, section 3.3.

3.3 Capstan Servo Block Diagram



Block diagram of the Capstan servo

The Capstan servo controls the capstan motor. The servo loop is closed by the feedback from the opto-electronic tacho generator in the motor. The 64-slot disc on the motor shaft interrupts the light to the opto-sensor and provides an output signal with a frequency proportional to the motor speed. This signal passes through the Tacho Amplifier and is applied to an accurate frequency-to-voltage converter that provides a voltage proportional to the motor speed.

The motor speed signal is compared with a signal originating in the Speed Reference Generator. Any difference between the two signals is amplified and results in a corrective input to the Pulse Width Modulator (PWM) which drives the motor.

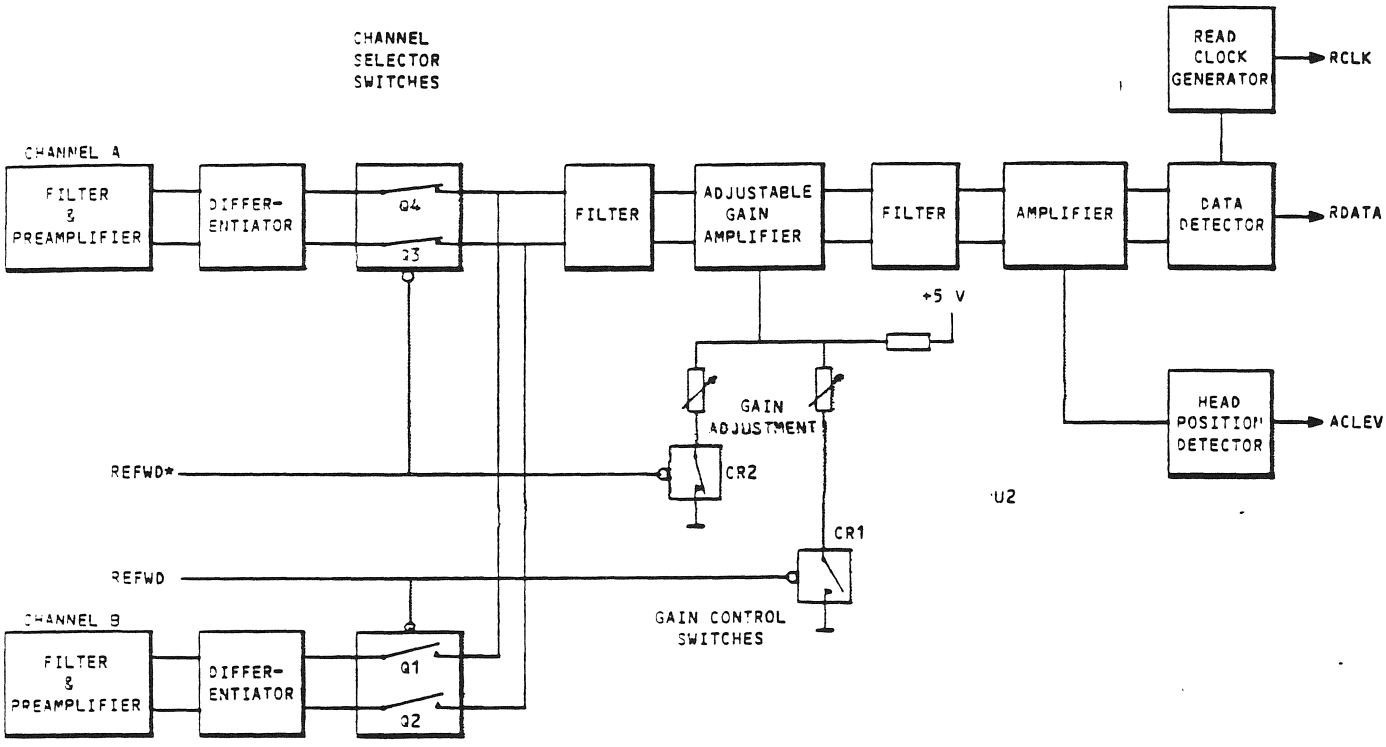
The PWM comprises a sawtooth generator operating at 56 kHz and a comparator that generates a pulse signal with the duty cycle required to maintain constant speed.

The speed can be set at 45 or 90 ips by the IPS90P signal which determines the conversion ratio of the Frequency-to-voltage Converter.

Start/stop is controlled by the CAPEN signal which applies the reference voltage within the Speed Reference Generator. REDSPD reduces the capstan speed by 10 % for test purposes. During stop the motor current is cut off.

Linear acceleration is ensured by applying the speed reference voltage via the Ramp Generator which converts the voltage step into a ramp voltage. During power-up or reset the MDIS* signal will inhibit the motor drive power FET.

3.4 Read Board Block Diagram



Block diagram of the Read board.

The signal from the read head in operation is applied to the channel selector switches via a filter, a preamplifier and a differentiator. The channel selector is operated by the REFWD signal. The state of this signal depends on whether the tape motion is forward or reverse.

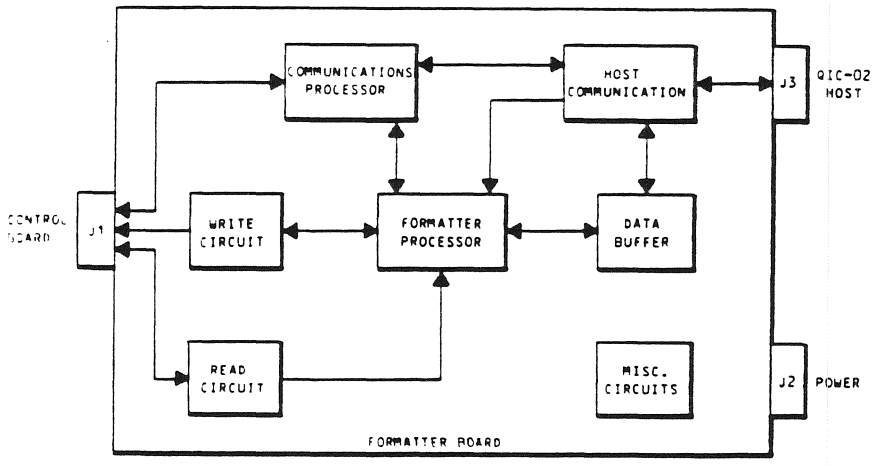
The differentiation shapes the signal into a waveform in which the peaks of the read head voltage have been transformed into distinct zero crossings.

After further filtering, the signal is applied to the Data Detector in which an RPLS pulse is generated for each binary "one" in the signal. RPLS is then applied to the Read Clock generator which phase-locks to the signal. The output of the Read Clock Generator, RCLK*, follows the long term variations in the bit-rate of the signal reproduced from tape.

Further, the RPLS pulses are elongated to establish the restored data signal, RDATA, in which the "ones" are represented by high and the "zeroes" by low signal levels during the whole clock period.

The ACLEV signal obtained by peak detection of the signal from the amplifier is utilized by the Control Logic to detect the edge of the tape or the position of the reference track and thus establish the basis for the head positioning system.

3.5 Formatter Block Diagram



Overall block diagram of the Formatter board

The formatter is the interface between the host and the tape unit. In one direction it converts parallel digital data from the host to serial data in GCR code for writing on the tape. In the opposite direction the formatter transforms serial GCR coded data from the tape into parallel digital data to the host.

HOST COMMUNICATION

Host Communication is the interface between the Formatter and the host. It contains the ports and the handshake logic required for the communication between the HD-bus and various formatter buses.

COMMUNICATIONS PROCESSOR

The Communications Processor decodes QIC-02 commands from the host, and issues commands to the control board processor in the basic drive and to the Formatter Processor. The Communications Processor also reads status signals from the processor on the control board in the basic drive and from the Formatter Processor.

FORMATTER PROCESSOR

The Formatter Processor has the primary control of the data flow on the FD and FDB buses, and it controls the Write Circuits in order to create the required data block format (described in section 2.3 of the TDC 3319 Reference Manual). The formatting involves generation of preamble and postamble, generation of the marker byte, controlling that the data field always contains 512 bytes, and assigning and generating the block address.

During a read operation the formatter processor starts the decoding of data when the read circuits have detected the block marker. At the end of the data block follows decoding of the block address, and the validation of the CRC check which determines whether the block shall be transferred to the host or whether it must be read once more. (Further explained in the TDC 3319 Reference Manual, subsection 8.8.6.)

DATA BUFFER

The Data Buffer provides sufficient storage capacity to allow data written on the tape to be stored long enough for re-writing if the read-after-write check indicates data error. Writing will not start until at least one data block (512 bytes) has been loaded into the buffer. While one block is being recorded, more data can be loaded within the total buffer capacity which is 4K minimum (optionally 8 or 16K). Except for the last 512 bytes already written on the tape and the 512 bytes being written, the total buffer area is always available for loading from the host because new data will be written over data already in the buffer, provided that this data has been successfully verified.

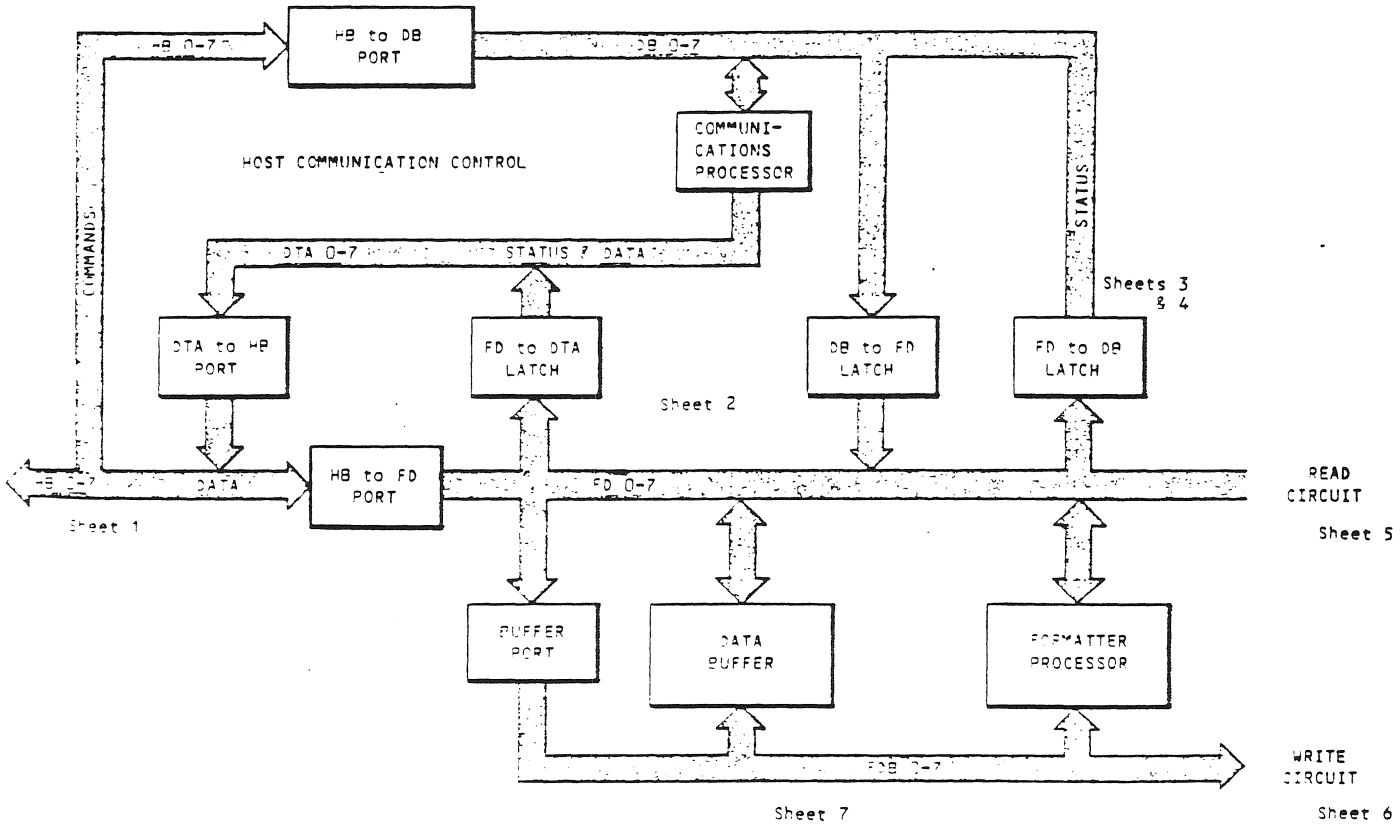
During read operations, each block of data is loaded into the buffer and remains there in queue for transferal to the host via the FD-to-DB port.

READ CIRCUITS

The Read Circuits process the RDATA signal from the Control Board in the Basic Drive unit. This involves detection of the file marker which follows immediately after the preamble, and conversion of of the GCR coded serial data into binary data on parallel form.

WRITE CIRCUITS

The Write Circuits convert parallel binary data from the host into GCR-coded serial data; and generates the CRC character included with each data block to be written on the tape.



Block diagram of Formatter bus connections.

THE FOLLOWING DESCRIPTION CONCERNS BUS MANAGEMENT AND REFERS TO THE BLOCK DIAGRAM ON THE PREVIOUS PAGE.

Communication on the buses is time-shared between the various circuits connected to each bus. The ports are controlled in such a manner that no collisions occur in the communication path.

HB-TO-DB PORT

Carries commands from the host to the Formatter. Controlled by the Communications Processor.

HB-TO-FD PORT

Carries data from the host to the Data Buffer. Controlled by the I/O Control. Enabled while the Formatter Processor executes a jump-instruction (FD-bus is free) whenever the host has data to be transferred to the formatter.

DTA-TO-HB PORT

Carries data from the Data Buffer via the FD-to-DTA port; or status signals from the Communication Processor to the host. Controlled by the Communication Processor.

FD-TO-DTA LATCH

Carries data from the Data Buffer to the host via the DTA-to-HB port. Controlled by the Communications Processor.

DB-TO-FD LATCH

Carries commands from the Communications Processor to the Formatter Processor. Loaded under control of the Communications Processor. Unloaded under control of the Formatter Processor (mailbox function).

FD-TO-DB LATCH

Carries status signals from the Formatter Processor to the Communication Processor. Loaded under control of the Formatter Processor. Unloaded under control of the Communications Processor (mailbox function).

BUFFER PORT

Carries data from the FD-bus to the FDB-bus. Permanently enabled.

4. CONTROL BOARD

4.1 Description/Adjustments/Schematic Diagrams

Sheet 1

SPEED REFERENCE GENERATOR

The voltage regulator U15 provides the reference voltage VREF. The reference voltage will only be applied to the Ramp Generator if Q11 is held cut off by CAPEN from the control logic.

REDSPD reduces the reference voltage to the Ramp Generator and hence reduces the speed by 10%.

RAMP GENERATOR

The voltage step applied to the Ramp Generator when the speed reference generator is enabled, gives a linearly rising voltage at the output (across C36). To maintain equal acceleration at 45 ips and 90 ips, the IPS90P signal connects C18 in parallel with C36 and thus reduces the ramp slope with a factor of 2.

TACHO AMPLIFIER

Amplifies the tacho pulses (TACPLS) to an amplitude suitable for the frequency-to-voltage converter. The time gaps between consequtive pulses, renamed CAPCNT, are monitored by the processor and the control logic to detect tape motion.

FREQUENCY-TO-VOLTAGE CONVERTER

The output signal at pin 6 of U17, a frequency-to-voltage converter, is a pulse train in which the duty cycle varies linearly with the tacho pulse rate at the input. The time constant and hence the conversion ratio can be varied by adjusting R16. When the 90-ips (IPS90P) is true, Q7 connects R19/R20 into the time constant circuit and thus alters the conversion ratio.

LOW PASS FILTER AND AMPLIFIER

Provides smoothing of the pulse signal from the frequency-to-voltage converter as well as the required phase stabilisation. The effect of the CAPEN signal is to offset the DC error voltage sufficiently to insure that there is absolutely no tape motion when the Speed Reference Generator is disenabled.

SPEED COMPARATOR

Compares the speed signal from the low pass filter with the speed reference signal. The resulting signal is applied to the PWM.

PULSE WIDTH MODULATOR (PWM)

Comparator U19-7 compares the speed error signal with the saw-tooth signal from generator U18-8 and produces a pulse modulated signal with a pulse width directly proportional to the required motor torque.

MOTOR HOLD GATE

Transistor Q9 connects the input of the Motor Drive Circuit to ground while DRST is present during power-up or reset, and will then prevent tape motion. Q13 has the same effect if +12 V fails.

MOTOR DRIVE CIRCUIT

The signal from the PWM is applied to the gate of the power FET Q10, which closes the motor circuit from +12 V during
the on-periods of the PWM signal provided the motor hold gate is not activated. The CAPFWD signal activates the relay K1 which changes the motor current and hence determines the direction of rotation.

DC/DC CONVERTER

Transistors Q3 and Q4 open and close in anti-phase. The circuit consists of two "current pumps": Q4 pumps a +12 V into C9
through CR1, then Q3 switches the negative side of C9 to the +12 V supply. This approximately doubles the voltage at the top of this capacitor referred to ground. C11 is now charged to approximately this voltage through CR2.
C10/CR3 and C14/CR4 operate in a way similar to C9/CR1 and C11/CR2, except that the positive side of C10 is switched to ground. This means that a negative charge is supplied to C14/C13 through CR4.
Regulator U10, offset by two diode voltage drops, provides a fairly stable -6.2 V supply.

TAPE SPEED ADJUSTMENT

Insert a cartridge and connect a frequency counter to the test pin.
IMPORTANT! 45-ips adjustment first!

45-ips adjustment

Conditions: Jumper JP1: OPEN
Jumper JP2: CLOSED

Momentarily short-circuit JP3, and adjust R16 to 1475 Hz on the frequency counter.

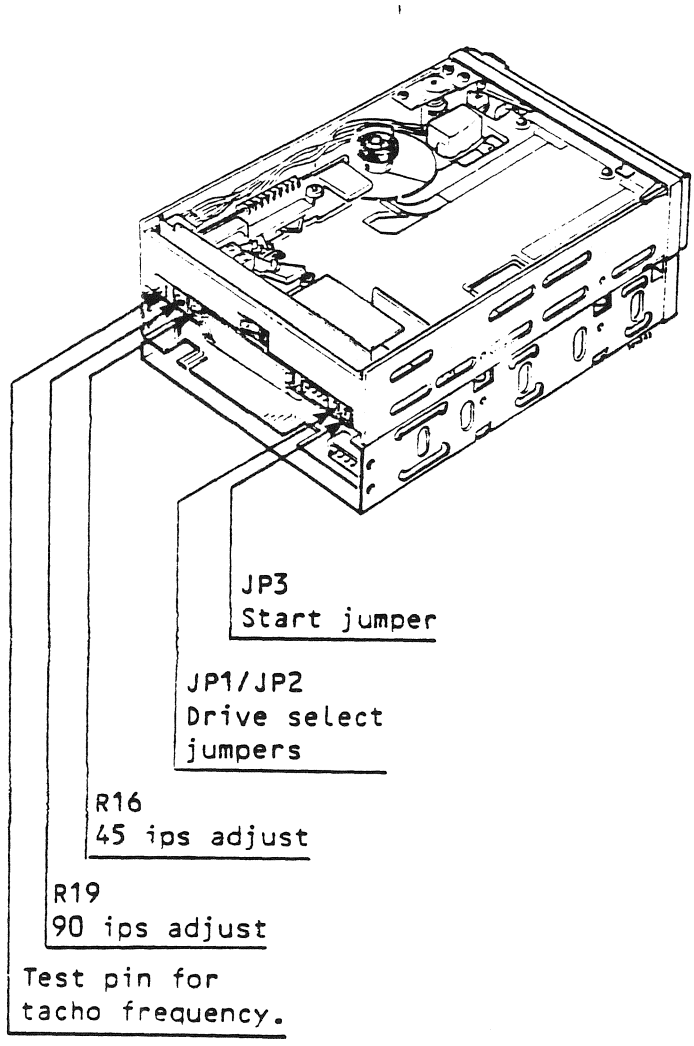
Alternatively, if no frequency counter is available, adjust for the brightest red light in the indicator LED at the front of the unit.

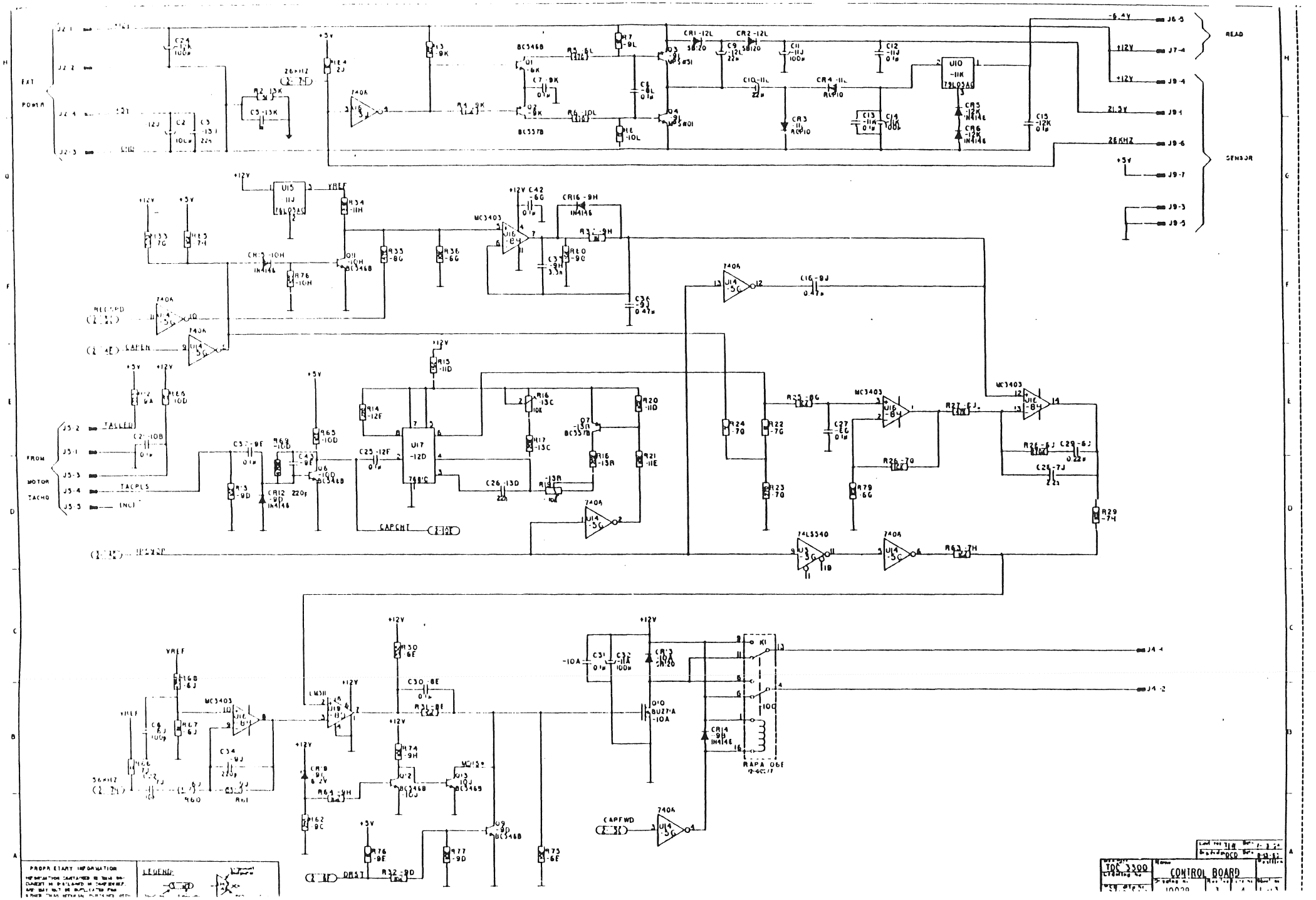
90 ips adjustment

Conditions: 45 ips tape speed must be correctly adjusted.
Jumper JP1: CLOSED
Jumper JP2: ~~OPEN~~ CLOSED

Momentarily short-circuit JP3 and adjust R19 to 2951 Hz.

Alternatively, if no frequency counter is avaliable, adjust for the brightest possible red light in the indicator LED at the front.




EXT POWER
FROM MOTOR TACHO
READ
SENSOR
CAPFWD
CAPENT
DRST
CONTROL BOARD
PROPRIETARY INFORMATION
LEGEND:

Sheet 2

TIMING CIRCUIT

The x-tal oscillator U1-3 operating at 7.2 MHz drives the ripple counter U4, from which the various clock signals are available.

CONTROL LOGIC

The microprocessor U9 is programmed during the power-up phase to operate as an input/output processor with no external data or address bus.

The mode programming of U9 is carried out automatically during power-up via the data selector U7 which applies +5 V to pins 8, 9, and 10 of U9 while the DRST* pulse is applied to U7. This sets U9 in single chip mode. After power-up the same lines are used for input signals connected via U7.

The processing of the input signals to produce the required outputs is controlled by a program stored in the internal program memory in U9.

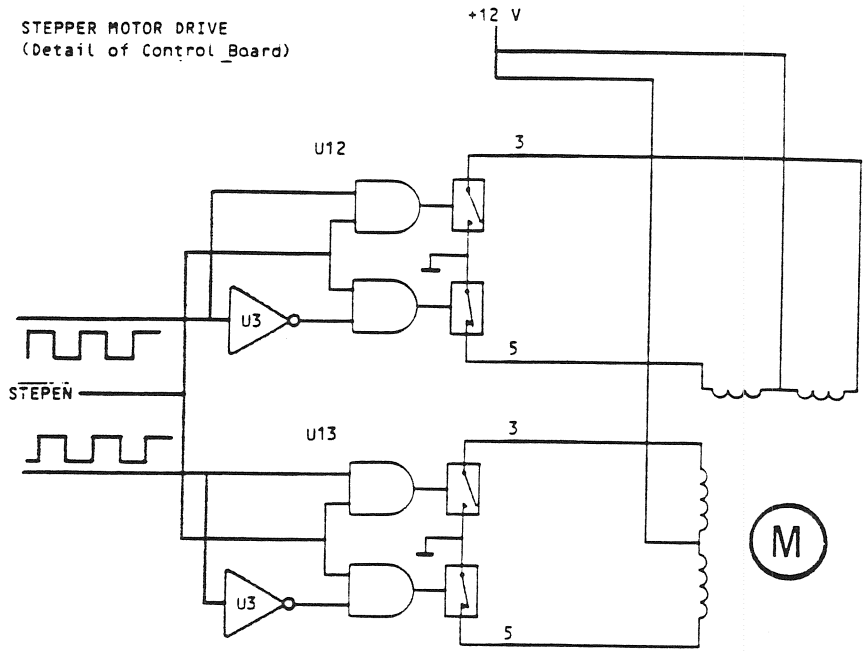
The STEPEN signal from the processor enables the stepper motor dual drivers, U12 and U13 (see detail schematic), and allows the drive signal from the processor to connect the outputs Y1 and Y2 of each driver to ground alternately at the drive pulse rate. The result is that the two halves of each motor winding draws current from the +12 V supply during alternate half cycles of the drive signal.

The drive signals for the two motor windings are in quadrature.

FORMATTER I/O CIRCUITS (Part of)

Convert V.11 input and output signals to and from TTL-levels.

Fold out



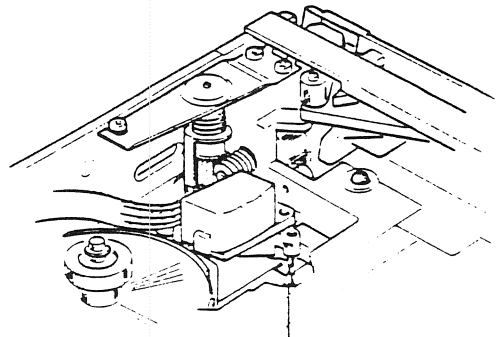
Detail of stepper motor drive.

HEAD SWITCH ADJUSTMENT

Conditions:

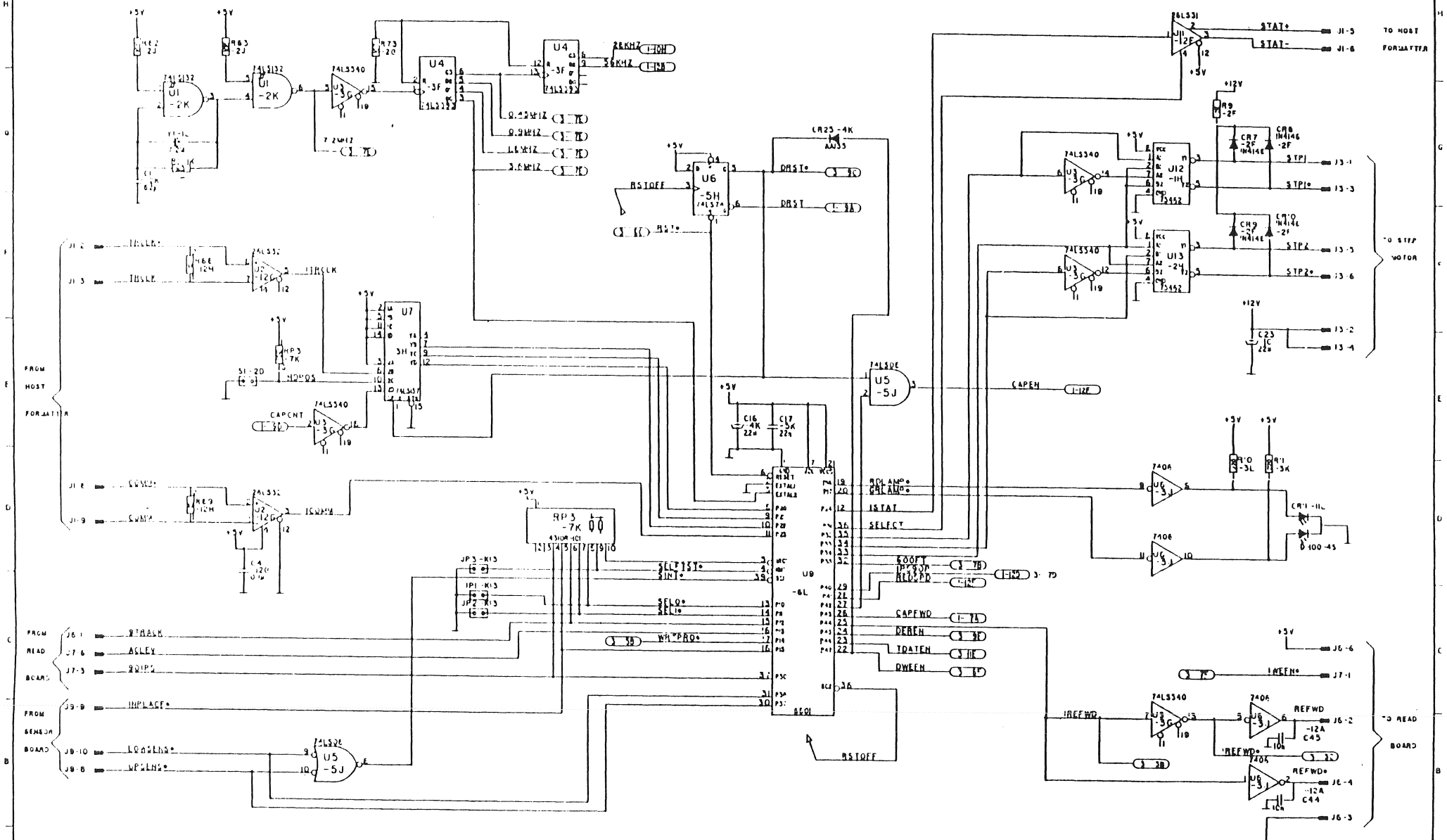
* Not-write-protected tape cartridge inserted
* Jumper JP1 closed
* Jumper JP2 open

Turn the head switch screw counterclockwise until it no longer protrudes above the head platform. Momentarily short-circuit JP3 to start the drive in search for the tape edge. Wait for the front panel light to switch off. Then turn the head switch screw clockwise until the red front panel light just switches on again (be careful not to adjust further clockwise beyond this point).



Head switch set screw.
Use the 1.5 mm Allen key.

NOTE: After completing the adustments, open the door slowly to allow the head to move up to Track 1 position.



PROPRIETARY INFORMATION

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LEGEND:

TOS 3300 SYSTEMS INC.	CONTROL BOARD				
DWG. NO. 8450-0-1-2	10029	3	4	2 OF 3	

Sheet 3

FORMATTER I/O CIRCUITS (Part of)

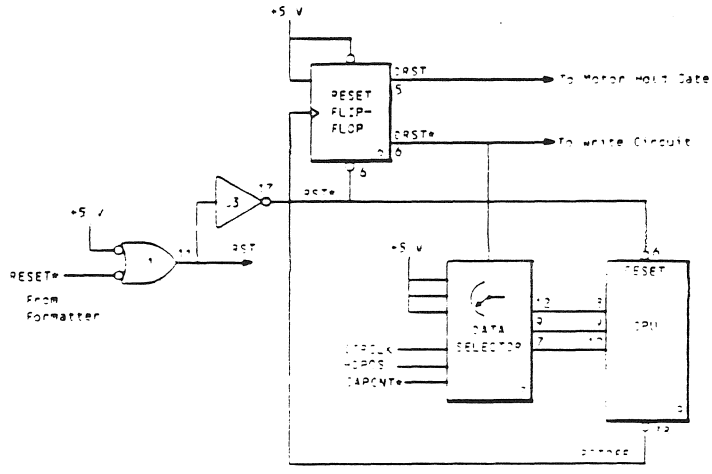
Convert V.11 input and output signals to and from TTL-levels.

RESET CIRCUIT

The reset sequence is initiated by a reset signal, RESET from the host via the Formatter, or by a power-up condition.

In either case the processor U9 and the U6 flip-flop is reset, and its output DRST* will in turn set the data selector U7 so as to apply +5 V to the programming inputs of U9. DRST also goes to the motor hold gate of the Capstan Servo where it prevents tape motion until the power-up or reset condition is over.

When the processor finds the conditions mature for normal operation, it ends the reset sequence by applying RSTOFF to the reset flip-flop, U6.



Simplified detail of Reset Circuit.

WRITE CIRCUIT

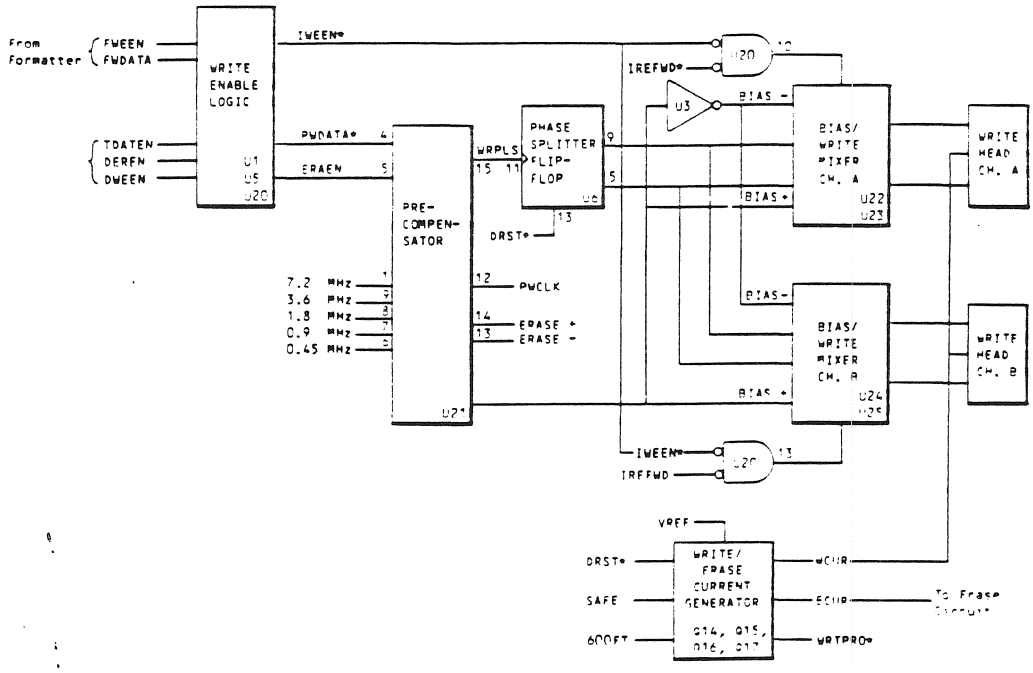
The write/bias current fed to the center tap of the write head is supplied from a gated voltage generator. The write and bias signals are synchronized in the bias/write gates.

The write current is inhibited in reset mode by DRST*, and SAFE from the sensor board inhibits writing if the tape cartridge is set for write protection. The 600-feet signal from the control logic sets the write current in accordance with the tape type present in the recorder.

The effect of the precompensator is to adjust the spacing between the write pulses in order to compensate for pulse crowding. The phase splitter flip-flop, U6, toggles at the write pulse frequency and provides a symmetrical drive signal for the bias/write gates.

The write enable logic controls the passage of write data from the formatter as well as activation of the erase circuit.

Fold out



Simplified detail of Write Circuit.

ERASE CIRCUIT

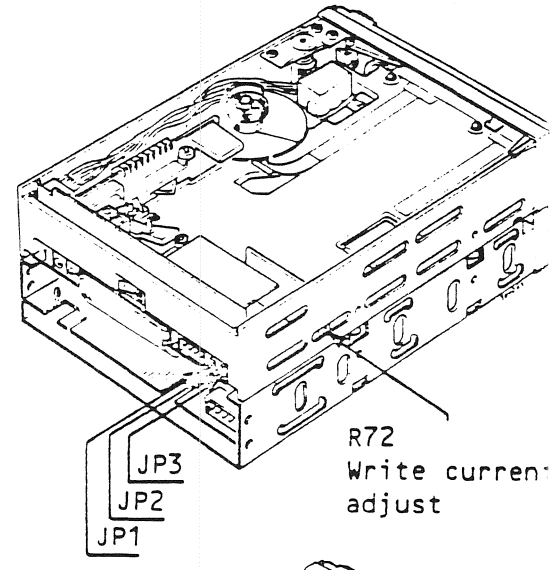
Driven by ERASE+ and ERASE- respectively, transistors Q18 and Q19 switche the erase current which is supplied from Q15. The potentiometer R87 adjusts the symmetry of the circuit.

WRITE CURRENT ADJUSTMENT

Conditions:

* Tape speed correctly adjusted
* Not-write-protected tape cartridge inserted
* Jumper JP1 closed
* Jumper JP2 closed
* DC voltmeter connected to the WCUR line. (Accessible from bottom of control board or on the head connector.)

Momentarily short-circuit JP3 to start the tape, and adjust R72 for 14 V on the WCUR line.

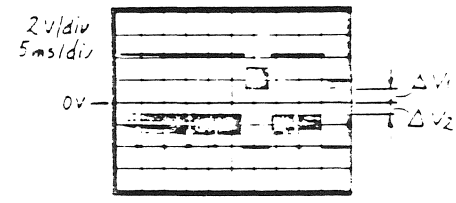


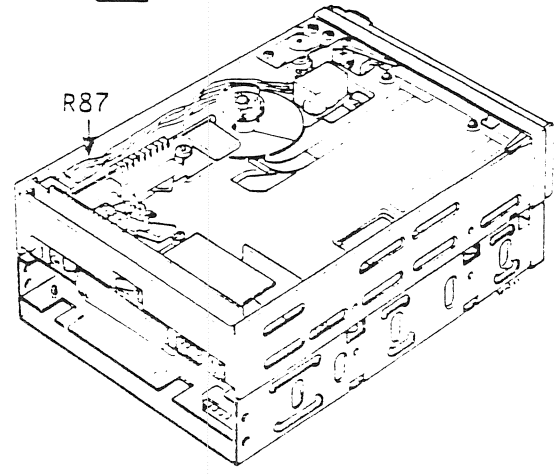
ERASE BALANCE ADJUSTMENT

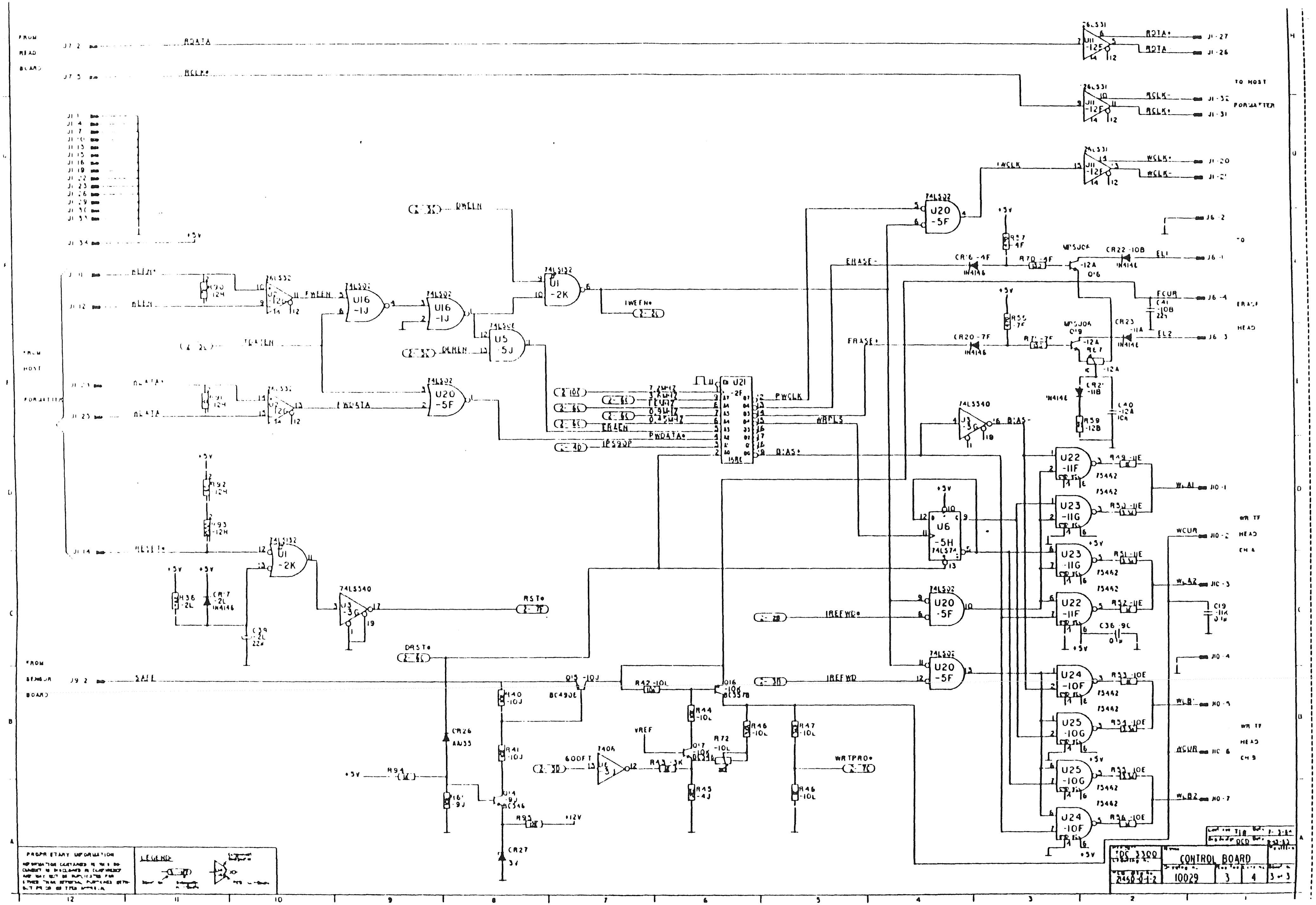
Conditions:

* Not-write-protected tape cartridge inserted
* Oscilloscope connected to TP2-2 and ground.

Set up a write command (60 hex pattern) on track 0 and adjust with R87 until balance is obtained ($\Delta V_1 = \Delta V_2$).



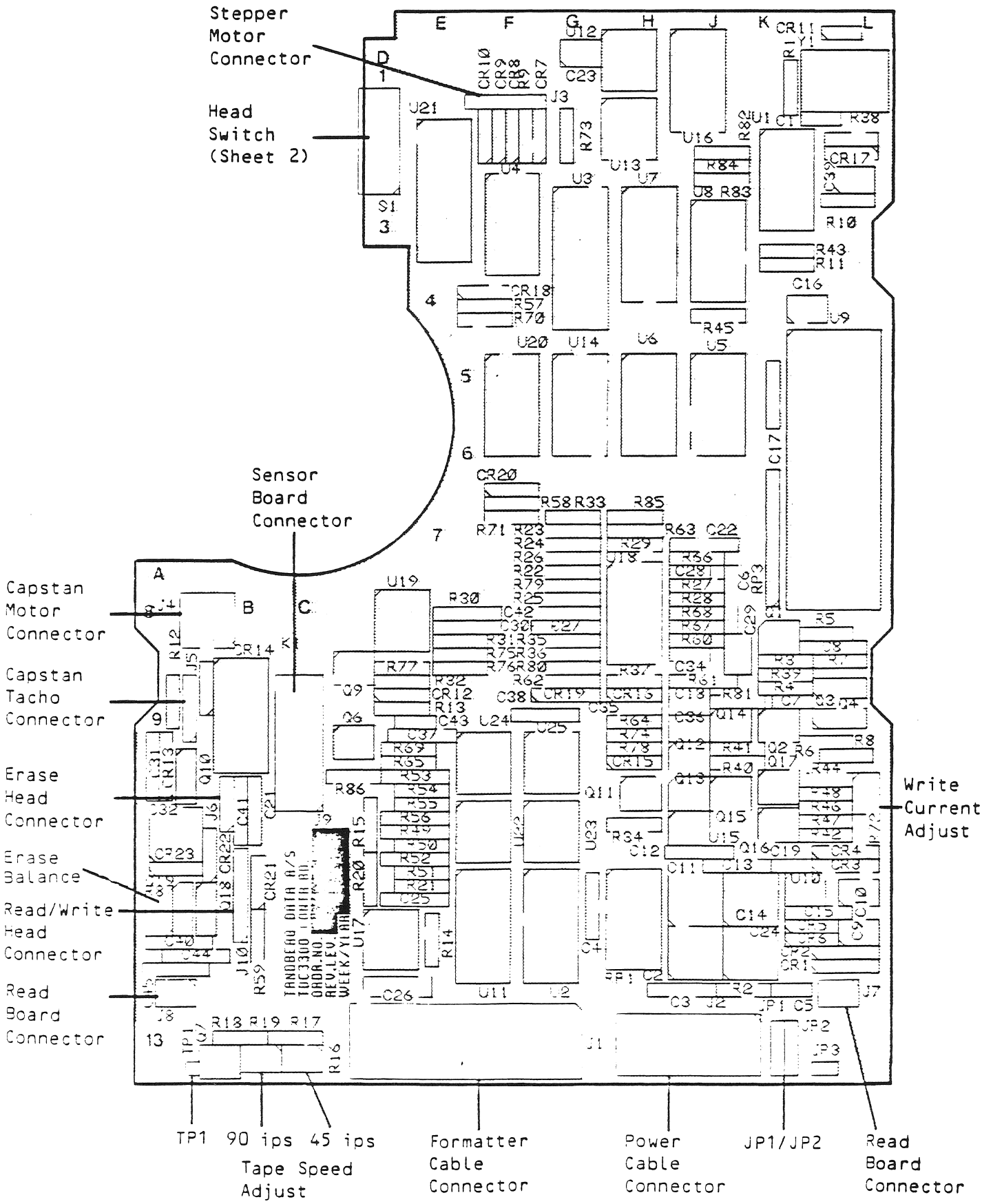




CONTROL BOARD
TDC 3300
10029
FROM HEAD BOARD
FROM HOST FORMATTER
FROM SENSOR BOARD
TO HOST FORMATTER
ERASE HEAD
WRITE HEAD CH A
WRITE HEAD CH B
RDATA
RCLK
RDATA+
RDATA-
RCLK-
RCLK+
WCLK+
WCLK-
IWCLK
PWCLK
ERASE-
ERASE+
WRPLS
BIAS-
BIAS+
IREFWD
IREFWD+
PWDATA+
ERAEN
DRST+
RST+
WRTPRO+
VREF
RESET+
SAFE
LEGEND
PROPRIETARY INFORMATION

4.2 Control Board Component Location

The Control board has revision level 0, and is seen from the component side.



4.3 Control Board Mnemonics List

The mnemonics refer to the scematic diagrams for the Control board. A "*" following a signal denotes the inverted signal.

Fold out

MNEMONIC	FUNCTION
0.45 MHz	0.45 MHz timing signal
0.9 MHz	0.9 MHz timing signal
1.8 MHz	1.8 MHz timing signal
28 kHz	28 kHz timing signal
3.6 MHz	3.6 MHz timing signal
56 Hz	56 Hz timing signal
56 kHz	56 kHz timing signal
7.2 MHz	7.2 MHz timing signal
600Ft	600 feet tape, sets write current for 600 ft. tape
90IPS	Control line, drive operates at 90 ips when active
9TRACK	Control line, tells processor that 9-tr. head is connected
ACLEV	Acceptable level on read channel
BIAS+	Bias positive signal
CAPCNT	Capstan tacho pulse, counts tacho pulses
CAPEN	Capstan enable
CAPFWD	Capstan forward, sets capstan motor direction
COMM+	Command positive line
COMM-	Command negative line
DEREN	Drive erase enable
DRST	Drive restart
DRST*	Drive restart
DWEEN	Drive write enable
ECUR	Erase current
EL1	Erase leg 1, connection for erase head
EL2	Erase leg 2, connection for erase head
ERASE+	Erase positive
ERASE-	Erase negative
FWDATA	Formatter write data
FWEEN	Formatter write/erase-enable
GRLMP*	Green lamp
ICOMM	Internal command line
INPLACE*	Cartridge in place
IPS90P	90 ips controlled from processor
IREFWD	Internal read forwards, enables heads
IREFWD*	Internal read forwards, enables heads
ISTAT	Internal status line
ITRCLK	Internal transmitter clock
IWCLK	Internal write clock
IWEEN*	Internal write/erase-enable
LOWSNS*	Lower sensor
MDIS*	Capstan motor disable
PWCLK	PAL write clock
PWDATA*	PAL write data

MNEMONIC	FUNCTION
RCLK*	Read clock from read board
RCLK+	Read clock, positive to formatter
RCLK-	Read clock, negative to formatter
RDATA	Read data from read board
RDATA+	Read data pos. to formatter
RDATA-	Read data neg. to formatter
RDLAMP*	Red lamp
REDSPD	Reduces speed by 10 %
REFWD	Read forwards
REFWD*	Read forwards
RESET*	Reset
RPLS	Read pulse
RST*	Restart
RSTOFF	Restart off
SAFE	Cartridge write protected
SELECT	Drive selected
SELFTST*	Triggers drive selftests
SEL1*	Drive select 1
SEL0*	Drive select 0
SINT*	Sensor interrupt
STAT+	Status positive to formatter
STAT-	Status negative to formatter
STP1	Stepper motor 1
STP1*	Stepper motor 1
STP2	Stepper motor 2
STP2*	Stepper motor 2
TACKLED	Tachometer led current
TACPLS	Tachometer pulse from capstan motor
TDATEN	Test data enable
TRCLK+	Transfer clock positive, from formatter
TRCLK-	Transfer clock negative, from formatter
UPSENS*	Upper sensor
VREF	+5 V ref. voltage
WCLK+	Write clock positive to formatter
WCLK-	Write clock negative to formatter
WCUR	Write current
WDATA+	Write data positive to formatter
WDATA-	Write data negative to formatter
WEEN+	Write/erase enable, positive
WEEN-	Write/erase enable, negative
WLA1	Write leg A 1, connection for lower write head
WLA2	Write leg A 2, connection for lower write head
WLB1	Write leg B 1, connection for upper write head
WLB2	Write leg B 2, connection for upper write head
WRPLS	Write pulse
WRTPRO*	Write protected cartridge
WRTPRO	Write protected cartridge

4.4 Control Board Parts List

Comp. Designator	Part no.	Description	Qty.
Capacitors			
C1	386386	82 pF cer.1	1
C2, C11, C14, C24, C32	398634	100 uF ELKO +/-20 % RE (F) 35 V	5
C3, C17	359232	0.022 uF MA 105 E 223 MAA	2
C4, C8, C12, C13, C15, C19, C21, C25, C27, C30, C31, C37, C38, C42	393311	0.1 uF SA 205 E 104 MAA	14
C5, C35	382456	1000 pF cer.2 10 % min. 50 V	2
C6	383864	100 pF cer.2 10 % min. 400 V	1
C7	394784	0.1 pF p.est.M 10 % 50 V	1
C9, C10, C16			
C23, C39	381637	22 uF tantalum 16 V	5
C18, C36	392047	0.47 uF p.est.M. 10 % 50 V	2
C22, C40, C44, C45	384999	0.01 uF	4
C26	402618	0.022 uF P.car 5 % 25 V MKC 1862	1
C28	382183	2200 pF cer.2 10 % min. 50 V	1
C29	390467	0.22 uF p.est.M. 10 63 V MKS2	1
C33	383354	0.22 uF CAC4Z5U224M/SA305E224MAA	1
C34	381192	220 pF cer.2 10 % min. 50 V	1
C41	392385	3.3 uF tantalum	1
Diodes			
CR1	400752	1.3 kohm met. film 1 %, 1/8 W	1
CR2, CR13	404756	120 SB 120	2
CR3, CR4, CR5	385107	10 RGP 10J	2
CR6, CR7, CR8, CR9, CR10, CR12, CR14, CR15, CR16, CR17, CR18, CR20, CR21, CR22, CR23	384841	1N 4148	16
CR11	399467	100 D100-4S LED (LD100-5/S)	1
CR19	286560	ZENER 8.2 V	1
CR24	350833	AA 135	1

Comp. Designator	Part no.	Description	Qty.
Circuits			
U1	340640	74LS132	1
U2	389518	26LS32	1
U3	393068	74LS540	1
U4	387700	74LS393	1
U5	381939	74LS08N	1
U6	380229	74LS08N	1
U7	382880	74LS157	1
U8	384604	7406N	1
U10	400956	79L05AC	1
U11	389166	26LS31	1
U12, U13, U22, U23, U24, U25	393233	75462	6
U14, U21	961630	TDC 3300 WR ASE Dec. firmw.	1
U15	394755	78L05ACP	1
U17	393068	76810P	1
U18	401066	MC3403	1
U19	389892	LM311	1
U20	384324	74KS02N	1
Transistors			
Q1, Q6, Q9, Q11, Q12, Q13, Q14, Q17	386436	548 BC 548B RL	8
Q2, Q7, Q8, Q16	389540	557 BC 557B RL	4
Q3	400899	51 MPSW51	1
Q4	402296	1 MPSW01	1
Q10	401290	71 BUZ71A	1
Q15	379066	490 BC490B p RL 80V1A 625MW DATA	1
Q18, Q19	392852	6 MPSU06	2
Assorted			
0300	403338	Spring 62353-3	1
J1	402145	Angled 2x17 pin connector	1
J2	402666	172294-1 4-pins M/172296-1 AMP	1
J3	402043	5268-6	1
J4	402972	5268-2 2-pin	1
J5	404214	5267-05 5-pin	1
J6	402235	5267-04 4-pin	1
J7, J8	391717	826632-3 2 straight rows 2x3 pin	2
J9	402324	163880-8 10-pin connector	1
J10	403265	5267-07 7-pin	1
J11	961607	Socket under S1	1
XRP1	400512	Socket 4E 39500 14-pin	1
JP1, JP2	402744	Jumper C42315-A1347-A102, 2 pol	2
Y1	399338	7.2 MHz NC-18/C series-res.	1
TP1	358894	4 mm metal plint	1
S1	403338	Depress switch	1

Comp. Designator	Part no.	Description	Qty.
Resistors			
R1	400752	1.3 kohm met. film 1 % 1/8 W	1
R5, R6, R57, R58	404198	470 ohm met. 1 %	4
R2, R67	390252	1 Mohm met.film 1 %	2
R3, R4, R13, R20, R21, R25, R26, R29, R31, R32, R36, R39, R40, R41, R42, R44, R63, R64, R65, R74, R75, R77, R78, R79, R80, R81, R82, R83, R85	403188	10 kohm met. film 1 %	29
R87	402153	10 ohm potmeter	1
R7, R8, R22, R24, R43, R48, R66, R76, R84, R86	403127	1 kohm met. film 1 %	10
R9	401457	2 kohm met. film 1 %	1
R10, R11, R14, R62	403579	220 ohm met. film 1 %	4
R12, R30	403864	330 ohm met. film 1 %	2
R15	400447	180 ohm met. film 1 %	1
R16, R19	402165	Pot. meter 10 kohm T7YB	2
R17, R18	400516	20 kohm met. film 1 %	2
R23, R73	400565	100 ohm met. film 1 %	2
R27, R35	401848	47 kohm met. film 1 %	2
R28	403416	270 kohm met. film 1 %	1
R33, R50, R51 R54, R55	403196	3.3 kohm met. film 1 %	5
R34	401738	9.1 kohm met. film 1 %	1
R37, R68, R69	383821	470 kohm met. film 1 %	3
R38	403249	56 kohm met. film 1 %	1
R45	400732	2.2 kohm met. film 1 %	1
R46	400117	4.7 kohm met. film 1 %	1
R47	404361	3.9 kohm met. film 1 %	1
R49, R52, R53, R56	312229	1 kohm met. film 1 %	4
R59	404752	22 ohm met. film 1 %	1
R60	402687	33 kohm met. film 1 %	1
R61	385265	330 kohm met. film 1 %	1
R70, R71	403974	150 ohm met. film 1 %	2
R72	400434	Pot. meter 2.2 kohm TX	1
RP1	401998	100 ohm package DIL 20 %	1
RP2, RP3	388311	10 kohm package 4310R-101-103	1

5. READ BOARD

5.1 Circuit Description

The following describes revision level 0 of the Read board. There are major changes between revison level 0 and revision level 1, most of them in the data detector circuitry. This will be described when the manual is updated.

FILTER AND PREAMPLIFIER

The read head is part of the input filter that precedes the amplifier U1. The filter has a low pass characteristics.

ADJUSTABLE-GAIN AMPLIFIER

The amplifier is common for the two channels, however the gain is individually adjustable for channel A and B to compensate for different characteristics of the two sections of the head.

GAIN CONTROL SWITCHES

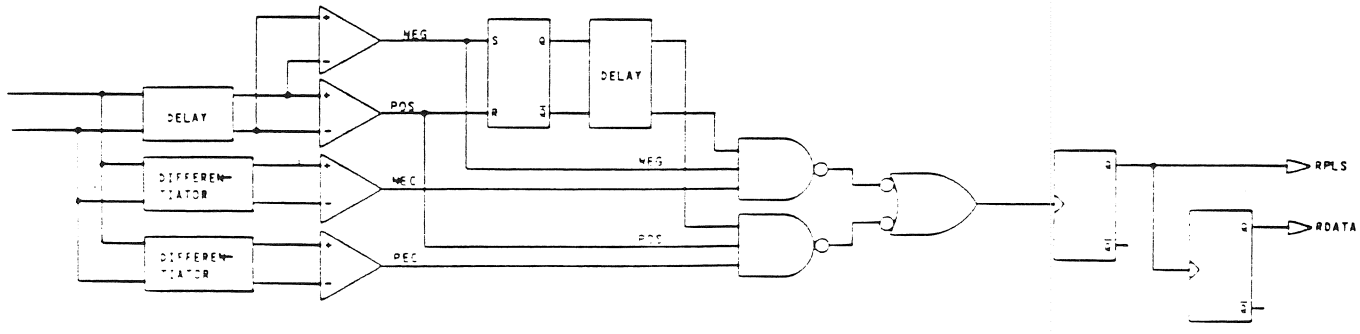
The gain control potentiometers R5 and R6 for channel B and channel A respectively are connected into the circuit via the diodes CR1 and CR2 which are switched by the signals REFWD and REFWD*.

DIFFERENTIATOR

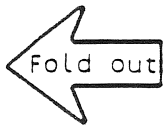
The capacitors C16 and C17 in conjunction with the filter succeeding the Channel selector differentiates the signal and thus transforms the peaks of the signal into zero crossings.

CHANNEL SELECTORS

Channel A is selected when REFWD* switches Q3 and Q4 on. Similarily, channel B is selected by REFWD.



Circuit diagram of Data Detector U2.



DATA DETECTOR (U2)

This circuit is custom made for Tandberg Data. Two comparators at the front end of the circuit detect the zero-crossings of the differentiated read signal. Control signals verify the validity of the resulting pulses which trigger a precision one-shot that generates 550 ns pulses (RPLS). Another one-shot, in series, generates the read data signal (RDATA).

U2 also generates the ACLEV signal that indicates that the level on the read channel is acceptable.

READ CLOCK GENERATOR (U3)

This circuit is custom made for Tandberg Data. It is a phase-locked loop that generates the RCLK* signal that follows the long term variations of the bit rate.

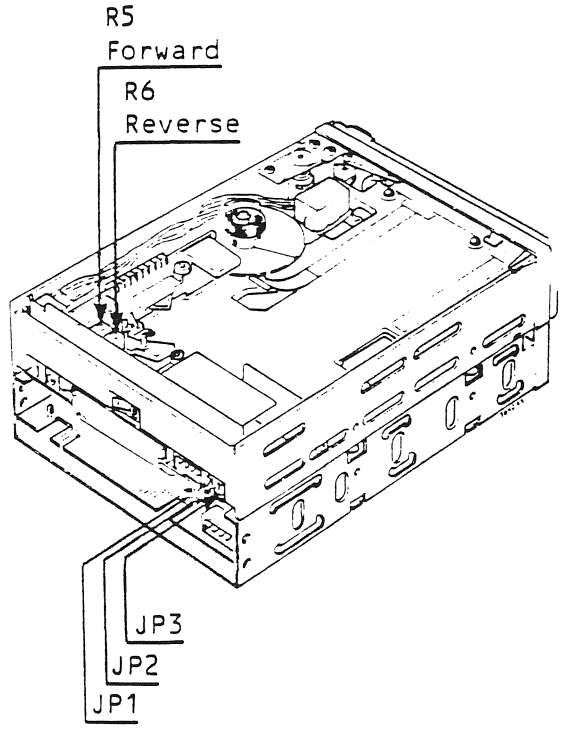
GAIN CONTROL ADJUSTMENT

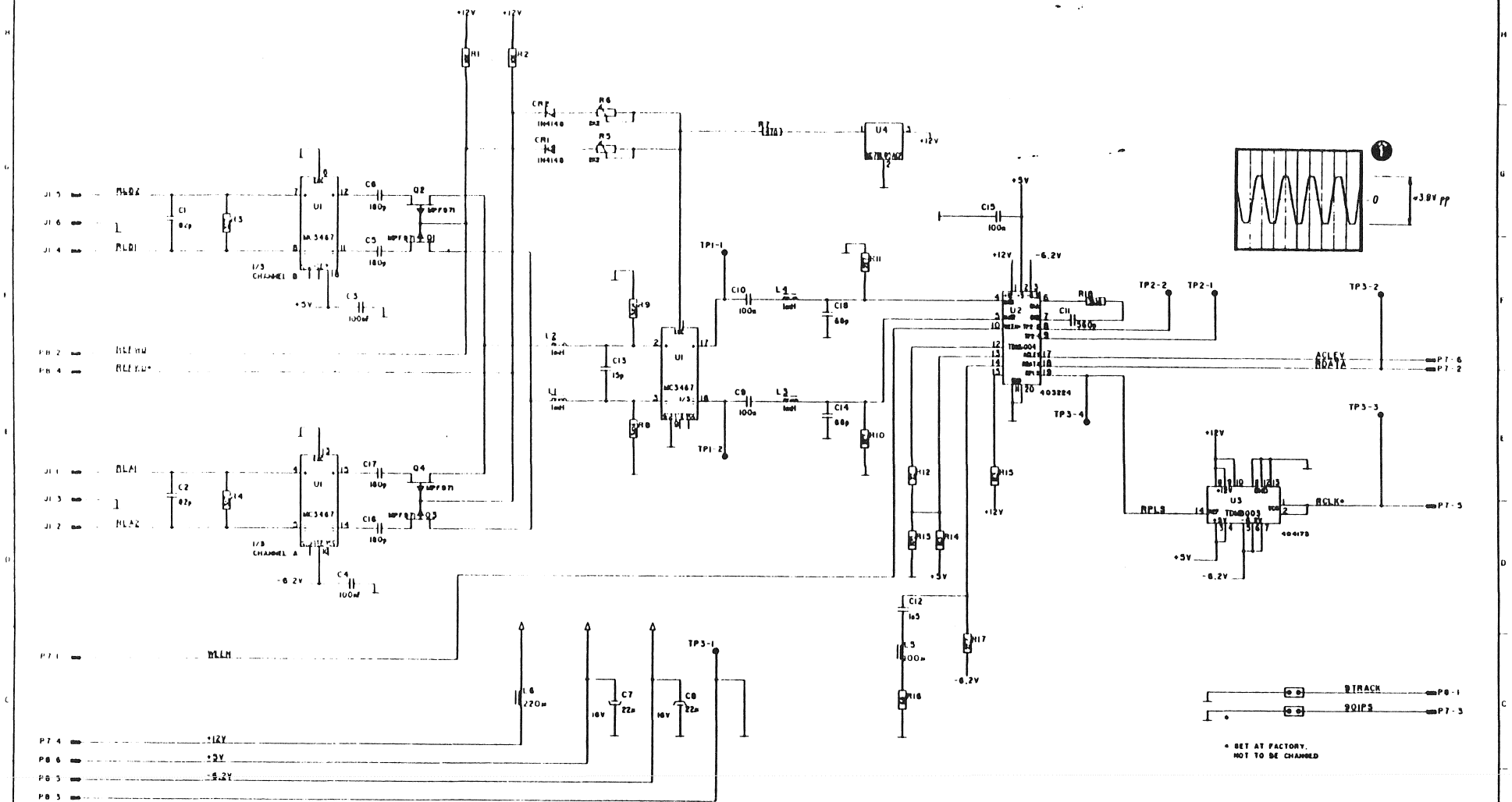
The adjustment potentiometers for gain in channels A and B (forward and reverse), are accessible when the top cover has been removed.

Conditions:

* Tape speed correctly adjusted
* Write current correctly adjusted
* Jumper JP1 closed
* Jumper JP2 closed
* Oscilloscope connected to TP2-1 or TP2-2
* Not-write-protected tape cartridge inserted.

Momentarily short-circuit JP3 to start the adjustment. Adjust R6 for slight clipping of the signal while the tape moves forward (see scope picture 1). Wait for the tape to reverse and adjust R5 similarly.





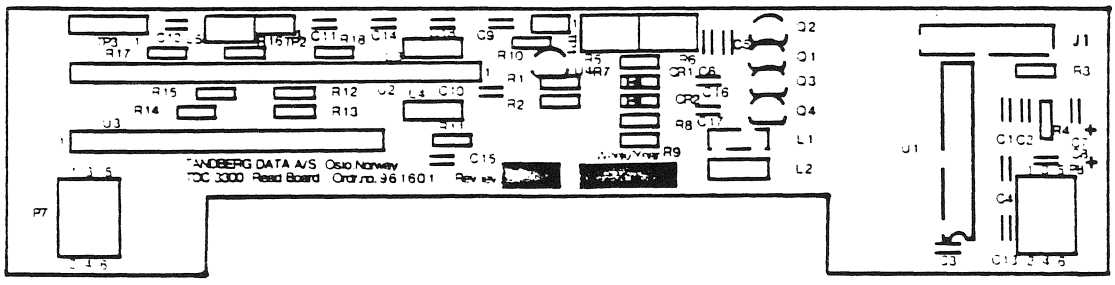
PROPRIETARY INFORMATION

LEGEND:

Last mod: ASK	Date: 9-23-94			
Drawing no. 105 3109	Name: READ BOARD			Position
Wiring no. 961691	Drawing no. 10035	Rev level 0	Corr no. 0	Sheet no. 1 of 1
PCB artwork no. 31329-0				

02

5.2 Read Board Component Location



5.3 Read Board Mnemonics List

The mnemonics refer to the schematic diagram for the Read board.
A "*" following a signal denotes the inverted signal.

MNEMONIC	FUNCTION
90IPS	90 ips control line, drive operates at 90 ips when active
9TRACK	Control line, tells processor that 9-tr. head is connected
ACLEV	Acceptable level on read channel
IWEEN*	Internal write/erase-enable
RCLK*	Read clock
RDATA	Raw read data from read board
REFWD	Read forwards, enables lower heads
RLA1	Read leg A 1 connection for lower head
RLA2	Read leg A 2 connection for lower head
RLB1	Read leg B 1 connection for upper head
RLB2	Read leg B 2 connection for upper head
RPLS	Read pulse

5.4 Read Board Parts List

Comp. Designator	Part no.	Description	Qty.
Capacitors			
C1, C2	386386	82 pF cer.1 2 %	2
C3, C4, C9, C10	393311	0.1 uF SA 205 E 104 MAA	4
C5, C6, C16, C17	288608	180 pF cer.1 2 %	4
C7, C8	381637	22 uF tantalum 16 V	2
C11	382298	560 pF cer.1 2 %	1
C12	380064	1500 pF cer.2 10 % min. 50 V	1
C13	401461	15 pF cer.1 2 %	1
C14	388160	68 pF cer.1 2 % 10 V	1
C15	394784	0.1 uF p.est. M.10 % 50 V	1
Diodes			
CR1, CR2	384841	1N 4148	2
Resistors			
R1, R2	403188	10 kohm met. film 1 %	2
R3, R4	403196	3.3 kohm 1 % 1/8 W	2
R5, R6	400434	Pot.meter 2.2 kohm TX	2
R11, R12, R23	402630	3.16 kohm met.film 1 %	3
R14	404198	470 ohm met. film 1 %	1
R15, R16, R22	403025	2.7 kohm met. film 1 %	3
R17	404752	22 ohm met. film 1 %	1
R18	400565	100 ohm met. film 1 %	1
R19, R20	401294	1.5 kohm met. film 1 %	2
R21	401123	68 ohm met. film 1 %	1
Transistors			
Q1, Q2, Q3, Q4	392874	971 MPF 971	4
Circuits			
U1	400540	MC3467P	1
U2	403224	TDMB004 custom made for TD	1
U3	920047	TDMB003 custom made for TD	1
U4	394755	78L05ACP	1
Assorted			
J1	402235	5267-04 4-pin	1
L1, L2, L3, L4	397082	1000 uH 10 %	4
L5	392960	100 uH 10 %	1
L6	393778	220 uH 10 % Plessey	1
P7, P8	403408	Connectors, 67118-003 2x3-pin	2
TP1, TP3	385503	Test points, 826629-2, 1 row 1x2-pin	2
TP2	390574	Test point, 826629-3, 1 row 1x3-pin	1

6. SENSOR BOARD

6.1 Description and Adjustments

SAFE is true when the tape cartridge in the basic drive is set for write protection (S1 open). Switch S2 confirms the presence of a cartridge in the drive by generating the INPLACE* signal (S2 closed).

Light from the two light emitting diodes CR1 and CR2 activates the corresponding photo transistors Q1 and Q2 when a hole in the tape opens the light path. Q1 will detect a hole in the upper part of the tape and results in UPSENS* being generated. Similary, LOWSNS* is generated when Q2 detects a hole in the lower half of the tape. These signals are analyzed by the processor on the Control board to determine the position of the tape.

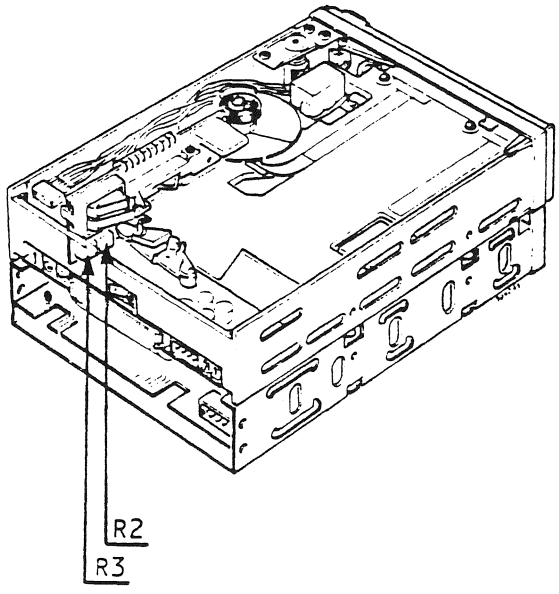
Adjusting Sensor Sensitivity

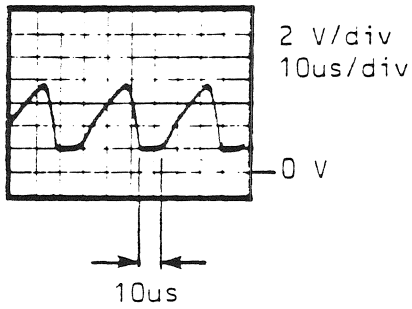
Conditions:

* Cartridge inserted
* Oscilloscope connected to U1 pin 3

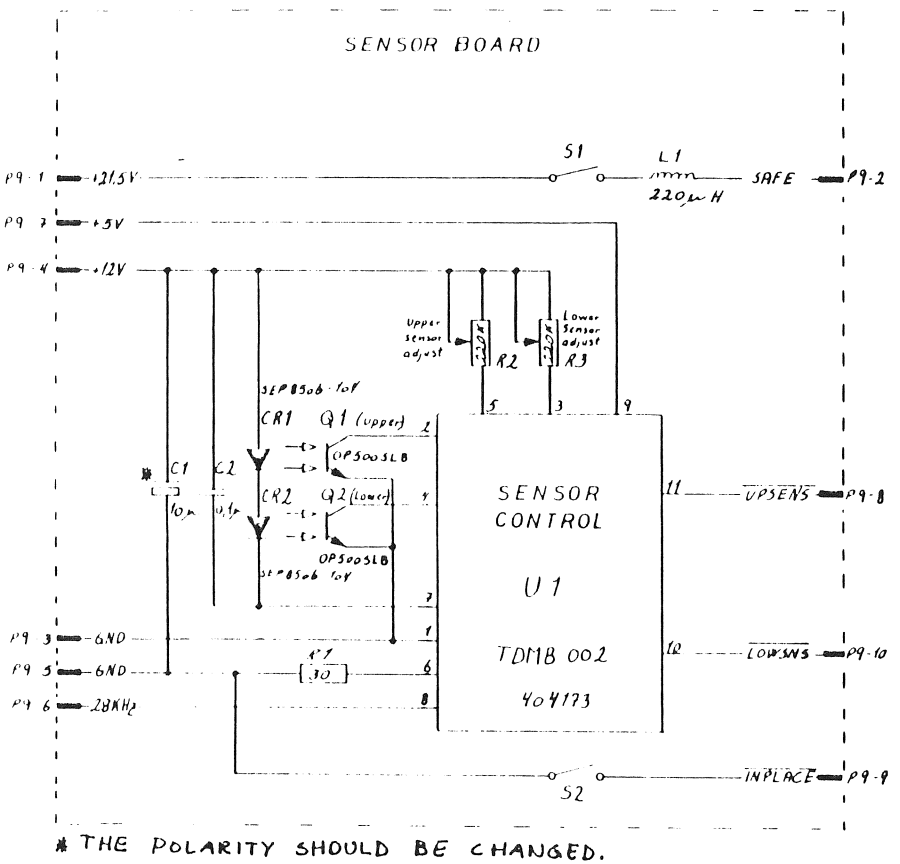
Rewind the tape to BOT. Turn the capstan wheel slowly to align one of the upper holes in the tape with the upper sensor. This corresponds to max signal on the scope. Then adjust R2 to obtain clipping over 10 us of the signal period (see picture).

Move the scope probe to U1 pin 5 and align one of the lower tape holes with the lower sensor (max signal). Use R3 to adjust to 10 us clipping as described above.

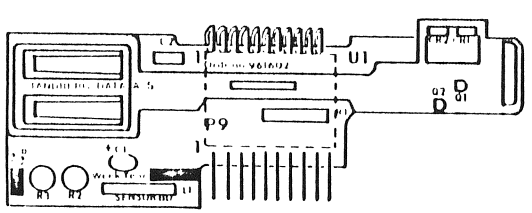




6.2 Schematics



6.3 Component Location



6.4 Mnemonics List

The mnemonics refer to the schematic diagram for the Sensor board.

MNEMONIC	FUNCTION
28KHz	28 kHz timing signal
GND	Ground
INPLACE	Cartridge in place
LOWSNS	Lower sensor
SAFE	Cartridge write protected
UPSENS	Upper sensor

6.5 Parts List

Comp. Designator	Part no.	Description	Qty.
Capacitors			
C1	384489	10 uF tantalum 25 V	1
C2	394784	0.1 uF p.est. MKT 1817/MKS 2	1
Diode			
CR1, CR2	394080	sep 8506-104 IR-LED. side row	1
Resistors			
R1	317249	31.6 ohm met. film 1 %	1
R2, R3	402491	Pot.meter 220 kohm TX 220 K	1
Circuit			
U1	404173	TDMB002 Custom made for TD	1
Assorted			
L1	393778	Coil 220 uH 10 % 11x5mm Q>45	1
P9	401147	163740-8 10-pin	1
Q1, Q2	404841	Transistor 500 or 500 SLB	1
S1, S2	403505	Switches SS-5 GLD	2
0400	402964	PA 6 black plastic bracket	1
0450	402406	Spring, write protect	1

7. FORMATTER BOARD

7.1 Description/Adjustments/Schematic Diagrams

Sheet 1

PARITY CHECKER AND GENERATOR

Checks data and commands from the host for odd parity and generates PERR* when parity error is detected. Sets correct level of parity bit in data and status words to the host.

DTA-TO-HB PORT

Carries data to the host when enabled by DIRS from the Communications Processor.

HB-TO-FD PORT

Carries data from the host to the Data Buffer when enabled by PWDEN* from the I/O-controller in the handshake control during the short time interval when the Formatter Processor makes a jump.

FD-TO-DTA LATCH

Loaded with data from the Data Buffer on the PLDRD* pulse from the I/O-control. The contents of the latch is applied to the DTA-bus while DTEN* from the System Control Latch is present.

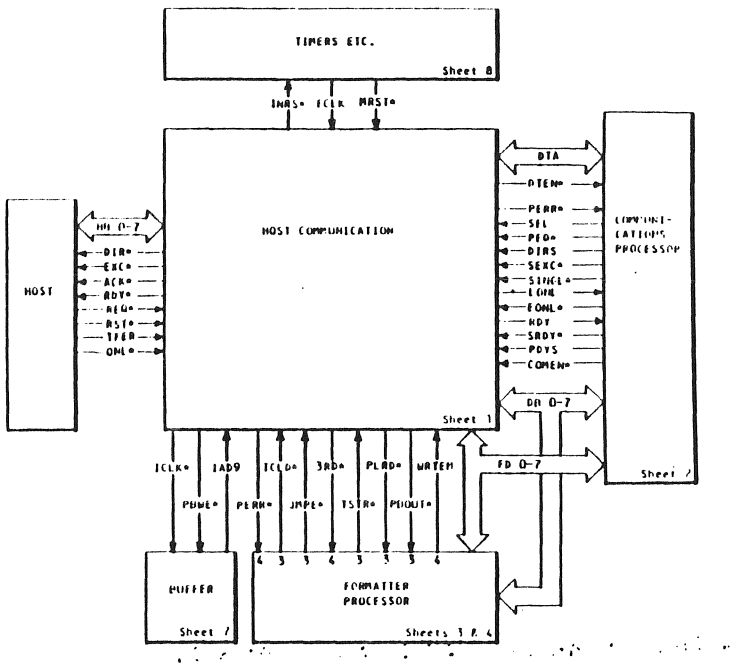
HB-TO-DB PORT

Carries commands from the host to the formatter when enabled by COMEN* from the Communications Processor.

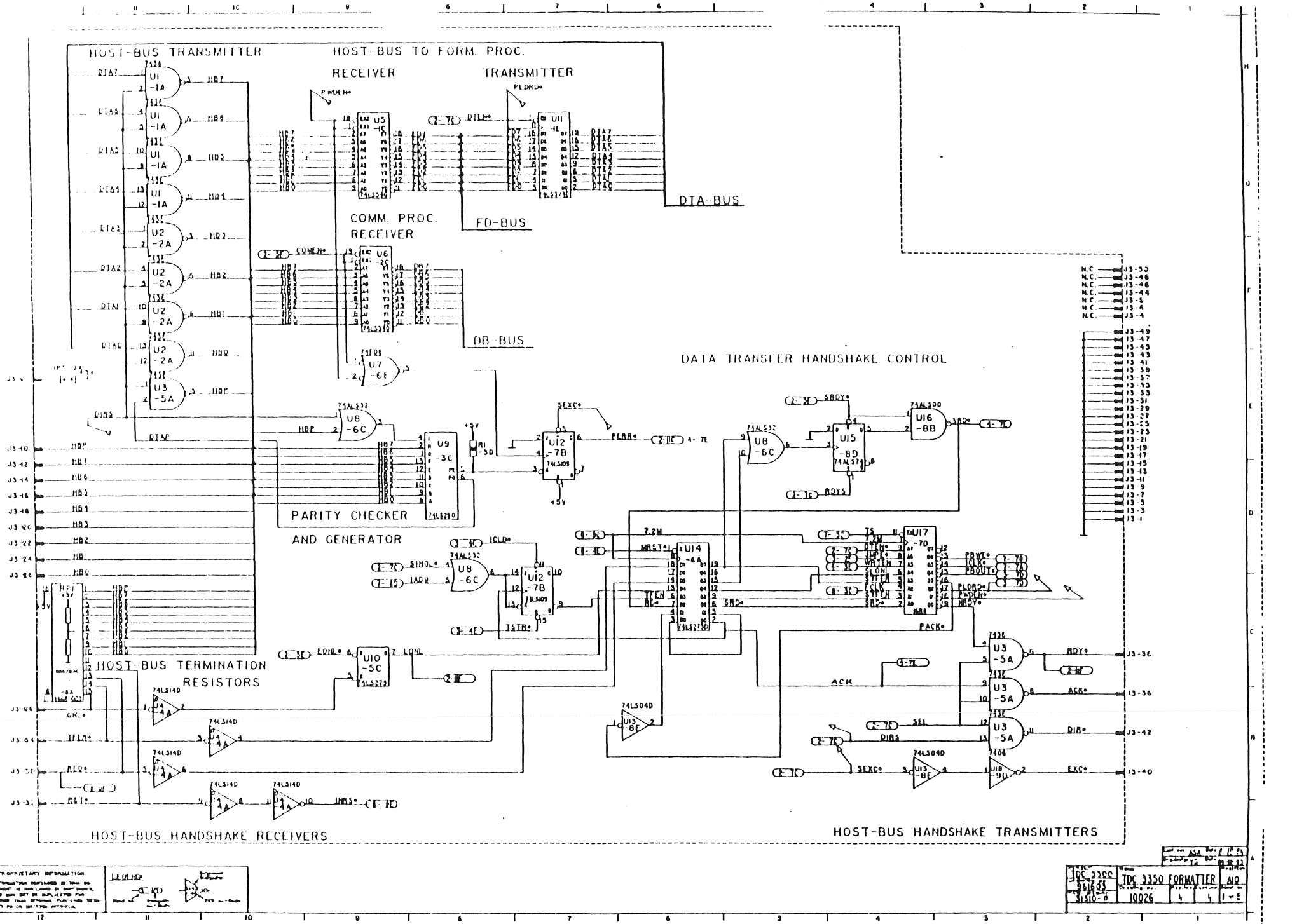
DATA TRANSFER HANDSHAKE CONTROL

Exchanges status signals and commands between the host and the formatter. The signals affect operation of the data buffer, the formatter processor and the Host Communications control.

Fold out



Signal connections between this circuit diagram sheet and other sheets of the Formatter circuit diagram.
Connections to other boards are also shown.


HOST-BUS TRANSMITTER
HOST-BUS TO FORM. PROC.
RECEIVER
TRANSMITTER
DTA-BUS
FD-BUS
COMM. PROC.
RECEIVER
DB-BUS
DATA TRANSFER HANDSHAKE CONTROL
PARITY CHECKER
AND GENERATOR
HOST-BUS TERMINATION
RESISTORS
HOST-BUS HANDSHAKE RECEIVERS
HOST-BUS HANDSHAKE TRANSMITTERS
PROPRIETARY INFORMATION
LEGEND
TDC 3350 FORMATTER
A10

COMMUNICATIONS PROCESSOR

The microprocessor with its internal program memory has an overriding control over all functions of the basic drive and the formatter. This includes:

* Reading and decoding commands from the host via HB-to-DB port.
* Starting or stopping the tape.
* Moving the head to the next track when reversing at BOT.
* Searching for tape edge or reference track at the beginning of a tape.
* Reversing tape motion, and carrying out a re-try operation when a reading error has occurred.
* Keeping track of the the number of blocks and filemarks on the tape and how many times repeated reading and writing has been carried out.

The processor also has communications tasks, such as:

* Loading commands to the Formatter Processor into the DB-to-FD latch.
* Reading the contents of the FD-to-DB latch to obtain status information from the Formatter Processor.
* Unloading the contents of the FD-to-DTA latch into the DTA-bus.

ADDRESS DECODER

Decodes data from the processor to provide the various clock pulses and enabling pulses.

STATUS AND CONFIGURATION LATCH

Via this port the Communications Processor can read:

* The size of the installed buffer circuits (necessary for generation of the correct segment addresses).
* Parity error.

The Port is enabled by CONFEN*

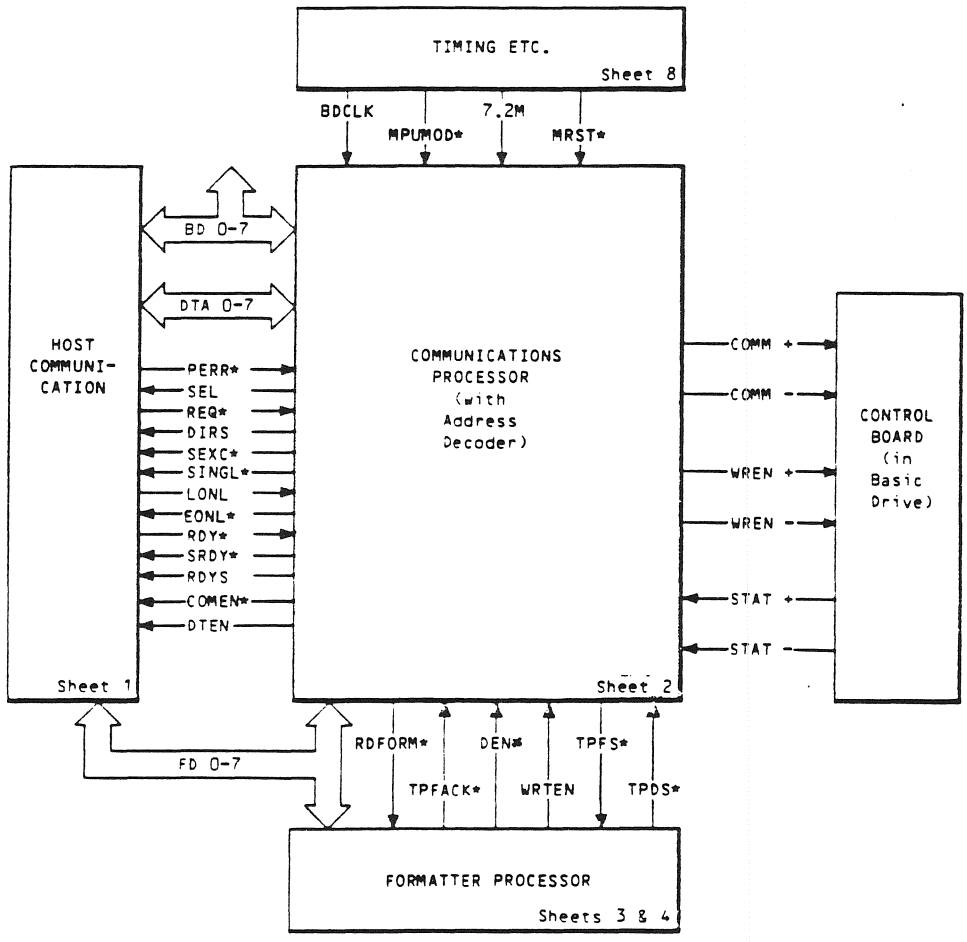
SYSTEM CONTROL LATCH

Stores a system control word issued by the Communications Processor. Each bit in the control word represents one particular system parameter.

DB-TO-FD LATCH

Stores commands from The Communications Processor to the Formatter Processor. The latch is loaded on the WRFORM-pulse from the Address Decoder, and output data is available on the FD-bus during the DEN* pulse from the Formatter Processor.

Fold out



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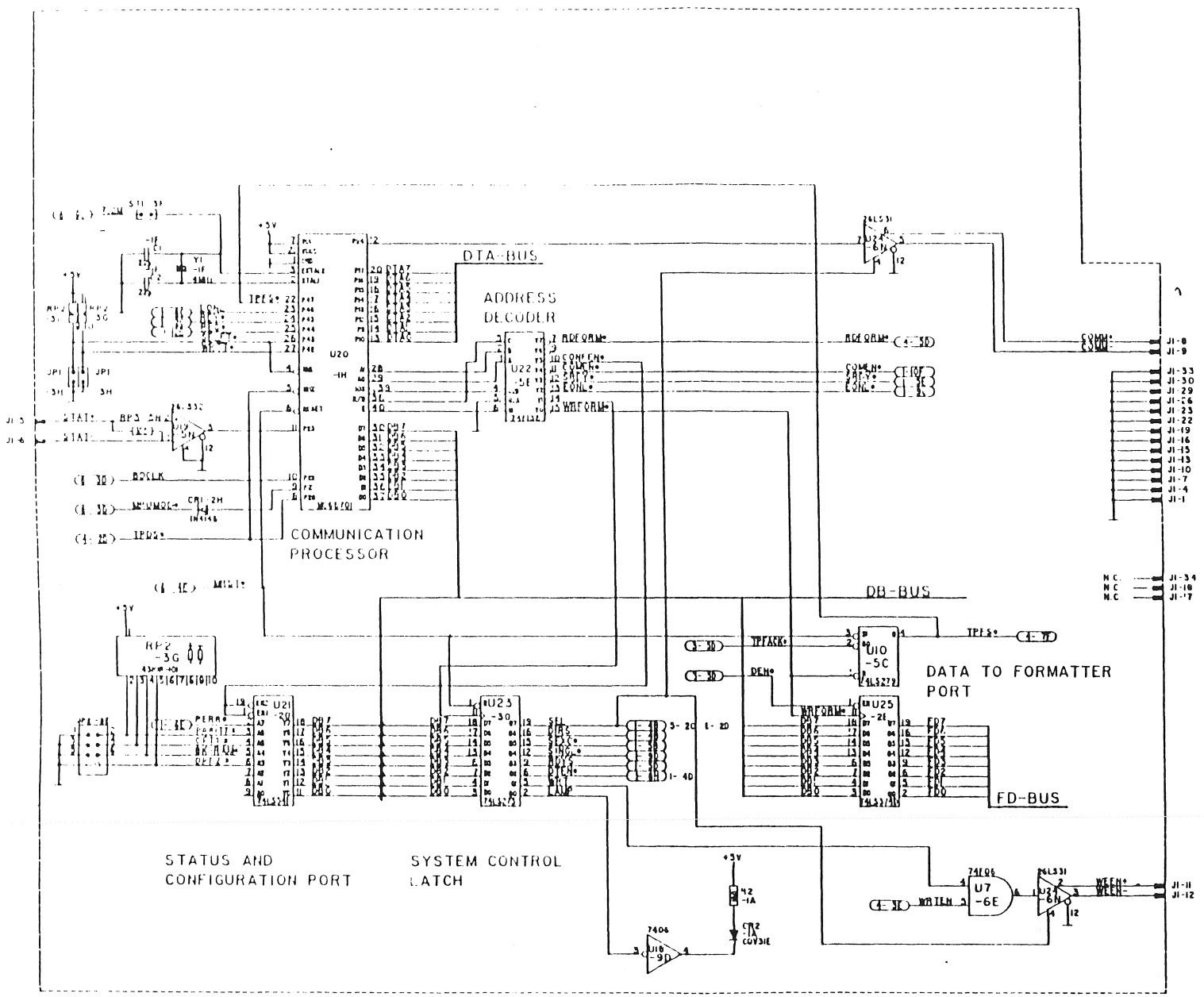


PROPRIETARY INFORMATION

TDC 3300	TDC 3350 FORMATTER	A10			
561602					
1.510-0	10026	4	5	2-8	

FORMATTER PROCESSOR

PROGRAM COUNTER

Loaded from Program Memory and Instruction Latch when a jump instruction is to be executed (PLD* present). Counts up on FCLK pulses between the jump instructions. MPUMOD* initializes the program counter at power-up and reset.

PROGRAM MEMORY

PROM containing the entire program for the Formatter Processor. The address being applied from the program counter selects the instruction to become available at the output.

INSTRUCTION LATCH

Loaded from the Program Memory when IREN* from the Instruction Decoder is present. The latch then holds the instruction for one FCLK period in 1-byte instructions; or until the operand has been transferred in 2-byte instructions.

OPERAND LATCH

Loaded from the program memory. In a 1-byte instruction the operand latch is loaded with the instruction. In a 2-byte instruction it is also loaded during the first FCLK pulse with the instruction (which is not used), but ends up with the operand after the second FCLK pulse.

INSTRUCTION DECODERS

Each instruction word stored in the instruction latch will activate one or more of the output lines from the decoders depending on the operation to be carried out.

DATA BUS BUFFER

Connects the output of the Operand Latch to the FD-bus when required.

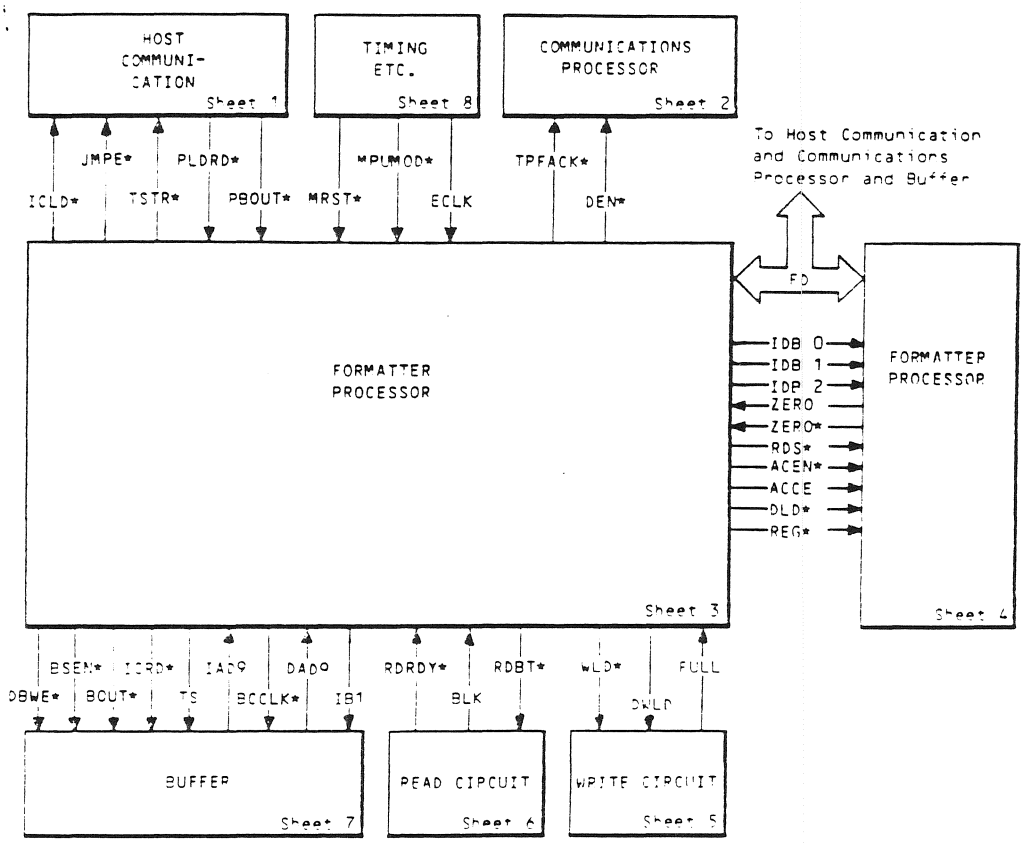
SCRATCH-PAD RAM

Temporary storage for variables and system parameters used by the formatter processor.

Fold out

JUMP SELECTOR

Generates PLD* which initiates loading of the Program counter when a jump instruction is to be executed. The jump condition is determined by the instruction bits IB4-IB6. JMPE* enables the selector. While the jump instruction is carried out the FD-bus is not occupied by the formatter processor and can therefore be used for data transmissions between data buffer and host.



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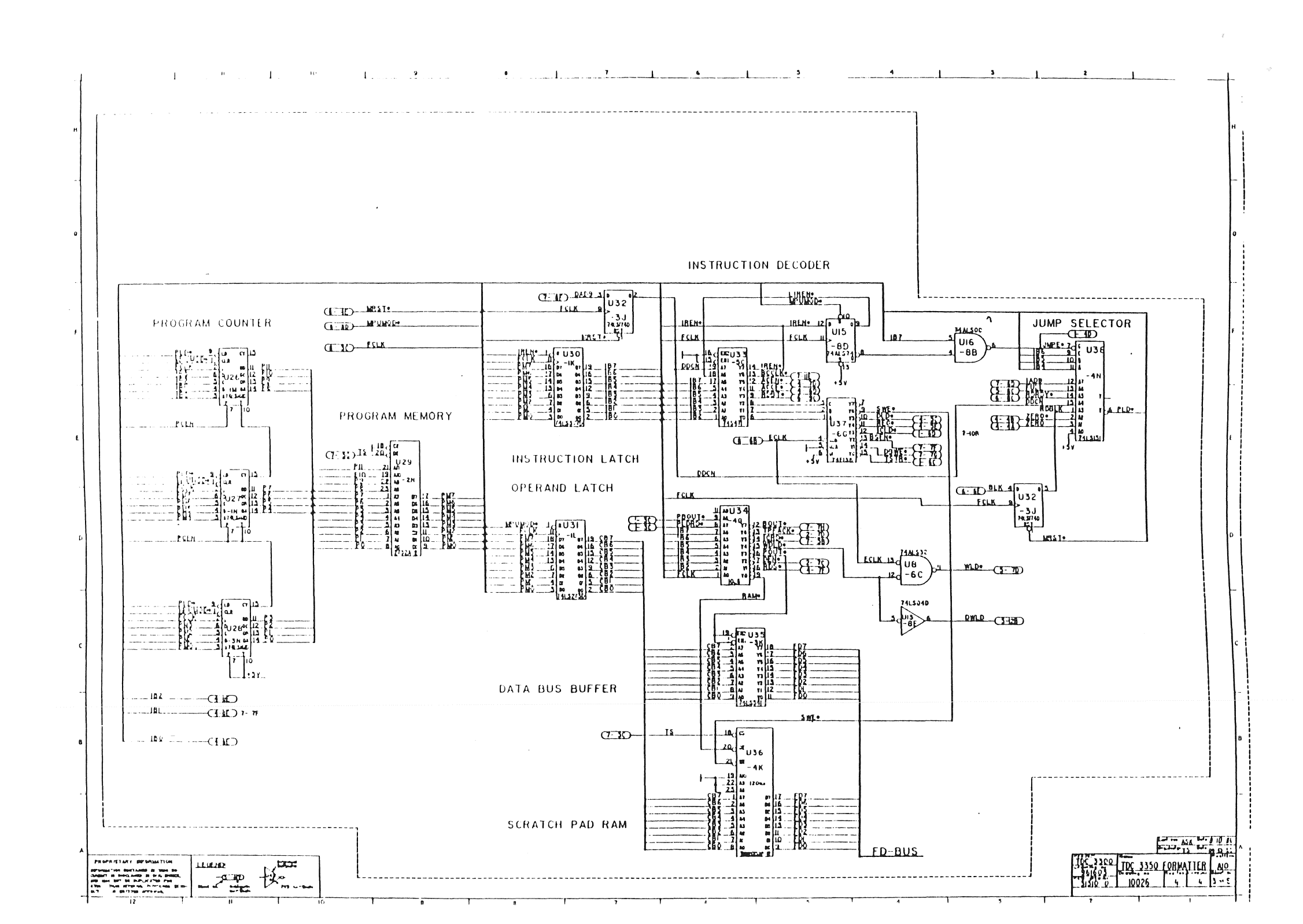

INSTRUCTION DECODER
PROGRAM COUNTER
PROGRAM MEMORY
INSTRUCTION LATCH
OPERAND LATCH
JUMP SELECTOR
DATA BUS BUFFER
SCRATCH PAD RAM
FD-BUS
TDC 3350 FORMATTER

Sheet 4

ARITHMETIC/LOGIC UNIT

Performs arithmetic and logic operations on data from the FDB bus and from the accumulator output. The result is presented to the accumulator input. The operation to be carried out is determined by IB0-IB2 from the Instruction latch.

ACCUMULATOR

Stores the result from the arithmetic/logic unit.

ACCUMULATOR BUFFER

The tristate outputs of these line drivers are enabled by ACEN* from the instruction decoder (sheet 3). Data in the Accumulator Buffer can be distributed to the following circuits:

- Data Buffer (Sheet 7)
- Block Address Selector (Sheet 7)
- External Address Counter (Sheet 7)
- Scratch Pad RAM (Sheet 3)
- FD-to-DB Latch (Sheet 4)
- System Control Latch (Sheet 2)
- Write FIFO (Sheet 5)

SYSTEM STATUS PORT

Applies system status parameters to the FD bus when the tristate outputs are enabled by RDS* from the Instruction Decoder (sheet3).

SYSTEM CONTROL LATCH

Generates system control signals based on data picked up from the FD-bus when REG* is present.

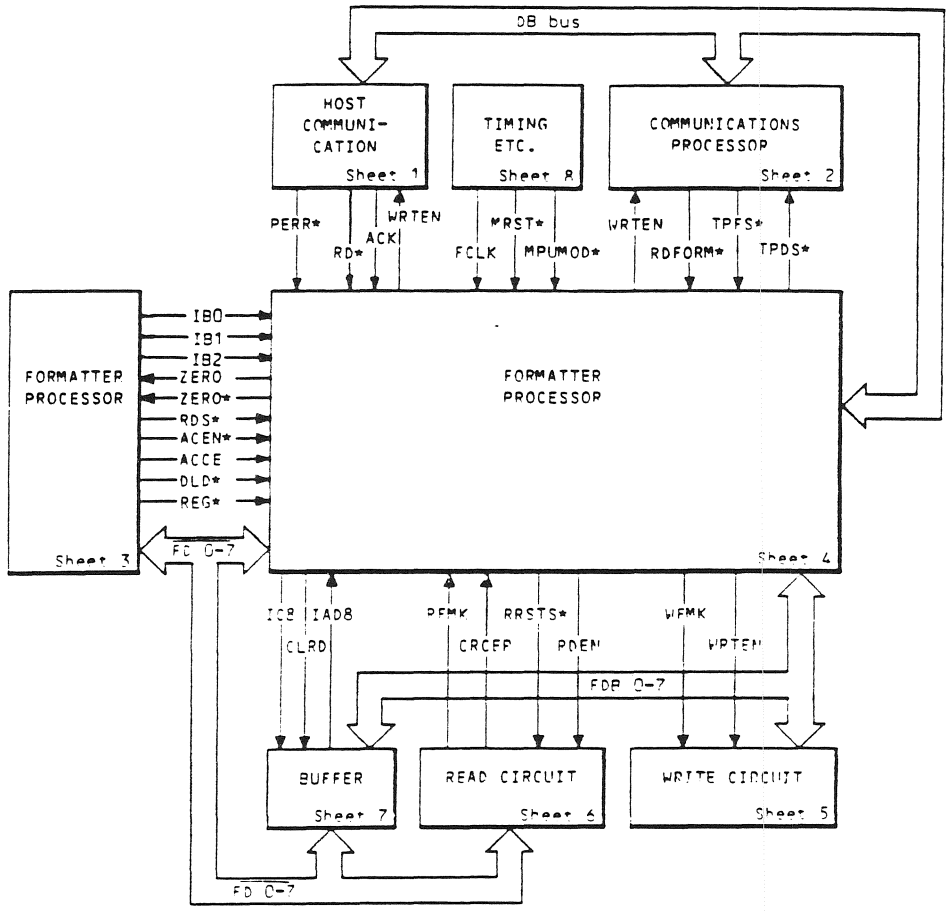
FD-TO-DB LATCH

Status signals for the Communication Processor is loaded into the latch from the FD-bus while DLD* is present. The tristate outputs apply the stored information to the DB-bus during RDFORM*.

ZERO DETECTOR

Provides two of the input signals (ZERO and ZERO*) to the Jump Selector when the accumulator output is zero.

Fold out



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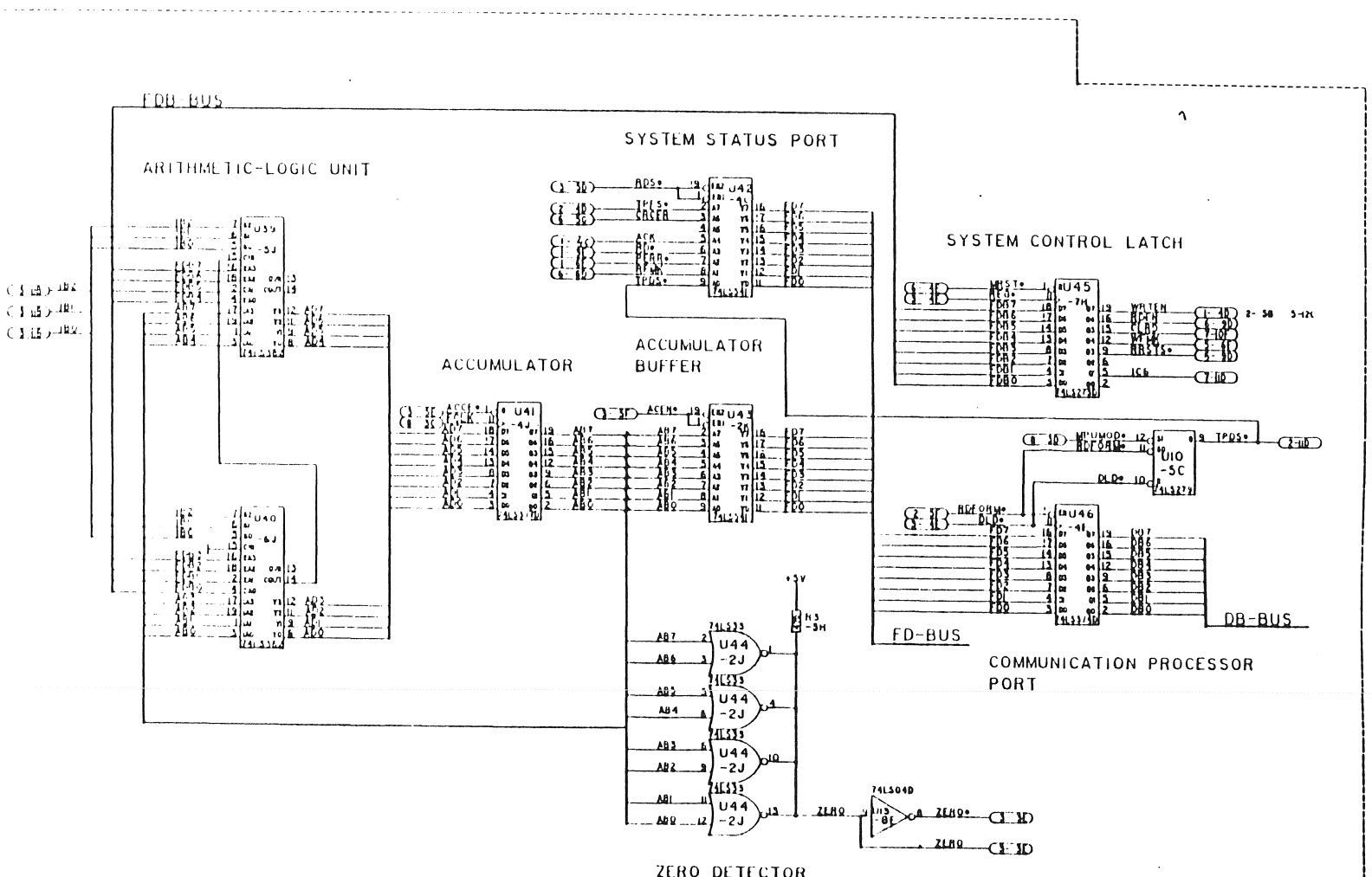

FDB BUS
ARITHMETIC-LOGIC UNIT
SYSTEM STATUS PORT
SYSTEM CONTROL LATCH
ACCUMULATOR
ACCUMULATOR BUFFER
FD-BUS
DB-BUS
COMMUNICATION PROCESSOR PORT
ZERO DETECTOR

WRITE CIRCUIT

The write operation includes the following phases as determined by WM0 and WM1 from the Write Data Sequencer:

* Generation of the preamble. Takes place in the write data controller until the write FIFO is full (while WM0=0 and WM1=0).

* Generation of the marker (1 byte). Takes place in the write data controller when WM0=1 and WM1=0.

* Conversion of the 512 data bytes and the block address into 5-bit serial GRC code. Takes place in the Write Data Controller when WM0=1 and WM1=1.

* Generation of the CRC character, which takes place in the CRC generator throughout the whole data field, and block address and subsequently converting it into 5-bit serial GRC code (takes place in the write data controller when WM0=0 and WM1=1).

* Generation of the postamble. Takes place in the write data controller when WM=0 and WM1=0 (high density mode).

The durations of preamble, data field and postamble are controlled by the FormatterProcessor.

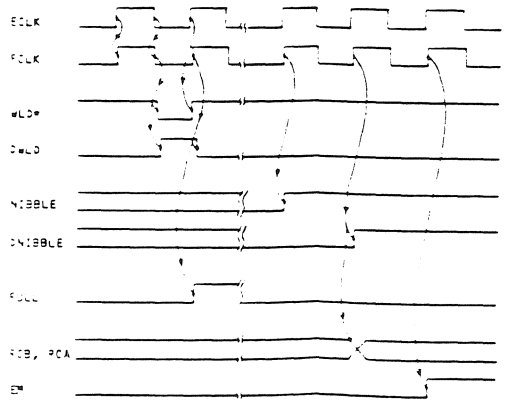
WRITE FIFO CONTROLLER

Generates:

* Read and write addresses for the Write FIFO.

* FIFO FULL signal which makes the Write Data Sequencer leave the high density mode.

* FIFO empty (EM) which makes the sequencer enter CRC mode.
  The FIFO controller is enabled by WRTEN from the Formatter Processor, whereas DWLD clocks the write address counter.



Write FIFO Controller timing.

Fold out

WRITE FIFO

Data from the FD bus can be written into either one of the four FIFO locations as determined by the write address while the WLD* pulse is present.

Reading out from the FIFO is controlled by the read address bits RCA and RCB, and takes place in two consecutive 4-bit nibbles. The MSN * or the LSN* enabling pulse from the Write Data sequencer selects the most significant or the least significant nibble.

WRITE DATA SEQUENCER

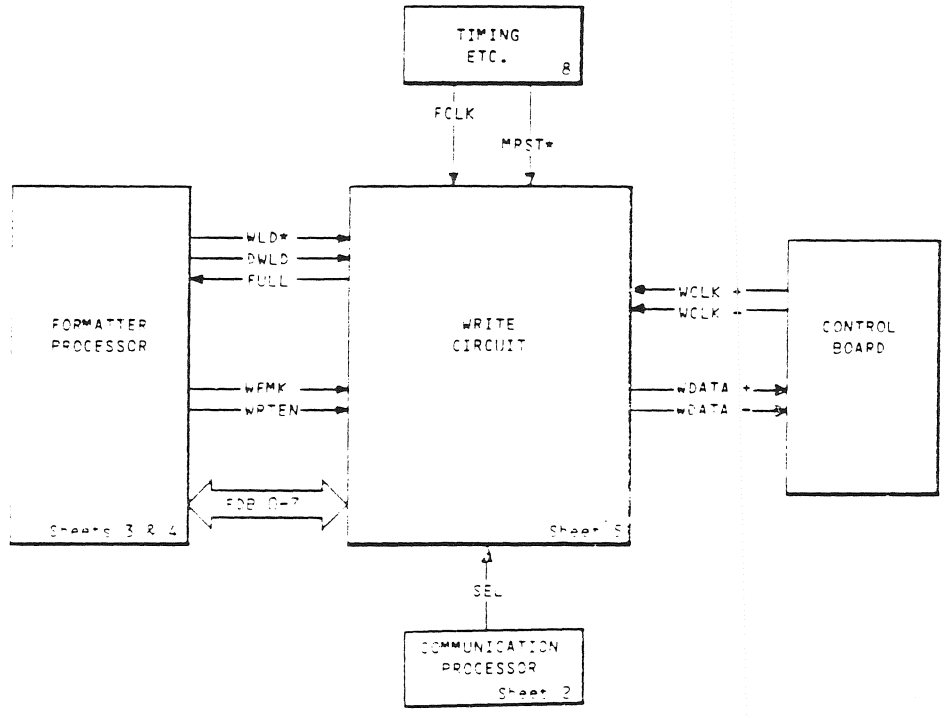
Interacts very closely with the Write Data Controller in the various phases of the write operation described above. WCLKS determines the bit rate of the serialized data signal from the Write Data Controller whereas WCLKS controls the nibble operation. Status signals from the FIFO Controller(EM and FULL) change the mode of operation.

WRITE DATA CONTROLLER

Performs the conversion of 4-bit nibbles into serial 5-bit GRC code in interaction with the Write Data Sequencer.

WRITE CLOCK SYNCHRONIZER

Locks the WCLK signal from the Control Board to the FCLK to generate the WCLKS pulses.



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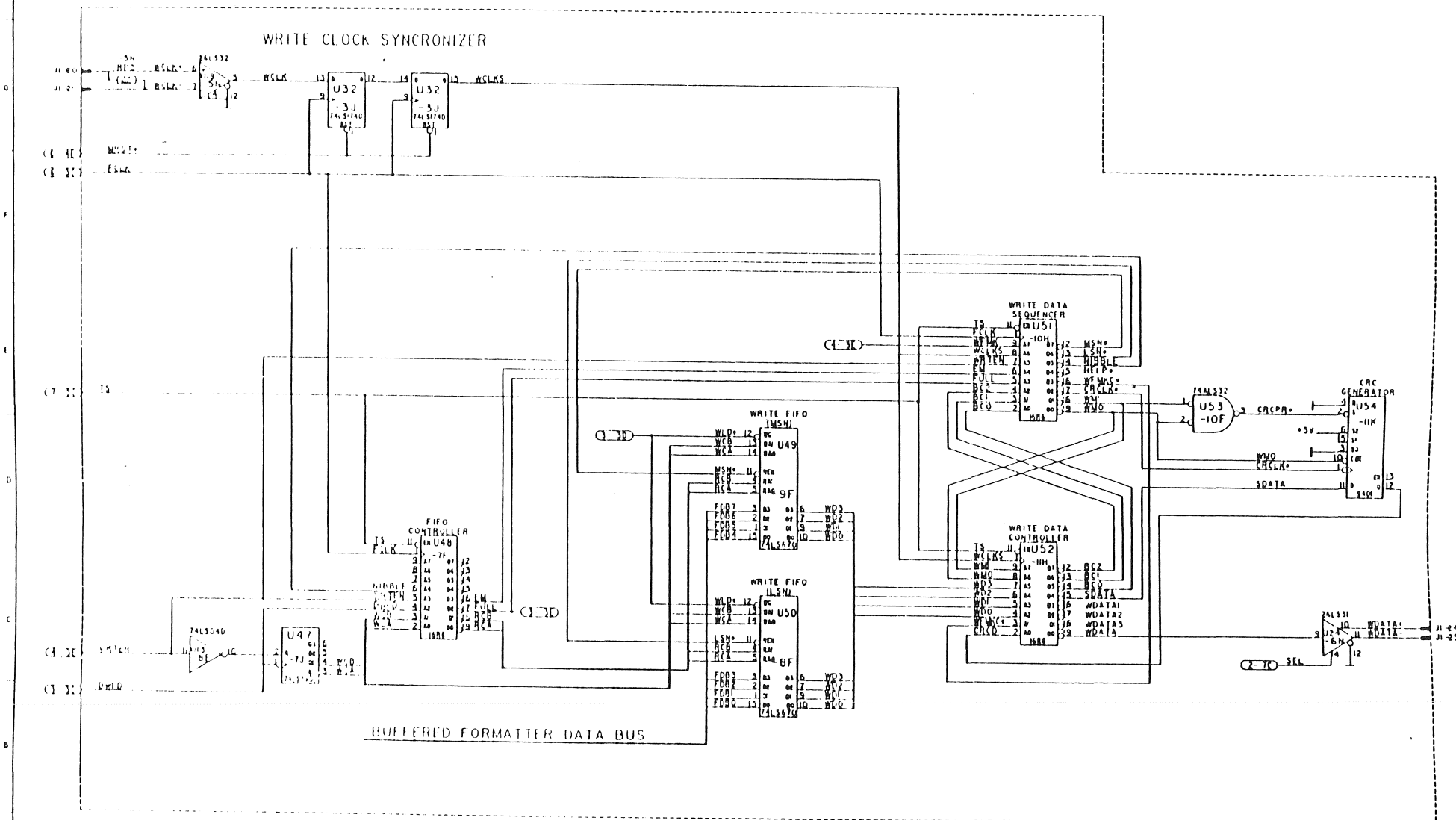

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READ CIRCUITS

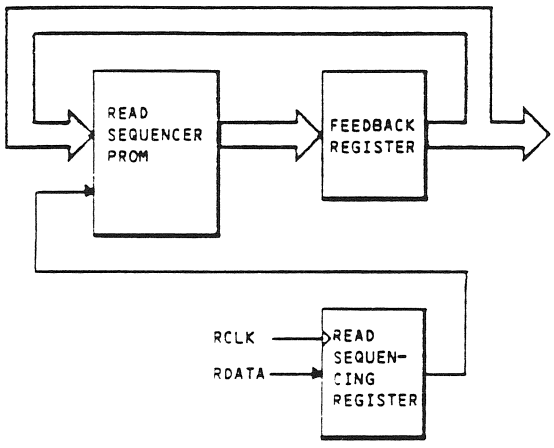
The read operation includes the following phases:

* Examination of the serial bit stream (RDATA) from the Read Board in the Basic Drive in search for the preamble and the block marker.

* After detection of the block marker, reduction of the 5-bit GRC coded data into 4-bit nibbles.

* Conversion of the nibbles into 8-bit words which are forwarded to the Formatter Processor on parallel form.

READ DATA SYNCHRONIZER AND CODE CONVERTER



Simplified diagram of Read Data Synchronizer and Code Converter.

GCR-coded RDATA is clocked into the Read Sequencing Register by RCLK, and appears at the DI output which represents one of the address bits for the Read Sequencer PROM. Each received data bit will thus represent one of two possible memory locations depending on whether the bit is a "one or a zero". The content of the accessed location is fed back via the Feedback Register and forms a new address along with the next bit on the DI-line.

Accordingly, a specific route through the memory will correspond to one particular DI bit pattern. It may help comprehension to think of the Read Sequencer PROM as a maze where you will reach a given destination only by taking the appropriate path at every diversion.

The operation of this circuit in search for specific bit patterns (preamble,block marker,etc), and for code conversion is explained in the following:

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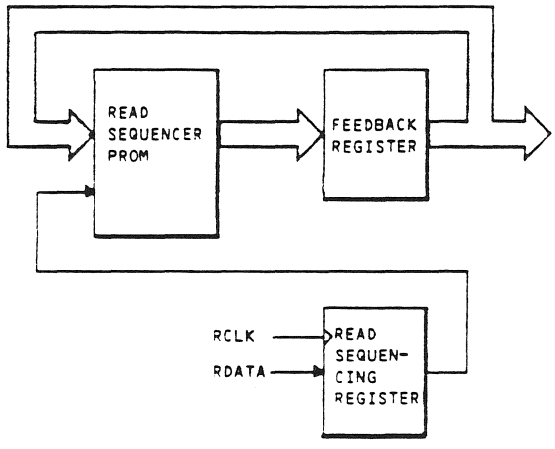

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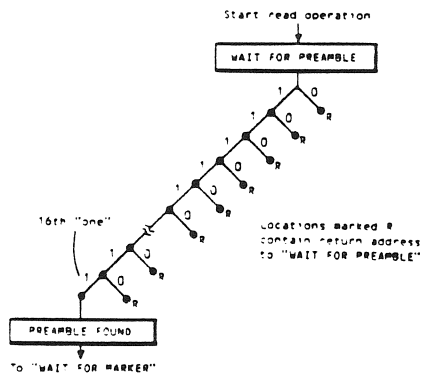
Fold out

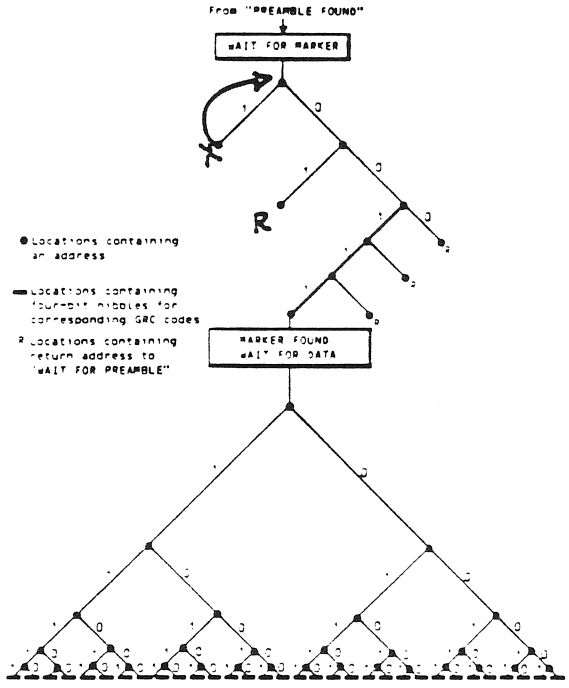


Path through the Read Sequencer PROM when searching for preamble in the DI bit stream.

Search for Preamble

Before the preamble arrives, DI from the Sequencing Register and the Feedback Register outputs are all zeroes.

As the first bit appears on the DI-line, a new memory location will be accessed in which the next address is stored. This address is fed back via the Feedback Register to the Read Sequencer PROM along with the bit on the DI line. The 16th DI pulse in a continuous string of "ones" will access the location which confirms that the preamble has been detected. Any departure from the string of 16 consecutive"ones" will return the sequencer to the starting point, and will require a subsequent string of 16 "ones".



Path through the Read Sequencer PROM when searching for block marker and when converting GCR codes to binary nibbles.

Search for Marker, and Conversion of GRC Codes

From the location representing preamble detection a search will now start for the block marker being represented by another location accessible only through an error-f reception of the marker bit pattern.

Similarly follows now a sequence for each received GRC code which always ends up in the location containing the binary nibble for the GRC code in question.

The nibbles are applied to the Read FIFO being enabled by LDFIF* from the Sequencing register.

DI bit for the next address in the pattern recognition or code conversion sequence. The final location in the code conversion sequence also contains the binary nibble for the code in question.

READ FIFO

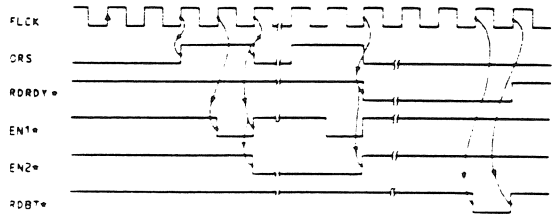
Loaded with binary nibble from the Feedback Register during the LDFIF* pulse. Unloaded into the FIFO Buffer under control of EN1* from FIFO Control.

FIFO BUFFER

Under control of EN1* and EN2* from the FIFO Control the nibbles from the Read FIFO are alternately loaded into the two buffer circuits; one reserved for the least significant nibble, the other for the most significant nibble. Two nibbles are then applied to the FD-bus as a complete byte under control of RDBT* from the Formatter Processor.

FIFO CONTROL

When data is available at the FIFO output (ORS), the FIFO Control generates the EN1* signal which unloads the FIFO into the FIFO Buffer which is simultaneously enabled by EN2 or EN2*, depending on whether it is the first (MSB) or the last nibble (LSB) in the byte. On the first FCLK pulse after both nibbles have been loaded, RDRDY is sent to the Formatter Processor. When the Formatter Processor has set up another RDBT, another loading of the FIFO Buffer will occur whenever data is available in the FIFO.



Typical read/write sequence.

CRC CHECKER

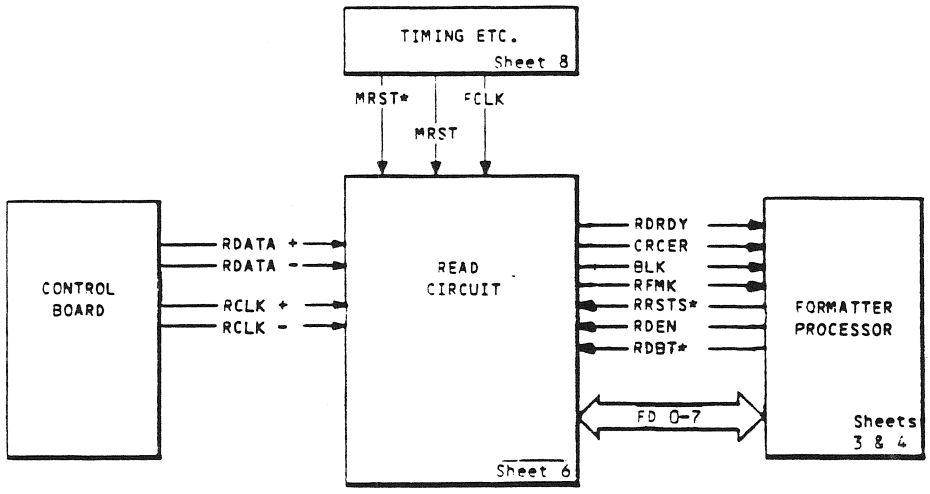
Continuously monitors the bit pattern of each nibble and accumulates the sum, which should be zero at the end of the block. If not, the CRCER signal is generated.

FEEDBACK REGISTER

Flip-flop register clocked by RCLKD* (corresponding to the trailing edge of RCLK). Serves as temporary storage for adresses read out from the Read Sequencer PROM, and for data to be loaded into the FIFO.

SEQUENCING REGISTER

Clocked by RCLK, this register serves as temporary storage for RDATA which is subsequently forwarded as DI to the Read Sequencer PROM coincidently with data from the Feedback Register. The Sequencing Register also stores the flag bit BLK which arrives from The Read Data Seqencer at end of the block.



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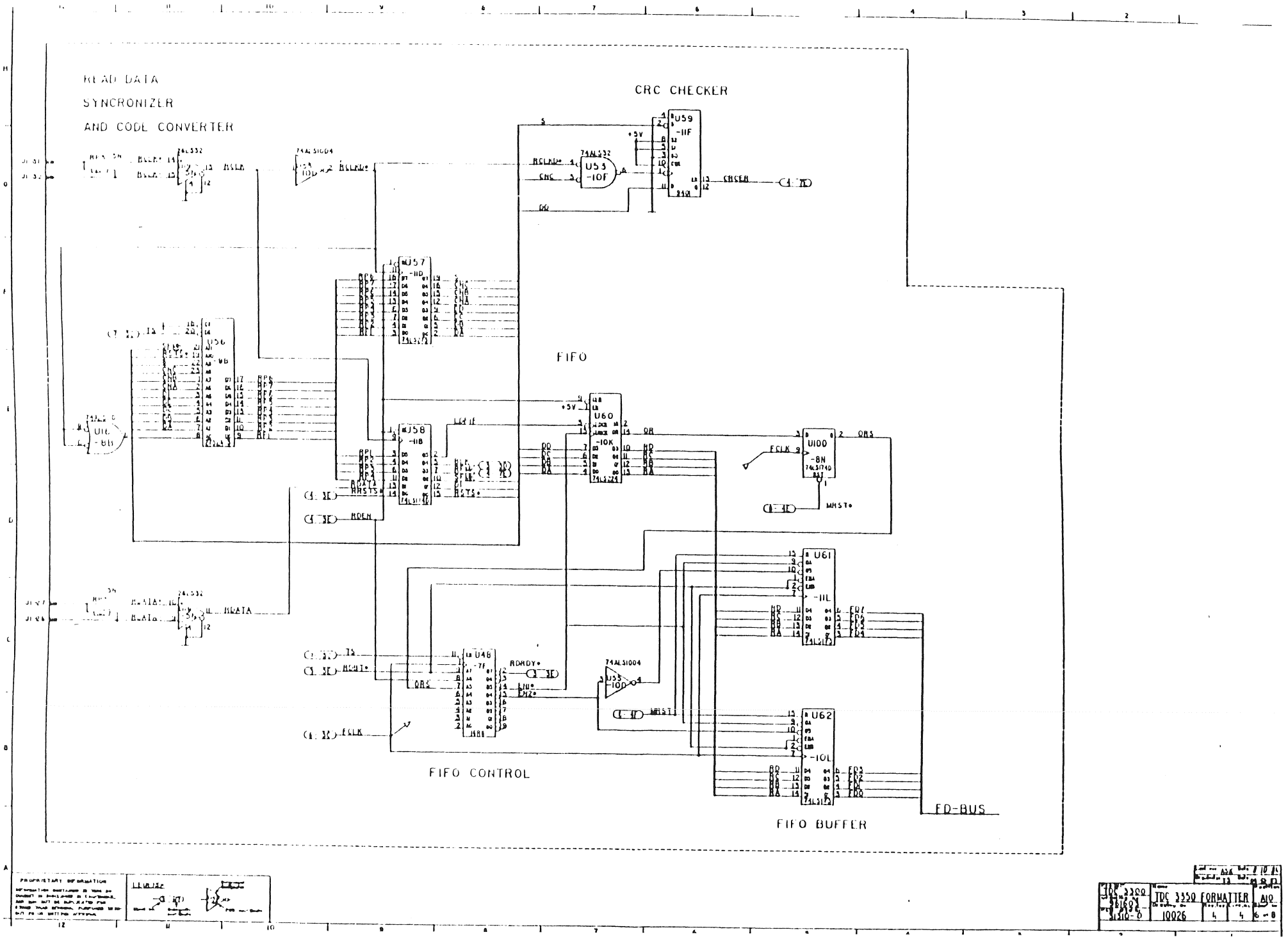

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BUFFER ADDRESSING

The complete address required for reading out of and writing into the data buffer consists of the block address (segment address) which determines the 512 byte wide section of the buffer (one data block); and the byte address which defines the location within the particular buffer section. The byte address consists of 9 bits from the internal or external address counter. Correspondingly, the internal and external segment addresses consist of five bits from the formatter processor.

BYTE ADDRESS SELECTOR

Selects the internal address for data from buffer to write circuits, or for data from read circuits to buffer. For data to or from the host, the ICLK* pulse switches the selector over to the external address.

BLOCK ADDRESS SELECTOR

The internal and external block addresses (segment addresses) set up by the Formatter Processor are loaded into the selector from the FDB-bus. For internal data handling the internal address is selected. However, for data to and from the host (while ICLK* pulse is present), the external address is applied to the address bus.

INTERNAL ADDRESS COUNTER

Generates the 9 least significant bits of the address used for loading data into the buffer from the read circuits, or for unloading data from the buffer to the write circuits. The counter is reset to zero at the beginning of every block, and is incremented at each BCCLK* pulse which coincide with the formatter system clock pulses (FCLK).

EXTERNAL ADDRESS COUNTER

Generates the 9 least significant bits of the address used for transferring data to the buffer from the host, or vice versa. The address is obtained by loading the counter with zero from the Formatter Processor at the beginning of the block and then counting to 511.

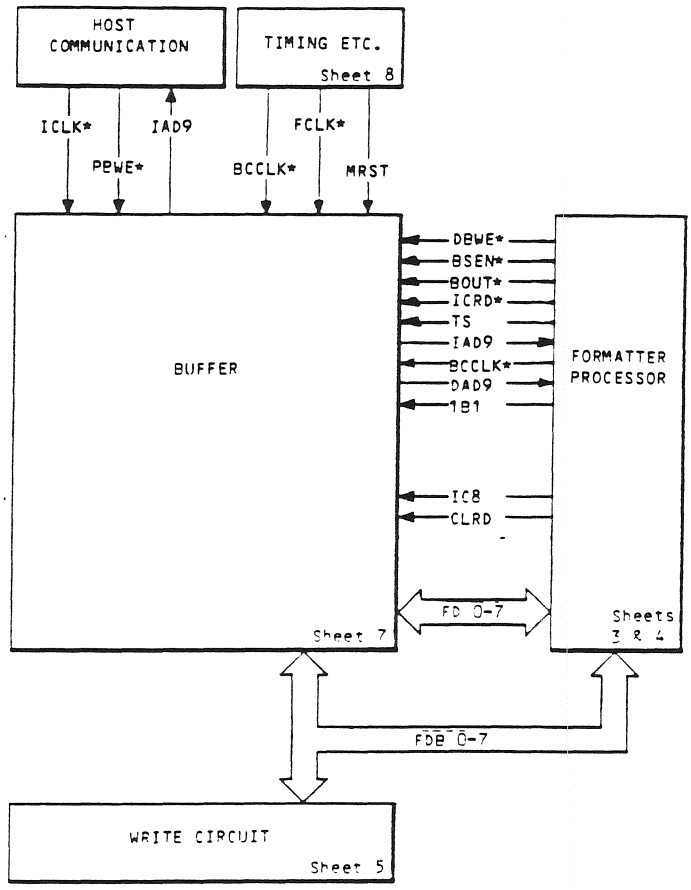
READ ADDRESS PORT

Allows the Formatter Processor to read the output of the external address counters. The port is enabled by ICRD* from the Formatter Processor.

BUFFER PORT

Connects the FD-bus to the FDB-bus. The port is permanently enabled.

Fold out



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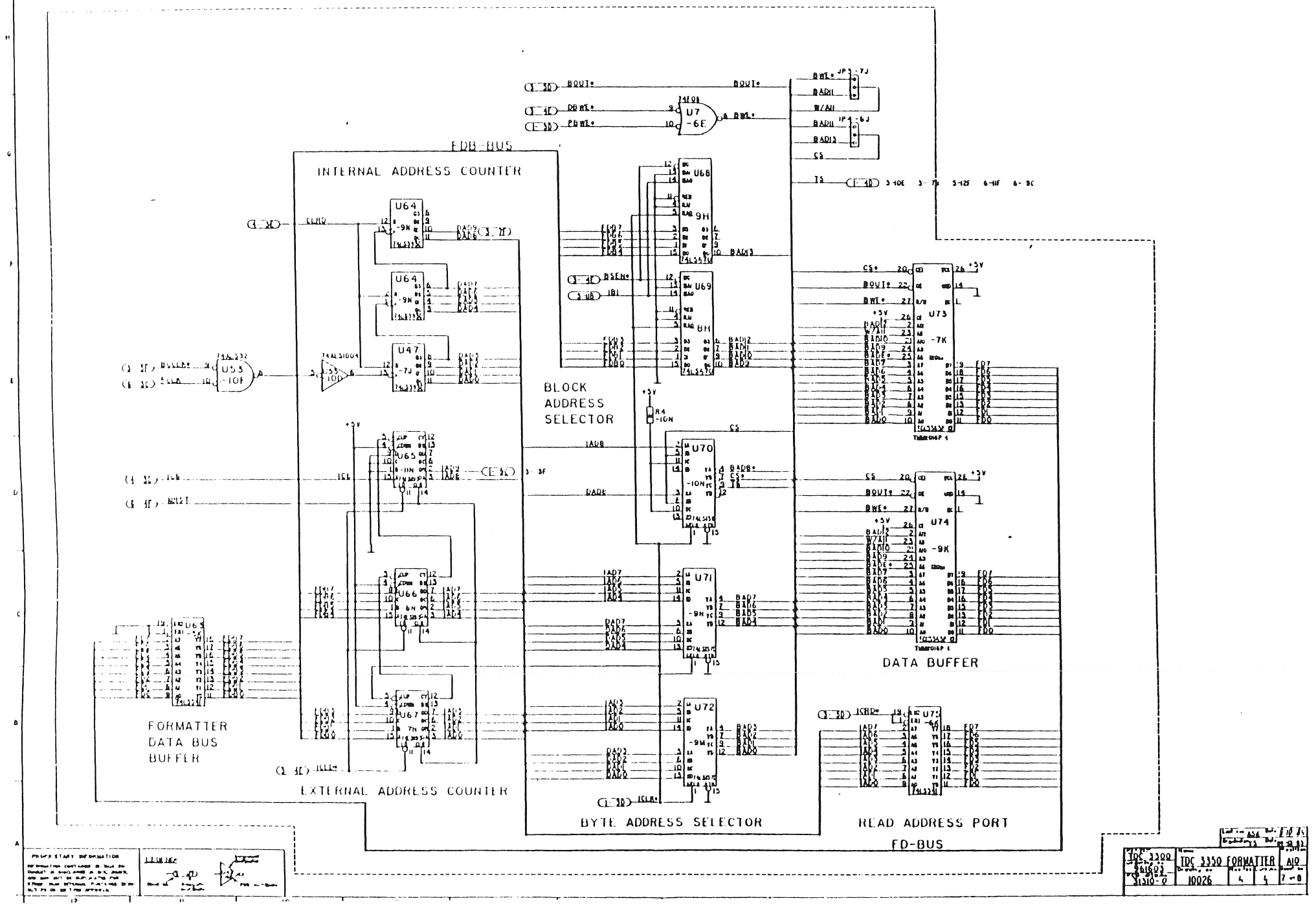


IDC 3300	IDC 3350 FORMATTER		A10
10026	4	4	7 - 8

Sheet 8

MASTER OSCILLATOR

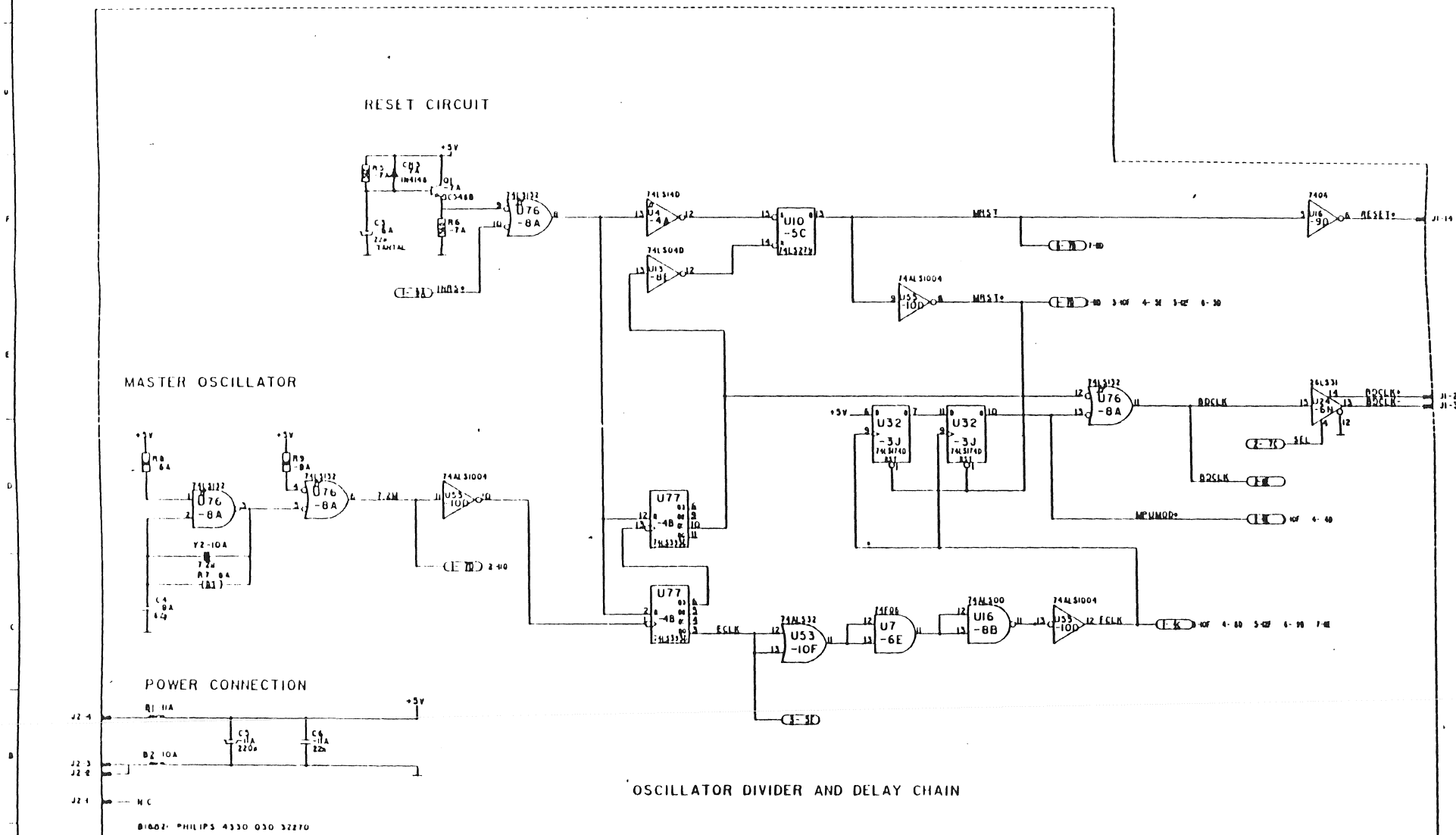
Crystal controlled at 7.2 MHz.

RESET CIRCUIT

A power-up condition or an INRS* pulse from host will cause a master pulse, MRST*.

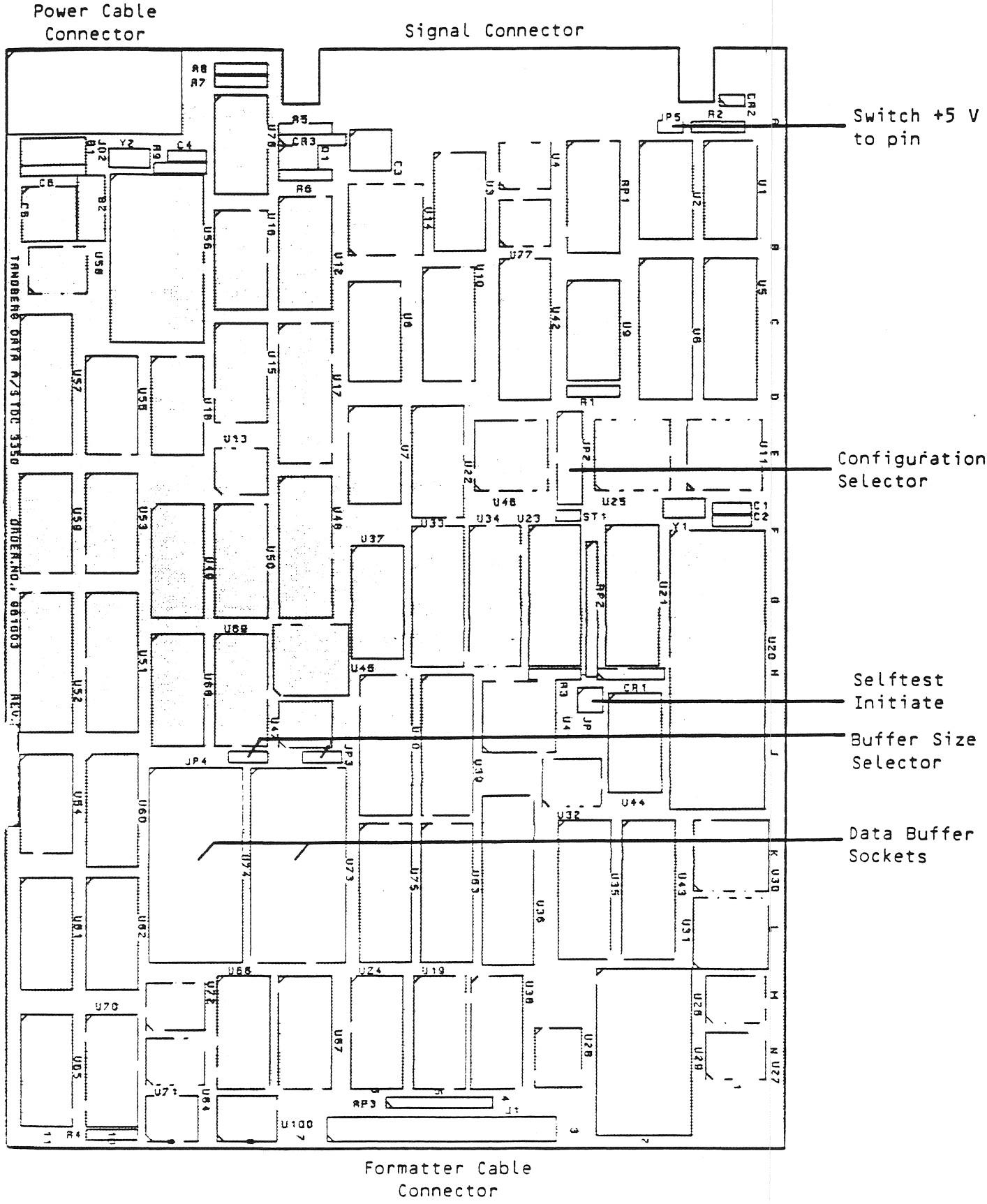
OSCILLATOR DIVIDER AND DELAY CHAIN

Derives various clock signals through division



IDC 3300	IDC 3350 FORMATTER		A10
10026		4	4

7.2 Formatter Board Component Location



7.3 Formatter Board Mnemonics List

The mnemonics refer to the schematic diagrams for the Formatter Board. A "*" following a signal denotes the inverted signal.

MNEMONIC	FUNCTION
7.2M	7.2 MHz System Clock
8K-RAM*	8K Data Buffer Devices
AB 0-7*	Accumulator Bus (bit 0-7)
ACCE*	Accumulator Enable
ACEN*	Accumulator Buffer Enable
ACK*	Acknowledge
AD 0-7	ALU Data Output Bus (bit 0-7)
BAD 0-13	Data Buffer Address Bus (bit 0-13)
BC 0-2	Bit Counter (bit 0-2)
BCCLK*	Byte Counter Clock
BDCLK	Baud Rate Clock
BDCLK+	Baud Rate Clock (positive line)
BDCLK-	Baud Rate Clock (negative line)
BLK	Block End Detected
BOUT*	Data Buffer Output Enable
BSEN*	Block Selector Write Enable
BWE*	Data Buffer Write Enable
CB 0-7	Operand Data Bus (bit 0-7)
CLRD	Clear Internal Address Counter
CNA	Read Sequencer Control (bit 0)
CNB	Read Sequencer Control (bit 1)
CNC	Read Sequencer Control (bit 2)
COMEN*	Command Enable
COMM+	Command to Basic Drive (positive line)
COMM-	Command to Basic Drive (negative line)
CONFEN*	Configurate Enable
CRCD	CRC Data
CRCER	CRC Error
CRCLK*	CRC Clock
CRCPR*	CRC Register Preset (write sequencer)
CS	Data Buffer Chip Enable (positive logic)
CS*	Data Buffer Chip Enable (negative logic)
DA	Read Sequencer Data (bit 0)
DAD 0-9	Internal Address Counter Output (bit 0-9)
DB	Read Sequencer Data (bit 1)
DB 0-7	Communication Processor Data Bus
DBWE*	Data Buffer Write Enable
DC	Read Sequencer Data (bit 2)
DD	Read Sequencer Data (bit 3)
DDCN	512 Bytes Read to/Written from Data Buffer
DEN*	Data Port Enable
DI	Read Sequencer Data Input
DIR*	Direction
DIRS	Direction
DLD*	Data Load
DTA 0-7	Communication Processor Data Bus (bit 0-7)
DTAP	Data Bus Parity Bit
DTEN*	Data Transfer Enable
DWLD	Data Word Load

MNEMONIC	FUNCTION
ECLK	Early Formatter System Clock (3.6 MHz)
EM	Write Fifo Empty
EN1*	Input enable Fifo Buffer
EN2*	Input enable Fifo Buffer
EONL*	Enable Online (strobe signal)
EXC*	Exception
FCLK	Formatter System Clock (3.6 MHz)
FD 0-7	Formatter Data Bus (bit 0-7)
FDB 0-7	Buffered Formatter Data Bus (bit 0-7)
FULL	Write Fifo Full
HB 0-7	Host Bus (bit 0-7)
HBP	Host Bus Parity Bit
IAD 0-9	External Address Counter Output (bit 0-9)
IB 0-7	Instruction Bus (bit 0-7)
IC8	External Address Counter, Loadable Bit 8
ICLD*	Load External Address Counter
ICLK*	External Address Counter Clock
ICRD*	Read Least Significant Nibble of External Address Counter
INRS*	Internal Reset
IREN*	Instruction Register Enable
JMPE*	Jump Enable
LAMP	Lamp Enable
LDFIF*	Load Read Fifo
LIREN*	Latched IREN*
LONL	Latched ONL (online)
LSN*	Least Significant Nibble
MPUMOD*	MPU Mode Select
MRST	Master Reset (positive logic)
MRST*	Master Reset (negative logic)
MSN*	Most Significant Nibble
NIBBLE	Nibble
NRDY*	Not Ready
ONL*	Online
OR	Read Fifo Data Output Ready
ORS	Read Fifo Data Output Ready, Synchronized
P 0-11	Program Counter, Current Address
PACK*	Early ACK (acknowledge)
PBOUT*	Read from Data Buffer
PBWE*	Data Buffer Write Enable
PCEN	Program Counter Enable
PERR*	Parity Error
PLD*	Load Program Counter
PLDRD*	Load Transmitter Register
PM 0-7	Prdgram Memory Data Bus (bit 0-7)
POUT*	Read Operand Latch
PWDEN*	Receiver Register Write Enable

MNEMONIC	FUNCTION
RA	Read Fifo Data (bit 0)
RAM*	Scratch Pad RAM Output Enable
RB	Read Fifo Data (bit 1)
RC	Read Fifo Data (bit 2)
RCA	Write Fifo, Read Address (least significant bit)
RCB	Write Fifo, Read Address (most significant bit)
RCLK	Read Clock
RCLK+	Read Clock (positive line)
RCLK-	Read Clock (negative line)
RCLKD*	Read Clock delayed
RD	Read Fifo Data (bit 3)
RD*	Ready
RDATA	Read Data
RDATA+	Read Data (positive line)
RDATA-	Read Data (negative line)
RDBLK	Read Block End Detected
RDBT*	Read One Byte from Read Fifo Buffer
RDEN	Read Sequencer Enable
RDFORM*	Read Data from Formatter
RDRDY*	Read Data Nibble is Ready
RDS*	Read from System Status Port
RDY*	Ready
RDYS	Reset Ready
REG*	Write into System Control Latch
REQ*	Request
RESET*	Reset
RFMK	Filemark Detected During Read
RP 1-8	Read Sequencer PROM Output
RRSTS*	Reset Read Status (equals RDEN)
RST*	Reset (from host)
RSTS*	Synchronized RRSTS*
S	CRC Register Preset (read sequencer)
SDATA	Serial Data to CRC Generator (read sequencer)
SEL	Formatter Select
SELFT*	Initiate Selftest
SEXC*	Exception
SFMK	Set Filemark Mode
SINGL*	Single Byte Transmission
SLONL	Synchronized and Latched ONL (Online)
SRD*	Synchronized Ready
SRDY*	Set Ready
STAT+	Status from Basic Drive (positive line)
STAT-	Status from Basic Drive (negative line)
STFEN	Synchronized TFEN (transfer enable)
STFER	Synchronized TFER (transfer)
SWE*	Scratch Pad RAM Write Enable
TFEN	Transfer Enable
TFER*	Transfer (from host)
TPDS*	Data from Formatter to Communication Processor
TPFACK*	TPFS Acknowledge
TPFS*	Data from Communication to Formatter Processor
TS	Test Signal
TSTR*	Transfer Enable

MNEMONIC	FUNCTION
W/A11	Data Buffer Write Enable/Data Buffer Address Bit 11
WCA	Write Fifo Write Address (least significant bit)
WCB	Write Fifo Write Address (most significant bit)
WCLK	Write Clock
WCLK+	Write Clock (positive line)
WCLK-	Write Clock (negative line)
WCLKS	Write Clock Synchronized
WD 0-3	Write Fifo Data Bus (bit 0-3)
WDATA	Write Data
WDATA+	Write Data (positive line)
WDATA-	Write Data (negative line)
WDLD*	Word Load
WEEN+	Write Enable (positive line)
WEEN-	Write Enable (negative line)
WFMK	Write Filemark
WFMKC*	Write Filemark Control
WLD*	Word Load
WM0	Write Data Sequencer Mode (least significant bit)
WM1	Write Data Sequencer Mode (most significant bit)
WRFORM*	Write to Formatter Processor
WRT	Write
WRTEN	Write Enable
WRTT*	Write Selftest
ZERO	Accumulator Zero Detector
ZERO*	Accumulator Zero Detector

7.4 Formatter Board Parts List

Comp. Designator	Part no.	Description	Qty.
Capacitors			
C1, C2	323693	22 pF cer. 1 2 % 63 V 2222 638 40229	2
C3	381637	22 uF tantalum 16 V	1
C4	381393	470 pF cer. 2 10 % min. 50 V	1
C5	398986	220 uF ELKO +/-20 % RE (F) 16 V	1
C6	359232	0.022 uF MA 105 E 223 MAA	1
Diodes			
CR1, CR3	384841	1N 4148	2
CR2	392758	31 CQV 31 E LED	1
Resistors			
R1, R4, R8, R9	403127	1 kohm met. film 1 %	4
R2	400447	180 ohm met. film 1 %	1
R3, R7	404198	470 ohm met. film 1 %	2
R5	403249	56 kohm met. film 1 %	1
R6	400569	560 kohm met. film 1 %	1
RP1	345388	220 ohm package 2 %	1
RP2	387851	1 kohm package 4310R-101-SIL	1
RP3	400272	100 ohm package 8-pin 5 %	1
Circuits			
U1, U2, U3	291115	7438/7438 A	3
U4	404353	74LS14D	1
U5, U6	401722	74LS540	2
U7	391659	74F08	1
U8, U53	402337	74ALS32	2
U9	400092	74LS280N	1
U10	382966	74LS279N	1
U11, U25, U46	402915	74LS374D	3
U12	403176	74ALS109	1
U13	402357	74LS04D	1
U14, U31, U45	401392	74LS273D	3
U15	403510	74ALS74	1
U16	401441	74ALS00	1
U17	961626	TDC 3350 I/O-ware	1
U18	384604	7406N (only TEXAS)	1
U19	389518	26LS32	1
U21, U35, U42, U43, U63, U75	393585	74LS541	6
U22, U37	404402	74F138	2
U23, U57	353945	74LS273N	2
U24	389166	26LS31	1
U26, U27, U28	402565	74LS161D	3
U29	961621	TDC 3350 FP-ware	1
U30, U41	402007	74LS377D	2

8. MAINTENANCE

8.1 Service Philosophy

It is assumed that deep surgery on the TDC 3319 will not be performed in the field. The first task there is to find out if the fault is in the system or in the TDC 3319. If it is in the drive, the most likely to happen is that 1) The Formatter board is changed, 2) The Basic Drive is changed, or 3) The whole TDC 3319 is changed.

Changing other modules will involve some adjustments, and are therefore easier to perform at the service shop.

8.2 Selftests

The three processors in the TDC 3319 add up to a lot of intelligence. We have used this opportunity to build in selftesting and adjustment possibilities.

Three different types of selftest procedures can be executed:

- The power-up selftest
- The manually activeted selftest
- The host activated selftest

How to activate the selftests and interpret the results of them, indicated by the front LED, is shown in section 8.4.

The selftests are extensively described in the "TDC 3319 Reference Manual".

8.3 Power-up Selftests

Each time power is turned on, both the processor in the Basic Drive and the processor on the Formatter board run through a selftest procedure that mainly tests the PROM contents, the RAM and some digital circuitry surrounding the two processors.

The Basic Drive uses the front LED as follows:

Steady green:	Drive OK
Steady red:	Power-up selftest failed. The drive is not selectable from the host.

When the Basic Drive has successfully performed a power-up selftest, the formatter normally takes control and sets the red LED to indicate that the Exception line to host is activated.

A successful formatter power-up selftest switches on the LED at the back of the Formatter board. Failure results in an unlit LED.

Comp. Designator	Part no.	Description	Qty.
Circuits cont.			
U32, U58, U100	401058	74LS174D	3
U33	961627	TDC 3350 FI-ware	1
U34	961628	TDC 3350 SI-ware	1
U36	404825	2015 TMM 2015 AP 12	1
U38	349922	74LS151N	1
U39, U40	401107	74LS382	2
U44	391552	74LS33D	1
U47, U64, U77	401673	74LS393D	3
U48	961622	TDC 3350 RW M-ware	1
U49, U50, U68, U69	390610	74LS670	4
U51	961624	TDC 3350 SI-ware	1
U52	961623	TDC 3350 WD-ware	1
U54, U59	346007	9401 PC	2
U55	404683	741004 74 ALS 1004	1
U56	390546	Circuit 2732 250 n.sec.	1
U60	402833	74LS224	1
U61, U62	360554	74LS173 AN	2
U65, U66, U67	352192	74LS193N	3
U70	353247	74LS158N	1
U71, U72	403530	74LS157D	2
U76	375417	74S132N	1
Assorted			
B1, B2	401326	Core 43303032270 (5x1.5x10 mm)	2
J1	390603	826632-2 two straight rows 2x3-pin	1
J2	402666	172294-1 4-pin M/172296-1 AMP	1
JP1	403742	826632-2 two straight rows 2x2-pin	1
JP2	391717	826632-3 two straight rows 2x3-pin	1
JP3, JP4	390574	826629-3 one straight row 1x3-pin	2
JP5	385503	826629-2 one straight row 1x2-pin	1
Q1	386436	Transistor 548 BC 548 B RL	1
XU17, XU33, XU34, XU48, XU51, XU52	392378	0-641602-3 IC 20-pin Diplomate	6
XU20	393707	0-641606-3 IC 40-pin Diplomate	1
XU29, XU56	390345	0-641604-3 IC 24-pin Diplomate	2
XU73, XU74	392026	0-641605-3 IC 28-pin Diplomate	2
Y1	389569	Crystal 4.00 MHz NC-18/C paral.res.	1
Y2	399338	Crystal 7.2 MHz NC-18/C serial res.	1
650	397233	Black knot on Formatter box	1

8.4 Manually Activated Selftests

The purpose of the manually activated selftest-procedures is mainly to act as diagnostic tools for the field-service technician. There is one selftest for the Basic Drive and one for the Formatter with the Basic Drive(s) connected.
Hint: If you have verified that the fault is in the drive, not somewhere else in the system, first use the selftest switches on the formatter to check the TDC 3319. Then activate the selftest on the Basic Drive (with disconnected Formatter).

Basic Drive Selftest

The selftest procedure for the Basic Drive will be performed according to the prevailing cartridge status:

a) If no cartridge is present in the drive, the capstan motor servo system is tested. The motor is run at 4 different speeds: 90 ips, 45 ips, 90 ips minus 10%, and 45 ips minus 10%. The correct speed is determined by counting tachometer pulses.

b) If a write protected cartridge is inserted in the drive, the tape is first rewound to BOT, then the capstan-motor test described above is performed, and then the tape is rewound to BOT again.

c) If a cartridge that is not write protected is inserted in the drive, the tape edge seek procedure is added to the test described above. The tape is rewound to BOT when the manually generated selftest is completed.

Formatter Board Selftest

There are two formatter selftest procedures:

- The first one follows points a) and b) above. A cartridge must be inserted, but it is irrelevant whether it is protected or not.

- The second, and most extensive of the two, follows point c), but with this addition: Following the tape edge seek procedure, it writes for five seconds forward on track 0, then for five seconds in reverse on track 1. Both patterns are 60 hex, the number of rewrites are limited to four per block.

The LED on the front of the drive lights steadily green during the test. It is turned off after a successful test, and lights red if the test failed.

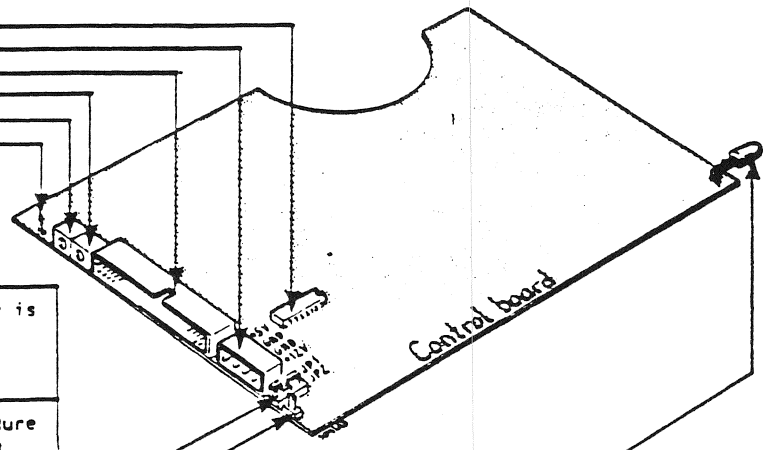
How to Activate the Selftests Manually

CONTROL BOARD

RP1: Termination resistor
Power connector
Basic drive signal connector
45 ips speed adjust; 1478 pulses per second (+/-2 %)
90 ips speed adjust; 2955 pulses per second (+/-2 %)
Tacho pulse test pin

Select Selftest type or adjustment procedure by setting the Drive Select jumpers JP1 and JP2. Activate tests manually by short circuiting Selftest jumper JP3.

Drive select jumper position		Drive address selected	Action when the test jumper is activated
JP1	JP2		
OPEN	OPEN	1	Basic drive selftest procedure
CLOSED	OPEN	2	Adjust head position switch
OPEN	CLOSED	3	Adjust capstan speed to 45 ips
CLOSED	CLOSED	4	Adjust capstan speed to 90 ips



JP3: Manual Selftest jumper

FRONT LED ON BASIC DRIVE INDICATES SELFTEST RESULTS:

Colour	Activated from JP3 (Control board)	Activated from JP1 (Formatter board)
Steady red:	Test in progress.	Test failed
Blinking green:	Test OK.	-
Blinking red:	Test failed.	-
Steady green:	Drive returned to normal operation.	Test in progress

FORMATTER BOARD

Selftest is activated by short circuiting the two rightmost pins on JP1. If the test is OK, the LED (see above) will return to normal setting.

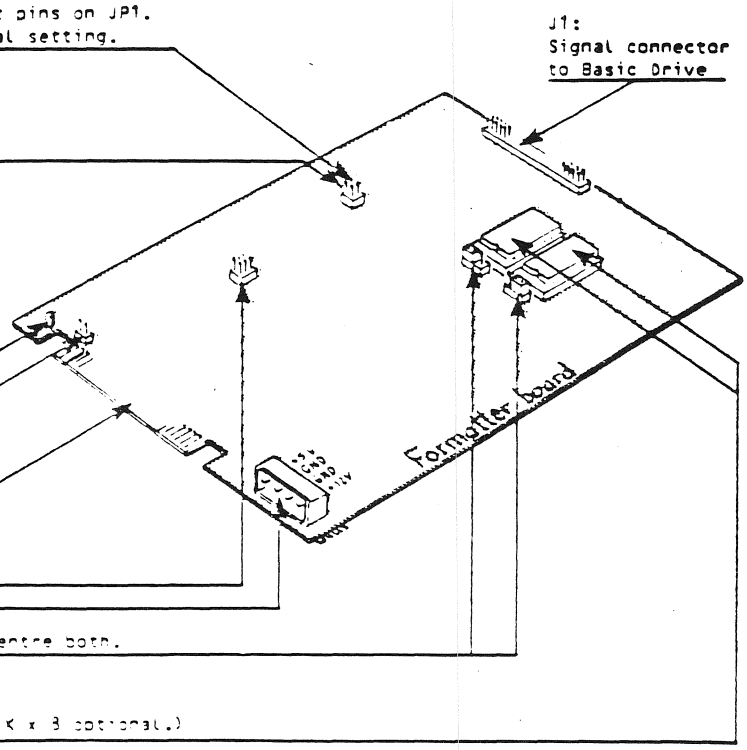
To perform an extensive Read/Write test, short the leftmost pins on JP1 and make sure that a not write protectedcartridge is inserted.

J1: Signal connector to Basic Drive

Red LED (CR2) lights when the formatter power-up Selftest is completed and the result is OK. If it does not light, the test failed.

JP5: +5 V when shorted.
Signal connector.
JP2: Pins 1 and 2: Inserted = parity enabled.
Pins 3 and 4: Reserved.
Pins 5 and 6: 8 K RAM buffer installed.
Power connector.
JP3/JP4: Select buffer size; 2 K or 8 K.
Jumper position for 2 K buffers shown; for 8 K centre both.

U73/U74:
Data buffer sockets. 2 K x 8 standard in each circuit. (8 K x 8 optional.)



8.5 Host Activated Selftest

Two software controlled selftests are available for the system designer who designs system-test software. The Selftest 1 command starts a limited selftest procedure. The Selftest 2 command performs a comnpre-hensive test of the capstan motor servo system and the head moving system, provided that an unprotected cartridge is inserted.

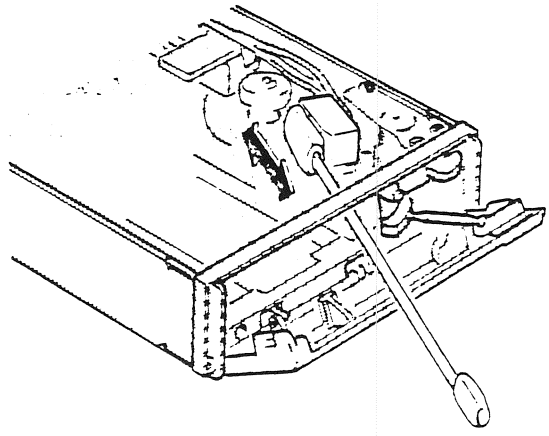
8.6 Head Cleaning

Isopropyl alcohol and cotton-tipped sticks are recommended for head cleaning. A cleaning kit, 3M's CK-90, that contains the necessary things, is available from Tandberg Data. The kit has ordering number 961536.

> IMPORTANT!
> Use no sharp objects when cleaning the head.
> Even small scratches may damage the head permanently.

The cleaning interval depends on three main factors:

1. How much the drive is used
2. The quality of the tape
3. The quality of the environment



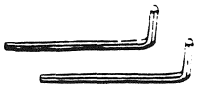
However, the following can be used as a recommended guideline:

Usage	Clean
Eight hours a day	Daily
Daily	Weekly
Weekly	Monthly

NOTE: Always clean the head immediately after using a new cartridge. And remember, it is better to clean too often than too seldom!

8.7 Necessary Hand Tools

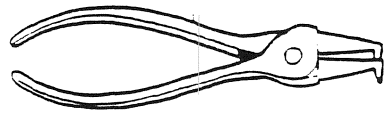
The list below shows the hand tools that are required to replace the spare modules of the drive.



1.5 mm and 2.0 mm Allen keys.

Small pozidrive screwdriver.

Tweezers.



Special pliers for removing retaining rings (circlips).

8.8 Diagnostic Tools

To locate faults on the printed circuit boards, you'll need an oscilloscope and a multimeter.

Two test boards are available from our Service Department:

- A Basic Drive test interface that enables external equipment to control the Basic Drive directly (without the TDC 3350 Formatter). Command and status information can be exchanged via a standard V.24 (RS-232) or V.11 (RS-422) interface. The test interface can also supply two simple test data patterns.
  Appendix 1 and 2 contain summaries of the commands and status bytes of the Basic Drive.

  The test interface has ordering number 961635.

- A test board, with LEDs that monitor the eight control lines. The test board plugs into the Formatter board. These LEDs, together with the red/green LED in the cartridge door, indicate where to look for malfunctioning circuits.

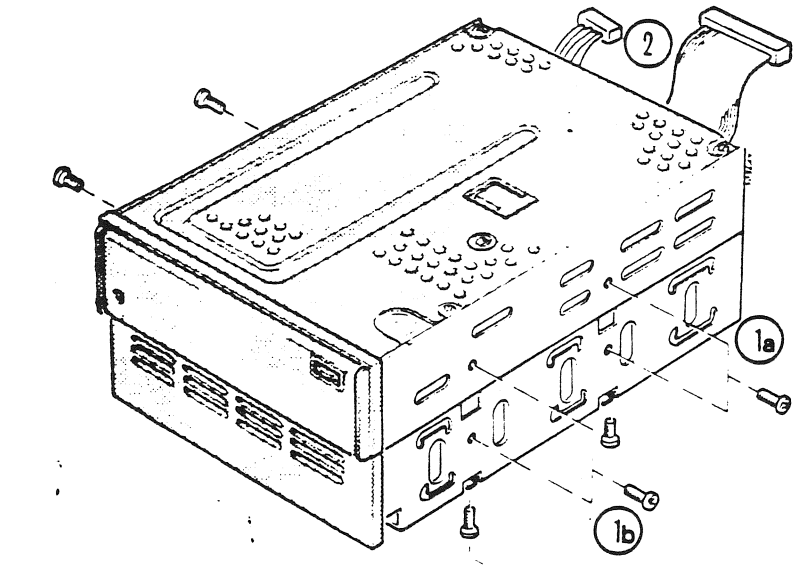
  The test board has ordering number 961533.

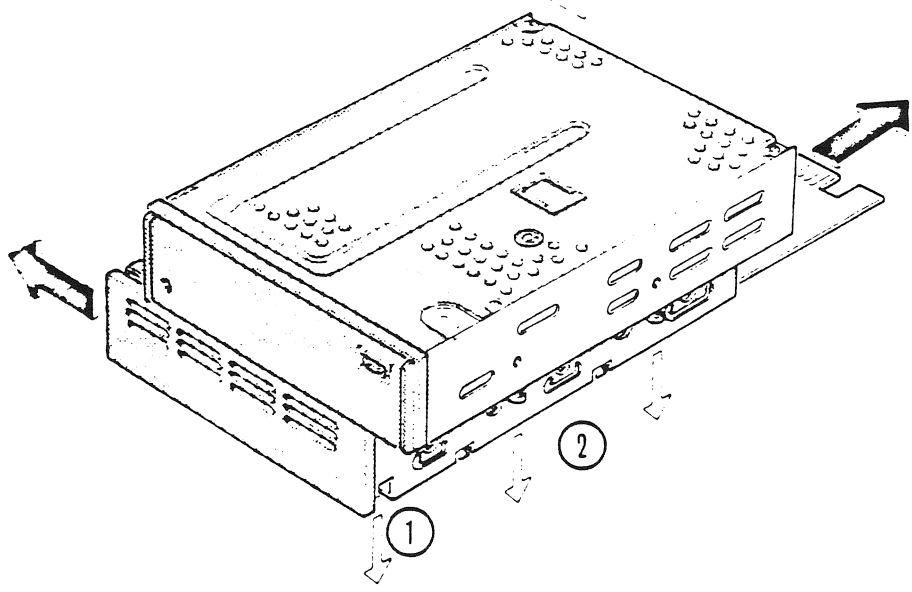
8.9 Adjustments

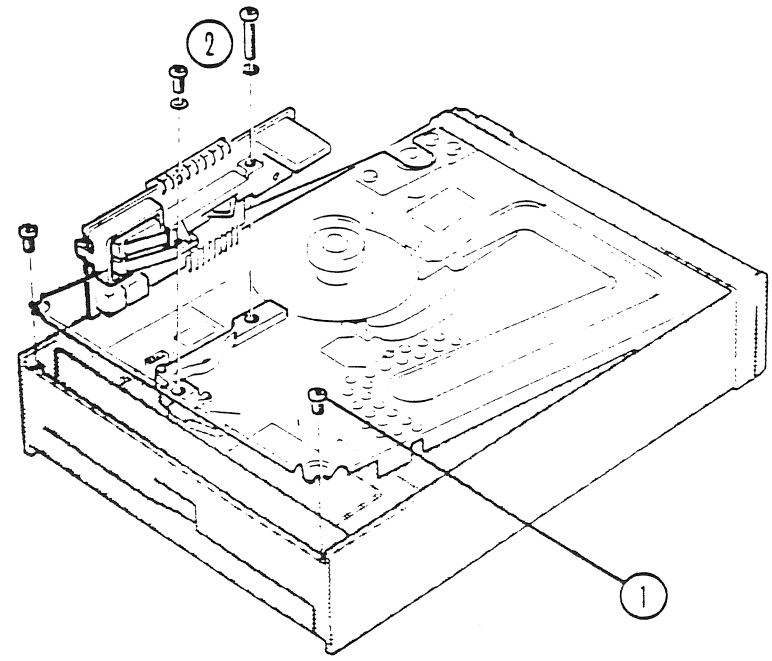
The table below shows the various adjustments of the drive, their corresponding potentiometers and testpoints, and under which chapter they are described.

ADJUSTMENT	POTMETER, TEST POINT/CHAPTER
Tape Speed	R16, R19, TP1/Control board, sheet 1
Write Current	R72, WCUR line/Control board, sheet 3
Read Channel Gain	R5, R6, TP2-2/Read board
Head Switch Screw	S1, set screw on head platform/Control bd., sheet 2
Erase Balance	R87, TP2-2 on Read board/Control board, sheet 3
Sensor Sensitivity	R2, U1-5; R3, U1-3/Sensor board

9. HOW TO CHANGE THE DIFFERENT MODULES







NOTE! Some of the module exchanges require subsequent mechanical or electrical adjustments. All adjustments are described briefly in chapter 8 and in detail under their correspond board description.

9.1 Removing the Drive

1. Take out the 4 mounting screws either from the drive (1a) or the formatte box (1b).

2. Unplug the signal cable an the power cable.

9.2 Removing the Formatter B from the Drive

1. Loosen the screw, then pul the Formatter board out.

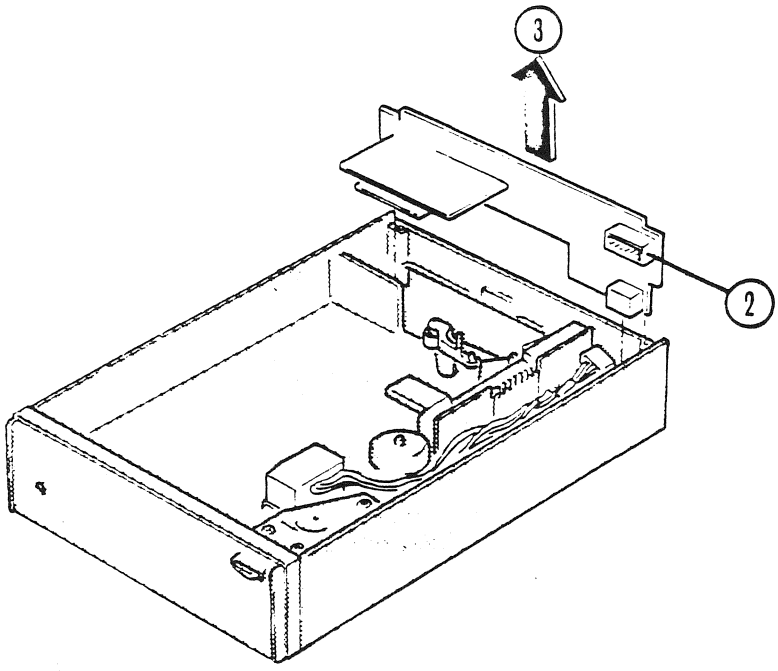
2. Loosen the 4 screws. Lift and slide the box off sideways.

9.3 Changing the Sensor Boar

1. Remove the top cover.

2. Remove the 2 screws in the Sensor board. Pull the board straight out of the plug on the Control board.

3. Check that the two sensors work properly. It may be necessary to readjust R2 and R3.

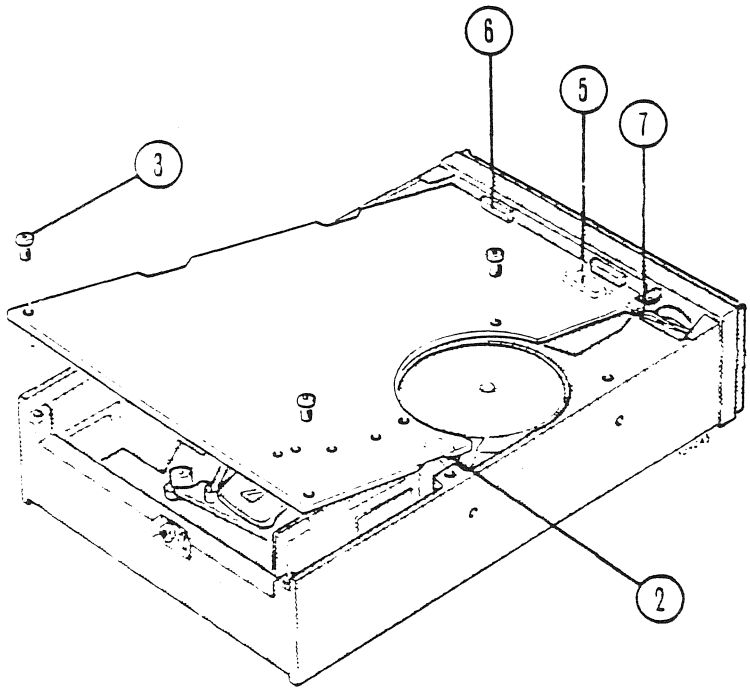


9.4 Changing the Read Board

1. Remove the top cover.
2. Unplug the head cable on the Read board.
3. Pull the board straight up.

NOTE! Don't use the hybrid board as a handle.

4. The gain control (R5/R6) must be adjusted if a new board is installed.



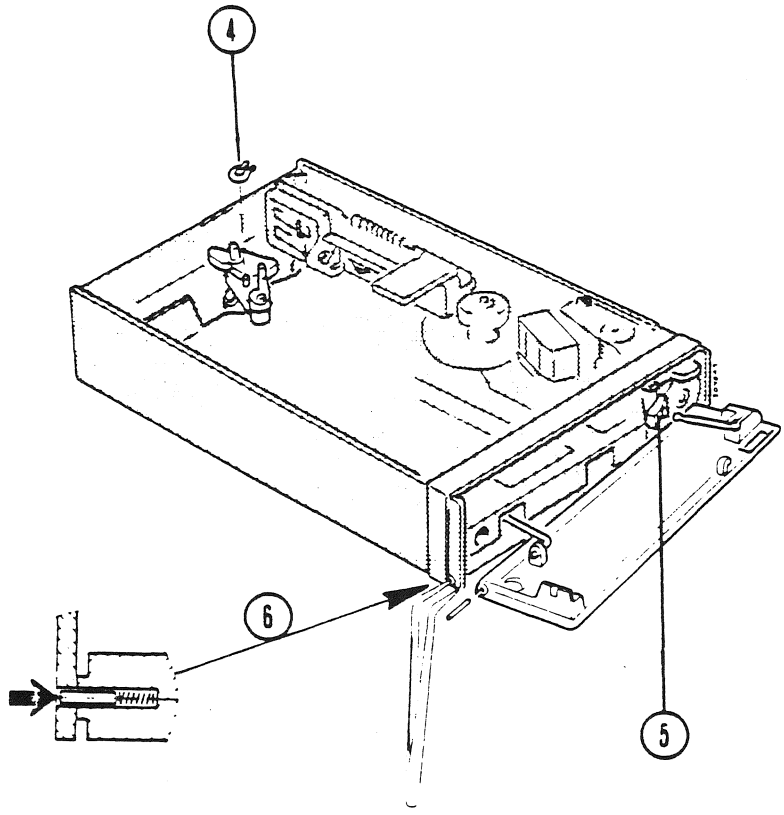
9.5 Changing the Control Board

1. Remove the Read board.
2. Disconnect head- and capstan tacho cables.
3. Remove the 3 screws as shown.
4. Lift the board out and disconnect the remaining cables.

Replacing the board:

5. Plug in the stepper motor cable.
6. Place board edge under the knobs on the casting.
7. Avoid getting the stepper motor cable caught between board and casting.
8. Plug in all cables and replace the boards.

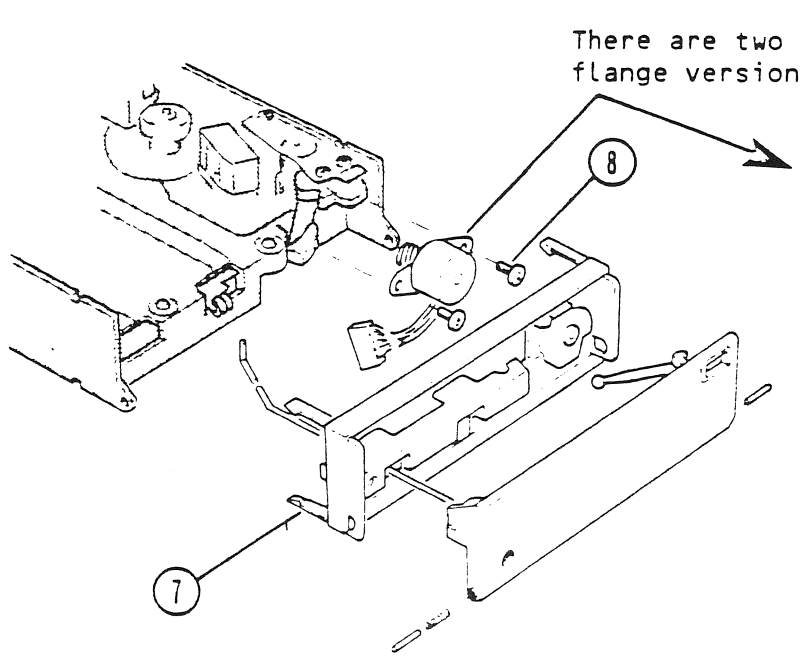
NOTE! If the same Control board has been taken out and put back in, adjust only the "head bottom switch". If a new Control board has been installed, adjust both the "head bottom switch" and Erase Balance. Control Capstan Speed and Write Current.

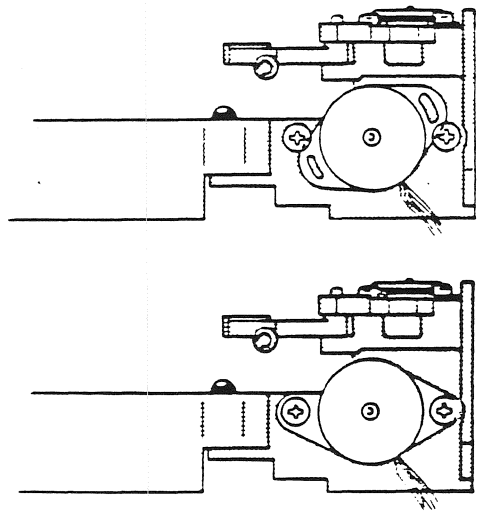


9.6 Changing the Stepper Motor

1. Remove the formatter box.
2. Remove the top cover.
3. Remove the Control board.
4. Remove the circlip from the rod.
5. Hold the cartridge locking arm and pull the ball joint out of its socket.
6. Push in the spring-loaded door axle with tweezers. Remove the door. BEWARE OF FLYING SPRING AND AXLES!

7. Disengage 4 hooks to remove the front frame.
8. Loosen the screws and pull the motor out.

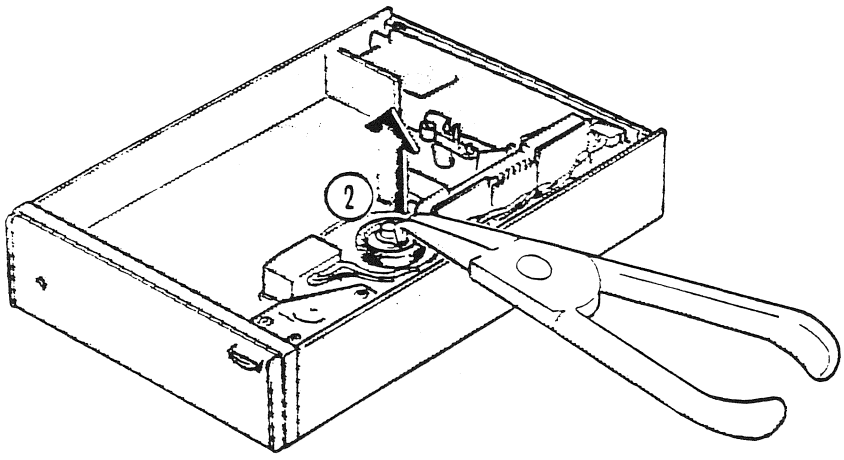




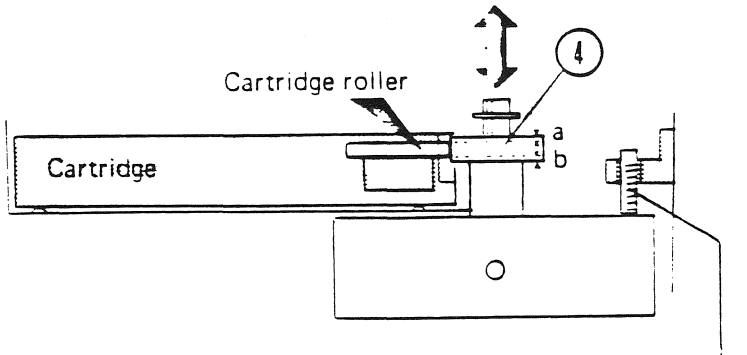
NOTE! Ensure correct orientation of the cable when replacing the motor. Check that the door moves freely when everything has been reassembled.

9. Adjust the Head Switch.

9.7 Changing the Capstan Wheel

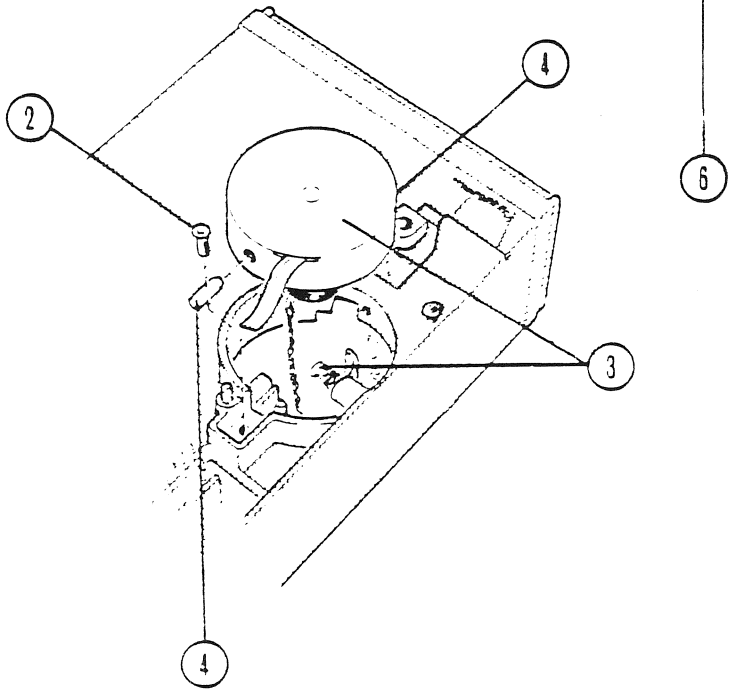


1. Remove the top cover.
2. Remove the retaining ring and pull the capstan wheel straight up.
3. Replace the capstan wheel.

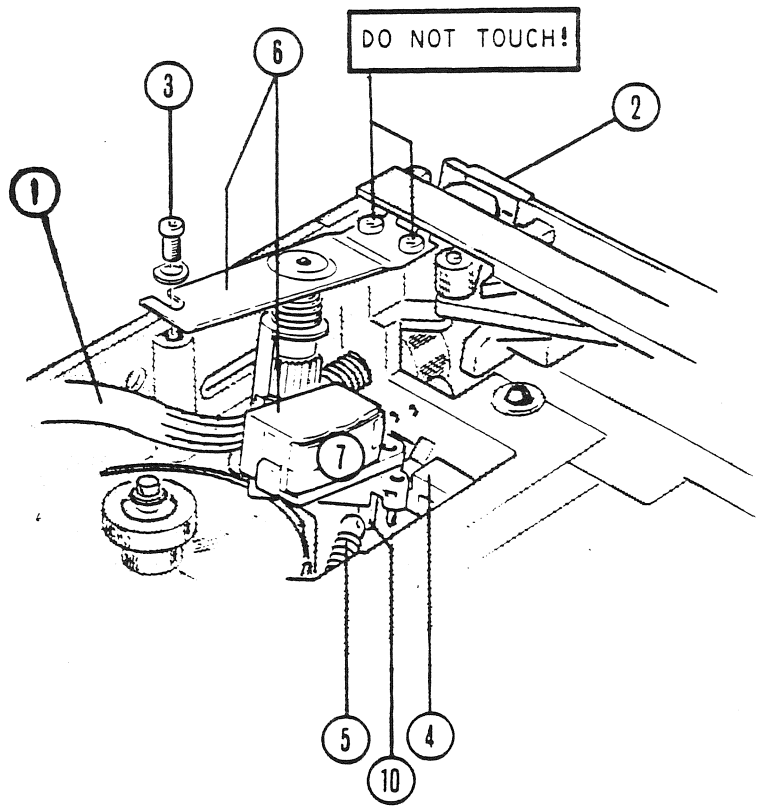


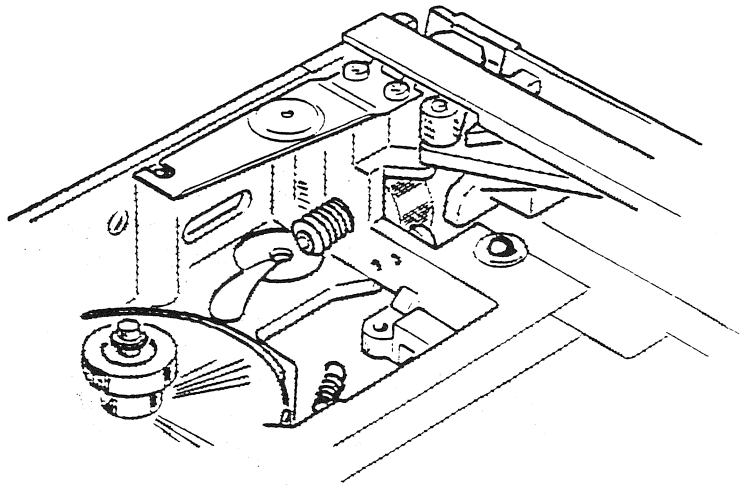
4. Insert a cartridge and adjust the capstan wheel so that it covers the cartridge roller (a and b > 0).

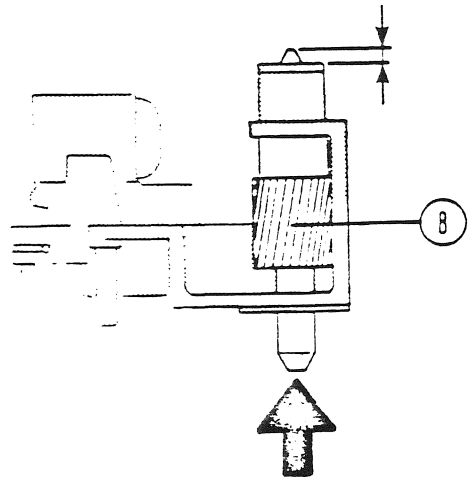
9.8 Changing the Capstan Motor



1. Remove the Control board.
2. Remove the screw that holds the axle.
3. Pull the motor out gently. Ensure that the spring that presses against the hub of the motor stays in place.
4. When replacing the motor, make certain that the pivot ball enters its recess.
5. Check that the motor tilts easily with no axial play in the pivot bearing.
6. If a new motor is installed, turn the set screw (use the 2.0 mm Allen key) clockwise until the capstan wheel lifts from the cartridge roller. Then turn 1/2-turn back.







9.9 Changing the Head Assembly

REMOVE THE CONTROL BO

Removing the Head Assy:

1. Unplug the head cables.
2. Open the door slightly.
3. Remove 1 screw from the spring plate.
   DO NOT TOUCH THE OTHER TWO SCREWS!
4. Bend the arm down.
5. Unhook the spring from the head platform.
6. Whilst bending the leat spr up, lift and pull out the h assembly. Slight force may necessary.
7. DO NOT DAMAGE THE NEW HEAD FRONT! KEEP WELL PROTECTED

Replacing the Head Assy:

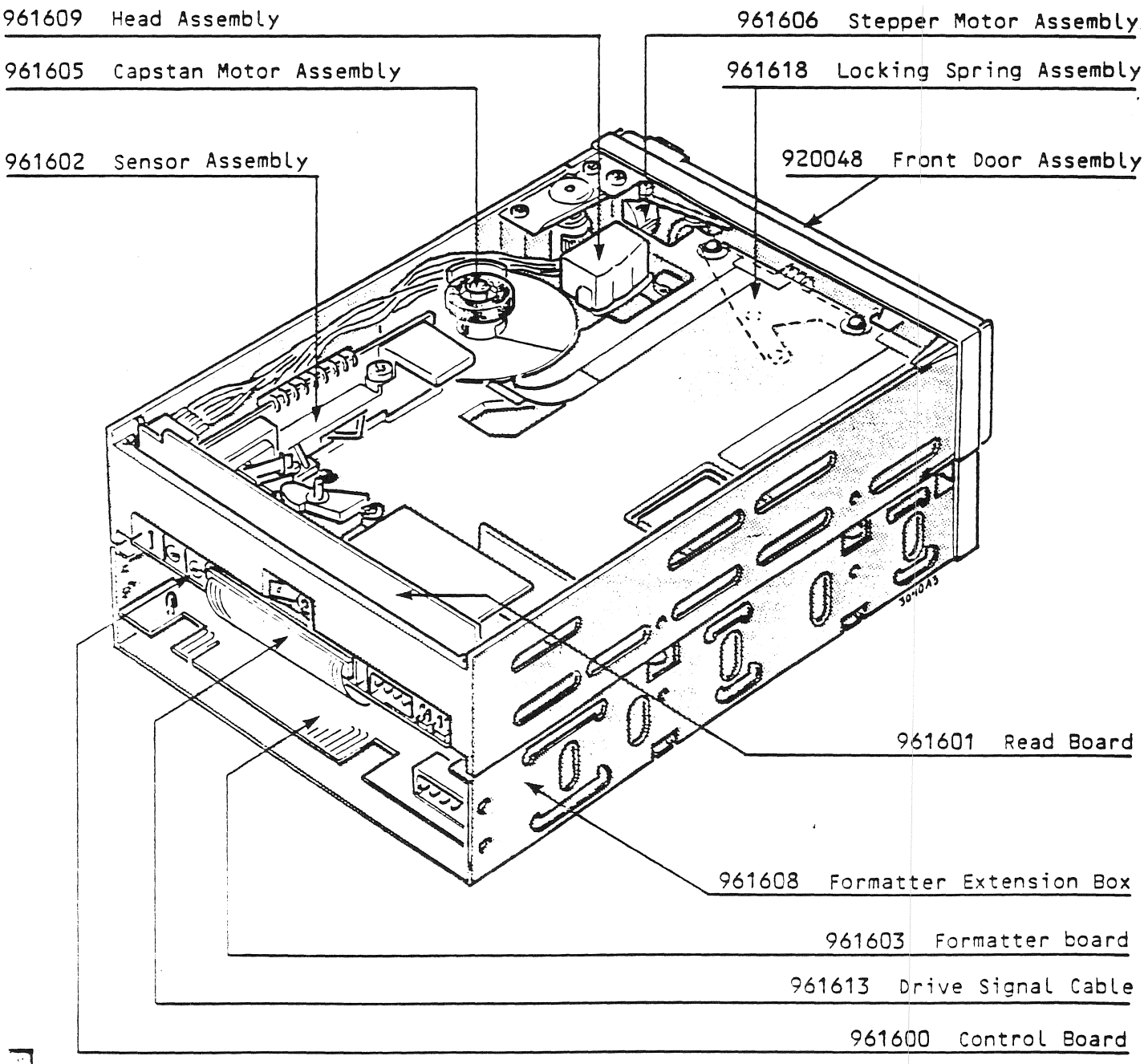
8. Press vertical axle upwards and turn cogwheel until onl the conical part of the axl is visible on top.
9. Compress the axle spring with the tweezers and wriggle assembly back in place, top of axle into hole first.
10. Replace arm (4) on head pla form pin.
11. Replace spring (5), washer and screw (3), and cable connectors.
12. Degausse and clean the head.
13. Adjust the Head Switch and Erase Balance.

10. SPARE MODULE LIST

Only complete spare modules (assemblies) are shown in this illustration. Complete parts lists for each printed circuit board are included in the individual descriptions of each board.

A comprehensive list, with prices, of spare mechanical and electrical parts, and some accessories, is available from our Service Department.

When ordering, please specify ordering number and full name of the required part.



APPENDIX 1. TDC 3300 BASIC DRIVE COMMAND SUMMARY (QIC-44)

MNEMONIC	COMMAND CODE	FUNCTION
SEL	00 - 03	Select Drive 0 - 3
	04	Deselect All Drives
EDGE	21	Seek Reference Track
	22	Seek Tape Edge
	23	Recalibrate Head Servo
TRACK	40 - 48	Seek Track 0 - 8
MOVE	60	Stop Tape
	61	Move Tape Forwards (Logically)
	62	Move Tape Revers (Logically)
	63	Rewind to BOT
	64	Tape Rentension
	65	Return to Reference Point
TEST	81	Selftest 1 (Capstan test)
	82	Selftest 2 (1 + Seek Edge)
	85	Head Switch Adjust
	86	45 ips Speed Adjust
	87	90 ips Speed Adjust
RSTAT	A1 - AF	Read Status Byte 1 - 15
CNFIG	C0	No Write, No Erase
	C1	Erase, No Write
	C2	Write, No Erase
	C3	Write and Erase
	C4	Position Head to Track Senter
	C5	Position Head 1/4 Track up
	C6	Position Head 1/4 Track down
	C9	Adjust Head 15 Steps Up
	CA	Adjust Head 15 Steps Down
	D0 - DF	Set Tape Reference Offset Distance
MISC	E0	Lamps Off
	E1	Red Lamp On
	E2	Green Lamp On
	E3	Red and Green Lamp On
	E4	Set Tape Speed Normal
	E5	Set Reduced Speed 10 %
	E6	Set Tape Position Reference Point

APPENDIX 2. TDC 3300 BASIC DRIVE STATUS BYTE SUMMARY

#	TYPE	BIT NUMBER	
1	Tape Position	2 - 0 :	0 = Unknown 1 = Position < BOT 2 = BOT < Position < LP 3 = LP < Position < EW 4 = EW < Position < EOT 5 = EOT < Position 6 = RUNOUT
2	Drive Selection	1 - 0 :	Drive Number 0 - 3
3	Drive Speed	2 - 0 : 3 :	1 = 30 ips 2 = 45 ips 3 = 60 ips 4 = 90 ips Speed reduced 10 %
4	Cartridge Status	1 - 0 : 2 : 3 : 4 : 5 :	0 = 450' tape (or don't know) 2 = 600' tape Cartridge has been inserted Cartridge has been removed Cartridge write protected Cartridge not in place
5	Drive Status	0 : 1 : 2 : 3 : 4 : 5 :	Power-up/reset occured Head Servo error Capstan error Edge/reference not detected ACLEV from read channel Sensor error
6	Tape Format/Head	2 - 0 : 5 - 4 :	0 = 4-track tape 1 = 9 track tape $10 = 4-track head $20 = 9-track head
7	Head Position	4 - 0 :	Track Number 0 - 8
8	Head Off-center	1 - 0 :	0 = On-center 1 = Off-center upwards 2 = Off-center downwards 3 = Track position unknown
9	Reserved		
10	Reserved		
11	Tape Reference	1 - 0 :	0 = No Reference Point Set 1 = Valid Reference Point Set 2 = Illegal to set ref. Point 3 = Illegal to set ref. Point
12	Drive Config.	0 : 1 : 2 : 3 :	Erase mode Write mode Red Lamp On Green Lamp On
13	Reserved		
14	Firmware Ident.	5 - 0 :	Firmware Code
15	Firmware Revision	5 - 0 :	Firmware Revision Level

COMMAND STATUS BYTE	3 - 0 : 5 : 6 :	Error Code 0 - 15 Communication Error Illegal Command

INTERRUPT STATUS BYTE	5 - 0 :	$80 = Cartridge inserted $82 = BOT detected $83 = LP detected $84 = EW detected $85 = EOT detected $8A = Erased tape detected $A0 = Cartridge removed $A6 = Tape runout $A8 = Sensor error $A9 = Capstan error